

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNITED MICROELECTRONICS CORPORATION,
AND
UMC GROUP (USA),
Petitioner,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,
Patent Owner.

Case IPR2025-01079
U.S. Patent No. 7,923,764

**DECLARATION OF DR. SANJAY BANERJEE IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,923,764**

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Declaration of Dr. Sanjay Banerjee
Inter Partes Review of U.S. Patent No. 7,923,764

I, Dr. Sanjay Banerjee, declare as follows:

1. My name is Sanjay Banerjee.
2. I have been retained as an expert witness on behalf of United Microelectronics Corporation and UMC Group (USA) (collectively, “Petitioner”) for the above-captioned Petition for *Inter Partes* Review (“IPR”) (“Petition”) of U.S. Patent No. 7,923,764 (“the ’764 patent”) (Ex.1001). I am being compensated for my time in connection with this Petition at my standard consulting rate of \$675 per hour. My compensation is not affected by the outcome of, or my testimony in, this IPR, or any litigation proceedings. I am informed that the assignee for the patent in the present proceeding is Advanced Integrated Circuit Process LLC (“Patent Owner”). I am also informed that the Petition names United Microelectronics Corporation and UMC Group (USA) as real-parties-in-interest.
3. I have been asked to provide my opinions regarding whether claims 1-6 and 11-19 of the ’764 patent (the “Challenged Claims”) are invalid as anticipated, or as obvious to a person having ordinary skill in the art at the time of the alleged invention of the ’764 patent (“POSITA”).
4. The ’764 patent issued on April 12, 2011, from U.S. Patent Application No. 12/505,799, filed on July 20, 2009. The ’764 patent claims priority to Japan Patent Application No. 2005-227457, filed on August 5, 2005.

5. I am not currently, and have not at any time in the past been, an employee of any Petitioner or any real-party-in-interest. Other than set out above, I have no affiliation, contractual connection, or financial connection with any Petitioner or any real-party-in-interest, or any of their respective subsidiaries or parents. I similarly have no financial interest in, or affiliation with the Patent Owner.

I. BACKGROUND AND QUALIFICATIONS

6. I am currently the Cockrell Family Chair Professor of Electrical and Computer Engineering at the University of Texas at Austin. At UT Austin, I was also the director of the Microelectronics Research Center from September 1999 through January 2025. I have been a faculty member at UT Austin since 1987.

7. I have also been active in industries related to the relevant field of art. As a Member of the Technical Staff, Corporate Research, Development and Engineering of Texas Instruments Incorporated from 1983–1987, I worked on polysilicon transistors and dynamic random access trench memory cells used by Texas Instruments in the world’s first 4-Megabit DRAM, for which I was co-recipient of the Best Paper Award, IEEE International Solid State Circuits Conference, 1986.

8. I received a B. Tech. degree from the Indian Institute of Technology, Kharagpur, and M.S. and Ph.D. degrees from the University of Illinois at Urbana-Champaign, all in Electrical Engineering.

9. I am a leading researcher and educator in various areas of transistor device fabrication technology, including the fabrication, characterization and application of memory devices, transistors, and nanotechnology. My research has been funded by the Texas Advanced Technology Program (ATP), the Texas Higher Education Coordinating Board, the National Science Foundation, the SEMATECH (Semiconductor Manufacturing Technology) consortium, the SRC (Semiconductor Research Corporation) consortium, DARPA, and the Department of Energy, among others.

10. At the University of Texas, I served as the director of the South West Academy of Nanoelectronics from its inception through the end (2006 - 2017), one of three centers in the United States established to develop a replacement for MOSFETs.

11. I have published over 1,200 technical articles, many related to semiconductor fabrication technology, most at highly competitive refereed conferences and rigorously reviewed journals. I have also published 8 books or chapters on transistor device physics and fabrication, and have supervised over 80 Ph.D. and 60 MS students.

12. I have been a member of scientific organizations and committees, including the IEEE Dan Noble Award Committee from 2010–2013, serving as Chair from 2012–2013, the International Technology Roadmap for Semiconductors, the

International Conference on MEMS (Microelectromechanical Systems) and Nanotechnology, the IEEE International Conference on Communications, Computers, Devices, the International Electron Devices Meeting, the International Conference on Simulation of Semiconductor Processes and Devices, and the IEEE Symposium on VLSI (Very-Large-Scale Integration) Technology. I have served as the Session Chair for the “Device Technology” Session conducted at the IEEE International Electron Devices Meeting in 1989–1990. I have also served as the General Chairman for the IEEE University Government Industry Microelectronics Symposium in 1994–1995, and Chair of the IEEE Device Research Conference.

13. I have served on the Technical Advisory Boards of AstroWatt, DSM Semiconductors, Cambrios, Nanocoolers Inc., BeSang Memories, Organic ID and ITU Ventures; Gerson Lehmann Group, NY; Austin Community College; Asia Pacific IIT; Rochester Institute of Technology, and HSMC Foundry.

14. I received the Engineering Foundation Advisory Council Halliburton Award (1991), the Texas Atomic Energy Fellowship (1990–1997), Cullen Professorship (1997–2001) and the Hocott Research Award from UT Austin (2007). I also received the SIA/SRC University Researcher Award (2018), IEEE Grove Award (2014), Distinguished Alumnus Award, IIT (2005), Industrial R&D 100 Award (2004), ECS Callinan Award, 2003, IEEE Millennium Medal, 2000, NSF Presidential Young Investigator Award in 1988, and several SRC Inventor

Recognition and Best Paper Awards. I was a Distinguished Lecturer for IEEE Electron Devices Society, and am a Fellow of the Institute of the Electrical and Electronics Engineers (IEEE), the American Physical Society (APS) and the American Association for the Advancement of Science (AAAS).

15. I am the inventor or co-inventor of over 35 United States patents in various areas of transistor device fabrication technology. I was elected a Fellow of the National Academy of Inventors in 2021.

16. My qualifications and publications are set forth more fully in my curriculum vitae, attached as Ex.1102.

II. MATERIALS AND OTHER INFORMATION CONSIDERED

17. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art and have considered the viewpoint of a POSITA at the time of the alleged invention.

18. I have considered the materials referenced herein, including the '764 patent (Ex.1001), the file history of the '764 patent (Ex.1002), the parent and related applications, the file histories of the parent and related applications, the Petition, and other documents listed in the Exhibit List of the Petition, including:

Declaration of Dr. Sanjay Banerjee
Inter Partes Review of U.S. Patent No. 7,923,764

Description	Date of Availability
U.S. Patent Application Publication No. 2003/0025135 A1 to Matsumoto, et al. (“Matsumoto”; Ex.1009)	Published February 6, 2003
U.S. Patent Application Publication No. 2006/0131672 A1 to Wang, et al. (“Wang”; Ex.1012)	Filed April 27, 2005
Sim, J. H., et al., “Effects of ALD HfO ₂ thickness on charge trapping and mobility,” <i>Microelectronic Engineering</i> , Vol. 80, pp. 218-221, June 17, 2005 (“Sim”; Ex.1024)	Published June 17, 2005
U.S. Patent Application Publication No. 2005/0045938 A1 to Mutou, et al. (“Mutou”; Ex.1019)	Published March 3, 2005
U.S. Patent Application Publication No. 2005/0051856 to Ono, et al. (“Ono”; Ex.1013)	Published March 10, 2005
U.S. Patent Application Publication No. 2004/0110352 A1 to Bu, et al. (“Bu”; Ex.1025)	Published June 10, 2004
Wilk, G. D., et al., “High-k gate dielectrics: Current status and materials properties considerations,” <i>Journal of Applied Physics</i> , Vol. 89, No. 10, pp. 5243-5275, May 15, 2001 (“Wilk”; Ex.1018)	Published May 15, 2001
JP2003-258241 to Kajiyama (“JP-Kajiyama”; Ex.1010) (with Certified Translation (“Kajiyama”); Ex.1011)	Published September 12, 2003

19. It is my understanding that the references listed above are prior art to the '764 patent, which is entitled to a priority date not earlier than August 5, 2005.

Matsumoto, Wang, Sim, Mutou, Ono, Bu, Wilk, and JP-Kajiyama (Exs. 1009, 1012, 1024, 1019, 1013, 1025, 1018, and 1010/1011, respectively) were not discussed during the prosecution of the '764 patent.

III. UNDERSTANDING OF PATENT LAW

20. I am not an attorney. For purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law is as listed below.

A. Claim Construction

21. I understand that in an IPR petition filed after November 13, 2018, a claim must be construed under the *Phillips* standard. Under that standard, words of a claim are given their plain and ordinary meaning as understood by a POSITA at the time of invention, in light of the specification and prosecution history, unless those sources show an intent to depart from such meaning, as well as pertinent evidence extrinsic to the patent.

22. I have applied this understanding in my declaration. I do not believe any claim terms require explicit construction in this proceeding to resolve the patentability of the Challenged Claims.

B. Anticipation and Obviousness

23. I have been informed that a patent claim is anticipated if a single prior art reference, such as a patent or a publication, discloses all the limitations of the claimed invention.

24. I have been informed and understand that a patent claim can be considered to have been obvious to a POSITA at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a POSITA at the time the application was filed. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

25. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to a POSITA. In determining whether a

combination based on either a single reference or multiple references would have been obvious, I have been informed that it is appropriate to consider at least the following factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;
- whether a POSITA could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed limitations represent one of a limited number of known design choices, and would have a reasonable expectation of success by a POSITA;
- whether a POSITA would have recognized a reason to combine known limitations in the manner described in the claim;
- whether there is some teaching or suggestion in the prior art to make the modification or combination of limitations claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

26. I understand that a POSITA has ordinary creativity and is not an automaton.

27. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

28. I understand that prior art to the '764 patent for purposes of my opinion herein includes patents and printed publications in the relevant art that predate the priority date of the '764 patent.

29. I understand that certain factors—often called “secondary considerations”—may support or rebut an assertion of obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the alleged invention, skepticism of those having ordinary skill in the art at the time of the alleged invention, unexpected results of the alleged invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field.

30. I further understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

IV. SUMMARY OF OPINIONS

31. It is my opinion that claims 1, 4-5, and 14-19 are obvious in view of Matsumoto (Ground I).

32. It is my opinion that claims 2-3, 6, and 11 are obvious in view of Matsumoto and Wang (Ground II).

33. It is my opinion that claim 11 is obvious in view of a combination of Matsumoto, Wang, and Sim (Ground III).

34. It is my opinion that claims 2-3 are obvious in view of Matsumoto and Mutou (Ground IV).

35. It is my opinion that claims 6, 12, and 13 are obvious in view of Matsumoto and Ono (Ground V).

36. It is my opinion that claim 15 is obvious in view of Matsumoto and Bu (Ground VI).

37. It is my opinion that claims 18-19 are obvious in view of Matsumoto and Wilk (Ground VII).

38. It is my opinion that claims 1, 5, and 16-17 are anticipated by Kajiyama (Ground VIII).

39. It is my opinion that claims 4, 6, and 18-19 are obvious in view of Kajiyama (Ground IX).

40. It is my opinion that claim 11 is obvious in view of Kajiyama and Wang (Ground X).

41. It is my opinion that claim 11 is obvious in view of Kajiyama and Sim (Ground XI).

42. It is my opinion that claims 12-13 are obvious in view of Kajiyama and Ono (Ground XII).

43. It is my opinion that claims 14-15 are obvious in view of Kajiyama and Bu (Ground XIII).

44. It is my opinion that claims 18-19 are obvious in view of Kajiyama and Wilk (Ground XIV).

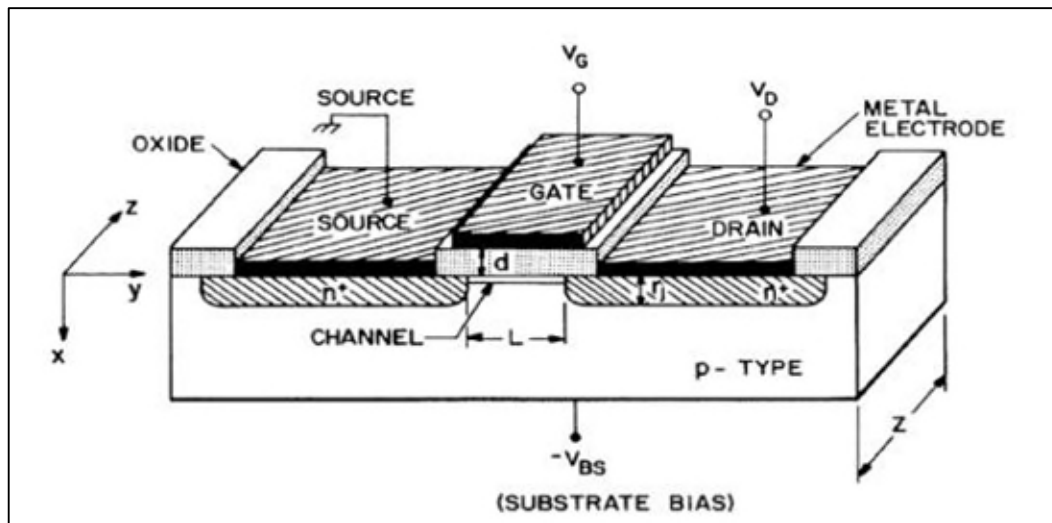
V. OVERVIEW OF THE TECHNOLOGY

45. Broadly speaking, a semiconductor device is an electrical device made of semiconductor material like silicon or germanium. This includes many types of devices like light-emitting diodes (LEDs) and metal oxide semiconductor (MOS) transistors. Field effect transistors are just one type of semiconductor devices and have been in commercial use for decades, as discussed in more detail below.

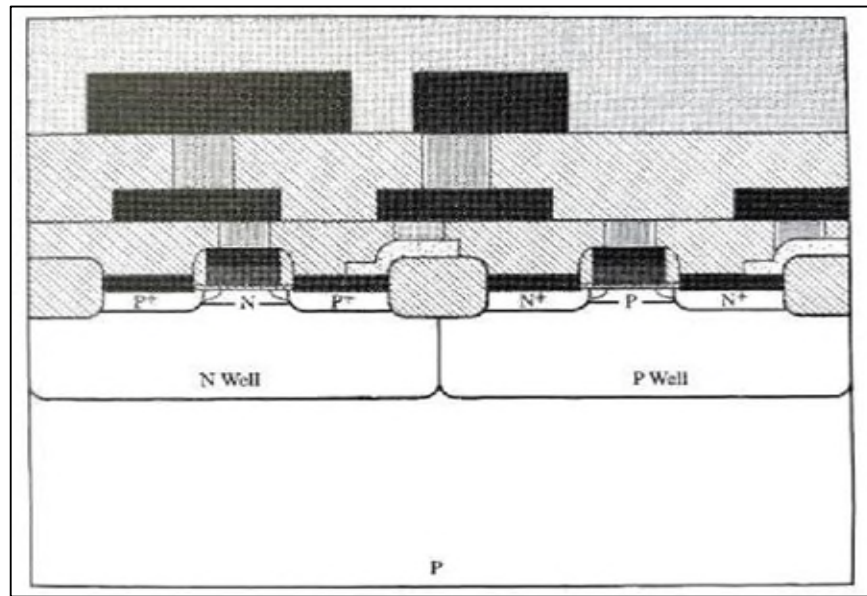
A. MISFET/MOSFET

46. A metal insulating semiconductor field-effect transistor (MISFET), commonly referred to as a metal oxide semiconductor field-effect transistor (MOSFET) if the insulator is an oxide, is a transistor that switches from an OFF state to an ON state

when a voltage greater than the threshold voltage is applied to a gate terminal. In the ON, or active state, current flows from a source to a drain through a channel region. For the transistor types at issue in this IPR, the channel region is located under the gate electrode (which can be made of stacked metal layers) and the gate insulating layer (often called a gate oxide or gate dielectric), and between the source and drain. Sze-1981, Ex.1413, 433-34, Fig. 3 (below); Plummer, Ex.1333, 71-76, Figs. 1-11 (further below).

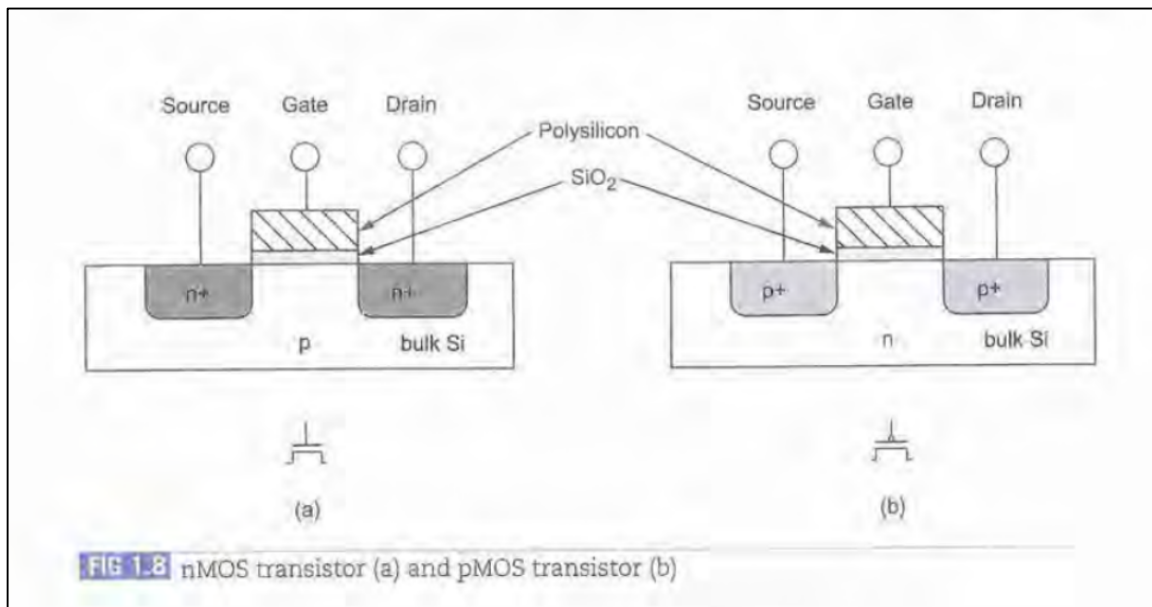


Sze-1981, Ex.1413, Fig. 3



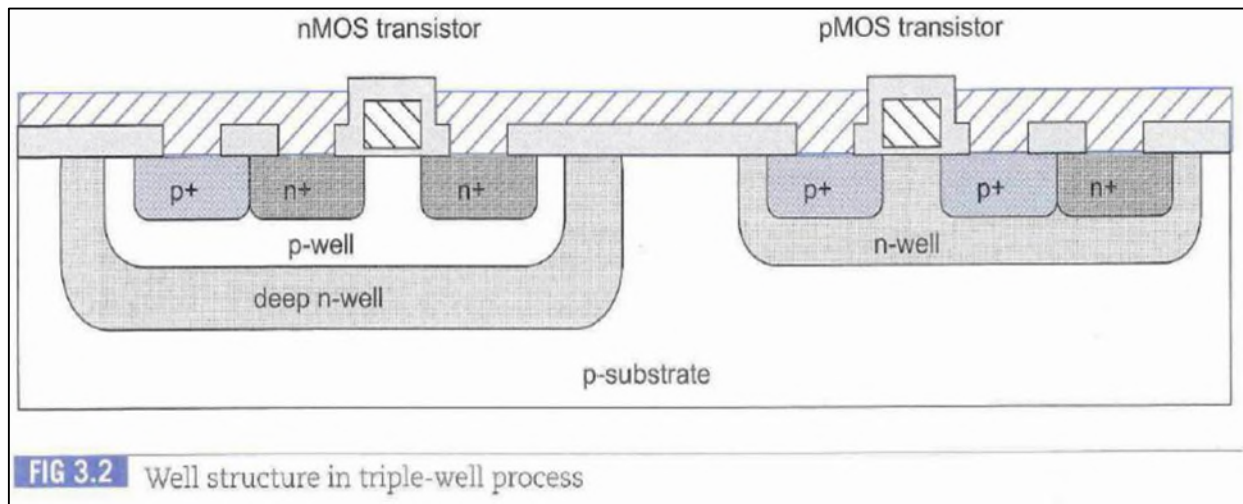
Plummer, Ex.1333, Fig. 1-11

47. MOSFETs are characterized by the material used in the source and drain. A MOSFET with source/drain regions made from “p-type” material is known as a PMOS or p-FET, while a MOSFET with source/drain regions made from “n-type” material is known as a NMOS or n-FET. Thus, MOSFETs generally include a gate electrode, a gate insulating layer, and “the silicon wafer, also called the substrate, body or bulk.” Weste, Ex.1341, 8. An nMOS transistor “is built with a p-type body and has regions of n-type semiconductor adjacent to the gate called the source and drain.” *Id.*, 8 (emphasis omitted), FIG. 1.8(a). A pMOS transistor “is just the opposite, consisting of p-type source and drain regions with an n-type body.” *Id.*



Id., 8, FIG. 1.8(b) (above, right).

48. In the mid-1980s, complementary MOS (CMOS) devices became popular, which have both PMOS (p-FET) and NMOS (n-FET) transistors on the same substrate or integrated circuit (IC). In such devices, the active areas (and associated transistors) are generally formed in regions called “wells,” and a transistor can even have more than one well, as seen below. See Weste, Ex.1341, 117-118, FIG. 3.2 (below).

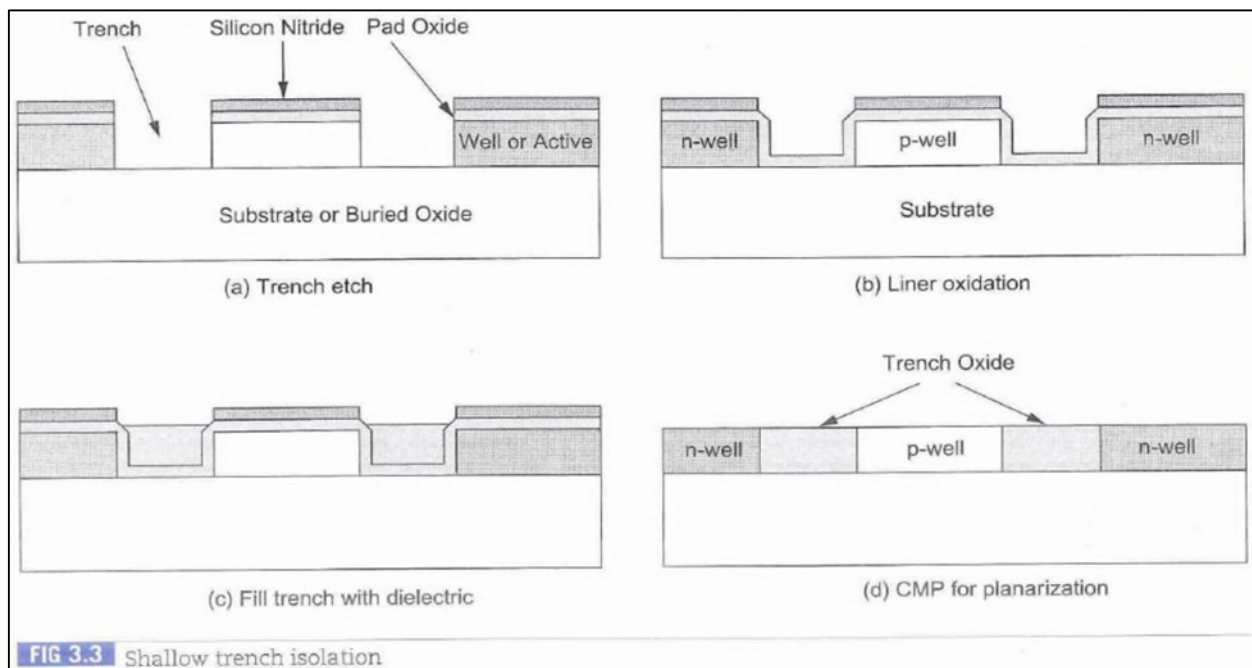


Weste, Ex.1341, Fig. 3.2

49. Impurities known as “dopants” are added to the active areas and wells to add charge carriers and tailor the electrical properties of these regions, such as their conductivity. The wells have opposite dopant types to the dopants of the source/drain. As such, an n-FET is formed in a p-well, and a p-FET is formed in an n-well. See Weste, Ex.1341, 8, FIG. 1.8(b).

50. With respect to dopants, charge carriers can be electrons (which are negatively charged) or holes (which are positively charged). When a region is doped with p-type dopants (like boron), the holes are majority carriers and the electrons are minority carriers. See Weste, Ex.1341, 7; Plummer, Ex.1333, 17. When a region is doped with n-type dopants (like arsenic), the electrons are majority carriers and the holes are minority carriers. See Weste, Ex.1341, 7; Plummer, Ex.1333, 17 (“The electrons or holes are introduced on a one for one basis by the dopants.”).

51. One issue with ICs relates to forming multiple devices on the same chip, and often it is necessary to isolate two structures from each other to ensure proper operation on the chip. One example of this isolation is forming a shallow trench isolation on the substrate between devices. *See Weste, Ex.1341, 117.* In the example below, a trench is etched between a p and n-well to form the shallow trench isolation. *Id.*, 119, Fig. 3.3 (below).



Weste, Ex.1341, Fig. 3.3

52. Once the dopants are added, or implanted, into the silicon substrate, they need to be annealed, for example to repair the silicon crystal lattice from any damage caused by the dopant implantation. Plummer, Ex.1333, 81-82. “Because the ion implantation process creates damage, most dopants are not electrically active at the end

of the implantation.” *Id.*, 470. A rapid thermal anneal, often at temperatures over 1000 degrees Celsius, can activate the dopants and repair some of the damage done by implantation. *Id.*, 81. Annealing can also cause diffusion of the implanted dopants throughout the substrate (and in certain circumstances, other layers of the device). The interaction of the implanted dopants between the source/drain, the gate electrode and the gate insulating layer, and the channel were all well understood by a POSITA long before the priority date of the challenged patents. In fact, a POSITA would often use the various interactions of the manufacturing process, for example the shape of the source/drain after dopant implantation and annealing, to improve and optimize the performance of the semiconductor device, as discussed further below.

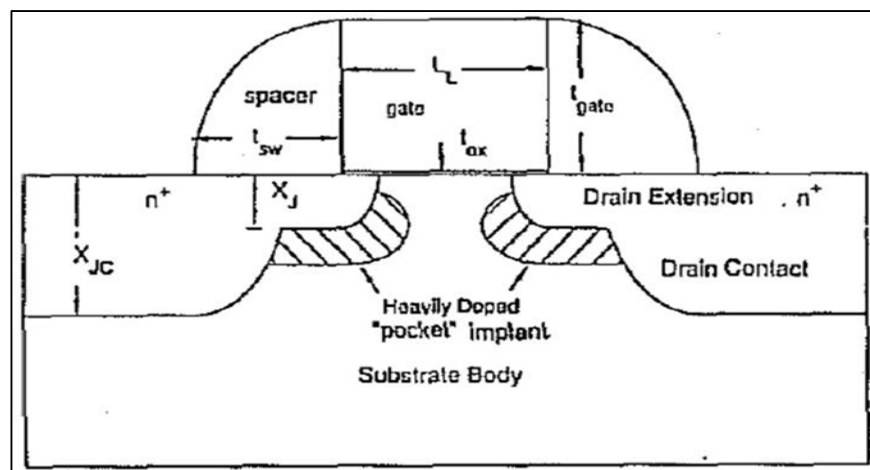
53. For example, varying the amount of dopants at different positions in the semiconductor device can have significant impacts on the device’s performance. Where a source/drain may be heavily doped, other areas may only be lightly doped. As one example, the prior art has recognized that as transistors continue to scale down in size, using source and drain extensions may provide certain benefits, and these extensions can have varying dopant levels, including what are commonly referred to as lightly doped drain (LDD) and highly doped drain (HDD). Plummer, Ex.1333, 77; Rodder, Ex.1323, 2:61-62, 3:65-67.

54. Source/drain extensions were known to assist in suppressing short channel effects of scaled-down transistors by varying the dopants and having a gradual

transition in the electrical field between the source, the source extension, the channel, the drain extension, and the drain. Plummer, Ex.1333, 77-78 (using a LDD “allows the drain voltage to be dropped over larger distance than would be the case if an abrupt N^+P junction were formed” and even “modest reductions in the field strength obtained through the LDD structure can make a significant difference in device reliability”).

55. As I discuss further below, sidewall structures placed on the edge of gate electrodes can serve many purposes, including to control the shape and position of source/drain extensions after annealing of the implanted dopants, as well as the overlap of the extension regions and the gate/gate insulating film. See Plummer, Ex.1333, 78.

56. As another example of varying dopants, the prior art also taught using pocket or halo implants to further mitigate the short channel effect as transistor sizes decreased. Pocket implants are placed below the channel region, as shown below. Wolf-4, Ex.1334, 219-20, Fig. 5-27 (below).



Wolf-4, Ex.1334, Fig. 5-27

57. In this example, the pocket implants are doped opposite of the source/drain and source/drain extension. Wolf-4, Ex.1334, 219 (“Precise control of the placement and dose of this implant within the transistor-structure is needed to obtain the intended enhancements.”).

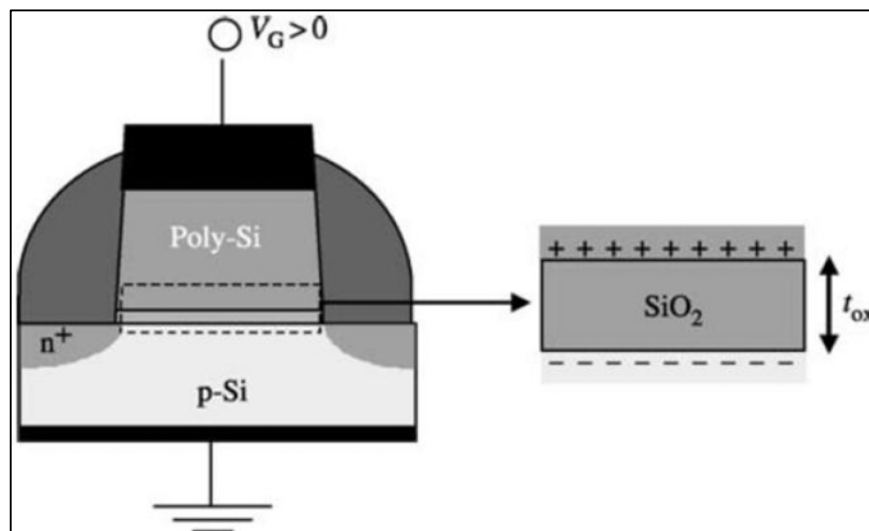
B. Gate Insulating Films & High-k Materials

58. The gate insulating film or gate dielectric isolates the gate electrode from the channel. Plummer, Ex.1333, 288. Silicon dioxide was primarily used as the gate dielectric material for many years (*id.*, 53), but silicon dioxide films presented problems when reduced in thickness for smaller and smaller transistors. In particular, “in ultrathin SiO₂ gate layers (thickness typically below 3 nm) charge carriers can flow through the gate dielectric by quantum mechanical tunnelling mechanism.” Houssa, Ex.1213, 5; *see also* Wolf-4, Ex.1334, 4-5.

59. The MOS transistor, from an electrical perspective, “behaves like parallel plate capacitor when gate voltage V_G is applied to the gate charges on the metal are compensated by opposite charges in the semiconductor, these latter charges forming the channel connecting the source and the drain of the transistor as illustrated in figure 1.1.4.” Houssa, Ex.1213, 8, Fig. 1.1.4 (below). The capacitance C can thus be represented by the following equation:

$$C = \frac{A\epsilon_r\epsilon_0}{t_{ox}} \quad (1.1.1)$$

60. In this equation, “A is the capacitor area, ϵ_r the relative dielectric constant of the material (3.9 for SiO_2), ϵ_0 the permittivity of free space ($8.85 \times 10^{12} \text{ F m}^{-1}$) and t_{ox} the gate oxide thickness.” Houssa, Ex.1213, 8. From this formula, the gate oxide thickness has an inverse relationship to capacitance: decreasing the gate oxide thickness increases the capacitance of the structure, with a corresponding “increase in the number of charges in the channel for a fixed value of V_G .” *Id.*



Houssa, Ex.1213, Fig. 1.1.4

61. In practical uses, however, problems occur when decreasing the gate oxide thickness of silicon dioxide past a certain point. Houssa, Ex.1213, 8. As one prior art textbook proposed, “[a]n alternative way of increasing the capacitance is to use an insulator with a higher relative dielectric constant than SiO_2 (it should be noticed that the relative dielectric constant is also represented by the letter k and one speaks about high-k materials).” *Id.*, 8-9. “One could then use a thicker gate layer and, hopefully,

reduce the leakage current flowing through the structure and also improve the reliability of the gate dielectric.” *Id.*

62. Equivalent oxide thickness (EOT) is one measure of high-k gate dielectrics. The EOT of a high-k material “is defined as the thickness of the SiO₂ layer that would be required to achieve the same capacitance density as the high-k material in consideration” (Houssa, Ex.1213, 9), which can be represented by the following equation:

$$\frac{t_{eq}}{\epsilon_{r, SiO_2}} = \frac{t_{high-k}}{\epsilon_{r, high-k}} \quad (1.1.2)$$

63. In this equation, “ t_{high-k} and $\epsilon_{r, high-k}$ are the thickness and relative dielectric constant of the high-k material, respectively.” *Id.* In one example shown by Houssa, “using ZrO₂ as gate dielectric ($\epsilon_r \approx 20$) would allow us to use a 5.1 nm thick layer in order to achieve a capacitance equivalent to a 1 nm thick SiO₂ layer; the equivalent oxide thickness of this ZrO₂ layer is thus 1 nm.” *Id.*

64. But make no mistake, more than just a hope, the use of high-k gate dielectrics were a well-known, well-understood, and well-documented component to improve transistor performance as a substitute for silicon dioxide gate dielectrics, especially as transistors continued to decrease in size in the early 2000s. Long before 2005, numerous industry publications and other prior art readily recognized the advantages of using high-k materials as a gate dielectric.

65. In 2002, for example, numerous industry papers identified high-k materials, and hafnium oxide HfO_2 in particular, as a significant contributor to increased transistor performance. A paper by Rim et al. titled “Mobility Enhancement in Strained Si NMOSFETs with HfO_2 Gate Dielectrics” recognized that POSITAs had already been looking to high-k materials to solve known problems: “[g]ate leakage reduction in ultra thin gate dielectric is the main motivation for the search of high-k materials.” Rim-2002, Ex.1109, Introduction; *see also id.*, Conclusion (“Strained Si NFETs with high-k dielectrics exhibit significantly enhanced NFET mobility, even over the universal mobility of the SiO_2 /bulk Si devices, and hold the promise for the best trade-off between mobility and gate leakage reduction, which is especially attractive for low power, high performance CMOS technology.”). Another article at the same industry conference concluded that “[h]igh-temperature FG annealing improved channel carrier mobility as well as subthreshold slopes in both N and PMOSFET with HfO_2 gate dielectrics,” which are “advantageous in achieving large on current while suppressing off current, and give more flexibility in V_t adjustment.” Onishi-2002, Ex.1107, Conclusion.

66. Yet another article at the same conference by Pidin et al., titled “Low Standby Power CMOS with HfO_2 Gate Oxide for 100-nm Generation,” concluded that HfO_2 was particularly suited for low standby current applications. Pidin-2002, Ex.1108, Conclusion (“55-nm CMOS with 3-nm HfO_2 gate dielectric was fabricated using conventional process flow with high-temperature anneal of $\geq 1000^\circ\text{C}$ and cobalt silicide.

Gate current reduction of more than 3 orders of magnitude was achieved and low off-state current devices were obtained demonstrating very promising characteristics of HfO₂ for low standby current applications.”).

67. But more than just the structure and use of high-k materials, the industry had already begun optimizing the process for making transistors with high-k gate dielectrics, with one article from the 2002 VLSI Symposium comparing two gate first approaches using HfO₂, one via physical vapor deposition and another via chemical vapor deposition. *See* Lee-2002, Ex.1105, Conclusion (“Compared with PVD TaN devices, the CVD TaN/HfO₂ devices exhibit lower leakage current and CV hysteresis, superior interface properties, higher transconductance, and superior effective electron and hole mobility.”).

68. Numerous other prior art references recognized the ability of high-k gate dielectrics to make up for the shortcomings of too-thin silicon dioxide gate dielectrics. One article in the Journal of Applied Physics titled “High-k Gate Dielectrics: Current Status and Materials Properties Considerations” recognized that already by 2001 “much work has been done on high-k metal oxides as a means to provide a substantially thicker (physical thickness) dielectric for reduced leakage and improved gate capacitance.” Wilk, Ex.1018, 5250; *see also* Wolf-4, Ex.1334, 146-47 (“The use of high-k dielectrics as the gate dielectric in submicron MOSFET structures also improves other device characteristics,” including in threshold voltage V_t and in the subthreshold-swing S_t .”).

69. For example, as shown by Figure 5 below in Wilk, using high-k materials in place of silicon dioxide for the gate dielectric improved both power consumption and gate leakage current.

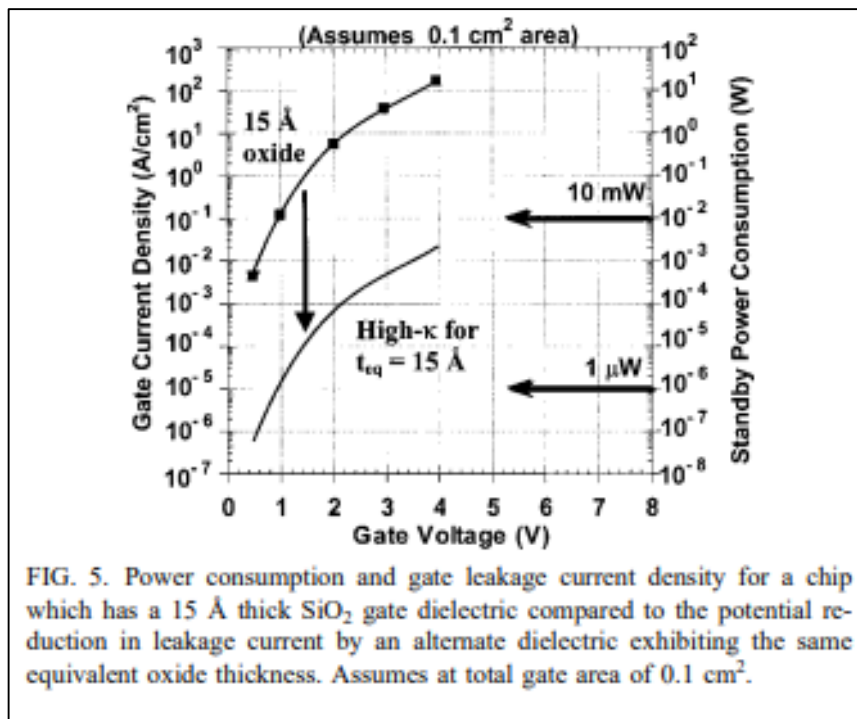
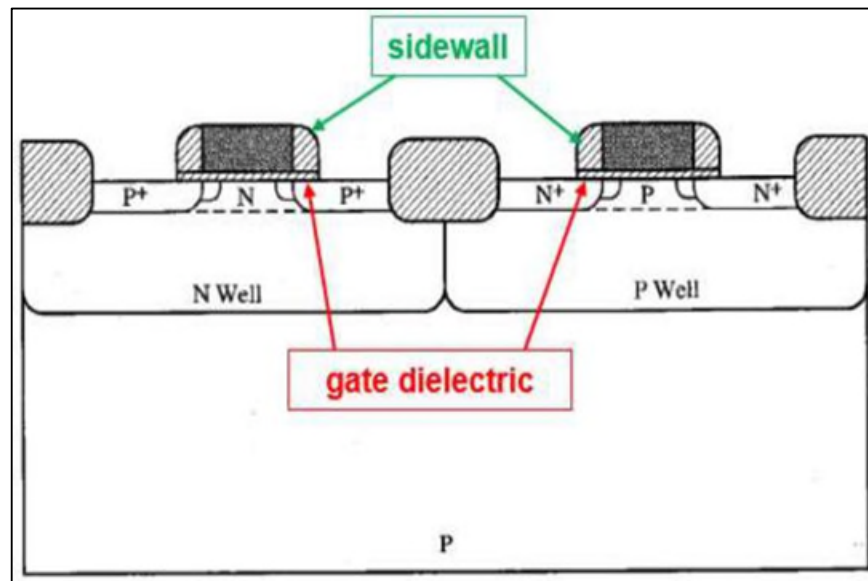


FIG. 5. Power consumption and gate leakage current density for a chip which has a 15 Å thick SiO₂ gate dielectric compared to the potential reduction in leakage current by an alternate dielectric exhibiting the same equivalent oxide thickness. Assumes at total gate area of 0.1 cm².

Wilk, Ex.1018, Fig. 5.

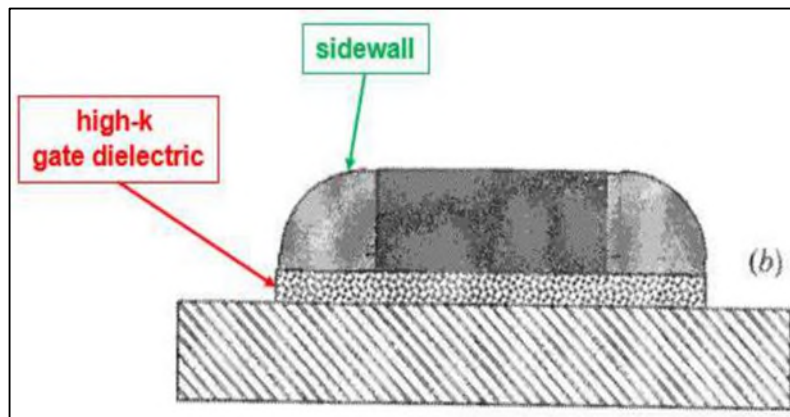
70. Not only did the prior art recognize the use of high-k materials as a substitute for silicon dioxide gate dielectrics, but the prior art also showed it was common to extend the gate dielectric out from underneath the gate electrode to underneath the sidewalls. For example, in Figure 2-34 below in Plummer, the gate dielectric is wider than the gate electrode.



Plummer, Ex.1333, Fig. 2-34

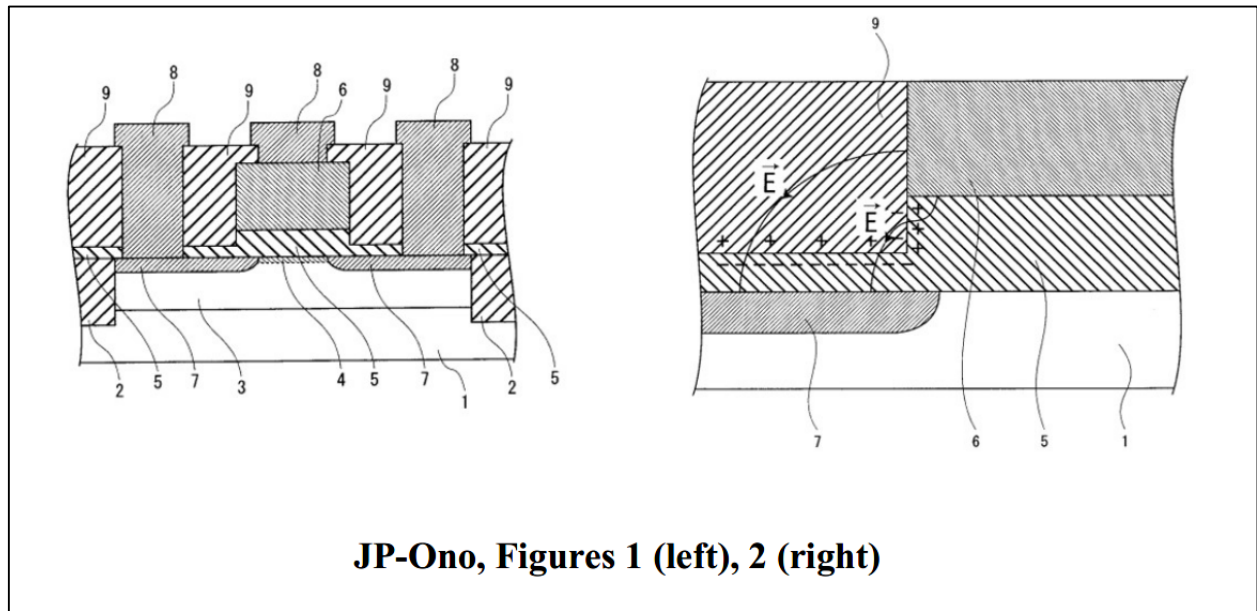
Plummer, Ex.1333, Fig. 2-34.

71. As another textbook example, Houssa shows using HfO_2 as the high-k gate dielectric, with and without extending the gate dielectric underneath the sidewalls. Houssa explains that by extending the gate dielectric “with the approach of figure 5.1.9(b), the etch requirements are relaxed but they will require LDD implants through the high-K layer.” Houssa, Ex.1213, 510, Fig. 5.1.9(b).

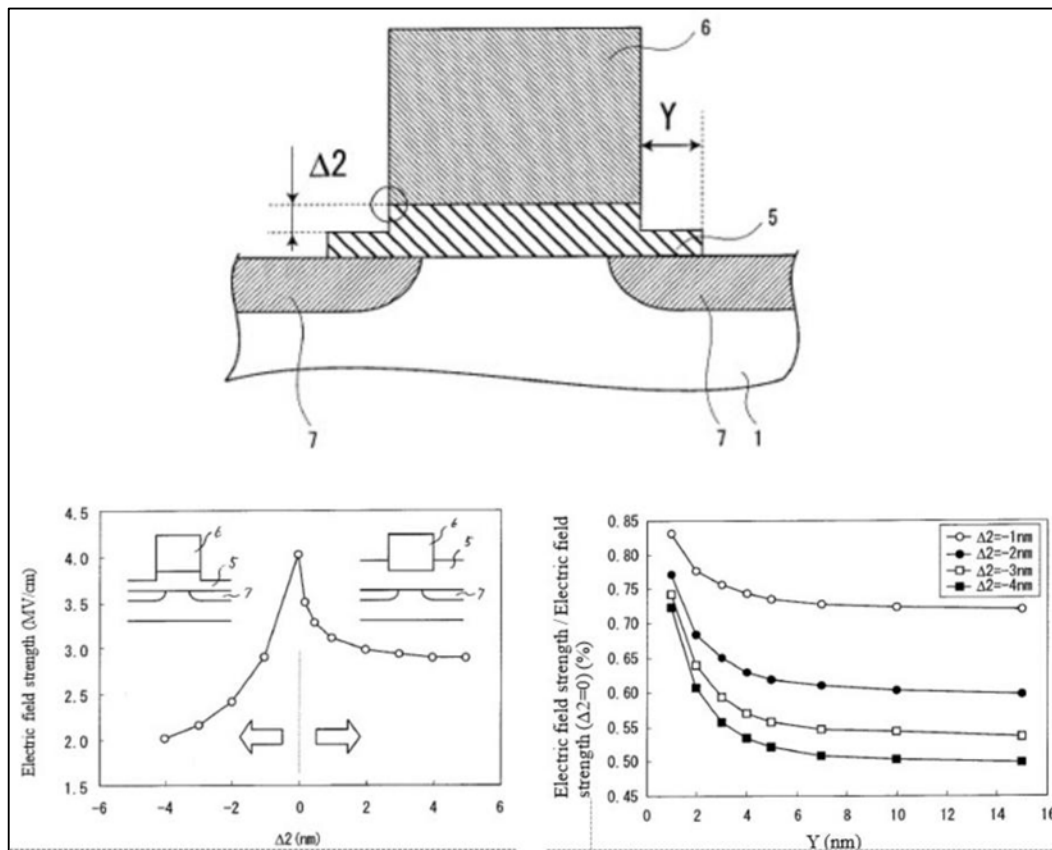


Houssa, Ex.1213, Fig. 5.1.9(b)

72. Japanese Publication No. 2005/064190 by Ono, et al. (“JP-Ono”) published on March 11, 2005 and described some of the known benefits of expanding the high-k gate dielectric wider than the gate electrode, including that “protruding the gate insulating film outside the gate electrode during processing results in higher values of the electric field.” JP-Ono, Ex.1340, ¶7. Further, JP-Ono suggests that extending the gate dielectric over the source/drain region, as well as reducing the thickness of the gate dielectric over the source/drain regions compared with under the gate electrode, “mitigate[s] the electric field at the lower end corner of the gate electrode 6” and “suppresses problems such as insulation breakdown and decreased reliability of the gate insulating film.” *Id.*, Abstract. Specifically, JP-Ono detailed how thinning the gate dielectric over the source/drain region minimizes the electric field at the edge of the gate. *Id.*, ¶¶29-32, Figs.1-2.

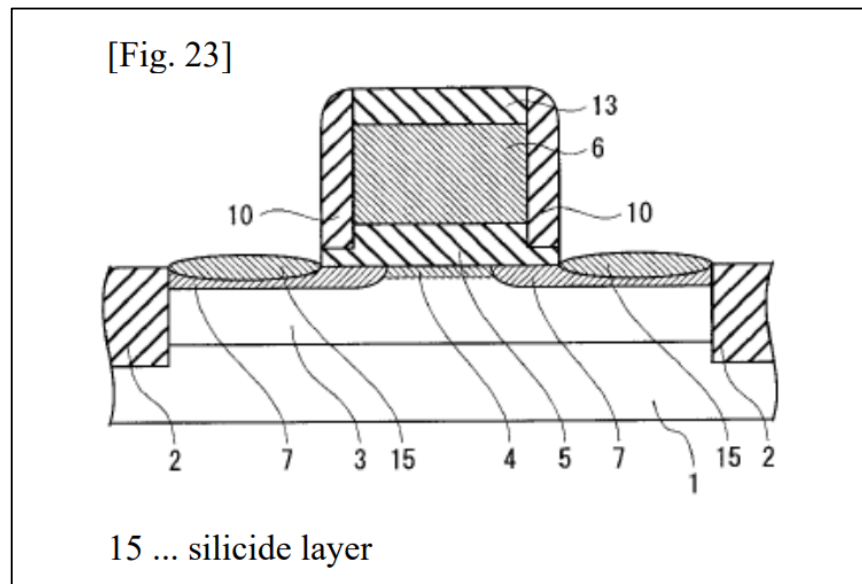


73. Further, JP-Ono studied how varying the thickness and length of the gate dielectric over the source/drain regions affects the electric field distribution. Figure 4 shows that when the gate dielectric over the source/drain region is the same thickness as under the gate, e.g. at $0 \Delta 2$, the electric field is strongest. JP-Ono, Ex.1340, ¶¶29-32, Figs. 1-2. As the gate dielectric becomes thinner compared with under the gate electrode, e.g. when $\Delta 2$ is negative, the electric field weakens more than with a thicker gate dielectric, which favors a thinner dielectric over the source/drain regions. *Id.*, ¶35. Figure 24 further shows that the electric field is further reduced as the gate dielectric protrudes farther from the corner of the gate, i.e., as Y increases. *Id.*, ¶87.



JP-Ono, Ex.1340, Figs. 3 (top), 4 (bottom-left), 24 (bottom-right)

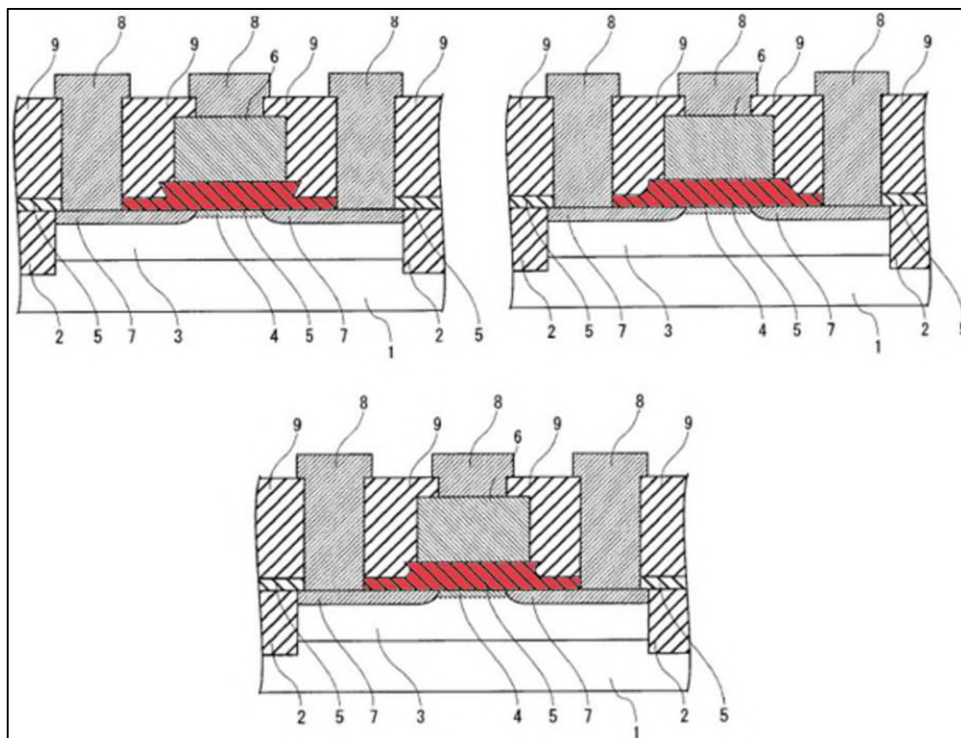
74. These improvements are explicitly taught in a FET having a gate sidewall made of “materials like silicon oxide, silicon nitride, or silicon oxynitride,” as shown Figure 23 below. JP-Ono, Ex.1340, ¶83.



JP-Ono, Ex.1340, Fig. 23

75. Thus, JP-Ono teaches a POSITA the benefits of changing not only the location of the gate dielectric, e.g. outside the gate electrode, but also the shape of the gate dielectric, e.g. with thinner ends over the source/drain regions than underneath the gate electrode. In reference to Figure 23, JP-Ono explained that “it is not essential for the side of the gate insulating film 5 to be located inside or outside of the outer surface of the gate-side wall 10,” but instead, the gate dielectric can be located both farther than the end of the sidewall, or closer than the end of the sidewall, with similar benefits. JP Ono, Ex.1340, ¶83 (“Therefore, it is preferable that the side of the gate insulating film does not protrude too far outward [or inward] from the outer surface of the gate-side wall.”).

76. JP-Ono demonstrated several different shapes for the protruding portions of the gate dielectric in Figures 36-44, as can be seen by some examples below in red. JP Ono, Ex.1340, Figs. 38, 41-42 (below). “By changing the shape of the gate insulating film near the lower corner of the gate electrode, as shown in the various examples here, it is possible to adjust the capacitance formed between the gate electrode 6 and the source-drain region 7, allowing for optimization.” *Id.*, ¶108. Although shown without any sidewalls, JP-Ono explained that “gate-side wall 10 may be removed after processing the gate insulating film, or it may be left as it is.” *Id.*, ¶103.



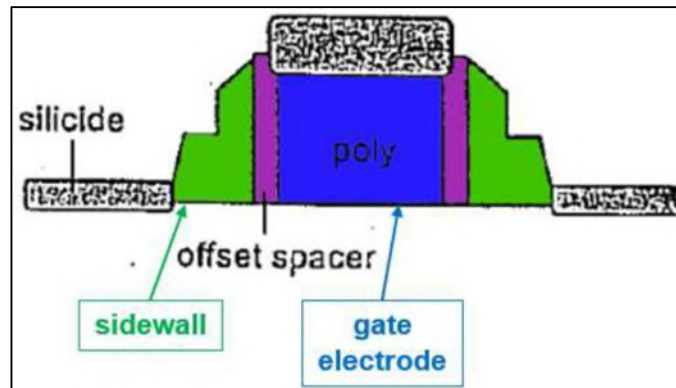
JP-Ono, Ex.1340, Figs. 38 (top-left), 41 (top-right), 42 (bottom)

C. Sidewall Structures

77. Varying the sidewall structure on the sides of the gate electrode is another way a POSITA had to further optimize device performance in the prior art. Sidewalls, also referred to as spacers or sidewall spacers, are formed on the side of the gate electrode for a variety of reasons. As discussed above, various sidewall structures may be used on the gate electrode to control the shape and position of source/drain extensions after annealing of the implanted dopants, as well as the overlap of the extension regions and the gate/gate insulating film. *See* Houssa, Ex.1213, 511; Weste, Ex.1341, 122; Wolf-4, Ex.1334, 9, 217, 219; Plummer, Ex.1333, 78. Alternatively, sidewall spacers can prevent shorts between the source/drain and the gate, for example if the source/drain regions have silicide portions. Plummer, Ex.1333, 742. These spacers are often made with silicon dioxide or silicon nitride, or combinations of multiple oxide and nitride layers. Houssa, Ex.1213, 511-12.

78. Varying the sidewall structure to control the source/drain extensions is one example of device optimization. As one textbook noted, “it has also been reported that the amount of overlap of the SDE-region with the gate-edge is also critical for optimum device performance.” Wolf-4, Ex.1334, 217. As shown in Wolf’s Figure 5-25 below, a POSITA knew that varying the size of the spacer at the gate electrode would affect formation of the source/drain extension and the resulting overlap with the gate edge: “an offset-spacer is fabricated on the side of the gate after the gate-poly is etched (but

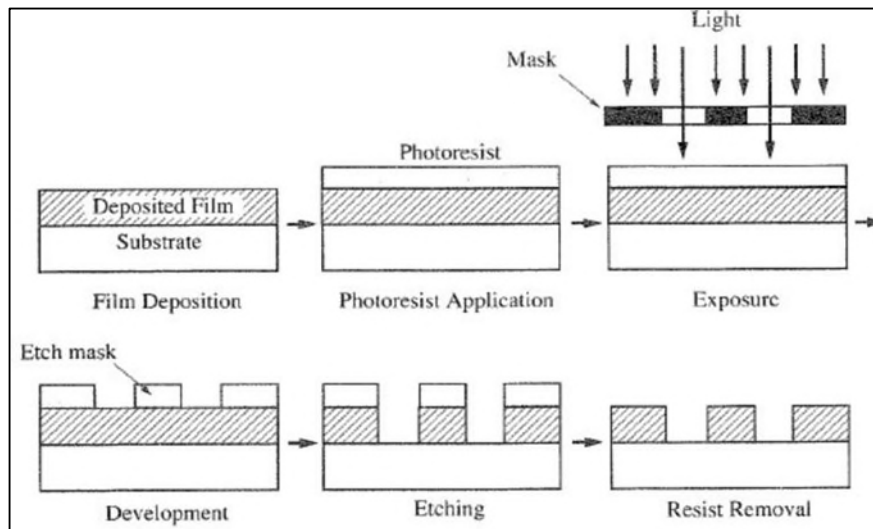
before the SDE implant step is carried out,” with the spacer width “varied from zero (no-spacer) to some upper-bound (e.g., 50-nm)” to control gate overlap and optimize device performance. *Id.*



Wolf-4, Ex.1334, Fig. 5-25

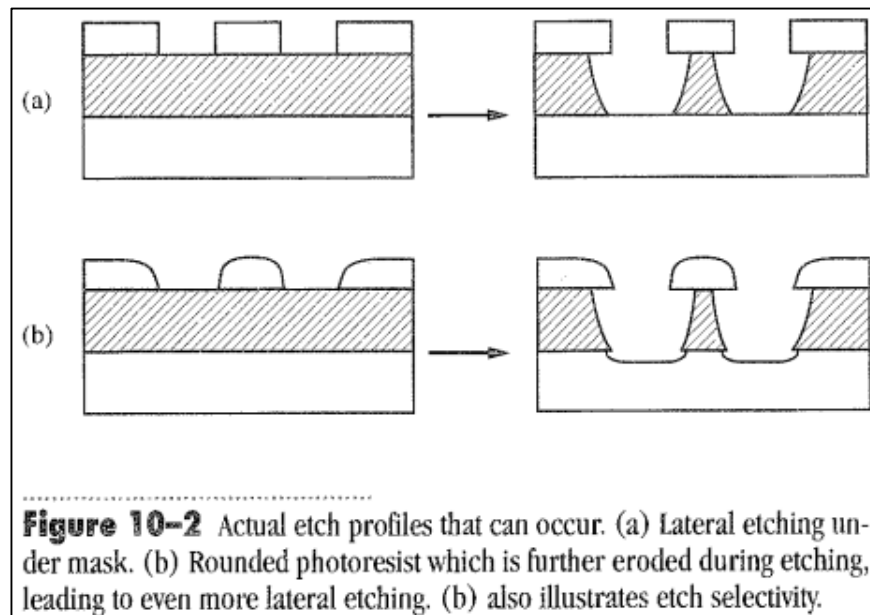
D. Etching

79. The process of manufacturing a semiconductor device, particularly one with varying transistor structures, often involves a series of material deposition and etching, including by deposition of thin films with selective etching to pattern a desired structure. Plummer, Ex.1333, 609-11. For example, a mask may be used in selective portions of a semiconductor device to “mask” or protect the underlying structure from further processing. As seen below, some areas may be masked while other areas are left unprotected such that a subsequent etching step etches the unmasked areas, while leaving the masked areas relatively intact. *Id.*, 609-10, Fig. 10-1.



Plummer, Ex.1333, Fig. 10-1

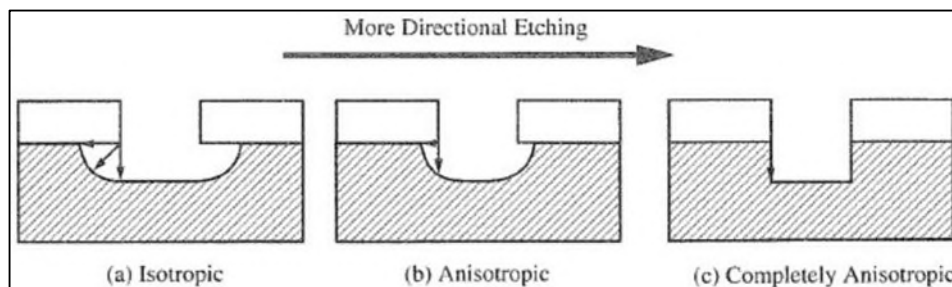
80. A POSITA can further optimize the structure of the semiconductor device by varying the etching process, as some processes are more selective than others. While the ideal etch profile “has perfectly straight sidewalls exactly under the edge of the mask,” as seen above in Figure 10-1, in practice etching has both lateral and vertical components, as seen below in Figure 10-2.



Plummer, Ex.1333, Fig. 10-2

81. Etching is accomplished through both wet and dry processes, where wet etching often entails immersing the wafers in liquid like hydrofluoric acid to perform chemical etching, while dry etching uses plasma instead to etch material through both a physical and chemical process. Plummer, Ex.1333, 609, 612.

82. Under certain circumstance, etching can also be targeted to etch directionally. Anisotropic etching, for instance, is considered a vertical etch with little to no etching in the lateral direction, while isotropic etching has more equal etching rates both vertically and laterally. Plummer, Ex.1333, 610-13. These differences can be seen below in Figure 10-3.



Plummer, Ex.1333, Fig. 10-3

E. Replacement Metal Gate Stacks

83. While the industry recognized the benefits of high-k gate dielectrics, the prior art also recognized that using metal gates on top of high-k gate dielectrics further enhanced transistor performance, particularly as transistor sizes became smaller. When formed on top of high-k gate dielectrics like HfO_2 , metal gate stacks addressed issues like Fermi-level pinning, eliminated polysilicon gate depletion, provided lower resistance, enhanced switching speeds, and improved overall transistor performance.

84. For example, a 2002 article by Samavedam et al. titled “Metal Gate MOSFETs with HfO_2 Gate Dielectric” recognized “[m]etal gates will eliminate gate depletion and address other issues like boron penetration and increased gate resistance, which will be aggravated as the poly gate thickness is scaled down.”). Samavedam-2002, Ex.1110, Introduction; *see also id.*, Conclusion (“We have successfully fabricated and characterized HfO_2 n-MOSFETs with TaSiN and PVD TiN gates and p-MOSFETs with CVD and PVD TiN gates using a conventional CMOS process. Metal-gated HfO_2 n-MOSFETs show a $10^4\times$ gate leakage reduction compared to

poly/SiO₂ devices. Reasonable Ion/Ioff performance and reliability were observed in PVD TiN/HfO₂ PMOS.”); *see also* Lee-2002, Ex.1105, Introduction (“As CMOS devices are scaled into sub-0.1 um regime, poly-depletion effects and boron penetration become significant concerns. Therefore, metal gate electrodes are being explored to replace the polysilicon gate.”). Just two years later, a 2004 article titled “55nm high mobility SiGe(:C) pMOSFETs with HfO₂ gate dielectric and TiN metal gate for advanced CMOS” concluded that “[f]or the first time, MOS transistors with compressively strained SiGe(:C) channel, metal gate and high-k dielectric are demonstrated down to 55nm gate length,” with significant improvements: “SiGe(:C) surface channel pMOSFETs with HfO₂ gate dielectric exhibit a 10⁴ gate leakage reduction and a 65% mobility enhancement at high transverse effective field (1MV/cm) when compared to the universal SiO₂/Si reference.” Weber-2004, Ex.1111, 42.

85. Other prior art references further recognized the problem of using polysilicon gates with high-k gate dielectrics specifically, or decreased transistor size in general. As gate dielectrics grew smaller consistent with transistor sizes, the polysilicon depletion effect worsened. Saito631, Ex.1518, 1:31-34; Hou, Ex.1519, 1:36-44. And where a high-k material is substituted for the silicon dioxide gate dielectric with a polysilicon gate electrode, diffusion of the polysilicon dopants into the high-k material can cause a large threshold voltage offset. Colombo, Ex.1520, ¶5; Kavalieros277, Ex.1515, ¶3. As discussed above, metal gate stacks were considered the

next step to address these problems. Saito631, Ex.1518, 1:31-34; Iriyama, Ex.1521, 1:28-34, 1:41-42; ITRS_FEP, Ex.1512, 2-3, 20; ITRS_PIDS, Ex.1216, 1, 3, 27, Fig. PIDS5.

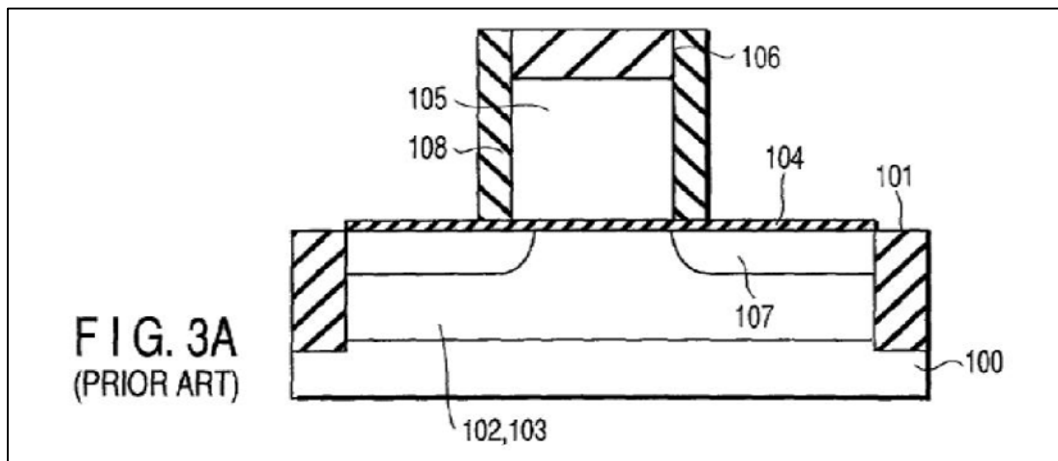
86. In particular, the prior art recognized that metal gates for PMOS and NMOS transistors would need separate metal gate stacks, and replacement metal gates (or gate-last processes) were well known to provide significant benefits compared with gate-first approaches. A material's "work function" is "the minimum energy required to bring an electron from the Fermi level to the vacuum level." Wolf-3, Ex.1229, 117. However, in MOS/MIS structures, the metal is in direct contact with a dielectric, not with the vacuum. Moreover, work functions of metal gates are highly dependent on material properties and interfaces. To differentiate this, an "effective work function" of the metal gate is commonly used to refer to the metal work function as measured (e.g., through the threshold voltage of the device).

87. In a CMOS device, PMOS transistors require a work function greater than about 4.8 eV, while NMOS transistors require a work function of less than about 4.6 eV. Hou, Ex.1519, 1:17-22; Colombo, Ex.1520, ¶¶20-21; ITRS_FEP, Ex.1512, Tbl. FEP4a ($|E_{c,v}-\phi_m|$ (eV) < 0.2). Where the same polysilicon gate electrode can be doped to adjust the work function for both NMOS and PMOS transistors, this is not the case for metal gates. Different metal gate stacks must be used. *See* Kavalieros277, Ex.1515,

¶3 (“When making a CMOS device that includes metal gate electrodes, it may be necessary to make the NMOS and PMOS gate electrodes from different materials.”).

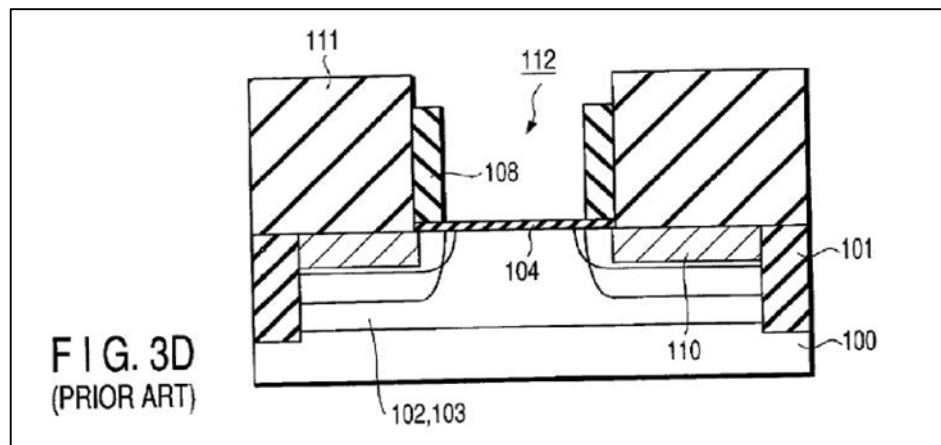
88. Some of the metals considered in the prior art for the PMOS metal gate stack showed less thermal stability than necessary, adversely affecting device performance when subjecting the metal to the high temperatures used to anneal the dopants in the source/drain regions. Hou, Ex.1519, 1:45-57; Iriyama, Ex.1521, 1:41-48.

89. One solution already considered by the prior art was replacement metal gates (“RMG”), which is a “gate-last” approach because a dummy gate is often manufactured first and then replaced by the metal gate. By making the metal gate last, the POSITA avoids subjecting the metal gate stacks to high temperatures during the source/drain annealing (because the annealing is done before placement of the metal gate). As seen below from one prior art reference, source/drain regions (107), the polysilicon dummy gate (105), a SiN film (106), and sidewalls (108) are formed for the NMOS and PMOS transistors before the replacement metal gate. Matsuo, Ex.1522, ¶¶9-10, 16, FIG. 3A.



Matsuo, Ex.1522, FIG. 3A

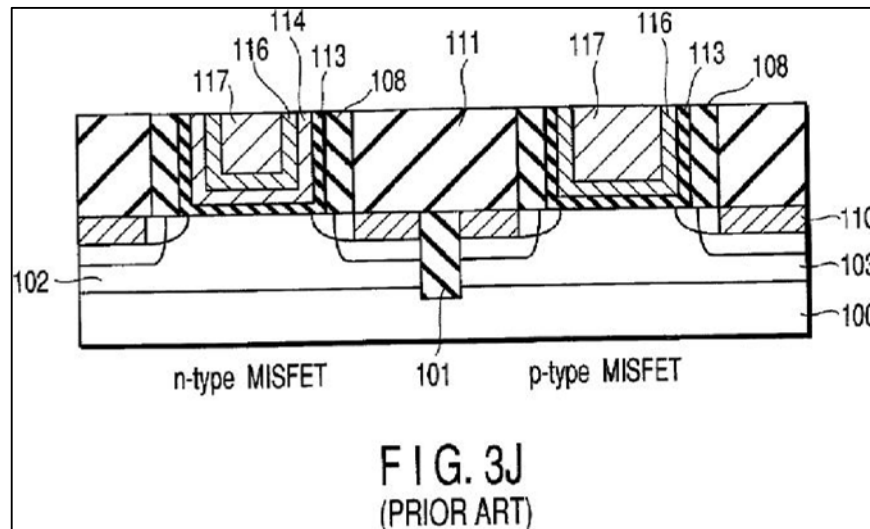
90. Before the dummy gate is replaced, the source/drain regions are doped and annealed. See Matsuo, Ex.1522, ¶10, FIGS. 3B-C; see also Hou, Ex.1519, 2:8-11; Iriyama, Ex.1521, 1:59-2:6. As one of the last steps, the dummy gates are removed to allow for placement of the metal gate stack. Matsuo, Ex.1522, ¶¶11-13, FIG. 3D.



Matsuo, Ex.1522, FIG. 3D

91. In this example, after removal of the dummy gate, both the NMOS and PMOS metal gate electrodes are formed, as seen below. Matsuo, Ex.1522, ¶¶12-16,

FIG. 3J. First, gate dielectric (113) is formed, and then metal layers 114, 116, and 117 after. Matsuo, Ex.1522, ¶¶12-16. This sequence can prevent damage to metal gate stacks susceptible to deterioration by high temperature annealing. Iriyama, Ex.1521, 2:22-29.



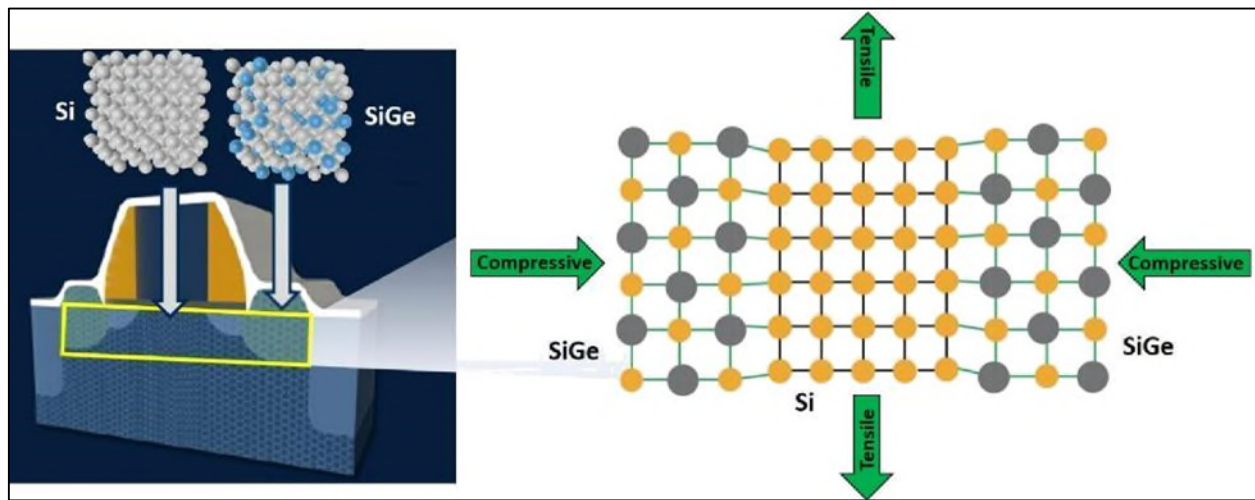
Matsuo, Ex.1522, FIG. 3J

92. In Fig. 3J above, the metal layer 114 is directly formed on the gate dielectric 113 for NMOS gate electrode (shown on the left), but a different metal gate stack is used for the PMOS gate electrode (shown on the right), which does not include metal layer 114. Matsuo, Ex.1522, ¶21. The two gate electrodes thus have different metal work functions, one for NMOS and one for PMOS. Matsuo, Ex.1522, ¶21, FIG. 3J; Hou, Ex.1519, 2:11-14; Iriyama, Ex.1521, 2:10-12; Mistry2007, Ex.1516, 247; Mistry_Presentation, Ex.1517, 16, 18.

F. Strained Silicon

93. In the early 2000s, strained silicon technology was recognized as another mechanism to improve transistor performance as transistor sizes continued to shrink. Until the large-scale adoption of strained silicon, PMOS transistors used to be slower than NMOS transistors and much effort was spent on improving PMOS transistor performance compared with NMOS transistors. But the prior art quickly realized that compressively strained PMOS transistors could be improved by as much as 50%, leading to a reversal in efforts spent trying to improve NMOS transistors compared with PMOS transistors.

94. Germanium is one source of compressive stress in PMOS transistors. The Ge atoms are larger in size than Si atoms, such that silicon-germanium (“SiGe”) can be used in the source/drain regions of PMOS transistors to apply compressive stress to the PMOS channel region. See Thompson-2004, Ex.1523, 1790-96; Sun-2007, Ex.1524, 2. By 2005, SiGe source/drain regions increased PMOS “hole mobility by as much as 50%” (James, Ex.1525, 2), doubling PMOS operating speeds.



95. Numerous prior art references recognized the benefits of strained silicon, for both PMOS and NMOS transistors. For example, in a 2004 paper titled “35% Drive Current Improvement from Recessed-SiGe Drain Extensions on 37 nm Gate Length PMOS,” Chidambaram et al. recognized that “Epitaxial SiGe, grown in recessed Si, has been used to compressively strain the PMOS channel and increase the hole mobility.” Chidambaram-2004, Ex.1104, Introduction; *see id.*, Abstract (“A highly compressive SiGe layer, in close proximity to the channel, results in large hole mobility improvements.”). Another 2004 article by Mistry et al. proclaimed that “[t]he use of strain to improve mobility has been known for 50 years,” concluding that “[u]ni-axial strained silicon has been implemented in a high volume manufacturing 90nm logic technology for the first time, with impressive performance results and improved power scaling.” Mistry-2004, Ex.1106, 50.

96. Where a PMOS transistor benefits from compressive strain, NMOS transistors benefit from tensile stress along the channel region. As seen in Figs. 2-4 from Mistry-2004 (Ex.1106), compressive stress from SiGe source/drain regions on PMOS transistors and tensile stress on NMOS transistors from a high tensile stress nitride overlayer were well known to improve transistor performance.

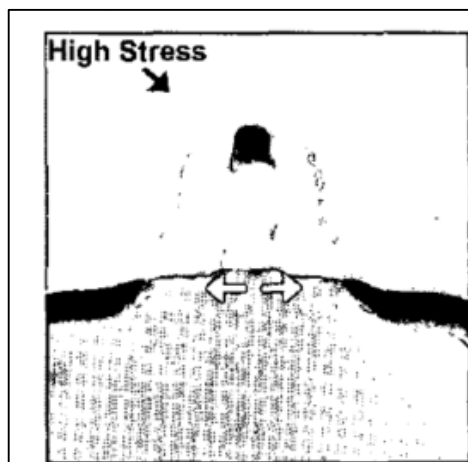
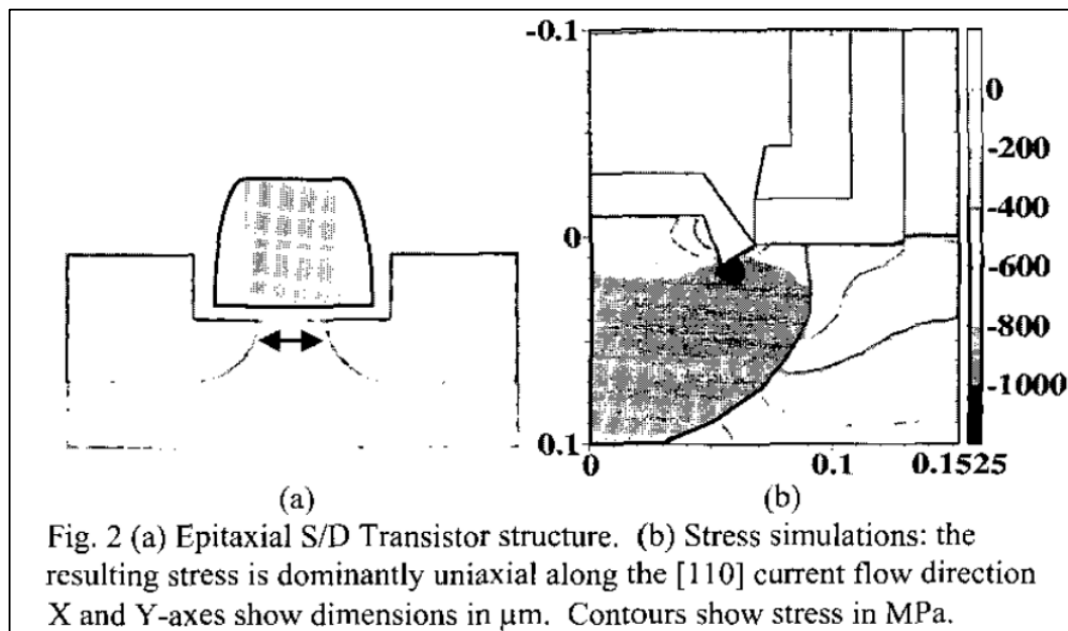


Fig. 3 TEM of NMOS transistor showing high tensile stress nitride overlayer.

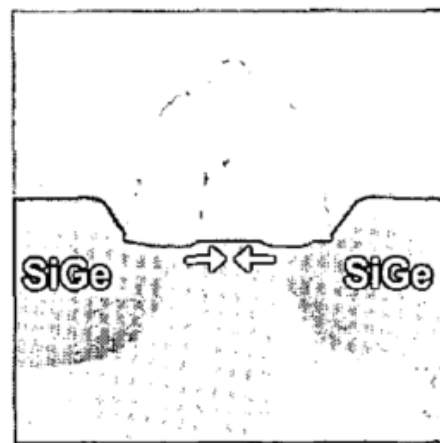


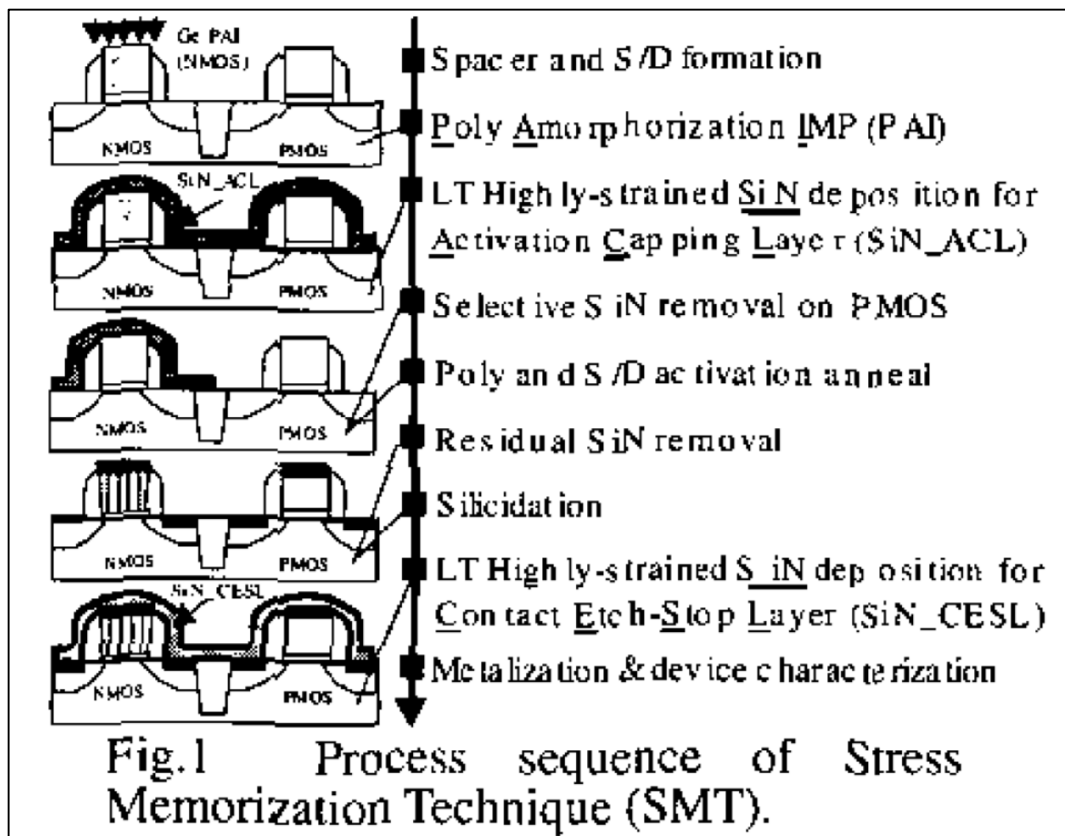
Fig. 4 TEM of PMOS showing SiGe heteroepitaxial S/D inducing uniaxial strain.

Mistry-2004, Ex.1106, FIGS. 2-4.

97. In another article that same year by Chien et al. titled “Stress Memorization Technique (SMT) by Selectively Strained-Nitride Capping for Sub-65nm High-Performance Strained-Si Device Application,” the prior art recognized that “[c]hannel stress control has become a critical technique for electron and hole mobility improvements as down scaling the device dimension.” Chen-2004, Ex.1103, Introduction. The article further recognized the tradeoffs inherent in stressing both PMOS and NMOS transistors on the same chip. *Id.* (“In addition, recent studies of high tensile capping layer on top of the silicide have demonstrated the NMOSFET driving current improvement capability, but with the PMOS performance degradation.”).

98. Searching for a cost-conscious method to effectively stress the NMOS transistor without degrading PMOS performance, the article proposed (1) selectively applying a high tensile nitride activation capping layer to the NMOS transistor, and (2) applying a low temperature, high-tensile nitride film as a contact etch stop layer to both the NMOS and PMOS transistors. Chen-2004, Ex.1103, Channel Stress Control by SMT; *see id.*, Introduction (“In this paper, we proposed a novel stress memorized technique (SMT) to improve the device performance without PMOS degradation. A high tensile nitride capping layer acts as a temporary stressor to effectively modulate the channel stress. The stress effect is then enhanced and memorized by well-controlled poly amorphization and re-crystallization procedures. This high tensile nitride

capping layer will be removed after the annealing step. Therefore, a much thicker capping layer can be used to increase the stress level without any process limitation to impact the subsequent gap filling process steps.”); *id.*, Channel Stress Control by SMT (“After the silicide formation, the low temperature, high-tensile Nitride film is deposited as Contact-Etch-Stop-Layer (SIN-CESL) to add up the stress effect.”).



Chen-2004, Ex.1103, Fig. 1.

99. Additional prior art references taught straining both PMOS and NMOS transistors. See Murthy151, Ex.1526, ¶¶5, 48, 72; James, Ex.1525, 2. For example, it was known to create tensile strain with epitaxial source/drain regions, similar to SiGe

for PMOS transistors, but it requires using an atom smaller than silicon, like carbon, to grow a material like silicon carbide (SiC) instead of SiGe,. See Murthy¹⁵¹, Ex.1526, ¶¶5, 48, 72; James, Ex.1525, 2; Bohr, Ex.1527, ¶45.

100. As either an alternative or a supplement to source/drain epitaxy, the semiconductor industry was also already depositing compressive and tensile stress-inducing films over PMOS and NMOS devices to induce a desired strain, as shown above. See also James, Ex.1525, 2, 4; Morin-2007, Ex.1528, 355-56, 367; Hsu⁸²³, Ex.1506, ¶3; Jung, Ex.1529, Abstract, ¶90 (“In addition to being deposited as part of a structure to control electron mobility, as shown in FIG. 1B, a stress-tuned silicon nitride film can be deposited for other purposes . . . , for example . . . , to provide an etch stop layer”). A contact etch stop layer (“CESL”) made of silicon nitride was frequently used, and if prepared under certain conditions, a silicon nitride CESL may apply stress to the channel and increase device performance. Hsu⁸²³, Ex.1506, ¶3; see also Ke, Ex.1531, ¶3 (“A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device.”); Jung, Ex.1529, ¶9 (“In addition to being deposited as part of a structure to control electron mobility, as shown in FIG. 1B, a stress-tuned silicon nitride film can be deposited for other purposes in various steps in the fabrication process, for example (and not by way of limitation), to provide an etch stop layer . . . , as well as to enhance channel mobility in various portions of the device structure.”); Morin-2007, Ex.1528, 355-56. It was well known

that a silicon nitride CESL may provide tensile stress, compressive stress, or no stress at all, depending on the process used to apply the layer. *See, e.g.*, Jung, Ex.1529, ¶¶17, 99-100, 131-32, Tbls. IV-V, VII, Fig. 15.

101. As evidenced by the prior art, strained silicon has been well known long before the priority date of the challenged patents. *See, e.g.*, Sun-2007, Ex.1524, 101 (“Strain is a relatively old topic in semiconductor physics.”). In fact, strained silicon was already commercially used in at least three generations of devices by 2007. *See* Thompson-2004, Ex.1523, 1790-91 (Intel’s 90nm devices); Bai-2004, Ex.1532, 657-58 (Intel’s 65nm devices); Mistry2007, Ex.1516, 247-48 (Intel’s 45nm devices); Mistry_Presentation, Ex.1517, 1-19 (same).

G. Stress Buffering Layers

102. Not only were tensile stress contact etch stop layers and SiGe source/drains well known in the prior art, but using buffer layers to mitigate the unwanted effects of those stress layers were also well understood concepts in the prior art.

103. If a tensile contact etch stop layer is deposited over a PMOS device, it generally applies a tensile stress to the channel region. Morin-2007, Ex.1528, 355-56, 367; Doris, Ex.1429, ¶¶5, 13; Hsu823, Ex.1506, ¶37. Where the PMOS device is already compressively stressed, for example with epitaxial SiGe source/drain regions, the tensile stress from the contact etch stop layer offsets some portion of the

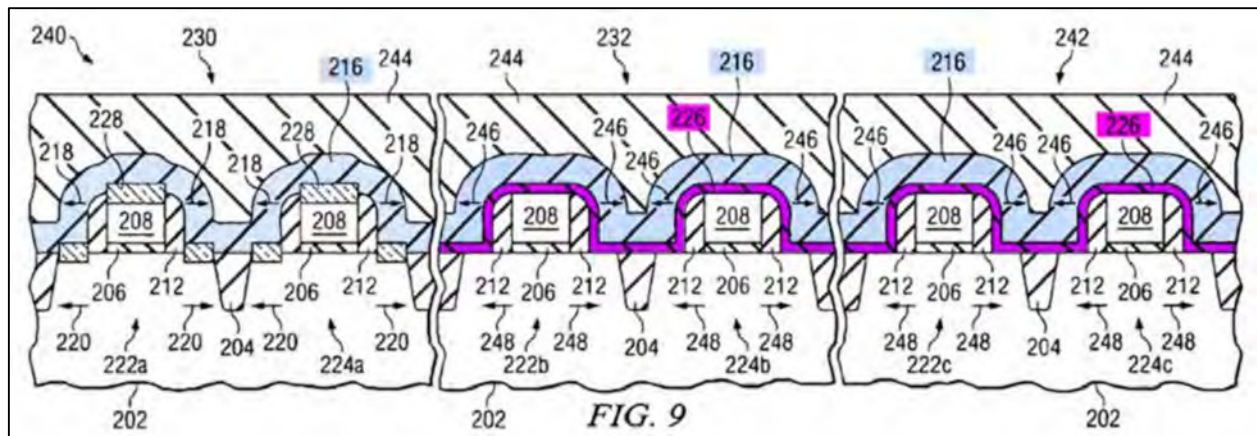
compressive stress, reducing improvements from the SiGe. Morin-2007, Ex.1528, 355-56, 367; Kavalieros729, Ex.1419, ¶¶2, 26; Doris, Ex.1429, ¶5. The tensile stress may even degrade performance, particularly in PMOS devices without SiGe source/drains. Morin-2007, Ex.1528, 355-56, 367.

104. A POSITA would have understood how to mitigate or negate performance decreases on the PMOS devices from tensile stress. First, a POSITA may choose to apply both a SiGe source/drain to a PMOS device as well as a tensile contact etch stop layer over both the NMOS and PMOS devices to optimize performance of both devices. If the compressive stress from the SiGe is greater than the tensile stress from the contact etch stop layer, the overall compressive stress may still increase PMOS performance, though it may be lessened by the contact etch stop layer. The tradeoff is that the tensile stress improves NMOS transistor performance.

105. A POSITA knew of other ways to mitigate the performance loss. For example, the tensile stress could be reduced for the PMOS device by using a stress-relief layer as a buffer between the SiGe and the tensile contact etch stop layer. Murthy556, Ex.1430, 9:27-29, FIGS. 2, 9, 13-15; Doris, Ex.1429, ¶42, Figs. 1-2, 14-15; Alvarez, Ex.1406, Abstract, ¶43, FIG. 9; Lee870, Ex.1431, ¶¶29, 46-67 (pFET performance degradation “is reduced/eliminated due to the inclusion of the stress relief layer 64 under the nitride layer 70 that reduces the tensile stress in the channel region”), FIGS. 2-5; Cheng810, Ex.1432, ¶¶22-31, Figs. 1B-1F (describing similar); Baik,

Ex.1433, ¶37 (“the tensile stresses of the [stressor layer] ha[ve] relatively little or no adverse impact [on] the adjacent PMOS device” because the intermediate layer “reduce[s] the amount of stresses induced in the PMOS device by acting as a physical barrier”).

106. A number of prior art references taught that using an intermediate layer “buffers the large stress inherent silicon nitride layer.” Murthy556, Ex.1430, 9:27-29; Alvarez, Ex.1406, ¶¶49, 66, 68, 77, FIGS. 9-11. As seen below, Alvarez depicts on example with a stress-inducing layer 216 (shown in blue below) that is buffered by stress-control layer 226 (shown in purple) to mitigate the adverse effects of the stress layer on the PMOS devices 224b and 224c (while still improving performance of the NMOS devices).

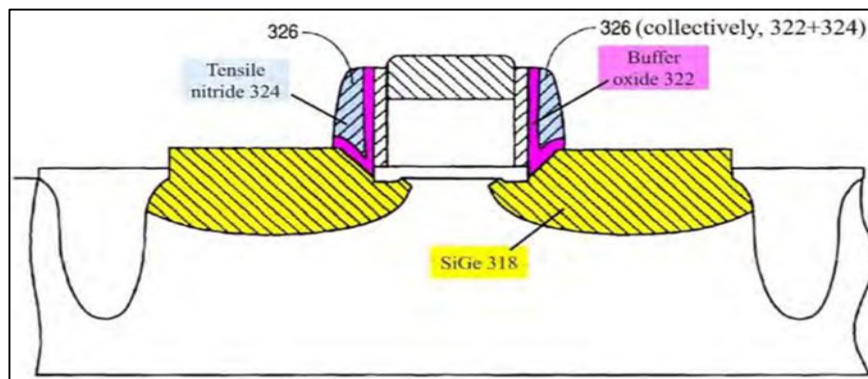


Alvarez, Ex.1406, FIG. 9

107. While the buffer layer above in Figure 9 is shown to be selectively applied, the prior art also explained that these layers could be applied to multiple areas, similar

to the one Alvarez discloses (e.g., dual-purpose stress-controlling and masking layer), as a way to save manufacturing cost or complexity. Alvarez, Ex.1406, ¶¶43, 45, 47, 49, 53-55, 78, FIGS. 7-9. This is particular advantageous where “different types of transistors . . . hav[e] different operating parameters and requirements” and/or “due to the performance requirements of transistors in the particular regions.” Alvarez, Ex.1406, ¶¶27, 32, FIGS. 7-9. Leaving the buffer layer over both the NMOS and PMOS, for example, can reduce the number of fabrication steps and lower the cost of manufacturing. Alvarez, Ex.1406, ¶75; *see also id.*, ¶¶74, 78.

108. In another example shown below, a buffer layer can be formed immediately between the SiGe source/drain regions and the gate electrode, particularly when raised SiGe source/drain regions are used. *See* Murthy556, Ex.1430, 9:11-15, 9:30-35, FIGS. 7-9; *see also* Miyashita, Ex.1435, ¶¶52-53, FIGS. 1U-1W; Koutny, Ex.1434, ¶¶88, 108 (silicon dioxide liner 485A between tensile stress-inducing layer 504A and source/drain “reduces the cumulative stress” caused by the tensile layer); Doris, Ex.1429, ¶¶34, 42; Cheng810, Ex.1432, ¶30; Lee870, Ex.1431, ¶67.



Murthy556, Ex.1430, FIG. 9 (annotated)

109. These buffer layers can prevent “the tension from materially adversely influencing the charge carrier mobility in the pFET,” such that the pFET “experiences a performance improvement” through “enhanc[ed] hole mobility in the pFET channel” compared to no buffer layer. Doris, Ex.1429, ¶¶34-35, Figs. 2, 14, 15. Using low-stress dielectric films like silicon oxides can create “a neutral buffer layer” between a compressively stressed source/drain and a tensile contact etch stop layer, which allows the compressively stressed region “to have maximum influence on the pFET channel mobility and minimizes the influence of the tensile barrier etch stop layer.” Doris, Ex.1429, ¶42; *see also* Lee870, Ex.1431, ¶¶29, 46-67 (explaining that an intermediate stress relief layer “with neutral stress or opposite stress relative to the [CESL]” reduces or eliminates any pFET performance degradation because it “reduces the tensile stress in the channel region”), FIGS. 2-5; Cheng810, Ex.1432, ¶¶22-31, Figs. 1B-1F.

H. System-on-Chip Design Advancements

110. Threshold voltage is an important characteristic when considering what a particular transistor will be used for. Threshold voltage is the minimum voltage applied at the gate to create a conductive channel between the source and drain—i.e., the ON or active voltage of the transistor. Van Zant, Ex.1211, 526, 474 (“Every MOS transistor is designed to operate at a specific threshold voltage.”). Because PMOS and NMOS transistors use different dopants for the source/drain and source/drain extensions, a

POSITA understands that PMOS and NMOS transistors have opposite gate voltages. That is, NMOS transistors require a positive voltage at the gate to induce the active state (and thus a positive threshold voltage), while PMOS transistors require a negative voltage at the gate to induce the active state (and thus a negative threshold voltage). *See, e.g.,* Weste, Ex.1341, 74, 293-296, 302.

111. Threshold voltage has three main components: flatband voltage (VFB), voltage drop across the gate oxide (V_o), and semiconductor potential at the semiconductor surface during strong inversion ($\psi_s(\text{inv})$). Sze-2002, Ex.1223, 175, 178, 194. For a given semiconductor and dielectric material, substrate doping, oxide thickness t_{ox} , and the metal work function Φ_m can be used to predictably tune a transistor's threshold voltage. Houssa, Ex.1213, 535, 537. When the substrate doping and gate oxide thickness are carefully engineered to control channel mobility and the gate capacitance, respectively, the gate electrode work function can be altered to optimize or fine-tune the threshold voltage further.

112. Consumer devices often have multiple transistors on the same chip, including transistors of the same conductivity types but with different threshold voltages, to cope with various demands on standby power and operation speed. For example, a device may include transistors for low operating power (LOP), transistors for low stand-by power (LSTP), and/or transistors for high performance (HP). ITRS-PIDS, Ex.1216, 5. HP transistors have the highest operating speed, the shortest gate

length, the thinnest gate oxide, and the lowest threshold voltage among the three. ITRS-PIDS, Ex. 1216, 11, 17, 21. LSTP transistors are designed for low performance and low leakage current and therefore have thicker gate oxides and higher threshold voltage, while LOP transistors are between the HP and LSTP devices in terms of performance, leakage current, and threshold voltage. *Id.*

113. As recognized by the prior art, instead of making different chips for different purposes, HP, LOP, and LSTP transistors can be formed on a single chip by varying the manufacturing process parameters. Because “[a]n increasing number of mixed-signal and system-on-a-chip applications require dual on-chip power-supply-voltages[,]” different transistors of the same type (e.g., PMOS or NMOS) are needed for different power-supply-voltages. Wolf-4, Ex.1334, 121. For example, “[t]he higher-voltage may be used for the analog and input/output (I/O) circuitry, and the lower-voltage for the core-digital-logic devices.” *Id.* And because analog and I/O regions must handle higher operating voltages, “the analog and I/O devices require thicker gate oxides than the core logic devices.” *Id.* As such, forming different transistors with different gate oxide thickness can be used where needed, for instance where both higher-voltage and lower-voltage transistors are desired on the same chip.

114. The prior art teaches different processes to vary oxide thickness across different transistors on the same chip. *See, e.g.,* Karve, Ex.1226, 3:45-4:36 (describing formation of nMOS with thicker gate oxide than core nMOS), Figs. 5-6, 8; Luo,

Ex.1227, 5:61-7:58 (describing formation of nMOS-DGO and nMOS core devices). As explained by one textbook, one process is to include two oxidation steps “with a masked etch-step in between to remove the first oxide from regions intended to have thinner oxide.” Wolf-4, Ex.1334, 121. Yet another process uses nitrogen implants to impede oxide growth in certain areas, which occurs because “the rate of thermal-oxidation on silicon is reduced by nitrogen implants.” *Id.* “Hence, nitrogen implantation into the silicon substrate prior to the oxidation process can be used to facilitate the implementation of such ‘dual-gate-oxide’ ICs.” *Id.*

VI. THE '764 PATENT

115. The '764 patent issued on April 12, 2011 from U.S. Patent Application No. 12/505,799, which was filed on July 20, 2009 as a divisional of U.S. Patent Application No. 11/491,260, filed on July 24, 2006 which issued as U.S. Patent No. 7,579,227 (“the ‘227 patent”). Ex.1001, cover. The '227 patent claims priority to Japan Patent Application No. 2005-227457, filed on August 5, 2005. *Id.*

A. Claims

116. The '764 patent has 21 claims, including one independent claim numbered 1, and dependent claims numbered 2-21. Ex.1001, 21:32-22:58. Claims 1-6 and 11-19 are the Challenged Claims with claims 2, 4-7, and 11-19 depending from claim 1 and claim 3 depending from claim 2.

117. The Challenged Claims are reproduced below:

1. [Preamble]: A semiconductor device comprising:

1[a]: a high dielectric constant gate insulating film formed on an active region in a substrate;

1[b]: a gate electrode formed on the high dielectric constant gate insulating film;

1[c]: a first insulating sidewall formed on each side surface of the gate electrode; and

1[d]: a second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween,

1[e]: wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, and

1[f]: part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

Ex.1001, 21:32-50.

2. The semiconductor device of claim 1, further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film.

Ex.1001, 21:51-53.

3. The semiconductor device of claim 2, wherein the buffer insulating film is a silicon oxide film.

Ex.1001, 21:54-55.

4. The semiconductor device of claim 1, wherein the first insulating sidewall is an offset sidewall.

Ex.1001, 21:56-57.

5. The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall.

Ex.1001, 21:58-60.

6. The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a Hf based oxide.

Ex.1001, 22:1-3.

11. The semiconductor device of claim 1, wherein each side end portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less.

Ex.1001, 22:22-24.

12. The semiconductor device of claim 1, wherein a side surface of the high dielectric constant gate insulating film is located at a predetermined distance from a side end surface of the first insulating sidewall toward the gate electrode.

Ex.1001, 22:25-28.

13. The semiconductor device of claim 1, wherein a side surface of the high dielectric constant gate insulating film is located at a predetermined distance from a side end surface of the gate electrode toward the first insulating sidewall.

Ex.1001, 22:29-32.

14. The semiconductor device of claim 1, wherein the second insulating sidewall has a double layer structure including an oxide film and a nitride film.

Ex.1001, 22:33-35.

15. The semiconductor device of claim 1, wherein the second insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film.

Ex.1001, 22:36-38.

16. The semiconductor device of claim 1, wherein a width of the high dielectric constant gate insulating film along a gate length is larger than a width of the gate electrode along the gate length.

Ex.1001, 22:39-42.

17. The semiconductor device of claim 1, wherein a width of a bottom surface of the high dielectric constant gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length.

Ex.1001, 22:43-46.

18. The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more.

Ex.1001, 22:47-49.

19. The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall.

Ex.1001, 22:50-52.

B. Summary of the Specification

118. The '764 Patent is directed to "a structure of a MISFET (metal insulator semiconductor field-effect transistor) and a method for fabricating the MISFET and,

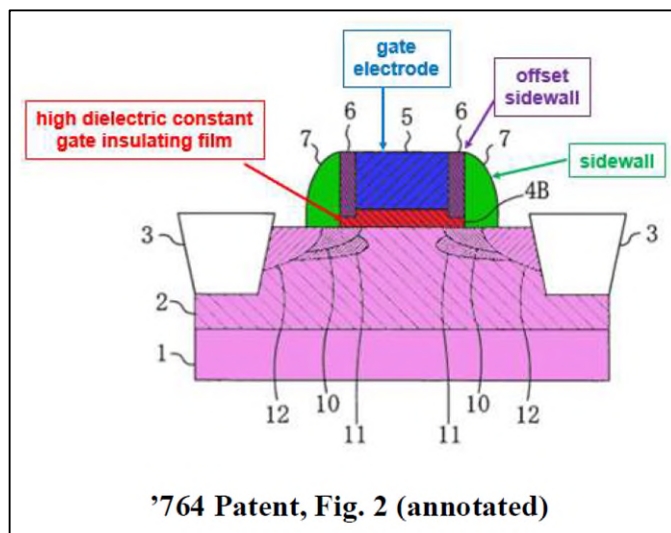
more particularly, relates to techniques for improving the driving power and reliability of a MISFET.” Ex.1001, 1:17-21. According to the ’764 patent, in prior art devices, the “side end portions” of the high-k film “are in direct contact with sidewalls,” which caused the reliability of the gate insulating film to degrade. *Id.*, 1:61-2:5.

119. The inventors of the ’764 patent purported to have solved this problem via “a MISFET structure in which a high dielectric constant gate insulating film is kept remaining under sidewalls to prevent end portions of the high dielectric constant gate insulating film from being in contact with the sidewalls, and a method for forming the MISFET structure.” *Id.*, 2:10-15. The ’764 patent discloses several exemplary embodiments in which the high-k gate insulating film extends at least partially under the insulating sidewall, and is thinner under the insulating sidewall than under the gate electrode, including devices with double sidewalls (e.g., the second and third embodiments) to which the ’764 patent’s claims are directed.

120. More specifically, the Challenged Claims recite a semiconductor device with a high dielectric constant gate insulating film, a gate electrode formed on the high dielectric constant gate insulating film, and first and second insulating sidewalls formed on each side surface of the gate electrode, wherein high dielectric constant gate insulating film extends from under the gate electrode to under the first insulating sidewall. Ex.1001, 21:33-45. Claim 1 of the ’764 patent further requires that part of

the high dielectric constant gate insulating film that is located under the first insulating sidewall has a smaller thickness than a thickness of another part of the high dielectric constant gate insulating film that is located under the gate electrode. *Id.*, 21:46-50.

121. Thus, Figure 2 (below) of the '764 patent, which corresponds to the second embodiment of the '764 patent, illustrates an exemplary device covered by claim 1:



122. As illustrated above in Figure 2, the high-k gate insulating film (shaded red) extends under first, or inner, sidewall 6 (shaded purple) and has a smaller thickness under inner sidewall 6 than under gate electrode 5 (shaded blue).

C. Summary of the Prosecution History

123. During prosecution of the application that led to the '764 patent, the Examiner rejected original claim 1 as anticipated by U.S. Patent 6,992,358 to Hieda.

Ex.1002, 122-23. The Applicant did not amend the claims, argued the Examiner misapplied Hieda, and the application was allowed thereafter. *Id.*, 142-44, 159.

VII. LEVEL OF ORDINARY SKILL IN THE ART

124. I understand that there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including the educational level of active workers in the field at the time of the alleged invention, the sophistication of the technology, the type of problems encountered in the art, and the prior art solutions to those problems.

125. I understand that there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including the educational level of active workers in the field at the time of the alleged invention, the sophistication of the technology, the type of problems encountered in the art, and the prior art solutions to those problems.

126. In determining the characteristics of a hypothetical person of ordinary skill in the art of the '764 patent at the time of the alleged invention, I considered several things, including the type of problems encountered in this field, and the rapidity with which innovations were made. I also considered the sophistication of the technology involved, and the educational background and experience of those actively working in the field, and the level of education that would be necessary to understand the '764 patent. Finally, I placed myself back in the relevant periods of

time and considered the state of the art and the level of skill of the engineers working in this field in those times.

127. It is my opinion that a POSITA at the time of the '764 patent would have had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or a related field, and three years of work experience in semiconductor design and manufacturing, including with respect to planar transistors, or equivalent work experience. Additional graduate education might compensate for a deficiency in experience, and vice-versa.

128. I also note that my opinions provided in this Declaration would not change in view of any minor modifications to this level of skill.

VIII. CLAIM CONSTRUCTION

129. It is my opinion that for purposes of this proceeding, the claim terms need not be construed to resolve the prior art issues presented in this Petition.

130. Nothing in this section should be construed as expressing any opinion as to whether the claims constitute patentable subject matter under 35 U.S.C. § 101, or whether they satisfy the definiteness, enablement, best mode, or written description requirements under 35 U.S.C. § 112.

IX. OVERVIEW OF THE PRIOR ART

A. Matsumoto (Ex.1009)

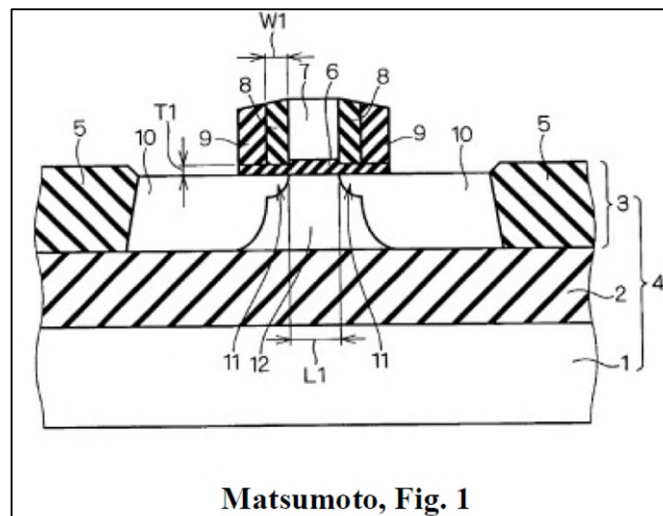
131. Similar to the '764 patent, Matsumoto relates “to a semiconductor device” and more specifically to an improved MOSFET (Metal Oxide Semiconductor Field Effect Transistor), and methods for manufacturing the same. Ex.1009, Abstract, ¶2. Matsumoto discloses a semiconductor device having a gate electrode, insulating sidewalls on the side of the gate electrode, and a gate insulating film that extends from under the gate electrode to the under the insulating sidewalls. Ex.1009, Abstract.

132. Although Matsumoto discloses several embodiments and modifications, many of the fabrication steps are discussed in relation to the second and fourth embodiments. *See, e.g.*, Ex.1009, ¶123 (“The remaining structure of the semiconductor device according to the second preferred embodiment is similar to the corresponding structure of the above-stated semiconductor device according to the first preferred embodiment shown in FIG. 1.”), ¶137 (“Referring first to FIG. 18, the gate electrode 7 is formed by the process described in the first preferred embodiment”). Moreover, Matsumoto repeatedly explains, and a POSITA would have understood, that the teachings of one embodiment (or modification thereof) could be readily applied to other embodiments. *See, e.g.*, Ex.1009, ¶140 (“The technique of the fourth preferred embodiment is applicable to any one of the first to third preferred embodiments.”), ¶141 (“The technique of the first modification of the fourth preferred embodiment is applicable to any one of the first to fourth

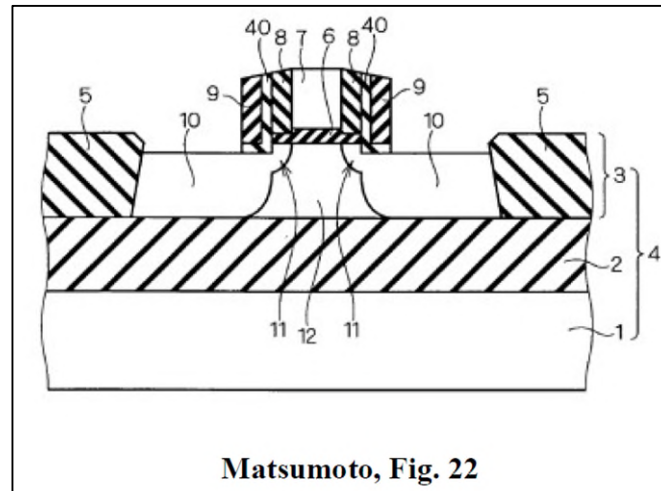
preferred embodiments.”), ¶143 (“The technique of the second modification of the fourth preferred embodiment is applicable to any one of the first to fourth preferred embodiments and the first modification of the fourth preferred embodiment.”).

133. According to Matsumoto, the “increased base width of a parasitic bipolar transistor reduces the gain of the parasitic bipolar transistor, thereby to suppress malfunctions and operating characteristic variations of the MOSFET. Additionally, a decreased amount of overlap between the gate electrode and the extensions as viewed in plan suppresses a gate overlap capacitance to achieve the increase in operating speed and the reduction in power consumption.” Ex.1009, ¶15.

134. As shown in Figure 1 below, Matsumoto's first embodiment has a gate insulating film 6 extends from under the gate electrode 7 to under both sidewalls 8 and 9, just like Figure 3 of the '764 patent. *See* Ex.1009, ¶103.



135. As shown in Figure 22 below, Matsumoto's fourth embodiment includes a gate insulating film 6 extending from under the gate electrode 7 to under only the sidewall film 8, comparable to Figure 2 of the '764 patent. See Ex.1009, ¶¶138-140.

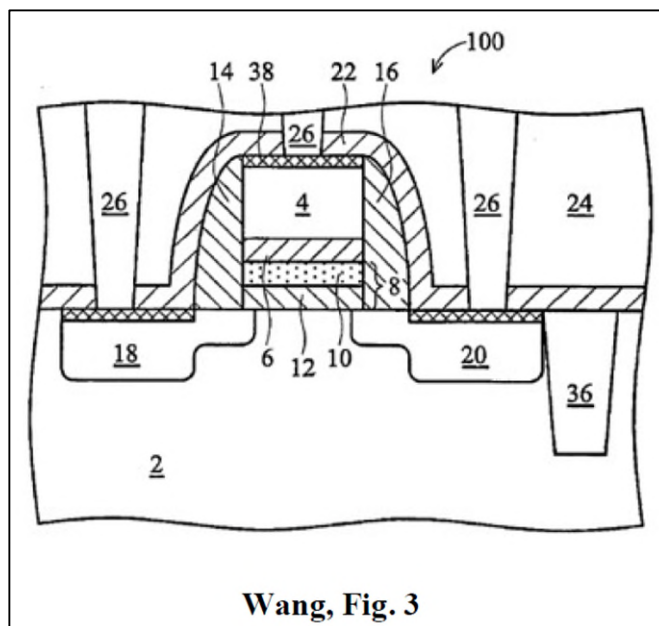


B. Wang (Ex.1012)

136. As in the '764 patent, Wang relates to “semiconductor devices and methods of manufacturing same.” Ex.1012, ¶2. More particularly, Wang discloses an improved transistor (e.g., MOSFET) having a nitrogen containing, high-k gate dielectric, and an underlying dielectric layer having a nitrogen containing portion in contact with the high-k dielectric layer and a non-nitrogen containing portion (e.g., oxide) that is in contact with the substrate. Ex.1012, Abstract, ¶2. Wang is therefore in the same field as Matsumoto and the '764 patent in my opinion. Ex.1001, 1:8-9 (“The present invention relates to a semiconductor device and a method for

fabricating the semiconductor device.”); Ex.1009, ¶2 (“The present invention relates to a semiconductor device and a method of manufacturing the same.”).

137. As shown below in Figure 3 of Wang, exemplary transistor 100 includes a gate stack with high-k dielectric layer 6 and underlying dielectric layer 8 comprising a nitrated portion 10 and a non-nitrated/substantially nitride-free portion 12. Ex.1012, ¶¶22, 24, 46, 48.



138. Wang also discloses options for forming its high-k gate dielectric, including Hf-based dielectrics (e.g., HfO₂, HfSiO, HfON, or HfSiON). Ex.1012, ¶9.

C. Sim (Ex.1024)

139. In the same field as Matsumoto and the '764 patent, Sim relates to the use of high-k dielectrics in semiconductor devices. Ex.1024, Abstract (“Scaling the physical thickness of the HfO₂ dielectric causes less charge trapping and higher

mobility.”). Ex.1001, 1:15-16 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); Ex.1009, ¶2 (“The present invention relates to a semiconductor device and a method of manufacturing the same.”); Ex.1012, ¶2.

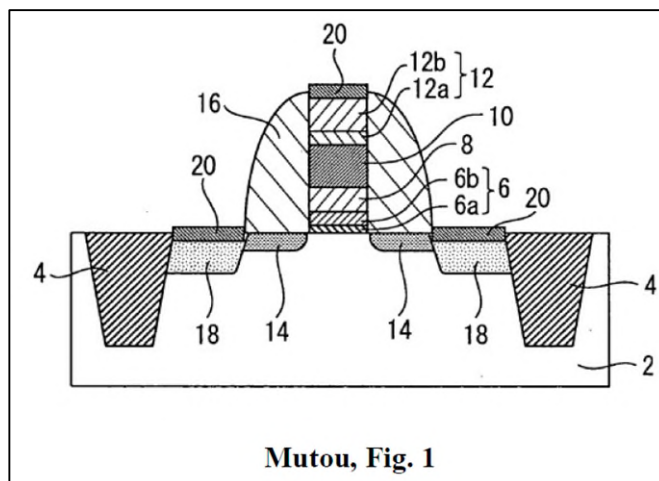
140. Sim explained that “[h]afnium-based high-k dielectrics and metal gate electrodes have been aggressively investigated to ensure continued scaling of CMOS technology, but several drawbacks such as low mobility and charge trapping have been identified.” Ex.1024, 218. Sim’s authors examined and addressed these drawbacks by testing films of different thickness and “systematically evaluat[ing] the effects of high-k film thickness on charge trapping and channel carrier mobility.” *Id.* Specifically, Sim explained that “scaling the high-k dielectric is a simple, but very effective means of improving mobility and other reliability characteristics.” *Id.* Sim concluded that “[s]caling the physical thickness of the HfO₂ dielectric to below 20Å causes less charge trapping and higher mobility.” *Id.*, 221.

D. Mutou (Ex.1019)

141. Mutou also relates to semiconductor devices, including MOSFETs. Ex.1019, Abstract, ¶¶2, 4. Mutou is therefore in the same field as Matsumoto and the ’764 patent in my opinion. Ex.1001, 1:8-9 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”);

Ex.1009, ¶2 (“The present invention relates to a semiconductor device and a method of manufacturing the same.”).

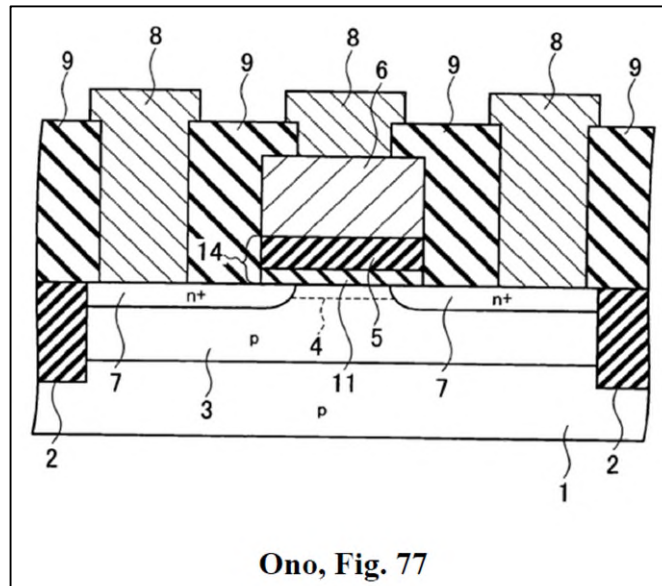
142. As shown in Figure 1 below, Mutou's transistor includes a silicon substrate 2, a gate dielectric film 6, including underlying interfacial layer 6a and high-k dielectric film 6b, and a gate electrode including a seed Si film 8, a SiGe film 10, a lower cap Si film 12a, an upper cap Si film 12b and a silicide layer 20. Ex.1019, ¶¶40-41, 44.



E. Ono (Ex.1013)

143. Ono also relates to semiconductor devices, including field effect transistors. Ex.1013, Abstract, ¶¶3-7. Ono is therefore in the same field as Matsumoto and the '764 patent in my opinion. Ex.1001, 1:8-9 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); Ex.1009, ¶2 (“The present invention relates to a semiconductor device and a method of manufacturing the same.”).

144. Ono discloses two base embodiments of a semiconductor device each of which includes a semiconductor substrate, source and drain regions arranged at the surface of the semiconductor substrate, a gate insulator film on the substrate, and a gate electrode on the gate insulator film. Ex.1013, ¶¶8-9. As shown below in Figure 77, Ono's semiconductor device includes a gate stack comprising gate insulator film 11 and gate insulator film 5 made of "HfO₂ film." *Id.*, ¶¶207, 209.



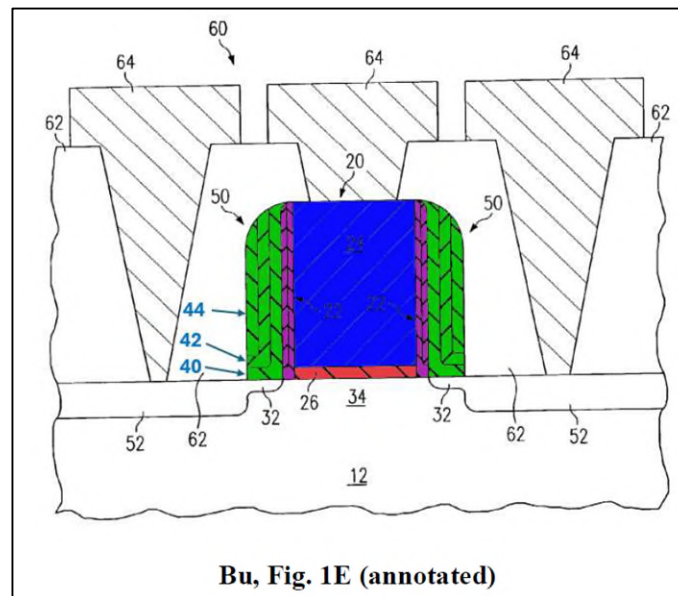
145. Gate electrode 6 is formed on gate insulator film 5, as shown in Figure 77 above, and may have gate sidewalls positioned adjacent to it. Ex.1013, ¶¶207, 181 (“sidewalls may be provided to the gate electrode”). In one example modification to adjust and optimize the electrical performance of the device, Ono teaches that “the sidewalls of the gate insulator film may curve.” *Id.*, ¶¶200, 216. Ono also discloses several examples in which a length of the gate insulating film is

varied in relation to the gate electrode, the sidewall of the gate insulating film is “slanted,” and the gate insulator films have curved end portions. *See e.g., id.*, FIGS. 86-123, ¶1216.

F. Bu (Ex.1025)

146. Bu discloses a method of forming a semiconductor device that includes forming one or more sidewall spacer layers on the outer surface of a gate stack. Ex.1025, Abstract. Bu is therefore in the same field as Matsumoto and the '764 patent. Ex.1001, 1:15-16 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); Ex.1009, ¶2 (“The present invention relates to a semiconductor device and a method of manufacturing the same.”).

147. Bu’s transistor includes a gate stack 20 comprising gate conductor 24 (*see* Ex.1025, FIG. 1E (below) (shaded blue)) and gate insulator 26 (*see id.* (shaded red)), and sidewall spacers 22 (*see id.* (shaded purple)). *Id.*, ¶42. Bu’s transistor further includes an outer sidewall (*see id.*, FIG. 1E (below) (shaded green)) formed on sidewall spacers 22. The outer sidewall has a triple-layer “ONO” structure with a first sidewall-forming layer 40 comprised of “oxide”; a second sidewall-forming layer 42 comprised of “nitride”; and third sidewall forming layer 44 comprised of “oxide.” *Id.*, ¶¶26-27, 30, 35, 43.



G. Wilk (Ex.1018)

148. Wilk describes a study of high-k dielectric candidates for use “as potential replacements for SiO₂ as the gate dielectric material for sub-0.1 μ m CMOS technology.” Ex.1018, Abstract. Wilk therefore relates to semiconductor devices, which is the same field as Matsumoto and the '764 patent. Ex.1001, 1:15-16 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); Ex.1009, ¶2 (“The present invention relates to a semiconductor device and a method of manufacturing the same.”).

149. Table I of Wilk (reproduced below) provides a “Comparison of relevant properties for high-k candidates,” including dielectric constants for those materials.

TABLE I. Comparison of relevant properties for high- κ candidates.				
Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si	Crystal structure(s)
SiO ₂	3.9	8.9	3.2	Amorphous
Si ₃ N ₄	7	5.1	2	Amorphous
Al ₂ O ₃	9	8.7	2.8 ^a	Amorphous
Y ₂ O ₃	15	5.6	2.3 ^a	Cubic
La ₂ O ₃	30	4.3	2.3 ^a	Hexagonal, cubic
Ta ₂ O ₅	26	4.5	1–1.5	Orthorhombic
TiO ₂	80	3.5	1.2	Tetrag. ^c (rutile, anatase)
HfO ₂	25	5.7	1.5 ^a	Mono. ^b , tetrag. ^c , cubic
ZrO ₂	25	7.8	1.4 ^a	Mono. ^b , tetrag. ^c , cubic

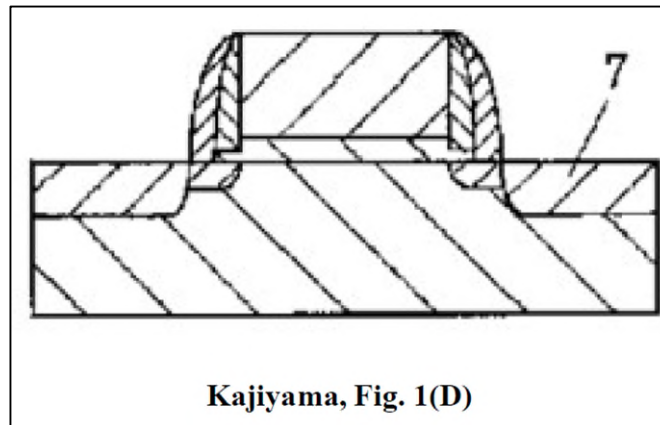
^aCalculated by Robertson (See Ref. 153).
^bMono.=monoclinic.
^cTetrag.=tetragonal.

Wilk, Table I

H. Kajiyama (Ex.1010/Ex.1011)

150. I was provided with, and conducted my analysis in this Declaration using, a certified translation (Ex.1011) of JP-Kajiyama (Ex.1010). I refer to that translation (i.e., Ex.1011) herein as “Kajiyama.”

151. Similar to the '764 patent, Kajiyama relates to semiconductor devices and, more particularly, to “insulating gate type field effect transistors having a gate dielectric film (high dielectric constant material).” Ex.1011, Cover, ¶1. As shown below in Figure 1(D), for example, Kajiyama’s semiconductor device includes a gate electrode surrounded by double sidewalls.

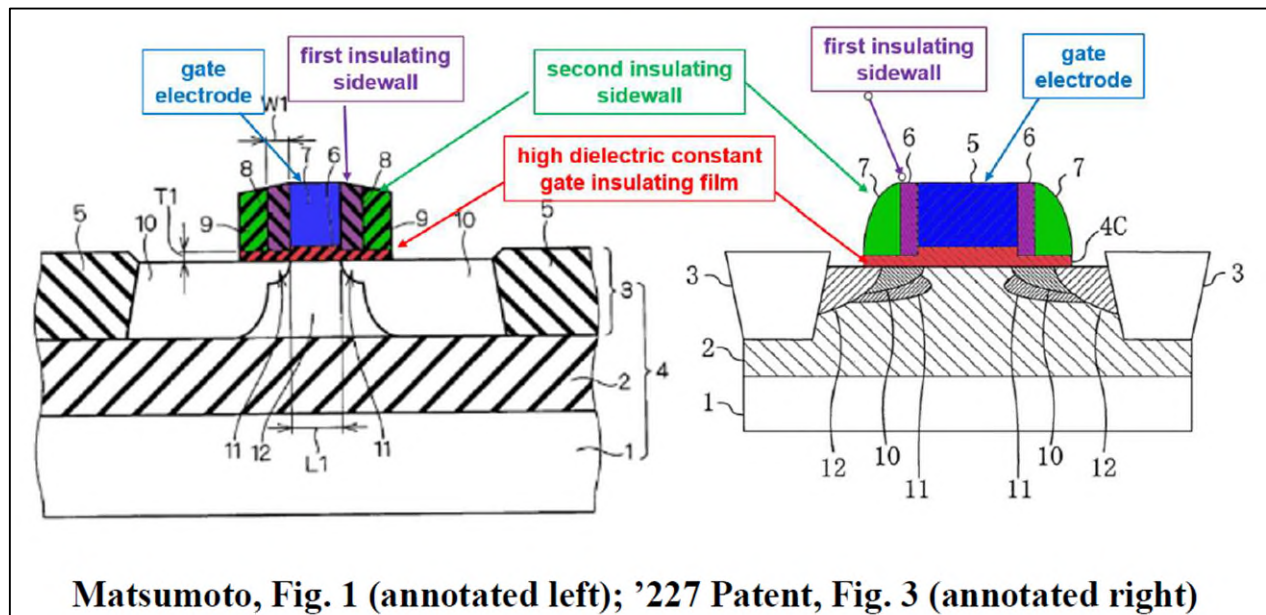


152. A gate insulating film extends from under the gate electrode to under only the first sidewall, which is interposed between the second sidewall and the gate electrode. Ex.1011, ¶28, FIG. 1(D) (above). The gate insulating film is thicker under the gate electrode than under the first sidewall. *Id.*

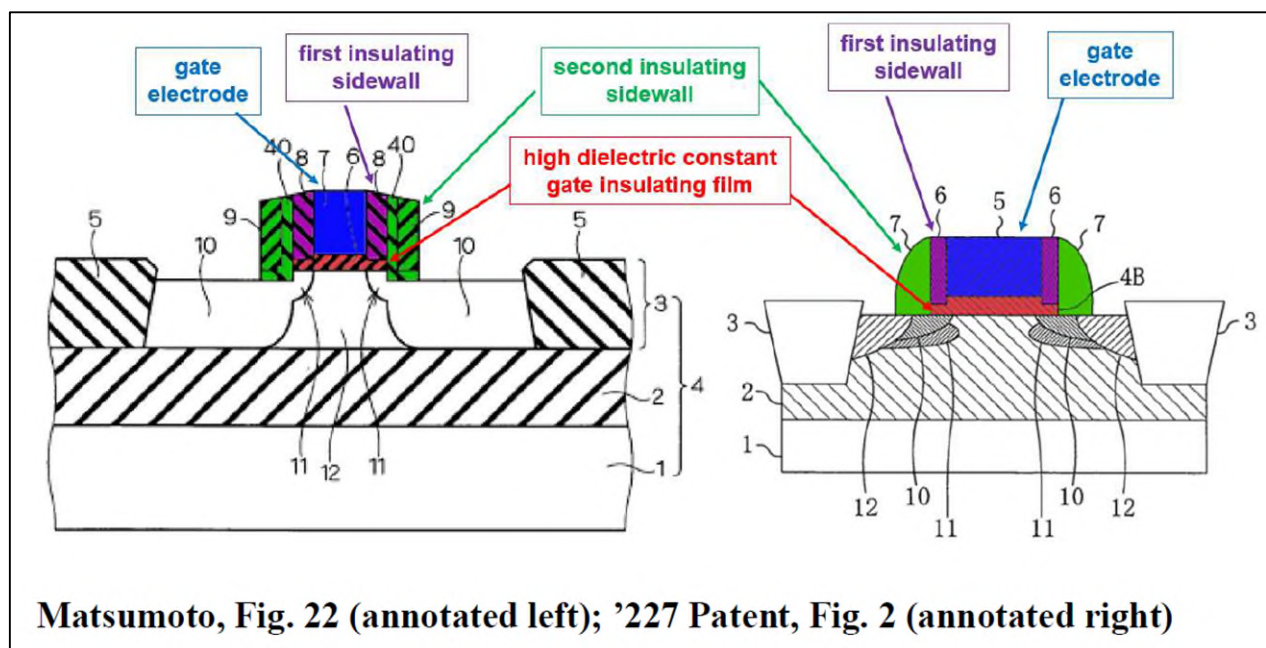
X. SPECIFIC GROUNDS FOR PETITION

A. Ground I

153. The semiconductor device of Matsumoto's first embodiment is represented below proximate an exemplary semiconductor device disclosed by the '764 patent to illustrate the similarity of those devices. See Ex.1009, FIG. 1 (below, left); Ex.1001, FIG. 3 (below, right).



154. The semiconductor device of Matsumoto's fourth embodiment is represented below proximate an exemplary semiconductor device disclosed by the '764 patent to illustrate the similarity of those devices. See Ex.1009, FIG. 22 (below, left); Ex.1001, FIG. 2 (below, right).



155. In my opinion, at least Matsumoto's first and/or fourth embodiments render obvious Challenged Claims 1 and 2 of the '764 patent (Ground I), as explained in detail below.

1. Independent Claim 1

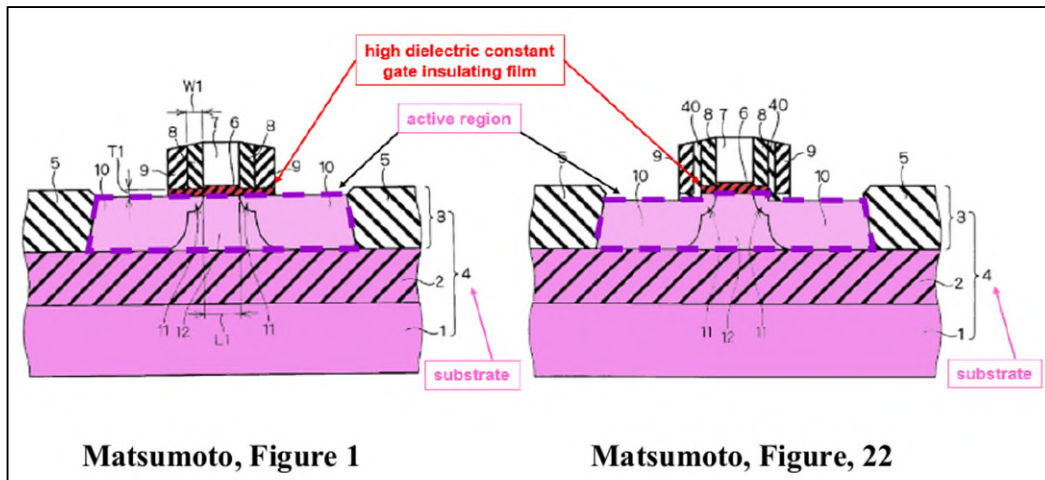
a. Preamble: "A semiconductor device comprising:"

156. Matsumoto's first and fourth embodiments each disclose a semiconductor device, as shown in Figures 1 and 22 of Matsumoto, above. See Ex.1009, FIGS. 1, 22. Matsumoto also is entitled "Semiconductor device and method of manufacturing same," and discloses that "[t]he present invention relates to a semiconductor device." See e.g., Ex.1009, Cover, ¶¶2, 102, 137, Abstract ("A semiconductor device"). Therefore, it is my opinion that Matsumoto discloses the preamble of claim 1 of the '764 patent.

b. Limitation 1[a]: "a high dielectric constant gate insulating film formed on an active region in a substrate;"

157. Matsumoto discloses that its first and fourth embodiments each includes a multi-layer SOI substrate 4 (see Ex.1009, FIGS. 1 (below, left), 22 (below, right) (shaded pink)) that includes silicon substrate 1, BOX layer 2 and single-crystalline silicon layer 3 "stacked in the order named." Ex.1009, ¶102; see *also* Ex.1009, ¶137 (relating process steps of first embodiment through forming gate

electrode to fourth embodiment), ¶140 (relating fourth embodiment to first embodiment).



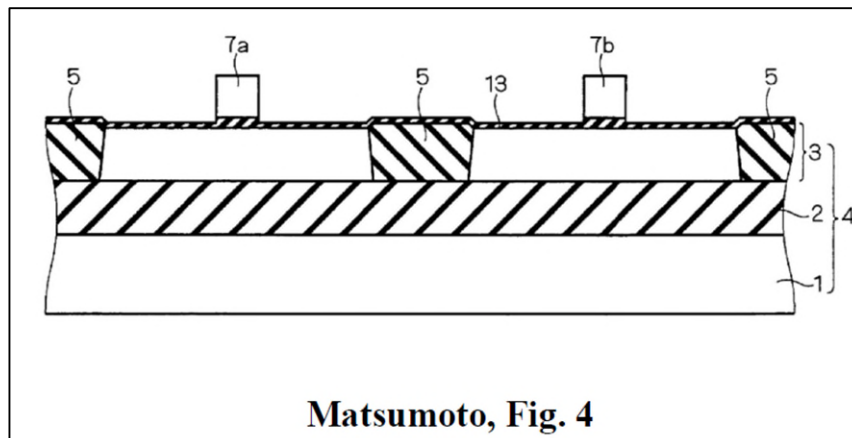
158. Matsumoto also explains that the first and fourth embodiment semiconductor devices each includes an active region in the substrate. For example, Matsumoto discloses that “isolating insulation film 5 extends from the upper surface of the silicon layer 3 to the upper surface of the BOX layer 2,” and that the “MOSFET is formed in a device region defined by the isolating insulation film 5.” Ex.1009, ¶¶102-03. In my opinion, the device region, identified by isolation regions, is an “active region in a substrate” and includes source/drain regions 10. *Id.*, ¶¶103-05, 139.

159. My opinion is consistent with the disclosure of the '764 patent, which confirms that the boundaries of an “active region” are defined by isolation structures. See Ex.1001, 1:34-35 (“The region of the well 102 surrounded by the STI serves as

an active region of a substrate 101”), 7:26-43 (active region includes source/drain regions surrounded by STI isolation structures).

160. In my opinion a POSITA would have understood Matsumoto’s film 6 to be the claimed gate insulating film. Ex.1009, ¶103 (referring to film 6 as a “gate insulation film”). In both Matsumoto’s first and fourth embodiments, “silicon oxide film 6 is formed partially on the upper surface of the silicon layer 3” in the device region and gate electrode 7 “is formed partially on the silicon oxide film 6.” Ex.1009, ¶103 (first embodiment), ¶137 (in the fourth embodiment, “gate electrode 7 is formed by the process described in the first embodiment”).

161. This fabrication process disclosed by Matsumoto is performed by forming film 13 on the substrate, as shown in Figure 4, below.



After one or more sidewalls are formed, film 13 is etched to form film 6. See Ex.1009, ¶107, FIGS. 1, 9-10, ¶114 (first embodiment); Ex.1009, ¶138, FIGS. 18-19, 22 (fourth embodiment).

162. Although Matsumoto does not recite the words “high dielectric constant” to describe its gate insulating film, in my opinion, a POSITA would have understood Matsumoto to disclose the use of a high dielectric constant (high-k) gate insulating film. At a minimum, a POSITA would have considered it obvious in my opinion because Matsumoto teaches that “[a] A silicon oxynitride film, a metal oxide film such as Al_2O_3 or a ferroelectric film such as Ta_2O_5 and BST may be formed in place of the silicon oxide film 13.” Ex.1009, ¶107. Al_2O_3 , Ta_2O_5 , and BST are, and a POSITA would have understood them to be, high-k dielectrics. See Ex.1018, Table I (identifying Al_2O_3 , Ta_2O_5 as high-k dielectrics).

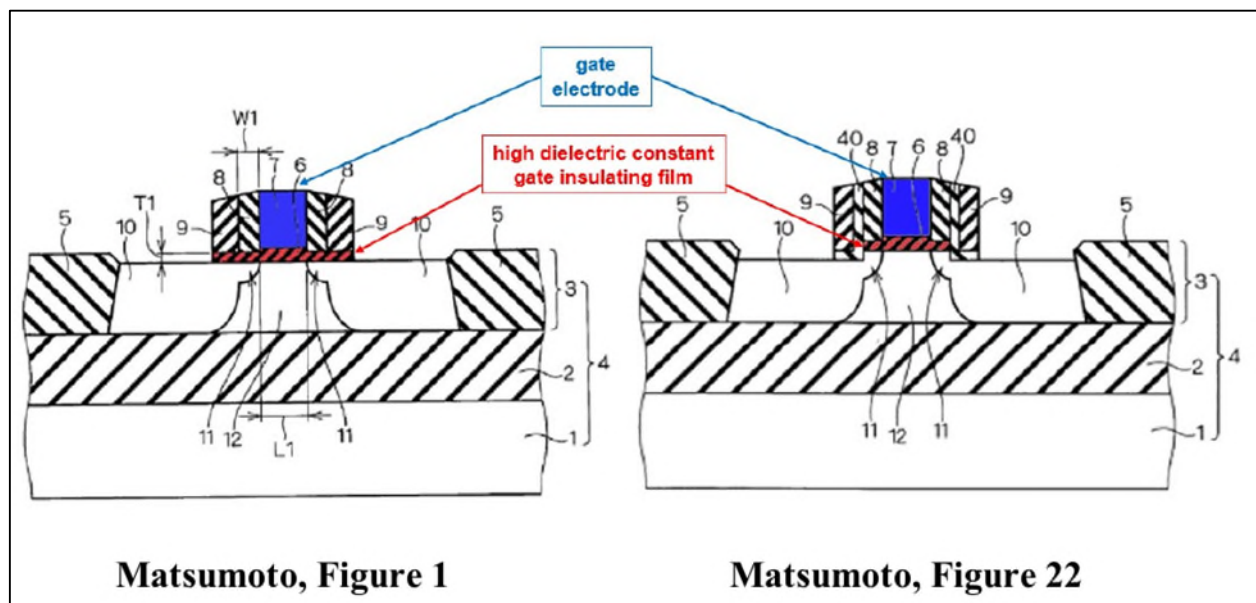
163. The '764 patent itself acknowledges that the metal oxide films recited in Matsumoto for its gate insulating film are high-k dielectrics, explaining that it was known to use, “as a gate insulating film of a MISFET, a high dielectric constant film formed of a Hf based oxide, Al based oxide or the like, which has a relative dielectric constant of 10 or more.” Ex.1001, 1:21-25. Al_2O_3 , as disclosed by Matsumoto, is an example of an “Al based oxide” as recited by the '764 patent, and Ta_2O_5 and BST would also have been understood by a POSITA to have dielectric constants greater than 10.

164. In my opinion, a POSITA would have been motivated to use a high-k dielectric in the first and/or fourth embodiment devices of Matsumoto, such as those materials expressly disclosed by Matsumoto, to address the well-documented issues

with silicon dioxide gate dielectrics in ultra-large-scale integration devices having scaled down features. *See* Ex.1333, 54. Therefore, it is my further opinion that Matsumoto discloses this limitation.

c. Limitation 1[b]: “a gate electrode formed on the high dielectric constant gate insulating film; and”

165. In both Matsumoto's first and fourth embodiment semiconductor devices, "gate electrode 7 [shaded blue] made of polysilicon is formed partially" on high-k insulating film 6 (shaded red). Ex.1009, ¶¶103, ¶107 (describing formation of high-k insulating film and gate electrode) 137-38, FIGS. 1 (below, left), 22 (below, right).



166. Therefore, it is my opinion that Matsumoto discloses this limitation.

d. Limitation 1[c]: “a first insulating sidewall formed on each side surface of the gate electrode; and”

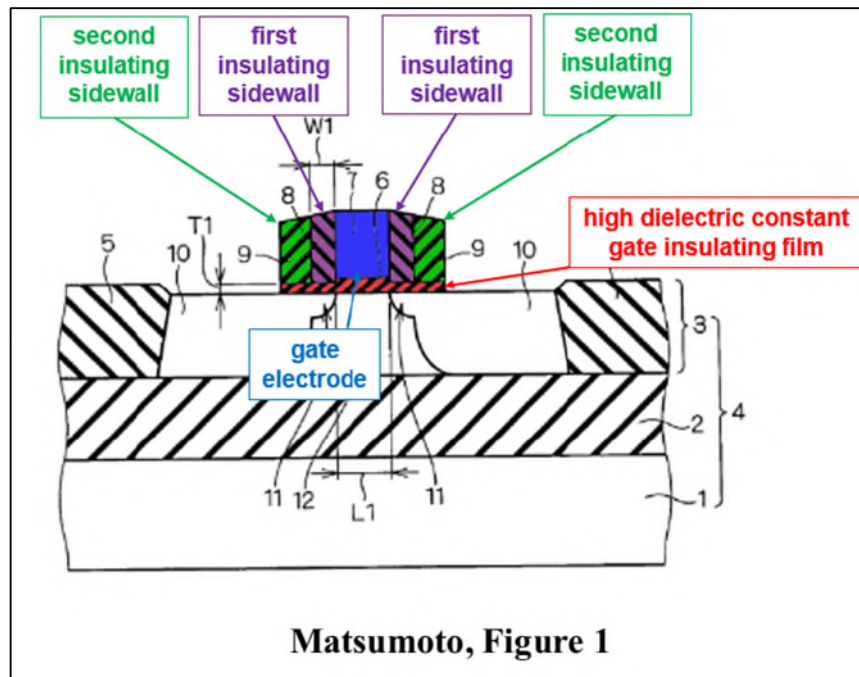
Limitation 1[d]: “a second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween,”

167. In Matsumoto’s first embodiment semiconductor device, “silicon nitride film 9 is formed on each side surface of the gate electrode 7, with a silicon oxide film 8 therebetween.” Ex.1009, ¶103. In my opinion, a POSITA would have understood film 8 to be the claimed first insulating sidewall and film 9 to be the claimed second insulating sidewall.

168. Matsumoto expressly refers to film 9 as a “sidewall insulation film.” Ex.1009, ¶114 (describing nitride films 9a/9b “serving as sidewall insulation films”). While Matsumoto does not expressly refer to film 8 as a sidewall, in my opinion, a POSITA would have understood film 8 to also be a sidewall. *Id.*, ¶¶104, 110. A POSITA also would have known that silicon oxide and silicon nitride are both insulators, and thus films 8 and 9 are insulating sidewalls. *See id.*, ¶¶110 (“This forms silicon oxide films 8a and 8b on the side surfaces of the gate electrodes 7a and 7b.”), 114 (“This forms silicon nitride films 9a and 9b serving as sidewall insulation films on the outer side surfaces of the silicon oxide films 8a and 8b.”), claim 1 (“a pair of second insulation films having respective inner side surfaces in contact with

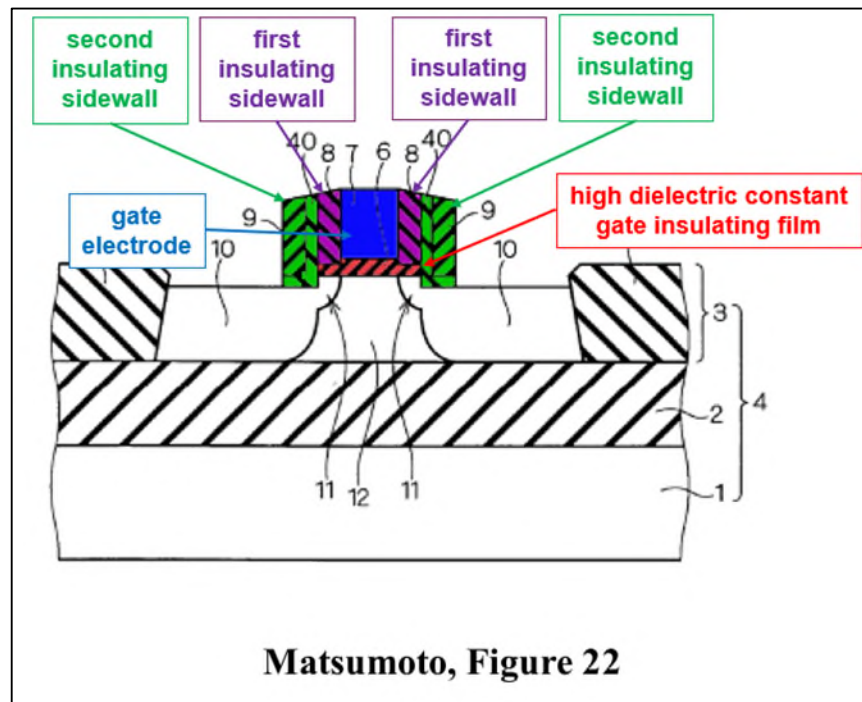
side surfaces of said gate electrode and respective outer side surfaces out of contact with said side surfaces of said gate electrode, with said gate electrode disposed between said pair of second insulation films”).

169. My opinion that Matsumoto’s silicon oxide film 8 and silicon nitride film 9 of its first embodiment are the claimed first and second insulating sidewalls, respectively, formed on each side surface of the gate electrode is consistent with the disclosure of the ’764 patent because film 8 (see Ex.1009, FIG. 1 (below) (shaded purple)) is a first insulating sidewall formed on a side surface of the gate electrode and film 9 (see *id.*, FIG. 1 (below) (shaded green)) is a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween.



170. I note that the '764 patent uses the term “insulating sidewall” broadly in my opinion to refer to a single component (Ex.1001, 5:66-67), a collective structure of two components (*id.*, 3:17-22), and as a component having multiple layers (*id.*, 21:5-15). Additionally, the '764 patent uses the term “formed on” generally to refer to location and not to require contact. *See e.g.*, Ex.1001, 1:31-33, 7:28-32. For example, claim 1 recites “a second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween.” *Id.*, claim 1. The second insulating sidewall is still “formed on the side surface of the gate electrode” even though “the first insulating sidewall [is] interposed therebetween,” meaning that the second insulating sidewall does not directly contact the gate electrode.

171. In Matsumoto’s fourth embodiment, silicon oxide film 40 and silicon nitride film 9 are formed “on the outer side surfaces of” film 8, as illustrated below in Figure 22.



172. Silicon oxide film 8, silicon oxide film 40, and silicon nitride film 9 are collectively an insulating sidewall with film 8 (*see* Ex.1009, FIG. 22 (above) (shaded purple)) being a first insulating sidewall and film 9 (*see id.*, shaded green)) alone, film 40 (*see id.* (shaded green)) alone, or their combination being a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween, consistent with the disclosures of the '764 patent. Ex.1001, 3:17-22, 21:515.

173. Additionally, Figure 23 of Matsumoto shows a modification of Matsumoto's fourth embodiment. Ex.1009, ¶141 ("FIG. 23 is a sectional view showing a first modification of the method of manufacturing the semiconductor device according to the fourth preferred embodiment. ... The technique of the first

modification of the fourth preferred embodiment is applicable to any one of the first to fourth preferred embodiments.”). In Figure 23, film 9 replaces films 40 and 9 of Figure 22. *Id.*, FIGS. 22-23. In my opinion, a POSITA would have understood from these teachings that films 40 and 9 in Figure 22 can also be considered the claimed second insulating sidewall.

174. Therefore, it is my opinion that Matsumoto discloses these limitations of claim 1 of the '764 patent.

e. Limitation 1[e]: “wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, and”

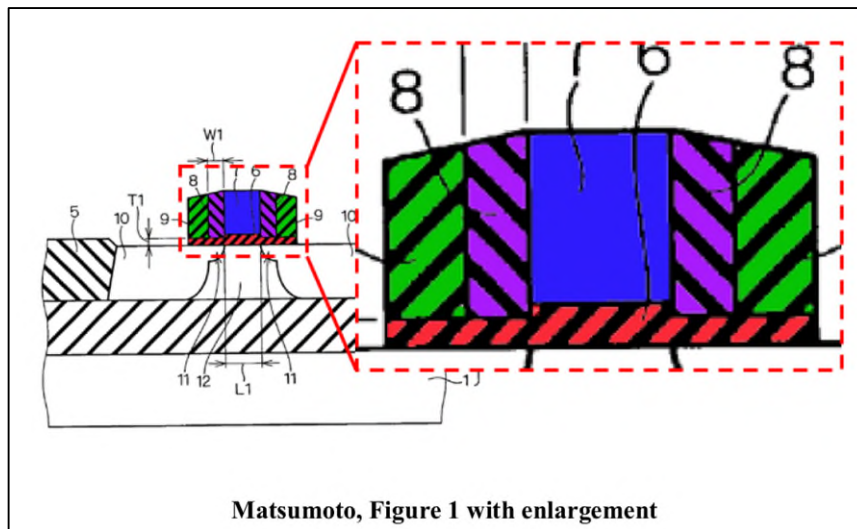
Limitation 1[f]: “part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.”

175. Limitation 1[e] recites “the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall” and limitation 1[f] recites “at least part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.” These limitations focus on the dimensions (e.g.,

width and thickness) of the gate insulating film in relation to the gate electrode and insulating sidewalls, which, in my opinion, are disclosed in both Matsumoto's first and fourth embodiment semiconductor devices, as I explain in detail below.

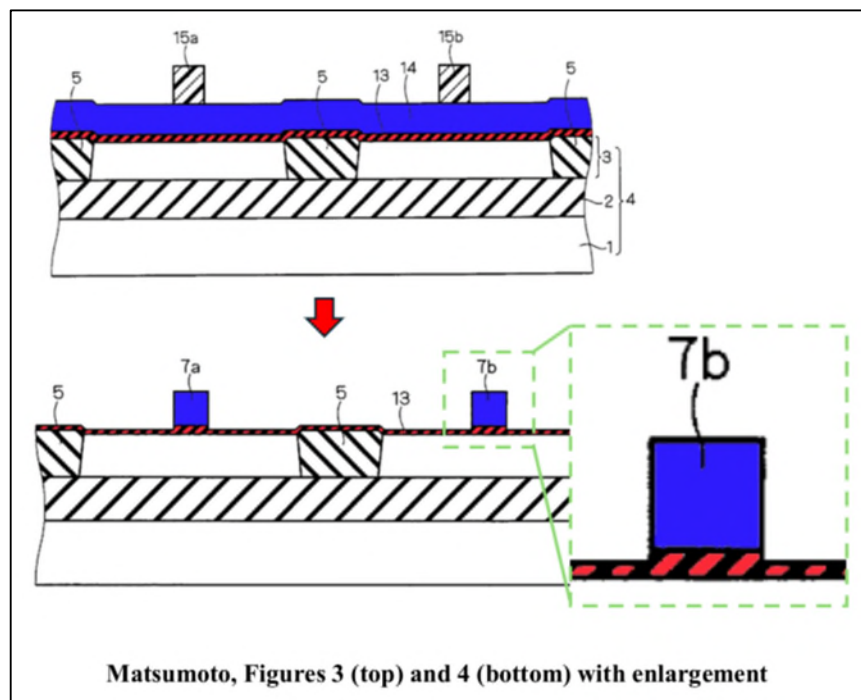
(1) Matsumoto's First Embodiment

176. In Matsumoto's first embodiment, the gate insulating film 6 (*see* Ex.1009, FIG. 1 (below) (shaded red)) is an uninterrupted layer (as evidenced by the absence of gaps) that extends from under the gate electrode 7 to under film 8 (*see id.*, FIG. 1 (below) (shaded purple)).



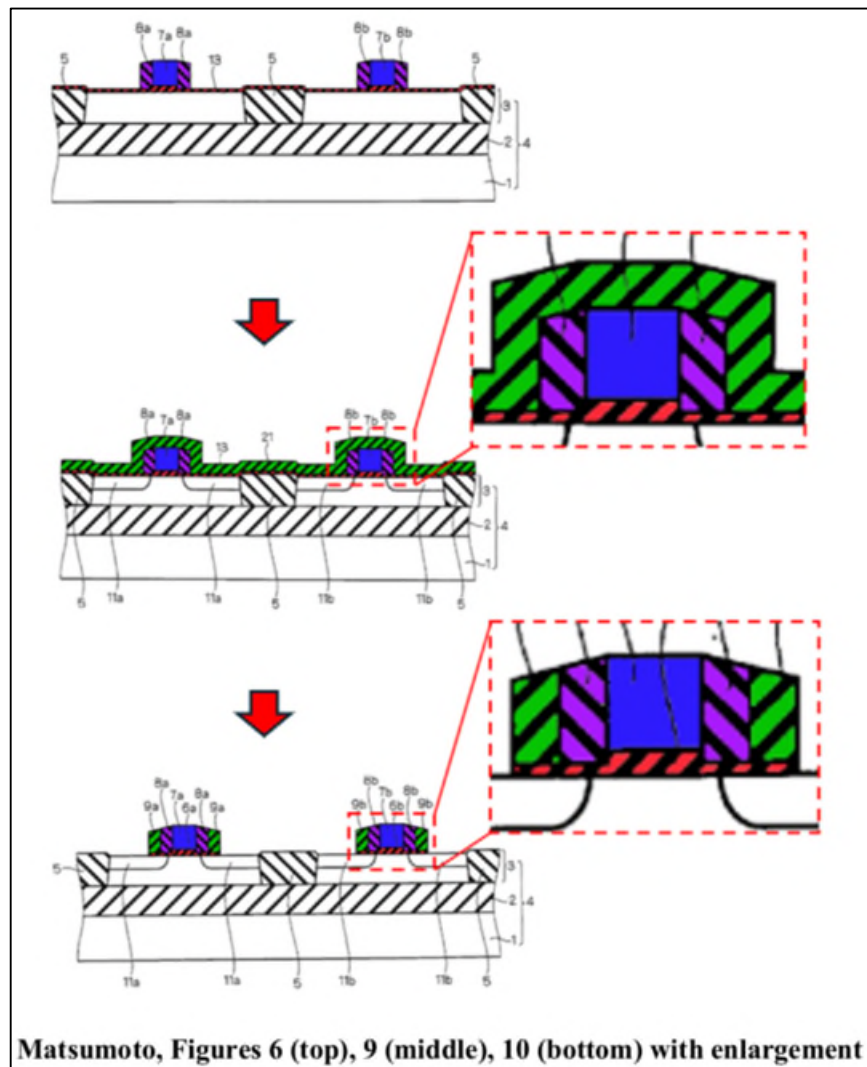
In my opinion, film 8 is the claimed first insulating sidewall, as explained above. Matsumoto also discloses in Figure 1 that gate insulating film 6 is thinner under film 8 (i.e., the claimed first insulating sidewall) than it is under the gate electrode 7 (*see id.*, FIG. 1 (above) (shaded blue)).

177. In my opinion, the larger thickness of the gate insulating film under the gate electrode compared to under the first insulating sidewall in Matsumoto's first embodiment semiconductor device is confirmed by Matsumoto's fabrication process. In that process, dielectric film 13 (see Ex.1009, FIGS. 3-4 (below) (shaded red)) is formed on the substrate and polysilicon film 14 (see *id.* (shaded blue)) is formed on high-k dielectric film 13. See also Ex.1009, ¶107.



178. The etching process used to form the gate electrodes (7a and 7b) “slightly etches the upper surface of” film 13, resulting in a high-k dielectric film with a larger thickness under the gate electrode than in the areas not under the gate electrode. Ex.1009, ¶108, FIG. 4 (above, bottom).

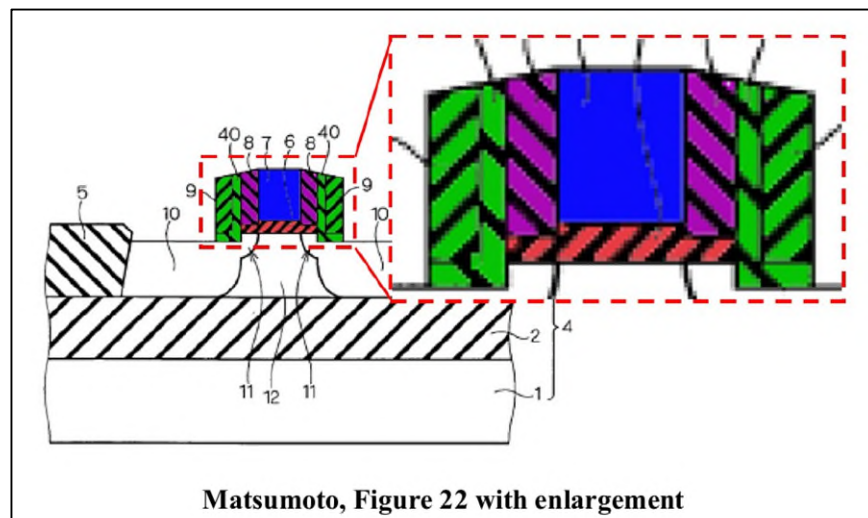
179. Matsumoto's manufacturing process also confirms that gate insulating film 6 is continuously formed so as to extend from under the gate electrode to under the insulating sidewall in my opinion. The dielectric film 13 that forms the gate insulating film 6 is formed continuously as one layer. *See* Ex.1009, FIGS. 3-4. After formation of sidewalls 8a/8b ("first insulating sidewall"; *see id.*, FIGS. 6, 9-10 (shaded purple)), silicon nitride film 21 is "formed on the entire top surface" of the intermediate structure. *Id.*, ¶¶109-10, 114, FIGS. 6 (below, top), 9 (below, middle). Film 21 and film 13 are then etched "until the upper surface of the silicon layer 3 is exposed," forming sidewalls 9a/9b ("second insulating sidewall"; *see id.*, FIGS. 6, 9 (below) (shaded green)). Ex.1009, ¶114. After this etching, the high-k dielectric film (*see id.*, FIGS. 6, 9-10 (below) (shaded red)) remains under the gate electrode and first and second sidewalls.



180. Through this process, the gate insulating film 6 is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, because gate insulating film 6 is formed by etching film 13, which was continuously formed, in the areas not covered by sidewall insulating films 8 and 9. Thus, it is my opinion that Matsumoto's first embodiment semiconductor device discloses these limitations of claim 1 of the '764 patent.

(2) Matsumoto's Fourth Embodiment

181. In Matsumoto's fourth embodiment semiconductor device, gate insulating film 6 (see Ex.1009, FIG. 22 (below) (shaded red)) is an uninterrupted layer (as evidenced by the absence of gaps) that extends from under the gate electrode to under only film 8, but not under films 9 and 40. In my opinion, film 8 *see id.* (shaded purple)) is the claimed "first insulating sidewall," as explained above.



182. In this fourth embodiment of Matsumoto, gate insulating film 6 is thinner under film 8 (i.e., the "first insulating sidewall") than it is under the gate electrode 7 (see Ex.1009, FIG. 22 (above) (shaded blue)).

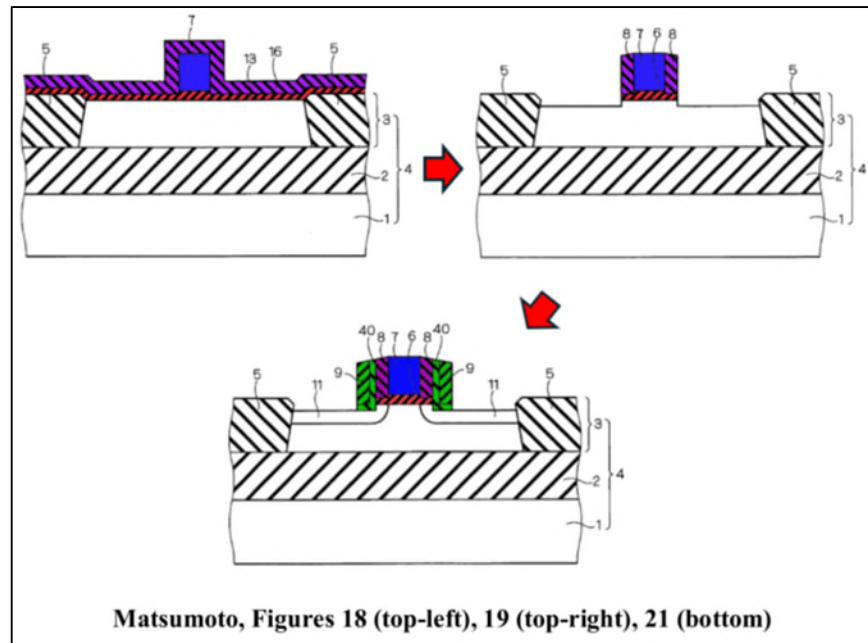
183. In my opinion, the larger thickness of the gate insulating film under the gate electrode compared to under the first insulating sidewall in Matsumoto's fourth embodiment semiconductor device is confirmed by Matsumoto's fabrication process. "[G]ate electrode 7 is formed by the process described in the first preferred

embodiment, and thereafter the silicon oxide film 16 is formed on the entire top surface of the resultant structure by a CVD process.” See Ex.1009, ¶¶137, 108. As explained above with respect to Matsumoto’s first embodiment, this process “slightly etches the upper surface of” film 13. See Ex.1009, ¶108. The “slight etching” of film 13 in the areas not covered by the gate electrode result in the dielectric film having a larger thickness under the gate electrode than in the areas not under the gate electrode. See also Ex.1009, FIGS. 3-4, above.)

184. Matsumoto’s manufacturing process also confirms that gate insulating film 6 is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall in my opinion. The dielectric film 13 that forms the gate insulating film 6 is formed continuously as one layer. See Ex.1009, FIGS. 3-4. After formation of the gate electrode, sidewalls 8 are formed. Ex.1009, ¶138. The etching process that forms sidewalls 8 (i.e., “the first insulating sidewall”; see *id.* FIGS. 18-19, 21 (below) (shaded purple)) “is continued to overetch the upper surface of the silicon layer 3 exposed by the etching of the silicon oxide film 16.” *Id.*, ¶138, FIGS. 18-19.

185. As a result, the high-k dielectric film (see *id.*, FIGS. 18-19, 21 (below) (shaded red)) remains only under the gate electrode and first insulating sidewall 8. *Id.*, ¶138, FIG. 19 (below, top-right). Film 40 and film 9 (alone or in combination the claimed “second insulating sidewall” (see Ex.1009, FIG. 21 (below, bottom)

(shaded green)) are then formed on the outer side surfaces of film 8 and on the substrate surface. *Id.*, ¶139.



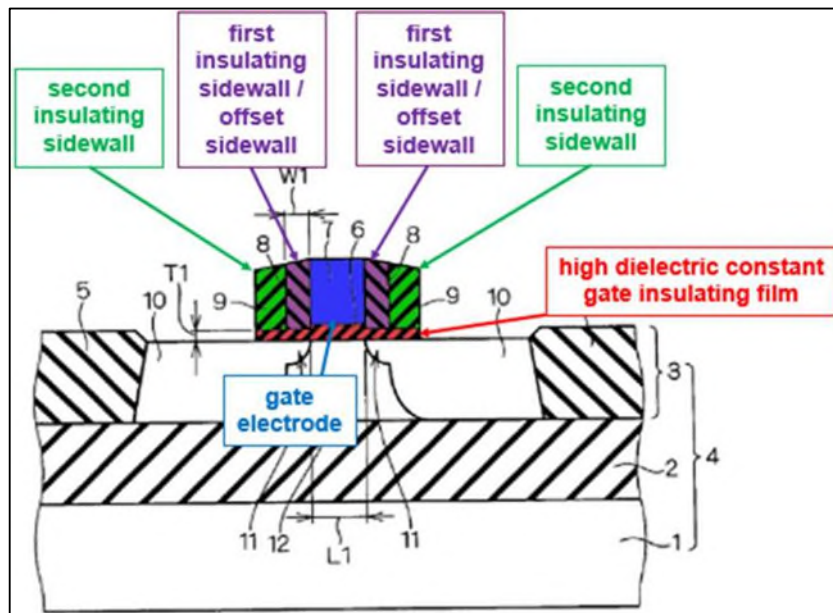
186. Through this process, the gate insulating film 6 is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, because gate insulating film 6 is formed by etching film 13, which was continuously formed, in the areas not covered by sidewall insulating films 8. Therefore, it is my opinion that Matsumoto's fourth embodiment semiconductor device also discloses these limitations of claim 1 of the '764 patent.

2. Dependent Claim 4: "The semiconductor device of claim 1, wherein the first insulating sidewall is an offset sidewall."

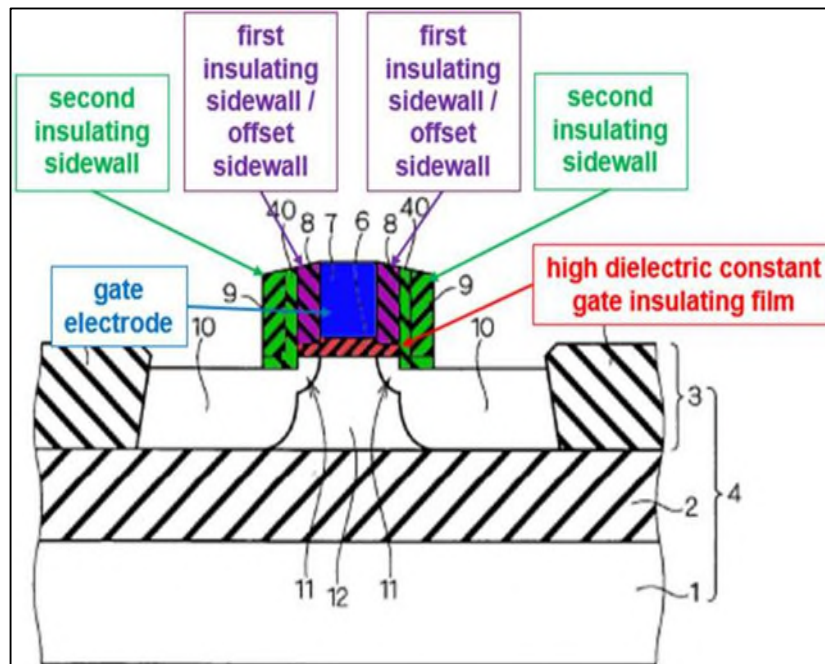
187. In Matsumoto's first and fourth embodiments, film 8 is the claimed "first insulating sidewall," as explained above. Matsumoto expressly refers to film

8, which is located between gate electrode 7 and the second insulating sidewall, as an “offset insulation film.” Ex.1009, ¶155 (“The relationship between the width W1 of the silicon oxide film 8 serving as an offset insulation film”), ¶157 (“FIG. 28 is a graph of the width W1 of the offset insulation film versus the delay time t_{pd} ...), FIG. 1 (below, showing width W1).

188. Matsumoto’s film 8 (*see* Ex.1009, FIGS. 1, 22 (below) (shaded purple)) is also formed on the sidewalls of the gate electrode (*see id.* (shaded blue)). Accordingly, in Matsumoto’s first and fourth embodiment devices, film 8 is an offset sidewall. *See* Ex.1001, 7:37-39 (referring to the inner sidewall as an offset sidewall), Figure 2; Ex.1334, FIG. 5-25. Therefore, it is my opinion that Matsumoto discloses claim 4 of the ’764 patent.



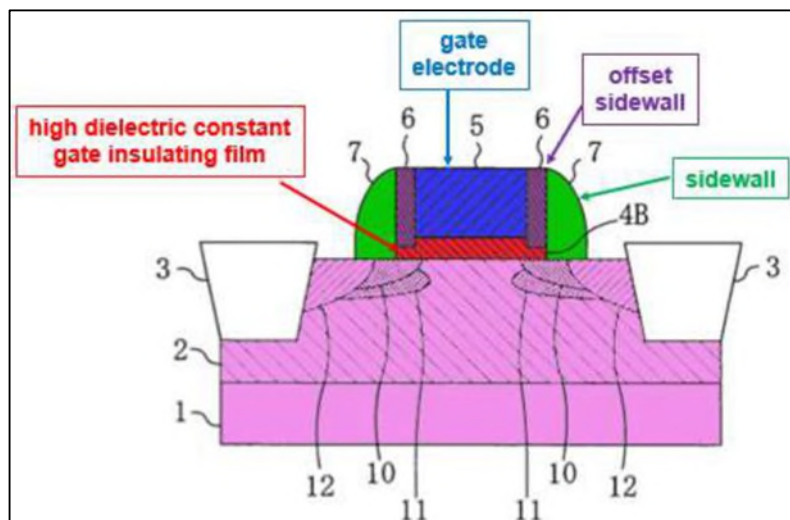
Matsumoto, Fig. 1 (annotated)



Matsumoto, Fig. 22 (annotated)

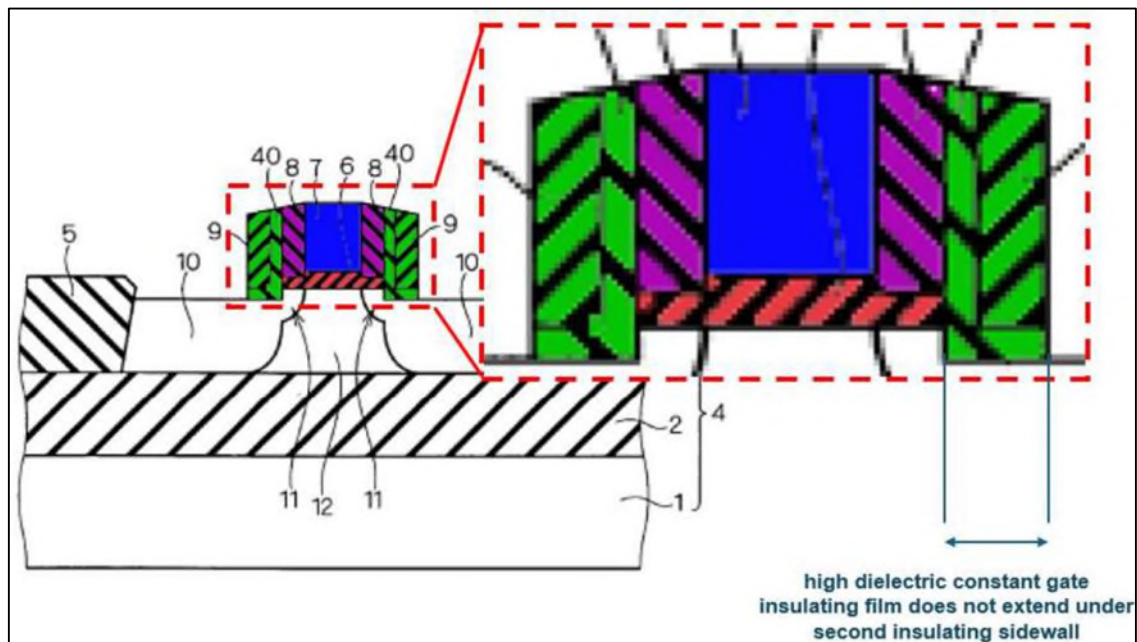
3. Dependent Claim 5: “The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall.”

189. As illustrated in Figure 2 of the '764 patent, the high-k gate insulating film (shaded red) extends under first, or inner, sidewall 6 (shaded purple) and has a smaller thickness under inner sidewall 6 than under gate electrode 5 (shaded blue) but does not extend under the second sidewall 7 (shaded green).



'764 Patent, Fig. 2 (annotated)

190. Matsumoto's fourth embodiment discloses a similar structure. As shown in Figure 22 of Matsumoto, below, and discussed above with regard to limitations 1[e]-1[f], the gate insulating film 6 of Matsumoto's fourth embodiment (shaded red) extends only under the film 8 (i.e., the claimed first insulating sidewall) but not under films 40 and 9 (alone or collectively the claimed "second insulating sidewall").



Matsumoto, Fig. 22 (annotated and enlarged)

191. Therefore, it is my opinion that Matsumoto discloses claim 5 of the '764 patent.

4. Dependent Claim 14: “The semiconductor device of claim 1, wherein the second insulating sidewall has a double layer structure including an oxide film and a nitride film.”

192. As discussed above with regard limitations 1[c]-1[d], silicon nitride film 9 and silicon oxide film 40 collectively disclose the claimed “second insulating sidewall,” as illustrated in Figure 22 of Matsumoto, for example. In my opinion, a POSITA would have understood these two films to be “layers” of the collective sidewall structure, consistent with the disclosures of the '764 patent. *See e.g.*, Ex.1001, 20:66-21:8 (“In each of the first through eighth embodiments, a single layer structure of a SiN film has been used as an example of the sidewall 7. However,

instead of the single layer structure of a SiN film, for example, a double layer structure of a combination of an oxide film (SiO₂ film) and a nitride film (SiN film) (for example, including a SiO₂ layer as a lower layer and a SiN film as an upper layer), a triple layer structure (for example including an SiO₂ film as a lower layer, a SiN film as a middle layer and a SiO₂ film as an upper layer) or the like may be used.”)

193. Silicon nitride film 9 is an example of a nitride film, and silicon oxide film 40 is an example of an oxide film, as claimed. For these reasons, Matsumoto’s fourth embodiment discloses that the second insulating sidewall has a double layer structure including an oxide film and a nitride film and it is therefore my opinion that Matsumoto discloses claim 14 of the ’764 patent.

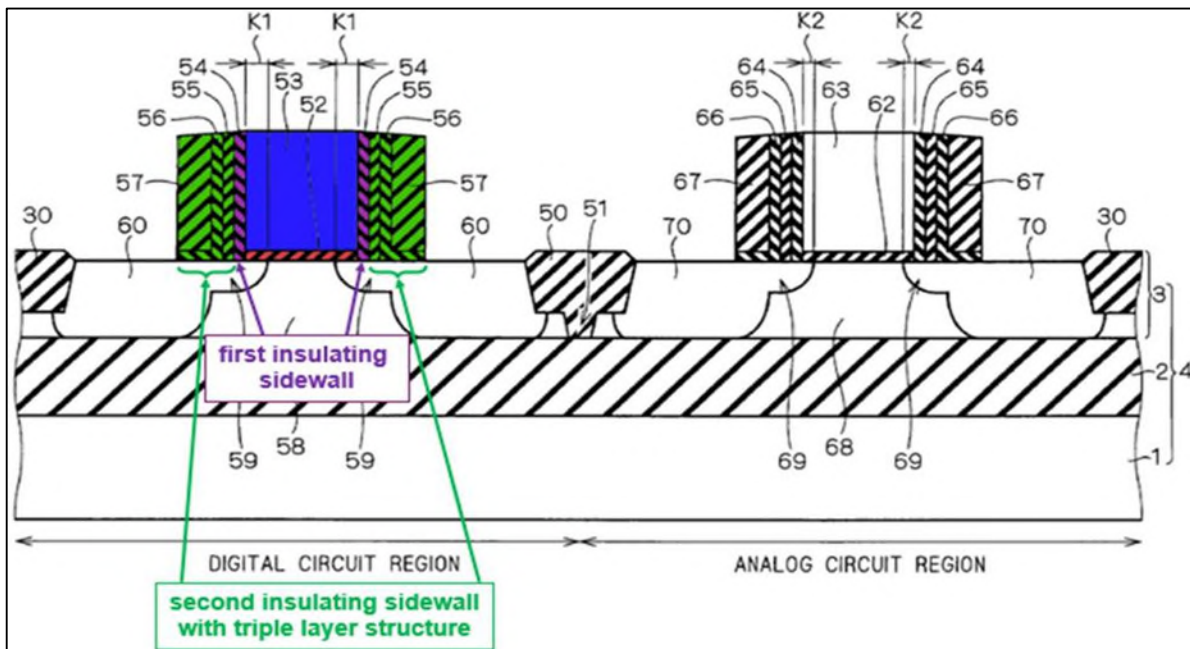
5. Dependent Claim 15: “The semiconductor device of claim 1, wherein the second insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film.”

194. As discussed above with regard to claim 14, in its fourth embodiment (*see e.g.*, Ex.1009, FIG. 22), Matsumoto discloses a second insulating sidewall with a double layer structure including an oxide film and a nitride film.

195. Matsumoto also discloses a digital FET, isolated from analog device regions, that includes additional layers. For example, the device shown in Matsumoto’s Figure 29 below includes silicon oxide film 54 (shaded purple) “formed in contact with each side surface of the gate electrode 53.” Ex.1009, ¶¶160,

162. Film 54 functions as an “offset insulation film.” Ex.1009, ¶162. Beyond this layer, “[a] silicon oxide film 55 is formed outside the silicon oxide film 54,” followed by a structure containing “a silicon oxide film 56 and a silicon nitride film 57.” Ex.1009, ¶162.

196. In my opinion, a POSITA would have considered this structure including films 55, 56, and 57 to be a second insulating sidewall with a triple layer structure. More specifically, silicon oxide film 55 (“*a first oxide film*”), silicon oxide film 56 (“*a second oxide film*”), and silicon nitride film 57 (i.e., the claimed nitride film) form a second insulating sidewall with a triple layer structure including a first oxide film, a nitride film and a second oxide film.



Matsumoto, Fig. 29 (annotated)

197. Should an argument be made that the gate insulating film in Matsumoto’s Figure 29 (above) does not extend under the insulating sidewalls, in my opinion, such a modification would have been obvious to a POSITA in light of at least Matsumoto’s fourth embodiment.

198. For example, in my opinion, it would have been obvious to a POSITA to modify Matsumoto’s fourth embodiment device by adding an additional oxide layer to the existing second insulating sidewall, which includes silicon nitride film 9 and silicon oxide film 40, as disclosed in Matsumoto’s sixth embodiment shown in Figure 29. Indeed, Matsumoto explicitly teaches that “[t]he structure according to the sixth preferred embodiment is applicable to the semiconductor device of any one of the first to fifth preferred embodiments.” Ex.1009, ¶159.

199. Therefore, it is my opinion that Matsumoto discloses claim 15 of the '764 patent.

6. **Dependent Claim 16: “The semiconductor device of claim 1, wherein a width of the high dielectric constant gate insulating film along a gate length is larger than a width of the gate electrode along the gate length.”**

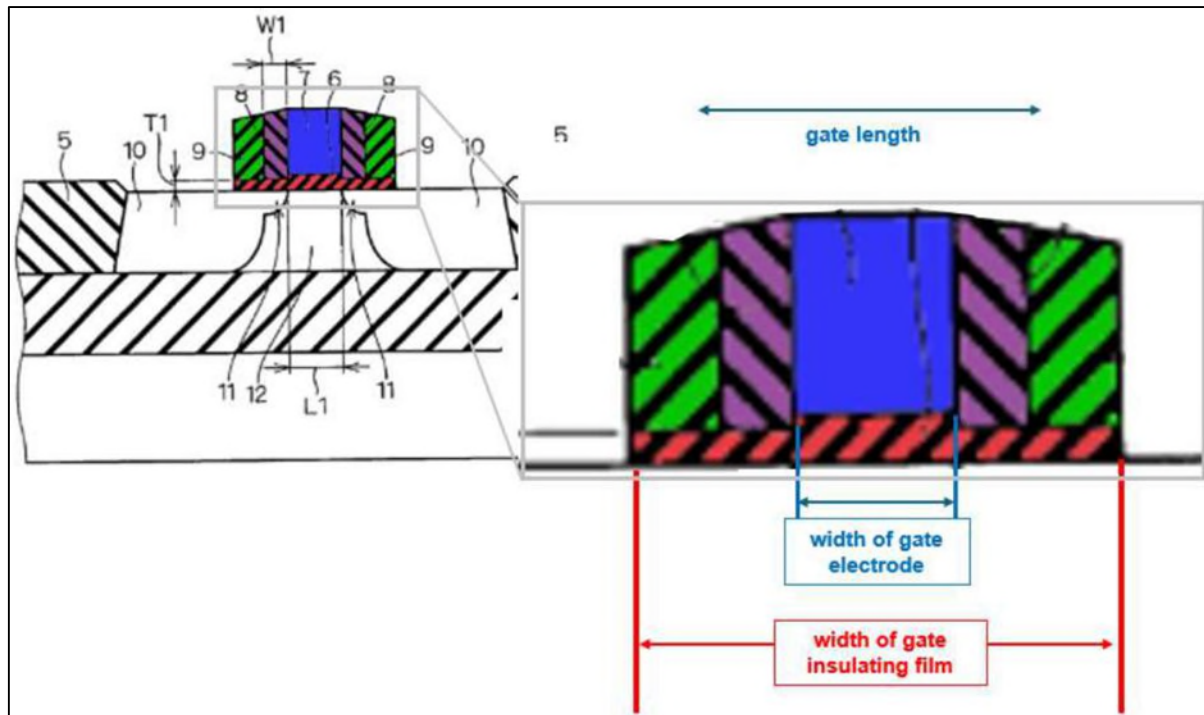
Dependent Claim 17: “The semiconductor device of claim 1, wherein a width of a bottom surface of the high dielectric constant gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length.”

200. Dependent claims 16 and 17 address the width of the gate insulating film relative to the gate electrode. Matsumoto's first and fourth embodiments each teaches these limitations, as explained below. I note that the '764 patent uses the term “along the gate length” to refer to a direction, specifically from the source region to the drain region.

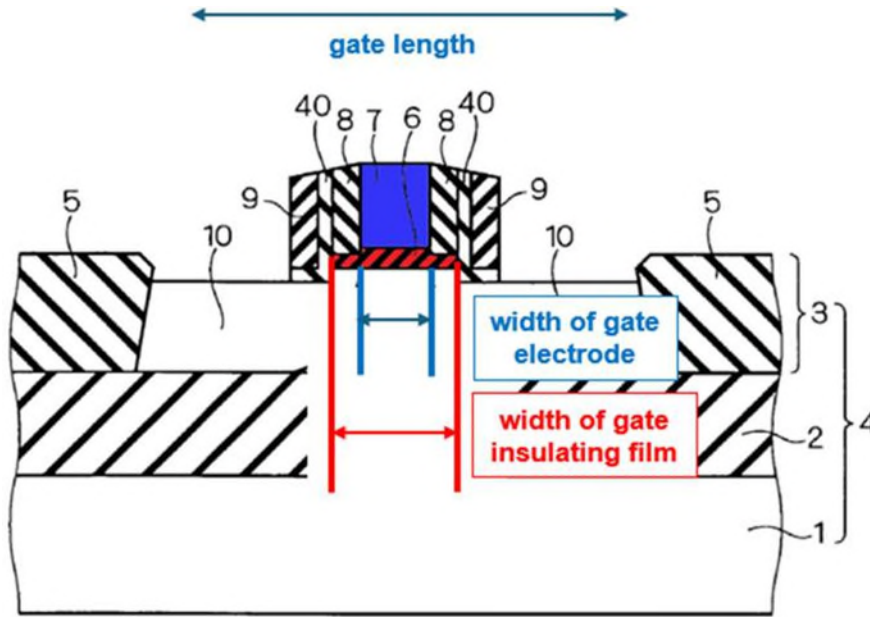
201. As I explained above with regard to limitation 1[e], the high-k gate insulating film 6 in Matsumoto's first and fourth embodiments extends from under the gate to under the first insulating sidewall 8, which is formed on the sidewalls of the gate electrode 7, as illustrated below in Figures 1 and 22.

202. More specifically, the width of Matsumoto's gate electrode 7 is constant across its entire height. In both Figures 1 and 22, the width of the high-k gate insulating film 6 (shaded red), including at film 6's bottom surface, is larger

than the width of the gate electrode 7 (shaded blue), including at gate electrode 7's bottom surface.



Matsumoto, Fig. 1 (annotated and enlarged)



Matsumoto, Fig. 22 (annotated)

203. The fabrication processes of both Matsumoto's first and fourth embodiments, discussed above with regard to limitations 1[e]-1[f], confirm the structures shown in Figures 1 and 22. Therefore, it is my opinion that Matsumoto discloses claims 16 and 17 of the '764 patent.

- 7. Dependent Claim 18: “The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more.”**

Dependent Claim 19: “The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall.”

204. Dependent claims 18 and 19 relate to the dielectric constant of the gate insulating film. In my opinion, Matsumoto's first and fourth embodiments disclose these limitations because the dielectric constants of materials disclosed by

Matsumoto for the gate insulating film and the second insulating sidewall are inherent to those materials. Even if that were not found to be the case, Matsumoto renders the limitations of claims 18 and 19 obvious based on knowledge of a POSITA in my opinion.

205. The claimed “relative dielectric constant” is an inherent property of a material. Indeed, the ’764 patent admits that a “high dielectric constant film formed of a Hf based oxide, Al based oxide or the like [] has a relative dielectric constant of 10 or more, instead of an SiO₂ based insulating film having a relative dielectric constant of about 4.” Ex.1001, 1:28-31. Matsumoto teaches that Ta₂O₅ is one example of a material that can be used to form the gate insulating film. Ex.1009, ¶107. The dielectric constant for Ta₂O₅ is known to be 26, which is greater than 10. See Ex.1018, Table I. Thus, the teachings of Matsumoto render obvious the limitations of claim 18.

206. As discussed above with regard limitations 1[c]-1[d], in Matsumoto’s first and fourth embodiments, sidewall film 9 is comprised of silicon nitride (Si₃N₄). The dielectric constant of Si₃N₄ is and was well-known to a POSITA to be approximately 7. See Ex.1018, Table 1; Ex.1352, FIG. 4 (disclosing that Si₃N₄ has dielectric constant of 7.2). Because Matsumoto’s sidewall film 9 is comprised of silicon nitride (Si₃N₄), which has a dielectric constant of 7, and Ta₂O₅ has a dielectric constant greater than 10 (see Ex.1009, ¶¶114, 139; Ex.1018, Table I), Matsumoto’s

first and fourth embodiments disclose that the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall, as recited by claim 19.

207. Therefore, it is my opinion that Matsumoto discloses claims 18-19 of the '764 patent.

B. Ground II

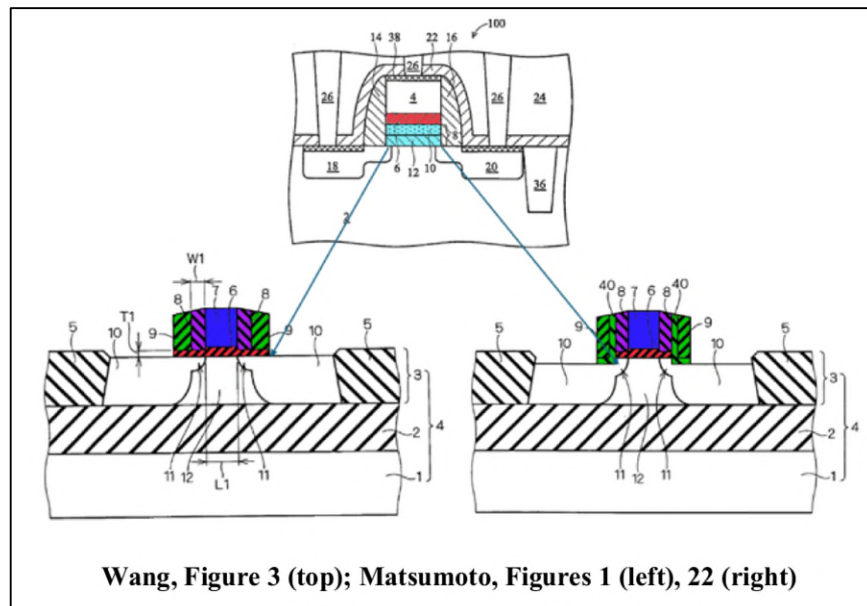
208. In my opinion, Matsumoto in combination with Wang renders obvious Challenged 2-3, 6-7, and 11 of the '764 patent (Ground II). As discussed above with regard to Ground I, Matsumoto discloses, or at least renders obvious, every limitation of claim 1 in my opinion. To the extent Matsumoto is found not to disclose the additional limitations of claims 2-3, 6-7, and/or 11, Wang teaches the limitations of those claims, as explained below. In my opinion, a POSITA would have been motivated to combine these references, thereby rendering obvious claims 2-3, 6-7, and 11.

1. **Dependent Claim 2: “The semiconductor device of claim 1, further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film.”**

Dependent Claim 3: “The semiconductor device of claim 2, wherein the buffer insulating film is a silicon oxide film.”

209. In my opinion, a POSITA would have been motivated to combine Wang’s disclosure of an underlying dielectric layer, as a buffer layer between a high-

k dielectric and silicon substrate, with Matsumoto's first and/or fourth embodiment semiconductor devices. The resulting semiconductor device would have included Wang's underlying dielectric layer 8 (*see* Ex.1012, FIG. 3 (below) (shaded aqua)) between the substrate and Matsumoto's high-k dielectric (*see* Ex.1009, FIGS. 1 (below left), 22 (below right) (shaded red)) in Matsumoto's first embodiment semiconductor device (Figure 1) and fourth embodiment semiconductor device (Figure 22).



210. Wang teaches that the underlying dielectric 8 is “preferably formed of silicon oxide” and “has a first, nitride portion 10 that is in contact with high-k dielectric layer 6 and a second non-nitrided, or substantially nitrogen-free, portion 12 that is in contact with the underlying substrate 2.” Ex.1012, ¶48.

211. In my opinion, a POSITA would have understood that Wang's underlying dielectric 8 is used as a "buffer insulating film," as required by claim 7, at least because Wang's Background of the Invention explains that Wang's disclosure provides an improved and optimal buffer between "undesirable interactions between high-k dielectrics and the underlying semiconductor material." Ex.1012, ¶3; *see also* Ex.1012, ¶¶4-6. Therefore, it is my opinion that Matsumoto combined with Wang discloses the claimed buffer insulating film between the substrate and the high dielectric constant gate insulating film of claim 5 of the '764 patent.

212. It is my further opinion that a POSITA would have understood that the underlying dielectric 8 (i.e., the claimed buffer insulating film) is a silicon oxide film (e.g., in non-nitrided portion 12), as required by claim 3. *See* Ex.1338, 88-89 describing use of "nitrided oxides" including SiO_xNy. Alternatively, in my opinion, a POSITA would have understood either the nitrided portion 10 or the non-nitrided portion 12 to be the claimed "buffer insulating film," as it serves the same purpose of preventing "undesirable interactions between high-k dielectrics and the underlying semiconductor material." Ex.1012, ¶3. Therefore, it is my opinion that Matsumoto combined with Wang discloses the claimed buffer insulating film is a silicon oxide film, as required by claim 3 of the '764 patent.

213. In my opinion, a POSITA would have been motivated to combine Matsumoto and Wang in the manner explained above. Wang explains that it was well known in the art that to use silicon oxide as a buffer layer between the high-k gate dielectric and the substrate. According to Wang, “[d]ue to the undesirable interactions between high-k dielectrics and the underlying semiconductor material (usually silicon, germanium, silicon germanium, and the like) to degrade carrier mobility, a thin silicon oxide layer is typically employed as part of the gate dielectric even when a high-k gate dielectric is employed.” Ex.-1012, ¶3. Wang’s explanation corresponds with the description of the buffer insulating film in the ’764 patent, which states that, by using a buffer insulating film, “deterioration of an interface between a substrate and a gate insulating film can be suppressed.” Ex.1001, 12:15-17.

214. A POSITA would have been further motivated to combine Matsumoto and Wang in my opinion, because Wang’s teachings can be integrated with Matsumoto’s devices to further Matsumoto’s goal of providing “a semiconductor device which achieves reductions in malfunctions and operating characteristic variations.” Ex.1009, ¶13. Wang explains that “underlying dielectric layer 8 advantageously provides higher mobility and higher reliability for the high-k peripheral (or I/O) device.” Ex.1012, ¶28. In my opinion, a POSITA would have been motivated to use Wang’s buffer insulating layer to improve carrier mobility,

and, thus, performance and reliability, of semiconductor devices such as the MOSFETs disclosed by both Wang and Matsumoto.

215. In my opinion, combining Wang's buffer layer with Matsumoto's high-k film in the manner described above would have been a straightforward use of a known technique (i.e., forming Wang's buffer insulating layer) to improve similar devices (i.e., Matsumoto's transistor using a high-k gate insulating film) in the same way (i.e., improving carrier mobility in high-k transistor designs).

216. Wang discloses the use of well-known and established methods for forming the underlying dielectric, including that it can be "a thermally grown oxide formed by subjecting substrate 2 to an oxygen ambient." Ex.1012, ¶22. Wang also teaches that deposition of the high-k dielectric layers "may be performed by conventional methods including remote plasma CVD (RPCVD), plasma enhanced CVD (PECVD), atomic layer deposition (ALD), MOCVD, MBE, PVD, sputtering or other methods known in the art." Ex.1012, ¶24. Matsumoto similarly discloses the use of well-known and existing techniques for forming the gate dielectric, including using CVD for dielectric film deposition. Ex.1009, ¶107.

217. Even further, Matsumoto discloses forming a layer of silicon oxide above the substrate, with other high-k dielectrics as alternative gate insulating films. Ex.1009, ¶107. In my opinion, a POSITA wanting to include a buffer layer between the substrate and the high-k gate dielectric, which Wang asserts was "typical" in the

art, would have simply applied Matsumoto's (or Wang's) disclosure of forming a silicon oxide layer along with (and before) Matsumoto's (or Wang's) disclosure regarding using other high-k materials for the gate dielectric. Wang's teachings for nitriding part of the underlying gate dielectric would then be applied, followed by Matsumoto's remaining steps of forming the insulating sidewalls.

218. In view of these teachings of Matsumoto and Wang, in my opinion, a POSITA would have had a reasonable expectation of success in combining Matsumoto and Wang in the manner discussed above, and the results of the combination would have been predictable to a POSITA. Therefore, it is my opinion that Matsumoto combined with Wang discloses claims 2 and 3 of the '764 patent.

2. Dependent Claim 6: "The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a Hf based oxide."

219. Matsumoto discloses exemplary high-k dielectrics for use in its semiconductor device and Wang explains that the Matsumoto's high-k film can be formed of a Hf based oxide, such as HfO_2 , or a nitrated Hf-based oxide, such as HfSiON , as the gate dielectric in the combined Matsumoto-Wang semiconductor device that renders claim 6 obvious.

220. Matsumoto teaches that high-k materials such as "a metal oxide film such as Al_2O_3 or a ferroelectric film such as Ta_2O_5 and BST" can be used as a gate insulating film. Ex.1009, ¶107. Wang teaches the use of similar high-k dielectrics,

including “HfSiON, amorphous HfSiON, Ta₂O₅, TiO₂, Al₂O₃, ZrO₂, HfO₂, Y₂O₂, La₂O₂, aluminates, silicates, HfAlO_x, TiO₂, PbTiO₂, BaTiO₂, SrTiO₂, and PbZrO₂, and combinations thereof.” Ex.1012, ¶12; *see also id.*, ¶¶ 9, 25. Matsumoto and Wang both explicitly list Al₂O₃ and Ta₂O₅ as exemplary high-k gate dielectrics, and Wang’s disclosure of HfO₂, for example, is consistent with Matsumoto’s disclosure of “a metal oxide film such as....” *See* Ex.1009, ¶107. Therefore, it is my opinion that Matsumoto combined with Wang discloses that the high dielectric constant gate insulating film is formed of a Hf-based oxide, as required by claim 6 of the ’764 patent.

221. In my opinion, a POSITA would have been motivated to use a Hf-based oxide as a high-k gate insulating film, as taught by Wang, in the semiconductor devices of Matsumoto’s first and/or fourth embodiments. By 2005, a POSITA would have been motivated to select HfO₂ as a high-k gate insulating film, as Hf-based dielectrics (e.g., HfO₂) had already become a popular high-k dielectric in advanced semiconductor manufacturing due to the many known benefits including superior thermal stability and band gap alignment. *See e.g.*, Ex.1337, 2.4.1 (“Recently, HfO₂ films have emerged as the most promising gate dielectric material for sub 100nm technology due to its superior thermal stability with poly-Si and reasonable band alignment”); Ex.1213, 207 (HfO₂ “combines a high k (15–26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ...”);

Ex.1349, 134 (“Excellent dielectric properties such as high dielectric constant, low leakage current, good thermal stability, negligible dispersion and excellent reliability were demonstrated. These results suggest that HfO_2 is a promising material for the future gate dielectric application.”). Additionally, HfO_2 also could be scaled down to a smaller EOT. Ex.1213, 207.

222. While HfO_2 is a Hf based oxide, a POSITA would have considered other materials disclosed by Wang, including HfSiON (hafnium-silicon oxynitride), to be hafnium-based oxide because they contain hafnium oxide as a key component. For example, HfSiON is an evolution of HfSiO with the addition of nitrogen. Even though HfSiON contains silicon and nitrogen, a POSITA would have understood HfSiON to be a hafnium-based oxide because the core dielectric properties stem from the presence of hafnium oxide.

223. Thus, it is my further opinion that a POSITA would have been motivated to use HfSiON to form the high dielectric constant gate insulating film to further enhance operation because nitrogen incorporation was found to improve thermal stability and electrical characteristics of HfSiON , including by enhancing the dielectric constant of the film. Ex.1329, 849.

3. Dependent Claim 11: “The semiconductor device of claim 1, wherein each side end portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less.”

224. Wang discloses that the high-k dielectric layer 6 “is preferably less than about 50 Å to maintain low gate leakage and thin equivalent oxide thickness (EOT).” Ex.1012, ¶26. For an exemplary HfSiON gate insulating layer, the film “was deposited to a thickness of about 5 to 50 Angstroms and having an equivalent oxide thickness (EOT) of less than about 2.0 nanometers.” *Id.*, ¶34. Wang also specifically claims a device “wherein the high-k dielectric has a thickness from about 5 to 50 Å.” *Id.*, claim 3.

225. In my opinion, a POSITA would have been motivated to use thinner gate insulating films, as taught by Wang, consistent with the goals of miniaturizing semiconductor devices.

226. In the combined device of Matsumoto and Wang, the thickness of the high-k gate insulating film at its side ends would also range from about less than 5 Angstroms to less than 50 Angstroms since the thickness of the layer is smaller under sidewall 8 than under the gate electrode 7. The range of 5 to 50 Angstroms is equivalent to 0.5 to 5 nm, and, therefore, Wang’s preferred range includes thicknesses less than 2 nm, as recited by claim 11. In other words, the thickness of 2 nm (i.e., 20 Angstroms) recited by claim 11 falls within the range of thicknesses

disclosed by Wang for the side end portion of its high dielectric constant gate insulating film.

227. I have been informed, and understand, that where a claimed range overlaps with a range disclosed in the prior art, there is a presumption of obviousness, and it becomes the patentee's burden to present evidence of teaching away, unexpected results or criticality, or other pertinent objective indicia indicating that the overlapping range would not have been obvious in light of that prior art. Based on my review of the intrinsic record, there is no discussion, evidence, or justification for the selection of 2 nm as the thickness of the gate insulating film.

228. For the foregoing reasons, it is my opinion that the combination of Matsumoto and Wang renders obvious claim 11 of the '764 patent.

C. Ground III

230. In my opinion, Matsumoto in combination with Wang renders obvious Challenged Claim 11 of the '764 patent (see Ground II). To the extent the combination of Matsumoto and Wang does is found not to disclose the additional limitations of claim 11, Sim teaches the limitations of that claim, as explained below. In my opinion, a POSITA would have been motivated to combine Matsumoto, Wang, and Sim, thereby rendering obvious claim 11.

1. Dependent Claim 11: “The semiconductor device of claim 1, wherein each side end portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less.”

231. Sim’s study related to the use of high-k dielectrics used in semiconductor devices. Ex.1024, Abstract (“Scaling the physical thickness of the HfO₂ dielectric causes less charge trapping and higher mobility.”). Sim is therefore in the same field as Matsumoto, Wang, and the ’764 patent. Ex.1001, 1:15-16 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); Ex.1009, ¶2 (“The present invention relates to a semiconductor device and a method of manufacturing the same.”); Ex.1012, ¶2.

232. Sim describes use of a gate insulating film having a thickness of 2nm or less. Specifically, Sim explains that “[h]afnium-based high-k dielectrics and metal gate electrodes have been aggressively investigated to ensure continued scaling of CMOS technology, but several drawbacks such as low mobility and charge trapping have been identified.” Ex.1024, 218. Sim’s authors addressed these drawbacks by testing films of different thickness and “systematically evaluat[ing] the effects of high-k film thickness on charge trapping and channel carrier mobility.” *Id.* As a result, Sim found that “scaling the high-k dielectric is a simple, but very effective means of improving mobility and other reliability characteristics.” *Id.*

233. In particular, Sim concluded that “[s]caling the physical thickness of the HfO₂ dielectric to below 20Å causes less charge trapping and higher mobility.”

Ex.1024, 221. 20Å is equal to 2 nm, which is the thickness recited by claim 11. The thickness of the high-k film is even smaller under sidewall 8 (i.e., the side portion) than under the gate electrode 7 and would therefore be less than 2 nm according to Sim's teachings. Thus, the semiconductor devices resulting from the combination of Matsumoto's first and/or fourth embodiments with Wang and Sim provides that each side portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less.

234. Wang discloses use of HfO₂ as an example of a high-k gate dielectric (Ex.1012, ¶12), the same film studied in Sim. Wang also discloses a preferred thickness (i.e., "5 to 50 Angstroms") that includes the ideal range disclosed by Sim (i.e., "below 20Å"). Ex.1012, ¶34; Ex.1024, 221. In my opinion, a POSITA would have been motivated to apply Sim's findings regarding ideal thicknesses of a HfO₂ gate insulating film (namely, a thickness of 20Å (2 nm) or less) to the combined devices of Matsumoto's first and/or fourth embodiments and Wang.

235. Sim explains why such a combination would have been desired. According to Sim, reducing the thickness of HfO₂ to below 20Å enhances mobility and reduces charge trapping, key issues in ensuring the performance and scalability of semiconductor devices. Ex.1024, 221. Sim's teachings are consistent with Wang's goal of using a thickness of "preferably less than about 50 Å to maintain low gate leakage and thin equivalent oxide thickness (EOT)." Ex.1012, ¶26.

236. The Matsumoto-Wang-Sim combination would have been nothing more than the use of a known technique (i.e., Sim's HfO₂ dielectric layer with less than 20Å thickness) to improve similar devices (i.e., the Matsumoto-Wang semiconductor device having a high-k dielectric layer that is 5 to 50Å thick), in the same way. In my opinion, a POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable because Sim uses a well-known process, atomic layer deposition (ALD), for fabricating high-k films. Ex.1024, 218.

237. Therefore, it is my opinion that the combination of Matsumoto, Wang, and Sim renders obvious claim 11 of the '764 patent.

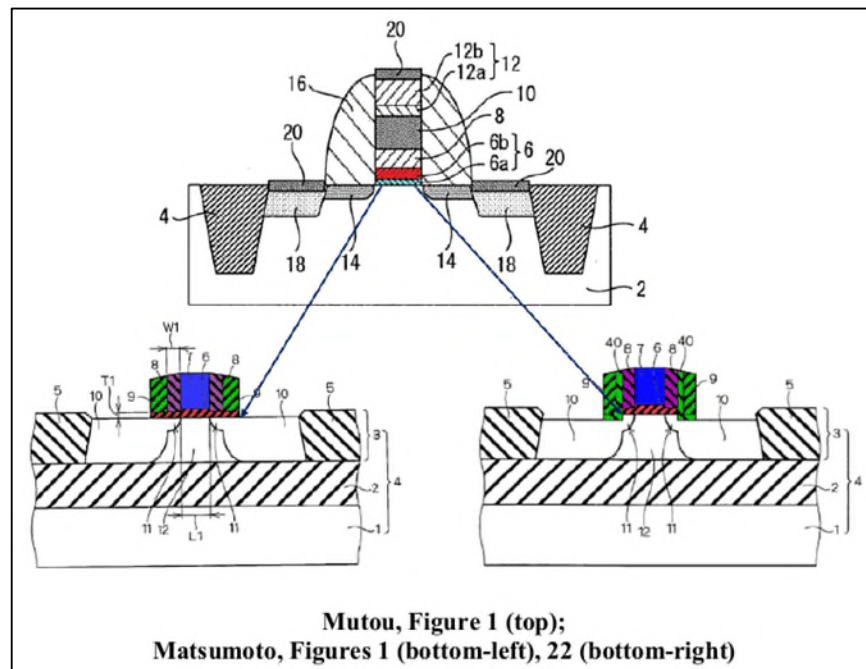
D. Ground IV

238. As discussed above with regard to Ground I, Matsumoto discloses, or at least renders obvious, every limitation of claim 1. To the extent Matsumoto is found not to disclose the additional limitations of claims 2-3, Mutou teaches the limitations of those claims, as explained below. In my opinion, a POSITA would have been motivated to combine Matsumoto and Mutou, thereby rendering claims 2-3 obvious.

1. **Dependent Claim 2: “The semiconductor device of claim 1, further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film.”**

Dependent Claim 3: “The semiconductor device of claim 2, wherein the buffer insulating film is a silicon oxide film.”

239. In my opinion, a POSITA would have been motivated to combine Mutou’s teachings regarding use of a buffer layer between a high-k dielectric and silicon substrate to Matsumoto’s first and/or fourth embodiment semiconductor devices. The resulting semiconductor device would have included Mutou’s underlying interfacial layer 6a (*see* Ex.1019, FIG. 1 (below, top) (shaded aqua)) located between the substrate 2 and high-k gate dielectric 6b (*see id.*, FIGS. 1 (below, top) (shaded red)) in Mutou, and placed that underlying interfacial layer between the substrate and high-k dielectric (*see* Ex.1009, FIGS. 1 (below, bottom-left), 22 (below, bottom-right) (shaded red)) of Matsumoto’s first embodiment (Figure 1) and fourth embodiment (Figure 22) devices. The combined Matsumoto-Mutou semiconductor device would include Matsumoto’s transistor with Mutou’s underlying interfacial layer situated between Matsumoto’s substrate and high-k gate insulating film 6, as illustrated below.



240. Mutou teaches that, “[o]n the substrate 2 in the element regions, a gate dielectric film 6 is formed.” Ex.1019, ¶41. Gate dielectric film 6 includes “an underlying interfacial layer 6a formed on the silicon substrate 2; and high-k dielectric film 6b formed on the underlying interfacial layer 6a and having higher dielectric constant than the underlying interfacial layer 6a.” Ex.1019, ¶41. Mutou also explains that the underlying interfacial layer 6a may be, “for example, a SiO₂ film, a Si₃N₄ film, or a SiON film (hereafter collectively referred to as ‘SiO₂ film of the like’),” and acts to “inhibit interfacial reaction between the silicon substrate 2 and the high-k dielectric film 6b.” Ex.1019, ¶42.

241. In my opinion, A POSITA would have understood from this disclosure that Mutou’s interfacial layer 6a serves as a buffer layer between Mutou’s substrate

and Mutou's high-k gate insulating film, as required by claim 2, and that Mutou's interfacial layer 6a is formed of silicon oxide, as required by claim 3. Thus, in my opinion, the combination of Matsumoto's first and/or fourth embodiments with Mutou's underlying interfacial layer 6a discloses claims 2 and 3.

242. It is my further opinion that a POSITA would have been motivated to combine Mutou and Matsumoto in the manner explained above. Mutou expressly motivates the combination by teaching that "[t]he underlying interfacial layer 6a is acted to inhibit interfacial reaction between the silicon substrate 2 and the high-k dielectric film 6b." Ex.1019, ¶42. Inhibiting such reactions between the substrate and the high-k film decreases degradation of the high-k film and, thus, improves performance of the device. *See* Ex.1001, 12:9-15 (by using a buffer insulating film, "deterioration of an interface between a substrate and a gate insulating film can be suppressed"). This use of a buffer layer is also what Wang described as "typical" before the alleged invention of the '764 patent, as discussed in Ground II above. Mutou's interfacial layer furthers Matsumoto's goal "to provide a semiconductor device[,] which achieves reductions in malfunctions and operating characteristic variations." Ex.1009, ¶13.

243. Based on these teachings of Mutou and Matsumoto, in my opinion, a POSITA would have been motivated to use Mutou's underlying interfacial layer to

inhibit interfacial reaction between the substrate and the high-k film and improve performance of Matsumoto's first and/or fourth embodiment semiconductor devices.

244. In my opinion, combining Mutou with Matsumoto's first and/or fourth embodiments would have required nothing more than the use of a known technique (i.e., Mutou's underlying interfacial layer) to improve similar devices (i.e., Matsumoto's transistor using a high-k gate insulating film) in the same way (i.e., forming an underlying interfacial layer prior to forming the high-k dielectric film). Additionally, in my opinion, combining Mutou with Matsumoto's first and/or fourth embodiments would have merely been the application of a known technique (i.e., Mutou's underlying interfacial layer) to a known device (i.e., Matsumoto's transistor using a high-k gate insulating film) ready for improvement.

245. More specifically, Mutou discloses the use of well-known processes to form its underlying interfacial layer: "Next, ... a SiO₂ film or the like ... is formed as an underlying interfacial layer 6a on the silicon substrate 2 using a method such as thermal oxidation (or thermal nitriding or thermal oxynitriding) or plasma oxidation (or plasma nitriding or plasma oxynitriding)." Ex.1019, ¶53. Mutou also discloses that deposition of the high-k dielectric film may be done "using an ALD (atomic layer deposition) method or an MOCVD (metal organic chemical vapor deposition) method." *Id.*, ¶54. Matsumoto similarly discloses the high-k gate insulating film is deposited using a CVD process. Ex.1009, ¶107.

246. Even further, in my opinion, a POSITA seeking to utilize an underlying interfacial layer underlying the high-k dielectric would have utilized the teachings of Mutou and Matsumoto in the order taught by those references. Matsumoto already discloses forming a layer of silicon oxide above the substrate, with other high-k dielectrics as alternative gate insulating films. Ex.1009, ¶107. A POSITA wanting to include a buffer layer of silicon oxide between the substrate and the high-k gate dielectric (e.g., as disclosed by Mutou) would have simply applied Matsumoto's (or Mutou's) disclosure of forming a silicon oxide layer along with (and before) Matsumoto's (or Mutou's) disclosure regarding using other high-k materials for the gate dielectric. Matsumoto's remaining steps of forming the gate electrode and insulating sidewalls could then be performed.

247. In view of these teachings of Matsumoto and Mutou, in my opinion, a POSITA would have had a reasonable expectation of success in combining Matsumoto and Mutou in the manner discussed above, and the results of the combination would have been predictable to a POSITA. Therefore, it is my opinion that Matsumoto combined with Mutou discloses claims 2 and 3 of the '764 patent.

E. Ground V

248. In my opinion, Matsumoto in combination with Ono renders obvious Challenged Claims 6, 12, and 13 of the '764 patent (Ground V). As discussed above with regard to Ground I, Matsumoto discloses, or at least renders obvious, every

limitation of claim 1 of the '764 patent. To the extent Matsumoto is found not to disclose the additional limitations of claims 6, 12, and 13, Ono teaches the limitations of those claims, as explained below. In my opinion, a POSITA would have been motivated to combine Matsumoto and Ono, thereby rendering obvious claims 6, 12, and 13.

1. Dependent Claim 6: “The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a Hf based oxide.”

249. Matsumoto discloses exemplary high-k dielectrics for use in its semiconductor device and Ono teaches that its gate insulator film 5 is made of a “HfO₂ film,” which is a HF based oxide, as required by claim 6 of the '764 patent. Ex.1013, ¶209. In my opinion, a POSITA would have combined Matsumoto and Ono by utilizing Ono’s Hf-based oxide (i.e., HfO₂) as the gate dielectric in the combined Matsumoto-Ono semiconductor device that renders claim 6 obvious.

250. In particular, it is my opinion that a POSITA would have been motivated to use a Hf-based oxide as a gate insulating layer, as taught by Ono, in Matsumoto’s first and/or four embodiment semiconductor devices because HfO₂ was already commonly used in the industry due to its many known benefits, including superior thermal stability and band gap alignment. Ex.1337, 2.4.1 (“Recently, HfO₂ films have emerged as the most promising gate dielectric material for sub 100nm technology due to its superior thermal stability with poly-Si and

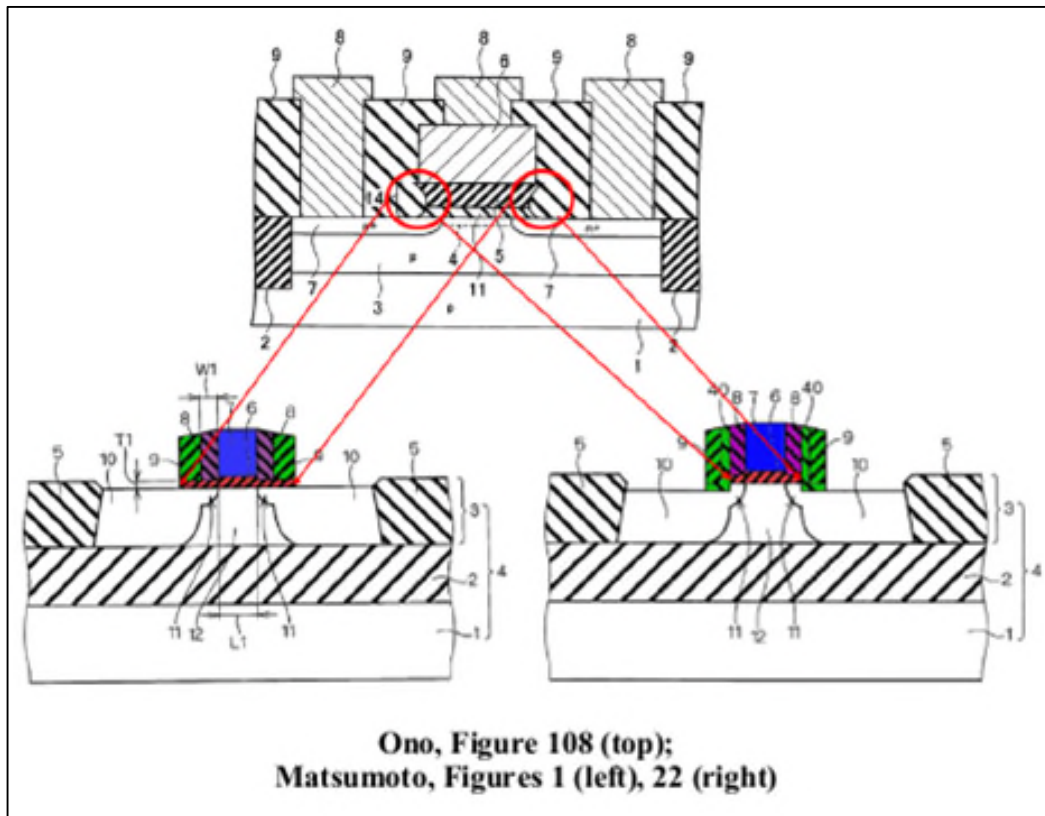
reasonable band alignment"); Ex.1213, 207 (HfO₂ "combines a high k (15–26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ..."); Ex.1349, 134 ("Excellent dielectric properties such as high dielectric constant, low leakage current, good thermal stability, negligible dispersion and excellent reliability were demonstrated. These results suggest that HfO₂ is a promising material for the future gate dielectric application."). Additionally, HfO₂ also could be scaled down to a smaller EOT. Ex.1213, 207.

251. In view of these teachings of Matsumoto and Ono, in my opinion, a POSITA would have been motivated to choose Ono's hafnium-based oxide (i.e., HfO₂) as the high-k gate insulating film 6 in Matsumoto's first and/or fourth embodiments. Therefore, it is my opinion that Matsumoto combined with Ono discloses claim 6 of the '764 patent.

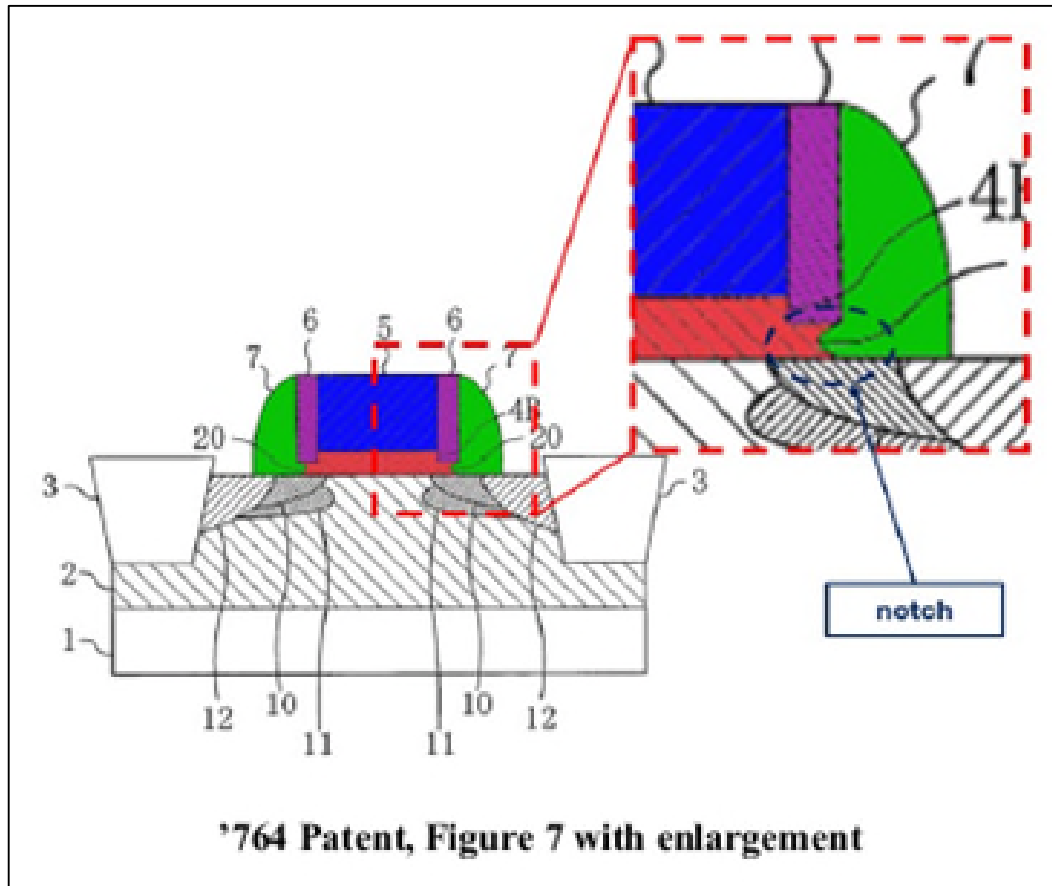
2. **Dependent Claim 12:** “The semiconductor device of claim 1, wherein a side surface of the high dielectric constant gate insulating film is located at a predetermined distance from a side end surface of the first insulating sidewall toward the gate electrode.”

Dependent Claim 13: “The semiconductor device of claim 1, wherein a side surface of the high dielectric constant gate insulating film is located at a predetermined distance from a side end surface of the gate electrode toward the first insulating sidewall.”

252. In the devices of the Matsumoto-Ono combination, the end portion of Matsumoto’s gate insulating film has a semicircular shape under the sidewall, as taught by Ono in, e.g., Figure 108 (below, top).



253. Consistent with the '764 patent's disclosure, the semicircular shape of the gate insulating film's side end in the combination discloses a notch. *See, e.g.*, Ex.1001, 8:35-40 (referring to notch 20 of FIG. 7), FIG. 7 (below) (depicting notch 20 having a semicircular shape).

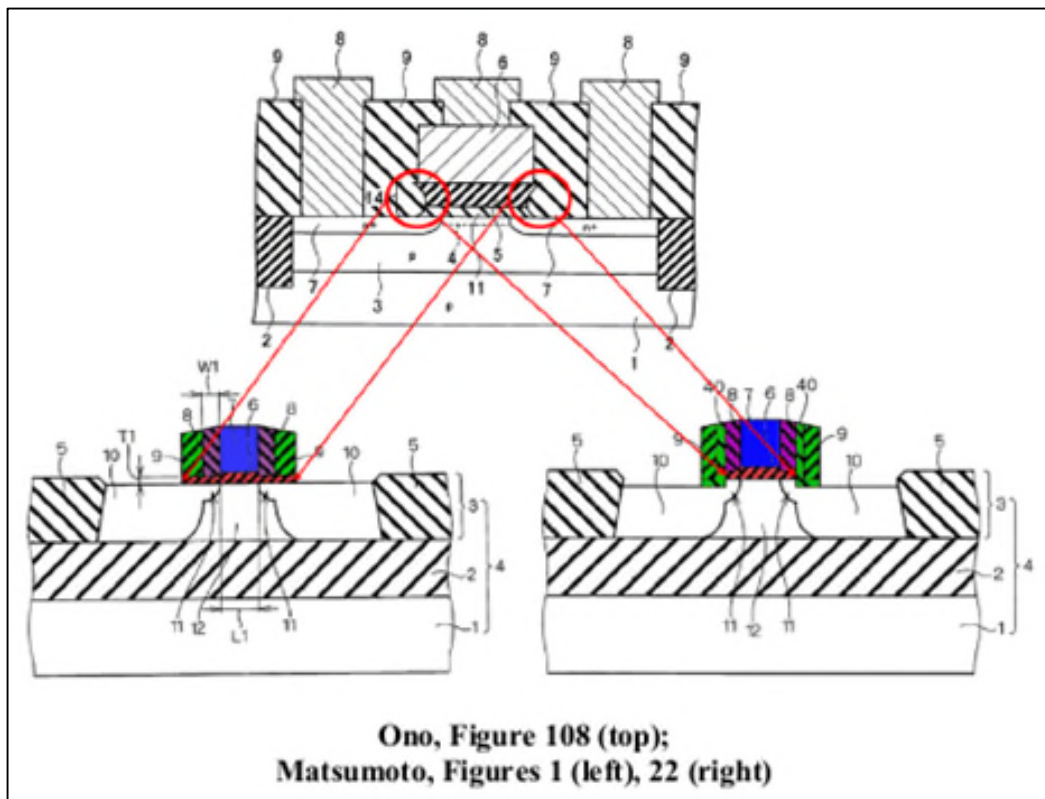


254. Additionally, in the combination of Matsumoto's fourth embodiment (Figure 22) and Ono, when the semicircular notch is applied at each side end of Matsumoto's gate insulating film 6 located under the first insulating sidewall film 8, the end of the gate insulating film no longer extends completely under the first insulating sidewall. The notch's semicircular shape (as taught by Ono) and the

distance which the semicircular shape extends inward toward the gate electrode are set by specific process parameters.

255. Accordingly, in the combination of Matsumoto's fourth embodiment and Ono, the gate insulating film's side surface is located at a predetermined distance from a side end surface of the first insulating sidewall toward the gate electrode and from a side end surface of the gate electrode toward the first insulating sidewall, consistent with the '764 patent's disclosure. Ex.1001, 21:26-30 ("side surface ... may be located at a predetermined distance from a side end surface of the sidewall 7 or the offset sidewall 6 toward the gate electrode 5").

256. In my opinion, a POSITA would have been motivated to apply Ono's teaching of curving the end portion of a gate insulating film to Matsumoto's first and/or fourth embodiment devices, as shown below. In the combination, the side ends of Matsumoto's gate insulating film have a semicircular shape, as taught by Ono.



257. Ono expressly suggests the combination, teaching that using curved side surfaces for the gate insulating film “reduc[es] the scattering of carriers as well as enhanc[es] the controllability of the gate electrode with respect to the potential of the channel region” and therefore provides “an advantage of optimization.” Ex.1013, ¶216, ¶200 (noting, for the first embodiment, by using curved side surfaces, “the electrical capacitance between the gate electrode 6 and the source/drain regions 7 may be adjusted,” resulting in “an advantage of optimization”). In my opinion, a POSITA would have been further motivated to curve the end of Matsumoto’s gate insulating film to optimize parasitic resistance and parasitic capacitance, improving device performance. Ex.1340, ¶108; §IV.B.2.

258. It is my opinion that the Matsumoto-Ono combination is merely the application of a known technique (Ono's curved film ends) to improve similar devices in the same way for the above reasons. A POSITA would have had a reasonable expectation of success in the combination in my opinion and the results of the combination would have been predictable. Matsumoto and Ono both use high-k gate insulating films that extend under the gate electrode and the insulating sidewall, a concept well-known before the '764 patent. Both Matsumoto and Ono also form their high-k dielectrics using conventional techniques. Ex.1009, ¶114; Ex.1013, ¶167.

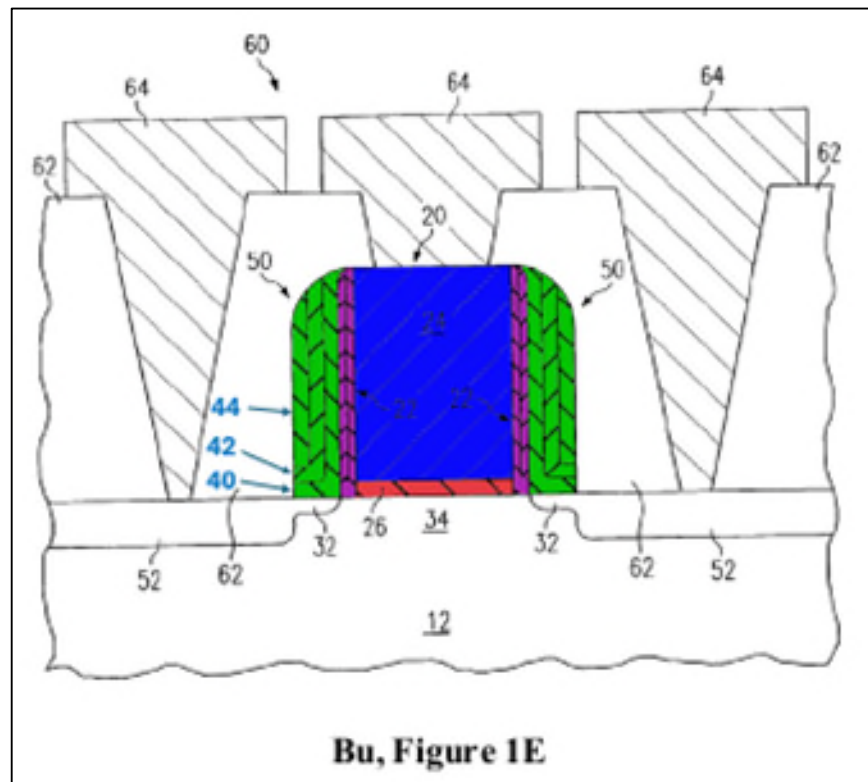
259. Therefore, it is my opinion that Matsumoto combined with Ono discloses claims 12 and 13 of the '764 patent.

F. Ground VI

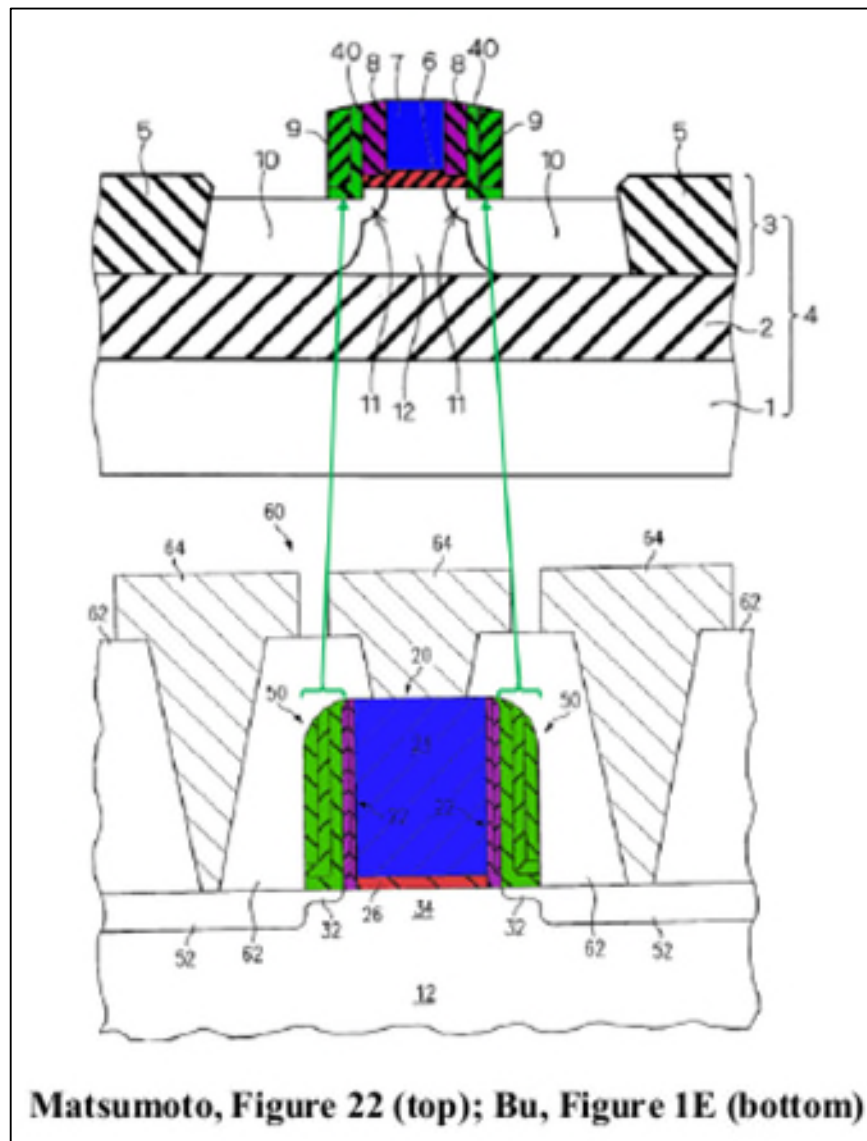
260. In my opinion, Matsumoto in combination with Bu renders obvious Challenged Claim 15 of the '764 patent (Ground VI). As discussed above with regard to Ground I, Matsumoto discloses, or at least renders obvious, every limitation of claims 1 and 15 of the '764 patent. To the extent Matsumoto is found not to disclose the limitations of claim 15, Bu teaches the limitations of that claim, as explained below. In my opinion, a POSITA would have been motivated to combine Matsumoto and Bu, thereby rendering obvious claim 15.

1. **Dependent Claim 15: “The semiconductor device of claim 1, wherein the second insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film.”**

261. Bu’s transistor includes gate stack 20, comprising gate conductor 24 (*see* Ex.1025, FIG. 1E (below) (shaded blue)) and gate insulator 26 (*see id.* (shaded red)), and sidewall spacers 22 (*see id.* (shaded purple)). Ex.1025, ¶42. Bu’s transistor further includes an outer sidewall formed on sidewall spacers 22 having a triple-layer ONO structure: first sidewall-forming layer 40, comprised of “oxide”; second sidewall-forming layer 42, comprised of “nitride”; and third sidewall-forming layer 44, comprised of “oxide”. Ex.1025, ¶¶26-27, 30, 35, 43, FIG. 1E. Bu and Matsumoto are in the same field as the ’764 patent. Ex.1001, 1:15-16; Ex.1009, ¶2; Ex.1025, Abstract.



262. Matsumoto's fourth embodiment includes inner "first sidewall" 8 and an outer "second sidewall" comprised of oxide film 40 and nitride film 9. Ex.1009, ¶¶110, 139, FIG. 22. In my opinion, a POSITA would have been motivated to use Bu's triple-layer ONO sidewall structure with Matsumoto's fourth embodiment device. Specifically, a POSITA would have been motivated to add an additional oxide layer to Matsumoto's second sidewall (see Ex.1009, FIG. 22 (below top) (shaded green)), as taught by Bu (see Ex.1025, FIG. 1E (below, bottom)). The resulting Matsumoto-Bu device discloses that the second insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film.



263. In my opinion, a POSITA would have specifically integrated Bu’s triple-layer ONO sidewall structure teachings into Matsumoto’s fourth embodiment device given the well-known benefits of ONO structures, including, for example, allowing independent control of spacer dimensions to optimize device scaling. Ex.1350, ¶¶5-6, FIG. 4. Bu further notes the benefits of using different materials in the sidewall structure: “film properties of sidewall-forming layers 40 and 42 may

minimize dopant loss from source drain extension region 32 to first sidewall-forming layer 40. Accordingly, parasitic resistance may be lowered.” Ex.1025, ¶26. Thus, a POSITA would have been motivated to make the combination to obtain these benefits and improve device performance and reliability in my opinion.

264. The Matsumoto-Bu combination semiconductor device represents nothing more than use of a known technique (Bu’s triple-layer sidewall) to improve similar devices in the same manner for the above reasons. In my opinion, a POSITA would have had a reasonable expectation of success in the combining these references, leading to predictable results, because both Matsumoto and Bu disclose forming sidewall layers using standard deposition and etching techniques, making the application of Bu’s triple layer structure to Matsumoto’s design straightforward. Ex.1009, ¶¶139, 162, Figure 29; Ex.1025, ¶¶27, 30, 35, 38.

265. Therefore, it is my opinion that Matsumoto combined with Bu discloses claim 15 of the ’764 patent.

G. Ground VII

266. In my opinion, Matsumoto in combination with Wilk renders obvious Challenged Claims 18 and 19 of the ’764 patent (Ground VII). As discussed above with regard to Ground I, Matsumoto discloses, or at least renders obvious, every limitation of claims 1, 18, and 19 of the ’764 patent. To the extent Matsumoto is found not to disclose the limitations of claims 18 and 19, Wilk teaches the limitations

of those claims, as explained below. In my opinion, a POSITA would have been motivated to combine Matsumoto and Wilk, thereby rendering obvious claims 18 and 19.

1. **Dependent Claim 18: “The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more.”**

Dependent Claim 19: “The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall.”

267. Wilk explores the properties of materials “under consideration” in 2001 “as potential replacements for SiO₂ as the gate dielectric material for sub-0.1 μ m CMOS technology.” Ex.1018, Abstract. Wilk discloses the following table of relevant properties, including dielectric constants, for various materials:

TABLE I. Comparison of relevant properties for high- κ candidates.				
Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si	Crystal structure(s)
SiO ₂	3.9	8.9	3.2	Amorphous
Si ₃ N ₄	7	5.1	2	Amorphous
Al ₂ O ₃	9	8.7	2.8 ^a	Amorphous
Y ₂ O ₃	15	5.6	2.3 ^a	Cubic
La ₂ O ₃	30	4.3	2.3 ^a	Hexagonal, cubic
Ta ₂ O ₅	26	4.5	1–1.5	Orthorhombic
TiO ₂	80	3.5	1.2	Tetrag. ^c (rutile, anatase)
HfO ₂	25	5.7	1.5 ^a	Mono. ^b , tetrag. ^c , cubic
ZrO ₂	25	7.8	1.4 ^a	Mono. ^b , tetrag. ^c , cubic

^aCalculated by Robertson (See Ref. 153).
^bMono.=monoclinic.
^cTetrag.=tetragonal.

Wilk, Table I

Id., Table 1.

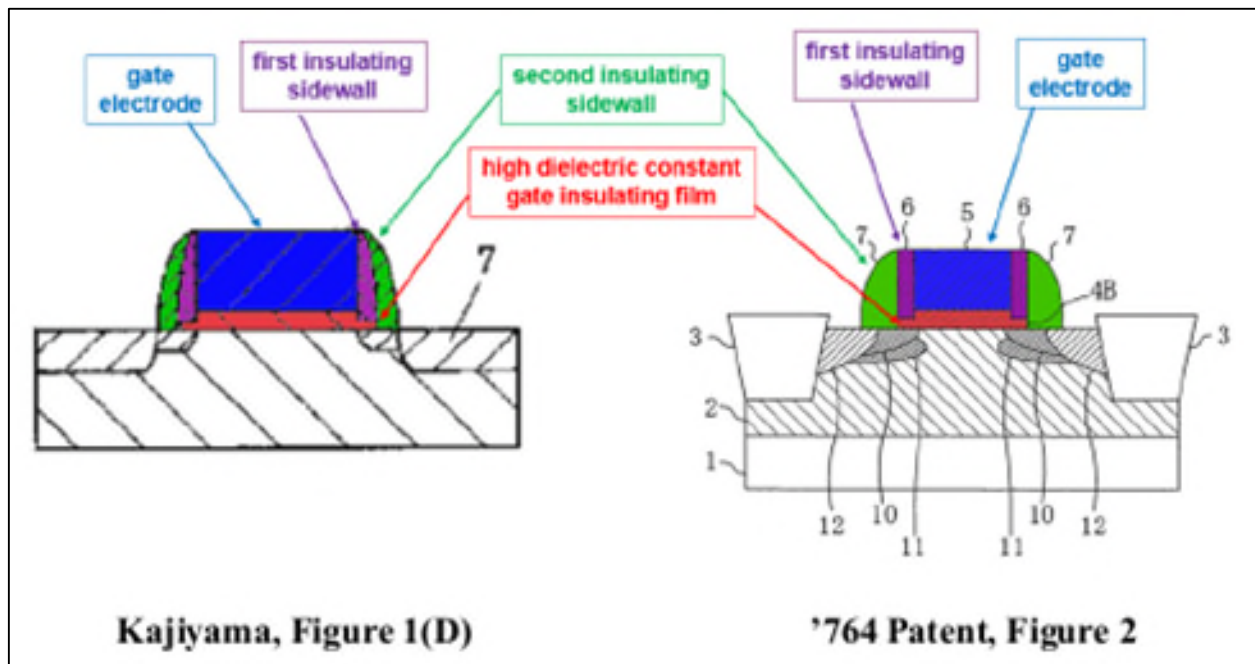
268. In my opinion, a POSITA would have been motivated to look to Wilk's teachings to understand the properties of materials discussed in Matsumoto. Wilk and Matsumoto are in the same field as the '764 patent. Ex.1001, 1:15-16; Ex.1009, ¶2; Ex.1018, Abstract. Wilk is specifically directed to high-k materials for gate dielectric applications and lists relevant properties of materials discussed in Matsumoto, allowing a POSITA to, for example, ensure that Matsumoto's gate insulating film had a sufficiently high dielectric constant.

269. Matsumoto teaches use of "Ta₂O₅" as the gate insulating film. Ex.1009, ¶107. Wilk discloses the dielectric constant for Ta₂O₅ is 26, which is greater than 10. Ex.1018, Table I. Matsumoto discloses second sidewall 9 (i.e., the claimed "second insulating sidewall") is comprised of silicon nitride (Si₃N₄), which has a dielectric constant of 7. Ex.1009, ¶¶114, 139; Ex.1018, Table I; Ex.1352, Fig. 4.

270. Thus, in the Matsumoto-Wilk combination device, the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more and the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall. Therefore, it is my opinion that Matsumoto combined with Wilk discloses claims 18 and 19 of the '764 patent.

H. Ground VIII

271. The semiconductor device of Kajiyama's first embodiment is represented below proximate an exemplary semiconductor device disclosed by the '764 patent to illustrate the similarity of those devices. See Ex.1011, FIG. 1(D) (below, left); Ex.1001, FIG. 2 (below, right).



272. In my opinion, at least Kajiyama's first embodiment anticipates Challenged Claims 1, 5, 16, and 17 of the '764 patent (Ground VIII), as explained in detail below.

1. Independent Claim 1

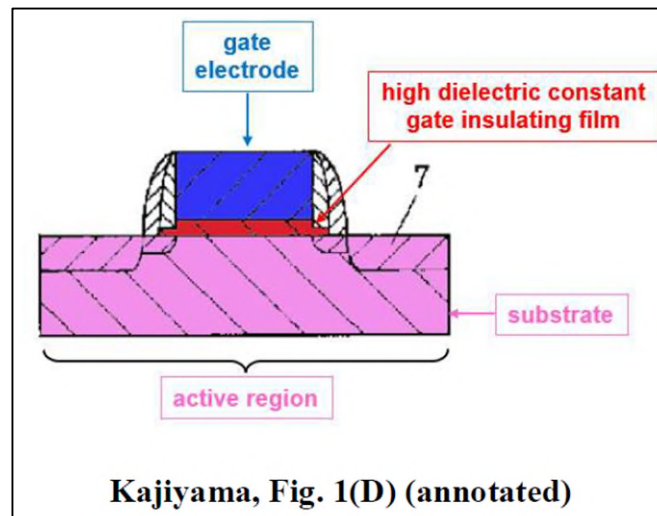
a. Preamble: “A semiconductor device comprising:”

273. Kajiyama’s first embodiment is a semiconductor device and Kajiyama discloses that “[t]he present invention relates to semiconductor devices.” Ex.1011, ¶1; *see also* Ex.1011, ¶27 (“Fig. 1 is a cross-sectional view illustrating a manufacturing process of a semiconductor device that functions as an n-type MOSFET according to a first embodiment of the present invention.”).

274. Therefore, it is my opinion that Kajiyama discloses the preamble of claim 1 of the ’764 patent.

b. Limitation 1[a]: “a high dielectric constant gate insulating film formed on an active region in a substrate”

275. Kajiyama discloses that its first embodiment semiconductor device has a “p-type Si substrate” (*see* Ex.1011, FIG. 1(D) (below) (shaded pink)) with an “element separation layer (not shown) on the Si substrate 1.” *Id.*, ¶¶28-29.



276. In my opinion, a POSITA would have understood Kajiyama's element separation layer active region to be equivalent to the '764 patent's shallow trench isolation (STI). Ex.1011, ¶¶5, 29; Ex.1001, 7:30-47 (describing active region with source/drain regions surrounded by STI structures 3). Within the active region defined by Kajiyama's element separation layer, an n-type LDD diffusion layer 4 is formed "on the surface of Si substrate 1" and, in a subsequent process step, an n⁺ source drain diffusion layer 7 is formed on the substrate. Ex.1011, ¶¶29, 32, FIGS. 1(A), 1(D). Thus, consistent with the disclosures of the '764 patent, Kajiyama's first embodiment device has an active region in a substrate.

277. In my opinion, Kajiyama's discloses that a high dielectric constant gate insulating film is formed on its active region in the substrate. Kajiyama discloses that "the semiconductor device of the present invention ... comprises a gate insulating film consisting of a high dielectric film formed on a semiconductor

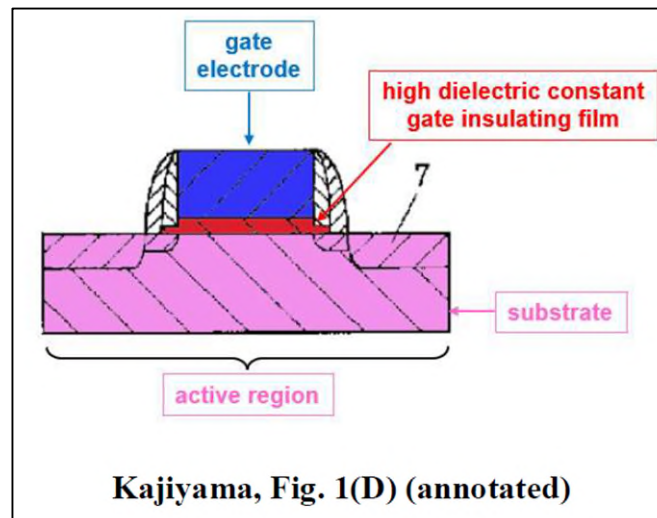
substrate.” Ex.1011, ¶14, FIG. 1(D); *see also* Ex.1011, ¶28. Kajiyama also refers to its high-k gate insulating film as ZrO₂ film 2. *Id.*, ¶29. ZrO₂ is a high-k dielectric. *See* Ex.1018, Table I (identifying ZrO₂ as having a dielectric constant of 25).

278. As shown above, the high-k gate insulating film (*see* Ex.1011, FIG. 1(D) (above) (shaded red)) disclosed by Kajiyama is formed on the substrate within the element separation layer and is therefore a high dielectric constant gate insulating film formed on an active region in a substrate. *Id.*, ¶29.

279. Therefore, it is my opinion that Kajiyama discloses this limitation of claim 1 of the '764 patent.

c. Limitation 1[b]: “a gate electrode formed on the high dielectric constant gate insulating film; and”

280. Kajiyama’s first embodiment device also includes a gate electrode formed on the high dielectric constant gate insulating film. For example, Kajiyama discloses that “the semiconductor device of the present invention ... comprises ... a gate electrode consisting of a conductive film formed on a gate insulating film.” Ex.1011, ¶14, FIG. 1(D). Gate electrode 3 (*see id.*, FIG. 1(D) (below) (shaded blue)) is shown below on the gate insulating film (*see id.* (shaded red)).

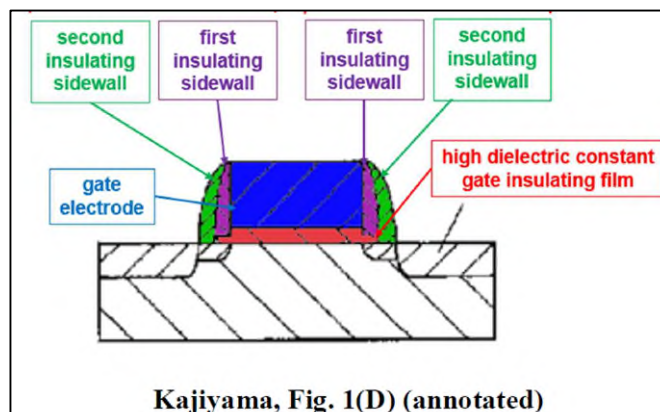


281. Therefore, it is my opinion that Kajiyama discloses this limitation of claim 1 of the '764 patent.

d. Limitation 1[c]: “a first insulating sidewall formed on each side surface of the gate electrode; and”

Limitation 1[d]: “a second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween,”

282. Kajiyama discloses that “the semiconductor device of the present invention ... comprises ... a first sidewall consisting of a dielectric film formed on a sidewall of the gate electrode, and a second sidewall consisting of an oxidizing resistant film formed to cover the first sidewall.” Ex.1011, ¶14, FIG. 1(D). Kajiyama’s first sidewall (*see id.*, FIG. 1(D) (below) (shaded purple)) and second sidewall (*see id.* (shaded green)) are illustrated below as formed on each side surface of the gate electrode.



283. Kajiyama discloses that its first sidewall 5 “consist[s] of ZrO_2 film (insulation film).” Ex.1011, ¶28. Kajiyama further teaches that “the effects of the present invention can be obtained even with other dielectric films [for first sidewall 5], such as TEOS films, BPSG films, or SiON films.” *Id.*, ¶47. In my opinion, a POSITA would have understood that each of TEOS, BPSG, and SiON is a silicon-based oxide and known insulating material.

284. Kajiyama’s second sidewall 6 is a silicon nitride film 6 (referred to as Si_3N_4 film), which, in my opinion, a POSITA would also have known to be an insulating material often used in sidewalls. Ex.1011, ¶28. Therefore, a POSITA would have understood Kajiyama’s first and second sidewalls formed on each side surface of the gate electrode to be insulating sidewalls in my opinion.

285. As shown above in Figure 1(D), Kajiyama’s second sidewall (*see* Ex.1011, FIG. 1(D) (above) (shaded green)) is also formed on the side surface of the gate electrode, with first sidewall 6 (*see id.* (shaded purple)) situated between the

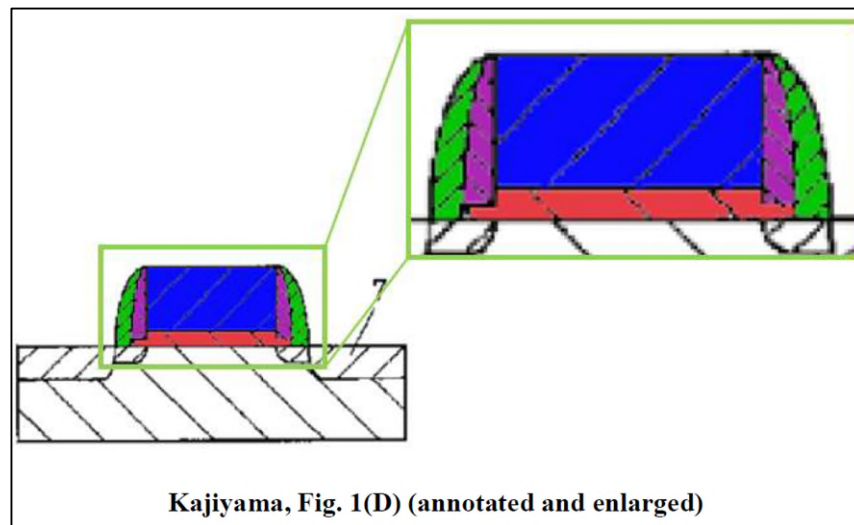
gate electrode 3 (*see id.* (shaded blue)) and the second sidewall. Kajiyama's second sidewall is therefore a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween.

286. Therefore, it is my opinion that Kajiyama discloses these limitations of claim 1 of the '764 patent.

- e. **Limitation 1[e]: “wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, and”**

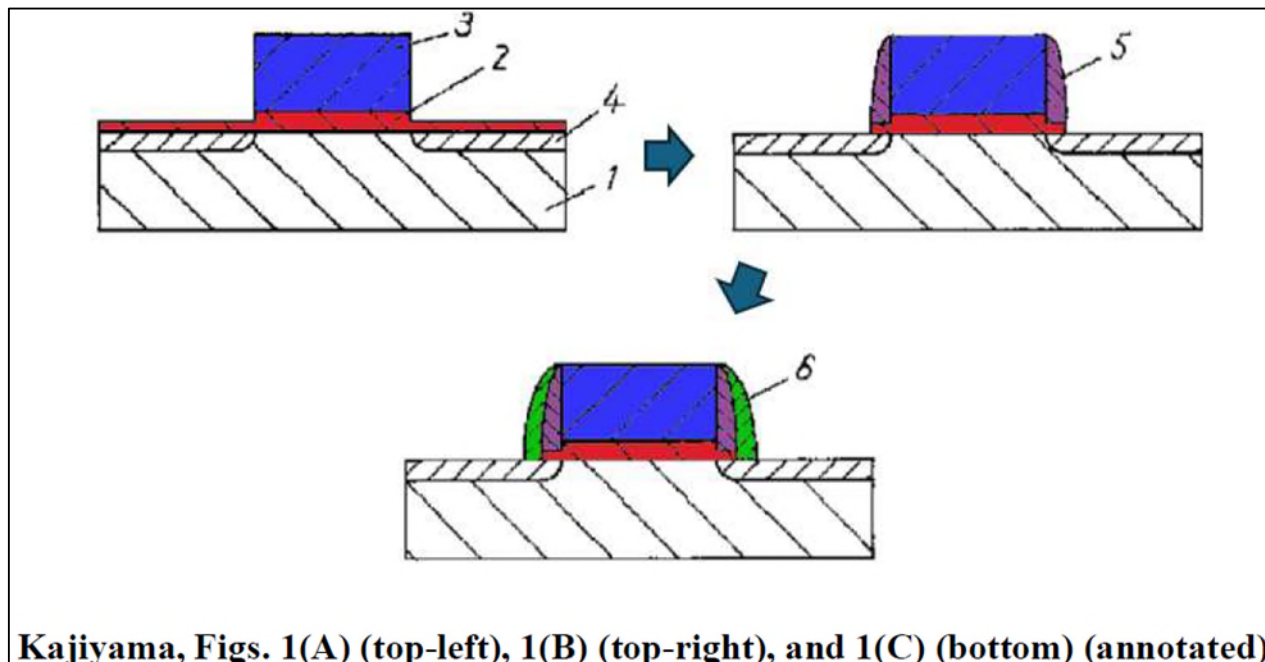
Limitation 1[f]: “part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.”

287. Kajiyama's high-k film 2 (*see* Ex.1011, FIG. 1(D) (below) (shaded red)) is an uninterrupted layer that extends from under the gate electrode to under first sidewall 5 (i.e., the claimed “first insulating sidewall” (*see id.* (shaded purple))).



288. The high-k film is thinner under sidewall 5 (i.e., the claimed “first insulating sidewall”) than it is under the gate electrode 3 (*see* Ex.1011, FIG. 1(D) (above) (shaded blue)). Therefore, Kajiyama’s semiconductor device discloses these limitations in my opinion.

289. Kajiyama’s fabrication process confirms the structure of its semiconductor device, as explained above. During fabrication, Kajiyama discloses that an n-type polySi film is deposited on high-k film 2 and etched “to form a gate electrode 3.” Ex.1011, ¶29. As part of that process, high-k film 2 “is also etched to reduce the film” *Id.*, ¶29. As a result, the thickness of high-k film 2 is greater under the gate electrode than in the areas outside of the gate electrode, which is illustrated below (*see id.*, FIG. 1(A) (below, top-left)).



290. After forming the gate electrode 3 (see Ex.1011, FIGS. 1(B)-(C) above) (shaded blue)) and partially etching the insulating film 2 (see *id.* (shaded red)), first sidewall 5 (see *id.* (shaded purple)) is formed on the side of gate electrode 3 and over the thinner portion of the high-k film 2. *Id.*, ¶30. The result of the formation of first sidewall 5 on the side of gate electrode 3 and over the thinner portion of the high-k film 2 is shown in Figure 1(B) (above, top-left).

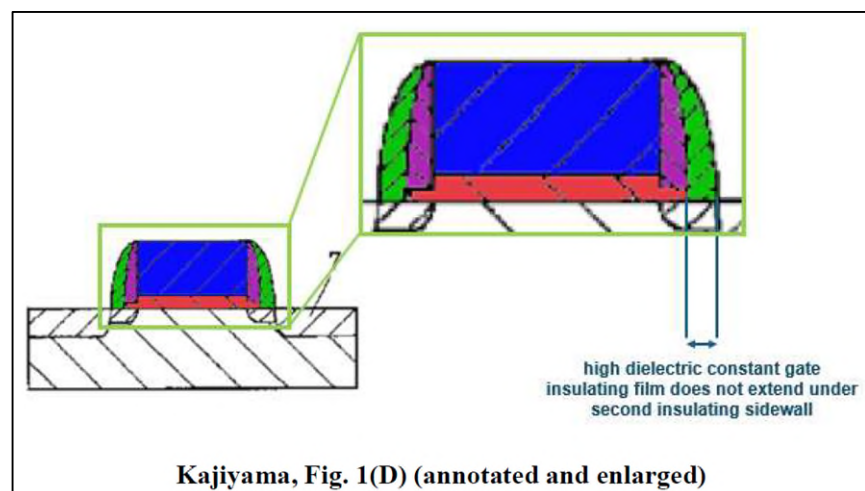
291. The high-k film 2 is then etched “to remove all,” which a POSITA would have understood to mean that the high-k film 2 outside the outer edge of sidewall 5 is etched down to the substrate and completely removed, leaving only the portions of the film covered by the gate electrode and first insulating sidewall. Ex.1011, ¶30. Then, second sidewall 6 (see *id.*, FIG. 1(C) (above, bottom) (shaded green)) is formed “to cover the first sidewall 5 provided on the sidewall of the gate

electrode 3.” *Id.*, ¶31. As shown in Figure 1(C) (above, bottom), a portion of the high-k dielectric film (shaded red) remains under the gate electrode and first sidewall 5 (shaded purple) but does not extend under sidewall 6 (shaded green).

292. Thus, it is my opinion that Kajiyama’s first embodiment semiconductor device discloses these limitations of claim 1 of the ’764 patent.

2. Dependent Claim 5: “The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall.”

293. In Kajiyama’s first embodiment semiconductor device, high-k dielectric film 2 (see Ex.1011, FIG. 1(D) (below) (shaded red)) is formed so as to be located only under gate electrode 3 (see *id.* (shaded blue)) and first sidewall 5 (see *id.* (shaded purple)), and not under sidewall 6 (i.e., the “second insulating sidewall” (see *id.* (shaded green))).



294. As explained above, Kajiyama's fabrication process includes etching the high-k film outside the outer edge of sidewall 5 down to the substrate, and removing the etched high-k film, leaving only the portions of the high-k film covered by the gate electrode and first insulating sidewall, prior to forming the second insulating sidewall. Ex.1011, ¶¶30-31.

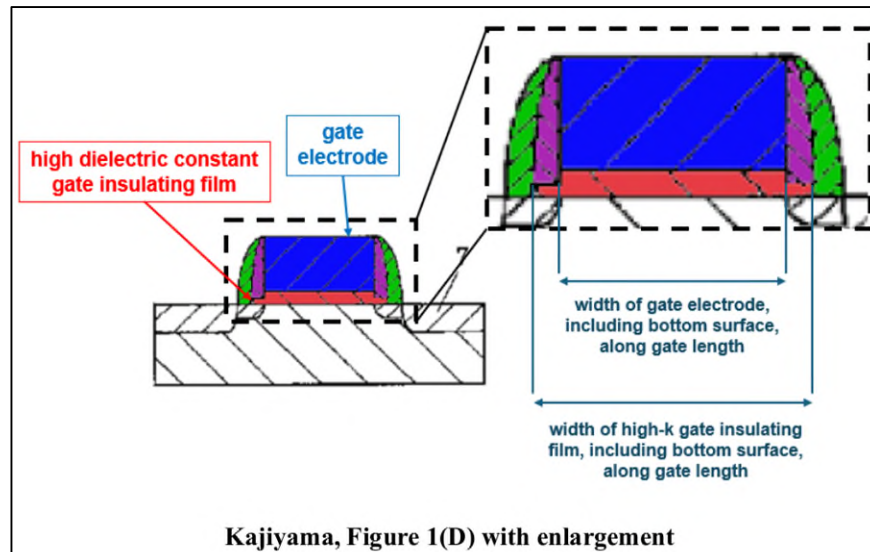
295. Therefore, it is my opinion that Kajiyama's fabrication process confirms the structure of its first embodiment semiconductor device that is discussed above and discloses claim 5 of the '764 patent.

3. **Dependent Claim 16: "The semiconductor device of claim 1, wherein a width of the high dielectric constant gate insulating film along a gate length is larger than a width of the gate electrode along the gate length."**

Dependent Claim 17: "The semiconductor device of claim 1, wherein a width of a bottom surface of the high dielectric constant gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length."

296. These claims address the width of the gate insulating film relative to the gate electrode. As I explained above, high-k gate insulating film 2 in Kajiyama's first embodiment extends from under the gate to under the first insulating sidewall. As illustrated in Figure 1(D) below, along the gate length, the width of high-k gate insulating film 2 (shaded red), including the bottom surface of high-k gate insulating film 2, is larger than the width of the gate electrode 3 (shaded blue), including the

bottom surface of the gate electrode 3. Therefore, it is my opinion that Kajiyama discloses claims 16 and 17.



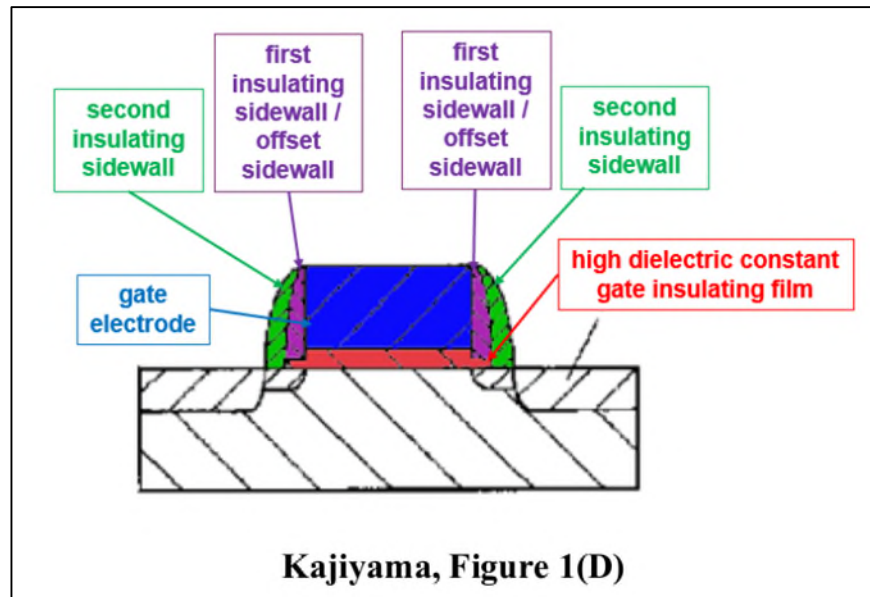
I. Ground IX

297. In my opinion, Kajiyama renders obvious Challenged Claims 4, 6, and 18-19 of the '764 patent (Ground IX). As discussed above with regard to Ground VIII, Kajiyama anticipates every limitation of claim 1 of the '764 patent. To the extent Kajiyama is found not to anticipate the additional limitations of claims 4, 6, and 18-19, a POSITA would have found those limitations obvious in view of Kajiyama, as explained below.

1. Dependent Claim 4: "The semiconductor device of claim 1, wherein the first insulating sidewall is an offset sidewall."

298. As discussed above with regard to limitation 1[c], in Kajiyama's first embodiment, first sidewall 5 is the claimed first insulating sidewall. While Kajiyama does not refer to first sidewall 5 as an offset sidewall, a POSITA would understand

first sidewall 5, located between gate electrode 3 and second sidewall 6, is an offset sidewall consistent with the disclosures of the '764 patent specification. Ex.1334, 216-17, Fig. 5-25; Ex.1011, FIG. 1(D) (below).



299. For example, the '764 patent refers to an inner sidewall as an offset sidewall: "An insulating sidewall 7 is formed on each side surface of the gate electrode 5 with an offset sidewall 6 interposed therebetween." Ex.1001, 7:37-39, FIG. 2. Kajiyama's first sidewall 5 meets the same description. *See also* Ex.1334, 216-17, Fig. 5-25. Therefore, it is my opinion that Kajiyama renders obvious claim 4 of the '764 patent.

2. Dependent Claim 6: “The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a Hf based oxide.”

300. Kajiyama discloses a ZrO_2 film as the gate insulating film in its first embodiment, but also states that “other high dielectric films, such as a HfO_2 film, a Ta_2O_5 film, or a Al_2O_3 film, can be used instead to obtain the effects of the invention” (Ex.1011, ¶45), indicating that the use of alternative high-k materials, including HfO_2 , was within the scope of the invention.

301. To the extent this teaching is not found to be an explicit disclosure of a gate insulating film formed of a Hf based oxide, as recited by claim 6, it would have been obvious to a POSITA in my opinion. Based on Kajiyama’s suggestion to use other high dielectric constant films such as HfO_2 as a substitute for ZrO_2 , a POSITA would have been motivated to select that Hf based oxide.

302. Furthermore, a POSITA would have found HfO_2 to be an advantageous choice for the high dielectric constant gate insulating film of Kajiyama’s semiconductor device because HfO_2 was already commonly used in the industry due to its many known benefits, including superior thermal stability and band gap alignment. Ex.1337, 2.4.1 (“Recently, HfO_2 films have emerged as the most promising gate dielectric material for sub 100nm technology due to its superior thermal stability with poly-Si and reasonable band alignment”); Ex.1213, 207 (HfO_2 “combines a high k (15–26) with a bandgap of 5.6 eV, with favourable

conduction and valence band offsets with respect to Si ...”); Ex.1349, 134 (“Excellent dielectric properties such as high dielectric constant, low leakage current, good thermal stability, negligible dispersion and excellent reliability were demonstrated. These results suggest that HfO₂ is a promising material for the future gate dielectric application.”). Additionally, HfO₂ also could be scaled down to a smaller EOT. Ex.1213, 207.

303. Therefore, in my opinion, a POSITA would have been motivated to choose Kajiyama’s hafnium-based oxide (i.e., HfO₂) as the high-k gate insulating film in its semiconductor device, rendering obvious claim 6 of the ’764 patent in view of Kajiyama.

3. **Dependent Claim 18: “The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more.”**

Dependent Claim 19: “The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall.”

304. Kajiyama’s first embodiment anticipates the limitations of claims 18 and 19 because the dielectric constants of materials disclosed by Kajiyama for the gate insulating film and the second insulating sidewall are inherent to those materials. However, even if that were not found to be the case, then at a minimum, Kajiyama renders obvious the limitations of claims 18 and 19.

305. The “relative dielectric constant” is an inherent property of a material. The ’764 patent acknowledges that a “high dielectric constant film formed of a Hf based oxide, Al based oxide or the like [] has a relative dielectric constant of 10 or more, instead of an SiO₂ based insulating film having a relative dielectric constant of about 4.” Ex.1001, 1:28-31. Kajiyama teaches that, in addition to ZrO₂ “other high dielectric films, such as a HfO₂ film, a Ta₂O₅ film, or a Al₂O₃ film, can be used instead to obtain the effects of the invention.” Ex.1011, ¶45. ZrO₂ has a dielectric constant of 25, HfO₂ has a dielectric constant of 25, and Ta₂O₅ has a dielectric constant of 26, all of which are greater than 10. Ex.1018, Table I.

306. Kajiyama also discloses that the second sidewall 6 is comprised of silicon nitride (Si₃N₄), which is known to have a dielectric constant of approximately 7. Ex.1011, ¶28; Ex.1018, Table I. While Kajiyama does not expressly disclose the relative dielectric constants of the listed materials, the dielectric constant is an inherent property of the material and, therefore, the dielectric constants for ZrO₂, HfO₂, Ta₂O₅, and Si₃N₄ are necessarily present in Kajiyama, and would have been understood by a POSITA in view of Kajiyama.

307. Since Kajiyama’s second sidewall 6 is comprised of silicon nitride (Si₃N₄), which has a dielectric constant of 7, and Kajiyama’s high-k gate insulating film can be a number of materials with a dielectric constant greater than 20, Kajiyama discloses the high dielectric constant gate insulating film has a larger

relative dielectric constant than that of the second insulating sidewall as recited by claim 19.

308. Therefore, it is my opinion that Kajiyama renders obvious claims 18 and 19 of the '764 patent.

J. Ground X

309. As discussed above with regard to Ground VIII, Kajiyama anticipates every limitation of claim 1. To the extent Kajiyama is found not to disclose the additional limitations of claim 11, Wang teaches the limitations of that claim, as explained below. In my opinion, a POSITA would have been motivated to combine these references, thereby rendering obvious claim 11.

1. Dependent Claim 11: “The semiconductor device of claim 1, wherein each side end portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less.”

310. Wang discloses that the high-k dielectric layer 6 “is preferably less than about 50 Å to maintain low gate leakage and thin equivalent oxide thickness (EOT).” Ex.1012, ¶26. For an exemplary HfSiON gate insulating layer, the film “was deposited to a thickness of about 5 to 50 Angstroms and having an equivalent oxide thickness (EOT) of less than about 2.0 nanometers.” *Id.*, ¶34. Wang also specifically claims a device “wherein the high-k dielectric has a thickness from about 5 to 50 Å.” *Id.*, claim 3.

311. As I noted above, Wang relates to semiconductor devices (Ex.1012, ¶2), so it is in the same field as Kajiyama and the '764 patent. Ex.1001, 1:15-16 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); Ex.1011, ¶1 (“The present invention relates to semiconductor devices.”) In my opinion, a POSITA would have been motivated to use thinner gate insulating films, as taught by Wang, consistent with the goal of miniaturizing semiconductor devices.

312. In the combined device of Kajiyama and Wang, the thickness of the high-k gate insulating film at its side ends would also range from about less than 5 Angstroms to less than 50 Angstroms since the thickness of the layer is smaller under sidewall 8 than under the gate electrode 7. The range of 5 to 50 Angstroms is equivalent to 0.5 to 5 nm, and, therefore, Wang’s preferred range includes thicknesses less than 2 nm, as recited by claim 11. In other words, the thickness of 2 nm (i.e., 20 Angstroms) recited by claim 11 falls within the range of thicknesses disclosed by Wang for the side end portion of its high dielectric constant gate insulating film.

313. I have been informed, and understand, that where a claimed range overlaps with a range disclosed in the prior art, there is a presumption of obviousness, and it becomes the patentee’s burden to present evidence of teaching away, unexpected results or criticality, or other pertinent objective indicia indicating

that the overlapping range would not have been obvious in light of that prior art. Based on my review of the intrinsic record, there is no discussion, evidence, or justification for the selection of 2 nm as the thickness of the gate insulating film.

314. For the foregoing reasons, it is my opinion that the combination of Kajiyama and Wang renders obvious claim 11 of the '764 patent.

K. Ground XI

315. In my opinion, Kajiyama in combination with Sim renders obvious Challenged Claim 11 of the '764 patent (Ground XI). To the extent the combination of Kajiyama and Wang is found not to disclose the additional limitations of claim 11, Sim teaches the limitations of that claim, as explained below. In my opinion, a POSITA would have been motivated to combine Kajiyama and Sim, thereby rendering obvious claim 11.

1. Dependent Claim 11: “The semiconductor device of claim 1, wherein each side end portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less.”

316. Sim’s study related to the use of high-k dielectrics used in semiconductor devices. Ex.1024, Abstract (“Scaling the physical thickness of the HfO₂ dielectric causes less charge trapping and higher mobility.”). Sim is therefore in the same field as Kajiyama and the '764 patent. Ex.1001, 1:15-16 (“The present invention relates to a semiconductor device and a method for fabricating the

semiconductor device.”); Ex.1011, ¶1 (“[t]he present invention relates to semiconductor devices.”

317. Sim describes use of a gate insulating film having a thickness of 2nm or less. Specifically, Sim explains that “[h]afnium-based high-k dielectrics and metal gate electrodes have been aggressively investigated to ensure continued scaling of CMOS technology, but several drawbacks such as low mobility and charge trapping have been identified.” Ex.1024, 218. Sim’s authors addressed these drawbacks by testing films of different thickness and “systematically evaluat[ing] the effects of high-k film thickness on charge trapping and channel carrier mobility.” *Id.* As a result, Sim found that “scaling the high-k dielectric is a simple, but very effective means of improving mobility and other reliability characteristics.” *Id.*

318. In particular, Sim concluded that “[s]caling the physical thickness of the HfO₂ dielectric to below 20Å causes less charge trapping and higher mobility.” Ex.1024, 221. 20Å is equal to 2 nm, which is the thickness recited by claim 11. The thickness of the high-k film is even smaller under sidewall 5 (i.e., the side portion) than under the gate electrode and would therefore be less than 2 nm according to Sim’s teachings. Thus, the semiconductor devices resulting from the combination of Kajiyama’s first embodiment with Sim provides that each side portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less.

319. Kajiyama discloses use of HfO_2 as an example of a high-k gate dielectric (Ex.1011, ¶145), the same film studied in Sim. A POSITA would have been motivated to apply Sim's findings regarding ideal thicknesses of a HfO_2 gate insulating film (namely, a thickness of $20\text{\AA}$ (2 nm) or less) to Kajiyama's semiconductor device.

320. According to Sim, reducing the thickness of HfO_2 to below $20\text{\AA}$ enhances mobility and reduces charge trapping, key issues in ensuring the performance and scalability of semiconductor devices. Ex.1024, 221. In my opinion, the combination would have been nothing more than the use of a known technique (Sim's HfO_2 dielectric layer with less than $20\text{\AA}$ thickness) to improve similar devices (the Kajiyama's semiconductor device having a HfO_2 high-k gate dielectric layer), in the same way. A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable because Sim uses a well-known process, atomic layer deposition (ALD), for fabricating high-k films. Ex.1024, 218.

321. Therefore, it is my opinion that the combination of Kajiyama and Sim renders obvious claim 11 of the '764 patent.

L. Ground XII

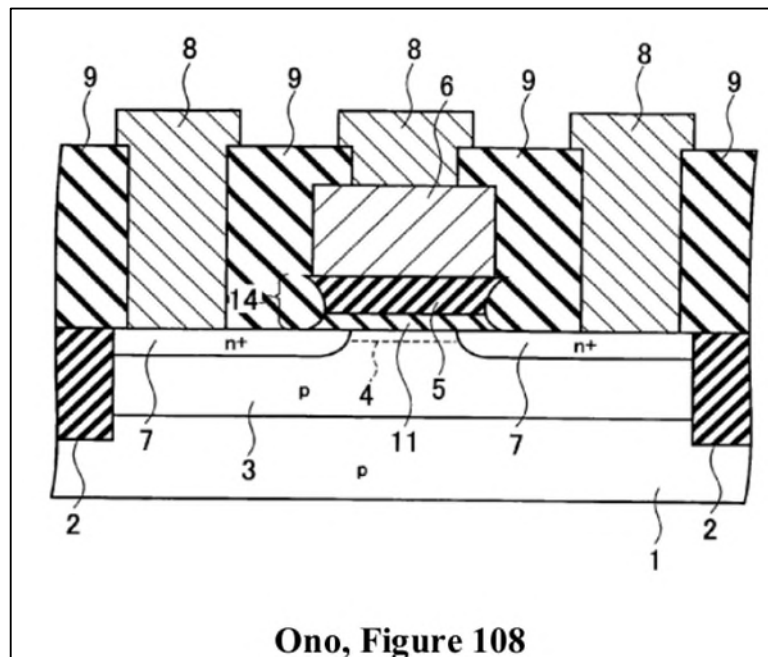
322. In my opinion, Kajiyama in combination with Ono renders obvious Challenged Claims 12 and 13 of the '764 patent (Ground XII). As discussed above

with regard to Ground VIII, Kajiyama anticipates every limitation of claim 1 of the '764 patent. To the extent Kajiyama is found not to disclose the additional limitations of claims 12 and 13, Ono teaches the limitations of those claims, as explained below. In my opinion, a POSITA would have been motivated to combine Kajiyama and Ono, thereby rendering obvious claims 12 and 13.

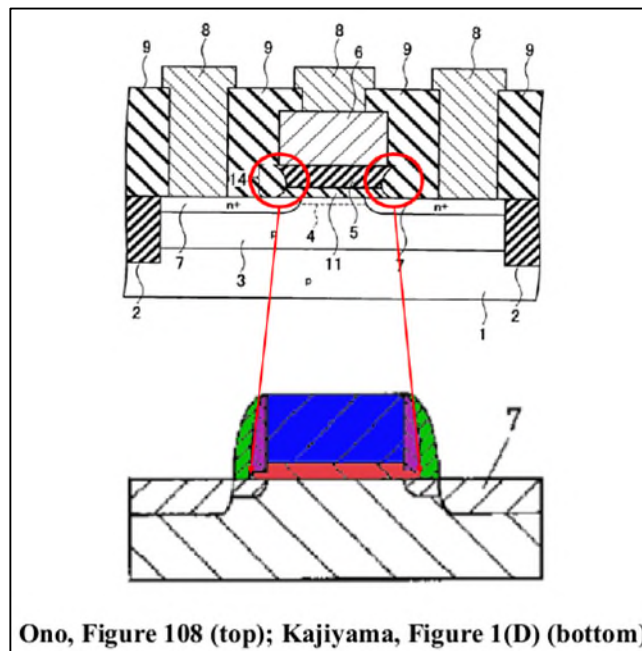
1. **Dependent Claim 12: “The semiconductor device of claim 1, wherein a side surface of the high dielectric constant gate insulating film is located at a predetermined distance from a side end surface of the first insulating sidewall toward the gate electrode.”**

Dependent Claim 13: “The semiconductor device of claim 1, wherein a side surface of the high dielectric constant gate insulating film is located at a predetermined distance from a side end surface of the gate electrode toward the first insulating sidewall.”

323. Ono and Kajiyama are in the same field as the '764 patent. Ex.1001, 1:15-16; Ex.1011, ¶1; Ex.1013, ¶¶3-7. Ono discloses that “the sidewalls of the gate insulator film may curve” as shown, e.g., in Figure 108 (below). Ex.1013, ¶216.



324. A POSITA would have been motivated to apply Ono's teaching of curving the end portions of a gate insulating film (see Ex.1013, FIG. 108 (below, top) (shaded red)) to Kajiyama's high-k dielectric in the first embodiment (see Ex.1012, FIG. 1(D) (below, bottom)), as illustrated below. In the combination, the side ends of Kajiyama's gate insulating film have a semicircular shape, as taught by Ono.

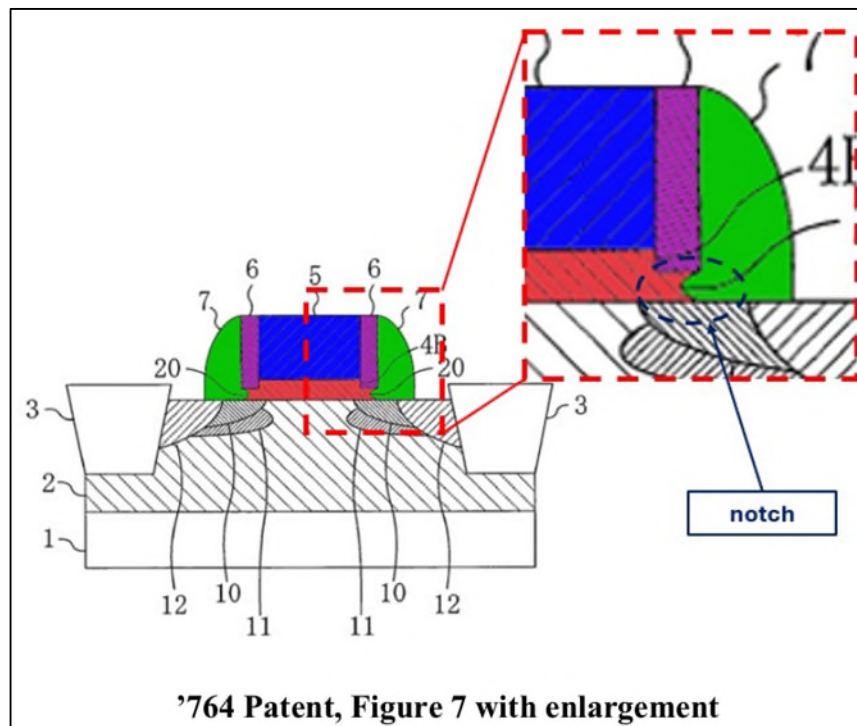


325. A POSITA would have been motivated to make the above combination because Ono expressly suggests the combination, as discussed above with reference to the combination of Ono with Matsumoto, and to improve performance of Kajiyama's first embodiment device by optimizing the electrical capacitance between the gate electrode and the source/drain regions. Ex.1013, ¶¶200, 216.

326. In my opinion, the Kajiyama-Ono combination is nothing more than the use of a known technique (Ono's use of curved side surfaces for a gate insulating film) to improve similar devices in the same way for the above reasons. Thus, a POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable.

327. Kajiyama and Ono both use high-k gate insulating films that extend under the gate electrode and the insulating sidewall, a concept well-known before

the '764 patent, and both form their high-k dielectrics using conventional techniques. Ex.1011, ¶29; Ex.1013, ¶167. In the device of the Kajiyama-Ono combination, the end portion of Kajiyama's gate insulating film has a semicircular shape, as taught by Ono. The Kajiyama-Ono combination therefore discloses a device where the high dielectric constant gate insulating film includes a notch at a side end portion, consistent with the disclosure of the '764 patent. *See e.g.*, Ex.1001, 8:35-40 (referring to notch 20 of FIG. 7), FIG. 7 (depicting notch 20 having a semicircular shape).



328. Additionally, in the Kajiyama-Ono combination, when the notch is applied at each side end of Kajiyama's gate insulating film 2 located under the first sidewall 5, the end of the gate insulating film no longer extends completely under

the first insulating sidewall. Further, the notch's semicircular shape and the distance which the semicircular shape extends inward toward the gate electrode are set by specific process parameters.

329. Accordingly, in the Kajiyama-Ono combination, the gate insulating film's side surface is located at a predetermined distance from a side end surface of the first insulating sidewall toward the gate electrode and from a side end surface of the gate electrode toward the first insulating sidewall, consistent with the disclosure of the '764 patent. Ex.1001, 21:26-30 ("side surface ... may be located at a predetermined distance from a side end surface of the sidewall 7 or the offset sidewall 6 toward the gate electrode 5").

330. Therefore, it is my opinion that the combination of Kajiyama and Ono renders obvious claims 12 and 13 of the '764 patent.

M. Ground XIII

331. In my opinion, Kajiyama in combination with Bu renders obvious Challenged Claims 14 and 15 of the '764 patent (Ground XIII). As discussed above with regard to Ground VIII, Kajiyama anticipates every limitation of claim 1 of the '764 patent. To the extent Kajiyama is found not to disclose the additional limitations of claims 14 and 15, Ono teaches the limitations of those claims. Specifically, the Kajiyama-Bu combination discloses an outer sidewall with "a double layer structure" and "a triple layer structure" in my opinion, as explained in detail below. In my

opinion, a POSITA would have been motivated to combine Kajiyama and Bu, thereby rendering obvious claims 14 and 15.

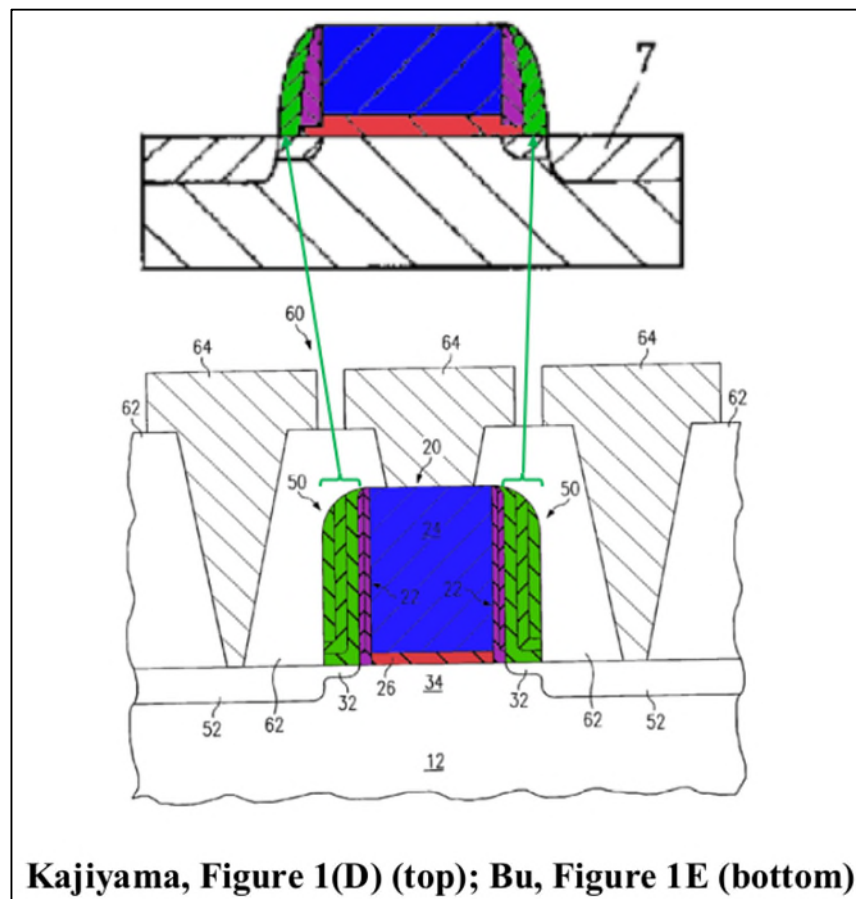
1. **Dependent Claim 14: “The semiconductor device of claim 1, wherein the second insulating sidewall has a double layer structure including an oxide film and a nitride film.”**

Dependent Claim 15: “The semiconductor device of claim 1, wherein the second insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film.”

332. As I noted above, Bu relates to semiconductor devices (Ex.1025, Abstract), so it is in the same field as Kajiyama and the '764 patent. Ex.1001, 1:15-16 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); Ex.1011, ¶1 (“The present invention relates to semiconductor devices.”). Bu teaches an outer sidewall structure having three layers. Ex.1025, ¶¶26, 42-43. Bu’s sidewall structure includes a first sidewall-forming layer 40 comprising an oxide, a second sidewall-forming layer 42 comprising a nitride, and a third sidewall-forming layer 44 comprising an oxide. Ex.1025, ¶¶27, 30, 35.

333. In my opinion, a POSITA would have been motivated to use Bu’s triple-layer ONO sidewall structure with Kajiyama’s first embodiment device. In Kajiyama’s first embodiment, the second sidewall 6 is a silicon nitride film (i.e., “a nitride film”). Ex.1011, ¶28. In my opinion, a POSITA would have been motivated

to form Kajiyama's second sidewall 6 (see Ex.1012, FIG. 1(D) (below, top) (shaded green)) with two additional silicon oxide layers to create a triple-layer ONO sidewall structure, as taught by Bu. See Ex.1025, FIG. 1E (below, bottom). The resulting device discloses that the second insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film.



334. A POSITA would have been motivated to combine Bu's teaching of a triple-layer ONO sidewall structure with Kajiyama in light of the known benefits of ONO structures. For example, Bu teaches that "the film properties of sidewall-forming layers 40 and 42 may minimize dopant loss from source drain extension

region 32 to first sidewall-forming layer 40,” thereby lowering parasitic resistance. Ex.1025, ¶26.

335. In my opinion, the combination is nothing more than the use of a known technique (Bu’s triple-layer sidewall) to improve similar devices in the same way. Finally, Kajiyama and Bu disclose forming sidewall layers using standard deposition and etching techniques (Ex.1011, ¶¶30-31; Ex.1025, ¶¶27, 30, 35, 38), making the application of Bu’s multiple-layer structure to Kajiyama’s device straightforward. Accordingly, a POSITA would have had a reasonable expectation of success in the combining Kajiyama and Bu, leading to predictable results.

336. Additionally, in my opinion, a POSITA would also have been motivated by Bu’s teachings to form Kajiyama’s second sidewall 6 (formed of nitride) with a single additional silicon oxide layer to create a double-layer sidewall structure, resulting in a device where the second insulating sidewall has a double layer structure including an oxide film and a nitride film. As discussed above, Bu teaches that the film properties of additional layers may minimize dopant loss and lower parasitic resistance. Ex.1025, ¶26. Additionally, where design requirements dictate reducing manufacturing complexity, a POSITA would have known to use fewer (i.e., two) layers to similarly achieve the benefits taught by Bu. In light of these considerations, a POSITA would have been motivated in my opinion to implement Bu’s teachings into Kajiyama’s device to form a double-layer sidewall structure.

337. For the same reasons discussed above with respect to the triple-layer sidewall structure, it is my opinion that the combination of Kajiyama and Bu to include a double-layer sidewall structure is nothing more than the use of a known technique to improve similar devices in the same way, and a POSITA would have had a reasonable expectation of success in the combining these references, leading to predictable results.

N. Ground XIV

338. In my opinion, Kajiyama in combination with Wilk renders obvious Challenged Claims 18 and 19 of the '764 patent (Ground XV). As discussed above with regard to Ground VIII, Kajiyama anticipates every limitation of claim 1 of the '764 patent.

339. As I explained above, it is my opinion that Kajiyama already discloses the limitations of claims 18 and 19 because the dielectric constants of materials disclosed by Kajiyama for both the gate insulating film and the second insulating sidewall are inherent to those materials. Even if it were not found to be the case, then Kajiyama in light of the knowledge of a POSITA, at a minimum, renders the limitations of claims 18-19 obvious.

340. If this were also not found to be the case, then Wilk provides an explicit disclosure of dielectric constants. In my opinion, a POSITA would have been motivated to combine Kajiyama and Wilk, thereby rendering obvious claims 18 and 19.

1. **Dependent Claim 18: “The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more.”**

Dependent Claim 19: “The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall.”

341. Wilk explores the properties of materials “under consideration” in 2001 “as potential replacements for SiO₂ as the gate dielectric material for sub-0.1 μm CMOS technology.” Ex.1018, Abstract. Wilk discloses the following table of relevant properties, including dielectric constants, for various materials:

TABLE I. Comparison of relevant properties for high- κ candidates.				
Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si	Crystal structure(s)
SiO ₂	3.9	8.9	3.2	Amorphous
Si ₃ N ₄	7	5.1	2	Amorphous
Al ₂ O ₃	9	8.7	2.8 ^a	Amorphous
Y ₂ O ₃	15	5.6	2.3 ^a	Cubic
La ₂ O ₃	30	4.3	2.3 ^a	Hexagonal, cubic
Ta ₂ O ₅	26	4.5	1–1.5	Orthorhombic
TiO ₂	80	3.5	1.2	Tetrag. ^c (rutile, anatase)
HfO ₂	25	5.7	1.5 ^a	Mono. ^b , tetrag. ^c , cubic
ZrO ₂	25	7.8	1.4 ^a	Mono. ^b , tetrag. ^c , cubic

^aCalculated by Robertson (See Ref. 153).
^bMono.=monoclinic.
^cTetrag.=tetragonal.

Wilk, Table I

Id., Table 1. In my opinion, a POSITA would have been motivated to look to Wilk’s teachings to understand the properties of materials discussed in Kajiyama.

342. As I noted above, Wilk relates to semiconductor devices (Ex.1018, Abstract), so it is in the same field as Kajiyama and the '764 patent. Ex.1001, 1:15-16 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); Ex.1011, ¶1 (“The present invention relates to semiconductor devices.”). Wilk is specifically directed to high-k materials for gate dielectric applications and lists relevant properties of materials discussed in Kajiyama, allowing a POSITA to, for example, ensure that Kajiyama’s gate insulating film had a sufficiently high dielectric constant.

343. Kajiyama teaches that, in addition to ZrO_2 , “other high dielectric films, such as a HfO_2 film, a Ta_2O_5 film, or a Al_2O_3 film, can be used instead to obtain the effects of the invention.” Ex.1011, ¶45. Wilk’s discloses, for example, that ZrO_2 has a dielectric constant of 25, HfO_2 has a dielectric constant of 25, and Ta_2O_5 has a dielectric constant of 26. Ex.1018, Table I. All of these values are greater than 10, as required by claim 18.

344. Kajiyama discloses that the second sidewall 6 is comprised of silicon nitride (Si_3N_4). Ex.1011, ¶28. Table I of Wilk discloses Si_3N_4 has a dielectric constant of 7. Ex.1018, Table I. The dielectric constants of ZrO_2 , HfO_2 , and Ta_2O_5 are also greater than 7, as required by claim 19.

345. Thus, in the devices resulting from the combination of Kajiyama and Wilk, the high dielectric constant gate insulating film has a relative dielectric

constant of 10 or more and the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall. Therefore, it is my opinion that Matsumoto combined with Wilk discloses claims 18 and 19 of the '764 patent.

XI. CONCLUSION

346. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

347. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Declaration of Dr. Sanjay Banerjee
Inter Partes Review of U.S. Patent No. 7,923,764

Date: May 30, 2025

Respectfully submitted,



Sanjay Banerjee, Ph.D.