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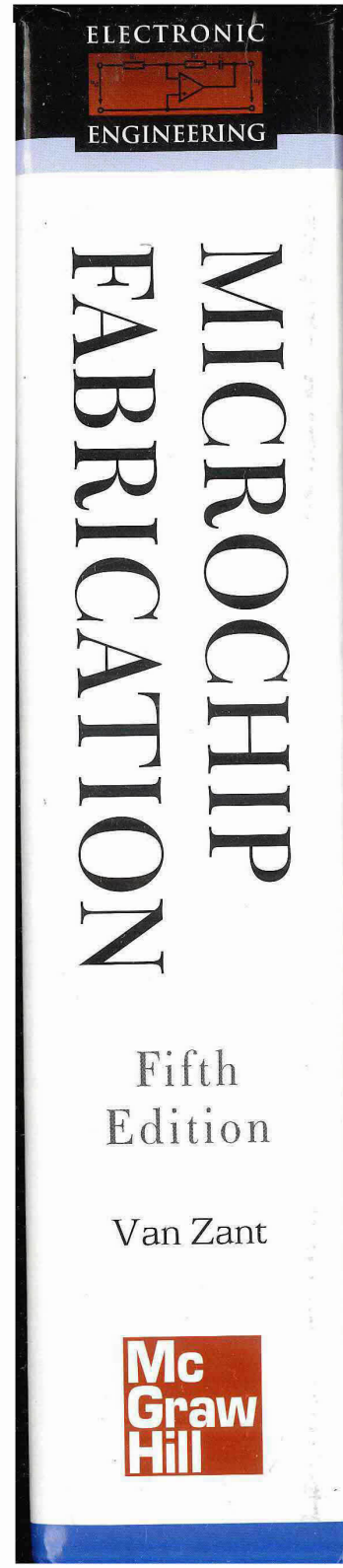
Microchip Fabrication

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A Practical Guide to Semiconductor Processing

Peter Van Zant

Fifth Edition

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This edition is dedicated to two exceptional women, Marilyn (Van Zant) O'Connor and Anne Miller. Marilyn is my lovely and loving sister. She is also my good friend, enthusiastic supporter, and a wise confidant. Thanks, sis.

For over twenty years Anne has been a collaborator, business partner, and friend. Her wise business counsel and contributions to this text are greatly appreciated.

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Preface to the Fifth Edition

Despite recessions, the microchip industry continues its evolutionary march to the physical limits of silicon-based ICs. Fortunately, the end seems always just over the hill, and the industry keeps chugging along. Unfortunately, keeping a textbook current with the advances in microchip fabrication means frequent updates. Hence this fifth edition.

This edition follows the same chapter sequence as the previous editions. Hopefully, this will assist instructors in upgrading their course curriculums. Fortunately, the basics of semiconductor device operation and wafer processing remain the same and will be found in this edition.

My thanks go to Steve Chapman, my editor at McGraw-Hill. His guidance and patience with my writing schedule are appreciated.

Many thanks to Anne Miller and Michael Heynes of Semiconductor Services for their consultation and input. Alex Braun, of Semiconductor International, and Nikki Wood, of Future Fab International, were most helpful with securing permission to reproduce material from their fine publications. Jeff Eckert, of J. K. Eckert & Co., did a fine job on organizing the over 600 figures and editing the manuscript. Mark Hall, Mark Hall Design, and David Wellner did yeoman's work transforming my hand drawings into understandable illustrations.

Last, but not least, thanks to my wife Mary Dewitt for enduring my 5:30 A.M. writing sessions and her unending support.

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About the Author

Peter Van Zant is an internationally known semiconductor professional with an extensive background in process engineering, training, consulting, and writing. Principal of Peter Van Zant Associates, a firm that supplies writing, training, and consulting services to business and industry, he is the author of *Semiconductor Technology Glossary,* Third Edition; *Integrated Circuits Text; Safety First Manual;* and *Chip Packaging Manual.* His books and training materials are used by chip manufacturers, industry suppliers, colleges, and universities. Peter Van Zant Associates' customers include Intel, National Semiconductor, Applied Materials, Air Products and Chemicals, SCP Global Inc., and a number of educational institutions. Mr. Van Zant is also the elected District 1 Supervisor in his home county of Nevada in California.

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Chapter

1

The Semiconductor Industry

Overview

In this chapter, you will be introduced to the semiconductor industry with a description of the historic product and process developments and the rise of semiconductors into a major world industry. The major manufacturing stages, from material preparation to packaged product, are introduced along with the mainstream product types, transistor building structures, and the different integration levels. Industry product and processing trends are identified.

Objectives

Upon completion of this chapter, you should be able to:

1. Describe the difference between discrete devices and integrated circuits.
2. Define the terms "solid-state, "planar processing" and "N-type" and "P-type" semiconducting materials.
3. List the four major stages of semiconductor processing.
4. Explain the integration scale and at least three of the implications of processing circuits of different levels of integration.
5. List the major process and device trends in semiconductor processing.

Birth of an Industry

The electronics industry got its jump start with the discovery of the audion vacuum tube in the 1906 by Lee Deforest.[1] It was made possi-

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ble the radio, television, and other consumer electronics. It also was the brains of the world's first electronic computer, named the Electronic Numeric Integrator and Calculator (ENIAC), first demonstrated at the Moore School of Engineering in Pennsylvania in 1947.

This ENIAC hardly fits the modern picture of a computer. It occupied some 1500 square feet, weighed 30 tons, generated large quantities of heat, required the services of a small power station, and cost $400,000 in 1940 dollars. The ENIAC was based on 19,000 vacuum tubes along with thousands of resistors and capacitors (Fig. 1.1).

A vacuum tube consists of three elements: two electrodes separated by a grid in a glass enclosure (Fig. 1.2). Inside the enclosure is a vacuum, required to prevent the elements from burning up and to allow the easy transfer of electrons.

Tubes perform two important electrical functions: *switching* and *amplification*. Switching refers to the ability of an electrical device to turn a current on or off. Amplification is a little more complicated. It is the ability of a device to receive a small signal (or current) and amplify it while retaining its electrical characteristics.

Vacuum tubes suffer from a number of drawbacks. They are bulky and prone to loose connections and vacuum leaks, they are fragile, they

Size, ft	30 × 50
Weight, tons	30
Vacuum Tubes	18,000
Resistors	70,000
Capacitors	10,000
Switches	6000
Power Requirements, W	150,000
Cost (in 1940)	$400,000

Figure 1.1 ENIAC statistics. *(Source:* Foundations of Computector Technology, *J. G. Giarratano, Howard W. Sams & Co., Indianapolis, IN, 1983.)*

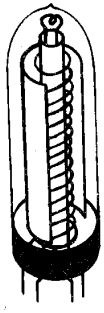


Figure 1.2 Vacuum tube.

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require relatively large amounts of power to operate, and their elements deteriorate rather rapidly. One of the major drawbacks to the ENIAC and other tube-based computers was a limited operating time due to tube burn-out. However, the world did not recognize the potential of computers early on. IBM Chairman, Thomas Watson, in 1943, ventured that, "I think there is a worldwide market for maybe five computers."

These problems were the impetus leading many laboratories around the country to seek a replacement for the vacuum tube. That effort came to fruition on December 23, 1947, when three Bell Lab scientists demonstrated an electrical amplifier formed from the semiconducting material germanium (Fig. 1.3).

This device offered the electrical functioning of a vacuum tube but added the advantages of being solid state (no vacuum), being small and lightweight, and having low power requirements and long lifetime. First named a *transfer resistor,* the new device soon became known as the *transistor.*

The three scientists, John Bardeen, Walter Brattin, and William Shockley were awarded the 1956 Nobel Prize in physics for their invention.

The Solid-State Era

That first transistor was a far distance from the high-density integrated circuits of today. But it was the component that gave birth to the solid-state electronics era with all its famous progeny. Besides transistors, solid-state technology is also used to create diodes, resistors, and capacitors. Diodes are two-element devices that function in a circuit as an on/off switch. Resistors are monoelements devices that serve to limit current flow. Capacitors are two-element devices that store charge in a circuit. In some integrated circuits, the technology is used to create fuses. Refer to Chapter 14 for an explanation of these concepts and an explanation of how these devices work.

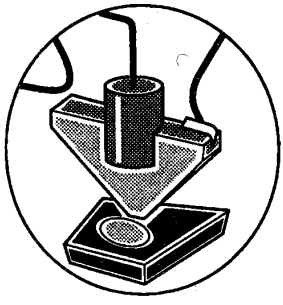


Figure 1.3 The first transistor.

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These devices, containing only one device per chip, are called *discrete* devices (Fig. 1.4). Most discrete devices have less-demanding operational and fabrication requirements than integrated circuits. In general, discrete devices are not considered leading-edge products. Yet, they are required in most sophisticated electronic systems. In 1998, they accounted for 12 percent of the dollar volume of all semiconductor devices sold.[2] The semiconductor industry was in full swing by the early 1950s, supplying devices for transistor radios and transistor based computers.

Integrated Circuits (ICs)

The dominance of discrete devices in solid-state circuits came to an end in 1959. In that year, Jack Kilby, a new engineer at Texas Instruments in Dallas, Texas, formed a complete circuit on a single piece of the semiconducting material germanium. His invention combined several transistors, diodes, and capacitors (five components total) and used the natural resistance of the germanium chip (called a *bar* by Texas Instruments) as a circuit resistor. This invention was the *integrated circuit*, the first successful integration of a complete circuit in and on the same piece of a semiconducting substrate.

The Kilby circuit did not have the form that is prevalent today. It took Robert Noyce, then at Fairchild Camera, to furnish the final piece of the puzzle. In Fig. 1.5 is a drawing of the Kilby circuit. Note that the devices are connected with individual wires.

Earlier, Jean Horni, also at Fairchild Camera, had developed a process of forming electrical junctions in the surface of a chip to create a solid-state transistor with a flat profile (Fig. 1.6). The flattened profile was the outcome of taking advantage of the easily formed natural oxide of silicon, which also happened to be a dielectric (electrical insulator). Horni's transistor used a layer of evaporated aluminum, that was patterned into the proper shape, to serve as wiring for the device. This technique is called *planar technology.* Noyce applied this technique to

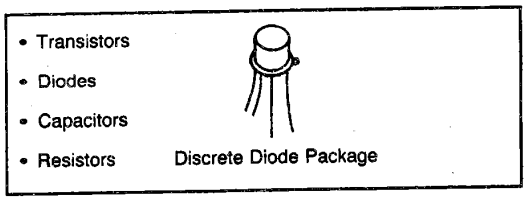


Figure 1.4 Solid-state discrete devices.

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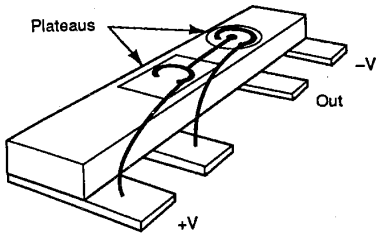


Figure 1.5 Kilby integrated circuit from his notebook.

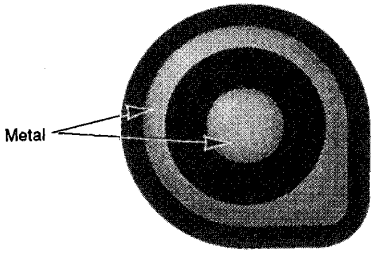


Figure 1.6 Horni "teardrop" transistor.

"wire" together the individual devices previously formed in the silicon wafer surface (Fig. 1.7).

The Noyce integrated circuit became *the* model for all integrated circuits. The techniques used not only met the needs of that era, but contained the seeds for all the miniaturization and cost-effective manufacturing that still drives the industry. Kilby and Noyce shared the patent for the integrated circuit.

Process and Product Trends

Since 1947, the semiconductor industry has seen the continuous development of new and improved processes. These process improvements have in turn led to the more highly integrated and reliable circuits that have, in their turn, fueled the continuing electronics revolution. These process improvements fall into two broad categories: process and structure. Process improvements are those that allow the fabrication of the devices and circuits in smaller dimensions, in ever higher density, quantity, and reliability. The structure improvements are the invention of new device designs allowing greater circuit performance, power control, and reliability.

Device component size and the number of components in an IC are the two common trackers of IC development. Component dimensions are characterized by the smallest dimension in the design. This is

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NOYCE PATENT U.S. PATENT No. 2,981,877

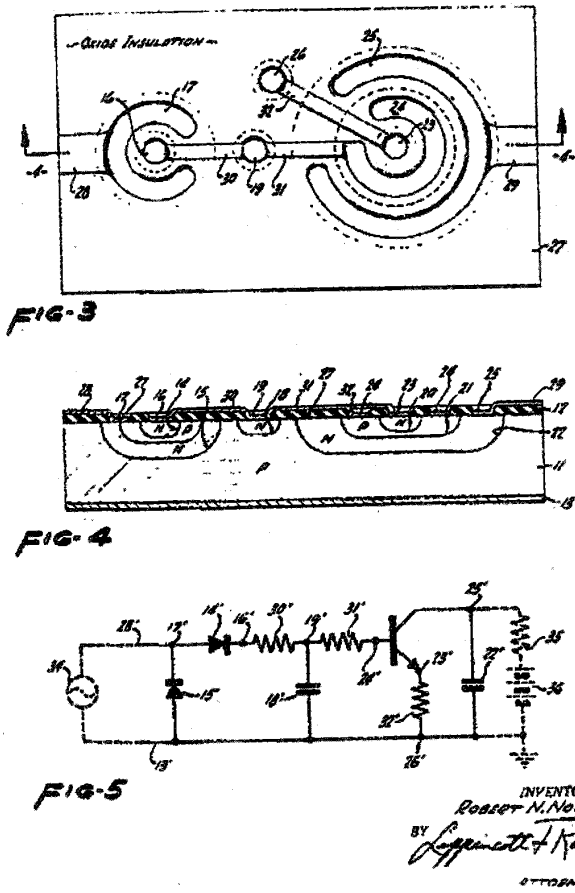


Figure 1.7 Noyce IC patent. *(Courtesy of* Semiconductor Reliability News, *June 2003.)*

called the *feature size* and is usually expressed in microns or nanometers. A micron is 1/1,000,000 of a meter or about 1/100 the diameter of a human hair. A nanometer is 1/1,000,000,000 of a meter. A more specific tracker of semiconductor devices is *gate width.* Transistors are composed of three parts, one of which acts to allow the passage of cur-

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rent. In today's technology, the most popular transistor is the metal-oxide-semiconductor (MOS) structure. The controlling part is called the *gate*. Smaller gate widths drive the industry by producing smaller and faster transistors and more dense circuits. Currently, the industry is driving to the 90-nm gate width, with projections in the *International Technology Roadmap* for semiconductors projecting 22 nm size in 2016.[3]

In 1965, Gordon Moore, a founder of Intel, noted that the number of transistors on a chip were doubling every 18 months. He published the observation, which was immediately dubbed *Moore's law.* Industry observers have used this law to predict the future density of chips. Over the years, it has proven very accurate and now drives technical advances (Fig. 1.8). It is the basis of the *International Technology Roadmap for Semiconductors,* developed by the Semiconductor Industry Association.

Circuit density is tracked by the *integration level,* which is the number of components in a circuit. Integration levels (Fig. 1.9) range from small scale integration (SSI) to ultra large scale integration (ULSI). ULSI chips are sometimes referred to as very very large scale integration (VVLSI). The popular press calls these newest products *megachips.*

Year	Transistor count
1978	29,000
1982	275,000
1985	1,200,000
1991	3,100,000
1993	7,500,000
1997	9,500,000
2001	55,000,000

Figure 1.8 *Source: Intel Corporation.*

Level	Abbreviation	# Components per Chip
Small Scale Integration	SSI	2 - 50
Medium Scale Integration	MSI	50 - 5000
Large Scale Integration	LSI	5000 - 100,000
Very Large Scale Integration	VLSI	Over 100,000 - 1,000,000
Ultra Large Scale Integration	ULSI	> 1,000,000

Figure 1.9 IC integration table.

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In addition to the integration scale, memory circuits are identified by the number of memory bits contained in the circuit (a four-meg memory chip can store four million bits of memory). Logic circuits are often rated by their number of "gates." A gate is the basic operational component of a logic circuit.

Decreasing feature size

The journey from small scale integration to today's megachips has been driven primarily by reductions in the feature size of the individual components. This decrease has been brought about by dramatic increases in the imaging process, known as lithography, and the trend to multiple layers of conductors. Actual and projected feature sizes are shown in Fig. 1.10. The Semiconductor Industry Association (SIA) has projected feature sizes decreasing to 22 nm (0.0022 μm) by the year 2016.[3] Along with the ability to make components on the chip smaller comes the benefit of crowding them closer together, further increasing density.

An analogy used to explain these trends is the layout of a neighborhood of single-family homes. The density of the neighborhood is a function of the house size, lot size, and the width of the streets. Accommodating a higher population could come by increasing size of the neighborhood (increasing the chip area). Another possibility is to reduce the size of the individual houses and place them on smaller lots. We can also reduce the street size to increase density. However, at some point, the streets cannot be reduced anymore in size or they won't be wide enough for autos. Furthermore, at some point, the houses cannot be further reduced in size and still function as dwelling units. At this point, an option is to build up by building multidecked freeways and/or replacing individual homes with apartment buildings. All of these concepts are used in semiconductor technology.

Year	DRAM pitch (nm)
2001	130
2004	90
2007	65
2010	45
2013	32
2016	22

Figure 1.10 Lithography DRAM pitch size. *(Source: SIA,* International Technology Roadmap for Semiconductors.)

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There are several benefits to the reduction of the feature size and its attendant increase in circuit density. At the circuit performance level, there is an increase in circuit speed. With less distances to travel and with the individual devices occupying less space, information can be put into and gotten out of the chip in less time. Anyone who has waited for their personal computer to perform a simple operation can appreciate the effect of faster performance. These same density improvements result in a chip or circuit that requires less power to operate. The small power station required to run the ENIAC has given way to powerful lap top computers that run on a set of batteries.

Increasing chip and wafer size

The advancement of chip density from the SSI level to ULSI chips has driven larger chip sizes. Discrete and SSI chips average about 100 mils (0.1 in) on a side. ULSI chips are in the 500 to 1000 mil (0.5 to 1.0 in) per side, or larger, range. ICs are manufactured on thin disks of silicon (or other semiconductor material, see Chapter 2) called *wafers*. Placing square or rectangular chips on a round wafer leaves unavailable areas around the edge (see Fig. 6.6). These unavailable areas can become large as the chip size increases (Fig. 1.11). The desire to offset the loss of usable silicon has driven the industry to larger wafers. As the chip size increases, the 1-in diameter wafers of the 1960s have given way to 200- and 300-mm (8-in and 12-in) sized wafers. Production efficiency increases, because the area of a circle increases as the mathematical square of the radius. Thus, doubling the wafer diameter from 6 to 12 in increases the area available for chip fabrication by four times.

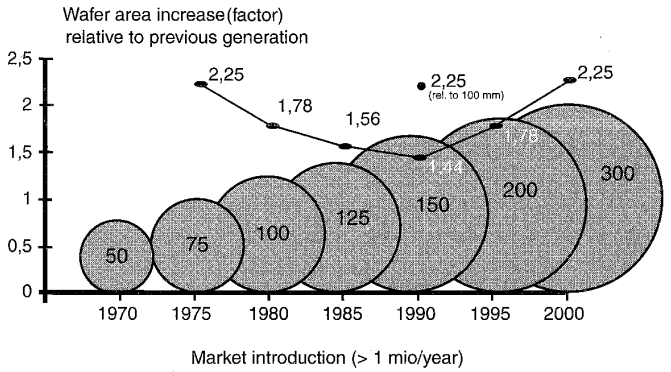


Figure 1.11 Wafer size history. *(Courtesy of Future Fab International.)*

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Reduction in defect density

As feature sizes have decreased, the need for reduced defect density and defect size on the chips (and in the manufacturing process) has become critical. A 1-micron piece of dirt on a 100-micron sized transistor may not be a problem. On a one-micron sized transistor, it becomes a killer defect that can render the component inoperable (Fig. 1.12). Contamination control needs has driven the cost of building an IC manufacturing facility into the multibillion dollar range.

Increase in interconnection levels

The component density increase has led to a "wiring" problem. In the neighborhood analogy, reducing street widths was one strategy to increase density. But, at some point, the streets become too narrow to allow cars to travel. The same thing happens in IC design. The increased component density and close packing rob the surface space needed on the surface to connect the components. The solution is multiple levels of "wiring" stacked (Fig. 1.13) above the surface components in layers of insulators and conducting layers (Chapter 13).

The SIA roadmap

These major IC parameters are interrelated. Moore's law predicts the future of component density, which triggers the calculation of the integration level (component density), chip size, defect density (and size), and the number of interconnection levels required. The Semiconductor Industry Association has made these projections into the future in a series of "roadmaps" covering these and other critical device and production parameters (Fig. 1.14).

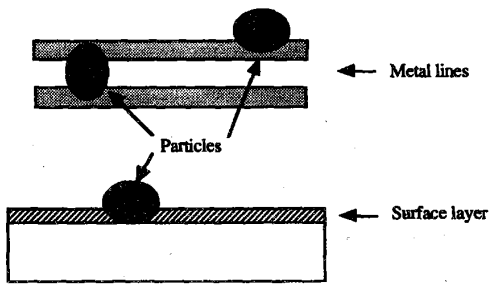


Figure 1.12 Relative size of airborne particles and wafer dimensions.

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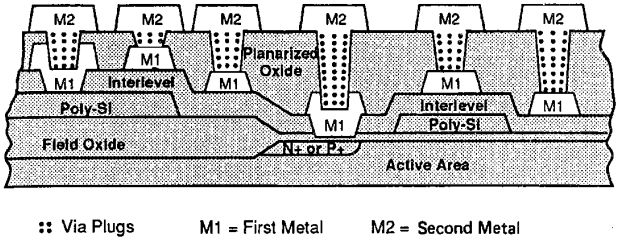


Figure 1.13 Cross section of typical planarized two-level metal VLI structure showing range of via depths after planarization. (*Courtesy of* Solid State Technology.)

Year of Production	2001	2006	2012
Line width (nm)	150	100	50
Memory size	1 Gb	16Gb	64 Gb
Logic Bits/cm^2	380M	2.2B	17B
Chip Size-DRAM (mm^2)	445	790	1580
Max wiring levels	7	7-8	9
Mask layers	23	24/26	28
Defect density-DRAM (D/m)	875	490	250
Chip conections-I/Os	1195	1970	3585
Wafer diameter (mm)	300	300	450

Figure 1.14 Projection of wafer and chip parameters.

Chip cost

Perhaps the most significant effect of these process and product improvements is the cost of the chips. Figure 1.15 shows the year-by-

Year	Transistor cost ($)
1986	1.00
1972	0.01
1976	0.001
1985	0.0001
1992	0.00001
2000	0.000001

Figure 1.15 Declining transistor cost. *(Source: Intel Corporation.)*

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year drop in transistors through the 1990s. The reductions are typical for any maturing product. Prices start high and, as the technology is mastered and manufacturing efficiencies increase, the prices drop and eventually become stable. These chip prices have constantly declined even as the performance of the chips has increased. In its first 30 years, the semiconductor industry had 2 to 5 times the economic impact in the U.S. that the railroads had in a similar period.[4] The factors affecting chip cost are discussed in Chapter 15.

The two factors, increased performance and less cost, have driven the explosion of products using solid-state electronics. By the 1990s, an auto had more computing power on-board than the first lunar space shots. Even more impressive is the personal computer. Today, for a moderate price, a desktop computer can deliver more power than a IBM mainframe manufactured in 1970. Major industry use of chips is shown in Fig. 1.16. By 2008, the global chip industry will be producing a billion transistors per person worldwide.[5]

Semiconductor industry growth

Overall, the semiconductor industry has experienced worldwide continuous growth. From its birth in the 1950s, it has grown to worldwide sales of over $200 billion dollars a year, supported by a supplier industry of over $30 billion.[6] The millions of chips are supplied by factories located throughout the world. Interestingly, even as the industry shows signs of maturing, it is still growing faster than other "mature" industries, indicating that microchips still have a lot of growth potential (Fig. 1.17).

An example of increasing chip power is shown in Fig. 1.18, which indicates the number of volumes of the *Encyclopaedia Britannica* that can be stored on larger capacity DRAM memory chips.

The history of the semiconductor industry is one of continual developments and advances emerging to world dominance in the mid-

CHIP USES	1996
Computer	48.0%
Consumer	21.2%
Telecom	14.7%
Industrial	9.8%
Automotive	4.4%
Military	1.9%
Total	100.0%

Figure 1.16 Semiconductor chip uses. *(Courtesy of In-Stat-1995 SEMI ISS seminary.))*

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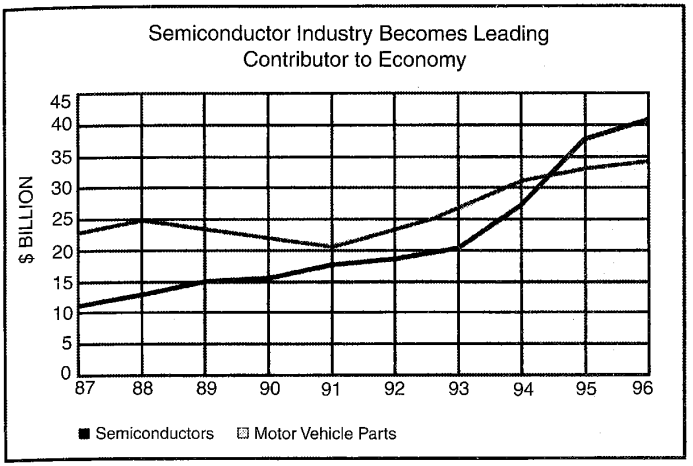


Figure 1.17 Semiconductor and vehicle parts growth. *(Courtesy Semiconductor Industry Association.)*

Year	1993	1996	1999	2002	2005
DRAM Capacity	16Mb	64Mb	256Mb	1Gb	4Gb
Feature Size (micron)	0.5	0.35	0.25	0.18	0.08
Volumes of Enc. Britannics	1/4/ Vol	1 Vol.	4 Vol.	16 Vol.	2 Sets

Figure 1.18 Future DRAM capacity. *(Source:* Business Week, *July 1994.)*

1990s. In that year, the semiconductor industry became the nation's leading value added industry, outperforming the auto industry (Fig. 1.19).

Industry Organization

The electronics industry is divided into two major segments: semiconductors and systems (or products). "Semiconductors" encompasses the material suppliers, circuit design, chip manufacturers, and all of the equipment and chemical suppliers to the industry. The systems segment encompasses the industry that designs and produces the vast number of semiconductor device based products, from consumer electronics to space shuttles. The electronics industry includes the manufacturers of printed circuit boards.

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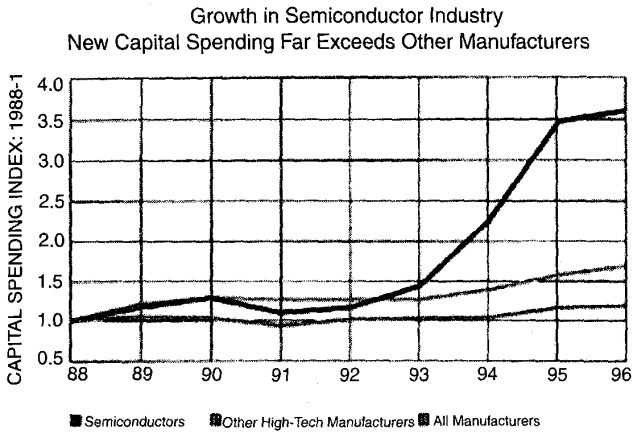


Figure 1.19 Growth of semiconductor industry capital spending. *(Courtesy Semiconductor Industry Association.)*

The semiconductor segment is composed of two major subsegments. One is the firms that actually make the semiconductor solid-state devices and circuits. The manufacturing process is named *wafer fabrication.* Within this segment there are three types of chip suppliers. Integrated device manufacturers (IDMs) design, manufacture, package, and market chips. Foundry companies build circuit chips for other chip suppliers. Waferless (or fabless) companies design and market chips, buying finished chips from chip foundries. Chips are fabricated by both merchant and captive producers. Merchant suppliers manufacture just chips and sell them on the open market. Captive suppliers are firms whose final product is a computer, communications system, or other product, and they produce chips in house for their own products. Some firms produce chips for in-house use and also sell on the open market, and others produce specialty chips in house and buy others on the open market. Since the 1980s, the trend has been to a greater percentage of chips being fabricated in captive fab areas.

Stages of Manufacturing

Solid-state devices are manufactured in the following five distinct stages (Fig. 1.20):

1. Material preparation
2. Crystal growth and wafer preparation
3. Wafer fabrication and sort

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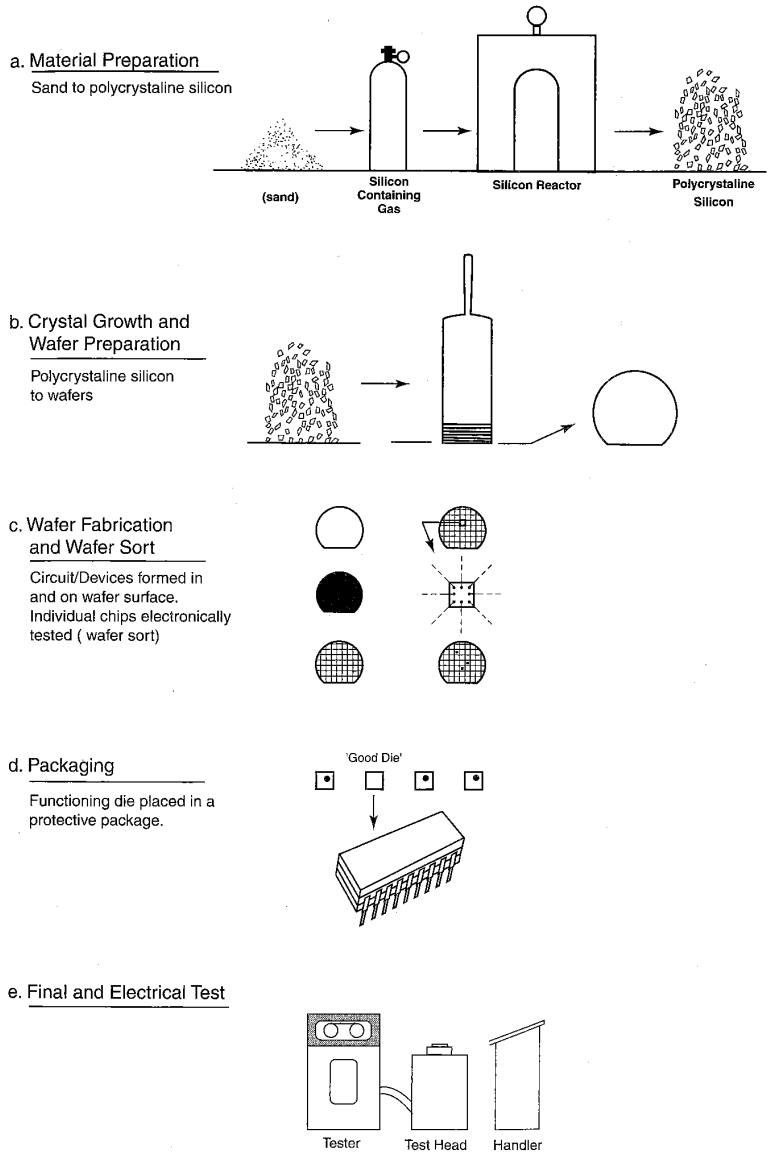


Figure 1.20 Stages of semiconductor production.

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4. Packaging
5. Final and electrical test

In the first stage, material preparation (see Chapter 2), the raw semiconducting materials are mined and purified to meet semiconductor standards. For silicon, the starting material is sand, which is converted to pure silicon with a polysilicon structure (Fig. 1.20*a*).

In stage two, the material is formed into a crystal with specific electrical and structural parameters. Next, thin disks called *wafers* are cut from the crystal and surface treated (Fig. 1.20*b*) in a process called crystal growth and wafer preparation (see Chapter 3). The industry also makes devices and circuits from germanium and compounds of different semiconductor materials.

In stage three (Fig. 1.20*c*), wafer fabrication, the devices or integrated circuits are actually formed in and on the wafer surface. Up to several thousand identical devices can be formed on each wafer, although two to three hundred is a more common number. The area on the wafer occupied by each discrete device or integrated circuit is called a *chip* or *die*. The wafer fabrication process is also called fabrication, fab, chip fabrication, or microchip fabrication. While a wafer fabrication operation may take several thousand individual steps, there are two major activities. In the front end of the line (FEOL), the transistors and other devices are formed in the wafer surface. In the back end of the line (BEOL), the devices are wired together with metallization processes, and the circuit is protected with a final sealing layer.

Following wafer fabrication, the devices or circuits on the wafer are complete, but untested and still in wafer form. Next comes an electrical test (called *wafer sort*) of every chip to identify those that meet customer specifications. Wafer sort may be the last step in the wafer fabrication or the first step in the *packaging* process.

Packaging (Fig. 1.20*d*) is the series of processes that separate the wafer into individual die and place them into protective packages. This stage also includes final testing of the chip for conformance to customer specifications. The industry also refers to this stage as *assembly and test* (A/T). A protective chip package is necessary to protect the chip from contamination and abuse, and to provide a durable and substantial electrical lead system to allow connection of the chip onto a printed circuit board or directly into an electronic product. Packaging takes place in a different department of the semiconductor producer and quite often in a foreign plant.

The vast majority of chips are packaged in individual packages. But a growing percentage are being incorporated into hybrid circuits, in multichip modules (MCMs), or mounted directly on printed circuit

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boards (chip-on-board, COB). An integrated circuit is an electrical circuit formed entirely by semiconductor technology on a single chip. A hybrid circuit combines semiconductor devices (discretes and ICs) with thick or thin film resistors and conductors and other electrical components on a ceramic substrate. These techniques are explained in Chapter 18.

The Junction Transistor

While the tremendous advantages of solid-state electronics was recognized early on, the advancements possible from miniaturization were not realized until two decades later. During the 1950s, engineers set to work and defined many of the basic processes and materials still used today.

The structure that makes semiconductor devices function is the *junction* (Fig. 1.21). It is formed by creating a structure that is rich in electrons (negative polarity or *N-type*) next to a region rich in *holes* (locations with missing electrons that act electrically positive or *P-type*) (see Chapter 11).

A transistor requires two junctions to work (see Chapter 16). Early commercial transistors were of the bipolar type (see Chapter 14), which dominated production well into the 1970s. The term *bipolar* refers to a transistor structure that operates on both negative and positive currents. The other major method of building a solid-state transistor is the *field effect transistor* (FET). William Shockley published the operational basics of a FET in 1951. These transistors operate with only one type of current and are also called *unipolar devices.* The FET came to the marketplace in volume in a structure known as the *metal oxide semiconductor* (MOS) transistor.

William Shockley and Bell Labs get much of the credit for the spread of semiconductor technology. Shockley left Bell Labs in 1955 and formed Shockley Laboratories in Palo Alto, California. While his company did not survive, it established semiconductor manufacturing on the West Coast and provided the beginning of what eventually became known as Silicon Valley. Bell Labs helped the fledgling industry with the decision to license its semiconductor discoveries to a host of companies.

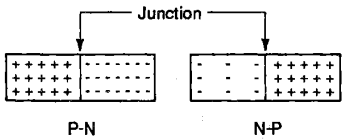


Figure 1.21 P-N and N-P junctions.

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The early semiconductor devices were made in the material germanium. Texas instruments changed that trend with the introduction of the first silicon transistor in 1954. The issue over which material would dominate was settled in 1956 and 1957 by two more developments from Bell Labs: diffused junctions and oxide masking.

It was the development of oxide masking that ushered in the "silicon age." Silicon dioxide (SiO_2) grows uniformly on silicon and has a similar index of expansion, which allows high-temperature processing without warping. Silicon dioxide is a dielectric material, which allows it to function on the silicon surface as an insulator. Additionally, SiO_2 is an effective block to the dopants that form the N and P regions in silicon.

The net effect of these advances was planar technology (Fig. 1.22), introduced by Fairchild Camera in 1960. With the above-named techniques, it was possible to form (diffusion) and protect (silicon dioxide) junctions during and after the wafer fabrication process. Also, the development of oxide masking allowed two junctions to be formed through the top surface of the wafer (Fig. 1.22); that is, in one *plane.* It was this process that set the stage for the development of thin film wiring.

Bell Labs conceived of forming transistors in a high purity layer of semiconducting material deposited on top of the wafer (Fig. 1.23). Called an *epitaxial layer,* this discovery allowed higher speed devices and provided a scheme for the closer packing of components in a bipolar circuit.

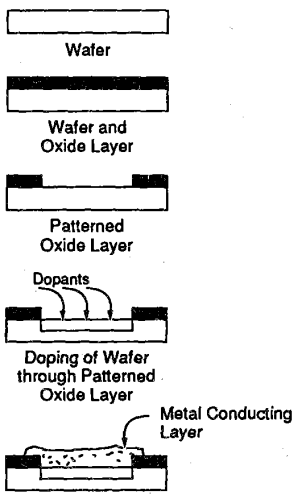


Figure 1.22 Basics of silicon planar processing.

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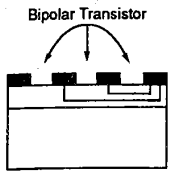


Figure 1.23 Double diffused bipolar transistor formed in epitaxial layer.

The 1950s was indeed the golden age of semiconductor development. During this incredibly short time, most of the basic processes and materials were discovered. The decade opened with the knowledge of how to manufacture small volumes of crude devices in germanium and ended with the first integrated circuit and silicon firmly established as the semiconductor of the future.

Five Decades of Industry Development

In the 1950s, basic and crude products and processes launched an industry that has grown into a major world manufacturing sector. The 1960s was the decade the industry started growing into a sophisticated industry, driven by new products that demanded new fabrication processes, which demanded new materials and new production equipment. The chip price erosion trend of the industry, well established in the 1950s, also was an industry driver.

Technology spread as engineers changed companies in the industry clusters in Silicon Valley, Route 128 around Boston, and in Texas. By the 1960s, the number of fab areas had grown sufficiently, and processes were approaching a level of commonalty that attracted semiconductor specialty suppliers.

On the company front, many of the key players of the 1950s formed new companies. Robert Noyce left Fairchild to found Intel (with Andrew Grove and Gordon Moore), and Charles Sporck also left Fairchild to grow National Semiconductor into a major player. Signetics became the first company dedicated exclusively to the fabrication of ICs. New device designs were the usual driver of start-up companies. However, the ever present price erosion was a cruel trend that drove both established and new companies out of business.

Price dropping was accelerated by the development of a plastic package for silicon devices in 1963. Also in that year, RCA announced the development of the *insulated field effect transistor* (IFET), which paved the way for the MOS industry. RCA also pioneered the first complementary MOS (CMOS) circuits.

At the start of the 1970s, the industry was manufacturing ICs primarily at the MSI level. The move to profitable, high-yield LSI devices

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was being somewhat hampered by mask-caused defects and the damage inflicted on the wafers by the contact aligners. The mask and aligner defect problem was solved with the development of the first practical projection aligner by Perkin and Elmer Company.

The decade also saw the improvement of cleanroom construction and operation, the introduction of ion implantation machines, and the use of e-beam machines for high-quality mask generation, and mask steppers began to show in fab areas for wafer imaging.

Automation of processes started with spin/bake and develop/bake systems. The move from operator control to automatic control of the processes increased both wafer throughput and uniformity.[20]

Once the processes were integrated into the equipment, the stage was set for dissemination throughout the world. Along with the process improvements came a more detailed understanding of the physics of solid-state devices, which allowed the mastering of the technology by student engineers worldwide.

The focus in the 1980s was automation of all phases of wafer fabrication and packaging and elimination of operators from the fab areas. Automation increases manufacturing efficiency, minimizes processing errors, and keeps the wafer fabrication areas cleaner by limiting the number of operators, who are one of the major sources of contamination in the process. These issues are examined in more detail in Chapter 4.

One feature of automation is flexibility. As in automobile industry automation, especially in the area of design, manufacturers began to design more complicated chips. The new designs, in turn, presented new manufacturing challenges that led to the development of new processes. At these sophisticated levels, machine automation is required to achieve the process control and repeatability.

The 1980s started with American and European dominance and ended as a worldwide industry. Through the 1970s and 1980s, the one-micron feature size barrier loomed as both opportunity and challenge. The opportunity was a new era of megachips with vastly increased speeds and memory. The challenge was the limitations of conventional lithography, additional layers, more step height variation on the wafer surface, and increasing wafer diameters, to mention a few. The one-micron barrier was crossed in the early 1990s when 50 percent[7] of microchip fabrication lines were working at the micron or submicron level.

The industry matured into more traditional focuses on manufacturing and marketing issues. Early on, the profit strategy was to ride the innovation curve. That meant always being first (or close to first) with the latest and greatest chip that could be sold with enough profit to pay for the R&D and finance new designs. The profit potential of this

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strategy overcame manufacturing yield problems and lower efficiencies. The spread of the technology (competition) and improvements in process control, however, moved the industry to greater emphasis on the production issues. The primarily productivity factors are automation, cost control, process characterization and control, and worker efficiency.

Strategies to control the cost have included detailed analysis of equipment cost of ownership, new fab layouts (such as cluster tools), robotic automation, wafer isolation technology (WIT), computer integrated manufacturing (CIM), sophisticated statistical process control, advanced metrology instruments, just-in-time inventory schemes, and others (see Chapter 15).

Technical driving factors (feature size reduction, wafer diameter increases, and yield improvement) all have physical or statistical limits. But productivity improvement, which incorporates many factors (see Chapter 15), is the source of continuing profit. The pressures are enormous.

Wafer fab facilities are in the gigabuck ($2 to 3 billion and increasing) level, and equipment and process development are equally expensive. Manufacturing chips with features sizes below 0.35 microns will require extensive and expensive development of conventional lithography or X-ray and deep UV (DUV) lithography.

The challenge of the *SIA Roadmap* (IRTS) is that many of the processes required to produce the next generations of chips are unknown or in very primitive states of development. However, the good news is that the industry is moving forward along an evolutionary curve rather than relying on revolutionary breakthroughs. Engineers are wringing every bit of productivity out of the processes before looking for a big technology jump to solve problems. This is another sign of a maturing industry.

Perhaps the major technological change of the decade was copper wiring. Aluminum wiring ran into limitations in several areas, notably in contact resistance with silicon. Copper has always been a better conductor but was difficult to deposit and pattern. It was also a killer of circuit operation if it got into the silicon. IBM[8] developed usable copper processes (Chapters 10 and 13), which gained almost instant acceptance for wiring together advanced chips.

The Nano Era

Microtechnology in the popular sense means "small." In the science world, it refers to one-billionth. Thus, feature sizes and gate widths are expressed in microns (micrometers), as in 0.018 μm. It is becoming

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more common to use nanometers (1×10^{-9} meters), thus making the above gate width 180 nm (Fig. 1.24).[9]

The way to the nano future is sketched out in the Semiconductor Industry Association's *International Technology Roadmap for Semiconductors* (*ITRS*). Gate widths of 22 nm or less are predicted by 2016. At these levels, the operational parts of devices consist of only a few atoms or molecules.

Getting there will not be easy. There is a predictable train of events that happen as devices are scaled to smaller dimensions. Advantages are faster operating transistors and higher-density chips. However, smaller dimensions require more sophisticated processes and equipment.

A gate area is the critical working part of an MOS transistor. Smaller gates are more vulnerable to contamination, which drives the development of cleaner chemicals and processes. Detecting lower levels of contamination requires more sensitive measurement techniques.

Surface roughness becomes a parameter requiring control. As the devices get closer together, they drive the need for a superstructure of metallization layers stacked on top of the surface. These put pressure on planarization techniques to keep the surfaces flat enough to allow patterning. More metallization layers bring with them higher electrical resistances, which drive the need for new metallization materials, such as copper. As the number of electrical functions on a chip increases, so does the internal temperature, driving the need for heat dissipation techniques.

All of these advances will have to take place in ever cleaner wafer fabrication facilities with super-clean materials and chemicals and with process tools clustered to minimize exposure to contamination and to increase process efficiency.

Wafer diameters will move into the 450+ mm range, and factory automation will be at the tool-to-tool level with on-board process moni-

	Meters (m)
Meter (m)	1
Centimeter (cm)	1/100
Millimeter (mm)	1/1,000
Micrometer (micron) (μm)	1/1,000,000
Nanometer (nm)	1/1,000,000,000
Angstrom (Å)	1/10,000,000,000

Figure 1.24 Comparative length units.

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toring. More processes at higher levels of detail will require higher-volume wafer fabrication plants with more sophisticated process automation and factory management. Price tags for these mega-plants are headed to the $10 billion level.[10] This level of investment will pressure faster R&D activities and quick factory startups.

By 2016, the industry and circuits will be far different from what they are now, and the industry will be near the end of the basic physics of silicon transistors. Post-silicon production materials have yet to be identified, but the industry will grow. Not all IC uses have to be state of the art. It is unlikely that toasters, refrigerators, and automobiles will require cutting-edge devices. New base materials are in R&D labs. Compound semiconductors, such as gallium arsenide (GaAs) are candidates. Technologies such as molecular beam epitaxy (MBE) (Chapter 12) may be employed to build entirely new materials one atom at a time.

Another use of the term "nano" is a new way to build very small structures, called *nanotechnology*. It is based on the discovery of a structure of carbon flat crystals shaped like a hollow tube (*nanotube*). These structures have promise for a number of uses. In semiconductor technology, it appears that these nets of carbon atoms can be doped to act as electronic devices and, eventually, electronic circuits.

It is safe to say that the semiconductor industry will continue to be the dominant industry as it continues to push the limits of material and manufacturing technology. It is also safe to predict that the use of ICs will continue to shape our world in ways yet unknown.

Review Questions

1. List the four types of discrete devices.
2. Describe the advantages of solid-state devices over vacuum tubes.
3. A VLSI circuit has more components than a ULSI circuit (true or false).
4. Describe the difference between a hybrid and integrated circuit.
5. State the stage of processing in which wafers are produced.
6. State the stage of processing that processes "chips."
7. Describe an N-P junction.
8. Describe what is meant by the term "feature size."
9. List three trends that have driven the semiconductor industry.
10. Describe the functions of a semiconductor package.

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Chapter

2

Properties of Semiconductor Materials and Chemicals

Overview

Semiconductor materials possess electrical and physical properties that allow the unique functions of semiconductor devices and circuits. These properties are examined along with the basics of atoms, electrical classification of solids, and intrinsic and doped semiconductors.

Wafer fabrication is a long series of steps that include many cleaning operations using ordinary and specialty chemicals. The basic properties of gases, acids, bases, and solvents are discussed.

Objectives

Upon completion of this chapter, you should be able to:

1. Identify the parts of an atom.
2. Name the two unique properties of a doped semiconductor.
3. List at least three semiconducting materials.
4. Explain the advantages and disadvantages of gallium arsenide compared with silicon.
5. Explain the difference in composition and electrical functioning of N- and P-type semiconducting materials.
6. Describe the properties of resistivity and resistance.
7. Identify the differences between acids, alkalis, and solvents.
8. List the four states of nature.

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9. Give the definition of an atom, a molecule, and an ion.
10. Explain four or more basic chemical handling safety rules.

Atomic Structure

The Bohr atom

The understanding of semiconductor materials requires a basic knowledge of atomic structure.

Atoms are the building blocks of the physical universe. Everything in the universe (as far as we know) is made from the 96 stable materials and 12 unstable ones known as *elements*. Each element has a different atomic structure. The different structures give rise to the different properties of the elements.

The unique properties of gold are due to its atomic structure. If a piece of gold is divided into smaller and smaller pieces, one eventually arrives at the last piece that exhibits the properties of gold. That last piece is the atom.

Dividing that last piece further will yield the three parts that compose individual atoms. They are called the *subatomic particles.* These are *protons, neutrons,* and *electrons*. Each of these subatomic particles has its own properties. A particular combination and structure of the subatomic particles are required to form the gold atom. The basic structure of the atom most used to understand physical, chemical, and electrical differences between different elements was first proposed by the famous physicist Niels Bohr (Fig. 2.1).

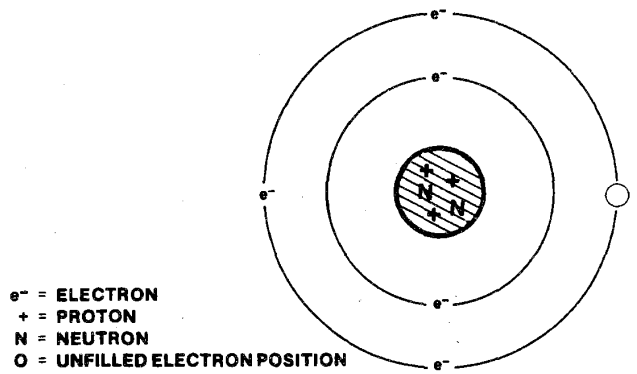


Figure 2.1 Bohr atom model.

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The Bohr atom model has the positively charged protons and neutral neutrons located together in the nucleus of the atom. The negatively charged electrons move in defined orbits about the nucleus, similar to the movement of the planets about the sun. There is an attractive force between the positively charged protons and the negatively charged electrons. However, this force is balanced by the outward centrifugal force of the electrons moving in their orbits. The net result is a structurally stable atomic structure.

Each orbit has a maximum number of positions available for electrons. In some atoms, not all of the positions are filled, leaving a "hole" in the structure. When a particular electron orbit is filled to the maximum, additional electrons must go into the next outer orbit.

The Periodic Table of the Elements

The elements differ from each other in the number of electrons, protons, and neutrons in their atoms. Fortunately, nature combines the subatomic particles in an orderly fashion. An examination of some of the rules governing atomic structure is helpful in understanding the properties of semiconducting materials and process chemicals. Atoms (and therefore the elements) range from the simplest, hydrogen (with one electron) to the most complicated one, lawrencium (with 103 electrons).

Hydrogen consists of only one proton in the nucleus and only one electron. This arrangement illustrates the first of the following rules of atomic structure.

1. In each atom, there is an equal number of protons and electrons.
2. Each element contains a specific number of protons, and no two elements have the same number of protons. Hydrogen has one proton in its nucleus, while the oxygen atom has eight.

   This fact leads to the assignment of numbers to each of the elements. Known as the *atomic number*, it is equal to the number of protons (and therefore electrons) in the atom. The basic reference of the elements is the periodic table (Fig. 2.2). The periodic table has a box for each of the elements, which is identified by two letters. The atomic number is in the upper left hand corner of the box. Thus, calcium (Ca) has the atomic number 20, so we know immediately that calcium has 20 protons in its nucleus and 20 electrons in its orbital system.

   Neutrons are electrically neutral particles that, along with the protons, make up the mass of the nucleus.

   Figure 2.3 shows the atomic structure of elements no. 1, hydrogen; no. 3, lithium; and no. 11, sodium. When constructing the dia-

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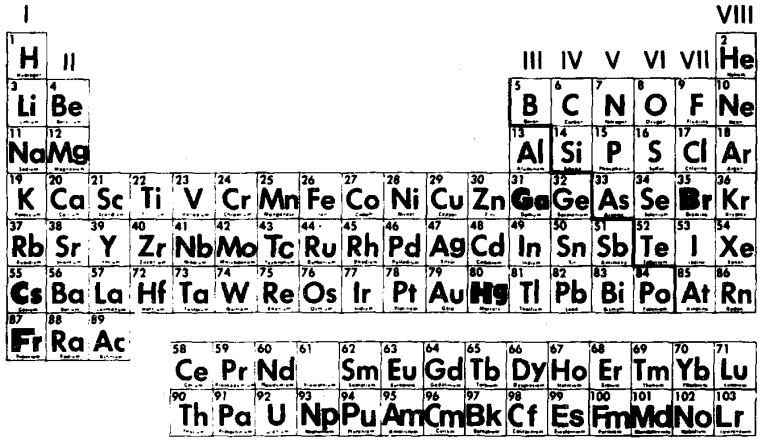


Figure 2.2 Periodic table of the elements.

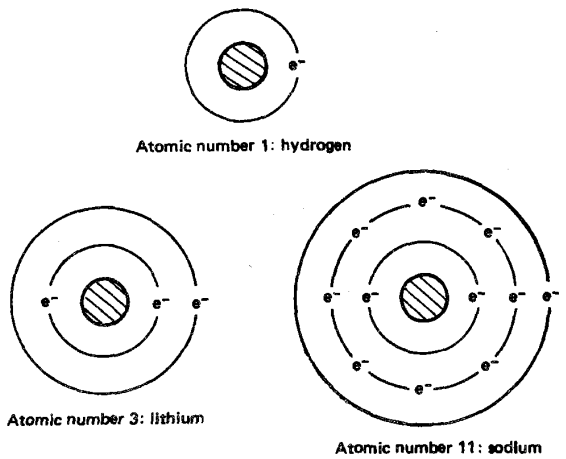


Figure 2.3 Atomic structures of hydrogen, lithium, and sodium.

grams, several rules were observed in the placement of the electrons in their proper orbits. The rule is that each orbit (n) can hold $2n^2$ electrons. Solution of the math for orbit no. 1 dictates that the first electron orbit can hold only two electrons. This rule forces the third electron of lithium into the second ring. The rule limits the number of electrons in the second ring to 8 and that of the third

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ring to 18. So, when constructing the diagram of the sodium atom, with 11 protons and electrons, the first two orbits take up 10 electrons, leaving the 11th in the third ring.

These three atoms have a commonalty. Each has an outer ring with only one electron in it. This illustrates another observable fact of elements.

3. Elements with the same number of outer-orbit electrons have similar properties. This rule is reflected in the periodic table. Note that hydrogen, lithium, and sodium appear on the table in a vertical column labeled with the Roman numeral one (I). The column number represents the number of electrons in the outer ring and all of the elements in each column share similar properties.

   It is no accident that the three of the best electrical conductors (copper, silver, and gold) all appear in the same column (Ib) (Fig. 2.4) of the periodic table.

   There are two more rules of atomic structure relevant to the understanding of semiconductors.

4. Elements are stable with a filled outer ring or with eight electrons in the outer ring. These atoms tend to be more chemically stable than atoms with partially filled rings.

5. Atoms seek to combine with other atoms to create the stable condition of full orbits or eight electrons in their outer ring.

Rules 4 and 5 influence the creation of N- and P-type semiconductor materials, as explained in the section on doped semiconductors.

Electrical Conduction

Conductors

An important property of many materials is the ability to conduct electricity or support an electrical current flow. An electrical current is

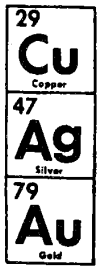


Figure 2.4 The three best electrical conductors.

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simply a flow of electrons. Electrical conduction takes place in elements and materials where the attractive hold of the protons on the outer ring electrons is relatively weak. In such a material, these electrons can be easily moved, which sets up an electrical current. This condition exists in most metals.

The property of materials to conduct electricity is measured by a factor known as *conductivity.* The higher the conductivity, the better the conductor. Conducting ability is also measured by the reciprocal of the conductivity, which is *resistivity.* The lower the resistivity of a material, the better the conducting ability.

$$C = 1/\rho$$

where C = conductivity
ρ = resistivity in ohm-centimeters (Ω-cm)

Dielectrics and Capacitors

At the opposite end of the conductivity scale are materials that exhibit a large attractive force between the nucleus and the orbiting electrons. The net effect is a great deal of resistance to the movement of electrons. These materials are known as *dielectrics.* They have low conductivity and high resistivity. In electrical circuits and products, dielectric materials such as silicon dioxide (glass) are used as insulators.

An electrical device known as a *capacitor* is formed whenever a dielectric layer is sandwiched between two conductors. In semiconductor structures, capacitors are formed in MOS gate structures, between metal layers and silicon substrates separated by dielectric layers, and other structures (see Chapter 16). The practical effect of a capacitor is that it stores electrical charges. Capacitors are used for information storage in memory devices to prevent unwanted charges to build up in conductors and silicon surfaces, and to form the working parts of field effect (MOS) transistors. The capacitance ability of a film is relative to the area and thickness and a property parameter known as the *dielectric constant.* Semiconductor metal conduction systems need high conductivity and, therefore, low-resistance and low-capacitance materials. These are referred to as *low-k dielectrics.* Dielectric layers used as insulators between conducting layers need high capacitances or *high-k dielectrics.*

$$C = \frac{kE_0A}{t}$$

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where C = capacitance
k = dielectric constance of material
E_0 = permittivity of free space (free space has the highest "capacitance")
A = area of capacitor
t = thickness of dielectric material

Resistors

An electrical factor related to the degree of conductivity (and resistivity) of a material is the electrical resistance of a specific volume of the material. The resistance is a factor of the resistivity and dimensions of the material. Resistance to electrical flow is measured in ohms as illustrated in Fig. 2.5.

The formula defines the electrical resistance of a specific volume of a specific material (in this illustration, the volume is a rectangular bar with dimensions X, Y, and Z). The relationship is analogous to density and weight, *density* being a material property and *weight* being the force exerted by a specific volume of the material.

Electric current flow is analogous to water flowing in a hose. For a given hose diameter and water pressure, only a given amount of water will flow out of the hose. The resistance to flow can be reduced by increasing the hose diameter, shortening the hose, and/or increasing the pressure. In an electrical system, the electron flow can be increased by increasing the cross section of the material, shortening the length of the piece, increasing the voltage (analogous to pressure), and/or decreasing the resistivity of the material.

Intrinsic Semiconductors

Semiconducting materials, as the name implies, are materials that have some natural electrical conducting ability. There are two elemental semiconductors (silicon and germanium), and both are found in col-

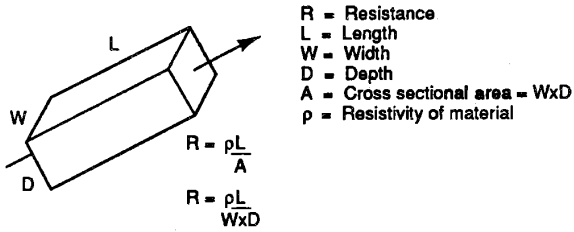


Figure 2.5 Resistance of rectangular bar.

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umn IV (Fig. 2.6) of the periodic table. In addition, there are some tens of material compounds (a compound is a material containing two or more chemically bound elements) that also exhibit semiconducting properties. These compounds come from elements found in columns III and V, such as gallium arsenide, indium gallium phosphide (InGaP), and gallium phosphide (GaP). Others are compounds from elements from columns II and VI of the periodic table.

The term *intrinsic* refers to these materials in their purified state and not contaminated with impurities or dopants purposely added to change properties.

Doped Semiconductors

Semiconducting materials, in their intrinsic state, are not useful in solid-state devices. However, through a process called *doping,* specific elements can be introduced into intrinsic semiconductor materials. These elements increase the conductivity of the intrinsic semiconductor material. The doped material displays two unique properties that *are* the basis of solid-state electronics. The two properties are

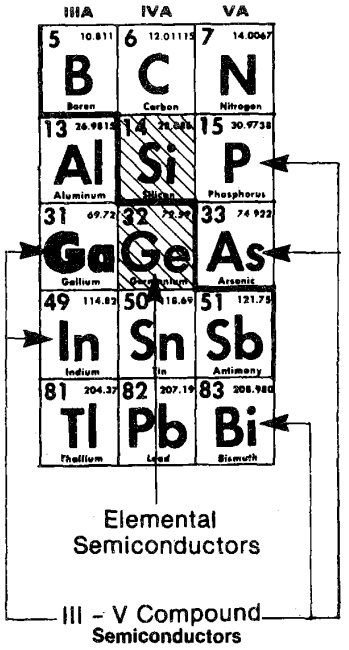


Figure 2.6 Semiconductor materials.

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1. Precise resistivity control through doping
2. Electron and hole conduction

Resistivity of doped semiconductors. Metals have a conductivity range limited to 10^4 to 10^6/ohm-cm. The implications of this limit are illustrated by an examination of the resistor represented in Fig. 2.5. Given a specific metal with a specific resistivity, the only way to change the resistance of a given volume is to change the dimensions. In a semiconducting material, the resistivity can be changed, giving another degree of freedom in the design of the resistor. Semiconductors are such a material. Their resistivity can be extended over the range of 10^{-3} to 10^3 by the addition of dopant atoms.

Semiconducting materials can be doped into a useful resistivity range by elements that make the material either electron rich (N-type) or hole rich (P-type).

Figure 2.7 shows the relationship of the doping level to the resistivity of silicon. The x-axis is labeled the carrier concentration because the electrons or holes in the material are called *carriers*. Note that there are two curves: N-type and P-type. That is due to the different amount of energies required to move an electron or a hole through the material. As the curves indicate, it takes less of a concentration of N-type dopants than P-type dopants to create a given resistivity in silicon. Another way to express this phenomenon is that it takes less energy to move an electron than to move a hole.

It takes only 0.000001 to 0.1 percent of a dopant to bring a semiconductor material into a useful resistivity range. This property of semiconductors allows the creation of regions of very precise resistivity values in the material.

Electron and Hole Conduction

Another limit of a metal conductor is that it conducts electricity only through the movement of electrons. Metals are permanently N-type. Semiconductors can be made either N- and P-type by doping with specific dopant elements. N- and P-type semiconductors can conduct electricity by either electrons or holes. Before examining the conduction mechanism, it is instructive to examine the creation of free (or extra) electrons or holes in a semiconductor structure.

To understand the situation of N-type semiconductors, consider a piece of silicon (Si) doped with a very small amount of arsenic (As) as shown in Fig. 2.8. Assuming even mixing, each of the arsenic atoms would be surrounded by silicon atoms. Applying the rule from the "Periodic Table of the Elements" section that atoms attempt to stabilize by having eight electrons in their outer ring, the atom is shown shar-

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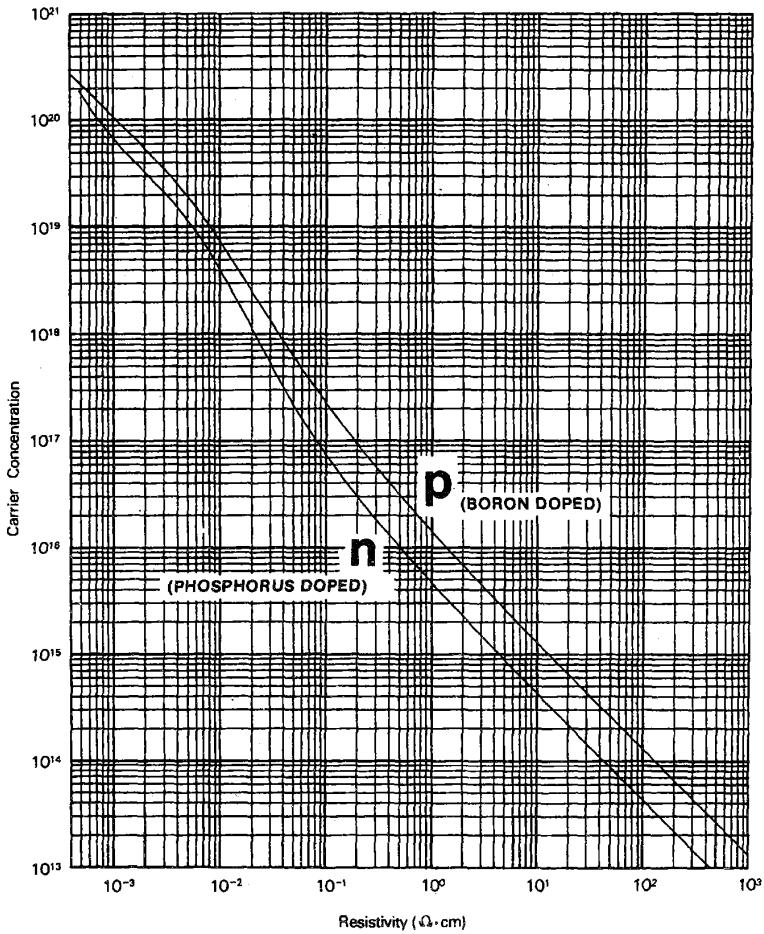


Figure 2.7 Silicon resistivity versus doping (carrier) concentration. *(After Thurber et al., Natl. Bur. Standards Spec. Publ. 400-64, May 1981, Tables 10 and 14.)*

ing four electrons from its neighboring silicon atoms. However, arsenic is from column V, which means it has five electrons in its outer ring. The net result is that four of them pair up with electrons from the silicon atoms, leaving one left over. This one electron is available for electrical conduction.

Considering that a crystal of silicon has millions of atoms per cm^3, there are lots of electrons available to conduct an electrical current. In

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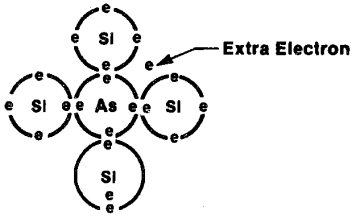


Figure 2.8 N-type doping of silicon with arsenic.

silicon, the elements arsenic, phosphorus and antimony create N-type conditions.

An understanding of P-type material is approached in the same manner (Fig. 2.9). The difference is that only boron, from column III of the periodic table, is used to make silicon P-type. When mixed into the silicon, it too borrows electrons from silicon atoms. However, having only three outer electrons, there is a place in the outer ring that is not filled by an electron. This unfilled position is defined as a *hole.*

Within a doped semiconductor material, there is a great deal of activity: holes and electrons are constantly being created. The electrons are attracted to the unfilled holes, in turn leaving an unfilled position, which creates another hole.

How the electrons contribute to electrical conduction is illustrated in Fig. 2.10. When a voltage is applied across a piece of conducting or semiconducting material, the negative electrons move toward the positive pole of the voltage source, such as a battery.

In P-type material (Fig. 2.11), an electron will move toward the positive pole by jumping into a hole along the direction of route (t_1).

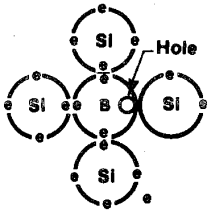


Figure 2.9 P-type doping of silicon with boron.

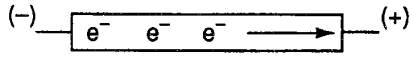


Figure 2.10 Electron conduction in N-type semiconductor material.

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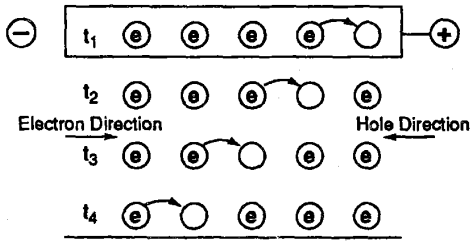


Figure 2.11 Hole conduction in P-type semiconductor material.

Of course, when it leaves its position, it leaves a new hole. As it continues toward the positive pole, it creates a succession of holes. The effect to someone measuring this process with a current meter is that the material is supporting a positive current, when actually it is a negative current moving in the opposite direction. This phenomenon is called *hole flow* and is unique to semiconducting materials.

The dopants that create a P-type conductivity in a semiconductor material are called *acceptors*. Dopants that create N-type conditions are called *donors*. An easy way to keep these terms straight is that acceptor has a p and donor is spelled with an n.

The electrical characteristics of conductors, insulators, and semiconductors are summarized in Fig. 2.12. The particular characteristics of doped semiconductors are summarized in Fig. 2.13.

N- and P-type conditions are also created in germanium and compound semiconductors with specific dopant elements.

Classification	Electrons	Examples	Conductivity
1. Conductor	Free to Move	Gold Copper Silver	10^{4}–10^{6} /ohm-cm
2. Insulator (Dielectric)	Bound	Glass Plastic	10^{-22}–10^{-10} /ohm-cm
3. Semiconductor a. Intrinsic	Some Available	Germanium Silicon III-IV	10^{-9}–10^{3} /ohm-cm
b. Doped	Controlled Amount Available	N-type Semiconductor P-type Semiconductor	

Figure 2.12 Electrical classification of materials.

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	N-TYPE	P-TYPE
1. Conduction	Electrons	Holes
2. Polarity	Negative	Positive
3. Dopant Term	Donor	Acceptor
4. Doping Elements in Silicon	Arsenic Phosphorus Antimony	Boron

Figure 2.13 Characteristics of doped semiconductors.

Carrier mobility

It was mentioned previously that it takes "less energy" to move an electron than a hole through a piece of semiconducting material. In a circuit we are interested in both the energy required to move these carriers (holes and electrons) and the speed at which they move. The speed of movement is called the *carrier mobility,* with holes having a lower mobility than electrons. This factor is an important consideration in selecting a particular semiconducting material for a circuit.

Semiconductor Production Materials

Germanium and silicon

Germanium and silicon are the two elemental semiconductors. The first transistor was made with germanium, as were the initial devices of the solid-state era. However, germanium presents problems in processing and in device performance. Its 937°C melting point limits high-temperature processing. More importantly, its lack of a natural occurring oxide leaves the surface prone to electrical leakage.

The development of silicon/silicon dioxide planar processing solved the leakage problem of integrated circuits, flattened the surface profile of the circuits and allowed higher temperature processing due to its 1415°C melting point. Consequently, silicon represents over 90 percent of the wafers processed worldwide.

Semiconducting Compounds

There are many semiconducting compounds formed from elements listed in columns III and IV and II to VI of the periodic table. Of these compounds, the ones most used in commercial semiconductor devices are gallium arsenide (GaAs) and gallium arsenide-phosphide (GaAsP), indium phosphide (InP), gallium aluminum arsenic (GaAlAs), and in-

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dium gallium phosphide (InGaP).[1] These compounds have special properties.[2] Diodes made from GaAs and GaAsP give off visible and laser light when activated with an electrical current. They are the materials used to make the light-emitting diodes (LEDs) used in electronic panel displays.

An important property of gallium arsenide is its high (electrical) carrier mobility. This property allows a gallium arsenide device to react to high-frequency microwaves and effectively switch them into electrical currents in communications systems faster than silicon devices.

This same property, carrier mobility, is the basis for the excitement over gallium arsenide transistors and ICs. Devices of GaAs operate two to three times faster than comparable silicon devices and find applications in super-fast computers and real-time control circuits such as airplane controls.

GaAs has a natural resistance to radiation-caused leakage. Radiation, such as that found in space, causes holes and electrons to form in semiconductor materials. It gives rise to unwanted currents that can cause the device or circuit to malfunction or cease functioning. Devices that can perform in a radiation environment are known as *radiation hardened.* GaAs is naturally radiation hardened.

GaAs is also semi-insulating. In an integrated circuit, this property minimizes leakage between adjacent devices, allowing a higher packing density, which in turn results in a faster circuit because the holes and electrons travel shorter distances. In silicon circuits, special isolating structures must be built into the surface to control surface leakage. These structures take up valuable space and reduce the density of the circuit.

Despite all of the advantages, GaAs is not expected to replace silicon as the mainstream semiconducting material. The reasons reside in the trade-offs between performance and processing difficulty. While GaAs circuits are very fast, the majority of electronic products do not require their level of speed. On the performance side, GaAs, like germanium, does not possess a natural oxide. To compensate, layers of dielectrics must be deposited on the GaAs, which leads to longer processing and lower yields. Also, half of the atoms in GaAs are arsenic, an element that is very dangerous to human beings. Unfortunately, the arsenic evaporates from the compound at normal process temperatures, requiring the addition of suppression layers (caps) or pressurized process chambers. These steps lengthen the processing and add to its cost.

Evaporation also occurs during the crystal growing stage, resulting in nonuniform crystals and wafers. The nonuniformity produces wafers that are very prone to breakage during fab processing. Also, the production of large-diameter GaAs wafers has lagged behind that of silicon (see Chapter 3).

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Despite the problems, gallium arsenide is an important semiconducting material that will continue to increase in use and will probably have a major influence on computer performance of the future.

Silicon Germanium

Competitors to GaAs are silicon/germanium (SiGe) structures. The combination increases transistor speeds to levels that allow ultra-fast radios and personal communication devices.[3] Device/IC structures feature a layer of germanium deposited by ultra-high vacuum/chemical vapor deposition (UHV/CVD).[4] Bipolar transistors are formed in the Ge layer. Unlike the simpler transistors formed in silicon technology, SiGe required transistors with *hetrostructures* or *heterojunctions.* These are structures with several layers and specific dopant levels to allow high-frequency operations (see Chapter 16).

A comparison of the major semiconducting production materials and silicon dioxide is presented in Fig. 2.14.

Engineered Substrates

A bulk wafer was the traditional substrate for fabricating microchips. Electrical performance demands new substrates, such as silicon on an

	Ge	Si	GaAs	SiO_2
Atomic Weight	72.6	28.09	144.63	60.08
Atoms/cm³ or Molecules	4.42×10^{22}	5.00×10^{22}	2.21×10^{22}	2.3×10^{22}
Crystal Structure	Diamond	Diamond	Zinc-Blends	Amorphous
Atoms/Unit Cell	8	8	8	—
Density	5.32	2.33	5.65	2.27
Energy Gap	0.67	1.11	1.40	8 (approx.)
Dielectric Constant	16.3	11.7	12.0	3.9
Melting Point (°C)	937°	1415°	1238°	1700° (approx.)
Breakdown Field (V/)	8 (approx.)	30 (approx.)	35 (approx.)	600 (approx.)
Linear Coefficient of Thermal Expansion $\frac{\Delta L}{LT}\frac{1}{C}$	5.8×10^{-6}	2.5×10^{-6}	5.9×10^{-6}	0.5×10^{-6}

Figure 2.14 Physical properties of semiconductor materials.

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insulator (SOI) such as sapphire, and silicon on diamond (SOD). Diamond dissipates heat better than silicon. Another structure is a layer of "strained" silicon deposited on a wafer of silicon-germanium. Strained silicon occurs when silicon atoms are deposited on a Si/Ge (sSOI) layer previously deposited on an insulator. Si/Ge atoms are more widely spaced than normal silicon. During the deposition, the silicon atoms "stretch" to align to the SI/Ge atoms, staining the silicon layer. The electrical effect is to lower the silicon resistance, allowing electrons to move up to 70 percent faster. This structure brings performance benefits to MOS transistors (see Chapter 16).

Ferroelectric Materials

In the ongoing search for faster and more reliable memory structures, ferroelectrics have emerged as a viable option. A memory cell must store information in one of two states (on/off, high/low, 0/1), be able to respond quickly (read and write), and be capable of changing states reliably. Ferroelectric material capacitors such as $PbZr_{1-x}T_xO_3$ (PZT) and $SrBi_2Ta_2O_9$ (SBT) exhibit these desirable characteristics. They are incorporated into SiCMOS (see Chapter 16) memory circuits known as ferroelectric random access memories (FeRAMs).[5]

Diamond Semiconductors

Moore's law cannot go indefinitely into the future. One end point is when the transistor parts become so tiny that the physics governing transistor action no longer work. Another limit is heat dissipation. Bigger and denser chips run very hot. Unfortunately, high heat also degrades the electrical operations and can render the chip useless. Diamond is a crystal material that dissipates heat much faster than silicon. Despite this positive aspect, diamond as a semiconductor wafer has faced barriers of cost, uniformity, and finding a supply of large diamonds. However, there is new research into making synthetic diamonds using vapor deposition techniques. Doping diamond is the next barrier. This material is being explored and may find its way into fabrication areas of the future.[6]

Process Chemicals

It should be fairly obvious that extensive processing is required to change the raw semiconducting materials into useful devices. The majority of these processes use chemicals. In fact, microchip fabrication is primarily a chemical process or, more correctly, a series of chemical

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processes. Up to 20 percent of all process steps are cleaning or wafer surface preparation.[6]

Great quantities of acids, bases, solvents, and water are consumed by a semiconductor plant. Part of this cost is due to the extremely high purities and special formulations required of the chemicals to allow precise and clean processing. Larger wafers and higher cleanliness requirements need more automated cleaning stations and the cost of removal of spent chemicals is rising. When the costs of producing a chip are added up, process chemicals can be up to 40 percent of all manufacturing costs.

The cleanliness requirements for semiconductor process chemicals are explored in Chapter 4. Specific chemicals and their properties are detailed in the process chapters.

Molecules, compounds, and mixtures

At the beginning of this chapter, the basic structure of matter was explained by the use of the Bohr atomic model. This model was used to explain the structural differences of the elements that make up all the materials in the physical universe. But it is obvious that the universe contains more than 103 (the number of elements) types of matter.

The basic unit of a nonelemental material is the molecule. The basic unit of water is a molecule composed of two hydrogen atoms and one oxygen atom. The multiplicity of materials comes about from the ability of atoms to bond together to form molecules.

It is inconvenient to draw diagrams such as in Fig. 2.15 every time we want to designate a molecule. The more common practice is to write the molecular formula. For water, it is the familiar H_2O. This formula tells us exactly the elements and their number in the material. Chemists use the more precise term *compound* in describing different combinations of elements. Thus, H_2O (water), NaCl (sodium chloride or salt), H_2O_2 (hydrogen peroxide), and As_2O_3 (arsine) are all different compounds composed of aggregates of individual molecules.

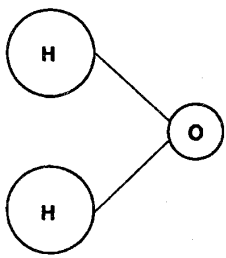


Figure 2.15 Diagram of water molecule.

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Slurries are used in polishing operations such as *chemical mechanical polishing* (CMP). Typical slurries have fine pieces of silica (glass) suspended in a mild base solution such as ammonium hydroxide.

Some elements combine into *diatomic molecules.* A diatomic molecule is one composed of two atoms of the same element. The familiar process gases (oxygen, nitrogen, and hydrogen), in their natural state, are all composed of diatomic molecules. Thus, their formula's are O_2, N_2, and H_2.

Materials also come in two other forms: mixtures and solutions. Mixtures are composed of two or more substances, but the substances retain their individual properties. A mixture of salt and pepper is the classic example.

Solutions are mixtures of a solid dissolved in a liquid. In the liquid, the solids are interspersed, with the solution taking on unique properties. However, the substances in a solution do not form into a new molecule. Saltwater is an example of a solution. It can be separated back into its starting parts: salt and water.

Ions

The term *ion* or *ionic* is used often in connection with semiconductor processing. This term refers to any atom or molecule that exists in a material with an unbalanced charge. An ion is designated by the chemical symbol of the element or molecule followed by a superscripted positive or negative sign (Na^+, Cl^-). For example, one of the serious contamination problems is mobile ionic contamination such as sodium (Na^+). The problem comes from the positive charge carried by the sodium when it gets into the semiconductor material or device. In some processes, such as the ion implantation process, it is necessary to create an ion, such as boron (B^+), to accomplish the process.

States of Matter

Solids, liquids, and gases

Matter is found in four different states. They are solids, liquids, gases, and plasma (Fig. 2.16).

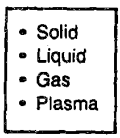


Figure 2.16 Four states of nature.

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- Solids are defined as having a definite shape and volume, which is retained under normal conditions of temperature and pressure.
- Liquids have definite volume but a variable shape. A liter of water will take the shape of any container in which it is stored.
- Gases have neither definite shape nor volume. They too will take the shape of any container but, unlike liquids, they will expand or can be compressed to entirely fill the container.

The state of a particular material has a lot to do with its pressure and temperature. Temperature is a measure of the total energy incorporated in the material. We know that water can exist in three states (ice, liquid water, and steam or water vapor) simply by changing the temperature and/or pressure. The influence of pressure is more complicated and beyond the scope of this text.

Plasma state

The fourth state of nature is plasma. A star is an example of a plasma state. It certainly does not meet the definitions of a solid, liquid, or gas. A plasma state is defined as a high-energy collection of ionized atoms or molecules. Plasma states can be induced in process gases by the application of high-energy radio-frequency (RF) fields. They are used in semiconductor technology to cause chemical reactions in gas mixtures. One of their advantages is that energy can be delivered at a lower temperature than in convention systems, such as convection heating in ovens.

Properties of Matter

All materials can be differentiated by their chemical compositions and the properties that arise from those compositions. In this section, several key properties required to understand and work with properties of semiconductor materials and chemicals are defined.

Temperature

The temperature of a chemical exerts great influence on its reactions with other chemicals, whether in an oxidation tube or in a plasma etcher. Additionally, safe use of some chemicals requires knowledge and control of their temperatures. Three temperature scales are used to express the temperature of a material. They are the Fahrenheit, Centigrade (or Celsius) and the Kelvin scale (Fig. 2.17).

The Fahrenheit scale was developed by Gabriel Fahrenheit, a German physicist, using a water and salt solution. He assigned to the so-

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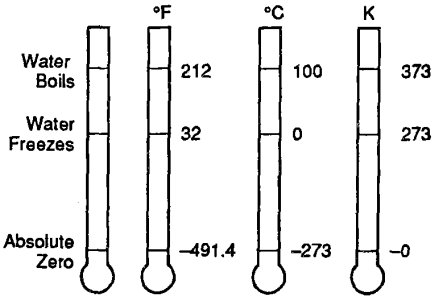


Figure 2.17 Temperature scales.

lution's freezing temperature the value of zero degrees Fahrenheit (0°F). Unfortunately, the freezing temperature of pure water is more useful, and we have ended up with the Fahrenheit scale having a water freezing point at 32°F and a boiling point of 212°F, with 180° between the two points.

The Celsius or centigrade scale is more popular in scientific endeavors. It more sensibly sets the freezing point of water at 0°C and boiling at 100°C. Note that there are exactly 100 degrees Celsius between the two points. This means that a one-degree change in temperature as measured on the centigrade scale requires more energy than a one-degree change on the Fahrenheit scale.

The third temperature scale is the Kelvin scale. It uses the same scale factor as the centigrade scale but is based on absolute zero. Absolute zero is the theoretical temperature at which all atomic motion would cease. This value corresponds to –273°C. On the Kelvin scale, water freezes at 273 K and boils at 373 K.*

Density, specific gravity, and vapor density

An important property of matter is density. When we say that something is *dense*, we refer to its mass or weight per unit volume. A cork has a lower density than an equal volume of iron. Density is expressed as the weight, in grams, per cubic centimeter of the material. Water is the standard, with one cubic centimeter (at 4°C) weighing 1 g. The densities of other substances are expressed as a ratio of their density to that of a comparable volume of water. Silicon has a density of 2.3. Therefore, a piece of silicon one cubic centimeter (1 cm^3) in volume will weigh 2.3 g.

Specific gravity is a term used to reference the density of liquids and gases at 4°C. It is the ratio of the density of the substance to that of

*The degree symbol is omitted when using the Kelvin scale.

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water. Gasoline has a specific gravity of 0.75, which means it is 75 percent as dense as water.

Vapor density is a density measurement of gases under certain conditions of temperature and pressure. The reference is air, with one cubic centimeter having an assigned density of one (1). Hydrogen has a vapor density of 0.60 which makes it 60 percent the density of a similar volume of air. The contents of a container of hydrogen will weigh 60 percent less than a similar container of air.

Pressure and Vacuum

Another important aspect of matter is pressure. Pressure, as a property, is usually used in connection with liquids and gases. It is defined as the force per unit area exerted against the surface of the container. It is the gas pressure in a cylinder that forces the gas out into a process chamber. All processes machines using gases must have gauges to measure and control the pressure.

Pressures are expressed in pounds per square inch of area (psia), in atmospheres or in torrs. An atmosphere (A) is the pressure exerted by the atmosphere surrounding the Earth at a specific temperature. Thus, a high-pressure oxidation system operated at 5 atmospheres contains a pressure 5 times that of the atmosphere.

One atmosphere of air has a pressure of 14.7 psia. Pressures inside gas tanks are measured in psig units or pounds per square inch gauge. This means that the gauge reading is absolute; it does not include the pressure of the outside atmosphere.

Vacuum is also a term and condition encountered in semiconductor processing. It is actually a condition of low pressure. Generally, pressures below standard atmospheric pressures are referred to as vacuums. But a vacuum condition is measured in units of pressure.

Low pressures tend to be expressed in torrs. The unit is named after the Italian scientist, Torricelli, who made many of the early discoveries in the field of gases and their properties. A torr is defined as the equivalent of one millimeter of mercury in a pressure measuring device known as a *manometer.*

Imagine the effect on the column of mercury in the manometer in Fig. 2.18*a* of increasing the pressure above atmospheric pressure. As the pressure goes up, it pushes down the mercury in the dish and raises the mercury in the column. Now imagine what happens as air is extracted from the system (Fig 2.18*b*) below atmospheric pressure creating a vacuum. As long as there are any gas molecules or atoms in the manometer, some small pressure will be exerted on the mercury in the dish, and the mercury in the column will rise some small but finite

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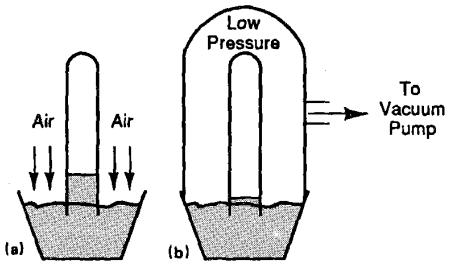


Figure 2.18 Pressure vacuum measurement.

amount. The amount of the rise as measured in millimeters (mm) is relative to the pressure or, in this case, the vacuum.

Vacuum systems for evaporation, sputtering, and ion implantation are operated at vacuums (pressures) of 10^{-6} to 10^{-9} torrs. Translated into a vacuum system containing a simple manometer, this means that the column of mercury would rise only 0.000000001 (1×10^{-9}) to 0.000001 (1×10^{-6}) millimeters—a *very* short length! In actual practice, a mercury manometer cannot measure these extremely low pressures. Other, more sensitive gauges are used.

Acids, Alkalis, and Solvents

Acids and alkalis

Semiconductor processing requires large amounts of liquid chemicals to etch, clean, and rinse the wafers and packages. These chemicals are identified by chemists into three major classifications.[7]

- Acids
- Alkalis
- Solvents

Acids and alkalis differ from each other due to the presence of specific ions in the liquid. Acids contain *hydrogen ions*, while alkalis (also called *bases*) contain *hydroxide ions*. An examination of the water molecule explains the differences.

The chemical formula for water normally is written as H_2O. It can also be written in the form HOH. When separated into its parts, we find that water is made up of a positively charged hydrogen ion (H^+) and a negatively charged hydroxide ion (OH^-).

When water is mixed with other elements, either the hydrogen or hydroxyl ion combines with other substances (Fig. 2.19). Liquids that contain the hydrogen ion are called *acids*. Liquids that contain the hydroxyl ion are called *alkalis* or *bases*. Acids and bases are commonly

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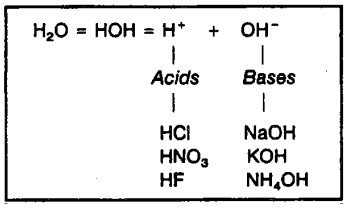


Figure 2.19 Acid and base solutions.

found in the home: lemon juice and vinegar are acids, and ammonia and baking soda in a solution of water are bases.

Acids are further divided into two categories: organic and inorganic. Organic acids are those that contain hydrocarbons, whereas inorganic acids do not. Sulfonic acid is an organic acid, and hydrogen fluoride (HF) is an inorganic acid.

The strength and reactivity of acids and bases are measured by the pH scale (Fig. 2.20). This scale ranges from 0 to 14, with 7 being a neutral point. Water is neutral, neither an acid or a base; therefore, it has a pH of 7. Strong acids, such as sulfuric acid (H_2SO_4), will have low pH values of 0 to 3. Strong bases, such as sodium hydroxide (NaOH), have pH values greater than 7.

Both acids and bases are reactive with skin and other chemicals and should be stored and handled with all of the prescribed safety precautions.

Solvents

Solvents are liquids that do not ionize; they are neutral on the pH scale. Water is a solvent; in fact, it is the solvent with the greatest

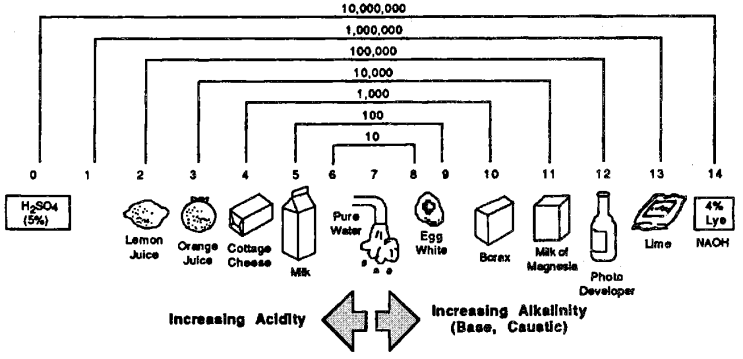


Figure 2.20 pH scale.

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ability to dissolve other substances. It is also the most commonly used solvent in semiconductor processing. Alcohol and acetone are other common solvents in the wafer fabrication process.

Most of the solvents in fab processing are volatile, flammable, or combustible. It is important to use them in properly exhausted stations and observe prescribed precautions in their storage and use.

Chemical Purity and Cleanliness

While the names of chemicals used in fabrication areas sound familiar, there is an entire supply industry dedicated to producing the highest-quality chemicals to meet semiconductor processing demands. Chemicals must meet very high purity requirements. In general the target is "six nines" purity. This translates to 99.9999 percent pure. Physical contamination such as particles are also controlled. Typical chemical specifications limit particles to parts per billion (PPB)/liter and microns. These and other specifications are established in the 2001 *International Technology Roadmap for Semiconductors* (ITRS). Specific chemicals used are identified in the chapter on contamination control and the individual process chapters.

Safety issues

The storage, use, and disposal of chemicals and electrical and other risks are present in semiconductor process areas. Companies address these risks by developing employee knowledge, skill, and awareness through training programs and safety inspections.

The Material Safety Data Sheet

For every chemical brought into a manufacturing site, the supplier must provide a form called the Material Safety Data Sheet (MSDS). It is required by the federal Occupational, Safety, and Health Administration (OSHA). The form is also called OSHA Form 20. This form contains chemical, storage, health, first aid, and usage information about the chemical. Under current regulations, the MSDSs must be filed on the site and available to employees.

Review Questions

1. Describe the electrical difference between a conductor, a dielectric and a semiconductor.
2. Why are doped semiconductors required for solid-state devices?

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3. Which has a higher resistivity, a metal or an intrinsic semiconductor?
4. Give two reasons silicon is the most common semiconducting material.
5. Name one element that will make silicon "N" type.
6. A "P"-type semiconductor exhibits a (negative or positive) current.
7. Indicate which classification (acid, base, solvent) is described below.

   a. Contains OH^- ions
   b. Contains H^- ions
   c. Is neutral on the pH scale

8. Acids have a pH between _____and _____.
9. Bases have a pH between _____ and _____.
10. What is the pH of water?

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Chapter

3

Crystal Growth and Silicon Wafer Preparation

Overview

In this chapter, the preparation of semiconductor-grade silicon from sand, its conversion into crystals and wafers (material preparation stage), and the processes required to produce polished wafers (crystal growth and wafer preparation) are explained.

Objectives

Upon completion of this chapter, you should be able to:

1. Explain the difference between crystalline and noncrystalline materials.
2. Explain the differences between a polycrystalline and a single crystalline material.
3. Draw a diagram of the two major wafer crystal orientations used in semiconductor processing.
4. Explain the Czochralski, float zone and liquid crystal encapsulated Czochralski methods of crystal growing.
5. Draw a flow diagram of the wafer preparation process.
6. Explain the use and meaning of the flats or notches ground on wafers.
7. Describe the benefits in the wafer fab process that come from edge-rounded wafers.

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8. Describe the benefits in the wafer fab process that come from flat and damage-free wafer surfaces.

Introduction

The evolution of higher-density and larger-size chips has required the delivery of larger diameter wafers. Starting with 1-in diameter wafers in the 1960s, the industry is now introducing 300-mm (12-in) diameter wafers into production lines. According the International Technology Roadmap for Semiconductors, 300-mm wafers will be the standard diameter until about 2007, and 400- or 450-mm diameter wafers are predicted for the far future (Figure 3.1). Larger-diameter wafers are necessary to accommodate increasing chip sizes with cost effective wafer fabrication processes (see Chaps. 6 and 15). The challenges in wafer preparation are formidable. In crystal growth, the issues of structural and electrical uniformity and contamination become challenges. In wafer preparation, flatness, diameter control, and crystal integrity are issues. Larger diameters are heavier, which requires more substantial process tools and, ultimately, full automation. A production lot of 300-mm diameter wafers weighs about 20 lb (7.5 kg) and can have a production value of half a million dollars or more.[1] These challenges coexist with ever tightening specifications for almost every parameter. Keeping abreast of these challenges and providing ever larger diameter wafers is a key to continued microchip evolution.

Semiconductor Silicon Preparation

Semiconductor devices and circuits are formed in and on the surface of wafers of a semiconductor material, usually silicon. Those wafers must have very low levels of contaminants, be doped to a specified resistivity level, have a specific crystal structure, be optically flat, and meet a host of other mechanical and cleanliness specifications. Manufacture of IC grade silicon wafers proceeds in four stages.

Year of production	2001	2006	2012
Wafer diameter (mm)	300	300	450

Figure 3.1 Wafer diameters. *(Courtesy of SIA.)*

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Silicon wafer preparation stages

- Conversion of ore to a high-purity gas
- Conversion of gas to polysilicon silicon
- Conversion of polysilicon silicon to a single crystalline, doped crystal ingot
- Preparation of wafers from the crystal ingot

The first stage of semiconductor manufacturing is the extraction and purification of the raw semiconductor material(s) from the earth. Purification starts with a chemical reaction. For silicon, it is the conversion of the ore to a silicon-bearing gas such as silicon tetrachloride or trichlorosilane. Contaminants, such as other metals, are left behind in the ore remains. The silicon bearing gas is then reacted with hydrogen (Fig. 3.2) to produce semiconductor grade silicon. The silicon produced is 99.9999999 percent pure, one of the purist materials on Earth.[2] It has a crystal structure known as polycrystalline or *polysilicon.*

Crystalline Materials

One way that materials differ is in the organization of their atoms. In some materials, such as silicon and germanium, the atoms are arranged into a very definite structure that repeats throughout the material. These materials are called *crystals.*

Materials without a definite periodic arrangement of their atoms are called noncrystalline or *amorphous.* Plastics are examples of amorphous materials.

Unit cells

There are actually two levels of atomic organization possible for crystalline materials. First is the organization of the individual atoms. The atoms in a crystal arrange themselves at specific points in a structure known as a *unit cell.* The unit cell is the first level of organization in a crystal. The unit cell structure is repeated everywhere in the crystal.

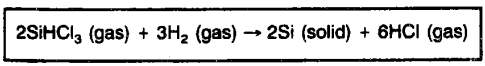


Figure 3.2 Hydrogen reduction of trichlorosilane.

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Another term used to reference crystal structures is *lattice*. A crystalline material is said to have a specific lattice structure and that the atoms are located at specific points in the lattice structure.

The number of atoms, relative positions, and binding energies between the atoms in the unit cell gives rise to many of the characteristics of the material. Each crystalline material has a unique unit cell. Silicon atoms have 16 atoms arranged into a diamond structure (Fig. 3.3). GaAs crystals have 18 atoms in a unit cell configuration called a zincblend (Fig. 3.4).

Poly and single crystals

The second level of organization within a crystal is related to the organization of the unit cells. In intrinsic semiconductors, the unit cells are *not* in a regular arrangement to each other. The situation is similar to a disorderly pile of sugar cubes, with each cube representing a unit cell. A material with such an arrangement has a polycrystalline structure.

The second level of organization occurs when the unit cells (sugar cubes) are all neatly and regularly arranged relative to each of the others (Fig. 3.5). Materials thus arranged have a single (or mono-) crystalline structure.

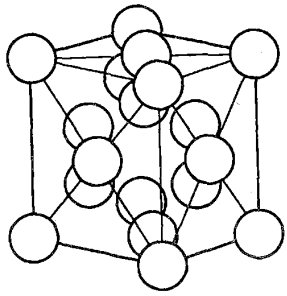


Figure 3.3 Unit cell of silicon.

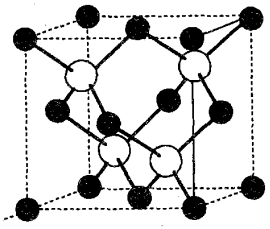


Figure 3.4 GaAs crystal structure.

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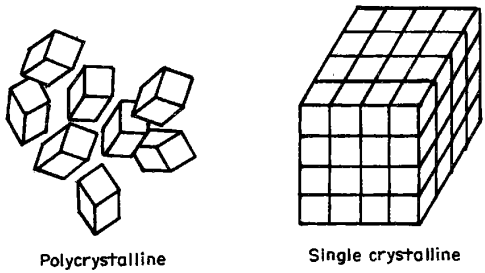


Figure 3.5 Poly- and single-crystal structures.

Single-crystal materials have more uniform and predictable properties than polycrystalline materials. The structure allows a uniform and predictable electron flow in semiconductors. At the end of the fab process, crystal uniformity is essential for separating the wafer into die with non-ragged edges (see Chapter 18).

Crystal Orientation

In addition to the requirement of a single-crystal structure for a wafer, there is the requirement of a specific *crystal orientation*. This concept can be visualized by considering slicing the single crystalline block in shown in Fig. 3.5. Slicing it in the vertical plane would expose one set of *planes,* while slicing it corner-to-corner would expose a different plane. Each plane is unique, differing in atom count and binding energies between the atoms. Each has different chemical, electrical, and physical properties that are imparted to the wafers. Specific crystal orientations are required for the wafers.

Crystal planes are identified by a series of three numbers known as Miller Indices. Two simple cubic unit cells nestled into the origin of a XYZ coordinate system are shown in Fig. 3.6. The two most common orientations used for silicon wafers are the ⟨100⟩ and the ⟨111⟩ planes. The plane designations are verbalized as the one-oh-oh plane and the one-one-one plane. The brackets indicate that the three numbers are Miller indices.

⟨100⟩ oriented wafers are used for fabricating MOS devices and circuits, while the ⟨111⟩ oriented wafers are used for bipolar devices and circuits. GaAs wafers are also cut along the ⟨100⟩ planes of the crystal.

Note that the ⟨100⟩ plane in Fig. 3.6 has a square shape, while the ⟨111⟩ plane is triangular in shape. These orientations are revealed when wafers are broken as shown in Fig. 3.7. The ⟨100⟩ wafers break

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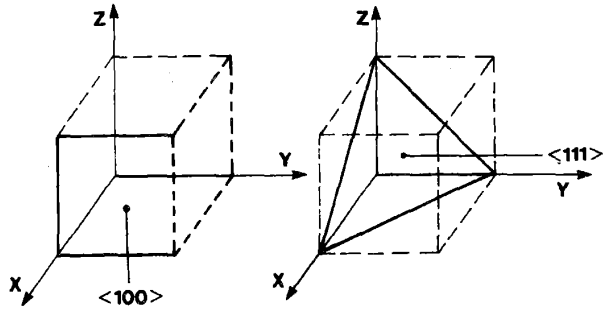


Figure 3.6 Crystal planes.

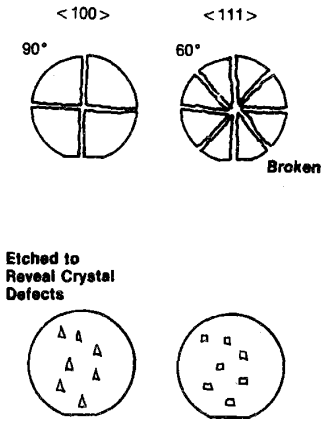


Figure 3.7 Wafer orientation indicators.

into quarters or with right angle (90°) breaks. The ⟨111⟩ wafers break into triangular pieces.

Crystal Growth

Semiconductor wafers are cut from large crystals of the semiconducting material. These crystals, also called *ingots*, are grown from chunks of the intrinsic material, which have a polycrystalline structure and are undoped. The process of converting the polycrystalline chunks to a large crystal of single-crystal structure, with the correct orientation and the proper amount of N- or P-type, is called *crystal growing*.

Three different methods are used to grow crystals: the Czochralski, liquid encapsulated Czochralski, and float zone techniques.

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Czochralski (CZ) method

The majority of silicon crystals are grown by the CZ method (Fig. 3.8). The equipment consists of a quartz (silica) crucible that is heated by surrounding coils that carry radio frequency (RF) waves or by electric heaters. The crucible is loaded with chunks of polycrystalline of the semiconductor material and small amounts of dopant. The dopant material is selected to create either an N-type or P-type crystal. First, the poly and dopants are heated to the liquid state at 1415°C (Fig. 3.9). Next, a seed crystal is positioned to just touch the surface of the liquid material (called the *melt*). The seed is a small crystal that has the same crystal orientation required in the finished crystal. Seeds can be

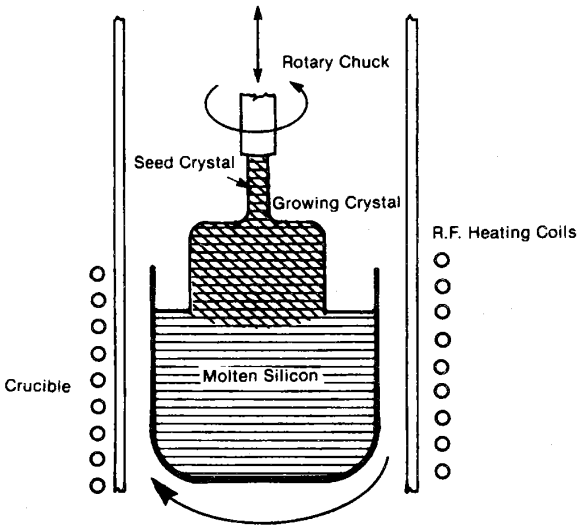


Figure 3.8 Czochralski crystal-growing system.

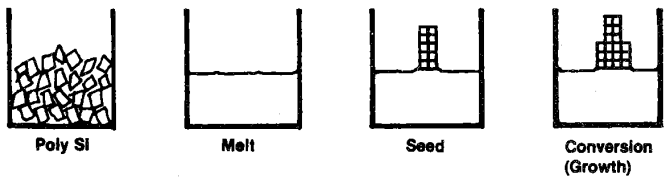


Figure 3.9 Crystal growth from a seed.

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produced by chemical vapor techniques. In practice, they are pieces of previously grown crystals and are reused.

Crystal growth starts as the seed is slowly raised above the melt. The surface tension between the seed and the melt causes a thin film of the melt to adhere to the seed and then to cool. During the cooling, the atoms in the melted semiconductor material orient themselves to the crystal structure of the seed. The net effect is that the crystal orientation of the seed is propagated in the growing crystal. The dopant atoms in the melt become incorporated into the growing crystal, creating an N- or P-type crystal.

To achieve doping uniformity, crystal perfection, and diameter control, the seed and crucible (along with the pull rate) are rotated in opposite directions during the entire crystal-growing process. Process control requires a complicated feedback system integrating the parameters of rotational speed, pull speeds, and melt temperature.

The crystal is pulled in three sections. First a thin neck is formed, followed by the body of the crystal ending with a blunt tail. The CZ method is capable of producing crystals several feet in length and with diameters up to 12 or more inches. A crystal for 200-mm wafers will weigh some 450 lb (168 kg) and take three days to grow.

Liquid encapsulated Czochralski (LEC)

LEC crystal growing[3] is used for the growing of gallium arsenide crystals. It is essentially the same as the standard CZ process but with a major modification for gallium arsenide. The modification is required because of the evaporative property of the arsenic in the melt. At the crystal growing temperature, the gallium and arsenic react, and the arsenic can evaporate, resulting in a nonuniform crystal.

Two solutions to the problem are available. One is to pressurize the crystal growing chamber to suppress the evaporation of the arsenic. The other is the LEC process (Fig. 3.10). LEC uses a layer of boron trioxide (B_2O_3) floating on top of the melt to suppress the arsenic evaporation. In this method, a pressure of about one atmosphere is required in the chamber.

Float zone

Float zone crystal growth is one of several processes explained in this text that were developed early in the history of the technology and are still used for special needs. A drawback to the CZ method is the inclusion of oxygen from the crucible into the crystal. For some devices, higher levels of oxygen are intolerable. For these special cases, the

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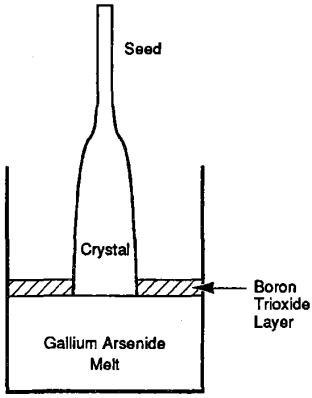


Figure 3.10 LEC system of crystal growth.

crystal might be grown by the float zone technique, which produces a lower oxygen content crystal.

Float zone crystal growth (Fig. 3.11) requires a bar of the polysilicon and dopants that have been cast in a mold. The seed is fused to one end of the bar and the assemblage placed in the crystal grower. Conversion of the bar to a single-crystal orientation starts when an RF coil heats the interface region of the bar and seed. The coil is then moved along the axis of the bar, heating it to the liquid point a small section at a time. Within each molten region, the atoms align to the orientation started at the seed end. Thus, the entire bar is converted to a single crystal with the orientation of the starting seed.

Float zone crystal growing cannot produce the large diameters that are obtainable with the CZ process, and the crystals have a higher dislocation density. But the absence of a silica (silicon) crucible yields higher-purity crystals with lower oxygen content. Lower oxygen allows crystals with higher that find use in semiconductor devices such as power thyristors and rectifiers. The two methods are compared in Fig. 3.12.

Crystal and Wafer Quality

Semiconductor devices require a high degree of crystal perfection. But even with the most sophisticated techniques, a perfect crystal is unobtainable. The imperfections, called *crystal defects*, result in process problems by causing uneven silicon dioxide film growth, poor epitaxial film deposition, uneven doping layers in the wafer, and other problems. In finished devices, the crystal defects cause unwanted current

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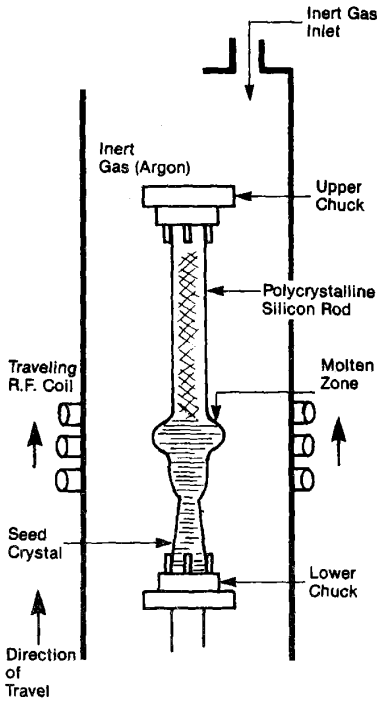


Figure 3.11 Float zone crystal-growing system.

PARAMETER	CZ	FLOAT ZONE
Large Crystal	Yes	Difficult
Cost	Lower	
Dislocations	0 - 10^4/cm^2	10^3 - 10^5/cm^2
Resistivity	Up to 100 ohm-cm	2000 ohm-cm Max.
Radial Resistivity	5 - 10%	5 - 10%
Oxygen Content	10^{16} - 10^{18} atoms/cm^3	0 - Very Low

Figure 3.12 Comparison of CZ and float crystal-growing methods.

leakage and may prevent the devices from operating at required voltages. There are three major categories of crystal defects:

1. Point defects
2. Dislocations
3. Growth defects

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Point defects

Point defects come in two varieties. One comes when contaminants in the crystal become jammed in the crystal structure, causing strain. The second is known as a vacancy. In this situation, there is an atom missing from a location in the structure (Fig. 3.13).

Vacancies are natural phenomena that occur in every crystal. Unfortunately, vacancies occur whenever a crystal or wafer is heated and cooled, such as in the fabrication process. The minimization of vacancies is one of the driving forces behind the desire for low-temperature processing.

Dislocations

Dislocations are misplacements of the unit cells in a single crystal. They can be imagined as a orderly pile of sugar cubes with one of the cubes slightly out of alignment with the others.

Dislocations occur from growth conditions and lattice strain in the crystal. They also occur in wafers from physical abuse during the fab process. A chip or abrasion of the wafer edge serves as a lattice strain site that can generate a line of dislocations that progresses into the wafer interior with each subsequent high-temperature processing of the wafer. Wafer dislocations are revealed by a special etch of the surface. A typical wafer has a density of 200 to 1000 dislocations per square centimeter.

Etched dislocations appear on the surface of the wafer in shapes indicative of their crystal orientation. ⟨111⟩ wafers etch into triangular dislocations, and ⟨100⟩ wafers show "squarish" etch pits (Fig. 3.7).

Growth defects

During crystal growth, certain conditions can result in structural defects. One is *slip,* which refers to the slippage of the crystal along crystal planes (Fig. 3.14). Another problem is *twinning.* This is a situation in which the crystal grows in two different directions from the same interface. Both of these defects are cause for rejection of the crystal.

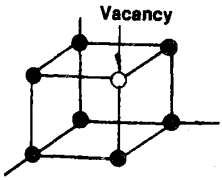


Figure 3.13 Vacancy crystal defect.

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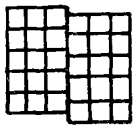


Figure 3.14 Crystal slip.

Wafer Preparation

End cropping

After removal from the crystal grower, the crystal goes through a series of steps that result in the finished wafer. First is the cropping off of the crystal ends with a saw.

Diameter grinding

During crystal growth, there is a diameter variation over the length of the crystal (Fig. 3.15). Wafer fabrication processing, with its variety of wafer holders and automatic equipment, requires tight diameter control to minimize warped and broken wafers.

Diameter grinding is a mechanical operation performed in a centerless grinder. This machine grinds the crystal to the correct diameter without the necessity of clamping it into a lathe-type grinder with a fixed center point—although lathe-type grinders are used.

Crystal orientation, conductivity, and resistivity check

Before the crystal is submitted to the wafer preparation steps, it is necessary to determine whether it meets orientation and resistivity specifications.

The crystal orientation (Fig. 3.16) is determined by either X-ray diffraction or collimated light refraction. In both methods, an end of the crystal is etched or polished to remove saw damage. Next, the crystal is mounted in the refraction apparatus and the X-rays or collimated light reflected off the crystal surface onto a photographic plate (X-rays) or screen (collimated light). The pattern formed on the plate or

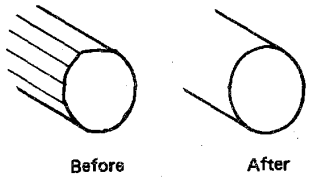


Figure 3.15 Crystal diameter grinding.

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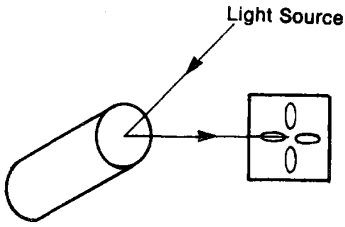


Figure 3.16 Crystal orientation determination.

screen is indicative of the crystal plane (orientation) of the grown crystal. The pattern shown in Fig. 3.16 is representative of a ⟨100⟩ orientation.

Most crystals are purposely grown several degrees off the major ⟨111⟩ or ⟨100⟩ plane. This off-orientation provides several benefits in wafer fabrication processing, particularly ion implantation. The reasons are covered in the applicable process chapters.

The crystal is positioned on a slicing block to ensure that the wafers will be cut from the crystal in the correct orientation.

Because each crystal is doped, an important electrical check is the conductivity type (N or P) to ensure that the right dopant type was used. A hot-point probe connected to a polarity meter is used to generate holes or electrons (depending on the type) in the crystal. The conductivity type is displayed on the meter.

The amount of dopant put into the crystal is determined by a resistivity measurement using a four-point probe. See Chapter 13 for a description of this measurement technique. The curves presented in Chapter 2 (Fig. 2.7) show the relationship between resistivity and doping concentration for N- and P-type silicon.

The resistivity is checked along the axis of the crystal due to dopant variation during the growing process. This variation results in wafers that fall into several resistivity specification ranges. Later in the process, the wafers will be grouped by resistivity range to meet customer specifications.

Grinding orientation indicators

Once the crystal is oriented on the cutting block, a flat is ground along the axis (Fig. 3.17). This flat will show up on each of the wafers and is called the *major flat.* The position of the flat is along one of the major crystal planes, as determined by the orientation check.

In the fabrication process, the flat functions as a visual reference to the orientation of the wafer. It is used to place the first pattern mask on the wafer so that the orientation of the chips is always to a major crystal plane.

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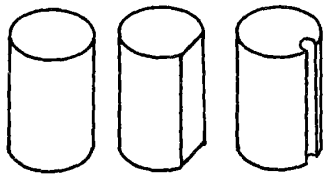


Figure 3.17 Crystal flat grinding.

On most crystals, there is a second, smaller, secondary flat ground on the edge. The position of the secondary flat to the major flat is a code that tells the wafer fabrication department both the orientation and conductivity type of the wafer. The code is shown in Fig. 3.18.

For larger wafer diameters, a notch is ground on the crystal to indicate the wafer crystal orientation (Fig. 3.17). In some cases, a simple notch is ground into the crystal to act as a production orientation locator.

Wafer Slicing

The wafers are sliced from the crystal with the use of diamond-coated inside diameter saws (Fig. 3.19). These saws are thin circular sheets of steel with a hole cut out of the center. The inside of the hole is the cutting edge and is coated with diamonds. An inside diameter saw has rigidity, but without being very thick. These factors reduce the kerf (cutting width) size which in turn prevents sizable amounts of the crystal being wasted by the slicing process.

For 300-mm diameter wafers, wire saws are used to ensure flat surfaces with little tapering and with a minimal amount of "kerf" loss.

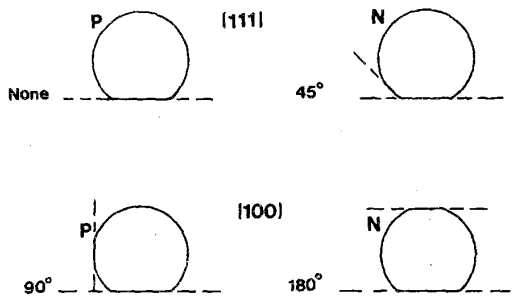
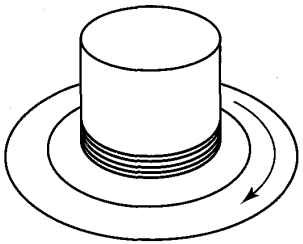
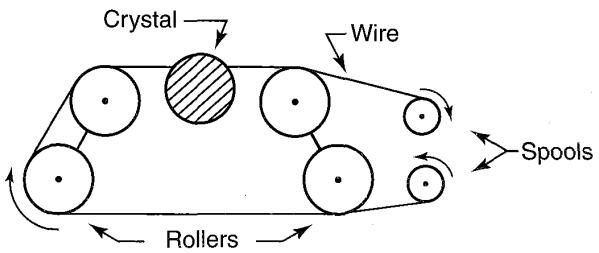


Figure 3.18 Wafer flat locations.

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a. Inside Diameter Diamond Saw



b. Wire Saw

Figure 3.19 Inside-diameter saw wafer slicing.

Wafer Marking

Large-area wafers represent a high value in the wafer fabrication process. Identifying them is necessary to prevent misprocessing and to maintain accurate tracking. Laser marking, using bar codes and a data matrix code[4] (Fig. 3.20), is used. Laser dots are the agreed upon method for 300-mm wafers.

Rough Polish

The surface of a semiconductor wafer has to be free of irregularities and saw damage and must be absolutely flat. The first requirement comes from the very small dimensions of the surface and subsurface layers making up the device. They have dimensions in the 0.5 to 2 micron range. To get an idea of the relative dimensions of a semiconductor device, imagine the cross section in Fig. 3.21 as tall as a house

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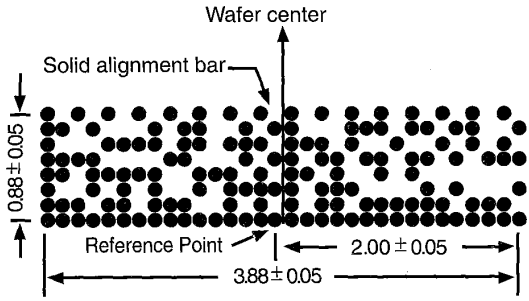


Figure 3.20 Laser dot coding. *(Reprinted from the Jan. 1998 edition of* Solid State Technology, *copyright 1998 by Penn-Well Publishing Company.)*

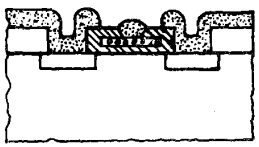


Figure 3.21 Cross section of a MOS transistor.

wall, about 8 ft (2.4 m). On that scale, the working layers on the top of the wafer would all exist within the top 1 or 2 in (25 or 50 mm) or less.

Flatness is an absolute requirement for small dimension patterning (see Chapter 11). The advanced patterning processes project the required pattern image onto the wafer surface. If the surface is not flat, the projected image will be distorted just as a film image will be out of focus on a non-flat screen.

The flatting and polishing process proceeds in two steps: rough polish and chemical/mechanical polishing (Fig. 3.22). Rough polishing is a conventional abrasive slurry lapping process, but it is fine tuned to semiconductor requirements. A primary purpose of the rough polish is to remove the surface damage left over from the wafer slicing process.

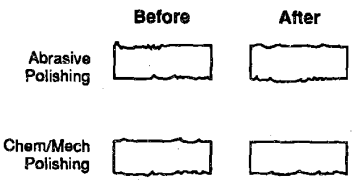


Figure 3.22 Abrasive and chemical-mechanical surface polishing.

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Chemical Mechanical Polishing (CMP)

The final polishing step is a combination of chemical etching and mechanical buffing. The wafers are mounted on rotating holders and lowered onto a pad surface rotating in the opposite direction. The pad material is generally a cast and sliced polyurethane with a filler or a urethane coated felt. A slurry of silica (glass) suspended in a mild etchant, such as potassium or ammonium hydroxide, is dropped onto the polishing pad.

The alkaline slurry chemically grows a thin layer of silicon dioxide on the wafer surface. The buffing action of the pad mechanically removes the oxide in a continuous action. High points on the wafer surface are removed until an extremely flat surface is achieved. If a semiconductor wafer surface was extended to 10,000 ft (3,048 m—the length of a typical airport runway), it would vary about plus or minus 2 in (50 mm) over its entire length.

Achieving the extreme flatness requires the specification and control of the polishing time, the pressure on the wafer and pad, the speed of rotation, the slurry particle size, the slurry feed rate, the chemistry (pH) of the slurry, and the pad material and conditions.

Chemical/mechanical polishing is one of the techniques developed by the industry that has allowed production of larger wafers. CMP is used in the wafer fabrication process to flatten wafer surfaces after the buildup of new layers creates uneven surfaces. In this application, CMP is the abbreviation for chemical mechanical *planarization.* A detailed explanation of this use of CMP appears in Chapter 10.

Backside Processing

In most cases, only the front side of the wafer goes through the extensive chem/mech polishing. The backs may be left rough or etched to a bright appearance. For some device use, the backs may receive a special process to induce crystal damage, called *backside damage.* Backside damage causes the growth of dislocations that radiate up into the wafer. These dislocations can act as a trap of mobile ionic contamination introduced into the wafer during the fab process. The trapping phenomenon is called *gettering* (Fig. 3.23). Sandblasting of the back-

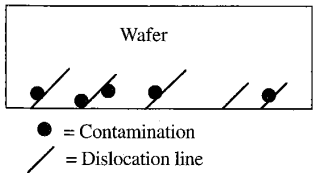


Figure 3.23 Trapping.

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side is another standard technique. Other methods include the deposition of a polysilicon layer or silicon nitride layer on the back.

Double-Sided Polishing

One of the many demands on larger diameter wafers is flat and parallel surfaces. Most manufacturers of 300-mm diameter wafers employ double-sided polishing to achieve flatness specifications of 0.25 to 0.18 μm over 25 × 25 mm sites.[5] A downside is that all further processing must employ handling techniques that do not scratch or contaminate the backside.

Edge Grinding and Polishing

Edge grinding is a mechanical process that leaves the wafer with a rounded edge (Fig. 3.24). Chemical polishing is employed to further create an edge that minimizes edge chipping and damage during fabrication that can result in wafer breakage or serve as the nucleus for dislocation lines.

Wafer Evaluation

Before packing, the wafers (or samples) are checked for a number of parameters as specified by the customer. Figure 3.25 illustrates a typical wafer specification.

Primary concerns are surface problems such as particulates, stain, and haze. These problems are detected with the use of high-intensity lights or automated inspection machines.



Figure 3.24 Wafer edge grinding.

Typical 200 mm Wafer Specification	
Diameter	200mm
Diam. Tolerance	0.25mm
Thickness	725 +/- μ
Crystal Orientation	<100> +/- 1 degree
Resistivity	2.7-4 Ω-cm
Res. Gradient	10%
Oxygen	25-29 ppma
Oxygen Gradient	5%
Carbon	0.3 ppma

Figure 3.25 Typical 200-mm wafer specification.

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Oxidation

Silicon wafers may be oxidized before shipment to the customer. The silicon dioxide layer serves to protect the wafer surface from scratches and contamination during shipping. Most companies start the wafer fabrication process with an oxidation step, and buying the wafers with an oxide layer saves a manufacturing step. Oxidation processes are explained in Chapter 7.

Packaging

While much effort goes into producing a high-quality and clean wafer, the quality can be lost during shipment to the customer or, worse, from the packaging method itself. Therefore, there is a very stringent requirement for clean and protective packaging. The packaging materials are of nonstatic, nonparticle-generating materials, and the equipment and operators are grounded to drain off static charges that attract small particles to the wafers. Wafer packaging takes place in cleanrooms.

Engineered Wafers (Substrates)

Increasingly, wafer fabrication companies are asking for wafer manufacturers to supply wafers with deposited top-side layers, such as epitaxial silicon. Other wafer products include silicon deposited on insulators (SOI and SOS) such as sapphire or diamond (Chapter 12).

Review Questions

1. In a polycrystalline structure, the atoms are not arranged (true or false).
2. In a single-crystal structure, the unit cells are not arranged (true or false).
3. Draw a cubic unit cell and identify the ⟨100⟩ plane.
4. ⟨111⟩ oriented wafers are used for (bipolar, MOS) devices.
5. What is the orientation of a semiconductor crystal if the seed has a ⟨100⟩ orientation.
6. Draw a diagram of a CZ crystal grower and identify all the major parts.
7. During crystal growth, the molten material is changed from single crystal structure to a polycrystal structure (true or false).
8. Why are wafers edge rounded?

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9. Draw a flow diagram of the wafer preparation process.
10. Give two reasons why semiconductor wafers require a flat surface.

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2. Sumitomo Sitix product brochure.
3. R. E. Williams, *Gallium Arsenide Processing Techniques,* Artech House Inc., Dedham MA, 1984, p. 37.
4. S. J. Brunkhorst and D. W. Sloat, "The impact of the 300-mm transition on silicon wafer suppliers," *Solid State Technology,* January 1998, p. 87.
5. *Ibid.*

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Chapter

4

Overview of Wafer Fabrication

Overview

This chapter will introduce the four basic processes used in the wafer fabrication to form the electrical elements of an integrated circuit in and on the wafer surface. Circuit design is traced from the functional diagram to the production of photomasks and reticles. Wafer and chip features and terminology are detailed. Finally, a flow diagram for the fabrication of a simple semiconductor device is presented.

Objectives

Upon completion of this chapter, you should be able to:

1. Identify and explain the four basic wafer operations.
2. Identify the parts of a wafer.
3. Draw a flow diagram of the circuit-design process.
4. Explain the definition and use of a composite drawing and mask set.
5. Draw cross sections showing the doping sequence of basic operations.
6. Draw cross sections showing the metallization sequence of basic operations.
7. Draw cross sections showing the passivation sequence of basic operations.
8. Identify the "parts" of an integrated circuit chip.

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Goal of Wafer Fabrication

The four stages of microchip manufacturing are materials preparation, crystal growth and wafer preparation, wafer fabrication, and packaging. The first two stages have been explored in Chapter 3. In this chapter, the fundamentals of stage 3, wafer fabrication, are explained.

Wafer fabrication is the manufacturing processes used to create the semiconductor devices in and on the wafer surface. The polished starting wafers come into fabrication with blank surfaces and exit with the surface covered with hundreds of completed chips (Fig. 4.1).

Wafer Terminology

A completed wafer is illustrated in Fig. 4.2. The regions of a wafer surface are:

1. Chip, die, device, circuit, microchip, or bar. All of these terms are used to identify the microchip patterns covering the majority of the wafer surface.
2. Scribe lines, saw lines, streets, and avenues. These areas are spaces between the chips that allow separation of the chip from the wafer. Generally, the scribe lines are blank, but some companies place alignment targets, or electrical test structures (see photomasking) in them.
3. Engineering die, test die. These chips are different from the regular device or circuit die. They contain special devices and circuit elements that allow electrical testing during the fabrication processing for process and quality control.
4. Edge chips. The edges of the wafer contain partial chip patterns that are wasted space. Larger chips on the same diameter wafer

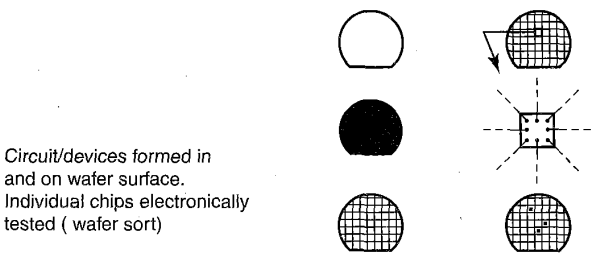


Figure 4.1 Wafer fabrication and wafer sort.

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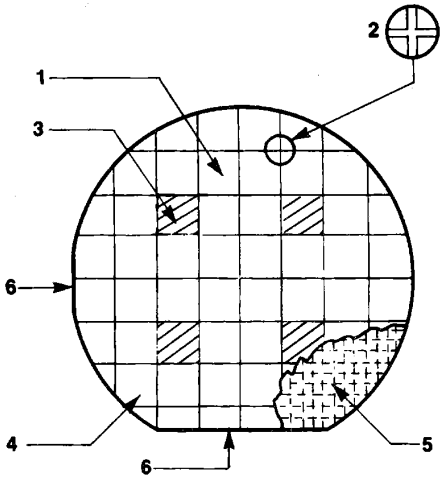


Figure 4.2 Wafer terminology.

result in large numbers of partial chips. Larger-diameter wafers minimize the amount of wasted space from larger chips.

5. Wafer crystal planes. The cutaway section illustrates the crystal structure of the wafer under the circuit layers. The diagram shows that the chip edges are oriented to the wafer crystal structure.
6. Wafer flats/notches. Wafers come from the wafer preparation stage with flats that indicate information about the crystal orientation and doping polarity of the wafer. Longer flats are called *major flats,* and shorter flats are called *minor flats.* The depicted wafer has a major and minor flat, indicating that it is a P-type ⟨100⟩ oriented wafer (see Chapter 3 for the flat code). Three-hundred-millimeter diameter wafers use notches as crystal orientation indicators. The flats and notches also assist alignment of the wafer in a number of the wafer fabrication processes.

Basic Wafer-Fabrication Operations

There are hundreds of thousands of different microchip types and functions. However, they are made with a small number of basic structures (primarily bipolar or MOS structures, see Chapter 16) and manufacturing processes. An analogy is the auto industry. This industry produces a wide variety of products, from sedans to bulldozers. Yet the processes of metal forming, welding, painting, and so on are common to all plants. Within the plant, these basic processes are applied in different ways to produce the desired product.

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The same is true in microchip fabrication. Companies use four basic operations in an infinite number of sequences and variations to produce specific microchips. They are layering, patterning, doping, and heat treatments (Fig. 4.3). Figure 4.4 illustrates how the four operations could be used to form a doped region in the wafer surface and contact it with a conductive layer of metal. A cross section of a simple metal oxide substrate (MOS) silicon gate transistor illustrates how these basic operations are used to create a real-life semiconductor device.

Layering

Layering is the operation used to add thin layers to the wafer surface. An examination of the simple MOS transistor structure in Fig. 4.4 shows a number of layers that have been added to the wafer surface. These layers could be insulators, semiconductors, or conductors. They are of different materials and are grown or deposited by a variety of processes.

The major techniques are grown silicon dioxide layers and deposition (Fig. 4.5) of a variety of materials. Common deposition techniques are physical vapor deposition (PVD), chemical vapor deposition (CVD), evaporation, and sputtering. Electroplating is used to deposit gold metallization on high density integrated circuits. Figure 4.6 lists common layer materials and layering processes. The details of each are explained in the process chapters. The role of the different layers in the structures is explained in Chapter 16.

Patterning

Patterning is the series of steps that results in the removal of selected portions of the added surface layers (Fig. 4.7). After removal, a *pattern* of the layer is left on the wafer surface. The material removed may be in the form of a hole in the layer or just a remaining island of the material.

The patterning process is known by the names photomasking, masking, photolithography, and microlithography. During the wafer fabrication process, the various physical *parts* of the transistors, diodes, capacitors, resistors, and metal conduction system are formed in and on the wafer surface. These parts are created one layer at a time by the combination of putting a layer on the surface and removing portions, with a patterning process, to leave a specific shape. The goal of the patterning operation is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other *parts*.

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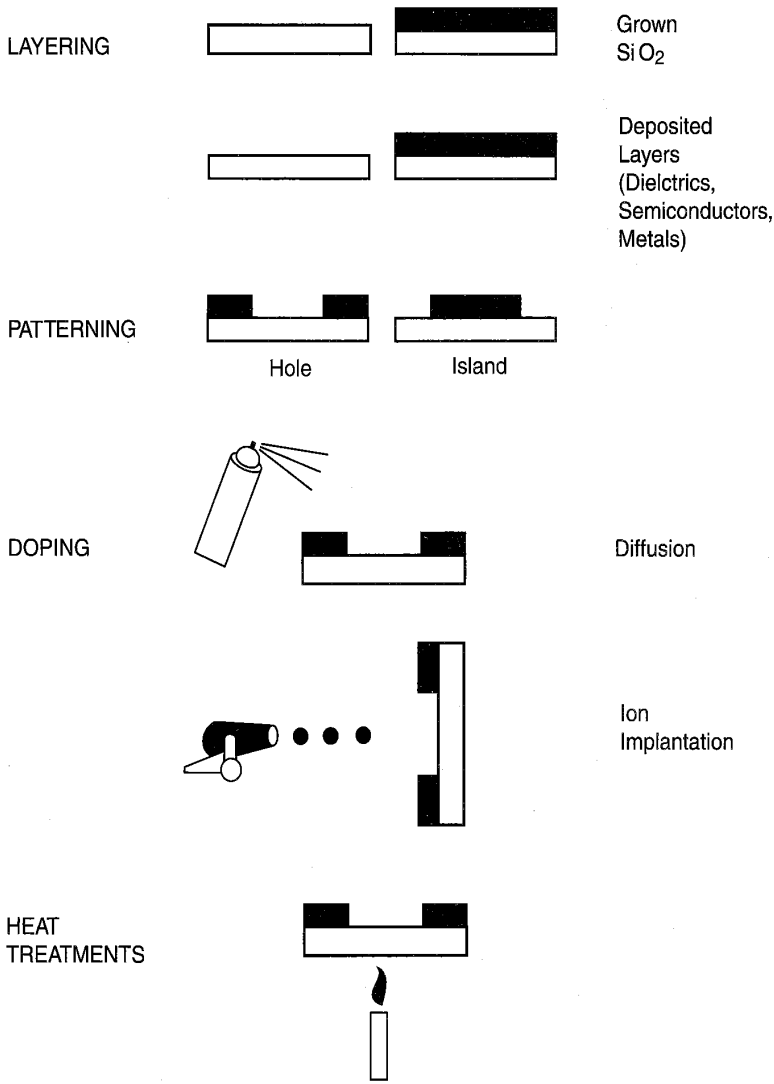


Figure 4.3 Basic wafer-fabrication operations.

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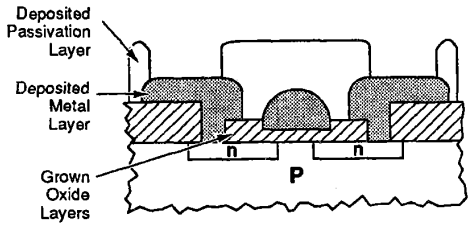


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

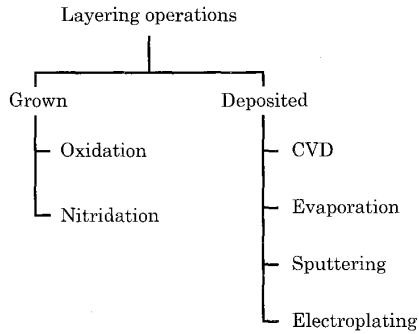


Figure 4.5 Layering operations.

Patterning is the most critical of the four basic operations. This operation sets the critical dimensions of the devices. Errors in the patterning process can cause distorted or misplaced patterns that result in changes in the electrical functioning of the device/circuit. Misplacement of the pattern can have the same bad results. Another problem is defects. Patterning is a high-tech version of photography but performed at incredibly small dimensions. Contamination in the process steps can introduce defects. This contamination problem is magnified by the fact that patterning operations are performed on the wafer from 5 to 20 or more times in the course of the wafer-fabrication process.

Doping

Doping is the process that puts specific amounts of electrically active dopants in the wafer surface through openings in the surface layers

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Layers	Thermal oxidation	Chemical vapor deposition	Evaporation	Sputtering	Electroplating
Insulators	silicon dioxide	silicon dioxide		silicon dioxide	
		silicon nitride		silicon monoxide	
Semiconductors		epitaxial silicon			
		polycrystalline silicon			
Conductors			aluminum	aluminum	gold
			aluminum alloys	aluminum alloys	copper
			nichrome	tungsten	
			gold	titanium	
				molybdenum	

Figure 4.6 Table of layers, processes, and materials.

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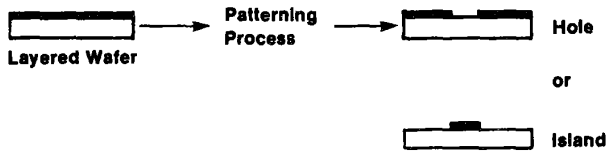


Figure 4.7 Patterning.

(Fig. 4.8). The two techniques are *thermal diffusion* and *ion implantation*, which are detailed in Chapter 11.

Thermal diffusion is a chemical process that takes place when the wafer is heated to the vicinity of 1000°C and is exposed to vapors of the proper dopant. A common example of diffusion is the spreading deodorant vapors into a room after being released from a pressurized can. Dopant atoms in the vapor move into the exposed wafer surface through the chemical process of diffusion to form a thin layer in the wafer surface. In microchip applications, diffusion is also called solid-state diffusion, since the wafer material is a solid. Diffusion is a chemical process.

Ion implantation is a physical process. Wafers are loaded in one end of an implanter and dopant sources (usually in gas form) in the other end. At the source end, the dopant atoms are ionized (given an electrical charge), accelerated to a high speed, and swept across the wafer surface. The momentum of the atoms carries them into the wafer surface, much like a ball shot from a cannon lodges in a wall.

The purpose of the doping operation is to create pockets in the wafer surface (Fig. 4.9) that are either rich in electrons (N-type) or rich in electrical holes (P-type). These pockets form the electrically active regions and N-P junctions required for operation of the transistors, diodes, capacitors, and resistors in the circuit.

Heat treatments

Heat treatments are the operations in which the wafer is simply heated and cooled to achieve specific results (Fig. 4.10). In the heat

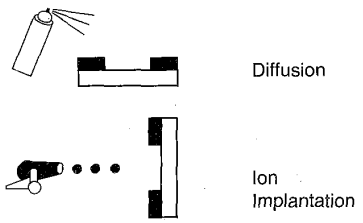


Figure 4.8 Doping techniques: diffusion and ion implantation.

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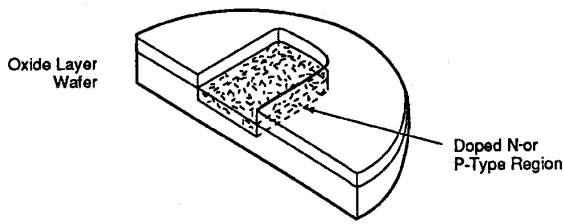


Figure 4.9 Formation of N- or P-type region in wafer surface.

Operation	Heat treatment
Patterning	Soft bake Hard bake Post exposure bake (develop)
Doping	Post ion implant anneal
Layering	Post metal deposition and patterning anneal

Figure 4.10 Table of major heat treatments.

treatment operations, no additional material is added or removed from the wafer, although contaminates and vapors may evaporate from the wafer surface.

An important heat treatment takes place after ion implantation. The implantation of the dopant atoms causes a disruption of the wafer crystal structure that is repaired by a heat treatment, called *anneal*, at about 1000°C. Another takes place after the conducting stripes of metal are formed on the wafer. These stripes carry the electrical current between the devices in the circuit. To ensure good electrical conduction, the metal is "alloyed" to the wafer surface by a heat treatment, which takes place at 450°C. A third important heat treatment is the heating of wafers with photoresist layers to drive off solvents that interfere with accurate patterning.

Circuit design

Circuit design is the first step in creation of a microchip. A circuit designer starts with a block functional diagram of the circuit such as the logic diagram in Fig. 4.11. This diagram lays out the primary functions and operation required of the circuit. Next, the designer translates the functional diagram to a schematic diagram (Fig. 4.12). This diagram identifies the number and connection of the various circuit

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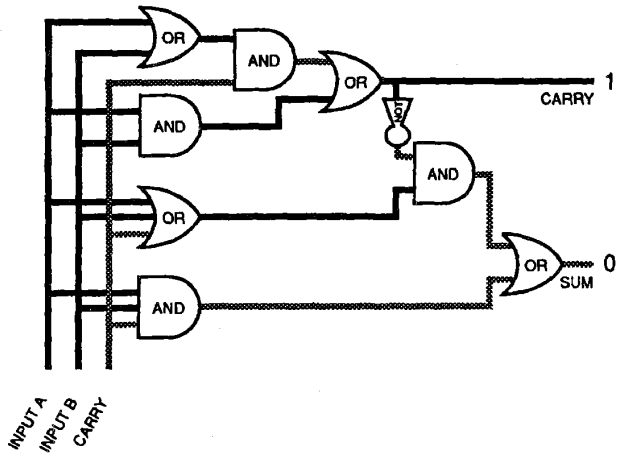


Figure 4.11 Example functional logic design of a simple circuit.

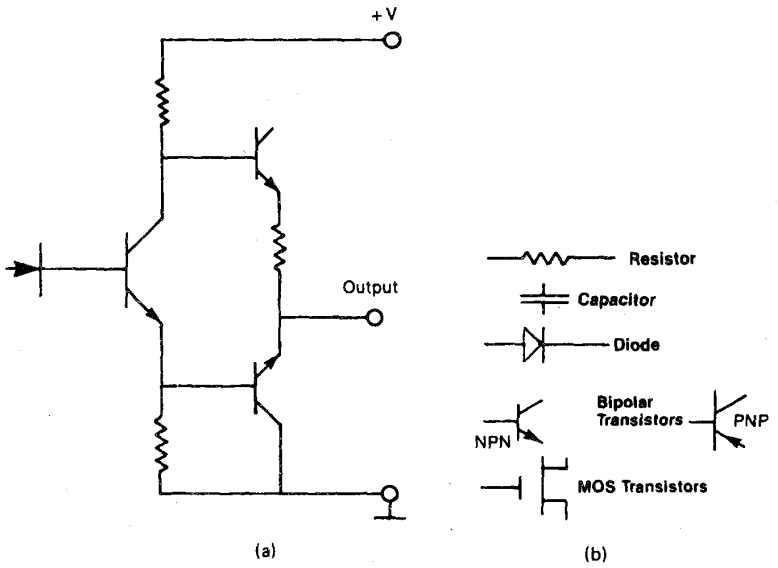


Figure 4.12 Example circuit schematic diagram with component symbols.

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components. Each component is represented by a symbol. Accompanying the schematic diagram are the electrical parameters (voltage, current, resistance, and so forth) required to make the circuit work.

The third step, circuit layout, is unique to semiconductor circuits. Circuit operation is dependent on a number of factors, including material resistivity, material physics, and the physical dimensions of the individual component "parts." The placement of the parts relative to each other is another factor. All these considerations dictate the physical layout and dimensions of the part/device/circuit. Layout starts with using sophisticated computer-aided design (CAD) systems to translate each circuit component into its physical shape and size. Through the CAD system, the circuit is built, exactly duplicating the final design. The result is a composite picture of the circuit surface showing all of the sublayer patterns. This drawing is called a *composite* (Fig. 4.13). The composite drawing is analogous to the blueprint of a multistory office building as viewed from the top and showing all of

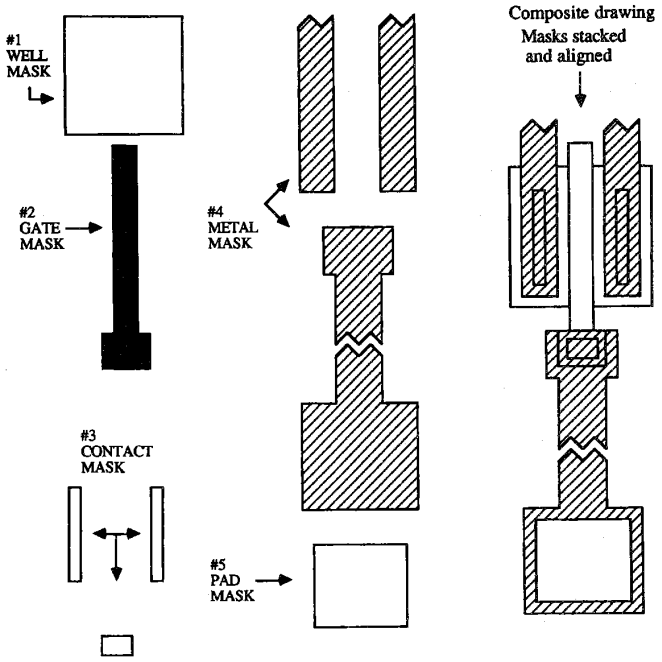


Figure 4.13 Composite and layer drawings for five-mask silicon gate transistor.

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the floors. However, the composite is many times the dimensions of the final circuit.

Both buildings and semiconductor circuits are built one layer at a time. Therefore, it is necessary to separate the composite drawing into the layout for each individual layer in the circuit. Figure 4.13 illustrates the composite and individual layer patterns for a simple silicon gate MOS transistor.

Each layer drawing is digitized (digitizing is the translation of the layer drawings to a digital data base) and plotted on a computerized *X–Y* plotting table.

Reticle and masks

The patterning process is used to create the required layer pattern and dimensions in and on the wafer surface. Getting the pattern from the digitized pattern to the wafer surface requires several steps. For the photo processes, there is an intermediate step called a reticle. A reticle is a "hard copy" of the individual drawing recreated in a thin layer of chrome deposited on a glass or quartz plate (Fig. 4.14*a*). The

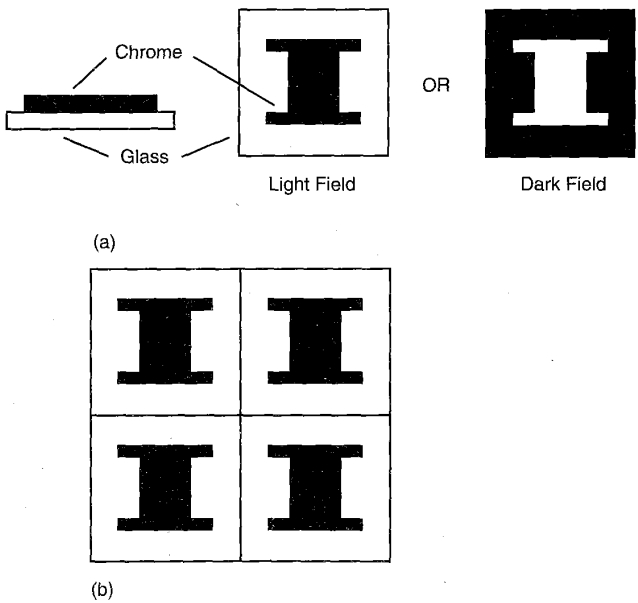


Figure 4.14 (*a*) Chrome on glass reticle and (*b*) photomask of the same pattern.

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reticle may be used directly in the patterning process or may be used to produce a photomask. A photomask is also a glass plate with a thin chrome layer on the surface. After production, it is covered with many copies of the circuit pattern (Fig. 4.14*b*). It is used to pattern a whole wafer surface in one pattern transfer. (Reticle and mask-making processes are detailed in Chapter 11.)

Reticles and masks are produced in a separate department or are purchased from outside vendors. They supply the fabrication area with a separate set of reticles or set of masks (*mask set*) for each circuit type.

Example Fabrication Process

The manufacture of a circuit starts with a polished wafer. The cross section sequence in Fig. 4.15 shows the basic operations required to form a simple MOS silicon-gate transistor structure. The following is an explanation of each operation in the fabrication process.

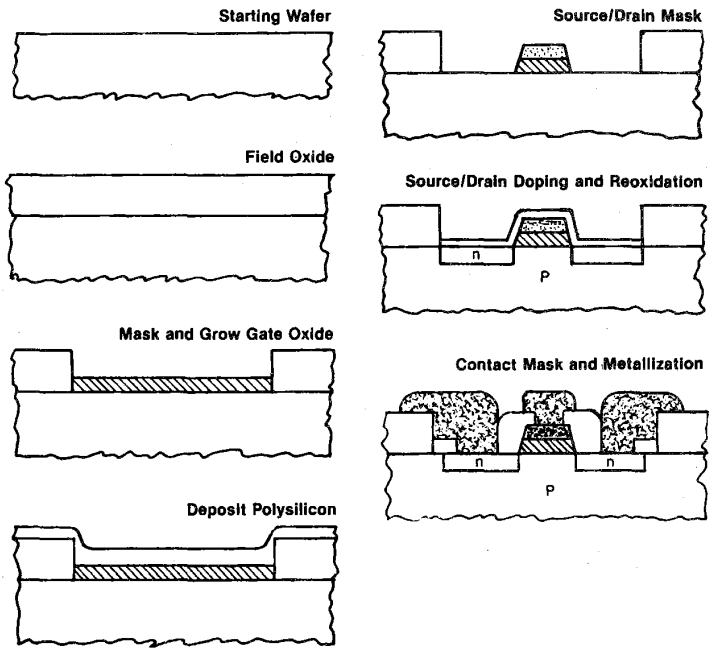


Figure 4.15 Silicon gate MOS process steps.

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Step 1: Layering Operation. The building starts with an oxidation of the wafer surface to form a thin protective layer and to serve as a doping barrier. This silicon dioxide layer is called the *field oxide.*

Step 2: Patterning Operation. The patterning process leaves a hole in the field oxide that defines the location of the source, gate, and drain areas of the transistor.

Step 3: Layering Operation. Next, the wafer goes to an silicon dioxide oxidation operation. A thin oxide is grown on the exposed silicon. It will service as the gate oxide.

Step 4: Layering Operation. In step 4, another layering operation is used to deposit a layer of polycrystalline (poly) silicon. This layer will also become part of the gate structure.

Step 5: Patterning Operation. Two openings are patterned in the oxide/polysilicon layer to define the source and drain areas of the transistor.

Step 6: Doping Operation. A doping operation is used to create an N-type pocket in the source and drain areas.

Step 7: Layering Operation. Another oxidation/layering process is used to grow a layer of silicon dioxide over the source/drain areas.

Step 8: Patterning Operation. Holes, called contact holes, are patterned in the source, gate, and drain areas.

Step 9: Layering Operation. A thin layer of conducting metal, usually an aluminum alloy, is deposited over the entire wafer.

Step 10: Patterning Operation. After deposition, the wafer goes back to the patterning area where portions of the metallization layer are removed from the chip area and the scribe lines. The remaining portions connect all the parts of the surface components to each other in the exact pattern required by the circuit design.

Step 11: Heat Treatment Operation. Following the metal patterning step, the wafer goes through a heating process in a nitrogen gas atmosphere. The purpose of the step is to "alloy" the metal to the exposed source and drain regions and the gate region to ensure good electrical contact.

Step 12: Layering Operation. The final layer of this device is a protective layer known variously as a *scratch* or *passivation layer.* Its purpose is to protect the components on the chip surface during the testing and packaging processes, and during use.

Step 13: Patterning Operation. The last step in the sequence is a patterning process that removes portions of the scratch protection layer over the metallization terminal pads on the periphery of the chip. This step is known as the *pad mask.*

The 13-step process illustrates how the four basic fabrication operations are used to build a particular transistor structure. The other

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components (diodes, resistors, and capacitors) required for the circuit are formed in other areas of the circuit as the transistors are being formed. For example, in this sequence, resistor patterns are put on the wafer at the same time as the source/drain pattern for the transistor. The subsequent doping operation creates the source/drain *and* the resistors. Other transistor types, such as bipolar and silicon gate MOS, are formed by the same basic four operations but using different materials and in different sequences.

In general, the circuit components are formed in the first series of fabrication operations and referred to as the *front end of the line* (FEOL). In the later series of operations, the various metallization layers that connect the circuit components are added to the wafer surface. These operations are called the *back end of the line* (BEOL).

Modern chip structures are many times more complicated than the simple process just described. They have multiple layers and pockets of dopants, numbers of layers added to the surface, including multiple layers of conductors interspersed with dielectrics (Fig. 4.16).

Achieving these complicated structures requires many processes. An each process, in turn, requires a number of steps and substeps. A speculative process for a 64-Gb CMOS device might require 180 major

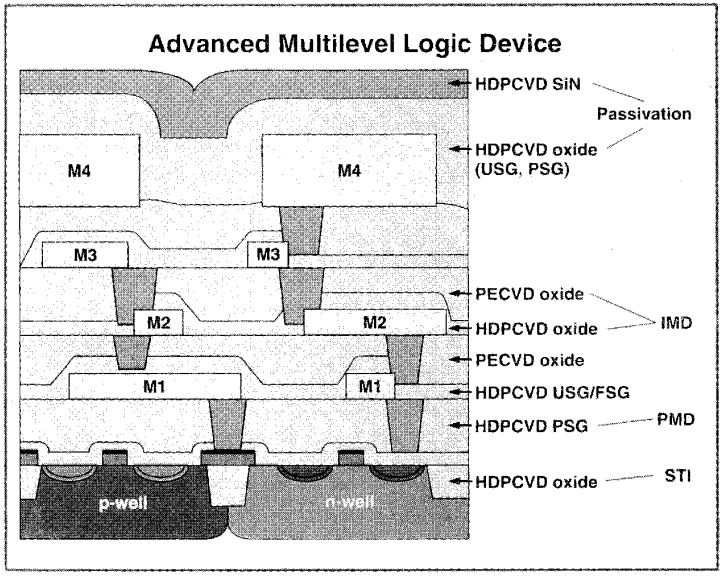


Figure 4.16 Modern chip structure.

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steps, 52 clean/strips, and up to 28 masks.[1] Yet all of the major steps are one of the four basic operations. Figure 4.17 lists the basic operations and the principle process options used for each. By the time the industry reaches circuits with gate widths of several atoms and stacks of metal on top of the circuit, the number of process steps will be in the 500, or higher, range.

Basic Operation	Process	Options
Layering	Oxidation	Atmospheric
		High Pressure
		Rapid Thermal Oxidation (RTO)
	Chemical Vapor Deposition (CVD)	Atmospheric Pressure
		Low Pressure (LPCVD)
		Plasma Enhanced (PECVD)
		Vapor Phase Epitaxy (VPE)
		Metaloranic CVD (MOCVD)
	Molecular Beam Epitaxy (MBE)	
	Physical Vapor Deposition (PVD)	Vacuum Evaporation
		Sputtering
Patterning	Resist	Positive
		Negative
	Exposure Systems	Contact
		Proximity
		Scanning Projection
		Stepper
	Exposure Sources	High Pressure Mercury
		X-Rays
		E-Beams
	Imaging Processes	Single Layer Resist
		Multilayer Resist
		Antireflecting layers
		Off-Axis Illumination
		Annular Ring Illumination
		Planarization
		Contrast Enhancement
	Etch	Wet Chemistry-Liquid/vapor
		Dry (Plasma)
		Lift-Off
		Ion Milling
		Reactive Ion Etch (RIE)
Doping	Diffusion	Open Tube-Horizontal/Vertical
		Closed Tube
		Rapid Thermal Processing (RTP)
	Ion Implantation	Medium/High Current
		Low/High Voltage (energy)
Heating	Thermal	Hot Plates
		Convection
		RTP
	Radiation	Infrared (IR)

Figure 4.17 Summary of wafer-fab operations/processes.

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Chip Terminology

Figure 4.18 depicts a photomicrograph of an MSI/bipolar integrated circuit. The level of integration was chosen so that some surface details could be seen. The components of higher-density circuits are so small that they cannot be distinguished on a photomicrograph of the entire chip. The chip features are:

1. A bipolar transistor
2. The circuit designation number
3. Bonding pads for connecting the chip into a package
4. A piece of contamination on a bonding pad
5. Metallization lines
6. Scribe (separation) lines
7. Unconnected component
8. Mask alignment marks
9. Resistor

Wafer Sort

Following the wafer fabrication process comes a very important testing step: wafer sort. This test is the report card on the fabrication process. During the test, each chip is electrically tested for electrical performance and circuit functioning. Wafer sort is also known as *die sort* or *electrical sort.*

For the test, the wafer is mounted on a vacuum chuck and aligned to thin electrical probes that contact each of the bonding pads on the chip (Fig. 4.19). The probes are connected to power supplies that test the circuit and record the results. The number, sequence, and type of tests are directed by a computer program. Wafer probers are automated so that, after the probes are aligned to the first chip (manually or with an automatic vision system), subsequent testing proceeds without operator assistance.

The goal of the test is threefold. First is the identification of working chips before they go into the packaging operation. Second is characterization of the device/circuit electrical parameters. Engineers need to track the parameter distributions to maintain process quality levels. The third goal is an accounting of the working and nonworking chips to give fab personnel feedback on overall performance. The location of the working and nonworking chips is logged into a wafer map in the computer. Older technologies deposit a drop of ink on the *nonworking* chips.

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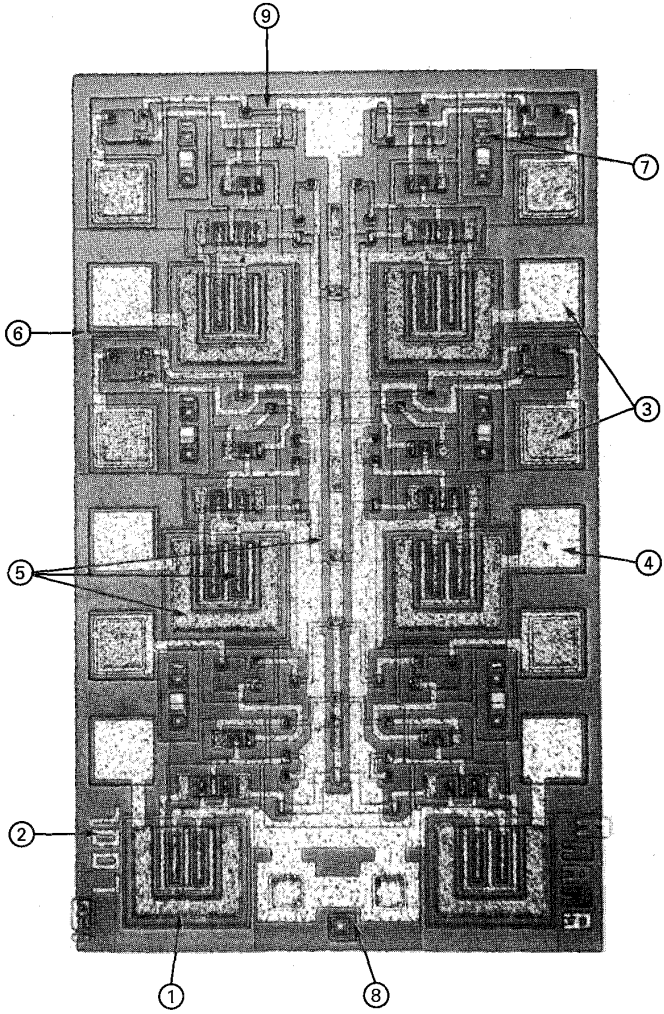


Figure 4.18 Chip terminology.

Wafer sort is one of the principal yield calculations in the chip production process. It also gets more expensive as the chips get larger and denser.[2] These chips require more time to probe, and power supplies, wafer handling mechanics, and computer systems have to be more sophisticated to perform the tests and track results. The vision systems

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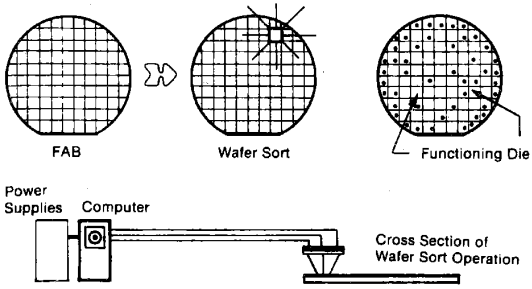


Figure 4.19 Wafer sort.

must also evolve in sophistication (and cost) with expanding die size. Cutting the chip test time is also a challenge. Chip designers are being asked to include test modes for memory arrays. Test designers are exploring ways to streamline test sequences using stripped-down tests once the chip is fully characterized, performing scan tests of the circuit, and parallel testing different circuit parts. The details of wafer parameter yield are addressed in Chapter 6.

Packaging

Most wafers continue on to stage four, called *packaging* (Fig. 4.20). The wafers are transferred to a packaging area on the same site or to a remote location. Many semiconductor producers package their chips in offshore facilities. (Chapter 18 details the packaging process.) In this stage, the wafers are separated into the individual chips, and the working chips are incorporated into a protective package. Some chips are directly incorporated into electrical systems without a package.

Summary

The semiconductor microchip fabrication process is long, complicated, and includes many variations, depending on the type of product, level of integration, feature size, and other factors. Understanding a particular process is easier by separating it into the four stages. Wafer fabrication is further understood by identifying the four basic operations performed on the wafer. Several simple processes have been used to illustrate the basic wafer fabrication operations. Actual processes used are addressed in the process chapters and in Chapters 16 and 17. Industry drivers and manufacturing trends are explained in Chapter 15.

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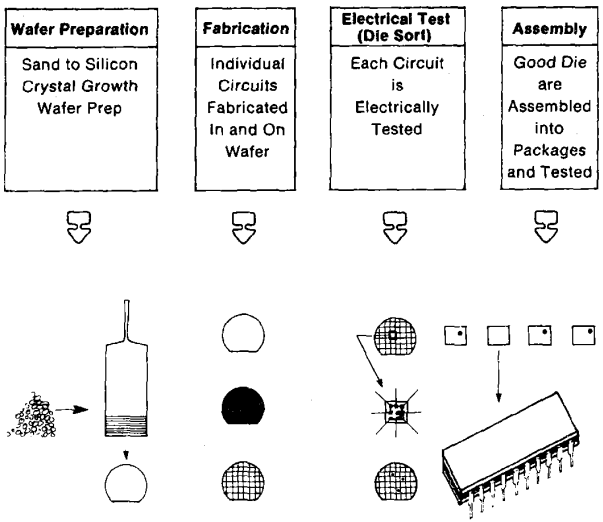


Figure 4.20 Integrated circuit manufacturing sequence.

Review Questions

1. Name one layering technique.
2. Which basic operation uses the ion implant technique?
3. List the four basic wafer fabrication operations.
4. Draw and label cross sections for a oxidation/patterning/doping sequence.
5. Describe a composite drawing.
6. Which basic operation uses a photomask?
7. What parameter is tested at wafer sort (wafer thickness, defect density, circuit function)?
8. What step in the circuit design process uses a CAD system?
9. What is the purpose of a chip package?
10. What is the role of the holes created in the contact mask step?

References

1. R. Kopp, *Kopp Semiconductor Engineering,* September 1996.
2. R. Iscoff, "VLSI Testing: The Stakes Get Higher," *Semiconductor International,* September 1993, p. 58.

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Chapter

5

Contamination Control

Overview

The effects of contamination on device processing, device performance, and device reliability are explained are identified along with the types and sources of contamination found in a fabrication area. Cleanroom layouts, major contamination-control procedures, and wafer surface cleaning techniques are explained.

Objectives

Upon completion of this chapter, you should be able to:

1. Identify the three major effects of contamination on semiconductor devices and processing.
2. List the major sources of contamination in a fabrication area.
3. Define the "class number" of a cleanroom.
4. List the particle density of class 100, 10, and 1 fabrication areas.
5. Describe the role of positive pressure, air showers, and adhesive mats in maintaining cleanliness levels.
6. List at least three techniques used to minimize contamination from fabrication personnel.
7. Identify the three contaminants present in "normal" water, and their control in semiconductor plants.
8. Describe the differences between normal industrial chemicals and semiconductor-grade chemicals.
9. Name two problems associated with high static levels, and two methods of static control.

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10. Describe a typical FEOL and BEOL wafer cleaning process.
11. List typical wafer rinsing techniques.

Introduction

One of the first problems to plague the infant microchip fabrication efforts was contamination. The industry started with a cleanroom technology developed by the space industry. However, these techniques proved inadequate for large-scale manufacturing of chips. Cleanroom technology has had to keep pace with chip design and density evolution. The ability of the industry to grow has been dependent on keeping up solving contamination problems presented by each generation of chips. Yesterday's minor problems become the killer defects of today's chips.

The problem

Semiconductor devices are very vulnerable to many types of contaminants. They fall into five major classes.

1. Particles
2. Metallic ions
3. Chemicals
4. Bacteria
5. Airborne molecular contaminants (AMCs)

Particles. Semiconductor devices, especially dense integrated circuits, are vulnerable to all kinds of contamination. The sensitivity is due to the small feature sizes and the thinness of deposited layers on the wafer surface. These dimensions are down to the submicron range. A micron or micrometer (μm) is very small. A centimeter contains 10,000 μm. Another way to envision a micron is that a human hair is about 100 μm in diameter (Fig. 5.1). The small physical dimensions of the devices make them very vulnerable to particulate contamination in the air coming from workers, generated by the equipment, and present in processing chemicals (Fig. 5.2). As the feature size and films become smaller (Fig. 5.3), the allowable particle size must be controlled to smaller dimensions.

A rule of thumb is that the particle size must be ten times smaller than the minimum feature size.[1] A 0.30-μm feature size device is vulnerable to 0.03-μm diameter particles. Particles that locate in a critical part of the device and destroy its functioning are called *killer defects.* Killer defects also include crystal defects and other process-

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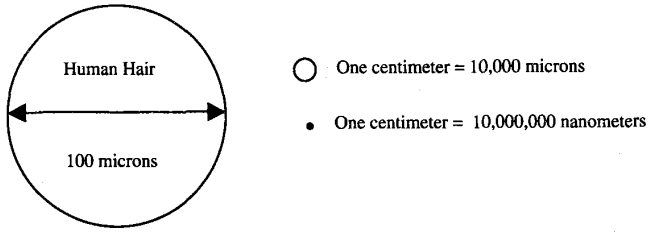


Figure 5.1 Relative sizes.

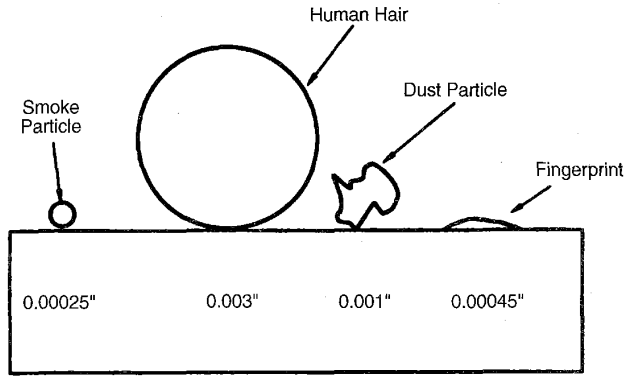


Figure 5.2 Relative size of contamination. (*Source:* Hybrid Microcircuit Technology Handbook.[12])

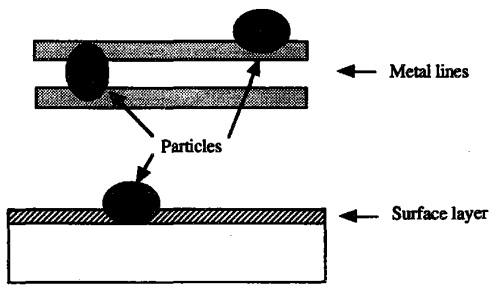


Figure 5.3 Relative size of airborne particles and wafer dimensions.

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induced problems. On any wafer, there are a number of particles. Some are the killer variety, but others locate in less sensitive areas and do no harm. The 1994 *Semiconductor Industry Association (SIA) National Technology Roadmap for Semiconductors* (NTRS) calls for defect densities for pattering operations for 0.18-μm design rules to be 135 per layer/m^2 at a 0.06-μm defect size.

Metallic ions. In Chapter 2, it was established that semiconductor devices require controlled resistivity in the wafers and in the doped N- and P-regions, and precise N-P junctions. These three properties are achieved by the purposeful introduction of specific dopants into the crystal and into the wafer. These desired effects are achieved with very small amounts of the dopants. Unfortunately, it takes only a small amount of certain electrically active contaminants in the wafer to alter device electrical characteristics, changing performance and reliability parameters.

The contaminants causing these types of problems are known as *mobile ionic contaminants* (MICs). They are atoms of metals that exist in the material in an ionic form. Furthermore, these metallic ions are highly mobile in semiconductor materials. This mobility means that the metallic ions can move inside the device, even after passing electrical testing and shipping, causing the device to fail. Unfortunately, the metals (Fig. 5.4) that cause these problems in silicon devices are present in most chemicals. On a wafer, MIC contamination has to be in the 10^{10} atoms/cm^2 range or less.[2]

Sodium is the most prevalent mobile ionic contaminant in most untreated chemicals and is the most mobile in silicon. Consequently, control of sodium is a prime goal in silicon processing. The MIC problem is most serious in MOS devices, a fact that has led some chemical suppliers to develop MOS or low-sodium-grade chemicals. These labels refer to low mobile ionic contaminant levels.

Trace Metal Impurity	Parts per billion (ppb)
Sodium	50
Potassium	50
Iron	50
Copper	60
Nickel	60
Aluminum	60
Manganese	60
Lead	60
Zinc	60
Chlorides	1000

Figure 5.4 Example resist stripper trace metal contents *(EKC Technology–830 Photoresist stripper).*

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Chemicals. The third major contaminant in semiconductor process areas is unwanted chemicals. Process chemicals and process water can be contaminated with trace chemicals that interfere with the wafer processing. They may result in unwanted etching of the surface, create compounds that cannot be removed from the device, or cause nonuniform processes. Chlorine is such a contaminant and is rigorously controlled in process chemicals.

Bacteria. Bacteria is the fourth major contaminant class. Bacteria are organisms that grow in water systems and on surfaces that are not cleaned regularly. Bacteria, once on the device, act as particulate contamination or may contribute unwanted metallic ions to the device surface.

Airborne molecular contaminants. Airborne molecular contaminants (AMCs) are fugitive molecules that escape from the process tools or the chemical delivery systems, or are carried into the fabrication area on materials or personnel. Transfer of wafers from one process tool to another can carry hitchhiking molecules to the next tool. AMCs include all of the gasses, dopants, and process chemicals used in the fabrication area. These can be oxygen, moisture, organics, acids, bases, and others.[3]

Their harm is highest in processes that involve delicate chemical reactions, such the exposure of photoresist in the patterning operations. Other problems include the shifting of etch rates and unwanted dopants that shift device electrical parameters and change the wetting characteristics of etchants leading to incomplete etching.[4] Detecting and controlling AMCs is an emerging field that will need to reach maturity as device sizes continue to diminish as projected by the SIA's *International Roadmap for Semiconductor Technology* (IRST).

Contamination-caused problems

The five types of contaminants affect the processing and devices in three specific performance areas.

1. Device processing yield
2. Device performance
3. Device reliability

Device processing yield. Device processing in a contaminated environment can cause a multitude of problems. Contamination may change the dimensions of device parts, change the cleanliness of the surfaces,

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and/or cause pitted layers. Within the fabrication process are a number of quality checks and inspections specifically designed to detect contaminated wafers. Contamination caused defects contribute the to rejection of wafers in the wafer fabrication process, reducing the overall yield (see Chapter 6).

Device performance. A more serious problem is related to small pieces of contamination that may escape the in-process quality checks. Or unwanted chemicals and AMCs in the process steps may alter device dimensions or material quality. High levels of mobile ionic contaminants in the wafer can change the electrical performance of the devices. These problems usually show up at an electrical (called *wafer* or *die sort*) that checks each chip after the wafer fabrication process (see Chapter 6).

Device reliability. Loss of device reliability is the most insidious of the contamination failures. Small amounts of metallic contaminants can get into the wafer during processing and not be detected during normal device testing. However, in the field, these contaminants can travel inside the device and end up in electrically sensitive areas, causing failure. This failure mode is a primary concern of the space and defense industries.

In the rest of this chapter, the sources, nature, and control of the types of contamination that affect semiconductor devices are identified. With the advent of LSI level circuits in the 1970s, the control of contamination became essential to the industry. Since that time, a great deal of knowledge about and control of contamination has been learned. Contamination control is now a discipline of its own and is one of the critical technologies that have to be mastered to profitably produce solid-state devices.

Contamination control issues addressed in this chapter apply to wafer fabrication areas, mask-making areas, some chip packaging areas, and areas in which semiconductor equipment and materials are manufactured.

Contamination Sources

General sources

Contamination in a cleanroom is defined as anything that interferes with the production of the product and/or its performance. The stringent requirements of solid-state devices define levels of cleanliness that far exceed those of almost any other industry. Literally everything that comes in contact with the product during manufacture is a

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potential source of contamination. The major contamination sources are:

1. Air
2. The production facility
3. Cleanroom personnel
4. Process water
5. Process chemicals
6. Process gases
7. Static charge

Each source produces specific types and levels of contamination and requires special controls to render it acceptable in the cleanroom.

Air

Normal air is so laden with contaminants that it must be treated before entering a cleanroom. A major problem is airborne particles, referred to as *particulates* or *aerosols*. Normal air contains copious amounts of small dust and particles, as illustrated in Fig. 5.5. A major problem with small particles (called *aerosols*) is that they "float" and remain in the air for long periods of time. Air cleanliness levels in cleanrooms are identified by the particulate diameters and their density in the air.

Air quality is designated by the *class number* of the air in the area as defined in Federal Standard 209E.[5] This standard designates air quality in the two categories of particle size and density. The class

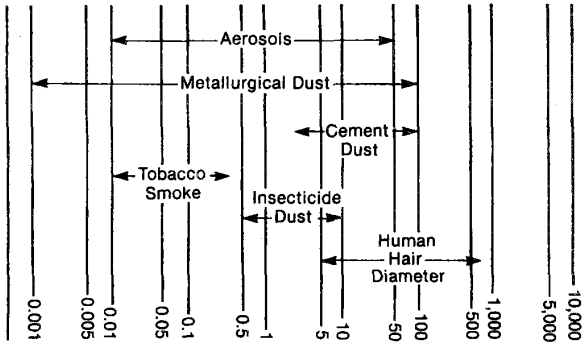


Figure 5.5 Relative size of airborne particulates (in microns).

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number of an area is defined as the number of particles 0.5 μm or larger in a cubic foot of air. The air in a typical city, filled with smoke, smog, and fumes, can contain up to 5 million particles per cubic foot, which is a class number of 5 million. Advancing chip sensitivity has identified smaller and smaller tolerable particle sizes for each generation of chip feature size.[6]

Figure 5.6 shows the relationship between particulate diameter and density as defined by Federal Standard 209E. Figure 5.7 lists the class numbers and associated particle size for various environments. Federal Standard 209E specifies cleanliness levels down to class 1 levels. While 209E defines class numbers at 0.5-μm particle size, successful wafer fabrication processing requires tighter controls. Engineers strive to achieve reduction of 0.3-μm particles in class 10 and class 1 environments. Specifications proposed by Semetech call for 64-Mbit memory process areas at class 0.1 and 256-Mbit air levels of class 0.01.[5]

Clean air strategies

The design of a cleanroom is integral to its ability to produce contamination-free wafers. A major consideration in the design is the maintenance of clean air in the process areas. Automation is also an important cleanroom strategy for the reduction of contamination. This issue is explored in the equipment section and in Chapter 15. Four distinct room design strategies are used:

1. Clean workstations
2. Tunnel design
3. Total cleanroom
4. Mini-environments

Cleanroom workstation strategy

The semiconductor industry adopted cleanroom techniques first developed by NASA to assemble space vehicles and satellites. However, the smallish cleanliness of rooms adequate for satellite assembly could not be maintained when expanded to larger fabrication areas with more production workers. The early semiconductor industry initially used ceiling and wall filters, which proved inadequate to keep the wafers clean. This problem was addressed with a cleanroom workstation strategy. This strategy focused on individual workstations with air filters and nonshedding materials. Outside the workstations, the wafers were stored and moved in covered boxes.

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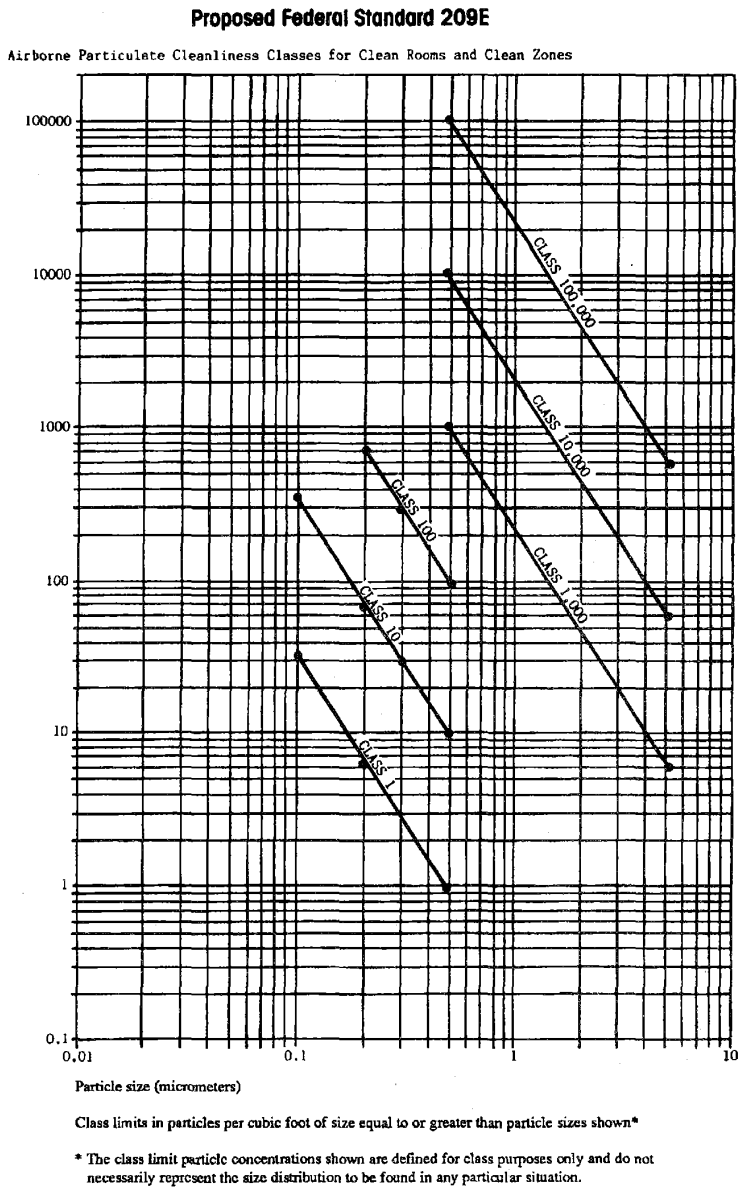


Figure 5.6 Air cleanliness class standard 209E.

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Environment	Class Number	Maximum particle size (micron)
Projected-256 Mbit	0.01	<<0.1
Mini environment	0.1	<0.1
ULSI Fab	1	0.1
VLSI Fab	10	0.3
VLF station	100	0.5
Assembly area	1000-10,000	0.5
House room	100000	
Outdoors	>500,000	

Figure 5.7 Typical class numbers for various environments.

The fabrication area consisted of a large room with the workstations (called *hoods*) arranged in rows so that the wafers could move sequentially through the process, never being exposed to dirty air. The filters in these clean hoods are either high-efficiency particulate attenuation (HEPA) filters or, for more demanding application, ultra-low-particle (ULPA) filters. These filters are constructed of fragile fibers with many small holes and are folded into the filter holder in an accordion design (Fig. 5.8). The high density of small holes and large area of the filter medium allow the passage of large volumes of air at low velocity. The low velocity contributes to the cleanliness of the hood by not causing air currents. The low velocity is also necessary for operator comfort. A typical airflow[6] is 90 to 100 ft/min. HEPA and ULPA filters achieve filtering efficiencies as high as 99.9999+ percent at 0.12-micron particle size.[7]

Typically, a clean hood (Fig. 5.9) has a HEPA/ULPA filter mounted in the top. Air is drawn from the room through a prefilter by a fan and forced through the HEPA filter. The air leaves the filter in a laminar pattern and, at the work surface, it turns and exits the hood. A shield directs the exiting air over the wafers in the hood. The formal name for the workstation is a *vertical laminar flow (VLF) station.* The term VLF is derived from the laminar nature of the airflow. Some worksta-

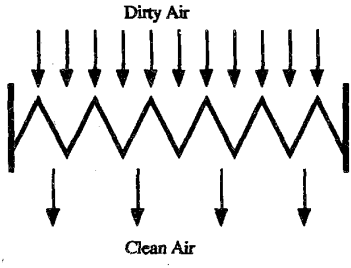


Figure 5.8 HEPA filter.

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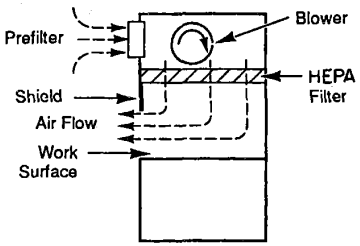


Figure 5.9 Cross section of VLF process section.

tions are designed with the HEPA filter in the back of the work surface. These stations are called *horizontal laminar flow (HLF) hoods.*

Both types of stations keep the wafers clean in two ways. First is the filtered air inside the hood. The second cleaning action is the slight positive pressure built up in the station. This pressure prevents airborne dirt from operators and from the aisle areas from entering the hood.

A special design of VLF hood is required for wet chemical processing stations (Fig. 5.10). These stations must be connected to an exhaust system to remove the chemical fumes. Removal designs include an exit port in the rear and/or exhaust ports around the lip of the process tanks (lip exhaust). The fumes can pose both safety and contamination problems. In this design, care must be taken to balance the VLF air and the exhaust to maintain the required class number in the station.

The clean-station strategy also applies to equipment in modern fabs. Individual tools must be fitted with a VLF- or HLF-designed hood to keep the wafers clean during loading and unloading steps.

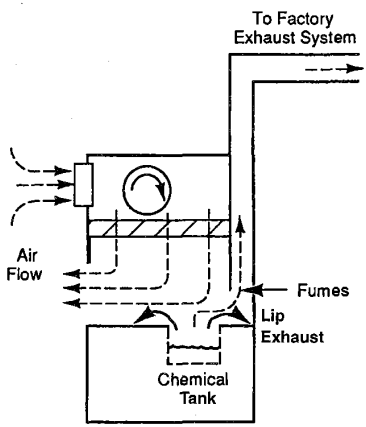


Figure 5.10 Cross section of a VLF exhaust process section.

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Tunnel/bay concept

As more critical particulate control became necessary, it was noted that the VLF hood approach had several drawbacks. Chief among them was the vulnerability to contamination from the many personnel moving about in the room. People entering and exiting the fabrication area had the potential of contaminating all the process stations in the area.

This particular problem is solved by dividing the fabrication area into separate tunnels or bays (Fig. 5.11). Instead of the individual VLF hoods, filters are built into the ceilings and serve the same purpose. The wafers are kept clean by the filtered air from the ceiling filters and are less vulnerable to personnel-generated contamination because of fewer workers in the immediate vicinity. On the downside, tunnel arrangements cost more to construct and are less versatile when the process changes.

Total cleanroom strategy

Developments in cleanroom design and filtering technology have allowed an evolution back to the open fabrication area (Fig. 5.12). In the latest version, air filtering is accomplished by HEPA filters in the ceiling with returns in the floor to give a continuous flow of clean air.

The workstations are tabletops with perforations to allow the filtered air to pass uninterrupted through the tabletop. This arrangement is often called a *ballroom* layout. Automation techniques used in wafer fabrication areas are presented in Chapter 15.

An important cleanroom parameter is recovery. This parameter is the time it takes for the filters to return the area to acceptable condi-

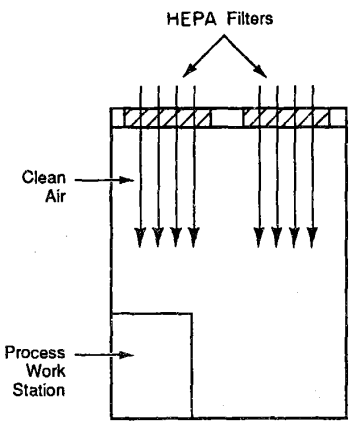


Figure 5.11 Cross section of a cleanroom tunnel.

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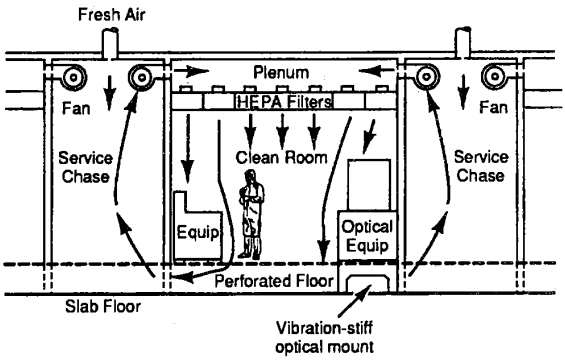


Figure 5.12 Cross section of a laminar flow cleanroom. *(Courtesy of Semiconductor International.)*

tions after a shift start, personnel break, or other disturbance. In a class 1 facility, the air may be turned over every six seconds.[9]

The trend of equipment and facility design has been to isolate the wafer from contamination sources. VLF hoods isolated the wafer from the room air, and tunnels isolate the wafer from excessive personnel exposure. The advent of CMOS ICs increased the number of process steps and the need to include more process stations in the cleanroom.

These larger rooms (and tunnels) bring with them the potential of contamination from the sheer volume of the air and the increased number of operators. These changes have driven the cost of cleanrooms up to several billion dollars.

Micro- and mini-environments

Projections in the mid-1980s showed increasing cleanroom costs with diminishing returns on effectiveness. The concept of isolating the wafer in as small an environment as possible became the new direction. This concept was already in place with steppers and other process tools that had build in clean *micro-environments* for wafer loading and unloading (Fig. 5.13).

The challenge was to string together a series of mini-environments such that the wafer was never exposed to the room air. Hewlett Packard developed a critical link with the invention, in the mid 1980s, of the *standard mechanical interface* (SMIF).[10] With SMIF, the traditional wafer box is replaced with a wafer enclosure (*mini-environment*) that can be pressurized with air or nitrogen to keep out room air. This approach took on the general name of *wafer isolation technology* (WIT) or a mini-environment system. There are three parts to the system:

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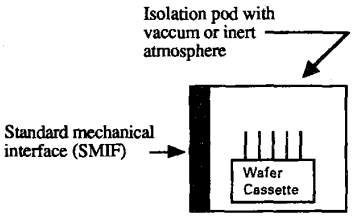


Figure 5.13 Wafer transfer micro-environment.

the wafer box or pod for transporting the wafers, the isolated microenvironment at the tool, and a mechanism for extracting and loading the wafers. The wafer *pod* features a mechanical interface that allows direct connection to the micro-environment of the process tool (Fig. 5.13). Wafers may be loaded directly from and to the pod onto the tool wafer system by dedicated handlers. Another approach is to move the cassette from the pod to the tool wafer handling system with a robot. Mini-environments offer the advantage of greater temperature and humidity control.

The WIT/mini-environment strategy includes the benefit of upgrading existing fabs along with other benefits (Fig. 5.14). Yield losses from contamination are lowered. This critical benefit can be delivered at lower facility construction and operating costs. WIT allows keeping the aisle air cleanliness at a lower cleanliness level, which reduces construction and operating costs. With the wafer isolated, there is less

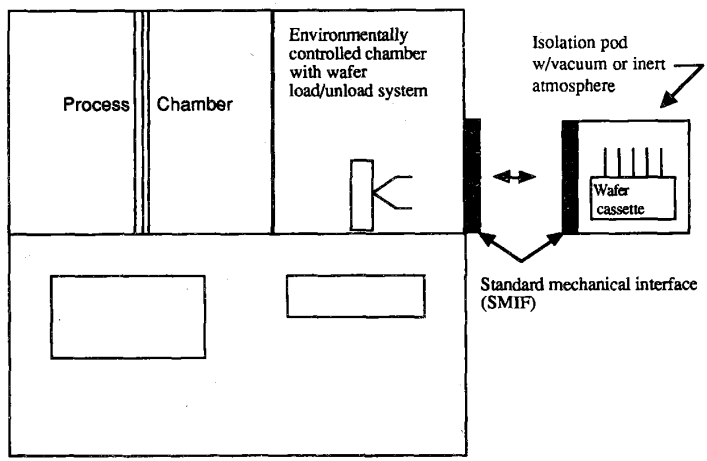


Figure 5.14 Mini-environment system elements.

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pressures on operator clothing, procedures, and constraints. However, the advent of larger-diameter wafers has driven up the weight of a pod of wafers to the point that they are too heavy for operators and too expensive to risk dropping. This situation requires robot handling, which increases cost and complexity. Mini-environment layouts must include storage for wafers (in pods) waiting for process tool availability. Current technology calls for storage units, called *stockers,* that hold the waiting pods or wafers. Layouts may include a central storage system with or without buffer storage at each tool.

Temperature, humidity, and smog

In addition to control of particulates, the air parameters of temperature, humidity, and smog must be specified and controlled in a cleanroom. Temperature control is necessary for operator comfort and process control. Many of the wet processes of etching and cleaning take place in non-temperature-controlled baths, and rely on the room temperature for control. This control is important. A rule of thumb is that chemical reactions, such as an etch rate, change by a factor of 2 with a 10°C change in temperature. A typical temperature range is 72°F, ±2°F (22.2°C, ±1.1°C).

The relative humidity is also a critical process parameter, especially in patterning areas. In this area, thin films of a polymer are put on the wafer to act as an etch stencil. If the humidity is too high, the wafers collect moisture, preventing the polymer from sticking. The situation is the same as applying paint on a wet surface. On the other side, low humidity can foster the buildup of static charge on the wafer surface. The charge causes the wafer to attract particles out of the air. Relative humidity is controlled at between 15 and 50 percent.

Smog is another airborne contaminant in a cleanroom. Again the problem is most critical in the patterning areas. A step in the patterning process is similar to photographic film developing, which is a chemical process. Ozone, a major component of smog, interferes with the development process and must be controlled. Ozone is filtered out of the air by installing carbon filters in the incoming air ducts.

Cleanroom layouts

The traditional cleanroom layout has individual process tunnels (or bays) opening onto a central hallway. Modular layouts have minifabs or major process areas clustered around a central area that serves the distribution of materials and personnel. These are two-level layouts, with the utility and some material services on the first level and the fab area on the second level. Three-level fabs, which have become the

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standard design, have the fabrication area on the second floor with gas, vacuum, deionizing (DI) water cleaners, and chemical supplies positioned on the first floor, from where they are piped up into the fab area. On the third floor are the air handlers and exhaust and scrubber systems.

Cleanroom Construction

Selection of the clean air strategy is the first step in the design of a cleanroom. Every cleanroom is a trade-off between cleanliness and cost. Whatever the final design, every cleanroom is built on basic principles. The primary design is a sealed room that is supplied with clean air, is built with materials that are noncontaminating, and includes systems to prevent accidental contamination from the outside or from operators.

Construction materials

The inside of a cleanroom is constructed entirely of materials that are nonshedding. This includes wall coverings, process station materials, and floor coverings. All piping holes are sealed, and even the light fixtures must have solid covers. Additionally, the design should minimize flat surfaces that can collect dust. Stainless-steel materials are favored for process stations and work surfaces.

Cleanroom elements

Both the design of a cleanroom and its operation must be set up to keep dirt and contamination from getting into the room from the outside. Figure 5.15 shows a layout for a typical fab processing area. The following nine techniques are used to keep out and control dirt:

1. Adhesive floor mats
2. Gowning area
3. Air pressure
4. Air showers
5. Service bays
6. Double-door pass-throughs
7. Static control
8. Shoe cleaners
9. Glove cleaners

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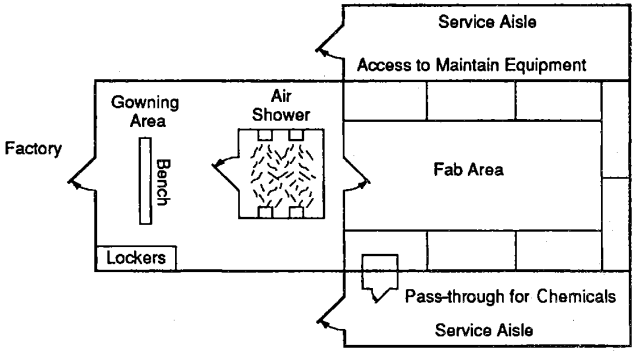


Figure 5.15 Fab area with gowning area, air showers, and service aisles.

Adhesive floor mats. At the entrance to every cleanroom is a floor mat with an adhesive surface. The adhesive pulls off and holds dirt adhering to the bottoms of shoes. In some cleanrooms, the entire floor has a surface treated to hold dirt. Most mats have layers of the adhesive sheets. When the top sheet becomes dirty, it is removed to expose the next clean one.

Gowning area. A major part of a cleanroom is the gowning area or anteroom. This area is a buffer between the cleanroom and the plant. It quite often is supplied with filtered air from ceiling HEPA filters. In this area, the operator's cleanroom apparel is stored. It is also the area where the cleanroom personnel change into their cleanroom garments. The management of this area varies with the degree of cleanliness required in the cleanroom. Quite often, it is managed to the same stringent requirements of the cleanroom itself. Often, the gowning area is divided into two sections by a bench. The operators don the garments on one side and put on their shoe coverings on the bench. The purpose is to keep the area between the bench and the cleanroom at a higher cleanliness level.

A good cleanroom procedure is to ensure that the doors between the factory and the cleanroom are never opened at the same time. This procedure ensures that the cleanroom is never exposed directly to the dirtier factory areas. Cleanroom management also includes lists of materials and garments that can and cannot come into the gowning room. Some areas will provide hallway lockers for coats and so on.

Air pressure. A key design element is the air pressure balances between the cleanroom, the gowning room, and the factory. The well de-

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signed facility will have the air of these three sections balanced such that the highest pressure is in the cleanroom, the second highest in the gowning area, and the lowest in the factory hallways. The higher pressure in the cleanroom causes a low flow of air out of the doors, which, in turn, blows airborne particles back into the dirtier hall way.

Air showers. The final design element protecting the cleanroom from outside contamination is the air shower located between the governing room and the cleanroom. Cleanroom personnel enter the air shower, where high-velocity air jets blow off particles from the outside of the garments. An air shower will have an interlocking system to prevent both doors from being opened at the same time.

Service bays. A cleanroom is really a series of rooms (Fig. 5.15) within the factory, each contributing to the maintenance of the cleanroom. In the center is the processing cleanroom. Surrounding it is a bay area that is maintained at some designated class number that is generally higher than the cleanroom. Class 1000 or Class 10,000 are typical for service bays. In the bay are the process chemical pipes, electrical power lines, and cleanroom materials. Critical-process machines are backed up to the wall dividing the cleanroom and the bay. This arrangement allows technicians to service the equipment from the back without entering the cleanroom.

Double-door pass-throughs. The bay also serves as a semi-clean area for the storage of materials and supplies. They are put into the cleanroom through double-door pass-through units that protect the cleanliness of the cleanroom. Pass-through units may be simple double-door boxes or may have a supply of positive-pressure filtered air with interlocking devices to prevent both doors from being opened at the same time. Often, the pass-throughs are fitted with HEPA filters. All materials and equipment brought into the cleanroom should be cleaned prior to entry.

Static control. Higher-density circuits with submicron feature sizes are vulnerable to smaller particles of contamination attracted by static to the wafer. Static charges build up on the wafers, the storage boxes, work surfaces, and equipment. Each of these items can carry static charges as high as 50,000 V (volts) that attract aerosols out of the air and from personnel garments. The attracted particles end up contaminating the wafers. Statically held particulates are very difficult to remove with standard brush and wet cleaning techniques.

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Most static charge is produced by *triboelectric* charging. This occurs when two materials initially in contact are separated. One surface becomes positively charged as it loses electrons. The other becomes negatively charged as it gains electrons. The triboelectric series table in Fig. 5.16 shows the charging potential for materials some materials found in a cleanroom.[11]

Static also represents a device operational problem. It occurs in devices with thin dielectric layers, as in MOS gate regions. An electrostatic discharge (ESD) of up to 10 A (amperes) is possible. This level of ESD can physically destroy a MOS device or circuit. ESD is a particular worry in device-packaging areas. This problem requires that sensitive devices, such as large-array memories, be handled and shipped in holders of antistatic materials.

Photomasks and reticles are particularly sensitive to ESD. A discharge can vaporize and destroy the chrome pattern.

Some equipment problems are static related—especially robots, wafer handlers, and measuring equipment. Wafers usually come to the equipment in carriers made of PFA-type materials. This carrier material is chosen for its chemical resistance, but it is not conductive. Charge builds up on the wafers but cannot dissipate to the carriers. When the carrier comes close to a piece of metal on the equipment, the wafer charge discharges to the equipment. The electromagnetic interference produced interferes with the machine operation.

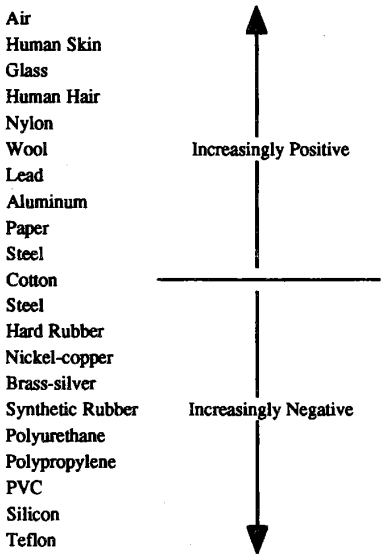


Figure 5.16 Triboelectric series. *(Source:* Hybrid Circuit Technology Handbook, *Noyes Publications.)*

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Static is controlled by prevention of charge buildup and the use of discharge techniques (Fig. 5.17). Prevention techniques include use of antistatic materials in garments and in-process storage boxes. In some areas, a topical antistatic solution may be applied to the walls to prevent the buildup of static charge. These solutions work by leaving a neutralizing residue on the surface. Generally, they are not used in critical stations because of the possible contaminating effect of the residue.

Discharge techniques include the use of ionizers and grounded static-discharge straps. Ionizers are placed just underneath the HEPA filters, where they function to neutralize any charge buildup in the filtered air. Ionizers are also placed on nitrogen blow-off guns for the same effect. Some stations will have a portable ionizer blowing ionized air directly on the wafers being processed. Static discharge is also accomplished by grounding operators with wrist straps, having grounded mats at critical stations, and grounding work surfaces. Comprehensive static control programs, with prevention and discharge methods along with personnel training and third party monitoring, are features in most advanced fabs.

Shoe cleaners. In any contamination-controlled area, the dirtiest region is the floor. Removal of dirt from the sides of shoes and shoe coverings is accomplished by shoe cleaners stationed at the cleanroom

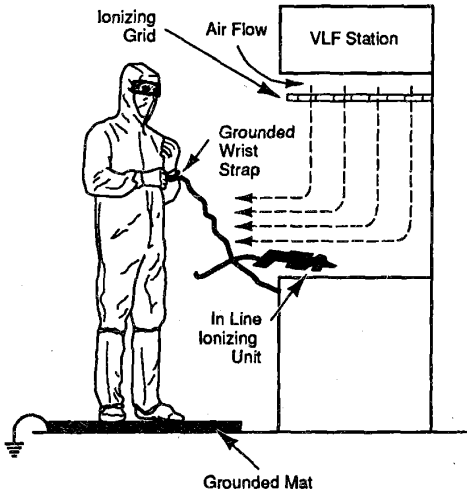


Figure 5.17 Static-charge reduction techniques.

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door. Rotating brushes remove the dirt. Typical machines feature an internal vacuum to capture the loosened dirt, and bags to hold the dirt for removal from the area.[12]

Glove cleaners. Maintaining clean gloves in the fab area is a challenge. Instructing operators to discard gloves when they are contaminated or dirty is one way. However, some contamination is hard to see, and the decision to discard becomes a judgment that can vary from operator to operator. Another approach is to discard the gloves after every shift. This can get very expensive. Some fab areas use glove cleaners that clean and dry the gloves in an enclosure.[13]

Personnel-generated contamination

Cleanroom personnel are among the biggest sources of contamination. A cleanroom operator, even after showering and sitting, can give off between 100,000 and 1,000,000 particles per minute.[14] This number increases dramatically when a person is in motion. At 2 miles per hour, a human being gives off up to 5 million particles per minute. The particles come from flakes of dead hair and normal skin flaking. Additional particle sources are hair sprays, cosmetics, facial hair, and exposed clothing. The table in Fig. 5.18 lists the percentage increase in particulate generation over the background contamination level for different operator activities.[17]

Normal clothing can add more millions of particles to the area, even under a cleanroom garment. In cleanrooms with very high cleanliness levels, operators will be directed to wear street clothing that is made of tight-weave, nonshedding materials. Garments made of wools and cottons are to be avoided, as are ones with high collars.

A human's breath also contains high levels of contaminants. Every exhale puts numerous water droplets and particles into the air. The breath of smokers carries millions of particles for a long time after a cigarette is finished. Body fluids such as saliva contain sodium, a killer to many semiconductor devices. While healthy human beings are sources of many contaminants, sick individuals are even worse.

Normal Breath	No Particles
Smoker's Breath after Smoking	500 %
Sneezing	2000%
Sitting Quietly	20 %
Rubbing Hands On Face	200%
Walking	200%
Stamping Foot on Floor	5000%

Figure 5.18 Activity-caused increase in particles. *(Source:* Hybrid Circuit Technology Handbook, *Noyes Publications.)*

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Specifically, skin rashes and respiratory infections are additional sources of contaminants. Some fabrication areas reassign personnel with certain health problems.

Given the scope of the problem, the only feasible way to render humans acceptable in a cleanroom is to cover them up. The style and material of clothing selected for cleanroom personnel depends on the level of cleanliness required. For a typical area (Fig. 5.17), the clothing material will be nonshedding and may contain conductive fibers to draw off static charges. Materials used are polyester and GORETEX™. The trade-off is the filtering ability of the material and operator comfort. The reclean versus discard issue applies to cleanroom suits as well as gloves. Most ULSI fabs have found that reusable gowns, even with the cost of recleaning, provide a overall lowered cost of ownership.[18]

Every part of the body is covered up. The head will have an inner cap that keeps the hair in place. This is covered by an outer shell that is designed to fit close to the face and has snaps or a tail for securing the headgear under the body-covering smock. Covering the face will be a mask. Masks vary from surgical types to full ski-mask-style designs. In some cleanrooms, both an inner and outer face mask are required. The eyes, which are a major source of fluid particles, are covered by glasses (usually safety glasses) with side shields. In contamination-critical areas, the operators might wear a covering that totally encloses the head and face, connected to an air supply and filter. These are lower-tech models of a space suit helmet. The unit attaches to a belt filter, blower, and pump system. Fresh air is supplied by the pump, while the filter ensures that no breath-generated contaminates are discharged into the room.[1]

Body covers are oversuits (called *bunny suits*) that have closures for the legs, arms, and neck. Well designed suits will have covers over the zippers and no outside pockets.

The feet are covered with shoe coverings, some with attached leggings that come up the leg. In static-sensitive areas, straps are available to drain off static charge.

Hands are covered with at least one pair of gloves. Most favored are medical-type PVC gloves that permit good tactile feeling. Glove materials for chemical handling include orange latex (acid protection), green nitrile (solvent protection), and silver multilayered PVA solvent (special solvents).[16] In some areas, an inner pair of cotton gloves is permitted for comfort. Gloves should be pulled up over the sleeves to prevent contamination from traveling down the arm and into the cleanroom.

Skin flaking can be further controlled with the use of special lotions that moisten the skin. Any lotions used must be sodium- and chlorine-free.

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In general, the order of gowning is from the head down. The theory is that dirt stirred up at each level is covered up by the next lower garment. Gloves are put on last. The garments and procedures needed to control contamination from cleanroom workers are well known. However, the primary level of defense is the dedication and training of the operators. It is easy for an area to become lax in maintaining cleanroom discipline and to suffer high levels of contamination.

Process water

During the course of fabrication processing, a wafer will be chemically etched and cleaned many times. Each of the etching or cleaning steps is followed by a water rinse. Throughout the entire process, the wafer may spend a total of several hours in water rinse systems. A modern wafer fabrication facility may use up to several million gallons of water per day, representing a substantial investment in water processing, delivery to the process areas, and treatment and discharge of waste water.[19] Given the vulnerability of semiconductor devices to contamination, it is imperative that all process water be treated to meet very specific cleanliness requirements.

Water from a city system contains unacceptable amounts of the following contaminants:

1. Dissolved minerals
2. Particulates
3. Bacteria
4. Organics
5. Dissolved oxygen
6. Silica

The dissolved minerals come from salts in normal water. In the water, the salts separate into ions. For example, salt (NaCl) breaks up into Na^+ and Cl^- ions. Each is a contaminant in semiconductor devices and circuits. They are removed from the water by reverse osmosis (RO) and ion-exchange systems.

The process of removing the electrically active ions changes the water from a conductive medium to a resistive one. This fact is used to improve the quality of deionized (DI) water. Deionized water has a resistivity of 18,000,000 $\Omega \cdot$cm at 25°C. It is called 18-megohm (MΩ) water. Figure 5.19 shows the effect on the resistivity of water when various amounts of dissolved minerals are present.

The resistivity of all process water is monitored at many points in the fabrication area. The goal and specification is 18 MΩ in VLSI ar-

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Resistivity Ohms-cm 25°C	Dissolved Solids (ppm)
18,000,000	0.0277
15,000,000	0.0333
10,000,000	0.0500
1,000,000	0.500
100,000	5.00
10,000	50.00

Figure 5.19 Resistivity of water versus concentration of dissolved solids.

eas, although some fabrication areas will run with 15-MΩ water levels. Solid particles (particulates) are removed from the water by sand filtration, earth filtration, and/or membranes to submicron levels. Bacteria and fungi find water a favorable host. They are removed by sterilizers that use ultraviolet radiation to kill the bacteria and filters to remove them from the stream of water.

Organic contaminates (plant and fecal materials) are removed with carbon bed filtration. Dissolved oxygen and carbon dioxide are removed with forced draft decarbonators and vacuum degasifiers.[20] Water specifications for a 4MB DRAM product are shown in Fig. 5.20.

The cost of cleaning process water to acceptable levels is a major operating expense of a fabrication area. In most fabrications, the process stations are fitted with water meters that monitor the used water. If the water falls within a certain range, it is recycled in the water system for cleanup. Excessively dirty water is treated as dictated by regulations and discharged from the plant. A typical fabrication system is shown in Fig. 5.21. Water stored in the system is blanketed with nitrogen to prevent the absorption of carbon dioxide. Carbon dioxide in the water interferes with resistivity measurements, causing false readings.

Contaminant	64Kb	1Mb	16Mb
Resistivity (MΩcm)	>17	>18	>18.1
TOC (micro-g/L)	<200	<50	<10
Bacteria (#/L)	<250	<50	<1
Particles (#/mL)	<50	<50	<1
Critical size (micron)	0.2	0.2	0.05
Dissolved oxygen (micro-g/L)	<200	<100	<20
Sodium (micro-g/L)	<1	<1	<0.01
Chlorine (micro-g/L)	<5	<1	<0.01
Manganese (micro-g/L)	N/A	<1	<0.005

Figure 5.20 DRAM water specs. *(Source:* Semiconductor International, *July 1994, p. 178.)*

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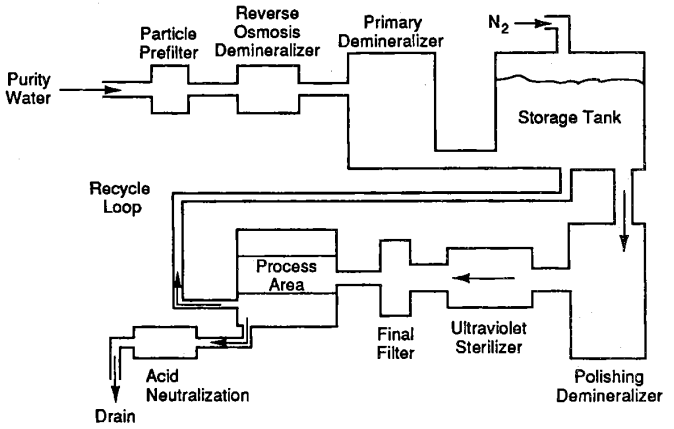


Figure 5.21 Typical deionized water system.

Process chemicals

The acids, bases, and solvents used to etch and clean wafers and equipment have to be of the highest purity for use in a fabrication area. The contaminants of concern are metallics, particulates, and other chemicals. Unlike water, process chemicals are purchased and used as they come into the plant. Industrial chemicals are rated by grade. They are commercial, reagent, electronic, and semiconductor grade. The first two are generally too dirty for semiconductor use. Electronic grade and semiconductor grade are cleaner chemicals, but levels of cleanliness vary from manufacturer to manufacturer.

Trade organizations such as SEMI are establishing cleanliness specifications for the industry. However, most semiconductor plants purchase their chemicals to in-house generated specifications. Of primary concern are the metallic mobile ionic contaminants. These are usually limited to levels of 1 part per million (ppm) or less. Some suppliers are making available chemicals with MIC levels of only 1 part per billion (ppb). Particulate filtering levels are specified at 0.2 μm or lower.

Chemical purity is indicated by its assay number. The assay number indicates the percentage of the chemical in the container. For example, an assay of 99.9 percent on a bottle of sulfuric acid means that the bottle contains 99.9 percent sulfuric add and 0.01 percent other substances.

The delivery of a clean chemical to the processing area involves more than just making a clean chemical. Care must be taken to clean the inside of the containers, using containers that do not dissolve, us-

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ing particulate-free labels, and placing the clean bottles in bags before shipping. Chemical bottle use is found only in older and lower technology fabs.

Most firms purchase clean process chemicals in bulk quantities. They are decanted into smaller vessels and are distributed to the process stations from a central location by pipes or distributed directly to the process station from a mini-unit. Bulk chemical distribution systems (BCDSs) offer cleaner chemicals and lower cost. Special care must be maintained to ensure that piping and transfer vessels are cleaned regularly to prevent contamination. A particular worry in secondary vessel filling is cross contamination. Vessels should be reserved for one type of chemical only.

The requirement for cleaner chemicals, tighter process control, and lower costs is being met by several techniques. One is point-of-use (POU) chemical mixers (another version of a BCDS). These units, connected to a wet bench or automatic machine, mix chemicals and deliver them directly to the process vessel or unit. Another technique is the use of chemical reprocessors. These units are located on the drain side of a wet process station. Discharged chemicals are refiltered and (in some cases) recharged for reuse. Critical recirculating etch baths are connected to filters to keep a clean supply of chemicals at the wafer. A newer process is point of use chemical generation (POUCG). Chemicals such as NH_4OH, HF, and H_2O_2 are made at the process station by combining the proper gases with DI water. Elimination of the contamination associated with chemical packaging and transfers gives this method the possibility of producing chemicals in the parts per trillion (ppt) range.[21]

Process gases

In addition to the many wet (liquid) chemical processes, a semiconductor wafer is processed with many gases. The gases are both the air-separation gases (oxygen, nitrogen, and hydrogen) and specialty gases such as arsine and carbon tetrafluoride.

Like the wet chemicals, they have to be delivered clean to the process stations and tools. Gas quality is measured in four categories:

1. Percentage of purity
2. Water vapor content
3. Particulates
4. Metallic ions

Extremely high purity is required for all process gases. Of particular concern are the gases used in oxidation, sputtering, plasma etch,

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chemical vapor deposition (CVD), reactive ion etch, ion implantation, and diffusion. All of these processes involve chemical reactions that are driven by an energy source. If the gases are contaminated with other gases, the anticipated reaction can be significantly altered or the result on the wafer changed. For example, chlorine contamination in a tank of argon used for sputtering can end up in the sputtered film, with disastrous results for the device. Gas purity is specified by the assay number, with typical values ranging from 99.99 to 99.999999 percent, depending on the gas and the use in the process. Purity is expressed as the number of 9s to the right of the decimal point. The highest purity is referred to as "six 9s pure."[22]

The challenge in fab areas is maintaining the gas purity from the manufacturer to the process station. From the source, the gas passes through a piping system, a gas panel containing valves and flowmeters, and a connection to the tool. Leaks in any part of the system are disastrous. Outside air (especially the oxygen) can enter into a chemical reaction with the process gas, changing its composition and the desired reaction in the process. Contamination of the gas can come from outgassing of the system materials. A typical system features stainless steel piping and valves along with some polymer components, such as connectors and seals. For ultra-clean systems, the stainless steel surfaces have electropolished and/or double vacuum melt inside surfaces to reduce outgassing.[23] Another technique is the growing of an iron oxide film, called *oxygen passivation* (OP), to further reduce outgassing. Polymer components are avoided. Gas panel design eliminates dead spaces that become repositories for contamination. Also critical is the use of clean welding processes to eliminate gases absorbed into the piping from the welding gases.

The control of water vapor is also critical. Water vapor is a gas and can enter into unwanted reactions just like other contaminating gases. In fabrication areas, processing silicon wafers with water vapor present is a particular problem. Silicon oxidizes easily wherever free oxygen or water is available. Control of unwanted water vapor is necessary to prevent accidental oxidation of silicon surfaces. Water-vapor limits are 3 to 5 ppm.

The presence of particulates and/or metallics in a gas has the same effect on the processing as in wet chemicals. Consequently, gases are filtered to the 0.2-μm level and metallic ions are controlled to parts per million or lower.

The air-separation gases are stored on the site in the liquid state. In this state, they are very cold, a situation that freezes some contaminants in the bottom of the tanks. Specialty gases are purchased in high-pressure cylinders. Since many of the specialty gases are toxic or flammable, they are stored in special cabinets outside the plant.

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Quartz. Wafers spend a lot of process time in quartz holders such as wafer holders, furnace tubes, and transfer holders. Quartz can be a significant source of contamination, both from outgassing and particulates. Evan high-purity quartz contains heavy metals that can outgas into diffusion and oxidation tube gas streams, especially during high-temperature processes. Particulates come from the abrasion of the wafers in the wafer boats and the scrapping of the boats against the furnace tubes. (Solutions to this problem are discussed in Chapter 11.) Both electric and flame fused quartz processes are used to produce quartz surfaces that are acceptable for semiconductor use.[24]

Equipment

Successful contamination control is dependent on knowing the sources of contamination. Most analysis (Fig. 5.22) identifies process equipment as the largest source of particulates. By the 1990s, equipment-induced particulates rose to the level of 75 to 90 percent of all particle sources.[23] This does not mean that the equipment is getting dirtier. Advances in particulate control in air, chemicals, and from personnel has shifted the focus to equipment. Defect generation is part of equipment specifications. Generally, the number of particles added to the wafer per product pass (ppp) through the tool is specified. The term *particles per wafer pass* (PWP) is also used.

Reduction of particle generation starts with design and material selection. Other factors are the transport of the particles to the wafer and deposition mechanisms such as static. Most equipment is assembled in a cleanroom with the same class number as the customer's fab

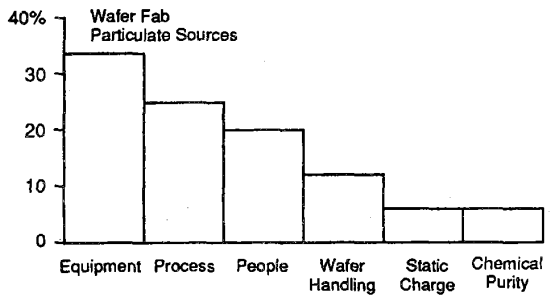


Figure 5.22 Sources of particulate contamination. This analysis, shown at SEMI Forecast by Dr. C. Rinn Cleavelin, Texas Instruments, revealed equipment-generated particles as the top enemy in 1985. *(Courtesy of Semiconductor Equipment and Materials Institute.)*

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area. The clustering of several process tools with one clean micro-environment for loading and unloading minimizes the contamination generation associated with multiple loading stations. Cluster tools are discussed in Chapter 15. There is interest in having *in situ* particle monitors in the process chambers. Challenges to this level of automation and detection include correlation of in-chamber levels with on wafer levels and the lifetime of detectors in the hostile and corrosive environments of most process chambers.

Cleanroom Materials and Supplies

In addition to the process chemicals, it takes a host of other materials and supplies to process the wafers. Each of these must meet cleanliness requirements. Logs, forms, and notebooks used will be either of nonshedding coated paper or of a polymer plastic. Pencils are not allowed, and pens are the nonretracting type.

Wafer storage boxes are made of specific non-particle-generating materials as are carts and tubing materials. Cart wheels and tools are used without greases or lubricants. In many areas, mechanics' tools and tool boxes are cleaned and left inside the cleanroom.

Cleanroom Maintenance

Regular maintenance of the cleanroom is essential. The cleaning personnel must wear the same garments as the operators. Cleanroom cleaners and applicators, including mops, must be carefully specified. Normal household cleaners are far too dirty for use in cleanrooms. Special care must be taken when using vacuum cleaners. Special cleanroom vacuums with HEPA filtered exhausts are available. Many cleanrooms will have built-in vacuum systems to minimize dirt generation during cleaning.

The wipe-down of process stations is done with special wipes made from non-shedding polyester or nylon, prewashed to reduce contamination. Some are prewetted with an isopropyl alcohol and DI water solution, which provides convenience and eliminates secondary contamination from spraying cleaners in the cleanroom.[27]

The wiping procedure is critical. Wall surfaces should be wiped from top to bottom and deck surfaces from back to front. Cleaning chemicals in spray bottle, if used, should be sprayed into wipes, not onto the surfaces. This prevents overspray onto the wafers and equipment. Cleanroom cleaning has, itself, become a critical supporting operation. Many fabs use outside certification services[24] to identify and document cleanliness levels, practices, documentation, and control procedures. Certification standards for cleanroom maintenance schedules is identified in the ISO Global Cleanroon Standards (ISO 14644-2).

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Copper metallization has become the metal of choice for advanced ULSI devices. While the copper has many advantages (see Chapter 13), there is a serious downside. Copper contamination inside a silicon wafer raises havoc with the electrical operation of the component devices. Isolating the copper processing areas and copper deposited wafers is essential. Separate areas and separate process tools are required with strict production control to ensure that no copper technology wafers get diverted into the other process areas.

Wafer Surface Cleaning

Clean wafers are essential at all stages of the fabrication process but are especially necessary before any of the operations are performed at high temperature. Up to 20 percent of all process steps relate to wafer cleaning.[28] The cleaning techniques described here are used throughout the wafer fabrication process.

The story of semiconductor process development is in many respects the story of cleaning technology keeping pace with the increasing need for contamination-free wafers. Wafer surfaces have four general types of contamination. Each represents a different problem on the wafer, and each is removed by different processes. The four types are:

1. Particulates
2. Organic residues
3. Inorganic residues
4. Unwanted oxide layers

In general, a wafer cleaning process, or series of processes, must (a) remove all surface contaminants (listed above), (b) not etch or damage the wafer surface, (c) be safe and economical in a production setting, and (d) be ecologically acceptable. Cleaning processes are generally designed to accommodate two primary wafer conditions. One, called the *front end of the line* (FEOL), refers to the wafer fabrication steps used to form the active electrical components on the wafer surface. During these steps, the wafer surface, and particularly the gate areas of MOS transistors, are exposed and vulnerable. A critical parameter in these cleans is *surface roughness.* Excessive surface roughness can alter device performance and compromise the uniformity of layers deposited on top of the devices. Surface roughness is measured in nanometers as the root mean square of the vertical surface variation (nmRMS). Year 2000 requirements are on the order of 0.15 nm, dropping to less than 0.1 nm by the year 2010.[29] Other concerns in FEOL cleaning processes are the electrical condition of the bare surface.

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Metal contaminants on the surface change the electrical characteristics of devices, with MOS transistors being particularly vulnerable. Sodium (Na) is a particular problem (see Chapter 4), along with Fe, Ni, Cu, and Zn. Cleaning processes will have to reduce concentrations to less than 2.5×10^9 atoms/cm^2 to meet 2010 device needs. Aluminum and calcium are also problems and need reduction on the surface to the 5×10^9 atoms/cm^2 level.[30]

A most critical factor is maintaining the integrity of gate oxides. Cleaning processes can attack and rough up gate oxides, with the thinner ones most vulnerable. A gate oxide is required to act as a dielectric in a MOS transistor, and as such must have a consistent structure, makeup, and thickness. *Gate oxide integrity* (GOI) is measured by testing the gate for electrical shorts. The NTRS indicates that, at 180-nm technology level, gates will have to exhibit less than 0.02 defects/cm^2 when tested at 5 MV/cm for 30 s.[33]

Specific concerns at the BEOL cleans, in addition to particles, metals, and general contamination, are anions, polysilicon gate integrity, contact resistance, via hole cleanliness, organics, and the overall numbers of shorts and opens in the metal system. These issues are explored in Chapter 13. Photoresist removal is also a cleaning process with both FEOL and BEOL consequences. These issues are explored in Chapter 9.

Different chemicals and cleaning methods are mixed and matched to accommodate the needs at particular steps in the process. A typical FEOL cleaning process (such as preoxidation clean) is listed in Fig. 5.23. The FEOL process listed is called a non-Hf-last process. Other variations have the HF removal step last. Non-Hf-last surfaces are hydrophilic that can be dried without water marks and have a thin oxide (grown in the cleaning steps) that can protect the surface. They also absorb more organic contamination. HF-last surfaces are hydrophobic, which can be difficult to dry without water marks if there are also hydrophilic (oxides) surface layers present. These surfaces are stable from hydrogen surface passivation.[29] A choice of either non-HF-last or HF-last depends on the sensitivity of the devices being fabricated in the wafer surface and general cleanliness requirements.

- Particle removal (mechanical)
- General chemical clean (such as sulfuric acid/H_2/O_2)
- Oxide removal (typically dilute HF)*
- Organic and metal removal (SC-1)
- Alkali metal and metal hydroxide removal (SC-2)
- Rinse steps
- Wafer drying

Figure 5.23 Typical FEOL cleaning process steps.

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Particulate removal

Particulates on the wafer surface vary from very large ones (50 μm in size) to very tiny ones (<1 μm in size). The larger ones can be cleaned off by conventional chemical baths and rinses. The smaller particulates are more difficult to remove, because they can be held to the surface by several strong forces. One is called the *van der Waals force.* It is a strong interatomic attraction between the electrons of one atom and the nucleus of another. A technique to minimize electrostatic attraction is manipulation of a factor called the *zeta potential.* Zeta potential arises from a charge zone around particles that is balanced by an oppositely charged zone in the cleaning liquid. This charge varies with velocity (the speed of movement of the cleaning liquid, as when the wafers are moved in a cleaning bath), the pH of the solution, and the concentration of electrolytes in the solution. It is also affected by additives to the cleaning solution, such as surfactants. These conditions can be set to create a large charge that has the same polarity of the wafer, thus creating a repulsion that serves to keep the particle in the solution and off the wafer surface.

Capillary force is another problem. It occurs when there is a liquid bridge between a particle and the surface (Fig. 5.24). Capillary forces can be higher than van der Waals forces.[30] Surfactants and mechanical assist, such as megasonics, are used to dislodge these particles from the surface.

Cleaning processes are most often a series of steps designed to remove both the large and small particles. The simplest particulate removal process is to blow off the wafer surface using a spray of filtered high-pressure nitrogen from a hand-held gun located in the cleaning stations. In fabrication areas where small particles are a problem, the nitrogen guns are fitted with ionizers that strip static charges from the nitrogen stream and neutralize the wafer surface.

Nitrogen blow-off guns are effective in removing most large particles. Since the guns are hand held, the operators must use them in a manner that does not contaminate other wafers in the station or the station itself. Blow-off guns are not generally used in Class 1/10 cleanrooms.

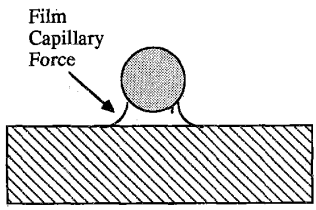


Figure 5.24 Capillary force from film.

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Wafer scrubbers

The stringent wafer cleanliness requirements for epitaxial growth led to the development of mechanical wafer surface scrubbers, which are used wherever particulate removal is critical.

The scrubbers hold the wafer on a rotating vacuum chuck (Fig. 5.25). A rotating brush is brought in near contact with the rotating wafer while a stream of deionized water is directed onto the wafer surface. The combination of the brush and wafer rotations creates a high-energy cleaning action at the wafer surface. The liquid is forced into the small space between the wafer surface and the brush ends where it achieves a high velocity, which aids the cleaning action. Caution must be exercised to keep the brushes and cleaning liquid lines clean to prevent secondary contamination. Also, the brush height above the wafer must be maintained to prevent scratching the wafer surface.

Surfactants may be added to the DI water to increase the cleaning effectiveness and prevent static buildup. In some applications, diluted ammonium hydroxide may be used as the cleaning liquid to prevent buildup of particles on the brush and to control the zeta potential in the system.[31]

Scrubbers are designed as stand-alone units with automatic loading capabilities or are built into other pieces of equipment to clean the wafers automatically before processing.

High-pressure water cleaning

The removal of statically attached particles first became a necessity for the cleaning of glass and chrome photomasks. A high-pressure water spray process was developed, using a small stream of water pressurized 2000 to 4000 psi. The stream is swept across the mask or

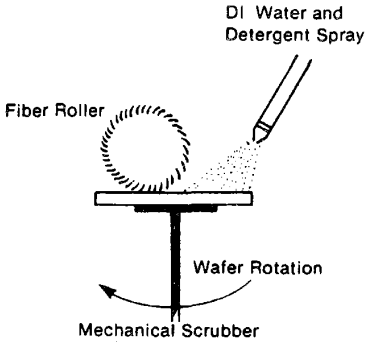


Figure 5.25 Mechanical scrubber.

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wafer surface, dislodging both large and small particles. Often, a small amount of surfactant will be added to the water stream to act as a destatic agent.

Organic residues

Organic residues are compounds that contain carbon, such as oils in fingerprints. These residues can be removed in solvent baths such as acetone, alcohol, or TCE. In general, solvent cleaning of wafers is avoided whenever possible due to the difficulty of drying the solvent completely off the wafer surface. Also, solvents always contain some impurities that themselves may represent a contamination source.

Inorganic residues

Inorganic residues are those that do not contain carbon. Examples are inorganic acids such as hydrochloric or hydrofluoric acid, which may be introduced from other steps in wafer processing. The organic and inorganic residues are cleaned from the wafers in a variety of cleaning solutions described in the following section.

Chemical cleaning solutions

A wide range of cleaning processes exist in the semiconductor industry. Each fabrication area has different cleanliness needs and different experiences with different solutions. The solutions described in this section are those in common use, although there are numerous variations and different combinations of solutions from one fabrication area to another. Described are processes used to clean wafers before doping, deposition, and metallization steps. (The special case of photoresist removal is addressed in Chapter 8.)

Liquid chemical cleaning processes are generally referred to as *wet processes* or *wet cleaning*. Immersion cleaning takes place in glass, quartz, or polypropylene tanks fitted into the deck of a cleaning station (see Chapter 4). Where heating of the solution is required, the tank may be sitting on a hot plate, be wrapped with heating elements, or have an immersion heater inside. Chemicals are also applied by spraying, either using direct impingement or in centrifugal tools (see spin rinse dryers).

General chemical cleaning

Sulfuric acid. A common general cleaning solution is hot sulfuric acid with an added oxidant. It is also a general photoresist stripper (see

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Chapter 8). The sulfuric acid is an effective cleaner in the 90 to 125°C range. At these temperatures, it will remove most inorganic residues and particulates from the surface. Oxidants are added to the sulfuric acid to remove carbon residues. The chemical reaction converts the carbon to carbon dioxide, which leaves the bath as a vapor by the following reaction:

$$C + O_2 \rightarrow CO_2(gas)$$

The oxidants normally used are:

- Hydrogen peroxide (H_2O_2)
- Ammonium persulfate [$(NH_4)_2S_2O_8$]
- Nitric acid (HNO_3), and ozone (O_2)

Sulfuric acid with hydrogen peroxide. Hydrogen peroxide with sulfuric acid is a common cleaner used to clean wafers at all stages of processing, especially before the tube processes. It is also used as a photoresist stripper in the patterning operation. Within the industry, this solution is known by a number of names, including *Carro's acid* and *piranha etch*. The latter term attests to the aggressiveness and effectiveness of the solution.

A manual method is to add about 30 percent (by volume) of hydrogen peroxide to a beaker of room-temperature sulfuric acid. In this ratio, an exothermic reaction takes place that quickly raises the temperature of the bath into the 110 to 130°C range. As time proceeds, the reaction slows, and the bath temperature falls below the effective range. At this point, the bath may be recharged with additional hydrogen peroxide or discarded. Recharging the bath eventually results in a lowered cleaning rate due to the conversion of the hydrogen peroxide to water, which dilutes the sulfuric acid.

In automated systems, the sulfuric acid is heated to the effective cleaning temperature range and small amounts (50 to 100 mL) of hydrogen peroxide are added before cleaning each batch of wafers. This method maintains the bath at the proper temperature, and the water created from the hydrogen peroxide evaporates out of the solution. The use of heated sulfuric acid is preferred for economic and process-control reasons. It is also easier to automate this approach to mixing the two chemicals.

Ozone. The purpose of oxidant additives is the addition of oxygen to the solution. Some companies use a flow of gaseous ozone (O_2) directly in the container of sulfuric acid. Ozone and DI water constitute a

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cleaning solution for light organic contamination.[32] A typical process is 1 to 2 ppm ozone in DI water for ten minutes at room temperature.[33]

Oxide layer removal

The ease of silicon oxidation has been mentioned. The oxidation can take place in air or in the presence of oxygen in the heated chemical cleaning baths. Often, the oxide grown in the baths, while thin (100 to 200 Å), is thick enough to block the silicon surface from reacting properly during one of the other process operations. The thin surface oxide can act as an insulator, preventing good electrical contact between the silicon surface and a layer of conducting metal.

The removal of these thin oxides is a requirement in many processes. Silicon surfaces with an oxide are called *hydroscopic*. Surfaces that are oxide free are termed *hydrophobic*. Hydrofluoric acid (HF) is the acid favored for oxide removal. Prior to an initial oxidation, when the surface is only silicon, the wafers are cleaned in a bath of full-strength HF (49 percent). The HF etches away the oxide but does not etch the silicon.

Later in the processing, when the surface is covered with previously grown oxides, thin oxides in patterned holes are etched away with a water and HF solution. These solutions vary in strength from 100:1 to 10:7 (H_2O to HF). The strength is chosen depending on the amount of oxide already on the wafer, since the water and HF solution will etch both the oxide on the silicon surface in the hole and the oxide covering the rest of the surface. A strength is chosen to ensure the removal of the oxide in the holes while not excessively thinning the other oxide layers. Typical dilutions are 1:50 to 1:100.

Management of the chemistry of the silicon surface is an ongoing challenge for cleaning processes. Generally, pregate cleaning uses the dilute HF as the last chemical step. It is called *HF-last*. HF-last surfaces are hydrophobic and passivated with low metallic contamination. However, hydrophobic surfaces are difficult to dry, often leaving *watermarks*.[34] Another problem is increased particle adhesion and copper plating out of the surface.[35]

RCA clean. In the mid 1960s, Werner Kern, an RCA engineer, developed a two-step process to remove organic and inorganic residues from silicon wafers. The process proved to be highly effective, and the formulas became known simply as the *RCA cleans*. Whenever an RCA cleaning process is referred to, it means that hydrogen peroxide is used along with some base or acid. The first step, Standard clean 1 (SC-1) uses a solution of water, hydrogen peroxide, and ammonium

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hydroxide. Solutions vary in composition from 5:1:1 to 7:2:1 and are heated to the 75 to 85°C range. SC-1 removes organic residues and sets up a condition for the desorption of trace metals from the surface. During the process, an oxide film keeps forming and dissolving.

Standard clean-2 (SC-2) uses a solution of water, hydrogen peroxide, and hydrochloric acid mixed in ratios of 6:1:1 to 8:2:1 and is used at the 75 to 85°C temperature range. SC-2 removes alkali ions and hydroxides and complex residual metals. It leaves behind a protective layer of oxide. The original mixtures are shown in Fig. 5.26.

The RCA formulas have proven durable over the years and are still the base cleaning processes for most pre-furnace cleaning. Improvements in chemical purity have kept pace with industry cleaning needs. Depending on the application, the order of SC-1 and SC-2 steps may be reversed. Where an oxide-free surface is required, an HF step is used before, in between, or after the RCA cleans.

Many adaptations and changes have been made to the original cleaning solutions. One problem is the removal of metallic ions from the wafer surface. These ions exist in chemicals and are not dissolved (made soluble) in most cleaning and etching solutions. The addition of a *chelating agent*, such as ethylenediamine-tetra-acetic acid, serves to bind up the ions so they do not redeposit on the wafer.

Diluted RCA solutions are finding more use. SC-1 dilutions are 1:1:50 (instead of 1:1:5) and SC-2 dilutions are 1:1:60 (instead of 1:1:6). These solutions have been found to be as effective as the more concentrated versions. Additionally, they produce less microroughing and are cost effective and easier to remove.[36]

Room-temperature and ozonated chemistries

The perfect cleaning process takes place at room temperature with totally safe chemicals that are easily and economically disposable. That

RCA Clean Type	Parts by Volume
Standard Clean (SC-1)	5: DI water
	1: 30% Hydrogen peroxide
	1: 29% Amonium hydroxide
Process	70 degrees centigrade for 5 min.
Standard Clean 2 (SC-2)6:	DI water
	1: 30% hydrogen peroxide
	1: 37% hydrochloric acid
Process	70 degrees centigrade, 5-10 min.

Figure 5.26 RCA clean formulas.

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process does not exist. However, there is research into room-temperature chemistries. One process[37] combines room temperature baths of ultrapure water infused with ozone and two HF solutions (Fig. 5.27). Megasonic assist elevates the cleaning efficiency.

Spray cleaning. The standard cleaning technique has been immersion in chemical baths performed in wet benches or automated machines. While wet cleans are projected to carry the industry into the 0.35 to 0.50 μm era, there are growing considerations. The chemicals are becoming more expensive, immersion in a tank presents a redeposition of contaminants, and smaller and deeper patterns on the wafer surface constrain cleaning efficiency. Alternative cleaning methods have emerged. Spray cleaning offers several advantages. Chemical costs go down, since the chemicals expended are directed to the wafer rather than maintaining large reserves in tanks. Less chemical use reduces the cost of treating or removing hazardous chemical waste. Cleaning efficiency is improved. The pressure of the spray assists in cleaning small patterns on surfaces with deep holes. Also, there is less chance of recontamination, because the wafer receives only fresh chemicals. Spray methods allow immediate water rinsing after cleaning, eliminating transfer to a separate water rinse station.

Dry cleaning. The considerations concerning wet immersion methods have spurred interest in and development of *vapor or gas phase* cleaning. For cleaning, the wafers are exposed to vapors of the cleaning or etching chemical(s). HF/water vapor mixtures have found their way into processes for oxide removal. Available are systems for vapor phase replacement of peroxide-based cleaners.[38]

The ultimate industry dream is all dry cleaning and etching. Dry-etching methods (plasma; see Chapter 9) are well established. Dry cleaning is under development. Ultraviolet (UV) ozone can oxidize and photo-dissociate contaminants form the wafer surface.

Cryogenic cleaning. High-pressure carbon dioxide CO_2, or *snow cleaning,* is an emerging technique (Fig. 5.28). CO_2 is directed at the wafer

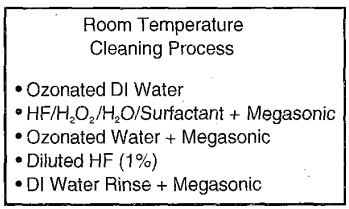


Figure 5.27 Experimental room-temperature cleaning process.

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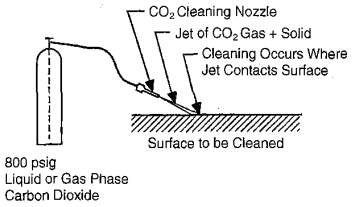


Figure 5.28 CO_2 "snow" cleaning. *(Courtesy of Walter Kern.)*

from a nozzle. As the gas leaves the nozzle, its pressure drops, causing a rapid cooling, which in turn forms CO_2 particles, or snow. The force of the impinging particle dislodges surface particles, and the flow carries them away. The physical bombardment of the surface supplies a cleaning action. Argon aerosol is another cryogenic technique. Argon is a fairly heavy and large atom that can dislodge particles when directed to the wafer under pressure.

A combination process, called *cryokinetic,* combines nitrogen and argon. Precooling of the gases under pressure forms a liquid/gas mixture that is flowed into a vacuum chamber. In the chamber, the liquid expands rapidly to form microscopic crystals that knock particles from the wafer surface.[39]

Water rinsing

Every wet-cleaning sequence is followed by a rinse in deionized water. Rinsing performs the dual function of removing the cleaning chemicals from the surface and ending the etching action of an oxide etch. Great quantities of DI water, and great expense, are expended to achieve the goal of clean wafers. Rinsing is done by several different methods. Future focus will be on higher rinse efficiency and an order of magnitude reduction in quantity. The 1997 NTRS calls for reducing the present 30 gal/in^2 of silicon to 2 gal/in^2 of silicon in the 50-nm gate size sometime around 2012.

Overflow rinsers. The need for atomically clean surfaces precludes just dunking the wafers in a tank of water. Thorough rinsing requires a continuous supply of clean water to the wafer surface. One such method is an overflow rinser (Fig. 5.29). It is a box sunk into the cleaning station deck. Deionized water is brought into the bottom of the box and flows through and around the wafers, exiting over a dam into a drain system. The rinsing action of the flowing water is enhanced by a stream of nitrogen bubbles introduced into the rinser from the bottom plate. As the nitrogen *bubbles* up through the water, it aids the mixing of the chemicals on the wafer surface with the water. This type of sys-

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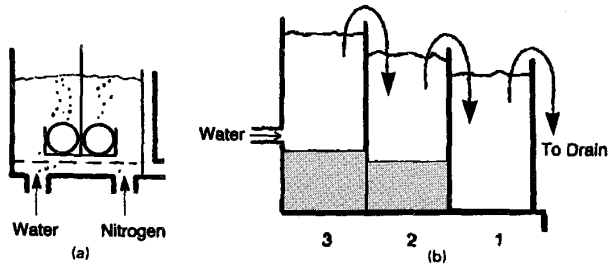


Figure 5.29 Rinse systems. (*a*) Single overflow and (*b*) three-stage overflow.

tem is often called a *bubbler.* A variation is the *parallel downflow rinser.* In this configuration, the water is brought into the system outside the rinser and directed to flow down through the wafers (Fig. 5.30).

A rule of thumb is that adequate rinsing takes a minimum of five minutes (depending on wafer diameter) with a flow rate equivalent to five times the volume of the rinser per minute (the number of turnovers per minute). If the size of the bubbler is 3 L, the flow rate should be a minimum of 15 L/min.

The rinse time is determined by measuring the resistivity of the water as it exits the rinser. Cleaning chemicals act as charged molecules in the rinse water, and their presence can be inferred from the electrical resistivity of the water. If the water goes into the rinser at an 18-MΩ level, a reading of 15 to 18 MΩ on the exit side indicates that the wafers are cleaned and rinsed. The rinsing step is so critical that, generally, a minimum of two rinsers are used, and the total rinsing time is set at two to five times the minimum determined by resistivity

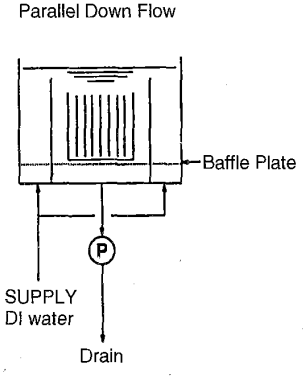


Figure 5.30 Parallel downflow rinsing. *(Courtesy of Walter Kern.)*

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measurements. Often, a water resistivity meter is mounted on the outlet to constantly measure the output resistivity and signal when rinsing is completed.

Spray rinsing. Flowing water removes a water-soluble chemical from the wafer surface by a dilution mechanism. The top layer of the chemical dissolves into the water and is carried away by the flow. This action occurs over and over in a continuous manner. Rinsing is speeded up by a faster water flow rate, which can remove the dissolved chemical more quickly. The number of turnovers directly determines the rinse rate. This can be understood by considering a very fast water flow rate, but in a huge rinse tank. The chemical removed from the wafer surface would be evenly distributed throughout the tank, and therefore some would still cling to the surface. The chemical could be removed from the tank only when enough water has flowed in and out of it to carry away the chemical.

One way to have a faster rinse rate is by using a water spray. The spray removes the chemical with a physical force from its own momentum, and the many small droplets continually hitting the wafer surface have the effect of an extremely high turnover rinse. Along with more efficient rinsing, a spray rinser uses considerably less water than an overflow rinser. A problem with a spray rinser comes when the resistivity of the exiting water is measured with a resistivity monitor. Carbon dioxide from the air gets trapped in the water spray; the CO_2 molecules act as charged particles, and the resistivity meter reads them as contaminants, which they aren't.

Dump rinsers. With respect to rinsing efficiency and water savings, a dump rinser (Fig. 5.31) is an attractive method. The system is like an overflow rinser but with a spray capability. The wafers are placed into the dry rinser and immediately sprayed with deionized water. While

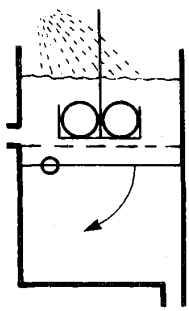


Figure 5.31 Ultrasonic/megasonic wafer cleaning/etching bath.

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they are being sprayed, the cavity of the rinser is rapidly filled with water. As the water overflows the top, a trap door in the bottom swings open, and the water is dumped instantly into the drain system. This fill-and-dump action is repeated several times until the wafers are entirely rinsed.

Dump rinsing is also favored, because all of the rinsing takes place in one cavity, which saves equipment and space. It is also a system that can be automated, so the operator only needs to load the wafers in (this can be done automatically) and push a button.

Sonic-assisted cleaning and rinsing. The addition of sonic energy waves to a tank of cleaning chemicals or a rinse system aids and speeds wet processes. Use of sonic waves can increase efficiency, which in turn allows a lower bath temperature. Sonic waves are energy waves generated from transducers arranged on the outside of the tank (See Fig. 5.32). Two ranges are used. In the 20,000 to 50,000 hertz (1 hertz (Hz) = one cycle per second) range, they are called *ultrasonic* and, in the 850 kilohertz (kHz) range, they are called *megasonic* waves.[40] Ultrasonic assists rinsing through cavitation. The waves pass through the liquid, causing microscopic bubbles to form and collapse rapidly. This creates a microscopic scrubbing action that dislodges particles. The phenomenon is called *cavitation*. Megasonic assist offers a different mechanism. In fluid dynamics, there is a static or slow-moving boundary at surfaces, such as wafers. Small particles can be held in this layer, unexposed to the cleaning chemicals. Megasonic energy reduces this layer, exposing the particles to cleaning action. In addition, a phenomenon called *acoustic streaming* fosters an increase in the velocity of the rinse or cleaning solutions passing the wafer surface, increasing cleaning efficiency.[41]

Spin-rinse dryers (SRDs). After rinsing, the wafers must be dried. This is not a trivial process. Any water that remains on the surface (even atoms) has the potential of interfering with any subsequent operation. There are three drying techniques (with variations) used.

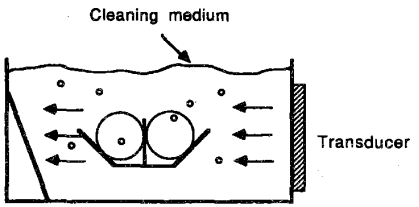


Figure 5.32 Ultrasonic/megasonic wafer cleaning/etching bath.

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Drying techniques

- Spin rinse dryers
- Isopropyl alcohol (IPA) vapor dry
- Surface tension/Marangoni drying

Complete drying is accomplished in a centrifuge-like piece of equipment. In one version, the wafer boats are put in holders around the inside surface of a drum. In the center of the drum is a pipe with holes, and it is connected to a source of deionized water and hot nitrogen (Fig. 5.33).

The drying process actually starts with a rinse of the wafers as they rotate around the center pipe that sprays the water. Next, the SRD switches to a high-speed rotation as heated nitrogen comes out of the center pipe. The rotation literally throws the water off the wafer surfaces. The heated nitrogen assists in the removal of small droplets of water that may cling to the wafer.

SRDs are also built for drying single-wafer boats. The boat slips into a rotating holder in the center of a chamber. The water and nitrogen come into the chamber through its side rather than through a pipe in the center. The rinsing and drying take place as the boat spins about its own axis. This type of SRD is called an *axial dryer*. These two machines are used for automatic wafer cleaning and etching. As a wafer cleaner, the required chemicals are plumbed to the machine, and microprocessor-controlled valves direct the right chemicals into the chamber.

Isopropyl alcohol (IPA) vapor drying. A recently rediscovered drying technique is alcohol drying (Fig. 5.34). In the bottom of the dryer is a

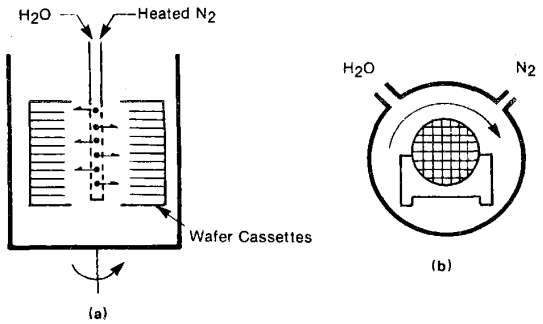


Figure 5.33 Spin rinse dryer styles. (*a*) Multiboat and (*b*) single-boat axial.

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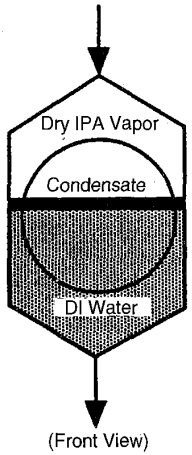


Figure 5.34 Vapor dry. *(Courtesy of Walter Kern.)*

heated reserve of liquid IPA with a vapor cloud (vapor zone) above it. When a wafer with residual water on the surface is suspended in the vapor zone, the IPA replaces the water. Chilled coils around the vapor zone condense the water vapor out of the IPA vapors, leaving the wafers water free. A variation is the *direct displacement vapor dryer.* In this system, the wafers are pulled out of a DI water bath directly into an IPA vapor zone where the water displacement occurs.

Surface tension/Marangoni drying. Water surface tension creates a unique condition when wafers are pulled slowly through a water surface. The tension draws the water away from the surface, leaving it dry. This effect is enhanced when a flow of an organic, such as IPA and nitrogen, is directed at the wafer water level interface. The IPA/N_2 flow creates a surface tension gradient, which in turns causes a water flow from the surface into the water. This internal flow further enhances the removal of water from the wafer. In practice, the wafers are either withdrawn from the water bath, or the water is allowed to slowly recede from the rinse tank.[42]

Contamination detection/summary

The detection of the various forms of contamination is detailed in Chapters 8 and 14. Figure 5.35 summarizes the specifications for cleanroom cleanliness.

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Year of Production	2001	2006	2012
Line width (nm)	150	100	50
Air Critical Particle Size (nm)	8	2	1
Water oxidizable carbon (ppb)	1	<1	<1
Water Dissolved Oxygen (ppb)	1-10	1	1
Water Particles>critical size	<0.2 per mL	<0.2 per mL	<0.2 per mL
Liquid Particles>critical size	<0.5 per mL	<0.5 per mL	<0.5 per mL
HCl, H2O impurities (ppt)	<1000	<1000	<1000
BEOL solvents K,Li,Na (ppt each)	<1000	<1000	<1000
POU Gases particles (per liter)	2	2	2

Figure 5.35 SIA Roadmap Projections *(Source:* Micro, *October 1998, p. 54.)*

Review Questions

1. State the class number required for VLSI processing and ULSI processing.
2. List three techniques used to keep contamination out of a cleanroom.
3. Draw a cross section of a "total" cleanroom, showing the filters and air patterns.
4. What does VLF mean?
5. What is the DI water specification?
6. Name three contaminants found in normal water.
7. What are the two ways that static is harmful in a fabrication area?
8. Explain the problem associated with high humidity in a fabrication area.
9. What is a mobile ionic contaminant, and why is it unwanted in a fabrication area?
10. How does a service bay contribute to the cleanliness of a cleanroom?
11. Describe a mini-environment.
12. Describe and sketch a SMIF/micro-environment unit.
13. List four types of contamination found on wafer surfaces.
14. List a cleaning chemical or chemical solution for each contaminant listed in question no. 13.
15. Describe the major techniques used to dry wafers.

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Chapter

6

Productivity and Process Yields

Overview

Wafer fabrication and packaging are incredibly long and complex processes involving hundreds of demanding steps. These steps are never performed perfectly every time, and contamination and material variations combine to wafer loss in the process. Additionally, some of the individual chips on the wafers fail to meet customer electrical and performance specifications. In this chapter, the major yield measurement points are identified along with the major process and material factors that effect yield. Typical yields for the different yield points and for different circuits are presented.

Objectives

Upon the completion of this chapter, you should be able to:

1. Name the three major yield measurement points in the process.
2. Explain the effect of wafer diameter, die size, die density, number of edge die, and defect density on the wafer-sort yield.
3. From a list of individual process step yields, calculate the accumulative fabrication yield.
4. Be able to explain and calculate an overall process yield.
5. Explain the four major influences on fabrication yield.
6. Sketch a yield-versus-time curve for different process and circuit maturities.
7. Explain the relationship between high process yields and device reliability.

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Yield Measurement Points

Maintaining and improving process and product *yields* is the lifeblood of semiconductor manufacturing. To the casual observer, it would seem that the industry is fixated on production yields. It is. The demanding nature of the process and sheer number of processes required to produce a packaged chip result in product loss. These two factors result in a production process that typically ships only 20 to 80 percent of the chips it commits into the wafer-fabrication line.

These yields seem extraordinarily low compared to most manufacturing operations. Yet, when one considers the challenge of producing hundreds of circuits, composed of millions of micron-size patterns in layers that are equally thin, at very stringent cleanliness levels, all within the confines of a 0.5-in^2 chip, it is a testament to the industry that any chips are produced at all.

Another factor that helps keep yields depressed is the nonrepairable nature of most production mistakes. While defective automobile parts can be replaced, few such options are available in semiconductor manufacturing. Defective chips or wafers generally cannot be recovered. In some cases, chips that fail performance tests can be downgraded for sale for a less demanding use. Scrapped wafers may find a new life as control wafers or "dummies" (see discussions of oxidation in Chapters 5 and 7).

Added to these process factors is the volume nature of the business. High capital costs and a higher-than-average percentage of engineering personnel translate to a high-overhead situation. This high overhead, coupled with competition that keeps downward pressure on selling prices, requires that most chip producers run a high-volume, high-yield process.

Given all of these factors, the preoccupation with yield is understandable. Most suppliers of equipment and materials tout the yield improvements possible with their products. Likewise, process engineering groups have as their prime responsibility the maintenance and improvement of process yields. Yield measurement starts at the individual process level and is tracked through the entire process sequence, from incoming blank wafer to shipment of the completed circuit.

Typically, a plant will monitor yields at three major points in the process. They are at the completion of the wafer fabrication processes, after wafer sort, and at the completion of the packaging and final test processes (Fig. 6.1).

Accumulative Wafer-Fabrication Yield

The first major yield measurement point is at the completion of wafer fabrication. This yield is called by a variety of names, including fab yield, line yield, accumulative fab yield, or "cum" yield.

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Major Yield Measurement Points

Manufacturing Stage	Measured
Wafer Fabrication- Yield =	# Wafers Out / # Wafers Started
Wafer Sort- Yield =	# Functioning (Good) Die / # Die On Wafer(s)
Packaging- Yield =	# Packages Die Passing Final Test / # Good Die Started Into Packaging

Figure 6.1 Major yield measurement points.

Whatever the name, it is expressed as a percentage of the wafers leaving the wafer fab divided by the number that entered the process. Since different product types have different components, feature sizes, and density factors, the wafer fab yield is calculated by product type rather than the entire fabrication line yield.

The cum fab yield starts by first calculating the number of wafers that leave each of the individual processes (called *station yields*) and dividing by the number that entered the station.

$$\text{Station yield} = \frac{\text{Number of wafers leaving station}}{\text{Number of wafers entering station}}$$

The station yields are in turn multiplied together to calculate the overall cum fab yield.

$$\text{Cum fab yield} = Y(\text{station } 1) \times Y(\text{station } 2) \times \ldots \times Y(\text{station } n)$$

Figure 6.2 lists an 11-step process such as the one illustrated in Chapter 5. Typical station yields are listed in column 3 and the accumulated yield in column 5. For a single product, the cum fab yield calculated from the station yields is the same as the yield calculated by dividing the number of wafers *out* by the number of wafers *in*. The accumulated yield equals the simple cum fab yield calculation for this individual circuit. Note that, even with very high individual station yields, the cum fab yield will continue to fall as the wafers come through the process. A modern integrated circuit will require 300 to 500 individual process steps, which represents a huge challenge to maintain profitable productivity. Successful wafer fabrication operations must achieve accumulative fabrication yields over 90 percent to stay profitable and competitive.

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Step	Wafers in	Yield*	Wafers out	Accumulated yield
1. Field oxidation	1000	99.5	995	99.5
2. Source/drain mask	995	99.0	965	96.5
3. Source/drain doping	965	99.3	978	97.8
4. Gate region mask	978	99.0	968	96.8
5. Gate oxidation	968	99.5	964	96.4
6. Contact hole mask	964	94.0	906	90.6
7. Deposit metal layer	906	99.2	899	89.9
8. Metal layer mask	899	97.5	876	87.6
9. Alloy metal layer	876	100	876	87.6
10. Passivation layer deposition	876	99.5	872	87.2
11. Passivation layer mask	872	98.5	859	85.9

*Yield values are typical for the particular steps.

Figure 6.2 Accumulated (wafer fab) yield calculation.

Wafer-fabrication cum yields vary from 50 to 95 percent, depending on a number of factors. The calculated cum yield is used for production planning and by engineering and management and as a measure of the process effectiveness.

Wafer-Fabrication Yield Limiters

Wafer-fabrication yield is limited by a number of factors. The five listed below are fundamental factors that must be controlled in any wafer-fabrication facility. These basic factors, in combination with device or circuit specific factors, result in the overall yield of good chips out of a given facility.

1. Number of process steps
2. Wafer breakage and warping
3. Process variation
4. Process defects
5. Mask defects

Number of process steps

Note in the calculation in Fig. 6.2 that each individual process operation yield must be in the high 90 percent range to produce the 85.9

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percent cum fab yield. Illustrated is a fairly simple 11-step process. ULSI circuits require hundreds of major process operations. Into the year 2012, the total number of major steps will reach 600.[1] Each operation requires several steps, each of which in turn involves a number of substeps. It is easy to appreciate the continual pressures on fabrication areas to maintain high cum yields generated by the number of process steps. The more complicated the circuit, with a high number of steps, the lower the expected cum yield.

More process steps also increase the probability that one of the other four yield limiters will affect the wafer during the process. This factor is a tyranny of numbers. For example, to achieve a 75 percent accumulated fabrication yield with a 50-step process, each of the individual steps would have to be 99.4 percent! A further tyranny of this type of calculation is that the cum yield can never exceed the lowest individual step yield. If one process step can achieve only a 50 percent yield, the overall cum yield can never be higher than 50 percent.

More manufacturing pressure is present in the fact that, for each major process operation, there are a number of steps and substeps. In the illustrated 11-step process, the first operation is oxidation. A simple oxidation process requires several steps: cleaning, oxidation, and evaluation. Each of the steps requires substeps. Figure 6.3 lists the eight substeps for a typical oxidation process. Each of the substeps represents an opportunity to contaminate, break, or damage the wafer.

Substep	Number of Wafer Handlings
1. Wafers are removed from carrier and placed in cleaning boat.	2
2. Wafers are cleaned, rinsed, and dried.	1
3. Wafers are removed from cleaning boat, inspected, and placed on oxidation boat.	2
4. Boat is removed from furnace.	0
5. Wafers are removed from boat and placed back in carrier.	1
6. Test wafers are removed from carrier and measured.	2
TOTAL NUMBER OF HANDLINGS	8

Figure 6.3 Substeps of oxidation process.

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Wafer breakage and warping

During the course of the fabrication process, the wafers are handled many times by a combination of manual and automatic techniques. Each handling presents an opportunity to break the relatively fragile wafers. A typical 300-mm (12-in) diameter wafer is only about 800 μm thick. Careful wafer handling is a required, and automatic handlers must be maintained to minimize breakage.

Heat treatments add to the susceptibility of the wafers to breaking. Strains are induced in the crystalline material that make them vulnerable to breaking in subsequent steps. Automatic processing machines accommodate only full-diameter wafers. Therefore, any breakage, however small, is a cause for rejecting the wafer from the process.

Silicon wafers are relatively easy to handle with good practices, and automatic equipment has reduced wafer breakage to a low level. Gallium arsenide wafers, however, are not that resilient, and breakage is a major wafer-yield limiter. In gallium arsenide fabrication lines, where the circuits command a high selling price, partial wafers are often processed.

Along with minimizing breakage, the wafer surfaces must remain flat throughout the processing. This is especially true on fabrication lines that use patterning techniques that project the pattern onto the wafer surface. If the surface is warped or wavy, the projected image will become distorted and change the required image dimensions. This is similar to projecting a slide onto a distorted screen. Warping comes about from rapid heating and/or cooling of the wafers in tube furnaces. (The solution for this problem is addressed in Chapter 7.)

Process variation

As the wafer comes through the fabrication process, it receives a number of doping, layering, and patterning processes, each of which must meet incredibly stringent physical and cleanliness requirements. But even the most sophisticated processes vary from wafer to wafer, lot to lot, and day to day. When a process exceeds its process limits (goes out of spec), it will cause some unallowed result on the wafer or within the chips on the wafer.

A goal of process engineering and process control programs is not only to keep each process operating within its control specifications but to maintain a constant distribution of the process parameters, such as time, temperature, pressure, and others. These process parameters are monitored with statistical *process control techniques* explained in Chapter 15.

Throughout the process, there are a number of inspections and tests designed to detect unwanted variations as well as frequent calibration

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of the equipment parameters to process specifications. Some of these tests are performed by production personnel and some by quality control organizations. However, even the best maintained and monitored process exhibits some variations. One of the challenges of process engineering and circuit design is to accommodate the variations and still have a functioning device.

Process defects. Process defects are defined as isolated regions (or spots) of contamination or irregularities on the wafer surface. These defects are often called *spot defects* or *point defects*. They occur randomly on the wafer surface. Some are non-fatal, and some will render the circuit inoperable. These are called *killer defects* (see Fig. 6.11, p. 151). Unfortunately, smaller defects are sometimes not detectable during the fabrication process. They become evident at wafer sort as rejected chips.

The major sources of these defects are the various liquids, gases, room air, personnel, process machines, and water used in the fabrication area. Particulates and other small contaminants become lodged in or on the wafer surface. Many of these defects occur in the patterning process. Recall that the patterning process requires using a thin, fragile layer of photoresist to protect the wafer surface during the etch steps. Any holes or tears in the photoresist layer from particulates will end up as tiny etched holes in the wafer surface layer. These holes are called *pinholes* and are a major concern of photomasking engineers. Consequently, the wafers are inspected often for contamination, usually after each major step for contamination. Wafers that exceed the established allowable density are rejected. The SIA *International Technology Roadmap for Semiconductors* (ITRS) calls for maximum defect densities on 300-mm wafer surfaces of 0.68 per square centimeter (cm^2).

Mask defects

A photomask or reticle is the source of the pattern that is transferred to the wafer surface in the patterning process. Defects on the mask/reticle end up on the wafer as defects or pattern distortions. There are three common mask/reticle originated defects. First is contamination, such as dirt or stains on the clear part of the mask/reticle. In optical lithography, they can block the light and print onto the wafer as though they were an opaque part of the pattern. Second are cracks in the quartz. They, too, can block the patterning light and/or scatter the light, causing unwanted images and/or distorted images. Third are pattern distortions that occur in the mask/reticle making process. These include pinholes or chrome spots, pattern extensions or missing

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parts, breaks in the pattern, or *bridges* between adjacent patterns (Fig. 6.4).

Control of mask generated defects is more critical for device/circuits with smaller feature sizes, higher densities, and larger die sizes.

Wafer-Sort Yield Factors

After fabrication, the wafers go to the wafer sort tester. During the test, each chip will be tested electrically for device specifications and

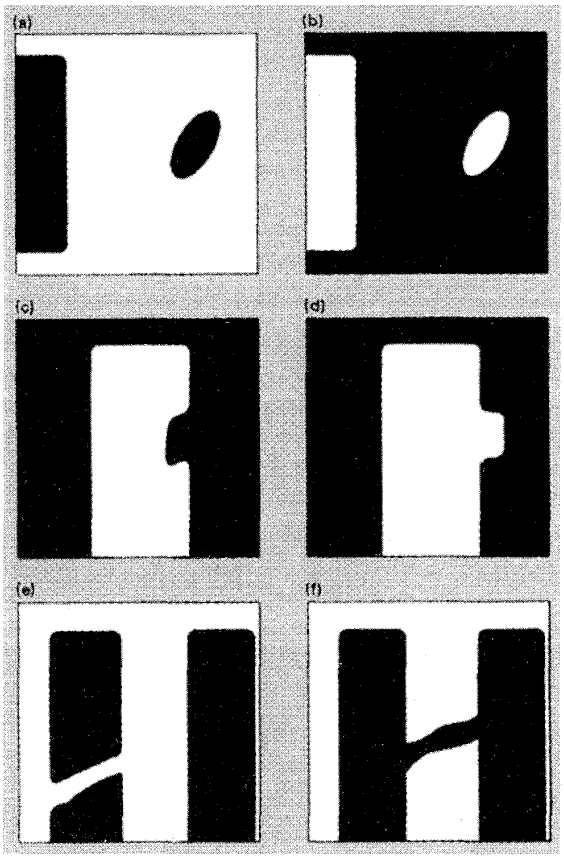


Figure 6.4 Mask defects. (*a*) Spot, (*b*) hold, (*c*) inclusion, (*d*) protrusion, (*e*) break, (*f*) bridge. *(Source:* Solid State Technology, *July 1993, p. 95.)*

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functionality. Up to several hundred individual electrical tests may be performed on each circuit. While these tests measure the electrical performance of the device(s), they indirectly measure the precision and cleanliness of the fabrication processes. Because of natural process variations and undetected defects, the wafer may have passed all the in-process checks and still have many chips that do not function.

Since wafer sort is a comprehensive test, many factors influence the yield. They are:

1. Wafer diameter
2. Die size (area)
3. Number of processing steps
4. Circuit density
5. Defect density
6. Crystal defect density
7. Process cycle time

Wafer diameter and edge die

The semiconductor industry went to round wafers with the introduction of silicon. The first wafers were less than one inch in diameter. Since that time, there has been a regular progression to larger-diameter wafers, with 150 mm (6 in) being the standard of VLSI fabrication lines in the late 1980s, and 200-mm wafers being developed for production use in the 1990s. Projections call for 300- and 450-mm diameter wafers early in this century.[3]

The move to larger-diameter wafers has been driven by production efficiency, increasing die sizes, and the influence on the wafer-sort yield. Production efficiency is easily understood when one considers that there is an incremental increase in the cost of processing a larger-diameter wafer, while the number of available whole chips on the wafer can increase substantially as illustrated in Fig. 6.5.

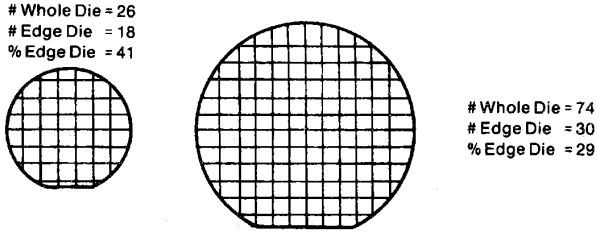


Figure 6.5 Effect of larger wafer diameter on percentage of partial die.

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The effect of increasing the wafer diameter also has positive effects on the wafer-sort yield. Figure 6.6 shows two wafers of the same diameter but with different die sizes. Note that the smaller-diameter wafer has a very large proportion of its surface covered with partial die—die that cannot function. The larger-diameter wafer, with its greater number and percentage of whole die, if all other factors are equal, will have a higher wafer-sort yield.

Wafer diameter and die size

Another driving force for larger-diameter wafers is the trend to larger die sizes. As shown in Fig. 6.6 increasing the die size *without* increasing the wafer diameter also results in a wafer surface with a smaller percentage of whole die. Maintaining a decent wafer-sort yield as the die size increases requires increasing the wafer diameter. Figure 6.7 lists the number of various size chips that will fit on different size wafers. The bottom line is that larger-diameter wafers are more cost effective.

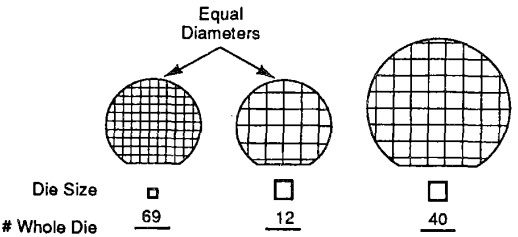


Figure 6.6 Effect of larger wafer diameter on percentage of partial die.

	Wafer diameter (mm)		
Die size (mils)	150	200	300
300 × 300	293	531	820
400 × 400	113	165	550
500 × 500	108	191	410

Figure 6.7 Die size versus number of die on wafer.

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Wafer diameter and crystal defects

In Chapter 3, the concept of a crystal dislocation was introduced. A crystal dislocation is a point defect *in the wafer* that comes from a local discontinuity of the crystal structure. Dislocations exist throughout the crystal structure and, like contamination and process defect density, affect the wafer-sort yield.

Dislocations also are generated during the fabrication process. They generate (or nucleate) at sites where there are chips and abrasions of the edge of the wafer. These chips and abrasions come from poor handling techniques and automatic handling equipment. The abraded area causes a crystal dislocation. Unfortunately, the dislocation is propagated into the center of the wafer (Fig. 6.8) during subsequent heat treatments, such as oxidations and diffusions. The length of the dislocation line into the interior of the wafer is a function of the thermal history of the wafer. Consequently, wafers receiving more process steps and/or more heating steps will have more and longer dislocation lines affecting a greater number of chips. One obvious solution to the problem is larger-diameter wafers, which leaves a larger number of unaffected die in the center of the wafer.

Wafer diameter and process variations

The process variations discussed in the section of wafer fabrication yields affect the wafer-sort yield. In the fabrication area, process variations are detected by sampling inspection and measurement techniques. The nature of inspection sampling is that not all of the variations and defects are detected, so that wafers are passed on with some number of problems. These problems show up at wafer sort as failed devices.

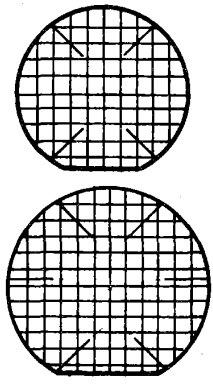


Figure 6.8 Effect of dislocations on wafer-sort yield for different wafer dimensions.

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Process variations occur at a higher rate around the edge of the wafer. In the high-temperature processes performed in tube furnaces, there is always some temperature nonuniformity across the wafers. The change in temperature results in uniformity differences on the wafer. Variations occur more at the wafer outer edges where heating and cooling occur at a faster rate. Another contributor to this wafer edge phenomenon is contamination and physical abuse of the wafer layers that emanates from handling and touching the wafers on their edges. In the patterning process, there can be feature size uniformity problems in the mask-driven processes (full mask projection, proximity and contact exposure). The nature of the light systems is such that the center will be of higher uniformity than the outside edges. In the reticle-driven masking processes (steppers), there is a smaller area of exposure (one or several die), which reduces the image variations across the wafer.

All of these problems result in a lower wafer-sort yield around the edge of the wafer, as illustrated in Fig. 6.9. Larger-diameter wafers help to maintain wafer-sort yields by having a larger area of unaffected die in the center of the wafer.

Die area and defect density

The die size also affects wafer-sort yield relative to the defect density on the wafer surface. The relationship is illustrated in Fig. 6.10. In Fig. 6.10*a*, a wafer is shown with five defects and no die pattern. This situation illustrates a background defect density produced by all of the fab area factors, regardless of the die size, device type, process control requirements, and so forth. The wafers in Fig. 6.10*b* and *c* illustrate the effect of this background defect density on the wafer-sort yield for two different die sizes. The larger the die size for a given defect density, the lower the yield.

Circuit density and defect density

The defects on the wafer surface result in die failures by causing a malfunction of some part of the die. Some of the defects are located in

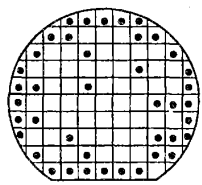


Figure 6.9 Typical location of functioning die after wafer sort.

• Nonfunctioning Die

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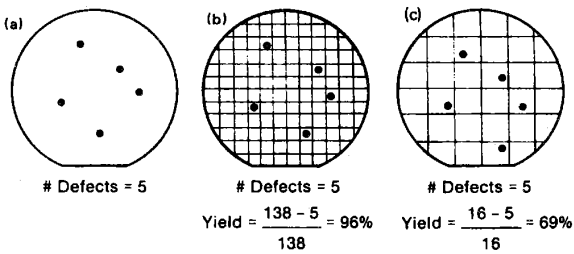


Figure 6.10 Effect of background defects on wafer-sort yield for different die sizes.

nonsensitive parts of the die and do not cause a failure. However, the trend is to higher levels of circuit integration, which came about because of smaller feature size and a higher density of die components. The result of these trends is a higher probability that any given defect will be in an active part of the circuit, thus lowering the wafer-sort yield as illustrated in Fig. 6.11.

Number of process steps

The number of process steps was indicated as a limiter of the fab cum yield. The more steps, the greater the opportunities to break or misprocess a wafer. The effect also influences the wafer-sort yield. As the number of process steps increases, the background defect density increases unless procedures are implemented to lower it. A higher background defect density affects more chips, lowering the wafer-sort yield.

Feature size and defect size

Smaller feature sizes make maintaining an acceptable sort yield difficult from two major factors. First, the smaller images are more difficult to print (see "Mask defects" section, p. 145, and Chapter 8). Second, the

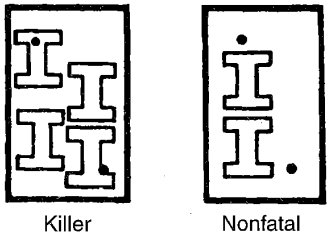


Figure 6.11 Killer defects (failed die) and nonfatal (passed die) defects.

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smaller images are vulnerable to ever-smaller defect sizes as well as the over all defect density. The 10:1 rule of minimum feature size to allowable defect size has been discussed. One assessment is that, at a defect density of 1 defect per cm^2, a circuit with 0.35-μm feature size will have a wafer-sort yield 10 percent less than that of a 0.5-μm circuit processed under the same conditions.[4]

Process cycle time

The time that the wafers are actually being processed can be measured in days. But due to queuing at the process stations and temporary slowdowns due to process problems, the wafer often stays in the fab area for several weeks. The longer the wafer is sitting around, the more opportunity for contamination that lowers wafer-sort yield. The move to just-in-time manufacturing (see Chapter 15) is one attempt to increase yields and decrease the manufacturing costs associated with increased in-line inventories.

Wafer-sort yield formulas

The ability to understand and predict wafer-sort yields with some accuracy is essential to the operation of a profitable and reliable chip supplier. Over the years, a number of models have been developed that relate process, defect densities, and chip size parameters to the wafer-sort yield. Five yield model formulas are shown in Fig. 6.12. Each relates different parameters to the wafer-sort yield. As the chips get larger, the number of process steps increases, the feature size decreases the sensitivity to smaller defect sizes increases, and more of the background defects become killer defects.

Negative binomial

$$Y_r = \frac{1}{\left(1 + \frac{AD_0}{\alpha}\right)^{\alpha}}$$

Murphy

$$Y_r = \left(\frac{1 - e^{-AD_0}}{AD_0}\right)^2$$

Bose-Einstein

$$Y_r = \frac{1}{(1 + AD_0)^n}$$

Seeds

$$Y_r = e^{-\sqrt{AD_0}}$$

Poisson

$$P(k) = \frac{\lambda^k k e^{-\lambda}}{k!}$$

$$Y_r = P(0) = e^{-\lambda} = e^{-AD_0}$$

$$Y_r = \int_0^{\infty} F(D) e^{-AD} d$$

Figure 6.12 Wafer-sort yield models.

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Exponential model. The exponential relationship (Fig. 6.12*a*) or Poisson model is the simplest and one of the first yield models[5] developed. It is applicable to individual process steps and assumes a random distribution of defects (D_0) across the wafer. For multistep analysis, the factor (n) equating to the number of process steps is used (Fig 6.12*b*). This model generally is used for products that contain over 300 die and MSI circuits of lower densities. Die sizes that are smaller are predicted by the Seeds model.

The exponential, Poisson, and Seeds models all illustrate the primary relationship between die area, defect density, and wafer-sort yield. In these, e is a constant with a value of 2.718.

B. T. Murphy proposed a model using a more sophisticated distribution of defects. The Bose-Einstein model adds the number of process steps (n), In the *negative binomial* model, there is a cluster factor. It accounts for defect distributions that tend to be "clustered" on the wafer surface rather than simply exhibiting a random distribution. Adopted by the SIA in the *ITRS*, the cluster factor is assigned a value of 2.[5]

In most yield models, the factor for processing steps (n) is actually the number of patterning steps. Experience has proved that the patterning steps contribute the greatest number of point defects and therefore have a direct bearing on sort yield.

Figure 6.13 illustrates the different predictions of the various yield models.[6] No two complex circuits have comparable designs or processes. Processes vary from company to company, as does the basic background defect density. These factors make the development of an accurate universal yield model difficult. Most chip companies have developed their own models that reflect their particular manufacturing process and product designs. The models are all defect driven. That is, they assume that all of the fab processes are under control and that the defect levels are those built into the process. They do not include major process problems, such as a contaminated tank of process gas.

The defect density used in all the models is not the same as a defect density determined by optical inspection of the wafer surface. The defect density that shows up in the yield models is all-inclusive; it includes contaminants and surface and crystal defects. Further, it predicts only the defects that destroy die: the "killer defects." Defects that fall in noncritical areas of the chip are not part of the models, nor are situations where two or more defects fall in the same sensitive area.

It is also important to keep in mind that the yield numbers predicted by the formulas are those expected from a process that is basically under control. In reality, the wafer-sort yield will vary from

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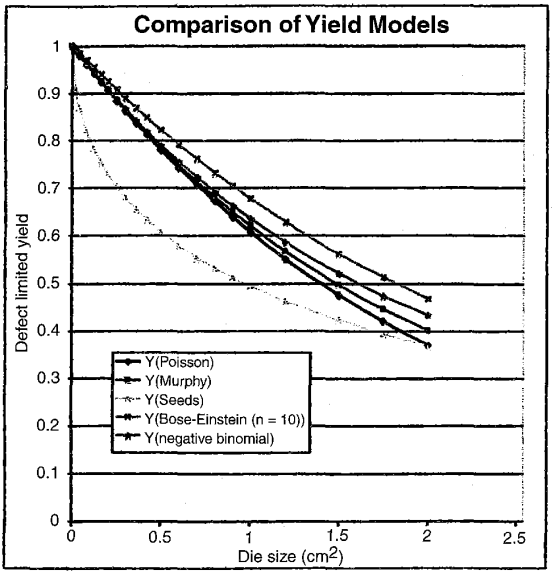


Figure 6.13 Yield models showing the die yield as a function of die size defect density.

wafer to wafer because of the normal process variations in the fabrication process. A typical wafer-sort yield plot is shown in Fig. 6.14.

Note that wafer 13 falls far below the normal range of sort yields. In a situation like this, the process engineer would look for some catastrophic process failure such as an out-of-spec layer thickness or a doping layer that is too deep or too shallow.

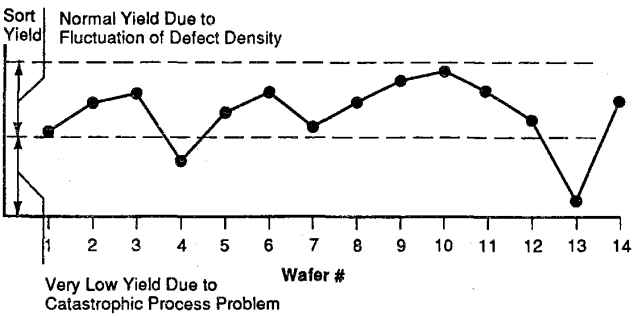


Figure 6.14 Plot of wafer-sort yields.

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Assembly and Final Test Yields

After wafer sort, the wafers go to the packaging process, also called *assembly and test*. There, the wafers are separated into the individual die and packaged into a protective enclosure. During this series of steps, there are a number of visual inspections and quality checks of the assembly process.

The last steps of the packaging process is a series of physical, environmental, and electrical tests, known collectively as the *final tests*. (The details of the processes, inspections, and final tests are described in Chapter 18.) After the final tests, the third major yield is calculated, which is the ratio of die passing the final tests compared with the number of *good die* that entered packaging after passing the wafer-sort test.

Overall Process Yields

The overall process yield is the mathematical product of the three major yield points (Fig. 6.15). This number, expressed in percent, gives the percentage of shipped die as compared with the number of whole die on the starting wafer. It is an inclusive measurement of the success of the entire process.

Overall yields vary with several major factors. In Fig. 6.16 is a list of typical process yields and their calculated overall yield. In the first two columns are major process factors that influence the individual and overall yields.

First is the integration level of the particular circuit. The more highly integrated the circuit, the lower the expected yield in all categories. Higher integration levels assume a corresponding decrease in feature size. Column 2 lists the maturity of the manufacturing process. Process yields almost always follow an *S* curve pattern (Fig. 6.17) through the lifetime of the product in manufacturing. In the beginning, the yield rises rather slowly as the initial bugs are worked out of the process. This is followed by a period when the yields rise rapidly, eventually leveling off as the limits imposed by the process maturity

Overall Yield Formula

(Wafer Fab Yield) (Wafer Sort Yield) (Packaging Yield) = Overall Yield

$$\frac{\#\text{ Wafers Out}}{\#\text{ Wafers Started}} \times \frac{\#\text{ Functioning (Good) Die}}{\#\text{ Die On Wafer(s)}} \times \frac{\#\text{ Packages Passing Final Test}}{\#\text{ Die Started Into Packaging}} = \text{Overall Yield}$$

Figure 6.15 Overall yield formula.

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Integration Level	Product Maturity	Fab Yield %	Sort Yield %	Assembly Final Test %	Overall Yield %
ULSI	Mature	95	85	97	78
ULSI	Mid	88	65	92	53
ULSI	Introduction	65	35	70	16
LSI	Mature	98	95	98	91
Discrete	Mature	99	97	98	94

Figure 6.16 Typical yields for various products.

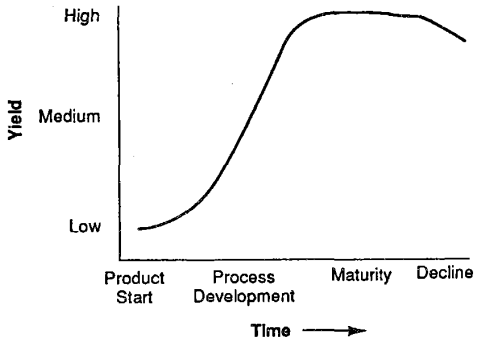


Figure 6.17 Yield changes with process maturity levels.

die size, integration level, circuit density, and defect density. As the table in Fig. 6.16 shows, overall yields can vary from very low (maybe even zero for new or poorly designed products) to the 90 percent range for simpler and mature products. Semiconductor producers consider their yield performance very proprietary, since profit and production control are a direct function of the process yields.

An examination of the yield values in the table reveals that wafer-sort is the lowest of the three yield points. This fact illustrates why yield-improvement programs are directed at the many factors that influence the wafer-sort yield. At one time, the improvement of wafer-sort yields had the biggest impact factor on productivity. The advent of larger and more complex chips (such as the megabit memories) has shifted productivity improvements to include other factors, including the cost of ownership of equipment (see Chapter 15). Successful competition in the mega-chip era will require wafer-sort yields 90 percent or higher.[7]

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Review Questions

1. Name the three yield measurement points in the manufacturing process.
2. Of the three yield points, which is typically the lowest?
3. Indicate if the wafer-sort yield would go up or down with the following changes:

   a. Change to larger-diameter wafers

   b. Change to smaller die size

   c. More process steps

   d. Decrease in defect density

   e. Increase in die density
4. If 1000 wafers are started into the process and 875 are passed to wafer sort, what is the accumulated fabrication yield?
5. Calculate the overall yield for a process that has an 82 percent fabrication yield, a 47 percent wafer-sort yield, and a 92 percent assembly and final test yield.
6. Which situation would you expect to have the highest overall yield, a 22-step LSI process or a 33-step VLSI process?

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Chapter

7

Oxidation

Overview

The ability of a silicon surface to form a silicon dioxide passivation layer is one of the key factors in silicon technology. In this chapter, the uses, formation, and processes of silicon dioxide growth are explained. Detailed is the all-important tube furnace, which is a mainstay of oxidation, diffusion, heat treatment, and chemical vapor deposition processes. Other oxidation methods, including rapid thermal processing, are also explained.

Objectives

Upon completion of this chapter, you should be able to:

1. List the three principal uses of a silicon dioxide layer in silicon devices.
2. Describe the mechanism of thermal oxidation.
3. Sketch and identify the principal sections of a tube furnace.
4. List the two oxidants used in thermal oxidation.
5. Sketch a diagram of a dryox oxidation system.
6. Draw a flow diagram of a typical oxidation process.
7. Explain the relationship of process time, pressure, and temperature on the thickness of a thermally grown silicon dioxide layer.
8. Describe the principles and uses of rapid thermal, high-pressure, and anodic oxidation.

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Silicon Dioxide Layer Uses

Of all the advantages of silicon for the formation of semiconductor devices, the ease of growing a silicon dioxide layer is perhaps the most useful. Whenever a silicon surface is exposed to oxygen, it is converted to silicon dioxide (Fig. 7.1). Silicon dioxide is composed of one silicon atom and two oxygen atoms (SiO_2). We encounter silicon dioxide daily. It is the chemical composition of ordinary window glass. It's semiconductor version, however, is purer and formed in a specific way. Silicon dioxide layers are formed on bare silicon surfaces at elevated temperatures in the presence of an oxidant. The process is called *thermal oxidation.*

Although silicon is a semiconducting material, silicon dioxide is a dielectric material. This combination, a dielectric layer formed on a semiconductor, along with other properties of silicon dioxide, makes it one of the most commonly used layers in silicon devices. Silicon dioxide layers find use in devices to pacify the silicon surface, to act as doping barriers and surface dielectrics, and to serve as dielectric parts of device structures.

Surface passivation

In Chapter 4, the extreme sensitivity of semiconductor devices to contamination was examined. While a major focus of a semiconductor facility is the control and elimination of contamination, the techniques are not always 100 percent effective. Silicon dioxide layers play an important role in protecting semiconductor devices from contamination.

Silicon dioxide performs this role in two ways. First is the physical protection of the surface and underlying devices. Silicon dioxide layers formed on the surface are very dense (nonporous) and very hard. Thus, a silicon dioxide layer (Fig. 7.1) acts as a contamination barrier by physically preventing dirt in the processing environment from getting to the sensitive wafer surface. The hardness of the layer protects the wafer surface from scratches and abuse endured by the wafer in the fabrication processes.

The second way silicon dioxide protects devices is chemical in nature. Regardless of the cleanliness of the processing environment, some electrically active contaminants (mobile ionic contaminants) end up in or on the wafer surface. During the oxidation process, the top layer of silicon is converted to silicon dioxide. Contaminants on the

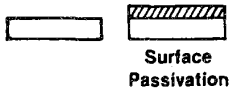


Figure 7.1 Surface passivation with silicon dioxide layers.

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surface end up in the new layer of oxide, away from the electrically active surface. Other contaminants are drawn up into the silicon dioxide film where they are less harmful to the devices. In the early days of MOS device processing, it was common to oxidize the wafers and then remove the oxide before further processing to rid the surface of unwanted mobile ionic contamination.

Doping barrier

In Chapter 5, doping was identified as one of the four basic fabrication operations. Doping requires creating holes in a surface layer through which specific dopants are introduced into the exposed wafer surface through diffusion or ion implantation. In silicon technology, the surface layer is most often silicon dioxide (Fig. 7.2). The silicon dioxide left on the wafer acts to block the dopant from reaching the silicon surface. All of the dopants used in silicon technology have a very slow rate of movement in silicon dioxide as compared to silicon. While the dopants penetrate to the required depth in the exposed silicon, they penetrate only a short distance into the silicon dioxide surface. It takes only a relatively thin silicon dioxide layer to block the dopants from reaching the silicon surface.

Another factor favoring the use of silicon dioxide is a coefficient of thermal expansion similar to that of silicon. In the high-temperature processes of oxidation, diffusion doping, and others, the wafer expands and contracts as it is heated and cooled. The silicon dioxide expands and contracts at close to the same rate as silicon, which means that the wafer will not warp during the heating and cooling.

Surface dielectric

Silicon dioxide is classified as a dielectric. This means that, under normal circumstances, it does not conduct electricity. When dielectrics are used in electrical circuits or devices, they are referred to as *insulators*. Acting as an insulator is an important role of silicon dioxide layers. Figure 7.3 shows a cross section of a wafer with a conductive layer of metal on top of a layer of silicon dioxide. The oxide prevents shorting of the metal layer to the underlying metal just as the insulation on an

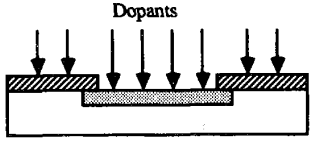


Figure 7.2 Silicon dioxide layer as dopant barrier.

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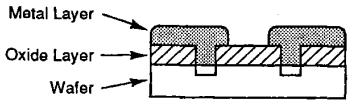


Figure 7.3 Oxide layer used as dielectric layer between wafer and metal.

electric cord prevents the wires from shorting. In this capacity, the oxide must be continuous; that is, have no holes or voids.

The oxide must also be thick enough to prevent a phenomenon known as *induction*. Induction can occur when the separating layer of oxide is thin enough to allow an electrical charge in a metal layer to cause a buildup of charge in the wafer surface. The surface charge can cause shorting and other unwanted electrical effects. A thick enough layer will prevent an induced charge in the wafer surface. Most of the wafer surface is covered with an oxide layer thick enough to prevent induction from the metal layers. This is called the *field oxide*.

Device dielectric

At the other end of the induction phenomenon is MOS technology. In an MOS transistor, a thin layer of silicon dioxide is grown in the gate region (Fig. 7.4). The oxide functions as a dielectric whose thickness is chosen *specifically* to allow induction of a charge in the gate region under the oxide. The gate is the part that controls the flow of current through the device (see Chapter 16). The dominance of MOS technology for ultra-large-scale integrated (ULSI) circuits has made the formation of gate regions a prime focus of process development and concern. Thermally grown oxides are also used as the dielectric layer in *capacitors* formed between the silicon wafer and a surface conduction layer (Fig. 7.5).

Silicon dioxide dielectric layers are also used in structures with two or more metallization layers. In this application, the silicon dioxide layers are deposited with *chemical vapor deposition* (CVD) techniques rather than thermal oxidation (see Chapter 12).



Figure 7.4 Silicon dioxide as field oxide and in MOS gate.

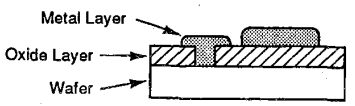


Figure 7.5 Silicon dioxide layer in solid-state capacitor.

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Device oxide thicknesses

The silicon dioxide layers used in silicon-based devices vary in thickness. At the thin end of the scale are advanced MOS gate oxides, in the 35 to 80 A range.[1] At the thick end are field oxides. Figure 7.6 lists the thickness ranges for the major uses.

Thermal Oxidation Mechanisms

Thermal oxide growth is a simple chemical reaction as shown in Fig. 7.7. This reaction takes place even at room temperature. However, an elevated temperature is required to achieve quality oxides in reasonable process times for practical use in circuits and devices. Oxidation temperatures are between 900 and 1200°C.

Although the formula shows the reaction of silicon with oxygen, it does not illustrate the growth mechanism of the oxide. To understand the growth mechanism, consider a wafer placed in a heated chamber and exposed to oxygen gas (Fig. 7.8*a*). Initially, the oxygen atoms combine readily with the silicon atoms. This stage is called *linear* because the oxide grows in equal amounts for each unit of time (Fig. 7.8*b*). After approximately 1000 angstroms (Å) of oxide is grown, a limit is imposed on the linear growth rate. [An angstrom is one ten-thousandth of a micron (μm); in other words there are 10,000 Å in 1 μm.]

For the oxide layer to keep growing, the oxygen and silicon atoms must come in contact. However the initially grown layer of silicon dioxide separates the oxygen in the chamber from the silicon atoms of the wafer surface. For oxide growth to continue, either the silicon in the wafer must migrate through the all-ready grown oxide layer to the oxygen in the vapor, or the oxygen must migrate to the wafer surface. In the thermal growth of silicon dioxide, the oxygen migrates (the techni-

Silicon Dioxide Thickness, Å	Application
60–100	Tunneling Gates
150–500	Gate Oxides, Capacitor Dielectrics
200–500	LOCOS Pad Oxide
2,000–5,000	Masking Oxides, Surface Passivation
3,000–10,000	Field Oxides

Figure 7.6 Silicon dioxide thickness chart.

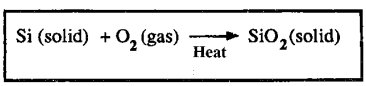


Figure 7.7 Reaction of silicon and oxygen to form silicon dioxide.

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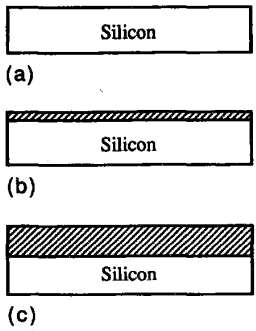


Figure 7.8 Silicon dioxide growth states. (*a*) Initial, (*b*) linear, and (*c*) parabolic.

cal term is *diffuses*) through the existing oxide layer to the silicon wafer surface. Thus, the layer of silicon dioxide consumes silicon atoms from the wafer surface—the oxide layer grows *into* the silicon surface.

With each succeeding new growth layer, the diffusing oxygen must move farther to reach the wafer. The effect is a slowing of the oxide growth *rate* with time. This stage of oxidation is called the *parabolic* stage. When graphed, the mathematical relationship of the oxide thickness, growth rate, and time takes the shape of a parabola. Other terms used for this second stage of growth is a *transport-limited reaction* or *diffusion limited reaction,* which means that the growth rate is limited by the transportation or diffusion of the oxygen through the oxide layer already grown. The linear and parabolic stages of growth are illustrated in Fig. 7.9. The formula in Fig. 7.10 expresses the fundamental parabolic relationship for oxide layers above approximately 1200 Å.

Thus, a growing oxide goes through two stages: the linear stage and the parabolic stage. The change from linear to parabolic is dependent on the oxidizing temperature and other factors (see the following section, "Influences on the oxidation rate"). In general oxides less than 1000 Å (0.1 μm) are controlled by the linear mechanism. This is the range of most MOS gate oxides.[2]

$X = B/A\ t$
Linear oxidation of silicon

$X = \sqrt{B\ t}$
Parabolic oxidation of silicon

X = oxide thickness
B = parabolic rate constant
B/A = linear rate constant
t = oxidation time

Figure 7.9 Linear and parabolic growth of silicon dioxide.

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$$R = \frac{X^2}{t}$$

where R = silicon dioxide growth rate
X = oxide thickness
t = oxidation time

Figure 7.10 Parabolic relationship of SiO_2 growth parameters.

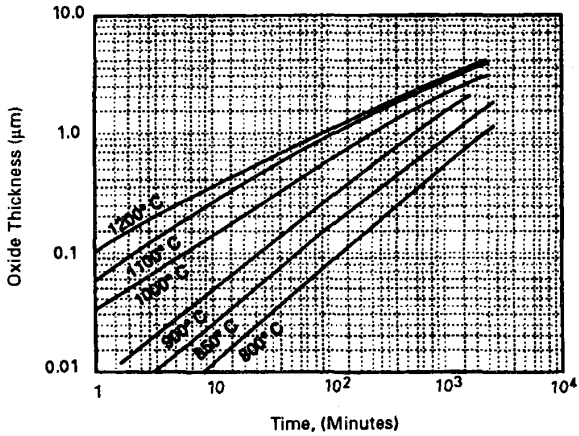
The major implication of this parabolic relationship is that thicker oxides require much more time to grow than thinner oxides. For example, growth of a 2000-Å (0.20-μm) film at 1200°C in dry oxygen requires 6 min (Fig. 7.11).[3] To double the oxide thickness to 4000 Å requires some 220 min—over 36 times as long. This longer oxidation time presents a problem for semiconductor processing. When pure dry oxygen is used as the oxidizing gas, the growth of thick oxide layers requires even longer oxidation times, especially at the lower temperatures. Generally, process engineers want to have the shortest process times possible as is consistent with quality control. The 220 min in the example given is excessive, i.e., only one oxidation would be possible in one shift of operation.

One way to achieve faster oxidations is to use water vapor (H_2O) instead of oxygen as the oxidizing gas (oxidant). The growth of silicon dioxide in water vapor proceeds by the reaction shown in Fig. 7.12. In the vapor state, the water is in the form $H–OH^-$. It is composed of one atom of hydrogen (H) and a molecule of oxygen and hydrogen with a negative charge (OH^-). This molecule is called the *hydroxyl ion.* The hydroxyl ion diffuses through the oxide layers already on the wafer faster than oxygen. The net effect is a faster oxidation of the silicon, as shown in the growth curves in Fig. 7.11.

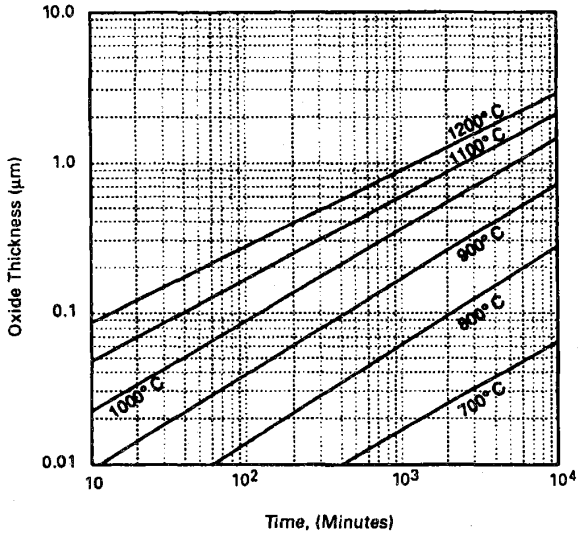
Water vapor at the oxidation temperatures is in the form of steam, and the process is called either *steam oxidation, wet oxidation,* or *pyrogenic steam.* The term *wet oxidation* comes from the time when liquid water was the primary water vapor source. An oxygen-only oxidation process is called *dry oxidation.* If oxygen only is used, it must be free of any water vapor (dry) or the oxide growth would be that of water vapor.

Notice in the reaction of water vapor and silicon that there are two hydrogen molecules ($2H_2$) on the right side of the equation. Initially, these hydrogen molecules are trapped in the solid silicon dioxide layer, making the layer less dense than an oxide grown in dry oxygen. However, after a heating of the oxide in an inert atmosphere, such as nitrogen (see "Oxidation Processes," p. 191), the two oxides become similar in structure and properties.

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(a)



(b)

Figure 7.11 Silicon dioxide thickness versus time and temperature in (*a*) dry oxygen and (*b*) steam.

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$$Si\ (solid) + H_2O\ (gas) \xrightarrow[Heat]{} SiO_2(solid) + 2H_2\ (gas)\uparrow$$

Figure 7.12 Reaction of silicon and water vapor to form silicon dioxide and hydrogen gas.

Influences on the oxidation rate

The original oxide thickness vs. time curves were determined on ⟨111⟩-oriented, undoped wafers.[4] MOS devices are fabricated in ⟨100⟩-oriented wafers and wafers surfaces are doped. Both of these factors influence the oxidation rate for a particular temperature and oxidant environment. Other factors influencing the oxidation growth are impurities intentionally included in the oxide (such as HCl) and oxidation of polysilicon layers.

Wafer orientation. The orientation of the wafer has an effect on the oxidation growth rate. ⟨111⟩ planes have more silicon atoms than ⟨100⟩ planes. The larger number of atoms allows for a faster oxide growth on ⟨111⟩-oriented wafers than for ⟨100⟩-oriented wafers. Figure 7.13 shows the growth rates for the two orientations in steam. This difference is seen more in the linear growth stage and at lower temperatures.

Wafer dopant redistribution. The silicon surface being oxidized always has dopants. A production silicon wafer starts into the line doped as

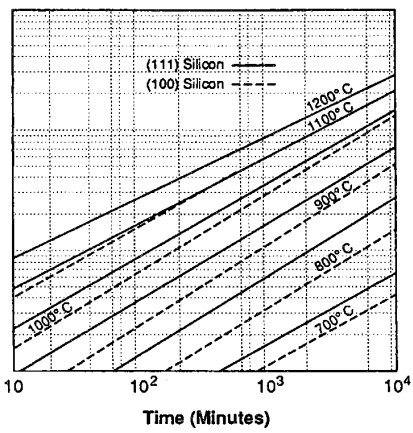


Figure 7.13 Oxidation of ⟨111⟩ and ⟨111⟩ silicon in steam.

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either an N-type or P-type. Later on in the process, wafers have dopant(s) in the surface from diffusion or ion implant operations. The dopant elements used and their concentration both have effects on the oxidation growth rate. For example, oxides grown over a highly doped phosphorus layer are less dense than those grown over the other silicon dopants. These phosphorus-doped oxides also etch faster and present an etching challenge in the patterning operation due to resist lifting and rapid undercutting.

Another effect on oxidation growth rate is the distribution of the dopant atoms in the silicon after the oxidation is completed.[5] Recall that during thermal oxidation, the oxide layer grows *down* into the wafer. A question is "What happens to the dopant atoms that were in the layer of silicon converted to silicon dioxide?" The answer depends on the conductivity type of the dopant. The N-type dopants of phosphorus, arsenic, and antimony have a higher solubility in silicon than in silicon dioxide. When the advancing oxide layer reaches them, they move down into the wafer. The silicon silicon-dioxide interface acts like a snowplow pushing ahead an ever-greater pile of snow. The effect is that there is a higher concentration (called *pile-up*) of N-type dopants at the silicon dioxide-silicon interface than was originally in the wafer.

When the dopant is the P-type boron, the opposite effect happens. The boron is drawn up into the silicon dioxide layer, causing the silicon at the interface to be depleted of the original boron atoms. Both of these effects, pile-up and depletion, have significant impact on electrical performance of devices. The exact effects of pile-up and depletion on the dopant concentration profile are illustrated in Chapter 17.

Doping concentration effects on the oxidation rate vary with the dopant type and concentration level. In general, higher doped regions oxidize faster than more lightly doped regions. Heavily doped phosphorus regions can oxidize 2 to 5 times the undoped oxidation rate.6

However doping-induced oxidation effects are more pronounced in the linear stage (thin oxides) of oxidation.

Oxide impurities. Certain impurities, particularly chlorine from hydrochloric acid (HCl), are included in the oxidizing atmosphere for inclusion in the growing oxide (see "Oxidation Processes," p. 191). These impurities have an influence on the growth rate. In the case of HCl, the growth rate can increase from 1 to 5 percent.[7]

Oxidation of polysilicon. Polysilicon conductors and gates are a feature of most MOS devices/circuits. The device/circuit processes require oxidation of the polysilicon. Compared to the oxidation of single-crystal silicon, polysilicon can be faster, lower, or similar. A number of fac-

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tors related to the formation of the polysilicon structure influence a subsequent oxidation. They are the polysilicon deposition method, deposition temperature, deposition pressure, the type and concentration of doping, and the grain structure of the polysilicon.[8]

Differential oxidation rates and oxide steps. After the initial oxidation step in a device/circuit fabrication process, the wafer surface has a variety of conditions. Some areas have the field oxide, some are doped, and some are polysilicon regions, and so on. Each of these areas has a different oxidation rate and will increase in oxide thickness depending on the condition. This oxidation thickness difference is called *differential oxidation.* For example, an oxidation of a MOS wafer after a polysilicon gate has been formed next to lightly doped source/drain areas (Fig. 7.14*a*) results in a thicker oxide growth on gate because silicon dioxide grows faster on polysilicon.

Differential oxidation rates cause the formation of steps in the wafer surface (Fig. 7.14*b*). Illustrated is a step created by the oxidation of an exposed area next to a relatively thick field oxide. The oxide will grow faster in the exposed area, since additional oxide growth in the field oxide is limited by the parabolic rate limitation. In the exposed area, the faster growing oxide will use up more silicon than under the field oxide. The step is shown in Fig. 7.14*b*.

Thermal Oxidation Methods

The oxide formation reaction formulas include a triangle under the reaction direction arrows. These triangles indicate that the reaction requires energy to proceed. In silicon technology, that energy is usually supplied by heating the wafers and is called *thermal oxidation.* Silicon

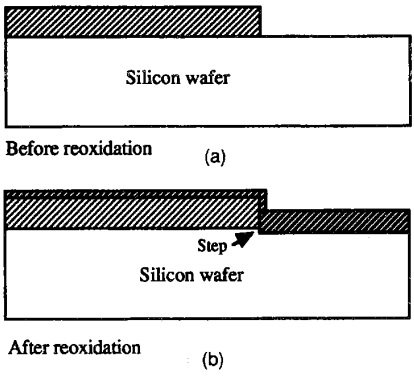


Figure 7.14 Differential oxidation of silicon.

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dioxide layers are grown either at atmospheric pressure or at high pressure. An atmospheric pressure oxidation takes place in a system without intentional pressure control—the pressure is simply that of the atmosphere for the location. There are two atmospheric techniques: tube furnaces and rapid thermal systems (Fig. 7.15).

Horizontal Tube Furnaces

Horizontal tube furnaces have been used in the industry since the early 1960s for oxidation, diffusion, heat treating, and various deposition processes. They were first developed for diffusion processes in germanium technology and to this day are often called simply *diffusion furnaces.* The more correct, generic, term is a *tube furnace.* Horizontal designs evolved into vertical designs with a number of advantages detailed in a following section. The basic tube furnace principles apply to both systems.

A cross section of a basic single horizontal three-zone tube furnace is shown in Fig. 7.16. It consists of a long ceramic tube made of mullite (a ceramic), with coils of copper tubing on the inside surface. Each of the coiled tubes defines a zone and is connected to a separate power supply operated by a proportional band controller. Furnaces may have up to seven separate zones. Inside the furnace tube is a quartz reaction tube that serves as the reaction chamber for the oxidation (or other processes). The reaction tube may itself be inside a ceramic liner called a *muffle.* The muffle acts as a heat sink fostering a more even heat distribution along the quartz tube.

Thermocouples are positioned against the quartz tube and send temperature information to the proportional band controllers. The controllers proportion power to the coils, which in turn heat the reac-

Thermal Oxidation		
• Atmospheric Pressure	Tube furnace	Dry Oxygen Wet Oxygen Bubbler Flash System Dry Oxidation
	Rapid Thermal	Dry Oxygen
• High Pressure	Tube Furnace	Dry or Wet Oxygen
Chemical Oxidation		
• Anodic Oxidation	Electrolytic Cell	Chemical

Figure 7.15 Oxidation methods.

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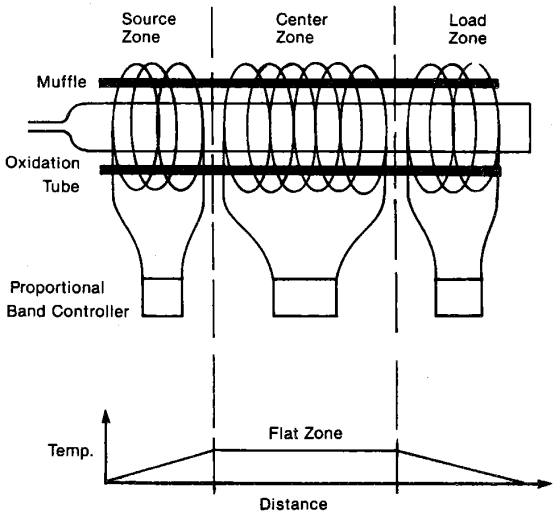


Figure 7.16 Cross section of single horizontal tube furnace with three heating zones.

tion tube by radiation and conduction. Radiation heating comes from the energy given off by the coils and impinging on the tube. Conduction takes place where the coils touch the tube. These controllers are very sophisticated and can control temperatures in the center zone (flat zone) to ±0.5°. For a process that operates at 1000°C, this variation is only ±0.05 percent. For the oxidation, the wafers are placed on a holder and positioned in the flat zone. The oxidant gas is passed into the tube, where the oxidation takes place. The details and the options used in actual practice are discussed in the following sections.

A production tube furnace is an integrated system of seven various sections (Fig. 7.17):

1. Reaction chamber(s)
2. Temperature control system
3. Furnace section
4. Source cabinet
5. Wafer cleaning station
6. Wafer load station
7. Process automation

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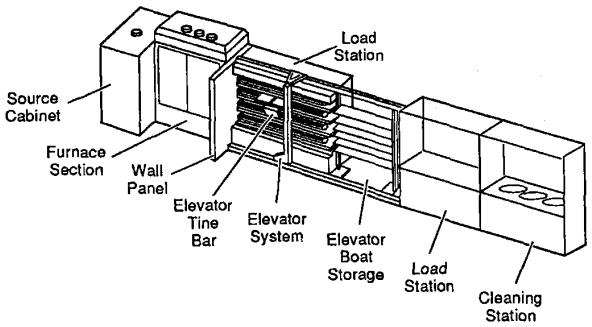


Figure 7.17 Tube furnace.

Reaction chamber

The basic tube furnace operation was previously described. An important part of the system is the reaction chamber. This part protects the wafers from outside contamination and serves as a heat sink to even out the temperature inside the tube. Tube furnace reaction tubes are round, with a gas inlet end and a wafer load end. The gas inlet end, also known as the source end, tapers down to a ground fitting to provide a leak-free connection to the gas sources. The load end also has a ground fitting to receive either an end cap that keeps dirt out of the furnace or a wafer transfer unit (see sections on "Automatic wafer loading," p. 188, and "Manual wafer loading," p. 189).

The traditional reaction chamber material is high-purity quartz. Quartz is a highly purified glass favored for its inherent stability at high temperatures and its basic cleanliness. Drawbacks to quartz are its fragility and the presence of some metallic ions. Quartz also allows sodium ions from the heating coils to pass into the reaction chamber.

Another drawback is the tendency of quartz to break up and sag at temperatures above 1200°C. The breakup is called *devitrification* and results in small flakes of the quartz tube surface falling onto the wafers. Sagging impedes the easy placement of the wafer holders in and out of the tube. Quartz tubes are manufactured by two methods: electric fusion and flame fusion. As the names imply, two different heat sources are used to fuse the quartz. Both materials have about the same levels of trace metals but, in one evaluation, flame-fused tubes produced devices with better characteristics.[9]

Quartz tubes require periodic cleaning. One method is to place them in a tank of hydrofluoric (HF) acid or a solution of HF and water. This cleaning process takes place outside of the fabrication area, necessi-

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tating the removal and cooling of the tube. The cooling and heating hasten the devitrification process. The HF cleans by removing a thin layer of the quartz. This continual etching eventually weakens the tube wall, thus limiting its lifetime.

Some firms do an *in situ* tube cleaning with a portable plasma generator. The plasma generator is positioned inside the tube, where it activates etching gases passed into the tube. Both nitrogen trifluoride (NH_3) and the gases etch away contaminants. A second *in situ* cleaning method uses etching gases in the tube, which are activated by a plasma field created in the tube. This type of cleaning is more applicable to tube furnaces used for chemical vapor deposition (CVD) processes where the buildup of reaction-created particles is greater than in oxidation processes.

An alternative material to quartz process tubes and wafer holders is silicon carbide. Silicon carbide is structurally stronger and does not break down with repeated heating and cooling. This resistance to temperature cycling also makes the material a better metallic ion barrier over a longer period of time. During processes where oxygen is in the tube, the inside surface grows a thin layer of silicon dioxide. When this oxide is removed in HF, there is no attack of the tube material, which also contributes to the extended lifetime. The widespread use of silicon carbide tubes and wafer holders has been slowed by their high cost and weight.

Temperature control system

The temperature control system connects thermocouples touching the reaction tube to proportional band controllers that feed the power to the heating coils. Proportional band controllers maintain even temperatures in the tube by feeding in or turning off the current to the coils in proportion to the deviation of the tube temperature from the set point. The closer the tube is to the set-point temperature, the smaller the amount of power that is fed to the coils. This system allows fast recovery of the tube to a cold load without overshoot. Adjustments are made to the controllers until the desired temperatures in the processing section of the tube (flat zone) are achieved.

Overshoot is the raising of the tube temperature too high above the desired process temperature as a result of applying too much power to the coils (Fig. 7.18).

Advanced systems have thermocouples positioned against the outside of the tube wall. These feed a microprocessor that, in turn, gives the information to the controllers. This system is called *autoprofiling*.[10] Good process control requires that the temperature profile inside the furnace be checked periodically with thermocouples

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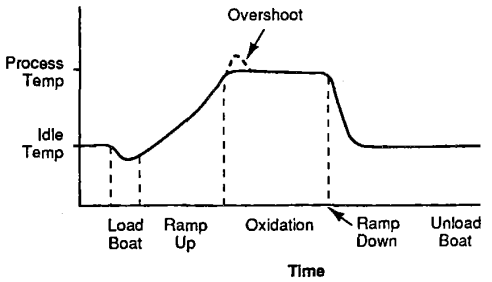


Figure 7.18 Temperature levels during oxidation.

inserted in the tube and the temperature measured by independent recorders.

The processing of larger-diameter wafers has brought with it the concern of wafer warping (Fig. 7.19). Silicon expands faster than silicon dioxide. When heated, the silicon dioxide pulls the wafer combination into a concave shape. Wafers that are heated or cooled rapidly will warp to the point of being useless. The degree of warping increases with higher process temperatures, that is, those above 1150°C.

Two methods are employed to minimize warping of wafers in tube furnaces. One is called *ramping* (or temperature ramping). Ramping is the procedure of maintaining the furnace at a temperature several hundred degrees below the process temperature. The wafers are slowly inserted into the furnace at this lower temperature and, after a short stabilization period, the controllers automatically take the furnace up to the process temperature. At the end of the process cycles, the furnace is cooled to the lower temperature before the wafers are removed. During the ramping process, the controllers must maintain the temperature control in the flat zone.

Tube furnaces are maintained at close to the process temperature 24 hours a day due to the devitrification of quartzware and the length of time it takes to stabilize the flat zone. In the interest of economy, some fabrication areas will keep the furnaces at the lower temperature. This is called an *idle* condition.

The second anti-warping procedure is the slow loading of the wafer boat into the tube. At loading rates of about 1 in/min, warping is mini-

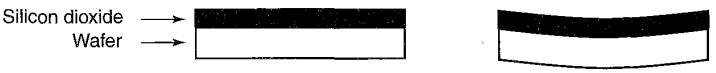


Figure 7.19 Wafer warping.

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mized. For large-diameter wafers and large batch sizes, both methods are used.

Another requirement of the heating system is a fast recovery time after the wafers are loaded in the tube. A full load of wafers can drop the tube temperature as much as 50°C or more.[11] The heating system works to bring the flat zone to temperature as fast as possible without introducing warping conditions or over shoot. Figure 7.18 illustrates a typical temperature-time recovery curve for a five-zone tube furnace.

Furnace section

A production-level tube furnace will contain three or four tubes (reaction chambers) and a separate temperature control system for each of the tubes. The tubes are arranged vertically above each other in a stack. The tubes open into an exhaust chamber that draws away the spent and heated gases as they exit the tube. This section of the furnace is called a *scavenger.* The scavenger is connected to the facility's exhaust system, which contains a scrubber to remove toxic gases from the withdrawn gases.

The tubes within a bank may be all used for the same purpose, such as oxidations, or be designated for different operations, such as oxidation, diffusion, alloy, or CVD, depending on the process requirements and the volume of wafers being processed. To change the use requires a change of tubeware and contamination monitoring to ensure that contaminants from a previous use are not present in the individual tube section.

Source cabinet

Each tube requires a number of gases to accomplish the desired chemical reaction. In the case of oxidation, the gas oxidants of oxygen or water vapor have been detailed. In addition, almost every tube process has nitrogen-flow capability. The nitrogen is used during the loading and unloading stage of the process to prevent accidental oxidation. In the idle condition, nitrogen is kept constantly flowing through the tube. The flow serves to keep dirt out of the system and maintain the pre-established flat zone.

Each of the tube processes requires that the gases be delivered to the tube in a specified sequence, at a specified pressure, at a specific flow rate, and for a specific time. The equipment used to regulate the gases is located in a cabinet attached to the furnace section of the system and is known as the *source cabinet.* There is a separate unit, called a *gas control panel* or *gas flow controller,* connected to each tube. The panel consists of solenoids, pressure gauges, mass flow controllers

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or flow meters, filters, and timers. In its simplest version, the gas flow controller consists of manually operated valves and timers. In production systems, the sequencing and timing of the various gases into the tube is controlled by a microprocessor. Required gases are plumbed to the panel. During operation, a timer opens a solenoid to admit the required gas to the panel. Its pressure is controlled by a pressure gauge. Flow amount into the tube is controlled by a flow meter or mass flow controller.

A *mass flow meter* is preferred in place of a flow meter for its inherent superior control. Stoichiometric considerations require that the same amount of material, as measured by its mass, be delivered into the reaction chamber. Standard flow meters measure the volume of material, and equal volumes of the same material may contain different amounts of material due to pressure and temperature differences. Semiconductor processes use a thermal-type of mass flow meter. The system consists of a heated gas passage tube with two temperature sensors. When no gas is flowing, the temperature sensors are at the same temperature. With the introduction of a gas flow, the downstream sensor reads higher. The difference between the two sensors is related to the amount of heat mass (not volume) that has moved downstream. The meter has a feedback mechanism to control the gas flow such that a steady amount of material flows through the meter. The source section also contains the microprocessor-controlled valves that meter the gas into the reaction chamber in the right sequence for the right amount of time. A general schematic of a mass flow meter is shown in Fig. 7.20. Mass flow meters can be set for a specific amount and on-board sensors measure and control the output with a feedback control system.[12] The piping material used in gas flow controllers is stainless steel to maintain high levels of cleanliness and to minimize chemical reactions between the gas and tube material.

Often, the gas flow controller is called a *jungle*. This term came about when the gas controllers were built in-house and had the look of a "jungle" of tubing and valves. Gases are supplied to the gas flow controller through piping from the liquid gas supplies in the pad section of the facility, or by smaller lecture bottles of gas located at the process tool.

Some processes require a chemical that is difficult to deliver in gas form. In this situation, a bubbler and liquid source is used. A bubbler consists of a quartz vial designed to admit a gas into the liquid. As the gas bubbles through the liquid and mixes with the source vapors in the top of the bubbler, it picks up the source chemicals and carriers them into the tube. Bubblers are used in oxidation, diffusion, and CVD processes. An oxidation bubbler is shown in Fig. 7.21. Diffusion and CVD bubblers generally have a cylindrical shape.

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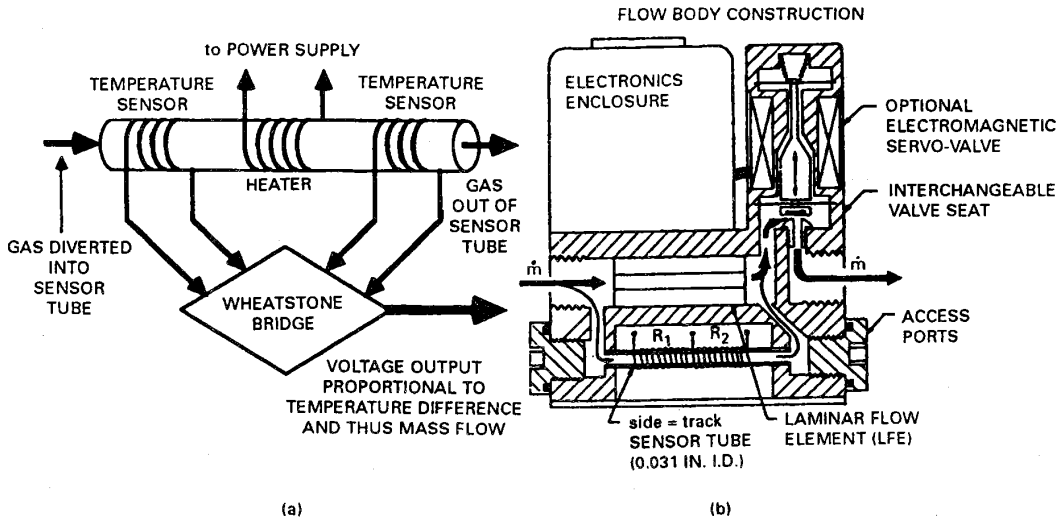


Figure 7.20 (*a*) Operating principle of a mass flow meter and (*b*) cutaway.

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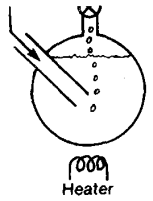


Figure 7.21 Bubbler water vapor source.

Vertical Tube Furnaces

Horizontal tube furnaces have enjoyed great popularity over the years. A lot of process development has taken place in the 40 years of their use. However, the need for greater contamination control and the move to ever increasing wafer diameters as well as the need for more productive processing has pushed horizontal tube furnaces to a limit.

While contamination control has led to the development of cantilever systems, they have had to get larger and stronger as the wafers have grown in diameter and weight. Also, the larger wafer diameters require larger tube diameters, which puts additional pressures on the maintenance of extended temperature flat zones. Few firms are reporting the use of horizontal tube furnaces for 200-mm and larger wafers.[14]

The larger wafer loads have caused a lengthening of the furnaces and their associated load stations. In cleanroom terms, the "footprint" of the equipment is increasing. The problem is that larger footprints require larger and more expensive cleanrooms.

There are also process problems associated with larger-diameter horizontal tubes. One is keeping the gas streams in a laminar flow pattern in the tube. *Laminar gas flow* is uniform with no separation of the gases into layers and without turbulence that causes uneven reactions within the tube.

These considerations have resulted in the development of vertical tube furnaces, which are the configuration of choice for high-production, large-diameter processes.[15] In this configuration, the tube is held in a vertical position (Fig. 7.22) with loading taking place from the top or bottom. Tube materials and heating systems are the same as for horizontal systems.

The wafers are loaded in standard cassettes and lowered or raised into the flat zone. This action is accomplished without the particulates generated by the cassettes scraping the sides of the tubes. In this configuration, the wafers are in the most dense loading for a tube furnace. An added plus for vertical tube furnaces is the ease of rotating the wafers in the tube, which produces a more uniform temperature across

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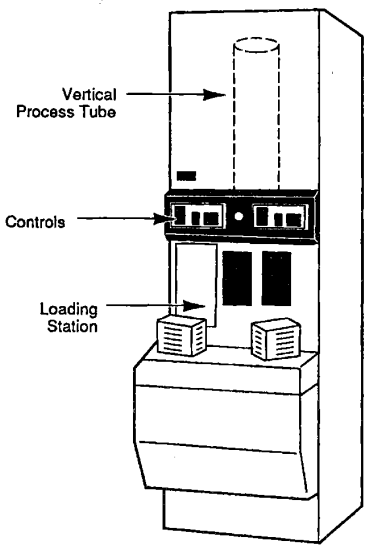


Figure 7.22 Vertical tube furnace.

the wafer. These furnaces have the same subsystems as horizontal furnaces.

Process uniformity is also enhanced by a more uniform (laminar) gas flow in a vertical tube. In a horizontal system, gravity tends to separate mixed gases as they flow down the tube. In a vertical system, the gas moves parallel to gravity minimizing the gas separation problem and the boat rotation minimizes gas turbulence. Vertical furnaces are capable of producing process variations 60 percent of those in horizontal furnaces.[16]

Particle generation associated with boat scrapping in horizontal systems is virtually eliminated in vertical systems, and the smaller area required for loading results in a cleaner system. Particle densities can reach into the $0.01/cm^2$ range.[17]

Perhaps one of the most appealing cost aspects of vertical tube furnaces is the small footprint. The system is smaller than a conventional four-stack system. Vertical systems offer the possibility of locating the furnaces outside the cleanroom with only a load station door opening into the cleanroom. In this arrangement, the cleanroom footprint of the furnace is practically zero, and maintenance can take place from the service chase. Another possible arrangement of vertical furnaces is in an island/cluster configuration. The furnaces are arranged around a central robot that alternately load several furnaces. A simpler design translates into a more reliable furnace with lower maintenance costs

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and longer periods of up-time. Vertical furnaces can be configured to perform any of the oxidation, diffusion, annealing, and deposition processes required in wafer fabrication.

Fast Ramp Furnaces

As wafer sizes (and mass) become larger, ramp-up and ramp-down times become longer, creating more cost and bottlenecks in the fab flow. One way to offset the time increase is make sure that the batch sizes are maximized. But this can slow up the flow if the furnace is sitting idle waiting for enough wafers to form a large batch. Into this breech has come the fast-ramp, low-batch furnaces. They are mini-horizontal furnaces with high-powered heating systems. Where conventional tube systems operate at a few degrees per minute of ramping, fast-ramp furnaces can achieve rates of tens of degrees per minute.[18] Their lower capacity can be offset by the faster process times.

Rapid Thermal Processing (RTP)

Ion implantation has replaced thermal diffusion due to its inherent doping control. However, ion implantation requires a follow-on heating operation, called *annealing,* to cure out crystal damage induced by the implant process. The annealing step has been traditionally done in a tube furnace. Although the heating anneals out the crystal damage, it also causes the dopant atoms to spread out in the wafer, an undesirable result. This problem led to the investigation of alternate energy sources to achieve the annealing without the spreading of the dopants. The investigations led to the development of rapid thermal process (RTP) technology.

RTP technology is based on the principle of radiation heating (Fig. 7.23). The wafer is automatically placed in a chamber fitted with gas inlets and exhaust outlets. Inside a heat source above (and possibly below), the wafer provides the rapid heating. Heat sources include graphite heaters, microwave, plasma arc, and tungsten halogen lamps.[19] Tungsten halogen lamps are the most popular.[20] The radiation from the heat source couples into the wafer surface and brings it up to the process temperature at rates of 75 to 125°C per second. The same temperature would take minutes to reach in a conventional tube furnace. A typical time-temperature cycle is shown in Fig. 7.24. Likewise, cooling takes place in seconds. With radiation heating, because of its very short heating times, the body of the wafer never comes up to temperature. For the ion implant annealing step, this means that the crystal damage is annealed while the implanted atoms stay in their original location.

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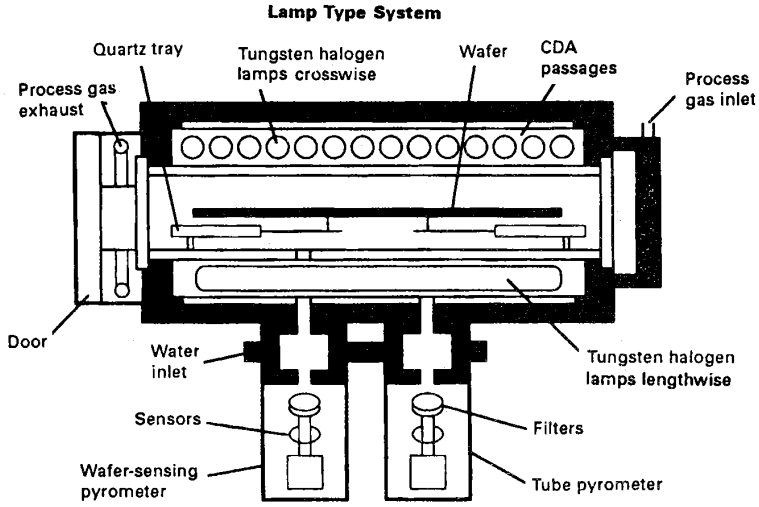


Figure 7.23 RTP design. *(Source:* Semiconductor International, *May 1993.)*

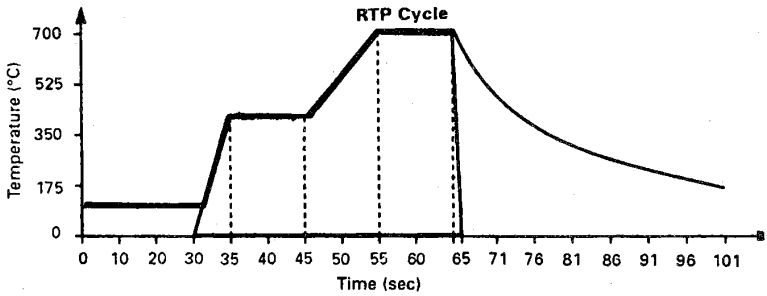


Figure 7.24 Example RTP time/temperature curve. *(Source:* Semiconductor International, *May 1993.)*

Use of RTP reduces the *thermal budget* required for a process. Every time a wafer is heated near diffusion temperatures, the doped regions in the wafer continue to spread down and sideways (see Chapter 11). Every time a wafer is heated and cooled, more crystal dislocations form (see Chapter 3). Thus, minimizing the total time a wafer is heated allows more dense designs and fewer failures from dislocations.

Another advantage is single-wafer processing. The move to larger-diameter wafers has introduced uniformity requirements that, in many processes, are best met in a single-wafer process tool.

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RTP technology is a natural choice for the growth of thin oxides used in MOS gates. The trend to smaller feature sizes on the wafer surface has brought along with it a decrease in the thickness of layers added to the wafer. Layers undergoing dramatic reduction in thickness are thermally grown gate oxides. Advanced production devices are requiring gate oxides less than 100 Å thick. Oxides this thin are sometimes hard to control in conventional tube furnaces due to the problem of quickly supplying and removing the oxygen from the system. RTP systems can offer the needed control by their ability to heat and cool the wafer temperature very rapidly. RTP systems used for oxidation, called *rapid thermal oxidation* (RTO) systems, are similar to the annealing systems but have an oxygen atmosphere instead of an inert gas. A typical time/temperature/thickness relationship for RTO is shown in Fig. 7.25.

Other processes using RTP technology include wet oxide (steam) growth, localized oxide growth, source/drain activation after ion implant, LPCVD polysilicon, amorphous silicon, tungsten, salicide contacts, LPCVD nitride, and LPCVD oxide.[21] RTP systems come in atmospheric, low-pressure, and ultra-high-vacuum designs.

Temperature control across a wafer is different in a radiation chamber as opposed to in a furnace tube. In an RTP system, the wafer never comes to thermal stability. The problem is particularly acute at the wafer edges. Another problem comes from the number and different layers already on an in-process wafer. These different layers each absorb the heating radiation in a different way, resulting in temperature differences across the wafer, which in turn contribute to temperature nonuniformity. This phenomenon is called *emissivity* and is a property of the particular material and the wavelength of the heating radiation. Temperature nonuniformity creates nonuniform process results in and on the wafer surface and, if the temperature differential is high enough, crystal slip at the wafer's edge.

Solutions to the problem include lamp placement and control of individual lamps in the system along with top and bottom lamps. Some systems have a heated annular ring to keep the edge of the wafer within the required temperature range. Process temperatures are usually measured by thermocouples; however, they require back contact with the heated wafer, which is impractical in a single-wafer system, and thermocouples have a response time that is longer than some RTP heating cycles. Optical pyrometers, which gauge temperatures by measuring characteristic energies given off by the heated object, are preferred. However, they too are prone to errors, especially on wafers with a number of layers. The difficulty is relating the emission given off by the wafer to the actual temperature on the surface. Solutions to this problem include a backside seal layer of silicon nitride to mini-

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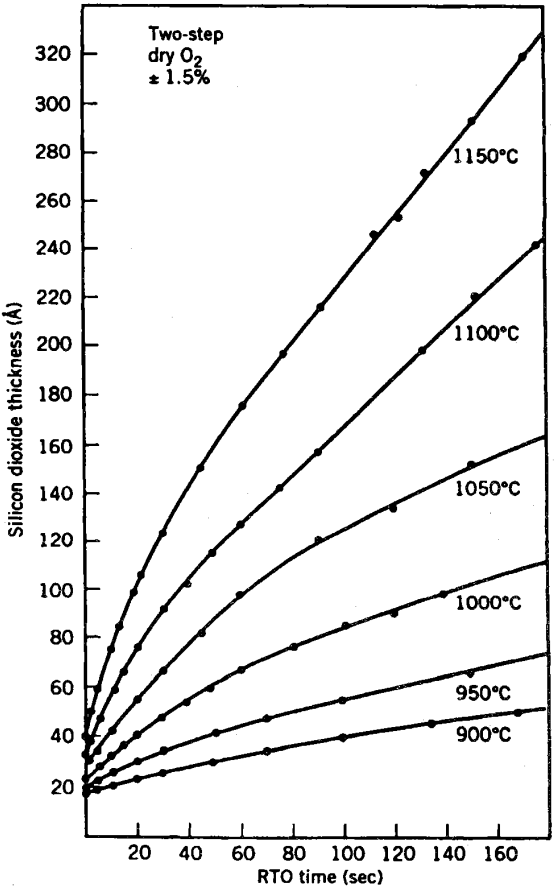


Figure 7.25 Oxidation of silicon by RTO. *(Source: Ghandhi,* VLSI Fabrication Principles.)

mize backside emissivity variations[22] and open-loop lamp control. *Open-loop control* is based on converting lamp control to direct current (dc) to get away from voltage variations to the lamps. Other approaches involve elaborate sampling of and/or filtering of the radiation coming off the wafer to more closely relate the measurement to the wafer surface temperature. It has also been suggested that measurement of the wafer expansion, which is directly due to temperature increases, may be a more reliable and direct measurement technique.[23]

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Given the benefits of RTP, especially in a high-production, single-wafer processing environment, it can be expected that the development will continue.

High-Pressure Oxidation

The thermal budget problem also was an impetus (along with others) for high-pressure oxidation. The growth of dislocations in the bulk of the wafer and the growth of hydrogen-induced dislocations along the edge of openings in layers on the wafer surface[24] are two high-temperature oxidation problems. In the first case, the dislocations cause various device performance problems. In the latter case, surface dislocations cause electrical leakage along the surface or the degradation of silicon layers grown on the wafer for bipolar circuits.

The growth of dislocations is a function of the temperature at which the wafer is processed and the time it spends at that temperature. A solution to this problem is to perform thermal oxidation processes at a lower temperature. This solution by itself causes the production problem of longer oxidation times. The solution that addresses both problems is high-pressure oxidation (Fig. 7.26). These systems are configured like conventional horizontal tube furnaces but with one major exception: the tube is sealed, and the oxidant is pumped into the tube at pressures of 10 to 25 atm (10 to 25 times the pressure of the atmosphere). The containment of the high pressure requires encasing the quartz tube in a stainless steel jacket to prevent it from cracking.

At these pressures, the oxidation proceeds at a faster rate than in atmospheric systems. A rule of thumb is that a 1-atm increase in pressure allows a 30°C drop in the temperature. In a high-pressure system, that increase relates to a drop of 300 to 750°C in temperature. This reduction is sufficient to minimize the growth of dislocations in and on the wafers.

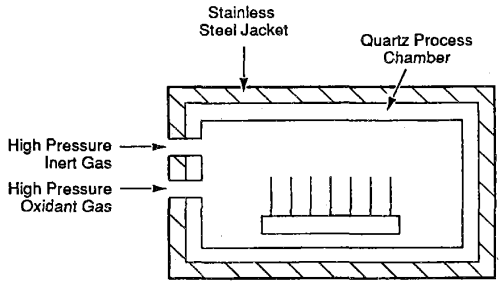


Figure 7.26 High-pressure oxidation.

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Another option using high-pressure systems is to maintain the regular process temperature and reduce the time of the oxidation. Other considerations concerning high-pressure systems focus on the safe operation of the system and possible contamination from the additional pumps and piping needed to create the high pressures inside the tube.

Very thin MOS gate oxide growth is a candidate for high-pressure oxidation. The thin oxide must have structural integrity (no holes, and so forth) and have a dielectric strength high enough to prevent charge induction in the gate region. Gate oxides grown in high-pressure processes have higher dielectric strength than similar oxides grown at atmospheric pressure.[25] High-pressure oxidation is also a solution for the *bird's beak* problem that occurs during local oxidation of silicon (LOCOS). See Chapter 16, "LOCOS process." An unwanted bird's beak of oxide grows into the active region of an MOS device as in Fig. 7.27. High-pressure oxidation can minimize the bird beak encroachment into the device area and minimize field oxide thinning during LOCOS processing.[26]

In addition to oxidation, high-pressure systems are finding some use in CVD epitaxial depositions and for flowing glass layers on the wafer surface.[27] Both of these processes are of higher quality when performed at lower temperatures.

Oxidant sources

Dry oxygen. When oxygen is used as the oxidant, it is supplied from the facility source or from tanks of compressed oxygen located in or near the source cabinet. It is imperative that the gas be dry, that is, not contaminated with water vapor. The presence of water vapor in the oxygen would increase the oxidation rate and cause the oxide layer to be out of specification. Dry oxygen oxidation is the preferred method for growing the very thin (≈1000 Å) gate oxides required for MOS devices.

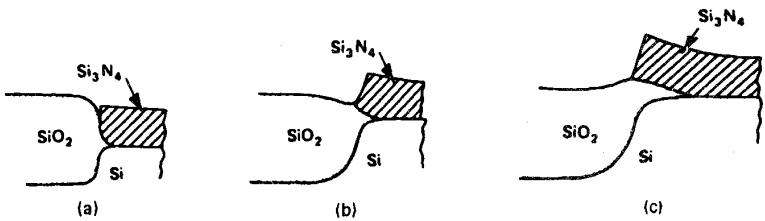


Figure 7.27 Bird's beak growth. (*a*) No pre-etch, (*b*) 1000 Å pre-etch, and (*c*) 2000 Å pre-etch. *(From Ghandhi,* VLSI Fabrication Principles.)

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Water vapor sources. Several methods are used to supply water vapor (steam) into the oxidation tube. The choice of method depends on the level of thickness and cleanliness control required of the oxide layer in the device.

Bubblers. The historic method of creating a steam vapor in the tube is by a bubbler (see "Source Cabinet"). For oxidation, the bubbler liquid is deionized (DI) water (refer back to Fig. 7.21) heated close to the boiling point (98 to 99°C), which creates a water vapor in the space above the liquid.

As the carrier gas is bubbled through the water and passes through the vapor, it becomes saturated with water. Under the influence of the elevated temperature inside the tube, the water vapor becomes steam and causes the oxidation of the silicon surfaces.

A primary drawback with a bubbler system is that control of the amount of water vapor entering the tube as the water level in the bubbler changes and fluctuations in the water temperature. With bubblers, there is always concern about contamination of the tube and oxide layer from dirty water or dirty flasks. This contamination potential is heightened by the need to open the system periodically to replenish the water.

Dry oxidation (dryox). Bubbler and flash new levels of thickness control and cleanliness came with the introduction of MOS devices. The heart of an MOS transistor is the gate structure, and the critical layer in the gate is a thin, thermally grown oxide. Liquid-water-steam systems are unreliable for growing thin, clean gate oxides. The answer was found in dry oxidation (or dry steam) process (Fig. 7.28).

In the dry oxidation system, gaseous oxygen and hydrogen are introduced directly into the oxidation tube. Inside the tube, the two gases mix and, under the influence of the high temperature, form steam. The result is a wet oxidation in steam. Dryox systems offer improved control and cleanliness over liquid systems. First, gases can be purchased in a very clean and dry state. Second, the amounts going into the tube can be very precisely controlled by the mass flow controllers. Dryox is the preferred general oxidation method for production for all advanced devices.

A drawback to dryox systems is the explosive property of hydrogen. At oxidation temperatures, hydrogen is very explosive. Precautions

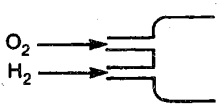


Figure 7.28 "Dryox" (dry steam) water vapor source.

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used to reduce the explosion potential include separate oxygen and hydrogen lines to the tube and flowing excess oxygen into the tube. The excess oxygen ensures that every hydrogen molecule (H_2) will combine with an oxygen atom to form the nonexplosive water molecule, H_2O. Other precautions used are hydrogen alarms and a hot filament in the source cabinet and in the scavenger end of the furnace to immediately burn off any free hydrogen before it can explode.

Chlorine-added oxidation. The thinner MOS gate oxides require very clean layers. Improvements in cleanliness and device performance are achieved when chlorine is incorporated into the oxide. The chlorine tends to reduce mobile ionic charges in the oxide layer, reduce structural defects in the oxide and silicon surface, and reduce charges at the oxide-silicon interface. The chlorine comes from the inclusion of anhydrous chlorine (Cl_2), anhydrous hydrogen chloride (HCl), trichloroethylene (TCE), or trichloroethane (TCA) in the dry oxygen gas stream. The gas sources, chlorine and hydrogen chloride, are metered into the tube along with the oxygen from separate flow meters in gas flow controller. The liquid sources, TCE and TCA, are carried into the tube as vapors from liquid bubblers. For safety and ease of delivery, TCA is the preferred source of chlorine. The oxidation-chlorine cycle may take place in one step or be preceded or followed by a dry oxidation cycle.

Wafer-cleaning station

When the wafers come to a tube furnace, they first go to the attached wafer-cleaning station. The need for stringent cleanliness control has been stressed throughout this text. It is especially important before the tube operations because of the heating of the wafers. Contamination left on the wafer surfaces can pit the surface, diffuse into the surface, or interfere with the quality of the layer being grown.

The cleaning station may be a VLF "wet" bench that has built-in tanks for cleaning chemicals, units for rinsing the wafers in deionized water, and drying units. The station may be, or include, an automatic cleaning machine The station also has a wafer rinse and drying machine. Wafer cleaning is detailed in the section on "Oxidation Processes."

Wafer-load station. After cleaning, the wafers are passed to the in-line load station. Here, the wafers are inspected for cleanliness and loaded into holders for insertion into the tube. The station is located under a ceiling-mounted HEPA filter or in a VLF hood. The loading station

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and the cleaning station are located next to each other in such a manner that the wafers stay in a clean environment during the transfer.

A quick surface inspection of the wafers is normally done with the aid of an ultraviolet light. These high-intensity light sources allow the operator to see small particles and stains that are not visible to the naked eye. Sometimes, a microscope inspection of the surface is performed.

Automatic wafer loading. Production efficiency and VLSI cleanliness requirements have led to the development of a variety of automatic boat- and tube-loading mechanisms. Pick-and-place machines (sometimes called *robots*) pick each of the wafers out of one cassette and place it into an empty one. Some versions of pick-and-place machines pick up the entire load of wafers and transfer it in one operation to the empty cassette. A challenge to any wafer boat-loading system is the correct placement of test wafers within the load of device wafers as well as "dummy wafers" often placed at the ends (or top and bottom) of a boat load of wafers (see p. 190). These wafers must be *picked* from other boats.

An additional challenge is the loading two wafers back-to-back in the same slot. This procedure is used to increase the productivity of the operation.

The loaded cassettes are put into the furnace by a number of techniques. One is to place the loaded boat into a transfer tube called an *elephant*. The elephant has a ground joint that mates with the joint on the load end of the tube. It also has a hole in the back end to admit a quartz rod that hooks into the back end of the wafer boat. The tube is used to push the boat into the flat zone of the tube furnace (Fig. 7.29). Other versions automate the push-pull action with a push rod connected to a motor. A number of cassettes are placed by the operator on a platform called a *paddle*. The paddle moves the cassettes into the tube under the control of a motor (Fig. 7.30).

Boat loading can be a source of severe wafer contamination from particles scraped from the inside of the tube as the cassettes are shoved down the tube. One technique for solving this problem is to use

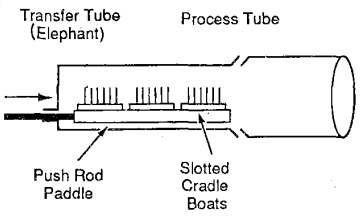


Figure 7.29 Transfer tube loading of wafers.

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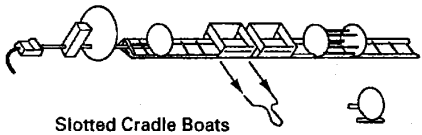


Figure 7.30 Wafer boat and cradle.

cassettes or paddles with small wheels. The rolling wheels kick up fewer particles than does scraping. Another solution is a cantilever system, which features a rigid rod with the cassettes positioned on the end. The rod moves the cassettes down the center of the tube without ever touching its sides. Some systems leave the cassettes suspended in the center of the tube, while others give the cassettes a soft landing on the tube bottom.

Automated push-pull machines are necessary to achieve the control required for slow entry and exit of the wafers to prevent warping. A typical push-pull rate is 1 in/min. A standard four-stack furnace system requires an automatic push-puller for each of the tubes. Although these systems load and unload automatically, they require an operator to place the loaded boats on the paddle.

An overriding goal of process equipment design is "hands-off" operation. That need is addressed in tube furnace systems built on the elevator design.[13] The concept employs a storage buffer of loaded tube cassettes whose tube destination is known by a computer. When it is time for the cassettes to be loaded in the tube, a robot selects the proper cassettes and moves to the correct tube position and loads them into the tube. The advantages of these systems are the computer production control and the need for only one loading mechanism per furnace stack. For a properly designed system, robotic activity is less contaminating to the wafers than human operators.

Manual wafer loading. Wafers are processed through the cleaning steps in Teflon® or Teflon-derivative wafer holders, also called *boats* or *cassettes*. They are transferred to quartz or silicon carbide holders for the furnace process. The boats come in various designs (Fig. 7.30), depending on the degree of control required of the operation and the loading density. The most productive designs have the wafers standing up in machined slots, positioned crosswise to the gas flow. In tube operations where uniformity is critical, the wafers may be loaded parallel to the gas flow.

The weight and value of larger diameter wafers dictates wafer handling by automatic systems. However there is always a need to select single wafers for examination or testing. For these operation wafer handling is by vacuum wands or limited-grasp tweezers (Fig. 7.31).

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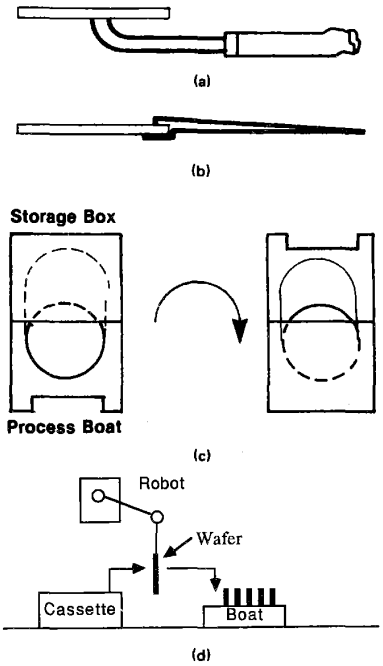


Figure 7.31 Manual wafer handling devices. (*a*) Vacuum pick-up, (*b*) limited-grasp tweezer, (*c*) flip transfer boats, and (*d*) auto pick-and-place.

Vacuum wands are attached to a vacuum source and are designed to allow grasping of the wafers from the backside. This arrangement minimizes damage and contamination of the sensitive front side of the wafer.

Oxidation Process Automation

Tube furnaces have evolved from operator-controlled manual systems to various levels of automation. A modern production tube furnace is automated from wafer load to wafer unload in a one-button operation. A goal is to automate the process from wafer clean to unload. The operator places the cassettes of cleaned wafers on the load mechanism and pushes the start button. The computer takes over and directs the tube furnace through the predetermined process, which is called a *recipe*. The times, temperatures, gas sequences, and push-pull rates are programmed into an on-board computer or a host computer. Full automation of a tube operation involves delivery of the proper wafers to the station with robots or automatic equipment taking the wafers entirely through the process and passing them on to the next process.

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The various components of a furnace process may be organized in a *cluster* arrangement (see Chapter 15).

Preoxidation Wafer Cleaning

Removal of surface contamination and unwanted native oxides is essential to a successful oxidation process. Contamination can diffuse into the wafer causing electrical problems in devices and structural integrity problems in the silicon dioxide film. Thin layers of native oxides can alter the thickness and integrity of the grown oxide layer.

Preoxidation processes (see Chapter 5) typically start with a mechanical scrubber, followed by an RCA wet cleaning sequence to remove organic and inorganic contamination. Finally, an HF or diluted HF etch is performed to rid the surface of native or chemically grown oxides. This is an HF-last process.

The processing of the wafers through the oxidation process is divided into several distinct steps, as shown in the flow diagram in Fig. 7.32. After the wafers are logged into the station, they receive a thorough cleaning. Clean wafers are essential at all stages of the fabrication process but are especially necessary before any of the operations performed at high temperature.

Oxidation Processes

After the wafers are precleaned, cleaned and etched, and loaded on the push-pull mechanism, they are ready for surface oxidation. The actual oxidation proceeds in different gas cycles (Fig. 7.33) within the furnace tube. The first gas cycle occurs as the wafers are being loaded into the tube. Since the wafers are at room temperature and precise oxide thickness is a goal of the operation, the gas metered into the

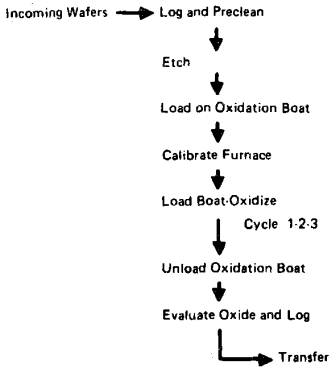


Figure 7.32 Oxidation process flow.

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Cycle	Gas	Purpose
1.	Nitrogen	Temperature Stabilization in an Inert Atmosphere
2.	Oxygen or Water Vapor	Oxide Growth
3.	Nitrogen	Stop Oxidation and Removal of Wafers in an Inert Atmosphere

Figure 7.33 Oxidation process cycles.

tube during loading is dry nitrogen. The nitrogen is necessary to prevent any oxidation while the wafers are coming up to the required oxidation temperature.

Once the wafers are stabilized at the correct temperature, the flow gas controller switches the gas flow to the selected oxidant. For oxides greater than 1200 Å, the oxidant is usually steam from one of the sources previously discussed. For oxides less than 1200 Å, pure oxygen is usually used because of its greater process control and the cleaner, denser oxide it produces. Thin MOS transistor gate oxides are usually grown at lower temperatures (900°C) in oxygen. However, oxidation process times can require hours in the furnace. One alternative is to grow thin gates oxides in wet oxygen environments to reduce process time, but in a reduced pressure. Lowering the pressure maintains oxide density and structural integrity.[28] The thinner MOS gate oxides require very clean layers. Improvements in cleanliness and device performance are achieved when chlorine is incorporated into the oxide.[29] The chlorine tends to reduce mobile ionic charges in the oxide layer, reduce structural defects in the oxide and silicon surface, and reduce charges at the oxide-silicon interface.

The chlorine comes from the inclusion of anhydrous chlorine (Cl_2), anhydrous hydrogen chloride (HCl), trichloroethylene (TCE), or trichloroethane (TCA) in the dry oxygen gas stream. The gas sources, chlorine and hydrogen chloride, are metered into the tube along with the oxygen from separate flow meters in gas flow controller. The liquid sources, TCE and TCA, are carried into the tube as vapors from liquid bubblers. For safety and ease of delivery, TCA is the preferred source of chlorine.

The oxidation-chlorine cycle may take place in one step or be preceded or followed by a dry oxidation cycle. After the oxidation cycle, the furnace gas is switched back to dry nitrogen. The nitrogen terminates the oxidation of the silicon by diluting and removing the oxidant used. It also prevents any oxidation during the wafer exit step.

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Postoxidation Evaluation

After the wafers are removed from the oxidation boats, they will receive an inspection and evaluation(s). The nature and number of the evaluations depend on the oxide layer and the precision and cleanliness required of the particular circuit being fabricated. (The details of the evaluations performed are explained in Chapter 14.)

A requirement of the oxidation process is a uniform noncontaminated layer of silicon dioxide on the wafer. As the wafers proceed through the wafer fabrication operations, there is a buildup of both thermally grown oxides and other deposited layers on the wafer surface. These other layers interfere with the determination of the quality of a particular oxide. For this reason, each batch of oxidized wafers going into the tube includes a number of test wafers, with bare surfaces placed at strategic locations on the wafer boat. Test wafers are necessary for the evaluations that are destructive or require large undisturbed areas of oxide. At the conclusion of the oxidation operation, they are used for the evaluation of the process. Some of the evaluations are performed by the oxidation operator and some are performed off line in quality control (QC) labs.

Surface inspection

A quick check of the cleanliness of the oxide is performed by the operator as the wafers are unloaded from the oxidation boat. Each wafer is viewed under a high-intensity ultraviolet (UV) light. Surface particulates, irregularities, and stains are readily apparent in UV light.

Oxide thickness

The thickness of the oxide is of major importance. It is measured on test wafers by a number of techniques (see Chapter 14). The techniques are color comparison, fringe counting, interference, ellipsometers, stylus apparatus, and scanning electron microscopes (SEMs).

Oxide and furnace cleanliness

In addition to the physical contaminants of particles and stains, the oxide should have a minimum number of mobile ionic contaminants. These are detected by the sophisticated capacitance-voltage (C/V) technique, which detects the total number of mobile ionic contaminants present in the oxide. It cannot identify the origin of those contaminants, which may come from the tubes, the gases, the wafers, or the cleaning process. Therefore, C/V evaluation is a go-no-go assessment of the wafers and serves as a check of the total furnace operation.

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In most fabrication lines, C/V analysis is also used to certify the cleanliness of the furnace and its associated parts. A oxide with a low-mobile ionic contamination level certifies that the entire system is clean. When the oxide fails the test, more investigation is necessary to identify the source.

A second oxide-cleanliness-related parameter is dielectric strength. This parameter measures the dielectric (nonconducting) property of the oxide by the destructive oxide rupture test.

A third cleanliness factor is the index of refraction of the oxide. Refraction is the property of a transparent substance that causes light to bend as it travels through it. The apparent versus actual location of an object on the bottom of a body of water is an example of refraction. The index of refraction of a pure oxide is 1.46. Variations of this value come about from impurities in the oxide. A constant index of refraction is the starting point for several of the interference thickness-measurement techniques. Variations in the index can lead to erroneous thickness measurements. The index of refraction is measured by interference and ellipsometry techniques (see Chapter 14).

Thermal nitridation

An important factor in the production of small high-performance MOS transistors is a thin gate oxide. However, in the 100-Å (or less) range, silicon dioxide films tend to be of poor quality and difficult to control. An alternative to silicon dioxide films is a thermally grown silicon nitride (Si_3N_4) film. Si_3N_4 is denser than silicon oxide and has fewer pinholes in these thin ranges. It also is a good diffusion barrier. Growth control of thin films is enhanced by a flat growth mechanism (after an initial rapid growth). This characteristic is shown (Fig. 7.34) in the

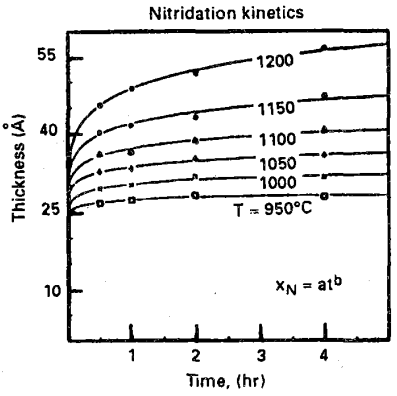


Figure 7.34 Nitridation of ⟨100⟩ silicon. *(Source: Wolf,* Silicon Process.)

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growth of silicon nitride formed by the exposure of the silicon surface to ammonia (NH_3) between 950 and 1200°C.[30]

Some advanced devices use silicon oxynitride (SiO_xN_y) films. They are also called *nitrided-oxide* or *nitroixide* films. These are formed from the nitridation of silicon oxide films. Unlike silicon dioxide films, oxynitride films vary in composition depending on the growth process.[31] Another MOS gate structure is a sandwich of oxide/nitrite/oxide (ONO).[32]

Review Questions

1. Describe the role and movement of oxygen during thermal oxidation.
2. Draw a sketch of a horizontal tube furnace and identify all the sections.
3. Explain why dryox is favored for VLSI oxidation processes.
4. Why are temperature ramping techniques required?
5. What is the advantage of rapid thermal oxidation?
6. Name the two oxidants added to sulfuric acid for wafer cleaning.
7. Make a flow diagram of the oxidation steps, from incoming wafer to evaluation.
8. Name the three factors that determine the oxide thickness.
9. What advantages are offered by high-pressure oxidation?
10. List three uses of silicon dioxide layers in semiconductor devices.

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Chapter

8

The Ten-Step Patterning Process—Surface Preparation to Exposure

Overview

Patterning is the series of processes that establishes the shapes, dimensions, and placement of the required physical "parts" (components) of the IC in and on the wafer surface layers. This chapter presents the first four steps of a basic ten-step photo process and a discussion of photoresist chemistry.

Objectives

Upon completion of this chapter, you should be able to:

1. Sketch wafer cross sections showing the basic ten-step photomasking process.
2. Explain the reaction of negative and positive photoresists to light.
3. Describe the correct resist and mask polarities required to produce holes and islands in wafer surface layers.
4. Make a list of the major process options for each of the ten basic steps.
5. Select from the list in objective 4 the processes used to pattern features in micron and submicron sizes.
6. Describe the need for, and process steps used in, double masking, multilayer resist processing, and planarization techniques.
7. Explain the use of antireflective coatings and contrast enhancement in the patterning of "small" feature sizes.

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8. List the optical and nonoptical methods used for alignment and exposure.
9. Compare the equipment and advantages of each alignment and exposure method.

Introduction

Patterning is one of the basic operations. At the end of the operation, a surface layer is left with either a hole or an island. (See Fig. 8.1.) *Patterning* is also called *photolithography, photomasking, masking, oxide removal (*OR)*), metal removal* (MR), and *microlithography.*

Patterning is one of the most critical operations in semiconductor processing. It is the process that sets the surface (horizontal) dimensions on the various parts of the devices and circuits. The goal of the operation is twofold. First is to create, in and on the wafer surface, a pattern with the dimensions established in the design phase of the IC or device. This goal is referred to as the *resolution* of the images on the wafer.

The second goal is the correct placement of the circuit pattern on the wafer. The entire circuit pattern must be correctly placed on the wafer surface relative to the crystal pattern of the wafer substrate, and the individual parts of the circuit must line up relative to each other (Fig. 8.2). This is called *alignment* or *registration* of the various circuit patterns. A typical IC requires 20 to 40 individual patterning (or masking) steps. This registration requirement is similar to the correct alignment of the different floors of a building. It is easy to visualize that misalignment of elevator shafts and stair wells would render the building useless. In a circuit, the effects of misaligned mask layers can cause the entire circuit to fail.

Control of the dimensions and defect levels is difficult, because each step in the patterning process contributes variations. A patterning

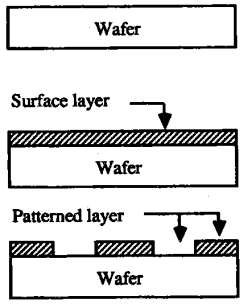


Figure 8.1 Basic patterning process.

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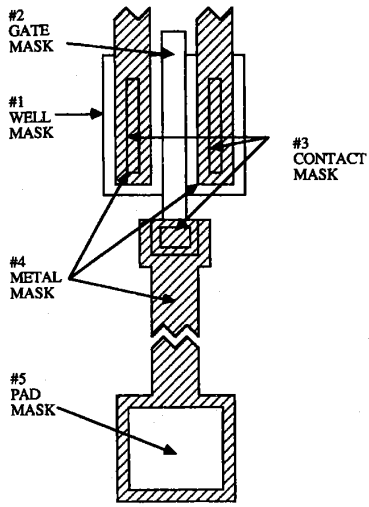


Figure 8.2 Five mask set silicon gate transistor.

process is one of trade-offs and balancing (see sections on individual patterning processes). In addition to dimensional control and pattern alignment, defect control during the process steps is critical. Given the number of steps in each patterning operation and the number of mask layers, the masking process is the chief source of defects.

Overview of the Photomasking Process

Photolithography is a multistep pattern transfer process similar to photography and stenciling. The required pattern is first formed in reticles or photomasks and transferred into the surface layer(s) of the wafer through the photomasking steps.

The transfer takes place in two steps. First, the pattern on the reticle or mask is transferred into a layer of photoresist (Fig. 8.3). Photoresist is a light-sensitive material similar to the coating on a regular photographic film. Exposure to light causes changes in its structure and properties. In the example in Fig. 8.3, the photoresist in the region exposed to the light was changed from a soluble condition to an insoluble one. Resists of this type are called *negatively acting,* and the chemical change is called *polymerization.* Removing the soluble portion with chemical solvents (developers) leaves a hole in the resist layer that corresponds to the opaque pattern on the reticle.

The second transfer takes place from the photoresist layer into the wafer surface layer (Fig. 8.4). The transfer occurs when etchants re-

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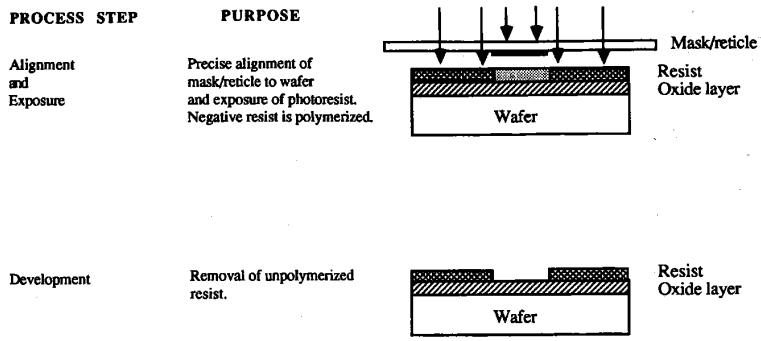


Figure 8.3 First pattern transfer—mask/reticle to resist layer.

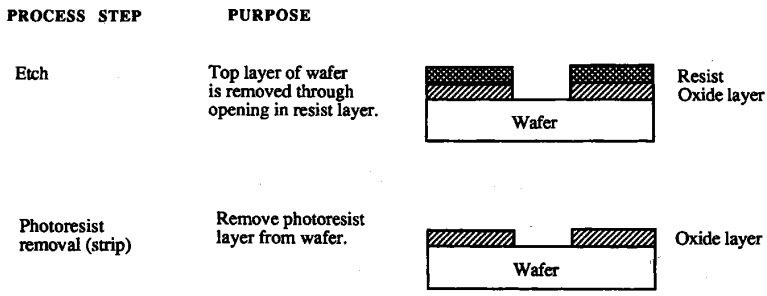


Figure 8.4 Second pattern transfer—resist layer to surface layer.

move the portion of the wafer's top layer that is not covered by the photoresist. The chemistry of photoresists is such that they do not dissolve (or dissolve slowly) in the chemical etching solutions; they are *etch-resistant,* hence the name *resists* or *photoresists.*

In the examples shown in Figs. 8.3 and 8.4, the result is a hole etched in the wafer layer. The hole came about because the pattern in the mask was opaque to the exposing light. A mask whose pattern exists in the opaque regions is called a *clear-field mask* (Fig. 8.5). The pattern could also be coded in the mask in the reverse, in a dark-field mask. If the same steps were followed, the result of the process would be an island of material left on the wafer surface (Fig. 8.6).

The resist reaction to light just described is a character of negative-acting photo resists. There are also positive-acting photo resists. Within these resists, the light changes the chemical structure from relatively nonsoluble to much more soluble. The term describing this

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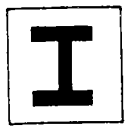




Figure 8.5 Mask-reticle polarities.

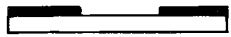




Figure 8.6 Photomasking hole and island.

change is *photosolubilization*. Figure 8.7 shows that an island is produced when a light-field mask is used with a positive photoresist.

The result obtained from the photomasking process from different combinations of mask and resist polarities is shown in Fig. 8.8. The choice of mask and resist polarity is a function of the level of dimensional control and defect protection required to make the circuit work. These issues are discussed in the process sections of the chapter.

Ten-Step Process

Transferring the image from the reticle or mask onto the wafer surface layer is a multistep procedure (Fig. 8.9). Feature size, alignment tolerance, the wafer surface, and the masking layer number all influence the difficulty and steps for a particular masking process. Many photo processes are customized to the particular conditions. However, most are variations or options of a basic ten-step process. The process illustrated is shown with a light-field mask and a negative photoresist.

The first image transfer takes place in steps 1 through 7. In steps 8, 9, and 10, the image is transferred (second image transfer) into the wafer surface layer. The reader is challenged to list the steps and draw the corresponding cross sections using combinations of a dark field mask and a positive photoresist. It is strongly recommended that the reader master this ten-step process before proceeding to the advanced photolithography processes.

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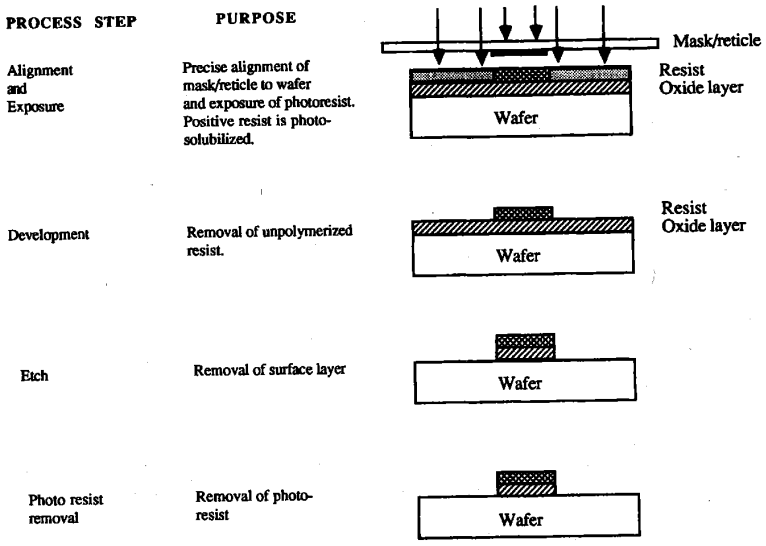


Figure 8.7 Image transfer from a light-field mask with a positive photoresist to create an island.

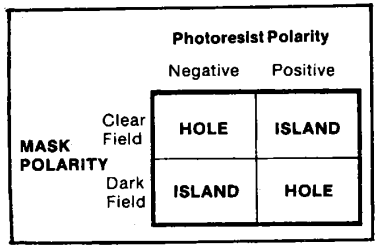


Figure 8.8 Mask and photoresist polarity results.

Basic Photoresist Chemistry

Photoresists have been used in the printing industry for over a century. In the 1920s, they found wide application in the printed circuit board industry. The semiconductor industry adapted this technology to wafer fabrication in the 1950s. Negative and positive photoresists designed for semiconductor use were introduced by Eastman Kodak and the Shipley Company, respectively, in the late 1950s.

The photoresist is the heart of the masking process. The preparation, bake, exposure, etch, and removal processes are fine-tuned to ac-

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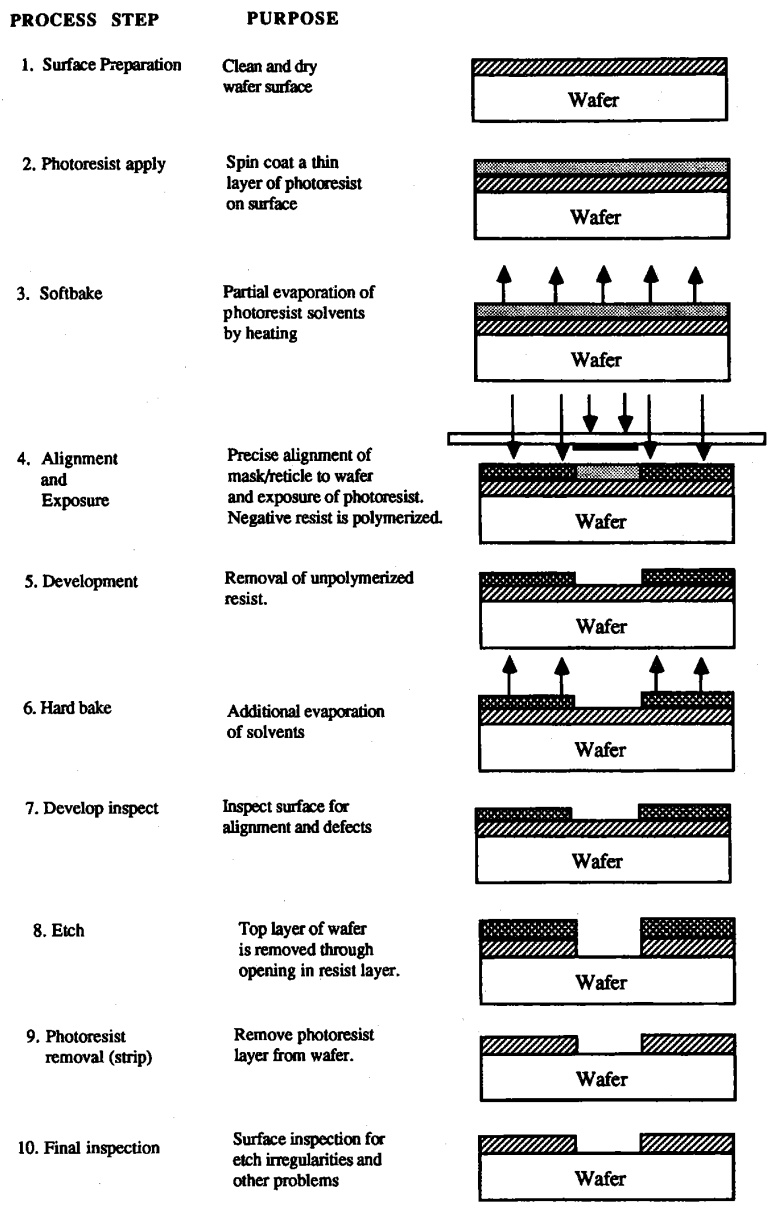


Figure 8.9 Ten-step photomasking process.

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commodate the particular resist used and the desired results. The selection of a resist and development of a resist process is a detailed and lengthy procedure. Once a resist process is established, it is changed very reluctantly.

Photoresist composition

Photoresists are manufactured for both general and specific applications. They are tuned to respond to specific wavelengths of light and different exposing sources. They are given specific thermal flow characteristics and formulated to adhere to specific surfaces. These properties come about from the type, quantity, and mixing procedures of the particular chemical components in the resist. There are four basic ingredients (Fig. 8.10) in photoresists: polymers, solvents, sensitizes, and additives.

Light-sensitive and energy-sensitive polymers. The ingredients that contribute the photosensitive properties to the photoresist are special light- and energy-sensitive polymers. Polymers are groups of large, heavy molecules containing carbon, hydrogen, and oxygen that are formed into a repeated pattern. Plastics are a form of polymers.

The most commonly used resists are designed to react to ultraviolet or laser sources. They are called *optical resists*. Others respond to X-rays or electron beams.

In a negative resist, the polymers change from unpolymerized to polymerized after exposure to a light or energy source. Physically, the polymers form a cross-linked material that is etch resistant (see Fig. 8.11). In most negative resists, the polymers are a polyisopreme,

Component	Function
Polymer	Polymer structure changes from soluble to polymerized (or vice versa) when exposed by the exposure source in an aligner.
Solvent	Thins resist to allow application of thin layers by spinning.
Sensitizers	Controls and/or modifies chemical reaction of resist during exposure.
Additives	Various added chemical to achieve process results, such as dyes.

Figure 8.10 Photoresist components.

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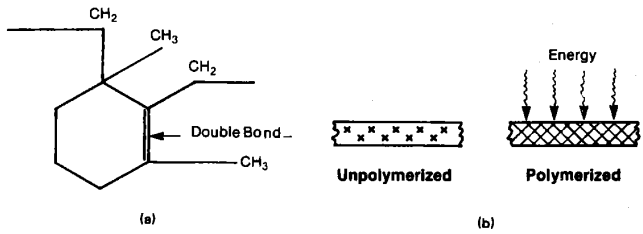


Figure 8.11 Negative resist chemistry.

which is a synthetic form of natural rubber. Polymerization also happens when the resist is exposed to heat and/or normal light. To prevent accidental exposure, photomasking areas processing negative resist use yellow filters or yellow lighting.

The basic positive photoresist polymer is the phenol-formaldehyde polymer, also called the phenol-formaldehyde novolak resin (Fig. 8.12). Within the resist, the polymer is relatively insoluble. After exposure to the proper light energy, the resist converts to a more soluble state. This reaction is called *photosolubilization.* The photosolubilized part of the resist can be removed by a solvent in the development process.

Photoresists respond to many forms of energy. The forms are often referred to by their general category (light, heat radiation, and so on), or by a specific portion of the electromagnetic spectrum [ultraviolet light (UV), deep ultraviolet (DUV), I line, and so forth] (see "Exposure sources," p. 233). The exposing energies used are detailed in the section on alignment and exposure. A number of strategies are used to resolve small images (see "Comparison of Positive and Negative Resists," p. 212). One is to use a narrower (or single) wavelength exposing source. The traditional novolak-based positive resist has been

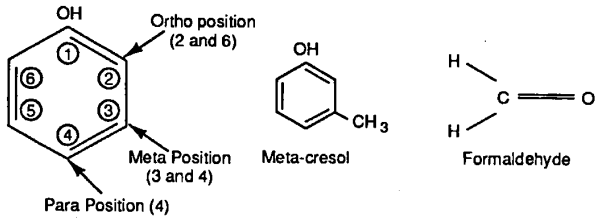


Figure 8.12 Phenol-formaldehyde novolak resin structure. *(After: W. S. DeForest,* Photoresist: Materials and Processes, *McGraw-Hill, New York, 1975.)*

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fine tuned for use with I-line exposure sources. However, it does not work as well with DUV sources. Resist manufacturers have developed *chemically amplified resists* for this exposure source. Chemically amplified means that the chemical reactions of the polymer are increased by chemical additives. Resists for X-ray and electron beam (e-beam) are based on polymers different from conventional positive and negative resist chemistry.

Figure 8.13 contains a list of resist polymers used in production resists. The relative merits of negative and positive resists are given at the end of this section, and uses of these two types of resists and others are discussed at the end of the process sections.

Solvents. The largest ingredient by volume in a photoresist is the solvent. It is the solvent that makes the resist a liquid and allows the resist to be applied to the wafer surface as a thin layer by spinning. Photoresist is analogous to paint, which is composed of the coloring pigment dissolved in an appropriate solvent. It is the solvent that allows the application of the paint onto a surface in a thin layer. For negative photoresist, the solvent is an aromatic type, xylene. In positive resist, the solvent is either ethoxyethyl acetate or 2-methoxyethyl.

Sensitizers. Chemical sensitizers are added to the resists to cause or control certain reactions of the polymer. In negative resists, the untreated polymer responds (polymerizes) to a certain range of the ultra-

Resist	Polymer	Polarity	Sensitivity (Coul/cm^2)	Exposure Radiation
Positive	Novolak (M-Cresol-formaldehyde)	+	$3\text{–}5 \times 10^{-5}$	UV
Negative	Poly Isoprene	-		UV
PMMA	Poly-(Methyl Methacrylate)	+	5×10^{-5}	E-Beam
PMIPK	Poly-(Methyl Isopropenyl Ketone	+	1×10^{-5}	E-Beam/ Deep UV
PBS	Poly-(Butene-1-Sulfone)	+	2×10^{-6}	E-Beam
TFECA	Poly-(Trifluoroethyl Chloroacrylate	+	8×10^{-7}	E-Beam
COP (PCA)	Copolymer-(α-Cyano Ethyl Acrylate-α-Amido Ethyl Acrylate)	-	5×10^{-7}	E-Beam X-Ray
PMPS	Poly-(2-Methyl Pentene-1-Sulfone)	+	2×10^{-7}	E-Beam

Figure 8.13 Resist comparison table.

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violet spectrum. Sensitizers are added to either broaden the response range or narrow it to a specific wavelength. In negative resists, a compound called bis-aryldiazide is added to the polymer to provide the light sensitivity.[1] In positive resists, the sensitizer is *o*-naphthaquinonediazide.

Additives. Various additives are mixed with resists to achieve particular results. Some negative resists have dyes intended to absorb and control light rays in the resist film. Positive resists may have chemical *dissolution inhibitor systems.* These are additives that inhibit the dissolution of nonexposed portions of the resist during the development step.

Photoresist Performance Factors

The selection of a photoresist is a complicated procedure. The primary driving force is the dimensions required on the wafer surface. The resist must first have the capability of producing those dimensions. Beyond that, it must also function as an etch barrier during the etching step, a function that requires a certain thickness for mechanical strength. In the role of etch barrier, it must be free of pinholes, which also requires a certain thickness. In addition, it must adhere to the top wafer surface, or the etched pattern will be distorted, just as a paint stencil will give a sloppy image if it is not taped tightly to the surface. These, along with process latitude and step coverage capabilities, are resist performance factors. In the selection of a resist, the process engineer often must make trade-off decisions between the various performance factors. The photoresist is one part of a complicated system of chemical processes and equipment that must work together to produce the image results and be productive; that is, it must enable an acceptable cost of ownership for the whole patterning process.

Resolution capability

The smallest opening or space that can be produced in a particular photoresist is generally referred to as its *resolution capability.* The smaller the opening or space produced, the better the resolution capability. Resolution capability for a particular resist is referenced to a particular process, including the exposing source and developing process. Changing the other process parameters will alter the inherent resolution capability of the resist. Generally, smaller line openings are produced with thinner resist film thicknesses. However, a resist layer must be thick enough to function as an etch barrier and be pinhole free. The selection of a resist thickness is a trade-off between these two goals.

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The capability of a particular resist relative to resolution and thickness is measured by its *aspect ratio* (Fig. 8.14). The aspect ratio is calculated as the ratio of the resist thickness to the image opening. As the industry requires smaller patterns, the factor of pattern density and shape become an influence on photoresist design. For a given resist, isolated patterns, small contact holes, and high-density pattern areas will all expose and develop differently as a result of reflection and chemical reaction factors. Consequently, there are available resists specifically designed for use in these situations.

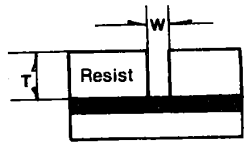
Positive resists have a higher aspect ratio as compared to negative resists, which means that, for a given image-size opening, the resist layer can be thicker. The ability of positive resist to resolve a smaller opening is a result of the smaller size of the polymer. It is a little like using a smaller brush to paint a thinner line.

Adhesion capability

In its role as an etch barrier, a photoresist layer must adhere well to the surface layer to faithfully transfer the resist opening into the layer. Lack of adhesion results in distorted images. Resists differ in their ability to adhere to the various surfaces used in chip fabrication. Within the photomasking process, a number of steps are specifically included to promote the natural adhesion of the resist to the wafer surface. Negative resists generally have a higher adhesion capability than positive resists.

Photoresist exposure speed, sensitivity, and exposure source

The primary action of a photoresist is a change in structure in response to an exposing light or radiation. An important process factor is the speed at which that reaction takes place. The faster the speed, the faster the wafers can be processed through the masking area. Negative resists typically require 5 to 15 sec of exposure time, whereas positive resists take three to four times longer.



Aspect Ratio = $\frac{W}{T}$

Figure 8.14 Aspect ratio.

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The sensitivity of a resist relates to the amount of energy required to cause the polymerization or photosolubilization to occur. Furthermore, sensitivity relates to the energy associated with specific wavelength of the exposing source. Understanding this property requires a familiarization with the nature of the electromagnetic spectrum (Fig. 8.15). Within nature, we identify a number of different types of energy: light, short and long radio waves, X-rays, and so on. In reality, they are all electromagnetic energy (or radiation) and are differentiated from each other by their wavelengths, with the shorter wavelength radiation having higher energies.

Common positive and negative photoresists respond to energies in the ultraviolet and deep ultraviolet (DUV) portion of the spectrum (Fig. 8.16). Some are designed to respond to particular wavelength peaks (g, h, i lines in Fig. 8.18) within those ranges. Some resists are designed to work with X-rays or electron beams (e-beams). Resist sensitivity, as a parameter, is measured as the amount of energy required to initiate the basic reaction. The units are millijoules per square centimeter (mJ/cm^2).[2] The specific wavelengths the resist reacts to are called the *spectral response characteristic* of the resist. Figure 8.17 shows the spectral response characteristic of a typical production resist. The peaks in the spectrum are regions (wavelengths) that carry higher amounts of energy (Fig. 8.18). The different light sources used

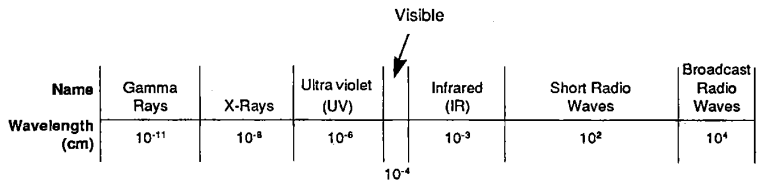


Figure 8.15 Electromagnetic spectrum.

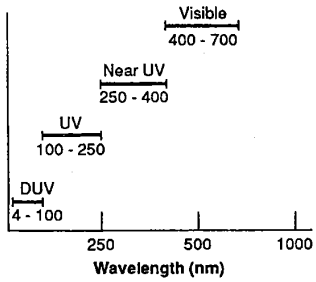


Figure 8.16 Ultraviolet and visible spectrum. (*After Elliott.*[1])

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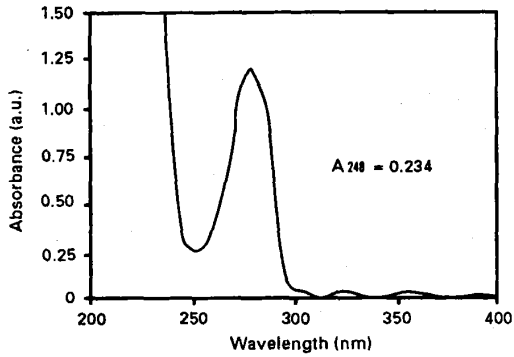


Figure 8.17 Exposure response curve. *(Source: Shipley Megaposit XP-89131 Photo Resist.)*

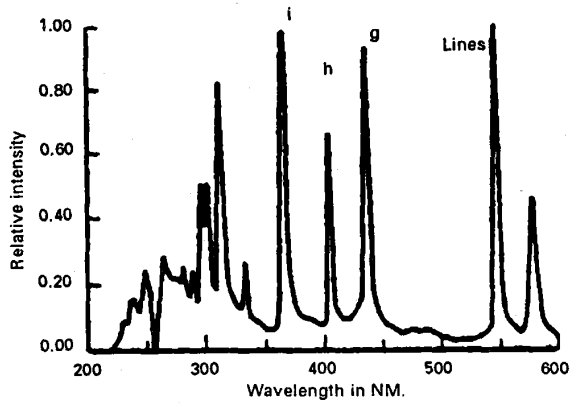


Figure 8.18 Mercury (Hg) spectrum. *(From* Silicon Processing for the VLSI, *by Wolf and Tauber.)*

in masking areas are covered in the "Alignment and Exposure" section, p. 231.

Process latitude

While reading the sections on the individual masking process steps, the reader should keep in mind the fact that the goal of the overall process is a faithful reproduction of the required image size in the wafer layer(s). Every step has an influence on the final image size, and each of the steps has inherent process variations. Some resists are

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more tolerant of these variations; that is, they have a wider process latitude. The wider the process latitude, the higher the probability that the images on the wafer will meet the required dimensional specifications.

Pinholes

Pinholes are microscopically small voids in the resist layer. They are detrimental, because they allow etchants to seep through the resist layer and etch small holes in the surface layer. Pinholes come from particulate contamination in the environment, the spin process, and from structural voids in the resist layer.

The thinner the resist layer, the more pinholes. Therefore, thicker films have fewer pinholes, but they also make the resolution of small openings more difficult. These two factors present one of the classic trade-offs in determining a process resist thickness. One of the principal advantages of positive resists is their higher aspect ratio, which allows a thicker resist film and a lower pinhole count for a given image size.

Particle and contamination levels

Resists, like other process chemicals, must meet stringent standards for particle content, sodium and trace metal contaminants, and water content.

Step coverage

By the time the wafer is ready for the second masking process, the surface has a number of steps. As the wafer proceeds through the fabrication process, the surface gains more layers. For the resist to perform its etch barrier role, it must maintain an adequate thickness over these earlier layer steps. The ability of a resist to cover surface steps with adequate resist is an important parameter.

Thermal flow

During the masking process, there are two heating steps. The first, called *soft bake,* evaporates solvents from the resist. The second one, *hard bake,* takes place after the image has been developed in the resist layer. The purpose of the hard bake is to increase the adhesion of the resist to the wafer surface. However, the resist, being a plastic-like material, will soften and flow during the hard-bake step. The amount of flow has an important effect on the final image size. The resist has to maintain its shape and structure during the bake, or the process design must account for dimensional changes due to thermal flow.

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The goal of the process engineer is to achieve as high a bake temperature as possible to maximize adhesion. This temperature is limited by the flow characteristics of the resist. In general, the more stable the thermal flow of the resist, the better it is in the process.

Comparison of Positive and Negative Resists

Up to the mid-1970s, negative resist was dominant in the masking process. The advent of VLSI circuits and image sizes in the 2- to 5-μm range strained the resolution capability of negative resists. Positive resists had been around for over 20 years, but their poorer adhesion properties were a drawback, and their superior resolution capability and pinhole protection were not needed.

In the 1980s, positive resist became the resist of choice. The transition was not easy. Switching to a positive resist requires changing the polarity of the masks or reticles. Unfortunately, it is not a matter of simply reversing the fields in the mask-making process. Reticle/mask dimensions print differently with the two resists (Fig. 8.19). With negative resist and a light-field masks, the dimension in the resist is smaller than the mask/reticle dimension as a result of light wrapping (diffraction) around the image. With a positive resist and a dark-field mask, the diffraction tends to widen the image. These changes must be considered in making the mask/reticle and designing the other masking processes. In other words, an entirely new process is required to switch resist types.

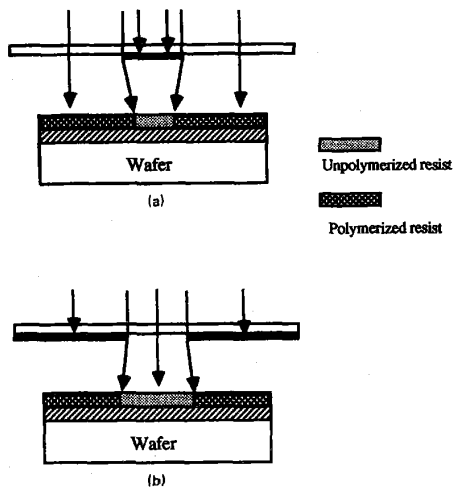


Figure 8.19 Changes in image size with (*a*) image size reduction with light-field mask and negative resist, and (*b*) image size enlargement with dark-field mask and positive photoresist.

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Most of the images on most of the mask layers are holes. With positive resist, the mask polarity is dark field, which results in additional pinhole protection for the wafer (Fig. 8.20). Clear-field masks are prone to small cracks in the glass surface. These cracks, called *glass damage,* block the exposing light, creating unwanted holes in the photoresist layer, which in turn etch into the wafer surface as holes. The same is true for dirt particles that locate on the clear area of the mask/reticle. On dark-field masks, the majority of the surface is covered by chrome, which is hard and less likely to have pinholes. Thus, the wafer has fewer unwanted pinholes.

Another problem with negative resists is oxygenation. This is a reaction of the resist to oxygen in the atmosphere, and it can cause a thinning of the resist film by as much as 20 percent. Positive resists do not have this property. Positive resists are more expensive than negative resists but, for a demanding process, the higher cost is offset by higher yield. For very small image sizes, positive resist is the only choice.

Developing characteristics differ between the two types of resists. Negative resists develop in readily available solvents and feature a high solubility differential between the polymerized and unpolymerized areas. The image dimensions remain relatively constant during the development step. Positive resists have a lower solubility between the polymerized and unpolymerized areas requiring carefully prepared developer solutions and require temperature control of the pro-

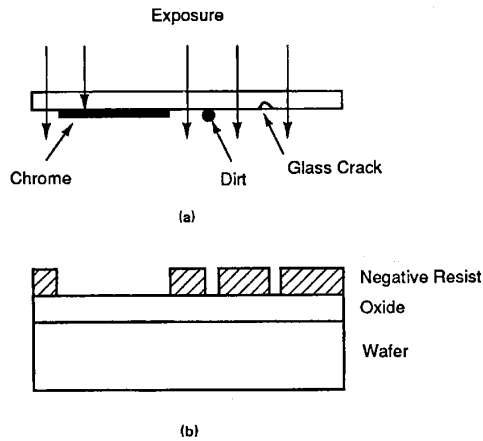


Figure 8.20 (*a*) Clear-field mask with dirt particle and glass crack, and (*b*) result in negative resist after develop.

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cess. Dissolution inhibitor systems are added specifically to control dimensions during development.

Photoresist removal is also a factor. Generally, the removal of positive resists is easier and takes place in chemicals that are more environmentally sound. Fabrication areas producing devices and circuits with image sizes greater than 2 μm may still use negative resists. Figure 8.21 shows a comparison of properties of the two resists.

Physical Properties of Photoresists

The performance factors just detailed and all of the ten basic process steps are related to a number of physical and chemical properties of the resist. These properties are rigorously controlled by resist manufacturers.

Solids content

A photoresist is a liquid that is applied to the wafer by a spinning technique. The thickness of resist left on the wafer is a function of the spin step parameters and several resist properties: *solids content* and *viscosity.*

Recall that the photoresist is a suspension of polymers, sensitizers, and additives in a solvent. Different resists will contain different amounts of these solids. The amount is referred to as the solids content of the resist and is expressed as the weight percent in the resist. Solids contents are in the 20 to 40 percent range.[3]

Viscosity

Viscosity is the quantitative measure of liquid flow. High-viscosity liquids, such as tractor oils, flow in a sluggish manner. Low-viscosity liq-

Parameter	Negative	Positive
Aspect Ratio (Resolution)		Higher
Adhesion	Better	
Exposure Speed	Faster	
Pinhole Count		Lower
Step Coverage		Better
Cost		Higher
Developers	Organic Solvents	Aqueous
Strippers		
Oxide Steps	Acid	Acid
Metal Steps	Chlorinated Solvent Compounds	Simple Solvents

Figure 8.21 Comparison of negative and positive results.

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uids, such as water, flow more readily. In both cases, the mechanism of flow is the same. The molecules in the liquid roll over each other as the liquid is being poured. As the molecules roll about, there exists an attraction between them that acts as an internal friction. Viscosity is the measurement of that friction.

Viscosity is measured by several techniques. Most photoresist manufacturers measure viscosity with a rotating vane in the resist. The higher the viscosity, the more force required to move the vane through the liquid at a constant speed. The rotating-vane apparatus illustrates the force-related character of viscosity.

The unit of viscosity is the *centipoise* (one-hundredth of a poise). It is named after the French scientist Poisseulle, who investigated the viscous flow of liquids. One poise is equal to one dyne second per centimeter. The viscosity unit of centipoise is more correctly named the absolute viscosity.

Another unit, called the *kinematic viscosity,* is the centistoke. This value is calculated from the absolute viscosity (centipoise) divided by the density of the resist. Viscosity varies with temperature; therefore, its specified value is stated at a particular temperature, usually 25°C. Viscosity is a major parameter determining the resist thickness during the spin process. Viscosity is closely related to the solids content. The higher the solids content, the higher the viscosity.

Surface tension

The surface tension of a resist also influences the outcome at spin. Surface tension is a measure of the attractive forces in the surface of the liquid (Fig. 8.22). Liquids with high surface tension flow less readily on a flat surface. It is the surface tension that draws a liquid into a spherical shape on a surface or in a tube.

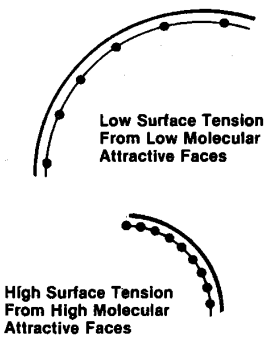


Figure 8.22 Surface tension.

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Index of refraction

The optical properties of the resist play a role in the exposure mechanism. One property is *refraction* or the bending of light as it passes through a transparent or semitransparent medium. Refraction is the same phenomenon that makes an object in a pool of water appear at a different location. This comes about as the light ray is slowed up by the material. The *index of refraction* is a measurement of the speed of light in a material compared to its speed in air, as shown in Fig. 8.23. It is calculated as the ratio of the reflecting angle to the impinging angle. For photoresists, the index of refraction is close to that of glass, approximately 1.45.

Storage and control of photoresists

Photoresists are delicate high-technology mixtures. Great care and precision go into their manufacture. Once a photomasking process is developed, its continuing success depends on the day-in, day-out control of the process parameters and a consistent photoresist product. Delivered batch-to-batch consistency is a responsibility of the manufacturer. Maintaining that consistency is the responsibility of the user. Several properties of resists dictate the required storage and control conditions.

Light and heat sensitivity

Both light and heat can activate the sensitive mechanisms in the resist intended to be activated in the closely controlled masking process

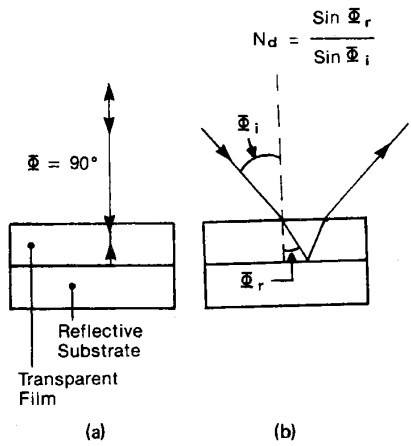


Figure 8.23 Index of refraction. (*a*) 90° incident light and (*b*) angled light refracted in the transparent film.

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steps. It is imperative that the resist be protected during storage and handling to prevent unwanted reactions that would interfere with the process results. This is the reason why masking areas use yellow light. It is also the reason why resist bottles are brown. The colored glass protects the resist from stray light. Proper transportation and storage of resist require temperature control within the limits specified by the manufacturer.

Viscosity sensitivity

Viscosity control is essential for good film thickness control. To maintain the photoresist's viscosity, resist bottles must remain capped prior to use. Opened bottles will allow evaporation of the solvent, which results in a higher solids content, which in turn results in a higher viscosity. If photoresist is dispensed from plastic tubing, the material should be tested to ensure that the resist is not leaching plasticizers out of the material. The plasticizers will increase the viscosity of the resist.

Resist is also available in sealed vacuum pouches. The resist is protected during shipping and storage. During use, the pouch continues to collapse as the resist is dispensed, preventing air from reaching the resist surface.

Shelf life

A container of photoresist comes with a recommended shelf life. The problem again has to do with the self-polymerization or photosolubilization of the resist. In time, changes to the polymer will take place, altering the resist performance when it reaches the production line.

Cleanliness

Needless to say, any and all equipment used to dispense photoresist must be maintained in the cleanest condition possible. Besides the effects of particular contamination from the system, the resist tubing must be cleaned regularly because of the possible buildup of dried photoresist. Cleaning agents should be checked for their compatibility with the resist. For example, TCE should not be used with negative resist, because it can cause bubbles in the resist.

Photomasking Processes

In the following sections, each of the ten basic masking steps is examined. Presented is the purpose of the step, technical considerations and challenges, options, and process control methods.

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Surface Preparation

Throughout this text, various analogies will be used to aid the reader in understanding the complicated processes. A good analogy to the photomasking process is painting. Even the amateur painter soon learns that, to end up with a smooth film of paint that adheres well, the surface must be dry and clean. The same is true in photomasking technology. Ensuring that the resist will stick to the wafer surface requires surface preparation. This step is performed in three stages: particle removal, dehydration, and priming.

Particle removal

The wafers coming to the photomasking area almost always come in a clean condition from another process such as oxidation, doping, or CVD. However, during storage, loading, and unloading into carriers, they may pick up some particulate contamination that must be removed from the surface. Depending on the level of contamination and/or the process requirements, several particulate removal techniques may be used (Fig. 8.24). In extreme cases, the wafers may be put through a wet chemical cleaning similar to the preoxidation cleaning processes, including an acid cleaning, water rinsing, and drying. The particular acid used must be compatible with the top layer on the wafer surface. Particle removal methods are the same as described in Chapter 7: manual blow-off, mechanical scrubbers, and/or high-pressure water spray.

Dehydration baking

It has been mentioned that the wafer surface has to be dry to promote adhesion. A dry surface is called *hydrophobic,* a chemical condition. Liquids form into small droplets on a hydrophobic surface, such as water beads on a newly waxed car. A hydrophobic surface is conducive to good photoresist adhesion (Fig. 8.25). Wafers coming to the masking operation usually have a hydrophobic surface.

Unfortunately, when the wafer is exposed to moisture, either from the air or from post-cleaning rinses, the surface condition changes to a *hydrophilic* one. This condition is evidenced by a liquid on the surface spreading out in a wide puddle, such as water on a nonwaxed car sur-

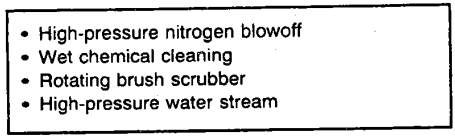


Figure 8.24 Prespin wafer cleaning methods.

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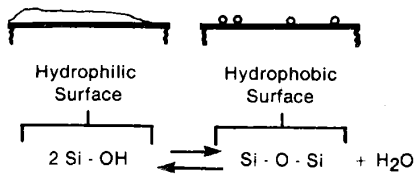


Figure 8.25 Hydrophilic versus hydrophobic surfaces.

face. A hydrophilic surface is also said to be *hydrated.* Resist does not adhere very well to hydrated surfaces (Fig. 8.25).

Two important ways to maintain a hydrophobic surface are to keep the room humidity below 50 percent and to coat the wafers with photoresist as quickly as possible after being received from a previous process. Storage of the wafers in desiccators purged with dry, filtered nitrogen or in the dry mini-environment of a SMIF box (see Chapter 4). Additional steps may be taken to establish a wafer surface with acceptable adhesion properties. These steps include a dehydration bake and priming with a chemical.

A heating operation may be used to reset the wafer surface to a dehydrated condition. Dehydration bakes take place in three temperature ranges to address three different dehydration mechanisms. In the range of 150 to 200°C (low temperature), surface water is evaporated. At 400°C (medium temperature), water molecules loosely attached to the surface will leave. At temperatures above 750°C (high temperature), the surface is chemically restored to a hydrated condition.

In most masking processes, only low-temperature dehydration bake temperatures are used. This is because this temperature range is easily obtainable with hot plates and chest-type convection and vacuum ovens. Another advantage of low-temperature dehydration is that the wafers do not have to wait for a cool-down before the spin process. Systems to perform this step can easily be integrated into a spin-bake system, making them dehydration-spin-bake systems. An explanation of these heating systems is provided in "Soft Bake," p. 227.

High-temperature dehydration bakes are rare. One reason is that reaching a temperature of 750°C usually requires the use of a tube furnace, and tube furnaces are large and cannot be integrated into the spin-bake processes. A second reason is the temperature level itself. At 750°C, doped junctions in the wafer can move (which is undesirable), and mobile ionic contaminants on the surface can move into the wafer causing reliability and performance problems.

Wafer priming

In addition to dehydration baking, the wafers may go through a chemical priming step to ensure good adhesion of the resist. In painting,

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primers are a subcoat selected for their ability to adhere to the surface and provide a good surface to which the paint will stick. In semiconductor photomasking, the primer effect is similar. The primer chemically ties up molecular water on the wafer surface, thereby increasing its adhesion property.[4]

A number of chemicals provide priming capabilities, but one, hexamethyldisilazane (HMDS), is in universal use. The use of HMDS is described in U.S. Patent 3,549,368 by R. H. Collins and F. T. Deverse (1970) of IBM. The HMDS is mixed with xylene in solutions of from 10 to 100 percent. The exact mixture is determined by the particular surfaces and environmental factors in the cleanroom. Unlike a painting primer, a thickness of only several molecules is sufficient to provide the necessary adhesion promotion.

Spin priming

In most photomasking areas, liquid primers are applied to the wafer while it is on the resist spinner chuck (Fig. 8.26). The dispensing of the HMDS can be manual from a syringe or automatic. Automatic spinners (see next section) have a separate system to dispense HMDS onto the wafer surface just prior to the application of the resist. After the spinner dispenses the primer onto the rotating wafer, the chuck is ramped to a higher speed to dry the HMDS layer. A major production advantage of spin priming is that it takes place in-line with the spin step.

Vapor priming

Both immersion and spin priming require the direct contact of the HMDS liquid with the wafer surface. Whenever a liquid is in contact with the wafer, there is the danger of contamination from the liquid. Another consideration is that the HMDS must be dry before the resist is applied. Wet HMDS can dissolve the bottom layer of the resist and interfere with the exposure, development, and etching. Lastly, HMDS

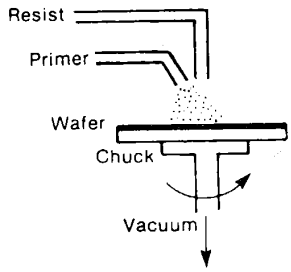


Figure 8.26 Spin dispense of primer.

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is relatively expensive, and in spin priming, an excess of HMDS is sprayed on the wafer to ensure adequate coverage. The excess is thrown off the wafer and discarded.

The preceding considerations are overcome by vapor priming techniques. Vapor priming is practiced in three forms. Two are performed at atmospheric pressure and one in a vacuum (Fig. 8.27). One atmospheric system employs a bubbler chamber connected to a desiccator-type chamber. Nitrogen is bubbled through the HMDS and carried into the chamber, where it coats the wafers. Another method employs a vapor degreaser with a reserve of liquid HMDS. The HMDS is heated to the vapor point and the wafers are suspended in the vapors for coating.

The third vapor technique is vacuum vapor priming, which uses a sealed flask of HMDS connected to a vacuum oven or single-wafer chamber. The wafers are first heated in the oven in a nitrogen atmosphere. After a temperature of about 150°C is reached, the atmosphere is switched to a vacuum. Once the vacuum level is reached, a valve is opened, and HMDS vapors are drawn into the chamber by the low pressure. Within the chamber, the wafers become completely coated as the vapors fill the entire chamber. This method has shown good adhesion longevity, even in the presence of high humidity.

Vacuum vapor priming offers the additional advantage of a combined dehydration bake and prime step and a significant reduction in HMDS usage. Vacuum vapor priming practiced in a chest-type oven adds an additional step to the process. Many automatic spinner systems incorporate in-line vacuum vapor primers.

Photoresist Application (Spinning)

The purpose of the photoresist application step is the establishment of a thin, uniform, defect-free film of photoresist on the wafer surface.

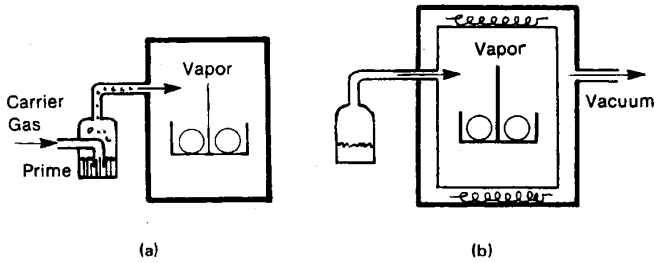


Figure 8.27 Vapor prime methods. (*a*) Atmospheric and (*b*) vacuum bake-vapor prime.

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These goals are easy to state, but they require sophisticated equipment and stringent controls to achieve. A typical resist layer varies from 0.5 to 1.5 μm in thickness and has to have a uniformity of only ±0.01 μm (100 Å). This variation is 1 percent of a 1.0-μm thickness.

The usual methods of applying thin layers of liquids to surfaces are brushing, rolling, and dipping. None of these methods is adequate to achieve the quality resist film necessary for photomasking. The method used is spinning, which was briefly described in the section on priming. Spinners are built in manual, semiautomatic, and automatic designs. The systems differ in the degree of automation and are described in the following text. However, the deposit of the film on the wafer is common to each of the systems.

Spin processes are designed to prevent or minimize the buildup of a bead of resist around the outer edge of the wafer. Called an *edge bead,* the buildup causes image distortions during the exposure and etch processes.

The static dispense spin process

Application of the resist occurs immediately after the priming process. The wafer is placed on a vacuum chuck and several cubic centimeters (cm^3) of the photoresist is deposited in the center of the wafer (Fig. 8.28) and allowed to spread out into a puddle. The puddle is allowed to spread until it covers the majority of the wafer surface. The amount of resist deposited in the puddle is critical only in the extremes. Too small an amount will result in incomplete resist coverage, and too much will cause a buildup of a resist rim or result in resist on the back of the wafer (Fig. 8.29).

When the puddle reaches its specified diameter, the chuck is rapidly accelerated to a predetermined speed. During the acceleration, centrifugal forces spread the resist to the wafer edge and throw off excess resist, leaving a thin uniform layer on the wafer. The high-speed spin

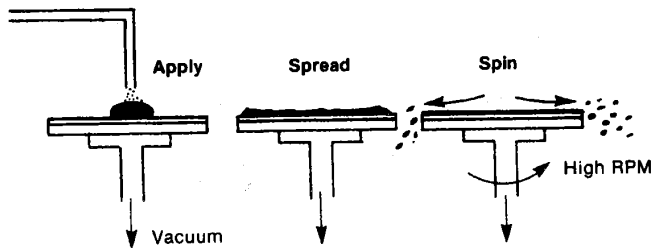


Figure 8.28 Static spin process.

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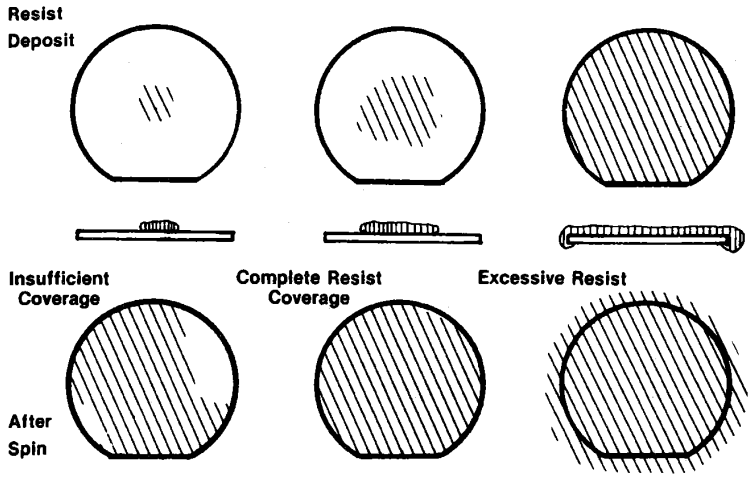


Figure 8.29 Example of resist coverage.

continues for some time after the resist is spread to allow drying of the resist.

The final thickness of the film is established as the result of the resist viscosity, the spin speed, the surface tension, and the drying characteristics of the resist. In practice, surface tension and the drying characteristics are properties of the resist, and the viscosity-spin speed relationship is determined from curves supplied by the resist manufacturer or established for the particular spin system used (Fig. 8.30).

Although spin speed is specified to control resist thickness, it is actually the acceleration rate that establishes the final resist thickness. The acceleration characteristic of the spinner must be specified and maintained as a constant in the spin process.

Dynamic dispense

The need for uniform resist films on larger-diameter wafers led to the development of the dynamic spin dispensing technique in the 1970s (Fig. 8.31). For this technique, the wafer is rotated at a low speed of approximately 500 rpm. While the wafer is rotating, the resist is dispensed onto the surface. The action of the rotation assists in the initial spreading of the resist. Less resist is used, and a more uniform layer is achieved. After spreading of the resist, the spinner is accelerated to a high speed to complete the spread and thin the resist into a uniform film.

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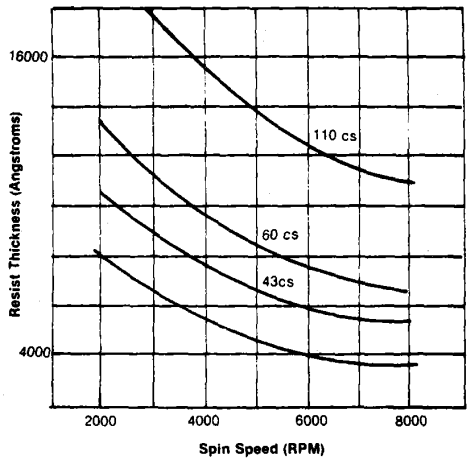


Figure 8.30 Resist speed thickness versus spin speed. *(Courtesy of KTI Chemicals.)*

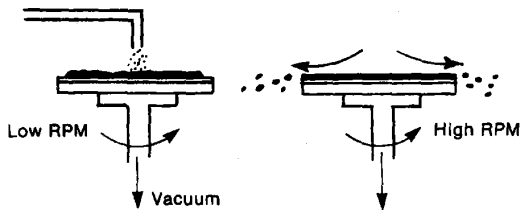


Figure 8.31 Dynamic spin dispense.

Moving-arm dispensing

An improvement on the dynamic dispense technique is the addition of a moving-arm resist dispenser (Fig. 8.32). The arm moves in a slow motion from the center of the wafer toward its edge. This action creates more uniform initial and final layers. A moving-arm dispenser also saves resist material, especially for larger-diameter wafers.

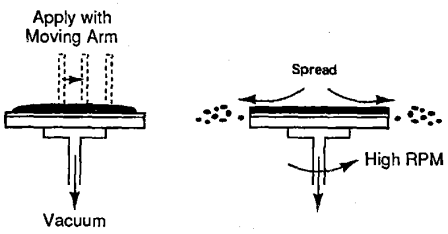


Figure 8.32 Moving-arm dispensing.

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Manual spinners

A manual spinner is a simple machine consisting of from one to four vacuum chucks (called *heads*), a motor, a tachometer, and a connection for a vacuum source. Each head is surrounded by a catch cup, which serves to collect the excess resist and direct it to a collection vessel. The catch cup also prevents "balls" of resist thrown off the wafers during the acceleration from landing on adjacent wafers. The process starts with the removal of particles from the wafer with a filtered nitrogen gun. The wafer(s) are mounted on the head with tweezers or a vacuum wand, and the chuck vacuum is turned on. Next, the HMDS is dispensed onto the surface from a syringe or squeeze bottle, and the wafer is spun and dried. Finally, the resist puddle is dispensed from another syringe or squeeze bottle. Most spin processes performed on manual spinners use the static dispense method.

Edge bead removal

A consequence of the high-speed spin can be a buildup of resist around the edge of the wafer, called an *edge bead.* It is removed by a solvent spray directed on the front and back of the wafer, near the edge.

Automatic spinners

A semiautomatic spinner adds automation to the resist blow-off, resist dispense, and spinning cycles. The nitrogen blow-off is accomplished from a separate tube over the vacuum chuck that is connected to a pressurized nitrogen source (Fig. 8.33). Also in the dispense chamber are a primer resist tube and a resist dispense tube. The resist tube is fed resist from either a nitrogen pressurized vessel or through a diaphragm-type pump. In general, the industry has moved away from pressurized, resist dispense systems because of problems that arise from the absorption of nitrogen into the resist. The nitrogen comes out of the resist after the dispense cycle, causing voids in the film. Diaphragm pumps eliminate this problem.

Automatic resist dispensers have a negative-pressure capability that automatically draws the resist back up into the dispenser tube after each dispensing operation. This *drawback* (or *suckback*) minimizes the exposed surface of the resist in the tube from drying into a hard ball that can be deposited on the wafer (Fig. 8.34). In fully automatic systems, all of the events of the spin process are controlled by microprocessors. The systems have mechanisms to extract the wafers from the carriers, place them on the chucks, perform the priming step, dispense the photoresist, remove the edge bead, perform a soft bake, and place the wafers back in their carriers. The standard system configu-

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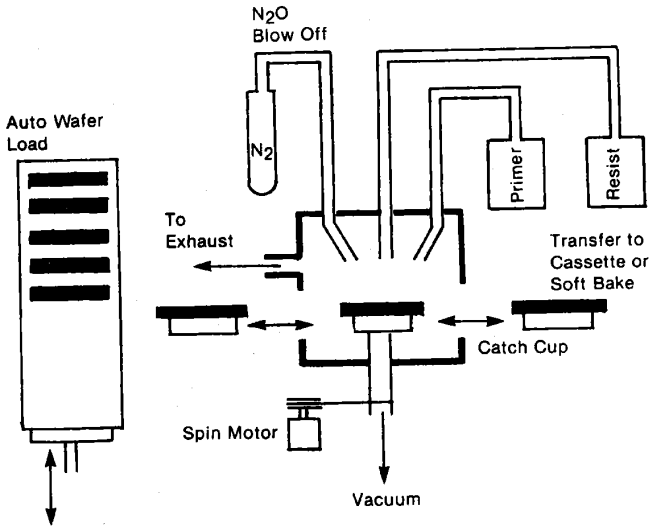


Figure 8.33 Automated spinner diagram.

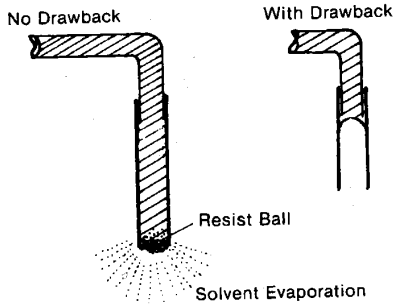


Figure 8.34 Automatic dispense with drawback.

ration is in a line, referred to as a *track*. Production-level spinners will have from two to four side-by-side tracks.

Backside coating

In some device processes, it is required that the oxide on the back of the wafer remain in place through the masking process. One way this is accomplished is by coating the back of the wafer with photoresist. The requirement for this backside coating is simply a thick enough layer to survive the etch process.

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Soft Bake

The soft bake step is a heating operation with the purpose of evaporating a portion of the solvents in the photoresist. After the bake, the resist film is still "soft," as opposed to being baked to a varnish-like finish. The solvents are evaporated for two reasons. Remember that the principal role of the solvents is to allow the application of the resist in a thin layer on the wafer. After that role is fulfilled, the presence of the solvent can interfere with the rest of the processing. The first interference occurs during the exposure step. The solvent(s) in the resist can absorb exposing radiation, thus interfering with the proper chemical change in the photosensitive polymers. The second problem is with the resist adhesion. Using the painting analogy, we know that complete drying (evaporation of the solvent) is necessary for good adhesion.

The principle soft-bake parameters are time and temperature. Two major goals of the patterning process are correct image definition and the adhesion of the resist to the wafer during the etch step. Both of these goals are influenced by soft bake. In the extreme, an underbaking will result in incomplete image formation at exposure and excessive lifting (poor adhesion) at the etch step. Overbaking will cause the polymers in the resist to polymerize and not react to exposing radiation.

Temperature and time ranges for the soft bake are provided by the resist manufacturer and are fine-tuned by the masking engineer. Negative photoresists have to be baked in a nitrogen atmosphere, whereas positive resists can be baked in air. A number of different methods are used to accomplish the soft-bake step, and various pieces of equipment incorporating all three heat transfer methods are used.

The three methods of heat transfer are conduction, convection, and radiation. Conduction is the transfer of heat by direct physical contact of the object with a heated surface. Hot plates heat by conduction. In the conduction process, the vibrating atoms of the hotter surface cause the object atoms to vibrate also. As they vibrate and collide, the atoms become hotter.

Some dehydration baking is in convection ovens. Systems using convection heating include home forced-air furnaces, hair dryers, air- and nitrogen-fed ovens, and oxidation furnaces. In these systems, a unit heats the gas and a blower or pressure pushes the gas to a space where it, in turn, heats the object.

The third method is radiation. The term *radiation* describes the travel of electromagnetic energy waves through space. Radiation waves travel in vacuums as well as through gases. The sun transfers heat to the Earth by radiation. Heating lamps also transfer heat by ra-

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diation. Radiation is the heating method used by RTP systems. When the radiation strikes an object, the energy carried by the wave is transferred directly to the atoms of the object.

Convection ovens

The mainstay baking oven for nonautomated fabrication lines is the convection oven (Fig. 8.35). It is a stainless steel chamber in an insulated enclosure. Either nitrogen or air is supplied by ducts surrounding the chamber and passed through a heater before being directed into the chamber. The inside of the chamber is fitted with racks for the wafer carriers. The carriers stay inside the oven for a predetermined time while the heated gas brings them up to temperature. Convection ovens used for VLSI applications have proportional band controllers and HEPA filters to maintain a clean baking environment.

There are several drawbacks to convection ovens for soft baking. One is batch-to-batch temperature variation, which arises from the amount of time the door is open for loading, the size of the load, and the variable time for all parts of the oven to reach a constant temperature. A process problem associated with convection heating is the tendency of the top layer of resist to "crust," trapping solvents in the resist (Fig. 8.36).

Manual hot plates

In manual and laboratory operations, a simple hot plate can be used for the soft bake. The wafers are placed on an aluminum holder, which

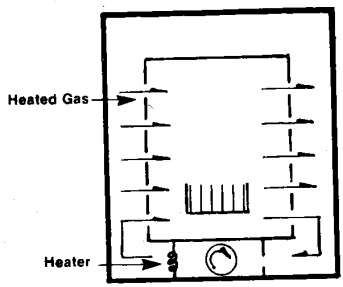


Figure 8.35 Convection oven.

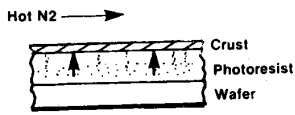


Figure 8.36 Crusting effect of ovens.

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has a dial thermometer set in a hole drilled into it. The wafers are put on the holder, which is set on the hot plate (Fig. 8.37). The operator monitors the rise in temperature on the thermometer and removes the holder when the proper temperature is reached. With a well controlled hot plate, an effective soft bake can be achieved. A process advantage of hot-plate heating is that the bottom of the wafer is heated first. This allows the solvents to escape through the top surface and also minimizes "crusting" of the surface. A hot-plate process is operator dependent and has low productivity.

In-line, single-wafer hot plates

The backside advantage of hot-plate heating can be gained in track systems when a single-wafer hot plate is built into the system. Wafers leaving the spinner are positioned on the hot plate and clamped to it with a vacuum. The wafer and resist are heated for a predetermined time, the vacuum released, and the wafer transferred to a carrier. These in-line systems are connected to the facility exhaust system for the removal of the solvent vapors.

Moving-belt hot plates

A constraint on the productivity of single-wafer hot plates in an integrated system is the total time of the spin step. A typical spin time is

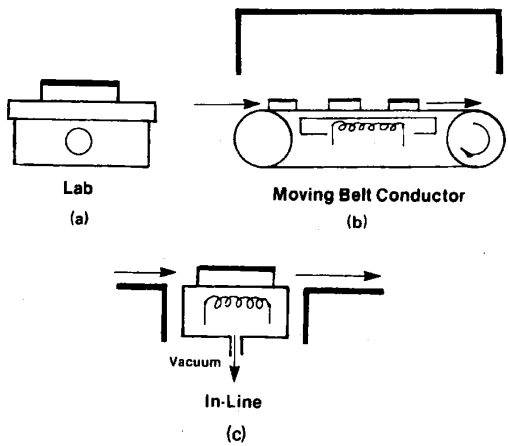


Figure 8.37 (*a*) Manual hot plate, (*b*) in-line continuous hot plate, and (*c*) in-line single-wafer hot plate.

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25 to 40 sec, which means the soft bake would have to be completed in that amount of time to keep the wafers moving in a continuous flow. For some resists and for some processes, this is too short a time. A way around the problem is a moving-belt hot plate. The wafers are placed on a heated, moving steel belt, and the temperature and belt speed are set to meet the soft bake requirements and process the wafers in a continuous flow.

Moving-belt infrared ovens

The desire for fast, uniform, and noncrusting soft bake methods led to the development of infrared (IR) radiation sources (Fig. 8.38). Infrared baking is much faster than conduction baking and heats from the "inside out." Inside-out baking is the principle of conduction hot plate baking. The infrared waves pass through the resist layer without heating it, much like sunlight will pass through a window without heating it. The wafer, however, absorbs the energy, gets hot, and in turn heats the resist layer from the bottom.

Microwave baking

Microwaves as a soft bake heating source have the advantage of infrared heating but at a much faster rate because of the higher energy carried in a microwave. Soft-bake temperatures can be well under 1 min. This brief time lends itself to on-chuck soft baking. Immediately after spinning, a microwave source is directed at the wafer, completing the soft bake (Fig. 8.39).

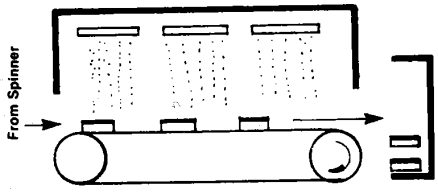


Figure 8.38 Moving-belt infrared (IR) heating.

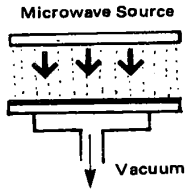


Figure 8.39 Microwave heating.

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Vacuum baking

Vacuum ovens offer several advantages for a number of process steps. A vacuum oven is configured similarly to a convection oven, but is fitted to a vacuum source. Vacuum is particularly efficient for evaporation processes, because the reduced pressure aids the evaporation of the solvents, reducing the reliance on the temperature. However, for soft baking, the wafers must be heated to a uniform temperature. A problem arises because heating in a vacuum oven is by radiation from the heated chamber walls to the wafers. This heat transfer method is sometimes called *line-of-sight* because, for uniformity, each wafer must have a clear line of sight to the heat source. In a chest-type vacuum oven packed with carriers of vertically held wafers, this condition cannot be met. The result is poor temperature uniformity in most vacuum ovens.

The benefits of vacuum and uniform hot-plate heating can be achieved with in-line, single-wafer systems. Figure 8.40 is a table summarizing the different soft bake methods.

Alignment and Exposure

Alignment and exposure (A&E) is, as the name implies, is one of the basic ten patterning steps, with two separate actions. The first part of the A&E step is the positioning or alignment of the required image on the correct location on the wafer surface. The second part is the encoding of the image in the photoresist layer from an exposing light or other radiation source. Correct alignment of the image patterns and establishment of the precise image dimensions in the resist are absolute requirements for the functioning of the devices and circuits. Furthermore, the wafers spend 60 percent of the process time in the lithography area.

Consider the challenge of building a typical ULSI megabit DRAM circuit. The SIA ITRS projects that by 2007 the functions in this device will be 17 Gb, in a chip size of 568 mm^2. The individual parts of the devices will have feature sizes in the submicron range and have to "fit" or overlay within or next to each other within tolerances of one-third the nominal feature size. This tolerance has to be maintained as each of the level patterns is exposed on the wafer. The SIA *International Technology Roadmap for Semiconductors* projects that, by 2007, advanced ICs will require 24 to 27 patterning steps. The allowable variation in wafer placement must be maintained over all of the pattern alignments.

Aligner system performance capabilities

An aligner system is composed of two major subsystems. One correctly positions the pattern(s) on the wafer surface. The different aligner

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Method	Bake Time Min.	Temperature Control	Productivity Type	Rate Waf/Hr.	Queuing
Hot Plate	5-15	Good	single to small batch	60	Yes
Convection Oven	30	Average - Good	Batch	400	Yes
Vacuum Oven	30	Poor - Average	Batch	200	Yes
I.R. Moving Belt	5-7	Poor - Average	Single	90	No
Conductive Moving Belt	5-7	Average	Single	90	No
Microwave	0.25	Poor Average	Single	60	No

Figure 8.40 Soft-bake chart.

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types have different alignment subsystems, which are explained in the equipment sections. The second part is the exposure subsystem. This subsystem includes an exposure source and a mechanism for directing the exposing radiation rays to the wafer surface.

Aligners are selected and compared by several criteria (Fig. 8.41) that relate to their ability to produce the required images in a consistent and productive manner. Perhaps the most important parameter is the *resolution capability,* or the ability of the machine to produce a particular size image. The higher the resolution capability, the better the machine. In addition to the resolution of the required image size, the aligner must be capable of placing the images in their correct position relative to each other. This performance parameter is called the *registration capability* of the aligner. These two factors must be performed over the entire wafer, a factor called *dimensional control.* The final performance factor is cost of ownership, which includes initial purchase cost, *wafer throughput* (the time required to load, align, expose, and unload the wafer), maintenance cost, and the uptime of the machine. These factors are discussed in Chapter 15.

Alignment and exposure systems

Up to the mid-1970s, the photoresist engineer had the choice of only two A&E systems: contact and proximity aligners. Today, the choice has expanded to include both optical and nonoptical aligners (Fig. 8.42), such as projection and steppers. Optical aligners use an ultraviolet light source, whereas nonoptical systems use exposure sources from other parts of the electromagnetic spectrum. The systems in use today were developed to keep pace with the reduction of feature size, increased circuit density, and required defect reductions of the ULSI era.

Exposure sources

While aligners are very sophisticated machines, they operate on several basic optical principles. Consider producing a shadow image of a

Alignment Selection Criteria
• Resolution Capability/ Limit
• Alignment Accuracy
• Contamination Level
• Reliability
• Productivity
• Overall cost of ownership (COO)

Figure 8.41 Aligner selection criteria.

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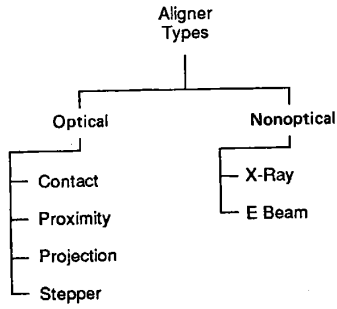


Figure 8.42 Table of aligner types.

fork on a wall by shining a flashlight through a real fork held near the wall. By semiconductor standards, the image of the fork is quite imprecise. But there are ways to improve the image. One way would be to replace the flashlight with a narrower-wavelength light. The white light that comes from a flashlight contains many different wavelengths (colors), all mixed. At the edge of the fork, a phenomenon called *diffraction* takes place. Diffraction is the bending of the light rays at an opaque edge (or going through a narrow slit). The amount of bending depends on the wavelength, and, with many wavelengths (white light), there are many rays scattering from the edge and fuzzing up the image. Using a shorter-wavelength light, or a single-wavelength source, minimizes the diffraction. Another way to improve the image is to get all of the rays traveling along the same path. In normal white light, the rays are coming from the light bulb in many directions and leave the edge of the fork with many directions, again fuzzing the image. With mirrors and lenses, the light rays can be *collimated* into a band of parallel rays, thus improving image quality. The sharpness of the image and its dimensions are also influenced by the distance of the light behind the fork and the distance of the fork to the wall. Closing up both of these distances sharpens the image. These techniques (narrower or single wavelength exposure sources, collimated light, and strict control of the distances) are all used in aligners to produce the required images.

Exposure sources are chosen to create the required image size in conjunction with a specific photoresist (see "Photoresist exposure speed, sensitivity, and exposure source," p. 208). The workhorse exposure source has been the high-pressure mercury lamp. It produces light in the ultraviolet (UV) range. The reduction of feature size has driven the development of improvements to the basic lamp and photoresists. To achieve greater definition, resists are tailored to respond to only narrow bands (lines) in the mercury lamp spectrum. This need also has resulted in the development of lamps and resists that operate

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in the shorter wavelengths of the spectrum. This region of the spectrum is known as the *deep ultraviolet* or DUV.

Other approaches to lower wavelength and higher-energy exposure sources are excimer lasers, X-rays, and electron beams. A more detailed discussion of the various exposure sources is provided in Chapter 10.

Alignment criteria

The first mask is aligned by positioning the y axis of the mask at a 90° angle to the major wafer flat on the wafer (Fig. 8.43). Subsequent masks are aligned to a previously patterned mask with the use of alignment marks (also called *targets*). These are special patterns (Fig. 8.44) located in an easily found position on the edge of each chip pattern or in the separation lines surrounding each chip on the wafer.

Alignment is accomplished by the operator positioning a mark on the mask to a corresponding mark in the wafer pattern. For automatic systems (see "Steppers," p. 238), the alignment marks serve the same purpose. Alignment marks become a permanent part of the chip surface through the etching process. They are then in place for the alignment of the next layer.

Alignment errors, called *misalignment,* fall into several categories (Fig. 8.45). A common one is a simple misplacement in the x-y directions. Another common misalignment is rotational, where one side of

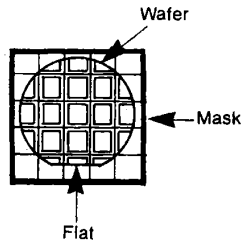


Figure 8.43 Diffracting reduction of image in resist.

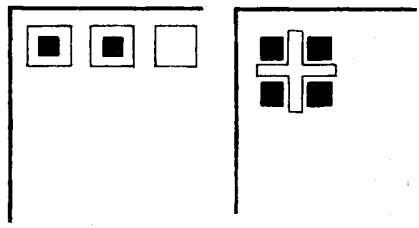


Figure 8.44 Types of alignment marks.

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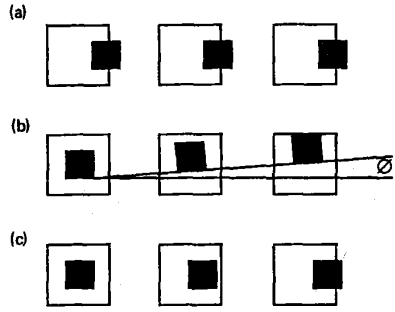


Figure 8.45 Misalignment types. (*a*) *x* direction, (*b*) rotational, and (*c*) run-out.

the wafer is aligned, but the patterns become increasingly misaligned across the wafer. A third rotational misalignment comes about when the die pattern is rotated on the mask or reticle.

Other misalignment problems associated with masks and stepper aligners are run-out and run-in. These problems arise when the chip patterns are not formed on the mask on constant centers or are placed on the chip off center. The result is that only a portion of the mask chip patterns can be properly aligned to the wafer patterns. The pattern becomes progressively misaligned across the wafer.

A rule of thumb is that circuits with micron or submicron feature sizes must meet registration tolerances of one-third the minimum feature. An *overlay budget* is calculated for the total circuit. It is the allowable accumulated alignment error for the entire mask set (see Fig. 8.2). For a 0.35-μm product, the allowable overlay budget is about 0.1 μm.[5]

Aligner types

Contact aligners. Until the mid-1970s, the contact aligner was the workhorse aligner of the semiconductor industry. The alignment part of the system uses a full wafer-size photomask positioned over a vacuum wafer chuck. The wafer is mounted on the chuck and viewed through a split-field objective microscope (Fig. 8.46). The microscope presents the operator with a simultaneous view of each side of the mask and wafer. The chuck is moved left, right, and/or rotated (*x*, *y*, and *z* movement) by manual controls until the wafer is aligned to the mask pattern.

Once the mask and wafer are aligned properly, the wafer chuck moves up on a piston, pushing the wafer into contact with the mask. Next, the collimated ultraviolet rays coming from a reflection and lens system pass through the mask and into the photoresist.

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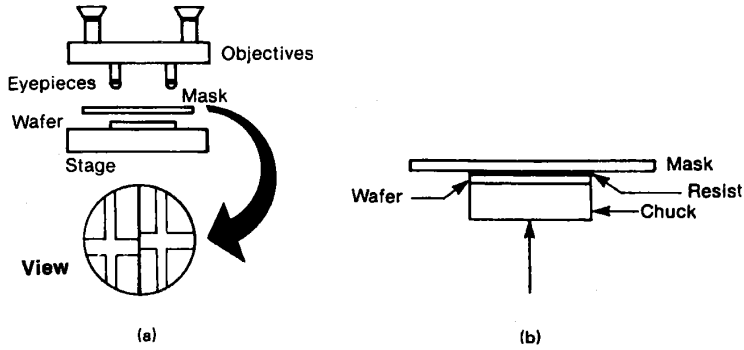


Figure 8.46 Contact aligner system. (*a*) Alignment stage and (*b*) contact stage.

Contact aligners are used in production for discrete devices and circuits with SSI and MSI densities and feature sizes of approximately 5 μm and above. They also are used for flat panel displays, infrared sensors, device packages, and multichip modules (MCMs).[6] A contact aligner is capable of submicron imaging with the proper resist and a well tuned process. Its replacement by other systems is more related to yield losses associated from the contact of the mask and wafer.

Contact can damage the soft resist layer, the mask, or both. Dirt adhering to the clear portions of the mask blocks light during exposure. Epitaxial layer spikes on bipolar wafers can degrade the mask. Mask damage is so prevalent that masks have to be removed and discarded or cleaned every 15 to 25 exposures. Dirt between the mask and wafer will cause resolution problems in the immediate area of the piece of dirt. Alignment of larger diameter wafers presents a light uniformity problem that causes image size variations and alignment problems.

Proximity aligners. Proximity aligners were a natural evolution of contact aligners. The systems are essentially contact aligners but with mechanisms that hold the wafer either in near or soft contact with the mask. Sometimes proximity aligners are called *soft-contact machines.*

The performance of a proximity aligner is a trade-off between resolution capability and defect density. With the wafer in soft contact with the mask, there is always some scattering of the light, which fuzzes the definition of the image in the resist. On the other hand, the soft contact also greatly reduces the number of defects associated with mask and resist damage. Even with the improved defect density, proximity aligners do not find much use in VLSI photomasking processes.

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Scanning projection aligners. The end of contact aligners was foreseen for years, and development work was ongoing in the search for an alternative. The search centered on the concept of projecting (Fig. 8.47) the mask image onto the wafer surface, much as a slide (the mask) is projected onto a screen (the wafer). While simple in concept, the technique requires an excellent optical system to expose an entire wafer surface in one exposure. The problem was solved with the introduction of the Perkin Elmer scanning projection aligner. This system avoided the problems of a full mask projection exposure in favor of a scanning technique that used a mirror system with a slit blocking part of the light coming from the light source. The slit allows a more uniform portion of the light to shine on the mirror system, which is in turn projected onto the wafer (Fig. 8.48). Since the size of the slit is smaller than the wafer, the light beam is scanned across the wafer. With this system, a new parameter, scan speed, became a parameter requiring control. They are called 1:1 aligners, since the image dimensions on the mask are the same size as the intended image dimensions on the wafer surface.

Steppers. Scanning projection aligners were a great leap forward over contact aligners for production work, but they still had some limitations, such as alignment and overlay (registration) problems associated with full-size masks, image distortion, and mask-induced defects from dust and glass damage.

By the mid-1970s there were thoughts of stepping images (Fig. 8.49) from a reticle directly onto the wafer surface—the same technique used to make masks. A reticle, carrying the pattern of one or several

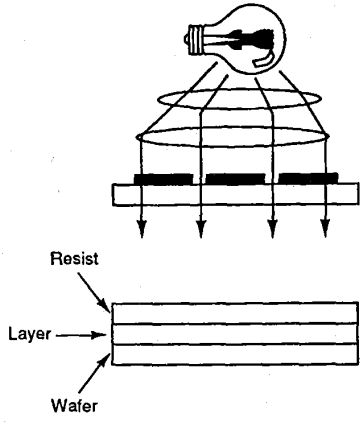


Figure 8.47 Concept of projection exposure.

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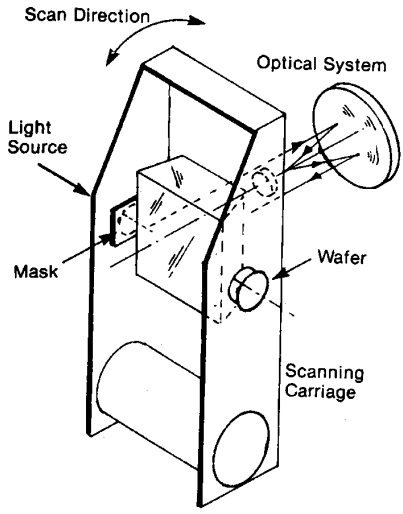


Figure 8.48 Perkin Elmer light projection system. *(Courtesy of Perkin Elmer Corp.)*

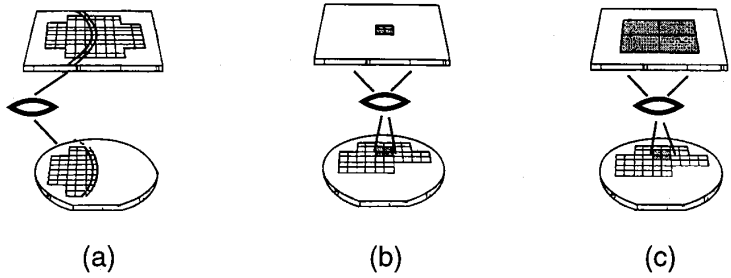


Figure 8.49 Projection imaging techniques. (*a*) Scan, (b) 1:1 step/repeat, and (*c*) reduction step/repeat.

chips, is aligned and exposed, then is *stepped* to the next site and the process *repeated*. A reticle is of a higher quality than a full-size mask so fewer defects occur. There is better overlay and alignment, because each chip is individually aligned. The procedure of stepping allows precise matching of larger-diameter wafers. Other advantages are resolution improvements, because a smaller area is being exposed each time and a lessened vulnerability to dust and dirt. Some steppers are 1:1; i.e., the image on the reticle is the same dimensions required on the wafer. Others use a reticle 5 to 10 times the final dimensions. These are called *reduction steppers*. Making an oversize reticle is eas-

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ier, and any dirt and small glass distortions are reduced out of existence during the exposure (Fig. 8.50). Generally, 5× reduction is preferred.

A 5× reticle is smaller and easier to make than a 10× one. Also, a 5× reticle projects a larger (up to 20 × 20 mm) field onto the wafer, resulting in faster wafer throughput.[7] Field size is projected in the SIA NTRS to grow beyond the 25 × 32 mm capability of 6-in reticles. Under development are 9-in reticles with the capability of 25 × 50 mm field sizes.[8]

The key to production use of steppers was automatic alignment systems. There is no way that an operator could individually align several hundred die on a wafer at a productive rate. Automatic alignment is accomplished by passing low-energy laser beams through alignment marks on the reticle and reflecting them off corresponding alignment marks on the wafer surface. The signal is analyzed, and information is fed to the *x-y-z* wafer chuck controls by a computer, which moves the wafer around until the wafer and reticle are aligned. The images are placed in the photoresist by sequentially exposing each die pattern across and down the wafer (Fig. 8.51).

An alternative to laser signal control is a vision system. These systems use a camera to capture a vision of the die and compare it to a data base. The wafer is moved until it and the mask/reticle image match the data base.

Most production steppers have UV exposure sources with G- or I-line capabilities. Steppers intended for small geometries are fitted with laser sources operating in the DUV range.[9] The maintenance of

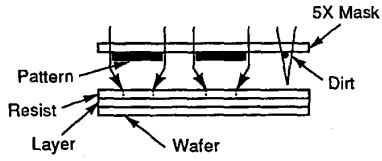


Figure 8.50 5× mask pattern transfer.

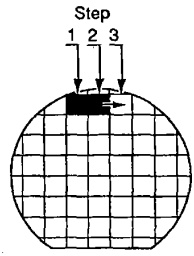


Figure 8.51 Step-and-repeat die alignment and exposure.

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the correct image size during the exposure part of the process requires tight humidity and temperature control. Most steppers are enclosed in an environmental chamber that controls these important parameters and keeps the wafers clean.

Step and scan aligners. Larger die sizes would normally require larger lens systems with larger fields of vision. Increasing the field of vision shortens the time of alignment and exposure. However, larger lenses become expensive. An alternative is a stepper with a smaller lens and the capability to scan the smaller field over the required area (see Fig. 8.52).

Post-exposure bake (PEB)

Standing waves are a problem that occurs with optical exposure and positive resists (see Chapter 10). One technique for minimizing the effect of standing waves is to bake the wafers after exposure. The bake method could be any one of the ones described earlier. The time/temperature specifications for the PEB are a function of the baking method, exposure conditions, and resist chemistry.

X-ray aligners. X-ray systems are similar to UV and DUV systems in function. However, the exposure sources are X-rays. These are high-energy beams with small wavelengths capable of patterning very small patterns. One drawback is the need for masks made of gold and other materials capable of blocking the high-energy rays. Also, the development of high-performance X-ray-capable resists has been slow. The challenge is to balance high sensitivity to X-rays while maintaining a good etch barrier.

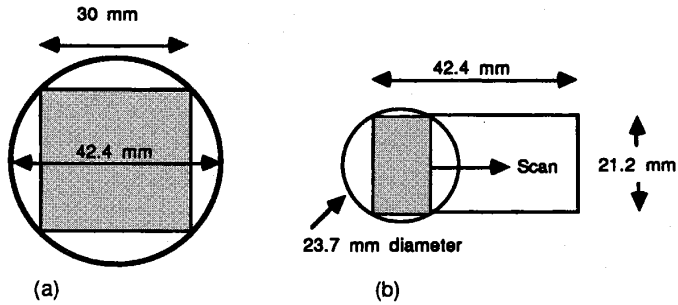


Figure 8.52 Step and scan comparison. (a) Step-and-repeat requires 42.4-mm diameter lens field for 9-cm^2 die; (b) step-and-scan for same die requires 23.7-mm lens field.

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X-ray systems are similar to other mask-using systems with the mask positioned between the source and wafer and with mechanisms for viewing and alignment.

Electron beam aligners. Electron beam lithography is a mature technology used in the production of high-quality masks and reticles. The system consists of an electron source that produces a small-diameter spot and a "blanker" capable of turning the beam on and off. The exposure must take place in a vacuum to prevent air molecules from interfering with the electron beam. The beam passes through electrostatic plates capable of directing (or steering) the beam in the *x-y* direction on the mask, reticle, or wafer. This system is functionally similar to the beam-steering mechanisms of television sets. Precise direction of the beam requires that the beam travel in a vacuum chamber in which there is the electron beam source, support mechanisms, and the substrate being exposed.

Since the pattern required generates from the computer, there is no mask. The beam is directed to specific positions on the surface by the deflection subsystem and the beam turned on where the resist is to be exposed. Larger substrates are mounted on an *x-y* stage and are moved under the beam to achieve full surface exposure. This alignment and exposure technique is called *direct writing*.

The pattern is exposed in the resist by either raster or vector scanning (Fig. 8.53). Raster scanning is the movement of the electron beam side to side and down the wafer. The computer directs the movement and activates the blanker in the regions where the resist is to be exposed. One drawback to raster scanning is the time required for the beam to scan, since it must travel over the entire surface. In vector scanning, the beam is moved directly to the regions that have to be ex-

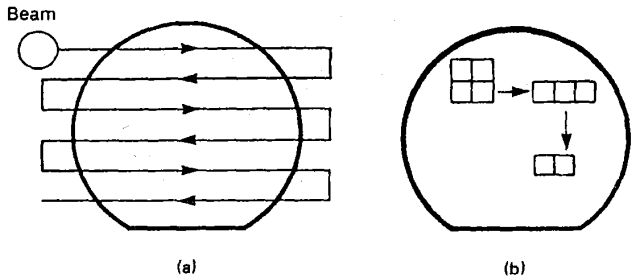


Figure 8.53 Electron beam scanning. (a) Raster scan and (b) vector scanning.

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posed. At each location, small square or rectangular shaped areas are exposed, building up the desired shape of the exposed area.

Mix and match aligners. Small-geometry imaging is expensive. Fortunately, only certain layers of a product mask set are critical enough to require the advanced imaging techniques. For advanced circuits, fully 50 percent of the layers may be noncritical.[10] The other, less critical layers can be imaged with more established techniques such as projection scanners or less expensive steppers. Mix and match will probably be a feature of fab operations that use X-ray or e-beam technologies.

Advanced Lithography

The industry is careening along Moore's law toward a 50-nm mode in 2016. The basic processes described in Chapters 8 and 9 would not suffice to produce feature sizes much below the 200-nm mode. Advancing beyond this milestone requires a whole host of improvements on the basic processes. They include new resists, new exposure sources, improved masks, and more.

Review Questions

1. Draw cross-sectional diagrams of the ten-step process with a positive resist and dark-field mask.
2. Make a list of the major components in photoresist and explain the role of each.
3. What type of polymers are in negative resist?
4. What type of polymers are in positive resist?
5. Describe the changes in positive and negative resist during exposure to light.
6. Name the exposure and alignment systems that require a mask or reticle.
7. Which exposure system(s) are used for ULSI processes? Explain why.
8. Name ten factors that effect the image size.
9. What is the result of too low a soft-bake temperature?
10. What process steps are required to complete the first image transfer?

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Chapter

9

The Ten-Step Patterning Process—Developing to Final Inspection

Overview

In this chapter, the basic patterning process step used for photoresist developing through final inspection (steps 5 through 10 of the basic process) are explained. The end of the chapter examines the processes used for mask making and a discussion of alignment error budgets.

Objectives

Upon completion of this chapter, you should be able to:

1. Draw a cross section of a wafer before and after developing.
2. Make a list of the developing methods.
3. Explain the purpose and methods of hard bake.
4. List at least five reasons why a wafer can be rejected at develop inspect.
5. Draw a diagram of the develop-inspect-rework loop.
6. Explain the methods and relative merits of wet and dry etch.
7. Make a list of the resist strippers used to strip photoresist from oxide and metal films.
8. Explain the purpose and methods of final inspection.

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Development

After the wafer completes the alignment and exposure step, the device or circuit pattern is coded (*latent image*) in the photoresist as regions of exposed and unexposed resist (Fig. 9.1). The pattern is "developed" in the resist by the chemical dissolution of the unpolymerized resist regions. Development processes are designed to form in the resist layer a pattern with the exact dimensions designated during the circuit design process. A problem resulting from a poor developing process (Fig. 9.1) is underdevelopment, which leaves the hole incompletely developed to the correct dimensions, or a coved sidewall. In some cases, the development will not be long enough (incomplete) and will leave a layer of resist in the hole. The third problem is overdevelopment, which removes too much resist from the image edge or top surface. High-aspect plug holes are a particular challenge with uniform hole diameter and cleaning being difficult due to the lack of fluid circulation in the deep hole.

Negative and positive resists have different developing characteristics and require different chemicals and processes (Fig. 9.2).

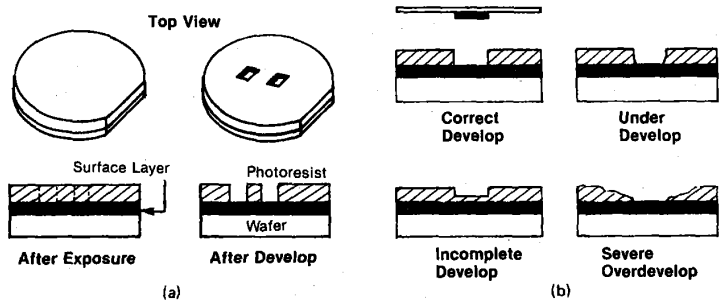


Figure 9.1 Photoresist development. (*a*) Process; (*b*) problems.

	Positive Resist	Negative Resist
Developer	Sodium hydroxide (NaOH) Tetramethyl amonium hydroxide (TMAH)	Xylene Stoddard solvent
Rinse	Water (H_2O)	n-Butylacetate

Figure 9.2 Resist developer and rinse chemicals.

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Negative resist development

The successful development of the image coded in the resist is dependent on the nature of the resist's exposure mechanisms. Negative resist, upon exposure to light, goes through a process of polymerization that renders the resist resistant to dissolution in the developer chemical. The dissolving rate between the two regions is high enough that little of the resist layer is lost from the polymerized regions.

The chemical preferred for most negative-resist developing situations is xylene, which is also used as the solvent in negative-resist formulas.

The development step is done with a chemical developer followed by a rinse. For negative resists, the rinse chemical is usually *n*-butyl acetate, because it neither swells nor contracts the resist. Either of these actions could change pattern dimensions. For wafers that have been patterned with a stepper, a milder-acting Stoddart solvent may be used.

The action of the rinse is twofold. First, it rapidly dilutes the developer chemical to stop the developing action. Although the polymerized resist is developer resistant, there is always a transition region at the exposed edge (Fig. 9.3) that contains partially polymerized molecules.

If the developer is allowed to stay in full strength on the wafer, it dissolves into this region and changes the image dimensions. The second action of the rinse is to remove partially polymerized pieces of resist from the open regions in the resist film.

Use of an all-aqueous negative-resist development system is an industry goal. Eliminating the organic solvents from the fab area would serve to reduce the safety systems and lower the cost of treating or removing the spent chemicals. To date, little success with an acceptable replacement has been reported.

Positive resist development

Positive resists present a different developing condition. The two regions, polymerized and unpolymerized, have a dissolving rate differ-

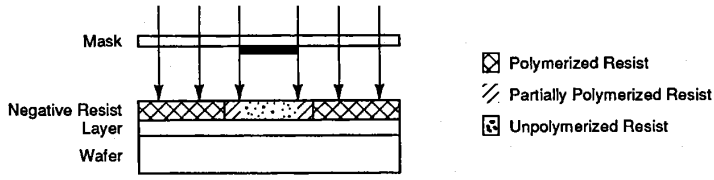


Figure 9.3 Transition region at resist image edge.

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ence of about 1:4. This means that, during the developing step, some resist is always lost from the polymerized region. The use of developers that are too aggressive or that have overly long developing times may result in an unacceptable thinning of the resist film, which in turn may cause it to lift or break down during the etch step.

Two types of chemical developers are used with positive resist, alkaline-water solutions and nonionic solutions. The alkaline-water solutions can be sodium hydroxide or potassium hydroxide. Since both of these solutions contain mobile ionic contaminants, they are not desirable in processing sensitive circuits. Most positive-resist fabrication lines use a nonionic solution of tetramethylammonium hydroxide (TMAH). Sometimes a surfactant is added to break down the surface tension and make the solution more wettable to the wafer surface. The aqueous nature of positive developers makes them more environmentally attractive than the solvent developers required for negative resists.

The positive-resist developing process is more sensitive than negative processes.[1] Factors influencing the outcome are the soft bake time and temperature; degree of exposure; developer concentration; and time, temperature, and method of developing. The development process parameters are determined by matrix testing of all the variables. The effect on line width for a particular process is shown in Fig. 9.4.

Tight control of the development and rinse process is critical for dimensional control when using a positive resist. The rinse chemical for positive-resist developers is water. It serves the same role as negative-resist rinsers but is cheaper, safer to use, and allows easier disposal.

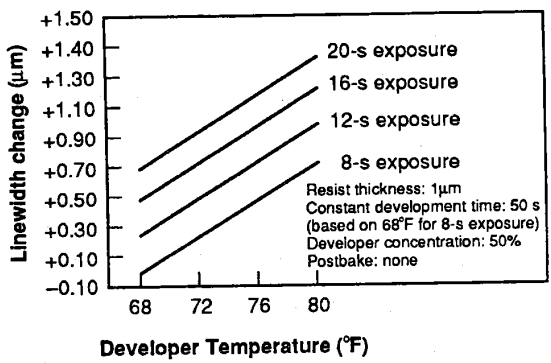


Figure 9.4 Developer temperature and exposure relationship versus line-width change.

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Wet development methods

- Immersion
- Spray
- Puddle

Figure 9.5 Development methods.

Several methods are used to develop resist films (Fig. 9.5). The selection of a method is dependent on the resist polarity, the feature size, defect density considerations, the thickness of the layer to be etched, and productivity.

Immersion. Immersion is the oldest development method. In its simplest form, the wafers, in a chemically resistant carrier, are immersed in a tank of the developer solution for a specific time before being transferred to a second tank of the rinse chemical (Fig. 9.6). The problems associated with such a simple wet procedure are the following:

1. The surface tension of the liquids can prevent the chemicals from penetrating into small openings.
2. Partially dissolved pieces of resist can cling to the wafer surface.
3. The tanks can become contaminated as hundreds of wafers are processed through them.
4. The wafers can become contaminated as they are drawn through the liquid surface.
5. Developer chemicals (especially positive developers) can become diluted through use.
6. Frequent changing of solutions to eliminate problems 1, 2, and 3 raises the cost of the process.
7. Fluctuations in room temperature can cause changes in the developing rate of the solution.
8. The wafers have to be quickly transferred to a drying process step, which introduces a third step.

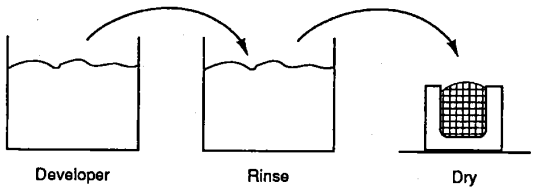


Figure 9.6 Immersion developer steps.

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Additions are often made to the immersion tanks to improve the development process. Uniformity and penetration of small openings are aided by mechanical agitation of the bath by stirring or rocking mechanisms. A popular stirring system is a Teflon®-encapsulated magnet that is coupled to a rotating magnetic field outside the tank.

Agitation is also achieved by passing ultrasonic or megasonic waves through the liquid. The ultrasonic waves cause a phenomenon called *cavitation*. The energy in the waves causes the liquid to separate into tiny cavities that immediately collapse. The rapid generation and collapse of the millions of microscopic cavities create a uniformity of development and help the liquid penetrate into small openings. Sonic energy in the megasonic range (1 MHz) reduces a stagnant boundary layer that naturally clings to the wafer surface.[2] Uniform development rates are also enhanced by the addition of heaters and temperature controllers to the bath.

Spray development. The preferred method of chemical development is by spray. In fact, spray processing is generally preferred over an immersion system for any wet process (clean, develop, etch) for a number of reasons. For instance, there is a major reduction in chemical use with spray systems. Process improvements include better image definition due to the mechanical action of the spray pressure in defining the resist edge and removing partially polymerized pieces of resist. Spray systems are always cleaner than immersion systems, because each wafer is developed (or etched or cleaned) only with fresh chemicals.

Spray processing is done in either single or batch systems. In the single-wafer configuration (Fig. 9.7), the wafer is clamped on a vacuum chuck and rotated while the developer and rinse are sequentially sprayed onto the surface. Drying takes place immediately after the rinse cycle by increasing the rotational speed of the wafer chuck. In

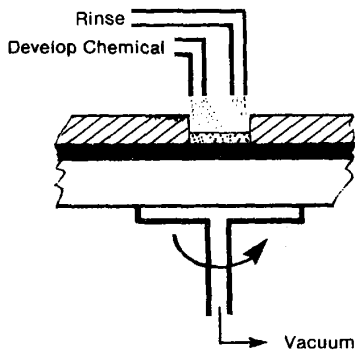


Figure 9.7 Spray development and rinse.

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appearance and design, a spray developer system for single wafers is the same as a resist spinner but plumbed for different chemicals. Single-wafer spray developers offer the advantage of track automation by integrating the developing and hard bake processes. A major process advantage of these systems is the increased uniformity from the direct impingement of the chemical spray on the wafer.

Spray development had been a standard process for negative resist for years, because negative resist is fairly insensitive to the temperature of the developer. For the temperature-sensitive positive resists, spray development is a more demanding process. The problem is the phenomenon of rapid cooling of a fluid dispensed through an orifice under pressure. Called *adiabatic cooling*, it is the same phenomenon that causes a can of pressurized household cleaner to cool during dispensing. Spray developers used for positive resist often have a heated wafer chuck or a heated spray nozzle to control the develop temperature. Other problems encountered with the spray development of positive resist are machine deterioration when alkaline developers are used and foaming as the water-based developer comes out of the nozzle under pressure. Batch developers come in two versions, single boat and multiple boat. These machines are the spin-rinse-dryers described in Chapter 7. As developers, they require additional plumbing to accommodate the developing chemicals. Batch developing systems, in general, are less uniform than direct-spray, single-wafer systems, because the spray does not impinge directly on each wafer surface, and temperature control for positive resist processing is more complicated.

Puddle development. Spray development is very attractive for its uniformity and productivity. A process variation used to gain the advantages of spray for development of positive resist is the *puddle procedure*. This system uses a standard single-wafer spray unit. The difference between regular spray development and the puddle procedure is in the application of the developer chemical to the wafer. The process starts with the deposit of enough developer on the static wafer to cover the surface (Fig. 9.8). Surface tension holds the developer in a puddle on the wafer. The puddle sits there for some required time, usually on a chuck-heated wafer, causing the majority of the development to take place. Puddle development is, in effect, a single-wafer, front-side-only immersion process. After the required puddle time, the wafer surface is sprayed with more developer and rinsed, dried, and passed on to the next step.

Plasma descum. A particularly difficult form of incomplete development is a condition called *scumming*. The scum may be undissolved

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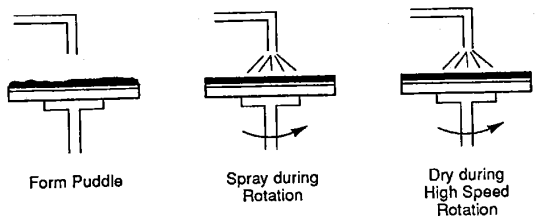


Figure 9.8 Puddle-spray development.

pieces of resist or dried developer[3] left on the surface. The film is very thin and is difficult to detect with visual inspection. In reaction to this problem, advanced ULSI lines with micron and submicron openings will remove (descum) the film from the wafers in a oxygen-rich plasma chamber after a chemical develop.

Dry (or plasma) development

The elimination of liquid processes has been a long-term goal. They are difficult to integrate into automated lines, and the chemicals are a substantial expense to purchase, store, control, and remove/dispose. One approach to replacing liquid chemical developers is to use a plasma etch process. Dry plasma etch is a well established process for etching wafer surface layers (see "Dry Etch"). In a plasma etcher, ions, energized by a plasma field, chemically dissolve (etch away) exposed layer surfaces. Dry resist development requires a photoresist chemistry that leaves either the exposed or unexposed portions of the resist layer readily removable by plasma energized oxygen. In other words, one part of the pattern is oxidized off the wafer surface. A dry development process, called DESIRE, uses silylation and plasma O_2 and is described in Chapter 10.

Hard Bake

Hard bake is the second heat treatment operation in the masking process. Its purpose is essentially the same as the soft bake step: the evaporation of solvents to harden the resist. For hard bake, however, the goal is exclusively to achieve good adhesion of the resist to the wafer surface. As such, this step is sometimes called *pre-etch bake* or *prebake.*

Hard bake methods

Hard bake is similar to soft bake in the equipment and methods used. Convection ovens, in-line and manual hot plates, infrared tunnel ov-

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ens, moving-belt conduction ovens, and vacuum ovens are all used for hard baking. The track systems are preferred for automated lines. See the "Soft Bake" section in Chapter 8 (p. 227).

Hard bake process

The exact time and temperature of the hard bake are determined much the same as in the soft bake process. The starting point is the process recommended by the resist manufacturer. After that, the process is fine-tuned to achieve the adhesion and dimensional control required. Nominal hard bake temperatures are from 130 to 200°C for 30 min in a convection oven. Temperatures and times vary in the other methods. The minimum temperature is set to achieve good adhesion of the resist image edge to the surface. The heat-caused adhesion mechanism is dehydration and polymerization. The heat drives water out of the resist, at the same time further polymerizing it, thereby increasing its etch-resistant properties.

The upper temperature limit of the hard bake is set by the flow point of the resist. Resist is a plastic-like material that softens and flows when heated (Fig. 9.9). When the resist flows, the image dimensions are changed. Resist flow is first evident as a thickening of the resist edge when viewed with a microscope. Extreme flow exhibits itself as a series of fringe lines around the image. The fringes are an optical effect from the slope left in the resist after the flow.

Hard bake takes place either immediately after the developing step or just before the etching step, as shown in Fig. 9.10. In most produc-

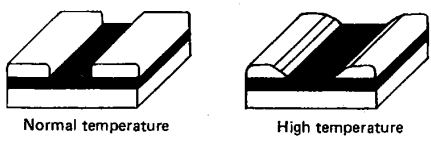


Figure 9.9 Resist flow at high temperature.

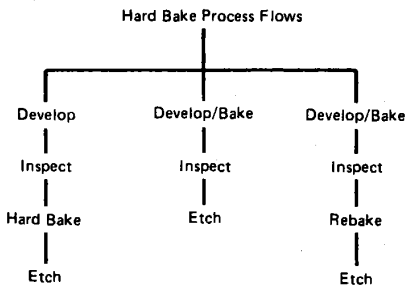


Figure 9.10 Hard bake process flow options.

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tion situations, the hard bake is performed in a tunnel oven that is in-line with the developer. When this procedure is used, it is important that the wafers be stored in a nitrogen atmosphere and/or be processed through the develop inspection step as quickly as possible to prevent the reabsorption of water into the resist film.

A goal of process engineering is to have as many common processes as possible. For hard baking, that is sometimes difficult due to the different adhesion characteristics of various wafer surfaces. The more difficult surfaces, such as aluminum- and phosphorus-doped oxides, are sometimes given a higher-temperature hard bake or a second hard bake in a convection oven just prior to being etched.

Integrated Image Processing

Often, the exact image dimensions cannot be obtained at the alignment and expose process. In some cases, the image can be brought to the correct dimension with a controlled overetch.

Develop inspect

The first quality check in the photomasking process is performed after developing and baking. It is appropriately called *develop inspect* or simply DI. The purpose of the inspection is to identify wafers that have a low probability passing the final masking inspection, provide process performance and process control data, and identify wafers for rework.

This inspection yield (that is, the number of wafers that pass this first quality check) is not factored into the overall yield formula, but it is a much-watched yield for two principal reasons. The critical nature of the photomasking process to the functioning of the circuit has been emphasized throughout this text. It is at develop inspect that the process engineer has the first chance to judge the performance of the process. The second importance of the develop inspect step is related to the two types of rejects made at this inspection. First, some of the wafers will have problems from previous steps that prevent their continuation in the process. These wafers are rejected at develop inspect and discarded. Other wafers have problems associated specifically with the quality of the pattern in the resist film. These wafers can be reworked (Fig. 9.11) by removal of the photoresist and reinsertion into the patterning process. This is one of the few places in the entire fabrication process where a general rework of mistakes is possible, since no permanent changes have been made to the wafer.

Wafers sent back into the masking process are called *reworks* or *redos*. The goal is to keep the rework rate as low as possible—certainly

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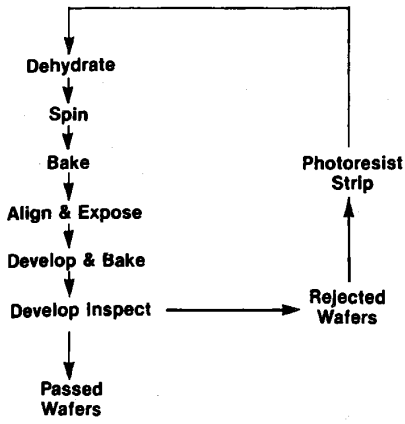


Figure 9.11 Rework process loop.

under 10 percent and preferably less than 5 percent. Experience has shown that wafers that have gone through a masking rework have a lower wafer sort yield at the end of the fab process. Reworking causes adhesion problems, and the additional handling can result in contamination and breakage. If too many wafers are in the rework loop, the overall wafer sort yield will suffer, and the production line will be clogged. A second reason for keeping the rework rate under control is related to the additional accounting and identification required to process the rework wafers.

The develop inspect yield and rework rate vary from mask level to mask level. In general, the first levels in the masking sequence have wider feature sizes, flatter surfaces, and lower density, all of which make for a higher yield out of the mask step. By the time the wafers are at the critical contact and metal masks, the rework rate tends to rise.

Develop inspect methods

Descriptions of the inspection equipment are presented in Chapter 14. In general, there are four primary categories of wafer problems that occur at both develop inspect and final inspect. There are deviations in the pattern dimensions (critical dimension measurements). There are misaligned patterns. There are surface problems such as contamination, holes or scratches in the photoresist, and stains or other surface irregularities. Finally, there are patterns that are distorted in shape.

Manual inspection. The flow diagram in Fig. 9.12 shows a typical manual develop inspection sequence. The first step is a naked-eye in-

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Step	Looking For:	Methods
1.	Stains/ gross contamination	Naked eye/UV light
2.	Stains/contamination Pattern irregularities Missalignment	100-400X microscope/ SEM/ AFM/ Automatic Inspection Systems
3.	Critical dimensions	microscope/SEM/ AFM

Figure 9.12 Order of develop inspection.

spection of the wafer surface. Since no magnification is used, this inspection is sometimes called a 1× inspection (a magnification of 1 is equal to naked-eye viewing). It may take place in normal room light, but it is more likely that the wafer will be viewed under a collimated white light or a high-intensity ultraviolet light. The wafer is viewed at an angle in the light beam. This method is surprisingly effective in showing film thickness irregularities, gross developing problems, scratches, and contamination, especially stains.

Wafers that pass the 1× visual inspection are inspected with a microscope. Most industrial inspection techniques use a system called *random sampling* based on probability theory. The theory determines the size of an area that must be inspected to accurately detect the level of defects on the complete wafer. Such an inspection system is based on the operator selecting sites for inspection in a random fashion.

Random sampling is not used in manual inspection. As the defect density goes down, as it must for VLSI circuits, the area of inspection must go up if the defects are to be statistically sampled. However, as the die density goes up, the individual parts also get smaller, which in turn requires a higher magnification to see them. The increasing magnification narrows the field of view, which in turn increases the time for an operator to inspect a wafer. The time required to statistically sample a large-diameter, low-defect wafer is prohibitive.

The usual procedure is to select a number of specific locations for inspection. The chosen die are assumed to geographically represent the wafer surface. This method also assumes that gross problems will show up on the selected die. This method is adequate for gross wafer-wide problems and for alerting the process engineer to problems in the masking process. Often, the microscopes will have motorized/programmable stages that automatically go to the inspection areas on the wafer.

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In addition to the issue of the die sampling plan, there is the issue of the wafer sampling plan. The number of wafers inspected varies with the sensitivity and difficulty of the particular mask level. The more sensitive and difficult the layer, the more wafers are likely to be inspected. The number of wafers inspected per batch varies from a few to 100 percent. In addition to process defects, dimensional measurement and control is part of the develop inspection. On each mask level, there is a region or set of patterns whose dimensions are critical to the functioning of the whole circuit. A representative pattern is chosen for each level as the *critical dimension* (CD). During the develop inspection, the dimensions of these patterns are measured using manual or automatic microscopic techniques.

Automatic inspection. With die getting larger, dimensions getting smaller, and processes getting more numerous and more sophisticated, the relatively slow manual inspection becomes nonproductive. Automatic inspection systems designed to detect surface and pattern distortion problems are the inspection system of choice for both off-line and on-line inspections. The systems are described in Chapter 14. Automatic systems offer the prospect of higher amounts of data, and this in turn enables the process engineers to characterize and control the processes. They also are consistent, whereas humans vary in abilities and fatigue doing repetitive tasks. However, some process defects such as very small particles and problems from previous patterning steps can escape detection with automated systems. Optical microscopes are still useful for analysis.

Causes of develop inspection reject

There are many reasons why a wafer can be rejected or sent for rework at the develop inspection step. Generally, the only defects looked for are those added to the wafer during the current photomasking step. Defects from previous masking steps are generally overlooked under the theory that every wafer is passed on with some defects or problems and that the wafer arrived at the current step with acceptable quality. If there is a serious problem with a wafer that somehow escaped previous inspections, it is pulled from the batch.

The inspection is generally on a *first-fail basis*. The operator or machine inspects until a rejectable level is reached on the wafer and the wafer is pulled. The information for each wafer is logged (Fig. 9.13) for data accumulation and analysis. Automatic and semiautomatic optical inspection stations have electronic memories for accumulating and correlating this reject data.

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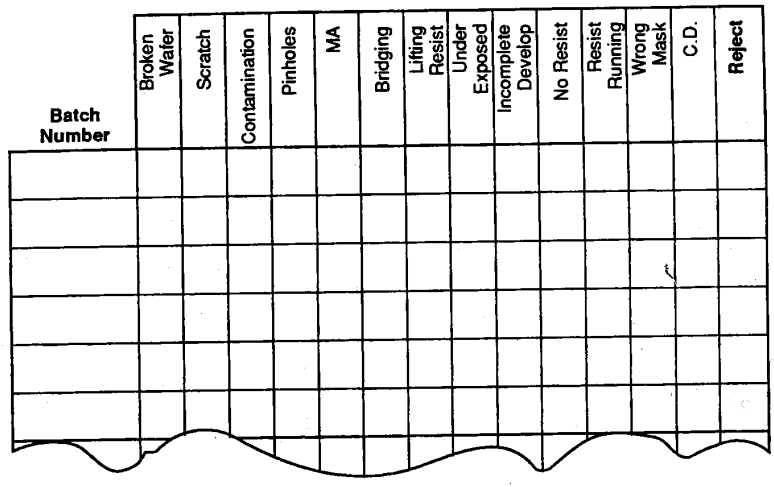


Figure 9.13 Typical develop inspect log.

Most of the causes for rejects have been discussed. One problem not discussed is bridging (Fig. 9.14). It is a condition in which two patterns are connected (bridged) by a thin layer of photoresist, usually at the metal layer. If passed on to the etch step, the photoresist bridge results in an electrical short between the patterns. Bridging comes from an overexposure, poor mask definition, or a resist film that is too thick. Bridging is a particularly vexing problem as patterns get closer together.

Etch

At the completion of the develop inspect step, the mask (or reticle) pattern is defined in the photoresist layer and is ready for etch. It is in

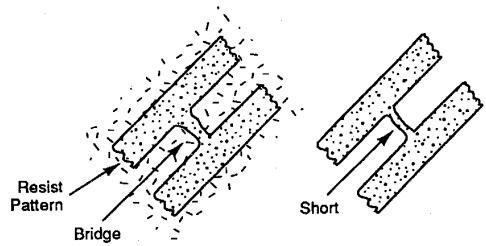


Figure 9.14 Bridged conduction lines.

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the etch step that the image is permanently transferred into the surface layer on the wafer. Etching is the process of removing the top layer(s) from the wafer surface through the openings in the resist pattern.

Etching processes fall into two main categories: wet and dry (see Fig. 9.21, p. 265). The primary goal of each is an exact transfer of the image from the mask/reticle into the wafer surface. Other etch process goals include uniformity, edge profile control, selectivity, cleanliness, and minimizing cost of ownership (COO).

Wet Etching

The historic method of etching has been by immersion techniques using wet etchants. The procedure is similar to the preoxidation clean-rinse-dry process (Chapter 7) and immersion development. Wafers are immersed in a tank of an etchant for a specific time, transferred to a rinse station for acid removal, and transferred to a station for final rinse and a spin-dry step. Wet etching is used for products with feature sizes greater than 3 μm. Below that level, the control and precision needed requires dry-etching techniques.

Etching uniformity and process control are enhanced by the addition of heaters and agitation devices, such as stirrers or ultrasonic and megasonic waves, to the immersion tanks.

Wet bench methods are giving way to spray systems similar to those described in Chapter 7. For etching, the control of the chemical composition and timing becomes critical.

Contamination problems is addressed by *point-of-use filters*. These are special filters fitted to automatic chemical dispensing systems to filter-clean the chemicals just prior to filling the immersion tank. This placement catches particulate contamination from the chemicals, the pumps, and the tubing systems.

Wet etchants are selected for their ability to uniformly remove the top wafer layer without attacking the underlying material (good selectivity).

Etch time variability is a process parameter influenced by temperature variations as the boat and wafers come to temperature equilibrium in the tank and the continued etching action as the wafers are transferred to a rinse tank. Generally, the process is set at the shortest time compatible with uniform etching and high productivity. The maximum time is limited to the amount of time the resist will continue to adhere to the wafer surface.

The exactness of the image transfer is dependent on several process factors. They include incomplete etch, overetching, undercutting, selectivity, and anisotropic/isotropic etching of the sidewalls.

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Incomplete etch

Incomplete etch is a situation in which a portion of the surface layer remains in the pattern hole or on the surface (Fig. 9.15). The causes of incomplete etch are too short an etch time, the presence of a surface layer that slows the etching, or an uneven surface layer that results in incomplete etch in the more thickly coated portions of the wafer. If wet-chemical etching is used, a lowered temperature or weak etch solution will cause incomplete etch. If dry-plasma etching is used, a wrong gas mixture or an improperly operated system can cause the same effect.

Overetch and undercutting

The opposite condition to incomplete etch is overetch. In any etch process, there is always some degree of overetch planned. This allows for thickness variations in the surface layer. Planned overetch also allows for the etch to break through any slow-etching layers on the top surface.

The ideal etch leaves vertical sidewalls in the layer (Fig. 9.16). Etch techniques that produce this ideal result are said to be *anisotropic*. However, the etchant removes material in all directions. This phenomenon is called *isotropic* etching. Etching takes place at the top of the layer for the entire time it takes to reach the bottom of the layer. The result is a sloped side. This action is also called *undercutting* (Fig. 9.17), because the surface layer is undercut below the resist edge. An ongoing goal of the etch step is the control of undercutting to an acceptable level. Circuit layout designers take undercutting into account when planning the circuit. Adjacent patterns must be separated a certain distance to prevent shorting. The amount of undercutting must be calculated when the pattern is designed. The anisotropic etching available with plasma etching is preferred for advanced circuits. Reducing undercutting allows denser circuits.

Severe undercutting (or overetch) takes place when the etch time is excessive, the etching temperature is too high, or the etch mixture is too strong. Undercutting is also present when the adhesion bond be-

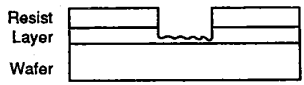


Figure 9.15 Incomplete etch.

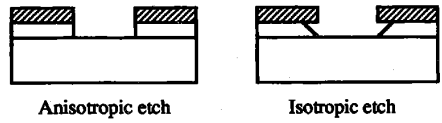


Figure 9.16 Anisotropic and isotropic etch.

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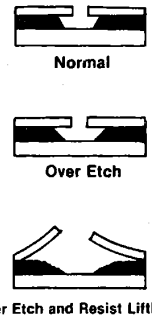


Figure 9.17 Degrees of undercutting.

tween the photoresist and the wafer surface is weak. This is a constant worry, and the purpose of the dehydration, prime, soft bake, and hard bake steps is to prevent this type of failure. Failure of the resist bond at the edge of the etch hole can result in severe undercutting. If the bond is very poor, the resist can lift from the wafer surface, causing catastrophic undercutting.

Selectivity

Another goal in the etch step is the preservation of the surface underlying the etched layer. If the underlying surface of the wafer is partially etched away, the physical dimensions and electrical performance of the devices are changed. The property of the etch process that relates to preservation of the surface is *selectivity.* It is expressed as the ratio of the etching rate of the layer material to the etch rate of the underlying surface. Oxide/silicon selectivity varies from 20 to 40,[4] depending on the etching method. High selectivity implies little or no attack of the underlying surface. Good selectivity becomes a problem in etching small contacts with aspect ratios greater than 3:1.[5] Selectivity also applies to the removal of the photoresist. This is more of a consideration in dry etch processes. While the top layer(s) is being removed by the etchant, some photoresist is also being removed. The selectivity factor must be high enough to ensure that the photoresist is not removed before the etched layer.

Silicon wet etching

Silicon layers are typically etched with a solution of nitric and hydrofluoric (HF) acids mixed in water. The formula becomes an important factor in control of the etch. In some ratios, the etch has an exothermic reaction with the silicon. Exothermic reactions are those that produce heat, which in turn speeds up the etch reaction, which in turn creates

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more heat, and so on, resulting in an uncontrollable process. Sometimes, acetic acid is mixed in with the other ingredients to control the exothermic reaction.

Some devices require the etching of a trough or trench into the silicon surface. The etch formula is adjusted to make the etch rate dependent on the orientation of the wafer. ⟨111⟩-oriented wafers etch at a 45° angle, whereas ⟨100⟩-oriented wafers etch with a "flat" bottom.[6]

Other orientations result in different-shaped trenches. Polysilicon films are also etched with the same basic formula.

Silicon dioxide wet etching

The most common etched layer is a thermally grown silicon dioxide. The basic etchant is hydrofluoric acid, which has the advantage of dissolving silicon dioxide without attacking silicon. However, full-strength HF has an etch rate of about 300 Å/s at room temperature.[7] This rate is too fast for a controllable process (a 3000-Å layer would etch in only 10 s).

In practice, the HF (assay of 49 percent) is mixed with water or ammonium fluoride and water. The ammonium fluoride (NH⟨INF/4⟩F) acts as a buffer to the unwanted generation of hydrogen ions which accelerate the etch rate. These solutions are known as *buffered oxide etches* or BOEs. They are mixed in different strengths to create reasonable etch times for the particular oxide thickness (Fig. 9.18). Some BOE formulas include a wetting agent (a surfactant such as Triton X-

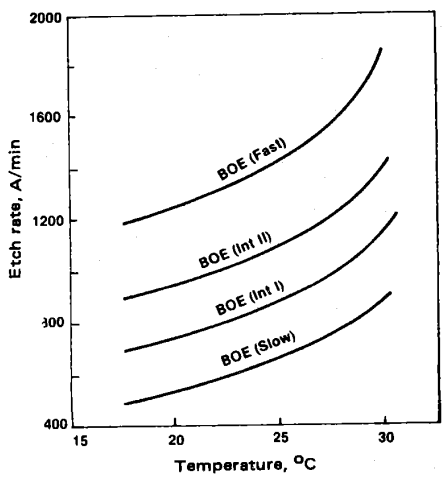


Figure 9.18 Etch rate versus temperature for BOEs.

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100 or equivalent) to reduce the surface tension of the etch, allowing it to uniformly penetrate into smaller openings.

Aluminum film wet etching

Selective etching solutions for aluminum and aluminum alloy layers are based on phosphoric acid. An unfortunate by-product of the reaction of aluminum and phosphoric acid is tiny bubbles of hydrogen, as shown in the reaction in Fig. 9.19. These bubbles cling to the wafer surface and block the etch action. The result is either bridges of aluminum that can cause electrical shorts between adjacent leads or spots of unwanted aluminum, called *snowballs*, left on the surface.

Neutralization of this problem is accomplished by use of an aluminum etching solution that contains phosphoric acid, nitric acid, acetic acid, water, and wetting agents. A typical solution of the active ingredients (less wetting agent) is 16:1:1:2.

In addition to the special formulas, a typical aluminum etch process will include wafer agitation by stirring or moving the wafer boat up and down in the solution. Sometimes, ultrasonic or megasonic waves are used to collapse and move the bubbles around.

Deposited oxide wet etching

One of the final layers on a wafer is a silicon dioxide passivation film deposited over the aluminum metallization pattern. These films are known as *vapox* or *silox* films. While the chemical composition of the films is that of silicon dioxide, the same as thermally grown silicon dioxide, they require a different etch solution. The difference is in the selectivity required of the etchant.

The usual etchant for silicon dioxide is a BOE solution. Unfortunately, the BOE attacks the underlying aluminum pads, causing bond-

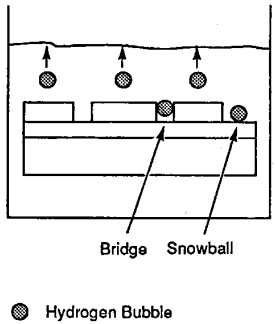


Figure 9.19 Hydrogen bubble blockage etchant.

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ing problems in the packaging process. This condition is called *brown*, or *stained, pads*. The preferred etchant for this layer is a solution of ammonium fluoride and acetic acid mixed in a ratio of 1:2.

Silicon nitride wet etching

Another compound favored for the passivation layer is silicon nitride. It is possible to etch this layer by wet chemical means, but it is not as easy as for the other layers. The chemical used is hot (180°C) phosphoric acid. Because the acid evaporates rapidly at this temperature, the etch must be done in a closed reflux container equipped with a cooled lid to condense the vapors. The major problem is that photoresist layers do not stand up to the etchant temperature and aggressive etch rate. Consequently, a layer of silicon dioxide or some other material is required to block the etchant. These two factors have led to the use of dry-etching techniques for silicon nitride.

Wet spray etching

Wet spray etching offers several advantages over immersion etching. Primary is the added definition gained from the mechanical pressure of the spray.[8] Spray etching also minimizes contamination from the etchants. From a process control point of view, spray etching is more controllable, since the etchant can be instantly removed from the surface by switching the system to a water rinse. Single-wafer spinning-chuck spray systems offer considerable process uniformity advantages.

Disadvantages to spray etching are system cost, safety considerations associated with caustic etchants in a pressurized system, and the requirement of etch-resistant materials to prevent the deterioration of the machine. On the plus side, spray systems are usually enclosed, which adds to worker safety. Figure 9.20 is a table of common semiconductor films and their common etchants.

Vapor etching

Vapor etching is the exposure of the wafer to etchant vapors. HF is the most common. Advantages are continued replenishment of the etchant at the surface with fresh vapors and instant etch termination. Keeping the toxic vapors contained in the system is a safety concern.

Dry Etch

The limits of wet etching for small dimensions have been mentioned in the previous section. For review, they include the following:

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	COMMON ETCHANT	ETCH TEMP	RATE Å /MIN	METHOD
SiO_2	HF & NH_4F (1 : 8)	Room	700	Dip & wetting agent predip
SiO_2	HF & NH_4F (1 : 8)	Room	700	Dip & wetting agent predip
SiO_2 (Vapox)	Acetic Acid & NH_4F(2 : 1)	Room	1000	Dip
Aluminum	H_3PO_4 : 16 HNO_3 : 1 Acetic : 1 H_2O : 2 Wetting Agent	40 - 50°C	2000	a) Dip & agitation b) Spray
Si_3N_4	H_3PO_4	150 - 180°C	80	Dip
POLYSi	HNO_3 : 50 H_2O : 20 HF : 3	Room	1000	Dip

Figure 9.20 Summary of wet-etching process.

1. Wet etching is limited to pattern sizes of 3 μm.
2. Wet etching is isotropic, resulting in sloped sidewalls.
3. A wet-etch process requires rinse and dry steps.
4. The wet chemicals are hazardous and/or toxic.
5. Wet processes represent a contamination potential.
6. Failure of the resist-wafer bond causes undercutting.

These considerations have led to the use of dry-etch processes for the definition of small feature sizes on advanced circuits. Figure 9.21 provides an overview of the dry etching techniques used.

Dry etching is a generic term that refers to the etching techniques in which gases are the primary etch medium, and the wafers are etched without wet chemicals or rinsing. The wafers enter and exit the system in a dry state. There are three dry-etching techniques: plasma, ion beam milling (etching), and reactive ion etch (RIE).

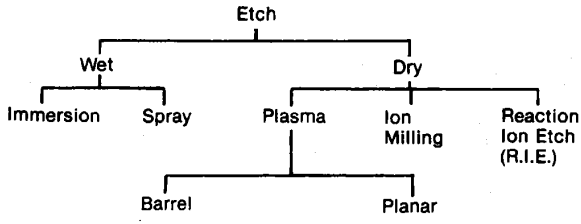


Figure 9.21 Guide to etch methods.

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Plasma etching

Plasma etching, like wet etching, is a chemical process but uses gases and plasma energy to cause the chemical reaction. Comparison of silicon dioxide etching in the two systems illustrates the differences. In wet etching of silicon dioxide, the fluorine in the BOE etchant is the ingredient that dissolves the silicon dioxide, converting it to water-rinsable components. The energy required to drive the reaction comes from the internal energy in the BOE solution or from an external heater.

A plasma etcher requires the same elements: a chemical etchant and an energy source. Physically, a plasma etcher consists of a chamber, vacuum system, gas supply, an end-point detector, and a power supply (Fig. 9.22). The wafers are loaded into the chamber, and the pressure inside is reduced by the vacuum system. After the vacuum is established, the chamber is filled with the reactive gas. For the etching of silicon dioxide, the gas is usually CF_4 mixed with oxygen. A power supply creates a radio frequency (RF) field through electrodes in the chamber. The field energizes the gas mixture to a plasma state. In the energized state, the fluorine attacks the silicon dioxide, converting it into volatile components that are removed from the system by the vacuum system.

Earlier plasma systems were designed with circular chambers and are called *barrel etchers*. In this design, ions are energized by the plasma in a nondirectional pattern. The etching ions attack the surface layer from all directions (isotropic etching), creating a tapered sidewall. Etch uniformity is a problem. It is hard to supply a constant amount of etchant to all the wafers in the system because of the nondirectionality of the etching ions and the close packing of the wafers.

Another consideration of barrel plasma etching is radiation damage resulting from the high-energy plasma field. The high energy causes charges to build up in the wafer surface that compromise the electrical functioning of the circuit. Protection of the wafers from the radiation is provided by perforated metal cylinders that isolate the wafers from the plasma field (Fig. 9.23).

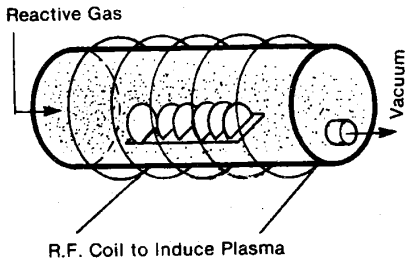


Figure 9.22 Barrel plasma etch.

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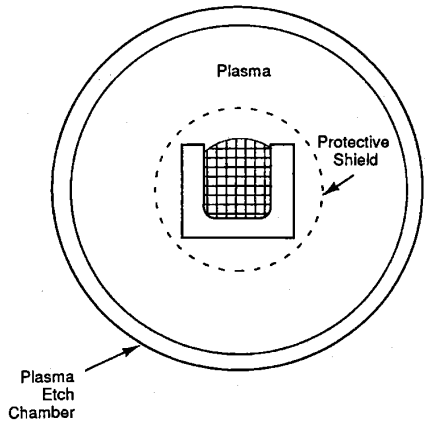


Figure 9.23 Barrel plasma stripper with protective shield.

Planar plasma etching. For more precise etching, plasma planar systems are preferred. These systems contain the basic components of the barrel system, but the wafers are placed on a grounded pallet under the RF electrode (Fig. 9.24). Etching takes place with the wafers actually in the plasma field. The etching ions are more directional than those in a barrel system, resulting in a more anisotropic etch. Almost vertical sidewalls are possible with plasma etch. Etching uniformity is increased with the rotation of the wafer pallet in the system.

Planar plasma etch systems are designed in both batch and single-wafer chamber configurations. Single-wafer systems are popular for their ability to have the etch parameters tightly controlled for uniform etching. Also, with load-lock chambers, single-wafer systems can maintain high production rates and are amenable to in-line automation.

RF-generated parallel plate plasma sources are giving way to new sources for 0.35-μm processing.[9] High-density, low-pressure plasma sources under consideration are electron cyclotron resonance (ECR),

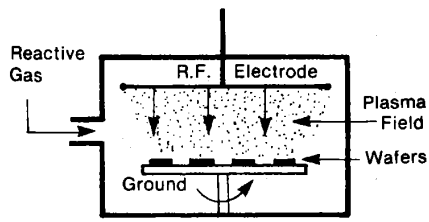


Figure 9.24 Planar plasma etch.

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high-density reflected electron, helicon wave, inductively coupled plasma (ICP), and transformer-coupled plasma (TCP).

The figures of merit for a dry etch process are: etch rate, radiation damage, selectivity, particulate generation, post-etch corrosion, and cost of ownership.

Etch rate

The etch rate of a plasma system is determined by a number of factors. System design and chemistry (Fig. 9.25) are two of them. Others are the ion density and system pressure. Ion density (no. ions/cm^3) is a function of the power supplied to the electrodes. (Power supply configurations are described in Chapter 12.) Increasing power creates more ions, which in turn increase the etch rate. Ion density is similar to increasing the strength of a liquid chemical etch solution. Ion densities are in the 3×10^{10} to 3×10^{12} range.[10] System pressure influences etch rate and uniformity through a phenomenon called *mean free path*. This is the average distance a gas atom or molecule will travel before a

Film	Etchant	Typical Gas Compounds
Al	Chlorine	BCl_3, CCl_4, Cl_2, $SiCl_4$
Mo	Fluorine	CF_4, SF_4, SF_8
Polymers	Oxygen DF_4, SF_4, SF_6	
Si	Chlorine, fluorine CF_4, SF_4, SF_6	BCl_3, CCl_4, Cl_2, $SiCl_4$
SiO_2	Chlorine, fluorine	CF_4, CHF_3, C_2F_6, C_3F_8
Ta	Fluorine	"
Ti	Chlorine, fluorine	"
W	Fluorine	"

Figure 9.25 Plasma etch chemicals.

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collision with another particle. At higher pressures, there are many collisions that give the particles many directions, which in turn causes loss of edge profile control. Low pressures are preferred, but there is a trade-off with plasma damage as explained below. System pressures typically run in the 0.4 to 50 m torr range.[11] Etch rates vary from 600 to 2000 Å/min.[12]

Radiation damage

It would seem that higher-density sources with low pressure is the preferred system design. However, there is a countervailing process of *radiation* or *plasma* damage to the wafers. Within the plasma field are energetic atoms, radicals, ions, electrons, and photons.[13] These species, depending on their concentration and energy levels, cause various damage in semiconductors. The damage includes surface leakage, changes in electrical parameters, degradation of films (especially oxides), and damage to silicon among others. There are two damage mechanisms. One is simple overexposure to the high-energy species in the plasma. The other is *dielectric wearout* from currents flowing across dielectrics during the etch cycle.[14] Higher-density sources also cause a problem for photoresist removal. The combination of the energy and low pressure tend to harden the resist to a level that is difficult to remove with conventional processes (see "Resist Stripping," p. 273). System designers are looking to plasma sources that feature high-density, low-energy ions (to reduce damage) and low-pressure operations.

Besides balancing the ion density/pressure parameters, *downstream plasma* processing is an option to reduce plasma damage. The damaging species come from the high energy applied to the gas by the plasma source. Downstream systems create the plasma field in one chamber and transport it downstream to the wafer(s). The wafers are separated from the damaging plasma. To minimize the damage, the system must allow for distinguishing the plasma discharge, ionic recombination, and reduction of the electron density.[15] Downstream plasma systems were developed to minimize damage during plasma resist removal. They are attracting interest for etch applications even though they add more complexity to an etch system.

Selectivity

Selectivity is a major consideration in plasma etching processes, especially when balanced against the need for overetch. Ideally, an etch time could be calculated to remove the anticipated layer thickness with just a little overetch time for safety. Unfortunately, the accumu-

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lated thickness and composition variations on multiple layer *stacks* on high-density devices present etch uniformity problems. Also on high-density devices, a phenomenon called *microloading* introduces etch rate variations. Microloading is a change in the local etch rate relative to the area of material being etched. A large area will *load* the etching process with removed material, slowing it down in that area while a smaller etch area proceeds at a faster rate. Topography issues also drive overetch considerations. A typical situation is the opening of contact holes in both thin regions and thick regions on the device/circuit (see Fig. 10.13). These factors can lead to an overetch of 50 to 80 percent[16] for metal etches and up to 200 percent for oxides and polysilicon etches.[17]

Overetch makes the issue of selectivity critical. There are two factors to consider: the photoresist and the underlying layer (usually silicon or silicon nitride). Dry-etch process have a higher resist removal rate than wet processes. Given the thinner photoresist layers used to define small geometries and the increasing use of stacks of layers, the photoresist selectivity becomes critical. Compounding the selectivity issue are high-aspect-ratio patterns. Advanced devices have patterns with up to 4:1 aspect ratios. The holes are so narrow compared to their height that etching can slow up or stop near the bottom.[18]

Four methods used to control selectivity are the selection of the etching gas formula, the etch rate, the dilution of the gas near the end of the process to slow down the attack of the underlying layer, and end-point detectors in the system.

Terminating the etch when the top layers have been removed requires an in-system end-point detector. Typically, a laser interferometer is used. A laser beam is reflected off of the wafer surface as the etch proceeds. It returns to the detector in an oscillating mode that varies with the type of material being etched.* An endpoint detector senses the presence of the etching layer material in the exhaust stream and automatically signals an end to the etch when no more material is detected.

Contamination, residues, corrosion, and cost of ownership. Other process problems of concern, especially in the submicron range, are particulate generation, residues, post-etch corrosion, and all the cost-of-ownership (COO) factors. One approach to reduction of particles is an electrostatic wafer holder to replace mechanical holders. Mechanical

*If the material(s) is transparent or semitransparent. When the characteristic signal from the last layer etched changes, the detector terminates the etch process. A typical reflectance pattern for a dual layer of salicide/polysilicon is shown in Fig. 9.26.

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holders generate particles and cause wafer breakage, and the clamps shadow part of the wafer surface. The electrostatic clamp holds the wafer with a direct current (dc) potential between the wafer and the chuck.[19]

The plasma etch environment is highly reactive, and many chemical reactions take place. Hydroxyl groups in the photoresist react with metal halide gases to form stable metal halide (such as AlF_3, WF_5, WF_6) and oxides such as TiO_3, TiO, and/or WO_2.[20] These residues create contamination problems and can interfere with the selective deposition of tungsten.[21]

Post-etch corrosion results from some etch residues left on metal patterns after the etch process. The addition of copper to aluminum metal and the use of titanium/tungsten metallization increase the corrosion problem from residual chlorine after plasma etch. Minimizing this problem includes substituting fluorine-based etchants for chlorine etchants, passivating the sidewalls, and post-etch processes such as removing the residual chlorine or using a native oxide to passivate the surface.[22] Other solutions include an oxygen plasma treatment, fuming nitric acid, and a wet photoresist stripper step.[23] Cost-of-ownership factors are detailed in Chapter 15. For etchers, a primary COO parameter is the etch rate.

Figure 9.25 lists the common gas etchants for various materials. Silicon and silicon dioxide processes favor fluorine-based etchants such as CF_4. Aluminum etching generally takes place with chlorine-based gases such as BCl_3.

Ion beam etching

A second type of dry-etch system is the ion beam system (Fig. 9.26). Unlike the chemical plasma systems, ion beam etching is a physical process. The wafers are placed on a holder in a vacuum chamber, and a stream of argon is introduced into the chamber. Upon entering the chamber, the argon is subjected to a stream of high-energy electrons from a set of cathode (–)-anode (+) electrodes. The electrons ionize the argon atoms to a high-energy state with a positive charge. The wafers are held on a negatively grounded holder, which attracts the ionized argon atoms. As the argon atoms travel to the wafer holder, they accelerate, picking up energy. At the wafer surface, they crash into the exposed wafer layer and literally blast small amounts from the wafer surface. Scientists call this physical process *momentum transfer.* No chemical reaction takes place between the argon atoms and the wafer material. Ion beam etching is also called *sputter etching* or *ion milling.*

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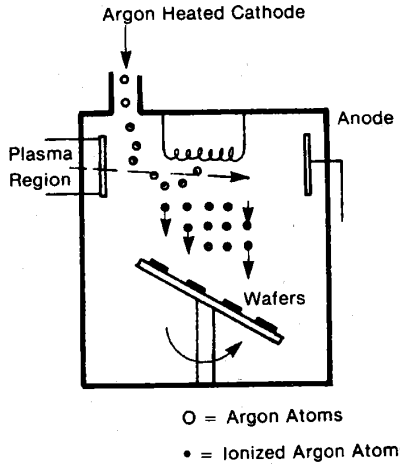


Figure 9.26 Ion beam milling.

The material removal (etching) is highly directional (anisotropic), resulting in good definition of small openings. Being a physical process, ion milling has poor selectivity, especially with photoresist layers.

Reactive ion etching

Reactive ion etching (RIE) systems combine plasma etching and ion beam etching principles. The systems are similar in construction to the plasma systems but have a capability of ion milling. The combination brings the benefits of chemical plasma etching along with the benefits of directional ion milling. A major advantage of RIE systems is in the etching of silicon dioxide over silicon layers. The combination etch results in a selectivity ratio of 35:1,[24] whereas ratios of only 10:1 are available with plasma-only etching. RIE systems have become the etching system of choice for most advanced product lines.

Resist effects in dry etching

For both wet- and dry-etching processes, a patterned photoresist layer is the preferred etch barrier. In wet etching, there is almost no attack of the resist by the etchants. However, in dry etching, residual oxygen in the system attacks the resist layer. The resist must remain thick enough to stand up to the etchants without becoming so thin that pinholes are present. Some structures use deposited layers as etch barriers to avoid the problem of resist lost (see Chapter 10).

Another resist-related dry etch problem is resist baking. Within the dry-etch chamber, the temperature can rise as high as 200°C, a tem-

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perature that can bake the resist to a condition that makes it difficult to remove from the wafer. Another temperature-related problem is the tendency of resist patterns to flow and distort the images.

One unwanted effect of plasma etching is the deposition of *sidewall polymer* strings on the sides of etch patterns. The polymer comes from the photoresist. During a subsequent oxygen-plasma resist strip step, the strings become metal oxides[25] that are difficult to remove.

Resist Stripping

After etching, the pattern is a permanent part of the top layer of the wafer. The resist layer that has acted as an etch barrier is no longer needed and is removed (or stripped) from the surface. Traditionally, the resist layer has been removed by wet chemical processing. Despite the issues, wet chemistry is the preferred method in the *front end of the line* (FEOL), where the surface and sensitive MOS gates are exposed and vulnerable to plasma damage.[26] There is a growing use of plasma O_2 stripping, primarily in the *back end of the line* (BEOL), where the sensitive devices parts are covered by surface layers of dielectrics and metals.

A number of different chemicals are used for stripping. Choices depend on the wafer surface (under the photoresist), production considerations, the polarity of the resist, and the condition of the resist (Fig. 9.27). Wafers are stripped of photoresist after a number of processes: wet etch, dry etch, and ion implantation. There are different degrees of difficulty depending on the prior process. High-temperature hard bakes, plasma etch residues and sidewall polymers, and ion implantation *crusting* all present challenges for the resist removal process.

Stripper Chemistry	Strip Temperature (Centigrade)	Surface Oxide	Metallized	Resist Polarity
Acids:				
Sulfuric acid+oxidant	125	X		+/-
Organic Acids	90-110	X	X	+/-
Chromic/Sulfuric	20	X		+/-
Solvents:				
NMP/Alkanolamine	95		X	+
DMSO/Monothanolamine	95		X	+
DMAC/Diethanolamine	100		X	+
Hydroxylamine (HDA)	65		X	+

Figure 9.27 Wet photoresist stripper chart.

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Generally, the strippers are divided into the categories of universal strippers, positive-resist-only, and negative-resist-only strippers. They are also divided by the type of wafer surface: metallized or nonmetallized.

Wet stripping is used for the following reasons:

1. It has a long process history.
2. It is cost effective.
3. It is effective in the removal of metallic ions.
4. It is a low-temperature process and does not expose the wafers to potentially damaging radiation.

Wet chemical stripping of nonmetallized surfaces

Sulfuric acid and oxidant solutions. Solutions of sulfuric acid and an oxidant (hydrogen peroxide or ammonium persulfate[27]) are the most common wet strippers used for the removal of resist from *nonmetallic* surfaces. Nonmetallic surfaces are either silicon dioxide, silicon nitride, or polysilicon. This solution strips both negative and positive resists. These are the same chemical solutions and processes used for pre-tube-cleaning wafers described in Chapter 7.

Nitric acid is sometimes used as an additive oxidant in a sulfuric acid bath. A mixing ratio of about 10:1 is typical. A drawback to nitric acid is that it turns the bath a light orange color, which can mask the buildup of carbon in the bath. Fuming nitric acid is used as a stripper in Europe and Japan. All of these solutions dissolve the resist by an oxidation mechanism.

Wet chemical stripping of metallized surfaces

Stripping from metallized surfaces is a more difficult task, because the metals are subject to attack or oxidation. Four types of wet chemicals are used for stripping metallized surfaces. They are:

1. Organic strippers
2. Solvent strippers
3. Solvent/amine strippers
4. Specialty strippers

Phenolic organic strippers. Organic strippers contain a combination of sulfonic acid (an organic acid) and chlorinated hydrocarbon solvents such as duodexabenzene. The formula requires phenol to create a rin-

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sable solution. In the 1970s, concern over the toxic ingredients in these formulas led to the development of sulfonic acid, nonphenolic, nonchlorinated[28] resist strippers. Stripping the photoresist requires heating the solutions into the 90 to 120°C range. Often, the process uses two or three heated strip baths. Rinsing is in two steps, the first being a solvent followed by a water rinse and drying step.

Solvent/amine strippers. One of the advantages of positive resists is their ease of removal from the wafer surface. A positive resist layer that has not been hard baked is easily removed from the wafer with a simple acetone soak. In fact, acetone has been the traditional positive-resist stripper. Unfortunately, acetone represents a fire hazard, and its use is discouraged.

Several manufacturers supply positive-only strippers based on solvent and organic amine solutions. *N*-methyl pyrrolidine (NMP)[29] is the most used solvent. Others are dimethylsulfoxide (DMSO), sulfolane, dimethylforamide (DMF), and dimethylacetamide (DMAC). These strippers are effective, water-rinsable, and drain-dumpable. The strippers may be heated to increase the removal rate and/or to remove resist films that have been through a high-temperature hard bake. Solvent and solvent/amine strippers remove the resist by a chemical dissolution mechanism.

Specialty wet strippers. A number of wet chemical strippers have been developed to solve specific problems. One is a positive-resist stripper based on hydroxylamine (HDA) chemistry.[30] Another chemistry relies on chelating agents to, in effect, chemically bind metal contaminants in the solution.[31] The stripper removes a host of plasma etch residues and polyimide layers not removed by solvent/amine strippers. Other strippers include corrosion inhibitors.[32]

Figure 9.27 is a table of the most common wet resist strippers and their uses. The advent of multilayer metallization systems with transition metal connecting plugs requires wet strippers that do not attack these metals.

Dry stripping

Like etching, the dry-plasma process can also be applied to resist stripping. The wafers are placed in a chamber, and oxygen is introduced (Fig. 9.28). The plasma field energizes the oxygen to a high-energy state, which in turn oxidizes the resist components to gases that are removed from the chamber by the vacuum pump. The term *ashing* is used to disiginate plasma processes designed to remove only organic

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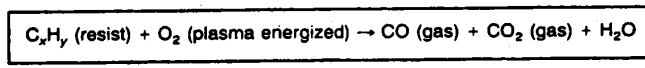


Figure 9.28 Resist removal by plasma oxygen.

residues. Plasma stripping indicates a process designed to remove both organic and inorganic residues. In dry strippers, the plasma is generated by microwave, RF, and UV-ozone sources.[33]

The major advantage of plasma resist stripping is the elimination of wet hoods and the handling of chemicals. The principal disadvantage is its ineffectiveness in the removal of metallic ions. There is not enough energy in the plasma field to volatilize the metallic ions. Another consideration of plasma stripping is radiation damage to the circuits from the high-energy plasma field. This problem is reduced with system designs that have the plasma chamber removed from the stripper chamber. They are called *downstream strippers,* because the plasma is created downstream from the wafers. MOS wafers are more sensitive to radiation effects during stripping.

Replacement of wet stripping by dry/plasma techniques has been a long-term industry desire. However, the inability of oxygen plasma to remove mobile ionic metal contamination and certain metal residues, and radiation damage concerns, have maintained wet stripping and wet/dry combinations as the mainstream photoresist removal processes. Plasma stripping is used to remove hardened resist layers. A following wet strip step is used to remove the residuals not removed by the plasma. Specialty wet strippers are available to attack these hardened layers.

Post-ion implant and plasma etch stripping

Two problem areas are photoresist removal after ion implant and after a plasma strip. Ion implant causes extreme polymerization of the resist and crusting of the top. Generally, the resist is removed or reduced with a dry process followed by a wet process. Post-plasma etch resist layers are similarly difficult to remove. In addition, the etch process can leave residues, such as $AlCl_3$ and/or $AlBr_3$, that react with water or air to form compounds that corrode the metal system.[34] Low-temperature plasma can remove the offending compounds before they take on a corrosive chemistry. Another approach is to add halogens to the plasma atmosphere to minimize the formation of the insoluble metal oxides. This is another instance of setting process parameters to achieve efficient processing (resist removal) without inducing wafer surface damage or metal corrosion.

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Final Inspection

The final step in the basic photomasking process is a visual inspection. It is essentially the same procedure as the develop inspect, with the exception that the majority of the rejects are fatal (no rework is possible).

The one exception is contaminated wafers that may be recleaned and reinspected. Final inspection certifies the quality of the outgoing wafers and serves as a check on the effectiveness of the develop inspection. Wafers that should have been identified and pulled from the batch at develop inspect are called *develop inspect escapes.*

The wafers receive a first surface inspection in incident white or ultraviolet light for stains and large particulate contamination. This inspection is followed by a microscopic or automatic inspection for defects and pattern distortions. Measurement of the critical dimensions for the particular mask level is also part of the final inspection. Of primary interest is the quality of the etched pattern, with underetching and undercutting being two parameters of concern. The table shown in Fig. 9.29 is a list of typical causes of wafer rejection found in the final inspection.

Possible Process Cause	Contamination	Misalign	Undercut	Incomplete Etch	Wrong Mask	Pin Holes	C.D.'s	Visual Reject
Contaminated Etch	x		x	x				
Contaminated Stripper	x							
Contaminated H_2O	x							
Insufficient Rinse	x		x					
No Wet Agent				x				
Under Etch				x			x	
Over Etch			x				x	
Wrong Etch			x	x			x	
Hard Bake Too High			x	x			x	
Poor Develop				x			x	
P_2O_5 & SiO_2			x				x	
B_2O_3 & SiO_2				x			x	
Low Hard Bake			x					
Develop Inspect Escapes		x	x	x	x	x		

Figure 9.29 Final inspect rejects and process causes.

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Mask Making

In Chapter 5, the steps of circuit design were detailed. In this section, the process used to construct a photomask or reticle is examined. Originally, the masks were made from emulsion-coated glass plates. The emulsions are similar to those found on camera film. These masks were vulnerable to scratches, deteriorated during use, and were not capable of resolving images in the sub-3-micron range. Masks for most modern work use a chrome-on-glass technology. This mask-making technology is almost identical to the basic wafer-patterning operation Figure 9.30. In fact, the goal is the same—the creation of a pattern in the thin chrome layer on the glass reticle surface. The preferred materials for mask/reticles are borosilicate glass or quartz, which have good dimensional stability and transmission properties for the wavelengths of the exposing sources. Chrome layers are in the 1000-Å range and deposited on the glass by sputtering (see Chapter 12). Advanced mask/reticles use layers of chromium, chromium oxide, and chromium nitride.[35]

Mask/reticle making follows a number of different paths depending on the starting exposure method (pattern generation, laser, e-beam) and the end result (reticle or mask) (Fig. 9.31). Flow A shows the process for making a reticle using a pattern generator, which is an older

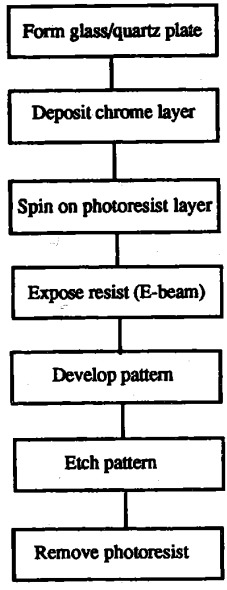


Figure 9.30 Major steps in mask/reticle plate processing.

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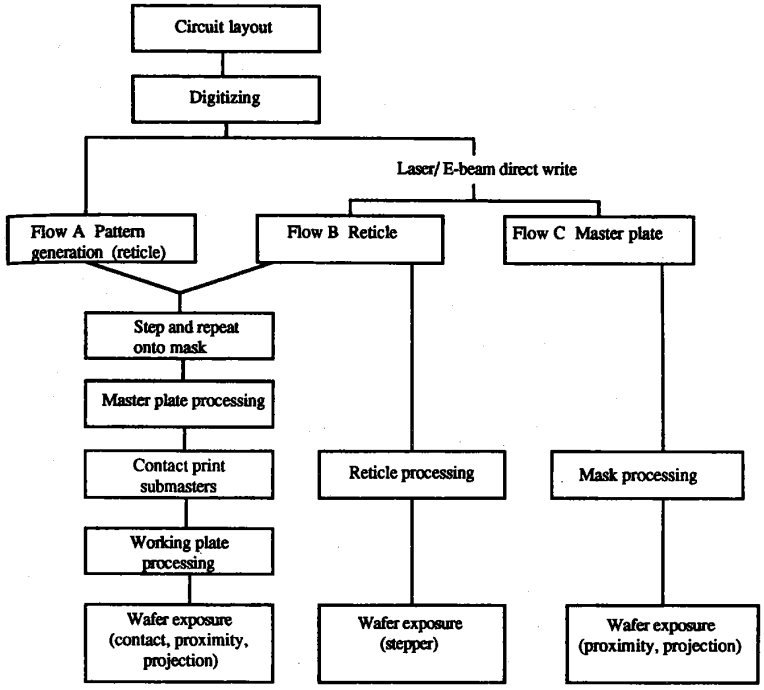


Figure 9.31 Mask/reticle-making processing flows.

technology. A pattern generator consists of a light source and a series of motor-driven shutters. The chrome-covered mask/reticle, with a layer of photoresist, is moved under the light source as the shutters are moved and opened to allow precisely shaped patterns of light to shine onto the resist, creating the desired pattern. The reticle pattern is transferred to the resist-covered mask blank by a step-and-repeat process to create a master plate. The master plate is used to create multiple working mask plates in a contact printer. This tool brings the master into contact with a resist-covered mask blank and has a UV light source for transferring the image. After each of the exposure steps (pattern generation, laser, e-beam, master plate expose, and contact print), the reticle/mask is processed through development, inspection, etch, strip, and inspection steps that transfer the pattern permanently into the chrome layer. Inspections are very critical, since any undetected mistake or defect has the potential of creating thousands of scrap wafers. Reticles for this use are generally 5 to 20 times the final image size on the mask.[36]

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Advanced products with very small geometries and tight alignment budgets require high-quality reticle and/or masks. The reticles and masks for these processes are made with lasers or e-beam direct write exposure (flows A & B). Laser exposure uses a wavelength of 364 nm, making it an I-line system. It allows using standard optical resists and is faster than e-beam. Direct-write laser sources are turned on and off with an acousto-optical modulator (AOM).[37] In all cases, the reticle or mask is processed to etch the pattern in the chrome.

Other mask/reticle process flows may be employed. The reticle in flow A may be laser/e-beam generated, or the master plate may be laser/e-beam generated.

VLSI and ULSI-level circuits require virtually defect-free and dimensionally perfect masks and reticles. Critical dimension (CD) budgets from all sources are 10 percent or better, leaving the reticles with a 4 percent error margin.[38] There are procedures to eliminate unwanted chrome spots and pattern protrusions with laser "zapping" techniques. Focused ion beams (FIB) is the preferred repair technology for small image masks and reticles. Clear or missing pattern parts are "patched" with a carbon deposit. Opaque or unwanted chrome areas are removed by sputtering from the beam.

Summary

For VLSI and ULSI work, the resolution and registration requirements are very stringent. In 1977, the minimum feature size was 3 μm. By the mid-1980s, it had passed the 1-micron barrier. By the 1990s, 0.5-micron sizes were common with 0.35-μm technology planned for production circuits. Circuit design projections call for minimum gate sizes of 10 to 15 nm in 2016.[39]

Chip manufacturers calculate several *budgets* for each circuit product. A *critical dimension (CD) budget* calculates the allowable variation in the image dimensions on the wafer surface. For products with submicron minimum feature sizes, the CD tolerances are 10 to 15 percent.[40] Also of concern is the critical defect size relative to the minimum feature size. These two parameters are brought together in an *error budget* calculated for the product. An *overlay budget* is the allowable accumulated alignment error for the entire mask set. A rule of thumb is that circuits with micron or submicron feature sizes must meet registration tolerances of one-third the minimum feature. For a 0.35-μm product, the allowable overlay budget is about 0.1μm.[41]

Review Questions

1. Name the major methods of resist development.

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2. What are the chemicals used to develop negative and positive resist?
3. What is the purpose of the hard bake step?
4. Name three methods used for hard bake.
5. What problems arise if the hard bake temperature is too low? Too high?
6. Name the preferred wet etchants for etching: silicon dioxide layers, silicon nitride layers, and aluminum layers.
7. Name two advantages of dry etching over wet etching.
8. List three principal dry etching techniques.
9. Write a wet stripping flow diagram.
10. Name the purpose and methods of final inspect.
11. List at least five problems and solutions for resolving submicron patterns.

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Chapter

10

Advanced Photolithography Processes

Overview

Feature sizes decreasing to the nanometer range, the increasing need for low defect densities, increasing chip density and size, along with larger diameter wafers have challenged the industry to squeeze every capability out of traditional processes and develop new ones. The problems encountered and current solutions to reaching nanometer circuit dimensions are explored in this chapter. Included is a discussion of post-optical lithography techniques, collectively known as *next-generation lithography* (NGL).

Objectives

Upon completion of this chapter, you should be able to:

1. Describe four exposure-related effects that cause image distortion.
2. Draw a cross-sectional flow diagram of a dual-layer resist process.
3. Draw a cross-section flow diagram of a dual damascene process.
4. List two planarization techniques.
5. State an advantage of an image-reversal process.
6. Describe how antireflective layers, contrast enhancement layers, and resist dye additives improve resolution.
7. Identify the parts of a pellicle and the advantages it offers to a resist process.

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Issues of VLSI/ULSI Patterning

The ten-step patterning process detailed in Chapters 8 and 9 is a one-photoresist-layer basic process. It would be sufficient for the production of MSI and some simple LSI and VLSI circuits. However, the VLSI/ULSI demands of decreasing feature sizes and defect densities is beyond the capabilities of the basic process. The limits showed up at the sub-three (3) micron level and became critical in the submicron era. Problems include physical limitations associated with the optical exposure equipment, resolution limits of photoresists, and a host of surface problems, including reflective surfaces and multilevel topographies.

"The report of my demise has been greatly exaggerated."—Mark Twain.

In the mid-1970s, it was widely accepted that optical photoresist processes had a lower resolution limit of about 1.5 μm. This projection gave rise to the interest in X-ray and e-beam exposure systems.

However, manipulation and improvements on the basic processes have successively lowered the usable range of optical lithography to the 0.2-μm range.[1] In the first edition of *Microchip Fabrication* (1984), I reported that "industry futurists that either e-beam or X-ray exposure will replace the UV and DUV sources by the mid-1990s. It did not happen. Optical lithography has been walking the plank for decades. And every generation of engineers has tweaked and improved patterning based on optical exposure systems to bring the industry to the 100-nm node.[2] The crystal ball of the past has been replaced with the SIA's *International Technology Roadmap for Semiconductors* (ITRS). Figure 10.1 shows the various "nodes" of future devices and their year of introduction.[3] A node is essentially the gate

Year of Production	2001	2006	2012
Line width (nm)	150	100	50
Memory size	1 Gb	16Gb	64 Gb
Logic Bits/cm2	380M	2.2B	17B
Chip Size-DRAM (mm2)	445	790	1580
Max wiring levels	7	7-8	9
Mask layers	23	24/26	28
Defect density-DRAM (D/m	875	490	250
Chip conections-I/O's	1195	1970	3585
Wafer diameter (mm)	300	300	450

Figure 10.1 SAI roadmap projections. *(Source:* Semiconductor International, *January 1998.)*

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width. The lithography requirement is characterized as the 1/2 pitch length of adjacent lines (Fig. 10.2). Another feature of future lithography processes is that the wavelength of the exposing radiation is larger than shown in Fig. 10.1. There are some future requirements that will drive lithography circa 2016. In most cases, the techniques required have yet to be defined.

In this chapter, some of the limits of optical imaging and advanced process solutions are presented. Also, industry developments extending optical lithography and development of NGL [called *next generation lithography* (NGL)] have proceeded on almost all of the individual elements of basic patterning processes. They include resist development, mask materials and designs, exposure sources (Fig. 10.2), alignment and exposure schemes, reflection control, and process schemes. In the present and future eras, lithography advances along the technology node scale will involve combinations of the factors listed. No single lithography process step is expected to provide a comprehensive breakthrough. Figure 10.3 illustrates major exposure systems identified for the future.

Resist. The general resist resolution problem is the wavefront that arrives at the resist layer. Simple cross-sectional drawings show the arriving rays as uniform arrows. The actual radiation in the wavefront has a mixture of directions and energies that vary across surface and in the vertical direction. This is called the *aerial image.*[4] Resolving one-half and one-third micron images with optical lithography requires management and manipulation of the aerial image. Control methods fall into three general areas: optical resolution, resist resolution limits, and surface problems. A fourth problem area is etch definition. Resist resolution is intimately mated to the exposure source and exposure system used. Basic resist formulation has improved with manufacturing control, matching the chemistry to the wavelength.

	DRAM level			
	4 kb	64 kb	256 Mb	64 Mb → 1 GB
Aligner type	Contact	Projection	Stepper	Stepper-scanner
Exposure	Hg	Hg	g, I line	KrF, Arf
Image	Mask	Mask	Reticle	Reticle

Figure 10.2 Patterning techniques versus DRAM level.

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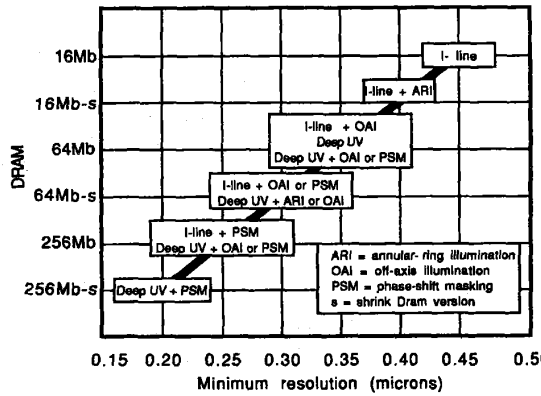


Figure 10.3 Lithography resolution process roadmap. *(Source:* Semiconductor International, *February 1993.)*

Chemically amplified (CA) resist moved the processes into 0.25-micron range. CA resists are considered the basic platform (with future improvements) to carry lithography to the 90-nm node and beyond. These resists, like older resists, are based on the photosensitive polymers, photoacid generators (PAGs), dissolution inhibitors, etch barriers, and an acid labile, base soluble group.[5] New resists must operate in the tougher etch environments of plasma etch. They not only must image the smallest features, usually gates, but also deal with imaging dense patterns and small metallization contacts. Additionally, etch *line edge roughness* (LER) becomes a factor as line size dimensions approach the size of the molecules in the resist.

Contrast effects

Good resolution becomes difficult in regions of the mask where an opaque line is surrounded by a large clear area. The large amount of radiation coming around the opaque line tends to shrink the dimension of the line in the resist layer (Fig. 10.4) as the exposing rays diffract around the edge of the pattern. This problem is called a *proximity effect.*

Another contrast effect is called *subject contrast* (Fig. 10.5). This situation comes about when some exposure radiation penetrates the opaque region of a mask or reflects off the wafer surface into the resist.

The result is a partially exposed region that leaves a distorted image after the development step. This is more a problem with negative resist than with positive resist.

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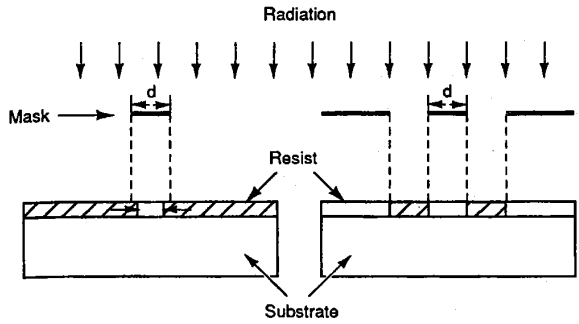


Figure 10.4 Proximity effects.

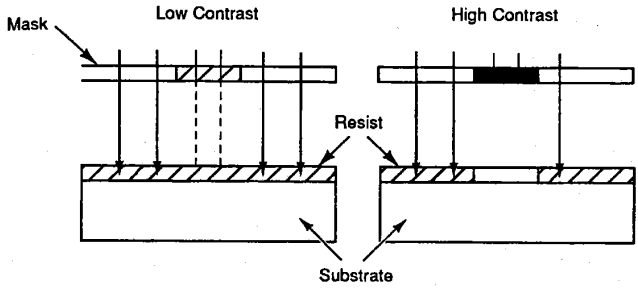


Figure 10.5 Subject contrast.

Exposure sources. Exposure sources are chosen to match the spectral response characteristic of the resist and the feature size of the images (see section on "Photoresist exposure speed, sensitivity, and exposure source"). Most optical aligner systems use a high-pressure mercury lamp, which produces light as a current is passed through a tube of mercury. A high-pressure atmosphere allows a higher level of stimulation of the mercury without evaporation.

The energy from the mercury comes out in bundles of waves grouped in ranges. Some resists are designed to react to the entire range of the wavelengths and some to specific wavelengths. Other resists are designed to respond to the specific high-energy peaks of a mercury lamp. The three peaks are at the 365-, 405-, and 436-nm wavelengths.

They are referred to as the 1, H, and G lines, respectively. Steppers used for advanced imaging often have filters to expose the resist to the G- or I-lines. I-line exposure has been the source of choice in the sub-

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micron era. The I-line has a wavelength of 365 nm (or 0.365 μm), which is near the image size for 0.350 products. The problem is the physical difficulty of resolving images smaller than the wavelength of the light.

The advantage of confining the exposure source to a narrow wavelength is to foster complete and faster exposure of the resist with little scattering. Narrowband exposure limits resolution problems associated with partial exposure of the resist at the clear/opaque edge on the mask. The exposure time is faster for a specific spectral resist, since the peaks represent higher-energy portions of the spectrum.

Resolution capabilities of the aligner and the resist are primarily a function of the wavelength of the exposing light. The smaller or narrower the exposing wavelength, the higher the resolution capability. This is due to the diffraction effect (Fig. 10.6). The longer the wavelength, the more the diffraction effect, which ultimately acts as a limit on the resolution capability of the system. Shorter wavelengths of light also carry more energy, allowing shorter exposure times and in turn limiting poor resolution coming from scattering of the light in the resist and from the wafer surface (Fig. 10.7).

Shorter ultraviolet wavelength peaks are in a region of the mercury lamp output spectrum called the mid- or deep ultraviolet (DUV). The peaks occur at 313 (mid UV) and at 254 nm (DUV). Deep- and mid-ultraviolet exposing sources are created by the use of filters with a standard ultraviolet source such as mercury-xenon, xenon, or deuterium lamps.[6]

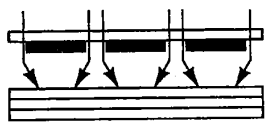


Figure 10.6 Diffracting reduction of image in resist.

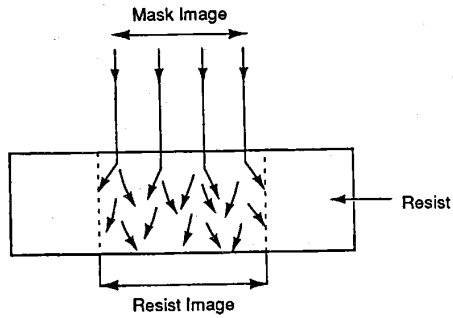


Figure 10.7 Light scattering in resist film.

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Excimer lasers. There are also DUV sources available from excimer lasers. The following gas lasers and their associated wavelength are used: XeF (351 nm), XeCl (308 nm), KrF (248 nm), ArF (193 nm).[7] Both KrF and ArF have been developed for above the 130-nm node processes, with ArF considered the source of choice for below 130-nm patterning.[8] F_2 is also considered a candidate to follow ArF.[9] Figure 10.8 shows the progression of exposure sources to pattern ever-smaller images.

Focused ion beams. The literature always includes the possibility of focused ion beams for photoresist exposure. The lure is less scattering of the beam and lower energy scattering in the resist, which should allow smaller and sharper images. Also, the energy of ion beams is higher than electrons, which could lead to faster exposure times. Unfortunately, development has been hampered by a host of production considerations, including vibration and ion-optical systems required for submicron imaging.[10]

X-ray. The desire for higher-resolution exposure sources inevitably led to the consideration of two nonoptical sources X-ray sources (Fig. 10.9) and electron beams (e-beams). X rays are high-energy photons with wavelengths of 4 to 50 Å.[11] This range of wavelengths is capable of very small image sizes (down to the 0.1-μm level) due to the lack of diffraction effects. X-ray aligners are projection systems using a full-size mask (1:1 mask to wafer image). They generally have higher

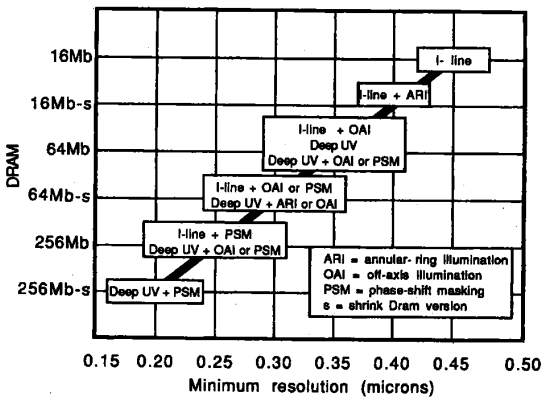


Figure 10.8 Lithography resolution process roadmap. *(Source:* Semiconductor International, *February 1993.)*

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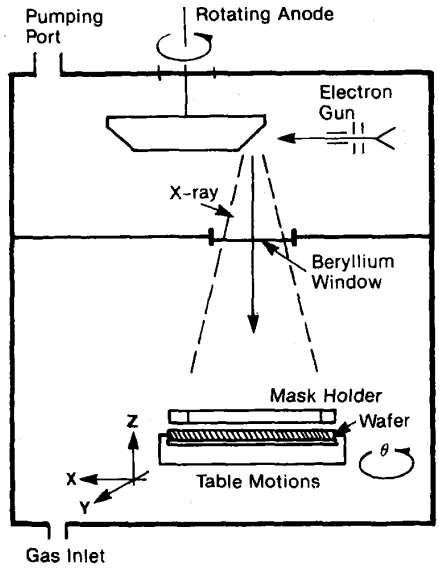


Figure 10.9 X-ray exposure system.

output through shorter exposure times. Reflection and scattering in the resist is minimum, and there are few depth-of-focus problems. X-ray-exposed wafers show a lower level of defects from dust and organic matter on the mask, because the X-rays pass through the spots.

A number of difficulties have surfaced with production-level X-ray aligners. A major problem has been with the development of X-ray blocking masks. Because X-rays pass through conventional chrome and glass masks, a process that requires gold as the blocking layer and other materials that stand up to the high energy of the X-rays needs to be developed (see "Maskmaking").

While development work goes on in defining X-ray equipment, it also goes on in developing X-ray resists. This work is complicated, because there is no standard X-ray source, and the resists must show high sensitivity to X-rays as well as being good etch barriers. These last two factors have proven difficult to balance in resist chemistries. Another barrier limits X-ray aligners to a 1:1 printing. The high-energy X-rays destroy conventional optics needed for reduction systems. And the limitation of reticle sizes means that only steppers are practical for production machines.

X-ray sources include standard X-ray tubes or laser-driven sources as point sources or synchrotron generators. Point sources are similar to conventional systems with one exposure source per machine. Synchrotrons are large, expensive machines that can accelerate electrons

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in an orbit. The orbiting electrons give off X-rays in a process called *synchrotron radiation.* As the X-rays rotate, they can be directed through ports to a number of individual aligners.

Electron beam. Electron beam lithography is a mature technology used in the production of high-quality masks and reticles. The system (Fig. 10.6) consists of an electron source that produces a small-diameter spot and a "blanker" capable of turning the beam on and off.

The exposure must take place in a vacuum to prevent air molecules from interfering with the electron beam. The beam passes through electrostatic plates capable of directing (or steering) the beam in the x-y direction on the mask, reticle, or wafer. This system is functionally similar to the beam-steering mechanisms of a television set. Precise direction of the beam requires that the beam travel in a vacuum chamber in which there is the electron beam source, support mechanisms, and the substrate being exposed.

There is no mask or reticle used to generate the pattern. With no mask, a source of defects and errors is eliminated along with the ex-

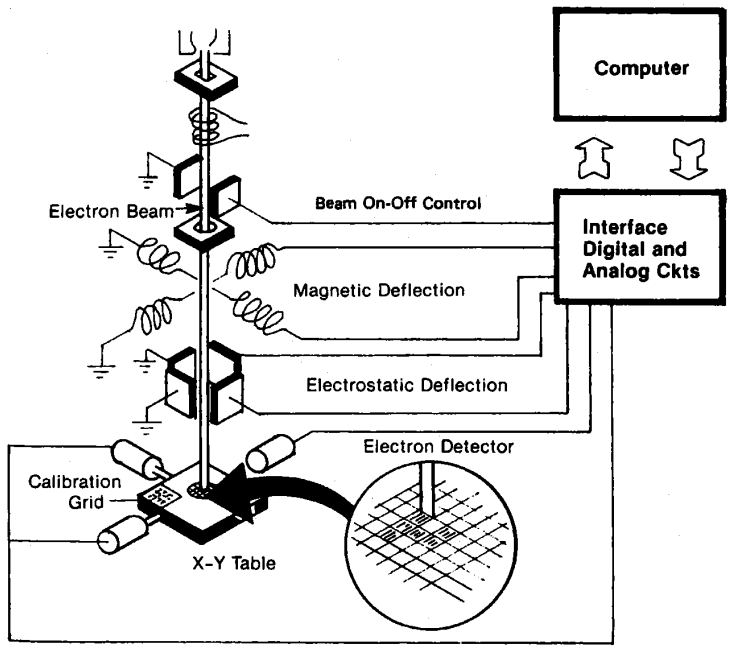


Figure 10.10 Electron beam exposure system.

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pense of the mask or reticle. The blanking and steering functions are controlled by a computer that has in its memory the wafer pattern taken directly from the CAD design stage. The beam is directed to specific positions on the surface by the deflection subsystem and the beam turned on where the resist is to be exposed. Larger substrates are mounted on an *x-y* stage and are moved under the beam to achieve full surface exposure. This alignment and exposure technique is called *direct writing*.

The pattern is exposed in the resist by either raster or vector scanning (Fig. 10.11). Raster scanning is the movement of the electron beam side to side and down the wafer. The computer directs the movement and activates the blanker in the regions where the resist is to be exposed. One drawback to raster scanning is the time required for the beam to scan, since it must travel over the entire surface. In vector scanning, the beam is moved directly to the regions that have to be exposed. At each location, small square or rectangular shaped areas are exposed, building up the desired shape of the exposed area.

Alignment and overlay parameters are very good with electron beam systems, because no distortions are introduced from masks or from optical effects such as diffraction. Resolution is also good, with current machines capable of 0.25-μm feature sizes.[9] Drawbacks to full use of electron-beam systems in wafer production are speed and cost. Current electron-beam aligners can expose fewer than ten 6-in diameter wafers per shift and cost several million dollars per system. A factor in the slowness of the system is the time required to create the vacuum and release it in the exposing chamber.

Other Exposure Issues

In Chapter 8, the issue of image resolution and exposure wavelength was explored. In general, the way to expose smaller images is to use a

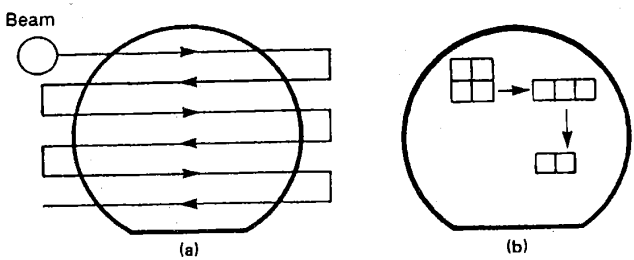


Figure 10.11 Electron beam scanning. (*a*) Raster scan and (*b*) vector scanning.

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smaller-wavelength exposure source. However, this leads to a smaller depth of field. In the sub-0.5-μm range, exposure processes extend from I-line to deep UV. The DOF problem requires other refinements, including variable numerical aperture lens, annular-ring illumination, off-axis illumination, and phase shift masks. In addition, there are other optical effects that come into play as the image size gets smaller and the pattern density gets larger. These issues and solutions are examined next.

Numerical aperture (NA) of a lens. In the example of the shadow image of the fork, distance was introduced as a resolution factor. In semiconductor imaging, there are contact/proximity exposure systems where the wafer and mask are touching or in close proximity (see "Contact, Proximity Aligners"). But most VLSI and ULSI products are exposed with projection systems where the mask/reticle and wafer are separated. Projection optics present particular problems. The challenge is to project the image from the mask/reticle to the wafer surface with as little loss of resolution or dimensional control as possible. Small image sizes require the use of short wavelengths. The minimum image that can be resolved on the wafer is constrained by the physical attributes of the projection optical system. One attribute is the numerical aperture (NA) of the projection lens. The NA is the ability of the lens to gather light. The relationship is:

$$\sigma = k\frac{\lambda}{NA}$$

where σ = the minimum feature size
k = a constant (sometimes called the Rayleigh constant)
λ = the wavelength of the exposing light
NA = is the numerical aperture of the lens

The term k (or k_1 in some formulas) relates to the ability of the lens (or total lithography system) to differentiate two adjacent images. Diffraction effects will cause even the most perfect lens to blur images as the get closer to each other. Values of k are about 0.5.

The formula suggests that decreasing the wavelength and/or increasing the NA are ways to print a smaller image size. Using deep UV, X-rays, or e-beams are ways to reduce the wavelength. However, there are limits to increasing the NA. That is because of a trade-off parameter called *depth of focus* or *depth of field*. In regular photography, we run into depth-of-field problems when the foreground is in focus and the background is out of focus, or vice versa. At the wavelengths

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used in patterning, even the micron-size topography on a wafer is enough to cause depth-of-field problems. Images, both on the top surface and at the bottom of valleys, must have good resolution and the correct dimensions. Another trade-off with increasing the *NA* is a decrease in the field of view. This is the same phenomenon experienced when going to a higher magnification with a zoom lens. At the higher powers, the breadth of the view is narrowed. Field of view becomes a production limit with steppers. A narrower field requires more time to complete exposure of the entire wafer.

All of these technical problems are complicated by the increasing amount of information that must be printed on advanced circuits. The technology driver product is the dynamic random access memory (DRAM). This product evolves about every three years to a new generation with four times more information. With feature size shrinkage, chip size increases, stacking of components, and better designs, three times more information (per square centimeter) is required of the masking process.[8] This trend pressures alignment makers, especially steppers, to develop ever more sophisticated lens systems, exposure sources, resists, and other image enhancement techniques such as light source improvements, phase shift masks, and so forth (see Chapter 10). These techniques effectively lower the constant k in the resolution limit formula above.

Variable numerical aperture (NA) lenses. The NA factor is an overall measurement of a lens's ability to gather light. The trade off is depth of field (DOF). A lens with a better ability to gather light (higher NA) suffers from a decreased depth of field (see Chapter 8). Unfortunately, advanced circuits have many layers and high and low points (*surface topography*) that require a large DOF. A stepper with one lens is limited to exposing wafers within its associated depth of field, which may or may not include the levels on the wafer surface. Newer steppers come with a variable NA lens, allowing their use over a wider range of DOF requirements.

Off-axis illumination. Shifting the direction of the exposure beam from the perpendicular (off-axis) interrupts the interference pattern that causes standing waves in the resist.

Lens issues and reflection systems. At the extremes of lithographic patterning shaping, the exposing beam through a lens system becomes an issue. The issue is absorption. An exposure system should deliver a specific wavelength (or bundle of controlled wavelengths) to the resist surface. The materials used for lenses can absorb radiation

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in the required ranges, and this becomes a serious problem below 193 nm. Calcium fluoride (CaF_2) is one material that is transparent in this radiation range, and it is expected to be used in the 157-nm node.[13]

Moving beyond optical lithography and into NGL, there are two primary candidates: extreme ultraviolet (EUV) and electron-beam projection lithography (EPL). EUV systems use a deep ultraviolet (DUV) source from the shorter end of that spectrum with a wavelength in the 10 to 15 nm range (Fig. 10.12). A projection system can more faithfully deliver the radiation to the wafer without the distortions that occur with lens systems. At the wafer surface, the e-beam is steered in a step-and-scan process.

The basics of an electron beam system have been described. Unfortunately maskless (raster or vector scanning) systems are too slow for patterning onto wafer surfaces. An advanced system using e-beam exposure is electron-beam projection lithography (EPL). This system uses an e-beam exposure source, a mask, and a scanning projection method (Fig. 10.13). A system developed by Lucent Technologies, called SCALPEL, uses a scattering mask. Electrons are highly energetic and pass through most materials. While conventional masks block portions of the exposing beam and allow other portions to pass through, a scattering mask allows passage of the e-beam through both segments. However, one part of the mask scatters the e-beam as shown. A reduction lens focuses the beam down toward the wafer. In between is an aperture that essentially allows the unimpeded beam to pass onto the wafer surface and blocks the scattered beams.

Current mask design for this system uses a multiplayer structure. The "pattern" is defined in a layer of silicon nitride that was deposited on a silicon wafer. Most of the wafer is etched away, except for silicon "struts" left to keep the mask rigid. This arrangement is mounted on a thin membrane. All of the parts of this mask are transparent to the e-beam. However, the pattern is defined because the incoming beam is broken into two components—scattered and nonscattered. Because

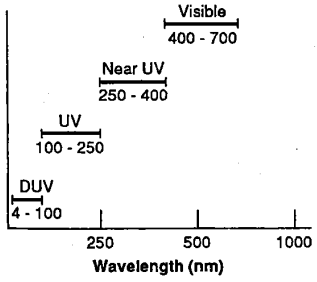


Figure 10.12 Ultraviolet and visible spectrum. *(After Elliott.[36])*

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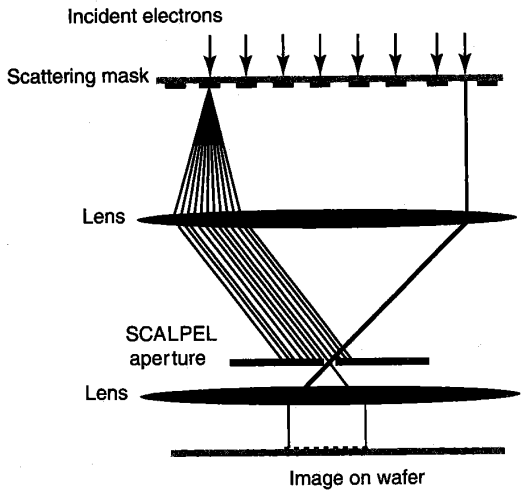


Figure 10.13 Basic SCALPEL principle of operation showing contrast generation by differentiating more or less scattered electrons. *(Bell Laboratories, Lucent Technologies web site.)*

this pattern is scanned onto the wafer surface, the struts do not come into the scanned pattern.

Phase shift masks (PSMs)

For conventional optical patterning, several techniques are used to improve image fidelity from mask to wafer. A diffraction problem occurs as two mask patterns get closer together. At some point, the normal diffraction of the exposure rays start touching, leaving the patterns unresolved in the resist. The blending of the two diffraction patterns into one is because all the rays are in the same phase. *Phase* is a wave term that relates to the relative positions of the peaks and valleys of a wave (Fig. 10.14). The waves in (*a*) are in phase, those in (*b*) out of phase. One way to prevent the diffraction patterns from wiping out two adjacent mask patterns is to cover one of the openings (Fig. 10.15) with a transparent layer that shifts one of the sets of exposing rays *out of phase,* which in turn nulls the blending. This approach to an *alternating phase shift mask* (also called *alternating aperture phase shift mask—AAPSM*) requires the deposition of a layer of silicon dioxide on the mask/reticle and a photomasking process to remove the oxide layer from alternate patterns. Covering every other

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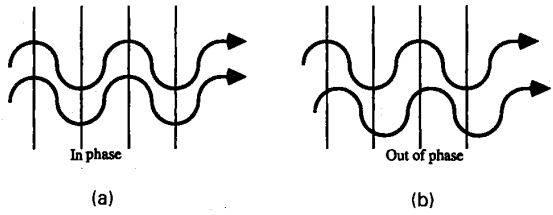


Figure 10.14 *Wave phases.*

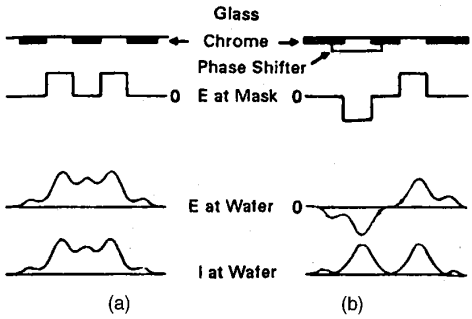


Figure 10.15 Light intensity patterns. (*a*) Without phase shifting and (*b*) with phase shifting. *(Source:* VLSI Fabrication Principles, *by Ghandhi.)*

clear opening works well for repeated array patterns such as those found in memory products.

Another solution is the addition of phase shifting layers to the edges of the mask/reticle patterns. This process also requires a oxide deposition and full masking process. There are several variations for this approach. They are subresolution (or outrigger) and rim phase shift masks.[14]

Optical proximity corrected or optical process correction (OPC)

It is known that, in the sub-0.5-μm range, a perfect image on the mask/reticle can, from proximity effects, result in a distorted pattern in the resist. OPC masks attempt to reverse that situation by having a distorted image on the mask/reticle that is designed to produce a perfect image in the resist. Situations that are particularly vulnerable are dense patterns of adjacent open/opaque regions and the shortening and/or rounding of pattern corners such as small contact holes. A computer is used to analyze exposure process conditions (contrast ef-

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fects) and design the on-mask pattern shapes.[15] An example of the correction of an end rounded pattern is shown in Fig. 10.16. Another technique is *double masking.* The first mask, a phase mask, creates part of the pattern in the resist. A follow-on mask, a trim mask, is somewhat oversized and completes the desired pattern.[16]

Annular ring illumination

Annular ring illumination is a technique that was first introduced in Perkin Elmer scanning projection aligners. One of the guns in the resolution arsenal is a more uniform exposing light. Unfortunately, conventional optical exposure sources produce a light spot that is too nonuniform for small image exposure. However, within the spot, there are areas (rings) of more uniform energy. An annular ring illuminator blocks off all but a *ring* portion of the spot, directing a more uniform wave of exposing radiation to the wafer.

Pellicles

The development of projection exposure systems (projection aligners and steppers) brought with them an increased mask and reticle lifetime. With the increased lifetime came the incentive to make higher quality masks and reticles. In a production line where masks are used for a long time, wafer-sort yield loss comes from dirt and scratches picked up during handling and use. One source of damage comes from mask and reticle cleaning steps. This situation is a "Catch-22." The

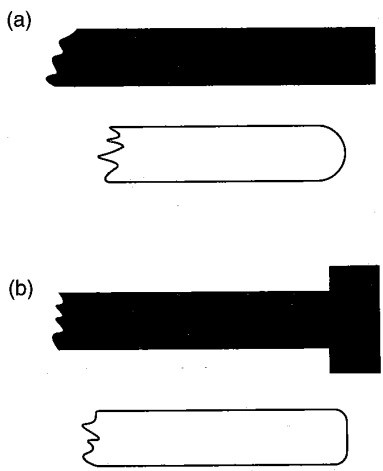


Figure 10.16 (*a*) Conventional image formation and (*b*) image enhancement with use of mask image "hammerhead."

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masks and reticles become dirty during the process and require cleaning. The cleaning procedure then itself becomes a source of contamination, scratches, and breakage.

A solution to these problems is a pellicle (Fig. 10.17). A *pellicle* is a thin layer of an optically neutral polymer stretched onto a frame. The frame is designed to fit onto the mask or reticle. The pellicle is fitted to the mask or reticle after the mask is made and cleaned. Once in place, the pellicle membrane is the surface collecting any dirt or dust in the environment. The height of the membrane above the mask surface holds the dirt particles out of the focal plane of the mask. In effect, the particles are transparent to the exposing rays.

Another benefit of a pellicle is the elimination of scratches from the mask surface, since the surface is covered. A third benefit is that, once pelliclized, a mask or reticle does not need in-process cleaning. For some applications, the pellicle membrane is given an antireflective coating, which assists in the imaging of small geometries, especially on reflective wafer surfaces. These benefits translate into wafer-sort yield increases of 5 to 30 percent.[17]

Pellicle membranes are made from either nitrocellulose (NC) or cellulose acetate (AC). NC films are used in exposure systems with broadband exposure sources (340 to 460 nm)[18] while AC films are used in mid-ultraviolet applications. The membranes are thin (0.80 to 2.5 μm) and must show a high transmission rate for the rate exposure wavelengths. A typical pellicle will exhibit over a 99 percent transmission rate for the peaks of the exposing wavelengths. Pellicle effectiveness requires stringent thickness control, on the order of ±800 Å, and control of particles to less than 25 μm in diameter.

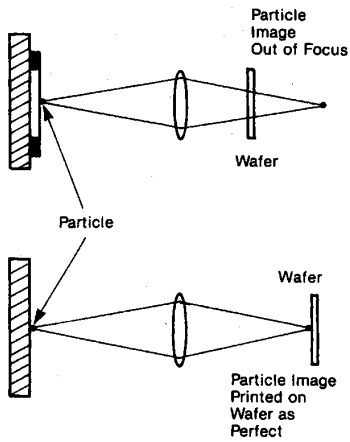


Figure 10.17 Pellicle.

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A pellicle membrane is made by a spin casting technique. The pellicle material is dissolved in a solvent and spun onto a rigid substrate, such as a glass plate. This is the same technique used to spin photoresist onto wafers. Thickness of the membrane is controlled by the viscosity of the solution and the spin speed of the spin coater. The membrane is removed from the substrate and fixed onto the frame. Frame shapes are determined by the size and shape of the mask or reticle. Cleanliness control requires class 10 or better cleanrooms and antistatic packaging.

Surface Problems

The resolution of small images is affected by several conditions on the wafer surface. Reflections off the surface layers, increasing variation of the topography, and the etching of multilayer stacks all require special process steps or "tweaking" of the process.

Resist light scattering

In addition to light radiation reflecting off the wafer surface, the radiation tends to diffuse into the resist causing poor image definition. The amount of diffusion is in proportion to the resist thickness. Some additives put in the photoresist to increase radiation absorption also increase the amount of radiation diffusion, thus reducing image resolution.

Subsurface reflectivity

The high-intensity exposing radiation ideally is directed at a 90° angle to the wafer surface. When this ideal situation exists, exposing waves reflect directly up and down in the resist, leaving a well defined exposed image (Fig. 10.18). In reality, some of the exposing waves are traveling at angles other than 90° and expose unwanted portions of the resist.

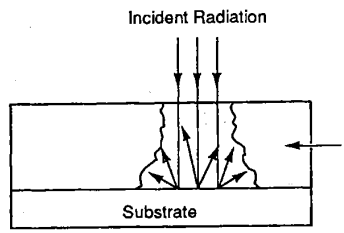


Figure 10.18 Subsurface reflectivity.

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This subsurface reflectivity varies with the surface layer material and the surface smoothness. Metal layers, especially aluminum and aluminum alloys, have higher reflectivity properties. A goal of the deposition processes is a consistent and smooth surface to control this form of reflection.

Reflection problems are intensified on wafers with many steps, also called a varied topography. The sidewalls of the steps reflect radiation at angles into the resist, causing poor image resolution. A particular problem is light interference at the step that causes a "notching" of the pattern as it crosses the step (Fig. 10.19).

Antireflective Coatings

Antireflective coatings (ARCs) spun onto the wafer surface before the resist (Fig. 10.20) can aid the patterning of small images. The ARC layer brings several advantages to the masking process. First is a planarizing of the surface, which makes for a more planarized resist layer. Second, an ARC cuts down on light scattering from the surface into the resist, which helps in the definition of small images. An ARC can also minimize standing wave effects and improve the image contrast. The latter benefit comes from increased exposure latitude with a proper ARC.

An ARC is spun onto the wafer and baked. After the resist is spun on top of the ARC, the wafer is aligned and exposed. The pattern is developed in both the resist and the ARC. During the etch, the ARC acts as an etch barrier. To be effective, an ARC material must transmit light in the same range as the resist. It must also have good adhesion properties with the wafer surface and the resist. Two other require-

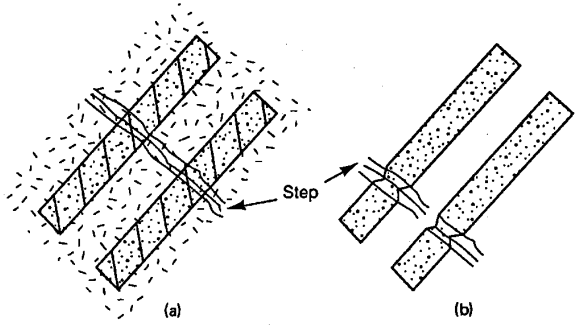


Figure 10.19 Metal line "notching" over step. (*a*) Before etch and (*b*) after etch.

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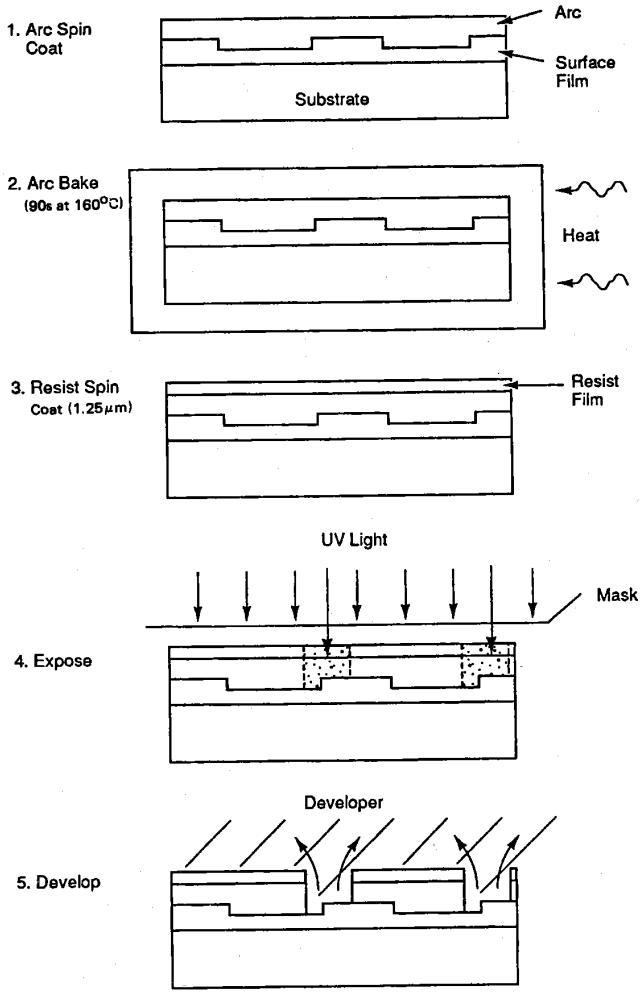


Figure 10.20 Antireflective process sequence.

ments are that the ARC must have a refractive index that matches the resist, and the ARC must develop and be stripped in the same chemicals as the resist.

There are several penalties associated with the use of an ARC. One is an additional layer requiring a separate spin and bake. The resolution gains offered by an ARC can be offset with poor thickness control

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and/or an ill-controlled developing step. The time of exposure can increase 30 to 50 percent increasing the wafer throughput time. ARC layers may also be used as the intermediate layer in a trilayer resist process or used on the top of the photoresist (top antireflective coating, or TAR).

Standing waves

In the "Subsurface reflectivity" section, it was mentioned that the ideal exposure situation is when the radiation waves are directed to the wafer surface at 90°. This is true when only reflection problems are under consideration. However, 90° reflection causes another problem in positive photoresists—the creation of standing waves. As the radiation wave reflects off the surface and travels back up through the resist, it interferes constructively and destructively with the incoming wave, creating regions of varying energy (Fig. 10.21). The result, after development, is a rippled sidewall and a loss of resolution. A number of solutions are used to moderate standing waves, including dyes in the resist and separate antireflective coatings directly on the wafer surface. Most positive resist processes include a post-exposure bake (PEB) step before development of the resist layer. The bake reduces the influence of standing waves on pattern sidewall definition.

Planarization

The advancement of circuits to VLSI levels has been brought about by both increased surface density and more surface layers. As the various layers are etched into patterns, the surface becomes stepped into high and low plateaus. The plateaus are delineated by steps each with dif-

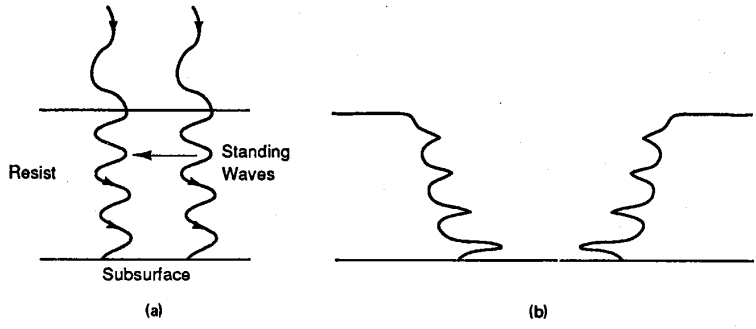


Figure 10.21 Standing-wave effect. (*a*) During exposure and (*b*) after develop.

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ferent reflection qualities. The resolution of submicron (especially 0.5 μm and smaller) images on this type of surface is not possible in a simple one-resist layer process. One problem is depth-of-field issues. A limited-DOF lens cannot resolve images on both the high and low plateaus. Another is light reflection at the steps causing the notching of metal lines (Fig. 10.22). A number of *planarization* techniques are used to offset the effects of a varied wafer topography. Techniques include multilayer resist processing, planarization layers, reflow techniques, and physically flattening the surface by chemical-mechanical polishing. Current focus is on the global flattening of the surface (CMP) to allow patterning with only one resist layer. However, the multilayer resist processes described are still useful during the transition.

Photoresist Process Advances

The ten-step lithography process detailed in Chapters 8 and 9 is based on a single photoresist layer, and it assumes that the layer can resolve the required images without pinholes or failing during the etch process. The nanometer era has forced the development of variations to the single resist layer process. These processes are usually used in conjunction with the advances in exposure control described previously.

Multilayer resist/surface imaging

There are a number of multilayer resist processes. The choice of a process depends on the size of the resist opening and the severity of the surface topography. While multilayer resist processes add the penalty of more process steps in some situations, they are the only reliable means of creating the desired images. A multilayer resist process features a thicker bottom layer that serves to fill in the valleys and pla-

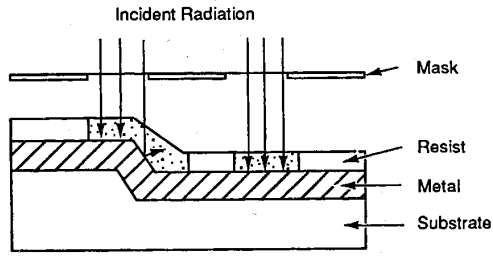


Figure 10.22 Light reflection at steps.

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narize the surface. The image is first formed in a layer of photoresist on the top of the planarizing layer(s). This *surface imaging* allows small dimension imaging because the surface is flat, i.e., away from reflecting steps and in the same plane to avoid DOF problems.

A dual multilayer resist process uses two layers of photoresist, each with a different polarity. The process is suited to resolve small geometries on wafers with a varied topography. First, a relatively thick layer of resist is applied and baked to the thermal flow point (Fig. 10.23). A typical thickness is three to four times the highest step height on the wafer. The goal is a planar top resist surface. A typical multilayer process will use a positive-acting polymethylmethacrylate (PMMA) resist sensitive to deep ultraviolet radiation.

Next, a thin layer of positive resist, sensitive only to ultraviolet radiation, is spun on top of the first layer and processed through the development step. The thin top layer allows the resolution of the pattern without the adverse effects encountered with thick resist layers or reflections from steps in the surface. Since the top layer conforms to the shape of the bottom layer, it is referred to as a *conformal layer* or *por-*

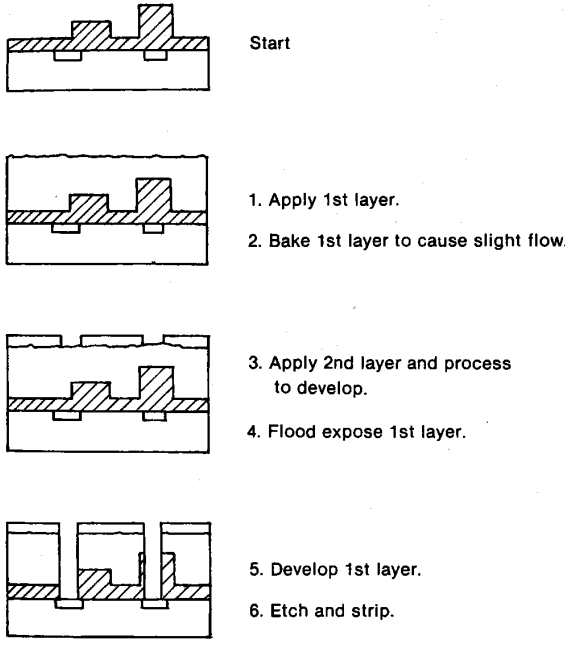


Figure 10.23 Dual-layer photoresist processing.

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table conformal layer. This top layer of resist acts as a radiation block, leaving the bottom layer unpatterned. Next, the wafer is given a blanket or flood (no mask) deep ultraviolet exposure, which exposes the underlying positive resist through the holes in the top layer, thus extending the pattern down to the wafer surface. A development step completes the hole resolution and the wafer is ready for etch.

Considerations in the choice of photoresists are compatibility of the two resists through the process, reflection problems from the subsurface, standing waves, and sensitivity problems with PMMA resists.[13] In addition, the two resists must have compatible bake processes and independent developing chemistries.

Variations on the basic dual-level resist process include dyes in the PMMA and the use of antireflection layers under the first resist layer. Many variations on the basic dual-level process are practiced. One use of a dual-layer resist process is as a lift-off technique. By adjusting the development of the bottom layer, an overhang can be created that assists in the clean definition of the metal line on the surface (Fig. 10.24).

A trilevel resist process (Fig. 10.25) incorporates a "hard" layer between the two resist layers. The hard layer may be a deposited layer of silicon dioxide or other developer-resistant material. As in the dual-layer process, the image is formed in the top photoresist layer. Then, the image is transferred into the hard layer by a conventional etching step. The finishing step is the formation of the pattern in the bottom layer, using the hard layer as an etch mask. The use of a hard intermediate layer makes possible the use of nonphotoresist bottom layers such as a polyimide layer.

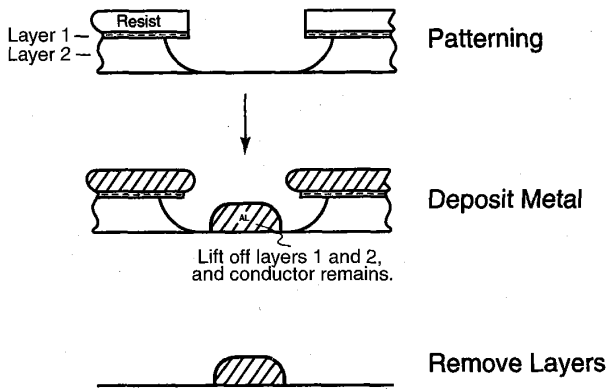


Figure 10.24 Dual-layer resist lift-off process.

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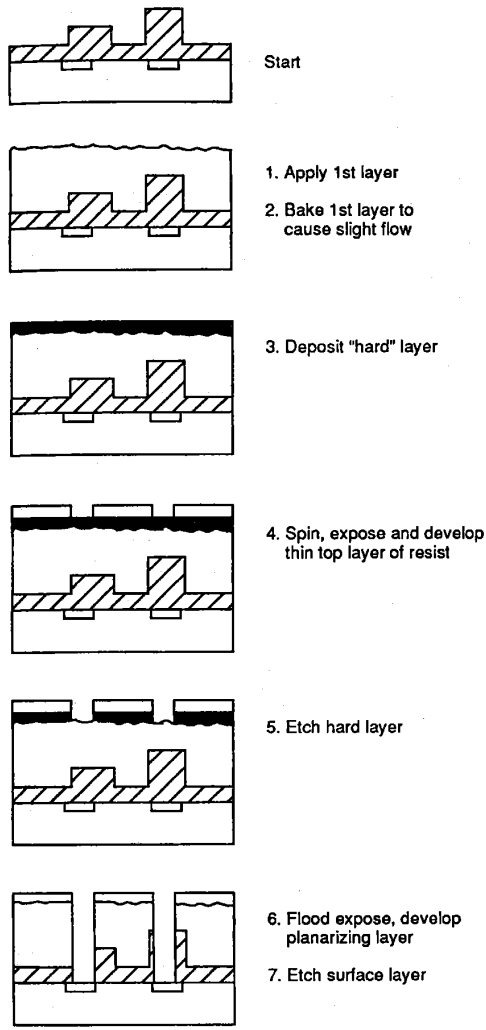


Figure 10.25 Trilevel resist process.

Silylation/DESIRE process

A novel approach to surface imaging is the diffusion enhanced silylating resist (DESIRE) process[20] (Fig. 10.26). Like other multilayer resist processes, the concept is to planarize the wafer and form the image in

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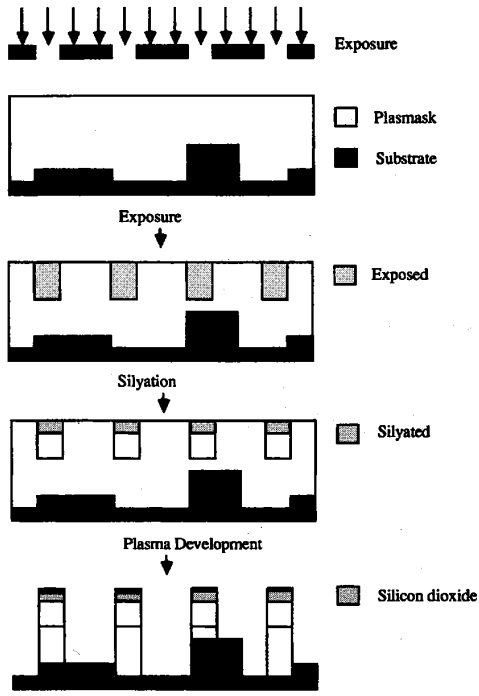


Figure 10.26 DESIRE process. *(Source:* Solid State Technology, *June 1987.)*

a surface layer. The DESIRE process uses on layer exposed by a standard UV exposure. In this process, the exposure is confined to the top layer of the planarizing layer. Next, the wafer is placed in a chamber (see vapor prime baking)[21] for exposure to HMDS for a *silylation process*. During this step, silicon becomes incorporated into the exposed areas. The silicon-rich areas become a hard mask, allowing the dry development and removal of the underlying material with an anisotropic RIE etch (Chapter 9). During the etch step, the silylated areas are converted to silicon dioxide (SiO_2), forming a more resistant etch mask. Techniques relying on defining the pattern in the top most layer are called *top surface imaged* (TSI).

Polyimide planarization layers

Polyimides have been used for years in printed circuit board manufacturing. For semiconductor use, the polyimides offer the dielectric

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strength of deposited silicon dioxide films and the process advantage of application to the wafer with the same spinning equipment used for photoresist.[22]

Once applied to the wafer, the polyimides flow over the surface, making it more planar. After application and flow, the polyimide can be covered with a hard layer and patterned with chemicals much like a photoresist. A popular use of polyimide layers is as an interdielectric layer between two layers of conducting metal. The planarizing effect of the polyimide makes the definition of the second metal layer easier.

Etchback planarization

Etchback is used for local planarization (Fig. 10.27). After metal lines are defined, a thick oxide layer is deposited and a photoresist layer spun on top of the oxide. Etch takes place in plasma etcher. First, the thinner resist etches away and starts etching the oxide. Later, the thicker resist etches away and some oxide is removed. The net result is a local flattening of the surface.

Dual-damascene process

Increased component density has forced the use of multimetal layers. Their use required the need for connecting conductors called *studs* or *plugs*. Tungsten is the preferred metal, but there are complications in

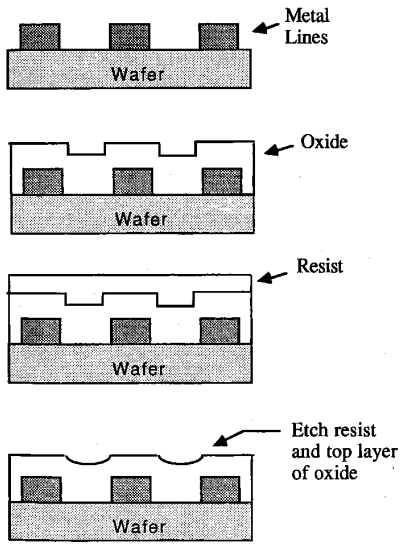


Figure 10.27 Etchback planarization.

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etching tungsten. Also, copper has become the preferred metallization system, replacing aluminum. However, copper technology introduces a whole host of process issues. One is the replacement of the traditional image and etch processes with a process called *dual-damascene.* It is an inlaid process similar in principle to the inlaid metal processes of antiquity. In that process, grooves are made in the surface of a bowl or other object. A metal is applied to the entire surface, also filling the groove. After the excess metal on the surface is removed, some remains in the grooves, leaving a decorative pattern. In the semiconductor application, the grooves are created with lithography techniques and the copper deposited by electroplating. The metal deposition process overspills the surface. A *chemical mechanical polishing* (CMP) step is used to remove the overspill, leaving the metal isolated in its trench (Fig. 10.28). Chapter 13 has a more detailed discussion on this new and important patterning technique.

Chemical mechanical polishing (CMP)

Each of the previously described planarization techniques tends to smooth out the surface but does not produce a totally flat surface (*global planarization*). Small-dimension images with most planarization techniques are still difficult to define because of light scattering. They also can cause metal step coverage problems at the steps. The chemical mechanical polishing process used to flatten wafers in the wafer preparation stage (Chapter 3) is also used for the global planarization of in-process wafer surfaces.

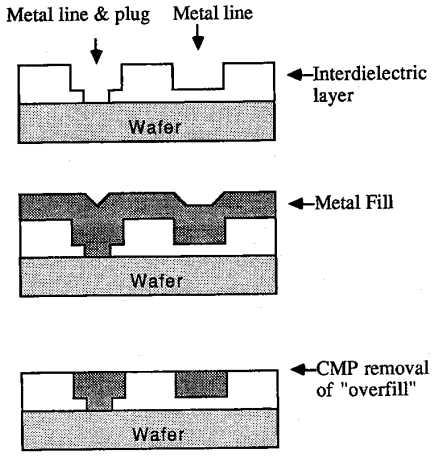


Figure 10.28 Dual-damascene (inlaid) process.

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CMP is favored because of its ability to:[29]

- Achieve *global planarization* across the entire wafer
- Polish and remove all materials
- Work on multimaterial surfaces
- Make possible a high-definition damascene process and copper metallization
- Avoid the use of hazardous gases
- Be a low-cost process

The same basic process is used for both wafer polishing and planarization (Fig 10.29). However, the challenges are very different. In wafer polishing, several microns of silicon is removed. In metallization processes, CMP is required to remove amounts of material on the order of a micron or less. Also, these metal processes present a number of materials for removal. They have different removal rates and high expectations of uniform planarization. These issues are addressed in Chapter 13.

Basic CMP processing steps. A wafer is mounted upside down on a carrier, which, in turn, is mounted, wafer face down, onto a rotating platen. The platen surface is covered with an polishing pad. A *slurry* carrying small abrasive particles is flowed onto the platen. The particles attack and remove small pieces of the wafer surface, which are carried away be the movement of the slurry across the surface. The combined actions of the two (orbital) rotations and the abrasive slurry polish the wafer surface. High plateaus on the wafer are polished first and faster than the lower areas, thus achieving planarization. These are the mechanical polishing actions. However, mechanical polishing alone is unacceptable for semiconductor processing due to excessive mechanical damage to the surface. Damage is reduced and/or managed by selecting a slurry chemistry that dissolves or etches the surface materials. Chemical removal generally requires the corrosion of the surface, usually through an oxidation mechanism. An analogy would be the rusting of iron, which is chemical corrosion. A layer of rust forms when iron is exposed to oxygen. However, the layer of rust slows down the rusting process by blocking the iron surface from the oxygen in the water or air. This is where the chemical and the mechanical work together. The abrasive particles wipe away the corrosion layer, exposing a fresh surface for corrosion, and the process repeats itself continuously. Following CMP, there is a *post-CMP cleaning* required to maintain wafer cleanliness.

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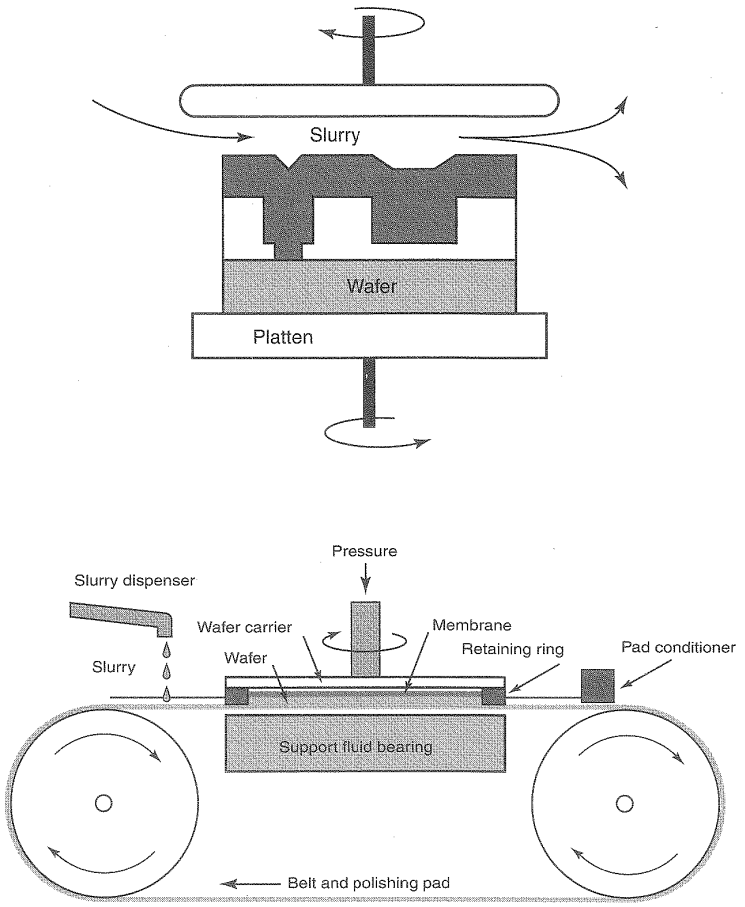


Figure 10.29 Chemical mechanical polishing and planarization (CMP).

Linear CMP systems are also used. In this arrangement, the wafer carriers are rotating over a moving belt instead of a rotating platen. A chief advantage of linear systems is the increased speed of the slurry movement under the wafer.

Primary measures of performance after a CMP process are:

- The surface flatness
- Surface mechanical condition
- Surface chemistry

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- Surface cleanliness
- Productivity
- Cost of ownership (see Chapter 15)

Polishing pads

Polishing pads are made of cast polyurethane foam with fillers, polyurethane impregnated felts, or other materials with special properties. Important pad properties are porosity, compressibility, and hardness.[24] Porosity, usually measured as the specific gravity of the material, governs the pad's ability to deliver slurry in its pores and remove material with the pore walls. Compressibility and hardness relate to the pad's ability to conform to the initial surface irregularities. Generally, the harder the pad, the more global the planarization. Softer pads tend to contact both the high and low spots, causing nonplanar polishing. Another approach is flexible polish heads that allow more conformity to the initial wafer surface.[31]

Slurry

Slurry chemistry is complex and critical as a result of its dual role. On the mechanical side, the slurry is carrying abrasives. Small pieces of silica (silicon dioxide) are used for oxide polishing. Alumina (Al_2O_3) is a standard for metals. Multimetal surfaces found in multimetal layer schemes (Chapter 13) are challenging the industry to identify more "universal" abrasives. Abrasive diameters are kept in the 10 to 300 nm size[32] to achieve polishing, as opposed to grinding, which uses larger-diameter abrasives but causes more surface damage.

On the chemical side, the etchant would be KOH or NH_4OH (basic solutions with low ph levels) for silicon or silicon dioxide. For metals such as copper, reactions usually start with an oxidation of the metal from the water in the slurry. A typical reaction is:

$$2CU + H_2O—Cu_2 + 2H^+ + 2^-$$

Following the oxidation, the basic materials chemically reduce the film, which is removed by the mechanical actions.

Various additives are found in production slurries. They perform various roles. Reducing post-CMP surface residues is addressed by balancing the ph of the slurry to control electrical charges on the 0^{28} abrasive particles. Silica-based slurries have high ph levels, while silica slurries have a ph below 7. Other additives are surfactants to establish desired flow characteristics and chelating agents. These latter

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agents interact with metal particles to reduce their redeposition on the wafer surface.

Other factors critical to a planar polish are the ph (degree of acidity or alkalinity), the flow dynamics at the wafer/pad interface, and the etch selectivity of the slurry on different surface materials and underlying layers.

Polishing rates

A primary production measure is the polishing rate. Many factors influence the rate. Pad material parameters already described, the slurry types and size, and the chemicals and their properties used for corroding the surface are important factors. Other process factors include the pad pressure, the rotation rates, the flow rate of the slurry, the flow property (viscosity) of the slurry, and the temperature and humidity in the polishing chamber. Wafer diameter, pattern sizes, and surface materials are also factors. All of these factor must be balanced to achieve a productive polish rate (go faster) without creating an out-of-control process (go slower).

Planarity

Global planarity is the goal of CMP, but the advent of multimetal schemes challenges that goal. Copper is a particular issue and illustrates several of the basic problems. Copper deposition into the trenches of a damascene patterning system (Fig. 10.30) results in lower density in the center. During the CPM process, the center polishes faster leaving a dish shape. Also, copper deposition density differences in dense patterns results in differential polishing across the pattern.

Tungsten plugs are also a CMP challenge (Fig. 10.31). During the initial CMP, the tungsten surface ends up recessed below the surrounding oxide. An oxide buff is required to planarize the surface.[32]

In some copper metallization schemes, tantalum is used as a diffusion barrier in trenches to keep the copper from diffusing into the silicon. However, the tantalum polishes much more slowly than copper (in a copper oriented slurry), leaving the copper surface exposed to more polishing time and more dishing.[28]

Pattern geometry variations result in differential removal rates. Larger areas tend to be removed faster, leaving dishing of low spots on the surface.

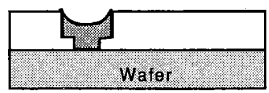


Figure 10.30 "Dishing" of copper in trench.

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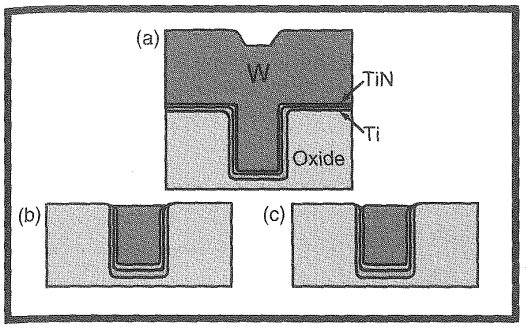


Figure 10.31 Tungsten plug formation. (*a*) Deposit W, (*b*) CMP removal, and (*c*) buff oxide layer. *(Reprinted from the April 1998 edition of* Solid State Technology, *copyright 1998 by PennWell Publishing Company.*

Also challenging is the presence of metals of different hardness, which polish at different rates, and interdielectric layers (IDL) of polymer materials that are soft. With all the challenges, by the year 2010, wafer surfaces will have to be flat down to the 150-nm range.

Post-CMP clean

The critical role of clean wafer surfaces has been stressed throughout this book. It is just as important after CMP, and there are some particular challenges. CMP is the only process that intentionally puts particulates on the surface; namely, the abrasive particles. These are usually removed with mechanical brush cleaners or high-pressure water jets. Chemical cleaning generally employs the same techniques used for other FEOL cleaning.

Carefully choosing slurry surfactants and adjusting the ph can create an electrical repulsion between the slurry particles and the wafer surface. This technique can reduce contamination, particularly of the types that become electrostatically attached to the surface.

Copper contamination is a particular concern. If it gets into the silicon, it changes and diminishes electrical operations of the circuit components. Copper residues should be reduced to the 4×10^{13} atoms/cm^2 range.[30]

CMP tools

Operating a successful CMP process requires a sophisticated integrated system more than the simple polishing unit (Fig. 10.32). Production-level tools include automatic wafer handling robots, on-board

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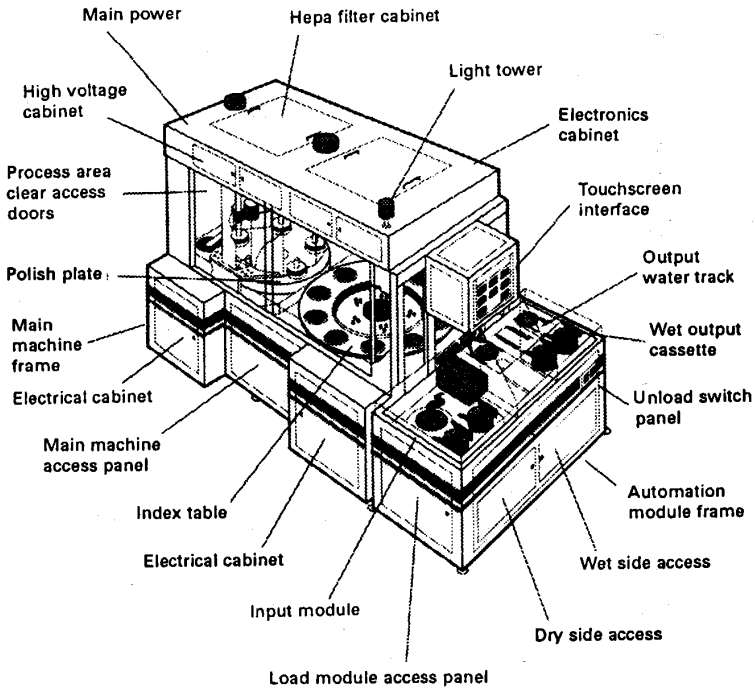


Figure 10.32 CMP System. *(Source: SpeedFam CMP-V system,* Semiconductor International, *May 1993.)*

metrology, and cleanliness detectors. Various end-point detection systems are used to signal when a particular layer material is gone or a specific removal depth is reached. Post-CMP cleaning units may be included in the main cabinet or mated to the primary CMP unit by robots in a cluster design. The goal is a "dry-in, dry-out" process.

CMP Summary

CMP is a critical planarization process that requires a high level of integration and balancing of many process parameters. The primary parameters are: polishing pad composition, polishing pad pressure, pad rotation speed, platen rotation speed, slurry flow rates, slurry chemistry, and slurry material selectivity. In addition to planarization for lithography improvements, CMP is the enabling process for dual-damascene patterning and copper metallization. This application is further explored in Chapter 13.[25]

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Reflow

Some device schemes use a hard planarizing layer or layers. A popular layer is a deposited silicon dioxide doped with about 4 to 5 percent boron, called boron silicate glass (BSG). The presence of the boron causes the glass to flow at a relatively low temperature (less than 500°C), creating a planarized surface.

Another hard planarizing layer used is a spin-on-glass (SOG) layer. The glass is a mixture of silicon dioxide in a solvent that evaporates quickly. After spin application, the glass film is baked, leaving a planarized silicon dioxide film. The glass as spun is brittle,[26] and some formulas contain between 1 and 10 percent carbon to increase resistance to cracking.

Image reversal

The preference for positive resists over negative resists for small geometry patterning has been discussed. One of the advantages with positive resists is the use of dark-field masks for the imaging of holes. Dark-field masks offer a lower-defect process, because the majority of the surface is covered by hard chrome that does not damage like glass. However, some mask levels require the printing of islands rather than holes. Metal mask levels are island patterns. Unfortunately, the printing of an island with a positive resist requires the use of a clear-field mask with its glass damage potential.

A process that allows the printing of islands with positive resists and dark-field masks is image reversal, which involves the formation of the image in the resist with a dark-field mask by conventional masking steps (Fig. 10.33). At the conclusion of the exposure step,

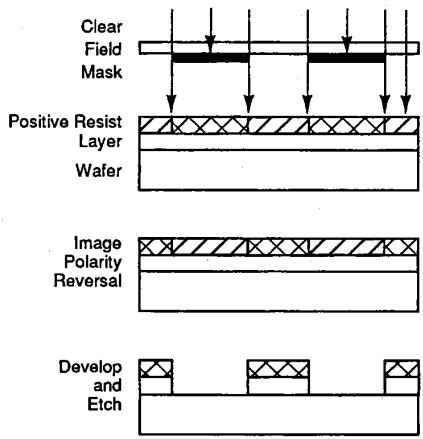


Figure 10.33 Image reversal.

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there is an image in the resist that is reversed from the desired image. That is, if the resist was developed, a hole rather than an island would be formed.

The image reversal process involves exposing the resist-covered wafer to amine vapors in a vacuum oven. The vapors penetrate the resist, reversing its polarity. On removal of the wafers from the oven, they are given a flood exposure which completes the reversal process. The effect of the amine bake and flood exposure is to change the relative dissolution rates of the exposed and unexposed regions, thus reversing the original image when the resist is finally developed. This process is capable of the same resolution capabilities as a nonreversed positive process.[33]

Contrast enhancement layers

Optical projection system resolution is approaching the limits imposed by the constraints of the lens and the wavelength of the exposing radiation. The two set up a condition in which the resist *contrast threshold* becomes the limiting factor. This is because, at short exposure times and ultraviolet and deep ultraviolet energies, the energy of the exposing wave varies in intensity. Thus, the image formed in the resist is fuzzy.

A method used to decrease this threshold is a contrast enhancement layer (CEL), which is a layer spun on top of the resist that is initially opaque to the exposing radiation (Fig. 10.34). During the exposure cycle, the CEL becomes bleached (transparent) and allows the radiation to pass into the underlying photoresist. The CEL responds first to the higher intensities before turning transparent, in effect storing the lower intensities before turning transparent. The result is that the resist receives a uniform exposure of high-intensity radiation, which improves its resolution capability. Another way to imagine the role of the CEL is as the top layer of a dual-layer resist system with the image being formed in the thin top layer.

Before the resist is developed, the CEL is removed by a chemical spray and development of the resist proceeds by normal processing. Positive resist processes normally capable of 1.0-μm resolution can achieve a 0.5-μm image with a CEL.

Dyed resists

Various dyes may be added into the resist during manufacture. A dye may have one or several effects during the exposure step. One possible effect is the absorption of radiation, thereby attenuating the reflected radiation and minimizing standing wave effects. Another is a change of the dissolution rate of the resist polymer during development. This

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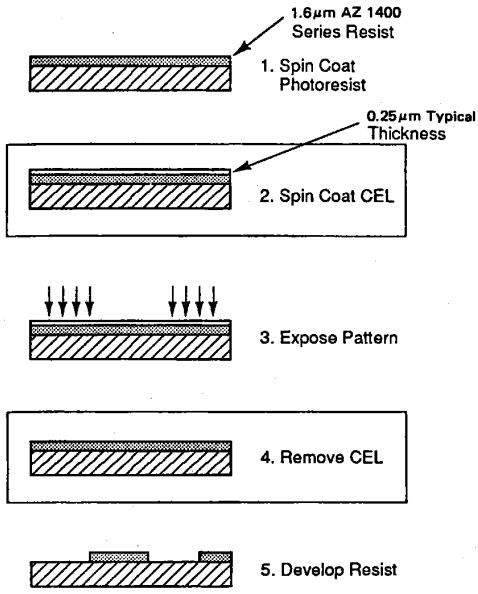


Figure 10.34 Contrast enhancement layer process flow.

effect creates a cleaner developed line (increased contrast).[34] An important use of dyes is the elimination of the notching that occurs in thin lines of deposited material crossing over surface steps. Addition of a dye to a resist can cause an increase in exposure time of 5 to 50 percent.[35]

Improving Etch Definition

Forming the correct image in the photoresist is a critical step, but not the only step that defines the image in the wafer surface. Etching must also be controlled and precise. Several techniques are available that provide improved etch definition.

Lift-off process

The final dimensions of the images in the surface layer are the result of variations in both the exposure step and the etch step. In processes where etch undercutting (resist adhesion) is a problem, such as aluminum etching, the etch component of the dimensional variation can be the dominant one.

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A patterning variation that eliminates the etch variation component is lift-off (Fig. 10.35). In this variation, the wafer is processed through the development step, leaving a hole in the resist layer where a deposited layer is to be located. The exposure and development steps are adjusted to create a negative slope in the sidewall of the hole.

Next, the wafer receives the deposited layer, which covers the entire wafer and fills in the hole. Definition of the pattern comes when the wafer is processed through a photoresist removal step that lifts off the resist and unwanted metal layer. Usually, the removal step is assisted by ultrasonic agitation. This helps form a clean break of the deposited film at the resist edge. After resist and film removal, the desired pattern is left on the wafer surface.

Self-Aligned Structures

Overetching has the effect of placing two structures closer together than intended. There is always some amount of overetching, and the alignment of some structures is absolutely critical. One solution is the *self-aligned structure,* such as a MOS gate (Chapter 16). The definition of the gate structure also defines the neighboring source/drain regions (Fig. 10.36). Opening the source/drain regions is a simple procedure of dip etching the oxide off the source/drain regions. The thinner oxide on the source/region allows a short etch time that does not allow enough time to etch the sides of the gate structure. The subsequent source/drain doping places the dopants next to the gate. This basic technique

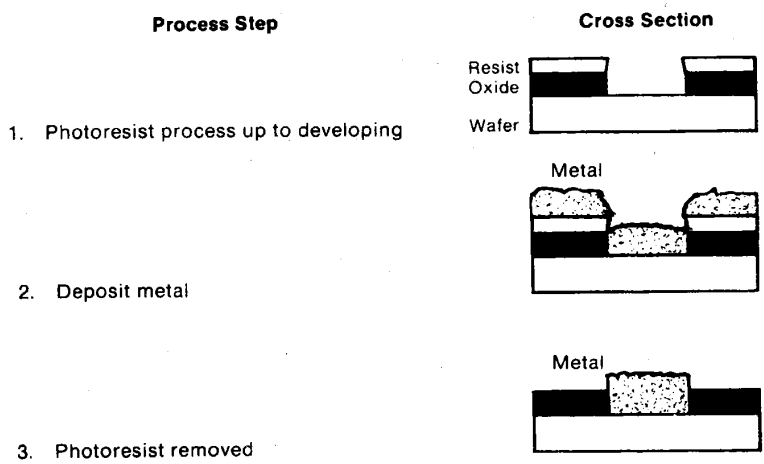


Figure 10.35 Lift-off.

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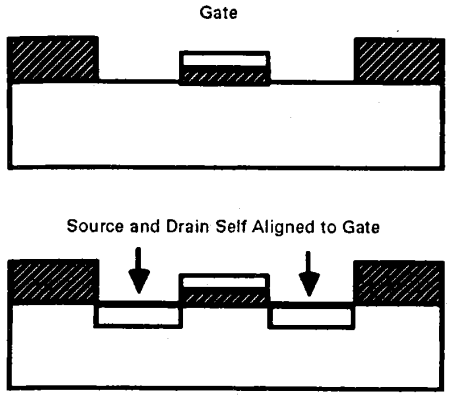


Figure 10.36 Self-aligned silicon gate (SAG) structure.

of a differential oxide thickness and dip etch is used to define/etch other structures. The design uses the gate structure as a doping block.

Etch Profile Control

In Chapter 9, the concept of anisotropic etching was explained as a way of producing vertical (or near vertical) etched side walls. The problem becomes more complicated when the etched layer is actually a stack of different materials (Fig. 10.37). Use of an etchant that has poor selectivity can produce a stack with varying widths (Fig. 10.37*b*). Profile control for multilayer etches becomes a trade-off of the etchant chemistry, power levels, and the system pressure and design.

Review Questions

1. What is a contrast effect, and how does it affect an image?
2. Name two problems resulting from subsurface reflection.

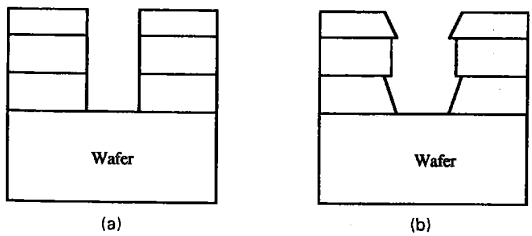


Figure 10.37 (*a*) Anisotropic and (*b*) isotropic etch of surface layer "stack."

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3. What is the purpose of the top layer of a multilayer resist process?
4. What is the purpose of the bottom layer of a multilayer resist process?
5. What is flood exposure, and at what step is it used in a multiresist process?
6. What basic resist process step is eliminated in a lift-off process?
7. What advantages come from a planarization surface?
8. How does a contrast enhancement layer improve resolution?
9. How does a pellicle improve the wafer sort yield?
10. Explain the advantage of a self-aligned structure and give an example.

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