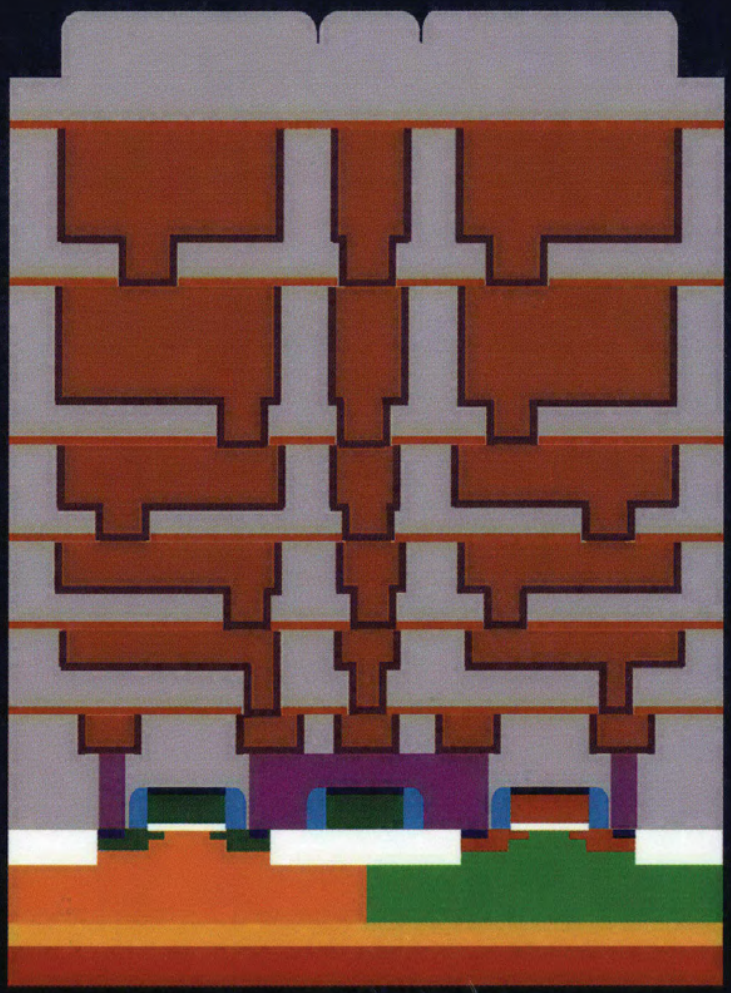
Silicon Processing

for the VLSI Era

Volume 4 - Deep-Submicron Process Technology



S. Wolf

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SILICON PROCESSING FOR THE VLSI ERA

VOLUME 4:

DEEP-SUBMICRON PROCESS TECHNOLOGY

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PREFACE

With the dawn of the new millennium, IC technology-nodes have evolved beyond 0.18-micron. New processes also had to be developed to meet the needs of this *Deep-Submicron Era,* including: copper/low-*k* dual-damascene interconnects; high-*k* MOSFET-gate and DRAM dielectrics; 300-mm wafers; chemical-mechanical polishing (CMP); excimer-laser-based DUV-lithography; chemically-amplified (CA) resists; silicon:germanium (Si:Ge); and silicon-on-insulator (SOI).

The semiconductor industry, however, also experienced an economic decline of unprecedented severity at the start of the 2000 decade. It seams clear that to fuel the recovery, chip manufacturers will have to exploit the above innovations. Such processes are a path to achieving the performance goals of future IC technology-nodes that will be needed for manufacturing new and profitable electronic products.

This is the *first available book dedicated exclusively to describing such deep-submicron process technologies* (including those listed above). It is intended to provide semiconductor engineers and researchers with a comprehensive, state-of-the-art reference about these emerging and leading-edge processes. While many other books have been written about the "traditional" IC fabrication processes, none offer what this volume contains. It's sole focus is those techniques needed to *manufacture chips for 0.18-μm (and smaller) generations*. Thus, it belongs on the shelf of every microelectronic professional whose livelihood depends on having a thorough grasp of the latest advances in IC fabrication techniques. There is no faster way to gain this information. As with our other volumes, owners will find themselves referring to this text again and again!

Readers can still consult Vol.1, 2nd Edition for background material on basic IC fabrication modules, as this book (Vol. 4) does not repeat that information. Instead, it presents over 800 pages of new content about the process technologies of the 2000's. It also has over 900 references (with 200 of these being published since 2000), and more than 500 illustrations. It is written in the same lucid, user-friendly style that has been widely praised in the other volumes of *Silicon Processing for the VLSI Era.*

As with the previous volumes, this text was produced using an accelerated book-production schedule. By employing revolutionary publishing techniques made available in the 1990's, Lattice Press can turn a finished manuscript into a published text in less than 3 months (a task that takes most publishers of technical books 15-18 months). This allows our books to be released faster, and to contain the most-up-to-date information at the time of publication.

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SILICON PROCESSING FOR THE VLSI ERA is a multi-volume treatise designed to provide a comprehensive and up-to-date treatment of this important and rapidly changing field. The volume in hand is the fourth in the series. Volume 1 (*Process Technology*, 2nd Edition) was published in 2000 and deals with individual processes employed in the fabrication of silicon ULSI circuits (such as silicon wafering, thermal oxidation of silicon, CVD and PVD of amorphous and polycrystalline films, diffusion and ion implantation of dopants in silicon, microlithography, and patterning technology). Volume 2 (*Process Integration*) was released in 1990, and describes how the individual processes of Volume 1 are combined in various ways to produce MOS and bipolar VLSI and ULSI circuits. The task of integrating these various fabrication processes together is referred to as *process integration.* In Volume 3 (*The Submicron MOSFET,* published in 1995) the topics of submicron MOSFET device physics and the relationship between such device physics and submicron MOSFET fabrication are addressed.

A book of this length and diversity would not have been possible without the indirect and direct assistance of many others. From an indirect perspective, virtually all of the information presented here is based on the research efforts of countless numbers of scientists and engineers. Their contributions are recognized to a small degree in citations of their articles given in the references at the end of each chapter. The direct help was also provided by many people, and the resulting text is thus significantly better. The author expresses heartfelt thanks to those who gave their time, energy, and intellect.

Important direct help came from members of my immediate family. My wife, Carrol, read the manuscript for grammatical and stylistic correctness. My son, Ross, designed the cover and improved many of the graphics. My daughter, Jennifer, helped in marketing the book. Thus, it truly represents a family enterprise.

Stanley Wolf

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Chapter 1

THE EVOLUTION OF THE STRUCTURE OF MOSFETS

The silicon MOSFET is the most important active-device in ULSI integrated circuits. Over the past 30 years, MOSFET dimensions have been decreasing at a dramatic rate - from gate lengths of 10-μm in the early 1970s to less than 0.13-μm today. This gate-length scaling is expected to continue, and may reach 0.05-μm (50-nm) at the end of the projected shrink path in 2012. Table 1-1 shows the predicted scaling of MOSFETs according to the 2001 IRTS Roadmap.[1]

MOSFETs are the dominant devices in Si ICs largely because they can be scaled to increasingly small dimensions, and this scaling results in higher performance. However, the structure of the MOSFET has undergone many changes besides the scaling of feature sizes down to the deep-sub-micron regime of today.

Figure 1-1 shows a SEM of a MOSFET with a gate length of 2-μm (Fig. 1-1a, circa 1985), and also of a MOSFET with a gate length of 0.2-μm (Fig. 1-1b). With the exception of being scaled, the basic structure of the MOSFET does not appear to be fundamentally changed. However, several aspects of the MOSFET device structure have been modified. (This can be better illustrated in schematic drawings that depict MOSFET cross-sections with a 1.5-μm gate length and a 0.18-μm gate length, see Fig. 1-2.) In this chapter the structure of deep-sub-micron MOSFETs is compared to those of technology generations in which the gate length exceeded 1.0-μm. In this discussion the term *deep-submicron MOSFET* refers to MOSFETs with a *gate length of 0.25-μm or smaller.* How the structure of CMOS devices must be reconfigured when building ICs using devices whose minimum sizes are in the deep-submicron regime is also covered.*

* By 2001, several novel MOSFET structures were being studied as alternatives for the "conventional" MOSFET when it's scaling limits are reached. Such new structures include the *vertical-*, the *replacement-gate-*, and *double-gate-MOSFETs.* However, by 2002 these structures (and others) were still in their infancy. It is not likely that they will be put into production for many years. The focus of this text, however, is on process technology that is in (or about to be put into) mainstream IC manufacturing lines in the 2001-3 timeframe. Thus, these novel structures will not be described here further. However, readers interested in more data on such futuristic MOSFETs should see such recent reviews as Ref. 8, and the *Technical Digests* of the *IEEE International Electron Devices Meetings* (*IEDM*), and *Digests of Technical Papers* of the *Symposium VLSI Technology.*

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Table 1-1 PRINTED GATE LENGTHS OF MOSFETS ITRS2001[1]

	2001	2002	2003	2004	2005	2006	2007
PRINTED GATE LENGTH (nm)	90	75	65	53	45	40	35

The purpose of this chapter is to show how the MOSFET structure has had to be changed when deep-submicron integrated circuits were fabricated. The device physics details that underlie the need for building such deep-submicron MOSFET structures are not presented here. While some of such information is found in later chapters, a more in-depth discussion of this topic is left to other texts (such as Vol. 3 of this series,[2] and elsewhere.[3])

1.1 THE STRUCTURE OF DEEP-SUBMICRON MOSFETS: (0.25 μm to 0.13 μm) COMPARED TO EARLIER-GENERATION MOSFETS: (2.0 μm to 0.5 μm)

In this section the structures of deep-submicron MOSFETs of the 2001-2002 timeframe (i.e., with gate lengths from 0.25 μm down to about 0.13 μm) are compared to those fabricated in the late 1980s and early 1990s (i.e., with gate lengths that ranged from 2.0 μm down to about 0.5 μm).

The following parts of the MOSFET will be examined, to see how the device structure had to be modified in order to allow high-performance deep-submicron MOSFETs to be implemented:

1. MOSFET gate-stack and contact structure;
2. Gate dielectric materials for the MOSFET;
3. Doping-concentration profiles of the MOSFET channel;
4. Drain structure of the MOSFET.

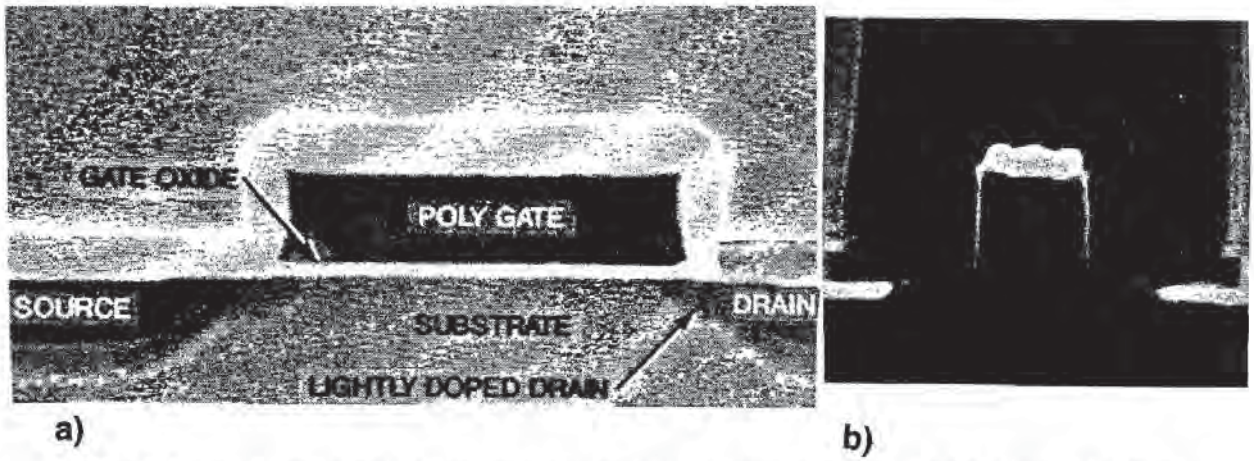


Fig. 1-1 SEMs of MOSFET cross-sections with different gate lengths: a) 2.0 μm; b) 0.2 μm.

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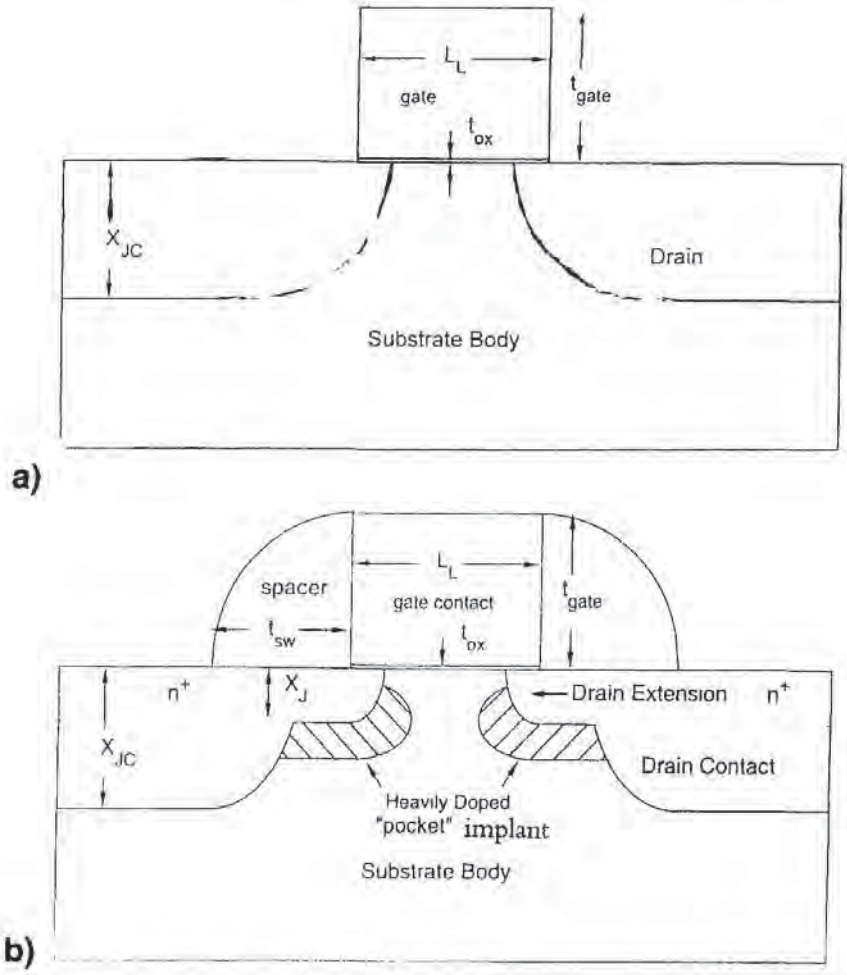


Fig. 1-2 Schematics of MOSFET cross-sections with different gate lengths: a) 1.5 μm; b) 0.2 μm.

Note that in CMOS ICs there are some additional structural aspects of the integrated circuit that must be considered besides those pertaining to the active device (MOSFET) structure. That is, the characteristics of the following two CMOS elements must also be addressed: **1**) the on-chip interconnect system; and **2**) the substrate and isolation structures. The issues relating to the substrate and the isolation structures will be considered in the following section of this chapter, while general issues related to the interconnect system are covered in Chap. 12.

1.1.1 Evolution of the MOSFET Gate Stack and Contact Structure

MOSFETs have used polysilicon as the gate material since the mid-1970s (i.e., when the polysilicon-gate structure replaced metal [Al] gates). The gate material in earlier MOSFETs for both NMOS and CMOS technologies down to about

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0.35-μm was n^+-doped poly (usually heavily doped with phosphorus - see also the following section on CMOS technology for more information on poly doping). However, as the MOSFET gate lengths were scaled below about 1.25-μm, the resistance of the polysilicon lines became too large for them to be effective in their secondary role as a local interconnect (even when they were doped as heavily as possible). At that point it became necessary to clad the top surface of the poly film with a metal silicide layer (most commonly WSi_x). This multi-layer gate *stack* was called a *polycide structure* (see Chap. 13 for more details on WSi_x polycides). Use of the polycide gate stack structure allowed the resistance of lines implemented with heavily-doped poly to be reduced by about a factor of four. Implementing WSi_x polycides thus permitted the use of single-level-metal interconnects in MOS-based ICs to be extended for one or two more technology nodes. (Note that the polycide structure is not shown in Fig. 1-2a, but is shown in Fig. 13-1.)

In deep-submicron CMOS, the silicide atop the poly layer is no longer WSi_x. Instead it is replaced with $TiSi_2$ or $CoSi_2$. These two silicides have lower resistivities than WSi_x. In addition, $TiSi_2$ or $CoSi_2$ can be simultaneously formed on the source and drain contact-regions at the same time they are formed on the poly lines. MOSFETs with a silicide on both the poly and the source/drain contact regions are said to contain a *self-aligned silicide* (or *salicide*) structure (as shown in Fig. 1-2b). The salicide structure provides two main benefits to the MOSFET: **1**) the poly lines have a lower resistivity due to the presence of the silicide; and **2**) the contact region exhibits a smaller contact resistance and sheet resistivity as compared to a contact region that does not have such a silicide. The details of the salicide formation processes, and the comparison of titanium silicides and cobalt silicides for this role are described in Chap. 13.

1.1.2 Gate Dielectric Materials in Deep-Submicron MOSFETs

Thermally grown SiO_2 has been used as the gate dielectric material for over 30 years (ever since MOSFETs ICs were first introduced). The thickness of this oxide has been continuously scaled to improve the MOSFET drain current and to control short-channel effects. The gate-oxide thickness has been approximately linearly scaled with channel length, with the ratio of gate length L_E to oxide thickness t_{ox} being maintained at approximately 45 (i.e., $L_E/t_{ox} \sim 45$).[4] For example, a 200-Å gate-oxide thickness was used in MOSFETs with a gate length of 1.0-μm, and a 40-Å gate-oxide thickness was used for 0.18-μm MOSFETs.

It is predicted that SiO_2 will continue to be used as the gate dielectric in MOSFETs until about 2004-2005. At that point (for MOSFETs with a gate

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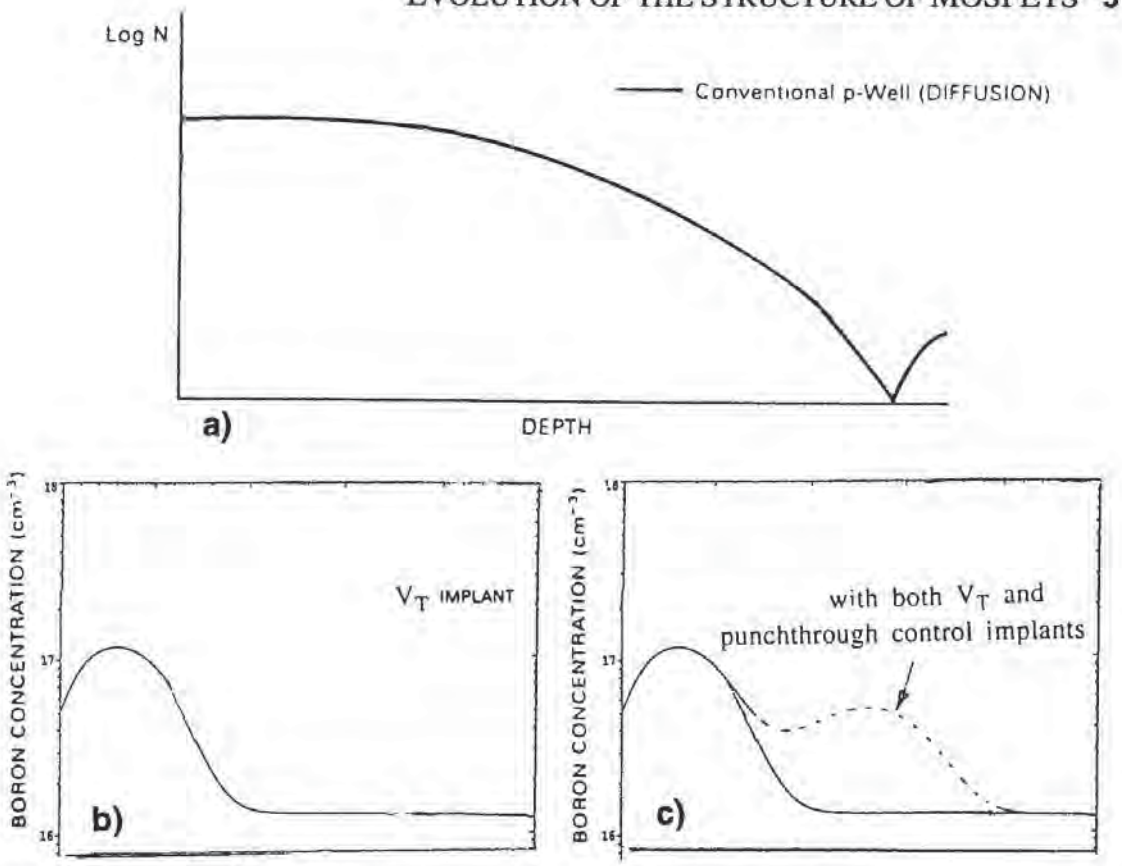


Fig. 1-3 a) Doping profile in a conventional diffused CMOS well; b) Doping profile in the CMOS well with a threshold-adjust implant; c) Doping profile in a CMOS well with a threshold-adjust implant *and* an anti-punchthrough implant.

length of 0.1 μm), the required oxide thickness will be less than 20-Å (assuming the same ratio L_E/t_{ox} is maintained). However, when the oxide reaches a thickness of less than 20Å, the gate-to-channel tunneling leakage-current will become approximately as great as the off-state source-to-drain leakage-current of the MOSFET (~10-nA/μm). As a result, it may not be feasible to build logic MOSFETs (i.e., not even high-performance-logic MOSFETs) with SiO_2 gate dielectric layers thinner than about 20-Å. Other devices (e.g., DRAM capacitors, or oxides used in non-volatile memory structures) will face even more stringent oxide thickness limitations. Such limits to gate oxide thickness are considered in more detail in Chap. 3.

To allow the gate lengths of MOSFETs to continue to be scaled below 0.1 μm, it seems it will be necessary to use alternative high-*k*-dielectric materials instead of SiO_2. With these materials, thicker dielectric layers can be used, and yet the same inversion layer characteristics can be maintained. These thicker layers result in less carrier tunneling, and thus they permit further scaling. The use

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of high-k dielectrics as alternative gate-dielectric materials is discussed in Chapter. 4.

1.1.3 Doping-Concentration Profiles of the MOSFET Channel

In earlier MOSFETs the channel region had a doping concentration profile (prior to the V_T-adjust implant) that is initially relatively flat with respect to depth below the silicon/oxide interface. In NMOS technology, this flat profile exists because the starting-substrate Si-wafers in which the NMOSFETs are fabricated are uniformly doped. In CMOS technology, the initial flat doping profiles are created from the processes used to create "conventional" CMOS well regions. That is, in such processes the well dopant is introduced into the silicon wafer near its surface using a shallow implant step. Then a long, high-temperature drive-in process diffuses these dopants away from the silicon surface, resulting in a doping profile that is relatively constant with depth near the silicon surface (see Fig. 1-3a). A V_T-adjust implant (using boron for both NMOS and PMOS) is then carried out to provide a doping profile as shown in Fig. 1-3b. As the NMOSFET approached 1-μm in gate length, a blanket anti-punchthrough boron implant was also carried out (typically following the V_T-adjust implant step). This caused a doping profile to exist in the channel as shown in Fig. 1-3c (and the MOSFET structure as in Fig. 1-2a).

In deep-submicron MOSFETs, the doping profile in both the vertical direction (i.e., in depth from the silicon surface) and in the lateral directions (i.e., along the channel) is changed from that which existed in earlier MOSFETs. Consider the profiles in the vertical and lateral directions separately.

In the *vertical direction*, the doping profile in the channel of deep-submicron MOSFETs has a so-called *super-steep retrograde* (SSR) shape (see Fig. 1-4). Such an SSR channel doping is needed to allow the correct value of the threshold voltage of the MOSFET to be achieved, while avoiding a degradation in the mobility of the carriers in the channel (due to excessively high dopant concentrations near the silicon/oxide interface - where the inversion layer exists). That is, it is desired to keep the doping density at the silicon surface to $<5x10^{17}/cm^3$. Such an SSR doping profile can be obtained by implanting a heavier dopant species than B for n-channel devices (typically In is used to replace B), and a heavier dopant species than P for p-channel devices (either As or Sb can be used). These species have a smaller diffusivity than either B or P, respectively, and thus the impurity profile does not get spread out during the

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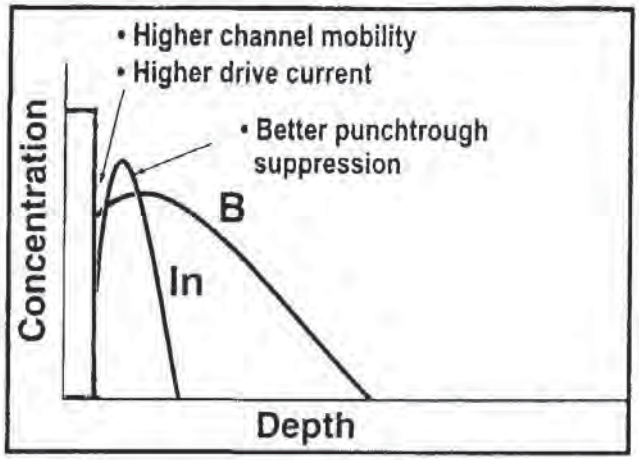


Fig. 1-4 As-implanted doping concentration profiles of threshold-adjust-implants with B and In as the implant species. The In implant produces a super-steep retrograde (SSR) profile.

subsequent heat cycles used to activate the implanted dopants. By choosing the correct implant energy and annealing cycles after implant, an appropriate SSR channel doping profile can be created. Chapter 5 covers this topic in more detail.

In the *lateral direction* (i.e., in the direction along the channel from the source to the drain), there is now also a non-uniform doping profile. That is, in the advanced "conventional" MOSFETs, a blanket implant for improving the punchthrough (PT) performance of the MOSFET is employed. Since this implant is a blanket process, the impurities that it introduces are in uniform concentration in the lateral direction of the channel (as shown in Fig. 1-2a). However, for deep-submicron MOSFETs, such blanket PT implants cause performance degradation.

To avoid these problems (and yet maintain the benefits provided by the blanket anti-punchthrough implant), the same dopant species is introduced in another fashion. As shown in Fig. 1-2b, the dopant is introduced only in selected, local regions; namely at the edge of the drain-extension region. This leaves much of the channel length with a lighter doping that is needed for a low V_T.

As the schematic drawing of Fig. 1-2b depicts, this extra dopant region surrounds the edge of the drain extension much like a halo surrounds the head of an angel in medieval paintings. Hence, this localized anti-punchthrough region has been termed a *halo anti-punchthrough structure*. Such a halo structure was originally produced (ca. 1985) by performing a second implant after the implant that created the lightly doped drain region (LDD - see Sect. 1.4.1). The halo implant is again self-aligned to the gate (and with the beam direction normal to the wafer surface). The same implant species as that already present in the well. is introduced by the halo implant, and it uses an energy that is somewhat higher than that used for the LDD implant. Thus, the range and lateral straggle of this

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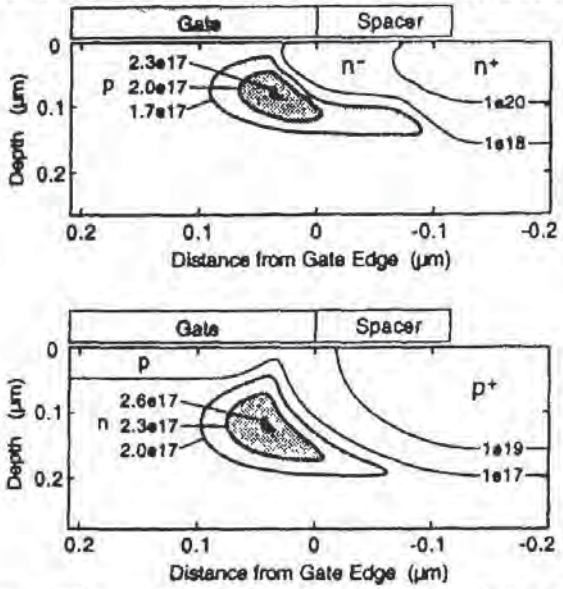


Fig. 1-5 Doping concentration contours resulting from a LATIPS implant.[7]

second implant will be greater than that of the first, resulting in the formation of a halo region as shown in Fig. 1-2b.

In more-advanced-technology generations, this second implant step is carried out with the ion beam directed at a high angle to the wafer surface. This allows the peak concentration of the implanted impurities to be located at a precise depth and lateral distance from the edge of the gate. Such an implant process has been named *large angle tilted implanted punchthrough structure* (*LATIPS*), or alternatively a *pocket implant.* Such lateral tailoring of the channel doping profile provides some additional design space to control V_T and punchthrough. Figure 1-5 shows the doping concentration contours resulting from such a LATIPS process, and more details on LATIPS are given in Chap. 5. These LATIPS (or pocket) implants, however, may be difficult to control at small dimensions.

1.1.4 Evolution of the Drain Structure of MOSFETs

When MOSFETs were first implemented in ICs, gate lengths were on the order of 10-μm. For MOSFETs with such long channel lengths, the drain-side of the *pn* junction at the drain end of the channel consisted of a simple single-region drain structure (Fig. 1-6a). As the gate lengths grew smaller than about 2.0–μm, the electric field in the depletion region of this drain *pn*-junction grew so large that it started to produce severe hot-carrier injection effects (HCI). These HCI effects caused long-term reliability-degradation in MOSFETs, and they had to be curtailed. The technique used to suppress HCI effects was to replace the single-region drain structure with a two-region drain structure (Fig. 1-6b). The two-region drain structure consisted of a region that was in contact with the MOSFET

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channel (and extended under the edge of the gate) and a second region that was further from the channel (but was connected to the first region). To reduce the electric field near the drain, the first region was more lightly doped (~10^{17}/cm^3) compared to the second region (~10^{20}/cm^3). The name given to this two-region drain structure is the *lightly doped drain* (or *LDD*).

The process sequence for forming this structure is as follows: **1**) After patterning the gate stack, the lightly doped drain region is formed with an ion implantation step using a medium-current implanter. The gate is used to align the drain dopant with that of the gate edge, forming the LDD region; **2**) A spacer is formed (by CVD of a dielectric film, followed by an anisotropic-etch step that leaves a spacer structure along the sidewalls of the gate); **3**) A high-current implanter is next used to introduce the dopants for the second heavily-doped drain-contact-region (with the spacer preventing these species from being implanted into the LDD region); and **4**) An anneal step activates the dopants implanted in both steps and drives the edge of the lightly doped region the proper distance beneath the edge of the gate.

In deep-submicron MOSFETs, the drain structure has been modified from the 2-region LDD-drain described above. The reason for this change is that the power-supply voltage has been reduced as MOSFET dimensions were scaled (primarily because gate oxide thicknesses have become thinner, and such thin oxides cannot withstand the oxide electric fields that exist at the higher supply voltage values – see Chap. 3). For MOSFETs at 0.18-μm, the power-supply

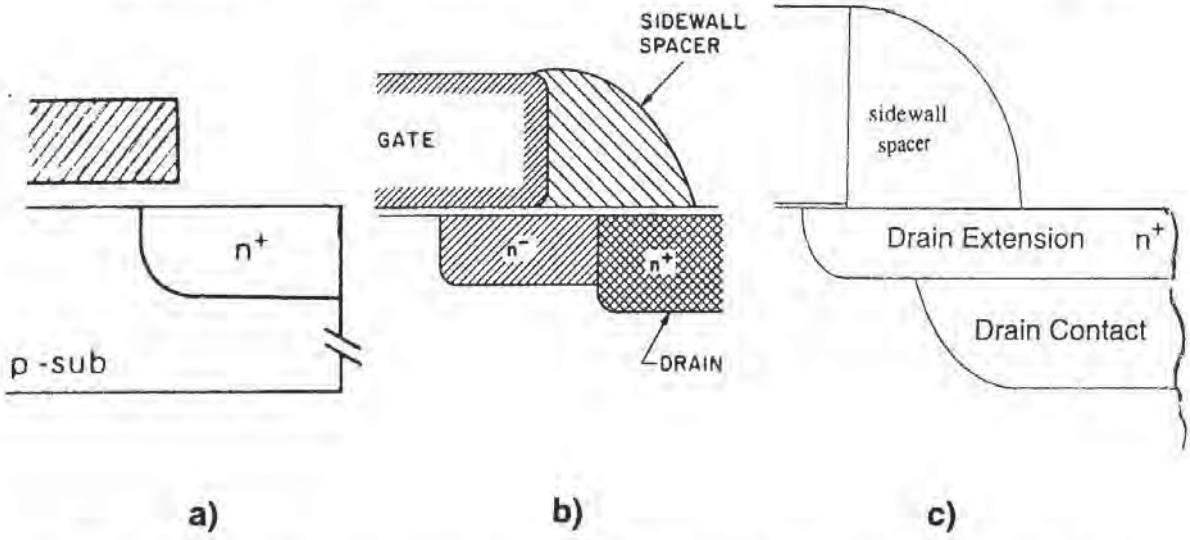


Fig. 1-6 a) Single-region drain in a MOSFET; b) Lightly-doped-drain in a MOSFET; c) Source/drain-extension and contact-drain-regions used in deep-submicron MOSFETs.

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voltage has been reduced to about 2.0 V (down from the 5.0 V power supply value that was retained until devices got to the 0.8-μm generation). In any case, for such small drain-voltage values, the electric field near the drain is already reduced to a degree where few carriers can now gain sufficient energy to create interface states or shallow oxide traps. Hence, in deep-submicron MOSFETs HCI-effects no longer need to be controlled by the use of an LDD structure. However, the parasitic resistance contribution to the overall MOSFET ON-resistance due to the LDD region is increased to an unacceptably large degree.

To overcome the above problem, the two-region drain structure is retained. However, the region closest to the channel is no longer an LDD region. Instead, the first region is now termed the *source/drain-extension-region* (*SDE*) because the peak doping is no longer lighter than in the contact region. The increase in peak doping is achieved by raising the implant dose into the SDE region (from 1-5x10^{13}/cm^2 to 5-10x10^{14}/cm^2), which produces an extension region of the drain having lower resistivity. The peak doping concentration in the SDE is as high as in the second (contact) region, but its junction depth is shallower. This second drain region is called the *contact region* (Fig. 1-6c). It should also be noted that the penetration of the junction due to the SDE under the gate edge must be more carefully controlled as the gate length gets shorter.

The main challenge is to continue to make the SDE more shallow (to control short-channel effects), while retaining a sufficiently low resistance. Shallow n^+/p S/D junctions can be formed easily by arsenic (As) implantation, because its high mass produces smaller R_p, and the high As dose in the SDE region amorphizes the silicon, suppressing channeling effects. On the other hand, it is more difficult to make shallow p^+/n S/D junctions due to the low mass and susceptibility to TED of boron (the only p-type dopant with solid solubility suitable for this application). This has driven boron implant energies to the ultra-low (0.5-1.0 keV) range, and has forced the development of specialized ion implanters to do these implants economically. These and other issues involved with the formation of the SDE and the contact region are described in detail in Chap. 5.

1.2 DEEP-SUBMICRON CMOS STRUCTURES

Other structures besides just MOSFETs have to be formed when fabricating monolithic ICs. That is, isolation structures and interconnects are also needed.

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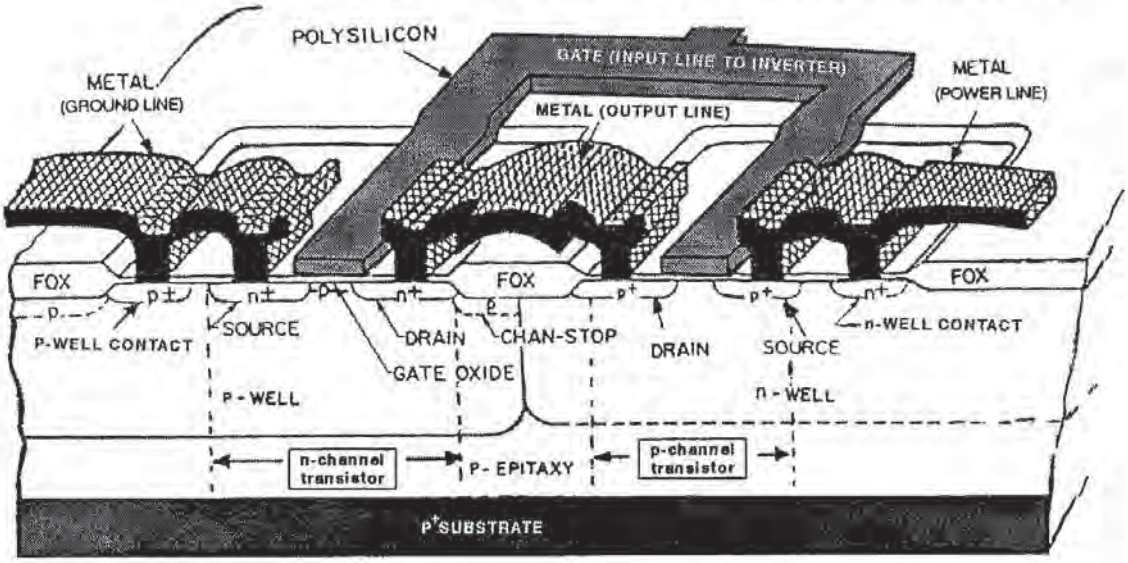


Fig. 1-7 Perspective schematic view of a twin-well CMOS structure.

Furthermore, the IC technology can be MOSFET-based (e.g., NMOS or CMOS), bipolar-junction-transistor (BJT) based (e.g., emitter-coupled-logic – ECL), or one that contains both BJTs and MOSFETs (e.g., BiCMOS). Since CMOS is the dominant silicon IC technology at the start of the 21st century, the focus will be on the CMOS structures within the silicon substrate that must be created when manufacturing deep-submicron CMOS ICs (Fig. 1-7).

1.2.1 Substrate Issues for Deep-Submicron CMOS

Czochralski-grown single-crystal silicon is the starting material on which silicon ICs are fabricated. Such single-crystal silicon is formed into *wafers*. There are two common doping-concentration configurations that ULSI wafers contain: **1**) the wafers are uniformly doped with a relatively light doping concentration of either *p*- or *n*-type dopant (and such wafers are referred to as *bulk* or, *polished wafers*); and **2**) the wafers are heavily *p*-doped during the crystal growing process, and then a lightly *p*-doped epitaxial Si layer is grown on the polished top surface of the wafer (and these wafers are referred to as *epitaxial*, *epi,* or *p-epi-on-p*$^+$ *wafers*).

Bulk wafers were used for NMOS technologies and some CMOS technologies (especially in chips that have lower selling prices, since the cost of bulk-Si wafers is about one-half that of epi wafers). The epi wafers were used for controlling latchup in CMOS logic circuits that needed high functional density but had a higher average selling price (ASP) than the chips that use bulk-Si wafers.

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In deep-submicron CMOS technologies, the *epi wafers* are used for other roles besides just controlling latchup. The use of an epi layer on a heavily p-doped Si wafer improves the gate-oxide-integrity (GOI - an important factor that determines the overall yield of the chips), and also the intrinsic-gettering capability of the wafer. That is, some impurities in the Si wafers (e.g., iron) are gettered by the formation of metal-atom-B pairs (Fe-B) in the heavily-B-doped bulk region of the wafer. Chapter 2 discusses both the GOI issue and this gettering capability in detail. It also reviews the new, alternative substrates that are beginning to replace the conventional epi-wafers described above (e.g., such new wafer types as *epi optimized substrates).*

1.2.2 Well Formation in Deep-Submicron CMOS

As described in Sect. 1.1.3, "conventional" wells in CMOS are formed by introducing the well dopants with a shallow implant process, and then diffusing them deeply into the silicon with a long, high-temperature drive-in step. This creates a well doping-concentration profile that has the highest doping concentration at the silicon/oxide interface, and decreases monotonically with distance into the depth of the silicon. Unfortunately, such a well-doping-profile forces tradeoffs to be made among various MOSFET device-performance characteristics, especially when fabricating deep-submicron MOSFETs.

To avoid this problem, and to enable independent optimization of key MOSFET performance characteristics, a different well-doping-profile must be produced. That is, by creating so-called *retrograde-wells* (instead of "conventional" wells), carrier mobility, S/D capacitance, inter-device leakage currents, V_T-control, punchthrough suppression, parasitic transistor effects, and latchup can be optimized almost independently. Retrograde wells are discussed in Ch. 5.

1.2.3 Dual-Doped Poly in Deep-Submicron CMOS

Conventional CMOS structures (down to about 0.35-μm) used n^+-poly for both NMOS and PMOS devices. Surface-channel MOSFETs are produced when n^+-poly is used as the gate material for NMOS transistors. However, the consequence of using n^+-poly as the gate material for PMOS transistors is that such PMOSFETs are buried-channel MOSFETs (see Vol. 3 for a complete discussion on surface-channel vs. buried channel MOSFETs, and why the use of n^+-poly makes buried-channel PMOSFETs inevitable). However, buried-channel PMOSFETs exhibit OFF-state leakage currents that are unacceptably large once MOSFETs are scaled to 0.25-μm (and smaller) gate lengths.

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To overcome this problem, it is necessary to build surface-channel PMOSFETs (as well as surface-channel NMOSFETs) in CMOS technologies at 0.25-μm and smaller. This requires the use of p^+-poly as the poly gate material on the PMOSFETs (Fig. 1-8), and n^+-poly for NMOSFETs (in other words, the poly in the 0.25-μm [and smaller] CMOS circuits must be *dual doped*). Such a change has several implications. First, additional complexity is introduced into the CMOS process flow (e.g., selective dual doping of the poly layer must be carried out instead of single doping, requiring additional masking layers to permit such selective doping). Second, the p-dopant introduced (boron, B), can penetrate the gate oxide into the silicon substrate unless a sufficiently low thermal budget is used after this poly doping step (or unless the gate oxide is somehow made more resistant to B penetration). Such B penetration would cause unacceptable variations in the threshold voltage of the PMOSFETs. Third, B diffusion along the poly lines can counterdope the poly in other parts of the IC. Some of the issues involved with the use of dual-doped poly in deep-submicron ICs are discussed further in Chap. 3, as well as in Vol. 3, Chap. 5 of this series.

1.2.4 Shallow Trench Isolation for Deep-Submicron CMOS

LOCOS isolation was developed in the early 1970s, and it remained the workhorse isolation structure for NMOS and CMOS ICs until these technologies reached the 0.35-μm generation (Fig. 1-9a). However, for IC generations beyond

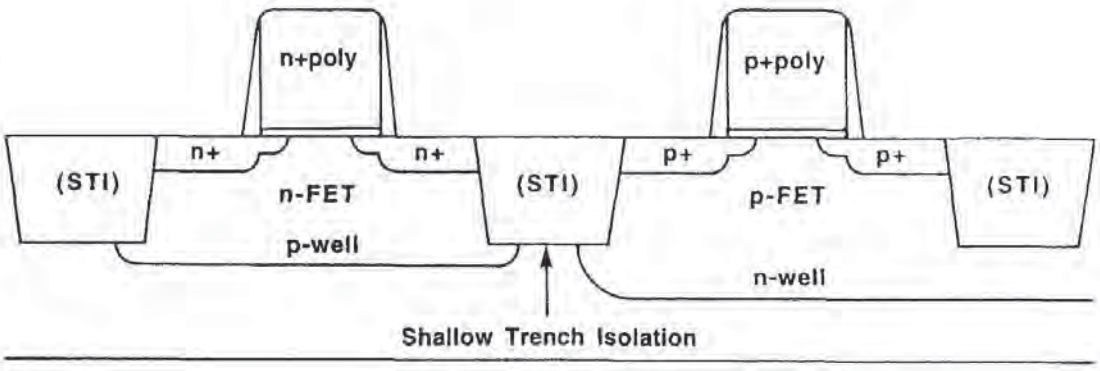


Fig. 1-8 Schematic cross-section of a CMOS structure with STI and dual-doped poly.

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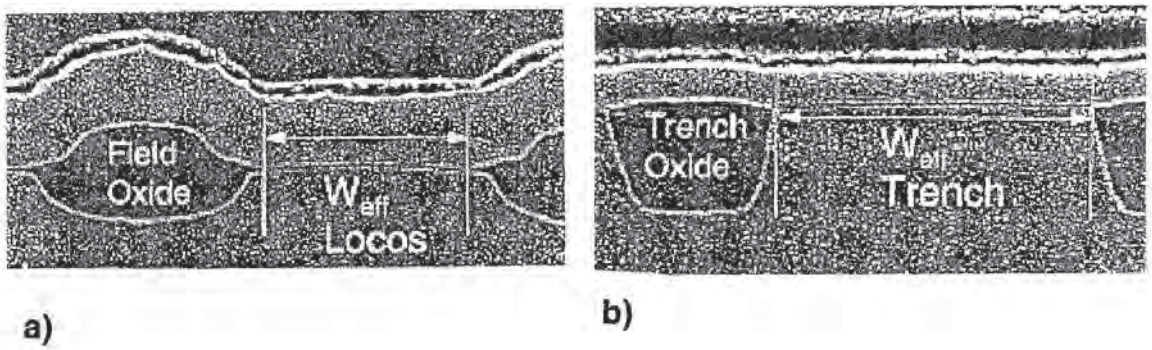


Fig. 1-9 a) Semirecessed LOCOS isolation structure; b) Shallow trench isolation structure.

0.35 μm, shallow-trench isolation (STI) replaced LOCOS. The drawbacks that LOCOS could not overcome were the field oxide bird's beak (that encroaches into the active areas of the chip) and the non-planar topography that results from thermally growing the semi-recessed field oxide.

Both of these problems are avoided by the use of STI (Fig. 1-8 and 1-9b). That is, in STI, trenches are etched and filled with oxide deposited by CVD to form the thick isolation oxide region. This method of forming the isolation oxide does not produce a bird's beak. In addition, by using CMP to planarize the surface in the course of forming this isolation oxide-structure, the wafer surface is flat at the conclusion of the STI-formation sequence. This eliminates the topography that exists at the conclusion of the LOCOS formation process. Chapter 9 covers the details of STI and CMP is discussed in Chap. 8.

1.2.5 Silicon-On-Insulator (SOI) Technology

CMOS technology has largely been built on so-called bulk-Si wafers. In such wafers the devices are isolated from one another by a combination of isolation structures at the silicon surface, and *pn* junctions in the bulk of the Si. However, latent current paths among devices may still be activated in the bulk regions by such phenomena as latchup or transient radiation events. Furthermore, parasitic circuit elements associated with the CMOS structure (such as source-to-substrate and drain-to-substrate capacitances) can become too large in CMOS structures built on bulk-Si wafers. As a result, the use of *silicon-on-insulator wafers* (SOI)

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instead of bulk-Si wafers for some CMOS applications is being pursued. Device isolation and latchup control are simplified for SOI with fewer processing steps required. SOI technology is described in Chap. 11

1.3 LIMITS TO CONVENTIONAL MOSFET SCALING

Conventional scaling of MOSFETs, with some modifications to the device structures (as described in the previous sections) has allowed MOSFETs with gate dimensions to be reduced from 10-μm in the 1970s down to 0.1-μm. (Figure 1-10 shows a SEM micrograph of 0.18-μm MOSFET transistors in typical logic structures.) Certain MOSFET structures were essentially just scaled (without undergoing any fundamental structural changes) as the minimum device dimension was reduced to about 0.1-μm. These include: the gate-oxide thickness; the source/drain junction depth; and the gate length.

However, below 0.1-μm, MOSFET devices built according to the structure described in this chapter (and depicted in Fig. 1-2), appear to run into some fundamental limits. These limits would prevent further size reductions if we were restricted to using only such traditional scaling approaches. Table 1-2 (as postulated by Thompson *et al.*), catalogs these limits.[4] Consequently, to enable MOSFETs to be scaled even further, new solutions will need to be developed, such as the use of high-k materials for gate dielectrics (see Chap. 4), and novel shallow, ultra-low-resistivity junctions (see Chap. 5). Other issues related to these limits also arise, and will be considered in the chapters of this book. For example, advanced lithography challenges will be covered in Chaps. 6 and 7, and

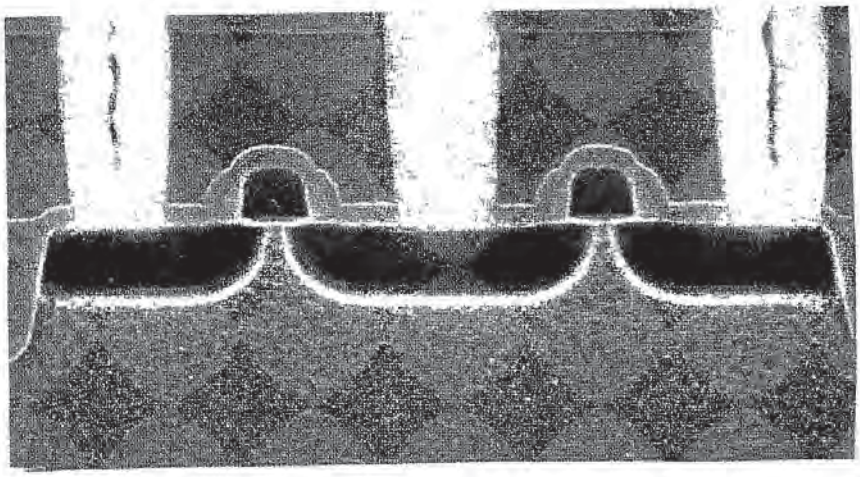


Fig. 1-10 A SEM micrograph of 0.18-μm MOSFET transistors in logic structures.

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Table 1-2 SCALING LIMITS OF CONVENTIONAL MOS DEVICES[4]

FEATURE	LIMIT	REASON
Oxide Thickness	2.0 nm	Leakage (I_{gate})
Junction Depth	30 nm	Resistance (R_{SDE})
Channel Doping	V_T = 0.25 V	Leakage (I_{off})
SDE Under-Diffusion	15 nm	Resistance (R_{inv})
Channel Length	0.06 μm	Leakage (I_{off})
Gate Length	0.10 μm	Leakage (I_{off})

alternative device architectures, such as Si:Ge technology and SOI CMOS will be discussed in Chaps. 10 and 11, respectively. Issues concerning ULSI interconnect issues are explored in Chaps. 12 to 16. A recent review by Hutchby *et al.*, discusses the novel structures being considered to replace conventional MOSFETs that are still being used in ICs at the start of the decade of 2000.[8] It describes how such nanoelectronic structures for memory, logic, and information processing architectures could possibly extend the time frame of the ITRS beyond CMOS.

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Chapter 2

300-mm SILICON WAFERS

This chapter deals with 300-mm wafer technology, including the growth of 300-mm Si crystals, 300-mm wafer specifications, and the economics of the 300-mm wafer industry. Readers wishing background information on material properties of silicon, general information on Si crystal growth and wafering can consult *Silicon Processing for the VLSI Era - Vol. 1: Process Technology, 2nd Edition.*

2.1 300-mm SILICON WAFER GROWTH

The fabrication of VLSI and ULSI takes place on Si substrates possessing very high crystalline perfection. The critical importance of utilizing single-crystal material for the transistor regions of microelectronic circuits was first recognized by Teal in 1949.[1] He reasoned that polycrystalline material would exhibit inadequately short minority-carrier-lifetimes, due to the defects at the grain boundaries of the polycrystalline grains. Teal also pointed out the need to define the degree of chemical purity and crystal perfection, the uniformity of structure, and the chemical composition of the single-crystals when specifying starting material on which to fabricate semiconductor products. The method of obtaining such single-crystal Si for IC fabrication, involves several steps (Fig. 2-1):

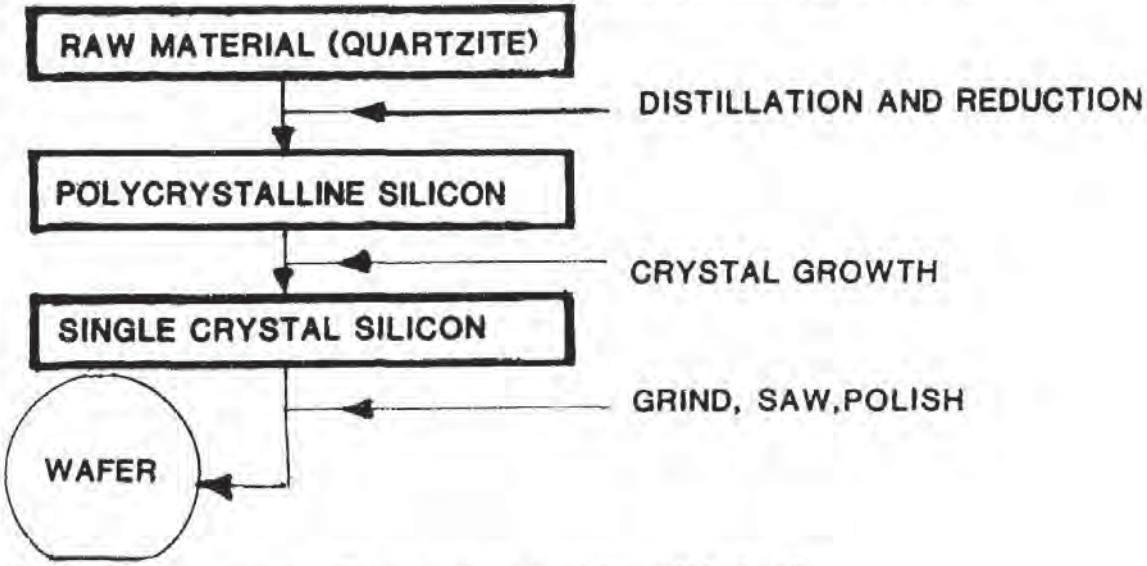


Fig. 2-1 Process sequence: From starting material to polished wafer.

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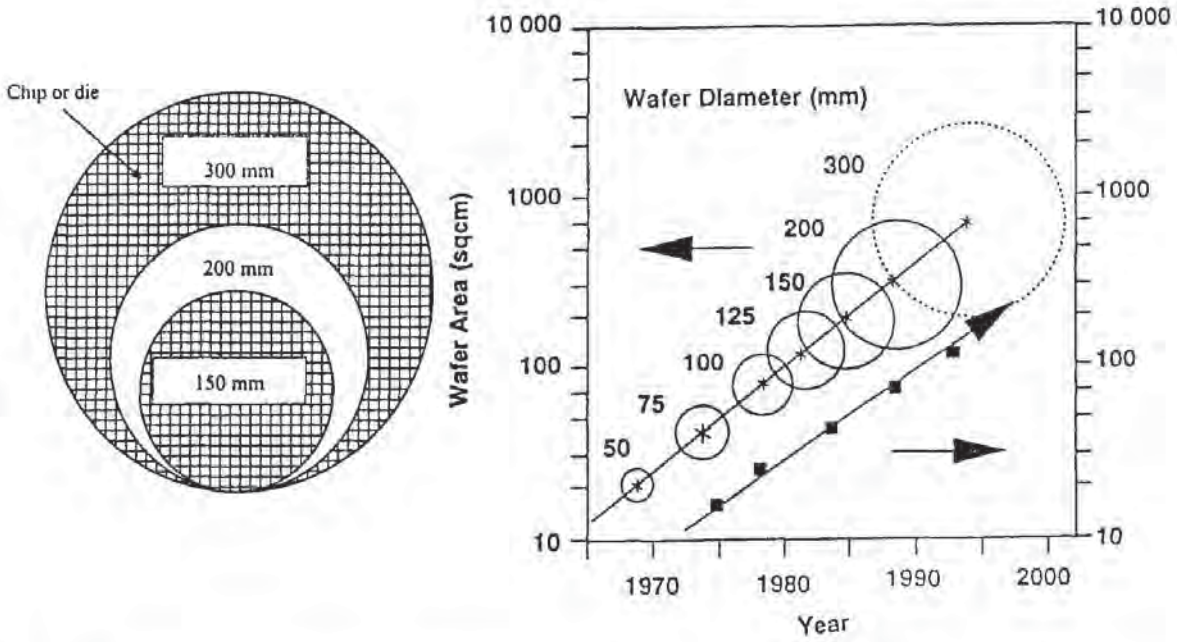


Fig. 2-2 The increase with time of CZ silicon crystal diameter and the percentage increase in wafer area with increase in wafer diameter.

1. Raw material (e.g., quartzite, a type of sand), is refined by a complex, multi-stage process that produces *electronic grade polysilicon*, EGS (Fig. 2-1).
2. This electronic grade polysilicon is used to grow single-crystal silicon by *Czochralski* (CZ) crystal growth or *float-zone* (FZ) crystal growth.

In CZ growth, single-crystal ingots are pulled from molten silicon contained in a crucible. Czochralski silicon is preferred for ULSI applications since it can withstand thermal stresses better than FZ material,[2] and it is able to offer an internal gettering mechanism (not available with FZ crystals) that can remove unwanted impurities from the device structures on wafer surfaces.

The simplicity of the CZ process and the relatively high-degree of crystal purity helped establish it as the dominant silicon-crystal-growing technology in the early years of the semiconductor industry. The development of dislocation-free ingot growth and automatic diameter control in the late 1960s lead to a rapid growth in the sizes of ingot diameters and crystal melts. Further increases in charge size and diameters were driven by the economic advantages of even larger ingots. As shown in Fig. 2-2, by 1998 300-mm diameter crystals had become available, grown with 150-kg charges. Typical commercial ingots are grown 0.5–2.5-m in length, and a 100-kg charge can grow an ingot roughly 1-m long

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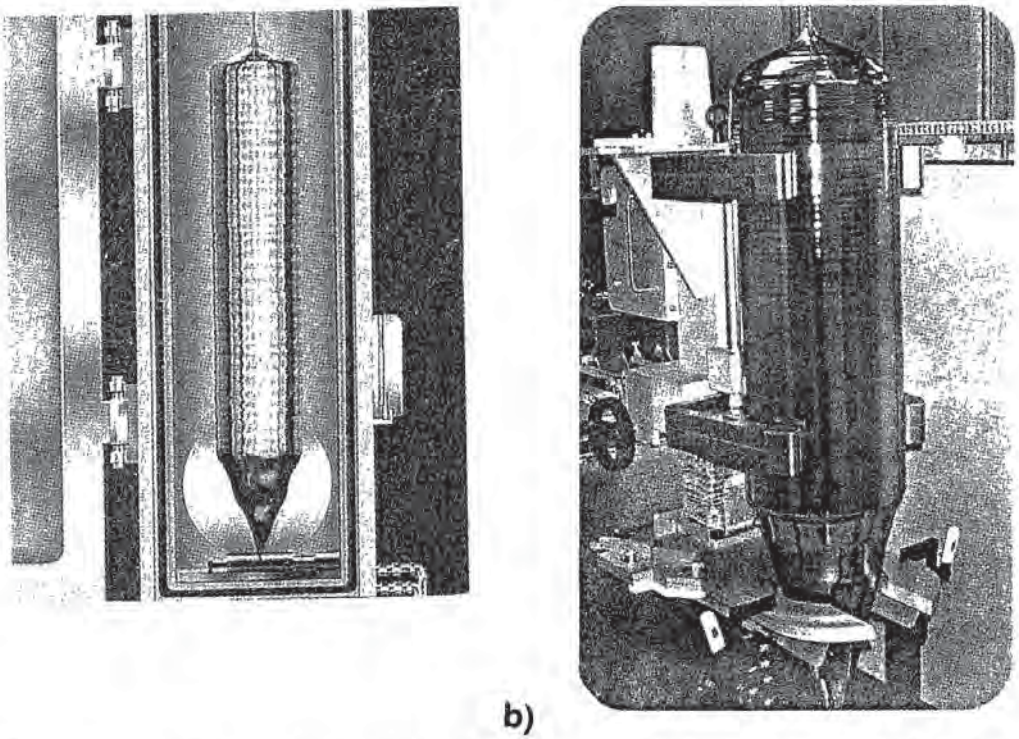


Fig. 2-3 a) 300-mm Si crystal after it has been removed from a 300-mm CZ puller; b) 300-mm ingot cooling on a materials-handling device.

with a diameter of 200-mm. The driving function for going to larger wafer diameters is the increase in Si area available per wafer. Figure 2-2 also shows that the area of a 300-mm wafer is 2.25 times the area of a 200-mm wafer. Figure 2-3b shows a 300-mm Si ingot mounted in a materials handling device. We will only concern ourselves in this section with the issues involving the growth of 300-mm Si-crystals.

The wafer manufacturing process for 300-mm wafers is not a straightforward extension or scale-up of 200-mm processes. Most tools needed to produce 200-mm wafers, including crystal pullers, grinders, polishers, cleaners, and inspection stations are not capable of being cost-effectively utilized for 300-mm wafer production. In addition, the cost of growing 300-mm silicon crystals is the principle challenge facing technologists striving to match the 200-mm unit-area cost performance. That is, to be able to achieve the same yield of 300-mm wafers as is possible with 200-mm wafers, the size of the charges will have be increased from the 150-kg charge being used in 1998 for 200-mm wafers to 300-400 kg for 300-mm wafers. The equipment used to pull crystals from such charges will also have to be able to rotate and lift the crystal while stirring and positioning the

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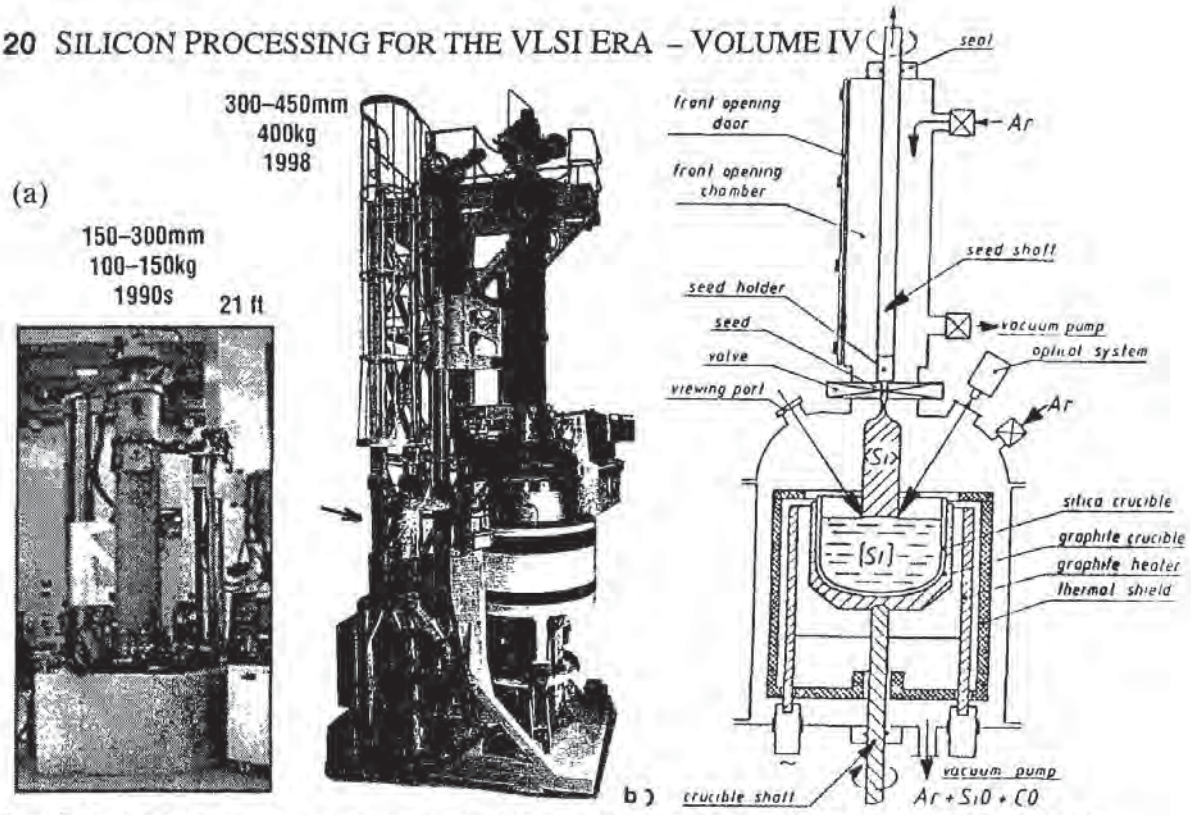


Fig. 2-4 a) Modern computer controlled CZ pullers. Larger silicon wafer sizes and the required manufacturing efficiency have driven crystal puller size. b) Schematic drawing of CZ puller.

melt, doing this all the while without vibration, in a high-vacuum atmosphere, and at temperatures that exceed 1400°C. Figure 2-4 shows how the size of the crystal puller has to be increased with respect to the size of a 200-mm puller to make it possible to handle such larger charges.

The charge must be held in a single-use, high-purity quartz crucible more than 30 inches in diameter. Demands on the crucible increase significantly for a 300-mm process, as the growth cycle time stretches to over 100 hours (~4 days). Any flaw that develops in the crucible during that multi-day crystal-growth time can cause a loss in atomic alignment of the crystal, making it unusable.

Another important factor that impacts the cost of producing the wafer is the crystal pull speed (i.e., the longer it takes to pull the crystal, the higher the cost of producing the wafer). However, in growth chambers of identical design, this speed $v_{pullrate}$ is inversely proportional to the crystal diameter $D_{crystal}$ or, $v_{pullrate} \sim (1/D_{crystal})$. The reason that the pull speed must be decreased as the diameter increases is that the crystal mass increases as the square of the ingot radius, while the surface area of the ingot (which radiates away the heat of fusion), is proportional to the diameter. Thus, a path toward reducing the cost of manufacturing larger diameter wafers is to develop new and innovative puller

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designs that allow the heat to be removed more quickly than in a conventional puller (a project apparently being pursued by most wafer suppliers).

Increasing the pull speed, however, is only one relatively small aspect of decreasing the cost of manufacturing large diameter wafers because there are many steps that comprise the entire growth cycle. (As shown in Fig. 2-5, by tripling the pull speed from 0.5 mm/min to 1.5 mm/min, the wafer production cost is reduced by only about 5%.) Two other significant factors that increase the cost of producing 300-mm wafers above the cost of producing 200-mm wafers are: **1**) a 300-mm wafer is 50-μm (or 7%) thicker than a 200-mm wafer; and **2**) the back surface of a 300-mm wafer is polished, whereas the back surface of a 200-mm wafer is not. The back-surface polishing process removes an additional 10-20-μm of silicon stock. In total, a 300-mm wafer therefore consumes about 9% more Si-crystal per unit area than a 200-mm wafer, resulting in fewer wafers per unit-length of ingot.

2.2 GROWN-IN CRYSTAL DEFECTS: CRYSTAL-ORIGINATED PARTICLES (COPs) and DISLOCATION LOOPS

As the silicon crystal is being grown in the CZ growth process, several phenomena occur that produce defects in the as-grown crystal. Since these defects arise from the various aspects of the CZ crystal growth sequence (namely, solidification from the melt and cool-down to room temperature), they are termed *grown-in defects*. As the minimum device dimensions in ICs are scaled below 0.25-μm, grown-in defects have been identified as a potential factor that reduces the performance characteristics and decreases the yields of CMOS ICs. The most significant of these grown-in defects are the so-called *crystal-originated defects* (COPs). The COP defects have the form of voids in the Si lattice, and these voids are caused by agglomeration of supersaturated vacancies

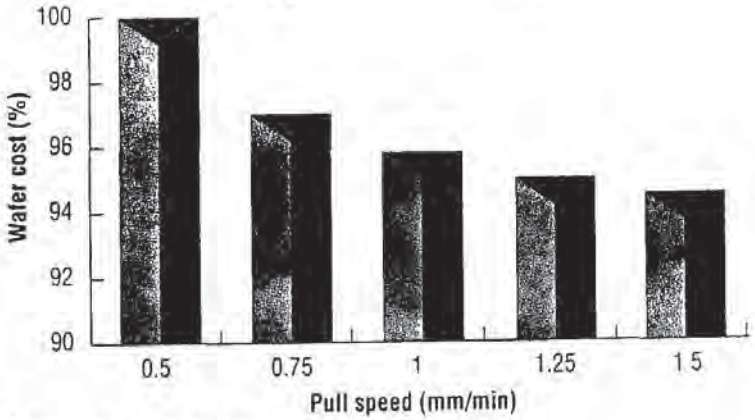


Fig. 2-5 300-mm crystal-growth-cycle-time components.

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that are introduced into the crystal as the liquid-phase-silicon solidifies. COPs cause two major problems when such voids intersect the wafer surface: **1**) they degrade the integrity of thin gate-oxide films (GOI); and **2**) they create leakage paths in the isolation structures of DRAMs.[3] In this section we describe the mechanisms that give rise to these COPs and provide details about the problems they cause in the devices fabricated on wafers containing such defects. Finally, we discuss measures that have been employed to mitigate their effects.

Note that another form of defect is also prevalent in CZ Si wafers, namely oxygen precipitates. These defects, however, form during IC processing (instead of during the crystal growth process itself), and thus oxygen precipitates are not considered to be grown-in defects. However, their density in the wafer (number/cm^3) and their size also strongly correlate with prior crystal growth conditions and subsequent heat treatments.

It is believed that the grown-in defects described above (i.e., COPs - as well as their complementary counterparts, dislocation loops) arise from an agglomeration of intrinsic point-defects (namely, vacancies to form COPs and self-interstitials to form dislocation loops), during the cooling of the silicon ingots following the crystallization from the liquid phase. The formation of voids from the homogeneous nucleation (agglomeration) of supersaturated vacancies in silicon was first suggested by Voronkov in 1982.[4]

Intrinsic point defects are incorporated into the silicon when it crystallizes. Estimates from computer simulation indicate that their thermodynamic equilibrium concentrations at the melting point of silicon (1412°C) are ~1x10^{15} cm^{-3} for vacancies, and about 20% less for self-interstitials.[5,6] As the crystal cools continually during CZ growth, the solubility of these intrinsic point-defects decreases, resulting in a condition of supersaturation. Intense recombination of the vacancies and interstitials occurs when the solidified crystal is cooling through the high-temperature range (i.e., from 1412°C to ~1200°C). At the same time, some net out-diffusion of self-interstitials occurs from regions near the surface (outer circumference) of the Si ingot. That is, more self-interstitials out-diffuse from the ingot surface than do vacancies because the self-interstitials diffuse 10 times faster than vacancies near the silicon melting-point temperature.

Computer simulations further indicate that ~10% of the original point-defects in both the vacancy- and interstitial-rich regions survive after the intense recombination events which occurred during the cooling through the high-temperature range, but that these surviving point-defects still remain in supersaturation when the temperature of the ingot drops below ~1200°C. Since the point-defects continue to diffuse rather rapidly at temperatures above

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~1150°C, they can come out of solution either by further recombination events, or by agglomerating into clusters of vacancies or self-interstitials. The vacancies have been found to agglomerate into octohedral voids at about 1150-1180°C. As noted earlier, these voids formed by vacancy-agglomeration are called crystal-originated particles (COPs).[7,8] Supersaturated self-interstitials, on the other hand, can form large dislocation loops. CZ-silicon-crystals, however, are pulled under conditions where vacancies are the prevailing type of intrinsic point-defect, and as a result, self-interstitial-agglomerated dislocation loops do not occur in significant numbers in 200-mm Si wafers used in IC production. Thus, our discussion of grown-in defects is primarily focused on COPs.

2.3 DETAILS OF THE FORMATION OF CRYSTAL ORIGINATED PARTICLES (COPS)

In this section we provide additional information about the formation of COPs and the effects they have on IC devices. We begin with a more detailed discussion of how COPs are formed during the cooling of the Si ingot.

The formation of COPs was studied by employing crystal-growth-halting-and-quenching techniques. That is, during CZ-growth the crystal ingot pull-rate was abruptly halted, and the ingot temperature was quickly lowered (quenched) to some specific value. By doing this with a number of ingots and quenching to different temperatures, the defects formed during the cooling of the ingot from solidification to that temperature could be examined. Such studies indicated that the formation of COPs consists of two stages. In the first, voids are rapidly formed as the ingot cools through the narrow temperature range of 1150-1180°C. In the second, an oxide is formed on the inner surface of the voids during the cooling-down process following void formation (down to about 900°C). The resultant voids formed within the bulk have been identified by TEM studies as having a tetrahedral shape, and with sizes between 0.1- and 0.3-μm (100-300-nm), Furthermore, their inner surfaces are covered with a thin oxide layer approximately ~5-nm thick (Figs. 2-6 and 2-7).[9] Such COPs are formed with densities between 10^5 to 10^7 cm^{-3}.[10]

It should be noted that before the nature of grown-in defects was well understood, COPs were identified in the literature under different names, depending on the technique that was used to delineate and detect them. These terms included: *COPs*, *laser-scattering tomography defects* (LSTDs), *flow-pattern defects* (FPDs), and *Secco etch-pit defects* (SEPDs). However, by comparative observation, it was confirmed that they were in fact the same type of defect (namely COPs), that just appear under different guises (depending on the technique used to detect them).

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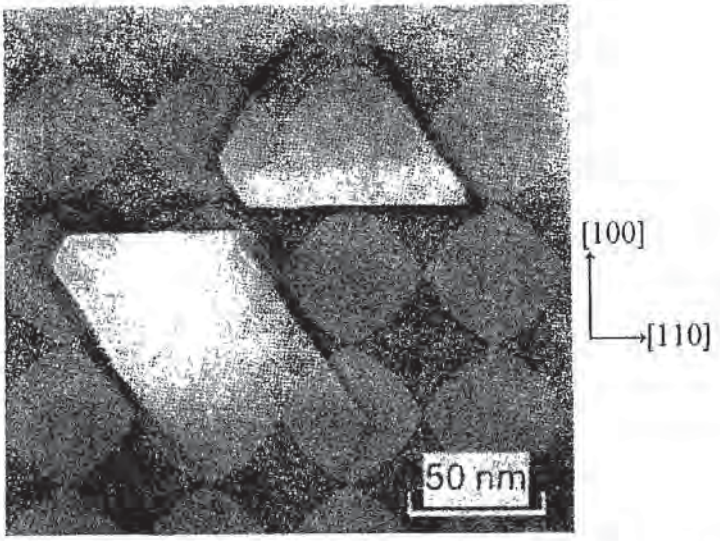


Fig. 2-6 SEM of COPs as they appear on the surface of a Si wafer. Oxide layer at the void:crystal-interface is visible.

In fact, the most common method used to make COPs visible with optical instruments when they intersect a wafer surface is to immerse bare silicon wafers in hot RCA-Clean SC-1 solutions (e.g., 4 h @ 85°C). The SC-1 solution etches Si slowly and isotropically, and this enlarges the lateral and vertical dimensions of any COPs that intersect the surface. They appear with the shapes shown in Figs. 2-6 and 2-7.[11] This shape enlargement also makes it possible for laser-based defect-detecting tools (which do not have as high a resolution capability as do TEMs - which can be used to image COPs directly), to detect the presence of any COPs as *localized light scatterers* (LLDs). By using this delineation technique, the entire wafer surface can be quickly mapped for the presence of COPs with

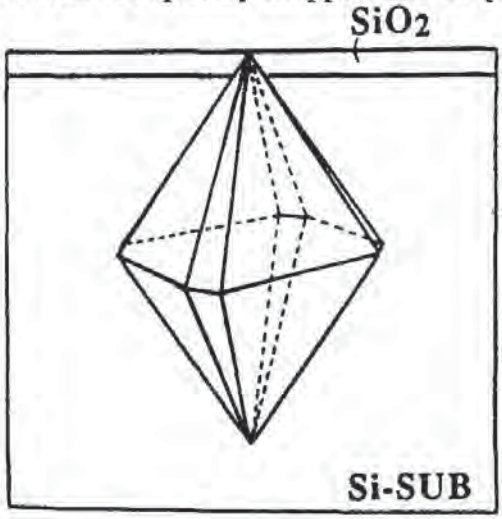


Fig. 2-7 Schematic representation of the octahedral structure of a COP defect.

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an automated scanning surface inspection system (such as the KLA-Tencor Surfscan).

2.3.1 The Radial Distribution of Grown-In Defects on the Wafer Surface

As described previously, typical 200-mm wafers being used for ULSI today have a central vacancy-rich region surrounded by a self-interstitial-rich edge. These regions are separated by the vacancy/self-interstitial (V/I) boundary that occurs at a critical value of a parameter, ς_c, defined as:

$$v/G(r) = \varsigma_c = 0.138 \text{ mm}^2/\text{min-K} \quad \textbf{(2.1)}$$

where v is crystal pull rate (in mm/min), G(r) is the axial temperature gradient {i.e., G(r) = dT(r)/dr [in K/mm]} at the crystal/melt interface at a radial position (r) from the center of the ingot, and T is the absolute temperature (in kelvins).[12]

The axial temperature gradient, G(r), at the center of the crystal ingot is usually lower than at the ingot surface. In addition, v is the same across the crystal growth interface at a given pull rate. Thus, in conventional CZ crystal growth, the value of v/G(r) is highest at the radial center of the ingot and decreases continually toward the crystal-ingot edge. The wafer central-region inside the V/I boundary is thus vacancy-rich, characterized by $v/G(r) > \varsigma_c$, while the edge-region outside the V/I boundary is self-interstitial-rich, with $v/G(r) < \varsigma_c$.

The concentration of the vacancies (C_V) and the self-interstitials (C_I) at a given radial position, r, relative to those of the equilibrium levels of (C_V^{eq}) and (C_I^{eq}) at about 1200°C, after passing the intense recombination and out-diffusion regime between the melting-point and ~1200°C, are apparently exponentially proportional to the difference between v/G(r) and ς_c, or:

$$(C_V/C_V^{eq})_r = \exp\{\alpha [v/G(r) - \varsigma_c]\} \quad \textbf{(2.2)}$$

$$(C_I/C_I^{eq})_r = \exp\{\beta [\varsigma_c - v/G(r)]\} \quad \textbf{(2.3)}$$

where α and β are not known at this time. The supersaturation of vacancies is highest at the radial center, and decreases radially from this value. Thus, more voids are formed at the central-region of the wafer. On the other hand, high supersaturation of self-interstitials is present at the crystal peripheral (edge) region. But, because of out-diffusion of the self-interstitials to the crystal surface (a result of the fact that self-interstitials diffuse 10 times as fast as vacancies near the melting point of Si), high-supersaturation of self-interstitials occurs at some distance from the edge.

In the v/G(r) ratio, the thermal gradient (G[r]) is controlled by the thermal environment in the hot-zone of the crystal puller, and by melt convection. With

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an appropriately designed crystal-puller, the value of G(r) can thus, in theory, also be controlled. The pull rate v is much more easily controllable. Computer simulations of both the melt convection and the thermal distributions within the puller hot-zone have been extensively employed to modify the design of the crystal puller so that an optimum v/G(r) value can be obtained. The recent rapid progress in the field of simulating crystal-growth processes permit the bulk properties and process stability of the growth processes to be predicted with remarkable accuracy. This should help reduce R&D costs, a requisite for allowing wafer manufacturers to profitably develop the new generations of wafers being called for by the industry.[13]

2.4 THE OXYGEN-STACKING-FAULT RING (OSF-RING)

It is observed that when a typical, polished 200-mm CZ-grown wafer (as described above) is oxidized and then etched in HF and SC-1 to delineate the defects present at the wafer surface, it manifests a multi-ring defect structure. The central region of the wafer contains COPs. The COP-filled region is surrounded by a ring of *oxidation-induced stacking faults*, OSFs (i.e., which emerge after the wafer is subjected to a thermal oxidation step). This feature is also termed an *OSF-ring* (Fig. 2-8). The region of the wafer outside of the OSF-ring is an essentially defect-free region that contains a very low density of dislocation loops. This region extends to the edge of the wafer (Fig. 2-9).[14] The origin of the COPs in the central region has already been described. Here we explain what is believed to be the cause of the OSF-ring.

In the OSF-ring, the delineated defects are oxidation-induced stacking faults (OSFs). These stacking faults, however, arise from the presence of oxygen precipitates.[15] The oxygen precipitates are the actual defects that exist in the as-grown state of the ingot. But since these precipitates act as heterogeneous nucleation sites for the OSFs, the OSFs become the defects that are delineated by the SC-1 etch. Hence, this region is called the OSF-ring. An important aspect of the OSF-ring is that the ring-radius decreases with decreasing pull rate, until at a critical pull-rate-value (that depends on thermal conditions), it disappears into the center of the crystal. The presence and radial location of an OSF-ring in CZ-silicon corresponds qualitatively to the neutral (or boundary) region that separates the vacancy-rich- and self-interstitial-rich-regions of the ingot.[16] (Sometimes anomalous oxygen precipitation is observed between the OSF-ring and the defect-free outer-region, as shown in Fig. 2-9, but we shall not consider this anomalous phenomenon here).

The OSF-ring is thought to be a region in which vacancies are only in slight

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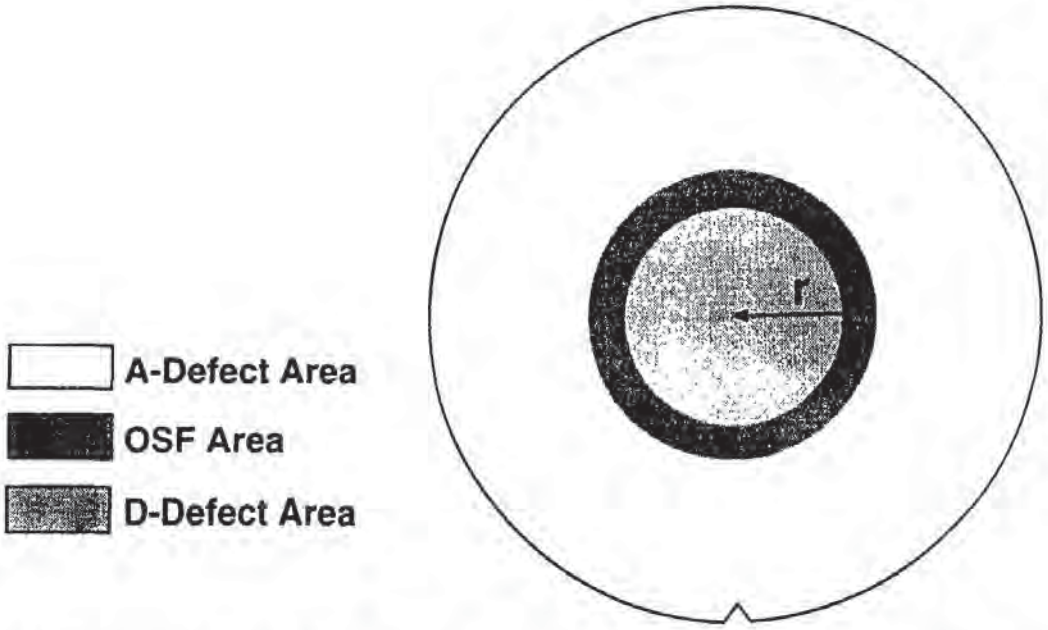


Fig. 2-8 Schematic drawing of the ring regions. An OSF-region after oxidation separates the A-defect-rich region (dislocation loops) from the D-defect-rich region (COPs) .

excess over self-interstitials, so recombination proceeds over a longer period of time, since neither species is strongly dominant. This competition results in a lower vacancy supersaturation and a delay in the onset of nucleation. Smaller voids are formed and the final vacancy concentration in the region of the OSF-ring is actually higher than inside the ring. These vacancies may provide the needed free volume for formation of the oxide precipitates that are observed at the center of the stacking faults in the OSF-ring region.[17]

2.5 MITIGATING THE EFFECTS OF COPS WITH THE USE OF POST-CRYSTAL-GROWTH ANNEALING

As we noted previously, for ULSI circuits it is important that the wafer be free of grown-in defects and oxide precipitates in the surface and sub-surface device regions of the wafer. Typically, a high-temperature annealing step is performed on the wafers to out-diffuse the oxygen near the surface, so that the concentration of oxygen there drops below the solubility limit. Thus, oxygen precipitation can no longer occur in this region, and no oxide precipitates are formed. High-temperature annealing processes have also been investigated as a method of annihilating the COPs near the wafer surface. That is, annealing at high temperatures (typically $\geq$ 1200°C) in an inert ambient (most commonly hydrogen, but also in argon) has been used to reduce the COP density near the wafer surface. Such hydrogen-annealed CZ-polished-wafers were introduced by

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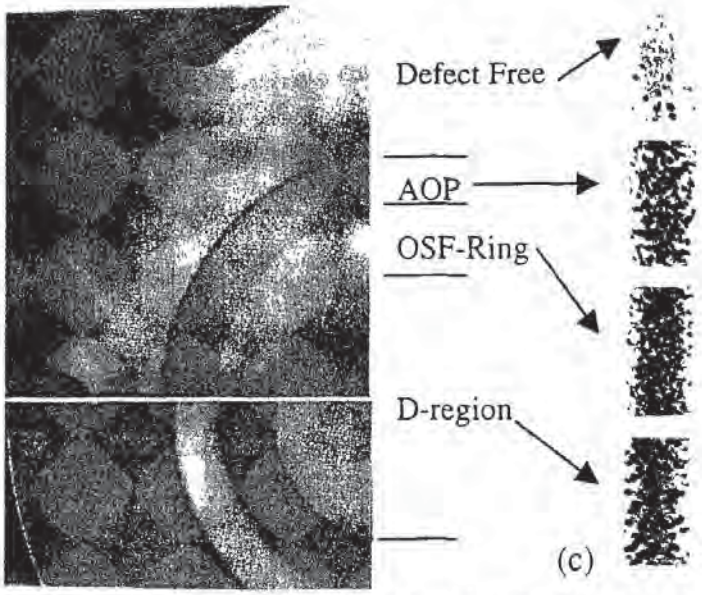


Fig. 2-9 a) Plane x-ray topograph of Cu-decorated CZ-Si wafer; b) Plane x-ray topograph of oxygen-precipitated CZ-Si wafer. The D-region, OSF ring, and defect-free regions are observed. c) Details of the defects delineated in each region.

Toshiba Ceramics in 1986, and they have been commercially available under the name of Hi-WAFER.™[18] Other silicon wafer vendors have also offered annealed CZ-polished-wafers (annealed in other gases). It should be noted that it has been reported that the annealing must be carried out in an oxygen-free ambient, otherwise the annealing procedures do not produce optimal benefits.[19]

The mechanism thought to be responsible for reducing the COP density in hydrogen-annealed wafers is as follows: The inner surface of the COP void is covered with a thin oxide. Under high-temperature annealing in a hydrogen ambient, the hydrogen species diffuse into the Si. The oxide on the COP surfaces (in regions near the wafer surface) is decomposed by the reduction effect of hydrogen and oxygen. Eventually the COP surface becomes bare-Si and the surface atoms within the COP-void are mobile enough to reconstruct this surface and cause the void to shrink (by vacancy-diffusion into the Si bulk). As the process of void dissolution proceeds, the void is first transformed into a spherical structure from a regularly octahedron (because this decreases the surface free-energy of the void during annealing).[20] It has also been proposed that a heavily-doped buried layer (created by high-energy implantation of a heavy boron dose) be incorporated into Hi-WAFERs. In that way, the benefits of a heavily-doped boron region in the substrate (as is available with p/p^+ epitaxial wafers) can also be obtained with a Hi-WAFER, at a lower cost than that of such epi wafers.[21]

Hydrogen annealing at 1150°C for several hours to reduce COP levels extends the usefulness of 200-mm polished wafers. However, it adds 15-20% to the wafer

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cost, and according to some opinions, it will not be a feasible technique for 300-mm wafers.[22]

In another report, wafers were annealed at 1300°C in an inert ambient for one hour. No observable COPs existed (i.e., at the wafer surface) after this annealing.[23] It was reported in another study that very-good GOI was obtained using such wafers. However, these wafers also showed a very high concentration of oxide precipitates after the thermal processes used during the IC fabrication were carried out. The presence of these precipitates may give rise to excess leakage values in such products as high-density DRAMs. As a result, this report concluded that the high-temperature-annealing process needs further optimization.[24]

2.6 ELIMINATION OF COPS WITH "PERFECT SILICON"

A special CZ-silicon-growth technique has been developed that eliminates COPs from silicon wafers by preventing their formation during the ingot growth process. Wafers obtained from ingots grown according to this technique are referred to as *"perfect" silicon wafers*, or *"pure" silicon wafers*.[25] The idea behind this approach is to create growth conditions such that the concentrations of intrinsic point defects remain close to their quasi-equilibrium values all along the radius of the crystal-melt interface. In that way, the silicon is not super-saturated with either vacancies or self-interstitials. Under these circumstances, regions will still exist that are either vacancy-rich, or self-interstitial-rich. But neither COPs nor dislocation loops can form (because even in those regions there is no supersaturation of the point-defect species which dominates in that region). The goal of the "perfect" silicon-growth-process is to the establish the conditions quantified by the following set of conditions:

$$v/G(r) - \varsigma_c \approx 0, \quad C_V \approx C_V^{eq}, \text{ and } C_I \approx C_I^{eq} \qquad \textbf{(2.4)}$$

The name "perfect silicon" was given to such point-defect-equilibrated silicon crystals because wafers from such crystals after immersion in a defect-delineation etch exhibit neither a boundary between vacancy-rich/self-interstitial-rich regions nor an OSF-ring. Instead, the wafer appears "perfect" or "pure." Specifically, a "perfect" silicon wafer will show negligible COP densities, so yield and performance of ULSI devices on such wafers will be enhanced to the levels exhibited by devices fabricated on epitaxial wafers. Growth processes and crystal pullers that can produce "perfect" silicon were being developed in 2000 to be able to produce 200-mm "perfect" silicon wafers in production quantities, and subsequently this effort is expected to be carried out for 300-mmwafers. However, there are some difficulties associated with this approach. The first is

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that the hot-zone in the crystal puller must be optimized so that it becomes possible to maintain the condition of $v/G(r) = \varsigma_c$ along the whole length of the crystal. The second is that a relatively slow pull-speed is needed to maintain the $v/G(r) = \varsigma_c$ condition. The latter requirement is not favorable in terms of the crystal yield.

The ingot yield from a crystal puller is reduced by this method for two reasons. First, the slower pull-speed reduces the throughput of the puller. Second, because the ingot growth cycle becomes much longer, more time is allowed for a disruptive event to occur during the crystal growth time (which would render the ingot useless). Nevertheless, since the cost to produce "perfect" silicon wafers seems to be less than the cost of producing epitaxial wafers, there is still an incentive to pursue the development of "perfect" silicon growth processes.

A report comparing the behavior of MOS-capacitor structures and *pn*-junction diodes fabricated on conventional polished CZ wafers, "perfect-silicon" CZ wafers, and p/p^+-epitaxial wafers was published by Niwa.[26] Junction leakage currents were smaller on the "perfect-silicon" and p/p^+-epitaxial wafers than on the conventional CZ wafers. GOI characteristics were also superior on the "perfect-silicon" and p/p^+-epitaxial wafers, and the "perfect-silicon" GOI results matched those obtained with the epitaxial wafers.

2.7 MINIMZING COPS PERFOMANCE DEGRADATION WITH HIGH-PULL-SPEED SILICON

Another approach that is being pursued to achieve wafer quality similar to "perfect-silicon" is to use a crystal pull-rate that is much faster than that used to pull a "perfect-silicon" ingot (three or four times as fast). With this faster pull-rate, G(r) is increased to some extent as a result of the higher pull-rate. However, since v is much larger than in the "perfect-silicon" case, the overall v/G(r) value becomes substantially larger than the critical value $\varsigma_c = 0.138$ mm^2/min-K. Thus, the crystal becomes completely vacancy-rich and the vacancy concentration at temperatures below 1200°C becomes much larger than the quasi-equilibrium value (i.e., the crystal becomes supersaturated with vacancies), or:

$$v/G(r) >> \varsigma_c, \text{ and } C_V >> C_V^{eq} \qquad \textbf{(2.5)}$$

Nevertheless, due to the high pull rate, the crystal passes quickly through the 1150-1180°C COP-forming temperature-range, so only COPs of smaller sizes and at a high density can be formed. Such small-sized voids near the wafer surface can be annihilated by post-growth wafer-annealing. Doping the ingot with nitrogen during crystal growth is another factor that contributes to the mini-

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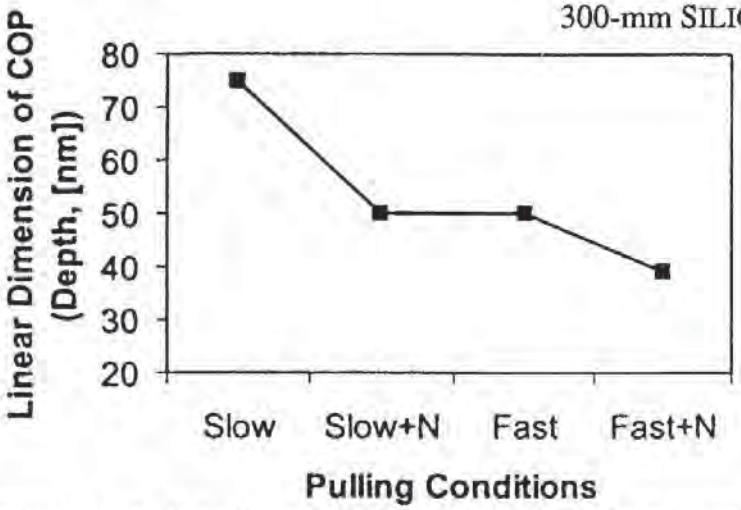


Fig. 2-10 Size of COPs in a silicon wafer as a function of pulling conditions.[28]

mization of void formation.[27] Figure 2-10 shows how the size of COPs is decreased by combining fast-pull and nitrogen-doping of CZ-ingots.[28] The fast-pull-approach offers potential advantages of high throughput and yield, and lower cost.

The process of performing the CZ-ingot-growth process at a high pull-speed and simultaneously doping the ingot with nitrogen (to get small COPs) has been combined with hydrogen annealing of wafers obtained from such ingots. By using infra-red topography, the concentration of COPs near and at the wafer surface (i.e., a technique that can detect the presence of COPs within 20-μm of the surface),[29] it was observed that the concentration of COPs decreases dramatically to depth of over 10-μm when such wafers are annealed in hydrogen at 1200°C.[30] The GOI of these wafers annealed in hydrogen was also significantly improved (Fig. 2-11).

Some concerns exist about the fast-pull CZ-Si growth processes. First, the relatively high vacancy concentrations remain in the wafer (which could cause

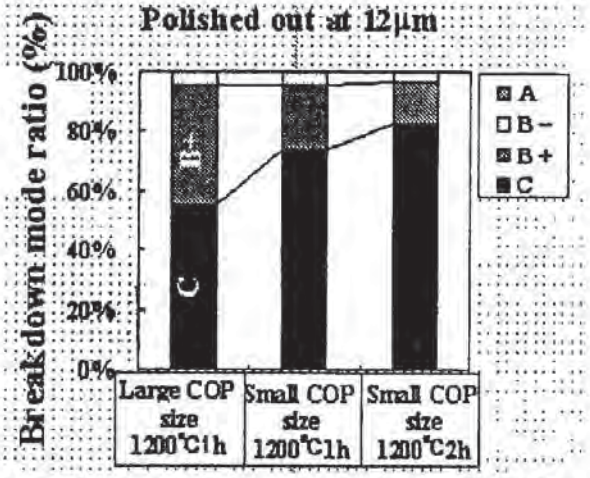


Fig. 2-11 Gate oxide integrity is best on wafers with small COP size ("C" breakdown mode indicates breakdown field of the gate oxide is > 10 MV/cm).[30]

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anomalous oxygen precipitation that degrades DRAM refresh time). Second, the formation of proper denuded zones during the high-temperature annealing steps is a question. For applications that require wafers without COPs that intersect the wafer surface, but which cannot afford to use "conventional" epitaxial wafers, a fast-pulled wafer with a thin epitaxial layer on it may be a possibility. Such wafers are termed *epitaxy-optimized substrates* (EOS), and they are described in Sect. 2.9.1.

2.8 GETTERING FOR ULSI PROCESSES

Unwanted crystalline defects and impurities can be introduced during silicon crystal growth or subsequent wafer fabrication processes. The presence of crystalline defects and impurities is undesirable because both can degrade device characteristics and overall yield. A detailed discussion of the degradation of VLSI device properties by *extended crystalline defects* (dislocations, stacking faults, and precipitates) can be found in *Silicon Processing for the VLSI Era* Vol.1, 2nd Ed. Chap. 2. The damaging effects by *impurities* are discussed here.

The impurities that create problems are grouped into two categories: **1**) impurities that participate in the process of nucleating extended crystalline defects (e.g., oxygen and carbon); and **2**) other impurities that decorate pre-existing extended crystalline defects (the latter being primarily metals, and include such elements as Cu, Ni, Au, and Fe). Such metallic impurities are highly mobile and diffuse long distances in the crystal at moderate process temperatures. Thus, there is a high probability they will migrate near extended defect sites, and be captured by them. Extended defects in device regions of the wafer which capture metal impurities give rise to larger leakage currents and lower breakdown voltages.

Efforts undertaken to eliminate the effects of impurities and defects have involved four approaches:[31] **1**) suppression of extended defect nucleation; **2**) annihilation of existing extended defects in the device regions; **3**) preventing device degrading impurities from being introduced into the wafer; and **4**) preventing any remaining metallic impurities from being captured in the device regions. Technique **4**) is referred to as *gettering*, which is a term originally used to describe the process in which an appropriate material (such as cesium), was used to getter (remove) the last traces of gas in vacuum tubes, so that the required high vacuums within the glass tubes could be achieved.

By combining these four approaches, the product yield of ICs can be enhanced. That is, proper application of the first two approaches minimizes the number of extended defects that exist in the active regions, and the third reduces

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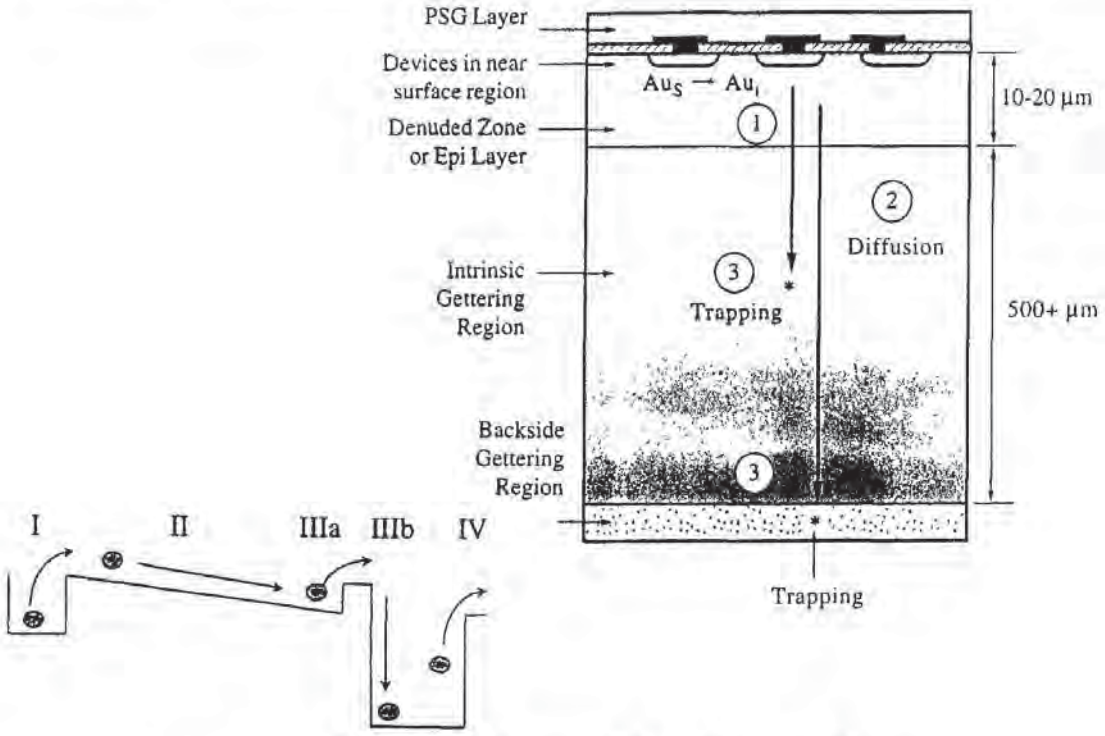
the concentrations of the impurities introduced into the silicon. Gettering is then used to remove any of those impurities that still manage to be incorporated during crystal growth or processing. Thus, gettering reduces the probability of decorating any extended defects formed in the device regions with metallic impurities.

Methods used to suppress extended defect nucleation include: **a**) control of the thermal process conditions during wafer fabrication that lead to excess thermal-stress and resultant dislocations; and **b**) creation of oxygen denuded zones at the wafer surface regions in which active devices are fabricated. The latter procedure eliminates oxygen precipitates in these device regions. *Annihilation of pre-existing* or *process-induced extended defects* such as stacking faults, is achieved by using various techniques, including elevated temperatures (>1200°C)[32] and the addition of HCl to the growth ambient[33] during the growth of SiO_2.

The use of technique **3**), namely *the control of unwanted impurities* (especially metals), involves identification and removal of the sources of contamination. Such approaches entail the thorough characterization of the material and processing equipment used to fabricate devices. Some examples of the contaminant sources that have been identified include: **a**) stainless steel fixtures in ion-implant machines that ended up being sputtered during the ion-implant process;[34] **b**) impurities originating from the sputtering of chamber walls and fixtures of reactive ion etching systems;[35] **c**) the diffusion of heavy metals from the heater coils through the fused silica walls of diffusion furnaces; and **d**) the release of transition metals (e.g., Fe and Ti) by the SiC-coated susceptors of (batch) epitaxial reactors.

A variety of procedures have been implemented to reduce the level of metal contamination arising from these sources. Stainless steel parts (which may release metal atoms as a result of sputtering in ion implanters and reactive-ion etchers) have been replaced with parts made from materials which produce less degradation if they are incorporated into Si than do Fe or Cr. Such materials include aluminum, silicon, and carbon. Suggested procedures to decrease contamination by sources of heavy metals have included the following: **1**) reducing process temperatures (since quartz tubes become increasingly permeable to the metal atoms of the furnace heating coils as the temperature increases); **2**) subjecting the furnace tubes to periodic high-temperature HCl cleaning; and **3**) use of double-wall furnace tubes (with HCl or inert gas flowing in the space between the inner and outer tubes). Contamination from epitaxial susceptors can be reduced by performing the epitaxy process at lower temperatures and reduced pressures, and by *in situ* cleaning of the wafers prior to

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	I	II	IIIa IIIb	IV
Gettering Stage	Release	Diffusion	Capture (over barrier)	Stability (release)
Driving Forces:	•temperature •photons •electric field	•Si_i, V •conc. grad. •charge state	•supersaturation •solubility enhancement.	•temperature •solubility

Fig. 2-12 Four stages of impurity gettering in silicon.

initiating epitaxial growth. The use of cassette-to-cassette operations in transporting of wafers has reduced the possibility of contamination due to manual handling. Use of vacuum wands is now mandated if automatic wafer handling fails or is not yet fully implemented.

2.8.1 Basic Gettering Principles

The mechanism of gettering removes transition metal impurities from device regions by four steps (Fig. 2-12):

1. The metal impurities to be gettered are released into solid solution from any stable-precipitate-form they have assumed;
2. They then diffuse through the silicon lattice;
3. They are "captured" at a position away from the device regions by either: **a**) the formation of chemical pairs (e.g., Fe-B pairs) with other impurities (e.g., boron) present in the crystal; or **b**) by deliberately created extended defects (dislocations or precipitates);

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4. The metal impurities are prevented from being re-released into the wafer during subsequent heat treatments.

In general, the transition-metal impurities are initially considered to rapidly disperse themselves uniformly throughout the wafer. This assumption is based on their high diffusivity and long diffusion lengths at typical processing temperatures (see Vol. 1, 2nd Ed., Chap. 2).

Gettering processes are divided into two categories: extrinsic and intrinsic. *Extrinsic gettering* involves the use of external means to create damage or stress on the surface of the silicon wafer that leads to the creation of the extended defects or chemically reactive sites at which the mobile impurities are captured. Normally such capturing sites are generated on the backside of the wafer, although front-side extrinsic gettering has also been explored. Extrinsic gettering can be performed prior to the first oxidation step (*pre-oxidation gettering*), or concurrently with the remainder of the fabrication steps (*gettering during* [or *subsequent to*] *junction formation*). *Intrinsic gettering* involves the localization of impurities at extended defects or regions of high concentration of electrical impurities (such as boron) which exist within the bulk material of the silicon wafer, and whose origin is due to an "intrinsic" property of the starting wafer, such as its oxygen or boron content acquired during CZ crystal growth.

The gettering of gold atoms in silicon by phosphorus diffusion is described, as this process serves to illustrate the basic mechanism of (extrinsic) gettering. A known concentration of gold atoms (e.g., $1x10^{14}/cm^3$) is first diffused uniformly throughout a group of silicon wafers. Phosphorus diffusions at 900°C are then carried out in an attempt to getter the gold. These diffusions produce surface regions having high concentrations of P ($1x10^{19}$–$1x10^{21}/cm^3$). After the P diffusions are completed, the gettering efficiency of the procedure is measured. It is observed that with increasing surface concentration of P, a strongly decreasing concentration of gold in the silicon bulk occurs. At P concentrations of 10^{21} atoms/cm^3, the gold concentration is decreased below the detection limit. Further investigations show that the gold has diffused into the phosphorus-containing layers in the silicon.

A model offered by some investigators describes the kinetics of this gettering process according to the following steps:[36] **a**) P diffusion is accompanied by the generation of phosphorus-vacancy complexes and/or misfit dislocations which become possible capture sites (sinks) for the gold atoms; **b**) during the P-diffusion step the highly mobile gold atoms also diffuse long distances in the wafer; **c**) the gold is captured at the phosphorus-vacancy or dislocation sites, and is thus removed from solution (this maintains a favorable

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concentration gradient of gold in solution toward the phosphorus-rich zones); and **d**) once a gold atom is captured, the electrostatic interaction energy with the capture site is so high that subsequent heat treatment does not release it back into the wafer. Sufficient phosphorus must be deposited to create enough capture sites to getter the gold present in the wafer.

Diffused phosphorus layers (and other backside gettering methods) are also effective in shrinking OISFs. Oxidation-induced stacking-faults are regions of excess point defects (i.e., Si self-interstitials). Diffused P-layers shrink them for reasons still being argued (i.e., either vacancies are injected, which shrinks the OISFs, or the supersaturated P-concentration causes precipitation to begin and the resulting dislocation loops form sites to soak up the interstitials).

2.8.2 Extrinsic Gettering

Historically, gettering of mobile metallic impurities has been accomplished by *extrinsic gettering*, in which the wafer backside is subjected to a process that creates damage or stress, and subsequently traps mobile impurities. A number of wafer backside treatments have been developed for this purpose. Mechanical damage and polysilicon deposition are the two used most widely.

Mechanical damage by abrasion, grooving, or sandblasting have all been used to create stress fields at the backside of wafers. During subsequent annealing steps, dislocations which relieve these stresses are generated. The dislocations then serve as gettering sites.

A *layer of polysilicon* deposited on the wafer backside (1.2–1.5-μm thick) is another extrinsic gettering technique that has been developed (Fig. 2-13).[37] Start-

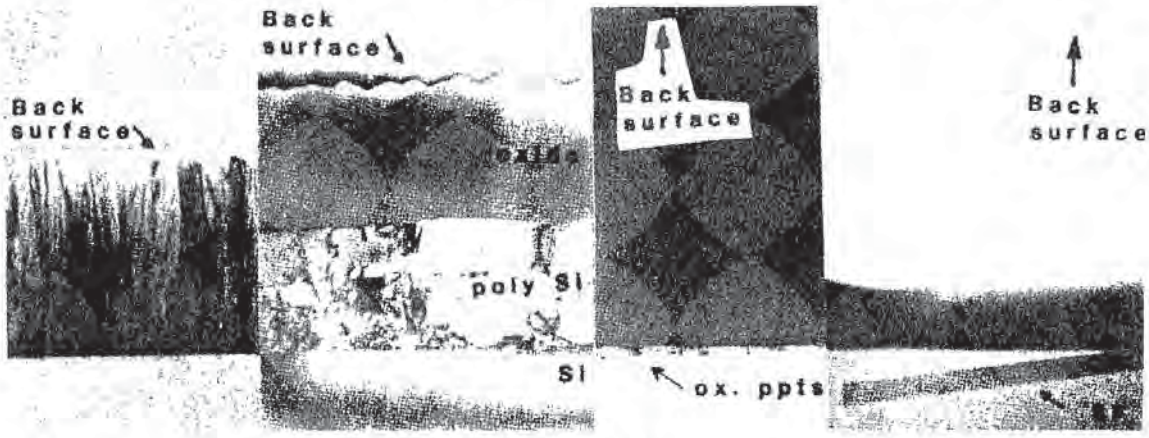


Fig. 2-13 Cross-sectional TEM micrographs of: a) as-deposited poly-Si, then wet oxidized at 1150°C for; b) 100 min; c) 765 min, and; d) 1300 min.[38]

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ing wafers up to 200-mm in diameter can be purchased with such a layer already deposited. (However, as we will see, such backside deposition is not compatible with 300-mmwafers.) The grain boundaries, and high degree of lattice disorder in polysilicon act as sinks for mobile impurities.

Unfortunately, extrinsic gettering techniques suffer from a variety of limitations. The primary general limitation of extrinsic gettering procedures is their inherent lack of stability, especially at high temperatures up to 1250°C for bipolar structures. Such instability manifests itself as the dissolution of gettered metal back into the wafer, and the annealing out of dislocations as the wafer undergoes a number of high-temperature steps. Upon being annealed out, dislocations can no longer trap newly introduced impurities, nor recapture the impurities released back into the wafer from getter sites. This limitation is one reason why extensive investigation of intrinsic gettering as a complementary gettering procedure has been undertaken, and why it is being increasingly implemented into ULSI fabrication sequences.

For 300-mm wafers, a *double-sided-polishing* (*DSP*) standard has been adopted. By polishing the wafer backside of the wafer (as well as the frontside), inspection of the entire wafer surface for the presence of particles can be achieved (i.e., small particles cannot be detected on the rough back-surface of a wafer). However, since the backside layer treatments of a wafer for the purposes of external gettering would have to be carried out after the DSP steps, it will no longer be possible to use them for 300-mm wafers. Hence, 300-mm wafers will have to rely on internal gettering processes.

2.8.3 Intrinsic Gettering

Intrinsic gettering is based on the principle that under proper conditions, fast-diffusing impurities are captured at sites existing within the interior of silicon wafer, away from the device regions near the surface. Two mechanisms are employed to implement internal gettering:

Gettering at Oxygen Precipitates: Supersaturated oxygen in silicon wafers will precipitate out of solution and form clusters within the wafer during thermal processing. The stresses that result as these clusters grow into larger precipitates can be relieved by punching out dislocation loops (or by emitting Si-self interstitials that agglomerate to form stacking faults and dislocation loops). These dislocations become sites at which unwanted impurities can be trapped and localized.[36] In an effectively designed intrinsic gettering process, these precipitates are only allowed to form in the bulk regions of the wafer. They are prevented from forming in the active

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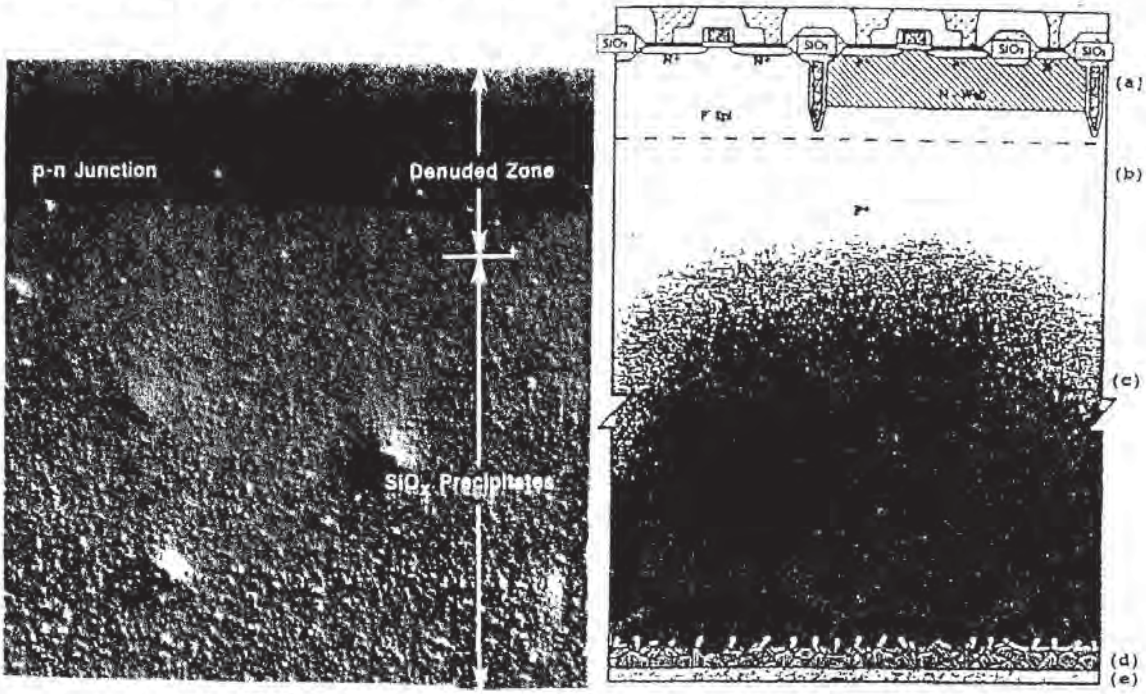


Fig. 2-14 SEM micrograph of a *pn* junction created by a 450°C anneal for 70 hr in denuded-zoned-Si with SiO_x precipitates formed by thermal treatment.[40]

device regions by reducing the oxygen concentrations to levels below the threshold required for precipitation (denuded zone formation). In this way, unwanted impurities are localized (gettered) only in regions not containing active devices (Fig. 2-14).

Gettering by Formation of Impurity Pairs: In this technique some types of metallic impurities are immobilized by chemically pairing them with other impurities deliberately introduced into the Si for this purpose. For example, Fe appears to form immobile Fe–B pairs. Thus, if regions of high B concentration are present in the interior of a wafer, migrating Fe atoms pair with a B atom and become immobilized at that location. Silicon wafers with a high bulk-concentration of B, topped with a lightly doped (e.g., $1x10^{16}$ cm^{-3}) thin epitaxial layer of Si (e.g., 3-μm-thick) can be used for this purpose. In fact, such silicon wafers have been historically used to control latchup in CMOS. Only recently has it been discovered that they are also very effective at gettering Fe through Fe–B pair formation, as described above. Recent reports indicate that a heavily doped region of B, created by a high-energy ion-implant process may be as effective in gettering Fe in wafers without an epi layer. If this claim is borne out, it may provide a less

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expensive way of obtaining the benefits of gettering and latchup protection offered by the heavily doped boron region in the Si with an epi layer.

The advantages of intrinsic gettering over extrinsic gettering include the following: **a**) the technique may be employed without any external treatment of the wafer other than heating; **b**) the volume of the wafer provides a sink during intrinsic gettering that is roughly two orders of magnitude larger than the volume of the gettering region on the wafer backside; and **c**) the gettering region in the bulk is much closer to the device regions than the backside of the wafer.[39] The distance required for impurities to diffuse from the circuit regions to the sinks is therefore 25–50 times shorter. Thus, intrinsic gettering allows diffusion cycles which are significantly shorter than those required for extrinsic gettering to remove the same contamination.

2.8.4 Gettering with Oxygen Precipitates

The first requirement for successfully implementing oxygen precipitate gettering techniques is to have appropriate oxygen concentration levels in the starting Si (i.e., 15–19 ppma). The lower limit of this range is somewhat above the threshold concentration of oxygen required for precipitation (~$6x10^{17}$ atoms/cm^3 = 12 ppma). Precipitation does not occur at a measurable rate for concentrations below the 12 ppma level.[40] Wafers from CZ-grown ingots, however, normally exceed this lower limit, with the oxygen being incorporated during crystal growth by erosion of the SiO_2 crucible. On the other hand, if oxygen concentrations exceed 19 ppma, too high a density of precipitates is formed. This may contribute to both wafer warpage and dislocation generation in the vicinity of the active devices (Fig. 2-15).[41,42]

Assume that the wafers contain appropriate concentrations of oxygen, and that the oxygen is uniformly distributed across the wafer diameter. The wafers can then be subjected to a series of temperature cycles to achieve intrinsic gettering (Fig. 2-16). A *high-low-high* sequence of such steps is then:

Step **1**. *Denuded Zone Formation* - a *high-temperature* step produces a region of reduced oxygen concentration near the wafer surface;

Step **2**. *Nucleation of SiO_x Clusters* - a *lower-temperature* step causes homogeneously nucleation of SiO_x precipitation sites;

Step **3**. *Precipitate Growth and Gettering* - a *high-temperature* step grows the SiO_x nuclei formed in Step **2** into larger oxide precipitates. The result of their growth is the formation of dislocation loops, which function as the desired gettering sites.

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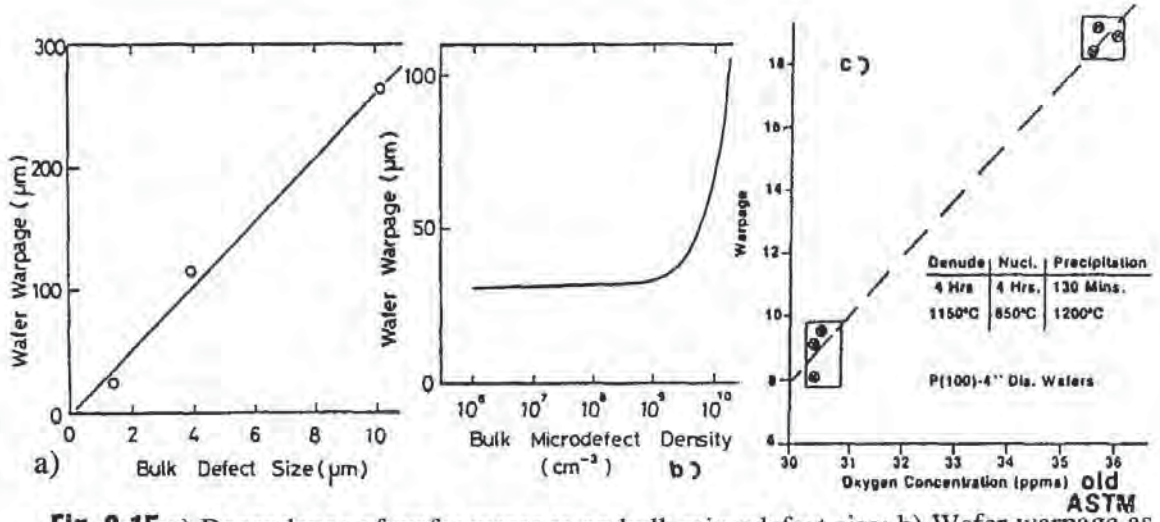


Fig. 2-15 a) Dependence of wafer warpage on bulk microdefect size; b) Wafer warpage as a function of bulk-microdefect-density.[42] c) Effect of Initial Oxygen content of the wafer on warpage.

In *Step* **1**, a region near the surface containing less oxygen than is required to form precipitates (*denuded zone*) is created. Thus, such precipitates or their punched out dislocation loops (which could intersect active device junctions or become decorated with impurities near device surfaces), are prevented from forming. Denuded zones are established by subjecting wafers to a high temperature step.[44,45,46] The oxygen near the top and bottom wafer surfaces thus diffuses out, reducing its concentration near the surface to about the solubility level

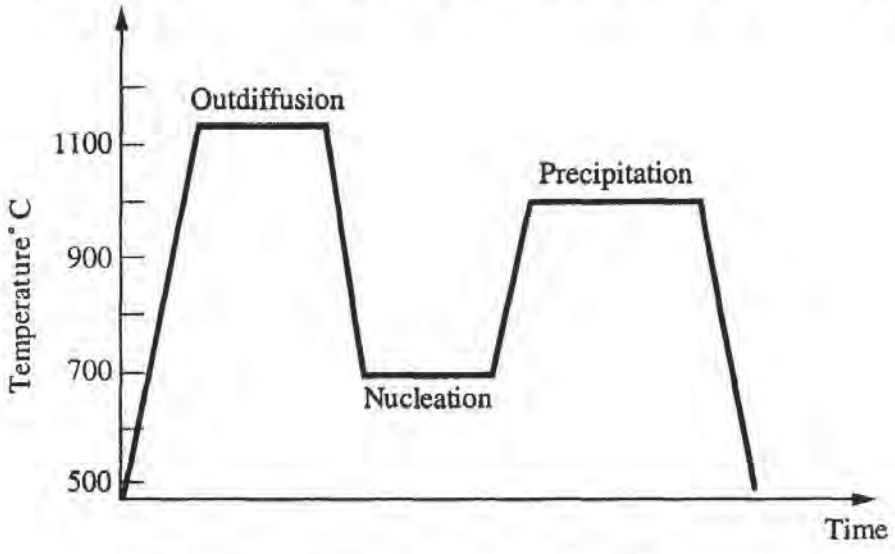


Fig. 2-16 Example of a thermal cycle to form the denuded zone.[48]

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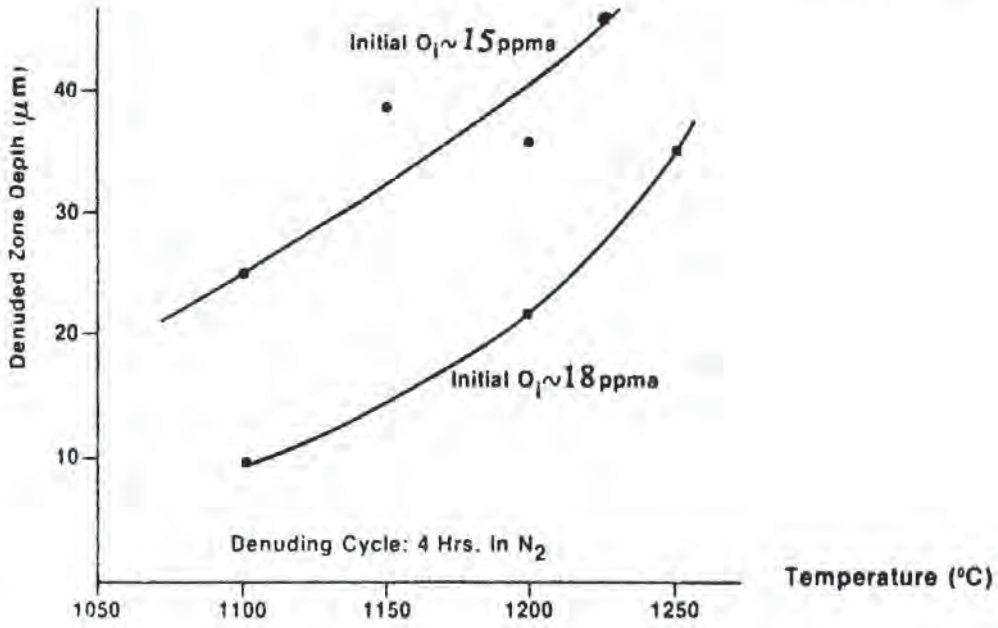


Fig. 2-17 Effect of initial oxygen concentration on the denuded zone depth.[43]

at that temperature. Denuded zones needed for a ULSI process must have a depth exceeding the deepest junction plus its surrounding space-charge region. Since the depletion region thickness depends on the wafer resistivity and the maximum operating voltage of the device, different devices made on the same substrate resistivity may need different denuded zone depths. Therefore, an important question that must be answered is: What is the shallowest denuded zone depth that the design and process can tolerate? There is no real shortcut to determining this information. Functional circuits must be fabricated on wafers containing a variety of initial oxygen levels. These circuits must be tested, and then cleaved and etched to determine the denuded zone depth and precipitate densities. Temperature cycles of 1100–1200°C for 30–240 min reportedly create denuded zones 10–40-μm deep. Figure 2-17 shows the outdiffusion depth for various temperatures and initial oxygen concentrations. Nitrogen and argon are typically suggested as appropriate ambient gases. However, it has been recommended that to avoid pitting, a thin oxide layer be grown before subjecting wafers to the high denuding temperature cycle ($\geq$ 1200°C) in these inert gases.[47]

In *Step* **2**, a lower temperature cycle (600–800°C) is next used to cause interstitial oxygen in the wafer bulk to form the nuclei required for the subsequent precipitation and gettering events of *Step* **3**. The supersaturated (interstitial) oxygen can diffuse and homogeneously nucleate into small clusters if wafers are subjected to temperatures between 650–800°C for prolonged

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periods (e.g., 4–64 hrs). Note that above 950°C, homogeneous nucleation appears to be negligible. Thus, the first temperature step on starting wafers (the denuding step) should be carried out a temperatures greater than 950°C, to prevent formation of clusters near wafer surfaces during this initial heat treatment.

A large number of relatively small oxygen clusters are formed by this step. This number, for a fixed temperature and time, depends on the oxygen content and increases with initial oxygen concentration. Since the oxygen content of the starting wafers is one important parameter that determines the density of oxygen clusters, it is crucial that this concentration be controlled in CZ silicon. Figure 2-18 shows the nucleation rate and final radius of the clusters that are created at 800°C for an initial oxygen content of 15 ppma.[47] If nucleation cycles are carried out at the lower end of the temperature range (~650°C), significantly longer annealing times are required to achieve a sufficient concentration of adequately sized clusters (16–64 hr). To enable an initial 650°C temperature to be used for this step, and yet allow a reduction in the overall nucleation cycle time, a *ramping up* of the temperature during *Step* **2** has been suggested.[42,49]

The rate of cluster formation can be enhanced by this procedure if the rate of change of the critical size, r_0, with temperature, is smaller than the rate of growth of the clusters during annealing. That is, by the time a growing cluster reaches a higher temperature, it will have grown fast enough that its size exceeds the required r_0 at that temperature.

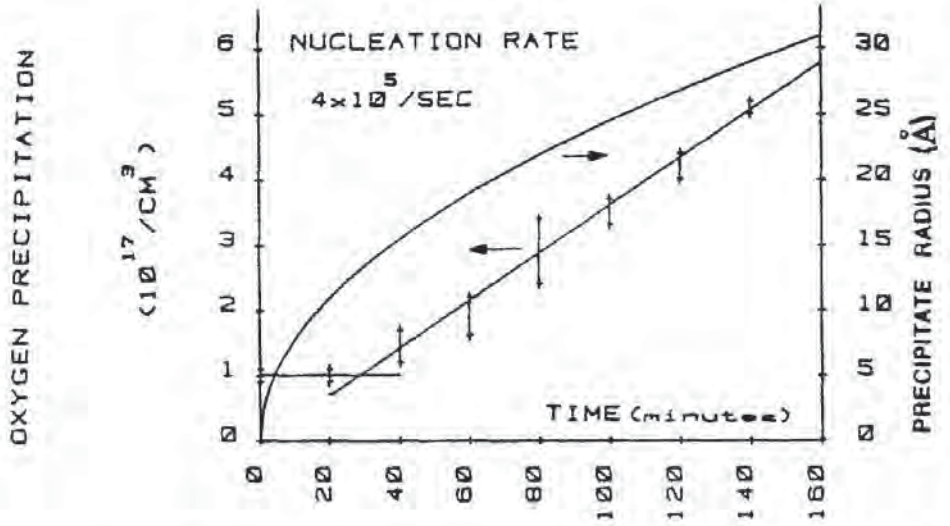


Fig. 2-18 Nucleation rate for oxygen precipitates. The curve is the expected rate of precipitate formation at 880°C.[47]

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The time to grow the clusters into precipitates that would be large enough to form the desired dislocations in the bulk is prohibitively long over the range of temperatures of *Step* **2**. Thus, once the clusters have grown to a size where they exceed the r_0 of a higher temperature step, a third thermal cycle at that temperature can be used to grow the clusters into larger precipitates in a shorter time. If a temperature-ramping technique during the nucleation cycle is used, the final temperature can be that called for by *Step* **3**.

In *Step* **3**, wafers are heated to high temperatures (900–1250°C) for extended periods (4–16 hrs). At these temperatures, oxygen clusters of a sufficient size (i.e., $> r_0$) which were formed during *Step* **2**, will grow (e.g., from 3–5-nm to ~50–100-nm in radius). Such growth is caused by diffusion of interstitial oxygen in the bulk to the SiO_x clusters, and reaction with silicon on the precipitate surface. For each SiO_2 molecule thus formed, a Si-self-interstitial is produced to accommodate the volume expansion. The large volume-change associated with the precipitation is not completely relieved by the emission of self-interstitials, and the precipitate builds up a strain field that can punch out prismatic dislocation loops (Fig. 2-19).[50]

The self-interstitials emitted by the precipitate can also form dislocation loops as discussed in the section on *Bulk Defects* in Vol.1, Ch. 2. The dislocation loops contain an extrinsic stacking fault that grows by absorbing the self-interstitials emitted by the growing precipitate. The dislocations formed from both mechanisms act as the gettering sites which can trap fast diffusing impurities.

The ultimate size of the precipitates apparently also plays a role in the warpage resistance of the wafers. Kishino[42] shows that wafer warpage increases

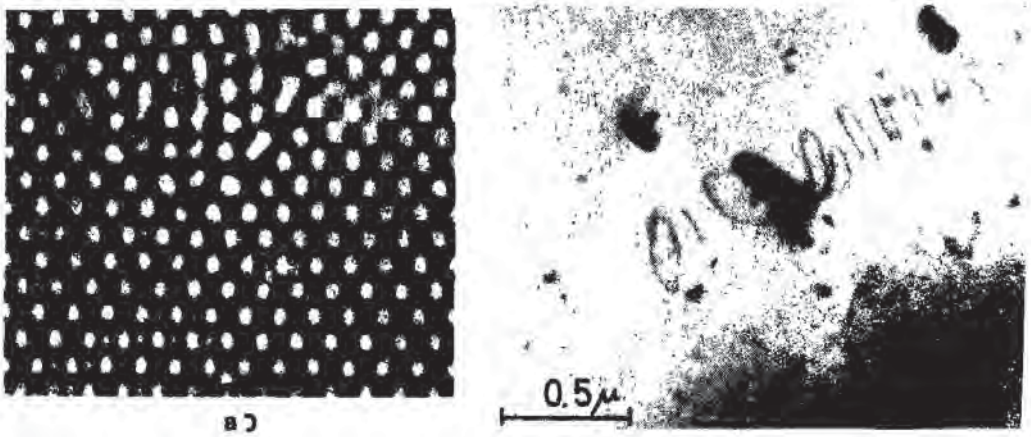


Fig. 2-19 a) Image of the core of a dislocation in Si obtained by high resolution TEM depicts an extra plane of atoms that terminates at the core of the dislocation. A precipitate is at the core.[24] (©1985 IEEE); b) Dislocation loops generated in Si due to prismatic punching by SiO_2 particles.[25]

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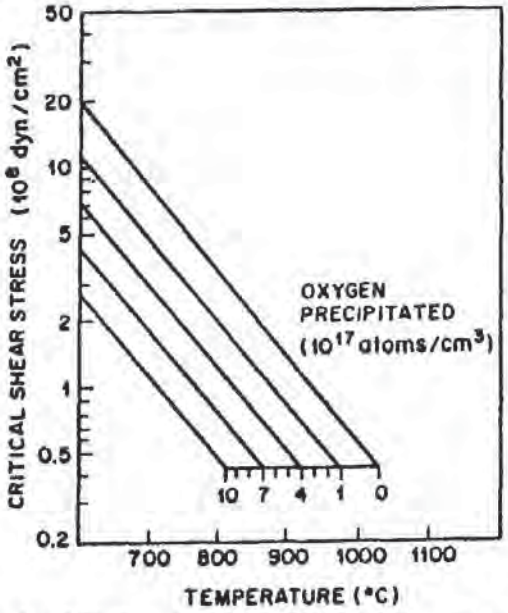


Fig. 2-20 Yield strength of Si showing the influence of oxygen precipitates.[42]

with increasing precipitate size (Fig. 2-20). These data, and that of others,[51,52] suggests that *Step* **3** heat cycles that lead to precipitates larger than 200-nm in size can negatively impact production yield. Several reports have, in fact, indicated that the best wafers are those in which the precipitation occurs slowly and uniformly throughout the wafer (especially with good radial uniformity), and which results in small precipitates with attached precipitation defect complexes.[53,54] The concern for wafer strength has lead most users of internal gettering away from materials with high oxygen levels (e.g., > 19 ppma), to material containing medium levels of oxygen (e.g., 15–19 ppma).

2.8.5 Summary of Gettering

Effective gettering is required to produce high-yielding ULSI. We have described a variety of gettering techniques, both extrinsic and intrinsic. In practice, more than one gettering mechanism has been simultaneously exploited in a wafer during fabrication. That is, the approach to gettering has been to deliberately implement more than one technique. An extrinsic, backside technique and an intrinsic gettering process were employed concurrently. Since typical CZ wafers contain oxygen in the appropriate range of 15–19 ppma, it is likely that many early IC processes had inadvertently benefited from intrinsic gettering. However, as low-temperature processes, and/or RTP, become more extensively utilized, and especially when 300-mm wafers are used, the use of intrinsic gettering can no longer be left to chance. The reduced thermal cycles in some cases, and the inability to use extrinsic gettering with 300-mm wafers will demand use of a

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gettering technique which allows the placement of gettering sinks in the wafer bulk (and closer to the device regions). The intrinsic gettering method, however, does require the strict control of a number of oxygen-related processes, and this can be a complex task.

2.9 STATUS OF SILICON WAFER TECHNOLOGY IN 2000 AND FUTURE TRENDS

By the year 2000, most 200-mm wafers being used for ULSI IC fabrication were either: **1**) conventional lightly-doped polished CZ wafers (i.e., which exhibit a grown-in defect distribution characterized by central vacancy-rich region surrounded with an OSF-ring); or **2**) conventional heavily *p*-doped CZ-silicon-substrate-wafers covered with a lightly-*p*-doped epitaxial layer. Some of the polished wafers are subjected to a post-growth high-temperature annealing step in hydrogen or argon to decrease the density of COPs at the wafer surface (see Sect. 2.5). The polished-CZ-wafers rely on both external gettering methods (e.g., backside polysilicon) and internal gettering methods which require the presence of oxide precipitates to establish gettering sites in the bulk of the wafer. The *p*-epitaxial/p^+-wafers also employ these two gettering techniques, but are able to rely on the gettering capability of the heavily doped p^+ substrate as an additional gettering mechanism (especially for such impurities as Fe and Cu). The polished-CZ-wafers usually use a deliberate process step (or steps), to create a zone near the surface denuded of oxygen (i.e., a denuded zone), to prevent oxide precipitates from forming in the device regions. Epitaxial wafers do not need to establish a separate denuded zone, as oxygen is not incorporated into the epitaxial layer during the epi deposition step (and thus such wafers automatically have a denuded device region).

As devices are being scaled below 0.18-μm and the wafer sizes are increasing to 300-mm in size, a new set of wafers types with respect to: **1**) the grown-in defect characteristics they exhibit; **2**) the gettering methods they employ; and **3**) the denuded zones they possess, will be used. Let us examine each of these characteristics.

There appear to be four types of wafers that will be offered for processes below 0.18-μm and 300-mm wafers; **1**) "perfect-silicon" wafers; **2**) fast-pulled wafers; **3**) *epitaxy-optimized substrate* wafers (EOS); and **4**) "conventional" epitaxial wafers. The "perfect-silicon" wafers are described in Sect. 2.5. The fast-pulled wafers are described in Sect. 2.7. The EOS wafers are described in Sect. 2.9.1. We compare the advantages and disadvantages of these four types of "new" wafers in Sect. 2.9.2.

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2.9.1 Epitaxy-Optimized-Substrate (EOS) Wafers

Epitaxy-optimized-substrate (EOS) wafers typically use a fast-pulled, lightly-*p*-doped wafer as the substrate, and cover it with a medium-*p*-doped, epitaxial layer that is thinner than those used in conventional epitaxial wafers The epitaxial layer in EOS wafers is not deposited thick enough so that it contains the entire device region. Its role instead, is merely to cover the COPs so that they do not degrade the isolation leakage behavior of DRAMs (and also not degrade the GOI of thin gate oxides). As noted, the COPs created in the fast-pulled substrate (i.e., a silicon crystal which may also be doped with nitrogen) are small and are formed with high density.

A thin (~0.5 μm thick), medium-*p*-doped epitaxial Si layer is thus deposited on a lightly-doped substrate. COPs are not formed in epitaxial layers because the epitaxial deposition temperature is much lower than the temperature encountered by the solidifying Si crystal in CZ growth. Thus, the vacancies created during the epitaxial process are in much lower concentrations (too low, in fact, to allow them to aggregate and form COP voids). In addition, it has also been demonstrated that the small COPs that are formed in the fast-pulled silicon which are covered with such a 0.5-μm-thick epitaxial layer are no longer detected with a surface scanning inspection system after an SC-1 delineation etch.[55,56] In fact, more thorough experimental data indicates that substrate COPs are still present after epitaxial deposition, but their morphology is radically changed. Their dimensions significantly decrease after being covered by a thin epitaxial layer (their thickness is around 2-nm, compared to 13-nm before the epi deposition), with no dependence on epi thickness detected for epi layers from 0.5 to 3.0-μm thick. Data also show a 100% GOI yield for epi layers only 0.5-μm thick. Thus, on such EOS wafers, the effects of COPs is dramatically reduced with the use of a fast-pull crystal growth process and the deposition of a very thin epitaxial layer.

Note that since these EOS wafers start with a lightly *p*-doped Si substrate, for some applications a heavily doped *p*-type buried layer (formed with high-energy ion implantation) may also be implemented. This type of buried layer would allow the latchup and gettering benefits of the heavily doped p^+-substrate (present in "conventional" epitaxial wafers) to be obtained on EOS wafers as well. EOS-type wafers are being offered commercially under such names as: fLASH® (Wacker Siltronic AG), and Epi-II® (MEMC).

2.9.2 Comparison of Grown-In-Defect Characteristics of the "New" Wafers

The four "new" types of wafers for near-future generations of ULSI circuits and 300-mm can now be compared, especially with respect to the tradeoffs among

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them involving low-grown-in defect densities, reliability of devices fabricated on each type, and cost:

1. "Perfect-silicon" wafers are beginning to be offered for mainstream production applications. However, the production of "perfect-silicon" wafers in large quantities presents some serious problems for the wafer manufacturers with respect to developing a cost-effective manufacturing process. That is, the pull-rate required to ensure "perfect-silicon" is slow, and this negatively impacts the throughput of the ingots that can be produced by an (expensive) crystal puller. Furthermore, the ingots must remain within the hot-zone of the puller for much longer periods of time, which increase the likelihood that a growth-disturbing event will occur during the growth cycle. This will further reduce the yield of acceptable ingots produced by a puller. Finally, a "perfect-silicon" growth-process must be developed for 300-mm wafers, which itself is a costly undertaking. In summary, the overall cost of "perfect-silicon" wafers for 300-mm wafer sizes may turn out to exceed the cost of even EOS wafers.

2. The fast-pulled (and perhaps also nitrogen-doped) wafers possess small-sized COPs, present in high densities. However, it has been demonstrated that the presence of COPs no longer degrades the GOI of oxides when the oxide thickness is smaller than 6.5-nm. As an example, it was reported that for MOSFETs fabricated with gate-oxides of 5-nm thickness, almost no COP failures were detected, independent of the size and density of the COPs in different crystals.[57] As a result, the use of fast-pulled wafers may be acceptable for many logic ICs, despite presence of the COPs (provided such circuit applications do not require the extremely low isolation leakage levels required by other products, such as DRAMs). Thus, such wafers might find use for a wide variety of CMOS IC circuit applications that use gate-oxide thicknesses of less than 6.5-nm-thick, built on 300-mm wafers. Of course, for some applications (such as 256-MB [and larger] DRAMS), the presence of a high-density of COPs might be the potential cause of such high leakage currents that this type of wafer would not be a suitable choice for them.

3. As described above, the EOS wafers use a lightly doped, fast-pulled substrate. Manufacturing such substrates can be achieved with higher throughput, and with a much-less-intensive process-development-effort than will be required for developing a "perfect-silicon" process for 300-mm wafers. In addition, the throughput and yield for such wafers will be

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significantly greater than for "perfect-silicon" wafers. Finally, the cost of producing such thin epitaxial layers is significantly lower than that to produce the thicker epitaxial layers used in "conventional" epitaxial-Si-wafers (up to 15-μm thick). That is, the production cost of depositing the epitaxial layer on "conventional" epitaxial wafer is a significant part of the overall wafer cost. It is possible that when all of the factors that go into the cost of producing 300-mm "perfect-silicon" wafers are compared to those that go into the cost of producing EOS wafers, that the EOS production costs will be lower.

4. "Conventional" epitaxial wafers will also probably continue to be used in 300-mm wafers, for a number of reasons. First, the p^+-substrate used in such wafers may provide latchup and gettering advantages for some circuit that may not be possible to achieve with either "perfect-silicon" or EOS wafers. The highly doped boron substrate enhances the formation of oxide precipitates as well as providing additional solubility gettering for impurity contamination. Second, a significant reduction in the epitaxial-to-polished wafer price-ratio is expected for 300-mm wafers, compared to that which existed for smaller diameter wafers. Finally, it has been observed that the COP density in highly-p-doped wafers ($2x10^{19}$ cm^{-3}) is very low,[58] and that this contributes to the excellent GOI of gate oxides fabricated on p/p^+ epitaxial wafers. Thus, despite the fact that such "conventional" epitaxial wafers will likely cost more than the other wafer types, they may still be chosen for some circuits built on 300-mm wafers.

2.9.3 Gettering Methods and Denuded Zone Formation Techniques Employed with the "New" Wafers

As noted in Sect. 2.8.3, external gettering processes based on backside wafer treatments are not compatible with the double-sided-polishing standard adopted for 300-mm wafers. Consequently, 300-mm wafers will have to rely on internal gettering processes. However, gettering sinks are even more critical today, when device fabrication increasingly uses copper interconnects (which could potentially introduce a very fast diffusing impurity in both the device region of the IC and into the IC manufacturing process lines). Let us therefore now discuss the forms of intrinsic gettering that will be available with the "new" wafers described earlier.

In the "new" wafers in which the substrate background doping is low, the intrinsic gettering capability will have to rely on gettering produced with the

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assistance of oxide precipitates in the bulk. In the "conventional" epitaxial wafers, the substrate is heavily-*p*-doped with boron. The formation of oxide precipitates is significantly enhanced by the heavy boron doping (allowing a sufficient number of oxide precipitates to be formed, even if the oxygen content in the silicon is low),[59,60] and some additional solubility gettering will occur due to the heavily-doped substrate that does not occur in the wafers with lightly-doped substrates. Hence, gettering will, in general, be more effective in wafers that have the more heavily-doped substrates (and in particular for gettering Fe). Nevertheless, in one report, it was indicated that equally effective gettering can be obtained in both the lightly-doped and heavily-doped substrates, provided that the oxygen concentration in the lightly doped substrates exceeds $7x10^{17}$ cm^{-3}.[61] By co-doping the Si with nitrogen during crystal growth, the oxide precipitate densities can, however, be significantly increased. Such nitrogen doping also acts to reduce COP sizes, as noted earlier.

Thus, to enable the use of such lower-cost "new" wafers which have a lightly-doped substrate, adequate gettering capability must be exhibited with such a substrate. To ensure that sufficient gettering capability is available, either one of two approaches is being followed: **1**) the wafers are being doped with nitrogen to enhance the number of oxygen precipitate nucleation sites; or **2**) an RTP process that manipulates the excess-vacancy-profile throughout the wafer is employed, as this allows the density of oxygen precipitate nucleation sites to be controlled.

As described in Sect. 2.8.4, part of the gettering process involves forming a denuded zone that extends from the wafer surface to a depth that exceeds the region in which device structures are formed. That is, the denuded zone is a region that is devoid of oxygen precipitates. In the "new" wafers, such denuded zones must also exist. In the case of "conventional" epitaxial wafers, the epitaxial layer is a denuded zone because there is no oxygen incorporated into the epitaxial layer as it is deposited. Hence, no oxygen precipitation will occur within the "thick" epitaxial layer of "conventional" epitaxial wafers. For the other three "new" wafer types, the denuded zone is typically formed as in conventional polished wafers with high-temperature annealing steps (>1000°C) to out-diffuse oxygen from the wafer near the surface (including the EOS wafers, in which the epitaxial layer is so thin that it does not extend deep enough to encompass the entire device region). It has been postulated that due to radical reductions in the total thermal budgets, the "conventional" methods of forming adequate denuded zones may no longer be cost effective.

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2.9.3.1 Magic DeNuded Zones™: A novel way of producing the denuded zone has recently been introduced by MEMC called the *Magic Denuded Zone* (MDZ).[TM,62,63] In this method the denuded zone (and the oxide precipitates within the bulk region of the wafer) are formed with the assistance of vacancy-concentration profiles that are introduced into the wafer with a Rapid Thermal Process (RTP) *prior* to the development of the oxygen precipitates in subsequent heat treatments. (Oxygen diffusion rates are much slower than vacancy diffusion rates in silicon.) The patented MDZ process creates a vacancy-concentration depth-profile that effectively pre-programs the oxide-precipitate-density in the bulk of the wafer, as well as the depth of the oxide-precipitate-free-zone to ideal targets. In late-2000 MEMC licensed this technology to Wacker Siltronic AG, another vendor of Si wafers, in a cross-licensing agreement involving a number of patents.

The physics of the Magic Denuded Zone concept is as follows: An otherwise perfect silicon crystal at any temperature above 0 K (e.g., room temperature) nevertheless contains an equilibrium-concentration of point defects, namely *vacancies* and *interstitials*. (For more details see Vol.1, Chap. 2, 2nd Ed.) The higher the equilibrium temperature, the higher are these concentrations. Consider a region in a bulk-silicon-crystal (i.e., far from any surface). If the crystal is heated above room temperature, thermal generation will create equal numbers of *additional* (or *excess)* vacancies and interstitials (vacancy-interstitial pairs). As long as the silicon is kept at an elevated temperature, such higher equilibrium-concentrations of point-defects will be sustained. However, if the silicon is returned to room temperature, the excess vacancies and interstitials will annihilate each other by a reverse process, i.e., recombination. Such recombination of excess point-defects will continue until the room-temperature equilibrium concentrations are restored.

The events that take place when a Si-crystal *wafer* is heated differ dramatically from when a region deep within the *bulk* of a Si-crystal is heated, due to the presence of *surfaces relatively close to any point within the silicon wafer.* The proximity to such surfaces radically alters the relative concentration of vacancies and interstitials in the heated wafer. This alteration in the relative concentrations of the two point defect types occurs for two reasons: **1**) interstitials are about 10 times as mobile as vacancies; and **2**) when either an interstitial or vacancy arrives at the surface, it is quickly annihilated. That is, when an interstitial arrives at a surface, it will quickly occupy one of the plentiful (vacant) surface lattice sites. Likewise, a vacancy moving onto a lattice site is really just a silicon atom moving from one filled site to an adjacent empty one. Since interstitials can move

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more quickly to any nearby surfaces, most vacancies trail behind. (Note that since thermal generation of interstitial-vacancy pairs is a continuous process, some vacancies are always able to recombine with interstitials. But, since the new interstitials also migrate more rapidly to the surfaces, there are always fewer interstitials within the bulk of a wafer than vacancies.) In other words, because of the inequality in point-defect mobility, and the presence of nearby surfaces, a net steady-state excess-vacancy-concentration will exist within a heated silicon wafer. The length of time from when a silicon wafer is heated to when the concentration values of interstitials and vacancies reaches their new, steady-state values is very fast – on the order of a few seconds.

If the wafer temperature is reduced to a value below its initial heated temperature (but to a value still higher than room temperature), the concentration of excess vacancies in the silicon will also eventually decrease to a new, lower, steady-state value. However, the process by which this reduction takes place in a wafer is a combination of: **1**) recombination; *and* **2**) the diffusion of vacancies to the surfaces from locations of higher concentration deep within the wafer.

The diffusion of vacancies is also dependent on temperature. At temperatures in the vicinity of 1000°C the vacancies can diffuse rapidly to the surfaces of the wafer (but of course, more slowly than the interstitials), but at room temperature the vacancy diffusion is so slow that the vacancies can be considered essentially immobile. Thus, if a heated wafer is rapidly cooled to room temperature, the concentration profile of excess vacancies within the wafer is "quenched in." In addition, by controlling the intermediate wafer temperature (and the time during which the wafer is kept at that intermediate temperature), the concentration of vacancies that will be "quenched in" at the surface can also be controlled.

MEMC has invented the MDZ process that uses RTP to produce vacancy-concentration-profiles within a wafer that are well-suited for internal gettering techniques. That is, it is known that the rate and oxygen concentration dependence of oxygen clustering can be substantially modified and controlled by the concentration of vacancies present (as was learned from studies of the oxide precipitate formation in the OSF-ring region of the wafer as was described in Sect. 2.3.2). MEMC determined that in regions of the silicon containing high concentrations of "quenched in" vacancies, the rate of formation of oxide nuclei is dramatically increased, whereas in regions where the concentrations are lower, the oxide nuclei formation rate is much slower. Thus, by creating a profile in which vacancies deep in the wafer bulk are high in concentration, the number of oxide precipitates that form there will also be high. Near the surface (and to the desired depth), the vacancy concentration is tailored to be much lower. Thus, in

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such near-surface regions oxide precipitate formation essentially does not occur, even in the presence of relatively high concentrations of oxygen. Thus, a "true denuded zone" near the silicon surface can be produced with a short RTP process after the wafers are formed - instead of with a long, high-temperature process for out-diffusing the oxygen (and which MEMC argues is not a "true denuded zone" because some oxygen nuclei may still remain from the time the oxygen concentration was high enough to have allowed them to form). On the other hand, in Si wafer regions below the denuded zone at the surface, a high number of oxygen precipitates forms, permitting an effective internal gettering scheme to be implemented. No special processing of the silicon during ingot growth (such as nitrogen doping during ingot growth) is necessary with this method.

By using the MDZ process, the density of oxide-precipitates and their depth distribution are completely decoupled from the oxygen and crystal growth influences and details of the IC thermal processes. The precipitation performance is completely controlled by the engineered vacancy-concentration-profile. In addition, the denuded-zone-depth and bulk-oxygen-precipitate-density may be engineered independently *of one another* by this technique. The denuded zone is also formed without the requirement of oxygen out-diffusion. The entire MDZ process is accomplished in less than one minute, and is therefore much faster if compared to the average oxygen diffusion process (that takes several hours).

MDZ provides internal gettering that is nearly independent of initial oxygen concentration, wafer position along the ingot, and thermal history effects. Since the MDZ process is also independent of the crystal growth-process, accurate MDZ performance may be achieved on any type of wafer. This means that the oxygen precipitation process is effectively decoupled from the crystal-growth-related intrinsic-point-defect issues.

2.10 FROM INGOT TO FINISHED WAFER: SLICING, ETCHING, and POLISHING

After a single crystal ingot has been grown, a complex sequence of shaping and polishing steps are performed to produce starting material suitable for fabricating semiconductor devices (*wafers*).[65,74] The wafering process for 300-mm wafers has been modified to some degree compared to ones used for previous wafer generations. We will emphasize those differences in this section. Figure 2-21 shows a flow chart depicting a generic 300-mm wafer shaping process. Figure 2-22 also illustrates this *wafering* procedure, which includes the steps covered next.

2.10.1 Ingot Evaluation

The grown single crystal ingot undergoes routine evaluation of resistivity, impurity content, crystal perfection, size, and weight. Sections of the ingot that

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are crystallographically defective, irregularly shaped, or undersized, are cut off and discarded (as are the seed and butt [or *tang*] ends). Loss of the ingot material may approach 50% at this point.

2.10.2 Ingot Surface Grinding

Since ingots do not grow perfectly round, nor with sufficiently uniform diameters, they must shaped to the desired form and dimension. Thus, ingots are deliberately grown larger than the final desired wafer diameter and a grinding operation removes the excess material to reduce as-grown crystals to a cylindrical shape of precise diameter. (Exact diameter dimensions are required to make wafers compatible with automated handling procedures.) Since silicon is a hard, brittle material (registering 72.6 on the Rockwell "A" hardness scale), grinding machines with diamond wheels are used to perform this cylindrical shaping process. The grinding step is followed by an etch step that removes the grinding work-damage. The ingot diameter is reduced 0.25-1.0-cm by the grinding and etch steps.

2.10.3 Grinding Flats or Notches on the Ingot for Orientation Purposes

For wafers up to 150 mm, *flats* are used for aligning and crystal orientation. For larger wafers ≥ 200 mm, *notches* are predominantly used (see Fig. 2-23). For 300-mm wafers, notches are used exclusively. These features are next ground along the length of the ingot. The largest flat, called the *primary flat*, is usually positioned relative to a specific crystal direction. (The primary flat orientation is found by using X-rays to produce a Laue photograph.) The primary flat is used for several purposes. Automated wafer handling equipment utilizes the primary flat to obtain correct alignment, and in addition, devices on the wafer can be oriented to specific crystal directions with this flat as a reference. Smaller flats are called *secondary flats*, and they are utilized to identify the orientation and conductivity type of the wafer. Since automated equipment relies on the flats for correct operation, the flat dimensions must be precisely machined. For example, the flat or notch is placed perpendicular to a <110> direction on a (100) wafer.

2.10.4 Sawing the Ingot into Slices (Wafers)

The sawing operation[66,74] that produces silicon slices from the shaped ingot also defines the surface orientation, thickness, taper, and warp of the slice. The ingot is rigidly mounted to maintain exact crystallographic orientation during the sawing process. Wafers of <100> orientation are normally cut "on orientation" (e.g., within ± 0.5°).

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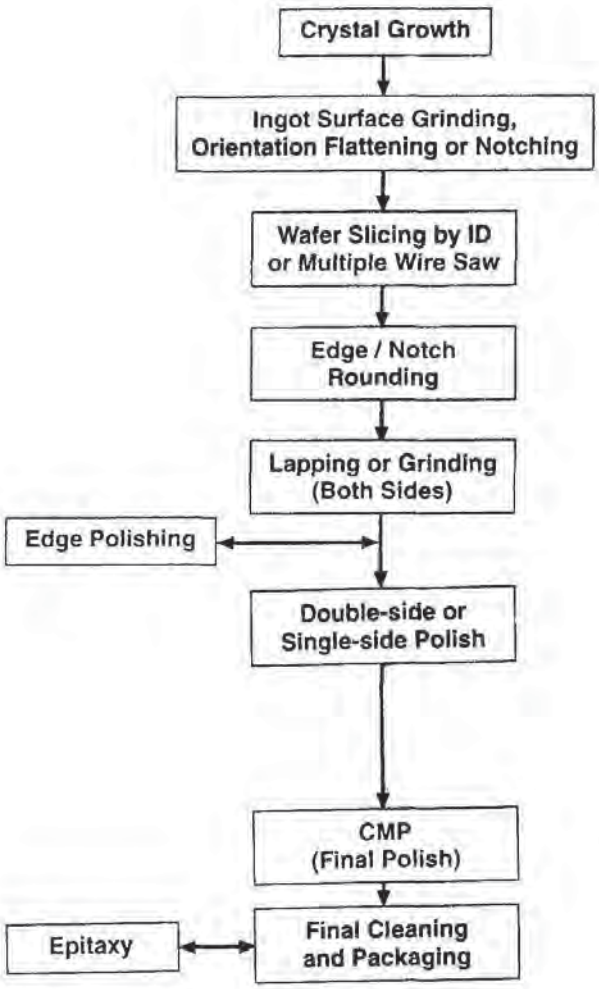


Fig. 2-21 Flow chart depicting the steps involved in wafer preparation starting with a whole Si ingot.

Wafer thickness is primarily set by the sawing operation, although some material is also removed by subsequent operations (e.g., for a 200-mm wafer of final 725-μm thickness, a total of ~1250 -μm of ingot silicon is needed: 725-μm final wafer thickness; 400-μm for kerf loss during sawing; 50-μm lapping loss; 50-μm etching loss; 25-μm polishing loss. Thus, about 8, 200-mm wafers per linear cm of ingot can be produced. As wafers get larger they must be thicker (Table 2-1) to allow them to withstand thermal processes (e.g., epitaxy and

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oxidation) and handling during fabrication. Thus, fewer wafers per unit length of ingot are possible than for smaller wafers.

The most common mode of slicing has been *inner diameter* (ID) *slicing* (Fig. 2-24) using stainless steel blades with diamond particles bonded to their edges.[74] Continuous monitoring with blade-deflection sensors is required to assure that slices are sawn adequately free of bow, taper, work damage, and saw marks. Cutting speeds are in the neighborhood of 0.05 cm/sec. Since one slice is cut at a time by the saw, this is a relatively slow process.

Wafers with 300-mm diameters are sawn with slurry-coated wires instead of inner-diameter saws. More slices per inch of ingot are possible due to smaller kerf loss (kerf loss is reduced by approximately 30% compared to the ID saw).[67] In addition, wire sawing enables the silicon slicing to be carried out at higher throughput and superior mechanical properties, such as reduced bow and warp. Figure 2-25 shows a schematic of multiple-wire saw. In this arrangement, parallel, equally spaced and properly tensioned stainless steel wires spun across two pulleys are part of single stainless-steel wire winding through a complex set of pulleys. Cutting of multiple slices results when the ingot is pressed against the traveling wires under injection of slurry. Although the cutting rate is much slower than the ID saw (the ordinary ID saw has a 80-100 times higher sawing

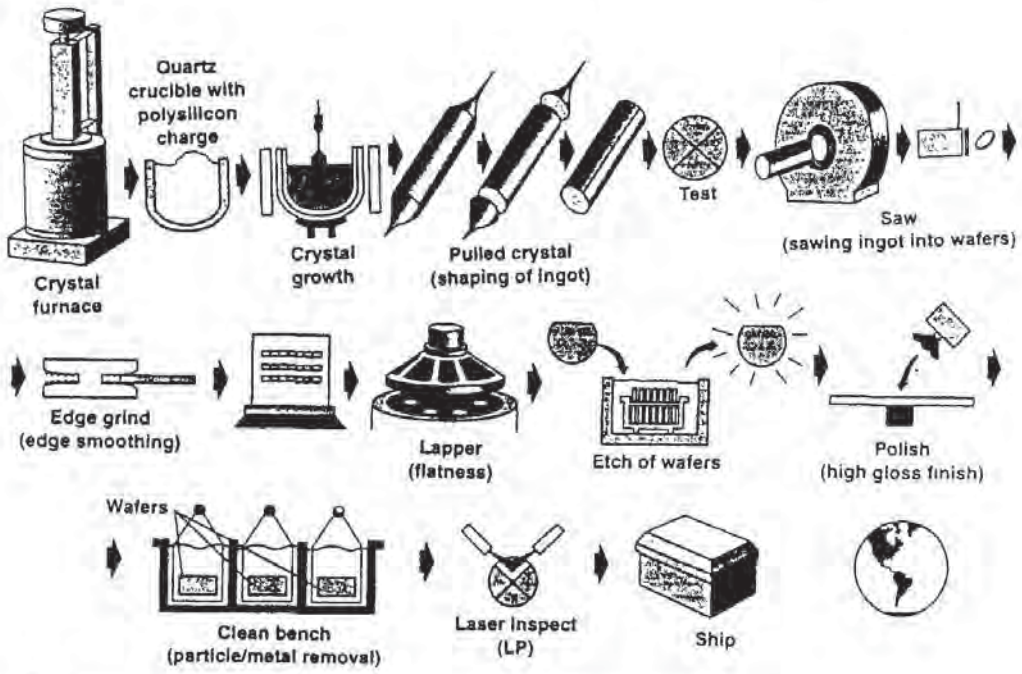


Fig. 2-22 Graphical depiction of the steps in the wafering process.

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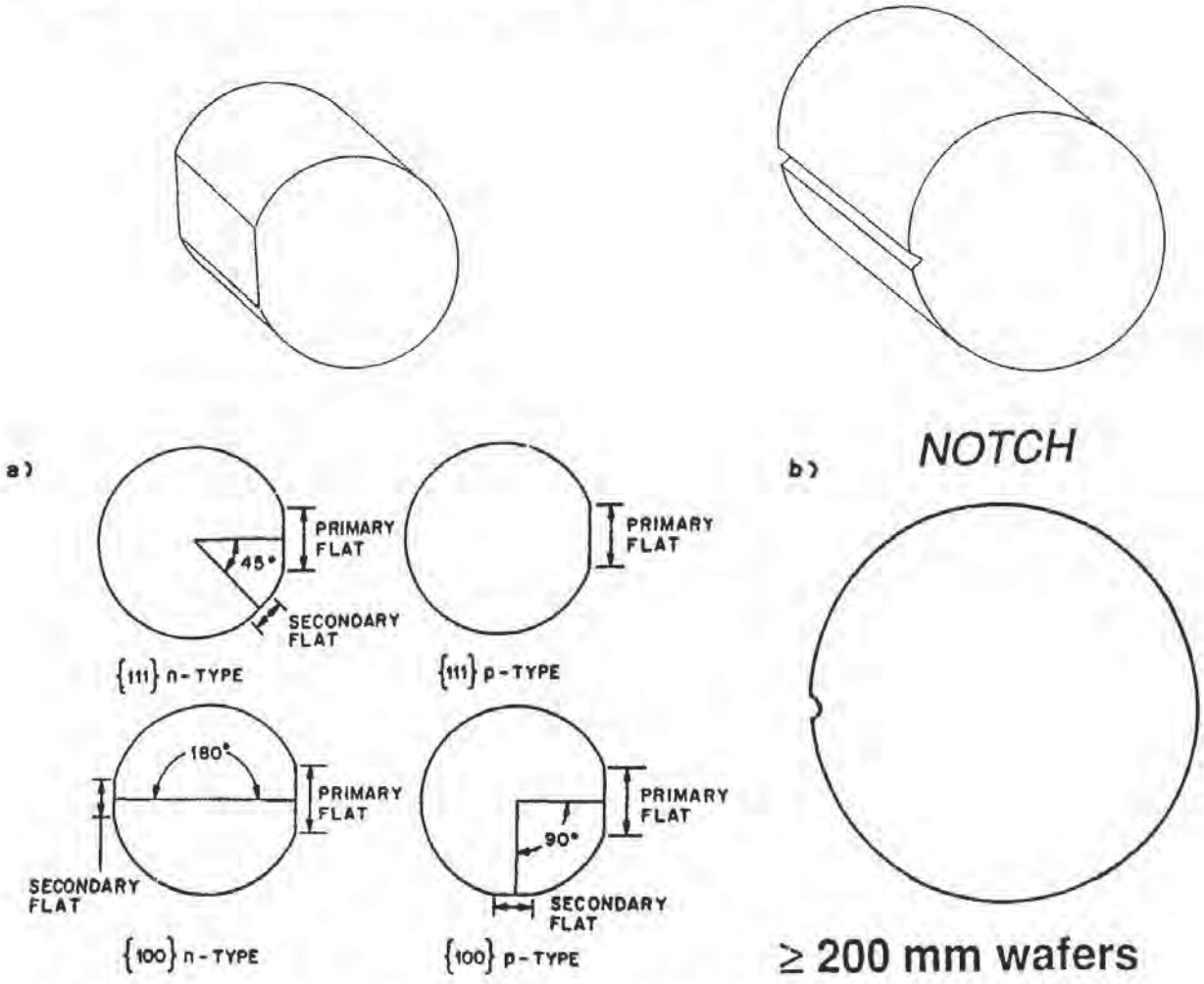


Fig. 2-23 a) Identifying flats on a silicon wafer; b) Notched wafers.

rate), as many as 300 slices can be produced simultaneously. Since slicing by the multi-wire saw is actually the result of low speed grinding action by the slurry, improved bow, warp, TTV, and taper are much more easily obtained than with the ID saw.

2.10.5 Laser Marking the Wafers

A technique using a *laser* to create an alphanumeric (or bar code) identification mark on the front of the wafer near the primary flat or notch (Fig. 2-26) is then employed. *Laser marking* according to SEMI[68] Std. M 1.8, specifies an 18 character field to identify the wafer manufacturer, conductivity type, resistivity, flatness, wafer number, and device type. This allows each wafer to be identified. Wafer traceability, correlation of device characteristics produced on a wafer with the wafer properties, and the ability to prevent in-process rejected wafers from being re-inserted into the fab line are all benefits of utilizing wafer marking.

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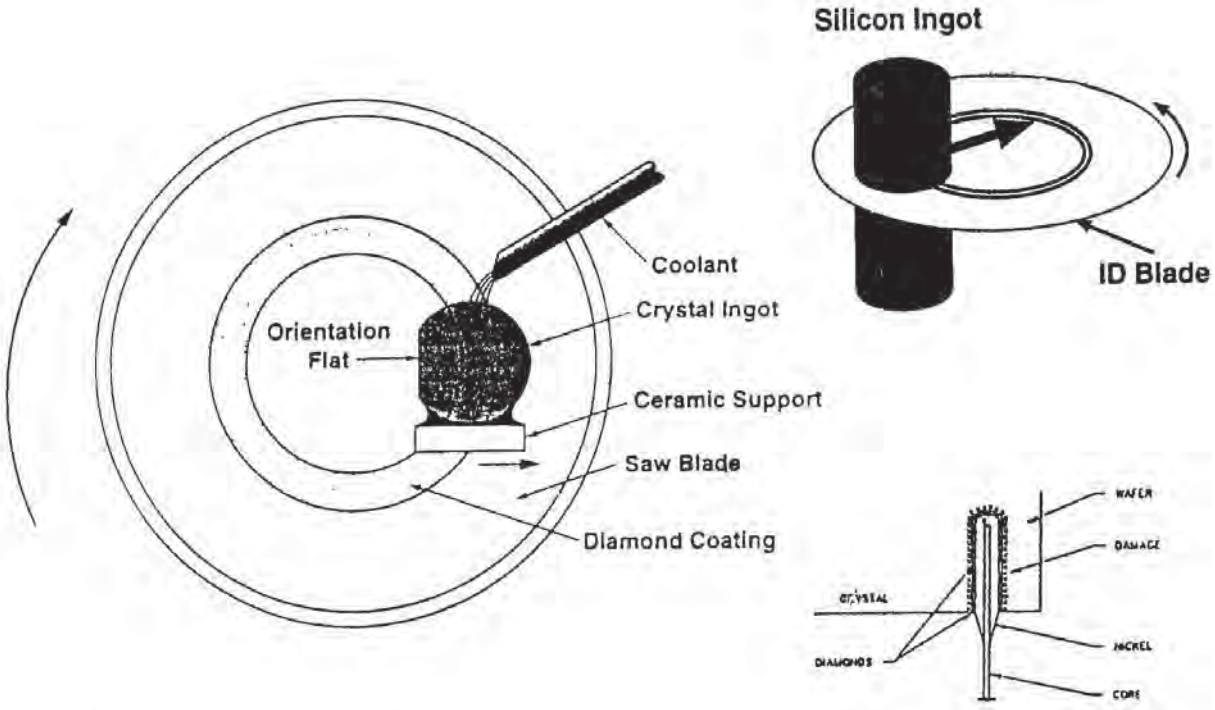


Fig. 2-24 ID saw geometry.[66]

Automatic code readers at various stages of processing can also track wafers and provide data on wafer movement in the fab.[69,70]

2.10.6 Lapping and Grinding the Wafers

The thickness of the as-sawn slices is sufficiently variable that a *lapping* and *grinding* step is next employed to bring all slices to within the specified thickness

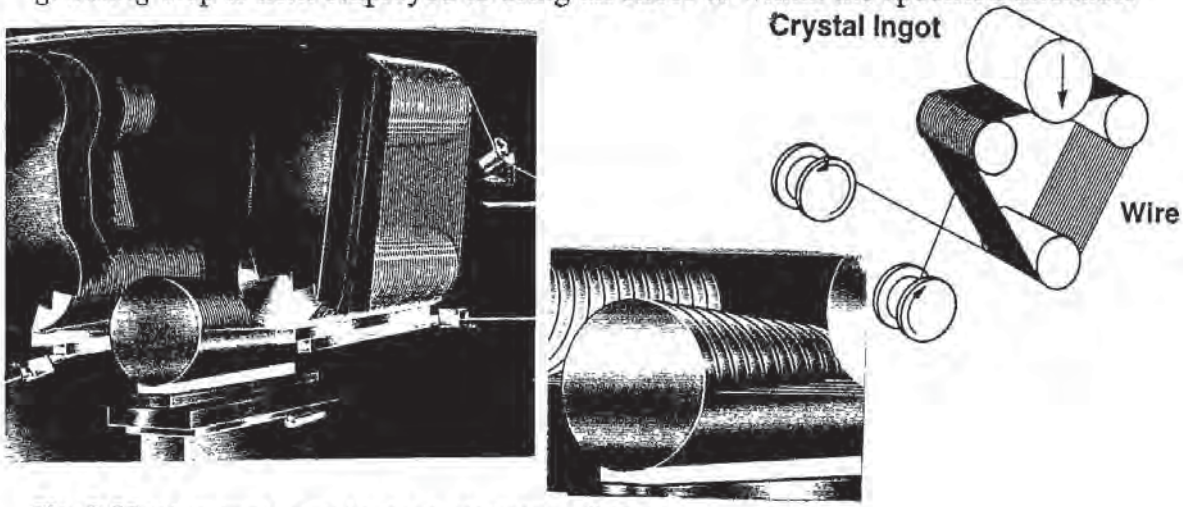


Fig. 2-25 Wire sawing an ingot to produce wafers.

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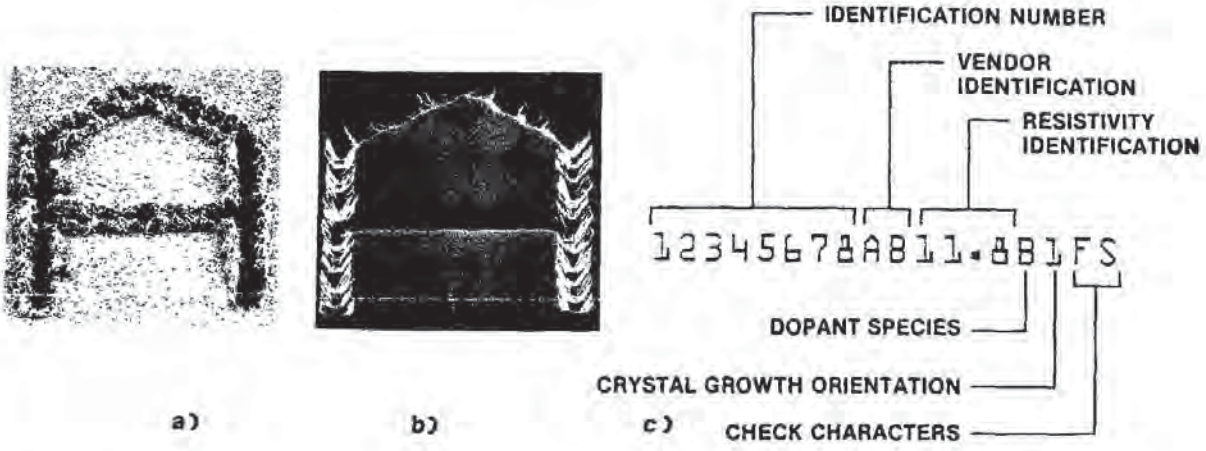


Fig. 2-26 a) SEM of letter "A" marked on wafer after it appears as marked on lapped wafer (left), after wafer has been etched (center), and after polishing. Courtesy of Wacker Siltronic; b) SEMI specification for marking vendor codes on wafers. Dimensions are specified along flat on wafer; c) SEMI specifications for 18-character vendor code. SEMI standard, used with permission.

tolerance. The lapping takes place between two counter-rotating cast-iron plates in the presence of an abrasive slurry, usually a mixture of micron-sized alumina or silicon carbide particles suspended in a solution. This step also serves to reduce bow and warp, and to increase slice flatness. Both sides of the slice are lapped using a mixture of Al_2O_3 and glycerine, and a succession of increasingly finer polishing grits is used in multiple lapping steps. This process can achieve flatness uniformities of 2-μm.

2.10.7 Removal of Surface Mechanical Damage by Chemical Etching

The work damage and contamination caused by the previous mechanical grinding, sawing, and lapping steps must be removed. This is done by chemically etching away the resultant damaged and contaminated layer.[71] The wet etch procedure for this step typically utilizes an etchant solution of hydrofluoric (HF) and nitric (HNO_3) acid (with modifiers such as acetic acid) to attack the silicon. The surface material removal is the result of two-step reactions. The Si surface is first oxidized by the nitric acid to form silicon oxide, and this oxide removed by the HF. A relatively non-porous and clean wafer backside is also produced by this step. Note that etching of the wafer may be repeated after the subsequent operation of edge rounding.

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2.10.8 Rounding the Wafer Edge (and Notch)

The edges of the silicon slices are then shaped (rounded) as shown in Fig. 2-27. Edge rounding substantially reduces the incidence of chipping during normal wafer handling, and helps minimize film buildup on the edge of the wafer during photoresist and epitaxial processes. (Edge-chip defect sites are known to nucleate plastic deformation [or *slip*] during subsequent thermal processing steps).[72] The shape of the rounded edge profile usually follows an industry standard (i.e., SEMI standard) in which the edge profile fits within the boundary of a standard template.

2.10.9 Edge Polishing of the Wafers

Particle contamination reduces yield. In advanced, submicron IC processing some of the major sources of particles are the process equipment and the wafer itself. Defects found on the wafers during the device fabrication sequence are often caused by tiny chips of silicon from the wafer, or by particles removed from the process equipment. This abrasive effect is caused by the contact of the silicon wafer with the process equipment, and can be influenced by the smoothness of the contact area, primarily the wafers edge.

Wafer edges of as-sawn wafers are sharp and prone to chipping (Fig 2-27a). As a result, after sawing, wafers are generally subjected to a grinding process that rounds the wafer edge (with much of the edge-grinding damage being later removed during the wafer-surface etching process). This results in a wafer edge that is rounded, but is not perfectly smooth, as shown in Fig. 2-27b.[64] Such relatively rough edges still produce enough particles to reduce the yield of ICs, when compared to the yields obtained when these edges are polished after the edge has been etched to remove the grinding damage. That is, after edge-polishing the wafer edge is perfectly smooth, as shown in Fig. 2-27c, and indications are that the defect density on wafers is reduced if their edges are so polished. For the future generations of ICs that will produced on 300-mm wafers, the benefit of edge-polishing should be even more pronounced. That is, the wafer-edge area increases with increasing wafer radius and thickness. In addition, it appears that other particle sources on the wafer topography (such as the notch and deep laser scribe marks), must also be polished (or in some other way smoothed) to further reduce defect density.

2.10.10 Chemical-Mechanical Polishing of the Wafers

A chemical-mechanical polishing[71] step is used to produce the highly reflective, scratch- and damage-free surface on one or both sides of the wafer. This is

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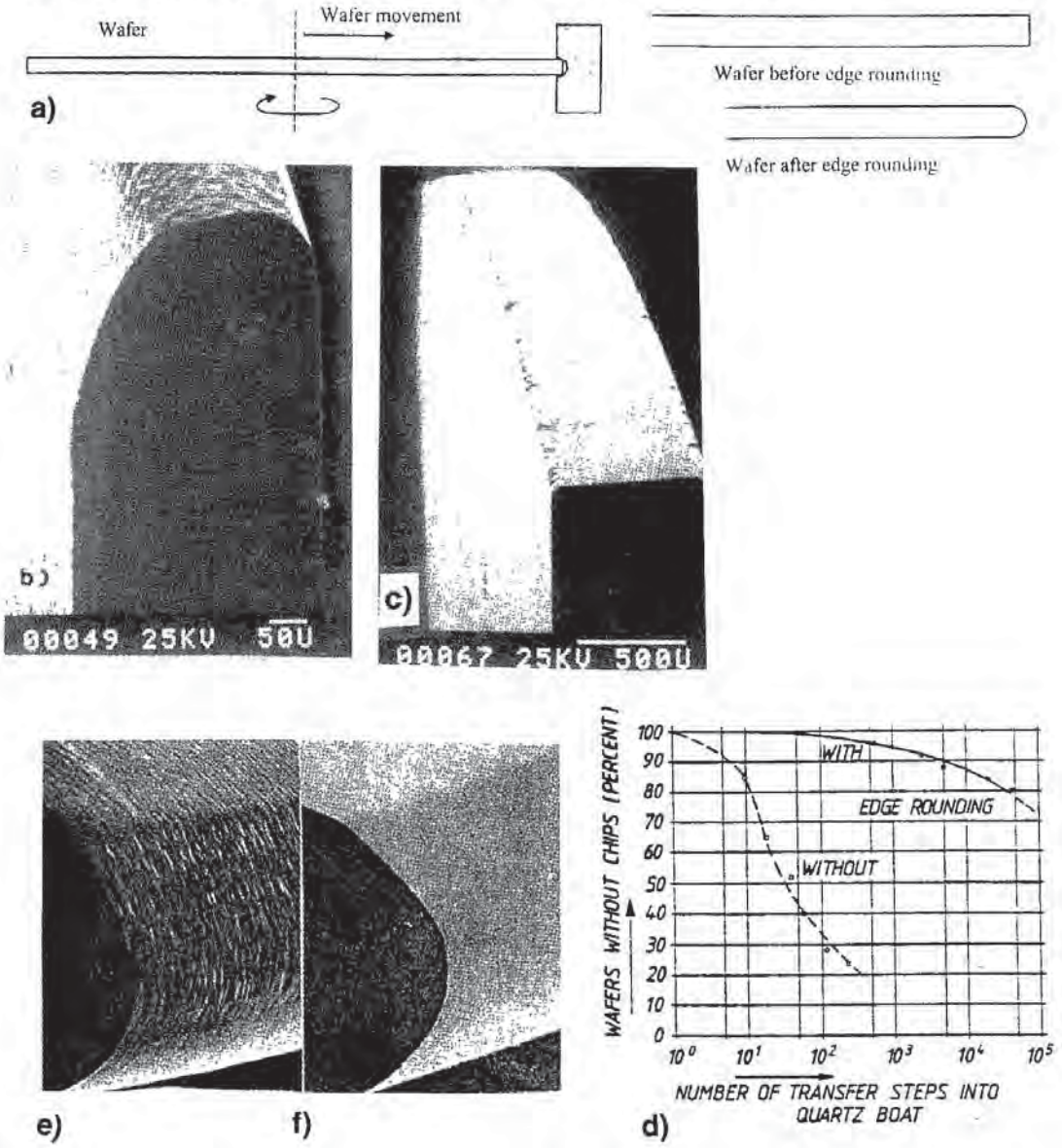


Fig. 2-27 a) Wafer edge-rounding process; b) Edge-rounded wafer; c) Non-edge rounded wafer; d) Mechanical strength of edge-rounded vs. non-edge-rounded wafers; e) Edge-rounded, but non-polished wafer; f) Edge-rounded, polished wafer.

accomplished by mounting unpolished slices onto a carrier, and then putting them on a polishing machine. There, a powered platen drives an appropriate polishing pad material across the wafer surface. A colloidal silica slurry of sodium hydroxide and fine (~10-nm) SiO_2 particles is dripped onto the table. The frictional heat of the sliding mounted wafers causes the sodium hydroxide to oxidize the Si (i.e., the chemical part of the process). The oxide is then abraded away by the silica particles (i.e., the mechanical part). Figure 2-28 shows the

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wafer thickness and surface roughness changes as it undergoes the various grinding,, lapping and polishing processes.

For 300-mm wafers, double-sided-polishing will be standard (instead of the single-sided-polishing used up to the 200-mm wafer sizes). Double-sided polishing (CMP on both the front and back surfaces simultaneously) has been found to result in superior flatness than single-sided polishing.

The wafer preparation via mechanical methods (i.e., grinding, CMP, etc.) has its limits in the degree of flatness that can be obtained. To supplement and fine tune the local lithography for further improvement in local flatness, tools that can carry out such processes as *plasma-assisted chemical etching* (PACE) have been developed.[73] Such a tool employs a spatially confined plasma with a scanning mechanism to allow material removal to be controlled as desired over the wafer surface. The PACE utilizes low-energy ions (i.e., << 1 eV), instead of the energetic ions that are employed in reactive-ion-etching. Therefore, PACE produces minimum or no subsurface damage.

2.10.11 Cleaning the Wafers

Following the polishing cycle (in which a layer of silicon about 25-μm-thick is removed) the wafers are subjected to series of chemical dips and rinses to remove the polish slurry. A cleaning process concludes this step. This is a very important

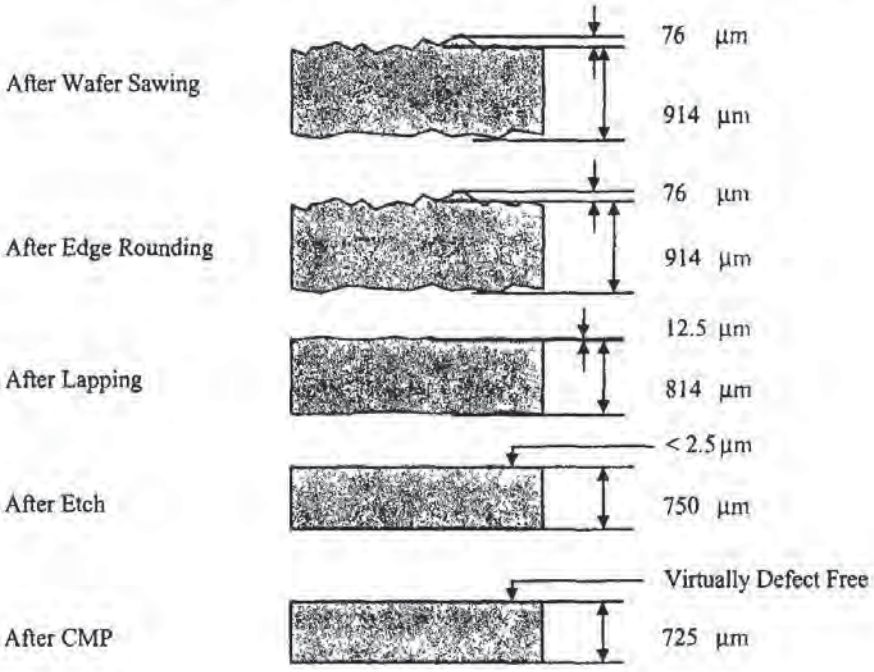


Fig. 2-28 Wafer thickness and surface roughness changes during grinding and polishing.

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step as the silicon wafer must be free of contamination before it is shipped to the device fabrication facility. Chemical cleaning is effective in removing contaminants from the wafer surface. The "RCA Clean" (see Vol. 1, Chap. 5) is widely used to clean the wafer before shipping.

2.10.12 Depositing Epitaxial Silicon Layers on the Wafers

Epitaxial layers are required for some ULSI process technologies. Wafer manufacturers are now supplying silicon wafers with a variety of epitaxial layers for CMOS ULSI technologies. Another option being offered is a layer of polysilicon or mechanical damage on the backside of the wafers for extrinsic gettering purposes.

2.10.13 Shipping 300-mm Wafers: Its Impact on the Evolution of Wafer Shipping Boxes

An inspection, followed by packing in a particle-free package finishes the wafering sequence. The box used to ship 300-mm wafers is called a *front-opening shipping box* (FOSB, pronounced *fos-bee*). FOSBs cost approximately 10 times as much as the boxes that are used to ship 200-mm wafers. The main reason for this cost discrepancy is that the 300-mm wafer is more susceptible to breakage because it is *proportionately* thinner than previous diameters. Consequently, the shipping package must provide more protection. In addition, the FOSB must be more rigid in order to interface with automated load ports.

Since the cost is so high, it must be possible to re-use the FOSB. In fact, as shown in Fig. 2-29, if the FOSB is used only once, the cost per wafer to use it is ~$15, whereas if it is reused 10 times, the cost per wafer drops to ~$7. Neverthe-

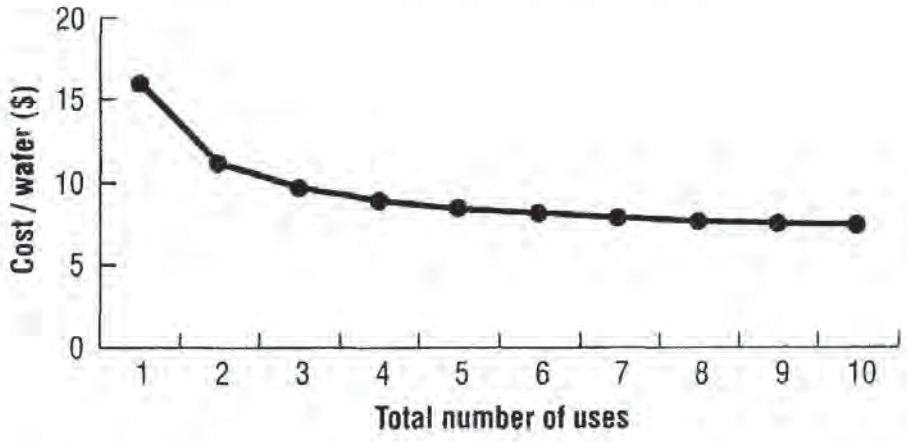


Fig. 2-29 The cost/reuse of a FOSB levels off at $7/wafer.

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less, the overall cost of the box to ship the wafer is at least 55% higher for 300-mm wafers than for 200-mm wafers.

One topic being discussed concerns the issue of FOSB ownership. One proposal before the SEMI 300-mm Wafer Shipping Box Taskforce is that manufacturers become owners of the FOSB. That is, since device manufacturers want a guarantee of wafer cleanliness, the best way to supply this is to maintain completely control the FOSB history. Ownership of the FOSB makes this possible. The protocol for using the FOSB is to remove the wafers upon receiving them from the wafer supplier, to then seal the FOSB in a polypropylene bag and ship it back to the wafer producer. The FOSB is like a wafer. Once it gets contaminated, it becomes hard, or impossible to clean.

2.11 SPECIFICATIONS OF SILICON WAFERS FOR VLSI

There are many properties that a wafer must exhibit (Table 2-2) in order to be an appropriate starting substrate for the fabrication of VLSI and ULSI. Table 2-3 provides some typical specification ranges for 125-, 150-, and 200-mm diameter CZ wafers. Figure 2-30 graphically summarizes the qualitative characteristics desired in 200-mm device quality Si wafers for ULSI circuits.[75] The semiconductor industry has seen quality improvements in Si crystals grown by the CZ technique continually over the years. In today's emerging sub-0.13-μm IC manu-

Table 2-2. COMPARISON OF MATERIAL PROPERTIES AND REQUIREMENTS FOR VLSI AND ULSI

Property	Czochralski	Float Zone	Requirements for ULSI
Resistivity (phosphorus) *n*-type (ohm-cm)	1–50	1–300 and up	5–50 and up
Resistivity (antimony) *n*-type (ohm-cm)	0.005–10	–	0.001– 0.02
Resistivity (boron) *p*-type (ohm-cm)	0.005–50	1–300	5–50 and up
Resistivity gradient (four point probe) (%)	5–10	20	< 1
Minority carrier lifetime (μs)	30–300	50–500	300–1000
Oxygen (ppma)	5–25	Not detected	Uniform and controlled
Carbon (ppma)	1–5	0.1–1	< 0.1
Dislocation (before processing) (per cm^2)	≤ 500	≤ 500	≤ 1
Diameter (mm)	up to 300	up to 100	up to 300
Wafer bow (μm)	≤ 25	≤ 25	< 5
Wafer taper (μm)	≤ 15	≤ 15	< 5
Surface flatness (μm)	≤ 5	≤5	< 1
Heavy-metal impurities (ppba)	≤ 1	≤ 0.01	< 0.001

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TABLE 2-3 SPECIFICATIONS FOR SINGLE-CRYSTAL SILICON WAFERS

Parameter	150 mm	200 mm	300 mm
Diameter (mm)	150 ± 0.2	200 ± 0.2	300 ± 0.1
Thickness (μm)	675 ± 25	725 ± 20	775 ± 25
Primary flat length (mm)	55–60	notch	notch
Oxygen content (ASTM '79) (ppma)		≥ 23 ± 2	≥ 22 ± 1.5
Flatness (μm) (GTIR)	1.5	1.5	1.5
Site Flatness (μm) (SFQD)		± 0.17 (1998)	± 0.12 (2001)
Surface orientation	(100)	(100)	(100)

facturing, 200-mm and 300-mm wafers must meet ever tightening wafer quality requirements in terms of the crystalline defects, heavy-metal impurities, oxygen level, oxygen radial uniformity, minority-carrier lifetimes, particles, and flatness.

Note that these specifications have also become tighter with increasing wafer size due to automatic wafer handling and photolithographic requirements. ADE Corporation is the major supplier of tools used to measure many of these specifications. While 300-mm wafers are just being introduced into full-scale IC production, the required quality as updated in the 1999 *Technology Roadmap for Semiconductors* (Table 2-4, p. 69) will be met by further developing and refining crystal growth technology being applied and developed for 200-mm wafers, particularly as it is applied to point-defect and secondary-defect control, and the control of oxygen.

Some questions have arisen, however, about whether some aspects of wafer "goodness" may be specified too tightly, especially with respect to contaminant levels in the silicon. That is, it may be necessary to balance "best wafer possible" against the cost of ownership opportunity of not driving silicon requirements to the detection limit, but to some less stringent value consistent with achieving high yield. This issue is important, as the cost of a 300-mm wafer is projected to account for as much as 30% of the total IC wafer processing cost.[76]

There has been a variety of data in the literature to support such a view.[77] One example, described earlier, is that the specification on the limits of COPS and metals may be relaxed for device technologies in which thinner gate dielectrics are employed. For example, at gate-oxide thicknesses of 5-nm or less, the influence of COPS on gate-oxide-integrity (GOI) has been found to become negligible for CZ polished wafers.[78] (On the other hand, at the 0.1-μm node, the device features will approach the size of the void diameters, and this might cause

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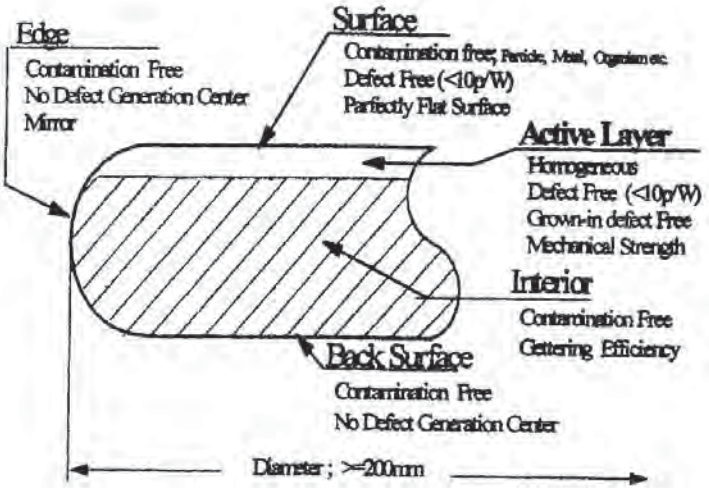


Fig. 2-30 Silicon wafer structure required for ULSI.[65]

shorts, e.g., between adjacent trench capacitors in a DRAM.) Furthermore, gate oxidation is generally performed after a number of prior thermal processes which typically annihilate near-surface COPs, thereby reducing whatever residual influence these defects may have on the GOI. In addition, in epitaxial material, the COPs are covered up to a depth beyond ~100 nm, essentially negating their influence. Accordingly, the necessity of using "perfect-silicon" (while being a remarkable scientific achievement, see Sect. 2.6), apparently needs to be reassessed for future generations of ICs from a cost-of-ownership perspective.

The implications of thin-gate-oxides for the specification of the metal levels in the Si wafer are based on the paradoxical fact that the integrity of thinner gate oxides may be less compromised by metals than is the integrity of thicker oxides.[79] A second reason that the maximum allowed levels of metal in the silicon may be allowed to be increased is that cleaning technologies have been improving, allowing the incoming critical metal level specifications to be somewhat higher than those now in use. This is because the improved cleaning processes drive the initial levels of metal down to an operational level that is an order of magnitude smaller than the initial level.

The utilization of multiple-well structures fabricated by ion-implantation in effect decouples the MOSFETs from the original silicon material characteristics. This reduces the sensitivity of these devices to the initial resistivity- and uniformity-tolerance of both CZ polished and epitaxial wafers. Whereas the nominal substrate doping for epitaxial wafers is typically in the range of ~5-10 mΩ-cm (to ensure latch-up control), shallow-trench-isolation (STI) is rendering

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classical concerns for latch-up, such as n^+-p^+ spacing moot. Accordingly, resistivity ranges ≥20% may be acceptable, also favorably impacting CoO.

Internal gettering (IG) in CZ-polished-Si wafers will still be required to remove deleterious metallic contaminants inadvertently introduced during IC processing. A ±2 ppma variation in bulk oxygen concentration in the range ~18-31 ppma (old ASTM standard) may be sufficient to ensure stringent bulk defect control with an acceptable homogeneous IG capability. Adequate wafer strength and resistance to warpage, along with denuded-zone width control, is also required. The utilization of heavily-boron-doped substrates for epitaxial wafers also offers an effective IG capability, especially for gettering Fe.

In summary, it appears that calling for further reduction of various contaminants and defects in Si wafers (and the continued drive to reduce certain other wafer specifications) may not necessarily be required to ensure continued improvements in IC performance.

2.12 THE ECONOMICS OF SILICON WAFERS

As discussed earlier, the size of silicon wafers has been continuously increasing. The motivation for using larger wafers is economic, and here we discuss this issue. The economic benefits of larger wafers are gained from the additional silicon area they provide (Fig. 2-31). If the manufacturing cost per wafer remains constant (or if its percentage increase is smaller than the percentage increase in silicon area) a reduction in the manufacturing cost per chip may be possible.

Let us address the issue of the silicon wafer costs. We see from Fig. 2-32 that the cost per square inch of silicon on a given wafer size is highest when the new wafer size is first introduced, but then drops with time.[80] For 125-mm prime

Diameter Increase	Percentage Area Increase
2" → 3"	125%
3" → 100 mm	78%
100 mm → 125 mm	56%
125 mm → 150 mm	44%
150 mm → 200 mm	78%
200 mm → 300 mm	125%

Diameter	Area (Sq. Inches)
2 Inch	3.1
3 Inch	7.1
100mm	12.6
125mm	19.6
150mm	28.3
200mm	50.2
300mm	109.5

Fig. 2-31 The increase in silicon wafer area with increasing wafer diameter.

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device wafers the minimum silicon cost reached ~$1/in^2. For each succeeding wafer size the minimum cost/in^2 is expected to be 1.4x the cost of the previous generation. Thus, for 200-mm wafers the silicon cost is $2/in^2, resulting in the minimum cost of prime bulk CZ wafers of this size being $80–$100. The cost of 300-mm wafers is expected to eventually decline to somewhere above $3/in^2, with a single bulk-CZ wafer thus eventually costing $350–$400. In 1998, the cost of prime 300- mm wafers was ~$1000. Note that adding an epitaxial layer to the wafer approximately doubles the wafer cost, and the cost of 200-mm epi wafers in 1998 was $150–$180.

The cost/in^2 increases with wafer size for a number reasons. First, larger wafers are thicker, meaning fewer wafers per cm of ingot length are produced. Second, a smaller percentage of the electronic-grade polysilicon (EGS) ends up in prime wafers. (For 150-mm wafers this percentage was 30%, for 200-mm wafers it dropped to 17%, and for 300 mm wafers it is expected to be only ~10%.[81]) Third, wafer specs are tighter for each generation, reducing the "sweet spot" in the middle of the ingot that yields prime wafers. Finally, epi may be required for DRAM production on 300-mm wafers, which will create a steep rise in average price of prime wafers.

Note that the consumption of wafers of à given size also varies with time (see Fig. 2-33), and each new wafer size remains in production for about 24 years.[82] For example, production of 150-mm wafers began in the late1970s, and their consumption rate peaked in 1997. Their use in production is expected to be phased out by about 2010. Next, 200-mm wafers were first introduced in 1988, and they are expected to reach their peak consumption rate sometime between 2005 and 2010 (depending on the rate of ramp up of the new 300-mm wafer generation).[72] By 1998, however, full-scale-production IC factories using 300-mm wafers were not yet running. As a result, well-designed 200-mm equipment is predicted to have a long working life before it is made obsolete by future wafer-fabs running larger wafer sizes.

The worldwide consumption of single-crystal silicon has been growing at 15–20% per year. In 1992, about 1.9 billion in^2 of silicon were sold. By 1994 this number was 2.7 billion in^2, and by 1999 it had increased to ~4.5 billion in^2. In 1994 this translated to a total production of about 100 million wafers. These sales generated an income of $5.9 billion US in 1999.[83,84] There are a relatively large number of silicon wafer suppliers. In the late 1990's the largest were Shin-Etsu Handotai (SEH: Japanese), MEMC (German); Wacker-Siltronic (German); Sumitomo-Sitix (Japanese); Mitsubishi Materials Silicon (Japanese); and Komatsu (Japanese).

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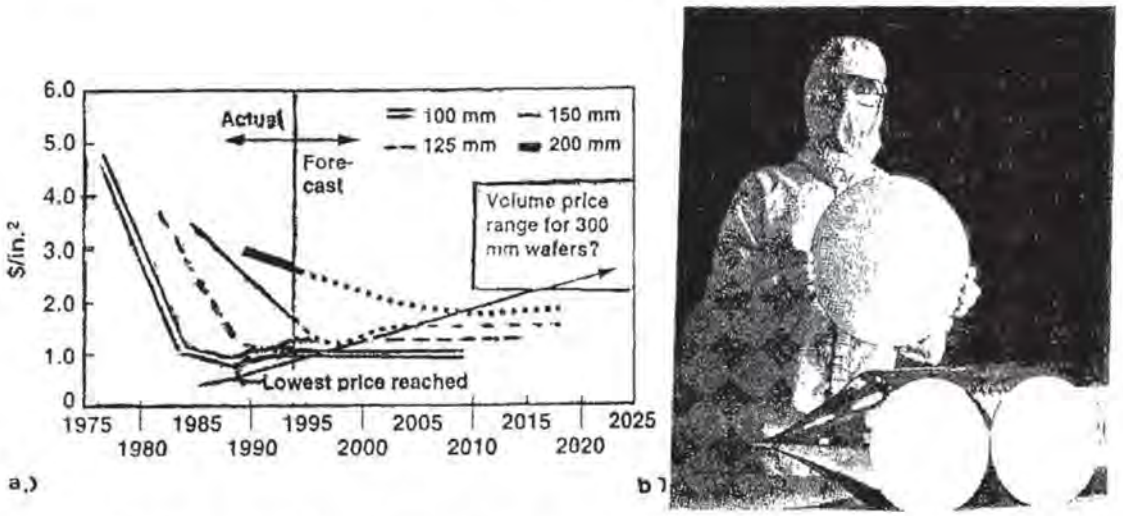


Fig. 2-32 a) Actual wafer pricing cycle by wafer diameter. Reprinted with permission of Semiconductor International.[70] b) Photograph of a 300-mm wafer. Courtesy of MEMC.

The silicon wafer industry historically funded its R&D and capacity expansion for the next generation, large-diameter wafer through the profits and cash flow from the previous-generation wafers. However, in the 2000-year timeframe the industry was being asked to fund the 200-mm and the 300-mm generation at the same time. According to the Rose Associates this is unprecedented, especially in an industry that lost nearly $1 billion in 1998 on sales.[85] These losses resulted from the semiconductor industry downturn, the Asian financial crisis, and excess silicon wafer capacity that combined to cause the average selling price of silicon wafers to fall by 36% over the three year period ending in mid-1999. This caused the industry to focus on cost reduction for survival. While losses in 1999 narrowed, and profitability returned in 2000, the profit outlook was still uncertain. Unless the profitability continues to improve, the funding for 300-mm development will compete with the economics of 200-mm growth and capability requirements.

One possible scenario will be that there will be a shortage of wafers in the 2000 timeframe, especially 300-mm wafers. One vehicle for alleviating this shortage is to use reclaimed wafers, especially for the role of test wafers used in process development applications. That is, during the development and marathon testing of wafer-manufacturing tools, reclaim wafers provide an excellent opportunity to re-use materials. While the maturation of 200-mm processes has greatly reduced the need for test wafers, their use will increase as the 300-mm processes enter the mainstream manufacturing arena. The price of 300-mm

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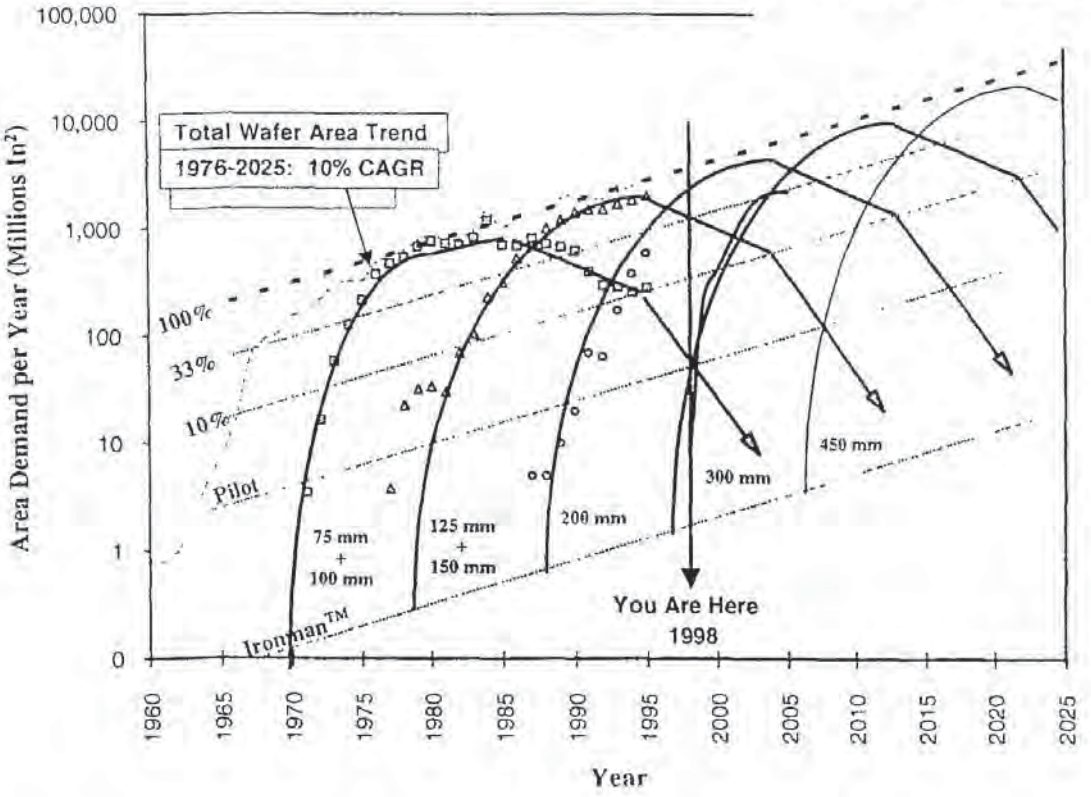


Fig. 2-33 The 24-year single-diameter cycle of silicon wafers.[82]

TABLE 2-4 Selected near-term general characteristics and polished wafer requirements for silicon*

□ = Solutions exist = Solutions being pursued ■ = No known solutions

Year	1999	2000	2001	2002	2003	2004	2005
Technology node (nm)	180			130			100
Wafer diameter (mm)*	200	300**	300	300	300	300	300
			Defined limit values				
Edge exclusion (mm)	2	1	1	1	1	1	1
Front surface particle and COP size (nm)	≥90	≥82 5	75	65	60	55	50
Particles and COPs (cm⁻²)***	≤0.13	≤0.12	0.12	0.14	0.13	0.12	0.10
Particles and COPs (#/wf) ***	≤38	≤84	80	95	89	84	72
Critical surface metals (at/cm²)	≤1.8x10¹⁰	≤1.4x10¹⁰	≤1 2x10¹⁰	≤8 8x10⁹	≤6 8x10⁹	≤5.8x10⁹	≤4 9x10⁹
Site flatness (mm)	≤180	≤165	≤150	≤130	≤120	110	100
Oxygen (center point value ±2.0 ppma)	19–31	18–31	18–31	18–31	18–31	18–31	18–31
Total bulk Fe (at/cm³)	≤1x10¹⁰	<1x10¹⁰	<1x10¹⁰	<1x10¹⁰	<1x10¹⁰	<1x10¹⁰	<1x10¹⁰
OSFs DRAM (cm⁻²)	≤4.4	≤3 9	≤3.4	≤2 8	≤2 5	≤2 2	≤1 9
OSFs MPU (cm⁻²)	≤3 1	≤2 5	≤1.9	≤1 5	≤1 4	≤1 1	≤1 0
Recombination lifetime (μm)	≤305	≤350	≤350	≤350	≤350	≤350	≤350

* Significant gaps in metrology and wafer manufacturing equipment need to be closed on 200mm, especially for the 180nm and 130nm nodes

** Values are for 300mm, although 200mm will be the dominant wafer diameter

*** The total allowable, front-surface, light-scattering defect density is the sum of crystal originated pits (COPs) and particles

* The complete Table 34A in the 1999 *International Technology Roadmap for Semiconductors* includes other parameters and requirements for epitaxial and SOI wafers

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reclaim wafers is about 60% of the price of virgin wafers. Reclaim wafers in 2000 represented about 10% of the 300-mm market.[86]

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Chapter 3

GATE DIELECTRICS: THIN SILICON DIOXIDE FILMS

Thermally grown films of silicon dioxide (SiO_2) play many key roles in the operation and fabrication of silicon integrated circuits. However, the most critical application of such films in deep-submicron CMOS USLI circuits is serving as the MOSFET gate dielectric material. Although the many other roles of SiO_2 are also important (including diffusion masking, surface passivation, and functioning as a field oxide, interlevel dielectric, screen oxide, pad oxide, trench liner in STI, tunneling oxide in non-volatile memory devices, and sidewall spacer), the discussion here will focus on its role as the *gate dielectric of MOSFETs*.

It is commonly believed that crystalline-silicon is the main material responsible for the growth and success of the semiconductor industry. But others maintain that the real magic in silicon technology lies with silicon dioxide and its amazing ability to satisfy the myriad demands placed upon it as the gate dielectric of the MOSFET.

In this chapter we will explore the role of thin gate oxide films in deep-submicron MOSFETs, and address the following issues that relate to this subject:

1. The structure and role of silicon dioxide (and the Si/SiO_2 interface) as the gate dielectric of the MOSFET.
2. Dielectric breakdown and defects in SiO_2;
3. Leakage currents in silicon dioxide films;
4. Models and processes of the growth of ultra-thin oxide films;
5. Strengthening silicon dioxide films through the addition of nitrogen (oxynitrides), and the related problem boron penetration through gate oxides;
6. Technology of growing ultra-thin oxides on large diameter wafers (200-mm and 300-mm);
7. Limits of silicon dioxide as a gate dielectric material.

Despite the fact that we will restrict our discussion to SiO_2-films as gate dielectrics, it is informative to list the other IC applications in which oxide films are employed, and the oxide thickness used in such roles (see Table 3-1).

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Table 3-1 RANGES OF THERMAL OXIDE THICKNESS USED IN ULSI PROCESSING

Application	SiO_2 Thickness (nm)
Gate oxide insulators for MOS devices	1.5–10.0
Tunnel oxides in EEPROMs and flash memories	6.0–10.0
Screen oxides for ion implantation	10.0–20.0
Side-wall liners for shallow trench isolation (STI)	15.0–40.0
Field oxide for LOCOS isolation	200–400
Re-oxidation of the etched gate stack side-wall damage	5.0-7.5
Inter-polysilicon dielectric	4.0–20.0
Masking film against ion implantation and diffusion	100–200
Sacrificial oxides for gate applications	6.0–15.0
Capacitor dielectric in DRAM circuits	5.0–10.0

3.1 REQUIRED CHARACTERISTICS OF GATE DIELECTRICS FOR DEEP-SUBMICRON MOSFETS

A dielectric material must satisfy a large number of important demands in order to successfully function as the gate dielectric of a MOSFET. Silicon dioxide has been used as the gate dielectric material in silicon-based MOS ICs ever since they were first introduced in the early 1970's. It continues to serve in this role, even as MOSFETs have been scaled down to the deep-submicron regime. We list the requirements of dielectric material for this application here, and provide more details about them in later sections of the chapter.

1. The most important requirement that the gate dielectric of a deep-submicron MOSFET must meet is the following: *It must be possible to continue to decrease the thickness of the oxide to the degree specified in accordance with the scaling of the gate length L_E of a MOSFET.* We should elaborate upon why being able to scale the gate oxide thickness is so fundamentally important for deep-submicron MOSFETs. Figure 3-1 shows that the ratio of the gate length to the oxide thickness (L_E/t_{ox}) has indeed remained constant at about a value of 45 for process technology at Intel for over 25 years.[1] The gate-oxide requirements for technology nodes for 0.18-μm and beyond (according to the ITRS Roadmap) are given in Table 3-2. At some point, *if SiO_2 cannot be scaled further to meet future demands, another material with higher reliability will be needed.*

As CMOS IC technology advances, the central focus of scaling the MOSFET device structure involves scaling the gate length L_E. That is, gate lengths of MOSFETs are scaled to obtain the significant benefits offered by such scaling. These benefits include: i) an increase in the drain current of the MOSFET I_D (which usually provides an improvement in the circuit

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Table 3-2 Gate Oxide Equivalent Thickness for Deep-Submicron CMOS

	1999 (180 nm)	2001 (150 nm)	2003 (130 nm)	2006 (100 nm)	2009 (70 nm)	2012 (50 nm)
Equivalent Oxide thickness (nm)	3–4	2–3	2–3	1.5–2	<1.5	<1.0

speed); ii) a decrease in the gate area of the minimum-size MOSFET (which results in a reduction of the input capacitance that must be charged when logic levels are switched - and thus also improves the circuit speed); and iii) an increase in the density of devices that can be fabricated on a chip. (See Vol. 3 for more details on these issues.)

In deep-submicron MOSFETs, however, such reduction of the gate length increases the subthreshold drain current I_{Dst} of a MOSFET (which is one component of the total off-state leakage current of CMOS ICs). That is, in deep-submicron MOSFETs the short-channel effect known as *drain-induced barrier lowering* (DIBL) causes the subthreshold (off-state) drain current to rise significantly as the gate length is reduced (see Vol. 3 for more details). Two measures must be employed to prevent (or at least mitigate) this rise in the subthreshold leakage current as the gate length is

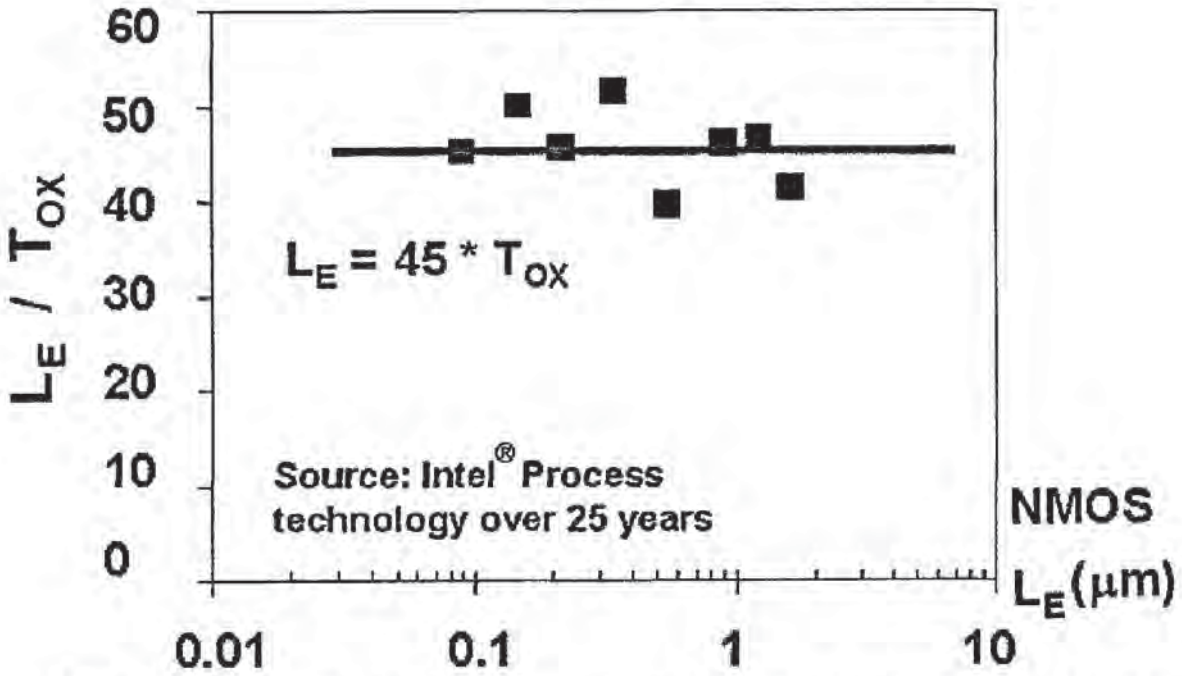


Fig. 3-1 Channel-length divided by gate-oxide thickness (L_E/t_{ox}) versus channel-length L_E for Intel's process technologies for the past 20 years.[1]

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reduced. First, the junction depth X_j of the source/drain-extension-regions must be made shallower. Second, the depth of the MOSFET channel-depletion-region must also be made shallower. Both measures serve to keep the electric field of the drain from penetrating along the channel toward the source (which would worsen the DIBL effect).

The second measure (making the channel-depletion-region shallower as the gate length is shortened) is achieved by increasing the doping concentration in the channel (typically with a heavier-dose threshold-adjust-implant). While it is relatively easy to implement such an increase in the channel doping, doing so causes another undesirable effect. That is, if the gate-oxide-thickness of the MOSFET remains unchanged, the threshold-voltage V_T is increased as the doping concentration near the surface of the channel (boron) is increased (e.g., for an NMOSFET with a *p*-doped channel region). Since the threshold voltage is generally kept unchanged (or it may even be slightly *decreased*) as the CMOS technology is scaled, the increase in V_T due to the increased channel doping must be counteracted. This can only be done by reducing the gate-oxide-thickness (see Fig. 3-2). For example, as shown in Fig. 3-2, if the doping concentration of an NMOSFET with a 250-Å gate-oxide is increased from $6x10^{16}/cm^3$ to $1x10^{17}/cm^3$, V_T will increase from 0.6-V to about 1.4-V – which is far higher than the required V_T value of ~0.6 V.

In summary, this shows that in order to continue to scale the gate-length of MOSFETs, it will be necessary to decrease the oxide thickness by about the same scaling factor applied to the gate-length! However, such scaling of the oxide thickness brings with it both benefits and problems. One additional benefit is that the on-state drain current is further increased as the oxide thickness is scaled down (see Vol. 3). However, several other negative factors also ensue: the thinner oxide films cannot tolerate the increased gate electric fields, and this forces smaller power-supply voltages to be used (and such smaller supply voltages reduce the MOSFET on-state drain current); the tunneling leakage-current (gate current) through the oxide increases; the oxide is more prone to penetration by poly dopant (especially boron); and defects and oxide-layer thickness non-uniformities become bigger problems when thinner oxides must be manufactured. Figure 3-3 depicts these concerns for ultrathin gate oxides.

2. It must be possible to form the oxide layer with a thickness that closely matches the design specification of the MOSFET. This oxide thickness

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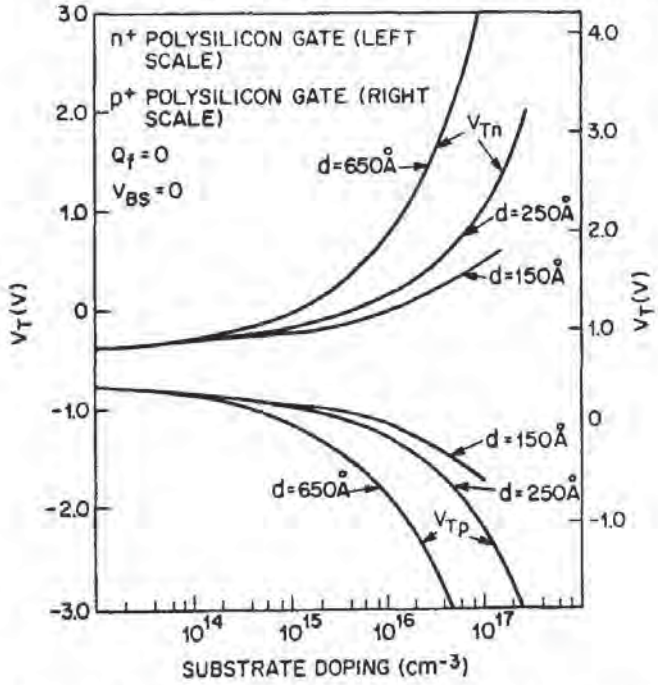


Fig. 3-2 Calculated threshold voltages of *n*-channel (V_{Tn}) and *p*-channel (V_{Tp}) transistors as a function of their substrate's doping, assuming n^+ polysilicon gate (left scale) and p^+ polysilicon gate (right scale). Curves for gate oxide thicknesses *d* of 150Å, 250Å, and 650Å are shown. From S.M. Sze Ed. *VLSI Technology,* 2nd Ed., Chap. 11, "VLSI Process Integration." Copyright, 1988 Bell Telephone Labs. Reprinted with permission.

must also be sufficiently uniform across the entire wafer, and from wafer-to-wafer, and from run-to-run.

3. The oxide film and the Si/SiO_2 interface must maintain stable electrical characteristics. This includes exhibiting adequately small values of charge in the oxide and at the $Si\text{-}SiO_2$ interface (i.e., low Q_f, D_{it}, Q_{ot} and Q_m values).

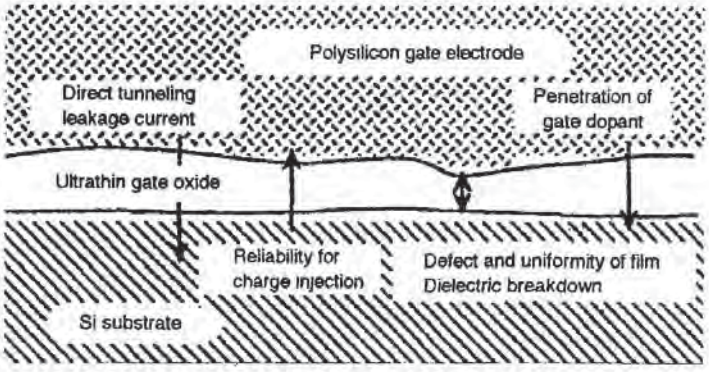


Fig. 3-3 Concerns in ultra-thin gate oxides.

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4. The dielectric breakdown strength of the oxide must be sufficiently high (e.g., > 8-MV/cm), implying that the film is pinhole free and contains a negligible number of defects that would lead to oxide breakdown at lower electric fields.

5. The oxide film must exhibit sufficiently long lifetime under normal operating conditions (i.e., t_{BD} is adequate). This characteristic is related to **4**.

6. The dielectric material (oxide) must be compatible with the other materials of the MOSFET structure, and be thermally, electrically, and chemically stable under the processes used to fabricate the ICs.

7. The leakage-current through the gate-oxide must be sufficiently small to meet the off-current leakage requirement of the IC in which it is used.

8. The oxide should exhibit high resistance to hot-carrier damage (i.e., device degradation should be low in the face of hot-carrier stressing).

9. If the oxide is to be used in a symmetric CMOS technology (i.e., in which both p^+ and n^+ poly are used), the oxide film needs to be resistant to the penetration of boron at the process temperatures used after gate doping.

10. The oxide must passivate the silicon surface.

3.2 THE STRUCTURE OF THERMALLY GROWN SiO_2 AND THE PROPERTIES OF THE Si/SiO_2 INTERFACE

3.2.1 The Microscopic Structure of Thermally Grown SiO_2

SiO_2 (silica) can be found in crystalline or amorphous (vitreous) forms. When the atomic structure of silica exhibits long-range order it is in *crystalline* form. Many varieties of crystalline-silica exist, including quartz, crystobalite, coesite, etc. However, the type of silica encountered in silicon ICs (i.e., silicon-dioxide films thermally grown under normal conditions) is not crystalline. Instead, it is silica in its *vitreous* (or *glassy*) form. Vitreous solids do not exhibit long-range order. Instead, their structure is ordered only over short ranges. This glassy state of SiO_2 is also often referred to as *fused-silica.* Since we are interested in thermally grown SiO_2, our discussion will focus on the glassy state of SiO_2 (fused-silica).

The basic structural unit of silica is centered around the *structural formula* (SiO_4). The spatial arrangement of Si and O atoms is due to their respective valence (+4 and -2), their relative sizes, and their electrostatic interactions. These factors give rise to elementary SiO_2 cells of tetrahedric configurations. That is, a silicon atom (with a valence of +4) is located at the center of the tetrahedron, with oxygen atoms (O^{2-}) at each of the corners (Fig. 3-4a).[3] In crystalline-SiO_2 (quartz), each oxygen atom belongs to two tetrahedra and is thus bonded to 2

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silicon atoms. Such oxygen atoms are then known as *bridging oxygen atoms*. (Fig. 3-4b).[3] In vitreous- or amorphous-SiO_2 some of the vertices of the tetrahedra have *nonbridging oxygen atoms*, meaning they are not shared between two tetrahedra (Fig. 3-4d). The greater the ratio of bridging-to-non-bridging oxygens, the greater the cohesiveness of the SiO_2 structure.

The interatomic distances (from the center of one atom to the center of its nearest neighbor) have been measured and found to have the following mean values: 1.62-Å for the Si-O bond; 2.27-Å for the O-O distance; and 3.12-Å for the Si-Si distance. Note this implies that a 2.0-nm gate oxide is only 10-12 atomic layers thick!

The structure of fused-silica is a continuous random network of tetrahedra, where the Si-O-Si bond angle varies from 110° to 180°, with the most probable value being 144°. A two-dimensional representation of the vitreous-SiO_2 lattice is shown in Fig. 3-4c.[4]

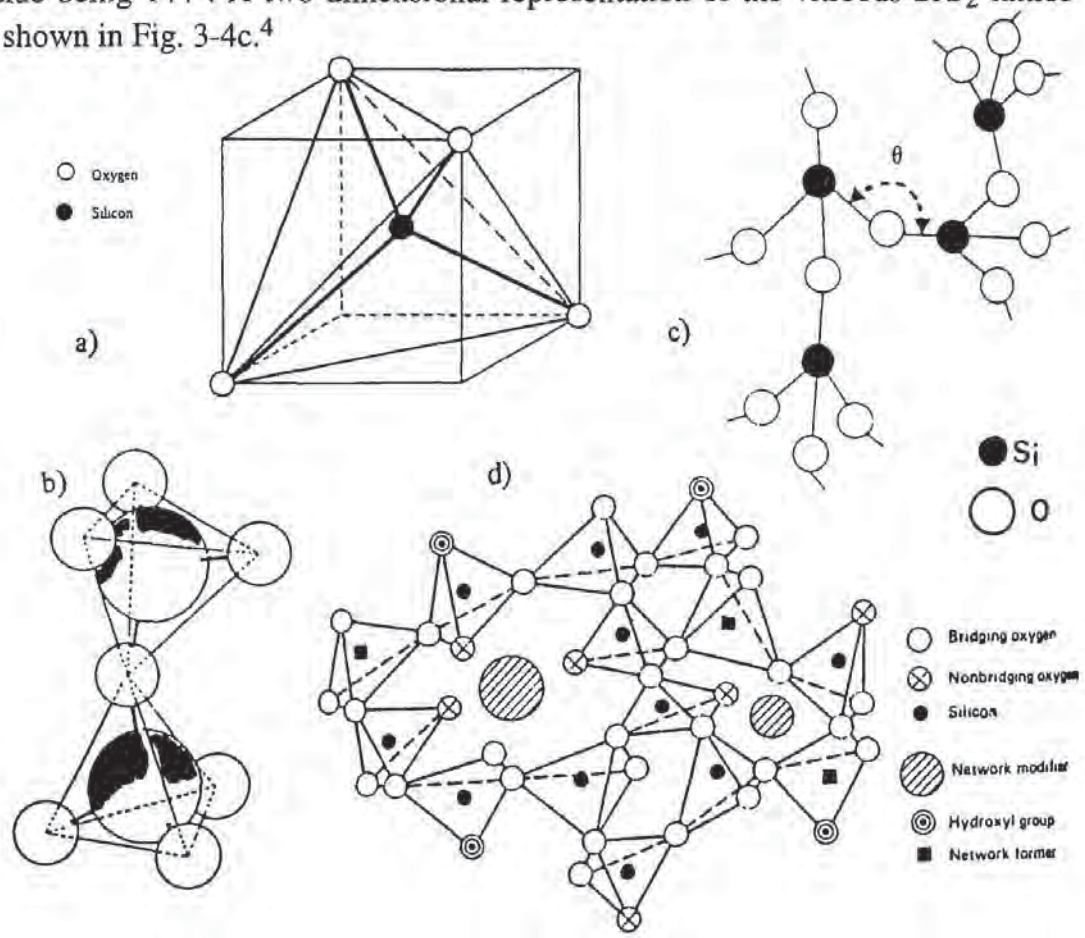


Fig. 3-4 (a) The basic structure of SiO_2.[2] (b) Three-dimensional representation of two neighboring SiO_4 cells, bridged by an oxygen atom. (c) Two-dimensional lattice representing vitreous-SiO_2.[2] (d) The structure of thermally grown SiO_2 showing bridging and non-bridging oxygen atoms and dopant (i.e., network modifier) atoms.[3] (© IEEE 1965)

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The density of thermal-SiO_2 (fused-silica) is 2.20-g/cm^3 which is smaller than that of quartz (2.65-g/cm^3). In fused silica only 43% of the lattice space is occupied, making its structure much more open than that of quartz. Consequently, a large variety of impurity atoms can easily enter this oxide network and diffuse through it. Since it is difficult to directly assess the density of thin films, the refractive index of SiO_2 is usually measured instead, and the density is then inferred from it. A refractive index of 1.460 corresponds to a density of 2.20-g/cm^3. Generally, CVD oxides exhibit smaller densities than thermally grown SiO_2, and worse electrical and material properties correspond to less dense films. Hence, measurements of the index of refraction also provide a method for rapidly comparing the characteristics of deposited oxides.

3.2.2 The Si/SiO_2 Interface

In addition to the characteristics of the SiO_2 bulk structure, the characteristics of the Si/SiO_2 interface also play a critical role when SiO_2 functions as the dielectric layer of a MOSFET. Hence, a discussion of these characteristics (and the structure) of the SiO_2 interface is also relevant. First, it is useful to define the types of charges that exist in the oxide and at the Si/SiO_2 interface. (It should be noted that such charges are not expected to exist in an "ideal" oxide or at an "ideal" interface.) Four different types of charges are associated with the bulk oxide and "real" Si/SiO_2 interfaces, as shown schematically in Fig. 3-5. The *effective net* (i.e., *total*) *charge-per-unit-area* due to such charges at the Si/SiO_2 interface and within the oxide bulk (in C/cm^2) is denoted by the symbol Q_{tot}, whereas the *net* (*total*) *number of charges* per unit area (Q_{tot}/q) is given by N_{tot}. The standardized terminology and symbols used to differentiate these various individual charge types are as follows:

1. Mobile ionic charge per unit area Q_m (C/cm^2), and N_m (no. of mobile charges/cm^2);
2. Fixed oxide charge per unit area Q_f (C/cm^2), and N_f (no. of fixed oxide charges/cm^2);
3. Interface trapped charge per unit area Q_{it} (C/cm^2), and N_{it} (no. of interface trapped charges/cm^2); D_{it} - number of interface trapped charges per unit area *and* energy (no. of interface trapped charges/cm^2-eV);
4. Oxide trapped charge Q_{ot} (C/cm^2), and N_{ot} (no. of oxide trapped charges/cm^2).

The issues relating to the reliability of deep-submicron MOSFETs primarily involve Q_{it} and Q_{ot}. That is, the problems caused by Q_m and Q_f are not only well

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controlled, but their impact does not get any more severe as oxides are scaled. On the other hand, those associated with Q_{it} and Q_{ot} are ongoing, scaling-dependent problems that must be addressed as MOSFETs are pushed further into the deep-submicron regime. Hence, the review provided here will examine only these two categories of interface/oxide bulk charges. This will include the origin of the charges and their effect on device behavior. A more detailed description of the characteristics of Q_m and Q_f can be found in Vols. 1 and 3, and in Refs. 1 and 7.

3.2.2.1 Interface Trapped Charge: The *interface-trapped charges* refer to charges which are localized at sites at the surface of the silicon (i.e., at the Si/SiO_2 interface). Such sites are believed to arise from energy states that exist in the forbidden gap of the silicon, and are referred to as *interface states.* Such surface states are extra allowed energy states (i.e., that electrons can occupy) present at the semi-conductor surface, but not within the bulk.

The term *surface state* was coined by Tamm in 1932.[5] Using quantum mechanical calculations, he showed that new electronic energy states arise in a crystal if the lattice is terminated at a surface. Such new states are confined to the region very close to the surface. He also calculated that these states will arise at interfaces (such as the Si/SiO_2 interface), as well as at free surfaces. Each of the states is associated with a single atom at the surface. Hence, an electron occupying one of these states is localized (i.e., it is forced to remain in a restricted region of space centered on that atom). Since such states thus effectively *trap* free carriers at the surface, they are also referred to as *interface traps.* The charge-per-unit-area stored in these traps is symbolized by Q_{it}.

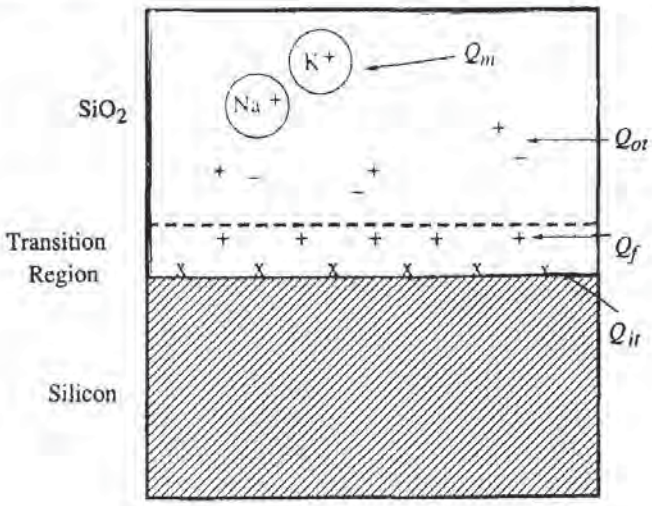


Fig. 3-5 Charges associated with the Si/SiO_2 system.

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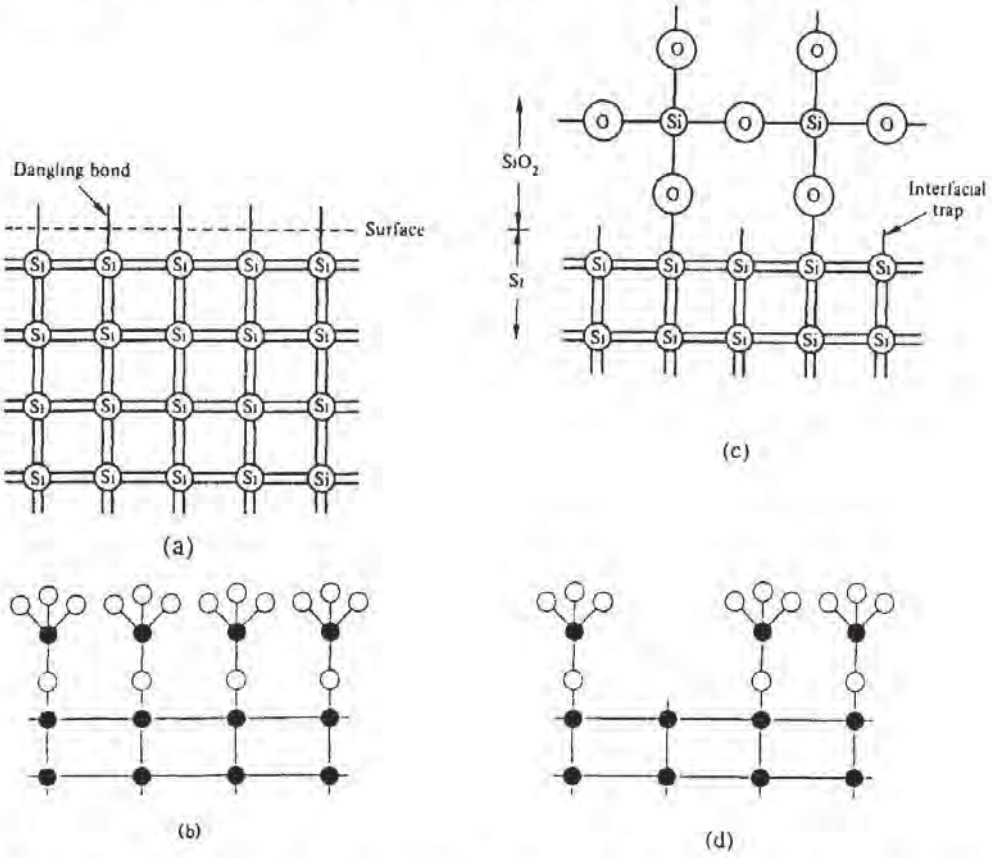


Fig. 3-6 Physical model for the interfacial traps. "Dangling bonds" which occur when the Si lattice is abruptly terminated along a given plane to form a surface. (b) Post-oxidation perfect (ideal) interface. (c & d) Post-oxidation dangling bonds that become interfacial traps.[7] Reprinted with permission of the publisher, the Electrochemical Society.

Although the theoretical basis of interface traps is well accepted and models exist that accurately detail the electrical behavior of the traps, the *physical origin* of these surface states has not been totally determined. The weight of experimental evidence supports the view that surface-states arise primarily from unsatisfied, or *dangling* bonds at the silicon surface (see Fig. 3-6). Note that a Si atom at a surface with a dangling bond can also be viewed as a *trivalent Si atom.*

From a qualitative perspective, the dangling bond model can be visualized with the aid of Fig. 3-6a. Here it is seen that if a Si lattice is abruptly terminated along a given plane to form a surface, one of the four bonds of each Si atom at the surface is left dangling. There will thus be extra states on this surface because the energy field of the crystal is one-sided (i.e., the electrons in the surface region are bonded only from the side directed toward the bulk). It is plausible that thermal formation of SiO_2 can tie up these surface Si bonds, and that along a perfect Si/SiO_2 interface all such bonds could be tied up (Fig. 3-6b). In this case,

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surface-states at the interface would be suppressed.[6] However, it is more plausible that such oxidation will not tie up *all* the bonds (Fig. 3-6c). If even a very small fraction of the number of dangling bonds is left unsatisfied, a significant number of surface-states could exist. For example, on a (100)-Si-surface there are 6.8×10^{14} Si atoms per cm^2. If oxidation left 1/1000 of these bonds dangling, and each of them gave rise to a surface-state, the density of interface trapped charges would be $6.8 \times 10^{11}/cm^2$ (assuming one electronic charge is associated with each energy state). If a gate-oxide-thickness of 20-nm was being used, this would cause a threshold-voltage-shift of 0.63-V. This indicates that if the dangling-bond model correctly describes the origin of interface states, then only a relatively small number of residual-dangling-bonds can significantly perturb MOSFET device characteristics. Crystal-defects near the surface or foreign atoms bonded at the surface are other interface perturbations that have been identified as possible sources of surface-states.

Figure 3-7 represents the bond-stretching and broken-bond model of the Si/SiO_2 bulk of Verwey[2] and of the Si/SiO_2 interface of Sakurai and Sugano.[6] That is, Fig. 3-7a depicts the stretched and broken Si-O bonds in the bulk, and Figs. 3-7b-e at the interface. Figures 3-7f-h illustrate the possible defects in the oxide bulk. In Fig. 3-7b, the dangling-Si-bond at the surface is depicted as an *interfacial-trivalent-Si-atom,* while in Fig. 3-7f, a dangling-Si-bond in the bulk is portrayed as a *trivalent-Si-atom.*

Trivalent-Si-atoms introduce a deep trap-level near the Si midgap when located at the interface, and a deep trap-level in the SiO_2 bandgap when located in the oxide bulk. The weak Si-Si* and Si-O stretched bonds (Figs. 3-7c and 3-7d) at the interface introduce a continuum of deep trap levels, or if such stretched bonds exist in the bulk of the oxide (Fig. 3-7g), they produce shallow trap levels. If a dangling-Si-bond is tied up with an impurity (most commonly H or OH), this is thought to produce an electron-trap, while the oxygen vacancy (or weak Si-Si stretched bond) is considered to be the precursor of a hole-trap.

An anneal in a hydrogen ambient (100% H_2 or 4%-H_2 in N_2 [forming gas]) at approximately 450°C is normally the final step prior to assembly and packaging of an IC. This step is thought to allow hydrogen to penetrate the gate-oxide and then tie up the remaining dangling bonds at the Si/SiO_2 interface not tied up by thermal oxidation (as suggested in Fig. 3-8). However, the Si-H or Si-OH bond can be easily broken by injected hot-electrons, giving rise to interface traps. Thus, hydrogen introduced in the post-metal anneal or other process steps (i.e., during the steam reflow of an interlevel BPSG layer, or during the deposition of silicon nitride), can increase hot-electron degradation in a MOSFET.

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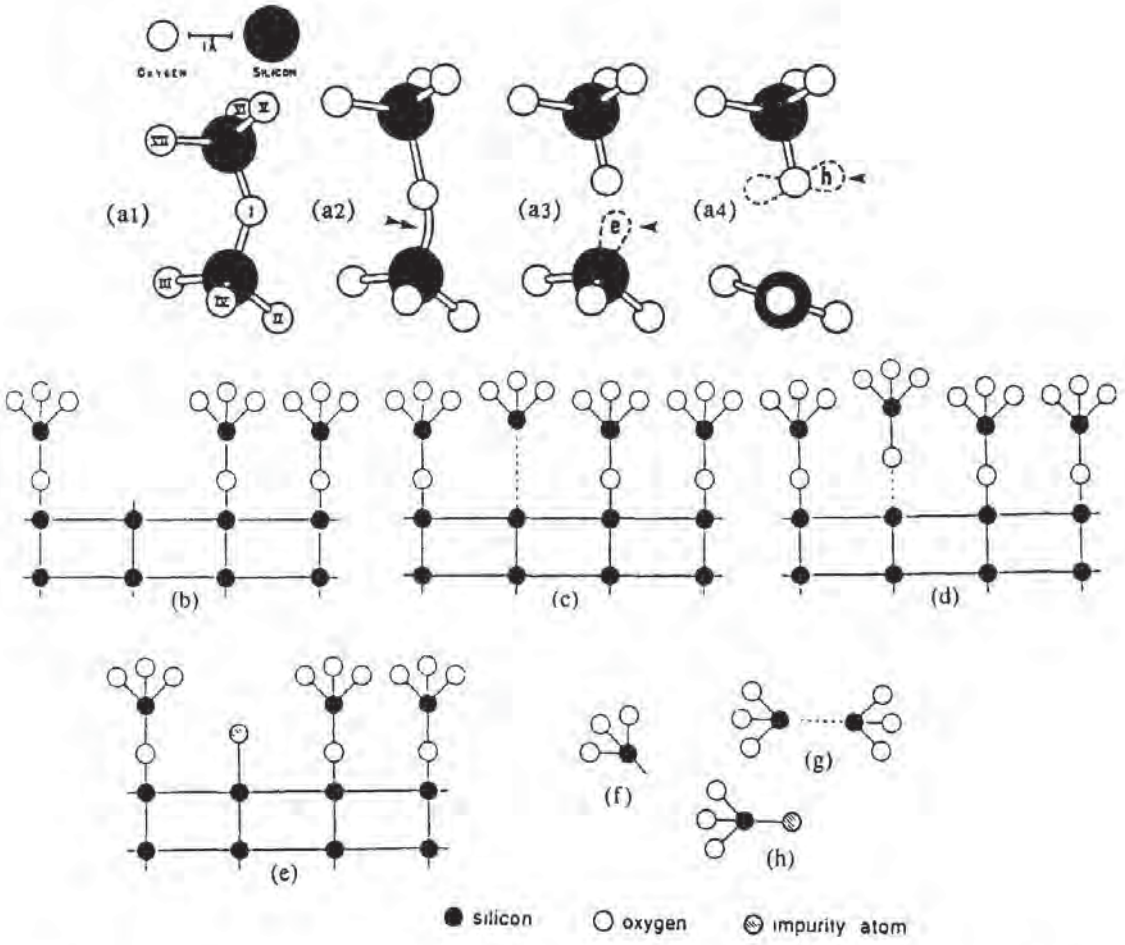


Fig. 3-7 (a) Strained and broken bonds: (a1) Normal Si-O bonds; (a2) Strained bond in vitreous silica; (a3) Broken bond represented with a trapped electron; (a4) Broken bond represented with a trapped hole. Possible interface defects (b-e): (b) Si dangling bonds. (c) Si-Si stretched bond (or oxygen vacancy). (d) Si-O stretched bond. (e) Impurity at interface. Possible oxide bulk defects (f-h): (f) Si dangling bond; (g) Si-Si stretched bond (or oxygen vacancy). (h) impurity in SiO_2.[6] (© IEEE 1988)

Consequently, it has been suggested that the ideal gate dielectric and all subsequent dielectric layers should contain as little hydrogen as possible to make them hot-electron resistant.

3.2.2.2 Effect of Interface Traps on IC Characteristics: The presence of interface traps has four major effects on the characteristics of ICs. First, the charge that is present in the interface traps interacts with the charge in the silicon near the surface and thus changes the silicon charge distribution and the surface potential. Second, interface traps act as generation-recombination centers, giving rise to leakage currents, as described below. Third, since the density of interface trap

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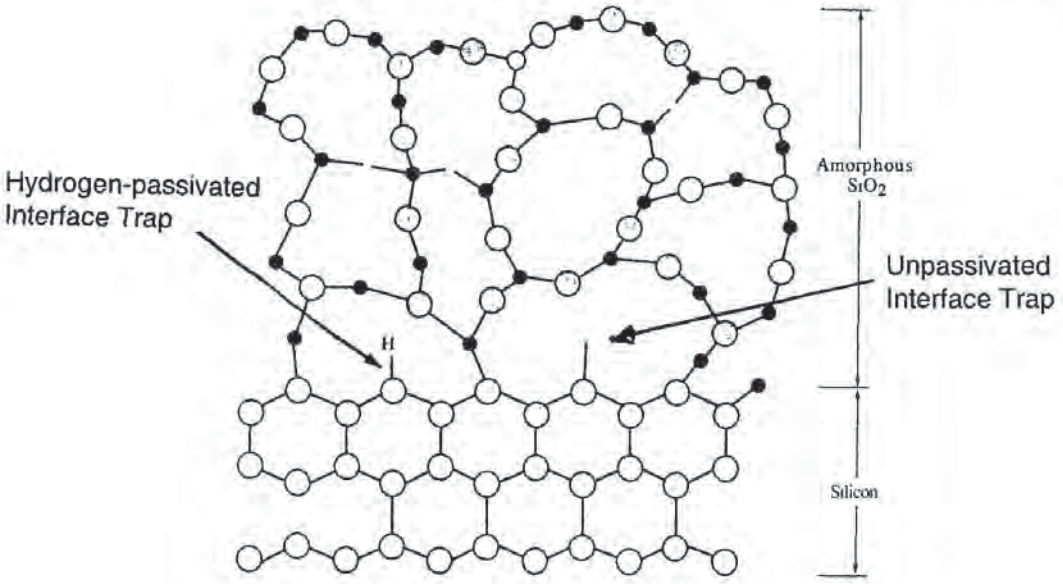


Fig. 3-8 How hydrogen can passivate the dangling bonds at the silicon surface shown in Fig. 3-7c and reduce the interface trap density.

charge changes with the surface potential, it gives rise to an additional capacitance component in parallel with the silicon gate capacitance. Fourth, an increase in interface-state-density has been correlated to weakening of the oxide, which appears to be a prelude to the second-stage breakdown event in gate oxides.

The issue concerning the *effect on the surface-potential of charge being trapped at the interface* is considered first. That is, such charge trapped at the interface has the same effect on the surface-potential as placing a sheet of charge Q_{ox} at the oxide-silicon interface. Such a sheet of charge will impact the threshold voltage, causing it to shift by an amount given by $\Delta V_T = -Q_{ox}/C_{ox}$. To keep this threshold voltage shift as small as possible, the value of Q_{ox} should also be kept as small as possible. The last paragraph of this section explains the measures taken to achieve this goal.

A secondary effect of interface-trap-charge on the surface-potential was introduced earlier. That is, injection of hot electrons into the gate-oxide is thought to produce interface traps (by breaking the bond between a silicon-surface atom and a hydrogen atom, which leaves a dangling bond on the Si atom). Since this process produces additional dangling bonds (and thus interface traps) as time goes by - and since these interface traps can trap electrons - this phenomenon will also cause the value of Q_{ox} to increase with time. In turn, this will cause the value of V_T to change with time. If V_T increases as result of the

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buildup of Q_{ox}, the drain current of the MOSFET will decrease. If such drain current degradation becomes too severe the device will eventually fail to operate properly. Thus, measures to avoid hot-carrier-injection have been employed in MOSFETs as their gate lengths approached 1.0-μm and smaller.

The second effect of interface states involves the fact that they can serve as generation-recombination centers. Since they are present at the silicon surface, they will exist in the depletion regions of *pn* junctions that intersect the surface of the silicon. There are many such junctions at the Si/SiO_2 interface in every device, and therefore in every IC.

Before the invention of integrated circuits, only discrete diodes, bipolar transistors, and field-effect transistors (FETs) could be fabricated. In the early 1950s, these discrete devices exhibited relatively high reverse-bias junction-leakage and low breakdown-voltage (caused by the large density of interface traps at the surface of single-crystal silicon).

In 1958, a group of workers at Bell Telephone Laboratories, led by Atalla, found that when a thin layer of SiO_2 was grown on the surface of silicon where a *pn*-junction intercepts the surface, the leakage current of the junction was reduced by a factor from 10 to 100. It was later understood that the oxide reduces the number (or stabilizes many) of the interface traps. Not only did such oxide-passivation of the silicon surfaces allow diodes and transistors to be fabricated with significantly improved device characteristics, but the leakage path along the surface of the silicon was also effectively shut off. Thus, one of the fundamental isolation capabilities needed for planar devices and integrated circuits had also been developed. In his report on the evolution of the MOS transistor, C.T. Sah remarks that the successful effort by the Bell Labs group to stabilize Si surfaces was the most important technological advance in microelectronics during the 1950s, and that it blazed the trail that led to the development of the silicon integrated circuit.[8]

The third effect of interface traps involves the interface-trap capacitance. As noted earlier, the *interface-trap capacitance* C_{it} is in parallel with the gate capacitance. However, only those interface traps that can be filled and emptied at a rate faster than the capacitance measurement signal can contribute to C_{it}. Traps too slow to follow the capacitance-measurement signal will not contribute to C_{it}. Therefore, the observed C_{it} is not only a function of the interface-trap density but also depends on the MOS-capacitor gate voltage (which controls the surface potential and hence the probability of occupancy of the traps) and the frequency at which the capacitance measurement is made.

All of these observations point to the conclusion that for a MOSFET to have

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predictable and reproducible capacitance characteristics, it is important to employ fabrication processes that minimize trap density. Using (100)-oriented silicon wafers, and a post-metallization hydrogen-annealing step (at temperatures around 400°C) at the end of the fabrication process, are the main techniques for keeping the interface-trap-density at a minimum.

It has been observed that the passage of tunneling current through a thin oxide also introduces interface traps at the Si/SiO_2 interface. Furthermore, while breakdown may not occur until about 10 C/cm^2 of charge has passed through the oxide, interface traps are detectable even after 0.001 C/cm^2 of charge passage. Thus, measuring interface traps has been proposed as a more sensitive means of quantitatively measuring oxide damage (due to Fowler-Nordheim stressing of oxides) prior to breakdown.

3.2.2.3 Oxide Trapped Charge: The oxide trapped charge Q_{ot} is due to holes or electrons trapped in the *bulk* of the oxide, and hence can be positive or negative. They become trapped at *trap centers* that are microscopic defects in the oxide structure *in the bulk of the oxide layer.* Such defects may be caused by ionizing radiation, hot-carrier injection, or high currents through the oxide (e.g., due to Fowler-Nordheim tunneling), or other reactions which either bend or break Si-O bonds in the oxide. Figures 3-7f-h show possible defects in the SiO_2 bulk that may give rise to such traps. For example, a trivalent Si atom in the SiO_2 will introduce a deep trap level in the SiO_2 bandgap ($.Si{\equiv}O_3$), and stretched Si-O or Si-Si bonds [in the latter, a missing bridging-oxygen atom leads to a defect ($O_3{\equiv}Si..S{\equiv}O_3$)]. Figure 3-9 shows schematics illustrating the potential wells of electron traps in silicon dioxide. While, as-grown SiO_2 films contain few such microscopic oxide defects, electron and hole traps can be easily introduced by bombardment with high-energy photons or particles.[9] (The exception to this

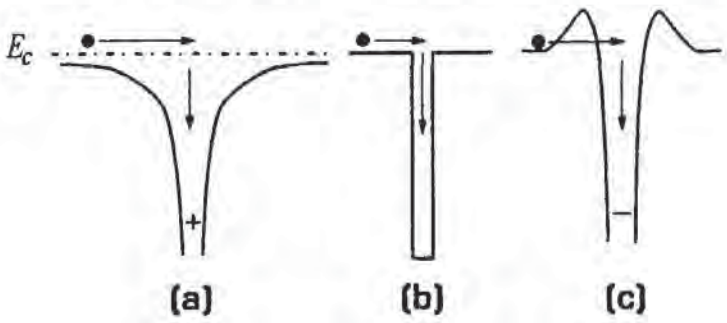


Fig. 3-9 Schematics illustrating the potential wells of electron traps in silicon dioxide: a) Coulomb-attractive trap; b) neutral trap; and c) Coulomb-repulsive trap.

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statement is that as-grown wet oxides tend to contain some oxide traps because they also contain OH^- and H_2O species. The density of oxide traps in wet oxides can be significantly reduced with an appropriate post-oxidation-anneal.)

Q_{ot} can be annealed out by low-temperature treatments (above 550°C) although some neutral traps may remain. Therefore, oxide trapped charge was been considered relatively less important than the other oxide charges in just-completed MOSFETs. In early generations of MOSFET ICs, exposure of the devices to ionizing radiation encountered in space flights was the main concern involving Q_{ot}. However, in deep-submicron CMOS ICs, the problems involving Q_{ot} are becoming serious for several reasons. First, processing techniques such as ion implantation, sputter deposition, and plasma etching are potential sources for creating charged and neutral traps in the gate dielectric (all of which may not be completely annealed out at the end of the fabrication process). This may result in long-term reliability problems, especially if hot carriers are injected in these oxides and get trapped. Another reliability concern involves gate-oxide degradation due to high electric-fields in the oxide (and subsequent Fowler-Nordheim tunneling currents in the oxide). This has become more of a concern as oxide thickness has been scaled down.

3.2.2.4 Effect of Oxide Trapped Charge on Device Characteristics: The major effect of oxide trapped charge on MOSFETs is that they are a manifestation of the damage done to the gate oxide during device fabrication or by electrical stressing (either by the application of a high electric-field across the oxide, or by the injection of carriers into or through the oxide). We will discuss this issue in more detail in Sect. 3.3.

3.3 DIELECTRIC BREAKDOWN IN SILICON DIOXIDE FILMS

Dielectric breakdown of the gate-oxide layer is one of the major reliability issues that affects MOSFETs. We provide a review of this phenomenon here, and recommend that interested readers consult Vol. 3, Chap. 7 for more background information on the various breakdown measurements, statistical models, and burn-in tests used to screen out parts with weak oxides. However, significant new information that has been published since 1995 (when Vol. 3 was released) and this new information will be focus of the discussion here.

Figure 3-10 shows the time dependence of the gate current through an oxide under a large and constant voltage stress applied across the oxide layer. One can see that there is a gradual decrease in the current with time until the oxide suffers *dielectric breakdown* (Fig. 3-10). At that point the current rises rapidly (*catastrophic breakdown*).[10] After such breakdown, the oxide is irreparably damaged,

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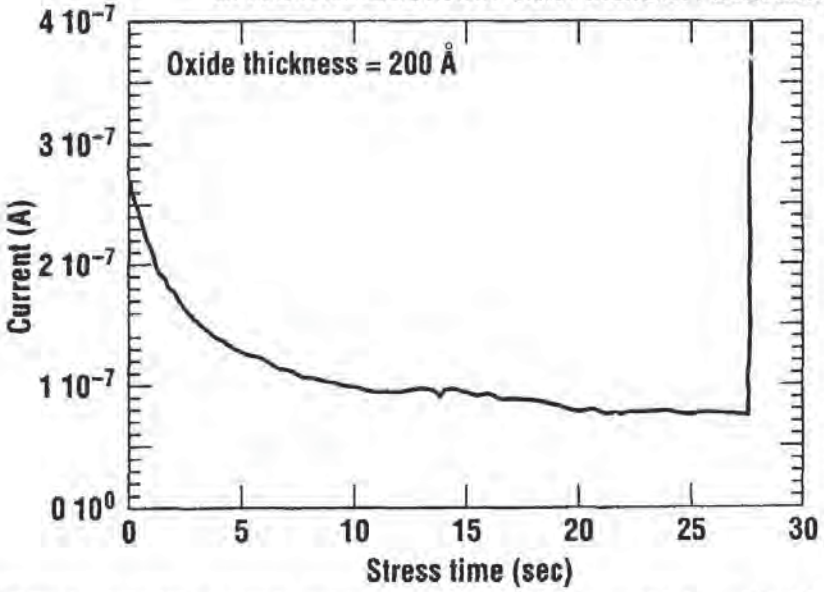


Fig. 3-10 Constant-voltage stress measurements of a 20-nm-thick oxide film. The sharp increase in current near the end of the trace indicates that irreversible breakdown has occurred.

and can no longer function as the dielectric layer in the MOSFET. Since such breakdown occurs after the oxide is subjected to a voltage stress for some extended period of time, this phenomenon is also referred to as *time-dependent dielectric breakdown* (TDDB). Anomalous "soft breakdown" of oxides also occurs for films < 5.0-nm thick, and this will be discussed in Sect. 3.8.

A different metric of the quality of oxide films is expressed in terms of the electric field at which dielectric breakdown occurs. To measure this value, a voltage (that increases linearly with time) is applied between the gate and substrate of a MOS-C test structure until the oxide breaks down. The "best" (apparently defect-free) oxides break down at fields greater than about 10 MV/cm, and failures at such field strengths are referred to as "intrinsic breakdown." Less-than-perfect-oxides (i.e., those that contain some form of defect) may fail at lower voltages (i.e., between 4-6-MV/cm).

In any case, dielectric breakdown in ICs must be avoided. Extensive work has demonstrated that 20-year oxide-lifetimes can be achieved if the oxide field remains below about 8-MV/cm.[11] Thus, for devices used in CMOS logic and memory chips, the maximum electric field during normal device operation is typically restricted to the 5 MV/cm range, and this limit on the electric field is projected to remain at about this value for each technology generation. That is, the 5-MV/cm value is expected to give an acceptable safety margin for 20-30-year oxide-lifetimes. Chips are also normally subjected to burn-in tests to screen out those chips that contain oxides that would fail under the normal operating conditions during their time of service.

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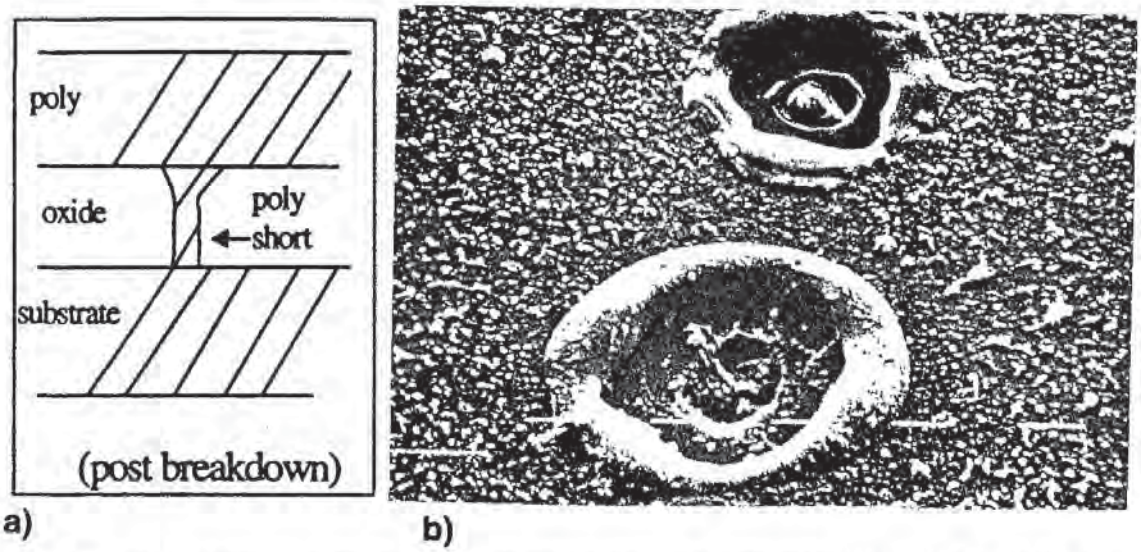


Fig. 3-11 a) Localized poly filament shorting the gate and substrate after gate oxide breakdown; b) A SEM photograph of two breakdown spots. The polysilicon electrode has melted away over 20 μm^2. The polysilicon is spread over a large area in the form of dust and little globules. The size of a dash is 1-μm. From D.R. Wolters and J.F. Verwey, "Breakdown and Wear-Out Phenomena in SiO_2 Films," Chap. 6, p. 329, in *Instabilities in Silicon Devices*, G.M. Barbottin and A. Vapaille Eds., © 1986 Elsevier Science.

Because dielectric breakdown is such a critical reliability issue in CMOS ICs, breakdown of thin oxide films has been (and still is) a subject of intense research. The physical mechanisms involved in the dielectric breakdown process are quite complex. We will discuss some of the latest proposed models to shed light on this phenomenon.

In general, the catastrophic breakdown of a dielectric is believed to be a two-stage process. First, the dielectric is slowly degraded over time (perhaps years) due to being subjected to high-electric fields or due to the passing of current through the oxide. This degradation takes the form of creating defects in the oxide (e.g., electron/hole traps and/or bond-breakage). These defects form a localized conductive path through the oxide during this time. The second stage is the very short runaway breakdown process itself (it may occur in microseconds). During the runaway breakdown phase the oxide is shorted (due to severe joule-heating that causes a conductive filament to form in the dielectric) and a very large current flows between the gate and substrate in the MOS device (Fig. 3-11).

There are numerous forms of damage to the oxide that are postulated to occur during the oxide degradation process, including lattice damage, trap creation by electrons, and trap creation by holes. The two physical mechanisms that are blamed for producing these types of damage are: 1) externally applied electric

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fields; and **2**) current that passes through the oxide. Thus, there are two classes of models that have been developed to predict TDDB: **1**) models that assume the oxide degradation is electric-field-driven (the so-called *E-models*); and **2**) models that assume the oxide degradation is current-driven (the so-called [1/*E*]-models). Here we briefly describe both models. Also note that although the physical basis for oxide degradation is still under debate, definitions and practices have been developed to describe and test the integrity of the oxide.

3.3.1 Electron Trapping in Silicon Dioxide: (and why the Current in the Oxide Decreases with Time During Constant-Voltage Stressing)

As described in Sect. 3.2.2.3, silicon-dioxide layers contain electron and hole traps (either as a result of residual damage inflicted during device processing, or caused by the electric fields applied across the oxide - or gate current that flows - during normal device operation). If these sites trap carriers which are transported in the oxide conduction-band (electrons), they can give rise to oxide-trap charge Q_{ot}. Electrons can enter the conduction band of the oxide in several ways, including: **1**) ionizing radiation can generate electron-hole pairs within the oxide itself; **2**) electrons can enter from the silicon substrate or the gate polysilicon either through tunneling or through hot-electron injection. Some of these electrons may get trapped at oxide trap sites. These trapped electrons will then cause the electric field in the oxide to be modified in the following manner: The field near cathode (i.e., the electrode that acts as an electron source) is decreased, while the electric field near the anode (the electrode that acts as the electron sink) is increased (as depicted in Fig. 3-12). A decrease in the field near the cathode causes Fowler-Nordheim current in the oxide to decrease. Since the gate current is due primarily to Fowler-Nordheim tunneling, this explains why the gate current declines with time under a constant-voltage stress (as shown in Fig 3-10).

3.3.2 The Electric-Field-Driven Model of Oxide Degradation

In the electric-field -driven models of oxide degradation (*E*-models), the cause of low-field (< 10-MV/cm) TDDB is postulated to be field-enhanced thermal bond breakage. That is, at a given temperature, chemical bonds in the SiO_2 structure can be broken by thermal vibrations. Such bond breakage produces local defects that weaken the oxide, and when the concentration of such defects reaches a critical value, breakdown can occur. An externally applied electric field serves to reduce the activation energy required for such thermal-bond breakage, and therefore increases the degradation-reaction rate for failure exponentially. The *time-to-breakdown* t_{BD} which is the inverse of degradation rate, decreases exponentially

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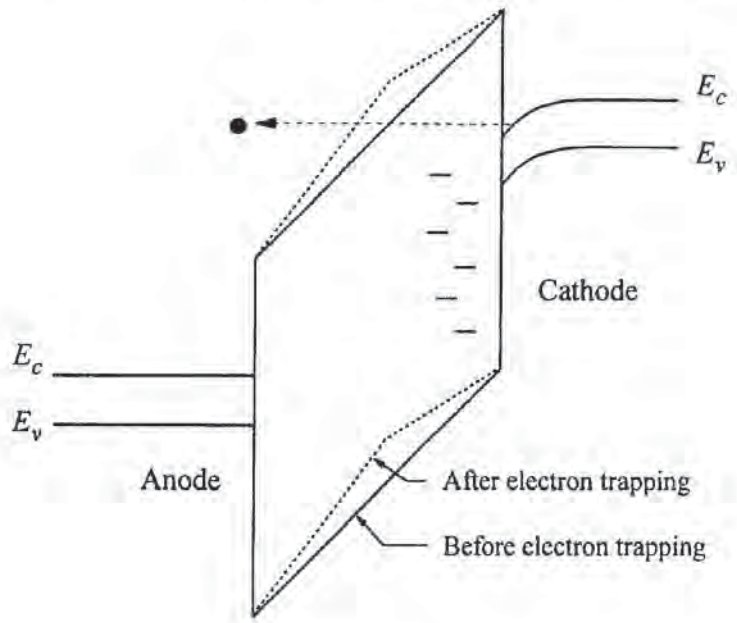


Fig. 3-12 Schematic illustrating the trapping of tunneling electrons. As electrons are trapped, the oxide field near the cathode (electron source) is decreased, while the oxide field near the anode (electron sink) is increased.

with field according to:

$$t_{BD} = A_o \exp(-\gamma E_{ox}) \exp(Q/k_B T) \quad \textbf{(3.1)}$$

where γ is the field acceleration-parameter, E_{ox} is the electric field in the oxide (usually expressed in MV/cm), and Q is the enthalpy of activation for bond breaking in the absence of an external electric field. Generally, for oxide thicknesses greater than 90-Å, γ ~2.5-3.5-cm/MV.

3.3.3 The Current-Driven Model of Oxide Degradation (1/E Model)

In the so-called 1/E model for TDDB, degradation is postulated to be due to current flow through the dielectric caused by Fowler-Nordheim conduction. Electrons, which are F-N injected from the cathode, may cause damage to the dielectric due to impact ionization as the electrons are accelerated through the oxide. Also, when these accelerated electrons reach the anode, hot holes may be produced (see Sect. 3.3.4 below) which can tunnel back into the dielectric causing damage. Since both the electrons from the cathode and the hot holes from the anode are the result of F-N conduction, the time-to-failure is expected to show an exponential dependence on the reciprocal of the electric field, $1/E$:

$$t_{BD} = \tau_0(T) \exp[G(T)/E_{ox}] \quad \textbf{(3.2)}$$

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where $\tau_0(T)$ is a temperature dependent pre-factor, G is the $1/E$-model field acceleration-factor, and k_B is Boltzmann's constant.

The temperature dependence of G has been expressed as a 1/T power series expansion, given by:[12]

$$G = G_0 [1 + (\gamma/k_B)\{(1/T) - (1/300K)\}] \quad \textbf{(3.3)}$$

where:

$$\gamma = (k_B/G_0) [dG/d(1/T)]_{300K} \quad \textbf{(3.4)}$$

and where the derivative is evaluated at $300K$. At room temperature, G_0 ~350-MV/cm and γ ~0.017-eV.

$\tau_0(T)$ is also usually represented as a 1/T expansion:

$$\tau_0(T) = \tau_0 \exp[(-E_a/k_B)\{(1/T) - (1/300K)\}] \quad \textbf{(3.5)}$$

where τ_0 ~$1x10^{-11}$ sec, and E_a ~0.3-eV.

3.3.4 The Hole-Trapping Model that Describes How Holes are Injected and Trapped in SiO_2

The transport of holes through the oxide has been shown to precede breakdown, indicating that holes cause damage to the oxide (namely by creating traps in the bulk oxide).[13] A model (the *anode-hole injection model* [*AHI model*]) has been published that seeks to explain how such holes are generated and injected into the oxide during high electrical field stress.[14] The mechanisms that occur are depicted in Fig. 3-13.

When an electric field is applied across an oxide layer using an MOS-C structure, the energy-band diagram of this situation is depicted in Fig. 3-13. If an electron tunnels from the cathode into the conduction band of an oxide layer (by F-N tunneling), it can then gain kinetic energy from the electric field applied across the oxide, and get accelerated toward the anode. When the electron arrives at the anode it has a large amount of kinetic energy (E_{gain} in Fig. 3-13). Some fraction of such electrons that arrive at the anode are able to transfer this energy to an electron deep within the valence band of the anode silicon near the oxide-anode interface. This valence band electron is excited to the bottom edge of the silicon conduction band in the anode. The excitation event also produces a hole deep within the valence band, and this "hot" hole can tunnel into the valence band of the oxide (again by F-N tunneling, as depicted in Fig. 3-13). These holes can be trapped in the oxide and also create the damage described earlier. This damage accumulates with time, degrading the oxide.[35]

In addition, the trapped holes in the oxide layer cause an increase in the oxide field near the cathode, and a decrease in the field near the anode (Fig. 3-14). A small increase in the oxide field near the cathode can cause a large increase in the

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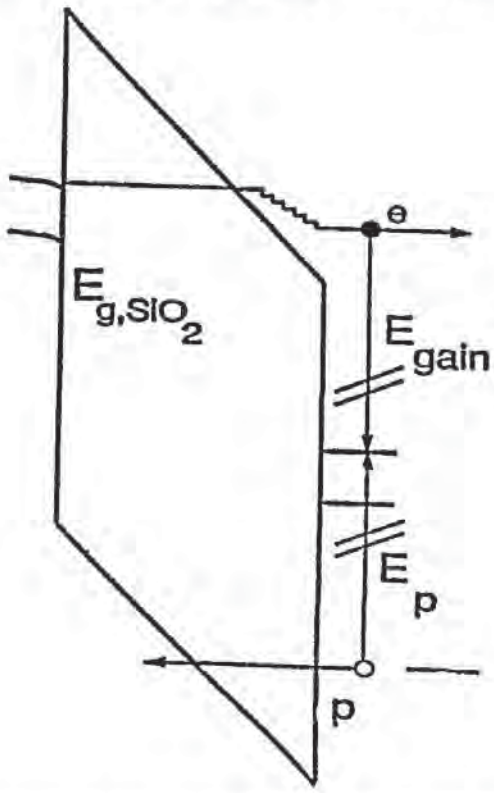


Fig. 3-13 Energy-band diagram of the anode-hole injection (AHI) model, illustrating the generation of an electron-hole pair by a tunneling electron. The hole thus generated can then be injected (by tunneling in this model), into the oxide layer.

tunneling current. Thus, hole trapping in the oxide near the cathode provides positive feedback to the electron tunneling process. It should be pointed out that the increase in tunneling current due to hole trapping is usually not readily observable, except near breakdown, because it is masked by the decrease in tunneling current due to electron trapping.

It should be noted that recent work has called some conclusions of this model into question. That is, until recently it was generally accepted that the substrate current originates from the anode-hole-injection (AHI) mechanism, which was schematically depicted in Fig. 3-13. Part of the holes created by the phenomena postulated by this model tunnel into the oxide, and the oxide degradation is related to the hole fluence (which is found to be constant at breakdown, independent of the stress current or stress voltage). However, the explanation of the substrate current by anode-hole-injection has never been completely verified, and other mechanisms such as minority-carrier generation due to F-N-induced photons have been suggested to be a cause as well. Two recent reports claim that the F-N-induced photons in the gate are the dominant source of the substrate hole

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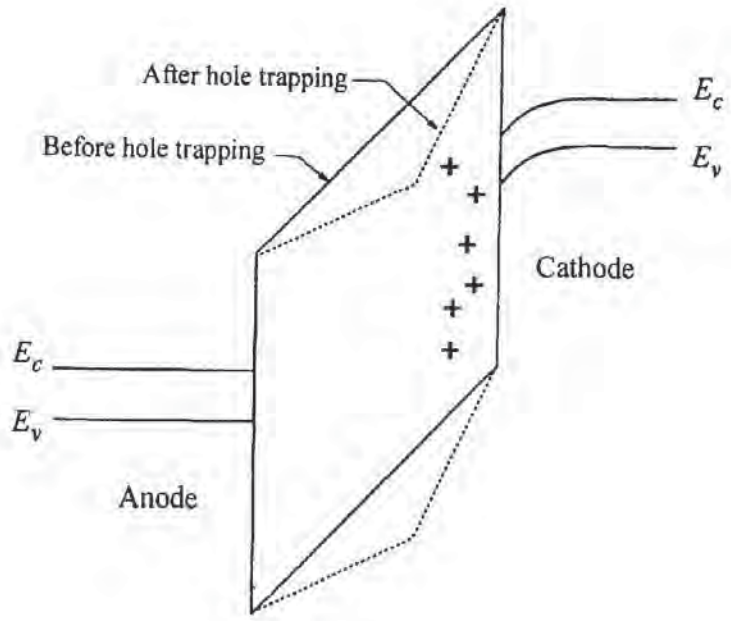


Fig. 3-14 Schematic showing the trapping of holes in the oxide layer. The trapped holes enhance the electric field near the cathode, and decrease the electric field near the anode.

current, and thus the generally accepted explanation of oxide degradation based on anode-hole-injection may have to be revised.[31,32]

3.3.5 Comparing the Electric-Field-Driven and the Current-Driven Oxide Breakdown Models

There has been a great deal of disagreement as to which is the dominant degradation mechanism for low-field TDDB in thin oxide films; i.e., is it field-induced or current-induced? The (1/*E*)-model fits the TDDB data very well at high fields (in which high F-N-currents exist), but falls short at lower fields (< 10-MV/cm). In fact, there have been several low-field/long-term TDDB studies carried out, with each showing that TDDB data were described much better by the *E*-model.[15,16,34] The good fit of the physics-based *E*-model to low-field/long-term TDDB data suggests strongly that it is field (not current), which is the dominant degradation mechanism at low fields because the F-N current is simply so vanishingly small at these lower fields. However, for very-thin oxides (< 40-Å) the direct tunneling-current is very high, which could mean that in these oxides the dominant degradation mechanism may again be current-driven.

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3.3.6 Time-to-Breakdown (t_{BD}) and Charge-to-Breakdown (Q_{BD})

The breakdown characteristics of an oxide film are described in terms of the *time-to-breakdown* (as was discussed earlier) and in terms of its *charge-to-breakdown* Q_{BD} (which measures the *integrated* total tunneling current [i.e., total charge] just before breakdown). Recent publications have tended to use the value of Q_{BD}. It appears that it is simpler to develop models relating to the other physical processes, such as hole current, trapping, trap generation, and interface-state generation, than it is to develop models relating time-to-breakdown to these processes. Thus, Q_{BD} needs to discussed further.

As mentioned above, evidence indicates that tunneling-electron-current can lead to hole-injection into the oxide. Thus, Q_{BD} is the sum of the charges passing through the oxide due to electrons and holes. If a MOS-C structure is used to measure Q_{BD}, then due to the two-terminal nature of the MOS-C, only the total charge can be measured. However, if an NMOSFET is used to measure Q_{BD}, then both the total charge and the hole-charge component can be determined. For the case of an NMOSFET, the bias configuration for such measurements is shown in Fig. 3-15. Integration of the gate current gives the total charge, while integration of the substrate current gives the charge due to the holes. For a given oxide film, Q_{BD} is often plotted as a function of oxide voltage. Figure 3-16 is such a plot for oxide thickness in the 2.5-10-nm range.[15] It shows that for a given oxide thickness, Q_{BD} decreases with increasing oxide voltage.

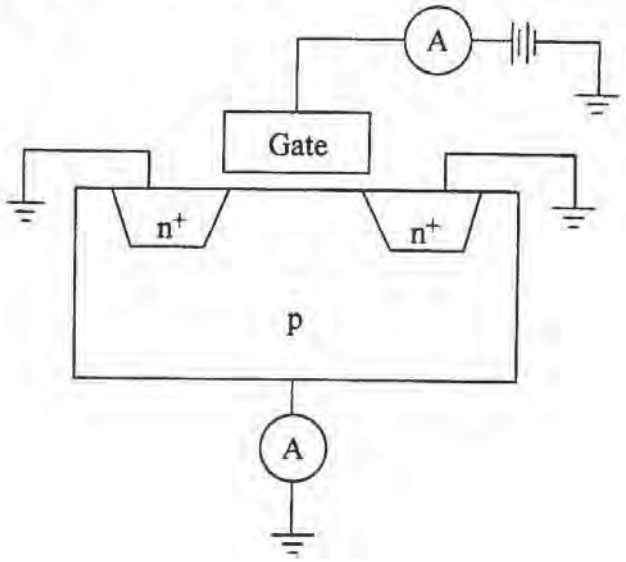


Fig. 3-15 Schematic depicting the bias configuration of an *n*-channel MOSFET for measuring the charge-to-breakdown Q_{BD} and its hole-charge component.

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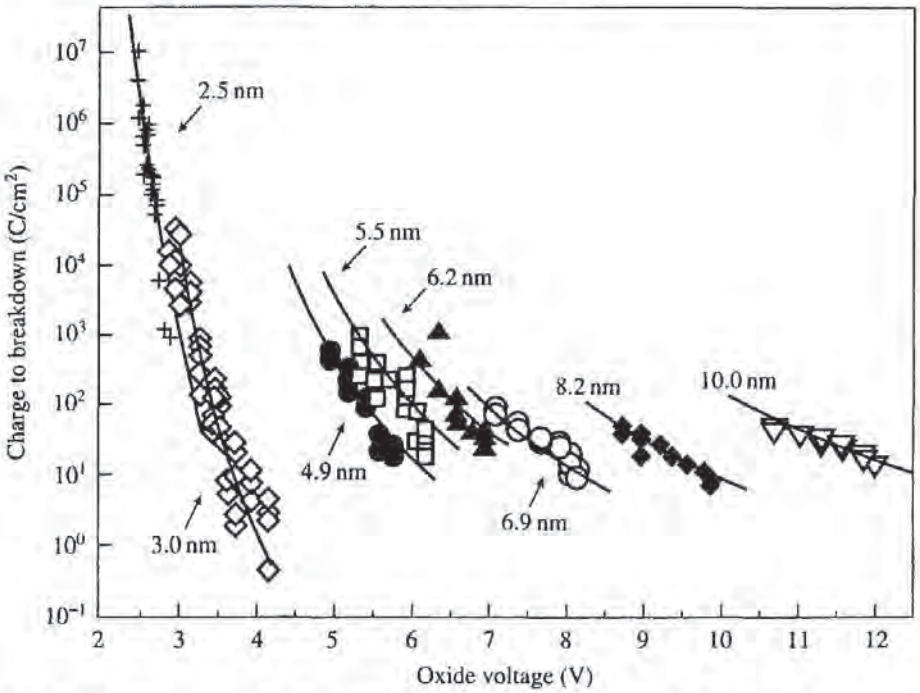


Fig. 3-16 Typical plot of charge to breakdown versus oxide voltage for several oxide thickness values.

3.4 LEAKAGE CURRENTS IN SiO_2 FILMS (TUNNELING PHENOMENA)

When considering the ideal MOS capacitor structure, it is assumed that no current flows through the oxide. However, in real MOS capacitors, a current from the gate to the substrate through the oxide can flow (termed *gate current,* I_g*).* Although the carriers that constitute such current can enter the conduction band (electrons) and valence band (holes) of silicon dioxide by hot-carrier injection, here we only discuss the other way that they can enter, namely by tunneling. This is because few carriers in deep-submicron MOSFETs enter the oxide as a result of hot-carrier injection during normal device operating conditions; hence they do not play a major role in the observed gate current.

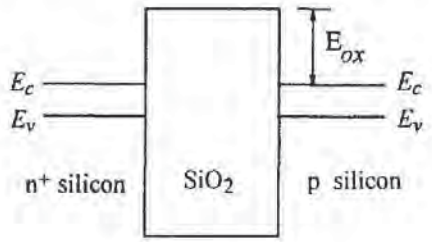


Fig. 3-17 Energy-band diagram of an *n*-type polysilicon-gate MOS structure at flat band.

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The phenomenon of carrier injection into the oxide by tunneling is due to the quantum-mechanical nature of the electron. In the classical sense, the oxide represents an impenetrable barrier to injection of electrons into the conduction-band of the silicon if they possess kinetic energies smaller than the interface energy barrier for the electrons (E_{ox} = 3.1-eV). In Fig. 3-17, the energy-band diagram of a MOS capacitor with silicon dioxide as the insulator and heavily *n*-doped-polysilicon as the gate is shown when biased at the flat-band condition. When a large positive voltage is applied to the gate electrode, electrons in the strongly inverted Si substrate surface can tunnel into or through the oxide layer, and give rise to gate current. (Similarly, if a large negative voltage is applied to the gate electrode, electrons from the n^+-polysilicon can tunnel into or through the oxide-layer and again give rise to gate-current.) Such tunneling occurs because the wave nature of an electron (or hole) allows a finite probability of crossing the barrier, even if the electron does not possess sufficient kinetic energy. This probability increases with larger gate electric fields and/or thinner barriers. Electrons injected by tunneling are generally considered to be in equilibrium with the lattice, and are thus characterized as "cold" (i.e., not "hot").

3.4.1 Fowler-Nordheim (F-N) Tunneling (Tunneling *Into* Silicon Dioxide)

The first type of tunneling is called *Fowler-Nordheim tunneling*. Here electrons are injected by tunneling into the conduction band of the oxide through the triangular energy barrier. Once injected into the oxide conduction-band, electrons are accelerated by the oxide field toward the anode (gate), causing a gate current. Figure 3-18a sketches the energy band diagram for this case assuming a positive bias is applied to the gate.

To determine the probability of an electron exhibiting F-N tunneling through a barrier, Schroedinger's equation is solved for a triangular barrier. The WKB approximation (discussed in most quantum mechanical textbooks) is invoked, and the following expression for the tunneling current-density expression is derived:

$$J = A_F E_{ox}^2 \exp(-B/E_{ox}) \quad \textbf{(3.6)}$$

where $A_F = 1.25 \times 10^{-6}$ A/V^2, B ~240-MV/cm, J is the current-density in A/cm^2, and E_{ox} is the oxide field in V/cm.[17] According to this equation, the oxide current is exponentially dependent on the electric field and experimental studies have found that the equation accurately describes the oxide current. This can be seen in Fig. 3-20, which shows the measured gate current and the gate current calculated using Eq. 3-6 in oxides 6-nm- and 8.3-nm-thick. The tunneling probability rapidly rises as E_{ox} increases because the tunneling distance (i.e., the

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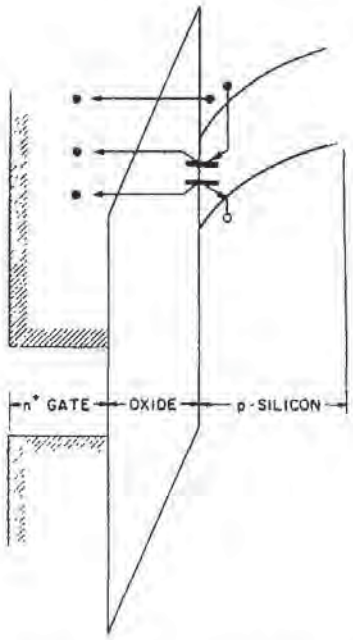


Fig. 3-18 Energy-band diagram for the phenomenon of Fowler-Nordheim tunneling in the MOSFET gate oxide. Also shown are some possible interface-trap assisted leakage paths, with trap levels indicated by short, solid bars.

distance from the Si-surface through the triangular barrier to the oxide conduction-band) becomes smaller as E_{ox} increases.*

It should also be noted that it may be possible for electrons to be "hot" but still not possess sufficient energy to surmount the barrier. In this case, carrier injection may occur by allowing these hot-carriers to tunnel through a smaller triangular-barrier distance. Thus, a synergistic combination of processes which individually would not have caused injection may yet enable carriers to be injected. This effect was modeled by Ning and Yu.[18]

At an oxide electric-field of 8-MV/cm, the measured Fowler-Nordheim tunneling-current-density is about 5×10^{-7} A/cm^2. Thus, for normal device operation, Fowler-Nordheim tunneling does not produce enough gate-current leakage to be significant. Hence, Fowler-Nordheim tunneling does not represent an issue when gate-oxides get thinner as the gate length of MOSFETs are scaled, even to deep-submicron gate-lengths.

3.4.2 Direct Tunneling (Tunneling Through Silicon Dioxide)

If the oxide is very thin (say 4-nm or less), electrons from the inverted silicon

* Because the distance of tunneling between Si surface and the oxide conduction band decreases with increasing electric field.

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surface can tunnel *directly* through the forbidden-energy-gap of the oxide layer instead of tunneling into the conduction-band of the SiO_2 layer. In direct-tunneling, electrons tunnel through a trapezoid-shaped barrier as shown in Fig. 3-19. (Because of the differences in the height of barriers for electrons and holes, and because holes have a much lower tunneling-probability in oxide than do electrons, the tunneling limit will be reached earlier for NMOS than PMOS.)

The theory of direct-tunneling is even more complex than that of Fowler-Nordheim-tunneling, and there is no theoretical simple dependence of the tunneling-current-density on voltage or electric field. (While an expression for the tunneling probability can be derived, no analytical expression is available for direct tunneling (as exists for the case of F-N tunneling). Instead, direct-tunneling-current must be calculated from numerical analysis, and the results of such calculations are plotted in Fig. 3-20.[19]) Nevertheless, experimental data indicates that tunneling current exhibits a weaker dependence on oxide fields than is shown by the equation that governs Fowler-Nordheim tunneling (Eq. 3-6). This means that direct-tunneling dominates in thin oxides at low voltages.

For oxide thicknesses smaller than 3-nm, the direct tunneling-current becomes very large. Figure 3-21 is a plot of the measured and simulated thin-oxide tunneling-current versus voltage in polysilicon gate MOSFETs. For the gate-voltage range shown in Fig. 3-21, the current is primarily a direct-tunneling current.[20] This tunneling represents a limit on the oxide thickness that can be used. This limit will be reached approximately when the gate-to-channel tunneling-current becomes equal to the off-state source-to-drain subthreshold

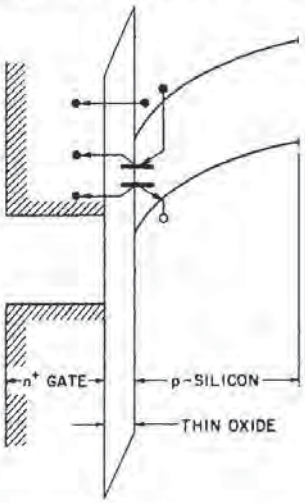


Fig. 3-19 Energy-band diagram for the phenomenon of direct tunneling through the gate oxide for thin oxides. Also shown are both unassisted-tunneling and some possible interface-trap-assisted leakage paths, with trap levels indicated by short, solid bars.

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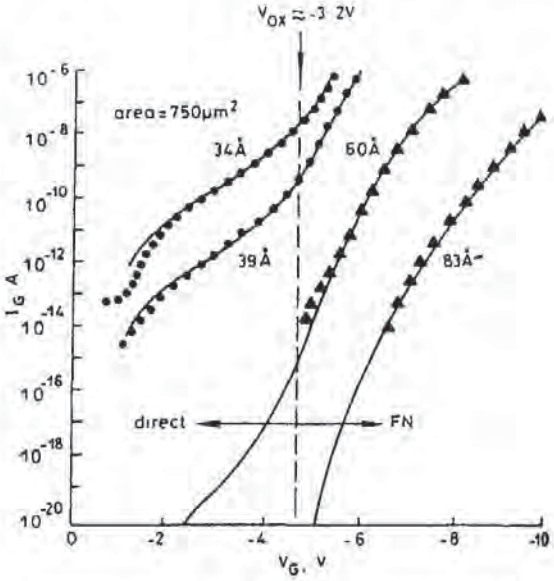


Fig. 3-20 Theoretical (and experimental) tunneling I-V curves of Al-gate *n*-channel MOS structures under negative gate-bias, illustrating the I-V characteristics of Fowler-Nordheim tunneling in 6-nm- and 8.3-nm-thick oxides and the calculated direct tunneling- currents in 3.9-nm- and 3.4-nm-thick oxides.[19] (© IEEE 1983)

leakage current (e.g., $I_{off}/W = 10$ nA/μm). That is, a MOSFET with a 1-μm gate length and width, would have a channel area of 1-μm^2. Thus, to keep its value equal to the subthreshold source-to-drain leakage current, the tunneling leakage current density should not exceed 10^{-8} A/μm^2 (which is equal to 1 A/cm^2).

From Fig. 3-21, the minimum oxide thickness that could be used to achieve a gate current density of 10^{-8} A/μm^2 is 1.4-nm.* Since this is the thickness of the oxide needed for the 70-nm generation (according to the L_E/t_{ox} guideline given at the beginning of Sect. 3.1 of this chapter), it appears that alternative gate-dielectric materials with reduced gate-leakage will be required for 50-nm MOSFETs and beyond. (Another, more detailed analysis of the leakage-currents in CMOS technology in the 100-nm regime arrives at the same oxide-thickness limit due to tunneling-leakage as the one given above [i.e., 1.4-nm].[30]) This topic is considered in Chap. 4. It should also be noted that logic circuits can usually withstand higher leakage currents than can DRAMs. Therefore. the gate oxide

* Note that the data shown in Fig. 3-21 are the results of work by researchers at Agere Systems.[20] They used an *in-situ* cleaning of the silicon surface (with HF gas, followed by ultra-violet [UV] cleaning) before the rapid-thermal-oxidation. The ultra-thin oxides they grew using this cleaning sequence resulted in oxides with very-low gate leakage currents (Fig. 3-21). Ultra-thin oxides grown by wet rapid-thermal-oxidation (RTO) processes have also reportedly shown smaller gate leakage currents (see Sect. 3.6.2).

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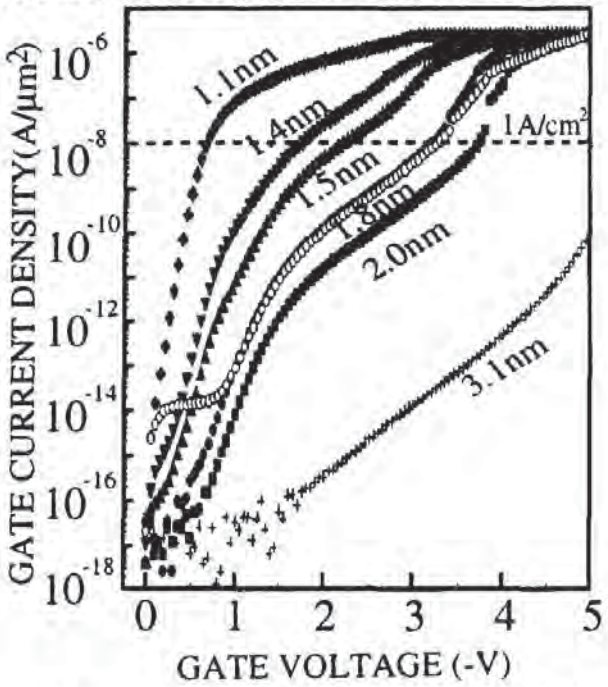


Fig. 3-21 Negative gate-current-density as a function of negative gate-voltage for oxide thicknesses from 1.1-nm to 3.1-nm, showing gate tunneling-leakage-current-densities.[20]

limit for DRAMs is expected to be larger (about 3-nm will be the minimum oxide thickness for DRAMs).

3.5 MODELS OF THIN-OXIDE GROWTH

The Deal-Grove model described in Vol. 1 for the growth of SiO_2 provides excellent agreement with experimental observations for thick oxides.[21] That is, the rate-constants derived in the Deal-Grove model allow the thickness of oxide films >350-Å to be well predicted as a function of temperature, furnace-ambient, silicon-doping-concentration, and silicon-crystal-orientation. However, the model does not give a detailed understanding of the mechanisms that produce these dependencies, nor is it valid when the oxide is thinner than 200-Å. Specifically, the experimental measurements of oxide-growth-rates in dry-O_2 are not accurately predicted by the Grove-Deal for oxides less than about 200-Å (20-nm). This is the so-called *anomalous regime* of the Deal-Grove model. This is particularly troublesome because gate-oxide-thicknesses of $\leq$ 100-Å are used for sub-micron MOSFETs. Figure 3-22 depicts a computer simulation of the formation of the first few layers of oxide being grown on a silicon surface.[22]

Several physical mechanisms have been proposed as models for the enhanced oxidation that is observed when oxides thinner than 200-Å are grown in dry-O_2, including:[23]

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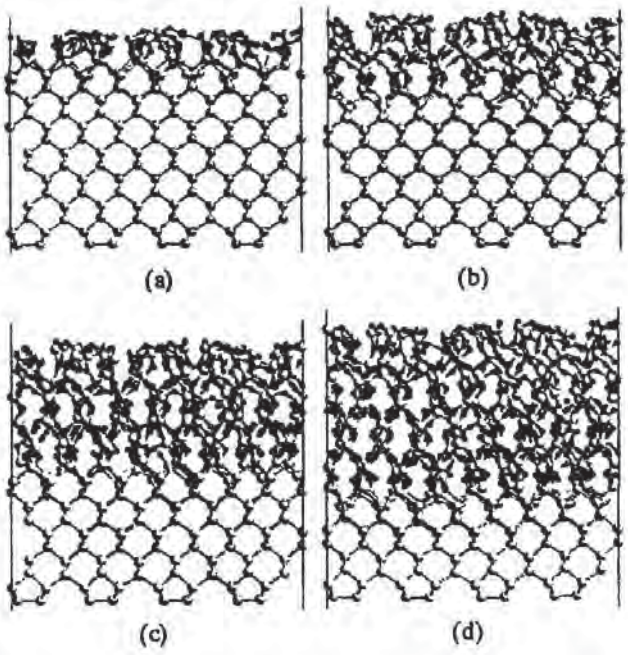


Fig. 3-22 Si(100)/SiO_2 interface structures after oxidation of a) 2nd b) 4th c) 6th d) 8th layer.[22]

1. Models based on space-charge effects where the oxidation-enhancement in the thin regime is due to field-assisted oxidant-diffusion (arising from O_2^- coupled diffusion with holes).

2. Models based on the existence of structural defects in the oxide, such as micropores or channels (~10-Å in diameter). These would allow the oxygen molecules to diffuse more rapidly when the oxide is thin.

3. Models based on parallel O_2 and O reactions at the Si/SiO_2 interface.

4. Models which postulate that a blocking layer exists near the Si/SiO_2 interface which forms as the oxide grows and slows down the rate for thicker layers.

5. A model by Massoud *et al.*, based on the presence of a thin surface layer in the silicon where additional reaction sites are available. The concentration of these sites decays exponentially with a characteristic decay length L_2 in Eq. 3-9.[23]

Despite the large number of models proposed to explain oxide growth in this very-thin regime, none has yet been shown to be clearly correct, and thus none have been convincingly accepted as more valid than the others. We are therefore left with several empirical models that yield reasonable agreement with measured values of oxide thickness in the thin regime, but with no completely satisfactory

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physical explanation. Additional work in the future may help clarify some of these issues.

One *empirical* model for thin oxide growth was proposed by Reisman and Nicollian in 1987.[59] By analyzing a vast amount of data, they derived an empirical model that calculates the oxide thickness versus time using a general power law of the form:

$$t_{ox} = a\,(t_g + \tau)^b \qquad \textbf{(3.7)}$$

where a and b are constants, and t_g is the growth time measured in a given experiment, and τ is the time to grow an oxide of thickness t_{ox_i} already present on the surface. Their model could fit all published dry-O_2 data. In fitting this equation to experimental data, they extracted b values between 0.25 and 1.0, depending on temperature and oxidant-partial-pressure. This equation has two fitting parameters (a and b), just as the Deal-Grove model has two (A and B/A). However, there are significant differences between the models. First, the Reisman-Nicollian model is claimed to be able to fit data down to oxide thicknesses of essentially zero thickness. There is no anomalous regime, as exists with the Deal-Grove model. Second, each model has its own physical basis for the oxide growth process. The Deal-Grove model is based on the idea of oxidant-diffusion and an interface-reaction - with each process dominating the growth under different conditions. Reisman suggests that the interface-reaction actually controls the oxidation process at all times, and that the volume expansion necessary at that interface to accommodate the growing oxide was provided by viscous-flow (relaxation) of the oxide layer. The time-dependent viscous-flow of the oxide in the Reisman model, is used to explain the extracted pressure- and temperature-dependence of the parameters in that model (a and b). A third model by Han and Helms (which we will not consider in detail here), has also been proposed to predict oxide growth. We will, however, compare the results of the Reisman and the Han and Helms model to the Grove-Deal model in upcoming paragraphs.

A comparison between the Reisman-Nicollian model of oxide thickness and the Deal-Grove model is shown in Fig. 3-23. Data from Deal and Grove at 700°C are plotted on linear scales and Eq. 3-7 is plotted with measured values of a and b. Shown for comparison is Eq. 3-7 with the appropriate constants obtained by a fractional weighted least squares fit to the data.[24] Kouvatsos extracted the a and b parameters of Eq. 3-7 at 950°C and 1100°C for oxide growth in O_2 diluted in He, and found very good fit to the Reisman-Nicollian power-law model.[25]

Figures 3-24 and 3-25 again compare the predictions of the Reisman and the Han and Helms models with those of the Deal-Grove model. The model para-

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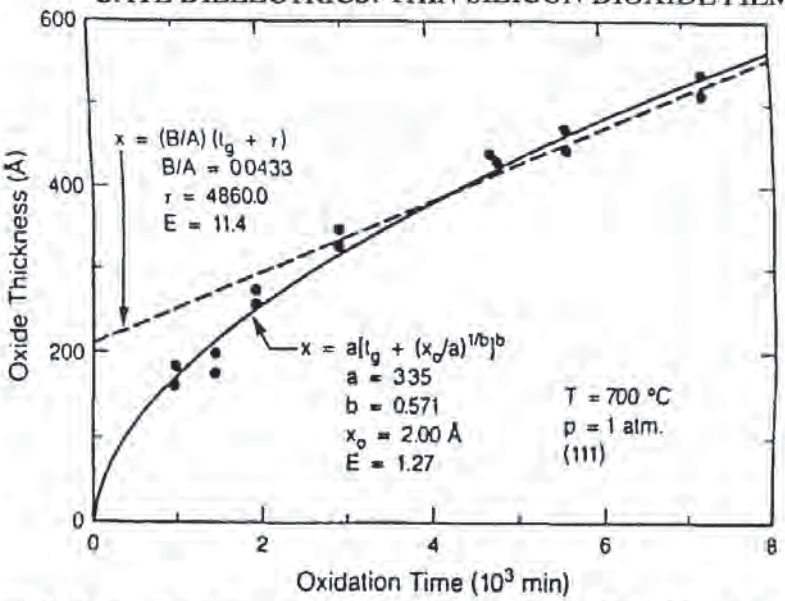


Fig. 3-23 Fits to oxide thickness versus oxidation time using the Deal-Grove model and the Reisman-Nicollian power-law model expression.[24]

meters for these plots for the Deal-Grove model are the standard A and B/A values for 1 atmosphere. For the Reisman model at 800°C, a = 0.302 nm, b = 0.704, and τ = 13.1 min. At 1000°C a = 3.02 nm, b = 0.701, and τ = 1.26 min. At 800°C (Fig. 3-24), the differences in these models for very-thin oxides is clear.

The Reisman (and the Han and Helms) model agree fairly well with each other and are a good match to experimental data in the thin regime. The Deal-Grove model does not do a good job for thin oxides, either with τ set at 8 hours

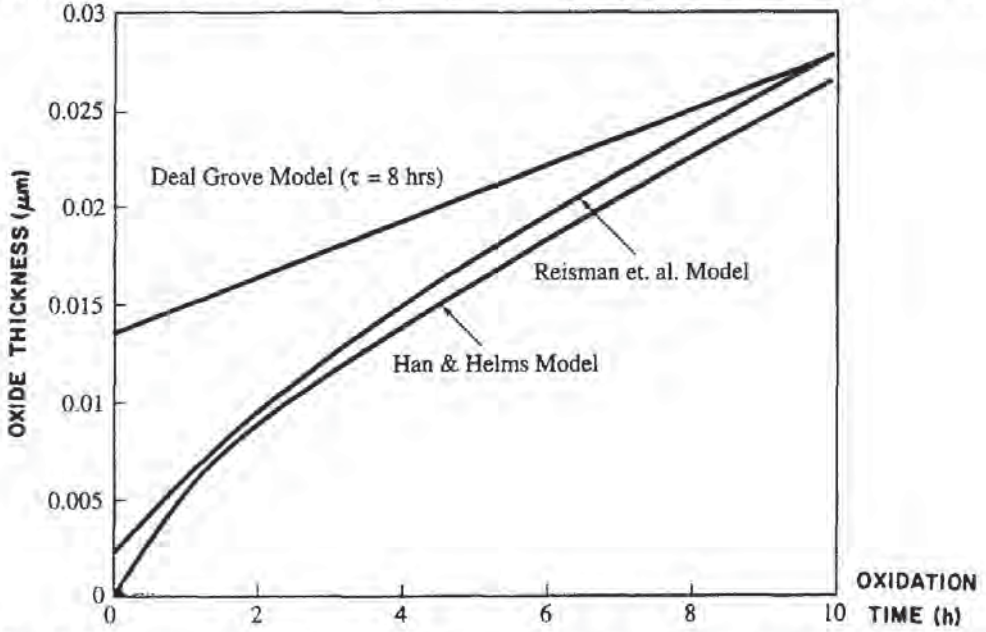


Fig. 3-24 Comparison of three oxidation models for 1 atmos, dry-O_2 oxidation at 800°C.

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(the value Deal and Grove extracted in their original work), or with $\tau = 0$ (which predicts even thinner oxide than do the Reisman or Han/Helms models). At 1000°C (Fig. 3-25), the differences in the models in the thin regime are less apparent since much thicker oxides grow at the higher temperature on the same time scale. For the particular parameters chosen for this plot, the Reisman-Nicollian model diverges from the predictions for thicker oxides.

Despite the fact that the Deal-Grove model in its original form does a poor job at predicting oxide growth in dry-O_2 in the thin-oxide regime, their model can be "fixed" to do a much better job. Such a"fix" was developed by Massoud *et al.*, who demonstrated that a much better fit can be accomplished than with the Deal-Grove model alone (by adding an additional term that decays exponentially with thickness to the oxidation rate.). The expression for the oxide growth-rate in the classical Deal-Grove model dt_{ox}/dt (see Vol. 1, Chap. 7) given by:

$$(dt_{ox}/dt) = B/(2t_{ox} + A) \quad \textbf{(3.8)}$$

then becomes

$$(dt_{ox}/dt) = \{B/(2t_{ox} + A)\} + C\exp(-t_{ox}/L_2) \quad \textbf{(3.9)}$$

where

$$C = C^0 \exp(-E_A/k_B T) \quad \textbf{(3.10)}$$

where $C^0 \sim 3.6 \times 10^8$-μm/hr, E_A ~2.35-eV, and L_2 is the characteristic decay length described in paragraph **5** above. For dry-oxidation of lightly doped substrates in

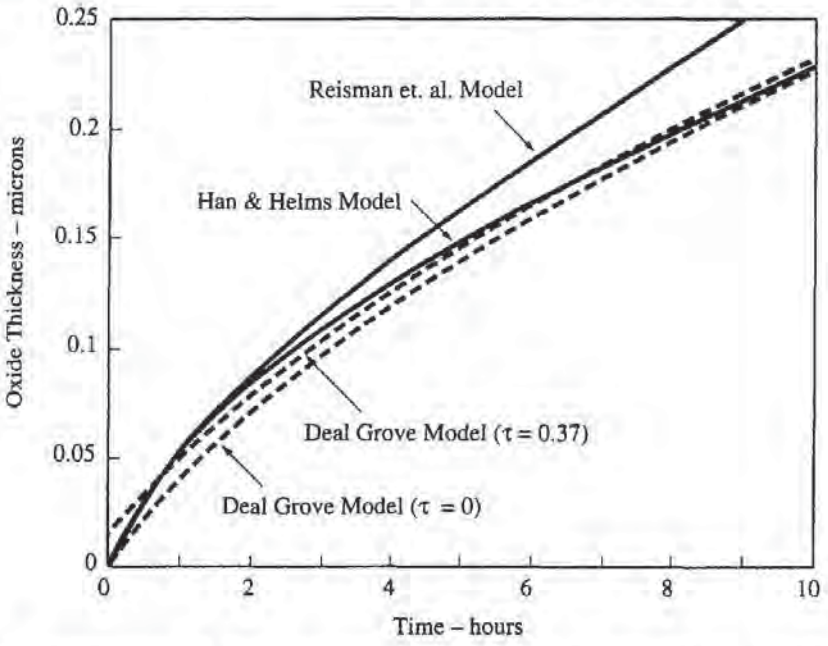


Fig. 3-25 Comparison of three oxidation models for 1 atmosphere, dry-O_2 oxidation at 1000°C. The dashed lines are the Deal-Grove model.

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the 800-1000°C range, L_2 was found to be ≅7-nm, independent of surface orientation [i.e., the above numbers apply to either (100)- or (111)-oriented silicon substrates]. Heavy doping was found to only slightly affect the oxidation-rate-enhancement in the thin regime. Equation 3-9 has been inserted into SUPREM III and SUPREM IV as the model for thin-oxide growth in dry-oxygen. With Massoud's addition to the Deal-Grove model, its predictions match the data well over the whole thickness range. Note that it was decided to implement the Massoud model (but not the Reisman model) in SUPREM III and IV. This is because many other oxidation-effects have also been tied to the basic Deal-Grove model, and these effects are also modeled in SUPREM III and IV.

While the debate continues about the physical mechanisms responsible for thin oxide kinetics, the problem has taken on a new importance. This is because deep-submicron MOSFET gate-oxides are routinely grown with thicknesses in the anomalous regime. This is an example of an industrial application outpacing basic scientific understanding. From the industrial view, it is more important to be able to grow thin oxide layers reproducibly and uniformly (and with good electrical properties), than it is to understand the governing physical principles.

3.6 SINGLE-WAFER TECHNOLOGY OF THIN OXIDE GROWTH

Thin oxides can be grown using a batch process or a single-wafer process. Batch processes currently use vertical furnaces (200-mm wafers), and such tools are discussed in more detail in Vol. 1, 2nd Ed. With the advent of 300-mm wafer processing and the need to grow uniformly-thick 20-nm oxides across such 300-mm wafers, the single-wafer process may begin to make inroads against batch-oxide-growth processes. Here we will limit the discussion to such single-wafer oxide processes, which are also based on rapid-thermal-oxidation (RTO) methods. Note that single-wafer RTP processes are also described in Vol. 1, 2nd Edition, Chap. 7, and a more comprehensive review of RTP systems and processes is given in Ref. 26. However, in both of these references, the focus is more on the general aspects of RTP systems. Here our focus is on the details of rapid-thermal-oxidation (RTO) tools and processes. Wet-RTO processes are also examined, a topic not covered in Vol. 1, 2nd Ed.

3.6.1 Rapid Thermal Oxidation Tools

Conventional furnace-based oxidation has been the workhorse of the industry, but it encounters some problems when gate oxides thinner than 2.0-nm must be grown, including: **1**) furnace oxidation is difficult to scale below 2.0-nm thickness; and **2**) the lower temperatures used during such ultra-thin oxide growth processes degrade the oxide quality.

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RTO is able to offer better quality ultra-thin oxides when compared to those grown in furnaces for two reasons: **1**) RTO grows the oxides at higher temperatures; and **2**) RTO is more conducive to cluster tooling. RTO can grow thin oxides at high temperatures because the oxidation time is kept down to just a few seconds (whereas the minimum oxidation time in a batch furnace is at least a few minutes).

There are several advantages to growing oxides at higher temperatures. First, oxides exhibit smaller gate-leakage-currents as their growth temperature increases (up to a maximum of 1050°C, beyond which leakage-currents increase).[27] Second, they show higher resistance to boron penetration. In one study, 2-nm-thick oxides grown in a furnace at 800°C were compared to RTP-grown oxides at 1000°C. The results indicated that boron penetration was suppressed better by the RTP-grown oxides.[28] The third advantage is that MOSFETs built with the RTP-grown oxides had higher effective carrier mobilities (for both electrons and holes) as the temperature of the oxide growth process was increased from 800°C to 1000°C.[29] This was attributed to the smoother Si/SiO_2 interface that results from growing the oxides at higher temperatures.

Cluster tools can potentially produce better-quality oxides because they allow process sequences to be carried out in an integrated fashion. For example, in oxide growth processes, a cleaning procedure is done prior to the growth step. If this can be done *in situ,* the quality of the oxides can be improved. Clustering is easily achievable with single-wafer RTP systems, but is impractical with batch furnace tools. By integrating RTO chambers with other processing modules it may be possible to extend the use of oxides to additional technology generations.

As noted above, with the introduction of single-wafer RTO-systems, it becomes possible to carry out *in situ* surface preparation, wafer rotation, ambient control, and process integration. Because such systems can grow oxides at such rapid rates (i.e., more than 1000-Å/min), it also makes RTO capable of competing economically with vertical hot-wall furnaces.

Figure 3-26 is a cross-sectional view of an RTO reaction-chamber depicting the necessary components of a lamp-heated RTO-system. In this reactor, the wafer is inserted into the reaction chamber by a robot wafer handler onto a rotating SiC support ring. The wafer is rapidly heated at rates of 50-100°C to the process temperature (800-1050°C). Process gases are introduced at reduced pressure in an axial flow pattern where they react to form water vapor, hydroxyl ions, oxygen ions, and other species (depending on the H_2:O_2-ratio and whether N_2, NH_3, HCl, or other reactant gases are introduced). At the conclusion of the oxidation and annealing steps, the wafer is cooled rapidly to a temperature where

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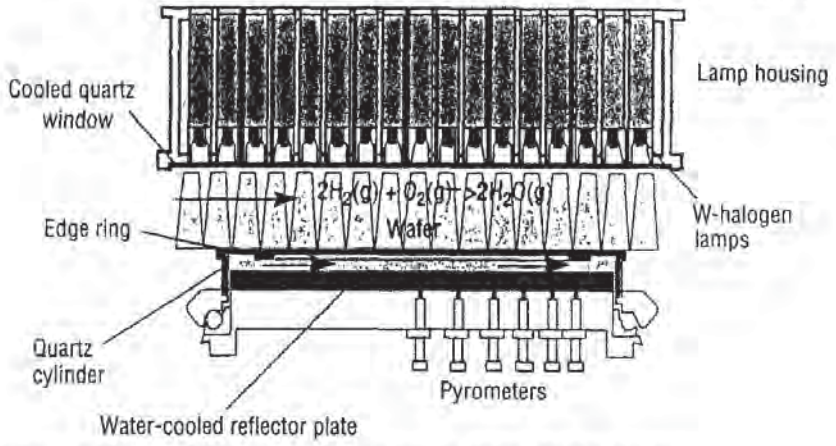


Fig. 3-26 Cross-section of an Applied Materials ISSG RTO reactor.

it can safely be removed by the wafer handler from the reaction chamber to an additional cool-down chamber that can be used to enhance system throughput. Cool-down can be enhanced further by providing a wafer backside cooling gas, such as helium or hydrogen.

3.6.2 Wet RTO Processes

As will be discussed in Sect. 3.8, traditional dry oxides are expected to be limited to minimum thicknesses somewhere between 1.6-nm[36] and 2.5-nm.[37] Various techniques are being explored to reduce this thickness limit. One of these methods employs wet-RTO. A technique pioneered by Applied Materials called *in-situ steam generation (ISSG)* has reportedly allowed oxides in the 2.0-nm thickness range to be formed with improved reliability compared to dry oxides of the same thickness.[38] ISSG-oxidation is a low-pressure process (typically below 20 torr, for safety reasons) performed in a cold-wall RTP reactor.

Unlike hot-wall furnaces that employ a pyrogenic torch for growing wet oxides, no hot quartz is used to generate the steam ambient (eliminating the problem of quartz devitrification). Instead, in ISSG-oxidation, H_2O, OH and atomic oxygen are generated directly in the reaction chamber without pre-combustion. The hot wafer acts as an ignition switch, causing reactions among electronic-grade H_2 and O_2 gases (that are pre-mixed in a plenum before being injected into the RTP chamber). This configuration reduces risk of metal contamination, since no metal catalyst is used in the in-situ steam generation method.

The oxidation-rate rapidly *increases* as the pressure is decreased below 20 torr (unlike in conventional oxidation processes where oxidation-rates decrease with decreasing pressure). The growth-rate at 10-torr is nearly twice that of atmospheric dry-rapid-thermal-oxidation. Modeling studies indicate that the oxidation-rate exhibits a strong correlation to the atomic-oxygen-concentration

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and not to any other atomic or molecular species. The oxidation-rate is also strongly temperature-dependent compared with wet-atmospheric-oxidation.

Oxides grown with the ISSG process show good characteristics. Within-wafer uniformity and wafer-to-wafer repeatability are well below 1% (1σ), both for thin (< 40-Å) and thick (> 100-Å) oxide-films. The faster growth-rates improve productivity while offering a thermal-budget reduction. The wide range of temperatures and hydrogen concentrations allow controlled oxidation for any thickness of oxide. The ISSG-oxides also demonstrate better reliability than comparable furnace-oxides, or those created by dry-RTO. Several independent measurements of charge-to-breakdown of 30-50-Å wet-RTP oxides show a threefold (or more) improvement over furnace-grown-oxides. The wet-RTO-oxides also exhibit about an order-of-magnitude less gate-leakage-current than dry-RTO oxides, which are comparable to furnace-grown-oxides (Fig. 3-27).[76]

3.7 NITRIDED AND FLUORINATED OXIDES AS MOSFET GATE DIELECTRICS

One modification to the basic SiO_2 material that has recently been intensely examined is the addition of nitrogen to the oxide. That is, oxynitrides have been studied as replacements for silicon dioxide as the gate dielectric of MOSFETs for thicknesses below 4.0 nm. The advantages of oxynitrides over silicon dioxide for this application are the following: **1**) they exhibit improved boron penetration resistance; **2**) they have better breakdown characteristics; **3**) they show greater immunity to hot-carrier-injection effects; and **4**) MOSFETs made with such layers exhibit improved high-field channel-electron-mobility. Improved performance of nitrided silicon-dioxide gate-dielectrics has been associated with the accumulation of a small amount of N at the Si/SiO_2 interface. Interfacial N-accumulation is thought to reduce interfacial defects by relieving strained Si-O bonds and "dangling" bonds. An interfacial peak-concentration of about 1-2 atom % is typically associated with higher breakdown electric fields and lower fixed-oxide charge densities. But, a higher N-concentration (> 5 atom %) is needed to effectively suppress boron penetration through the dielectric layer.

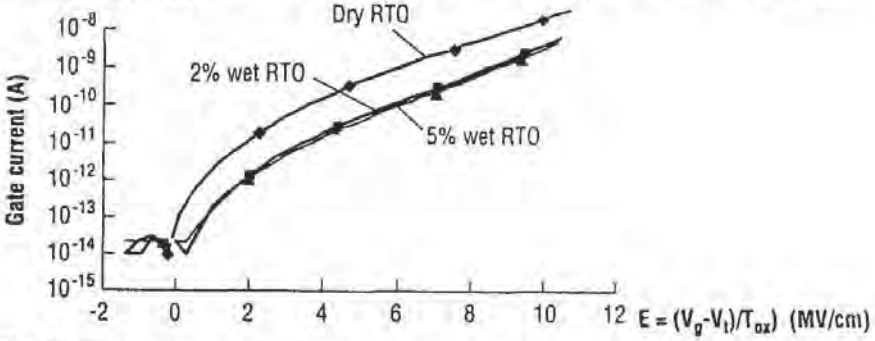


Fig. 3-27 Gate leakage current comparing dry-RTO to 2% & 5% ISSG RTO for 30Å oxides.[76]

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Nitridation of oxides is considered to be a variation of silicon oxidation, and such films are formed mainly though the nitridation of silicon oxide or the oxidation of silicon in a nitrogen containing ambient such as NH_3, N_2O, NO (or mixtures of O_2 and NO). Such films have been formed in high-temperature furnace processing or rapid-thermal-processing tools. Fluorine can also be incorporated into gate oxides as a method for improving its dielectric characteristics. This subject is also discussed in a following section.

3.7.1 Oxynitridation of Silicon in N_2O

Early oxynitride films were formed by nitriding a thermally grown oxide film by exposing it to an NH_3 ambient at high temperatures, and then re-oxidizing the nitrided oxide to reduce the amount of hydrogen that remains in the film after NH_3 nitridation. Such oxynitrides were thus called *reoxidized nitrided oxide* (*ROXNOX*) films.

Although ROXNOX films exhibit better hot-carrier resistance than do pure oxides, some practical issues make them troublesome to manufacture. First, the ROXNOX formation sequence is complex and difficult to optimize, especially for CMOS applications. For example, the combination of nitridation and reoxidation steps used in the ROXNOX process may leave excess hydrogen in the film. In that case, the density of electron traps will be higher than in a pure oxide film. Since electron trapping is the dominant degradation mechanism in PMOS devices, PMOSFETs with such films will exhibit worse hot-carrier degradation.[39] On the other hand, if the reoxidation step is excessive, the film can lose its strength against interface-state generation by hot-carriers. Thus, NMOSFETs containing such films would be prone to more hot-carrier degradation. The gate dielectric layer might also grow too thick. Another drawback is that the best NH_3-nitrided films always exhibit higher densities of positive fixed charge (Q_f) than do the best SiO_2 films. The fixed charge arises as a result of the nitridation process. Finally, the ROXNOX process generally involves multiple high-temperature steps, which are undesirable for ULSI CMOS applications. As a result, ultra-thin oxynitrides are not formed in production by using NH_3 as the nitrogen source.*

A solution to some of the problems of NH_3-nitrided films is to avoid the incorporation of hydrogen in the film in the first place. One way to accomplish this is to replace NH_3 with N_2O as the nitriding ambient. Such N_2O-based techniques have indeed proved to be more fruitful because of the hydrogen-free nature of the processing.

* Interested readers can find more details on ROXNOX films in Vol. 3.

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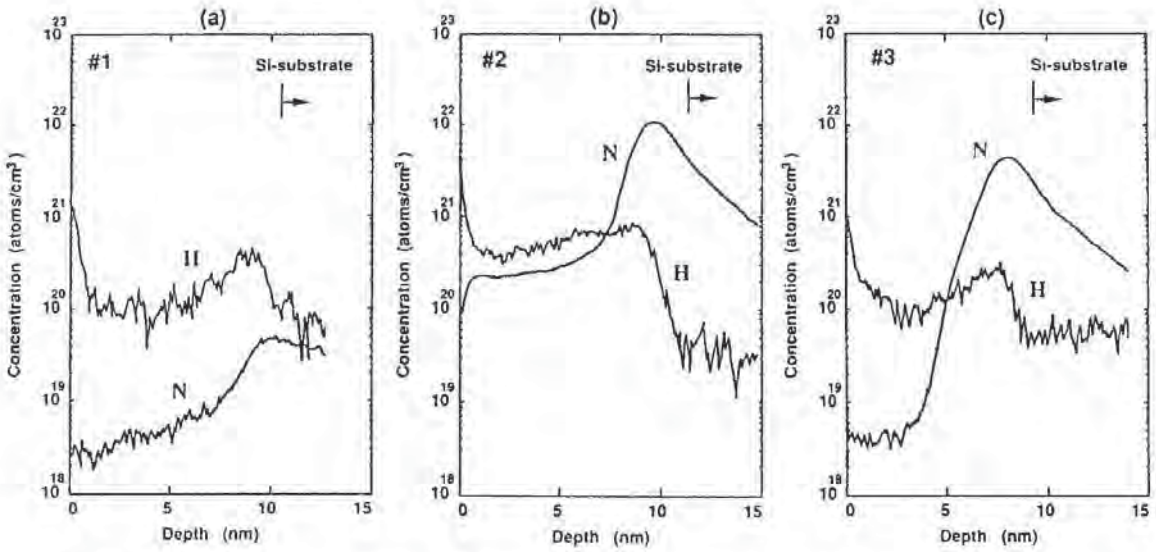


Fig. 3-28 SIMS depth profiles of N and H in three kinds of oxide films: (a) pure SiO_2 (#1); (b) NH_3-nitrided SiO_2 (#2); and (c) N_2O-nitrided SiO_2 (#3).

This approach was first used to grow a gate dielectric by directly reacting N_2O at the silicon surface in an RTP system.[40,41,42,43] Since there is no hydrogen in N_2O, this process results in films with significantly less incorporated hydrogen than NH_3-nitride films. Figure 3-28 shows SIMS profiles of dielectric films prepared by: (a) thermally oxidizing silicon; (b) nitriding an oxide film in NH_3; and (c) growing a film on silicon by RTP in an N_2O ambient.[41] It can be seen that the hydrogen concentration in the N_2O film is significantly smaller than in the NH_3 film. It is also evident that the nitrogen concentration in the N_2O film is highest at the Si-SiO_2 interface. Early studies of such films concluded that they are self-limiting in thickness, as is shown in Fig. 3-29a.[40,44] The build up of the nitrogen concentration was thought to block the oxidation reaction that occurs simultaneously at the interface. Later work showed that the thickness was not self-limiting (see Fig. 3-29b),[45,46] and that the thickness in fact, increases approximately as $(\text{time})^{1/2}$. This seems to indicate that the growth is instead limited by the diffusion of N_2O through the oxide bulk (rather than through the nitrogen-rich layer).[47] The discrepancy in the apparent growth mechanisms may have been explained by Okada, who observed significant retardation of the growth only at relatively high (~0.9 at%) interfacial nitrogen concentrations, which is higher than observed in some N_2O furnace processes.[59] However, the interfacial reactions may still dominate growth rates for short times and thin oxides.

Nevertheless, the nitrogen profile in the N_2O film is similar to that in the ROXNOX film, yet this is achieved with only a one-step process (i.e., no

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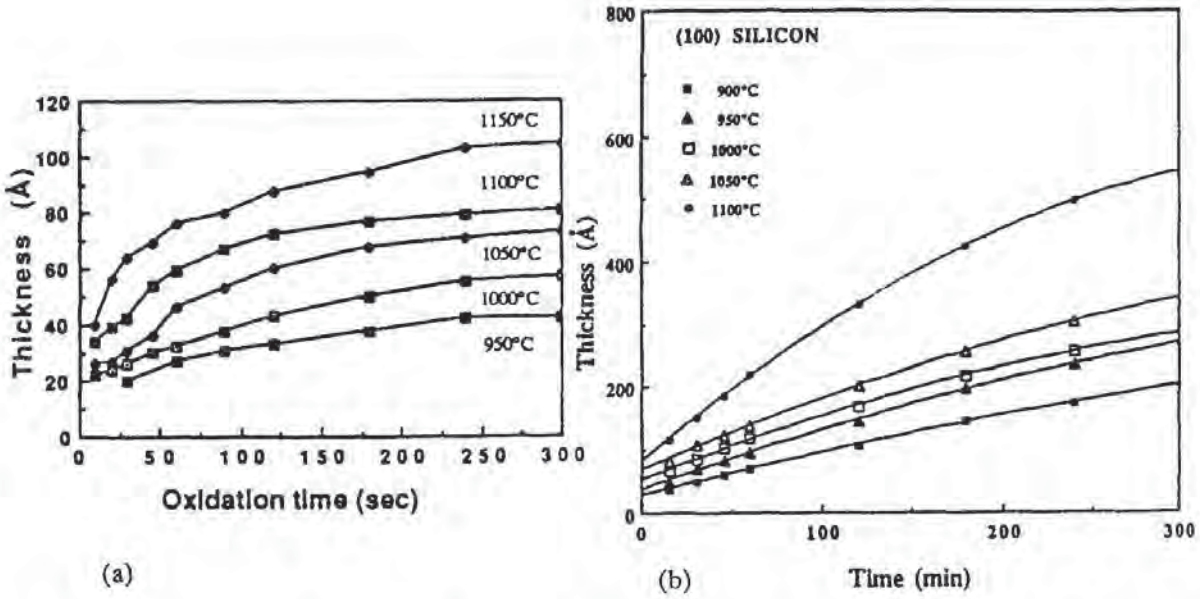


Fig. 3-29 (a) N_2O oxynitride thickness versus oxidation time using RTP for various process temperatures. Ramp-up rate was 200°C/sec. Oxide thickness was measured at a fixed refractive index (1.46)[40] (© IEEE 1990); (b) N_2O oxynitride thickness versus time in a furnace-anneal process. (© Electrochemical Society 1993)[45]

reoxidation is necessary). The peak nitrogen concentration (at the Si/SiO_2 interface) is ~0.5%, which is less than that found (2-10 atom%) in SiO_2 furnace-nitrided in NH_3 under atmospheric pressure. Furthermore, residual hydrogen incorporation into the film is no longer a concern. This is evidenced by the low electron trapping density exhibited by such films. NMOSFETs fabricated with such films also exhibited less tendency toward hot-carrier degradation than those made with control oxides (i.e., they showed smaller values of ΔD_{it}), and were also less susceptible to the creation of electron traps throughout the oxide under hot-carrier stressing.[48]

However, several limitations were still observed in these N_2O-grown oxynitrides. First, larger initial values of D_{it} were observed than in pure oxide films (Fig. 3-30), even though the rate of their generation under hot-carrier stressing was much smaller (see also Fig. 3-30).[48] Second, the initial Q_f values were also somewhat higher. Third, the slow growth-rate of such films make them only practical for ULSI applications which use dielectric films thinner than 100Å (see Fig. 3-29). Fourth, the maximum mobility of electrons in MOSFETs made with such films is ~5% less than in MOSFETs with oxide gate dielectrics (but the mobility is actually higher at large lateral electric fields - see Fig. 3-31).[49] The most severe limitation, however, is that such RTP N_2O-grown films exhibit

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unacceptably large nonuniformities in composition and thickness across a wafer.[50] Such non-uniformities would limit the use of such films in ULSI MOS devices. Temperature nonuniformities in the RTP chamber, gas depletion, and heat-transfer effects were some of the phenomena suspected of leading to these nonuniformities.

Nevertheless, it was found that growth of such N_2O dielectrics in a furnace (rather than by RTP) resulted in films with thickness uniformities comparable to those of pure oxide films, and with adequate compositional uniformity as well.[51,52] The process described in these reports was a 950°C furnace step in N_2O, which grew 60-Å-thick dielectric films having a nitrogen concentration at the Si/SiO_2 interface of ~3%. Hot-carrier degradation of PMOSFETs with such films was excellent since electron-trap-densities in these films was also low.

3.7.2 Oxynitridation of Oxides in N_2O or NO

Another method used to form thin oxynitride layer involves a two-step operation. Oxides are first grown in O_2, and are then subjected to an oxynitridation step in N_2O or NO. When N_2O is used as a post-oxidation-annealing ambient, a wide range of final oxide thicknesses is achievable with much smaller thermal budgets. Processes using this two-step N_2O sequence have been described using an atmospheric-pressure-furnace,[46,53,54,55] a low-pressure-furnace,[56] and RTP conditions,[57] Figure 3-32 shows an example of such a two-step process performed in a conventional furnace at atmospheric pressure.[54]

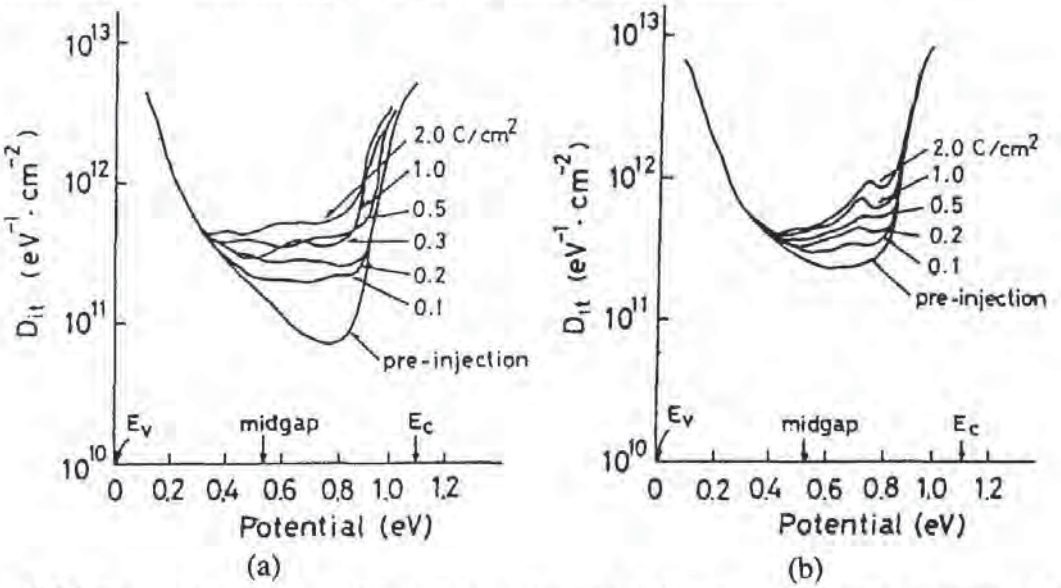


Fig. 3-30 Changes in the interface trap densities of MOS capacitors with: a) pure SiO_2; and b) SiO_xN_y by Fowler-Nordheim electron injection. Electrons were injected from the gate electrodes into the oxide films at a current density of ~10 mA/cm².[42] (© IEEE 1991)

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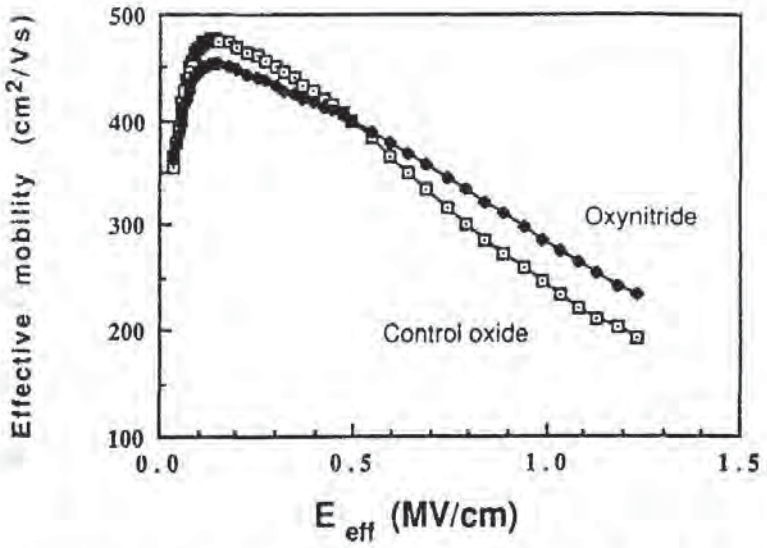


Fig. 3-31 Effective electron mobility versus effective normal field of NMOSFETs with a 65-Å-thick gate dielectric. The mobility values were calculated using the linear region I_D versus V_{GS} curves (V_{DS} = 100 mV), with a Z/L ratio of 75-μm/60-μm. The maximum effective mobility of the oxynitride is 5% lower than that of the control oxide. However, the high-field mobility of the oxynitride shows a 10% improvement.[49] (© IEEE 1991)

Typically, the oxide is grown in dry-O_2 in a furnace at 850-900°C. The N_2O step is usually carried out at 800-850°C for 5-40 minutes. In the process described in Ref. 55, 50-Å SiO_2 films are grown in dry-O_2 at 850°C for 30 minutes. During the second step in N_2O at 950°C, an additional 35-Å of oxide is grown to form films with a final thickness of 85-Å.

PMOSFETs made by oxynitridation of SiO_2 in N_2O also exhibit enhanced

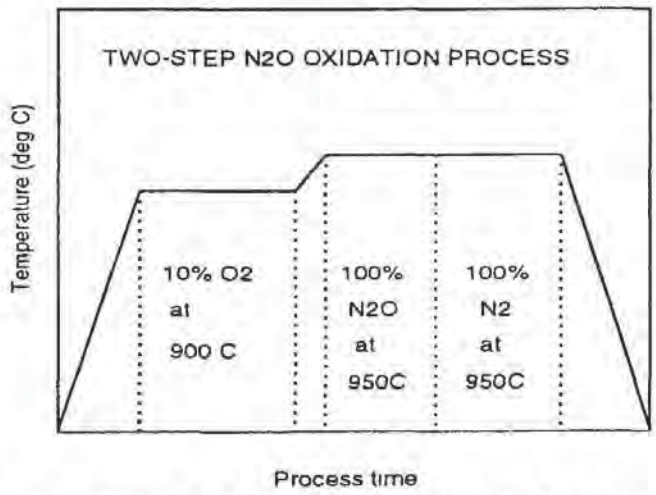


Fig. 3-32 Two-step oxidation & N_2O nitridation process in a conventional furnace.[54] (© IEEE 1993)

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hot-carrier immunity compared to devices made with pure oxide. This is thought to be due to the fact that electron trapping is suppressed in devices with such N_2O dielectrics.[58] Consequently, it has been suggested that the optimum N_2O oxynitride process is oxidation in O_2 followed by nitridation in N_2O, rather than oxidation in N_2O alone.

In the low-pressure approach[56] it was reported that a minimum pressure of between 1 and 50 torr of N_2O was needed before a measurable amount of nitrogen was incorporated into the oxide. However, at low pressures of N_2O (i.e., just beyond the minimum needed for the onset of nitrogen incorporation), the concentration of nitrogen at the interface could be well controlled, but at the same time, minimal additional oxide was grown during the oxynitridation step. Thus, tight control of the final film thickness could be maintained.

As noted in a previous paragraph, the oxide film continues to grow during the second (i.e., N_2O) step. However, if re-oxidation of N_2O oxides is carried out after they are formed, unusual behavior occurs. That is, new SiO_2 grows at the Si/SiO_2 interface, and the existing N-rich layer remains intact and is displaced away from the interface by growth of the new oxide (see Fig. 3-33).[59]

Using N_2O as the nitrogen source during the second step of this procedure was found to have some disadvantages. The concentration of N-incorporation may be

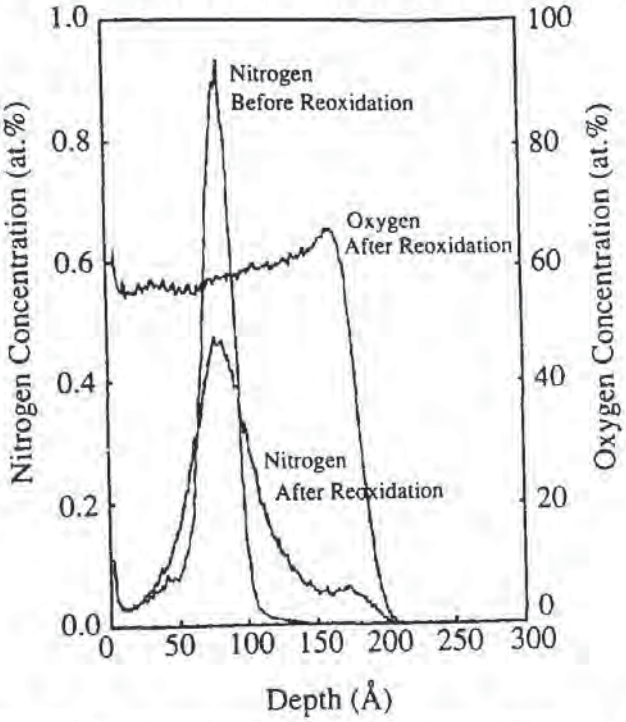


Fig. 3-33 SIMS profile of the oxynitride film grown from 100% N_2O at 1100°C before reoxidation, and after 85 min reoxidation.[59] By permission of the Electrochemical Society.

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too low for some applications, especially suppression of boron penetration, unless a much higher thermal budget is permitted.

More recently oxynitrides formed with the two-step process using NO as the nitrogen source have been reported. Generally, the results for NO oxynitrides overcame the problems of using N_2O as the nitrogen source, in that they offer a lower thermal budget process for incorporating higher concentrations of N, as well as better thickness control for scaled dielectrics.[60,61] It is thought that nitrogen incorporation in the N_2O process is driven by NO species, which is a product of N_2O molecule dissociation. The N_2O molecule likely dissociates into NO (4.7%), N_2 (64.3%), and O_2 (31%), according to calculations by Tobin *et al.*[62] Such by-products act in competition. That is, while the NO incorporates nitrogen, O_2 continues the oxidation by reacting with the silicon substrate, and N_2 reduces the partial-pressure of the nitridation species (which increases the thermal budget). The parallel oxidation explains the observed increase of oxide thickness during annealing in N_2O. The high temperature needed for N_2O dissociation (> 850°C) mandates the high thermal budget needed to get acceptable results. Good quality gate-dielectric-films have reportedly been produced with RTP processes using NO + O_2 mixtures.

The percent nitrogen incorporation also depends on the relative amount of NO in the gas mixture. Figure 3-34 shows the dependence of N incorporation on NO concentration for both direct (1-step), and 2-step oxynitride growth carried out in a NO + O_2 mixtures using RTP processes. This indicates that NO can produce

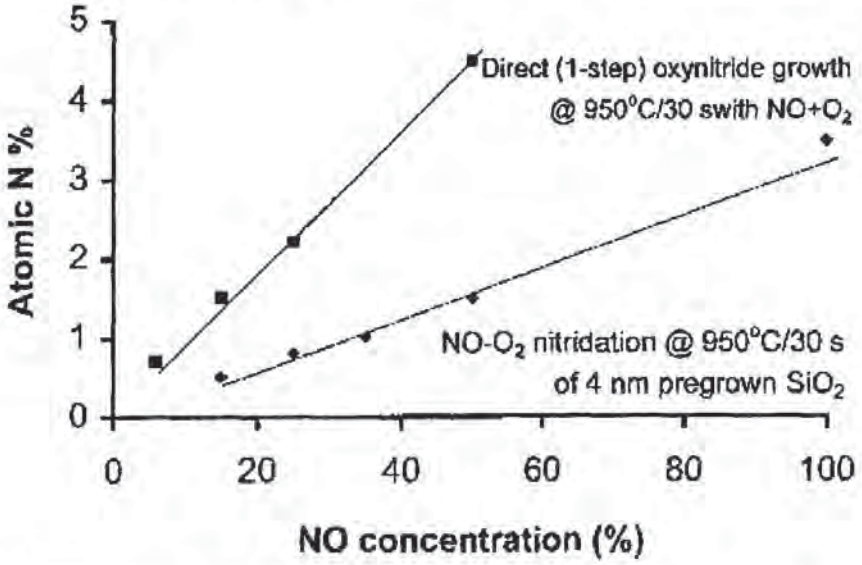


Fig. 3-34 Dependence of nitrogen incorporation in oxide on NO concentration in NO + O_2 mixtures.

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oxynitride films with a wide range of incorporated N, allowing the films to be tailored for specific applications.

In another reported process, 4.0-nm-thick oxynitrides were formed in a two-step furnace operation. First, 4.0 nm oxides were grown in O_2 at 800°C with a 6% HCl, and a post-oxidation anneal in N_2. The second step involved annealing this oxide in a diluted NO ambient at 800°C for 45 min.[60] Finally, a process that uses a mixture of N_2O and NO in the reaction chamber has been described. The postulated advantage of this method is that the vertical positions of the nitrogen concentration peaks within the oxynitride layer can be adjusted by changing the N_2O + NO mixture.[64]

We should also mention that adding nitrogen to gate oxides has also been reported by several other novel techniques, including implantation of nitrogen through the polysilicon gate and drive-in annealing,[64] reoxidation of films formed by growing the oxynitride in N_2O or NO,[65] and nitridation of the Si surface by using a nitrogen remote plasma.[66,67,68]

3.7.3 Fluorinated Gate Oxides

The presence of fluorine in the gate oxide has also been reported to increase the hot-electron resistance of devices fabricated with such oxides.[69,70] Such fluorine may inadvertently be introduced from a BF_2^+ source/drain implant, or from an LPCVD-W or LPCVD WSi_x process. (In the W-CVD and WSi_x-CVD processes fluorine is produced during the reaction of WF_6 and SiH_4.[71]) Other reports confirm that deliberate incorporation of fluorine into the gate oxide (from implanting fluorine into a polysilicon film, and then diffusing it into the gate oxide) produces a more hot-electron resistant interface.[72,73] The increased hot-carrier-resistance of the F-containing-oxides is thought to be due to fluorine atoms which form Si-F bonds. These are stronger than Si-H bonds. The presence of the fluorine implies that some of the Si-H bonds at the Si/SiO_2 interface are replaced by Si-F bonds, thus yielding an interface that has better hot-carrier-resistance.

Unfortunately, while the above benefits make fluorinated oxides attractive for NMOSFETs, the presence of fluorine in the gate oxide may increase the penetration of boron (from p^+-poly gates) though the gate oxides, and this represents a potential problem for deep-submicron PMOSFETs. That is, BF_2^+ is used when the shallow source/drain-extension-region is formed, and this implant enters the poly gate. Thus, the F from this implant will diffuse through the poly and into the gate oxide during the implant activation steps. However, a recent study indicated that if the fluorine dose implanted into the poly is restricted to a medium dose ($1x10^{14}/cm^2$), no noticeable enhanced boron penetration effect is

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observed. In addition, the charge-to-breakdown (Q_{BD}) characteristics of the PMOSFET capacitors fabricated with 4-nm-thick oxides are also significantly improved.[74]

Recently, a new form of "anomalous" leakage was discovered in oxides used in Flash-memory devices. Such leakage occurs at temperatures below 150°C, and thus cannot be screened by a traditional 250°C high-temperature retention bake. However, by incorporating a high concentration of fluorine in the tunnel oxide (introduced in a WSi_2 capped-control-gate process), a much higher resistance to this anomalous leakage is obtained.[75]

3.7.4 "Dual-Gate-Oxide-Thickness" Structures

An increasing number of mixed-signal and system-on-a-chip applications require dual on-chip power-supply-voltages. The higher-voltage may be used for the analog and input/output (I/O) circuitry, and the lower-voltage for the core digital-logic-devices. However, a serious reliability problem would be created if the same thin oxide needed for the high-performance logic MOSFETs was used in the devices subjected to the higher voltage (i.e., the analog and I/O circuitry MOSFETs). That is, the analog and I/O devices require thicker gate oxides than the core logic devices. (The thicker oxide also makes the I/O devices more robust against transient, off-chip electrostatic-discharge-events.) Consequently, it must be possible to fabricate gate oxides with different thicknesses on such ICs.

Early "dual-gate-oxide-thickness" processes had two oxidation steps, with a masked etch-step in between to remove the first oxide from regions intended to have thinner oxide. Newer processes use a different, simpler approach. That is, it has been discovered that the rate of thermal-oxidation on silicon is reduced by nitrogen implants.[88] Hence, nitrogen implantation into the silicon substrate prior to the oxidation process can be used to facilitate the implementation of such "dual-gate-oxide" ICs. Namely, selective implantation of nitrogen will cause oxides grown on such areas to be thinner than those simultaneously grown on non-implanted areas (Fig. 3-35a). Typical implant conditions for the nitrogen implant are energies of 10-30 keV, at doses of $2x10^{14}/cm^2$-$1x10^{15}/cm^2$. Figure 3-35b shows how the oxide thickness from an 800°C, dry-O_2 oxidation is reduced with increasing nitrogen dose.[89] It is suggested that nitrogen suppresses oxidation by forming Si-N bonds at the interface of the growing oxide, thereby constraining further growth.

3.8 PROJECTIONS OF THICKNESS LIMITS OF GATE OXIDES

In the late 1970's it was projected that the scaling limit of MOSFETs would be 0.5-μm. In the mid-1980's, this limit was reduced to 0.25-μm. In 2001, there

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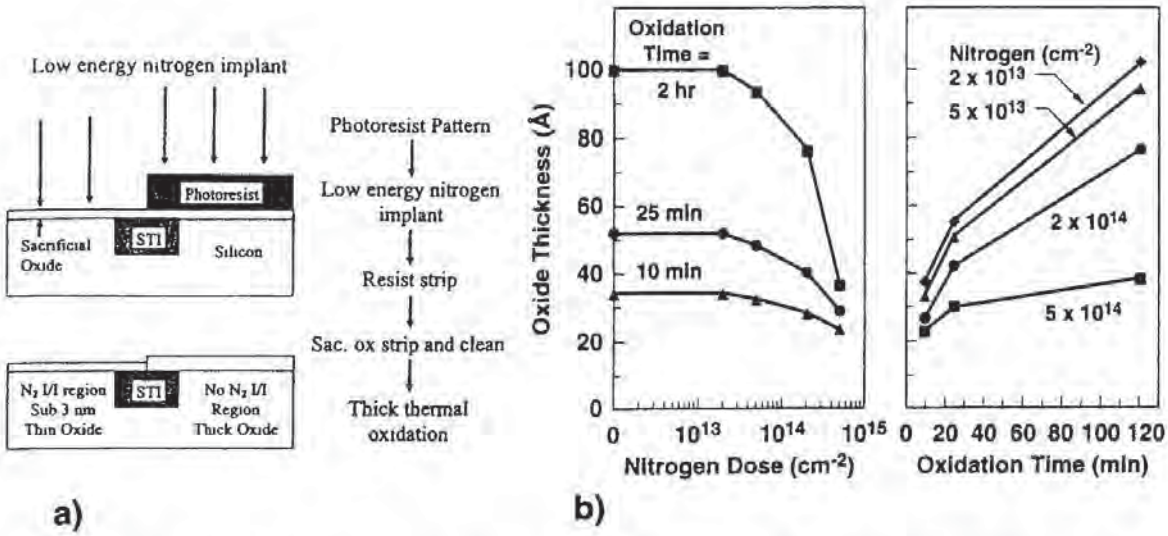


Fig. 3-35 a) Schematic of the process flow for sub-3-nm gate oxide formation on N_2-implanted substrates. b) Oxide thicknesses obtained in dry-O_2 at 800°C for various nitrogen implant doses (energy = 25 keV) and oxidation times.[89] (© IEEE 1997)

does not seem to be any device physics barrier for scaling at least to 0.05-μm (50-nm). The factor that kept the predicted limit on MOSFET gate lengths in previous decades higher than it is today was the uncertainty in the minimum thickness of the gate-oxide-layer that could be successfully implemented in MOSFETs as they were scaled. Thus, the question of the minimum-oxide-thickness that can be implemented in MOSFETs remains an important one. Here we address the predictions of the minimum-oxide-thickness as viewed in 2001.

There are a number of factors that play a role in the minimum-oxide-thickness that can be used, including: oxide-reliability, tunneling-leakage-current, stress-induced leakage-currents (SILC), polysilicon-depletion, process-induced oxide-damage, and hot-carrier-induced damage. The type of application in which the oxide is to be used also plays a role. That is, different minimum-oxide-thickness limits exist for logic devices, DRAMs, and nonvolatile memory devices. We will discuss each of these topics here, with the exception of hot-carrier-induced damage. The latter phenomenon is not treated because hot-carrier-reliability is expected to greatly improve as the gate voltage is decreased below 3-V (since at such low voltages, few carriers can gain sufficient energy to create interface-traps or shallow oxide-traps). This is one of the positive aspects of scaling devices below 0.25-μm.

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3.8.1 Minimum-Oxide-Thickness Due to Defects and Tunneling

The first two (and probably the most important) phenomena that impact the minimum-oxide-thickness that will be usable in full-scale IC production are: **1**) defect densities in the thin-oxide films and; **2**) the direct-tunneling-current through these films. We discuss these two effects together here because approximately the same minimum-oxide-thickness limit is set by either of them.

In 1996, Hu predicted what the minimum-oxide-thicknesses would be in production ICs, depending on the power-supply voltage.[11] He based these values on the following assumptions: First, the oxides will be used in ICs designed to operate for at least 10 years. Second, the time-to-breakdown (t_{BD}) that oxides of various thicknesses will exhibit can be extrapolated to the 10-year limit by using the anode-hole-injection (AHI) model discussed in Sect. 3.3.4. Figure 3-36 shows a plot of such t_{BD} data for oxides of various thicknesses and intrinsic failure behavior (i.e., the oxides depicted in this plot are assumed to be defect-free, and thus fail according to intrinsic-breakdown failure mechanisms). For such defect-free oxide films, the following thicknesses could be expected to exhibit a 10-year time-to-breakdown behavior for respective power supply voltages: **a**) 80-Å for 5.5 V (5 V power supply + 10%); **b**) 45-Å for 3.6 v (3.3 V + 10%); **c**) 33-Å (3.3-nm) for 2.75 V (2.5 V + 10%).

To allow for defects in the oxide that would weaken them (i.e., the B-mode defects, which locally thin, but do not create catastrophic pinholes in the oxide), Hu suggested that a safety margin be employed. That is, he used a 30% increase

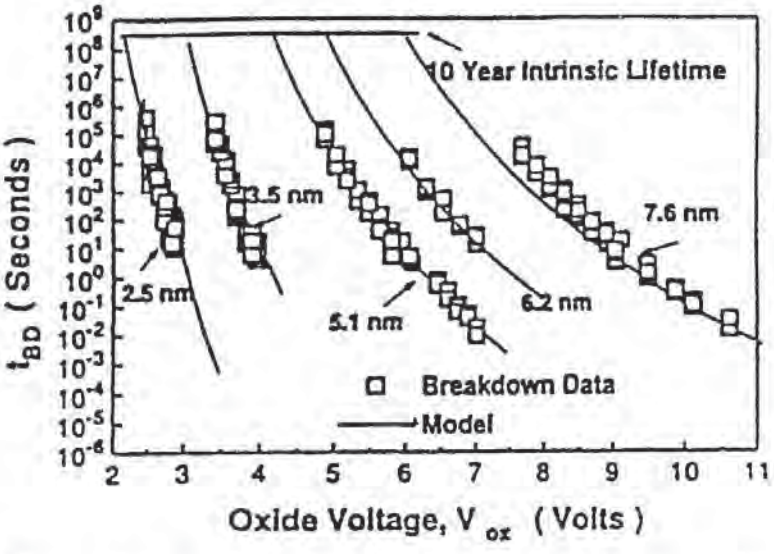


Fig. 3-36 Oxide lifetime as described the anode-hole-injection model.[11]

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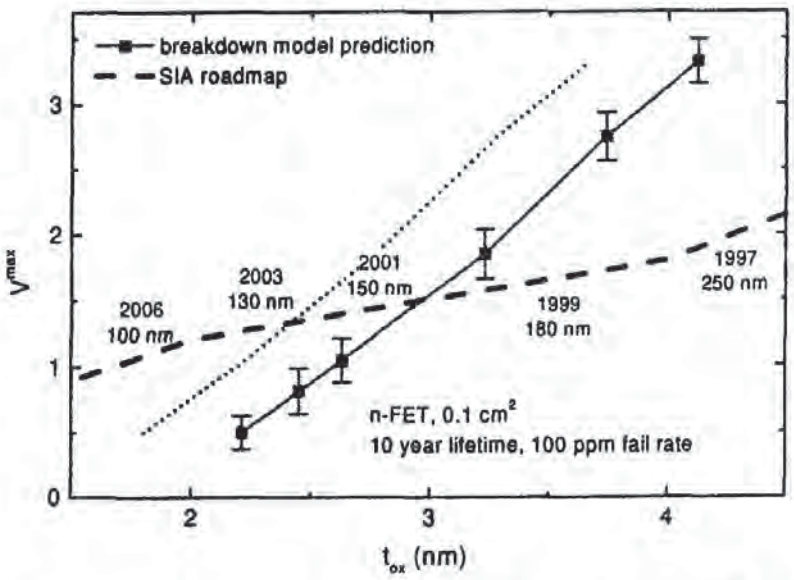


Fig. 3-37 The largest allowable supply (gate) voltage, V^{max}, as a function of oxide thickness, consistent with a failure rate of 100-ppm for a total gate area of 10 cm^2 on a chip operating at room temperature for 10 years. Solid and dotted curves correspond to t_{ox} measured by CV-extrapolation or quantum mechanical methods, respectively. The heavy dashed line is the SIA Roadmap (1997 version) for t_{ox} and V_{DD}, corresponding to the indicated year of first manufacture and technology generation.[37]

in the oxide thickness to allow for such defects. Thus, the minimum oxide thicknesses that he predicted that could be used in production were: a) 110Å for 5 V; b) 65Å for 3.3 V; and c) 45Å for 2.5 V.

Since that time, however, MOSFET scaling has been projected to even smaller gate lengths, mandating the use of even thinner gate-oxides (and smaller power-supply voltages). That is, projections for MOSFETs scaled to 50-nm (and using oxides below 2.0-nm) have been subsequently published. In 1998, Stathis and Di Maria of IBM published a study in which they projected the minimum oxide thickness that could be used in production was 2.6-nm for a 1.0-V power supply in order to meet the 10-year operating lifetime.[37] This was based on the conclusion that intrinsic oxide-degradation and breakdown would become the most significant reliability concerns, and therefore the dominant limiting factors that would set the allowable oxide thickness. Figure 3-37 shows the graph reported in that study, indicating that at 1.0 V, the minimum oxide thickness to meet a 10-year lifetime would be about 2.6-nm. This plot also implies that a 2.2-nm-thick gate oxide would no longer meet the ITRS Roadmap requirements.

In 1999, however, another study by Weir *et al.*, of Bell Labs (Lucent Technologies) indicated that if the oxide uniformity could be significantly imp-

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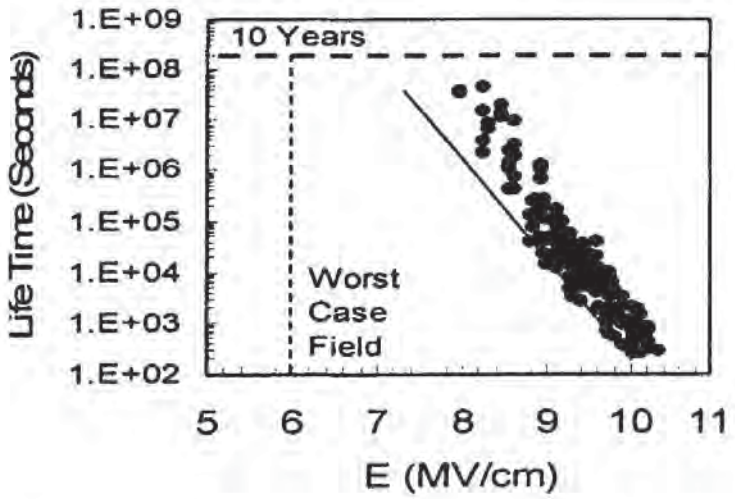


Fig. 3-38 TDDB data for 2.0-n- thick oxides at 125°C from MOS-capacitor data.[79]

roved, the reliability projections of an oxide at a given thickness can also be increased. That implies that thinner oxide films than were projected by Stathis and Di Maria may be possible. In fact, Weir showed that oxides with a thickness of 1.6-nm could meet the 10-year operating lifetime goal with a power-supply of 1.2 V - if they were produced with a process that allowed the film-thickness-uniformity to be increased.

In 1999, a 100-nm CMOS-technology that uses an oxide with a thickness of 2.0-nm and a power-supply voltage of 1.5 V was reported by Intel.[79] Figure 3-38 indicates that this oxide is able to meet the 10-year operating lifetime. In 2000, another report by the same group indicated it could fabricate 130-nm CMOS ICs with a gate oxide that was 1.5-nm-thick and with a 1.3-V power supply. These recent results appear to exceed the predictions of the minimum gate oxide thicknesses made just 2 years ago. At this point (circa 2002), the limit of oxide scaling does not yet seem to have reached.

The tunneling gate-leakage-current is another factor that has been predicted to put a limit on the minimum-oxide-thickness that can be used. In Sect. 3.4.2 we mentioned that at oxide thicknesses below 1.4-nm, the tunneling-leakage-current would become excessive.* This about the same thickness of oxide that has been reported to be used in the most advanced CMOS processes by 2000. Thus, both gate oxide reliability and excessive gating tunneling currents both limit the gate

* At some point this leakage will grow to be too large. That is, for SiO_2 at a gate-bias of ~1 V, the leakage-current changes from $1x10^{-12}$ A/cm^2 at 35-Å, to 1x10 A/cm^2 at ~15-Å (see also Fig. 3-21). This represents a change of *twelve orders of magnitude* in leakage-current for an oxide-thickness-change of little more than a factor of 2!

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oxide thickness at about the same value. (Although, it has been reported that even high levels of tunneling current do not seem to affect device reliability.[87])

3.8.2 Minimum-Oxide-Thickness Due to Stress-Induced Leakage-Current (SILC)

When thin oxides are exposed to high electric-field-stress (and consequently Fowler-Nordheim gate current), it causes them to subsequently exhibit low-field leakage. This effect, termed *stress-induced leakage current* (SILC), was first reported in 1987 (Fig. 3-39).[80] Apparently, such high-field stress generates neutral oxide-traps that facilitate electron tunneling. In addition, SILC is a transient phenomenon in thicker oxides, but is a continuous current in thinner oxides.[81,82] That is, in thicker oxides the SILC is observed to decay as traps are filled without significant tunneling out of traps. In thinner oxides, a steady-state current flows when there is an equilibrium between trap-filling and -emptying processes.[83]

The SILC is a particular problem for non-volatile memory devices because such oxide leakage reduces data retentivity. As shown in Fig. 3-40, it also tends to increase under the high-field program/erase cycles that the tunnel-oxides of such devices experience. The leakage makes nonvolatile-memory tunneling-oxide scaling much below 8-nm difficult (and perhaps impossible), unless the 10-year retention requirement is relaxed.

3.8.3 Soft-Breakdown in Thin Gate Oxides

In Sect. 3.3 we described how oxide films undergo sudden, catastrophic breakdown in which the I-V characteristic becomes essentially ohmic after being

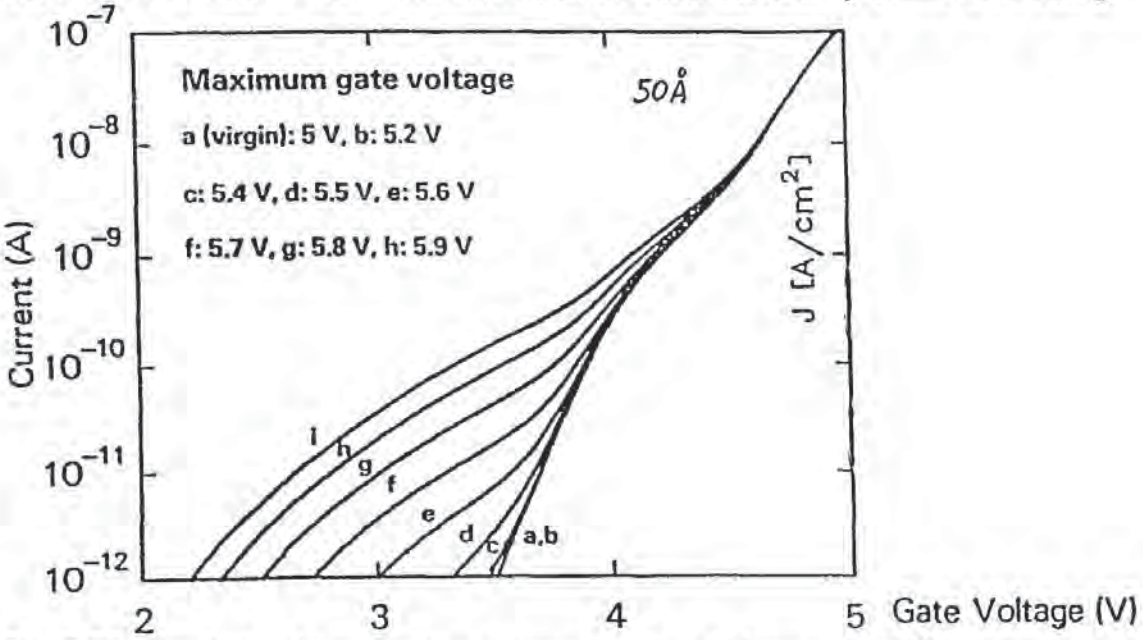


Fig. 3-39 Stress-induced (gate) leakage current (SILC) in 50Å gate oxides.[80]

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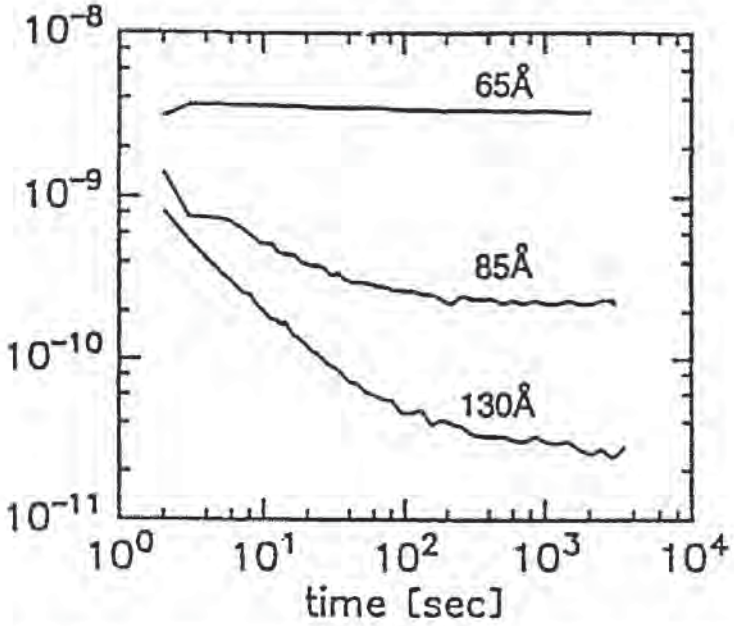


Fig. 3-40 Stress-induced leakage current is a transient current in thicker oxides but is a continuous current in thinner oxides, preventing nonvolatile memory scaling.[81]

subjected to sufficient electrical stress. However, for oxide films thinner than 5.0-nm, the breakdown mechanism may be fundamentally different. That is, another "anomalous" breakdown mode, termed *soft breakdown* or *quasi-breakdown,* occurs. Soft breakdown is detected by a much smaller change of voltage or current during stress, and a post-breakdown I-V characteristic that is given by a power law. In fact, while hard breakdown dominates for thicker oxides, it is often not observed in thin gate oxides. Instead, thin oxides appear to undergo soft breakdown. Also, soft breakdown is exhibited when oxides are stressed using lower and more realistic voltages or current densities. Soft break-down becomes "softer" and even less abrupt as the stress and oxide thickness is decreased.[90]

Figure 3-41a shows how the gate current in MOSFETs with thin (2.5-nm) oxides changes with time during voltage stressing (V_G = 4.1V and T = 140°C). Two breakdown regimes are observed: **1**) soft breakdown - where the current rises suddenly to an intermediate level of ~10^{-4} A in some devices, and **2**) hard breakdown – where the current rises suddenly to about 10^{-2} A. The I-V curves of a pre-breakdown oxide (before), and a post-breakdown oxide (after) are shown in Fig. 3-41b. In fact, when the thin oxide is first stressed with excess voltage, it undergoes SILC. However, further stress beyond a critical oxide-field-value causes the SILC to transition to soft breakdown. That is, soft breakdown is observed to be triggered once the oxide electric-field exceeds 10.7-11.0-MV/cm.[91]

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After the oxide has undergone soft breakdown, the gate voltage becomes noisy (Fig. 3-42), but the threshold voltage V_T and transconductance g_m do not change significantly (as observed in MOSFETs with an oxide thickness of 2.5-nm). While MOSFETs with thicker oxides (5.5-nm-thick) undergo hard breakdown, their V_T and g_m also undergo little change. However, the current through the gate becomes so large that the transistor characteristics are distorted (making the MOSFETs that undergo hard breakdown unusable). Nevertheless, the only measurable effect on MOSFETs after soft breakdown is an increase in noise level in the gate voltage signal. While such noise fluctuations can couple into the drain current, for many applications this effect will not prevent MOSFETs from functioning properly. This suggests the possibility of a low-voltage technology which does not have gate-oxide breakdown as a failure mode.[90]

A later report, however, indicated that the soft breakdown mode in MOSFETs with channel lengths smaller than 1.0-μm is not observed. That is, such small MOSFETs undergo hard-breakdown.and immediate device failure.[92] Thus, being able to operate deep-submicron MOSFETs in a mode in which gate oxides do not undergo hard breakdown is not a likely scenario. This same study also demonstrated that hard- and soft-breakdown events are triggered by the same type of defect paths. The impact of soft breakdown on the reliability of ICs fabricated with deep-submicron MOSFETs is still being actively examined.

3.8.4 Impact of Polysilicon Depletion

Polysilicon depletion becomes a significant effect in MOSFETs when gate

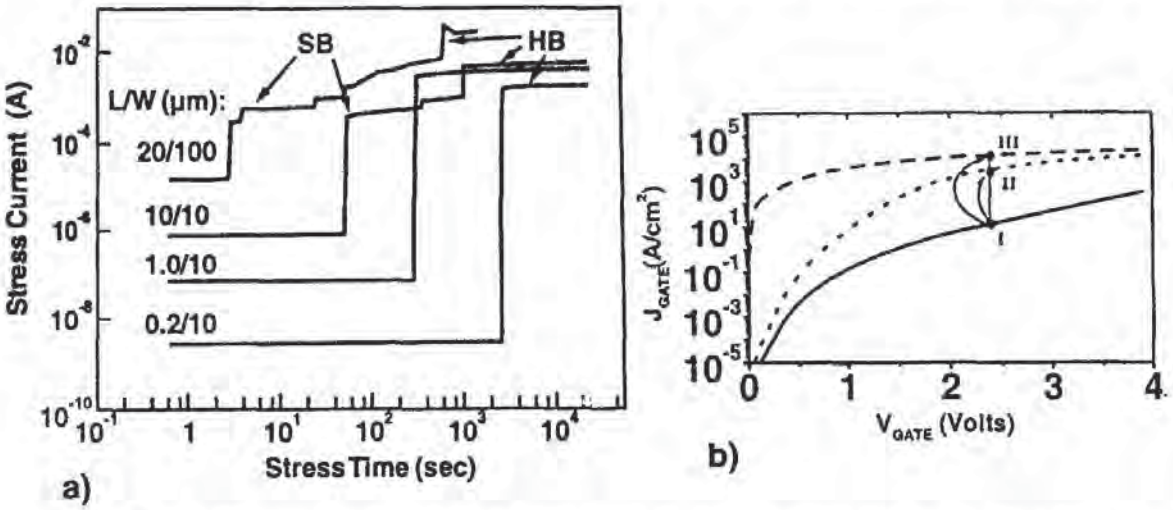


Fig. 3-41 a) Observed soft and hard breakdown in stress current curves vs. time for t_{ox} = 2.5-nm with V_G = 4.1 V at 140°C. [93] b) Oxide I-V characteristics before and after soft-breakdown.[94] (Pre-breakdown – solid line; Post-soft (short-dash); Post-hard (long-dash).

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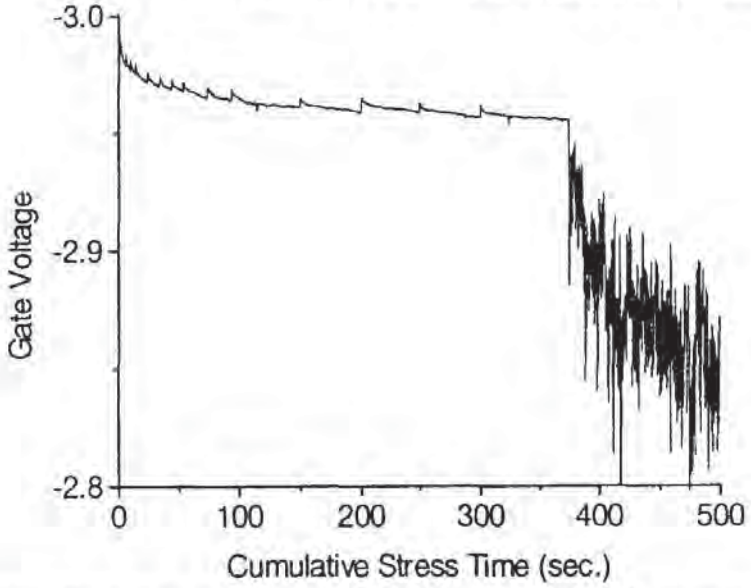


Fig. 3-42 Gate voltage measured during sequential −10 mA/cm^2 constant-current stresses of a 2.0-nm gate oxide. Soft breakdown occurs after about 360 seconds. Spikes are visible in the pre-breakdown trace because the stress was removed periodically.[90]

lengths are scaled below 0.25-μm. However, while the effect is widely discussed as being a problem, its physical basis on a fundamental level has not been carefully addressed in most texts. Thus, it is useful to explain the origin of this effect before describing its ramifications on the characteristics of deep-submicron MOSFETs.

While the polysilicon-depletion-effect has recently become a topic of attention in the technical literature, in truth it is an effect that *always* exists when a MOS-C (or MOSFET) is biased into depletion or inversion. Although the polysilicon-depletion-effect always occurs under such biasing conditions, it can be ignored by treating the polysilicon gate layer as being an ideal, equipotential region. In fact, this idealized perspective is *merely an approximation, that can only be invoked as long as doing so has insignificant effects on the device behavior.* Once the effect becomes significant, this idealization must be removed. (Note that most book authors are probably oblivious to the fact that this approximation is even invoked, as the correct energy-band diagram is only mentioned in one or two of the dozens of device physics texts that purport to treat MOSFETs.)

Let us consider an MOS-C which has an n^+-doped polysilicon gate and a p-doped silicon substrate. When a positive bias is applied between the gate and substrate, this causes depletion or depletion/inversion in the silicon substrate (depending on the bias voltage), and the charges induced in the silicon substrate by this biasing are *negative*. In any case, an equivalent *positive* charge must exist

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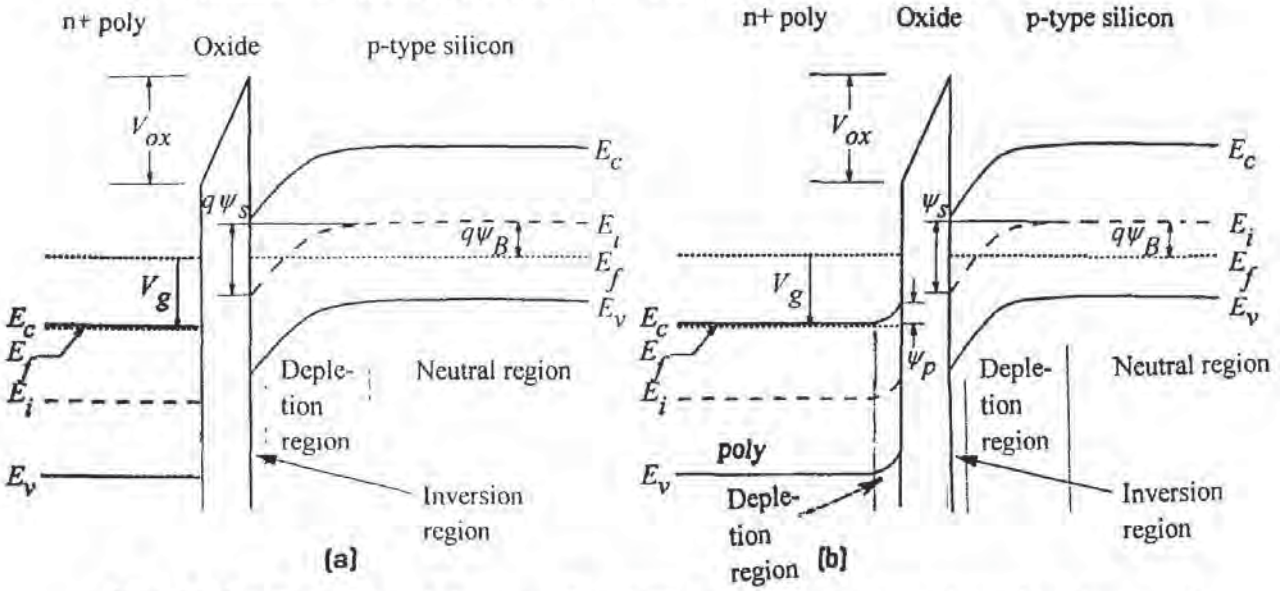


Fig. 3-43 a) Energy-band diagram of an NMOS-C biased to inversion which ignores the depletion-region formed in the polysilicon gate; b) Energy-band diagram of an NMOS-C biased to inversion showing the polysilicon depletion-region that actually always forms.

on the gate (polysilicon electrode). Donor ions in the n^+-doped poly constitute this positive charge (i.e., some of the mobile, negatively charged electrons leave the poly gate when a positive bias is applied to it). In other words, the biasing causes a *depletion region* of some finite thickness to be formed in the poly gate (at the poly/oxide interface). This depletion region in the poly is the basis of the *polysilicon-depletion-effect* (*PDE*). While most energy-band diagrams depict the situation of a MOS-C under depletion (or inversion) as in Fig. 3-43a, this is not strictly correct. That is, this diagram ignores the polysilicon depletion-region. The more correct energy-band-diagram is shown in Fig. 3-43b. Here, the presence of the poly depletion-region is indicated by band-bending (which implies the presence of an electric field) in the poly gate near the oxide.

The existence of an electric field means that a voltage-drop exists across the polysilicon depletion-region (which represents some fraction of the applied gate voltage). This means that the remaining voltage (i.e., the sum of the voltage across the gate oxide and the silicon substrate) is smaller than if no voltage was dropped across the poly depletion-region. The reduced remaining voltage will induce a smaller inversion-layer charge-density than if there was no voltage dropped across the polysilicon depletion-layer. (The effect is the same as if the gate oxide thickness was increased; i.e., PDE increases the "equivalent oxide thickness" $t_{ox_{eq}}$ – see Chap. 4, Sect 4.1). The decreased inversion-layer charge-density results in a degradation of the drain-current I_D of the MOSFET.

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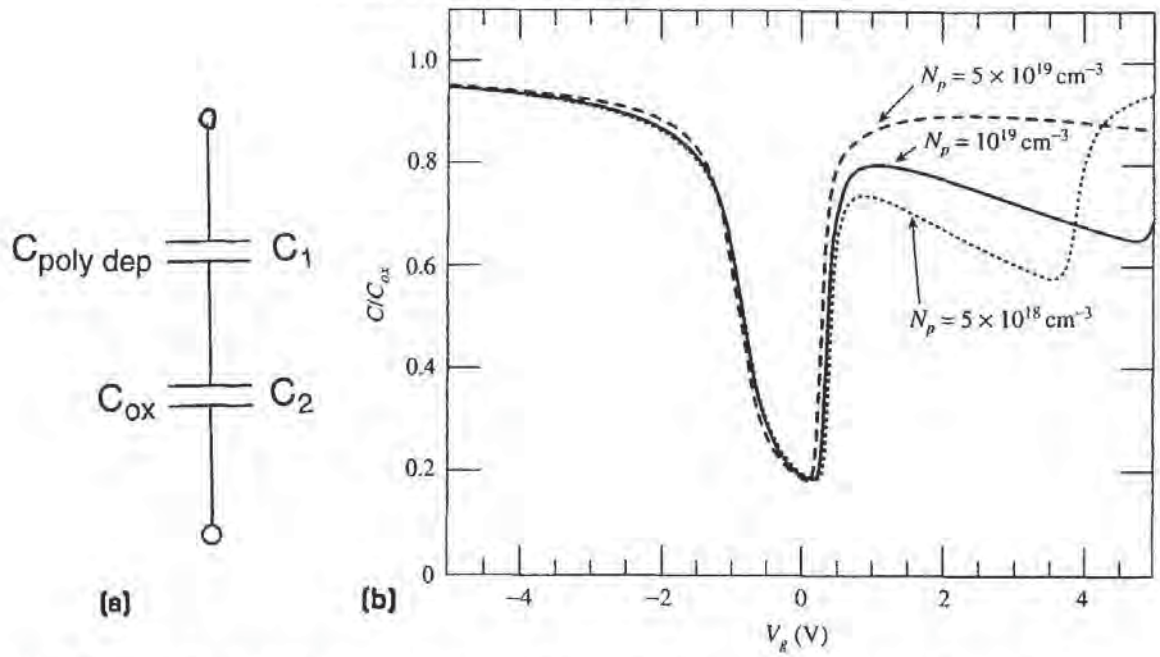


Fig. 3-44 a) Equivalent-circuit diagram of the polysilicon depletion-capacitance in series with the gate-oxide-capacitance. b) Low-frequency C-V curves of *p*-type MOS capacitor with an n^+-polysilicon gate doped at several different concentrations.[96]

The polysilicon-depletion-effect (PDE) becomes more significant as device scaling continues because the oxide capacitance increases as the oxide is made thinner, but the capacitance due to the polysilicon-depletion-layer remains constant (assuming there is no increase in the poly doping). At some point (i.e., at about when the gate-oxide thickness is scaled below 10.0-nm and the gate voltages are 2.5-V [or lower]), the depletion effect starts to adversely impact the device performance of MOSFETs made with polysilicon gates to a significant degree. We will now explain quantitatively why this is so.

The depletion-capacitance due to the PD-region is in series with the gate-oxide-capacitance (and the silicon-substrate depletion-region-capacitance, as well). An equivalent circuit diagram of the poly-depletion-capacitance in series with the gate-oxide-capacitance is shown in Fig. 3-44a.* The total capacitance of two capacitors in series is given by:

$$1/C_{tot} = (1/C_1) + (1/C_2) \qquad \textbf{(3.11)}$$

Thus, the smaller capacitor largely determines the total capacitance value. For the

* Note that although no capacitor electrodes physically exist at the poly/SiO_2 interface, such "virtual" electrodes are shown in Fig. 3-44a. This is nevertheless a valid equivalent-circuit representation because the two "virtual" electrodes each have the same amount of charge (although of opposite polarity). Thus, the effect of one cancels that of the other.

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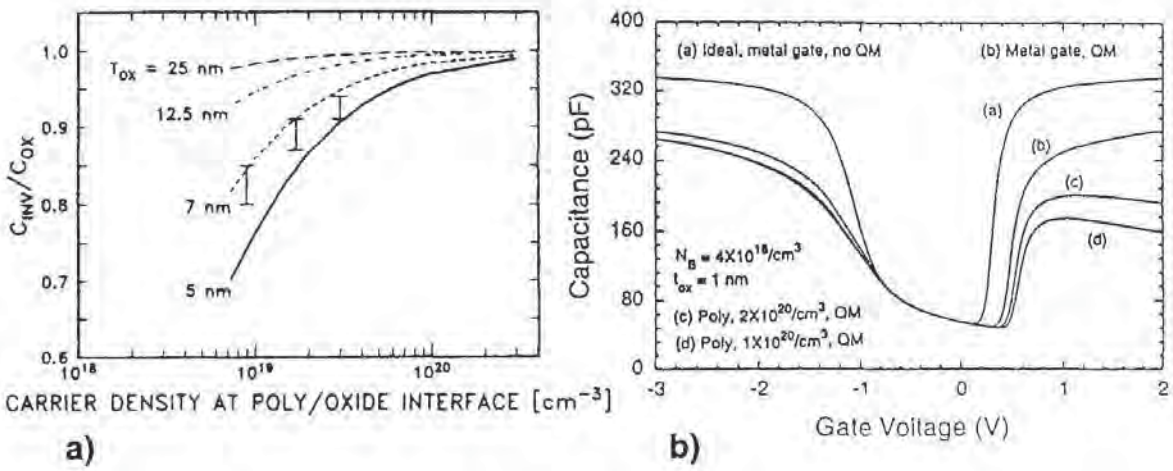


Fig. 3-45 a) Theoretical plot of C_{inv}/C_{ox} as a function of carrier concentration at the polysilicon/oxide interface for different gate oxide thickness.[101] b) Theoretical C-V curves for a thin gate oxide (1-nm-thick) including quantum mechanical effects and polysilicon depletion.[96]

case of the polysilicon-depletion-capacitance and the gate-oxide-capacitance, the gate-oxide-capacitance is much smaller than the polysilicon-depletion-capacitance until the oxide thickness gets below about 10.0-nm. For such thin oxides (assuming the poly layers doping remains constant), the oxide-capacitance starts to get large enough that the poly-depletion-capacitance can begin impacting the total capacitance. This is also shown in Fig. 3-44b in which the low-frequency C-V curves are shown for an MOS capacitor (with a 7-nm gate oxide, a *p*-substrate, and an n^+-poly gate with several doping concentrations).[86] It can be seen that the total capacitance at inversion (C_{inv}) does not return to the full oxide capacitance (i.e., the total capacitance in inversion is reduced by the PDE). The degree of reduction in C_{inv} depends on the poly doping concentration (Fig. 3-45a). This is because the higher the doping concentration, the narrower is the PD region, and thus the smaller is effect of PD. For the 7-nm gate-oxide thickness used in Fig. 3-44b, the poly-depletion effect becomes negligible only when the poly doping reaches about $1x10^{20}/cm^3$ (C_{inv} ~.98C_{ox}, see Fig. 3.45a).

As the oxide thickness gets smaller, the problem gets worse.[95] Figure 3-45b depicts computer simulated C-V curves for an MOS-C with a 1-nm-thick oxide, and an n^+-poly on a *p*-type substrate having a doping density of $4x10^{18}/cm^3$ (to allow for a V_T of several tenths of a volt). Curve a) is the C-V curve for an ideal (infinite conductivity) gate material, ignoring quantum effects. Curve b) is for a metal gate but including quantum effects. Curves c) and d) are for n^+-poly gates

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doped to $2x10^{20}/cm^3$ and $1x10^{20}/cm^3$, respectively, and including quantum effects. Curves c) and d) illustrate the effects of finite polysilicon doping.[96]

The above discussions indicate that if the polysilicon doping density could be increased without limit, the polysilicon depletion effect could be minimized. However, it appears that it will be very difficult to get electrically active doping densities above $10^{20}/cm^3$ for *n*-type polysilicon and above the mid- to upper-$10^{19}/cm^3$ for *p*-type polysilicon. This will result in reductions in drive-current capability that might not be acceptable.

To summarize, the impact of polysilicon-depletion on the minimum-oxide-thickness is the following: As the oxide is made thinner, the capacitance of the MOS gate structure is more impacted by the polysilicon-depletion-layer capacitance (assuming the doping in the poly remains constant). The effect is to reduce the total MOS-gate-capacitance to a lower value than if there was no poly depletion-layer-capacitance. For the same gate voltage, the potential at the Si surface is thus reduced, which in turn decreases the inversion-layer charge-density. Thus, the drain current actually decreases as the oxide is made thinner, causing the speed of the circuits made with such MOSFETs to decrease. Figure 3-46 shows how the propagation-delay in a ring oscillator increases with decreasing oxide thickness due to this effect.[84] This implies that it may not be appropriate to use the thinnest oxide thickness that is allowed by the 5-MV/cm breakdown limit.

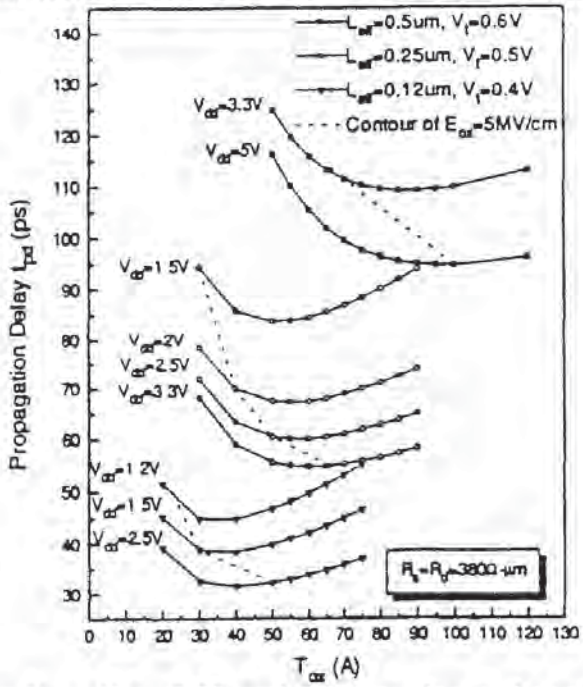


Fig. 3-46 At low V_{DD} (e.g., 2 V) and 0.2- μm, due to the polysilicon-depletion-effect, optimum speed may require a thicker t_{ox} than that allowed by the 5-MV/cm limit.[84]

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3.8.5 Impact of Process Induced Damage

In 1996, Hu suggested that process -induced damage would have less impact on gate-oxide-reliability as oxides less than 10-nm in thickness were used.[78] That is, oxides that were 6.4-nm-thick showed an order of magnitude smaller interface-trap-density than did oxides that were 11.6-nm-thick (Fig. 3-47). A model that sought to explain this effect treats plasma charging-current as a constant-current-source, rather than a fixed voltage-source. Thus, for the same plasma process conditions, the same amount of current will pass through oxides as they are scaled below 10-nm, regardless of their thickness. In addition, the thinner oxide (e.g., 6.4-nm) is more tolerant of the same current stress than the thicker oxide (11.6-nm-thick). This data led Hu to conclude that plasma-process damage would not become a more serious issue with oxide scaling below 5-nm.

However, more recent information was not as optimistic. In 2000, at the 5th International Symposium on Plasma Process-Induced Damage, P.W. Mason of Lucent Technologies reported that plasma damage did, in fact, increase as the gate oxide thickness was decreased from 11.5-nm to 5.5-nm. The main damage source was the rf-backsputter via-clean process used to prepare vias for metal deposition. The plasma damage was found to correlate with long-term oxide reliability degradation, although not with short-term reliability problems. Another report from K.P. Cheung of Lucent at the same conference indicated that currently available measurement techniques cannot determine whether or not a low-level of plasma-induced damage is occurring.

The fact that plasma-induced damage in gate oxides may still remain a relia-

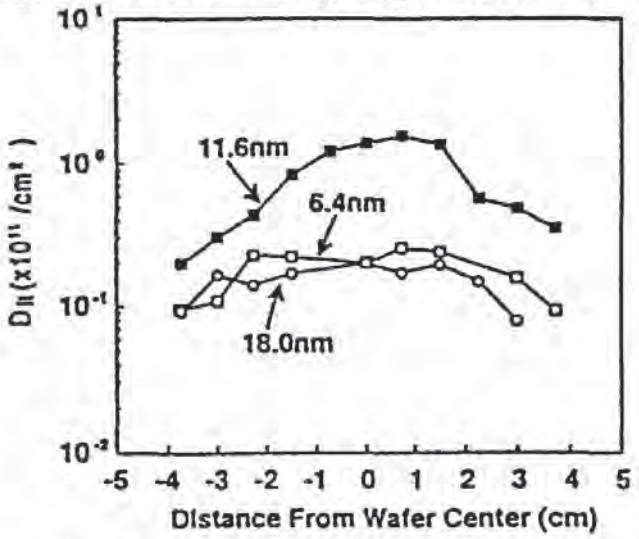


Fig. 3-47 Plasma-process-antenna-effect actually causes less damage to 6.4-nm oxides than to 11.6-nm oxides.[11]

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bility problem, has led work to continue on ways to limit such damage. In July 2000 it was reported that using 3.0-nm-thick oxides nitrided in N_2O produced CMOS transistors which showed significantly improved resistance to charging damage, especially for PMOS devices.[85]

3.9 MEASURING ULTRA-THIN GATE OXIDES

Ultra-thin oxide films can be measured in a number of ways, as described in detail in Ref. 98. Two of the more common methods are *ellipsometry* and *high-resolution transmission electron microscopy* (HRTEM). Ellipsometry is a powerful and accurate optical method. The technique uses plane-polarized monochromatic light to illuminate the oxidized silicon surface at an angle. (The name *ellipsometer* comes from the use of elliptically polarized light to measure film properties.) An elliptically polarized laser beam is directed at the Si surface at an angle, and is then reflected from both the silicon substrate and oxide surface (Fig. 3-48). The technique makes use of the change of state of polarization when light is reflected from a surface. If the index of refraction (n_i) and the extinction coefficient (κ) of the substrate are known, and if the film is non-absorptive at the wavelength being used (so it's $\kappa = 0$), the state of polarization of the reflected beam then depends only on the thickness of the transparent film (and n_i).

The reflected beam passes through an analyzer drum and onto a detector. The analyzer drum is rotated to produce a minimum value in the light intensity reaching the photodetector. By reading the polarizer and analyzer settings, the

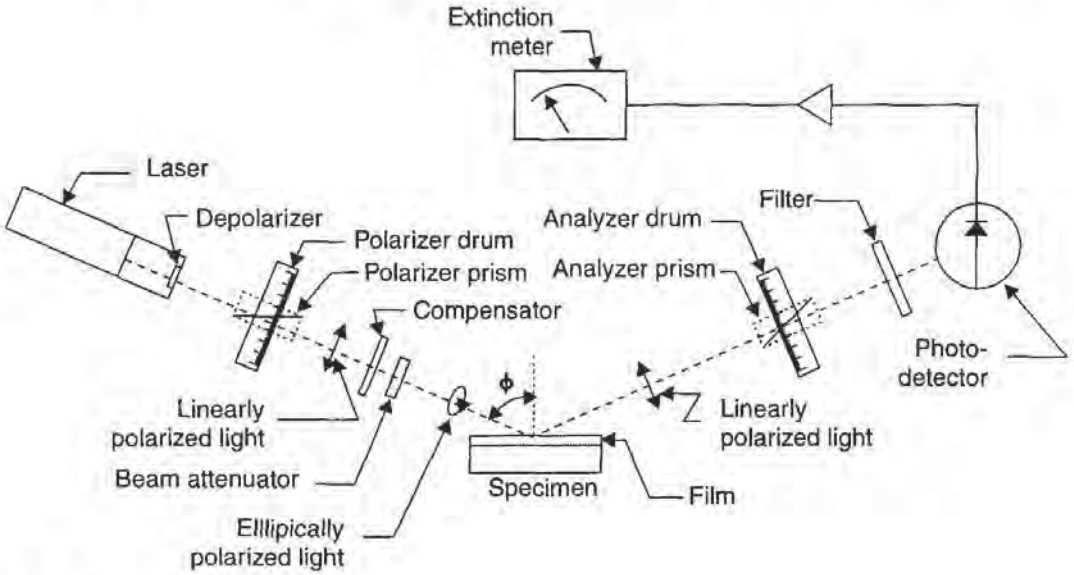


Fig. 3-48 Schematic of an ellipsometer.

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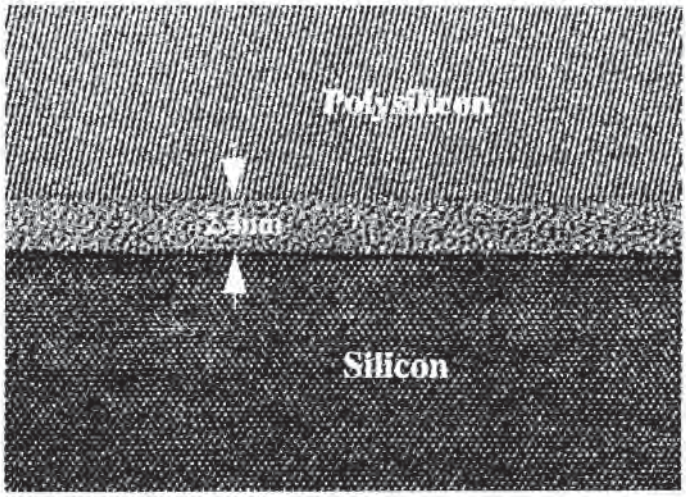


Fig. 3-49 HRTEM of 2.4 nm-thick oxide.[90] (© 1997 IEEE)

film thickness and index of refraction can be determined. The direct outputs of an ellipsometric measurement are the angles ϕ and ψ, which are related to the refractive index of the silicon substrate, the refractive index of the silicon oxide, and the thickness of the film.

If a single reflectance angle is used, multiple film thicknesses can produce a null, and the user must thus start with some idea of the expected film thickness to select the correct value. However, if multiple angles are used, an unambiguous single thickness value can be obtained. In any case, ellipsometry can be used to measure oxide thicknesses down the very thin regime (< 50-Å). However, inaccuracies in this regime may be present. Therefore, more complicated methods, such as multiple-wavelength ellipsometry or multiple-angle ellipsometry may be used to improve the accuracy of these measurements.[97] One recently described technique for measuring ultra-thin oxides involves a modification to conventional ellipsometry. In this method, an oxide *under* a polysilicon gate film is measured with a multiple-wavelength, multiple-angle, laser ellipsometer (the Rudolph Technologies S200-*ultra*® model). This allows the thickness of oxides fabricated *in-situ* in the single-wafer cluster tools described in Sect. 3.8.6, to be determined.[99]

Thin-oxide film-thickness can also be measured from micrographs obtained by HRTEM (Fig. 3-49). Preparing a sample for HRTEM requires the tedious tasks of slicing the wafer, mounting the slice in epoxy, and mechanically polishing and ion milling it to the proper thickness. However, unlike other techniques, no physical values such as index-of-refraction or dielectric constant are needed.

As gate-oxides scale to the ultra-thin regime, issues associated with measuring these films becomes increasingly critical. A transition region is thought to exist between the crystalline-silicon and bulk-silicon-dioxide that extends from

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several angstroms up to about 10-Å from the silicon. For ultra-thin oxide films this could constitute 20-50% of the film. The structural differences in the transition region can change the properties of the film, including its refractive index, static dielectric constant, band gap, and effective mass. These property changes can effect many measurement techniques used to determine the oxide thickness. Thus, it is necessary to examine the extent to which this interlayer must be included in optical models to obtain the required measurement precision for ultra-thin oxide films. Surface roughness will also play a role since many of the measurements assume an atomically smooth transition between silicon ad silicon dioxide. Leakage and tunnel currents through the oxide will also affect many metrology aspects, including capacitance and conductance measurements.

The presence of contamination on the surface of the dielectrics to be measured is another complicating factor. Such airborne contaminants can form an ad-layer on the surface (see Sect. 3.10.1). Under these circumstances, the ellipsometric response will include the effect of the ad-layer. To eliminate these effects, it is necessary to develop a reproducible and easily implemented cleaning procedure. The analysis of ultra-thin stacked dielectrics consisting of individual layers of oxide and nitride may also be made more complex by parameter correlation effects.

3.10 MANUFACTURING ULTRA-THIN GATE OXIDES IN EARLY-2001

3.10.1 Process Control Issues of Growing Ultra-Thin Gate Oxides

In the 2001 timeframe, gate oxides were still largely being grown with batch processes that employ vertical furnaces. Details of such batch oxide-growth processes (and the tools used to carry them out) are found in Vol.1, 2nd Ed., Chap. 7. It has been demonstrated that these types of processes can grow oxide films as thin as 2.5-nm, and with a uniformity of ±0.5-Å across a 200-mm wafer.[100]

However, when oxide thicknesses have to be made even thinner (≤ 2.0-nm), it becomes very difficult to maintain this kind of control using such conventional processing methods (i.e., in which the gate oxide is grown in an oxidation furnace and the polysilicon gate electrode is subsequently deposited in a separate processing tool). In the time between gate-oxide-formation and polysilicon-deposition, the gate oxide is exposed to the fab environment, allowing adsorption of *molecular airborne contamination* (MACs – see also Chap. 6).[102] Such MACs have been shown to have a negative effect on gate-oxide integrity, and they are also known to cause the measured thickness of the gate oxide to increase over time. In traditional batch processing, wafers may be stored for hours (or even days) after the gate oxide is grown, before the poly gate electrode is deposited.

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Newer production methods thus form both the gate oxide and the polysilicon in the single vacuum environment of a cluster tool (with separate process chambers linked by an isolated vacuum robot that transfers wafers between chambers). This not only speeds the formation of the gate stack but also does not MACs the opportunity to become incorporated MACs between the two layers.[99]

3.10.2 Extending the Use of Ultra-Thin Silicon Dioxide Layers as Gate Dielectrics: Stacked Oxide Films Which Incorporate Nitrogen

As argued earlier, growing gate dielectrics with a thickness of < 2.0-nm in a manufacturing environment may not be possible, due to several limits: reliability; tunneling leakage-current; and boron penetration. However, work has continued to try and extend the use of oxides into this thickness regime. The main thrust in the 2001 timeframe for doing this involves the formation a dielectric *stack*, still mainly based on SiO_2. However, nitrogen is incorporated into the oxide such that it is present in several places: **1**) in a very-thin layer near the Si/SiO_2 interface at a concentration of < 1atom%; and **2**) in another very thin layer at the poly/SiO_2 interface, at a percentage of greater than 5 atom% (or, more commonly, in the form of a very thin SiON layer on top of the SiO_2 layer). To make such a gate-dielectric stack-structure effective, it is critical to be able to control the amount, position, and concentration-profile of the nitrogen throughout the stack.

Excess nitrogen in the bulk of the film may harm the oxide properties, and thus it is desirable that little (or none) exists in the bulk of the oxide. However, nitrogen at a concentration of < 1% close to the Si/SiO_2 interface has been found to be useful in strengthening the bottom Si/SiO_2 interface against hot-carrier degradation and interface-state generation, without degrading the electrical properties of the stack. On the other hand, a nitrogen concentration of at least 5 atom% is needed at the top oxide/poly interface to prevent boron penetration into the oxide bulk during subsequent high-temperature processing steps. Such boron penetration into the oxide (i.e., from the p^+-doped poly of deep-submicron PMOSFETs) has two detrimental effects: **1**) If not prevented from doing so, the boron can enter the Si substrate, causing unacceptable shifts in the V_T of the PMOSFETs; and **2**) If the boron does enter the oxide, but is prevented from entering the silicon substrate, it will nevertheless pile up in the oxide. Such boron-pileup in the oxide has been shown to degrade the oxide reliability, likely by causing defects that weaken the oxide structure.

Thermal oxidation with O_2, N_2O, and NO (as described in Sects. 3.7.1 and 3.7.2) can tailor the nitrogen profile such that reasonable control of the nitrogen density and profile at the Si/SiO_2 interface and within the bulk oxide can be

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maintained. However, it may not be possible to form a layer with enough nitrogen at the oxide/poly interface to prevent B penetration (i.e., > 5 atom% is needed) using thermal techniques in oxide films ≤ 2.0-nm thick. Instead, a low-temperature plasma-technique (e.g., using a remote nitrogen plasma) can be used to form a very-thin nitride film on the top oxide surface (actually a heavily-nitrided oxide-film is formed with this method).[103] Such thin SiON-layers may be enough not only to reduce or eliminate boron penetration, but also to increase the stacks permittivity. The result is that by adding an oxynitride film to the stack may cause an increase in its effective thickness of approximately 30%. This, in theory, may also make it possible to reduce the gate leakage-current. The nitride film formed by such a remote plasma nitridation process has also recently been shown to improve the reliability of the dielectric stack.[104] These improvements reportedly arise from reduced leakage and higher voltage acceleration factor.

3.10.3 Use of Ultra-Thin Oxide Layers Under High-*k* Gate-Dielectric Films

Even when it comes time to use high-*k* dielectrics in MOSFETs, an ultra-thin silicon oxide layer may still need to be formed on the silicon surface under the high-*k* dielectric film (to produce a reliable interface between the high-*k* material and silicon substrate). Such an SiO_2 layer would preserve the interface state characteristics and channel mobility. However, since the interfacial layer contributes to the equivalent oxide thickness, the oxide thickness will still have to be minimized the without compromising reliable interface properties. Thus, it seems that processing ultra-thin SiO_2 films may remain a part of silicon IC fabrication for yet a long time!

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Chapter 4

HIGH-*k* DIELECTRICS

For IC applications, high-*k* dielectrics are defined as those with a dielectric constant greater than that of silicon nitride (i.e., $> k = 7$). High-*k* dielectric materials are being investigated for use in three main IC applications: **1**) as a gate dielectric material to replace SiO_2 in advanced MOSFET structures; **2**) as a dielectric material in the capacitor structures of dynamic RAMS (DRAMs); and **3**) as a dielectric in the capacitor structure of non-volatile ferroelectric random access memories (FeRAMs). In this chapter we will primarily focus on the first two of these applications. That is, since FeRAMS are not yet a mainstream IC product, we will only give a brief description of high-*k* FeRAM structures.

There are currently a variety of materials with dielectric constants greater than that of SiO_2 being studied as such high-*k* replacement dielectrics. These include: silicon nitride (Si_3N_4); aluminum oxide (Al_2O_3), tantalum pentoxide (Ta_2O_5); zirconium oxide (ZrO_2); hafnium oxide (HfO_2), barium strontium titanate (BST), and lead-lanthanum-zirconium-titanate (PLZT - $PbLaTiO_3$). Table 4-1 lists the dielectric constant and bandgap of these materials.

4.1 HIGH-*k* DIELECTRICS AS THE GATE DIELECTRIC IN MOSFETS

Let us begin by describing the need for high-*k* dielectrics in the first of the above three applications, namely, as a gate dielectric in advanced MOSFET structures. Metal-oxide-semiconductor field-effect transistors (MOSFETs) have been continually scaled since they were first introduced in the early 1960s. The gate dielectric employed in all of these scaled generations has been silicon dioxide (SiO_2). As each generation was scaled, this gate oxide also had to be made progressively thinner. For the most advanced CMOS technologies being fabricated in 2001 (0.13-μm), the gate oxides had thicknesses of ~3.0-nm. According to the *International Technology Roadmap for Semiconductors - 1999* (ITRS-99),[1] when MOSFET devices used in CMOS are scaled to gate lengths below 0.1-μm (100-nm), they will require gate-oxide-equivalent thicknesses, $t_{oxeq} < 1.5$ nm. However, because direct tunneling increases exponentially with decreasing thickness, it may not be feasible to use SiO_2 films with thicknesses

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TABLE 4-1 IMPORTANT HIGH-*k* DIELECTRIC MATERIALS

	Dielectric Constant	Bandgap (eV)	Crystal Structure
PbLa $ZrTiO_3$	1000		
$BaSrTiO_3$	300		
Ta_2O_5	26	4.5	Orthorhombic
ZrO_2	25	7.8	Monoclinic
HfO_2	24	5.7	Monoclinic
Al_2O_3	9	8.7	Amorphous
Si_3N_4	7	5.1	Amorphous
SiO_2 (Reference)	3.9	8.9	Amorphous

smaller than 1.5 nm. Thus, it appears that SiO_2 may become unsuitable as the gate insulator in sub-100-nm MOSFETs if future device scaling requirements are to be met. Of course, process engineers will do everything possible to keep using SiO_2 for this role. This is because SiO_2 is compatible with silicon (and polysilicon) and is well behaved and well understood. Furthermore, it has also been used as the gate dielectric since the inception of MOSFET technology some 40 years ago. Finally, it has been widely predicted that the substitution of high-*k* dielectrics for SiO_2 as a gate dielectric will be markedly difficult due to intrinsic chemical bonding effects and difficult process integration challenges.[2] *Some have predicted that the greatest challenge to the continued scaling of the MOS transistor may be the replacement of SiO_2 with a high-k dielectric!*

In any case, when (and if) SiO_2 is replaced, the replacement material will have to be thicker than oxide to reduce the direct-tunneling current and yet maintain the same MOSFET drive-current capability. This can be achieved by using an insulator that has a higher dielectric constant ($\varepsilon_{high\text{-}k}$) than does oxide ($\varepsilon_{ox} = 3.9$). That is, it must be possible to achieve the same equivalent thickness as required for SiO_2, where the oxide equivalent thickness t_{oxeq}, is given by:

$$t_{oxeq} = t_{high\text{-}k}\,(\varepsilon_{ox}/\varepsilon_{high\text{-}k}) = t_{high\text{-}k}\,(3.9/\varepsilon_{high\text{-}k}) \qquad \textbf{(4.1)}$$

For example, a high-*k* gate insulator with a thickness $t_{high\text{-}k}$ = 10-nm and a dielectric constant ($\varepsilon_{high\text{-}k}$) of 20, will behave in the same way in a MOSFET as an SiO_2 layer with a thickness of ~2.0 nm (see also Fig. 4-1).

Of course, an interfacial layer of SiO_2 (or some other lower-*k* material) will limit the highest possible gate stack capacitance or, equivalently, the lowest achievable t_{oxeq} value. That is, when a gate-dielectric structure consists of a

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stack of several dielectric materials, the layer with the lowest-k value dominates the overall capacitance and also sets a limit on the minimum achievable t_{oxeq} value.

The capacitance of two dielectrics in series is given by:

$$1/C_{tot} = (1/C_1) + (1/C_2) \quad \textbf{(4.2)}$$

For example, a dielectric stack structure with an SiO_2 bottom layer and a top layer having a higher-k value, will thus have a t_{oxeq} that is calculated from:

$$t_{oxeq} = t_{SiO_2} + t_{high\text{-}k}\,(\varepsilon_{ox}/\varepsilon_{high\text{-}k}) \quad \textbf{(4.3)}$$

Since the minimum achievable t_{oxeq} value will never be less than that of the lower-k layer, a bilayer approach necessarily compromises the performance of the high-k dielectric film.

4.1.1 Integrating High-k Dielectrics into MOSFET Structures

The use of high-k dielectrics as the gate dielectric in submicron MOSFET structures also improves other device characteristics. First, as a MOSFET is scaled below about 0.3 microns, the threshold voltage V_T begins to decrease as the gate length is decreased (for a constant channel doping value and gate dielectric thickness). This is seen in Fig. 4-2a, where the effect of channel length reduction on the threshold voltage value is plotted for deep-submicron MOSFETs (i.e., gate lengths smaller than 1.0-μm) fabricated with gate dielectric films of

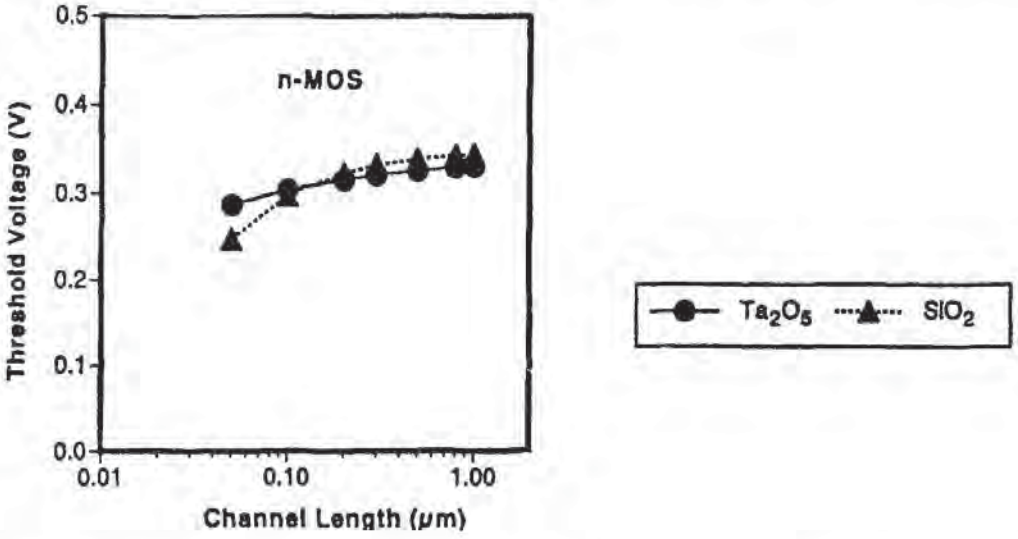


Fig. 4-1 As shown in this hypothetical transistor gate stack, a high-k material can be physically thicker yet provide an oxide-equivalent thickness that is electrically thinner (t_{oxeq} = 10 Å for both) than would be possible using oxynitride dielectrics.

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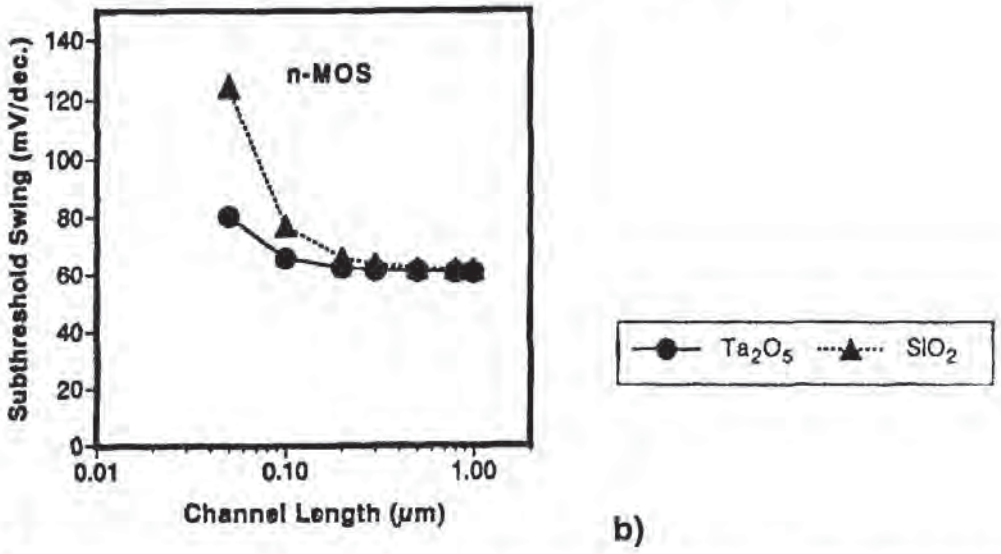


Fig. 4-2 a) The effect of channel-length-reduction on the threshold voltage V_T for deep-submicron MOSFETs fabricated with SiO_2 and Ta_2O_5 as the gate dielectric. The use of Ta_2O_5 reduces the V_T degradation with channel length scaling.[3] b) The effect of channel length reduction on the subthreshold swing S_t for deep submicron MOSFETs fabricated with SiO_2 and Ta_2O_5 as the gate dielectric. The use of Ta_2O_5 allows an improved S_t value with channel length scaling.[3]

SiO_2 and Ta_2O_5. This data shows that for a specific gate length (e.g., 0.1-μm), the change in V_T from that of a long channel MOSFET (e.g., with a length > 0.5 μm, in this example) is greater for MOSFETs built with a gate oxide than with a Ta_2O_5 gate dielectric.

The second improvement in device performance observed when a high-*k* gate dielectric is used involves the subthreshold-swing of a MOSFET, S_t. This is a measure of how effectively a MOSFET is turned off as the gate voltage is decreased below V_T (see Vol. 3 for more information on S_t). As shown in Fig. 4-2b, a value of 80 mV/decade can still be obtained for MOSFETs built with a high-*k* gate dielectric (e.g., Ta_2O_5). Note that S_t values smaller than 100 mV/decade are considered very good, and the smaller the S_t value the better. It has been shown that for a dielectric thickness of 5-nm, the optimum dielectric constant is 25, which corresponds to the *k*-value of Ta_2O_5.[3] For MOSFETs, there is a specific dielectric constant for a given dielectric thickness for which the circuit performance is optimum.

One of the drawbacks of using high-*k* dielectrics is that if they are deposited directly on Si they tend to have a high-level of interface states, D_{it}. The interface-state-density can be reduced by growing a thin layer of oxide (1-2 atomic layers) on the silicon to passivate the surface. We will describe this issue and other

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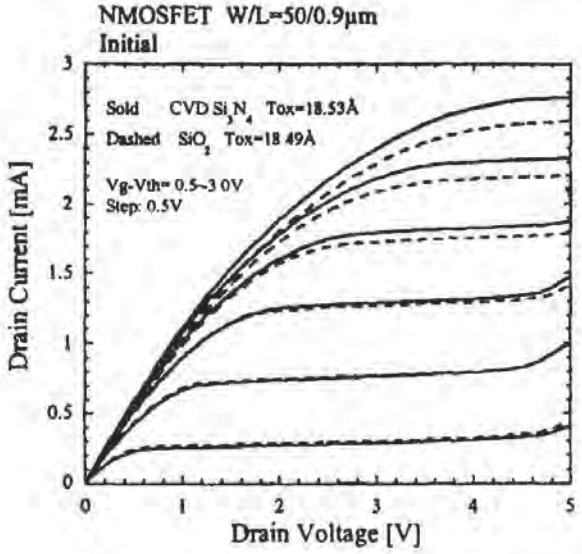


Fig. 4-3 The current-voltage (I_D-V_{DS}) characteristics of a 0.9 μm NMOSFET using Si_3N_4 and SiO_2 as the gate dielectrics.[4]

processing challenges related to the deposition and etching of various high-*k* films with respect to their suitability as alternatives to SiO_2 as a gate dielectric.

Note that initial results of using an alternative dielectric instead of SiO_2 in MOSFETs has produced some promising results, although none are clearly yet ready for full-scale IC production. Several examples of MOSFETs fabricated with alternative gate dielectrics have been reported. Figure 4-3 compares the current-voltage (I_D-V_{DS}) characteristics of a 0.9-μm NMOSFET using a 20-nm-thick Si_3N_4 gate dielectric to one using a 20-nm-thick SiO_2 gate dielectric. The device structure using the RTCVD-Si_3N_4 gate dielectric exhibits greater drain current.[4] A second MOSFET used a thermal-CVD process to deposit a Ta_2O_5 gate dielectric. The current-voltage characteristics of 150-nm MOS transistors using such a 4.0 nm-thick Ta_2O_5 film showed an improved drain current value compared to those fabricated with a gate oxide.[5] A third MOSFET used a Ta_2O_5/SiO_2 gate dielectric with a 2.8-nm equivalent-oxide thickness.[6] A fourth MOSFET used a gate dielectric stack consisting of $SiON/Ta_2O_5/TiN$.[7]

According to some researchers,[54] the ideal gate dielectric stack may end up having an interface consisting of a few atomic layers of Si-O (and possibly N), containing a pseudo-binary oxide. This oxide layer could preserve the critical high-quality characteristics of the SiO_2 interface while providing a higher-*k* value. Then a different, higher-*k* material could be used on top of this interfacial layer.

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4.2 HIGH-*k* DIELECTRICS AS THE CAPACITOR DIELECTRIC IN DRAMS

A DRAM capacitor is a stack of materials consisting of a dielectric sandwiched between two electrodes. Since the invention of the DRAM nearly 30 years ago, either SiO_2 with a dielectric constant (k) of 4, or SiN with $k = 7$, or a combination of these materials has been used as the capacitor dielectric. Polysilicon is used as both the bottom and top electrode. Structures containing these materials are therefore called *silicon-insulator-silicon capacitors* (SIS).

As progress is made to put more memory bits on a chip, the surface area of silicon available for each individual memory cell in a DRAM shrinks rapidly (Fig. 4-4). At the same time operating voltages have been falling from 5V a few years ago, to below 3V today (and probably to about a volt in a few years). However, the charge-storage-capacity for each cell remains at about 30 fF/cell (corresponding to about $1\text{-}2\text{x}10^6$ electrons/cell). There are three reasons that the amount of stored charge per cell has not been decreased. First, this charge-storage-capacity is needed to prevent the occurrence of soft errors. Soft errors are caused by alpha particles emitted from naturally occurring trace radioactive impurities in packaging materials or from cosmic rays. Such energetic particles generate minority carriers in the silicon, whose charge can alter memory states. By maintaining the capacitance-per-cell at about 30 fF/cell, the soft-error-rate (SER) can be kept acceptably low. Second, as DRAMs have evolved, the detection capability of the DRAM sense amplifiers has remained about the same. Thus, each cell still needs to have about the same charge-storage-capacity to enable the state of the cell to be read. Third, the data-retention time has remained constant, again requiring about the same charge-storage-capacity per cell.

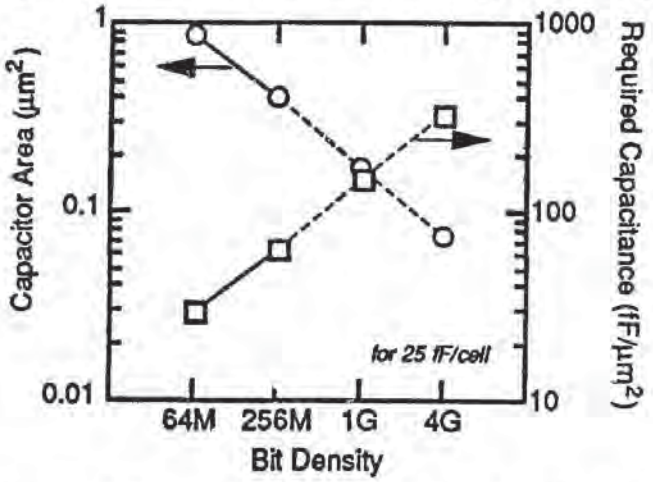


Fig. 4-4 Capacitor area and the required capacitance density as a function of DRAM bit density.[27] (© IEEE)

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Until recently, three approaches have been used to maintain this constant value of charge storage per cell. The first involves the use of three-dimensional structures to increase the cell surface area (such as trench capacitors and stacked capacitors). The second involves using ever-thinner layers of dielectric in the capacitor. The latter approach entails increasing the surface area of the capacitor by about a factor of 2x by roughening the surface of the polysilicon bottom electrode. This is achieved by growing the bottom-electrode polysilicon with larger grains, and the resulting films are called *hemispherical silicon grain* (HSG) or *rough-surface polysilicon* (RSP).

However, as the silicon area per cell has continued to decrease, the three-dimensional structures can no longer be scaled further to increase surface area. Thus, in the face of shrinking capacitor area and reduced capacitor voltage, even thinner layers of SiO_2 (or multilayers of *oxide/nitride/oxide* - ONO) have been implemented. Nevertheless, in ONO dielectrics, the minimum thickness is about 50-Å (5-nm). In thinner films, tunneling currents produce excessive leakage. However, the combination of such ONO films, together with HSG is currently used in 0.18-μm and 0.15-μm DRAM production.

But, as memory chips surpass about 256 MB this approach will no longer be adequate because unacceptably high values of leakage current occur. Furthermore, the storage capacitors suffer premature catastrophic breakdown, even with reduced operating voltages. Thus, by examining the capacitor equation, the only remaining option for increasing the capacitance per unit area is to incorporate a dielectric with a higher *k*-value. This enables use of a capacitor dielectric with a large enough thickness that low leakage and high operating reliability to be maintained - while still providing sufficient charge storage with a continuously shrinking plate area and storage voltage. By using such high-*k* dielectrics, the DRAM cell structures could also be significantly simplified.

When the list of high-*k* dielectric candidates for DRAM capacitors is examined one notes that Al_2O_3 (with a *k*-value of 9), does not provide a sufficient increase in *k* to maintain the required charge storage/cell. However, Ta_2O_5, with a *k*-value of 25 can meet the requirement for the next generation or two of DRAMs. The IC industry has had some experience with Ta_2O_5, and it can be deposited in a variety of ways, including CVD, metal-organic CVD, sputtering, and anodization. However, Ta_2O_5 does not provide a sufficiently large improvement in charge storage for the memory generations above 4 Gb that are expected to begin production within the next few years (~2006). The long-term solution appears to lie in the various ferroelectric or near-ferroelectric dielectric materials, such as the various combinations of barium and strontium

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with titanate (e.g., barium/strontium-titanate - BST), lead/zirconium-titanate (PZT), and other perovskite metal oxides. These types of materials exhibit *k*-values from a few hundred to several thousand, enabling them, in principle, to provide sufficient capacitance for DRAMs into the foreseeable future. Such ultra-high-*k* materials can be deposited using almost any method by which a thin film can be formed (and they come in a wide variety of compositions and morphologies). The dielectric constants tend to be a strong function the specific elemental ratios and crystal structures which, in turn, are a function of the deposition method. The selection of a particular dielectric material and the design of the DRAM cell depend on a number of complex factors, including the process simplification leading to cost reduction.

There are, however, several challenging process integration issues involving the use of high-*k* materials in DRAM capacitor structures. First, note that in DRAM capacitors the bottom capacitor electrode is the *storage node* and the top capacitor electrode is termed the *plate electrode* (Fig. 4-5). Doped-polysilicon has traditionally been the material used to form the bottom electrode of the DRAM capacitor, and either polysilicon or metal has been used to form the plate electrode. (As noted earlier, if polysilicon is used for both electrodes, the capacitor is a called a *silicon-insulator-silicon* capacitor [SIS]. If the top electrode is made of metal, the structure is called a *metal-insulator-silicon* capacitor [MIS].) In any case, polysilicon has been used to form at least one of the capacitor electrodes. However, polysilicon has the problem that it tends to form a

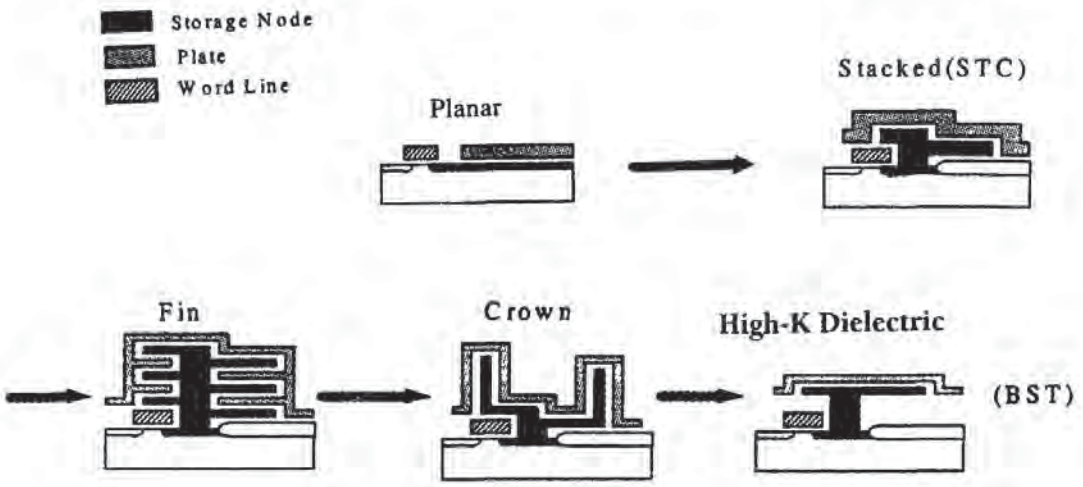


Fig. 4-5 The evolution of the capacitor-electrode structure in stacked-capacitor DRAMs.

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silicon oxide layer at the polysilicon/high-*k* interface, either as a native oxide, or during the processing steps used to form or anneal the high-*k* dielectric layer (or even during the subsequent chemical-vapor-deposition of interlevel dielectric layers). These interfacial SiO_2 layers cause an increase in the SiO_2-equivalent thickness of the overall capacitor dielectric layer (which, in turn, reduces the cell capacitance). As a result, a number of other bottom-electrode materials are being considered for the manufacture of cell capacitors, including aluminum (Al), iridium (Ir), platinum (Pt), ruthenium (Ru), tantalum nitride (TaN), titanium nitride (TiN) and tungsten (W). Note that if *both* the bottom and top electrodes of the DRAM capacitor are made of metal, the structure is called a *metal-insulator-metal capacitor* (MIM). Table 4-2 shows the requirements of DRAM capacitors as the DRAM size increases above 1Gb/chip.

The Platinum Group Metals (PGM) - Pt, Ir, and Ru - have been actively studied due to their low resistivity, chemical corrosion resistance, thermal stability, and diffusion barrier properties. Each, however, has unique problems with respect to serving as an electrode. For example, Pt has adhesion and etch residue problems, while Ru forms RuO_4 as a toxic by-product of the etch process (and Ru is also susceptible to pinholes and notching because of its ease of oxidation). We discuss these issues in more detail in later sections. Note that PVD and CVD are the most common deposition methods for these materials. Each has its advantages and disadvantages. CVD is capable of much better conformality at lower processing temperatures. However, obtaining high-purity precursors of the PGMs is a rather difficult process. PGM deposition by CVD also presents a significant challenge in the development of volatile precursors.

Cost is another significant factor. For example, to sputter deposit a 50-nm (500-Å) film of Pt onto a 200-mm wafer with a 40% deposition efficiency, the cost is roughly $1000 per wafer. At 20,000 wafer-starts per month, this cost is

TABLE 4-2 DRAM Stack Capacitor Films Technology Requirements

Year	1999	2002	2005	2008	2011	2014
Technology Node	180 nm	130 nm	100 nm	70 nm	50 nm	35 nm
DRAM Capacity	1 Gb	4 Gb	8 Gb	24 Gb	64 Gb	192 Gb
Capacitor Structure	Cylinder MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM
Capacitor Dielectric Material	Ta_2O_5	Ta_2O_5	BST	Epi-BST	???	???
Capacitor Dielectric Constant	22	50	250	700	1500	1500

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is significant. In CVD, only 20% of the precursor is deposited in the chamber, and roughly 80% of the precursor is exhausted as waste. After subsequent processing, on the order of only 1% of the original material remains on the finished wafer. The remaining deposited-99% is removed by plasma etch or chamber cleaning. For expensive metals, this remaining 99% must be reclaimed.[8] One report describes an MOCVD deposition process for Pt films.[9]

4.3 HIGH-*k* DIELECTRICS FOR FeRAM APPLICATONS

The use of high-*k* dielectric materials in non-volatile memory FeRAMs is an emerging area. Ferroelectric dielectrics such as *lead zirconium titanate* (PZT - whose *k* value is 1000-1500), or *strontium bismuth titanate* (SBT), have a perovskite structure and are unique in that this crystal structure retains its "memory" without power. That is, since ferroelectric polarization retention is nearly perpetual, refresh is not needed. The capacitor structure in FeRAMs controls read/write speeds, data-storage lifetime, device layout, and packing density. Figure 4-6 shows a cross-section of an FeRAM cell and an example of a process flow used to incorporate such a cell into a conventional IC structure.[25] The early FeRAM device (manufactured by Ramtron Corp.) is being used in game cartridges, where memory is maintained without the use of a battery. The challenges of implementing ferroelectric dielectrics in FeRAMs are similar to those encountered in integrating high-*k* dielectrics into DRAMs. These include: controlling the interfacial reactions between the dielectric and electrode materials; maintaining thermal stability of the electrodes of the capacitor; and developing plasma-etching processes that provide critical dimensions of the devices. A review of the current status of FeRAMs has recently been published.[25]

4.4 TANTALUM PENTOXIDE (Ta_2O_5)

Tantalum pentoxide, Ta_2O_5, has a *k*-value of 25 and the IC industry has been developing techniques for forming thin films of this material since the early 1980s. It can be deposited in various ways including: **1**) LPCVD; **2**) metalorganic CVD; **3**) sputtering of Ta films followed by oxidation; and **4**) anodic oxidation of deposited Ta films. For use as a high-*k* dielectric layer in DRAMs, the most common deposition method of Ta_2O_5 films is LPCVD. Vendors that supply CVD tools to deposit Ta_2O_5 include Lam Research and Applied Materials.

4.4.1 Tantalum Pentoxide as a DRAM Capacitor Dielectric

We will discuss the use of Ta_2O_5 as a DRAM capacitor dielectric first because it

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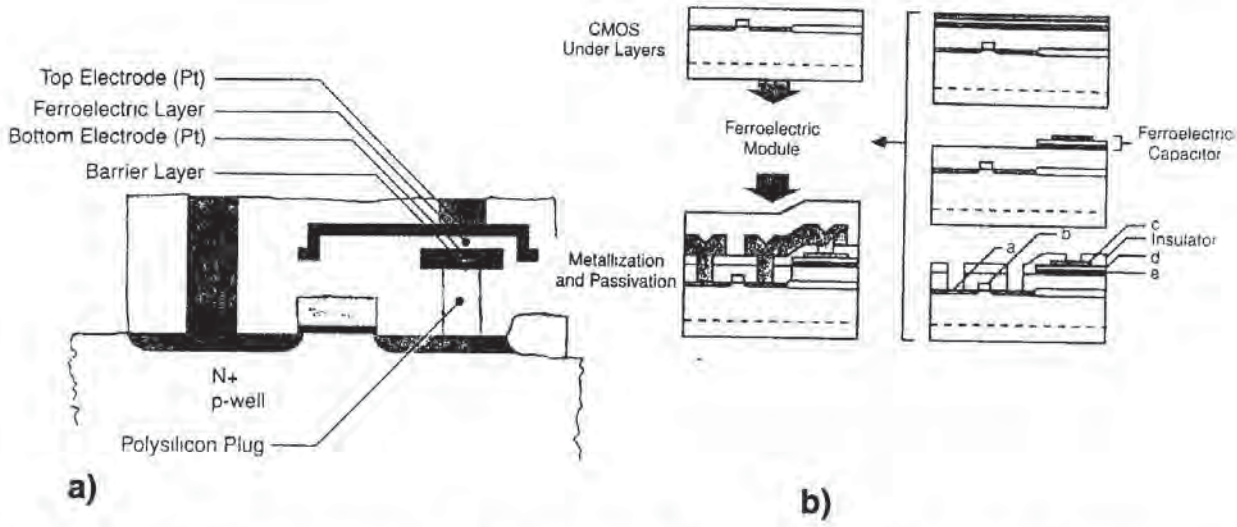


Fig. 4-6 a) The cross-section of a ferroelectric RAM cell (FRAM); and b) A typical FRAM process flow.[25]

is more likely to be implemented in this role than as a gate dielectric in MOSFETs. However, we will also discuss the application of Ta_2O_5 as a gate dielectric in the next section. The integration of Ta_2O_5 as a DRAM-capacitor-dielectric has been pursued because its *k*-value of 25 is high enough to result in adequately high charge-storage values per cell for DRAMs after the 256-Mb generation (i.e., perhaps for the 1-Gb and 4-Gb DRAM generations). In addition, Ta_2O_5 capacitors can simply replace ONO-based capacitors without major process integration problems. (The other change in the DRAM capacitor structure that accompanies the shift to a Ta_2O_5 dielectric is the replacement of the top plate polysilicon electrode with TiN – forming a TiN/Ta_2O_5/polysilicon structure [which is an MIS capacitor]). Here we describe the various processing issues associated with implementing Ta_2O_5 as a DRAM capacitor dielectric material. While Ta_2O_5 films exhibit many outstanding characteristics, their biggest drawback for DRAM applications is their relatively high leakage-current densities.

As noted above, the most common technique for forming Ta_2O_5 films for DRAM dielectrics is LPCVD.[10] Such films provide good step coverage. The film is formed by the oxygen-assisted thermal decomposition of an organometallic precursor in the presence of oxygen, typically tantalum ethylate (i.e., $Ta[OC_2H_5]_5 + O_2$), or tantalum tetraethoxy dimethylaminoethoxide (i.e. $Ta[OC_2H_5]_4[OCH_2CH_2N(CH_3)_2]$ TATDMAE and O_2) at 450°C, and at a

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pressure of 1-4 torr. Tantalum ethylate is also referred to as tantalum ethoxide – or TAETO. TAETO was the first precursor used for CVD of Ta_2O_5 and has become the standard one. Typically, a 10-nm-thick Ta_2O_5 layer is deposited, whose SiO_2-equivalent thickness (t_{oxeq}) is 2.5-nm.

Note that both of these precursors are liquid at room temperature, and so must first be vaporized at 170°C before being flowed into the CVD chamber with Ar as the carrier gas. In addition, the freezing point of TAETO is 18°C and that of TATDMAE is 9°C. Thus, it is a challenge to deliver a fully vaporized precursor to the heated wafer surface without any condensation or decomposition anywhere in the liquid delivery system. To circumvent this problem, TAETO is typically mixed with ethanol. TAETO with 2.5% ethanol has a freezing point of <10°C and thus does not require a heated ampule or heated liquid lines.

The deposition rate of TAETO in the 450-485°C range is reaction-rate limited and is thus sensitive to temperature. (The activation energy of the deposition process is 1.3 eV, which implies that the deposition rate doubles every 25°C in this region.) Above 485°C the process transitions into a mass-flow limited regime. Since excellent step coverage and film conformality are needed in DRAM capacitors, the deposition process must be carried out in the reaction-rate limited regime. Figure 4-7 is a SEM showing that excellent step coverage and conformality is achieved in such high-aspect-ratio structures as found in DRAM devices. The smaller SEMs in this figure show the film details at the top and bottom of the opening.

Since these films are deposited on the doped-polysilicon bottom electrode of the DRAM capacitor, it is undesirable to have an interfacial oxide form on the polysilicon either as a native oxide or during thermal process steps that are performed after the Ta_2O_5 layer has been deposited. (As noted earlier, such an interfacial oxide layer would cause the effective thickness of the capacitor dielectric layer to increase.) To eliminate the possibility of such an oxide layer from existing on the poly, a rapid-thermal nitridation (RTN) step is thus carried out on the polysilicon prior to depositing the Ta_2O_5 film (e.g., at 900°C for 60 sec in NH_3). This RTN step both nitrides any native oxide layer already existing on the poly, and the nitride layer that is thus formed acts as a diffusion barrier to oxygen, preventing any new oxide from forming on the poly during later processes.

The as-deposited Ta_2O_5 films, however, exhibit poor leakage characteristics. It is believed that this occurs because the as-deposited LPCVD-Ta_2O_5 films are oxygen deficient and amorphous. Thus, such Ta_2O_5 layers are densified using an anneal in O_2 to improve their leakage characteristics. Annealing in oxygen is

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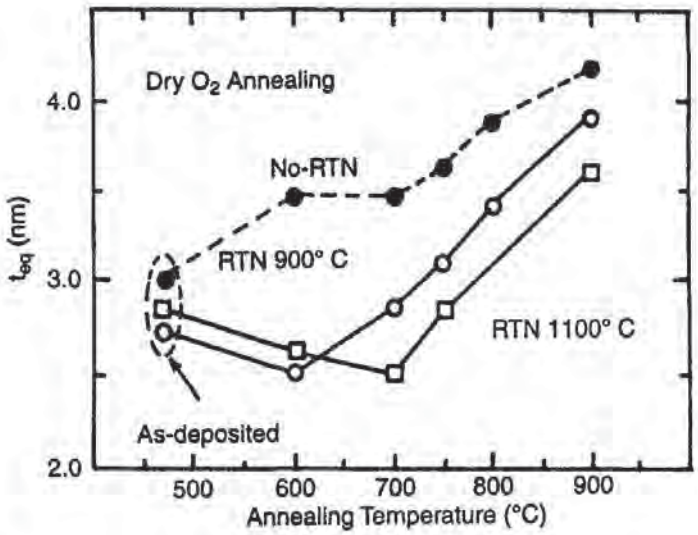


Fig. 4-8 An oxide grows on Ta_2O_5 during post-deposition O_2 annealing. This graph depicts the dependence of $t_{ox_{eq}}$ of Ta_2O_5 on the annealing temperature in a dry-O_2 atmosphere.[11]

thought to balance the stoichiometry of the films by filling vacancies in the undensified film, thus causing the leakage current to decrease.

The conventional oxygen-annealing method is performed in a furnace at 500°C in the presence of UV-generated O_3.[27] However, more recent methods use a rapid-thermal-process in oxygen (RTO). The RTO process minimizes the impact on the thermal budget and reduces the time during which oxygen can react with the substrate beneath the electrode. The oxygenation process in one approach is carried out at 600°C in an oxygen plasma and the temperature is then ramped quickly above 700°C to achieve crystallization of the Ta_2O_5 film.[26] The maximum temperature of the RTO step must still be kept below 800°C because the interfacial oxide under the Ta_2O_5 will grow too thick at higher temperatures (Fig. 4-8)[11] - making the SiO_2-equivalent thickness of the Ta_2O_5 film too great. (That is, at higher temperatures than 800°C, Si can diffuse through the SiN barrier on the polysilicon surface and react with the Ta_2O_5 to form SiO_2.) Up to a six-order-of-magnitude improvement in leakage current has been reported at 1V using such an RTO-annealing procedure.[26]

The densification step also crystallizes the amorphous as-deposited film, and this is also thought to reduce the leakage current through the Ta_2O_5 layers. Finally, since the precursor $Ta[OC_2H_5]_5$ is an organometallic material, the as-deposited Ta_2O_5 layer is not carbon-free. The densification step desorbs some of the hydrocarbon and water molecules, which also shrinks the film thickness. The decrease in film thickness also decreases the $t_{ox_{eq}}$ of the film.

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Another issue involves keeping the top polysilicon electrode from forming a silicide with the Ta_2O_5 layer. This can be prevented by inserting a barrier layer between the Ta_2O_5 layer and the poly. Materials such as TiN and WN have reportedly be employed for this purpose. Another way around this problem is to use a plate electrode material other than polysilicon. For example, as mentioned earlier TiN (deposited by PVD), is typically used as a top (or plate) electrode material with Ta_2O_5.

In addition, even the nitride layer formed on the bottom polysilicon electrode will degrade the overall capacitance to some degree, reducing the benefit of using a high-k dielectric. As a result, an alternative material for the bottom electrode has also been studied. In one report, TiN was used for the bottom electrode, and Pt for the top electrode.[12] In another report, reactively sputter-deposited RuO_2 was used for the bottom electrode. (RuO_2 is a conductive oxide with a conductivity of 35 $\mu\Omega$-cm. Since it is already an oxide, it will not form a dielectric oxide layer at the RuO_2/Ta_2O_5 interface during post-Ta_2O_5 thermal processes.) In one other publication, a $Ru/Ta_2O_5/Ru$ capacitor structure was described. The Ru electrodes were deposited by sputtering. In this report, the Ta_2O_5 film after annealing was found to have a k-value of 65. It was speculated that the Ta_2O_5 layer crystallized on the Ru material during the annealing step in such a way that its k-value was significantly increased compared to layers used with other electrode materials. Significantly lower leakage-currents through the Ta_2O_5 layers were also observed after annealing them in forming-gas at 400°C.[13]

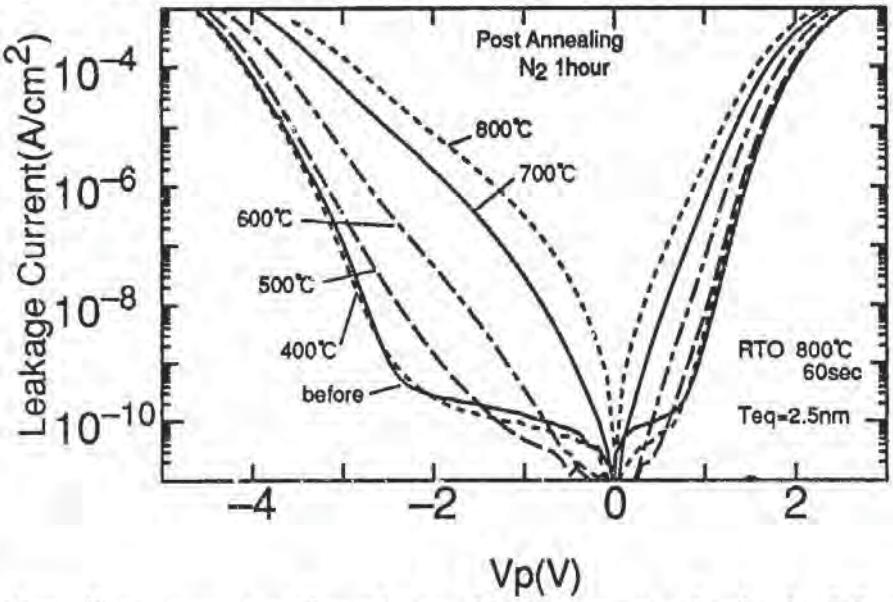


Fig. 4-9 Annealing temperature dependence of leakage current density for 2.5 nm Ta_2O_5 capacitors. A rapid thermal oxidation (RTO) is performed after Ta_2O_5 film deposition.[19]

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Subsequent high-temperature process steps, however, cause the leakage currents through the Ta_2O_5 layers to significantly increase (see Fig. 4-9).[14] In this figure, it is observed that if the Ta_2O_5 layers are subjected to furnace-annealing temperatures of 800°C for 1 hour (or more), the leakage current rises precipitously. Two such high temperature steps that are commonly used in post-Ta_2O_5 layer deposition are those used to reflow the BPSG ILD layer, and to activate the dopants after the source-drain implant step. In one paper, this leakage current was reduced by using a novel low-thermal-budget process that exposed the Ta_2O_5 layers to temperatures no higher than 500°C after the Ta_2O_5 layers are deposited. That is, instead of using a conventional BPSG film, the interlevel dielectric layer (ILD) was formed as follows: An SOG film was first spun on, and this was followed by the deposition of an SiO_2 capping-layer using a low-temperature-CVD process. The source/drain regions were formed with an optimized implant step that employed only a 500°C activation anneal.[14] The application of a Ta_2O_5 layer to a DRAM capacitor formed with rugged polysilicon as the bottom electrode and TiN as the top electrode was described in Ref. 15.

Since leakage through the Ta_2O_5 layers is one of the biggest issues with such films for DRAM applications, work has been done to try and solve this problem. One factor that seems to influence leakage is the surface roughness of the underlying electrode.[16]

Another technique for depositing Ta_2O_5 layers is by *metalorganic solution deposition* (MOSD). This also allows the Ta_2O_5 layer to be doped with Al (a factor that improves some of the Ta_2O_5 layer dielectric properties). For example, thin films with $0.9Ta_2O_5$-$0.1Al_2O_3$ composition exhibited an increased k value of 42 and a lower leakage-current density ($6x10^{-8}$ A/cm^2 up to an applied electric field of 1 MeV/cm).[17]

Etching of Ta_2O_5 layers can be carried out in variety of fluorocarbon gases (e.g., C_2F_6, CH_4, CF_3Cl, CHF_3, and CCl_3F_2),[18] as well as in discharges of Cl_2, SF_6, N_2, or CH_4/H_2. Selectivities of > 6 for Si over Ta_2O_5 were obtained for SF_6/O_2 discharges.[19]

In summary, Ta_2O_5 seems to be the DRAM capacitor dielectric material that will replace ONO. Combined with such polysilicon-electrode techniques as hemispherical-grain poly (HSG), Ta_2O_5 capacitors will be suitable for DRAMs up the 1-Gb and 4-Gb generations (0.15-μm node). The minimum thickness of Ta_2O_5 is estimated to be about an equivalent oxide thickness of 1.5 nm. This implies that even by using HSG and the minimum possible Ta_2O_5 thickness, the limits of Ta_2O_5 technology may be reached at the 1-Gb integration level.

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However, for the 0.13 μm technology node it may be possible that Ta_2O_5 will be used with a MIS capacitor structure (i.e., RuO_2/Ta_2O_5/poly). At the 0.1 μm node it may be necessary to use metal-insulator-metal (MIM) structure (i.e., $RuO_2/Ta_2O_5/RuO_2$). At the 0.05 μm node (50 nm) it is likely that the insulator in an MIM structure will be BST.

4.4.2 Tantalum Pentoxide as a MOSFET Gate Dielectric

Tantalum pentoxide has also been considered as an alternative gate-dielectric material to SiO_2 for MOSFETs with gate lengths of less than 0.1-μm. Since oxide films for such devices would have to be thinner than 1.5-nm, excessive leakage-current through the oxide film would make such MOSFETs impractical for use in most circuit applications. Due to the fact that direct-tunneling leakage currents decrease exponentially with the thickness increase of the dielectric layer, a dielectric with a higher k-value could provide the same electrical behavior as SiO_2 but it could be used with a larger thickness. For the case of Ta_2O_5, which has a k-value of 25, a Ta_2O_5 layer would have a thickness 25/4.0 times larger than that of an equivalent SiO_2 film. Many of the process integration issues of incorporating into a MOS structure were discussed in the previous section. Here, we describe the challenges specific to using Ta_2O_5 as a gate-dielectric layer.

The first problem that must be addressed involves the fact that when Ta_2O_5 is deposited directly on silicon (or when it is subsequently annealed in oxygen), SiO_2 grows under the Ta_2O_5. As much as 2-nm of oxide can grow, thereby increasing t_{oxeq} (see Eq. 4-3). This was demonstrated in a report in which Ta_2O_5 was deposited directly on Si and NMOSFET transistors were subsequently fabricated.[20] An interfacial SiO_2 layer was found to be under the Ta_2O_5 at the conclusion of all processing. A way to prevent uncontrollable growth of such an oxide during subsequent thermal processing steps is to form an interfacial layer between the Ta_2O_5 and the Si substrate. In the first report of fabricating MOSFETs with a Ta_2O_5 gate dielectric, a 2-nm-thick oxide layer was in fact deliberately grown on the Si before the Ta_2O_5 was deposited. This layer was then annealed in N_2 at 800°C for 30 min (nitriding the oxide). A diffusion-barrier is thus created which prevents oxygen from reaching the underlying Si substrate and growing additional oxide. A TiN gate electrode was employed instead of poly (Fig. 4-10). The leakage current was reported to be equivalent to that of a MOSFET with an SiO_2 gate dielectric of identical thickness.[21]

In a second report describing MOSFETs Ta_2O_5 with a gate dielectric layer, the gate dielectric consisted of a stack (i.e., 1.5-nm SiO_2/3.0-7.5-nm Ta_2O_5/0.5-1.5-nm SiO_2). This dielectric stack was electrically equivalent to 20-35-nm

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SiO_2.[22,31] A later report described the use of RTP to grow an interfacial layer on the Si substrate with NO at 800°C for 20 sec - which when combined with a CVD Ta_2O_5 layer - produced a gate dielectric with a t_{oxeq} = 2.3-nm thick. The main benefit of using this approach was that the leakage current through the dielectric film was 1000x smaller than when an oxide was used as the interfacial layer.[23] A similar process flow reported use of a RTN step (nitridation of the silicon substrate surface by RTP in an NH_3 ambient at 800°C for 30 sec), to form an interfacial layer on the poly before depositing the Ta_2O_5 film.[24]

Related to the oxide growth under the Ta_2O_5 is the issue of unacceptably large values of interface traps when using a dielectric other than SiO_2 is in contact with Si. In the Kizilyalli study above, a Ta_2O_5 gate-dielectric-stack (with SiO_2 in contact with both the underlying Si and the overlying poly gate) exhibited interface trap densities comparable to those in MOSFETs fabricated with SiO_2. Charge trapping (a major problem of layered dielectrics) was reportedly not an issue.

A final limitation of using Ta_2O_5 as a gate dielectric is that a barrier over the Ta_2O_5 is needed to prevent silicide from forming due to a chemical reaction of the Ta_2O_5 and the polysilicon gate during subsequent thermal processes. This barrier must be conductive, and TiN, WN, or PGMs used in DRAM top electrodes can be used. However, the difficulty with using such a metallic gate barrier is that the threshold voltage of MOSFETs is increased by about 0.6V. Obviously, this high threshold voltage value is not compatible with low-voltage, low-power technologies. Hence, proper threshold voltage adjustment with counterdoping in the active areas must be employed. However, this produces buried-channel MOSFETs, which degrades their short-channel behavior.

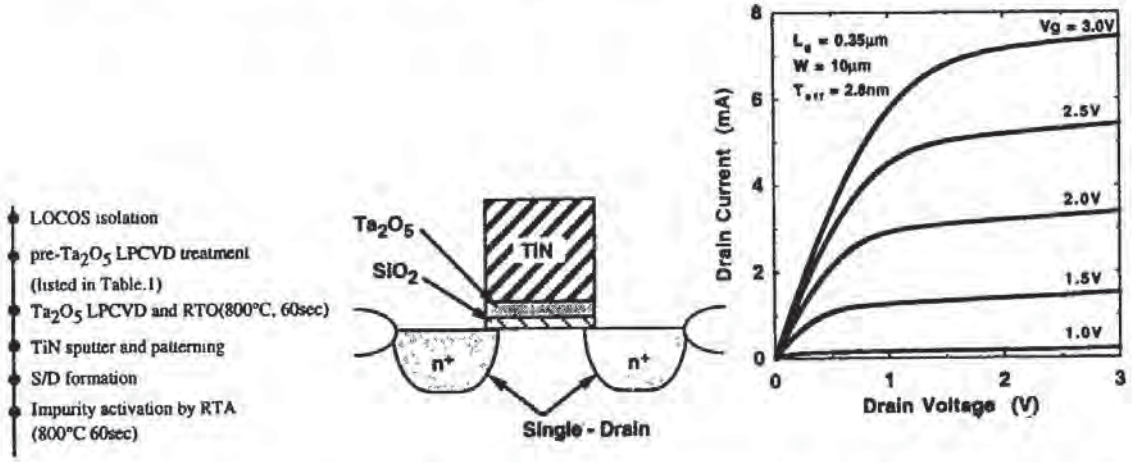


Fig. 4-10 Process flow, cross section, and I-V characteristics of an NMOSFET fabricated with a with a Ta_2O_5/SiO_2 gate dielectric. A TiN gate electrode was also employed.[21]

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4.5 BARIUM STRONTIUM TITANATE (BST) FILMS FOR DRAM CAPACITOR DIELECTRICS

Barium:strontium-titanate (BST) is the candidate material of most promise for use as a capacitor dielectric in future generations of high-density DRAMs. BST films are polycrystalline films, with the crystalline grains having a perovskite oxide structure. The chemical formula of BST is $(Ba_xSr_{1-x})TiO_3$. Common compositions for DRAM use are $0.5 < x < 0.7$. BST films are the leading candidates for advanced DRAM capacitor dielectrics because of their high dielectric constant (k = 88-90 in the film thickness range used in DRAM capacitors), and because the value of k in BST films exhibits a relatively small frequency dependence. That is, the permittivity of perovskite oxide films tends to decrease at high frequencies. For BST films deposited by MOCVD k decreases by < 2% from 100 Hz to 10 MHz and by < 7% from 200 MHz to 2GHz.[30] This is sufficient to meet the requirements of future DRAM generations. Its large dielectric constant (like those of many other perovskites) is the result of the strong ionic polarization in the material.

Many believe that dielectric films with such high-k values will be needed for DRAM capacitors following the 130-nm generation. For example, the required capacitance density in a DRAM technology with a minimum feature size of 0.15-μm with a DRAM capacitor having a stack structure of 0.3-μm in height (i.e., a 2:1 aspect ratio) and a rectangular area of 0.15-μm by 0.45-μm is ~80 fF/μm^2. Figure 4-11 shows a schematic representation of a simple stack-capacitor DRAM cell incorporating a high-k dielectric in the stack capacitor. The high-k dielectric

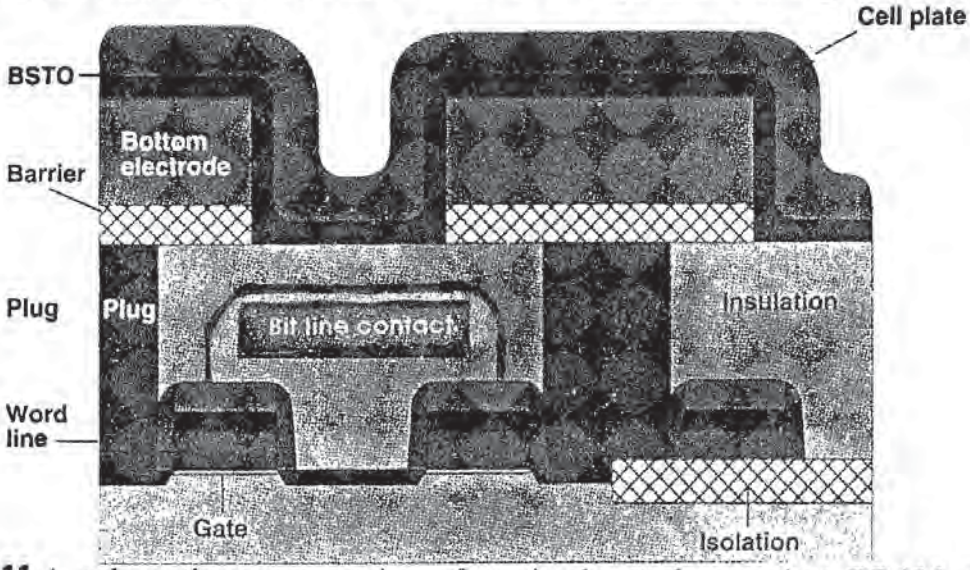


Fig. 4-11 A schematic representation of a simple stack capacitor DRAM cell incorporating a high-k dielectric layer.[47] Courtesy of Semiconductor International.

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material (e.g., BST) covers the top and sides of the patterned bottom electrode. The top electrode forms the common plate electrode, and the word lines and bit lines are located below the capacitor. The structural simplicity in the capacitor of this cell is apparent. In addition, the vertical height of the bottom electrode can be reduced to provide improved control over the critical dimension by reducing depth-of-focus issues.

Note that perovskite materials exhibit *ferroelectric behavior* when held below their Curie point, and *paraelectric behavior* when above that temperature.[28] In conventional DRAMs, the perovskite materials used as the capacitor dielectric are chosen so that they exhibit paraelectric behavior. On the other hand, perovskites that exhibit ferroelectric behavior are used as the dielectrics of FeRAM capacitor structures. BST is a perovskite that has a Curie point that varies linearly with composition, with a value of about 1207°C when x = 1, and about –2207°C when x = 0.[29] The strontium is added to reduce the Curie point below room temperature, which ensures paraelectric operation. The dielectric constant also depends on the film composition, and barium/strontium composition is an important parameter in the use of BST in memory capacitors.

To obtain the high-*k* values necessary for high-density DRAMs, the films must be free of impurities, have correct stoichiometry, and be crystalline.

4.5.1 Deposition of BST Films by CVD

The deposition of BST films can be carried out by a number of methods, including PVD by rf sputtering, thermal MOCVD, sol-gel, and pulsed laser ablation. However, BST film deposition is most commonly done with MOCVD. One reason for this is that rf sputtering requires an appropriately designed composite target. Since sputtering rates for the different elements vary, the useful lifetime of a single sputtering target is too short. BST films deposited by sputtering and sol-gel methods also have a conformality which is typically smaller than 60%, while the conformality of BST films deposited by thermal MOCVD processes can exceed 80%. Because of the high conformality which can be realized, the MOCVD method is likely to be used to deposit the high-dielectric layers for DRAM capacitors. Consequently, we will restrict our discussion of deposition of BST films to the MOCVD processes.

Most precursors of BST are solids at room temperature and are dissolved in an organic solvent for delivery as a liquid to a vaporizer. The liquid is flash-vaporized (to minimize the time precursors spend at elevated temperatures, which minimizes precursor decomposition), and is then transported in a gaseous state to the CVD chamber. This liquid delivery method enables the use of solid

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precursors. However, it chemically complicates the deposition process by introducing a solvent. Most of the published work on CVD BST uses precursors that are adducts of barium and strontium β-diketones along with organometallic titanium compounds, primarily: $Ba(THD)_2$·tetraglyme, $Ba(THD)_2$·PMDTA, $Sr(THD)_2$-tetraglyme, $Sr(THD)_2$·PMDTA, and $(THD)_2Ti(i\text{-}Pr\text{-}O)_2$. (Note that: THD = 2,2,6,6-tetramethylheptane-dionate, and (i-Pr-O) = isopropoxide). These diketones and organometallic-Ti compounds are usually dissolved in butyl acetate. BST films of good quality have been produced using this precursor scheme at deposition temperatures around 550°C. However, at these temperatures, conformality of the deposited films is typically poor and may not be acceptable for three-dimensional capacitor fabrication. A different set of precursors has therefore been developed, which appear promising for BST film growth at lower temperatures. In this precursor scheme, non-adducted versions of the same barium and strontium β-diketones: $(Ba\{THD\}_2)_4$ and $(Sr\{THD\}_2)_4$, along with $(THD)_2$ $Ti(i\text{-}Pr\text{-}O)_2$, are dissolved in tetrahydrofuran (THF). Reports in the literature state that BST films with capacitance densities (planar capacitors) of over 100 $fF/\mu m^2$ and leakage currents in the 10^{-8} A/cm^2 range can be grown at wafer temperatures of 480°C using these precursors. Other work has demonstrated conformality of 100% at 480°C using non-adducted precursors.

The low-temperature CVD processes for depositing BST films give better conformality than do the higher temperature deposition processes. This is due to the fact that different mechanisms are limiting the deposition process. An Arrhenius plot of the deposition rate of BST growth is shown in Fig. 4-12. It can

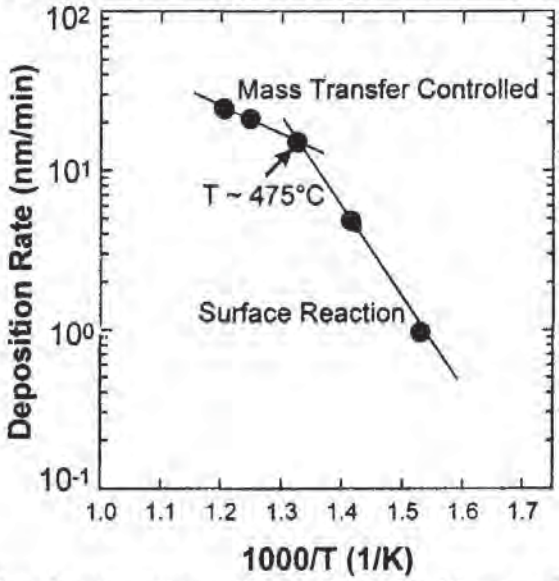


Fig. 4-12 Arrhenius plot showing two regimes of rate-limiting mechanisms for CVD BST deposition using non-adducted precursors. Courtesy of Marcel Dekker Publishing.

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be seen that two distinct regimes are apparent with a crossover at ~480°C. In the higher temperature regime (where the deposition rate is approximately constant with increasing temperature), film growth is rate-limited by mass transport from the vapor phase to the film surface. In the lower temperature regime, film growth is limited by the chemical reaction rate on the surface. Films grown at the higher temperatures exhibit poor conformality because the precursor material reacts immediately upon arriving at the surface and does not have time to diffuse into narrow patterned features before being incorporated into the growing BST film. In the surface-reaction-limited regime, the precursor molecules can diffuse a long way on the wafer surface (i.e., into the narrow patterned regions) before reacting and being incorporated into the growing film.

In BST deposition, a tradeoff occurs between needing a high enough deposition temperature to ensure good crystallinity of the perovskite phase, and needing a low enough temperature to achieve adequate conformality. The adducted precursors form highly crystalline perovskites at high temperatures, but such films deposited at low temperatures are mostly amorphous (i.e., they do not exhibit the perovskite crystalline structure). On the other hand, non-adducted precursors can produce perovskite BST films in the low-temperature regime. The low-temperature deposition is also favored when Ru bottom electrodes are used (see Sect. 4.5.3), to prevent the Ru surfaces from being oxidized during the BST deposition in an O_2 atmosphere.

Note, however, that since the BST films are deposited by CVD at low temperatures (400-500°C) to meet the stringent step-coverage requirements, these films must be subsequently annealed to achieve the desired capacitance and leakage-current behavior. Annealing is usually done after the top electrode has been deposited. Such a post-top-electrode deposition anneal is especially beneficial if the top electrode is deposited using a technique that bombards the BST surface with energetic species (such as PVD). That is, the anneal then serves the additional purpose of healing the damage done to the BST film by the PVD process that deposits the top electrode. Reported annealing parameters vary widely. Temperatures between ~500°C and 700°C have been used, and both oxidizing (N_2O, O_2) and inert (N_2) ambients have been observed to improve the BST electrical properties. Typically, films grown at higher temperatures (550°C) using the adducted precursors require lower annealing temperatures – around 550°C in oxygen is commonly used. Low-temperature depositions require higher annealing temperatures, closer to 700°C.

The main benefit of the annealing processes is a reduction in the leakage characteristics of BST capacitors. Before annealing, films are leaky (Fig. 4-13),

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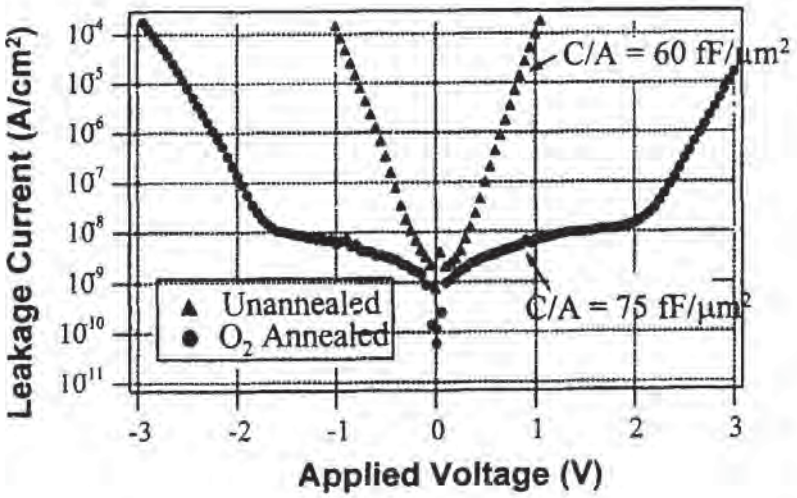


Fig. 4-13 Leakage curves from unannealed and 550°C oxygen-annealed BST films deposited at 600°C. Labels on the leakage curves give the corresponding capacitance densities of the films.

although the capacitance is quite high. After annealing leakage improves to an acceptable level and capacitance increases by roughly 25%, although the improvement is not as dramatic as that seen in the leakage-current properties.

4.5.2 Microstructure Effects on the Electrical Properties of BST Films

A key factor that impacts the electrical properties of BST films is the amount of titanium in the film. Titanium content is referred to as a percentage of all cations in the film, i.e., Ti% = {[Ti]/([Ba] + [Sr] + [Ti])} x 100%. The best properties (e.g., highest capacitance-density) are found when there is a slight excess of titanium, ~51% (compared to the stoichiometric perovskite composition of 50%). Above this amount, the dielectric constant decreases. The sensitivity of the value of k to the titanium content is quite high (e.g., the dielectric constant drops by ~40% when the titanium concentration increases from 51% to 53%). Hence, it is critical that the amount of titanium incorporated during deposition be tightly controlled. A low-temperature, the non-adducted precursor process has been shown to provide such control of incorporated titanium content.

Another important parameter that impacts the BST electrical properties is the surface roughness. Increased surface roughness correlates with lower dielectric constants and higher leakage currents. Roughness is often observed as a hazy film. That is, films that are rough appear hazy to the naked eye under bright light. Roughness can be caused by depositing the film on a rough underlayer, as well as film growth occurring in an island mode. Roughness resulting from film growth

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mode is very sensitive to deposition process parameters, and such parameters must be optimized to find a haze-free process window. Typically less haze is observed at higher deposition temperatures, above 600°C.

4.5.3 BST Integration Issues

Integrating BST into a DRAM process poses many difficult challenges. First, BST is incompatible with the materials that have been used for electrodes up to this point, namely: polysilicon, TiN, and aluminum. This is because BST films contain significant amounts of oxygen and also require high-temperature post-deposition annealing in oxygen ambients. Thus, aluminum films cannot be used as the bottom electrode of a BST DRAM capacitor because they cannot tolerate the high-temperatures used to anneal BST films after deposition (> 500°C). Likewise, polysilicon will oxidize either by reaction with the oxygen that can bleed out from the BST film or with the oxygen present in the annealing ambients. Finally, TiN is no longer stable against oxidizing species at temperatures above 500°C. Hence, alternative electrode materials must be employed.

The most suitable electrode materials are based on the metals found near the middle of the periodic table - such as platinum (Pt), ruthenium (Ru), and iridium (Ir). Oxides of these metals are also conductive, making them candidates for inclusion in the electrode stack. As we will discuss in more detail, one of the major problems of using these materials is the problem of electrode patterning, as these materials produce minimal volatile species during dry etching of the noble metal electrodes (with Ru and RuO_2 being the exceptions).

Platinum is the most commonly used electrode for BST in R&D work, as it is non-reactive with BST, and the growth characteristics of BST films on Pt films are good. However, using platinum is also difficult. Since it is a chemically-inert noble metal, it is difficult to dry-etch. But, it does form silicides, and hence it must be deposited on a diffusion barrier to prevent Si-Pt reactions with the Si wafer. (An example of such a film is stacked layer of Ti/TiN, which is deposited on the silicon substrate. Then the Pt film is deposited on the Ti/TiN film.) Since Pt has poor adhesion to most surfaces, the barrier layer must also serve as a "glue layer." This entire multi-layer bottom electrode structure must then be oxidation resistant and thermally stable enough to withstand the high-temperature, oxidizing environments employed in the processes used to deposit and anneal BST films. Finally, platinum can catalyze reduction in the BST during a forming-gas anneal (instead of protecting the BST against such reduction). Thus, Pt is not a good candidate for the top electrode.

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Other electrode materials can also be used, especially for the top electrode. These include ruthenium metal (Ru), ruthenium oxide (RuO_2), iridium oxide (IrO_2), or conducting perovskite oxides such as $SrRuO_3$ or $(La,Sr)CoO_3$. Ruthenium and RuO_2 are relatively easy to etch, although one of the products of the etching process, RuO_4, has a melting point of 25.4°C, and is both a flammable and highly toxic gas. Figure 4-14 shows the process flow for the fabrication of Ru/BST/Ru capacitors. However, none of these materials is standard in semiconductor processing, and hence all will require significant process-development for incorporation in DRAMs.

Dry-etching of metal oxides, perovskites (including BST), and refractory metals will also provide some serious challenges because they do not have volatile by-products. The etching mechanism for these materials must therefore be more physical, like ion milling. Ion milling has been used for patterning these kinds of materials, but the small feature sizes hinder this technique. Dual-frequency plasma etching is also being examined as a way to etch materials such as platinum, metal oxides, and perovskites. The energy of the ions striking the wafer is controlled to maximize the physical effect while taking advantage of whatever chemistry effect there is. Work has also been carried out on developing high-temperature etch processes for such materials (i.e., > 350°C), as a way to improve the etch-profile and etch-rate of such materials. Masking for the etch process is another challenge. The material to be etched must be physically attacked, while the materials that are used for the mask are etched more easily.

The exceptions, as noted earlier, are Ru and RuO_2, both of which can be patterned by dry-etching (in O_2/Cl_2 plasmas) to give totally anisotropic profiles through chemical reactions which produce RuO_4 in oxygen-containing plasmas. Thus, the profile and feature size of the storage electrodes can be precisely controlled by short gas-residence-time techniques to suppress the deposition of reaction products from the plasma onto the sidewalls. This will permit a 3-D stacked capacitor structure with vertically sided Ru bottom electrodes and BST dielectrics to be used down to 4-16-Gbit DRAMs.

It should also be noted that a diffusion barrier under the bottom electrode is also needed to keep the electrodes from reacting with the polysilicon plug during BST deposition and post-deposition annealing (see Fig. 4-14). Several kinds of materials have been investigated for this role, including: TiN, TiAlN, and TiSiN.

The introduction of high-dielectric materials for DRAM fabrication will also require additional tooling, including:

1. A sputtering system for electrode deposition;

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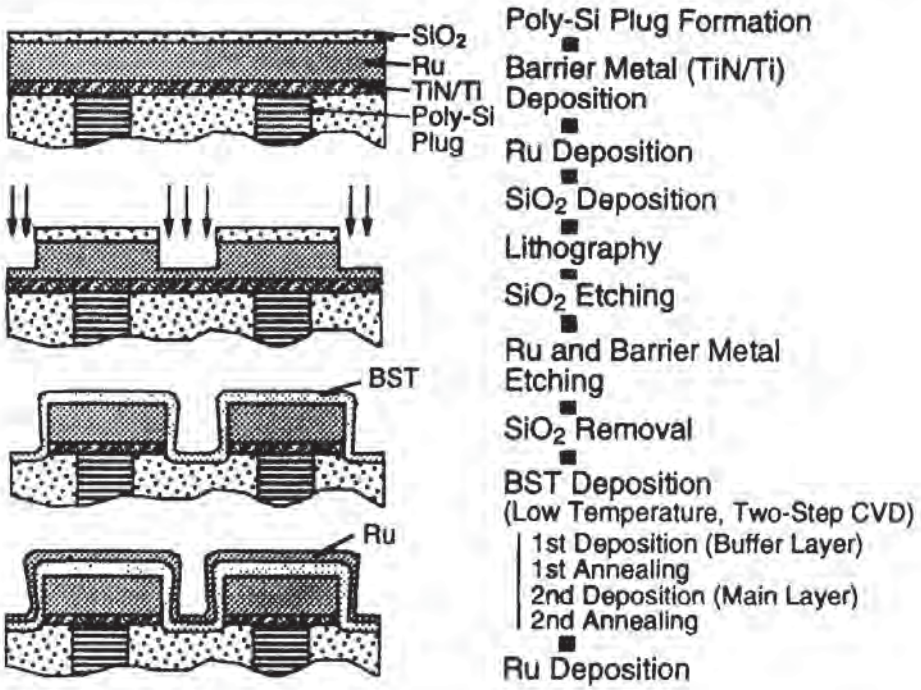


Fig. 4-14 Process flow for the fabrication of Ru/BST/Ru capacitors.[48] (© 2000 IEEE).

2. An MOCVD reactor for the deposition of the high-k dielectric layer, and;
3. A reactive-ion-etch system to pattern the electrode.

Numerous companies manufacture sputtering systems capable of depositing the electrode materials. Applied Materials and Novellus have developed MOCVD reactors capable of depositing BST on 200-mm wafers. Tegal Corp. and Lam Research (along with other suppliers of etch equipment) have demonstrated etch processes for Pt electrodes.

4.6 USE OF OTHER HIGH-k MATERIALS AS GATE DIELECTRICS

An extensive worldwide research effort is being undertaken to develop alternative high-k dielectrics for MOSFETs to replace silicon dioxide. By the end of 2000 workers in the field were not optimistic that despite intensive efforts to find a high-k material that works well, such a material would readily be available for IC manufacturing applications. Their view is that it is going to take at least five years (i.e., until 2006) before a suitable high-k material can be introduced into manufacturing. A review of research on the use of binary metal oxides and silicates up to 2000 was published by Wilk *et al,*[50] and by Gusev *et al,*[51] Here we describe some of the candidates for that application, as of 2001.

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4.6.1 Atomic Layer Deposition for Depositing Thin High-*k* Dielectric Films

Before describing the individual high-*k* materials that are candidates for gate dielectrics in MOSFETs, it is useful to discuss a new deposition technique that may be employed for forming such thin dielectric layers. That is, a promising method for depositing very-thin films has been developed for a variety of applications, including gate dielectrics, DRAM capacitor dielectrics, and diffusion barriers. This technique is called *atomic layer deposition (ALD)*, or *atomic layer chemical vapor deposition* (ALCVD). This technique was pioneered by Tuomo Suntola who invented *atomic layer epitaxy* (ALE) in 1980. The appeal of ALE was that it could deposit very-thin layers of material (<10 nm-thick) with tight composition control. However, at that time the thinnest layers in IC devices were about 100-nm thick, and so ALE was not immediately seen as a technique for the semiconductor market. (It was initially developed for depositing ZnS films for electroluminescent devices.)

In the ensuing 20 years, however, things have changed. Aggressive scaling of critical feature sizes led to lateral dimensions approaching 100-nm, and the thinnest layers approached atomic dimensions. For example, in the gate-dielectric layer, only about 1-nm, or about 4 atomic layers in silicon-oxide equivalents are needed. Clearly, the aggressive scaling has now made applications of the Suntola invention appropriate for integrated circuits. The ALE technique has therefore been modified and commercialized as the ALD technique. The ALD process appears to have several advantages over traditional CVD: it can be carried out at lower temperatures (typically < 400°C); it uses a wider range of precursors; it produces very-thin films; and it inherently obtains 100% step coverage and excellent conformality even over the most challenging topography, and with lower impurity levels.

However, deposition rates are limited by the ALD mechanism. By definition, the thickness of each cycle cannot exceed a few angstroms as determined by the lattice constant of the materials. ALD is therefore targeted at very-thin films having the highest quality demands. The thickness of these films can be controlled simply by counting the cycles. The composition can also be modified and controlled at the atomic level, thus providing an opportunity to create new dielectrics that cannot be easily obtained by other means. Further scaling of critical IC feature sizes will inevitably lead to more applications into the realm of ALD. We will show how ALD can be used to deposit various films in the upcoming sections.

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Several equipment vendors have introduced ALD tools. The first is ASM International (Bilthoven, Netherlands) which, through its acquisition of Microchemistry Ltd. (Finland) now has several systems capable of ALD for semiconductor and flat-panel display applications. (Note that Atomic Layer CVD and ALCVD are trademarks of ASM International). Genus (Sunnyvale, CA) also announced a new ALD capability on its Lynx2 platform. Other equipment suppliers are also apparently developing tools with ALD capability. The nature of the ALD process is such that it can be done in a simplified reactor, where gas flow and temperature uniformity will be relatively unimportant. Instead, the hardware design will focus on preventing deposition on the reactor interior and the wafer backside. Development efforts will be focused on creating ALD tools with high throughput, long mean times between cleans, and low defect density. Reliable and precise control of reactants, quick removal of extra reactants and reaction by-products, and short cycle-time will also be critical to the success of this emerging technology.

ALD works quite differently from conventional CVD techniques. Instead of mixing two or more reactant gases inside the deposition chamber - where they either react in the gas phase and fall on the wafer surface, or they react on the wafer surface - in ALD one reactant gas is introduced at a time. Through a process called "chemisorption," a monolayer of the first gas is adsorbed on the wafer surface. That is, individual precursors are pulsed onto the wafer surface in a sequential manner, without mixing in the gas phase. Each individual precursor reacts with the surface to form an atomic layer in such a way that only one layer can form at a time. This is because the surface reaction occurs such that the reaction is complete, and permits no more than one layer at a time to be deposited, no matter how many molecules are applied to the surface in an overdosing mode. Films are built up by introducing short bursts of gases in cycles.

As an example, ALD can be used to deposit a thin silicon-oxide layer by using silane and oxygen. At room temperature, silane gas is introduced into a chamber containing the wafer. Silane molecules will be adsorbed onto the wafer surface until a monolayer of silane molecules exists over the entire exposed surface of the wafer. Thereafter, no more molecules will be adsorbed by the wafer surface. If the temperature is kept low enough, a stable chemisorbed monolayer will form over the exposed wafer surface. Then, the excess silane gas is pumped from the chamber, and it is replaced with oxygen or water vapor. These molecules react with the silane to form an oxide, and the reaction is completed when one monolayer of oxide has been formed. Then, the excess oxygen is removed, and a

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second burst of silane gas is fed into the chamber to form the next monolayer of silane, and so on. This discussion demonstrates that ALD is a technique best suited for depositing binary materials such as SiO_2 and metal oxides (e.g., Ta_2O_5, Al_2O_3, ZrO_2, HfO_2, etc).

By quickly switching the gases on and off (in less than 1 sec), it is possible to obtain reasonable growth rates, up to 200-Å/min. For those films that are deposited in the thickness range of 10-50-Å (or less), such growth rates should produce acceptable throughputs. In addition, since it is only necessary to saturate the wafer with the precursor, the chamber does not have to be designed for uniform reactant coverage. This allows the chamber to be kept very small (e.g., only 4 mm high), which in turn, allows as many as 4 cycles per second to be run. The claim made earlier that ALD deposition temperatures are generally low can now be understood in light of the fact that this process depends on chemisorption.

4.6.2 Aluminum Oxide (Al_2O_3) as a Gate Dielectric

Aluminum forms a stable oxide (aluminum oxide, Al_2O_3), and it is one of the materials that is being studied as a high-k gate dielectric. The k-value of Al_2O_3 is about 9, which is about three times as large as that of SiO_2. The effective k-value of the dielectric layer which employs Al_2O_3 is, in fact, even somewhat smaller (i.e., it is ~5.5-6.0). This reduction in the effective k-value occurs because a thin interfacial SiO_2 layer inevitably forms between the Al_2O_3 layer and the silicon substrate during Al_2O_3 deposition. This extra, unwanted, interfacial layer reduces the effective k-value, and increases the equivalent oxide thickness (EOT) of the Al_2O_3 layer. (But this interfacial layer also plays a beneficial role in reducing the interface state density leakage current.) Thus, while Al_2O_3 promises to provide a dielectric layer that has an improved k-value, this improvement may only be adequate for a single technology node.

Aluminum oxide is attractive as a gate dielectric for future MOSFETs not only because it has a higher k-value than SiO_2, but because it also exhibits excellent thermal stability when it is in contact with silicon, and because it has a wide energy gap (~8.3 eV). Furthermore, it is compatible with polysilicon without requiring any barrier materials.

Recent work has described the fabrication of CMOS devices with an Al_2O_3 gate dielectric.[37,38] The Al_2O_3 layer is deposited by atomic layer deposition (ALD - as described in Sect. 4.6.1), using trimethyl-aluminum (TMA) and ozone as the precursors, at 450°C. (Figure 4-15 shows how an ALD process can be used to deposit an Al_2O_3 layer using the above precursors.) Polycrystalline silicon is then deposited and patterned, junction implants are performed, and a rapid ther-

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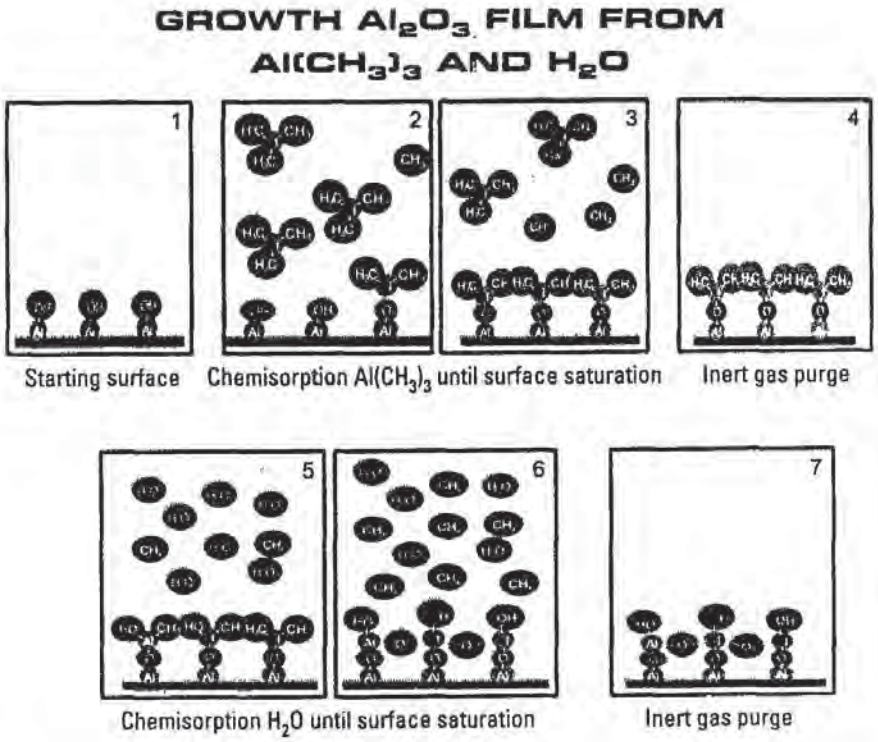


Fig. 4-15 Atomic layer CVD works by introducing one reactant gas at a time. The first gas is "chemisorbed" onto the wafer surface. Excess gas is then purged and the second gas (in this case, water vapor) is introduced. This gas reacts with the chemisorbed layer, creating a monolayer of deposited film. Courtesy of Semiconductor International.

mal anneal at T = 1000°C is performed. The leakage current density exhibited by MOS capacitors with an Al_2O_3 layer is 2-3 orders of magnitude lower than that observed in MOS capacitor built with an SiO_2 layer with the same EOT.

One major drawback of MOSFETs built with an Al_2O_3 dielectric layer is that the carrier mobility is smaller than in MOSFETs built with SiO_2 dielectric layers, probably due to electron trapping by the Al_2O_3 material. By the end of 2000, the reason why such electron trapping occurs in Al_2O_3 layers (and other high-*k* dielectric materials) is still unknown.

4.6.3 Zirconium Oxide (ZrO_2) as a Gate Dielectric

Zirconium oxide (ZrO_2) is considered to be one of the most promising high-*k* dielectric candidates to replace the SiO_2 gate dielectric. ZrO_2 has a dielectric constant of ~20-25 and is thermodynamically stable in contact with silicon.[44] In addition, ZrO_2 has a band gap of ~5.1 eV and a lattice mismatch with silicon of only 2.1%. It has been shown that reactively sputtered ZrO_2 (i.e., a Zr sputter target is used in an Ar + O_2 ambient) has a low equivalent-oxide-thickness

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(EOT), low leakage, and good reliability characteristics.[40,41] (Another way that ZrO_2 can be formed with a PVD process is by oxidizing a sputtered Zr film in an RTP process.[45]) ZrO_2 films can also be etched in HF solutions. It has also been reported that doping the ZrO_2 films with Al produces amorphous films with better uniformity, but with a slightly lower dielectric constant. This doping can be achieved in a PVD deposition process by co-sputtering with an Al target.[41]

ZrO_2 films can also be deposited using an atomic layer deposition process (ALD).[42,43] The ALD process has the inherent advantage of conformality over PVD deposition processes. Such an ALD process for ZrO_2 is illustrated in Fig. 4-16. Generally, ALD requires that the metal compound precursor and nonmetal compound precursor ($ZrCl_4$ and H_2O, respectively, for the case of ZrO_2) are introduced alternately instead of simultaneously as in a standard CVD process (see Sect. 4.6.1). This results in the layer-by-layer growth that creates the characteristics of ALD films, making them appropriate for several applications. In the case of Zr-based dielectrics, the material may consist of zirconium, aluminum, and oxygen.

In any case the ZrO_2 films are amorphous, and a very thin interfacial silicate layer (9-Å thick) exists at the silicon/ZrO_2 interface. Post-deposition annealing in oxygen or inert gases (at 400-500°C) is found to be necessary to reduce the leakage current of deposited films. After high-temperature annealing, this layer grows and converts to a more stoichiometric SiO_2 layer. Significant SiO_2 growth is observed at the ZrO_2/Si interface annealed at 400-600°C even under low partial pressures of oxygen. Reaction with the Si substrate and the polysilicon gate also occurs at higher temperature (≤ 1000°C) processing steps.

Films of zirconium silicate doped with aluminum (Zr-Al-Si-O) have also been studied as candidate high-*k* gate materials.[42] It was noted that doping ZrO_2 films with Al improves the resultant ZrO_2 dielectric layer. That is, the undoped ZrO_2 films have high diffusivity of oxygen, and so oxygen can diffuse through the ZrO_2 during the post-deposition anneal and react with the underlying Si to form an SiO_2 interfacial layer. The addition of Al reduces the rate of oxygen diffusion through the ZrO_2 film. Another report described the use of yttria-stabilized ZrO_2 (YSZ) films as a high-dielectric constant layer in MOSFETs. The advantage of the YSZ film is that it can be epitaxially grown on a silicon substrate by pulsed laser ablation without the formation of an interfacial silicon oxide layer.[46]

At the end of 2001, Intel announced that a new transistor structure that included a ZrO_2 gate dielectric layer, deposited by ALD. They stated that this new MOSFET structure would be used for devices built by Intel from 2005 and beyond.[55]

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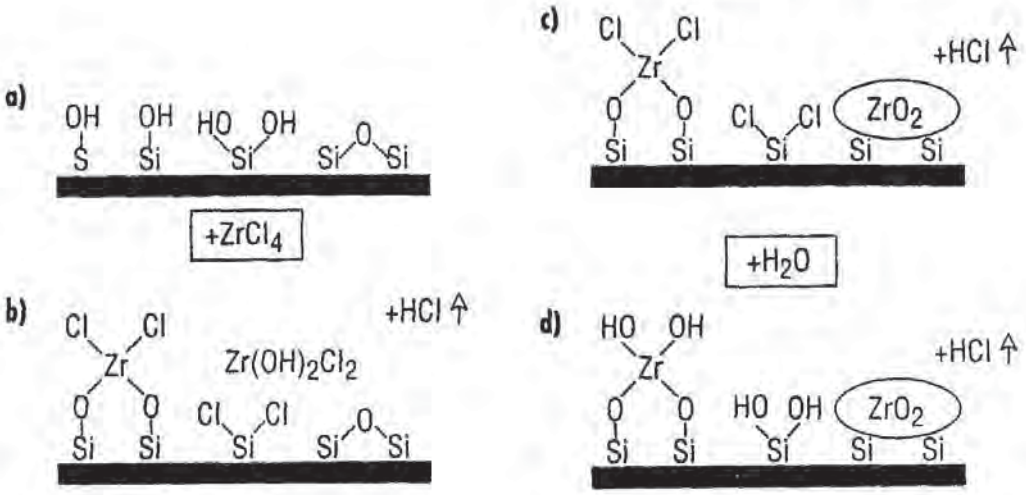


Fig. 4-16 Atomic layer CVD growth mechanism of the high-*k* dielectric ZrO_2 from $ZrCl_4$ and H_2O. Courtesy of ASM International.

4.6.4 Hafnium Oxide (HfO_2) as a Gate Dielectric

Hafnium oxide (HfO_2) has been investigated as a high-*k* dielectric for MOSFET devices. Early reports described fabrication of MOSFETs with n^+ polysilicon gates,[32] and more recent ones have discussed the characteristics of MOSFETs with p^+ polysilicon gates as well.[33] Hafnium oxide exhibits excellent materials properties for these applications, namely: a high dielectric constant (k = 24 - 40); good thermal stability when in contact with silicon; and an energy gap of 5.65 eV. (Hf forms the most stable oxide with the highest heat of formation [ΔH_f = 271 Kcal/mol] among the elements in the IVA group of the periodic table [Ti, Zr, Hf].) In addition, HfO_2 is very resistive to impurity diffusion and intermixing at the silicon/dielectric interface because of its high density (9.68 g/cm^3).[39]

The HfO_2 films described in the reports were deposited either by PVD (reactive sputtering),[32,33] or by *in situ* RTCVD.[34] MOS capacitors were fabricated with an equivalent oxide thickness (EOT) of 12-Å (and a physical thickness of 38-Å) by optimizing the polysilicon deposition process and the subsequent annealing steps that would be used to activate the MOSFET source/drain implants. That is, no interfacial layer was found to be formed between the HfO_2 and the polysilicon gates if the polysilicon deposition temperature was kept below 600°C, and the RTA anneals were carried out at 1000°C. However, the same report indicated that an unwanted interfacial SiO_2 layer IL does form between the HfO_2 and the silicon substrate during the HfO_2 deposition (Fig. 4-17). In addition, some crystallization of the HfO_2 is observed to occur during the RTA anneal steps. A more recent study claims that HfO_2

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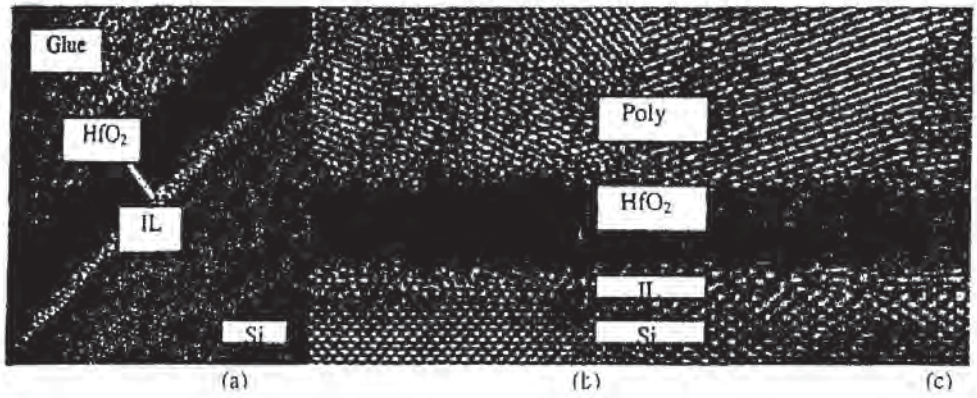


Fig. 4-17 HR-TEM showing HfO_2 (~38Å) and IL (~6Å): (a) after PDA, and (b) and (c) RTA 900°C and 1000°C for 1 min, respectively.[33] (© 2000 IEEE).

exhibits more thermal stability than does ZrO_2.[51] Two other papers published at the same time also states that better MOSFETs were fabricated with HfO_2 than with ZrO_2 as the gate dielectric.[52,53]

The leakage current characteristics of such MOS capacitors was about four orders of magnitude smaller than a MOS capacitor fabricated with SiO_2 having the same 12-Å EOT (as a result of the HfO_2 layer having a physical thickness more than double that of the SiO_2 layer). However, like other high-*k* dielectrics, the HfO_2 films also tend to trap electrons and thus degrade carrier mobility in the MOSFET channel. In another report, scalability of the EOT of the HfO_2 layer to less than 10-Å was demonstrated by using a TaN gate electrode to replace the polysilicon gate electrode.[35] That is, the polysilicon-depletion effect is avoided if a TaN gate electrode is used instead of polysilicon, and therefore an EOT as small as 8-Å can be obtained.

A recent study was published on the use of HfSiON as a high-*k* gate dielectric. This is an amorphous material and exhibits smaller leakage currents than does silicon dioxide at equivalent oxide thicknesses. HfSiON films scaled below 13-Å showed good reliability performance.

4.6.5 Praseodymium Oxide (Pr_2O_3) as a High-*k* Gate Dielectric

Another exotic material that has been studied as a high-*k* gate dielectric is *praseodymium oxide* (Pr_2O_3).[36] The key advantage that is exhibited by MOS capacitors made with Pr_2O_3 layers is that they exhibit ultra-low leakage current densities. That is, leakage currents of 5 nA/cm^2 at 1V have been demonstrated for Pr_2O_3 layers with EOT of 14-Å. This is four orders of magnitude lower than the best reported results for other high-*k* materials. Such Pr_2O_3 films also exhibit an effective dielectric constant of 31. In addition, no significant hysteresis is

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observed in the C-V measurements, provided the material is furnace annealed only briefly at 600°C. These layers can also survive an RTA anneal of up to 1000°C for up to 15 seconds with no degradation in electrical properties.

The Pr_2O_3 layers are polycrystalline. Ordinarily, the dielectric layers of MOS capacitors have an amorphous structure, and if the structure begins to become polycrystalline, the films become leaky. High-temperature post-deposition anneals tend to crystallize the dielectric films, and this can cause an increase in the leakage currents through other dielectric layers. Apparently this is not the case with Pr_2O_3. It should be noted, however, that although it is possible to deposit polysilicon films on these layers, the poly/Pr_2O_3 interface is rough. (In this work, instead of using polysilicon as the top electrode, a top electrode to the Pr_2O_3 was formed by evaporating gold onto the Pr_2O_3 through a shadow mask.)

The Pr_2O_3 layers in this study were deposited by molecular beam epitaxy (MBE) at temperatures between 625 and 725°C at a growth rate of 0.1-Å/sec. They were then subsequently furnace-annealed at 600°C for 5 minutes in dry nitrogen. A 1000°C/15 sec RTA anneal in N_2 was shown to cause no structural change in the films, and no change in their electrical properties.

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Chapter 5

THE STRUCTURE OF DEEP-SUBMICRON MOSFETS: Retrograde-Wells; Super-Steep Retrograde Channel Doping; Drain Engineering; Punchthrough-Control Structures

In Chapter 1 we discussed the evolution of MOSFET structures down to the submicron technology nodes in production at the time publication of this text. In this chapter we delve further into the details of the MOSFET regions that are fabricated in such deep-submicron MOSFETs, namely: **1**) retrograde wells for CMOS twin-well technology; **2**) super-steep retrograde (SSR) channel doping profiles; **3**) drain engineering issues in deep-submicron MOSFETs; and **4**) punchthrough-control structures.

5.1 WELL-FORMATION IN DEEP-SUBMICRON CMOS

Twin-well CMOS is now the dominant CMOS technology in IC production. In twin-well CMOS each well is formed separately by implanting the well dopants into a lightly doped substrate region. Having two well implants allows each well-type to be tailored separately, permitting independent device performance adjustments for both PMOS and NMOS transistors. When first introduced, twin-well CMOS structures were fabricated by using moderate-energy implants to place both types of well dopant near the wafer surface. These dopants then had to be driven into the substrate by a long (12-24 hour), high-temperature (>1100°C) diffusion process (Fig. 5-1). Such a deep drive-in step was needed to prevent punchthrough from the MOSFET drain regions at the surface to the substrate under the well. This type of CMOS-well-structure is referred to as a *diffused-well.* However, use of diffused-well structures gives rise to some problems which limits their use when CMOS is scaled below 0.5 μm:

1. Lateral (as well as vertical) diffusion occurs during the diffusion step, which has the effect of reducing packing density. For example, since the lateral diffusion is ~0.7 times the junction depth, a typical diffused well having a vertical junction depth of 3-4-μm, results in a lateral spread of well dopant of 2-3-μm. Consequently, the maximum aspect ratio of a diffused well is limited to about 1.6:1 (i.e., wells narrower than about 1.6 times their depth would intermingle with the dopant of adjacent wells).

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2. If LOCOS isolation is used, boron from the *p*-well-dopant implant-step segregates into the oxide during the long, high-temperature field-oxide growth step. Compensating for this effect requires a separate field-threshold-adjust implant (also referred to as a *channel-stop-implant*), prior to the field-oxidation step. This additional step adds process complexity.

3. Diffusion of the channel-stop-implant dopant into the active regions during field oxidation adversely affects both the junction-capacitance and the turn-off characteristics of the NMOSFETs (see Vol. 3).

4. The lengthy, high-temperature drive-in-step increases process cycle time, and increases the risk of silicon wafer warpage, bow, and flatness degradation (and the likelihood of metal contamination from furnace heating elements).

5. The diffused-well profile for a particular technology node is the net result of compromises between the need to control threshold-voltage, to suppress hot-carrier effects, to control punchthrough and soft-error effects, and to provide latch-up immunity. For example, a high dopant concentration is desirable deep in the well to strengthen latch-up immunity. This cannot be achieved in a diffused-well because doping at the bottom of such a well must be lower than at the surface, and the maximum surface doping is set by limits on junction breakdown voltage and junction capacitance.

For all of the above reasons, the diffused-well approach to forming a twin-well CMOS process becomes less effective for each smaller technology node. As a result, an alternative method of forming the wells was sought. The technique adopted to replace the older diffused-well structure when CMOS technologies are scaled below about 0.5-μm involves *retrograde-well formation* with *high-energy ion-implant steps*.

5.1.1 Retrograde-Wells for Deep-Submicron CMOS

The medium-energy implant steps used to introduce well-dopants into the substrate in the diffused-well approach (50-100-keV), can be replaced with high-energy-implant steps (300-keV to 1-Mev). Such high-energy implants cause the peak of the implant to be located considerably deeper within the silicon substrate (at roughly 1-μm for the energies most frequently used in high-energy implant processes). Since the implant peak is now far beneath the silicon surface, the impurity concentration thus decreases as the doping profile approaches the wafer surface. Since the well-profile in this case is different from that of a conventional

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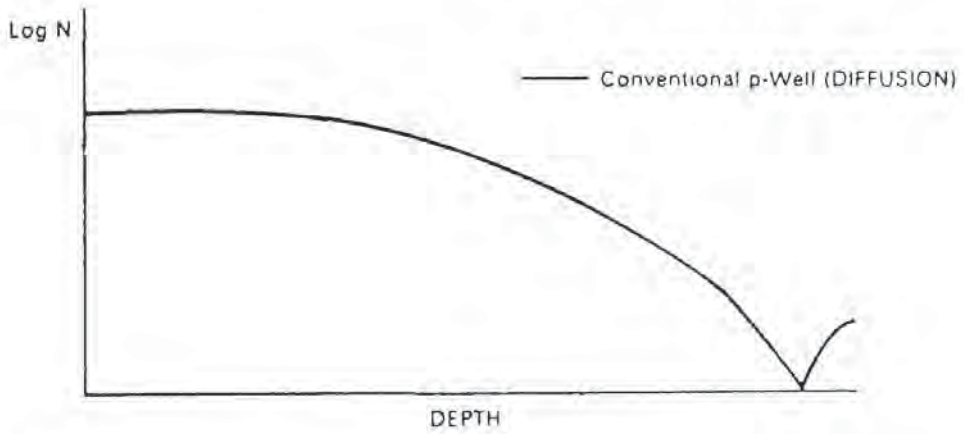


Fig. 5-1 Doping profile in a conventional well formed by a shallow implant and drive-in step.

diffused well (in which the doping concentration after drive-in is highest at the surface, and decreases monotonically with depth, as seen in Fig. 5-1), such deeply implanted wells are known as *retrograde-wells*.* Comparison of the doping profiles in conventional and implanted *p*-well profiles (obtained by simulation) is shown in Fig. 5-2.[2,3] The retrograde-doping-profile is retained by minimizing the temperature-cycles of later process steps (e.g., by using RTP instead of furnace anneals).

The retrograde-well approach to forming the twin-well CMOS-structure has several major advantages over the diffused-well process:

1. Much less lateral-dopant-spread occurs for a retrograde-well having the same junction depth as a diffused-well. This is because ion implantation is a more anisotropic dopant-distribution process than diffusion (i.e., the lateral-straggle for implant energies of 500-keV is only ~0.7-μm). In addition, little additional diffusion occurs after the implant is performed, since only a short anneal at a relatively low-temperature is needed to activate the implant. Thus, the total lateral-dopant-spread barely exceeds 1-μm after all thermal processing (compared to at least 2-μm for the same well-depth using a diffused-well process).[2] Figure 5-3 depicts the doping concentration profile of a high-energy implanted *p*-well. In this example, the implanted *p*-well is formed by boron implantation at 400-keV.

In addition, high-energy implanters can place dopant beneath a shallow-

* In order to avoid excessive spread of the active-device electrical parameters, the surface concentration after the retrograde implant should be at least five times smaller than its final value - which will be set by subsequently performed, shallower low-dose implants specifically designed for threshold and punchthrough control.

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trench-isolation oxide or a LOCOS field oxide, allowing the CMOS twin-well structure to be implanted *after* the dielectric isolation features are formed. (In diffused-wells, the well-dopants must be implanted before the field-oxide, and driven-in either before - or during - the field-oxidation step). Thus, since the high-energy implanted wells are formed after the long, high-temperature cycle needed to grow the LOCOS field-oxide, lateral-spread of the well-dopants is further reduced. (A higher threshold voltage can also be achieved in the LOCOS field-regions of the p-wells if the boron implant is done following field-oxidation, because the boron does not segregate out into the oxide during the field-oxide growth-step.[1]) Hence, the 7-9-μm n^+-to-p^+ spacing required for a twin-well 1.2-μm CMOS process which uses conventional wells, can be reduced to ~5-μm if retrograde wells are used instead. Such overall reduced lateral-dopant-diffusion permits higher circuit-packing-densities.

2. By combining the high-energy-implant step with the other lower-energy MOSFET channel implants (V_T-adjust and punchthrough stopper) and since minimal thermal diffusion occurs, control of dopant levels throughout the depth of the well becomes possible with fewer tradeoffs (a task that has been dubbed "Well Engineering"). This permits optimization of such key

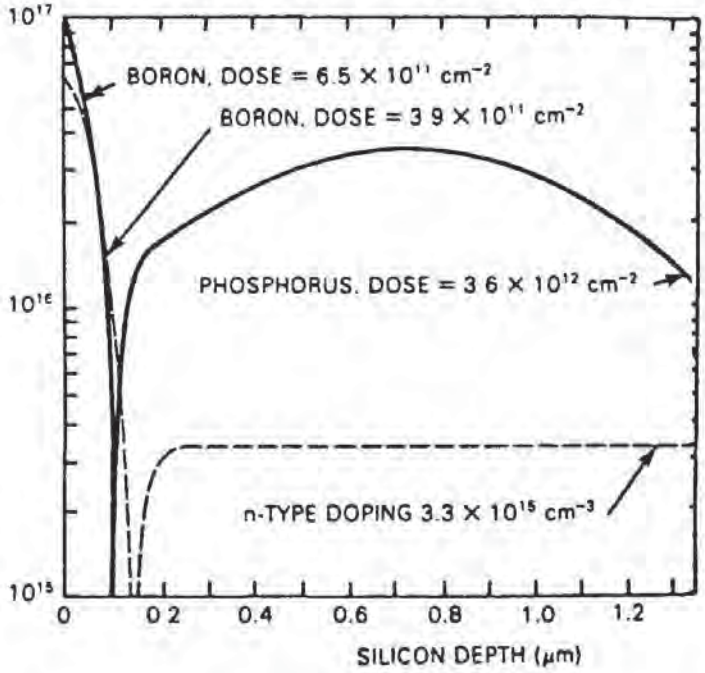


Fig. 5-2 Simulated doping profiles in PMOS channel regions: dashed lines, lightly doped substrate; solid lines, retrograde n-well.[3] (© 1982 IEEE).

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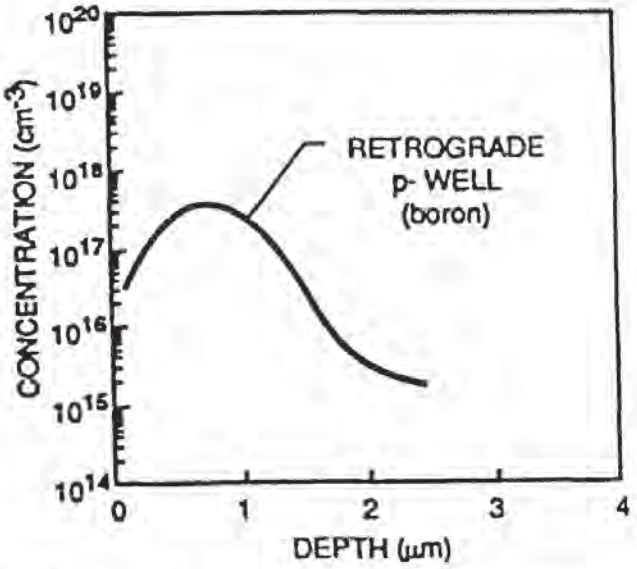


Fig. 5-3 Example of the doping profile of a retrograde *p*-well (boron) implant (400 keV).

MOSFET performance characteristics as: device speed (carrier mobility and, S/D capacitance), inter-device leakage-currents, V_T-control, punch-through suppression, parasitic-transistor effects, and soft-error and latch-up resistance. That is, low surface-doping levels increase mobility and decrease capacitance. Heavier doping below the surface (retrograde doping) suppresses minority carrier collection by decreasing depletion widths; thus reducing soft errors and latchup susceptibility. This degree of flexibility in optimizing device parameters is not possible with diffused-wells.

Besides the primary benefits of increased packing-density and greater process flexibility, retrograde-wells offer the following secondary advantages:[5]

1. A retarded electric field is created in the parasitic-vertical-bipolar-transistor, thereby reducing its current gain. This affords some extra protection against latchup.

2. Susceptibility to vertical-punchthrough is reduced without having to significantly raise the surface-doping-concentration.

3. The conductivity in the bottom of the well is increased, which also provides additional resistance against latchup.

4. The shallower well depth should also make the drain of the parasitic n^+-to-n-well (or p^+-to-p-well) parasitic-FETs shallower. This contributes to improvements in both the short-channel threshold-roll-off-effect and the in the punchthrough characteristics of these parasitic field-region devices (see Vol. 3, Chap. 6).

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5. The formation of retrograde-wells with high-energy implants results in a reduced-doping-concentration under the bottom of the source and drain regions, which reduces the source/drain-to-body junction-capacitance.

However, some concerns associated with the retrograde process should also be mentioned. First, the process requires a thick photoresist as a masking material for the high-energy implant. Typical resist thicknesses are 2.0-2.5-μm, and special exposure and development techniques are required for this process. Implant shadowing arising from the use of such thick resists must also be addressed. (We will address the challenges associated with the use of thick resists as high-energy-implant masks in more detail at the end of this section.) Questions have also been raised about the possibility that the high-energy implants could cause damage that may degrade device and circuit performance.

5.1.2 Process Integration Issues Involving the Use of Retrograde Wells

Advanced twin-well CMOS processes with both retrograde *n*- and *p*-wells (using short [~5 min] RTP well-drive-in steps), were reported for submicron applications as early as 1991.[6] Further advances continued throughout the decade. Scaling CMOS to 0.5-μm and below reduces the well depths required to prevent vertical punchthrough and latchup. In turn, as device and isolation dimensions shrink with each device node, retrograde-well implant-energies for both DRAM and logic circuits are also gradually being reduced. However, the retrograde-well implants used for DRAM devices typically require higher doses than those used in logic devices (i.e., to achieve better minority-carrier suppression [soft-error rate]). This, in turn, requires a higher well-implant-energy (to avoid excessive dopant in the near-surface [channel] region). In addition, the well-depth and well-dopant-concentration can be reduced if additional, lower-energy implants are precisely located with respect to the transistor structure (to suppress punchthrough of the MOSFET channels and enhance the field-isolation characteristics).

The high-energy implant step used to form retrograde-wells in deep-submicron-CMOS is typically performed together with the V_T-adjust, punchthrough, and channel stop (isolation) implants. These implants are all done in the same implanter, without removing the wafers from the implant process chamber in between (unless channel engineering implants [that use high wafer-tilt-angle for precision dopant placement] are required - see Sect. 5.4). Such a "chained" implant sequence is performed by doing the highest-energy implant first, with the lowest-energy implant being done last. This ensures that no ions traverse the end-of-range (EOR) damage of a previous implant. Note that because

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of economic requirements for high equipment utilization, this sequence must be carried out in an implanter that has the capability of doing not only high-energy implants (e.g., up to about 1-MeV for the retrograde *n*-well implant), but also lower-energy boron implants (down to about 10-keV, for the NMOS V_T-adjust implant).

An example of a "chained implant" retrograde twin-well CMOS process is given in Ref. 7. Here, a retrograde *n*-well is formed by a 600-keV, $3x10^{13}$ cm^{-2} phosphorus implant. Then, a second phosphorus implant (150-keV, $4x10^{12}$ cm^{-2}) is used to obtain both punchthrough prevention and intra-field isolation (channel stop), and a third phosphorus implant (70-keV, $6x10^{12}$ cm^{-2}) sets the threshold voltage. In an identical manner, three selective boron implants are placed in the *p*-well region. The retrograde *p*-well implant is boron at 300-keV, $3x10^{13}$ cm^{-2}. Then a punchthrough/channel-stop-implant at 150-keV, $4x10^{12}$ cm^{-2} and a threshold-adjust-implant at 30-keV, $5.5x10^{12}$ cm^{-2} are added. The process displays very good inter-well isolation characteristics, which allows a minimum p^+-*to*-n^+ spacing 40% lower than the same process without retrograde wells. It also achieves very good intra-well isolation, allowing n^+-to-n^+ (and p^+-to-p^+) device separation of 0.5-μm, without an additional channel-stop implant.

From a manufacturing perspective, the well-formation sequence thus appears to be a single implant step, reducing manufacturing complexity and cost. Figure 5-4 compares an advanced diffused-well process with a high-energy implanted process up to gate oxidation, showing the process simplification possible with "well-engineering." Eliminating process steps has other benefits besides reducing cycle time. These include a reduction in work-in-progress (WIP) inventory, less wafer handling, and fewer defects.

The cycle-time and cost savings obtained from such a "chained-implant" sequence was assessed by SEMATECH. They sponsored a comparison of a baseline diffused-well process with a high-energy retrograde-well process at two different chip manufacturers. The high-energy processes were engineered to achieve minimum cycle-time and maximum cost savings, while maintaining the same basic device and circuit parametric data (and thus were identical to the baseline processes after gate-oxidation). Significant improvements in cycle-time, cost, and device-performance were achieved by both companies.

By chaining these implants, the doping-profile in the well-regions of the MOSFETs has a *modulated* characteristic as depicted in Fig. 5-5 (where the term "modulated" means that the doping-concentration-profile has several maxima and minima).[7] The incorporation of such multiple implants to form a modulated well has become a firmly established processing approach in chip production.

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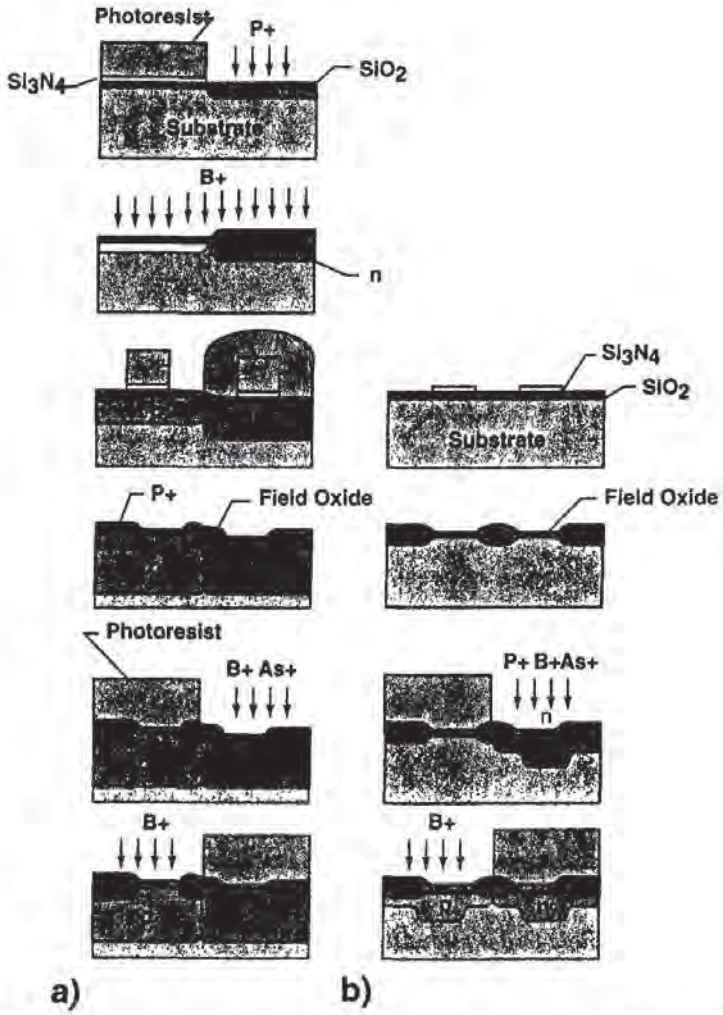


Fig. 5-4 Fabrication sequences for: a) conventional-diffused-well and; b) high-energy-implanted-well processes.

Another issue of using high-energy implants to introduce the well and isolation dopants involves implant shadowing. That is, as shown in Fig. 5-6a, thick photoresist films must be used as masks against the high-energy implant (e.g., 2.0-2.5 μm thick). The doping asymmetry resulting from high energy implants with a small (7°) tilt angle can have significant effects on retrograde well structures and inter-well isolation. Figure 5-7 depicts the simulated doping profiles from a 1 MeV phosphorus implant with a 7° tilt.[8] The simulation accounted for the fact that opposite corners of the photoresist will wear down and carbonize differently because of the asymmetry in the incoming ion beam. As the sidewall shape of the photoresist changes with time, this will affect the implanted profile in the silicon. The doping profiles in Fig. 5-7 clearly show a bulge of lightly doped material on the shadow side of the profile. More seriously, on the

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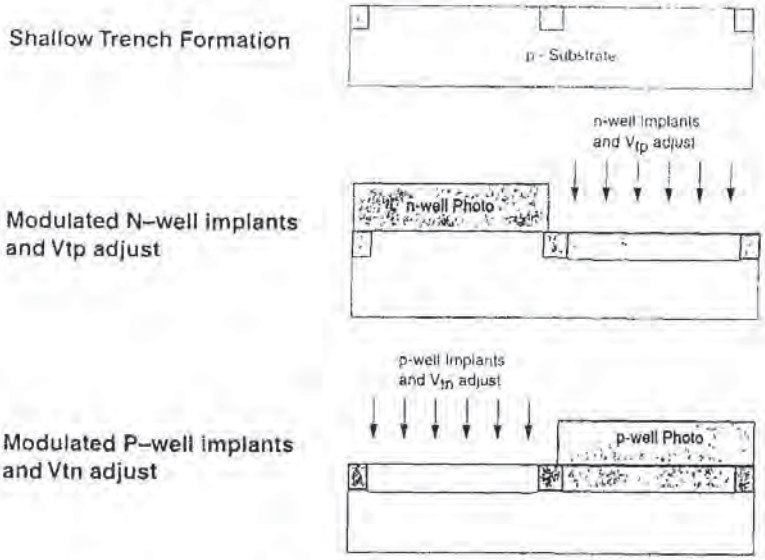


Fig. 5-5 Modulated *n*-well structure for advanced devices, showing the functions of each implant.[7]

incoming side, a channel doped to 20% of the peak-concentration extends from the projected range up to the surface. Doping variations such as these can adversely affect the mobilities and junction-capacitances of the resulting devices. This will also make it harder to maintain adequate isolation structures as isolation widths scale below 400-nm. These problems can be mitigated by reducing the tilt-angle to the 2-4° range, using 0°-tilt. However, using 0°-tilt-implants is not always possible, due to channeling effects (which are severe at high energies).

An alternative solution to the implant shadowing problem during high-energy

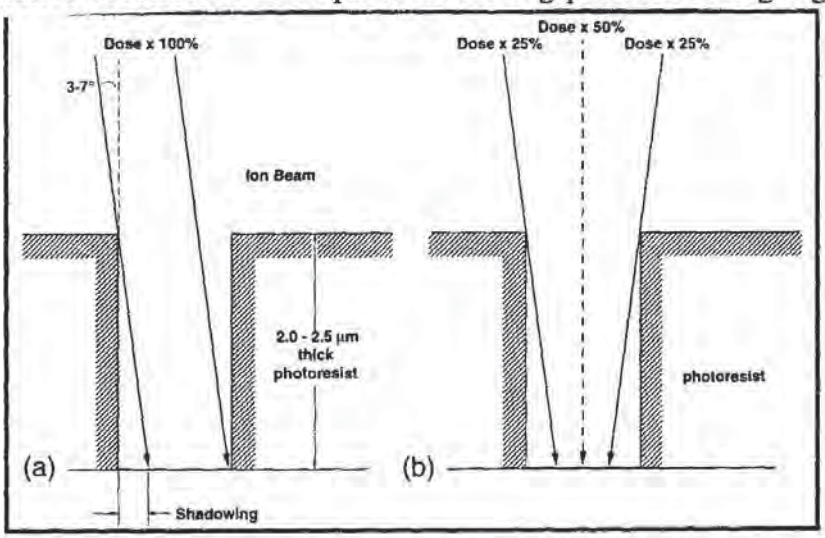


Fig. 5-6 The geometric effects of ion implantation into a narrow active region: a) low-tilt-angle shadowing and well misalignment; b) low-tilt quad implant provides both lateral and vertical (no channeling) uniformity.

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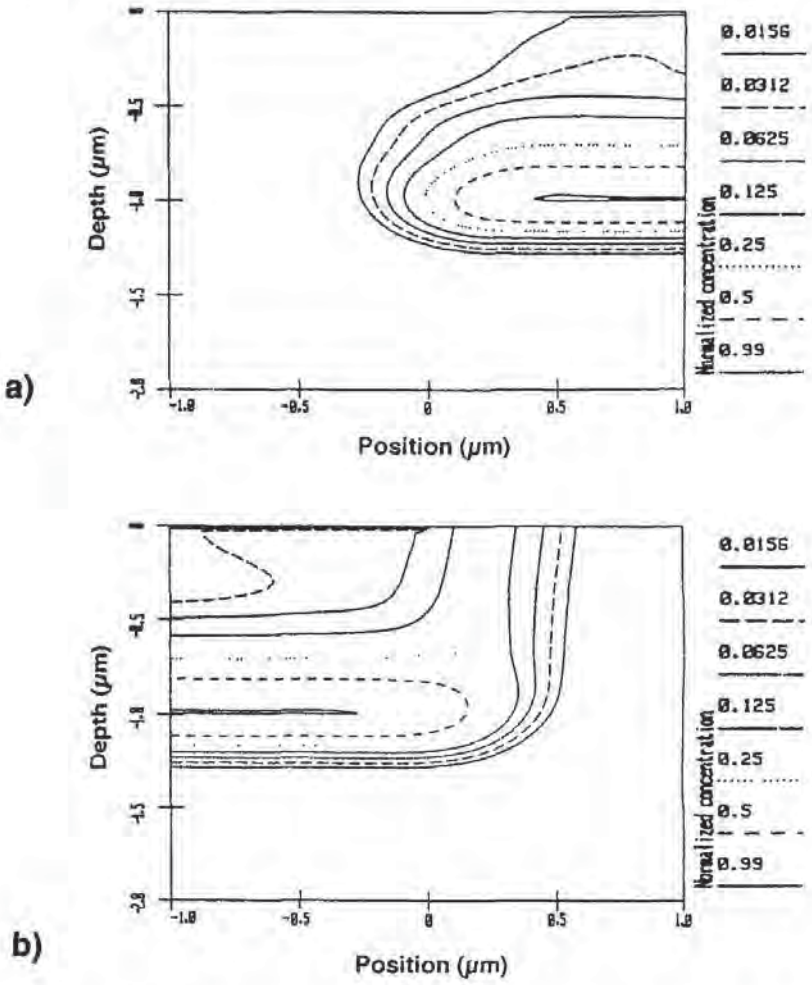


Fig. 5-7 Normalized doping profile of 1 MeV phosphorus implantation. a) On the shadow side (a) a lowly doped bulge is found (according to Monte Carlo simulation). b) On the incoming side, Monte Carlo simulation shows a trunk.[8]

7°-tilt implants is to reposition the wafers part-way through the implant process. If the wafers are repositioned four times, and 25% of the total dose is implanted with the wafer in each position (*quad implant*), all the areas of the exposed silicon surface will receive the same implant dose, eliminating the implant-shadowing problem (Fig. 5-6b). That is, well profiles are symmetric, both laterally and vertically, and shadowing effects near the surface are compensated.

A high-energy batch-implanter capable of performing low-tilt quad-implants without unloading the wafers from the disk addresses the isolation scaling problem with high productivity. Since it is not practical to scan a high-energy ion beam, implanters with fixed beams and batch end-stations using simultaneous disk spinning and scanning is the method-of-choice for process uniformity. The

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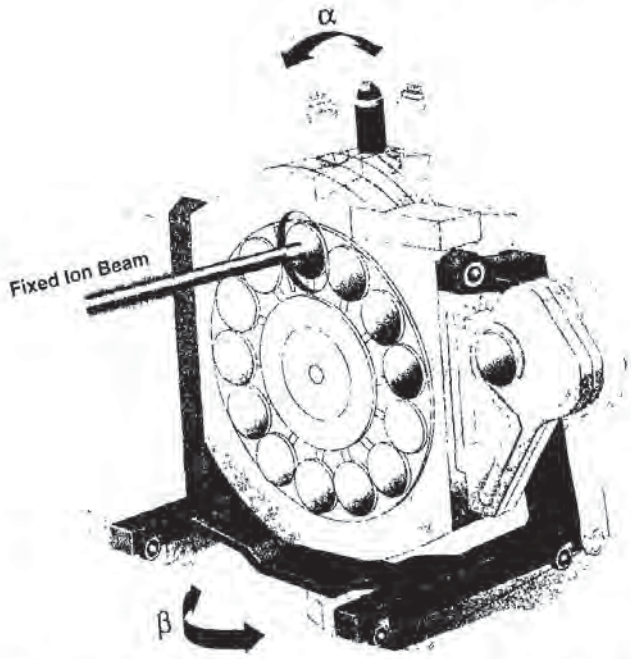


Fig. 5-8 *In situ* quad implants can be run on a batch end-station with orthogonal tilt axes (designated α and β).

quad-implant capability is achieved with a disk chamber as shown in Fig. 5-8.[9] Here the disk can be independently tilted in two orthogonal directions. Such batch high-energy implanters are sold by Axcelis Corp. Single-wafer high-energy implanters are also commercially available. A model offered by Applied Materials also permits tilting the wafer and repositioning it several times during an implant step. Higher tilt-angle control is claimed for such single-wafer high-energy implanters compared to the batch types.[10]

5.2 SUPERSTEEP RETROGRADE (SSR) CHANNEL DOPING PROFILES

The appropriate choice of substrate doping and engineering of doped layers under the gate are critical to optimum performance of deep-submicron MOSFETs (with respect to drain-to-source punchthrough, threshold voltage, and channel mobility). Specifically, the doping-density in the region between the source and drain must increase as the gate-length is reduced to prevent punchthrough. As shown in Fig. 5-9, the mean channel-doping-density needed to control punchthrough when gate lengths scale below about 0.13-μm begins to exceed $5x10^{17}/cm^3$. However, to avoid reduction of carrier mobility in the channel, the doping at the surface must be kept below $5x10^{17}/cm^3$ to obtain the universal mobility curve.[11] To allow the surface concentration to be kept below this value, and still have a mean doping concentration in the channel above this number, a vertical *retrograde doping concentration profile* is needed in the channel region.

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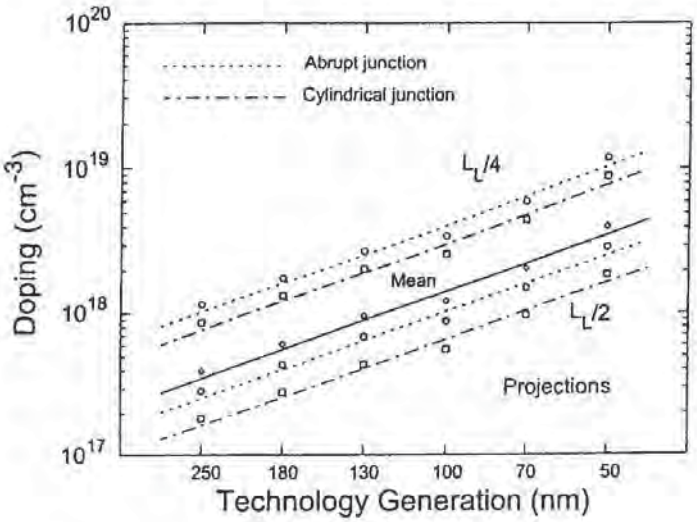


Fig. 5-9 Doping density required for punchthrough control.[11]

Assume that a lighter doped surface layer with a concentration of $1x10^{17}/cm^3$ exists down to a depth X_I (taken to be approximately 1/2 of the source/drain junction depth X_j), and that at that depth the doping abruptly changes to the value needed for the heavily doped punchthrough-control layer. Figure 5-10 shows the scaling required for X_I at each technology generation. Because the transition in doping concentration from the lighter doped region near the surface to the heavily doped punchthrough-control region below must occur over such a short distance, the gradient in the doping concentration must be very steep. Hence, such a doping concentration profile is termed a *super-steep retrograde* (SSR) profile.

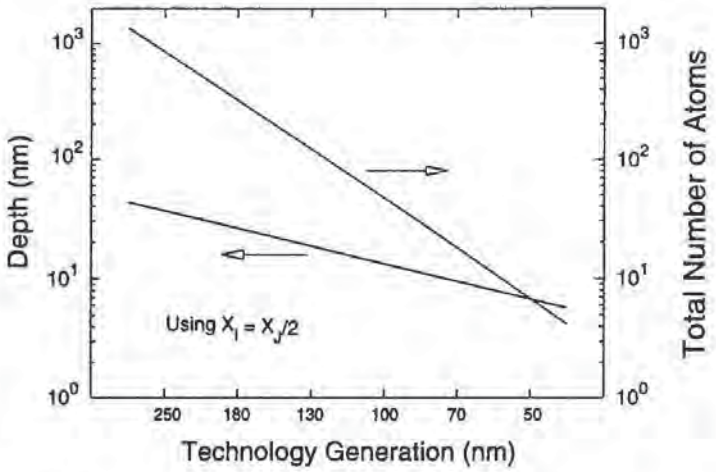


Fig. 5-10 Typical thickness of lighter-doped layer and total number of impurity atoms for $10^{17}/cm^3$ surface doping density.[11]

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The formation of SSR channel-doping-profiles for technology nodes from 0.18-μm down to about 0.1-μm is done using ion implantation (in place of the conventional V_T-adjust implant step). In these implant processes, however, higher-mass dopants are substituted for the dopants typically used to carry out the V_T–adjust implants. That is, indium (In) is used instead of boron (B) for the NMOS devices, and either arsenic (As) or antimony (Sb) replace phosphorus (P) in PMOS devices. Heavier implant species provide steeper as-implanted profiles (due to their smaller straggle), and the heavier ions have reduced diffusivity (keeping the as-implanted profile from spreading out during subsequent thermal processes). Thus, well-profiles implanted with In and As (using implant energies in the 100-200-keV range) can be fabricated with sufficiently low doping ($\sim 5 \times 10^{16}/cm^3$) at the gate-oxide interface, and a higher peak doping level ($\sim 1 \times 10^{18}/cm^3$) 80-nm below the gate oxide. (Note that peak doping concentrations of indium cannot be made higher than about $10^{18}/cm^3$ because of the solubility limit of indium atoms in silicon.)

Figure 5-11a shows indium doping-profiles for various annealing temperatures, up to 1000°C.[12] It is evident that little change occurs in the as-implanted indium doping profile for annealing temperatures up to 1000°C, making it a promising candidate for forming SSR channel-doping-profiles. Indium implants for retrograde-channels in NMOSFETs have been reported in some cases to *improve* subthreshold-slopes relative to conventional boron implanted-channels,[12,13] while in another case it was found to have *degraded* the subthreshold-slope.[14] It is generally agreed that SSR doping-profiles are effective at reducing short-channel-effects and drain-induced-barrier-lowering, but it is not equally certain whether this translates into overall improvement in device performance (as this also depends on many other variables, including gate-oxide-thickness, gate-length, and junction-doping). Figures 5-11b and 11c, respectively, show the vertical concentration-doping-profile for an SSR and a conventional process for PMOSFETs (Sb for SSR, and P for the conventional process), and NMOSFETs (indium for SSR, and boron for the conventional process).[15]

The use of SSR channel-doping-profiles is entering some mainstream process flows, despite disagreements over their advantages compared to conventional channel-profiles. In late 1999, the successful fabrication of 100-nm-gate-length devices was reported. They were built using SSR channel-profiles, source/drain-extensions, and deep source/drain-regions for contact. A 100-nm-process yielded devices with 1.04-mA/μm (NMOS) and 0.46 -mA/μm (PMOS) on-currents at 1.5 V with 3-nA/μm off-current. This process uses indium and arsenic as the implant

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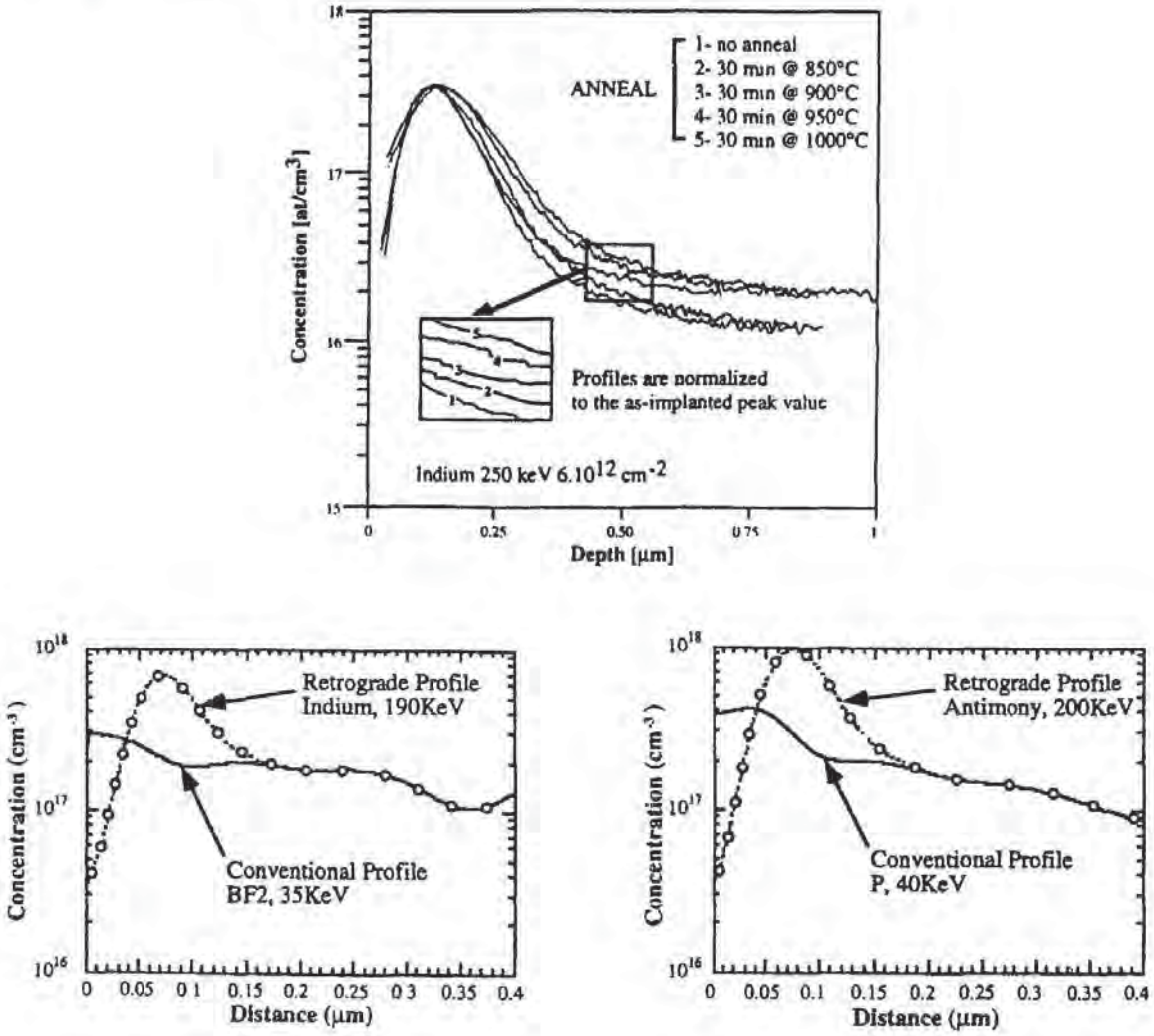


Fig. 5-11 a) SIMS data of indium profiles over a large range of annealing temperatures. Conventional and retrograde doping profiles (simulated) for b) NMOS and c) PMOS .[12]

species for the SSR-channel-doping-profiles, low-energy boron and arsenic source/drain-extensions, and high-angle pocket-implants.[16]

The source for indium ions in implant processes is $InCl_3$, a solid material at room temperature. The production of ion beams from solid $InCl_3$ presents some special challenges for ion implanters. First, $InCl_3$ is hygroscopic (i.e., it readily absorbs moisture), and thus may require excessive outgassing if not handled properly outside of the ion-source vaporiser. In addition, although $InCl_3$ is a solid, it has a low melting-point. Thus, indirect heating from a second vaporiser in the ion-source may cause unintentional vaporization. Both of these effects can lead to premature loss of the source charge, as well as the problem of indium

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coating in and around the source area. Finally, even during normal operation, indium tends to drift down the beamline, covering the beamline components. This creates a risk of cross-contamination, since the indium atoms can be dislodged from these surfaces if they are struck by ion beams of other species.

Two ion-implanter features can adequately suppress such effects. First, active cooling in the source eliminates indirect heating, decreasing indium-loss and excess beamline-coating. Second, an electrostatic (or other) filtering element near the end-station greatly reduces the magnitude of such cross-contamination, allowing all species to be run on a single implanter. The latest generations of single-wafer, medium-current-implanters incorporate such features.[17]

5.2.1 Fabricating SSR Profiles for Sub-0.1 μm MOSFETs

When gate-lengths scale below 0.1-μm, it probably will no longer be possible to create SSR channel-doping-profiles using ion implantation (even if In and As are used as the implanted species). For example, if a lightly-doped surface-layer is established for a 50-nm-generation MOSFET (with a doping concentration of $1x10^{17}/cm^3$), the heavily-doped punchthrough-control layer ($10^{19}/cm^3$) will have begin at a depth of just 7-nm beneath the silicon surface. Since the width of the surface-inversion-layer is typically thinner than 7-nm, the channel electrons will still be located primarily in the lightly-doped surface-region. However, thin surface-layers with such an abrupt doping-concentration-increase cannot be fabricated with ion implantation (and its ancillary annealing processes). Other doping techniques, such as low-temperature selective-epitaxy (of perhaps Si-Ge layers[19]) will likely be needed for 50-nm and beyond MOSFETs.*

5.3 SOURCE/DRAIN ENGINEERING IN DEEP-SUBMICRON CMOS

In deep-submicron MOSFETs, the typical source/drain contact-structures consist of two regions: **1**) A shallow source/drain-extension-region (SDE), with a junction-depth X_j; and **2**) A deeper contact-source/drain-region, with a junction-depth X_{jC}. As also described in Chap. 1, when MOSFETs were first designed with such two-region source/drain-structures, the first-region had lighter doping than the second-region (and it was in fact called a *lightly-doped drain* (*LDD*) re-

* Figure 5-10 also shows a graph of N_T (the total number of impurity atoms in the lightly doped layer) versus technology generation. For 50-nm and below, this value approaches a small number (< 10), so that for cases where the doping density is important to device operation, any device parameter depending strongly on N_T will show large statistical fluctuations from device-to-device. If all parameters depend only very weakly on N_T then the layer may as well be undoped,[18] so that V_T-control relates to the positioning of the step (i.e., the increase in doping) and the doping in the heavily doped layer.

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gion. This region was added to the single-region MOSFET drain-structures at about the time when MOSFETs were scaled below 1.5-μm. Its function was to reduce the peak electric-field (and thus hot-electron-injection) near the drain-end of the channel. However, as MOSFETs gate-lengths were scaled to the deep-submicron regime, the power-supply voltages also had to be reduced, and this resulted in a significant decrease in the peak electric-field near the drain. Hence, the LDD region was no longer needed to suppress hot-carrier-injection effects.

However, in deep-submicron MOSFETs the SDE-region remains a part of the drain structure. But, its role now is to reduce short-channel-effects. The drain contact-region is required to accommodate the thickness of the salicide contact-layer and minimize junction-leakage. Nevertheless, the junction depth X_{jC} of the contact-region should not be larger than that needed to meet these conditions. That is, the greater the junction-depth, the larger must be the width of the sidewall-spacer. This, in turn, will result in a longer SDE-region (which increases the value of the parasitic SDE-resistance, R_{SDE}). In Sect 5.3.1.3, we will see that to enable a MOSFET to deliver improved performance as the gate length is scaled, it is critical that the source/drain contact design should minimize both the parasitic series-resistance-effects and the salicide-substrate contact-resistance. In addition, to ensure that short-channel-effects are effectively controlled as the MOSFET is scaled, both X_j and X_{jC} will also have to appropriately scaled,.

Figure 5-12 shows the depths of the source/drain-region junctions and undoped channel-region as MOSFETs are scaled below 200-nm (where L_L is the lithographically-drawn gate-length), as taken from the ITRS 1999 study.[20] The design rules used in ITRS 2001 to calculate these same values have been relaxed slightly from those in the 1999 study: **1**) the source/drain-contact junction-depth is 1.1 L_L (±33%), compared to 0.8 L_L; **2**) the source/drain-extension junction-depth is 0.55 L_L (±25%), compared to 0.4 L_L; and **3**) the undoped region near the Si/gate-oxide interface in a super-steep retrograde doped channel (SSR) is 0.3 L_L (±25%), compared to 0.2 L_L. Creating and maintaining these ultra-shallow junctions remains a fundamental challenge for doping and metrology techniques.

In this section we will discuss two subjects related to the formation of the source/drain-structure in deep-submicron MOSFETs, namely: **1**) the issues involved in keeping the value of the resistance of the drain region R_S (which is the sum of the parasitic resistance components and contact resistance), to a value that is sufficiently low to meet the requirements of scaled-MOSFET device-design, and **2**) the process technology needed to form shallow SDE-junctions.

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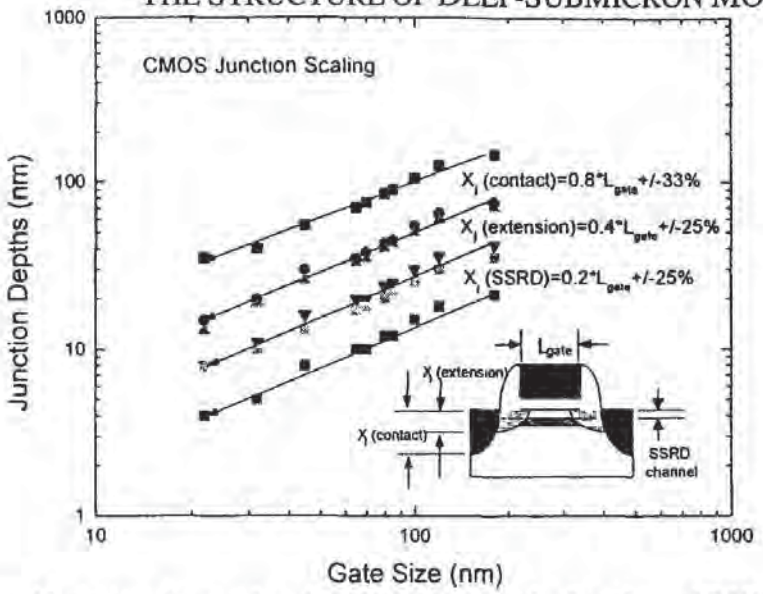


Fig. 5-12 Source/drain junction and undoped-channel depths for planar CMOS on bulk-Si.

5.3.1 Resistance of Deep-Submicron Source/Drains

In the planar MOSFET, the device-region in which transistor-action occurs is the *channel* under the gate. The current coming from the metal-interconnect lines must flow from the metal-Si-contact to the edge of the channel through the source or drain regions (Fig. 5-13). In the MOSFET, current enters the contact perpendicular to the wafer-surface, and then travels parallel to the surface in order to reach the channel. The total parasitic series-resistance, R_S, of the current path from the contact to the edge of the channel of a single-region drain (i.e., one

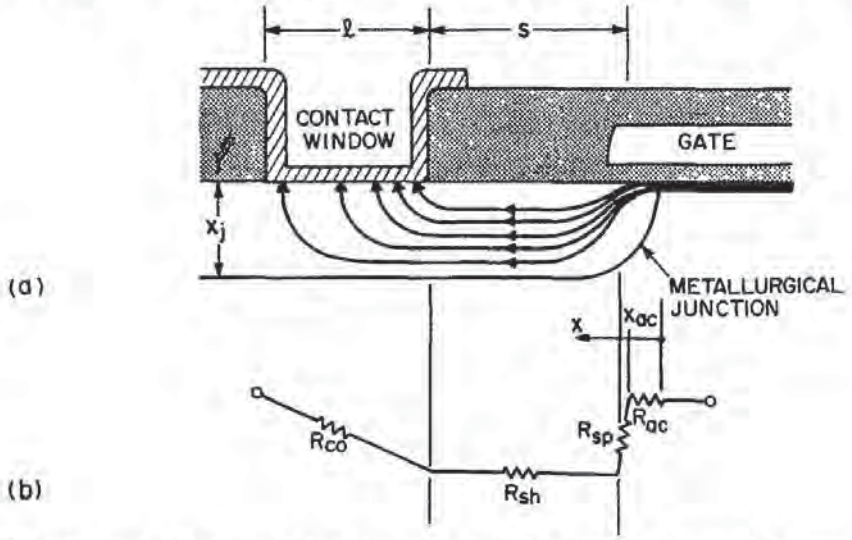


Fig. 5-13 Schematic drawing showing: a) current paths within the source and drain regions, of a planar MOSFET and; b) their corresponding representative series resistance components.[21] (© 1987 IEEE).

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that does not have an LDD or a SDE) can be modeled by the sum of four components;[21]

$$R_S = R_{co} + R_{sh} + R_{sp} + R_{ac} \quad \textbf{(5.1)}$$

where R_{co} is the *contact resistance* between the metal and the source/drain region, R_{sh} is the *sheet resistance* of the bulk region of the source and drain, R_{sp} describes the *resistance of the current lines crowding near the channel end of the source*, and R_{ac} is the *accumulation-layer resistance*.

If the MOSFET drain has an SDE, the R_{sh} component of R_S can be replaced by R_{SDE}, as indicated in Fig. 5-14, so that R_S is now given by:

$$R_S = R_{co} + R_{SDE} + R_{sp} + R_{ac} \quad \textbf{(5.2)}$$

In any case, the value of R_S must be viewed from the perspective of how it affects the performance of a MOSFET. Specifically, its value must be compared to that of the channel-resistance R_{sat} of the MOSFET in its ON state:

$$R_{sat} = V_{DD}/I_{Dsat} \quad \textbf{(5.3)}$$

When the external resistance of the source + drain regions is equal to approximately 10% of the value of R_{sat}, the saturation-drain-current I_{Dsat} is reduced by about 8%. In most MOSFET design approaches, the goal is to keep I_{Dsat} from being reduced by no more than 10% due to such series-resistance of the source and drain regions. Thus, it is useful to analyze the components of R_S, so that it can be understood what factors can be adjusted to keep the value of R_S to the value which will meet the I_{Dsat}-degradation design goal.

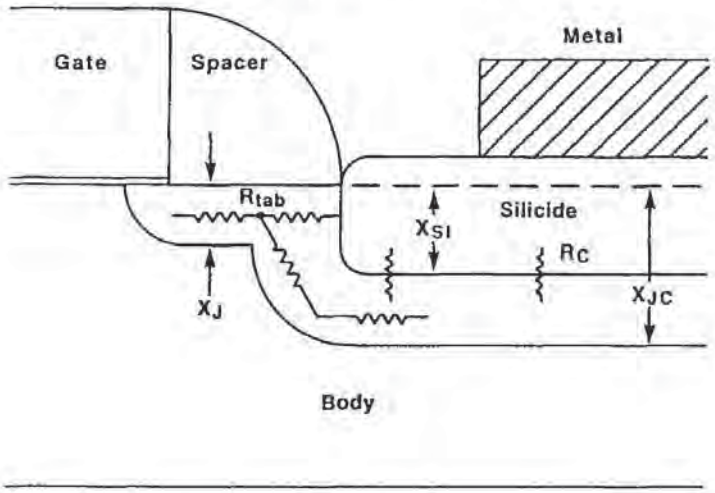


Fig. 5-14 Schematic drawing of the components of source or drain resistance in a deep-submicron MOSFET.

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For future scaling, the value of R_{sat} (actually $R_{sat}W$, normalized per unit device width) is given by:

$$R_{sat}W \cong V_{DD}t_{ox}/(0.47v_{sat}\varepsilon_{ox}\,[V_{DD} - V_T]) \cong t_{ox}/(0.376v_{sat}\varepsilon_{ox}) \qquad \textbf{(5.4)}$$

Equation 5-4 indicates that since t_{ox} will continue to be made smaller as MOSFETs are scaled, the value of $R_{sat}W$ will also decrease as the devices are scaled. This implies that the value of R_S will also have to be made lower with each technology node. Before we examine in detail the implications of a decreasing R_{sat} (and therefore also a decreasing R_S), we first need to give a more thorough discussion of the physical meaning of the parasitic resistance components of the drain contact region, namely R_{ac}, R_{sp}, and R_{SDE}.

5.3.1.1 Physical Meaning of R_{ac}, R_{sp}, and R_{SDE}: Let us discuss the physical origins of the three parasitic resistance components of the drain/source-regions, with respect to deep-submicron NMOSFET structures. Figure 5-15 depicts the doping gradient of an n^+-p junction at the source (or drain) end of an NMOSFET. The dotted lines indicate contours of constant doping concentration. We define the end of the MOSFET channel as the location where the metallurgical junction occurs (i.e., where $N_D = N_A$ at the surface). When the MOSFET is turned ON, an inversion layer is induced along the length of the channel (i.e., in the substrate-region - where for this NMOSFET the doping is p-type). However, because the gate is an equipotential region, the positive bias needed to turn the MOSFET ON, will have a different effect on the silicon region under the gate if it is doped n-type. That is, in the region where the *drain doping* overlaps under the gate edge, an accumulation-layer (instead of an inversion-layer) is formed (dark region in Fig. 5-15).

The length of the accumulation-region is determined by the point where the induced (accumulated) carrier-concentration at the surface equals the background doping level. For example, a typical bias induces ~10^{19}/cm^3 carriers in the accumulation layer while the maximum doping level in the source/drain region is in the 10^{20}-10^{21}/cm^3 range. Therefore, the accumulation-layer has a more negligible effect in the more heavily doped region of the drain (i.e., further away from the channel edge). Nevertheless, there is still a component of resistance due to the resistance of the accumulation-layer in series with the channel-ON-resistance, and this component is referred to as the accumulation-resistance, R_{ac}. Both the accumulation-layer and the inversion-layer have about the same thickness (which is given by X_C,and to which we will refer again in the discussion on R_{sp}). *In any case, for deep-submicron MOSFETs, the length of the accumulation-layer is so short, that R_{ac} does not play a significant role in causing the value of R_S to*

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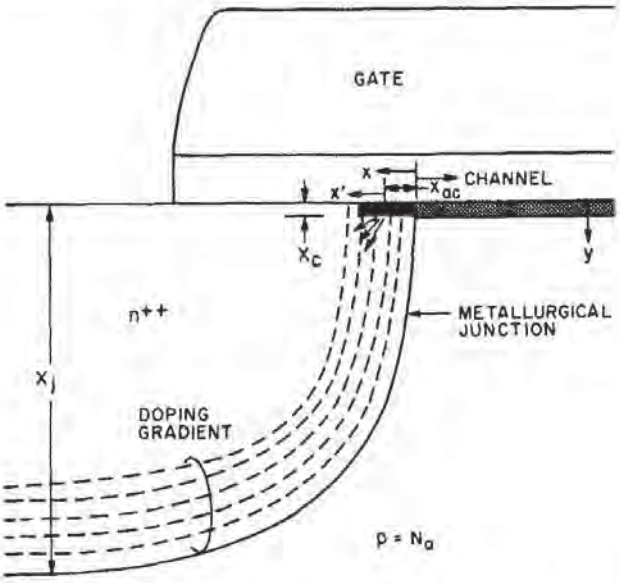


Fig. 5-15 Details of structures near the vicinity of the channel end. The dotted lines are contours of constant concentration. Dark region represents the accumulation layer.[21] (© 1987 IEEE).

rise as the devices are scaled. Hence, we will not consider this component any further in discussing the problem of the increase in R_S as the MOSFET is scaled.

Let us consider R_{sp} next, as this parasitic resistance component does play a role in the increase of R_S as the devices are scaled in the deep-submicron regime. Qualitatively, for a non-abrupt junction (i.e., where the doping contours are spaced over some finite distance, as depicted in Fig. 5-15), R_{sp} arises because after leaving the channel, the current does not immediately spread into the bulk of the source-drain regions (where the resistance effect is given by R_{SDE}). Instead, the carriers leave the accumulation layer and spread out as they move from the thin accumulation layer into the (laterally) uniformly-doped SDE-region of the source or drain SDE (Fig. 5-16).[22] This resistance component is called the spreading resistance, R_{sp}.

An analytical approximation for calculating the value of R_{sp} is given by:

$$R_{sp} \sim (2\rho/\pi W) \ln (\beta X_j/X_C) \qquad \textbf{(5.5)}$$

where ρ is the resistivity of the SDE-region, and X_C is the inversion-/accumulation-layer thickness, and β is a constant that varies from 0.37 to 0.9 (depending on the method of derivation). For the purpose of this discussion, an intermediate value of 0.58 will be used.[21]

The value of the series-resistance component R_{SDE} of the SDE-region as shown in Fig. 5-14 can be estimated from (i.e., $R = \rho l/A$):

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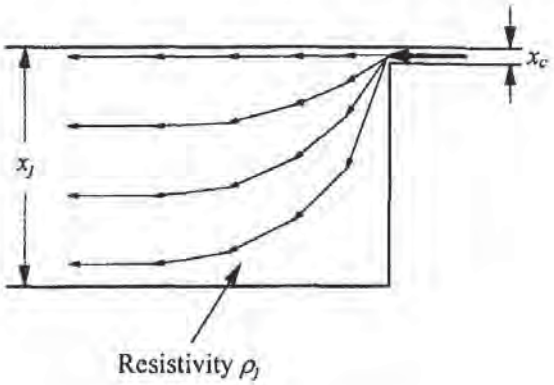


Fig. 5-16 Schematic diagram showing the resistance component associated with the injection region where the current spreads from a thin surface layer into a uniformly doped source or drain region.[22] (© 1983 IEEE)

$$R_{SDE} \cong \rho\, l_{SDE}/(WX_j) \qquad \textbf{(5.6)}$$

Without resorting to a two-dimensional analysis to calculate the length of the SDE region l_{SDE}, a reasonable estimate of its value is $L_L/2$ (where L_L is the lithographically drawn gate-length). Thus, since $X_j \sim 0.55\, L_L$ (as described in the introduction of this section), with scaling the ratio of l_{SDE} to the SDE junction-depth X_j will remain approximately 1.2.

The sum of R_{sp} and R_{SDE} will give the value of the parasitic series resistance component of the SDE region of the drain contact structure. That is, when Eq. 5.5 and 5.6 are added together we get:

$$(R_{sp} + R_{SDE})W \equiv \rho\,(l_{SDE}/X_j)\left[1 + (2X_j/\pi\, l_{SDE})\ln(\beta X_j/X_C)\right] \qquad \textbf{(5.7)}$$

From Eq. 5-7 it can be seen that, in effect, R_{sp} multiplies the resistance of the SDE region by the quantity given in the brackets of Eq. 5-7. This quantity is expected to range from a factor of 2.09 at the 250-nm generation to about 1.48 at the 50-nm generation, which indicates the R_{sp} plays a significant role in the parasitic resistance of deep-submicron MOSFETs, and it would be beneficial if methods could be developed that could reduce its value.

5.3.1.2 Comparing the Resistance of the SDE Region (R_{sp} + R_{SDE}) to R_{sat}: With the equations derived in Sect. 5.3.1.1 it becomes possible to estimate the values of (R_{sp} + R_{SDE}) that will be required for MOSFETs scaled down to 50-nm. (Note that this analysis was adapted from Ref. 23.) The center curve of Fig. 5-17 shows the calculated values of the channel resistance $R_{sat}W$ (in Ω-cm) of MOSFETs from the 0.25-μm (250-nm) node down to the 50-nm node. The upper and lower curves show what the value of $20(R_{sp} + R_{SDE})W$ would be if the SDE region had sheet resistance values of 500-Ω/sq and 1000-Ω/sq, respectively. Note that

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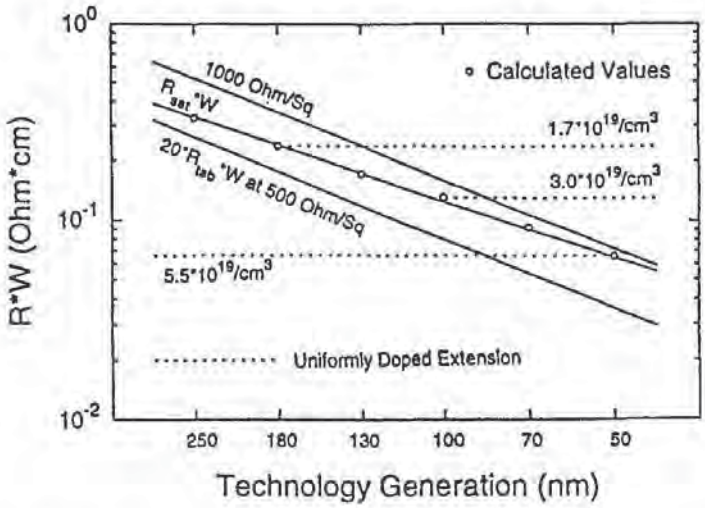


Fig. 5-17 Allowed values of drain (or source) extension resistance considering both bulk extension resistance R_{SDE} and extension spreading resistance R_{sp}.[23]

values are shown for *n*-channel devices, *p*-channel devices would be about 20% higher. In addition, $20(R_{sp} + R_{SDE})W$ is used because the source and drain contact regions each contribute to the resistance in series with $R_{sat}W$.

The data in Fig. 5-17 indicates that the sheet resistance values of $(R_{sp} + R_{SDE})$ will need to be about 650-Ω/sq for 250-nm MOSFETs and about 900-Ω/sq for 50-nm MOSFETs if the value of $20(R_{sp} + R_{SDE})W$ needed to limit the degradation in I_{Dsat} to 8-10% is to be achieved. However, since the junction-depths of the SDE-regions decrease as the gate-lengths are reduced, in order to keep the sheet-resistance-values in the 650-900-Ω/sq range, the average doping-densities in the SDE-regions will have to be increased. As shown in Fig. 5-17, the peak values of doping will have to exceed $10^{19}/cm^3$ (e.g., for the 50-nm node, the peak doping will have be $5.5x10^{19}/cm^3$).

By 2001 it was determined that junctions whose depth was 35-nm could be fabricated with 0.5-keV implants and spike-anneals, but that this was about as low as could be practically achieved (see Sect. 5.3.3). Thus, for 0.1-μm technologies, it will be possible to fabricate SDE-regions with adequately shallow junctions and sufficiently low-values of sheet-resistance. However, it is not clear if it will be possible to do this for 50-nm devices, since the junction-depth will have to decreased to about 20-25-nm, and this will mean that the sheet resistance will have to be significantly increased above 350-Ω/sq.

Also note that the model for R_{sp} given by Eq. 5-5 does not include the effect of the steepness of the lateral-doping-concentration-gradient of the SDE-implant.

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