

Filed on behalf of:

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Petitioner

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UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNITED MICROELECTRONICS CORPORATION,
AND
UMC GROUP (USA),
Petitioner,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,
Patent Owner.

Case IPR2025-01079
U.S. Patent No. 7,923,764

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT U.S. PATENT No. 7,923,764
UNDER 35 U.S.C. §§ 311, 312 AND 37 C.F.R. § 42.104**

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EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 7,923,764 to Hirase, et al. (“the ’764 patent”)
1002	File History of U.S. Patent No. 7,923,764 (“’764 File History”)
1003-1008	RESERVED
1009	U.S. Patent Application Publication No. 2003/0025135 A1 to Matsumoto, et al. (“Matsumoto”)
1010	JP2003-258241 to Kajiyama (“JP-Kajiyama”)
1011	Certified Translation of JP2003-258241 to Kajiyama (“Kajiyama”)
1012	U.S. Patent Application Publication No. 2006/0131672 A1 to Wang, et al. (“Wang”)
1013	U.S. Patent Application Publication No. 2005/0051856 A1 to Ono, et al. (“Ono”)
1014-1017	RESERVED
1018	Wilk, G. D., et al., “High-k gate dielectrics: Current status and materials properties considerations,” Journal of Applied Physics, Vol. 89, No. 10, pp. 5243-5275, May 15, 2001 (“Wilk”)
1019	U.S. Patent Application Publication No. 2005/0045938 A1 to Mutou, et al. (“Mutou”)

Exhibit No.	Description
1020-1023	RESERVED
1024	Sim, J. H., et al., “Effects of ALD HfO ₂ thickness on charge trapping and mobility,” <i>Microelectronic Engineering</i> , Vol. 80, pp. 218-221, June 17, 2005 (“Sim”)
1025	U.S. Publication 2004/0110352 to Bu, et al. (“Bu”)
1026-1051	RESERVED
1101	Declaration of Sanjay Banerjee, PhD
1102	Curriculum Vitae of Sanjay Banerjee, PhD
1103	“Stress Memorization Technique (SMT) by Selectively Strained-Nitride Capping for Sub-65nm High-Performance Strained-Si Device Application,” Chen et al., 2004 Symposium on VLSI Technology Digest of Technical Papers (2004) (“Chen-2004”)
1104	“35% Drive Current Improvement from Recessed-SiGe Drain Extensions on 37 nm Gate Length PMOS,” Chidambaram et al., 2004 Symposium on VLSI Technology Digest of Technical Papers (2004) (“Chidambaram-2004”)
1105	“Self-Aligned Ultra Thin HfO ₂ CMOS Transistors with High Quality CVD TaN Gate Electrode,” Lee et al., 2002 Symposium On VLSI Technology Digest of Technical Papers (2002) (“Lee-2002”)
1106	“Delaying Forever: Uniaxial Strained Silicon Transistors in a 90nm CMOS Technology,” Mistry et al., 2004 Symposium on VLSI Technology Digest of Technical Papers (2004) (“Mistry-2004”)

Exhibit No.	Description
1107	“Effects of High-Temperature Forming Gas Anneal on HfO ₂ MOSFET Performance,” Onishi et al., 2002 Symposium On VLSI Technology Digest of Technical Papers (2002) (“Onishi-2002”)
1108	“Low Standby Power CMOS with HfO ₂ Gate Oxide for 100-nm Generation,” 2002 Symposium On VLSI Technology Digest of Technical Papers (2002) (“Pidin-2002”)
1109	“Mobility Enhancement in Strained Si NMOSFETs with HfO ₂ Gate Dielectrics,” Rim et. al., 2002 Symposium On VLSI Technology Digest of Technical Papers (2002) (“Rim-2002”)
1110	“Metal Gate MOSFETs with HfO ₂ Gate Dielectric,” Samavedam et al., 2002 Symposium On VLSI Technology Digest of Technical Papers (2002) (“Samavedam-2002”)
1111	“55nm high mobility SiGe(:C) pMOSFETs with HfO ₂ gate dielectric and TiN metal gate for advanced CMOS,” Weber et al., 2004 Symposium on VLSI Technology Digest of Technical Papers (2004) (“Weber-2004”)
1112	Japanese Patent Publication JP2005-064190 to Ono (with English Abstract and Japanese Publication) (“JP-Ono Abstract”)
1113-1210	RESERVED
1211	Van Zant, “Microchip Fabrication”(Fifth Ed. 2004) (“Van Zant”)
1212	RESERVED

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Exhibit No.	Description
1213	Houssa, M., “High-k Dielectrics”to Houssa (IOP Publishing Ltd. 2004) (Houssa)
1214-1215	RESERVED
1216	“International Technology Roadmap for Semiconductors: Process Integration, Devices, and Structures”(2007 Edition) (“ITRS-PIDS”)
1217-1222	RESERVED
1223	“Semiconductor Devices: Physics and Technology” by Sze (Second Edition, 2002) (“Sze-2002”)
1224-1225	RESERVED
1226	U.S. Patent No. 7,709,331 to Karve, et al. (“Karve”)
1227	U.S. Patent No. 8,017,469 to Luo, et al. (“Luo”)
1228	RESERVED
1229	Wolf, “Silicon Processing for the VLSI Era, Volume 3 – The Submicron MOSFET”(1995) (“Wolf-3”)
1230-1304	RESERVED
1305	Translated Excerpts from JP File History
1306-1322	RESERVED
1323	U.S. Patent No. 6,306,712 to Rodder, et al. (“Rodder”)

Exhibit No.	Description
1324-1325	RESERVED
1326	Declaration of June Ann Munford
1327-1328	RESERVED
1329	Koyama, M., et al., “Effects of Nitrogen in HfSiON Gate Dielectric on the Electrical and Thermal Characteristics,” Digest of International Electron Devices Meeting, pp. 849-852, Dec. 8-11, 2002 (“Koyama”)
1330-1332	RESERVED
1333	Plummer, J., et al., “Silicon VLSI Technology: Fundamentals, Practice and Modeling” (Prentice Hall 2000) (“Plummer”)
1334	Wolf, S., “Silicon Processing for the VLSI Era, Volume 4 – Deep-Submicron Process Technology” (Lattice 2002) (“Wolf-4”)
1335-1336	RESERVED
1337	Lee, S. J., et al. “High Quality Ultra Thin CVD HfO ₂ Gate Stack with Poly-Si Gate Electrode,” Digest of International Electron Devices Meeting, pp. 31-34, Dec. 10-13, 2000 (“Lee”)
1338	Campbell, “The Science and Engineering of Microelectronic Fabrication”, Second Edition (2001) (“Campbell”)
1339	RESERVED
1340	Japanese Patent Publication JP2005-064190 to Ono with certified translation (“JP-Ono”)

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Exhibit No.	Description
1341	N. Weste and D. Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, Third Edition (Pearson/Addison Wesley, 2005) (“Weste”)
1342-1348	RESERVED
1349	Lee, B.H., et al., “Ultrathin Hafnium Oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application,” Digest of International Electron Devices Meeting, pp. 133-36, Dec. 5-8, 1999 (“Lee-1999”)
1350	U.S. Patent Application Publication No. 2005/0040479 to Koldiaev, et al. (“Koldiaev”)
1351	RESERVED
1352	Albertin, K.F., et al., “Study of PECVD SiO _x Ny films dielectric properties with different nitrogen concentration utilizing MOS capacitors,” Microelectronic Engineering, Vol. 77, pp. 144-49 (2005) (“Albertin”)
1353-1405	RESERVED
1406	U.S. Patent Application Publication No. 2007/0249069 A1 to Alvarez et al. (“Alvarez”)
1407-1412	RESERVED
1413	S.M. Sze, Physics of Semiconductor Devices (2d ed. 1981) (excerpted) (“Sze-1981”)
1414-1418	RESERVED

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Exhibit No.	Description
1419	U.S. Patent Application Publication No. 2006/0286729 A1 to Kavalieros et al. ("Kavalieros729")
1420-1428	RESERVED
1429	U.S. Patent Application Publication 2004/0262784 A1 to Doris et al. ("Doris")
1430	U.S. Patent No. 6,797,556 B2 to Murthy et al. ("Murthy556")
1431	U.S. Patent Application Publication No. 2007/0134870 A1 to Lee et al. ("Lee870")
1432	U.S. Patent Application Publication No. 2005/0260810 A1 to Cheng et al. ("Cheng810")
1433	U.S. Patent Application Publication No. 2009/0020820 A1 to Baik et al. ("Baik")
1434	U.S. Patent Application Publication No. 2008/0293207 A1 to Koutny et al. ("Koutny")
1435	U.S. Patent Application Publication No. 2010/0075476 A1 to Miyashita ("Miyashita")
1436-1505	RESERVED

Exhibit No.	Description
1506	U.S. Patent Application Publication 2007/0235823 A1 to Hsu et al. ("Hsu823")
1507-1511	RESERVED
1512	International Technology Roadmap for Semiconductors: Front End Processes (2007 ed.) ("ITRS_FEP")
1513-1514	RESERVED
1515	U.S. Patent Application Publication No. 2006/0022277 A1 to Kavalieros et al. ("Kavalieros277")
1516	K. Mistry, et al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging," Technical Digest of the of the 2007 IEEE International Electron Devices Meeting (IEDM), pp. 247-50 (Dec. 2007) ("Mistry2007")
1517	K. Mistry, et al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging," presented at 2007 IEEE International Electron Devices Meeting (IEDM), pp. 1-37 (Dec. 2007) ("Mistry_Presentation")
1518	U.S. Patent No. 6,881,631 B2 to Saito et al. ("Saito631")
1519	U.S. Patent No. 7,812,414 B2 to Hou et al. ("Hou")

Exhibit No.	Description
1520	U.S. Patent Application Publication No. 2005/0258468 A1 to Colombo et al. ("Colombo")
1521	U.S. Patent No. 6,849,511 B2 to Iriyama et al. ("Iriyama")
1522	U.S. Patent Application Publication No. 2002/0037615 A1 to Matsuo ("Matsuo")
1523	S.E. Thompson et al., "A 90-nm Logic Technology Featuring Strained Silicon," IEEE Transactions on Electron Devices, vol. 51. No. 11, pp. 1790-97 (Nov. 2004) ("Thompson-2004")
1524	Y. Sun et al., "Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors," Journal of Applied Physics, vol. 101, Art. No. 104503 (22 pages) (May 2007) ("Sun-2007")
1525	D. James, "2004 –The Year of 90-nm: A Review of 90 nm Devices," 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 72-77 (2005) ("James")
1526	U.S. Patent Application Publication No. 2006/0148151 A1 to Murthy et al. ("Murthy151")
1527	U.S. Patent Application Publication No. 2004/0262683 A1 to Bohr et al. ("Bohr")

Exhibit No.	Description
1528	P. Morin et al., “Extensive Study of the Correlation between Contact Etch Stop Nitride Material Properties and Negative Bias Temperature Instabilities Measured in pMOSFETS,” ECS Transactions, vol. 6, no. 3, pp. 355-69 (2007) (“Morin-2007”)
1529	U.S. Patent Application Publication No. 2005/0170104 A1 to Jung et al. (“Jung”)
1531	U.S. Patent Application Publication No. 2008/0145984 A1 to Ke et al. (“Ke”)
1532	P. Bai et al., “A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell,” Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 657-60 (Dec. 2004) (“Bai-2004”)

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Under 35 U.S.C. §§311, 312 and 37 C.F.R. §42.104, United Microelectronics Corporation and UMC Group (USA) (collectively, “Petitioner”) request *inter partes* review (“IPR”) of claims 1-6 and 11-19 (“Challenged Claims”) of U.S. Patent No. 7,923,764 (Ex.1001, “the ’764 patent”).

I. INTRODUCTION

The ’764 patent relates “to techniques for improving the driving power and reliability of a MISFET [metal insulator semiconductor field-effect transistor]” by (1) extending a high-k gate insulating film from under the gate electrode to under a sidewall and (2) making the high-k film thicker under the gate electrode than under the sidewall. Ex.1001, 1:15-21, 2:6-15, 2:37-44. These basic concepts were known before the ’764 patent, a fact corroborated by the Examiner and acquiesced to by the Applicant during Japanese prosecution. Petitioner, supported by the declaration of Dr. Sanjay Banerjee, demonstrates the Challenged Claims are unpatentable.

II. GROUNDS FOR STANDING

Petitioner certifies under 37 C.F.R. §42.104(a) that the ’764 patent is available for IPR and Petitioner is not barred or estopped from requesting IPR of the Challenged Claims on the grounds identified in this Petition.

III. IDENTIFICATION OF CHALLENGE AND REQUESTED RELIEF

A. Prior Art

The application that resulted in the ’764 patent was filed on July 20, 2009 as a divisional of U.S. Patent No. 7,579,227 (“the ’227 patent”), which claims priority

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to JP2005-227457 (“JP application”), filed August 5, 2005. Petitioner does not acquiesce the ’764 patent is entitled to priority of the JP application. Regardless, each applied prior art reference identified below was filed or published before August 5, 2005 and is prior art to the ’764 patent.

1. U.S. Publication No. 2003/0025135 to Matsumoto, et al.
 (“Matsumoto”; Ex.1009), published February 6, 2003, is prior art under 35 U.S.C. §102(b).¹
2. JP2003-258241 to Kajiyama (“JP-Kajiyama”; Ex.1010), published September 12, 2003, is prior art under §102(b). A certified translation of JP-Kajiyama (“Kajiyama”) is provided as Ex.1011.
3. U.S. Publication No. 2006/0131672 to Wang, et al. (“Wang”; Ex.1012), filed April 27, 2005, is prior art under §102(e).
4. U.S. Publication No. 2005/0045938 to Mutou, et al. (“Mutou”; Ex.1019), published March 3, 2005, is prior art under §102(b).
5. U.S. Publication No. 2005/0051856 to Ono, et al. (“Ono”; Ex.1013), published March 10, 2005, is prior art under §102(b).

¹ Pre-AIA 35 U.S.C. §102 applies.

6. “Effects of ALD HfO₂ thickness on charge trapping and mobility” to Sim, et al. (“Sim”; Ex.1024), published June 17, 2005, is prior art under §102(b). Ex.1326, ¶¶18-21.
7. U.S. Publication No. 2004/0110352 to Bu, et al. (“Bu”; Ex.1025), published June 10, 2004, is prior art under §102(b).
8. “High-k gate dielectrics: Current status and materials properties considerations” to Wilk, et al. (“Wilk”; Ex.1018), published in 2001, is prior art under §102(b). Ex.1326, ¶¶14-17.

B. Grounds for Challenge

The specific Grounds of the challenge are set forth below and are supported by the Declaration of Sanjay Banerjee, Ph.D. (Ex.1101).

Ground	Basis	Challenged Claims	Prior Art Reference(s)
I	§103 ²	1, 4-5, 14-19	Matsumoto (Ex.1009)
II	§103	2-3, 6, 11	Matsumoto (Ex.1009) – Wang (Ex.1012)
III	§103	11	Matsumoto(Ex.1009) – Wang (Ex.1012) - Sim
IV	§103	2-3	Matsumoto (Ex.1009) – Mutou (Ex.1019)
V	§103	6, 12, 13	Matsumoto (Ex.1009) – Ono (Ex.1013)

² Cites to 35 U.S.C. §§102 and 103 are to the pre-America Invents Act (pre-AIA).

Ground	Basis	Challenged Claims	Prior Art Reference(s)
VI	§103	15	Matsumoto (Ex.1009) – Bu (Ex.1025)
VII	§103	18-19	Matsumoto (Ex.1009) – Wilk (Ex.1018)
VIII	§102	1, 5, 16-17	Kajiyama (Ex.1010/1011)
IX	§103	4, 6, 18-19	Kajiyama (Ex.1010/1011)
X	§103	11	Kajiyama (Ex.1010/1011) – Wang (Ex.1012)
XI	§103	11	Kajiyama (Ex.1010/1011) – Sim (Ex.1024)
XII	§103	12-13	Kajiyama (Ex.1010/1011) – Ono (Ex.1013)
XIII	§103	14-15	Kajiyama (Ex.1010/1011) – Bu (Ex.1025)
XIV	§103	18-19	Kajiyama (Ex.1010/1011) – Wilk (Ex.1018)

IV. THE '764 PATENT

A. Applicant Admitted Prior Art (“AAPA”)

The '764 patent recognized that, prior to August 2005, semiconductor devices had used “a high dielectric constant film formed of a Hf based oxide, Al based oxide or the like” as a gate insulating film. Ex.1001, 1:23-31. It describes two exemplary prior art metal insulator semiconductor field-effect transistors (MISFETs), depicted in

In these prior art devices, the “side end portions” of the high-k gate insulating film “are in direct contact with sidewalls.” Ex.1001, 1:61-64. The ’764 patent purports to address issues with this arrangement by extending the high-k film under the “sidewalls to prevent end portions of the [high-k] film from being in contact with the sidewalls.” *Id.*, 2:10-16. It also purports to make the high-k film thicker under the gate than under the sidewalls. Ex.1001, 2:37-44.

However, these basic concepts were well-known. *See, e.g.*, §§IV.B.2, IV.D.2, V, XII.

B. Technical Background

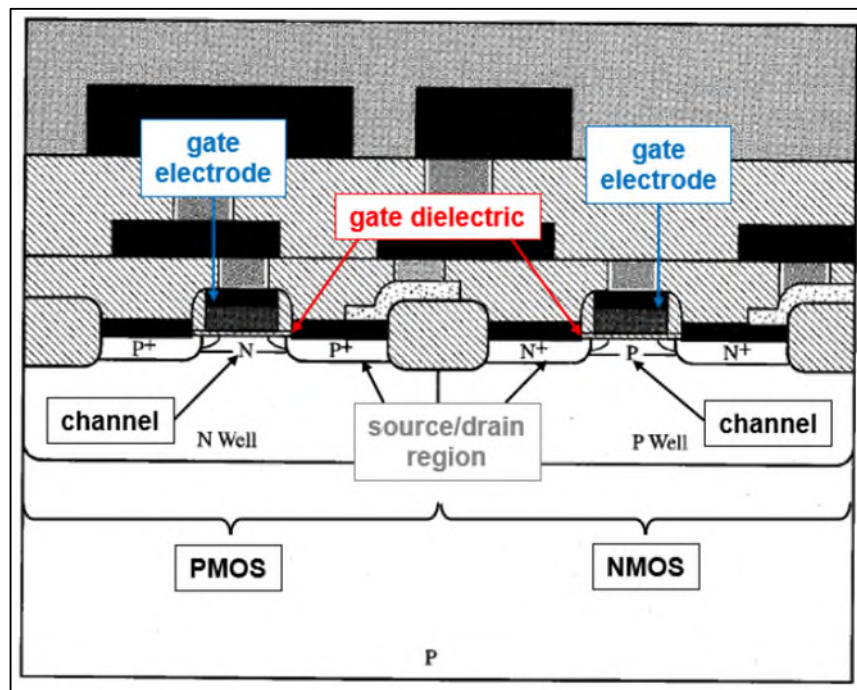
A semiconductor device, at its most basic, exploits the properties of semiconductor materials such as silicon. Many types of semiconductor devices exist including, *e.g.*, diodes and MOS transistors (*e.g.*, field effect transistors (FETs)). *See, e.g.*, Ex.1333, 33-41. For ease of discussion, Petitioner describes FET devices in further detail below. A POSITA would understand the basic concepts in §IV.B also apply to other types of semiconductor devices.

1. MISFET/MOSFET

MISFETs⁵ have a **source/drain** for current input/output. Ex.1101, ¶46;

⁵ The terms “MISFET” and “MOSFET” (“Metal-***Oxide***-Semiconductor Field-Effect Transistor”) are interchangeable. Ex.1101, ¶46)

Ex.1333, 76-82. MISFETs like the ones at issue here also have a **gate** above a **channel** region between the source and drain. Ex.1101, ¶46; Ex.1333, 71-76. The **gate** includes a **gate electrode** and **gate dielectric** (also referred to as a gate insulating film) separating the gate electrode from the channel region. *Id.* Applying voltage to the gate electrode controls the channel region to connect (ON state) or disconnect (OFF state) the source and drain. Ex.1101, ¶46; Ex.1341, 8-9. Generally, source/drain regions are **doped** with either a **p-type** or **n-type** impurity. Ex.1101, ¶47; Ex.1333, 76-82. MISFETs with n-type source/drain regions are called **NMOS**, and MISFETs with p-type source/drain regions are called **PMOS**, as illustrated below. Ex.1101, ¶46; Ex.1333, 13, Figure 1-11 (below).

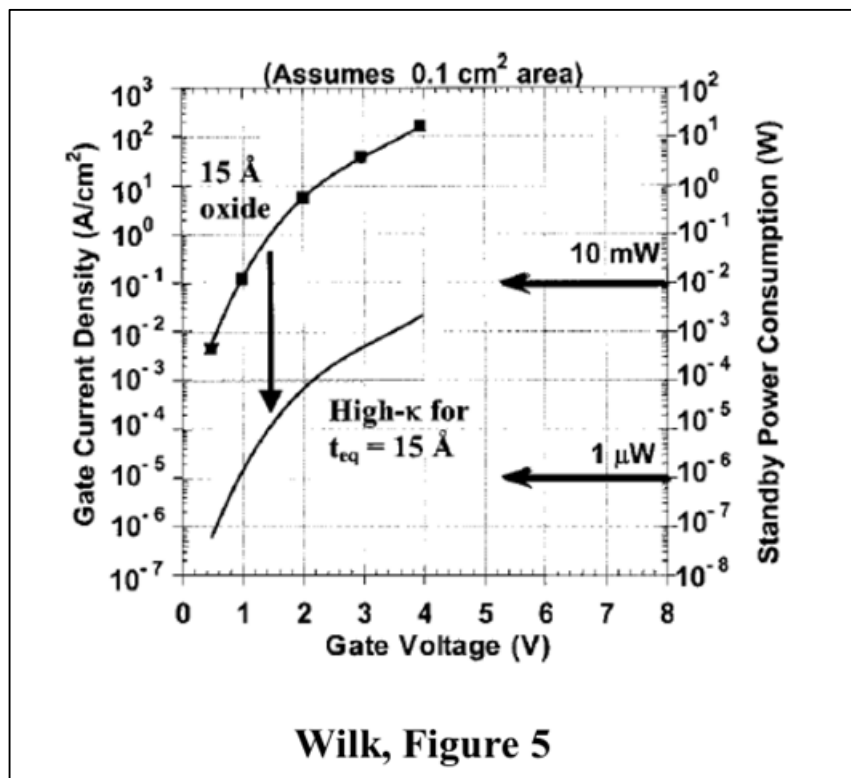


2. Gate Insulating Film

a. Materials

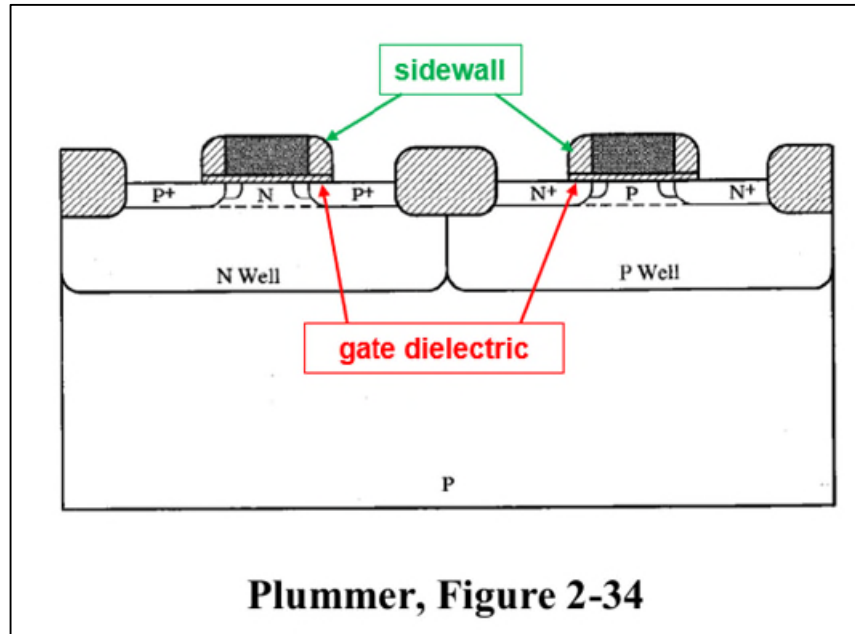
A common feature of a FET is the gate dielectric. Ex.1333, 288. For decades prior to the '764 patent, silicon dioxide (SiO_2) was the primary material used for gate dielectrics in MOSFETs. Ex.1101, ¶58; Ex.1333, 53 (“ SiO_2 is essentially a perfect insulator and provides the needed [electrical] isolation.”); Ex.1213, 3-4. As gate dielectric layers continued to shrink in thickness (*e.g.*, below 1.5 nm), use of SiO_2 became untenable, because the amount of gate-to-channel tunneling leakage-current passing through the gate dielectric prevents the gate electrode from effectively controlling the ON/OFF states of the FET. Ex.1101, ¶¶59-64; Ex.1334, 4-5.

High-k dielectrics, like Hf-based oxides, Ta_2O_5 , or ZrO_2 , replaced SiO_2 to address these challenges. Ex.1101, ¶64; Ex.1334, 146. For example, it was known by 2005 that, as compared to SiO_2 , high-k materials significantly reduce the amount of leakage current and, thus, improve energy efficiency. Ex.1101, ¶¶64-69; Ex.1018, 5250, Fig. 5 (below); Ex.1334, 146-47.



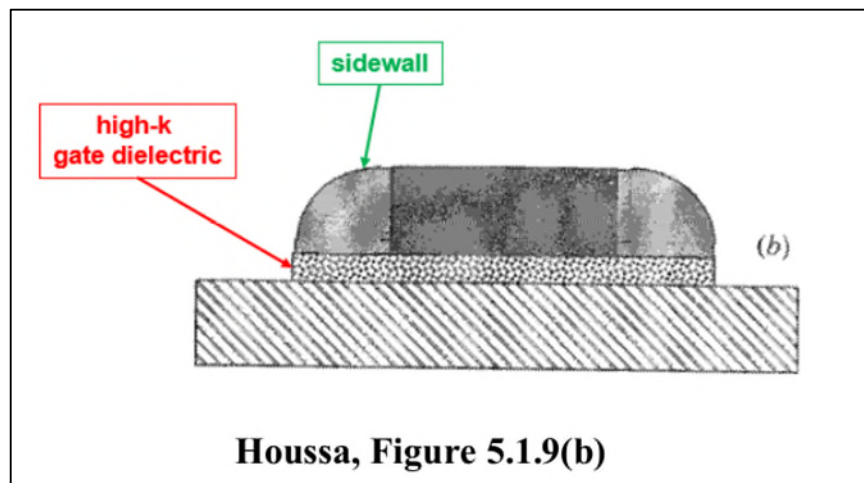
b. Extended Gate Insulating Films

Prior to 2005, it was common practice to extend the gate dielectric from under the gate electrode to under the gate sidewalls. For example, Plummer depicts a CMOS device having an extended gate dielectric in the NMOS and PMOS transistors. Ex.1101, ¶70; Ex.1333, Fig. 2-34 (below), 82-83.

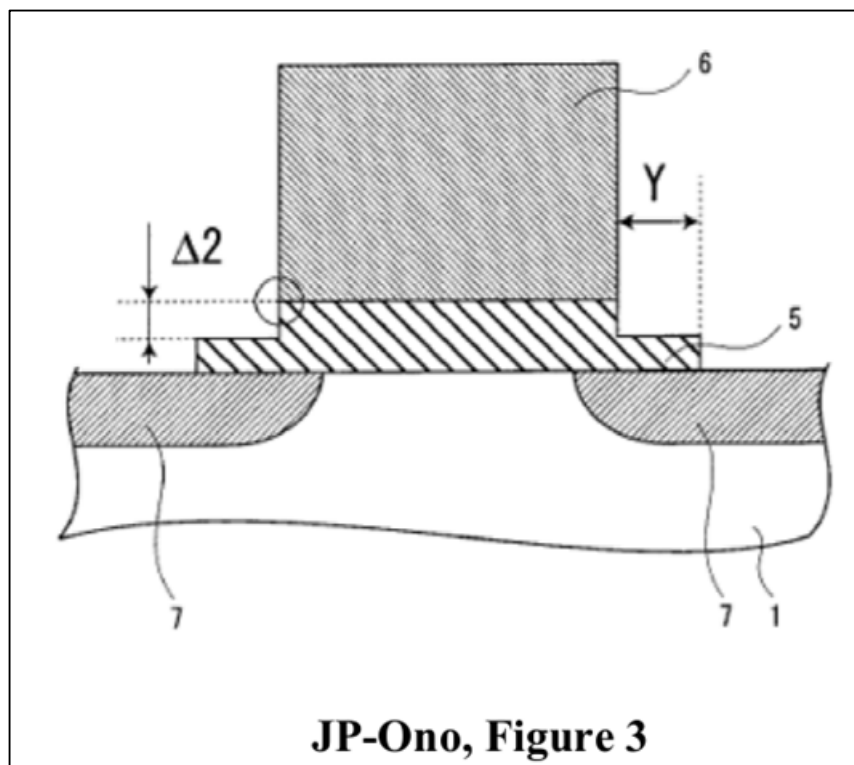


Houssa discloses another example using a high-k material as the gate insulating film that extends from under the gate electrode to under the sidewalls.

Ex.1101, ¶71; Ex.1213, 510, Fig. 5.1.9(b) (below).



JP Publication No. 2005-064190 (“JP-Ono”⁶; Ex.1340), filed two years before the earliest priority date of the ’764 patent, also describes extending the gate dielectric and varying its thickness. Specifically, JP-Ono adjusts both the reduction in thickness of the gate dielectric ($\Delta 2$) outside the gate electrode and the length of the gate dielectric from the outer edge of the gate electrode (Y) (*i.e.*, how far the gate dielectric protrudes from under the gate electrode). Ex.1340, ¶35, Fig. 3 (below); Ex.1101, ¶¶72-76.

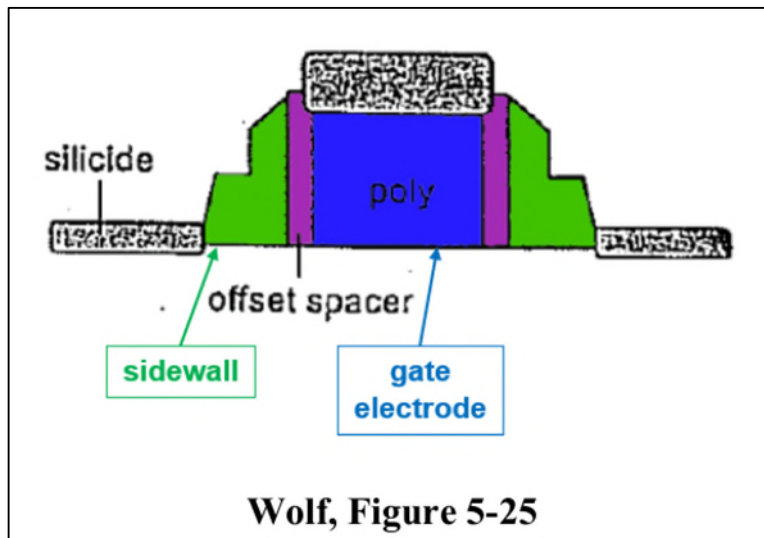


⁶ A certified translation of JP-Ono is included with Ex.1340.

3. Sidewall Structures

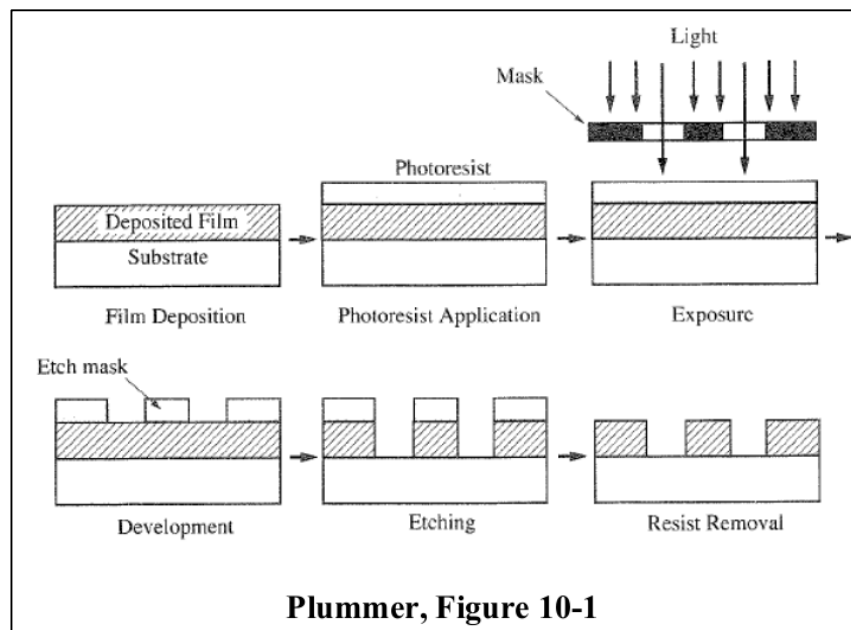
Another common feature of a semiconductor device is sidewalls, vertical insulating structures formed on or proximate to the side surfaces of a gate electrode. Sometimes, the terms “sidewall,” “spacer,” and “sidewall spacer” are used interchangeably. Ex.1101, ¶¶77. Sidewalls serve a variety of purposes and functions in a semiconductor device such as defining the source/drain region, providing isolation, protecting the gate during subsequent fabrication, and controlling the width of the gate in the gate length direction. *Id.*

As an example, sidewalls may be used for “[c]ontrolling the position of the edge of the SDE [source/drain extension] region with respect to the gate edge” so as to achieve optimal amount of overlap between the SDE and the gate edge. Ex.1334, 217. As shown below, “an offset-spacer is fabricated on the side of the gate after the gate-poly is etched (but before the SDE implant step is carried out ...,” with offset-spacer width “varied from zero (no-spacer) to some upper-bound (e.g., 50-nm)” to achieve optimum device characteristics. *Id.*, 217, Fig. 5-25 (below); Ex.1101, ¶78.

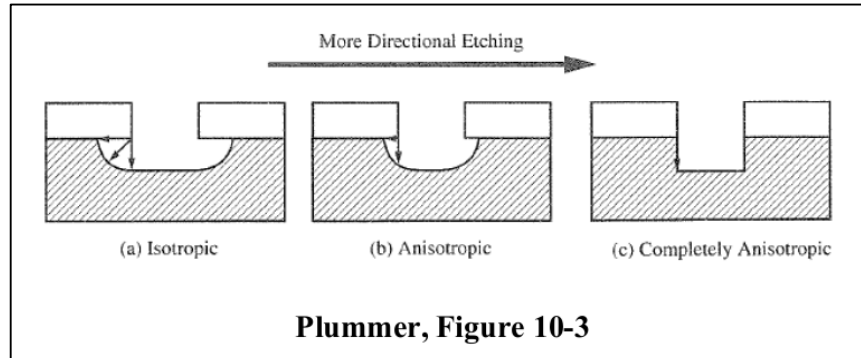


4. Etching Properties

In semiconductor devices, thin films are often first deposited on the wafer surface and then selectively removed by etching to leave the desired pattern of the film. Ex.1101, ¶79; Ex.1333, 609-11. The desired pattern is often defined by placing a mask on the surface before etching; the mask is removed after etching. Ex.1101, ¶79; Ex.1333, 609-10, Fig. 10-1 (below).



Etching is performed in a “wet” or “dry” environment. Ex.1101, ¶81; Ex.1333, 609, 612-37. Wet etching involves the use of liquid etchants (*e.g.*, hydrofluoric acid), whereas dry etching involves the use of gas-phase etchants in a plasma. Ex.1101, ¶81; Ex.1333, 609. Etching processes are also described based on the relative etch rates in different directions. Ex.1101, ¶82; Ex.1333, 610-11. Isotropic etching occurs when the etch rate is the same in all directions, resulting in a semicircular etch profile as shown in Figure 10-3(a) below.

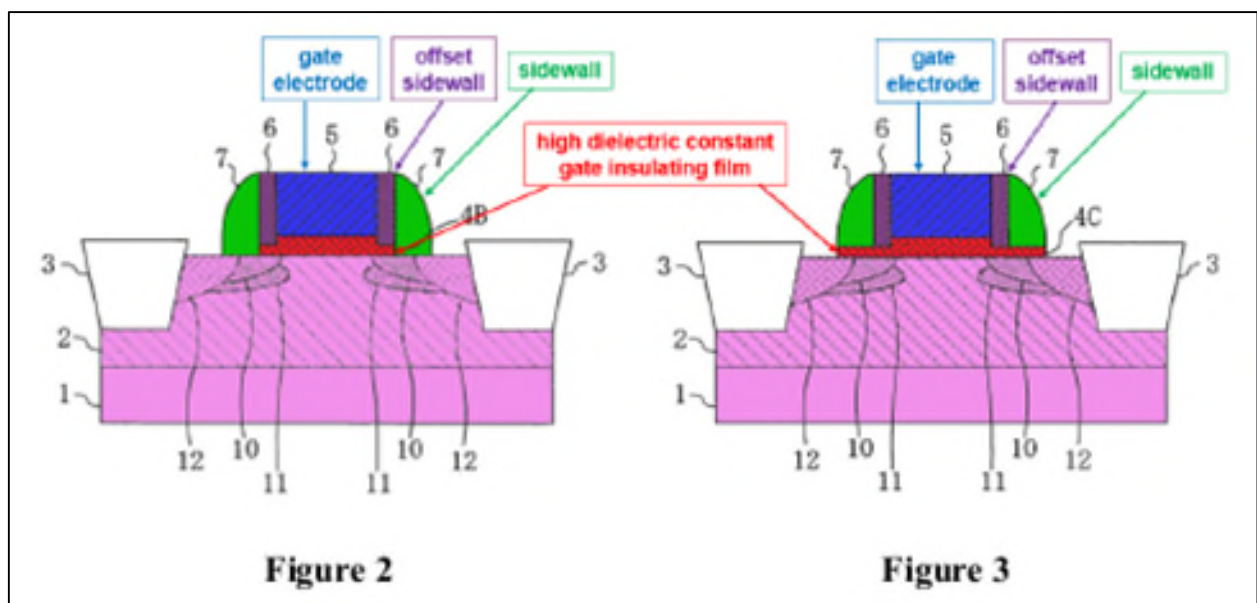


Ex.1333, Fig. 10-3. Most wet chemical etchants etch isotropically. *Id.*, 610-13. Anisotropic etching occurs where there is little or no etching in the lateral direction. *Id.*, 611, Figure 10-3(b), (c) (above). For anisotropic etching, the amount of lateral etching may vary, such that the etched surface may be curved or sloped (*see id.*, Fig. 10-3(b) (above)) to completely vertical (*see id.*, Fig. 10-3(c) (above)). Ex.1101, ¶82.

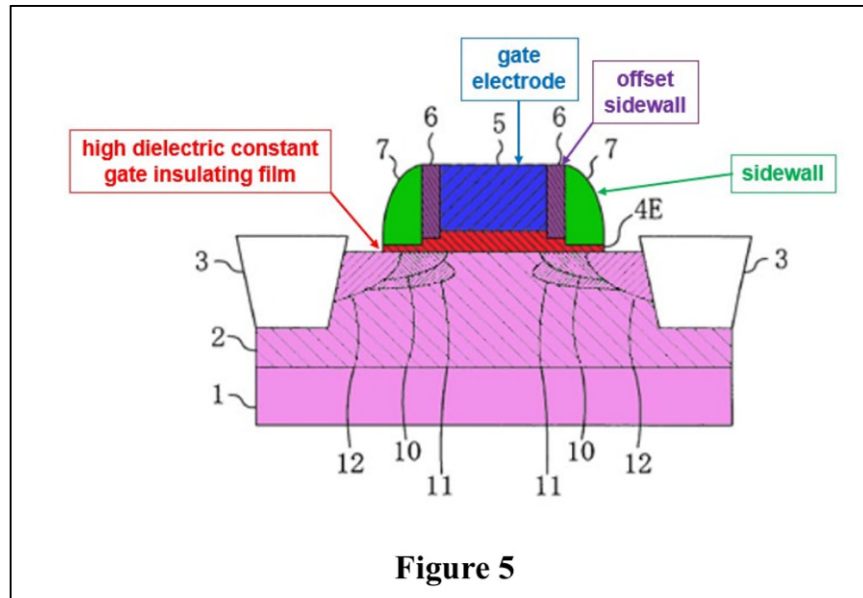
C. '764 Patent Overview

The four semiconductor device embodiments presented in the '764 patent can be separated into two groups—single sidewall devices (first/fourth embodiments) and double sidewall devices (second/third embodiments). The '764 patent's claims are directed to double sidewall devices and cover different alternatives for varying the thickness of the high-k gate insulating film.

In the second embodiment (see Ex.1001, FIG. 2 (below, left)), the high-k gate insulating film (shaded red) extends only under offset sidewall 6 (shaded purple) and has a smaller thickness under offset sidewall 6 than under gate electrode 5 (shaded blue), corresponding, *e.g.*, to claim 1. Ex.1001, 7:48-59. In a modification (see *id.*, FIG. 3 (below, right)), the thickness of the high-k gate insulating film is the same under both offset sidewall 6 and insulating sidewall 7 and is thinner under both sidewalls than under gate electrode 5, also corresponding to claim 1.



In the third embodiment device (see Ex.1001, FIG. 5 (below)), the high-k gate insulating film has declining thicknesses under gate electrode 5, under offset sidewall 6, and under insulating sidewall 7, which also corresponds to claim 1. Ex.1001, 10:53-62.



D. Prosecution History

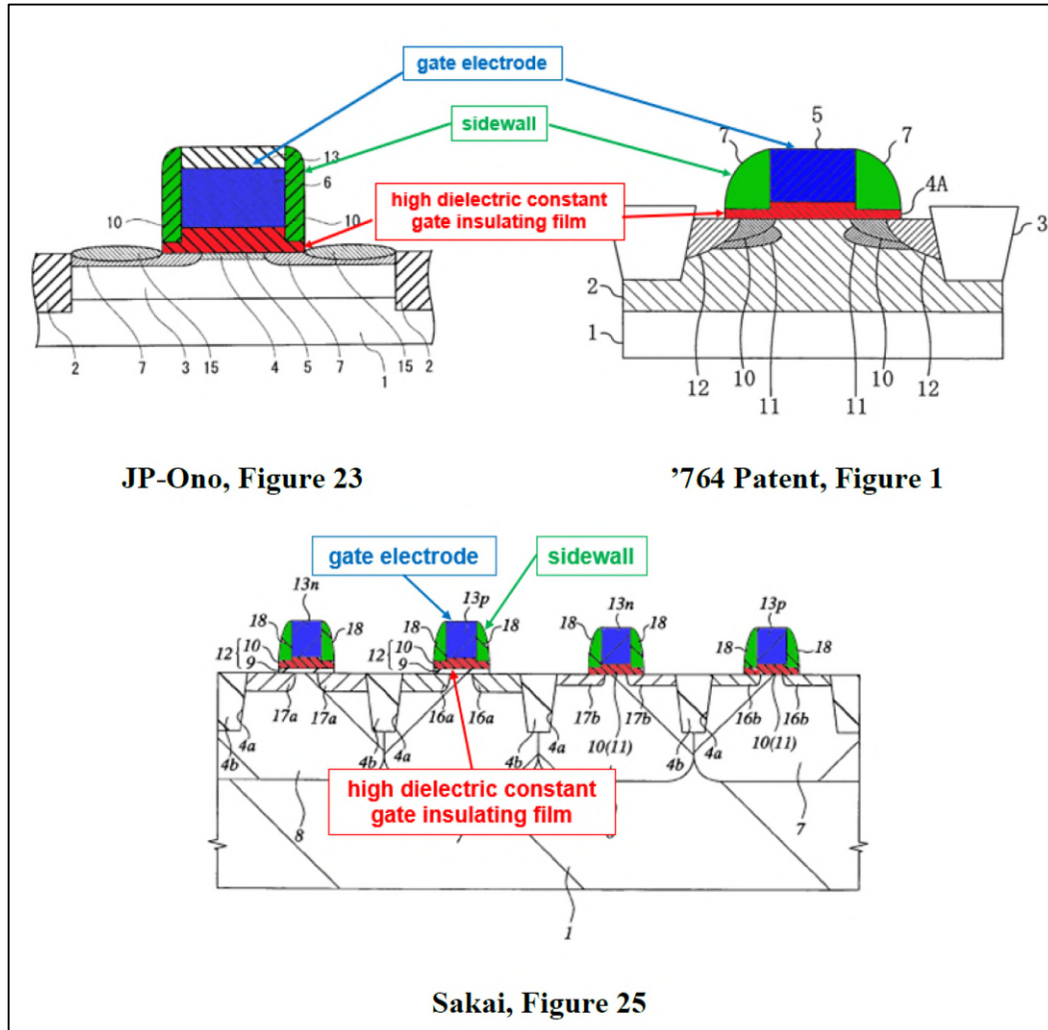
1. '764 Patent

The corresponding U.S. application was filed with one independent device claim corresponding to issued claim 1. The Examiner rejected this claim as anticipated by U.S. Patent 6,992,358 to Hieda (“Hieda”). Ex.1002, 122-23. Applicant did not amend the claims, successfully arguing the Examiner misapplied Hieda. *Id.*, 142-44, 159.

2. JP Application

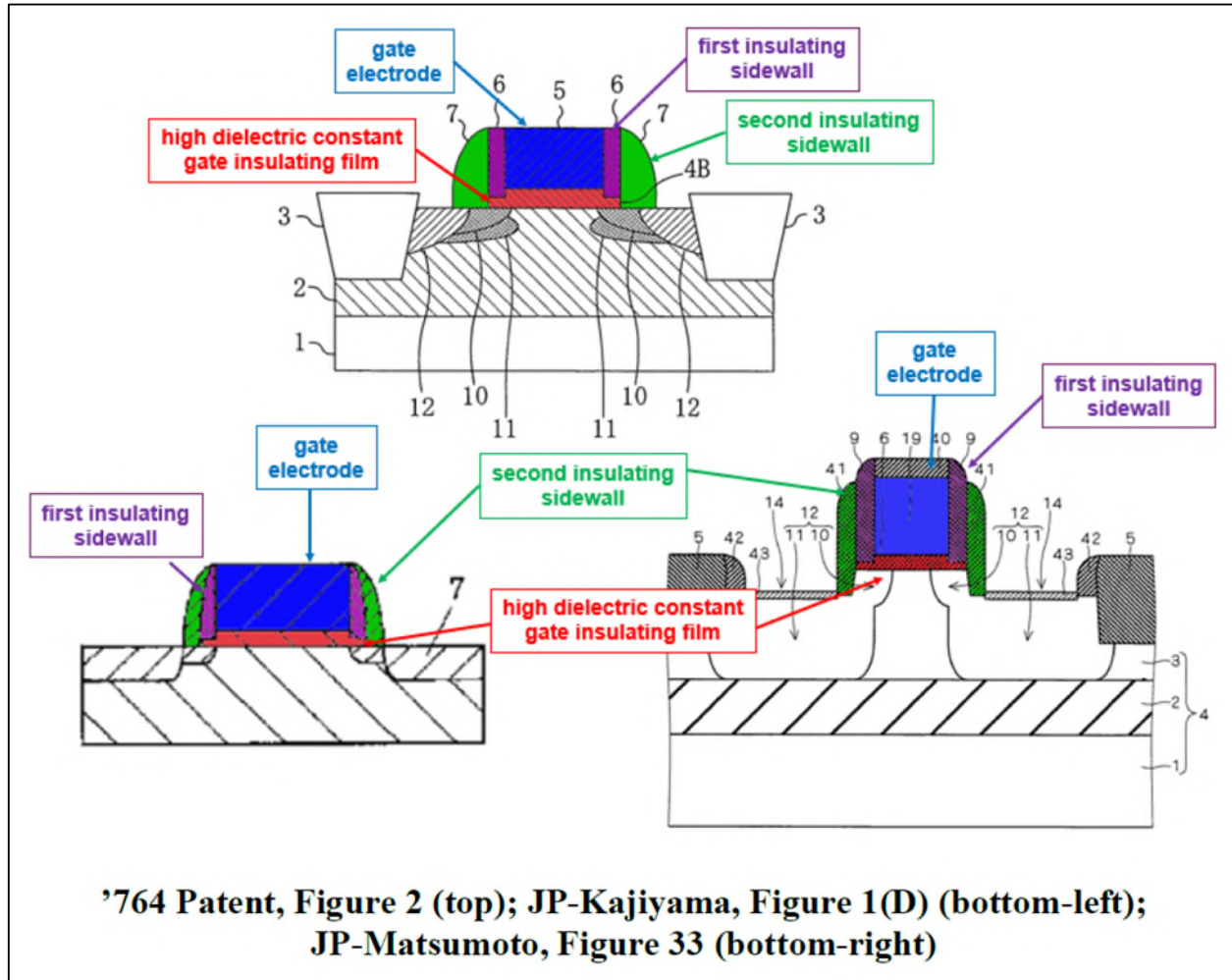
The JP priority application was filed with the same device claim originally

filed with the U.S. application associated with the '227 patent. Ex.1305, 1. On September 16, 2011, the JP-Examiner found this claim scope unpatentable, citing JP-Ono discussed above (see Ex.1340, Fig. 23 (below, top-left)) and WO2004/017418 to Sakai, et al. ("Sakai"; see FIG. 25 (below, bottom)), which both teach a high-k gate insulating film with a smaller thickness under the sidewall than under the gate electrode, like *e.g.*, the '764 patent's single sidewall embodiments. (see Ex.1001, FIG. 1 (below, top-right)). Ex.1305, 4-6.



In response, Applicant narrowed the claim to recite (1) a double sidewall

structure with a high-k film having a smaller thickness under a first sidewall than under the gate electrode and (2) extension and source/drain regions. Ex.1305, 8. The JP-Examiner rejected the amended claim based on both JP Application No. 2003-258241 to Kajiyama (“JP-Kajiyama”; Ex.1010, Fig. 1(D) (below, bottom-left)) and JP Application No. 2004-241755 to Matsumoto (“JP-Matsumoto”; Fig. 33 (below, bottom-right)), which each teach the same basic structure as the ’764 patent’s Figure 2. Ex.1305, 14-16; *compare* Ex.1001, FIG. 2 (below, top).



In response, Applicant further narrowed the claim to recite that the thickness of the high-k gate insulating film under the second sidewall is smaller than the thickness under the first sidewall which is smaller than the thickness under the gate electrode. Ex.1305, 18. The JP-Examiner allowed the claim based on this amendment. Ex.1305, 20.

In short, to secure allowance over the prior art, Patent Owner acquiesced during JP prosecution that the scope of at least issued claim 1 of the '764 patent was known in the art.

E. Claim Construction

Petitioner does not believe any claims require construction to resolve the patentability disputes in this proceeding. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

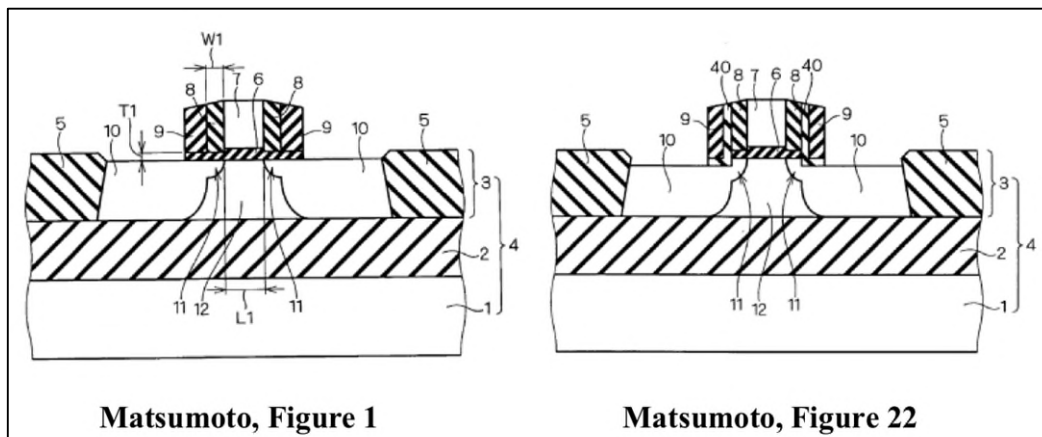
F. Level of Ordinary Skill in the Art

A POSITA would have had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. Ex.1101, ¶¶125-27. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education. *Id.*

V. GROUND I: Matsumoto Renders Claims 1, 4-5, and 14-19⁷ Obvious.

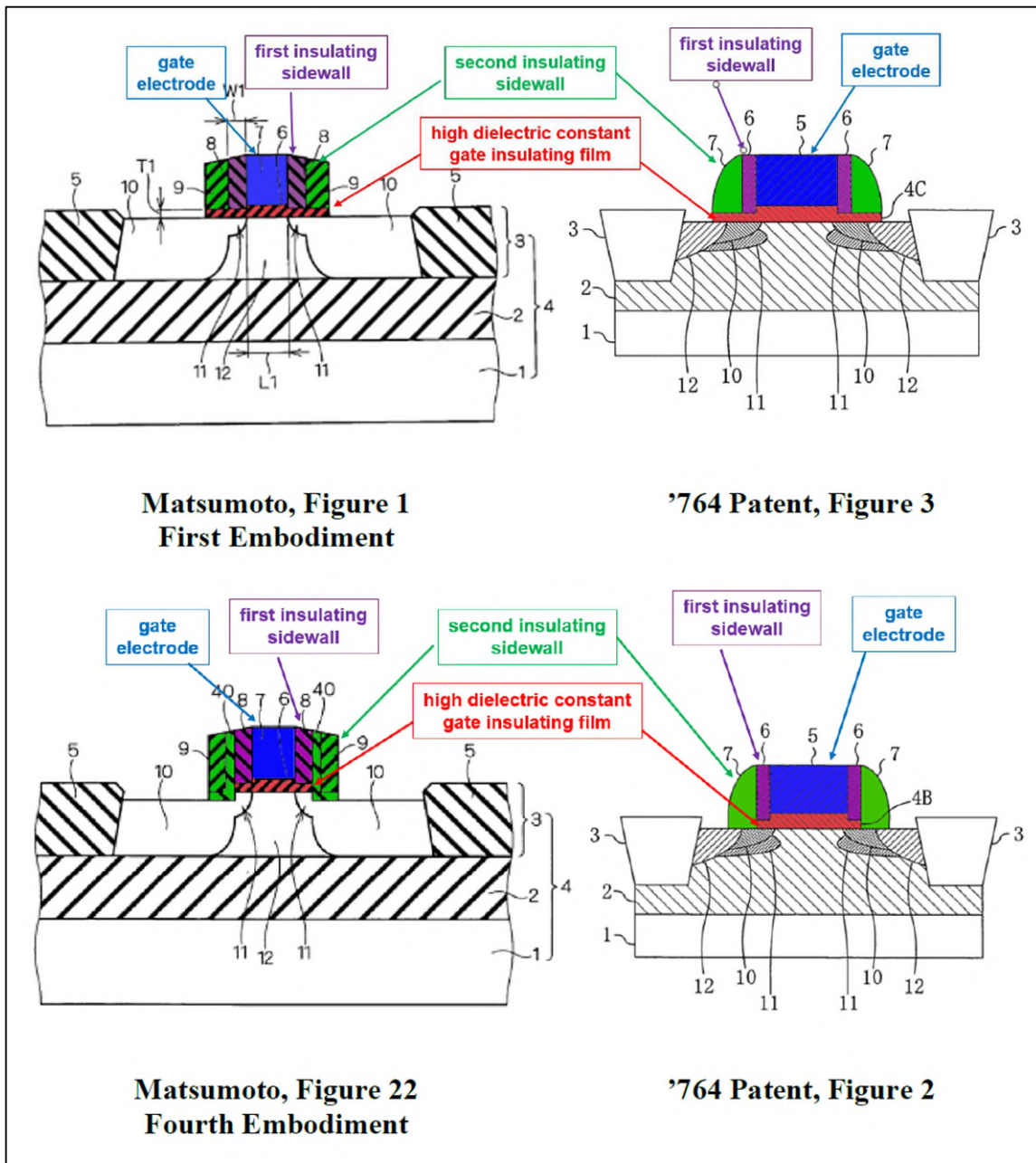
A. Overview

Matsumoto relates “to a semiconductor device” and more specifically to a MOSFET. Ex.1009, ¶2; Ex.1101, ¶131. Matsumoto presents seven embodiments of its semiconductor device. This Petition focuses on Matsumoto’s first and fourth embodiment MOSFETs, which each includes a multilayer sidewall structure and gate insulating film 6 extending from under a gate electrode. In the first embodiment, gate insulating film 6 extends under both films 8 and 9 formed on the gate electrode’s side surfaces. *See* Ex.1009, ¶¶102-21, FIG. 1 (below, left). In the fourth embodiment, gate insulating film 6 extends under only film 8 of the sidewall. *See id.*, ¶¶137-40, FIG. 22 (below, right).



B. Independent Claim 1

Matsumoto's first and fourth embodiment devices each renders claim 1 obvious, as illustrated by the side-by-side figures below. Ex.1101, ¶155; Ex.1009, FIGS. 1 (below, top-left), 22 (below, bottom-left); Ex.1001, FIGS. 3 (below, top-right), 2 (below, bottom-right).



1. Preamble

Matsumoto’s first embodiment (*see* Ex.1009, FIG. 1) and fourth embodiment (*see id.*, FIG. 22) each discloses a “*semiconductor device*”⁸: “The present invention relates to **a semiconductor device.**”⁹ Ex.1009, ¶¶2, 102, 137; Ex.1101, ¶156.

2. Limitation 1[a]

Matsumoto’s first and fourth embodiments each teaches “*a high dielectric constant gate insulating film formed on an active region in a substrate*” (Limitation 1[a]). Ex.1101, ¶¶157-164.

Both embodiments include “*a substrate.*” Ex.1101, ¶157. Each device has multi-layer SOI **substrate 4** (*see* Ex.1009, FIGS. 1 (below, left), 22 (below, right) (shaded pink)) with silicon substrate 1, BOX layer 2 and single-crystalline silicon layer 3. Ex.1009, ¶102, ¶¶137 and 140 (relating fourth embodiment to first embodiment);¹⁰ *Google LLC v. Jenam Tech, LLC*, IPR2021-00630, 2022 WL

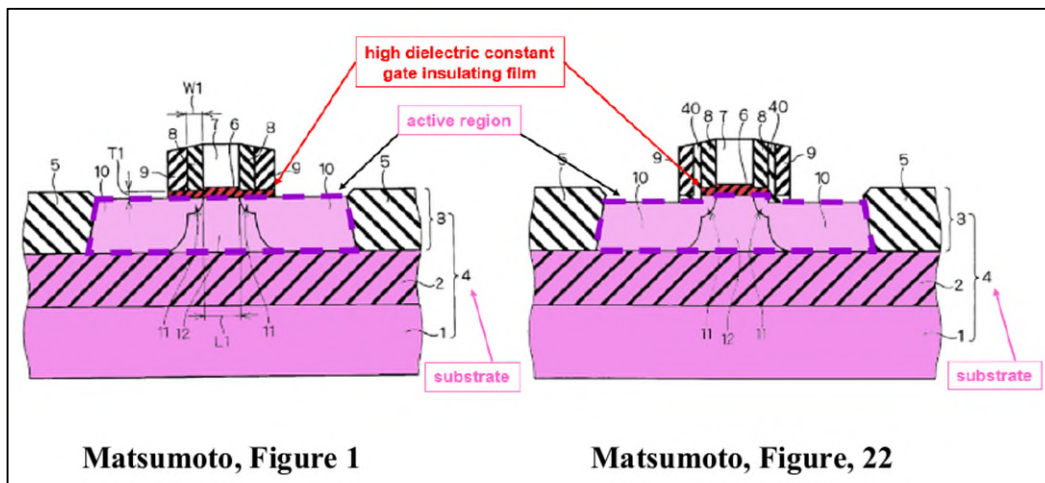
⁸ Claim language is indicated by italics throughout.

⁹ Unless otherwise noted, all emphasis added.

¹⁰ Although Matsumoto discloses several embodiments, many of the fabrication steps are discussed in relation to the first embodiment. Ex.1101, ¶132; Ex.1009, ¶137. Thus, Petitioner at times also relies on disclosures from Matsumoto’s first embodiment when discussing the fourth embodiment.

4287797, *9 n.9 (P.T.A.B. Sept. 16, 2022) (applying same disclosure where “figures refer to corresponding features using the same reference numbers”).

Isolating insulation film structures 5 “extend[ing] from the upper surface of silicon layer 3 to the upper surface of the BOX layer 2”, define a “**device region.**” Ex.1009, ¶¶102-103, FIG. 1 (below, left), ¶¶137, 140, FIG. 22 (below, right). The device region, identified by isolation regions, is an “*active region in a substrate*” and includes source/drain regions 10. Ex.1009, ¶¶105, 139; Ex.1101, ¶158; see Ex.1001, 1:34-35 (“region of the well 102 surrounded by the STI serves as an active region of a substrate 101”), 7:26-43 (active region includes source/drain regions surrounded by STI structures).



In both embodiments, film 6 (see Ex.1009, FIGS. 1 (above, left), 22 (above, right) (shaded red)) “is formed partially on the upper surface of the silicon layer 3” in the device region with gate electrode 7 “formed partially” thereon. *Id.*, ¶103, ¶137 (fourth embodiment’s gate electrode “formed by the process described in the first

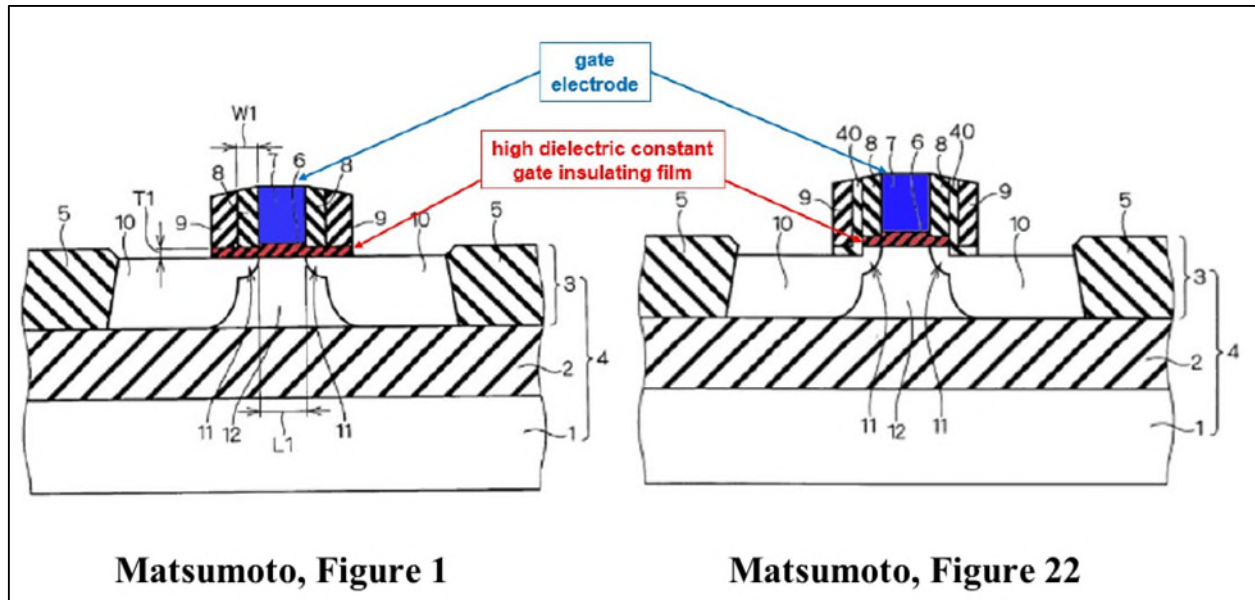
preferred embodiment”), FIG. 22 (elements 6, 7). “A silicon oxynitride film, a metal oxide film such as Al_2O_3 or a ferroelectric film such as Ta_2O_5 and BST may be formed in place of the silicon oxide film 13,” which is etched during fabrication to form film 6. *Id.*, ¶¶107, 114, 138, FIGS. 1, 9-10, 18-19, 22. Al_2O_3 , Ta_2O_5 , and BST are high-k dielectrics. Ex.1101, ¶162; see Ex.1001, 1:28-30 (“**high dielectric constant film** formed of a Hf based oxide, Al based oxide or the like, which has a relative dielectric constant of 10 or more”); Ex.1018, Table I (identifying Al_2O_3 , Ta_2O_5 as high-k dielectrics). A POSITA would have been motivated to use a high-k dielectric in Matsumoto’s device to address the well-documented issues with scaling SiO_2 to thicknesses needed for large scale device integration. See Ex.1213, 3-12; Ex.1334, 4-5, 146-47; Ex.1101, ¶¶163-64.

Film 6, present in both Matsumoto’s first and fourth embodiments, is therefore “a high dielectric constant gate insulating film formed on an active region in a substrate” (Limitation 1[a]). Ex.1101, ¶164; *e.g.*, Ex.1009, ¶103 (disclosing that a portion of film 6, which “lies under the gate electrode 7 functions as a gate insulation film”).

3. Limitation 1[b]

Matsumoto’s first and fourth embodiments each teaches “a gate electrode formed on the high dielectric constant gate insulating film” (Limitation 1[b]). Ex.1101, ¶¶165-66.

In both embodiments (illustrated below), “**gate electrode 7** [shaded blue] made of polysilicon **is formed partially**” on high-k dielectric insulating film 6. Ex.1009, ¶¶103, 107 (describing formation of high-k insulating film and gate electrode), 137-138, FIGS. 1 (below, left), FIG. 22 (below, right).



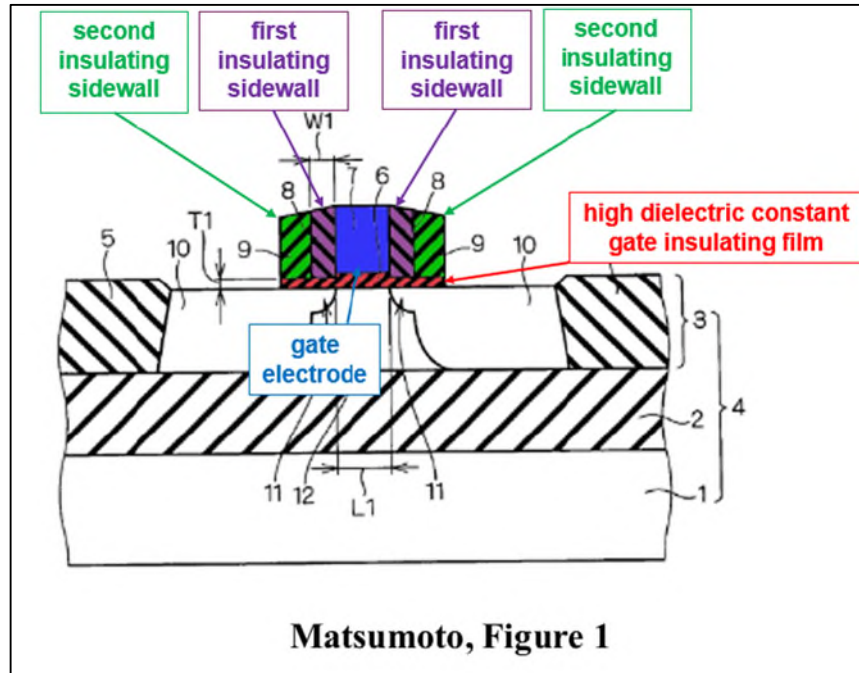
4. Limitations 1[c]/1[d]

Matsumoto’s first and fourth embodiments each teaches “*a first insulating sidewall formed on each side surface of the gate electrode*” (Limitation 1[c]) and “*a second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween*” (Limitation 1[d]). Ex.1101, ¶¶167-174.

In Matsumoto’s first embodiment, “silicon nitride film 9 is formed on each side surface of the gate electrode 7, with a silicon oxide film 8 therebetween.” Ex.1009, ¶103, FIG. 1 (below). Matsumoto refers to film 9 as a “sidewall insulation

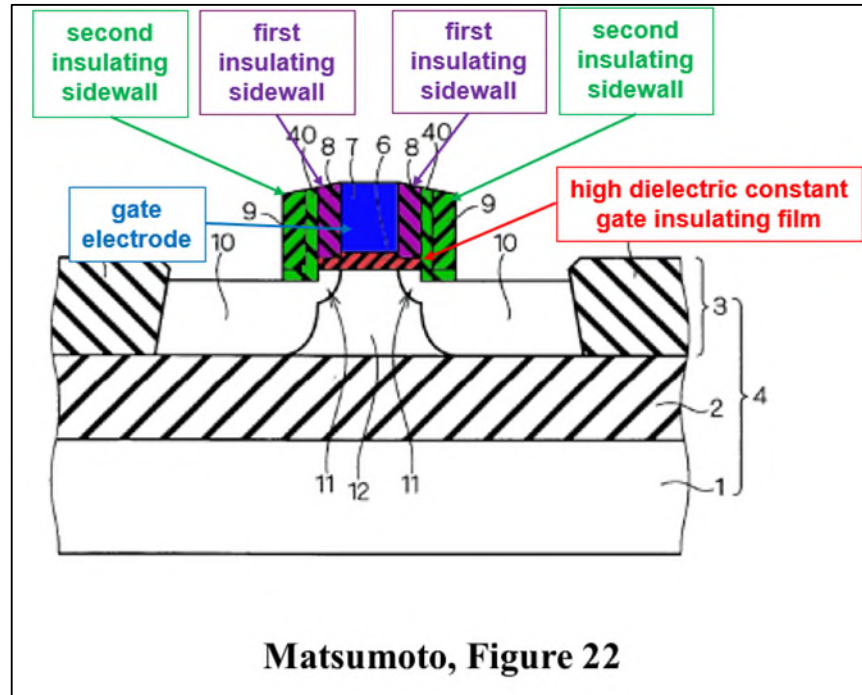
film” but does not refer to film 8 as a “sidewall.” *See id.*, ¶114 (describing nitride films 9a/9b “serving as **sidewall** insulation films”). A POSITA would have understood film 8 also to be a sidewall, as it is formed vertically on gate electrode 7’s side surface. *Id.*, ¶¶104, 110, 40 (“semiconductor device further includes a second sidewall formed on the side surface of the gate electrode, with the first sidewall therebetween”); Ex.1101, ¶168. Because silicon oxide and silicon nitride are both insulators, silicon oxide film 8 (*see* Ex.1009, FIG. 1 (below) (shaded purple)) is “*a first insulating sidewall*” (Limitation 1[c]) and silicon nitride film 9 (*see id.*, FIG. 1 (below) (shaded green)) is “*a second insulating sidewall*” (Limitation 1[d]). Ex.1101, ¶169. Both, as discussed above, are “*formed on*”¹¹ the gate electrode’s side surfaces. *See id.*, ¶¶110 (describing formation of silicon oxide films 8a/8b on the side surfaces of the gate electrodes), 114, claim 1 (referring to “**insulation** films” formed on side surfaces on gate electrode); Ex.1101, ¶170.

¹¹ The ’764 patent uses the term “*formed on*” generally to refer to location and does not require contact. Ex.1001, 1:37-39, 7:32-37; Ex.1101, ¶170.



In Matsumoto’s fourth embodiment, silicon oxide film 40 and silicon nitride film 9 are formed “on the outer side surfaces of” film 8, as illustrated in Figure 22. See Ex.1009, ¶¶110, 139, FIG. 22 (below). Silicon oxide film 8 (see Ex.1009, FIG. 22 (below) (shaded purple)) is “a first insulating sidewall” (Limitation 1[c]) and film 9 (see *id.*, (shaded green) alone, film 40 (see *id.*, (shaded green)) alone, or their combination is “a second insulating sidewall” (Limitation 1[d], consistent with the ’764 patent’s disclosure.¹² Ex.1001, 3:17-22, 21:515; Ex.1101, ¶¶171-74.

¹² The ’764 patent uses the term “insulating sidewall” to refer to a single component (Ex.1001, 6:4-5), a collective structure of two components (*id.*, 3:23-28), and a component having multiple layers (*id.*, 20:66–21:8).



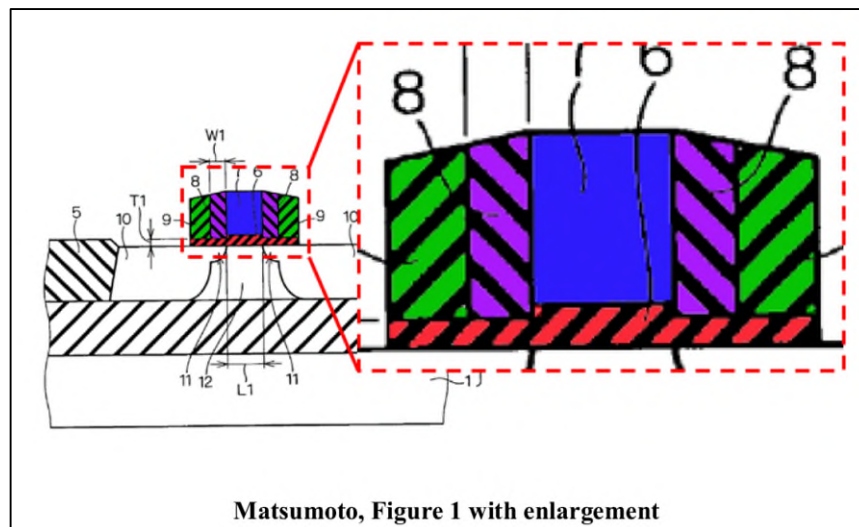
5. Limitations 1[e]-1[f]

For the reasons explained in detail below, Matsumoto’s first and fourth embodiments each teaches “the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall” (Limitation 1[e]) and “part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode” (Limitation 1[f]). Ex.1101, ¶¶175-86.

a. First Embodiment

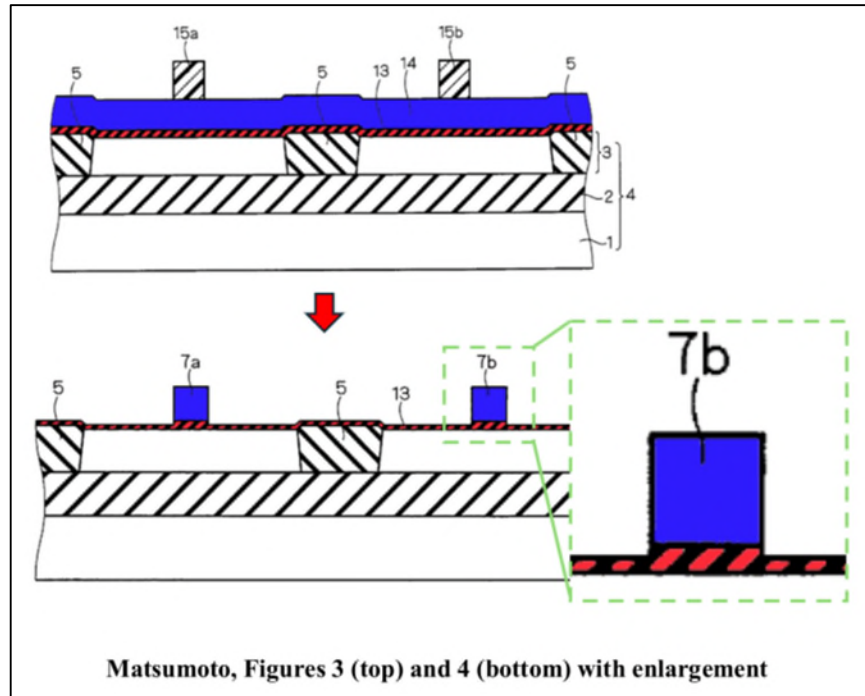
As shown in the Matsumoto Figure 1 enlargement and confirmed by Matsumoto’s fabrication process teachings, high-k gate insulating film 6 (see Ex.1009, FIG. 1 (below) (shaded red)) is an uninterrupted layer (as evidenced by

absence of gaps) extending from under the gate electrode 7 to under film 8 (“*first insulating sidewall*”; see *id.*, FIG. 1 (below) (shaded purple)). High-k film 6 is thinner under film 8 (“*first insulating sidewall*”) than it is under the gate electrode 7 (see *id.*, FIG. 1 (below) (shaded blue)). Matsumoto’s first embodiment device therefore discloses limitations 1[e]-1[f]. *Unified Pats., LLC v. Oceana Innovations LLC*, IPR2020-01463, 2022 WL 500391, *17 (PTAB Feb. 14, 2022) (“patent drawing may serve as prior art ‘without referring to the surrounding description’ if ‘the prior art features are clearly disclosed by the drawing.’”) (citations omitted); Ex.1101, ¶176.

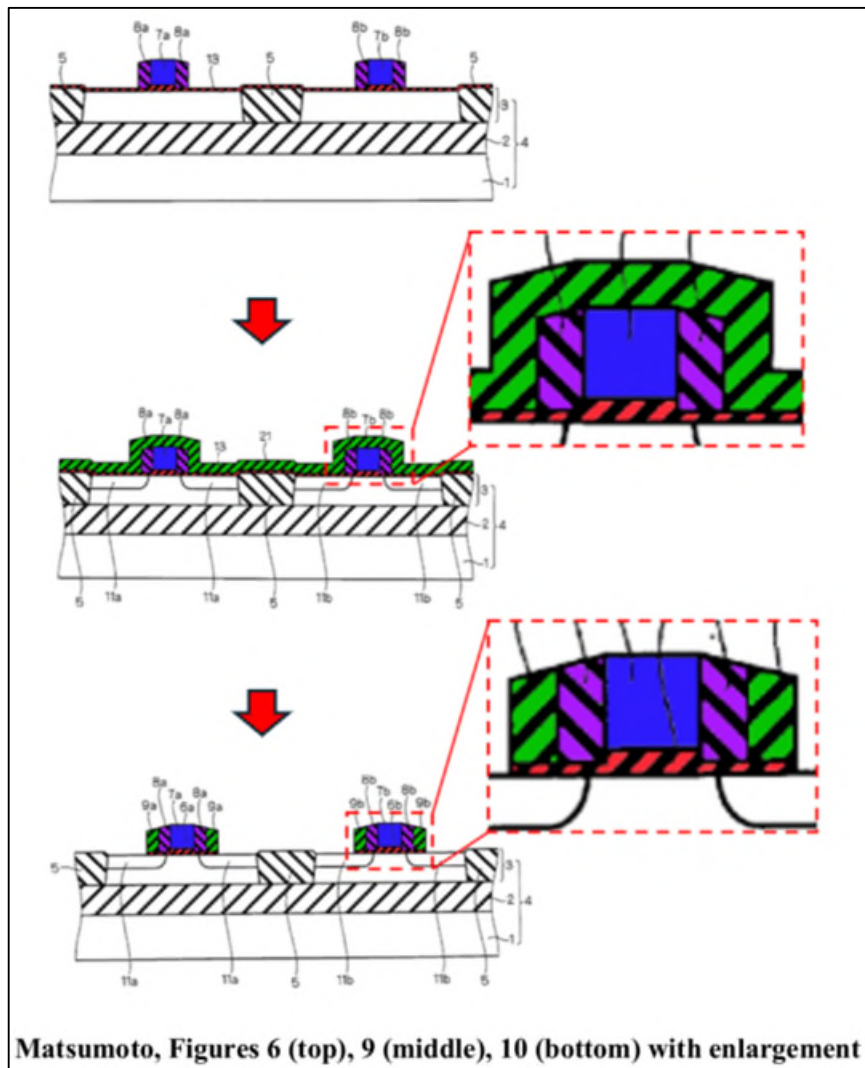


The fabrication process of the first embodiment device confirms the Figure 1 device structure. During fabrication, high-k dielectric film 13 (see Ex.1009, FIGS. 3-4 (below) (shaded red)) is formed on the substrate and polysilicon film 14 (see *id.* (shaded blue)) is formed on high-k dielectric film 13. See *id.*, ¶107. The etching process used to form the gate electrode “slightly etches the upper surface of” film

13, resulting in a high-k dielectric film with a larger thickness under the gate electrode than in the areas not under the gate electrode. Ex.1009, ¶108, FIG. 4 (below, bottom); Ex.1101, ¶178.



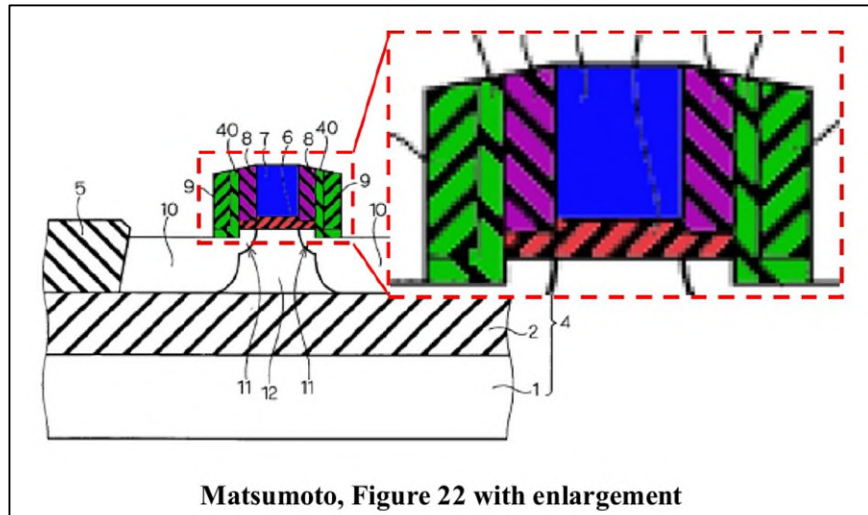
After formation of sidewalls 8a/8b (“*first insulating sidewall*”; see Ex.1009, FIGS. 6, 9-10 (shaded purple)), silicon nitride film 21 is “formed on the entire top surface” of the intermediate structure. *Id.*, ¶¶109-10, 114, FIGS. 6 (below, top), 9 (below, middle). Film 21 and film 13 are etched “until the upper surface of the silicon layer 3 is exposed,” forming sidewalls 9a/9b (“*second insulating sidewall*”; see *id.*, FIGS. 6, 9 (below) (shaded green)). Ex.1009, ¶114, Figure 10 (below-bottom). After this etching, the high-k dielectric film (see *id.*, FIGS. 6, 9-10 (below) (shaded red)) remains under the gate electrode and first and second sidewalls. Ex.1101, ¶¶179-80.



b. Fourth Embodiment

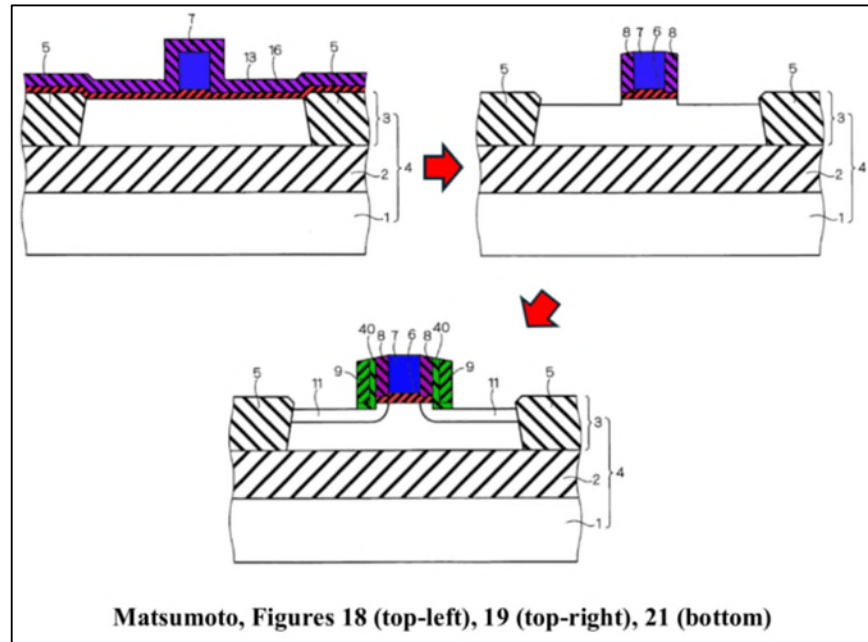
As shown in the enlargement of Matsumoto's Figure 22 and confirmed by Matsumoto's fabrication process teachings, high-k gate insulating film 6 (*see* Ex.1009, FIG. 22 (below) (shaded red)) is an uninterrupted layer (as evidenced by absence of gaps) extending from under the gate electrode to under only film 8 ("*first insulating sidewall*"). The high-k film is thinner under film 8 ("*first insulating sidewall*"; *see id.* (shaded purple)) than it is under the gate electrode (*see id.* (shaded

blue)). Matsumoto's fourth embodiment device therefore discloses limitations 1[e]-1[f]. See *Unified*, 2022 WL 500391, *17; Ex.1101, ¶¶181-82.



The fabrication process of Matsumoto's fourth embodiment device confirms the Figure 22 device structure. During fabrication, "gate electrode 7 is formed by Matsumoto's process described in the first preferred embodiment," resulting in high-k dielectric film 13 having a larger thickness under the gate electrode (see Ex.1009, FIG. 18 (below, top-left)). See *id.*, Ex.1009, ¶¶137, 107-08; Ex.1101, ¶183. The etching process that forms sidewall 8 ("the first insulating sidewall"; see Ex.1009, FIGS. 18-19, 21 (shaded purple)) "overetch[es] the upper surface of the silicon layer 3" and as a result, the high-k dielectric film (see *id.*, FIGS. 18-19, 21 (shaded red)) remains only under the gate and sidewall 8. *Id.*, ¶138, FIG. 19 (below, top-right); Ex.1101, ¶¶184-86. Film 40 and film 9 (alone or in combination the "second insulating sidewall" (see Ex.1009, FIG. 21 (below, bottom) (shaded green)) are then

formed on the outer side surfaces of film 8 and on the substrate surface. *Id.*, ¶139; Ex.1101, ¶¶184-86.

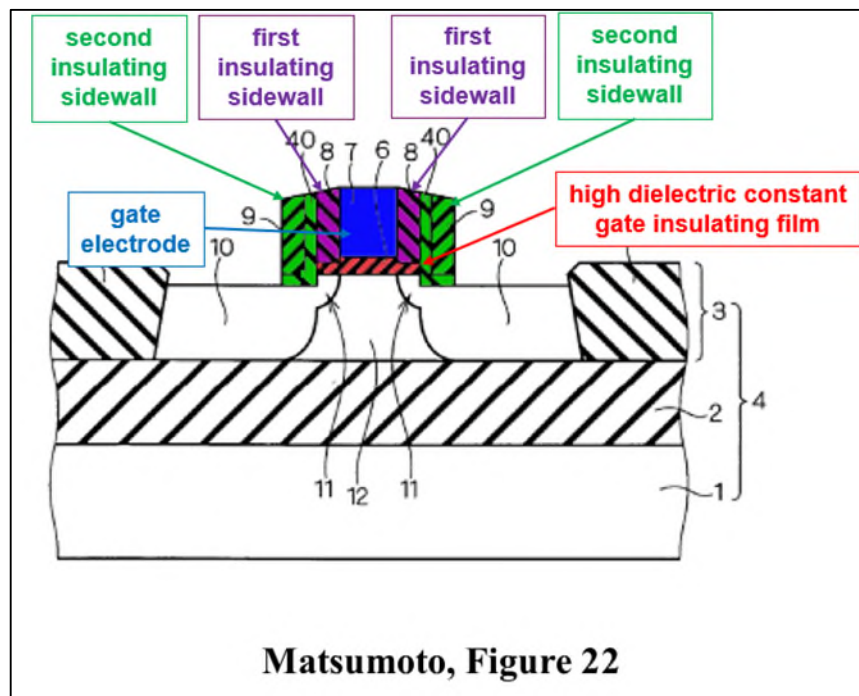
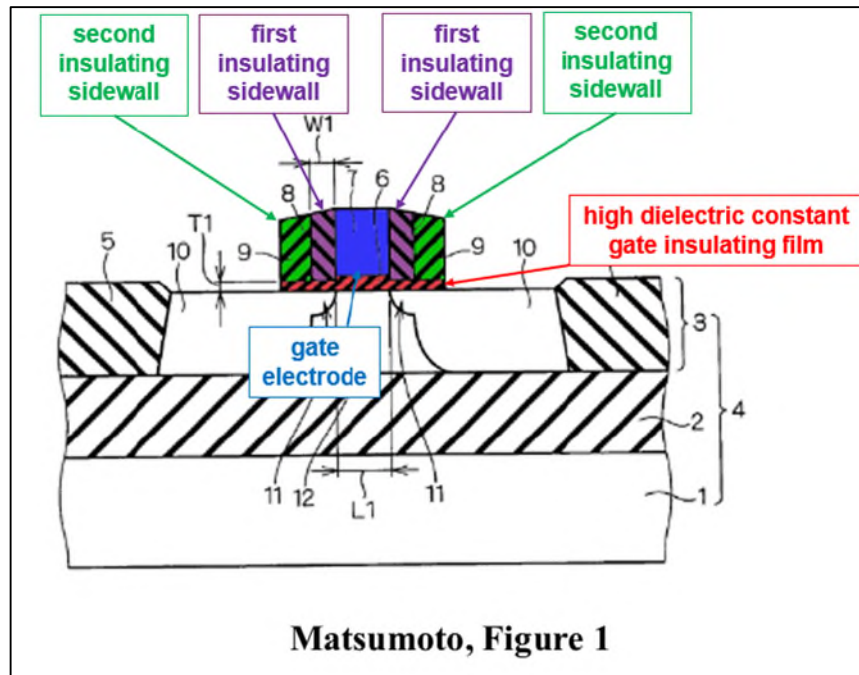


C. Claim 4

Matsumoto’s first and fourth embodiments each teaches “*the first insulating sidewall is an offset sidewall*” (Limitation 4). Ex.1101, ¶¶187-88.

In both embodiments, film 8 is the “*first insulating sidewall.*” §V.B.4. Matsumoto expressly refers to film 8, which is located between gate electrode 7 and the “*second insulating sidewall,*” as an “**offset** insulation film.” Ex.1009, ¶155 (“The relationship between the width W1 of the **silicon oxide film 8 serving as an offset insulation film**”), ¶157 (“FIG. 28 is a graph of the **width W1 of the offset insulation film** versus the delay time t_{pd} ...), FIG. 1 (below, showing width W1); see Google, 2022 WL 4287797, *9 n.9. Accordingly, in Matsumoto’s first and fourth

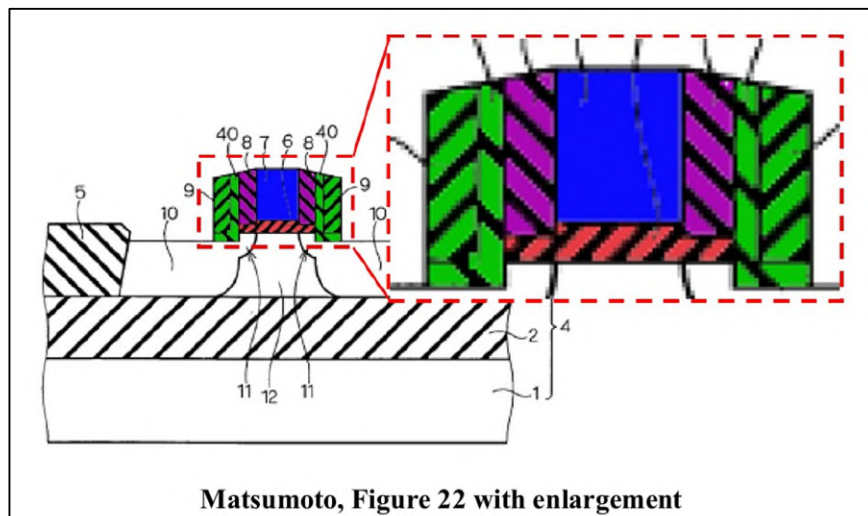
embodiment devices, film 8 “is an offset sidewall” (Limitation 4). Ex.1101, ¶¶187-88; Ex.1001, 7:37-39 (referring to inner sidewall as an offset sidewall), FIG. 2; Ex.1334, Figure 5-25.



D. Claim 5

Matsumoto’s fourth embodiment teaches “the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall” (Limitation 5). Ex.1101, ¶¶189-91.

As shown in the Matsumoto Figure 22 enlargement below and discussed in §V.B.5.b, high-k gate insulating film 6 (shaded red) extends only under film 8 (“*first insulating sidewall*”) and is not located under films 40 and 9 (alone or collectively the “*second insulating sidewall*”). See *Unified*, 2022 WL 500391, *17; Ex.1101, ¶¶189-90. The fabrication process of the fourth embodiment, discussed in §V.B.5.b, confirms the Figure 22 device structure. Ex.1009, ¶¶138-39.



E. Claim 14

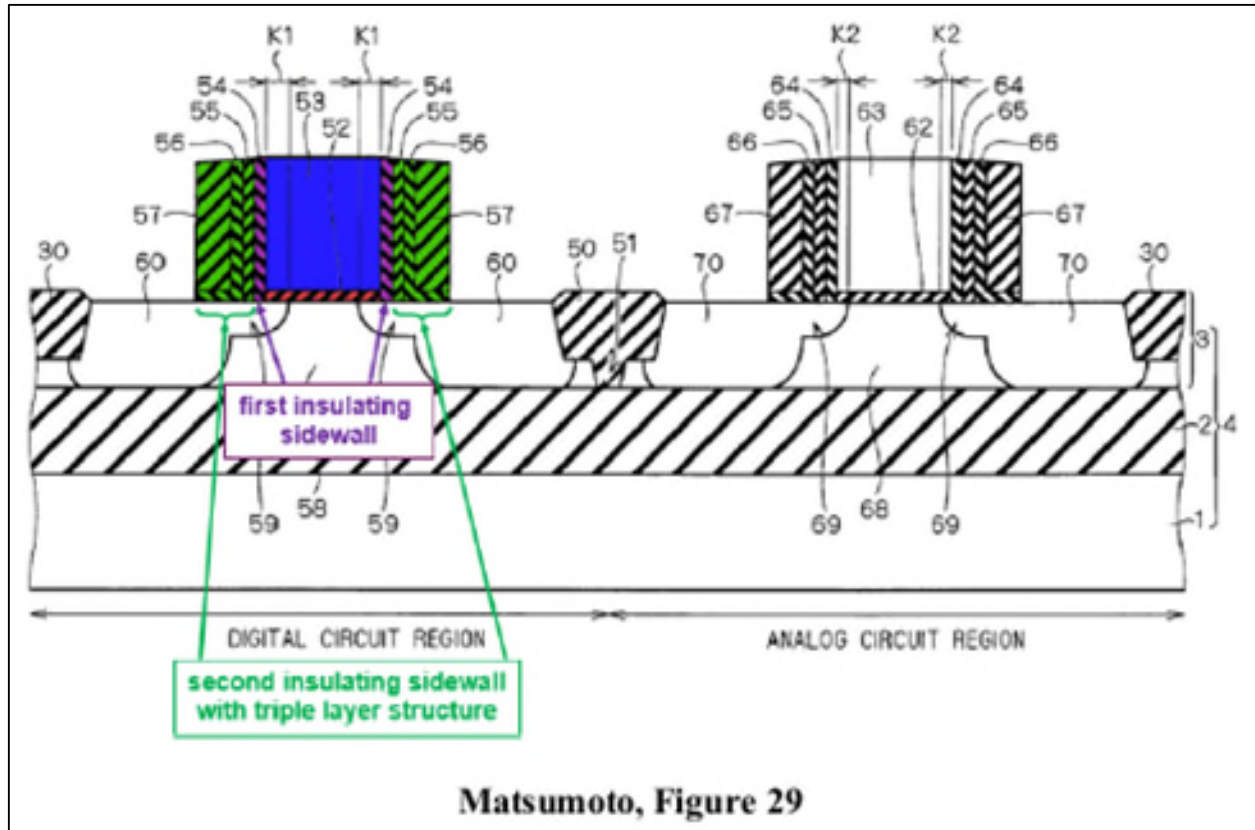
Matsumoto’s fourth embodiment teaches “*the second insulating sidewall has a double layer structure including an oxide film and a nitride film*” (Limitation 14). Ex.1101, ¶¶192-93.

As discussed in §V.B.4, silicon **nitride** film 9 and silicon **oxide** film 40 are collectively the “*second insulating sidewall*.” Ex.1101, ¶192. A POSITA would have considered the films to be “layers” of the collective sidewall structure, consistent with the ’764 patent’s disclosure. *Id.*; see Ex.1001, 20:66-21:8. Accordingly, in Matsumoto’s fourth embodiment, “*the second insulating sidewall has a double layer structure including an oxide film and a nitride film*” (Limitation 14). Ex.1101, ¶¶192-93.

F. Claim 15

Matsumoto renders obvious “*the second insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film*” (Limitation 15). Ex.1101, ¶¶194-99.

Matsumoto discloses a digital FET, isolated from analog device regions, that includes silicon oxide film 54 (“*first insulating sidewall*”; (Ex.1009, FIG. 29 (below) (shaded purple)) “formed in contact with each side surface of the gate electrode 53.” *Id.*, ¶¶160, 162. Film 54 functions as an “offset insulation film.” *Id.*, ¶162. Beyond this layer, “[a] silicon oxide film 55 is formed outside the silicon oxide film 54,” followed by a structure containing “a silicon oxide film 56 and a silicon nitride film 57.” *Id.* Together, silicon oxide films 55 (“*first oxide film*”) and 56 (“*second oxide film*”) along with silicon nitride film 57 (“*nitride film*”) form a “*second insulating sidewall*” with “*a triple layer structure*.” Ex.1101, ¶¶194-96.



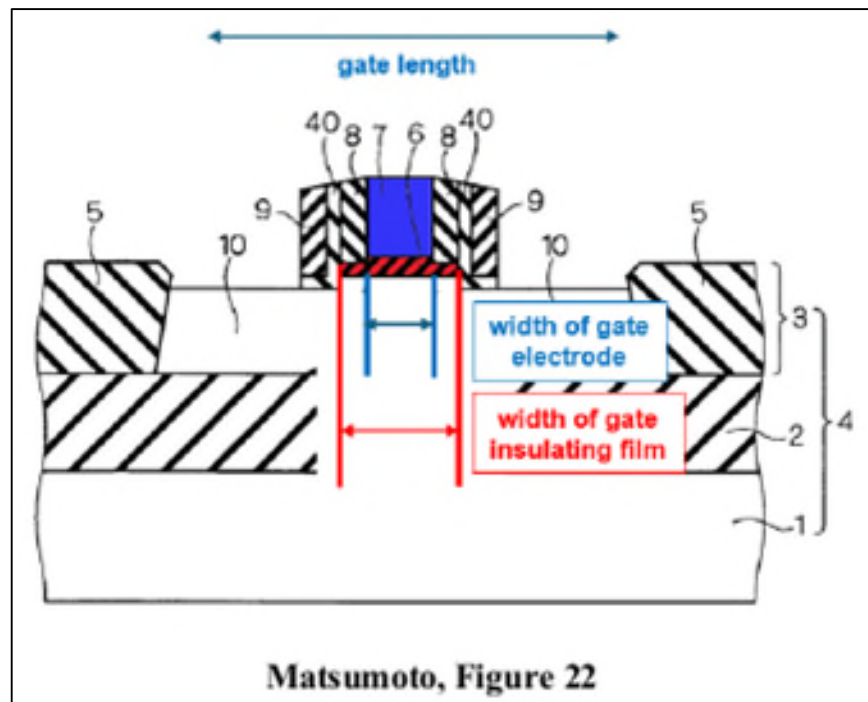
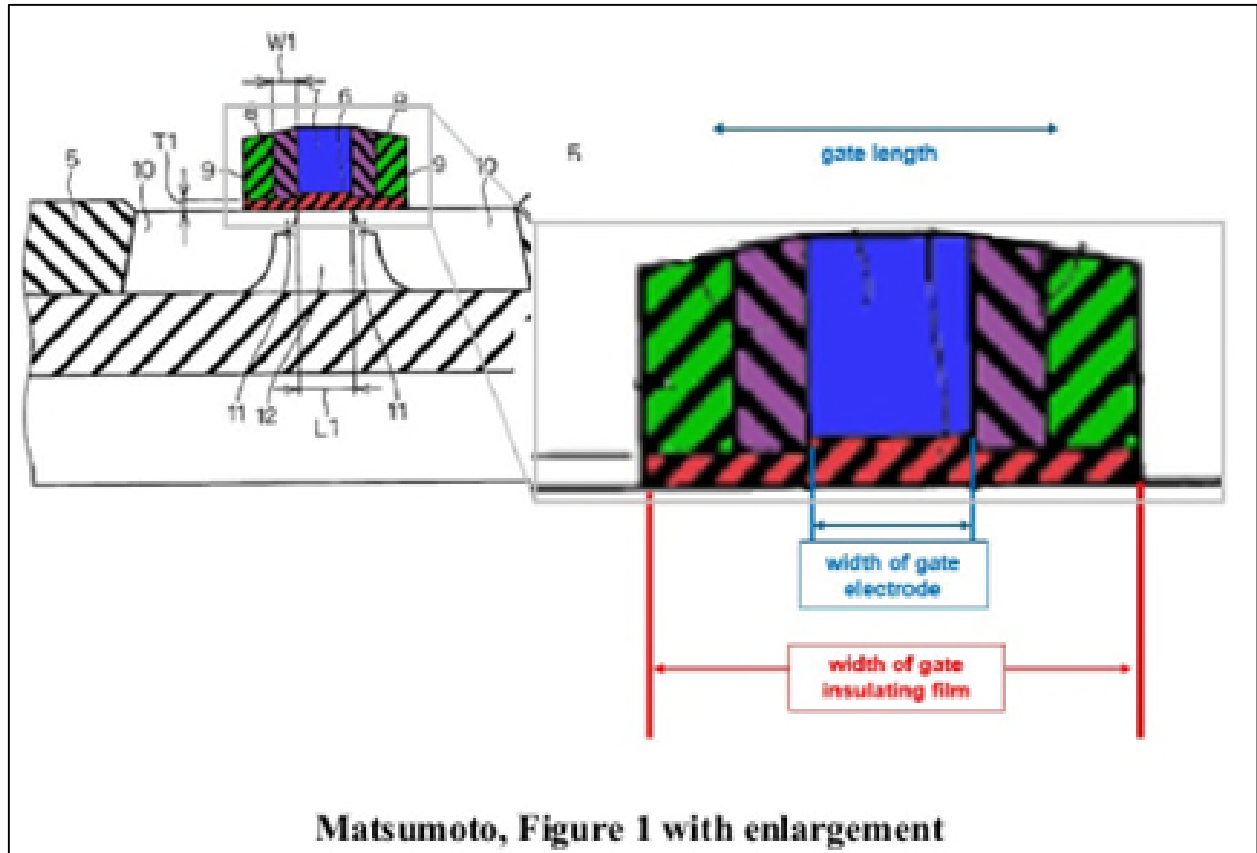
It would have been obvious to a POSITA to modify Matsumoto's fourth embodiment device by adding an additional oxide layer to the existing second insulating sidewall, which includes silicon nitride film 9 and silicon oxide film 40, as disclosed in Matsumoto's Figure 29 embodiment. Ex.1101, ¶197; *Boston Sci. Scimed, Inc. v. Cordis Corp.*, 554 F.3d 982, 991 (Fed. Cir. 2009) ("[c]ombining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness."). Matsumoto expressly motivates the combination, stating that "[t]he structure according to the sixth preferred embodiment [Figure 29] is applicable to the semiconductor device of any one of the first to fifth preferred embodiments." Ex.1009, ¶159; Ex.1101, ¶198.

G. Claims 16-17

Matsumoto's first and fourth embodiments each teaches "*a width of the high dielectric constant gate insulating film along a gate length¹³ is larger than a width of the gate electrode along the gate length*" (Limitation 16) and "*a width of a bottom surface of the high dielectric constant gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length*" (Limitation 17). Ex.1101, ¶¶200-03.

As established in §V.B.5, high-k gate insulating film 6 in Matsumoto's first and fourth embodiments extends from under the gate to under the first insulating sidewall 8. As illustrated in Figures 1 and 22 below, the width of Matsumoto's gate electrode 7 is constant across its entire height. The width of the high-k gate insulating film 6 (*see* Ex.1009, FIGS. 1 and 22 (below) (shaded red)), including at film 6's bottom surface, is larger than the width of the gate electrode 7 (*see id.*, shaded blue), including at gate electrode 7's bottom surface. Ex.1101, ¶¶201-02. The fabrication process of both embodiments discussed in §§V.B.5a-b confirms the structures of Figures 1 and 22. Ex.1101, ¶¶203.

¹³ The '764 patent uses the term "gate length" to refer to a direction, specifically from source to drain regions. Ex.1101, ¶200.



H. Claims 18-19

Matsumoto's first and fourth embodiments, using knowledge of a POSITA, as reflected in AAPA, renders "*the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more*" (Limitation 18) and "*the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall*" (Limitation 19) obvious. Ex.1101, ¶¶204-07.

The "*relative dielectric constant*" is an inherent property of a material. Ex.1101, ¶205. Indeed, the '764 patent admits a "high dielectric constant film formed of a Hf based oxide, Al based oxide or the like [] **has a relative dielectric constant of 10 or more**, instead of an SiO₂ based insulating film having a **relative dielectric constant of about 4.**" Ex.1001, 1:28-31 (background-AAPA). Although not mentioned in the '764 patent, the dielectric constant of Si₃N₄ is 7, a fact that would have been known to a POSITA. Ex.1018, Table 1. Matsumoto teaches use, *e.g.*, of "**Ta₂O₅**" as a gate insulating film. Ex.1009, ¶107. The dielectric constant for Ta₂O₅ is known to be 26, which is greater than 10. Ex.1018, Table I. Sidewall film 9 is comprised of silicon nitride (Si₃N₄), which has a dielectric constant of 7 and is therefore less than the dielectric constant for Ta₂O₅. Ex.1009, ¶¶114, 139; Ex.1018, Table I; Ex.1101, ¶206; Ex.1352, Fig. 4 (Si₃N₄ has dielectric constant of 7.2).

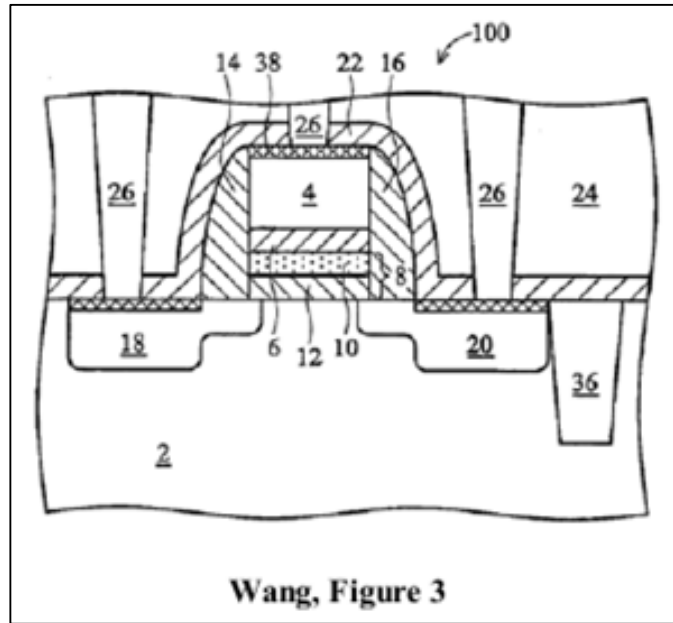
VI. GROUND II: Matsumoto-Wang Combination Renders 2-3, 6, and 11 Obvious.

Should PO argue Matsumoto does not expressly disclose “*a buffer insulating film*,” recited in claims 2-3, or a high-k film “*formed of a Hf based oxide*” (Limitation 6), “*of a HfSiON film*” (Limitation 7) or with “*thickness of 2 nm or less*” (Limitation 11), Wang discloses these limitations.

A. Wang

Wang’s transistor 100 includes a gate stack with high-k dielectric layer 6 formed on dielectric layer 8 comprising a nitrided portion 10 and a non-nitrided/substantially nitride-free portion 12. Ex.1012, ¶¶22, 24, 48, FIG. 3 (below). Wang and Matsumoto are in the same field as the ’764 patent, “a semiconductor device and a method for fabricating.” Ex.1001, 1:15-16; Ex.1009, ¶2; Ex.1012, ¶2; Ex.1101, ¶136.

Wang presents a list of alternatives for its high-k gate dielectric including Hf-based dielectrics (*e.g.*, HfO₂, HfSiO, HfON, or HfSiON). Ex.1012, ¶¶9, 25.

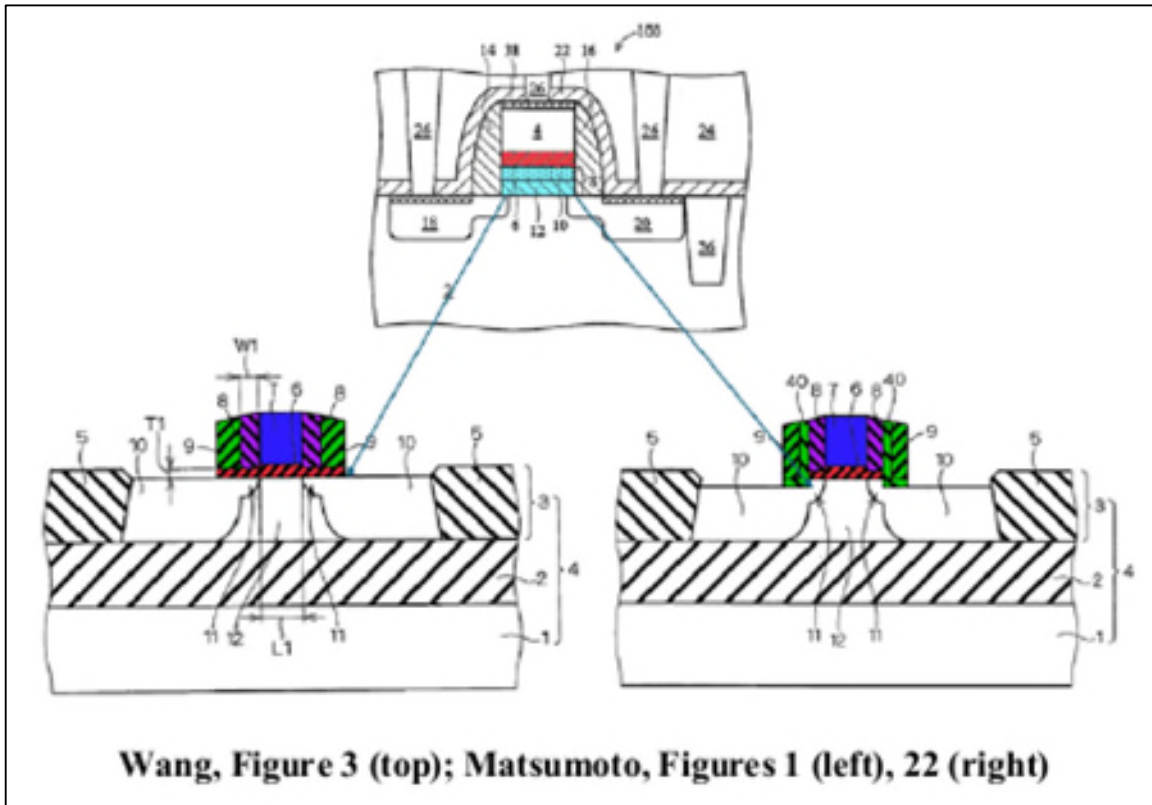


B. Claims 2-3

The combination of Matsumoto’s first and/or fourth embodiments and Wang discloses “a buffer insulating film between the substrate and the high dielectric constant gate insulating film” (Limitation 2) where “the buffer insulating film is a silicon oxide film” (Limitation 3). Ex.1101, ¶¶209-218.

A POSITA would have been motivated to combine Wang’s teachings regarding use of a dielectric layer between a high-k gate insulating film and the silicon substrate with Matsumoto’s first and/or fourth embodiment devices. Ex.1101, ¶209. For example, a POSITA would have been motivated to integrate Wang’s underlying dielectric layer 8 (see Ex.1012, FIG. 3 (below, top) (shaded aqua)) under Matsumoto’s high-k dielectric (see Ex.1009, FIGS. 1 (below, bottom

left), 22 (below, bottom-right) (shaded red)) in the first embodiment device (Figure 1) and fourth embodiment device (Figure 22). Ex.1101, ¶209.



Wang's underlying dielectric 8 is "preferably formed of silicon oxide" and "has a first, nitrided portion 10 that is in contact with high-k dielectric layer 6 and a second non-nitrided, or substantially nitrogen-free, portion 12 that is in contact with the underlying substrate 2." Ex.1012, ¶48. Underlying dielectric 8 is therefore a "buffer insulating film" and a "silicon oxide film" (e.g., in non-nitrided portion 12). Ex.1101, ¶¶201-11. Alternatively, portion 12 is the "buffer insulating film." *Id.* In the combination, Wang's underlying dielectric is between the substrate and Matsumoto's high-k gate insulating film 6. *Id.*

Wang explicitly motivates the above combination, teaching that “[d]ue to the undesirable interactions between high-k dielectrics and the underlying semiconductor material (usually silicon, germanium, silicon germanium, and the like) to degrade carrier mobility, a thin silicon oxide layer is typically employed as part of the gate dielectric even when a high-k gate dielectric is employed.” Ex.1012, ¶3. This is consistent with the purpose of the buffer insulating film in the ’764 patent. Ex.1001, 12:9-18 (by using a buffer insulating film, “deterioration of an interface between a substrate and a gate insulating film can be suppressed”). Wang further stresses that “underlying dielectric layer 8 advantageously provides higher mobility and higher reliability for the high-k peripheral (or I/O) device.” Ex.1012, ¶28. A POSITA would have therefore been motivated to use Wang’s buffer insulating layer to improve carrier mobility and performance of Matsumoto’s first and/or fourth embodiment devices. Ex.1101, ¶213; Ex.1009, ¶13 (describing objective to reduce malfunctions and operating characteristic variations).

Applying Wang’s buffer layer to Matsumoto’s first or fourth embodiment device is merely use of a known technique (Wang’s buffer insulating layer) to improve similar devices in the same way for the above reasons. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-17 (2007); Ex.1101, ¶215. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable because Wang uses established methods

for forming the underlying dielectric and its high-k gate dielectric. Ex.1012, ¶22 (describing “thermally grown oxide”), ¶24 (describing use of CVD, ALD and PVD for deposition of high-k film); Ex.1009, ¶107 (describing use of CVD for high-k film deposition); Ex.1101, ¶218.

C. Claim 6

The combination of Matsumoto’s first and/or fourth embodiments and Wang discloses “*the high dielectric constant gate insulating film is formed of a Hf based oxide*” (Limitation 6). Ex.1101, ¶¶219-223.

Matsumoto teaches use of a high-k film “such as Al₂O₃ or a ferroelectric film such as Ta₂O₅ and BST” as a gate insulating film. Ex.1009, ¶107. Wang teaches use of similar high-k dielectrics (*e.g.*, Al₂O₃ and Ta₂O₅) and others including “**HfSiON**” and “**HfO₂**.” Ex.1012, ¶12; *see also id.*, ¶¶9, 25.

By 2005, a POSITA would have been motivated to select a Hf-based oxide, such as HfO₂, given its known benefits, including, for example, “its superior thermal stability with poly-Si and reasonable band alignment.” Ex.1337, 2.4.1; Ex.1213, 207 (HfO₂ “combines a high k (15–26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ...”); Ex.1349, 134 (“Excellent dielectric properties ... suggest that HfO₂ is a promising material for the future gate dielectric application.”); Ex.1101, ¶221. Another benefit that would have

been known to a POSITA is that HfO_2 can be scaled down to a smaller EOT. Ex.1213, 207; Ex.1101, ¶221.

D. Claim 11

Wang further teaches that for a HfSiON gate insulating layer, the film “was deposited to a thickness of about 5 to 50 Angstroms [0.5 to 5 nm] and having an equivalent oxide thickness (EOT) of less than about 2.0 nanometers.” Ex.1012, ¶34. Thus, in combination with Matsumoto, the thickness of the HfSiON gate insulating film at its side ends would also range from about less than 5 Angstroms to less than 50 Angstroms since the thickness of the layer is smaller under sidewall 8 than under the gate electrode 7. Ex.1101, ¶224. The thickness of 2 nm (20 Angstroms) falls within the range of thicknesses disclosed by Wang. Ex.1101, ¶226.

The '764 patent provides no discussion, evidence, or justification for the selection of 2 nm as the thickness of the gate insulating film. “[W]here there is a range disclosed in the prior art, and the claimed invention falls within that range, the burden of production falls upon the patentee to come forward with evidence of teaching away, unexpected results or criticality, or other pertinent objective indicia indicating that the overlapping range would not have been obvious in light of that prior art.” *E.I. DuPont de Nemours & Co. v. Synvina C.V.*, 904 F.3d 996, 1008 (Fed. Cir. 2018). Thus, the Matsumoto-Wang combination renders obvious that “*each side end portion of the high dielectric constant gate insulating film has a thickness of 2*

nm or less” (Limitation 11). *Ormco Corp. v. Align Tech., Inc.*, 463 F.3d 1299, 1311 (Fed. Cir. 2006) (citation omitted) (“Where a claimed range overlaps with a range disclosed in the prior art, there is a presumption of obviousness.”); Ex.1101, ¶¶225-28.

VII. GROUND III: Matsumoto-Wang-Sim Combination Renders Claim 11 Obvious.

Should an argument be made the combination of Matsumoto and Wang does not render claim 11 obvious, Sim explicitly describes use of a gate insulating film having a thickness 2 nm or less, as required by claim 11. Sim, like Matsumoto and Wang, is in the same field as the ’764 patent, “a semiconductor device and a method for fabricating.” Ex.1001, 1:15-16; Ex.1009, ¶2; Ex.1012, ¶2; Ex.1024, Abstract; Ex.1101, ¶139.

Sim highlights that “[h]afnium-based high-k dielectrics and metal gate electrodes have been aggressively investigated to ensure continued scaling of CMOS technology, but several drawbacks such as low mobility and charge trapping have been identified.” Ex.1024, 218. To address these issues, Sim “systematically evaluated the effects of high-k film thickness on charge trapping and channel carrier mobility” and found that “scaling the high-k dielectric is a simple, but very effective means of improving mobility and other reliability characteristics.” *Id.* Specifically, Sim concluded that “[s]caling the physical thickness of the HfO₂ dielectric to below 20Å [2 nm] causes less charge trapping and higher mobility.” Ex.1024, 221.

Wang discloses use of HfO_2 as a high-k gate dielectric (Ex.1012, ¶12), the same film studied in Sim. A POSITA would have been motivated to adopt Sim's solution of forming a gate insulating film with a thickness of $20\text{\AA}$ (2 nm) or less in the combined device(s) of Matsumoto's first and/or fourth embodiments and Wang. Ex.1101, ¶234. Accordingly, because the thickness of the high-k film is smaller under sidewall 8 than under the gate electrode 7, the combination of Matsumoto's first and/or fourth embodiments, Wang, and Sim discloses "*each side portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less*" (Limitation 11). *Id.*

Sim expressly motivates the combination, finding that reducing the thickness of HfO_2 to below $20\text{\AA}$ (2 nm) enhances mobility and reduces charge trapping, key issues in ensuring the performance and scalability of semiconductor devices. Ex.1024, 221; Ex.1101, ¶235. Sim's teachings are consistent with Wang's goal of using a thickness of "preferably less than about $50\text{\AA}$ to maintain low gate leakage and thin equivalent oxide thickness (EOT)." Ex.1012, ¶26.

Additionally, the combination is nothing more than use of a known technique (Sim's HfO_2 dielectric layer with less than $20\text{\AA}$ (2 nm) thickness) to improve similar devices in the same way for the above reasons. *KSR*, 550 U.S. at 416-17; Ex.1101, ¶236. A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable at least because Sim uses a well-

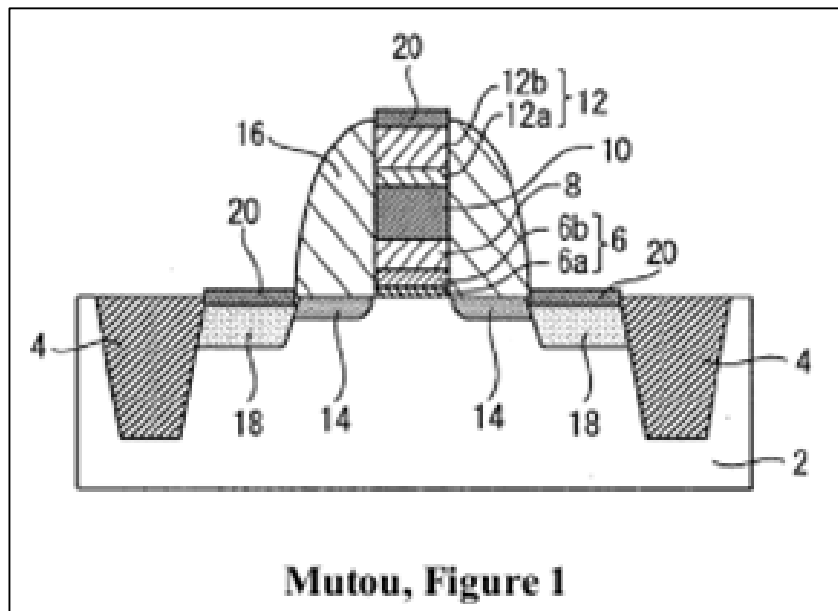
known process, atomic layer deposition (ALD), for fabricating high-k films. Ex.1024, 218; Ex.1101, ¶236.

VIII. GROUND IV: Matsumoto-Mutou Combination Renders Claims 2-3 Obvious.

Should an argument be made the combination of Matsumoto and Wang fails to render claims 2-3 obvious, Mutou also explicitly describes a “*buffer insulating film*,” and the Matsumoto-Mutou combination renders claims 2-3 obvious.

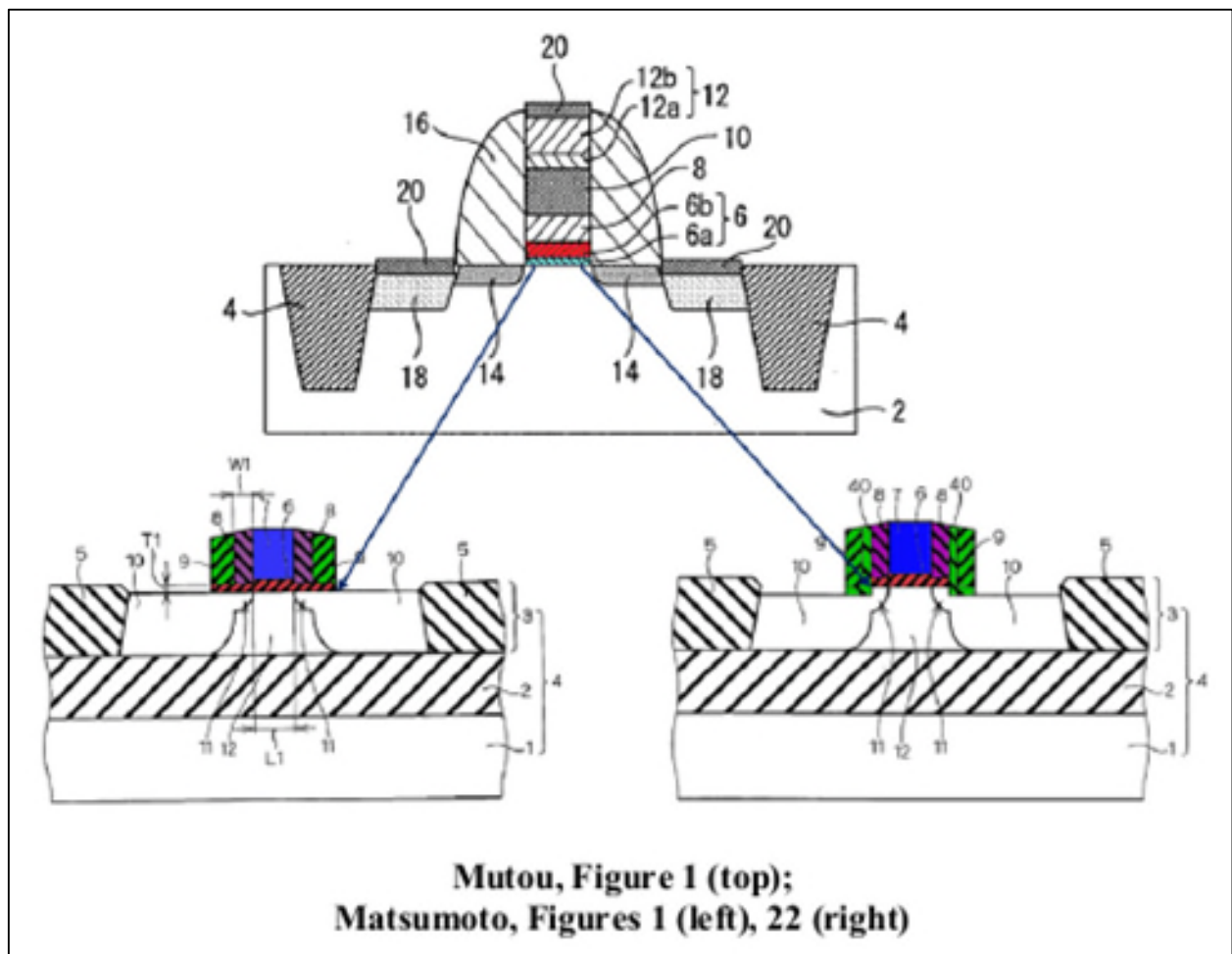
A. Mutou

Mutou’s device includes silicon substrate 2 and a gate stack comprising interfacial layer 6a, high-k dielectric film 6b, and a multilayer gate electrode. Ex.1019, ¶¶40-41, 44, FIG. 1 (below). Mutou and Matsumoto are in the same field as the ’764 patent, “a semiconductor device and a method for fabricating.” Ex.1001, 1:15-16; Ex.1009, ¶2; Ex.1019, Abstract, ¶¶2, 4; Ex.1101, ¶141.



B. Motivation to Combine

A POSITA would have been motivated to integrate Mutou's underlying interfacial layer 6a (“*buffer insulating film*”) (see Ex.1019, FIG. 1 (below, top) (shaded aqua)) under Matsumoto's high-k dielectric (see Ex.1009, FIG. 1 (below, bottom-left), 22 (below, bottom-right) (shaded red)) in the first embodiment (Figure 1) and/or fourth embodiment (Figure 22) devices, as shown below. Ex.1101, ¶229.



Mutou expressly motivates the combination, teaching “[t]he underlying interfacial layer 6a is acted to inhibit interfacial reaction between the silicon

substrate 2 and the high-k dielectric film 6b.” Ex.1019, ¶42. Inhibiting such reactions between the substrate and the high-k film decreases degradation of the high-k film and, thus, improves performance of the device. Ex.1101, ¶242; Ex.1001, 12:9-18 (by using a buffer insulating film, “deterioration of an interface between a substrate and a gate insulating film can be suppressed”). This furthers the Matsumoto’s goal “to provide a semiconductor device which achieves reductions in malfunctions and operating characteristic variations.” Ex.1009, ¶13. Based on these disclosures, a POSITA would have been motivated to make the above combination to inhibit interfacial reaction between the substrate and the high-k film and improve performance of Matsumoto’s devices. Ex.1101, ¶243.

The above combination is nothing more than use of a known technique (Mutou’s underlying interfacial layer) to improve similar devices in the same way for the above reasons. *KSR*, 550 U.S. at 416-17; Ex.1101, ¶244. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable because Mutou uses conventional processes to form the underlying interfacial layer and deposit the high-k gate insulating film on top. Ex.1019, ¶¶53-54; Ex.1009, ¶107; Ex.1101, ¶245.

C. Claims 2-3

Mutou’s interfacial layer 6a is formed on the silicon substrate 2 and high-k dielectric film 6b is formed on interfacial layer 6a. Ex.1019, ¶41. Mutou’s interfacial

layer 6a, as used in Matsumoto's first and fourth embodiments, is "*a buffer insulating film.*" Ex.1101, ¶239. Underlying interfacial layer 6a may be, "for example, a SiO₂ film, a Si₃N₄ film, or a SiON film" Ex.1019, ¶42.

Thus, the combination of Matsumoto's first and/or fourth embodiments and Mutou discloses "*a buffer insulating film between the substrate and the high dielectric constant gate insulating film*" (Limitation 2) where "*the buffer insulating film is a silicon oxide film*" (Limitation 3). Ex.1101, ¶¶239-47.

IX. GROUND V: Matsumoto-Ono Combination Renders Claims 6, 12, and 13 Obvious.

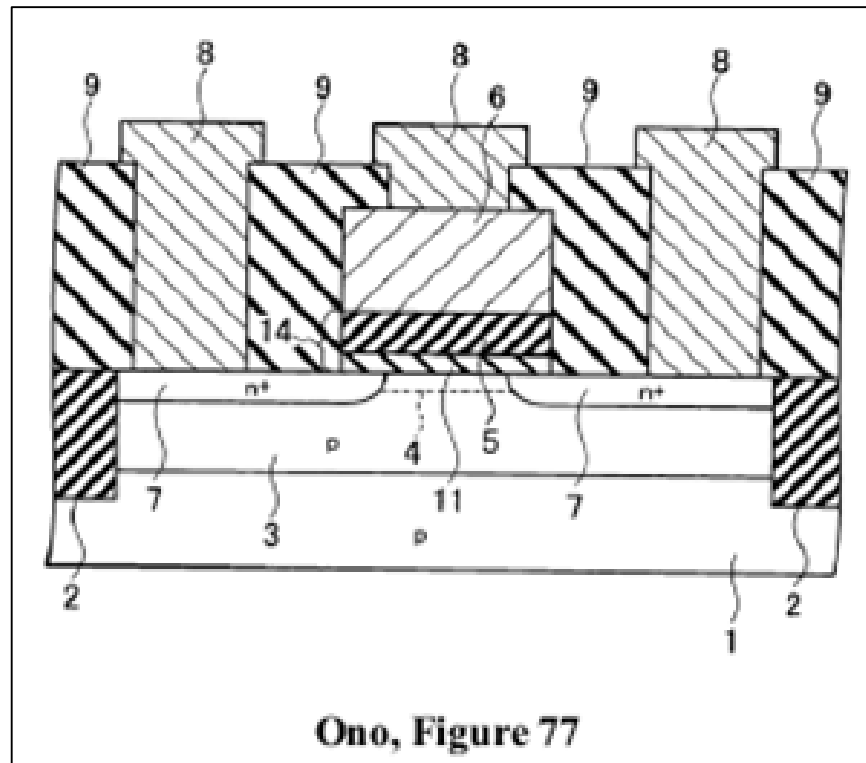
Should PO argue Matsumoto's first and/or fourth embodiment devices do not expressly disclose "*the high dielectric constant gate insulating film is formed of a Hf based oxide*" (Limitation 6) or that the high-k film's side surface "*is located at a predetermined distance from a side end surface of the first insulating sidewall toward the gate electrode*" (Limitation 12) or "*is located at a predetermined distance from a side end surface of the gate electrode toward the first insulating sidewall*" (Limitation 13), Ono teaches these limitations, and the Matsumoto-Ono combination renders claims 6, 12, and 13 obvious.

A. Ono¹⁴

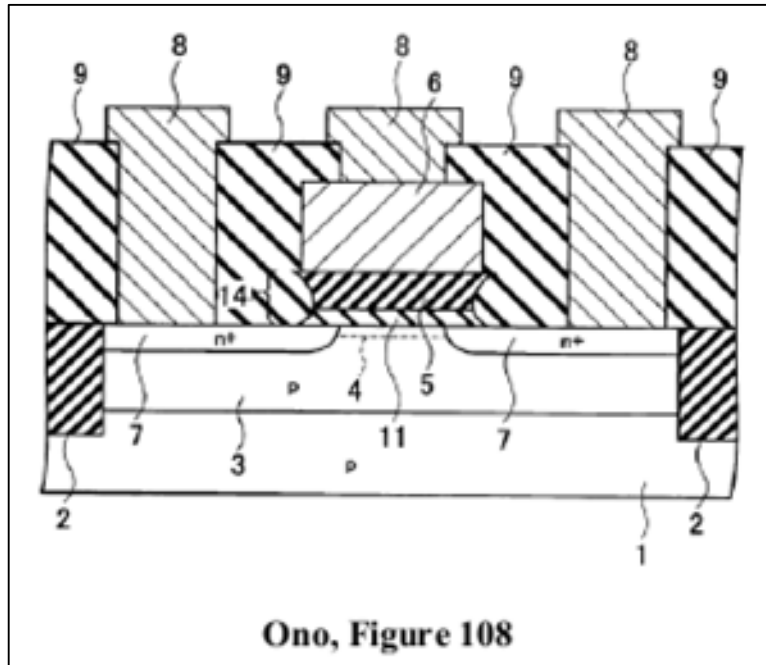
Ono's second embodiment FET includes a gate stack comprising gate insulator film 5 "made of a metal oxide" and gate insulator film 11 "made of a metal oxide with a higher dielectric constant than the gate insulator film 5." Ex.1013, ¶207, FIG. 77 (below). Gate insulator film 5 is made of a "HfO₂ film." Ex.1013, ¶209. Gate electrode 6 is formed on gate insulator film 5 and can have gate sidewalls.

¹⁴ None of the ground references was applied by the Examiner during prosecution of the '764 patent. Applicant cited JP-Ono on an information disclosure statement ("IDS"). However, JP-Ono has no familial relationship to Ono, is not a foreign counterpart to JP-Ono, does not have the same specification as Ono, and was filed by different inventors than Ono. See Ex.1340, cover ("Ono Tamashiro"); compare Ex.1013, cover ("Mizuki Ono"). JP-Ono was not applied by the Examiner and thus was not evaluated during examination. Significantly, Applicant supplied JP-Ono with its IDS in the Japanese language with only an English language abstract. See Ex.1112. Even assuming JP-Ono was evaluated by the Examiner, which the record does not support, the Examiner erred in allowing the claims over JP-Ono and by failing to recognize its teachings relating to the side end of the gate insulating film, which is understandable in view of the limited English language content of JP-Ono submitted by the Applicant.

Ex.1013, ¶¶207, 181, 210, FIG 77 (below); Ex.1101, ¶144. Ono and Matsumoto are in the same field as the '764 patent. Ex. 1001, 1:15-16; Ex.1009, ¶2; Ex.1013, Abstract, ¶¶3-7; Ex.1101, ¶143.

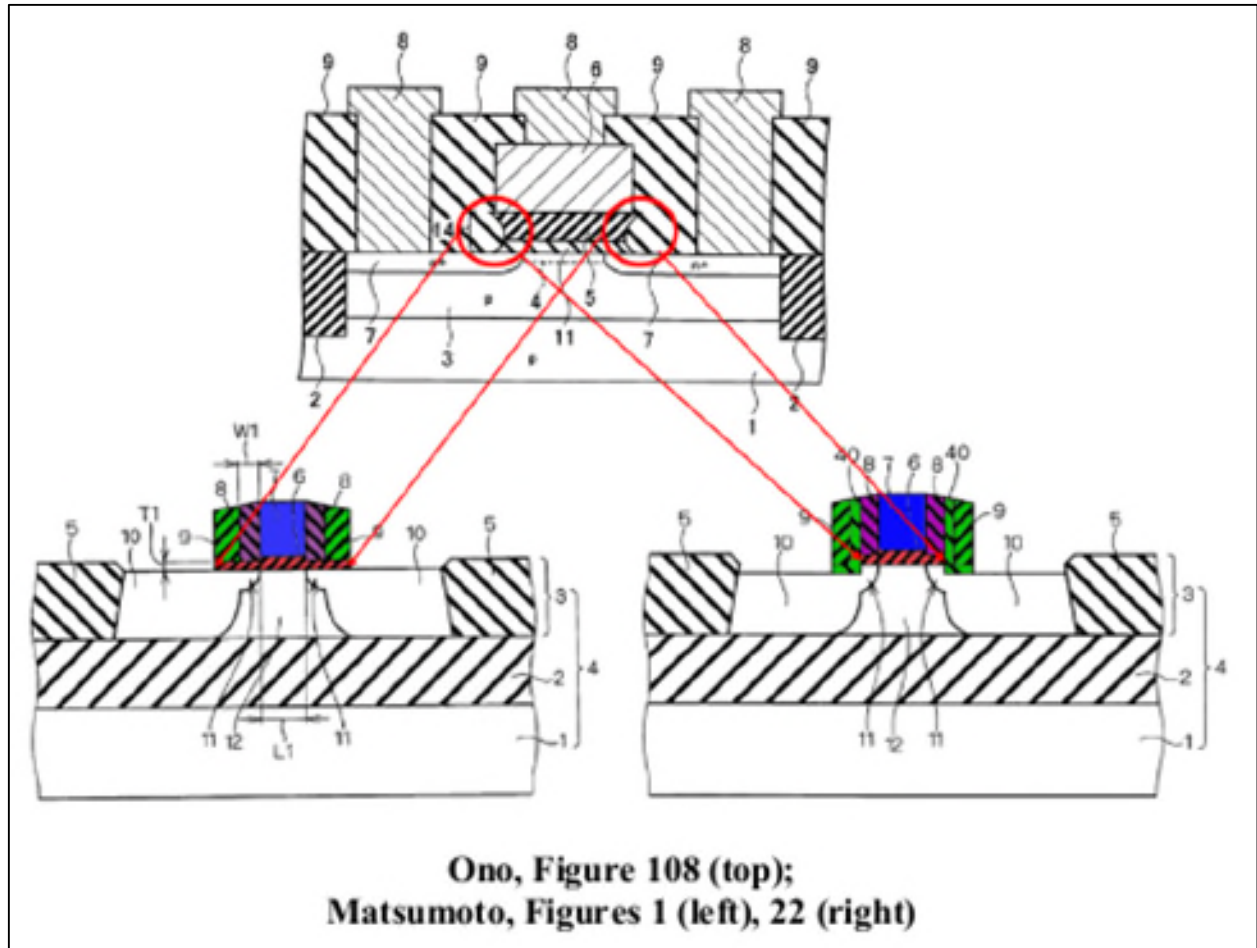


Ono discloses a modification of its second embodiment device where the side end portions of its gate insulating film “may curve.” Ex.1013, ¶216. Ono discloses numerous examples of such curved end portions. *See, e.g., id.*, FIGS. 104-23. Petitioner focuses its analysis on the structure depicted in Figure 108 (below), although other structures are equally applicable.



B. Motivation to Combine

A POSITA would have been motivated to apply Ono's teaching of curving the end portion of a gate insulating film to Matsumoto's first and/or fourth embodiment device(s), as shown below. Ex.1101, ¶250. Thus, in the combination, the side ends of Matsumoto's gate insulating film have a semicircular shape, as taught by Ono.



Ono expressly suggests the combination, teaching that using curved side surfaces for the gate insulating film “reduc[es] the scattering of carriers as well as enhanc[es] the controllability of the gate electrode with respect to the potential of the channel region” and therefore provides “an advantage of optimization.” Ex.1013, ¶216, ¶200 (noting, for the first embodiment, by using curved side surfaces, “the electrical capacitance between the gate electrode 6 and the source/drain regions 7 may be adjusted,” resulting in “an advantage of optimization”). A POSITA would have been further motivated to curve the end of Matsumoto’s gate insulating film to

optimize parasitic resistance and parasitic capacitance, improving device performance. Ex.1101, ¶257; Ex.1340, ¶108; §IV.B.2.

The Matsumoto-Ono combination is merely the application of a known technique (Ono's curved film ends) to improve similar devices in the same way for the above reasons. *KSR*, 550 U.S. at 416-17; Ex.1101, ¶258. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable. *Id.* Matsumoto and Ono both use high-k gate insulating films that extend under the gate electrode and the insulating sidewall, a concept well-known before the '764 patent. §§IV.B.2.b, IV.D.2, V.B.5, IX.A. Both Matsumoto and Ono also form their high-k dielectrics using conventional techniques. Ex.1009, ¶114; Ex.1013, ¶167; Ex.1101, ¶258.

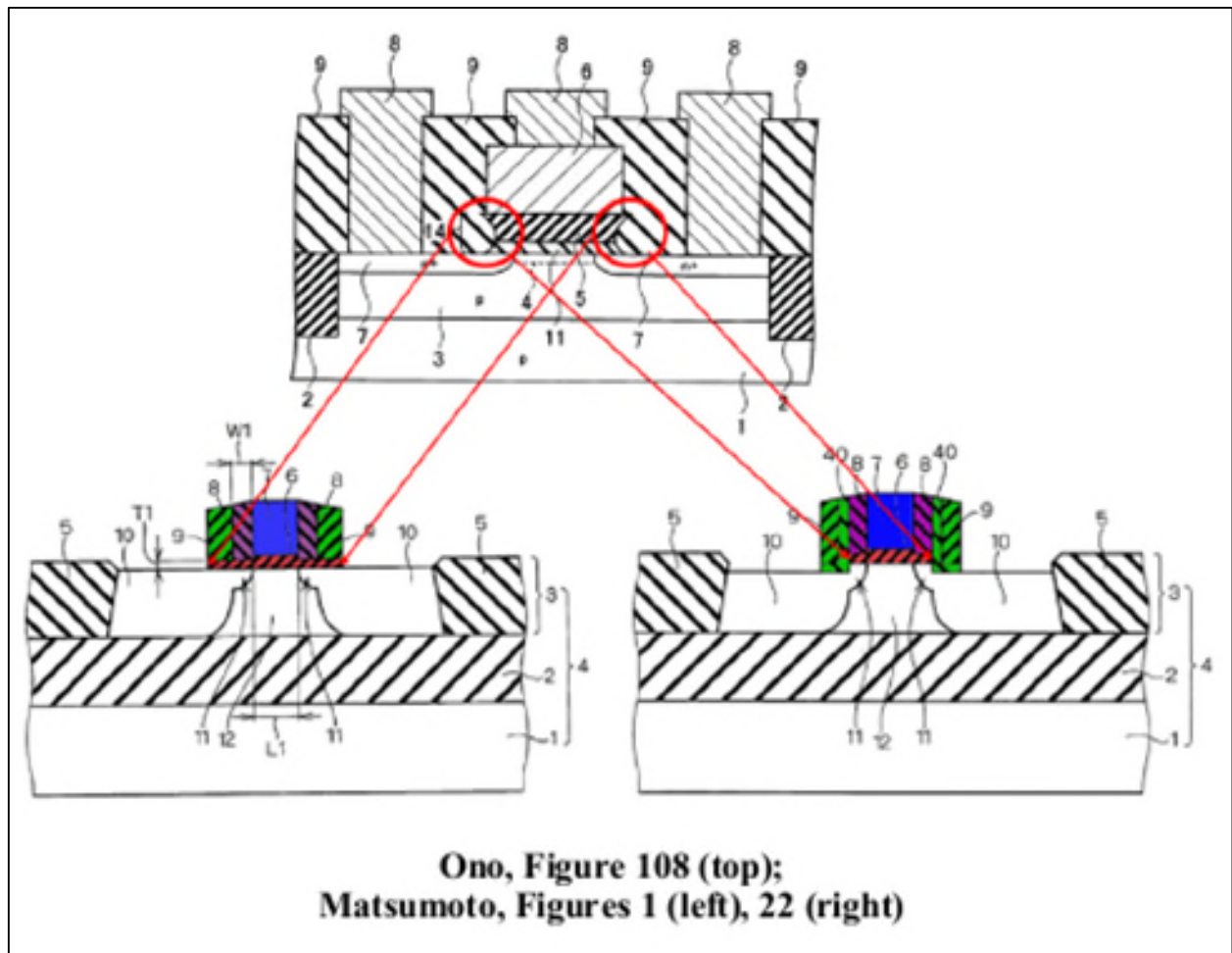
C. Claim 6

The combination of Matsumoto's first and/or fourth embodiments and Ono discloses "*the high dielectric constant gate insulating film is formed of a Hf based oxide*" (Limitation 6). Ex.1101, ¶¶249-51. Ono's gate insulator film 5 is made of a "HfO₂ film." Ex.1013, ¶209. As discussed in §VI.C, a POSITA would have been motivated to use a Hf-based oxide as a gate insulating layer as taught by Ono in Matsumoto's first and/or fourth embodiments. Ex.1101, ¶¶249-51.

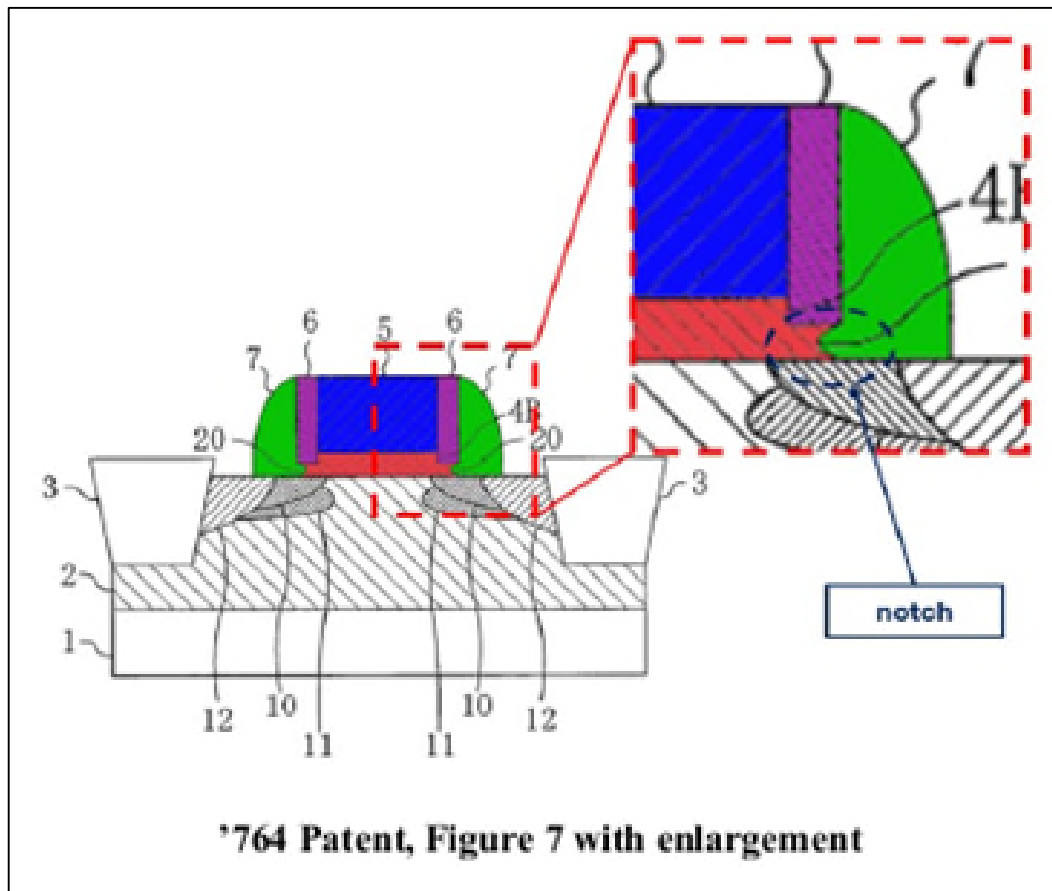
D. Claims 12-13

The combination of Matsumoto's first and/or fourth embodiments and Ono discloses "*is located at a predetermined distance from a side end surface of the first insulating sidewall toward the gate electrode*" (Limitation 12) or "*is located at a predetermined distance from a side end surface of the gate electrode toward the first insulating sidewall*" (Limitation 13). Ex.1101, ¶¶252-59.

In the devices of the Matsumoto-Ono combination, the end portion of Matsumoto's gate insulating film has a semicircular shape under the sidewall, as taught by Ono in, *e.g.*, Figure 108 (below, top).



Consistent with the '764 patent's disclosure, the semicircular shape of the gate insulating film's side end in the combination discloses "a notch." See, e.g., Ex.1001, 8:35-40 (referring to notch 20 of FIG. 7), FIG. 7 (below) (depicting notch 20 having a semicircular shape); Ex.1101, ¶253.



Additionally, in the combination of Matsumoto's fourth embodiment (Figure 22) and Ono, when the semicircular notch is applied at each side end of Matsumoto's gate insulating film 6 located under the first insulating sidewall film 8, the end of the gate insulating film no longer extends completely under the first insulating sidewall. The notch's semicircular shape (as taught by Ono) and the distance which the semicircular shape extends inward toward the gate electrode are set by specific process parameters. Ex.1101, ¶254.

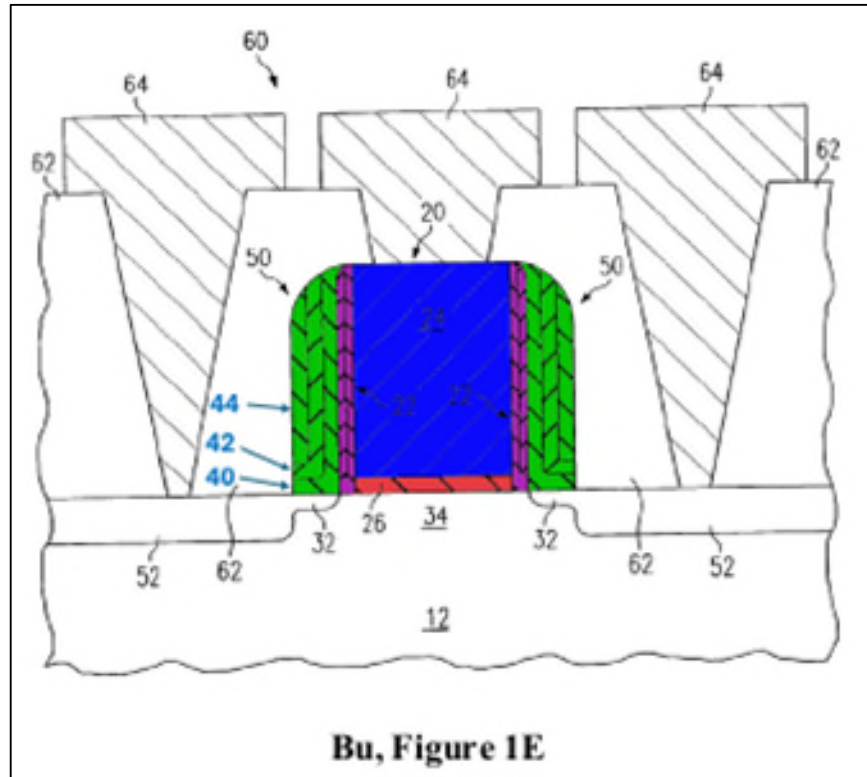
Accordingly, in the combination of Matsumoto's fourth embodiment and Ono, the gate insulating film's side surface is "*located at a predetermined distance*

from a side end surface of the first insulating sidewall toward the gate electrode” (Limitation 12) and *“located at a predetermined distance from a side end surface of the gate electrode toward the first insulating sidewall”* (Limitation 13), consistent with the ’764 patent’s disclosure. Ex.1001, 21:26-30 (“side surface ... may be located at a predetermined distance from a side end surface of the sidewall 7 or the offset sidewall 6 toward the gate electrode 5”); Ex.1101, ¶¶255-59.

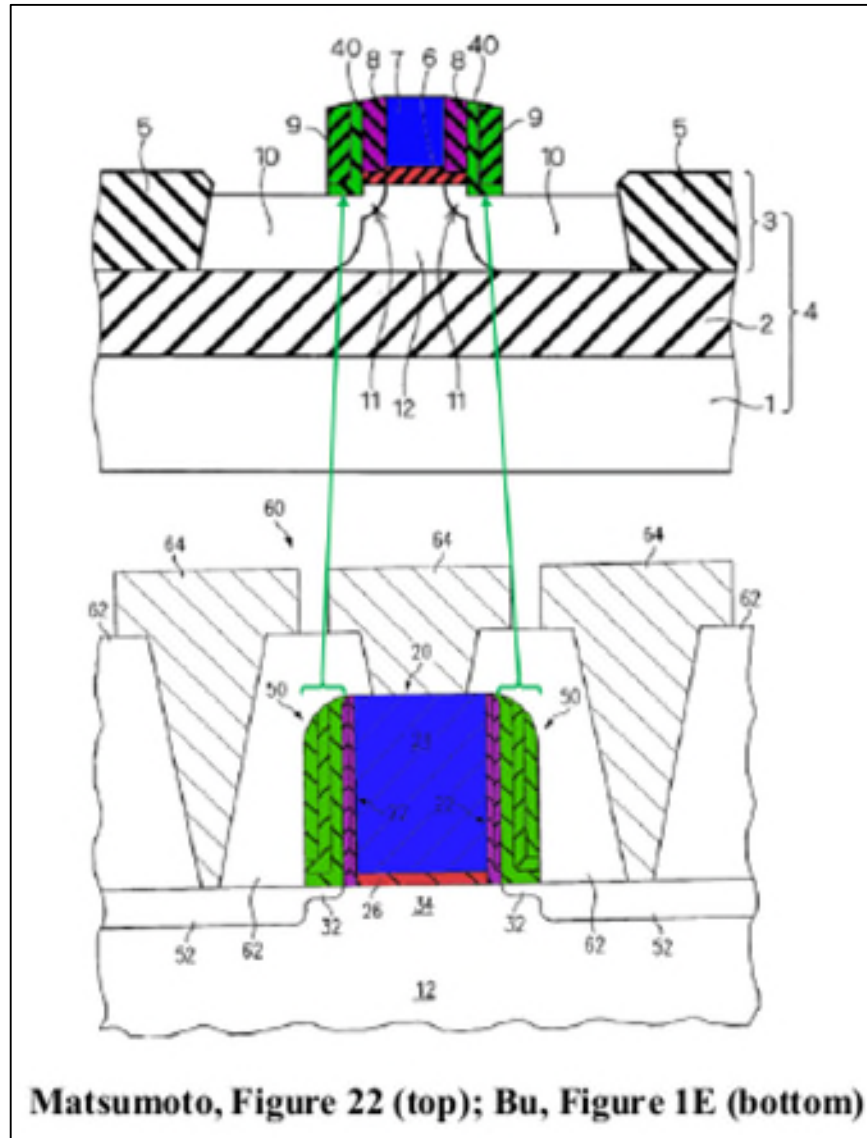
X. GROUND VI: Matsumoto-Bu Combination Renders Claim 15 Obvious.

Should PO argue Matsumoto fails to render claim 15 obvious, Bu discloses an outer sidewall with *“a triple layer structure”* (Limitation 15). Ex.1101, ¶¶260-65.

Bu’s transistor includes gate stack 20, comprising gate conductor 24 (*see* Ex.1025, FIG. 1E (below) (shaded blue)) and gate insulator 26 (*see id.* (shaded red)), and sidewall spacers 22 (*see id.* (shaded purple)). Ex.1025, ¶42. Bu’s transistor further includes an outer sidewall formed on sidewall spacers 22 having a triple-layer ONO structure: first sidewall-forming layer 40, comprised of **“oxide”**; second sidewall-forming layer 42, comprised of **“nitride”**; and third sidewall-forming layer 44, comprised of **“oxide”**. Ex.1025, ¶¶26-27, 30, 35, 43, FIG. 1E. Bu and Matsumoto are in the same field as the ’764 patent. Ex.1001, 1:15-16; Ex.1009, ¶2; Ex.1025, Abstract; Ex.1101, ¶146.



Matsumoto’s fourth embodiment includes inner “first sidewall” 8 and an outer “second sidewall” comprised of oxide film 40 and nitride film 9. Ex.1009, ¶¶110, 139, FIG. 22. A POSITA would have been motivated to use Bu’s triple-layer ONO sidewall structure with Matsumoto’s fourth embodiment device. Specifically, a POSITA would have been motivated to add an additional oxide layer to Matsumoto’s second sidewall (see Ex.1009, FIG. 22 (below top) (shaded green)), as taught by Bu (see Ex.1025, FIG. 1E (below, bottom)). Ex.1101, ¶262. The resulting device of the combination of Matsumoto and Bu discloses that “*the second insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film*” (Limitation 15). *Id.*, ¶264.



A POSITA would have specifically integrated Bu’s triple-layer ONO sidewall structure teachings into Matsumoto’s fourth embodiment device given the well-known benefits of ONO structures, including, for example, allowing independent control of spacer dimensions to optimize device scaling. Ex.1101, ¶263; Ex.1350, ¶¶5-6, FIG. 4. Bu further notes the benefits of using different materials in the sidewall structure: “film properties of sidewall-forming layers 40 and 42 may

minimize dopant loss from source drain extension region 32 to first sidewall-forming layer 40. Accordingly, parasitic resistance may be lowered.” Ex.1025, ¶26. A POSITA would have been motivated to make the combination to obtain these benefits and improve device performance and reliability. Ex.1101, ¶263.

The Matsumoto-Bu combination represents nothing more than use of a known technique (Bu’s triple-layer sidewall) to improve similar devices in the same manner for the above reasons. *KSR*, 550 U.S. at 416-17; Ex.1101, ¶264. A POSITA would have had a reasonable expectation of success in the combining these references, leading to predictable results, because both Matsumoto and Bu disclose forming sidewall layers using standard deposition and etching techniques, making the application of Bu’s triple layer structure to Matsumoto’s design straightforward. Ex.1009, ¶¶139, 162, Figure 29; Ex.1025, ¶¶27, 30, 35, 38; Ex.1101, ¶264.

XI. GROUND VII: Matsumoto-Wilk Combination Renders Claims 18-19 Obvious.

Should PO argue Matsumoto’s disclosure as informed by knowledge of a POSITA and AAPA fails to teach claims 18-19, Wilk, “High-k Gate Dielectrics: Current Status and Materials Properties considerations,” discloses the limitations of those claims.

Wilk explores the properties of materials “under consideration” in 2001 “as potential replacements for SiO₂ as the gate dielectric material for sub-0.1 μm CMOS

technology.” Ex.1018, Abstract. Wilk discloses the following table of relevant properties, including dielectric constants, for various materials:

TABLE I. Comparison of relevant properties for high- κ candidates.				
Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si	Crystal structure(s)
SiO ₂	3.9	8.9	3.2	Amorphous
Si ₃ N ₄	7	5.1	2	Amorphous
Al ₂ O ₃	9	8.7	2.8 ^a	Amorphous
Y ₂ O ₃	15	5.6	2.3 ^a	Cubic
La ₂ O ₃	30	4.3	2.3 ^a	Hexagonal, cubic
Ta ₂ O ₅	26	4.5	1–1.5	Orthorhombic
TiO ₂	80	3.5	1.2	Tetrag. ^c (rutile, anatase)
HfO ₂	25	5.7	1.5 ^a	Mono. ^b , tetrag. ^c , cubic
ZrO ₂	25	7.8	1.4 ^a	Mono. ^b , tetrag. ^c , cubic

^aCalculated by Robertson (See Ref. 153).
^bMono.=monoclinic.
^cTetrag.=tetragonal.

Wilk, Table I

Id., Table 1. A POSITA would have been motivated to look to Wilk’s teachings to understand the properties of materials discussed in Matsumoto, for example, to ensure the gate insulating film had a sufficiently high dielectric constant. Ex.1101, ¶268. Wilk and Matsumoto are in the same field as the ’764 patent. Ex.1001, 1:15--16; Ex.1009, ¶2; Ex.1018, Abstract; Ex.1101, ¶148.

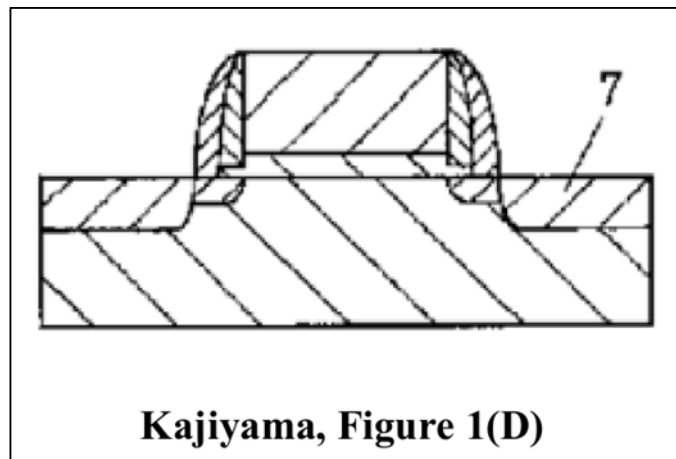
Matsumoto teaches use of “Ta₂O₅” as the gate insulating film. Ex.1009, ¶107. Wilk discloses the dielectric constant for Ta₂O₅ is 26, which is greater than 10. Ex.1018, Table I. Matsumoto discloses second sidewall 9 (“*second insulating sidewall*”) is comprised of silicon nitride (Si₃N₄), which has a dielectric constant of 7. Ex.1009, ¶¶114, 139; Ex.1018, Table I; Ex.1352, Fig. 4.

Thus, in the devices of the Matsumoto-Wilk combination, “*the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more*” (Limitation 18) and “*the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall*” (Limitation 19). Ex.1101, ¶270.

XII. GROUND VIII: Kajiyama Anticipates Claims 1, 5, and 16-17.

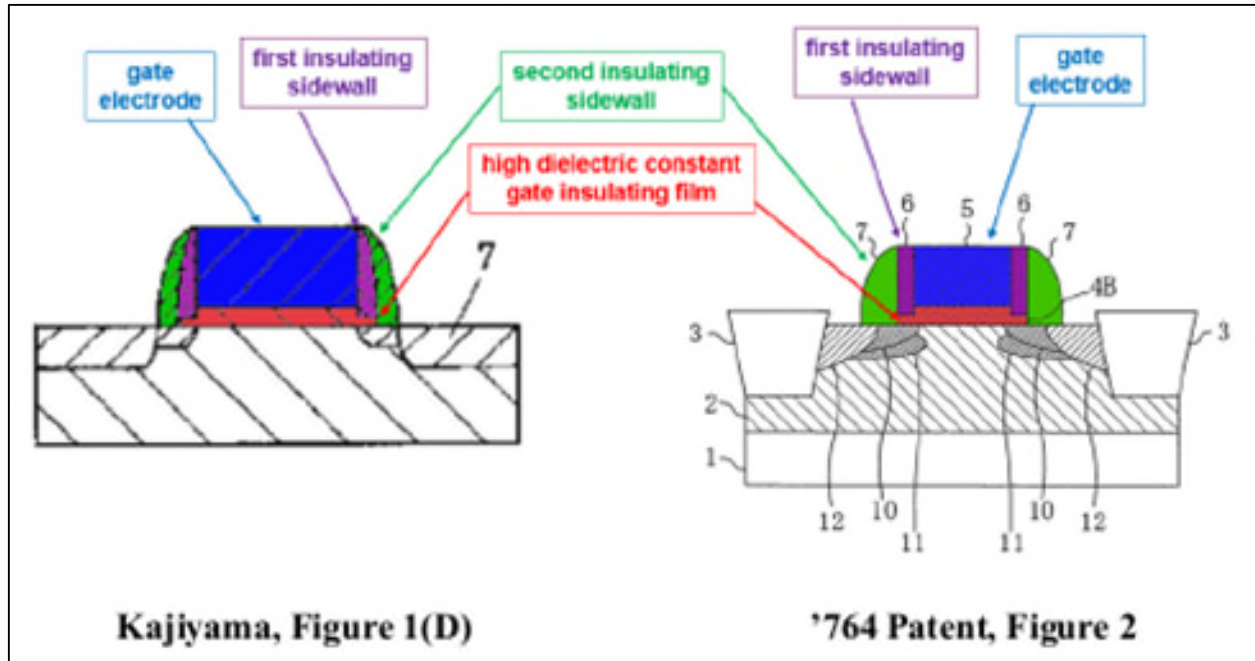
A. Kajiyama

Kajiyama’s first embodiment FET includes a gate electrode with two sidewalls. A high-k gate insulating film extends from under the gate electrode to under only the first sidewall. Ex.1011, ¶¶1, 28, FIG. 1(D) (below).



1. Independent Claim 1

Kajiyama’s first embodiment device anticipates claim 1, as illustrated by the side-by-side figures below. Ex.1011, FIG. 1(D) (below, left); Ex.1011, FIG. 2, (below, right).



a. Preamble

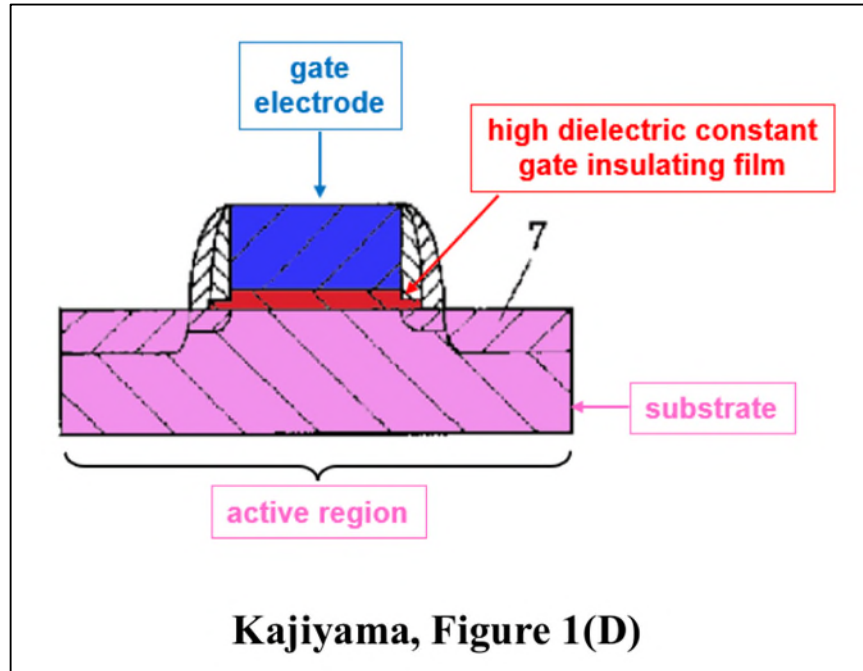
Kajiyama’s first embodiment discloses a “*semiconductor device*”: “[t]he present invention relates to semiconductor devices and manufacturing methods thereof, and in particular to insulating gate type field effect transistors having a gate dielectric film (high dielectric constant material).” Ex.1011, ¶1; *see also* Ex.1011, ¶27; Ex.1101, ¶¶273-74.

b. Limitation 1[a]: “a high dielectric constant gate insulating film formed on an active region in a substrate”

Limitation 1[b]: “a gate electrode formed on the high dielectric constant gate insulating film”

Kajiyama discloses these limitations. Ex.1101, ¶¶275-81. Kajiyama’s device has a “p-type Si **substrate** [shaded pink]” with an “element separation layer (not shown) on the Si substrate 1.” Ex.1011, ¶¶28-29, FIG. 1(D) (below). Kajiyama’s

element separation layer is equivalent to the '764 patent's STI structures. Ex.1011, ¶¶5, 29; Ex.1001, 7:30-47 (showing active region with source/drain regions surrounded by STI structures 3); Ex.1101, ¶276. In Kajiyama, within the region defined by the element separation layer, an n-type LDD diffusion layer 4 is formed and then an n⁺ source drain diffusion layer 7 is formed. Ex.1011, ¶¶29, 32, FIGS. 1(A), 1(D). The region defined by Kajiyama's element separation layer is "*an active region in a substrate.*" Ex.1101, ¶276.



Kajiyama's "device comprises a gate insulating film [labeled 2 in Figure 1(A)] consisting of a high dielectric film¹⁵ [shaded red] formed on a semiconductor substrate." Ex.1011, ¶¶14, 28, claim 1, FIG. 1(D) (above). The high-k film, formed

¹⁵ Kajiyama also refers to high-k film 2 as "ZrO₂ film 2." See, e.g., Ex.1101, ¶277.

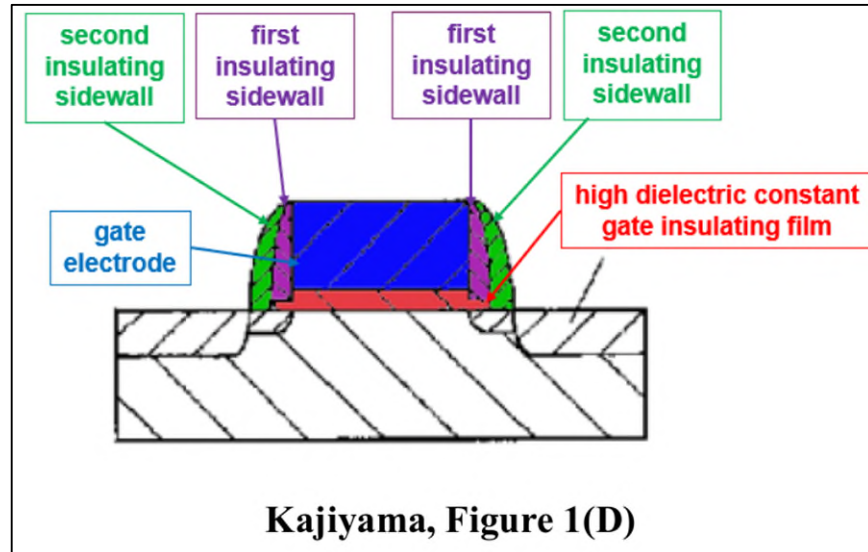
on the substrate within the element separation layer, is therefore the “*high dielectric constant gate insulating film formed on an active region in a substrate*” (Limitation 1[a]). Ex.1011, ¶29; Ex.1101, ¶¶277-78.

Gate electrode 3 (see Ex.1011, FIG. 1(D) (above) (shaded blue)) “consisting of a conductive film [is] formed on [the] gate insulating film.” Ex.1011, ¶14; Ex.1101, ¶280. Kajiyama’s device thus includes “*a gate electrode formed on the high dielectric constant gate insulating film*” (Limitation 1[b]). Ex.1101, ¶¶280-81.

c. Limitation 1[c]: “a first insulating sidewall formed on each side surface of the gate electrode”

Limitation 1[d]: “a second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween

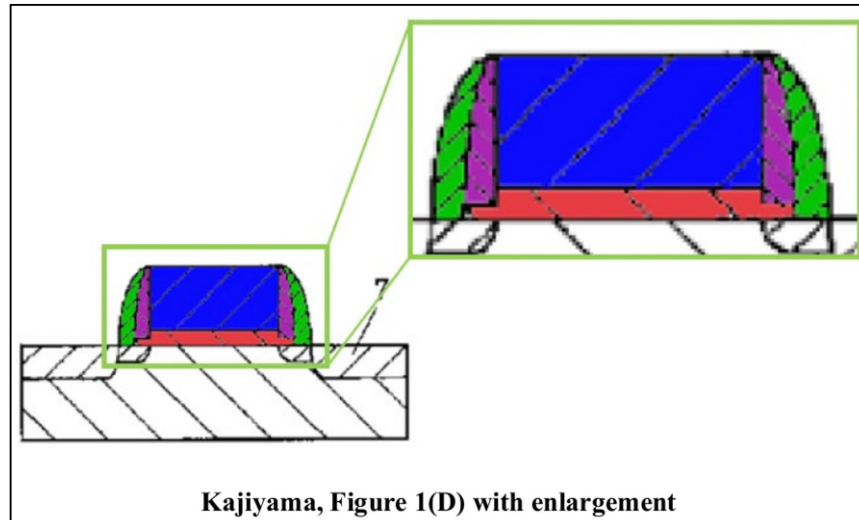
Kajiyama’s device includes “first sidewall [labeled 5 in Figure 1(B), shaded purple below] consisting of a dielectric film formed on a sidewall of the gate electrode, and a second sidewall [labeled 6, shaded green] ... formed to cover the first sidewall.” Ex.1011, ¶¶14, 28, FIG. 1(D) (below). First sidewall 5 “consist[s] of ZrO₂ film (**insulation** film)” and is therefore “*a first insulating sidewall formed on each side surface of the gate electrode*” (Limitation 1[c]). Ex.1011, ¶28; Ex.1101, ¶¶282-84. Second sidewall 6 is a silicon nitride film 6 (referred to as Si₃N₄ film) and is therefore “*a second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween*” (Limitation 1[d]). Ex.1011, ¶28; Ex.1101, ¶¶285-86.



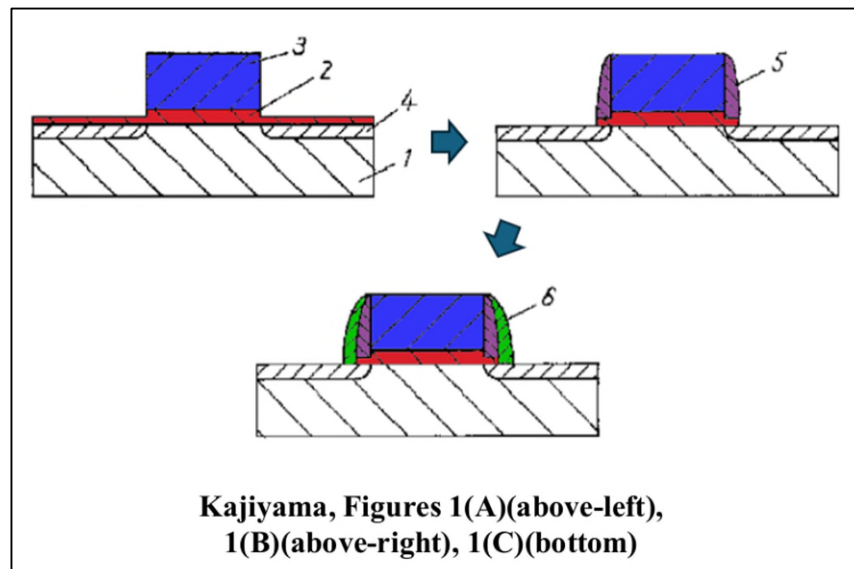
- d. **Limitations 1[e]: “wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall”**

Limitation 1[f]: “part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode”

As shown in Kajiyama’s device and confirmed by the disclosed process, high-k film 2 (see Ex.1011, FIG. 1(D) (below) (shaded red)) is an uninterrupted layer (as evidenced by the absence of gaps) that extends from under the gate electrode to under first sidewall 5 (“*first insulating sidewall*”; see *id.* (shaded purple)). The high-k film is thinner under sidewall 5 (“*first insulating sidewall*”) than it is under the gate electrode (see *id.*, FIG. 1(D) (below) (shaded blue)). Ex.1101, ¶288; See *Unified*, 2022 WL 500391, at *17.



Kajiyama's fabrication process confirms the Figure 1(D) structure. During fabrication, an n-type polySi film is deposited on high-k film 2 and etched "to form a gate electrode 3." Ex.1011, ¶29. High-k film 2 "is also etched to reduce the film." Ex.1011, ¶29, FIG. 1(A) (below, top-left). As a result, the thickness of high dielectric constant film 2 is larger under the gate electrode than elsewhere. Ex.1101, ¶289.



First sidewall 5 (see Ex.1011, FIG. 1(B) (above, top-right) (shaded purple)) is then formed on the side of gate electrode 3 and over the thinner portion of the high-

k film. Ex.1011, ¶30. The high-k film is then etched “to remove all.” Ex.1011, ¶30. That is, the high-k film outside the outer edge of sidewall 5 is removed. Ex.1101, ¶290. Next, second sidewall 6 (*see* Ex.1011, FIG. 1(C) (above, bottom) (shaded green)) is formed “to cover the first sidewall 5 [shaded purple] provided on the sidewall of the gate electrode 3 [shaded blue].” Ex.1011, ¶31. As shown above, a portion of the high-k film (*see id.*, FIGS. 1(A)-(C) (above) (shaded red)) remains under the gate electrode and first sidewall 5 but does not extend under sidewall 6. Ex.1101, ¶291.

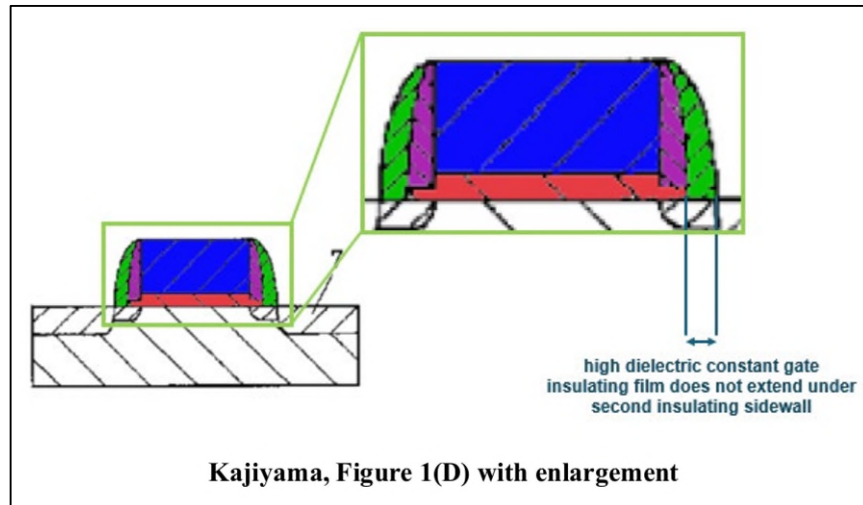
Thus, Kajiyama’s device teaches “*the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall*” (Limitation 1[e]) and “*part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode*” (Limitation 1[f]). Ex.1101, ¶¶291-92.

2. Claim 5

Kajiyama teaches “*the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall*” (Limitation 5). Ex.1101, ¶¶293-95.

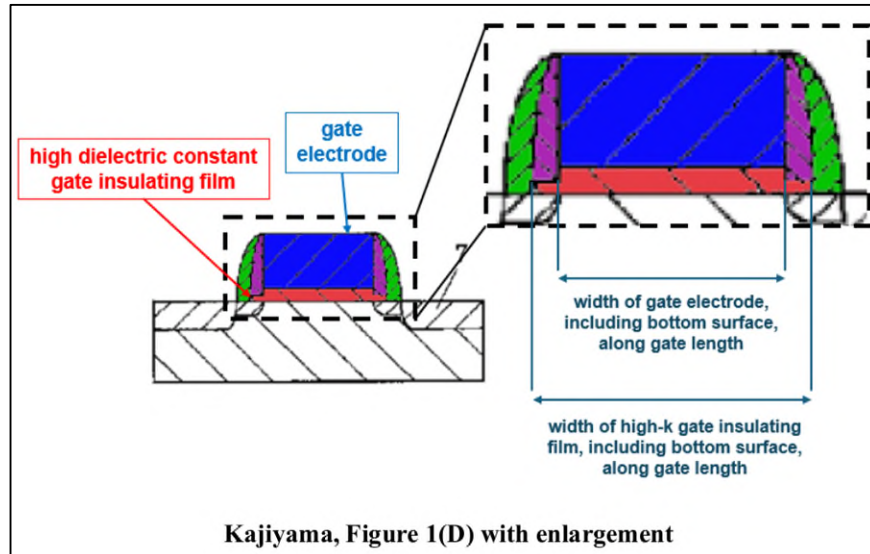
As shown in Figure 1(D) below, high-k dielectric film 2 (*see* Ex.1011, FIG. 1(D) (below) (shaded red)) remains under only the gate electrode 3 and the first

sidewall 5—it is not located under sidewall 6 (“*the second insulating sidewall*”; shaded green). *See Unified*, 2022 WL 500391, at *17. The fabrication process, discussed in §XIII.B.4, confirms the structure illustrated in Figure 1(D). Ex.1011, ¶¶30-31; Ex.1101, ¶¶293-95.



3. Claims 16-17

High-k gate insulating film 2 in Kajiyama’s first embodiment extends from under the gate to under the first insulating sidewall. §XIII.B.4. As illustrated in the Figure 1(D) below, along the gate length, the width of high-k gate insulating film 2 (shaded red), including the bottom surface of high-k gate insulating film 2, is larger than the width of the gate electrode 3 (shaded blue), including the bottom surface of the gate electrode 3. Ex.1101, ¶296. Therefore, Kajiyama anticipates claims 16-17. *Id.*

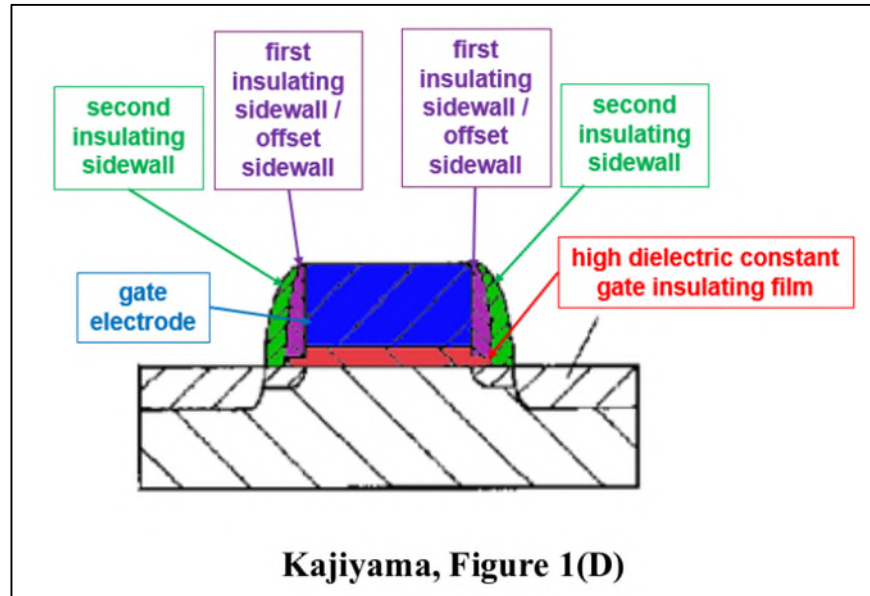


XIII. GROUND IX: Kajiyama Renders Claims 4, 6, and 18-19 Obvious.

A. Claim 4

Kajiyama renders obvious *“the first insulating sidewall is an offset sidewall”* (Limitation 4). Ex.1101, ¶¶298-99.

As discussed in §XIII.B.3, in Kajiyama’s first embodiment, first sidewall 5 is the *“first insulating sidewall.”* While Kajiyama does not refer to first sidewall 5 as an offset sidewall, a POSITA would understand first sidewall 5, located between gate electrode 3 and second sidewall 6, is an offset sidewall. Ex.1101, ¶298; Ex.1334, 216-17, Fig. 5-25; Ex.1011, FIG. 1(D) (below). This is also consistent with the ’764 patent specification, which refers to an inner sidewall as an offset sidewall: “insulating sidewall 7 is formed on each side surface of the gate electrode 5 with an offset sidewall 6 interposed therebetween.” Ex.1001, 7:37-39, FIG. 2.



B. Claim 6

Kajiya renders “the high dielectric constant gate insulating film is formed of a Hf based oxide” (Limitation 6) obvious. Ex.1101, ¶¶300-03.

Kajiya discloses that, while the gate insulating film 2 in the first embodiment is a ZrO_2 film, “other high dielectric films, such as a HfO_2 film, a Ta_2O_5 film, or a Al_2O_3 film, can be used instead to obtain the effects of the invention.” Ex.1011, ¶45. A POSITA would have been motivated to select HfO_2 as the high-k material for Kajiya’s gate dielectric for the reasons discussed in §VI.C. Ex.1101, ¶¶301-03.

C. Claims 18-19

Kajiya renders claims 18-19 obvious. Ex.1101, ¶¶304-08. Kajiya teaches that, in addition to ZrO_2 “other high dielectric films, such as a HfO_2 film, a Ta_2O_5 film, or a Al_2O_3 film, can be used instead to obtain the effects of the invention.”

Ex.1011, ¶45. ZrO_2 has a dielectric constant of 25, HfO_2 has a dielectric constant of 25, and Ta_2O_5 has a dielectric constant of 26, all of which are greater than 10. Ex.1018, Table I. Further, Kajiyama discloses that the second sidewall 6 is comprised of silicon nitride (Si_3N_4), which has a dielectric constant of 7. Ex.1011, ¶28; Ex.1018, Table I.

While Kajiyama itself does not expressly disclose the relative dielectric constants of the listed materials, the dielectric constant is a material property and, therefore, the dielectric constants for ZrO_2 , HfO_2 , Ta_2O_5 , and Si_3N_4 are necessarily present in Kajiyama, a fact that would have been known by a POSITA. Ex.1101, ¶306. Thus, in Kajiyama's device "*the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more*" (Limitation 18) and "*the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall*" (Limitation 19). *Id.*, ¶¶304-08.

XIV. GROUND X: Kajiyama-Wang Combination Renders Claim 11 Obvious.

Should PO argue that Kajiyama does not explicitly disclose a high-k film that "*has a thickness of 2 nm or less*" (Limitation 11), Wang discloses that limitation, and the Kajiyama-Wang combination renders claim 11 obvious. Ex.1101, ¶¶310-14. Wang and Kajiyama are in the same field as the '764 patent. Ex.1001, 1:15-16; Ex.1011, ¶1; Ex.1012, ¶2; Ex.1101, ¶311.

Kajiyama teaches that, while high-k film 2 is discussed as a ZrO_2 film, “**other high dielectric films ... can be used instead.**” Ex.1011, ¶45. Based on this suggestion, a POSITA would have been motivated to investigate different high-k materials and would have been led to Wang, which presents a list of alternatives for its high-k gate dielectric including Hf-based dielectrics (*e.g.*, HfO_2 , HfSiO , HfON , or HfSiON). Ex.1012, ¶¶9, 25; Ex.1101, ¶¶138, 301.

A POSITA would have also been motivated to use HfSiON to enhance operation of Kajiyama’s device because nitrogen incorporation was found to improve thermal stability and electrical characteristics of HfSiON , including by enhancing the dielectric constant of the film. Ex.1329, 849; Ex.1101, ¶223.

Wang further teaches that, for a HfSiON gate insulating layer, the film “was deposited to a thickness of about 5 to 50 Angstroms [0.5 to 5 nm]” with “an equivalent oxide thickness (EOT) of less than about 2.0 nanometers.” Ex.1012, ¶34. Thus, in combination with Kajiyama, the thickness of the HfSiON gate insulating film at its side ends would also range from about less than 0.5 nm to less than 5 nm since the thickness of the layer is smaller under first sidewall 5 than under the gate electrode. Ex.1101, ¶312. The thickness of 2 nm (20 Angstroms) falls within the range of thicknesses disclosed by Wang. *Id.*

The ’764 patent provides no discussion, evidence, or motivation associated with the selection of 2 nm for the gate insulating film. Ex.1101, ¶313. Thus, the

Kajiyama-Wang combination renders obvious that “*each side end portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less*” (Limitation 11). *See Ormco Corp.*, 463 F.3d at 1311 (“Where a claimed range overlaps with a range disclosed in the prior art, there is a presumption of obviousness.”); *E.I. DuPont de Nemours*, 904 F.3d at 1008.

XV. GROUND XI: Kajiyama-Sim Combination Renders Claim 11 Obvious.

Should an argument be made the Kajiyama-Wang combination does not render claim 11 obvious, Sim discloses the limitations of claim 11. §VII; Ex.1101, ¶¶315-21. Sim and Kajiyama are in the same field as the ’764 patent. Ex.1001, 1:15-16; Ex.1011, ¶1; Ex.1024, Abstract; Ex.1101, ¶316.

As noted above, Sim concluded that “[s]caling the physical thickness of the HfO₂ dielectric to below 20Å [2 nm] causes less charge trapping and higher mobility.” Ex.1024, 221. Kajiyama discloses use of HfO₂ as a high-k gate dielectric (see Ex.1011, ¶45), the same film studied in Sim. A POSITA would have been motivated to apply Sim’s teachings in Kajiyama’s first embodiment device to form a HfO₂ gate insulating film with a thickness of 20Å (2 nm) or less. Ex.1101, ¶319.

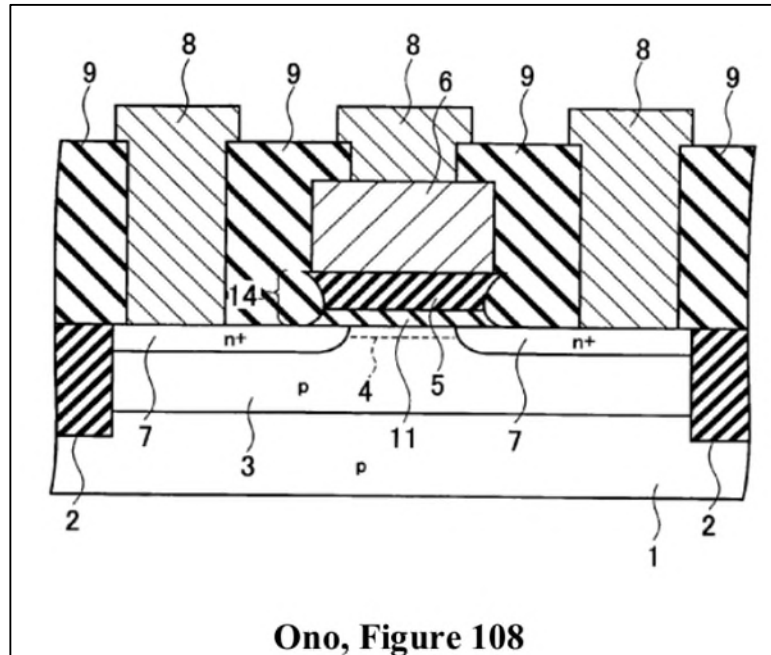
A POSITA would have been motivated to make the above combination for the reasons discussed in §VII and to improve the performance of Kajiyama’s device. Ex.1101, ¶320. The combination is nothing more than use of a known technique (Sim’s HfO₂ dielectric layer with less than 20Å thickness) to improve similar devices

in the same way for the above reasons. *KSR*, 550 U.S. at 416-17; Ex.1101, ¶320. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable because Sim uses a well-known process for fabricating high-k films. Ex.1024, 218; §VII; Ex.1101, ¶320.

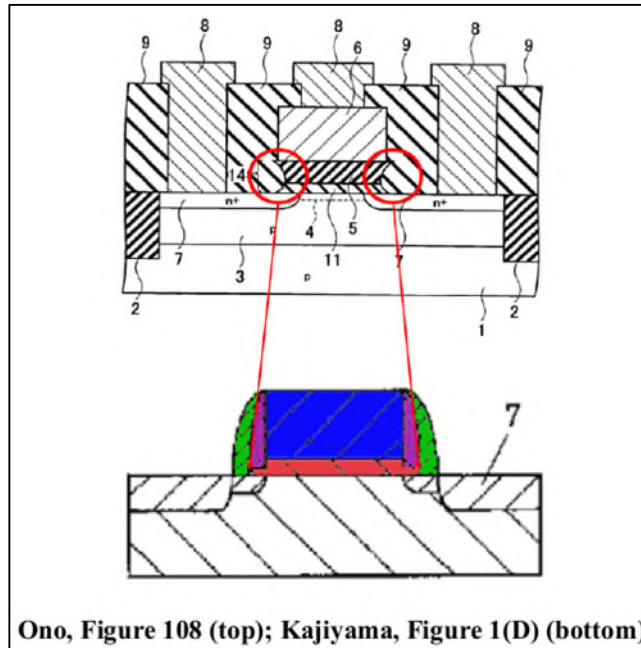
XVI. GROUND XII: Kajiyama-Ono Combination Renders Claims 12 and 13 obvious.

Should PO argue that Kajiyama does not expressly disclose the high-k gate insulating film's side surface "*is located at a predetermined distance from a side end surface of the first insulating sidewall toward the gate electrode*" (Limitation 12) or "*is located at a predetermined distance from a side end surface of the gate electrode toward the first insulating sidewall*" (Limitation 13), Ono teaches these limitations, and the Kajiyama-Ono combination renders obvious claims 12 and 13. Ex.1101, ¶¶322-30. Ono and Kajiyama are in the same field as the '764 patent. Ex.1001, 1:15-16; Ex.1011, ¶1; Ex.1013, ¶¶3-7; Ex.1101, ¶323.

Ono discloses that "the sidewalls of the gate insulator film may curve" as shown, *e.g.*, in Figure 108 (below). Ex.1013, ¶216.



A POSITA would have been motivated to apply Ono's teaching of curving the end portions of a gate insulating film (see Ex.1013, FIG. 108 (below, top) (shaded red)) to Kajiyama's high-k dielectric in the first embodiment (see Ex.1012, FIG. 1(D) (below, bottom)), as illustrated below. Ex.1101, ¶324. Thus, in the combination, the side ends of Kajiyama's gate insulating film have a semicircular shape, as taught by Ono.

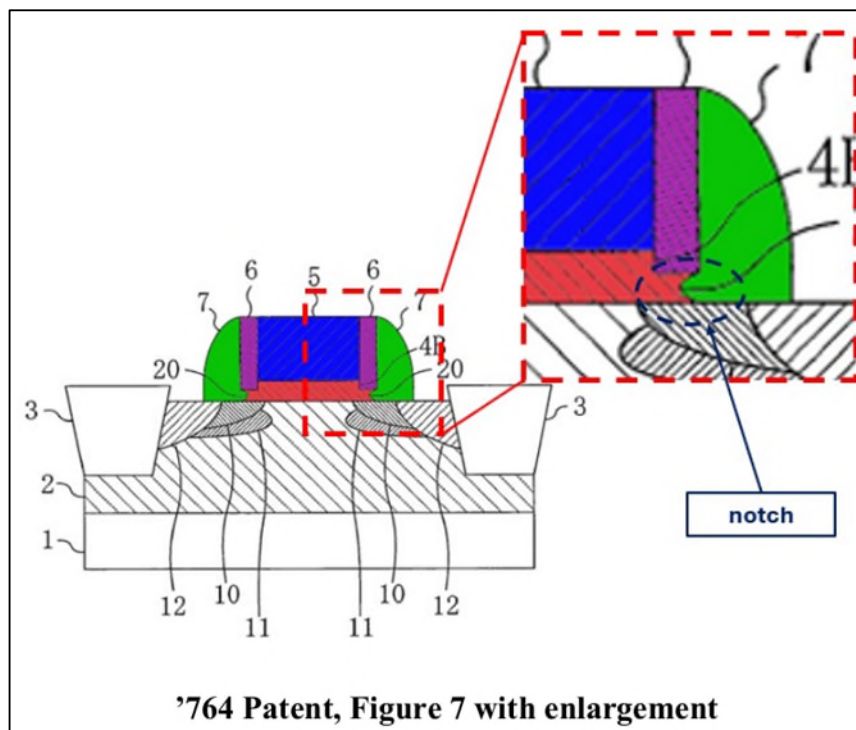


A POSITA would have been motivated to make the above combination because Ono expressly suggests the combination, as discussed in §IX.B, and to improve performance of Kajiyama's first embodiment device by optimizing the electrical capacitance between the gate electrode and the source/drain regions. Ex.1013, ¶¶200, 216; Ex.1101, ¶325.

The Kajiyama-Ono combination is nothing more than the use of a known technique (Ono's use of curved side surfaces for a gate insulating film) to improve similar devices in the same way for the above reasons. *KSR*, 550 U.S. at 416-17; Ex.1101, ¶326. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable. *Id.* Kajiyama and Ono both use high-k gate insulating films that extend under the gate electrode and the insulating sidewall, a concept well-known before the '764 patent.

§§IV.B.2.b, IV.D.2, XIII.B.4, IX.A. And both form their high-k dielectrics using conventional techniques. Ex.1011, ¶29; Ex.1013, ¶167; Ex.1101, ¶327.

In the device of the Kajiyama-Ono combination, the end portion of Kajiyama's gate insulating film has a semicircular shape, as taught by Ono. The Kajiyama-Ono combination therefore discloses a device where the high dielectric constant gate insulating film includes a notch at a side end portion, consistent with the disclosure of the '764 patent. *See, e.g.*, Ex.1001, 8:35-40 (referring to notch 20 of FIG. 7), FIG. 7 (depicting notch 20 having a semicircular shape); Ex.1101, ¶327.



Additionally, in the Kajiyama-Ono combination, when the notch is applied at each side end of Kajiyama's gate insulating film 2 located under the first sidewall 5, the end of the gate insulating film no longer extends completely under the first insulating

sidewall. Ex.1101, ¶328. Further, as discussed in §IX.C, the notch's semicircular shape and the distance which the semicircular shape extends inward toward the gate electrode are set by specific process parameters. *Id.*, ¶328.

Accordingly, in the Kajiyama-Ono combination, the gate insulating film's side surface is “*located at a predetermined distance from a side end surface of the first insulating sidewall toward the gate electrode*” (Limitation 12) and “*located at a predetermined distance from a side end surface of the gate electrode toward the first insulating sidewall*” (Limitation 13), consistent with the disclosure of the '764 patent. Ex.1001, 21:26-30 (“side surface ... may be located at a predetermined distance from a side end surface of the sidewall 7 or the offset sidewall 6 toward the gate electrode 5”); Ex.1101, ¶¶329-30.

XVII. GROUND XIII: Kajiyama-Bu Combination Renders Claims 14-15 Obvious.

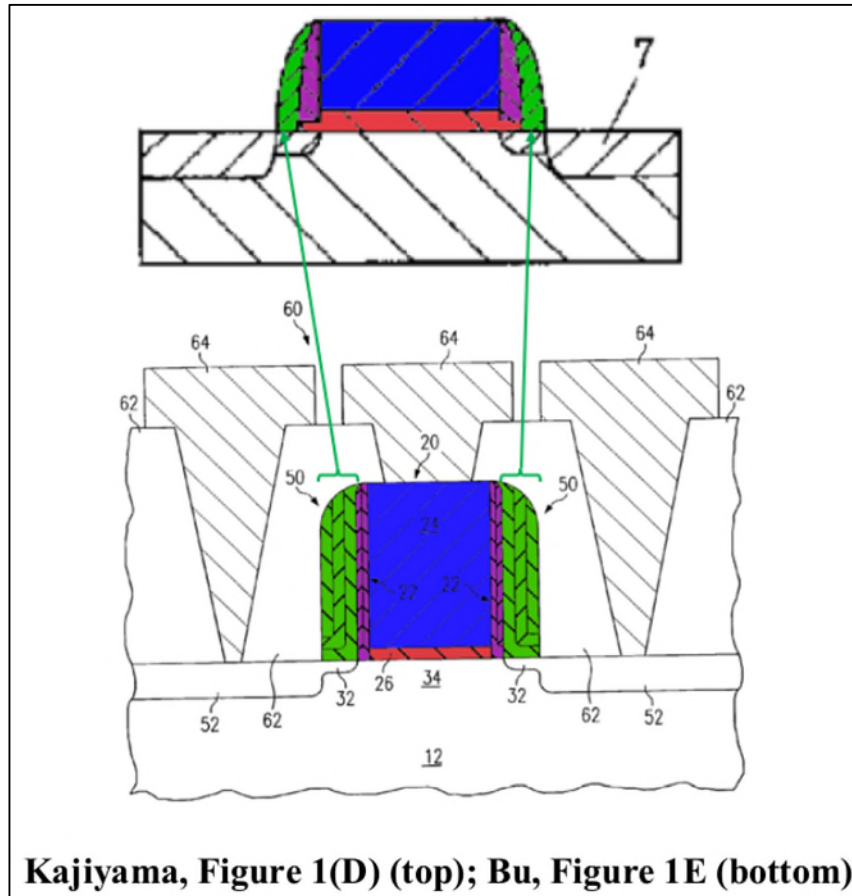
The Kajiyama-Bu combination discloses an outer sidewall with “*a double layer structure*” (Limitation 14) and “*a triple layer structure*” (Limitation 15). Ex.1101, ¶¶331-37.

Bu teaches an outer sidewall structure having three layers. Ex.1025, ¶¶26, 42-43; §XI. Bu's sidewall structure includes a first sidewall-forming layer 40 comprising an oxide, a second sidewall-forming layer 42 comprising a nitride, and a third sidewall-forming layer 44 comprising an oxide. Ex.1025, ¶¶27, 30, 35. Bu

and Kajiyama are in the same field as the '764 patent. Ex.1001, 1:1516; Ex.1011, ¶1; Ex.1025, Abstract; Ex.1101, ¶332.

A. Triple Layer-Claim 15

In Kajiyama's first embodiment, the second sidewall 6 is a silicon nitride film ("*a nitride film*"). §XIII.B.3; Ex.1011, ¶28; Ex.1101, ¶332. A POSITA would have been motivated to use Bu's triple-layer ONO sidewall structure with Kajiyama's first embodiment device. Specifically, a POSITA would have been motivated to form Kajiyama's second sidewall 6 (*see* Ex.1012, FIG. 1(D) (below, top) (shaded green)) with two additional silicon oxide layers to create a triple-layer ONO sidewall structure, as taught by Bu. Ex.1101, ¶333; *see* Ex.1025, FIG. 1E (below, bottom). The resulting device discloses that "*the second insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film*" (Limitation 15). Ex.1101, ¶333.



A POSITA would have been motivated to combine Bu’s teaching of a triple-layer ONO sidewall structure with Kajiyama in light of the known benefits of ONO structures. §XI; Ex.1101, ¶334. For example, Bu teaches that “the film properties of sidewall-forming layers 40 and 42 may minimize dopant loss from source drain extension region 32 to first sidewall-forming layer 40,” thereby lowering parasitic resistance. Ex.1025, ¶26.

The combination is nothing more than the use of a known technique (Bu’s triple-layer sidewall) to improve similar devices in the same way. *KSR*, 550 U.S. at 416-17; Ex.1101, ¶335. Finally, Kajiyama and Bu disclose forming sidewall layers

using standard deposition and etching techniques (Ex.1011, ¶¶30-31; Ex.1025, ¶¶27, 30, 35, 38), making the application of Bu’s multiple-layer structure to Kajiyama’s device straightforward. Accordingly, a POSITA would have had a reasonable expectation of success in the combining Kajiyama and Bu, leading to predictable results. Ex.1101, ¶337.

B. Double Layer-Claim 14

A POSITA would also have been motivated by Bu’s teachings to form Kajiyama’s second sidewall 6 (formed of nitride) with a single additional silicon oxide layer to create a double-layer sidewall structure, resulting in a device where “*the second insulating sidewall has a double layer structure including an oxide film and a nitride film*” (Limitation 14). Ex.1101, ¶336. As discussed previously, Bu teaches that the film properties of additional layers may minimize dopant loss and lower parasitic resistance. Ex.1025, ¶26. Additionally, where design requirements dictate reducing manufacturing complexity, a POSITA would have known to use fewer (*i.e.*, two) layers to similarly achieve the benefits taught by Bu. Ex.1101, ¶336. In light of these considerations, a POSITA would have been motivated to implement Bu’s teachings into Kajiyama’s device to form a double-layer sidewall structure. *Id.*

For the same reasons discussed above, the combination of Kajiyama and Bu to include a double-layer sidewall structure is nothing more than the use of a known technique to improve similar devices in the same way, and a POSITA would have

had a reasonable expectation of success in the combining these references, leading to predictable results. *KSR*, 550 U.S. at 416-17; Ex.1101, ¶337.

XVIII. GROUND XIV: Kajiyama-Wilk Combination Renders Claims 18-19 Obvious.

Should PO argue that Kajiyama does not disclose claims 18-19, Wilk expressly teaches these limitations. Wilk and Kajiyama are in the same field as the '764 patent. Ex.1001, 1:15-16; Ex.1011, ¶1; Ex.1018, Abstract; Ex.1101, ¶¶338-45.

As noted in §XII, Wilk discloses the following table for various high- κ materials:

TABLE I. Comparison of relevant properties for high- κ candidates.				
Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si	Crystal structure(s)
SiO ₂	3.9	8.9	3.2	Amorphous
Si ₃ N ₄	7	5.1	2	Amorphous
Al ₂ O ₃	9	8.7	2.8 ^a	Amorphous
Y ₂ O ₃	15	5.6	2.3 ^a	Cubic
La ₂ O ₃	30	4.3	2.3 ^a	Hexagonal, cubic
Ta ₂ O ₅	26	4.5	1–1.5	Orthorhombic
TiO ₂	80	3.5	1.2	Tetrag. ^c (rutile, anatase)
HfO ₂	25	5.7	1.5 ^a	Mono. ^b , tetrag. ^c , cubic
ZrO ₂	25	7.8	1.4 ^a	Mono. ^b , tetrag. ^c , cubic

^aCalculated by Robertson (See Ref. 153).
^bMono.=monoclinic.
^cTetrag.=tetragonal.

Wilk, Table I

Ex.1018, Table 1. A POSITA would have been motivated to look to Wilk's teachings to understand the properties of materials discussed in Kajiyama, for example, to ensure that the gate insulating film had a sufficiently high dielectric constant. Ex.1101, ¶342.

Kajiyama teaches that, in addition to ZrO_2 , “other high dielectric films, such as a HfO_2 film, a Ta_2O_5 film, or a Al_2O_3 film, can be used instead to obtain the effects of the invention.” Ex.1011, ¶45. ZrO_2 has a dielectric constant of 25, HfO_2 has a dielectric constant of 25, Ta_2O_5 has a dielectric constant of 26, all of which are greater than 10. Ex.1018, Table I. Further, Kajiyama discloses that the second sidewall 6 is comprised of silicon nitride (Si_3N_4), which has a dielectric constant of 7. Ex.1011, ¶28; Ex.1018, Table I. The combination of Kajiyama and Wilk therefore renders obvious claims 18-19. Ex.1101, ¶345.

XIX. Mandatory Notices

A. Real Party in Interest (37 C.F.R. §42.8(b)(1))

The Petitioner and real parties-in-interest are United Microelectronics Corporation and UMC Group (USA).

B. Related Matters (37 C.F.R. §42.8(b)(2))

To the best of Petitioner’s knowledge, the ’764 patent is subject of the following active proceedings:

- *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation*, Civil Action No. 2:24-cv-00730 in the Eastern District of Texas (Lead Case), filed September 6, 2024;
- *Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Manufacturing Company Limited*, Civil Action No. 2:24-cv-00623 in the

Eastern District of Texas (Consolidated Member Case), filed August 1, 2024; and

- *Taiwan Semiconductor Manufacturing Company, Ltd. v. Advanced Integrated Circuit Process LLC*, IPR2025-00829 in the U.S. Patent and Trademark Office, Patent Trial and Appeal Board, filed April 15, 2025.

C. Lead and Back-up Counsel (37 C.F.R. §42.8(b)(3))

Pursuant to 37 C.F.R. §§42.8(b)(3) and 42.10(a), Petitioner appoints the following lead and back-up counsel:

Lead Counsel	Back Up Counsel
Tim Tingkang Xia (No. 45,242) Tim.Xia@troutman.com TROUTMAN PEPPER LOCKE LLP 600 Peachtree Street, NE, Suite 3000 Atlanta, GA 30308 Telephone: (404) 870-4698	Emma A. Bennett (No. 80,631) Emma.Bennett@troutman.com TROUTMAN PEPPER LOCKE LLP 600 Travis Street, Suite 2800 Houston, TX 77002 Telephone: (713) 226-1549

D. Service Information (37 C.F.R. §42.8(b)(4))

Service information is provided in the designation of counsel above. Petitioner consents to electronic service by email to Tim.Xia@troutman.com and Emma.Bennett@troutman.com.

E. Payment of Fees (37 C.F.R. §42.103)

The Office is authorized to charge the fee set forth in 37 C.F.R. §42.15(a)(1) for this Petition to Deposit Account No. DA201507. Review of fifteen claims is

Petition for *Inter Partes* Review of U.S. Patent No. 7,923,764

requested. The undersigned further authorizes payment for any additional fees that may be due in connection with this Petition.

XX. Conclusion

For the reasons set forth above, *Inter Partes* Review of the Challenged Claims of the '764 patent is respectfully requested.

Respectfully submitted,

Date: June 2, 2025

/s/ Tim Tingkang Xia

Tim Tingkang Xia (Lead Counsel)

Registration No. 45,242

Counsel for Petitioner

CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), I certify that this Petition complies with the type-volume limits of 37 C.F.R. §42.24(a)(1)(i) because it contains 12,745 words, according to the word-processing system used to prepare this Petition, excluding the parts of this Petition that are exempted by 37 C.F.R. §42.24(a)(1) (table of contents, table of authorities, mandatory notices under §42.8, certificate of service, certificate of word count, or appendix of exhibits or claim listing).

Date: June 2, 2025

/s/ Tim Tingkang Xia
Tim Tingkang Xia (Lead Counsel)
Registration No. 45,242
Counsel for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §42.6(e), this is to certify that on this 2nd day of June, 2025, I caused to be served on a USB flash drive a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,923,764 Under 35 U.S.C. §§311, 312 and 37 C.F.R. §42.104 (with Exs. 1001-1002, 1009-1013, 1018-1019, 1024-1025, 1101-1112, 1211, 1213, 1216, 1223, 1226-1227, 1229, 1305, 1323, 1326, 1329, 1333-1334, 1337-1338, 1340-1341, 1349-1350, 1352, 1406, 1413, 1419, 1429-1435, 1506, 1512, 1515-1529, 1531-1532) via Federal Express Priority Overnight at the Correspondence Address for Patent Owner:

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Courtesy copies have been concurrently served via email on Patent Owner's litigation counsel at:

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/s/ Tim Tingkang Xia
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Counsel for Petitioner

APPENDIX: CHALLENGED CLAIMS LISTING

1. **Preamble:** A semiconductor device comprising:

Limitation 1[a]: a high dielectric constant gate insulating film formed on an active region in a substrate;

Limitation 1[b]: a gate electrode formed on the high dielectric constant gate insulating film;

Limitation 1[c]: a first insulating sidewall formed on each side surface of the gate electrode; and

Limitation 1[d]: a second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween,

Limitation 1[e]: wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, and

Limitation 1[f]: part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.
2. **Limitation 2:** The semiconductor device of claim 1, further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film.

3. **Limitation 3:** The semiconductor device of claim 2, wherein the buffer insulating film is a silicon oxide film.
4. **Limitation 4:** The semiconductor device of claim 1, wherein the first insulating sidewall is an offset sidewall.
5. **Limitation 5:** The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall.
6. **Limitation 6:** The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a Hf based oxide.
11. **Limitation 11:** The semiconductor device of claim 1, wherein each side end portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less.
12. **Limitation 12:** The semiconductor device of claim 1, wherein a side surface of the high dielectric constant gate insulating film is located at a predetermined distance from a side end surface of the first insulating sidewall toward the gate electrode.
13. **Limitation 13:** The semiconductor device of claim 1, wherein a side surface of the high dielectric constant gate insulating film is located at a predetermined distance from a side end surface of the gate electrode toward the first insulating sidewall.

14. **Limitation 14:** The semiconductor device of claim 1, wherein the second insulating sidewall has a double layer structure including an oxide film and a nitride film.
15. **Limitation 15:** The semiconductor device of claim 1, wherein the second insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film.
16. **Limitation 16:** The semiconductor device of claim 1, wherein a width of the high dielectric constant gate insulating film along a gate length is larger than a width of the gate electrode along the gate length.
17. **Limitation 17:** The semiconductor device of claim 1, wherein a width of a bottom surface of the high dielectric constant gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length.
18. **Limitation 18:** The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more.
19. **Limitation 19:** The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall.