

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

Petitioner,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,

Patent Owner.

IPR2025-00829

U.S. Patent 7,923,764

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT 7,923,764**

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EXHIBIT LIST

Exhibit	Description
1001	U.S. Patent 7,923,764 to Hirase, et al. (“the ’764 patent”)
1002	File History of U.S. Patent 7,923,764 (“’764 File History”)
1003	Declaration of Dr. Jack Lee in Support of IPR Petition
1004	CV of Dr. Jack Lee
1005	Translated Excerpts from JP File History
1006	U.S. Patent 7,579,227 to Hirase, et al. (“the ’227 patent”)
1007	Reserved
1008	Reserved
1009	U.S. Publication 2003/0025135 to Matsumoto, et al. (“Matsumoto”)
1010	JP2003-258241 to Kajiyama (“JP-Kajiyama”)
1011	Certified Translation of JP2003-258241 to Kajiyama (“Kajiyama”)
1012	U.S. Publication 2006/0131672 to Wang, et al. (“Wang”)
1013	U.S. Publication 2005/0051856 to Ono, et al. (“Ono”)
1014	Reserved
1015	Reserved
1016	Reserved
1017	Reserved
1018	Wilk, G. D., et al., “High-k gate dielectrics: Current status and materials properties considerations,” Journal of Applied Physics, Vol. 89, No. 10, pp. 5243-5275, May 15, 2001 (“Wilk”)

Exhibit	Description
1019	U.S. Publication 2005/0045938 to Mutou, et al. (“Mutou”)
1020	Reserved
1021	Reserved
1022	Reserved
1023	U.S. Patent 6,306,712 to Rodder, et al. (“Rodder”)
1024	Sim, J. H., et al., “Effects of ALD HfO ₂ thickness on charge trapping and mobility,” Microelectronic Engineering, Vol. 80, pp. 218-221, June 17, 2005 (“Sim”)
1025	U.S. Publication 2004/0110352 to Bu, et al. (“Bu”)
1026	Declaration of June Ann Munford
1027	Reserved
1028	Reserved
1029	Koyama, M., et al., “Effects of Nitrogen in HfSiON Gate Dielectric on the Electrical and Thermal Characteristics,” Digest of International Electron Devices Meeting, pp. 849-852, Dec. 8-11, 2002 (“Koyama”)
1030	Reserved
1031	Reserved
1032	Houssa, M., “High-κ Gate Dielectrics” (CRC Press 1st Ed. 2003) (“Houssa”)
1033	Plummer, J., et al., “Silicon VLSI Technology: Fundamentals, Practice and Modeling” (Prentice Hall 2000) (“Plummer”)
1034	Wolf, S., “Silicon Processing for the VLSI Era, Volume 4 – Deep-Submicron Process Technology” (Lattice 2002) (“Wolf”)

Exhibit	Description
1035	Reserved
1036	Reserved
1037	Lee, S. J., et al. “High Quality Ultra Thin CVD HfO ₂ Gate Stack with Poly-Si Gate Electrode,” Digest of International Electron Devices Meeting, pp. 31-34, Dec. 10-13, 2000 (“Lee”)
1038	Campbell, “The Science and Engineering of Microelectronic Fabrication”, Second Edition (2001) (“Campbell”)
1039	Reserved
1040	JP2005-064190 to Ono with certified translation (“JP-Ono”)
1041	N. Weste and D. Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, Third Edition (Pearson/Addison Wesley, 2005) (“Weste”)
1042	Reserved
1043	Reserved
1044	Reserved
1045	Reserved
1046	Reserved
1047	Reserved
1048	Reserved
1049	Lee, B.H., et al., “Ultrathin Hafnium Oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application,” Digest of International Electron Devices Meeting, pp. 133-36, Dec. 5-8, 1999 (“Lee-1999”)
1050	U.S. Publication 2005/0040479 to Koldiaev, et al. (“Koldiaev”)

Exhibit	Description
1051	U.S. Publication 2005/0139932 to Cho, et al. (“Cho”)
1052	Albertin, K.F., et al., “Study of PECVD SiO _x N _y films dielectric properties with different nitrogen concentration utilizing MOS capacitors,” Microelectronic Engineering, Vol. 77, pp. 144-49 (2005)

I. Introduction

Taiwan Semiconductor Manufacturing Company Ltd. (“Petitioner”) petitions for *inter partes* review of claims 1-21 of U.S. Patent 7,923,764 (“the ’764 patent”; TSMC-1001).

The ’764 patent relates “to techniques for improving the driving power and reliability of a MISFET [metal insulator semiconductor field-effect transistor]” by (1) extending a high-k gate insulating film from under the gate electrode to under a sidewall and (2) making the high-k film thicker under the gate electrode than under the sidewall. (TSMC-1001, 1:15-21, 2:6-15, 2:37-44.) These concepts were known before the ’764 patent, a fact corroborated by the Examiner and acquiesced to by the Applicant during Japanese prosecution.

Petitioner demonstrates the challenged claims are unpatentable.

II. Grounds for Standing

Petitioner certifies the ’764 patent is available for IPR and it is not barred or estopped from requesting IPR on the grounds herein.

III. Identification of Challenge

A. Prior Art

The ’764 patent was filed on July 20, 2009 as a divisional of U.S. Patent 7,579,227 (“the ’227 patent”) which claims priority to JP2005-227457 (“JP application”), filed August 5, 2005. Petitioner does not acquiesce the ’764 patent is

entitled to priority of the JP application. Regardless, each applied reference was filed or published before August 5, 2005.

1. **U.S. Publication 2003/0025135 to Matsumoto, et al.** (“Matsumoto”; TSMC-1009), published February 6, 2003, is prior art under 35 U.S.C. §102(b).¹
2. **JP2003-258241 to Kajiyama** (“JP-Kajiyama”; TSMC-1010), published September 12, 2003, is prior art under §102(b). A certified translation of JP-Kajiyama (“Kajiyama”) is provided as TSMC-1011.
3. **U.S. Publication 2006/0131672 to Wang, et al.** (“Wang”; TSMC-1012), filed April 27, 2005, is prior art under §102(e).
4. **U.S. Publication 2005/0045938 to Mutou, et al.** (“Mutou”; TSMC-1019), published March 3, 2005, is prior art under §102(b).
5. **U.S. Publication 2005/0051856 to Ono, et al.** (“Ono”; TSMC-1013), published March 10, 2005, is prior art under §102(b).
6. **U.S. Patent 6,306,712 to Rodder, et al.** (“Rodder”; TSMC-1023), issued October 23, 2001, is prior art under §102(b).

¹ Pre-AIA 35 U.S.C. §102 applies.

7. **“Effects of ALD HfO₂ thickness on charge trapping and mobility”**
to **Sim, et al.** (“Sim”; TSMC-1024), published June 17, 2005, is prior art under §102(b). (TSMC-1026, ¶¶18-21.)
8. **U.S. Publication 2004/0110352 to Bu, et al.** (“Bu”; TSMC-1025), published June 10, 2004, is prior art under §102(b).
9. **“High-k gate dielectrics: Current status and materials properties considerations” to Wilk, et al.** (“Wilk”; TSMC-1018), published in 2001, is prior art under §102(b). (TSMC-1026, ¶¶14-17.)

B. Grounds for Challenge

Ground		Claims	Prior Art
1	103	1, 4-5, 14-21	Matsumoto
2	103	2-3, 6-7, 11	Matsumoto-Wang
3	103	11	Matsumoto-Wang-Sim
4	103	2-3	Matsumoto-Mutou
5	103	6, 10, 12, 13	Matsumoto-Ono
6	103	8-9	Matsumoto-Rodder
7	103	15	Matsumoto-Bu
8	103	18-19	Matsumoto-Wilk
9	102	1, 5, 16-17, 21	Kajiyama
10	103	4, 6, 18-20	Kajiyama
11	103	7, 11	Kajiyama-Wang

Ground		Claims	Prior Art
12	103	11	Kajiyama-Sim
13	103	8-9	Kajiyama-Rodder
14	103	10, 12, 13	Kajiyama-Ono
15	103	14-15	Kajiyama-Bu
16	103	18-19	Kajiyama-Wilk

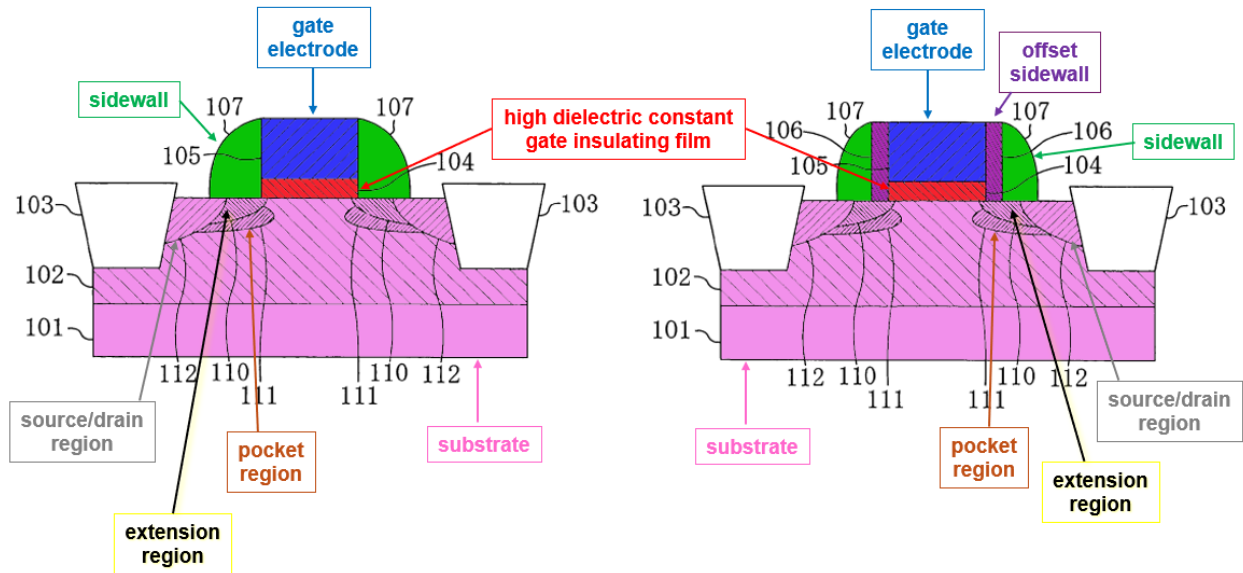
IV. The '764 Patent

A. Applicant Admitted Prior Art (“AAPA”)

The '764 patent recognized that, prior to August 2005, semiconductor devices had used “a high dielectric constant film formed of a Hf based oxide, Al based oxide or the like” as a gate insulating film. (TSMC-1001, 1:23-31.) It describes two exemplary prior art metal insulator semiconductor field-effect transistors (MISFETs), depicted in Figures 16A-16B, each including a high dielectric constant gate insulating film² 104 (shaded red) interposed between gate electrode 105 (shaded blue) and the substrate. In the Figure 16A device, an insulating sidewall 107 (shaded green) is formed on each side of gate electrode 105. (TSMC-1001, 1:43-44.) In the Figure 16B device, an additional insulating

² The term “high dielectric constant” is also referred to as “high-k” in this Petition and prior art documents.

offset sidewall 106 (shaded purple) is interposed between sidewall 107 and gate electrode 105. (TSMC-1001, 1:52-55.)



'764 Patent, Figure³ 16A

'764 Patent, Figure 16B

In these devices, the “side end portions” of the high-k film “are in direct contact with sidewalls.” (TSMC-1001, 1:61-64.) The '764 patent purports to address issues with this arrangement by extending the high-k film under the “sidewalls to prevent end portions of the [high-k] film from being in contact with the sidewalls.” (TSMC-1001, 2:10-16.) It also purports to make the high-k film thicker under the gate than under the sidewalls. (TSMC-1001, 2:37-44.)

These basic concepts were well-known. (*E.g.*, §§IV.B.2, IV.D.2, V, XIII.)

³ All shading and annotations in figures added, unless otherwise noted.

B. Technical Background

A semiconductor device, at its most basic, exploits the properties of semiconductor materials such as silicon. Many types of semiconductor devices exist including, e.g., diodes and MOS transistors (e.g., field effect transistors (FETs)). (E.g., TSMC-1033, 33-41.) For ease of discussion, Petitioner describes FET devices in further detail below.

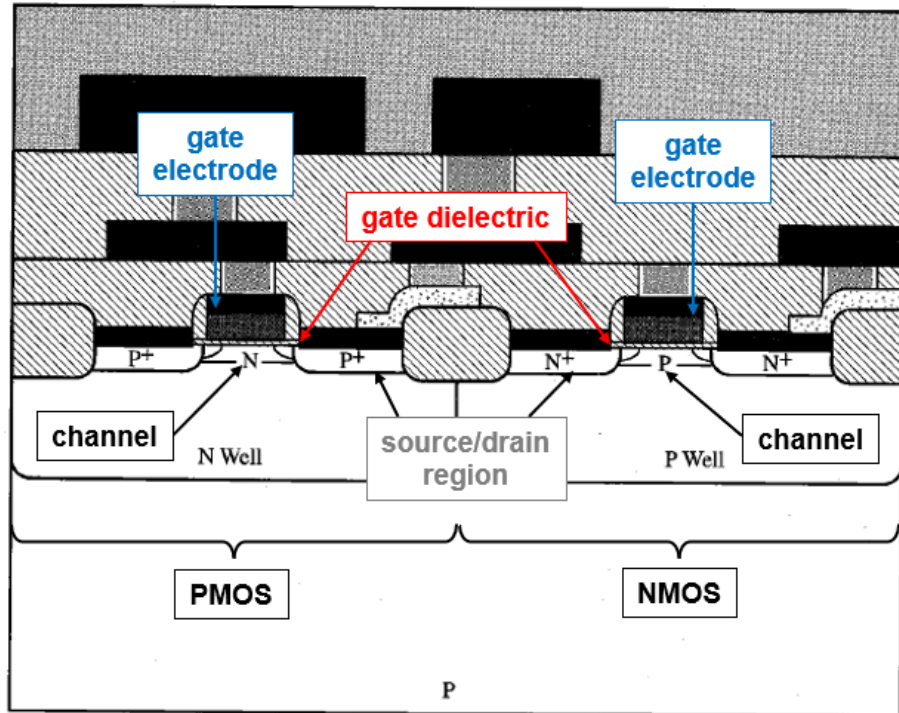
1. MISFET/MOSFET

MISFETs⁴ have a **source/drain** for current input/output. (TSMC-1003, ¶36; TSMC-1033, 76-82.) MISFETs like the ones at issue here also have a **gate** above a **channel** region between the source and drain. (TSMC-1003, ¶36; TSMC-1033, 71-76.) The **gate** includes a **gate electrode** and **gate dielectric** (also referred to as a gate insulating film) separating the gate electrode from the channel region. (TSMC-1003, ¶36; TSMC-1033, 71-76.) Applying voltage to the gate electrode controls the channel region to connect (ON state) or disconnect (OFF state) the source and drain. (TSMC-1003, ¶37; TSMC-1041, 8-9.) Generally, source/drain regions are **doped** with either a **p-type** or **n-type** impurity. (TSMC-1003, ¶38; TSMC-1033, 76-82.) MISFETs with n-type source/drain regions are called

⁴ The terms “MISFET” and “MOSFET” (“Metal-**Oxide**-Semiconductor Field-Effect Transistor”) are interchangeable. (TSMC-1003, ¶34.)

NMOS, and MISFETs with p-type source/drain regions are called **PMOS**.

(TSMC-1003, ¶44; TSMC-1033, 13, Figure 1-11.)



Plummer, Figure 1-11

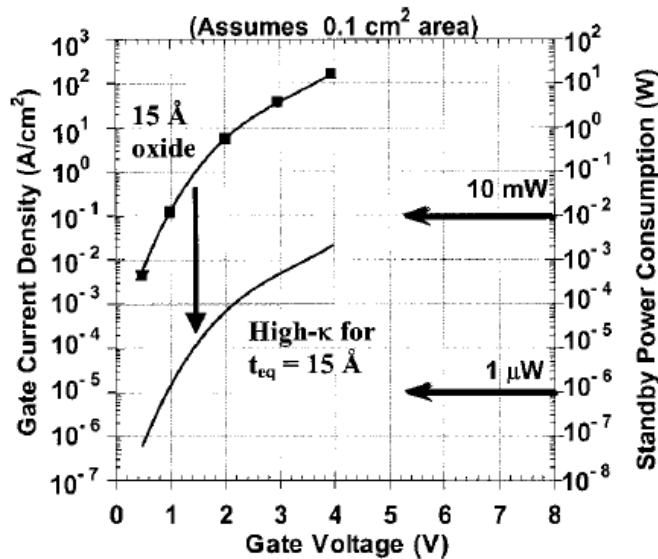
2. Gate Insulating Film

a. Materials

A common feature of a FET is the gate dielectric. (TSMC-1033, 288.) For decades prior to the '764 patent, silicon dioxide (SiO_2) was the primary material used for gate dielectrics in MOSFETs. (TSMC-1003, ¶46; TSMC-1033, 53 (“ SiO_2 is essentially a perfect insulator and provides the needed [electrical] isolation.”); TSMC-1032, 3-4.) As gate dielectric layers continued to shrink in thickness (e.g., below 1.5 nm), use of SiO_2 became untenable, because the amount of gate-to-

channel tunneling leakage-current passing through the gate dielectric prevents the gate electrode from effectively controlling the ON/OFF states of the FET. (TSMC-1003, ¶46; TSMC-1034, 4-5.)

High-k dielectrics, like Hf-based oxides, Ta₂O₅, or ZrO₂, replaced SiO₂ to address these challenges. (TSMC-1003, ¶¶47-48; TSMC-1034, 146.) For example, it was known by 2005 that, as compared to SiO₂, high-k materials significantly reduce the amount of leakage current and, thus, improve energy efficiency. (TSMC-1003, ¶49; TSMC-1018, 5250, Figure 5 (below); TSMC-1034, 146-47.)

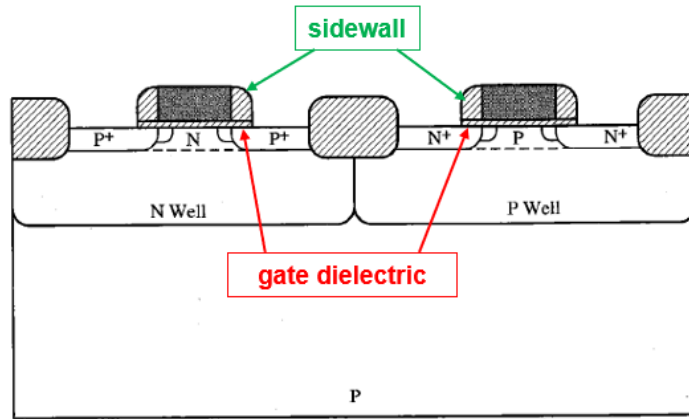


Wilk, Figure 5

b. Extended Gate Insulating Films

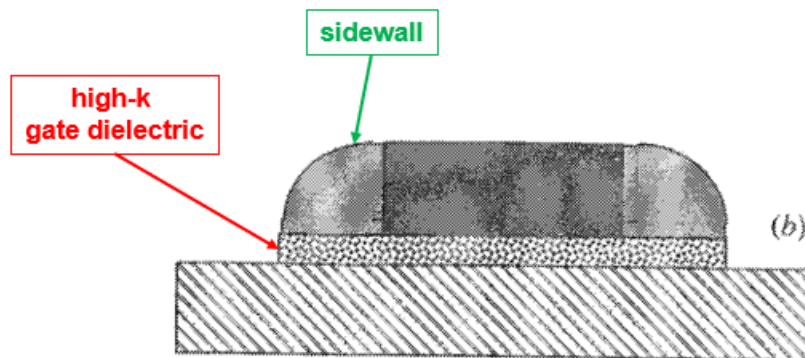
Prior to 2005, it was common practice to extend the gate dielectric from under the gate electrode to under the gate sidewalls. For example, Plummer depicts

a CMOS device having an extended gate dielectric in the NMOS and PMOS transistors. (TSMC-1003, ¶50; TSMC-1033, Figure 2-34 (below), 82-83.)



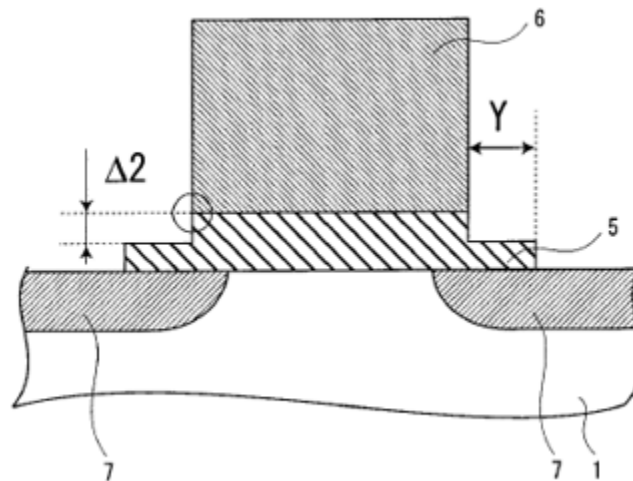
Plummer, Figure 2-34

Houssa discloses another example using a high-k material as the gate insulating film that extends from under the gate electrode to under the sidewalls. (TSMC-1032, 510.)



Houssa, Figure 5.1.9(b)

JP Publication 2005-064190 (“JP-Ono”⁵; TSMC-1040), filed two years before the ’764 patent, also describes extending the gate dielectric and varying its thickness. Specifically, JP-Ono adjusts both the reduction in thickness of the gate dielectric ($\Delta 2$) outside the gate electrode and the length of the gate dielectric from the outer edge of the gate electrode (Y) (i.e., how far the gate dielectric protrudes from under the gate electrode). (TSMC-1040, ¶35, Figure 3 (below); TSMC-1003, ¶¶53-54.)



JP-Ono, Figure 3

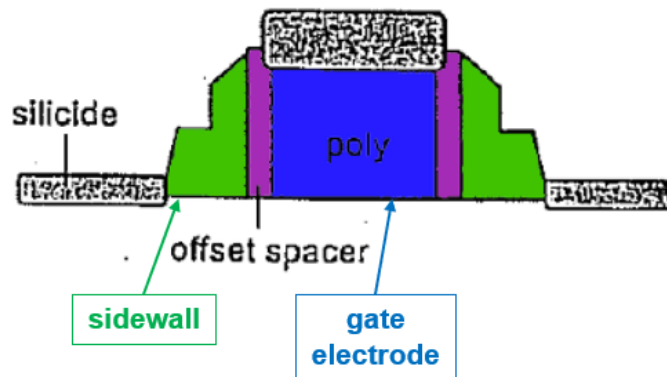
3. Sidewalls

Another common feature of a semiconductor device is sidewalls, vertical insulating structures formed on or proximate to the side surfaces of a gate

⁵ A certified translation of JP-Ono is included with TSMC-1040.

electrode. Sometimes, the terms “sidewall,” “spacer,” and “sidewall spacer” are used interchangeably. (TSMC-1003, ¶58.) Sidewalls serve a variety of purposes and functions in a semiconductor device such as defining the source/drain region, providing isolation, protecting the gate during subsequent fabrication, and controlling the width of the gate in the gate length direction. (*Id.*)

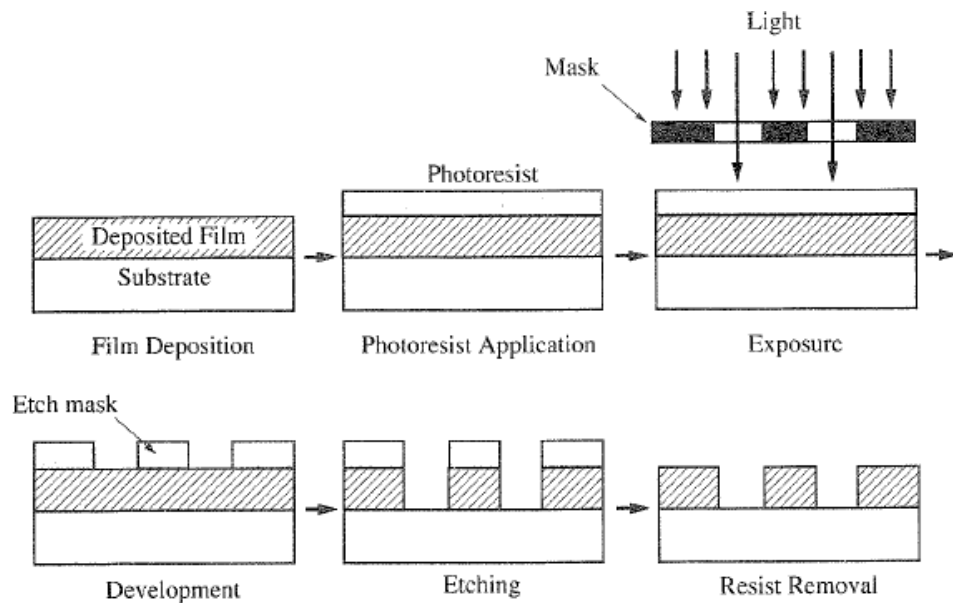
As a non-limiting example, sidewalls may be used for “[c]ontrolling the position of the edge of the SDE [source/drain extension] region with respect to the gate edge” so as to achieve optimal amount of overlap between the SDE and the gate edge. (TSMC-1034, 217.) As shown below, “an offset-spacer is fabricated on the side of the gate after the gate-poly is etched (but before the SDE implant step is carried out ...),” with offset-spacer width “varied from zero (no-spacer) to some upper-bound (e.g., 50-nm)” to achieve optimum device characteristics. (*Id.*)



Wolf, Figure 5-25

4. Etching Properties

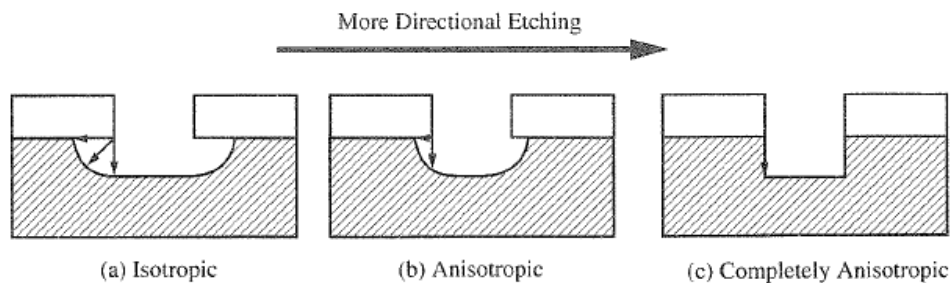
In semiconductor devices, thin films are often first deposited on the wafer surface and then selectively removed by etching to leave the desired pattern of the film. (TSMC-1003, ¶60; TSMC-1033, 609-11.) The desired pattern is often defined by placing a mask on the surface before etching; the mask is removed after etching. (TSMC-1003, ¶60; TSMC-1033, 609-10, Figure 10-1 (below).)



Plummer, Figure 10-1

Etching is performed in a “wet” or “dry” environment. (TSMC-1003, ¶61; TSMC-1033, 609, 612-37.) Wet etching involves the use of liquid etchants (e.g., hydrofluoric acid), whereas dry etching involves the use of gas-phase etchants in a plasma. (TSMC-1003, ¶61; TSMC-1033, 609.) Etching processes are also described based on the relative etch rates in different directions. (TSMC-1003, ¶60;

TSMC-1033, 610-11.) Isotropic etching occurs when the etch rate is the same in all directions, resulting in a semicircular etch profile as shown in Figure 10-3(a) below. Most wet chemical etchants etch isotropically. (TSMC-1033, 610-13.) Anisotropic etching occurs where there is little or no etching in the lateral direction. (TSMC-1033, 611, Figure 10-3(b), (c) (below).) For anisotropic etching, the amount of lateral etching may vary, such that the etched surface may be curved or sloped (TSMC-1033, Figure 10-3(b)) to completely vertical (TSMC-1033, Figure 10-3(c)). (TSMC-1003, ¶63.)



Plummer, Figure 10-3

C. '764 Patent Overview

The four semiconductor device embodiments presented in the '764 patent can be separated into two groups—single sidewall devices (first/fourth embodiments) and double sidewall devices (second/third embodiments). The '764 patent's claims are directed to double sidewall devices.

In the second embodiment (Figure 2 (left)), the high-k gate insulating film (shaded red) extends only under offset sidewall 6 (shaded purple) and has a smaller

thickness under offset sidewall 6 than under gate electrode 5 (shaded blue), corresponding, e.g., to claim 1. (TSMC-1001, 7:48-59.) In a modification (Figure 3 (right)), the thickness of the high-k gate insulating film is the same under both offset sidewall 6 and insulating sidewall 7 and is thinner under both sidewalls than under gate electrode 5, also corresponding to claim 1.

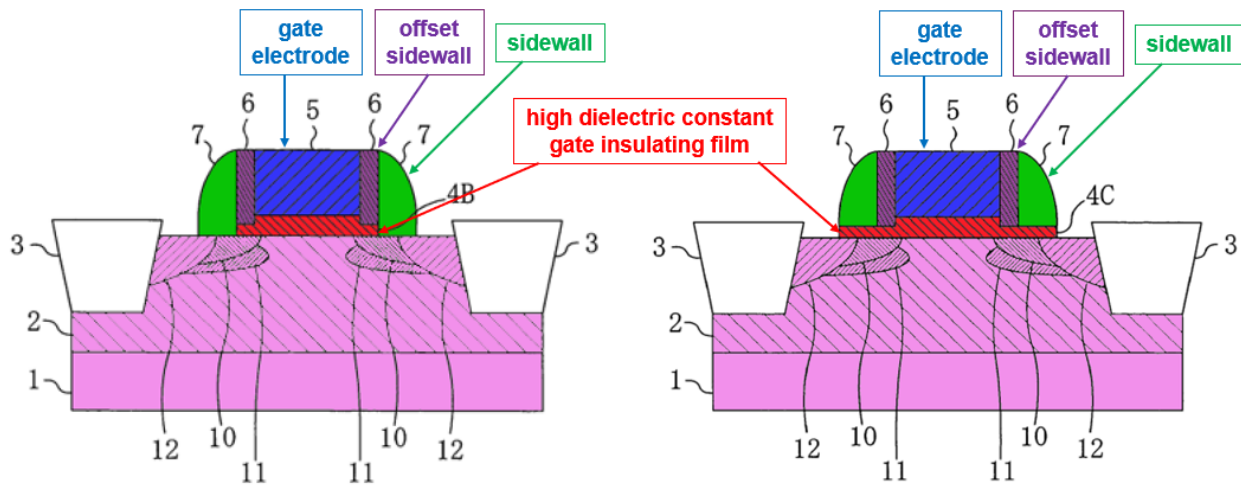


Figure 2

Figure 3

In the third embodiment device (Figure 5 (below)), the high-k gate insulating film has declining thicknesses under gate electrode 5, under offset sidewall 6, and under insulating sidewall 7, which also corresponds to claim 1. (TSMC-1001, 10:53-62.)

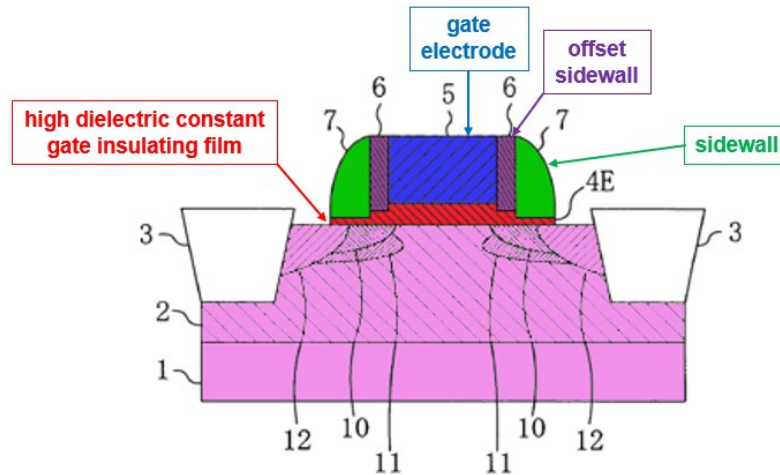


Figure 5

D. Prosecution History

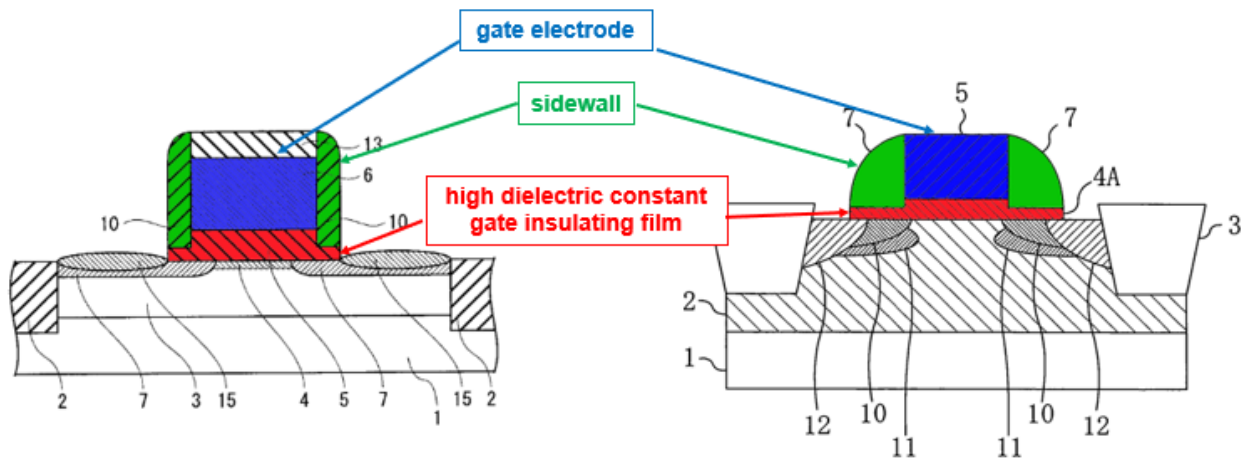
1. '764 Patent

The U.S. application was filed with one independent claim corresponding to issued claim 1. The Examiner rejected this claim as anticipated by U.S. Patent 6,992,358 to Hieda (“Hieda”). (TSMC-1002, 122-23.) Applicant did not amend the claims, successfully arguing the Examiner misapplied Hieda. (TSMC-1002, 142-44, 159.)

2. JP Application

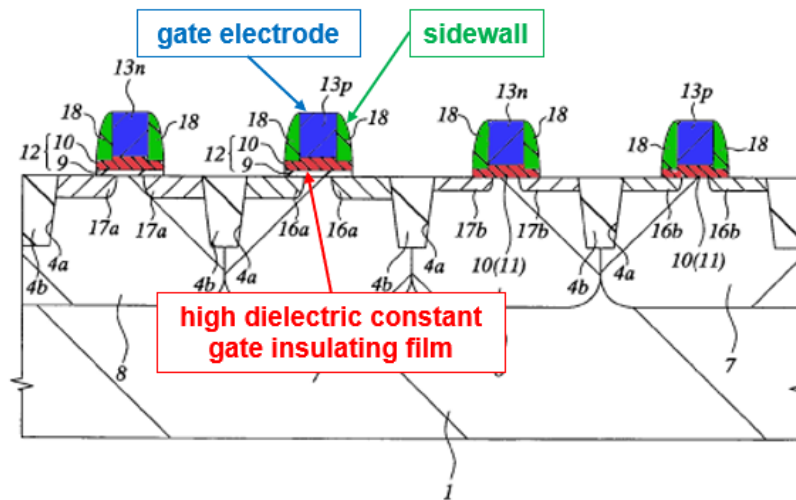
The JP priority application was filed with the same device claim originally filed with the application associated with the '227 patent. (TSMC-1005, 1.) On September 16, 2011, the JP-Examiner found this claim scope unpatentable, citing JP-Ono discussed above (Figure 23 (top-left)) and WO2004/017418 (“Sakai”; Figure 25 (below-bottom)), which both teach a high-k gate insulating film with a

smaller thickness under the sidewall than under the gate electrode, like e.g., the '764 patent's single sidewall embodiments. (TSMC-1005, 4-6; TSMC-1001, Figure 1 (top-right)).



JP-Ono, Figure 23

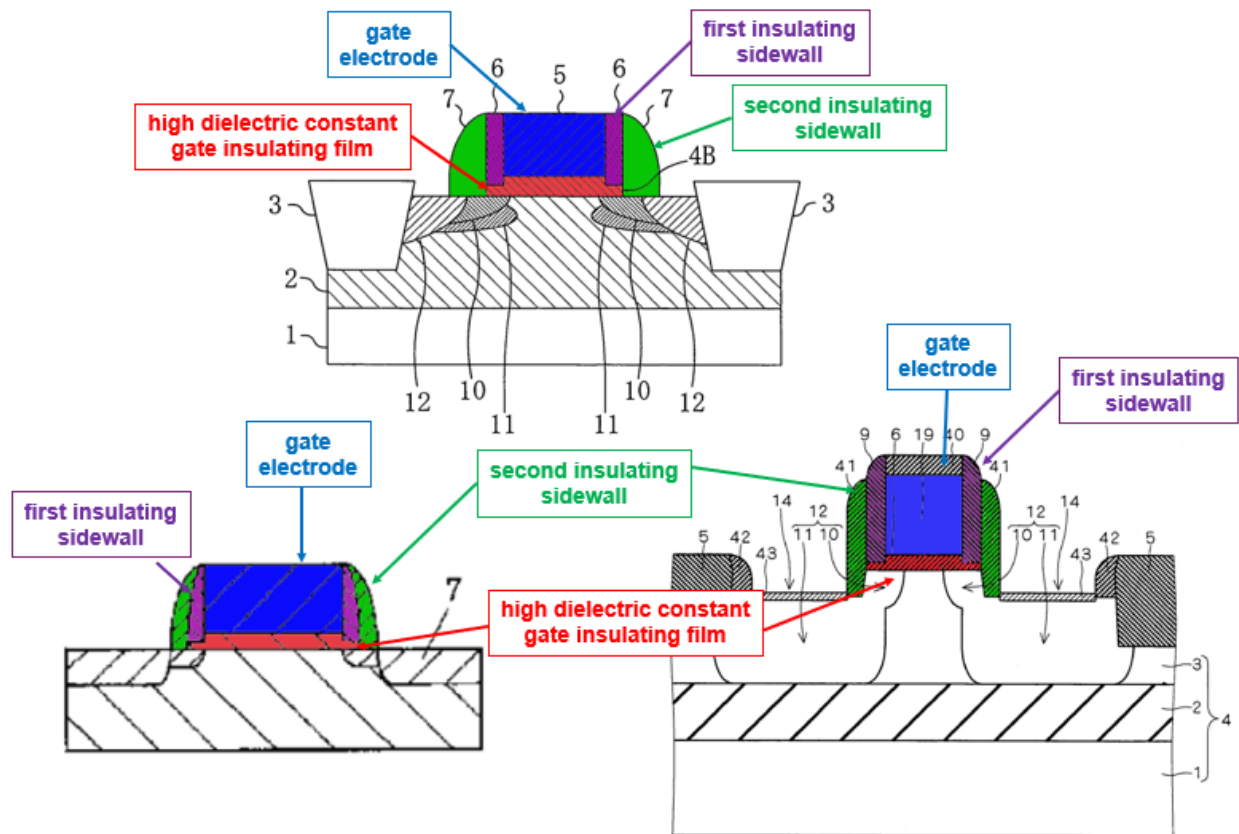
'764 Patent, Figure 1



Sakai, Figure 25

In response, Applicant narrowed the Japanese claim to recite (1) a double sidewall structure with a high-k film having a smaller thickness under a first

sidewall than under the gate electrode and (2) extension and source/drain regions. (TSMC-1005, 8.) The JP-Examiner rejected the amended claim based on both JP 2003-258241 to Kajiyama (“JP-Kajiyama”; TSMC-1010 (bottom-left)) and JP 2004-241755 to Matsumoto (“JP-Matsumoto” bottom-right) which each teaches the same basic structure as the ’764 patent’s Figure 2. (TSMC-1005, 14-16; *compare* TSMC-1001, Figure 2 (top).)



**’764 Patent, Figure 2 (top); JP-Kajiyama, Figure 1(D) (bottom-left);
JP-Matsumoto, Figure 33 (bottom-right)**

In response, Applicant further narrowed the claim to recite that the thickness of the high-k gate insulating film under the second sidewall is smaller than the

thickness under the first sidewall which is smaller than the thickness under the gate electrode. (TSMC-1005, 18.) The JP-Examiner allowed the claim based on this amendment. (TSMC-1005, 20.)

In short, to secure allowance over the prior art, PO acquiesced during JP prosecution that the scope of at least '764 patent issued claim 1 was known in the art.

E. Claim Construction

Petitioner does not believe any claims require construction to resolve the patentability disputes in this proceeding. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

F. Level of Ordinary Skill in the Art

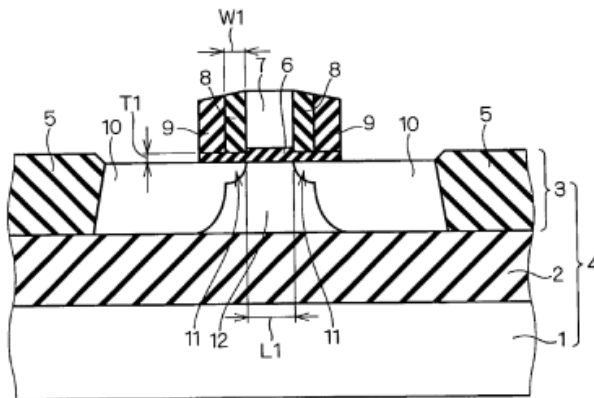
A POSITA would have had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. (TSMC-1003, ¶31.)

Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education. (*Id.*)

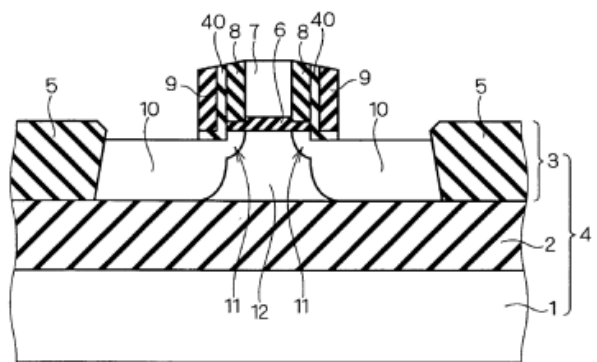
V. GROUND 1: Matsumoto Renders Claims 1, 4-5, 14-21⁶ Obvious.

A. Overview

This Petition focuses on Matsumoto's first and fourth embodiment MOSFETs which each includes gate insulating film 6 extending from under a gate electrode. In the first embodiment, gate insulating film 6 extends under both films 8 and 9 formed on the gate electrode's side surfaces. (TSMC-1009, ¶¶102-21, Figure 1 (below-left).) In the fourth embodiment, gate insulating film 6 extends under only film 8. (TSMC-1009, ¶¶137-40, Figure 22 (below-right).)



Matsumoto, Figure 1

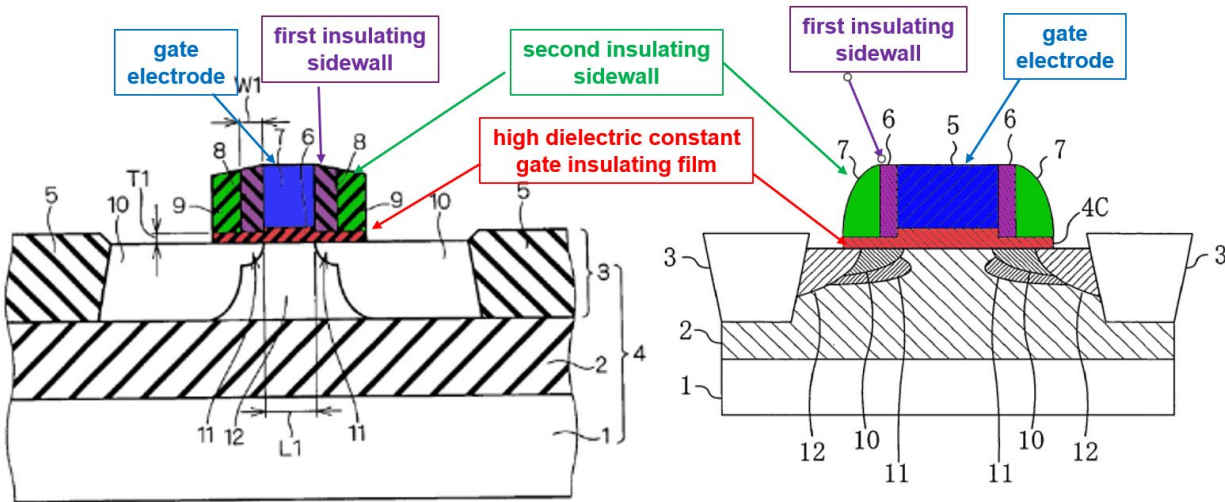


Matsumoto, Figure 22

⁶ A listing of challenged claims is provided in the Appendix.

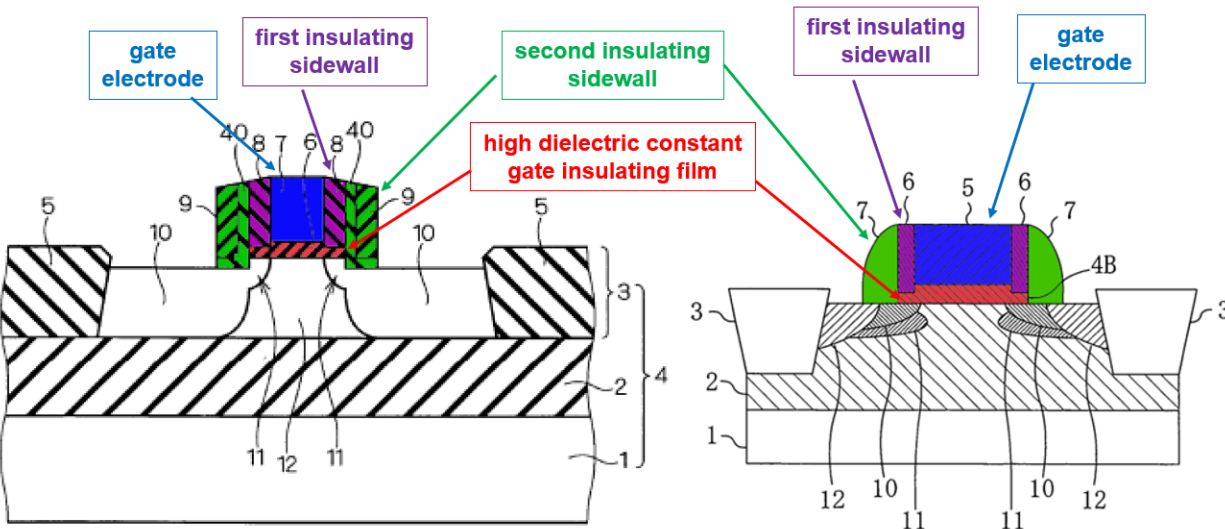
B. Independent Claim 1

Matsumoto's first and fourth embodiment devices each renders claim 1 obvious, as illustrated by the side-by-side figures below.



**Matsumoto, Figure 1
First Embodiment**

'764 Patent, Figure 3



**Matsumoto, Figure 22
Fourth Embodiment**

'764 Patent, Figure 2

1. Preamble [1P]

Matsumoto discloses a “*semiconductor device*”⁷: “The present invention relates to a **semiconductor device**.”⁸ (TSMC-1009, ¶¶2, 102, 137; TSMC-1003, ¶86.)

2. Limitation [1A]

Matsumoto’s first and fourth embodiments each teaches “*a high dielectric constant gate insulating film formed on an active region in a substrate*” [1A]. (TSMC-1003, ¶¶87-94.)

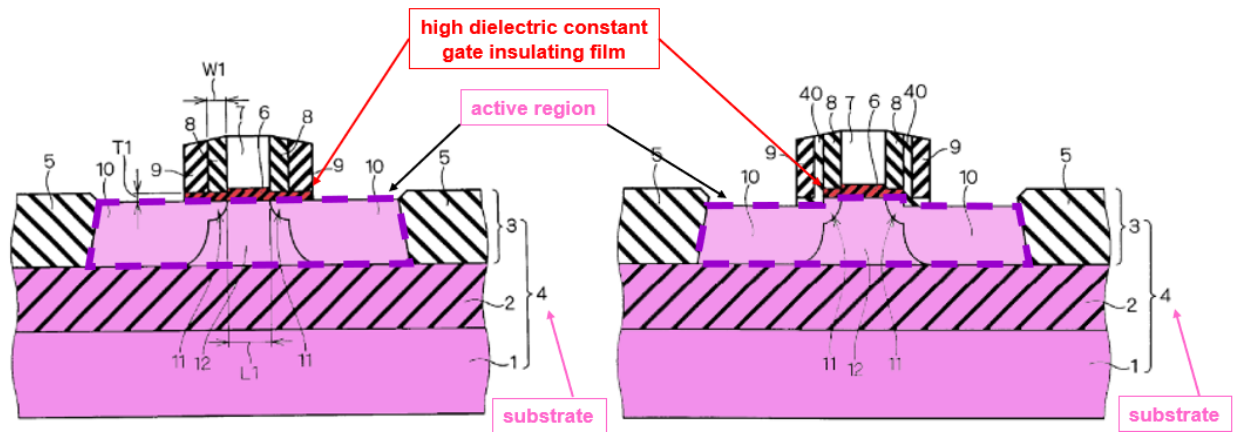
Both embodiments include “*a substrate*.” (TSMC-1003, ¶88.) Each device has multi-layer SOI **substrate 4** (shaded pink) with silicon substrate 1, BOX layer 2 and single-crystalline silicon layer 3. (TSMC-1009, ¶102, ¶¶137 and 140 (relating fourth embodiment to first embodiment); *Google LLC v. Jenam Tech, LLC*, IPR2021-00630, 2022 WL 4287797, *9 n.9 (P.T.A.B. Sept. 16, 2022) (applying same disclosure where “figures refer to corresponding features using the same reference numbers”).)

Isolating insulation film structures 5 “extend[ing] from the upper surface of silicon layer 3 to the upper surface of the BOX layer 2”, define a “**device region**.”

⁷ Claim language is indicated by italics throughout.

⁸ Unless otherwise noted, all emphasis added.

(TSMC-1009, ¶¶102-103, Figure 1 (below-left), ¶¶137, 140, Figure 22 (below-right).) The device region, identified by isolation regions, is an “*active region in a substrate*” and includes source/drain regions 10. (TSMC-1009, ¶¶105, 139; TSMC-1003, ¶89; TSMC-1001, 1:39-40, 7:30-47.)



Matsumoto, Figure 1

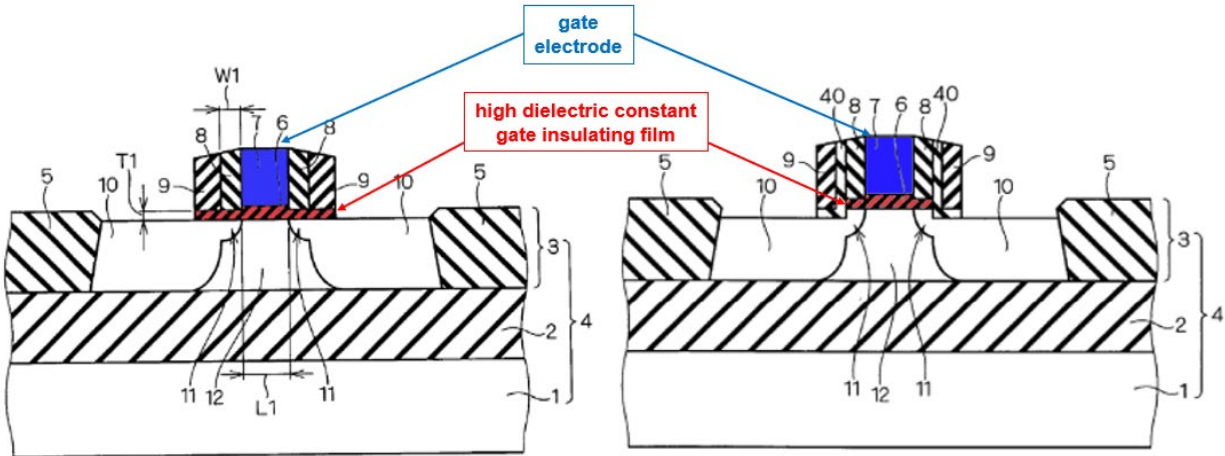
Film 6 “is formed partially on the upper surface of the silicon layer 3” in the device region with gate electrode 7 “formed partially” thereon. (TSMC-1009, ¶¶103, ¶137 (fourth embodiment’s gate electrode “formed by the process described in the first preferred embodiment”).) “A silicon oxynitride film, a metal oxide film such as Al_2O_3 or a ferroelectric film such as Ta_2O_5 and BST may be formed in place of the silicon oxide film 13” which is etched during fabrication to form film 6. (TSMC-1009, ¶¶107, 114, Figures 1, 9-10, ¶138, Figures 18-19, 22.) Al_2O_3 , Ta_2O_5 , and BST are high-k dielectrics. (TSMC-1003, ¶92; TSMC-1001, 1:28-30 (“**high dielectric constant film** formed of a Hf based oxide, Al based oxide or the

like”); TSMC-1018, Table I (identifying Al_2O_3 , Ta_2O_5 as high-k dielectrics).) A POSITA would have been motivated to use a high-k dielectric in Matsumoto’s device to address the well-documented issues with scaling SiO_2 to thicknesses needed for large scale device integration. (TSMC-1032, 3-12; TSMC-1034, 4-5, 146-47; TSMC-1003, ¶93.)

Film 6, present in both embodiments, is therefore “*a high dielectric constant gate insulating film formed on an active region in a substrate*” [1A]. (TSMC-1003, ¶¶90-94; *e.g.*, TSMC-1009, ¶103 (referring to film 6 as a “gate insulation film”).)

3. Limitation [1B]

Matsumoto’s first and fourth embodiments each teaches “*a gate electrode formed on the high dielectric constant gate insulating film*” [1B]. (TSMC-1003, ¶¶95-96.) In both embodiments, “**gate electrode 7** [shaded blue] made of polysilicon **is formed partially**” on high-k dielectric insulating film 6. (TSMC-1009, ¶103 (first embodiment), ¶107 (describing formation of high-k insulating film and gate electrode), Figure 1 (left), ¶¶137-38 (fourth embodiment), Figure 22 (right).)



Matsumoto, Figure 1

Matsumoto, Figure 22

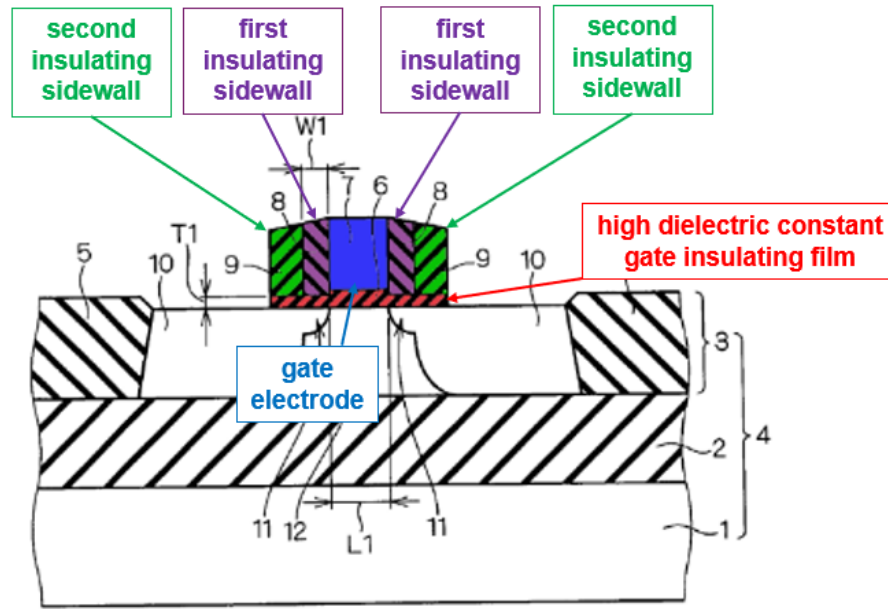
4. Limitations [1C]/[1D]

Matsumoto's first and fourth embodiments each teaches "*a first insulating sidewall formed on each side surface of the gate electrode*" [1C] and "*a second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween*" [1D]. (TSMC-1003, ¶¶97-102.)

In Matsumoto's first embodiment, "silicon nitride film 9 is formed on each side surface of the gate electrode 7, with a silicon oxide film 8 therebetween." (TSMC-1009, ¶103, Figure 1 (below).) Matsumoto refers to film 9 as a "sidewall insulation film" but does not refer to film 8 as a "sidewall." (TSMC-1009, ¶114 (describing nitride films 9a/9b "serving as **sidewall** insulation films").) A POSITA would have understood film 8 also to be a sidewall, as it is formed vertically on gate electrode 7's side surface. (TSMC-1009, ¶¶104, 110, 40 ("semiconductor device further includes a second sidewall formed on the side surface of the gate

electrode, with the first sidewall therebetween”); TSMC-1003, ¶99.) Because silicon oxide and silicon nitride are both insulators, silicon oxide film 8 is “*a first insulating sidewall*” [1C] and silicon nitride film 9 is “*a second insulating sidewall*” [1D]. (TSMC-1003, ¶99.) Both, as discussed above, are “*formed on*”⁹ the gate electrode’s side surfaces. (TSMC-1009, ¶110 (describing formation of silicon oxide films 8a/8b on the side surfaces of the gate electrodes), ¶114; TSMC-1009, claim 1 (referring to “insulation films” formed on side surfaces on gate electrode); TSMC-1003, ¶100.)

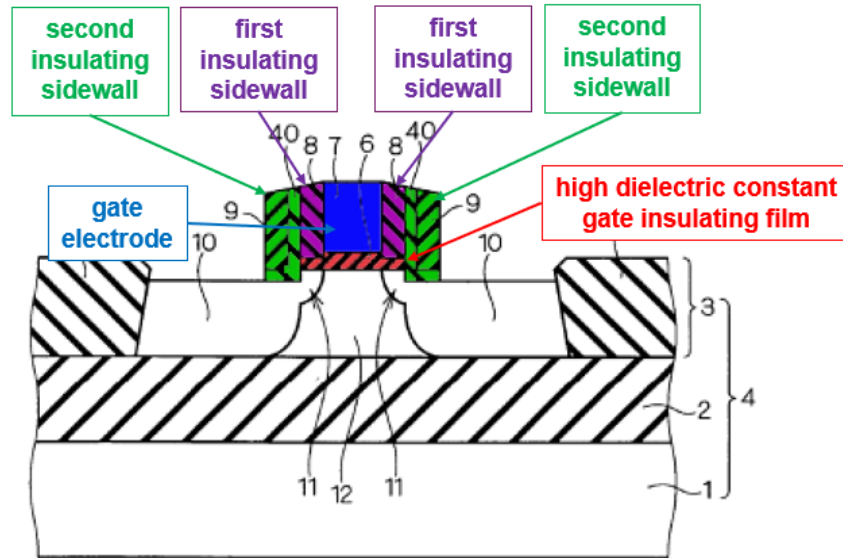
⁹ The ’764 patent uses the term “*formed on*” generally to refer to location and does not require contact. (TSMC-1001, 1:37-39, 7:32-37; TSMC-1003, ¶100 n.3.)



Matsumoto, Figure 1

In the fourth embodiment, silicon oxide film 40 and silicon nitride film 9 are formed “on the outer side surfaces of” film 8. (TSMC-1009, ¶139, Figure 22 (below), ¶110.) Film 8 (shaded purple) is “a first insulating sidewall” [1C] and film 9 (shaded green) alone, film 40 (shaded green) alone, or their combination is “a second insulating sidewall” [1D], consistent with the ’764 patent’s disclosure.¹⁰ (TSMC-1003, ¶102.)

¹⁰ The ’764 patent uses the term “insulating sidewall” to refer to a single component (TSMC-1001, 6:4-5), a collective structure of two components (TSMC-1001, 3:23-28), and a component having multiple layers (TSMC-1001, 20:66-21:8).



Matsumoto, Figure 22

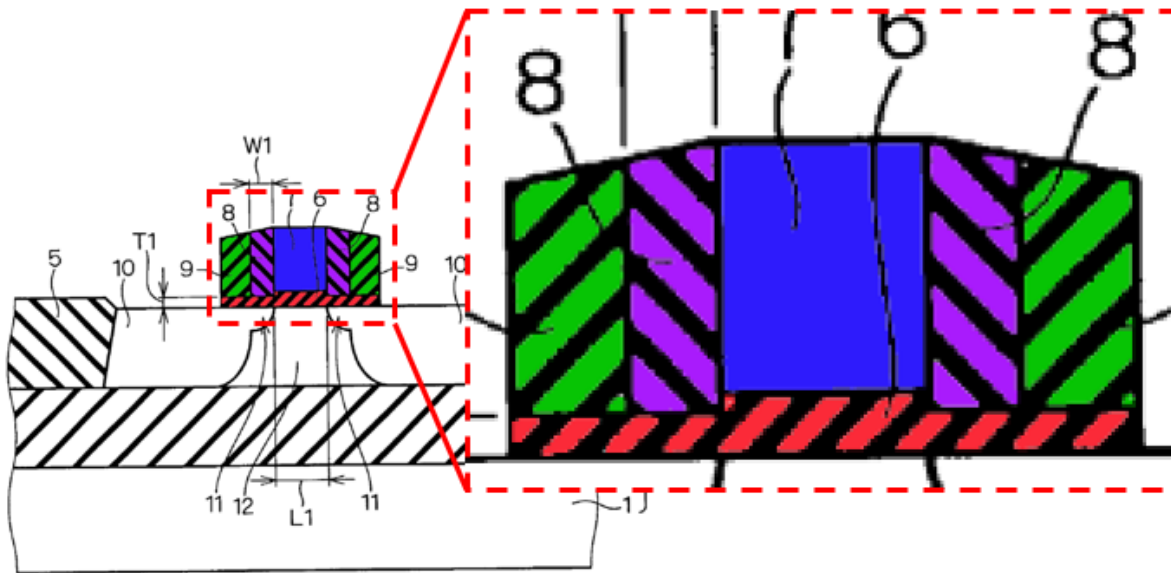
5. Limitations [1E]-[1F]

Matsumoto's first and fourth embodiments each teaches "*the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall*" [1E] and "*part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode*" [1F]. (TSMC-1003, ¶¶103-14.)

a. First Embodiment

As shown in the Matsumoto Figure 1 enlargement and confirmed by the disclosed process, high-k gate insulating film 6 (shaded red) is an uninterrupted layer (as evidenced by absence of gaps) extending from under the gate electrode 7 to under film 8 ("*first insulating sidewall*"). High-k film 6 is thinner under film 8

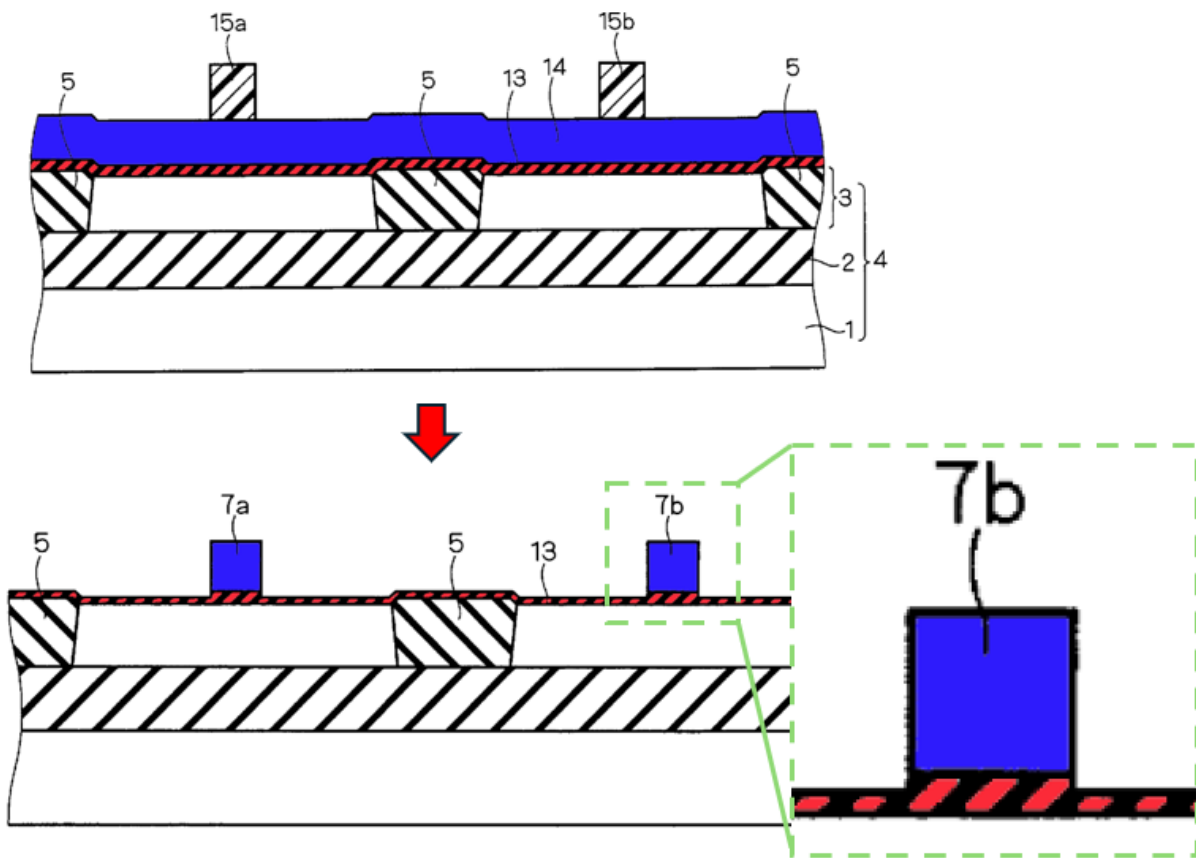
(“*first insulating sidewall*”; shaded purple) than it is under the gate electrode 7 (shaded blue). Matsumoto’s first embodiment device therefore discloses limitations [1E]-[1F]. *Unified Pats., LLC v. Oceana Innovations LLC*, IPR2020-01463, 2022 WL 500391, *17 (P.T.A.B. Feb. 14, 2022) (“patent drawing may serve as prior art ‘without referring to the surrounding description’ if ‘the prior art features are clearly disclosed by the drawing.’”) (citations omitted); TSMC-1003, ¶¶105-06.



Matsumoto, Figure 1 with enlargement

The fabrication process of the first embodiment device confirms the Figure 1 device structure. During fabrication, high-k dielectric film 13 (shaded red) is formed on the substrate and polysilicon film 14 (shaded blue) is formed on high-k dielectric film 13. (TSMC-1009, ¶107, Figure 3 (top).) The etching process used to

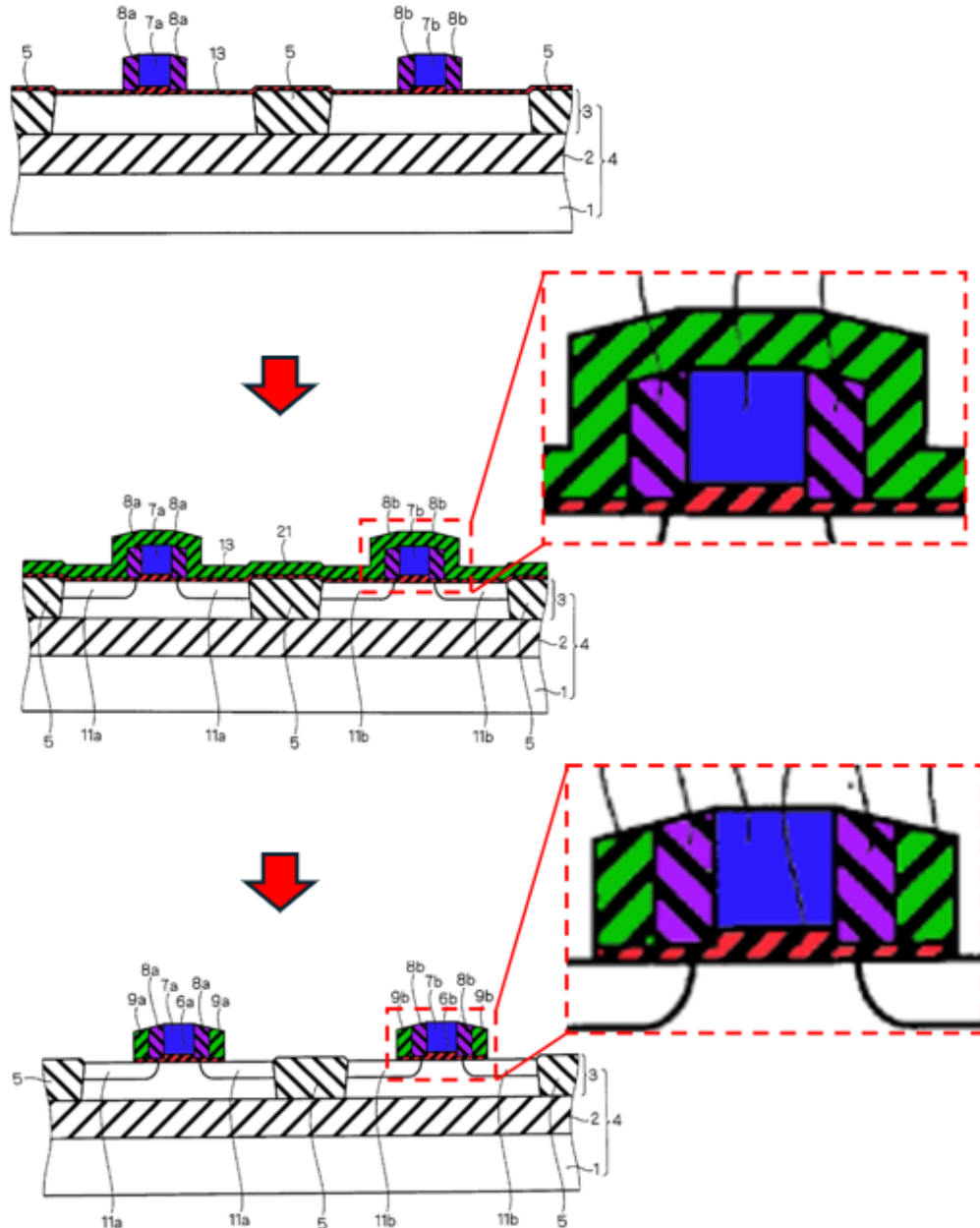
form the gate electrode “slightly etches the upper surface of” film 13, resulting in a high-k dielectric film with a larger thickness under the gate electrode than in the areas not under the gate electrode. (TSMC-1009, ¶108, Figure 4 (bottom); TSMC-1003, ¶107.)



Matsumoto, Figures 3 (top) and 4 (bottom) with enlargement

After formation of sidewalls 8a/8b (“*first insulating sidewall*”; shaded purple), silicon nitride film 21 is “formed on the entire top surface” of the intermediate structure. (TSMC-1009, ¶¶109-10, 114, Figure 6 (below-top), Figure 9 (below-middle).) Film 21 and film 13 are etched “until the upper surface of the

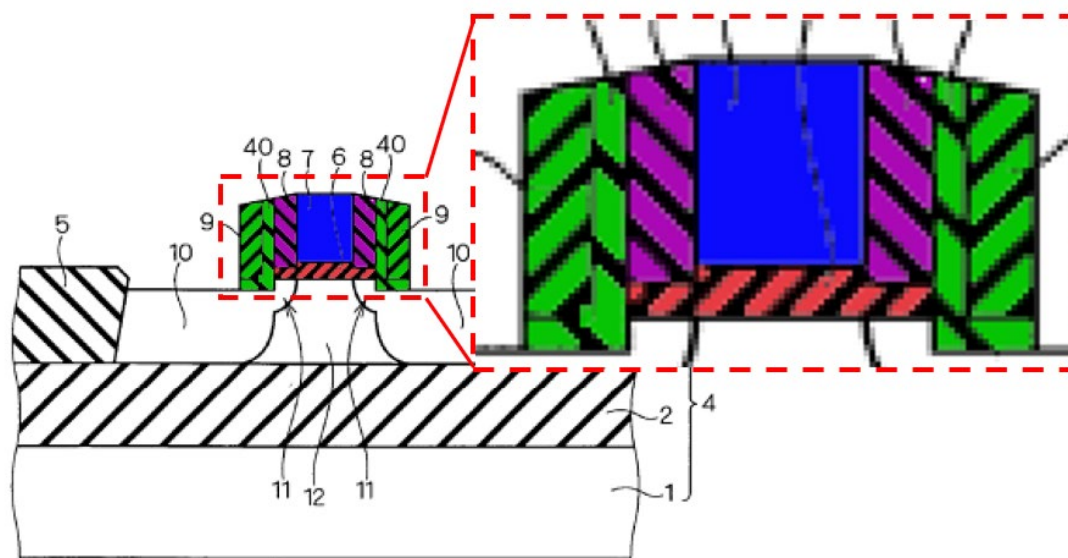
silicon layer 3 is exposed”, forming sidewalls 9a/9b (“*second insulating sidewall*”; shaded green). (TSMC-1009, ¶114, Figure 10 (below-bottom).) After this etching, the high-k dielectric film (shaded red) remains under the gate electrode and first and second sidewalls. (TSMC-1003, ¶108.)



Matsumoto, Figures 6 (top), 9 (middle), 10 (bottom) with enlargement

b. Fourth Embodiment

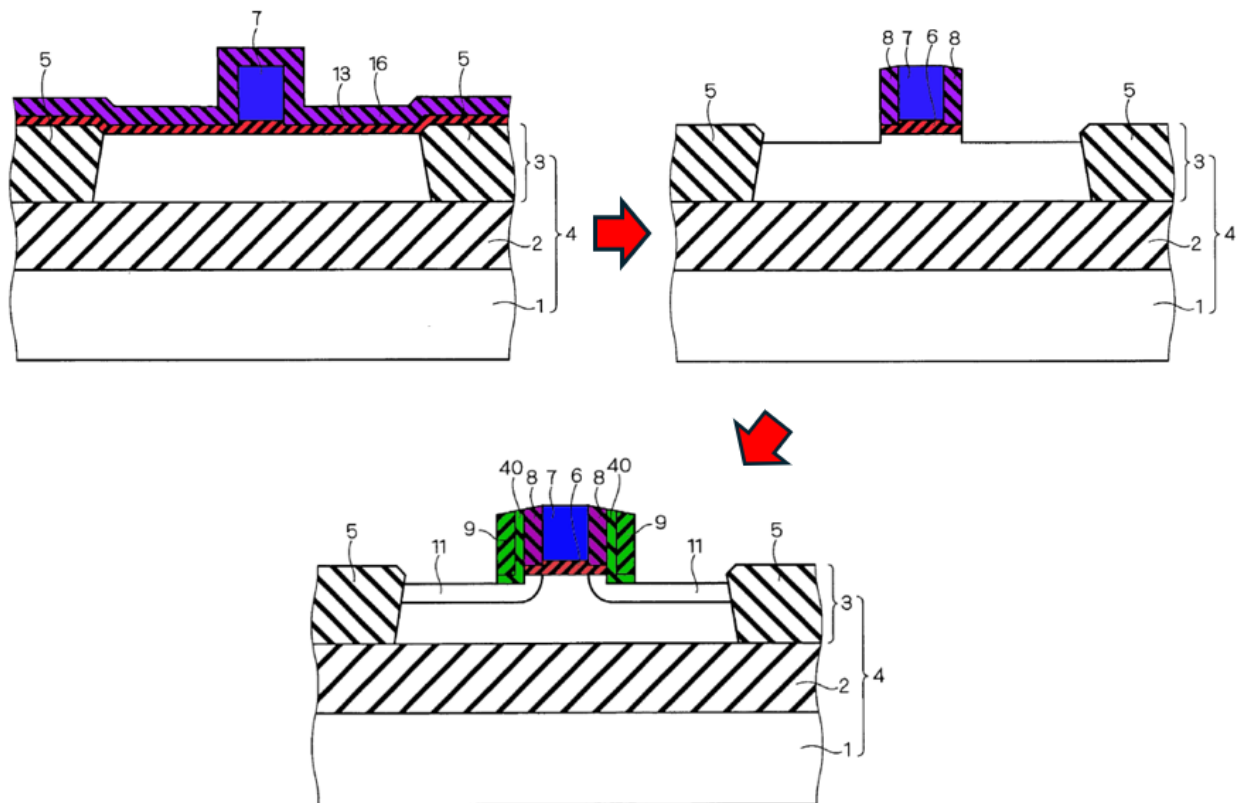
As shown in the Matsumoto Figure 22 enlargement and confirmed by the disclosed process, high-k gate insulating film 6 (shaded red) is an uninterrupted layer (as evidenced by absence of gaps) extending from under the gate electrode to under only film 8 (“*first insulating sidewall*”). The high-k film is thinner under film 8 (“*first insulating sidewall*”; shaded purple) than it is under the gate electrode (shaded blue). Matsumoto’s fourth embodiment device therefore discloses limitations [1E]-[1F]. *Unified*, 2022 WL 500391, *17; TSMC-1003, ¶¶110-11.



Matsumoto, Figure 22 with enlargement

The fabrication process of the fourth embodiment device confirms the Figure 22 device structure. During fabrication, “gate electrode 7 is formed by the process described in the first preferred embodiment”, resulting in high-k dielectric film 13 having a larger thickness under the gate electrode (Figure 18 (top-left)).

(TSMC-1009, ¶¶137, 107-08; TSMC-1003, ¶112.) The etching process that forms sidewall 8 (“*the first insulating sidewall*”; shaded purple) “overetch[es] the upper surface of the silicon layer 3” and as a result, the high-k dielectric film (shaded red) remains only under the gate and sidewall 8. (TSMC-1009, ¶138, Figure 19 (top-right); TSMC-1003, ¶113.) Film 40 and film 9 (alone or in combination the “*second insulating sidewall*” (shaded green)) are then formed on the outer side surfaces of film 8 and on the substrate surface. (TSMC-1009, ¶139; TSMC-1003, ¶113.)

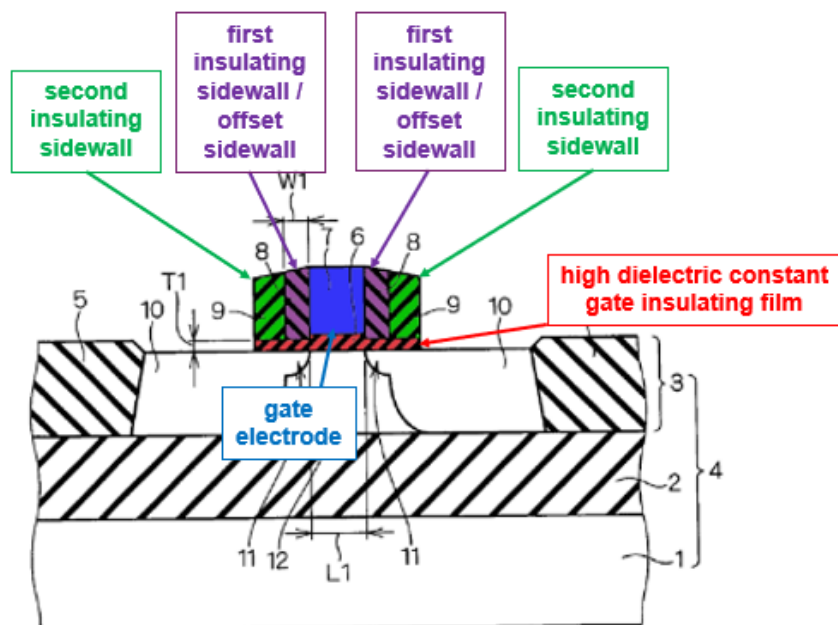


Matsumoto, Figures 18 (top-left), 19 (top-right), 21 (bottom)

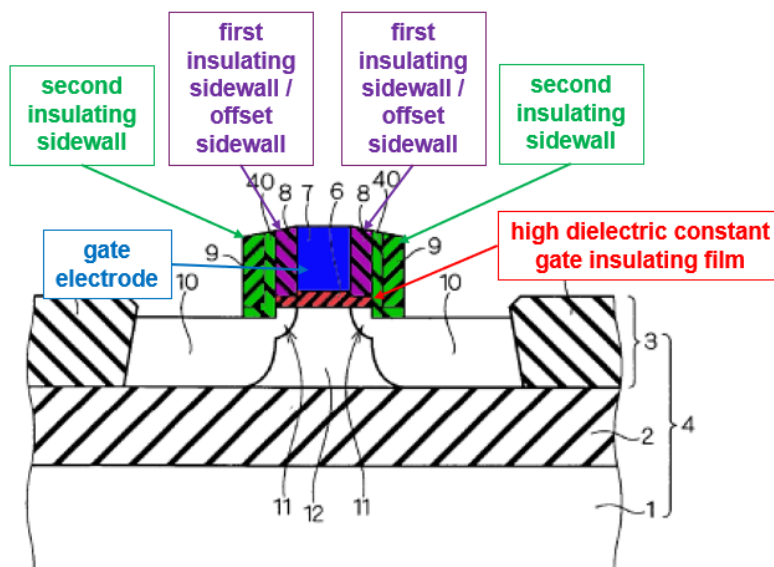
C. Claim 4

Matsumoto's first and fourth embodiments each teaches "*the first insulating sidewall is an offset sidewall*" [4]. (TSMC-1003, ¶115.)

In both embodiments, film 8 is the "*first insulating sidewall*." (§V.B.4.) Matsumoto expressly refers to film 8, which is located between gate electrode 7 and the "*second insulating sidewall*", as an "**offset** insulation film." (TSMC-1009, ¶155 ("The relationship between the width W1 of the **silicon oxide film 8 serving as an offset insulation film** ..."), ¶157 ("FIG. 28 is a graph of the **width W1 of the offset insulation film** versus the delay time t_{pd} ...), Figure 1 (below, showing width W1)); *Google*, 2022 WL 4287797, *9 n.9. Accordingly, in Matsumoto's first and fourth embodiment devices, film 8 "*is an offset sidewall*" [4]. (TSMC-1003, ¶115; TSMC-1001, 7:37-39 (referring to inner sidewall as an offset sidewall), Figure 2; TSMC-1034, Figure 5-25.)



Matsumoto, Figure 1

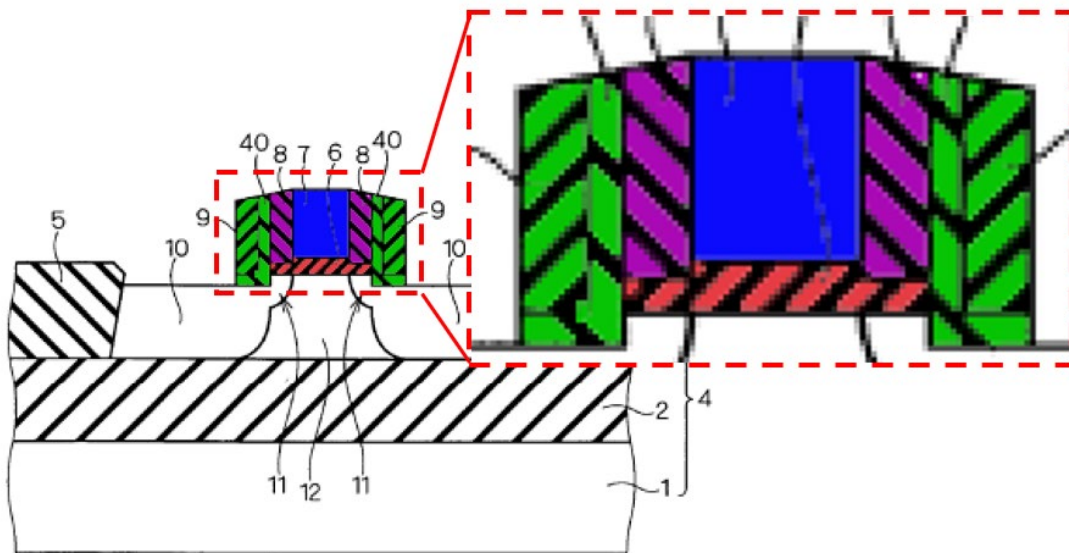


Matsumoto, Figure 22

D. Claim 5

Matsumoto's fourth embodiment teaches "*the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall*" [5]. (TSMC-1003, ¶¶116-19.)

As shown in the Matsumoto Figure 22 enlargement below and discussed in §V.B.5.b, high-k gate insulating film 6 (shaded red) extends only under film 8 ("*first insulating sidewall*") and is not located under films 40 and 9 (alone or collectively the "*second insulating sidewall*"). *Unified*, 2022 WL 500391, *17; TSMC-1003, ¶118. The fabrication process of the fourth embodiment, discussed in §V.B.5.b, confirms the Figure 22 device structure. (TSMC-1009, ¶¶138-39; TSMC-1003, ¶¶112-13.)



Matsumoto, Figure 22 with enlargement

E. Claim 14

Matsumoto's fourth embodiment teaches "*the second insulating sidewall has a double layer structure including an oxide film and a nitride film*" [14]. (TSMC-1003, ¶¶120-21.)

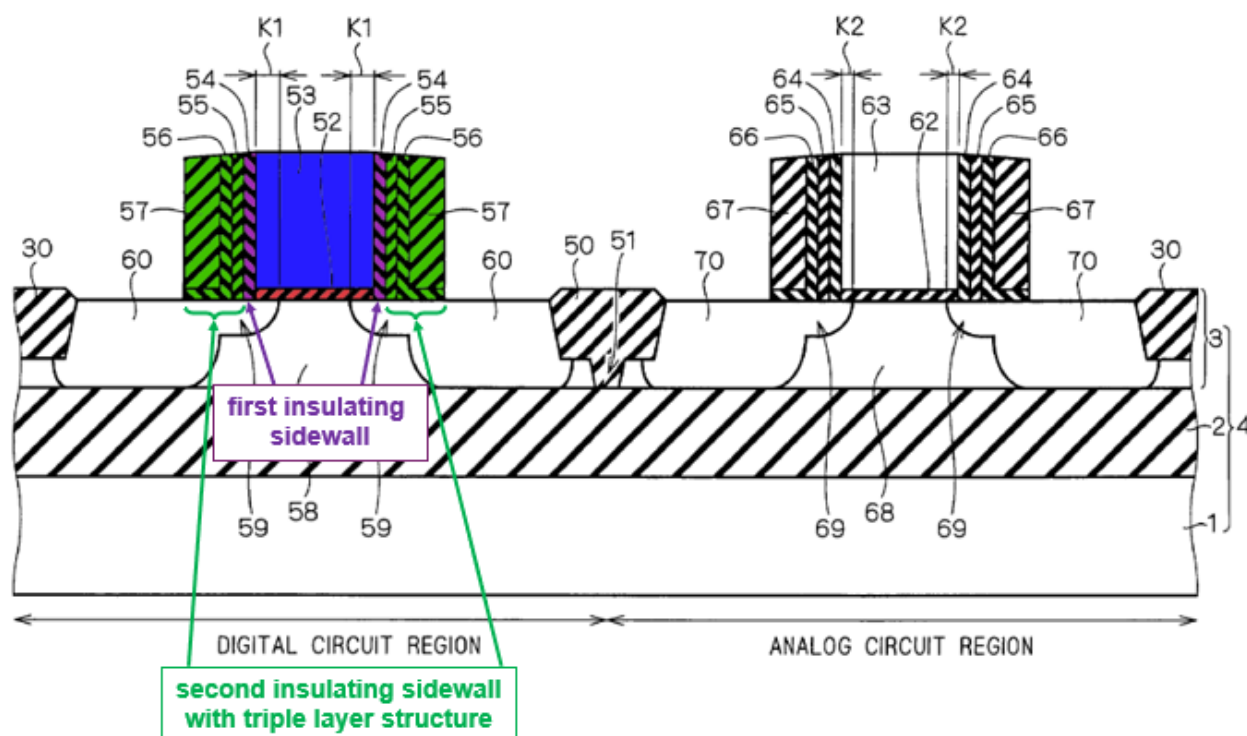
As discussed in §V.B.4, silicon **nitride** film 9 and silicon **oxide** film 40 are collectively the "*second insulating sidewall.*" (TSMC-1003, ¶121.) A POSITA would have considered the films to be "layers" of the collective sidewall structure, consistent with the '764 patent's disclosure. (TSMC-1003, ¶121; TSMC-1001, 20:66-21:8.) Accordingly, in Matsumoto's fourth embodiment, "*the second insulating sidewall has a double layer structure including an oxide film and a nitride film*" [14]. (TSMC-1003, ¶121.)

F. Claim 15

Matsumoto renders obvious "*the second insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film*" [15]. (TSMC-1003, ¶¶122-24.)

Matsumoto additionally discloses a digital FET, isolated from analog device regions, that includes silicon oxide film 54 ("*first insulating sidewall*"; shaded purple) "formed in contact with each side surface of the gate electrode 53." (TSMC-1009, ¶¶160, 162, Figure 29 (below).) Film 54 functions as an "offset insulation film." (TSMC-1009, ¶162.) Beyond this layer, "[a] silicon oxide film 55

is formed outside the silicon oxide film 54”, followed by a structure containing “a silicon oxide film 56 and a silicon nitride film 57.” (*Id.*) Together, silicon oxide films 55 (“*first oxide film*”) and 56 (“*second oxide film*”) along with silicon nitride film 57 (“*nitride film*”) form a “*second insulating sidewall*” with “*a triple layer structure.*” (TSMC-1003, ¶123.)



Matsumoto, Figure 29

It would have been obvious to a POSITA to modify Matsumoto’s fourth embodiment device by adding an additional oxide layer to the existing second insulating sidewall, which includes silicon nitride film 9 and silicon oxide film 40, as disclosed in the Figure 29 embodiment. (TSMC-1003, ¶124; *Boston Sci. Scimed, Inc. v. Cordis Corp.*, 554 F.3d 982, 991 (Fed. Cir. 2009) (“[c]ombining two

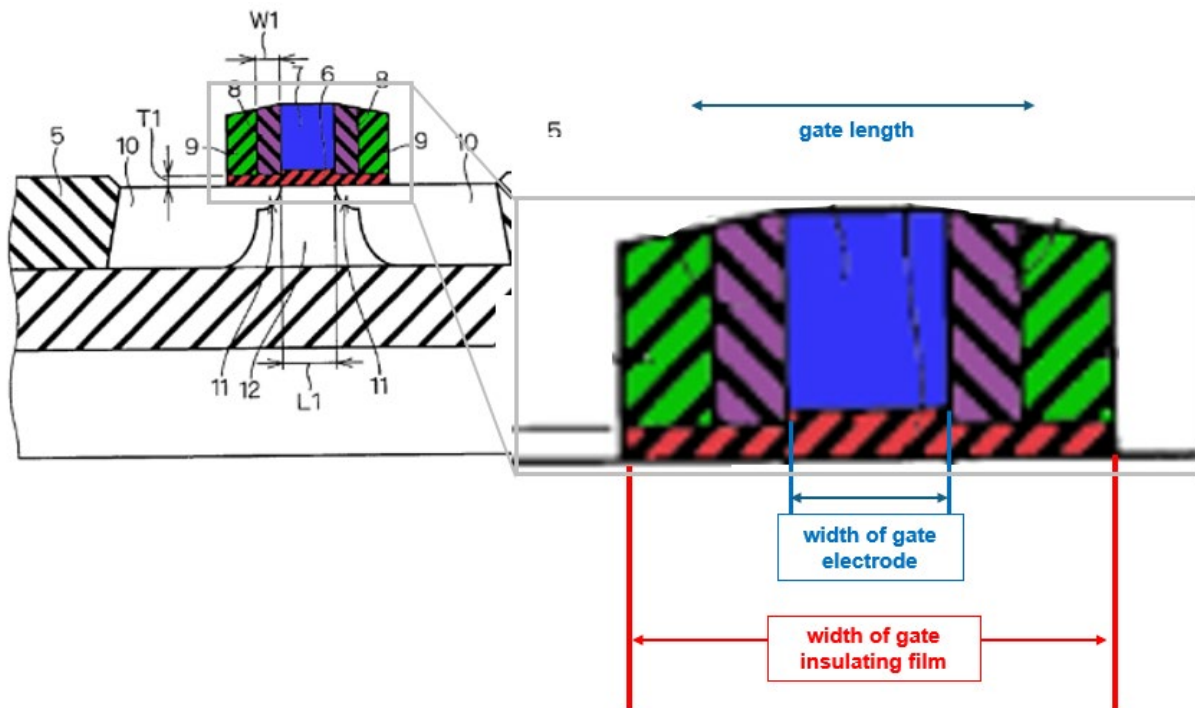
embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness.”.) Matsumoto expressly motivates the combination, stating that “[t]he structure according to the sixth preferred embodiment [Figure 29] is applicable to the semiconductor device of any one of the first to fifth preferred embodiments.” (TSMC-1009, ¶159; TSMC-1003, ¶124.)

G. Claims 16-17

Matsumoto’s first and fourth embodiments each teaches “*a width of the high dielectric constant gate insulating film along a gate length¹¹ is larger than a width of the gate electrode along the gate length*” [16] and “*a width of a bottom surface of the high dielectric constant gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length*” [17]. (TSMC-1003, ¶¶125-27.) As established in §V.B.5, high-k gate insulating film 6 in Matsumoto’s first and fourth embodiments extends from under the gate to under the first insulating sidewall 8. As illustrated in the figures below, the width of Matsumoto’s gate electrode 7 is constant across its entire height. The width of the high-k gate insulating film 6 (shaded red), including at film 6’s bottom surface, is

¹¹ The ’764 patent uses the term “gate length” to refer to a direction, specifically from source to drain regions. (TSMC-1003, ¶126 n.6.)

larger than the width of the gate electrode 7 (shaded blue), including at gate electrode 7's bottom surface. (TSMC-1003, ¶¶126-27.) The fabrication process of both embodiments discussed in §§V.B.5a-b confirms the structures of Figures 1 and 22.



Matsumoto, Figure 1 with enlargement



The diagram shows a cross-section of a gate electrode. A blue line at the top represents the gate electrode, with a dimension line indicating its width. Below it is a red line representing the gate insulating film, with a dimension line indicating its width.

Matsumoto’s first and fourth embodiments, using knowledge of a POSITA, as reflected in AAPA, renders “*the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more*” [18] and “*the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall*” [19] obvious. (TSMC-1003, ¶¶128-30.)

a relative dielectric constant of about 4.” (TSMC-1001, 1:28-31 (background-

AAPA).) Although not mentioned in the '764 patent, the dielectric constant of Si_3N_4 is 7, a fact that would have been known to a POSITA. (TSMC-1018, Table 1.) Matsumoto teaches use, e.g., of “ Ta_2O_5 ” as a gate insulating film. (TSMC-1009, ¶107.) The dielectric constant for Ta_2O_5 is known to be 26, which is greater than 10. (TSMC-1018, Table I.) Sidewall film 9 is comprised of silicon nitride (Si_3N_4), which has a dielectric constant of 7 which is less than the dielectric constant for Ta_2O_5 . (TSMC-1009, ¶¶114, 139; TSMC-1018, Table I; TSMC-1003, ¶¶129-30; TSMC-1052, Figure 4 (Si_3N_4 has dielectric constant of 7.2).)

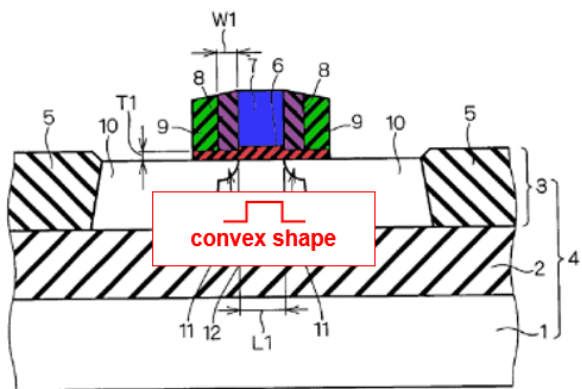
I. Claim 20

Matsumoto's first and fourth embodiments each teaches “*the high dielectric constant gate insulating film is formed to have a convex cross-sectional shape*” [20], consistent with the '764 patent's disclosures. (TSMC-1003, ¶¶131-33.)

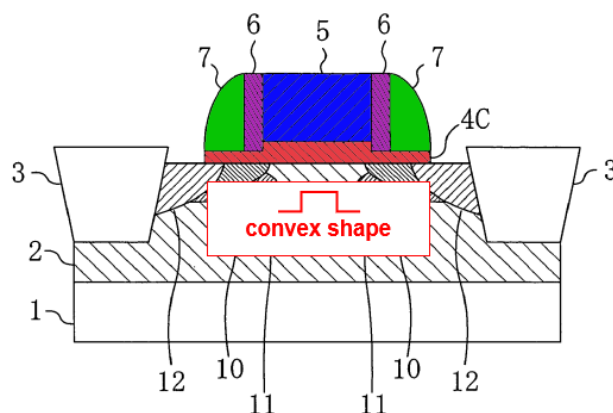
As illustrated below, the part of gate insulating film 6 under first and second insulating sidewalls 8, 9 in Matsumoto's first embodiment (Figure 1 (top-left)) and under the first insulating sidewall in Matsumoto's fourth embodiment (Figure 22 (bottom-left)) has a smaller thickness than the part of gate insulating film 6 under gate electrode 7. This forms a gate insulating film 6 having a generally convex cross-sectional shape, consistent with the disclosure of the '764 patent's Figure 2 (bottom-right):

have a convex shape.

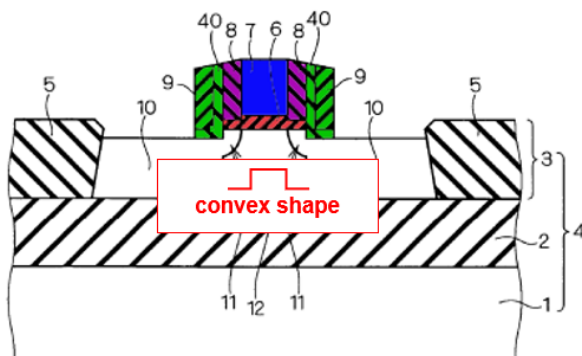
(top-right)); *Unified*, 2022 WL 500391, at *17.)



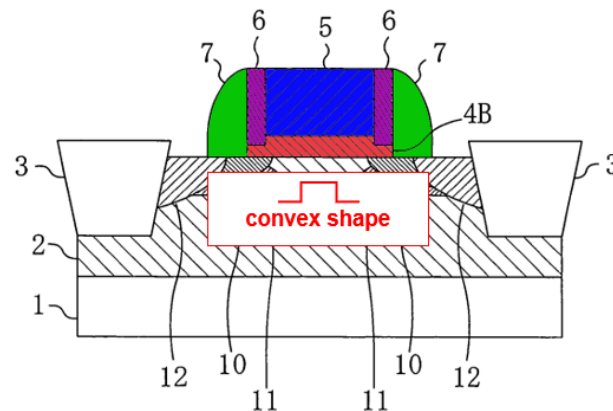
Matsumoto, Figure 1



'764 Patent, Figure 3



Matsumoto, Figure 22

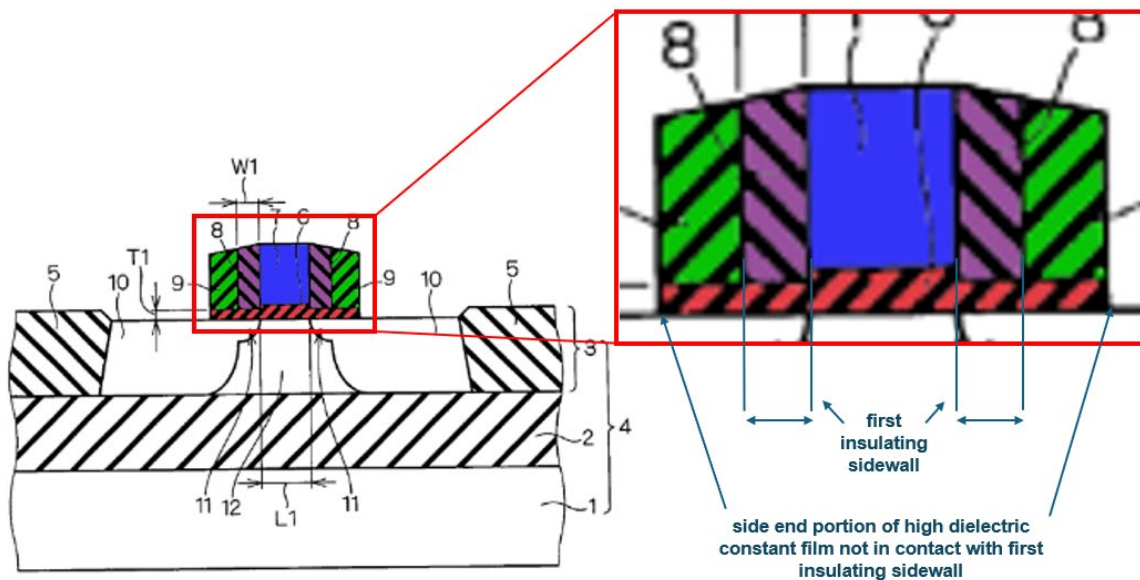


'764 Patent, Figure 2

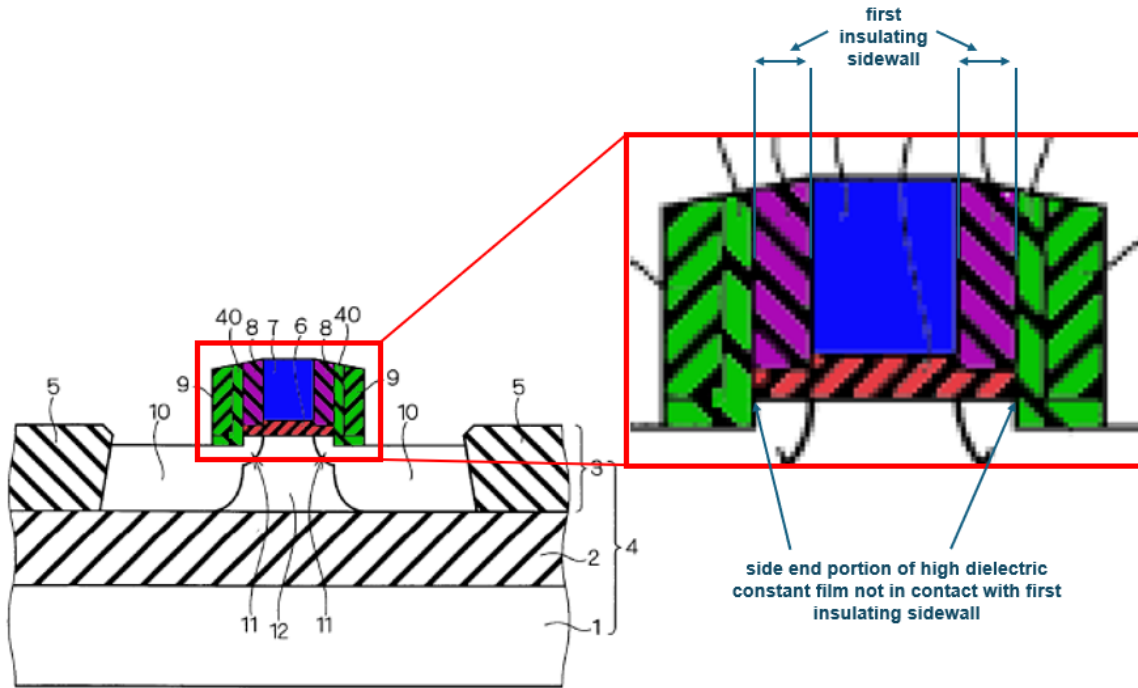
J. Claim 21

Matsumoto's first and fourth embodiments each teaches "*each side end portion of the high dielectric constant gate insulating film is not in contact with the first insulating sidewall*" [21]. (TSMC-1003, ¶¶134-39.)

As discussed in §V.B.5, gate insulating film 6 extends from under gate electrode 7 to under film 8 ("*first insulating sidewall*"). In the first embodiment, gate insulating film 6 further extends under film 9. Because film 6 is completely under film 8 in both embodiments, its side end cannot contact sidewall film 8. (TSMC-1003, ¶139.)



Matsumoto, Figure 1 with enlargement



Matsumoto, Figure 22 with enlargement

VI. GROUND 2: Matsumoto-Wang Combination Renders 2-3, 6-7, and 11 Obvious.

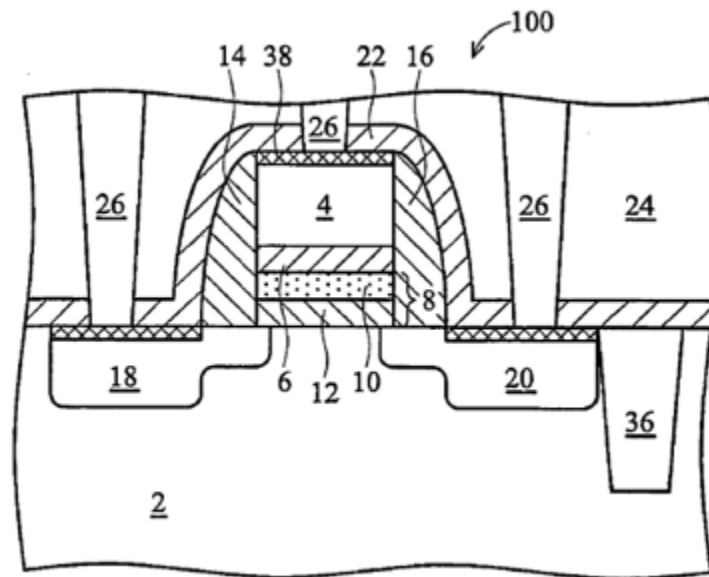
Matsumoto does not expressly disclose “a buffer insulating film” recited in claims 2-3. And while Matsumoto discloses exemplary high-k dielectrics, it does not explicitly disclose a high-k film “formed of a Hf based oxide” [6], “of a HfSiON film” [7] or with “thickness of 2 nm or less” [11]. Wang discloses these teachings.

A. Wang

Wang’s transistor 100 includes a gate stack with high-k dielectric layer 6 formed on dielectric layer 8 comprising a nitrated portion 10 and a non-nitrated/substantially nitride-free portion 12. (TSMC-1012, ¶¶22, 24, 48, Figure 3

(below).) Wang and Matsumoto are in the same field as the '764 patent, “a semiconductor device and a method for fabricating.” (TSMC-1001, 1:15-16; TSMC-1009, ¶2; TSMC-1012, ¶2; TSMC-1003, ¶141.)

Wang presents a list of alternatives for its high-k gate dielectric including Hf-based dielectrics (e.g., HfO₂, HfSiO, HfON, or HfSiON). (TSMC-1012, ¶¶9, 25.)

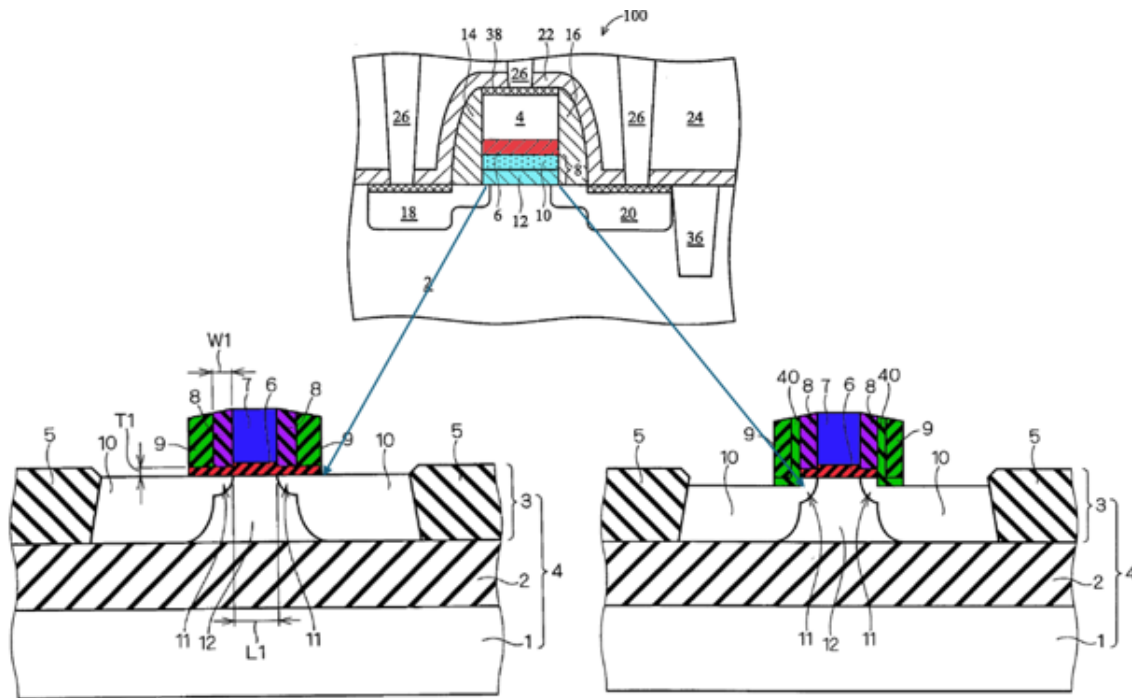


Wang, Figure 3

B. Claims 2-3

The combination of Matsumoto (first/fourth embodiments) and Wang discloses “a buffer insulating film between the substrate and the high dielectric constant gate insulating film” [2] where “the buffer insulating film is a silicon oxide film” [3]. (TSMC-1003, ¶¶144-53.)

A POSITA would have been motivated to combine Wang's teachings regarding use of a dielectric layer between a high-k gate insulating film and the silicon substrate with Matsumoto's first and fourth embodiment devices. (TSMC-1003, ¶¶148-49.) For example, a POSITA would have been motivated to integrate Wang's underlying dielectric layer 8 (shaded aqua) under Matsumoto's high-k dielectric (shaded red) in the first embodiment device (Figure 1) and fourth embodiment device (Figure 22). (TSMC-1003, ¶144.)



Wang, Figure 3 (top); Matsumoto, Figures 1 (left), 22 (right)

Wang's underlying dielectric 8 is "preferably formed of silicon oxide" and "has a first, nitrided portion 10 that is in contact with high-k dielectric layer 6 and a second non-nitrided, or substantially nitrogen-free, portion 12 that is in contact

with the underlying substrate 2.” (TSMC-1012, ¶48.) Underlying dielectric 8 is therefore a “*buffer insulating film*” and a “*silicon oxide film*” (e.g., in non-nitrided portion 12). (TSMC-1003, ¶145.) Alternatively, portion 12 is the “*buffer insulating film*.” (*Id.*) In the combination, Wang’s underlying dielectric is between the substrate and Matsumoto’s high-k gate insulating film 6.

Wang explicitly motivates the above combination, teaching that “[d]ue to the undesirable interactions between high-k dielectrics and the underlying semiconductor material (usually silicon, germanium, silicon germanium, and the like) to degrade carrier mobility, a thin silicon oxide layer is typically employed as part of the gate dielectric even when a high-k gate dielectric is employed.” (TSMC-1012, ¶3.) This is consistent with the purpose of the buffer insulating film in the ’764 patent. (TSMC-1001, 12:9-18 (by using a buffer insulating film, “deterioration of an interface between a substrate and a gate insulating film can be suppressed”).) Wang further stresses that “underlying dielectric layer 8 advantageously provides higher mobility and higher reliability for the high-k peripheral (or I/O) device.” (TSMC-1012, ¶28.) A POSITA would have therefore been motivated to use Wang’s buffer insulating layer to improve carrier mobility and performance of the Matsumoto’s first or fourth embodiment device. (TSMC-1003, ¶¶148-49; TSMC-1009, ¶13 (describing objective to reduce malfunctions and operating characteristic variations).)

Applying Wang's buffer layer to Matsumoto's first or fourth embodiment device is merely use of a known technique (Wang's buffer insulating layer) to improve similar devices in the same way for the above reasons. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-17 (2007); TSMC-1003, ¶150. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable because Wang uses established methods for forming the underlying dielectric and its high-k gate dielectric. (TSMC-1012, ¶22 (describing "thermally grown oxide"), ¶24 (describing use of CVD, ALD and PVD for deposition of high-k film); TSMC-1009, ¶107 (describing use of CVD for high-k film deposition); TSMC-1003, ¶¶151-53.)

C. Claims 6-7

The combination of Matsumoto (first/fourth embodiments) and Wang discloses "*the high dielectric constant gate insulating film is formed of a Hf based oxide*" [6] and "*the high dielectric constant gate insulating film is formed of a HfSiON film*" [7]. (TSMC-1003, ¶¶154-60.)

Matsumoto teaches use of a high-k film "such as Al₂O₃ or a ferroelectric film such as Ta₂O₅ and BST" as a gate insulating film. (TSMC-1009, ¶107.) Wang teaches use of similar high-k dielectrics (e.g., Al₂O₃ and Ta₂O₅) and others including "**HfSiON**" and "**HfO₂**." (TSMC-1012, ¶12; TSMC-1012, ¶¶9, 25.)

By 2005, a POSITA would have been motivated to select HfO₂ given its known benefits, including, for example, “its superior thermal stability with poly-Si and reasonable band alignment.” (TSMC-1037, 2.4.1; TSMC-1032, 207 (HfO₂ “combines a high k (15–26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ...”); TSMC-1049, 134 (“Excellent dielectric properties ... suggest that HfO₂ is a promising material for the future gate dielectric application.”); TSMC-1003, ¶158.) Another known benefit is that HfO₂ can be scaled down to a smaller EOT. (TSMC-1032, 207; TSMC-1003, ¶158.)

A POSITA would have also been motivated to use HfSiON to further enhance operation because nitrogen incorporation was found to improve thermal stability and electrical characteristics of HfSiON, including by enhancing the dielectric constant of the film. (TSMC-1029, 849; TSMC-1003, ¶159.)

D. Claim 11

Wang further teaches that for a HfSiON gate insulating layer, the film “was deposited to a thickness of about 5 to 50 Angstroms [0.5 to 5 nm] and having an equivalent oxide thickness (EOT) of less than about 2.0 nanometers.” (TSMC-1012, ¶34.) Thus, in combination with Matsumoto, the thickness of the HfSiON gate insulating film at its side ends would also range from about less than 5 Angstroms to less than 50 Angstroms since the thickness of the layer is smaller

under sidewall 8 than under the gate electrode 7. (TSMC-1003, ¶¶162-63.) The thickness of 2 nm (20 Angstroms) falls within the range of thicknesses disclosed by Wang. (TSMC-1003, ¶163.) The '764 patent provides no discussion, evidence, or justification for the selection of 2 nm as the thickness of the gate insulating film. “[W]here there is a range disclosed in the prior art, and the claimed invention falls within that range, the burden of production falls upon the patentee to come forward with evidence’ of teaching away, unexpected results or criticality, or other pertinent objective indicia indicating that the overlapping range would not have been obvious in light of that prior art.” *E.I. DuPont de Nemours & Co. v. Synvina C.V.*, 904 F.3d 996, 1008 (Fed. Cir. 2018). Thus, the Matsumoto-Wang combination renders obvious that “*each side end portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less*” [11]. *Ormco Corp. v. Align Tech., Inc.*, 463 F.3d 1299, 1311 (Fed. Cir. 2006) (“Where a claimed range overlaps with a range disclosed in the prior art, there is a presumption of obviousness.”) (citation omitted); TSMC-1003, ¶164.

VII. GROUND 3: Matsumoto-Wang-Sim Combination Renders Claim 11 Obvious.

Should an argument be made the combination of Matsumoto and Wang does not render claim 11 obvious, Sim explicitly describes use of a gate insulating film having a thickness 2 nm or less. Sim, like Matsumoto and Wang, is in the same

field as the '764 patent, “a semiconductor device and a method for fabricating.” (TSMC-1001, 1:15-16; TSMC-1009, ¶2; TSMC-1012, ¶2; TSMC-1024, Abstract; TSMC-1003, ¶165.)

Sim highlights that “[h]afnium-based high-k dielectrics and metal gate electrodes have been aggressively investigated to ensure continued scaling of CMOS technology, but several drawbacks such as low mobility and charge trapping have been identified.” (TSMC-1024, 218.) To address these issues, Sim “systematically evaluated the effects of high-k film thickness on charge trapping and channel carrier mobility” and found that “scaling the high-k dielectric is a simple, but very effective means of improving mobility and other reliability characteristics.” (*Id.*) Specifically, Sim concluded that “[s]caling the physical thickness of the HfO₂ dielectric to below 20Å [2 nm] causes less charge trapping and higher mobility.” (TSMC-1024, 221.)

Wang discloses use of HfO₂ as a high-k gate dielectric (TSMC-1012, ¶12), the same film studied in Sim. A POSITA would have been motivated to adopt Sim’s solution of forming a gate insulating film with a thickness of 20Å (2 nm) or less in the combined devices of Matsumoto (first/fourth embodiments) and Wang. (TSMC-1003, ¶¶167-69.) Accordingly, because the thickness of the high-k film is smaller under sidewall 8 than under the gate electrode 7, the combination of Matsumoto (first/fourth embodiments), Wang, and Sim discloses “*each side*

portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less” [11]. (TSMC-1003, ¶166.)

Sim expressly motivates the combination, finding that reducing the thickness of HfO₂ to below 20Å enhances mobility and reduces charge trapping, key issues in ensuring the performance and scalability of semiconductor devices. (TSMC-1024, 221; TSMC-1003, ¶168.) Sim’s teachings are consistent with Wang’s goal of using a thickness of “preferably less than about 50 Å to maintain low gate leakage and thin equivalent oxide thickness (EOT).” (TSMC-1012, ¶26.)

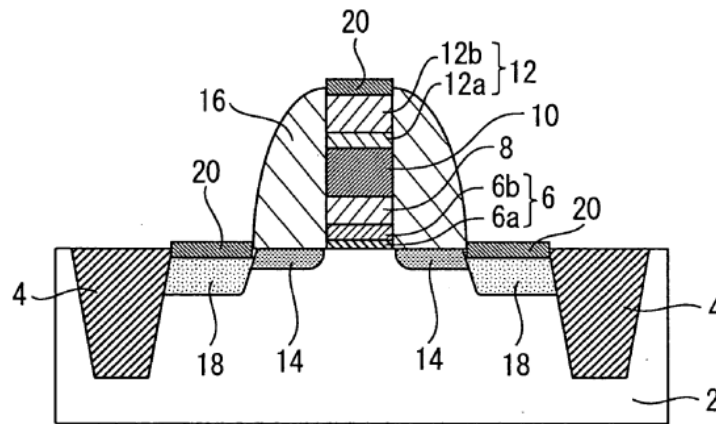
Additionally, the combination is nothing more than use of a known technique (Sim’s HfO₂ dielectric layer with less than 20Å thickness) to improve similar devices in the same way for the above reasons. *KSR*, 550 U.S. at 416-17; TSMC-1003, ¶169. A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable because Sim uses a well-known process, atomic layer deposition (ALD), for fabricating high-k films. (TSMC-1024, 218; TSMC-1003, ¶169.)

VIII. GROUND 4: Matsumoto-Mutou Combination Renders Claims 2-3 Obvious.

Should an argument be made the combination of Matsumoto and Wang fails to render claims 2-3 obvious, Mutou also explicitly describes a “*buffer insulating film*,” and the Matsumoto-Mutou combination renders claims 2-3 obvious.

A. Mutou

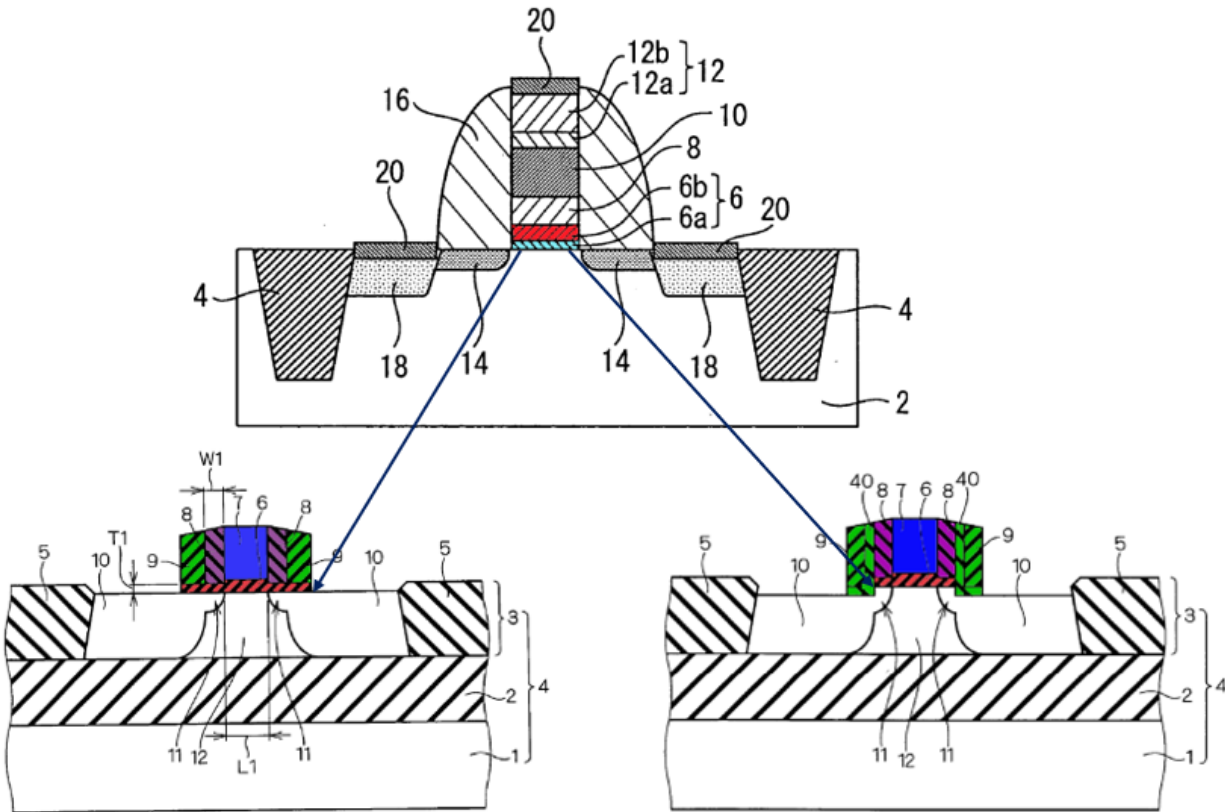
Mutou's device includes silicon substrate 2 and a gate stack comprising interfacial layer 6a, high-k dielectric film 6b, and a multilayer gate electrode. (TSMC-1019, ¶¶40-41, 44, Figure 1 (below).) Mutou and Matsumoto are in the same field as the '764 patent, "a semiconductor device and a method for fabricating." (TSMC-1001, 1:15-16; TSMC-1009, ¶2; TSMC-1019, Abstract, ¶¶2, 4; TSMC-1003, ¶171.)



Mutou, Figure 1

B. Motivation to Combine

A POSITA would have been motivated to integrate Mutou's underlying interfacial layer 6a ("*buffer insulating film*") (shaded aqua) under Matsumoto's high-k dielectric (shaded red) in the first embodiment (Figure 1) and fourth embodiment (Figure 22) devices, as shown below. (TSMC-1003, ¶173.)



**Mutou, Figure 1 (top);
Matsumoto, Figures 1 (left), 22 (right)**

Mutou expressly motivates the combination, teaching “[t]he underlying interfacial layer 6a is acted to inhibit interfacial reaction between the silicon substrate 2 and the high-k dielectric film 6b.” (TSMC-1019, ¶42.) Inhibiting such reactions between the substrate and the high-k film decreases degradation of the high-k film and, thus, improves performance of the device. (TSMC-1003, ¶176; TSMC-1001, 12:9-18 (by using a buffer insulating film, “deterioration of an interface between a substrate and a gate insulating film can be suppressed”).) This furthers the Matsumoto’s goal “to provide a semiconductor device which achieves

reductions in malfunctions and operating characteristic variations.” (TSMC-1009, ¶13.) Based on these disclosures, a POSITA would have been motivated to make the above combination to inhibit interfacial reaction between the substrate and the high-k film and improve performance of Matsumoto’s devices. (TSMC-1003, ¶176.)

The above combination is nothing more than use of a known technique (Mutou’s underlying interfacial layer) to improve similar devices in the same way for the above reasons. *KSR*, 550 U.S. at 416-17; TSMC-1003, ¶177. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable because Mutou uses conventional processes to form the underlying interfacial layer and deposit the high-k gate insulating film on top. (TSMC-1019, ¶¶53-54; TSMC-1009, ¶107; TSMC-1003, ¶¶178-80.)

C. Claims 2-3

Mutou’s interfacial layer 6a is formed on the silicon substrate 2 and high-k dielectric film 6b is formed on interfacial layer 6a. (TSMC-1019, ¶41.) Mutou’s interfacial layer 6a, as used in Matsumoto’s first and fourth embodiments, is “*a buffer insulating film.*” (TSMC-1003, ¶175.) Underlying interfacial layer 6a may be, “for example, a SiO₂ film, a Si₃N₄ film, or a SiON film” (TSMC-1019, ¶42.)

Thus, the combination of Matsumoto (first/fourth embodiments) and Mutou discloses “a buffer insulating film between the substrate and the high dielectric constant gate insulating film” [2] where “the buffer insulating film is a silicon oxide film” [3]. (TSMC-1003, ¶175.)

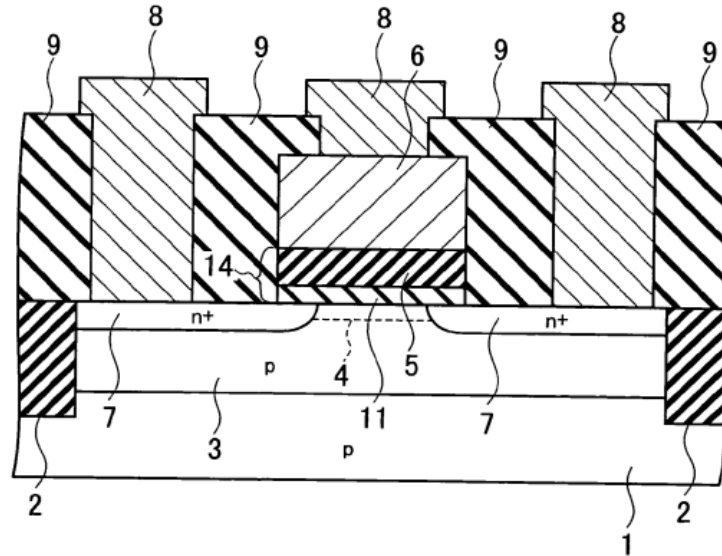
IX. GROUND 5: Matsumoto-Ono Combination Renders Claims 6, 10, 12, and 13 Obvious.

Matsumoto’s first and fourth embodiment devices do not expressly disclose the high-k gate insulating film “includes a notch at a side end portion” [10], or the high-k film’s side surface “is located at a predetermined distance from a side end surface of the first insulating sidewall toward the gate electrode” [12] or “is located at a predetermined distance from a side end surface of the gate electrode toward the first insulating sidewall” [13]. Ono teaches these features, and the Matsumoto-Ono combination renders claims 6, 10, 12, and 13 obvious.

A. Ono

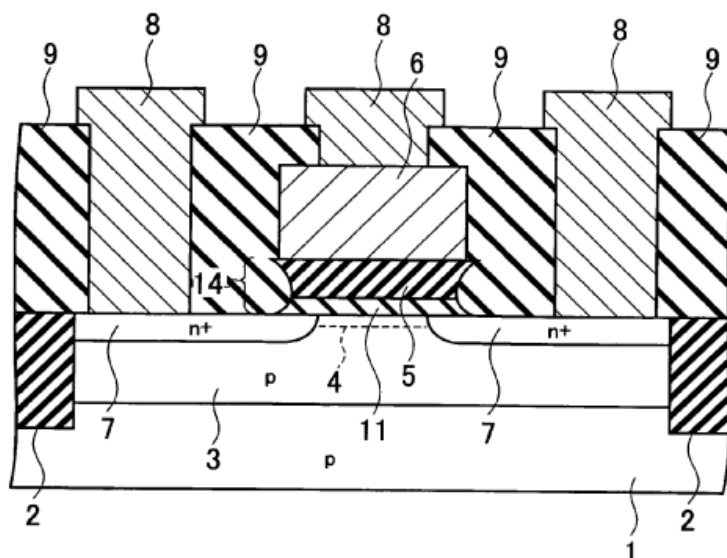
Ono’s second embodiment FET includes a gate stack comprising gate insulator film 5 “made of a metal oxide” and gate insulator film 11 “made of a metal oxide with a higher dielectric constant than the gate insulator film 5.” (TSMC-1013, ¶207, Figure 77.) Gate insulator film 5 is made of a “HfO₂ film.” (TSMC-1013, ¶209.) Gate electrode 6 is formed on gate insulator film 5 and can have gate sidewalls. (TSMC-1013, ¶¶207, 181, 210, Figure 77; TSMC-1003, ¶¶182-84.) Ono and Matsumoto are in the same field as the ’764 patent. (TSMC-

1001, 1:15-16; TSMC-1009, ¶2; TSMC-1013, Abstract, ¶¶3-7; TSMC-1003, ¶182.)



Ono, Figure 77

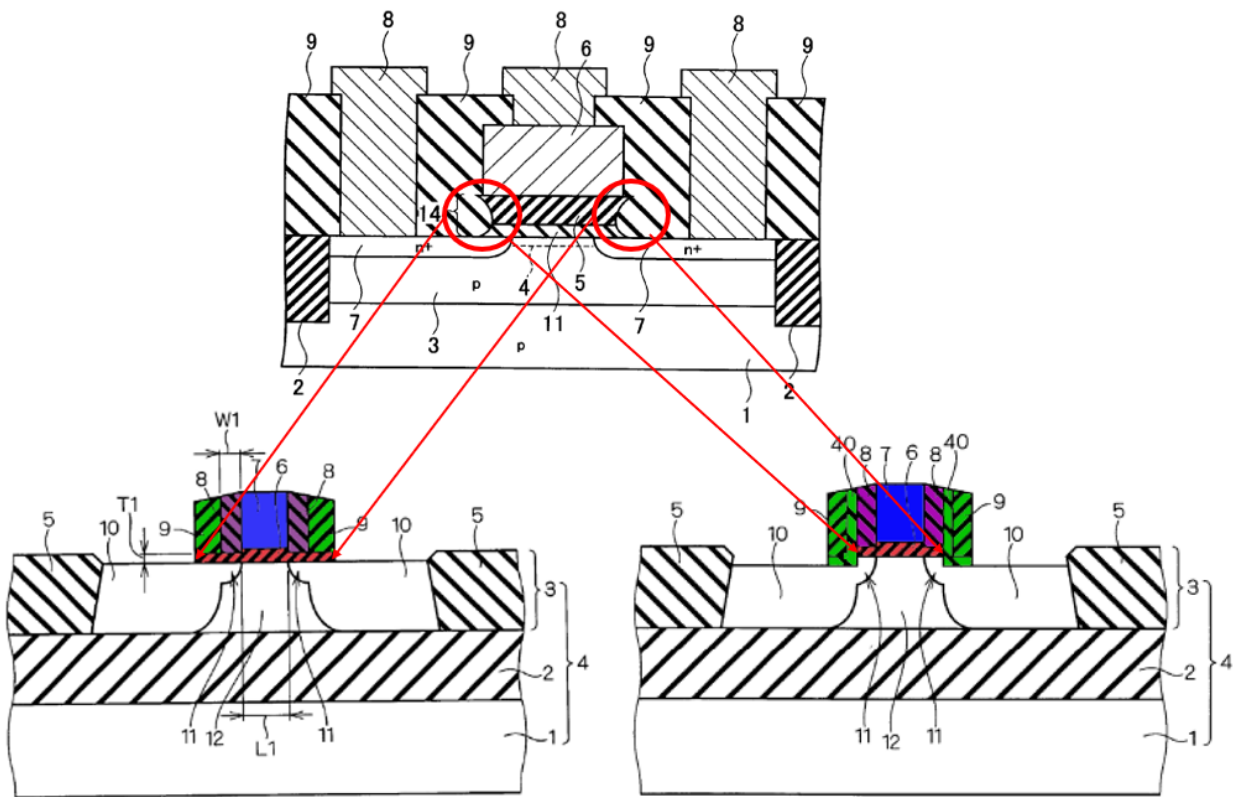
Ono discloses a modification of its second embodiment device where the side end portions of its gate insulating film “may curve.” (TSMC-1013, ¶216.) Ono discloses numerous examples of such curved end portions (Figures 104-23). (*Id.*) Petitioner focuses its analysis on the structure depicted in Figure 108 (reproduced below), although other structures are equally applicable.



Ono, Figure 108

B. Motivation to Combine

A POSITA would have been motivated to apply Ono's teaching of curving the end portion of a gate insulating film to Matsumoto's first and fourth embodiments, as shown below. (TSMC-1003, ¶¶190, 192-95.) Thus, in the combination, the side ends of Matsumoto's gate insulating film have a semicircular shape, as taught by Ono.



**Ono, Figure 108 (top);
Matsumoto, Figures 1 (left), 22 (right)**

Ono expressly suggests the combination, teaching that using curved side surfaces for the gate insulating film “reduc[es] the scattering of carriers as well as enhanc[es] the controllability of the gate electrode with respect to the potential of the channel region” and therefore provides “an advantage of optimization.” (TSMC-1013, ¶216, ¶200 (noting, for first embodiment, by using curved side surfaces, “the electrical capacitance between the gate electrode 6 and the source/drain regions 7 may be adjusted,” resulting in “an advantage of optimization”). A POSITA would have been further motivated to curve the end of Matsumoto’s gate insulating film to optimize parasitic resistance and parasitic

capacitance, improving device performance. (TSMC-1003, ¶194; TSMC-1040, ¶108; §IV.B.2.)

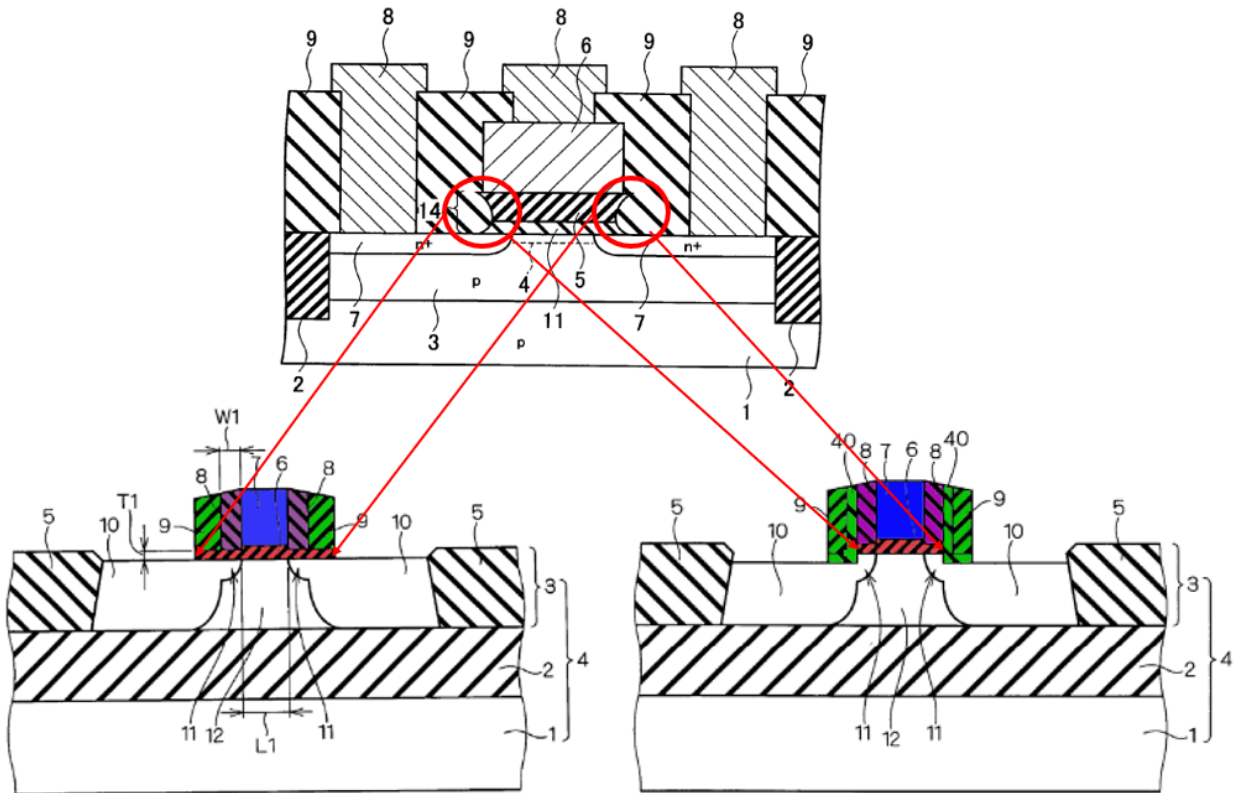
The Matsumoto-Ono combination is merely the application of a known technique (Ono’s curved film ends) to improve similar devices in the same way for the above reasons. *KSR*, 550 U.S. at 416-17; TSMC-1003, ¶195. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable. (TSMC-1003, ¶195.) Matsumoto and Ono both use high-k gate insulating films that extend under the gate electrode and the insulating sidewall, a concept well-known before the ’764 patent. (§§IV.B.2.b, IV.D.2, V.B.5, IX.A.) And both form their high-k dielectrics using conventional techniques. (TSMC-1009, ¶114; TSMC-1013, ¶167; TSMC-1003, ¶195.)

C. Claim 10

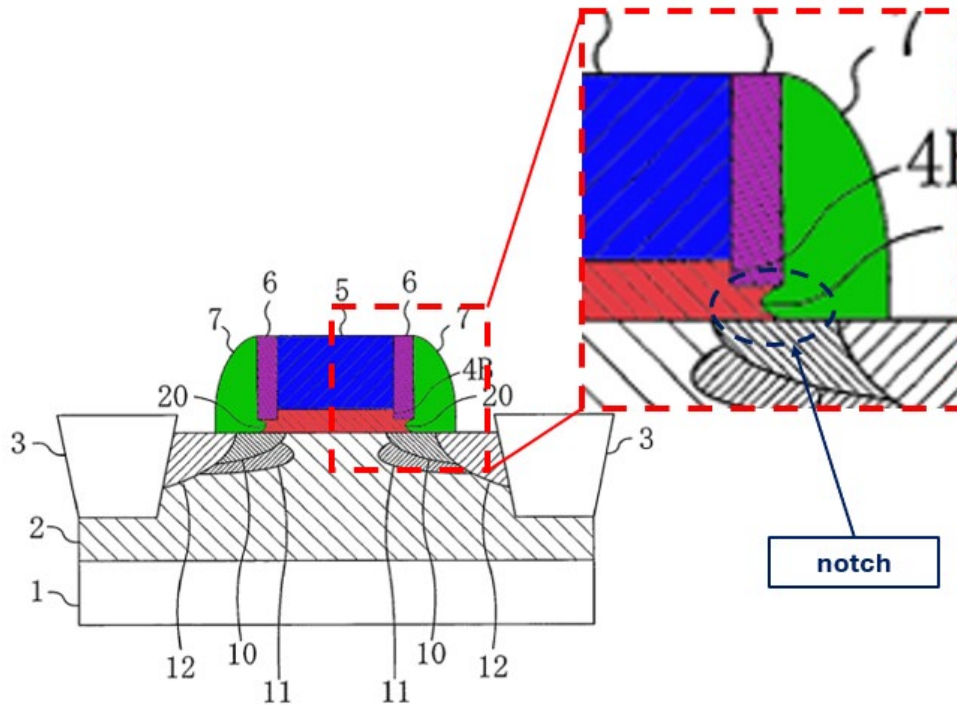
The combination of Matsumoto (first/fourth embodiments) and Ono discloses “*the high dielectric constant gate insulating film includes a notch at a side end portion*” [10]. (TSMC-1003, ¶¶190-95.)

In the devices of the Matsumoto-Ono combination, the end portion of Matsumoto’s gate insulating film has a semicircular shape under the sidewall, as taught by Ono in, e.g., Figure 108. Consistent with the ’764 patent’s disclosure, the semicircular shape of the gate insulating film’s side end in the combination

discloses “a notch.” (E.g., TSMC-1001, 8:35-40 (referring to notch 20 of Figure 7), Figure 7 (depicting notch 20 having a semicircular shape); TSMC-1003, ¶191.)



**Ono, Figure 108 (top);
Matsumoto, Figures 1 (left), 22 (right)**



'764 Patent, Figure 7 with enlargement

D. Claims 12-13

Additionally, in the combination of Matsumoto's fourth embodiment (Figure 22) and Ono, when the semicircular notch is applied at each side end of Matsumoto's gate insulating film 6 located under the first insulating sidewall film 8, the end of the gate insulating film no longer extends completely under the first insulating sidewall. The notch's semicircular shape (as taught by Ono) and the distance which the semicircular shape extends inward toward the gate electrode are set by specific process parameters. (TSMC-1003, ¶196.) Accordingly, in the combination of Matsumoto's fourth embodiment and Ono, the gate insulating film's side surface is "*located at a predetermined distance from a side end surface*

of the first insulating sidewall toward the gate electrode” [12] and “located at a predetermined distance from a side end surface of the gate electrode toward the first insulating sidewall” [13], consistent with the ’764 patent’s disclosure.

(TSMC-1001, 21:26-30 (“side surface ... may be located at a predetermined distance from a side end surface of the sidewall 7 or the offset sidewall 6 toward the gate electrode 5”); TSMC-1003, ¶196.)

E. Claim 6

The combination of Matsumoto (first/fourth embodiments) and Ono further discloses “*the high dielectric constant gate insulating film is formed of a Hf based oxide*” [6]. (TSMC-1003, ¶¶187-89.) Ono’s gate insulator film 5 is made of a “HfO₂ film.” (TSMC-1013, ¶209.) As discussed above in §VI.C, a POSITA would have been motivated to use a Hf-based oxide as a gate insulating layer as taught by Ono in Matsumoto’s first and fourth embodiments. (TSMC-1003, ¶188.)

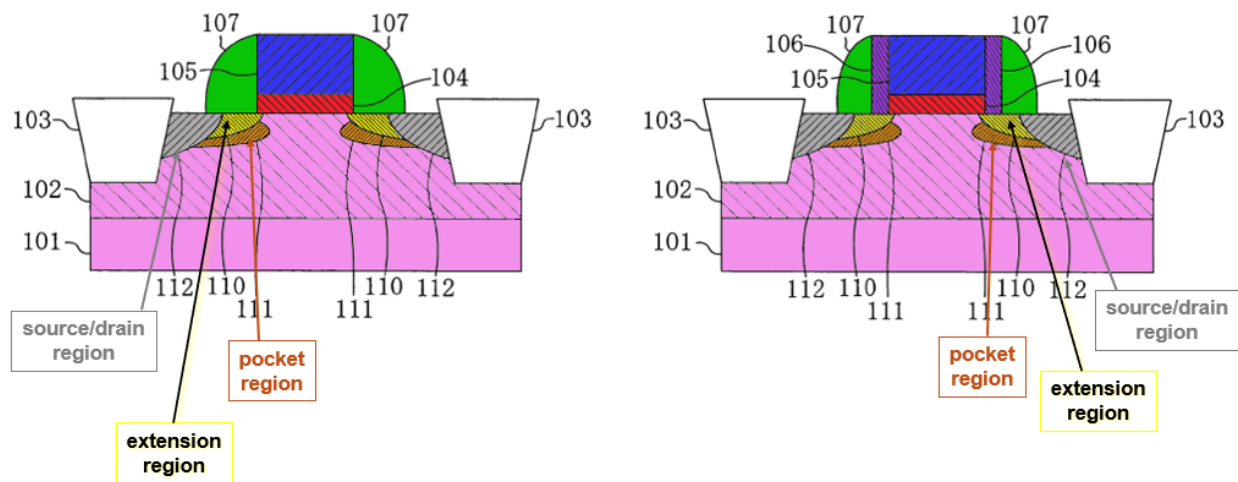
X. GROUND 6: Matsumoto-Rodder Combination Renders Claims 8-9 Obvious.

Claims 8-9 recite features that were common in semiconductor devices prior to the ’764 patent: “*extension region[s]*”, “*pocket region[s]*”, and “*source/drain regions.*” The ’764 patent admits this fact, presenting the claimed subject matter almost verbatim in its background section when describing two prior art devices:

A pocket region 111 [shaded orange] is formed in part of the well 102 located under the extension region 110 [shaded yellow]. Source/drain

regions 112 [shaded gray] are formed so that each of the source/drain regions 112 is provided in parts of the well 102 located at the external side to the extension region 110 and the pocket region 111 when viewed from the gate electrode 105.

(TSMC-1001, 1:45-51, Figures 16A-16B (below).) Matsumoto alone, in view of AAPA, renders claims 8-9 obvious. Rodder also discloses these features.

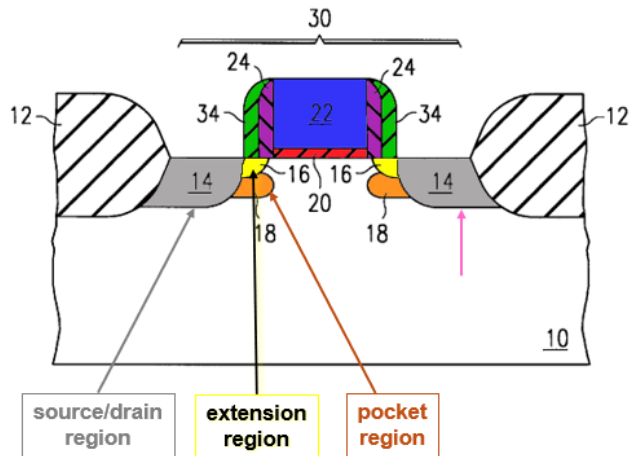


'764 Patent, Figures 16A (left), 16B (right) [AAPA]

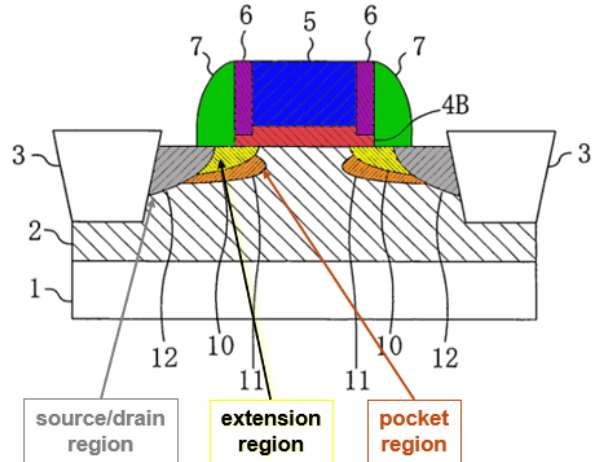
A. Rodder

Rodder describes a transistor substrate having highly doped regions (n-type) 16 (shaded yellow) “commonly referred to as drain extensions” and “[p]ocket regions 18 [shaded orange] ... doped oppositely to drain extension regions 16.” (TSMC-1023, 2:61-3:1, Figure 1 (below-left).) Rodder’s substrate also includes “deep source/drain regions 14 [shaded gray].” (TSMC-1023, 2:62-63.) As shown below, Rodder’s Figure 1 has the same structure, including placement of the extension, pocket, and source/drain regions, as ’764 patent-Figure 2. (TSMC-1003,

¶201; compare TSMC-1001, Figures 16A-B.) Rodder and Matsumoto are in the same field as the '764 patent. (TSMC-1001, 1:15-16; TSMC-1009, ¶2; TSMC-1023, Abstract; TSMC-1003, ¶ 200.)



Rodder, Figure 1

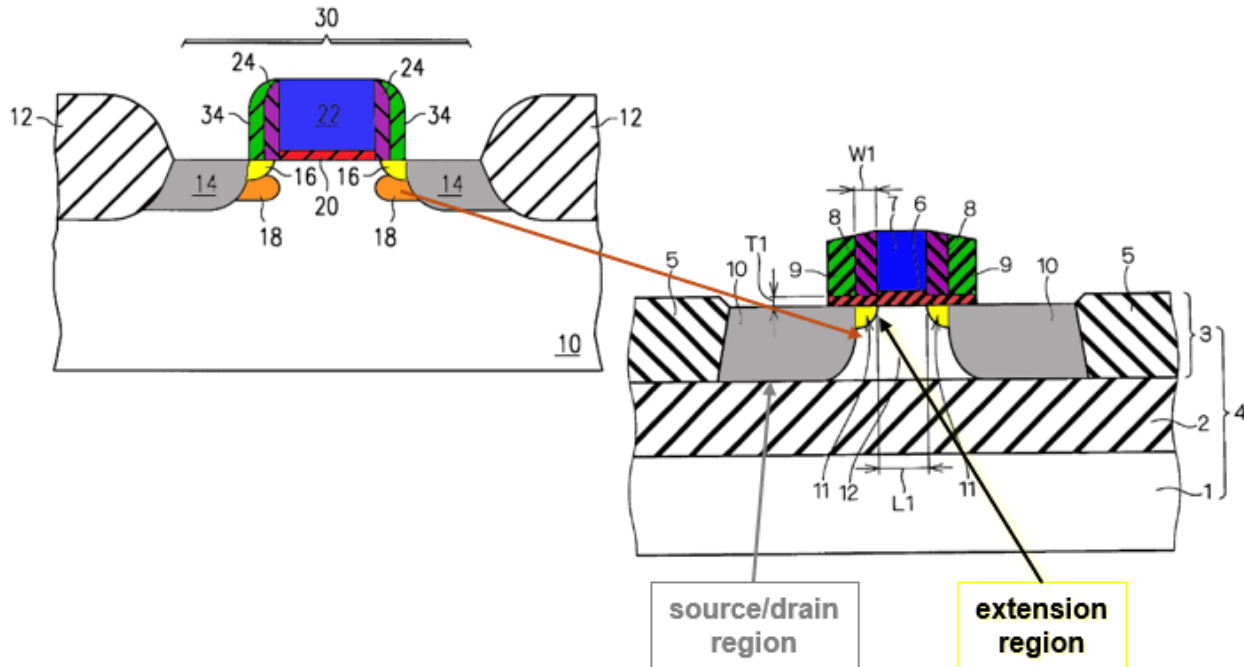


'764 Patent, Figure 2

B. Combination Overview

Matsumoto's first embodiment device includes extensions 11 (shaded yellow) located under sidewall film 8 (*"first insulating sidewall"*) "in the upper surface of the silicon layer 3" (part of the *"active region"* of the substrate). (TSMC-1009, ¶111 (describing formation of extensions 11), Figures 7-8 (showing intermediate structure having extensions 11), Figure 10 (showing intermediate structure showing extensions under sidewall films 8 and 9), Figure 1 (below); §V.B.2.) Matsumoto's substrate further includes source/drain regions (shaded grey) formed in silicon layer 3 after formation of sidewall film 9 (*"second*

insulating sidewall”). (TSMC-1009, ¶¶115-16 (describing formation of source/drain regions 10).)



Rodder, Figure 1 (left); Matsumoto, Figure 1 (right)

Matsumoto further discloses that, for an NMOS device, p-type ions are implanted in the pocket region, and n-type ions are implanted in the extensions and the source/drain regions. (TSMC-1009, ¶¶111, 115.) Similarly, for a PMOS device, n-type ions are implanted in the pocket region, and p-type ions are implanted in the extensions and the source/drain regions. (TSMC-1009, ¶¶113, 116.) Additionally, although Matsumoto does not explicitly show the extension region extending beyond sidewall film 8, a POSITA would have understood the extension regions remain at least partially under film 9 after creation of the source/drain regions, as

admitted by the '764 patent and also taught by Rodder. (TSMC-1001, 1:45-51; TSMC-1023, 2:61-3:1; TSMC-1003, ¶¶204-05; TSMC-1038, 463.) Matsumoto therefore teaches “*an extension region of a first conductivity type is formed in each of parts of the active region located under the first insulating sidewall and the second insulating sidewall*” [8A] and “*each of source/drain regions of a first conductivity type is formed in part of the active region ...*” [9]. (TSMC-1003, ¶¶204-05.) Matsumoto, however, does not specify the location of its pocket regions.

Rodder describes “*pocket regions*” placed under extensions regions. (TSMC-1023, 4:35-36.) Rodder also discloses its source/drain regions are located external to the extensions and pocket regions, when viewed from the gate electrode. (*E.g.*, TSMC-1023, Figure 1.) A POSITA would have been motivated to combine Rodder’s teaching regarding the placement of “*pocket regions*” with Matsumoto’s first embodiment device, as shown above. (TSMC-1003, ¶¶207-08.)

A POSITA would have been motivated to make the above combination to obtain the well-understood benefits of “*pocket regions*” and their locations described by Rodder, such as “reduc[ing] the threshold voltage (V_t) rolloff, reduc[ing] the nominal V_t , and thus improv[ing] the nominal drive current.” (TSMC-1023, 1:22-25; TSMC-1003, ¶209; TSMC-1038, 463-64 (describing pocket implants which “reduce short-channel effects by shielding the channel from

the deep source/drain diffusion”).) Matsumoto also corroborates these benefits noting that pocket regions “suppress a short channel effect resulting from device size reduction.” (TSMC-1009, ¶111.)

The combination is also nothing more than use of a known technique (Rodder’s formation of pocket regions below extension regions and outside of source/drain regions) to improve similar devices in the same way for the above reasons. *KSR*, 550 U.S. at 416-17; TSMC-1003, ¶210. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable because both Matsumoto and Rodder use known ion implantation processes for forming doped regions, including pocket regions. (TSMC-1009, ¶¶111, 113; TSMC-1023, 4:21-62; TSMC-1038, 463-64 (describing techniques for forming pocket/halo implants); TSMC-1003, ¶210.)

C. Claims 8-9

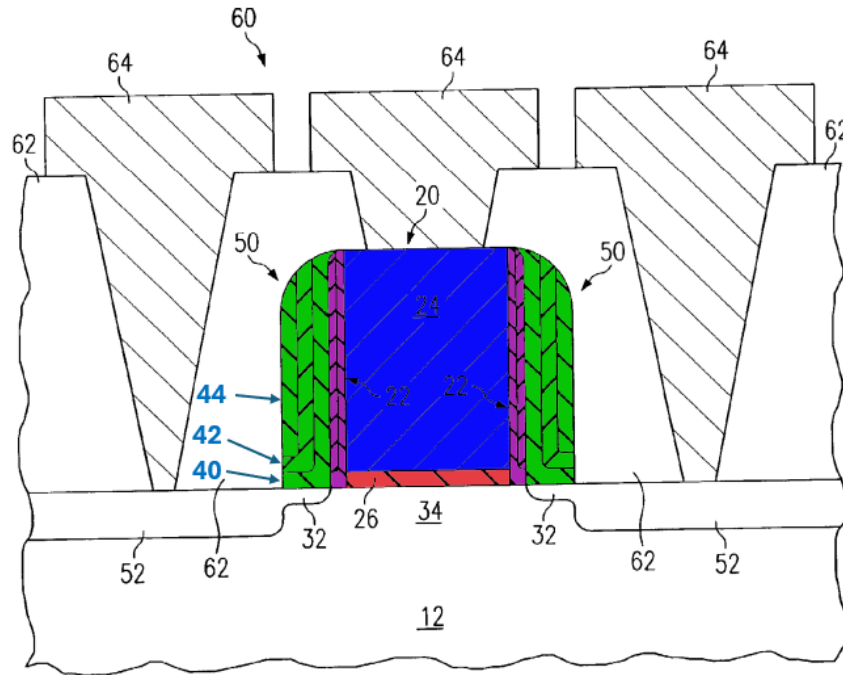
In the combination of Matsumoto and Rodder, Matsumoto’s pocket regions, which are of an opposite conductivity to the extensions and source/drain regions, are formed under the extensions such that the source/drain regions are external to the pocket regions, as taught by Rodder. (TSMC-1009, ¶¶111, 113, 115-16.) Accordingly, the combination of Matsumoto’s first embodiment and Rodder discloses “*a pocket region of a second conductivity type is formed in part of the active region located under the extension region*” [8B] and “*each of source/drain*

regions ... located in an external side to the extension region and the pocket region when viewed from the gate electrode” [9]. (TSMC-1003, ¶¶207-08.) For this reason, and the reasons discussed above, the combination of Matsumoto (first embodiment) and Rodder renders claims 8-9 obvious.

XI. GROUND 7: Matsumoto-Bu Combination Renders Claim 15 Obvious.

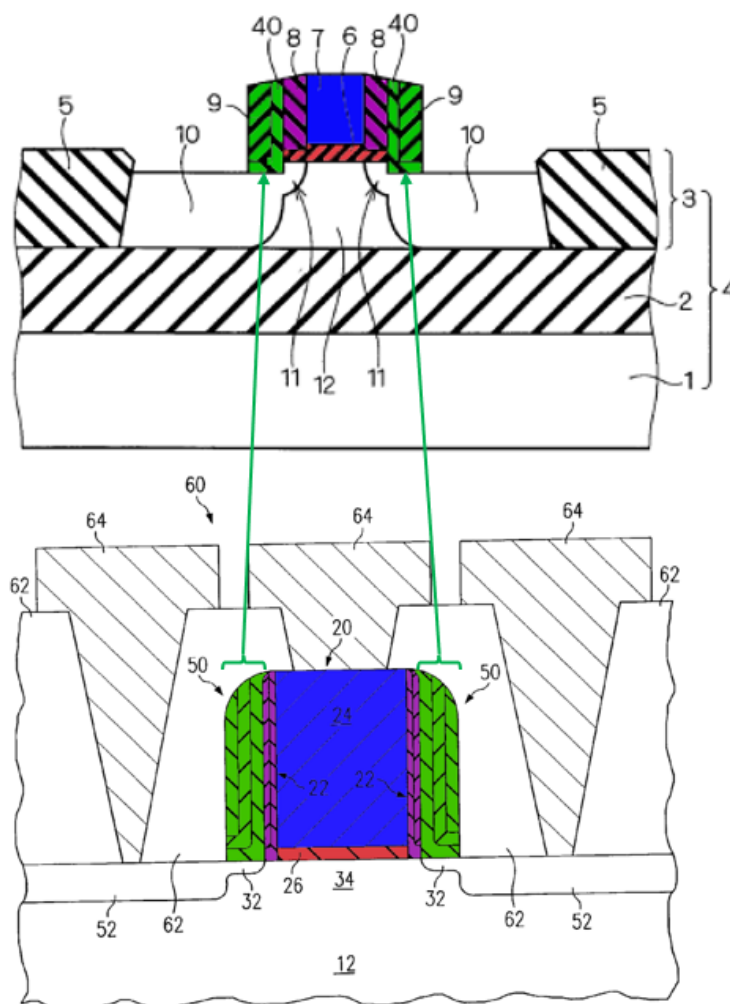
Should PO argue Matsumoto’s fails to render claim 15 obvious, Bu discloses an outer sidewall with “*a triple layer structure*” [15]. (TSMC-1003, ¶¶211-15.)

Bu’s transistor includes gate stack 20, comprising gate conductor 24 (shaded blue) and gate insulator 26 (shaded red), and sidewall spacers 22 (shaded purple). (TSMC-1025, ¶42, Figure 1E (below).) Bu’s transistor further includes an outer sidewall formed on sidewall spacers 22 having a triple-layer ONO structure: first sidewall-forming layer 40, comprised of “**oxide**”; second sidewall-forming layer 42, comprised of “**nitride**”; and third sidewall-forming layer 44, comprised of “**oxide**”. (TSMC-1025, ¶¶26-27, 30, 35, 43, Figure 1E.) Bu and Matsumoto are in the same field as the ’764 patent. (TSMC-1001, 1:15-16; TSMC-1009, ¶2; TSMC-1025, Abstract; TSMC-1003, ¶212.)



Bu, Figure 1E

Matsumoto's fourth embodiment includes inner "first sidewall" 8 and an outer "second sidewall" comprised of oxide film 40 and nitride film 9. A POSITA would have been motivated to use Bu's triple-layer ONO sidewall structure with Matsumoto's fourth embodiment device. Specifically, a POSITA would have been motivated to add an additional oxide layer to Matsumoto's second sidewall (shaded green in Figure 22), as taught by Bu. (TSMC-1003, ¶213.) The resulting device of the combination of Matsumoto and Bu discloses that "*the second insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film*" [15]. (*Id.*)



Matsumoto, Figure 22 (top); Bu, Figure 1E (bottom)

A POSITA would have specifically integrated Bu’s triple-layer ONO sidewall structure teachings into Matsumoto’s device given the well-known benefits of ONO structures, including, for example, allowing independent control of spacer dimensions to optimize device scaling. (TSMC-1003, ¶¶214; TSMC-1050, ¶¶5-6, Figure 4.) Bu further notes the benefits of using different materials in the sidewall structure: “film properties of sidewall-forming layers 40 and 42 may minimize dopant loss from source drain extension region 32 to first sidewall-

forming layer 40. Accordingly, parasitic resistance may be lowered.” (TSMC-1025, ¶26.) A POSITA would have been motivated to make the combination to obtain these benefits and improve device performance and reliability. (TSMC-1003, ¶214.)

The Matsumoto-Bu combination represents nothing more than use of a known technique (Bu’s triple-layer sidewall) to improve similar devices in the same manner for the above reasons. *KSR*, 550 U.S. at 416-17; TSMC-1003, ¶215. A POSITA would have had a reasonable expectation of success in the combining these references, leading to predictable results, because both Matsumoto and Bu disclose forming sidewall layers using standard deposition and etching techniques, making the application of Bu’s triple layer structure to Matsumoto’s design straightforward. (TSMC-1009, ¶¶139, 162, Figure 29; TSMC-1025, ¶¶27, 30, 35, 38; TSMC-1003, ¶215.)

XII. GROUND 8: Matsumoto-Wilk Combination Renders Claims 18-19 Obvious.

Should PO argue Matsumoto’s disclosure as informed by knowledge of a POSITA and AAPA fails to teach claims 18-19, Wilk, “High-k Gate Dielectrics: Current Status and Materials Properties considerations”, discloses the express teaching.

Wilk explores the properties of materials “under consideration” in 2001 “as potential replacements for SiO₂ as the gate dielectric material for sub-0.1 μm CMOS technology.” (TSMC-1018, Abstract.) Wilk discloses the following table of relevant properties, including dielectric constants, for various materials:

TABLE I. Comparison of relevant properties for high- κ candidates.

Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si	Crystal structure(s)
SiO ₂	3.9	8.9	3.2	Amorphous
Si ₃ N ₄	7	5.1	2	Amorphous
Al ₂ O ₃	9	8.7	2.8 ^a	Amorphous
Y ₂ O ₃	15	5.6	2.3 ^a	Cubic
La ₂ O ₃	30	4.3	2.3 ^a	Hexagonal, cubic
Ta ₂ O ₅	26	4.5	1–1.5	Orthorhombic
TiO ₂	80	3.5	1.2	Tetrag. ^c (rutile, anatase)
HfO ₂	25	5.7	1.5 ^a	Mono. ^b , tetrag. ^c , cubic
ZrO ₂	25	7.8	1.4 ^a	Mono. ^b , tetrag. ^c , cubic

^aCalculated by Robertson (See Ref. 153).

^bMono.=monoclinic.

^cTetrag.=tetragonal.

Wilk, Table I

A POSITA would have been motivated to look to Wilk’s teachings to understand the properties of materials discussed in Matsumoto, for example, to ensure the gate insulating film had a sufficiently high dielectric constant. (TSMC-1003, ¶218.)

Wilk and Matsumoto are in the same field as the ’764 patent. (TSMC-1001, 1:15-16; TSMC-1009, ¶2; TSMC-1018, Abstract; TSMC-1003, ¶217.)

Matsumoto teaches use of “Ta₂O₅” as the gate insulating film. (TSMC-1009, ¶107.) Wilk discloses the dielectric constant for Ta₂O₅ is 26, which is greater

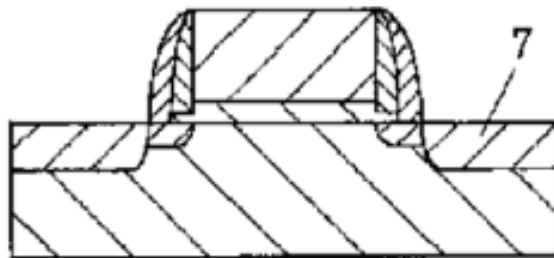
than 10. (TSMC-1018, Table I.) Matsumoto discloses second sidewall 9 (“*second insulating sidewall*”) is comprised of silicon nitride (Si_3N_4), which has a dielectric constant of 7. (TSMC-1009, ¶¶114, 139; TSMC-1018, Table I; TSMC-1052, Figure 4.)

Thus, in the devices of the Matsumoto-Wilk combination, “*the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more*” [18] and “*the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall*” [19]. (TSMC-1003, ¶¶219-20.)

XIII. GROUND 9: Kajiyama Anticipates Claims 1, 5, 16-17, and 21.

A. Kajiyama

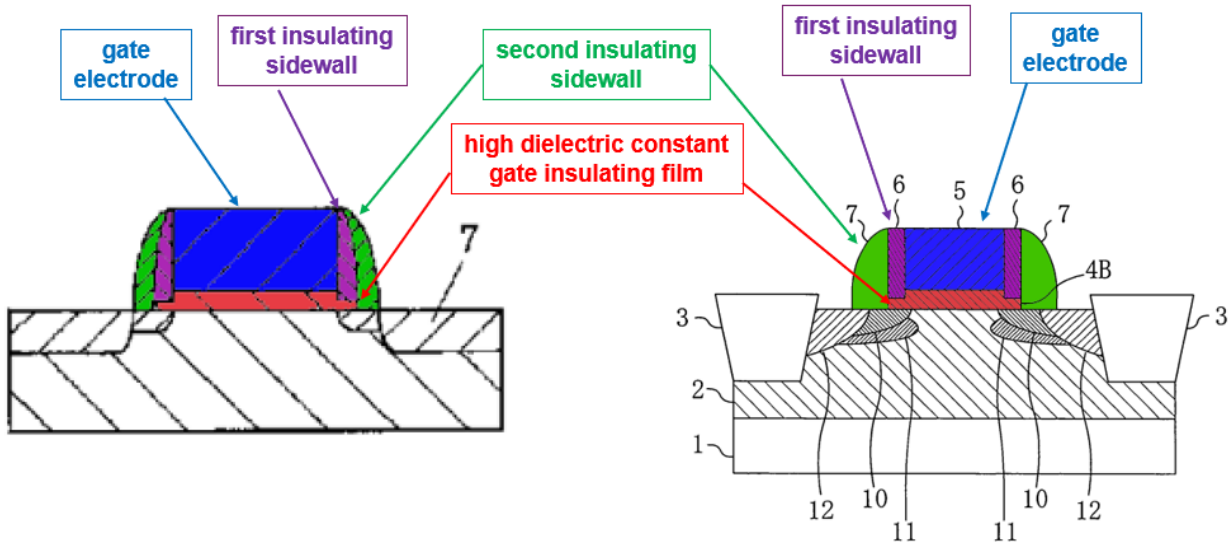
Kajiyama’s first embodiment FET includes a gate electrode with two sidewalls. A high-k gate insulating film extends from under the gate electrode to under only the first sidewall. (TSMC-1011, ¶¶1, 28, Figure 1(D) (below).)



Kajiyama, Figure 1(D)

B. Independent Claim 1

Kajiyama's first embodiment device anticipates claim 1, as illustrated by the side-by-side figures below.



Kajiyama, Figure 1(D)

'764 Patent, Figure 2

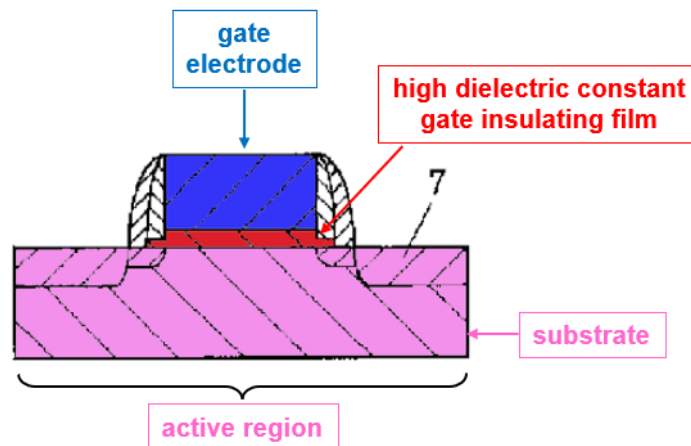
1. Preamble [1P]

Kajiyama discloses a “*semiconductor device*”: “present invention relates to semiconductor devices.” (TSMC-1011, ¶1; *see also* TSMC-1011, ¶27; TSMC-1003, ¶225.)

2. Limitations [1A]-[1B]

Kajiyama teaches “a *high dielectric constant gate insulating film formed on an active region in a substrate*” [1A] and “a *gate electrode formed on the high dielectric constant gate insulating film*” [1B]. (TSMC-1003, ¶¶226-31.)

Kajiyama's device has a "p-type Si **substrate** [shaded pink]" with an "element separation layer (not shown) on the Si substrate 1." (TSMC-1011, ¶¶28-29, Figure 1(D) (below).) Kajiyama's element separation layer is equivalent to the '764 patent's STI structures. (TSMC-1011, ¶¶5, 29; TSMC-1001, 7:30-47 (showing active region with source/drain regions surrounded by STI structures 3).) In Kajiyama, within the region defined by the element separation layer, an n-type LDD diffusion layer 4 is formed and then an n⁺ source drain diffusion layer 7 is formed. (TSMC-1011, ¶¶29, 32, Figures 1(A), 1(D).) The region defined by Kajiyama's element separation layer is "*an active region in a substrate.*" (TSMC-1003, ¶228.)



Kajiyama, Figure 1(D)

Kajiyama's "device comprises a gate insulating film [labeled 2 in Figure 1(A)] consisting of a high dielectric film¹² [shaded red] formed on a semiconductor substrate." (TSMC-1011, ¶¶14, 28, claim 1, Figure 1(D) (above).) The high-k film, formed on the substrate within the element separation layer, is therefore "*formed on an active region in a substrate.*" (TSMC-1011, ¶29; TSMC-1003, ¶¶229-30.)

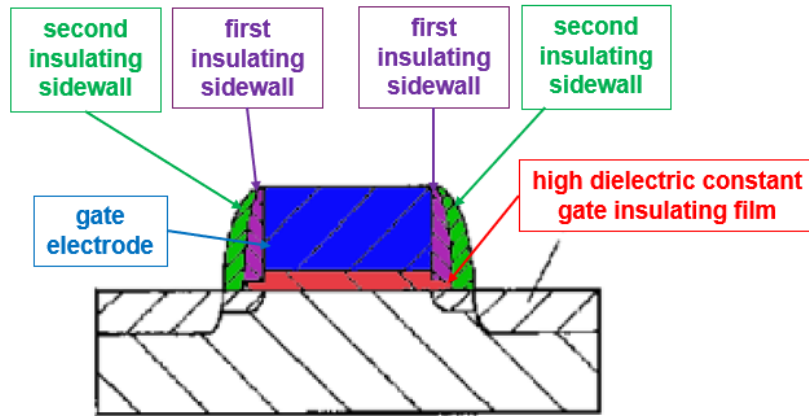
Gate electrode 3 (shaded blue) "consisting of a conductive film [is] formed on [the] gate insulating film." (TSMC-1011, ¶14; TSMC-1003, ¶231.)

3. Limitations [1C]-[1D]

Kajiyama's device includes "first sidewall [labeled 5 in Figure 1(B), shaded purple] consisting of a dielectric film formed on a sidewall of the gate electrode, and a second sidewall [labeled 6, shaded green] ... formed to cover the first sidewall." (TSMC-1011, ¶¶14, 28, Figure 1(D) (below).) First sidewall 5 "consist[s] of ZrO₂ film (**insulation** film)" and is therefore "*a first insulating sidewall formed on each side surface of the gate electrode*" [1C]. (TSMC-1011, ¶28; TSMC-1003, ¶¶233-34.) Second sidewall 6 is a silicon nitride film 6 (referred to as Si₃N₄ film) and is therefore "*a second insulating sidewall formed on said*

¹² Kajiyama also refers to high-k film 2 as "ZrO₂ film 2". (E.g., TSMC-1011, ¶29.)

each side surface of the gate electrode with the first insulating sidewall interposed therebetween” [1D]. (TSMC-1011, ¶28; TSMC-1003, ¶235.)

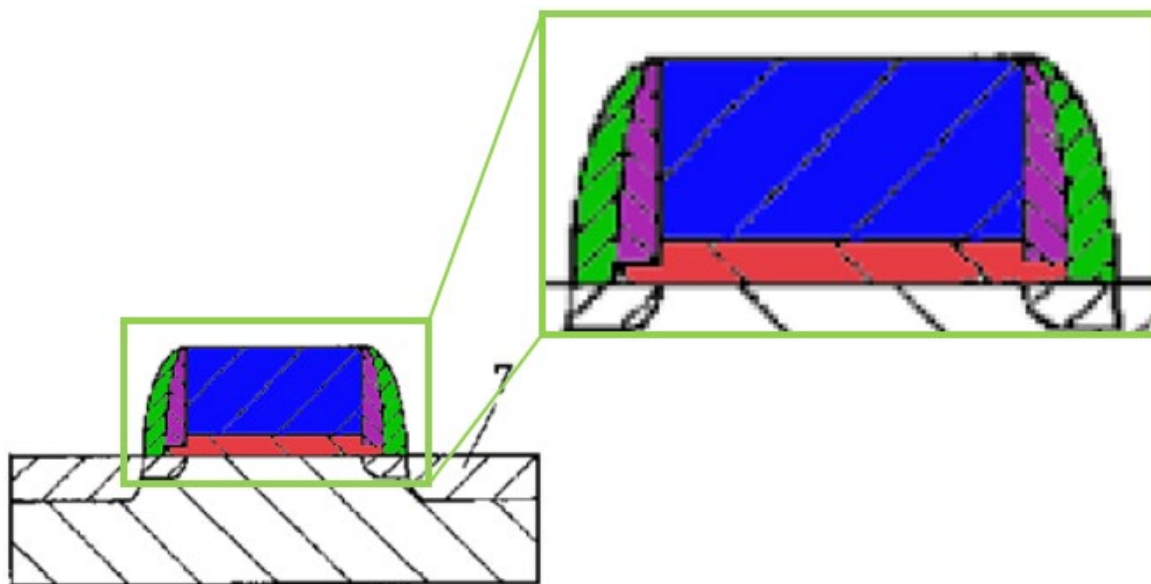


Kajiyama, Figure 1(D)

4. Limitations [1E]-[1F]

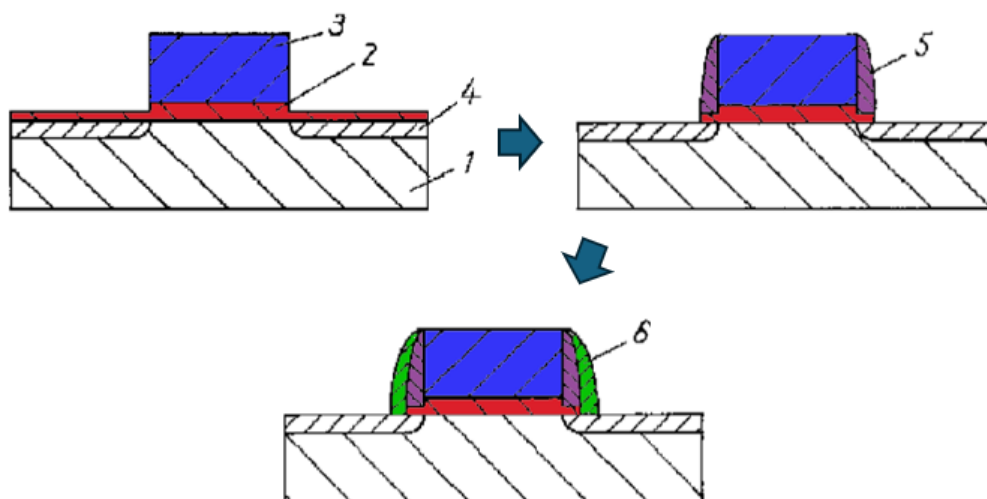
As shown in Kajiyama’s device and confirmed by the disclosed process, high-k film 2 (shaded red) is an uninterrupted layer (as evidenced by the absence of gaps) that extends from under the gate electrode to under first sidewall 5 (“*first insulating sidewall*”; shaded purple). The high-k film is thinner under sidewall 5 (“*first insulating sidewall*”) than it is under the gate electrode (shaded blue).

(TSMC-1003, ¶238; *Unified*, 2022 WL 500391, at *17.)



Kajiyama, Figure 1(D) with enlargement

Kajiyama's fabrication process confirms the Figure 1(D) structure. During fabrication, an n-type polySi film is deposited on high-k film 2 and etched "to form a gate electrode 3." (TSMC-1011, ¶29.) High-k film 2 "is also etched to reduce the film." (TSMC-1011, ¶29, Figure 1(A) (top-left).) As a result, the thickness of high dielectric constant film 2 is larger under the gate electrode than elsewhere. (TSMC-1003, ¶239.)



**Kajiyama, Figures 1(A) (above-left),
1(B) (above-right), 1(C) (bottom)**

First sidewall 5 (shaded purple) is then formed on the side of gate electrode 3 and over the thinner portion of the high-k film. (TSMC-1011, ¶30, Figure 1(B) (top-right).) The high-k film is then etched “to remove all.” (TSMC-1011, ¶30.) That is, the high-k film outside the outer edge of sidewall 5 is removed. (TSMC-1003, ¶241.) Next, second sidewall 6 (shaded green) is formed “to cover the first sidewall 5 [shaded purple] provided on the sidewall of the gate electrode 3 [shaded blue].” (TSMC-1011, ¶31, Figure 1(C) (bottom).) As shown above, a portion of the high-k film (shaded red) remains under the gate electrode and first sidewall 5 but does not extend under sidewall 6.

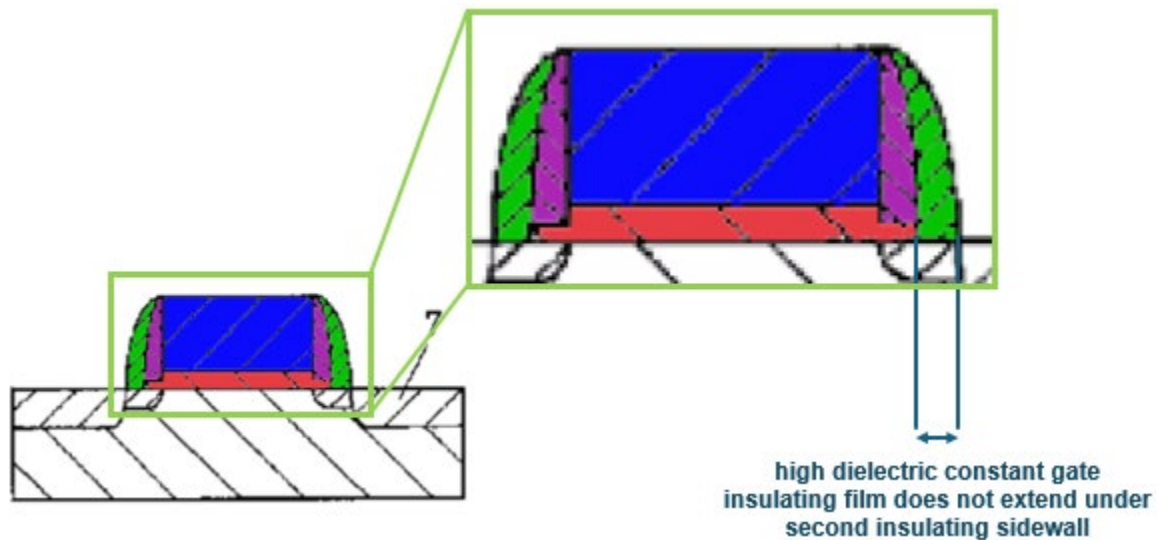
Thus, Kajiyama’s device teaches “*the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall*” [1E] and “*part of the high*

dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode” [1F]. (TSMC-1003, ¶¶236-41.)

C. Claim 5

Kajiyama teaches “*the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall*” [5]. (TSMC-1003, ¶¶242-44.)

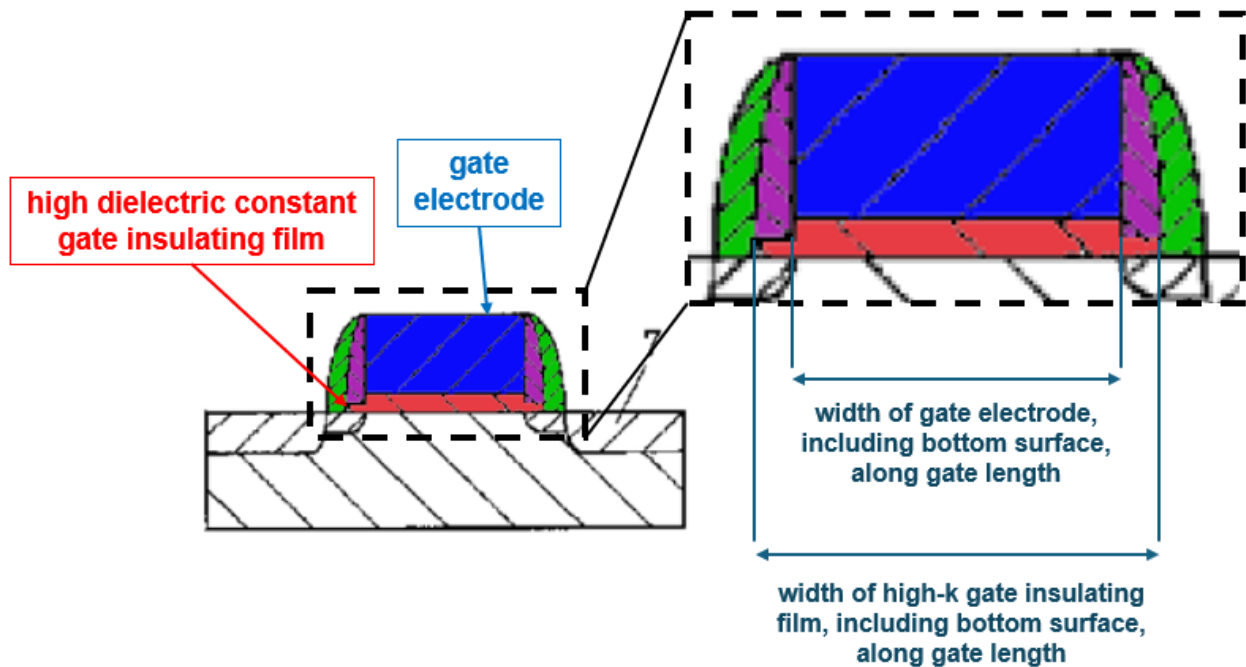
As shown in Figure 1(D) below, high-k dielectric film 2 (shaded red) remains only under the gate electrode 3 and the first sidewall 5—it is not located under sidewall 6 (“*the second insulating sidewall*”; shaded green). *Unified*, 2022 WL 500391, at *17. The fabrication process, discussed in §XIII.B.4, confirms the structure illustrated in Figure 1(D). (TSMC-1011, ¶¶30-31; TSMC-1003, ¶244.)



Kajiyama, Figure 1(D) with enlargement

D. Claims 16-17

High-k gate insulating film 2 in Kajiyama's first embodiment extends from under the gate to under the first insulating sidewall. (§XIII.B.4.) As illustrated in the figures below, along the gate length, the width of high-k gate insulating film 2 (shaded red), including the bottom surface of high-k gate insulating film 2, is larger than the width of the gate electrode 3 (shaded blue), including the bottom surface of the gate electrode 3. (TSMC-1003, ¶245.) Kajiyama anticipates claims 16-17.

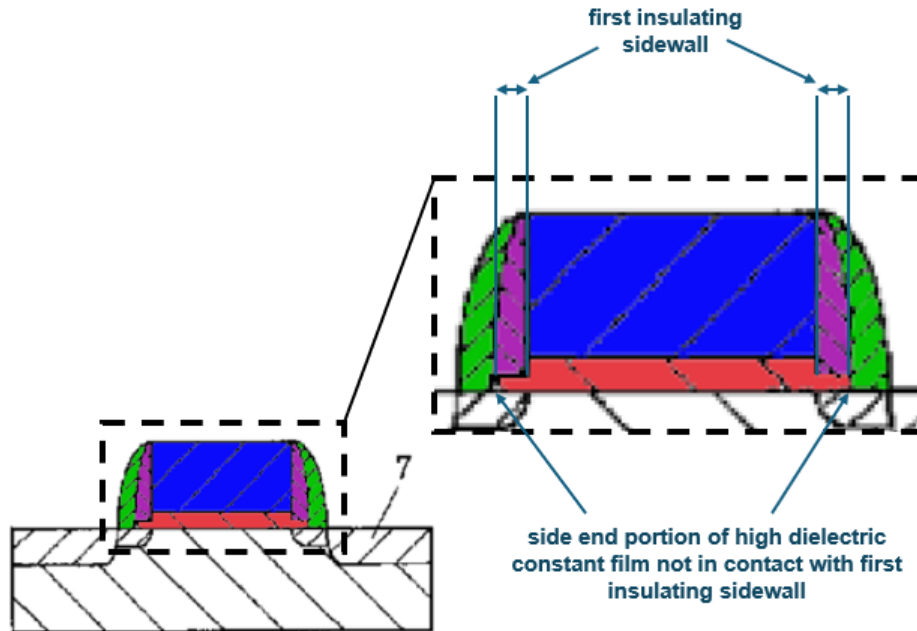


Kajiyama, Figure 1(D) with enlargement

E. Claim 21

As discussed in §XIII.B.4, Kajiyama's first embodiment device is manufactured such that gate insulating film 2 (shaded red) extends from beneath the gate electrode 3 (shaded blue) to under the first sidewall 5 (shaded purple) and

ends at the second sidewall 6 (shaded green). The side end portion of film 2 therefore is not in contact with sidewall 5. *Unified*, 2022 WL 500391, *17; TSMC-1003, ¶¶246-49. Kajiyama anticipates claim 21.



Kajiyama, Figure 1(D) with enlargement

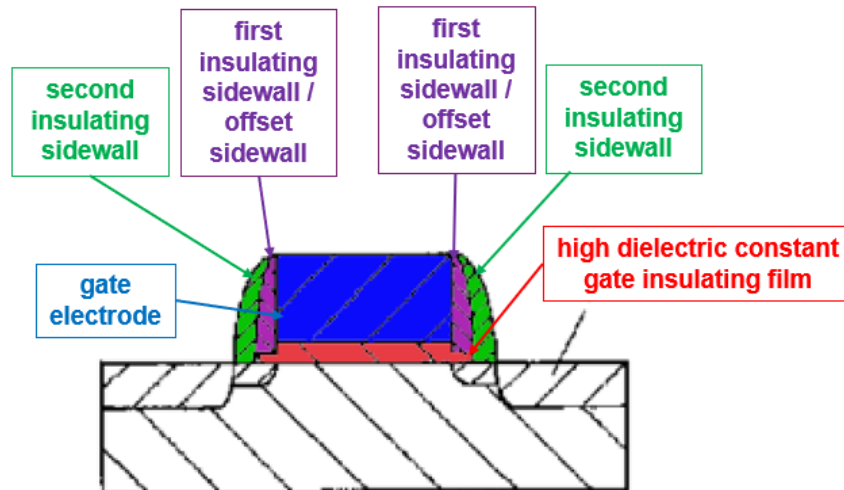
XIV. GROUND 10: Kajiyama Renders Claims 4, 6, and 18-20 Obvious.

A. Claim 4

Kajiyama renders obvious “*the first insulating sidewall is an offset sidewall*” [4]. (TSMC-1003, ¶250.)

As discussed in §XIII.B.3, in Kajiyama’s first embodiment, first sidewall 5 is the “*first insulating sidewall.*” While Kajiyama does not refer to first sidewall 5 as an offset sidewall, a POSITA would understand first sidewall 5, located between gate electrode 3 and second sidewall 6, is an offset sidewall. (TSMC-1003, ¶250;

TSMC-1034, 216-17, Figure 5-25.) This is also consistent with the '764 patent specification, which refers to an inner sidewall as an offset sidewall: “insulating sidewall 7 is formed on each side surface of the gate electrode 5 with an offset sidewall 6 interposed therebetween.” (TSMC-1001, 7:37-39, Figure 2.)



Kajiyama, Figure 1(D)

B. Claim 6

Kajiyama renders “*the high dielectric constant gate insulating film is formed of a Hf based oxide*” [6] obvious. (TSMC-1003, ¶251.)

Kajiyama discloses that, while the gate insulating film 2 in the first embodiment is a ZrO_2 film, “other high dielectric films, such as a HfO_2 film, a Ta_2O_5 film, or a Al_2O_3 film, can be used instead to obtain the effects of the invention.” (TSMC-1011, ¶45.) A POSITA would have been motivated to select HfO_2 as the high-k material for Kajiyama’s gate dielectric for the reasons discussed in §VI.C. (TSMC-1003, ¶251.)

C. Claims 18-19

Kajiyama renders claims 18-19 obvious. (TSMC-1003, ¶¶252-54.)

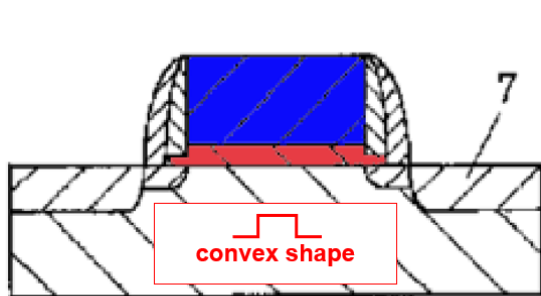
Kajiyama teaches that, in addition to ZrO_2 “other high dielectric films, such as a HfO_2 film, a Ta_2O_5 film, or a Al_2O_3 film, can be used instead to obtain the effects of the invention.” (TSMC-1011, ¶45.) ZrO_2 has a dielectric constant of 25, HfO_2 has a dielectric constant of 25, and Ta_2O_5 has a dielectric constant of 26, all of which are greater than 10. (TSMC-1018, Table I.) Further, Kajiyama discloses that the second sidewall 6 is comprised of silicon nitride (Si_3N_4), which has a dielectric constant of 7. (TSMC-1011, ¶28; TSMC-1018, Table I.) While Kajiyama itself does not expressly disclose the relative dielectric constants of the listed materials, the dielectric constant is a material property and, therefore, the dielectric constants for ZrO_2 , HfO_2 , Ta_2O_5 , and Si_3N_4 are necessarily present in Kajiyama, a fact that would have been known by a POSITA. (TSMC-1003, ¶254.)

D. Claim 20

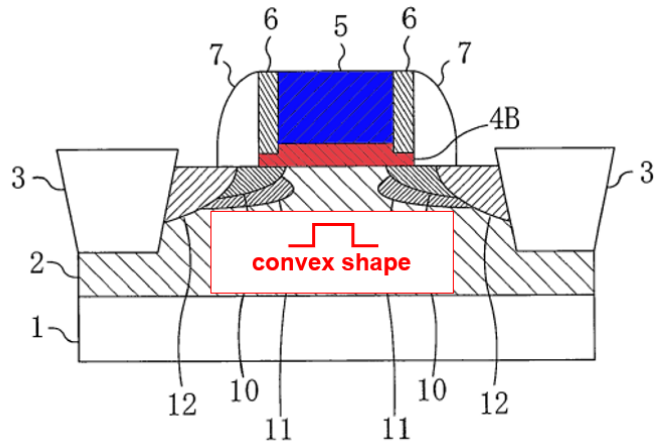
Kajiyama renders obvious “*the high dielectric constant gate insulating film is formed to have a convex cross-sectional shape*” [20]. (TSMC-1003, ¶¶255-57.)

In Kajiyama’s first embodiment, the part of the gate insulating film under the first insulating sidewall has a smaller thickness than the part of the gate insulating film under the gate electrode. (§XIII.B.4.) This forms a gate insulating film having a generally convex cross-sectional shape, consistent with the

disclosure of the '764 patent. (TSMC-1001, 7:54-59 (describing the gate insulating film 4B as having “a convex shape”).)



Kajiyama, Figure 1(D)



'764 Patent, Figure 2

XV. GROUND 11: Kajiyama-Wang Combination Renders Claims 7 and 11 Obvious.

While Kajiyama discloses exemplary high-k dielectrics, it does not explicitly disclose a high-k film formed “of a *HfSiON film*” [7] or that “*has a thickness of 2 nm or less*” [11]. Wang discloses these teachings, and the Kajiyama-Wang combination renders claims 7 and 11 obvious. Wang and Kajiyama are in the same field as the '764 patent. (TSMC-1001, 1:15-16; TSMC-1011, ¶1; TSMC-1012, ¶2; TSMC-1003, ¶258.)

A. Claim 7

Kajiyama teaches that, while high-k film 2 is discussed as a ZrO_2 film, “other high dielectric films ... can be used instead.” (TSMC-1011, ¶45.) Based on this suggestion, a POSITA would have been motivated to investigate different

high-k materials and would have been led to Wang, which presents a list of alternatives for its high-k gate dielectric including Hf-based dielectrics (e.g., HfO₂, HfSiO, HfON, or HfSiON). (TSMC-1012, ¶¶9, 25; TSMC-1003, ¶¶259-60.)

A POSITA would have also been motivated to use HfSiON to enhance operation of Kajiyama's device because nitrogen incorporation was found to improve thermal stability and electrical characteristics of HfSiON, including by enhancing the dielectric constant of the film. (TSMC-1029, 849; TSMC-1003, ¶260.)

B. Claim 11

Wang further teaches that, for a HfSiON gate insulating layer, the film “was deposited to a thickness of about 5 to 50 Angstroms [0.5 to 5 nm]” with “an equivalent oxide thickness (EOT) of less than about 2.0 nanometers.” (TSMC-1012, ¶34.) Thus, in combination with Kajiyama, the thickness of the HfSiON gate insulating film at its side ends would also range from about less than 0.5 nm to less than 5 nm since the thickness of the layer is smaller under first sidewall 5 than under the gate electrode. (TSMC-1003, ¶¶262-63.) The thickness of 2 nm (20 Angstroms) falls within the range of thicknesses disclosed by Wang. (TSMC-1003, ¶263.)

The '764 patent provides no discussion, evidence, or motivation associated with the selection of 2 nm for the gate insulating film. (TSMC-1003, ¶264.) Thus,

the Kajiyama-Wang combination renders obvious that “*each side end portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less*” [11]. *Ormco Corp.*, 463 F.3d at 1311 (“Where a claimed range overlaps with a range disclosed in the prior art, there is a presumption of obviousness.”); *E.I. DuPont de Nemours*, 904 F.3d at 1008.

XVI. GROUND 12: Kajiyama-Sim Combination Renders Claim 11 Obvious.

Should an argument be made the Kajiyama-Wang combination does not render claim 11 obvious, Sim discloses this feature. (§VII.) Sim and Kajiyama are in the same field as the ’764 patent. (TSMC-1001, 1:15-16; TSMC-1011, ¶1; TSMC-1024, Abstract; TSMC-1003, ¶265.)

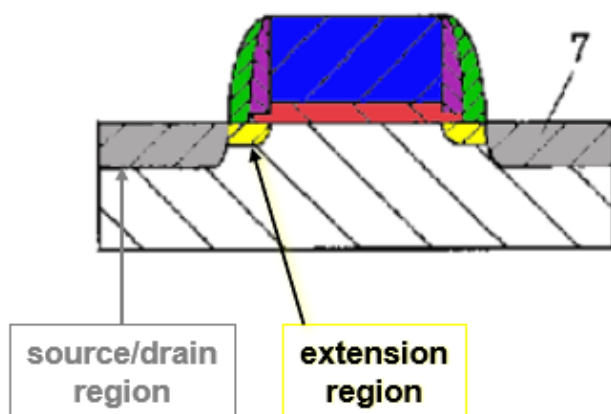
As noted above, Sim concluded that “[s]caling the physical thickness of the HfO₂ dielectric to below 20Å [2 nm] causes less charge trapping and higher mobility.” (TSMC-1024, 221.) Kajiyama discloses use of HfO₂ as a high-k gate dielectric (TSMC-1011, ¶45), the same film studied in Sim. A POSITA would have been motivated to apply Sim’s teachings in Kajiyama’s first embodiment device to form a HfO₂ gate insulating film with a thickness of 20Å (2 nm) or less. (TSMC-1003, ¶¶267-69.)

A POSITA would have been motivated to make the above combination for the reasons discussed in §VII and to improve the performance of Kajiyama’s device. (TSMC-1003, ¶268.) The combination is nothing more than use of a known

technique (Sim's HfO₂ dielectric layer with less than 20Å thickness) to improve similar devices in the same way for the above reasons. *KSR*, 550 U.S. at 416-17; TSMC-1003, ¶269. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable because Sim uses a well-known process for fabricating high-k films. (TSMC-1024, 218; §VII; TSMC-1003, ¶269.)

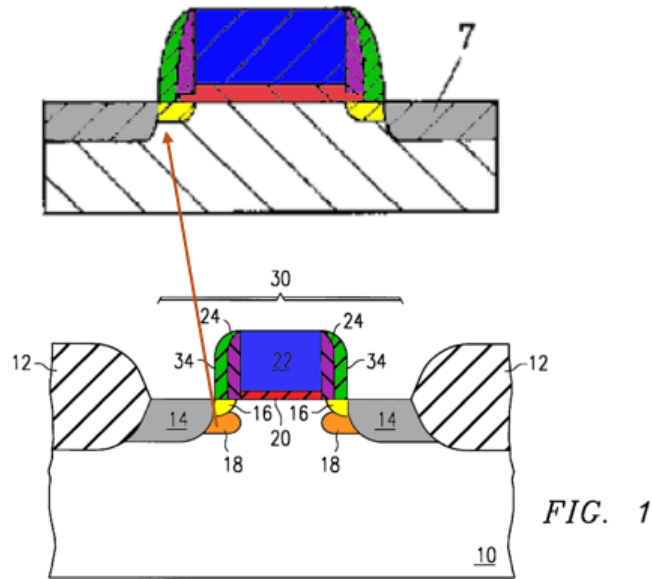
XVII. GROUND 13: Kajiyama-Rodder Combination Renders Claims 8-9 Obvious.

Kajiyama describes an **n-type** LDD diffusion layer 4 (“*extension region*”) (shaded yellow) located under first and second sidewalls 5, 6 and “on the surface of Si substrate 1” (part of the “*active region*” of the substrate). (TSMC-1011, ¶29, Figure 1(D).) Kajiyama’s device further includes “an **n**⁺ source drain diffusion layer 7” formed after first and second sidewalls 5, 6. (TSMC-1011, ¶32.) Kajiyama therefore teaches “*an extension region of a first conductivity type is formed in each of parts of the active region located under the first insulating sidewall and the second insulating sidewall*” [8A] and “*each of source/drain regions of a first conductivity type is formed in part of the active region ...*” [9]. (TSMC-1003, ¶271.) Kajiyama however does not teach use of “*pocket regions*”, a feature the ’764 patent admits was known. (TSMC-1001, 1:45-51, Figures 16A-B.)



Kajiyama, Figure 1(D)

Rodder describes use of “*pocket regions*” having “opposite conductivity to” the conductivity of the extensions. (TSMC-1023, 4:35-36; §IX.B.) A POSITA would have been motivated to combine Rodder’s teachings regarding the use of a pocket region below the extension region and external to the source/drain regions in Kajiyama’s first embodiment device, as illustrated below. Rodder and Kajiyama are in the same field as the ’764 patent. (TSMC-1001, 1:15-16; TSMC-1011, ¶1; TSMC-1023, Abstract; TSMC-1003, ¶141.)



Kajiyama, Figure 1(D) (top); Rodder, Figure 1 (bottom)

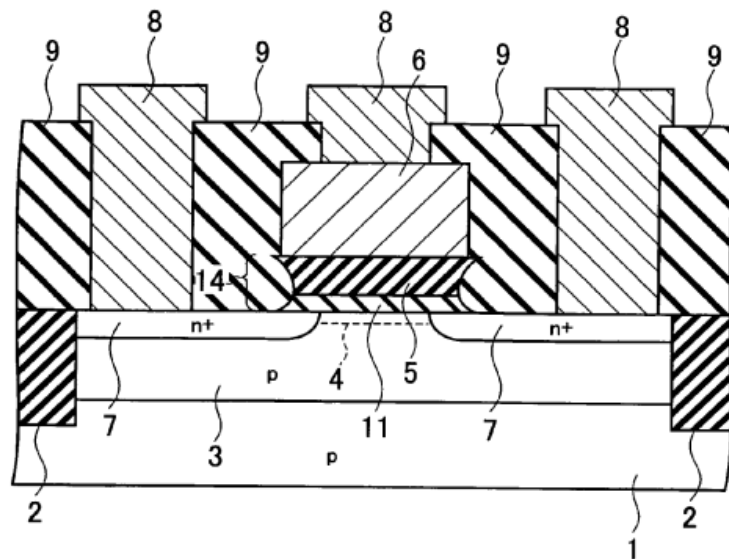
A POSITA would have been motivated to make this combination to obtain the benefits of pocket regions described by Rodder. (TSMC-1023, 1:22-25; §IX.B; TSMC-1003, ¶273.) The combination is also nothing more than the use of a known technique (Rodder’s formation of pocket regions below extension regions and outside of source/drain regions) to improve similar devices in the same way. *KSR*, 550 U.S. at 416-17; TSMC-1003, ¶274. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable for the reasons discussed in §X.B. (TSMC-1003, ¶274.)

XVIII. GROUND 14: Kajiyama-Ono Combination Renders Claims 10, 12, and 13 obvious.

Kajiyama does not expressly disclose the high-k gate insulating film “includes a notch at a side end portion” [10], or that the high-k film’s side surface

“is located at a predetermined distance from a side end surface of the first insulating sidewall toward the gate electrode” [12] or “is located at a predetermined distance from a side end surface of the gate electrode toward the first insulating sidewall” [13]. Ono teaches these features, and the Kajiyama-Ono combination renders obvious claims 10, 12, and 13. (TSMC-1003, ¶¶275-80.) Ono and Kajiyama are in the same field as the ’764 patent. (TSMC-1001, 1:15-16; TSMC-1011, ¶1; TSMC-1013, ¶¶3-7; TSMC-1003, ¶275.)

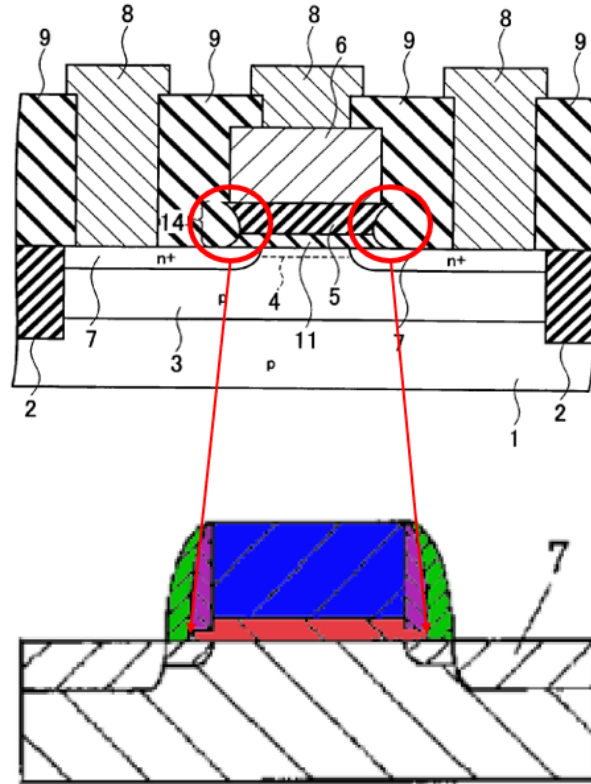
Ono discloses that “the sidewalls of the gate insulator film may curve” as shown, e.g., in Figure 108 (below). (TSMC-1013, ¶216.)



Ono, Figure 108

A POSITA would have been motivated to apply Ono’s teaching of curving the end portions of a gate insulating film to Kajiyama’s high-k dielectric (shaded red) in the first embodiment (Figure 1(D)), as illustrated below. (TSMC-1003,

¶277.) Thus, in the combination, the side ends of Kajiyama's gate insulating film have a semicircular shape, as taught by Ono.



Ono, Figure 108 (top); Kajiyama, Figure 1(D) (bottom)

A POSITA would have been motivated to make the above combination because Ono expressly suggests the combination, as discussed in §IX.B, and to improve performance of Kajiyama's first embodiment device by optimizing the electrical capacitance between the gate electrode and the source/drain regions. (TSMC-1013, ¶¶200, 216; TSMC-1003, ¶279.)

The Kajiyama-Ono combination is nothing more than the use of a known technique (Ono's use of curved side surfaces for a gate insulating film) to improve

similar devices in the same way for the above reasons. *KSR*, 550 U.S. at 416-17; TSMC-1003, ¶280. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable. (TSMC-1003, ¶280.) Kajiyama and Ono both use high-k gate insulating films that extend under the gate electrode and the insulating sidewall, a concept well-known before the '764 patent. (§§IV.B.2.b, IV.D.2, XIII.B.4, IX.A.) And both form their high-k dielectrics using conventional techniques. (TSMC-1011, ¶29; TSMC-1013, ¶167; TSMC-1003, ¶280.)

In the device of the Kajiyama-Ono combination, the end portion of Kajiyama's gate insulating film has a semicircular shape, as taught by Ono. The Kajiyama-Ono combination therefore discloses a device where "*high dielectric constant gate insulating film includes a notch at a side end portion*", consistent with the disclosure of the '764 patent. (*E.g.*, TSMC-1001, 8:35-40 (referring to notch 20 of Figure 7), Figure 7 (depicting notch 20 having a semicircular shape); TSMC-1003, ¶278.)



'764 Patent, Figure 7 with enlargement

Additionally, in the Kajiyama-Ono combination, when the notch is applied at each side end of Kajiyama's gate insulating film 2 located under the first sidewall 5, the end of the gate insulating film no longer extends completely under the first insulating sidewall. Further, as discussed in §IX.C, the notch's semicircular shape and the distance which the semicircular shape extends inward toward the gate electrode are set by specific process parameters. (TSMC-1003, ¶281.) Accordingly, in the Kajiyama-Ono combination, the gate insulating film's side surface is “located at a predetermined distance from a side end surface of the first insulating sidewall toward the gate electrode” [12] and “located at a predetermined distance from a side end surface of the gate electrode toward the

first insulating sidewall” [13], consistent with the disclosure of the ’764 patent.

(TSMC-1001, 21:26-30 (“side surface ... may be located at a predetermined distance from a side end surface of the sidewall 7 or the offset sidewall 6 toward the gate electrode 5”); TSMC-1003, ¶281.)

XIX. GROUND 15: Kajiyama-Bu Combination Renders Claims 14-15 Obvious.

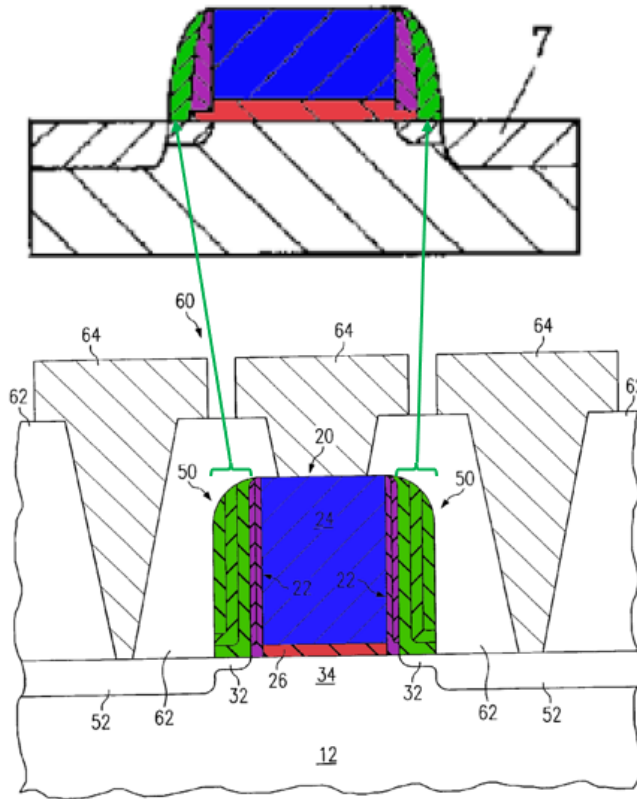
The Kajiyama-Bu combination discloses an outer sidewall with “*a double layer structure*” [14] and “*a triple layer structure*” [15]. (TSMC-1003, ¶¶282-90.)

Bu teaches an outer sidewall structure having three layers. (TSMC-1025, ¶¶26, 42-43; §XI.) Bu’s sidewall structure includes a first sidewall-forming layer 40 comprising an oxide, a second sidewall-forming layer 42 comprising a nitride, and a third sidewall-forming layer 44 comprising an oxide. (TSMC-1025, ¶¶27, 30, 35.) Bu and Kajiyama are in the same field as the ’764 patent. (TSMC-1001, 1:15-16; TSMC-1011, ¶1; TSMC-1025, Abstract; TSMC-1003, ¶141.)

A. Triple Layer-Claim 15

In Kajiyama’s first embodiment, the second sidewall 6 is a silicon nitride film (“*a nitride film*”). (§XIII.B.3; TSMC-1011, ¶28; TSMC-1003, ¶284.) A POSITA would have been motivated to use Bu’s triple-layer ONO sidewall structure with Kajiyama’s first embodiment device. Specifically, a POSITA would have been motivated to form Kajiyama’s second sidewall 6 (shaded green in Figure 1(D) (top)) with two additional silicon oxide layers to create a triple-layer

ONO sidewall structure, as taught by Bu. (TSMC-1003, ¶¶284-86.) The resulting device discloses that “the second insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film” [15]. (TSMC-1003, ¶284.)



Kajiyama, Figure 1(D) (top); Bu, Figure 1E (bottom)

A POSITA would have been motivated to combine Bu’s teaching of a triple-layer ONO sidewall structure with Kajiyama in light of the known benefits of ONO structures. (§XI; TSMC-1003, ¶285.) For example, Bu teaches that “the film properties of sidewall-forming layers 40 and 42 may minimize dopant loss from

source drain extension region 32 to first sidewall-forming layer 40,” thereby lowering parasitic resistance. (TSMC-1025, ¶26.)

The combination is nothing more than the use of a known technique (Bu’s triple-layer sidewall) to improve similar devices in the same way. *KSR*, 550 U.S. at 416-17; TSMC-1003, ¶286. Finally, Kajiyama and Bu disclose forming sidewall layers using standard deposition and etching techniques (TSMC-1011, ¶¶30-31; TSMC-1025, ¶¶27, 30, 35, 38), making the application of Bu’s multiple-layer structure to Kajiyama’s device straightforward. Accordingly, a POSITA would have had a reasonable expectation of success in the combining these references, leading to predictable results. (TSMC-1003, ¶286.)

B. Double Layer-Claim 14

A POSITA would also have been motivated by Bu’s teachings to form Kajiyama’s second sidewall 6 (formed of nitride) with a single additional silicon oxide layer to create a double-layer sidewall structure, resulting in a device where *“the second insulating sidewall has a double layer structure including an oxide film and a nitride film”* [14]. (TSMC-1003, ¶¶287-88.) As discussed previously, Bu teaches that the film properties of additional layers may minimize dopant loss and lower parasitic resistance. (TSMC-1025, ¶26.) Additionally, where design requirements dictate reducing manufacturing complexity, a POSITA would have known to use fewer (i.e., two) layers to similarly achieve the benefits taught by Bu.

(TSMC-1003, ¶289.) In light of these considerations, a POSITA would have been motivated to implement Bu's teachings into Kajiyama's device to form a double-layer sidewall structure. (*Id.*)

For the same reasons discussed above, the combination of Kajiyama and Bu to include a double-layer sidewall structure is nothing more than the use of a known technique to improve similar devices in the same way, and a POSITA would have had a reasonable expectation of success in the combining these references, leading to predictable results. *KSR*, 550 U.S. at 416-17; TSMC-1003, ¶290.

XX. GROUND 16: Kajiyama-Wilk Combination Renders Claims 18-19 Obvious.

Should PO argue that Kajiyama does not teach claims 18-19, Wilk expressly teaches these limitations. Wilk and Kajiyama are in the same field as the '764 patent. (TSMC-1001, 1:15-16; TSMC-1011, ¶1; TSMC-1018, Abstract; TSMC-1003, ¶292.)

As noted in §XII, Wilk discloses the following table for various high-k materials:

TABLE I. Comparison of relevant properties for high- κ candidates.

Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si	Crystal structure(s)
SiO ₂	3.9	8.9	3.2	Amorphous
Si ₃ N ₄	7	5.1	2	Amorphous
Al ₂ O ₃	9	8.7	2.8 ^a	Amorphous
Y ₂ O ₃	15	5.6	2.3 ^a	Cubic
La ₂ O ₃	30	4.3	2.3 ^a	Hexagonal, cubic
Ta ₂ O ₅	26	4.5	1–1.5	Orthorhombic
TiO ₂	80	3.5	1.2	Tetrag. ^c (rutile, anatase)
HfO ₂	25	5.7	1.5 ^a	Mono. ^b , tetrag. ^c , cubic
ZrO ₂	25	7.8	1.4 ^a	Mono. ^b , tetrag. ^c , cubic

^aCalculated by Robertson (See Ref. 153).

^bMono.=monoclinic.

^cTetrag.=tetragonal.

Wilk, Table I

A POSITA would have been motivated to look to Wilk’s teachings to understand the properties of materials discussed in Kajiyama, for example, to ensure that the gate insulating film had a sufficiently high dielectric constant. (TSMC-1003, ¶¶292-93.)

Kajiyama teaches that, in addition to ZrO₂, “other high dielectric films, such as a HfO₂ film, a Ta₂O₅ film, or a Al₂O₃ film, can be used instead to obtain the effects of the invention.” (TSMC-1011, ¶45.) ZrO₂ has a dielectric constant of 25, HfO₂ has a dielectric constant of 25, Ta₂O₅ has a dielectric constant of 26, all of which are greater than 10. (TSMC-1018, Table I.) Further, Kajiyama discloses that the second sidewall 6 is comprised of silicon nitride (Si₃N₄), which has a dielectric

constant of 7. (TSMC-1011, ¶28; TSMC-1018, Table I.) The combination of Kajiyama and Wilk renders obvious claims 18-19. (TSMC-1003, ¶¶292-96.)

XXI. Discretionary Denial Is Not Appropriate.

A. 35 U.S.C. §314(a)

Pursuant to the Stewart Memorandum dated March 26, 2025, titled “Interim Process for PTAB Workload Management,” Petitioner will respond to any discretionary denial arguments Patent Owner may raise through the Board’s bifurcated briefing process.

Nevertheless, to simplify the *Fintiv* analysis, and following the precedential *Sotera* decision, Petitioner stipulates that, if IPR is instituted, Petitioner will not pursue in the related district court proceeding any ground that Petitioner raised or reasonably could have raised against the challenged claims during the instituted IPR.

B. 35 U.S.C. §325(d)

The *Advanced Bionics* framework favors institution. *Advanced Bionics LLC v. MED-EL Elektromedizinische Gerate GmbH*, IPR2019-01469, Paper 6 (P.T.A.B. Feb. 13, 2020) (precedential). None of the applied references was applied by the Examiner during prosecution. Applicant cited a different JP publication to Ono (JP2005-064190; “JP-Ono”) on an information disclosure statement. While Petitioner disputes that JP-Ono is sufficiently similar to Ono to trigger *Advanced*

Bionics Part 1, JP-Ono was not applied by the Examiner and thus was not evaluated during examination. Even assuming JP-Ono was evaluated (which the record does not support), the Office erred in allowing the claims. Petitioner relies on Ono only for dependent claims 6, 10, and 12-13 relating to the side end of the gate insulating film. Petitioner's other cited art discloses all limitations of independent claim 1, including, for example, a "gate insulating film," a "gate electrode," and the thickness of the high-k film under the first insulating sidewall has a smaller thickness than the thickness of the high-k film under the gate electrode, which Applicant argued in prosecution distinguished the prior art. (§§V.B, XIII.B.) The Petition therefore presents grounds never considered by the Office. The Petition's evidence warrants consideration because it presents a compelling case of unpatentability never considered by the Office. These circumstances weigh heavily against §325(d) discretionary denial.

XXII. Mandatory Notices

A. Real Party in Interest

The Petitioner and real party-in-interest is Taiwan Semiconductor Manufacturing Company Ltd.

B. Related Matters

To the best of Petitioner's knowledge, the '764 patent is involved in the following ongoing litigation:

- *Advanced Integrated Circuit Process LLC, v. Taiwan Semiconductor Manufacturing Company Limited*, No. 2:24-CV-623 (E.D. Tex.)
- *Advanced Integrated Circuit Process LLC, v. United Microelectronics Corporation*, No. 2:24-CV-730 (E.D. Tex.)

On April 15, 2025, Petitioner filed petitions for *inter partes* review of U.S. Patent 7,579,227 (IPR2025-00828), U.S. Patent 8,253,180 (IPR2025-00830), and U.S. Patent 8,587,076 (IPR2025-00831).

C. Notice of Counsel and Service Information

Pursuant to 37 C.F.R. §§42.8(b)(3), 42.8(b)(4) and 42.10(a), Petitioner appoints the following lead and backup counsel:

Lead Counsel	Back Up Counsel
Lori A. Gordon (Reg. No. 50,633) Goodwin Procter LLP 1900 N. Street NW Washington, D.C. 20036 Phone: (202) 346-4000 Fax: (202) 346-4444 Gordon-PTAB@goodwinlaw.com	Andrew S. Ong (Reg. No. 69,076) Goodwin Procter LLP 601 Marshall Street Redwood City, CA 94063 Phone: (650) 752-3100 Fax: (650) 853-1038 AOng@goodwinlaw.com
	Theodoros Konstantakopoulos, Ph.D. (Reg. No. 74,155) Goodwin Procter LLP 620 Eighth Avenue New York, NY 10018 Phone: (212) 813-8800 Fax: (212) 355-3333 TKonstantakopoulos@goodwinlaw.com

	Jesse Cheng (<i>pro hac vice</i> forthcoming) Goodwin Procter LLP 601 Marshall Street Redwood City, CA 94063 Phone: (650) 752-3100 Fax: (650) 853-1038 JesseCheng@goodwinlaw.com
	Filippos Papadatos (Reg No. 78,834) Goodwin Procter LLP 620 Eighth Avenue New York, NY 10018 Phone: (212) 813-8800 Fax: (212) 355-3333 fpapadatos@goodwinlaw.com

Petitioner consents to electronic service by email at the addresses: Gordon-ptab@goodwinlaw.com, aong@goodwinlaw.com, jessecheng@goodwinlaw.com, fpapadatos@goodwinlaw.com, and tkonstantakopoulos@goodwinlaw.com.

XXIII. Conclusion

Inter partes review of the challenged claims is respectfully requested.

Respectfully submitted,

/Lori A. Gordon/

Lori A. Gordon
Reg. No. 50,633

GOODWIN PROCTER LLP
1900 N Street, N.W.
Washington, D.C. 20036-1612
(202) 346-4000

Date: April 15, 2025

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(a), Petitioner hereby certifies that portions of the above-captioned **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 7,923,764**, in accordance with and reliance on the word count provided by the word-processing system used to prepare this Petition, that the number of words in this paper is 13,989. Pursuant to 37 C.F.R. §42.24(a), this word count is in compliance and excludes the table of contents, table of authorities, mandatory notices under §42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing. This word count was prepared using Microsoft Word.

Respectfully submitted,

/Lori A. Gordon/

Lori A. Gordon
Reg. No. 50,633
Attorney for Petitioner

Goodwin Procter LLP
1900 N. Street NW
Washington, D.C. 20036
Phone: (202) 346-4000
Fax: (202) 346-4444

Date: April 15, 2025

CERTIFICATE OF SERVICE

The undersigned hereby certifies, in accordance with 37 C.F.R. § 42.105, that the foregoing **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 7,923,764**, TSMC's Power of Attorney, and all supporting exhibits were served via FedEx Next Business Day Delivery on April 15, 2025, in their entirety on the Patent Owner as detailed below:

Michael J. Cherskov & Szymon M. Gurda
Cherskov, Flaynik & Gurda, LLC
903 Commerce Drive, Suite 310
Oak Brook, IL 60523

Courtesy copies have been concurrently served by electronic mail on Patent Owner's litigation counsel at:

Justin A. Nelson
SUSMAN GODFREY L.L.P.
1000 Louisiana Street, Suite 5100
Houston, TX 77002
Jnelson@susmangodfrey.com

Respectfully submitted,

/Lori A. Gordon/

Lori A. Gordon
Reg. No. 50,633
Attorney for Petitioner

Goodwin Procter LLP
1900 N. Street NW
Washington, D.C. 20036
Phone: (202) 346-4000
Fax: (202) 346-4444

Date: April 15, 2025

Appendix: Challenged Claims Listing

[1P] A semiconductor device comprising:

[1A] a high dielectric constant gate insulating film formed on an active region in a substrate;

[1B] a gate electrode formed on the high dielectric constant gate insulating film;

[1C] a first insulating sidewall formed on each side surface of the gate electrode; and

[1D] a second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween,

[1E] wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, and

[1F] part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

[2] The semiconductor device of claim 1, further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film.

[3] The semiconductor device of claim 2, wherein the buffer insulating film is a silicon oxide film.

[4] The semiconductor device of claim 1, wherein the first insulating sidewall is an offset sidewall.

[5] The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall.

[6] The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a Hf based oxide.

[7] The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a HfSiON film.

[8] The semiconductor device of claim 1,

[8A] wherein an extension region of a first conductivity type is formed in each of parts of the active region located under the first insulating sidewall and the second insulating sidewall, and

[8B] a pocket region of a second conductivity type is formed in part of the active region located under the extension region.

[9] The semiconductor device of claim 8, wherein each of source/drain regions of a first conductivity type is formed in part of the active region located in an external side to the extension region and the pocket region when viewed from the gate electrode.

[10] The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film includes a notch at a side end portion.

[11] The semiconductor device of claim 1, wherein each side end portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less.

[12] The semiconductor device of claim 1, wherein a side surface of the high dielectric constant gate insulating film is located at a predetermined distance from a side end surface of the first insulating sidewall toward the gate electrode.

[13] The semiconductor device of claim 1, wherein a side surface of the high dielectric constant gate insulating film is located at a predetermined distance from a side end surface of the gate electrode toward the first insulating sidewall.

[14] The semiconductor device of claim 1, wherein the second insulating sidewall has a double layer structure including an oxide film and a nitride film.

[15] The semiconductor device of claim 1, wherein the second insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film.

[16] The semiconductor device of claim 1, wherein a width of the high dielectric constant gate insulating film along a gate length is larger than a width of the gate electrode along the gate length.

[17] The semiconductor device of claim 1, wherein a width of a bottom surface of the high dielectric constant gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length.

[18] The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more.

[19] The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall.

[20] The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed to have a convex cross-sectional shape.

[21] The semiconductor device of claim 1, wherein each side end portion of the high dielectric constant gate insulating film is not in contact with the first insulating sidewall.