# Reduction of sidewall defect induced leakage currents by the use of nitrided field oxides in silicon selective epitaxial growth isolation for advanced ultralarge scale integration

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Defects in the near sidewall region in selective epitaxial growth of silicon have prevented its widespread use as a viable dielectric isolation technology. The main cause of these defects has been demonstrated to be thermal stress due to mismatch in the coefficient of thermal expansion between silicon and silicon dioxide. This article presents the detailed electrical characterization of these sidewall defects using $P+/N$ junction diodes fabricated using silicon dioxide and thermally nitrided silicon dioxide as the field insulator. It is shown that the use of field oxide which was nitrided at 1100 °C for 60 min in ammonia gas ambient reduced the reverse saturation current density in the diodes by a factor of 6 and also improved the forward recombination and ideality factors when compared to standard thermal field oxide isolated diodes. The improvement of the sidewall quality was attributed to a reduction in thermal stress due to the modification of the coefficient of thermal expansion of nitrided silicon oxide. © *2000 American Vacuum Society.* [S0734-211X(00)08802-8]

## I. BACKGROUND/MOTIVATION

Selective growth of silicon is finding increasing use in a variety of applications in advanced, submicron ultralarge scale integration (ULSI). Selective epitaxial growth (SEG), epitaxial lateral overgrowth (ELO), and confined lateral selective epitaxial growth (CLSEG) have been demonstrated to be useful for a variety of devices and three-dimensional applications in complementary metal-oxide-semiconductors (CMOS), bipolar and biCMOS devices.[1–4] More recently, selective growth has been used for epitaxial base for bipolar junction transistors,[5–7] epitaxial channel in metal-oxide-semiconductor field effect transistors (MOSFETs),[8–10] and device regions for advanced isolation.[11] Figure 1 shows the various selective growth techniques and how they can be applied to device fabrication. In addition, as silicon devices are scaled down to the deep submicron regime, the cost of device processing is increasing very rapidly. As compared to conventional recessed local oxidation of silicon (LOCOS) or shallow trench isolation (STI), SEG of silicon provides a simple and cost effective process for the formation of isolated device islands.[12]

The bulk SEG material for these applications is of excellent quality but the material close to the sidewall insulator can have a high defect density. The main cause of these defects has been demonstrated to be coefficient of thermal expansion (CTE) mismatch induced by thermal stress during the cooldown period of the epitaxial growth.[13,14] The detrimental effects of these defects can be circumvented if the defective sidewall region is implanted and is encompassed well within a junction. This is the case for bipolar junction transistors where, for most device layouts, the extrinsic base region intersects the sidewall of the oxide isolation region as shown in Fig. 2(a). For the case of MOSFETs, however, as shown in Fig. 2(b), there is always the region under the gate that does not get implanted and increases the leakage between the source and drain, resulting in poor yield.

Two possible ways to reduce the thermal stress are to reduce the growth temperature or to reduce the mismatch in expansion coefficients. Introducing nitrogen into the field oxide to change its coefficient of thermal expansion (CTE) has been proposed as a means to reduce these sidewall defects.[14] It is known that CTE $(SiO_2)<CTE(Si)<CTE(Si_3N_4)$, and hence nitridation of the field oxide should bring the thermal expansion coefficient of oxide closer to that of silicon. The purpose of the work described in this article is to experimentally demonstrate the reduction of the defect induced leakage currents in SEG silicon grown in nitrided field oxides (termed NOX) when compared to SEG structures which were grown in thermal oxide (OX) isolated regions. $P+/N$ junction diodes with varying perimeter-area ratios were fabricated and used to characterize the sidewall defects. Forward and reverse leakage currents were measured and used to evaluate and demonstrate the improved sidewall quality with the use of nitrided thermal oxide.

## II. SEG ISOLATION AND NATURE OF DEFECTS

Figure 3 shows a scanning electron micrograph of silicon SEG grown from a 0.2-$\mu$m-wide seed hole demonstrating the scalability of SEG to form deep submicron device islands. Device isolation using selective epitaxial growth has been proposed earlier.[11,15,16] Figure 4 shows a typical device isolation process using selective epitaxial growth. As can be noted from the cross sections, the process is simple and easy

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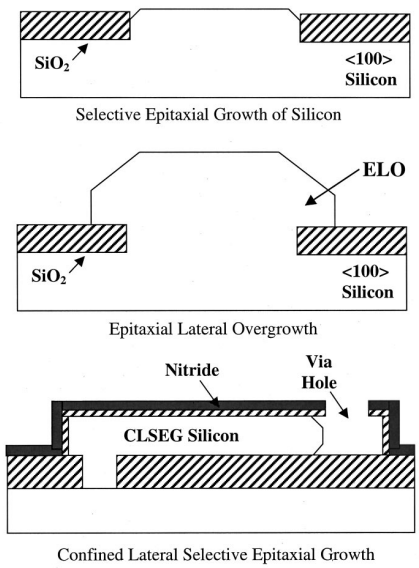


FIG. 1. Various selective epitaxial growth processes.

to implement. In addition, the process is also cost effective when compared to shallow trench isolation.[13] The only hindrance is the formation of these defects when the growth is done at high temperatures. A theoretical understanding and a one-dimensional model have been developed which explain that the defects are generated when the thermal stress induced from the sidewall and corner region of the oxide exceeds the yield strength of silicon, resulting in plastic deformation.[14,17] Generally, the thermal stress due to a mismatch in expansion coefficients is given by

$$\sigma_{\mathrm{Th}}=\frac{E}{1-\nu}\int_{25\,^{\circ}\mathrm{C}}^{T_{\mathrm{GR}}}[\alpha_{\mathrm{Si}}(T)-\alpha_{\mathrm{Ox}}(T)]dT, \tag{1}$$

where $E$ is the Young modulus of silicon, $\nu$ is the Poisson ratio, $\alpha_{\mathrm{Si}}$ and $\alpha_{\mathrm{Ox}}$ are the thermal expansion coefficient for

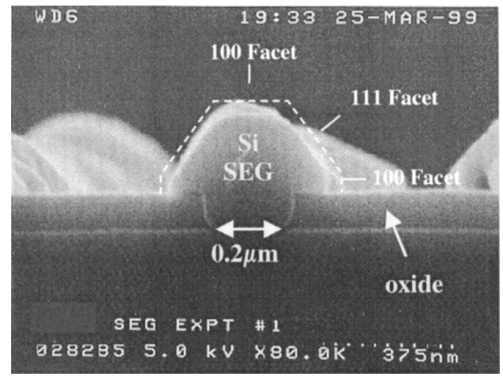


FIG. 3. SEG silicon grown from a 0.2-$\mu$m-wide seed hole.

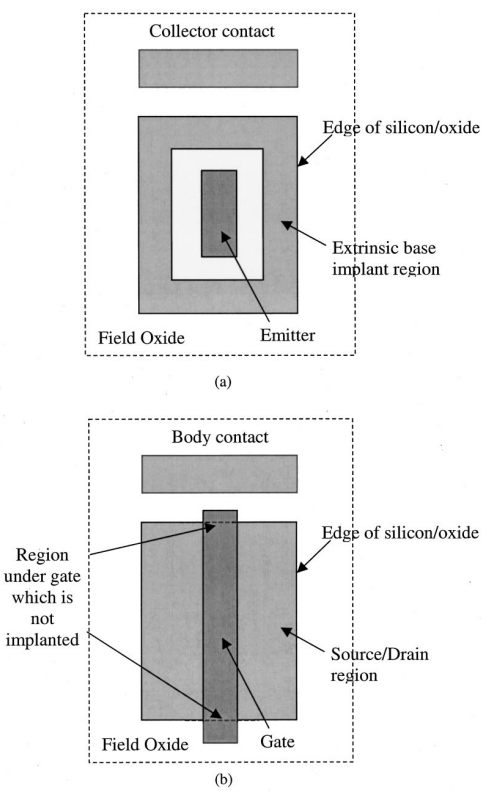


FIG. 2. (a) Top view layout of a bipolar junction transistor (BJT) device. Note that the region near the sidewall is always implanted with the extrinsic base region. (b) Top view layout of the MOSFET device. The region under the gate is not implanted with the source and drain.

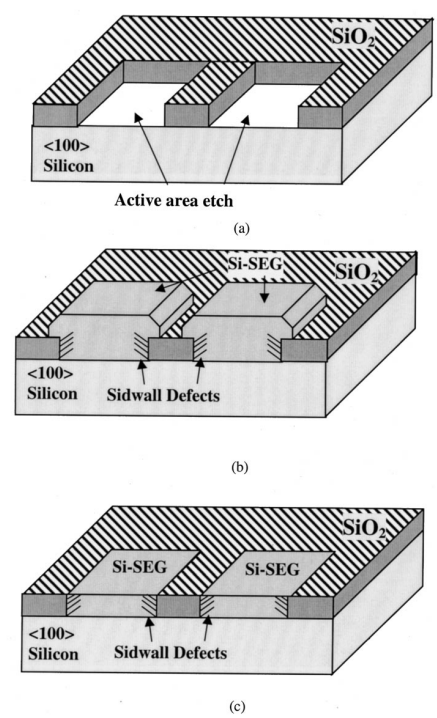


FIG. 4. Process flow for the SEG isolation flow. (a) Active regions are defined within an oxide window. (b) Selective epitaxial growth of silicon is performed to form the active device regions. The epitaxy can overgrow the insulator regions. (c) The silicon overgrowth is polished off using chemical-mechanical polishing, a process very commonly used in the semiconductor industry. The field insulator is used as an etch stop for the polishing.



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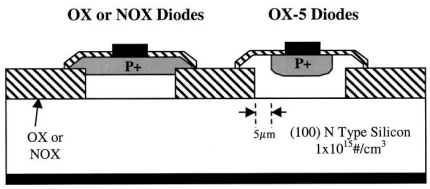


FIG. 5. Final cross section for the test structures used in this study.

silicon and oxide, and $T_{GR}$ is the growth temperature. The thermal stress should be less than the yield strength of silicon, which is a function of temperature and the strain rate. Hence, the two most obvious ways to reduce the thermal stress according to Eq. (1) are to reduce the SEG growth temperature or to match the coefficient of thermal expansion of silicon and the insulator. Reduction in growth temperature is useful for thin films where single wafer processing systems are increasingly being used. For high throughput processes, thicker silicon films used for isolation, and applications such as power devices, growth temperatures less than 900 °C are not very practical and can result in undesirably long growth cycles. Hence, the approach of modification of the coefficient of thermal expansion was proposed.[11,15] Since it is known that CTE ($SiO_2 = 0.6\times10^{-6}$ °C$^{-1}$)<CTE (Si $= 2.6\times10^{-6}$ °C$^{-1}$)<CTE ($Si_3N_4 = 3.2\times10^{-6}$ °C$^{-1}$), nitridation of the thermal oxide should bring the expansion coefficient closer to silicon. This approach was used to reduce the SEG sidewall thermal stress as described below.

## III. PROCESS FLOW AND DETAILS

The process used for this study began with the formation of a 1-$\mu$m-thick field oxide, which was grown on *N*-type (100) silicon wafer doped at $1\times10^{15}$ #/cm$^3$ using a dry/wet oxidation at 1100 °C for 2 h. Some of the wafers were then thermally nitrided in pure $NH_3$ at conditions described below. These wafers will be referred to as NOX wafers. The untreated wafers will be referred to as OX wafers. Seed windows for the SEG were reactive ion etched (RIE) into both the OX and NOX wafers using a 200 W, 80 mT $CHF_3$ plasma etch. Any RIE damage on the seed hole surface was removed by a 5 min steam oxidation at 1000 °C. This oxide was then removed in buffered hydrofluoric acid and the wafers were cleaned for SEG. *N*-type SEG silicon was then grown at 970 °C, 40 T using a $SiH_2Cl_2$ flow of 0.22 slm and HCl flow of 0.66 slm in a pancake-type reactor. Hydrogen was used as the carrier gas at a flow of 60 slm and the resulting growth rates were about 0.12 $\mu$m/min to result in a total growth of about 1.2 $\mu$m. Hence about 0.2 $\mu$m of silicon was overgrown. Boron was then implanted at an energy of 25 keV and a dose of $1\times10^{14}$ #/cm$^2$ to form the $P+$ region in the *N*-type SEG. The junctions were annealed at 1000 °C for 10 min, followed by contact mask, Al-1% Si metalization, and a hydrogen anneal step at 475 °C. Control diodes were also fabricated with junctions 5 $\mu$m away from the sidewall interface (referred as OX-5) to test the intrinsic material quality. The final cross section of the diodes is shown in Fig. 5.

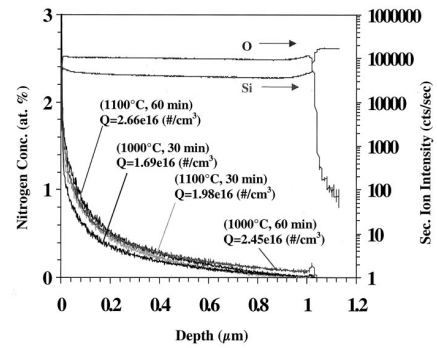


FIG. 6. Nitrogen profiles in the oxide from SIMS analysis as a function of nitridation conditions.

Test wafers with thermal oxide were nitrided in a pure $NH_3$ ambient at 1000 °C and 1100 °C for 30 and 60 min. The nitrogen profile as a function of depth and nitridation conditions is shown in Fig. 6. The secondary ion mass spectroscopy (SIMS) profile shown in this figure was obtained prior to the oxide etch in the field regions. The nitrogen profiles were measured using Quad SIMS using a cesium primary ion source beam (Charles Evans and Associates). Beam current of about 100 nA was used. Primary beams with 3 kV energy were used to get the best depth resolution. The conversion of measured secondary ion counts to concentration was performed by using relative sensitivity factors, which were obtained for nitrogen using a SiON reference sample. The inset in Fig. 6 also shows the nitrogen dose as a function of the nitridation condition. At 1000 °C, increasing the time from 30 to 60 min increased the dose by 45%. At 1100 °C, increasing the time from 30 to 60 min increased the dose by 34%. The time of nitridation appears to have a strong impact on the nitrogen incorporation dose. An 1100 °C, 60 min nitridation was chosen since it resulted in the highest dose among the conditions attempted. There is also a slight pileup at the nitrided oxide/silicon interface, which is consistent with literature.[18]

## IV. EXPERIMENTAL RESULTS

The reverse and forward currents of the $P+/N$ junction diodes were measured to study the material and sidewall quality of the SEG silicon. Table I shows the dimensions of

TABLE I. Perimeter and area of the diodes fabricated for the study.

| Diode | Area ($\times10^{-5}$ cm$^2$) | Perimeter ($\times10^{-2}$ cm) | *P/A* (cm$^{-1}$) |
|---|---|---|---|
| 1 | 7.00 | 3.40 | 486 |
| 2 | 4.71 | 2.76 | 586 |
| 3 | 4.50 | 2.80 | 622 |
| 4 | 3.46 | 2.36 | 683 |
| 5 | 3.20 | 2.28 | 713 |
| 6 | 2.18 | 1.88 | 861 |
| 7 | 1.60 | 1.60 | 1000 |
| 8 | 1.20 | 1.40 | 1167 |



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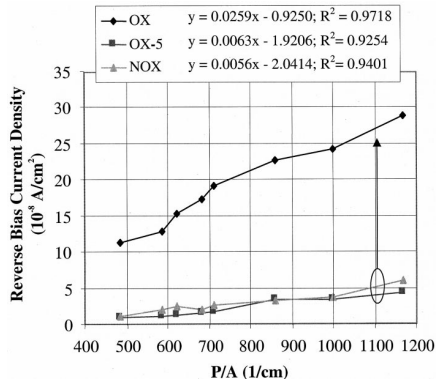


FIG. 7. Reverse saturation current density as a function of the perimeter to area ratio for the $P+/N$ junction diodes.

the diodes used in the study with a perimeter to area ratio ranging from 480 to 1100 (1/cm). The reverse and forward characterization is described below.

### A. Reverse characterization results and discussion

The total reverse leakage current can be broken into a bulk component and a perimeter component. The ratio of the total reverse leakage current and the area results in the following equation:

$$I_{TR}=J_{BR}\times A+J_{PR}\times P, \tag{2}$$

where $I_{TR}$ is the total reverse saturation current, $J_{BR}$ is the bulk reverse saturation current density and $J_{PR}$ is the perimeter reverse saturation current density. A plot of $J_{TR}$ $(=I_{TR}/A)$ versus perimeter to area ratio can then be used to extract the perimeter reverse saturation current. Figure 7 shows such a plot of $J_{TR}$ vs *P/A* ratio for the three types of diodes as measured using a Hewlett-Packard pico-ammeter. In the structures described herein, the silicon overgrowth on the oxide was about 0.2 $\mu$m and the junction formed was deeper than the overgrowth with the given implant and diffusion conditions. Hence, the junction does intersect the sidewall of the RIE etched oxide. The depletion will mainly extend downwards and intersect the sidewall of the oxide as desired, within the SEG region. The field oxide is 1 $\mu$m deep and the expected field threshold voltage will be around 5 V. Hence, the reverse voltage was kept low at around 0.3–0.5 V for these reverse current measurements. It is also important that the diode junction depletion region does not get connected to the field oxide capacitor depletion in the substrate. Calculations show that the depletion for the diode fabricated herein and reverse biased at around 0.5 V is around 0.2 $\mu$m. Hence the depletion regions from the diode and the possible depletion under the field oxide will not connect. The measurements, thus, should reflect only the leakage from the diode depletion regions.

As clearly seen, the reverse saturation current density $J_{TR}$ for the OX diode was about a factor of 5–6 higher than the other three types indicating the higher defect density along the oxide/silicon sidewall. Most interestingly, the value of the reverse perimeter saturation current density $J_{RP}$ for the NOX diodes was $0.63\times10^{-10}$ A/cm which was also very close to the $J_{RP}$ value for the OX-5 diode of $0.55\times10^{-10}$ A/cm. The $J_{RP}$ for the OX diode (the worse case) was $2.59\times10^{-10}$ A/cm and about a factor of 6 higher than the OX-5 and NOX diode. The OX-5 control diodes exhibited ideal current–voltage characteristics and were as good as $p+/n$ junction diodes reported earlier in selective epitaxial growth studies.[11–13] Hence, when the junctions were 5 $\mu$m away from the sidewall or when the field insulator is nitrided, the reverse saturation current density (both total and the perimeter component) were about the same. These reverse and forward measurements clearly show the improvement and reduction in the sidewall leakage currents due to the presence of the nitrided field oxide, thus proving the fact that the presence of the nitrided field oxide does reduce the thermal induced defects and hence the leakage currents.

TABLE II. Surface generation velocity ($S_0$) at the sidewall interface and the extrapolated saturation current density ($I_0$) from the forward characteristics for the various diodes.

| Diode type | $S_0$ (cm/s) | $I_0$ (A) $P/A$=486 cm$^{-1}$ | $I_0$ (A) $P/A$=1167 cm$^{-1}$ |
|---|---|---|---|
| OX | 2847 | 1*e*-12 | 3*e*-13 |
| OX-5 | 692 | 9*e*-15 | 6*e*-15 |
| NOX | 615 | 2*e*-13 | 2*e*-13 |

The reverse perimeter saturation current density can also be used to extract the sidewall perimeter surface generation velocity $S_0$ (cm/s) according to the formula

$$J_{PR}=qn_iWS_0, \tag{3}$$

where $q$ is the charge of an electron, $n_i$ is the intrinsic carrier, $W$ is the width of the depletion region, and $S_0$ is the surface generation velocity. Table II gives the values of $S_0$ for a depletion width of 0.37 $\mu$m as calculated using ideal step junction diode formulation.[19] The perimeter surface generation velocities for the NOX and OX-5 diodes are very close to each other and a factor of 4 smaller than the value for the OX diodes, indicating an improvement in the sidewall material quality with nitridation of the field oxide.

### B. Forward characterization results and discussion

The current through a diode in the forward bias region is the sum of the diffusion component and a recombination component. The recombination current dominates at low forward bias voltages while the diffusion current dominates at higher bias voltages. The forward characteristics of the three types of diodes were measured for the various *P/A* ratios. Figures 8 and 9 show the current–voltage characteristics for the diodes with *P/A* (1/cm) ratio of 486 and 1167, respectively. As can be clearly noted, the OX diodes have significantly higher current than the OX-5 diodes, especially at forward voltages less than 0.6 V indicating an increased recombination in the depletion region. The region of current from 0.3 to 0.5 V was used to extrapolate the curve down to a value of $V=0$ to obtain the total forward saturation current



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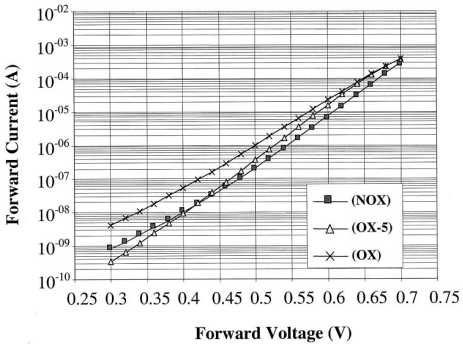


FIG. 8. Forward current–voltage characteristics of the three types (OX, NOX, OX-5) of diodes with the smallest *P/A* ratio [486 (1/cm)].

$I_0$. This value of saturation current is also an indication of the material quality, keeping in mind that it includes both the bulk and the perimeter effects. As noted from the values in Table II, $I_0$ decreases by an order of magnitude for the NOX diodes when compared to the OX diodes but is still larger than the OX-5 control diodes for the smallest *P/A* ratio device. Similarly, for the device with the largest *P/A* ratio, the improvement in $I_0$ is still present but is reduced due to the increased effect of the perimeter component. These forward $I$–$V$ results again show the same trend as the reverse characteristics, i.e., the NOX devices were significantly improved when compared to the OX diodes. It should also be pointed out that the reasons for the sidewall quality improvement could also include an impact on the viscous flow of the NOX sidewall, which would impact the stress along the sidewall.

## V. CONCLUSIONS

This article presented the detailed electrical characterization of $P+/N$ junction diodes fabricated in selective epitaxial silicon isolation structures using a nitrided field oxide insulator. It was demonstrated that the use of field oxide which was nitrided at 1100 °C for 60 min in an ammonia gas ambient improves the sidewall material quality by minimizing thermal stress due to modification of the coefficient of expansion. The reverse saturation current density and the forward recombination current significantly decreased in the diodes isolated in nitrided oxide when compared to standard thermal field oxide isolated diodes. Using diodes with various perimeter to area ratios, the perimeter sidewall saturation current density was also extracted and the values were found to be a factor of 4–6 lower for the nitrided oxide isolated diodes.

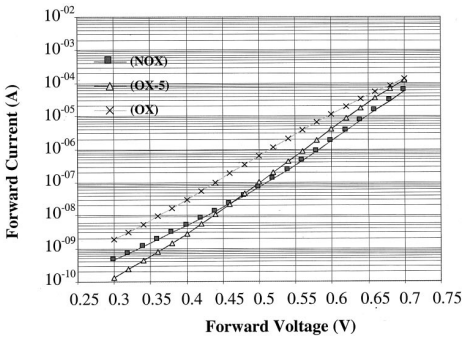


FIG. 9. Forward current–voltage characteristics of the three types (OX, NOX, OX-5) of diodes with the largest *P/A* ratio [1167 (1/cm)].

## ACKNOWLEDGMENTS

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[1]G. W. Neudeck, P. J. Schubert, J. L. Glenn, J. A. Friedrich, W. A. Klaasan, R. P. Zingg, and J. P. Denton, J. Electron. Mater. **19**, 1111 (1990).
[2]L. Jastrzebski, J. Cryst. Growth **63**, 493 (1983).
[3]R. Zingg, J. A. Friedrich, G. W. Neudeck, and J. P. Denton, IEEE Trans. Electron Devices **37**, 1452 (1990).
[4]R. Bashir, S. Venkatesan, G. W. Neudeck, and J. P. Denton, IEEE Electron Device Lett. **13**, 392 (1992).
[5]S. Decoutere, R. Kuhn, F. Vleugels, G. Vancuyck, M. Caymax, B. Mohadjeri, and L. Deferm, Proceedings of the 1998 Bipolar/BiCMOS Circuits and Technology Meeting, 1998, p. 124.
[6]A. Pruijmboom, D. Terpstra, C. E. Timmering, W. B. de Boer, M. J. J. Theunissen, J. W. Slotboom, R. J. E. Heuting, and J. J. Hageraats, Int. Electron Devices Meet. Tech. Dig. 747 (1995).
[7]K. Washio, E. Ohue, K. Oda, M. Tanabe, H. Shimamoto, T. Onai, and M. Kondo, IEEE Trans. Electron Devices **46**, 1411 (1999).
[8]T. Ohguro, H. Naruse, H. Sugaya, E. Morifuji, S. Nakamura, T. Yoshitomi, T. Morimoto, H. S. Momose, Y. Katsumata, and H. Iwai, Int. Electron Devices Meet. Tech. Dig. 837 (1997).
[9]V. Dudek, W. Appel, L. Beer, and B. Hofflinger, Proceedings of the 25th European Solid State Device Research Conference, 1995, p. 221.
[10]U. Konig, M. Gluck, and G. Hock, J. Vac. Sci. Technol. B **16**, 2604 (1998).
[11]J. M. Sherman, G. W. Neudeck, J. P. Denton, R. Bashir, and W. W. Fultz, IEEE Electron Device Lett. **17**, 267 (1996).
[12]J. C. Hughes, G. W. Neudeck, and R. Uzsoy, Proceedings of the 23rd IEEE/CPMT International Electronics Manufacturing Technology Symposium, 1998, pp. 333–336.
[13]R. Bashir, G. W. Neudeck, Y. Haw, E. P. Kvam, and J. P. Denton, J. Vac. Sci. Technol. B **13**, 923 (1995).
[14]R. Bashir, G. W. Neudeck, Y. Haw, and E. P. Kvam, J. Vac. Sci. Technol. B **13**, 928 (1995).
[15]H. Kurtan, H. Voss, W. Kim, and W. L. Engl, IEEE Trans. Electron Devices **ED-30**, 1511 (1983).
[16]N. Endo, N. Kasai, A. Ishitano, H. Kitajima, and Y. Kurogi, IEEE Trans. Electron Devices **ED-33**, 1283 (1984).
[17]A. Ishitani, H. Katijima, N. Endo, and N. Kasai, Jpn. J. Appl. Phys., Part 1 **28**, 841 (1989).
[18]T. Hori, H. Iwasaki, Y. Naito, and H. Esaki, IEEE Trans. Electron Devices **ED-34**, 2338 (1987).
[19]R. F. Pierret, *Advanced Semiconductor Fundamentals*, Modular Series on Solid State Devices, Vol. 5 (Addison-Wesley, Reading, MA, 1987), pp. 157–168.



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