



Semicon Processing

for the VLSI Era
Volume 1 - Process Technology
Second Edition

S. Wolf and R.N. Tauber

**SILICON PROCESSING
FOR
THE VLSI ERA**

**VOLUME 1:
PROCESS TECHNOLOGY
Second Edition**

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Chapter 7

SILICON EPITAXIAL GROWTH and SILICON ON INSULATOR

The *epitaxial* growth process provides an excellent means of growing a thin film of single crystal material upon the surface of a single crystal substrate. The term *epitaxy* is derived from two Greek words meaning "arranged upon." If the grown film is the same material as the substrate, the process is termed *homoeptitaxy*. Homoeptitaxy is generally referred to as *epitaxy* or simply *epi* and these terms will be used interchangeably throughout this text. Homoeptitaxy of single crystalline silicon is the most important technological use of epitaxy, and is the primary subject of this chapter.

On the other hand, if the epitaxial film is grown on a substrate that is chemically different, the process is then termed *heteroeptitaxy*. The principal applications of heteroeptitaxy are in the deposition of silicon on sapphire (SOS) and in the fabrication of heterojunction semiconductor devices. When a heteroeptitaxial deposition is made on a substrate that has a lattice constant very different than that of the film, a strained layer can form near the film/substrate interface. If the deposited film is thin enough, the strain can be accommodated elastically, but if the film is too thick the strain becomes relaxed through the generation of defects (e.g., misfit dislocations). These defects are known to propagate from the interface into the device region where they can adversely affect device properties. Conversely, if the lattice mismatch is small (as in the case of the growth of silicon-germanium alloys on silicon substrates), the strain is accommodated elastically. Under these conditions the epitaxial growth is termed *pseudomorphic* growth. Pseudomorphic growth is the method used in the formation of silicon-heterojunction-bipolar transistors (HBTs). Figures 7-1a, 7-1b, and 7-1c show a schematic representation of homoeptitaxy, heteroeptitaxy (strain relieved), and pseudomorphic epitaxial growth, respectively.

Epitaxial growth can be achieved by depositing the film directly from either the vapor phase,

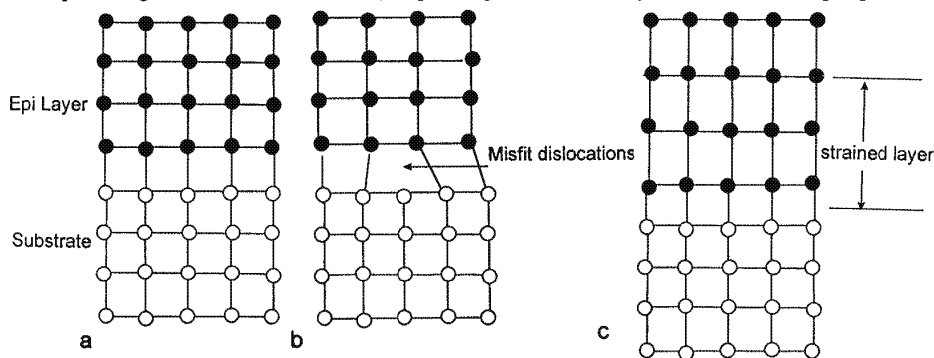


Fig. 7-1 Schematic of epitaxial structures: a) homoeptitaxy; b) strain relieved heteroeptitaxy (e.g., silicon-on-sapphire [SOS]); and c) pseudomorphic epitaxy.

the liquid phase, or the solid phase. These techniques are termed *vapor-phase epitaxy* (VPE), *liquid-phase epitaxy* (LPE), and *solid-phase epitaxy* (SPE), respectively. VPE is the predominant method used in silicon processing, since it provides a means of achieving excellent control of the film thickness, impurity concentration, and crystalline perfection. A disadvantage of VPE is that it requires relatively high temperatures (800–1150°C) in order to realize the necessary crystalline perfection. Such high-temperature processing can lead to the occurrence of *out-diffusion* and *autodoping*. These phenomena place a limitation on the ability to control the doping level in the epi layer and are discussed in detail in Section 7.4.4 of this chapter.

LPE has found its widest use producing epitaxial layers of III-V compounds (e.g., GaAs and InP). LPE, however, occurs during the re-freezing of molten layers of silicon on a silicon surface during the laser melting GILD process (see Chap. 9). SPE occurs during the crystalline re-growth that takes place during the low-temperature annealing of amorphous layers formed as a result of damage during high-dose ion implantation (see Chap. 10).

This chapter covers: 1) device applications of epitaxy; 2) fundamentals of epitaxial film growth; 3) epitaxial process considerations, including silicon precursors and doping effects; 4) defects in epitaxial layers; 5) pattern effects; 6) low-temperature epitaxy; 7) selective epitaxy; 8) epitaxial film characterization; and 9) silicon on insulators (SOI). The fundamentals of the kinetics and gas dynamics of CVD (epitaxial growth is a CVD process) are covered in detail in Chapter 6. In this chapter only the relevant results are repeated.

7.1 THE DEVICE APPLICATIONS OF EPITAXY

In the early days of semiconductor fabrication, epitaxial deposition was used to improve the performance of bipolar transistors that were then commonly used. By growing a lightly doped n -type epitaxial layer over a heavily doped n^+ substrate the bipolar device could be optimized for high breakdown voltage of the collector-substrate junction, while preserving a low collector resistance. The low collector resistance was required to improve the device operating speeds at moderate currents. Figure 7-2 depicts a cross-section of a high-speed oxide-isolated bipolar transistor showing the presence of the epitaxial layer. A key feature of bipolar epitaxy is that the film is deposited over patterned, n^+ -doped diffused layers called *buried layers* or *sub-collectors*. BiCMOS devices are also fabricated in epitaxial films deposited over buried layers.

More recently, epitaxial processes have been used to fabricate CMOS integrated circuits. In CMOS circuits the complete device is built in a thin (2–4 μm), lightly-doped p -type (or in some cases, intrinsic) epitaxial layer that is deposited over a uniformly heavily p^+ -doped substrate. Figure 7-3 shows a cross section of a twin-well CMOS device depicting the epi layer.

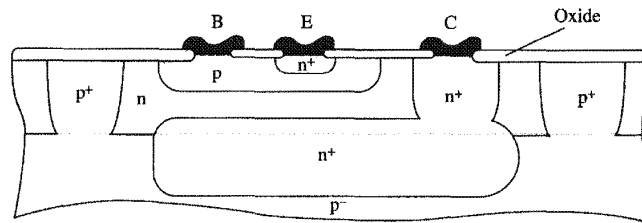


Fig. 7-2 Cross-section of a bipolar transistor built in an epitaxial layer. The light line indicates the boundary of the deposited n -type epi layer. Note that the n^+ -buried layer extends into the epi layer as a result of autodoping and out-diffusion.

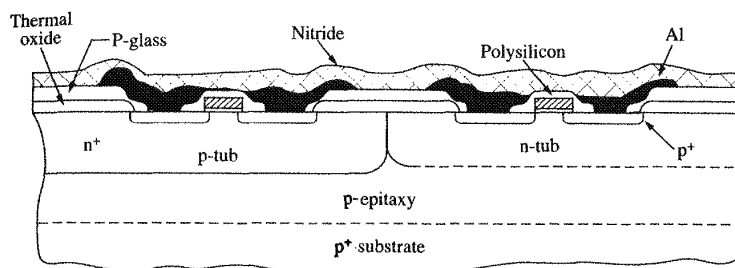


Fig. 7-3 Cross-section of a twin-well CMOS structure built in a p^- epitaxial layer and a p^+ substrate. Note that the p^+ -region extends into the epi layer as a result of autodoping and out-diffusion.

In the next section we discuss the reasons for using epitaxial silicon rather than *polished bulk wafers (PBW)* for constructing advanced CMOS devices. It is interesting to note that IC manufacturers usually purchase CMOS epitaxial wafers directly from the wafer suppliers, while for bipolar ICs they process the epitaxy themselves. The reason is that a masking layer is required to produce the buried layer prior to the epi in the bipolar process.

7.1.1. Why Are CMOS Epitaxial Wafers Used?

CMOS epitaxial wafers, when compared to polished bulk wafers provide: a) improved latch-up immunity; b) layers of silicon free of SiO_x precipitates, COPs, or vacancy condensates (all of which are formed during crystal growth); and c) a silicon surface that is smoother than that found on PWBs, with minimal surface damage.

Latch-up in CMOS circuits is a phenomenon that causes the formation of a low resistance path between the supply voltage and ground. As a result, it is possible for the circuit to draw an unusually high amount of current. Such current draw can cause the circuit to cease functioning or even to "burn-up." The device physics underlying latch-up is beyond the scope of this text, but is covered in detail in Vol. 2 of this series. Although there are process and design techniques that can minimize latch-up, the use of epitaxial silicon has become the "standard" approach to fabricating ULSI CMOS microprocessor circuits because it provides latch-up protection.

Polished bulk wafers are known to include SiO_x precipitates, COPs, and vacancy condensate defects at or near the wafer surface. Moreover, despite the best polishing techniques, the wafer surface can retain polishing defects such as micro-damage and surface roughness. Surface defects are known to diminish the gate-oxide integrity and increase junction leakage. Epitaxial layers, on the other hand, do not contain oxygen (hence no SiO_x precipitates), COPs, or vacancy condensates, since these defects only form during crystal growth (during which oxygen is dissolved in the as-grown Si crystal, see Chaps 1 and 2). Since epi is deposited on a polished wafer, the new surface that forms is generally free of polishing micro-damage and surface roughness. As a result, CMOS devices produced in epitaxial material have superior dielectric integrity and junction leakage currents, compared to similar devices made on polished wafers.

The use of epitaxial wafers in the fabrication of microprocessors is now standard, while its use in DRAM devices is rather limited. There are two reasons for this. First, the gate oxide thickness required for DRAM devices is generally thicker than that required for microprocessor devices, even for the same "generation" of technology. These thicker gate oxides are less susceptible to the presence of surface defects and do not benefit as much from the advantages of the epi layer. Second, the cost to purchase a 200-mm epitaxial wafer is about 1.5–1.8 times that of a polished wafer. Since low manufacturing costs for DRAMs are vital for profitability, the

Table 7-1 APPLICATIONS OF EPITAXY

Application	Thickness (μm)	Resistivity Range (ohm-cm)
Bipolar devices	0.8–1.6	0.5–4.0
CMOS devices	2–4	2–10
BiCMOS devices	3–5	2–20
High voltage devices	5–50	50–80

added cost per wafer is often too high to justify its use. However, the use of epi wafers for DRAM manufacturing is under serious consideration as thinner gate oxides become necessary. When the yields on devices fabricated in bulk wafers no longer meets the requirements for DRAM manufacturing, the industry may be compelled to change to epitaxial wafers. On the other hand, the DRAM manufacturers will try to find alternative processes to extend the life of bulk wafers, rather than pay the added cost associated with the use of epitaxial wafers.

- Table 7-1 shows some of the applications of silicon epitaxy along with the epi thickness and resistivity ranges that are commonly used. Table 7-2 (which is extracted from the SIA roadmap) shows the epi layer requirements for the most advanced CMOS devices.¹ The two key points illustrated in that table are: 1) thinner epi layers are required (i.e., down to 1 μm); and 2) the structural defect density must be reduced by more than a factor of 2 from its current level. These two discordant requirements represent a significant challenge, since thinner films require lower growth temperatures, and lower temperatures can lead to increased defect density.

7.2 GROWTH OF EPITAXIAL LAYERS

In this section an atomic mechanism that has been proposed to explain epi film growth is first discussed. Then the various chemicals precursors used in conventional epitaxial growth are described. The kinetics of CVD were covered in detail in Chap. 6, and only the results pertinent to epitaxial growth will be repeated here.

7.2.1 Atomistic Model of Film Growth

Whatever *precursor* (source gas) is used and whatever chain of reactions occur (see next section) the final reactant species must be adsorbed on the growing surface where the reaction takes place. The reaction produces silicon and some by-product. In order for film growth to occur, the silicon atoms must remain adsorbed on the surface and the by-products desorbed. The adsorbed silicon atoms are referred to as *adatoms*. If an adatom is in a position such as A in Fig. 7-4, one of several events can take place. If the adatom A remains in its position other silicon atoms can become attached to it and a small silicon cluster or island can form. If numerous clusters form and begin to grow, it is likely that as they merge, a highly defected or even polycrystalline film will form. However, as it turns out, adatoms in position A are quite mobile at the deposition

Table 7-2 EPITAXIAL LAYER REQUIREMENTS vs. TECHNOLOGY NODE

Extracted from NTRS, SIA (1997)¹

First year product shipment	1997	1999	2001	2003
Feature size (nm)	250	180	150	130
Layer thickness (μm)	2–5	2–5	2–4	2–4
Thickness tolerance ($\pm\%$)	5	4	4	4
Layer structural defect density (m^2)	≤ 3.3	≤ 2.9	≤ 2.6	≤ 2.3

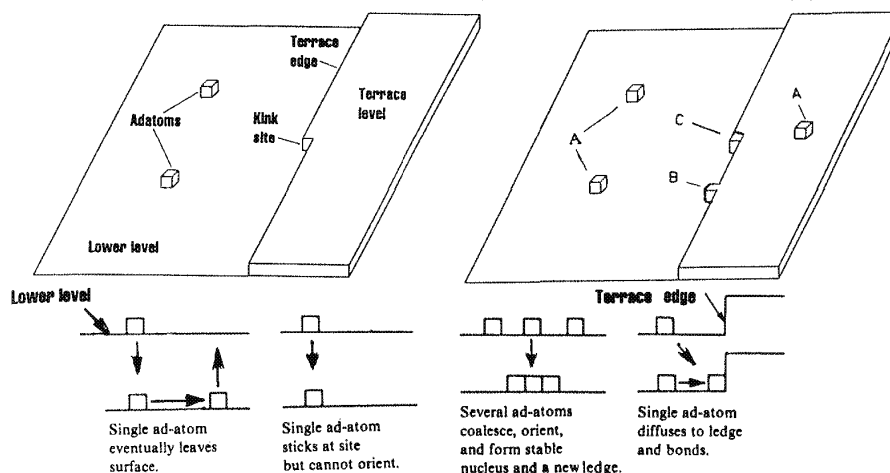


Fig. 7-4 Epitaxial growth model showing step-wise growth with adatoms in terrace positions A, adatoms at steps (or terrace edges) B, and adatoms at stable kink positions C.

temperatures and are likely to migrate along the surface. If a migrating adatom reaches a position along a growing *step* (or *terrace edge*), such as position B in Fig. 7-4, the adatom is more likely to remain in place (since atoms at position B are more energetically stable than at positions A). The stability arises from the fact that more Si-Si bonds have already formed when the adatom is at position B. The most energetically favored site for the adatom, however, is the so-called *kink position* (position-C in Fig. 7-4). When the adatom arrives at such a kink position, one-half of the Si-Si bonds can be established and further migration is thereafter unlikely to occur. For growth to continue, additional adatoms must migrate to kink positions and become incorporated in the growing film. In this respect, film growth proceeds by lateral movement (2-dimensional) of the steps on the lattice surface. After one layer is completed a second layer grows. Since epi proceeds by this lateral growth, an impurity sitting on the wafer surface can impede the motion and produce a stacking fault or dislocation defect in the film. For this reason, extremely clean silicon surfaces are required to achieve high-quality epi growth.

If adatom migration is suppressed during growth, a polycrystalline film is more likely to be deposited. Atom mobility is restricted by high deposition rates and low temperatures. At any particular deposition temperature there exists a maximum deposition rate above which polycrystalline films are deposited, but below which single crystal epitaxial films are formed.² Figure 7-5, shows a plot of the effect of growth rate and temperature on the formation of single (monocrystalline) or polycrystalline films. From that curve we observe that monocrystalline growth is favored at high temperatures and low growth rates, and polycrystalline deposition is favored under conditions of high growth rates and low temperatures. The maximum deposition rate at which single-crystal growth can be maintained is found to increase exponentially with temperature. When these results are plotted on an Arrhenius plot (Fig. 7-5) a straight-line dependence is obtained (indicative of a thermally activated process). The value of the activation energy extracted from this curve is ~ 5 eV. These results may be explained as follows. At high growth rates there is not sufficient time for the adatoms to migrate to the kink sites, thereby polycrystalline growth is favored. As the temperatures increase, however, the surface migration rate also increases, allowing time for silicon to reach the kink sites before additional adatoms form other clusters. Once at the kink site, the film continues to grow by lateral motion. The

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