

tively small 2D region. For example, the spatial region to be solved ranges from a few hundred micrometers to a few millimeters for the heat flow equations and from a few micrometers to a few ten micrometers for the device equations. Then, we propose to use a new quasi-3D temperature analysis for solving the heat flow equations in such wide region with a fast computational turn-around time, because it is a very time-consuming calculation to solve the complete 3D heat flow equations in the wide region according to the conventional method.

In this new temperature analysis, the cylindrical coordinates are employed for describing the radial heat flow. Furthermore, the doughnut and sector meshes are used in the regions except for the electrode regions and in the electrode regions, respectively. The device region is approximated by one small disk mesh which is placed in the center of the cylindrical coordinates. The dissipation power previously obtained is put into this small disk mesh when the heat flow equations are solved. Thus we can obtain the temperature distribution in the wide region. The average temperature in the device region is approximated by the temperature in the small disk mesh. Then, the device equations are again solved using this average device temperature according to the coupled Monte Carlo-energy transport analysis.

By using our new device simulator, we can accurately simulate the drain current reduction and the negative output resistance in the saturation region due to the temperature rise in the channel. In addition, it is found that such temperature rise is significantly influenced by the layout design rule such as the wiring width, the contact hole size, the gate-to-contact hole separation. Furthermore, it is revealed that the maximum electron temperature is reduced and consequently the drain breakdown voltage is increased due to the decreased number of hot carriers with higher energy when the temperature rise is taken into account.

*K. Yamaguchi is with Central Research Laboratory, Hitachi Ltd., Kohubunji, Tokyo 185, Japan.

[1] M. Koyanagi, H. Kurino, H. Kiba, H. Mori, T. Hashimoto, Y. Hiruma, T. Fujimori, Y. Yamaguchi, and T. Nishimura, in *IEDM Tech. Dig.*, 1991, pp. 45-48.

IIA-8 Electron Mobilities and High-Field Drift Velocities in Strained Silicon on Silicon-Germanium Substrates—Th. Vogelsang and K. R. Hofmann, Siemens AG, Corporate Research and Development, Otto-Hahn-Ring 6, D-8000 Munich 83, Germany (+49) 89 636 49784.

Recently, several research groups have reported very high electron mobilities in modulation-doped layers of strained Si pseudomorphically grown on relaxed $\text{Si}_{1-x}\text{Ge}_x$ buffers with values exceeding the bulk Si lattice mobility [1]–[4]. MODFET's of high transconductance utilizing such high mobility Si/ $\text{Si}_{1-x}\text{Ge}_x$ n-channels have been demonstrated and show considerable promise as Si-based

heterostructure devices with high-speed digital and analog applications [5]. For an evaluation of the performance potential of such devices not only low- but also high-field transport properties are essential. To this end we have performed a detailed analysis of the in-plane electron transport in strained Si on $\text{Si}_{1-x}\text{Ge}_x$ with a Monte Carlo method [6]. We present for the first time data on electron drift mobilities and velocities in the whole range from low to very high electric fields [7] that can serve as a reference for the transport in modulation-doped channels. Results on the temperature dependence of the mobility are compared to recent experimental data [1], [2].

The Monte Carlo transport simulations are based on the conduction band structure of pseudomorphic Si grown on $\text{Si}_{1-x}\text{Ge}_x$ (001) [8]. The tensile bi-axial strain raises the energy of the four conduction band minima on the in-plane $\langle 100 \rangle$ axes with respect to the two minima on the $\langle 001 \rangle$ axes normal to the plane by $\Delta E(\text{eV}) = 0.67 \cdot x$. These two minima have low effective transverse masses m_t suggesting improved in-plane transport. Semi-empirical pseudopotential band-structure calculations [9] have shown that to first order only the relative energy but not the shape of the valleys is changed. The transverse and longitudinal masses of the six ellipsoidal valleys deviate only marginally from the values $m_t = 0.19 \cdot m_e$ and $m_l = 0.92 \cdot m_e$ of unstrained Si; and ΔE is well described by the linear deformation potential theory [8]. Thus we retain these parameters including the non-parabolicity of the valleys. The following scattering processes were included: acoustic phonon intravalley scattering (inelastic scattering), f - and g -type optical phonon intervalley scattering, impact ionization, and ionized impurity scattering for an assumed background impurity density of 10^{14} cm^{-3} . As usual, the parameters for coupling strength of acoustic and optical phonon scattering E_1 and D_1K were determined by fitting the calculated velocity-field characteristic of unstrained Si to the experiments of [10]. Our model is based on the assumption that in the considered first-order approximation, all scattering parameters such as deformation potentials and matrix elements, except for the valley energy offset, are independent of the SiGe substrate composition. Thus no further fitting was necessary for the strained material calculations.

We investigated the electron drift velocities, mobilities, mean carrier energies, and valley populations for in-plane electric fields from 1×10^3 to $1 \times 10^5 \text{ V/cm}$, for temperatures between 300 and 50 K, and Ge contents of the substrate up to 40%. We found a substantial increase of both low-field mobility and of high-field drift velocity when the Ge content x of the substrate is raised from 0 to 40%. Both quantities saturate already at comparatively small x values. At room temperature, the low-field mobility increases from $1420 \text{ cm}^2/\text{V} \cdot \text{s}$ in unstrained Si to a saturated value of about $2000 \text{ cm}^2/\text{V} \cdot \text{s}$ at a Ge content of 30%. The high-field drift velocities show considerable improvement relative to unstrained Si, e.g., 16% at an intermediate field of $1 \times 10^4 \text{ V/cm}$ for 25% Ge, in the whole field range up to about $1 \times 10^5 \text{ V/cm}$, where they

saturate just above the unstrained Si saturation velocity 1×10^7 cm/s. The calculated low-field (1 kV/cm) drift mobility data agree very well (over the whole calculated temperature range) with the highest Hall mobilities measured by [1] and [2] on thin (15–20 nm) modulation-doped Si channels on relaxed $\text{Si}_{1-x}\text{Ge}_x$ ($x = 25\text{--}30\%$) buffers.

Our results demonstrate significant improvements of the in-plane electron drift velocity in strained Si on $\text{Si}_{1-x}\text{Ge}_x$ compared to bulk Si in the low-field and the high-field regions both at 300 and 77 K. This advantage should contribute considerably to the high-performance potential of devices based on modulation-doped Si/SiGe heterostructures such as n-channel quantum-well MODFET's and MOSFET's.

- [1] F. Schäffler *et al.*, *Semicond. Sci. Technol.*, vol. 7, p. 260, 1992.
- [2] Y. J. Mii *et al.*, *Appl. Phys. Lett.*, vol. 59, p. 1611, 1991.
- [3] J. C. Sturm *et al.*, private communication, Sept. 1991.
- [4] K. Ismail *et al.*, *Appl. Phys. Lett.*, vol. 58, p. 2117, 1991.
- [5] U. König *et al.*, *Electron. Lett.*, vol. 28, p. 160, 1992.
- [6] C. Jacoboni and L. Reggiani, *Rev. Mod. Phys.*, vol. 55, p. 645, 1983.
- [7] C. Smith and M. E. Jones, *Superlattices and Microstruct.*, vol. 4, p. 391, 1988, have reported calculations for mobilities in the low-field range.
- [8] R. People, *IEEE J. Quantum Electron.*, vol. QE-22, p. 1696, 1986.
- [9] M. Rieger, thesis, Technical University Munich (Prof. P. Vogl), 1991.
- [10] Canali *et al.*, *Phys. Rev. B*, vol. 12, p. 2265, 1975.

IIB-1 A New Single Electron Transistor—S. Y. Chou and Y. Wang, Department of Electrical Engineering, University of Minnesota, Minneapolis, MN 55455 (612) 625-1316.

We propose and demonstrate a new single-electron transistor (SET) where the drain current is controlled by a single electron. The new SET is similar to a GaAs/AlGaAs heterostructure modulation-doped FET, except that it has a split gate which electrostatically squeezes a 2D channel into a 1D channel, and it also has a nanoscale metal bar inside the gate gap to form a potential barrier in the 1D channel. At certain gate voltages, a single electron can be “stopped” inside the 1D channel by the potential barrier, and due to Coulomb repulsion this electron “blocks” the current flow from the source of the FET to the drain (Coulomb Blockade). Therefore, the drain current of the SET will oscillate with the gate voltage giving strong negative differential resistances, instead of being a linear function of gate voltage as that in a conventional FET operated in the linear regime.

The SET's with gate gaps of 50 and 100 nm were fabricated using MBE and ultra-high resolution e-beam lithography. As the gate voltage was swept at low temperatures, for a SET with a 50-nm gate gap, more than 10 periodic oscillation peaks in the drain current were observed before the onset of the first $2e^2/h$ plateau. Similar periodic conductance oscillations were observed in a SET with a 100-nm gate gap. The oscillation periods were 15 and 9 mV for devices with gate gaps of 50 and 100 nm, respectively. The oscillation peaks were so strong that they could be seen without the use of a lock-in amplifier,

and they persisted after thermal cycling and photon excitation. These oscillations were not observed in the FET's that have a split gate without a metal bar in the gate gap.

Further measurements showed that the oscillation period in the gate voltage corresponds to the gate voltage needed to put a single electron into the 1D channel. The shape of the oscillation peak can be well fitted by the derivative of the Fermi-Dirac distribution, indicating the peak width is caused by thermal broadening of a sharp energy level. A single electron blockade model was developed for the operation of the SET and agrees well with experimental observation.

IIB-2 Effects of Single Impurity Scattering on One-Dimensional Quantum-Effect Devices—C. C. Eugster, J. A. del Alamo, M. R. Melloch*, and M. J. Rooks,** Massachusetts Institute of Technology, Rm. 13-3018, Cambridge, MA 02139 (617) 253-4699.

The potential for increased functionality and for continued device scaling underly the optimism for the future of quantum-effect electronics. These electron-wave phenomena devices have shown very dramatic transport characteristics which could possibly be used in future circuits. However, in order for such practical applications to become a reality, the robustness of the individual devices against manufacturing defects and undesirable impurities must be well understood. Unfortunately, impurities will be most detrimental for one-dimensional (1D) structures which have recently shown very exciting and promising quantum effects. We report on dramatic changes in the 1D quantum-effect features if only a *single* impurity exists in the device.

A split-gate dual-electron waveguide device has recently demonstrated novel quantum-effect features in a variety of different implementations including two isolated 1D electron waveguides [1] and leaky 1D electron waveguides [2]. With such well-understood characteristics, it is an ideal structure to study imperfections in 1D electronic systems. Since these devices are implemented in very-high-mobility AlGaAs/GaAs heterostructures, only a small number of impurities exist in the intrinsic device area. Therefore, we are sometimes able to measure a device in which one waveguide contains only very few impurities while the other waveguide is impurity-free. Using such a device we can compare in detail variations between an ideal 1D waveguide and a nonideal 1D waveguide.

The signature of a clean split-gate dual-waveguide device is the observation of discrete $2e^2/h$ conductance steps for each waveguide as its electronic width is increased. The steps correspond to the opening of an additional propagation mode in the waveguide or, in a more electronic sense, the crossing of a subband through the Fermi level. A more unique feature of this device can be seen in the tunneling current leaking from the waveguides through the thin middle barrier. Here, we observe very strong oscil-