

Flexible Threshold Voltage FinFETs with Independent Double Gates and an Ideal Rectangular Cross-Section Si-Fin Channel

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Introduction

Recently, Double-gate (DG) MOSFETs [1] have been attracted intensive attentions as an emerging device in the ultimate scaled MOSFETs due to its excellent short-channel effects (SCEs) immunity. So far, a number of fin-type DG MOSFETs (FinFETs) [2-6] have been reported and its high performances have already been confirmed experimentally. The DG MOSFET is also characterized as a four-terminal device [7, 8]. To our knowledge, however, there has been no report of a threshold voltage (V_{th}) controllable FinFET in the short gate length regime. This paper demonstrates, for the first time, flexible threshold voltage 80 nm gate length FinFETs (FT-FinFETs) with independent double gates fabricated by using the newly developed orientation-dependent wet etching [6]. We also report the excellent experimental results of the V_{th} control by the second gate and the synchronized driving mode operation by the double gates.

Fabrication process

Three-dimensional schematic diagram of the proposed FT-FinFET and the fabrication process flow are shown in Fig. 1 and Fig. 2. First, heavily doped n^{++} source-drain (S-D) contact regions were formed with the same processes as described in Ref. 6. Then, nondoped silicate glass (NSG) and nitride (Si_3N_4) layers were deposited as shown in Fig. 2(a). The Fin pattern was shaped in parallel with the $\langle 112 \rangle$ direction by EB-lithography and the Si-Fin was formed by etching the (110) SOI layer with a 2.38 % tetramethylammonium hydroxide (TMAH) solution (Figs. 2(b) and 2(c)). After the 2.2-nm-thick gate oxide (t_{ox}) formation, the n^+ poly silicon (poly-Si) gate was made by using EB-lithography and RIE (Fig. 2(d)). Then, the PSG+NSG layers were deposited by LPCVD, and the n^+ doping for the S-D extension was performed by RTA. To separate the initial poly-Si gate region, the convex area at the cross-region of the poly-Si gate and Si-Fin was polished to the Si_3N_4 /NSG stopper layer by using a CMP process. Then, a 110-nm-thick NSG layer was deposited by LPCVD (Fig. 2(e)). Finally, the contact holes and aluminum electrodes were formed and sintered in a pure H_2 ambient at 400 °C for 30 min (Fig. 2(f)).

Results and discussion

Figures 3 and 4 show the SEM images of the fabricated FT-FinFET before and after the CMP. It can be confirmed that the CMP process was successfully stopped at the Si_3N_4 /NSG layer and the poly-Si gates were completely separated. The enlarged cross-sectional STEM image of the fabricated FT-FinFET is shown in Fig. 5. It is noteworthy that the Si-Fin shows an ideal rectangular channel shape. We define the left gate (G_1) as a driving gate and the

right gate (G_2) as a control gate. The measured I_d - V_{g1} and I_d - V_d characteristics of the FT-FinFET with the 43-nm-thick Si-Fin channel and 80-nm gate length (L_g) are shown in Figs. 6(a), 6(b) and 6(c). It is clear that the S-slope and off-state current are dramatically improved and the V_{th} is effectively changed in a positive direction, by applying V_{g2} from 0 to -1 V. The Si-Fin thickness (T_{si}) dependence of the subthreshold characteristics with V_{g2} as a parameter is experimentally shown in Fig. 7. It should be noticed that the V_{th} shift rate increases with reducing T_{si} . Both the experimental and simulated results of the V_{th} ($@ I_d = 10^{-6}$ A/ μ m, $V_d = 0.05$ V) and S-slope as a function of V_{g2} for the FT-FinFET with $T_{si} = 43$ nm and $L_g = 80$ nm are summarized in Fig. 8. The experimental data are in fairly good agreement with the simulated ones, especially at low $|V_{g2}|$ range. By adopting a proper metal gate, an optimal V_{th} with low $|V_{g2}|$ or 0 V can be obtained. Figure 9 shows the simulated results of the V_{th} and S-slope for the FT-FinFETs with asymmetric gate oxide thicknesses. It is remarkable that the S-slope is greatly improved with increasing t_{ox2} thickness in the low $|V_{g2}|$ region. Such asymmetric gate FT-FinFETs are now under development. The measured I_d - V_{g1} characteristics at the synchronized driving mode, (a) $V_{g2} = V_{g1}$, i.e., double-gate mode, (b) $V_{g2} = V_{g1} - 0.5$ V and (c) $V_{g2} = V_{g1} - 1$ V are shown in Fig. 10. It should be noticed that the S-slopes keep almost the same as that of the double-gate mode, but the V_{th} varies from -0.25 to 0.03 V by changing the gate voltage conditions from $V_{g2} = V_{g1}$ to $V_{g2} = V_{g1} - 1$ V. This is a unique feature of the independent double gates MOSFETs.

Conclusion

The FT-FinFETs with independent double gates and an ideal rectangular cross-section Si-Fin channel have successfully been fabricated by using newly developed orientation-dependent wet etching. The flexible V_{th} controllability by using one of the double gates as a control gate and by the synchronized driving mode operation is experimentally confirmed. The developed processes are attractive for the fabrication of the advanced separate-gates FinFET for a flexible function VLSI circuit.

References

- [1] T. Sekigawa et al., Solid-State Electronics, 27, 827 (1984).
- [2] D. Hisamoto et al., IEEE Trans. Electron Devices, 47, 2320 (2000).
- [3] J. Kedzierski et al., IEDM. Tech. Dig. 247 (2002).
- [4] B. Yu et al., IEDM. Tech. Dig. 251 (2002).
- [5] Y.-K. Choi et al., IEDM. Tech. Dig. 259 (2002).
- [6] Y. X. Liu et al., IEEE Electron Device Lett. 24, 484 (2003).
- [7] I. Y. Yang et al., IEEE Trans. Electron Devices, 44, 822 (1997).
- [8] D. M. Fried et al., DRC. Tech. Dig. 45 (2003).

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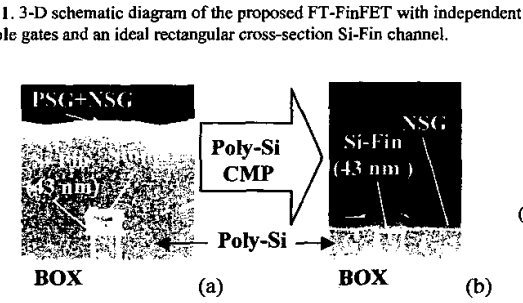
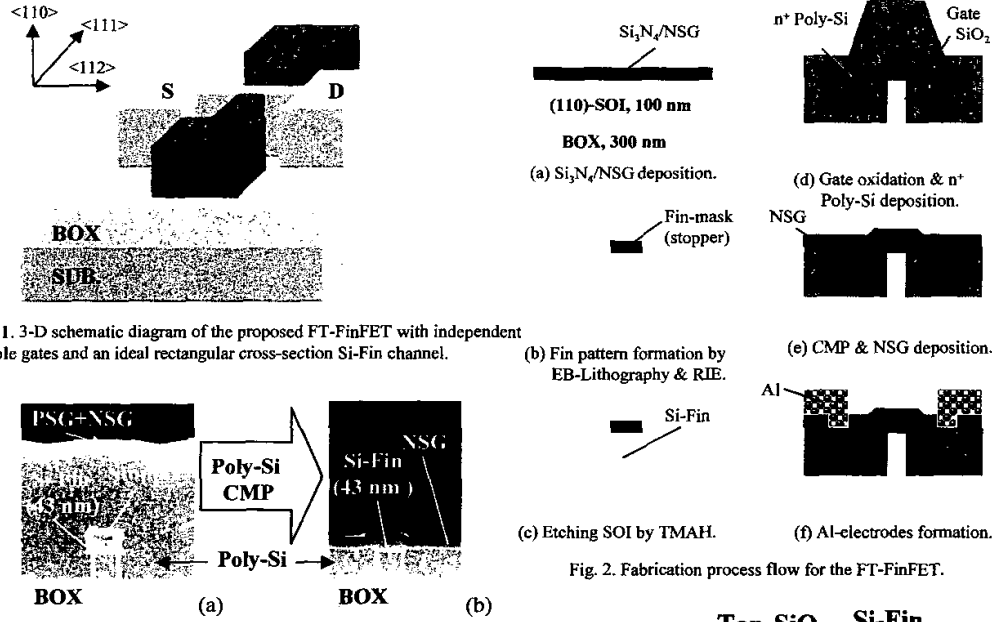
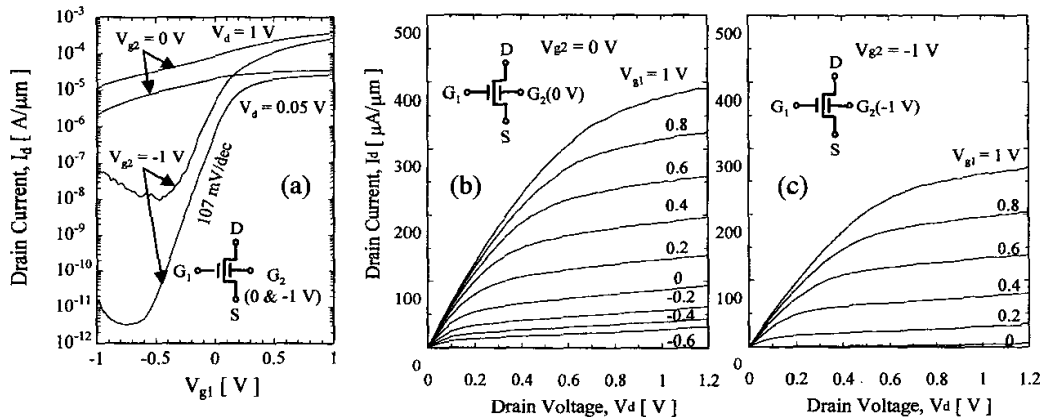
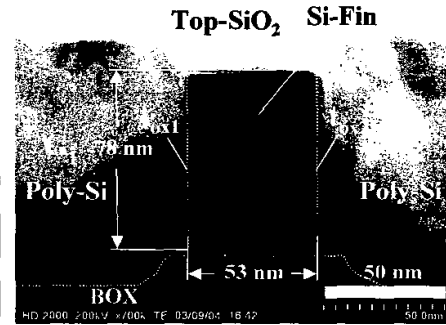
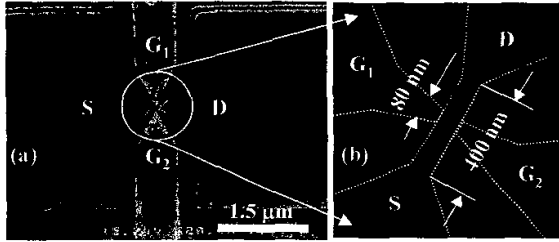


Fig. 3. Cross-sectional SEM images of the fabricated FT-FinFET. (a) before CMP, (b) after CMP and NSG deposition.



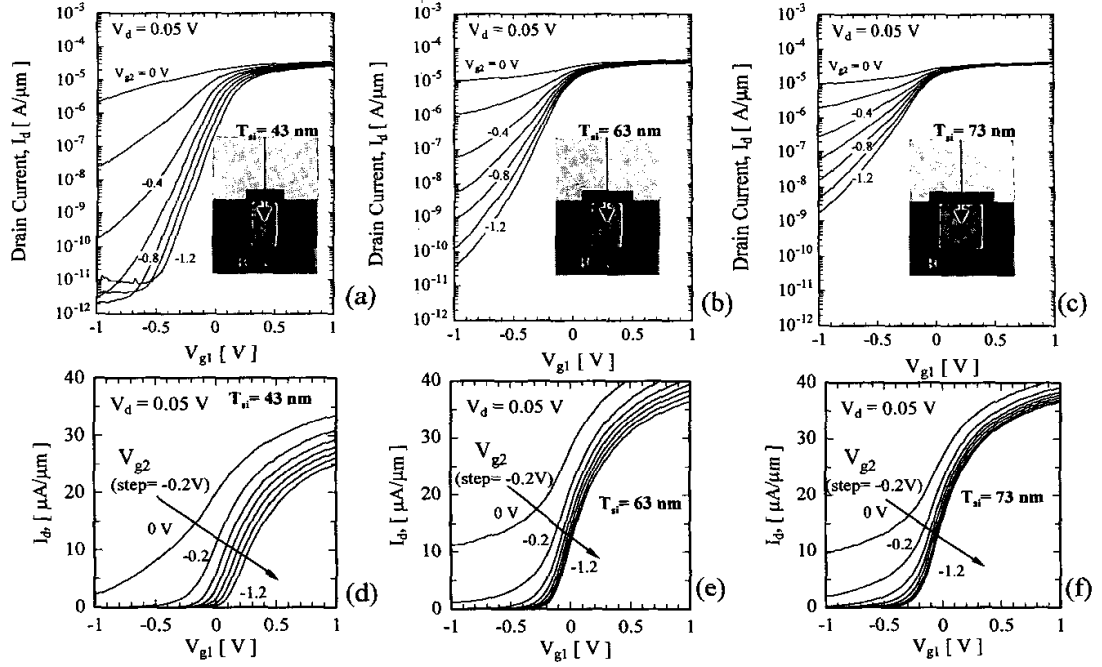


Fig. 7. I_d - V_{g1} characteristics of the fabricated FT-FinFETs with different Si-Fin thicknesses from 43 to 73 nm and with different V_{g2} . (a)-(c) log-scale and (d)-(f) linear-scale. The gate length for all devices is 80 nm. The V_{th} shift rate increases with reducing Si-Fin thickness.

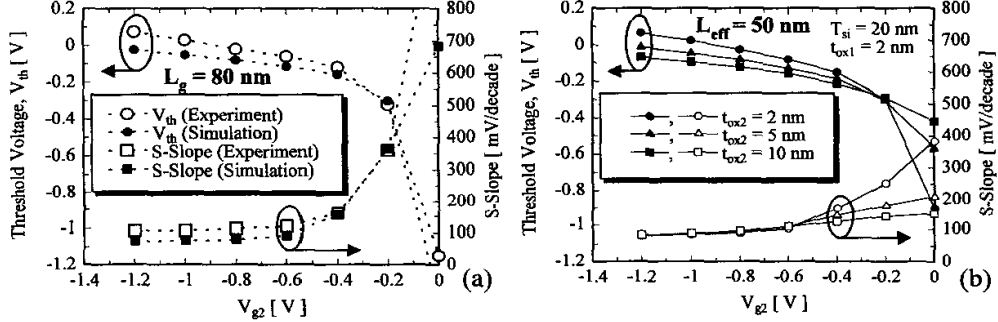


Fig. 8 (a). Experimental and simulated results of the V_{th} & S-slope as a function of V_{g2} for the FT-FinFETs.

Fig. 9 Simulated results of the V_{th} and S-slope for the FT-FinFETs with asymmetric gate oxide thicknesses.

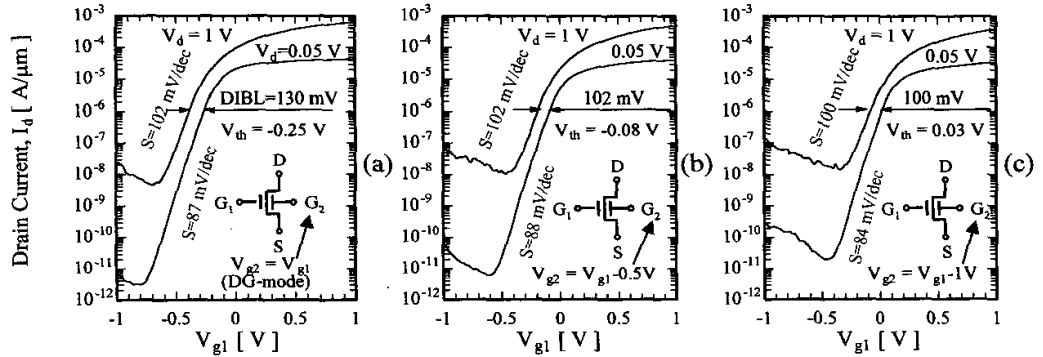


Fig. 10. Experimental I_d - V_{g1} characteristics of the fabricated FT-FinFET with $L_g = 80$ nm and $T_{si} = 43$ nm at the synchronized driving mode operation, (a) double-gate mode ($V_{g1} = V_{g2}$), (b) and (c) $V_{g2} = V_{g1} - 0.5$ V and $V_{g2} = V_{g1} - 1$ V. It is noteworthy that the S-slopes keep almost the same as that of the double-gate mode, but the V_{th} shifts from -0.25 to 0.03 V by changing the gate condition from $V_{g2} = V_{g1}$ to $V_{g2} = V_{g1} - 1$ V.