

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner,

v.

Marlin Semiconductor Limited,

Patent Owner.

U.S. Patent No. 6,888,181

Filing Date: March 18, 2024

Issue Date: May 3, 2005

Title: TRIPLE GATE DEVICE HAVING STRAINED-SILICON CHANNEL

Inter Partes Review No. IPR2025-01082

**DECLARATION OF DR. PAUL BRAUN IN SUPPORT OF PETITION FOR
INTER PARTES REVIEW OF UNITED STATES PATENT NO. 6,888,181**

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I, Dr. Paul Braun, Ph.D., declare as follows:

I. INTRODUCTION

1. I have been asked to submit this declaration on behalf of Taiwan Semiconductor Manufacturing Company Limited (“TSMC”) in connection with a petition for *inter partes* review of U.S. Patent No. 6,888,181 (“’181 Patent”), which I understand is being submitted to the Patent Trial and Appeal Board of the United States Patent and Trademark Office.

2. TSMC has retained me as a technical expert to study and provide my opinions on the technology covered by, and the patentability or non-patentability of, claims 1-10 of the ’181 Patent (“Challenged Claims”). Claims 1-10 of the ’181 Patent are included in attached Appendix B.

3. This declaration is directed to the Challenged Claims and sets forth certain opinions I have formed, the conclusions I have reached, and the basis for each.

4. Based on my experience, knowledge of the art at the relevant time, analysis of prior art references, and the understanding a person of ordinary skill in the art would have had regarding the claim terms in light of the specification, it is my opinion that each of the Challenged Claims of the ’181 Patent is unpatentable for at least the reasons I discuss below.

II. BACKGROUND AND QUALIFICATIONS

A. Education and Career

5. I have summarized in this section my educational background, career history, and other relevant qualifications.

6. I have over 30 years of academic and research experience in designing, applying, studying, teaching, and writing about semiconductor devices and semiconductor materials, including the design, process integration, and fabrication of various types of transistors.

7. I received a B.S. in Materials Science and Engineering from Cornell University with Distinction in 1993, and a Ph.D. in Materials Science and Engineering from the University of Illinois Urbana-Champaign in 1998.

8. From 1998 to 1999, I worked as a postdoctoral scientist for the Department of Condensed Matter Physics Research at Bell Laboratories. During my time there, I discovered how to micropattern silicon, selenium, polymer, and II-VI semiconductor photonic and microelectronic devices and grow 3D photonic crystals. I also developed a process suitable for reel-to-reel production of high-performance organic field effect transistors (FETs) and circuits.

9. Since 1999, I have served as a professor in the Department of Materials Science and Engineering at the University of Illinois Urbana-Champaign, starting as an assistant professor and progressing to my current role as the Grainger

Distinguished Chair in Engineering and Director of the Materials Research Laboratory. In these roles, I conducted fundamental research in semiconductor materials and devices, including on materials used in FETs. This research included investigating the properties of various semiconductor materials, including silicon, germanium, Cu_2O , and III-IV materials including GaAs, GaInP, InGaAs, and AlGaAs. Of specific relevance to this case, my research involves epitaxial growth of semiconductor heterostructures on silicon and other materials, selective area epitaxy of compound semiconductors, and semiconductor p-n junctions. I have grown both silicon and germanium (including silicon and germanium thin films) via chemical vapor deposition (the key growth method for growing strained silicon on silicon germanium (“SiGe”) cores).

10. The discovery that strain induced by epitaxially growing Si on SiGe increases the mobility of electrons in the Si was recognized by at least 1992. *See, e.g.,* TSMC-1019. The use of epitaxial silicon in channel regions to strain the channel in FETs, was technology developed by at least the year 1992 (about 12 years before the earliest claimed priority date for the '181 Patent). During my time as a professor (and assistant professor) at the University of Illinois Urbana-Champaign, I have studied and taught these well-known technologies. My accomplishments have resulted in my election as a Fellow of the Materials Research Society, the

National Academy of Inventors, the American Association for the Advancement of Science, and the American Academy of Arts and Sciences.

11. A full list of my research and professional experience, my expert witness or consultant experience, and other activities and awards is further detailed in my curriculum vitae, attached as Appendix C.

12. As a professor and inventor myself, I am familiar with patents, the patent process, patent claims, and patent analysis.

B. Publications

13. I am a named inventor on over 34 granted United States patents and have authored over 355 peer-reviewed academic journal publications. Some examples of relevant patents and/or publications to the technology at issue in this proceeding are:

Patents:

1. Paul V. Braun, Michael L. Steigerwald and Pierre Wiltzius, “Electrochemical process for fabricating article exhibiting substantial three-dimensional order and resultant article.”, Patent No. 6,409,907 issued June 25, 2002.
2. Paul V. Braun, James J. Coleman, Victor C. Elarde, Erik C. Nelson, and Varun B. Verma, “Porous Device for Optical and Electronic Applications and Method of Fabricating the Porous Device,” Patent No. 8,222,988 issued July 17, 2012.

3. Paul V. Braun, Hui Gang Zhang and Xindi Yu, “Porous Battery Electrode for a Rechargeable Battery and Method of Making the Electrode,” Patent No. 8,237,538, issued August 7, 2012.
4. Shailesh N. Joshi, Naoya Take, Paul Braun, Julia Kohanek, Gaurav Singhal, “Methods of Forming Power Electronic Assemblies Using Metal Inverse Opals and Cap Structures,” Patent No. 10,818,576 issued October 27, 2020.
5. Lynford L. Goddard, Kimani C. Toussaint, Paul V. Braun, Jinlong Zhu, Daniel Bacon-Brown, Christian H. Ocier, Qing Ding, Corey Richards, “Volumetric Optical Integrated Circuits,” Patent No. 11,232,7343 issued February 1, 2022.

Publications:

1. S. I. Stupp and P. V. Braun: Molecular manipulation of microstructures: biomaterials, ceramics, and semiconductors, *Science*, 277, 1242-1248 (1997).
2. J. A. Rogers, Z. Bao, A. Makhija and P. Braun: Printing process suitable for reel-to-reel production of high-performance organic transistors and circuits, *Advanced Materials*, 11, 741-745 (1999).
3. P. V. Braun and P. Wiltzius: Electrochemically grown photonic crystals, *Nature*, 402, 603-604 (1999).
4. P. V. Braun and P. Wiltzius: Electrochemical Fabrication of 3-D Microperiodic Porous Materials, *Advanced Materials*, 13, 482-485 (2001).

5. P. V. Braun, R. W. Zehner, C. A. White, M. K. Weldon, C. Kloc, S. S. Patel and P. Wiltzius: Epitaxial growth of high dielectric contrast three-dimensional photonic crystals, *Advanced Materials*, 13, 721-724 (2001).
6. P. V. Braun and P. Wiltzius: Macroporous materials – electrochemically grown photonic crystals, *Current Opinion in Colloid and Interface Science*, 7, 116-123 (2002).
7. G. M. Gratson, F. García-Santamaría, V. Lousse, M. Xu, S. Fan, J. A. Lewis, and P. V. Braun: Direct-Write Assembly of 3D Photonic Crystals: Conversion of Polymer Scaffolds to Silicon Hollow-Woodpile Structures, *Advanced Materials*, 18, 461-465 (2006).
8. F. García-Santamaría, M. Xu, V. Lousse, S. Fan, P. V. Braun and J. A. Lewis: A germanium inverse woodpile structure with a large photonic band gap, *Advanced Materials*, 19, 1567-1570 (2007).
9. S. A. Rinne, F. Garcia-Santamaria & P. V. Braun: Embedded cavities and waveguides in three-dimensional silicon photonic crystals, *Nature Photonics*, 2, 52-56 (2008)
10. V. Ramanan, E. Nelson, A. Brzezinski, P. V. Braun and P. Wiltzius: Three dimensional silicon-air photonic crystals with controlled defects using interference lithography, *Applied Physics Letters*, 92, 173304 (1-3) (2008).

- 11.E. C. Nelson and P. V. Braun: Photons and electrons confined, *Nature Photonics*, 2, 650-651 (2008).
- 12.D. Shir, E.C. Nelson, Y.C. Chen, A. Brzezinski, H. Liao, P.V. Braun, P. Wiltzius, K.H.A. Bogart, and J.A. Rogers: Three dimensional silicon photonic crystals fabricated by two photon phase mask lithography, *Applied Physics Letters*, 94, 011101-1 (2009).
- 13.M. Miyake, Y.-C. Chen, P. V. Braun and P. Wiltzius: Fabrication of three-dimensional photonic crystal using multi-beam interference lithography and electrodeposition, *Advanced Materials*, 21, 3012-3015 (2009).
- 14.D. J. Shir, E. C. Nelson, D. Chanda, A. Brzezinski, P. V. Braun, P. Wiltzius and J. Rogers: Dual exposure, two-photon, conformal phasemask lithography for three dimensional silicon inverse woodpile photonic crystals, *Journal of Vacuum Science and Technology*, 28, 783-788 (2010).
- 15.S.-G. Park, M. Miyake, S.-M. Yang and P. V. Braun: Cu₂O Inverse Woodpile Photonic Crystals by Prism Holographic Lithography and Electrodeposition, *Advanced Materials*, 23, 2749-2752 (2011).
- 16.E.C. Nelson, N. Dias, K. Bassett, S. Dunham, V. Verma, M. Miyake, P. Wiltzius, J. Rogers, J. Coleman, X. Li and P.V. Braun: Epitaxial growth of three-dimensionally architected optoelectronic devices, *Nature Materials*, 10, 676-681 (2011). (cover) DOI: 10.1038/NMAT3071

- 17.J. Ma, B.R. Parajuli, M.G. Ghossouh, A. Mihi, J. Sadhu, P.V. Braun and S. Sinha: Coherent Phonon-Grain Boundary Scattering in Silicon Inverse Opals, *Nano Letters*, 13, 618-624 (2013). DOI: 10.1021/nl304190s
- 18.J. Kim, H. Kim, J.-H. Choi, H. Jeon, Y. Yoon, J. Liu, J.-G. Park and P.V. Braun, Epitaxial Growth of Three-Dimensionally Mesostructured Single Crystalline Cu₂O via Templated Electrodeposition, *Chemistry of Materials*, 26, 7051-7058 (2014). DOI: 10.1021/cm5034645
- 19.Q. Zheng, H. Kim, R. Zhang, M. Sardela, J.-M. Zuo, B. Manavaimaran, S. Lourdudoss, Y.-T. Sun and P.V. Braun, Epitaxial growth of three dimensionally structured III-V photonic crystal via hydride vapor phase epitaxy, *Journal of Applied Physics*, 118, 224303 (2015). DOI: 10.1063/1.4937273
- 20.J.H. Choi, J. Kim, H. Yoo, J. Liu, S. Kim, C.-W. Baik, C.-R. Cho, J.G. Kang, M. Kim, P.V. Braun, S. Hwang and T.-S. Jung, Heteroepitaxial Growth of GaN on unconventional templates and layer-transfer for large-area, flexible or stretchable light-emitting diodes, *Advanced Optical Materials*, 4, 505-521 (2015). DOI: 10.1002/adom.201500526
- 21.K.W. Tan, J. Werner, M. Goodman, H.S. Kim, B. Jung, H. Sai, P.V. Braun, M. Thompson and U. Wiesner, Synthesis and Formation Mechanism of All-Organic Block Copolymer-Directed Templating of Laser-Induced Crystalline

Silicon Nanostructures, *ACS Applied Materials & Interfaces*, 10, 42777-42785 (2018). DOI: 10.1021/acsami.8b12706

22.S. Kim, B. Lee, J. T. Reeder, S.H. Seo, S.U. Lee, A. Hourlier-Fargette, J. Shin, Y. Sekine, H. Jeong, Y.S. Oh, A.J. Aranyosi, S.P. Lee, J.B. Model, G. Lee, M.H. Seo, S.S. Kwak, S. Jo, G. Park, S. Han, I. Park, H.I. Jung, R. Ghaffari, J. Koo, P.V. Braun, and J.A. Rogers, Soft, skin-interfaced microfluidic systems with integrated immunoassays, fluorometric sensors and impedance measurement capabilities, *Proceedings of the National Academy of Sciences*, 117, 27906-27915 (2020). DOI: 10.1073/pnas.2012700117

23.A.J. Littlefield, J. Huang, M.L. Holley, N.B. Duggar, J. Gao, D. Xie, C.A. Richards, T. Silberg, U. Purakayastha, J. Herr, C.R. Ocier, X. Deng, X. Wang, P.V. Braun, and L.L. Goddard, Low loss fiber-coupled volumetric interconnects fabricated via direct laser writing, *Optica*, 11, 7, 995-1007 (2024). DOI: 10.1364/OPTICA.525444

C. Compensation

14. I am being compensated for services provided in this matter at my standard consulting rate. I am also being reimbursed for expenses that I incur during the course of my work in this matter. My compensation is not contingent upon the results of my study or analysis, the substance of my opinions, or the outcome of any

proceeding involving the Challenged Claims. I have no financial interest in the outcome of this matter or in any litigation involving the '181 Patent.

III. MATERIALS REVIEWED

15. In forming my opinions regarding the '181 Patent, I reviewed the materials discussed in this declaration, including the references listed in Appendix A. All citations to materials in Appendix A in this declaration are to the page number of the original reference, not the stamped exhibit page numbers.

IV. LEGAL STANDARDS

16. I am not an attorney and have not been asked to offer my opinion on the law. However, as an expert offering an opinion on whether the claims in the '181 Patent are patentable, I understand that I am obliged to follow existing law.

A. Anticipation

17. I understand the following legal principles apply to analysis of patentability pursuant to 35 U.S.C. §102, a provision in the patent law regarding anticipation. I understand that, in *inter partes* review proceedings, a patent claim may be deemed unpatentable for anticipation if it is shown by preponderance of the evidence (i.e., it is more likely than not) that the claim was anticipated by a prior-art patent or publication.

18. I understand that for a claim to be anticipated, every limitation of the claimed invention must be disclosed by a single prior-art reference, viewed from the perspective of a person of ordinary skill in the art.

B. Obviousness

19. I understand that under 35 U.S.C. §103(a), “[a] patent may not be obtained though the invention is not identically disclosed or described as set forth in §102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” I understand that, in inter partes review proceedings, a patent claim may be deemed unpatentable if it is shown by preponderance of the evidence (i.e., it is more likely than not) that it would have been obvious.

20. When considering the issues of obviousness, I understand that I am to do the following:

- a. Determine the scope and content of the prior art;
- b. Ascertain the differences between the prior art and the claims at issue;
- c. Resolve the level of ordinary skill in the pertinent art; and
- d. Consider evidence of secondary indicia of obviousness or non-obviousness (if available).

21. I understand that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of alleged invention, which I have been asked to assume is just before the earliest claimed priority date of the '181 Patent (i.e., March 18, 2004).

22. I understand that obviousness is a determination of law based on underlying determinations of fact. I understand that these factual determinations include the scope and content of the prior art, the level of ordinary skill in the art, the differences between the claimed invention and the prior art, and any objective indications of obviousness or non-obviousness that may exist (although I am not aware of any objective indications of non-obviousness relating to the '847 Patent).

23. I understand that a prior-art reference may be combined with one or more other references and/or the knowledge of a person of ordinary skill in the art to show obviousness. I also understand that a person of ordinary skill in the art is presumed to know all relevant prior art. I understand that the obviousness analysis may account for the inferences and creative steps that a person of ordinary skill in the art would have employed at the time of invention.

24. In determining whether the teachings contained in one prior-art reference would have been combined with the teachings contained in another reference or information known to a person of ordinary skill in the art, I understand

that the following principles may be considered, and I have been asked to consider them:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;
- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;
- d. The application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;
- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and
- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

25. I understand that whether a prior art reference renders a patent claim unpatentable as obvious is determined from the perspective of a person of ordinary skill in the art. I understand that there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, but a suggestion to combine known elements to achieve the claimed invention may come from the prior art, as filtered through the knowledge of one skilled in the art. In addition, I understand that the inferences and creative steps a person of ordinary skill in the art would have employed are also relevant to the obviousness inquiry.

26. I understand the reasons a person of ordinary skill in the art would have wanted to modify teachings available in the prior art teachings do not need to match the inventor's reasons for making the claimed invention. In determining whether the subject matter of a patent claim is obvious, I understand that what matters is the objective reach of the claim and whether it covers an obvious variation of the prior art. I understand it would be improper to consider only the specific problem the patentee was trying to solve.

27. I understand that when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I understand that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation was likely to have been obvious. I understand that in many fields, there

may be little discussion of obvious combinations, and, in these fields, market demand, not scientific literature, may drive design trends. I understand that when there was a design need or market pressure and there were a finite number of predictable solutions, a person of ordinary skill in the art would have had good reason to pursue those known options.

28. I understand that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine them. But I also understand that any “teaching, suggestion, or motivation” present in the prior art may be useful in establishing a rationale for combining aspects of the prior art. I understand this “teaching, suggestion, or motivation” test poses the question as to whether the prior art contains an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

29. I understand that a claimed invention may be obvious even when the prior art does not teach each claim limitation, so long as the record contains some reason why a person of ordinary skill in the art would have applied the prior art to obtain the claimed invention.

30. I understand that when there is a known technique to address a known problem using prior art elements according to their established functions, then a person of ordinary skill in the art would have had a motivation to combine.

31. I understand that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I understand that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address; or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

V. LEVEL OF ORDINARY SKILL IN THE ART

32. I understand that a person of ordinary skill in the art (“person of ordinary skill in the art”) is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

33. I understand that I am to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

34. In my opinion, a person having ordinary skill in the art in reference to the '181 Patent would have had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work or research experience in semiconductor manufacturing, including FETs. Additional

graduate education could substitute for work experience, and additional work experience/training could substitute for formal education.

35. I have not analyzed the priority date of the '181 Patent, but I note that the earliest claim of priority listed on the face of the '181 Patent is its filing date, March 18, 2004. Because all the prior art discussed in this declaration predates March 18, 2004, I have been asked for simplicity to treat **March 18, 2004**, as the priority date for the '181 Patent. I have also treated this date as the date from which to assess the knowledge available to a person of ordinary skill in the art.

VI. TECHNOLOGY BACKGROUND

36. In my opinion, all the elements of the claims in the '181 Patent were well known before March 18, 2004. For example, as explained below, FinFETs were invented by at least 1999. Further, SiGe/Strained Silicon technology was also well-known prior to March 18, 2004.

37. A person of ordinary skill in the art in the timeframe relevant to the '181 Patent would have been familiar with the background information described in subsections A through C below.

A. Planar Field Effect Transistor (FET) vs. Three-Dimensional Fin FET (FinFET) Transistor

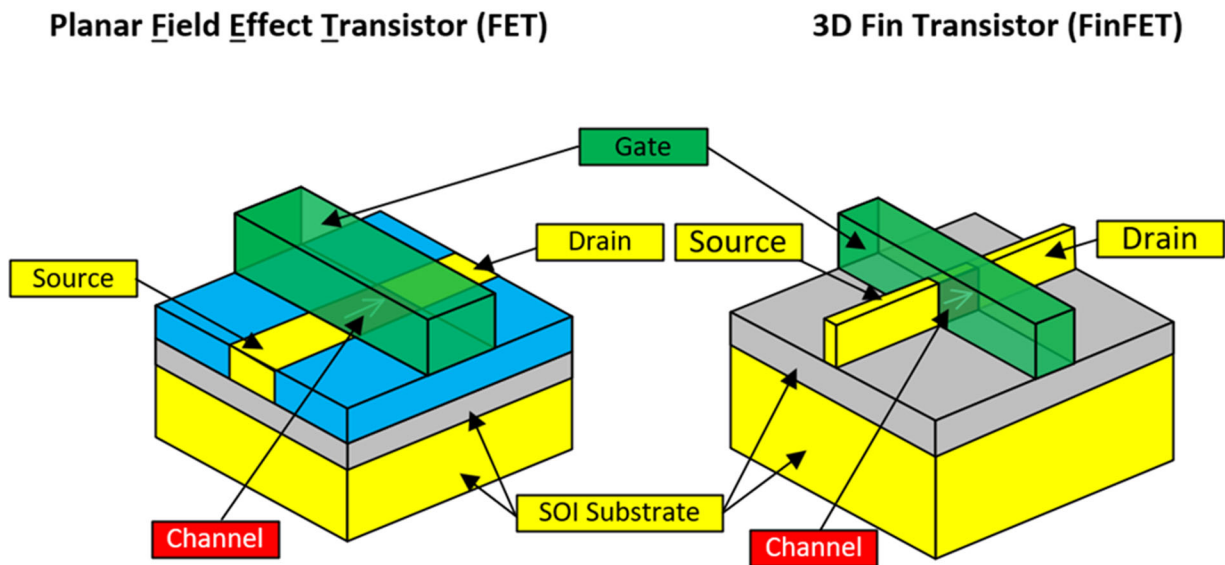
38. Transistors are the building blocks for semiconductor chips. By combining huge numbers of transistors together, circuit designers can implement

electronic hardware like processors used in computers and mobile phones. There are often billions of transistors within a single semiconductor chip.

39. A field effect transistor (“FET”) includes three components: a “source,” a “drain,” and a “gate” that allow the transistor to operate as a switch by either allowing or preventing electrical current from flowing. When the transistor is “off,” no current flows from the source to the drain. When turned “on,” current flows between the source and drain regions through a “channel” under the gate.

40. The figures below illustrate two types of FETs that were commonly used by the semiconductor industry by 2004: a planar FET and a non-planar, three-dimensional “FinFET.” Traditional planar FETs are built into the surface of a semiconductor substrate. A planar FET generally utilizes a two-dimensional structure in which the gate, source, and drain terminals are oriented in the same plane. By contrast, in a non-planar, three-dimensional FinFET, the channel is embodied within a three-dimensional fin structure that is raised above and thus extends three-dimensionally beyond a supporting substrate where the gate covers the top and both sides of the fin structure. For a silicon-on-insulator device, the FinFet extends three-dimensionally from an insulating layer of the substrate. As such, the gate, source, and drain terminals are not all oriented in the same plane. Non-planar, three-dimensional FinFET designs offered various advantages over planar FETs, including reducing parasitic resistance while facilitating large-scale integration and

local interconnection. *See* TSMC-1012, 1; TSMC-1013, 1. An example planar FET is shown beside an example 3D FinFET below:



41. The operation of both types of FETs is generally the same, as is the underlying physics. And except for forming the fin shape in the latter, their fabrication is also generally the same. *See* TSMC-1011, Abstract, 2:11-14, 5:37-40; TSMC-1012, 1.

B. Multi-Gate Technology

42. FinFET devices have long utilized various multi-gate structures, such as triple gates, etc., to impart gate voltages on multiple sides of the channel region. *See* TSMC-1008, ¶[0006]; TSMC-1009, ¶¶[0044]-[0047], Figs. 8A-8F; *see* TSMC-1001, 1:14-16, 1:37-39 (acknowledging, under heading “Description of the Prior Art,” that “[t]hree dimensional (3D) vertical double-gate transistors are known in the

art” and involve forming a fin with a gate “wrapped around and over the fin”). In this way, the channel width of the FinFET is dramatically increased, enabling a much higher driving current as compared to traditional planar FETs having single gate structures. *See* TSMC-1008, ¶[0006]; TSMC-1004, 2:9-18; TSMC-1013.

43. A “double gate” refers to a gate that is formed on at least two sides of the channel region. *See* TSMC-1004, 12:26-30; TSMC-1009, ¶[0047]. A “triple gate” is formed on at least three sides of the channel region, and a “quadruple gate” is formed on all four sides of the channel region. *See* TSMC-1009, ¶[0046]; TSMC-1013, 1. Prior to the ’181 Patent, and indeed as acknowledged by the ’181 Patent, three-dimensional FinFET devices utilizing triple gate structures were well-known in the art. *See, e.g.*, TSMC-1004, 12:26-30 (“The double gate 103 is actually a ***triple gate*** because it covers both sides and the top of the strained silicon channel 104. The term ‘double gate’ in the context of the present invention is a generic term to mean ‘more than one gate’ and therefore covers double or triple gate device.”); TSMC-1007, Title (“***Tri-gate devices*** and methods of fabrication”), TSMC-1009, ¶[0046] (“FIG. 8C represents a ***triple gate*** FinFET 92, wherein a triple gate 97 is formed over the thin oxide layer 33, which is disposed over the channel 16 (shown in FIGS. 8A-B).”); TSMC-1013, Abstract (“Fully-depleted (FD) ***tri-gate*** CMOS transistors with 60 nm physical gate lengths on SOI substrates have been fabricated.”). Further, prior to the ’181 Patent, it was known in the art that such triple gate structures exhibit

improved performance including superior short channel characteristics while maintaining full depletion at larger channel region dimensions as compared to planar FETs with single gate structures. *See* TSMC-1013, Abstract (“Fully-depleted (FD) tri-gate CMOS transistors with 60 nm physical gate lengths on SOI substrates have been fabricated. These devices consist of a top and two side gates on an insulating layer. The transistors show near-ideal subthreshold gradient and excellent drain-induced barrier lowering (DIBL) behavior, and have drive current characteristics greater than any non-planar devices reported so far, for correctly-targeted threshold voltages. The tri-gate devices also demonstrate full depletion at silicon body dimensions approximately 1.5–2 times greater than either single gate SOI or non-planar double-gate SOI for similar gate lengths, indicating that these devices are easier to fabricate using the conventional fabrication tools.”); TSMC-1007, ¶¶[0016]-[0017].

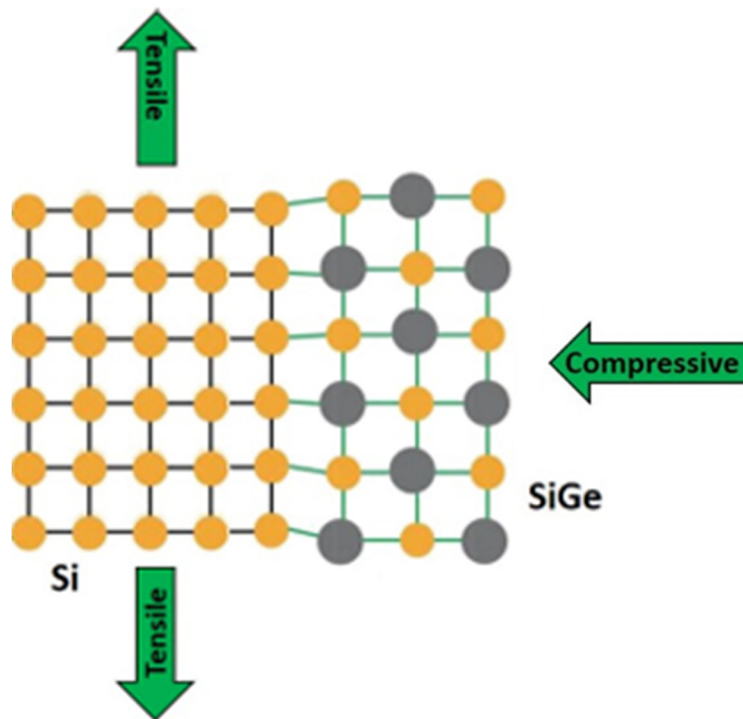
44. Accordingly, prior to the '181 Patent, a POSITA was familiar with FinFET devices with triple gate (and other multi-gate) structures and understood their associated benefits and characteristics vis-à-vis other gate and planar FET configurations.

C. Strained Silicon Technology to Improve Channel Carrier Mobility, to Increase Drive Current

45. Imparting strain to the silicon channel to improve carrier mobility and thereby increase drive current across a fin structure was also well-known prior to the '181 Patent. *See, e.g.*, TSMC-1009, ¶¶[0004]-[0006], [0044] (“[S]tretching the crystalline lattice structure of silicon can speed the flow of electrons through a transistor, thereby enhancing performance and decreasing power consumption.”); TSMC-1004, 1:66-2:8 (“Generally speaking, a compressive strained channel MOSFET has significant hole mobility enhancement, and a tensile strained channel MOSFET achieves both significant hole and electron mobility enhancement. Enhanced carrier mobility allows strained silicon MOSFET devices to exhibit vastly increased performance over their bulk silicon counterparts at identical gate lengths.”); TSMC-1008, Abstract (“Strained silicon has an increased carrier mobility compared to relaxed silicon, and as a result the epitaxial strained silicon provides increased carrier mobility in the FinFET. A higher driving current can therefore be realized in a FinFET employing a strained silicon channel layer.”), ¶[0029] (“As a result, carrier mobility is dramatically increased in strained silicon as compared to relaxed silicon, offering a potential increase in mobility of 80% or more for electrons and 20% or more for holes.”). The increased carrier mobility and drive current enhances performance and decreases power consumption of the FET.

46. One well-known example of strained silicon involves using the strained silicon in combination with adjacent silicon germanium layers. *See, e.g.*, TSMC-

1009, ¶¶[0004]-[0006], [0044]. The lattice constant mismatch between silicon and silicon germanium compounds results in straining/stretching of the silicon atoms in the silicon layer. *Id.* As shown below, SiGe semiconductor compounds (“Si_xGe_{1-x}” or, more briefly, “SiGe”) have a larger lattice spacing than silicon (*see, e.g.*, TSMC-1015); TSMC-1016, 1:64-2:13, 4:32-39; TSMC-1017, 3:1-16, 4:12-22; TSMC-1008, ¶[0029]):



47. A lattice mismatch between the Si and SiGe atoms causes stretching and/or compressing of the mismatched structures along a planar interface of the mismatch. TSMC-1009, ¶[0005]. As a result, when a silicon layer is grown on an SiGe surface, such as by using epitaxial growth of the silicon layer, this combination of components results in large tensile and compressive stresses developing and

straining the silicon in the channel region of the transistor. The strain allows charge carriers to move much more quickly from source to drain. This is known as enhanced “channel mobility” or “charge carrier mobility.” Accordingly, the strained silicon enhances electron/hole mobility and thus driving current and the ultimate operating speed of the FinFET. TSMC-1009, ¶[0006]; TSMC-1017, 7:64-8:9 (“The electron mobility of strained Si is increased by an effect that the strain exerts the band structure. Since the hole mobility of Ge is higher than that of Si, the hole mobility of the SiGe is higher than that of Si. These facts mean that the CMOSFET of the present invention that the channel region of the n-channel MOSFET is made of strained Si and the channel region of the p-channel MOSFET is made of SiGe has high current drive power and is excellent in circuit performance. In the CMOSFET of the present invention, strained Si is used for the channel of the n-channel MOSFET and SiGe is used for the channel of the p-channel MOSFET, so the threshold voltage can be decreased, and the other performance of the semiconductor device can also be increased.”); *see also* TSMC-1017, 7:64-8:9; TSMC-1008, Abstract, ¶¶[0009], [0029].

48. It was well-known prior to the '181 Patent to form strained layers using epitaxial growth. *See, e.g.*, TSMC-1004, 2:32-58, 4:20-28; TSMC-1007, ¶[0048]; TSMC-1008, Abstract, 3:44-4:11. Epitaxial growth refers to a process by which a thin film of a single crystal material is grown upon a surface of a single crystal

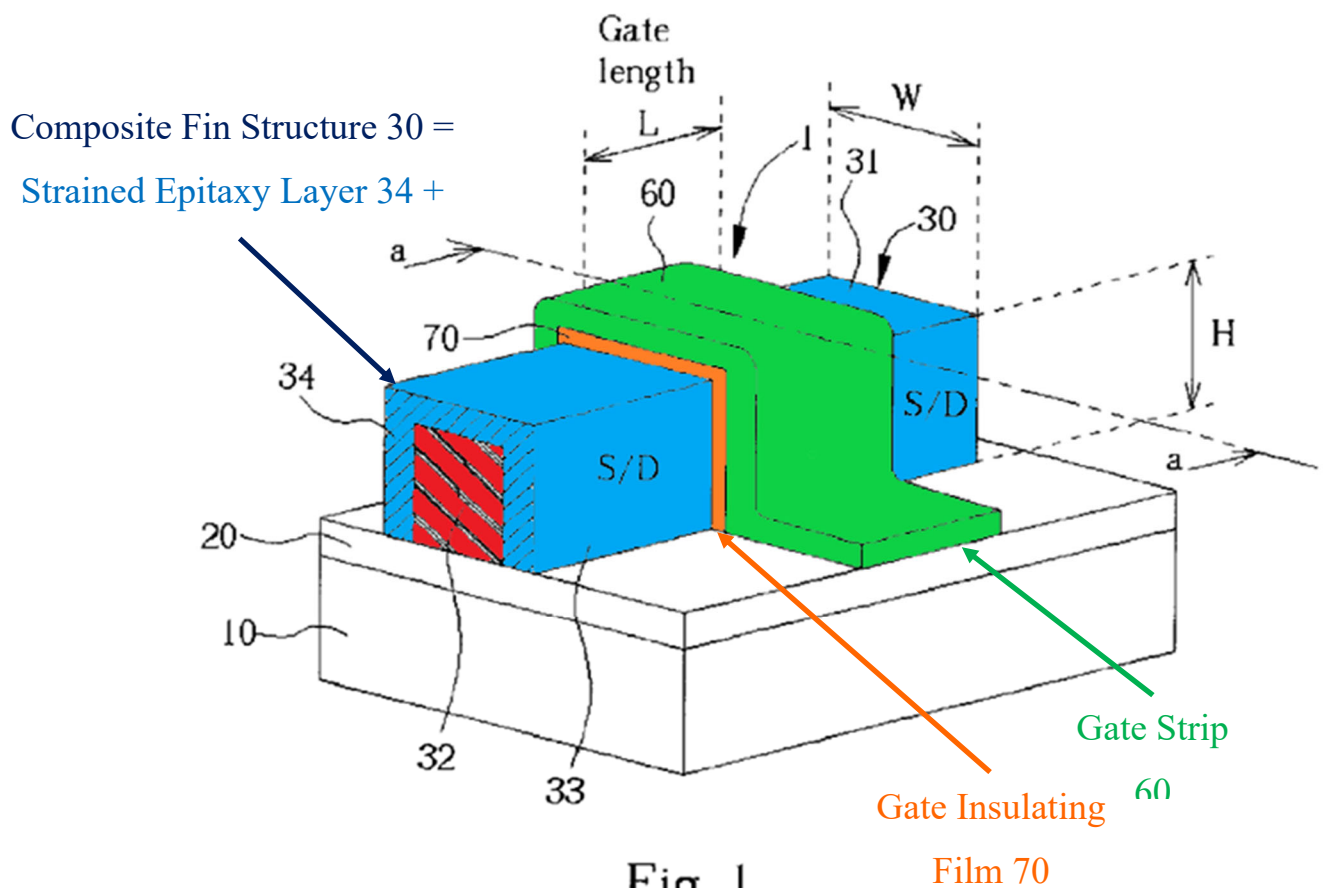
substrate. TSMC-1015, 225. Epitaxial growth is achieved by depositing the thin film directly from either the vapor phase (via vapor-phase epitaxy), the liquid phase (via liquid-phase epitaxy), or the solid phase (via solid-phase epitaxy). *Id.* Vapor-phase epitaxy such as chemical vapor deposition was a well-known process prior to the '181 Patent for growing a silicon film on diverse substrates such as silicon germanium. *Id.* It was well-known to FET designers prior to the '181 Patent that by controlling the epitaxial growth process, strain could be induced in the underlying substrate layer which impacts carrier mobility therein. And thus, a POSITA, prior to the '181 Patent filing, was already well aware that the resulting strain created due to the mismatch between lattice constants of a silicon film layer and a silicon germanium core provided enhanced channel mobility and corresponding increased driving current and improved device performance.

VII. THE '181 PATENT

A. Brief Description

49. The '181 Patent is directed to a “three-dimensional Triple-Gate (Tri-gate) device having a three-sided strained silicon channel,” which it purports provides “superior drive current.” TSMC-1001, Abstract, 1:7-10. In particular, the '181 Patent touts its Tri-gate devices as including a “composite fin structure” that consists of a semiconductor core (e.g., silicon germanium) and a “*three-sided*” strained epitaxy layer (e.g., strained silicon) grown on the semiconductor core. *Id.*,

Abstract; *see also id.*, 2:15-19. “A gate strip wraps a channel portion of the composite fin structure” and a “gate insulating layer is interposed between the composite fin structure and the gate strip.” *Id.*, 2:19-24. Figure 1 of the '181 Patent is reproduced below with annotations highlighting the composite fin structure, gate insulating film, and gate strip components of its Tri-gate device:



50. The '181 Patent touts the “strained silicon epitaxy layer 34” as “greatly improv[ing]” performance of the device by providing “superior carrier mobility, and thus higher drive current.” *Id.*, 3:18-21.

51. However, as discussed in the Technology Background section above and explained in detail in the Grounds below, it was well-known prior to the '181 Patent to utilize a composite fin structure that includes a strained silicon epitaxy layer grown on a silicon germanium core in a FinFET (including in a triple gate device), and it was well-known that such a structure improves carrier mobility and increases drive current in the very same manner discussed in the '181 Patent.

B. Prosecution History

52. The prosecution history of the '181 Patent is brief. Application Serial No. 10/708,694 was filed in the U.S. PTO on March 18, 2004, without any claim of priority to any earlier application. The U.S. PTO issued a single non-final office action, mailed on September 7, 2004. The U.S. PTO Examiner rejected original claims 6 and 9-11 under 35 U.S.C. § 103(a) over U.S. Pat. No. 6,764,884 to Yu et al., which reference is not relied on in the present petition. In the office action, original claims 1-5 were allowed without any substantive rejection, and original dependent claims 7-8 were noted as allowable if rewritten in independent form. TSMC-1002, 38-41. The office action did not provide any statements concerning reasons for allowability of claims 1-5 and 7-8.

53. The Applicant filed a response on December 2, 2004, amending original independent claim 6 to incorporate the subject matter of dependent claim 7. *Id.*, 28-32. In particular, independent claim 6 was amended to further recite that “said

semiconductor core having a first lattice constant that miss-matches a second lattice constant of said strained epitaxy layer.” *Id.* The U.S. PTO then allowed the application, without any reasons for allowance. The Examiner did not consider any of the Lee, Sugiyama, Dakshina, or Chau references discussed herein.

C. Claim Construction

54. I understand that claim terms are construed with the meanings they would have to a person of ordinary skill in the art in the context of the patent document. In my analysis of the Challenged Claims, I have therefore applied the meanings of the claim terms as understood by a person of ordinary skill in the art in the context of the '181 Patent and claims. In forming my opinions, I do not believe that any express constructions are required because the prior art teaches substantially the same teachings as the '181 Patent's disclosures. If Patent Owner offers constructions of any terms, I reserve the right to address those constructions at a future time.

VIII. PRIOR ART

A. Lee (TSMC-1004)

55. Similar to the '181 Patent, Lee is directed to “a strained silicon finFET device having a strained silicon fin channel.” TSMC-1004, Abstract. With reference to Figure 14, Lee's disclosed FinFET devices include a three-dimensional triple gate device in which a gate (e.g., triple gate 103) covers three sides of a composite fin

structure (e.g., combination of “strained silicon layer 11”/“strained silicon channel 104” and “seed fin 10”/“seed fin 105”):

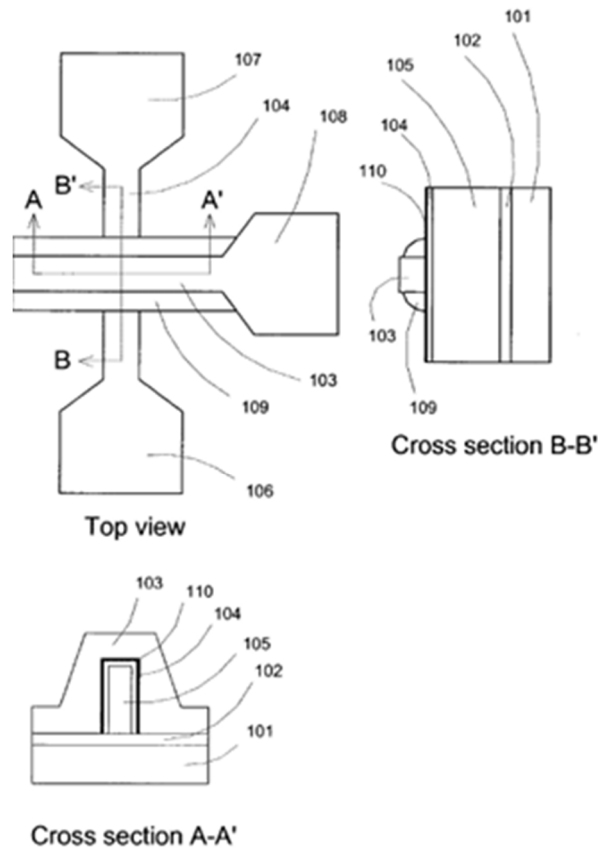


Fig. 14

TSMC-1004, 12:31-48; *see id.* Fig. 1, 4:12-19.

56. Lee’s composite fin structure consists of a seed fin 10/105 on which an epitaxial silicon layer 11/104 is grown. *Id.*, 3:51-54 (“The strained silicon fin structure is fabricated by forming a silicon-containing epitaxial layer on a silicon-containing seed fin having different lattice constant.”); 3:60-63 (“The present invention strained silicon fin structure comprises a seed fin structure disposed on an

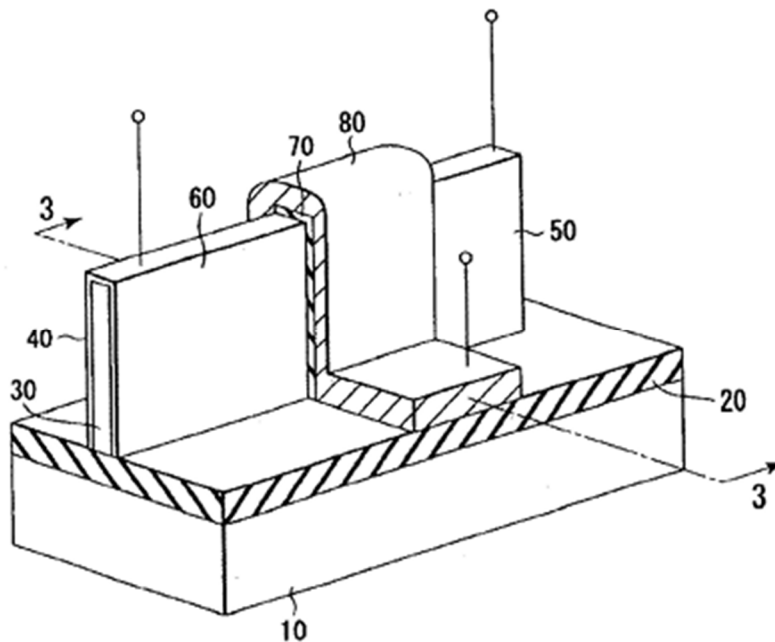
insulator substrate, and a strained channel layer fabricated on the seed fin structure.”); 4:12-19 (“In FIG. 1, a strained channel silicon layer 11 covers a relaxed silicon germanium fin seed fin 10 on an insulator layer 12. The relaxed silicon germanium fin 10 is preferably disposed on an insulator layer 12 (such as silicon dioxide) on a silicon substrate 13. The seed fin 10 is a relaxed silicon germanium fin having lattice constant larger than the lattice constant of silicon, therefore the epitaxial silicon layer 11 grown on the seed fin 10 will be tensilely strained.”); 12:34-36 (“The finFET channel is a strained silicon channel, comprising a seed fin 105 and a strained silicon channel 104....”).

57. A “lattice mismatch between the [epitaxial] silicon layer and the seed fin ... improve[s] hole and electron mobility enhancement, in addition to short channel effect reduction characteristic inherently in a finFET device.” *Id.*, Abstract.

B. Sugiyama (TSMC-1005)

58. Like the ’181 Patent, Sugiyama is directed to a “semiconductor device,” and specifically a metal insulator semiconductor “MIS field effect transistor” (MISFET). TSMC-1005, 1:14-15 (“The present invention relates to a semiconductor device using a MIS field effect transistor.”). Sugiyama’s MISFET devices include a composite fin structure that consists of a “projecting SiGe layer (semiconductor board) 30” and a “strained Si layer (semiconductor layer) 40 [that] is formed on the side and upper surfaces of the SiGe layer 30.” *Id.*, 6:65-7:2. A gate 80 surrounds the

composite fin structure on three sides. *See id.*, 7:8-10 (“band-like gate electrode 80 [that] is so formed as to cover the vertical surfaces and horizontal upper surface of the strained Si layer 40”), Fig. 2.



59. Accordingly, a POSITA would understand Sugiyama's MISFET device to be a three dimensional triple gate device just as called for in the '181 Patent.

60. Additionally, just as in the '181 Patent, Sugiyama explains that a lattice constant mismatch resulting from the strained induced by growth of the strained Si layer 40 on the projecting SiGe layer 30 results in higher performance due to increased electron and hole mobilities. *See* TSMC-1005, 5:35-63 (“The present invention has been made to solve this problem, relates to a MISFET using, as a channel layer, a second semiconductor layer such as a strained Si layer which is joined to a first semiconductor layer such as a SiGe crystal layer formed on an

insulating layer, has a lattice constant different from that of the first semiconductor layer, and has a stress strain in crystal lattices, and also relates to a CMIS circuit which is combined with the MISFET.... When the first semiconductor layer is formed from a SiGe crystal layer and the second semiconductor layer is formed from strained Si, the strained Si layer which covers the surface of the SiGe crystal layer functions as a channel. It has been reported that the electron and hole mobilities increase in the strained Si channel, compared to a general Si layer. Hence, a high-performance MISFET in which the carrier exhibits high mobility can be manufactured from even a p-channel MISFET or n-channel MISFET.”).

C. Dakshina (TSMC-1006)

61. Similar to the '181 Patent, Dakshina is directed to “fin field effect transistors (FinFETs)” having “a fin and a [strained] layer formed on the fin.” TSMC-1006, 1:5-6, Abstract. Dakshina’s FinFET devices use “a vertically formed strained channel layer that is self-aligned to the fin channel. The strained channel layer may include a crystalline material that is lattice constant mismatched with the crystalline material of the fin of the FinFET. The lattice constant mismatch induces tensile strain within the strained channel layer that increases carrier mobility. Increasing the carrier mobility, in turn, increases the drive current of the FinFET transistor, thus, improving FinFET performance.” *Id.*, 1:31-40. The strained channel layer is grown on the fin using an epitaxial deposition process. *See id.*, 3:61-67

(“strained layer 305 may be formed on fin 205, source 210 and drain 215 using a selective epitaxial deposition process. Strained layer 305 may include a crystalline material whose lattice constant is smaller than the lattice constant of the crystalline material used for fin 205.”).

62. Dakshina’s FinFET devices constitute three-dimensional triple gate devices having a composite fin structure that utilize a lattice constant mismatch induced by a strained epitaxial layer to increase carrier mobility, and thus device performance, just as discussed in the ’181 Patent.

D. Chau (TSMC-1007)

63. Again like the ’181 Patent, Chau is directed to the configuration and fabrication of “tri-gate devices.” TSMC-1007, Title (“Tri-gate devices and methods of fabrication”). Chau’s tri-gate devices include fins (e.g., “semiconductor bodies 520”) around which a gate (e.g., gate electrode 530) is formed. *Id.*, ¶¶[0039]-[0040] (“After forming photoresist mask 510, semiconductor film 508 is etched in alignment with photoresist mask 510 to form one or more silicon bodies or fins and source.... After semiconductor film 508 is etched to form semiconductor bodies or fins 520 (and source/ drain landing pads 522 and 524, if desired) the photoresist mask is removed by well-known techniques....”).

64. An epitaxial silicon layer is grown on the fins, forming a composite fin structure. *See id.*, ¶[0048] (“semiconductor film 560 can be formed on the exposed

surfaces of semiconductor body 520 (as well as on landing pads 522 and 524) as shown in FIG. 5H. Additionally, if desired, a semiconductor film 562 can be formed on the top of gate electrode 530.... In an embodiment of present invention, semiconductor film 560 is an epitaxial (single crystalline) silicon film.”).

65. Chau further teaches to vary the height and width dimensions of the semiconductor bodies/fins 520 to accommodate desired manufacturing constraints and/or performance characteristics for the FinFET devices, including configurations in which the body heights and widths are approximately the same to configurations in which the body height is between half and twice the body width. *See id.*, ¶[0019], Fig. 6.

66. Accordingly, Chau teaches choosing dimensions of a composite fin structure such that the width of the fin structure was approximately equal to its height.

IX. CLAIMS 1-10 ARE UNPATENTABLE

A. Ground 1: Lee anticipates, or alternatively renders obvious, Claims 1-10

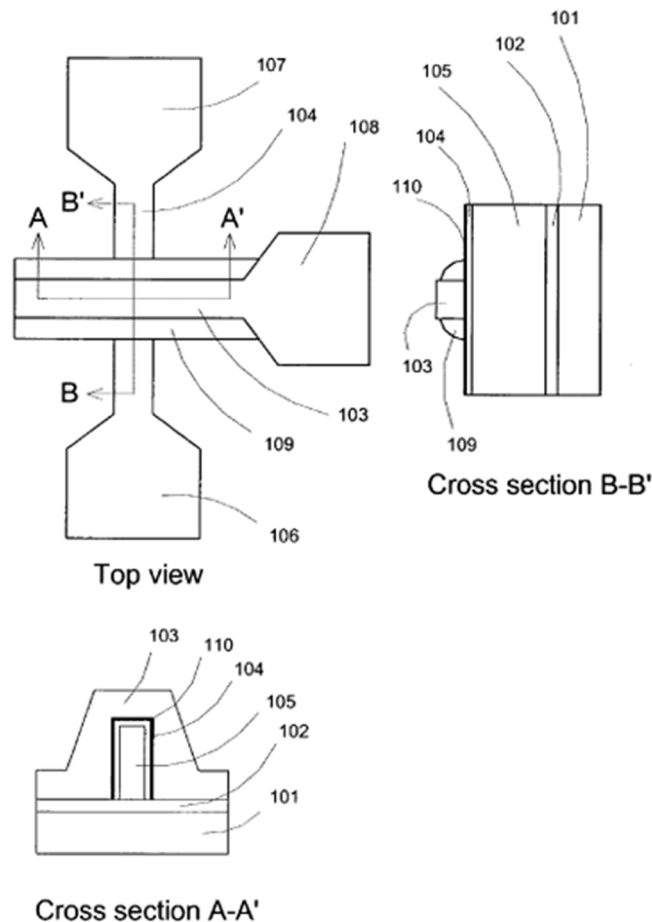
1. Claim 1

1[pre] “Three Dimensional Triple Gate (Tri-gate) Device”

67. Lee discloses a three dimensional triple gate (Tri-gate) device, e.g., “strained silicon finFET device employing [a] strained silicon fin structure.” TSMC-1004, 3:49-51; *see also id.*, Abstract, 3:51-4:11, 4:33-36, 12:17-30, Fig. 14.

68. In one example, Lee teaches that the “strained silicon finFET device” of Figure 14 includes a “channel 104” for which “conduction is controlled by double gate 103.” TSMC-1004, 12:17-24 (“FIG. 14 shows the top view of the disclosed strained silicon finFET device having the first embodiment of a silicon layer on a seed fin structure without a hard mask. The finFET is a field effect transistor having a source 106 and a drain 107 separated by a channel 104. The channel 104 conduction is controlled by the double gate 103, extending and covering the channel 104, and connected to the gate electrode 108.”). Lee further explains that “double gate 103 is *actually a triple gate* because it covers both sides and the top of the strained silicon channel 104. *The term ‘double gate’ in the context of the present invention is a generic term to mean ‘more than one gate’, and therefore **covers double or triple gate devices**.*” *Id.*, 12:26-30 (emph. added); *see also id.*, 12:34-40 (“The finFET channel is a strained silicon channel, comprising a seed fin 105 and a strained silicon channel 104, covering both sides and the top of the seed fin 105. *The finFET device becomes a triple gate device* because the gate 103 covers the strained silicon channel 104 on both sides and also on the top of the fin. The triple gate 103 is isolated from the channel 104 by a gate dielectric 110.”) (emph. added). A

POSITA prior the '181 Patent recognized that FET devices having a gate that covers at least three sides of the gate constitute “triple gate” or “tri-gate” devices. Figure 14 depicts one example of Lee’s three dimensional triple gate device:



69. A POSITA at the time of the '181 Patent filing would have readily understood the foregoing “triple gate device” of Lee to be “three dimensional” at least because of the presence of the “fin structure” formed from the combination of “fin channel 104” and “seed fin layer 105,” which extends in three dimensions from “insulator 102” on “substrate 101” (and is thus non-planar). *See also* TSMC-1004,

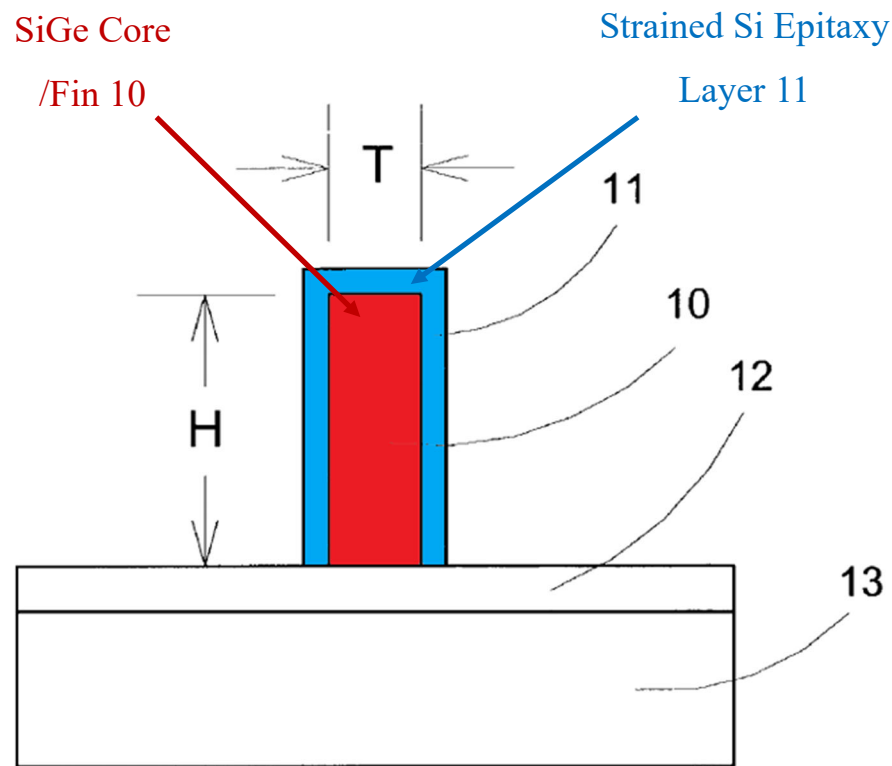
12:17-40 (“The finFET channel is a strained silicon channel, comprising a seed fin 105 and a strained silicon channel 104, covering both sides and the top of the seed fin 105. The finFET device becomes a triple gate device because the gate 103 covers the strained silicon channel 104 on both sides and also on the top of the fin. The triple gate 103 is isolated from the channel 104 by a gate dielectric 110.”), Fig. 14. As discussed in the background section about these “three dimensional” FinFET devices differ from planar FETs by virtue of, at least in part, their three dimensional nature. *Supra*, §VI(A).

70. Accordingly, a POSITA would understand that Lee’s FinFET devices are “three dimensional Triple Gate (Tri-gate) devices,” as recited in claim 1.

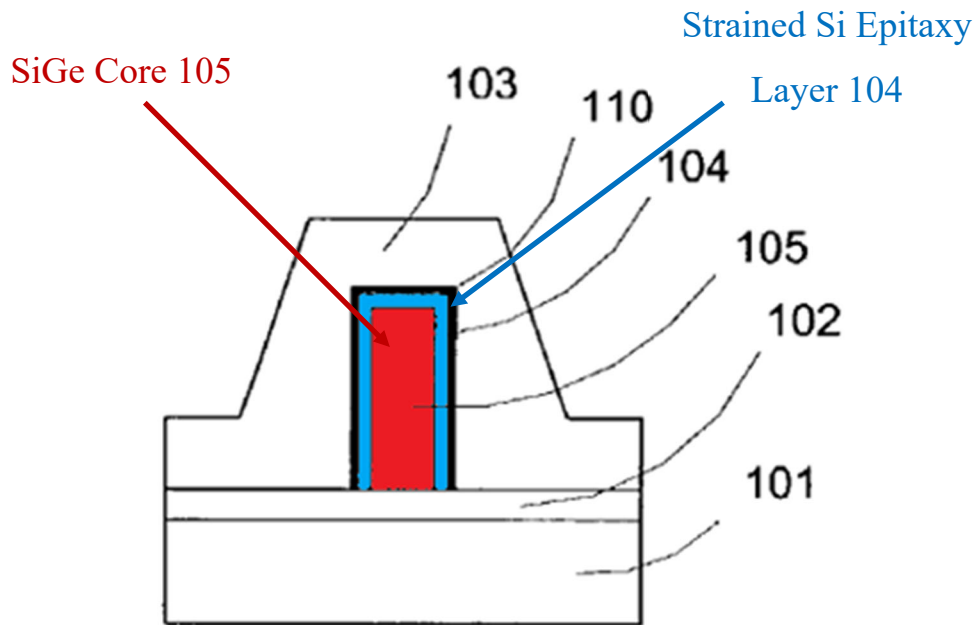
1[a] “Composite Fin Structure”

71. Lee’s FinFET device includes a composite fin structure (referred to variously in Lee as a “strained silicon fin structure,” “silicon fin channel,” “finFET channel”) consisting of: (i) a silicon germanium core (e.g., “silicon germanium seed fin,” “silicon germanium seed fin 10,” “seed fin 105”) and (ii) a strained silicon epitaxy layer (e.g., “strained silicon layer,” “silicon layer 11,” “strained silicon channel 104”) grown from the surface of said silicon germanium core. *See* TSMC-1004, Abstract, 3:49-4:19, 12:17-48, 11:31-38, 16:26-33, Figs. 1, 3C, 14.

72. Figures 1 and 14 depict Lee's composite fin structure made of the combination of the silicon germanium fin 10/105 (depicted in red) and the strained silicon epitaxy layer 11/104 (depicted in blue), as shown below with annotations:



Lee Figure 1



Lee Figure 14

Figures 1 and 14 of Lee depicts a same composite fin structure design (including the combination of a silicon germanium core and epitaxial strained silicon layer thereon).

73. Regarding Figure 1, Lee describes a “strained silicon fin structure” that consists of a “***strained*** channel ***silicon*** layer 11” which “covers a relaxed ***silicon germanium***...seed fin 10.” TSMC-1004, 4:7-13 (“An embodiment of the present invention strained silicon fin structure is shown in FIG. 1 wherein the channel layer covers both the top side and the two sidewalls of the seed fin. The seed fin of this embodiment can be a strained seed fin, but preferably a relaxed seed fin.”) (emph. added). “Strained channel silicon layer 11” is an “epitaxial silicon layer” that is

“grown on the seed fin 10.” TSMC-1004, 4:18-19; *see also id.*, 4:20-28 (“The relaxed silicon germanium fin structure is preferably fabricated from a silicon germanium-on-insulator (SGOI) substrate with the concentration of germanium ranging from 10% to 100%. Then the SGOI substrate is patterned into a silicon germanium fin structure. Then a ***silicon layer is epitaxially deposited on the silicon germanium fin structure.*** The ***epitaxial deposition is preferably selectively epitaxial deposition wherein the deposition only occurs on the silicon germanium exposed surfaces.***”) (emph. added), 6:58-7:7 (“The starting substrate of the above embodiment is a relaxed silicon germanium layer 15 on an insulator 12 on a silicon substrate 13 (SiGe-On-Insulator, SGOI) (FIG. 3a). A fin structure is patterned on the SGOI substrate. The patterning of the silicon germanium fin is preferably by photolithography process. The silicon germanium fin structure 10 after the patterning process is shown in FIG. 3b with a thickness T and height H. FIG. 3b shows the etching of the silicon germanium layer 15 and stopping on the insulator layer 12, but the pattern etching of the fin structure may be over-etched onto the insulator layer 12. The fabrication process continues with a ***selective deposition of an epitaxial silicon layer 11, covering the exposed surface of the silicon germanium*** (FIG. 3c). Due to the mismatched lattice constants between the silicon germanium seed fin structure and the ***epitaxial deposited silicon layer***, the deposited silicon layer is under strained to form a strained silicon fin structure.”) (emph.

added), Figs. 3b-3c. Accordingly, a POSITA would understand that the foregoing strained silicon layer shown in, and described in connection with, Figure 1 of Lee is an epitaxy layer grown from the surface of the silicon germanium seed fin/core.

74. Similarly, Lee describes the FinFET device of Figure 14 as having “a seed fin 105 and a strained silicon channel 104, covering both sides and the top of the seed fin 105.” TSMC-1004, 12:34-37. “Strained silicon channel 104” is “selectively **grown on** the seed fin 105.” *Id.*, 12:52-55 (emph. added). Lee further describes that a channel layer such as “strained silicon channel 104” may include “epitaxial silicon layer deposited on a relaxed silicon germanium seed fin.” *Id.*, 11:32-38.

75. Accordingly, given Lee’s express teachings regarding the epitaxial deposition of a silicon layer onto a silicon germanium seed fin, a POSITA would readily understand that Lee’s FinFET devices include a composite fin structure consisting of a silicon germanium core and a strained silicon epitaxy layer grown from the surface of said silicon germanium core, thereby satisfying limitation 1[a].

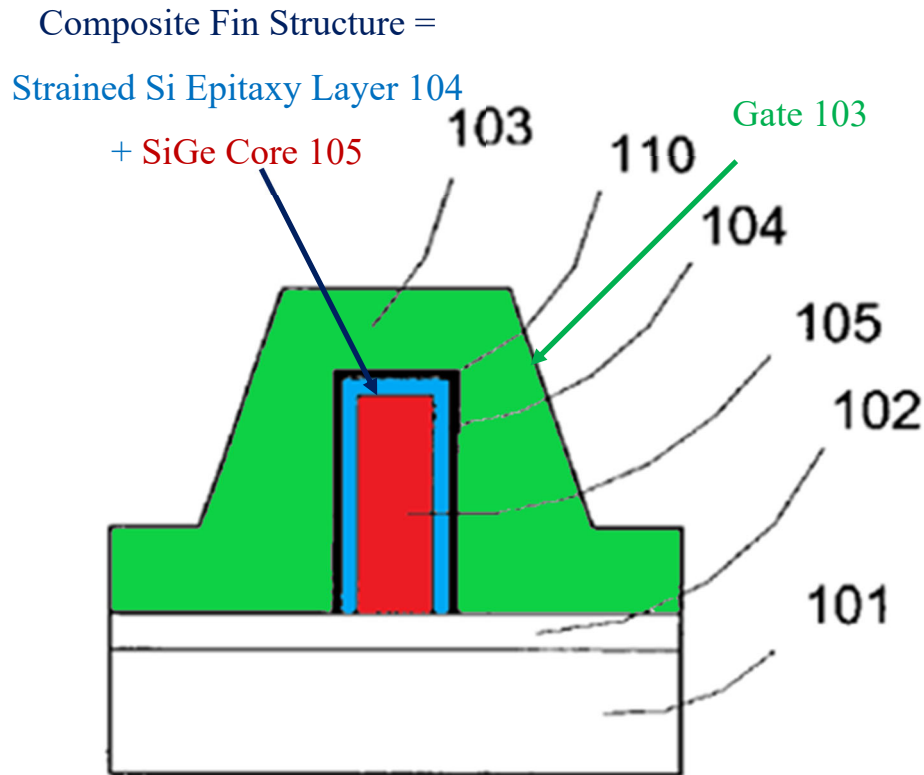
1[b] “Gate Strip”

76. Lee discloses a gate strip (e.g., “gate 103”) wrapping a portion of said composite fin structure (e.g., “strained silicon fin structure,” “silicon fin channel,” “finFET channel”). *See* TSMC-1004, 12:21-48, 3:54-59, 13:17-42, 15:1-36, 16:34-36, Fig. 14. Lee describes that the “channel 104 conduction is controlled by the

double **gate 103**, extending and covering the channel 104, and connected to the gate electrode 108.... The ***double gate 103 is actually a triple gate because it covers both sides and the top of the strained silicon channel 104.***” TSMC-1004, 12:21-39 (emph. added).

77. Annotated Figure 14 cross section A-A’ is shown below, depicting gate 103 (in green) wrapping a portion of the composite fin structure/fin channel on the top surface and both sides:¹

¹ As also illustrated in Figure 14, Lee discloses that the gate 103 is electrically isolated from the channel 104 including by a gate dielectric 110. TSMC-1004, 12:24-26. The ’181 Patent embodiment is directly analogous, illustrating, in Figure 6, a gate insulating layer 70 between the gate strip 60 and the composite fin structure 34/90. TSMC-1001, 3:41-44, 3:60-4:8.



78. Figure 14 top view and Figure 14 cross section B-B' further demonstrate that the gate 103 extends across a central portion of the strained Si epitaxy layer 104 and SiGe core 105, i.e., covering part of the layer 104/core 105. Accordingly, a POSITA would understand that Lee's gate 103 constitutes a gate strip that wraps a portion of the combined strained silicon epitaxy layer 104/silicon germanium core 105 (i.e., the "composite fin structure"), satisfying this limitation.

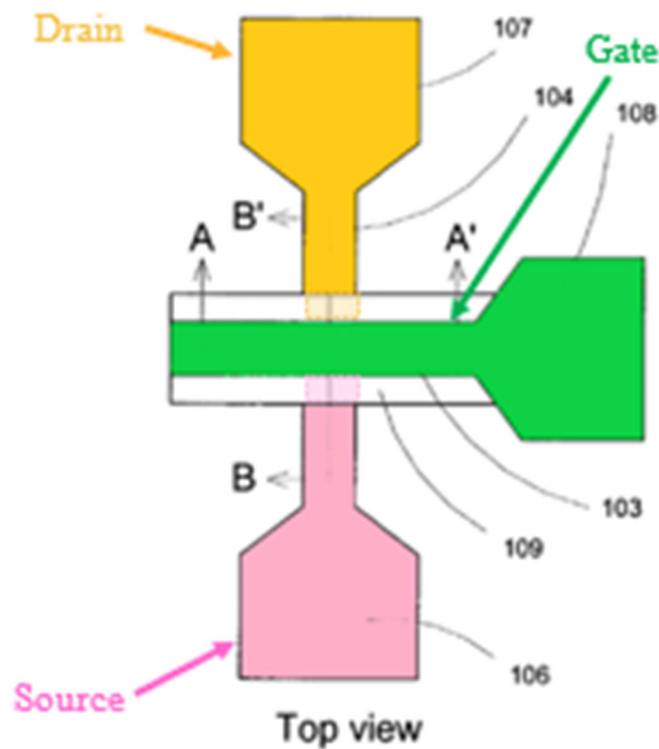
1[c] "Source/Drain Regions"

79. Lee discloses that portions of said composite fin structure (e.g., "strained silicon fin structure," "silicon fin channel," "finFET channel") not covered by said gate strip (e.g., "gate 103") constitute source/drain regions (e.g., "source

106,” “drain 107”) of said Tri-gate device. *See* TSMC-1004, 2:61-64; 3:54-56, 12:17-21, 13:17-42, Fig. 14. Regarding the FinFET device depicted in Figure 14, Lee states that “a *source 106* and a *drain 107 [are] separated by a channel 104.*” TSMC-1004, 12:20-21 (emph. added). The channel 104 is covered by the gate 103: “The double gate 103 is actually a triple gate because it covers both sides and the top of the strained silicon channel 104.” TSMC-1004, 12:26-28; *see id.*, 12:37-38 (“The finFET device becomes a triple gate device because the gate 103 covers the strained silicon channel 104 on both sides and also on top of the fin.”); *see id.*, 10:46-48 (stating that in a “finFET structure, the gate length of the finFET structure is the distance between the source and drain and often is defined by a spacer gap.”).

80. Lee’s Figure 14 top view is reproduced and annotated below demonstrating that the portions of the composite fin structure not covered by gate 103 (in green) constitute source 106 (in pink) and drain 107 (in gold) of the Tri-gate device:²

² Uncolored portion 109 is a “spacer” that serves to “isolate the double gate 103 from the silicon channel 104.” TSMC-1004, 12:63-64. As such, a POSITA would understand that spacer 109 is not itself a part of the “composite fin structure” of Lee.

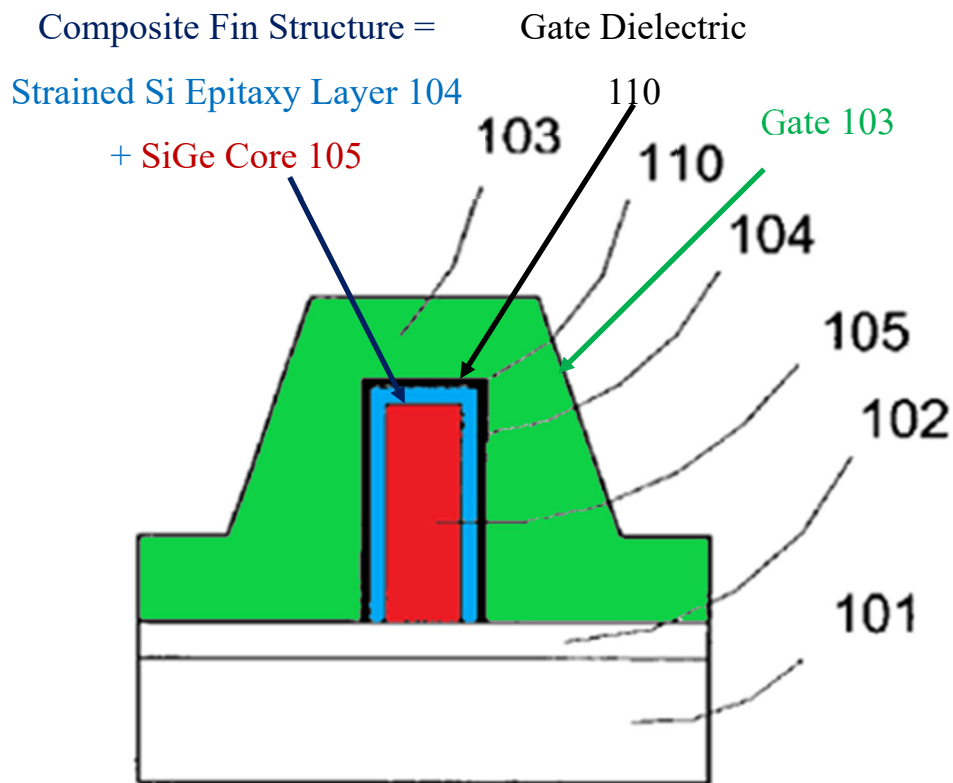


81. Accordingly, the composite fin structures of Lee’s FinFET devices include portions that are not covered by gate 103 that constitute source/drain regions (including the source and drain portions under spacers 109) of the Tri-gate device, thereby satisfying limitation 1[c].

1[d] “Gate Insulating Layer”

82. Lee discloses a gate insulating layer (e.g., “gate dielectric 110”) interposed between said composite fin structure (e.g., “strained silicon fin structure,” “silicon fin channel,” “finFET channel”) and said gate strip (e.g., “gate 103”). *See* TSMC-1004, 3:49-59, 12:24-57, 13:33-40, Fig. 14.

83. Lee's "gate 103 is electrically isolated from the channel 104 by a *gate dielectric 110*," which is a "gate insulating layer," as claimed. TSMC-1004, 12:39-40 (emph. added); *see id.*, 12:24-26 ("The double gate 103 is electrically isolated from the channel 104 by a spacer 109 and a gate dielectric 110."). As depicted in annotated Figure 14 cross section A-A' below, gate dielectric 110 (shown in black) is interposed between Lee's composite fin structure (i.e., the combination of strained silicon channel 104 and seed fin 105) and Lee's gate strip (i.e., "gate 103"):



See also TSMC-1004, Fig. 14 cross section B-B' (illustrating gate dielectric 110 disposed between the gate and the composite fin structure made of silicon channel 104/seed fin 105).

84. Accordingly, Lee's gate dielectric 110 constitutes the claimed "gate insulating layer," satisfying this limitation.

85. A POSITA would thus understand that Lee discloses all limitations of claim 1.

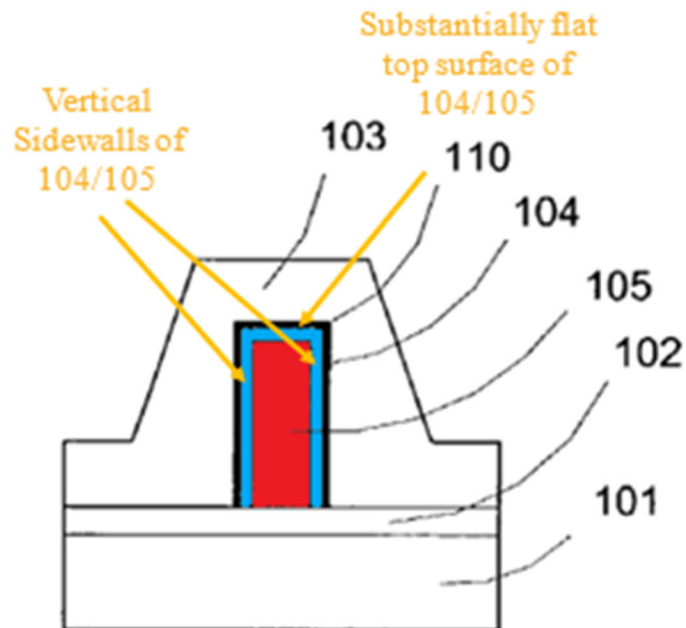
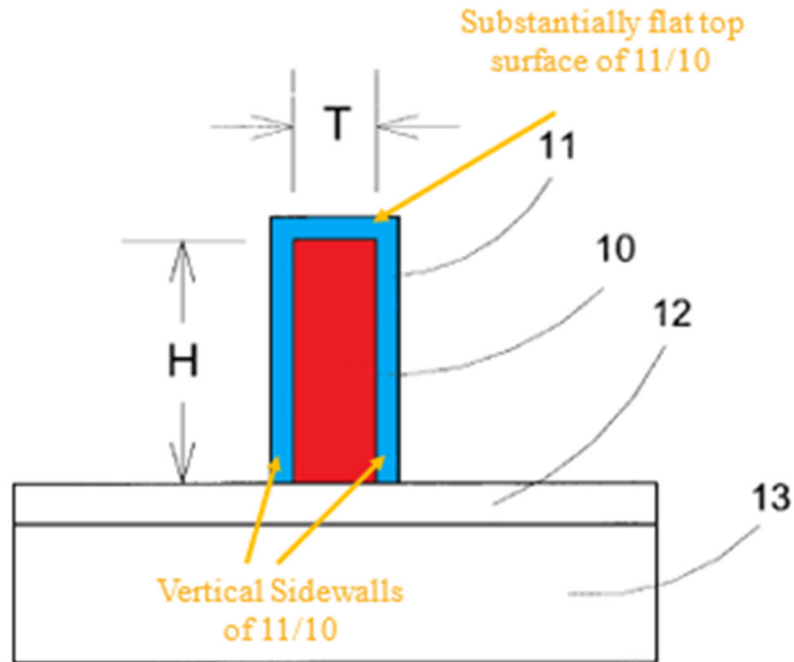
2. Claim 2

[2] The Tri-gate device of claim 1 wherein said composite fin structure has a substantially flat top surface and vertical sidewalls.

86. As depicted in annotated Figures 1 and 14 of Lee below, Lee's composite fin structure (e.g., "strained silicon fin structure," "silicon fin channel," "finFET channel") has a substantially flat top surface and vertical sidewalls. *See* TSMC-1004, Abstract, 3:49-4:43, 10:42-50, 12:17-48, Figs. 1, 3C, 14.

87. Lee's strained silicon channel 104, which in turn covers the sides and top of seed fin 105, has "sides" and a "top." TSMC-1004, 12:26-28 ("The double gate 103 is actually a triple gate because it covers both sides and the top of the strained silicon channel 104."), 12:34-39 ("The finFET channel is a strained silicon channel, comprising a seed fin 105 and a strained silicon channel 104, covering both sides and the top of the seed fin 105. The finFET device becomes a triple gate device because the gate 103 covers the strained silicon channel 104 on both sides and also on the top of the fin."). As depicted in annotated Figures 1 and 14 below, these

“sides” of Lee’s composite fin structure are vertical and the “top” surface of the composite fin structure is substantially flat:



See also TSMC-1004, Fig. 14 cross-section B-B' (depicting that composite fin structure made of strained silicon channel 104/seed fin 105 has a substantially flat top surface). A POSITA would understand that the top surface and sidewalls of Lee's composite fin structure are "substantially flat" and "vertical," respectively. Additionally, regardless of "substantially flat" and "vertical" are interpreted, the top surface and sidewalls of Lee's composite fin structure are "substantially flat" and "vertical" at least to the same extent as the devices disclosed in the '181 Patent.

88. A POSITA would further recognize that manufactured fin structures having a substantially flat top surface and vertical sidewalls were well-known. For example, contemporaneous publications at the time include STEM images depicting fin structures that have such a substantially flat top surface and vertical sidewalls (*see, e.g.*, TSMC-1020, Fig. 5):

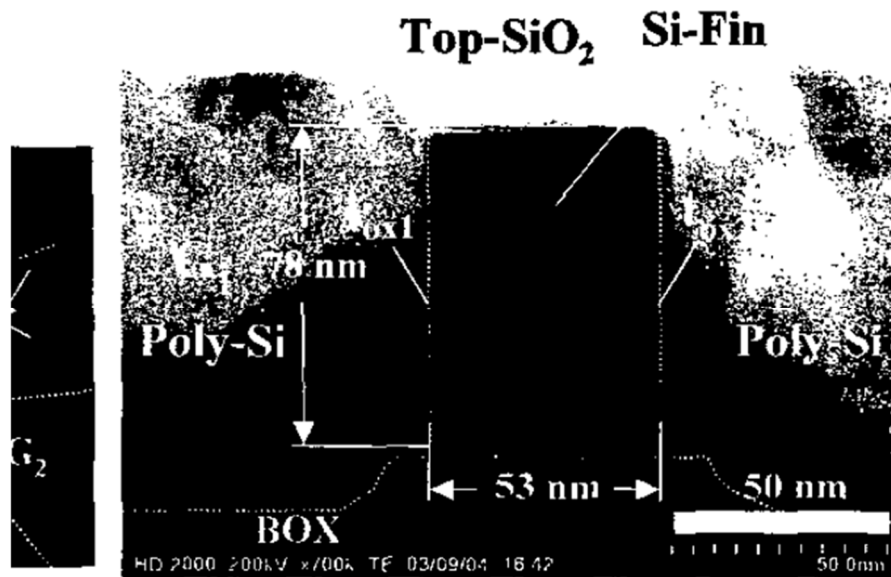


Fig. 5. Cross-sectional STEM image of the fabricated FT-FinFET.

A POSITA would have recognized that such fin structures would have retained the vertical sidewalls and substantially flat top surface upon deposition of an epitaxial layer upon the fin, which would merely grow on those walls and top surface of the fin to a generally consistent thickness.

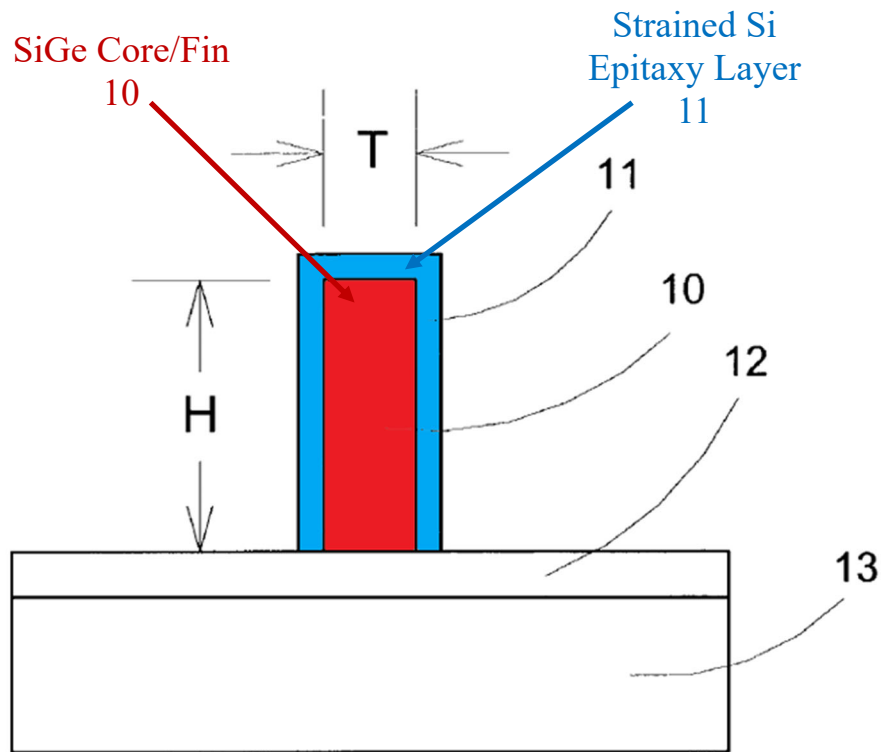
89. Accordingly, a POSITA would understand that the “sides” and “top” of Lee’s strained silicon channel 104/seed fin 105 constitute “vertical sidewalls” and a “substantially flat top surface” as recited in claim 2 of the ’181 Patent.

3. Claim 3

[3] The Tri-gate device of claim 2 wherein said composite fin structure has a width of said flat top surface that is approximately equal to its height.

90. A POSITA would read Lee as disclosing that its composite fin structure (e.g., “strained silicon fin structure,” “silicon fin channel,” “finFET channel”) has a width of said substantially flat top surface that is approximately equal to its height. TSMC-1004, 4:33-43 (“The strained silicon fin structure as shown in FIG. 1 can become triple gate device in a finFET structure because the silicon channel covers two sides and top of the seed fin structure. The height H of the seed fin is preferably in the range of 10 nm to 200 nm, and the thickness T of the seed fin is preferably in the range of 5 nm to 100 nm. The epitaxial silicon layer thickness is preferably in the range of 5 to 15 nm. The optimized dimensions of the disclosed strained silicon fin structure are preferably chosen to ensure fully depleted body under the operation conditions of the finFET device.”), Figs. 1, 14.

91. As discussed above, Lee discloses a composite fin structure (which consists of the combination of silicon germanium fin 10 and strained silicon epitaxy layer 11), which is depicted for example in Figure 1 (as annotated and reproduced below):



92. As depicted in Figure 1 of Lee above, the silicon germanium fin 10 of the composite fin structure 10/11 has a “height H” and a “thickness T” (or “width”). See TSMC-1004, 4:12-43. Lee further describes preferred numerical ranges for these dimensions. Specifically, Lee states that its “seed fin” (e.g., “silicon germanium fin 10,” “seed fin 105”) has a “height H [that] is preferably in the range of 10 nm to 200 nm” and a “thickness T” (i.e., a “width”) that “is preferably in the range of 5 nm to 100 nm.” TSMC-1004, 4:36-38 (“The height H of the seed fin is preferably in the range of 10 nm to 200 nm, and the thickness T of the seed fin is preferably in the range of 5 nm to 100 nm.”).

93. Additionally, as depicted in Figure 1 of Lee above and discussed above with respect to claim 1, a strained epitaxial silicon layer 11 is formed on the silicon germanium seed fin 10. *See* TSMC-1004, 4:12-19 (“In FIG. 1, a strained channel silicon layer 11 covers a relaxed silicon germanium fin seed fin 10 on an insulator layer 12. The relaxed silicon germanium fin 10 is preferably disposed on an insulator layer 12 (such as silicon dioxide) on a silicon substrate 13. The seed fin 10 is a relaxed silicon germanium fin having lattice constant larger than the lattice constant of silicon, therefore the epitaxial silicon layer 11 grown on the seed fin 10 will be tensilely strained.”), Fig. 1. Lee further describes preferred thickness for this layer, stating that the “epitaxial silicon layer” (e.g., “strained channel silicon layer 11,” “strained silicon channel 104”) has a “thickness [that] is preferably in the range of 5 to 15nm.” *Id.*, 4:38-40. Lee teaches that the thickness of the epitaxial silicon layer is uniform on the top and the sides. *See id.* A POSITA would understand that constructing a composite fin structure having dimensions for its silicon germanium seed fin and epitaxial silicon layer within the foregoing ranges would result in a composite fin structure that has a substantially flat top surface and vertical sidewalls, including at least to the same degree as the devices disclosed and depicted in the ’181 Patent (*see, e.g.*, Figs. 1-2 of the ’181 Patent).

94. As understood from Figures 1 and 14, a POSITA would recognize that the height of the top surface of the composite fin structure (i.e., H_{CFS}) of Lee is equal

to the height of the seed fin (i.e., H_{SF}) plus the thickness of the “epitaxial silicon layer” (i.e., T_{ESL})— $H_{CFS}=H_{SF}+T_{ESL}$. A POSITA would further recognize that the width of the top surface of the composite fin structure (i.e., W_{CFS}) of Lee is equal to the thickness of the seed fin (i.e., T_{SF}) plus two times the thickness of the epitaxial silicon layer (i.e., T_{ESL})— $W_{CFS}=T_{SF}+2*T_{ESL}$.

95. As discussed above, Lee discloses, as endpoints of disclosed ranges, that the “height H of the seed fin” may be 10 nm, the “thickness T of the seed fin” may be 5 nm, and the “epitaxial silicon layer thickness” may be 5 nm. TSMC-1004, 4:36-40 (“The height H of the seed fin is preferably in the range of 10 nm to 200 nm, and the thickness T of the seed fin is preferably in the range of 5 nm to 100 nm. The epitaxial silicon layer thickness is preferably in the range of 5 to 15 nm.”). Applying these dimensions results in the height of the sidewalls of Lee’s composite fin structure being substantially equal to the width of the top surface of the composite fin structure— $H_{CFS}=10\text{ nm}+5\text{ nm}=15\text{ nm}$; $W_{CFS}=5\text{ nm}+2*(5\text{ nm})=15\text{ nm}$. Thus, using the expressly disclosed endpoints of Lee’s ranges for the height and width of the fin core and the epitaxial layer thickness, the total height of Lee’s composite fin structure is substantially equal to the total width of its top surface.

96. A composite fin structure having a substantially equal width and height also is the result of selecting dimensions from well within Lee’s disclosed ranges. For example, selecting a height H of the seed fin of 80 nm (within Lee’s disclosed

10-200 nm seed fin height range), a thickness T of the seed fin of 70 nm (within Lee's disclosed 5-100 nm seed fin thickness range), and an epitaxial silicon layer thickness of 10 nm (within Lee's disclosed 5-15 nm epitaxial thickness range), results in a height of the seed fin of 90 nm and a width of the seed fin of 90 nm. It is clear that numerous other dimension selections within Lee's disclosed ranges also result in a composite fin structure having a substantially equal width and height. A POSITA would have easily recognized from Lee's range disclosures that a composite fin structure having an equal width and height was a disclosed dimensional option/shape for the fin structure.

97. Furthermore, a POSITA would have understood that there was no critical importance to having equal width and height dimensions for the composite fin structure. A POSITA understood prior to the '181 Patent that equal height and width dimensions for a composite fin structure would not have significantly impacted the operation of the device vis-à-vis other different (non-equal height and width) dimensions within Lee's disclosed ranges. Indeed, similar performance characteristics could have been achieved by such a device when the height and width of its composite fin structure were either substantially equal or somewhat different. *See* TSMC-1007, [0027], Fig. 6 (depicting full depletion achieved with composite fin structures of equal height/width and differing height/width); *infra*, §IX(B). For example, while slightly changing the width to, for example, 60%, 70%, or 80% of

the height, might slightly vary the current-voltage characteristics of the device for a given gate voltage, such variations were amount to merely a minor degree in change, and a change that was well-known and expected to a POSITA. The thickness of the epitaxial Si layer affects the current-voltage characteristics for a given gate length, as the thickness of the strained silicon determines the field strength required for depletion. By 1999, such effects were well understood. Indeed, models were available to simulate the effect of silicon thickness on MOSFET operation. *See* TSMC-1021. In situations where the width and height of a composite fin device changes but the thickness of the Si layer does not change, the current-voltage characteristics will not substantially change. In situations where the thickness of the epitaxial Si layer changes, the effects on the current-voltage characteristics were also well understood. For a given trigate height, the fraction of silicon in the top corners will increase slightly as the trigate width is decreased (for a given height, the total volume of silicon decreases as the width decreases since the top of the gate becomes smaller, but the volume of silicon in the corner remains constant), but the electric field in these corners would not substantially change. Because the electric field experienced by the corners would not substantially change until the fin width becomes similar to the epitaxial silicon thickness, the effect of changing the relative width and height of the composite fin structure would have been very small and predictable. Indeed, as the total cross-sectional area of the silicon changes, the

current carrying capacity of the composite fin device would change roughly linearly. Indeed, as depicted in Chau's Fig. 6 for example, devices having equal width and height dimensions as well as those having different widths and heights could still provide fully depleted operation as desired for FET operation. Reading off the graph of Chau Fig. 6, as the body height increases from 20 nm to 30 nm for example, the body width for full depletion changes from only 20 nm to 17 nm illustrating the low sensitivity on fully depleted operation on device dimensions when the body height and width are similar. Additionally, Chau demonstrates that a POSITA fully understood how varying dimensions of the fin structure would affect the functionality or operation of the device and that no significant or critical change to the operation of the fin structure or FinFET would have occurred just because equal width and height dimensions were used for the fin structure.

98. When settling on specific desired height and width dimensions, a POSITA would have balanced various well-known design considerations that may be impacted by such height and width dimensions. But once again, those design considerations were well-known prior to the '181 Patent as was the impact on the height and width dimensions of a composite fin structure on such considerations (or vice versa). For example, a POSITA would have considered current carrying capacity requirements, horizontal space constraints for the chip on which such FETs were used, cost, manufacturing error tolerance, manufacturing capital costs, and

manufacturing capacity. A POSITA understood that larger, more square-shaped fin structures were generally easier to manufacture and thus less costly as compared to smaller or higher aspect ratio (taller) fin structures. Likewise, larger cross-section fins would generally have more current carrying capacity, but also take up more space than smaller devices or require a taller fin structure. Thus, a POSITA would have balanced such design requirements when selecting a dimension size for the fin structure and well knew how to optimize the dimensions (which included choosing equal width and height dimensions) to achieve the design goals at acceptable cost.

99. A POSITA also would have found implementing the selected dimensions (particularly equal width and height dimensions) for the composite fin structure to be a relatively straightforward task at the time, and thus would have fully expected success when doing so. Indeed, a POSITA would have recognized that well-known fabrication techniques at the time (e.g., known lithographic patterning, etching, and deposition techniques, including those described in Lee) could have been used to create such devices without any expected concerns. Such techniques were widely used at the time, including to implement composite fin structures of equal width and height and in the dimensional ranges described in Lee. *See also* TSMC-1004, 13:43-14:67 (“A *photoresist is applied to define a pattern* through the use of optical *lithography*, electron beam lithography, X-ray lithography, or other conventional means to produce a photoresist mask comprising a fin channel between

a source and drain structures. After the photoresist mask definition, an *etch process is used to pattern* the silicon germanium layer 204 and the silicon layer 203.... A selective *epitaxial silicon layer is next deposited* on the seed fin surface as shown in FIG. 18c.”); TSMC-1007, ¶¶[0036]-[0038], [0048], Figs. 5A-5H.

100. Accordingly, as recognized by a POSITA, Lee discloses a composite fin structure with a substantially flat top surface having a width that is approximately equal to its height, thereby satisfying claim 3. Alternatively, a POSITA would have found such a shaped composite fin structure to be obvious.

4. Claim 4

[4] The Tri-gate device of claim 1 wherein said strained silicon epitaxy layer has a thickness of about 50-300 angstroms.

101. Lee discloses that its strained silicon epitaxy layer (e.g., “strained silicon layer,” “silicon layer 11,” “strained silicon channel 104,” “epitaxial silicon layer”) has a thickness that “is preferably in the range of 5 nm to 15 nm.” TSMC-1004, 4:38-40. 5-15 nanometers is equivalent to 50-150 angstroms, and thus Lee satisfies claim 4.

5. Claim 5

[5] The Tri-gate device of claim 1 wherein said gate strip is made of polysilicon or metal gate.

102. Lee discloses that the “gate of the disclosed strained silicon finFET structure is preferably polysilicon, doped polysilicon or metal.” TSMC-1004, 13:40-42; *see also id.*, 15:10-36 (“The *gate material can be polysilicon*, silicon germanium, a *refractory metal* or compound such as titanium nitride or molybdenum, *or other suitable conductive material such as aluminum, copper, or aluminum copper alloy*.... The *polysilicon gate* 225 may also be doped at this step if not already doped.”). Accordingly, a POSITA would understand that Lee’s gate strip (e.g., “gate 103”) is made of polysilicon or metal, each of which satisfies claim 5.

6. Claim 6

6[pre] “Tri-gate Device”

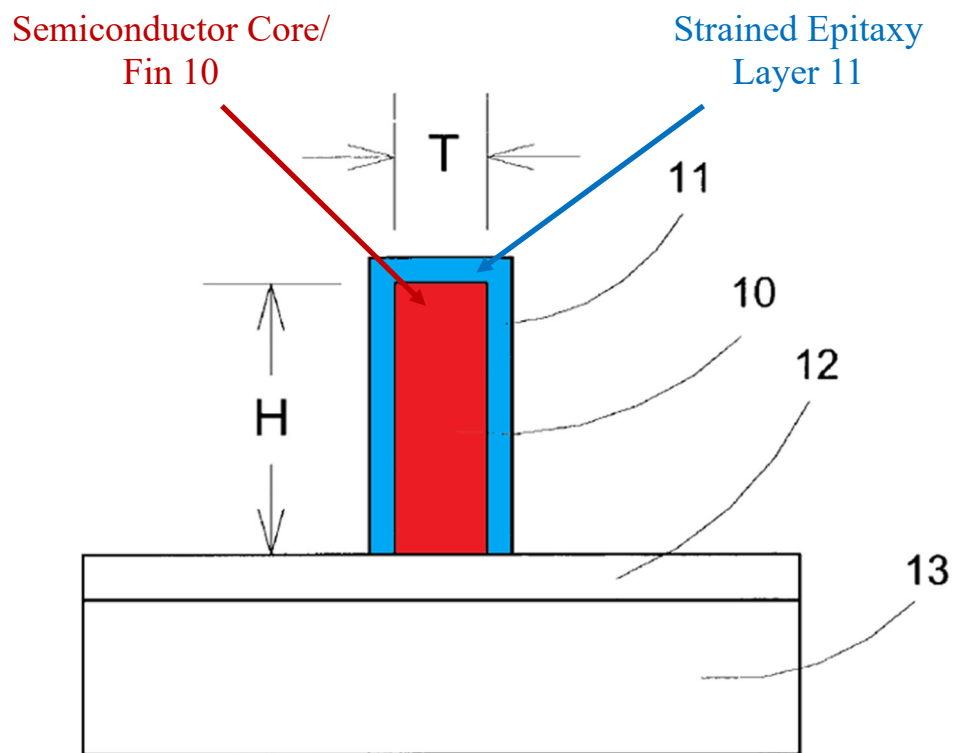
103. Lee discloses a triple gate (Tri-gate) device , e.g., “strained silicon finFET device employing [a] strained silicon fin structure.” TSMC-1004, 3:49-51; *see id.*, Abstract, 3:51-4:11, 4:33-36, 12:17-30, Fig. 14; *supra*, §IX(A)(1)(1[pre]).

6[a] “Composite Fin Structure”

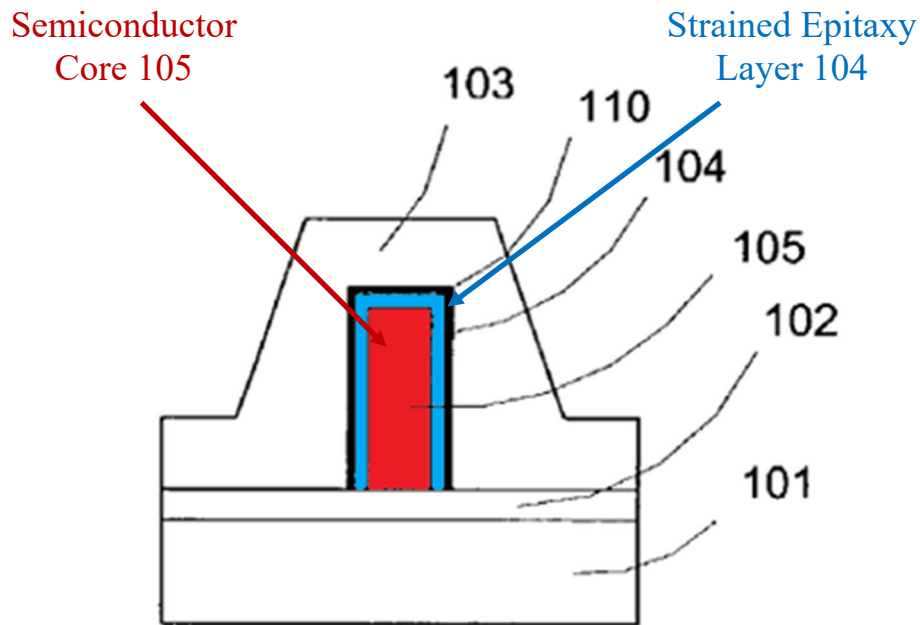
104. Lee’s FinFET device includes a composite fin structure (referred to variously in Lee as a “strained silicon fin structure,” “silicon fin channel,” “finFET channel”) consisting of: i) a semiconductor core (e.g., “silicon germanium seed fin,” “silicon germanium seed fin 10” “seed fin 105”); and ii) a strained epitaxy layer (e.g., “strained silicon layer,” “silicon layer 11,” “strained silicon channel 104”)

grown from surface of said semiconductor core. See TSMC-1004, Abstract, 3:49-4:19, 12:17-48, 11:31-38, 16:26-33, Figs. 1, 3C, 14; *supra*, §IX(A)(1)(1[a]).

105. Figures 1 and 14 depict Lee's composite fin structure made of the combination of the semiconductor core/fin 10/105 (depicted in red) and the strained silicon epitaxy layer 11/104 (depicted in blue), as shown below with annotations:



Lee Figure 1



Lee Figure 14

106. Regarding Figure 1, Lee describes a “strained silicon fin structure” that consists of a “*strained* channel *silicon* layer 11” which “covers a relaxed *silicon germanium*...seed fin 10.” TSMC-1004, 4:7-13 (“An embodiment of the present invention strained silicon fin structure is shown in FIG. 1 wherein the channel layer covers both the top side and the two sidewalls of the seed fin. The seed fin of this embodiment can be a strained seed fin, but preferably a relaxed seed fin.”) (emph. added). “Strained channel silicon layer 11” is an “epitaxial silicon layer” that is “grown on the seed fin 10.” TSMC-1004, 4:18-19; *see also id.*, 4:20-28 (“The relaxed silicon germanium fin structure is preferably fabricated from a silicon germanium-on-insulator (SGOI) substrate with the concentration of germanium

ranging from 10% to 100%. Then the SGOI substrate is patterned into a silicon germanium fin structure. Then a *silicon layer is epitaxially deposited on the silicon germanium fin structure*. The *epitaxial deposition is preferably selectively epitaxial deposition wherein the deposition only occurs on the silicon germanium exposed surfaces.*) (emph. added), 6:58-7:7 (“The fabrication process continues with a *selective deposition of an epitaxial silicon layer 11, covering the exposed surface of the silicon germanium* (FIG. 3c). Due to the mismatched lattice constants between the silicon germanium seed fin structure and the *epitaxial deposited silicon layer*, the deposited silicon layer is under strained to form a strained silicon fin structure.”) (emph. added), Figs. 3b-3c; *supra*, §IX(A)(1)(1[a]). Accordingly, a POSITA would understand that the foregoing strained silicon layer shown in, and described in connection with, Figure 1 of Lee is an epitaxy layer grown from the surface of the semiconductor seed fin/core.

107. Similarly, Lee describes the FinFET structure of Figure 14 as including “a seed fin 105 and a strained silicon channel 104, covering both sides and the top of the seed fin 105.” TSMC-1004, 12:34-37. “Strained silicon channel 104” is “selectively **grown on** the seed fin 105.” *Id.*, 12:52-55 (emph. added). Lee further describes that a channel layer such as “strained silicon channel 104” may include “epitaxial silicon layer deposited on a relaxed silicon germanium seed fin.” *Id.*, 11:32-38.

108. Thus, a POSITA would readily understand “silicon germanium...seed fin 10” and “seed fin 105” to each constitute a “semiconductor core,” as claimed. Additionally, a POSITA would understand “strained channel silicon layer 11” and “strained silicon channel 104” to each constitute a “strained epitaxy layer grown from [the] surface of the semiconductor core,” as claimed.

109. Additionally, Lee’s foregoing semiconductor cores (e.g., silicon germanium seed fins 10, 105) have a first lattice constant that mis-matches a second lattice constant of Lee’s example strained epitaxy layers (e.g., strained channel silicon layer 11, strained silicon channel 104). *See* TSMC-1004, 3:49-67, 4:16-33, 8:16-8:52, 9:12-28, 11:24-38. For example, Lee states that, in the disclosed invention, the FinFET devices each have a “strained silicon fin structure [that] is fabricated by forming a silicon-containing epitaxial layer on a silicon-containing seed fin having [a] *different lattice constant*.” TSMC-1004, 3:51-54 (emph. added). As another example, in discussing Figure 1, Lee further states that its “seed fin 10 is a relaxed silicon germanium fin **having [a] *lattice constant larger than the lattice constant of silicon***, therefore the epitaxial silicon layer 11 grown on the seed fin 10 will be tensilely strained.” *Id.*, 4:16-19 (emph. added); *see id.*, 4:28-30 (“The silicon is under biaxial tensile stress because *the lattice constant of silicon is smaller than the lattice constant of silicon germanium*.”), 6:35-42 (“In a further variation of the above embodiment, the seed layer is a silicon seed fin, and the epitaxial layer is an

epitaxial silicon germanium layer. Because *the lattice constant of silicon is smaller than the lattice constant of silicon germanium*, the epitaxial silicon germanium layer fabricated on the silicon seed layer will have a compressive strain, and thus forming a compressive strained silicon germanium channel fin structure.”), 7:4-7 (“*Due to the mismatched lattice constants* between the silicon germanium seed fin structure and the epitaxial deposited silicon layer, the deposited silicon layer is under Strained to form a strained silicon fin structure.”).

110. Accordingly, a POSITA would recognize that Lee’s various FinFET devices each have a composite fin structure consisting of a semiconductor core and a strained epitaxy layer grown from surface of said semiconductor core, and further that the semiconductor core has a first lattice constant that miss-matches a second lattice constant of the strained epitaxy layer, thereby satisfying this limitation.

6[b] “Gate Strip”

111. Lee discloses a gate strip (e.g., “gate 103”) wrapping a portion of said composite fin structure (e.g., “strained silicon fin structure,” “silicon fin channel,” “finFET channel”). See TSMC-1004, 12:21-48, 3:54-59, 13:17-42, 15:1-36, 16:34-36, Fig. 14; *supra*, §IX(A)(1)(1[b]).

6[c] “Source/Drain Regions”

112. Lee discloses that portions of said composite fin structure (e.g., “strained silicon fin structure,” “silicon fin channel,” “finFET channel”) not covered

by said gate strip (e.g., “gate 103”) constitute source/drain regions (e.g., “source 106,” “drain 107”) of said Tri-gate device. *See* TSMC-1004, 3:54-56, 12:17-21, 13:17-42, Fig. 14; *supra*, §IX(A)(1)(1[c]).

6[d] “Gate Insulating Layer”

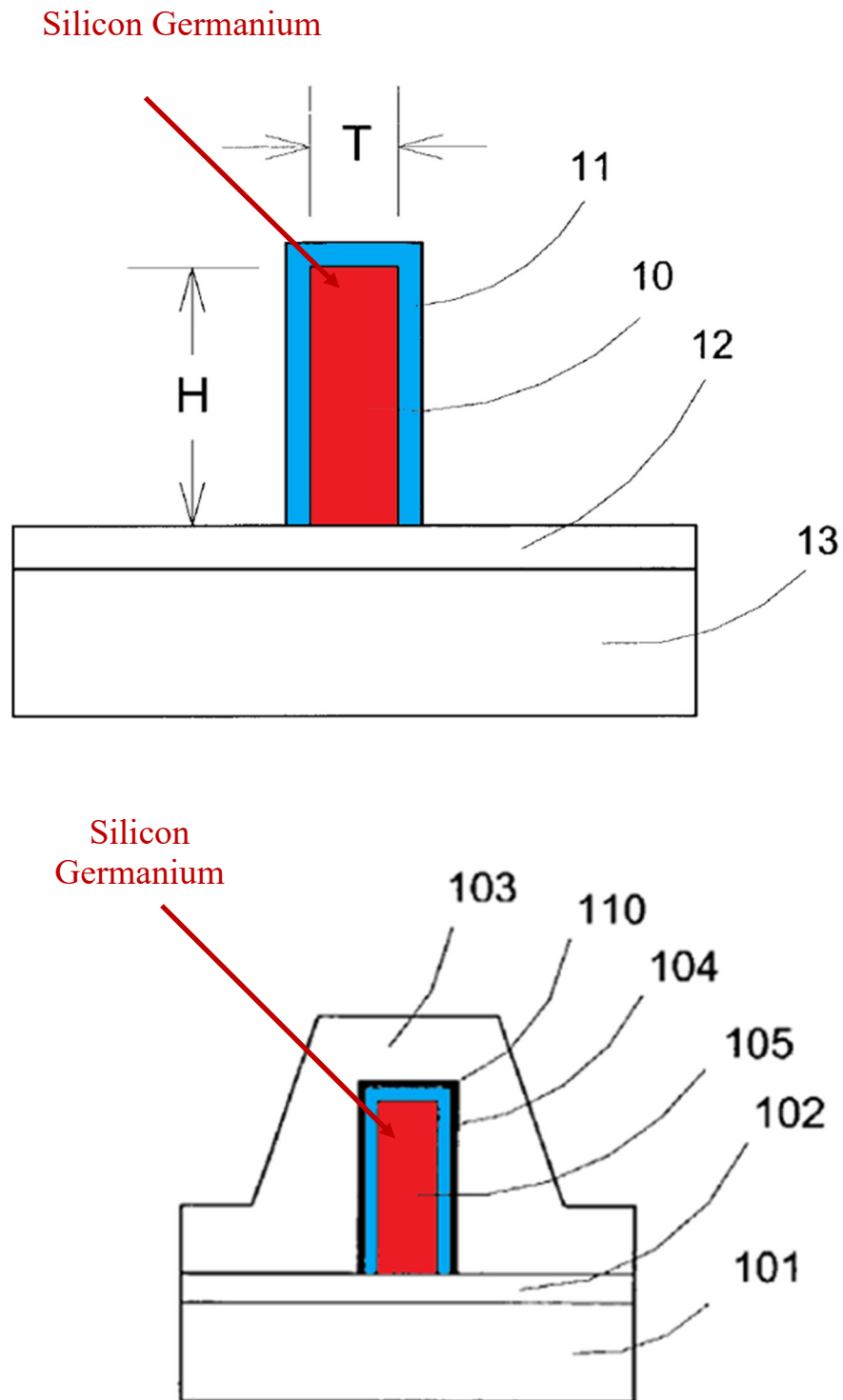
113. Lee discloses a gate insulating layer (e.g., “gate dielectric 110”) interposed between said composite fin structure (e.g., “strained silicon fin structure,” “silicon fin channel,” “finFET channel”) and said gate strip (e.g., “gate 103”). *See* TSMC-1004, 3:49-59, 12:24-57, 13:33-40, Fig. 14; *supra*, §IX(A)(1)(1[d]).

7. Claim 7

[7] The Tri-gate device of claim 6 wherein said semiconductor core consists of silicon germanium.

114. Lee’s semiconductor core (e.g., seed fin 10, seed fin 105) consists of silicon germanium (e.g., “silicon germanium seed fin,” “silicon germanium seed fin 10”). *See* TSMC-1004, Abstract, 3:49-4:19, 12:17-48, 11:31-38, 16:26-33, Figs. 1, 3C, 14.

115. Figures 1 and 14 depict Lee’s composite fin structure as shown below with annotations depicting the silicon germanium seed fin 10:



116. Specifically, regarding Figure 1, Lee describes a “strained silicon fin structure” that consists of a “strained channel silicon layer 11” which “covers a

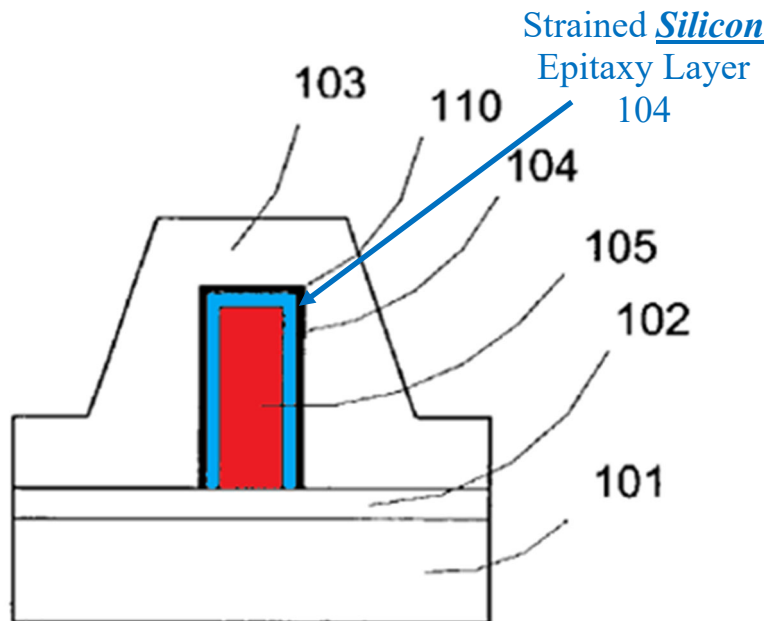
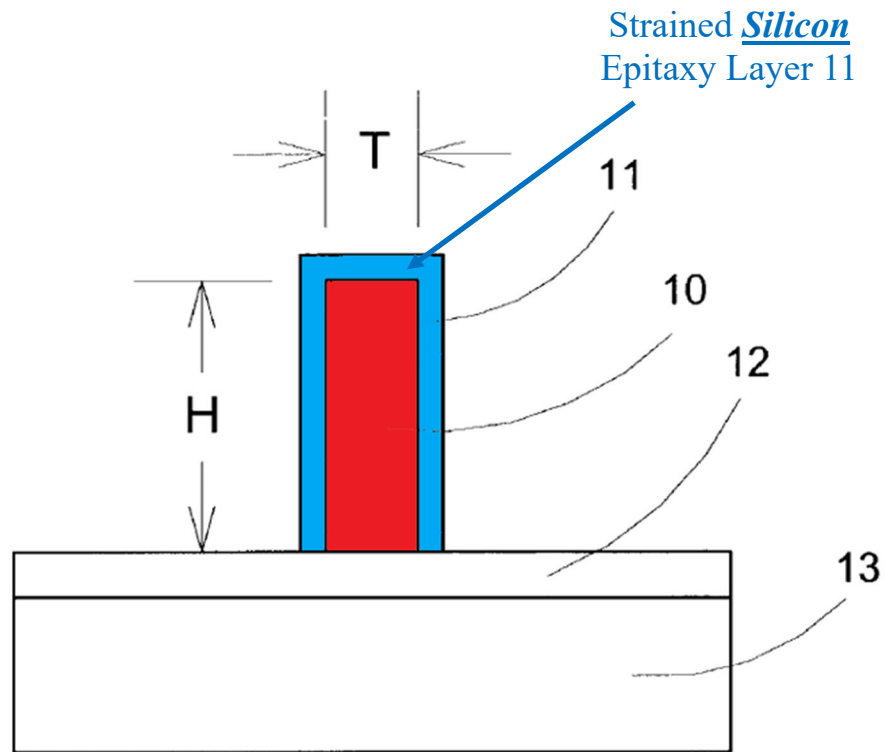
relaxed ***silicon germanium***...seed fin 10.” TSMC-1004, 4:7-13 (emph. added). Lee further describes that a channel layer such as “strained silicon channel 104” includes “epitaxial silicon layer deposited on a relaxed ***silicon germanium seed fin***.” *Id.*, 11:32-38 (emph. added). As understood by a POSITA, Lee teaches using silicon germanium for the seed fin/seed core of each Lee’s disclosed FinFET devices, and thus Lee satisfies claim 7.

8. Claim 8

[8] The Tri-gate device of claim 6 wherein said strained epitaxy layer is a strained silicon epitaxy layer.

117. Lee’s strained epitaxy layer (e.g., “strained ***silicon*** layer,” “***silicon*** layer 11,” “strained ***silicon*** channel 104”) is a strained ***silicon*** epitaxy layer. *See* TSMC-1004, Abstract, 3:49-4:19, 12:17-48, 11:31-38, 16:26-33, Figs. 1, 3C, 14; *supra*, §IX(A)(1)(1[a]).

118. Figures 1 and 14 depict Lee’s composite fin structure as shown below with annotations depicting the strained silicon epitaxy layer:



119. Regarding Figure 1, Lee describes a “strained *silicon* fin structure” that consists of a “*strained* channel *silicon* layer 11” which “covers a relaxed silicon

germanium...seed fin 10.” TSMC-1004, 4:7-13 (emph. added). “***Strained channel silicon*** layer 11” is an “epitaxial silicon layer” that is “grown on the seed fin 10.” TSMC-1004, 4:18-19; *see also id.*, 4:20-28 (“The relaxed silicon germanium fin structure is preferably fabricated from a silicon germanium-on-insulator (SGOI) substrate with the concentration of germanium ranging from 10% to 100%. Then the SGOI substrate is patterned into a silicon germanium fin structure. Then a ***silicon layer is epitaxially deposited*** on the silicon germanium fin structure. The epitaxial deposition is preferably selectively epitaxial deposition wherein the deposition only occurs on the silicon germanium exposed surfaces.”), 6:58-7:7 (“The starting substrate of the above embodiment is a relaxed silicon germanium layer 15 on an insulator 12 on a silicon substrate 13 (SiGe-On-Insulator, SGOI) (FIG. 3a). A fin structure is patterned on the SGOI substrate. The patterning of the silicon germanium fin is preferably by photolithography process. The silicon germanium fin structure 10 after the patterning process is shown in FIG. 3b with a thickness T and height H. FIG. 3b shows the etching of the silicon germanium layer 15 and stopping on the insulator layer 12, but the pattern etching of the fin structure may be over-etched onto the insulator layer 12. The fabrication process continues with a ***selective deposition of an epitaxial silicon layer 11, covering the exposed surface of the silicon germanium*** (FIG. 3c). Due to the mismatched lattice constants between the silicon germanium seed fin structure and the ***epitaxial deposited silicon layer***, the

deposited silicon layer is under strained to form a strained silicon fin structure.”), Figs. 3b-3c; *supra*, §IX(A)(1)(1[a]).

120. Similarly, Lee describes the FinFET structure of Figure 14 as having “a seed fin 105 and a strained **silicon** channel 104, covering both sides and the top of the seed fin 105.” TSMC-1004, 12:34-37 (emph. added). “Strained silicon channel 104” is “selectively grown on the seed fin 105.” *Id.*, 12:52-55. Lee further describes that a channel layer such as “strained silicon channel 104” is made of an “epitaxial **silicon** layer deposited on a relaxed silicon germanium seed fin.” *Id.*, 11:32-38 (emph. added).

121. Accordingly, Lee describes its composite fin structures as having a strained epitaxy layer that is a strained silicon epitaxy layer, thereby satisfying claim 8.

9. Claim 9

[9] The Tri-gate device of claim 8 wherein said strained silicon epitaxy layer has a thickness of about 50-300 angstroms.

122. Lee discloses that its strained silicon epitaxy layer (e.g., “strained silicon layer,” “silicon layer 11,” “strained silicon channel 104,” “epitaxial silicon layer”) has a thickness that “is preferably in the range of 5 nm to 15 nm.” TSMC-1004, 4:38-40. 5-15 nanometers is equivalent to 50-150 angstroms, and thus Lee satisfies claim 9.

10. Claim 10

[10] The Tri-gate device of claim 6 wherein said gate strip is made of polysilicon or metal gate.

123. Lee discloses that the “gate of the disclosed strained silicon finFET structure is preferably polysilicon, doped polysilicon or metal.” TSMC-1004, 13:40-42; *see also id.*, 15:10-36 (“The *gate material can be polysilicon*, silicon germanium, a *refractory metal* or compound such as titanium nitride or molybdenum, *or other suitable conductive material such as aluminum, copper, or aluminum copper alloy*.... The *polysilicon gate* 225 may also be doped at this step if not already doped.”). Accordingly, a POSITA would understand that Lee’s gate strip (e.g., “gate 103”) is made of polysilicon or metal, and either one satisfies claim 10.

B. Ground 2: Lee in combination with Chau renders Claim 3 unpatentable

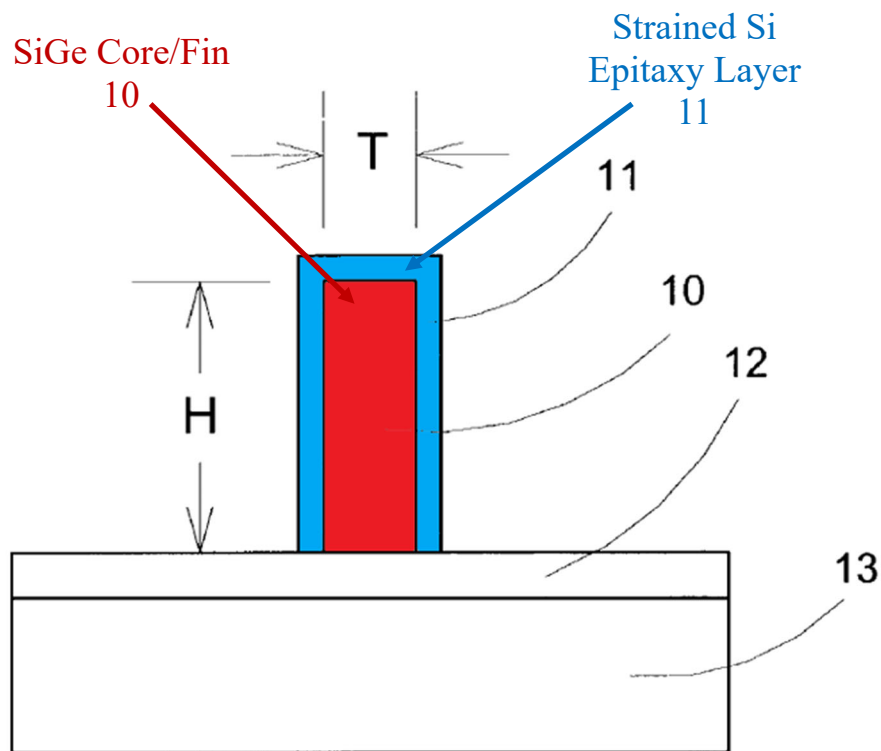
1. Claim 3

[3] The Tri-gate device of claim 2 wherein said composite fin structure has a width of said flat top surface that is approximately equal to its height.

124. As discussed above, Lee’s composite fin structure (e.g., “strained silicon fin structure,” “silicon fin channel,” “finFET channel”) has a width of said

substantially flat top surface that is approximately equal to its height. TSMC-1004, 4:33-43, Figs. 1, 14; *supra*, §IX(A)(3).

125. Lee's composite fin structure (which consists of the combination of silicon germanium fin 10 and strained silicon epitaxy layer 11) is depicted for example in Figure 1 (as annotated and reproduced below):



126. As depicted in Figure 1 of Lee above, the silicon germanium fin 10 of the composite fin structure 10/11 has a “height H” and a “thickness T” (or “width”). See TSMC-1004, 4:12-43. Lee further describes preferred ranges for these dimensions. Specifically, Lee states that its “seed fin” (e.g., “silicon germanium fin 10,” “seed fin 105”) has a “height H [that] is preferably in the range of 10 nm to 200

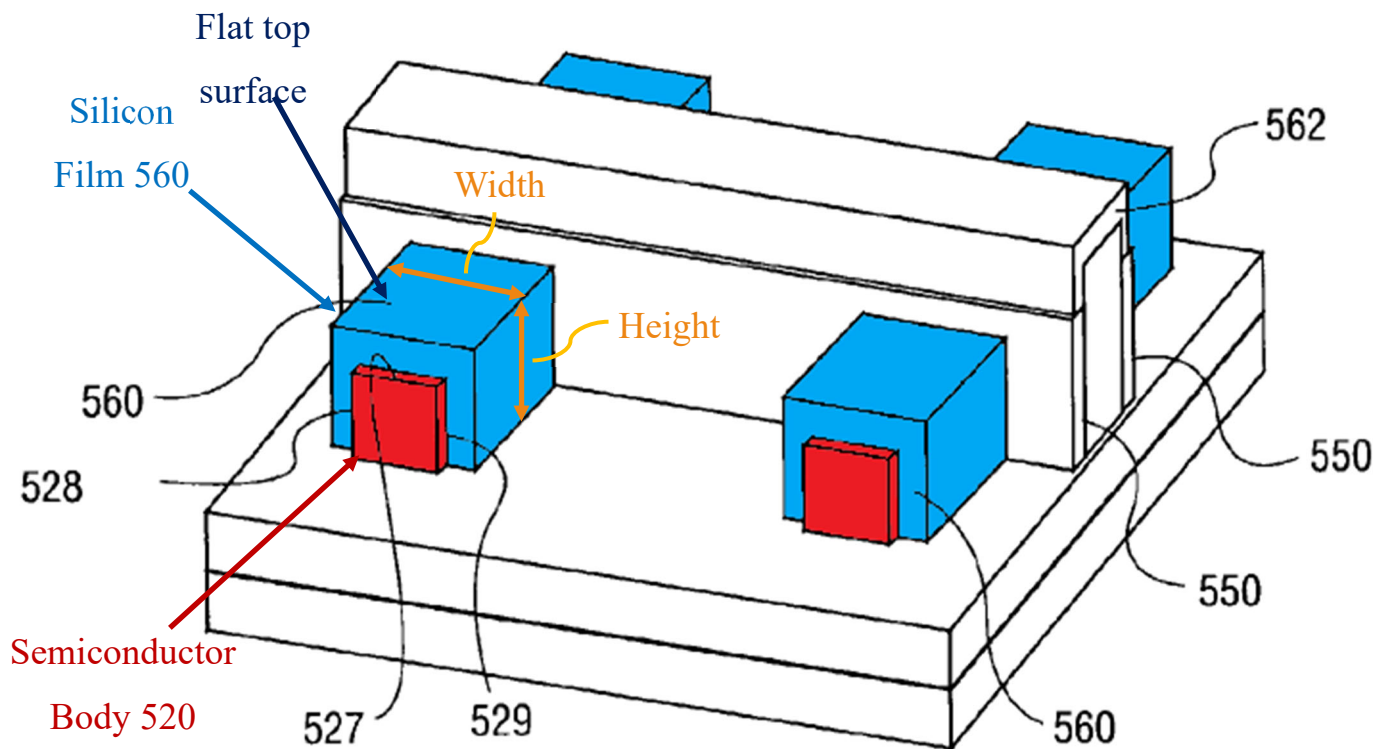
nm” and a “thickness T” (i.e., a “width”) that “is preferably in the range of 5 nm to 100 nm.” TSMC-1004, 4:36-38.

127. Additionally, as depicted in Figure 1 of Lee and discussed above with respect to claim 1, a strained epitaxial silicon layer 11 is formed on the silicon germanium seed fin 10. *See* TSMC-1004, 4:12-19 (“a strained channel silicon layer 11 covers a relaxed silicon germanium fin seed fin 10 on an insulator layer 12. The relaxed silicon germanium fin 10 is preferably disposed on an insulator layer 12 (such as silicon dioxide) on a silicon substrate 13. The seed fin 10 is a relaxed silicon germanium fin having lattice constant larger than the lattice constant of silicon, therefore the epitaxial silicon layer 11 grown on the seed fin 10 will be tensilely strained”), Fig. 1. Lee further describes a preferred thickness for this layer, stating that the “epitaxial silicon layer” (e.g., “strained channel silicon layer 11,” “strained silicon channel 104”) has a “thickness [that] is preferably in the range of 5 to 15nm.” *Id.*, 4:38-40. The thickness of the epitaxial silicon layer is uniform on the top and the sides.

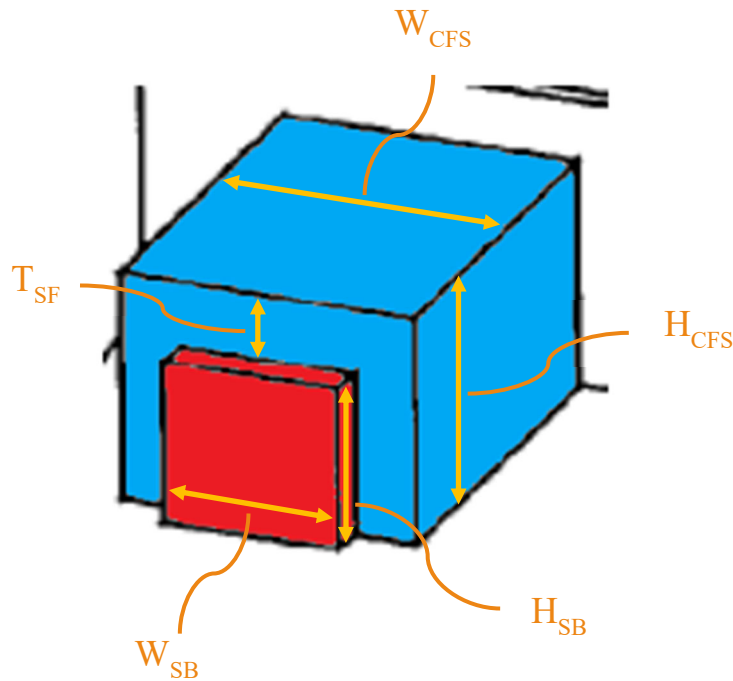
128. As discussed above, a POSITA would understand Lee to disclose a composite fin structure having a substantially equal height and width. Alternatively, it was further apparent and thus obvious in view of Chau for a POSITA to choose dimensions from Lee’s disclosed ranges such that Lee’s composite fin structure

would have a width of its substantially flat top surface that is approximately equal to its height, as recited in claim 3.

129. Like Lee, Chau also discloses a tri-gate transistor having a composite fin structure (e.g., combination of “semiconductor body 520” and “silicon film 560”) where a width of its substantially flat top surface is approximately equal to its height. See TSMC-1007, [0002] (“Chau is directed to a “tri-gate full depleted substrate transistor and its methods of fabrication.”), Figs. 3, 4A, 5G-5H, 6. As depicted in annotated Figure 5H below, Chau’s tri-gate transistor includes a composite fin structure that consists of a “semiconductor film 560 ... formed on the exposed surfaces of semiconductor body 520” (*id.*, ¶[0048]):



The semiconductor body 520 may be silicon germanium (TSMC-1007, ¶[0033]), and the silicon film 560 may be an epitaxial silicon film (*id.*, ¶[0048]). As depicted above, the “width” of the flat top surface of the composite fin structure and the “height” of the composite fin structure are shown in orange. Thus, focusing on one composite fin structure of Figure 5H, as annotated below, the height of the composite fin structure (i.e., H_{CFS}) is equal to the height of the semiconductor body (i.e., H_{SB}) plus the thickness of the silicon film (i.e., T_{SF}), i.e., $H_{CFS} = H_{SB} + T_{SF}$:



Likewise, the width of the composite fin structure (i.e., W_{CFS}) is equal to the width of the semiconductor body (i.e., W_{SB}) plus two times the thickness of the silicon film (i.e., T_{SF}), i.e., $W_{CFS} = W_{SB} + 2 * T_{SF}$.

130. Chau discloses that its semiconductor body (e.g., semiconductor body 520, which is also element 308 in Figure 3) may have a height/thickness that is “substantially equal” to its width, and further states that the height/thickness may be varied between $\frac{1}{2}$ and 2 times the width. *See, e.g.*, TSMC-1007, ¶¶[0017] (“the structure of the tri-gate transistor of the present invention enables a fully depleted transistor to be fabricated where ***the thickness of the semiconductor body and width of the semiconductor body are equal to the gate length of the device.***”), [0019] (“In an embodiment of the present invention the ***body height 320 is substantially equal to the body width 314.*** In an embodiment of the present invention, the body 308 has a width 314 and height 320 less than 30 nanometers and ideally less than 20 nanometers. In an embodiment of the present invention, the ***body height 320 is between $\frac{1}{2}$ the body width 314 to 2 times the body width 314.***”), [0020], [0034], [0037] (“In an embodiment of the present invention, the patterns 512 for the ***semiconductor bodies or fins have a width 518 approximately equal to the silicon body height 509.*** In an embodiment of the present invention, the photoresist patterns 512 have a ***width 518 which is between $\frac{1}{2}$ the semiconductor body height 509 and two times the semiconductor body height 509.***”), [0048] (emph. added). Chau also states that the height and width of the semiconductor body are equal to the gate length, and that the gate length may be “less than 60 nm.” *See id.*, ¶[0017] (“the structure of the tri-gate transistor of the present invention enables a fully depleted

transistor to be fabricated where *the thickness of the semiconductor body and width of the semiconductor body are equal to the gate length* of the device”) (emph. added); claims 25-26 (“wherein said *gate length* of said transistor is less than or equal to the width of said silicon body; ... wherein said *gate length is less than 60 nanometers.*”)³. As such, a POSITA would recognize that Chau discloses a semiconductor body width and height of approximately 60 nm.

131. The silicon film 560 has a thickness of 50-500 angstroms (i.e., 5-50 nm). TSMC-1007, ¶[0048]. Depositing a 50 angstrom, or 5 nm, silicon film 560 on the semiconductor body 520 whose height and width are substantially the same, and within Chau’s disclosed values, results in the composite fin structure having a width of its flat top surface that is approximately equal to its height. For example, applying the foregoing semiconductor body height and width dimensions of approximately 60 nm, and the thickness of the silicon film 560 of 5 nm, results in $H_{CFS}=60\text{ nm}+5\text{ nm}=65\text{ nm}$; $W_{CFS}=60\text{ nm}+2*(5\text{ nm})=70\text{ nm}$, which the POSITA would understand to be approximately equal.

132. Still further, applying Chau’s additional disclosure for the width and height to be less than 30 nm and also the specific dimensions for the semiconductor

³ Claims 25 and 26 of Chau were included in the application originally filed on August 23, 2002. See TSMC-1018.

body height and width as disclosed by the plot lines in Chau's Figure 6 also results in a composite fin structure having an approximately equal height and width. Figure 6 of Chau depicts a chart plotting the "body height and body width" of the semiconductor body of Chau's composite fin structure that "will produce either fully depleted (F.D) or partially depleted (P.D) tri-gate transistors having gate length (L_g) of 30 nm (602) and 20 nm (604) respectively." TSMC-1007, ¶[0027]. The "body height" in Figure 6 is equivalent to the height of the semiconductor body 520, i.e., H_{SB} , and the "body width" is equivalent to the width of the semiconductor body, i.e., W_{SB} .

133. An annotated version of Chau's Figure 6 below depicts specific points along the plot lines and the corresponding height and width dimensions for the associated semiconductor body at those points. The specific plot lines of Figure 6 define boundaries between fully-depleted transistors and partially-depleted transistors for respective gate lengths, where those boundaries correspond to specific body height and width dimensions. *See* TSMC-1007, ¶[0027] ("FIG. 6 is an illustration of two plots 602 and 604 which set forth the body height and body width which will produce either fully depleted (F.D) or partially depleted (PD) tri-gate transistors having gate length (L_g) of 30 nm (602) and 20 nm (604) respectively. In an embodiment of the present invention, the body height, body width and gate length are chosen to have dimensions in which a fully depleted transistor will be formed.

In other embodiments, the tri-gate transistor has a body height, body width and gate length such that a partially depleted transistor is formed.”). As such, each plot line identifies specific threshold body height and width dimensions for a fully-depleted transistor at the respective gate lengths associated with the plot line.

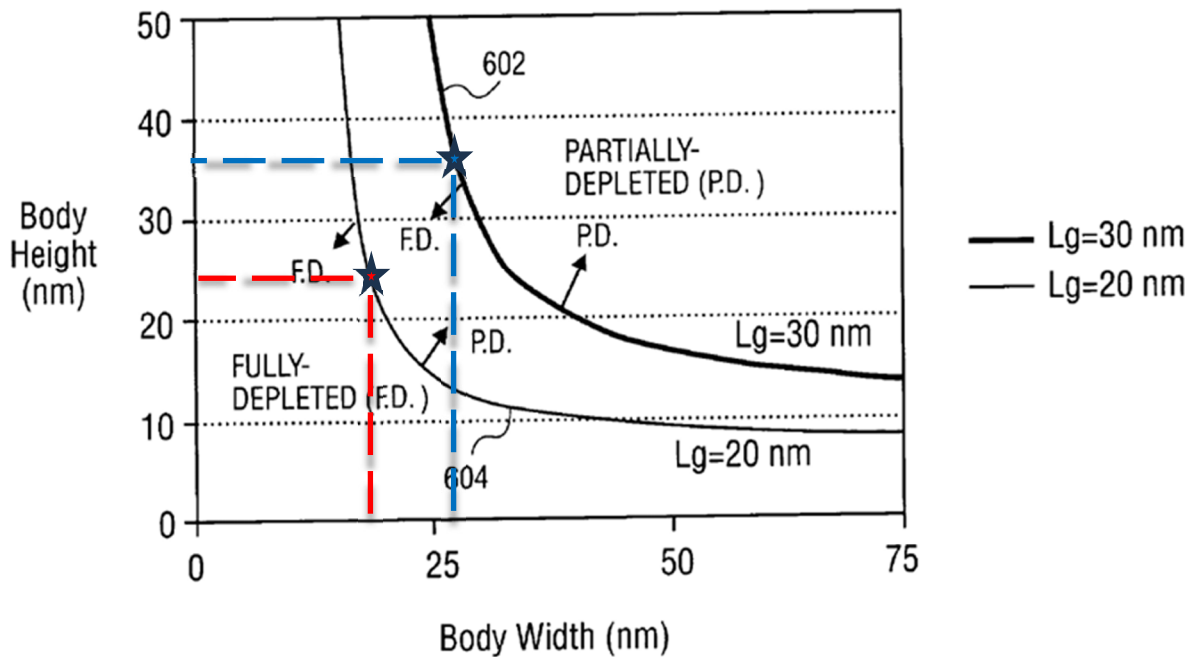


FIG. 6

134. As demonstrated by the graph of Fig. 6, it was known to a POSITA that the height and width dimensions of a fin could be varied for a given gate length to ensure full depletion. If a fully depleted transistor is desired, a POSITA was motivated to use dimensions at the boundary between fully-depleted and partially-depleted zones (i.e., along plot lines 602, 604), taking into account manufacturing variability, because devices having the relatively larger dimensions along this

boundary (as compared to further into the fully-depleted zone) are generally easier to manufacture and have a lower cost.

135. Accordingly, as shown above, the selected point (star at red line intersection) on plot line 604 (i.e., the plot line associated with the 20 nm gate length transistor) has a body height (H_{SB}) of approximately 24 nm and a body width (W_{SB}) of approximately 19 nm. As noted above, the height and width of the associated composite fin structure (i.e., H_{CFS} , W_{CFS}) includes the thickness of the silicon film 560 (i.e., T_{SF}). Regarding “silicon film 560,” Chau states that “silicon film 560 is formed to a thickness between **50-500** [angstroms]” (i.e., **5-50 nm**). TSMC-1007, ¶[0048] (emph. added).

136. Thus, combining Chau’s disclosed silicon film thickness of 5 nm with the disclosed height and width dimensions for the semiconductor body 520 associated with plot line 604 (i.e., body height (H_{SB}) of approximately 24 nm and body width (W_{SB}) of approximately 19 nm) gives a width of the composite fin structure that substantially equals a height of the composite fin structure. Specifically, $W_{CFS} = W_{SB} + 2 * T_{SF} = 19 \text{ nm} + 2 * 5 \text{ nm} = \underline{\mathbf{29 \text{ nm}}}$; and $H_{CFS} = H_{SB} + T_{SF} = 24 \text{ nm} + 5 \text{ nm} = \underline{\mathbf{29 \text{ nm}}}$.

137. Similarly, the selected point (star at blue line intersection) on plot line 602 has a body height (H_{SB}) of approximately 37 nm and a body width (W_{SB}) of approximately 27 nm. An epitaxial silicon layer thickness of 10 nm (within Chau’s

range of 5-50 nm) results in both the total width and total height of the composite fin structure being 47 nm. The height and width values of the semiconductor body and the thickness of the silicon film for each of these examples are within the ranges taught by Lee. TSMC-1004, 4:36-40 (disclosing seed fin height from 10-200 nm, seed fin width from 5-100 nm, and epitaxial silicon layer thickness from 5-15 nm).

138. Further, these values of height and width of the semiconductor body and film thickness of the silicon film are entirely consistent and in the ranges taught by Lee. TSMC-1004, 4:36-40 (disclosing seed fin height in range 10 nm to 200 nm, seed fin width in range 5nm to 100 nm, and epitaxial silicon layer thickness in range 5 to 15 nm). In view of at least the foregoing, a POSITA would recognize that Chau teaches a composite fin structure having a height that is approximately equal to the width of its substantially flat top surface.

139. Thus, in addition to Lee disclosing a composite fin structure having approximately equal width and height dimensions, it was obvious to incorporate a composite fin structure having approximately equal width and height dimensions into Lee's tri-gate device in view of the teachings of Chau. Choosing the specific width and height dimensions of the composite fin structure are merely dependent on the design goals for the ultimate device, the selection of which would be dictated by manufacturing limitations and/or designer preferences regarding the desired performance characteristics of the FinFET device including full/partial depletion

characteristics, current carrying capacity, space limitations, cost, manufacturing complexity, etc. *See supra*, §IX(A)(3). As discussed above, Lee expresses a desire to “ensure fully depleted body under the operation conditions of the finFET device” when selecting such dimensions. *See* TSMC-1004, 4:36-43. Thus, a POSITA would have found it obvious and been motivated to choose dimensions that create a fully depleted body while balancing other design goals, which would include considering and choosing equal height and width dimensioned composite fin structures when suitable.

140. Because equal height and width dimensions were well-known options (as demonstrated by the foregoing discussion of Chau as well as Lee) and easily achievable given the overlapping height and width dimension ranges expressly contemplated by Lee, when motivated by overall design considerations, it was obvious to a POSITA to select approximately equal height and width dimensions for the resulting composite fin structure when designing and manufacturing the device. Additionally, the approximately equal height and width dimensions of the claim composite fin structure are not critical nor do they produce any unexpected results, and the '181 Patent does not provide any indication that they do. *See supra*, §IX(A)(3).

141. Moreover, a POSITA would have been motivated to use a composite fin structure having approximately equal width and height dimensions for a number

of reasons. For example, a POSITA would have been motivated to select such approximately equal dimensions so that the resulting FET device operates properly when fully depleted, including with excellent short channel performance and optimized sub-threshold gradients. *See, e.g.*, TSMC-1007, ¶¶[0005] (“Fully depleted SOI have been proposed as a transistor structure to take advantage of ideal sub-threshold gradients for optimized on current/off current ratios.”), [0027] (“the [equal] body height, body width and gate length are chosen to have dimensions *in which a fully depleted transistor will be formed*”); TSMC-1013, Abstract (“Furthermore, three-dimensional (3-D) simulations of tri-gate transistors with transistor gate lengths down to 30 nm show that the 30 nm tri-gate device *remains fully depleted, with near-ideal subthreshold swing and excellent short channel characteristics*, suggesting that the tri-gate transistor could pose a viable alternative to bulk transistors in the near future.”), 3 (“Three-dimensional simulations of the tri-gate transistor with $L_g = T_{Si} = W_{Si} = 30$ nm show that the *tri-gate device maintains full depletion at these dimensions, and exhibit excellent short channel performance*, and suggest that this transistor design could supplant bulk CMOS transistors in the near future.”). Indeed, Lee expressly discloses a desire for optimizing dimensions of the fin structure in order to ensure a “fully depleted body.” TSMC-1004, 4:40-43 (“The optimized dimensions of the disclosed strained silicon fin structure are preferably chosen to ensure fully depleted body under the operation

conditions of the finFET device.”). As demonstrated above with respect to its Figure 6, Chau teaches that FET devices having a composite fin structure with approximately equal height and width dimensions achieve this goal by enabling a fully-depleted device with the improved performance characteristics, and thus a POSITA would have been motivated to use such a fin structure when design goals called for such a fully-depleted device.

142. Additionally, a POSITA would have been motivated to use a composite fin structure having approximately equal width and height dimensions to simplify device fabrication. Traditional double-gate FinFET devices utilized high aspect ratio fins that become difficult to fabricate as the overall size of the FinFET device is shrunk due to the increasing narrowness of the fin relative to its height. *See* TSMC-1012, 1 (“FinFET double-gate transistors have been offered for future transistor design, but, while this device offers excellent short channel effect (SCE) control, *the vertical nature of the device and the difficulties in fabricating such a device* suggest that the Tri-Gate might be the next transistor design.”). In contrast, the larger widths associated with the fins of triple-gate devices that have approximately equal heights and widths facilitate easier manufacturing. *See id.*; *see also* TSMC-1013, Abstract (“The tri-gate devices also demonstrate full depletion at silicon body dimensions approximately 1.5–2 times greater than either single gate SOI or non-planar double-gate SOI for similar gate lengths, indicating that these devices are

easier to fabricate using the conventional fabrication tools.”). Indeed, Chau discusses the well-known preference at the time to avoid “ultra-thin” fins, largely due to the difficulty of manufacturing such high aspect ratio structures. *See* TSMC-1007, ¶[0017] (“thereby enabling the formation of a fully depleted transistor with gate lengths of less than 30 nanometers *without requiring the use of ultra-thin semiconductor bodies or requiring photolithographic patterning of the semiconductor bodies to dimensions less than the gate length* (L_g) of the device”). Thus, a POSITA would have been motivated to use such a fin structure having approximately equal height and widths to simplify device fabrication.

143. A POSITA would have found implementing approximately equal height and width dimensions for the composite fin structure to be routine and easily achievable (and indeed easier than high aspect ratio double-gate devices as discussed above) at the time of the alleged invention, and thus would have had a reasonable expectation of success in doing so. Indeed, such a modification merely would have amounted to creating a composite fin structure having the selected approximately equal height and width dimensions while utilizing the same fabrication techniques (e.g., well-known photolithographic, etching, and deposition techniques) already widely used at the time for creating fin structures in FinFET devices. For example, Chau’s composite fin structures are formed using “well-known photolithographic and etching techniques” (e.g., to form the semiconductor body/core of the composite

fin structure) and epitaxial deposition processes (e.g., for forming the semiconductor/silicon film 560 portion of the composite fin structure). *See* TSMC-1007, ¶¶[0036]-[0038], [0048], Figs. 5A-5H. Lee utilizes similar processes for forming its composite fin structures. *See* TSMC-1004, 13:43-14:67 (“A **photoresist is applied to define a pattern** through the use of optical **lithography**, electron beam lithography, X-ray lithography, or other conventional means to produce a photoresist mask comprising a fin channel between a source and drain structures. After the photoresist mask definition, an **etch process is used to pattern** the silicon germanium layer 204 and the silicon layer 203.... A selective **epitaxial silicon layer is next deposited** on the seed fin surface as shown in FIG. 18c.”). The foregoing fabrication processes were well-known to a POSITA prior to the '181 Patent, and thus a POSITA would have found it relatively simple to implement such processes to fabricate a composite fin structure have approximately equal height and width dimensions.

144. Accordingly, a POSITA would have found claim 3 obvious over the combination of Lee and Chau.

C. Ground 3: Sugiyama anticipates Claims 1-10

1. Claim 1

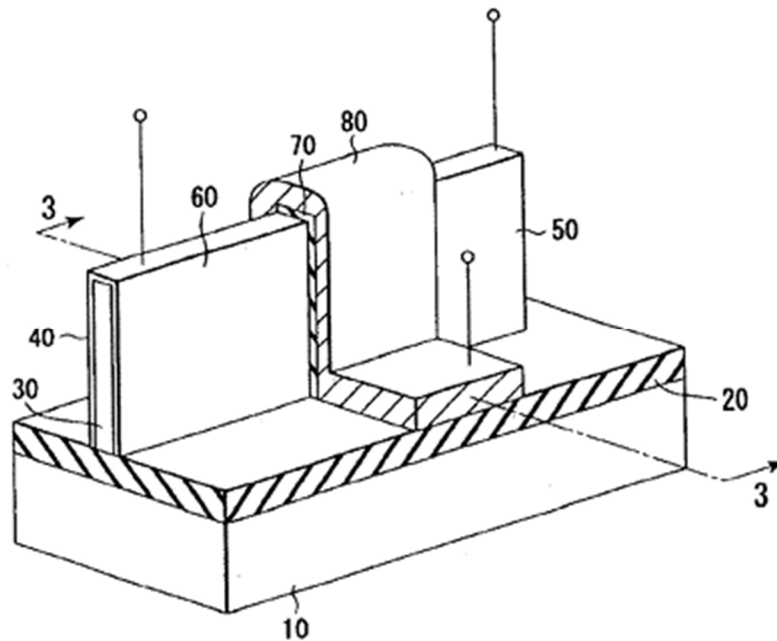
1[pre] “Three Dimensional Triple Gate (Tri-gate) Device”

145. Sugiyama discloses a three dimensional triple gate (Tri-gate) device (e.g., “semiconductor device,” “MISFET”). TSMC-1005, Abstract, 6:63-7:10, 10:4-55, Figs. 2, 3B, 12B-14C.

146. For example, Sugiyama discloses “a MISFET using, as a channel layer, a second semiconductor layer such as a strained Si layer which is joined to a first semiconductor layer such as a SiGe crystal layer formed on an insulating layer, has a lattice constant different from that of the first semiconductor layer, and has a stress strain in crystal lattices.” TSMC-1005, 5:35-42.

147. In one example, Sugiyama teaches that the MISFET includes a “projecting SiGe layer (semiconductor board) 30,” a “strained Si layer (semiconductor layer) 40 [that] is formed on the side and upper surfaces of the SiGe layer 30,” and a “band-like gate electrode 80 [that] is so formed as to cover the vertical surfaces and horizontal upper surface of the strained Si layer 40.” *Id.*, 6:63-7:10 (“In a MISFET according to the first embodiment, as shown in FIGS. 2, 3A, and 3B, an insulating layer 20 such as silicon oxide is formed on a semiconductor substrate 10, and a projecting SiGe layer (semiconductor board) 30 is formed on the insulating layer 20. A strained Si layer (semiconductor layer) 40 is formed on the side and upper surfaces of the SiGe layer 30 so as to cover this SiGe layer 30. The strained Si layer 40 suffices to be formed on at least one of the vertical surfaces of the SiGe layer 30. The strained Si layer 40 may be continuously formed on the

vertical surfaces in parallel to each other and horizontal upper surface, as shown in FIG. 2. A band-like gate electrode 80 is so formed as to cover the vertical surfaces and horizontal upper surface of the strained Si layer 40 via a gate insulating layer 70.”). Figure 2 depicts one example of such a MISFET of Sugiyama:



148. A POSITA at the time would have understood the foregoing “MISFET” of Sugiyama to be a “three dimensional triple gate device” including because of the presence of the three-dimensional semiconductor board 30/strained layer 40 (i.e., a composite fin structure) and a gate electrode that covers three surfaces of the semiconductor board 30/strained layer 40 (i.e., both side surfaces and the top surface of the semiconductor board 30/strained layer 40). *See* TSMC-1005, 6:63-7:10, Figs. 2, 3B, 12B; *see also* TSMC-1004, 12:26-30 (“The double gate 103 ***is actually a triple gate because it covers both sides and the top of the strained silicon channel***

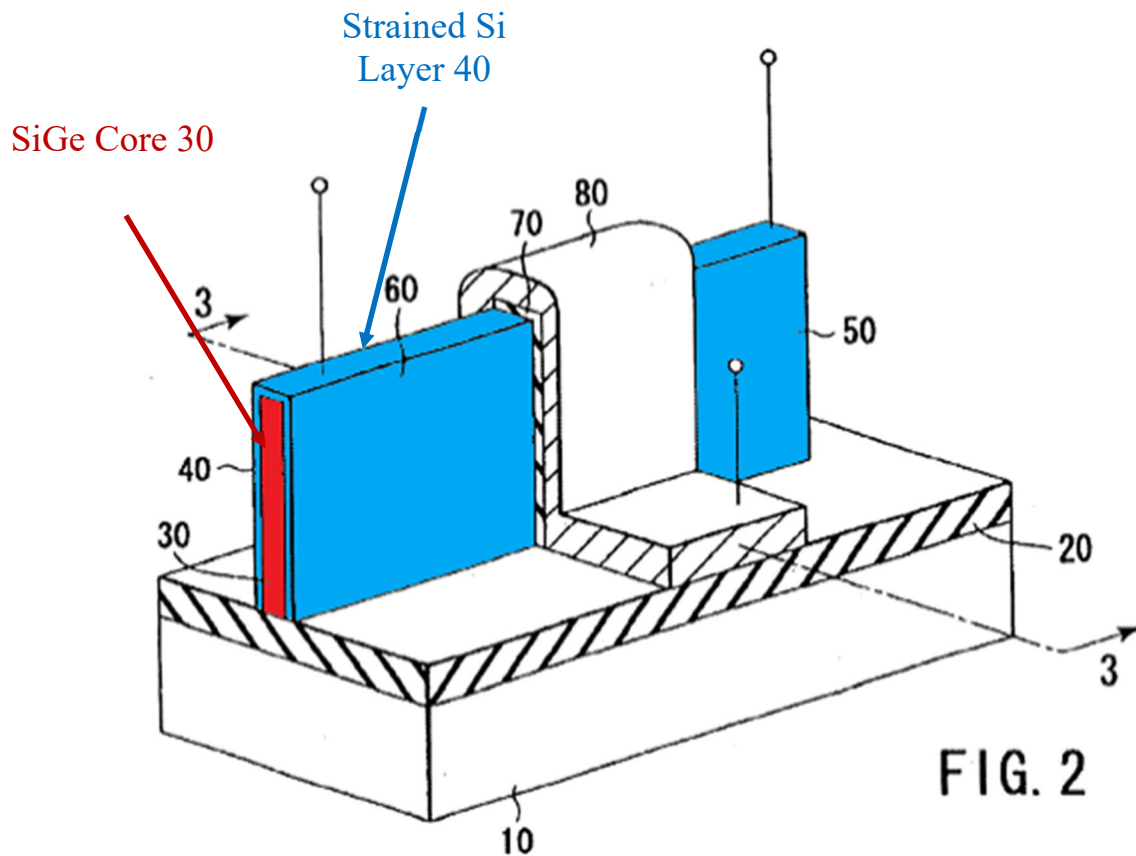
104. The term ‘double gate’ in the context of the present invention is a generic term to mean ‘more than one gate’ and therefore covers double or triple gate device.”) (emph. added).

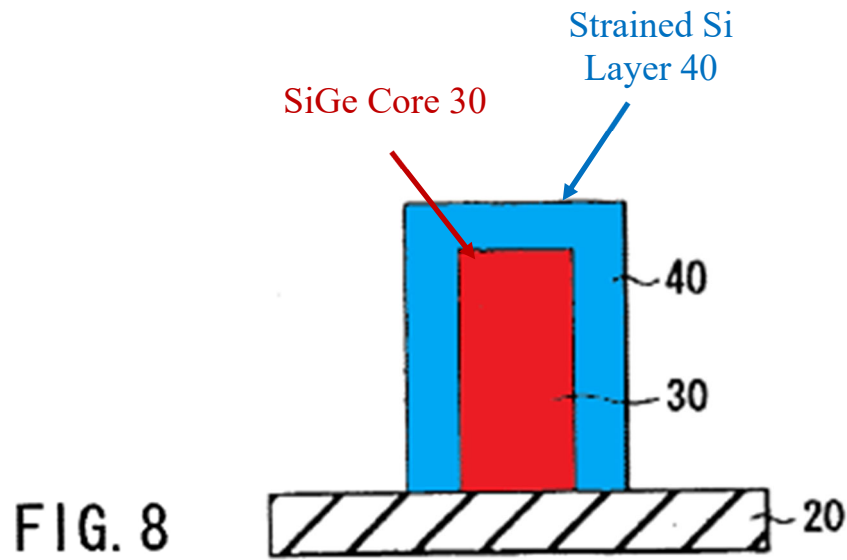
149. Accordingly, a POSITA would understand the MISFET devices disclosed in Sugiyama constitute a “three dimensional Triple Gate (Tri-gate) device,” as recited in the preamble of claim 1.

1[a] “Composite Fin Structure”

150. Sugiyama’s MISFET devices include a composite fin structure consisting of: (i) a silicon germanium core (e.g., “SiGe layer (semiconductor board) 30”) and (ii) a strained silicon epitaxy layer (e.g., “strained Si layer (semiconductor layer) 40”) grown from surface of said silicon germanium core. *See* TSMC-1005, Abstract, 5:35-42 (“The present invention has been made to solve this problem, relates to a MISFET using, *as a channel layer, a second semiconductor layer such as a strained Si layer which is joined to a first semiconductor layer such as a SiGe crystal layer* formed on an insulating layer, has a lattice constant different from that of the first semiconductor layer, and has a stress strain in crystal lattices, and also relates to a CMIS circuit which is combined with the MISFET.”) (emph. added); *see also id.*, 5:55-61, 6:63-7:10, Figs. 2, 3B, 8.

151. Figures 2 and 8 each depict Sugiyama's composite fin structure as shown below with annotations highlighting its constituent layers (i.e., silicon germanium core 30 in red and strained silicon layer 40 in blue):





152. Regarding Figures 2 and 8 (which use common reference numbers for the same components, 7:64-67), Sugiyama describes a “projecting *SiGe layer* (semiconductor board) 30 [that] is formed on the insulating layer 20” and a “*strained Si layer* (semiconductor layer) 40 [that] is formed *on the side and upper surfaces* of the SiGe layer 30 so as to cover this SiGe layer 30.” TSMC-1005, 6:65-7:3 (emph. added). “Strained Si layer 40” is “grown” on “the surface of the SiGe crystal layer 30 *by epitaxial growth.*” *Id.*, 9:46-47 (emph. added); *see also id.*, 5:18-19 (“a strained Si layer 140 *epitaxially grown* on the upper SiGe crystal layer 130 are formed on a Si substrate 110.”) (emph. added), Figs. 2, 8. Accordingly, a POSITA would recognize that the foregoing strained silicon layer 40 described in Sugiyama is an epitaxy layer grown from the surface of the silicon germanium core 30.

153. Accordingly, given Sugiyama's teachings regarding the epitaxial growth of a strained silicon layer on the surface of the silicon germanium core, a POSITA would understand that Sugiyama's MISFET devices include a composite fin structure consisting of a silicon germanium core and a strained silicon epitaxy layer grown from the surface of said silicon germanium core, thereby satisfying this limitation.

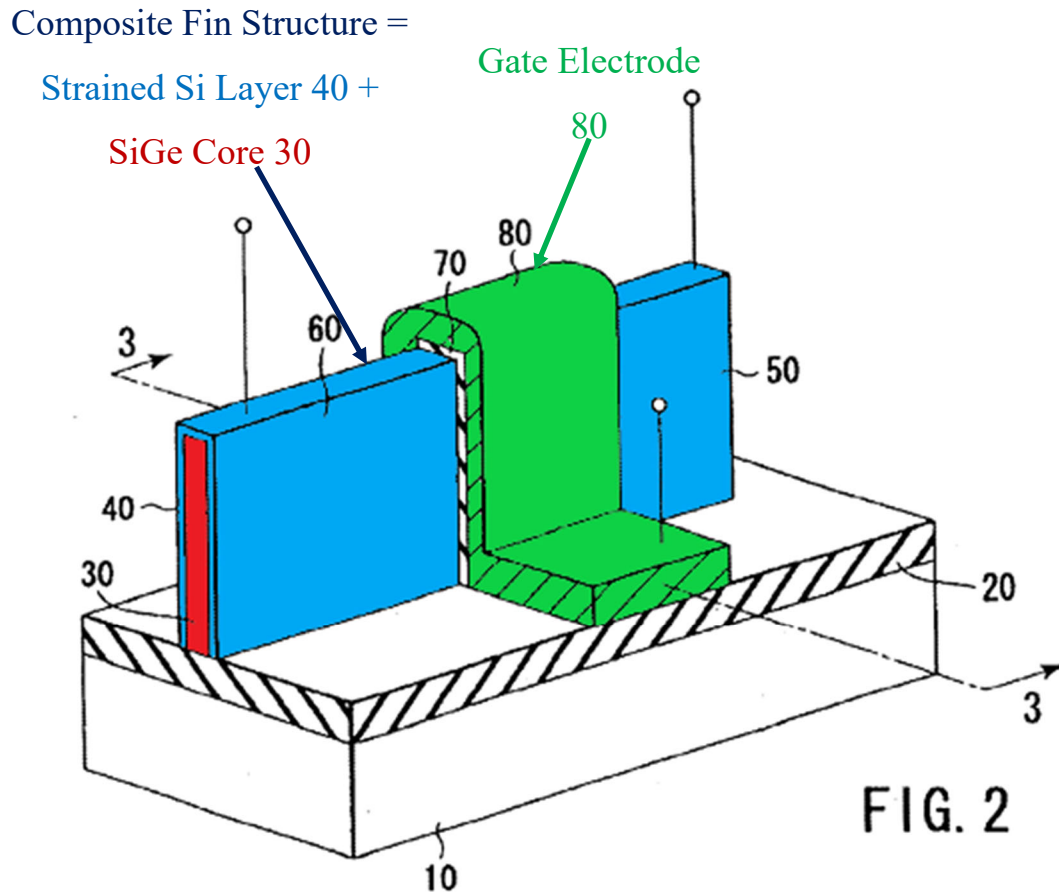
1[b] "Gate Strip"

154. Sugiyama discloses a gate strip, e.g., "gate electrode 80," wrapping a portion of said composite fin structure. TSMC-1005, 5:44-51 ("In the MISFET, the second semiconductor layer is joined to at least one of the major side surfaces of the first projecting semiconductor layer which is formed on the insulating layer in a board-like shape. In *forming a gate on the second semiconductor layer*, the gate is formed such that the area of a channel portion in the surface of the second semiconductor layer is set smaller than the junction area between the SiGe layer and the insulating layer.") (emph. added), Figs. 2, 3B. For example, Sugiyama states that a "*band-like gate electrode 80* is so formed as to cover *the vertical surfaces and horizontal upper surface* of the strained Si layer 40 via a gate insulating layer 70." *Id.*, 7:8-10 (emph. added).

155. Annotated Figure 2 is shown below, depicting Sugiyama's gate electrode 80 (in green) wrapping a portion of the composite fin structure (i.e., the

combination of strained silicon layer 40 and silicon germanium layer 30) on the vertical surfaces and the upper surface of the composite fin structure, where some portions of the composite fin structure are covered and other portions remain uncovered.⁴

⁴ As also illustrated in Figure 2, Sugiyama discloses a gate insulating layer 70 between the gate electrode 80 and the composite fin structure. *See* TSMC-1005, 7:8-10 (disclosing that gate electrode 80 covers the vertical surfaces and horizontal upper surface of the strained Si layer 40 “via a gate insulating layer.”). The ’181 Patent embodiment is directly analogous, illustrating, in Figure 6, a gate insulating layer 70 between the composite fin structure 34/90 and the gate strip 60. TSMC-1001, 3:41-44, 3:60-4:8.

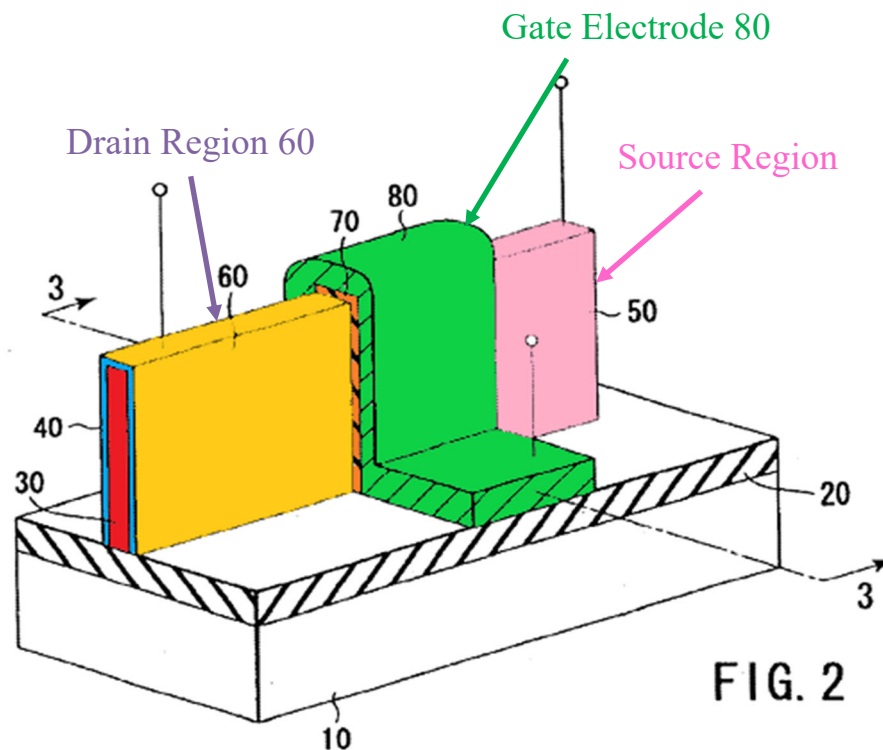


156. Accordingly, Sugiyama’s “gate electrode 80” constitutes a gate strip that wraps a portion of the combined strained silicon layer 40/silicon germanium layer 30 (i.e., the “composite fin structure”), satisfying this limitation.

1[c] “Source/Drain Regions”

157. Sugiyama discloses that portions of said composite fin structure (e.g., combination of “SiGe layer 30” and “strained Si layer 40”) not covered by said gate strip (e.g., “gate electrode 80”) constitute source/drain regions (e.g., “source region 50,” “drain region 60”) of said Tri-gate device. *See* TSMC-1005, 7:10-17, Fig. 2;.

Specifically, regarding the device of Figure 2, Sugiyama states that “[t]hose *portions of the strained Si layer 40 that are not covered with the gate insulating layer 70 and gate electrode 80* serve as a *source region 50 and drain region 60*.” *Id.*, 7:10-13 (emph. added). Sugiyama’s Figure 2 is reproduced and annotated below depicting the portions of the composite fin structure which are not covered by gate electrode 80, which constitute source region 50 (in pink) and drain region 60 (in gold):



See also TSMC-1005, 7:14-17 (stating that “[a] channel is formed in the strained Si layer 40 covered with the gate electrode 80 *between the source region 50 and the drain region 60*”) (emph. added).

158. Accordingly, the composite fin structures of Sugiyama's MISFET devices include portions not covered by gate electrode 80 that constitute source/drain regions 50/60 of the tri-gate device, thereby satisfying this limitation.

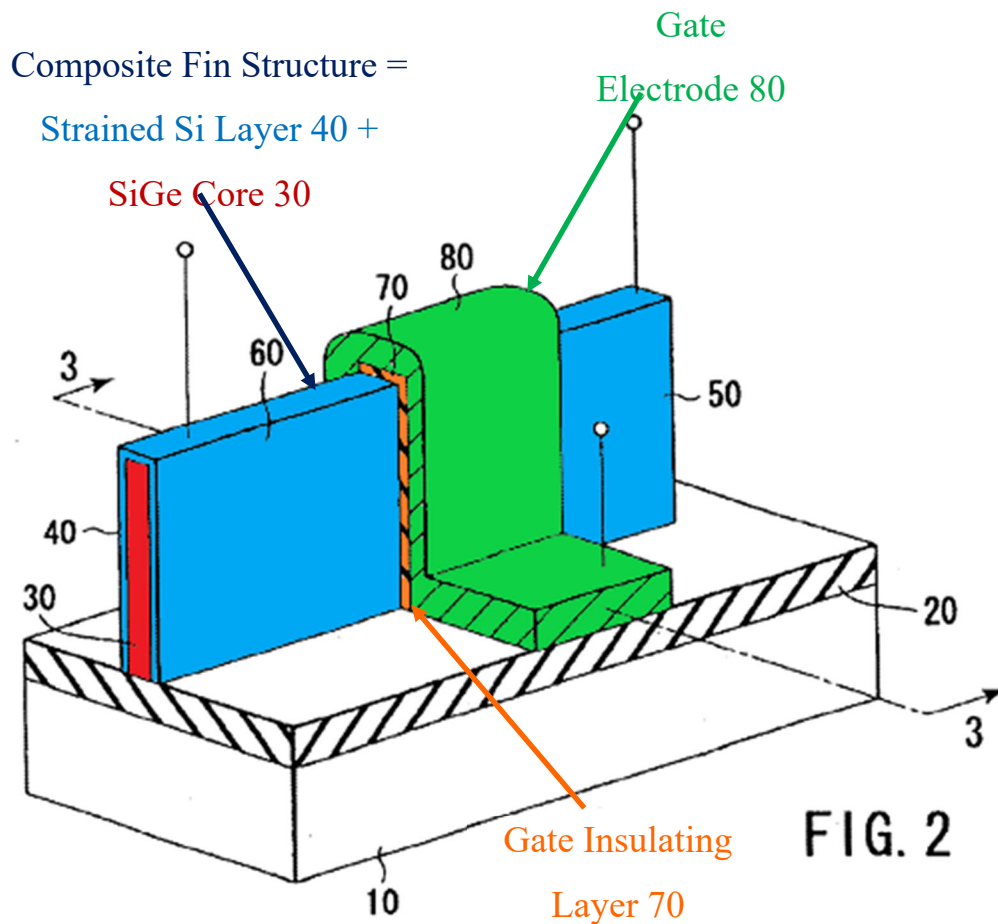
1[d] “Gate Insulating Layer”

159. Sugiyama discloses a gate insulating layer (e.g., “gate insulating layer 70”) interposed between said composite fin structure (e.g., combination of “SiGe layer 30” and “strained Si layer 40”) and said gate strip (e.g., “gate electrode 80”). See TSMC-1005, 7:8-21, 10:4-45, Figs. 2, 13B-14C.

160. Sugiyama states that a “band-like gate electrode 80 is so formed as to cover the vertical surfaces and horizontal upper surface of the strained Si layer 40 *via a gate insulating layer 70.*” TSMC-1005, 7:8-10 (emph. added). Regarding the formation of “gate insulating layer 70,” Sugiyama describes that “the surface of the strained Si layer 40 is thermally oxidized to form a second *insulating layer 70 as a gate insulating layer*” and, thereafter, “a band-like gate electrode 80 is formed on the surface of a part of the second insulating layer 70.” *Id.*, 10:4-20 (emph. added).⁵

⁵ Figures 9A to 14C depict gate processing for the second embodiment. TSMC-1005, 9:62-64, 4:38-44. See, e.g., Figures 10B, 10C, 11B, 11C, 12B, 12C, 13B, 13C 14B, 14C, each depicting gate insulating layer 70 between gate electrode 80(25) and composite fin structure 30/40. Figures 4-8 show the process steps for manufacturing the active region of the MISFET for the second embodiment.

161. As depicted in annotated Figure 2 below, gate insulating layer 70 is interposed between Sugiyama's composite fin structure (i.e., the combination of SiGe layer 30 and strained Si layer 40) and Sugiyama's gate strip (i.e., "gate electrode 80"):



TSMC-1005, 4:35-37. Further, common reference numbers are used for the same components between the first and second embodiments. *Id.*, 7:64-67.

162. Accordingly, Sugiyama's gate insulating layer 70 constitutes the claimed "gate insulating layer," satisfying this limitation.

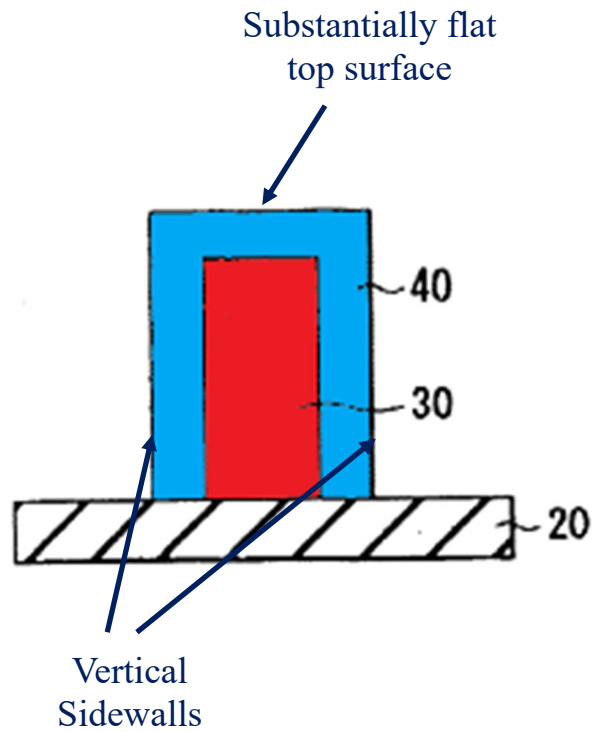
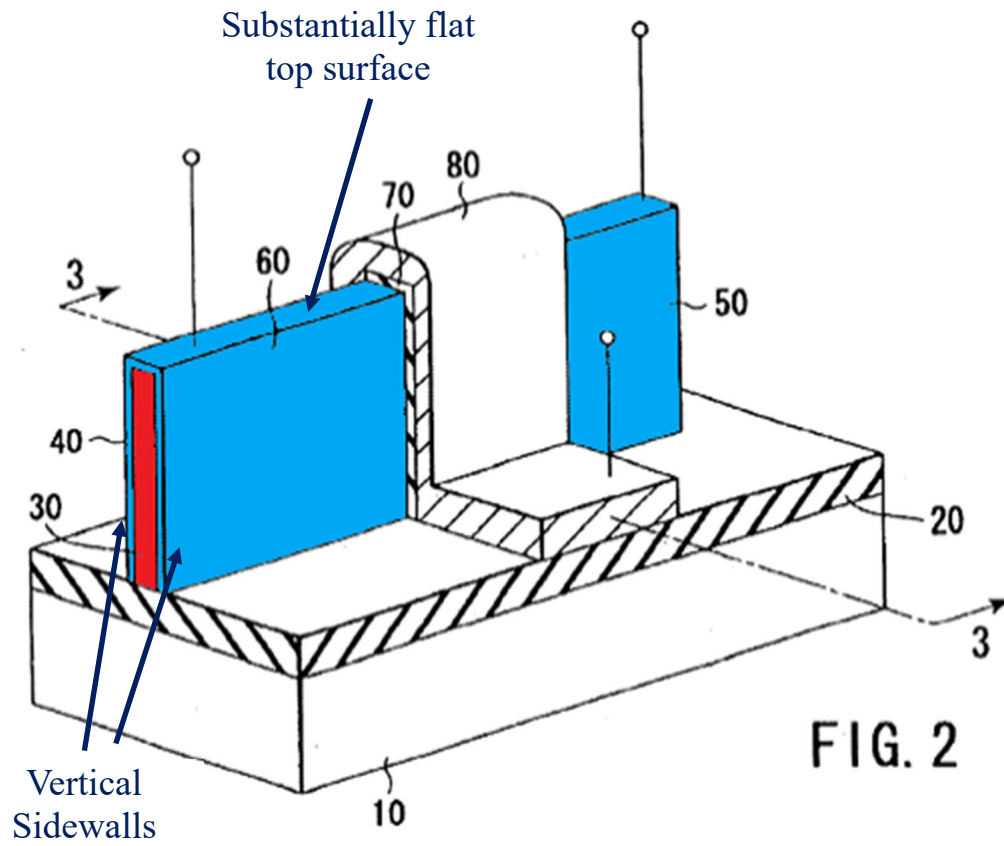
163. Sugiyama thus discloses all limitations of claim 1.

2. Claim 2

[2] The Tri-gate device of claim 1 wherein said composite fin structure has a substantially flat top surface and vertical sidewalls.

164. As depicted in annotated Figures 2 and 8 of Sugiyama below, Sugiyama's composite fin structure (e.g., the combination of "SiGe layer 30" and "strained Si layer 40") has a substantially flat top surface and vertical sidewalls. *See* TSMC-1005, 6:63-7:10 ("In a MISFET according to the first embodiment, as shown in FIGS. 2, 3A, and 3B, an insulating layer 20 such as silicon oxide is formed on a semiconductor substrate 10, and a projecting SiGe layer (semiconductor board) 30 is formed on the insulating layer 20. A strained Si layer (semiconductor layer) 40 is ***formed on the side and upper surfaces*** of the SiGe layer 30 so as to cover this SiGe layer 30. The strained Si layer 40 suffices to be formed on at least one of the ***vertical surfaces*** of the SiGe layer 30. The strained Si layer 40 may be continuously formed on the ***vertical surfaces in parallel to each other and horizontal upper surface***, as shown in FIG. 2. A band-like gate electrode 80 is so formed as to cover the ***vertical surfaces and horizontal upper surface*** of the strained Si layer 40 via a gate insulating layer 70.") (emph. added), Figs. 1, 3C, 8, 10C.

165. Sugiyama describes its strained silicon layer 40 (which forms the outer layer of Sugiyama's composite fin structure) as having a "horizontal upper surface" and "vertical surfaces," which for the same reasons discussed regarding Lee a POSITA would understand to correspond to the claimed "substantially flat top surface" and "vertical sidewalls" of the composite fin structure, respectively. *See* TSMC-1005, 7:4-10 ("The strained Si layer 40 may be continuously formed on the vertical surfaces in parallel to each other and horizontal upper surface, as shown in FIG. 2. A band-like gate electrode 80 is so formed as to cover the ***vertical surfaces and horizontal upper surface*** of the strained Si layer 40 via a gate insulating layer 70.") (emph. added); *see also supra*, §IX(A)(2). Annotated versions of Figures 2 and 8 of Sugiyama are shown below depicting these surfaces of Sugiyama's composite fin structure, where the composite fin structure has a top surface that is substantially flat top surface and has vertical sidewalls:



166. A POSITA would understand that the top surface and sidewalls of Sugiyama's composite fin structure are "substantially flat" and "vertical," respectively. Additionally, regardless of "substantially flat" and "vertical" are interpreted, the top surface and sidewalls of Sugiyama's composite fin structure are "substantially flat" and "vertical" at least to the same extent as the devices disclosed in the '181 Patent. Accordingly, the "horizontal upper surface" and "vertical surfaces," of Sugiyama's composite fin structure outlined above constitute a "substantially flat top surface" and "vertical sidewalls" of the composite fin structure, thereby satisfying claim 2.

3. Claim 3

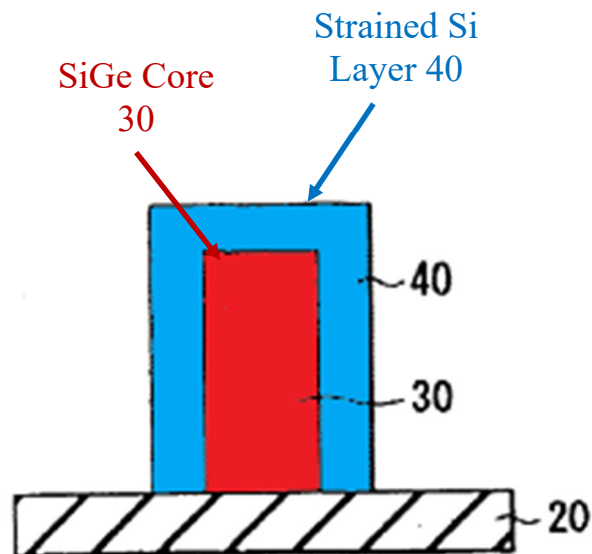
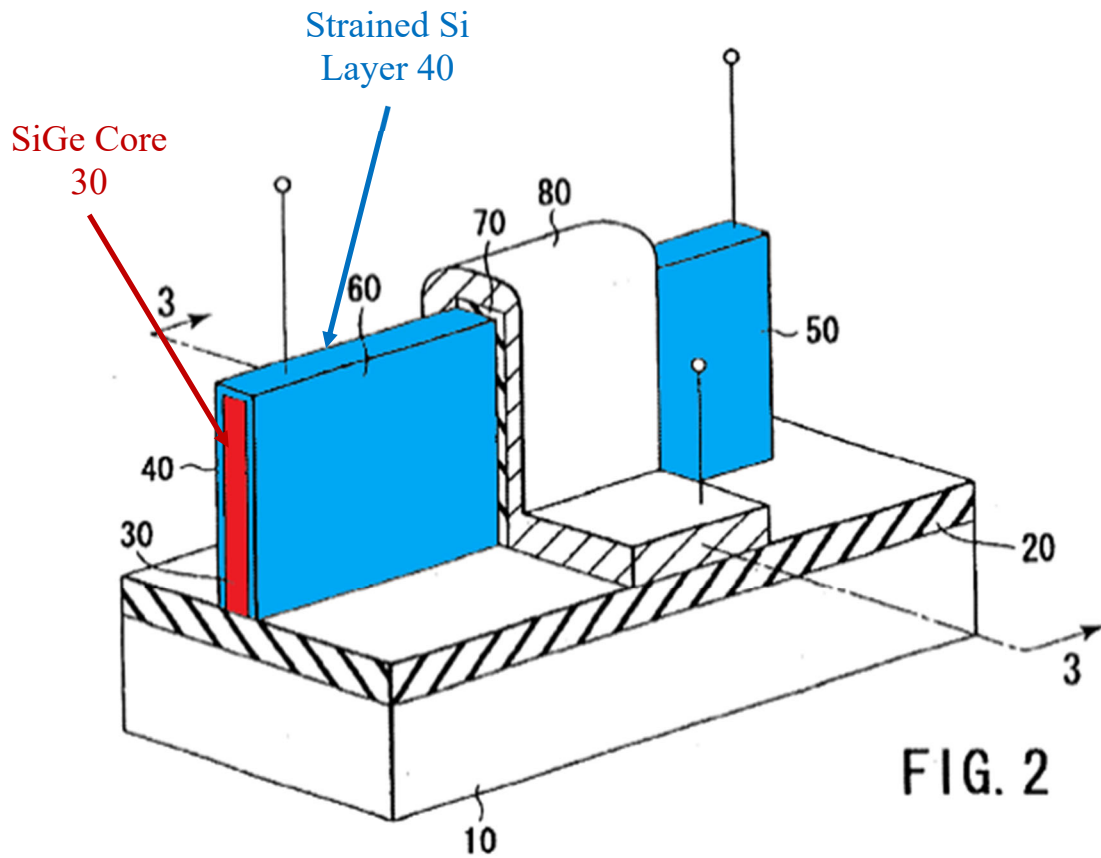
[3] The Tri-gate device of claim 2 wherein said composite fin structure has a width of said flat top surface that is approximately equal to its height.

167. Sugiyama's composite fin structure (e.g., combination of "SiGe layer 30" and "strained Si layer 40") has a width of said substantially flat top surface that is approximately equal to its height. *See* TSMC-1005, 9:30-50, Fig. 8; *supra*, §IX(C)(2).

168. Sugiyama states preferred dimension ranges for its SiGe layer 30 and strained Si layer 40. Specifically, Sugiyama's SiGe layer 30 has a "height W" of "50 nm or more" and a "width d" that is "desirably 10 nm (inclusive) to 50 nm

(inclusive).” TSMC-1005, 9:30-40 (“In the second embodiment, the width d of the board formed from the SiGe crystal layer 30 is desirably 10 nm (inclusive) to 50 nm (inclusive) in order to strain a Si crystal layer to be formed in the subsequent step. The depth (in this case, a length in a direction perpendicular to the sheet surface of FIG. 6) of the board formed from the SiGe crystal layer 30 determines the sum of the channel gate length and source/drain electrode length, and falls within the range of 0.5 μm (inclusive) to 5 μm (inclusive). A board height W determines the channel gate width, and must be 50 nm or more.”). Sugiyama’s strained Si layer 40 has a thickness that “is desirably 5 nm (inclusive) to 30 nm (inclusive).” *Id.*, 9:49-50.

169. As described above (*see supra*, §IX(C)(1)(1[a])) and shown in annotated Figures 2 and 8 of Sugiyama below, Sugiyama’s composite fin structure consists of a combination of the foregoing SiGe layer 30 and strained Si layer 40:



170. As understood from Figures 2 and 8, a POSITA would recognize that the height of the top surface of the composite fin structure (i.e., H_{CFS}) of Sugiyama is equal to the height of the SiGe layer 30 (i.e., H_{SG}) plus the width/thickness of the strained Si layer 40 (i.e., T_{SiL})— $H_{CFS}=H_{SG}+T_{SiL}$. A POSITA would further recognize that the width of the top surface of the composite fin structure (i.e., W_{CFS}) of Sugiyama is equal to the width/thickness of the SiGe layer 30 (i.e., T_{SG}) plus two times the thickness of the strained Si layer 40 (i.e., T_{SiL})— $W_{CFS}=T_{SG}+2*T_{SiL}$.

171. Sugiyama discloses that the “height W” of the SiGe layer 30 may be 50 nm, the “width d”/thickness of the SiGe layer 30 may be from 10-50 nm, which includes as an example, 45 nm, and the thickness of the strained Si layer 40 may be 5 nm. TSMC-1005, 9:30-50. Using Sugiyama’s teachings of these dimensions results in a device in which the height of the sidewalls of Sugiyama’s composite fin structure is substantially equal to the width of the top surface of the composite fin structure— $H_{CFS}=50\text{ nm}+5\text{ nm}=55\text{ nm}$; $W_{CFS}=45\text{ nm}+2*(5\text{ nm})=55\text{ nm}$.

172. In addition applying the endpoints of “height W” of the SiGe layer 30 of 50 nm, the “width d”/thickness of the SiGe layer 30 of 50 nm, and the thickness of the strained Si layer 40 may be 5 nm, results in $H_{CFS}=50\text{ nm}+5\text{ nm}=55\text{ nm}$; $W_{CFS}=50\text{ nm}+2*(5\text{ nm})=60\text{ nm}$, which the POSITA would understand to be approximately equal.

173. Accordingly, a POSITA would recognize that Sugiyama discloses a composite fin structure a height that is approximately equal to the width of its flat top surface, thereby satisfying claim 3.

174. As discussed above for Lee, using equal height and width dimensions for the composite fin structure is not critical nor did it offer any significant change in operation or function to the device. *Supra*, §IX(A)(3). Additionally, it was apparent and obvious to a POSITA at the time that the specific height and width dimensions of the fin structure were at best parameters that could tailored in a known way based on well-known design factors or priorities. Thus, a POSITA knew how and why one might want to change such dimensions of the composite fin structure and would have found it obvious to select equal height and width dimensions when the design factors called for it.

4. Claim 4

[4] The Tri-gate device of claim 1 wherein said strained silicon epitaxy layer has a thickness of about 50-300 angstroms.

175. Sugiyama discloses that its strained silicon epitaxy layer (e.g., “strained Si layer 40”) has a thickness that “is desirably 5 nm (inclusive) to 30 nm (inclusive).” TSMC-1005, 9:49-50; *see also id.*, (“the thickness of the strained Si layer 40 becomes 5 nm”). The thickness of 5-30 nanometers is equivalent to 50-300 angstroms, thus satisfying claim 4.

5. Claim 5

[5] The Tri-gate device of claim 1 wherein said gate strip is made of polysilicon or metal gate.

176. Sugiyama discloses that “gate electrode 80” is made from “polysilicon.” TSMC-1005, 10:9-20 (“***Poly-Si*** is deposited to a thickness of 200 nm on the entire surface of a second insulating layer 24 by CVD, forming a conductive layer 25 as a gate electrode. At this time, phosphorus is heavily doped in the conductive layer 25. Phosphorus may be doped at the same time as poly-Si deposition, or may be ion-implanted after poly-Si deposition. A resist layer (not shown) is patterned on the conductive layer 25, and the conductive layer 25 is etched using the resist layer as a mask. As a result, as shown in FIG. 11A, a band-like gate electrode 80 is formed on the surface of a part of the second insulating layer 70.”) (emph. added). Thus, poly-Si is deposited on the second insulating layer to form conductive layer 25 as a gate electrode, and following patterning of the conductive layer 25, the band-like gate electrode 80 is formed on the second insulating layer 70. TSMC-1005, 10:9-20. The same gate electrode 80 is shown in Figure 2 (for first embodiment) and Figures 9-14 (for second embodiment). *See id.*, 7:64-67 (noting that common reference numbers are used for the same components between the first and second embodiments). A POSITA would understand that the gate electrode 80 disclosed in the first and second embodiments of Sugiyama may be polysilicon.

177. Accordingly, Sugiyama satisfies the limitation of claim 5.

6. Claim 6

6[pre] “Tri-gate Device”

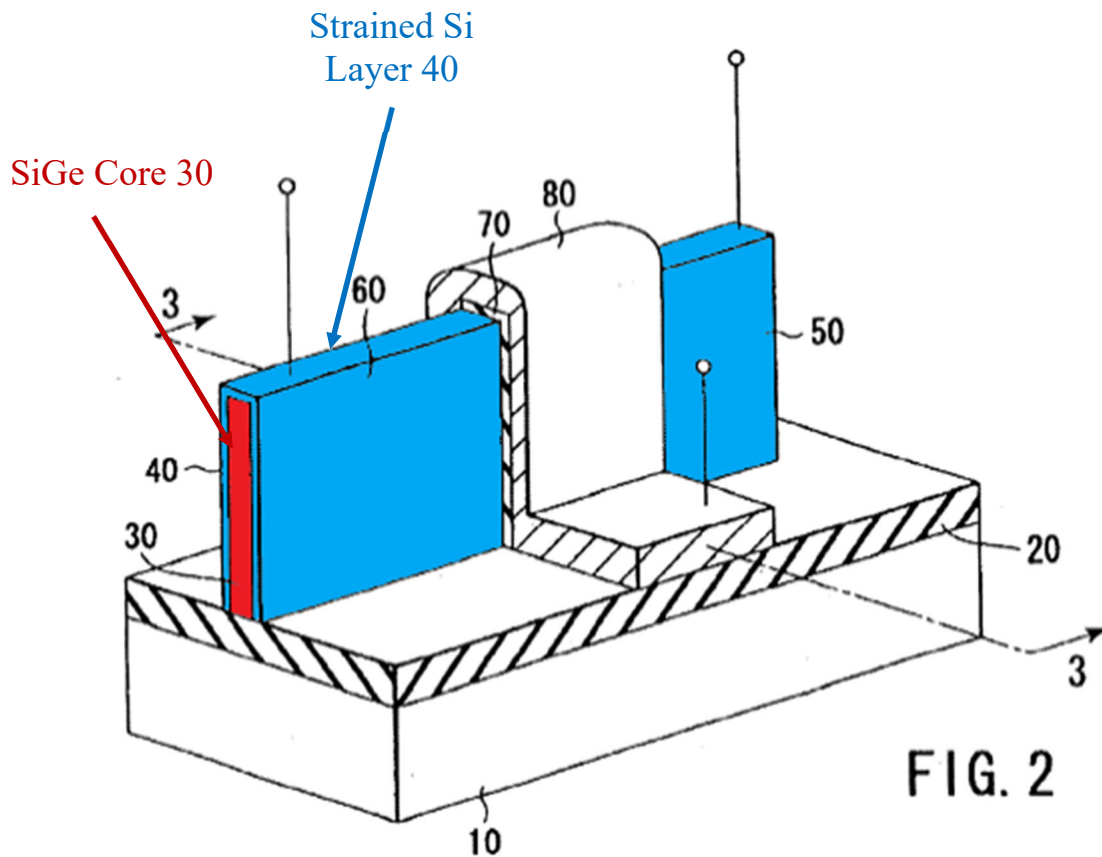
178. Sugiyama discloses a triple gate (Tri-gate) device (e.g., “semiconductor device,” “MISFET”). *See* TSMC-1005, Abstract, 6:63-7:10, 10:4-55, Figs. 2, 3B, 12B-14C; *supra*, §IX(C)(1)(1[pre]). For example, Sugiyama discloses “a MISFET using, as a channel layer, a second semiconductor layer such as a strained Si layer which is joined to a first semiconductor layer such as a SiGe crystal layer formed on an insulating layer, has a lattice constant different from that of the first semiconductor layer, and has a stress strain in crystal lattices.” TSMC-1005, 5:35-42.

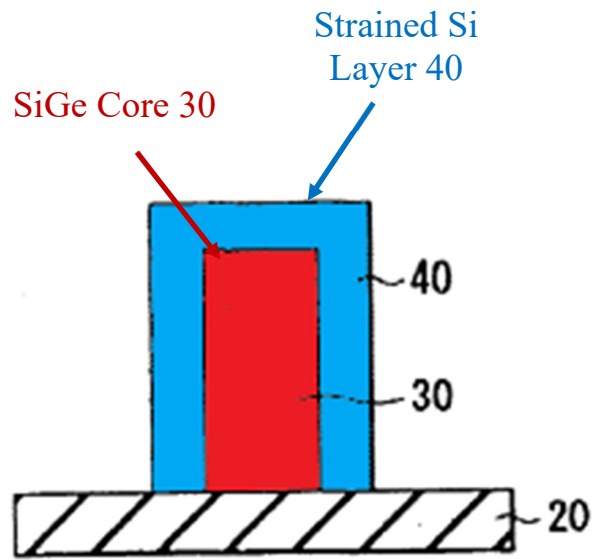
6[a] “Composite Fin Structure”

179. Sugiyama’s MISFET device includes a composite fin structure (e.g., combination of “SiGe layer 30” and “strained Si layer 40”) consisting of: i) a semiconductor core (e.g., “SiGe layer (semiconductor board) 30”); and ii) a strained epitaxy layer (e.g., “strained Si layer (semiconductor layer) 40”) grown from surface of said semiconductor core. *See* TSMC-1005, Abstract, 5:35-42 (“The present invention has been made to solve this problem, relates to a MISFET using, *as a channel layer, a second semiconductor layer such as a strained Si layer which is joined to a first semiconductor layer such as a SiGe crystal layer* formed on an

insulating layer, has a lattice constant different from that of the first semiconductor layer, and has a stress strain in crystal lattices, and also relates to a CMIS circuit which is combined with the MISFET.”) (emph. added); *see also id.*, 5:55-61, 6:63-7:10, Figs. 2, 3B, 8; *supra*, §IX(C)(1)(1[a]).

180. Figures 2 and 8 each depict Sugiyama’s composite fin structure as shown below with annotations highlighting its constituent layers (i.e., silicon germanium semiconductor core 30 in red and strained silicon epitaxy layer 40 in blue):





181. Regarding Figures 2 and 8 (which use common reference numbers for the same components, 7:64-67), Sugiyama describes a “projecting *SiGe layer* (semiconductor board) 30 [that] is formed on the insulating layer 20” and a “*strained Si layer* (semiconductor layer) 40 [that] is formed on the side and upper surfaces of the SiGe layer 30 so as to cover this SiGe layer 30.” TSMC-1005, 6:65-7:3 (emph. added). “Strained Si layer 40” is “grown” on “the surface of the SiGe crystal layer 30 *by epitaxial growth.*” *Id.*, 9:46-47 (emph. added); *see also id.*, 5:18-19 (“a strained Si layer 140 *epitaxially grown* on the upper SiGe crystal layer 130 are formed on a Si substrate 110.”) (emph. added), Figs. 2, 8. Accordingly, a POSITA would recognize that the foregoing strained silicon layer 40 described in Sugiyama is an epitaxy layer grown from the silicon germanium semiconductor core 30.

182. Additionally, Sugiyama's foregoing example semiconductor core (e.g., SiGe layer 30) has a first lattice constant that mis-matches a second lattice constant of Sugiyama's strained epitaxy layer (e.g., strained Si layer 40). See TSMC-1005, 1:33-40 ("More specifically, a MISFET using a semiconductor substrate in which a ***SiGe crystal layer slightly larger in lattice constant than the Si crystal*** is used as an underlayer and a Si thin layer is stacked on the SiGe crystal layer to form a strained Si layer has been proposed. In the MISFET, the carrier exhibits high mobility in the strained Si layer. By using the strained Si layer as a channel region, a high speed and small power consumption can be realized.") (emph. added); 2:14-17 ("a semiconductor layer formed on at least one of the major side surfaces of the semiconductor board, the ***semiconductor layer having a lattice constant different from that of the semiconductor board***") (emph. added), 2:41-48, 4:4-8, 5:35-43, 6:63-7:16, 13:38-42. For example, Sugiyama's disclosed invention are MISFET devices that use "as a channel layer, a second semiconductor layer such as a strained Si layer which is joined to a first semiconductor layer such as a SiGe crystal layer formed on an insulating layer, has a ***lattice constant different*** from that of the first semiconductor layer, and has a stress strain in crystal lattices." TSMC-1005, 5:35-41 (emph. added).

183. Accordingly, a POSITA would recognize that Sugiyama's various MISFET devices each have a composite fin structure consisting of a semiconductor

core and a strained epitaxy layer grown from surface of said semiconductor core, and further that the semiconductor core has a first lattice constant that miss-matches a second lattice constant of the strained epitaxy layer, thereby satisfying this limitation.

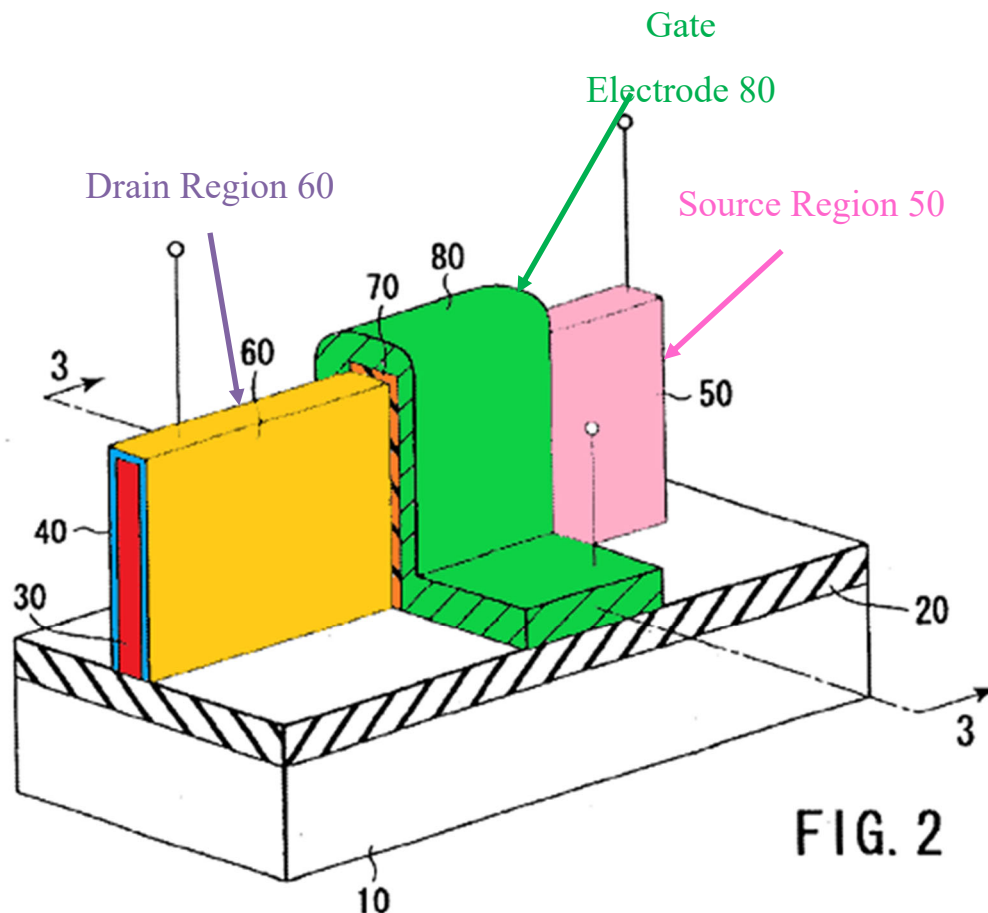
6[b] “Gate Strip”

184. Sugiyama discloses a gate strip, e.g., “gate electrode 80,” wrapping a portion of said composite fin structure. TSMC-1005, 5:44-51 (“In the MISFET, the second semiconductor layer is joined to at least one of the major side surfaces of the first projecting semiconductor layer which is formed on the insulating layer in a board-like shape. In *forming a gate on the second semiconductor layer*, the gate is formed such that the area of a channel portion in the surface of the second semiconductor layer is set smaller than the junction area between the SiGe layer and the insulating layer.”) (emph. added), Figs. 2, 3B; *supra*, §IX(C)(1)(1[b]). For example, Sugiyama states that a “*band-like gate electrode 80* is so formed as to *cover the vertical surfaces and horizontal upper surface* of the strained Si layer 40 via a gate insulating layer 70.” TSMC-1005, 7:8-10 (emph. added).

6[c] “Source/Drain Regions”

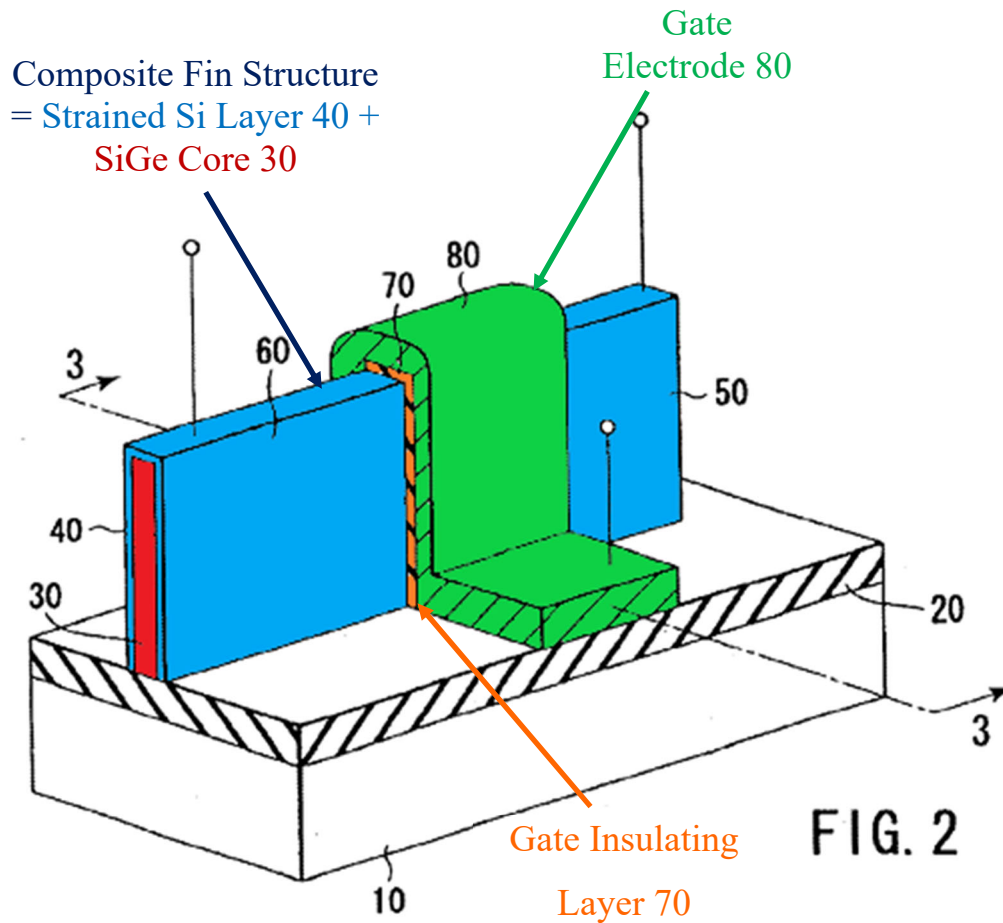
185. Sugiyama discloses that portions of said composite fin structure (e.g., combination of “SiGe layer 30” and “strained Si layer 40”) not covered by said gate strip (e.g., “gate electrode 80”) constitute source/drain regions (e.g., “source region

50,” “drain region 60”) of said Tri-gate device. *See* TSMC-1005, 7:10-17 (“Those portions of the strained Si layer 40 that are not covered with the gate insulating layer 70 and gate electrode 80 serve as a source region 50 and drain region 60 which are activated by heavily doping an impurity. A channel is formed in the strained Si layer 40 covered with the gate electrode 80 between the source region 50 and the drain region 60 such that a current flows parallel to the surface of the insulating layer 20.”) (emph. added), Fig. 2; *supra*, §IX(C)(1)(1[c]).



6[d] “Gate Insulating Layer”

186. Sugiyama discloses a gate insulating layer (e.g., “gate insulating layer 70”) interposed between said composite fin structure (e.g., combination of “SiGe layer 30” and “strained Si layer 40”) and said gate strip (e.g., “gate electrode 80”). TSMC-1005, 7:8-21 (“A band-like gate electrode 80 is so formed as to cover the vertical surfaces and horizontal upper surface of the strained Si layer 40 *via a gate insulating layer 70*. Those portions of the strained Si layer 40 that are not covered with the gate insulating layer 70 and gate electrode 80 serve as a source region 50 and drain region 60 which are activated by heavily doping an impurity. A channel is formed in the strained Si layer 40 covered with the gate electrode 80 between the source region 50 and the drain region 60 such that a current flows parallel to the surface of the insulating layer 20. The gate electrode 80 applies the field effect to the channel via the gate insulating layer 70, and performs three-terminal field effect transistor operation.”) (emph. added), 10:4-45, Figs. 2, 13B-14C; *supra*, §IX(C)(1)(1[d]).



7. Claim 7

[7] The Tri-gate device of claim 6 wherein said semiconductor core consists of silicon germanium.

187. Sugiyama's semiconductor core (e.g., SiGe core 30) consists of silicon germanium. TSMC-1005, Abstract, 5:35-42 ("The present invention has been made to solve this problem, relates to a MISFET using, as a channel layer, a second semiconductor layer such as a strained Si layer which is joined to *a first semiconductor layer such as a SiGe crystal layer* formed on an insulating layer, has

a lattice constant different from that of the first semiconductor layer, and has a stress strain in crystal lattices, and also relates to a CMIS circuit which is combined with the MISFET.) (emph. added), 5:55-61 (“When *the first semiconductor layer is formed from a SiGe crystal layer* and the second semiconductor layer is formed from strained Si, the strained Si layer which covers the surface of the *SiGe* crystal layer functions as a channel. It has been reported that the electron and hole mobilities increase in the strained Si channel, compared to a general Si layer.”) (emph. added), 6:63-7:10, Figs. 2, 3B, 8; *supra*, §IX(C)(1)(1[a]). Figures 2 and 8 depict Sugiyama’s silicon germanium semiconductor core as shown below with annotations in red:

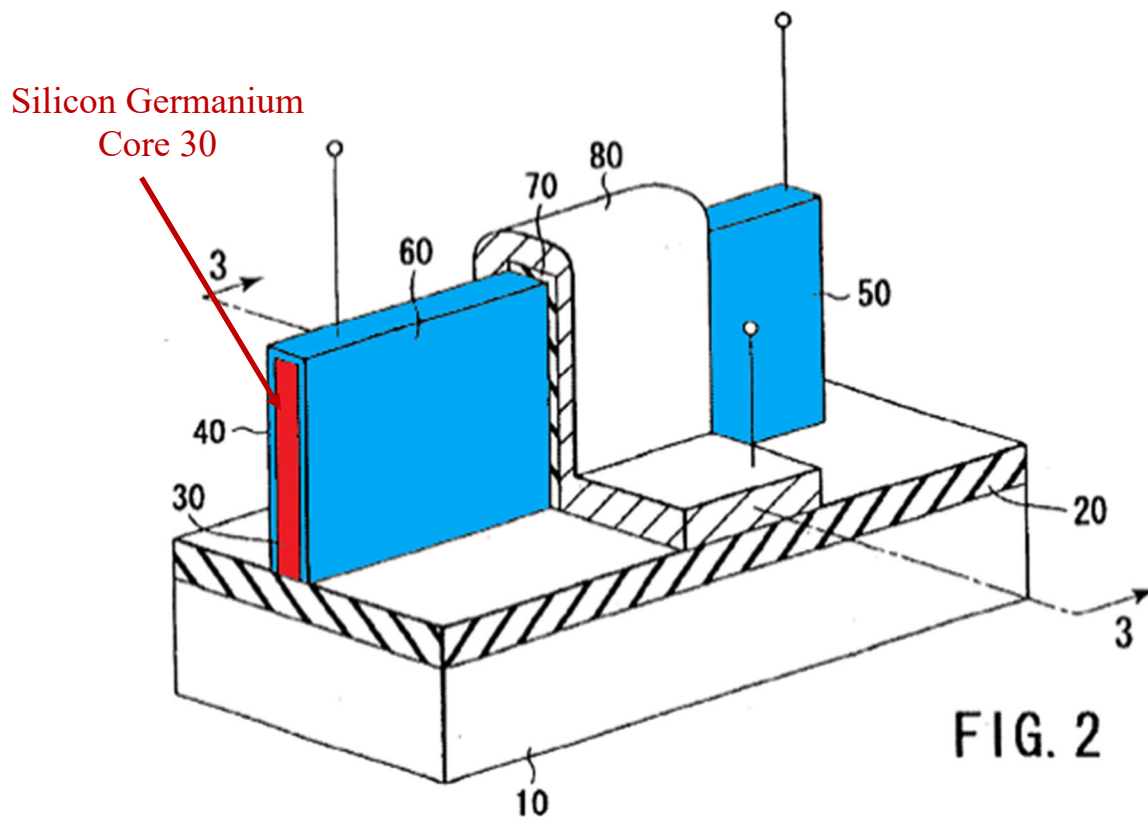
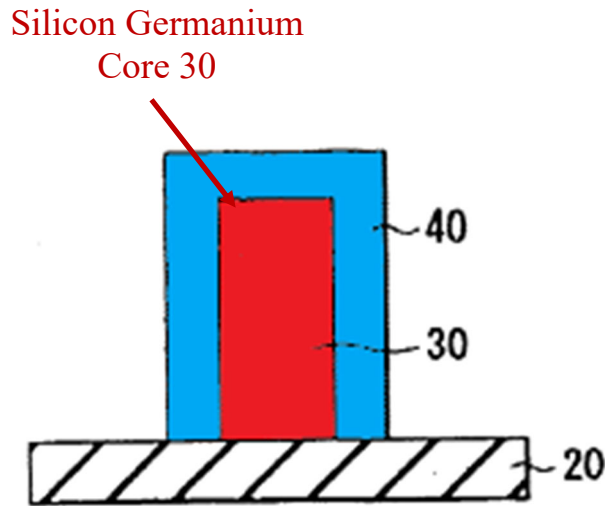


FIG. 2



188. Specifically, regarding Figure 2, Sugiyama describes a “projecting *SiGe layer* (semiconductor board) 30 [that]is formed on the insulating layer 20.” TSMC-1005, 6:65-7:3 (emph. added).

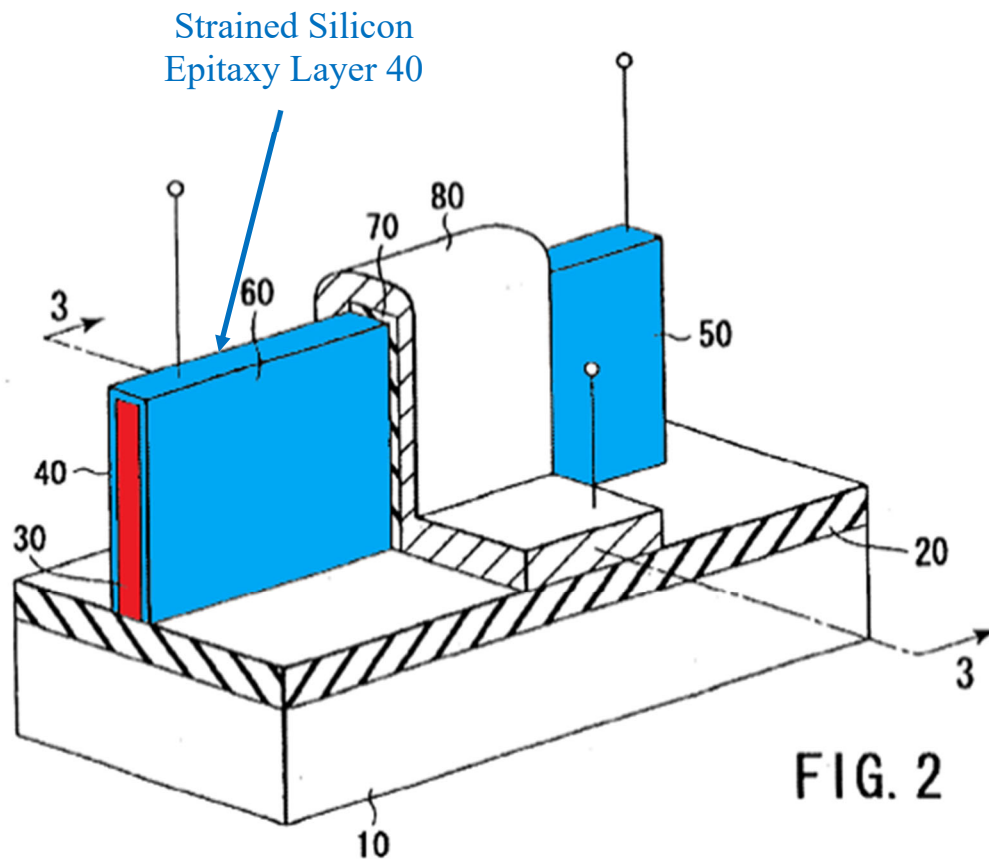
189. Thus, Sugiyama satisfies claim 7.

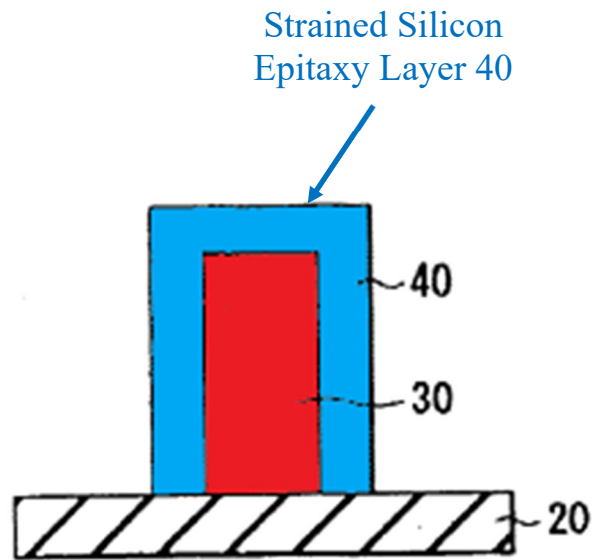
8. Claim 8

[8] The Tri-gate device of claim 6 wherein said strained epitaxy layer is a strained silicon epitaxy layer.

190. Sugiyama’s MISFET device includes a strained silicon epitaxy layer (e.g., “strained Si layer (semiconductor layer) 40”). See TSMC-1005, Abstract, 5:35-42, (“The present invention has been made to solve this problem, relates to a MISFET using, as a channel layer, *a second semiconductor layer such as a strained Si layer which is joined to a first semiconductor layer* such as a SiGe crystal layer formed on an insulating layer, has a lattice constant different from that of the first

semiconductor layer, and has a stress strain in crystal lattices, and also relates to a CMIS circuit which is combined with the MISFET.) (emph. added), 5:55-61 (“When the first semiconductor layer is formed from a SiGe crystal layer and *the second semiconductor layer is formed from strained Si*, the strained Si layer which covers the surface of the SiGe crystal layer functions as a channel. It has been reported that the electron and hole mobilities increase in the strained Si channel, compared to a general Si layer.”) (emph. added), 6:63-7:10, Figs. 2, 3B, 8; *supra*, §IX(C)(1)(1[a]). Figures 2 and 8 depict the strained silicon epitaxy layer (in blue) of Sugiyama’s composite fin structure as shown below with annotations:





191. Specifically, regarding Figure 2, Sugiyama describes a “*strained Si layer* (semiconductor layer) 40 [that] is formed on the side and upper surfaces of the SiGe layer 30 so as to cover this SiGe layer 30.” TSMC-1005, 6:65-7:3 (emph. added). “Strained Si layer 40” is “grown” on “the surface of the SiGe crystal layer 30 *by epitaxial growth*.” *Id.*, 9:46-47 (emph. added); *see also id.*, 5:18-19 (“a strained Si layer 140 *epitaxially grown* on the upper SiGe crystal layer 130 are formed on a Si substrate 110.”) (emph. added), Figs. 2, 8. Accordingly, a POSITA would recognize that the foregoing strained silicon layer 40 described in Sugiyama is a strained silicon epitaxy layer, satisfying claim 8.

9. Claim 9

[9] The Tri-gate device of claim 8 wherein said strained silicon epitaxy layer has a thickness of about 50-300 angstroms.

192. Sugiyama discloses that its strained silicon epitaxy layer (e.g., “strained Si layer 40”) has a thickness that “is desirably 5 nm (inclusive) to 30 nm (inclusive).” TSMC-1005, 9:49-50; *see also id.*, 10:8-9 (“the thickness of the strained Si layer 40 becomes 5 nm”). The thickness of 5-30 nanometers is equivalent to 50-300 angstroms, thus satisfying claim 9.

10. Claim 10

[10] The Tri-gate device of claim 6 wherein said gate strip is made of polysilicon or metal gate.

193. Sugiyama discloses that “gate electrode 80” is made from “polysilicon.” TSMC-1005, 10:9-20 (“**Poly-Si** is deposited to a thickness of 200 nm on the entire surface of a second insulating layer 24 by CVD, forming a conductive layer 25 as a gate electrode. At this time, phosphorus is heavily doped in the conductive layer 25. Phosphorus may be doped at the same time as poly-Si deposition, or may be ion-implanted after poly-Si deposition. A resist layer (not shown) is patterned on the conductive layer 25, and the conductive layer 25 is etched using the resist layer as a mask. As a result, as shown in FIG. 11A, a band-like gate electrode 80 is formed on the surface of a part of the second insulating layer 70.”) (emph. added). Thus, poly-Si is deposited on the second insulating layer to form conductive layer 25 as a gate electrode, and following patterning of the conductive layer 25, the band-like gate electrode 80 is formed on the second insulating layer 70.

TSMC-1005, 10:9-20. The same gate electrode 80 is shown in Figures 2 (for first embodiment) and Figures 9-14 (for second embodiment). *See id.*, 7:64-67 (noting that common reference numbers are used for the same components between the first and second embodiments). A POSITA would understand that the gate electrode 80 disclosed in the first and second embodiments of Sugiyama may be polysilicon.

194. Accordingly, Sugiyama satisfies claim 10

D. Ground 4: Sugiyama in combination with Chau renders Claim 3 unpatentable

1. Claim 3

[3] The Tri-gate device of claim 2 wherein said composite fin structure has a width of said flat top surface that is approximately equal to its height.

195. As described above, Sugiyama discloses that its composite fin structure (e.g., combination of “SiGe layer 30” and “strained Si layer 40”) has a width of said substantially flat top surface that is approximately equal to its height. TSMC-1005, 9:30-50, Fig. 8; *supra*, §IX(C)(3).

196. As further described above, Sugiyama discloses preferred dimension ranges for its SiGe layer 30 as having a “height W” of “50 nm or more” and a “width d” that is “desirably 10 nm (inclusive) to 50 nm (inclusive).” TSMC-1005, 9:30-40 (“In the second embodiment, the width d of the board formed from the SiGe crystal

layer 30 is desirably 10 nm (inclusive) to 50 nm (inclusive) in order to strain a Si crystal layer to be formed in the subsequent step. The depth (in this case, a length in a direction perpendicular to the sheet surface of FIG. 6) of the board formed from the SiGe crystal layer 30 determines the sum of the channel gate length and source/drain electrode length, and falls within the range of 0.5 μ m (inclusive) to 5 μ m (inclusive). A board height W determines the channel gate width, and must be 50 nm or more.”). Sugiyama additionally discloses that its strained Si layer 40 has a thickness that “is desirably 5 nm (inclusive) to 30 nm (inclusive).” *Id.*, 9:49-50.

197. As an additional ground, it was obvious in view of Chau for a POSITA to choose dimensions from these ranges such that Sugiyama’s composite fin structure would have a width of its substantially flat top surface that is approximately equal to its height, as recited in claim 3.

198. As discussed above, Lee expressly discloses a FinFET device that includes a composite fin structure (e.g., “strained silicon fin structure,” “silicon fin channel,” “finFET channel”) that has a width of said substantially flat top surface that is approximately equal to its height, demonstrating the well-known nature of such dimensions. TSMC-1004, 4:33-43 (“The strained silicon fin structure as shown in FIG. 1 can become triple gate device in a finFET structure because the silicon channel covers two sides and top of the seed fin structure. The height H of the seed fin is preferably in the range of 10 nm to 200 nm, and the thickness T of the seed fin

is preferably in the range of 5 nm to 100 nm. The epitaxial silicon layer thickness is preferably in the range of 5 to 15 nm. The optimized dimensions of the disclosed strained silicon fin structure are preferably chosen to ensure fully depleted body under the operation conditions of the finFET device.”), Figs. 1, 14; *supra*, §IX(A)(1).

199. Chau likewise discloses a composite fin structure (e.g., combination of “semiconductor body 520” and “silicon film 560”) that has a width of its substantially flat top surface that is approximately equal to its height, including Figure 6’s graph which includes various plot lines depicting multiple dimension combinations that amount to the claimed approximately equal height and width. TSMC-1007, Figs. 3, 4A, 5G-5H, 6; *supra*, §IX(B)(1).

200. Thus, in addition to Sugiyama disclosing the limitations of claim 3, it was also obvious to a POSITA to incorporate a composite fin structure having approximately equal width and height dimensions into Sugiyama’s tri-gate device in view of the teachings of Chau. Indeed, the same reasons apply to here as above for combining Lee and Chau. *See supra*, IX(B)(1). As discussed above, the specific width and height dimensions of the composite fin structure amount to a simple design choice, the selection of which would be dictated by manufacturing limitations and/or designer preferences regarding the desired performance characteristics of the FinFET device. *Supra*, §§IX(A)(3), IX(B)(1). Because equal height and width dimensions were well-known options (as demonstrated by the foregoing discussions

of both Lee and Chau) and easily achievable given the overlapping height and width dimension ranges expressly contemplated by Lee, Chau, and Sugiyama, when motivated by overall design considerations, it was obvious to a POSITA to select approximately equal height and width dimensions for the resulting composite fin structure when designing and manufacturing the device. *Id.* Additionally, the approximately equal height and width dimensions of the claim composite fin structure are not critical nor do they produce any unexpected results, and the '181 Patent does not provide any indication that they do. *Id.*

201. Moreover, a POSITA would have been motivated to use a composite fin structure having approximately equal width and height dimensions for a number of reasons. For example, a POSITA would have been motivated to select such approximately equal dimensions for the same reasons discussed above, included ensuring full depletion and for easier manufacturing. *Id.* Furthermore, a POSITA would have found implementing approximately equal height and width dimensions for the composite fin structure to be routine and easily achievable (and indeed easier than high aspect ratio double-gate devices as discussed above) at the time of the alleged invention, and thus would have fully expected to succeed when doing so. *Id.*

202. Accordingly, the combination of Sugiyama with Chau renders claim 3 obvious.

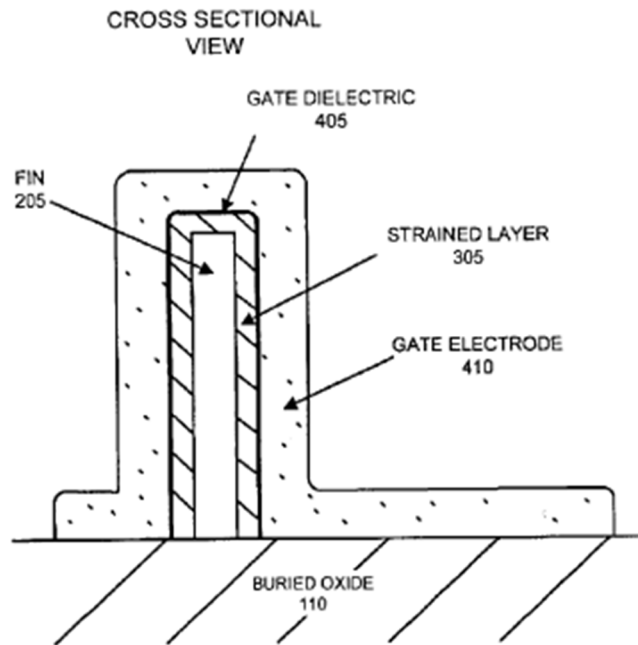
E. Ground 5: Dakshina anticipates Claims 1-2 and 4-10

1. Claim 1

1[pre] “Three Dimensional Triple Gate (Tri-gate) Device”

203. Dakshina discloses a three dimensional triple gate (Tri-gate) device (e.g., “semiconductor structure,” “FinFET”). *See* TSMC-1006, Abstract, 1:5-6 (“The present invention relates generally to transistors and, more particularly, to fin field effect transistors (FinFETs).”), 1:32-41, 2:65-3:7, 4:10-30, Figs. 4A-4B.

204. For example, Dakshina discloses “an increased mobility channel FinFET” that “uses a vertically formed strained channel layer that is self-aligned to [a] fin channel.” TSMC-1006, 2:65-66, 1:31-33. The FinFet includes “gate dielectric 405 and gate electrode 410 upon fin 205, [which] thus, produces a FET sidewall vertical channel that includes a thin strained layer 305 at both vertical surfaces of fin 205.” *Id.*, 4:21-24. Figure 4A depicts an example vertical cross-section of such a FinFET of Dakshina:



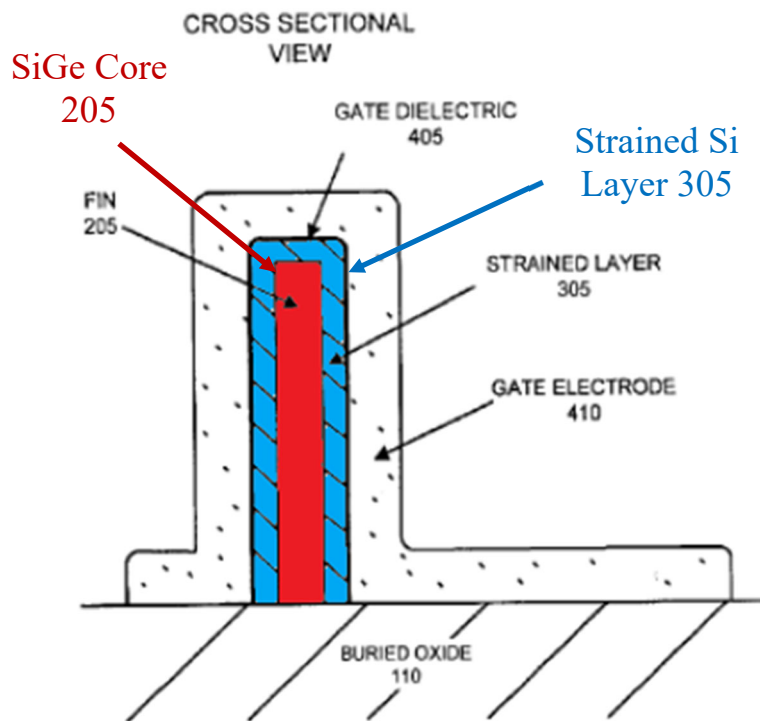
205. A POSITA at the time would have understood this “FinFET” of Dakshina to be a “three dimensional triple gate device” at least because of the presence of the three-dimensional fin 205/strained layer 305 and a gate electrode 410 that covers three surfaces of the fin 205/strained layer 305 (i.e., both vertical side surfaces and the top surface of the fin 205/strained layer 305). *See* TSMC-1006, 3:37-4:24, Figs. 4A-4B; *see also* TSMC-1004, 12:26-30 (“The double gate 103 is actually a triple gate because it covers both sides and the top of the strained silicon channel 104. The term ‘double gate’ in the context of the present invention is a generic term to mean ‘more than one gate’. and therefore covers double or triple gate device.”).

206. Accordingly, a POSITA would understand that it was obvious for the FinFET devices disclosed in Dakshina to include a “three dimensional Triple Gate (Tri-gate) device,” as recited in the preamble of claim 1.

1[a] “Composite Fin Structure”

207. Dakshina’s FinFET device includes a composite fin structure consisting of: (i) a silicon germanium core (e.g., “fin 205”); and (ii) a strained silicon epitaxy layer (e.g., “strained layer 305”) grown from surface of said silicon germanium core. *See* TSMC-1006, Abstract, 3:10-28, 3:38-44, 3:57-4:6, Figs. 1-4B.

208. Figure 4A depicts Dakshina’s composite fin structure as shown below with annotations:



209. Regarding fin 205, Dakshina explains that fin 205 is “formed from fin channel layer 105,” which may include “ $\text{Si}_x\text{Ge}_{(1-x)}$ ” (i.e., silicon germanium) with x approximately equal to 0.7. TSMC-1006, 3:25-28 (“Fin channel layer 105 may include, for example, $\text{Si}_x\text{Ge}_{(1-x)}$ with x approximately equal to 0.7. Other values of x may be appropriately selected.”), 3:39-44 (“Fin 205 may be formed, for example, with a width (w) in a range of 10-15 nm. Fin 205 may be formed from fin channel layer 105 using any existing process, including, but not limited to, existing photolithographic and etching processes.”).

210. Regarding strained layer 305, Dakshina explains that “strained layer 305 may [be] formed on fin 205 ... using a selective *epitaxial* deposition process.” TSMC-1006, 3:59-64 (emph. added). Dakshina further states that “strained layer 305” may include “*silicon*.” *Id.*, 4:5-6 (emph. added).

211. Accordingly, a POSITA would recognize that the foregoing strained layer 305 described in Dakshina is a silicon epitaxy layer grown from the silicon germanium core 205, and these two components together form a composite fin structure and satisfy this limitation.

1[b] “Gate Strip”

212. Dakshina discloses a gate strip (e.g., “gate electrode 410”) wrapping a portion of said composite fin structure. *See* TSMC-1006, 4:10-24, Figs. 4A-4B. For example, Dakshina states that “[a]fter formation of strained layer 305, a gate

dielectric 405 and *gate electrode 410* may be formed *on the portion of fin 205* not covered by source 210 and drain 215.” TSMC-1006, 4:10-13 (emph. added); *see id.*, 4:21-24 (“*Formation of* gate dielectric 405 and *gate electrode 410 upon fin 205*, thus, produces a FET sidewall vertical channel that includes a thin strained layer 305 at both vertical surfaces of fin 205”) (emph. added).

213. Annotated Figures 4A (cross-section view) and 4B (top view) are shown below, depicting Dakshina’s gate electrode 410 (in green) wrapping a portion of the composite fin structure:

Composite Fin Structure
= Strained Layer 305 +
Fin/Core 205

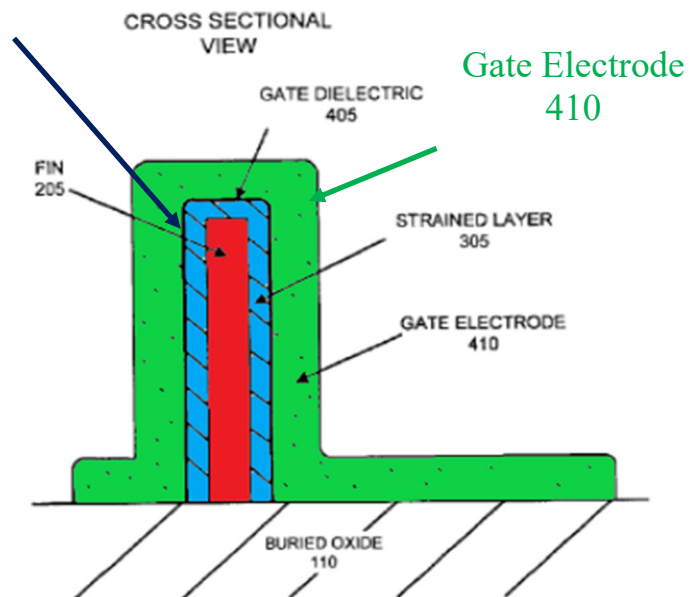
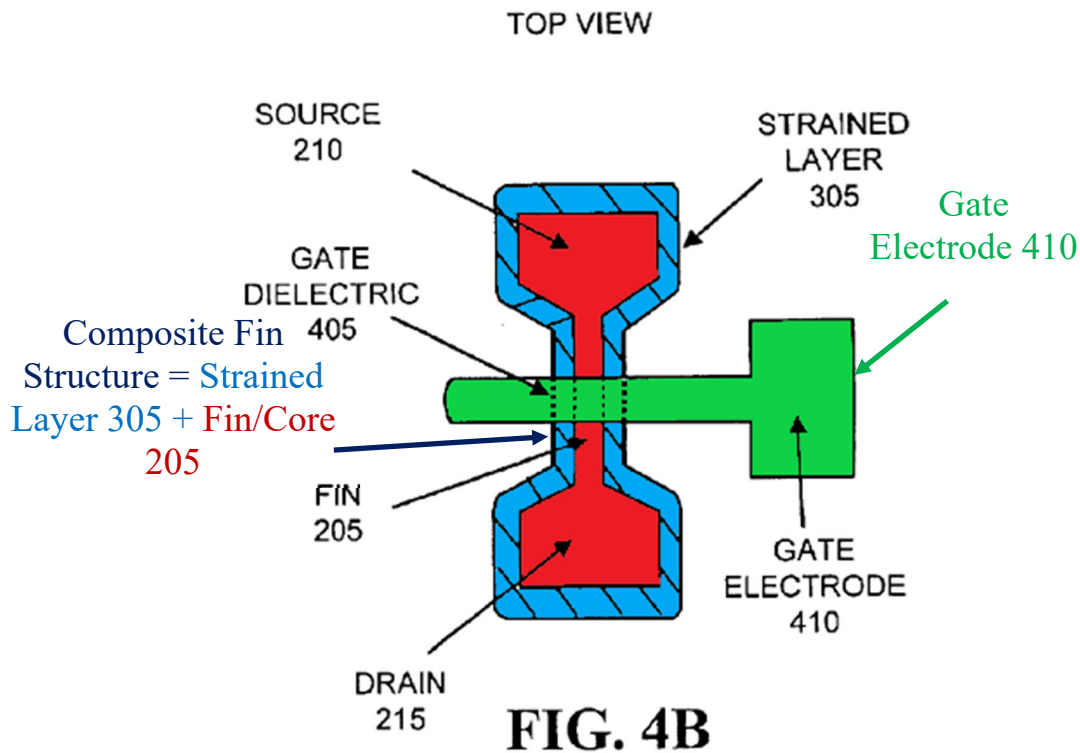


Fig. 4A



214. As seen in Figure 4A, the gate electrode covers both the top and both sides of the composite fin structure. TSMC-1006, 2:44-49 (“FIG. 4A illustrates a cross-sectional view of a gate dielectric and gate electrode formed upon a fin consistent with the invention; FIG. 4B illustrates a top view of the gate dielectric and gate electrode of FIG. 4A formed upon a fin consistent with the invention.”). As seen in Figure 4B, the gate electrode only covers a part of the composite fin structure, traversing the center region of the composite fin structure that is between the source and drain. Dakshina’s explanation matches what Fig. 4B shows, i.e., the gate electrode is formed on the “portion of the fin 205 not covered by source 210 and drain 215.” TSMC-1006, 4:10-13 (“After formation of strained layer 305, a gate

dielectric 405 and gate electrode 410 may be formed on the portion of fin 205 not covered by source 210 and drain 215, as shown in FIGS. 4A and 4B.”).

215. Accordingly, Dakshina’s “gate electrode 410” constitutes a gate strip that wraps a portion of the combined strained silicon layer 305/silicon germanium core 205 (i.e., the “composite fin structure”), satisfying this limitation.

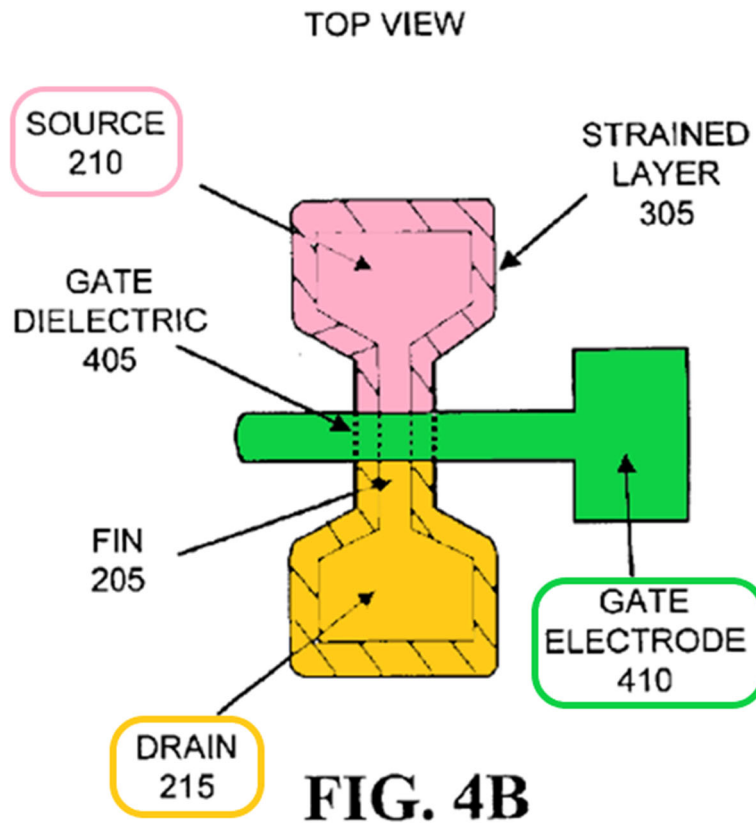
1[c] “Source/Drain Regions”

216. Dakshina discloses that portions of said composite fin structure (e.g., combination of “fin 205” and “strained layer 305”) not covered by said gate strip (e.g., “gate electrode 410”) constitute source/drain regions (e.g., “source 210,” “drain 215”) of said Tri-gate device. *See* TSMC-1006, 3:45-64, 4:10-13, Figs. 2C, 2D, 3B, 4B.

217. For example, Dakshina discloses that “source 210 and drain 215 regions may be formed adjacent the respective ends of fin 205” from the same material (e.g., $\text{Si}_x\text{Ge}_{(1-x)}$) as fin 205. TSMC-1006, 3:45-56 (“Subsequent to formation of fin 205, source 210 and drain 215 regions may be formed adjacent the respective ends of fin 205, as shown in FIGS. 2C and 2D. Source 210 and drain 215 regions may be formed by, for example, deposition of a layer of crystalline material over fin 205. The source 210 and drain 215 regions may be formed from the layer of crystal line material using, for example, existing photolithographic and etching processes. One skilled in the art will recognize, however, that other existing techniques may be used for

forming source 210 and drain 215 regions. Source 210 and drain 215 regions may include a crystalline material such as, for example, $\text{Si}_x\text{Ge}_{(1-x)}$, with x approximately equal to 0.7.”). “Strained layer 305” is then “***formed on fin 205, source 210 and drain 215,***” thereby forming the composite fin structure and included source 210 and drain 215. *See id.*, 3:57-67 (“***After formation of source 210 and drain 215 regions,*** a strained layer 305 may be ***formed on fin 205, source 210 and drain 215,*** as shown in FIGS. 3A and 3B. Strained layer 305 may be formed on fin 205, source 210 and drain 215 using any appropriate existing process. In some exemplary embodiments, for example, strained layer 305 may be formed on fin 205, source 210 and drain 215 using a selective epitaxial deposition process. Strained layer 305 may include a crystalline material whose lattice constant is smaller [than] the lattice constant of the crystalline material used for fin 205.”) (emph. added).

218. Indeed, in describing Figures 4A and 4B, Dakshina states that “[a]fter formation of strained layer 305, a gate dielectric 405 and ***gate electrode 410*** may be formed ***on the portion of fin 205 not covered by source 210 and drain 215.***” TSMC-1006, 4:10-13 (emph. added). Dakshina’s Figure 4B (which depicts the FinFET after formation of the strained layer 35 and gate structure) is reproduced and annotated below depicting the portions of the composite fin structure which are not covered by gate electrode 410, which constitute source 210 (in pink) and drain 215 (in gold):



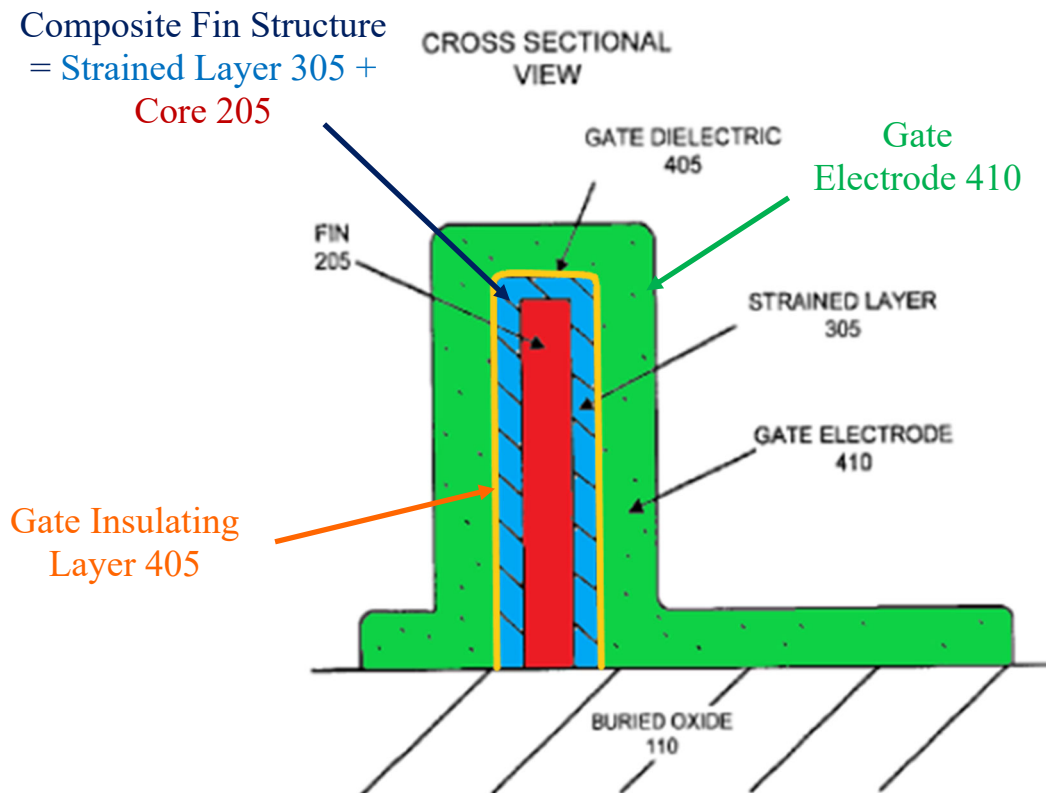
219. Accordingly, the composite fin structures of Dakshina's FinFET devices include portions not covered by gate electrode 410 that constitute source/drain regions 210, 215 of the tri-gate device, thereby satisfying this limitation.

1[d] "Gate Insulating Layer"

220. Dakshina discloses a gate insulating layer (e.g., "gate dielectric 405") interposed between said composite fin structure (e.g., combination of "fin 205" and "strained layer 305") and said gate strip (e.g., "gate electrode 410"). *See* TSMC-1006, 4:10-24, Figs. 4A, 4B. For example, Dakshina states that "[a]fter formation of

strained layer 305, a *gate dielectric 405* and gate electrode 410 may be formed on the portion of fin 205 not covered by source 210 and drain 215.” TSMC-1006, 4:10-12 (emph. added). Gate dielectric 405 includes an “insulating” material such as “SiO, SiO₂, SiN, SiON, HFO₂, ZrO₂, Al₂O₃, HFSiO(x) ZnS, MgF₂, or other dielectric materials.” *Id.*, 4:13-16. And, after discussing formation of gate dielectric 405, Dakshina explains that “[g]ate electrode 410 may be formed upon gate dielectric 405.” *Id.*, 4:16-17.

221. As depicted in annotated Figure 4A below, gate dielectric 405 is interposed between Dakshina’s composite fin structure (i.e., the combination of fin 205 and strained layer 305) and Dakshina’s gate strip (i.e., “gate electrode 410”):



222. Accordingly, Dakshina's gate dielectric 405 constitutes the claimed "gate insulating layer," satisfying this limitation.

223. Dakshina thus discloses all limitations of claim 1.

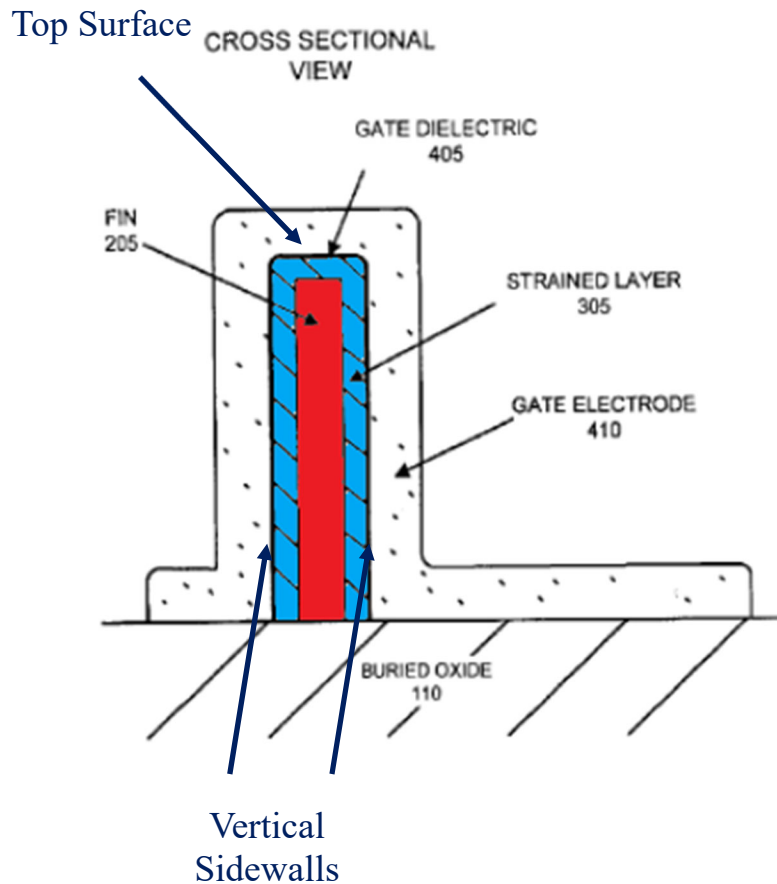
2. Claim 2

[2] The Tri-gate device of claim 1 wherein said composite fin structure has a substantially flat top surface and vertical sidewalls.

224. As depicted in annotated Figure 4A of Dakshina below, Dakshina's composite fin structure (e.g., combination of "fin 205" and "strained layer 305") has a substantially flat top surface and vertical sidewalls. *See* TSMC-1006, 3:37-64, 4:21-30, Figs. 3A, 4A.

225. Dakshina's strained layer 305 (which forms the upper layer of Dakshina's composite fin structure) is formed on three sides of fin 205, including – as shown in the figures – on a top surface and both "vertical surfaces," which a POSITA would understand to correspond to the claimed "substantially flat top surface" and "vertical sidewalls," respectively. *See* TSMC-1006, 4:21-24 ("Formation of gate dielectric 405 and gate electrode 410 upon fin 205, thus, produces a FET sidewall vertical channel that includes a thin strained layer 305 at both vertical surfaces of fin 205."). Thus, an annotated version of Figure 4A of Dakshina is shown below depicting these surfaces of Dakshina's composite fin

structure, where the composite fin structure has a top surface that is substantially flat and has vertical sidewalls:



226. A POSITA would understand that the top surface and sidewalls of Dakshina's composite fin structure are "substantially flat" and "vertical," respectively. Additionally, regardless of "substantially flat" and "vertical" are interpreted, the top surface and sidewalls of Dakshina's composite fin structure are "substantially flat" and "vertical" at least to the same extent as the devices disclosed in the '181 Patent. Accordingly, Dakshina's composite fin structure includes a

“substantially flat top surface” and “vertical sidewalls” as demonstrated above, thereby satisfying claim 2.

3. Claim 4

[4] The Tri-gate device of claim 1 wherein said strained silicon epitaxy layer has a thickness of about 50-300 angstroms.

227. Dakshina discloses that its strained silicon epitaxy layer (e.g., “strained layer 305”) has a thickness that “may be 5 nm.” TSMC-1006, 4:4-5. Dakshina further indicates that the thickness of strained layer 305 “is approximately $\frac{1}{2}$ to $\frac{1}{3}$ of the fin 205 width w” and that fin 205 “may be formed, for example, with a width (w) in a range of 10-15 nm.” TSMC-1006, 4:2-4, 3:40-41. Accordingly, Dakshina discloses different values and ranges of thicknesses for strained layer 305 that includes an example of 5 nm (50 angstroms) along with endpoints of 10nm (100 angstroms) and 15nm (150 angstroms), thus satisfying claim 4.

4. Claim 5

[5] The Tri-gate device of claim 1 wherein said gate strip is made of polysilicon or metal gate.

228. Dakshina discloses that “gate electrode 410” is made of “polysilicon.” See TSMC-1006, 4:16-18, claims 8, 11, 24. For example, Dakshina states that “[g]ate electrode 410 may be formed upon gate dielectric 405 and may include, for example, a ***layer of polysilicon.***” TSMC-1005, 4:16-18 (emph. added); see also *id.*,

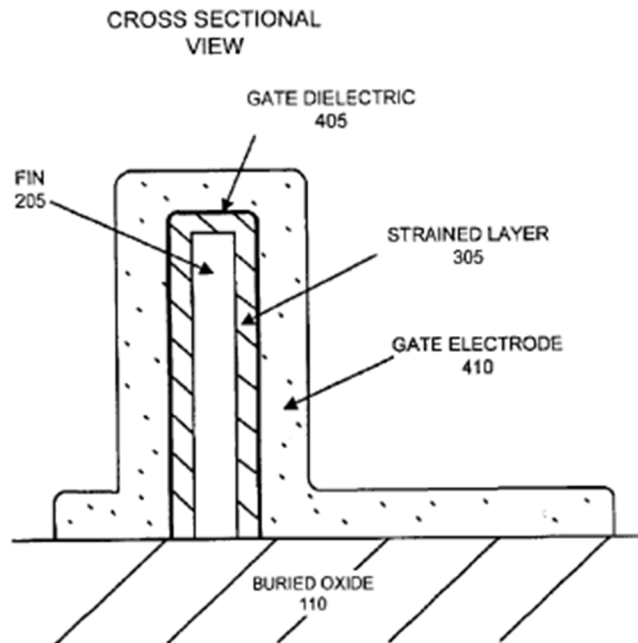
4:54-56 (“Fin 605 may be thinned down and a gate 620 may be formed by depositing and polishing *polysilicon* in gate area 615.”) (emph. added). Accordingly, Dakshina satisfies the limitation of claim 5.

5. Claim 6

6[pre] “Tri-gate Device”

229. Dakshina discloses a three dimensional triple gate (Tri-gate) device (e.g., “semiconductor structure,” “FinFET”). *See* TSMC-1006, Abstract, 1:5-6 (“The present invention relates generally to transistors and, more particularly, to fin field effect transistors (FinFETs).”), 1:32-41, 2:65-3:7, 4:10-30, Figs. 4A-4B; *supra*, §IX(E)(1)(1[pre]).

230. For example, Dakshina discloses “an increased mobility channel FinFET” that “uses a vertically formed strained channel layer that is self-aligned to [a] fin channel.” TSMC-1006, 2:65-66, 1:31-33. The FinFet includes “gate dielectric 405 and gate electrode 410 upon fin 205, [which] thus, produces a FET sidewall vertical channel that includes a thin strained layer 305 at both vertical surfaces of fin 205.” *Id.*, 4:21-24. Figure 4A depicts an example vertical cross-section of such a FinFET of Dakshina:

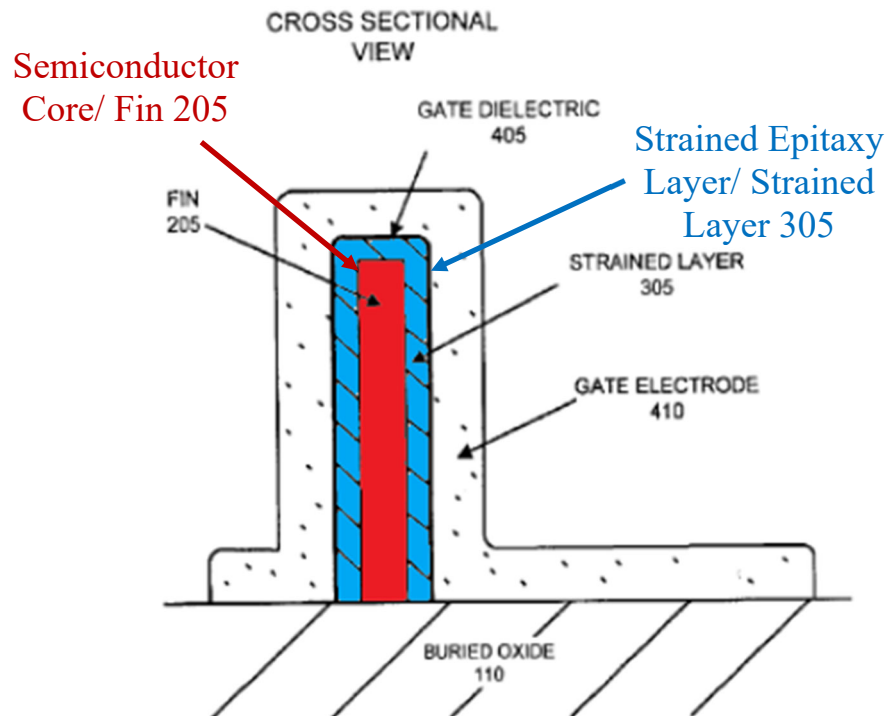


231. A POSITA at the time would have understood this “FinFET” of Dakshina to be a “three dimensional triple gate device” at least because of the presence of the three-dimensional fin 205/strained layer 305 and a gate electrode 410 that covers three surfaces of the fin 205/strained layer 305 (i.e., both vertical side surfaces and the top surface of the fin 205/strained layer 305). *See* TSMC-1006, 3:37-4:24, Figs. 4A-4B; *see also* TSMC-1004, 12:26-30 (“The double gate 103 is actually a triple gate because it covers both sides and the top of the strained silicon channel 104. The term ‘double gate’ in the context of the present invention is a generic term to mean ‘more than one gate’. and therefore covers double or triple gate device.”).

6[a] “Composite Fin Structure”

232. Dakshina's FinFET device includes a composite fin structure consisting of: i) a semiconductor core (e.g., "fin 205"); and ii) a strained epitaxy layer (e.g., "strained layer 305") grown from surface of said semiconductor core. *See* TSMC-1006, Abstract, 3:10-28, 3:38-44, 3:57-4:6, Figs. 1-4AB; *supra*, §IX(E)(1)(1[a]).

233. Figure 4A depicts Dakshina's composite fin structure as shown below with annotations highlighting its constituent layers (i.e., silicon germanium semiconductor core 205 in red and strained silicon epitaxy layer 305 in blue):



234. Regarding core/fin 205, Dakshina explains that fin 205 is "formed from fin channel layer 105," which may include " $\text{Si}_x\text{Ge}_{(1-x)}$ " (i.e., a *semiconductor*) with x approximately equal to 0.7. TSMC-1006, 3:25-28 ("Fin channel layer 105 may

include, for example, $\text{Si}_x\text{Ge}_{(1-x)}$ with x approximately equal to 0.7. Other values of x may be appropriately selected.”), 3:39-44 (“Fin 205 may be formed, for example, with a width (w) in a range of 10-15 nm. Fin 205 may be formed from fin channel layer 105 using any existing process, including, but not limited to, existing photolithographic and etching processes.”).

235. Regarding strained layer 305, Dakshina explains that “strained layer 305 may be formed on fin 205 ... using a selective *epitaxial* deposition process.” TSMC-1006, 3:59-64 (emph. added). Dakshina further states that “strained layer 305” may include “*silicon*.” *Id.*, 4:5-6 (emph. added). Accordingly, a POSITA would recognize that the foregoing strained layer 305 described in Dakshina is a strained epitaxy layer grown from the silicon germanium semiconductor core/fin 205, and these two components together form a composite fin structure and satisfy this limitation.

236. Additionally, Dakshina’s foregoing example semiconductor core (e.g., fin 205) has a first lattice constant that mis-matches a second lattice constant of Dakshina’s strained epitaxy layer (e.g., strained layer 305). *See* TSMC-1006, Abstract, 1:33-40, 1:49-57; 3:1-7, 3:20-36, 4:24-45, 5:29-27, 6:20-26. For example, Dakshina states that “[s]trained layer 305 provides improved carrier mobility through the induction of tensile strain in strained layer 305 caused by the *lattice mismatch between strained layer 305 and fin 205*.” TSMC-1006, 4:24-27 (emph.

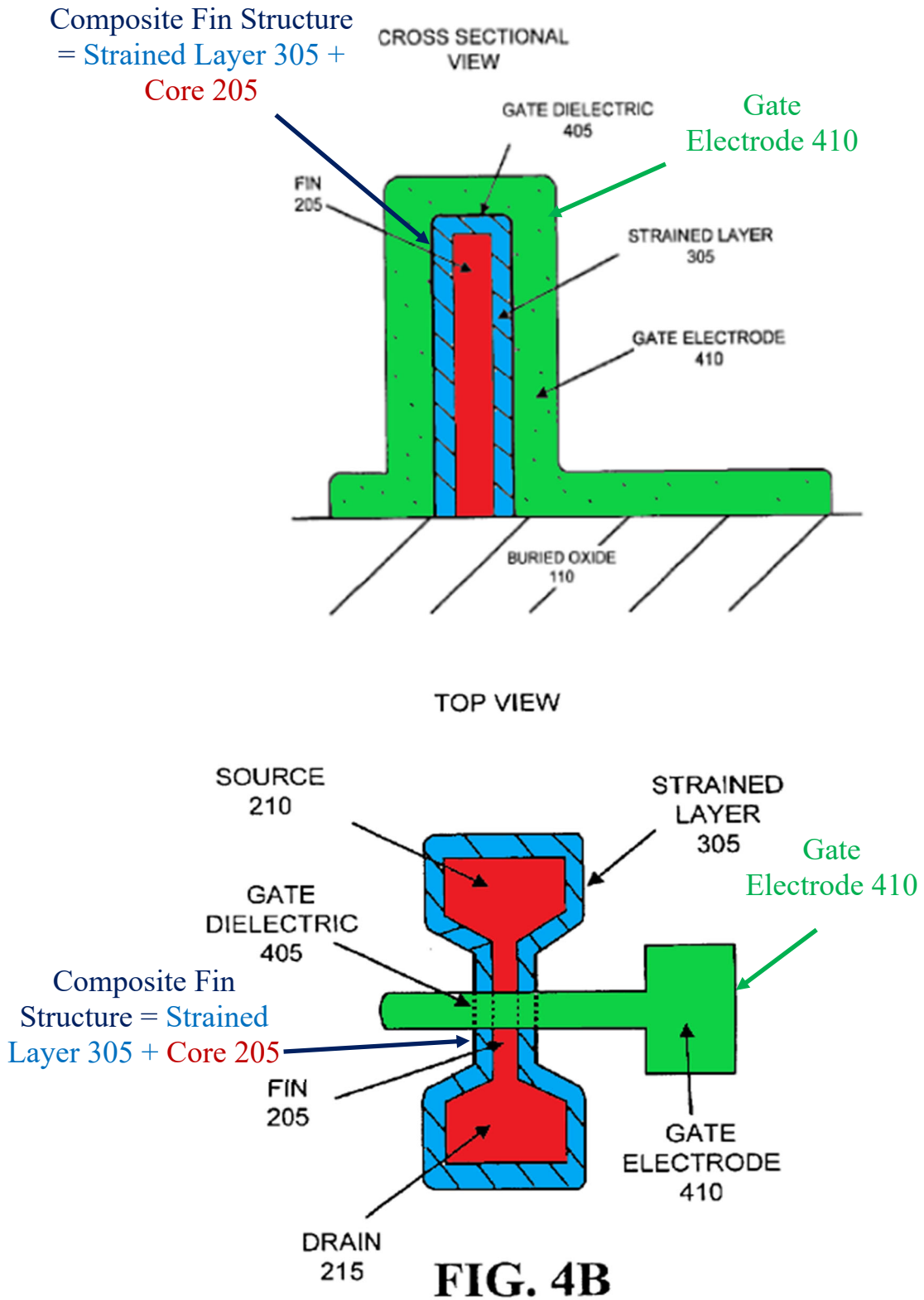
added). Dakshina further describes that the “lattice constant of silicon” (which is used to form “strained layer 305”) is different from (i.e., *mis-matches*) the lattice constant of “Si_xGe_(1-x)” (which is used to form “fin 205”). *See id.*, 3:19-24 (“Fin channel layer 105 may include a crystalline material *with a lattice constant larger than the lattice constant of a crystalline material selected for a strained channel layer* (described with respect to FIGS. 3A and 3B below). If, for example, silicon is selected for the strained channel layer, fin channel layer 105 may include a crystalline material *with a lattice constant large than the lattice constant of silicon.*”) (emph. added); 3:64-4:2 (“Strained layer 305 may include a crystalline material *whose lattice constant is smaller [than] the lattice constant of the crystalline material used for fin 205.* With a *lattice mismatch* between fin 205 and strained layer 305 tensile strain is produced in strained layer 305.”) (emph. added). This lattice constant difference or mis-match induces tensile strain within the strained layer, which enhances carrier mobility and increases the drive current of the resulting FinFET transistor. *See id.*, 4:24-30 (“Strained layer 305 provides *improved carrier mobility through the induction of tensile strain in strained layer 305 caused by the lattice mismatch* between strained layer 305 and fin 205. This carrier mobility enhancement can *increase the drive current* of a FinFET transistor created using the semiconductor structure shown in FIGS. 4A and 4B.”) (emph. added), 1:36-40, 3:1-7, Abstract.

237. Accordingly, a POSITA would recognize that Dakshina's FinFET devices have a composite fin structure consisting of a semiconductor core and a strained epitaxy layer grown from surface of said semiconductor core, and further that the semiconductor core has a first lattice constant that miss-matches a second lattice constant of the strained epitaxy layer, thereby satisfying this limitation.

6[b] "Gate Strip"

238. Dakshina discloses a gate strip (e.g., "gate electrode 410") wrapping a portion of said composite fin structure. *See* TSMC-1006, 4:10-24, Figs. 4A-4B; *supra*, §IX(E)(1)(1[b]). For example, Dakshina states that "[a]fter formation of strained layer 305, a gate dielectric 405 and *gate electrode 410* may be formed *on the portion of fin 205* not covered by source 210 and drain 215." TSMC-1006, 4:10-13 (emph. added); *see id.*, 4:21-24 ("*Formation of* gate dielectric 405 and *gate electrode 410 upon fin 205*, thus, produces a FET sidewall vertical channel that includes a thin strained layer 305 at both vertical surfaces of fin 205") (emph. added).

239. Annotated Figures 4A and 4B are shown below, depicting Dakshina's gate electrode 410 wrapping a portion of the composite fin structure:



240. As seen in Figure 4A, the gate electrode covers both the top and both sides of the composite fin structure. TSMC-1006, 2:44-49 (“FIG. 4A illustrates a cross-sectional view of a gate dielectric and gate electrode formed upon a fin consistent with the invention; FIG. 4B illustrates a top view of the gate dielectric and gate electrode of FIG. 4A formed upon a fin consistent with the invention.”). As seen in Figure 4B, the gate electrode only covers a part of the composite fin structure, traversing the center region of the composite fin structure that is between the source and drain. Dakshina’s explanation matches what Fig. 4B shows, i.e., the gate electrode is formed on the “portion of the fin 205 not covered by source 210 and drain 215.” TSMC-1006, 4:10-13 (“After formation of strained layer 305, a gate dielectric 405 and gate electrode 410 may be formed on the portion of fin 205 not covered by source 210 and drain 215, as shown in FIGS. 4A and 4B.”).

241. Accordingly, Dakshina’s “gate electrode 410” constitutes a gate strip that wraps a portion of the combined strained silicon layer 305/silicon germanium core 205 (i.e., the “composite fin structure”), satisfying this limitation.

6[c] “Source/Drain Regions”

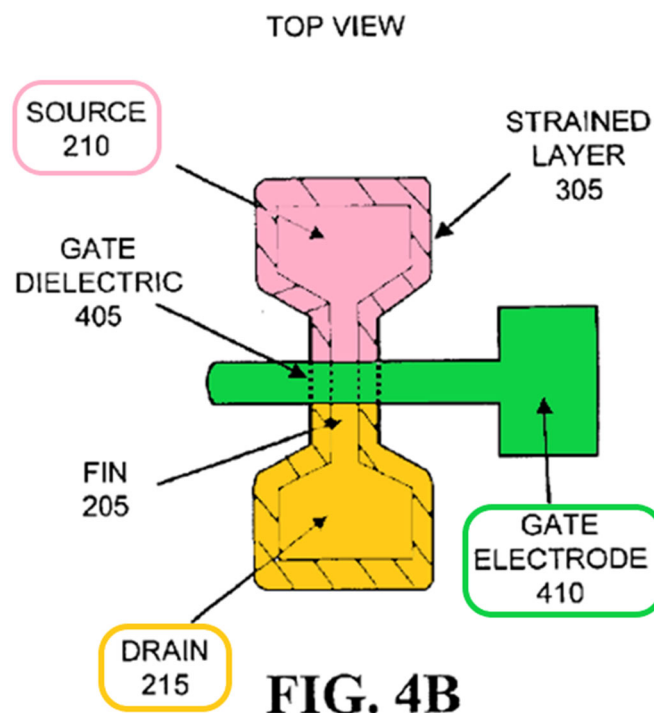
242. Dakshina discloses that portions of said composite fin structure (e.g., combination of “fin 205” and “strained layer 305”) not covered by said gate strip (e.g., “gate electrode 410”) constitute source/drain regions (e.g., “source 210,”

“drain 215”) of said Tri-gate device. *See* TSMC-1006, 3:45-64, 4:10-13, Figs. 2C, 2D, 3B, 4B; *supra*, §IX(E)(1)(1[c]).

243. For example, Dakshina discloses that “source 210 and drain 215 regions may be formed adjacent the respective ends of fin 205” from the same material (e.g., $\text{Si}_x\text{Ge}_{(1-x)}$) as fin 205. TSMC-1006, 3:45-56 (“Subsequent to formation of fin 205, source 210 and drain 215 regions may be formed adjacent the respective ends of fin 205, as shown in FIGS. 2C and 2D. Source 210 and drain 215 regions may be formed by, for example, deposition of a layer of crystalline material over fin 205. The source 210 and drain 215 regions may be formed from the layer of crystal line material using, for example, existing photolithographic and etching processes. One skilled in the art will recognize, however, that other existing techniques may be used for forming source 210 and drain 215 regions. Source 210 and drain 215 regions may include a crystalline material such as, for example, $\text{Si}_x\text{Ge}_{(1-x)}$, with x approximately equal to 0.7.”). “Strained layer 305” is then “***formed on fin 205, source 210 and drain 215,***” thereby forming the composite fin structure and included source 210 and drain 215. *See id.*, 3:57-67 (“***After formation of source 210 and drain 215 regions,*** a strained layer 305 may be ***formed on fin 205, source 210 and drain 215,*** as shown in FIGS. 3A and 3B. Strained layer 305 may be formed on fin 205, source 210 and drain 215 using any appropriate existing process. In some exemplary embodiments, for example, strained layer 305 may be formed on fin 205, source 210 and drain 215

using a selective epitaxial deposition process. Strained layer 305 may include a crystalline material whose lattice constant is smaller [than] the lattice constant of the crystalline material used for fin 205.”) (emph. added).

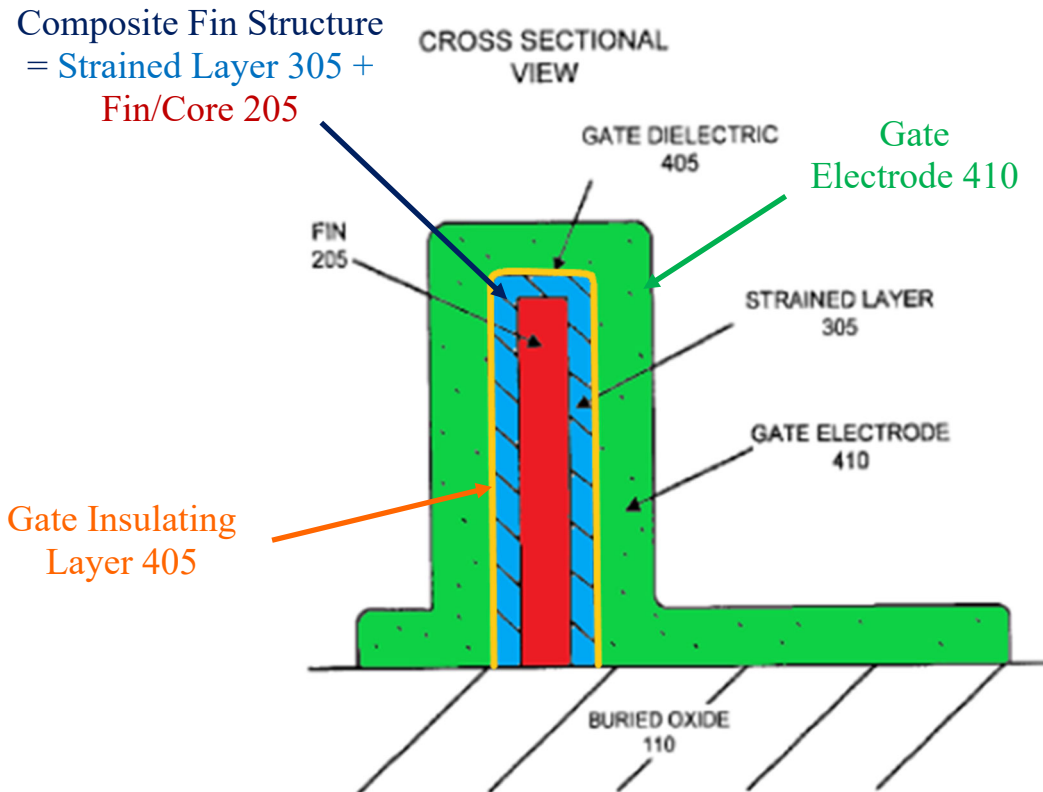
244. Indeed, in describing Figures 4A and 4B, Dakshina states that “[a]fter formation of strained layer 305, a gate dielectric 405 and *gate electrode 410* may be formed *on the portion of fin 205 not covered by source 210 and drain 215.*” TSMC-1006, 4:10-13 (emph. added). Dakshina’s Figure 4B (which depicts the FinFET after formation of the strained layer 35 and gate structure) is reproduced and annotated below depicting the portions of the composite fin structure which are not covered by gate electrode 410, which constitute source 210 (in pink) and drain 215 (in gold):



6[d] “Gate Insulating Layer”

245. Dakshina discloses a gate insulating layer (e.g., “gate dielectric 405”) interposed between said composite fin structure (e.g., combination of “fin 205” and “strained layer 305”) and said gate strip (e.g., “gate electrode 410”). *See* TSMC-1006, 4:10-24, Figs. 4A, 4B; *supra*, §IX(E)(1)(1[d]). For example, Dakshina states that “[a]fter formation of strained layer 305, a **gate dielectric 405** and gate electrode 410 may be formed on the portion of fin 205 not covered by source 210 and drain 215.” TSMC-1006, 4:10-12 (emph. added). Gate dielectric 405 includes an “insulating” material such as “SiO, SiO₂, SiN, SiON, HFO₂, ZrO₂, Al₂O₃, HFSiO(x) ZnS, MgF₂, or other dielectric materials.” *Id.*, 4:13-16. And, after discussing formation of gate dielectric 405, Dakshina explains that “[g]ate electrode 410 may be formed upon gate dielectric 405.” *Id.*, 4:16-17.

246. As depicted in orange in annotated Figure 4A below, gate dielectric 405 is interposed between Dakshina’s composite fin structure (i.e., the combination of fin 205 and strained layer 305) and Dakshina’s gate strip (i.e., “gate electrode 410”):

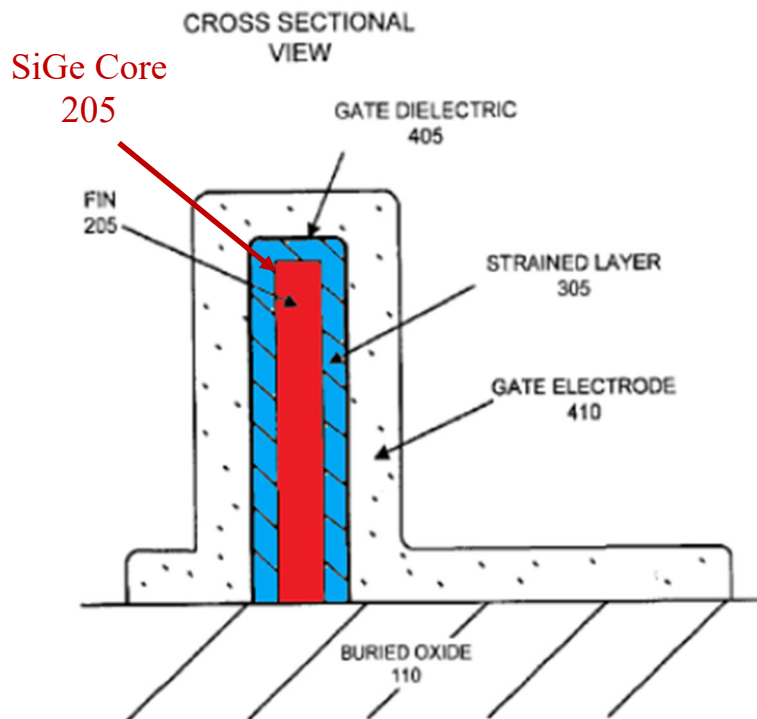


6. Claim 7

[7] The Tri-gate device of claim 6 wherein said semiconductor core consists of silicon germanium.

247. Dakshina's semiconductor core (e.g., "fin 205") consists of silicon germanium (e.g., " $\text{Si}_x\text{Ge}_{(1-x)}$ "). See TSMC-1006, Abstract, 3:10-28, 3:38-44, 3:57-4:6, Figs. 1-4AB; *supra*, §IX(E)(1)(1[a]).

248. Figure 4A depicts Dakshina's silicon germanium semiconductor core as shown below in red:



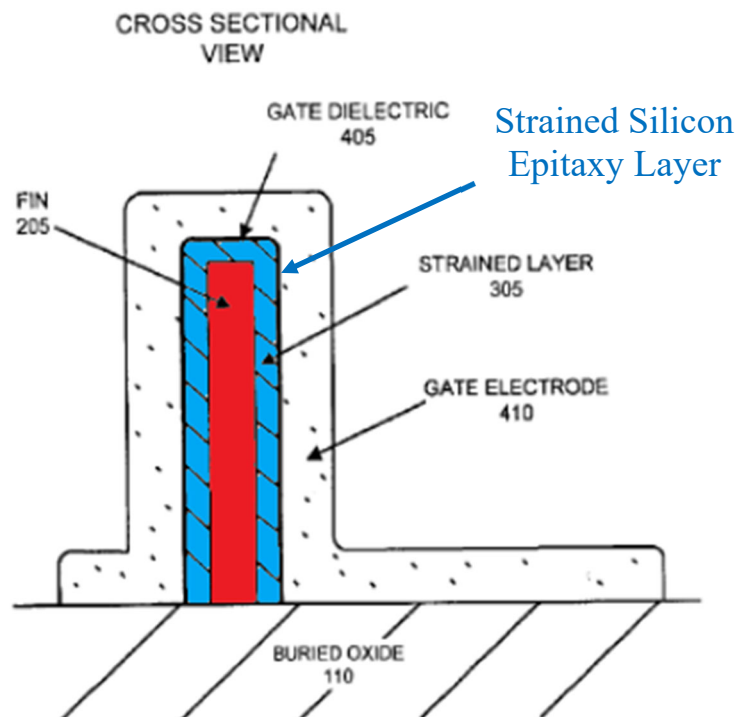
249. Regarding core/fin 205, Dakshina explains that core/fin 205 is “formed from fin channel layer 105,” that may include “ $\text{Si}_x\text{Ge}_{(1-x)}$ ” (i.e., silicon germanium). TSMC-1006, 3:25-28 (“Fin channel layer 105 may include, for example, ***$\text{Si}_x\text{Ge}_{(1-x)}$*** with x approximately equal to 0.7. Other values of x may be appropriately selected.”) (emph. added), 3:39-44. Dakshina does not state that there is any combination of materials for the core/fin 205.

7. Claim 8

[8] The Tri-gate device of claim 6 wherein said strained epitaxy layer is a strained silicon epitaxy layer.

250. Dakshina's FinFET device includes a strained silicon epitaxy layer (e.g., "strained layer 305"). See TSMC-1006, Abstract, 3:10-28, 3:38-44, 3:57-4:6, Figs. 1-4AB; *supra*, §IX(E)(1)(1[a]).

251. Figure 4A depicts the strained silicon epitaxy layer of Dakshina's FinFET device as shown below in blue:



252. Regarding strained layer 305, Dakshina explains that "strained layer 305 may formed on fin 305...using a selective *epitaxial* deposition process." TSMC-1006, 3:59-64 (emph. added). Dakshina further states that "strained layer 305" may include "*silicon.*" *Id.*, 4:5-6 (emph. added). Accordingly, a POSITA would

recognize that the foregoing strained layer 305 described in Dakshina is a strained silicon epitaxy layer, which satisfies this limitation.

8. Claim 9

[9] The Tri-gate device of claim 8 wherein said strained silicon epitaxy layer has a thickness of about 50-300 angstroms.

253. Dakshina discloses that its strained silicon epitaxy layer (e.g., “strained layer 305”) has a thickness that “may be 5 nm.” TSMC-1006, 4:4-5. Dakshina further indicates that the thickness of strained layer 305 “is approximately $\frac{1}{2}$ to $\frac{1}{3}$ of the fin 205 width w” and that fin 205 “may be formed, for example, with a width (w) in a range of 10-15 nm.” *Id.*, 4:2-4, 3:40-41. Accordingly, Dakshina discloses different values and ranges of thicknesses for strained layer 305 that includes an example of 5 nm (50 angstroms) along with endpoints of 10nm (100 angstroms) and 15nm (150 angstroms), thus satisfying claim 9.

9. Claim 10

[10] The Tri-gate device of claim 6 wherein said gate strip is made of polysilicon or metal gate.

254. Dakshina discloses that “gate electrode 410” is made of “polysilicon.” *See* TSMC-1006, 4:16-18, claims 8, 11, 24. For example, Dakshina states that “[g]ate electrode 410 may be formed upon gate dielectric 405 and may include, for example, a **layer of polysilicon.**” TSMC-1006, 4:16-18 (emph. added); *see also id.*,

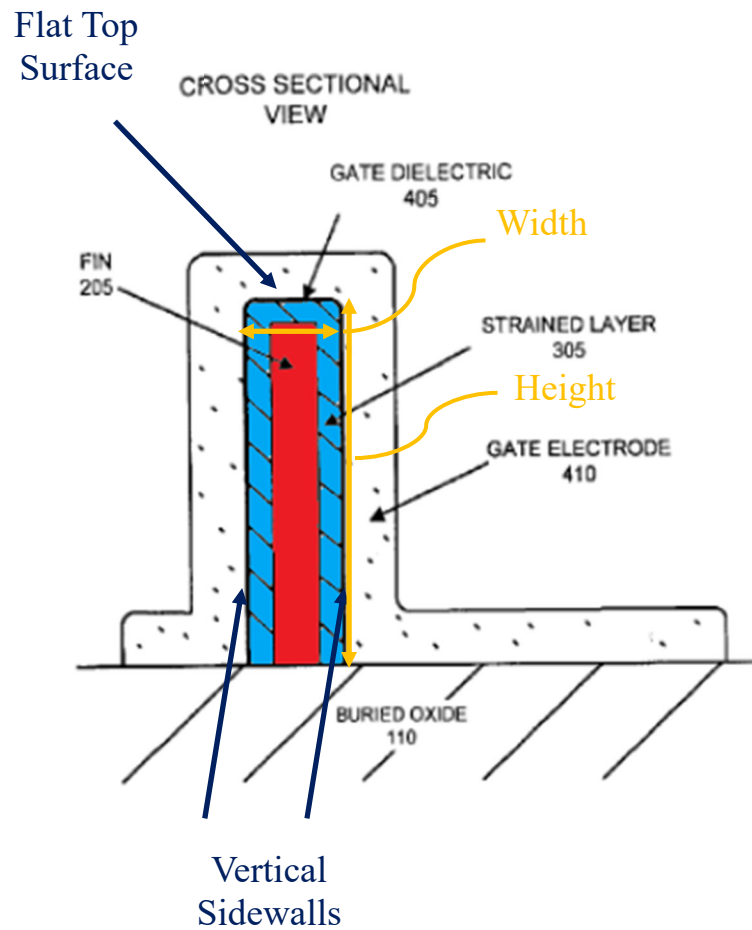
4:54-56 (“Fin 605 may be thinned down and a gate 620 may be formed by depositing and polishing *polysilicon* in gate area 615.”) (emph. added). Accordingly, Dakshina satisfies claim 10.

F. Ground 6: Dakshina in combination with Chau renders Claim 3 unpatentable

1. Claim 3

[3] The Tri-gate device of claim 2 wherein said composite fin structure has a width of said flat top surface that is approximately equal to its height.

255. As described above, Dakshina discloses that its composite fin structure (e.g., combination of “fin 205” and “strained layer 305”) has a substantially flat top surface and vertical sidewalls. *See* TSMC-1006, Abstract, 3:10-28, 3:37-64, 3:57-4:6, 4:21-30, Figs. 1-4AB; *supra*, §IX(E)(2). Annotated Figure 4A of Dakshina is shown below depicting these surfaces of Dakshina’s composite fin structure as well as the corresponding width and height:



256. As discussed above, Lee discloses a composite fin structure (e.g., “strained silicon fin structure,” “silicon fin channel,” “finFET channel”) that has a width of said flat top surface that is approximately equal to its height, demonstrating the well-known nature of such dimensions. TSMC-1004, 4:33-43, Figs. 1, 14; *supra*, §IX(A)(3).

257. Likewise, Chau discloses a composite fin structure (e.g., combination of “semiconductor body 520” and “silicon film 560”) that has a width of its

substantially flat top surface that is approximately equal to its height. TSMC-1007, Figs. 3, 4A, 5G-5H, 6; *supra*, §IX(B)(3).

258. For the same reasons it was obvious to combine Lee with Chau or Sugiyama with Chau, it was obvious in view of Chau for the width of the substantially flat top surface of Dakshina's composite fin structure to be approximately equal to its height. *See supra*, §§IX(A)(3), IX(B)(3), IX(D)(3). As discussed above, the specific width and height dimensions of the composite fin structure amount to a simple design choice, the selection of which would be dictated by manufacturing limitations and/or designer preferences regarding the desired performance characteristics of the FinFET device. *Id.* Because equal height and width dimensions were well-known options (as demonstrated by the foregoing discussions of each of Lee, Chau, and Sugiyama) and easily achievable given the fabrication processes widely used at the time, when motivated by overall considerations, it was obvious to a POSITA to select approximately equal height and width dimensions for the resulting composite fin structure when designing and manufacturing the device. *Id.* Additionally, the approximately equal height and width dimensions of the claim composite fin structure are not critical nor do they produce any unexpected results, and the '181 Patent does not provide any indication that they do. *Id.*

259. Moreover, a POSITA would have been motivated to use a composite fin structure having approximately equal width and height dimensions for a number of reasons. *Id.* For example, a POSITA would have been motivated to select such approximately equal dimensions so that the resulting FET device operates properly when fully depleted, including with excellent short channel performance and optimized sub-threshold gradients. *Id.* Additionally, a POSITA would have been motivated to use a composite fin structure having approximately equal width and height dimensions to simplify device fabrication. *Id.*

260. A POSITA would have found implementing approximately equal height and width dimensions for the composite fin structure to be routine and easily achievable (and indeed easier than high aspect ratio double-gate devices as discussed above) at the time of the alleged invention, and thus would have expected to succeed when doing so. *Id.*

261. Accordingly, the combination of Dakshina with Chau renders claim 3 obvious.

X. CONCLUSION

262. As discussed above, it is my opinion that the Challenged Claims of the '181 Patent are unpatentable because they are anticipated by the prior art, because they would have been obvious to a person of ordinary skill in view of the prior art, or both.

263. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested proceeding before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the proceeding and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

264. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner raises and to account for new information as it becomes available to me.

265. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Declaration of Dr. Paul Braun

Executed on this 6th day of August, 2025, in Champaign, IL.

By: _____

Dr. Paul V. Braun

Appendix A

Exhibit No.	Description
1001	U.S. Patent No. 6,888,181 (“the ’181 Patent”)
1002	Prosecution File History, U.S. Patent No. 6,888,181 (“Prosecution History”)
1003	Declaration of Dr. Paul Braun
1004	U.S. Patent No. 7,045,401 (“Lee”)
1005	U.S. Patent No. 6,774,390 (“Sugiyama”)
1006	U.S. Patent No. 6,803,631 (“Dakshina”)
1007	U.S. Pat. App. Publication No. 2004/0036126 (“Chau”)
1008	U.S. Pat. App. Publication No. 2004/0061178 (“Lin”)
1009	U.S. Pat. App. Publication No. 2005/0017377 (“Joshi”)
1010	Reserved
1011	U.S. Patent No. 6,413,802 to Hu et al. (“Hu”)
1012	B. Doyle et al., Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout, Digest of the 2003 Symposium on VLSI Technology, pp. 133-34 (2003)
1013	B. S. Doyle et al., High Performance Fully-Depleted Tri-Gate CMOS Transistors, IEEE Electron Device Letters, Vol. 24, No. 4, pp. 263-65 (April 2003)
1014	Reserved

1015	S. Wolf et al., Silicon Processing for the VLSI Era Volume 1: Process Technology, 2 nd ed., pp. 225-29 (2000)
1016	U.S. Patent No. 5,461,250 to Burghartz et al. (“Burghartz”)
1017	U.S. Patent No. 6,339,232 to Shinichi Takagi (“Takagi”)
1018	U.S. Patent Application No. 10/227,068, as filed August 23, 2002
1019	T. Vogelsang; K.R. Hofmann, Electron mobilities and high-field drift velocities in strained silicon on silicon-germanium substrates, IEEE Transactions on Electron Devices, Volume: 39, Issue: 11, November 1992
1020	Y. X. Liu et al.; Flexible Threshold Voltage FinFETs with Independent Double Gates and an Ideal Rectangular Cross-Section Si-Fin Channel, IEEE International Electron Devices Meeting 2003, December 8-10, 2003
1021	JainNong Feng et al., BSIMSOI v.2.0 MOSFET Model – User’s Manual for BSIMDD2.0, Electronics Research Laboratory, 1999

Appendix B

Claim Element	Claim Language
1[pre]	A three dimensional Triple Gate (Tri-gate) device comprising:
1[a]	a composite fin structure consisting of a silicon germanium core and a strained silicon epitaxy layer grown from surface of said silicon germanium core;
1[b]	a gate strip wrapping a portion of said composite fin structure,
1[c]	wherein portions of said composite fin structure not covered by said gate strip constitute source/drain regions of said Tri-gate device; and
1[d]	a gate insulating layer interposed between said composite fin structure and said gate strip.
2	The Tri-gate device of claim 1 wherein said composite fin structure has a substantially flat top surface and vertical sidewalls.
3	The Tri-gate device of claim 2 wherein said composite fin structure has a width of said flat top surface that is approximately equal to its height.
4	The Tri-gate device of claim 1 wherein said strained silicon epitaxy layer has a thickness of about 50~300 angstroms.

5	The Tri-gate device of claim 1 wherein said gate strip is made of polysilicon or metal gate.
6[pre]	A Tri-gate device comprising:
6[a]	a composite fin structure consisting of a semiconductor core and a strained epitaxy layer grown from surface of said semiconductor core, said semiconductor core having a first lattice constant that miss-matches a second lattice constant of said strained epitaxy layer;
6[b]	a gate strip wrapping a portion of said composite fin structure,
6[c]	wherein portions of said composite fin structure not covered by said gate strip constitute source/drain regions of said Tri-gate device; and
6[d]	a gate insulating layer interposed between said composite fin structure and said gate strip.
7	The Tri-gate device of claim 6 wherein said semiconductor core consists of silicon germanium.
8	The tri-gate device of claim 6 wherein said strained epitaxy layer is a strained silicon epitaxy layer.

9	The tri-gate device of claim 8 wherein said strained silicon epitaxy layer has thickness of about 50~300 angstroms.
10	The Tri-gate device of claim 6 wherein said gate strip is made of polysilicon or metal gate.

Appendix C

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Professional Appointments

2020-present	<i>Grainger Distinguished Chair in Engineering</i> Department of Materials Science and Engineering University of Illinois Urbana-Champaign
2018-present	<i>Co-Founder and CTO</i> TearDX, Champaign, Illinois
2016-present	<i>Director, Materials Research Laboratory</i> University of Illinois Urbana-Champaign
2012-present	<i>Co-Founder and CTO</i> Xerion Advanced Battery Company, Kettering, Ohio
2011-2020	<i>Ivan Racheff Professor</i> Department of Materials Science and Engineering University of Illinois Urbana-Champaign
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2010-present *Guest Professor*

4th Physics Institute, University of Stuttgart, Germany

2009-2011 *Professor*, Department of Materials Science and Engineering

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2005-2009 *Associate Professor*, Department of Materials Science and Engineering

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1999-2005 *Assistant Professor*, Department of Materials Science and Engineering,

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1998-1999 *Postdoctoral Scientist*, Department of Condensed Matter Physics Research

Advisor: Dr. Pierre Wiltzius

Bell Laboratories. Murray Hill, NJ

1993-1998 *Graduate Research Assistant*, Dept. of Materials Science and Engineering

Advisor: Professor S. I. Stupp

University of Illinois Urbana-Champaign

1991, '92, '93 *Summer Intern*

Martin Marietta/General Electric Company, Moorestown, New Jersey

1991-1993 *Undergraduate Research Assistant*, Dept. of Materials Science & Engineering

Advisor: Professor E. P. Giannelis

Cornell University (except summers)

Additional University of Illinois Urbana-Champaign Appointments

- Beckman Institute for Advanced Science and Technology
- Holonyak Micro and Nanotechnology Laboratory
- Department of Chemical and Biomolecular Engineering
- Department of Mechanical Sciences and Engineering
- Department of Chemistry

Education

Doctor of Philosophy in Materials Science and Engineering, 1998

University of Illinois Urbana-Champaign, Urbana, Illinois

Bachelor of Science in Materials Science and Engineering with Distinction,
1993

Cornell University, Ithaca, New York

Awards and Honors

- Tau Beta Pi Daniel C. Drucker Eminent Faculty Award, Grainger College of Engineering, University of Illinois Urbana-Champaign (2025)
- Grainger Award for Excellence in Translational Research, Grainger College of Engineering, University of Illinois Urbana-Champaign (2024)
- Named on List of Teachers Ranked as Excellent by Their Students (2023, 2022, 2019, 2016, 2015, 2014, 2013, 2012, 2011, 2008, 2005)
- Fellow, National Academy of Inventors (2022)
- Fellow, American Association for the Advancement of Science (2020)
- Fellow of the Materials Research Society (2018)
- Visiting Lecturer Award of the Chemistry Promotion Center, Ministry of Science and Technology, Taiwan (2017)
- Engineering Council Award for Excellence in Advising, College of Engineering, University of Illinois Urbana-Champaign (2012, 2011, 2007, 2006, 2003)

- Young Alumnus Award, Department of Materials Science and Engineering Alumni Board, University of Illinois Urbana-Champaign (2011)
- Selected for Defense Science Study Group, DARPA (2010)
- Friedrich Wilhelm Bessel Research Award, Alexander Humboldt Foundation, Germany (2010)
- Stanley H. Pierce Faculty Award, College of Engineering, University of Illinois Urbana-Champaign (2010)
- Xerox Award for Faculty Research, College of Engineering, University of Illinois Urbana-Champaign (2009)
- Accenture Multi-year Faculty Achievement Award, College of Engineering, University of Illinois Urbana-Champaign (2007)
- University Scholar, University of Illinois Urbana-Champaign (2006)
- Burnett Teaching Award, Department of Materials Science and Engineering, University of Illinois Urbana-Champaign (2005)
- Xerox Award for Faculty Research, College of Engineering, University of Illinois Urbana-Champaign (2004)
- 3M Nontenured Faculty Award, College of Engineering, University of Illinois Urbana-Champaign (2004, 2003, 2002, 2001)
- Willett Faculty Scholar Award, College of Engineering, University of Illinois Urbana-Champaign (2002)
- Robert Lansing Hardy Award, TMS (2002)
- Beckman Young Investigator Fellowship, Arnold and Mabel Beckman Foundation (2001)
- Racheff Assistant Professorship, Department of Materials Science and Engineering, University of Illinois Urbana-Champaign (1999)
- Mavis Memorial Fund Scholarship, College of Engineering, University of Illinois Urbana-Champaign (1997)
- Beckman Institute for Advanced Science and Technology Graduate Research Assistantship (1996, 1995)
- Racheff Award for Outstanding Graduate Research in Materials Science and Engineering, Department of Materials Science and Engineering, University of Illinois Urbana-Champaign (1996)

Editorships and Editorial Boards

- Editorial Advisory Board, *Device* (2023-)
- Editorial Advisory Board, *Electron* (2023-)
- Editorial Advisory Board, *Nano Research Energy* (2022-)

- Editor, *Current Opinion in Solid State and Materials Science* (2019-)
- Editorial Advisory Board, *Frontiers in Energy* (2016-)
- Editorial Advisory Board, *Energy Storage Materials*, (2015-)
- Editorial Advisory Board, *ACS Photonics* (2015-)
- Editorial Advisory Board, *Advanced Optical Materials*, (2012-)
- Editorial Advisory Board, *Current Opinion in Solid State and Materials Science* (2011-2019)
- Editorial Advisor Board, *Chemistry of Materials* (2009-2015)

Professional Affiliations & Leadership Positions

- Director, Materials Research Laboratory, University of Illinois Urbana-Champaign (2016-)
- Committee member, OSA CLEO Nano-Optics and Plasmonics Subcommittee (2013-2014)
- Leader, 3D Micro- and Nanosystems Group, Beckman Institute (2005-2018)
- AAAS (2002-)
- American Physical Society (1999-)
- American Chemical Society (1993-)
- Materials Research Society (1993-)
- Electrochemical Society (various years)
- TMS (various years)

Panels and Advisory Boards

- Academic Program Review Committee, Department of Chemistry, University of California San Diego (2025)
- Academic Program Review Committee, Department of Applied Physical Sciences, University of North Carolina at Chapel Hill (2025)
- Review Panel Chair, CORE Program, Fonds National de la Recherche, Luxembourg (2025)
- Academic Program Review Committee, Department of Materials Science and Engineering, Stanford University (2022)
- Academic Program Review Committee, Geballe Laboratory for Advanced Materials, Stanford University (2022)

- Academic Program Review Committee, Materials Science and Engineering Department, Whiting School of Engineering, Johns Hopkins University (2022)
- Reviewer, Arnold and Mabel Beckman Foundation (2020-2022)
- Panel Lead, DOE BES Basic Research Needs for Transformative Manufacturing (2020)
- Academic Program Review Committee, Materials Science and Engineering at Texas A&M (2019)
- Review Panelist, CORE Program, Fonds National de la Recherche, Luxembourg (2018, 2022-2024)
- Governance Board Member, BP International Center for Advanced Materials (ICAM) (2017–)
- Panel Lead, DOE BES Basic Research Needs for Next-Generation Electrical Energy Storage (2017)
- National Academies Panel on Materials Science and Engineering, Army Research Laboratory (2015-2017)
- Site Review Panelist, Ames Laboratory (2015)
- Advisory Board Member, Department of Physics and Chemistry, University of Stuttgart, Germany (2010)
- Site Review Panelist, Los Alamos National Laboratory (2010)
- Review Panelist, University of Washington NSF STC (2009)
- DOE Workshop Panelist, “Future Science Needs and Opportunities for Electron Scattering” (2007)

Outreach and Development Activities

- MatSE Department Faculty Awards Committee (2016-)
- MatSE Department Faculty Development Committee (2015-2022)
- Special lecturer, Illinois College of Law, *Energy in the 21st Century* (2008, 2009)
- 20th Anniversary Planning Committee, Beckman Institute (2008-2009)
- MatSE Department Diversity Committee (2007-2008)
- National Science Olympiad Campus Steering Committee (2003-2005)
- Presented *Nanomaterials Through the Microscope* to groups of underrepresented first through fifth graders (2002-2003)
- Annually presented *Materials Science Show* for rural high school (2001-2009)
- Lecturer, World Wide Youth in Science and Engineering Program (2000-)

- Faculty Advisor, Engineering Open House (1999-2002, 2015-2016)

Activities Archival Journal Publications (Google Scholar, h-index=100)

<https://scholar.google.com/citations?user=61oXNbsAAAAJ&hl=en>

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23. Paul V. Braun, Runyu Zhang, Jessica A. Krogstad, Jesse P. Angle, Pralav P. Shetty, "Aluminized Metallic Scaffold for High Temperature Applications and Method of Making an Aluminized Metallic Scaffold," Patent No. 10,822,710 issued November 3, 2020.
24. Shailesh N. Joshi, Naoya Take, Paul Braun, Julia Kohanek, Gaurav Singhal, "Methods of Forming Power Electronic Assemblies Using Metal Inverse Opals and Cap Structures," Patent No. 11,069,594 issued July 20, 2021.
25. Lynford L. Goddard, Kimani C. Toussaint, Paul V. Braun, Jinlong Zhu, Daniel Bacon-Brown, Christian H. Ocier, Qing Ding, Corey Richards, "Volumetric Optical Integrated Circuits," Patent No. 11,232,7343 issued February 1, 2022.
26. Shailesh N. Joshi, Paul Braun, Gaurav Singhal, "Methods of Forming a Flat Surface MIO Structure," Patent No. 11,319,639 issued May 3, 2022.
27. Shailesh N. Joshi, Paul Braun, Julia Kohanek, Gaurav Singhal, "Methods of Forming Electronic Assemblies with Textured Surfaces Using Low

- Current Density Electroplating,” Patent No. 11,380,604 issued July 5, 2022.
28. Eugene Orloff, Paul V. Braun, Eleonora Orloff, “Ocular Devices and Methods for the Employment Thereof,” Patent No. 11,395,630 issued July 26, 2022.
 29. Shailesh N. Joshi, Paul V. Braun, Julia Kohanek, Gaurav Singhal, “Systems and Methods of Forming Power Electronic Assemblies with Cooling Channels and Integrated Electrodes,” Patent No. 11,483,951 issued October 25, 2022.
 30. Shailesh N Joshi, Gaurav Singhal, Paul VanNest Braun, Danny J Lohan, Kai-Wei Lan, “Graded Pore Structure Without Phase Mask,” Patent No. 11,726,236 issued August 15, 2023.
 31. Shailesh N. Joshi, Gaurav Singhal, Paul VanNest Braun, Kai-Wei Lan, Nenad Miljkovic, “Electrodeposition compatible anti-reflection coatings for laser interference lithography applications,” Patent No. 11,815,822 issued November 14, 2023.
 32. Shailesh N Joshi, Gaurav Singhal, Paul VanNest Braun, Danny J Lohan, Kai-Wei Lan, “Controlling Porosity of an Interference Lithography Process by Fine Tuning Exposure Time,” Patent No. 11,914,304 issued February 27, 2024.
 33. Shailesh N Joshi, Gaurav Singhal, Paul VanNest Braun, Danny J Lohan, Kai-Wei Lan, “SU-8 Etching Technique Using Molten Salt,” Patent No. 11,920,252 issued March 5, 2024.
 34. Shailesh N Joshi, Dajie Xie, Paul Braun, “Passive thermal management using thermoresponsive hydrogel,” Patent No. 11,999,152 issued June 4, 2024.

Invited Lectures and Seminars

- *Materials Research Society*, Boston, MA, December 2025
- *68th International Conference on Electron, Ion, Photon Beam Technology and Nanofabrication (EIPBN)*, Savannah, GA, May 2025
- *Materials Research Society*, Seattle, WA, April 2025
- *Materials Chemistry Seminar*, University of Wisconsin, Madison, WI, February 2025
- *SPIE Photonics West*, San Francisco, CA, January 2025
- *(plenary) Materials Research Society – Taiwan Annual Meeting*, Taichung, Taiwan, November 2024

- *Materials Science and Engineering Seminar*, Georgia Institute of Technology, Atlanta, GA, October 2024
- *Founders Week Technology Showcase*, University of Illinois, October 2024
- *Grainer Engineering Alumni Webinar*, University of Illinois, October 2024
- *National Academies Sciences Engineering Medicine*, Virtual, September 2024
- *American Chemical Society, Energy Summit*, Denver, CO, August 2024
- *American Chemical Society, Geochemistry & Environmental Chemistry at the Water-Energy Nexus*, Denver, CO, August 2024
- (keynote) *SPIE Active Photonic Platforms*, San Diego, CA, August 2024
- *SPIE Active Photonic Platforms*, San Diego, CA, August 2024 (invited)
- *MATS Symposium and Workshop*, San Diego, CA, July 2024
- *American Chemical Society*, New Orleans, LA, March 2024
- *Partnerships for Research and Education in Materials (PREM)*, Virtual Seminar, February 2024
- *Gordon Research Conference on Batteries*, Ventura, CA, February 2024
- *SPIE Photonics West*, San Francisco, CA, January 2024
- *Materials Science and Engineering Department Colloquium*, Rensselaer Polytechnic Institute, Troy, NY, November 2023
- (keynote) *ACerS MCare and Energy Harvesting 2023 (MCARE)*, Seattle, WA, August 2023
- (keynote) *International Conference on Materials for Advanced Technologies (ICMAT)*, Singapore, June 2023
- *International Conference on Materials for Advanced Technologies (ICMAT)*, Singapore, June 2023 (invited)
- *Department of Energy's Advanced Manufacturing Office Microbattery Design Prize Panelist*, Virtual, May 2023
- *University of Stuttgart*, Stuttgart, Germany, May 2023
- *North Carolina A&T State University*, Virtual Seminar, Greensboro, NC, April 2023
- *Materials Research Society*, San Francisco, CA, April 2023
- *ACS Award in Colloid Chemistry Symposium*, Indianapolis, IN, March 2023
- *Gordon Research Conference on Nanomaterials for Applications in Energy Technology*, Ventura, CA, February 2023
- *National Science Foundation Panelist for Nanotechnology for Clean and Sustainable Energy Storage*, December 2022

- *Co-Design for Materials Discovery, Reliability, and Extreme Environments Workshop*, Hosted by Sandia National Laboratories and Universities Research Association. Virtual, November 2022
- (keynote) *bp-ICAM Annual Conference*, Manchester, England, November 2022
- (keynote) *Advanced Materials Science and Engineering and High Tech Device Applications Conference*, Hybrid event, October 2022.
- *Nature Inspires Creativity Engineers Conference (NICE)*, France, June 2022
- *University of Stuttgart*, Stuttgart, Germany, June 2022
- *241st Electrochemical Society Meeting*, Vancouver, BC, Canada, May 2022
- *Porous Semiconductors - Science and Technology Conference*, Lido di Camaiore, Italy, March 2022
- *TMS Nano-architected Metallic Materials Symposium*, Anaheim, CA, February 2022
- *American Chemical Society*, San Diego, CA, February 2022
- *Chicago Future Manufacturing Seminar*, Chicago, IL February 2022
- *SPIE Photonics West*, San Francisco, CA, January 2022
- *Michigan Materials Research Institute Symposium*, Ann Arbor, MI, November 2021
- (keynote) *Conference on Metamaterials, Photonic Crystals and Plasmonics (META)*, Virtual, July 2021
- *International Conference on Materials for Humanity, Materials Research Society Singapore*, Virtual, July 2021
- *239th ECS Meeting with the 18th International Meeting on Chemical Sensors*, Virtual, May 2021
- *American Chemical Society*, Virtual Meeting, April 2021
- *Argonne National Laboratory*, Virtual Seminar, Lemont, IL, April 2021
- *NanoGe Spring Symposium*, Virtual Meeting, March 2021
- *International Conference on Advances in Catalysis, Energy, and Environmental Research (CACEE-2020)*, Telangana, India, (Virtual) December 2020
- *Materials Research Society*, Virtual Meeting, November 2020
- *Chemical Engineering Seminar*, University of Illinois at Chicago, Chicago, IL, October 2020
- *Materials Science and Engineering Seminar*, University of California, Merced, CA, September 2020
- *NSF Mid-scale Research Infrastructure Engineering Workshop*, Virtual Seminar, August 2020

- *3M*, Virtual Seminar, July 2020
- *BP ICAM*, Virtual Seminar, July 2020
- *Electrochemical Society*, Montreal, Canada, May 2020 (canceled, COVID-19)
- *Materials Research Society*, Phoenix, AZ, April 2020 (canceled, COVID-19)
- *American Chemical Society*, Philadelphia, PA, March 2020 (canceled, COVID-19)
- *Composites at Lake Louise*, Banff, Alberta, Canada, November 2019
- *Seminar, Leuven*, Belgium, November 2019
- *International Institute for Nanotechnology Seminar*, Northwestern University, Evanston, IL, October 2019
- *School of Molecular Sciences Seminar*, Arizona State University, Tempe, AZ, October 2019
- *AVS Symposium*, Columbus, OH, October 2019
- *(plenary), DSEC VI*, Fisicano, Italy, September 2019
- *ACS*, San Diego, CA, August 2019
- *META 2019*, Lisbon, Portugal, July 2019
- *(keynote) ACS Colloids and Surface Science Symposium*, Atlanta, GA, June 2019
- *(keynote) NGRC*, Kyoto, Japan, June 2019
- *PACSUN*, Hawaii, December 2018
- *MRS Fall Meeting*, Boston, MA, November 2018
- *Lithium Battery Materials & Chemistries*, Arlington, VA, November 2018
- *Department of Mechanical Engineering*, Carnegie Mellon, Pittsburgh, PA, November 2018
- *(plenary) YUCOMAT*, Herceg Novi, Serbia, September 2018
- *BASF Committee for Scientific Innovation and Interaction Seminar*, Southland, MI, September 2018
- *(plenary) User Meeting of the Center for Nanophase Materials*, Oak Ridge National Laboratory, Oak Ridge, TN, August 2018
- *ACS*, Boston, MA, August 2018
- *Beyond Lithium-ion XI Meeting*, Cleveland, OH, July 2018
- *MRS Spring Meeting*, Phoenix, AZ, April 2018
- *MRS Spring Meeting*, Phoenix, AZ, April 2018
- *Department of Physics, Illinois State University*, Normal, IL, March 2018
- *IMRE Advanced Surfaces and Dynamic Materials Symposium*, Singapore, February 2018

- *Department of Materials Science and Engineering, Arizona State University, Tempe, AZ, January 2018*
- *Department of Chemistry, New York University, New York, NY, October 2017*
- *TACT, Hua Lien, Taiwan, October 2017*
- *(keynote) WCCE10, Barcelona, Spain, September 2017*
- *ACS, Washington, DC, August 2017*
- *SPIE – Optics and Photonics, San Diego, CA, August 2017*
- *GRC on Nano-Mechanical Interfaces, Hong Kong, China, July 2017*
- *ICMAT 2017, Singapore, June 2017*
- *Department of Chemistry, National Tsing Hua University, Hsin-Chu, Taiwan, May 2017*
- *Department of Chemistry, National Sun Yat-sen University, Kaohsiung, Taiwan, May 2017*
- *Material and Chemical Research Laboratories, ITRI, Hsin-Chu, Taiwan, May 2017*
- *(keynote) TMS 2017, San Diego, CA, February 2017*
- *(keynote) SPIE Photonics West, San Francisco, CA, January 2017*
- *Lecture at Shanghai Jiaotong University, Shanghai, China, January 2017*
- *Workshop on Emerging Science and Technology of Electrochemical Materials and Devices for Alternative Energy, Shanghai, China, January 2017*
- *NICE 2016, Nice, France, October 2016*
- *9th Sino-German Joint Symposium on Opto and Microelectronic Devices and Circuits, Changchun, China, September 2016*
- *SPIE Optics and Photonics, San Diego, CA, August 2016*
- *ECS Meeting, San Diego, CA, June 2016*
- *Washington University seminar, St. Louis, MO, May 2016*
- *DSEC V, Warsaw, Poland, April 2016*
- *Spring MRS Meeting, Phoenix, AZ, March 2016*
- *IMRE Seminar, Singapore, March 2016*
- *IMRE Focused Group Talk, Singapore, March 2016*
- *NUS Seminar, Singapore, March 2016*
- *NTU Seminar, Singapore, March 2016*
- *TTI Vanguard Conference, San Francisco, CA, December 2015*
- *DOE BES Seminar, Gaithersburg, MD, December 2015*
- *University of Illinois, Department of Chemistry Seminar, Urbana, IL, November 2015*
- *MRS Fall Meeting, Boston, MA, November 2015*
- *Nanotechnology for Defense, City of Industry, CA, November 2015*

- *(plenary) Composites at Lake Louise*, Banff, Alberta, Canada, November 2015
- *PlugVolt*, Detroit, MI, October 2015
- *AVS Meeting*, San Jose, CA, October 2015
- *Medtronic Seminar*, Minneapolis, MN, September 2015
- *ACS Meeting*, Boston, MA, August 2015
- *SPIE*, San Diego, CA, August 2015
- *(keynote) 5th Molecular Materials Meeting*, Singapore, August 2015
- *NEES EFRC Seminar*, University of Maryland, July 2015
- *PIERS 2015*, Czech Republic, July 2015
- *CBD S&T Meeting*, St. Louis, MO, May 2015
- *TCO Seminar*, Collegeville, PA, May 2015
- *Next Gen Materials*, San Diego, CA, April 2015
- *(plenary) XIX Argentine Congress of Physical and Inorganic Chemistry*, Buenos Aires, Argentina, April 2015
- *Spring MRS Meeting*, San Francisco, CA, April 2015
- *ACS Meeting*, Denver, CO, March 2015
- *Seminar*, University of Central Florida, Orlando, FL, March 2015
- *TMS 2015*, Orlando, FL, March 2015
- *SPIE*, San Francisco, CA, February 2015
- *IFCO – The Institute of Photonic Sciences*, Barcelona, Spain, February 2015
- *Institute of Materials Science*, Barcelona, Spain, February 2015
- *John van Geuns Lecture*, Amsterdam, Netherlands, December 2014
- *Latin America Optics and Photonics Conference (LAOP)*, Cancun, Mexico, November 2014
- *AVS Meeting*, Baltimore, MD, November 2014
- *Department of Materials Science and Engineering*, Georgia Tech Institute of Technology, Atlanta, GA, November 2014
- *Department of Materials Science and Engineering seminar*, The University of Texas at Austin, Austin, TX, November 2014
- *Department of Chemistry Colloquia*, University of Nebraska, Lincoln, Nebraska, October 2014
- *(Keynote) E-MRS and IUPAC*, Nice, France, October 2014
- *Hybrid & Electric Vehicles Forum*, Prague, September 2014
- *SPIE*, San Diego, CA, August 2014
- *Sustainable Battery Symposium*, Cancun, Mexico, July 2014
- *META 14*, Singapore, May 2014
- *Spring MRS Meeting*, San Francisco, April 2014
- *Brookhaven National Lab*, Upton, NY, April 2014

- *Spring ACS Meeting*, Dallas, TX, March 2014
- *TMS Meeting (two talks)*, San Diego, CA, February 2014
- *38th International Conference & Expo on Advanced Ceramics and Composites (two talks)*, Daytona Beach, FL, January 2014
- *Fall MRS Meeting*, Boston, MA December 2013
- *Composites at Lake Louise*, Banff, Canada, November 2013
- *University of Pennsylvania*, Philadelphia, PA, November 2013
- *ECS Meeting*, San Francisco, CA, October 2013
- *PAT 2013*, Berlin, Germany, September 2013
- *ACS PMSE Symposium*, Indianapolis, IN, September 2013
- *SPIE*, San Diego, CA, August 2013
- *Particles 2013*, Kettering, OH, August 2013
- *Max Planck Institute for Solid State Research*, Stuttgart, Germany, July 2013
- *(plenary) 2013 National Nanotechnology Initiative Stakeholder Workshop*, Washington, DC, June 2013
- *Technische Universität Kaiserslautern*, Germany, June 2013
- *Nanostructures for Electrical Energy Storage, EFRC*, University of Maryland, May 2013
- *MRS Spring Meeting*, San Francisco, CA, April 2013
- *4th International Conference on Metamaterials, Photonic Crystals and Plasmonic*, Sharjah, Sharjah (Dubai), March 2013
- *TMS Meeting*, San Antonio, TX, March 2013
- *Photonics West*, San Francisco, CA, February 2013
- *University of Houston*, Houston, TX, February 2013
- *University of Michigan*, Ann Arbor, MI, January 2013
- *University of Minnesota*, Minneapolis, MN, January 2013
- *MRS Fall Meeting*, Boston, MA, November 2012
- *Nano3D*, Kassel, Germany, October 2012
- *2012 Symposium on Stimuli-Responsive Materials*, Sonoma, CA, October 2012
- *IEEE Photonics*, San Francisco, CA, September 2012
- *TechConnect World 2012, Nanotech*, San Jose, CA, June 2012
- *(Keynote) 2012 ACS Colloid and Surface Science Symposium*, Baltimore, MD, June 2012
- *PECS-X Conference*, Santa Fe, NM, June 2012
- *ESPS-NIS*, Eindhoven, The Netherlands, May 2012
- *MRL Workshop on Programmable Functional Materials*, Urbana, IL, May 2012
- *Materials Research Society, Spring Meeting*, San Francisco, April 2012

- *Nano-EP Seminar*, Urbana, IL, April 2012
- *ARPA-E Workshop*, Washington, DC, March 2012
- *Telluride Workshop*, Telluride, CO, February 2012
- *Hybrid and Electronic Vehicles*, Prague, February 2012
- *Physical Chemistry Seminar*, Urbana, IL, February 2012
- *Schlumberger Doll*, Cambridge, MA, November 2011
- *Alcatel-Lucent*, Naperville, IL, November 2011
- *Materials Research Society Fall Meeting*, Boston, MA, November 2011
- *Composites at Lake Louise*, Banff, Alberta, Canada, October 2011
- *AIChE Annual Meeting*, Minneapolis, MN, October 2011
- *3M*, St. Paul, MN, October 2011
- *Rice University*, Houston, TX, September 2011
- *NAATBatt Annual Meeting*, Louisville, KY, September 2011
- *SPIE Optics and Photonics*, San Diego, CA, August 2011
- *Particles 2011*, Berlin, Germany, July 2011
- *(Keynote) ASME 2011*, Chicago, IL, May 2011
- *nPEAP*, University of Illinois, Urbana, IL, May 2011
- *California Institute of Technology*, Pasadena, CA, February 2011
- *(Keynote) University of Illinois Postdoctoral Research Symposium*, University of Illinois, Urbana, IL, January 2011
- *SPIE Photonics West*, San Francisco, CA, January 2011
- *Advanced Concepts in Semiconductor Materials and Devices for Energy Conversion*, Beltsville, MD, December 2010
- *Materials Research Society Fall Meeting*, Boston, MA, November 2010
- *NU/AIC Symposium*, Northwestern University, Evanston, IL, October 2010
- *VINSE Seminar*, Vanderbilt University, Nashville, TN, October 2010
- *Department of Materials Science*, University of Minnesota, Minneapolis/St. Paul, September 2010
- *KAIST Workshop on Colloids and Interface*, Seoul, Korea, August 2010
- *SPIE Optics and Photonics*, San Diego, CA, August 2010 (*Agustin Mihi*)
- *E-MRS*, Strasbourg, France, June 2010
- *Particles 2010*, Orlando, FL, May 2010 (*Dara Gough*)
- *Korea Institute of Science and Technology*, Seoul, Korea, April 2010
- *Karlsruhe Institute of Technology*, Karlsruhe, Germany, April 2010
- *Instituto de Ciencia de Materiales de Madrid*, Madrid, Spain, April 2010
- *Institute of Materials Science*, Seville, Spain, April 2010
- *American Chemical Society Meeting*, San Francisco, CA, March 2010
- *META '10*, Cairo, Egypt, February 2010
- *Photonics West Meeting*, San Francisco, CA, January 2010

- *Materials Research Society Fall Meeting*, Boston, MA, November 2009
- *Department of Chemistry, University of California at Riverside, Riverside, CA, November 2009*
- *(Plenary) Composites at Lake Louise*, Banff, Alberta, Canada, October 2009
- *Self-Healing Polymer Coatings- II Workshop*, Stuttgart, Germany, October 2009
- *Department of Materials Science and Engineering*, Carnegie Mellon, Pittsburgh, PA, September 2009
- *Naval Research Laboratory*, Washington, DC, September 2009
- *Department of Materials Science and Engineering*, University of Florida, Gainesville, FL, September 2009
- *PCN Colloquium*, Sandia National Laboratory, Albuquerque, NM, September 2009
- *Department of Materials Science and Engineering*, University of Illinois, Urbana, IL, September 2009
- *ICAM*, Rio de Janeiro, Brazil, September 2009
- *Second International Conference on Self-Healing Materials*, Chicago, IL June 2009
- *Department of Chemistry*, Illinois Institute of Technology, Chicago, IL, April 2009
- *Fundamental Aspects of Protection at NACE/RIP*, Atlanta, GA, March 2009
- *American Chemical Society National Meeting*, Salt Lake City, UT, March 2009
- *Department of Materials Science and Engineering*, North Carolina State University, Raleigh, NC, September 2008
- *SPIE Symposium on Active Photonic Crystals, SPIE Optics and Photonics*, San Diego, CA August 2008
- *Organic Thin Films for Photonics Applications Symposium (OTF'08)*, ACS National Meeting, Philadelphia, August 2008
- *International Conference on Optical, Optoelectronic and Photonic Materials and Applications (ICOOPMA2008)*, Edmonton, Canada, July 2008
- *Colloquium Seminar*, Center for Nanoscale Materials, Argonne National Lab, Argonne, IL, June 2008
- *Nanotech08*, Boston, MA, June 2008
- *Particles 2008*, Orlando, FL, May 2008
- *Materials Research Society Spring Meeting*, San Francisco, CA, March 2008

- *Symposium 2008 Nanomaterials --Fabrication, Properties, and Applications*, TMS 2008 Annual Meeting, New Orleans, LA, March 2008
- *17th International Symposium on Applications of Ferroelectrics (ISAF)*, Santa Fe, NM, February 2008
- *Photonic Bandgap Materials and Devices Conference in Optoelectronics, 2008 Photonics West*, San Jose, CA, January 2008
- *Japanese-American Kavli Frontiers of Science Symposium*, Kanagawa, Japan, December 2007
- *Composites at Lake Louise*, Banff, Alberta, Canada, October 2007
- *54th International AVS Symposium and Exhibition*, Seattle, WA, October 2007
- *School of Materials Seminar Series*, Arizona State University, Tempe, AZ, October 2007
- *Seminar at POSTEC*, Pohang, Korea, September 2007
- *Seminar at KAIST*, Daejon, Korea, September 2007
- *Seminar at POSCO*, Gwangyang, Korea, September 2007
- *Functional Materials Seminar at KIST*, Seoul, Korea, September 2007
- *Seminar at SNU*, Seoul, Korea, September 2007
- *SPIE Symposium on NanoScience & Engineering*, San Diego, CA August 2007
- *Particles 2007*, Toronto, Ontario, Canada August 2007
- *Materials Chemistry 8*, University College, London, United Kingdom, July 2007
- *81st Colloid & Surface Science Symposium*, ACS, Newark, DE, June 2007
- *Sandia National Lab*, Albuquerque, NM, June 2007
- *NSF IGERT Seminar Series*, University of New Mexico, Albuquerque, NM, June 2007
- *Technology Accelerator Workshop*, University of Illinois Urbana-Champaign, May 2007
- *German-American Frontiers of Engineering Symposium*, Hamburg, Germany, April 2007.
- *Materials Research Society Spring Meeting*, San Francisco, CA, April 2007
- *International Symposium on Photonic and Electromagnetic Crystal Structures, PECS-VII*, Monterey, California, April 2007
- *Optical Society of America UIUC Chapter Nano-Photonics Seminar*, Champaign-Urbana, Illinois, April 2007
- *West Point Military Academy Photonic Materials Seminar*, March 2007

- Spring 2007 ACS National Meeting, Chicago, March 2007
- Photonic Bandgap Materials and Devices Conference in Optoelectronics, 2007 Photonics West, San Jose, CA, January 2007
- Hitachi Nano-Technology Seminar, Argonne National Laboratory, November 2006
- American Chemical Society National Meeting, San Francisco, CA, September 2006
- SPIE Optics and Photonics 2006, San Diego, CA, August 2006,
- (Keynote) Particles 2006, Orlando, FL May 2006
- German-American Frontiers of Engineering Symposium, Murray Hill, NJ, May 2006
- Materials Research Society Spring Meeting, San Francisco, CA, April 2006
- University of Toronto Seminar, Toronto, Ontario, Canada, April 2006
- Brockhouse Institute for Materials Research Seminar, McMaster University, Hamilton, Ontario, Canada, April 2006
- University of Utah Physical Chemistry Seminar, University of Utah, Salt Lake City, UT, February 2006
- Army Research Lab, Adelphi, Maryland, February 2006
- DOE Solid-State Lighting Workshop, Orlando, FL, February 2006
- SPIE- Photonics West, San Jose, CA, January 2006
- Workshop on Self-Healing Materials, Raleigh, NC, January 2006
- Pacificchem 2005, Honolulu, Hawaii, December 2005
- Materials Research Society Fall Meeting, Boston, MA, December 2005
- NSF Workshop on Emerging Opportunities of Nanoscience to Energy Conversion, Washington, DC, November 2005
- Photonic NanoSystems 2005, San Francisco, CA, November 2005
- Composites at Lake Louise, Lake Louise, Alberta, Canada, November 2005
- SPIE- Optics East, Boston, MA, October 2005
- MRS Three-Dimensional Multifunctional Ceramic Composites Workshop, Urbana, IL October 2005
- Cornell MSE 40th Anniversary, Ithaca, NY, September 2005
- Department of Chemistry, Purdue University, West Lafayette, IN, September 2005
- Microscopy & Microanalysis 2005, Honolulu, HI, August 2005
- Department of Chemistry and Chemical Biology, Stevens Institute of Technology, Hoboken, NJ, July 2005
- 79th ACS Colloid and Surface Science Symposium (2 lectures), Potsdam, NY, June 2005

- Department of Chemistry, University of Pittsburgh, Pittsburgh, April 2005
- Department of Chemical and Biomolecular Engineering, North Carolina State University, Raleigh, NC, April 2005
- Materials Science & Engineering Department, RPI, Troy, NY, March 2005
- American Chemical Society National Meeting (two talks), San Diego, CA, March 2005
- Materials Science & Engineering Department, MIT, Cambridge, MA, February 2005
- CINT Workshop, Albuquerque, NM, January 2005
- 3M, St. Paul, November 2004
- MatSE Department Colloquium, University of Illinois Urbana-Champaign, September 2004
- Beckman Young Investigators, Thirteenth Annual Symposium, Newport Beach, CA, August 2004
- New England International Nanomanufacturing Workshop, Boston, MA, June 2004
- ACS PRF Summer School on Nanoparticle Materials (2 lectures), Ypsilanti, MI, June 2004
- Rock River ACS May Meeting, Rockford, IL, May 2004
- UIUC Careers in Chemistry, Urbana, IL, April 2004
- Particles 2004, Orlando, FL, March 2004
- SPIE- Photonics West, San Jose, CA, January 2004
- Materials Research Society Fall Meeting, Boston, MA, December 2003
- WUN Advanced Materials Seminar Series, Teleconference to 10 Universities in Europe and the USA, October 2003
- OSA Frontiers in Optics, Tucson, AZ, October 2003
- Particles 2003, Toronto, Canada, August 2003
- 3M, St. Paul, April 2003
- 17th Annual CFMR Symposium at Michigan State, East Lansing, MI, March 2003
- Wright Patterson Air Force Base, *Dayton, OH, December 2002*
- The Knowledge Foundation: Photonic Nanostructures 2002, San Diego, CA, October 2002
- Communication and Integration in Nanomaterials, Brasov, Romania, September 2002
- IEEE Nano 2002, Alexandria, VA, August 2002
- Microscopy and Microanalysis 2002, Quebec City, Quebec, Canada, August 2002

- SPIE- International Symposium on Optical Science and Technology, Seattle, WA, July 2002
- American Chemical Society National Meeting, Orlando, FL, April 2002
- American Physical Society March Meeting, Indianapolis, IN, March 2002
- The National Radio Science Meeting, Boulder, CO, January 2002
- The Knowledge Foundation: Photonic Nanostructures, Advancing Materials to Control Light, San Diego, CA, October 2001
- 3M, St. Paul, September 2001
- Gordon Conference on Thin Film and Crystal Growth Mechanisms, Williamston, MA July 2001
- The Knowledge Foundation: NanoStructured Materials 2001, Chicago, IL, June 2001
- Materials Research Society Spring Meeting, San Francisco, CA, April 2001
- Particles 2001, Orlando, FL, February 2001
- (Plenary) NASDA Workshop on Space Utilization, Fine Particles, Nanostructures and Self-Organization, January 2001
- National Space Development Agency of Japan, Tokyo Japan, January 2001
- Materials Research Society Fall Meeting, Boston, MA, December 2000
- NanoMaterials Workshop CNRS-NSF, Montreal, Quebec, Canada, October 2000
- Fifth International Conference on Nanostructured Materials (NANO2000), Sendai, Japan, August 2000
- Dept. of Materials Science and Engineering, City University of Hong Kong, August 2000
- The Knowledge Foundation: Commercialization of Nanostructured Materials, Miami, FL, April 2000
- Swiss-US-Forum on Nanoscience and Nanotechnology, Zürich, Switzerland, September 1999
- Dept. of Materials Science and Engineering, Rensselaer Polytechnic Institute, April 1999
- Nanocomposite Materials: Design and Applications, Girdwood, AK, March 1999
- Princeton Materials Institute, Princeton University, April 1998
- Dept. of Materials Science and Engineering, Cornell University, March 1998
- Dept. of Chemical Engineering, University of Michigan, February 1998
- Dept. of Chemical Engineering, Princeton University, February 1998

- Bell Labs, Lucent Technologies, February 1998
- Dept. of Polymer Science and Engineering, University of Massachusetts Amherst, February 1998
- Dept. of Materials Science and Engineering, University of Illinois, Urbana, IL, January 1998
- Dept. of Materials Science and Engineering, The Pennsylvania State University, January 1998
- DOE Workshop on Microstructural Engineering with Polymers, Alta, UT, August 1997
- Beckman Institute Research Assistantship Seminar, University of Illinois, Urbana, IL, May 1997
- Materials Research Society Spring Meeting, San Francisco, CA, April 1997
- Racheff Award Competition, Dept. of Materials Science and Engineering, University of Illinois, Urbana, IL, May 1996
- Beckman Institute Research Assistantship Seminar, University of Illinois, Urbana, IL, April 1996

Conference Symposia and Sessions Organized

- Symposium Organizer, “Advanced Polymer Surfaces, from Advanced Surface Treatment to Dynamic Surfaces to Paint” *International Conference on Materials for Advanced Technologies (ICMAT)*, Singapore, June 2023
- Meeting Chair, *Materials Research Society Fall Meeting*, Boston, MA, November 2011.
- Local Organizing Committee, *2nd International Conference on Self-Healing Materials*, Chicago, IL, June 2009.
- Symposium Organizer, “Material Systems and Processes for Three-Dimensional Micro- and Nano-Scale Fabrication and Lithography,” *Materials Research Society Spring Meeting*, San Francisco, CA, April 2009.
- Symposium Organizer, “Polymers for Photonics and Optoelectronics,” *237th ACS National Meeting & Exposition*, Salt Lake City, UT, March 2009.
- Symposium Organizer, “Physics of Colloids,” *81st Colloid & Surface Science Symposium, ACS Division of Colloid and Surface Science*, University of Delaware, Newark, Delaware, June 2007.

- Program Committee, *Photonic and Electromagnetic Crystal Structures Meeting (PECS-VII)*, Monterey, California, April 2007.
- Organizing Committee, *German-American Frontiers of Engineering Symposium, National Academy of Engineering and the Alexander von Humboldt Foundation*, Germany, April 2007.
- Symposium Organizer, “Three-dimensional Nano and Microphotonics,” *Materials Research Society Spring Meeting*, San Francisco, CA, April 2007.
- Conference Organizer, “Tuning the Optical Response of Photonic Bandgap Structures III,” *Conference at SPIE 2006 - International Society for Optical Engineering, Optics & Photonics 2006*, San Diego, CA, August 2006.
- Conference Organizer, “Science and Technology of Photonic Bandgap Crystals and Photonic Crystal Fibers for Sensing Applications,” *Conference at SPIE 2005 - International Society for Optical Engineering, Optics East*, Boston, MA, October 2005 (program committee).
- Organizer, “Three-Dimensional Multifunctional Ceramics Composites Workshop,” *MRS Workshop*, Urbana, IL, October 2005.
- Conference Organizer, “Tuning the Optical Response of Photonic Bandgap Structures II,” *Conference at SPIE 2005 - International Society for Optical Engineering, Optics & Photonics 2005*, San Diego, CA, July-August 2005.
- Symposium Organizer, “Mesoscale architectures from nanounits: assembly, fabrication and properties” *Materials Research Society Fall Meeting*, Boston, MA, December 2004.
- Conference Organizer, “Tuning the Optical Response of Photonic Bandgap Structures” *Conference at the 2004 SPIE - International Society for Optical Engineering, International Symposium on Optical Science and Technology*, Denver, CO, August 2004.
- Conference Organizer, “Nanomaterials and Their Optical Applications” *Conference at the 2003 SPIE - International Society for Optical Engineering, International Symposium on Optical Science and Technology*, San Diego, CA, August 2003.

Current Research Group

Ph.D. Candidates

Pushan Bal

Ziyi Che

Yunkyu Choi

Sujan Dewanjee^M

Carlos Juarez-Yescas

Jarom Sederholm

Nikita Duggar^G

Brian (Jr Wen) Lin

Falak Sher

Alexandru Grindeanu

Alex Littlefield^G

Shijie (Jack) Sun

Rosy Huang^C

Jiayu Liu

Baichuan Wang

Bill (Yifei) Huang

Peilin Lu

Fu Wu

Hyewon Jeong

Saeed Moradi

Dajie Xie

Imani Jones

Mayur Prabhudesai^S

Jingyi Zhou

*co-advised with: ^CD. Cahill, ^GL. Goddard, ^MN. Miljkovic, ^SS. Sinha*M.S. Candidates*

Mingyo Jung

Yicheng Jung

Postdocs/Visiting Scientists

Dr. Changyong Park

Dr. Jonathan Turnley

Dr. Thomas Leonard

Dr. Abigail Serrano

Dr. Arghya Patra

Dr. Aliya Mukanova

Undergraduates

Sam Brown

Mary Fowler

Joshua Garcia

Hee Hwang

Zayd Khan

Martin Pouliot

Edrick Wang

Charlie Wu

Graduates, Thesis Title, and First Placement (56 Ph.D. Students, 13 M.S. Students)

- Octavio Cervantes, “*Chemical Characterization of Steel/Polymer Interfaces*,” (M.S., January 2002), Lawrence Livermore National Laboratory
- Timothy Dellinger, “*Bismuth Ceramic Nanocomposites through Ball Milling and Liquid Crystal Synthetic Methods*,” (Ph.D. October 2004), Dow Chemical
- Yun-Ju (Alex) Lee, “*Synthesis and Characterization of Functional Mesostructures Using Colloidal Crystal Templating*,” (Ph.D. May 2005), UT - Dallas
- Carla Heitzman, “*Diffusion of Prodan on Self-Assembled Monolayers and Grafted Polymer Layers*,” (Ph.D. May 2005)
- Wendy Chan, “*Formation of Colloidal Crystals from Nanoparticle Stabilized Colloidal Suspensions*,” (M.S., April 2005), Intel
- Huilin Tu, “*Polymer Brushes for Molecular Transport*,” (Ph.D. December 2005), Schlumberger-Doll Research Center, Boston
- Zhenbin Ge, “*Nanoscale Thermal Transport At Solid-Liquid Interfaces*,” (Ph.D. June 2006), Applied Materials Inc., California
- Stephanie (Pruzinsky) Rinne, “*Two-Photon Polymerization of Defects in Photonic Crystals*,” (Ph.D. October 2006), Owens Corning
- Soo Hyoun Cho, “*Polydimethylsiloxane-Based Self-Healing Composite and Coating Material*,” (Ph.D. February 2007) POSCO, Kwangyang, S. Korea.
- Rachel Evans, “*Transport Of Small Molecules Through Patterned Polymer Brushes*,” (M.S. July 2007) Abbot Labs, Illinois
- Robert Shimmin, “*Evaporation-driven assembly as a route to photonic materials*,” (Ph.D. July 2007) Epic Systems Corp. Madison, Wisconsin
- Margaret Shyr, “*DNA Hybridization and Ligation for Directed Colloidal Assembly*,” (Ph.D. February 2009), Shook, Hardy and Bacon LLP. Kansas City, Missouri.
- Matthew George, (Ph.D. February 2009), MOXTEK
- Ying-Chieh (Christy) Chen, “*Fabrication and Characterization of Three Dimensional Photonic Crystals Generated by Multibeam Interference Lithography*” (Ph.D. June 2009), Intel

- John Busbee, “*Nanoparticle Transport Via Holographic Photopolymerization*” (Ph.D. December 2009), Air Force Research Lab
- Andrew Brzezinski, “*Engineering and Characterizing Light-Matter Interactions in Photonic Crystals*” (Ph.D. December 2009)
- Xindi Yu, “*Functional Nanomaterials Via Colloidal Assisted Fabrication*” (Ph.D. January 2010), Dow Chemical
- Erik Nelson, “*Three-Dimensional Photonic Crystal Optoelectronics*” (Ph.D. September 2010), Harvard
- Abigail Juhl, “*Interference Lithography for Optical Devices and Coatings*” (Ph.D. October 2010), Air Force Research Lab
- Asfand Waqar, “*Click Chemistry for Colloidal Assembly*” (M.S. December 2010)
- Dara Gough, “*Materials with Engineered Mesoporosity for Programmed Mass Transport*” (Ph.D. January 2011), Sandia National Laboratory
- Lindsay Elliott (co-advised w/Paul Bohn, now at Notre Dame) (Ph.D. January 2011)
- Tae Wan Kim, “*The Applications for 3D Inverse Opal Microstructures*” (M.S. May 2011)
- Nihan Yonet-Tanyeri, “*Polymers as Directing Agents for Motions of Chemical and Biological Species*” (Ph.D. June 2011), University of Illinois
- Aaron Jackson, “*Novel Encapsulation Technologies for Small Size-Scale Self-Healing Applications,*” (Ph.D. August 2011), Army Research Lab
- Ian Blitz, “*Thermal Transport in Self-Assembled Nanostructures,*” (M.S. December 2011), kCura
- Austin Pickett, “*Electrospinning Applications in Mechanochemistry and Multi-Functional Hydrogel Materials,*” (M.S. May 2012), Kimberly-Clark
- Jonathan Lange, “*Improving Lithium-Ion Battery Power and Energy Densities Using Novel Cathode Architectures and Materials,*” (M.S. May 2012), Corning
- Sidhartha Gupta, “*Design and Fabrication of Novel and Functional 3D Structures via Proximity Field Nano-Patterning,*” (Ph.D. September 2012), Intel
- Kevin Arpin, “*Three-dimensional metallic architectures for photonic and energy storage applications,*” (Ph.D. November 2012), Xerion
- Corissa Lee, “*Force-Induced Mechanochemical Reactions in Polymeric Systems,*” (Ph.D. May 2013), Exponent
- Ha Seong Kim, “*Fabrication of Three-Dimensional Nanostructures for Thermal Study,*” (M.S. August 2013), UCLA
- Bibek Parajuli, “*Guiding of Plasmons and Phonons in Complex Three Dimensional Structures,*” (Ph.D. August 2013), Intel

- Hailong Ning, *“Three-Dimensional Periodic Structures for Enhancing Light-Matter Interaction and Energy Storage,”* (Ph.D. December 2013), Xerion Advanced Battery Corp.
- Matthew Goodman, *“Unique Templating of and Applications Enabled Through Mesoporous Colloids,”* (Ph.D. July 2014), University of Illinois
- Chunjie Zhang, *“Functionalized Hydrogel Systems for Molecular Sensing and Transport,”* (Ph.D. September 2014), 3M
- Jonathan Streufert, *“Encapsulation of Shock-Sensitive Materials and Their Implementation into Matrices,”* (M.S. May 2015)
- James Pikul (co-advised with W. King) (Ph.D. July 2015), University of Pennsylvania
- Daniel Vissers (co-advised with J. Moore), *“Investigation into key interfacial reactions within lithium-ion batteries,”* (Ph.D. April 2016)
- Neil Krueger, *“Porous Silicon as a Platform for Gradient Refractive Index Photonics,”* (Ph.D. June 2016), Honeywell
- Junjie Wang, *“Improving energy and power densities of three-dimensional next generation secondary battery electrodes,”* (Ph.D. October 2016)
- Xuejiao, Li, *“Autonomic thermal switch based on phase transition alloys,”* (M.S. December 2017)
- Qiye Zheng, *“Functional materials for thermal regulation,”* (Ph.D. October 2017), University of Illinois
- Yavuz Savsatli, *“Visualization of energy transfer among redox active polymeric colloids via in-situ fluorescence microscopy,”* (M.S. May 2018), Xerion Advanced Battery Corp.
- Runyu Zhang, *“Design of multidimensional nanophotonic materials with improved performance and functionalities,”* (Ph.D. April 2018), Apple
- Eric Epstein, *“Towards reversible mechanochemically triggered strengthening, toughening and assembly of soft materials,”* (Ph.D. April 2018), PPG
- Daniel Bacon-Brown, (M.S.), MOXTEK
- Jin Gu Kang, *“Thermal, electrical and mechanical properties of three-dimensional functional materials,”* (Ph.D. September 2018), KIST
- Sanghyeon Kim, *“Investigation of non-intercalation electrode materials for next-generation batteries,”* (Ph.D. October 2018), Argonne National Lab
- Kaitlin Tyler, *“Spatial confinement of metallodielectric eutectic alloys and related outreach curriculum studies,”* (Ph.D. December 2018), Granta Design
- Osman Safa Cifci, *“Spectrum Management for High Efficiency Photonic Devices,”* (Ph.D. November 2018), TAI USA Inc.

- Jungwoo Shin, “*Thermal conductivity switching of polymers and Li-ion battery electrode materials in response to external stimuli*,” (Ph.D. November 2018), Google
- Kewang Nan, “*A Mechanically-Guided Approach to Three-Dimensional Functional Mesostructures Towards Unconventional Applications*,” (Ph.D. November 2018), Harvard
- Julia Kohanek, “*Solidification of Eutectics Utilizing Directional Solidification and Confining Templates for Optical Metamaterial Applications*,” (Ph.D. April 2019), University of Arkansas
- Shuqi Lai “*Chemical amplification in self-stiffening materials*,” (Ph.D. April 2019), Intel
- Kali Miller “*Synthesis and Kinetic Processes in Designed Polymers*,” (Ph.D. May 2019), American Chemical Society
- Shiyang Zhang, “*Functional gels for directed molecular transport and sensor applications*,” (Ph.D. October 2019)
- Ashish Kulkarni “*Controlling the Emergent Microstructures in Template-directed Eutectic Solidification for Optical Applications*,” (Ph.D. May 2020), Veeco Instruments
- Subing (Alan) Qu “*Direct Visualization of Electron Transport among Nonconjugated Polymeric Redox-Active Colloids via Fluorescence Microscopy*,” (Ph.D. December 2020), Lam Research Corporation
- Christian Ocier “*Realization of a 3D Gradient Index Medium in Porous Silicon*,” (Ph.D. May 2021), Apple
- Nathan Fritz “*Synthesis and Compositional Investigations of Electrodeposited Silicon for 3D Structured Lithium-ion Battery Anodes*,” (Ph.D. October 2022), Cabot Corporation
- Corey Richards, “*SCRIBE: Subsurface Volumetric Integration of Freeform Micro-Optical Elements for Advanced Beam Shaping and Light Routing*,” (Ph.D. December 2022), Apple
- Gaurav Singhal, “*Advancing Porous Heat Transfer Materials and Polymer Coatings with Photonic Structures*,” (Ph.D. December 2023), Intel
- Junrou Huang, “*Controlling transport properties and self-assembly of polymers using dynamic covalent chemistry*,” (Ph.D. December 2023) Yale
- Arghya Patra, “*Electrochemically Grown Ceramic Oxide Films for Energy Storage*,” (Ph.D. January 2024), University of Illinois
- Patrick Kwon, “*Can batteries take the heat? Investigating the electrode-electrolyte interface for solid-state battery performance at elevated temperatures*,” (Ph.D. June 2024), SES AI

- Michael Caple, “*Characterizing the Influence of Layered Transition Metal Oxide Morphology on Cathode Performance*” (Ph.D. June 2024), Argonne National Laboratory
- Youngbum Lee, “*Self-Healing Thermoset Polymers and Embedded 3D Printing via Chemical Activation,*” (Ph.D. August 2024), UC Santa Barbara
- Chen Chen, “Transport and segmental relaxation in polymer networks,” (Ph.D. December 2024),

Previous Postdocs/Visiting Scientists and First Placement (85 Total)

Dr. Kyung-Sang Cho (1999-2001) IBM

Dr. Michael Bevan (Beckman Fellow) (2001-2002) Chemical and Biomolecular Engineering, Johns Hopkins University.

Ms. Orla Wilson (September 2001-July 2002)

Mr. Seokwoo Jeon (August 2001-July 2002)

Dr. Sang Hern Kim (2002-2003), Hanbat National University, Korea

Dr. Wonmok Lee (March 2001-April 2003) Sejong University, Korea

Dr. Elena Rogojina (Rogozhina) (October 1999-July 2003) Lyten, Inc.

Dr. Alejandro Wolosiuk (November 2002-March 2006) Unidad de Actividad Química, CNEA, Centro Atómico Constituyentes

Mr. Dongyeon Son (May 2005-January 2006)

Dr. Huilin Tu (December 2005-July 2006) Schlumberger-Doll Research Center, Boston.

Dr. Ryan Kershner, *Beckman Fellow* (February 2004-October 2006) Mechanical Engineering, University of Wisconsin-Madison

Dr. Dong-Guk Yu (October 2005-July 2007) Samsung Corp., Korea

Dr. Florencio García Santamaría (January 2004-November 2007) General Electric

Dr. Weon Sik Chae (April 2005-December 2007) Korea Basic Science Institute

Dr. Jyh-Tsung Lee (February 2006-January 2008) National Sun Yat-Sen University

Dr. Jeong-Ho Park (2007-2010)

Dr. Matthew George (May 2009-March 2010) MOXTEK

Dr. Masao Miyake (April 2009-March 2010) Kyoto University

Dr. Yoonho Jun (October 2006-May 2010) Medical Devices

Mr. Shi Chen (September 2007-October 2008)

Ms. Peng Wan (December 2007-2008)

Mr. Chao-Lun Mai (September 2008-September 2009)

Mr. Sung-gyu Park (June 2009-December 2009)

Dr. Agustin Mihi (September 2008-August 2011) ICFO, Barcelona

Dr. Mark Losego (September 2008-September 2011) North Carolina State University

Dr. Joe Geddes (May 2010-April 2012) Rolith

Dr. Hui Gang Zhang (September 2007-July 2012) Nanjing University

Dr. Hongyi Sang (September 2011-September 2012) China Agricultural University

Dr. Jiping Yang (November 2011-September 2012) Beihang University

Dr. Ming Fu (January 2012-January 2013) Beihang University

Dr. Youngzheng Zhu (August 2012-February 2013)

Dr. Kristospher Waynant (July 2012-September 2013) University of Idaho

Dr. Chaeryong Cho (March 2013-February 2014) Pusan National University

Dr. Dong Hyun Kim (September 2010-May 2014)

Dr. Jiung Cho (September 2010-June 2014) KBSI

Dr. Jaewon Yoon (July 2013-June 2014), BASF

Prof. Suresh Valiyaveetil (July 2013-June 2014), National University of Singapore

Dr. Jun-Hee Choi (August 2013-August 2014), Samsung Advanced Institute of Technology

Prof. Jyh-Tsung Lee (July 2013-August 2014), National Sun Yat-Sen University

Prof. Chia-Chen Li (July 2013-August 2014), National Taipei University of Technology

Dr. Hyung-Jun Koo (August 2012-August 2014), Seoul National University of Science & Tech

Dr. Marta Hatzell (July 2014-July 2015), Georgia Tech University

Ms. Kai-Ling Liang (September 2014-July 2015)

Dr. Zhenxing Yu (August 2014-August 2015)

Dr. Jinyun Liu (May 2012-May 2016), Institute of Intelligent Machines of Chinese Academy of Sciences

Dr. Zhen Bi (August 2015-2016), Xidian University

Dr. Tsung-Han Tsai (October 2013-June 2016), DuPont

Dr. Wei Luo (September 2014-September 2016)

Dr. Jaewon Choi (Septebmer 2014-December 2016), Sungkyunkwan University

Dr. Jinwoo Kim (January 2013-December 2016), KAIST

Dr. Young Soo Yun (2015-2016)

Dr. Sung Kon Kim (March 2013-February 2017), Chonbuk University

Dr. Brian Mosby (July 2014-June 2017), Rollins College

Dr. Tingting Feng (September 2016-September 2017)

Dr. Masao Miyake (August 2016-August 2017), Kyoto University

Serkan Demirel, (June 2016-June 2017), Inonu University, Turkey

Dr. MinHo Yang (March 2016-August 2017), LG Innotek

Dr. Lilong Xiong (August 2016-September 2017)

Dr. Xiangming Li (September 2015-January 2017), Xi'an Jiaotong University

Dr. Limei Tian (2015-2018), Texas A&M University

Dr. Hao Chen (2015-2018)

Dr. Hongliang Guo (2015-2018)

Dr. Akkisetty Bhaskar (August 2016-August 2018), IIT Hyderabad

Dr. Zhao Li (2016-2018)

Dr. Yuefeng Liu (2016-2018), Jilin University

Prof. Jong-Ho Kim (July 2017-August 2018), Hanyang University

Yusen Huang (2017-2018), Xi-an Jiaotong University

Dr. Jong-Min Ju (July 2017-August 2018), Hanyang University

Dr. Juan Hong (2017-2019), Yancheng Institute of Technology

Dr. Mohammad Amdad Ali (September 2015-April 2019), University of Illinois

Dr. Ali Shayesteh (January 2019-April 2019)

Dr. Ali Can Zaman (October 2018-August 2019)

Dr. Hangchuan Zhang (October 2017-September 2019)

Dr. Xinlu Wang (October 2018-October 2019)

Dr. Fanying Kong (December 2018-November 2019)

Ms. Youngjin Ham (February 2020-July 2020)

Dr. Ravichandran Kollarigowda (January 2018-November 2020)

Dr. Sungbong Kim (February 2019-December 2020)

Dr. Dijo Damien (January 2020-October 2021)

Dr. Beniamin Zahiri (May 2019-February 2022), University of Illinois

Dr. Yuting Luo (April 2022-December 2023), Johns Hopkins University

Dr. Jay Taylor (January 2020-July 2024), Xerion Battery Corporation

Dr. Sung Bum Kang (October 2020-August 2024), Samsung

Dr. Lihong Lao (June 2022-August 2024), Syracuse University