

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner,

v.

Marlin Semiconductor Limited,

Patent Owner.

IPR2025-01082

U.S. Patent No. 6,888,181

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 6,888,181**

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EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 6,888,181 (“the ’181 Patent”)
1002	Prosecution File History, U.S. Patent No. 6,888,181 (“Prosecution History”)
1003	Declaration of Dr. Paul Braun
1004	U.S. Patent No. 7,045,401 (“Lee”)
1005	U.S. Patent No. 6,774,390 (“Sugiyama”)
1006	U.S. Patent No. 6,803,631 (“Dakshina”)
1007	U.S. Pat. App. Publication No. 2004/0036126 (“Chau”)
1008	U.S. Pat. App. Publication No. 2004/0061178 (“Lin”)
1009	U.S. Pat. App. Publication No. 2005/0017377 (“Joshi”)
1010	Reserved
1011	U.S. Patent No. 6,413,802 to Hu et al. (“Hu”)
1012	B. Doyle et al., Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout, Digest of the 2003 Symposium on VLSI Technology, pp. 133-34 (2003)
1013	B. S. Doyle et al., High Performance Fully-Depleted Tri-Gate CMOS Transistors, IEEE Electron Device Letters, Vol. 24, No. 4, pp. 263-65 (April 2003)
1014	Reserved
1015	S. Wolf et al., Silicon Processing for the VLSI Era Volume 1: Process Technology, 2 nd ed., pp. 225-29 (2000)

1016	U.S. Patent No. 5,461,250 to Burghartz et al. (“Burghartz”)
1017	U.S. Patent No. 6,339,232 to Shinichi Takagi (“Takagi”)
1018	U.S. Patent Application No. 10/227,068, as filed August 23, 2002
1019	T. Vogelsang; K.R. Hofmann, Electron mobilities and high-field drift velocities in strained silicon on silicon-germanium substrates, IEEE Transactions on Electron Devices, Volume: 39, Issue: 11, November 1992
1020	Y. X. Liu et al.; Flexible Threshold Voltage FinFETs with Independent Double Gates and an Ideal Rectangular Cross-Section Si-Fin Channel, IEEE International Electron Devices Meeting 2003, December 8-10, 2003
1021	JainNong Feng et al., BSIMSOI v.2.0 MOSFET Model – User’s Manual for BSIMDD2.0, Electronics Research Laboratory, 1999

LIST OF CHALLENGED CLAIMS

Claim Element	Claim Language
1[pre]	A three dimensional Triple Gate (Tri-gate) device comprising:
1[a]	a composite fin structure consisting of a silicon germanium core and a strained silicon epitaxy layer grown from surface of said silicon germanium core;
1[b]	a gate strip wrapping a portion of said composite fin structure,
1[c]	wherein portions of said composite fin structure not covered by said gate strip constitute source/drain regions of said Tri-gate device; and
1[d]	a gate insulating layer interposed between said composite fin structure and said gate strip.
2	The Tri-gate device of claim 1 wherein said composite fin structure has a substantially flat top surface and vertical sidewalls.
3	The Tri-gate device of claim 2 wherein said composite fin structure has a width of said flat top surface that is approximately equal to its height.
4	The Tri-gate device of claim 1 wherein said strained silicon epitaxy layer has a thickness of about 50~300 angstroms.
5	The Tri-gate device of claim 1 wherein said gate strip is made of polysilicon or metal gate.

6[pre]	A Tri-gate device comprising:
6[a]	a composite fin structure consisting of a semiconductor core and a strained epitaxy layer grown from surface of said semiconductor core, said semiconductor core having a first lattice constant that miss-matches a second lattice constant of said strained epitaxy layer;
6[b]	a gate strip wrapping a portion of said composite fin structure,
6[c]	wherein portions of said composite fin structure not covered by said gate strip constitute source/drain regions of said Tri-gate device; and
6[d]	a gate insulating layer interposed between said composite fin structure and said gate strip.
7	The Tri-gate device of claim 6 wherein said semiconductor core consists of silicon germanium.
8	The tri-gate device of claim 6 wherein said strained epitaxy layer is a strained silicon epitaxy layer.
9	The tri-gate device of claim 8 wherein said strained silicon epitaxy layer has thickness of about 50~300 angstroms.
10	The Tri-gate device of claim 6 wherein said gate strip is made of polysilicon or metal gate.

I. INTRODUCTION

Taiwan Semiconductor Manufacturing Company Ltd. (“Petitioner”) petitions for *Inter Partes* Review (“IPR”) of claims 1-10 (“the Challenged Claims”) of U.S. Patent No. 6,888,181 (“the ’181 Patent”). The Challenged Claims are unpatentable as set forth herein, and thus trial should be instituted and the Challenged Claims canceled.

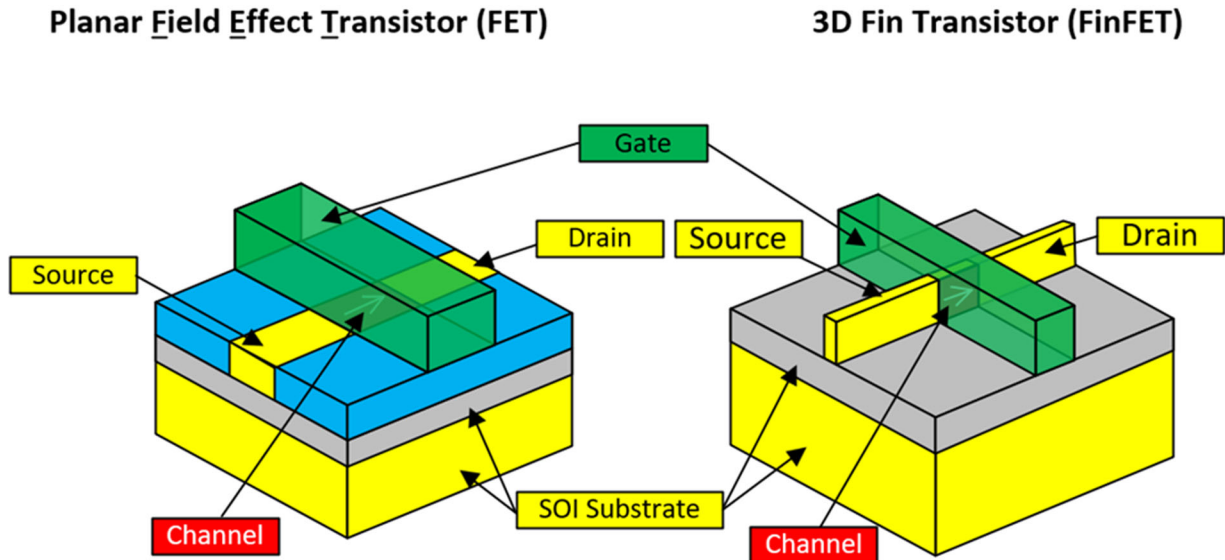
II. TECHNOLOGY BACKGROUND

A. Planar Field-Effect Transistor (FET) vs. Three-Dimensional Fin FET (FinFET)

A field-effect transistor (“FET”) includes three components: a “source,” a “drain,” and a “gate,” which together allow the transistor to operate as a switch by allowing or preventing current flow. TSMC-1003, ¶39. When the FET is “on,” current flows between the source and drain through a “channel” under the gate. When “off,” no current flows between the source and the drain. *Id.*

The figures below illustrate two types of FETs: a planar FET and a non-planar, three-dimensional “FinFET.” Traditional planar FETs are built into the surface region of a semiconductor substrate and utilize a two-dimensional structure in which the gate, source, and drain are oriented in the same plane. *Id.*, ¶40. By contrast, a FinFET has a three-dimensional fin structure where the channel rises up, extending three-dimensionally from an insulating layer of the substrate, with

the gate covering the top and sides of the fin. *Id.* As such, the gate, source, and drain terminals are not all oriented in the same plane, as seen below:



The operation and physics of both types of FETs is the generally the same, and their fabrication is also generally the same except for forming the fin shape in the FinFET. *Id.*, ¶41; *see also* TSMC-1011, Abstract, 2:11-14, 5:37-40; TSMC-1012, 1. The FinFET design offers advantages over planar FETs, including reducing parasitic resistance while facilitating large-scale integration and local interconnection. TSMC-1003, ¶40; *see also* TSMC-1012, 1; TSMC-1013, 1.

B. Multi-Gate Technology

FinFET devices have long utilized multi-gate structures, such as triple gates, to impart gate voltages on multiple sides of the channel region, i.e., the fin. *See* TSMC-1008, ¶[0006]; TSMC-1009, ¶¶[0044]-[0047], Figs. 8A-8F; TSMC-1001, 1:14-16, 1:37-39; TSMC-1003, ¶¶42-44. In this way, the channel width of the

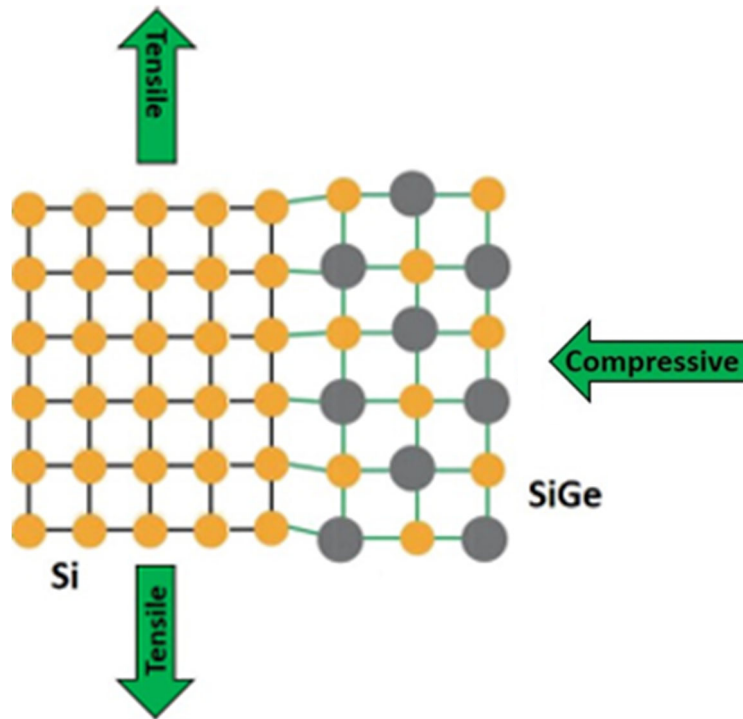
FinFET is dramatically increased, enabling a higher driving current as compared to planar FETs having single gates. *See* TSMC-1008, ¶[0006]; TSMC-1004, 2:9-18; TSMC-1013.

A “double gate” refers to a gate that is formed on at least two sides of the fin. TSMC-1004, 12:26-30; TSMC-1009, ¶[0047]; TSMC-1003, ¶43. A “triple gate” covers three sides of the fin; a “quadruple gate” covers all four sides of the fin. TSMC-1009, ¶[0046]; TSMC-1013, 1; TSMC-1003, ¶43. Prior to the ’181 Patent, and indeed as acknowledged by the ’181 Patent, three-dimensional FinFETs utilizing triple gate structures were well-known. *See, e.g.*, TSMC-1004, 12:26-30 (“The double gate 103 is actually a ***triple gate*** because it covers both sides and the top of the strained silicon channel 104.”); TSMC-1007, Title (“***Tri-gate devices*** and methods of fabrication”), TSMC-1009, ¶[0046] (“FIG. 8C represents a ***triple gate*** FinFET....”); TSMC-1013, Abstract (“Fully-depleted (FD) ***tri-gate*** CMOS transistors...have been fabricated.”). It was also already known that such triple-gate structures exhibited improved performance, including superior short-channel characteristics while maintaining full depletion at larger channel region dimensions, as compared to planar FETs with single gate structures. *See* TSMC-1013, Abstract; TSMC-1007, ¶¶[0016]-[0017].

C. Strained Silicon

Imparting strain to the silicon channel to improve performance was well-known prior to the '181 Patent. *See* TSMC-1009, ¶¶[0004]-[0006], [0044] (“[S]tretching the crystalline lattice structure of silicon can speed the flow of electrons through a transistor, thereby enhancing performance and decreasing power consumption.”); *see also* TSMC-1004, 1:66-2:8; TSMC-1008, Abstract, ¶[0029]; TSMC-1003, ¶¶45-48.

One well-known example utilizes strained silicon in combination with adjacent silicon germanium layers (“Si_xGe_{1-x}” or, more briefly, “SiGe”). TSMC-1009, ¶¶[0004]-[0006], [0044]; TSMC-1003, ¶46. Because silicon and silicon germanium have mismatched lattice constants (*see* TSMC-1015; TSMC-1016, 1:64-2:13, 4:32-39; TSMC-1017, 3:1-16, 4:12-22; TSMC-1008, ¶[0029]), the silicon atoms in the silicon layer experience tensile strain, as depicted below:



As known in the art, the strained silicon resulting from the mismatched structures along the planar Si-SiGe interface (TSMC-1009, ¶[0005]) beneficially allows charge carriers to move more quickly from source to drain. This is known as enhanced “channel mobility” or “charge carrier mobility.” Accordingly, strained silicon enhances electron/hole mobility and thus the driving current, improving the operating speed of the FinFET. TSMC-1009, ¶[0006]; TSMC-1017, 7:64-8:9; *see also* TSMC-1017, 7:64-8:9; TSMC-1008, Abstract, ¶¶[0009], [0029]; TSMC-1003, ¶47.

It was well-known to form such strained layers using epitaxial growth of silicon on SiGe cores. *See* TSMC-1004, 2:32-58, 4:20-28; TSMC-1007, ¶[0048]; TSMC-1008, Abstract, 3:44-4:11; TSMC-1003, ¶48. Epitaxial growth involves

growing a thin film of single crystal material upon a surface of a crystal substrate. TSMC-1015, 225. It was well-known that, by controlling the epitaxial growth process, strain could be induced in the underlying substrate layer. TSMC-1003, ¶48; TSMC-1004, 2:32-58, 4:20-28.

III. OVERVIEW OF THE '181 PATENT

The '181 Patent is directed to a “three-dimensional Triple-Gate (Tri-gate) device having a three-sided strained silicon channel,” which purportedly provides “superior drive current.” TSMC-1001, Abstract, 1:7-10. The '181 Patent says its Tri-gate device includes a “composite fin structure” that consists of a semiconductor (e.g., SiGe) core and a “*three-sided*” strained epitaxy layer (e.g., strained silicon) grown on the semiconductor core. *Id.*, Abstract, 2:15-19. “A gate strip wraps a channel portion of the composite fin structure” and a “gate insulating layer is interposed between the composite fin structure and the gate strip.” *Id.*, 2:19-24. Annotated Figure 1 depicts the composite fin structure, gate insulating layer, and gate strip of the Tri-gate device:

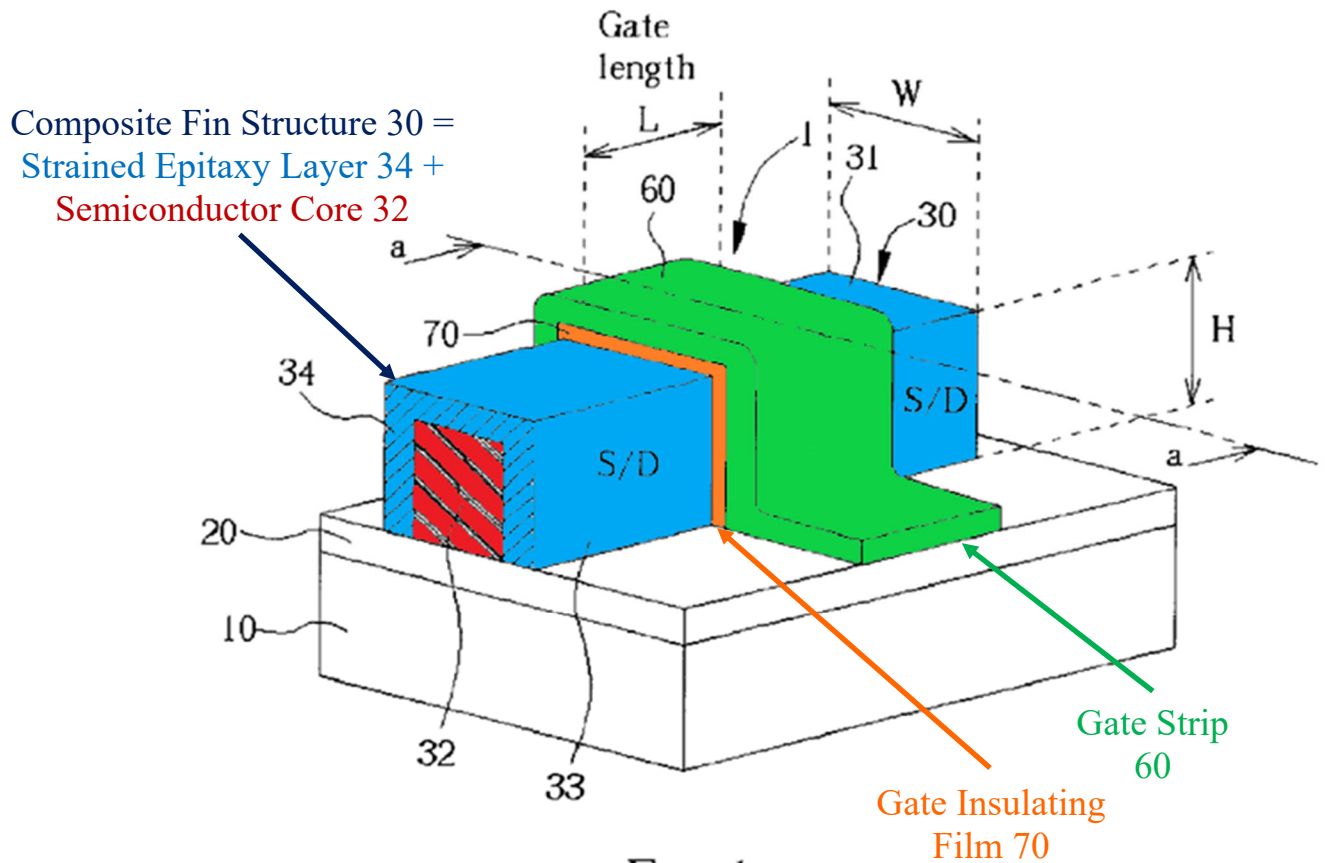


Fig. 1

The '181 Patent touts “strained silicon epitaxy layer 34” as “greatly improv[ing]” performance of the device by providing “superior carrier mobility, and thus higher drive current.” *Id.*, 3:18-21.

However, as discussed in the Technology Background above and explained in the Grounds below, it was well-known prior to the '181 Patent to utilize a composite fin structure having a strained silicon epitaxy layer grown on a silicon germanium core in a triple gate FinFET, and it was well-known that such a structure improved carrier mobility and increased drive current in the very same manner discussed in the '181 Patent.

A. Prosecution of the '181 Patent

During prosecution, the USPTO issued a single office action, September 7, 2004, in which claims 6 and 9-11 were rejected under 35 U.S.C. §103(a) over U.S. Pat. No. 6,764,884 (Yu). Yu is not relied on in this petition. Claims 1-5 were allowed, and claims 7-8 were noted as allowable. TSMC-1002, 38-41.

In a December 2, 2004 response, Applicant amended independent claim 6 to incorporate claim 7. *Id.*, 28-32. In particular, claim 6 was amended to recite “said semiconductor core having a first lattice constant that miss-matches a second lattice constant of said strained epitaxy layer.” *Id.* All claims were subsequently allowed. The Examiner did not consider any of the Lee, Sugiyama, Dakshina, or Chau references discussed herein.

IV. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art (hereinafter “POSITA”) would have had at least a Master’s degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work or research experience in semiconductor manufacturing, including FETs. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education. TSMC-1003, ¶34.

V. CLAIM CONSTRUCTION

The Board construes claims under the standard in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). For purposes of this proceeding, Petitioner does not believe that any terms need to be construed to resolve the prior art issues presented in this Petition. The Challenged Claims are invalid under their plain and ordinary meaning.

VI. GROUNDS OF CHALLENGE

Petitioner requests *inter partes* review and cancellation of the Challenged Claims on the following grounds:

Grounds	Challenged Claims	Statutory Basis	Prior Art
1	1-10	§102(e)/§103(a)	Lee
2	3	§103(a)	Lee and Chau
3	1-10	§§102(a), (e) /§103(a)	Sugiyama
4	3	§103(a)	Sugiyama with Chau
5	1-2, 4-10	§102(e)	Dakshina
6	3	§103(a)	Dakshina with Chau

Lee (U.S. Pat. No. 7,045,401; TSMC-1004) is prior art under pre-AIA §102(e). Lee was filed June 23, 2003, before the '181 Patent's filing date of March 18, 2004.

Sugiyama (U.S. Pat. No. 6,774,390; TSMC-1005) is prior art under pre-AIA §§102(a) and 102(e). Sugiyama was filed February 21, 2003, and published December 11, 2003, both before the '181 Patent's filing date.

Dakshina (U.S. Pat. No. 6,803,631; TSMC-1006) is prior art under pre-AIA §102(e). Dakshina was filed January 23, 2003, before the '181 Patent's filing date.

Chau (U.S. Pat. App. Pub. No. 2004/0036126; TSMC-1007) is prior art under pre-AIA §§102(a) and 102(e). Chau was filed August 23, 2002, and published February 26, 2004, both prior to the '181 Patent's filing date.

VII. CITED ART

A. Lee (TSMC-1004)

Lee is directed to “a strained silicon finFET device having a strained silicon fin channel.” TSMC-1004, Abstract. Lee's FinFET devices include a three-dimensional triple gate device having a triple gate 103 covering three sides of a composite fin structure (e.g., combination of “strained silicon layer 11”/“strained silicon channel 104” and SiGe “seed fin 10”/“seed fin 105”):

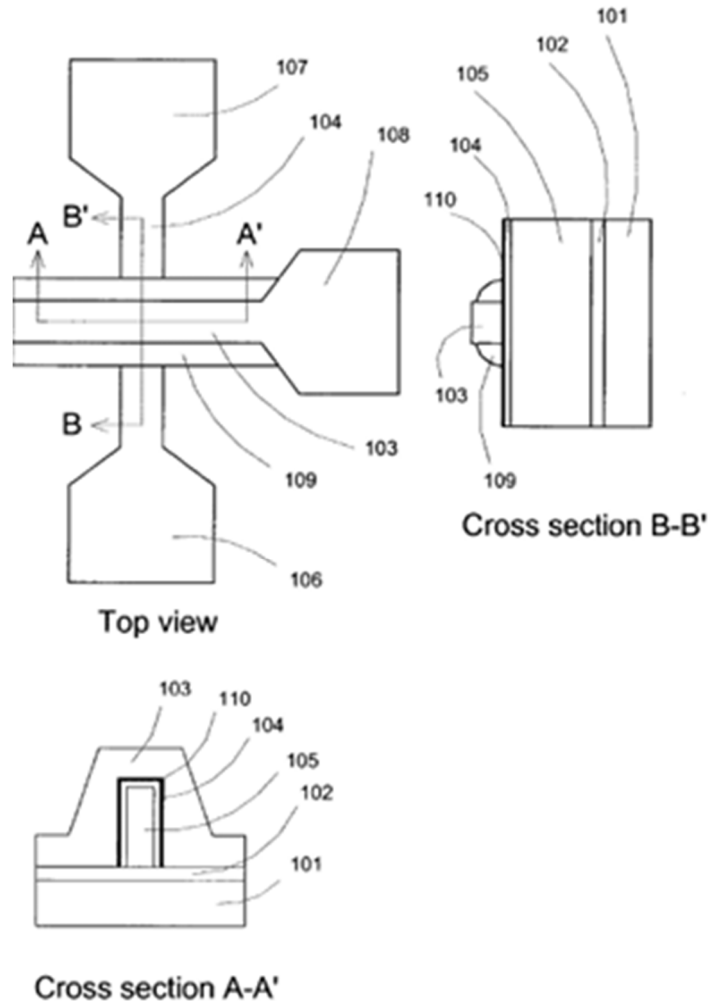


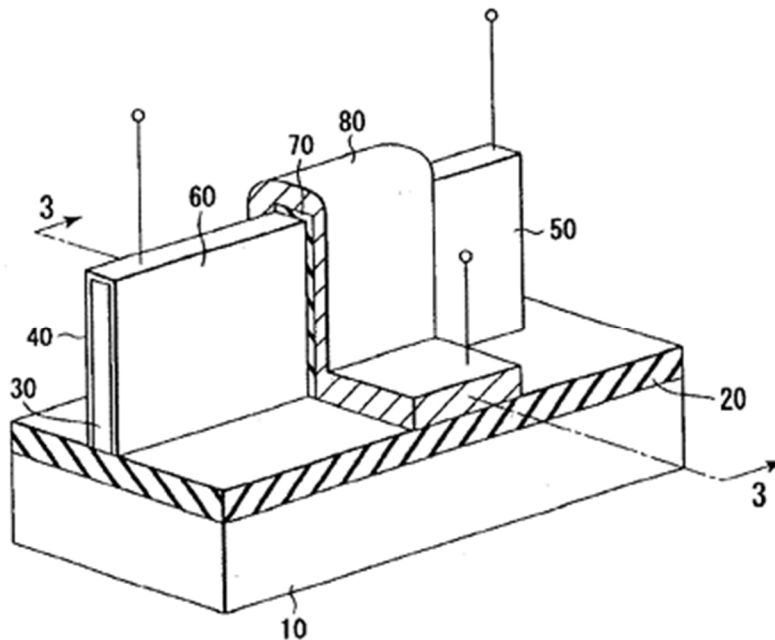
Fig. 14

TSMC-1004, 3:39-4:43, 12:31-48, Fig. 1.

Lee's composite fin structure consists of a SiGe seed fin 10/105 on which an epitaxial silicon layer 11/104 is grown. *Id.*, 3:51-54, 4:12-36, 12:34-36. A "lattice mismatch between the [epitaxial] silicon layer and the seed fin...improve[s] hole and electron mobility enhancement, in addition to short channel effect reduction characteristic inherently in a finFET device." *Id.*, Abstract. As discussed below, Lee's FinFET devices satisfy each limitation of the Challenged Claims.

B. Sugiyama (TSMC-1005)

Sugiyama is directed to a metal-insulator-semiconductor field-effect transistor (MISFET). TSMC-1005, 1:14-15. Sugiyama's MISFET devices include a composite fin structure that consists of a "projecting SiGe layer (semiconductor board) 30" and a "strained Si layer (semiconductor layer) 40 [that] is formed on the side and upper surfaces of the SiGe layer 30." *Id.*, 6:65-7:2. A gate (e.g., "band-like gate electrode 80") surrounds the composite fin structure on three sides (*see id.*, 7:8-10, Fig. 2):



Accordingly, Sugiyama's MISFET device is a three-dimensional triple gate FinFET device. TSMC-1003, ¶59.

Additionally, just as in the '181 Patent, Sugiyama explains that a lattice constant mismatch resulting from the strain induced by growth of strained Si layer 40 on SiGe layer 30 results in higher performance due to increased carrier mobility. *See* TSMC-1005, 5:35-63.

As discussed below, Sugiyama's MISFET devices satisfy each limitation of the Challenged Claims.

C. Dakshina (TSMC-1006)

Dakshina is directed to FinFETs having "a fin and a [strained] layer formed on the fin." TSMC-1006, 1:5-6, Abstract. Dakshina's devices have an epitaxially-grown "strained channel layer [that] include[s] a crystalline material that is lattice constant mismatched with the crystalline material of the fin of the FinFET. The lattice constant mismatch induces tensile strain within the strained channel layer that increases carrier mobility [which], in turn, increases the drive current of the FinFET transistor." *Id.*, 1:31-40, 3:61-67.

Accordingly, just as in the '181 Patent, Dakshina's FinFETs constitute three-dimensional triple gate devices having a composite fin structure that utilizes a lattice constant mismatch induced by a strained epitaxial layer to increase carrier mobility. TSMC-1003, ¶62. Dakshina's FinFETs satisfy the limitations of nearly all Challenged Claims.

D. Chau (TSMC-1007)

Chau is directed to the design and fabrication of “tri-gate” FinFET devices. TSMC-1007, Title (“Tri-gate devices and methods of fabrication”). Chau’s tri-gate devices include fins (e.g., semiconductor bodies 520) around which a gate electrode 530 is formed. *Id.*, ¶¶[0039]-[0040]. An epitaxial silicon layer is grown on the fins, forming a composite fin structure. *Id.*, ¶[0048].

Chau teaches varying the height and width dimensions of the semiconductor bodies/fins 520 to accommodate desired manufacturing constraints and/or performance characteristics for the FinFET, including configurations in which body heights and widths are approximately the same to configurations in which body height is between half to twice the body width. *Id.*, ¶¶[0019], [0037], Fig. 6.

Accordingly, Chau teaches choosing dimensions of a composite fin structure such that the width of the fin structure is approximately equal to its height.

VIII. GROUND 1: Lee anticipates, or alternatively renders obvious, Claims 1-10

Lee anticipates, or alternatively renders obvious, Claims 1-10 as detailed below and in Dr. Braun’s declaration (*see* TSMC-1003, §IX(A)).

i) Claim 1

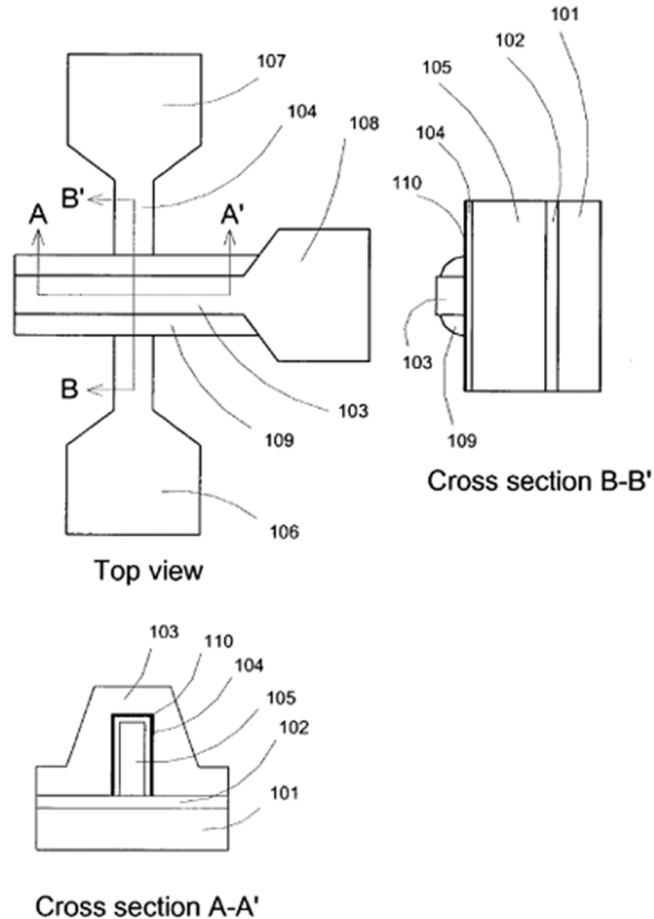
1[pre] “Three Dimensional Triple Gate (Tri-gate) Device”

Claim 1’s preamble calls for a three dimensional Triple Gate (Tri-gate) device. To the extent the preamble is considered limiting, Lee discloses a three-

dimensional Tri-gate device, e.g., “strained silicon finFET device.” TSMC-1004, 3:49-51; *see also id.*, Abstract, 3:51-4:11, 4:33-36, 12:17-30, Fig. 14; TSMC-1003, ¶¶67-70.

Lee’s “strained silicon finFET device” includes a “channel 104” in which “conduction is controlled by double gate 103.” TSMC-1004, 12:17-24, Fig. 14. Lee explains that “double gate 103 is *actually a triple gate* because it covers both sides and the top of the strained silicon channel 104. *The term ‘double gate’...is a generic term to mean ‘more than one gate’, and therefore covers double or triple gate devices.*”¹ *Id.*, 12:26-30; *see also id.*, 12:34-40. Figure 14 depicts Lee’s three-dimensional Tri-gate device:

¹ All emphases throughout Petition are added.



Additionally, Lee’s “triple gate device” is “three dimensional” because of its fin structure comprising “fin channel 104” and “seed fin layer 105,” which extends in three dimensions from “insulator 102” on “substrate 101.” TSMC-1003, ¶69; TSMC-1004, 12:17-40, Fig. 14; *supra*, §II(A).

Accordingly, Lee’s FinFET devices constitute “three dimensional Triple Gate (Tri-gate) devices,” as recited in claim 1’s preamble.

1[a] “Composite Fin Structure”

Element 1[a] calls for “a composite fin structure consisting of a silicon germanium core and a strained silicon epitaxy layer grown from surface of said silicon germanium core,” which Lee discloses. TSMC-1003, ¶¶71-75.

For example, Lee’s FinFETs include a composite fin structure (referred to variously as a “strained silicon fin structure,” “silicon fin channel,” “finFET channel”) consisting of: (i) a silicon germanium core (e.g., “silicon germanium seed fin,” “silicon germanium seed fin 10,” “seed fin 105”), and (ii) a strained silicon epitaxy layer (e.g., “strained silicon layer,” “silicon layer 11,” “strained silicon channel 104”) grown from the surface of the silicon germanium core. *See* TSMC-1004, Abstract, 3:49-4:36, 11:31-38, 12:17-48, 16:26-41, Figs. 1, 3C, 14; TSMC-1003, ¶71.

Annotated Figures 1 and 14 depict Lee’s composite fin structure constructed from the combination of silicon germanium fin 10/105 (depicted in red) and strained silicon epitaxy layer 11/104 (depicted in blue):²

² Figures 1 and 14 depict a same composite fin structure design. TSMC-1003, ¶72.

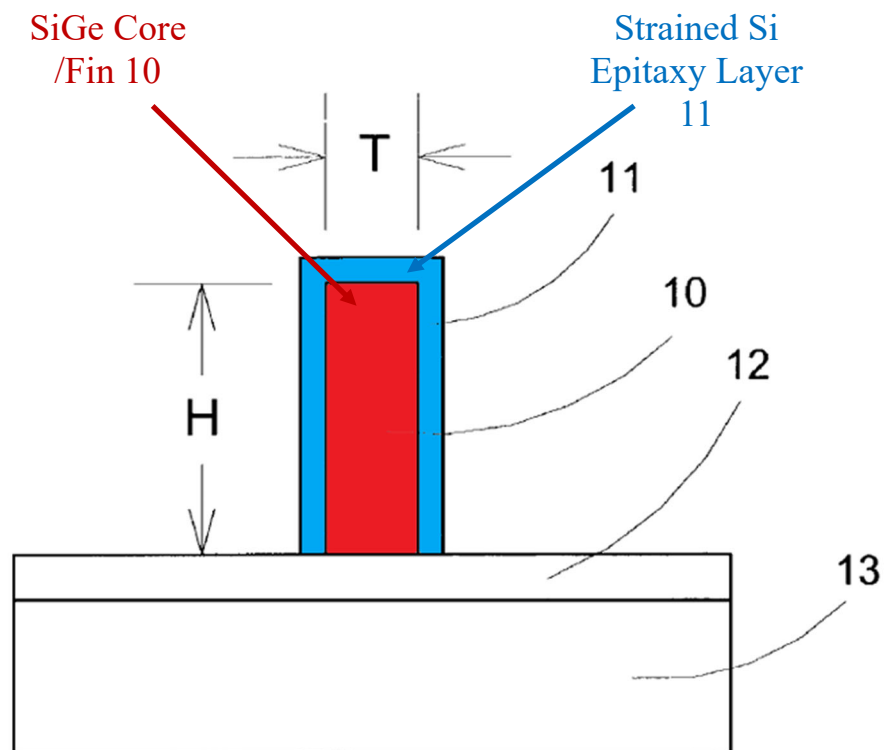


Figure 1

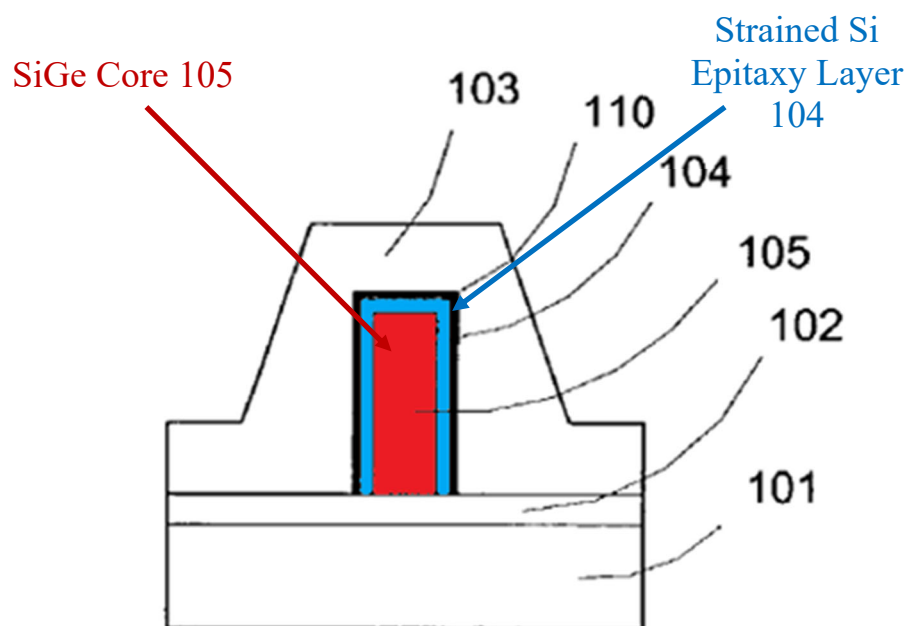


Figure 14

TSMC-1003, ¶72.

Regarding Figure 1, Lee describes a “strained silicon fin structure” that consists of “*strained* channel *silicon* layer 11” “cover[ing] a relaxed *silicon germanium*...seed fin 10.” TSMC-1004, 4:7-13. “Strained channel silicon layer 11” is an “*epitaxial* silicon layer” that is “grown on the seed fin 10.” *Id.*, 4:18-28, 6:58-7:7, Figs. 3b-3c, claims 2-3. Accordingly, Lee’s strained silicon layer is an epitaxy layer grown from the surface of the silicon germanium seed fin/core.

TSMC-1003, ¶73.

The FinFET device of Figure 14 likewise includes “a seed fin 105 and a strained silicon channel 104, covering both sides and the top of the seed fin 105.” TSMC-1004, 12:34-37. “Strained silicon channel 104” is “*grown on* the seed fin 105” (*id.*, 12:52-55) and may include an “*epitaxial* silicon layer deposited on a relaxed silicon germanium seed fin” (*id.*, 11:32-38).

Accordingly, Lee’s FinFETs satisfy limitation 1[a].

1[b] “Gate Strip”

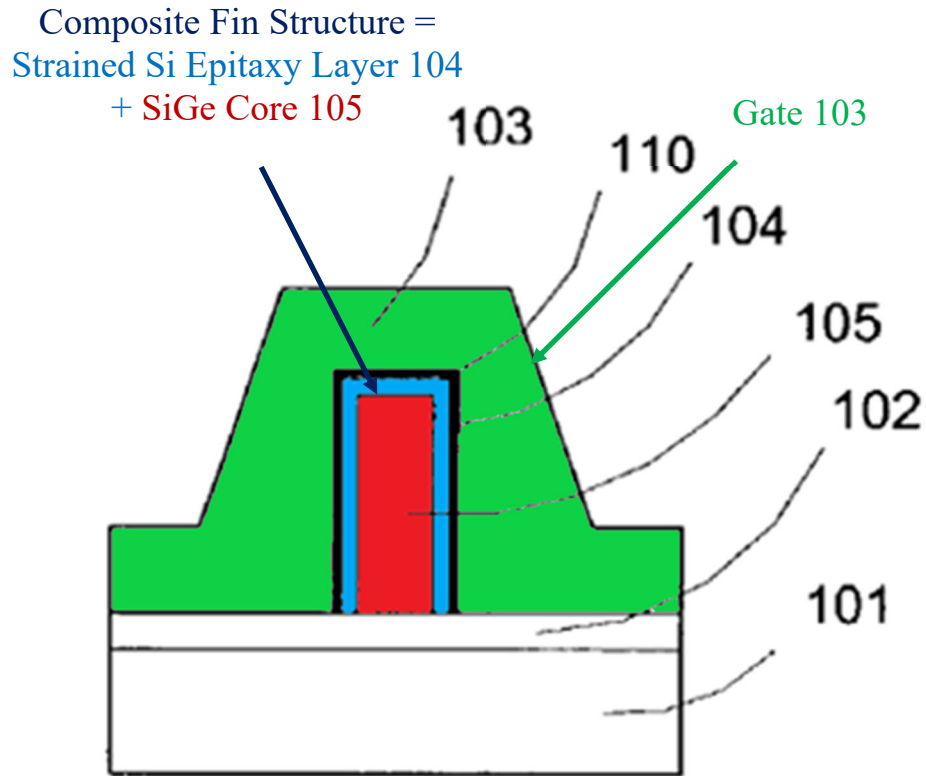
Element 1[b] calls for “a gate strip wrapping a portion of said composite fin structure,” which Lee discloses. TSMC-1003, ¶¶76-78.

Specifically, Lee discloses a gate strip (e.g., “gate 103”) wrapping a portion of the composite fin structure (e.g., “strained silicon fin structure,” “silicon fin channel,” “finFET channel”). *See* TSMC-1004, 12:21-48, 3:54-59, 13:17-42, 15:1-

36, 16:34-36, Fig. 14; TSMC-1003, ¶76. Lee explains that “channel 104 conduction is controlled by the double *gate 103*, extending and covering the channel 104, and connected to the gate electrode 108.... The double **gate 103** is actually a triple gate because it *covers both sides and the top of the strained silicon channel 104*.” TSMC-1004, 12:21-39.

Annotated Figure 14 cross section A-A’ depicts gate 103 wrapping a portion of the composite fin structure/fin channel on the top surface and both sides:³

³ In Figure 14, Lee’s gate 103 is electrically isolated from channel 104 including by gate dielectric 110. TSMC-1004, 12:24-26. The ’181 Patent embodiment is directly analogous, illustrating, in Figure 6, gate insulating layer 70 between gate strip 60 and composite fin structure 34/90. TSMC-1001, 3:41-44, 3:60-4:8.



TSMC-1003, ¶77.

Figure 14's top and cross section B-B' views further depict gate 103 extending across a central portion of strained Si epitaxy layer 104 and SiGe core 105, i.e., covering part of layer 104/core 105. *Id.*, ¶78. Accordingly, Lee's gate 103 constitutes a gate strip that wraps a portion of the combined strained Si epitaxy layer 104/SiGe core 105 (i.e., the "composite fin structure"), satisfying this limitation.

1[c] “Source/Drain Regions”

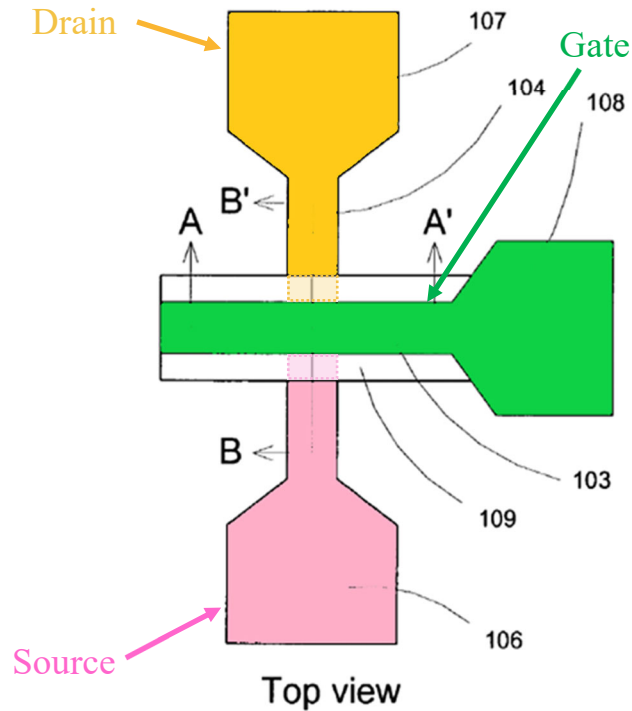
Element 1[c] specifies that “portions of said composite fin structure not covered by said gate strip constitute source/drain regions of said Tri-gate device.”

Lee discloses this element. TSMC-1003, ¶¶79-81.

Specifically, Lee discloses that portions of said composite fin structure (e.g., “strained silicon fin structure,” “silicon fin channel,” “finFET channel”) not covered by said gate strip (e.g., “gate 103”) constitute source/drain regions (e.g., “source 106,” “drain 107”) of the Tri-gate device. *See* TSMC-1004, 2:61-64; 3:54-56, 12:17-21, 13:17-42, Fig. 14, claim 1; TSMC-1003, ¶79. Regarding the FinFET of Figure 14, Lee states that “a *source 106* and a *drain 107 [are] separated by a channel 104*” (TSMC-1004, 12:20-21), with channel 104 covered by gate 103 (TSMC-1004, 12:26-28; *see also id.*, 12:37-38, 10:46-48).

Lee’s Figure 14 top view depicts the portions of the composite fin structure not covered by gate 103 (in green) that constitute source 106 (pink) and drain 107 (gold):⁴

⁴ Uncolored portion 109 is a “spacer” that “isolate[s] double gate 103 from the silicon channel 104.” TSMC-1004, 12:63-64. Thus, spacer 109 is not itself part of Lee’s “composite fin structure.” TSMC-1003, ¶80.



TSMC-1003, ¶80.

Accordingly, Lee’s composite fin structures include portions not covered by gate 103 that constitute source/drain regions (including the source and drain portions under spacers 109), satisfying this limitation.

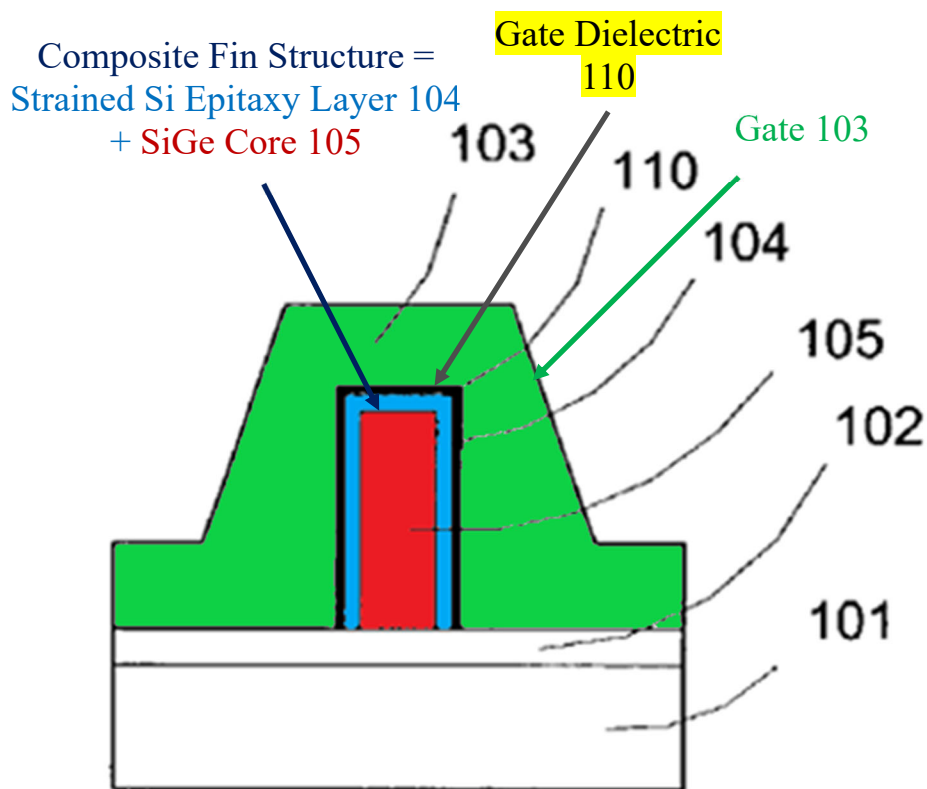
1[d] “Gate Insulating Layer”

Element 1[d] calls for “a gate insulating layer interposed between said composite fin structure and said gate strip,” which Lee discloses. TSMC-1003, ¶¶82-84.

Specifically, Lee discloses a gate insulating layer (e.g., “gate dielectric 110”) interposed between the composite fin structure (e.g., “strained silicon fin

structure,” “silicon fin channel,” “finFET channel”) and gate strip (e.g., “gate 103”). See TSMC-1004, 3:49-59, 12:24-57, 13:33-40, Fig. 14; TSMC-1003, ¶82.

Lee’s “gate 103 is **electrically isolated** from the channel 104 by a *gate dielectric 110*,” which is thus a “gate insulating layer.” TSMC-1004, 12:39-40; see also *id.*, 12:24-26; TSMC-1003, ¶83. As depicted in annotated Figure 14’s cross section A-A’, gate dielectric 110 is interposed between Lee’s composite fin structure (i.e., the combination of strained silicon channel 104 and seed fin 105) and Lee’s gate strip (i.e., “gate 103”):



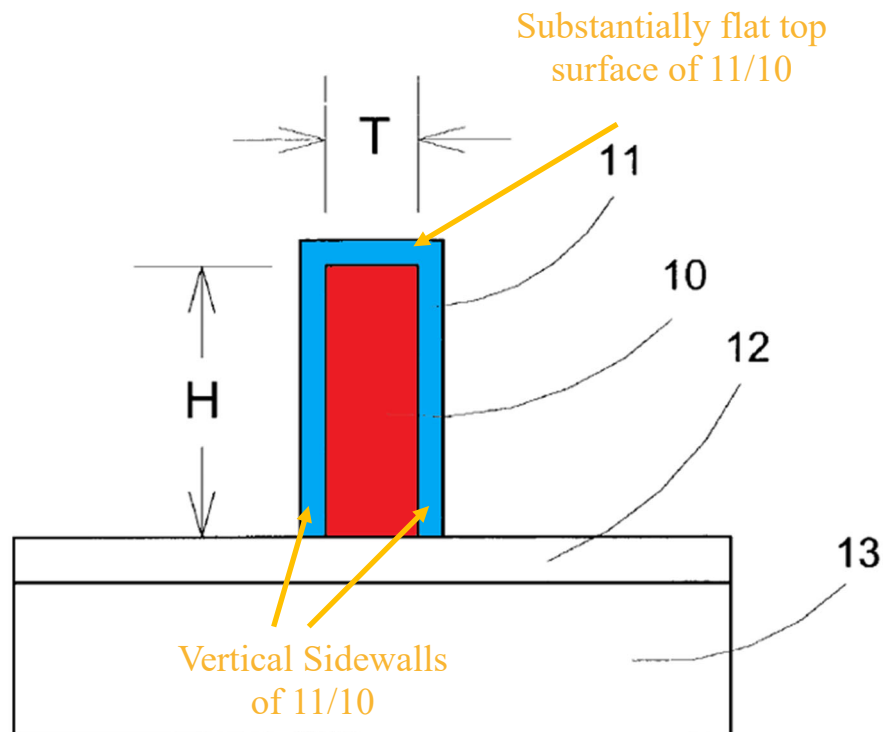
TSMC-1003, ¶83; see also TSMC-1004, Fig. 14 cross section B-B’ (illustrating gate dielectric 110 disposed between the gate and the composite fin structure).

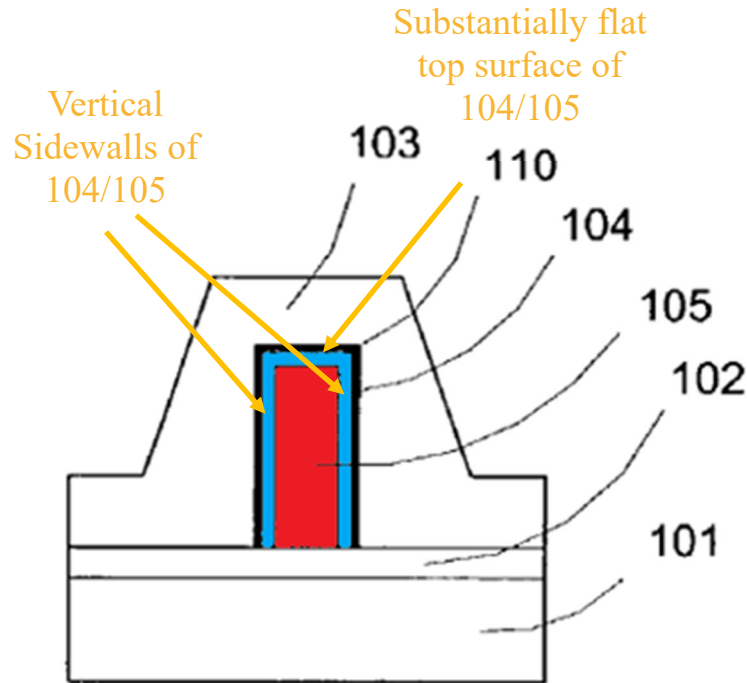
Accordingly, Lee satisfies limitation 1[d] and anticipates claim 1.

ii) Claim 2

[2] The Tri-gate device of claim 1 wherein said composite fin structure has a substantially flat top surface and vertical sidewalls.

As depicted in annotated Figures 1 and 14 below, Lee's composite fin structure has a substantially flat top surface and vertical sidewalls. See TSMC-1004, Abstract, 3:49-4:43, 10:42-50, 12:17-48, Figs. 1, 3C, 14; TSMC-1003, ¶¶86-89. Lee's strained silicon channel 104, which covers the sides and top of seed fin 105, has "sides" and a "top." See TSMC-1004, 12:26-28, 12:34-39. These "sides" of Lee's composite fin structure are vertical, and the "top" surface of the composite fin structure is substantially flat:





TSMC-1003, ¶¶87-88; *see also* TSMC-1004, Fig. 14 cross-section B-B’

(disclosing a composite fin structure made of strained silicon channel 104/seed fin 105 with a substantially flat top surface).

Accordingly, the “sides” and “top” of Lee’s strained silicon channel 104/seed fin 105 constitute “vertical sidewalls” and a “substantially flat top surface,” satisfying claim 2.

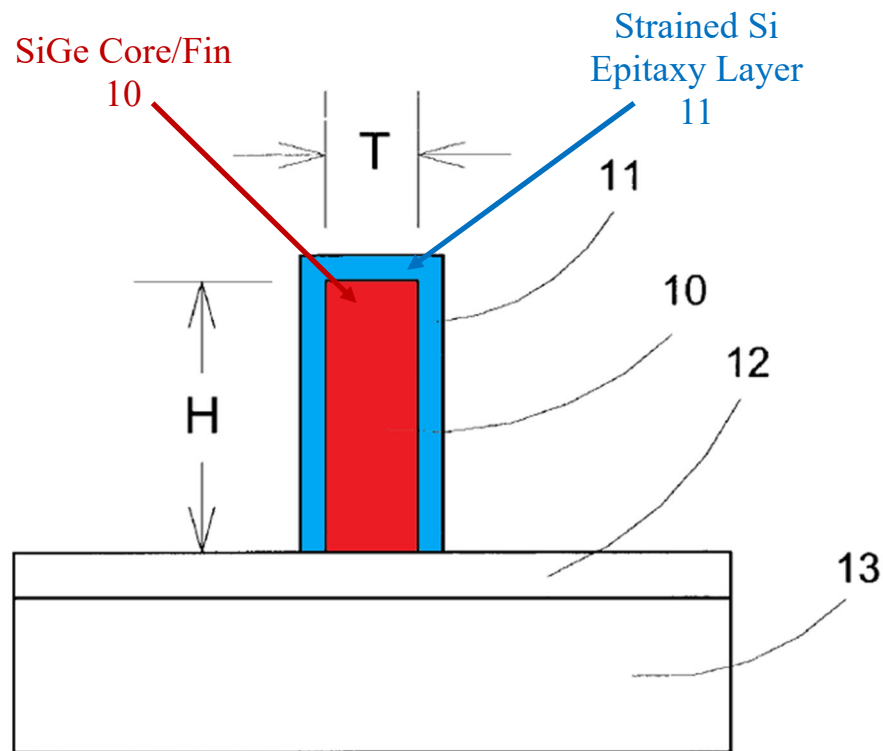
iii) Claim 3

[3] The Tri-gate device of claim 2 wherein said composite fin structure has a width of said flat top surface that is approximately equal to its height.

Lee anticipates claim 3.

Lee's composite fin structure has a width of said substantially flat top surface that is approximately equal to its height, and thus anticipates claim 3. TSMC-1004, 4:33-43, Figs. 1, 14; TSMC-1003, ¶¶90-97.

As depicted in annotated Figure 1, Lee discloses a composite fin structure (e.g., the combination of SiGe fin 10 and strained silicon epitaxy layer 11):



TSMC-1003, ¶91; *supra* §VIII(i)(1[a]).

Referring to the height “H” and thickness “T” of SiGe fin 10 depicted in Figure 1, Lee explains that the “seed fin” (e.g., “silicon germanium fin 10”/“seed fin 105”) has a “height H [that] is preferably in the range of 10 nm to 200 nm” and a “thickness T” (i.e., a “width”) that “is preferably in the range of 5 nm to 100

nm.” TSMC-1004, 4:12-43, Fig. 1. Additionally, Lee describes the preferred thicknesses for the strained epitaxial silicon layer 11 formed on SiGe seed fin 10, stating that the “epitaxial silicon layer” (e.g., “strained channel silicon layer 11,” “strained silicon channel 104”) has a “thickness [that] is preferably in the range of 5 to 15nm.” *Id.* The thickness of the epitaxial silicon layer is uniform on the top and sides. *Id.*

As understood from Figures 1 and 14, the height of the top surface of Lee’s composite fin structure (i.e., H_{CFS}) is equal to the height of the seed fin (i.e., H_{SF}) plus the thickness of the “epitaxial silicon layer” (i.e., T_{ESL}), such that $H_{CFS} = H_{SF} + T_{ESL}$. TSMC-1003, ¶94. The width of the top surface of Lee’s composite fin structure (i.e., W_{CFS}) is equal to the thickness of the seed fin (i.e., T_{SF}) plus two times the thickness of the epitaxial silicon layer (i.e., T_{ESL}), such that $W_{CFS} = T_{SF} + 2 * T_{ESL}$. *Id.*

As discussed above, Lee discloses, as endpoints of disclosed ranges, that the “height H of the seed fin” may be 10 nm, the “thickness T of the seed fin” may be 5 nm, and the “epitaxial silicon layer thickness” may be 5 nm. TSMC-1004, 4:36-40. The overall height and width of Lee’s composite fin structure can thus be calculated using these expressly disclosed dimensions:

$$H_{CFS} = 10 \text{ nm} + 5 \text{ nm} = 15 \text{ nm}$$

$$W_{CFS} = 5 \text{ nm} + 2 * (5 \text{ nm}) = 15 \text{ nm}$$

TSMC-1003, ¶95. As seen, using the lower endpoints of Lee’s ranges for the height and width of the fin core and the epitaxial layer thickness, the total height of Lee’s composite fin structure is substantially equal to the total width of its top surface. *Id.*

A composite fin structure having a substantially equal width and height likewise also results from selecting dimensions other than the endpoints of Lee’s disclosed ranges. For example, selecting a seed fin height H of 80 nm (within Lee’s disclosed 10-200 nm height range), a seed fin thickness T of 70 nm (within Lee’s disclosed 5-100 nm thickness range), and an epitaxial silicon layer thickness of 10 nm (within Lee’s disclosed 5-15 nm thickness range), results in a composite fin (the seed fin plus epitaxial layer) having an equal height and width of 90 nm. *Id.*, ¶96. As apparent to a POSITA, numerous other dimension selections within Lee’s disclosed ranges also result in a composite fin structure having a substantially equal width and height. *Id.*

The Federal Circuit has explained that, even “[i]f the prior art discloses its own range, rather than a specific point,” such art is anticipatory if “it describes the claimed range with sufficient specificity such that a reasonable fact finder could conclude that *there is no reasonable difference in how the invention operates over the ranges.*” *Ineos USA LLC v. Berry Plastics Corp.*, 783 F.3d 865 (Fed. Cir. 2015) (emphasis added). For example, the Court held that a prior art disclosure for a

process of clarifying water with alkalinity below 150 ppm was defined with sufficient specificity to anticipate a claim to a similar process for water with alkalinity of 50 ppm or less, because there was “no evidence demonstrating any difference across the range.” *Clearvalue, Inc. v. Pearl River Polymers, Inc.*, 668 F.3d 1340 (Fed. Cir. 2012). Like in *Clearvalue*, there is no evidence in either the ’181 Patent or Lee that demonstrates that a composite fin structure having equal height and width dimensions would operate significantly differently than a composite fin structure having other height and width dimensions from within Lee’s disclosed ranges. Regarding the equal width and height of a composite fin structure, the ’181 Patent does not explain how (or even whether) having equal height and width dimensions would impact device performance or operation, stating only that such dimensions may be used “[a]ccording to the preferred embodiment.” TSMC-1001, 3:11-13, 3:46-49.

Additionally, a POSITA understood at the time that equal height and width dimensions for the composite fin structure would not have significantly impacted the operation of the device vis-à-vis other different (i.e., non-equal height and width) dimensions within Lee’s ranges. TSMC-1003, ¶97. Indeed, similar performance characteristics could have been achieved by such a device when the height and width of its composite fin structure were either substantially equal or somewhat different. *Id.*; see also TSMC-1007, [0027], Fig. 6 (depicting full

depletion achieved with composite fin structures of equal height/width and differing height/width); *infra*, §IX(i).

Alternatively, Lee renders claim 3 obvious

Alternatively, substantially equal height and width dimensions for a composite fin structure were obvious in view of Lee. TSMC-1003, ¶¶90-100. As demonstrated above, the preferred dimension ranges for Lee’s composite fin structure components substantially overlap with dimensions that satisfy the limitations of claim 3. In such situations, the Federal Circuit has stated that “[a] *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art.” *E.I. du Pont de Nemours & Co. v. Synvina C.V.*, 904 F.3d 996, 1006 (Fed. Cir. 2018) (*quoting In re Peterson*, 315 F.3d 1325, 1329 (Fed. Cir. 2003)); *see also In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); *In re Harris*, 409 F.3d 1339 (Fed. Cir. 2005) (“[A] *prima facie* case of obviousness arises when the ranges of a claimed composition overlap the ranges disclosed in the prior art.”).

To overcome this presumption, there must be “[e]vidence that the variables interacted in an unpredictable or unexpected way [to] render the combination nonobvious.” *In re Applied Materials*, 692 F.3d 1289, 1298 (Fed. Cir. 2012); *see also In re Richard E. Woodruff*, 919 F.2d 1575 (Fed. Cir. 1990). Here, the ’181 Patent offers no evidence of an unpredictable, surprising, or unexpected result

associated with an “approximately equal” width and height for the composite fin structure, nor does the ’181 Patent teach any criticality of such dimensions.

Additionally, a POSITA at the time would have recognized that there was no criticality associated with such dimensions. TSMC-1003, ¶97. Indeed, as demonstrated by Chau, a POSITA well understood the impact of varying fin structure dimensions on the operation of the device. *Id.*, see TSMC-1007, Fig. 6. Because the ’181 Patent does not demonstrate any criticality of the claimed equal height and width dimensions (and indeed no such criticality exists), the mere selection of such dimensions is obvious.

Still further, “where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” *In re Aller*, 220 F.2d 454 (CCPA 1955); see also *E.I. du Pont de Nemours*, 904 F.3d at 1006. As discussed by Lee, it was well-known to choose dimensions of the composite fin structure to “ensure fully depleted body under the operation conditions of the finFET device.” See TSMC-1004, 4:36-43; see also TSMC-1007, Fig. 6. Accordingly, it was apparent to a POSITA prior to the ’181 Patent that the width and height dimensions of a seed fin as well as the thickness of an epitaxial layer on the seed fin could be varied as needed to ensure full depletion. TSMC-1003, ¶¶90, 134. Contemporary prior art (e.g., Chau) further demonstrated that it was well-known to select width and height dimensions of a composite fin

structure in accordance with other characteristics of the device (e.g., gate length) while ensuring full depletion. *See* TSMC-1007, Fig. 6; *infra*, §IX(i). And as demonstrated in the graph in Chau's Figure 6, both equal height and width dimensions as well as non-equal height and width dimensions for a composite fin structure provide a fully depleted device. *See id.*; TSMC-1003, ¶¶133-134.

Still further, a POSITA prior to the '181 Patent would have understood and balanced other competing design considerations when selecting specific dimensions for the fin structure, including current carrying capacity, horizontal space constraints, cost, and manufacturing complexity. TSMC-1003, ¶98. A POSITA understood that composite fin structures having equal width and height were a suitable option depending on the specific combination of considerations at issue for a given design. *Id.*

Finally, a POSITA would have found implementing approximately equal height and width dimensions in composite fin structures to be routine and easily achievable (and indeed easier than high aspect ratio double-gate devices) at the time of the alleged invention, and thus would have had a reasonable expectation of success in doing so. *Id.*, ¶99. Such a modification would have amounted to merely creating a composite fin structure having the selected approximately equal height and width dimensions while utilizing the same fabrication techniques (e.g., well-

known patterning, etching, and deposition techniques) already widely used for creating fin structures in FinFET devices.

For example, Chau teaches forming composite fin structures using “well-known photolithographic and etching techniques” (e.g., to form the semiconductor body/core of the composite fin structure) and epitaxial deposition processes (e.g., for forming the semiconductor/silicon film 560 portion of the composite fin structure). *See* TSMC-1007, ¶¶[0036]-[0038], [0048], Figs. 5A-5H. Lee utilizes similar processes for forming its composite fin structures. *See* TSMC-1004, 13:43-14:67. These fabrication processes were well-known, and thus a POSITA would have found it straightforward to implement such processes to fabricate a composite fin structure having approximately equal height and width dimensions arrived at through routine optimization. TSMC-1003, ¶¶99, 143.

Accordingly, Lee anticipates, or alternatively renders obvious, claim 3.

iv) Claim 4

[4] The Tri-gate device of claim 1 wherein said strained silicon epitaxy layer has a thickness of about 50-300 angstroms.

Lee’s strained silicon epitaxy layer has a thickness that “is preferably in the range of 5 nm to 15 nm.” TSMC-1004, 4:38-40. Because 5-15 nm (i.e., nanometers) is equivalent to 50-150 Ångstroms, Lee discloses the 50-300 Ångstroms limitation of claim 4. TSMC-1003, ¶101.

v) Claim 5

[5] The Tri-gate device of claim 1 wherein said gate strip is made of polysilicon or metal gate.

Lee discloses that the “gate of the disclosed strained silicon finFET structure is preferably polysilicon, doped polysilicon or metal.” TSMC-1004, 13:40-42; *see also id.*, 15:10-36. Accordingly, Lee’s gate strip (e.g., “gate 103”) is made of polysilicon or metal, each of which satisfies claim 5. TSMC-1003, ¶102.

vi) Claim 6

6[pre] “Tri-gate Device”

Lee discloses a Tri-gate device. *Supra*, §VIII(i)(1[pre]); TSMC-1004, 3:49-51, Abstract, 3:51-4:11, 4:33-36, 12:17-30, Fig. 14; TSMC-1003, ¶103.

6[a] “Composite Fin Structure”

Element 6[a] calls for “a composite fin structure consisting of a semiconductor core and a strained epitaxy layer grown from surface of said semiconductor core, said semiconductor core having a first lattice constant that miss-matches a second lattice constant of said strained epitaxy layer.” Lee discloses this element. TSMC-1003, ¶¶104-110.

Specifically, Lee’s composite fin structure consists of: i) a semiconductor core (e.g., “silicon germanium seed fin,” “silicon germanium seed fin 10,” “seed fin 105”); and ii) a strained epitaxy layer (e.g., “strained silicon layer,” “silicon layer 11,” “strained silicon channel 104”) grown from surface of said

semiconductor core. See TSMC-1004, Abstract, 3:49-4:30, 11:31-38, 12:17-48, 16:26-33, Figs. 1, 3C, 14; TSMC-1003, ¶104; *supra*, §VIII(i)(1[a]).

Annotated Figures 1 and 14 depict Lee's composite fin structure (i.e., the combination of semiconductor core/fin 10/105 (depicted in red) and strained silicon epitaxy layer 11/104 (depicted in blue)):

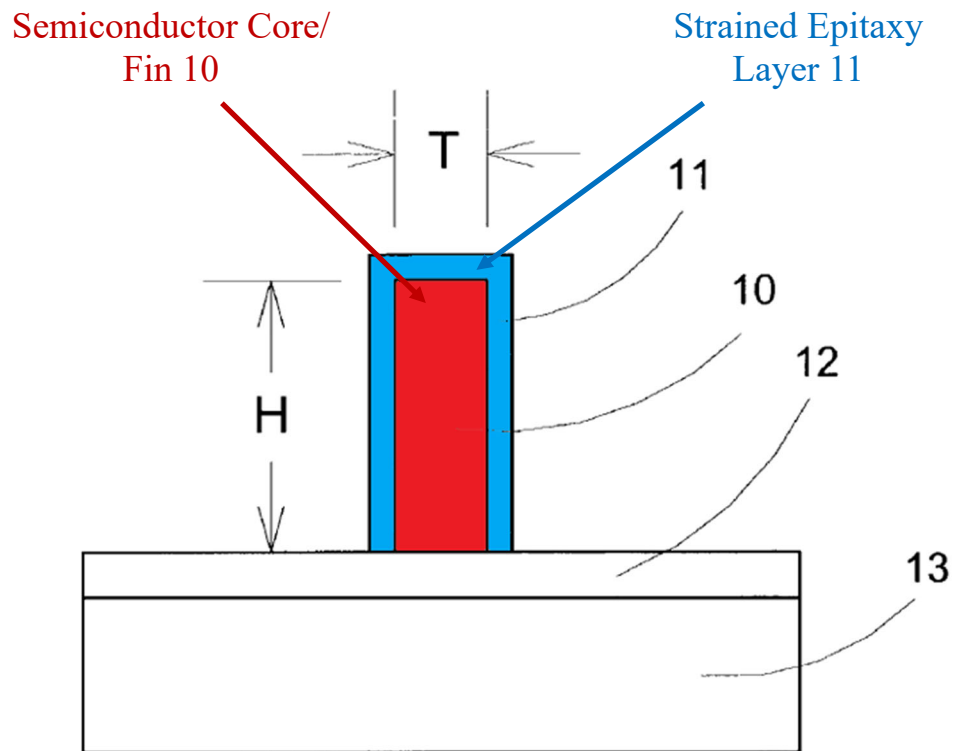


Figure 1

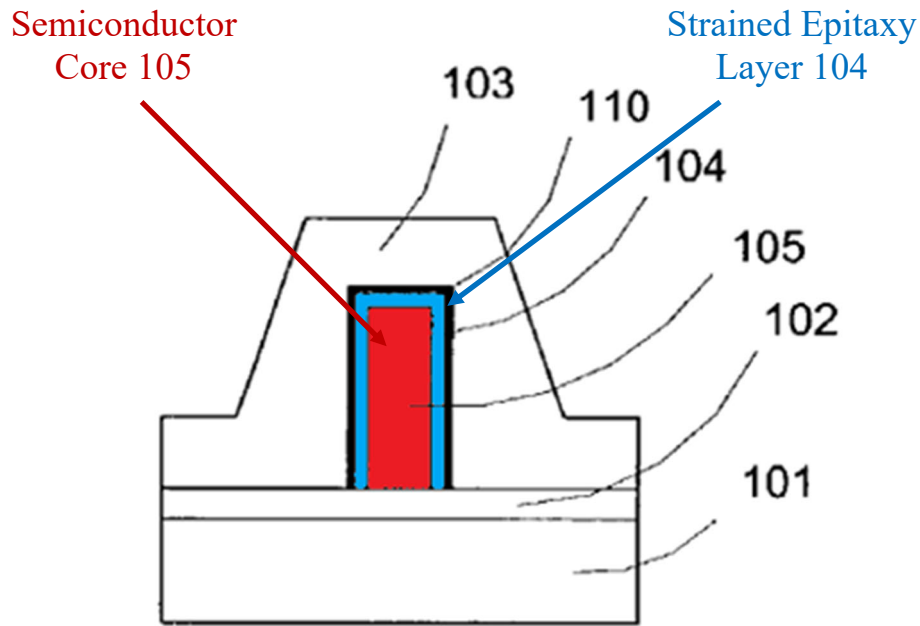


Figure 14

TSMC-1003, ¶105.

Regarding Figure 1, Lee describes a “strained silicon fin structure” that consists of a “*strained* channel *silicon* layer 11” which “covers a relaxed *silicon germanium*...seed fin 10.” TSMC-1004, 4:7-13. “Strained channel silicon layer 11” is an “epitaxial silicon layer” that is “grown on the seed fin 10.” TSMC-1004, 4:18-19; *see also id.*, 4:20-28, 6:58-7:7, Figs. 3b-3c; *supra*, §VIII(i)(1[a]).

Accordingly, the strained silicon layer of Lee’s Figure 1 is an epitaxy layer grown from the surface of the semiconductor seed fin/core. TSMC-1003, ¶106.

Similarly, regarding Figure 14, Lee describes a FinFET including “seed fin 105 and strained silicon channel 104, covering both sides and the top of the seed fin 105.” TSMC-1004, 12:34-37. “Strained silicon channel 104” is “selectively

grown on the seed fin 105,” (*id.*, 12:52-55), and includes “epitaxial silicon layer deposited on a relaxed silicon germanium seed fin” (*id.*, 11:32-38).

Thus, “silicon germanium...seed fin 10” or “seed fin 105” constitutes a “semiconductor core,” as claimed. TSMC-1003, ¶108. Additionally, “strained channel silicon layer 11” or “strained silicon channel 104” constitutes a “strained epitaxy layer grown from [the] surface of the semiconductor core,” as claimed. *Id.*

Further, Lee’s foregoing semiconductor cores (e.g., SiGe seed fins 10, 105) have a first lattice constant that mis-matches a second lattice constant of Lee’s strained epitaxy layers (e.g., strained channel silicon layer 11, strained silicon channel 104). *See* TSMC-1004, 3:49-67, 4:16-33, 8:16-8:52, 9:12-28, 11:24-38; TSMC-1003, ¶109. For example, Lee’s FinFET devices each have a “strained silicon fin structure [that] is fabricated by forming a silicon-containing epitaxial layer on a silicon-containing seed fin having [a] *different lattice constant.*” TSMC-1004, 3:51-54. As another example, Lee states that “seed fin 10 is a relaxed silicon germanium fin **having [a] lattice constant larger than the lattice constant of silicon**, therefore the epitaxial silicon layer 11 grown on the seed fin 10 will be tensilely strained.” *Id.*, 4:16-19; *see also id.*, 4:28-30, 6:35-42, 7:4-7.

Accordingly, Lee’s various FinFET devices meet limitation 6[a].

6[b] “Gate Strip”

Element 6[b] calls for “a gate strip wrapping a portion of said composite fin structure.” Lee discloses a gate strip (e.g., “gate 103”) wrapping a portion of its composite fin structure (e.g., “strained silicon fin structure,” “silicon fin channel,” “finFET channel”). *See* TSMC-1004, 12:21-48, 3:54-59, 13:17-42, 15:1-36, 16:34-36, Fig. 14; TSMC-1003, ¶111; *supra*, §VIII(i)(1[b]).

6[c] “Source/Drain Regions”

Element 6[c] specifies that “portions of said composite fin structure not covered by said gate strip constitute source/drain regions of said Tri-gate device,” which Lee discloses. TSMC-1003, ¶112.

For example, Lee discloses that portions of its composite fin structure not covered by said gate strip (e.g., “gate 103”) constitute source/drain regions (e.g., “source 106,” “drain 107”) of said Tri-gate device. *See* TSMC-1004, 3:54-56, 12:17-21, 13:17-42, Fig. 14; *supra*, §VIII(i)(1[c]).

6[d] “Gate Insulating Layer”

Element 6[d] calls for “a gate insulating layer interposed between said composite fin structure and said gate strip.” Lee discloses this element.

For example, Lee discloses a gate insulating layer (e.g., “gate dielectric 110”) interposed between said composite fin structure (e.g., “strained silicon fin structure,” “silicon fin channel,” “finFET channel”) and said gate strip (e.g., “gate

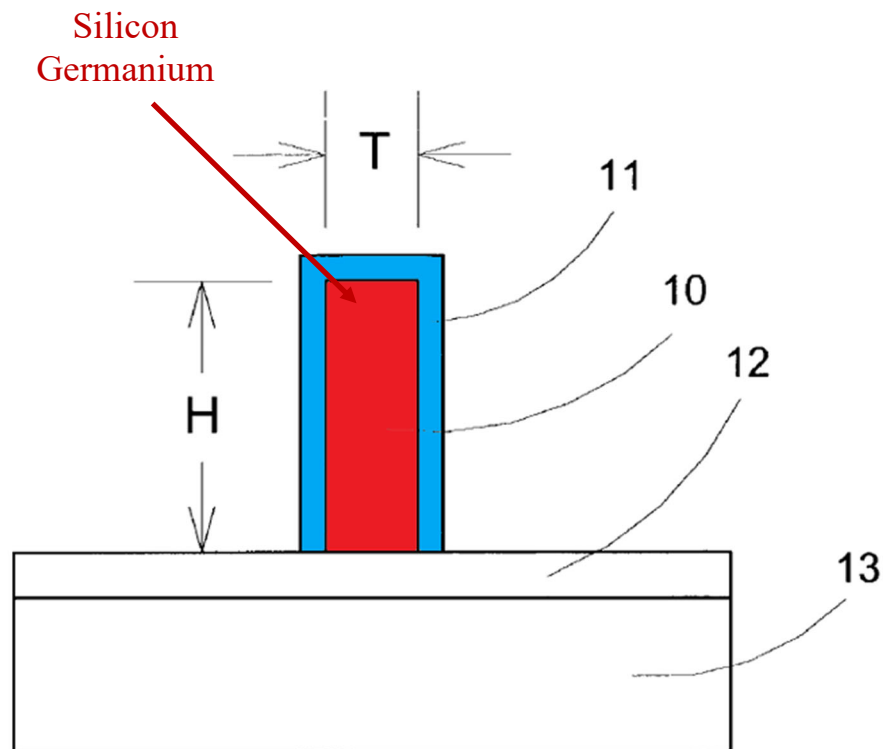
103”). See TSMC-1004, 3:49-59, 12:24-57, 13:33-40, Fig. 14; TSMC-1003, ¶113; *supra*, §VIII(i)(1[d]).

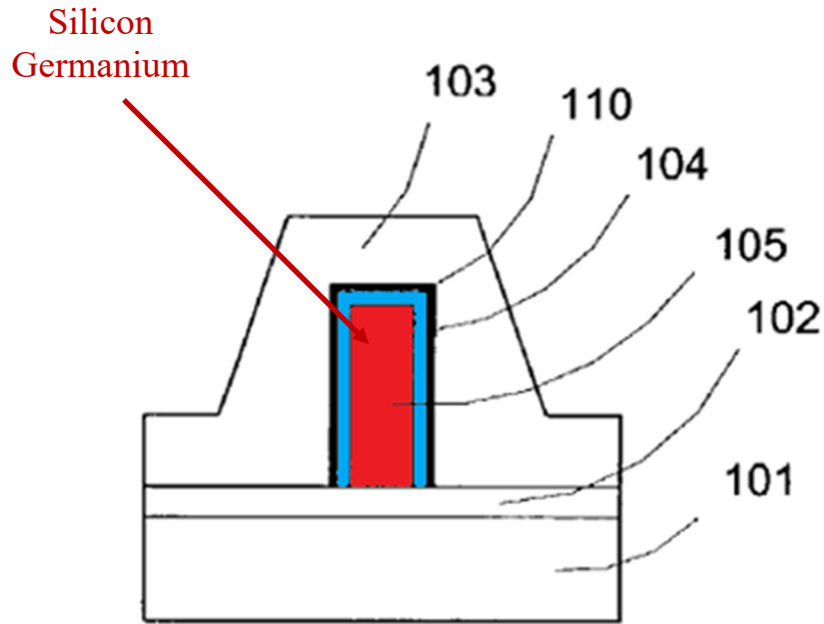
vii) Claim 7

[7] The Tri-gate device of claim 6 wherein said semiconductor core consists of silicon germanium.

Lee’s semiconductor core (e.g., seed fin 10, seed fin 105) consists of silicon germanium (e.g., “silicon germanium seed fin,” “silicon germanium seed fin 10”). See TSMC-1004, Abstract, 3:49-4:25, 11:31-38, 12:17-48, 16:8-39, Figs. 1, 3C, 14; TSMC-1003, ¶¶114-116.

Annotated Figures 1 and 14 depict Lee’s composite fin structure below depict silicon germanium seed fin 10/105:





TSMC-1003, ¶115.

Regarding Figure 1, Lee describes a “strained silicon fin structure” that consists of a “strained channel silicon layer 11” which “covers a relaxed *silicon germanium*...seed fin 10.” TSMC-1004, 4:7-13; *see also id.*, 11:32-38, 16:37-39.

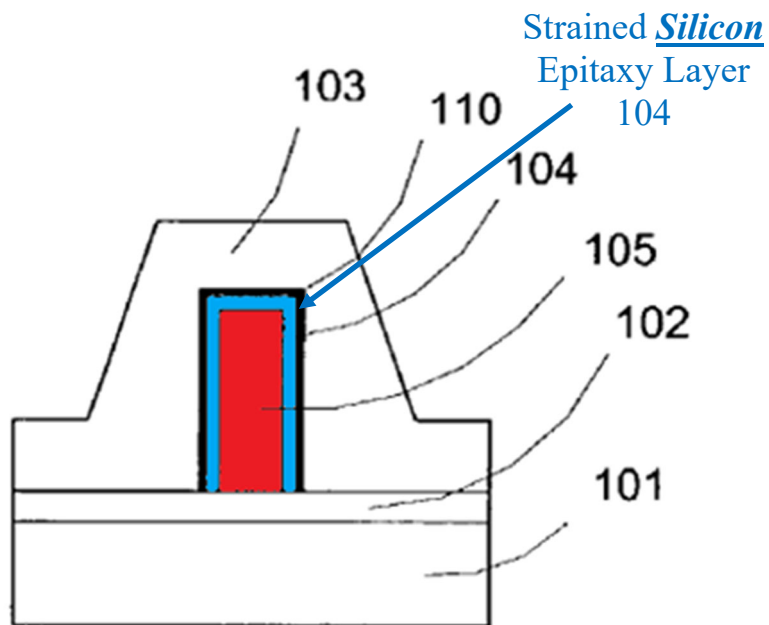
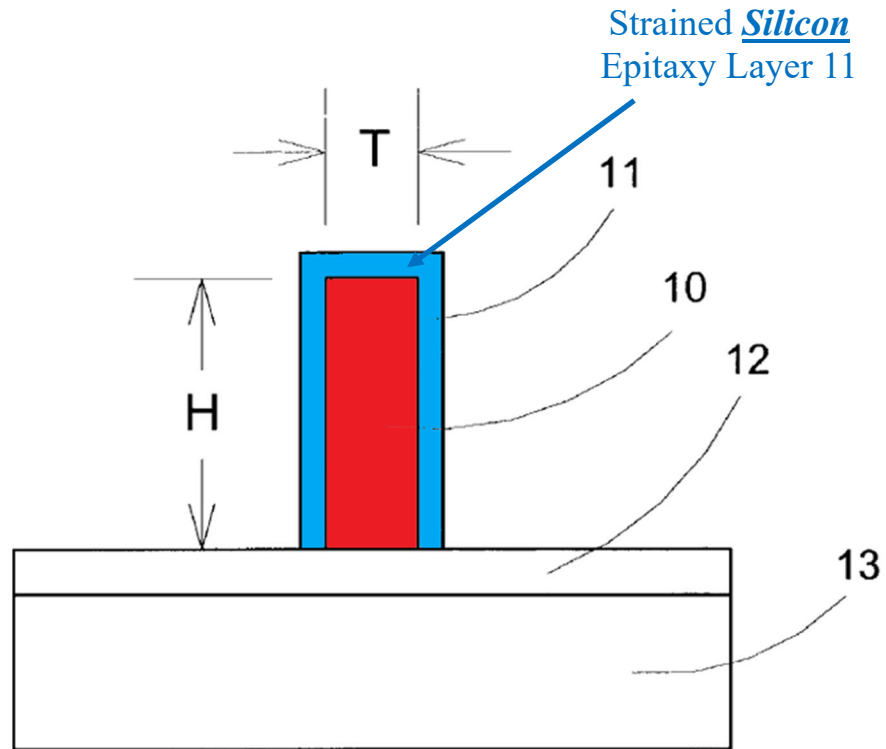
Lee thus meets claim 7.

viii) Claim 8

[8] The Tri-gate device of claim 6 wherein said strained epitaxy layer is a strained silicon epitaxy layer.

Lee’s strained epitaxy layer (e.g., “strained *silicon* layer,” “*silicon* layer 11,” “strained *silicon* channel 104”) is a strained *silicon* epitaxy layer. *See* TSMC-1004, Abstract, 3:49-4:30, 11:31-38, 12:17-48, 16:26-41, Figs. 1, 3C, 14; TSMC-1003, ¶¶117-121; *supra*, §VIII(i)(1[a]).

Annotated Figures 1 and 14 depict Lee's composite fin structure and its strained *silicon* epitaxy layer:



TSMC-1003, ¶118.

Regarding Figure 1, Lee describes a “strained **silicon** fin structure” that consists of a “**strained** channel **silicon** layer 11” which “covers a relaxed silicon germanium...seed fin 10.” TSMC-1004, 4:7-13; see also id., 4:18-19 (“**strained channel silicon** layer 11” is an “epitaxial **silicon** layer”), 4:20-28, 6:58-7:7, Figs. 3b-3c; *supra*, §VIII(i)(1[a])). Similarly, Lee’s Figure 14 FinFET includes “strained **silicon** channel 104.” TSMC-1004, 12:34-37, 11:32-38.

Accordingly, Lee satisfies claim 8.

ix) Claim 9

[9] The Tri-gate device of claim 8 wherein said strained silicon epitaxy layer has a thickness of about 50-300 angstroms.

The thickness of Lee’s strained silicon epitaxy layer ranges from 50-150 Ångstroms, (5-15 nm), which satisfies claim 9. *Supra*, §VIII(iv); TSMC-1004, 4:38-40; TSMC-1003, ¶122.

x) Claim 10

[10] The Tri-gate device of claim 6 wherein said gate strip is made of polysilicon or metal gate.

The “gate of [Lee’s] disclosed strained silicon finFET structure is preferably polysilicon, doped polysilicon or metal,” which satisfies claim 10. *Supra*, §VIII(v); TSMC-1004, 13:40-42, 15:10-36; TSMC-1003, ¶123.

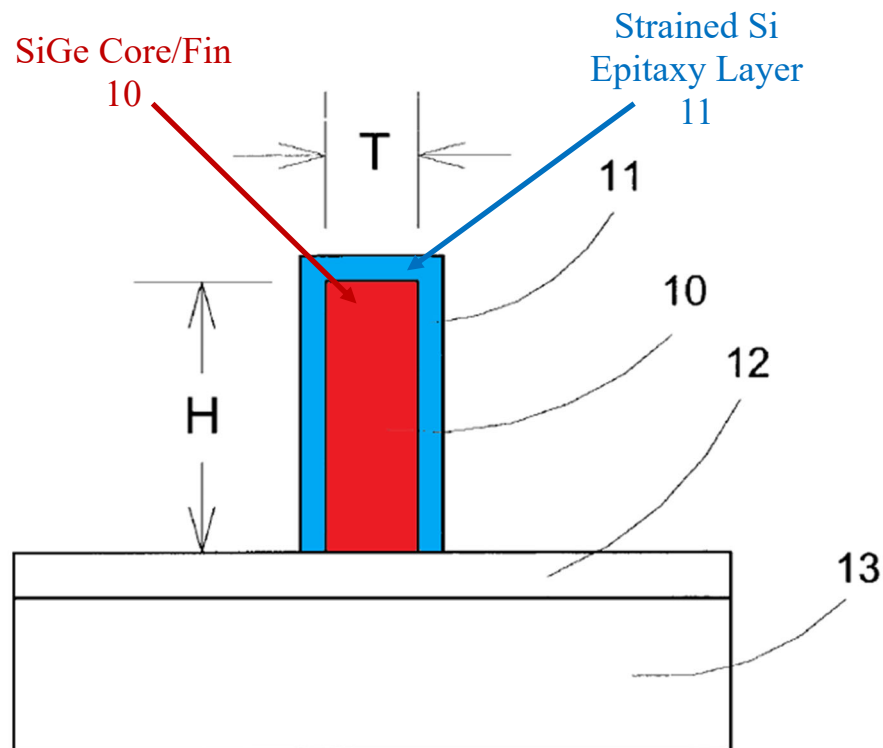
IX. GROUND 2: Lee and Chau render Claim 3 unpatentable

Claim 3 is obvious over Lee in view of Chau, as detailed below and in Dr. Braun's declaration (*see* TSMC-1003, §IX(B)).

i) Claim 3

As discussed above, Lee discloses dimensions for its composite fin structure wherein the width of said substantially flat top surface is equal to its height. *Supra*, §VIII(iii).

As depicted in Lee's Figure 1, SiGe fin 10 of composite fin structure 10/11 has a "height H" and a "thickness T" (or "width") (*id.*):

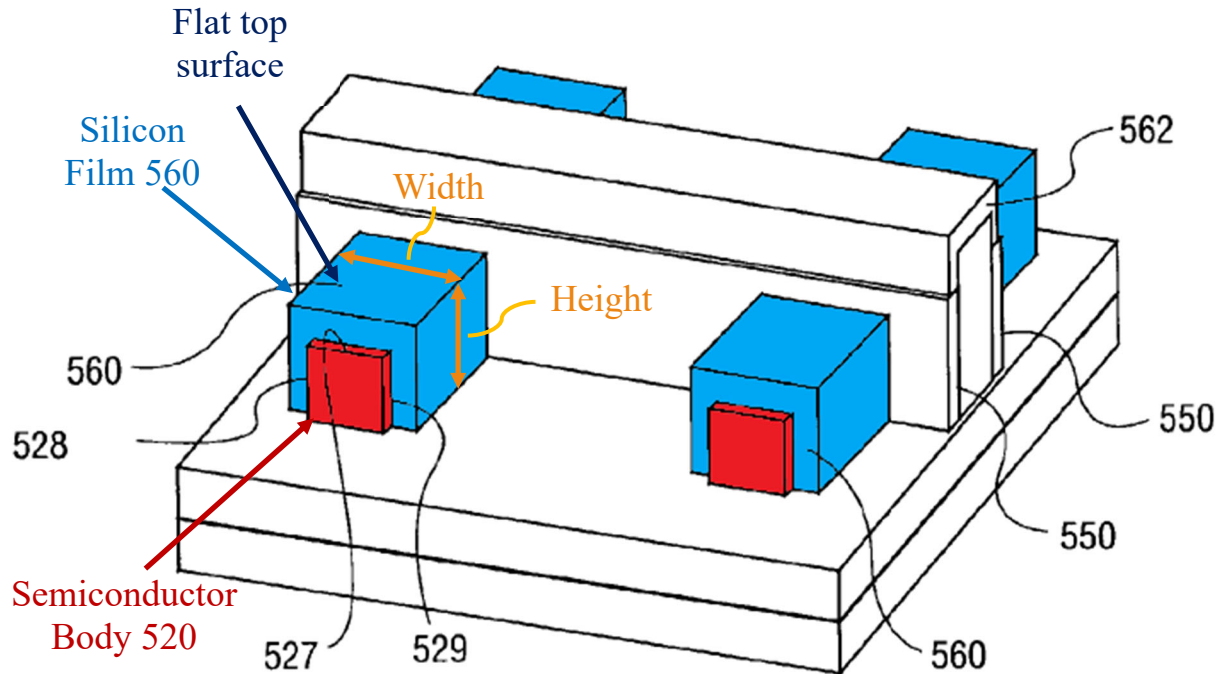


Lee further describes specific ranges for these dimensions (i.e., height H of 10-200 nm; thickness T of 5-100 nm) as well as the thickness of the “epitaxial silicon layer [11]” (i.e., 5-15 nm). *See* TSMC-1004, 4:36-40; *supra*, §VIII(iii). Lee thus discloses and/or renders obvious ranges that meet claim 3. *Supra*, §VIII(iii).

Further, it would also have been obvious to a POSITA in view of Chau to choose dimensions from Lee’s disclosed ranges such that Lee’s composite fin structure would have a width of its substantially flat top surface that is approximately equal to its height. TSMC-1003, ¶128.

The recited parameters in claim 3 are nothing more than workable ranges involving routine experimentation. Along with teaching range values that meet the recited parameters, as discussed in Lee, it was well-known to choose dimensions of a composite fin structure to “ensure fully depleted body under the operation conditions of the finFET device.” *See* TSMC-1004, 4:36-43.

Chau further teaches to vary the width and height dimensions of a composite fin to ensure full depletion, and discloses specific width and height dimension values. *See* TSMC-1007, ¶¶[0014], [0027], Fig. 6. Similar to Lee, Chau is directed to a “tri-gate fully depleted substrate transistor.” TSMC-1007, ¶[0002]. As depicted in annotated Figure 5H below, Chau’s tri-gate transistor includes a composite fin structure that consists of a “semiconductor film 560...formed on the exposed surfaces of semiconductor body 520” (*id.*, ¶[0048]):



TSMC-1003, ¶129. Semiconductor body 520 may be silicon germanium (TSMC-1007, ¶[0033]), and silicon film 560 may be an epitaxial silicon film (*id.*, ¶[0048]). The “width” of the flat top surface and the “height” of Chau’s composite fin structure are depicted in orange. The height of the composite fin structure (i.e., H_{CFS}) is equal to the height of the semiconductor body (i.e., H_{SB}) plus the thickness of the silicon film (i.e., T_{SF}), i.e., $H_{CFS} = H_{SB} + T_{SF}$. A POSITA viewing Chau’s Figure 5H would have interpreted the composite fin structure shown therein as having a substantially equal height and width as illustrated. TSMC-1003, ¶129.

Additionally, Chau’s Figure 6 depicts how the width and height dimensions of a seed fin (e.g., semiconductor body 520) could be varied to ensure full depletion. A POSITA would understand that selection of such dimensions may be

at least partially based on other characteristics of the device (such as gate length). TSMC-1003, ¶¶133-135; TSMC-1007, ¶[0027], Fig. 6. The plot lines of Chau's Figure 6 define boundaries between fully-depleted transistors (more desired) and partially-depleted transistors (less desired) for two gate lengths, where those boundaries correspond to specific body height and width dimensions. *See* TSMC-1007, ¶[0027]. As such, each plot line identifies specific threshold fin body height and width dimensions for a fully-depleted transistor at the respective gate lengths associated with the plot line:

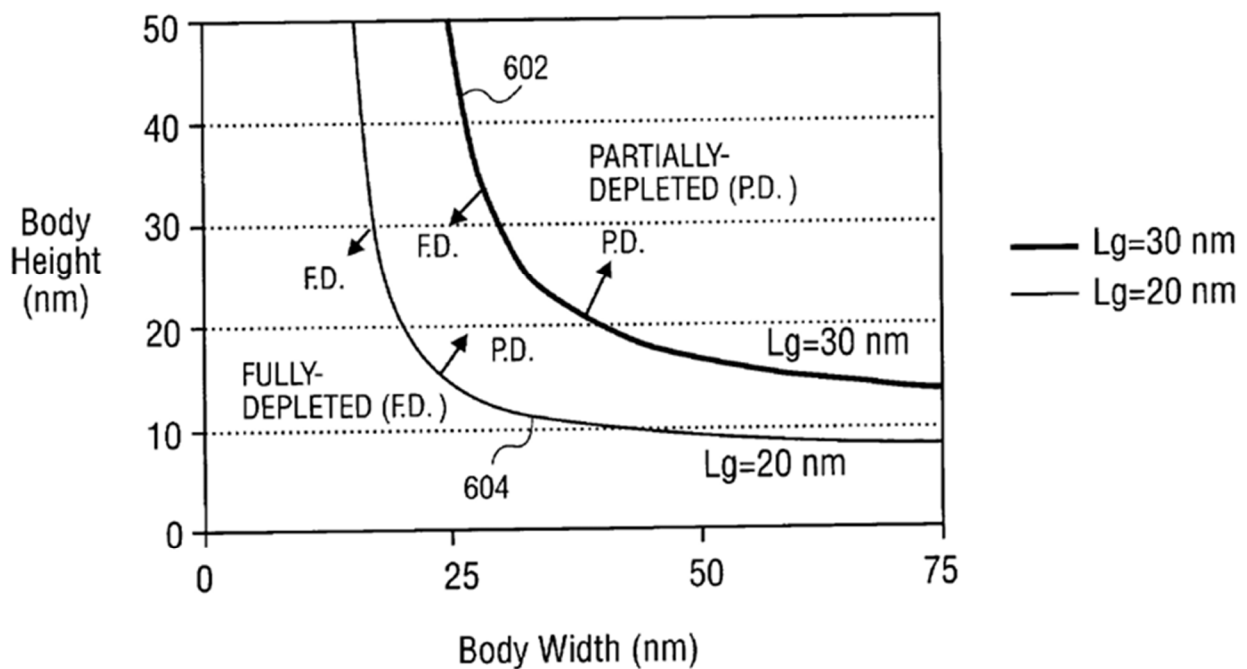


FIG. 6

As demonstrated by this graph, it was known that the height and width dimensions of a fin could be varied for a given gate length to ensure full depletion. TSMC-

1003, ¶134. A POSITA was motivated to use dimensions at the boundary between fully-depleted and partially-depleted zones (i.e., along plot lines 602, 604), because devices having the relatively larger dimensions along this boundary (as compared to further into the fully-depleted zone) are generally easier to manufacture and have a lower cost. *Id.*

The various height and width dimensions disclosed by Chau for achieving full depletion include dimensions that result in a composite fin structure having an equal height and width for a given epitaxial silicon film thickness. *Id.*, ¶¶135-138. Annotated Figure 6 below depicts specific points along its plot lines that correspond to example dimensions that, when a thickness of silicon film 562 is added thereto, result in a composite fin structure having a substantially equal width and height⁵:

⁵ The “body height” in Figure 6 is equivalent to the height of the semiconductor body 520, i.e., H_{SB} , and the “body width” is equivalent to the width of the semiconductor body, i.e., W_{SB} . TSMC-1003, ¶132.

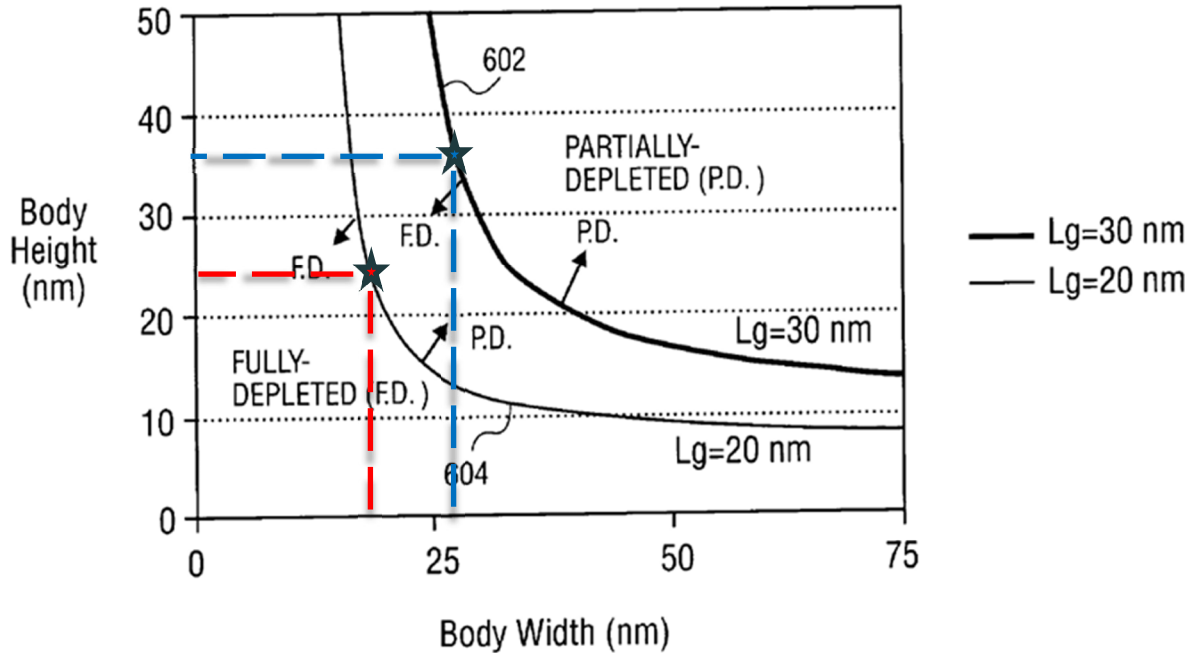


FIG. 6

TSMC-1003, ¶133.

The selected point (star at red line intersection) on plot line 604 has a body height (H_{SB}) of approximately 24 nm and a body width (W_{SB}) of approximately 19 nm. As noted above, the height and width of the associated composite fin structure (i.e., H_{CFS} , W_{CFS}) includes the thickness of the silicon film 560 (i.e., T_{SF}) (which Chau states is “formed to a thickness between **50**-500 [angstroms]” (i.e., **5**-50 nm)). TSMC-1007, ¶[0048].

Thus, combining Chau’s disclosed silicon film thickness of 5 nm with the disclosed height and width dimensions for the semiconductor body associated with plot line 604 (i.e., body height (H_{SB}) of approximately 24 nm and body width

(W_{SB}) of approximately 19 nm) gives a width of the composite fin structure that substantially equals its height. Specifically:

$$W_{CFS} = W_{SB} + 2 * T_{SF} = 19 \text{ nm} + 2 * 5 \text{ nm} = 29 \text{ nm}$$

$$H_{CFS} = H_{SB} + T_{SF} = 24 \text{ nm} + 5 \text{ nm} = 29 \text{ nm}.$$

TSMC-1003, ¶136. Similarly, the selected point (star at blue line intersection) on plot line 602 has a body height (H_{SB}) of approximately 37 nm and a body width (W_{SB}) of approximately 27 nm. An epitaxial silicon layer thickness of 10 nm (within Chau's range of 5-50 nm) results in both the total width and total height of the composite fin structure being 47 nm. *Id.*, ¶137. The height and width values of the semiconductor body and the thickness of the silicon film for each of these examples are within the ranges taught by Lee. *Id.*; TSMC-1004, 4:36-40 (disclosing seed fin height from 10-200 nm, seed fin width from 5-100 nm, and epitaxial silicon layer thickness from 5-15 nm).

Thus, Chau teaches a composite fin structure with a height approximately equal to the width of its substantially flat top surface. TSMC-1003, ¶138. It was thus apparent to a POSITA that dimensions for a seed fin and epitaxial silicon layer formed on the seed fin that result in a composite fin structure having a substantially equal width and height were obvious design options when seeking to create a fully depleted tri-gate transistor. As such, a POSITA would have found it obvious in view of Chau to use such dimensions in Lee's transistor device when optimizing

the device to ensure full depletion in addition to balancing other design considerations such as current carrying capacity, space limitations, cost, or manufacturing complexity. *Id.*, ¶139. Indeed, as discussed above, Lee expresses a desire to “ensure fully depleted body under the operation conditions of the finFET device” when selecting such dimensions. *See* TSMC-1003, 4:36-43. “Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” *Aller*, 220 F.2d at 456; *see also E.I. du Pont de Nemours*, 904 F.3d at 1006.

In short, it was obvious to utilize a composite fin structure having approximately equal width and height dimensions for Lee’s tri-gate device in view of Chau. TSMC-1003, ¶139. The specific width and height dimensions of the composite fin structure amount to a simple design choice based on well-known design considerations, including full depletion preference, as taught by both Lee and Chau. *Id.* Because equal height and width dimensions were well-known options and easily achievable given the overlapping height and width dimension ranges expressly disclosed by Lee, it was obvious to select approximately equal height and width dimensions for the resulting composite fin structure when designing and manufacturing the device. Additionally, as discussed previously, the approximately equal height and width dimensions of the claim composite fin

structure are not critical nor do they produce any unexpected results, and the '181 Patent does not provide any indication otherwise. *Supra*, §VIII(iii).

Motivation to Combine

A POSITA would have been motivated to use a composite fin structure having approximately equal width and height dimensions, such as taught by Chau, for several reasons. As discussed above, a POSITA would have been motivated to select such dimensions so that the resulting device operates properly when fully depleted, including with excellent short channel performance and optimized sub-threshold gradients. *See, e.g.*, TSMC-1004, 4:40-43 (“The optimized dimensions of the disclosed strained silicon fin structure are preferably chosen to ensure fully depleted body under the operation conditions of the finFET device.”); TSMC-1007, ¶[0005] (“Fully depleted SOI have been proposed as a transistor structure to take advantage of ideal sub-threshold gradients for optimized on current/off current ratios.”), ¶[0027] (“the [equal] body height, body width and gate length are chosen to have dimensions *in which a fully depleted transistor will be formed*”); TSMC-1013, Abstract (the “tri-gate device *remains fully depleted, with near-ideal subthreshold swing and excellent short channel characteristics....*”), 3 (“Three-dimensional simulations of the tri-gate transistor with $L_g = T_{Si} = W_{Si} = 30$ nm show that the *tri-gate device maintains full depletion at these dimensions, and exhibit excellent short channel performance....*”). As demonstrated above, Chau teaches

that FETs having a composite fin structure with approximately equal height and width dimensions achieve this goal by enabling a fully-depleted device with the associated improved performance characteristics, and thus a POSITA would have been motivated to use such a fin structure. TSMC-1003, ¶141.

Additionally, a POSITA would have been motivated to use a composite fin structure having approximately equal width and height dimensions to simplify device fabrication. *Id.*, ¶142. Traditional double-gate FinFET devices utilized high aspect ratio fins that become difficult to fabricate as the overall size of the FinFET device is shrunk due to the increasing narrowness of the fin relative to its height. TSMC-1012, 1 (“FinFET double-gate transistors have been offered for future transistor design, but...*the vertical nature of the device and the difficulties in fabricating such a device* suggest that the Tri-Gate might be the next transistor design.”). In contrast, the larger relative widths associated with the fins of triple-gate devices having approximately equal heights and widths facilitate easier manufacturing. *Id.*; *see also* TSMC-1013, Abstract (“[T]ri-gate devices also demonstrate full depletion at silicon body dimensions approximately 1.5-2 times greater than either single gate SOI or non-planar double-gate SOI for similar gate lengths, indicating that these devices are *easier to fabricate*...”). Additionally, Chau discusses a preference for avoiding “ultra-thin” fins due to the difficulty of manufacturing high aspect ratio structures. *See* TSMC-1007, ¶[0017]. Thus, a

POSITA was motivated to use a fin structure having approximately equal height and width to simplify device fabrication.

Reasonable Expectation of Success

A POSITA would have found implementing approximately equal height and width dimensions in composite fin structures to be routine and easily achievable at the time of the alleged invention, and thus would have had a reasonable expectation of success in doing so. TSMC-1003, ¶143; *supra*, §VIII(iii).

Accordingly, the combination of Lee and Chau renders claim 3 obvious.

X. GROUND 3: Sugiyama anticipates, or alternatively renders obvious, Claims 1-10

Sugiyama anticipates, or alternatively renders obvious, Claims 1-10, as detailed below and in Dr. Braun’s declaration (*see* TSMC-1003, §IX(C)).

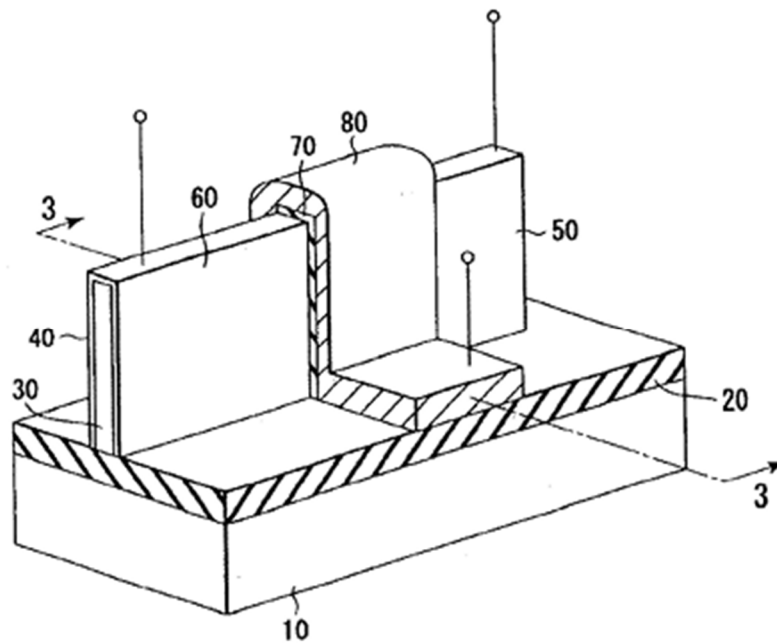
i) Claim 1

1[pre] “Three Dimensional Triple Gate (Tri-gate) Device”

To the extent the preamble is limiting, Sugiyama discloses a three dimensional Tri-gate device (e.g., “semiconductor device,” “MISFET”). TSMC-1005, Abstract, 6:63-7:10, 10:4-55, Figs. 2, 3B, 12B-14C; TSMC-1003, ¶¶145-149.

For example, Sugiyama discloses “a MISFET using, as a channel layer, a second semiconductor layer such as a strained Si layer which is joined to a first

semiconductor layer such as a SiGe crystal layer formed on an insulating layer, has a lattice constant different from that of the first semiconductor layer, and has a stress strain in crystal lattices.” TSMC-1005, 5:35-42. Sugiyama’s MISFET includes a “projecting SiGe layer (semiconductor board) 30,” a “strained Si layer (semiconductor layer) 40 [that] is formed on the side and upper surfaces of the SiGe layer 30,” and a “band-like gate electrode 80 [that] is so formed as to cover the vertical surfaces and horizontal upper surface of the strained Si layer 40.” *Id.*, 6:63-7:10. Figure 2 depicts such a MISFET:



Sugiyama’s “MISFET” is a “three dimensional triple gate device” because of the three-dimensional semiconductor board 30/strained layer 40 (i.e., a composite fin structure) and a gate electrode that covers three surfaces of the semiconductor board 30/strained layer 40 (i.e., both side surfaces and the top

surface). TSMC-1003, ¶148; *see* TSMC-1005, 6:63-7:10, Figs. 2, 3B, 12B; *see also* TSMC-1004, 12:26-30 (“The double gate 103 *is actually a triple gate because it covers both sides and the top of the strained silicon channel* 104.”).

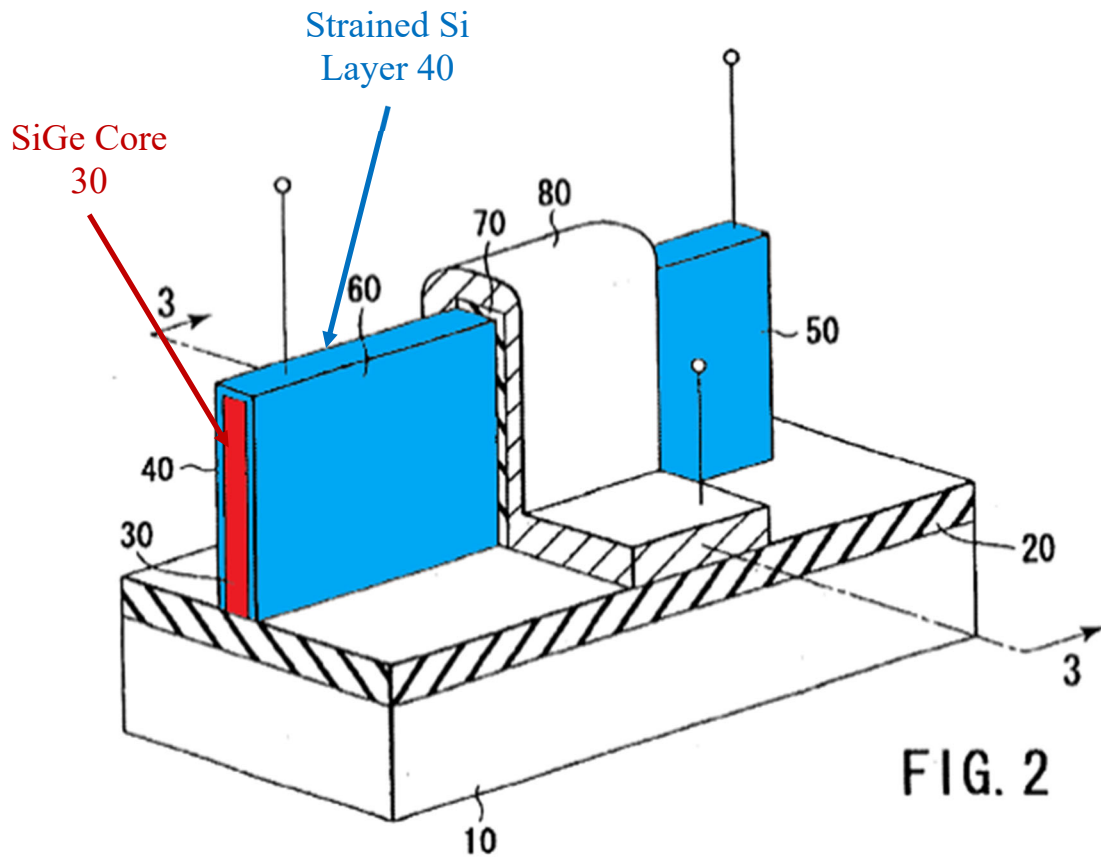
Accordingly, Sugiyama’s MISFET devices meet the preamble of claim 1.

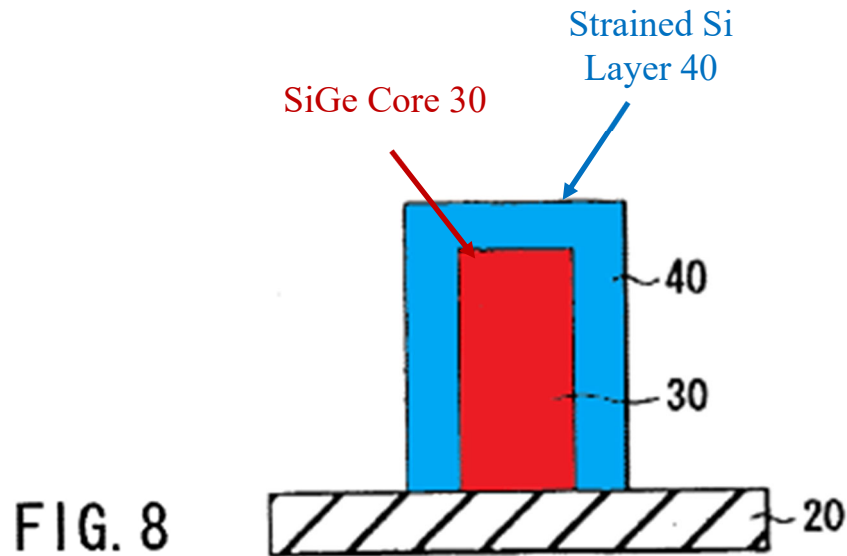
1[a] “Composite Fin Structure”

Element 1[a] calls for “a composite fin structure consisting of a silicon germanium core and a strained silicon epitaxy layer grown from surface of said silicon germanium core.” Sugiyama discloses this element. TSMC-1003, ¶¶150-153.

For example, Sugiyama’s MISFET devices include a composite fin structure consisting of: (i) a silicon germanium core (e.g., “SiGe layer (semiconductor board) 30”) and (ii) a strained silicon epitaxy layer (e.g., “strained Si layer (semiconductor layer) 40”) grown from the surface of the silicon germanium core. *See* TSMC-1005, Abstract, 5:35-42 (“The present invention...relates to a MISFET using, *as a channel layer, a second semiconductor layer such as a strained Si layer which is joined to a first semiconductor layer such as a SiGe crystal layer* formed on an insulating layer....”); *see also id.*, 5:55-61, 6:63-7:10, Figs. 2, 3B, 8; TSMC-1003, ¶150.

with annotations highlighting its constituent layers (i.e., silicon germanium core 30 in red and strained silicon layer 40 in blue):





TSMC-1003, ¶151.

Regarding Figures 2 and 8 (which use common reference numbers for the same components, TSMC-1005, 7:64-67), Sugiyama describes a “projecting *SiGe layer* (semiconductor board) 30 [that] is formed on the insulating layer 20” and a “*strained Si layer* (semiconductor layer) 40 [that] is formed *on the side and upper surfaces* of the SiGe layer 30 so as to cover this SiGe layer 30.” TSMC-1005, 6:65-7:3. Strained Si layer 40 is “grown” on “the surface of the SiGe crystal layer 30 *by epitaxial growth*.” *Id.*, 9:46-47; *see also id.*, 5:18-19, Figs. 2, 8.

Accordingly, Sugiyama’s strained silicon layer 40 is an epitaxy layer grown from the surface of silicon germanium core 30. TSMC-1003, ¶152.

Accordingly, Sugiyama’s MISFET devices satisfying limitation 1[a].

1[b] “Gate Strip”

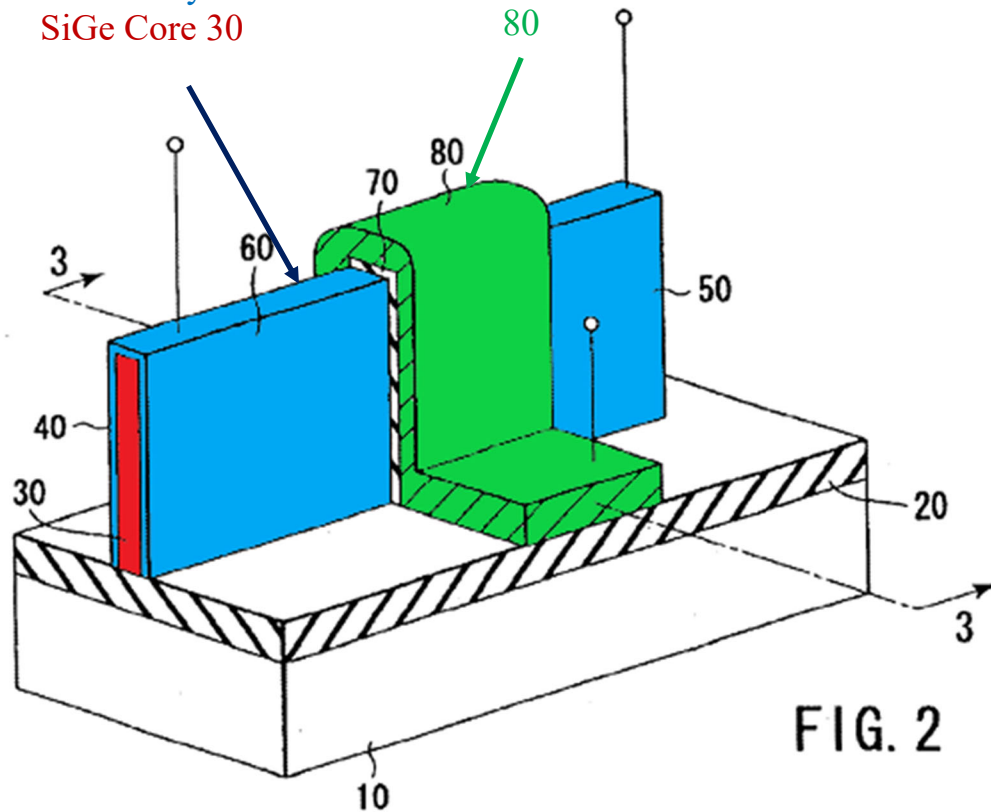
Element 1[b] requires “a gate strip wrapping a portion of said composite fin structure,” which Sugiyama discloses. TSMC-1003, ¶¶154-156.

For example, Sugiyama discloses a gate strip, e.g., “gate electrode 80,” wrapping a portion of said composite fin structure. TSMC-1005, 7:8-10 (a “*band-like gate electrode 80* is so formed as to cover *the vertical surfaces and horizontal upper surface* of the strained Si layer 40 via a gate insulating layer 70.”), Figs. 2, 3B; TSMC-1003, ¶154. Sugiyama further states that, “[i]n *forming a gate on the second semiconductor layer*, the gate is formed such that the area of a channel portion in the surface of the second semiconductor layer is set smaller than the junction area between the SiGe layer and the insulating layer.”). *Id.*, 5:44-51.

Annotated Figure 2 is shown below, depicting Sugiyama’s gate electrode 80 (in green) wrapping a portion of the composite fin structure (i.e., the combination of strained silicon layer 40 and silicon germanium layer 30) on the vertical surfaces and the upper horizontal surface of the composite fin structure, where some portions of the composite fin structure are covered and other portions remain uncovered:

Composite Fin Structure =
Strained Si Layer 40 +
SiGe Core 30

Gate Electrode
80



TSMC-1003, ¶155.

Accordingly, Sugiyama’s “gate electrode 80” constitutes a gate strip that wraps a portion of the combined strained silicon layer 40/silicon germanium layer 30 (i.e., the “composite fin structure”), satisfying this limitation.

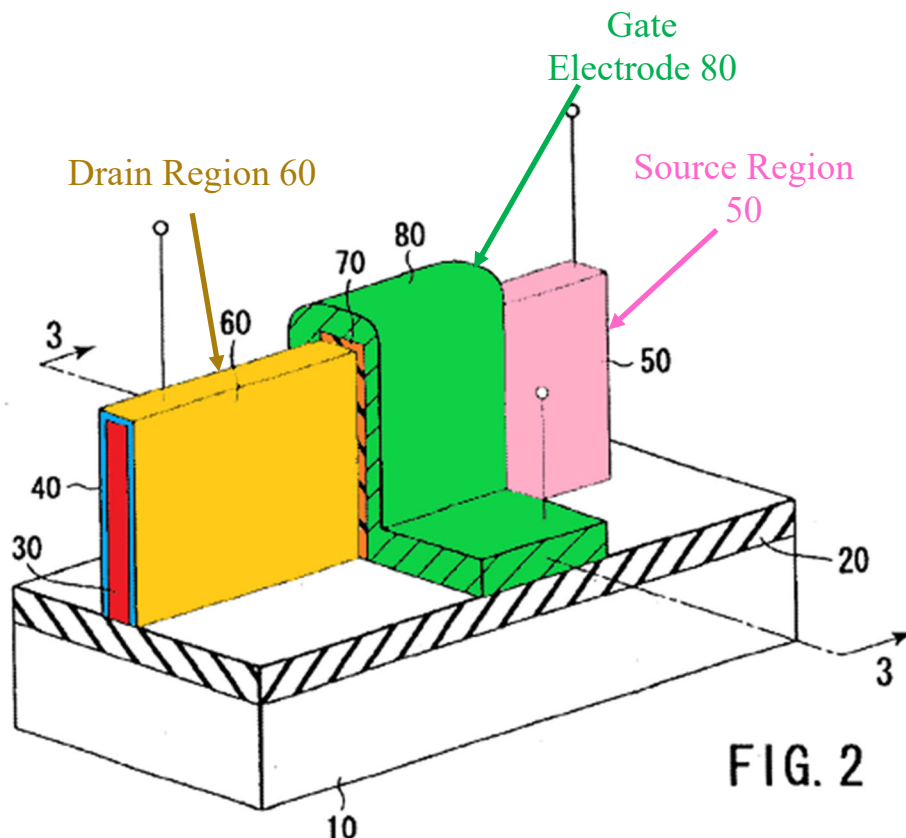
1[c] “Source/Drain Regions”

Element 1[c] specifies that “portions of said composite fin structure not covered by said gate strip constitute source/drain regions of said Tri-gate device.”

Sugiyama discloses this element. TSMC-1003, ¶¶157-158.

For example, portions of Sugiyama's composite fin structure (e.g., combination of "SiGe layer 30" and "strained Si layer 40") not covered by said gate strip (e.g., "gate electrode 80") constitute source/drain regions (e.g., "source region 50," "drain region 60") of said Tri-gate device. See TSMC-1005, 7:10-17, Fig. 2; TSMC-1003, ¶157. Indeed, Sugiyama states that "[t]hose *portions of the strained Si layer 40 that are not covered with the gate insulating layer 70 and gate electrode 80* serve as a *source region 50 and drain region 60.*" *Id.*, 7:10-13.

Sugiyama's Figure 2 is reproduced and annotated below depicting the portions of the composite fin structure not covered by gate electrode 80, which constitute the source region 50 (in pink) and drain region 60 (in gold):



TSMC-1003, ¶157; *see also* TSMC-1005, 7:14-17.

Accordingly, the composite fin structures of Sugiyama's MISFET devices include portions not covered by gate electrode 80 that constitute source/drain regions 50/60 of the tri-gate device, thereby satisfying this limitation.

1[d] “Gate Insulating Layer”

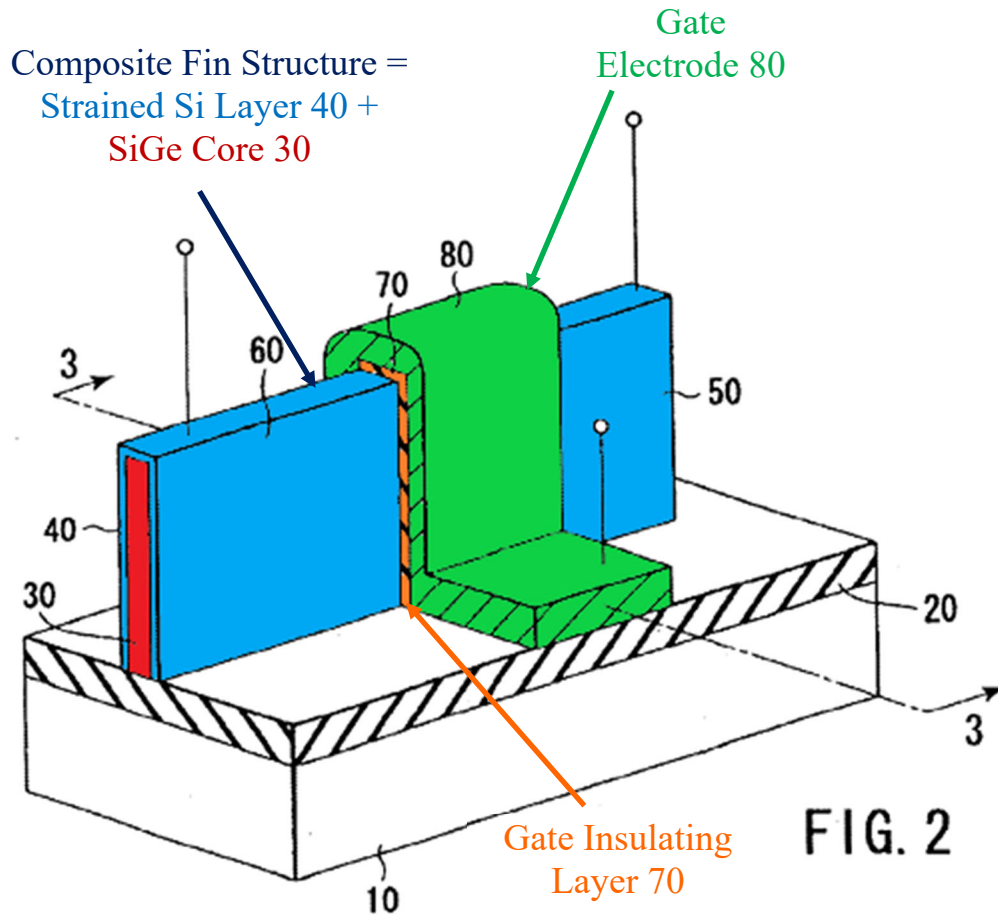
Element 1[d] calls for “a gate insulating layer interposed between said composite fin structure and said gate strip.” Sugiyama discloses this element.

TSMC-1003, ¶¶159-162.

Specifically, Sugiyama discloses a gate insulating layer (e.g., “gate insulating layer 70”) interposed between said composite fin structure (e.g., combination of “SiGe layer 30” and “strained Si layer 40”) and said gate strip (e.g., “gate electrode 80”). *See* TSMC-1005, 7:8-21, 10:4-45, Figs. 2, 13B-14C; TSMC-1003, ¶159.

Sugiyama's “band-like gate electrode 80 is so formed as to cover the vertical surfaces and horizontal upper surface of the strained Si layer 40 *via a gate insulating layer 70.*” TSMC-1005, 7:8-10, 10:4-20; TSMC-1003, ¶160.

Annotated Figure 2 depicts gate insulating layer 70 interposed between Sugiyama's composite fin structure (i.e., the combination of SiGe layer 30 and strained Si layer 40) and gate strip (i.e., “gate electrode 80”) (TSMC-1003, ¶161):



Accordingly, Sugiyama's gate insulating layer 70 constitutes the claimed "gate insulating layer," satisfying this limitation.

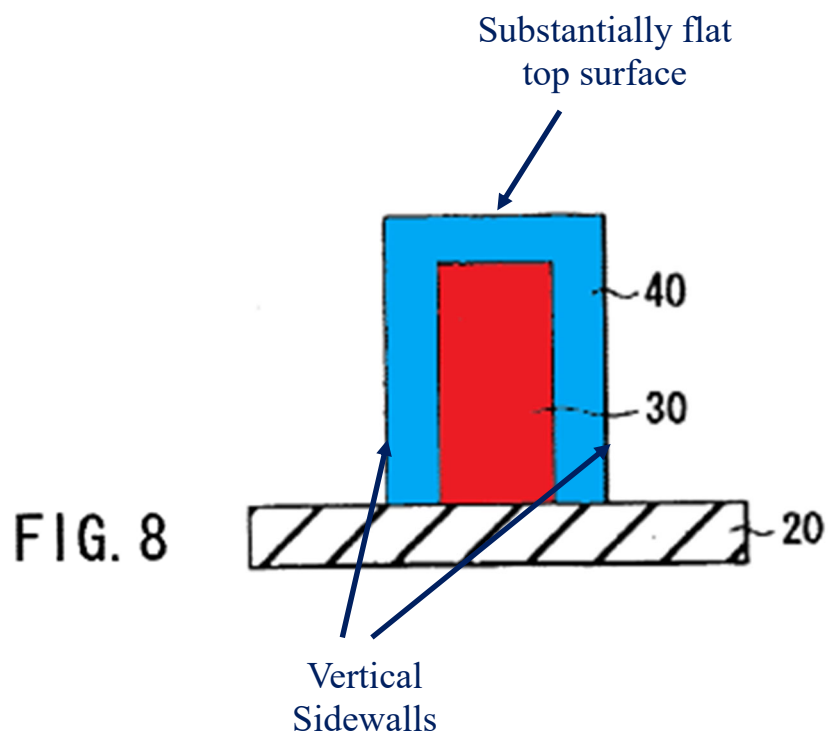
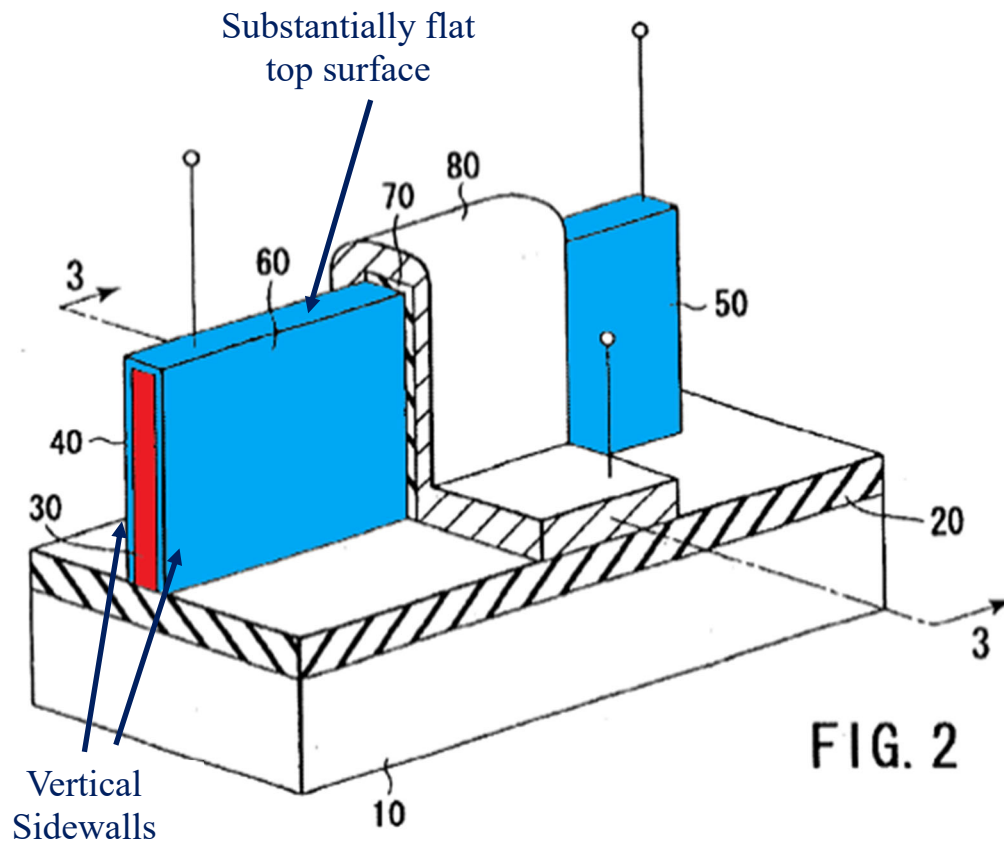
Sugiyama thus discloses all limitations of claim 1, thereby anticipating claim 1.

ii) Claim 2

Claim 2 recites that said composite fin structure has a substantially flat top surface and vertical sidewalls, which Sugiyama discloses. TSMC-1003, ¶¶164-166.

Sugiyama's composite fin structure (e.g., combination of "SiGe layer 30" and "strained Si layer 40") has a substantially flat top surface and vertical sidewalls. *See* TSMC-1005, 6:63-7:10, 7:4-10, Figs. 1, 2, 3C, 8, 10C; TSMC-1003, ¶164. For example, strained silicon layer 40 (which forms the outer layer of Sugiyama's composite fin structure) has a "horizontal upper surface" and "vertical surfaces," which correspond to the claimed "substantially flat top surface" and "vertical sidewalls" of the composite fin structure, respectively. *See* TSMC-1005, 7:4-10 ("The strained Si layer 40 may be continuously formed on the vertical surfaces in parallel to each other and horizontal upper surface, as shown in FIG. 2. A band-like gate electrode 80 is so formed as to cover the *vertical surfaces and horizontal upper surface* of the strained Si layer 40 via a gate insulating layer 70."); TSMC-1003, ¶165.

Annotated Figures 2 and 8 depict the substantially flat top surface and vertical sidewalls of Sugiyama's composite fin structure (TSMC-1003, ¶165):

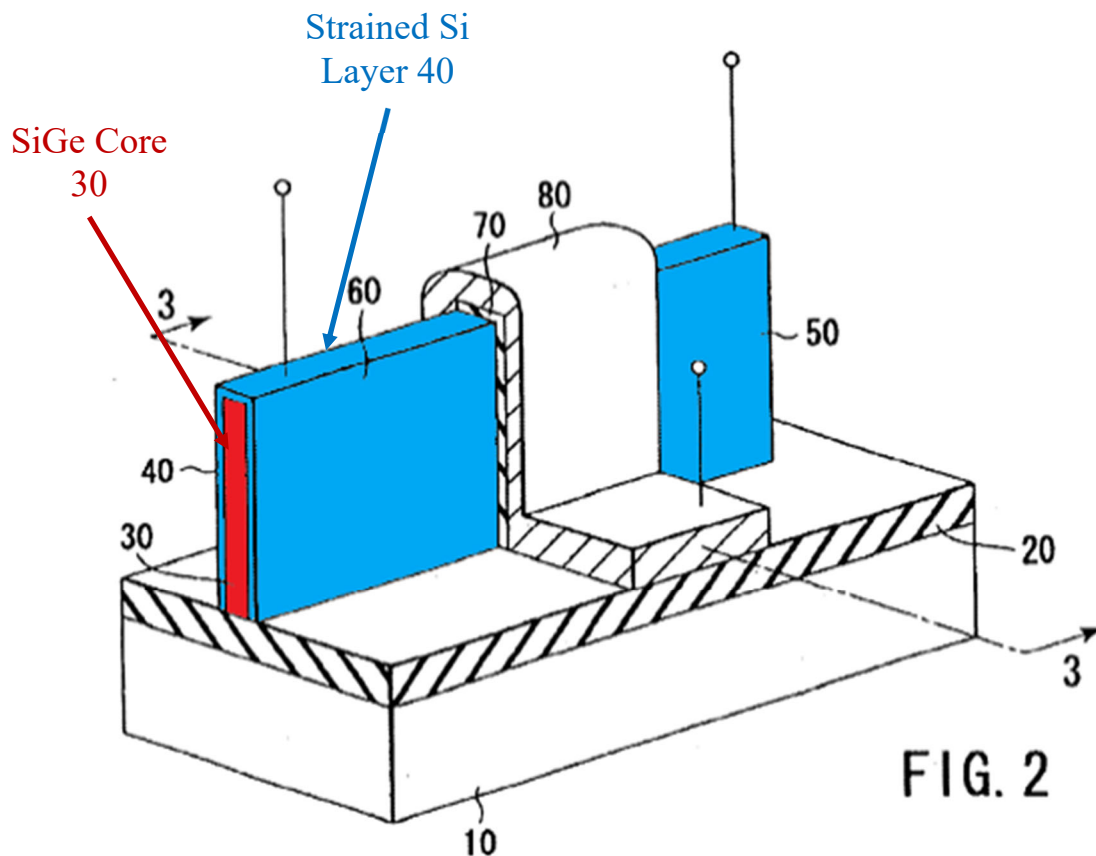


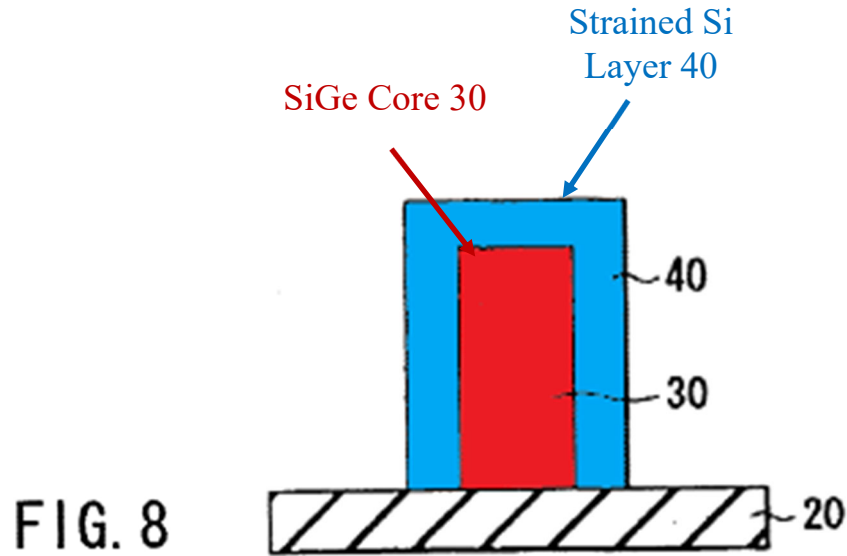
Accordingly, Sugiyama satisfies claim 2.

iii) Claim 3

Claim 3 recites that said composite fin structure has a width of said substantially flat top surface that is approximately equal to its height, which Sugiyama discloses. TSMC-1003, ¶¶167-173.

As described above (*supra*, §X(i)(1[a])) and shown in annotated Figures 2 and 8, Sugiyama's composite fin structure consists of a combination of SiGe layer 30 and strained Si layer 40 (TSMC-1003, ¶169):





As understood from Figures 2 and 8, the height of the top surface of Sugiyama's composite fin structure (i.e., H_{CFS}) is equal to the height of SiGe layer 30 (i.e., H_{SG}) plus the width/thickness of strained Si layer 40 (i.e., T_{SiL})—
 $H_{CFS} = H_{SG} + T_{SiL}$. TSMC-1003, ¶170. The width of the top surface of Sugiyama's composite fin structure (i.e., W_{CFS}) is equal to the width/thickness of SiGe layer 30 (i.e., T_{SG}) plus two times the thickness of strained Si layer 40 (i.e., T_{SiL})—
 $W_{CFS} = T_{SG} + 2 * T_{SiL}$. *Id.*

Sugiyama teaches an embodiment where SiGe layer 30 has a “height W” of “50 nm or more” and a “width d” that is “desirably 10 nm (inclusive) to 50 nm (inclusive).” TSMC-1005, 9:30-40. Sugiyama's strained Si layer 40 has a thickness that “is desirably 5 nm (inclusive) to 30 nm (inclusive).” *Id.*, 9:49-50.

Thus, taking an example where the SiGe layer 30 has a height of 50 nm and a width of 45 nm, and the strained silicon epitaxial layer 40 has a thickness of 5 nm, yields a composite fin structure having an equal height and width of 55 nm:

$$H_{\text{CFS}} = 50 \text{ nm} + 5 \text{ nm} = 55 \text{ nm}$$

$$W_{\text{CFS}} = 45 \text{ nm} + 2*(5 \text{ nm}) = 55 \text{ nm}.$$

TSMC-1003, ¶171. Similarly, applying the endpoints of “height W” of the SiGe layer of 50 nm and the “width d”/thickness of 50 nm, and employing a strained Si layer of 5 nm, results in $H_{\text{CFS}} = 50 \text{ nm} + 5 \text{ nm} = 55 \text{ nm}$; $W_{\text{CFS}} = 50 \text{ nm} + 2*(5 \text{ nm}) = 60 \text{ nm}$, giving a H:W ratio of 0.92, which a POSITA would understand to be approximately equal to 1. *Id.*, ¶172.

For the same reasons as discussed above with respect to Lee, Sugiyama anticipates or, alternatively, renders obvious claim 3. *Supra*, §VIII(iii). Indeed, there is no evidence in either the '181 Patent or Sugiyama that a composite fin structure with equal height and width dimensions would operate significantly differently than a composite fin structure having other height and width dimensions from within the ranges of Sugiyama. TSMC-1003, ¶174. Additionally, equal height and width dimensions are not critical, and are at best optimizable parameters that may be varied in a known manner in accordance with design considerations. *Id.* A POSITA would have found implementing approximately equal height and

width dimensions in Sugiyama's composite fin structures to have had a reasonable expectation of success for the same reasons discussed for Lee. *Id.*

Accordingly, Sugiyama discloses, or alternatively renders obvious, claim 3.

iv) Claim 4

Claim 4 requires a strained silicon epitaxy layer about 50-300 Ångstroms thick. Sugiyama teaches a strained silicon epitaxy layer (e.g., "strained Si layer 40") having a thickness that "is desirably 5 nm (inclusive) to 30 nm (inclusive)." TSMC-1005, 9:49-50; *see also id.*, 10:8-9. Because 5-30 nanometers equals 50-300 Ångstroms, Sugiyama discloses claim 4. TSMC-1003, ¶175.

v) Claim 5

Claim 5 recites that said gate strip is made of polysilicon or metal gate. Sugiyama discloses this element. TSMC-1003, ¶176.

Sugiyama's "gate electrode 80" is made from "polysilicon." TSMC-1005, 10:9-20 ("***Poly-Si*** is deposited to a thickness of 200 nm on the entire surface of a second insulating layer 24 by CVD, forming a conductive layer 25 as a gate electrode.... As a result, as shown in FIG. 11A, a band-like gate electrode 80 is formed...."); TSMC-1003, ¶176. Thus, poly-Si is deposited to form conductive layer 25 as a gate electrode, and following patterning of the conductive layer 25, the band-like gate electrode 80 is formed. *Id.* The same gate electrode 80 is shown in Figure 2 (for first embodiment) and Figures 9-14 (for second

embodiment). *See id.*, 7:64-67 (noting that common reference numbers are used for the same components in the first and second embodiments). Thus, the gate electrode 80 disclosed in the first and second embodiments of Sugiyama may be polysilicon, satisfying claim 5.

vi) Claim 6

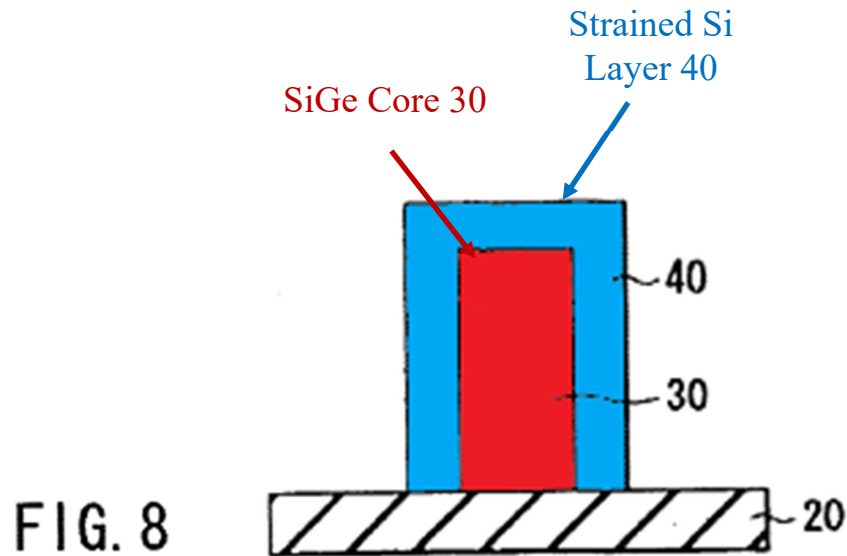
6[pre] “Tri-gate Device”

Sugiyama discloses a Tri-gate device. *Supra*, §X(i)(1[pre]); *see* TSMC-1005, Abstract, 6:63-7:10, 10:4-55, Figs. 2, 3B, 12B-14C; TSMC-1003, ¶178.

6[a] “Composite Fin Structure”

Element 6[a] calls for “a composite fin structure consisting of a semiconductor core and a strained epitaxy layer grown from surface of said semiconductor core, said semiconductor core having a first lattice constant that miss-matches a second lattice constant of said strained epitaxy layer.” Sugiyama discloses this element. TSMC-1003, ¶¶179-183.

For example, Sugiyama’s MISFET device includes a composite fin structure consisting of: i) a semiconductor core (e.g., “SiGe layer (semiconductor board) 30”); and ii) a strained epitaxy layer (e.g., “strained Si layer (semiconductor layer) 40”) grown from the surface of the semiconductor core. *See* TSMC-1005, Abstract, 5:35-42 (“The present invention...relates to a MISFET using, *as a channel layer, a second semiconductor layer such as a strained Si layer which is*



TSMC-1003, ¶180.

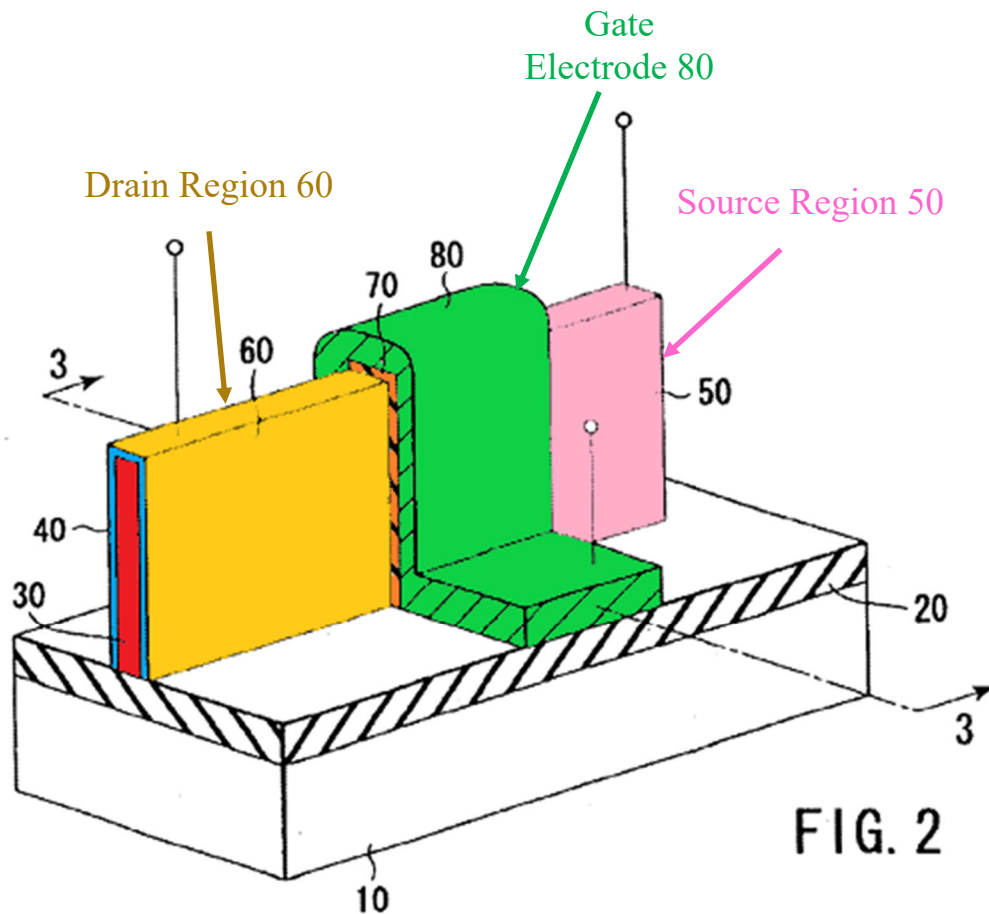
In particular, Sugiyama describes a “projecting *SiGe layer* (semiconductor board) 30 [that] is formed on the insulating layer 20” and a “*strained Si layer* (semiconductor layer) 40 [that] is formed on the side and upper surfaces of the SiGe layer 30 so as to cover this SiGe layer 30.” TSMC-1005, 6:65-7:3.

“Strained Si layer 40” is “grown” on “the surface of the SiGe crystal layer 30 *by epitaxial growth.*” *Id.*, 9:46-47; *see also id.*, 5:18-19, Figs. 2, 8. Accordingly, Sugiyama’s strained silicon layer 40 is an epitaxy layer grown from the SiGe semiconductor core 30. TSMC-1003, ¶181.

Additionally, Sugiyama’s semiconductor core (e.g., SiGe layer 30) has a first lattice constant that mis-matches a second lattice constant of Sugiyama’s strained epitaxy layer (e.g., strained Si layer 40). *See* TSMC-1005, 1:33-40 (“MISFET using a semiconductor substrate in which a *SiGe crystal layer slightly larger in*

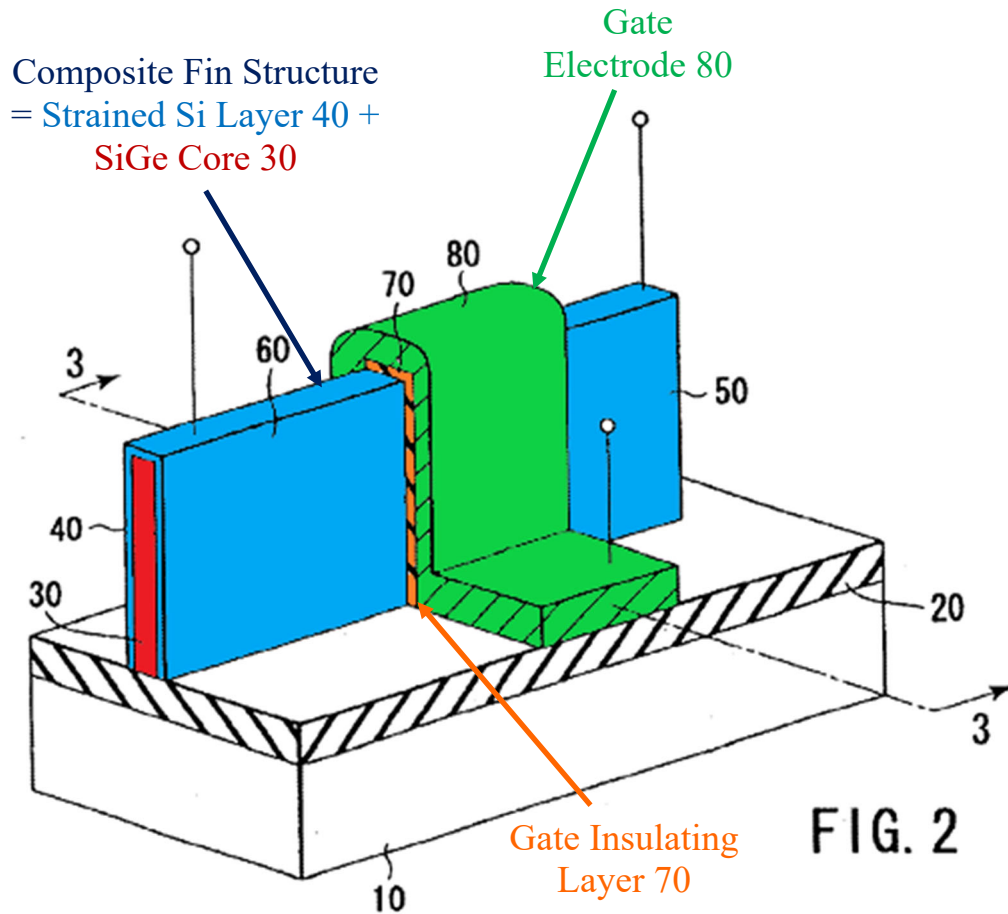
6[c] “Source/Drain Regions”

Element 6[c] specifies that “portions of said composite fin structure not covered by said gate strip constitute source/drain regions of said Tri-gate device,” which Sugiyama discloses. *Supra*, §X(i)(1[c]); TSMC-1005, 7:10-17, Fig. 2; TSMC-1003, ¶185.



6[d] “Gate Insulating Layer”

Element 6[d] calls for “a gate insulating layer interposed between said composite fin structure and said gate strip,” which Sugiyama discloses. *Supra*, §X(i)(1[d]); TSMC-1005, 7:8-31, 10:4-45, Figs. 2, 13B-14C; TSMC-1003, ¶186.

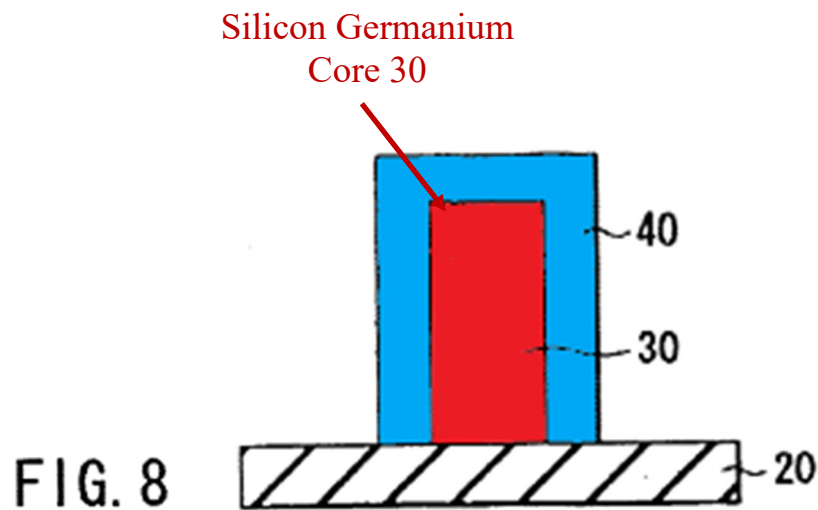
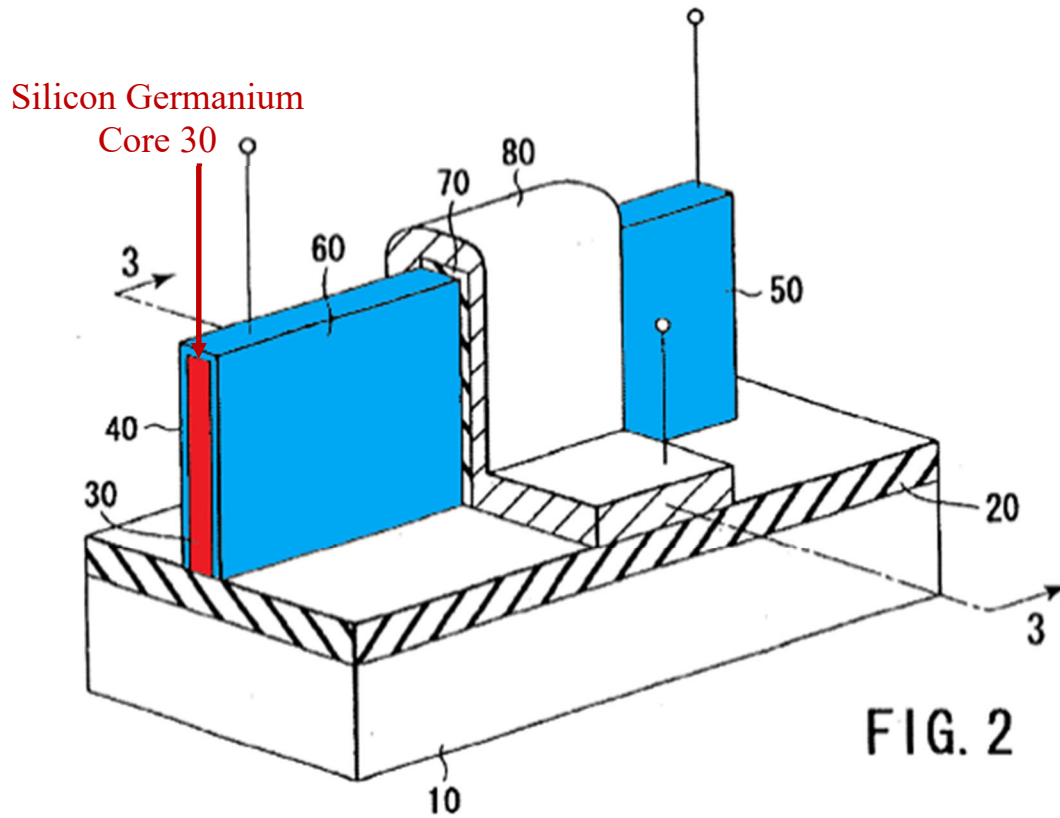


vii) Claim 7

Sugiyama’s semiconductor core (e.g., *SiGe* core 30) consists of silicon germanium, satisfying claim 7. TSMC-1005, Abstract, 5:55-61 (“*the first*

semiconductor layer is formed from a SiGe crystal layer....”), 5:35-42, 6:63-7:10,

Figs. 2, 3B, 8; TSMC-1003, ¶187; *supra*, §X(i)(1[a]).



viii) Claim 8

Claim 8 recites that the strained epitaxy layer is a strained silicon epitaxy layer. Sugiyama's MISFET device includes such a strained silicon epitaxy layer (e.g., "strained Si layer (semiconductor layer) 40"). See TSMC-1005, Abstract, 5:35-42 ("a second semiconductor layer such as a *strained Si layer*...."), 5:55-61 ("the second semiconductor layer is formed from *strained Si*, the strained Si layer which covers the surface of the SiGe crystal layer functions as a channel."), 5:18-19, 6:63-7:10, 9:46-47, Figs. 2, 3B, 8; TSMC-1003, ¶¶190-191; *supra*, §X(i)(1[a]). Figures 2 and 8 depict the strained silicon epitaxy layer (in blue) of Sugiyama's composite fin structure as shown below with annotations:

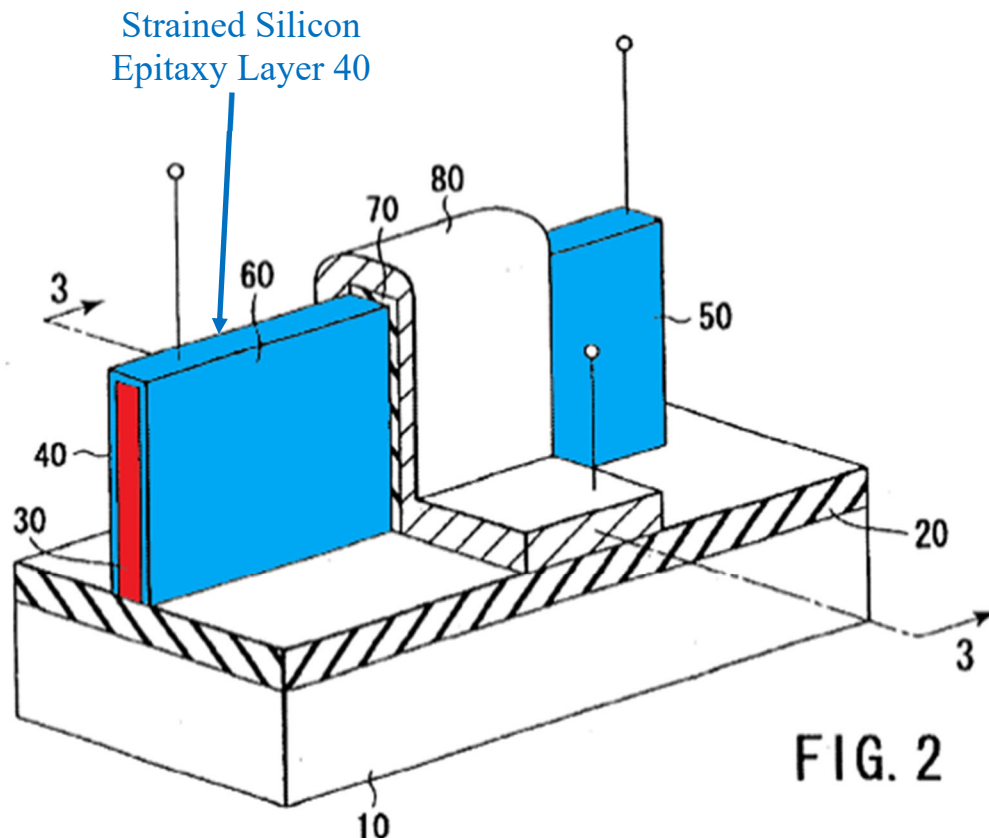
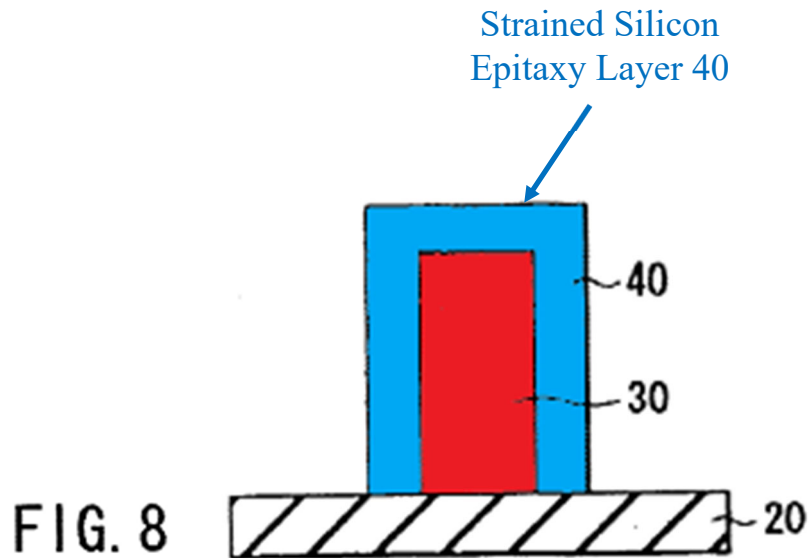


FIG. 2



TSMC-1003, ¶190.

Accordingly, Sugiyama satisfies claim 8.

ix) Claim 9

Claim 9 recites that said strained silicon epitaxy layer has a thickness of about 50-300 angstroms. Sugiyama's strained silicon epitaxy layer (e.g., "strained Si layer 40") has a thickness that "is desirably 5 nm (inclusive) to 30 nm (inclusive)," which satisfies claim 9. *Supra*, §X(iv); TSMC-1005, 9:49-50, 10:8-9; TSMC-1003, ¶192.

x) Claim 10

Sugiyama's gate strip (e.g., "gate electrode 80") is made from "polysilicon," which satisfies claim 10. *Supra*, §X(v); TSMC-1005, 10:9-20, 7:64-67; TSMC-1003, ¶193.

XI. GROUND 4: Sugiyama combined with Chau renders Claim 3 unpatentable

Claim 3 is obvious over Sugiyama in view of Chau, as detailed below and in Dr. Braun's declaration (*see* TSMC-1003, §IX(D)).

i) Claim 3

Sugiyama discloses a composite fin structure (e.g., combination of “SiGe layer 30” and “strained Si layer 40”) having a width of said substantially flat top surface that is approximately equal to its height. *Supra*, §X(iii); TSMC-1005, 9:30-50, Fig. 8; TSMC-1003, ¶¶195-196.

Sugiyama further discloses preferred dimension for SiGe layer 30 of a “height W” of “50 nm or more” and a “width d” that is “desirably 10 nm (inclusive) to 50 nm (inclusive).” TSMC-1005, 9:30-40, 9:49-50; *supra*, §X(iii).

It was obvious in view of Chau for a POSITA to choose dimensions from these ranges such that Sugiyama's composite fin structure would have a width of its substantially flat top surface that is approximately equal to its height, as recited in claim 3. TSMC-1003, ¶¶197-202. Indeed, Chau discloses a composite fin structure having a width of its substantially flat top surface that is approximately equal to its height. *Supra*, §IX(i).

It was obvious to incorporate a composite fin structure having approximately equal width and height dimensions into Sugiyama's tri-gate device in view of Chau

for the same reasons it was obvious to similarly modify Lee in view of Chau.

TSMC-1003, ¶¶197-201; *supra*, §IX(i).

Additionally, for the same reasons discussed above, a POSITA would have found implementing approximately equal height and width dimensions for Sugiyama's composite fin structure routine and easily achievable, and thus would have had a reasonable expectation of success in doing so. TSMC-1003, ¶201; *supra*, §IX(i). Indeed, Sugiyama discloses similar photolithographic, patterning, etching, and deposition processes for fabricating composite fin structures as used by Chau, and thus a POSITA have found it relatively simple to implement such processes to fabricate a composite fin structure having approximately equal height and width dimensions. *See* TSMC-1005, 7:64-9:61, Figs. 4-8, 12:60-67; *supra*, §IX(i); *see also supra*, §VIII(iii).

Accordingly, Sugiyama combined with Chau renders claim 3 obvious.

XII. GROUND 5: Dakshina anticipates Claims 1-2 and 4-10

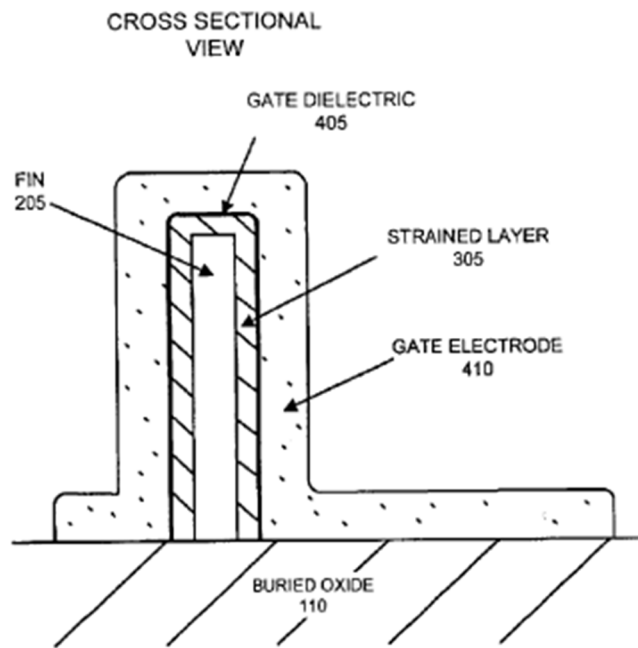
Dakshina anticipates Claims 1-2 and 4-10, as detailed below and in Dr. Braun's declaration (*see* TSMC-1003, §IX(E)).

i) Claim 1

1[pre] "Three Dimensional Triple Gate (Tri-gate) Device"

Dakshina discloses a Tri-gate device (e.g., “semiconductor structure,” “FinFET”). *See* TSMC-1006, Abstract, 1:5-6, 1:32-41, 2:65-3:7, 4:10-30, Figs. 4A-4B; TSMC-1003, ¶¶203-206.

For example, Dakshina discloses “an increased mobility channel FinFET” that “uses a vertically formed strained channel layer that is self-aligned to [a] fin channel.” TSMC-1006, 2:65-66, 1:31-33, 4:21-24. Figure 4A depicts an example vertical cross-section of Dakshina’s FinFET:



Dakshina’s “FinFET” is a “three dimensional triple gate device” at least because of the presence of the three-dimensional fin 205/strained layer 305 and gate electrode 410 that covers three surfaces of the fin 205/strained layer 305 (i.e., both vertical side surfaces and the top surface of the fin 205/strained layer 305). TSMC-1003, ¶205; *see* TSMC-1006, 3:37-4:24, Figs. 4A-4B; *see also* TSMC-

1004, 12:26-30 (“The double gate 103 is actually a triple gate because it covers both sides and the top of the strained silicon channel 104.”).

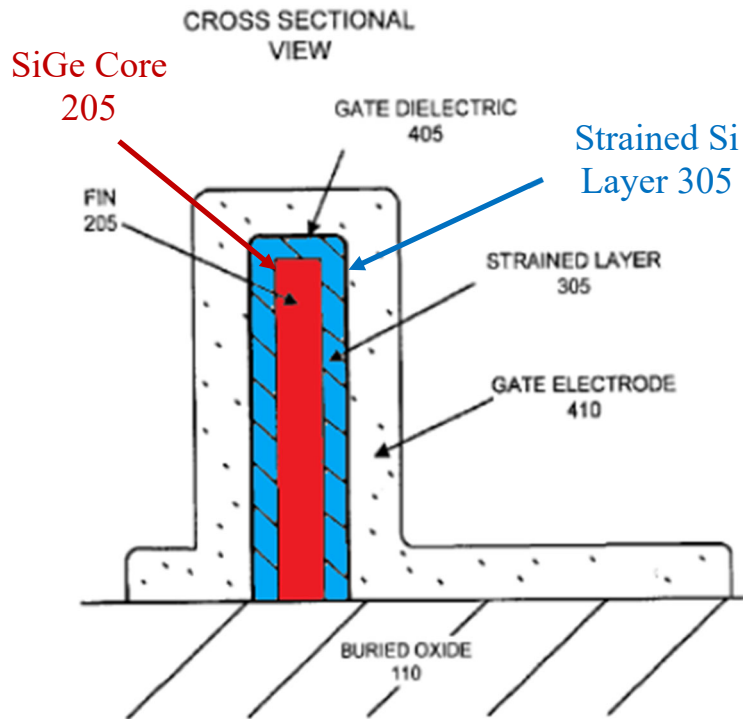
Accordingly, Dakshina’s device satisfies claim 1’s preamble.

1[a] “Composite Fin Structure”

Element 1[a] calls for “a composite fin structure consisting of a silicon germanium core and a strained silicon epitaxy layer grown from surface of said silicon germanium core,” which Dakshina discloses. TSMC-1003, ¶¶207-211.

For example, Dakshina’s FinFET device includes a composite fin structure consisting of: (i) a silicon germanium core (e.g., “fin 205”); and (ii) a strained silicon epitaxy layer (e.g., “strained layer 305”) grown from the surface of the silicon germanium core. *See* TSMC-1006, Abstract, 3:10-28, 3:38-44, 3:57-4:6, Figs. 1-4AB; TSMC-1003, ¶207.

Annotated Figure 4A depicts Dakshina’s composite fin structure:



TSMC-1003, ¶208.

Dakshina’s fin 205 is “formed from fin channel layer 105,” and made of “ $\text{Si}_x\text{Ge}_{(1-x)}$ ” (i.e., silicon germanium). TSMC-1006, 3:25-28, 3:39-44; TSMC-1003, ¶209.

Dakshina’s “strained layer 305 may [be] formed on fin 205...using a selective *epitaxial* deposition process” (TSMC-1006, 3:59-64), and is made of “*silicon*” (*id.*, 4:5-6). Accordingly, Dakshina’s strained layer 305 is a silicon epitaxy layer grown from silicon germanium core 205, and these two components together form a composite fin structure and satisfy this limitation.

1[b] “Gate Strip”

Element 1[b] calls for “a gate strip wrapping a portion of said composite fin structure.” Dakshina discloses this element. TSMC-1003, ¶¶212-215.

For example, Dakshina discloses a gate strip (e.g., “gate electrode 410”) wrapping a portion of said composite fin structure. See TSMC-1006, 4:10-24, Figs. 4A-4B; TSMC-1003, ¶212. “After formation of strained layer 305, a gate dielectric 405 and *gate electrode 410* may be formed *on the portion of fin 205* not covered by source 210 and drain 215.” TSMC-1006, 4:10-13; *see id.*, 4:21-24.

Annotated Figures 4A (cross-section view) and 4B (top view) depict Dakshina’s gate electrode 410 (in green) wrapping a portion of the composite fin structure:

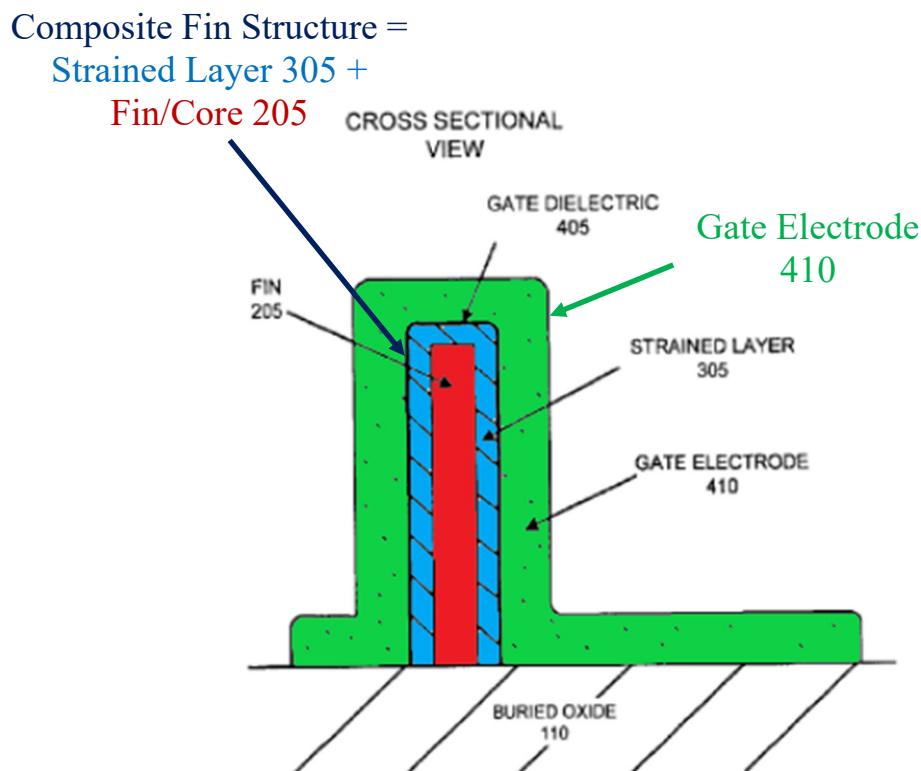
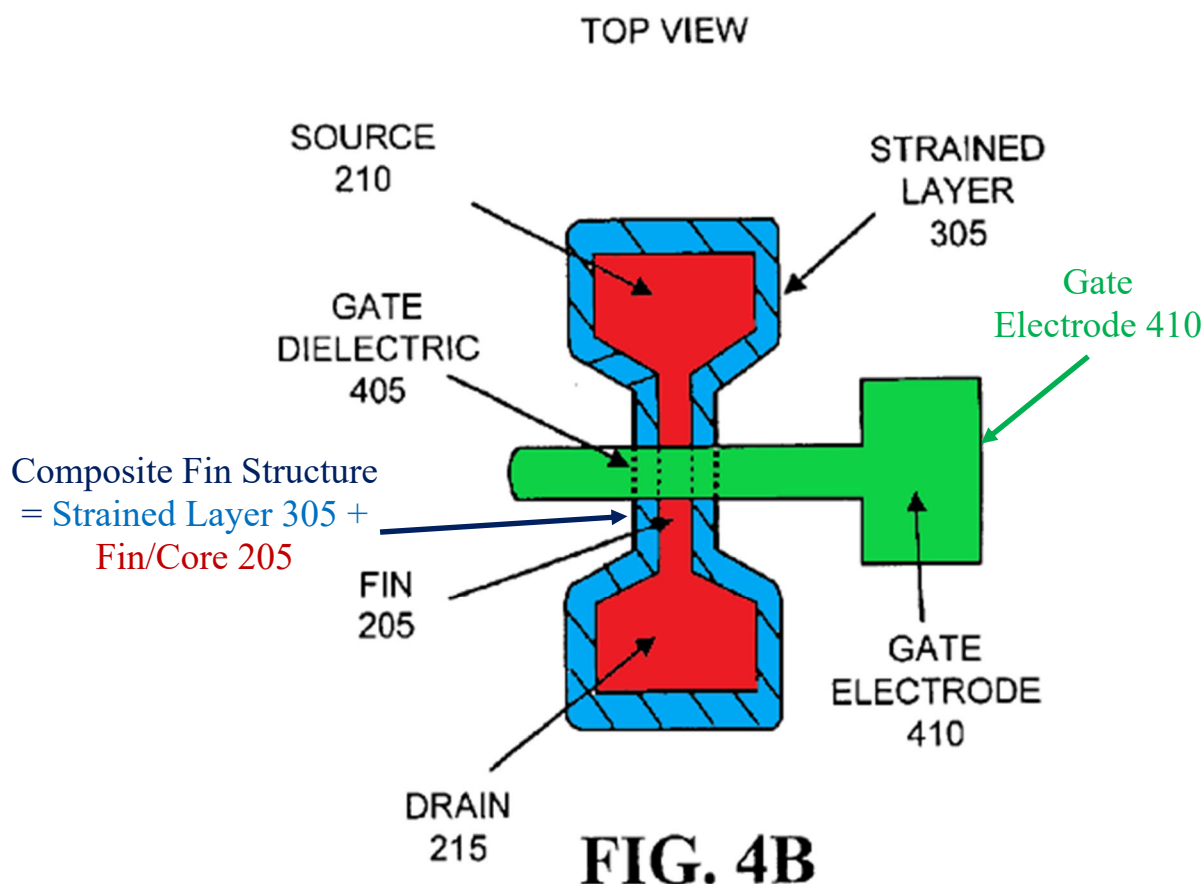


Fig. 4A



TSMC-1003, ¶213.

The gate electrode covers both the top and both sides of the composite fin structure. TSMC-1003, ¶214; TSMC-1006, 2:44-49 (“FIG. 4A illustrates a cross-sectional view of a...gate electrode formed upon a fin ...”). As seen in Figure 4B, the gate electrode only covers part of the composite fin structure between the source and drain. TSMC-1003, ¶214; TSMC-1006, 4:10-13 (the gate electrode is formed on the “portion of the fin 205 not covered by source 210 and drain 215”).

Accordingly, Dakshina satisfies this limitation.

1[c] “Source/Drain Regions”

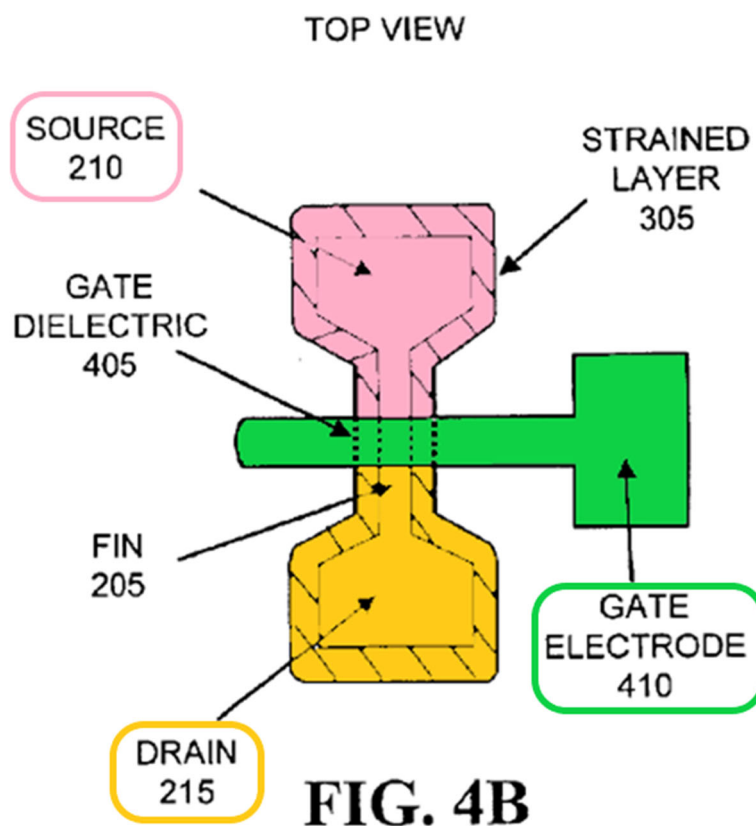
Element 1[c] specifies that “portions of said composite fin structure not covered by said gate strip constitute source/drain regions of said Tri-gate device.”

Dakshina discloses this element. TSMC-1003, ¶¶216-219.

For example, Dakshina discloses that portions of said composite fin structure (e.g., combination of “fin 205” and “strained layer 305”) not covered by said gate strip (e.g., “gate electrode 410”) constitute source/drain regions (e.g., “source 210,” “drain 215”) of said Tri-gate device. *See* TSMC-1006, 3:45-64, 4:10-13, Figs. 2C, 2D, 3B, 4B; TSMC-1003, ¶216.

Dakshina’s “source 210 and drain 215 regions may be formed adjacent the respective ends of fin 205” from the same material (e.g., $\text{Si}_x\text{Ge}_{(1-x)}$) as fin 205. TSMC-1006, 3:45-56. “Strained layer 305” is then “***formed on fin 205, source 210 and drain 215,***” thereby forming the composite fin structure and included source 210 and drain 215. *See id.*, 3:57-67; TSMC-1003, ¶217.

Indeed, in describing Figures 4A and 4B, Dakshina states that “[a]fter formation of strained layer 305, a gate dielectric 405 and ***gate electrode 410*** may be formed ***on the portion of fin 205 not covered by source 210 and drain 215.***” TSMC-1006, 4:10-13. Annotated Figure 4B depicts the portions of the composite fin structure not covered by gate electrode 410, which constitute source 210 (in pink) and drain 215 (in gold):



TSMC-1003, ¶218.

Accordingly, Dakshina satisfies this limitation.

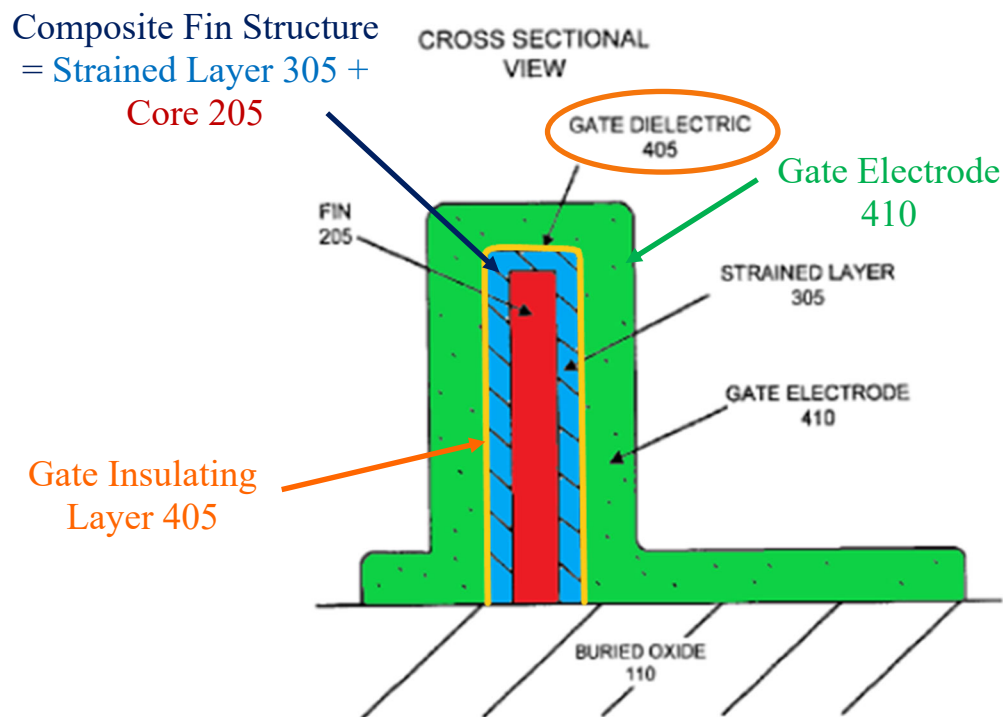
1[d] “Gate Insulating Layer”

Element 1[d] calls for “a gate insulating layer interposed between said composite fin structure and said gate strip,” which Dakshina discloses. TSMC-1003, ¶¶220-222.

For example, Dakshina discloses a gate insulating layer (e.g., “gate dielectric 405”) interposed between said composite fin structure (e.g., combination of “fin 205” and “strained layer 305”) and said gate strip (e.g., “gate electrode 410”). *See*

TSMC-1006, 4:10-24, Figs. 4A, 4B; TSMC-1003, ¶220. “After formation of strained layer 305, a *gate dielectric 405* ... may be formed on the portion of fin 205 not covered by source 210 and drain 215.” TSMC-1006, 4:10-12. Gate dielectric 405 includes an “insulating” material such as “SiO, SiO₂, SiN, SiON, HFO₂, ZrO₂, Al₂O₃, HFSiO(x) ZnS, MgF₂, or other dielectric materials.” *Id.*, 4:13-16. Dakshina further explains that “[g]ate electrode 410 may be formed upon gate dielectric 405.” *Id.*, 4:16-17.

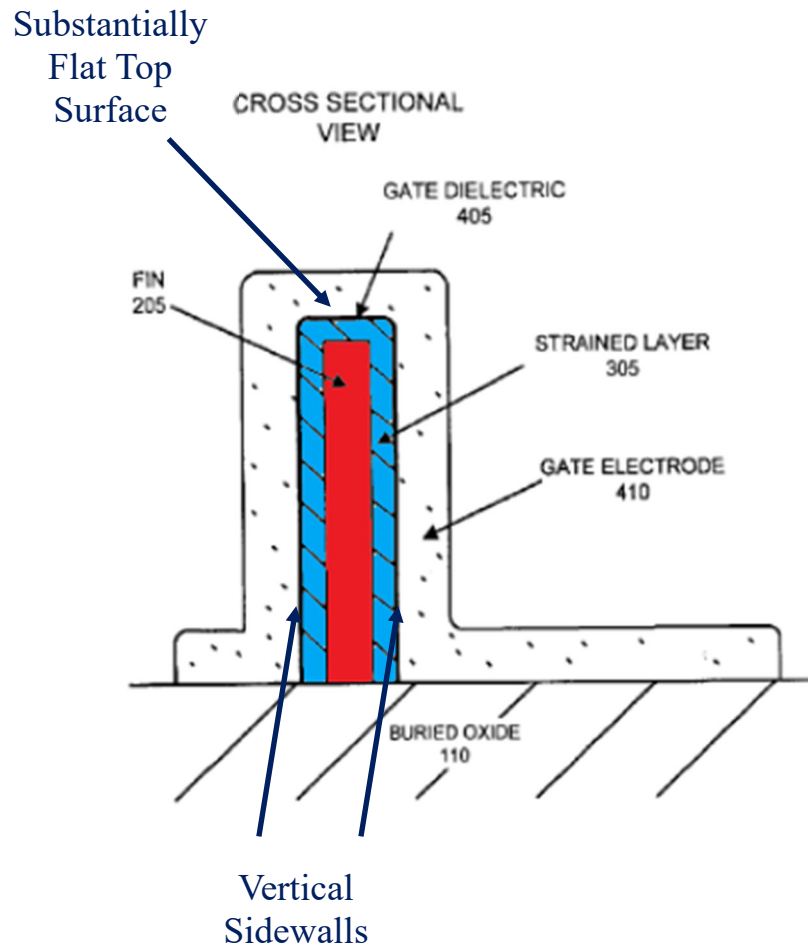
As depicted in annotated Figure 4A, gate dielectric/insulating layer 405 is interposed between Dakshina’s composite fin structure (i.e., the combination of fin 205 and strained layer 305) and gate strip (i.e., “gate electrode 410”) (TSMC-1003, ¶221):



Accordingly, Dakshina satisfies limitation 1[d] and all limitations of claim 1.

ii) Claim 2

Dakshina's composite fin structure (e.g., combination of "fin 205" and "strained layer 305") has a substantially flat top surface and vertical sidewalls, as recited in claim 2. *See* TSMC-1006, 3:37-64, 4:21-30, Figs. 3A, 4A; TSMC-1003, ¶¶224-226. Dakshina's strained layer 305 (which forms the upper layer of Dakshina's composite fin structure) is formed on three sides of fin 205, including—as shown in the figures—on a top surface and both "vertical surfaces." *See* TSMC-1006, 4:21-24 ("Formation of gate dielectric 405 and gate electrode 410 upon fin 205, thus, produces a FET sidewall vertical channel that includes a thin strained layer 305 at both vertical surfaces of fin 205."); TSMC-1003, ¶225. Annotated Figure 4A depicts these surfaces of Dakshina's composite fin structure, where the composite fin structure has a top surface that is substantially flat and has vertical sidewalls (TSMC-1003, ¶225):



Accordingly, Dakshina satisfies claim 2.

iii) Claim 4

Claim 4 recites that said strained silicon epitaxy layer has a thickness of about 50-300 angstroms.

Dakshina's strained silicon epitaxy layer (e.g., "strained layer 305") has a thickness that "may be 5 nm." TSMC-1006, 4:4-5. Dakshina further indicates that the thickness of strained layer 305 "is approximately $\frac{1}{2}$ to $\frac{1}{3}$ of the fin 205 width w" and that fin 205 "may be formed...with a width (w) in a range of 10-15 nm."

TSMC-1006, 4:2-4, 3:40-41. Accordingly, Dakshina discloses values and ranges of thicknesses for strained layer 305 that include a specific example of 5 nm (50 angstroms) and also an example range of 5-7.5 nm (50-75 angstroms) for a 15 nm wide fin, thus satisfying claim 4. TSMC-1003, ¶227.

iv) Claim 5

Dakshina's gate strip (e.g., "gate electrode 410") is made of "polysilicon." TSMC-1006, 4:16-18, claims 8, 11, 24; TSMC-1003, ¶228. "Gate electrode 410 may be formed upon gate dielectric 405 and may include...a *layer of polysilicon*." TSMC-1005, 4:16-18; *see also id.*, 4:54-56. Accordingly, Dakshina satisfies claim 5.

v) Claim 6

6[pre] "Tri-gate Device"

Dakshina discloses a Tri-gate device. *Supra*, §XII(i)(1[pre]); *see* TSMC-1006, Abstract, 1:5-6, 1:32-41, 2:65-3:7, 4:10-30, Figs. 4A-4B; TSMC-1003, ¶¶229-231.

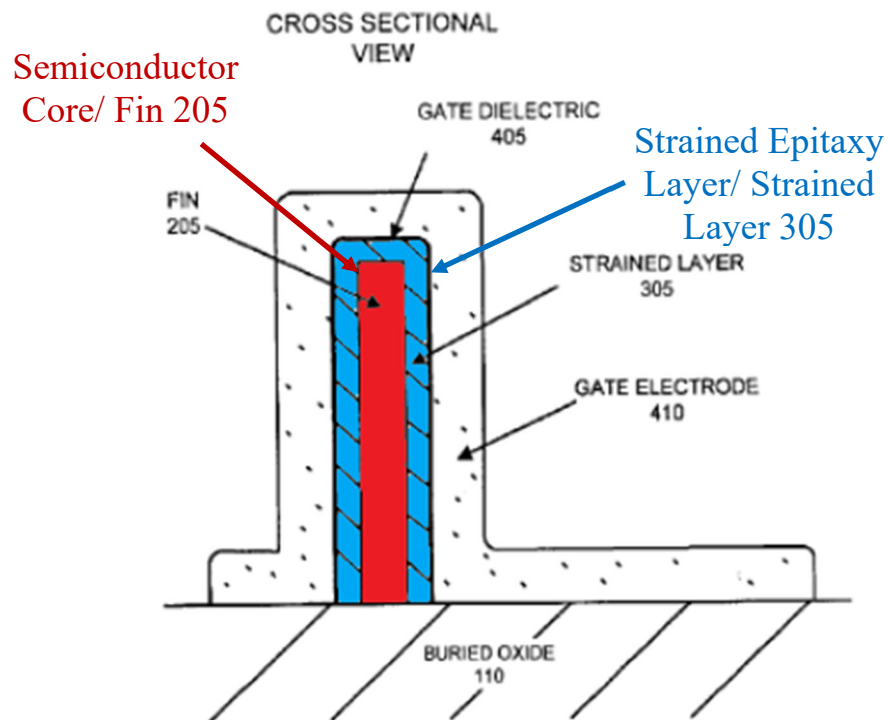
6[a] "Composite Fin Structure"

Element 6[a] calls for "a composite fin structure consisting of a semiconductor core and a strained epitaxy layer grown from surface of said semiconductor core, said semiconductor core having a first lattice constant that

miss-matches a second lattice constant of said strained epitaxy layer.” Dakshina discloses this element. TSMC-1003, ¶¶232-237.

For example, Dakshina’s FinFET device includes a composite fin structure consisting of: i) a semiconductor core (e.g., “fin 205”); and ii) a strained epitaxy layer (e.g., “strained layer 305”) grown from the surface of the semiconductor core. See TSMC-1006, Abstract, 3:10-28, 3:38-44, 3:57-4:6, Figs. 1-4AB; TSMC-1003, ¶232; *supra*, §XII(i)(1[a]).

Figure 4A depicts Dakshina’s composite fin structure with annotations highlighting its constituent layers (i.e., silicon germanium semiconductor core 205 in red and strained silicon epitaxy layer 305 in blue):



TSMC-1003, ¶233.

Dakshina explains that fin 205 is “formed from fin channel layer 105” and made of “ $\text{Si}_x\text{Ge}_{(1-x)}$ ” (i.e., a ***semiconductor***). TSMC-1006, 3:25-28, 3:39-44; TSMC-1003, ¶234.

Dakshina further explains that “strained layer 305 may be formed on fin 205...using a selective ***epitaxial*** deposition process.” TSMC-1006, 3:59-64. “Strained layer 305” is made of “***silicon***.” *Id.*, 4:5-6. Accordingly, strained layer 305 is a strained epitaxy layer grown from the silicon germanium semiconductor core/fin 205, which together form a composite fin structure. TSMC-1003, ¶235.

Additionally, Dakshina’s semiconductor core (e.g., fin 205) has a first lattice constant that mis-matches a second lattice constant of Dakshina’s strained epitaxy layer (e.g., strained layer 305). *See* TSMC-1006, Abstract, 1:33-40, 1:49-57; 3:1-7, 3:20-36, 4:24-45, 5:29-27, 6:20-26; TSMC-1003, ¶236. “Strained layer 305 provides improved carrier mobility through the induction of tensile strain in strained layer 305 caused by the ***lattice mismatch between strained layer 305 and fin 205***.” TSMC-1006, 4:24-27. Dakshina further describes the “lattice constant of silicon” (used to form “strained layer 305”) as different from (i.e., ***mis-matches***) the lattice constant of “ $\text{Si}_x\text{Ge}_{(1-x)}$ ” (used to form “fin 205”). *See id.*, 3:19-24 (“Fin channel layer 105 may include a crystalline material ***with a lattice constant larger than the lattice constant of a crystalline material selected for a strained channel layer***.... If, for example, silicon is selected for the strained channel layer, fin

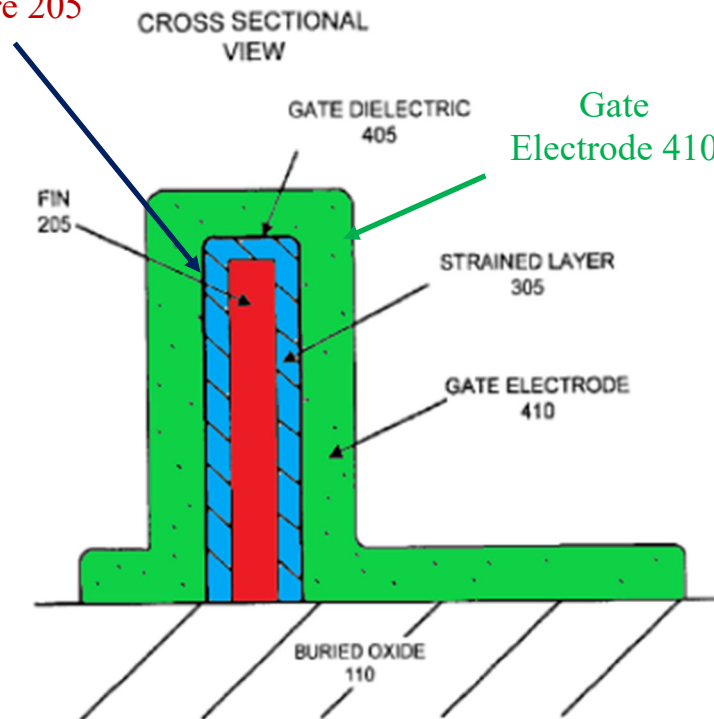
channel layer 105 may include a crystalline material *with a lattice constant large than the lattice constant of silicon.*”); 3:64-4:2.

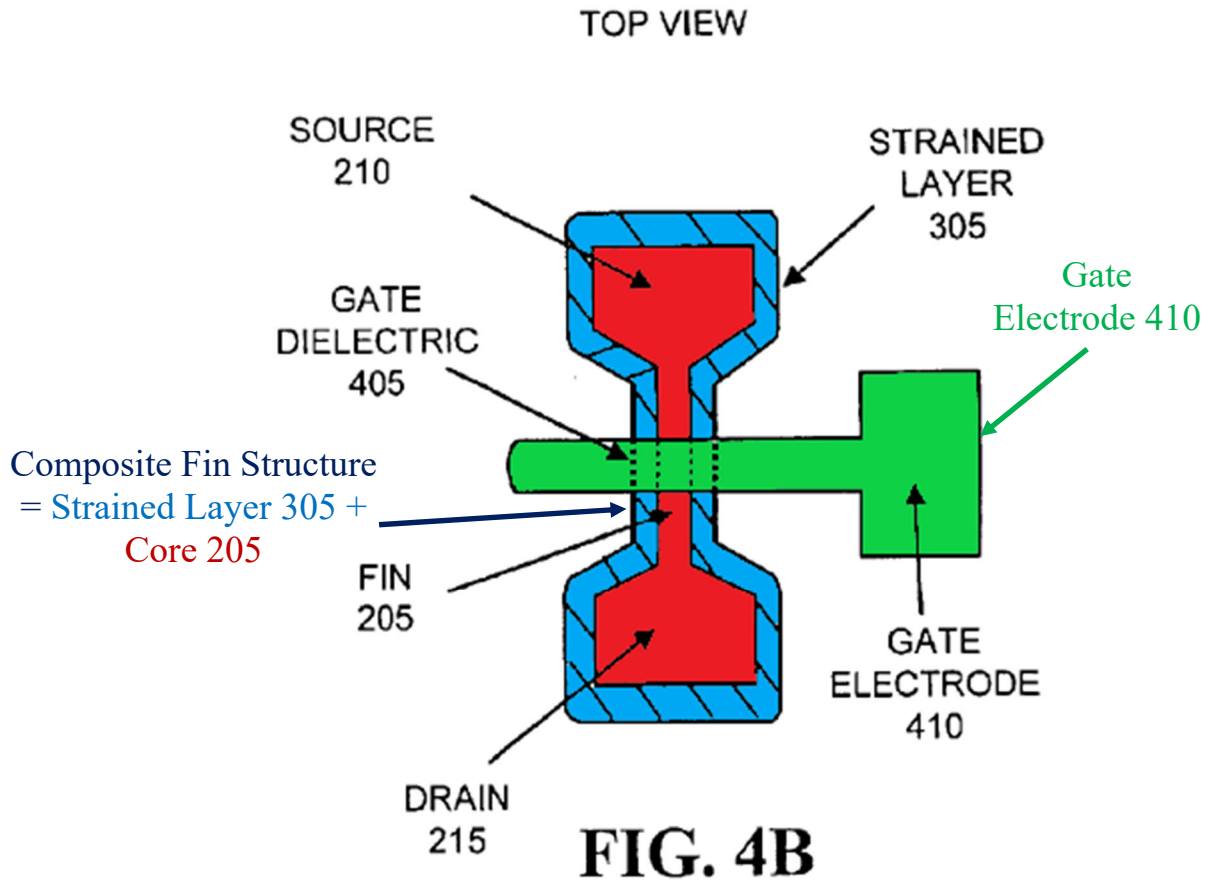
Accordingly, Dakshina satisfies limitation 6[a].

6[b] “Gate Strip”

Element 6[b] calls for “a gate strip wrapping a portion of said composite fin structure.” Dakshina discloses this element (e.g., “gate electrode 410”). *Supra*, §XII(i)(1[b]); see TSMC-1006, 4:10-24, Figs. 4A-4B; TSMC-1003, ¶¶238-241.

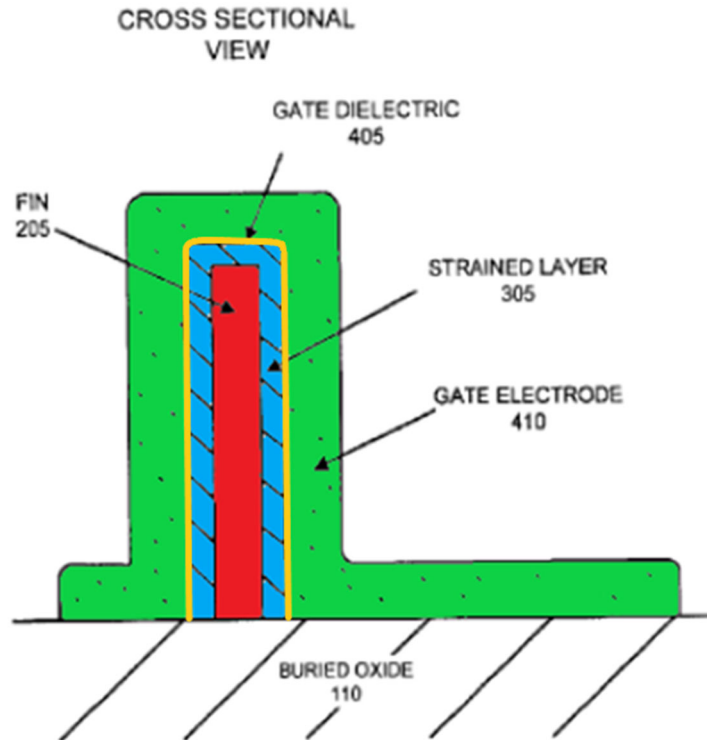
Composite Fin Structure
= Strained Layer 305 +
Core 205





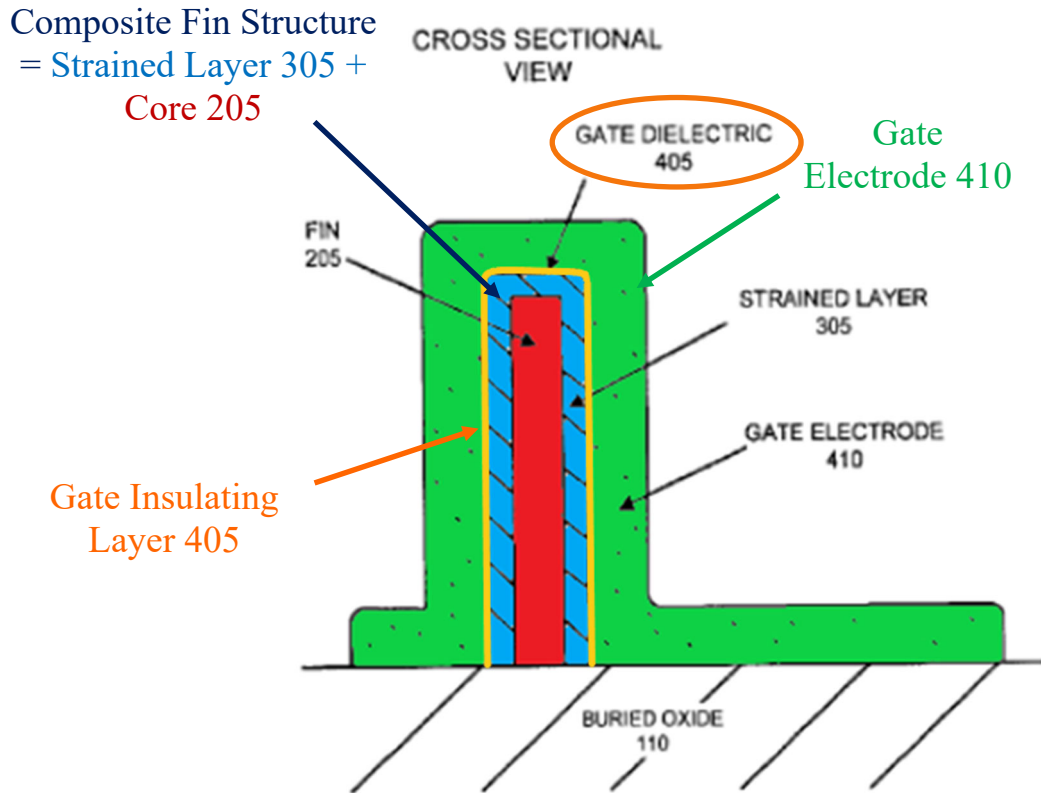
6[c] “Source/Drain Regions”

Element 6[c] specifies that “portions of said composite fin structure not covered by said gate strip constitute source/drain regions of said Tri-gate device,” which Dakshina discloses. *Supra*, §XII(i)(1[c]); see TSMC-1006, 3:45-64, 4:10-13, Figs. 2C, 2D, 3B, 4B; TSMC-1003, ¶¶242-244.



6[d] “Gate Insulating Layer”

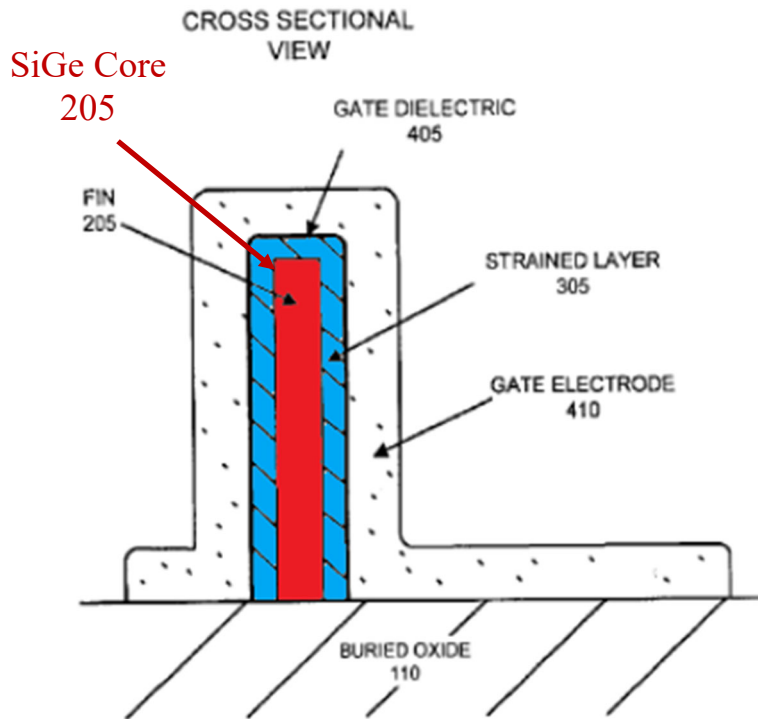
Element 6[d] calls for “a gate insulating layer interposed between said composite fin structure and said gate strip.” Dakshina discloses this element (e.g., “gate dielectric 405”). *Supra*, §XII(i)(1[d]); *see* TSMC-1006, 4:10-24, Figs. 4A, 4B; TSMC-1003, ¶¶245-246.



vi) Claim 7

Dakshina's semiconductor core (e.g., "fin 205") consists of silicon germanium (e.g., " $\text{Si}_x\text{Ge}_{(1-x)}$ ") as recited by claim 7. *See* TSMC-1006, Abstract, 3:10-28 ("Fin channel layer 105 may include, for example, ***Si_xGe_(1-x)***...."), 3:38-44, 3:57-4:6, Figs. 1-4AB; TSMC-1003, ¶¶247-249; *supra*, §XII(i)(1[a]). Dakshina does not state that any additional materials are included in the core/fin 205. TSMC-1003, ¶249.

Annotated Figure 4A depicts Dakshina's silicon germanium semiconductor core:



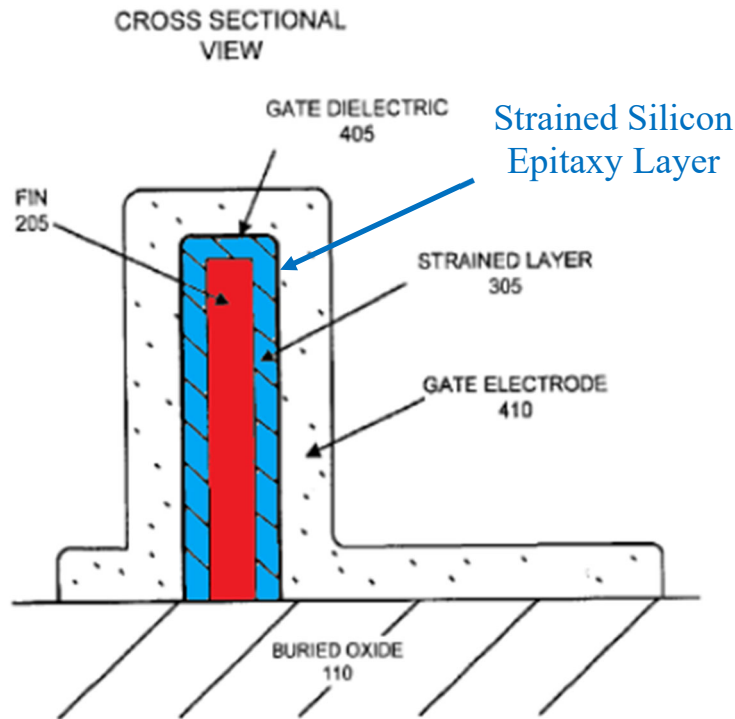
TSMC-1003, ¶248.

vii) Claim 8

Claim 8 recites that the strained epitaxy layer is a strained silicon epitaxy layer.

Dakshina’s FinFET device includes a strained silicon epitaxy layer (e.g., “strained layer 305”). See TSMC-1006, Abstract, 3:10-28, 3:38-44, 3:57-4:6, Figs. 1-4AB; TSMC-1003, ¶¶250-252; *supra*, §XII(i)(1[a]).

Annotated Figure 4A depicts the strained silicon epitaxy layer of Dakshina’s FinFET device:



TSMC-1003, ¶251.

Dakshina explains that “strained layer 305 may formed on fin 305...using a selective *epitaxial* deposition process.” TSMC-1006, 3:59-64. “Strained layer 305” includes “*silicon.*” *Id.*, 4:5-6. Accordingly, Dakshina satisfies claim 8.

viii) Claim 9

Claim 9 recites that said strained silicon epitaxy layer has a thickness of about 50-300 angstroms. Dakshina discloses strained silicon epitaxy layers (e.g., “strained layer 305”) having thicknesses within this range. *Supra*, §XII(iii); see TSMC-1006, 4:2-5, 3:40-41; TSMC-1003, ¶253.

ix) Claim 10

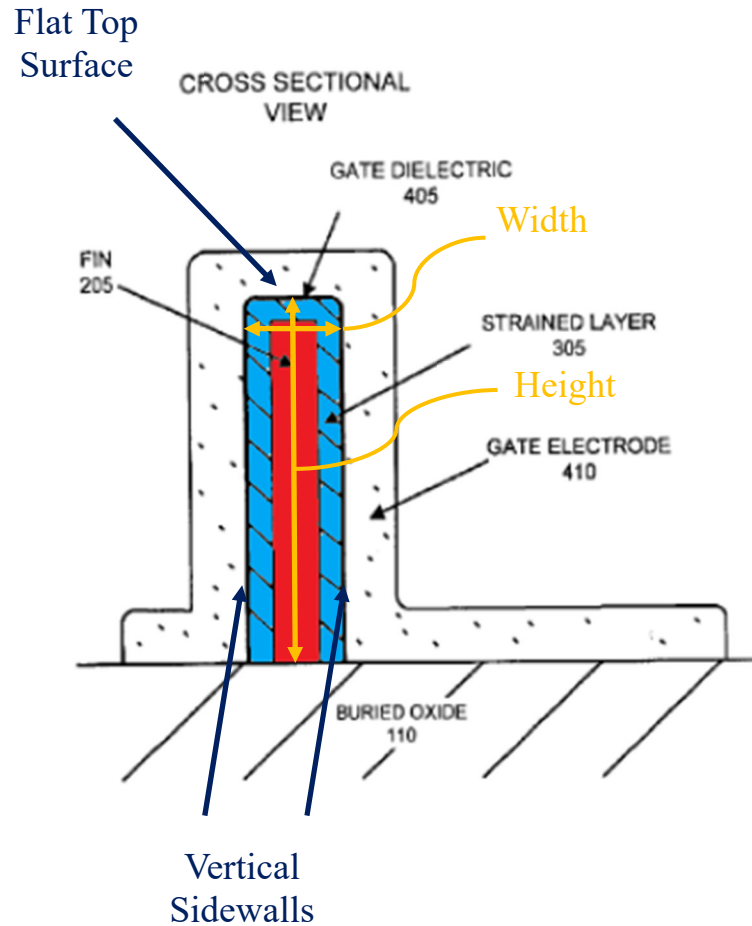
Dakshina's "gate electrode 410" is made of "polysilicon," which satisfies claim 10. *Supra*, §XII(iv); *see* TSMC-1006, 4:16-18, claims 8, 11, 24; TSMC-1003, ¶254.

XIII. GROUND 6: Dakshina combined with Chau renders Claim 3 unpatentable

Claim 3 is obvious over Dakshina in view of Chau, as detailed below and in Dr. Braun's declaration (*see* TSMC-1003, §IX(F)).

i) Claim 3

Dakshina's composite fin structure (e.g., combination of "fin 205" and "strained layer 305") has a substantially flat top surface and vertical sidewalls. *Supra*, §XII(ii); *see* TSMC-1006, Abstract, 3:10-28, 3:37-64, 3:57-4:6, 4:21-30, Figs. 1-4AB; TSMC-1003, ¶255. Annotated Figure 4A depicts these surfaces of Dakshina's composite fin structure with corresponding width and height:



TSMC-1003, ¶255.

Chau discloses a composite fin structure having a width of said flat top surface that is approximately equal to its height. *Supra*, §IX(i). It was obvious to construct Dakshina's composite fin structure with a width of its substantially flat top surface approximately equal to its height in view of the teachings of Chau, for the same reasons discussed above for similarly combining Lee with Chau or Sugiyama with Chau. TSMC-1003, ¶258; *supra*, §§VIII(iii), IX(i), XI(i).

Additionally, for the same reasons discussed above, a POSITA would have found implementing approximately equal height and width dimensions for

Dakshina's composite fin structure routine and easily achievable, and thus would have had a reasonable expectation of success in doing so. TSMC-1003, ¶¶258-260; *supra*, §§VIII(iii), IX(i), XI(i). Dakshina discloses similar processes for fabricating composite fin structures as Chau, and thus a POSITA would have found using such processes to fabricate a composite fin structure having approximately equal height and width dimensions straightforward. TSMC-1003, ¶260; *see* TSMC-1006, 3:40-44, 3:59-64; *supra*, §§VIII(iii), IX(i), XI(i).

Accordingly, Dakshina in combination with Chau renders claim 3 obvious.

XIV. GROUNDS FOR STANDING

Petitioner certifies that the '181 Patent is available for *Inter Partes* Review, and Petitioner is not barred or estopped from requesting Review on the identified grounds.

XV. MANDATORY NOTICES AND FEES

A. Real Party-In-Interest

The real party-in-interest is Taiwan Semiconductor Manufacturing Company Limited. No other parties directed, controlled, or funded this *Inter Partes* Review proceeding.

B. Related Matters

Petitioner is not aware of any related matters to this *Inter Partes* Review proceeding or the '181 Patent.

C. Counsel and Service Information

Pursuant to 37 C.F.R. §42.8(b)(3) and 42.10(a), Petitioner provides the following counsel and service information. Pursuant to 37 C.F.R. § 42.10(b), a Power of Attorney accompanies this Petition.

LEAD COUNSEL	BACK-UP COUNSEL
Nicholas M. Lagerwall Reg. No. 63,272 FOLEY & LARDNER LLP 150 East Gilman Street, Suite 5000 Madison, Wisconsin 53703 608-257-5035 nlagerwall@foley.com	Pavan K. Agarwal Reg. No. 40,888 FOLEY & LARDNER LLP 3000 K Street N.W., Suite 600 Washington, DC 20008 202-672-5300 pagarwal@foley.com Michael R. Houston Reg. No. 58,486 FOLEY & LARDNER LLP 321 North Clark Street, Suite 3000 Chicago, Illinois 60654 312-832-4500 mhouston@foley.com

Petitioner consents to electronic service directed to the following email address: Foley_TSMC_181_IPR2025-01082@foley.com.

D. Payment of Fees

The Office is authorized to charge fees for this Petition to Deposit Account No. 19-0741. Any additional fees that might be due are also authorized.

XVI. CONCLUSION

For the foregoing reasons, Petitioner requests institution of an IPR and cancellation of the Challenged Claims.

Date: August 8, 2025

Respectfully submitted,

By: /Nicholas Lagerwall/

Nicholas Lagerwall
Reg. No. 63,272
FOLEY & LARDNER LLP
Counsel for Petitioner

**CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATION,
TYPEFACE REQUIREMENTS, AND TYPE STYLE REQUIREMENTS**

1. This Petition complies with the type-volume limitation of 14,000 words, comprising 13,547 words, as counted using the “Word Count” feature of the Microsoft Word software that was used to prepare this paper, excluding the parts exempted by 37 C.F.R. §42.24(a).

2. This Petition complies with the general format requirements of 37 C.F.R. §42.6(a) and has been prepared using Microsoft® Word for Microsoft 365 in 14-point Times New Roman.

Date: August 8, 2025

By: /Nicholas Lagerwall/

Nicholas Lagerwall
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Counsel for Petitioner

CERTIFICATE OF SERVICE

The undersigned hereby certifies that on August 8, 2025, true and correct copies of the foregoing document and supporting materials were served in its entirety on the Patent Owner at the following address of record listed on the USPTO's Patent Center via FedEx International Priority:

Winston Hsu
North America Intellectual Property Corporation
5F., No.398, Fuhe Rd., Yonghe Dist.
New Taipei City 234645
Taiwan

Courtesy copies have been concurrently served by FedEx Priority delivery on Patent Owner's litigation counsel at:

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Date: August 8, 2025

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