cādence®

23 Apr 2025

Also announce tool certification for TSMC N3C process and initial collaboration on TSMC's newest A14 technology

SAN JOSE, Calif.— Cadence (Nasdaq: CDNS) today announced it is furthering its longstanding collaboration with TSMC to accelerate time to silicon for 3D-IC and advanced-node technologies through certified design flows, silicon-proven IP and ongoing technology collaboration. As a leading provider of IP for TSMC N2P, N5 and N3 process nodes, Cadence continues to deliver cutting-edge AI-driven design solutions to the TSMC ecosystem for multiple horizontal applications from chiplets and SoCs to advanced packaging and 3D-ICs. The deep collaboration encompasses certified tools and flows for TSMC's N2P and A16™ technologies, paves the way for TSMC's A14 and further unlocks 3D-IC possibilities by extending support for TSMC 3DFabric® design and packaging. In addition, Cadence and TSMC are extending tool certification for newly announced TSMC N3C technology based on available N3P design solutions.

N2P and A16 AI Silicon Design

Cadence is driving innovation in AI chip design with certified tools and optimized IP for TSMC's advanced N2P and A16™ process technologies. Reinforcing its memory IP leadership, Cadence offers TSMC9000 pre-silicon-certified DDR5 12.8G IP for N2P. Cadence® digital, custom/analog design and thermal analysis solutions are certified for TSMC N2P and A16 technologies. Combined with continued collaboration on AI-driven digital design solutions

for N2P, including leveraging large language models (LLMs), these advancements play an important role in improving digital design flows for future process nodes.

Leading-Edge Automotive Solutions

ADAS, autonomous driving and software-defined vehicles are driving the need for leading-edge silicon for next-generation applications, and Cadence is accelerating this evolution with certified IP for TSMC's N5A and N3A processes. Cadence's high-performance design IP portfolio—featuring LPDDR5X-9600, PCI Express® (PCIe®) 5.0, CXL 2.0, 25G-KR and 10G multi-protocol SerDes—is specifically optimized for automotive use.

Expanding and Elevating 3DFabric Solution

Cadence provides the only complete chiplet design, packaging and system analysis solution for TSMC 3DFabric®. Cadence is expanding its design IP portfolio to meet the demands of the AI training market, delivering TSMC 9000-certified IP for 3D-IC design, including HBM3E 9.6G in N5/N4P and pre-silicon HBM3E 10.4G in N3P, alongside Universal Chiplet Express™ (UCIe™) 16G N3P solutions. In addition, Cadence's HBM4 test chip is pre-silicon-ready for tapeout, which is paving the way for CoWoS-L.

The Cadence Integrity™ 3D-IC Platform now features enhanced support for improved quality of results (QoR) and 3DIC full flow QC with reference flows for 3Dblox, while enabling global resource optimization, chip-package co-design and advanced multiphysics convergence analysis across static timing, power-IR and thermal. New support includes feedthrough creation for multi-chiplet designs and AI-powered tools for end-to-end 3D-IC planning, partitioning and optimization.

Cadence's Sigrity™ X technologies and Clarity™ 3D Solver are also enabled to facilitate compliance automation for 3Dblox Signal and Power Integrity (SIPI) analysis by integrating with the Cadence Integrity™ 3D-IC Platform. The integration flow fully automates high-speed S-parameter extraction and transient time domain analysis for the UCIe and HBM channels. Additionally,

the Cadence EMX® Planar 3D Solver is certified for N3 and in the process of N2P certification, enhancing simulation accuracy to meet the rigorous demands of advanced-node IC designs.

More-than-Moore Technology Innovation

Cadence continues to push the limits of technology scaling with continued More-than-Moore technology innovation. Cadence's Virtuoso® Studio supports analog and RF design migration, substantially reducing turnaround time when designing with advanced and RF nodes. Cadence is also driving design solutions advancements for TSMC's compact universal photonic engine (COUPE™) and enabling next-generation efficiency with TSMC design in the cloud, featuring GPU-accelerated compute for enhanced performance.

"Our collaboration with TSMC reinforces Cadence's commitment to driving innovation and accelerating time to silicon for our customers," said Chin-Chi Teng, senior vice president and general manager of the Digital & Signoff Group at Cadence. "By providing certified design flows, silicon-proven IP and support for TSMC's advanced-node technologies like N2P, N3 and N5, we're empowering designers to develop leading-edge solutions across infrastructure AI and physical AI applications, including automotive. Together with TSMC, we're pushing the boundaries of technology scaling, enabling next-generation advancements in chip design and packaging."

"Our enduring collaboration with Open Innovation Platform® (OIP) partners like Cadence has been pivotal in tackling some of the most intricate challenges in semiconductor design," said Lipen Yuan, senior director of advanced technology business development at TSMC. "By combining TSMC's advanced process and 3D stacking and packaging technologies with Cadence's cutting-edge design solutions, we empower our mutual customers to accelerate time to silicon while achieving exceptional performance, power efficiency and area optimization. Together, we continue to drive breakthroughs that transform technology and enable innovation."

About Cadence

Cadence is a market leader in AI and digital twins, pioneering the application of computational software to accelerate innovation in the engineering design of silicon to systems. Our design solutions, based on Cadence's Intelligent System Design™ strategy, are essential for the world's leading semiconductor and systems companies to build their next-generation products from chips to full electromechanical systems that serve a wide range of markets, including hyperscale computing, mobile communications, automotive, aerospace, industrial, life sciences and robotics. In 2024, Cadence was recognized by the Wall Street Journal as one of the world's top 100 best-managed companies. Cadence solutions offer limitless opportunities—learn more at www.cadence.com.

© 2025 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence, the Cadence logo and the other Cadence marks found at www.cadence.com/go/trademarks are trademarks or registered trademarks of Cadence Design Systems, Inc. All other trademarks are the property of their respective owners.

Category: Featured

For more information, please contact:

Cadence Newsroom
408-944-7039
newsroom@cadence.com

Source: Cadence Design Systems, Inc.

A Great Place to Do Great Work!

Tenth year on the FORTUNE 100 list

The Wall Street Journal

Best Managed Companies

Our Culture

Join The Team

Products

Company

Media Center

Contact Us

Connect with us

Sign up to receive the latest Cadence news

Email Address*

Subscribe

English (US)

Trademarks

Terms of Use

Privacy

Cookie Policy

Accessibility

Do Not Sell or Share My Personal Information

© 2025 Cadence Design Systems, Inc.