

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
Petitioner,

v.

MARLIN SEMICONDUCTOR LTD.,
Patent Owner.

Case No. IPR2025-01082
U.S. Patent No. 6,888,181

**PETITIONER'S OPPOSITION TO PATENT OWNER'S
DISCRETIONARY DENIAL REQUEST**

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PETITIONER’S UPDATED EXHIBIT LIST

Ex.	Description
1001	U.S. Patent No. 6,888,181 (“’181 patent”).
1002	Prosecution File History, U.S. Patent No. 6,888,181 (“Prosecution History”)
1003	Declaration of Dr. Paul Braun
1004	U.S. Patent No. 7,045,401 (“Lee”)
1005	U.S. Patent No. 6,774,390 (“Sugiyama”)
1006	U.S. Patent No. 6,803,631 (“Dakshina”)
1007	U.S. Pat. App. Publication No. 2004/0036126 (“Chau”)
1008	U.S. Pat. App. Publication No. 2004/0061178 (“Lin”)
1009	U.S. Pat. App. Publication No. 2005/0017377 (“Joshi”)
1010	<i>Reserved</i>
1011	U.S. Patent No. 6,413,802 to Hu et al. (“Hu”)
1012	B. Doyle et al., Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout, Digest of the 2003 Symposium on VLSI Technology, pp. 133-34 (2003)
1013	B. S. Doyle et al., High Performance Fully-Depleted Tri-Gate CMOS Transistors, IEEE Electron Device Letters, Vol. 24, No. 4, pp. 263-65 (April 2003)
1014	<i>Reserved</i>
1015	S. Wolf et al., Silicon Processing for the VLSI Era Volume 1: Process Technology, 2 nd ed., pp. 225-29 (2000)
1016	U.S. Patent No. 5,461,250 to Burghartz et al. (“Burghartz”)
1017	U.S. Patent No. 6,339,232 to Shinichi Takagi (“Takagi”)

1018	U.S. Patent Application No. 10/227,068, as filed August 23, 2002
1019	T. Vogelsang; K.R. Hofmann, Electron mobilities and high-field drift velocities in strained silicon on silicon-germanium substrates, IEEE Transactions on Electron Devices, Volume: 39, Issue: 11, November 1992
1020	Y. X. Liu et al.; Flexible Threshold Voltage FinFETs with Independent Double Gates and an Ideal Rectangular Cross-Section Si-Fin Channel, IEEE International Electron Devices Meeting 2003, December 8-10, 2003
1021	JainNong Feng et al., BSIMSOI v.2.0 MOSFET Model – User’s Manual for BSIMDD2.0, Electronics Research Laboratory, 1999
1022	Nasdaq – This 1 Number May Ensure TSMC’s Market Dominance
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1026	TSMC Technology Overview
1027	Another Historic Investment Secured Under President Trump
1028	Decoding TSMC’s Contribution to the AI and 5G Ecosystem
1029	TSMC-Ansys Collaboration Press Release
1030	TSMC-Cadence Press Release
1031	TSMC’s Resurgence: What Lies Ahead for the Architect of AI
1032	Alex He, In the Global AI Chips Race, China Is Playing Catch-Up (September 18, 2024)
1033	NVIDIA and Oracle to Build US Department of Energy’s Largest AI Supercomputer for Scientific Discovery (October 28, 2025); available at https://nvidianews.nvidia.com/news/nvidia-oracle-us-department-of-energy-ai-supercomputer-scientific-discovery

1034	NVIDIA Blackwell Architecture; The engine behind AI factories for the age of AI reasoning—now in full production.; available at https://www.nvidia.com/en-us/data-center/technologies/blackwell-architecture/
1035	Decoding TSMC’s Contribution to the AI and 5G Ecosystem
1036	Yahoo! Finance Article on TSMC Fab 21
1037	Declaration of Mr. Robert W. Bahr
1038	U.S. Pat. App. Publication No. 2004/0145019 (“Dakshina’019”)
1039	U.S. Pat. App. Publication No. 2004/0256647 (“Lee’647”)
1040	Kevin Zhai, The changing landscape of semiconductor manufacturing: why the health sector should care (June 11, 2023)

I. Introduction

A core purpose of the PTAB is to strengthen the integrity of the U.S. patent system by cancelling improperly granted claims. The challenged patent, U.S. Patent No. 6,888,181 (“the ’181 patent”), issued due to many material Examiner errors. First, the Examiner overlooked multiple references (e.g., Dakshina and Sugiyama) that were captured in the Examiner’s search, each teaching limitations the Examiner (incorrectly) thought novel, and even anticipating nearly every ’181 patent claim. Second, the Examiner also missed these and other anticipatory references (e.g., Lee), by failing to keyword search the allegedly novel features, misspelling a critical search term, and not searching the U.S. publication database. TSMC’s Petition shows that Lee and Sugiyama each anticipate *all* ’181 patent claims, and Dakshina anticipates all but one claim, establishing its very strong merits.

TSMC’s and its customers’ settled expectations outweigh Marlin’s, further favoring institution. TSMC and its customers expected non-enforcement because the ’181 patent was never asserted in any proceeding before it expired. UMC, an alleged “primary” competitor that owned the patent for most its life, never asserted it. Marlin produces no evidence of prior commercialization, licensing, or marking in TSMC’s “technology space” where Marlin now asserts it (despite not suing TSMC). During this inactivity, TSMC invested billions of dollars to manufacture FinFETs, including for American customers who expect to utilize those chips without incident. Marlin,

a foreign entity who recently acquired the patent, has no comparable expectations.

Institution is warranted and an efficient use of Board resources under *Fintiv* because the '181 patent is not being asserted in litigation, let alone set for an early trial. Still, a threat of enforcement looms, as evidenced by Marlin's infringement claim and its ITC and district court lawsuits on other patents. In response, TSMC has diligently challenged the patent's validity before litigation to provide a true alternative to litigation. This case is also best adjudicated by PTAB judges given the complicated semiconductor technology and the need to correct past examiner errors.

Compelling national security, economic, and public interests also support review. TSMC is the world's largest chip maker, reportedly providing around 90% of the world's advanced chips (i.e., FinFETs). TSMC-1022, 2. Its sophisticated semiconductor technology, which Marlin alleges to infringe the '181 patent, is vital to the U.S. supply chain for a wide range of applications including AI, 5G, health care, and national security. Promoting semiconductor development and the technology it enables (e.g., AI) is an important U.S. goal. TSMC-1023, TSMC-1024. The Office and the Administration have a heightened interest in correcting errors that impact U.S. companies' use of this critical technology.

A holistic assessment of the facts, evidence, circumstances, and relevant considerations (detailed below) confirms that TSMC's Petition should be instituted.

II. Institution Is Warranted In View Of Material Errors By The Examiner.

TSMC's Petition should be instituted to correct material errors associated with the Examiner missing no less than *three anticipatory references*. First, the Examiner overlooked anticipatory references that fell squarely within the Examiner's searches. Specifically, the Examiner's minimal keyword search still captured Dakshina, and the Examiner's classification searches captured Dakshina and Sugiyama. Second, the Examiner: (i) failed to perform keyword searching directed to the allegedly allowable features, (ii) misspelled a critical term in the minimal keyword searching performed, and (iii) failed to adequately search publication databases. *See* TSMC-1037, Decl. of Robert W. Bahr,¹ ¶¶4, 19-39. These errors caused *all three anticipatory references* applied in TSMC's Petition to be missed. *Id.*

A. The Examiner Missed Multiple Anticipatory References that Were Captured by the Examiner's Searches.

The '181 application had 11 claims including independent claims 1 and 6. During examination, the Examiner issued one office action, allowing claims 1-5, rejecting claim 6 (and claims 9-11), and indicating that claims 7-8 recited allowable subject matter. TSMC-1002, 40-41. Original claims 7 and 8 recited (*see id.*, 72):

7. The Tri-gate device of claim 6 wherein said semiconductor core has a first lattice constant that mis-matching a second lattice constant of said strained epitaxy layer.

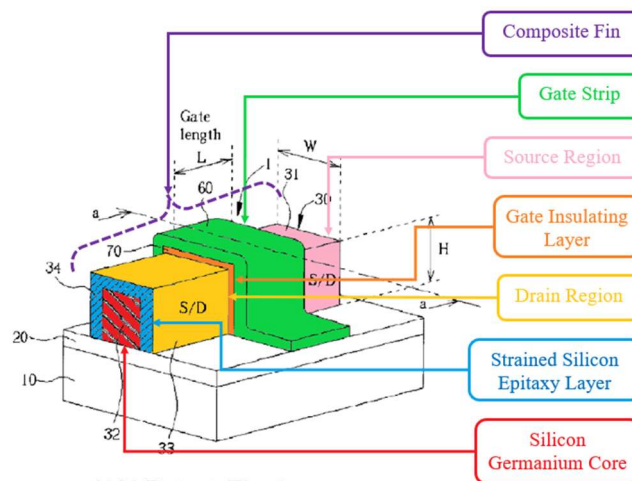
8. The Tri-gate device of claim 6 wherein said semiconductor core consists of silicon germanium.

¹ An expert on USPTO policy, practice, and procedures. TSMC-1037, ¶¶2-7.

Like claim 8, claim 1 recited a silicon germanium core. In response, Applicant amended claim 6 to incorporate claim 7, leading to allowance. *Id.*, 11-14, 28-32.

Annotated claims 1 and 6 and Figure 1 are shown below:

'181 Patent - Claim 1	'181 Patent - Claim 6
1. A three dimensional Triple Gate (Tri-gate) device comprising:	6. A Tri-gate device comprising:
a composite fin structure consisting of a silicon germanium core and a strained silicon epitaxy layer grown from surface of said silicon germanium core;	a composite fin structure consisting of a semiconductor core and a strained epitaxy layer grown from surface of said semiconductor core, said semiconductor core having a first lattice constant that miss-matches a second lattice constant of said strained epitaxy layer;
a gate strip wrapping a portion of said composite fin structure, wherein portions of said composite fin structure not covered by said gate strip constitute source/drain regions of said Tri-gate device; and	a gate strip wrapping a portion of said composite fin structure, wherein portions of said composite fin structure not covered by said gate strip constitute source/drain regions of said Tri-gate device; and
a gate insulating layer interposed between said composite fin structure and said gate strip.	a gate insulating layer interposed between said composite fin structure and said gate strip.



'181 Patent, Fig. 1

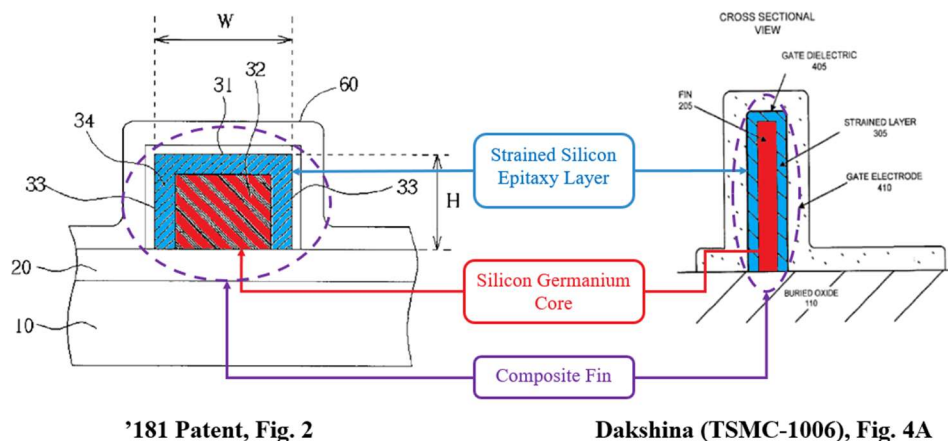
The Examiner apparently considered the “composite fin structure” limitations of claims 1 and 6 as novel only because of multiple, material errors.

1. The Examiner inadequately reviewed the keyword search results, thereby missing key references.

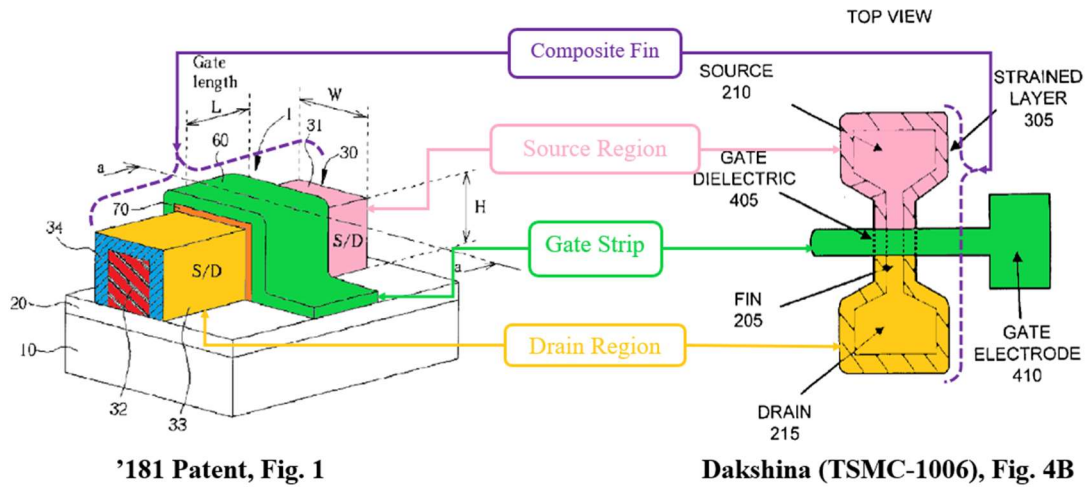
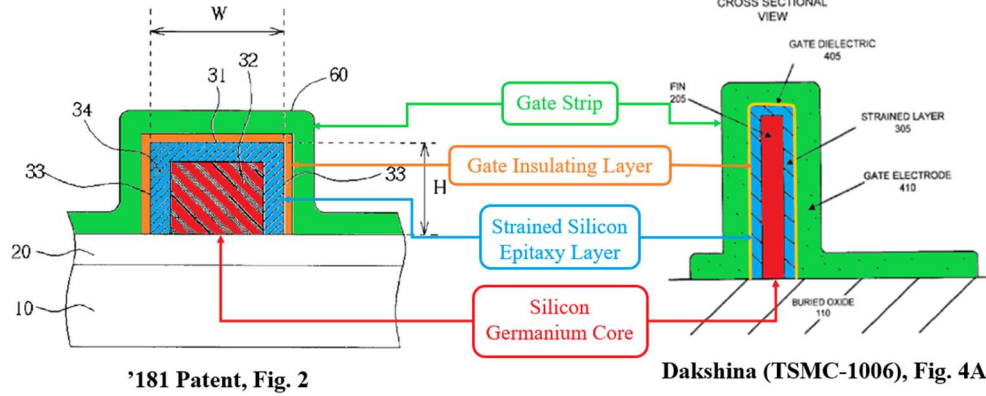
Even though the Examiner’s keyword searching was deficient, it still returned Dakshina, which the Examiner then overlooked. In January 2005, the Examiner searched “finfet” in the USPT database (*see* TSMC-1002, 21), capturing Dakshina:

Examiner Keyword Search			Dakshina		
DB=USPT; PLUR=YES; OP=OR			United States Patent		
			Dakshina-Murthy et al.		
			(10) Patent No.: US 6,803,631 B2		
			(45) Date of Patent: Oct. 12, 2004		
			DISCLOSURE OF THE INVENTION		
L17	6838322	1	L17	Consistent with the present invention, a FinFET transistor is provided that uses a vertically formed strained channel layer that is self-aligned to the fin channel. The strained channel layer may include a crystalline material that is lattice constant mismatched with the crystalline material of the fin of the FinFET. The lattice constant mismatch induces tensile strain within the strained channel layer that increases carrier mobility. Increasing the carrier mobility, in turn, increases the drive current of the FinFET transistor, thus, improving FinFET performance.	
L16	finfet	88	L16		
L15	4996574 and epitax	37	L15		
L14	4996574 and fin	7	L14		
L13	4996574 and finL12	0	L13		
L12	L11 and fin	3	L12		
L11	5338959	26	L11		
L10	4996574	63	L10		

TSMC-1037, ¶36; TSMC-1006, 1:30-41. Yet the Examiner missed that Dakshina taught the allegedly novel “composite fin structure” of claims 1 and 6 as seen below (*see also* Pet., 82-83):



Dakshina even anticipates claims 1 and 6 (and all but one claim) (*see id.*, 80-100):



2. The Examiner conducted an inadequate review of the classification search results.

The Examiner also inadequately reviewed the classification-based search results. In September 2004, the Examiner searched class/subclasses 257/331-369, which encompassed both Dakshina's pre-grant publication and Sugiyama:

SEARCHED				SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
Class	Subclass	Date	Examiner		DATE	EXMR
257	331-369	9/3/2004	FA	WEST	9/3/2004	FA

United States Patent Sugiyama et al.		(10) Patent No.: US 6,774,390 B2 (45) Date of Patent: Aug. 10, 2004
(52) U.S. Cl.	257/19; 257/45; 257/18; 257/20; 257/347	

United States Patent Application Publication Dakshina-Murthy et al.		(10) Pub. No.: US 2004/0145019 A1 (45) Pub. Date: Jul. 29, 2004
(52) U.S. Cl.	257/349	

TSMC-1002, 45; TSMC-1005, 1; TSMC-1038, 1; TSMC-1037, ¶¶37-39. In January

2005, while inexplicably not searching subclasses 257/331-369 again, the Examiner instead searched just 257/192,² but *again* missed Dakshina as its issued patent³:

SEARCHED			
Class	Subclass	Date	Examiner
257	192	[Sie: 1/5/2005] 1/5/2004	FA

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
WEST	1/5/2005	FA

United States Patent Dakshina-Murthy et al. (52) U.S. Cl. 257/349; 257/192		(10) Patent No.: US 6,803,631 B2 (45) Date of Patent: Oct. 12, 2004
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TSMC-1002, 18; TSMC-1037, ¶39. Thus, the Examiner conducted *three* different searches (the “finfet” keyword search and two different classification searches) that returned Dakshina, but inexplicably overlooked its invalidating teachings each time.

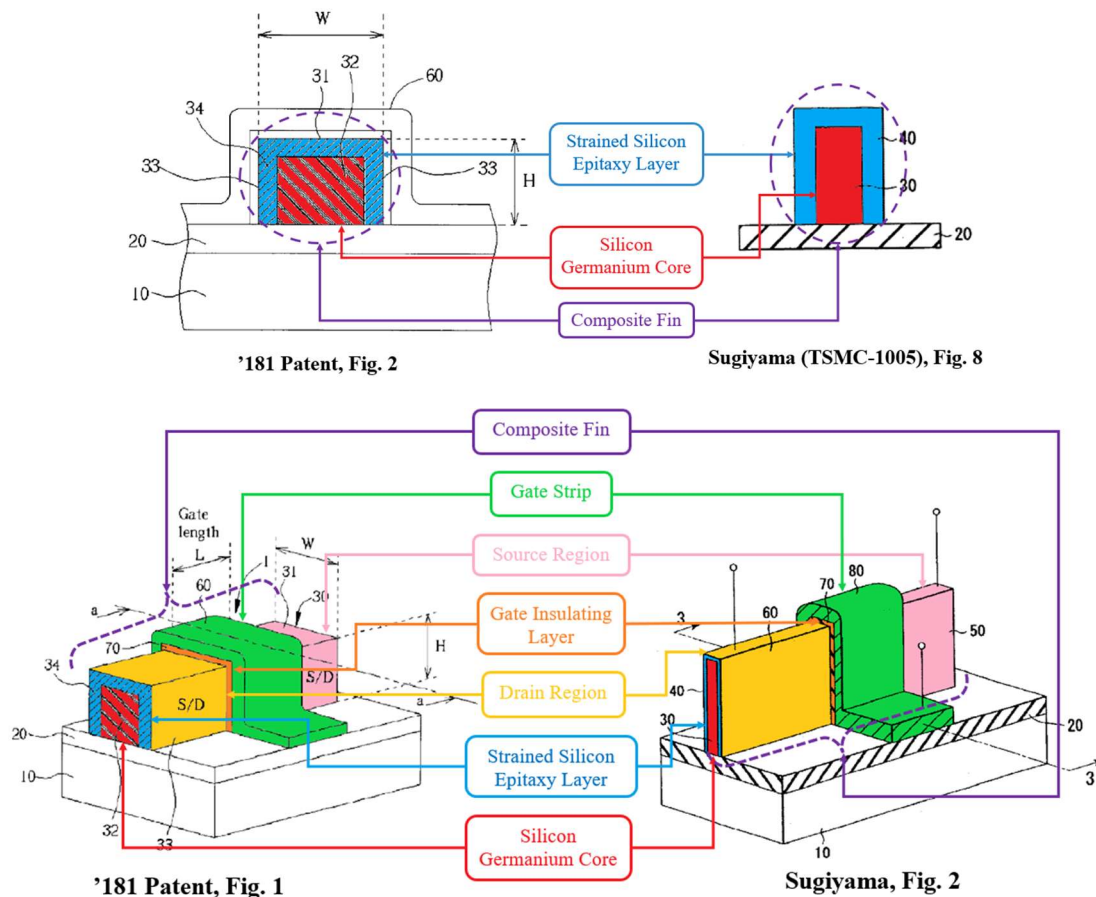
A “Field of Search” is “*A complete search of a subclass, including all United States...documents...and other publications placed therein.*” MPEP §719.05 (Eighth Ed., Rev. 2, May 2004) (emph. in orig.). The “Search Notes” must reflect any limitations on this search/review, but no such notes exist for the classification searches, confirming they captured Sugiyama and Dakshina. TSMC-1037, ¶¶15-18.

The September 2004 classification search also captured Sugiyama (*id.*, ¶32), yet its disclosure of the allegedly novel composite fin structure (*see* Pet., 56-58) and

² The Examiner also failed to search the classes/subclasses in which two of three references cited by the Examiner were classified. TSMC-1037, ¶¶19-20.

³ The “1/5/2004” date in the search notes should plainly be “1/5/2005.” *Id.*, ¶38.

its anticipation of claims 1 and 6 (*see* Pet., 54-78) were likewise overlooked:



B. The Examiner Failed to Conduct a Reasonable Search.

1. The Examiner failed to search the limitations upon which allowance was based.

The Examiner failed to conduct a keyword search for the apparently allowable features, which would have identified all three anticipatory references. In the January 2005 search, **15 of 17** queries inexplicably used an unduly narrow forward-citation limiter that only identifies U.S. patents that cite the specific reference being searched. TSMC-1037, ¶¶21, 26; TSMC-1002, 21-22. Furthermore, the only other **two** keyword searches did not even search the allegedly allowable features.

As outlined above, the Examiner considered original claims 7 and 8 to be allowable, shown below with key features highlighted:

7. The Tri-gate device of claim 6 wherein said semiconductor core has a first **lattice constant** that mismatching a second **lattice constant** of said **strained epitaxy** layer.
8. The Tri-gate device of claim 6 wherein said semiconductor core consists of **silicon germanium**.

TSMC-1002, 41, 72. Like claim 8, allowed claim 1 recited “a composite fin structure consisting of a silicon germanium core.” But the Examiner *never searched these key features*. Keyword searching “**lattice constant**,” “**strained**,” **epitax**\$5, or “**silicon germanium**”/“**SiGe**” (alone or in combination) in the USPT and PGPB databases would have yielded Dakshina, Sugiyama, and Lee’647 (TSMC-1037, ¶¶30-32):

(19) **United States**
(12) **Patent Application Publication** (10) Pub. No.: US 2004/0256647 A1
Lee et al. (43) Pub. Date: Dec. 23, 2004

enhancing drive current. The silicon fin channel of the disclosed finFET device is a **strained silicon fin** channel, comprising a **strained silicon layer** deposited on a seed fin having **different lattice constant**, for example, a silicon layer deposited on a **silicon germanium seed fin**, or a carbon doped silicon layer deposited on a silicon seed fin. The **lattice mismatch** between the silicon layer and the seed fin generates the strained silicon fin channel in the disclosed finFET device to improve hole and electron mobility enhancement, in addition to short channel effect reduction characteristic inherently in a finFET device.

...

[0041] The **epitaxial channel silicon layer 11** or **11'** grown on the relaxed **silicon germanium seed fin 10** will be tensilely **strained** because the **lattice constant** of **silicon** is smaller than that of **silicon germanium**. Due to this tensile

United States Patent
Dakshina-Murthy et al.

(10) Patent No.: US 6,803,631 B2
(45) Date of Patent: Oct. 12, 2004

DISCLOSURE OF THE INVENTION

Consistent with the present invention, a **FinFET** transistor is provided that uses a vertically formed strained channel layer that is self-aligned to the fin channel. The strained channel layer may include a crystalline material that is lattice constant mismatched with the crystalline material of the fin of the FinFET. The **lattice constant mismatch** induces tensile strain within the **strained channel layer** that increases carrier mobility. Increasing the carrier mobility, in turn, increases the drive current of the FinFET transistor, thus, improving FinFET performance.

United States Patent
Sugiyama et al.

(10) Patent No.: US 6,774,390 B2
(45) Date of Patent: Aug. 10, 2004

The present invention has been made to solve this problem, relates to a MISFET using, as a channel layer, a second semiconductor layer such as a **strained Si layer** which is joined to a first semiconductor layer such as a **SiGe** crystal layer formed on an insulating layer, has a **lattice constant different** from that of the first semiconductor layer, and has a stress strain in crystal lattices, and also relates to a CMIS circuit which is combined with the MISFET.

...

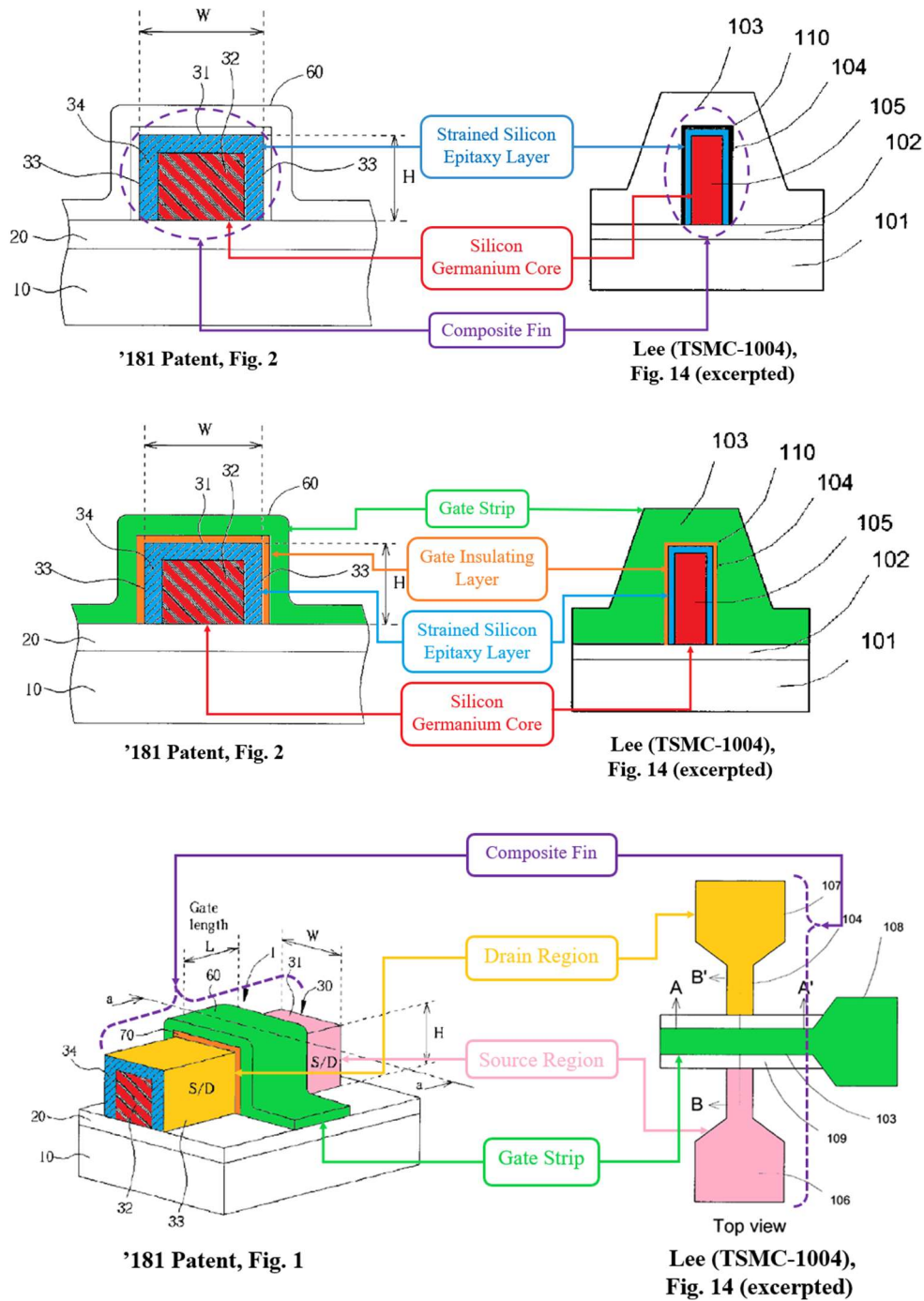
As shown in FIG. 8, the mask **13** and thermal oxide layer **14** are removed by wet etching or the like. After surface processing, a Si layer is grown to a thickness of 7 nm on the surface of the **SiGe** crystal layer **30** by **epitaxial growth**. The **Si layer** is a **strained Si layer 40** as the second semiconductor layer. The thickness of the **strained Si layer 40** is desirably

Fin channel layer **105** may include a crystalline material with a **lattice constant larger than the lattice constant** of a crystalline material selected for a strained channel layer (described with respect to FIGS. 3A and 3B below). If, for example, **silicon is selected for the strained channel layer**, fin channel layer **105** may include a crystalline material with a **lattice constant large than the lattice constant of silicon**. Fin channel layer **105** may include, for example, **Si_{1-x}Ge_x** with x approximately equal to 0.7. Other values of x may be

TSMC-1039, Abstract, ¶[0041]; TSMC-1005, 5:35-43, 9:44-50; TSMC-1006, 1:32-

40, 3:19-34, 3:57-4:9.

As shown above, both Dakshina and Sugiyama disclose the allegedly novel composite fin structure, and also anticipate most '181 claims. Lee does the same:



See Pet., 14-43.

2. The Examiner failed to adequately search publications, and misspelled important search terms.

The Examiner's only query of U.S. patent application publications using the PGPB database in his January 2005 search (TSMC-1002, 22) was **futile** because it encompassed a forward citation of USP 6,764,884:

DB=PGPB; PLUR=YES; OP=OR			
L4	L3	0	L4
DB=USPT; PLUR=YES; OP=OR			
L3	11 and epitax\$5	0	L3
L2	"fin" same ("tripple gate" or "tri-gate")	0	L2
L1	6764884	1	L1

The PGPB database includes only published U.S. patent applications *which do not even cite prior art* (TSMC-1037, ¶¶24-25), so this search **inevitably returned 0 hits** (*id.*, ¶35). Given this defective search strategy that would always return zero hits, the Examiner effectively excluded U.S. application publications, contrary to the MPEP. TSMC-1037, ¶¶13-14 (citing MPEP §904.02 (Eighth Ed., Rev. 2, May 2004) (stating that publications “must be considered”)).

Moreover, the Examiner also misspelled the keyword “triple gate”:

DB=USPT; PLUR=YES; OP=OR			
L3	11 and epitax\$5	0	L3
L2	"fin" same ("tripple gate" or "tri-gate")	0	L2
L1	6764884	1	L1

“tripple” misspelling → “0” search results

TSMC-1002, 22; TSMC-1037, ¶33. Correctly spelling “triple gate” would have captured the underlying published application corresponding to Lee:

[0093] FIG. 14 further shows the cross section BB', cutting through the triple gate 103 of the finFET structure. The cross section BB' cuts through the seed fin layer 105 on a insulator layer 102 and a substrate 101, the strained silicon channel 104 and the gate dielectric 110. The triple gate 103 also covers the top section of the fin structure, with the spacer 109 to isolate the triple gate 103 from the silicon channel 104.

TSMC-1039, ¶[0093]; *see also id.*, ¶¶[0037], [0091], [0092]; TSMC-1037, ¶34.

These compound, material examination errors warrant institution. *See, e.g., Samsung Elecs Co., Ltd. v. Wilus Institute of Standards and Tech., Inc.*, IPR2025-01043, Paper-9, 20-27 (discussing flawed text and classification code searching) & Paper-11 (denying PO's request for discretionary denial); *Anthony, Inc. v. ControlTec, LLC*, IPR2025-00559, Paper-12 (Jul. 16, 2025) (finding material prosecution error where examiner failed to locate a petition reference).

III. Institution Is Warranted Because Of The Strength Of The Petition, Which Invalidates All Claims Over Three Separate Primary References, Each Of Which Is Anticipatory For All (Or Nearly All) Claims.

The merits of TSMC's Petition are very strong, well-supported, and well-reasoned, and the invalidity positions are straightforward. The Petition presents three separate anticipation grounds over Lee, Sugiyama, and Dakshina, respectively; two (Lee and Sugiyama) anticipate all claims and the other (Dakshina) anticipates all but one claim. Pet., 14-43, 54-78, 80-100. The side-by-side figures provided above show the striking similarities between the alleged invention and each of these references. Marlin identifies no substantive deficiencies in any of these references.

IV. Institution Is Warranted Because The Settled Expectations Of Petitioner And Others Outweigh Marlin's Alleged Expectations.

Marlin's settled expectations rely on the patent issuing many years ago and that alone effectively trumping all other considerations. Paper-6, 2-9. Disregarding the expectations of TSMC, its customers, and the public is not balanced or fair. TSMC, its customers, and the public have "settled expectations" that heavily outweigh Marlin's, especially for an expired, unasserted patent.

Since acquiring the '181 patent in June 2021 (TSMC-1025), Marlin began an enforcement campaign against the semiconductor industry, including TSMC's customers. Ex. 2104, 1. And Marlin has since asserted patents against TSMC in the ITC, seeking an exclusion order. The Petition can resolve patentability of the '181 patent's claims before Marlin sues TSMC or its customers and disturbs the parties' well-settled expectations that the '181 patent is dormant.

First, TSMC and its customers had settled expectations that the '181 patent would not be asserted given the prior owner UMC's inaction for 16 years. TSMC has been engaged in FinFET manufacture since 2013. TSMC-1026, 3. For over a decade after, TSMC invested billions in fabrication facilities to manufacture chips using FinFET technology, and its customers invested significant resources based on that technology. TSMC-1027. During this time, UMC, who Marlin claims is "TSMC's main competitor" (Paper-6, 3), remained silent, creating settled expectations for TSMC and its customers that the patent would remain dormant.

Marlin's recent activities cannot unwind settled expectations through inaction.

In analogous bodies of law, the expectations of others would exceed those of a new property owner under such circumstances. *See* Restatement (First) of Prop. §459 cmt. a (1993) (“Through lapse of time old rights become obscure. A long continued use raises reasonable expectations of its continuance.”); *Anaheim Gardens, L.P. v. United States*, 953 F.3d 1344, 1350-51 (Fed. Cir. 2020); *Nordlinger v. Hahn*, 505 U.S. 1, 12-13 (1992) (“[A]n existing owner rationally may be thought to have vested expectations in his property or home that are more deserving of protection than the anticipatory expectations of a new owner at the point of purchase.”).

Second, despite holding confidential information as the Patent Owner, Marlin has yet to produce any evidence that the '181 patent was ever “commercialized, asserted, marked, licensed, or otherwise applied” in the same “particular technology space.” This weighs against Marlin's “settled expectations.” *Shenzhen Tuozhu Tech. Co., Ltd. v. Stratasys, Inc.*, IPR2025-00531, Paper-10, 3 (July 17, 2025).

The '181 patent has never been asserted in any proceeding. Marlin points to UMC as “TSMC's main business competitor” (Paper-6, 1) but cites no evidence that UMC enforced or demanded a license for the '181 patent against TSMC (or anyone) during UMC's 16 years of ownership. That the '181 patent was never asserted in any proceeding *against anyone during its entire lifetime* creates TSMC's settled expectation that it does not apply to TSMC's activities. *See Google v. Sandpiper*

CDN, IPR2025-00806, Paper-13, 2 (Sept. 12, 2025) (referring, despite patent being “in force for many years,” where patent expired prior to assertion); *Apple v. Allani*, IPR2025-00856, Paper-11, 3 (Sept. 5, 2025) (referring, despite strong settled expectations based on patent age, in part due to patent expiring before assertion). Marlin's reliance on *Dabico Airport* (Paper-6, 2) based on patent age is misplaced because, among other reasons, that case did not involve an expired patent as here.

Marlin also misleadingly argues that the '181 patent “has been commercialized, at least in the form of licensing” with Intel and Samsung Electronics. Paper-6, 4-5. Marlin has not produced these licenses here such that Petitioner can review their terms ahead of this filing, nor has Petitioner been authorized to depose Mr. Ahern regarding his bare assertion of licenses. Ex. 2104; Ex. 3101. Marlin also has not shown that any purported licensees marked products with the '181 patent.

When Marlin acquired patents (including the '181 patent) that had never been asserted in any proceeding with the intention of enforcing them, they had to expect to have their validity challenged. *See Anaheim Gardens*, 953 F.3d at 1350-51 (“timing” of a property purchase and “knowledge of the purchaser” are relevant in assessing purchaser’s investment-backed expectations); *Celgene Corp. v. Peter*, 931 F.3d 1342, 1361-63 (Fed. Cir. 2019) (patent owners know their patents may be subject to post-issuance reconsideration proceedings).

Marlin's attacks on TSMC's strong settled expectations are unpersuasive. Relying on *iRhythm Tech., Inc. v. Welch Allyn, Inc.*, IPR2025-00363, Marlin says that TSMC's knowledge of the '181 patent through prosecution of its own patents favors denial. Paper-6, 4. But *iRhythm* is inapposite. There, the parties were already engaged in litigation, and the Petitioner failed to file any stipulation to eliminate overlap between the IPR and the district court litigation. *Id.*, Paper-7, 34. And, the Petitioner identified no examiner errors and relied heavily on the "General Knowledge" of a POSA (*id.*, 5-6) counter to PTAB guidance. USPTO Memorandum issued July 31, 2025 titled, "Enforcement and Non-Waiver of 37 C.F.R. §42.104(b)(4) and Permissible Uses of General Knowledge in Inter Partes Reviews." By contrast, here, there is no co-pending litigation, three solid §102 references not relying on "general knowledge," and material examiner errors as outlined above.

Marlin tries to rely on previous patent owner expectations and license negotiations between the parties beginning in 2024 as weighing against TSMC's settled expectations. Paper-6, 5-6 (citing *DataDome S.A. v. Arkose Labs Holdings, Inc.* IPR2025-00693, Paper-13, 7). Marlin's reliance on *DataDome* is unavailing. First, in *DataDome*, there was a parallel proceeding involving the challenged patents and the Petitioner did not even argue that the Examiner had materially erred during prosecution. *Id.*, Paper-6, 7; *see also id.*, Paper-39, 26-31. Both of these factors differ from the present case and weigh in favor of institution. The '181 patent also expired

roughly six months before Marlin’s alleged license proposal in August 2024, by which time TSMC fully expected that the expired ’181 patent would not apply.

Moreover, TSMC filed this Petition within a year after receiving that licensing proposal and less than 6 months after Marlin asserted other patents against TSMC in court. TSMC was far more diligent than the *DataDome* petitioner who waited over two years after receiving an initial demand and 15 months after refusing a license to file its IPR Petition. *Id.*, Paper-13, 7; *see also id.*, Pet’r. Ex. 1013 (January 11, 2023 letter seeking license on one of the challenged patents).

V. Institution Is An Efficient Use Of Board Resources.

Institution is warranted as an efficient use of Board resources because there is no parallel litigation involving the ’181 patent, making the PTAB the most efficient forum to resolve this dispute. *See, e.g., Intas Pharms. Ltd. v. Atossa Therapeutics, Inc.*, IPR2025-00799, Paper-12, 2-3 (Aug. 12, 2025) (“[T]he parties are not involved in a parallel proceeding involving the challenged patents. As a result, there is no concern of inconsistent outcomes or significant duplication of efforts....”). No other tribunal is set to resolve the merits of this dispute, removing any risk of duplicated efforts, inconsistent decisions, or unnecessary expense for the parties.

Marlin sidesteps this important fact, arguing it is not dispositive because the petitions in *Intel Corp. v. Proxense LLC* were still discretionarily denied despite having no *trial date*. Paper-6, 7-8 (citing IPR2025-00327, -00328, -00329, Paper-

12, 2 (June 25, 2025)). However, in *Intel*, the decision to discretionarily deny was based upon Petitioner's failure to "provide any persuasive reasoning as to why [IPR] is an appropriate use of Board resources." *Intel*, Paper-12, 2. Here, TSMC presents several compelling reasons why IPR is an appropriate use of resources, including addressing the Examiner's material errors and resolving the parties' dispute while avoiding "unnecessary and counterproductive litigation costs" before Marlin sues TSMC. November 2019 Consolidated Trial Guide, 56 (quoting H.R. Rep. No. 112-98, pt. 1, 40 (2010), 2011 U.S.C.C.A.N. 67, 69 (explaining the rationale underlying the AIA)). With no parallel litigation and every factor weighing heavily in favor of institution other than the age of the patent, allowing institution here would be a good use of the Office's resources.

VI. National Security, Economic, And Public Interest Considerations Warrant Institution.

Marlin acknowledges it has alleged infringement of the '181 patent by TSMC. Ex. 2104. Marlin's threat to weaponize the '181 patent undermines the U.S. semiconductor supply chain, harming priorities that this Administration has made clear are vital to U.S. economic interests and national security. TSMC-1023, 3; TSMC-1024, 1. TSMC's FinFET fabrication capabilities are vital to leading U.S. companies (e.g., Apple, NVIDIA, Amazon). In particular, TSMC's 5nm processing node technology supports U.S. advanced semiconductor R&D in industries such as AI, health care, and national security and defense. TSMC-1028, 18-19. Promoting

these emerging industries advances the Administration's priorities. TSMC-1023, 3; TSMC-1024, 1. The threat to these industries by Marlin's litigation tactics make this IPR an appropriate and efficient use of the Office's resources and expertise.

Indeed, the U.S. government has recognized the importance of AI to the national security, and TSMC is important to the U.S.'s AI-dominance strategy. TSMC-1029; TSMC-1030. TSMC is a global AI technology leader "steering" the AI wave for tech giants, producing "advanced processors that Nvidia (AMD)[] and Apple[] rely on to bring AI to life." TSMC-1031, 2. These include chips driving AI systems, e.g., NVIDIA's H100 manufactured with TSMC's 4nm process, and NVIDIA's latest B100 and B200 chips that can only be manufactured using TSMC's 3nm process. TSMC-1032, 2. The plan to build the U.S. Department of Energy's largest AI supercomputer will include 100,000 Blackwell GPUs, which use TSMC's 4nm process. TSMC-1033; TSMC-1034. Moreover, healthcare is a key area of projected growth in the AI semiconductor market, where the demand for "advanced chips—TSMC's specialty—will continue to surge." TSMC-1035, 5. Burdening access to TSMC-made advanced semiconductors could create a catastrophic single-point failure for medical R&D, causing "direct effects on future patient care" and "far-reaching consequences" for the development of life-saving technologies. TSMC-1040.

Instead, Marlin paints itself as protector of local industries. Paper-6, 10-11.

The facts belie this strawman argument. Marlin does not practice the '181 patent nor any patent. No evidence exists that Marlin, a foreign entity, has invested in U.S. semiconductor technology, except by asserting acquired patents. Marlin's assertion of its patents against U.S.-based companies (e.g., Apple, Qualcomm, Broadcom) makes its claim of protecting "local industry" ring hollow.

Finally, casting TSMC as a "foreign entity" that "import[s] infringing products" and must be protected against twists the facts beyond recognition. There is zero evidence, other than a bare, unsupported statement from an interested party, Mr. Ahern, that any TSMC product infringes the '181 patent. Additionally, Marlin ignores TSMC's commitment to invest \$165 billion in manufacturing facilities in the United States in support of this Administration's goal to onshore semiconductor manufacturing to bolster U.S. economic and national security interests. TSMC-1023, 3. Indeed, TSMC's Arizona facilities are already producing 4nm chips for American customers. TSMC-1036, 2. Marlin's enforcement campaign against TSMC seeks to damage the core supply chain of semiconductor chips to the United States. National security, economic, and public interest considerations therefore warrant institution.

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Respectfully submitted,

By: s/Michael Houston/

Michael R. Houston
Reg. No. 58,486
FOLEY & LARDNER LLP

321 N Clark St Ste 3000

Chicago, IL 60654

Tel: (312) 832-4378

Fax: (312) 832-4700

Counsel for Petitioner

CERTIFICATE OF SERVICE

The undersigned hereby certifies that copies of the foregoing
**PETITIONER'S OPPOSITION TO PATENT OWNER'S
DISCRETIONARY DENIAL REQUEST and Exhibits 1022-1040** were served
on November 21, 2025 by filing in the PTACTS system and via email delivery
directed to the attorneys of record for Patent Owner at the addresses listed below:

WAMeunier@mintz.com
ARizk@mintz.com
MTRenaud@mintz.com
RDokhanchy@mintz.com
TAGoma@mintz.com
Mintz-Marlin-IPRs@mintz.com

Patent Owner has consented to electronic service at the aforementioned email
addresses. Paper-4, at 1-2.

Date: November 21, 2025

By: s/Michael Houston/

Michael R. Houston
Reg. No. 58,486
FOLEY & LARDNER LLP
321 N Clark St Ste 3000
Chicago, IL 60654
Tel: (312) 832-4378
Fax: (312) 832-4700

Counsel for Petitioner