

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.,
Petitioner

v.

QUICKER CONNECTIONS LLC,
Patent Owner

IPR2025-01088
U.S. Patent No. 7,061,859

PATENT OWNER'S PRELIMINARY RESPONSE

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TABLE OF AUTHORITIES

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EXHIBIT LIST

Ex.	Description
2001	Complaint for Copyright and Patent Infringement in <i>Cisco Systems, Inc. v. Arista Networks, Inc.</i> , No. 5:14-cv-05344-BLF (N.D. Cal.)
2002	Email from Petitioner's counsel providing Orckit's 2005 SEC Form 20-F filing, dated Apr. 25, 2025
2003	Orckit's 2005 SEC Form 20-F filing
2004	Petitioner's U.S. Patent No. 7,349,348
2005	Prosecution History for Petitioner's U.S. Patent No. 7,349,348
2006	Petitioner's U.S. Patent No. 6,965,558
2007	Prosecution History for Petitioner's U.S. Patent No. 6,965,558
2008	Petitioner's U.S. Patent No. 7,602,706
2009	Prosecution History for Petitioner's U.S. Patent No. 7,602,706
2010	Petitioner's U.S. Patent No. 8,886,831
2011	Prosecution History for Petitioner's U.S. Patent No. 8,886,831
2012	Petitioner's U.S. Patent No. 8,300,523
2013	Prosecution History for Petitioner's U.S. Patent No. 8,300,523
2014	IPWatchdog article, <i>Stewart Says USPTO Wants Early Validity Challenges, Not Late IPRs</i> , dated June 10, 2025 (available at https://ipwatchdog.com/2025/06/10/189554/id=189554/)
2015	Cisco's Partial Motion to Dismiss Quicker Connections' Complaint in EDTX-Litigation, dated Mar. 3, 2025
2016	Google Patents Assignee Search Results
2017	Google Patents Assignee Search Results
2018	Quicker Connections' First Amended Complaint in EDTX-Litigation, dated Mar. 31, 2025
2019	L. Spencer letter to E. Robinson RE: Deficiencies in P.R. 3-1 and 3-2 Disclosures, dated Apr. 29, 2025
2020	RTT News article, <i>Corrigent Signs 15-Yr Agreement With Media Broadcast For Deutsche Telekom's Customer In Germany - Quick Facts</i> , Feb. 6, 2008 (available at https://www.rttnews.com/472822/corrigent-signs-15-yr-agreement-with-media-broadcast-for-deutsche-telekom-s-customer-in-germany-quick-facts.aspx)
2021	Forbes article, <i>The silicon spin</i> , Feb. 10, 2000 (updated June 6, 2013) (available at https://www.forbes.com/2000/02/10/mu3.html)
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2036	Letter accompanying Cisco’s fourth production volume, dated July 31, 2025
2037	Service email accompanying Quicker Connections’ Infringement Contentions and first production volume, dated Mar. 12, 2025
2038	Service email accompanying Quicker Connections’ second production volume, dated July 31, 2025
2039	Reserved
2040	Cisco’s notice of third-party subpoena to Nokia of America Corporation, dated Apr. 14, 2025
2041	Service email accompanying Nokia’s third-party production, dated June 3, 2025
2042	Letter accompanying Orckit Communications’ third-party production, dated Aug. 1, 2025
2043	Quicker Connections’ PR 3-1 and 3-2 Disclosures, dated Mar. 12, 2025
2044	Service email accompanying Cisco’s Invalidity Contentions, dated May 7, 2025
2045	Quicker Connections’ First Set of RFAs to Cisco (Nos. 1-9), dated July 11, 2025
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2056	H. Laidlaw letter to L. Spencer RE: Document Categories, dated June 13, 2025
2057	E. Weber letter to E. Robinson RE: Document Categories, dated June 16, 2025
2058	Declaration of Dr. Nenad Medvidović in Support of Patent Owner's Preliminary Response
2059	Curriculum Vitae of Dr. Medvidović
2060	Declaration of Harold S. Laidlaw in Support of <i>Pro Hac Vice</i> Admission
2061	Webster's Third New International Dictionary, Unabridged (1981) (Excerpted)
2062	Merriam-Webster's Dictionary, definition of "Superimpose." https://www.merriam-webster.com/dictionary/superimpose (last viewed September 24, 2025)

I. INTRODUCTION

The Board should deny the Petition for *Inter Partes* Review of U.S. Patent No. 7,061,859 (“the ’859 Patent”) because Petitioner Cisco Systems, Inc. (“Petitioner” or “Cisco”) fails to demonstrate a reasonable likelihood that any challenged claim is not patentable.

The sole ground on which the Petition relies is alleged obviousness of the challenged claims over Japanese Patent Publication No. JP2001053772A to Omichi (“Omichi,” Ex. 1005). The Petition fails to carry its burden of establishing that any of the ’859 Patent’s claims are obvious over this reference.

First, Omichi does not teach or render obvious the claimed “general mask” of the ’859 Patent. The ’859 Patent’s general mask is a sequence of bits corresponding to network link segments, in which each bit is set to “1” if a link segment is *unreachable* and “0” if it is *reachable*. As reflected in the plain language of the claim and the disclosures of the Patent specification, this means that *every link* in a segment cut off from the rest of the network by non-adjacent link failures is set to “1” to reflect its being unreachable. Ex. 1001 5:32-33.

Omichi’s link failure table, though relied on by Petitioners for the claimed general mask, uses bits only to reflect link *failures* without accounting for link *reachability*. Omichi’s link failure table does not adjust bits for segments rendered unreachable by link failures (such as when two non-adjacent links fail and

disconnect a portion of the network links) and thus does not teach or suggest the use of the claimed general mask that reflects link reachability.¹ Ex. 1005 at [0036]. The Petition thus fails to show a reasonable likelihood of prevailing as to the obviousness of the claimed general mask, which is an element of every claim of the '859 Patent.

Second, Omichi fails to teach or suggest the claimed “superimposing” operation. Despite using bits to represent link failures and desired paths in a ring network, Omichi fails to disclose the use of bitwise Boolean operations, such as bitwise AND, to overlay the entries of its respective tables. In view of (i) the conspicuous absence of such a disclosure to a POSITA, (ii) disclosures in Omichi suggestive of the serial comparison of individual bits, such as the flowchart of Figure 7 and the description of the link failure table as a “table”, and (iii) the options to implement the “comparison” operation described of Omichi without bitwise binary operations, the Petition’s argument that Omichi renders the use of a bitwise AND operation obvious in order to meet the “superimposing” element of each '859 Patent claim fails.

¹ The Petition’s argument that Omichi renders this element obvious is purely conclusory and does not substantively address the lack of such disclosure in Omichi. A POSITA would also not be motivated to modify Omichi to include such a data structure.

Lastly, for at least dependent claims 3, 6, 9, and 12, Omichi fails to teach or suggest refraining from sending data in the event that a node or segment is unreachable from both a primary and alternate path around the network ring. Omichi discloses only a *change in direction* rather than a *withholding* of data and implicitly reflects an assumption that link errors will be infrequent and unlikely to result in the complete disconnection of two paths around a ring. A POSITA viewing Omichi would not be motivated to modify it to account for failure conditions that Omichi does not.

For at least these reasons, the Board should deny institution of the Petition.

II. LEGAL STANDARDS FOR INSTITUTION

The Petition must demonstrate a reasonable likelihood that at least one of the Challenged Claims is unpatentable for the Board to institute review. 35 U.S.C. §314(a); 37 C.F.R. §42.108(c). The Board “will not take on the role of advocate for a party, trying to make out a case the party has not adequately stated.” Standing Order ¶121.5.2 (B.P.A.I. Mar. 8, 2011). Rather, it is Petitioner’s duty to provide sufficient grounds for the institution of a review “focus[ing] on concise, well organized, easy-to-follow arguments supported by readily identifiable evidence of record.” *Cisco Sys., Inc. v. C-Cation Tech, LLC*, IPR2014-00454, Paper No. 12 at 11 (PTAB Aug. 29, 2014).

For the purpose of this POPR, it is sufficient to establish that the Petition fails to demonstrate a reasonable likelihood that the independent claims are unpatentable. As shown below, the Petition fails to establish a reasonable likelihood that Petitioner will prevail on any independent claim. A trial therefore should not be instituted.

III. OVERVIEW OF THE '859 PATENT

The '859 Patent, entitled “Fast Protection in Ring Topologies,” claims methods and devices relating to packet routing in response to fault detection in bidirectional ring networks – i.e., networks in which (i) each node is connected to exactly one node on either side, forming a closed loop, and (ii) in which data can flow in either direction (i.e., either clockwise or counterclockwise).

FIG. 1

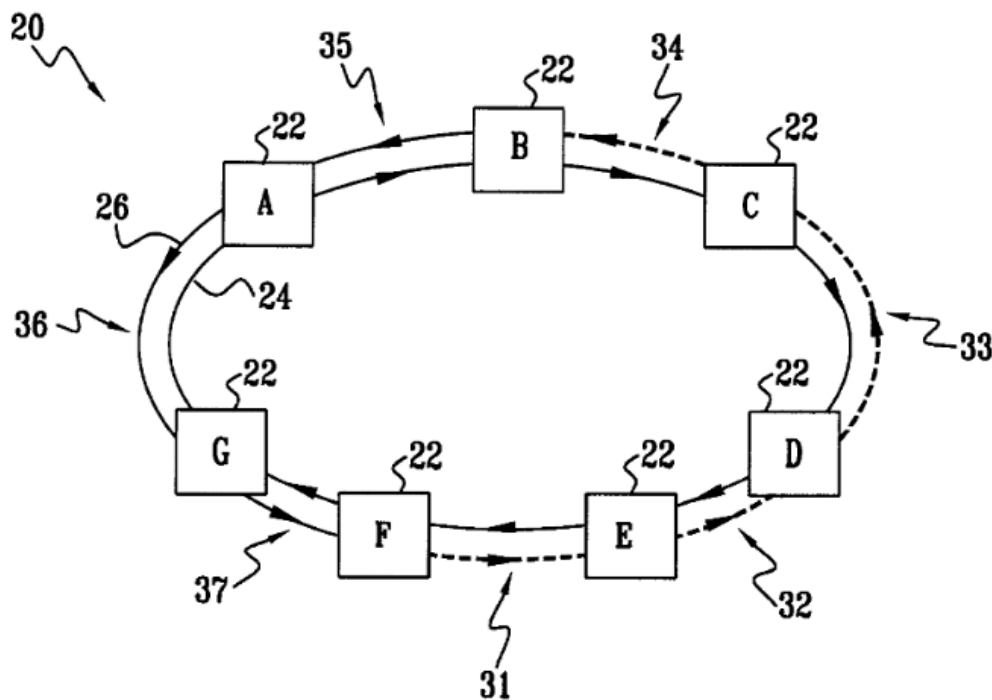


FIG. 1 of the '859 Patent – an example of a bidirectional ring network topology. (Ex. 1001 FIG 1.)

In ring networks like those of the '859 Patent, communication between any two nodes² X and Y can take one of two alternate paths (clockwise or counterclockwise), with traffic routed through intermediate nodes if X and Y are not adjacent to each other on the chosen path.

Because traffic can flow between either of two paths between a first node X and a second node Y, in the event of a bidirectional link failure that does not disconnect both possible routes from X to Y, traffic can be rerouted from a first (default) direction that would traverse the failed link to an alternative path going the other direction. If each node is aware of all link failures, then each node will also have the information to route packets appropriately to take the non-failed path (if one exists) to a given node or, if no such path exists (due to multiple link failures, at least one in each direction) the origin node can refrain from sending undeliverable packets. Ex. 1001 2:31-47.

² “Nodes” (letters A-G in '859 Patent FIG. 1) generally refers to switching equipment either connected to computers (“access nodes”) or else serving as a gateway to other networks (“gateway nodes”) in the ring network topology, while “segments” (Nos. 1-37 in FIG. 1) refers to the links between the nodes. Ex. 1001 at 3:55-57, 4:7-18. Ex. 2058 ¶ 48.

The '859 Patent claims methods and systems for minimizing packet loss and packet misrouting in a bidirectional ring network by having each node maintain a *general mask* reflecting information about the reachability of links in the network in view of any link failures in the network³ and a *specific mask* reflecting the route (i.e. set of links) that, by default, packets would take from the originating node to a destination node. Ex. 1001 4:38-46. Ex. 2058 ¶ 52.

In order to determine the routing of a packet, the general and specific masks of the '859 Patent are *superimposed* (i.e., the whole of one mask is compared to the whole of the other), for example with a bitwise Boolean AND operation. Ex. 1001 2:31-34, 4:64-5:1. This operation determines the overlap (if any) of unreachable links and links in the default routing path. If there is such an overlap, then either the data should be conveyed using the alternate routing path (if the destination is reachable in the other direction) or not conveyed at all the data (if there are unreachable links in both directions unreachable). Ex. 1001 5:8-21; Cls. 3-6, 9-12. Ex. 2048 ¶ 53.

The construction of the masks and the use of a superimposition operation allow for fast and efficient determination of the need to reroute or refrain from

³ Link failures are detected and reported via band network fault detection communication mechanisms known in the art. Ex. 1001 1:57-60.

sending packets along a given path, which is especially valuable in the context of packet-based networking where low latency (and hence low overhead of routing determinations) is highly desirable. Ex. 2058 ¶¶ 55-56.

A. Bitwise Operations

Both the general mask the and the specific mask of the '859 Patent are *bitmaps* or *bit vectors* (a data structure often representable internally as an unsigned integer, depending on the size of the bitmaps and of the size of integer mathematics⁴ defined in the relevant system architecture) comprising a sequence of “0s” and “1s”. Ex. 1001 2:23-26. The bits of the general mask are set “0” for links that are reachable “1” for links that are not reachable. Ex. 1001 2:19-30. The bits of the specific mask reflect the links along the path that a packet would take in the absence of a fault. Ex. 1001 2:26-30.

The use of bitmaps in the '859 Patent⁵ enables the use of the claimed *superimposition* operations by which the general mask and the specific mask are compared to each other in their entirety. Ex. 1001 4:64-5:1. In particular, the bitmaps claimed in the '859 Patent enable superimposition by means of *bitwise* Boolean

⁴ E.g., 8-bit, 16-bit, 32-bit, 64-bit.

⁵ The term “masks” as used in the '859 Patent would be understood by a POSITA to refer to bitmaps even without the specification disclosure. See Ex. 2058 ¶¶ 38-40.

operations such as AND, OR, or XOR (in the context of the '859 Patent, bitwise AND is preferred (Ex. 1001 4:64-5:1)).

As would be understood by a POSITA, bitwise operations in the computer programming context, such as bitwise AND,⁶ are low-level operations whose invocation in source code closely parallels the implementation of such operations down to the register- or logic gate-level when compiled into machine code. Ex. 2058 ¶ 90. As such, bitwise comparisons such as bitwise AND tend to be extremely fast operations that require few instructions to implement when the source code is compiled and that are executed very quickly. *Id.* As would be understood by a POSITA, fast execution is at a premium in a networking environment when making packet-routing determinations, because each such determination adds latency in a context in which minimal latency is highly desirable. Ex. 2058 ¶ 92. *See, e.g.* 1001 ('859 Patent) at 1:1-6 ("Field of the Invention" section) "The present invention relates generally to communication networks, and specifically to high-speed packet rings); 1:9-14 ("Network ring topologies are gaining in popularity, particularly in Internet Protocol (IP) networks. Such networks enable carriers to offer large

⁶ By convention, Boolean operations (*e.g.* AND, OR, NOT, XOR) are capitalized in the programming arts. Ex. 2058 ¶ 90 n.6.

bandwidth to users in a cost-effective manner. They also lend themselves to fast rerouting in the event of network failures . . . “).

An advantage of the '859 Patent – as reflected in its title, “Fast Protection in Ring Topologies” – is the use of bitwise superimposition operations to compare the intended packet route reflected in the specific mask with the reachability table reflected in the general mask, because such operations tend to be extremely fast and incur relatively little computational overhead. Because of the minimal computational overhead, such operations are well-suited to environments requiring minimal latency (such as network routing comparisons) and minimize the overhead of the fault-sensitive routing decisions and path selection claimed in the '859 Patent. Ex 2058 ¶ 93.

B. The '859 Patent's General Mask: A Link Reachability Map rather than a Link Failure Map

Central to the '859 Patent is the use of a general mask in which bits are set to indicate whether segments are reachable from a given node in the event of a fault:

1. In a bidirectional ring network, in which nodes are mutually connected by network segments, a method of fault protection, comprising:

constructing a general mask indicating which of the segments are reachable in the event of a fault in the network by assigning a respective general mask bit to each segment, indicating whether the segment is reachable following occurrence of the fault;

[. . .]

Ex. 1001, '859 Patent, Cl. 1. Note that each node in the network constructs its own general mask (Ex. 1001 4:42-45), which is desirable because in the event that a portion A of the network becomes isolated from another portion B, the nodes within the isolated portion A may be reachable to each other but not reachable to or from the remainder of the network B, and vice versa for the nodes on the other hand of the isolation divide in B. Ex. 2058 ¶ 58.

A key feature of the '859 Patent's general mask is that the general mask bitmap reflects link segment *reachability* rather than link segment *failure* – i.e., it is not just a failure table. As example of how the '859 Patent's reachability table differs from merely enumerating known link segment failures is described at 5:32-33 of the '859 Patent specification:

If segments **33** and **35** fail, the general mask is 0011100
(since segment **34** is also unreachable).

In a link *failure* table, the general mask would be “001**0**100,” because segment 34 is not known to have failed at the time at which it becomes disconnected from the network.⁷ A link *reachability* table, however, is “001**1**100” because even if segment 34 remains *functional*, it is not *reachable*.

⁷ If segment 34 failed *after* links 33 and 35, other nodes would not be aware of this due to the absence of communications with the isolated portion of the network to communicate the link failure, and a segment failure table would still (inaccurately)

As discussed further *infra*, the difference between a link *reachability* bitmap and a link *failure* table is that bits corresponding to unreachable (but not known-to-be-failed) segments will *not* be marked in a failure table but *will* be marked in segment reachability table. This means that in *any case in which two non-adjacent segments fail* and two portions of the network become isolated from each other, the bits of the ‘859 Patent *link reachability* bitmap will *not be the same* as those of a bit-based failure table (like that disclosed in the Omichi reference.). Thus, a bit-based failure table will not *in general* have the same values as the contents of a *reachability* bitmap or bit vector. This is a key distinction between a failure table and a reachability bitmap, and one that critically differentiates the ‘859 patent from the disclosure in the asserted Omichi reference, as detailed below. Ex. 2058 ¶¶ 61-62.

IV. OVERVIEW OF THE OMICHI REFERENCE

Omichi discloses a specific mechanism for tracking link failures in a ring network and, in the event that a link failure is detected in an intended route (“working path”), routing traffic to the alternative route (the other “virtual path” around the ring) based on a flowchart. Ex. 1005 at [0014].

reflect “00010100.” A link *reachability* table, however, is necessarily accurate because it makes no claim about whether inaccessible segments are or not functional, merely that they are not reachable. Ex. 2058 ¶ 60 & n.4.

The data structure that Omichi uses to track link failures is a “table” of bits, as to which link failures are marked (as either “1” in a group of “0s” or “0” in a group of “1”s). Ex. 1005 at [0036]. The values of this table are “compared” (Omichi is silent as to how⁸) with the values of the bits of the “working path” to see if a data flow will traverse a failed link. Ex. 1005 at [0040-41]. If the data flow will traverse a failed link on the “working” (default) path, the data flow is redirected to the alternative (“protection”) path around the ring. No provision is made for the prospect of failures in both directions. Ex. 1005 at [0039-44] and FIG. 7.

As discussed further below, Omichi’s disclosures differ in several key respects from the ’859 Patent’s claims. For example, Omichi’s does not teach or suggest the claimed general mask because its “link failure table” does not reflect link *reachability* as claimed in the ’859 Patent. Additionally, Omichi’s lack of express disclosure of *bitwise* Boolean operations, its suggestion of individual bit-by-bit comparisons in its flowcharts and specification, and the conspicuous absence of any

⁸ Ex 1005 at [0040] (“If the route switching flag is “0” (S3, 0), the used ring link table that corresponds to the virtual path number that was specified in step S2 is compared against the ring link failure table, and a determination is made as to whether or not there are bits having the same bit number and whose contents are both ‘1’ (S4)”).

disclosure of bitwise Boolean operations such as bitwise AND, mean that Omichi fails to teach or suggest the use of the claimed “superimposing.” Lastly, Omichi neither teaches nor suggests withholding from sending data in the event of multiple network failures making a link unreachable as claimed in dependent claims 3, 6, 9, and 12 – instead, Omichi reflects an assumption that this class of failure is unlikely to happen and that network conditions are unlikely to have high dynamism, and countenances only the prospect of redirection to the alternative path in the event of a failure on the default path. Ex. 2058 ¶¶ 64-67.

V. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (POSITA) would possess at least a bachelor’s degree in computer science, with an additional 2-4 years’ experience in networking technologies or equivalent field. Additional work experience could substitute for education, or vice versa. Ex. 2058 ¶ 33.

VI. CLAIM CONSTRUCTION

A. Mask

Patent Owner agrees in most respects with the substance of Petitioner’s proposed construction of “mask.”

For the sake of clarity, in the context of the ‘859 Patent, Patent Owner suggests that “pattern of characters” in Petitioner’s proposed construction should be replaced with “pattern of bits,” such that the construction of mask is “a pattern of bits that is

used to control the retention or elimination of portions of another pattern of bits.” Ex. 2058 ¶¶ 38-40. Patent Owner does not believe that the use of “pattern of bits” versus “pattern of characters” reflects a point of material dispute between the parties (See, e.g., Petition at 15-16 (“In other words, a mask may be ‘a pattern of bits’”) (citing Ex.1006, 668)).

B. Null

Patent owner agrees that “null” means a zero value, although Patent Owner does not believe that this term needs explicit construction and is not presently aware of any dispute as to which it would be material.

C. Superimposing

The term “superimposing” means “as part of a routing determination, combining or comparing by overlaying all bits as a whole.”⁹

⁹ Certain claims suggest that the claimed “superimposing” may encompass more of the routing determination step than just the overlay of bits, which is why the proposed construction includes the preamble “as part of a routing determination.” Compare Ex. 1001 at Cl. 2 (“2. A method according to claim 1, wherein superimposing the masks comprises combining the masks by means of a Boolean operation.”) with *id.* at Cl. 3 (“3. A method according to claim 1, wherein superimposing the masks comprises determining whether to convey the data flow

This construction is consistent with the disclosures and claims of the '859 Patent, which contemplate the use of bitwise Boolean operations such as bitwise AND to evaluate the overlap of any bits in the general mask's bitmap of unreachable segments and the specific mask's bitmap of proposed path through the ring network. Ex. 1001 at 2:31-47; Cl. 2 ("A method according to claim 1, wherein superimposing the masks comprises combining the masks by means of a Boolean operation."); Cl. 4 ("A method according to claim 3, wherein superimposing the masks comprises generating a combined mask, and determining that the data flow should be conveyed over the desired path when the combined mask is null.")

The plain meaning of the term "superimpose" is defined by Merriam-Webster as "to place or lay over or above something."¹⁰ Implicitly – and as exemplified by the example sentences in the dictionary entries of Exhibits 2061 and 2062, which

over the desired path, to steer the data flow over an alternative path, or to stop conveying the data flow."). Ex. 2048 ¶ 46.

¹⁰ Ex. 2062, Merriam-Webster definition of "superimpose" <https://www.merriam-webster.com/dictionary/superimpose> (last viewed September 24, 2025). *See also* Ex. 2061 (Webster's Third International Dictionary, (1981) (definition of "superimpose") ("to place in a covering position: OVERLAY <a transparent mask . . . is *superimposed* over the print – *Eastman Kodak Monthly Abstract Bull.*>").

refer to the physical overlay of photographic or film cells or shapes – this suggests that one object or item is aligned to be overlaid on top of another as a whole. Ex. 1001 at 2:31-47 (discussing “overlap” of the respective masks), Ex. 2058 ¶¶ 42-44.

In the context of the ’859 Patent, it is clear that the two masks must be aligned and overlaid in parallel in order to preserve the indices of the bits in the general and specific masks – that is, if bit 3 of the general mask corresponds to segment “C,” then the bit of the specific mask corresponding to the general mask must also correspond to segment “C,” or no information can be gleaned from comparing the two masks. Ex. 1001 at 4:64-5:21. *See also* Ex. 1006 (IEEE dictionary definition of “mask”) at 668 (definition 2, cited by Petitioner at 15-16) (“for example, the bit string ‘00000011’ when logically ANDED with an eight-bit data item, gives a result that retains the last two bits of the data item and has zero in all the other bit positions.”); Ex. 2058 ¶ 44. Accordingly, superimposing the general mask and specific mask requires aligning the respective bits of the masks, and then combining or comparing them as a whole to determine the overlap (if any) of matching “1” bits. Ex. 1001 at 2:31-47. (“When the result corresponds exactly to the general mask (showing that the unreachable segments are all contained within the intended path), the node steers the flow in the opposite direction, away from the failed segments. In any other case (only partial overlap of the unreachable segments with the desired

path), the node concludes that the destination node has been isolated by the fault, and is no longer reachable in either ring direction.”).

The requirement that the masks be compared as a whole or in parallel is an implication of the use of term “superimposing” as well as the knowledge of a POSITA. Boolean AND operations—which are expressly described as a form of superimposition, *see* Ex. 1001 Cl. 2, and which Petitioners rely on for the alleged obviousness of this claim element in Omichi (*e.g.* Petition at 1)—generally take bit vectors (*e.g.* unsigned integers, which can represent strings of zeroes and ones up to the length supported by the underlying language and hardware/operating system) as arguments rather than evaluating individual bits one at a time, and return a bit vector reflecting the comparison of each bit. *E.g.* Ex. 1001 at 4:64-5:7 (“If the conjunction is 0000000, the node can conclude that there is no overlap between this data flow and the failed segments in network 20, and therefore determines that no steering of this flow is required[.]”). Ex. 2058 ¶ 44. Conversely, comparison in serial would risk reading the patentee’s choice of the word “superimposing” out of the claim.

In view of the plain and ordinary meaning of the word “superimposing” as it would be understood by a POSITA reading the ’859 Patent, “superimposing” should be construed as “as part of a routing determination, combining or comparing by overlaying all bits as a whole.”

VII. PETITIONER FAILS TO SHOW A REASONABLE LIKELIHOOD OF PREVAILING ON ANY CHALLENGED CLAIM

A. The Petition Fails to Teach, Suggest, or Render Obvious the Claimed “General Mask” (All claims)

Omichi fails to teach or suggest the claimed general mask of the ’859 Patent. the *link failure table* of Omichi is not the same as the claimed *segment reachability bitmap* of the ’859 Patent and the contents (i.e., bits) of the two respective data structures will differ in any instance of a failure of non-adjacent network segments. Ex. 2058 ¶ 68. The Petition fails to even address this deficiency, let alone overcome it. Because the Petition fails to establish a reasonable likelihood that Omichi teaches, suggests, or renders obvious the claimed general mask, which is an element of both independent claims of the ’859 Patent (Claims 1 and 7), the Board should deny institution.

The claimed general mask of the ’859 Patent reflects segments that are *unreachable* in the event of a fault:

1. In a bidirectional ring network, in which nodes are mutually connected by network segments, a method of fault protection, comprising:

constructing a general mask indicating **which of the segments are reachable** in the event of a fault in the network by assigning a respective general mask bit to each segment, indicating whether the segment is **reachable** following occurrence of the fault;

Ex. 1001, ’859 Patent Cl. 1; (emphasis added). *See also id.* at Cl. 7 (“... the device comprising a network processor, which is adapted to **construct a general mask**

indicating which of the segments are reachable in the event of a fault in the network . . .”) (emphasis added). See also *supra* § II.B; Ex. 2058 ¶ 69.

As reflected in the ’859 Patent specification, in the event that two non-adjacent segments fail (separating the network into different portions), the contents of the claimed general mask will mark the intermediate segments of the disconnected network shard as unreachable:

If segments **33** and **35** fail, the general mask is **0011100**
(since segment **34** is also unreachable).

Ex. 1001, ’859 Patent at 5:32-33 (emphasis added).

This example illustrates the difference between a general mask for link *reachability* and Omichi’s link *failure* table. Were the ’859 Patent’s general mask merely used to mark link *failures*, the general mask in this case would be “0010100,” because segment 34 is not known to have failed at the time at which it becomes disconnected.¹¹ A link *reachability* table, however, is “0011100” because even if segment 34 remains *functional*, it is not *reachable*. Ex. 2058 ¶ 70-71.

¹¹ If segment 34 failed *after* links 33 and 35, other nodes would not be aware of this due to the absence of communications with the isolated portion of the network to communicate the link failure, and a segment failure table would still (inaccurately) reflect “00010100.” A link *reachability* table, however, is necessarily accurate

1. Omichi discloses only a link failure table and not the '859 Patent's link-reachability general mask

Unlike the '859 Patent's general mask, Omichi discloses only a *link failure table* in which bits are set based on link failures, rather than setting bits for all link segments known to be unreachable. Ex. 1005, Omichi, at [0036] (emphasis added)

[0036] FIGS. 6(a) through FIG. 6(c) show the tables that are stored in route information part 9. **The ring link failure table shown in FIG. 6(a) is used to hold information that indicates whether or not a failure has occurred in a ring link.** The ring link failure table has a bit width equal to the maximum number of ring links in the ring network, and the bit number corresponds to the ring link number. A particular bit with a value of "0" indicates that there is no failure in the corresponding ring link. A value of "1" indicates a failure in the corresponding ring link. Thus, there is no failure anywhere, and all bits in the ring link failure table are "0." However, if a failure occurs in a ring link, a branch insertion node 1a through 1d that receives the failure notification sets the value to "1" for the bit number corresponding to the ring link number where a failure has occurred.

See also Petition at 22 ("Omichi describes using a first set of bits in the form of a *ring link failure table*[.]") (citing same disclosure) (emphasis added).

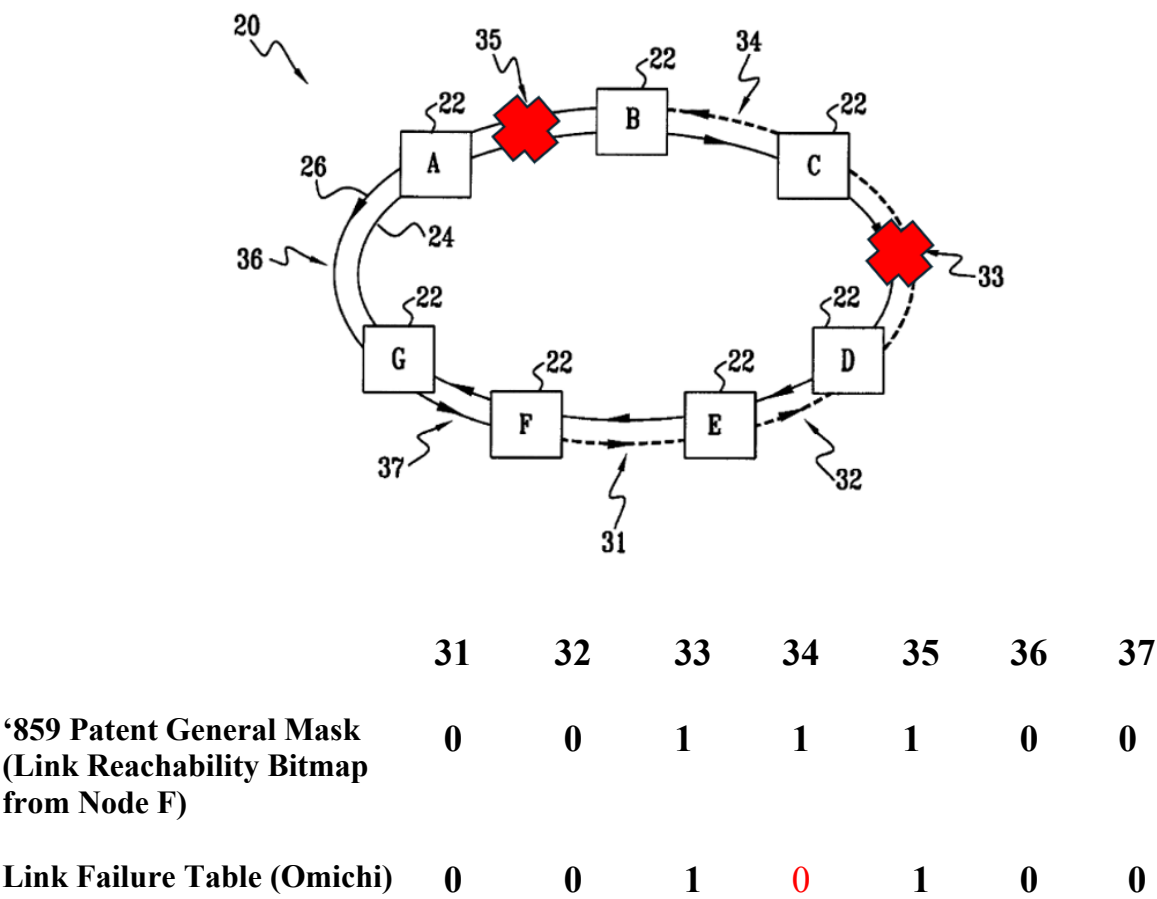
The link-failure data structure disclosed by Omichi is thus *not the reachability-based the general mask of the '859 Patent* and will differ in exactly the circumstances described in the '859 specification that exemplify what the general mask is. In the '859 Patent, "if segments 33 and 35 fail, the general mask is **0011100**

because it makes no claim about whether inaccessible segments are or not functional, merely that they are not reachable. Ex. 2058 ¶ 72.

(since segment 34 is also unreachable)” (Ex. 1001, ’859 Patent at 5 :32-33). Ex. 2058 ¶ 74.

Omichi’s link failure table, by contrast to the general mask, *would not mark the segments of the disconnected portion of the network* and thus *would not mark the bit corresponding to segment 34*—Omichi’s link failure table would, instead, contain the bits “0010100” – distinct from and different than the bits of the claimed general mask. Omichi’s *link failure table* is thus demonstrably *not the same* as the claimed general mask for link reachability. Ex. 2058 ¶ 75.

FIG. 1



Example bit values for link Reachability Bitmap ('859 Patent) versus link failure table (Omichi) in the circumstances described in '859 Patent 5:32-36 (failure of Segments 33 and 35 in annotated FIG. 1) – Note the difference in values between the two data structures. The link failure table is not a general mask.

2. The Petition fails to remedy the deficiencies in Omichi

The Petition wholly fails to remedy, or even substantively address, the discrepancy between Omichi's link failure table and the claimed link-reachability general mask of the '859 Patent.

Initially, the Petition first suggests (incorrectly) that that Omichi's ring link failure table *is* the claimed general mask (Petition at 28, “. . . Omichi describes a ring link failure table (“*general mask*”) that indicates whether a failure has occurred in a ring link . . .).” Later on, the Petition instead states that “Omichi's ring link failure table is similar to the general mask as described in the '859 patent” (Petition at 30, emphasis added.)—implicitly conceding that Omichi does not disclose the element directly and so the Petition must rely on an obviousness argument as to the claimed general mask. However, the Petition fails to establish that a POSITA would modify Omichi's link failure table to meet the claimed general mask.

The Petition's argument as to why Omichi renders the claimed general mask obvious despite its failure to teach the same data structure is purely conclusory:

Thus, because Omichi constructs a ring link failure table in which each bit corresponds to a ring link and indicate whether there is a fault in that ring link, Omichi renders obvious “*constructing a general mask*

indicating which of the segments are reachable in the event of a fault in the network by assigning a respective general mask bit to each segment, indicating whether the segment is reachable following occurrence of the fault.” Ex.1003, ¶¶68-72.

(Petition at 30.) This statement contains no argument for, nor even acknowledgment of, the need to modify Omichi’s link failure table in order to create the same sequence of bits as the claimed general mask of the ’859 Patent.¹² The lack

¹² While the Petition’s citation to Dr. Min’s declaration without presenting a substantive argument in-line would be improper in any event, the quoted portion of Dr. Min’s declaration adds nothing of substance to the Petition regardless – instead, the cited portions of the declaration (¶¶68-72) identically mirror the Petition’s section 1.1 (pages 28-30) with the addition of longer block quotes. Dr. Min’s argument as to why Omichi renders the claimed general mask obvious is a verbatim duplicate – and identically conclusory – as the last paragraph of this section of the Petition. Ex. 1003 (Min Decl.) at 72 (“Thus, because Omichi constructs a ring link failure table in which each bit corresponds to a ring link and indicate whether there is a fault in that ring link, Omichi renders obvious...”). *Apple Inc. v. MPH Techs. Oy*, 28 F.4th 254, 263 (Fed. Cir. 2022) (“substantial evidence supports the Board’s finding that Apple failed to show a motivation to modify the prior art combination to include substitution. Apple relied solely on its expert’s contrary testimony, which the Board properly disregarded as conclusory.”) (citations omitted).

of any substantive argument as to the nature or motivation of a POSITA to modify Omichi's link failure table is fatal to the argument for obviousness of the claimed general mask claim element in view of the fact that Omichi does not inherently or expressly disclose such an element. *Regents of Univ. of California v. Broad Inst., Inc.*, 903 F.3d 1286, 1291 (Fed. Cir. 2018) (“An obviousness determination requires finding that a person of ordinary skill in the art would have been motivated to combine or modify the teachings in the prior art and would have had a reasonable expectation of success in doing so.”); *In re Stepan Co.*, 868 F.3d 1342, 1345–46 (Fed. Cir. 2017) (making the same observation and noting that motivation to modify is a question of fact). *Cf.* Petition at 30 (“Omichi's ring link failure table is **similar to [i.e., not *the same as*]** the general mask as described in the '859 patent”) (emphasis added).

Because the claimed general mask is an element of every claim in the '859 Patent, the failure to establish that it is rendered obvious by Omichi is fatal to the Petition as a whole, and Petitioners have not established a reasonable likelihood of prevailing on any challenged claim.

3. A POSITA would not be motivated to modify Omichi to include the '859 Patent's claimed general mask

While the Petition's failure to establish—or even substantively argue for—the obviousness of the claimed general mask is fatal on its own, a POSITA would also not be motivated to modify Omichi's link failure table to match the contents of the

claimed general mask. Ex. 2058 ¶¶ 76-80. Such a modification provides no clear benefit to the design of Omichi: a virtual path in Omichi (i.e., a proposed path around the ring) encompasses “1” bits for each path segment. Ex. 2058 ¶ 77. Any overlap (even a single bit) between a bit corresponding to a link of a proposed virtual path and a bit of Omichi’s link failure table indicates that the data flow cannot be sent over the proposed virtual path, and so an alternative path should be used. Thus there is no need for a POSITA to (redundantly) ensure that each bit of the failure table corresponding to a network segment isolated by multiple non-adjacent faults should be set to “1,” because any single match between a bit index of link failure table and the corresponding bit index of the virtual path of Omichi would be sufficient on its own to enable Omichi’s design. Thus, there is no motivation for a POSITA to modify Omichi’s link failure table to meet the requirements of the ’859 Patent’s claimed link-reachability general mask. 2058 ¶¶ 76-79.

B. Omichi Fails to Teach or Render Obvious the Claimed “Superimposing”

The petition fails to establish that the claimed “superimpos[ing]” of the general mask and specific masks claimed in the ’859 Patent is either disclosed or rendered obvious by Omichi. *See* Ex 1001 at Cl. 1 (“superimposing the general and specific masks in order to determine a disposition of the flow.”), Cl. 7 (“superimpose the general and specific masks in order to determine a disposition of the flow.”).

1. Only *bitwise* Boolean operations, rather than serial *logical* Boolean operations, would meet the “superimposing” claim element

As discussed *supra* regarding claim construction, a POSITA would understand “superimposing” in the ’859 Patent to mean “as part of a routing determination, combining or comparing by overlaying all bits as a whole.” (§ VI.C *supra*, Ex. 2058 ¶ 83).

In order for the claimed general and specific masks to be “superimposed,” a POSITA would understand that the bits of the respective masks must be *overlaid* (i.e., compared or combined in their entirety) – preferably by means of a bitwise binary¹³ Boolean operation such as bitwise AND (in computer programming, typically represented by the ‘&’ operator), bitwise OR (‘|’), or bitwise XOR (‘^’). (See, e.g., Ex. 1001 Cl. 2 (“2. A method according to claim 1, wherein superimposing the masks comprises combining the masks by means of a Boolean operation.”) (emphasis added). Ex. 1001 2:31-34, 4:64-5:1 (“In order to determine how to handle the data flow following the fault, node F mathematically superimposes the applicable general and specific masks, preferably by taking the Boolean conjunction (AND) of the masks, at a conjunction step 54”).

¹³ “Binary” here referring to taking two arguments rather than to operating on zeroes and ones. Ex. 2058 ¶ 43 & n.1

A POSITA would understand that, in the '859 Patent, taking the Boolean conjunction (AND) of the masks (which are described as “bitmaps” 2:23-30; Cl. 1, Cl. 7) to yield a new bit vector (such as “0000000” or “0000100” as discussed as Ex. 1001 at 4:64-5:13) refers to a *bitwise* binary operation, typically represented in source code by the operator “&” (single ampersand) and taking as arguments unsigned integers. Ex. 2058 ¶ 84.

Bitwise Boolean operations differ somewhat conceptually (and, in many programming languages, such as Java, accept different argument types) from *Logical* Boolean operations.

Logical Boolean operations work conceptually on propositions that are “true” or “false” (such as “X is greater than 10”). More modern programming languages and have a primitive “boolean” (e.g. Java) or “bool” type (e.g. C#, Python) that can take the values “true” or “false.” Ex. 2058 ¶ 85.

By contrast, *bitwise* Boolean operators take as inputs and provide as outputs *sequences of bits* rather than *logical propositions*, and are more akin to mathematical or even physical operators such as arithmetic operators like “+”, “-”, etc. Ex. 2058 ¶ 86.

The conceptual distinction between logical and bitwise operators is reflected at a source code level: logical Boolean operations typically use different or doubled characters (“&&” for logical AND, “||” for logical OR, “!” for logical NOT) whereas

bitwise operators use single character (“&” for bitwise AND, “|” for bitwise OR, “~” for bitwise NOT, “^” for bitwise XOR). Ex. 2058 ¶ 87.

The Petition relies on the alleged disclosure of “Boolean” operations in Omichi, but does not clearly highlight the distinction between *bitwise* and *logical* Boolean operations despite their different scopes and implementations. *E.g.* Petition at 1 (discussing Omichi) (“To determine if data for that path should be rerouted in the opposite direction, the first set of bits is compared with the second set of bits using a Boolean AND operation”). However, the distinction between the two concepts is not merely academic: a series of individual bit-by-bit comparisons using logical Boolean operations would not overlay one bit pattern on top of another as a whole, and thus *would not be superimposing as claimed in the ’859 Patent*, whereas a bitwise Boolean operation would be.

Accordingly, for the “Boolean AND operation” relied on by Petitioners to read on the ’859 Patent’s claimed “superimposing” elements, it must specifically be a *bitwise* Boolean operation. However, as discussed below Omichi does not teach such a bitwise Boolean operation, and in fact the use of bitwise Boolean operations is conspicuously absent from Omichi.

2. The claimed “superimposition” (i.e. bitwise Boolean operation) is not taught by Omichi

Petitioners are inconsistent—or perhaps deliberately vague—as to whether Omichi expressly discloses the claimed superimposition by the use of a bitwise AND

operation. *Compare* Petition at 40 (“ . . . a POSITA would have understood that comparing bits in the manner described by Omichi is effectively performing a Boolean AND operation.”) (emphasis added), *with id.* at 41 (“Thus, Omichi describes what is known as a Boolean AND operations by comparing the two tables to see where there is a ‘1’ in both corresponding bit numbers”) (emphasis added). To the extent the Petition relies on an express or inherent disclosure of the claimed superimposition (i.e., bitwise Boolean operation), however, such an argument fails: Omichi does not expressly or inherently teach a bitwise Boolean comparison.

Instead of teaching the claimed superimposition, Omichi refers only to “comparing” the “tables”¹⁴ of route information, after which “a determination is made” as to whether there are bits at the same index of the working path and the link failure table with value ‘1.’

[0040] Next, route selection processing part 8 determines whether or not the route switching flag that corresponds to the virtual path number that was specified in step S2 is “0” (S3). If the route switching flag is “0” (S3, 0), the used ring link table that corresponds to the virtual path number that was specified in step S2 **is compared against** the ring link failure table, **and a determination is made** as to whether or not there are bits having the same bit number and whose contents are both “1” (S4).

¹⁴ As discussed *infra*, the term “tables” is suggestive to a POSITA of serial element-by-element comparison. Ex. 2058 ¶ 102.

Ex. 1005 at [0040] (emphasis added). There is no express or inherent disclosure here or anywhere else in Omichi of a bitwise AND or other bitwise Boolean operation.

The Petition argues conclusorily that “Omichi’s comparing of both the ring link failure table and the used ring link table is within the scope of “superimposing” as recited in claim 1” (Petition at 35). This argument ignores any number of ways by which comparisons may be accomplished that do not involve superimposition. A POSITA would understand that the recited “comparison” of Omichi would not necessarily imply the use of bitwise binary operations that would practice the claimed superimposition, and instead could refer to *logical* Boolean operations performed bit-by-bit, without any overlay of Omichi’s bit-tables as a whole. Indeed, on their own, the terms “comparison” and “a determination is made” would most commonly suggest the use of logical Boolean operations. Ex. 2058 ¶¶ 100-101, as would the use of word “table,” which would typically be understood by a POSITA to suggest a data structure with individually addressable or indexable entries (for example, an array) in which entries are compared element-by-element rather than as, e.g., arguments to a binary bitwise operation. Ex. 2058 ¶ 102.

For example, the following code (in a language such as C or C#) compares the “tables” of Omichi bit-by-bit *without superimposing* them or using a bitwise Boolean operator (such as AND (“&”) or OR (“|”)), and if implemented would facilitate comparing bits for equality while also making clear precisely which bit of

the general and specific masks are both “1” (i.e., which link has both failed and is in the proposed working path of Omichi):

```

for(int i = 0; i < Omichi_table_length; i++)
{
    uint link_failure_status_bit =
        (ring_link_failure_table >> i) % 2;
    uint desired_working_path_bit =
        (used_ring_link_table >> i) % 2;
    if (link_failure_status_bit == 1 &&
        desired_working_path_bit == 1){
        // desired path has a link failure at
        // bit "i" - take appropriate action
        // and stop comparison
        use_alternative_path();
        break;
    }
}

```

Ex. 2058 ¶ 98. As is clear from the above, the mere presence of a “comparison” in Omichi does not—contrary to the Petition’s claims—equate to the claimed superimposition (*i.e.* bitwise Boolean operations relied on by the Petition) of the ’859 Patent. Such a comparison could be accomplished in any number of

alternative ways. The Petition’s argument to the contrary is misleading and inaccurate in an attempt to paper over Omichi’s deficient disclosure only of a *comparison* but not of the *superimposition* claimed in the ‘859 Patent. Ex. 2058 ¶¶ 97-99.

3. Omichi does not suggest the use of bitwise Boolean superimposition operations to a POSITA

Omichi not only lacks any express or inherent disclosure of bitwise Boolean operations with respect to its link failure table and virtual paths, but also contains disclosures that are suggestive of operations other than the claimed superimposition of the ‘859 Patent.

Firstly, Omichi’s use of the term “table” to refer to the bit-valued link failure data structure (*See* Fig. 6a) would be understood by a POSITA to typically refer to a data structure with individually addressable or indexable entries (for example, an array) in which entries are compared element-by-element rather as a whole. Ex. 2058 ¶ 102.

Secondly, at least Fig. 7 of Omichi (the flowchart as to routing path determinations) reflects the evaluation of an individual bit’s value at item “S3.” Ex. 1005 Fig. 7.

Thirdly, a POSITA would typically expect to see explicit rather than implicit disclosure of bitwise Boolean operations, were they present. Ex. 2058 ¶ 107. Particularly in the context of the comparison of two bit-valued tables (the link failure

table and the virtual path of Figs. 6a and 6b), such disclosure is conspicuously absent from Omichi, in favor of the use of the generic terms—more typically associated with logical than bitwise Boolean operations—of “compared against” and “a determination is made” Ex. 1005 [0044]. This gives rise to at least an inference that Omichi does not contemplate the use of bitwise Boolean operators, relying instead on element-by-element comparisons. *See* Ex. 2058 ¶ 107.

That Omichi (1) refers to its link-failure data structure as a *table*, which would be understood by a POSITA to suggest entry-by-entry comparison (2) illustrates comparison flowcharts on a bit-by-bit level, and (3) uses the general term “compared against” and “determination is made” with respect to tables with bit-valued entries without ever expressly alluding to bitwise comparisons, are suggestive a POSITA that Omichi not does not disclose bitwise Boolean operations or the claimed “superimposing” element, instead suggesting to a POSITA that Omichi prefers an element-by-element comparison would be. Rather than addressing these deficiencies, the Petition strategically elides the distinction between bitwise and logical Boolean operations and between express disclosure and obviousness. This is not enough to give rise to a reasonable likelihood that any challenged claim is not patentable.

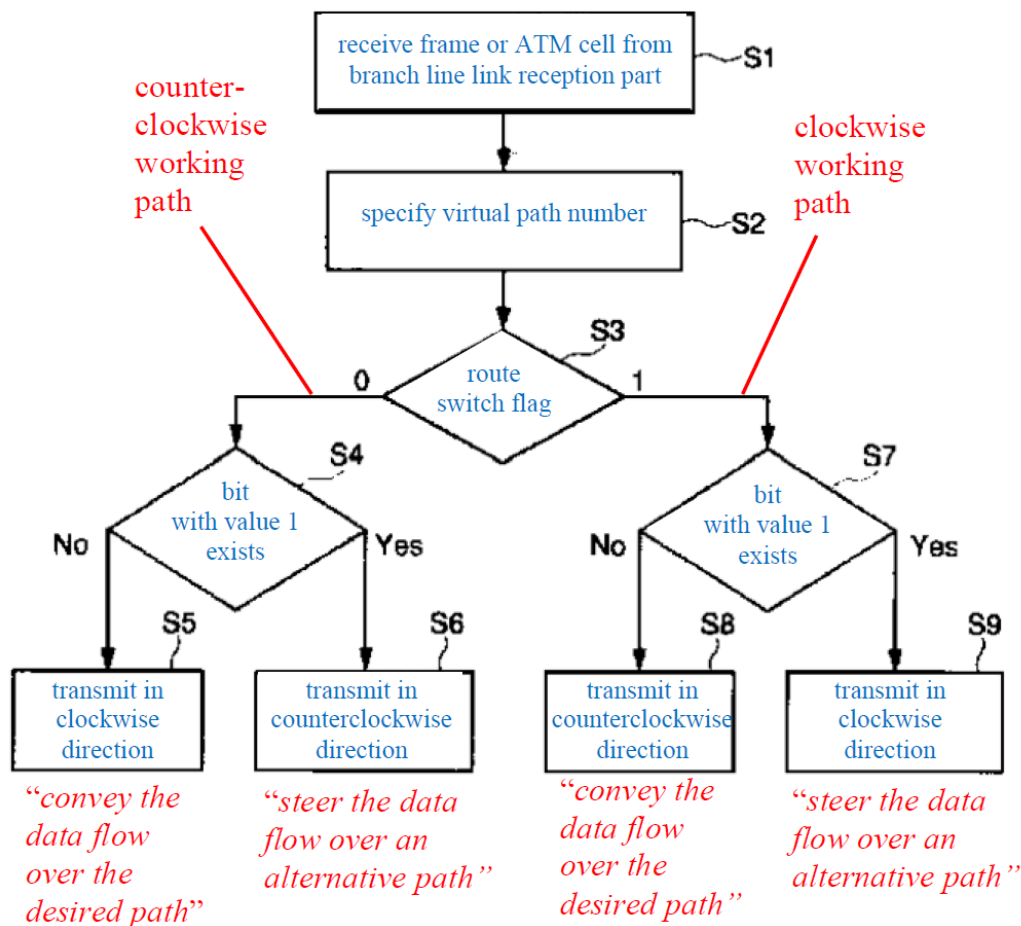
C. Omichi does not disclose or render obvious not conveying a data flow when the destination node is unreachable [Claims 3, 6, 9, 12]

The Petition further fails to establish that Omichi renders obvious ceasing to provide a data flow (*i.e.* not sending packets) when a destination node or segment is unreachable, which forms a part of '859 Patent Claims 3 (*A method according to claim 1, wherein superimposing the masks comprises determining whether to convey the data flow over the desired path, to steer the data flow over an alternative path, or to stop conveying the data flow*“) 6 (*“A method according to claim 3, wherein superimposing the masks comprises generating a combined mask, and determining that the data flow should not be conveyed when the combined mask is neither null, nor does it correspond to the general mask.”*), 9 (parallel in relevant part to claim 3)¹⁵ (*See* Petition at 57-58 (relying on same arguments as claim 3 for claim 9)), and 12 (parallel in relevant part to claim 6)¹⁶ (*See* Petition at 58 (relying on same arguments as claim 6 for claim 12)).

¹⁵ (“A device according to claim 7, wherein the processor is adapted to determine whether to convey the data flow over the desired path, to steer the data flow over an alternative path, or to stop conveying the data flow based on the superimposed masks”)

¹⁶ (“A device according to claim 9, wherein the processor is adapted to superimpose the masks so as to generate a combined mask, and to determine that the data flow

Omichi clearly teaches a fundamentally binary view of data transmission (i.e., data can take one path or the other around the ring), as reflected by the flowchart of Fig. 7 (See, e.g. elements S3, S5, S6, S8, S9) and does not contemplate the multiple-failure scenario in which failures exist on both sides of the ring network.



Ex.1005, Fig. 7 (annotated); Ex.1003, ¶98.

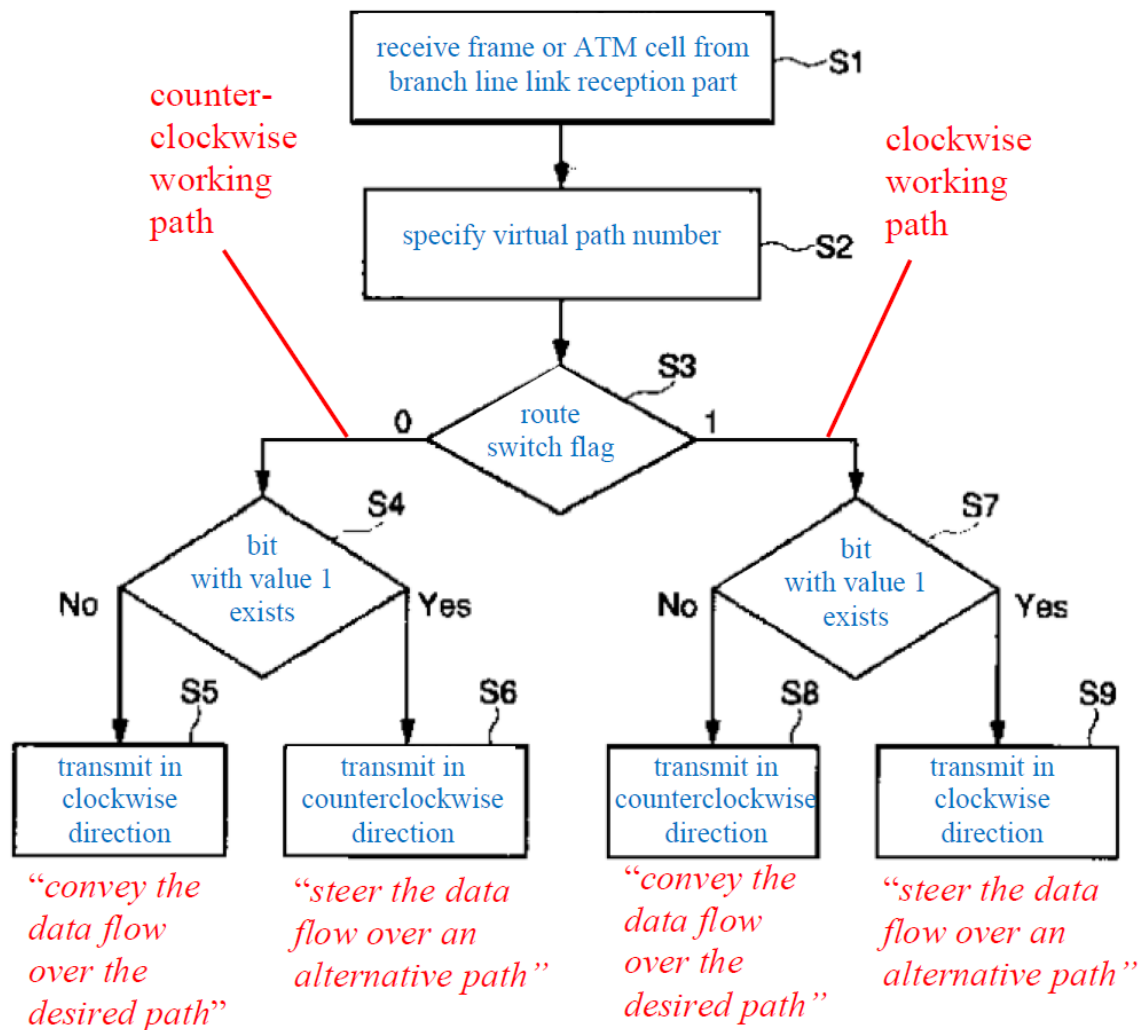
(Fig. 7 (annotated), reproduced, including annotations, from Petition at 45).

should not be conveyed when the combined mask is neither null, nor does it correspond to the general mask.”)

Omichi reflects an underlying assumption that multiple non-adjacent link failures are unlikely to isolate a network segment. Ex. 2058 ¶ 110-111. *See also* Ex. 1005 at [0039]-[0044] (discussing Fig. 7 and reflecting only the binary choice of using the “working” (default) path or the alternative “protection” path.)

Petitioners concede that Omichi does not expressly or inherently disclose not sending data in the event of a failure along both possible routes to the destination. Instead, the Petition argues that not transmitting data in the event of no failure is “merely obvious to try.” Petition at 45 (discussing claim 3). This contradicts both the explicit disclosures and the implicit assumptions of Omichi.

Firstly, refraining from transmitting data is inconsistent with the disclosure of Omichi, including the extensive flowchart (Fig. 7) cited by Petitioners on the same page of their statement regarding such a modification being “obvious to try.”



Ex.1005, Fig. 7 (annotated); Ex.1003, ¶98.

(Fig. 7 (annotated), reproduced, including annotations, from Petition at 45). *See also* Ex. 2058 ¶ 110.

Secondly, as discussed, Omichi reflects an underlying assumption that multiple non-adjacent link failures are unlikely to isolate a network segment. Ex. 2058 ¶ 111. A POSITA would understand that this is reflected in both Fig. 7 and in Omichi at [0044], which suggests the resetting of alternative paths back to their

original working paths only on the clearing of all failures in the network, rather than dynamically switching from the alternate “protection paths” back to the default “working paths” as individual segments recover from failure. Ex. 1005 [0044]; Ex. 2058 ¶ 112. This reflects an assumption of infrequent network failures typically fixed all at once, rather than dynamic network conditions requiring more robust failure recovery. Ex. 2058 ¶ 113. In view of these assumptions, it would not be obvious to a POSITA to modify (or try to modify) Omichi to account for a situation that was clearly not expected to arise. Ex. 2058 ¶¶ 113-114.

Because Omichi clearly reflects a set of assumptions that network failures are (i) infrequent and (ii) unlikely to occur on both potential paths of a ring network, a POSITA viewing Omichi’s binary path-decision flowchart and related disclosures would not understand it to teach or suggest refraining from sending data in the event of multiple network failures resulting in complete disconnection, nor—despite the Petition’s conclusory allegation that such a modification would be “obvious to try”—would a POSITA be motivated to modify Omichi to include such behavior in view of such assumptions.

VIII. CONCLUSION

For the foregoing reasons, Patent owner submits that the 1088 Petition fails to demonstrate that there is a reasonable likelihood that one or more of the challenged

claims of the '859 Patent is unpatentable. Patent Owner respectfully submits that the Board should not institute *inter partes review* of the '859 Patent.

Date: September 25, 2025

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), the undersigned hereby certifies that the foregoing Patent Owner's Preliminary Response to Petition for *Inter Partes* Review contains 8,430 words using the word count feature of Microsoft Word.

Date: September 25, 2025

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CERTIFICATE OF SERVICE

I hereby certify that on September 25, 2025, I caused a true and correct copy of the foregoing Patent Owner's Preliminary Response to Petition for *Inter Partes* Review to be served via electronic mail upon the following attorneys of record for the Petitioner:

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