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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/528,526	06/20/2012	Satoru ITOU	085393-0792	2414

53080 7590 08/22/2013
McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

EXAMINER
NGUYEN, LAWRENCE-LIN T

ART UNIT	PAPER NUMBER
2897	

NOTIFICATION DATE	DELIVERY MODE
08/22/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mweipdocket@mwe.com

PTOL-90A (Rev. 04/07)

UMC 1002
UMC v. AICP

Office Action Summary	Application No. 13/528,526	Applicant(s) ITOU ET AL.	
	Examiner LAWRENCE-LINH T. NGUYEN	Art Unit 2897	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☐ Claim(s) _____ is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) 1-15 is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some * c)☐ None of the:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 06/20/2012 & 05/16/2013.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____

4) ☐ Other: _____.

Detailed Action

1. This non-final Office action is responsive to Applicants' application filed **06/20/2012**. Claims **1-15** are presented for examination and claims **1-15** are rejected for the reasons indicated herein below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*
>
> *The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: (See MPEP Ch. 2141)*
>
> *Determining the scope and contents of the prior art;*
>
> *Ascertaining the differences between the prior art and the claims in issue; Resolving the level of ordinary skill in the pertinent art; and Evaluating evidence of secondary considerations for indicating obviousness or nonobviousness*

3. Claims **1-15** are rejected under 35 U.S.C. 103(a), as being anticipated by **Fujimoto** et al., (**US20090065807 A1**, hereinafter **Fujimoto)** in view of **Sell** et al.,

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(**US20080029834 A1**, hereinafter **Sell**).

4. In reclaim **1**, in FIG. 1A-4C, Fujimoto teaches a semiconductor device comprising: a first MIS transistor, wherein the first MIS transistor includes

a. a first gate insulating film(**15b**) formed on a first active region(**11b**) in a semiconductor substrate(**11**),

b. a first gate electrode(**17**) formed on the first gate insulating film(**15b**),

c. a first sidewall(**24b**) formed on a side surface of the first gate electrode(**17**),

d. a first source/drain region(**28**) of a first conductivity type which is formed in a trench(**12**) provided in the first active region(**11b**) on a lateral side of the first sidewall(**24b**), and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region(**11b**), and

e. a stress insulating film(**30A**) which is formed on the first active region(**11b**) to cover the first gate electrode(**17**), the first sidewall(**24b**), and the first source/drain region(**11b**), and which causes a second stress opposite to the first stress,

f. an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate(**11b**) located directly under the first gate electrode(**17**), and (*See* ***§ [0058-78]***).

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5. In reclaim **1**, Fujimoto fails to teach a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall.

6. But in the same field of endeavor of invention, **Sell** teaches a first stress-relief film(**250**) is formed in a space between the silicon compound layer(**218**) and the first sidewall(**270**).

7. **Sell** is evidence that ordinary workers skilled in the art would find reasons, suggestions or motivations to modify the device of **Sell** with Fujimoto. Therefore, at the time the invention was made, it would have been obvious to use the teaching of **Sell** in the device of Fujimoto since isolation spacer may provide the same physical separation and protection of the conductive region as a conventional single-component isolation spacer, but may also enable a reduction in fringe capacitance, i.e. "cross-talk," between conductive regions within a semiconductor structure (*See* ***§ [0009]***).

8. In reclaim **2**, in Fig. 1A, Fujimoto in view of Sell, teaches a semiconductor device of claim **1**, further comprising: a first offset spacer(**19**) which is formed between the first gate electrode(**17**) and the first sidewall(**24**), and whose cross-section has an I shape (*See* ***§ [0058]***).

9. In reclaim **3**, in Fig. 3C, Fujimoto in view of Sell, teaches a semiconductor device of claim **1**, further comprising: a first silicide layer(**29**) formed on the first gate electrode(**17**); and a second silicide layer(**29**) formed on the first source/drain region(**11b**) which includes the silicon compound layer (*See* ***§ [0068]***).

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10. In reclaim **4**, in Fig. 4C, Fujimoto in view of Sell, teaches a semiconductor device of claim **1**, wherein the first stress-relief film(**30A**) is formed on a side surface of the silicon compound layer (*See* ***§ [0077]***).

11. In reclaim **5**, in Fig. 1C, Fujimoto in view of Sell, teaches a semiconductor device of claim **1**, wherein the first sidewall(**24b**) includes an inner sidewall(**22**) which is formed on the side surface of the first gate electrode(**17**), and whose cross-section has an L shape, and an outer sidewall(**19b**) formed on the inner sidewall (*See* ***§ [0059]***).

12. In reclaim **6**, in Fig. 1C, Fujimoto in view of Sell, teaches a semiconductor device of claim **1**, wherein the first sidewall(**24b**) includes an inner sidewall(**22**) whose cross-section has an L shape, and the stress insulating film is formed in contact with a surface of the inner sidewall which is curved to have an L-shaped cross-section (*See* ***§ [0061]***).

13. In reclaim **7**, in Fig. 1A, Fujimoto in view of Sell, teaches a semiconductor device of claim **1**, wherein the first MIS transistor is a p-type MIS transistor, the first stress is a compressive stress, and the second stress is a tensile stress (*See* ***§ [0058]***).

14. In reclaim **8**, in Fig. 1A, Fujimoto in view of Sell, teaches a semiconductor device of claim **1**, wherein the silicon compound layer is a SiGe layer, the stress insulating film is a silicon nitride film, and the first stress-relief film is a silicon oxide film (*See* ***§*** *[*Fujimoto *(**0065,0075**), & Sell (**0029**)]*).

15. In reclaim **9**, in Fig. 1A, Fujimoto in view of Sell, teaches a semiconductor

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device of claim **1**, wherein the first MIS transistor is an n-type MIS transistor, the first stress is a tensile stress, and the second stress is a compressive stress (*See* ***§ [0058]***).

16. In reclaim **11**, in Fig. 1A-C, Fujimoto in view of Sell, teaches a semiconductor device of claim **1**, further comprising: a second MIS transistor, wherein the second MIS transistor includes a second gate insulating film(**15a**) formed on a second active region(**11a**) in the semiconductor substrate(**11**), a second gate electrode(**16**) formed on the second gate insulating film(**15a**), a second sidewall(**24a**) formed on a side surface of the second gate electrode(**16**), a second source/drain region(**25**) of a second conductivity type which is formed in the second active region(**11a**) on a lateral side of the second sidewall, and the stress insulating film formed on the second active region(**11a**) to cover the second gate electrode(**16**), the second sidewall(**24a**), and the second source/drain region(**25**) (*See* ***§ [0058-61]***).

17. In reclaim **12**, in Fig. 4C, Fujimoto in view of Sell, teaches a semiconductor device of claim **11**, wherein no first stress-relief film is formed on the second active region.

18. Claims **10, 13-15** are rejected under 35 U.S.C. 103(a), as being anticipated by Fujimoto in view of Sell further in view of **Maeda** et al., (**US20080099786 A1**, hereinafter **Maeda**).

19. In reclaim **13**, Fujimoto in view of Sell fails to teach a semiconductor device of claim **1**, further comprising: a third MIS transistor, wherein the third MIS transistor includes a third gate insulating film formed on a third active region in the semiconductor

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substrate, a third gate electrode formed on the third gate insulating film, a third sidewall formed on a side surface of the third gate electrode, a third source/drain region of a first conductivity type which is formed in the third active region on a lateral side of the third sidewall, a protective film formed on the third active region to cover the third gate electrode, the third sidewall, and the third source/drain region, and the stress insulating film formed on the protective film.

20. But in the same field of endeavor of invention, Maeda teaches a semiconductor device of claim **1**, further comprising: a third MIS transistor, wherein the third MIS transistor includes a third gate insulating film(**110**) formed on a third active region(**104b**) in the semiconductor substrate(**100**), a third gate electrode(**XX**) formed on the third gate insulating film(**110**), a third sidewall(**124**) formed on a side surface of the third gate electrode(**130**), a third source/drain region(**128**) of a first conductivity type which is formed in the third active region(**104b**) on a lateral side of the third sidewall(**124**), a protective film(**150**) formed on the third active region(**104b**) to cover the third gate electrode(**130**), the third sidewall(**124**), and the third source/drain region(**128**), and the stress insulating film(**150**) formed on the protective film.

21. Maeda is evidence that ordinary workers skilled in the art would find reasons, suggestions or motivations to modify the device of Maeda with Fujimoto in view of Sell. Therefore, at the time the invention was made, it would have been obvious to use the teaching of Maeda in the device of Fujimoto in view of Sell since In semiconductor devices in which both NMOS devices and PMOS devices are used to perform in different modes such as analog and digital modes, stress engineering is selectively

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applied to particular devices depending on their required operational modes. That is, the appropriate mechanical stress, i.e., tensile or compressive, can be applied to and/or removed from devices, i.e., NMOS and/or PMOS devices, based not only on their conductivity type, i.e., n-type or p-type, but also on their intended operational application, for example, analog/digital, low-voltage/high-voltage, high-speed/low-speed, noise-sensitive/noise-insensitive, etc. The result is that performance of individual devices is optimized based on the mode in which they operate. For example, mechanical stress can be applied to devices that operate in high-speed digital settings, while devices that operate in analog or RF signal settings, in which electrical noise such as flicker noise that may be introduced by applied stress may degrade performance, have no stress applied (*See* ***§ [Abstract]***).

22. In reclaim **14**, in Fig. 1D, Fujimoto in view of Sell and further in view of Maeda, Sell teaches a semiconductor device of claim **13**, wherein no silicide layer is formed on the third gate electrode and the third source/drain region.

23. In reclaim **15**, in Fig. 1D, Fujimoto in view of Sell and further in view of Maeda, teaches a semiconductor device of claim **13**, wherein the first stress-relief film and the protective film are made of a same insulating material (*See* ***§ [0061]***).

24. In reclaim **10**, in Fig. 1D, Fujimoto in view of Sell and further in view of Maeda, Maeda teaches a semiconductor device of claim **1**, further comprising: an isolation region(**102**) formed in the semiconductor substrate(**100**) to surround the first active region; a gate interconnect(**pMOS in Dig Cir Area**) formed on the isolation region(**102**);

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an interconnect sidewall(**124**) formed on a side surface of the gate interconnect(**pMOS in Dig Cir Area**); a second stress-relief film(**150**) formed on a side surface of a recessed portion provided in the isolation region(**102**) on a lateral side of the interconnect sidewall(**124**); and the stress insulating film formed on the isolation region(**24b**) to cover the gate interconnect(**pMOS in Dig Cir Area**), the interconnect sidewall(**124**), and the second stress-relief film(**150**) (*See* ***§ [0079-82]***).

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Conclusion

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LAWRENCE-LINH T. NGUYEN whose telephone number is (571) 272-6267. The examiner can be reached on M-F (8AM - 4PM EST).

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fernando Toledo can be reached on (571) 272-1867. The fax phone number for the organization where this application or proceeding is assigned is (571) 272-8300.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call (800) 786-9199 (in USA or CANADA) or (571) 272-1000.

/Lawrence-Linh T Nguyen/

Examiner, Art Unit 2897

/Fernando L. Toledo/

Supervisory Patent Examiner, Art

UMC 1002
UMC v. AICP

Unit 2897

Notice of References Cited	Application/Control No. 13/528,526	Applicant(s)/Patent Under Reexamination ITOU ET AL.	
	Examiner LAWRENCE-LINH T. NGUYEN	Art Unit 2897	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2009/0065807	03-2009	FUJIMOTO, Hiromasa	257/190
*	B	US-2008/0029834	02-2008	Sell, Bernhard	257/411
*	C	US-2008/0099786	05-2008	Maeda et al.	257/190
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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BIB DATA SHEET

CONFIRMATION NO. 2414

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/528,526	06/20/2012 RULE	257	2897	085393-0792

APPLICANTS
Satoru ITOU, Hyogo, JAPAN;
Toshie Kutsunai, Osaka, JAPAN;

**** CONTINUING DATA ***************************
This application is a CON of PCT/JP2010/005117 08/19/2010

**** FOREIGN APPLICATIONS ***************************
JAPAN 2010-002225 01/07/2010

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
06/29/2012

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /LAWRENCE-LINH T NGUYEN/ Examiner's Signature	☐ Met after Allowance Initials:	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		JAPAN	10	15	1

ADDRESS
McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001
UNITED STATES

TITLE
SEMICONDUCTOR DEVICE

FILING FEE RECEIVED		
1250	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07)

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)		
	Application Number	13528526
	Filing Date	2012-06-20
	First Named Inventor	Satoru ITOU
	Art Unit	2811
	Examiner Name	Lynne Ann Gurley
	Attorney Docket Number	085393-0792

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					
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U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20110147852	A1	2011-06-23	Maeda et al.	
	2	20080099786	A1	2008-05-01	Maeda et al.	
	3	20080064157	A1	2008-03-13	Maeda et al.	
	4	20050218455	A1	2005-10-06	Maeda et al.	
	5	20030040158	A1	2003-02-27	Saitoh	

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.N./

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13528526
	Filing Date	2012-06-20
	First Named Inventor	Satoru ITOU
	Art Unit	2811
	Examiner Name	Lynne Ann Gurley
	Attorney Docket Number	085393-0792

	6	20110039379	A1	2011-02-17	NAKAGAWA et al.	
	7	20090026551	A1	2009-01-29	Nakagawa et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2008124171	JP	A	2008-05-29	Matsushita Electric Ind Co Ltd	English translation only	☒
	2	2006080161	JP	A	2006-03-23	Fujitsu Ltd	English translation	☒

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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		☐

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EXAMINER SIGNATURE

Examiner Signature	/Lawrence-Linh Nguyen/	Date Considered	08/07/2013

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.N./

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Docket No.: 085393-0792 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Satoru ITOU, et al.	:	Confirmation Number: 2414
Application No.: 13/528,526	:	Group Art Unit: 2897
Filed: June 20, 2012	:	Examiner: Lawrence-Lin NGUYEN
For: SEMICONDUCTOR DEVICE		

AMENDMENT UNDER 37 C.F.R. § 1.111

Mail Stop – Amendment
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Madam:

In response to the Office Action dated August 22, 2013 having a shortened statutory period of response set to expire on November 22, 2013, please amend the above-identified application as follows:

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IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently amended) A semiconductor device, comprising:

a first MIS transistor, wherein:

the first MIS transistor includes:

a first gate insulating film formed on a first active region in a semiconductor substrate,

a first gate electrode formed on the first gate insulating film,

a first sidewall spacer formed on a side surface of the first gate electrode,

a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region, and

a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress,

an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode, and

a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer, and

the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween.

2. (Currently amended) The semiconductor device of claim 1, further comprising:

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a first offset spacer which is formed between the first gate electrode and the first sidewall spacer, and whose cross-section has an I shape.

3. (Original) The semiconductor device of claim 1, further comprising:

a first silicide layer formed on the first gate electrode; and

a second silicide layer formed on the first source/drain region which includes the silicon compound layer.

4. (Original) The semiconductor device of claim 1, wherein the first stress-relief film is formed on a side surface of the silicon compound layer.

5. (Currently amended) The semiconductor device of claim 1, wherein the first sidewall spacer includes an inner sidewall spacer which is formed on the side surface of the first gate electrode, and whose cross-section has an L shape, and an outer sidewall spacer formed on the inner sidewall spacer.

6. (Currently amended) The semiconductor device of claim 1, wherein

the first sidewall spacer includes an inner sidewall spacer whose cross-section has an L shape, and

the stress insulating film is formed in contact with a surface of the inner sidewall spacer which is curved to have an L-shaped cross-section.

7. (Original) The semiconductor device of claim 1, wherein

the first MIS transistor is a p-type MIS transistor,

the first stress is a compressive stress, and

the second stress is a tensile stress.

8. (Original) The semiconductor device of claim 1, wherein

the silicon compound layer is a SiGe layer,

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the stress insulating film is a silicon nitride film, and

the first stress-relief film is a silicon oxide film.

9. (Original) The semiconductor device of claim 1, wherein

the first MIS transistor is an n-type MIS transistor,

the first stress is a tensile stress, and

the second stress is a compressive stress.

10. (Currently amended) The semiconductor device of claim 1, further comprising:

an isolation region formed in the semiconductor substrate to surround the first active region;

a gate interconnect formed on the isolation region;

an interconnect sidewall spacer formed on a side surface of the gate interconnect;

a second stress-relief film formed on a side surface of a recessed portion provided in the isolation region on a lateral side of the interconnect sidewall spacer; and

the stress insulating film formed on the isolation region to cover the gate interconnect, the interconnect sidewall spacer, and the second stress-relief film.

11. (Currently amended) The semiconductor device of claim 1, further comprising:

a second MIS transistor, wherein:

the second MIS transistor includes:

a second gate insulating film formed on a second active region in the semiconductor substrate,

a second gate electrode formed on the second gate insulating film,

a second sidewall spacer formed on a side surface of the second gate electrode,

a second source/drain region of a second conductivity type which is formed in the

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second active region on a lateral side of the second sidewall spacer, and

the stress insulating film formed on the second active region to cover the second gate electrode, the second sidewall spacer, and the second source/drain region.

12. (Original) The semiconductor device of claim 11, wherein no first stress-relief film is formed on the second active region.

13. (Currently amended) The semiconductor device of claim 1, further comprising:

a third MIS transistor, wherein:

the third MIS transistor includes:

a third gate insulating film formed on a third active region in the semiconductor substrate,

a third gate electrode formed on the third gate insulating film,

a third sidewall spacer formed on a side surface of the third gate electrode,

a third source/drain region of a first conductivity type which is formed in the third active region on a lateral side of the third sidewall spacer,

a protective film formed on the third active region to cover the third gate electrode, the third sidewall spacer, and the third source/drain region, and

the stress insulating film formed on the protective film.

14. (Original) The semiconductor device of claim 13, wherein no silicide layer is formed on the third gate electrode and the third source/drain region.

15. (Original) The semiconductor device of claim 13, wherein the first stress-relief film and the protective film are made of a same insulating material.

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REMARKS

I. Introduction

In response to the pending Office Action, Applicants have amended claims 1, 2, 5, 6, 10, 11 and 13 so as to further clarify the intended subject matter of the present disclosure. Support for the amendments to the claims can be found, for example, in Fig. 6B and the corresponding disclosure set forth in the specification. No new matter has been added.

For at least the reasons set forth below, it is respectfully submitted that all pending claims are patentable over the cited prior art references.

II. The Rejection Of The Claims Under 35 U.S.C. § 103

Claims 1-15 were rejected under 35 U.S.C. § 103 as being unpatentable over USP Pub. No. 2009/0065807 to Fujimoto in view of USP Pub. No. 2008/0029834 to Sell. For at least the following reasons, it is respectfully submitted that claim 1, as amended, is patentable over Fujimoto and Sell, taken alone or in combination with one another.

Claim 1 relates to a semiconductor device and as amended recites, *inter alia*, that a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer, *and that* ***the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween***.

For example, referring to the exemplary embodiment shown in Fig. 6B, the first stress-relief film 28a is formed in a space between the silicon compound layer 23 and the first sidewall spacer 19A, and ***the first stress-relief film 28a is formed on the side surface of the first gate electrode 14a with the first sidewall spacer 19a interposed therebetween***.

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Turning to the pending rejection and the cited prior art references, it is acknowledged in the pending rejection that Fujimoto does not disclose or suggest the first stress-relief film recited by claim 1. Sell is relied upon as curing this deficiency, however Sell does not do so.

More specifically, it is asserted that material layer 250 of Sell corresponds to the recited first stress-relief film, and that it would be obvious to modify Fujimoto to include this layer. Referring to Fig. 2K of Sell, Sell discloses a replacement low-k isolation spacer 270 in which a lower portion 255 is made of the material layer 250 and an upper portion 265 is made of a material layer 260.

Thus, as shown in Fig. 2K, the material layer 250 (*i.e.*, the lower portion 255) of Sell, which is asserted as corresponding to the first stress-relief film of claim 1, is formed in a space between the gate electrode 202 and the epitaxial source/drain region 218, and in **direct** contact with a side surface of the gate electrode 202. In other words, in the device of Sell, no element that corresponds to the first sidewall spacer of claim 1 is provided in a space between the side surface of the gate electrode 202 and the material layer 250 (*i.e.*, the lower portion 255).

Accordingly, even assuming *arguendo* that it is proper to modify Fujimoto to include the material layer 250 of Sell, in accordance with the teachings of Sell, the material layer 250 would be placed in **direct contact** with the gate electrode of Fujimoto, as is taught by Sell. Thus, the resulting combination of the prior art references would still fail to disclose or suggest a device in which ***the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween***, as recited by amended claim 1.

As it is well know that each and every element of the claim must be disclosed or suggested by the cited prior art references in order to establish a *prima facie* case of obviousness (*see*, M.P.E.P. § 2143.03) and the combination of Fujimoto and Sell fails to do so for at least the

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foregoing reasons, it is respectfully submitted that claim 1, as amended, is patentable over Fujimoto and Sell, taken alone or in combination.

III. Dependent Claims

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as the pending independent claim is patentable for at least the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable.

IV. Summary

Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

/Michael E. Fogarty/

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/528,526	06/20/2012	Satoru ITOU	085393-0792	2414

53080 7590 02/14/2014
McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

EXAMINER
NGUYEN, LAWRENCE-LIN T

ART UNIT	PAPER NUMBER
2897	

NOTIFICATION DATE	DELIVERY MODE
02/14/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mweipdocket@mwe.com

PTOL-90A (Rev. 04/07)

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Office Action Summary	Application No. 13/528,526	Applicant(s) ITOU ET AL.	
	Examiner LAWRENCE-LINH T. NGUYEN	Art Unit 2897	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/25/2013*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☐ Claim(s) _____ is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-15* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☒ Some** c)☐ None of the:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____

4) ☐ Other: _____.

Detailed Action

1. The present application is being examined under the pre-AIA first to invent provisions.

2. This **Final Office** action is responsive to Applicants' Amendment/Req. Reconsideration-After-Non-Final Rejection filed on **10/25/2013**. Claims **1-15** are presented for examination and claims **1-15** are rejected for the reasons indicated herein below.

3. In response to the pending Office Action, Applicants have amended claims **1, 2, 5, 6, 10, 11 and 13**. Support for the amendments to the claims can be found, for example, in Fig. 6B and the corresponding disclosure set forth in the specification. No new matter has been added.

4. Now claims **1-15** are pending.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*
>
> *The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining*

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obviousness under 35 U.S.C. 103(a) are summarized as follows: (See MPEP Ch. 2141)

Determining the scope and contents of the prior art;

Ascertaining the differences between the prior art and the claims in issue; Resolving the level of ordinary skill in the pertinent art; and Evaluating evidence of secondary considerations for indicating obviousness or nonobviousness

6. Claims **1-15** are rejected under 35 U.S.C. 103(a), as being anticipated by **Fujimoto** et al., (**US20090065807 A1**, hereinafter **Fujimoto)** in view of **Sell** et al., (**US20080029834 A1**, hereinafter **Sell**).

7. In reclaim **1**, in FIG. 1A-4C, Fujimoto teaches a semiconductor device comprising: a first MIS transistor; wherein the first MIS transistor includes:

a. a first gate insulating film(**15b**) formed on a first active region(**11b**) in a semiconductor substrate(**11**),

b. a first gate electrode(**17**) formed on the first gate insulating film(**15b**),

c. a first sidewall spacer(**24b**) formed on a side surface of the first gate electrode(**17**),

d. a first source/drain region(**25**) of a first conductivity type which is formed in a trench(**12**) provided in the first active region(**11b**) on a lateral side of the first sidewall spacer(**24b**), and which includes a silicon compound layer(**26**) causing a first stress in a gate length direction of a channel region in the first active region(**11b**), and

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e. a stress insulating film(**30A**) which is formed on the first active region(**11b**) to cover the first gate electrode(**17**), the first sidewall spacer(**24b**), and the first source/drain region(**11b**), and which causes a second stress opposite to the first stress,

f. an uppermost surface of the silicon compound layer(**28A**) is located higher than a surface of the semiconductor substrate(**11b**) located directly under the first gate electrode(**17**), and (*See* ***§ [0058-88]***).

8. In reclaim **1**, Fujimoto fails to teach a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer, and the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween.

9. But in the same field of endeavor of invention, in FIG. 2K, **Sell** teaches a first stress-relief film(**250**) is formed in a space(**255**) between the silicon compound layer(**218**) and the first sidewall(**270**), and the first stress-relief film(**250**) is formed on the side surface of the first gate electrode(**202**) with the first sidewall spacer(**265**) interposed therebetween.

10. **Sell** is evidence that ordinary workers skilled in the art would find reasons, suggestions or motivations to modify the device of **Sell** with Fujimoto. Therefore, at the time the invention was made, it would have been obvious to use the teaching of **Sell** in the device of Fujimoto since isolation spacer may provide the same physical separation and protection of the conductive region as a conventional single-component isolation

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spacer, but may also enable a reduction in fringe capacitance, i.e. "cross-talk," between conductive regions within a semiconductor structure (*See* ***§ [0009]***).

11. In reclaim **2**, in Fig. 1A, Fujimoto in view of Sell, teaches a semiconductor device of claim **1**, further comprising: a first offset spacer(**19b**) which is formed between the first gate electrode(**17**) and the first sidewall spacer(**24b**), and whose cross-section has an **I** shape (*See* ***§ [0058]***).

12. In reclaim **3**, in Fig. 3C, Fujimoto in view of Sell, teaches a semiconductor device of claim **1**, further comprising: a first silicide layer(**29**) formed on the first gate electrode(**17**); and a second silicide layer(**29**) formed on the first source/drain region(**11b**) which includes the silicon compound layer(**28**) (*See* ***§ [0068]***).

13. In reclaim **4**, in Fig. 4C, Fujimoto in view of Sell, teaches a semiconductor device of claim **1**, wherein the first stress-relief film(**30A**) is formed on a side surface of the silicon compound layer (*See* ***§ [0077]***).

14. In reclaim **5**, in Fig. 1C, Fujimoto in view of Sell, teaches a semiconductor device of claim **1**, wherein the first sidewall spacer(**24b**) includes an inner sidewall spacer(**22**) which is formed on the side surface of the first gate electrode(**17**), and whose cross-section has an L shape, and an outer sidewall spacer(**24b**) formed on the inner sidewall (*See* ***§ [0059]***).

15. In reclaim **6**, in Fig. 1C, Fujimoto in view of Sell, teaches a semiconductor device of claim **1**, wherein the first sidewall spacer (**24b**) includes an inner sidewall spacer(**22**)

whose cross-section has an L shape, and the stress insulating film is formed in contact with a surface of the inner sidewall which is curved to have an L-shaped cross-section (*See* ***§ [0061]***).

16. In reclaim **7**, in Fig. 1A, Fujimoto in view of Sell, teaches a semiconductor device of claim **1**, wherein the first MIS transistor is a p-type MIS transistor, the first stress is a compressive stress, and the second stress is a tensile stress (*See* ***§ [0058]***).

17. In reclaim **8**, in Fig. 1A, Fujimoto in view of Sell, teaches a semiconductor device of claim **1**, wherein the silicon compound layer is a SiGe layer, the stress insulating film is a silicon nitride film, and the first stress-relief film is a silicon oxide film (*See* ***§*** *[*Fujimoto *(**0065,0075**), & Sell (**0029**)]*).

18. In reclaim **9**, in Fig. 1A, Fujimoto in view of Sell, teaches a semiconductor device of claim **1**, wherein the first MIS transistor is an n-type MIS transistor, the first stress is a tensile stress, and the second stress is a compressive stress (*See* ***§ [0058]***).

19. In reclaim **11**, in Fig. 1A-D, Fujimoto in view of Sell, teaches a semiconductor device of claim **1**, further comprising: a second MIS transistor, wherein the second MIS transistor includes a second gate insulating film(**15a**) formed on a second active region(**11a**) in the semiconductor substrate(**11**), a second gate electrode(**16**) formed on the second gate insulating film(**15a**), a second sidewall spacer(**24b**) formed on a side surface of the second gate electrode(**16**), a second source/drain region(**25**) of a second conductivity type which is formed in the second active region(**11a**) on a lateral side of the second sidewall spacer(**24b**), and the stress insulating film formed on the second

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active region(**11a**) to cover the second gate electrode(**16**), the second sidewall(**24a**), and the second source/drain region(**25**) (*See* ***§ [0058-61]***).

20. In reclaim **12**, in Fig. 4C, Fujimoto in view of Sell, teaches a semiconductor device of claim **11**, wherein no first stress-relief film is formed on the second active region.

21. Claims **10, 13-15** are rejected under 35 U.S.C. 103(a), as being anticipated by Fujimoto in view of Sell further in view of **Maeda** et al., (**US20080099786 A1**, hereinafter **Maeda**).

22. In reclaim **13**, Fujimoto in view of Sell fails to teach a semiconductor device of claim **1**, further comprising: a third MIS transistor, wherein the third MIS transistor includes a third gate insulating film formed on a third active region in the semiconductor substrate, a third gate electrode formed on the third gate insulating film, a third sidewall formed on a side surface of the third gate electrode, a third source/drain region of a first conductivity type which is formed in the third active region on a lateral side of the third sidewall, a protective film formed on the third active region to cover the third gate electrode, the third sidewall, and the third source/drain region, and the stress insulating film formed on the protective film.

23. But in the same field of endeavor of invention, Maeda teaches a semiconductor device of claim **1**, further comprising: a third MIS transistor, wherein the third MIS transistor includes a third gate insulating film(**110**) formed on a third active region(**104b**) in the semiconductor substrate(**100**), a third gate electrode(**XX**) formed on the third gate

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insulating film(**110**), a third sidewall spacer(**124**) formed on a side surface of the third gate electrode(**130**), a third source/drain region(**128**) of a first conductivity type which is formed in the third active region(**104b**) on a lateral side of the third sidewall spacer(**124**), a protective film(**150**) formed on the third active region(**104b**) to cover the third gate electrode(**130**), the third sidewall spacer(**124**), and the third source/drain region(**128**), and the stress insulating film(**150**) formed on the protective film.

24. Maeda is evidence that ordinary workers skilled in the art would find reasons, suggestions or motivations to modify the device of Maeda with Fujimoto in view of Sell. Therefore, at the time the invention was made, it would have been obvious to use the teaching of Maeda in the device of Fujimoto in view of Sell since In semiconductor devices in which both NMOS devices and PMOS devices are used to perform in different modes such as analog and digital modes, stress engineering is selectively applied to particular devices depending on their required operational modes. That is, the appropriate mechanical stress, i.e., tensile or compressive, can be applied to and/or removed from devices, i.e., NMOS and/or PMOS devices, based not only on their conductivity type, i.e., n-type or p-type, but also on their intended operational application, for example, analog/digital, low-voltage/high-voltage, high-speed/low-speed, noise-sensitive/noise-insensitive, etc. The result is that performance of individual devices is optimized based on the mode in which they operate. For example, mechanical stress can be applied to devices that operate in high-speed digital settings, while devices that operate in analog or RF signal settings, in which electrical noise such as flicker noise that may be introduced by applied stress may degrade performance.

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have no stress applied (*See* ***§ [Abstract]***).

25. In reclaim **14**, in Fig. 8, Fujimoto in view of Sell and further in view of Maeda, Maeda teaches a semiconductor device of claim **13**, wherein no silicide layer is formed on the third gate electrode and the third source/drain region.

26. In reclaim **15**, in Fig. 1D, Fujimoto in view of Sell and further in view of Maeda, teaches a semiconductor device of claim **13**, wherein the first stress-relief film and the protective film are made of a same insulating material (*See* ***§ [0061]***).

27. In reclaim **10**, in Fig. 8, Fujimoto in view of Sell and further in view of Maeda, Maeda teaches a semiconductor device of claim **1**, further comprising: an isolation region(**102**) formed in the semiconductor substrate(**100**) to surround the first active region; a gate interconnect(**pMOS in Dig Cir Area**) formed on the isolation region(**102**); an interconnect sidewall spacer(**124**) formed on a side surface of the gate interconnect(**pMOS in Dig Cir Area**); a second stress-relief film(**150**) formed on a side surface of a recessed portion provided in the isolation region(**102**) on a lateral side of the interconnect sidewall spacer(**124**); and the stress insulating film formed on the isolation region(**24b**) to cover the gate interconnect(**pMOS in Dig Cir Area**), the interconnect sidewall spacer(**124**), and the second stress-relief film(**150**) (*See* ***§ [0079-82]***).

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Response to Applicant's Remarks

28. With respect to the claims, the following are addressed:

29. Applicant's arguments filed with respect to the claim **1**, under USC 103(a) have been fully considered but they are not persuasive.

30. The Applicant argues that accordingly, even assuming *arguendo* that it is proper to modify Fujimoto to include the material layer 250 of Sell, in accordance with the teachings of Sell, the material layer 250 would be placed in direct contact with the gate electrode of Fujimoto, as is taught by Sell. Thus, the resulting combination of the prior art references would still fail to disclose or suggest a device in which *the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween,* as recited by amended claim 1.

31. As it is shown in FIG. 2K, *the first stress-relief film(**255**) is formed on the side surface of the first gate electrode(**255**) with the first sidewall spacer(**265**) interposed therebetween i.e. the right triangle sides of the first sidewall spacer(**265**)is bordering with the first gate electrode(**255**) and the first stress-relief film(**255**). The claim language does not specify whether it can or cannot be* in direct contact with a side surface of the gate electrode(202).

32. In view of the prior art have been shown to disclose the limitations of the claims, the rejection of claims 1-15 is maintained as previously cited based on Fujimoto in view of Sell and further in view of Maeda.

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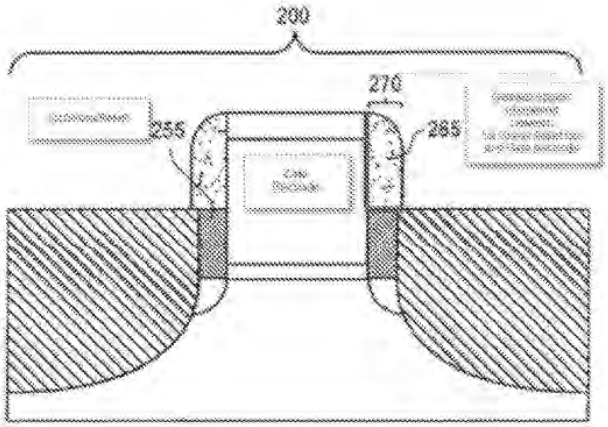

FIG. 2K

FIG. 2K – Illustration of the First Sidewall Spacer(**265**) interposed between First Stress Relief film(**255**) and Gate Electrode(**202**)

Conclusion

33. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

34. A shortened statutory period for reply to this final action is set to expire THREE(3) MONTHS from the mailing date of this action. In the event a first reply is filed within TWO(2) MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE(3)-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX(6) MONTHS from the mailing date of this final action

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LAWRENCE-LINH T. NGUYEN whose telephone number is (571) 272-6267. The examiner can be reached on M-F (8AM - 4PM EST).

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fernando Toledo can be reached on (571) 272-1867. The fax phone number for the organization where this application or proceeding is assigned is (571) 272-8300.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

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published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call (800) 786-9199 (in USA or CANADA) or (571) 272-1000.

/Lawrence-Linh T Nguyen/

Examiner, Art Unit 2897

/Fernando L. Toledo/

Supervisory Patent Examiner, Art Unit 2897

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Notice of References Cited	Application/Control No. 13/528,526	Applicant(s)/Patent Under Reexamination ITOU ET AL.	
	Examiner LAWRENCE-LINH T. NGUYEN	Art Unit 2897	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2009/0065807	03-2009	FUJIMOTO, Hiromasa	257/190
*	B	US-2008/0029834	02-2008	Sell, Bernhard	257/411
*	C	US-2008/0099786	05-2008	Maeda et al.	257/190
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Docket No.: 085393-0792 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Satoru ITOU, et al.	:	Confirmation Number: 2414
	:	
Application No.: 13/528,526	:	Group Art Unit: 2897
	:	
Filed: June 20, 2012	:	Examiner: Lawrence-Lin NGUYEN
	:	
For: SEMICONDUCTOR DEVICE		

AMENDMENT WITH RCE

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Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Madam:

In response to the Office Action dated February 14, 2014 having a shortened statutory period of response set to expire on May 14, 2014, please amend the above-identified application as set forth below.

A Request for Continued Examination is being filed concurrently herewith.

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IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently amended) A semiconductor device, comprising:

a first MIS transistor, wherein:

the first MIS transistor includes:

a first gate insulating film formed on a first active region in a semiconductor substrate,

a first gate electrode formed on the first gate insulating film,

a first sidewall spacer formed on a side surface of the first gate electrode,

a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region, and

a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress,

an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode, [[and]]

a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer, [[and]]

the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween, and

the first stress-relief film is not in direct contact with the side surface of the first gate

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electrode.

2. (Previously presented) The semiconductor device of claim 1, further comprising:

a first offset spacer which is formed between the first gate electrode and the first sidewall spacer, and whose cross-section has an I shape.

3. (Original) The semiconductor device of claim 1, further comprising:

a first silicide layer formed on the first gate electrode; and

a second silicide layer formed on the first source/drain region which includes the silicon compound layer.

4. (Original) The semiconductor device of claim 1, wherein the first stress-relief film is formed on a side surface of the silicon compound layer.

5. (Previously presented) The semiconductor device of claim 1, wherein the first sidewall spacer includes an inner sidewall spacer which is formed on the side surface of the first gate electrode, and whose cross-section has an L shape, and an outer sidewall spacer formed on the inner sidewall spacer.

6. (Previously presented) The semiconductor device of claim 1, wherein

the first sidewall spacer includes an inner sidewall spacer whose cross-section has an L shape, and

the stress insulating film is formed in contact with a surface of the inner sidewall spacer which is curved to have an L-shaped cross-section.

7. (Original) The semiconductor device of claim 1, wherein

the first MIS transistor is a p-type MIS transistor,

the first stress is a compressive stress, and

the second stress is a tensile stress.

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8. (Original) The semiconductor device of claim 1, wherein

the silicon compound layer is a SiGe layer,

the stress insulating film is a silicon nitride film, and

the first stress-relief film is a silicon oxide film.

9. (Original) The semiconductor device of claim 1, wherein

the first MIS transistor is an n-type MIS transistor,

the first stress is a tensile stress, and

the second stress is a compressive stress.

10. (Previously presented) The semiconductor device of claim 1, further comprising:

an isolation region formed in the semiconductor substrate to surround the first active region;

a gate interconnect formed on the isolation region;

an interconnect sidewall spacer formed on a side surface of the gate interconnect;

a second stress-relief film formed on a side surface of a recessed portion provided in the isolation region on a lateral side of the interconnect sidewall spacer; and

the stress insulating film formed on the isolation region to cover the gate interconnect, the interconnect sidewall spacer, and the second stress-relief film.

11. (Previously presented) The semiconductor device of claim 1, further comprising:

a second MIS transistor, wherein:

the second MIS transistor includes:

a second gate insulating film formed on a second active region in the semiconductor substrate,

a second gate electrode formed on the second gate insulating film,

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a second sidewall spacer formed on a side surface of the second gate electrode,

a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer, and

the stress insulating film formed on the second active region to cover the second gate electrode, the second sidewall spacer, and the second source/drain region.

12. (Original) The semiconductor device of claim 11, wherein no first stress-relief film is formed on the second active region.

13. (Previously presented) The semiconductor device of claim 1, further comprising:

a third MIS transistor, wherein:

the third MIS transistor includes:

a third gate insulating film formed on a third active region in the semiconductor substrate,

a third gate electrode formed on the third gate insulating film,

a third sidewall spacer formed on a side surface of the third gate electrode,

a third source/drain region of a first conductivity type which is formed in the third active region on a lateral side of the third sidewall spacer,

a protective film formed on the third active region to cover the third gate electrode, the third sidewall spacer, and the third source/drain region, and

the stress insulating film formed on the protective film.

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14. (Original) The semiconductor device of claim 13, wherein no silicide layer is formed on the third gate electrode and the third source/drain region.

15. (Original) The semiconductor device of claim 13, wherein the first stress-relief film and the protective film are made of a same insulating material.

REMARKS

I. Introduction

In response to the pending Office Action, Applicants have amended claim 1 so as to further clarify the intended subject matter of the present disclosure. Support for the amendment to the claim can be found, for example, in paragraph [0084] and Fig. 5B of the published application (*see*, USP Pub. No. 2012/0256266). No new matter has been added.

For at least the reasons set forth below, it is respectfully submitted that all pending claims are patentable over the cited prior art references.

II. The Rejection Of The Claims Under 35 U.S.C. § 103

Claims 1-15 were rejected under 35 U.S.C. § 103 as being unpatentable over USP Pub. No. 2009/0065807 to Fujimoto in view of USP Pub. No. 2008/0029834 to Sell. For at least the following reasons, it is respectfully submitted that claim 1, as amended, is patentable over Fujimoto and Sell, taken alone or in combination with one another.

Claim 1 relates to a semiconductor device and recites, *inter alia*, that a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer, and that the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween. As amended, claim 1 now further expressly recites that ***the first stress-relief film is not in direct contact with the side surface of the first gate electrode***.

For example, referring to the exemplary embodiment shown in Fig. 5B, the first stress-relief film 28a is formed in a space between the silicon compound layer 23 and the first sidewall

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spacer 19A, and the first stress-relief film 28a is formed on the side surface of the first gate electrode 14a with the first sidewall spacer 19a interposed therebetween. ***Further, the first stress-relief film 28a <u>is not in direct contact</u> with the side surface of the first gate electrode 14a***. It is noted that the foregoing amendment is intended to address the Examiner's interpretation of the prior art set forth in the Response to Arguments section of the Office Action.

Turning to the pending rejection and the cited prior art references, it is acknowledged in the pending rejection that Fujimoto does not disclose or suggest the first stress-relief film recited by claim 1. Sell is relied upon as curing this deficiency. However Sell does not do so.

More specifically, it is asserted that although the alleged first stress-relief film 255 of Sell is in direct contact with the first gate electrode 202, the first sidewall spacer 265 is also disposed between the first stress-relief film 255 and the first gate electrode 202. As noted in the Response to the Arguments section, it appears to be asserted that the upper surface of the first-stress relief film 255 is separated from an upper side surface of the first gate electrode 202 by the first sidewall spacer 265.

In response to the foregoing, Applicants have amended claim 1 to expressly state that ***the first stress-relief film <u>is not in direct contact</u> with the side surface of the first gate electrode***. Clearly, Sell does not disclose or suggest this element of amended claim 1. As noted above, and clearly shown in the figures of Sell, the asserted first stress-relief film 255 of Sell **<u>is in direct</u>** contact with a side surface of the gate electrode 202.

Accordingly, even assuming *arguendo* that it is proper to modify Fujimoto to include the material layer 250 of Sell, in accordance with the teachings of Sell, the material layer 250 would be placed in **<u>direct contact</u>** with the gate electrode of Fujimoto, as is taught by Sell. Thus, at a minimum, the resulting combination of the prior art references would still fail to disclose or

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suggest a device in which ***the first stress-relief film <u>is not in direct contact</u> with the side surface of the first gate electrode***, as recited by amended claim 1.

As it is well know that each and every element of the claim must be disclosed or suggested by the cited prior art references in order to establish a *prima facie* case of obviousness (*see*, M.P.E.P. § 2143.03) and the combination of Fujimoto and Sell fails to do so for at least the foregoing reasons, it is respectfully submitted that claim 1, as amended, is patentable over Fujimoto and Sell, taken alone or in combination.

III. Dependent Claims

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as the pending independent claim is patentable for at least the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable.

IV. Summary

Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper.

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

/Michael E. Fogarty/

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

500 North Capitol Street, N.W.
Washington, DC 20001
Phone: 202.756.8000 MEF:
Facsimile: 202.756.8087
Date: May 9, 2014

DM_US 51543182-1.085393.0792

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

53080 7590 10/07/2014
McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

EXAMINER
NGUYEN, LAWRENCE-LIN T

ART UNIT	PAPER NUMBER
2897	

DATE MAILED: 10/07/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/528,526	06/20/2012	Satoru ITOU	085393-0792	2414

TITLE OF INVENTION: SEMICONDUCTOR DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	01/07/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

53080 7590 10/07/2014
McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/528,526	06/20/2012	Satoru ITOU	085393-0792	2414

TITLE OF INVENTION: SEMICONDUCTOR DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	01/07/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, LAWRENCE-LIN T	2897	257-368000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.
(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/528,526	06/20/2012	Satoru ITOU	085393-0792	2414

53080 7590 10/07/2014
McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

EXAMINER
NGUYEN, LAWRENCE-LIN T

ART UNIT	PAPER NUMBER
2897	

DATE MAILED: 10/07/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UMC 1002
UMC v. AICP

Notice of Allowability	Application No. 13/528,526	Applicant(s) ITOU ET AL.	
	Examiner LAWRENCE-LINH T. NGUYEN	Art Unit 2897	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *05/09/2014*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-15*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☒ All b) ☐ Some *c) ☐ None of the:
   1. ☒ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/LAWRENCE-LINH T NGUYEN/
Examiner, Art Unit 2897

DETAIL ACTION

Allowable Subject Matter

1. The present application is being examined under the pre-AIA first to invent provisions.

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on **May 09, 2014** has been entered.

3. Applicant's arguments, see Response After Final, filed **05/09/2014**, with respect to independent claim **1** have been fully considered and are persuasive. The **103** rejection of independent claim **1** is withdrawn.

4. The following is an examiner's statement of reasons for allowance:

   a. With respect to independent claim **1**, the prior art teaches:

      i. A semiconductor device, comprising: a first MIS transistor, wherein: the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate, a first gate electrode formed on the first gate insulating film, a first sidewall spacer formed on a side surface of the first gate electrode, a first source/drain region of a first

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conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region, and a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress, an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode, a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer, the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween, and the first stress-relief film is not **in** direct contact with the side surface of the first gate

ii. But the prior arts of record do not teach or fairly suggest a limitation of: the first stress-relief film is not **in** direct contact with the side surface of the first gate.

iii. Claims **2-15** are depended on claim **1**.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

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Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **LAWRENCE-LINH T. NGUYEN** whose telephone number is **(571) 272-6267** and fax number is **(571) 273-6267**. The examiner can normally be reached on M-F (Flex hours). If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Fernando Toledo** can be reached on **571-272-1867**. The fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Fernando L. Toledo/

Supervisory Patent Examiner, Art Unit 2897

/LAWRENCE-LINH T NGUYEN/

Examiner, Art Unit 2897

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/528,526	12/09/2014	8907425	085393-0792	2414

53080 7590 11/19/2014
McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 30 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Satoru ITOU, Hyogo, JAPAN;
Toshie Kutsunai, Osaka, JAPAN;

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IR103 (Rev. 10/09)

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/528,526	Filing Date 06/20/2012	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT

01/20/2016	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 25	Minus	** 25	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SLIE
/WANDA BROWN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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