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Fukutome et al.

(54) SEMICONDUCTOR DEVICE, METHOD OF MANUFACTURING THE SAME, AND METHOD OF EVALUATING SEMICONDUCTOR DEVICE

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(30) **Foreign Application Priority Data**

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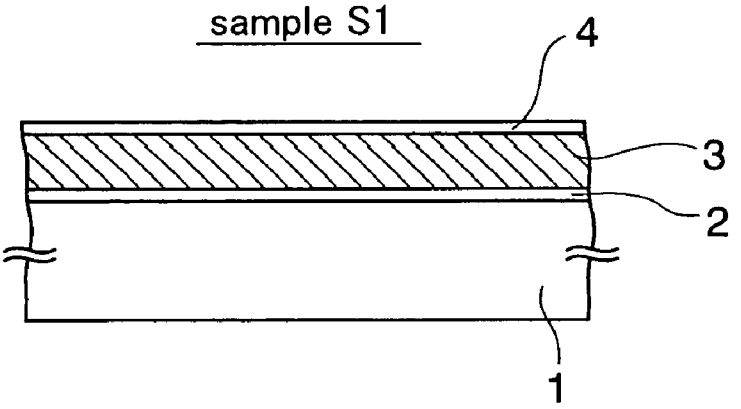
(51) **Int. Cl.**[7] **H01L 29/76**

(52) **U.S. Cl.** **257/368**

(57) **ABSTRACT**

A semiconductor device has: a silicon (semiconductor) substrate; a gate insulating film and a gate electrode, which are formed on the silicon substrate in this order; and source/drain material layers formed in recesses (holes) in the silicon substrate, the recesses being located beside the gate electrode. Here, each of side surfaces of the recesses, which are closer to the gate electrode, is constituted of at least one crystal plane of the silicon substrate.



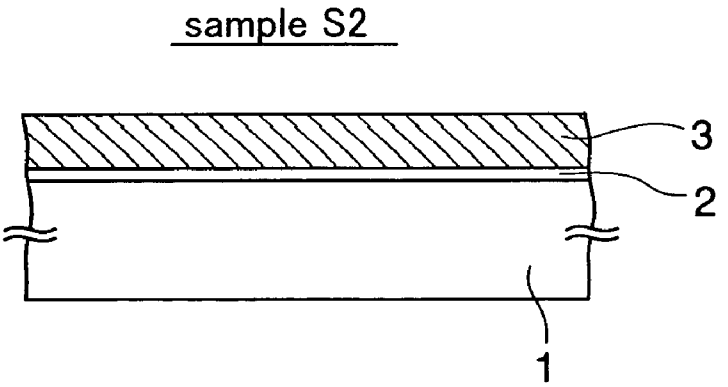


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FIG. 1

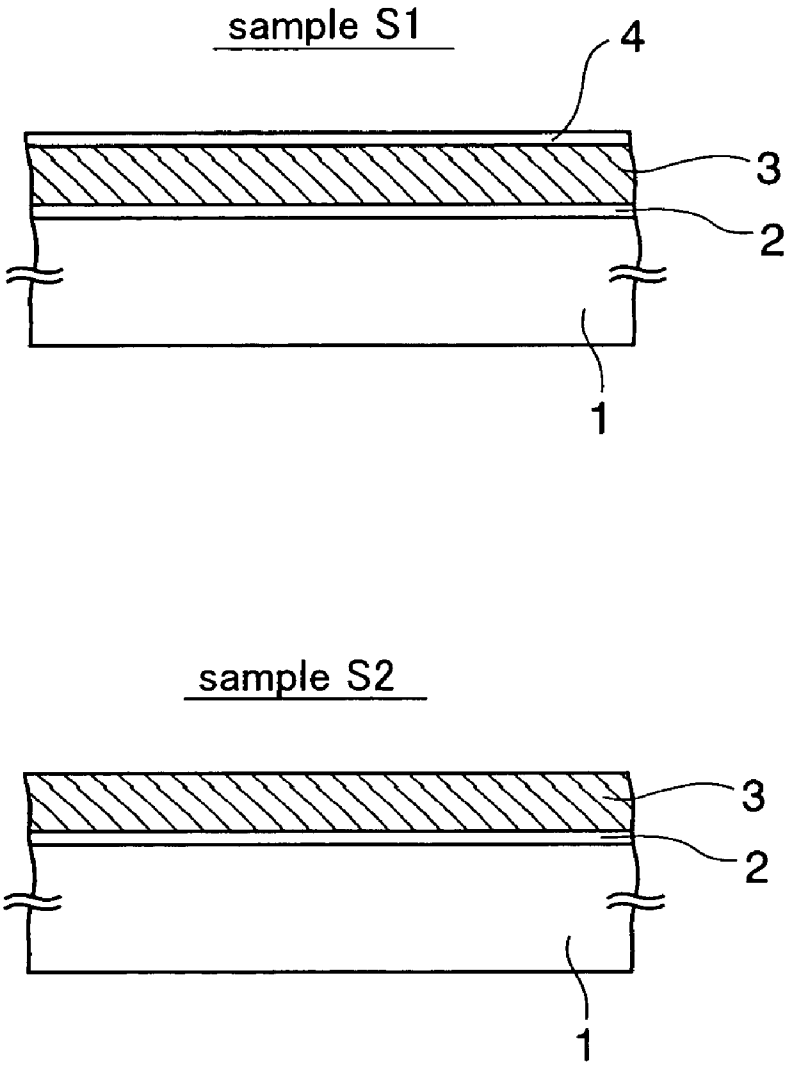

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FIG. 2

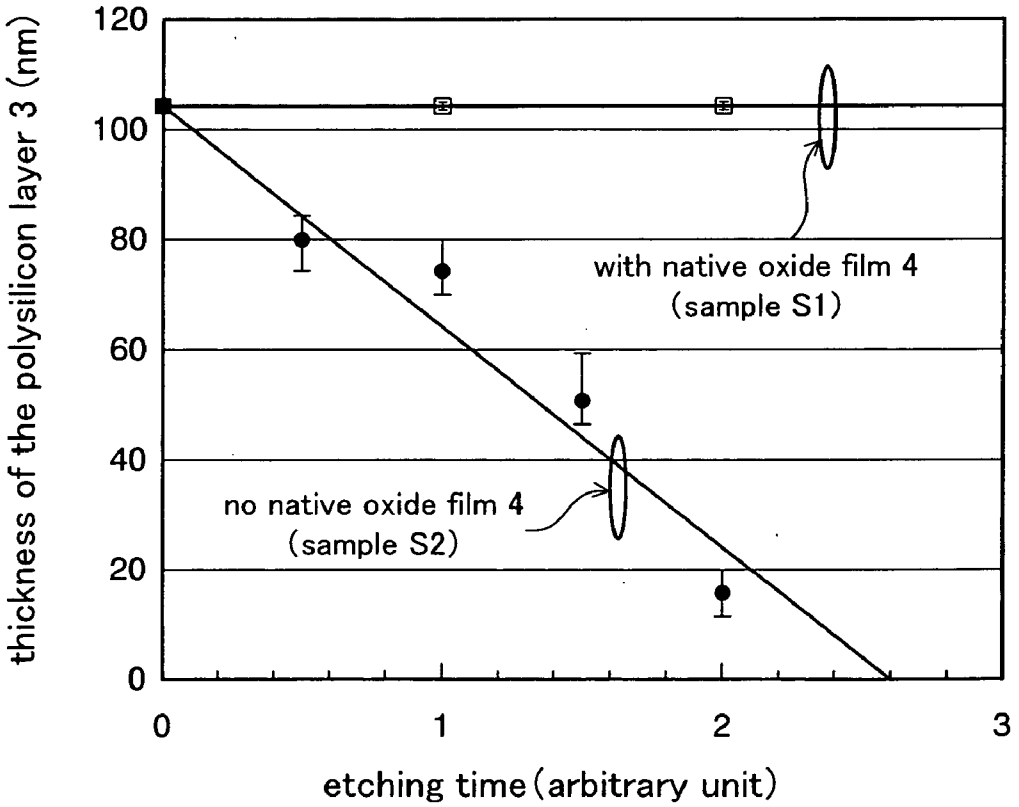
thickness of the polysilicon layer 3 (nm)
120
100
80
60
40
20
0
0
1
2
3
etching time (arbitrary unit)
with native oxide film 4
(sample S1)
no native oxide film 4
(sample S2)

FIG. 3

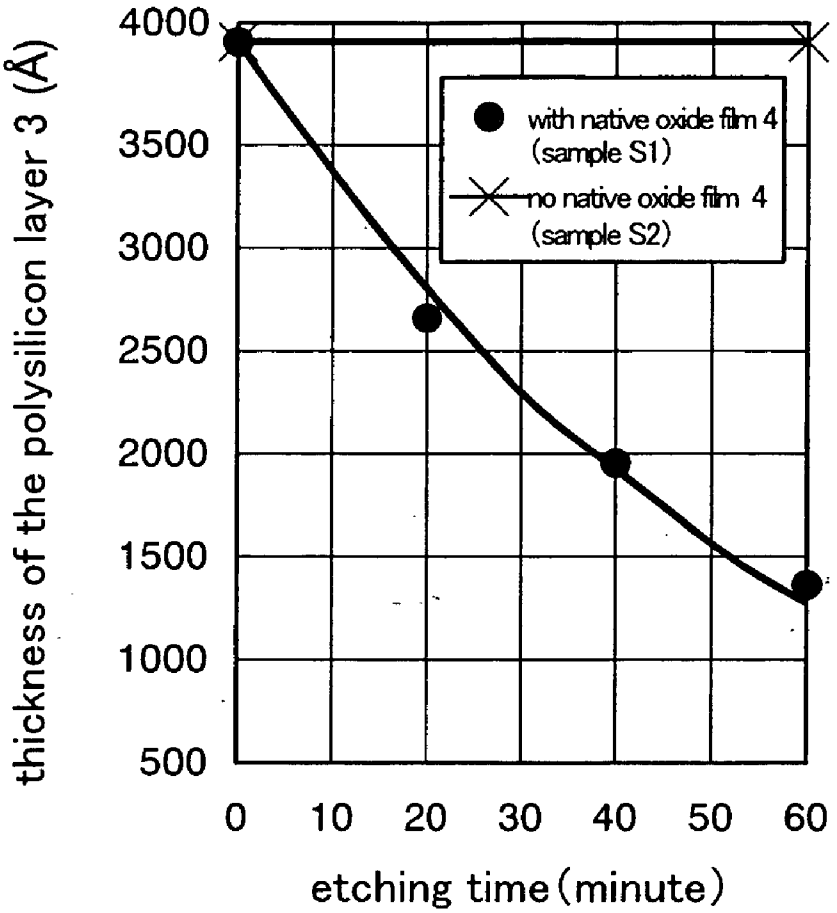

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FIG. 4

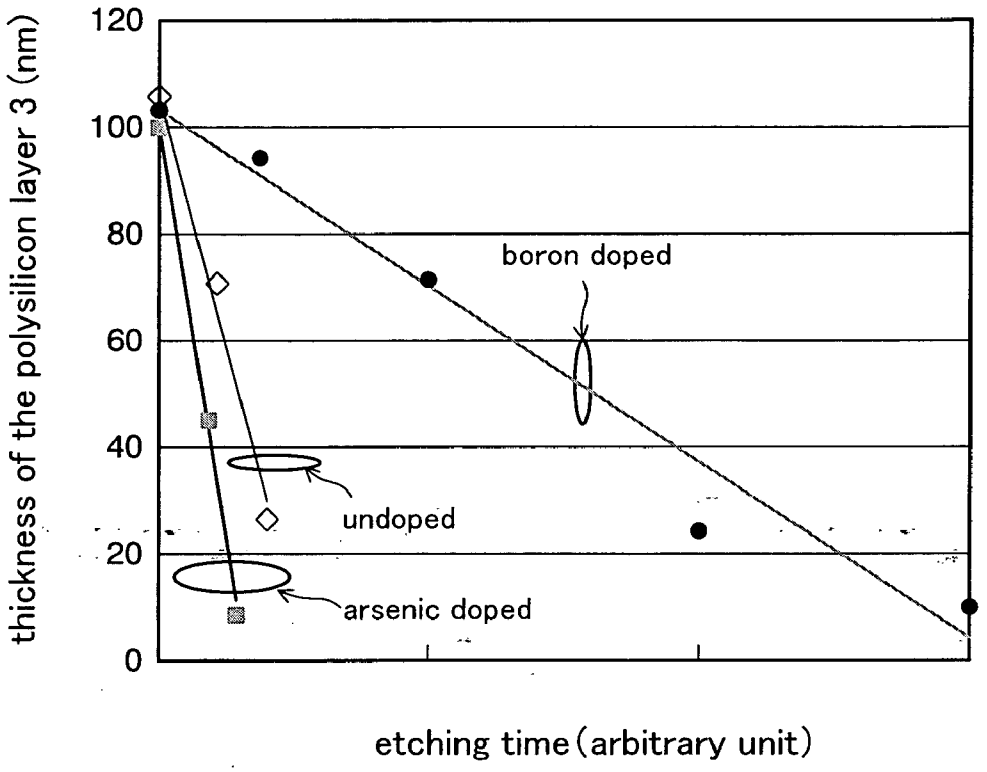
thickness of the polysilicon layer 3 (nm)
120
100
80
60
40
20
0
boron doped
undoped
arsenic doped
etching time (arbitrary unit)

FIG. 5A

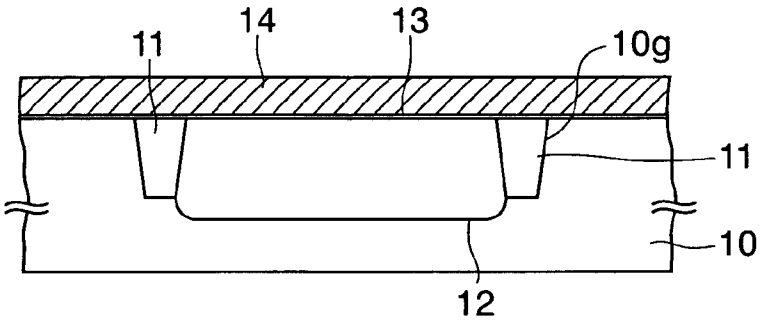

FIG. 5B

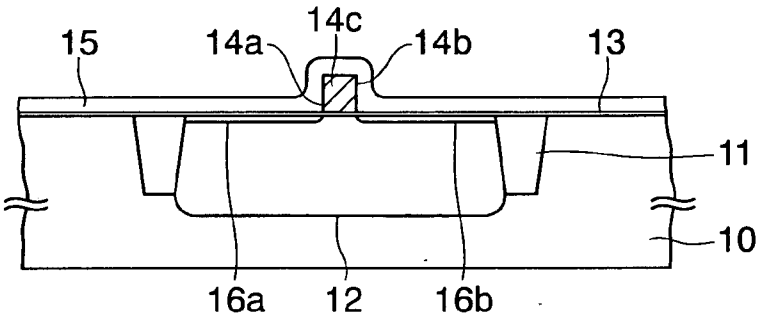

FIG. 5C

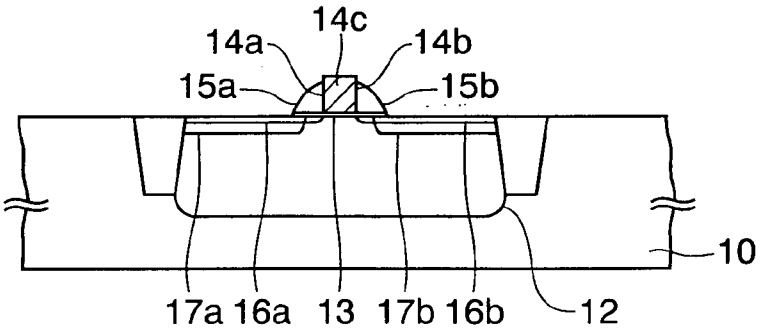

FIG. 5D

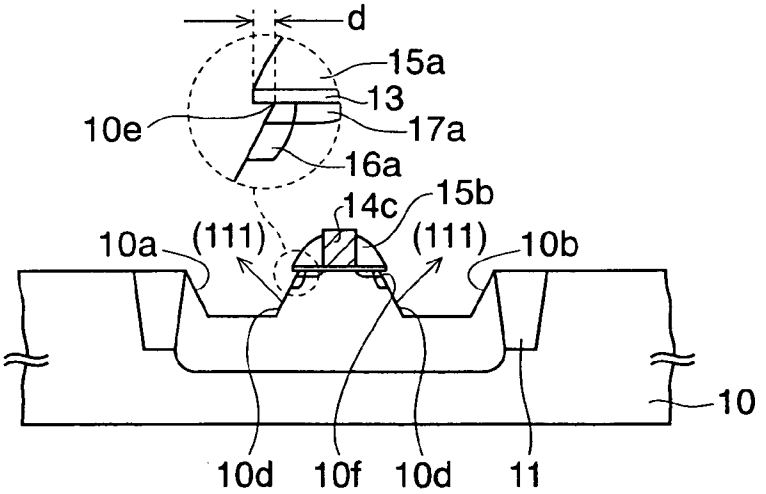

FIG. 5E

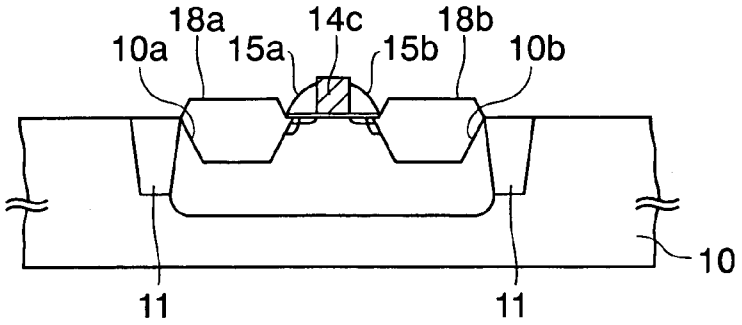

FIG. 5F

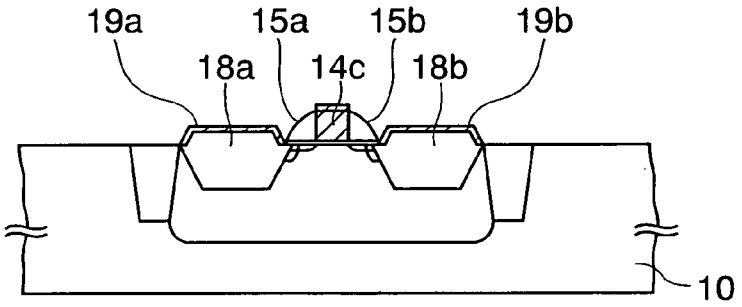

FIG. 5G

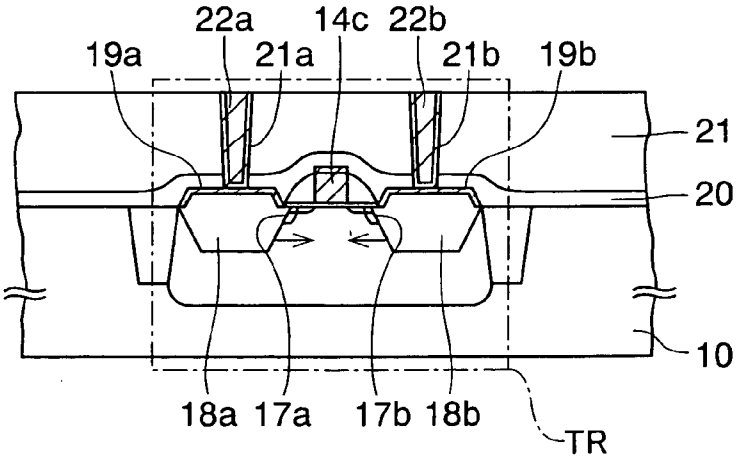

FIG. 6

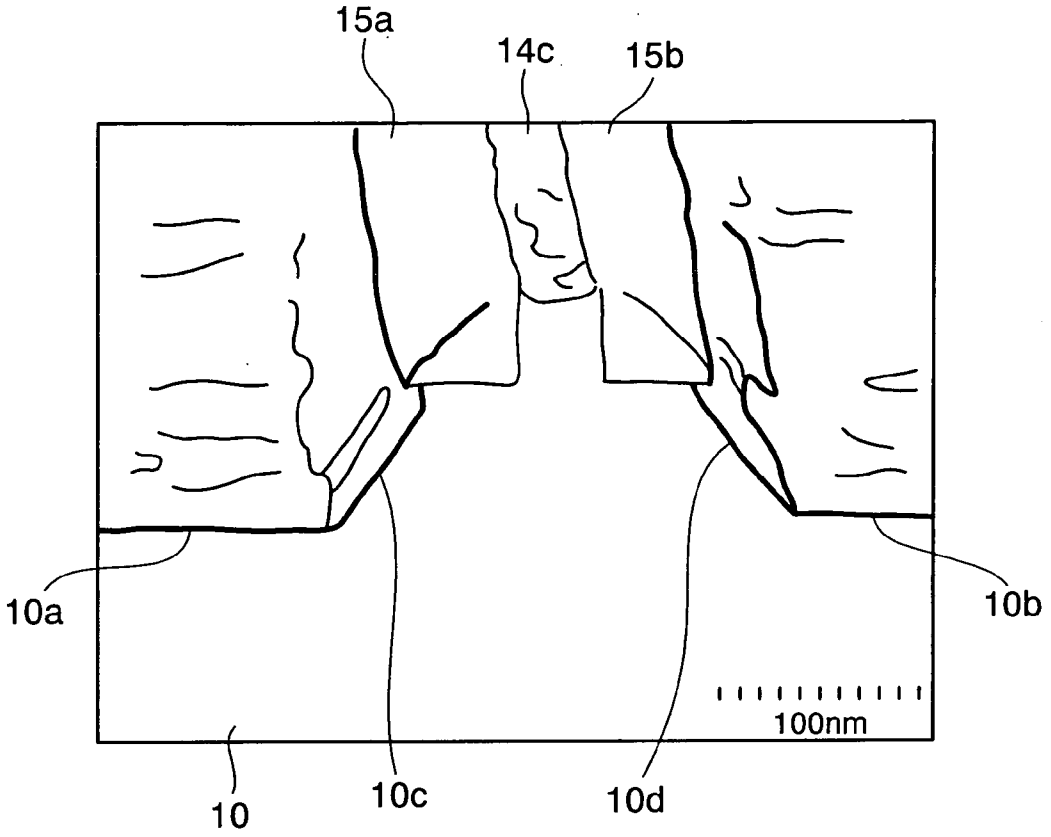

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FIG. 7

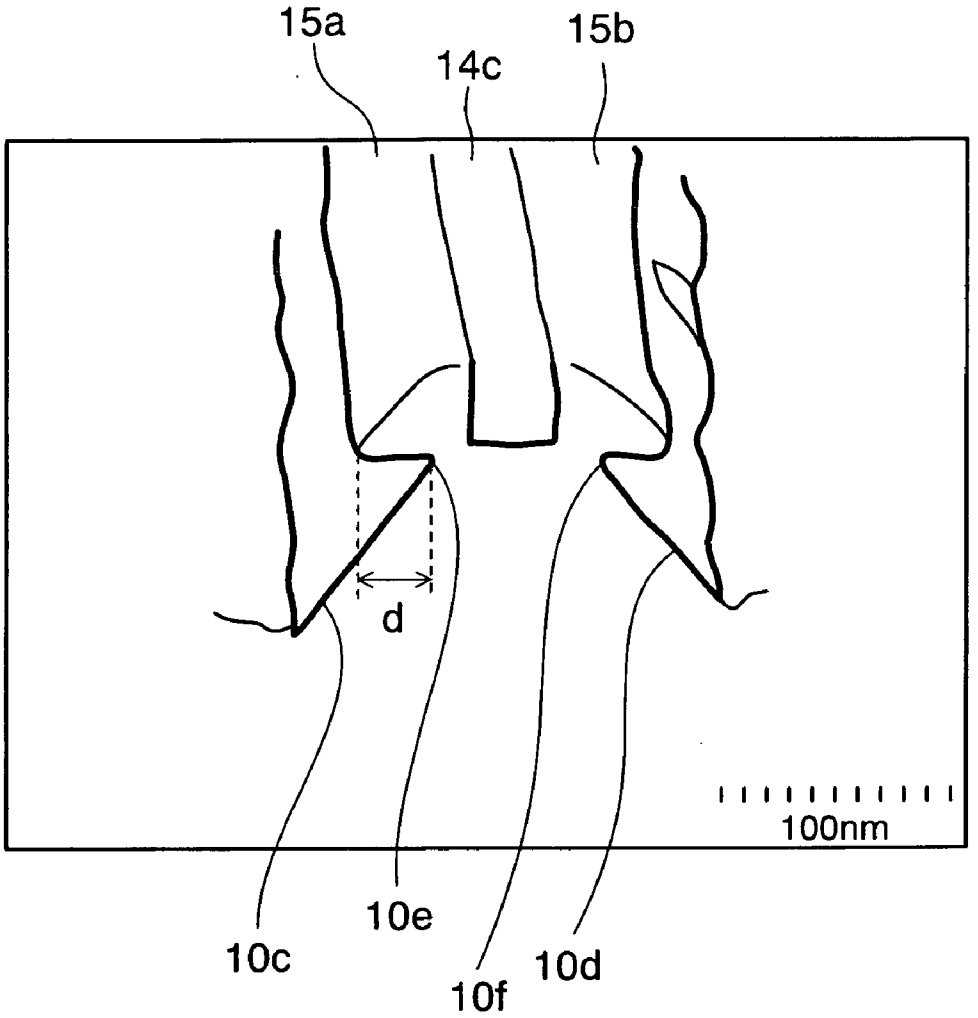

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FIG. 8A

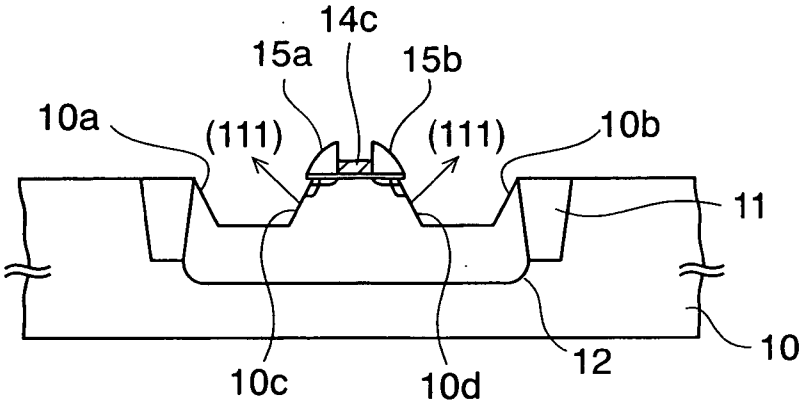

FIG. 8B

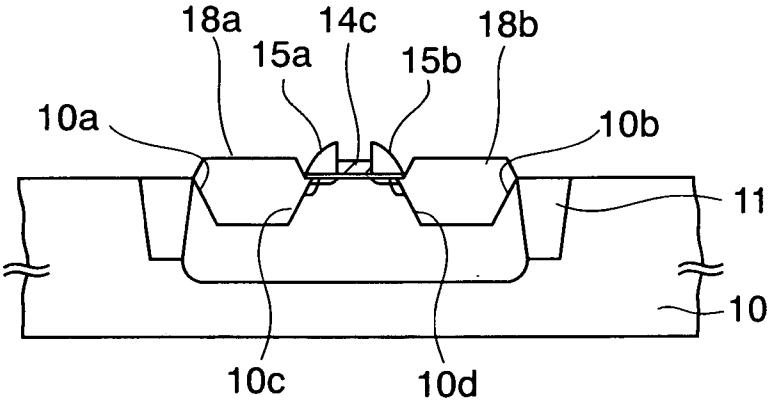

FIG. 8C

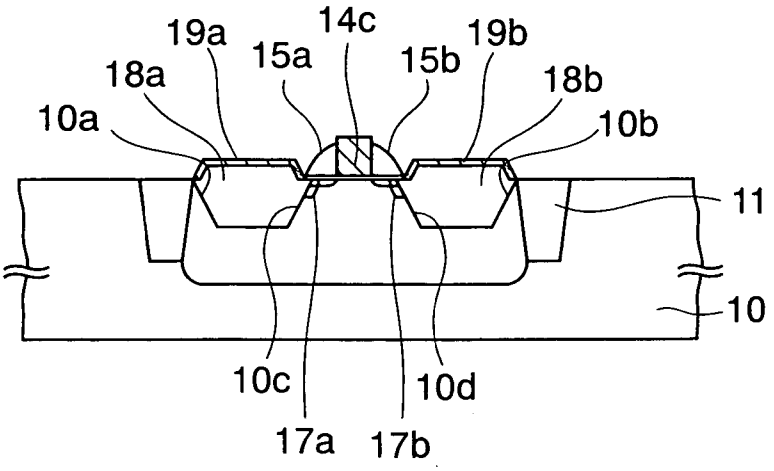

FIG. 9A

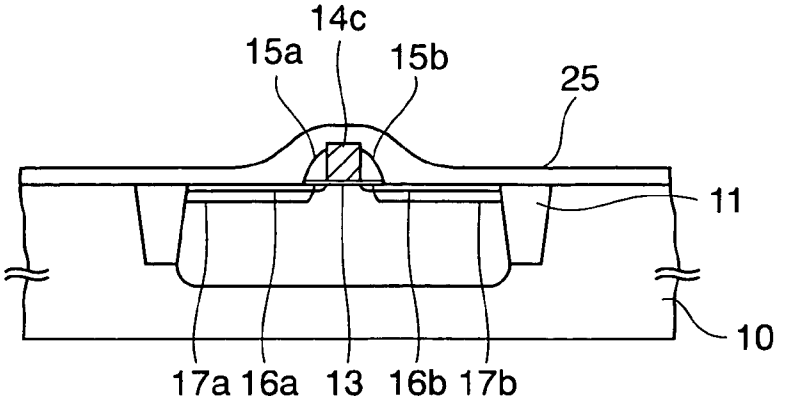

FIG. 9B

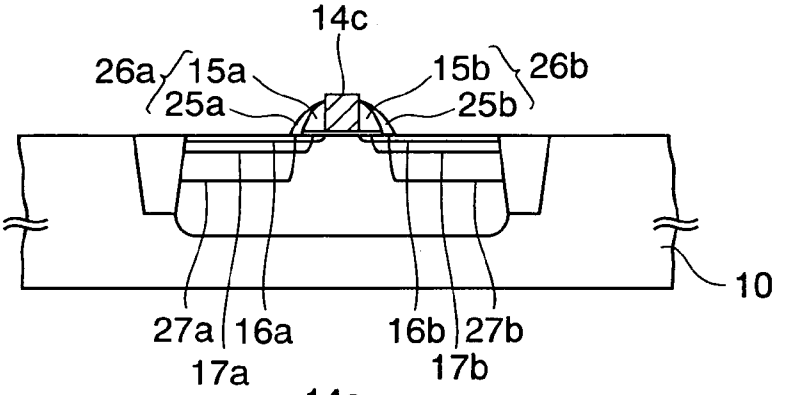

FIG. 9C

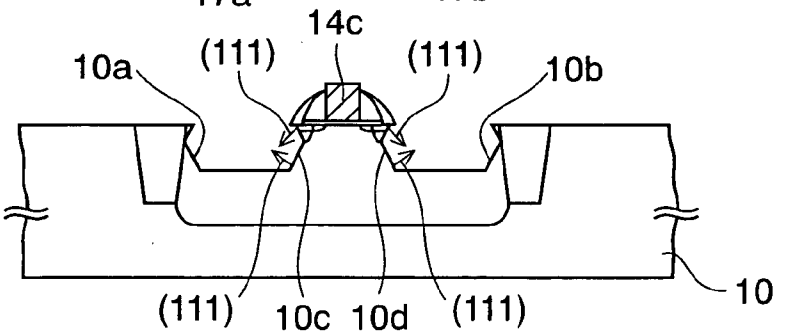

FIG. 9D

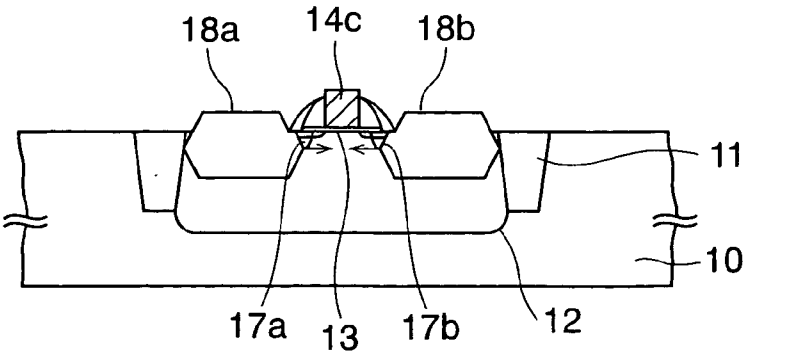

FIG. 10

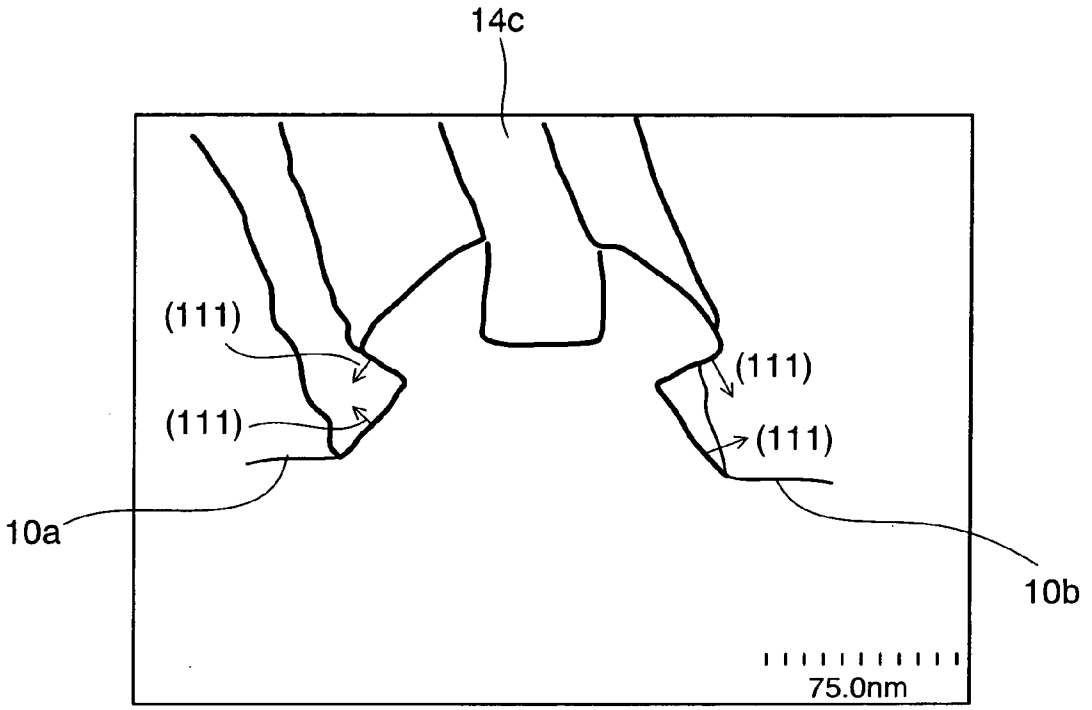

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FIG. 11A

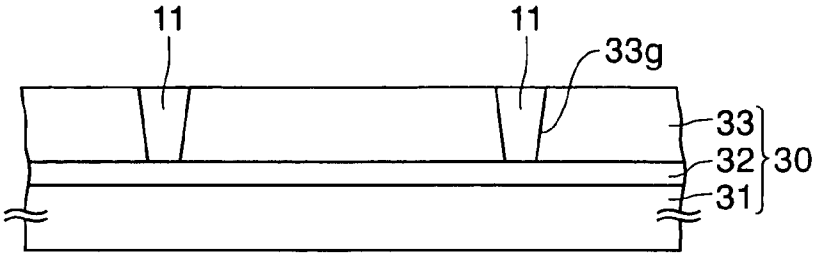

FIG. 11B

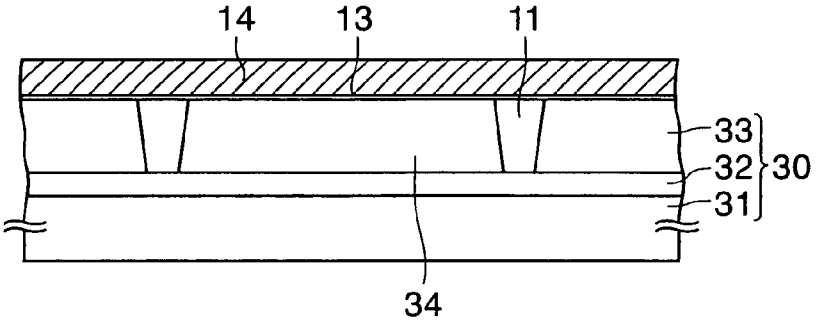

FIG. 11C

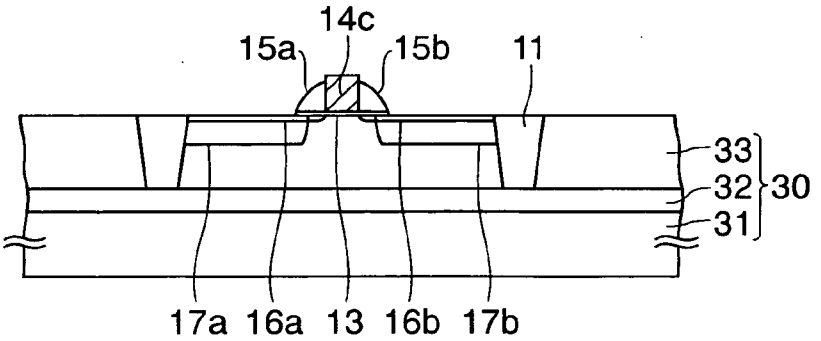

FIG. 11D

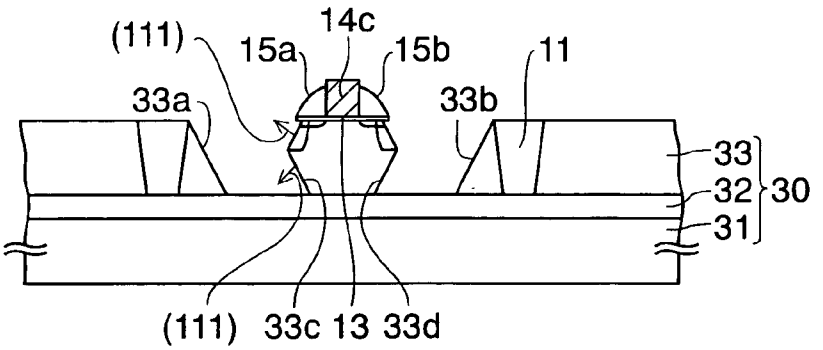

FIG. 11E

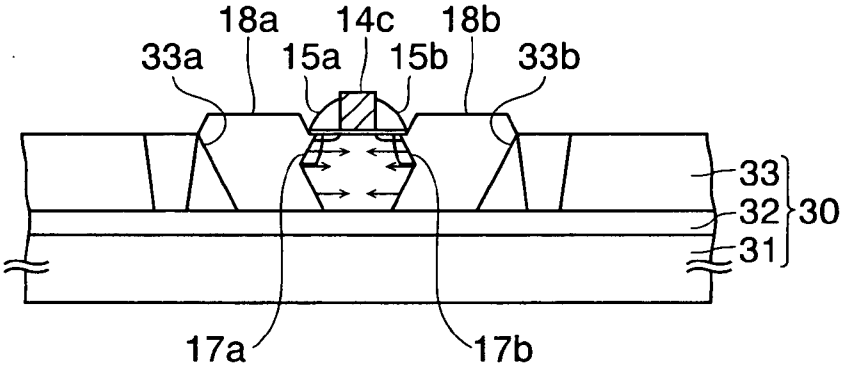

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FIG. 12A

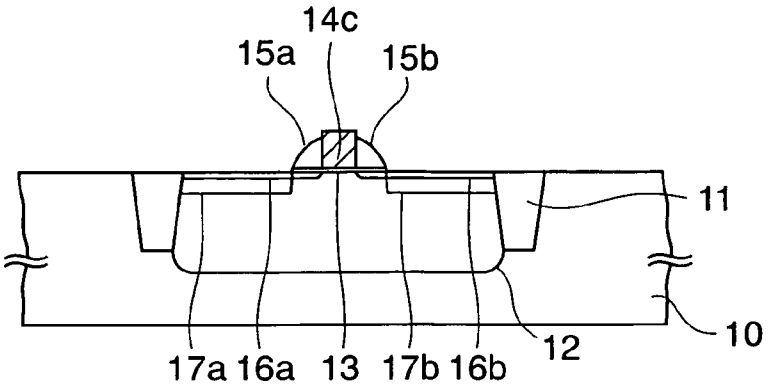

FIG. 12B

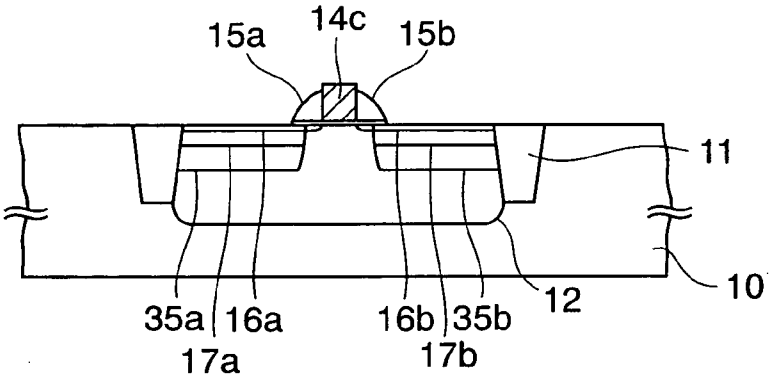

FIG. 12C

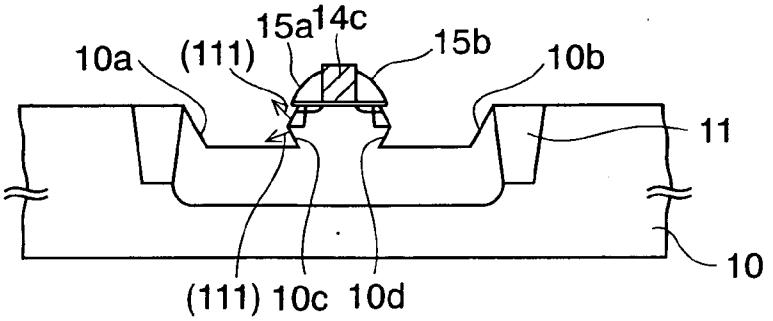

FIG. 12D

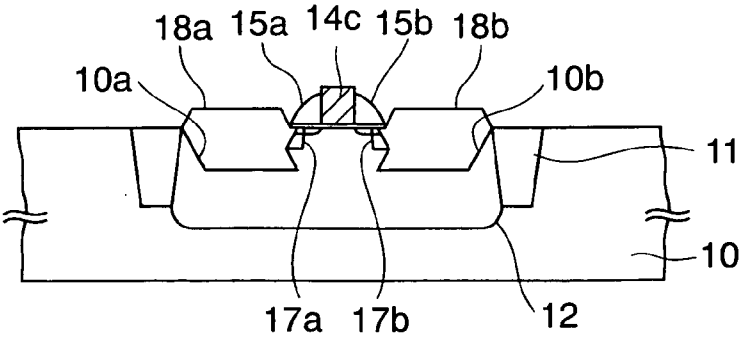

FIG. 13A

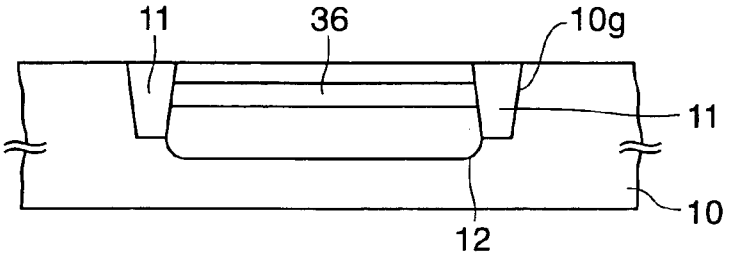

FIG. 13B

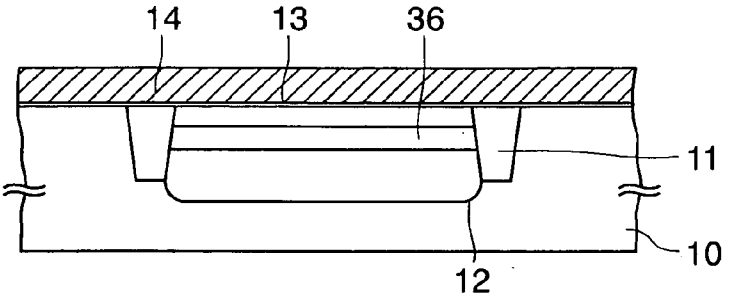

FIG. 13C

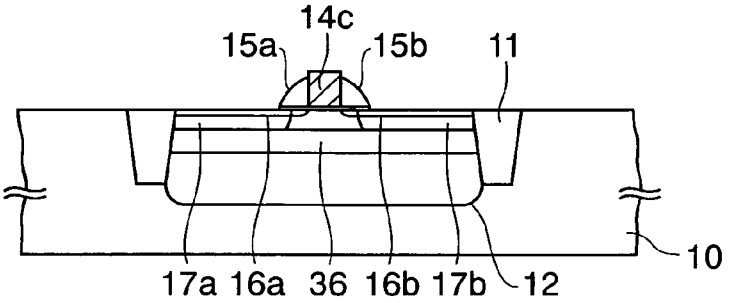

FIG. 13D

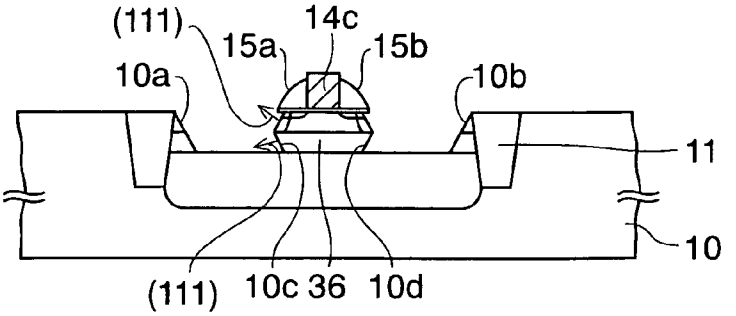

FIG. 13E

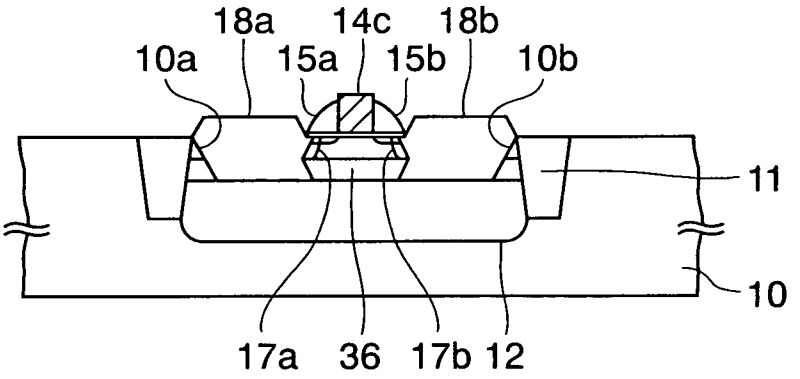

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FIG. 14A

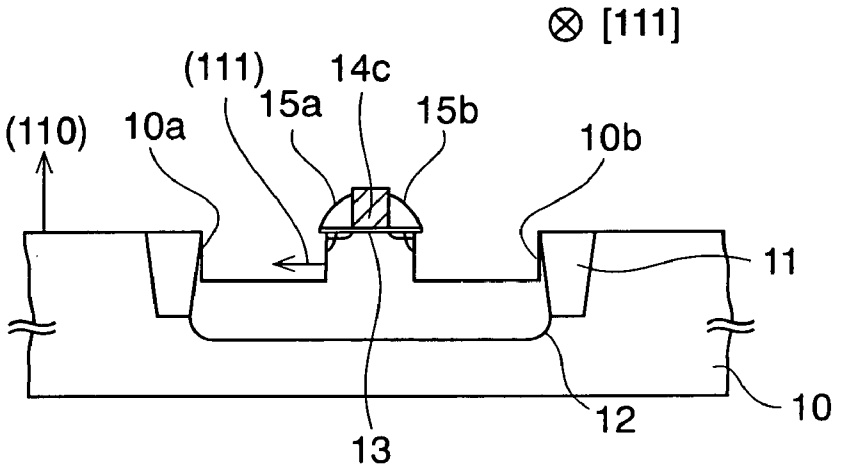

FIG. 14B

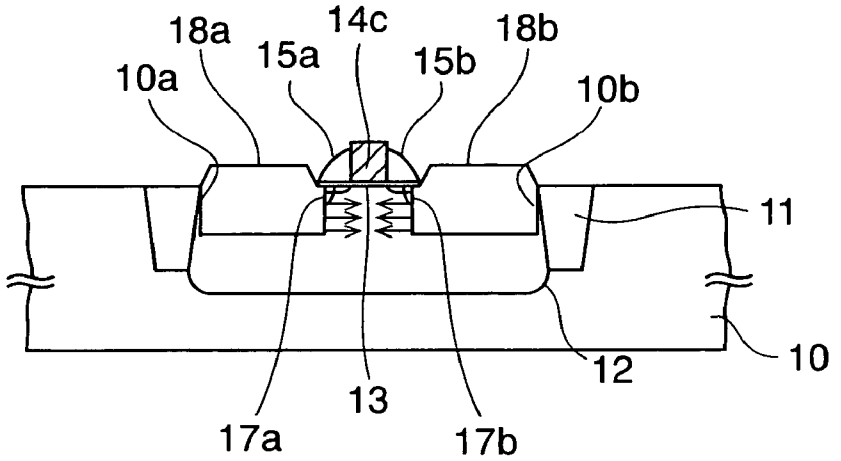

FIG. 15

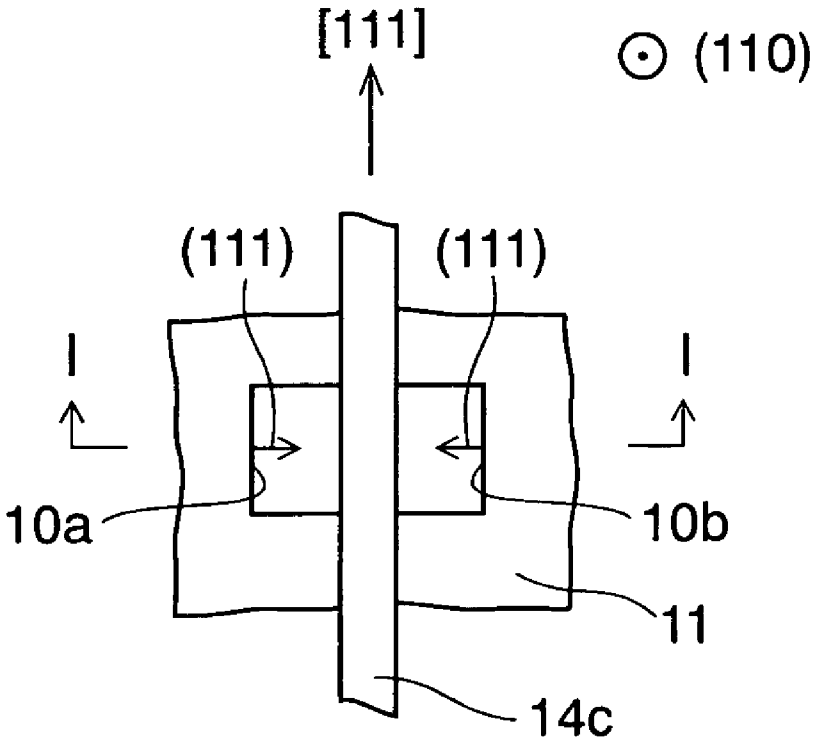

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FIG. 16

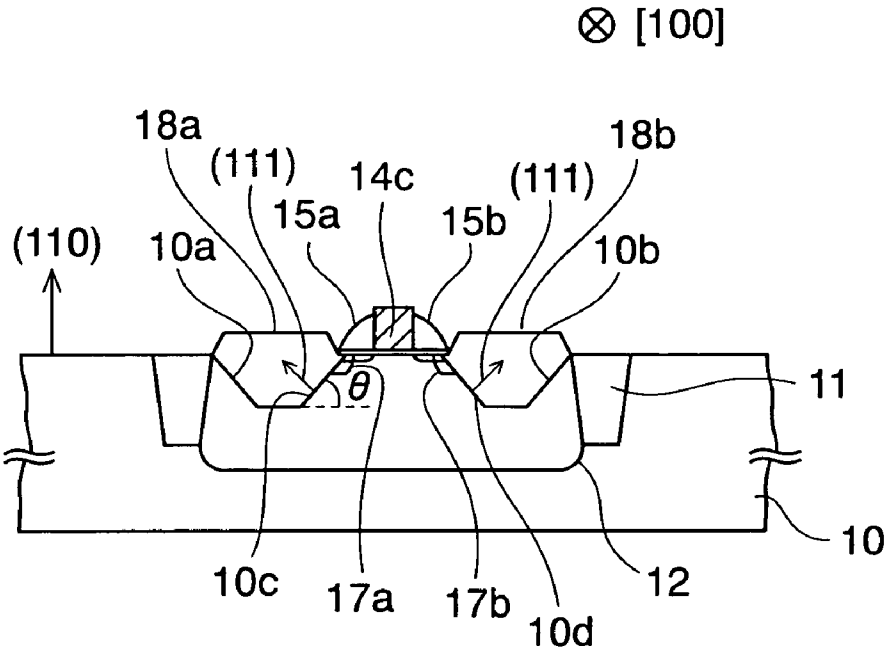
⊗ [100]
18a
(111)
14c
(111)
18b
15a
15b
(110)
10a
10b
θ
11
10
10c
17a
17b
10d
12

FIG. 17

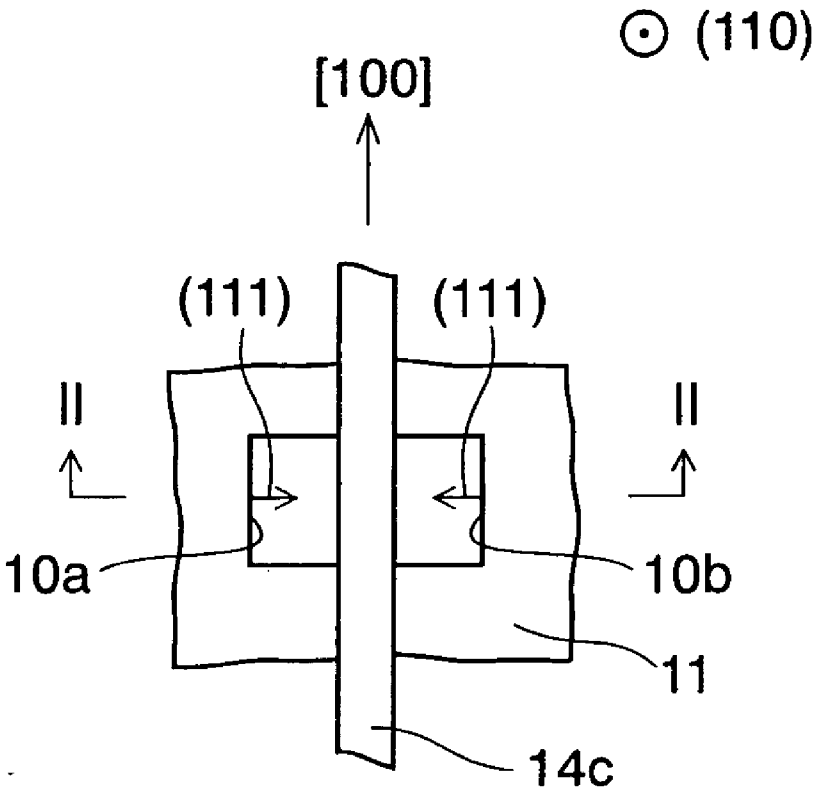

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FIG. 18A

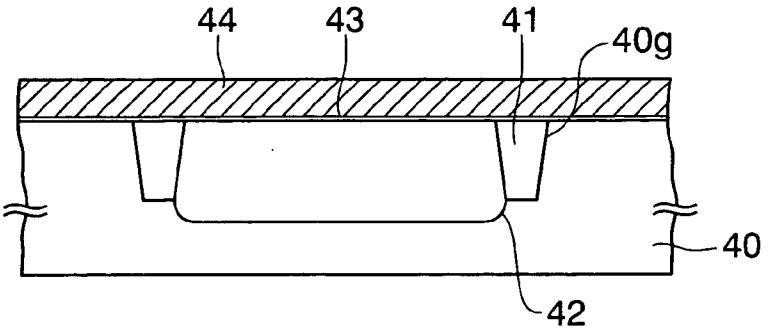

FIG. 18B

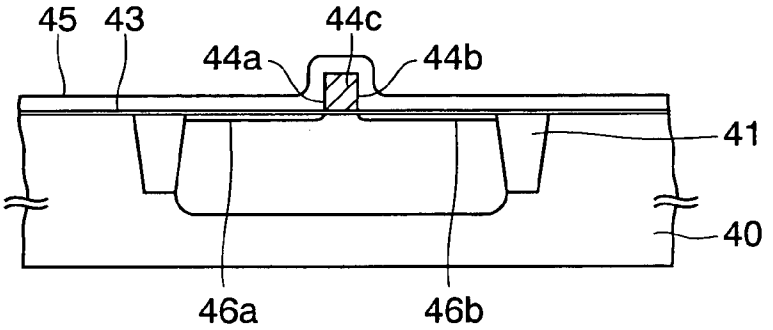

FIG. 18C

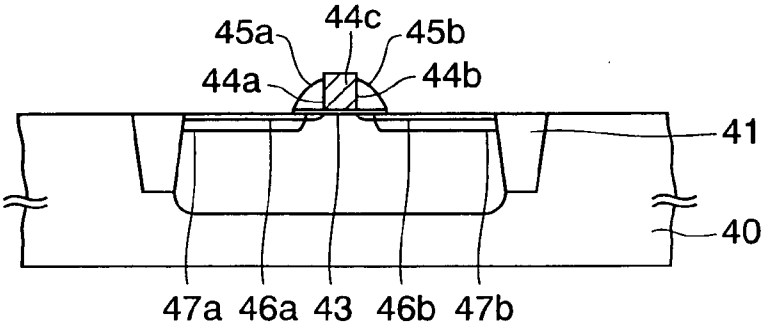

FIG. 18D

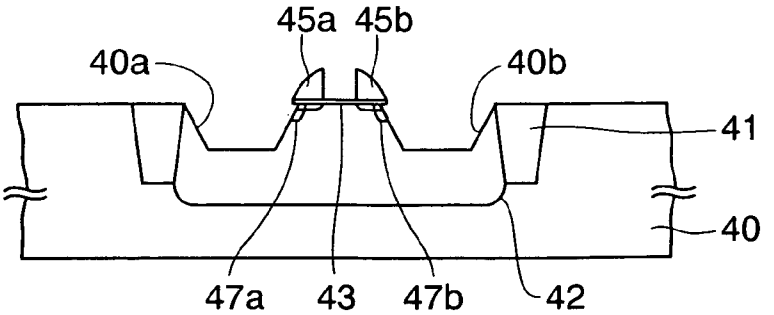

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FIG. 18E

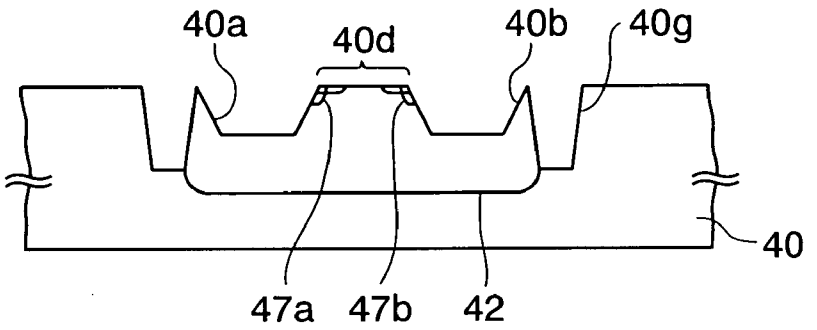

FIG. 19

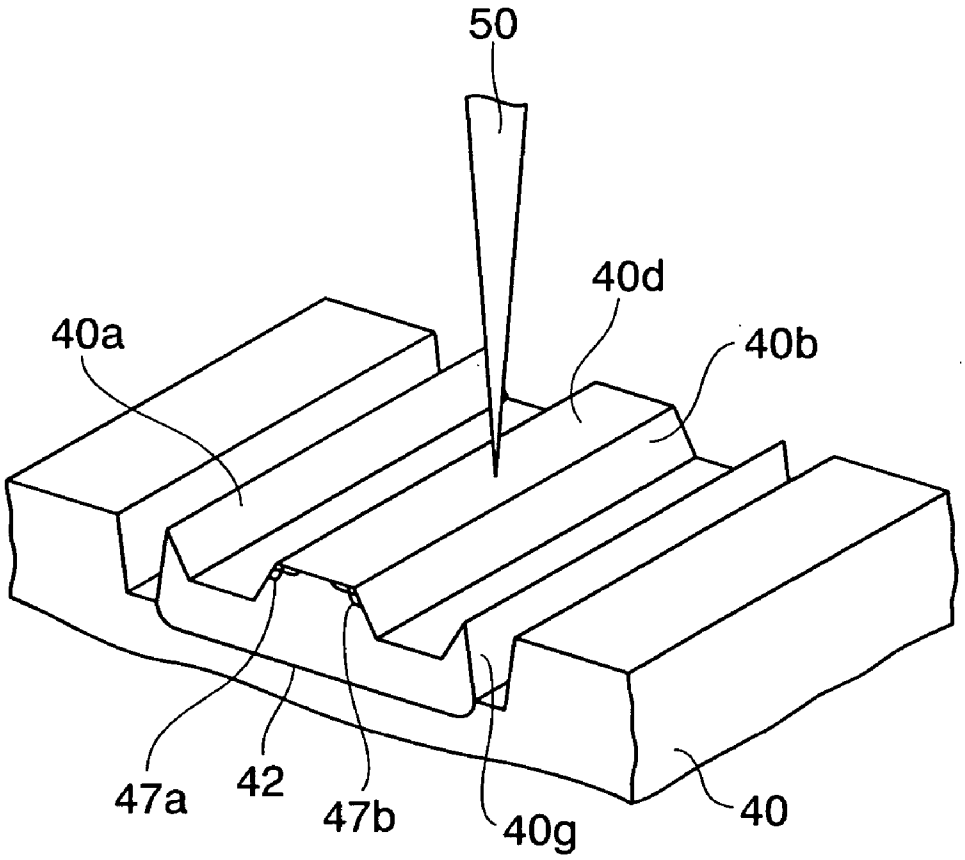

FIG. 20A

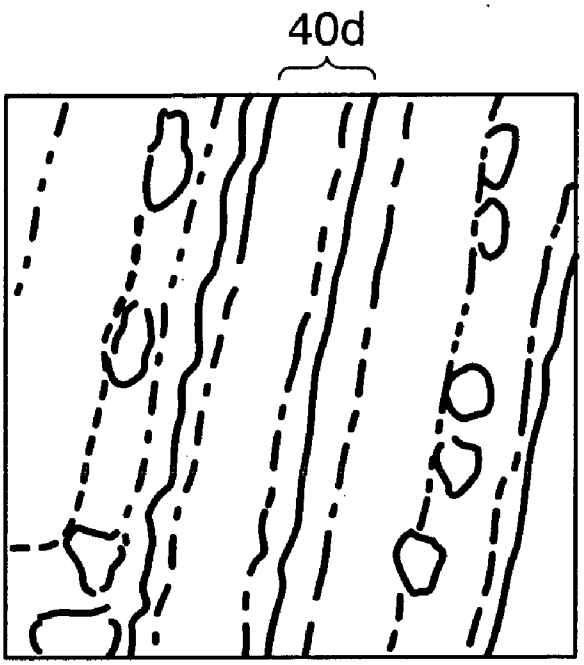

FIG. 20B

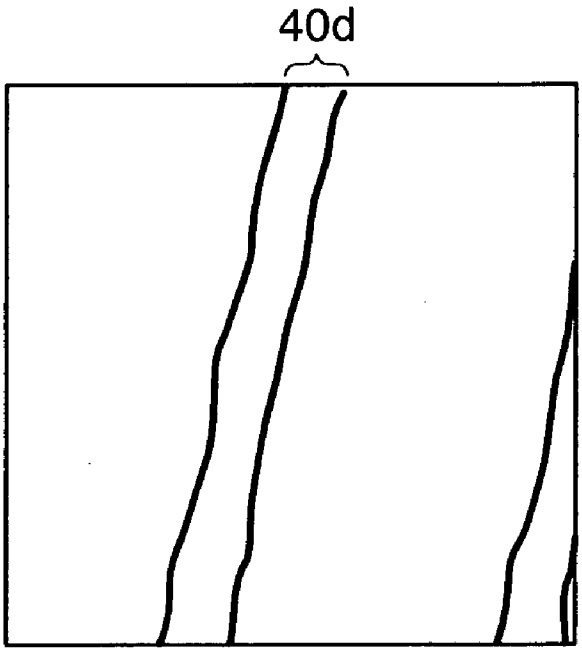

FIG. 21

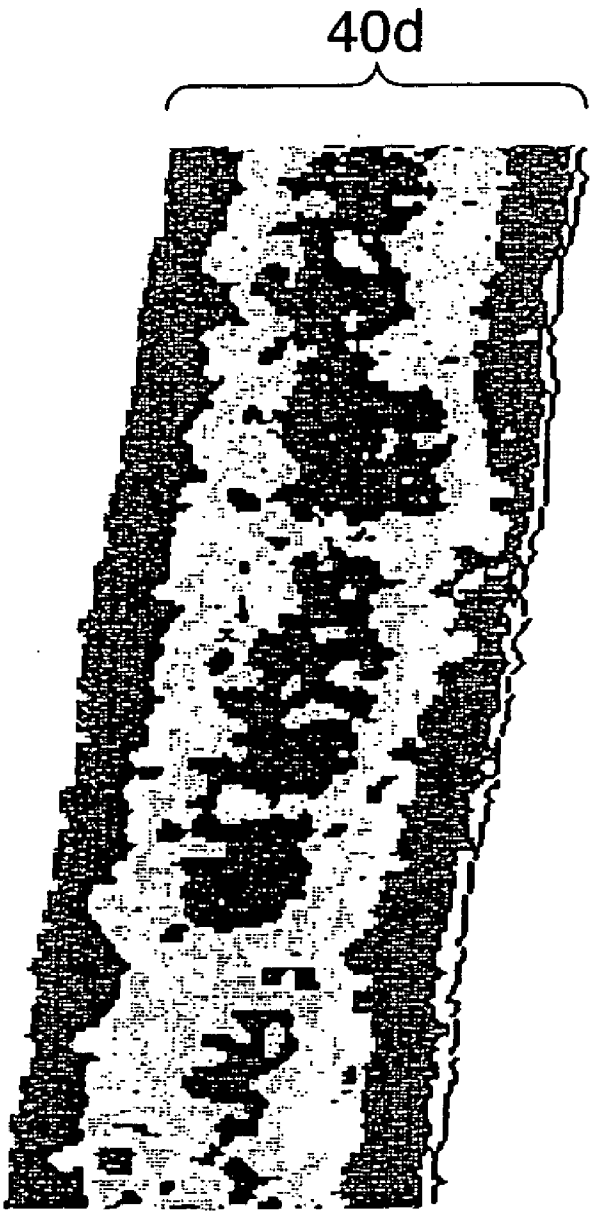

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FIG. 22

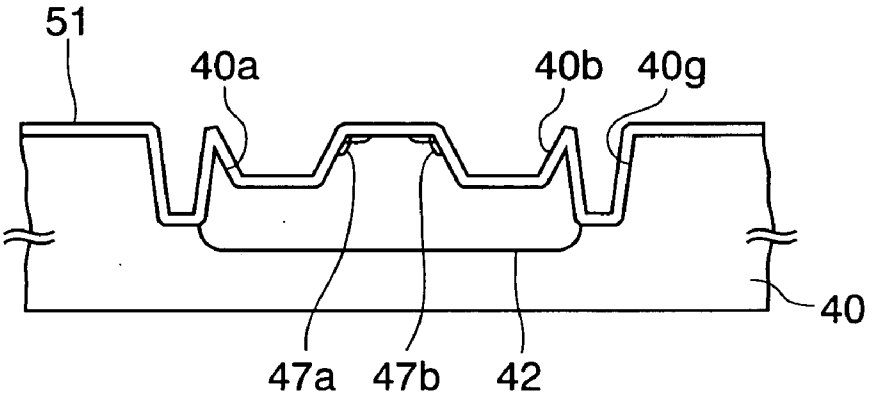
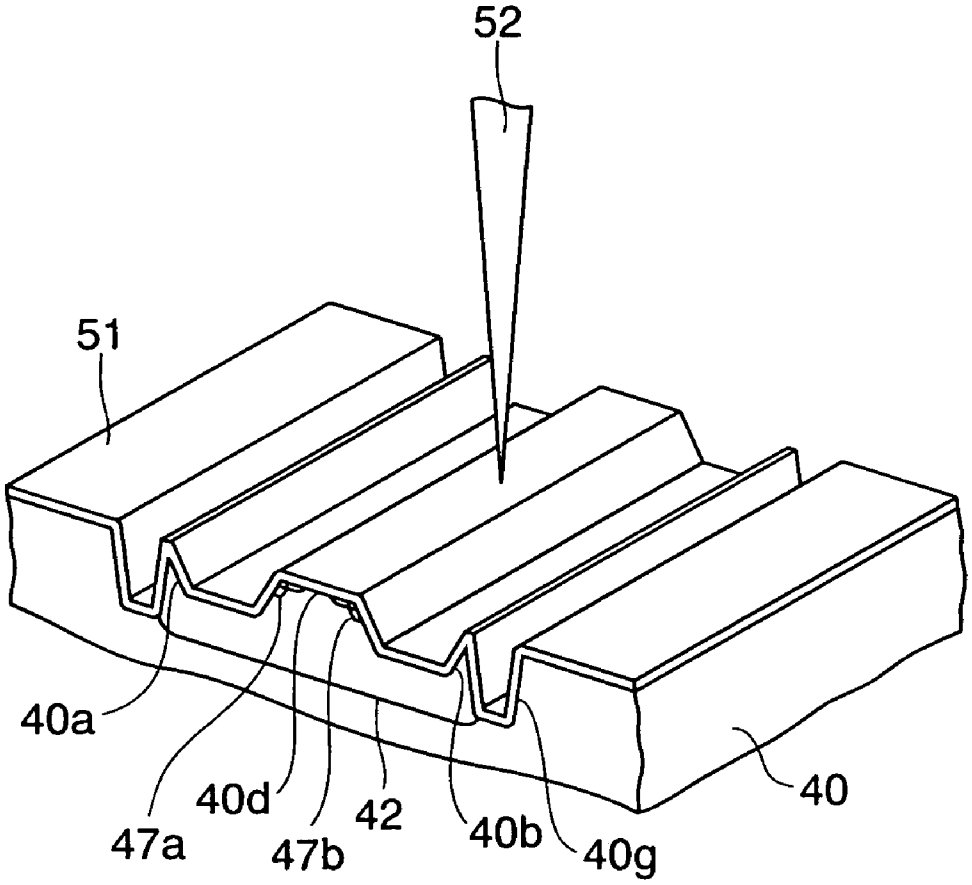


FIG. 23



SEMICONDUCTOR DEVICE, METHOD OF MANUFACTURING THE SAME, AND METHOD OF EVALUATING SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based on and claims priority of Japanese Patent Application No. 2004-187053 filed on Jun. 24, 2004, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a semiconductor device, a method of manufacturing the same, and a method of evaluating a semiconductor device.

[0004] 2. Description of the Related Art

[0005] In recent years, semiconductor devices including LSIs and the like have been miniaturized. However, the improvement of the performance of MOS transistors by miniaturization is approaching a limit. Attempts to improve the performance in a generally used MOS transistor by modifying the structure thereof are being made. As one of such attempts, there is a method in which the mobility of carriers is improved by applying appropriate stress to a channel region of the MOS transistor. There are various ways to apply the stress. In Non-Patent Document 1, recesses are formed in a silicon substrate on both sides of a gate electrode, and SiGe layers to be used as source/drain electrodes are epitaxially grown in the recesses, thus introducing strain into a channel by utilizing a difference in lattice constant between silicon and SiGe. According to Non-Patent Document 1, this structure is said to have the significant effect in that the drive current of a p-type MOS transistor is improved by 10% or more.

[0006] Moreover, in addition to Non-Patent Document 1, technologies related to the present invention are also disclosed in Patent Documents 1 to 4.

[0007] (Patent Document 1) Japanese Unexamined Patent Publication No. Sho 58(1983)-35938

[0008] (Patent Document 2) Japanese Unexamined Patent Publication No. Hei 4(1992)-180633

[0009] (Patent Document 3) Japanese Unexamined Patent Publication No. Hei 7(1995)-50293

[0010] (Patent Document 4) WO98/40909 International Publication Pamphlet

[0011] (Non-Patent Document 1) T. Ghani et al., "A 90 nm High Volume Manufacturing Logic Technology Featuring Novel 45 nm Gate Length Strained Silicon CMOS Transistors," IEDM Tech Dig., pp. 978-980, (2003) Incidentally, in the structure disclosed in Non-Patent Document 1, stress is applied to the channel from the SiGe layers as described previously. If the amount of the stress is nonuniform in the gate width direction or varies among transistors, this transistor cannot be produced in volume to be widely used.

[0012] Moreover, not only in the MOS transistor disclosed in Non-Patent Document 1, but also in a general MOS transistor in which recesses for SiGe layers are not formed in a silicon substrate, when a new device or the like is developed, a test MOS transistor is fabricated, and characteristics thereof are evaluated. Among a number of characteristics, a carrier distribution in a channel greatly influences the performance of a transistor. Accordingly, it is preferable that the carrier distribution is directly measured. However, a method of measuring the carrier distribution has not been established so far.

SUMMARY OF THE INVENTION

[0013] According to an aspect of the present invention, there is provided a semiconductor device including: a semiconductor substrate; a gate insulating film and a gate electrode which are formed on the semiconductor substrate in this order; and a source/drain material layer formed in a hole in the semiconductor substrate, the hole being located beside the gate electrode. Here, a side surface of the hole which is closer to the gate electrode includes at least one crystal plane of the semiconductor substrate.

[0014] In the above-described semiconductor device, the side surface of the hole in which the source/drain material layer is formed is constituted of a crystal plane of the semiconductor substrate. Accordingly, as compared to Patent Document 1 in which a side surface of a hole is constituted of not a crystal plane but a curved surface, stress is stably applied to a channel under the gate electrode, and variation in characteristics of MOS transistors among elements is suppressed.

[0015] Such a side surface of the hole may be constituted of two crystal planes of the semiconductor substrate, and a cross-sectional shape of the side surface may be concave. Such a cross-sectional shape makes characteristics of the interface between the semiconductor substrate and the gate insulating layer less prone to deterioration due to the stress because the stress has a peak at a position deeper than the surface of the semiconductor substrate, and can also make the reliability of the MOS transistor favorable while improving the drive capability thereof.

[0016] Alternatively, the following may be adopted: the side surface of the hole is constituted of two crystal planes of the semiconductor substrate, and a cross-sectional shape of the side surface is made convex. In the source/drain material layer formed in the hole having such a cross-sectional shape, large stress is generated in directions from the upper and lower surfaces of the source/drain material layer toward the channel, whereas stress becomes weak in the vicinity of the top of the convex. Thus, stress favorable for the improvement in the performance of a MOS transistor can be obtained.

[0017] Furthermore, instead of such a concave or convex side surface, the side surface of the hole may be constituted of a single crystal plane perpendicular to the semiconductor substrate. This allows uniform stress having a small strength variation in the depth direction to be stably applied to the channel from the source/drain material layer in the hole.

[0018] Moreover, according to another aspect of the present invention, there is provided a method of manufacturing a semiconductor device, which includes the steps of: forming a gate insulating film on a semiconductor substrate; forming a gate electrode on the gate insulating film; forming a sidewall on a side surface of the gate electrode; forming a

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hole in the semiconductor substrate beside the gate electrode using an organic alkaline solution or a tetramethylammonium hydroxide (TMAH) solution as an etchant, after forming the sidewall; and forming a source/drain material layer in the hole.

[0019] In this method of manufacturing a semiconductor device, since the hole is formed in the semiconductor substrate using an organic alkaline solution or a TMAH solution, a crystal plane of the semiconductor substrate appears at the etched surface, and a side surface of the hole is constituted of the crystal plane. Accordingly, the excellent reproducibility of the shape of the hole comes to be shown as compared to the case where the side surface of the hole is constituted of a curved surface as in Patent Document 1. Even in the case where MOS transistors are integrally formed in the semiconductor substrate, stress is applied to the channel from the source/drain material layer formed in the hole, without variation among elements.

[0020] Further, when the hole is formed, the thickness of the gate electrode may be reduced by etching. In that case, a refractory metal layer is formed on the thinned gate electrode, and the refractory metal layer is heated to undergo reaction with the gate electrode, whereby the entire gate electrode is silicided. Such a gate electrode is called a metal gate. The above-described technique allows compatibility between a formation process of the metal gate and that of the hole.

[0021] Note that, in the case where the gate electrode does not need to be etched as described above, p-type impurities having the effect of delaying etching in a TMAH solution or an organic alkaline solution can be introduced into the gate electrode in advance.

[0022] Furthermore, the following may be adopted: a first conductivity type impurity diffusion region and a second conductivity type impurity diffusion region which is deeper than the first conductivity type impurity diffusion region are formed in the silicon substrate, and the hole is formed more deeply than the first conductivity type impurity diffusion region. This causes the etch rate for forming the hole to vary between the first and second conductivity type impurity diffusion regions due to differences in impurity concentration and conductivity type between the impurity diffusion regions. Accordingly, a plurality of crystal planes appear at the side surface of the hole.

[0023] For example, in the case where the first conductivity type impurity diffusion region is set to the p-type and the second conductivity type impurity diffusion region is set to the n-type, the side surface of the hole is constituted of two crystal planes, and the cross-sectional shape of the side surface becomes a concave shape which bends at the interface between these two crystal planes as a boundary.

[0024] On the other hand, in the case where the first conductivity type impurity diffusion region is set to the p-type and p-type impurities are introduced into the second conductivity type impurity diffusion region at a higher concentration than in the first conductivity type impurity diffusion region, the side surface of the hole is constituted of two crystal planes, and the cross-sectional shape of the side surface becomes a convex shape which bends at the interface between these two crystal planes as a boundary.

[0025] Furthermore, an SOI substrate may be used as the semiconductor substrate. In the case where an SOI substrate is used, when the hole is formed by etching in a TMAH solution or an organic alkaline solution, the etch rate becomes low in the vicinity of a buried insulating film partially constituting the SOI substrate, and the etch rate varies depending on the depth in the substrate. Thus, a plurality of crystal planes appear at the side surface of the hole in etching, and these crystal planes constitute the side surface of the hole.

[0026] Moreover, in the case where a silicon substrate is used as the semiconductor substrate, the surface orientation of the silicon substrate is set to (110), and the gate width direction is set to the [111] direction, whereby the side surface of the hole is constituted of a (111) plane perpendicular to the surface of the silicon substrate.

[0027] On the other hand, in the case where the surface orientation of the silicon substrate is set to (110) similarly to the above and the gate width direction is set to [100], the tilt of a (111) plane which is viewed from the surface of the silicon substrate becomes gentle, and the gentle (111) plane constitutes the side surface of the hole.

[0028] Furthermore, according to another aspect of the present invention, there is provided a method of evaluating a semiconductor device, which includes the steps of: removing a gate electrode of a MOS transistor, which is formed in a semiconductor substrate, by selective etching using an organic alkaline solution or a TMAH solution as an etchant; exposing a channel of the MOS transistor by removing a gate insulating film of the MOS transistor by wet etching; and investigating a carrier distribution in the exposed channel using a microscope.

[0029] An organic alkaline solution and a TMAH solution provide high etch selectivity between semiconductor, such as silicon, and oxide, such as silicon dioxide. Accordingly, when the gate electrode of the MOS transistor is selectively etched, the thickness of the gate insulating film under the gate electrode is scarcely reduced. As a result, in the above-described method of evaluating a semiconductor device, damage does not easily occur in the channel under the gate insulating film, and the carrier distribution in the channel is not easily disturbed. Accordingly, a carrier distribution in a state similar to that of actual use can be obtained.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] **FIG. 1** contains cross-sectional views of samples used for investigating the etch selectivity between silicon and silicon dioxide in a TMAH solution in a first embodiment of the present invention;

[0031] **FIG. 2** is a graph obtained by investigating the etch rates of silicon and silicon dioxide in the TMAH solution in the first embodiment of the present invention;

[0032] **FIG. 3** is a graph obtained by investigating the etch rates of silicon and silicon dioxide in an organic alkaline solution in the first embodiment of the present invention;

[0033] **FIG. 4** is a graph obtained by investigating the dependence of the etch rate in the TMAH solution on the concentration of impurities in the first embodiment of the present invention;

[0034] **FIGS. 5A** to **5G** are cross-sectional views showing a method of manufacturing a semiconductor device according to a second embodiment of the present invention, in the process of manufacture;

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[0035] **FIG. 6** is a view drawn based on an SEM image of recesses after the recesses have been formed according to the second embodiment of the present invention;

[0036] **FIG. 7** is a view drawn based on an SEM image in the case where the distance d, by which each recess goes under a sidewall, is increased by adjusting the substrate temperature when the first sidewall insulating layer is formed in the second embodiment of the present invention;

[0037] **FIGS. 8A** to **8**C are cross-sectional views of a semiconductor device according to a third embodiment of the present invention in the process of manufacture;

[0038] **FIGS. 9A** to **9**D are cross-sectional views of a semiconductor device according to a fourth embodiment of the present invention in the process of manufacture;

[0039] **FIG. 10** is a view drawn based on an SEM image of recesses after the recesses have been formed according to the fourth embodiment of the present invention;

[0040] **FIGS. 11A** to **11**E are cross-sectional views of a semiconductor device according to a fifth embodiment of the present invention in the process of manufacture;

[0041] **FIGS. 12A** to **12**D are cross-sectional views of a semiconductor device according to a sixth embodiment of the present invention in the process of manufacture;

[0042] **FIGS. 13A** to **13**E are cross-sectional views of a semiconductor device according to a seventh embodiment of the present invention in the process of manufacture;

[0043] **FIGS. 14A and 14B** are cross-sectional views of a semiconductor device according to an eighth embodiment of the present invention in the process of manufacture;

[0044] **FIG. 15** is a plan view of the semiconductor device according to the eighth embodiment of the present invention in the process of manufacture;

[0045] **FIG. 16** is a cross-sectional view of a semiconductor device according to a ninth embodiment of the present invention in the process of manufacture;

[0046] **FIG. 17** is a plan view of the semiconductor device according to the ninth embodiment of the present invention in the process of manufacture;

[0047] **FIGS. 18A** to **18**E are cross-sectional views of a TEG to be used in a method of evaluating a semiconductor device according to a tenth embodiment of the present invention in the process of manufacture;

[0048] **FIG. 19** is a perspective view for explaining the method of evaluating the semiconductor device according to the tenth embodiment of the present invention;

[0049] **FIGS. 20A and 20B** are views drawn based on a relief image obtained by actually measuring the TEG used in the tenth embodiment of the present invention, using a scanning tunneling microscope;

[0050] **FIG. 21** is a view obtained by actually measuring the carrier distribution in the TEG used in the tenth embodiment of the present invention;

[0051] **FIG. 22** is a cross-sectional view of a TEG used in a method of evaluating a semiconductor device according to an eleventh embodiment of the present invention; and

[0052] **FIG. 23** is a perspective view for explaining the method of evaluating the semiconductor device according to the eleventh embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0053] Hereinafter, best modes for carrying out the present invention will be described in detail with reference to the accompanying drawings.

(1) First Embodiment

[0054] Recesses of a silicon substrate for growing SiGe layers can be formed by generally-used wet etching in which KOH or a mixture of hydrofluoric acid and nitric acid is used as an etchant. However, use of these etchants makes it difficult to control the shapes of the recesses because the side surface of each recess becomes a gently curved surface as shown in FIG. 1 of Patent Document 1. Accordingly, there is variation in the shapes of the side surfaces of the recesses among elements, and characteristics of MOS transistors may therefore vary among the elements.

[0055] Moreover, if dry etching is used instead of the above-described wet etching, the surfaces of the recesses are damaged by plasma. Accordingly, lattice defects may be created in the SiGe layers epitaxially grown on the recesses.

[0056] In light of these points, the inventor of the present application has searched for an etchant replacing KOH and a mixture of hydrofluoric acid and nitric acid to find out that a tetramethylammonium hydroxide (TMAH) solution can be used as a suitable etchant for forming the recesses. Furthermore, it has been found out that an organic alkaline solution made by mixing an alkaline solution, alcohol, and water is also suitable as the above-described etchant.

[0057] Accordingly, hereinafter, experiments which the inventor of the present application performed in order to investigate etching characteristics of the TMAH and the organic alkaline solution will be described.

[0058] (a) Etch Selectivity

[0059] **FIG. 1** contains cross-sectional views of samples used for investigating the etch selectivity between silicon and silicon dioxide in a TMAH solution. Of these samples, sample **S1** was prepared as described below.

[0060] First, a silicon dioxide layer **2** was formed on a silicon substrate **1** by plasma chemical vapor deposition (CVD) using silane (SiH_4), and then a polysilicon layer **3** having a thickness of 100 nm was formed by low-pressure CVD (LPCVD) using silane as reactant gas. Subsequently, the surface of the polysilicon layer **3** was exposed to nitric acid to be oxidized, thereby forming an oxide film **4** having a thickness of approximately 1.0 nm.

[0061] On the other hand, sample **S2** was made by forming a polysilicon layer **3** in the same way as that for sample **S1** and then terminating the surface of the polysilicon layer **3** with hydrogen by exposure to hydrofluoric acid. A layer corresponding to the oxide film **4** of sample **S1** was not formed.

[0062] Thereafter, a TMAH solution with a volume concentration of 5 to 30% was prepared by dissolving TMAH in pure water, and the above-described samples **S1** and **S2**

were wet-etched using this TMAH solution. Then, after this etching was performed for a predetermined time, the film thickness of the native oxide film **4** of sample **S1** and that of the polysilicon layer **3** of sample **S2** were measured using a film thickness gauge, and the results of the measurements are compared with the initial film thicknesses of these films, whereby etched amounts were estimated. The results are shown in **FIG. 2**.

[**0063**] The horizontal axis of **FIG. 2** represents etching time in the TMAH solution, and the vertical axis thereof represents the thickness of the polysilicon layer **3** after etching.

[**0064**] As apparent from **FIG. 2**, etching does not proceed at all in sample **S1** in which the native oxide film **4** is formed, whereas, in sample **S2** in which the polysilicon layer **3** is exposed, the polysilicon layer **3** is etched as the etching time proceeds.

[**0065**] The above-described results have revealed that the etch rate of silicon dioxide in the TMAH solution can be regarded as 0 nm/min and that, on the other hand, the etch rate of silicon is a finite value. Moreover, the result of other experiment performed by the inventor of the present application has also revealed that the etch rate of silicon in the TMAH solution depends on the temperature of the TMAH solution.

[**0066**] **FIG. 3** is a graph obtained by performing the same experiment as the above using an organic alkaline solution instead of the TMAH solution. The organic alkaline solution was prepared as follows: an ammonium hydroxide solution with a concentration of 20 wt % or more was prepared by putting ammonium hydroxide in pure water, and then isopropyl alcohol (IPA) was dissolved in this ammonium hydroxide solution with a concentration of 2 wt % or more.

[**0067**] As shown in **FIG. 3**, it has been revealed that the organic alkaline solution also selectively etches silicon but does not etch silicon dioxide.

[**0068**] Incidentally, an organic alkaline solution is not limited to the above-described one. A mixed solution of an alkaline solution other than an ammonium hydroxide solution and heavy alcohol, such as IPA or the like, may be used as the organic alkaline solution.

[**0069**] (b) Dependence of Etch Rate in TMAH Solution on Impurity Concentration

[**0070**] In the above-described experiments of **FIGS. 2 and 3**, impurities were not introduced into the polysilicon layer **3**. However, it is speculated that the etch rate of the polysilicon layer **3** depends on the concentration of impurities. In order to confirm this point, the inventor of the present application performed the experiment described below.

[**0071**] In this experiment, three samples having the same structure as that of the aforementioned sample **S2** were prepared. Then, arsenic ions as n-type impurities and boron ions as p-type impurities are implanted into the polysilicon layers **3** of two of these samples, respectively. The doping amount in the ion implantation was set to 1.0×10^{17} cm^{-3} to 2.0×10^{21} cm^{-3}. Meanwhile, the polysilicon layer **3** of the other sample was left undoped, that is, impurities were not introduced into the polysilicon layer **3** of the other sample.

[**0072**] Thereafter, the polysilicon layers **3** of these samples were exposed to the TMAH solution for a predetermined time, and the etched amounts of the polysilicon layers **3** were investigated. The results are shown in **FIG. 4**.

[**0073**] As shown in **FIG. 4**, it has been revealed that, in the case where the n-type impurities (arsenic) have been introduced, the etch rate of the polysilicon layer **3** becomes faster compared to the undoped case. On the other hand, it has been revealed that, in the case where the p-type impurities (boron) are introduced, the etch rate of the polysilicon layer **3** becomes slower compared to the undoped case. Furthermore, other experiment performed by the inventor of the present application has also revealed that, in the case where the doping amount of boron is set to ten times that shown in **FIG. 4**, the etching of the polysilicon layer **3** hardly proceeds.

(2) Second Embodiment

[**0074**] Next, a method of fabricating a MOS transistor will be described. In this method, recesses are formed in a silicon substrate by utilizing etching characteristics of a TMAH solution or an organic alkaline solution. The etching characteristics have been revealed in the first embodiment, and SiGe layers in the recesses are used as source/drain electrodes.

[**0075**] **FIGS. 5A** to **5G** are cross-sectional views of a semiconductor device according to the present embodiment in the process of manufacture.

[**0076**] To begin with, steps to be performed before the cross-sectional structure shown in **FIG. 5A** is obtained will be described.

[**0077**] First, an element isolation trench log for shallow trench isolation (STI) is formed in a p-type silicon (semiconductor) substrate **10** with (001) surface orientation, and then a silicon dioxide layer is buried as an element isolation insulating film **11** in the element isolation trench log. Thereafter, ion implantation is performed on the silicon substrate **10** under the following conditions: for example, in the case where phosphorus is used as n-type impurities, the acceleration energy is approximately 300 keV or more, and the dose is 1×10^{13} cm^{-2} or more. Thus, an n-well **12** is formed in a p-type MOS transistor formation region delimited by the element isolation insulating film **11**.

[**0078**] Incidentally, in the case where a CMOS structure is formed by fabricating an n-type MOS transistor in addition to the p-type MOS transistor, a p-well (not shown) is formed by implanting, for example, boron ions as p-type impurities into an n-type MOS transistor formation region of the silicon substrate **10** under the following conditions: the acceleration energy is 100 keV or more, and the dose is 1×10^{13} cm^{-2} or more. In this case, the p-type and n-type impurities are respectively implanted using resist patterns (not shown) on the silicon substrate **10**, and each resist pattern is removed in a wet process after ion implantation.

[**0079**] Subsequently, the surface of the silicon substrate **10** is thermally oxidized, thus forming a gate insulating film **13** which is made of silicon dioxide and which has a thickness of approximately 0.5 to 5.0 nm. Here, a gate insulating film in which a very small amount of nitrogen is added to silicon dioxide may be adopted as the gate insulating film **13**. Further, a polysilicon layer **14** having a

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thickness of approximately 10 to 300 nm is formed on the gate insulating film **13** by LPCVD using silane, and then ions of p-type impurities are implanted into the polysilicon layer **14** at a concentration at which the etching of polysilicon in a TMAH solution does not proceed. In the present embodiment, boron is adopted as such p-type impurities, and ion implantation is performed on the polysilicon layer **14** under conditions optimized so that a sufficiently high concentration can be achieved in the entire gate electrode. The conditions are an acceleration energy of approximately 0.5 to 20 keV and a dose of approximately 1×10^{14} to 1×10^{17} cm^{-2}.

[**0080**] Next, steps to be performed before the cross-sectional structure shown in **FIG. 5B** is obtained will be described.

[**0081**] First, the polysilicon layer **14** is patterned into a gate electrode **14***c* by photolithography.

[**0082**] In this example, though description will be made based on a process in which extensions and pockets are formed after gate processing without forming thin spacers, a method can also be adopted in which extension and pocket implantation is performed after thin spacers having thicknesses of 5 to 20 nm have been formed in order to form optimum overlaps between the gate and the extensions. Further, a method can also be adopted in which spacers are formed only for one of the nMOS and the PMOS. Any spacer can be adopted as long as the spacer has the function as a spacer, regardless of the film structure and shape of the spacer.

[**0083**] Subsequently, using the gate electrode **14***c* as a mask, for example, boron ions as p-type impurities are implanted into the silicon substrate **10** under the following conditions: the acceleration energy is approximately 0.2 to 1.0 keV, the dose is approximately 1×10^{14} to 2×10^{15} cm^{-2}, and the tilt angle is 0 to 15 degrees. Thus, first and second source/drain extensions **16***a* and **16***b* are shallowly formed in the silicon substrate **10** beside the first and second side surfaces **14***a* and **14***b* of the gate electrode **14***c*. In the same positions, pocket implantation for suppressing the short channel effect is performed under the following conditions: for example, antimony is used, the acceleration energy is 30 to 80 keV, the dose is 1×10^{13} to 2×10^{14} cm^{-2}, and the tilt angle is 0 to 35 degrees. In the case where BF2 is used as ionic species for the source/drain extension implantation, optimum conditions are provided by setting the energy to 1 to 2.5 keV and doubling the dose. The above-described optimum conditions change with the presence or absence of spacers and the thicknesses thereof. In the case where there are spacers, it is necessary to achieve optimum conditions by setting the energy for the pockets higher and setting the dose for the extensions larger. Further, pocket implantation using arsenic, phosphorus, antimony, or the like can also be adopted, and this pocket implantation may be performed before and after the extension implantation.

[**0084**] Thereafter, a silicon dioxide layer is formed as a first sidewall insulating layer **15** on the entire surface by plasma CVD using silane under conditions where the substrate temperature is approximately 600° C. or less, thus covering the first and second side surfaces **14***a* and **14***b* of the gate electrode **14***c* with the first sidewall insulating layer **15**. Note that, instead of the silicon dioxide layer, a silicon nitride layer may be formed as the first sidewall insulating layer **15**.

[**0085**] Next, steps to be performed before the cross-sectional structure shown in **FIG. 5C** is obtained will be described.

[**0086**] First, the first sidewall insulating layer **15** is etched back by plasma etching to leave first sidewalls **15***a* and **15***b* on the first and second side surfaces **14***a* and **14***b*. Further, in this etching, the portion of the gate insulating film **13** which is not covered with the first sidewalls **15***a* and **15***b* is also etched, whereby the gate insulating film **13** is left only under the gate electrode **14***c*.

[**0087**] Furthermore, using the gate electrode **14***c* and the first sidewalls **15***a* and **15***b* as a mask, for example, boron ions are implanted as p-type impurities (impurities of a first conductivity type) into the silicon substrate **10**. Thus, source/drain regions **17***a* and **17***b* which are deeper and denser than the source/drain extensions **16***a* and **16***b* are formed in the silicon substrate **10** beside the gate electrode **14***c*.

[**0088**] Thereafter, the impurities in the source/drain regions **17***a* and **17***b* are activated by performing activation anneal under the following conditions: for example, the substrate temperature is approximately 950 to 1050° C. This heat treatment may be omitted as needed.

[**0089**] Next, steps to be performed before the cross-sectional structure shown in **FIG. 5D** is obtained will be described.

[**0090**] First, the silicon substrate **10** is immersed in a TMAH solution having a volume concentration of 5 to 30% and a temperature of 0 to 50° C., thereby starting the etching of the silicon substrate **10**. At this time, as in the experimental results shown in **FIG. 2**, the TMAH solution selectively etches only silicon but does not etch silicon dioxide. Accordingly, in this etching, the first sidewalls **15***a* and **15***b* and the element isolation insulating film **11** function as an etching mask, and the portion of the silicon substrate **10** which is not covered with this etching mask comes to be selectively etched.

[**0091**] Moreover, as in the experimental results shown in **FIG. 4**, the etch rate of silicon doped with p-type impurities in the TMAH solution is slow. Accordingly, the gate electrode **14***c* into which boron ions are implanted at a high concentration in the step of **FIG. 5A** is hardly etched by this TMAH solution.

[**0092**] In addition, in etching using the TMAH solution, (111) planes of the silicon substrate **10** are neatly exposed to the outside, instead of curved surfaces as in Non-Patent Document 1. Accordingly, first and second recesses (holes) **10***a* and **10***b* having these (111) planes as first and second side surfaces **10***c* and **10***d* are formed.

[**0093**] The depths of the first and second recesses **10***a* and **10***b* are controlled by etching time, and set to an optimum value in a range of approximately 20 to 70 nm in the present embodiment.

[**0094**] Moreover, since the above-described etching also proceeds in the horizontal direction, the upper end portions **10***e* and **10***f* of the recesses **10***a* and **10***b*, which are closer to the gate electrode **14***c*, go under the first sidewalls **15***a* and **15***b* by a distance d. As described previously, the etch rate of the silicon substrate **10** in a TMAH solution depends on the concentration of impurities in silicon. Accordingly, the

above-described distance d can be controlled by adjusting the concentrations of impurities in the source/drain extensions **16***a* and **16***b* and the source/drain regions **17***a* and **17***b*.

[**0095**] Moreover, as shown in the experimental results of **FIG. 2**, silicon dioxide is hardly etched by a TMAH solution. Accordingly, when the recesses **10***a* and **10***b* are being formed by etching in a TMAH solution, the etch rate of the silicon substrate **10** decreases near the sidewalls **15***a* and **15***b* made of silicon dioxide. Consequently, the rate at which the upper end portions **10***e* and **10***f* go under the sidewalls **15***a* and **15***b* due to etching is slow compared to other portions, and the above-described entry length d can be easily controlled. Furthermore, the entry length d is also determined by the substrate temperature when the first sidewall insulating layer **15** is formed, and therefore can also be controlled by the relevant substrate temperature. This also applies to each embodiment to be described later.

[**0096**] Note that use of an organic alkaline solution instead of a TMAH solution also makes it possible to expose neat (111) planes at the first and second side surfaces **10***c* and **10***d* and to control the entry length d of each recess **10***a* and **10***b*.

[**0097**] Next, steps to be performed before the cross-sectional structure shown in **FIG. 5E** is obtained will be described.

[**0098**] First, the silicon substrate **10** is put into a chamber (not shown) for epitaxial growth, and the substrate temperature is stabilized. Then, a SiGe layer with a Ge concentration of 3 to 30% is selectively epitaxially grown in each of the recesses **10***a* and **10***b* by supplying a silane-based gas or the like to the inside of the chamber. The SiGe layers selectively grow only on silicon but do not grow on the element isolation insulating film **11** and the first sidewalls **15***a* and **15***b*, which are made of silicon dioxide.

[**0099**] Thereafter, when the thicknesses of the SiGe layers, which are measured from the bottom surfaces of the respective recesses **10***a* and **10***b*, reach an optimum value of approximately 20 to 120 nm, the epitaxial growth is stopped, and the obtained SiGe layers are used as first and second source/drain material layers **18***a* and **18***b*.

[**0100**] The thicknesses of the source/drain material layers **18***a* and **18***b* are not limited to the above. However, the distances between the bottom surface of the n-well **12** and the upper surfaces of the source/drain material layers **18***a* and **18***b* are increased by forming the upper surfaces of the source/drain material layers **18***a* and **18***b* at positions higher than the surface of the silicon substrate **10** as in the present embodiment. This increases the distances between the p-n junction at the bottom surface of the n-well **12** and conductive plugs to be formed on the source/drain material layers **18***a* and **18***b* later. Thus, a junction leakage in the above-described p-n junction can be suppressed, and the reliability of the transistor can be improved.

[**0101**] Moreover, in the above, the source/drain material layers **18***a* and **18***b* are formed after the source/drain regions **17***a* and **17***b* have been formed. However, the order of formation of these is not particularly limited. The source/drain regions **17***a* and **17***b* may be formed after the source/drain material layers **18***a* and **18***b* have been formed.

[**0102**] Next, in the present embodiment, boron ions are implanted as p-type impurities into the source/drain material layers **18***a* and **18***b* under the following optimized conditions: the acceleration energy is approximately 0.5 to 20 keV, and the dose is approximately 1×10^{14} to 1×10^{16} cm^{-2}. Then, the impurities in the source/drain regions **17***a* and **17***b* are activated by performing activation anneal under the following conditions; for example, the substrate temperature is approximately 950 to 1050° C. In the case where in-situ doping is performed when the source/drain regions **17***a* and **17***b* are formed, impurity implantation and heat treatment may be omitted.

[**0103**] Subsequently, as shown in **FIG. 5F**, for example, nickel layers as refractory metal layers are formed by sputtering, and then a reaction is caused between nickel and silicon by heat treatment, thereby forming first and second nickel silicide layers **19***a* and **19***b* on the source/drain material layers **18***a* and **18***b*. A nickel silicide layer is also formed on the surface layer of the gate electrode **14***c*, whereby the gate electrode **14***c* has a polycide structure. Thereafter, an unreacted nickel layer is removed by wet etching.

[**0104**] Note that, instead of the nickel layers, cobalt layers may be formed as refractory metal layers.

[**0105**] Next, steps to be performed before the cross-sectional structure shown in **FIG. 5G** is obtained will be described.

[**0106**] First, a silicon nitride layer is formed as a cover insulating layer **20** on the entire surface by plasma CVD, and then a silicon dioxide layer is formed by high-density CVD (HDPCVD) which is excellent in filling capability. The silicon dioxide layer is used as an interlayer insulating layer **21**. Thereafter, in order to planarize projections and depressions formed on the upper surface of the interlayer insulating layer **21** under the influence of projections and depressions of the gate electrode **10***c* and the like, the upper surface of the interlayer insulating layer **21** is polished and planarized by chemical mechanical polishing (CMP).

[**0107**] Subsequently, the interlayer insulating layer **21** and the cover insulating layer **20** are patterned by photolithography, thus forming first and second holes **21***a* and **21***b* having depths which reach the nickel silicide layers **19***a* and **19***b*. Then, a TiN layer is formed as a glue layer in the first and second holes **21***a* and **21***b* and on the upper surface of the interlayer insulating layer **21** by sputtering, and a tungsten layer is further formed thereon by CVD, whereby the holes **21***a* and **21***b* are completely filled with the tungsten layer. Thereafter, redundant portions of the tungsten layer and the glue layer, which are formed on the interlayer insulating layer **21**, are polished by CMP to be removed, but these films are left as first and second conductive plugs **22***a* and **22***b* in the holes **21***a* and **21***b*.

[**0108**] Thereafter, the step of forming metal interconnections electrically connected to the conductive plugs **22***a* and **22***b* on the interlayer insulating layer **21** is taken, but details thereof will be omitted.

[**0109**] Through the above-described steps, the basic structure of a p-type MOS transistor TR in which the source/drain material layers **18***a* and **18***b* are buried in the recesses **10***a* and **10***b* is completed.

[**0110**] In the MOS transistor TR, silicon lattice in the silicon substrate **10** is forcefully stretched so as to match the

large lattice spacing of SiGe due to a mismatch between the lattice constant of the silicon substrate **10** and those of the source/drain material layers **18***a* and **18***b*, and stress in the directions of the arrows in the drawing are applied to a channel under the gate electrode **14***c*. As a result, compared to the case where stress is not applied, the mobility of carriers in the channel is improved, and the drive capability of the MOS transistor can be improved.

[**0111**] According to the above-described embodiment, in the step of **FIG. 5D**, a TMAH solution or an organic alkaline solution has been used as an etchant for forming the first and second recesses **10***a* and **10***b*. Accordingly, one (111) plane automatically appears at the first or second side surface **10***c* or **10***d* of each recess **10***a* and **10***b*, and the shape of each recess **10***a* or **10***b* can be easily controlled. Consequently, even when MOS transistors configured as described above are integrally formed in the silicon substrate **10**, the shapes of the recesses **10***a* and **10***b* are less prone to vary among the MOS transistors, compared to Non-Patent Document 1 in which the first and second side surfaces **10***c* and **10***d* become curved surfaces. This makes it possible to suppress variation in characteristics of MOS transistors among elements and to improve the reliability of a semiconductor device such as an LSI.

[**0112**] **FIG. 6** is a view drawn based on a scanning electron microscope (SEM) image of recesses **10***a* and **10***b* after the recesses **10***a* and **10***b* have been formed in accordance with the present embodiment. As shown in this drawing, (111) planes appear at the first and second side surfaces **10***c* and **10***d* constituting side surfaces of the first and second recesses **10***a* and **10***b*.

[**0113**] The distance d to which each recess **10***a* or **10***b* goes under the first sidewall **15***a* or **15***b* is not particularly limited.

[**0114**] **FIG. 7** is a view drawn based on an SEM image in the case where the above-described distance d is increased by adjusting the substrate temperature when the first sidewall insulating layer **15** is formed.

[**0115**] When the entry length d is made large as described above, the distances between the channel under the gate electrode **10***c* and the upper end portions **10***e* and **10***f* of the recesses **10***a* and **10***b* become short. Accordingly, stress can be efficiently applied from the upper end portions **10***e* and **10***f* to the channel. Such an advantage can also be obtained in each embodiment to be described later.

[**0116**] Incidentally, the present embodiment is not limited to the above. For example, the source/drain material layers **18***a* and **18***b* may be constituted of metal layers made of a noble metal such as Pt (platinum), instead of the SiGe layers. In this case, the fabricated transistor TR is a Schottky transistor. This also applies to each embodiment to be described later.

(3) Third Embodiment

[**0117**] Next, a method of manufacturing a semiconductor device according to a third embodiment of the present invention will be described.

[**0118**] **FIGS. 8A** to **8**C are cross-sectional views of a semiconductor device according to the present embodiment in the process of manufacture. Note that the components already described in the second embodiment are denoted by the same reference numerals and codes in these drawings and will not be further described below.

[**0119**] First, in accordance with the second embodiment, the structure shown in **FIG. 5A** is completed. However, though ions of p-type impurities have been implanted into the polysilicon layer **14** at a high concentration sufficient to inhibit the etching of polysilicon in the TMAH solution from proceeding in the second embodiment, ions of p-type impurities are implanted into the polysilicon layer **14** at a low concentration at which the polysilicon layer **14** is etched by a TMAH solution partway in the present embodiment. In the present embodiment, boron is adopted as such p-type impurities, and ions thereof are implanted into the above-described polysilicon layer **14** under the following conditions: the acceleration energy is approximately 0.5 to 20 keV, and the dose is approximately 1×10^{13} to 5×10^{15} cm^{-3}.

[**0120**] Thereafter, the structure shown in **FIG. 5C** is obtained in accordance with the aforementioned second embodiment.

[**0121**] Next, steps to be performed before the cross-sectional structure shown in **FIG. 8A** is obtained will be described.

[**0122**] First, the silicon substrate **10** is immersed in a TMAH solution having a volume concentration of 5 to 30% and a temperature of 0 to 50° C., thereby starting the etching of the silicon substrate **10**. At this time, since the concentration of the p-type impurities introduced into the polysilicon layer **14** constituting the gate electrode **14***c* has been set low in advance, not only the silicon substrate **10** but also the upper surface of the gate electrode **14***c* are etched in this etching.

[**0123**] Then, when the depths of the first and second recesses **10***a* and **10***b* reach approximately 20 to 70 nm and the thickness of the gate electrode **14***c* is reduced to approximately 30 to 150 nm, the above-described etching is stopped. Thus, as shown in the drawing, a structure can be obtained, in which the first and second recesses **10***a* and **10***b* having the first and second side surfaces **10***c* and **10***d* constituted of (111) planes are formed, and in which the height of the gate electrode **14***c* is smaller than those of the first sidewalls **15***a* and **15***b*.

[**0124**] Subsequently, as shown in **FIG. 8B**, SiGe layers to be used as first and second source/drain material layers **18***a* and **18***b* are selectively epitaxially grown in the first and second recesses **10***a* and **10***b* by performing the aforementioned step of **FIG. 5E**.

[**0125**] Next, in the present embodiment, boron ions are implanted as p-type impurities into the source/drain material layers **18***a* and **18***b* under the following optimized conditions: the acceleration energy is approximately 0.5 to 20 keV, and the dose is approximately 1×10^{14} to 1×10^{6} cm^{-2}. Thereafter, the impurities in the source/drain regions **17***a* and **17***b* are activated by performing activation anneal under the following conditions: for example, the substrate temperature is approximately 950 to 1050° C. In the case where in-situ doping is performed when the source/drain regions **18***a* and **18***b* are formed, impurity implantation and heat treatment may be omitted. Next, as shown in **FIG. 8C**, nickel layers are respectively formed as refractory metal layers on the first and second source/drain material layers

18*a* and **18***b* and the gate electrode **14***c* by sputtering, and then a reaction is caused between nickel and silicon by heat treatment, thereby forming nickel silicide layers **19***a* and **19***b* on the first and second source/drain material layers **18***a* and **18***b* made of SiGe layers. This silicidation also occurs in the gate electrode **14***c*. However, since the thickness of the gate electrode **14***c* has been reduced in the step of **FIG. 8A** in advance, the silicidation occurs in the entire gate electrode **14***c*, and the gate electrode **14***c* becomes a metal gate made of nickel silicide.

[**0126**] Note that, instead of the nickel layers, cobalt layers, platinum layers, or layers of a mixture of cobalt and platinum may be adopted as refractory metal layers.

[**0127**] Thereafter, the aforementioned step of **FIG. 5G** is performed, thereby completing the basic structure of a MOS transistor.

[**0128**] According to the present embodiment described above, the first or second side surface **10***c* or **10***d* of each recess **10***a* or **10***b* can be constituted of one (111) plane similarly to the second embodiment.

[**0129**] Furthermore, in the present embodiment, the concentration of the p-type impurities introduced into the gate electrode **14***c* is set lower than that in the second embodiment, whereby the gate electrode **14***c* is etched simultaneously with the formation of the recesses **10***a* and **10***b* using the TMAH solution and the height of the gate electrode **14***c* is reduced.

[**0130**] This allows the gate electrode **14***c* to become a metal gate by silicidation simultaneously with the formation of the nickel silicide layers **19***a* and **19***b* by siliciding the first and second source/drain material layers **18***a* and **18***b*, and therefore allows compatibility between a formation process of the metal gate and that of the recesses **10***a* and **10***b*.

[**0131**] Incidentally, in the above, the TMAH solution has been used as an etchant when the recesses **10***a* and **10***b* are formed. However, an advantage similar to the above can also be obtained when an organic alkaline solution is used instead of the TMAH solution.

(4) Fourth Embodiment

[**0132**] Next, a method of manufacturing a semiconductor device according to a fourth embodiment of the present invention will be described.

[**0133**] **FIGS. 9A** to **9D** are cross-sectional views of a semiconductor device according to the present embodiment in the process of manufacture. Note that the components already described in the second embodiment are denoted by the same reference numerals and codes in these drawings and will not be further described below.

[**0134**] First, after the cross-sectional structure shown in **FIG. 5C** has been obtained in accordance with the aforementioned second embodiment, a silicon dioxide layer having a thickness of approximately 5 to 100 nm is formed as a second sidewall insulating layer **25** on the silicon substrate **10**, the first sidewalls **15***a* and **15***b*, and the gate electrode **14***c*, as shown in **FIG. 9A**. A method of forming the silicon dioxide layer is not particularly limited. However, in the present embodiment, the silicon dioxide layer is formed by CVD using silane as reactant gas. Further, instead of the silicon dioxide layer, a silicon nitride layer may be formed as the second sidewall insulating layer **25**.

[**0135**] Next, steps to be performed before the cross-sectional structure shown in **FIG. 9B** is obtained will be described.

[**0136**] First, the second sidewall insulating layer **25** is etched back by plasma etching to leave second sidewalls **25***a* and **25***b* on the side surfaces of the first sidewalls **15***a* and **15***b*. Sidewalls **26***a* and **26***b* each including two insulating layers as described above are also referred to as double sidewalls.

[**0137**] Subsequently, using the second sidewalls **25***a* and **25***b* and the gate electrode **14***c* as a mask, ions of, for example, arsenic are implanted as n-type impurities into the silicon substrate **10** under the following conditions: the acceleration energy is approximately 3 to 20 keV, and the dose is 1×10^{14} to 5×10^{15} cm^{-2}. Thus, in the silicon substrate **10**, first and second impurity diffusion regions **27***a* and **27***b* of a second conductivity type (n-type) are formed more deeper than the source/drain extensions **16***a* and **16***b* of the first conductivity type (p-type).

[**0138**] Next, steps to be performed before the cross-sectional structure shown in **FIG. 9C** is obtained will be described.

[**0139**] First, the silicon substrate **10** is immersed in a TMAH solution having a volume concentration of 5 to 30% and a temperature of 0 to 50° C., thereby starting the etching of the silicon substrate **10**. Thus, first and second recesses **10***a* and **10***b* having depths of approximately 20 to 80 nm, which are deeper than that of the source/drain extensions **16***a* and **16***b*, are formed in the silicon substrate **10** beside the gate electrode **14***c*.

[**0140**] At this time, as apparent from the experimental results described using **FIG. 4**, silicon into which n-type impurities are introduced has a higher etch rate in a TMAH solution, compared to silicon into which p-type impurities are introduced. Accordingly, the etching of the first and second impurity diffusion regions **27***a* and **27***b* into which the n-type impurities (arsenic) are introduced proceeds faster in the TMAH solution compared to those of the first and second source/drain extensions **16***a* and **16***b* and the source/drain regions **17***a* and **17***b* into which the p-type impurities (boron) are introduced.

[**0141**] In the case where etch rates differ between two layers as described above, different etched surfaces are exposed to the outside on opposite sides of the interface between these layers. Accordingly, at the first and second side surfaces **10***c* and **10***d* of each of the recesses **10***a* and **10***b*, (111) planes appear in portions which are in contact with the first and second impurity diffusion regions **27***a* and **27***b* of the p-type, whereas other (111) planes different from the above-described ones appear in portions which are in contact with the first and second source/drain extensions **16***a* and **16***b* and the source/drain regions **17***a* and **17***b*, which are of the n-type.

[**0142**] As a result, in the present embodiment, the first and second recesses **10***a* and **10***b* can be obtained in which each of the first and second side surfaces **10***c* and **10***d* is constituted of two different (111) planes and in which the cross-

sectional shapes of the first and second side surfaces **10***c* and **10***d* are concave shapes recessed below the gate electrode **14***c*.

[**0143**] Note that the recesses **10***a* and **10***b* having the above-described cross-sectional shapes can also be formed using an organic alkaline solution instead of the TMAH solution.

[**0144**] Thereafter, as shown in **FIG. 9D**, SiGe layers are selectively epitaxially grown in the recesses **10***a* and **10***b* by performing the aforementioned step of **FIG. 5E**, respectively. The SiGe layers are used as first and second source/drain material layers **18***a* and **18***b*.

[**0145**] Thereafter, the aforementioned steps of **FIGS. 5F and 5G** are performed, thereby completing the basic structure of a MOS transistor.

[**0146**] According to the present embodiment described above, as shown in **FIG. 9B**, at positions deeper than the first and second source/drain extensions **16***a* and **16***b* and the source/drain regions **17***a* and **17***b*, which are of the p-type, the first and second impurity diffusion regions **27***a* and **27***b* of the n-type, which is opposite to the conductivity type of the foregoing, have been formed. Due to this difference in conductivity type, different (111) planes appear at each of the first and second side surfaces **10***c* and **10***d* of the first and second recesses **10***a* and **10***b* when these recesses **10***a* and **10***b* are formed using the TMAH solution in the step of **FIG. 9C**, and the first and second recesses **10***a* and **10***b* can be obtained in which the cross-sectional shapes of the first and second side surfaces **10***c* and **10***d* are concave shapes recessed below the gate electrode **14***c*.

[**0147**] **FIG. 10** is a view drawn based on an SEM image of recesses **10***a* and **10***b* after the recesses **10***a* and **10***b* have been formed in accordance with the present embodiment. As shown in this drawing, two different (111) planes appear at each of the respective side surfaces of the first and second recesses **10***a* and **10***b*.

[**0148**] Such a recess shape makes characteristics of interface between the silicon substrate **10** and the gate insulating film **13** less prone to being deteriorated by stress because the stress has a peak at a position slightly deeper than the surface of the silicon substrate **10** as represented by the arrows in **FIG. 9D**, and therefore can achieve excellent reliability of the MOS transistor while improving the drive characteristics thereof.

(5) Fifth Embodiment

[**0149**] Next, a method of manufacturing a semiconductor device according to a fifth embodiment of the present invention will be described.

[**0150**] **FIGS. 11A** to **11**E are cross-sectional views of a semiconductor device according to the present embodiment in the process of manufacture. Note that the components already described in the second to fourth embodiments are denoted by the same reference numerals and codes in these drawings and will not be further described below.

[**0151**] As described below, a silicon-on-insulator (SOI) substrate is used as a semiconductor substrate in the present embodiment.

[**0152**] To begin with, steps to be performed before the cross-sectional structure shown in **FIG. 11A** is obtained will be described.

[**0153**] First, an SOI substrate **30** in which a buried insulating layer **32** and a silicon layer **33** are formed on a silicon substrate **31** is prepared by, for example, bond-and-etch-back technique. Then, an element isolation trench **33***g* having a depth which reaches the buried insulating layer **32** is formed in the silicon layer **33**. Furthermore, a silicon dioxide layer is buried as an element isolation insulating film **11** in the element isolation trench **33***g*.

[**0154**] The surface orientation of the silicon layer **33** is not particularly limited. However, in the present embodiment, the silicon layer **33** is formed so that the orientation thereof becomes (001). Further, a silicon dioxide layer having a thickness of, for example, approximately 5 to 100 nm is formed as the buried insulating layer **32**.

[**0155**] Next, as shown in **FIG. 11B**, an n-well **34** is formed in a p-type MOS transistor formation region delimited by the element isolation insulating film **11** by implanting phosphorus ions as n-type impurities into the silicon layer **33** under the following conditions: the acceleration energy is approximately 300 keV or more, and the dose is 1×10^{13} cm^{-3} or more.

[**0156**] Subsequently, the surface of the silicon layer **33** is thermally oxidized, thus forming a gate insulating film **13** which is made of silicon dioxide and which has a thickness of approximately 0.5 to 5.0 nm. Here, a gate insulating film in which a very small amount of nitrogen is added to silicon dioxide may be adopted as the gate insulating film **13**. Further, a polysilicon layer **14** having a thickness of approximately 10 to 300 nm is formed on the gate insulating film **13** by LPCVD using silane, and then ions of p-type impurities are implanted into the polysilicon layer **14** at a concentration which is similar to that of the second embodiment and at which the etching of polysilicon in a TMAH solution does not proceed.

[**0157**] Thereafter, the structure shown in **FIG. 11C** is obtained by performing the aforementioned steps of **FIGS. 5B and 5C**. In this structure, the first and second source/drain extensions **16***a* and **16***b* and the source/drain regions **17***a* and **17***b* are formed in the silicon layer **33** beside the gate electrode **14***c*.

[**0158**] Next, the silicon substrate **10** is immersed in a TMAH solution having a volume concentration of 5 to 30% and a temperature of 0 to 50° C., thereby starting the etching of the silicon substrate **10**. Thus, as shown in **FIG. 11D**, first and second recesses **33***a* and **33***b* having depths of approximately 5 to 50 nm are formed in the silicon layer **33** beside the gate electrode **14***c*.

[**0159**] According to the experimental results shown in **FIG. 2**, a TMAH solution selectively etches only silicon but does not etch silicon dioxide. Accordingly, in this etching, the etch rate of the silicon layer **33** becomes low in the vicinities of the gate insulating film **13** and the buried insulating layer **32**, which are made of silicon dioxide, whereas the etch rate becomes fast in a portion located apart from these insulating layers. Due to such a difference in etch rate, each of the first and second side surfaces **33***c* and **33***d* constituting the side surfaces of the recesses **33***a* and **33***b* is not constituted of a single crystal plane but constituted of two different (111) planes, and the cross-sectional shape thereof becomes convex.

[0160] The recesses **33***a* and **33***b* having the above-described cross-sectional shapes can also be formed using an organic alkaline solution instead of the TMAH solution.

[0161] Thereafter, as shown in **FIG. 11E**, SiGe layers are selectively epitaxially grown in the recesses **33***a* and **33***b* by performing the aforementioned step of **FIG. 5E**, respectively. The SiGe layers are used as first and second source/drain material layers **18***a* and **18***b*.

[0162] Thereafter, the aforementioned steps of **FIGS. 5F and 5G** are performed, thereby completing the basic structure of a MOS transistor.

[0163] According to the present embodiment described above, in the etching using the TMAH solution which has been described in **FIG. 11D**, the etch rate of the silicon layer **33** becomes low in the vicinity of the gate insulating film **13** and in the vicinity of the buried insulating film **32** partially constituting the SOI substrate **30**. As a result, the etch rate of the silicon layer **33** varies depending on the depth. Accordingly, each of the first and second side surfaces **33***c* and **33***d* of the first and second recesses **33***a* and **33***b* obtained by the above-described etching is constituted of two different (111) planes, and the cross-sectional shape thereof becomes convex.

[0164] As represented by the arrows in **FIG. 11E**, the first and second source/drain material layers **18***a* and **18***b* formed in the recesses **33***a* and **33***b* having the above-described cross-sectional shapes generate strong stress at the upper and lower surfaces of the silicon layer **33**. A stress distribution can be obtained in which stress becomes weak at the intermediate position of the film where both (111) planes intersect each other.

(6) Sixth Embodiment

[0165] Next, a method of manufacturing a semiconductor device according to a sixth embodiment of the present invention will be described.

[0166] **FIGS. 12A** to **12**D are cross-sectional views of a semiconductor device according to the present embodiment in the process of manufacture. In these drawings, the components already described in the second to fourth embodiments are denoted by the same reference numerals and codes and will not be further described below.

[0167] In the aforementioned fifth embodiment, the first and second recesses **33***a* and **33***b* having convex cross-sectional shapes are formed by using the SOI substrate **30**. On the other hand, in the present embodiment, recesses having the same cross-sectional shapes as the above-described ones are formed using not an SOI substrate but a general silicon substrate.

[0168] First, the cross-sectional structure shown in **FIG. 12A** is obtained by performing the aforementioned steps of **FIGS. 5A** to **5**C.

[0169] Subsequently, as shown in **FIG. 12B**, boron ions are implanted as p-type impurities which have the effect of delaying etching in a TMAH solution, into the silicon substrate **10** using the gate electrode **14***c* and the first sidewalls **15***a* and **15***b* as a mask, thus forming third and fourth impurity diffusion regions **35***a* and **35***b* of the p-type. As conditions for this ion implantation, conditions are adopted under which the third and fourth impurity diffusion regions **35***a* and **35***b* have higher concentrations and deeper depths than the source/drain extensions **16***a* and **16***b* and the source/drain regions **17***a* and **17***b*, which are of the p-type. In the present embodiment, as such conditions, for example, boron implantation under conditions where the acceleration energy is approximately 1 to 20 keV and where the dose is approximately 5×10^{14} to 2×10^{16} cm^{-2} is adopted. As a result of such ion implantation, the third and fourth impurity diffusion regions **35***a* and **35***b* which are of the p-type and which densely spread to portions of the silicon substrate **10** that are at deeper positions than the source/drain regions **17***a* and **17***b* are formed.

[0170] Thereafter, activation anneal is performed by adopting the same conditions as those in the second embodiment, thus activating the impurities in the source/drain regions **17***a* and **17***b*.

[0171] Incidentally, the order of formation of the third and fourth impurity diffusion regions **35***a* and **35***b* and the source/drain regions **17***a* and **17***b* is not particularly limited to the above. For example, the above-described order may be reversed to form the source/drain regions **17***a* and **17***b* after the third and fourth impurity diffusion regions **35***a* and **35***b* have been formed.

[0172] Subsequently, the silicon substrate **10** is immersed in a TMAH solution having a volume concentration of 5 to 30% and a temperature of 0 to 50° C., thereby starting the etching of the silicon substrate **10**. Thus, first and second recesses **10***a* and **10***b* having depths of approximately 30 to 120 nm are formed in the silicon substrate **10** beside the gate electrode **14***c* as shown in **FIG. 12C**.

[0173] As described in **FIGS. 2 and 3**, in the etching of silicon in a TMAH solution, the etch rate becomes low in silicon dioxide and silicon into which p-type impurities are introduced at a high concentration. Accordingly, in this etching, the etch rate becomes low in the vicinity of the gate insulating film **13** made of silicon dioxide and in the vicinities of the third and fourth impurity diffusion regions **35***a* and **35***b* into which the p-type impurities are introduced at a high concentration, whereas the etch rate does not become low in a portion located apart from the foregoing. Due to such an uneven etch rate, each of the first and second side surfaces **10***c* and **10***d* of the respective recesses **10***a* and **10***b* is not constituted of a single crystal plane but constituted of two different (111) planes, similarly to the fifth embodiment. The cross-sectional shape thereof becomes convex.

[0174] The recesses **10***a* and **10***b* having the above-described cross-sectional shapes can also be formed using an organic alkaline solution instead of the TMAH solution.

[0175] Subsequently, as shown in **FIG. 12D**, SiGe layers are selectively epitaxially grown in the recesses **10***a* and **10***b* by performing the aforementioned step of **FIG. 5E**, respectively. The SiGe layers are used as first and second source/drain material layers **18***a* and **18***b*.

[0176] Thereafter, the aforementioned steps of **FIGS. 5F and 5G** are performed, thereby completing the basic structure of a MOS transistor.

[0177] According to the present embodiment described above, p-type impurities which have the effect of delaying etching in a TMAH solution have been introduced into the third and fourth impurity diffusion regions **35***a* and **35***b*.

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Accordingly, in the etching step of **FIG. 12C**, the etch rate of silicon becomes low in the vicinities of the third and fourth impurity diffusion regions **35***a* and **35***b* and the gate insulating film **13**. As a result, as shown in **FIG. 12C**, each of the first and second side surfaces **10***c* and **10***d* of the first and second recesses **10***a* and **10***b* is constituted of two (111) planes, and the first and second recesses **10***a* and **10***b* having convex cross-sectional shapes can be formed. Thus, stress favorable for the improvement in the mobility can be applied to the channel from the source/drain material layers **18***a* and **18***b* formed in the respective recesses **10***a* and **10***b*.

(7) Seventh Embodiment

[**0178**] Next, a method of manufacturing a semiconductor device according to a seventh embodiment of the present invention will be described.

[**0179**] **FIGS. 13A** to **13**E are cross-sectional views of a semiconductor device according to the present embodiment in the process of manufacture. In these drawings, the components already described in the second to sixth embodiments are denoted by the same reference numerals and codes and will not be further described below.

[**0180**] In the aforementioned sixth embodiment, as shown in **FIG. 12B**, the third and fourth impurity diffusion regions **35***a* and **35***b* for delaying etching in the TMAH solution have been formed using the gate electrode **14***c* and the first sidewalls **15***a* and **15***b* as a mask for ion implantation.

[**0181**] On the other hand, in the present embodiment, before a gate electrode **14***c* is formed, an impurity diffusion region having the effect of increasing the etch rate is formed.

[**0182**] First, as shown in **FIG. 13A**, an element isolation insulating film **11** is formed in an element isolation trench **10***g*, and then an n-well **12** is formed in a p-type MOS transistor formation region delimited by the element isolation insulating film **11**.

[**0183**] Subsequently, boron ions are implanted as n-type impurities, which have the effect of delaying etching in a TMAH solution, into a silicon substrate **10** under conditions where the acceleration energy is approximately 5 to 30 keV and where the dose is approximately 1×10^{13} to 5×10^{15} cm^{-3}, thus forming a fifth impurity diffusion region **36** at a position deeper than source/drain regions to be formed later.

[**0184**] Next, as shown in **FIG. 13B**, a gate insulating film **13** made of silicon dioxide is formed by thermally oxidizing the surface of the silicon substrate **10**, and a polysilicon layer **14** is further formed on the gate insulating film **13** by LPCVD using silane. Thereafter, adopting ion implantation conditions similar to those of the second embodiment, ions of p-type impurities are implanted into the polysilicon layer **14** at a concentration at which the etching of polysilicon in a TMAH solution does not proceed.

[**0185**] Subsequently, as shown in **FIG. 13C**, source/drain extensions **16***a* and **16***b* and source/drain regions **17***a* and **17***b* are formed in the silicon substrate **10** beside the gate electrode **14***c* by performing the aforementioned steps of **FIGS. 5B and 5C**.

[**0186**] Then, the silicon substrate **10** is immersed in a TMAH solution having a volume concentration of 5 to 30% and a temperature of 0 to 50° C., thereby starting the etching of the silicon substrate **10**. Thus, first and second recesses **10***a* and **10***b* having depths of approximately 20 to 150 nm are formed in the silicon substrate **10** beside the gate electrode **14***c* as shown in **FIG. 13D**.

[**0187**] In this etching, the etch rate of silicon increases in the vicinity of the fifth impurity diffusion region **36** into which the n-type impurities having the effect of increasing the etch rate are introduced at a high concentration, whereas the etch rate of silicon decreases in the vicinities of the source/drain extensions **16***a* and **16***b* and the source/drain regions **17***a* and **17***b* into which the p-type impurities are introduced at a high concentration. Accordingly, for the same reason as that in the sixth embodiment, each of the first and second side surfaces **10***c* and **10***d* of the respective recesses **10***a* and **10***b* is not constituted of a single crystal plane but constituted of two different (111) planes, and the cross-sectional shape thereof becomes convex.

[**0188**] Note that the first and second recesses **10***a* and **10***b* having cross-sectional structures similar to the above can also be formed using an organic alkaline solution instead of the TMAH solution.

[**0189**] Next, as shown in **FIG. 13E**, SiGe layers are selectively epitaxially grown in the recesses **10***a* and **10***b* by performing the aforementioned step of **FIG. 5E**, respectively. The SiGe layers are used as first and second source/drain material layers **18***a* and **18***b*.

[**0190**] Thereafter, the aforementioned steps of **FIGS. 5F** and **5**G are performed, thereby completing the basic structure of a MOS transistor.

[**0191**] According to the present embodiment described above, the fifth impurity diffusion region **36** having the effect of suppressing the etching of silicon in a TMAH solution or an organic alkaline solution has been formed at a position deeper than the source/drain regions **17***a* and **17***b* in the silicon substrate **10**. Accordingly, similar to the sixth embodiment, when the first and second recesses **10***a* and **10***b* are formed by etching, the etch rate varies depending on the distance from the surface of the silicon substrate **10**. Consequently, each of the first and second side surfaces **10***c* and **10***d* of the first and second recesses **10***a* and **10***b* is constituted of two (111) planes, and the first and second recesses **10***a* and **10***b* having convex cross-sectional shapes can be obtained. Thus, similar to the sixth embodiment, stress favorable for the improvement in the mobility can be applied to the channel from the source/drain material layers **18***a* and **18***b* formed in the respective recesses **10***a* and **10***b*.

(8) Eighth Embodiment

[**0192**] **FIGS. 14A and 14B** are cross-sectional views of a semiconductor device according to an eighth embodiment of the present invention in the process of manufacture, and **FIG. 15** is a plan view thereof. In these drawings, the components already described in the second to sixth embodiments are denoted by the same reference numerals and codes and will not be further described below.

[**0193**] In the aforementioned second to fourth embodiments, a substrate with (001) surface orientation is adopted as a silicon substrate in which a MOS transistor is fabricated, and the gate width direction (extending direction of the gate electrode) is set to the [110] direction of the silicon substrate.

[**0194**] On the other hand, in the present embodiment, a silicon substrate with (110) surface orientation is adopted,

and the gate width direction (extending direction of a gate electrode) is set to the [111] direction of the silicon substrate.

[0195] Adopting such an orientation, after the steps of **FIGS. 5A** to **5**C described in the second embodiment have been performed, first and second recesses **10***a* and **10***b* having depths of approximately 10 to 100 nm are formed in the silicon substrate **10** beside the gate electrode **14***c* by immersing the silicon substrate **10** in a TMAH solution having a volume concentration of 5 to 30% and a temperature of 0 to 50° C., thus obtaining a cross-sectional structure as shown in **FIG. 14A**.

[0196] In the case where the orientation of the silicon substrate **10** is (110) and the extending direction of the gate electrode **14***c* is the [111] direction as described above, a (111) plane which is exposed by etching in the TMAH solution is perpendicular to the surface of the silicon substrate **10**. Accordingly, the side surfaces of the first and second recesses **10***a* and **10***b*, each of which is constituted of this (111) plane, are perpendicular to the surface of the silicon substrate **10**.

[0197] **FIG. 15** is a plan view after this step has been finished. The aforementioned **FIG. 14A** corresponds to a cross-sectional view taken along the I-I line of **FIG. 15**.

[0198] As shown in **FIG. 15**, the gate width direction, i.e. the extending direction of the gate electrode **14***c*, is the [111] direction, and the orientation of the silicon substrate **10** is (110). By adopting such an orientation, the side surfaces of the first and second recesses **10***a* and **10***b* can be made perpendicular to the surface of the silicon substrate **10**.

[0199] Next, as shown in **FIG. 14B**, SiGe layers are selectively epitaxially grown in the recesses **10***a* and **10***b* by performing the aforementioned step of **FIG. 5E**, respectively. The SiGe layers are used as first and second source/drain material layers **18***a* and **18***b*.

[0200] Thereafter, the aforementioned steps of **FIGS. 5F and 5G** are performed, thereby completing the basic structure of a MOS transistor.

[0201] According to the present embodiment described above, the silicon substrate **10** with (110) orientation has been adopted, and the extending direction of the gate electrode **14***c* has been set to the [111] direction. Thus, etched surfaces of the silicon substrate **10** which have been etched in a TMAH solution or an organic alkaline solution become (111) planes in a direction perpendicular to the surf ace of the silicon substrate **10**, and the first and second side surfaces **10***c* and **10***d* of the respective recesses **10***a* and **10***b* are constituted of the (111) planes. Accordingly, as represented by the arrows in **FIG. 14B**, uniform stress having a small variation in strength in the depth direction can be stably applied to the channel from the first and second source/drain material layers **18***a* and **18***b* in the recesses **10***a* and **10***b*.

(9) Ninth Embodiment

[0202] **FIG. 16** is a cross-sectional view of a semiconductor device according to a ninth embodiment of the present invention in the process of manufacture, and **FIG. 17** is a plan view thereof. In these drawings, the components already described in the eighth embodiment are denoted by the same reference numerals and codes and will not be further described below.

[0203] In the eighth embodiment, the silicon substrate **10** with (110) orientation has been adopted, and the extending direction of the gate electrode **14***c* has been set to the [111] direction.

[0204] On the other hand, in the present embodiment, the orientation of a silicon substrate **10** is (110) similarly to the eighth embodiment, but the extending direction of the gate electrode **14***c* is set to the [100] direction.

[0205] In the case where such an orientation has been adopted and the steps of **FIGS. 14A and 14B** in the eighth embodiment have been performed, (111) planes constituting the first and second side surfaces **10***c* and **10***d* of the first and second recesses **10***a* and **10***b* come to have a tilt angle θ which is more gentle than that in the aforementioned second embodiment.

[0206] Thus, stress applied to the channel from the first and second source/drain material layers **18***a* and **18***b* steeply changes at positions closer to the surface layer than at positions deeper in the silicon substrate **10**. Accordingly, a large stress can be applied to the channel, and the amount of the stress can be easily controlled.

[0207] Note that **FIG. 17** is a plan view of this semiconductor device and that **FIG. 16** corresponds to a cross-sectional view taken along the II-II line of **FIG. 17**.

(10) Tenth Embodiment

[0208] Next, a method of evaluating a semiconductor device according to a tenth embodiment of the present invention will be described.

[0209] In order to check whether a MOS transistor has characteristics as designed, a test transistor called a test element group (TEG) is fabricated in the development phase, and the carrier distribution in the channel of this transistor is actually physically measured. For the realization of this, it is necessary to expose the surface of a silicon substrate, which becomes a channel, to the outside by removing a gate electrode and a gate insulating film after the MOS transistor has been fabricated.

[0210] However, when the gate electrode and the gate insulating film are removed, if the silicon substrate is damaged, the carrier distribution in the channel is disturbed, and the obtained measurement value may deviate from the value in the transistor provided for actual use.

[0211] Accordingly, for an evaluation as described above, it is necessary to remove the gate electrode and the gate insulating film while preventing the silicon substrate from being damaged.

[0212] **FIGS. 18A** to **18**E are cross-sectional views showing a method of fabricating a TEG used in a test method according to the present embodiment.

[0213] To begin with, steps to be performed before the cross-sectional structure shown in **FIG. 18A** is obtained will be described.

[0214] First, an element isolation trench **40***g* for shallow trench isolation (STI) is formed in a silicon substrate **40** with (001) surface orientation, and then a silicon dioxide layer is buried as an element isolation insulating film **41** in the element isolation trench **40***g*. Thereafter, an n-well **42** is formed in a p-type MOS transistor formation region delim-

ited by the element isolation insulating film **41** by implanting phosphorus ions as n-type impurities into the silicon substrate **40** under the following conditions: the acceleration energy is approximately 300 keV or more, and the dose is 1×10^{15} cm^{-2} or more.

[**0215**] Subsequently, a gate insulating film **43** which is made of silicon dioxide and which has a thickness of approximately 0.5 to 10.0 nm is formed by thermally oxidizing the surface of the silicon substrate **40**, and then a polysilicon layer **44** having a thickness of approximately 20 to 300 nm is formed on the gate insulating film **43** by LPCVD using silane. Here, a gate insulating film in which a very small amount of nitrogen is added to silicon dioxide may be adopted as the gate insulating film **43**.

[**0216**] In the aforementioned second embodiment, in order to prevent the gate electrode from being etched in the TMAH solution, the p-type impurities having the effect of delaying the etch rate have been introduced into the polysilicon layer **14** (refer to **FIG. 5A**) constituting the gate electrode. However, in the present embodiment, since such a slow etch rate makes the removal of a gate electrode difficult, p-type impurities are not introduced into the polysilicon layer **44**.

[**0217**] Next, steps to be performed before the cross-sectional structure shown in **FIG. 18B** is obtained will be described.

[**0218**] First, the polysilicon layer **44** is patterned into a gate electrode **44***c* by photolithography.

[**0219**] Subsequently, for example, boron ions are implanted as p-type impurities into the silicon substrate **40** using the gate electrode **44***c* as a mask, thus shallowly forming first and second source/drain extensions **46***a* and **46***b* in the silicon substrate **40** beside the first and second side surfaces **44***a* and **44***b* of the gate electrode **44***c*. As conditions for this ion implantation, the same ones for actual MOS transistors for commercial products are adopted. For example, conditions where the acceleration energy is approximately 0.2 to 1.0 keV and where the dose is approximately 1×10^{14} to 5×10^{15} cm^{-2} are adopted. At the same time, pocket implantation of arsenic, phosphorus, antimony, or the like is performed as needed. Further, first and second source/drain extensions **46***a* and **46***b* using n-type impurities may be shallowly formed.

[**0220**] Thereafter, a silicon dioxide layer having a thickness of approximately 5 to 100 nm is formed as a sidewall insulating layer **45** on the entire surface by CVD using silane, thus covering the first and second side surfaces **44***a* and **44***b* of the gate electrode **44***c* with this sidewall insulating layer **45**. Note that, instead of the silicon dioxide layer, a silicon nitride layer may be formed as the sidewall insulating layer **45**.

[**0221**] Next, steps to be performed before the cross-sectional structure shown in **FIG. 18C** is obtained will be described.

[**0222**] First, the sidewall insulating layer **45** is etched back by plasma etching to leave sidewalls **45***a* and **45***b* on the first and second side surfaces **44***a* and **44***b*. Further, in this etching, the portion of the gate insulating film **43** which is not covered with the sidewalls **45***a* and **45***b* is also etched, whereby the gate insulating film **43** is left only under the gate electrode **44***c*.

[**0223**] Furthermore, similar to the actual MOS transistor for commercial products, using the gate electrode **44***c* and the sidewalls **45***a* and **45***b* as a mask, for example, boron ions are implanted as p-type impurities into the silicon substrate **40** under the following conditions: the acceleration energy is approximately 1 to 10 keV, and the dose is approximately 5×10^{14} to 1×10^{16} cm^{-2}. Thus, source/drain regions **47***a* and **47***b* which are deeper and denser than the source/drain extensions **46***a* and **46***b* are formed in the silicon substrate **40** beside the gate electrode **44***c*. This impurity implantation may be omitted as needed.

[**0224**] Thereafter, the impurities in the source/drain regions **47***a* and **47***b* are activated by performing activation anneal under the following conditions: for example, the substrate temperature is approximately 950 to 1050° C., and the processing time is 0 to 10 seconds.

[**0225**] Next, steps to be performed before the cross-sectional structure shown in **FIG. 18D** is obtained will be described.

[**0226**] First, the silicon substrate **40** is immersed in a TMAH solution having a volume concentration of 5 to 30% and a temperature of 0 to 50° C., thereby etching the portion of the silicon substrate **40** and the portion of the gate electrode **44***c*, which are not covered with silicon dioxide. As in the experimental results shown in **FIG. 2**, a TMAH solution is very excellent in the etch selectivity between silicon and silicon dioxide. Accordingly, in this etching, the erosion of the gate insulating film **43** made of a silicon dioxide layer having a small film thickness is negligibly small, and the channel under the gate insulating film **43** is not damaged.

[**0227**] Further, by this etching, first and second recesses **40***a* and **40***b* are formed in the portion of the silicon substrate **40**, which is not covered with the element isolation insulating film **41** and the sidewalls **45***a* and **45***b*.

[**0228**] Incidentally, this etching may be performed using an organic alkaline solution instead of the TMAH solution. In that case, damage to the channel is also small.

[**0229**] Thereafter, the silicon substrate **40** is immersed in an etchant made by mixing HF (hydrofluoric acid) and HCl at a volume ratio of 1:19, and the element isolation insulating film **41**, the sidewalls **45***a* and **45***b*, and the gate insulating film **43**, which are made of silicon dioxide, are thereby selectively removed. Thus the channel **40***d* of which carrier distribution is to be measured is exposed to the outside as shown in **FIG. 18E**. The channel **40***d* is terminated with hydrogen using hydrogen ions contained in the etchant, and is brought into a chemically active state.

[**0230**] Through the above-described steps, the basic structure of a TEG in which the channel **40***d* is exposed to the outside is completed.

[**0231**] Next, a method of evaluating a carrier distribution in the channel **40***d* of this TEG will be described with reference to **FIG. 19**.

[**0232**] First, the TEG fabricated through the aforementioned steps is put into a scanning tunneling microscope (STM) which is a kind of probe microscope, and a probe **50** is moved in a plane parallel to the channel **40***d* with the tip of the probe **50** in a noncontact state. At this time, a predetermined voltage is applied between the probe **50** and

the silicon substrate **40**, and the value of the tunneling current flowing between the probe and the silicon substrate **40** changes depending on the carrier distribution in the channel **40***d*. The carrier distribution in the channel **40***d* can be grasped by visualizing the change in the tunneling current.

[**0233**] According to the present embodiment described above, the gate electrode **44***c* is selectively etched using the TMAH solution or an organic alkaline solution as shown in **FIG. 18D**, and thereafter the gate insulating film **43** is etched and removed using the etchant made by mixing HF and HCl, thus exposing the channel **40***d* as shown in **FIG. 18E**.

[**0234**] Thus, use of a TMAH solution or an organic alkaline solution, which is excellent in the selectivity between silicon and silicon dioxide makes it possible to remove only the gate electrode **44***c* at a high etch selectivity without damaging the channel region **44***d* under the gate electrode **44***c*. Accordingly, in the process of exposing the channel **40***d*, there is no fear that the carrier distribution in the channel may fluctuate, and almost the same carrier distribution as that in the MOS transistor provided for actual use can be measured, thus making it possible to accurately evaluate the performance of the MOS transistor.

[**0235**] Furthermore, according to the present embodiment, since the gate insulating film **43** is etched and removed using an etchant containing HF, the surface of the channel **40***d* which is exposed after the gate insulating film **43** has been removed is automatically terminated with hydrogen. In the measurement of the carrier distribution using an STM, it is preferable that a surface to be measured is terminated with hydrogen in order to clearly observe the change in conductivity in the surface to be measured. According to the above, since hydrogen termination can be performed simultaneously with the removal of the gate insulating film **43**, there is no need for a step for hydrogen termination, and the carrier distribution can be easily measured.

[**0236**] **FIGS. 20A and 20B** are views drawn based on a relief image after the surface of the TEG of the present embodiment has been actually scanned using an STM. **FIG. 20B** is a view in which the brightness in the image of **FIG. 20A** is enhanced.

[**0237**] Further, **FIG. 21** is an image obtained by observing the carrier distribution in the channel **40***d* of the TEG of **FIGS. 20A and 20B** using an STM.

[**0238**] As described previously, in the present embodiment, the channel is less prone to being damaged when the gate electrode **44***c* is etched and removed. The carrier distribution shown in **FIG. 21** is expected to be almost the same distribution as that in the MOS transistor provided for actual use.

[**0239**] In the present embodiment as described above, it may also be considered that plasma etching is adopted for the removal of the gate electrode **44***c*. However, in plasma etching, as the etching proceeds, more damage occurs in the channel **40***d* through the gate insulating film **43** due to the kinetic energy of ions in an etching atmosphere. Accordingly, the carrier distribution fluctuates, and the performance of the MOS transistor cannot be accurately evaluated, unlike the present embodiment.

[**0240**] Moreover, the MOS transistor to be evaluated in the present embodiment is not limited to a type in which stress is applied to the channel by forming source/drain material layers, such as SiGe layers, in the first and second recesses **40***a* and **40***b*. For example, a MOS transistor of a general type in which recesses do not exist in actual use can be an object of evaluation. However, in a TEG for a MOS transistor of this type, the portion of the silicon substrate **40** having no element isolation insulating film **41** therein is also etched when the gate electrode **44***c* is etched in the step of **FIG. 18D**. Accordingly, the recesses **40***a* and **40***b* are formed in these portions.

(11) Eleventh Embodiment

[**0241**] Next, a method of evaluating a semiconductor device according to an eleventh embodiment of the present invention will be described.

[**0242**] **FIG. 22** is a cross-sectional view of a TEG used in the present embodiment.

[**0243**] In the tenth embodiment, the channel **40***d* has been observed using an STM, which is a kind of probe microscope. On the other hand, in the present embodiment, the channel **40***d* is observed using a scanning capacitance microscope.

[**0244**] In the scanning capacitance microscopy, a probe of the microscope and the channel **40***d* constitute a capacitor, and the capacitance value of the capacitor is detected, whereby an impurity distribution in the channel **40***d* is observed. In the present embodiment, in order to form a dielectric layer of the capacitor, a silicon dioxide layer (dielectric layer) **51** having a thickness of approximately 1.0 nm as shown in **FIG. 22** is formed on the surface of the silicon substrate **40** by applying ozone to the surface of the channel **40***d*.

[**0245**] Thereafter, as shown in **FIG. 23**, the silicon dioxide layer **51** is scanned by the probe **52** with the tip of the probe **52** of the scanning capacitance microscope brought into contact with the surface of the silicon dioxide layer **51**, thereby obtaining the carrier distribution in the channel **40***d* through the silicon dioxide layer **51**.

[**0246**] In the case where the channel **40***d* is observed using a scanning capacitance microscope as described above, the removal of the gate electrode **44***c* by wet etching using a TMAH solution similarly to the tenth embodiment makes it possible to prevent damage to the silicon substrate **40** and to measure almost the same carrier distribution as that in the MOS transistor provided for actual use.

[**0247**] Note that, though a scanning capacitance microscope has been used in the above, use of a scanning spreading resistance microscope instead can also provide the same advantages as those of the present embodiment.

[**0248**] In the semiconductor device according to the present invention, a crystal plane of a semiconductor substrate constitutes a side surface of each of holes in which source/drain material layers are respectively formed. Accordingly, stress applied to a channel from the source/drain material layers can be prevented from varying among elements, and the reliability of the semiconductor device can be improved.

[**0249**] Moreover, in the method of manufacturing a semiconductor device according to the present invention, holes are formed in a silicon substrate beside the gate electrode by

wet etching using an organic alkaline solution or a TMAH solution as an etchant. Accordingly, a crystal plane of the semiconductor substrate is exposed at each etched surface, and the crystal plane constitutes a side surface of each hole. Thus, excellent reproducibility comes to be shown, and stress is applied to the channel from the source/drain material layers, which are formed in the holes, without variation among elements even in the case where MOS transistors are integrally formed in the semiconductor substrate.

[0250] Furthermore, in the method of evaluating a semiconductor device according to the present invention, since a gate electrode is removed by etching using an organic alkaline solution or a TMAH solution, damage does not easily occur in a channel in etching, and a carrier distribution in the channel is not easily disturbed. Accordingly, a carrier distribution in a state similar to that of actual use can be obtained.

What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate;

a gate insulating film and a gate electrode which are formed on the semiconductor substrate in this order; and

a source/drain material layer formed in a hole in the semiconductor substrate, the hole being located beside the gate electrode,

wherein a side surface of the hole which is closer to the gate electrode includes at least one crystal plane of the semiconductor substrate.

2. The semiconductor device according to claim 1, wherein the side surface of the hole includes two crystal planes, and a cross-sectional shape of the side surface is concave.

3. The semiconductor device according to claim 1, wherein the side surface of the hole includes two crystal planes, and a cross-sectional shape of the side surface is convex.

4. The semiconductor device according to claim 3, wherein a buried insulating layer is formed under the hole in the semiconductor substrate.

5. The semiconductor device according to claim 1, wherein the side surface of the hole includes a single crystal plane perpendicular to the semiconductor substrate.

6. The semiconductor device according to claim 5, wherein the semiconductor substrate is a silicon substrate, a surface orientation of the silicon substrate is (110), and a gate width direction of the gate electrode is a [111] direction of the silicon substrate.

7. The semiconductor device according to claim 1, wherein the semiconductor substrate is a silicon substrate, and the side surface of the hole includes a (111) plane of the silicon substrate.

8. The semiconductor device according to claim 7, wherein a surface orientation of the silicon substrate is (001).

9. The semiconductor device according to claim 7, wherein a surface orientation of the silicon substrate is (110), and a gate width direction of the gate electrode is a [100] direction of the silicon substrate.

10. The semiconductor device according to claim 1, wherein a sidewall is formed on a side surface of the gate electrode, and an upper end portion of the hole goes under the sidewall and is brought closer to a channel under the gate electrode.

11. The semiconductor device according to claim 1, wherein the entire gate electrode is made of silicide of refractory metal.

12. The semiconductor device according to claim 1, wherein the source/drain material layer is a SiGe layer.

13. The semiconductor device according to claim 1, wherein the source/drain material layer is a metal layer.

14. A method of manufacturing a semiconductor device, comprising the steps of:

forming a gate insulating film on a semiconductor substrate;

forming a gate electrode on the gate insulating film;

forming a sidewall on a side surface of the gate electrode;

forming a hole in the semiconductor substrate beside the gate electrode using any one of an organic alkaline solution and a tetramethylammonium hydroxide (TMAH) solution as an etchant, after forming the sidewall; and

forming a source/drain material layer in the hole.

15. The method according to claim 14,

wherein in the step of forming the hole, a thickness of the gate electrode is reduced by the etchant, and

the method further comprises, after the step of forming the hole, the steps of:

forming a refractory metal layer on the source/drain material layer and the gate electrode; and

causing a reaction between the refractory metal layer and the gate electrode by heating the refractory metal layer and siliciding the entire gate electrode.

16. The method according to claim 15, further comprising, before the step of forming the hole, the step of introducing p-type impurities into the gate electrode.

17. The method according to claim 14, further comprising, before the step of forming the hole, the steps of:

forming a first conductivity type impurity diffusion region in the silicon substrate; and

forming a second conductivity type impurity diffusion region in the silicon substrate more deeply than the first conductivity type impurity diffusion region,

wherein, in the step of forming the hole, the hole is formed more deeply than the first conductivity type impurity diffusion region.

18. The method according to claim 17,

wherein, in the step of forming the first conductivity type impurity diffusion region, impurities of a first conductivity type are introduced into the silicon substrate using the gate electrode as a mask to form a source/drain extension, and the source/drain extension is used as the first conductivity type impurity diffusion region, and

in the step of forming the second conductivity type impurity diffusion region, impurities of a second conductivity type are introduced into the silicon substrate using the gate electrode and the sidewall as a mask.

19. The method according to claim 18,

wherein the step of forming the sidewall includes the steps of: forming a first sidewall on a side surface of the gate electrode; and forming a second sidewall on a side surface of the first sidewall, and

the method further comprises, after the step of forming the first sidewall, the step of forming a source/drain region by introducing impurities of the first conductivity type into the silicon substrate using the first sidewall as a mask.

20. The method according to claim 17, wherein a p-type impurity diffusion region is formed as the first conductivity type impurity diffusion region, and an n-type impurity diffusion region is formed as the second conductivity type impurity diffusion region.

21. The method according to claim 17, wherein a p-type impurity diffusion region is formed as the first conductivity type impurity diffusion region, and a p-type impurity diffusion region having a higher impurity concentration than that in the first conductivity type impurity diffusion region is formed as the second conductivity type impurity diffusion region.

22. The method according to claim 21, wherein any one of a source/drain extension and a source/drain region is formed as the first conductivity type impurity diffusion region.

23. The method according to claim 14, wherein an SOI substrate is used as the semiconductor substrate.

24. The method according to claim 14, wherein a silicon substrate is used as the semiconductor substrate.

25. The method according to claim 24, wherein a substrate with (001) surface orientation is used as the silicon substrate.

26. The method according to claim 24,

wherein a substrate with (110) surface orientation is used as the silicon substrate, and

in the step of forming the gate electrode, the gate electrode is formed with a gate width direction being set to a [111] direction.

27. The method according to claim 24,

wherein a substrate with (110) surface orientation is used as the silicon substrate, and

in the step of forming the gate electrode, the gate electrode is formed with a gate width direction being set to a [100] direction.

28. The method according to claim 14, wherein a length by which an upper end portion of the hole goes under the sidewall is controlled by adjusting a substrate temperature when the sidewall is formed.

29. The method according to claim 14, wherein a mixed solution of an ammonium hydroxide solution and isopropyl alcohol (IPA) is used as the organic alkaline solution.

30. The method according to claim 14, wherein a SiGe layer is epitaxially grown as the source/drain material layer.

31. The method according to claim 14, wherein a metal layer is formed as the source/drain material layer.

32. A method of evaluating a semiconductor device, comprising the steps of:

removing a gate electrode of a MOS transistor, which is formed over a semiconductor substrate, by selective etching using any one of an organic alkaline solution and a TMAH solution as an etchant;

exposing a channel of the MOS transistor by removing a gate insulating film of the MOS transistor by wet etching; and

investigating a carrier distribution in the exposed channel using a microscope.

33. The method according to claim 32,

wherein in the step of exposing the channel, the gate insulating film is removed using an etchant containing hydrofluoric acid, and

in the step of investigating the carrier distribution, a probe microscope is used as the microscope.

34. The method according to claim 32, further comprising the step of forming a dielectric layer on the exposed channel,

wherein in the step of investigating the impurity distribution, any one of a scanning capacitance microscope and a scanning spreading resistance microscope is used as the microscope, and the carrier distribution is investigated through the dielectric layer.

35. The method according to claim 34, wherein in the step of forming the dielectric layer, an oxide layer is formed as the dielectric layer by applying ozone to a portion of the semiconductor substrate which corresponds to the channel.

36. The method according to claim 32, wherein a silicon substrate is used as the semiconductor substrate.

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