

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNITED MICROELECTRONICS CORPORATION,
AND
UMC GROUP (USA),

Petitioner,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,

Patent Owner.

Case No. IPR2025-01090
U.S. Patent 8,907,425

**DECLARATION OF JUNE ANN MUNFORD IN SUPPORT OF PETITION
FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 28,907,425**

TABLE OF CONTENTS

	Page
I. INTRODUCTION	1
A. Qualifications and Work Experience	2
B. MARC	2
C. Scope of this Declaration	4
D. Resources Consulted and Evidence Considered	4
II. AUTHENTICITY AND PUBLIC AVAILABILITY OF JAMES	6
A. MARC Record.....	6
B. Authentication	7
III. CONCLUSION.....	7

I. INTRODUCTION

I, June Ann Munford, do hereby declare as follows:

1. I am over the age of 18, have personal knowledge of the facts set forth herein, and am competent to testify to the same.

2. I have been retained as an expert witness by Troutman Pepper Locke LLP on behalf of United Microelectronics Corporation and UMC Group (USA) (collectively “Petitioner”) for proceedings before the United States Patent and Trademark Office (“USPTO”) regarding the authenticity and public availability of certain prior art references discussed in this declaration in relation to U.S. Patent No. 8,907,425 (“the ’425 patent”).

3. I am being compensated for my work in this matter at my standard hourly rate of \$200.00 per hour and am being reimbursed for any reasonable expenses associated with my work and my testimony in this matter. My statements are objective, and my compensation does not depend on the outcome of this matter.

4. I reserve the right to supplement or amend my opinions in response to any additional evidence, testimony, discovery, argument, and/or other additional information that may be provided or that I may obtain independently after the date of this declaration.

A. Qualifications and Work Experience

5. I earned a Master of Library and Information Science (MLIS) from the University of Wisconsin-Milwaukee in 2009. I have over ten years of experience in the library/information science field. Beginning in 2004, I have served in various positions in the public library sector including Assistant Librarian, Youth Services Librarian and Library Director. I have attached my Curriculum Vitae as Appendix CV.

6. During my career in the library profession, I have been responsible for materials acquisition for multiple libraries. In that position, I have cataloged, purchased and processed incoming library works. That includes purchasing materials directly from vendors, recording publishing data from the material in question, creating detailed material records for library catalogs and physically preparing that material for circulation. In addition to my experience in acquisitions, I was also responsible for analyzing large collections of library materials, tailoring library records for optimal catalog, search performance and creating lending agreements between libraries during my time as a Library Director.

B. MARC

7. I am fully familiar with the catalog record creation process in the library sector. In preparing a material for public availability, a library catalog record describing that material would be created. These records are typically written using

Machine Readable Catalog (herein referred to as “MARC”) codes and contain information such as a physical description of the material, metadata from the material’s publisher, and date of library acquisition.

8. I am very familiar with MARC, which became the national standard for sharing bibliographic data in the United States by 1971 and the international standard by 1973. MARC is the primary communications protocol for the transfer and storage of bibliographic metadata in libraries. Experts in my field reasonably rely upon MARC records when forming their opinions.

9. A MARC record contains several fields, each identified by a standardized, unique, three-digit code corresponding to the data that follows. (See, Appendix XX, Parts VII to X of “Understanding MARC Bibliographic: Machine-Readable Cataloging” (<http://www.loc.gov/marc/umb/um07to10.html>).) For example, the author of a work is recorded in Field 100, the title/attribution is recorded in Field 245, the publisher is recorded in Figure 260, a book’s physical description is record in Field 300, and Field 008 is reserved for denoting the date of creation of the library record itself. As this typically occurs during the process of preparing materials for public access, it is my experience that an item’s MARC record indicates the date of an item’s public availability.

10. Typically, in creating a MARC record, a librarian would gather various bits of metadata such as book title, publisher and subject headings among others and

assign each value to a relevant numerical field. The 008 field of the MARC record is reserved for denoting the creation of the library record itself. As this is the only date reflecting the inclusion of said materials within the library's collection, it is my experience that an item's 008 field accurately indicates the date of an item's public availability.

C. Scope of this Declaration

11. I have been asked to offer an opinion on the authenticity and public availability date of the following document:

- D. James, "2004 – The Year of 90-nm: A Review of 90 nm Devices," 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (2005) ("James").

D. Resources Consulted and Evidence Considered

12. I am personally familiar with many online catalogs, databases, and search engines. In preparing this declaration, I used the following resources to search for records:

- Ecosia – A search engine aggregator that provides web results for search queries from several sources, including Bing and Google. This search engine is capable of advanced search queries and provides results in several multimedia formats. I used Ecosia to search for each document authenticated in this declaration to

confirm publication information such as journal title, issue number, proceedings title, year of publication, name of publisher and related international standard numbers such as ISBN and ISSN.

- Worldcat – A search engine that indexes library holdings across thousands of different library collections. This search engine is capable of advanced search queries and provides results describing the library holdings of thousands of libraries, museums and non-profits. I used Worldcat to help source library copies of each reference.
- Library Catalogs – For each library holding, I used the associated library catalog to locate MARC records and library holdings for each reference included in this declaration. The catalog referenced in this declaration is North Carolina State University. These catalogs function similarly to search engines, capable of advanced search queries and detailed results filtering.

13. In preparing this declaration, I have also reviewed the documents referenced below and any other document that I mention herein. Each of the listed documents is a type of material that experts in my field would rely upon when forming their opinions.

II. AUTHENTICITY AND PUBLIC AVAILABILITY OF JAMES

A. MARC Record

14. Attached hereto as Appendix JAMES01 is a true and correct copy of the MARC record for Proceedings of the 2005 Advanced Semiconductor Manufacturing Conference as held by the North Carolina State University Library. The MARC record contained within Appendix JAMES01 accurately describes the title, publisher and ISBN number of Proceedings of the 2005 Advanced Semiconductor Manufacturing Conference. The 245 field present on page 1 represents the record's title, in this case "ASMC 2005 Proceedings: Advancing Semiconductor Manufacturing Excellence". The 264 field present on page 1 represents the book's publisher, in this case 'IEEE'. The 020 field present on page 1 represents the book's ISBN number, in this case '0780389964'.

15. The 008 field of the MARC record in Appendix JAMES01 indicates the date of record creation. The 008 field of Appendix JAMES01 indicates the North Carolina State University Library first acquired Proceedings of the 2005 Advanced Semiconductor Manufacturing Conference as of July 15, 2005. Considering this information, it is my determination that Proceedings of the 2005 Advanced Semiconductor Manufacturing Conference and therefore "2004 – The Year of 90-nm: A Review of 90 nm Devices" by D. James was made available to the public

shortly after its initial publication shortly after July 15, 2005 if not earlier via the conference.

B. Authentication

16. Attached hereto as Appendix JAMES02 is a true and correct copy of “2004 – The Year of 90-nm: A Review of 90 nm Devices” by D. James as published in Proceedings of the 2005 Advanced Semiconductor Manufacturing Conference. These scans were secured from the collection of the North Carolina State University.

17. The document submitted as 1012-c in the inter partes review of the ‘425 patent is the same as the copy of James provided as Appendix JAMES02. In comparing 1012-c to Appendix JAMES02, it is my determination that 1012-c is a true and correct copy of “2004 – The Year of 90-nm: A Review of 90 nm Devices” by D. James as published in Proceedings of the 2005 Advanced Semiconductor Manufacturing Conference.

III. CONCLUSION

18. In signing this Declaration, I understand it will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I understand I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

19. I declare that all statements made herein of my knowledge are true, that all statements made on information and believe are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on June 2, 2025 in Pittsburgh, Pennsylvania.

Respectfully submitted,

Signed by:

69C46E8864684FD
June Ann Munford

APPENDIX CV

June A. Munford
Curriculum Vitae

Education

University of Wisconsin-Milwaukee - MS, Library & Information Science, 2009
Milwaukee, WI

- Coursework included cataloging, metadata, data analysis, library systems, management strategies and collection development.
- Specialized in library advocacy, cataloging and public administration.

Grand Valley State University - BA, English Language & Literature, 2008
Allendale, MI

- Coursework included linguistics, documentation and literary analysis.
- Minor in political science with a focus in local-level economics and government.

Professional Experience

Researcher / Expert Witness, October 2017 – present
Freelance ● Pittsburgh, Pennsylvania & Grand Rapids, Michigan

- Material authentication and public accessibility determination. Declarations of authenticity and/or public accessibility provided upon research completion. Experienced with appeals and deposition process.
- Research provided on topics of public library operations, material publication history, digital database services and legacy web resources.
- Past clients include Alston & Bird, Arnold & Porter, Baker Botts, Fish & Richardson, Erise IP, Irell & Manella, O'Melveny & Myers, Perkins-Coie, Pillsbury Winthrop Shaw Pittman and Slayden Grubert Beard.

Library Director, February 2013 - March 2015
Dowagiac District Library ● Dowagiac, Michigan

- Executive administrator of the Dowagiac District Library. Located in Southwest Michigan, this library has a service area of 13,000, an annual operating budget of over \$400,000 and total assets of approximately \$1,300,000.

- Developed careful budgeting guidelines to produce a 15% surplus during the 2013-2014 & 2014-2015 fiscal years while being audited.
- Using this budget surplus, oversaw significant library investments including the purchase of property for a future building site, demolition of existing buildings and building renovation projects on the current facility.
- Led the organization and digitization of the library's archival records.
- Served as the public representative for the library, developing business relationships with local school, museum and tribal government entities.
- Developed an objective-based analysis system for measuring library services - including a full collection analysis of the library's 50,000+ circulating items and their records.

November 2010 - January 2013

Librarian & Branch Manager, Anchorage Public Library ● Anchorage, Alaska

- Headed the 2013 Anchorage Reads community reading campaign including event planning, staging public performances and creating marketing materials for mass distribution.
- Co-led the social media department of the library's marketing team, drafting social media guidelines, creating original content and instituting long-term planning via content calendars.
- Developed business relationships with The Boys & Girls Club, Anchorage School District and the US Army to establish summer reading programs for children.

June 2004 - September 2005, September 2006 - October 2013

Library Assistant, Hart Area Public Library

Hart, MI

- Responsible for verifying imported MARC records and original MARC cataloging for the local-level collection as well as the Michigan Electronic Library.
- Handled OCLC Worldcat interlibrary loan requests & fulfillment via ongoing communication with lending libraries.

Professional Involvement

Alaska Library Association - Anchorage Chapter

- Treasurer, 2012

Library Of Michigan

- Level VII Certification, 2008
- Level II Certification, 2013

Michigan Library Association Annual Conference 2014

- New Directors Conference Panel Member

Southwest Michigan Library Cooperative

- Represented the Dowagiac District Library, 2013-2015

Professional Development

Library Of Michigan Beginning Workshop, May 2008

Petoskey, MI

- Received training in cataloging, local history, collection management, children's literacy and reference service.

Public Library Association Intensive Library Management Training, October 2011

Nashville, TN

- Attended a five-day workshop focused on strategic planning, staff management, statistical analysis, collections and cataloging theory.

Alaska Library Association Annual Conference 2012 - Fairbanks, February 2012

Fairbanks, AK

- Attended seminars on EBSCO advanced search methods, budgeting, cataloging, database usage and marketing.

Depositions

2019 ● Fish & Richardson

Apple v. Qualcomm (Case No. IPR2018-001281, 39521-00421IP, IPR2018-01282 and 39521-00421IP2)

2019 ● Erise IP

Implicit, LLC v. Netscout Systems, Inc (Case No. 2:18-cv-53-JRG)

2019 ● Perkins-Coie

Adobe Inc. v. RAH Color Technologies LLC (Case No. IPR2019-00627, IPR2019-00628, IPR2019-00629 and IPR2019-00646)

2020 ● O'Melveny & Myers

Maxell, Ltd. v. Apple Inc. (Case No. 5:19-cv-00036-RWS)

2021 ● Pillsbury Winthrop Shaw Pittman LLP

Intel v. SRC (Case No. IPR2020-1449)

2022 ● Perkins-Coie

Realtek v. Future Link (Case No. IPR2021-01182)

2023 ● Fish & Richardson

Neuroderm Ltd. v. Abbvie, Inc (Case No. PGR2022-00040)

2023 ● Fish & Richardson

Nearmap US Inc. v. Pictometry International Corp. (Case No. IPR2022-00735)

2023 ● Fish & Richardson

Samsung Electronics v. MemoryWeb LLC (Case No. 39843-0136PS1)

2023 ● Pillsbury Winthrop Shaw Whitman LLP

Gravel Rating Systems v. Costco Wholesale Corp. (Case No. 4:21-cv-149-ALM)

2024 ● Willkie-Farr

Netflix, Inc. v. VideoLabs. Inc. (Case No. IPR2023-00628)

2024 ● Quinn Emanuel Urquhart & Sullivan

Purdue University v. Wolfsped (Case No. 1:21-CV-840)

2024 ● Fish & Richardson

Dish Network v. Entropic Communications (Case No. IPR2024-00393)

2025 ● Perkins Coie

Amazon.com, Inc. v. Nokia Technologies Oy (Case No. IPR2024-00572)

2025 ● Fish & Richardson

Dish Network v. Entropic Communications (Case No. IPR2024-00373)

Limited Case and Clientele History

Alston & Bird

- Ericsson

v. Collision Communications (Case No. IPR2022-01233)

- Nokia

v. Neptune Subsea, Xtera (Case No. 1:17-cv-01876)

- Universal Electronics Inc

v. Roku Inc (Case No. IPR2022-00818)

Alavi & Anaipakos PLLC

- Stingray Group Inc. and Stingray Music USA, Inc.

v. Edwin A. Hernandez-Mondragon and Eglia Corp. (Case No. 1:24-cv-21226-RAR)

Arnold & Porter

- Ivantis

v. Glaukos (Case No. 8:18-cv-00620)

- Samsung

v. Jawbone (Case No. 2:21-cv-00186)

Benesch Friedlander Coplan & Aronoff

- Voyis
v. Cathx (Case No. 5:21-cv-00077-RWS)

Buchanan, Ingersoll & Rooney PC

- Google LLC, AT&T Service Inc., T Mobile USA Inc., Cellco Partnership, Ericsson Inc. & Nokia of America Corp.
v. KT Corp & Pegasus Wireless Innovation LLC (Case No. IPR2025-00293)

Deschert LLP

- Smaxtec Animal Care
v. ST Reproductive Technologies, LLC (Case No. IPR2024-00885)

Duane Morris

- Kangxi Communication Technologies
v. Skyworks Solutions Inc. (Case No. IPR2025-00373)
- Microsoft
v. Edge Networking Systems LLC (Case No. 1:24-cv-00215)

Erise I.P.

- Apple
v. Ericsson Inc. (Case No. IPR2022-00715)
v. Future Link Systems (Case No. IPRs 6317804, 6622108, 6807505, and 7917680)
v. INVT (Case No. 20-1881)
v. Navblazer LLC (Case No. IPR2020-01253)
v. Qualcomm (Case No. IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)

- v. Quest Nettech Corp (Case No. 2:19-cv-00118-JRG)
- v. Telefonaktiebolaget LM Ericsson (Case No. IPR2022-00275)
- v. Theta IP, LLC (Case No. IPR2024-00818)
- v. THL Holding Company LLC (Case No. 1:23-cv-00548)

- Fanduel

- v. CGT (Case No. 19-1393)

- Garmin

- v. Phillips North America LLC (Case No. 2:19-cv-6301-AB-KS)

- Netscout

- v. Longhorn HD LLC (Case No. 2:20-cv-00349)
- v. Implicit, LLC (Case No. 2:18-cv-53-JRG)

- Sony Interactive Entertainment LLC

- v. Bot M8 LLC (Case No. IPR2020-01288)
- v. Infernal Technology LLC (Case No. 2:19-CV-00248-JRG)

- Tesla

- v. Charge Fusion Technologies LLC (Case No. IPR2025-00032)

- Unified Patents

- v. GE Video Compression (Case No. 2:19-cv-248)

Fish & Richardson

- Apple

- v. AliveCor (Case No. 3:21-cv-03958)
- v. LBS Innovations (Case No. 2:19-cv-00119-JRG-RSP)
- v. Koss Corporation (Case No. IPR2021-00305)

v. Masimo (Case No. IPR 50095-0012IP1, 50095-0012IP2, 50095-0013IP1, 50095-0013IP2, 50095-0006IP1, 50095-0135IP1)

v. Neonode (Case No. 21-cv-08872-EMC)

v. Qualcomm (Case No. IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)

v. Resonant Sys. (Case No. 7:23-cv-00077-ADA)

- AsusTek Computer Inc.

v. Videolabs, Inc. (Case No. 22-CV-00720-ADA)

- Dell

v. Neo Wireless (Case No. IPR2022-00616)

- Dish Network

v. Entropic Communications, LLC (Case No. 2:2023-CV-01043)

v. Entropic Communications LLC (Case No. IPR2024-00393)

v. Realtime Adaptive Streaming (Case No. 1:17-CV-02097-RBJ)

v. TQ Delta LLC (Case No. 18-1798)

- Evapco Dry Cooling

v. SPG Dry Cooling (Case No. IPR2021-00688)

- Genetec

v. Sensormatic Electronics (Case No. 1:20-CV-00760)

- Huawei

v. Bell Northern Research LLC (Case No. IPR2019-01174)

- Kianxis

v. Blue Yonder (Case No. 3:20-cv-03636)

- LG Electronics
 - v. Bell Northern Research LLC (Case No. 3:18-cv-2864-CAB-BLM)
- MediaTek
 - v. MOSAID (Case No. IPR2024-00718)
- Metaswitch
 - v. Sonus Networks (Case No. IPR2018-01719)
- Microsoft
 - v. Throughputer Inc (Case No. IPR2022-00757)
- Mom Enterprises
 - v. Ddrops Company (Case No. 1:22-cv-00332)
- MLC Intellectual Property
 - v. MicronTech (Case No. 3:14-cv-03657-SI)
- Nearmap Inc
 - v. EagleView Technologies (Case No. IPR2022-01009)
- Neuroderm Ltd.
 - v. Abbvie, Inc (Case No. PGR2022-00040)
- Posco Co Ltd.
 - v. Pascal Drillet et al. (Case No. IPR2025-00370)
- Realtek Semiconductor
 - v. Future Link (Case No. IPR2021-01182)

- Quectel
 - v. Koninklijke Philips (Case No. 1:20-cv-01710)
- Samsung
 - v. Aire Technology (Case No. IPR2022-00877)
 - v. Bell Northern Research (Case No. 2:19-cv-00286-JRG)
 - v. Communication Technologies Inc (Case No. IPR2022-01221)
 - v. Jawbone Innovations (Case No. IPR2022-00865)
 - v. MemoryWeb LLC (Case No. IPR2022-00885)
 - v. Dodots Licensing Solutions (Case No. IPR2023-00701)
 - v. Telefonaktiebolaget LM Ericsson (Case No. IPR2021-00615)
- Texas Instruments
 - v. Vantage Micro LLC (Case No. IPR2020-01261)
- Xilinx
 - v. Sentient Sensors LCC (Case No. 1:22-cv-00173)

Goodwin Proctor

- Intel
 - v. Proxense, LLC (Case No. 6:24-cv-00283)
- Samsung Electronics
 - v. Mobile Data Technologies (Case No. 2:24-cv-00435)
- Taiwan Semiconductor Manufacturing Company Ltd.
 - v. Advanced Integrated Circuit Process LLC (Case No. 2:24-cv-00623)

Groombridge Wu

- Nearmap

v. Eagle View Technologies Inc. and Pictometry International Corp. (Case No. 2:21-cv-00283-TS-DAO)

Irell & Manella

- Curium

Latham & Watkins LLP

- Apple

v. Advanced Coding Research LLC

Leydig, Voit & Mayer, Ltd.

- Public Availability Consultancy

O'Melveny & Myers

- Apple

v. Maxell (Case No. 5:19-cv-00036-RWS)

- Disney Media & Entertainment Distribution LLC

v. Digital Media Technology Holdings, LLC (Case No. 2:22-cv-01642)

- Micron Technology Inc.

v. Besang Inc (Case No. IPR2023-00900)

- Samsung

v. Daedalus Prime LLC (1335 Investigation)

Perkins-Coie

- Amazon
 - v. Nokia (Case No. IPR2024-00847 and IPR2024-00848)
 - v. Nokia Technologies Oy (Case No. IPR2024-00572)
- Heru Industries
 - v. The UAB Research Foundation (Case No. IPR2022-01148)
- Intel Corporation
 - v. BeSang Inc. (Case No. IPR2023-00991)
 - v. BitMICRO (Case No. 5:23-cv-00625)
 - v. Telefonaktiebolaget L M Ericsson (Case No. IPR2024-00610)
- Realtek Semiconductor
 - v. Future Link (Case No. IPR2021-01182)
- r-pac
 - v. Adasa, Inc. (Case No. 1:2024cv06102)
- Twitter Inc
 - v. VOIP-Pal.com (Case No. 3:20-cv-02397-JD)
- TCL Industries
 - v. Koninklijke Philips NV (Case No. IPR2021-00495, IPR2021-00496 and IPR2021-00497)
- VusionGroup
 - v. Hanshow (Case No. IPR2024-00857)

Pillsbury Winthrop Shaw Pittman

- Intel

v. FG SRC LLC (Case No. 6:20-cv-00315)

- Gravel Rating Systems

v. Costco (Case No. 4:21-cv-149)

v. Lowe's Home Centers (Case No. 4:21-cv-150)

v. T-Mobile USA (Case No. 4:21-cv-152)

v. Kohl's Inc. (Case No. 4:21-cv-258)

v. Under Armor (Case No. 4:21-cv-356)

Quinn Emanuel

- Exact Sciences Corporation

v. Geneoscopy, Inc. (Case No. IPR2024-00459 and IPR2024-1330)

- ServiceNow, Inc.

v. InQusient, Inc. (Case No. 22-900-CJB)

- Wolfsped

v. The Trustees of Purdue University (Case No. 1:2021-cv-00840)

Sheppard, Mullin, Richter & Hampton LLP

- Advanced Micro Devices, Inc and Pensando Systems, Inc.

v. Concurrent Ventures LLC and Xtreamedge, Inc. (Case No. IPR2025-00478)

- Cadence Design Systems Inc.

v. Semiconductor Design Technologies (Case No. 3:23-cv-01001)

Shook, Hardy & Bacon LLP

- HP Inc.

v. Universal Connectivity Technologies (Case No. 1:23-cv-01177)

Stern, Kessler, Goldstein & Fox

- Preliminary Research

Wilmer, Cutler, Pickering, Hale and Dorr

- Apple

v. Shunock (Case No. 1:23-cv-08598)

- Quest Diagnostics Inc., Haystack Oncology Inc. and Haystack Oncology GmbH

v. Natera, Inc. (Case No. 1:23-cv-08598)

- Roche Diabetes, Inc.

v. Trividia Health, Inc. (Case No. 1:24-cv-00668)

Willkie, Farr & Gallagher LLP

- Lenovo, Dell, HP

v. Universal Connectivity Technologies Inc. (Case No. 2:2023cv00449)

- Neurent

v. The Foundry, LLC (Case No. IPR2024-00669)

- Netflix, Inc.

v. VideoLabs, Inc. (Case No. IPR2023-00628)

APPENDIX JAMES01

- 000 10022cam a2200541Ia 4500
 003 OCoLC
 005 20050721124512.0
 008 050715t20052005nyua b 101 0 eng d
 020 |a0780389964
 035 |a(OCoLC)60939757
 040 |aCLU|beng|cCLU|dOrLoB-B
 049 |xtmc
 090 |aTK7871.85|b.I25 2005 e-book
 111 2 |aIEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop|d(2005 :|cMunich, Germany)
 245 10 |aASMC 2005 proceedings :|badvancing semiconductor manufacturing excellence /|c2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop, 11-12 April, 2005, Munich, Germany.
 246 30 |aAdvancing semiconductor manufacturing excellence
 246 14 |a2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop (ASMC)
 264 1 |a[New York] :|bIEEE ;|aPiscataway, N.J. :|bIEEE Operations Center,|c[2005]
 264 4 |c@2005
 300 |aviii, 282 pages :|billustrations ;|c28 cm
 336 |atext|btxt|2rdacontent
 337 |aunmediated|bn|2rdamedia
 338 |avolume|bnc|2rdacarrier
 500 |a"IEEE Catalog Number 05CH37654"--T.p. verso.
 504 |aIncludes bibliographical references and author index.
 505 00 |tNon-damaging chemical photoresist strip process for Copper/low-k interconnects /|rPhilip G. Clark and Kurt K. Christenson -- |tPolishing of bulk micro-machined substrates by fixed abrasive pads for smoothing and planarization of MEMS structures /|rMartin Kulawski, Hannu Luoto, Kimmo Henttinen, Tommi Suni, Frauke Welmar and Jari Makinen -- |tAdvanced cryogenic aerosol cleaning : application to damage free cleaning sensitive structured wafers /|rJeff Lauerhaas, James F. Weygand and Greg P. Thomes -- |tEtch chamber condition-based process control model for shallow trench isolation trench depth control /|rSreedhar Gaddam and Martin W. Braun --
 505 80 |tNew optical range inspection and improving optical response for spectroscopic-based endpoint detection /|rGiuseppe Fazio, Pietro Petruzza and Alessandro Spandra -- |tAdaptive sampling methodology for in-line defect inspection /|rAli Bousetta and Andrew J. Cross -- |tImpact of back side defects on FEOL processes and yield /|rLaura Pressley, Shirley Hardin, Kevin Harper, Brian Dunham, Dan Sutton Travis Kirsch, Mike Allen Buster Klingemann, Teresa Mathews, Laurence Kohler, Chris Lansford, Terri Couteau, Bryon Hance, John Darilek, Carolyn Cariss, Eric Apeltgren, Rhonda Stanley, Joyce Witowski and Lisa Cheung --
 505 80 |tEffective wafer inspection strategy for memory manufacturing foundries with inspiring HARI results /|rLuke Lin, Feng-Ming Kuo and Terry Chen -- |tInline automated defect classification : a novel approach to defect management /|rDavid Pepper, Olivier Moreau and Guillaume Hennion -- |tEdge and bevel automated defect inspection for 300mm production wafers in manufacturing /|rJaime Morillo, Thomas Houghton, Joseph M. Bauer, Randy Smith and Randy Shay -- |tExposure tool for immersion lithography /|rSolchi Owa, Yuuki Ishii and Kenichi Shiraishi -- |tExploring the capabilities of immersion lithography /|rChris Mack and Jeffrey Byers --
 505 80 |tProcess-window sensitive full-chip inspection for design-to-silicon optimization in the sub wavelength era /|rMaryJane Brodsky, Scott Halle, Vickie Jophlin-Gut, Lars Liebmann, Don Samuels, Gary Crispo, Kourosh Nafisi, Vijay Ramani and Ingrid Peterson -- |t2004 -the year of 90-nm : a review of 90 nm devices /|rDick James -- |tNext generation manufacturing execution system [MES] enabling fully integrated fab automation in 300mm technology development and manufacturing /|rChandra Mouli -- |tInterface a prototyping experiences - paving the way to e-manufacturing /|rHarvey Wohlwend and Steve Fulton --
 505 80 |tSingle wafer management systems and bare wafer storage as key to increased yield and productivity /|rHeinz Ritzmann -- |tA progressive strategy to achieving automated lot processing /|rMurali Krishna, Meena Baker, Ross Giddings and Chris Hunter -- |tAn advanced methodology for the reporting of original adders for process tool defect monitoring /|rTimothy Zazado and Jeffrey R. Bottin -- |tThe case for a near real-time production scheduling in a highly automated semiconductor manufacturing environment /|rNirmal Govind and Bala Iyer -- |tChamber cleaning process selection for the installed-base CVD tools /|rFranco Blundo, Manfredi Alberghina, Marcello Frazzica, Gary Loh and Michael Mocella --

- 505 80 |tComparison of three different methods to model the semiconductor manufacturing yield /|rYoan Dupret, Erwan Perrin, Jean-Luc Groller and Richard Kielbasa -- |tE-beam inspection of SO1 wafers for the evaluation of barrier nitride RIE etching /|rAlexander Ache, Nicole Rowand and Kevin Wu -- |tEffects of wafer bow and warp on performance of electrostatic chucks in high volume manufacturing /|rPiotr Kurkowski, Sergei Drizlikh, Roger Sawyer, Heath Angis and Patrick Loisel -- |tEmbodiment of compact and high performance HVIC process /|rC. K. Jeon, L. Kim, M. H. Kim, T. H. Kwon and J. J. Kim -- |tEQ integrated process trending with TFM monitoring for back end equipment /|rThomas Rathgeber and Norbert Haueis --
- 505 80 |tFault detection in reactive ion etching systems using one-class support vector machines /|rTommas Sarmiento, Gary S. May and Sang J. Hong -- |tImprovement of film uniformity stability of PECVD silicon nitride deposition process by addition of fluorine removal to the plasma clean sequence /|rAilian Zhao, Joseph Bulger, Marc French, Leslie Green, William C. Harris, Timothy J. Hunt, Holly Lisy, William Marchesseault and Richard Shuman -- |tLow-yield wafer analysis strategies /|rBrian Dunham, Travis D. Kirsch, Stuart Litwin, Michael Covert, Daniel Garcia, Alex Bierwag and Kendall Holt -- |tMoisture effects on purifier/chemical filter materials /|rDaniel Alvarez, Joseph Rotter and Troy Scoggins --
- 505 80 |tReducing defectivity in 90nm BEOL metal CMP using a geometry-based segmented inspection strategy /|rAndrew Stamper and Wee Teck Chia -- |tA reticle quality management strategy in wafer fabs addressing progressive mask defect growth problem at low k-1 lithography /|rKaustuve Bhattacharyya, Mark Eickhoff, Michael Long, Mark Ma and Sylvia Pas -- |tScanner influences on resolution capabilities /|rHolly Magoon -- |tSilicon carbide : barriers to manufacturable devices /|rJoseph Shovlin, Richard Woodin, Tony Witt, Gary Dolny and Praveen Shenoy -- |tSPC based in-line reticle monitoring on product wafers /|rKarsten Mai and Martin Tuckermann --
- 505 80 |tThoughts on an automation concept for complex production process within a learning organization /|rGerhard Luhn, Walter Reithofer, Hans-Joachim Schmidt, Martin Peiter, Frank Boelstler and Thomas Lang -- |tUltra short pulse laser meeting the requirements for high speed and high quality dicing of low-k wafers /|rJan Sillanpaa, Jarno Kangastupa, Arto Salokatve and Harry Asonem -- |tUsing TCAD for fast analysis of misprocessed wafers and yield excursions /|rRainer Minixhofer and Dieter Rathei -- |tA novel high speed and high voltage complimentary bipolar process using 1st base-poly silicon collector and SO1 technique /|rJ. H. Kim, S. H. Lee, H. J. Park, M. H. Choi, Dale Wedel and J. J. Kim --
- 505 80 |tIntegration of nickel silicide : minimizing defect generation during formation /|rJohn Foggia and Woo Sik Yoo -- |tCritical challenges in packaging MEMS devices /|rRobert Daweaux and Lakshmi Munukutla -- |tUse of surface sensitive analysis techniques for the study of silicide process in power transistors : platinum silicide formation as an example /|rDaniel Kraft, Paul Gantzer, Philip Kohler-Redlich and Uwe Schelthauer -- |tStretching factory performance beyond world class, an organizational approach /|rScott Lantz -- |tOperations and product development : integrating methodologies for improved product success /|rThomas Carbone --
- 505 80 |tHybrid manufacturing - lower cost access to DSM technology /|rBrett Williams and Mark Nelson -- |tExploring new design architectures to reach time-to-market goals /|rAki Fujimori and Ketan Joshi -- |tMeasurement and reduction of critical area using Voronoi diagrams /|rDaniel Maynard -- |tYield enhancement through fast statistical scan test analysis for digital logic /|rHans Peter Erb, Christian Burmer and Andreas Leininger -- |tMOS transistor mismatch modeling for high voltage CMOS processes /|rWerner Posch, Gerhard Rappitsch and Georg Leonardelli -- |tYield management practice by user designable YMS /|rMasayuki Inokuchi --
- 505 80 |tEnabling remote operations and cycle time reduction via automated lot-equipment assignments /|rBala Iyer, Joseph J. Concelman, Thomas Jefferson, Robert A. Madson and Jason M. Trujillo -- |tIntegration of lot dispatching and AMHS control in a 300mm wafer FAB /|rDong-Seok Sun, No-Sik Park, Young-Joong Lee, Young-Chul Jang, Chung-Sam Ahn and Tae-Eog Lee -- |tA systems approach to evaluating the impact of technician training /|rBob Simington -- |tLot identification, lot location and information distribution using radio frequency and ultrasonic signals /|rHanspeter Fischer, Ralf Schrodell, Stefan Eisen and Markus Dierkes.
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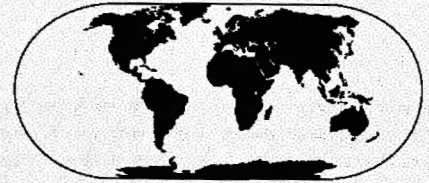
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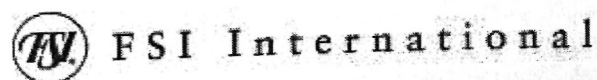
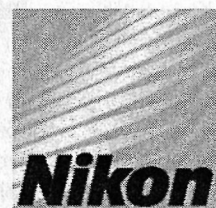


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TABLE OF CONTENTS

Sponsors and Committee

Session I -Advanced Processing I - sponsored by FSI International, Inc.

1.1a "Non-Damaging Chemical Photoresist Strip Process for CopperLow-k Interconnects"	1
Philip G. Clark and Kurt K. Christenson, FSI International, Inc.	
1.2a "Polishing of Bulk Micro-Machined Substrates by Fixed Abrasive Pads for Smoothing and Planarization of MEMS Structures"	5
Martin Kulawski, Hannu Luoto, Kimmo Henttinen, Tommi Suni, VTT Microelectronics; Frauke Weimar, 3M Deutschland; Jari Makinen, Okmetic Oy	
1.3a "Advanced Cryogenic Aerosol Cleaning: Application to Damage Free Cleaning Sensitive Structured Wafers"	11
Jeff Lauerhaas, James F. Weygand, Greg P. Thomes, FSI International, Inc.	
1.4a "Etch Chamber Condition-Based Process Control Model for Shallow Trench Isolation Trench Depth Control"	17
Sreedhar Gaddam and Martin W. Braun, Texas Instruments Inc.	
1.5a "New Optical Range Inspection and Improving Optical Response for Spectroscopic-based Endpoint Detection"	21
Giuseppe Fazio, Pietro Petruzza, Alessandro Spandra, STMicroelectronics	

Session 2 - Defect Inspection

2.1a "Adaptive Sampling Methodology for In-line Defect Inspection"	25
Ali Bousetta and Andrew J. Cross, KLA-Tencor Corporation	
2.2a "Impact of Back Side Defects on FEOL Processes and Yield"	32
Laura Pressley, Shirley Hardin, Kevin Harper, Brian Dunham, Dan Sutton Travis Kirsch, Mike Allen Buster Klingemann, Teresa Mathews, Laurence Kohler, Chris Lansford, Terri Couteau, Bryon Hance, John Darilek, Carolyn Carliss, Eric Apelgren, Spansion; Rhonda Stanley, Joyce Witowski, Lisa Cheung, KLA-Tencor Corporation	
2.3a "Effective Wafer Inspection Strategy for Memory Manufacturing Foundries with Inspiring HARI Results"	38
Luke Lin, Feng-Ming Kuo, Powerchip Semiconductor Manufacturing; Terry Chen, Applied Materials Inc.	
2.4a "Inline Automated Defect Classification: a Novel Approach to Defect Management"	43
David Pepper, Crolles 2 Alliance; Olivier Moreau and Guillaume Hennion, KLA-Tencor Corporation	
2.5a "Edge and Bevel Automated Defect Inspection for 300mm Production Wafers in Manufacturing"	49
Jaime Morillo, Thomas Houghton, Joseph M. Bauer, IBM Microelectronics; Randy Smith and Randy Shay, August Technology	

Session 3 - Lithography Challenges and Advances - sponsored by Nikon Precision Europe

3. 1a "Exposure Tool for Immersion Lithography"	53
Soichi Owa, Yuuki Ishii, Kenichi Shiraishi, Nikon Corporation	
3.2a "Exploring the Capabilities of Immersion Lithography"	58
Chris Mack and Jeffrey Byers KLA-Tencor Corporation	
3.3a "Process-Window Sensitive Full-Chip Inspection for Design-to-Silicon Optimization in the Sub Wavelength Era"	64
MaryJane Brodsky, Scott Halle, Vickie Jophlin-Gut, Lars Liebmann, Don Samuels, IBM Microelectronics; Gary Crispo, Kourosh Nafisi, Vijay Ramani, Ingrid Peterson, KLA-Tencor Corporation	
3.4a "2004 -The Year of 90-nm: A Review of 90 nm Devices"	72
Dick James, Chipworks, Inc.	

Session 4 - Factory Automation and Integration I

4. 1a "Next Generation Manufacturing Execution System (MES) Enabling Fully Integrated Fab Automation in 300mm Technology Development and Manufacturing"	78
Chandra Mouli, Intel Corporation	
4.2a "Interface a Prototyping Experiences - Paving the Way to e-Manufacturing"	87
Harvey Wohlwend and Steve Fulton, ISMI	

4.3a "Single Wafer Management Systems and Bare Wafer Storage as Key to Increased Yield and Productivity"	91
Heinz Ritzmann, Tec-Sem AG	
4.4a "A Progressive Strategy to Achieving Automated Lot Processing"	96
Murali Krishna, Meena Baker, Ross Giddings, Chris Hunter, Intel Corporation	
Session 5 - Poster Session - sponsored by KLA-Tencor Corporation	
5.1a "An Advanced Methodology for the Reporting of Original Adders for Process Tool Defect Monitoring"	101
Timothy Zazado, Texas Instruments; Jeffrey R. Bottin, KLA-Tencor Corporation	
5.2a "The Case for a Near Real-Time Production Scheduling in a Highly Automated Semiconductor Manufacturing Environment"	108
Nirmal Govind, Bala Iyer, Intel Corporation	
5.3a "Chamber Cleaning Process Selection for the Installed-base CVD Tools"	114
Franco Blundo, Manfredi Alberghina, Marcello Frazzica, ST Microelectronics; Gary Loh, Michael Mocella, Dupont Electronic Gases	
5.4a "Comparison of Three Different Methods to Model the Semiconductor Manufacturing Yield"	119
Yoan Dupret, Erwan Perrin, Jean-Luc Grolier, Altis Semiconductor; Richard Kielbasa, Supelec	
5.5a "E-beam Inspection of SOI Wafers for the Evaluation of Barrier Nitride RIE Etching"	125
Alexander Ache, Nicole Rowand, IBM Microelectronics; Kevin Wu, KLA-Tencor Corporation	
5.6a "Effects of Wafer Bow and Warpage on Performance of Electrostatic Chucks in High Volume Manufacturing"	128
Piotr Kurkowski, Sergei Drizlikh, Roger Sawyer, Heath Angis, Patrick Loisel, National Semiconductor Corporation	
5.7a "Embodiment of Compact and High Performance HVIC process"	131
C.K. Jeon, L. Kim, M. H. Kim, T. H. Kwon, J. J. Kim, Fairchild Semiconductor Corporation	
5.8a "EQ Integrated Process Trending with TFM Monitoring for Back End Equipment"	135
Thomas Rathgeber, Norbert Hauels, Infineon Technologies	
5.9a "Fault Detection in Reactive Ion Etching Systems Using One-Class Support Vector Machines"	140
Tomas Sarmiento, and Gary S. May, School of Electrical and Computer Engineering, Georgia Institute of Technology; Sang J. Hong, Myongji University	
5.10a "Improvement of Film Uniformity Stability of PECVD Silicon Nitride Deposition Process by Addition of Fluorine Removal to the Plasma Clean Sequence"	144
Ailian Zhao, Joseph Bulger, Marc French, Leslie Green, William C. Harris, Timothy J. Hunt, Holly Lisy, William Marchesseault and Richard Shuman, Intel Corporation	
5.11a "Low-Yield Flier Wafer Analysis Strategies"	150
Brian Dunham, Travis D. Kirsch, Stuart Litwin, Michael Covert, Daniel Garcia, Alex Bierwag, Kendall Holt, Spansion	
5.12a "Moisture Effects on Purifier/Chemical Filter Materials"	155
Daniel Alvarez, Joseph Rotter, Troy Scoggins, Mykrolls Corporation	
5.13a "Reducing Defectivity in 90nm BEOL Metal CMP Using a Geometry-Based Segmented Inspection Strategy"	160
Andrew Stamper, IBM Microelectronics; Wee Teck Chia, KLA-Tencor Corporation	
5.14a "A Reticle Quality Management Strategy in Wafer Fabs Addressing Progressive Mask Defect Growth Problem at low k-1 Lithography"	167
Kaustuve Bhattacharyya, Mark Eickhoff, Michael Lang, KLA-Tencor Corporation; Mark Ma, Sylvia Pas, Texas Instruments, Inc.	
5.15a "Scanner Influences on Resolution Capabilities"	175
Holly Magoon, Nikon Precision Inc.	
5.16a "Silicon Carbide: Barriers to Manufacturable Devices"	180
Joseph Shovlin, Richard Woodin, Tony Witt, Gary Dolny and Praveen Shenoy, Fairchild Semiconductor Corporation	
5.17a "SPC Based In-line Reticle Monitoring on Product Wafers"	185
Karsten Mai, Infineon Technologies GmbH; Martin Tuckermann, KLA-Tencor GmbH	
5.18a "Thoughts on an Automation Concept for Complex Production Process within a Learning Organization"	190
Gerhard Luhn, Walter Reithofer, Hans-Joachim Schmidt, Martin Peiter, Infineon Technologies Dresden; Frank Boelstler, IPA Stuttgart; Thomas Lang, Systema Dresden	

5.19a "Ultra Short Pulse Laser Meeting the Requirements for High Speed and High Quality Dicing of Low-K Wafers"	195
Jan Sillanpaa, Jarno Kangastupa, Arto Salokatve, Harry Asonem, Corelase	
5.20a "Using TCAD for Fast Analysis of Misprocessed Wafers and Yield Excursions"	198
Rainer Minixhofer, austriamicrosystems AG and Dieter Rathei, D R YIELD Software & Solutions	
Session 6 - Advanced Processing	
6.1a "A Novel High Speed and High Voltage Complimentary Bipolar Process Using 1st Base-Poly Silicon Collector and SOI Technique" ...	201
J. H. Kim, S. H. Lee, H. J. Park, M.H. Choi, Dale Wedel, J. J. Kim, Fairchild Korea Semiconductor	
6.2a "Integration of Nickel Silicide: Minimizing Defect Generation During Formation"	206
John Foggiano and Woo Sik Yoo, WaferMasters, Inc.	
6.3a "Critical Challenges in Packaging MEMS Devices"	211
Robert Daweaux, Amkor Technology and Lakshmi Munukutla, Arizona State University	
6.4a "Use of Surface Sensitive Analysis Techniques for the Study of Silicide Processes in Power Transistors: Platinum Silicide Formation as an Example"	218
Daniel Kraft, Paul Ganitzer, Philipp Kohler-Redlich, Infineon Technologies Austria; Uwe Scheithauer, Siemens AG	
Session 7 - Improving Factory Performance	
7.1a "Stretching Factory Performance Beyond World Class, An Organizational Approach"	224
Scott Lantz, Intel Corporation	
7.2a "Operations and Product Development: Integrating Methodologies for Improved Product Success"	228
Thomas Carbone, Fairchild Semiconductor Corporation	
7.3a "Hybrid Manufacturing - Lower Cost Access to DSM Technology"	234
Brett Williams and Mark Nelson, AM1 Semiconductor, Inc.	
7.4a "Exploring New Design Architectures to Reach Time-to-Market Goals"	239
Aki Fujimori, Cadence Design Systems; Ketan Joshi, X Initiative	
Session 8: Advanced Yield Methodologies	
8.1a "Measurement and Reduction of Critical Area Using Voronoi Diagrams"	243
Daniel Maynard, IBM Microelectronics	
8.2a "Yield Enhancement Through Fast Statistical Scan Test Analysis for Digital Logic"	250
Hans Peter Erb, Christian Burmer, Andreas Leininger, Infineon Technologies	
8.3a "MOS Transistor Mismatch Modeling for High Voltage CMOS Processes"	256
Werner Posch, Gerhard Rappitsch, Georg Leonardelli, austriamicrosystems AG	
8.4a "Yield Management Practice by User Designable YMS"	261
Masayuki Inokuchi, JEOL System Technology Company	
Session 9: Factory Automation and Integration II	
9.1a "Enabling Remote Operations and Cycle Time Reduction Via Automated Lot-Equipment Assignments"	266
Bala Iyer, Joseph J. Concelman, Thomas Jefferson, Robert A. Madson, Jason M. Trujillo, Intel Corporation	
9.2a "Intergration of Lot Dispatching and AMHS Control in a 300mm Wafer FAB"	270
Dong-Seok Sun, No-Sik Park, Young-Joong Lee, Young-Chul Jang, Chung-Sam Ahn, Samsung Electronics Inc. Ltd; Tae-Eog Lee, Korea Advanced Institute of Science and Technology	
9.3a "A Systems Approach to Evaluating the Impact of Technician Training"	275
Bob Simington, Intel Corporation	
9.4a "Lot Identification, Lot Location and Information Distribution Using Radio Frequency and Ultrasonic Signals"	280
Hanspeter Fischer, Infineon Technologies Austria; Ralf Schrodell, Infineon Technologies AG; Stefan Eisen, Markus Dierkes, Intellion AG	

2004 – The Year of 90-nm: A Review of 90 nm Devices

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Abstract

The year 2004 saw the introduction of the first 90-nm process node devices into the marketplace. This node is notable not only for the expected reduction in feature sizes, but also for the more general adoption of low-k dielectric layers, and the first use of nickel silicide and strained silicon.

Chipworks, as a supplier of competitive intelligence to the semiconductor and electronics industries, monitors the evolution of chip processes as they come into commercial production. Chipworks has obtained parts from leading edge manufacturers, and performed structural analyses to examine the features and manufacturing processes of the devices.

The paper shows how “90nm” has been interpreted by various vendors, details the physical transistor structures we have analyzed, and comments on the introduction of strain into CMOS processing.

INTRODUCTION – WHAT IS 90 NM?

We continually see parts labeled as “130 nm” or “90 nm”. To the uninitiated, this must seem to be some form of code, but it is actually just industry jargon for a process generation or ‘node’.

The 199□ NTRS (National Technology Roadmap for

Semiconductors) predicted a minimum feature size of 130 nm in 200□, with a 90 nm feature size in 2008. It is a reflection of the frenetic pace of process development that we are currently seeing feature sizes of less than 50 nm, and metal pitches ~230 nm.

Table 1 shows a comparison of the metal 1 half-pitch and minimum gate dimensions that we found in the samples analyzed by Chipworks. As can be seen, no manufacturer meets the actual ITRS numbers – Intel is closest in M1 dimensions, and Fujitsu the closest in gate length.

90-NM TRANSISTORS

Sony/Toshiba CXD9797GB from Sony PSX

Toshiba was the first off the mark in January, with the Sony PSX chip, which combined the Sony graphics synthesizer with their Emotion Engine™ on one die. The process used five layers of copper + one aluminium, two low-k layers at metal 2 and metal 3 (M2 and M3), and a □5 nm minimum gate.

Figure 1 shows a SEM image of NMOS transistors stained to show the source/drains. Figure 2 is a TEM image; the structure of the sidewall spacers can be seen. In essence, this seems to be a dimensional shrink from the previous generation.

Table 1. Comparison of Published and Found Dimensions with ITRS 2003 Dimensions for the 90nm Node

	Metal 1 Half-Pitch (nm)		Minimum Gate Length (nm)	
	Published	Found	Published	Found
ITRS 2003 (MPU/ASIC)	107		37	
Sony/Toshiba	120	130	65	□5
Texas Instruments	165	165	52	□7
Intel	110	120	50	□5
IBM	158	135	□6	□5
UMC (Xilinx)	2□0	2□0	70	55
TSMC (Altera)	120	125	59	55
Fujitsu (Transmeta)	1□0	1□5	□0	□0
AMD	N/A	130	N/A	□9

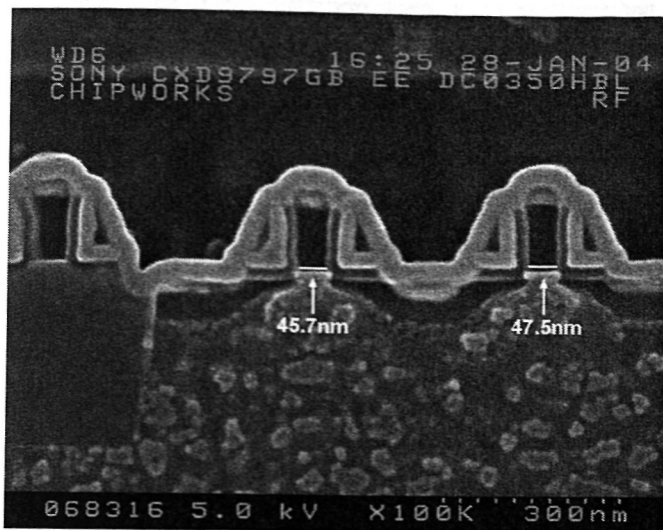


Figure 1. SEM Cross-Section of NMOS Transistors in Sony PSX

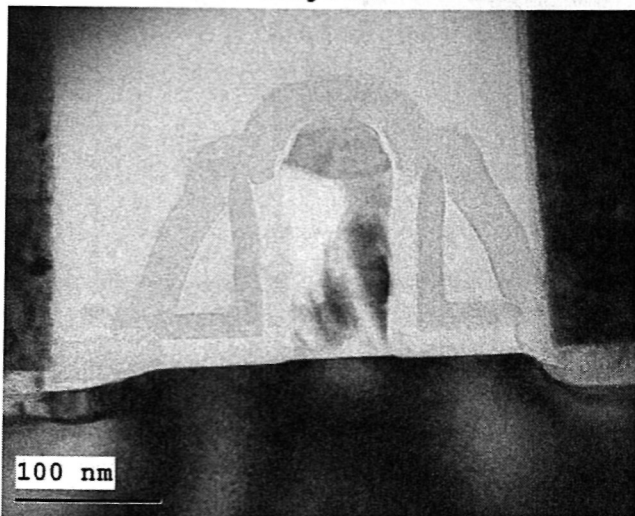


Figure 2. TEM Cross-Section of Sony PSX Transistor

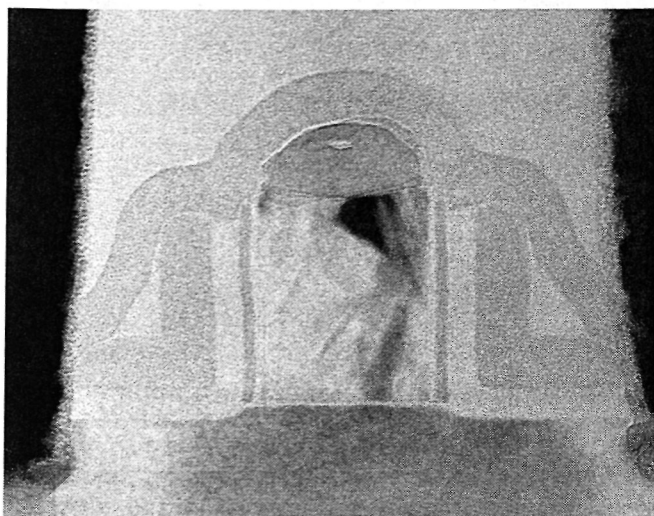


Figure 3. Transistor in TI DSP

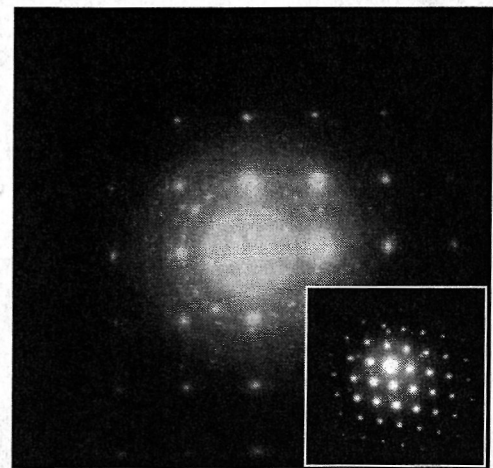


Figure 4. TEM Electron Diffraction Image of TI Transistor Channel Region (Inset – Intel Prescott, <110> Channel Direction)

Texas Instruments TMX320C6416T 1 GHz DSP

The TI DSP is a 7-metal part, with low-k at M1 – M7. The transistor again appears to be a shrink down to a 70 nm gate length, with a nitride liner on the side of the gate electrode. Figure 3 is a TEM image of the transistor cross-section.

The distinguishing feature of the TI process revealed itself in an electron diffraction image (Figure 4). This showed that the channel was oriented in the <100> direction, compared with the more normal <110> direction. This orientation gives higher PMOS mobility.

Intel Prescott

Intel first announced their 90-nm P1262 process in March 2002. Process details such as the use of strained silicon and nickel silicide were given later in the year and at the 2002 IEDM [1], and at IEDM 2003 Intel showed the different strain techniques for NMOS and PMOS transistors [2]. The Prescott die analysed by Chipworks had seven metal levels, with five low-k layers at M2 – M7.

An NMOS transistor is imaged in Figure 5. Localized tensile stress is applied to the channels of NMOS devices by a highly stressed nitride sealant layer, in undercut regions under the edges of the sidewall spacers. This increases electron mobility by ~10%. The gate oxide thickness is ~1.3 nm.

The PMOS transistors (Figure 6) use epitaxial SiGe source/drains to create compressive stress – this improves hole mobility by as much as 50%. The substrate is etched out in the source/drain regions, and local epi-SiGe (~17% Ge) is deposited into the cavities. Crystalline facets form raised source/drains, reducing the series resistance. The tensile stress from the nitride layer is counteracted by the compressive effect.

The strain has induced dislocations at the SiGe/Si interface. The SiGe was likely *in-situ* boron-doped, and also implanted with the polysilicon gate implant. The boron

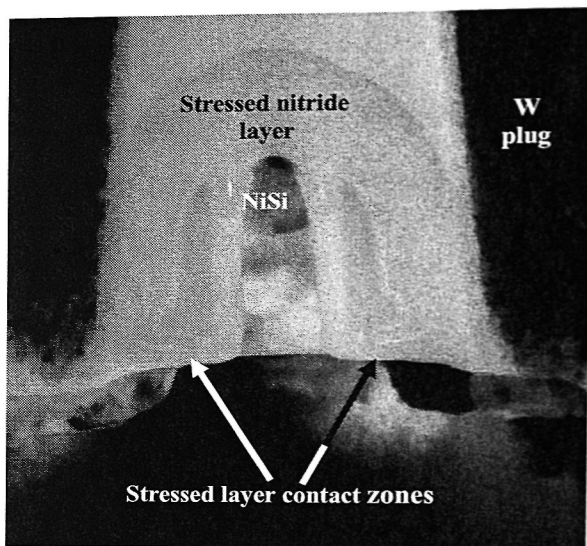


Figure 5. NMOS Transistor in Intel Prescott

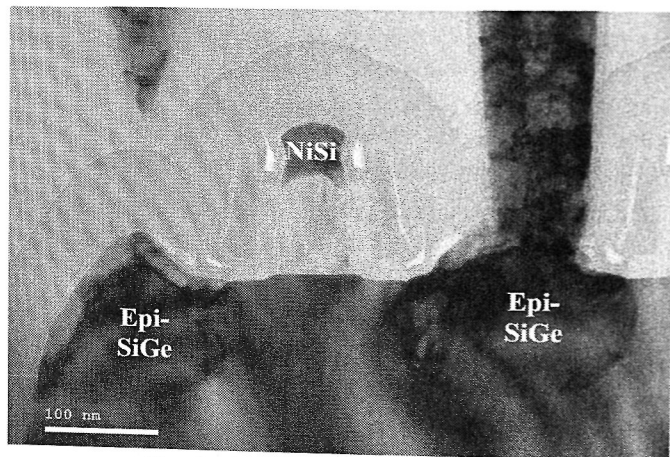


Figure 6. Intel PMOS Transistor

out-diffuses from the SiGe into the silicon to neutralize the potential leakage caused by the dislocations. Nickel silicide was chosen because it consumes less silicon and forms at a lower temperature, making it more compatible with the SiGe.

Figure 7 is a longitudinal section of a PMOS source/drain, clearly showing a stacking fault extending from the epitaxial interface to the silicide layer.

IBM PowerPC PC970FX

The IBM PowerPC is built on a 5 nm-thick SOI layer, with a 5 nm gate length with a 1.5 nm gate oxide thickness. The part has ten metal levels with a hybrid FSG/USG dielectric structure.

IBM had stated that the part would use strain technology, and press reports in the spring of 2000 speculated that the "Strained Silicon Directly on Insulator" (SSDOI) technique, which was announced at IEDM 2003 [3], would be used.

The device appears to use a stressed nitride layer to

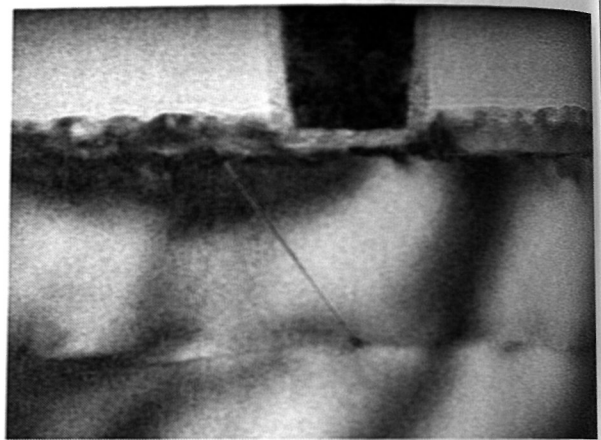


Figure 7. Longitudinal Section of Intel PMOS Source/Drain

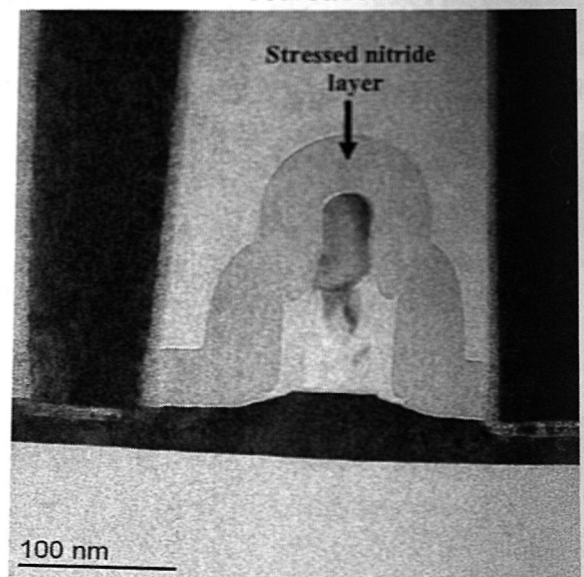


Figure 8. NMOS Transistor in IBM PPC970FX

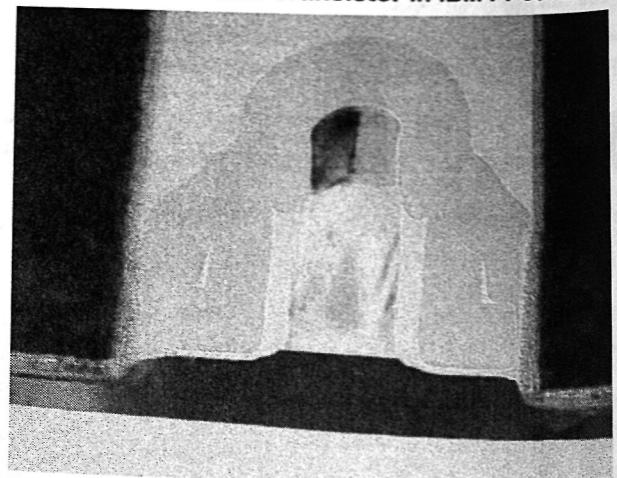


Figure 9. PMOS Transistor in IBM PPC970FX

enhance the NMOS transistors. Figure 8 is a TEM image of a NMOS transistor, and it can be seen that the sidewall spacers are very slim, and it is only ~20 nm from the gate edge to the cobalt silicide of the source/drain. Comparison with a PMOS transistor (Figure 9) illustrates that the

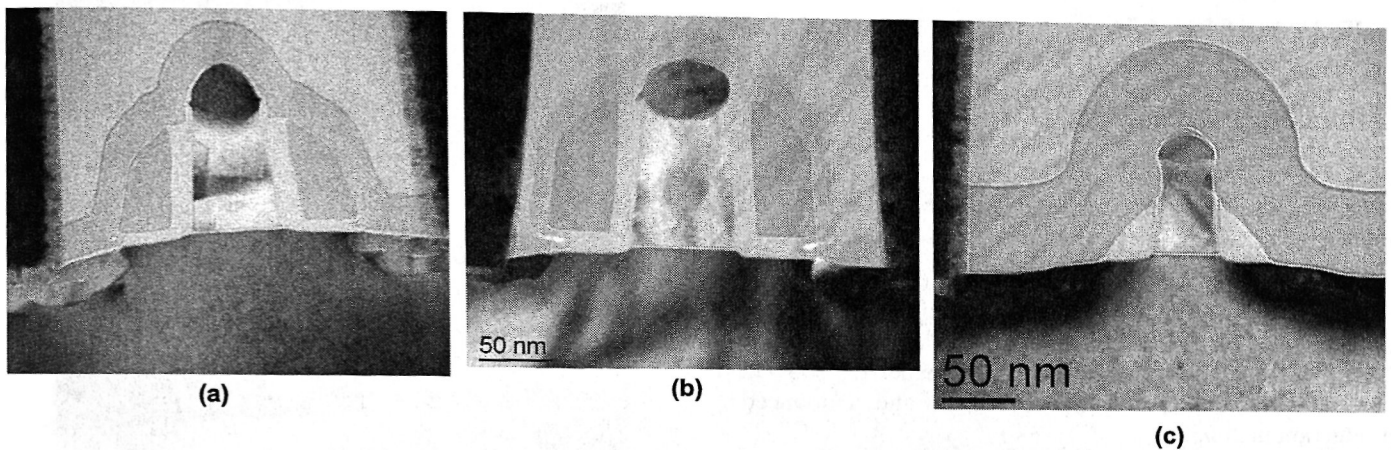


Figure 10. Transistors in (a) Xilinx Spartan-3, (b) Altera Stratix-II, (c) Transmeta Efficeon-2

NMOS spacers have indeed been etched back in order to reduce series resistance, and place the stressed nitride layer closer to the gate edge. Electron diffraction studies on the SOI body confirmed $\langle 110 \rangle$ -channel orientation, and there was no indication of a SSDOI substrate. The IEDM SSDOI paper indicated that $\sim 1.5\%$ lattice distortion was required to give useful mobility enhancement.

It is interesting to note that at IEDM 2000, IBM and AMD presented a joint paper [1] on “dual stress liner” technology, which uses stressed nitride layers optimized to apply tensile stress to NMOS transistors, and compressive stress to PMOS devices.

This technique is to be integrated into 90-nm product in the first half of 2005. There was no mention of the use of SSDOI substrates.

UMC (Xilinx Spartan-3)

The Xilinx part was the first 90-nm part from a pure foundry analyzed by Chipworks. The transistor structure was very similar to the 130-nm node device, with the gate shrunk to 55 nm (Figure 10(a)). The gate length was smaller than the UMC-published value of 70 nm, but in other respects the part was manufactured using a more conservative process; FSG was used as the inter-metal dielectric, with seven copper + one aluminium metal levels (although UMC states that low-k dielectrics are available as an option).

There does not appear to be any use of strain to enhance mobility – the nitride layer is thinner than those used in strained devices, and there seems to be no structural changes to move the nitride contact zone closer to the gate edge. However, the gate edge/silicide distance is a respectably small ~ 5 –50 nm.

TSMC (Altera Stratix™-II)

The other major foundry to launch a 90nm process in 2000 was TSMC. The product analyzed by Chipworks was the Altera Stratix™-II FPGA. This displayed a gate length of 55 nm, similar to UMC, although closer to the published 59

nm physical gate length of the Nexsys™ process. This is another ten-metal part (9 Cu + 1 Al), using low-k at M1 – M6.

The transistor structure (Figure 10(b)) is not a direct shrink from the 130nm node; it has been modified to change the sidewall spacer structure from the typical L-shaped spacer of previous process generations. Again, the nitride layer appears to be too thin to be used as a stress layer for mobility enhancement. Gate/silicide spacing is ~ 55 nm.

The other major feature of the TSMC 90-nm process is its evolution towards a second-generation low-k dielectric process – the trench and via etching are noticeably cleaner than at the 130-nm node, and the cap layer has changed to a SiCO (rather than SiCN) composition.

Fujitsu (Transmeta Efficeon-2)

Transmeta announced shipment of its Efficeon-2 in September, fabricated by Fujitsu at their Akiruno Advanced Technology Center. This part also seems to use a strained nitride layer. Figure 10(c) displays what is becoming a characteristically thick nitride sealant layer, which combined with the heavily etched sidewall spacers, leads us to conclude that nitride stress is being used.

Fujitsu had announced the use of nitride strain for the 65-nm node at VLSI 2003 and 2000 [5][6], and they seem to have used the technique in their nominal 90-nm process. Given that the gate length is an impressively small ~ 40 nm, and the gate length for the 65-nm process is quoted at 35 nm, this part could be regarded as an interim step to 65-nm. (They also published a dual-stress process at IEDM '00 [7])

In addition, electron diffraction shows that the channels are oriented in the $\langle 100 \rangle$ direction, so Fujitsu is the first manufacturer to combine channel re-orientation and strain to optimise mobility.

The dielectric layers are also advanced, using Novellus Coral low-k (not SiLK!) with SiCO copper-cap and etch-stop layers at M1 – M5. It is an eight-metal part, again with a top aluminium layer.

AMD Athlon 64 Mobile

AMD continued their use of “double spacer” technology at the 90-nm node, with a gate shrink to ~50 nm. The NMOS device (Figure 11) consistently has dislocations under the inner spacer, presumably caused by the drain extension implant. These do not appear in the PMOS transistors (Figure 12), which likely have a different amorphisation implant to fix the drain extension.

There is no evidence of either nitride strain or substrate strain in this part; the nitride is relatively thick, and the double spacer places the contact zone further from the gate. The joint AMD/IBM “dual stress liner” paper [□] showed an Athlon fabricated with the technique, and announced production in 2005.

AMD have also evolved their interconnect structure for the 90-nm node, compared with the 130 nm; the metallisation (9 Cu + 1 Al) is now predominantly dual-damascene, although whilst the dielectric structure is still a hybrid low-k/FSG.

SUMMARY AND DISCUSSION

We have seen eight examples of 90-nm processes in this review, with transistor gate lengths ranging from □0 – 55 nm. Intel, IBM, and Fujitsu have introduced strain for mobility enhancement, and notably Intel has taken the extra steps of embedded SiGe strain for PMOS, and nickel silicide. Texas Instruments and Fujitsu have also used re-orientation of the substrates to improve mobility.

It appears that 90-nm is the node at which strained silicon is coming into production, although not by using epitaxially strained substrates. The strain method of choice has been localised uni-axial strain, as opposed to the bi-axial strain created by strained SiGe layers.

It is perhaps ironic that stress in silicon nitride layers, a problem in previous process generations, has now been harnessed to apply strain. So far, it has been used only to provide tensile stress to enhance NMOS performance (at least in the three examples we have shown), but the dual-stress approach announced by IBM/AMD and Fujitsu indicates that the layer can also be tuned to provide compressive stress to improve hole mobility for PMOS devices. This technique has the noteworthy convenience that it can be accomplished by process tuning, and involves no extra cost for either capital equipment or special substrates.

It remains to be seen if the embedded SiGe approach used by Intel will become the dominant method of applying compressive stress for PMOS. Texas Instruments has indicated that it will be using local SiGe strain and nickel silicide in its 65-nm process [8], so Intel will not be alone.

All in all, 200□ was an important year in CMOS process evolution, with significant developments in transistor engineering, and further improvement in low-k dielectric usage. We will see what 2005 brings!

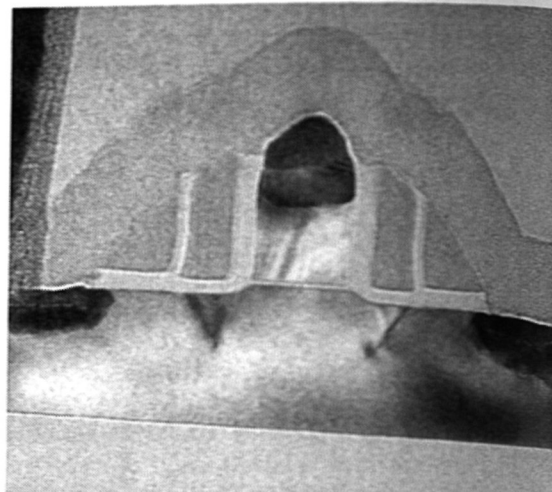


Figure 11. NMOS Transistor in AMD Athlon

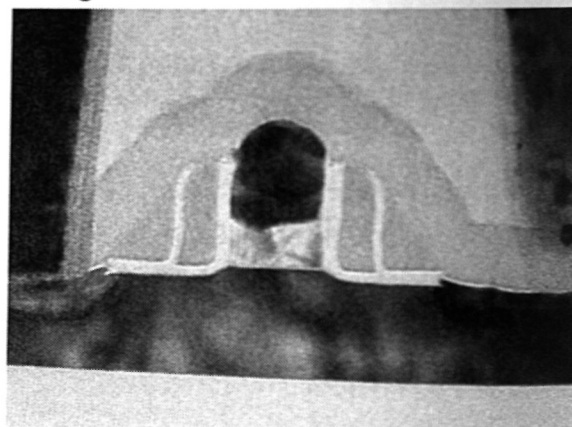


Figure 12. PMOS Transistor in AMD Athlon

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BIOGRAPHY

Dick James graduated in 1971 with a Masters degree in Microelectronics and Semiconductor Devices from the University of Southampton in England, after gaining a B.Sc in Applied Chemistry from the University of Salford. He has spent over 30 years working in the process development, design, manufacturing, packaging and reverse engineering of semiconductor devices. He joined the Chipworks team in March 1995 as Manager, Microstructural Characterization, and is currently Senior Technology Analyst.

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