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Matsui

(54) SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

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(52) **U.S. Cl.** **257/344**

(57) **ABSTRACT**

In view of micronizing semiconductor device and of suppressing current leakage in a shared contact allowing contact between a gate electrode and an impurity-diffused region, a semiconductor device **100** includes a first gate electrode **108**, a fourth source/drain region **114**b, and a shared contact electrically connecting the both, wherein in a section taken along the gate length direction, the first gate electrode **108** and the fourth source/drain region **114**b are disposed as being apart from each other, an element-isolating insulating film **102** is formed over the entire surface of a semiconductor substrate **160** exposed therebetween, and the distance between the first gate electrode **108** and the fourth source/drain region **114**b is made substantially equal to the width of the sidewall formed on the side face of the first gate electrode **108**, when viewed in another section taken along the gate length direction.

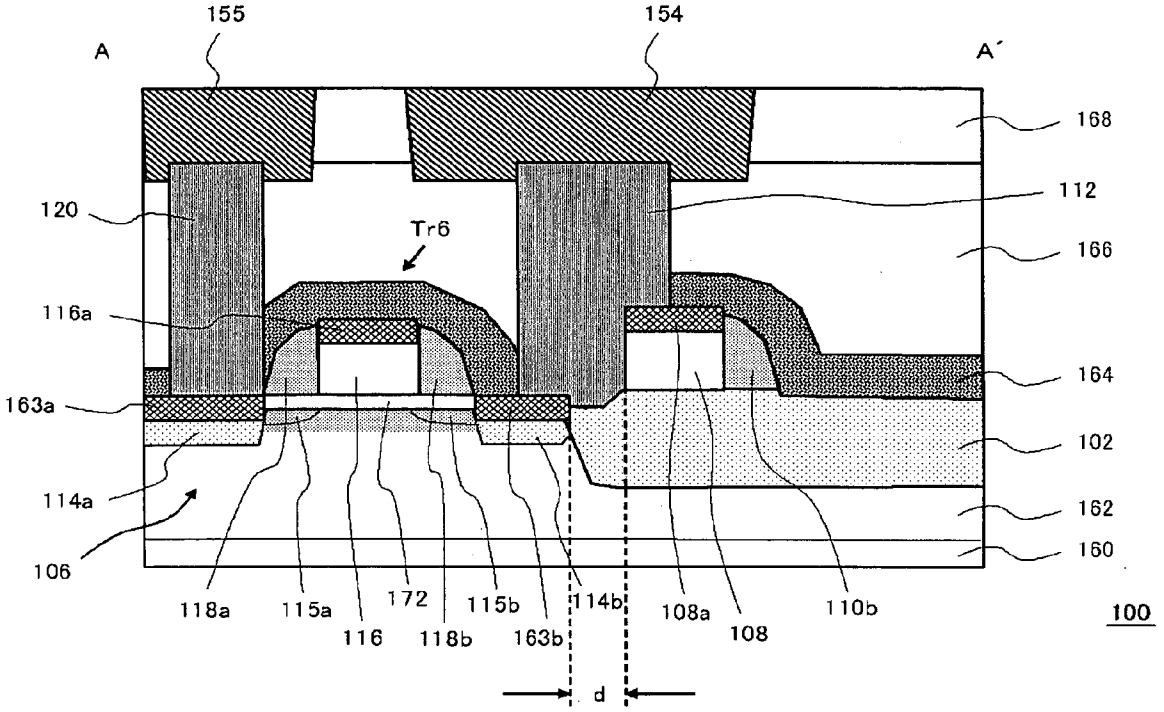

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FIG. 1

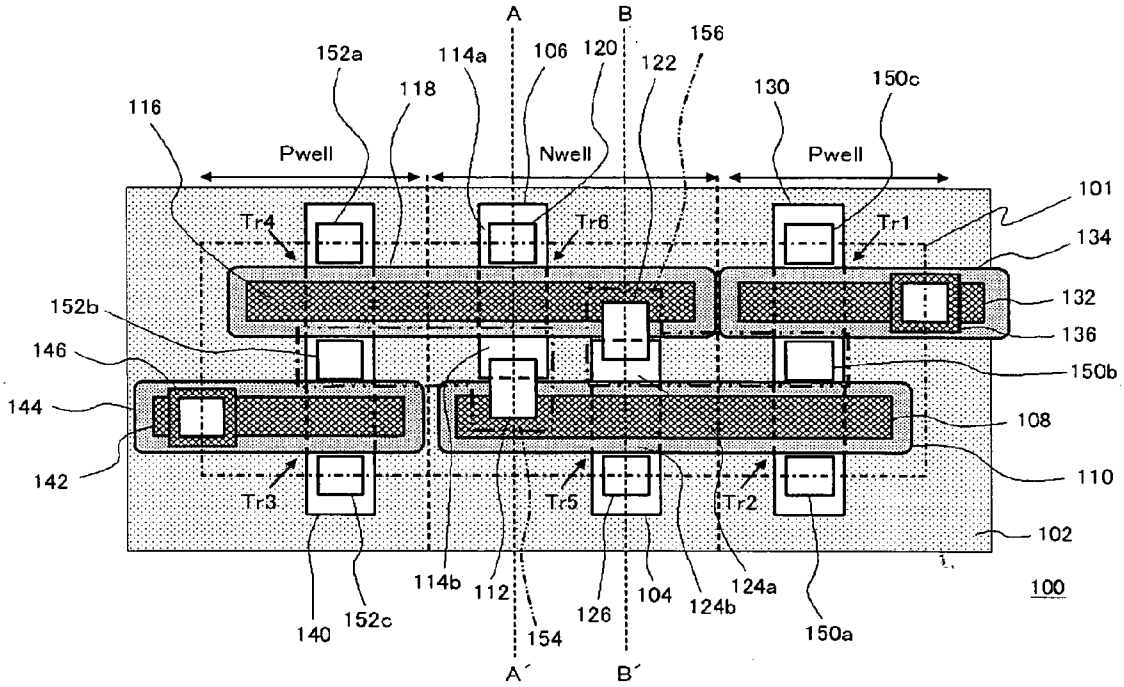

A
B
152a
114a
106
120
156
122
118
130
150c
116
Pwell
Nwell
Pwell
101
Tr4
Tr6
Tr1
134
152b
132
136
146
150b
144
108
142
110
Tr3
Tr5
Tr2
102
114b
112
124a
100
140
152c
126
104
124b
150a
154
A´
B´

FIG. 2

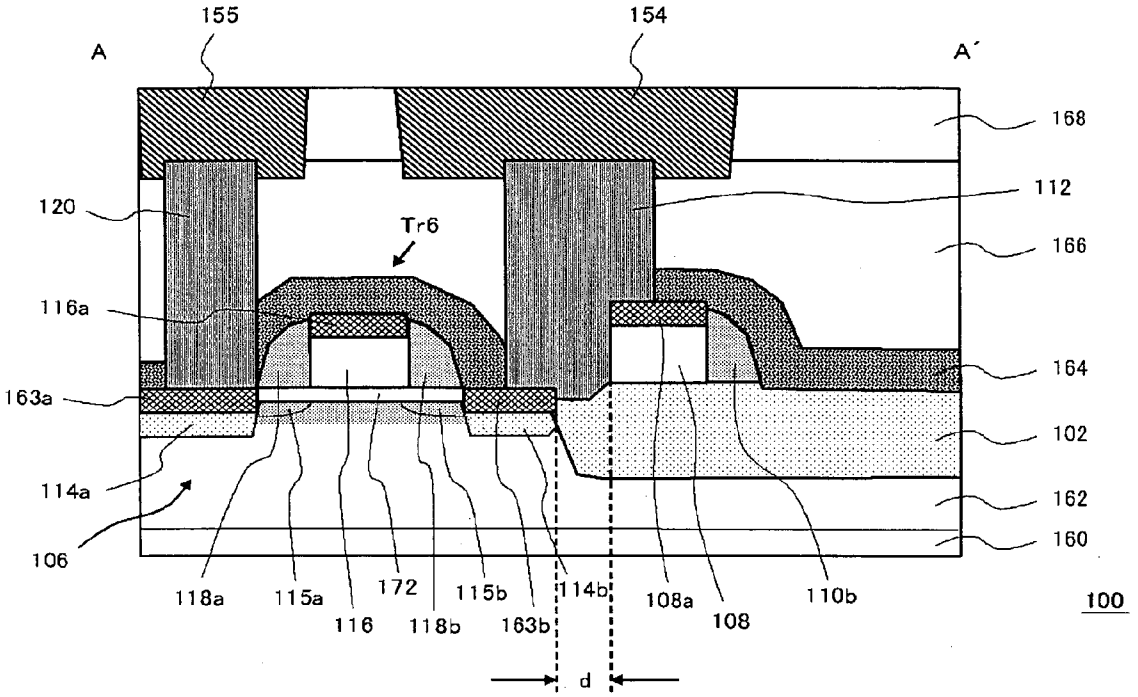

155
154
A
A´
168
112
120
Tr6
166
116a
164
163a
102
114a
162
106
160
118a
115a
172
115b
114b
108a
110b
100
116
118b
163b
108
d

FIG. 3

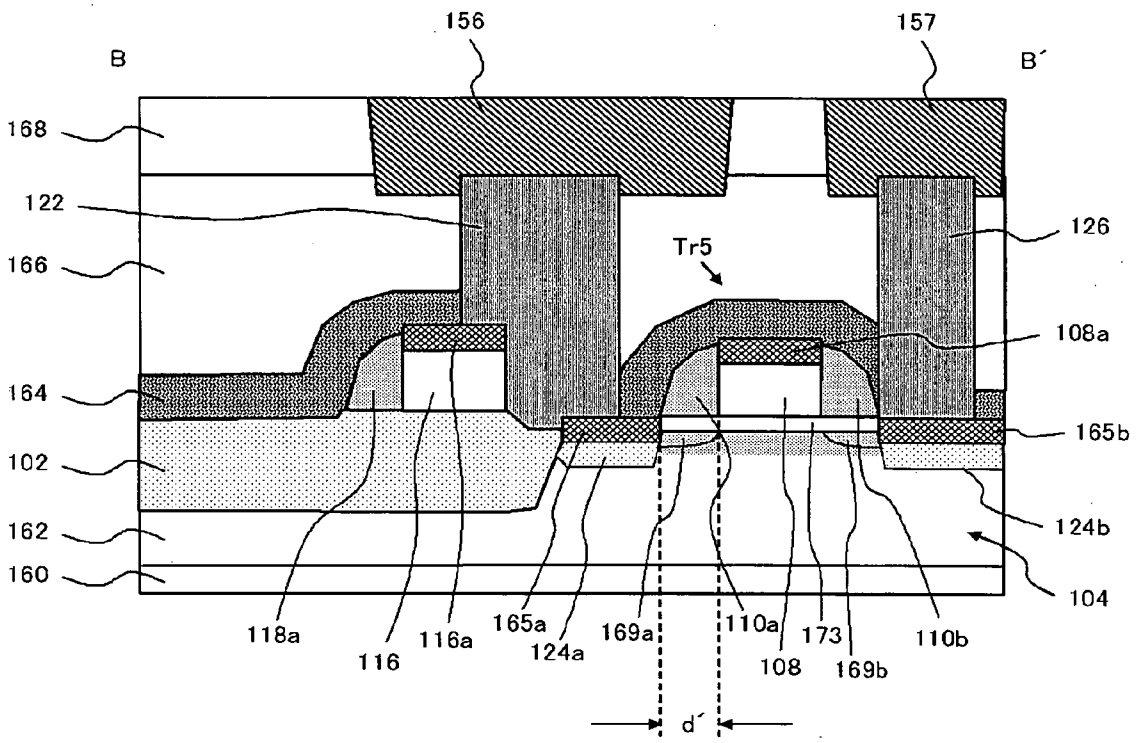

156
157
B
B´
168
122
126
166
Tr5
108a
164
165b
102
124b
162
160
104
118a
116
116a
165a
124a
169a
110a
108
173
169b
110b
d´

FIG. 4A

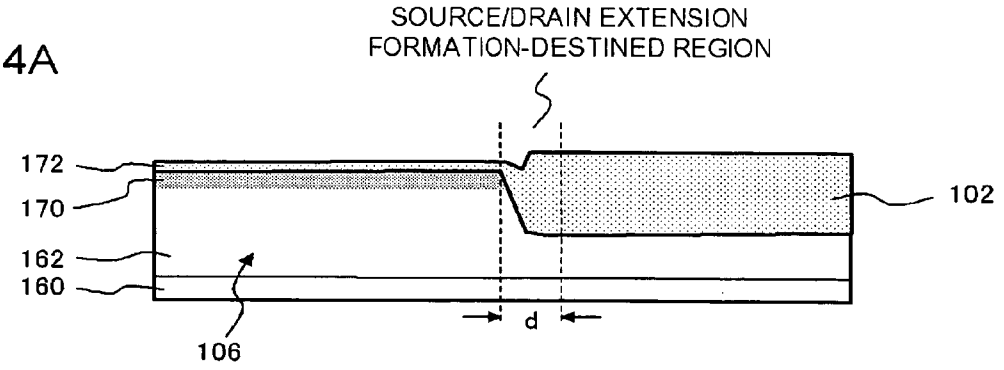


FIG. 4B

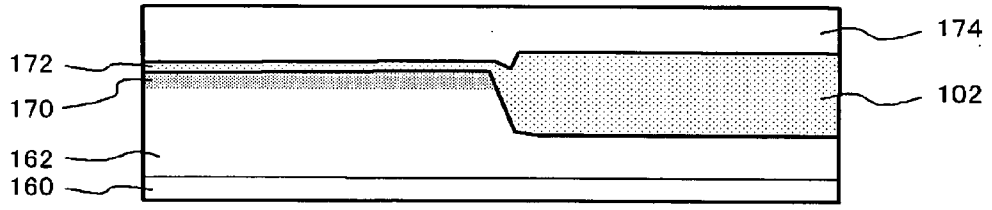


FIG. 4C

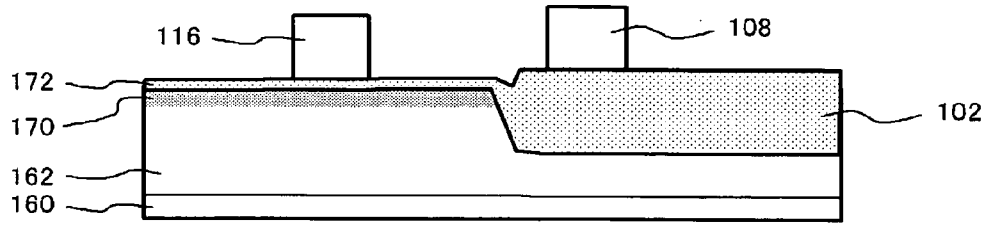


FIG. 5A

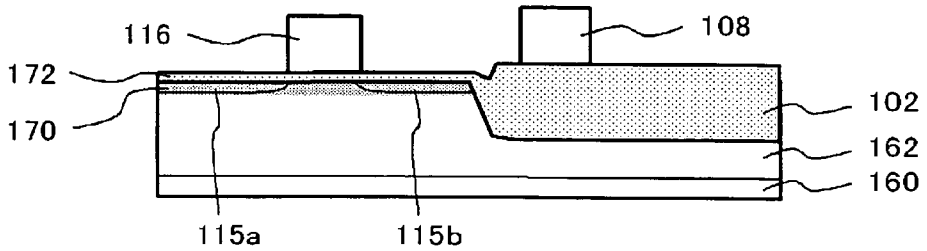


FIG. 5B

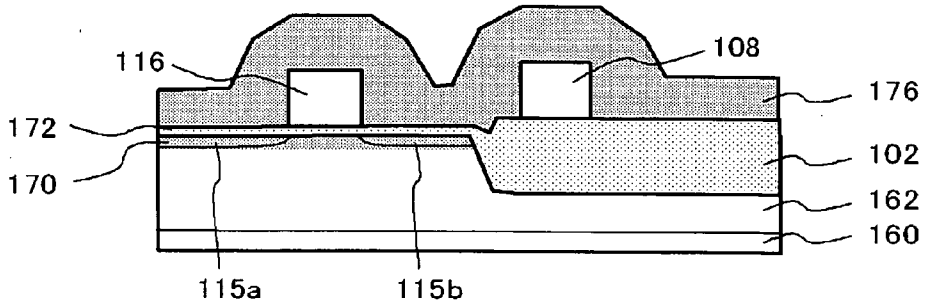


FIG. 5C

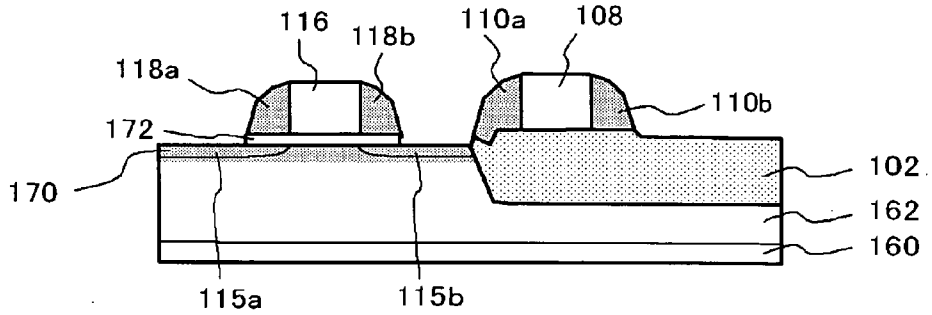


FIG. 5D

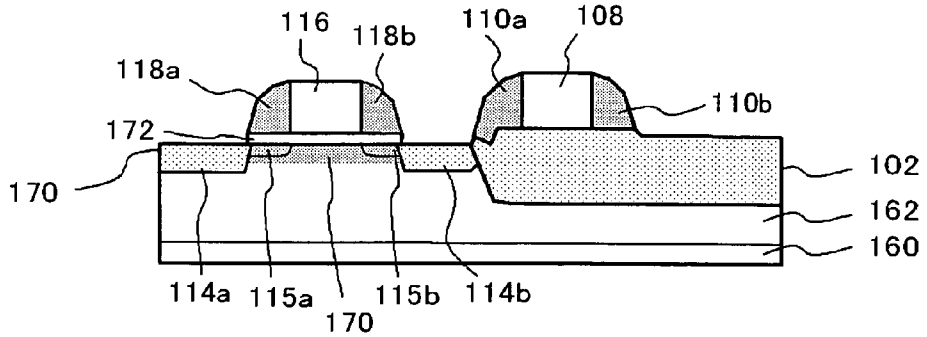


FIG. 6A

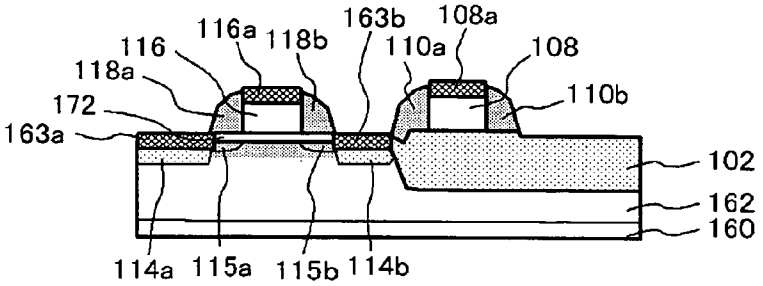


FIG. 6B

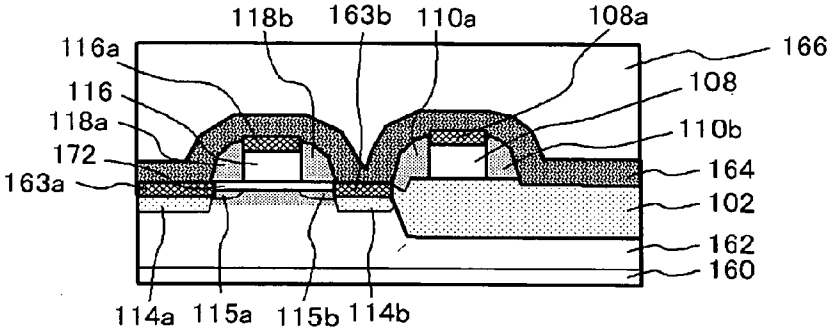


FIG. 6C

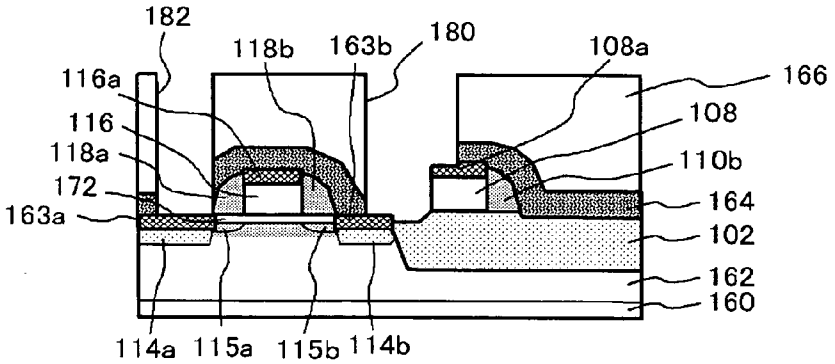


FIG. 6D

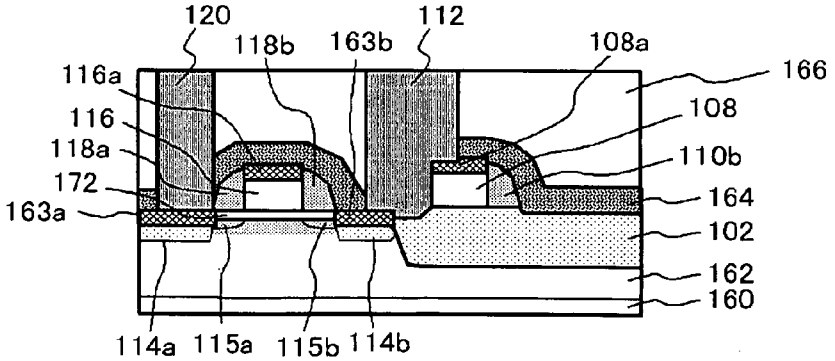


FIG. 7A

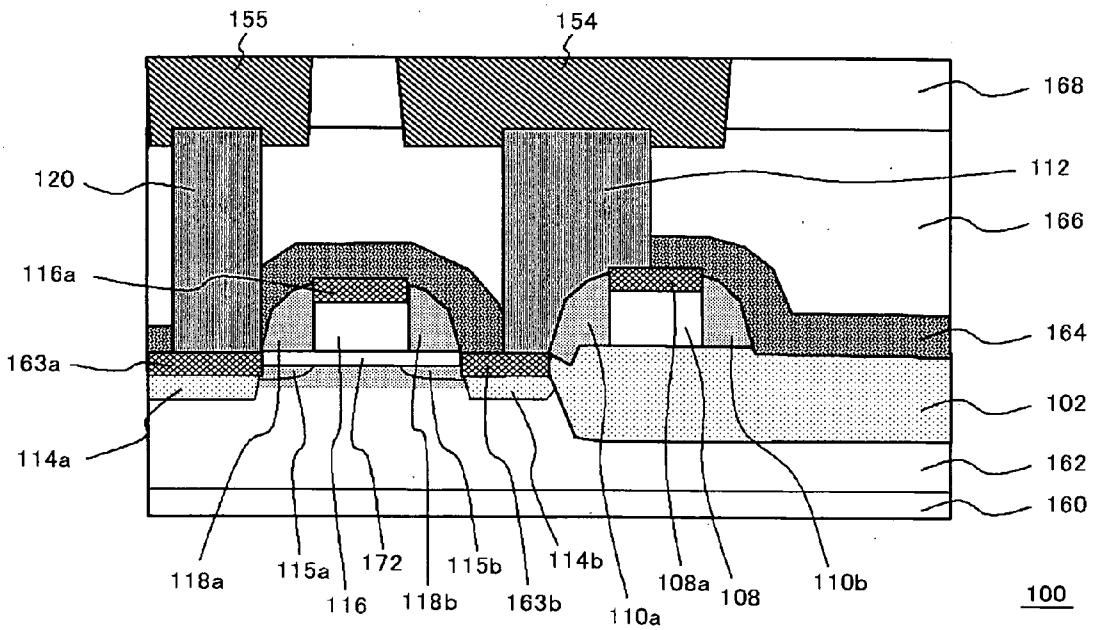

155
154
168
120
112
166
116a
164
163a
102
114a
162
160
118a
115a
172
115b
114b
108a
110b
116
118b
163b
110a
108
100

FIG. 7B

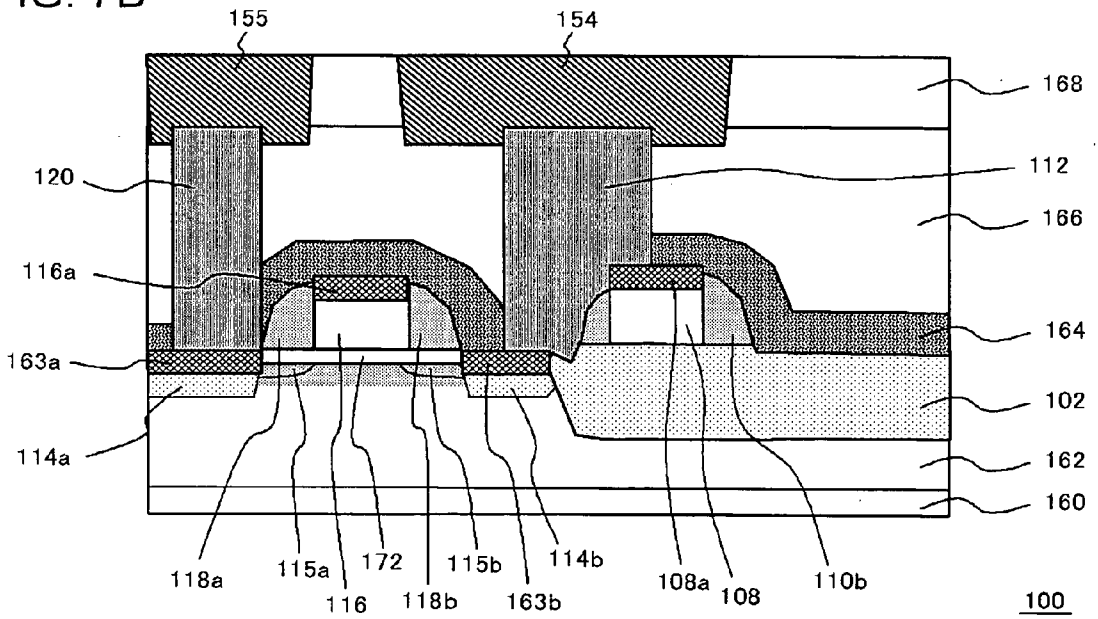

155
154
168
120
112
166
116a
164
163a
102
114a
162
160
118a
115a
172
115b
114b
108a
110b
116
118b
163b
108
100

FIG. 8A

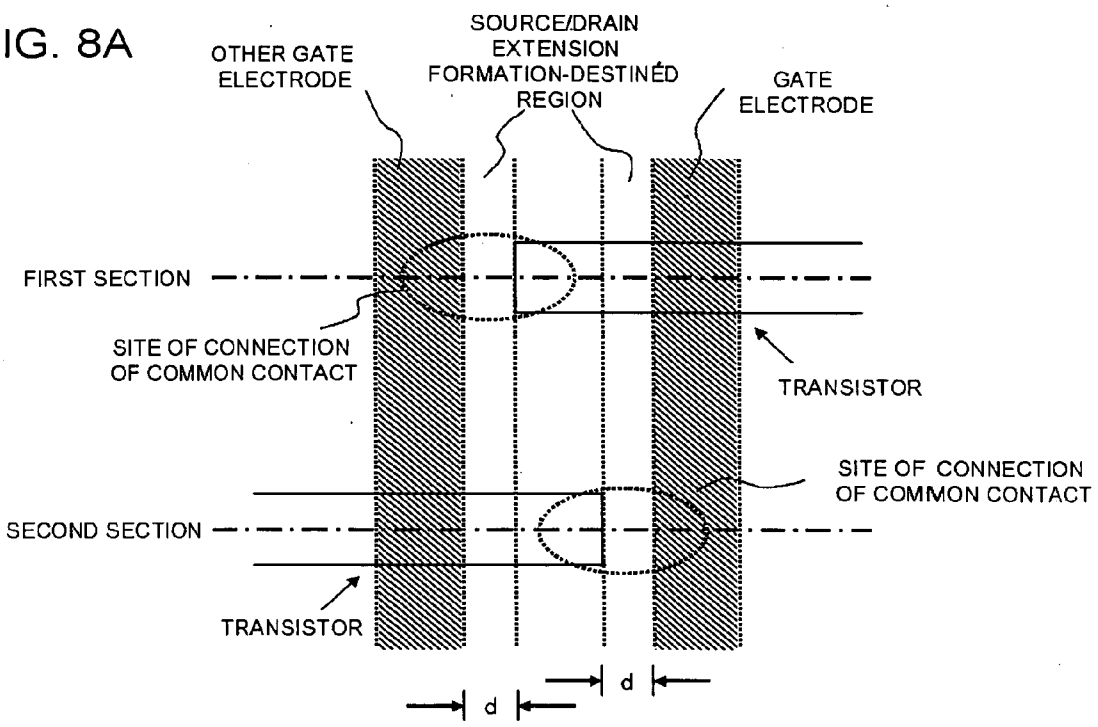

OTHER GATE ELECTRODE
SOURCE/DRAIN EXTENSION FORMATION-DESTINÉD REGION
GATE ELECTRODE
FIRST SECTION
SITE OF CONNECTION OF COMMON CONTACT
TRANSISTOR
SITE OF CONNECTION OF COMMON CONTACT
SECOND SECTION
TRANSISTOR
d
d

FIG. 8B

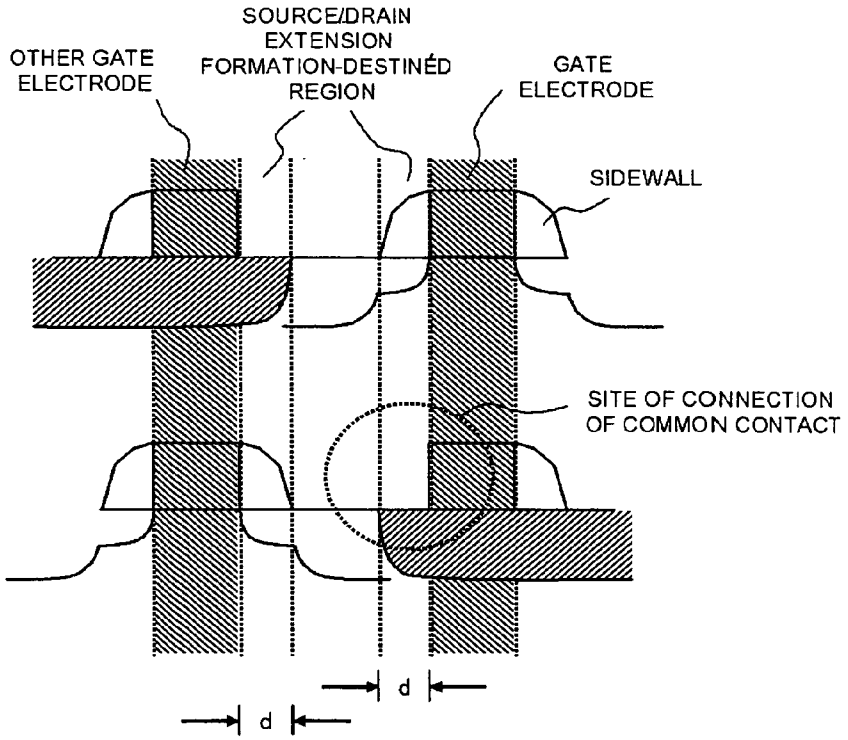

OTHER GATE ELECTRODE
SOURCE/DRAIN EXTENSION FORMATION-DESTINÉD REGION
GATE ELECTRODE
SIDEWALL
SITE OF CONNECTION OF COMMON CONTACT
d
d

FIG. 9

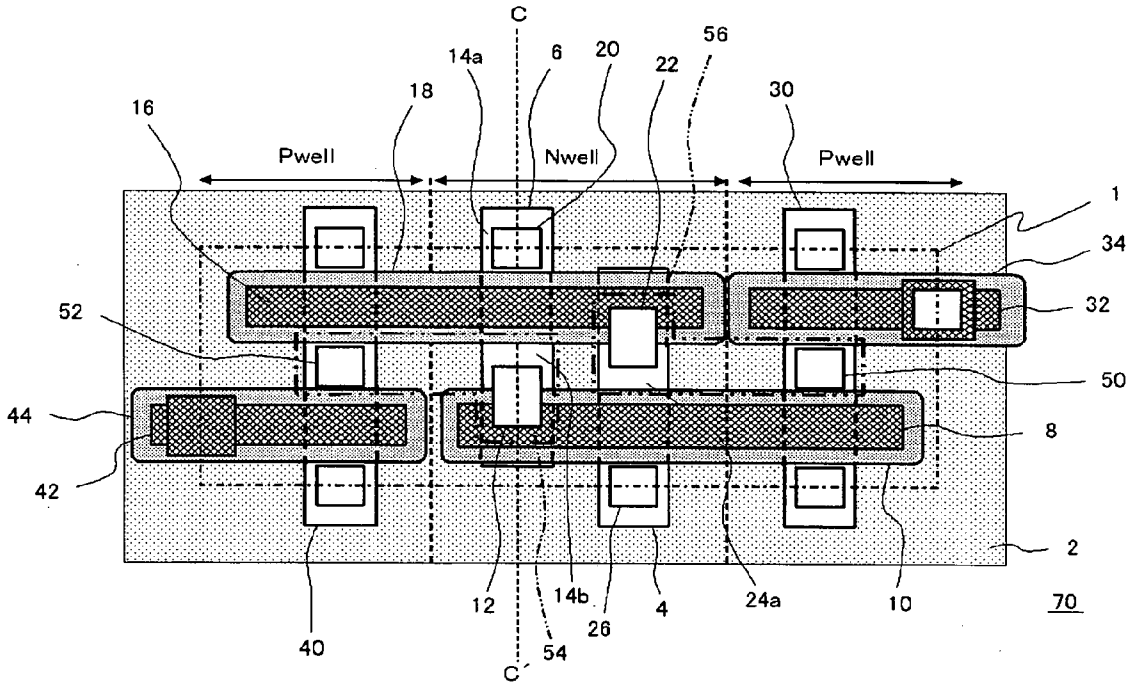

C
14a
6
20
56
22
18
30
16
Pwell
Nwell
Pwell
1
34
52
32
50
44
8
42
2
12
14b
26
4
24a
10
70
40
54
C'

FIG. 10A

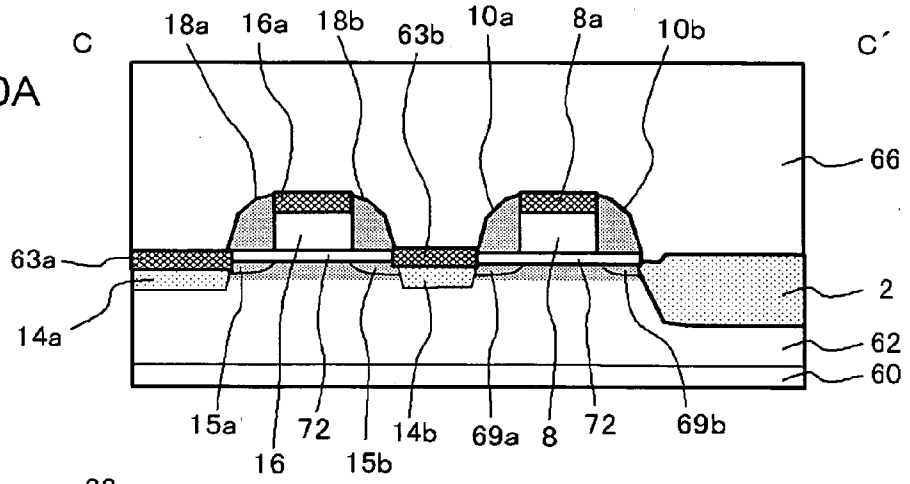


FIG. 10B

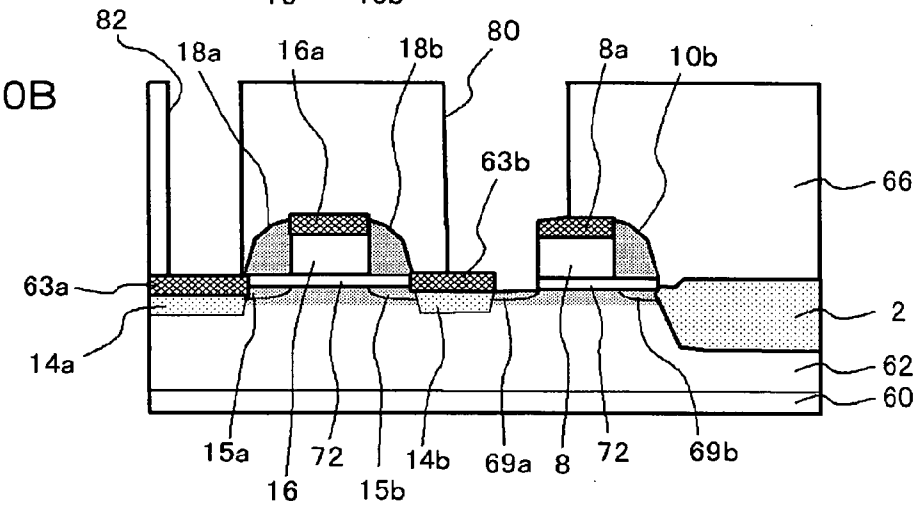


FIG. 10C

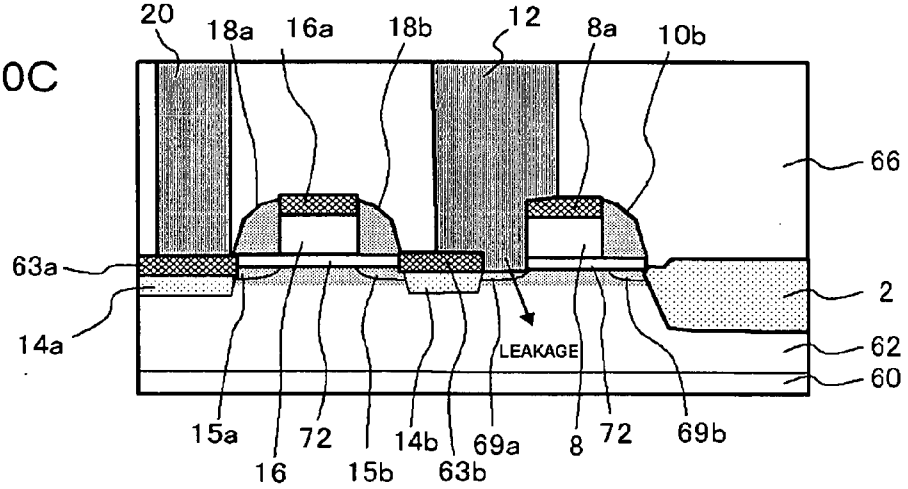


FIG. 11

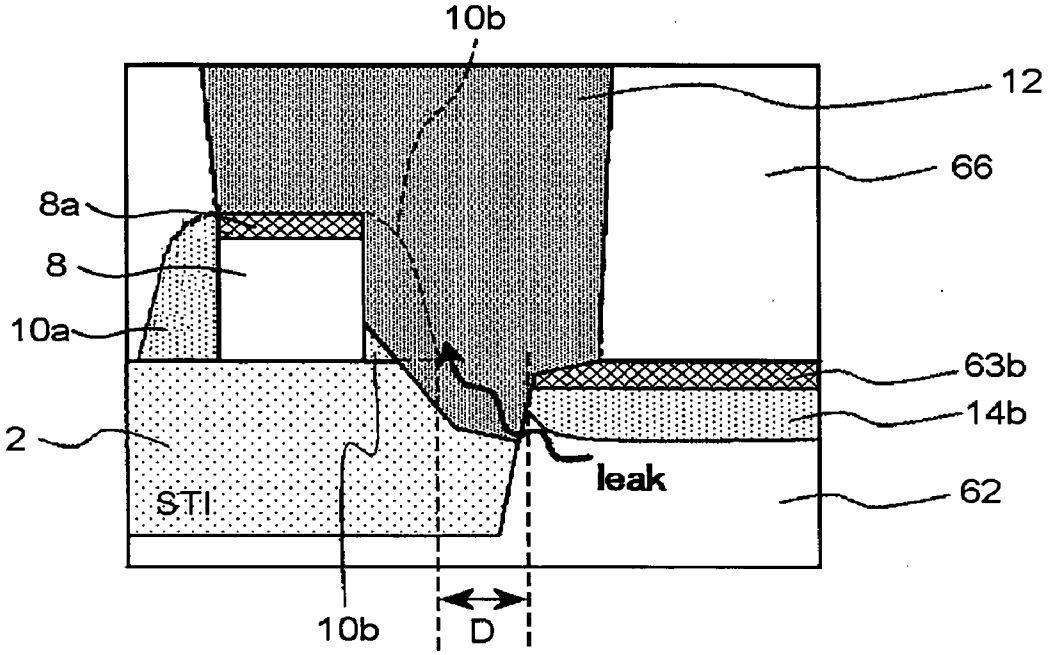
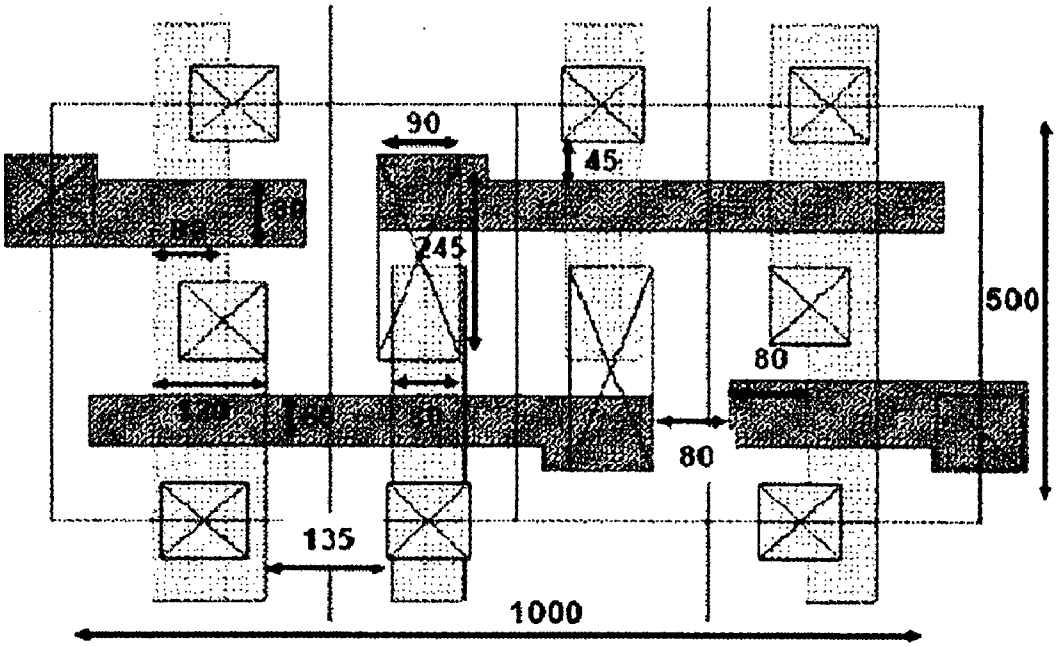


FIG. 12



SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

[0001] This application is based on Japanese patent applications No. 2005-222493 and No. 2006-159567 the contents of which are incorporated hereinto by reference.

DISCLOSURE OF THE INVENTION

TECHNICAL FIELD

[0002] The present invention relates to a semiconductor device containing a shared contact connecting a gate electrode and a impurity-diffused region, and a method of fabricating the same.

RELATED ART

[0003] Inverter circuit, for example, uses an interconnection structure electrically connecting a gate electrode of a MOS (metal-oxide-semiconductor) field effect transistor (referred to as "MOS transistor", hereinafter) and an impurity-diffused region such as source/drain region.

[0004] Japanese Laid-Open Patent Publication No. H7-115198 discloses a local interconnection structure connecting a gate electrode formed on a field oxide film and a source/drain region. Japanese Laid-Open Patent Publication No. S61-168265 and Japanese Laid-Open Patent Publication No. 2002-270701 disclose semiconductor devices each having an electrode interconnection formed in the field region, configured so that, when the contact window laid on both of the electrode interconnection and the source/drain region is opened, the end portion of the field region exposed in the contact window is covered with a sidewall formed on the side face of the electrode interconnection, so as to prevent a field insulating film from being etched and to prevent a silicon substrate from being exposed, even when an interlayer insulating film on the source/drain and on the electrode interconnection is etched.

[0005] On the other hand, F. Arnaud et al., "Low Cost 65 nm CMOS Platform for Low Power & General Purpose Applications", 2004 Symposium on VLSI Technology Digest of Technical Papers, p10-11, (2004) (see FIG. **2** and FIG. **7**) discloses a structure having an impurity-diffused layer and a gate electrode connected with each other through a shared contact, wherein a region below the gate electrode is configured using an STI (shallow trench isolation).

[0006] FIG. **9** is a top view of a semiconductor device **70** containing an SRAM.

[0007] The drawing herein shows a configuration of a unit cell **1** of an SRAM (static random access memory). The unit cell **1** contains a semiconductor region **4** and a semiconductor region **6** formed in an N-well, a semiconductor region **30** and a semiconductor region **40** formed in a P-well, and an element-isolating insulating film **2** isolating them. The semiconductor region **30** has, formed therein, an n-type MOS transistor containing a gate electrode **32**, and an n-type MOS transistor containing a gate electrode **8**. The semiconductor region **40** has, formed therein, an n-type MOS transistor containing a gate electrode **42**, and an n-type MOS transistor containing a gate electrode **16**. The semiconductor region **4** has, formed therein, a p-type transistor containing the gate electrode **8**, and a shared contact **22** electrically connecting a source/drain region **24***a* and the gate electrode **16** of the transistor. The semiconductor region **6** has, formed therein, a p-type transistor containing the gate electrode **16**, and a shared contact **12** electrically connecting a source/drain region **14***b* and the gate electrode **8** of the transistor. In the periphery of the gate electrode **8**, the gate electrode **16**, the gate electrode **32** and the gate electrode **42**, there are formed a sidewall **10**, a sidewall **18**, a sidewall **34**, and a sidewall **44**, respectively.

[0008] In the semiconductor region **30**, a contact is formed on the source/drain region between the gate electrode **32** and the gate electrode **8**. On the contact **50** and the shared contact **22**, an interconnection **56** (indicated by a two-dot chain line in the drawing) electrically connecting the both is formed. In the semiconductor region **40**, on the source/drain region between the gate electrode **42** and the gate electrode **16**, a contact **52** is formed so as to electrically connecting them. On the contact **52** and the shared contact **12**, there is formed an interconnection **54** electrically connecting them (indicated by a two-dot chain line in the drawing). It is to be noted herein that FIG. **9** indicates the semiconductor regions formed below the gate electrodes and the sidewalls using dashed lines, for simplicity in understanding.

[0009] A procedure of fabricating such semiconductor device **70** will be explained referring to FIGS. **10**A to **10**C. FIGS. **10**A to **10**C are corresponding to the C-C' section of FIG. **9**.

[0010] First, an element-isolating insulating film **2** is formed in a semiconductor substrate **60**. An N-well **62** is then formed by well implantation, followed by channel implantation. A gate insulating film **72** is then formed on the surface of the N-well **62**, then a polysilicon layer is formed over the entire surface. The polysilicon layer is then etched to form a gate pattern, to thereby form the gate electrode **16** and the gate electrode **8**. Next, impurity ion is implanted using the gate electrode **16** and the gate electrode **8** as a mask, to thereby form source/drain extension regions **15***a*, **15***b*, **69***a* and **69***b*.

[0011] An insulating film later remained as the sidewall is then formed over the entire surface, and then etched back to thereby form sidewalls **18***a*, **18***b*, **10***a* and **10***b*. Then using these sidewalls **18***a*, **18***b*, **10***a* and **10***b* as a mask, ion implantation is carried out to thereby form a source/drain region **14***a* and a source/drain region **14***b*. The source/drain region **14***a* and the source/drain region **14***b* are formed as having an impurity concentration higher than that of the source/drain extension regions **15***a*, **15***b*, **69***a* and **69***b*.

[0012] Next, a metal film is formed over the entire surface, and then annealed to thereby selectively form silicide layers **63***a*, **63***b*, **16***a* and **8***a* on the top surfaces of the source/drain region **14***a*, the source/drain region **14***b*, the gate electrode **16** and the gate electrode **8**, respectively. An interlayer insulating film **66** is then formed over the entire surface. A structure shown in FIG. **10**A is thus obtained.

[0013] Next, the interlayer insulating film **66** is selectively etched, to thereby form a contact hole **82** which reaches the silicide layer **63***a* on the source/drain region **14***a*, and a contact hole **80** which reaches the silicide layer **8***a* on the gate electrode **8** and the silicide layer **63***b* on the source/drain region **14***b*.

[0014] There has been known a problem in that, during formation of the contact hole **80**, also the sidewall **10***a* is

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readily etched, supposedly because of reasons below. First, for the case where the sidewall **10***a* is composed of a material of the same series with a material composing the interlayer insulating film **66**, also the sidewall **10***a*, together with the interlayer insulating film **66**, is likely to be etched. Because the sidewall **10***a* is formed by etch-back of the insulating film, the outer side face of the sidewall **10***a* is consequently not normal to the surface of the semiconductor substrate **60**, but slightly inclined. Any efforts of etching under conditions of selectively removing only the interlayer insulating film **66**, by composing the side wall **10***a* with a material different from that of the interlayer insulating film **66**, may therefore fail in ensuring a sufficient level of etching selectivity, so that the sidewall **10***a* may be etched. As a consequence, if several tens of thousands of unit cells **1** are formed in the semiconductor device **70**, some of them may have, as shown in FIG. **10**B, the sidewall **10***a* removed therefrom by etching.

[**0015**] Thereafter, the contact hole **82** and the contact hole **80** are filled with an electro-conductive material, to thereby form a contact **20** and the shared contact **12** (FIG. **10**C).

[**0016**] However, some of the shared contacts **12** may contact with the source/drain extension region **69***a* if the sidewall **10***a* has been removed by etching when the contact holes **80** were formed. The source/drain extension region **69***a* has an impurity concentration smaller than that of the source/drain region **14***b*, and has no silicide layer formed on the surface thereof. For this reason, a problem has been arisen in that current leakage may occur in a region where the shared contact **12** comes into contact with the source/drain extension region **69***a*. In particular, such current leakage is more likely to occur when the source/drain extension region is formed only to a small depth.

[**0017**] On the other hand, in view of micronizing the semiconductor device, there is a demand on downsizing, for example, unit cells of SRAM as possible. The conventional semiconductor device has, however, failed in suppressing the current leakage at the contact interconnecting the gate electrode and the impurity-diffused region as the micronization advances.

[**0018**] In contrast to this, the technique described by F. Arnaud et al., causes no problem of current leakage in a region where the shared contact comes into contact with the source/drain extension region, because the STI is formed below the sidewall of the gate electrode. However, as shown in FIG. **7** in the literature by F. Arnaud et al., a problem arose in that the STI in a shared contact forming region was considerably removed, and another current leakage would occur. In order to make clear understanding of this problem, FIG. **11** shows a schematic drawing of a portion around the shared contact. A gate electrode **8** having a silicide layer **8***a* formed on the surface thereof, and the source/drain region **14***b* having a silicide layer **63***b* formed on the surface thereof are connected by the shared contact **12**. Any large removal of the element-isolating insulating film (STI) **2** results in the current leakage between the well (semiconductor region) **62** and the shared contact **12**.

SUMMARY OF THE INVENTION

[**0019**] According to the present invention, there is provided a semiconductor device having a gate electrode formed on a semiconductor substrate, an impurity-diffused region formed in the surficial portion of the semiconductor substrate on one side of the gate electrode, and a shared contact electrically connecting the gate electrode and the impurity-diffused region,

[**0020**] having formed therein, when viewed in a first section taken along the gate length direction of the gate electrode, a sidewall formed on the side face on the above-described one side of the gate electrode, a source/drain extension region formed in the surficial portion of the semiconductor substrate in a self-aligned manner with respect to the gate electrode, and a source/drain region formed in a self-aligned manner with respect to the sidewall, and having an impurity concentration higher than that of the source/drain extension region,

[**0021**] wherein, when viewed in a second section along the gate length direction of the gate electrode, the gate electrode and the impurity-diffused region are disposed as being apart from each other, an element-isolating insulating film is formed over the entire surface of the semiconductor substrate exposed between the gate electrode and the impurity-diffused region, and the distance between the gate electrode and the impurity-diffused region is substantially equal to the width of the sidewall as viewed in the first section.

[**0022**] "Substantially equal" herein means a configuration including a margin to some degree inevitably produced in the fabrication process of the semiconductor device.

[**0023**] According to the present invention, there is provided also a method of fabricating a semiconductor device which has:

[**0024**] a gate electrode formed on a semiconductor substrate so as to extend in one direction;

[**0025**] a sidewall formed on the semiconductor substrate and on the side face of the gate electrode on one side of the gate electrode, as having a predetermined width; and

[**0026**] a source/drain extension formation-destined region having a predetermined width, located on the semiconductor substrate on one side of the gate electrode, so as to be adjacent to the gate electrode,

[**0027**] wherein the method has:

[**0028**] forming, on the semiconductor substrate, an element-isolating insulating film partitioning a first semiconductor region and a second semiconductor region, so that the first semiconductor region is formed on the source/drain extension formation-destined region and so that the second semiconductor region is not formed on the source/drain extension formation-destined region;

[**0029**] forming, on the semiconductor substrate, the gate electrode so as to extend in the direction from the first semiconductor region to the second semiconductor region, in adjacent to the source/drain extension formation-destined region;

[**0030**] a first impurity implanting step implanting an impurity in the surficial portion of the semiconductor substrate using the gate electrode as a mask, to thereby form a source/drain extension region in the first semiconductor region;

[0031] forming, on the semiconductor substrate, the sidewall on the side face on the above-described one side of the gate electrode;

[0032] a second impurity implanting step implanting an impurity in the surficial portion of the semiconductor substrate using the sidewall as a mask, to thereby form, in the second semiconductor region, an impurity-diffused region as being a predetermined distance apart from the gate electrode; and

[0033] forming, on the gate electrode and on the impurity-diffused region, a contact electrically connecting them with each other.

[0034] According to the present invention, even in a configuration having, in a partial region thereof, the sidewall on the side face of the gate electrode and having the source/drain extension region (or LDD: lightly doped drain) formed therebelow in a self-aligned manner, the region having the shared contact formed therein can be configured as having no source/drain extension region formed beside the gate electrode. The shared contact is no more in contact with the region having a low impurity concentration in the surficial portion of the semiconductor substrate, even if the side wall has been removed in the process of forming the contact which allows therein electrical connection of the gate electrode and the impurity-diffused region connected through the shared contact. For this reason, it is made possible to suppress the current leakage at the shared contact connecting the gate electrode and the impurity-diffused region.

[0035] In general, the impurity-diffused region such as source/drain extension region of MOS transistors is formed by implanting ion over the entire surface. Therefore the semiconductor region located beside the gate electrode of the MOS transistor containing the source/drain extension region will have the source/drain extension region having a predetermined width. In the shared contact structure connecting the gate electrode and the impurity-diffused region, micronization can be realized by shortening the distance between the gate and the impurity-diffused region. However for the case where a portion of the gate electrode, used also as the gate electrode of a MOS transistor, is used as a connection point with the shared contact, excessively shortened distance between the gate electrode and the semiconductor region will undesirably result in formation of the source/drain extension region beside the gate electrode also at the connection point with the shared contact. In this case, removal-by-etching of the sidewall in the process of formation of the contact hole will cause the problem of current leakage as described in the above. The semiconductor device and the method of fabricating the same according to the present invention are configured so as to make the distance between the gate electrode and impurity-diffused region substantially equal to the width of the sidewall, and so as to form the element-isolating insulating film under the contact in the region between the gate electrode and the impurity-diffused region. It is therefore made possible to avoid the problem of current leakage, and to realize micronization of the semiconductor device.

[0036] According to the present invention, there is provided a technique of micronizing the semiconductor device, and of suppressing current leakage at the shared contact connecting the gate electrode and the impurity-diffused region.

BRIEF DESCRIPTION OF THE DRAWINGS

[0037] The above and other objects, advantages and features of the present invention will be more apparent from the following description taken in conjunction with the accompanying drawings, in which:

[0038] FIG. **1** is a top view of a configuration of a semiconductor device according to an embodiment of the present invention;

[0039] FIG. **2** is the A-A' section of FIG. **1**;

[0040] FIG. **3** is the B-B' section of FIG. **1**;

[0041] FIGS. **4**A to **4**C, FIGS. **5**A to **5**D, and FIGS. **6**A to **6**D are sectional views sequentially showing procedures of fabrication of the semiconductor device according to the embodiment of the present invention;

[0042] FIGS. **7**A and **7**B are sectional views showing configurations of the semiconductor device according to the embodiment of the present invention;

[0043] FIGS. **8**A and **8**B are schematic drawings explaining a configuration of the semiconductor device according to the embodiment of the present invention;

[0044] FIG. **9** is a top view showing a configuration of a conventional semiconductor device;

[0045] FIGS. **10**A to **10**C are sectional views sequentially showing procedures of fabricating the conventional semiconductor device;

[0046] FIG. **11** is a schematic drawing of a portion around the shared contact of the conventional semiconductor device; and

[0047] FIG. **12** is a drawing corresponded to a conventional configuration.

DETAILED DESCRIPTION

[0048] The invention will be now described herein with reference to an illustrative embodiment. Those skilled in the art will recognize that many alternative embodiments can be accomplished using the teachings of the present invention and that the invention is not limited to the embodiment illustrated for explanatory purposes.

[0049] Paragraphs below will explain an embodiment of the present invention, referring to the attached drawings. It is to be noted that, in all drawings, any constituents commonly appear will be given with the same reference numerals, so as to appropriately omit the explanation.

[0050] FIGS. **8**A and **8**B are schematic drawings explaining a configuration of a semiconductor device **100** according to the embodiment of the present invention. FIG. **8**A is a schematic top view of the semiconductor substrate, and FIG. **8**B is a schematic top view shown in FIG. **8**A, overlaid with a sectional structure taken along a first section and a second section.

[0051] As shown in FIGS. **8**A and **8**B, a single gate electrode can serve, in one region, as the gate of the transistor having the source/drain extension region formed therein, and can provide, in another region, a site of contact with the shared contact (or common contact) making connection with the impurity-diffused region of another transistor. In this case, the source/drain extension formation-

destined region in which the source/drain extension region will be formed later, is formed beside the gate electrode, if the semiconductor region is exposed there. Hereinafter, a region below the sidewall formed on the side face of the gate electrode is defined as the source/drain extension formation-destined region. In ion implantation, any exposed semiconductor region in the source/drain extension formation-destined region will have the source/drain extension region formed therein.

[**0052**] In this embodiment, the element-isolating insulating film is formed over the entire surface of the source/drain extension formation-destined region at the site of formation of shared contact. Therefore, the source/drain extension region will never be formed in the source/drain extension formation-destined region at the site of formation of shared contact. By virtue of this configuration, the shared contact will never be connected to the source/drain extension region even if the sidewall on the source/drain extension formation-destined region is removed at the site of formation of shared contact. As can be understood from the above, the current leakage, anticipated when the impurity-diffused region source/drain region and the gate electrode is connected through the shared contact, can be suppressed.

[**0053**] The semiconductor device of this embodiment can be configured also as having two gate electrodes disposed almost in parallel with each other on the semiconductor substrate. On the side portions between two these gate electrodes, the source/drain extension formation-destined regions are respectively located. In a first section, one gate electrode functions as the gate electrode of a transistor, and the other gate electrode provides a site of contact with the shared contact making connection with the source/drain diffusion region of the transistor. In a second section, the other gate electrode serves as the gate electrode of a transistor, and one gate electrode provides a site of contact with the shared contact making connection with the source/drain diffusion region of the transistor. In the second section, the other sidewall is formed on the source/drain extension formation-destined region on the side of the other transistor. In the first section, the above-described other gate electrode and the source/drain region are disposed as being apart from each other, the element-isolating insulating film is formed over the entire surface of the semiconductor substrate exposed between the above-described other gate electrode and the source/drain region, and the distance between the above-described other gate electrode and the source/drain region is substantially equal to the width of the other sidewall as viewed in the second section. By virtue of this configuration, the current leakage at the individual shared contacts can be suppressed, even in a configuration having the source/drain region of one transistor is connected to the gate electrode of the other transistor, and the gate electrode of one transistor is connected to the source/drain region of the other transistor.

[**0054**] In the embodiment of the present invention, the semiconductor device can be configured as having a plurality of combinations of the gate electrode, the shared contact and the source/drain extension region in a predetermined region, and as having all of the shared contacts contained in the predetermined region being not in contact with the source/drain extension region. The predetermined region herein may be, for example, a unit cell of SRAM.

[**0055**] FIG. **1** is a top view of the semiconductor device **100** according to the embodiment of the present invention. The semiconductor device **100** contains SRAMs. The drawing herein shows a configuration of a unit cell **101**.

[**0056**] The unit cell **101** contains a semiconductor region **104** and a second semiconductor region **106** formed in an N-well, a third semiconductor region **130** and a fourth semiconductor region **140** formed in a P-well, and an element-isolating insulating film **102** isolating them. The third semiconductor region **130** has, formed therein, an n-type MOS transistor Tr**1** having a third gate electrode **132**, and an n-type MOS transistor Tr**2** having the first gate electrode **108**. The fourth semiconductor region **140** has, formed therein, an n-type MOS transistor Tr**3** having a fourth gate electrode **142**, and an n-type MOS transistor Tr**4** having a second gate electrode **116**.

[**0057**] The first semiconductor region **104** has, formed therein, a p-type transistor Tr**5** having a first gate electrode **108**, and a shared contact **122** electrically connecting a first source/drain region **124***a* and the second gate electrode **116** of the p-type transistor Tr**5**. The second semiconductor region **106** has, formed therein, a p-type transistor Tr **6** having the second gate electrode **116** and a shared contact **112** electrically connecting a fourth source/drain region **114***b* and the first gate electrode **108** of the p-type transistor Tr**6**. The first gate electrode **108**, the second gate electrode **116**, the third gate electrode **132** and the fourth gate electrode **142** have a sidewall **110**, a sidewall **118**, a sidewall **134** and a sidewall **144**, respectively, formed therearound.

[**0058**] In the third semiconductor region **130**, a contact **150***b* is formed on the source/drain region between the third gate electrode **132** and the first gate electrode **108**, and on the contact **150***b* and the shared contact **122**, an interconnection **156** (indicated by two-dot chain line in the drawing) electrically connecting them is formed. In the fourth semiconductor region **140**, a contact **152***b* is formed on the source/drain region between the fourth gate electrode **142** and the second gate electrode **116** so as to connect them, and on the contact **152***b* and the shared contact **112**, an interconnection **154** (indicated by two-dot chain line in the drawing) electrically connecting them is formed. The third semiconductor region **130** has a contact **150***a* and a contact **150***c* formed therein, and the fourth semiconductor region **140** has a contact **152***a* and a contact **152***c* formed therein, respectively. The third gate electrode **132** has a contact **136** formed thereon, and the fourth gate electrode **142** has a contact **146** formed thereon. It is to be understood that FIG. **1** indicates the semiconductor regions formed under the gate electrodes, under the sidewalls and under the shared contacts using broken lines, for better understanding.

[**0059**] Layout of the first semiconductor region **104** and the second semiconductor region **106** in the semiconductor device **100** according to the embodiment of the present invention differs from that of the semiconductor region **4** and the semiconductor region **6** in the conventional semiconductor device **70** explained referring to FIG. **9**, but layouts of other constituents are same.

[**0060**] In the embodiment of the present invention, the p-type transistor Tr**5** and the p-type transistor Tr**6** are configured so that the gate electrodes of which are electrically connected to the source/drain regions of the other. More specifically, the first gate electrode **108** functions as

the gate electrode of the p-type transistor Tr**5** in the first semiconductor region **104**, and is connected with the fourth source/drain region **114***b* of the p-type transistor Tr**6** through the shared contact **112**, in the section containing the second semiconductor region **106**, taken along the gate length direction. Similarly, the second gate electrode **116** functions as the gate electrode of the p-type transistor Tr**6** in the second semiconductor region **106**, and is connected with the first source/drain region **124***a* of the p-type transistor Tr**5**, in the section containing the first semiconductor region **104**, taken along the gate length direction. The section taken along the gate length direction (A-A' section, second section) in the second semiconductor region **106**, and the section taken along the gate length direction (B-B' section, first section) in the first semiconductor region **104** are configured as being nearly symmetrical with each other.

[**0061**] FIG. **2** is the A-A' section of FIG. **1**.

[**0062**] The semiconductor device **100** has a semiconductor substrate **160**, an N-well **162** formed therein, and an element-isolating insulating film **102** formed in the N-well **162** and partitioning the second semiconductor region **106**. The N-well **162** has the p-type transistor Tr**6** disposed thereon, and the element-isolating insulating film **102** has, disposed thereon, a first gate electrode **108** having a silicide layer **108***a* formed thereon. The p-type transistor Tr**6** is composed of a gate insulating film **172**, a second gate electrode **116** having a silicide layer **116***a* formed on the top portion thereof, a side wall **118***a* and a sidewall **118***b* (sidewalls **118**) formed on the side faces of the second gate electrode **116**, a source/drain extension region **115***a* and a source/drain extension region **115***b* formed respectively under the sidewall **118***a* and the sidewall **118***b*, and a third source/drain region **114***a* and a fourth source/drain region **114***b* formed on both sides thereof. The third source/drain region **114***a* and the fourth source/drain region **114***b* have a silicide layer **163***a* and a silicide layer **163***b* respectively formed on the top portions thereof. On one side face of the first gate electrode **108**, a second sidewall **110***b* (sidewall **110**) is provided.

[**0063**] The semiconductor device **100** also includes an etching stopper insulating film **164** formed on the p-type transistor Tr**6** and the first gate electrode **108**, an interlayer insulating film **166** formed thereon, and an interlayer insulating film **168** formed further thereon. The interlayer insulating film **166** and the etching stopper insulating film **164** have, formed therein, a contact hole opened over a region ranging from the silicide layer **163***b* to the silicide layer **108***a*, and the shared contact **112** is formed in the contact hole. The interlayer insulating film **166** and the etching stopper insulating film **164** have, formed therein, also a contact **120** making contact with the silicide layer **163***a* of the p-type transistor Tr**6**. The contact **120** and the shared contact **112** are respectively connected to an interconnection **155** and an interconnection **154** formed in the interlayer insulating film **168**.

[**0064**] FIG. **3** is the B-B' section of FIG. **1**.

[**0065**] The p-type transistor Tr**5** is disposed on the N-well **162** partitioned as the first semiconductor region **104** by the element-isolating insulating film **102**, and the second gate electrode **116** is disposed on the element-isolating insulating film **102**. The p-type transistor Tr**5** is composed of a gate insulating film **173**, a first gate electrode **108** having the silicide layer **108***a* formed on the top portion thereof, a first sidewall **110***a* and the second sidewall **110***b* formed on the side faces of the first gate electrode **108**, a source/drain extension region **169***a* and a source/drain extension region **169***b* respectively formed under the first sidewall **110***a* and the second sidewall **110***b*, and the first source/drain region **124***a* and the second source/drain region **124***b* formed on both sides thereof. The first source/drain region **124***a* and the second source/drain region **124***b* have a silicide layer **165***a* and a silicide layer **165***b* respectively formed thereon. On one side face of the second gate electrode **116**, the sidewall **118***a* is provided.

[**0066**] The interlayer insulating film **166** and the etching stopper insulating film **164** have, formed therein, a contact hole opened over a region ranging from the silicide layer **165***a* to the silicide layer **116***a*, and the shared contact **122** is formed in the contact hole. The interlayer insulating film **166** and the etching stopper insulating film **164** have, formed therein, a contact **126** making contact with the silicide layer **165***b* of the p-type transistor Tr**5**. The shared contact **122** and the contact **116** are respectively connected to an interconnection **156** and an interconnection **157** formed in the interlayer insulating film **168**.

[**0067**] The distance "d" between the first gate electrode **108** and the fourth source/drain region **114***b* shown in FIG. **2** is made substantially equal to the width "d" of the first sidewall **110***a* shown in FIG. **3**. As shown in FIG. **2**, the element-isolating insulating film **102** is formed in a region between the first gate electrode **108** and the fourth source/drain region **114***b*.

[**0068**] Similarly, also the distance between the second gate electrode **116** and the first source/drain region **124***a* shown in FIG. **3** is made substantially equal to the width of the sidewall **118***b* shown in FIG. **2**.

[**0069**] Paragraphs below will describe process steps of fabricating the semiconductor device **100** of this embodiment, referring to FIG. **4**A to FIG. **6**D. The explanation herein will be made referring to the A-A' section of FIG. **1**, similarly as shown in FIG. **2**. As described in the above, the A-A' section and the B-B' section of the semiconductor device **100** shown in FIG. **1** show nearly symmetrical configurations, so that in the process steps of fabrication described below, the p-type transistor Tr**5** has a configuration similar to that of the p-type transistor Tr**6**.

[**0070**] First, the element-isolating insulating film **102** is formed in the semiconductor substrate **160** which is typically a silicon substrate. The element-isolating insulating film **102** can be configured as an STI (shallow trench isolation). The element-isolating insulating film **102** can be formed by forming a recess (not shown) in the semiconductor substrate **160**, forming an insulating film such as a silicon oxide film over the entire surface of the semiconductor substrate **160**, and by removing a portion of the insulating film exposed outside the recess by CMP (chemical mechanical polishing). In this process, the element-isolating insulating film **102** is formed so as to partition the second semiconductor region **106**, so that the width of the source/drain extension formation-destined region between the gate electrode forming region in which the first gate electrode **108** will be formed in the later process step, and the second semiconductor region **106** is adjusted substantially equal to the width of the first sidewall **110***a* formed on the side face of the first gate electrode **108**.

[0071] Next, the N-well **162** is formed by well-forming ion implantation, and a channel region **170** is then formed by channel-forming ion implantation. Thereafter the gate insulating film **172** is formed on the surface of the N-well **162** (FIG. **4**A). Next, a polysilicon layer **174** is formed over the entire surface (FIG. **4**B). The polysilicon layer **174** is then etched to obtain a gate pattern, to thereby form the second gate electrode **116** and the first gate electrode **108** (FIG. **4**C).

[0072] Thereafter, ion is implanted using the second gate electrode **116** and the first gate electrode **108** as a mask, to thereby form the source/drain extension region **115***a* and the source/drain extension region **115***b* in the surficial portion of the N-well **162** (FIG. **5**A). In this process, as shown in the B-B' section in FIG. **3**, also the source/drain extension region **169***a* and the source/drain extension region **169***b* are formed in a self-aligned manner on both sides of the first gate electrode **108**. However, as shown in the A-A' section in FIG. **5**A, the element-isolating insulating film **102** is formed between the second semiconductor region **106** and the first gate electrode **108**. In addition, the first gate electrode **108** is formed on the element-isolating insulating film **102**, so that the source/drain extension regions are never formed on both sides of the first gate electrode **108**, in a region containing the A-A' section.

[0073] Next, an insulating film **176**, later processed to give the sidewalls, is formed over the entire surface (FIG. **5**B). The insulating film **176** can be configured by using a silicon oxide film or a silicon nitride film. Next, the insulating film **176** is anisotropically etched so as to respectively form the sidewall **118***a* and the sidewall **118***b* on both side faces of the second gate electrode **116**, and to form the first sidewall **110***a* and the second sidewall **110***b* on both side faces of the first gate electrode **108** (FIG. **5**C). In this embodiment, as described in the above, the element-isolating insulating film **102** is formed so that the distance between the first gate electrode **108** and the second semiconductor region **106** will be substantially equal to the width of the first sidewall **110***a*. As shown by the section in FIG. **5**C, the element-isolating insulating film **102** is formed under the first sidewall **110***a*.

[0074] Ion is then implanted using the sidewall **118***a*, the sidewall **118***b* and the first sidewall **110***a* as a mask, to thereby form the third source/drain region **114***a* and the fourth source/drain region **114***b* (FIG. **5**D). As a consequence, the fourth source/drain region **114***b*, having an impurity concentration higher than that of the source/drain extension region such as the source/drain extension region **169***a*, is formed in a region of the second semiconductor region **106** adjacent to the element-isolating insulating film **102**. In this process, as shown by the B-B' section in FIG. **3**, the first source/drain region **124***a* and the second source/drain region **124***b* are formed using the first sidewall **110***a* and the second sidewall **110***b* as a mask. It is to be noted that the fourth source/drain region **114***b* in the second semiconductor region **106** and the first source/drain region **124***a* in the first semiconductor region **104** are formed at the same time by ion implantation as shown in FIG. **5**A and ion implantation as shown in FIG. **5**D, so that they have an identical impurity concentration profile over the entire range thereof in the depth-wise direction and in the gate length direction.

[0075] Next, a metal film is formed over the entire surface, and then annealed to thereby selectively form silicide layers **163***a*, **163***b*, **116***a* and **108***a* on the top surfaces of the third source/drain region **114***a*, the fourth source/drain region **114***b*, the second gate electrode **116** and the first gate electrode **108**, respectively (FIG. **6**A). Provision of such silicide layers is successful in lowering the electric resistance of the semiconductor device **100**. It is also made possible to prevent the current leakage in the shared contact **112** from occurring.

[0076] Next, the etching stopper insulating film **164** is formed over the entire surface. The etching stopper insulating film **164** may be composed of a material different from those composing the element-isolating insulating film **102** and the interlayer insulating film **166**. As a consequence, the element-isolating insulating film **102** can be prevented from being etched in the later process of forming the contact hole in a region ranging from the fourth source/drain region **114***b* to the first gate electrode **108**. The interlayer insulating film **166** is then formed on the etching stopper insulating film **164** (FIG. **6**B). The interlayer insulating film **166** may be formed typically by using a silicon oxide film.

[0077] Next, the interlayer insulating film **166** is selectively removed, to thereby form the a contact hole **182** which communicates with the silicide layer **163***a* on the third source/drain region **114***a*, and a contact hole **180** opened over a region ranging from the silicide layer **163***b* on the fourth source/drain region **114***b* to the silicide layer **108***a* on the first gate electrode **108** (FIG. **6**C). Procedures for forming the contact hole **180** will be described later.

[0078] The contact hole and **182** the contact hole **180** are then filled with an electro-conductive material to thereby form the contact **120** and the shared contact **112** (FIG. **6**D). Next, the interlayer insulating film **168** is formed on the interlayer insulating film **166**, etched according to a predetermined pattern to thereby form therein interconnection trenches, and the interconnection trenches are filled with an interconnection material, to thereby form the interconnection **155** and the interconnection **154** connected to the contact **120** and the shared contact **112**, respectively. The semiconductor device **100** configured as shown in FIG. **2** is thus obtained.

[0079] The contact hole **180** explained referring to FIG. **6**C is formed by the procedures below. First, using a resist film already patterned according to a predetermined geometry, the interlayer insulating film **166** is selectively dry-etched. In this process, the etching stopper insulating film **164** is already formed over the entire surface under the interlayer insulating film **166**. Etching of the interlayer insulating film **166** can therefore be stopped on the etching stopper insulating film **164**, if the etching is proceeded under a condition of ensuring a large etching selectivity with respect to the etching stopper insulating film **164**. Then the etching stopper insulating film **164** is selectively removed under a condition of ensuring a large etching selectivity with respect to the first sidewall **110***a* and the element-isolating insulating film **102**, and thereby the contact hole can be formed while leaving the first sidewall **110***a* unremoved on the side face of the first gate electrode **108**. FIG. **7**A shows a configuration of the unit cell **101** having the first sidewall **110***a* left unremoved on the side face of the first gate electrode **108**, even after the etching for forming the contact hole **180**.

[0080] However, on the first sidewall **110***a*, the etching stopper insulating film **164** formed thereon may sometimes

be etched when the interlayer insulating film **166** is etched, because the first sidewall **110***a* has a slightly inclined geometry, rather than a vertical geometry, with respect to the surface of the semiconductor device **100** as described in the above. This case may sometimes result in etching of the first sidewall **110***a* at the same time. As a consequence, for the case where the semiconductor device **100** contains several tens of thousands of unit cells **101**, as shown in FIG. **6**C, some of the unit cells **101** may be obtained as having the first sidewall **110***a* completely removed therefrom, or may be obtained as having a portion of the first sidewall **110***a* removed therefrom, thereby having a region between the first gate electrode **108** and the fourth source/drain region **114***b* where the shared contact **112** and the element-isolating insulating film **102** are brought into direct contact (FIG. **7**B).

[**0081**] In this embodiment, in a region containing the A-A' section, the element-isolating insulating film **102** is formed in the source/drain extension formation-destined region under the first sidewall **110***a*, so as to contact with the fourth source/drain region **114***b* and the silicide layer **163***b* formed thereon. Therefore, the shared contact **112** will never contact with the source/drain extension region having a low impurity concentration, even if the first sidewall **110***a* is removed when the contact hole **180** is formed, so that the current leakage is avoidable.

[**0082**] The semiconductor device **100** of the present invention is configured so as to avoid a problem of current leakage, so as to equalize the distance between the fourth source/drain region **114***b* and the first gate electrode **108** with the width of the first sidewall **110***a* as viewed in a region containing the A-A' section, and so as to form the element-isolating insulating film in the surficial portion of the semiconductor substrate **160** in this region, to thereby realize micronization of the semiconductor device **100**.

[**0083**] As is obvious from comparison of the semiconductor device **100** of this embodiment shown in FIG. **1** with the semiconductor device **70** shown in FIG. **9**, the above-described problem of current leakage can be solved only by altering a partition layout of the second semiconductor region **106** and the first semiconductor region **104** by the element-isolating insulating film **102**, without altering layout of another element. It is also made possible to avoid direct contact between the shared contact and the low-impurity-concentration region in the surficial portion of the semiconductor substrate **160** even when misalignment should occur, by partitioning the first semiconductor region **104** and the second semiconductor region **106** using the element-isolating insulating film **102**, and by disposing, at the common-contact-forming site, the first gate electrode **108** and the second gate electrode **116** on the element-isolating insulating film **102**.

[**0084**] Comparing now the configurations described in the present invention and described by F. Arnaud et al., the configuration described by F. Arnaud et al. has, in the common-contact-forming region, the element-isolating insulating film not covered by the sidewall. The element isolating region is therefore likely to be etched when the interlayer insulating film is etched, and tends to show a largely-notched geometry of the element-isolating insulating film (STI) **2** as shown in FIG. **11**. This problem will become more distinctive unless the etching stopper insulating film **164** described in the above embodiment is used, and will be causative of leakage current. In contrast to this, the present invention can suppress the amount of removal of the element-isolating insulating film in the shared contact region.

[**0085**] The present invention can also reduce the cell area as compared with that of the SRAM described by F. Arnaud et al. Based on the scale given on the SEM photograph in FIG. **7** of the literature by F. Arnaud et al., the length D of the element-isolating insulating film (STI) **2** projecting out from the edge of the side wall **10***b* into the source/drain region **14***b* shown in FIG. **11** can be estimated as approximately 35 nm.

[**0086**] FIG. **12** is a drawing corresponded to FIG. **2** in the literature by F. Arnaud et al. According to the present invention, the distance between the gate electrode and the impurity-diffused region, connected with each other by the shared contact, is substantially same as the width of the sidewall, so that the length in the longitudinal direction of the shared contact of the SRAM unit cell in the layout shown in FIG. **12** of the literature by F. Arnaud et al. can be shortened by 35 nm×2=70 nm or around. Amount of reduction in the area of the SRAM unit cell is calculated as 1 μm×(0.035×2) μm=0.07 μm^2. This means a rate of reduction of approximately 14%, because the SRAM unit cell without adopting the present invention has an area of 0.5 μm^2. The present invention is, therefore, effective also in reduction in the cell area, that is, micronization of the semiconductor device.

[**0087**] The embodiment of the present invention has been described in the above merely for exemplary purposes, while allowing adoption of any other configurations.

[**0088**] The embodiment in the above has explained a case where the element-isolating insulating film **102** was configured as STI, whereas the element-isolating insulating film **102** can be configured also as a LOCOS (local oxidation of silicon) film. The element-isolating insulating film **102** configured as STI can be formed also by forming a recess in the semiconductor substrate **160**, forming for example a first insulating film on the side face of the recess, and filling the recess with a second insulating film different from the first insulating film. In this case, the first insulating film may be a silicon nitride film, and the second insulating film may be a silicon oxide film. Provision of such first insulating film on the side face of the element-isolating insulating film **102** makes it possible to control the element-isolating insulating film **102** so that the end portion thereof is not etched.

[**0089**] Although the embodiment in the above exemplified an SRAM, the present invention is also applicable to various semiconductor devices other than SRAM, such as flipflop structure, containing shared contact allowing therein connection of the gate electrode and the impurity-diffused region.

[**0090**] The embodiment in the above explained an exemplary case where the p-type transistor and the shared contact were formed in the N-well, but an n-type transistor and the shared contact can be formed in a P-well in a similar manner.

[**0091**] It is apparent that the present invention is not limited to the above embodiment, that may be modified and changed without departing from the scope and spirit of the invention.

1. A semiconductor device comprising a gate electrode formed on a semiconductor substrate, an impurity-diffused

region formed in the surficial portion of said semiconductor substrate on one side of said gate electrode, and a shared contact electrically connecting said gate electrode and said impurity-diffused region,

having formed therein, when viewed in a first section taken along the gate length direction of said gate electrode, a sidewall formed on the side face on said one side of said gate electrode, a source/drain extension region formed in the surficial portion of said semiconductor substrate in a self-aligned manner with respect to said gate electrode, and a source/drain region formed in a self-aligned manner with respect to said sidewall, and having an impurity concentration higher than that of said source/drain extension region,

wherein, when viewed in a second section along the gate length direction of said gate electrode, said gate electrode and said impurity-diffused region are disposed as being apart from each other, an element-isolating insulating film is formed over the entire surface of said semiconductor substrate exposed between said gate electrode and said impurity-diffused region, and the distance between said gate electrode and said impurity-diffused region is substantially equal to the width of said sidewall as viewed in said first section.

2. The semiconductor device according to claim 1, wherein said impurity-diffused region as viewed in said second section has an impurity concentration profile same as that of said source/drain region as viewed in said first section.

3. The semiconductor device according to claim 1 wherein, when viewed in said second section, said impurity-diffused region contains a silicide layer formed on the surface thereof, and said shared contact contacts with said silicide layer.

4. The semiconductor device according to claim 1, further comprising:

an etching stopper insulating film formed, when viewed at least in said second section, so as to cover said impurity-diffused region and said gate electrode, and composed of a material different from that composing said element-isolating insulating film; and

an interlayer insulating film formed on said etching stopper insulating film, and composed of a material different from that composing said etching stopper insulating film,

wherein said shared contact is formed on said impurity-diffused region and said gate electrode, using an electro-conductive material filled in a contact hole formed in said interlayer insulating film and said etching stopper insulating film.

5. The semiconductor device according to claim 1, wherein, when viewed along said second section, said shared contact and said element-isolating insulating film are brought into direct contact, between said gate electrode and said impurity-diffused region.

6. The semiconductor device according to claim 1, wherein, when viewed along said second section, said element-isolating insulating film is formed so as to extend into a region containing a portion under said gate electrode, and said gate electrode is formed on said element-isolating insulating film.

7. The semiconductor device according to claim 1, further comprising another gate electrode formed on said semiconductor substrate on said one side of said gate electrode, so as to extend in parallel with said gate electrode from a region containing said first section to a region containing said second section, and another shared contact electrically connecting, when viewed along said first section, said another gate electrode and said source/drain region,

having formed therein, when viewed along said second section, another sidewall formed on the side face of said another gate electrode on one side opposing to said gate electrode, and another source/drain extension region formed in the surficial portion of said semiconductor substrate in a self-aligned manner with respect to said another gate electrode, said impurity-diffused region being formed so as to contact with said another source/drain extension region, in a self-aligned manner with respect to said another sidewall, and

having formed therein, when viewed along said first section, said another gate electrode and said source/drain region disposed as being apart from each other, an element-isolating insulating film formed over the entire surface of said semiconductor substrate exposed between said another gate electrode and said source/drain region, the distance between said another gate electrode and said source/drain region being substantially equal to the width of said another sidewall as viewed in said second section.

8. The semiconductor device according to claim 1, configured:

so as to contain, in a predetermined region, a plurality of combinations of said gate electrode, said shared contact, and said source/drain extension region; and

so that all of said shared contacts contained in said predetermined region do not contact with said source/drain extension region.

9. A method of fabricating a semiconductor device comprising:

a gate electrode formed on a semiconductor substrate so as to extend in one direction;

a sidewall formed on said semiconductor substrate and on the side face of said gate electrode on one side of said gate electrode, as having a predetermined width; and

a source/drain extension formation-destined region having a predetermined width, located on said semiconductor substrate on one side of said gate electrode, so as to be adjacent to said gate electrode,

wherein the method comprising:

forming, on said semiconductor substrate, an element-isolating insulating film partitioning a first semiconductor region and a second semiconductor region, so that said first semiconductor region is formed on said source/drain extension formation-destined region and so that said second semiconductor region is not formed on said source/drain extension formation-destined region;

forming, on said semiconductor substrate, said gate electrode so as to extend in the direction from said first

semiconductor region to said second semiconductor region, in adjacent to said source/drain extension formation-destined region;

a first impurity implanting step implanting an impurity in the surficial portion of said semiconductor substrate using said gate electrode as a mask, to thereby form a source/drain extension region in said first semiconductor region;

forming, on said semiconductor substrate, said sidewall on the side face on said one side of said gate electrode;

a second impurity implanting step implanting an impurity in the surficial portion of said semiconductor substrate using said sidewall as a mask, to thereby form, in said second semiconductor region, an impurity-diffused region as being a predetermined distance apart from said gate electrode by; and

forming, on said gate electrode and on said impurity-diffused region, a contact electrically connecting them with each other.

10. The method of fabricating a semiconductor device according to claim 9,

further comprising, posterior to said second impurity implantation step, selectively forming a silicide layer on the surface of said second semiconductor region,

wherein, in said forming said contact, said contact is formed on said silicide layer.

11. The method of fabricating a semiconductor device according to claim 9,

further comprising, prior to said forming said contact, forming an interlayer insulating film over the entire surface of said semiconductor substrate,

said forming said contact comprising:

forming, in said interlayer insulating film, a contact hole opened over a region ranging from said gate electrode to said impurity-diffused region; and

filling said contact hole with an electro-conductive material.

12. The method of fabricating a semiconductor device according to claim 11,

further comprising, prior to said forming said interlayer insulating film, forming an etching stopper insulating film composed of a material different from that composing said element-isolating insulating film, on the entire surface of said semiconductor substrate,

wherein, in said forming said contact hole, said contact hole is formed in said interlayer insulating film and said etching stopper insulating film.

13. The semiconductor device according to claim 2, wherein, when viewed along said second section, said shared contact and said element-isolating insulating film are brought into direct contact, between said gate electrode and said impurity-diffused region.

14. The semiconductor device according to claim 3, wherein, when viewed along said second section, said shared contact and said element-isolating insulating film are brought into direct contact, between said gate electrode and said impurity-diffused region.

15. The semiconductor device according to claim 4, wherein, when viewed along said second section, said shared contact and said element-isolating insulating film are brought into direct contact, between said gate electrode and said impurity-diffused region.

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