

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNITED MICROELECTRONICS CORPORATION,
AND
UMC GROUP (USA),
Petitioners,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,
Patent Owner.

Case No. IPR2025-01090
U.S. Patent 8,907,425

**DECLARATION OF DR. SANJAY BANERJEE IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,907,425**

UMC 1101

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Declaration of Dr. Sanjay Banerjee
Inter Partes Review of U.S. Patent No. 8,907,425

I, Dr. Sanjay Banerjee, declare as follows:

1. My name is Sanjay Banerjee.
2. I have been retained as an expert witness on behalf of United Microelectronics Corporation and UMC Group (USA) (collectively, “Petitioner”) for the above-captioned Petition for *Inter Partes* Review (“IPR”) (“Petition”) of U.S. Patent No. 8,907,425 (“the ’425 patent”) (Ex.1001). I am being compensated for my time in connection with this Petition at my standard consulting rate of \$675 per hour. My compensation is not affected by the outcome of, or my testimony in, this IPR, or any litigation proceedings. I am informed that the assignee for the patent in the present proceeding is Advanced Integrated Circuit Process LLC (“Patent Owner”). I am also informed that the Petition names United Microelectronics Corporation and UMC Group (USA) as real-parties-in-interest.
3. I have been asked to provide my opinions regarding whether claims 1, 3, 4, 7, 8, and 11 of the ’425 patent (the “Challenged Claims”) are invalid as anticipated, or as obvious to a person having ordinary skill in the art at the time of the alleged invention (“POSITA”).
4. The ’425 patent issued on December 9, 2014, from U.S. Patent Application No. 13/528,526, filed on June 20, 2012. The ’425 patent claims priority to Japan Application No. 2010-002225, filed on January 7, 2010.

5. I am not currently, and have not at any time in the past been, an employee of any Petitioner or any real-party-in-interest. Other than set out above, I have no affiliation, contractual connection, or financial connection with any Petitioner or any real-party-in-interest, or any of their respective subsidiaries or parents. I similarly have no financial interest in, or affiliation with the Patent Owner.

I. BACKGROUND AND QUALIFICATIONS

6. I am currently the Cockrell Family Chair Professor of Electrical and Computer Engineering at the University of Texas at Austin. At UT Austin, I was also the director of the Microelectronics Research Center from September 1999 through January 2025. I have been a faculty member at UT Austin since 1987.

7. I have also been active in industries related to the relevant field of art. As a Member of the Technical Staff, Corporate Research, Development and Engineering of Texas Instruments Incorporated from 1983–1987, I worked on polysilicon transistors and dynamic random access trench memory cells used by Texas Instruments in the world’s first 4-Megabit DRAM, for which I was co-recipient of the Best Paper Award, IEEE International Solid State Circuits Conference, 1986.

8. I received a B. Tech. degree from the Indian Institute of Technology, Kharagpur, and M.S. and Ph.D. degrees from the University of Illinois at Urbana-Champaign, all in Electrical Engineering.

9. I am a leading researcher and educator in various areas of transistor device fabrication technology, including the fabrication, characterization and application of memory devices, transistors, and nanotechnology. My research has been funded by the Texas Advanced Technology Program (ATP), the Texas Higher Education Coordinating Board, the National Science Foundation, the SEMATECH (Semiconductor Manufacturing Technology) consortium, the SRC (Semiconductor Research Corporation) consortium, DARPA, and the Department of Energy, among others.

10. At the University of Texas, I also served as the director of the South West Academy of Nanoelectronics from its inception through the end (2006 - 2017), one of three centers in the United States established to develop a replacement for MOSFETs.

11. I have published over 1,200 technical articles, many related to semiconductor fabrication technology, most at highly competitive refereed conferences and rigorously reviewed journals. I have also published 8 books or chapters on transistor device physics and fabrication, and have supervised over 80 Ph.D. and 60 MS students.

12. I have been a member of scientific organizations and committees, including the IEEE Dan Noble Award Committee from 2010–2013, serving as Chair from 2012–2013, the International Technology Roadmap for Semiconductors, the

Declaration of Dr. Sanjay Banerjee
Inter Partes Review of U.S. Patent No. 8,907,425

International Conference on MEMS (Microelectromechanical Systems) and Nanotechnology, the IEEE International Conference on Communications, Computers, Devices, the International Electron Devices Meeting, the International Conference on Simulation of Semiconductor Processes and Devices, and the IEEE Symposium on VLSI (Very-Large-Scale Integration) Technology. I have served as the Session Chair for the “Device Technology” Session conducted at the IEEE International Electron Devices Meeting in 1989–1990. I have also served as the General Chairman for the IEEE University Government Industry Microelectronics Symposium in 1994–1995, and Chair of the IEEE Device Research Conference.

13. I have served on the Technical Advisory Boards of AstroWatt, DSM Semiconductors, Cambrios, Nanocoolers Inc., BeSang Memories, Organic ID and ITU Ventures; Gerson Lehmann Group, NY; Austin Community College; Asia Pacific IIT; Rochester Institute of Technology, and HSMC Foundry.

14. I received the Engineering Foundation Advisory Council Halliburton Award (1991), the Texas Atomic Energy Fellowship (1990–1997), Cullen Professorship (1997–2001) and the Hocott Research Award from UT Austin (2007). I also received the SIA/SRC University Researcher Award (2018), IEEE Grove Award (2014), Distinguished Alumnus Award, IIT (2005), Industrial R&D 100 Award (2004), ECS Callinan Award, 2003, IEEE Millennium Medal, 2000, NSF Presidential Young Investigator Award in 1988, and several SRC Inventor

Recognition and Best Paper Awards. I was a Distinguished Lecturer for IEEE Electron Devices Society, and am a Fellow of the Institute of the Electrical and Electronics Engineers (IEEE), the American Physical Society (APS) and the American Association for the Advancement of Science (AAAS).

15. I am the inventor or co-inventor of over 35 United States patents in various areas of transistor device fabrication technology. I was elected a Fellow of the National Academy of Inventors in 2021.

16. My qualifications and publications are set forth more fully in my curriculum vitae, attached as Ex.1102.

II. MATERIALS AND OTHER INFORMATION CONSIDERED

17. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art and have considered the viewpoint of a POSITA at the time of the alleged invention.

18. I have considered the materials referenced herein, including the '425 patent (Ex.1001), the file history of the '425 patent (File History, Ex.1002), the parent and related applications, the file histories of the parent and related applications, the Petition, and other documents listed in the Exhibit List of the Petition, including:

Declaration of Dr. Sanjay Banerjee
Inter Partes Review of U.S. Patent No. 8,907,425

Description	Date of Public Availability
U.S. Patent Publication No. 2009/0246922 A1 to Wu922 et al. (“Wu922”) (Ex.1005)	Published October 1, 2009
U.S. Patent Publication No. 2007/0249069 A1 to Alvarez et al. (“Alvarez”) (Ex.1006)	Published October 25, 2007
U.S. Patent Publication No. 2005/0112817 A1 to Cheng817 et al. (“Cheng817”) (Ex.1008)	Published May 26, 2005
U.S. Patent Publication No. 2007/0034906 A1 to Wang906 et al. (“Wang906”) (Ex.1009)	Published February 15, 2007
U.S. Patent Publication No. 2008/0029825 A1 to Saito825 et al. (“Saito825”) (Ex.1010)	Published February 7, 2008
U.S. Patent Publication No. 2005/0285203 A1 to Fukutome et al. (“Fukutome”) (Ex.1011)	Published December 29, 2005
D. James, “2004 – The Year of 90-nm: A Review of 90 nm Devices,” 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (2005) (“James”) (Ex.1012)	Published 2005

19. It is my understanding that the references listed above are prior art to the '425 patent, which is entitled to a priority date not earlier than January 7, 2010. Wu922, Alvarez, Cheng817, Wang906, Saito825, Fukutome, and James (Exs. 1005, 1006, 1008, 1009, 1010, 1011, and 1012 respectively) were not discussed during the prosecution of the '425 patent.

III. UNDERSTANDING OF PATENT LAW

20. I am not an attorney. For purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law is as listed below.

A. Claim Construction

21. I understand that in an IPR petition filed after November 13, 2018, a claim must be construed under the *Phillips* standard. Under that standard, words of a claim are given their plain and ordinary meaning as understood by a POSITA at the time of invention, in light of the specification and prosecution history, unless those sources show an intent to depart from such meaning, as well as pertinent evidence extrinsic to the patent.

22. I have applied this understanding in my Declaration. I do not believe any claim terms require explicit construction in this proceeding to resolve the patentability of the Challenged Claims.

B. Anticipation and Obviousness

23. I have been informed that a patent claim is anticipated if a single prior art reference, such as a patent or a publication, discloses all the elements of the claimed invention.

24. I have been informed and understand that a patent claim can be considered to have been obvious to a POSITA at the time the application was filed.

This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a POSITA at the time the application was filed. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

25. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to a POSITA. In determining whether a combination based on either a single reference or multiple references would have been obvious, I have been informed that it is appropriate to consider at least the following factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;

- whether a POSITA could implement a predictable variation, and would *see* the benefit of doing so;
- whether the claimed limitations represent one of a limited number of known design choices, and would have a reasonable expectation of success by a POSITA;
- whether a POSITA would have recognized a reason to combine known limitations in the manner described in the claim;
- whether there is some teaching or suggestion in the prior art to make the modification or combination of limitations claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

26. I understand that a POSITA has ordinary creativity, and is not an automaton.

27. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

28. I understand that prior art to the '425 patent for purposes of my opinion herein includes patents and printed publications in the relevant art that predate the priority date of the '425 patent.

29. I understand that certain factors—often called “secondary considerations”—may support or rebut an assertion of obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the alleged invention, skepticism of those having ordinary skill in the art at the time of the alleged invention, unexpected results of the alleged invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field.

30. I further understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

IV. SUMMARY OF OPINIONS

31. It is my opinion that claims 1, 3-4, 7-8, and 11 are anticipated by Wu922 (Ex.1005) and Alvarez (Ex.1006) (Ground 1).

32. It is my opinion that claims 1, 3-4, 7-8, and 11 are obvious in view of Cheng817 (Ex.1008) (Ground 2).

33. It is my opinion that claims 1, 3-4, 7-8, and 11 are obvious in view of a combination of Cheng817 (Ex.1008) and Wang906 (Ex.1009) (Ground 2A).

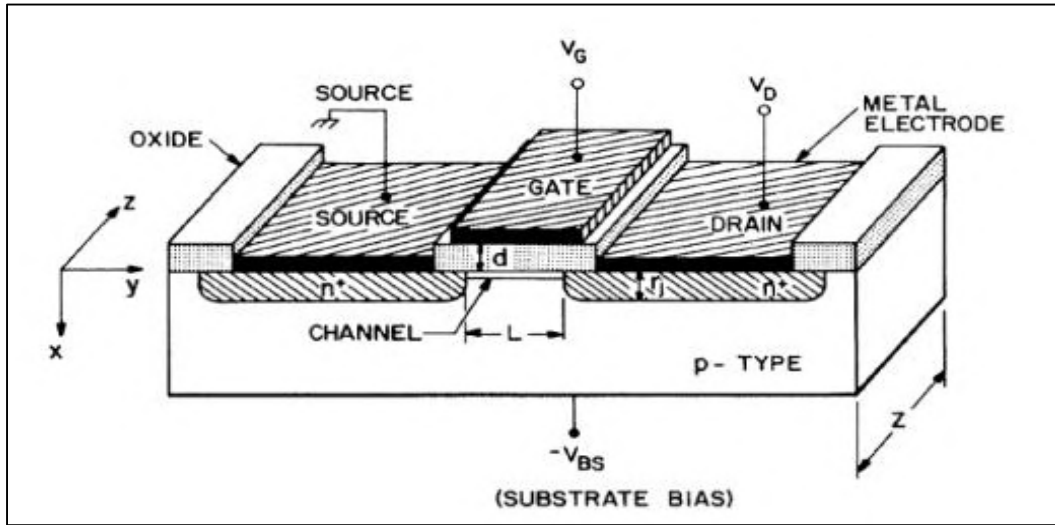
34. It is my opinion that claims 1, 3-4, and 7-8 are obvious in view of Saito⁸²⁵ (Ex.1010), Fukutome (Ex.1011), and James (Ex.1012) (Ground 3).

V. OVERVIEW OF THE TECHNOLOGY

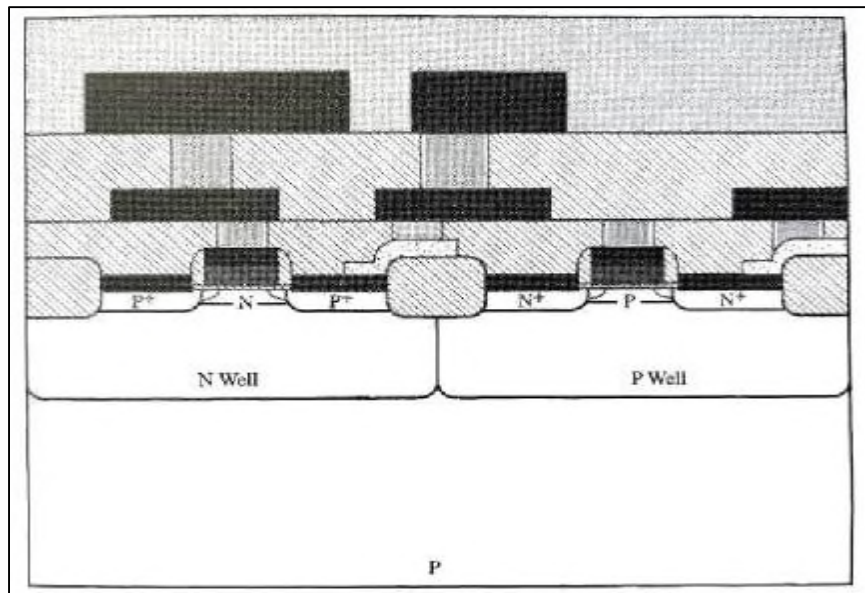
35. Broadly speaking, a semiconductor device is an electrical device made of semiconductor material like silicon or germanium. This includes many types of devices like light-emitting diodes (LEDs) and metal oxide semiconductor (MOS) transistors. Field effect transistors are just one type of semiconductor devices and have been in commercial use for decades, as discussed in more detail below.

A. MISFET/MOSFET

36. A metal insulating semiconductor field-effect transistor (MISFET), commonly referred to as a metal oxide semiconductor field-effect transistor (MOSFET) if the insulator is an oxide, is a transistor that switches from an OFF state to an ON state when a voltage greater than the threshold voltage is applied to a gate terminal. In the ON, or active state, current flows from a source to a drain through a channel region. For the transistor types at issue in this IPR, the channel region is located under the gate electrode (which can be made of stacked metal layers) and the gate insulating layer (often called a gate oxide or gate dielectric), and between the source and drain. Sze-1981, Ex.1413, 433-34, Fig. 3 (below); Plummer, Ex.1215, 71-76, Figs. 1-11 (further below).



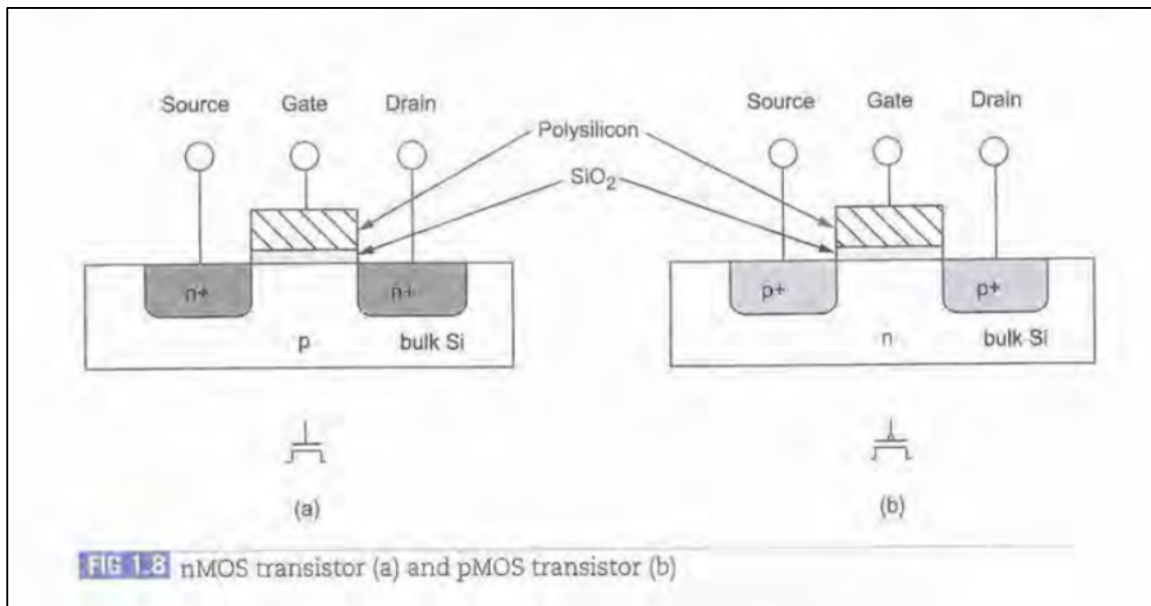
Sze-1981, Ex.1413, Fig. 3



Plummer, Ex.1215, Fig. 1-11

37. MOSFETs are characterized by the material used in the source and drain. A MOSFET with source/drain regions made from “p-type” material is known as a PMOS or p-FET, while a MOSFET with source/drain regions made from “n-type” material is known as a NMOS or n-FET. Thus, MOSFETs generally include a gate

electrode, a gate insulating layer, and “the silicon wafer, also called the substrate, body or bulk.” Weste, Ex.1212, 8. An nMOS transistor “is built with a p-type body and has regions of n-type semiconductor adjacent to the gate called the source and drain.” *Id.*, 8 (emphasis omitted), FIG. 1.8(a). A pMOS transistor “is just the opposite, consisting of p-type source and drain regions with an n-type body.” *Id.*

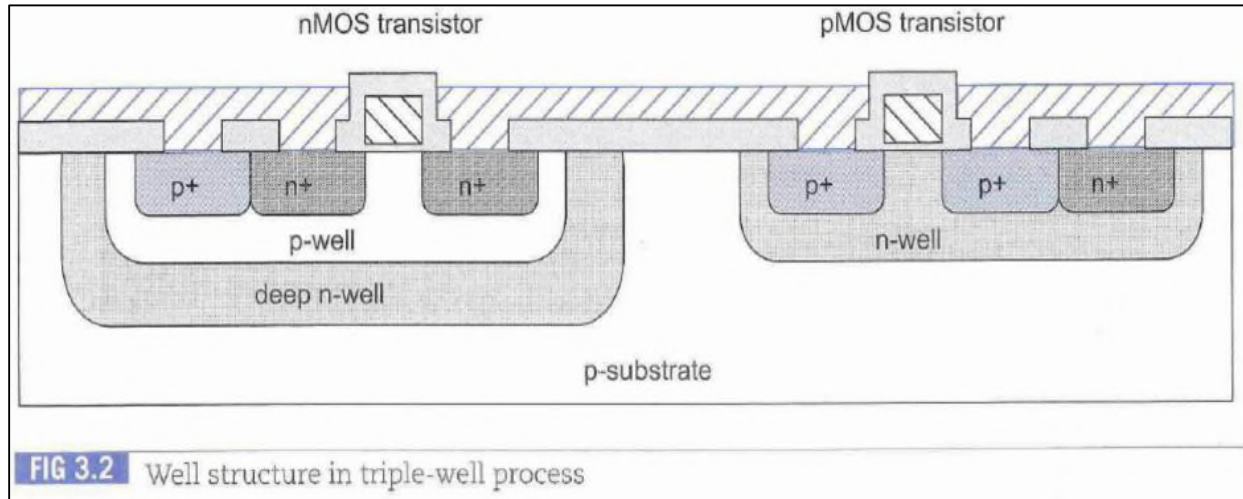


Weste, Ex.1212, Fig. 1.8

Id., 8, FIG. 1.8(b) (above, right).

38. In the mid-1980s, complementary MOS (CMOS) devices became popular, which have both PMOS (p-FET) and NMOS (n-FET) transistors on the same substrate or integrated circuit (IC). In such devices, the active areas (and associated transistors) are generally formed in regions called “wells,” and a transistor can even

have more than one well, as seen below. *See* Weste, Ex.1212, 117-118, FIG. 3.2 (below).



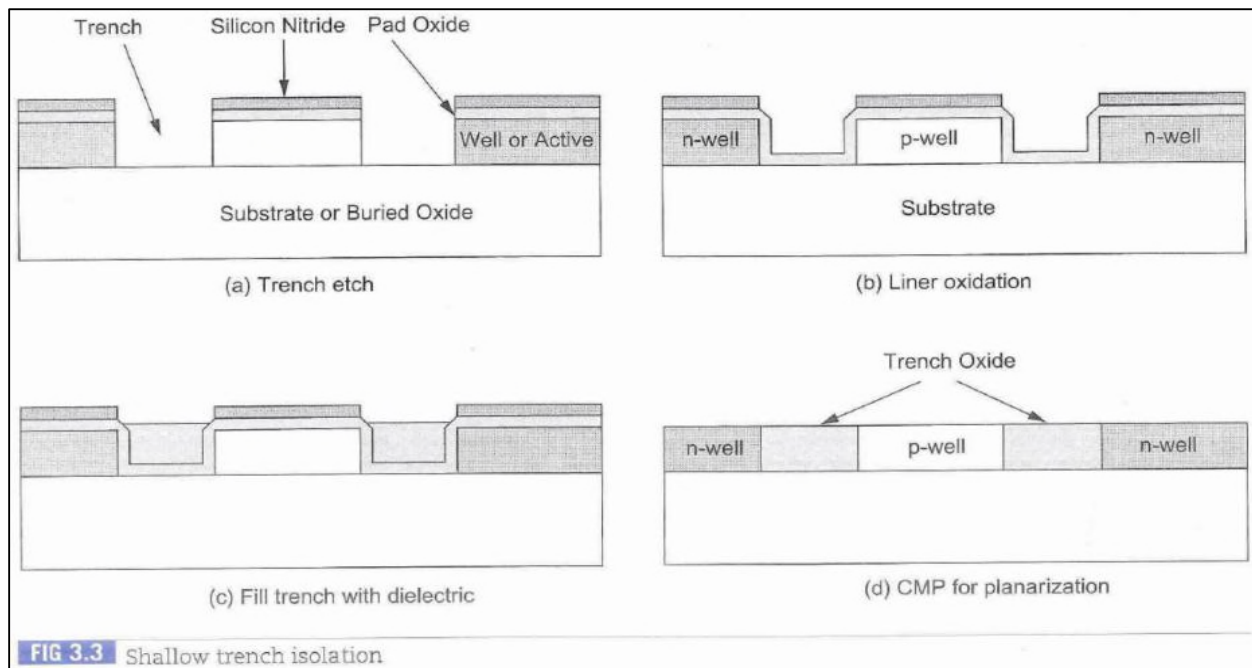
Weste, Ex.1212, Fig. 3.2

39. Impurities known as “dopants” are added to the active areas and wells to add charge carriers and tailor the electrical properties of these regions, such as their conductivity. The wells have opposite dopant types to the dopants of the source/drain. As such, an n-FET is formed in a p-well, and a p-FET is formed in an n-well. *See* Weste, Ex.1212, 8, FIG. 1.8(b).

40. With respect to dopants, charge carriers can be electrons (which are negatively charged) or holes (which are positively charged). When a region is doped with p-type dopants (like boron), the holes are majority carriers and the electrons are minority carriers. *See* Weste, Ex.1212, 7; Plummer, Ex.1215, 17. When a region is doped with n-type dopants (like arsenic), the electrons are majority carriers and the

holes are minority carriers. *See* Weste, Ex.1212, 7; Plummer, Ex.1215, 17 (“The electrons or holes are introduced on a one for one basis by the dopants.”).

41. One issue with ICs relates to forming multiple devices on the same chip, and often it is necessary to isolate two structures from each other to ensure proper operation on the chip. One example of this isolation is forming a shallow trench isolation on the substrate between devices. *See* Weste, Ex.1212, 117. In the example below, a trench is etched between a p and n-well to form the shallow trench isolation. *Id.*, 119, Fig. 3.3 (below).



Weste, Ex.1212, Fig. 3.3

42. Once the dopants are added, or implanted, into the silicon substrate, they need to be annealed, for example to repair the silicon crystal lattice from any damage caused by the dopant implantation. Plummer, Ex.1215, 81-82. “Because the ion

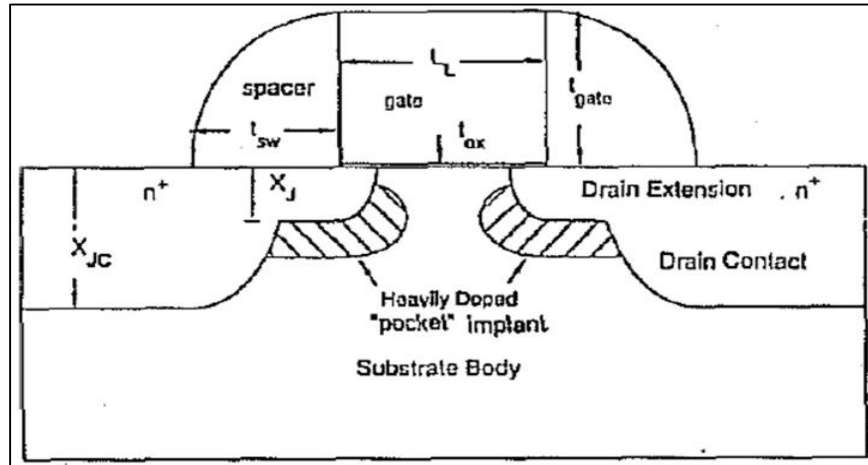
implantation process creates damage, most dopants are not electrically active at the end of the implantation.” *Id.*, 470. A rapid thermal anneal, often at temperatures over 1000 degrees Celsius, can activate the dopants and repair some of the damage done by implantation. *Id.*, 81. Annealing can also cause diffusion of the implanted dopants throughout the substrate (and in certain circumstances, other layers of the device). The interaction of the implanted dopants between the source/drain, the gate electrode and the gate insulating layer, and the channel were all well understood by a POSITA long before the priority date of the challenged patents. In fact, a POSITA would often use the various interactions of the manufacturing process, for example the shape of the source/drain after dopant implantation and annealing, to improve and optimize the performance of the semiconductor device, as discussed further below.

43. For example, varying the amount of dopants at different positions in the semiconductor device can have significant impacts on the device’s performance. Where a source/drain may be heavily doped, other areas may only be lightly doped. As one example, the prior art has recognized that as transistors continue to scale down in size, using source and drain extensions may provide certain benefits, and these extensions can have varying dopant levels, including what are commonly referred to as lightly doped drain (LDD) and highly doped drain (HDD). Plummer, Ex.1215, 77; Rodder, Ex.1323, 2:61-62, 3:65-67.

44. Source/drain extensions were known to assist in suppressing short channel effects of scaled-down transistors by varying the dopants and having a gradual transition in the electrical field between the source, the source extension, the channel, the drain extension, and the drain. Plummer, Ex.1215, 77-78 (using a LDD “allows the drain voltage to be dropped over larger distance than would be the case if an abrupt N⁺P junction were formed” and even “modest reductions in the field strength obtained through the LDD structure can make a significant difference in device reliability”).

45. As I discuss further below, sidewall structures placed on the edge of gate electrodes can serve many purposes, including to control the shape and position of source/drain extensions after annealing of the implanted dopants, as well as the overlap of the extension regions and the gate/gate insulating film. *See* Plummer, Ex.1215, 78.

46. As another example of varying dopants, the prior art also taught using pocket or halo implants to further mitigate the short channel effect as transistor sizes decreased. Pocket implants are placed below the channel region, as shown below. Wolf-4, Ex.1214, 219-20, Fig. 5-27 (below).



Wolf Vol. 4, Ex.1214, Fig. 5-27

47. In this example, the pocket implants are doped opposite of the source/drain and source/drain extension. Wolf-4, Ex.1214, 219 (“Precise control of the placement and dose of this implant within the transistor-structure is needed to obtain the intended enhancements.”).

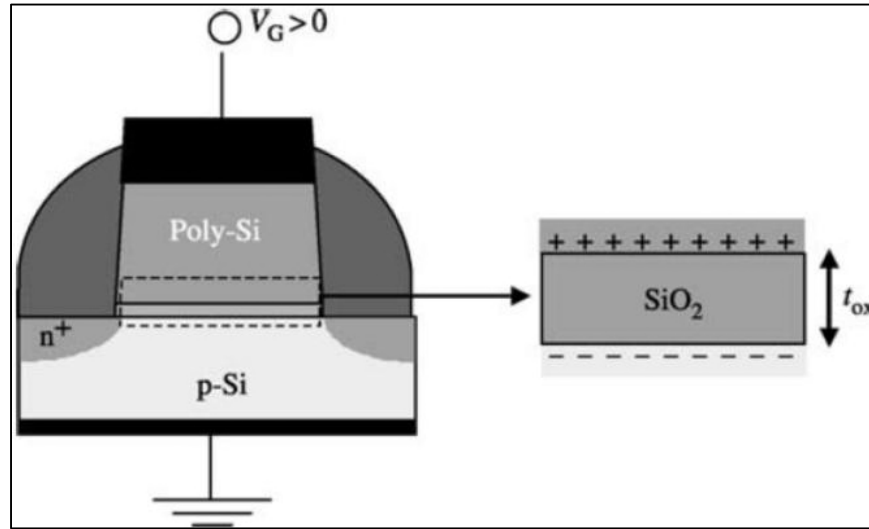
B. Gate Insulating Films & High-k Materials

48. The gate insulating film or gate dielectric isolates the gate electrode from the channel. Plummer, Ex.1215, 288. Silicon dioxide was primarily used as the gate dielectric material for many years (*id.*, 53), but silicon dioxide films presented problems when reduced in thickness for smaller and smaller transistors. In particular, “in ultrathin SiO₂ gate layers (thickness typically below 3 nm) charge carriers can flow through the gate dielectric by quantum mechanical tunnelling mechanism.” Houssa, Ex.1213, 5; *see also* Wolf-4, Ex.1214, 4-5.

49. The MOS transistor, from an electrical perspective, “behaves like parallel plate capacitor when gate voltage V_G is applied to the gate charges on the metal are compensated by opposite charges in the semiconductor, these latter charges forming the channel connecting the source and the drain of the transistor as illustrated in figure 1.1.4.” Houssa, Ex.1213, 8, Fig. 1.1.4 (below). The capacitance C can thus be represented by the following equation:

$$C = \frac{A\epsilon_r\epsilon_0}{t_{ox}} \quad (1.1.1)$$

50. In this equation, “ A is the capacitor area, ϵ_r the relative dielectric constant of the material (3.9 for SiO_2), ϵ_0 the permittivity of free space ($8.85 \times 10^{12} \text{ F m}^{-1}$) and t_{ox} the gate oxide thickness.” Houssa, Ex.1213, 8. From this formula, the gate oxide thickness has an inverse relationship to capacitance: decreasing the gate oxide thickness increases the capacitance of the structure, with a corresponding “increase in the number of charges in the channel for a fixed value of V_G .” *Id.*



Houssa, Ex.1213, Fig. 1.1.4

51. In practical uses, however, problems occur when decreasing the gate oxide thickness of silicon dioxide past a certain point. Houssa, Ex.1213, 8. As one prior art textbook proposed, “[a]n alternative way of increasing the capacitance is to use an insulator with a higher relative dielectric constant than SiO₂ (it should be noticed that the relative dielectric constant is also represented by the letter k and one speaks about high-k materials).” *Id.*, 8-9. “One could then use a thicker gate layer and, hopefully, reduce the leakage current flowing through the structure and also improve the reliability of the gate dielectric.” *Id.*

52. Equivalent oxide thickness (EOT) is one measure of high-k gate dielectrics. The EOT of a high-k material “is defined as the thickness of the SiO₂ layer that would be required to achieve the same capacitance density as the high-k material in consideration” (Ex.1213, 9), which can be represented by the following equation:

$$\frac{t_{eq}}{\epsilon_{r,SiO_2}} = \frac{t_{high-k}}{\epsilon_{r,high-k}} \quad (1.1.2)$$

53. In this equation, “ t_{high-k} and $\epsilon_{r,high-k}$ are the thickness and relative dielectric constant of the high-k material, respectively.” *Id.* In one example shown by Houssa, “using ZrO_2 as gate dielectric ($\epsilon_r \approx 20$) would allow us to use a 5.1 nm thick layer in order to achieve a capacitance equivalent to a 1 nm thick SiO_2 layer; the equivalent oxide thickness of this ZrO_2 layer is thus 1 nm.” *Id.*

54. But make no mistake, more than just a hope, the use of high-k gate dielectrics were a well-known, well-understood, and well-documented component to improve transistor performance as a substitute for silicon dioxide gate dielectrics, especially as transistors continued to decrease in size in the early 2000s. Long before 2005, numerous industry publications and other prior art readily recognized the advantages of using high-k materials as a gate dielectric.

55. In 2002, for example, numerous industry papers identified high-k materials, and hafnium oxide HfO_2 in particular, as a significant contributor to increased transistor performance. A paper by Rim et al. titled “Mobility Enhancement in Strained Si NMOSFETs with HfO_2 Gate Dielectrics” recognized that POSITAs had already been looking to high-k materials to solve known problems: “[g]ate leakage reduction in ultra thin gate dielectric is the main motivation for the search of high-k materials.” Rim-2002, Ex.1109, at Introduction; *see also id.*, Conclusion (“Strained Si NFETs with high-

K dielectrics exhibit significantly enhanced NFET mobility, even over the universal mobility of the SiO₂/bulk Si devices, and hold the promise for the best trade-off between mobility and gate leakage reduction, which is especially attractive for low power, high performance CMOS technology.”). Another article at the same industry conference concluded that “[h]igh-temperature FG annealing improved channel carrier mobility as well as subthreshold slopes in both N and PMOSFET with HfO₂ gate dielectrics,” which are “advantageous in achieving large on current while suppressing off current, and give more flexibility in V_t adjustment.” Onishi-2002, Ex.1107, Conclusion.

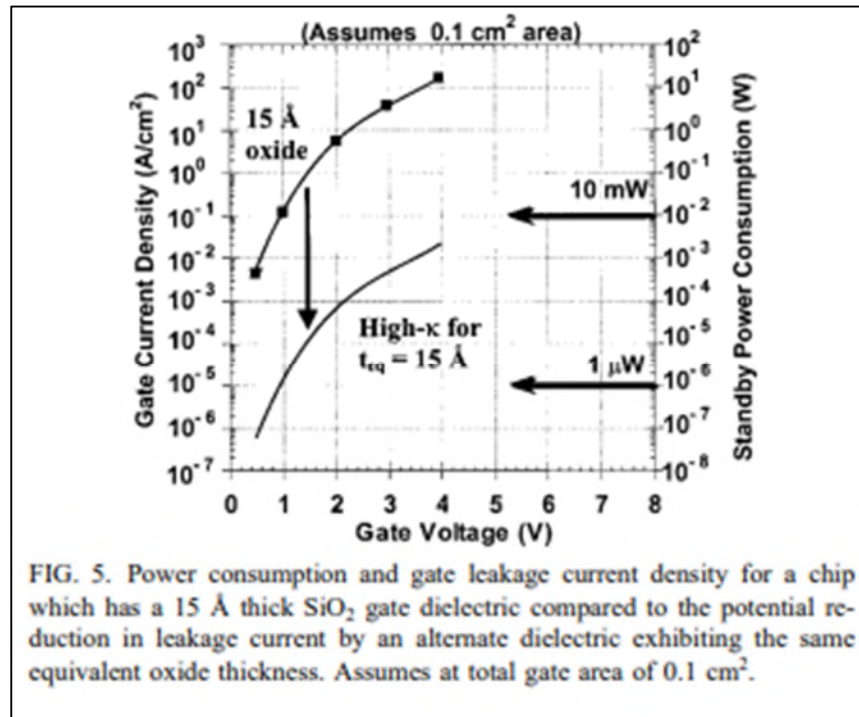
56. Yet another article at the same conference by Pidín et al., titled “Low Standby Power CMOS with HfO₂ Gate Oxide for 100-nm Generation,” concluded that HfO₂ was particularly suited for low standby current applications. Pidín-2002, Ex.1108, Conclusion (“55-nm CMOS with 3-nm HfO₂ gate dielectric was fabricated using conventional process flow with high-temperature anneal of $\geq 1000^{\circ}\text{C}$ and cobalt silicide. Gate current reduction of more than 3 orders of magnitude was achieved and low off-state current devices were obtained demonstrating very promising characteristics of HfO₂ for low standby current applications.”).

57. But more than just the structure and use of high-k materials, the industry had already begun optimizing the process for making transistors with high-k gate dielectrics, with one article from the 2002 VLSI Symposium comparing two gate first approaches using HfO₂, one via physical vapor deposition and another via chemical

vapor deposition. *See* Lee-2002, Ex.1105, Conclusion (“Compared with PVD TaN devices, the CVD TaN/HfO₂ devices exhibit lower leakage current and CV hysteresis, superior interface properties, higher transconductance, and superior effective electron and hole mobility.”).

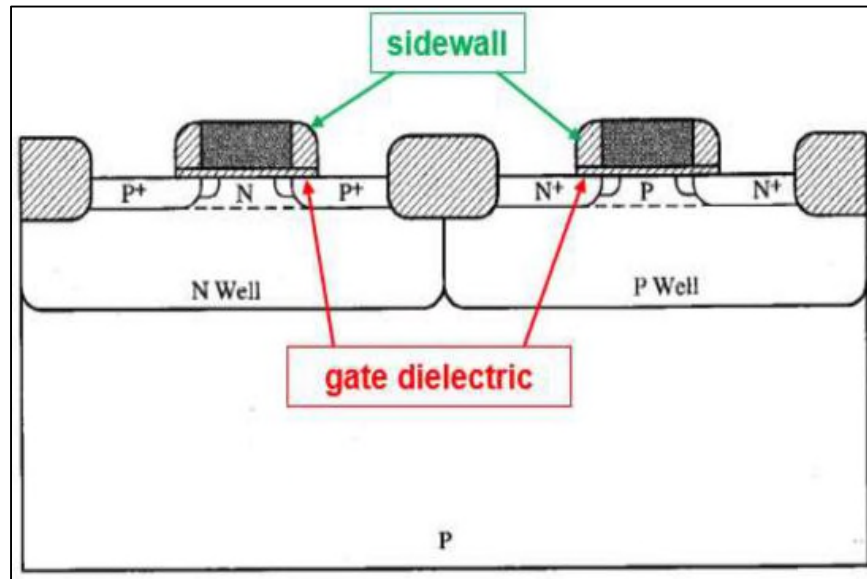
58. Numerous other prior art references recognized the ability of high-k gate dielectrics to make up for the shortcomings of too-thin silicon dioxide gate dielectrics. One article in the Journal of Applied Physics titled “High-k Gate Dielectrics: Current Status and Materials Properties Considerations” recognized that already by 2001 “much work has been done on high-k metal oxides as a means to provide a substantially thicker (physical thickness) dielectric for reduced leakage and improved gate capacitance.” Wilk, Ex.1318, 5250; *see also* Wolf-4, Ex.1214, 146-47 (“The use of high-k dielectrics as the gate dielectric in submicron MOSFET structures also improves other device characteristics,” including in threshold voltage V_t and in the subthreshold-swing S_t .”).

59. For example, as shown by Figure 5 below in Wilk, using high-k materials in place of silicon dioxide for the gate dielectric improved both power consumption and gate leakage current.



Wilk, Ex.1318, Fig. 5.

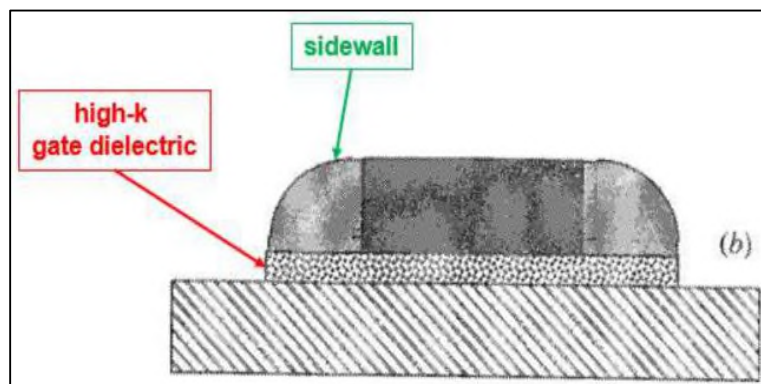
60. Not only did the prior art recognize the use of high-k materials as a substitute for silicon dioxide gate dielectrics, but the prior art also showed it was common to extend the gate dielectric out from underneath the gate electrode to underneath the sidewalls. For example, in Figure 2-34 below in Plummer, the gate dielectric is wider than the gate electrode.



Plummer, Ex.1215, Fig. 2-34

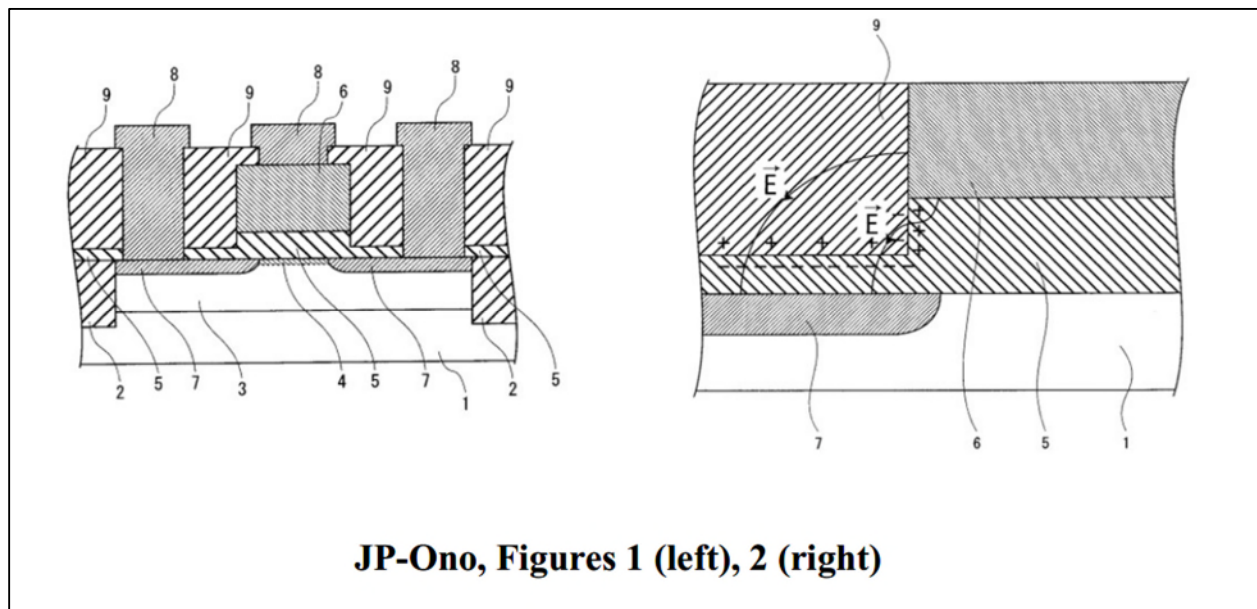
Plummer, Ex.1215, Fig. 2-34.

61. As another textbook example, Houssa shows using HfO_2 as the high-k gate dielectric, with and without extending the gate dielectric underneath the sidewalls. Houssa explains that by extending the gate dielectric “with the approach of figure 5.1.9(b), the etch requirements are relaxed but they will require LDD implants through the high-k layer.” Houssa, Ex.1213, 510, Fig. 5.1.9(b).



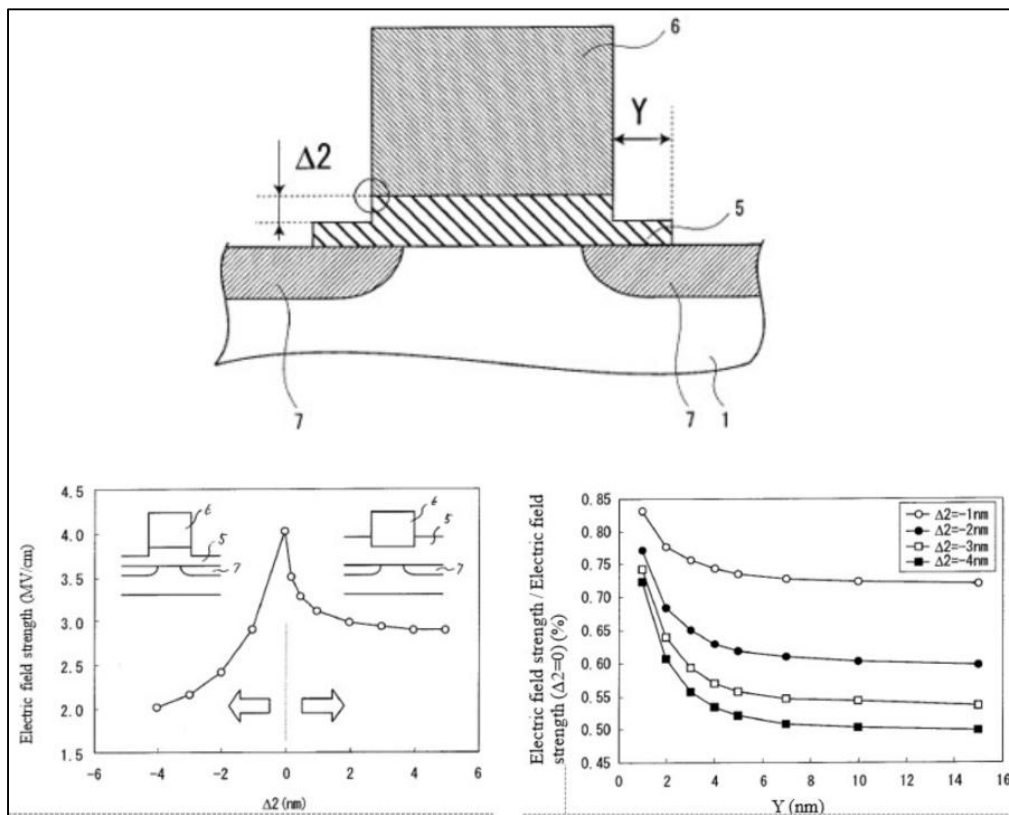
Houssa, Ex.1213, Fig. 5.1.9(b)

62. Japanese Publication No. 2005/064190 by Ono, et al. (“JP-Ono”) published on March 11, 2005 and described some of the known benefits of expanding the high-k gate dielectric wider than the gate electrode, including that “protruding the gate insulating film outside the gate electrode during processing results in higher values of the electric field.” JP-Ono, Ex.1340, ¶7. Further, JP-Ono suggests that extending the gate dielectric over the source/drain region, as well as reducing the thickness of the gate dielectric over the source/drain regions compared with under the gate electrode, “mitigate[s] the electric field at the lower end corner of the gate electrode 6” and “suppresses problems such as insulation breakdown and decreased reliability of the gate insulating film.” *Id.*, Abstract. Specifically, JP-Ono detailed how thinning the gate dielectric over the source/drain region minimizes the electric field at the edge of the gate. *Id.*, ¶¶29-32, Fig.1-2.



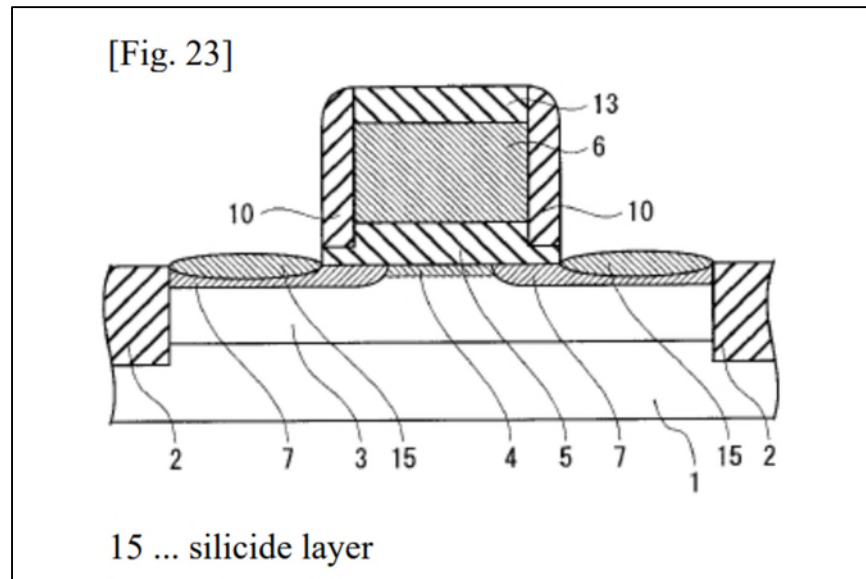
JP-Ono, Figures 1 (left), 2 (right)

63. Further, JP-Ono studied how varying the thickness and length of the gate dielectric over the source/drain regions affects the electric field distribution. Figure 4 shows that when the gate dielectric over the source/drain region is the same thickness as under the gate, e.g. at 0 $\Delta 2$, the electric field is strongest. JP-Ono, Ex.1340, ¶¶29-32, Fig.1-2. As the gate dielectric becomes thinner compared with under the gate electrode, e.g. when $\Delta 2$ is negative, the electric field weakens more than with a thicker gate dielectric, which favors a thinner dielectric over the source/drain regions. *Id.*, ¶35. Figure 24 further shows that the electric field is further reduced as the gate dielectric protrudes farther from the corner of the gate, i.e., as Y increases. *Id.*, ¶87.



JP-Ono, Figs. 3 (top), 4 (bottom-left), 24 (bottom-right)

64. These improvements are explicitly taught in a FET having a gate sidewall made of “materials like silicon oxide, silicon nitride, or silicon oxynitride,” as shown Figure 23 below. JP-Ono, Ex.1340, ¶83.

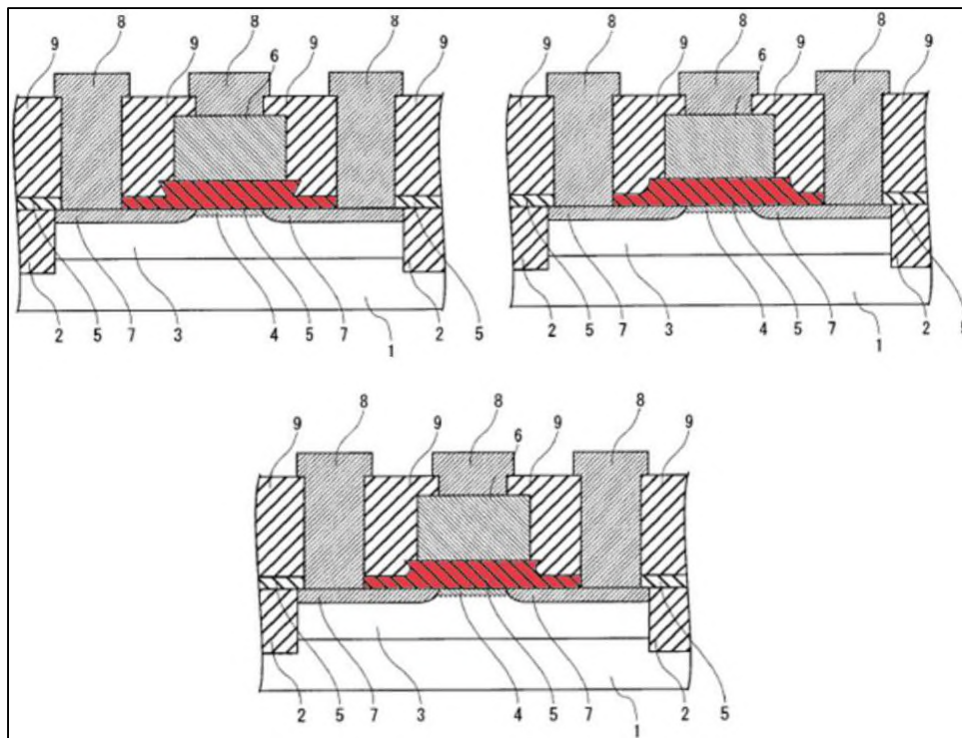


JP-Ono, Ex.1340, Fig. 23

65. Thus, JP-Ono teaches a POSITA the benefits of changing not only the location of the gate dielectric, e.g. outside the gate electrode, but also the shape of the gate dielectric, e.g. with thinner ends over the source/drain regions than underneath the gate electrode. In reference to Figure 23, JP-Ono explained that “it is not essential for the side of the gate insulating film 5 to be located inside or outside of the outer surface of the gate-side wall 10,” but instead, the gate dielectric can be located both farther than the end of the sidewall, or closer than the end of the sidewall, with similar benefits. JP-Ono, Ex.1340, ¶83 (“Therefore, it is preferable that the side of the gate insulating film

does not protrude too far outward [or inward] from the outer surface of the gate-side wall.”).

66. JP-Ono demonstrated several different shapes for the protruding portions of the gate dielectric in Figures 36-44, as can be seen by some examples below in red. JP-Ono, Ex.1340, Figs. 38, 41-42 (below). “By changing the shape of the gate insulating film near the lower corner of the gate electrode, as shown in the various examples here, it is possible to adjust the capacitance formed between the gate electrode 6 and the source-drain region 7, allowing for optimization.” *Id.*, ¶108. Although shown without any sidewalls, JP-Ono explained that “gate-side wall 10 may be removed after processing the gate insulating film, or it may be left as it is.” *Id.*, ¶103.



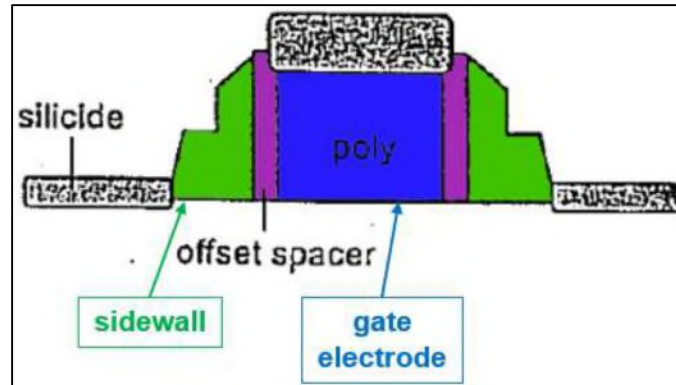
JP-Ono, Ex.1340, Figs. 38 (top-left), 41 (top-right), 42 (bottom)

C. Sidewall Structures

67. Varying the sidewall structure on the sides of the gate electrode is another way a POSITA had to further optimize device performance in the prior art. Sidewalls, also referred to as spacers or sidewall spacers, are formed on the side of the gate electrode for a variety of reasons. As discussed above, various sidewall structures may be used on the gate electrode to control the shape and position of source/drain extensions after annealing of the implanted dopants, as well as the overlap of the extension regions and the gate/gate insulating film. *See* Houssa, Ex.1213, 511; Weste, Ex.1212, 122; Wolf-4, Ex.1214, 9, 217, 219; Plummer, Ex.1215, 78. Alternatively, sidewall spacers can prevent shorts between the source/drain and the gate, for example if the source/drain regions have silicide portions. Plummer, Ex.1215, 742. These spacers are often made with silicon dioxide or silicon nitride, or combinations of multiple oxide and nitride layers. Houssa, Ex.1213, 511-12.

68. Varying the sidewall structure to control the source/drain extensions is one example of device optimization. As one textbook noted, “it has also been reported that the amount of overlap of the SDE-region with the gate-edge is also critical for optimum device performance.” Wolf-4, Ex.1214, 217. As shown in Wolf’s Figure 5-25 below, a POSITA knew that varying the size of the spacer at the gate electrode would affect formation of the source/drain extension and the resulting overlap with the gate edge: “an offset-spacer is fabricated on the side of the gate after the gate-poly is etched (but

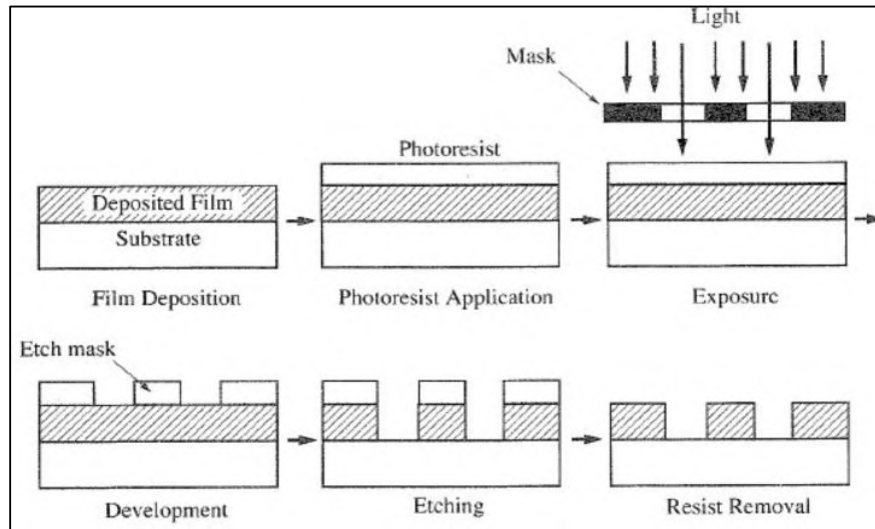
before the SDE implant step is carried out,” with the spacer width “varied from zero (no-spacer) to some upper-bound (e.g., 50-nm)” to control gate overlap and optimize device performance. *Id.*



Wolf-4, Ex.1214, Fig. 5-25

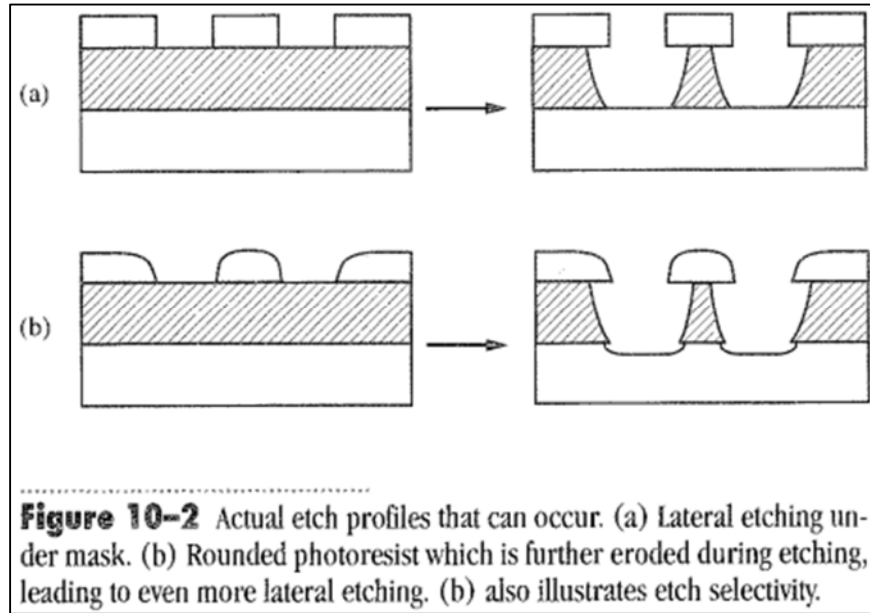
D. Etching

69. The process of manufacturing a semiconductor device, particularly one with varying transistor structures, often involves a series of material deposition and etching, including by deposition of thin films with selective etching to pattern a desired structure. Plummer, Ex.1215, 609-11. For example, a mask may be used in selective portions of a semiconductor device to “mask” or protect the underlying structure from further processing. As seen below, some areas may be masked while other areas are left unprotected such that a subsequent etching step etches the unmasked areas, while leaving the masked areas relatively intact. *Id.*, 609-10; Fig. 10-1.



Plummer, Ex.1215, Fig. 10-1

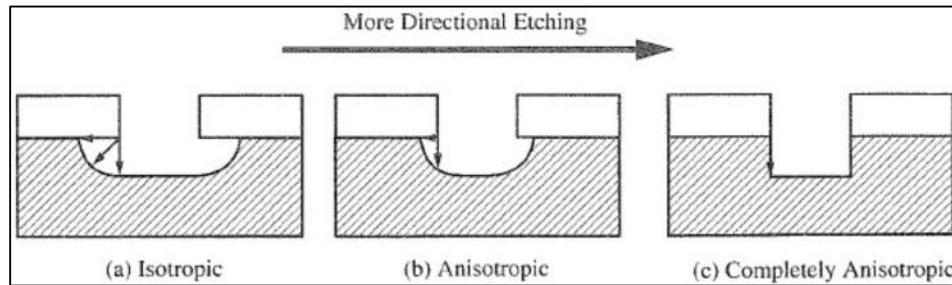
70. A POSITA can further optimize the structure of the semiconductor device by varying the etching process, as some processes are more selective than others. While the ideal etch profile “has perfectly straight sidewalls exactly under the edge of the mask,” as seen above in Figure 10-1, in practice etching has both lateral and vertical components, as seen below in Figure 10-2.



Plummer, Ex.1215, Fig. 10-2.

71. Etching is accomplished through both wet and dry processes, where wet etching often entails immersing the wafers in liquid like hydrofluoric acid to perform chemical etching, while dry etching uses plasma instead to etch material through both a physical and chemical process. Plummer, Ex.1215, 609, 612.

72. Under certain circumstance, etching can also be targeted to etch directionally. Anisotropic etching, for instance, is considered a vertical etch with little to no etching in the lateral direction, while isotropic etching has more equal etching rates both vertically and laterally. Plummer, Ex.1215, 610-13. These differences can be seen below in Figure 10-3.



Plummer, Ex.1215, Fig. 10-3

Id., Fig. 10-3.

E. Replacement Metal Gate Stacks

73. While the industry recognized the benefits of high-k gate dielectrics, the prior art also recognized that using metal gates on top of high-k gate dielectrics further enhanced transistor performance, particularly as transistor sizes became smaller. When formed on top of high-k gate dielectrics like HfO_2 , metal gate stacks addressed issues like Fermi-level pinning, eliminated polysilicon gate depletion, provided lower resistance, enhanced switching speeds, and improved overall transistor performance.

74. For example, a 2002 article by Samavedam et al. titled “Metal Gate MOSFETs with HfO_2 Gate Dielectric” recognized “[m]etal gates will eliminate gate depletion and address other issues like boron penetration and increased gate resistance, which will be aggravated as the poly gate thickness is scaled down.”). Samavedam-2002, Ex.1110, Introduction; *see also id.*, Conclusion (“We have successfully fabricated and characterized HfO_2 n-MOSFETs with TaSiN and PVD TiN gates and p-MOSFETs with CVD and PVD TiN gates using a conventional CMOS process. Metal-

gated HfO₂ n-MOSFETs show a 10⁴X gate leakage reduction compared to poly/SiO₂ devices. Reasonable Ion/Ioff performance and reliability were observed in PVD TiN/HfO₂ PMOS.”); *see also* Lee-2002, Ex.1105, Introduction (“As CMOS devices are scaled into sub-0.1 um regime, poly-depletion effects and boron penetration become significant concerns. Therefore, metal gate electrodes are being explored to replace the polysilicon gate.”). Just two years later, a 2004 article titled “55nm high mobility SiGe(:C) pMOSFETs with HfO₂ gate dielectric and TiN metal gate for advanced CMOS” concluded that “[f]or the first time, MOS transistors with compressively strained SiGe(:C) channel, metal gate and high-k dielectric are demonstrated down to 55nm gate length,” with significant improvements: “SiGe(:C) surface channel pMOSFETs with HfO₂ gate dielectric exhibit a 10⁴ gate leakage reduction and a 65% mobility enhancement at high transverse effective field (1MV/cm) when compared to the universal SiO₂/Si reference.” Weber-2004, Ex.1111.

75. Other prior art references further recognized the problem of using polysilicon gates with high-k gate dielectrics specifically, or decreased transistor size in general. As gate dielectrics grew smaller consistent with transistor sizes, the polysilicon depletion effect worsened. Saito631, Ex.1518, 1:31-34; Hou, Ex.1519, 1:36-44. And where a high-k material is substituted for the silicon dioxide gate dielectric with a polysilicon gate electrode, diffusion of the polysilicon dopants into the high-k material can cause a large threshold voltage offset. Colombo, Ex.1520, ¶5;

Kavalieros277, Ex.1515, ¶3. As discussed above, metal gate stacks were considered the next step to address these problems. Saito631, Ex.1518, 1:31-34; Iriyama, Ex.1521, 1:28-34, 1:41-42; ITRS_FEP, Ex.1512, 2-3, 20; ITRS_PIDS, Ex.1216, 1, 3, 27, Fig. PIDS5.

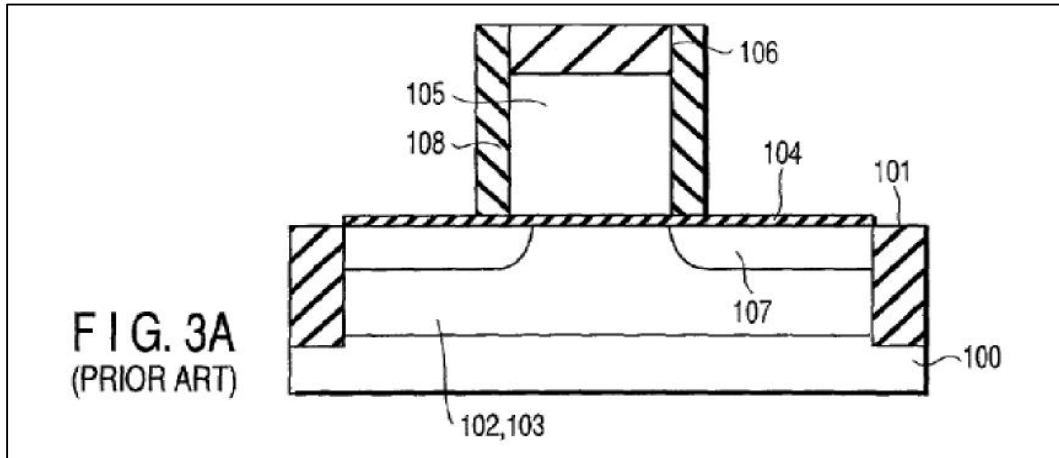
76. In particular, the prior art recognized that metal gates for PMOS and NMOS transistors would need separate metal gate stacks, and replacement metal gates (or gate-last processes) were well known to provide significant benefits compared with gate-first approaches. A material's "work function" is "the minimum energy required to bring an electron from the Fermi level to the vacuum level." Wolf-3, Ex.1229, 117. However, in MOS/MIS structures, the metal is in direct contact with a dielectric, not with the vacuum. Moreover, work functions of metal gates are highly dependent on material properties and interfaces. To differentiate this, an "effective work function" of the metal gate is commonly used to refer to the metal work function as measured (e.g., through the threshold voltage of the device).

77. In a CMOS device, PMOS transistors require a work function greater than about 4.8 eV, while NMOS transistors require a work function of less than about 4.6 eV. Hou, Ex.1519, 1:17-22; Colombo, Ex.1520, ¶¶20-21; ITRS_FEP, Ex.1512, Tbl. FEP4a ($|E_{c,v}-\phi_m|$ (eV) < 0.2). Where the same polysilicon gate electrode can be doped to adjust the work function for both NMOS and PMOS transistors, this is not the case for metal gates. Different metal gate stacks must be used. *See* Kavalieros277, Ex.1515,

¶3 (“When making a CMOS device that includes metal gate electrodes, it may be necessary to make the NMOS and PMOS gate electrodes from different materials.”).

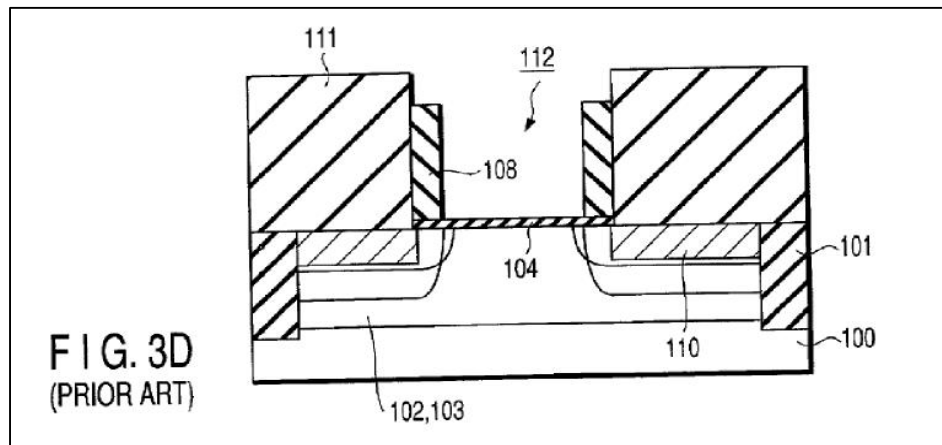
78. Some of the metals considered in the prior art for the PMOS metal gate stack showed less thermal stability than necessary, adversely affecting device performance when subjecting the metal to the high temperatures used to anneal the dopants in the source/drain regions. Hou, Ex.1519, 1:45-57; Iriyama, Ex.1521, 1:41-48.

79. One solution already considered by the prior art was replacement metal gates (“RMG”), which is a “gate-last” approach because a dummy gate is often manufactured first and then replaced by the metal gate. By making the metal gate last, the POSITA avoids subjecting the metal gate stacks to high temperatures during the source/drain annealing (because the annealing is done before placement of the metal gate). As seen below from one prior art reference, source/drain regions (107), the polysilicon dummy gate (105), a SiN film (106), and sidewalls (108) are formed for the NMOS and PMOS transistors before the replacement metal gate. Matsuo, Ex.1522, ¶¶9-10, 16, FIG. 3A.



Matsuo, Ex.1522, FIG. 3A

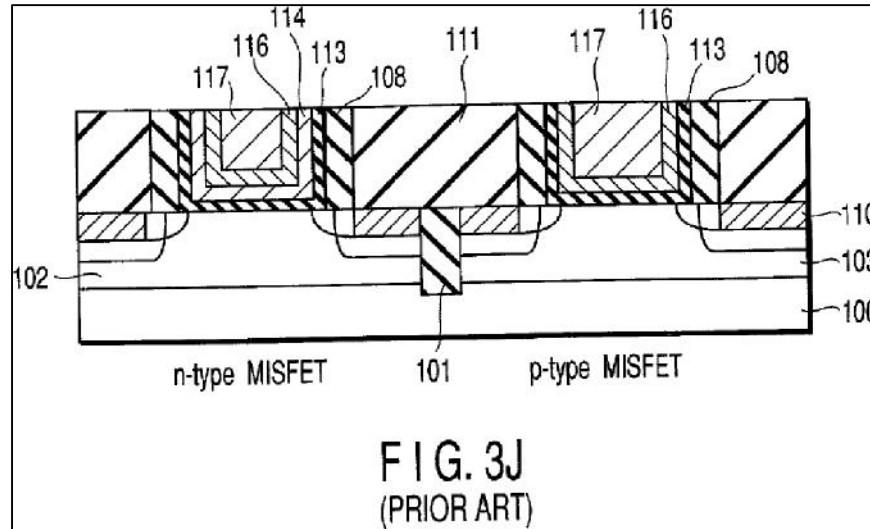
80. Before the dummy gate is replaced, the source/drain regions are doped and annealed. *See* Matsuo, Ex.1522, ¶10, FIGS. 3B-C; *see also* Hou, Ex.1519, 2:8-11; Iriyama, Ex.1521, 1:59-2:6. As one of the last steps, the dummy gates are removed to allow for placement of the metal gate stack. Matsuo, Ex.1522, ¶¶11-13, FIG. 3D.



Matsuo, Ex.1522, FIG. 3D

81. In this example, after removal of the dummy gate, both the NMOS and PMOS metal gate electrodes are formed, as seen below. Matsuo, Ex.1522, ¶¶12-16,

FIG. 3J. First, gate dielectric (113) is formed, and then metal layers 114, 116, and 117 after. *Id.*, ¶¶12-16. This sequence can prevent damage to metal gate stacks susceptible to deterioration by high temperature annealing. Iriyama, Ex.1521, 2:22-29.



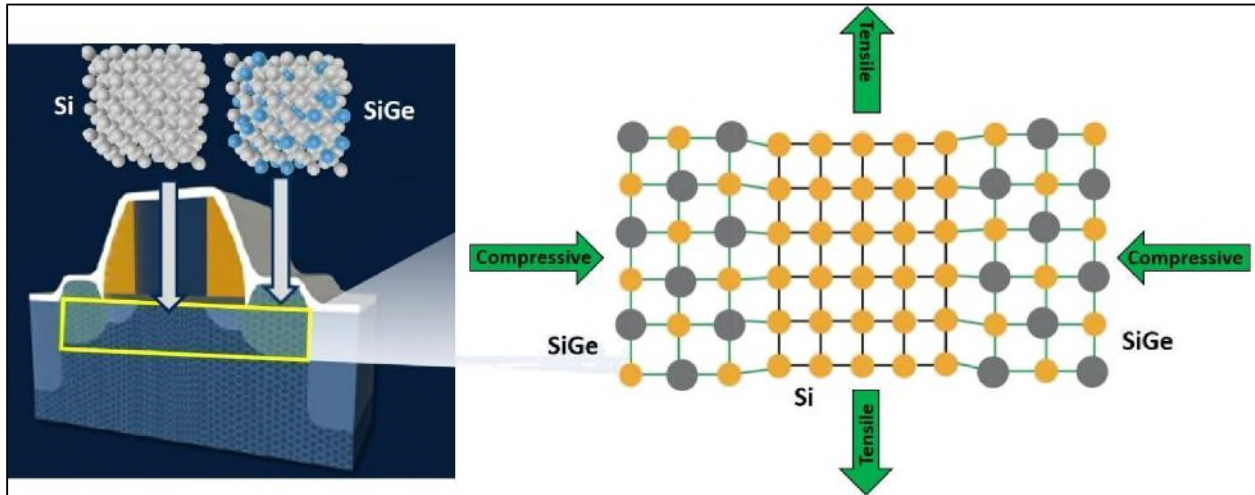
Matsuo, Ex.1522, FIG. 3J

82. In Fig. 3J above, the metal layer 114 is directly formed on the gate dielectric 113 for NMOS gate electrode (shown on the left), but a different metal gate stack is used for the PMOS gate electrode (shown on the right), which does not include metal layer 114. Matsuo, Ex.1522, ¶21. The two gate electrodes thus have different metal work functions, one for NMOS and one for PMOS. *Id.*, ¶21, FIG. 3J; Hou, Ex.1519, 2:11-14; Iriyama, Ex.1521, 2:10-12; Mistry2007, Ex.1516, 247; Mistry_Presentation, Ex.1517, 16, 18.

F. Strained Silicon

83. In the early 2000s, strained silicon technology was recognized as another mechanism to improve transistor performance as transistor sizes continued to shrink. Until the large-scale adoption of strained silicon, PMOS transistors used to be slower than NMOS transistors and much effort was spent on improving PMOS transistor performance compared with NMOS transistors. But the prior art quickly realized that compressively strained PMOS transistors could be improved by as much as 50%, leading to a reversal in efforts spent trying to improve NMOS transistors compared with PMOS transistors.

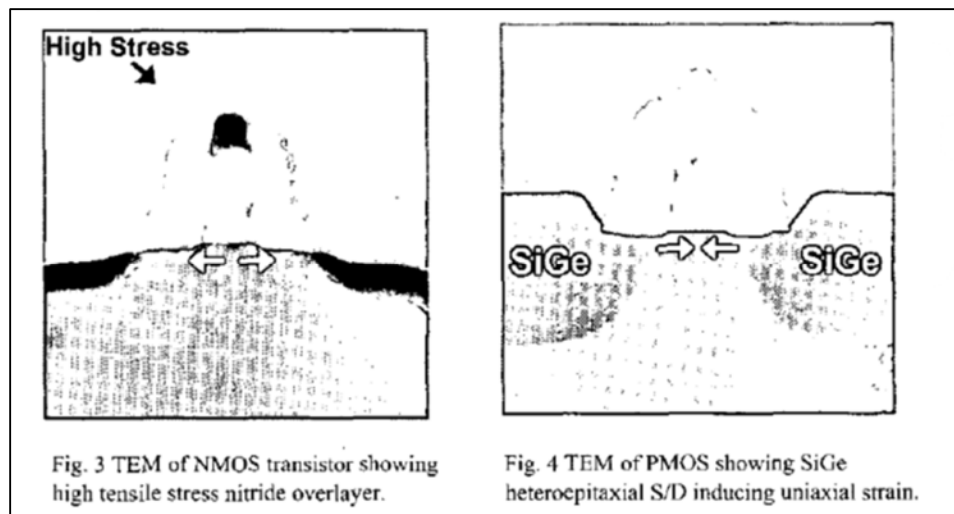
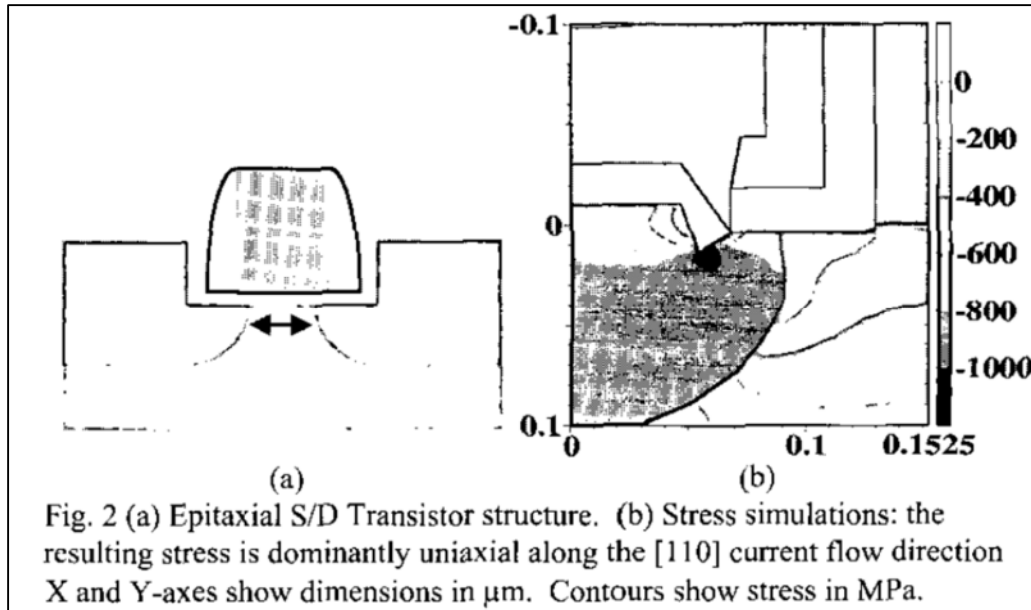
84. Germanium is one source of compressive stress in PMOS transistors. The Ge atoms are larger in size than Si atoms, such that silicon-germanium (“SiGe”) can be used in the source/drain regions of PMOS transistors to apply compressive stress to the PMOS channel region. *See* Thompson-2004, Ex.1523, 1790-96; Sun-2007, Ex.1524, 2. By 2005, SiGe source/drain regions increased PMOS “hole mobility by as much as 50%” (James, Ex.1012, 2), doubling PMOS operating speeds.



85. Numerous prior art references recognized the benefits of strained silicon, for both PMOS and NMOS transistors. For example, in a 2004 paper titled “35% Drive Current Improvement from Recessed-SiGe Drain Extensions on 37 nm Gate Length PMOS,” Chidambaram et al. recognized that “Epitaxial SiGe, grown in recessed Si, has been used to compressively strain the PMOS channel and increase the hole mobility.” Chidambaram-2004, Ex.1104, Introduction; *see id.*, Abstract (“A highly compressive SiGe layer, in close proximity to the channel, results in large hole mobility improvements.”). Another 2004 article by Mistry et al. proclaimed that “[t]he use of strain to improve mobility has been known for 50 years,” concluding that “[u]ni-axial strained silicon has been implemented in a high volume manufacturing 90nm logic technology for the first time, with impressive performance results and improved power scaling.” Mistry-2004, Ex.1106.

86. Where a PMOS transistor benefits from compressive strain, NMOS transistors benefit from tensile stress along the channel region. As seen in Figs. 2-4 from

Mistry-2004, compressive stress from SiGe source/drain regions on PMOS transistors and tensile stress on NMOS transistors from a high tensile stress nitride overlayer were well known to improve transistor performance.



Mistry-2004, Ex.1106, FIGS. 2-4.

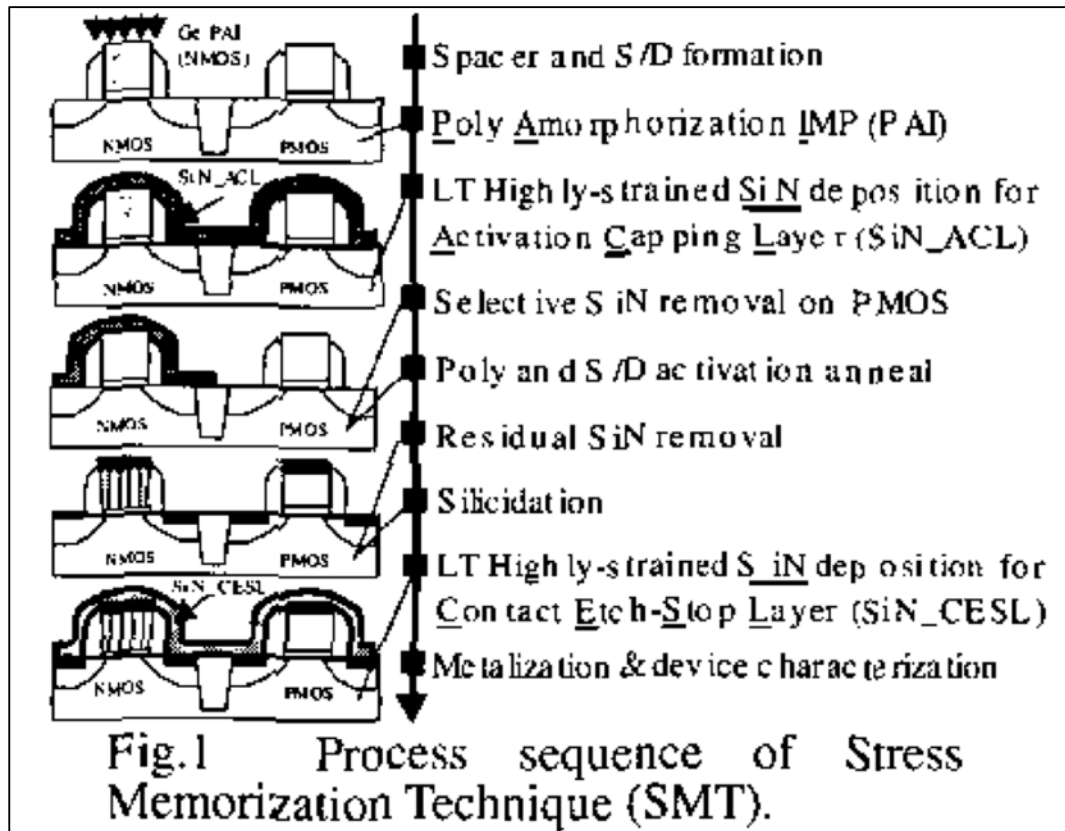
87. Other prior art references taught inducing strain by using strained films.
See Chen et al. titled "Stress Memorization Technique (SMT) by Selectively Strained-

Nitride Capping for Sub-65nm High-Performance Strained-Si Device Application.”

The prior art recognized that “[c]hannel stress control has become a critical technique for electron and hole mobility improvements as down scaling the device dimension.” Chen-2004, Ex.1103, Introduction. The article further recognized the tradeoffs inherent in stressing both PMOS and NMOS transistors on the same chip. *Id.* (“In addition, recent studies of high tensile capping layer on top of the silicide have demonstrated the NMOSFET driving current improvement capability, but with the PMOS performance degradation.”).

88. Searching for a cost-conscious method to effectively stress the NMOS transistor without degrading PMOS performance, the article proposed (1) selectively applying a high tensile nitride activation capping layer to the NMOS transistor, and (2) applying a low temperature, high-tensile nitride film as a contact etch stop layer to both the NMOS and PMOS transistors. Chen-2004, Ex.1103, Channel Stress Control by SMT; *see id.*, Introduction (“In this paper, we proposed a novel stress memorized technique (SMT) to improve the device performance without PMOS degradation. A high tensile nitride capping layer acts as a temporary stressor to effectively modulate the channel stress. The stress effect is then enhanced and memorized by well-controlled poly amorphization and re-crystallization procedures. This high tensile nitride capping layer will be removed after the annealing step. Therefore, a much thicker capping layer can be used to increase the stress level without any process limitation to

impact the subsequent gap filling process steps.”); *id.*, Channel Stress Control by SMT (“After the silicide formation, the low temperature, high-tensile Nitride film is deposited as Contact-Etch-Stop-Layer (SiN-CESL) to add up the stress effect.”).



Chen-2004, Ex.1103, Fig. 1.

89. Additional prior art references taught straining both PMOS and NMOS transistors. *See* Murthy151, Ex.1526, ¶¶5, 48, 72; James, Ex.1012, 2. For example, it was known to create tensile strain with epitaxial source/drain regions, similar to SiGe for PMOS transistors, but it requires using an atom smaller than silicon, like carbon, to grow a material like silicon carbide (SiC) instead of SiGe,. *See* Murthy151, Ex.1526, ¶¶5, 48, 72; James, Ex.1012, 2; Bohr, Ex.1527, ¶45.

90. As either an alternative or a supplement to source/drain epitaxy, the semiconductor industry was also already depositing compressive and tensile stress-inducing films over PMOS and NMOS devices to induce a desired strain, as shown above. *See also* James, Ex.1012, 2, 4; Morin-2007, Ex.1528, 355-56, 367; Hsu823, Ex.1506, ¶3; Jung, Ex.1529, Abstract, ¶90 (“In addition to being deposited as part of a structure to control electron mobility, as shown in FIG. 1B, a stress-tuned silicon nitride film can be deposited for other purposes . . . , for example . . . , to provide an etch stop layer . . .”). A contact etch stop layer (“CESL”) made of silicon nitride was frequently used, and if prepared under certain conditions, a silicon nitride CESL may apply stress to the channel and increase device performance. Hsu823, Ex.1506, ¶3; *see also* Ke, Ex.1531, ¶3 (“A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device.”); Jung, Ex.1529, ¶90 (“In addition to being deposited as part of a structure to control electron mobility, as shown in FIG. 1B, a stress-tuned silicon nitride film can be deposited for other purposes in various steps in the fabrication process, for example (and not by way of limitation), to provide an etch stop layer . . . , as well as to enhance channel mobility in various portions of the device structure.”); Morin-2007, Ex.1528, 355-56. It was well known that a silicon nitride CESL may provide tensile stress, compressive stress, or no stress at all, depending on the process used to apply the layer. *See, e.g.*, Jung, Ex.1529, ¶¶17, 99-100, 131-32, Tbls. IV-V, VII, Fig. 15.

91. As evidenced by the prior art, strained silicon has been well known long before the priority date of the challenged patents. *See, e.g.*, Sun-2007, Ex.1524, 1 (“Strain is a relatively old topic in semiconductor physics.”). In fact, strained silicon was already commercially used in at least three generations of devices by 2007. *See* Thompson-2004, Ex.1523, 1790-91 (Intel’s 90nm devices); Bai-2004, Ex.1532, 657-58 (Intel’s 65nm devices); Mistry2007, Ex.1516, 247-48 (Intel’s 45nm devices); Mistry_Presentation, Ex.1517, 1-19 (same).

G. Stress Buffering Layers

92. Not only were tensile stress contact etch stop layers and SiGe source/drains well known in the prior art, but using buffer layers to mitigate the unwanted effects of those stress layers were also well understood concepts in the prior art.

93. If a tensile contact etch stop layer is deposited over a PMOS device, it generally applies a tensile stress to the channel region. Morin-2007, Ex.1528, 355-56, 367; Doris, Ex.1429, ¶¶ 5, 13; Hsu823, Ex.1506, ¶37. Where the PMOS device is already compressively stressed, for example with epitaxial SiGe source/drain regions, the tensile stress from the contact etch stop layer offsets some portion of the compressive stress, reducing improvements from the SiGe. Morin-2007, Ex.1528, 355-56, 367; Kavalieros729, Ex.1419, ¶¶2, 26; Doris, Ex.1429, ¶5. The tensile stress may

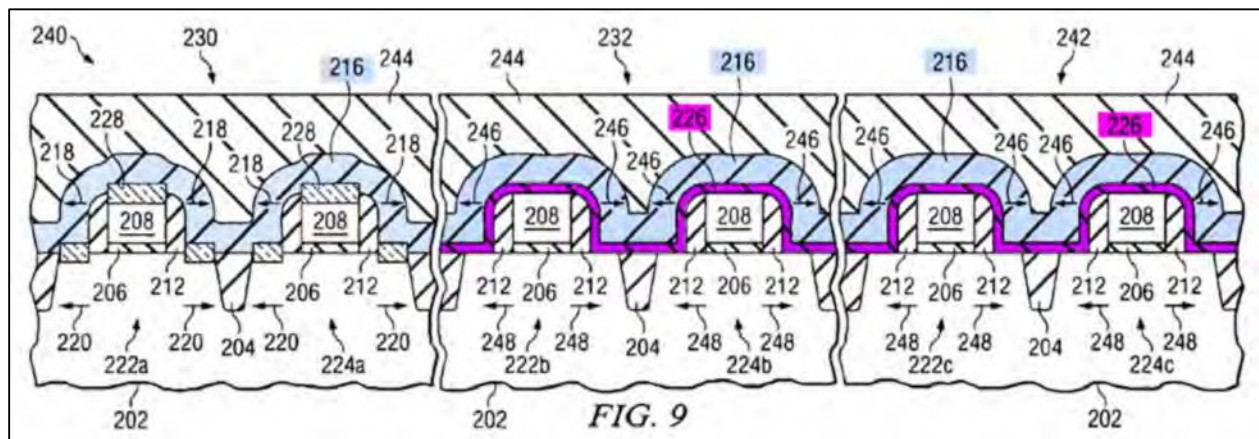
even degrade performance, particularly in PMOS devices without SiGe source/drains. Morin-2007, Ex.1528, 355-56, 367.

94. A POSITA would have understood how to mitigate or negate performance decreases on the PMOS devices from tensile stress. First, a POSITA may choose to apply both a SiGe source/drain to a PMOS device as well as a tensile contact etch stop layer over both the NMOS and PMOS devices to optimize performance of both devices. If the compressive stress from the SiGe is greater than the tensile stress from the contact etch stop layer, the overall compressive stress may still increase PMOS performance, though it may be lessened by the contact etch stop layer. The tradeoff is that the tensile stress improves NMOS transistor performance.

95. A POSITA knew of other ways to mitigate the performance loss. For example, the tensile stress could be reduced for the PMOS device by using a stress-relief layer as a buffer between the SiGe and the tensile contact etch stop layer. Murthy556, Ex.1430, 9:27-29, FIGS. 2, 9, 13-15; Doris, Ex.1429, ¶42, Figs. 1-2, 14-15; Alvarez, Ex.1006, Abstract, ¶43, FIG. 9; Lee870, Ex.1431, ¶29, ¶¶46-67 (pFET performance degradation “is reduced/eliminated due to the inclusion of the stress relief layer 64 under the nitride layer 70 that reduces the tensile stress in the channel region”), FIGS. 2-5; Cheng810, Ex.1432, ¶¶22-31, Figs. 1B-1F (describing similar); Baik, Ex.1433, ¶37 (“the tensile stresses of the [stressor layer] ha[ve] relatively little or no adverse impact [on] the adjacent PMOS device” because the intermediate layer

“reduce[s] the amount of stresses induced in the PMOS device by acting as a physical barrier”).

96. A number of prior art references taught that using an intermediate layer “buffers the large stress inherent silicon nitride layer.” Murthy556, Ex.1430, 9:27-29; Alvarez, Ex.1006, ¶¶49, 66, 68, 77, FIGS. 9-11. As seen below, Alvarez depicts on example with a stress-inducing layer 216 (shown in blue below) that is buffered by stress-control layer 226 (shown in purple) to mitigate the adverse effects of the stress layer on the PMOS devices 224b and 224c (while still improving performance of the NMOS devices).

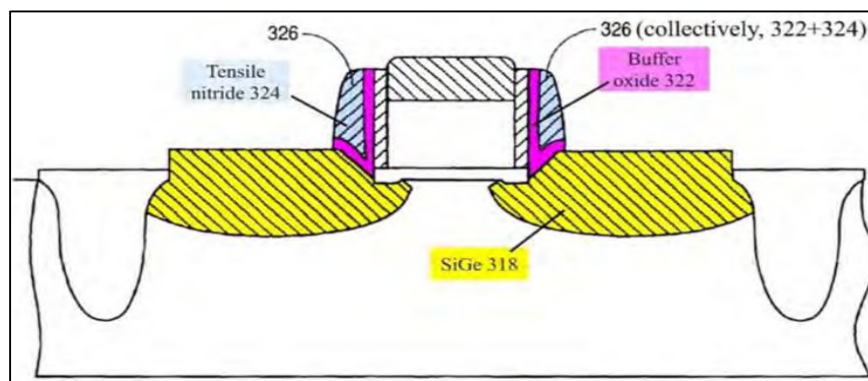


Alvarez, Ex.1006, FIG. 9

97. While the buffer layer above in Figure 9 is shown to be selectively applied, the prior art also explained that these layers could be applied to multiple areas, similar to the one Alvarez discloses (e.g., dual-purpose stress-controlling and masking layer), as a way to save manufacturing cost or complexity. Alvarez, Ex.1006, ¶¶43, 45, 47, 49,

53-55, 78, FIGS. 7-9. This is particular advantageous where “different types of transistors . . . hav[e] different operating parameters and requirements” and/or “due to the performance requirements of transistors in the particular regions.” *Id.*, ¶¶27, 32, FIGS. 7-9. Leaving the buffer layer over both the NMOS and PMOS, for example, can reduce the number of fabrication steps and lower the cost of manufacturing. *Id.*, ¶[0075]; *see also id.*, ¶¶74, 78.

98. In another example shown below, a buffer layer can be formed immediately between the SiGe source/drain regions and the gate electrode, particularly when raised SiGe source/drain regions are used. *See* Murthy556, Ex.1430, 9:11-15, 9:30-35, FIGS. 7-9; *see also* Miyashita, Ex.1435, ¶¶[0052]-[0053], FIGS. 1U-1W; Koutny, Ex.1434, ¶¶88, 108 (silicon dioxide liner 485A between tensile stress-inducing layer 504A and source/drain “reduces the cumulative stress” caused by the tensile layer); Doris, Ex.1429, ¶¶34, 42; Cheng810, Ex.1432, ¶30; Lee870, Ex.1431, ¶67.



Murthy556, Ex.1430, FIG. 9 (annotated)

99. These buffer layers can prevent “the tension from materially adversely influencing the charge carrier mobility in the pFET,” such that the pFET “experiences a performance improvement” through “enhanc[ed] hole mobility in the pFET channel” compared to no buffer layer. Doris, Ex.1429, ¶¶34-35, Figs. 2, 14, 15. Using low-stress dielectric films like silicon oxides can create “a neutral buffer layer” between a compressively stressed source/drain and a tensile contact etch stop layer, which allows the compressively stressed region “to have maximum influence on the pFET channel mobility and minimizes the influence of the tensile barrier etch stop layer.” *Id.*, ¶42; *see also* Lee870, Ex.1431, ¶¶29, 46-67 (explaining that an intermediate stress relief layer “with neutral stress or opposite stress relative to the [CESL]” reduces or eliminates any pFET performance degradation because it “reduces the tensile stress in the channel region”), FIGS. 2-5; Cheng810, Ex.1432, ¶¶22-31, Figs. 1B-1F.

H. System-on-Chip Design Advancements

100. Threshold voltage is an important characteristic when considering what a particular transistor will be used for. Threshold voltage is the minimum voltage applied at the gate to create a conductive channel between the source and drain—i.e., the ON or active voltage of the transistor. Van Zant, Ex.1211, 526, 474 (“Every MOS transistor is designed to operate at a specific threshold voltage.”). Because PMOS and NMOS transistors use different dopants for the source/drain and source/drain extensions, a POSITA understands that PMOS and NMOS transistors have opposite gate voltages.

That is, NMOS transistors require a positive voltage at the gate to induce the active state (and thus a positive threshold voltage), while PMOS transistors require a negative voltage at the gate to induce the active state (and thus a negative threshold voltage). *See, e.g.,* Weste, Ex.1212, 74, 293-296, 302.

101. Threshold voltage has three main components: flatband voltage (V_{FB}), voltage drop across the gate oxide (V_o), and semiconductor potential at the semiconductor surface during strong inversion ($\psi_s(inv)$). Sze-2002, Ex.1223, 175, 178, 194. For a given semiconductor and dielectric material, substrate doping, oxide thickness t_{ox} , and the metal work function Φ_m can be used to predictably tune a transistor's threshold voltage. Houssa, Ex.1213, 535, 537. When the substrate doping and gate oxide thickness are carefully engineered to control channel mobility and the gate capacitance, respectively, the gate electrode work function can be altered to optimize or fine-tune the threshold voltage further.

102. Consumer devices often have multiple transistors on the same chip, including transistors of the same conductivity types but with different threshold voltages, to cope with various demands on standby power and operation speed. For example, a device may include transistors for low operating power (LOP), transistors for low stand-by power (LSTP), and/or transistors for high performance (HP). ITRS-PIDS, Ex.1216, 5. HP transistors have the highest operating speed, the shortest gate length, the thinnest gate oxide, and the lowest threshold voltage among the three. ITRS-

PIDS, Ex.1216, 11, 17, 21. LSTP transistors are designed for low performance and low leakage current and therefore have thicker gate oxides and higher threshold voltage, while LOP transistors are between the HP and LSTP devices in terms of performance, leakage current, and threshold voltage. *Id.*

103. As recognized by the prior art, instead of making different chips for different purposes, HP, LOP, and LSTP transistors can be formed on a single chip by varying the manufacturing process parameters. Because “[a]n increasing number of mixed-signal and system-on-a-chip applications require dual on-chip power-supply-voltages[,]” different transistors of the same type (e.g., PMOS or NMOS) are needed for different power-supply-voltages. Wolf-4, Ex.1214, 121. For example, “[t]he higher-voltage may be used for the analog and input/output (I/O) circuitry, and the lower-voltage for the core-digital-logic devices.” *Id.* And because analog and I/O regions must handle higher operating voltages, “the analog and I/O devices require thicker gate oxides than the core logic devices.” *Id.* As such, forming different transistors with different gate oxide thickness can be used where needed, for instance where both higher-voltage and lower-voltage transistors are desired on the same chip.

104. The prior art teaches different processes to vary oxide thickness across different transistors on the same chip. *See, e.g.,* Karve, Ex.1226, 3:45-4:36 (describing formation of nMOS with thicker gate oxide than core nMOS), Figs. 5-6, 8; Luo, Ex.1227, 5:61-7:58 (describing formation of nMOS-DGO and nMOS core devices). As

explained by one textbook, one process is to include two oxidation steps “with a masked etch-step in between to remove the first oxide from regions intended to have thinner oxide.” Wolf-4, Ex.1214, 121. Yet another process uses nitrogen implants to impede oxide growth in certain areas, which occurs because “the rate of thermal-oxidation on silicon is reduced by nitrogen implants.” *Id.* “Hence, nitrogen implantation into the silicon substrate prior to the oxidation process can be used to facilitate the implementation of such ‘dual-gate-oxide’ ICs.” *Id.*

VI. THE ’425 PATENT

A. Overview

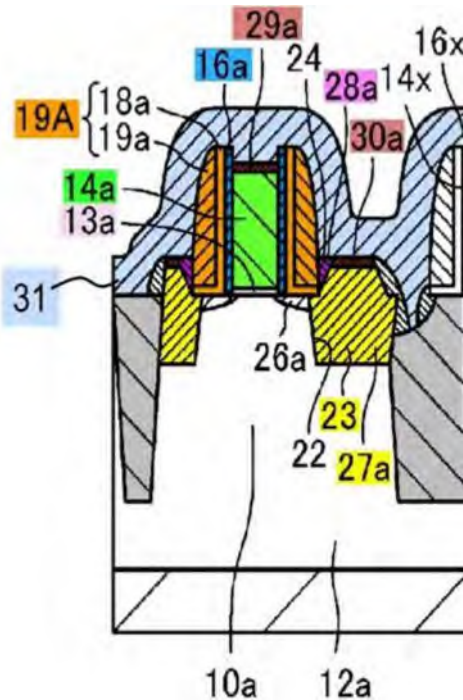
105. The ’425 patent issued on December 9, 2014, from U.S. Patent Application No. 13/528,526, filed on June 20, 2012. The ’425 patent, Ex.1001, cover. The ’425 patent claims priority to Japan Patent Application No. 2010-002225, filed on January 7, 2010. *Id.*

106. The ’425 patent is directed to “semiconductor devices and methods for fabricating the semiconductor devices,” including “semiconductor devices which include a metal-insulator-semiconductor field-effect-transistor (MISFET) having a source/drain region including a silicon compound layer.” The ’425 patent, Ex.1001, 1:15-22.

107. The ’425 patent recognized it was known, prior to the invention thereof, to use a “distortion technique of enhancing the drive capability of a MISFET . . . by

applying a stress to the channel region . . . to improve the performance of a semiconductor integrated circuit device.” The ’425 patent, Ex.1001, 1:23-27. It was previously established in the prior art that, for PMOS devices, “if a *compressive* stress is applied to the channel region in the gate length direction, the mobility of carriers is increased, and the drive capability . . . is enhanced.” The ’425 patent, Ex.1001, 1:27-43 (emphasis added) (citing examples). Likewise, for NMOS devices, the ’425 patent recognizes the widely acknowledged fact from prior art that, “the drive capability . . . is enhanced” “if a *tensile* stress is applied to the channel region of the active region in the gate length direction.” The ’425 patent, Ex.1001, 3:1-4 (emphasis added). The related principal is relevant, as PMOS devices require *compressive* stress to improve drive capability, “the drive capability . . . is reduced” in PMOS devices if tensile stress is applied to the channel region. The ’425 patent, Ex.1001, 3:1-4. The ’425 patent aims to address the decrease in compressive stress within PMOS device regions when a tensile stress-inducing film is applied to improve NMOS channel conductivity in NMOS devices. *See* The ’425 patent, Ex.1001, 3:13-17.

108. FIG. 6B, excerpted and annotated below, illustrates an exemplary PMOS device of the ’425 patent. *See* The ’425 patent, Ex.1001, 13:66-15:5, FIG. 6B



10a: active region
 13a: gate insulating film
 14a: gate electrode
 16a: offset spacer
 19A: sidewall
 22: trench
 23: silicon compound layer
 24: space
 27a: p-type source/drain region
 28a: first stress-relief film
 29a: first silicide layer
 30a: second silicide layer
 31: stress insulating film

The '425 patent, Ex.1001, FIG. 6B (excerpted, annotated)

109. Annotated FIG. 6B above shows a PMOS transistor with known structures, such as “first stress-relief film 28a . . . formed in [a] space 24 located between the silicon compound layer 23 [e.g., SiGe] and the first sidewall 19A.” The '425 patent, Ex.1001, 13:6-8. Above, “stress insulating film 31 can be separated from the channel region in the first active region 10a by the thicknesses of the protruding portion of the silicon compound layer 23 and the first stress-relief film 28a.” The '425 patent, Ex.1001, 16:2-6. The '425 patent teaches this results in making it “possible to reduce the tensile stress applied from the stress insulating film

31 to the channel region in first active region 10a in the gate length direction” and “to prevent a reduction in drive capability.” The ’425 patent, Ex.1001, 16:6-11.

B. Claims

110. The ’425 patent has 15 claims, including one independent claim numbered 1, and dependent claims numbered 2-15. The ’425 patent, Ex.1001, 19:48-22:16. Claims 1, 3, 4, 7, 8, and 11 are the Challenged Claims.

111. The Challenged Claims are reproduced below:

1. [Preamble]: A semiconductor device comprising:

1[a]: a first MIS transistor, wherein:

1[b]: the first MIS transistor includes:

1[c]: a first gate insulating film formed on a first active region in a semiconductor substrate,

1[d]: a first gate electrode formed on the first gate insulating film,

1[e]: a first sidewall spacer formed on a side surface of the first gate electrode,

1[f]: a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region, and

1[g]: a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress,

1[h]: an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode,

1[i]: a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer,

1[j]: the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween, and the first stress-relief film is not in direct contact with the side surface of the first gate electrode.

The '425 patent, Ex.1001, 19:48-20:10.

3. The semiconductor device of claim 1, further comprising: a first silicide layer formed on the first gate electrode; and a second silicide layer formed on the first source/drain region which includes the silicon compound layer.

The '425 patent, Ex.1001, 20:16-20.

4. The semiconductor device of claim 1, wherein the first stress-relief film is formed on a side surface of the silicon compound layer.

The '425 patent, Ex.1001, 20:21-23.

7. The semiconductor device of claim 1,

7[a]: wherein the first MIS transistor is a p-type MIS transistor,

7[b]: the first stress is a compressive stress, and

7[c]: the second stress is a tensile stress.

The '425 patent, Ex.1001. 20:35-38.

8. [Preamble]: The semiconductor device of claim 1,

8[a]: wherein the silicon compound layer is a SiGe layer,

8[b]: the stress insulating film is a silicon nitride film, and

8[c]: the first stress-relief film is a silicon oxide film.

The '425 patent, Ex.1001, 20:39-42.

11. [Preamble]: The semiconductor device of claim 1, further comprising:

11[a]: a second MIS transistor, wherein:

11[b]: the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate,

11[c]: a second gate electrode formed on the second gate insulating film,

11[d]: a second sidewall spacer formed on a side surface of the second gate electrode,

11[e]: a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer, and

11[f]: the stress insulating film formed on the second active region to cover the second gate electrode, the second sidewall spacer, and the second source/drain region.

The '425 patent, Ex.1001, 20:60-21:8.

C. Summary of the Prosecution History

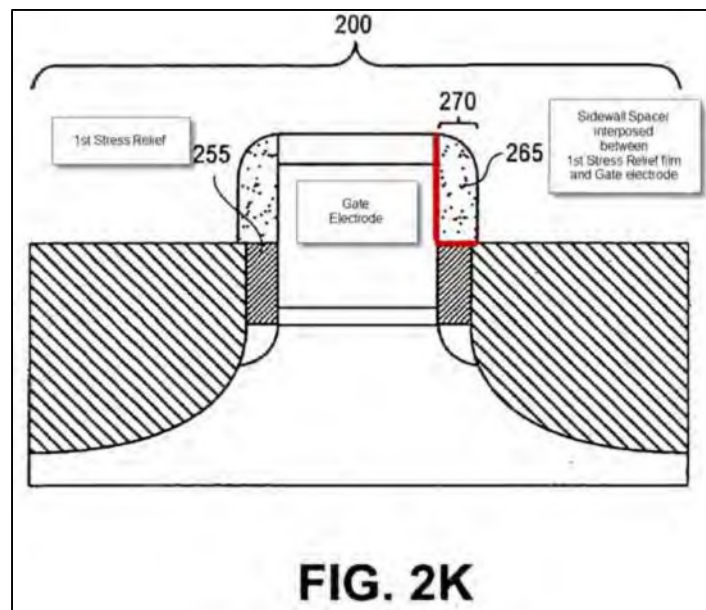
112. The File History of the '425 patent includes two office actions and two amendments. *See generally* File History, Ex.1002.

113. In the initial Office Action, the Examiner contended that the original claims were anticipated. Ex.1002, 1-11. As per the Examiner, the prior art revealed “a first stress-relief film[] . . . formed in a space between the silicon compound layer[] and the first sidewall[].” File History, Ex.1002, 5.

114. In response, the Applicant argued that the alleged stress-relief film from the prior art was “formed in a space between the gate electrode 202 and the epitaxial source/drain region 218, and in **direct** contact with a side surface of the gate electrode 202.” File History, Ex.1002, 23-24. Accordingly, the Applicant amended independent claim 1 to additionally recite that “the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween.” File History, Ex.1002, 18. Thus, according to the Applicant, the resulting combination of prior art still would fail “to disclose or suggest a device in which *the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween.*” File History, Ex.1002, 23-24.

115. In the subsequent Final Office Action, the Examiner disagreed with Applicant’s arguments and upheld the position that the prior art rendered the amended claims obvious. *See* File History, Ex.1002, 27-39. According to the Examiner, the purported stress-relief film in the prior art was “formed on the side surface of the first gate electrode(202) with the first sidewall spacer(265) interposed therebetween.” File History, Ex.1002, 30. The Examiner specifically disagreed because “[t]he claim language does not specify whether [the stress-relief film] can or cannot be in direct contact with a side surface of the gate electrode (202).” File History, Ex.1002, 36. The Examiner also included the annotated figure below,

utilizing the red annotation to indicate that the upper portion 265 (first sidewall spacer) in the prior art is positioned between the first gate electrode 202 and the first stress-relief film 255. *See* File History, Ex.1002, 36-37 (“[T]he right triangle sides of the first sidewall spacer (265) is [*sic*] bordering with the first gate electrode (255 [*sic*:202]) and the first stress-relief film (255).”).



File History, Ex.1002, 37 (annotated)¹

116. In response, the Applicant further revised claim 1 to state: “the first stress-relief film is not in direct contact with the side surface of the first gate

¹ I have been informed that this colored figure was obtained by downloading the document from the U.S. Patent Office’s Patent Center website in .docx format and appears as it did in the .docx document.

electrode.” File History, Ex.1002, 42-43. Applicant explained the proposed amended “is intended to address the Examiner’s interpretation of the prior art.” File History, Ex.1002, 48. The Applicant also maintained that the prior art “would still fail to disclose or suggest a device in which *the first stress-relief film is not in direct contact with the side surface of the first gate electrode.*” File History, Ex.1002, 48-49.

117. The Examiner subsequently approved the claims. Ex.1002, 51-58. In the statement of reasons for allowability, the Examiner still asserted that the prior art demonstrated “a first stress-relief film . . . formed in a space between the silicon compound layer and the first sidewall spacer,” and that “the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween.” File History, Ex.1002, 56-57. However, the Examiner determined that the prior art neither disclosed nor made obvious that “the first stress-relief film is not in direct contact with the side surface of the first gate [electrode].” File History, Ex.1002, 57 (emphasis omitted).

VII. LEVEL OF ORDINARY SKILL IN THE ART

118. I understand that there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including the educational level of active workers in the field at the time of the alleged invention, the sophistication of the

technology, the type of problems encountered in the art, and the prior art solutions to those problems.

119. In determining the characteristics of a hypothetical person of ordinary skill in the art of the '425 patent at the time of the alleged invention, I considered several things, including the type of problems encountered in this field, and the rapidity with which innovations were made. I also considered the sophistication of the technology involved, and the educational background and experience of those actively working in the field, and the level of education that would be necessary to understand the '425 patent. Finally, I placed myself back in the relevant periods of time, and considered the state of the art and the level of skill of the engineers working in this field in those times.

120. It is my opinion that a POSITA at the time of the '425 patent would have had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or a related field, and three years of work experience in semiconductor design and manufacturing, including with respect to planar transistors, or equivalent work experience. Additional graduate education might compensate for a deficiency in experience, and vice-versa.

121. I also note that my opinions provided in this Declaration would not change in view of any minor modifications to this level of skill.

VIII. CLAIM CONSTRUCTION

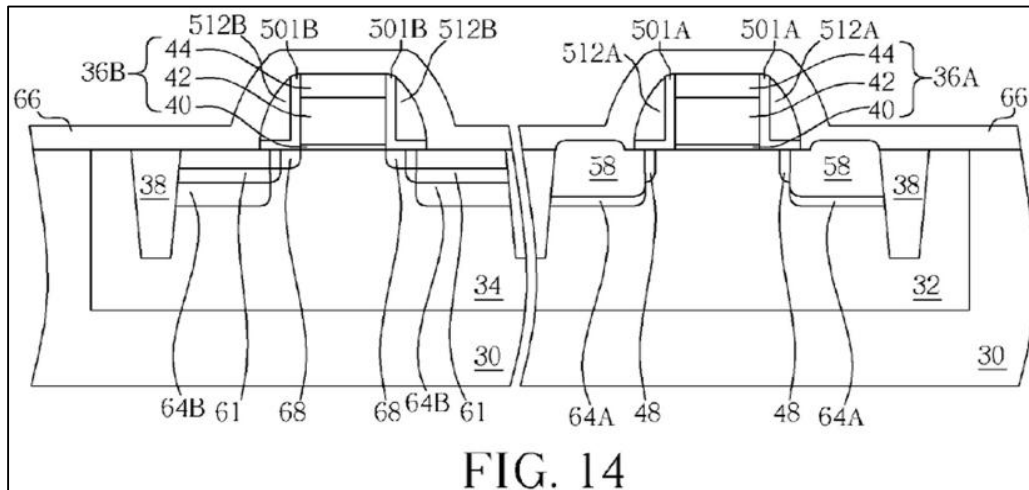
122. It is my opinion that for purposes of this proceeding, the claim terms need not be construed to resolve the prior art issues presented in this Petition.

123. Nothing in this section should be construed as expressing any opinion as to whether the claims constitute patentable subject matter under 35 U.S.C. § 101, or whether they satisfy the definiteness, enablement, best mode, or written description requirements under 35 U.S.C. § 112.

IX. OVERVIEW OF THE PRIOR ART

A. Wu922 (Ex.1005)

124. Wu922 discloses “strained CMOS” structures with, *e.g.*, a PMOS transistor region 31 and an NMOS transistor region 33. Wu922, Ex.1005, ¶¶[0009], [0017], FIG. 14. Wu922 explains that “[a] plurality of first active area[s] and a plurality of second active area[s] are defined on the semiconductor substrate 30,” whereby “[e]ach of the first active area[s] includes a first-type well and a gate structure, and each of the second active area[s] includes a second-type well and a respective gate structure thereon.” Wu922, Ex.1005, ¶[0017]. In a “preferred embodiment,” Wu922’s “first active area is a PMOS transistor region 31” and the “second active area is an NMOS transistor region 33.” Wu922, Ex.1005, ¶[0017].

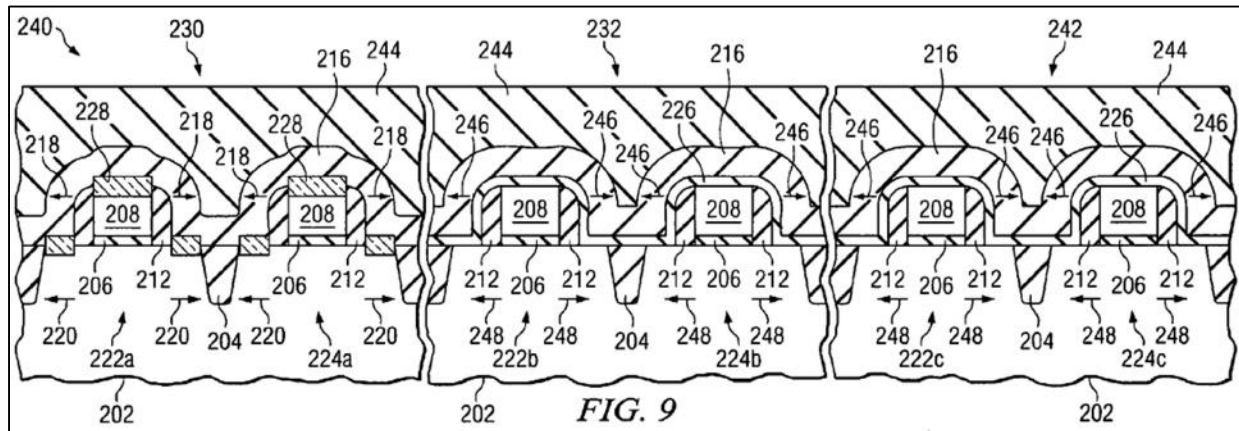


Wu922, Ex.1005, FIG. 14

125. In the PMOS transistor region, Wu922 discloses “an epitaxial layer 58 of silicon germanium” that is “slightly projected from the top surface of the semiconductor substrate 30 to compress the channel.” Wu922, Ex.1005, ¶¶[0021], [0041], FIG. 14. Further, Wu922 discloses removing a “sacrificial layer 52” that creates a space between the raised edge of the SiGe epitaxial layer 58 and the sidewall structure of the gate electrode. *See, e.g.*, Wu922, Ex.1005, ¶¶[0022], [0042], FIGS. 5-7, 13-14. After depositing sidewalls 512A, Wu922 teaches a strained contact etch stop layer (CESL) 66 deposited over PMOS transistor 31 and NMOS transistor 33. Wu922, Ex.1005, ¶¶[0025], [0044], FIG. 14. Further, “a self-aligned silicide process (salicide process) is optionally performed” in certain areas before depositing CESL 66. Wu922, Ex.1005, ¶¶[0024], [0043].

B. Alvarez (Ex.1006)

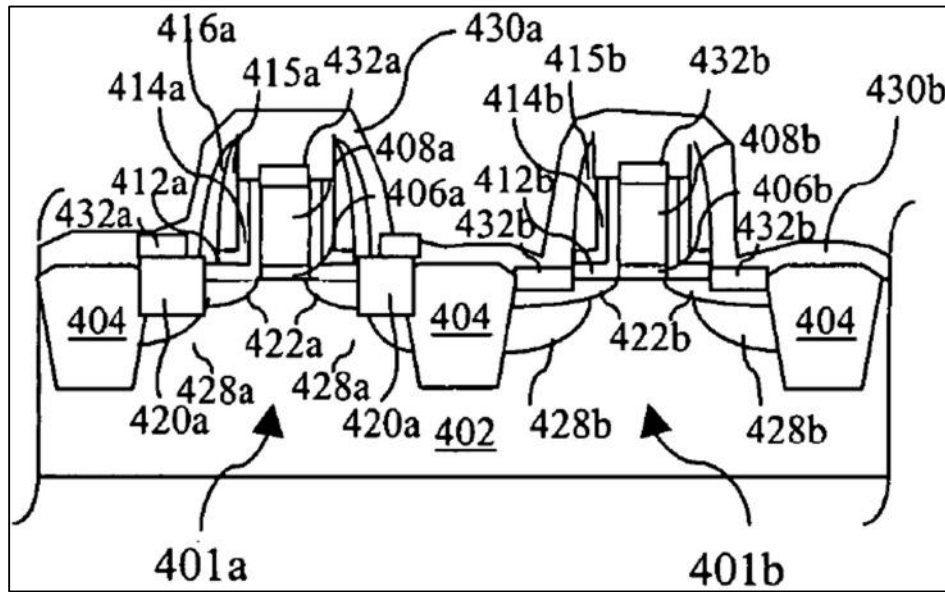
126. Alvarez discloses a “semiconductor device” with “a plurality of active areas,” such as silicide region 230, non-silicide region 232, and stress-control region 242, each including PMOS transistors 224x and NMOS transistors 222x. Alvarez, Ex.1006, Abstract, ¶¶[0037]-[0038], FIGS. 9-11. In regions 232 and 242, Alvarez discloses a “stress-controlling material 226” to mitigate stress caused by a “stress-increasing material 216” and to prevent silicidation in certain regions, such as “non-silicide region” 232 and “stress-control region” 242. Alvarez, Ex.1006, ¶¶[0035], [0037], [0045], [0049], [0054], [0078], FIG. 9. Alvarez teaches that “stress-controlling material 226 reduces the amount that the stress-increasing material 216 increases the first amount of stress by about the second amount of stress 218 less the third amount of stress 246, for example.” Alvarez, Ex.1006, ¶¶[0045], [0049], [0054], FIG. 9. For example, “stress-increasing material 216 is formed over the at least one first active area and over the stress-controlling material 226,” and “the stress-controlling material 226 reduces the amount that the stress-increasing material 216 increases a stress level” in the active area. Alvarez, Ex.1006, ¶[0061], FIG. 9; *see also* Alvarez, Ex.1006, ¶[0054], Tbl. 1.



Alvarez, Ex.1006, FIG. 9

C. Cheng817 (Ex.1008)

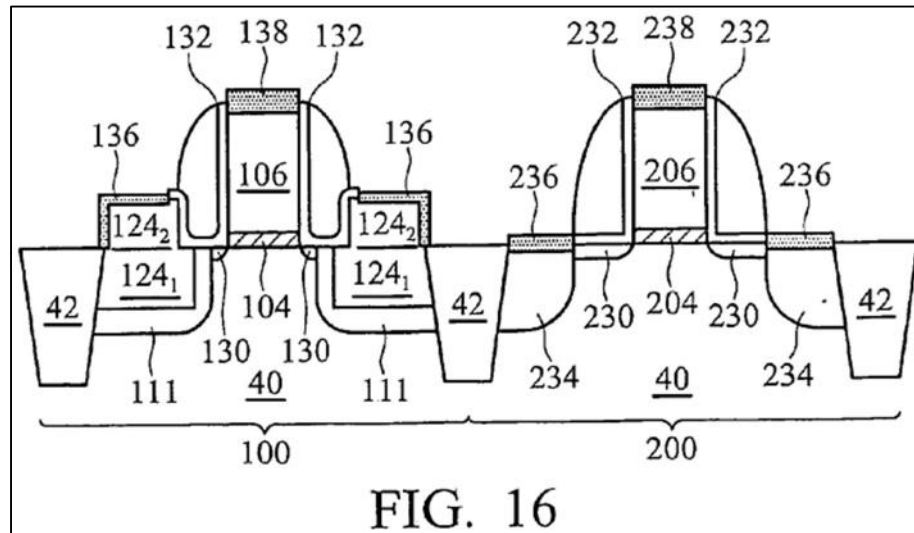
127. Cheng817 discloses “a P-type MOS device” 401a and an “N-type MOS device” 401b. Cheng817, Ex.1008, ¶[0056], Fig. 4j. The PMOS device 401a includes raised SiGe “source and drain regions 420a” that are “built-up” to “extend above the substrate surface” and impart compressive stress to the PMOS channel. Cheng817, Ex.1008, ¶[0022], [0065], Fig. 4j. Additionally, an etch stop layer 430a/430b may be a “tensile film” or “compressive film” made of “silicon nitride (Si_xN_y).” Cheng817, Ex.1008, ¶[0070], Fig. 4j.



Cheng817, Ex.1008, Fig. 4j

D. Wang906 (Ex.1009)

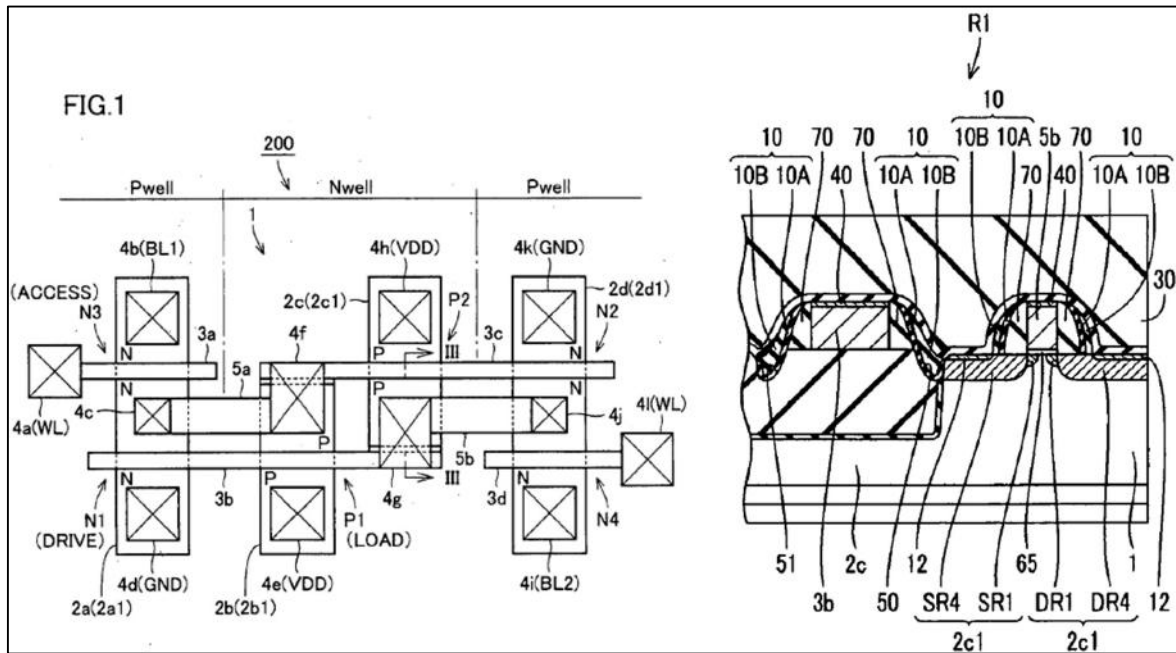
128. Wang906, similar to Cheng817, discloses “a region 100 for forming a pMOS device and a region 200 for forming an nMOS device.” Wang906, Ex.1009, ¶[0023], FIG. 16. Wang906 explains that “to strengthen the compressive stress applied by the silicon [SiGe] alloy regions 124 [in pMOS devices], the silicon alloy regions 124 preferably outgrow the top surface of the substrate 40, forming raised portions 124₂,” having a height between 10 and 70 nm. Wang906, Ex.1009, ¶[0031], FIG. 16.



Wang906, Ex.1009, FIG. 16

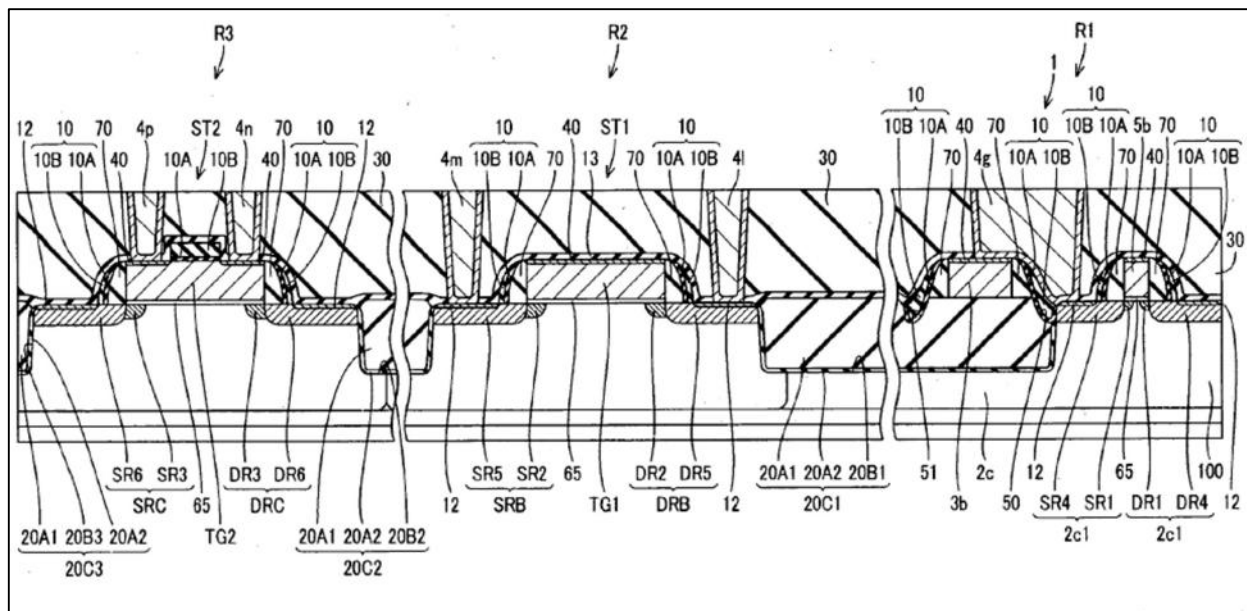
E. Saito825 (Ex.1010)

129. Saito825 discloses an SRAM circuit with PMOS transistors P1-P2 and NMOS transistors N1-N4. Saito825, Ex.1010, ¶¶[0056]-[0059], FIG. 1. During manufacturing, Saito825 discloses that recesses 50 form in isolation regions 20A1 located next to polysilicon wirings 3b and 3c in PMOS active regions 2b and 2c. Saito825, Ex.1010, ¶¶[0096], [0099], FIGS. 1, 5, 17. Saito825 teaches “fill[ing] up” recesses 50 by depositing silicon oxide layer 10A and nitride layer 10B. Saito825, Ex.1010, ¶¶[0074]-[0076], ¶¶[0112]-[0113], FIGS. 3, 11, 12, 21. Saito825 also discloses a nitride insulating film 13 formed over the entire wafer. *See* Saito825, Ex.1010, ¶[0091] (explaining that FIG. 12 includes “well region[s] of various conductivity types”), FIGS. 12, 21.



Saito825, Ex.1010, FIG. 1

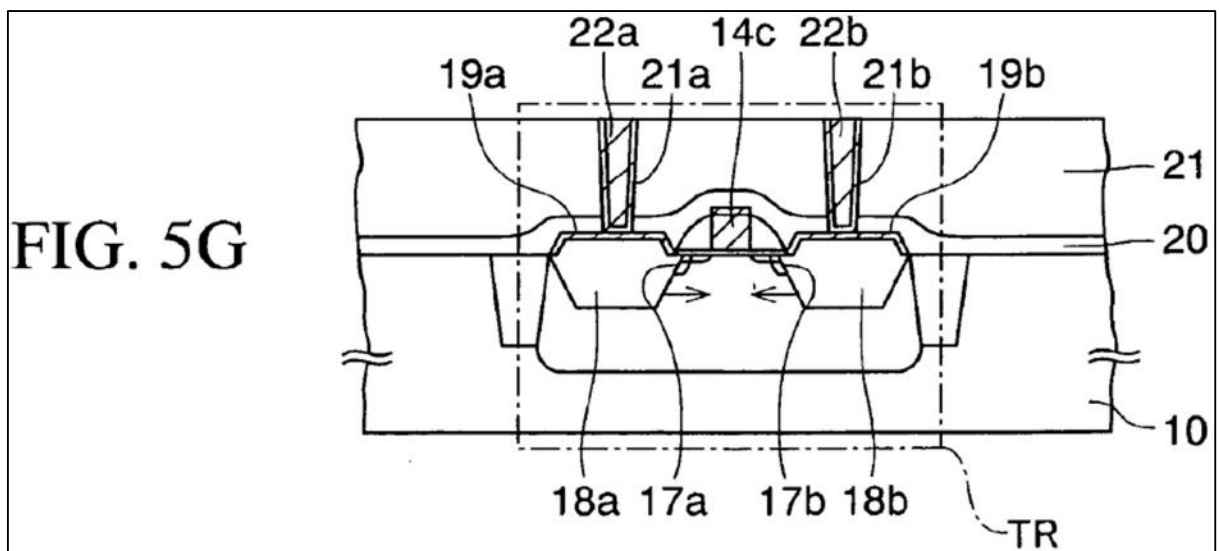
Saito825, Ex.1010, FIG.21
(excerpted)



Saito825, Ex.1010, FIG. 21

F. Fukutome (Ex.1011)

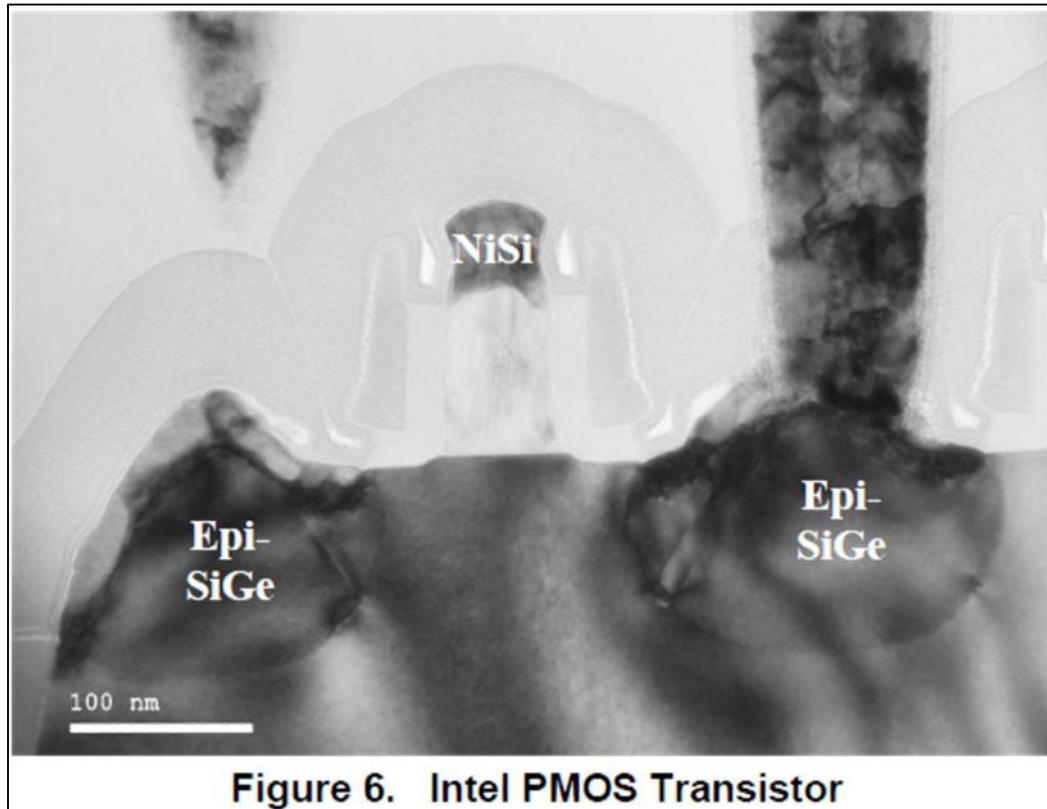
130. Fukutome discloses a semiconductor device in which faceted epitaxial SiGe “source/drain material layers 18a and 18b” are grown to “positions higher than the surface of the silicon substrate.” Fukutome, Ex.1011, ¶¶[0092], [0096], [0100], FIGS. 5D-5G. According to Fukutome, growing the SiGe higher than the substrate “increases the distances between the p-n junction at the bottom surface of the n-well 12 and conductive plugs to be formed on the source/drain material layers 18a and 18b later.” Fukutome, Ex.1011, ¶[0100]. Fukutome explains that, in such cases, “a junction leakage in the above-described p-n junction can be suppressed, and the reliability of the transistor can be improved.” Fukutome, Ex.1011, ¶[0100]. Fukutome also teaches a silicon nitride layer 20 deposited “on the entire surface” of the device. Fukutome, Ex.1011, ¶[0106], FIG. 5G.



Fukutome, Ex.1011, FIG. 5G

G. James (Ex.1012)

131. James describes various “physical transistor structures” of commercial devices, including devices made by Intel’s 90nm process (codenamed Prescott or P1262). James, Ex.1012, 1-5, Figs. 1-3, 5-12; Ex.1436. James explains that, in Prescott, “[l]ocalized tensile stress is applied to the channels of NMOS devices by a highly stressed nitride sealant layer” that “increases electron mobility by ~10%.” James, Ex.1012, 2, Figs. 5, 6. Prescott’s “PMOS transistors (Figure 6) use epitaxial SiGe source/drains to create compressive stress,” which “improves hole mobility by as much as 50%.” James, Ex.1012, 2, Fig. 6. The raised PMOS SiGe source/drain regions in FIG. 6 have “[c]rystalline facets” that “reduc[e] the series resistance” and apply compressive stress that “counteract[s]” the “tensile stress from the nitride layer.” James, Ex.1012, 2, Fig. 6.



James, Ex.1012, Fig. 6

X. SPECIFIC GROUNDS FOR PETITION

A. Ground 1

132. In my opinion, Wu922 in view of Alvarez renders obvious all of the Challenged Claims 1, 3, 4, 7, 8, and 11 of the '425 patent (Ground 1).

1. Motivation to Combine Wu922 and Alvarez

133. In my opinion, a POSITA would have found it obvious to combine Wu922 and Alvarez to arrive at the invention claimed in claims 1, 3, 4, 7, 8, and 11 of the '425 patent. Specifically, in my view, a POSITA would have found it obvious to make Wu922's CESL 66 layer apply tensile stress, as Alvarez illustrates (for

example, Alvarez's tensile stress-insulating layer 216/316/416), and to further apply a stress-relief layer, similar to the one described by Alvarez (such as Alvarez's stress-control layer 226/326/426), selectively to Wu922's transistors. The prior art demonstrates that there are known advantages to both structures and a POSITA would have reasonably expected success by modifying Wu922 in view of Alvarez.

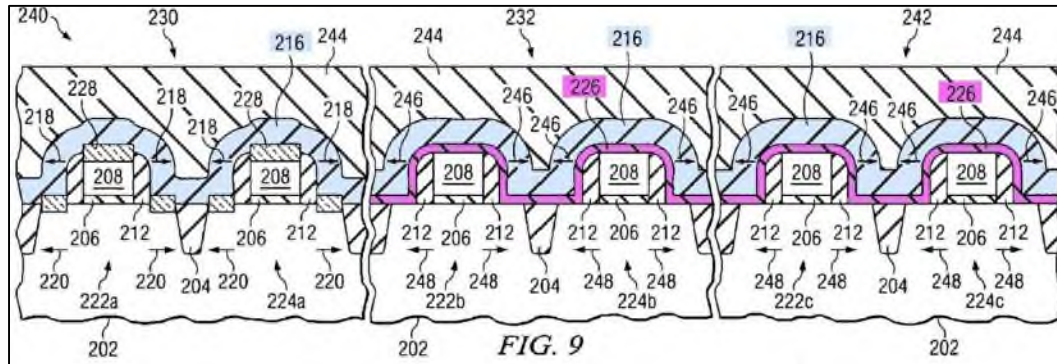
a. A POSITA would have found it obvious to make Wu922's CESL layer apply tensile stress and to further form a stress-relief layer.

134. In my opinion, a POSITA would have found it obvious to implement a tensile CESL in Wu922's design because it is well known that the tensile stress of the CESL would enhance the performance of Wu922's nFETs by increasing electron mobility within those devices.

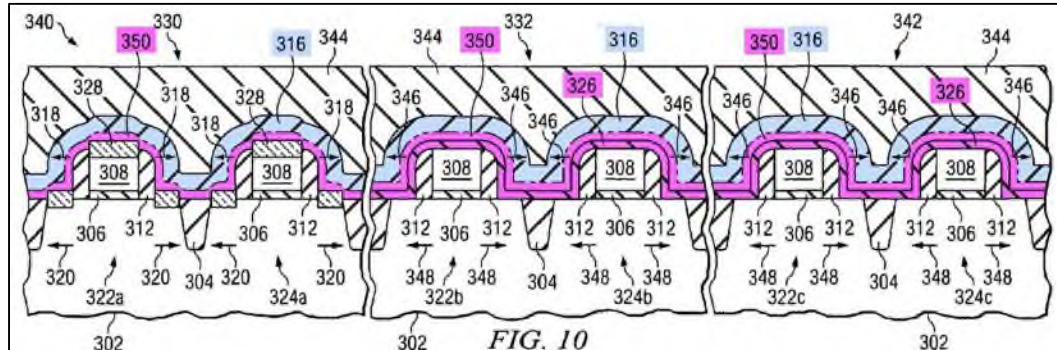
135. In my opinion, a POSITA would have found it obvious to incorporate a stress-controlling layer, disclosed in Alvarez², into Wu922's transistor structure to

² Alvarez clarifies that similar features are indicated by common designations in the last two digits of reference numerals. For instance, x06 denotes the gate dielectric material. Alvarez, Ex.1006, ¶[0039], ¶[0063]. Similarly, x22 refers to nFETs, whereas x24 refers to pFETs. See Alvarez, Ex.1006, ¶¶[0025], [0028], [0063]. Therefore, I may refer to multiple designations for a feature, but even if I refer to

alleviate the effects of tensile stress CESL on pFETs. As taught by Alvarez, this combination would be apparent to a POSITA as it effectively balances enhancements to both nFET and pFET devices, which in turn, streamlines manufacturing and reduces cost.



Alvarez, Ex.1006, FIG. 9 (annotated)



Alvarez, Ex.1006, FIG. 10 (annotated)

only one feature (*e.g.*, 226), the discussion generally encompasses Alvarez's commentary or analogous features (*e.g.*, 326, 426).

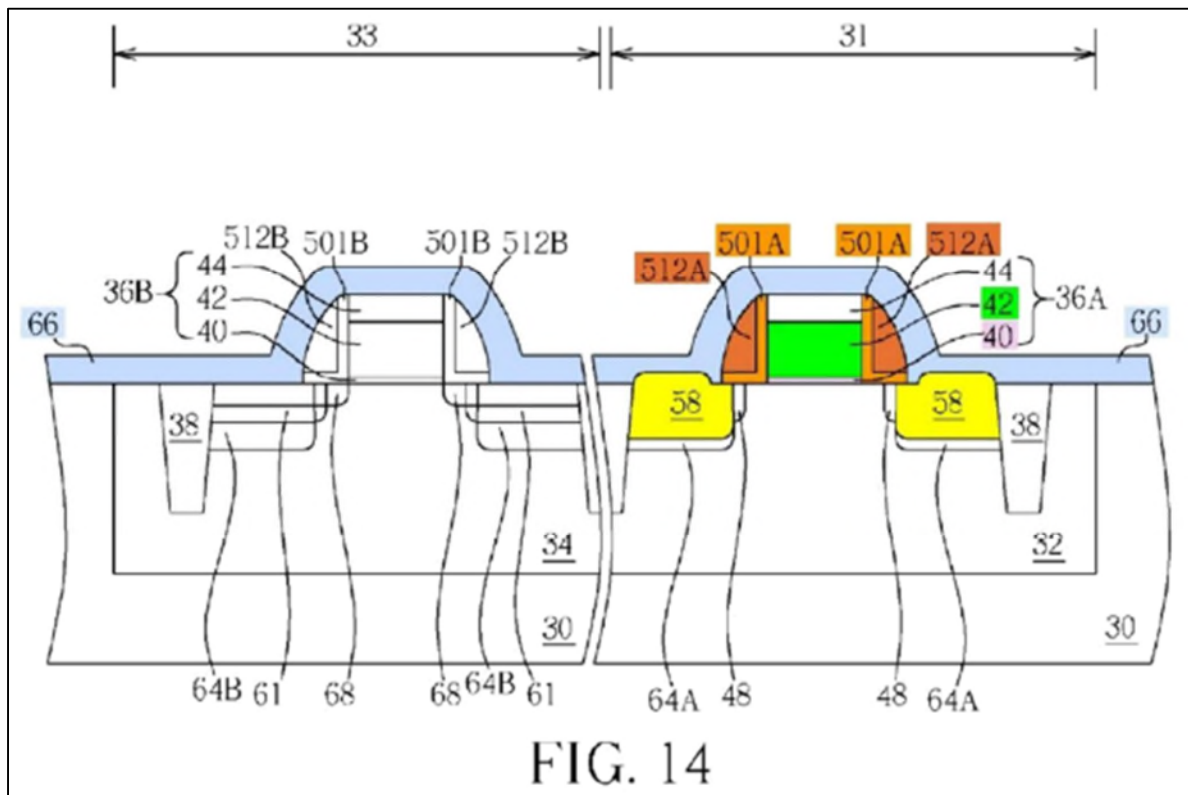
136. As I explain in further detail below, a POSITA would have found it obvious to combine certain teachings from Alvarez with Wu922's transistor.

137. First, a POSITA would have found it obvious to form a stress-controlling layer (such as Alvarez's stress-control layer 226/326/426), over both pFET and nFET devices. *See* Alvarez, Ex.1006, FIGS. 9 and 10 (annotated). Second, a POSITA would have found it obvious to implement Wu922's transistor structure into various circuit regions, such as Alvarez's silicide region 230/330, non-silicide region 232/332, and stress-control region 242/342. In this Wu922-Alvarez combination, the pFET in the stress-control region 242/342 would satisfy the claim elements of claims 1, 4, 7 and 8 of the '425 patent. Likewise, this Wu922-Alvarez combination the pFET in the silicide region 330 would satisfy the claim elements of claims 1 and 3 of the '425 patent and the nFET in silicide region 230 would satisfy the claim elements of claim 11 of the '425 patent. Alternatively, the nFET in stress-control region 242/342 would satisfy the claim elements of claim 11 of the '425 patent.

(1) Wu922 as part of the Wu922-Alvarez Combination

138. Wu922 discloses "a method of forming a strained CMOS transistor to improve CMOS transistor performance and reliability." Wu922, Ex.1005, ¶[0009], FIGS. 1-7, 9-14. Wu922 explains that the semiconductor device includes a first

active region 31, such as “PMOS transistor region 31.” Wu922, Ex.1005, ¶¶[0017], [0023], [0038], [0042]-[0043], FIGS. 1-7, 9-14. PMOS transistor region 31 includes conventional structures and layers, such as gate structure 36A, which includes “a gate dielectric layer 40, a gate 42, and a cap layer 44.” Wu922, Ex.1005, ¶¶[0017], [0039], FIGS. 1-7, 9-14. To demonstrate these and other features, an annotated version of Wu922’s FIG. 14 is below.



Wu922, Ex.1005 FIG. 14 (annotated)

139. Wu922’s gate structure includes sidewalls 501A, 502A. Wu922, Ex.1005, ¶¶[0017], ¶¶[0039], FIGS. 1-7, 9-14. Following the formation of sidewalls 501A and 502A, Wu922 details the addition of an extra spacer to the sacrificial layer

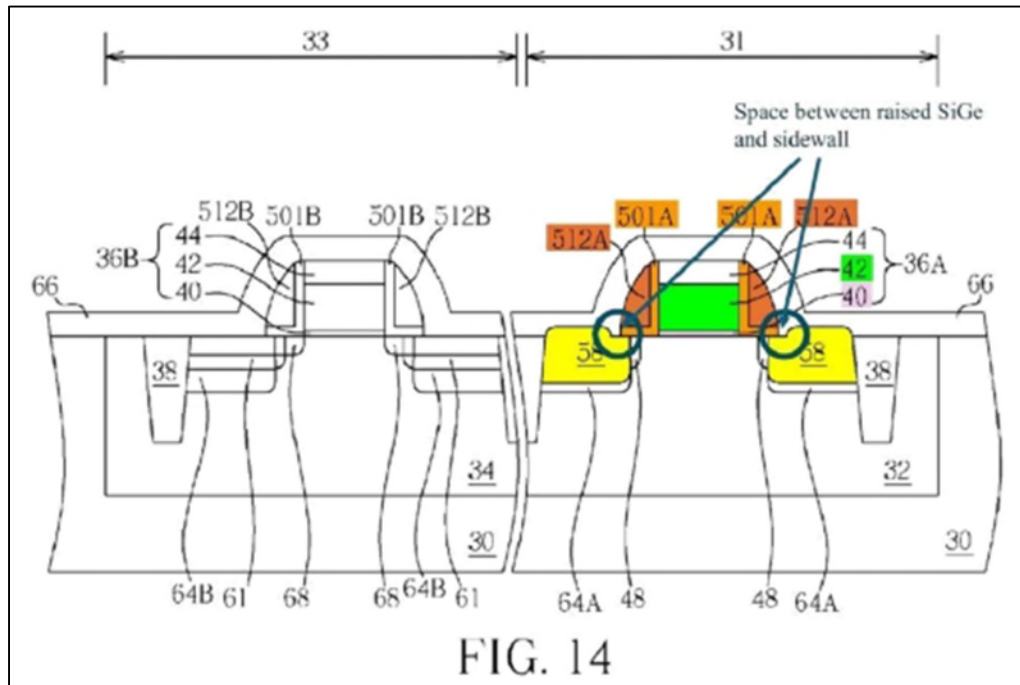
52. Wu922, Ex.1005, ¶¶[0019]-[0022], ¶¶[0040]-[0041], FIGS. 2-4, 10-12. For example, “sacrificial layer 52, such as a silicon nitride layer, is formed covering the semiconductor substrate 30.” Wu922, Ex.1005, ¶[0040]. After forming the sacrificial layer 52 on the gate structure 36A, Wu922 outlines the process of etching a trench 56 into the silicon substrate, followed by the growth of an epitaxial silicon germanium (SiGe) layer 58 within recess 56, or a trench. Wu922, Ex.1005, ¶¶[0019]-[0021], [0040]-[0041], FIGS. 2-4, 10-12. More specifically, Wu922 explains that “an etch process . . . is performed . . . to etch the sacrificial layer 52 and the semiconductor substrate 30 beside the gate structure 36A” to form “recess 56 . . . on the surface of the N well 32 beside the gate structure 36A.” Wu922, Ex.1005, ¶¶[0040], [0020], FIGS. 2-3, 10-11.

140. Wu922 explains that the epitaxial SiGe layer 58 can be grown so that its top surface is elevated above the substrate surface. This configuration, as Wu922 describes, and that a POSITA would readily understand, induces compressive stress in the PMOS channel region of the PMOS transistor region 31. Wu922, Ex.1005, ¶¶[0019]-[0021], [0040]-[0041], FIGS. 2-4, 10-12. The “epitaxial layer 58 is slightly projected from the top surface of the semiconductor substrate 30,” which a POSITA would have understood that this describes the epitaxial SiGe layer 58 being elevated above the surface of substrate 30, as illustrated in FIGS. 4-7 and 12-14. Wu922,

Ex.1005, ¶¶[0021], [0041], FIGS. 4-7, 12-14. The raised epitaxial layer 58 is separated from the sidewalls 501A/502A by the width of sacrificial layer 52.

141. The SiGe layers 58 of Wu922 have “a lattice constant greater than that of the semiconductor substrate 30.” Wu922, Ex.1005, ¶¶[0021], [0040]-[0041], FIGS. 4-5, 12. Wu922 further explains that this larger lattice constant “compress[es] the channel” under PMOS transistor 31, which improves PMOS hole mobility and PMOS performance, which was already well known in the prior art (*see* Section V.F above). Wu922, Ex.1005, ¶¶[0021], [0041], FIGS. 4, 12.

142. After forming the raised SiGe source/drains 58, Wu922 teaches that the sacrificial layer 52 and sidewall 502A are then removed by etching. Wu922, Ex.1005, ¶¶[0022]-[0024], [0042]-[0043], FIGS. 5-7, 13-14. Sidewall spacer 512A is then “formed on the sidewalls of the gate structures 36A, 36B” using “the same . . . processes [as] for forming the first spacers 502A.” Wu922, Ex.1005, ¶¶[0024], FIGS. 7, 14. The foregoing process results in a space between sidewalls 501A/512A and the raised SiGe 58, as annotated FIG. 14 shows below. Wu922, Ex.1005, ¶¶[0022]-[0024], [0032], [0042]-[0043], FIGS. 5-7, 13-14.



Wu922, Ex.1005 FIG. 14 (annotated)

143. Wu922 teaches that “a self-aligned silicide process (salicide process) is optionally performed,” after growing the raised SiGe layer 58. Although this silicide process is not shown in Wu922 FIG. 14. Wu922, Ex.1005, ¶[0024]; *see also* Wu922, Ex.1005, ¶[0043] (“[A] self-aligned silicide process is optionally performed to form a silicide layer (not shown) on the surfaces of the gate structures or the source/drain.”), ¶[0036] (“A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”), ¶[0055] (same). To do this, “[a] metal layer, including titanium (Ti), cobalt (Co), nickel (Ni), palladium (Pd), platinum (Pt) or the like, is deposited. And

a rapid thermal process is performed to form a silicide layer (not shown) on the surfaces of the source/drain 64A, 64B.” Wu922, Ex.1005, ¶[0024].

144. Wu922 teaches the next step of processing which is “form[ing] a contact etch stop layer (CESL) 66 on the surface of the gate structures 36A, 36B, the second spacers 512A, 512B, and the sources/drains 64A, 64B,” as well as oxide layers 501A/501B. Wu922, Ex.1005, ¶¶[0025], [0039], [0044], FIGS. 7, 14. Wu922 discloses that the CESL 66 may be “a strained silicon material, i.e. silicon nitride.” Wu922, Ex.1005, ¶[0025]. Wu922 teaches that it can “exert tensile stress or compressive stress upon the MOS transistor” to “reduce carrier mobile resistance [,] thereby improving carrier mobility and MOS transistor performance,” which was already well understood in the art. Wu922, Ex.1005, ¶[0005]; *See* Section V.F above.

145. While Wu922 teaches that the CESL may be strained silicon, it does not explicitly state it exerts tensile stress to improve NMOS electron mobility or whether it exerts compressive stress to improve PMOS hole mobility. *See* Wu922, Ex.1005, ¶¶[0005], [0025]; *See* Section V.F above. Given Wu922’s general description of improving “carrier mobility,” and not clarifying whether that is “hole” or “electron” improvement, would have suggested to a POSITA that Wu922’s CESL layer 66 could exert either tensile stress to improve nFET carrier (electron) mobility or compressive stress to improve pFET carrier (hole) mobility. Again, it was already

widely recognized in the field that employing a strained CESL could enhance the carrier mobility of MOS transistors. *See* Section V.F above.

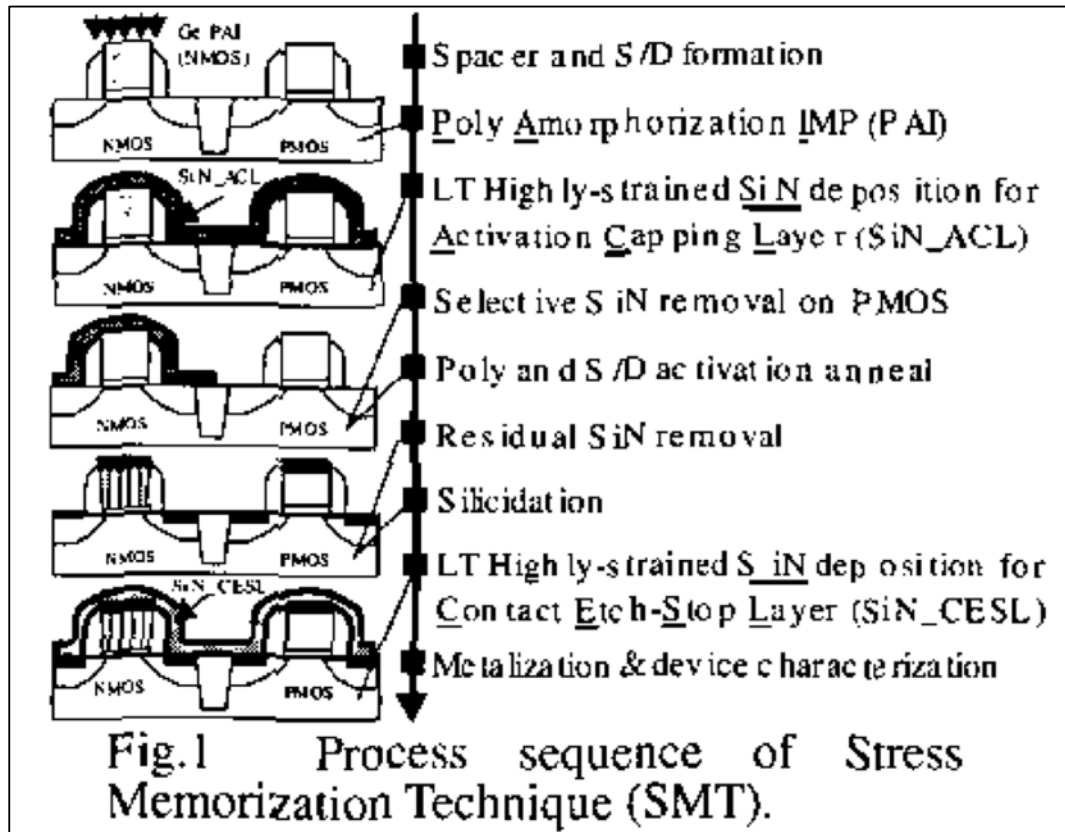
(2) Well known improvements in transistor devices to use a tensile stress inducing CESL and a strain-buffer layer

146. It is my opinion that a POSITA, in reading Wu922 in view of Alvarez, would have found it obvious to modify the formation of Wu922's CESL 66 layer to cause a tensile stress for the purpose of improving pFET carrier (electron) mobility. First, it was well known in the prior art that a tensile CESL improves carrier mobility this technique had been implemented in several generations of commercial devices. *See* Section V.F above. Second, a POSITA would have recognized that the Wu922-Alvarez tensile CESL 66 would have benefitted nFETs that are "relatively difficult to improve" while simultaneously, the pFET carrier mobility would have been improved by Wu922's compressive epitaxial SiGe layer 58. Hsu823, Ex.1506, ¶[0039].

147. It was already well known in the prior art that forming SiN layers on top of P and N transistors causing channel benefits as transistors continued to decrease in size. *See* Section V.F.

148. For example, Chen-2004 demonstrates that it was well known to use tensile CESL over both the PMOS and NMOS transistors. As can be seen in Chen-2004 Fig. 1, below, the "SiN_CESL" or the "LT Highly strained SiN deposition for

Contact Etch Stop Layer” is formed over both the PMOS and NMOS structures. Chen-2004, Ex.1103, Fig. 1. Chen-2004 further teaches a stress memorization technique. *See e.g.*, Chen-2004, Ex.1103 (“An advanced stress memorization technique (SMT) for device performance enhancement is presented. A high-tensile nitride layer is selectively deposited on the n⁺ poly-Si gate electrode as a stressor with poly amorphization implantation in advance. And, this high-tensile nitride capping layer will be removed after the poly and S/D activation procedures. The stress modulation effect was found to be enhanced and memorized to affect the channel stress underneath the re-crystallized poly-Si gate electrode after this nitride layer removal. More than 15% current drivability improvement was obtained on NMOS without any cost of PMOS degradation.”).



Chen-2004, Ex.1103 Fig. 1

149. A POSITA would have known that, historically, nFETs generally exhibited superior performance compared to pFETs, due to the naturally higher mobility of electrons in silicon within nFETs, as opposed to the mobility of holes in pFETs. A POSITA would have recognized the proposed Wu922-Alvarez combination balances carrier mobility improvements in pFETs and nFETs with other considerations, such as ease of manufacturing. A POSITA would have further recognized that the stress from a tensile CESL could be counteracted by a strain-buffer layer effectively mitigating the negative side effects of tensile stress on pFET mobility. *See* Section V.G above. In fact, Alvarez itself teaches that a strain-

buffering layer (e.g., stress-control layer 226/326/426 and/or 350/450) mitigates the adverse effects of a tensile CESL on pFET carrier (hole) mobility.

150. In my opinion, a POSITA also would have recognized other benefits to the strain-buffer layer in Alvarez, such as to match “performance requirements of transistors in the particular regions,” “tun[ing]” channel strain, and streamlining manufacturing by reducing steps and, in turn, reducing cost. *See* Alvarez, Ex.1006, ¶¶[0028], [0032], [0034]-[0035], [0045]-[0046], [0053]-[0055], [0063]-[0068], [0075], [0078], Tbl. 1, FIGS. 8-11.

151. Alvarez itself suggests that it was well known in the art that “[s]ome NMOS FETs have demonstrated performance enhancement” introducing “tensile stress to the channel region,” but “some PMOS FETs may suffer from decreased performance” when a tensile nitride material layer is deposited over the PMOS transistor. Alvarez, Ex.1006, ¶[0025]; *See also* Section V.F above; Morin-2007, Ex.1528, 355-56. Alvarez also explains that the negative effects on PMOS carrier mobility from using a tensile CESL formed over both the NMOS and PMOS can be mitigated by applying an intermediate stress-controlling layer 226/326/426 and/or 350/450 beneath the tensile CESL layer. (216/316/416). Alvarez, Ex.1006, ¶¶[0028], [0032], [0034]-[0035], [0045]-[0046], [0053]-[0055], [0063]-[0068], [0075], [0078], Tbl. 1, FIGS. 8-11. Alvarez states that, “due to the presence of the first material or stress-controlling material 226 in the second region 232 and the third

region 242, the stress-increasing material 216 has less of an impact [on] the stress 248 in the channel regions of the [PMOS] transistors . . . 224b, . . . and 224c in the second region 232 and the third region 242.” Alvarez, Ex.1006, ¶[0049]; *See also* Alvarez, Ex.1006, ¶¶[0043], [0053]-[0055], [0065], Tbl. 1 (“The first material 226 preferably comprises a material adapted to screen or control the amount of stress that a subsequently deposited stress-increasing material has on an underlying material layer, such as channel regions . . .”).

152. Alvarez describes the stress-control layer 226/326/426 and/or 350/450 benefits include: (i) reducing the negative side effects from stress-inducing layer 216/316/416 on the PMOS channel regions by “screen[ing] or control[ling] the amount of stress” imparted by the stress-inducing layer 216/316/416; (ii) selectively blocking the forming of silicide in certain circuit regions, such as non-silicide region 232 and stress-control region 242; and (iii) streamlining manufacturing by reducing steps and, in turn, reducing cost. Alvarez, Ex.1006, ¶¶[0037], [0043], [0049], [0061], [0063]-[0064], [0069]-[0075], [0078], [0081], FIGS. 9-13.

153. In my opinion, a POSITA would have realized that the benefits discussed above may be interrelated in some instances. For example, Alvarez discloses using stress-control layer 226/326/426 to selectively block the forming of silicide in non-silicide region 232 and stress-control region 242, for example. Alvarez, Ex.1006, ¶¶[0045]-[0047], [0068], [0078], FIGS. 7-10. Moreover, by not

etching the stress-control layer 226/326/426 and/or 350/450 before depositing a tensile CESL 216/316/416, manufacturing is streamlined by reducing steps. Alvarez, Ex.1006, ¶[0033] (describing “costly and time-consuming” process” of depositing both tensile and compressive layers), [0045] (explaining that stress-control layer 226 is also used as silicide masking material layer), [0074], [0078] (explaining that using stress-control layer as silicide masking layer “results in a cost savings”).

154. In my opinion, a POSITA, would have found it obvious to achieve these various benefits by modifying Wu922’s strained CESL 66 to cause a tensile strain for the purpose of improving NMOS carrier mobility. *See* Alvarez, Ex.1006, ¶¶[0053]-[0055] (“Preferably the material and deposition process for the first [stress-controlling] material 226 is selected or tuned to achieve the amount of control desired on the stress of the underlying material layer, e.g., such as the channel regions of the transistors 222b, 224b, 222c, and 224c in the second region 232 and the third region 242, of the effect of the second [stress-increasing] material 216.”), FIGS. 9-11, Tbl. 1. Further, in my opinion a POSITA also would have also found it obvious to achieve these benefits by adding a stress-buffering film, like Alvarez’s layer 226/326/426 and/or 350/450, to Wu922’s structure for the purpose of (i) mitigating (e.g., screen or control) the negative side effects of the tensile CESL on PMOS carrier mobility by “tuning” the relevant films to balance the stresses applied to the NMOS and PMOS transistors; and (ii) block undesired formation of silicide

in certain regions (e.g., regions analogous to Alvarez's non-silicide region 232/332 and stress-control region 242/342); and (iii) streamlining manufacturing by reducing steps and, in turn, reducing cost. Alvarez, Ex.1006, ¶¶[0037], [0049], [0053]-[0055], [0061], [0070]-[0075], [0078], [0081], FIGS. 9-11.

155. Alvarez explains that its stress-controlling layer 226/326/426 and/or 350/450 formed between the source/drain regions and a tensile CESL has benefits compared to applying a tensile CESL over the nFETs and a compressive CESL over the pFETs. Although the two dual-strain CESL layers may have some advantages, Alvarez states it results in “stress mismatch . . . at the lateral interface of the tensile stress material layer and the compressive stress material layer,” and is more “costly and time-consuming” than using one CESL with one kind of strain. Alvarez, Ex.1006, ¶¶[0033], [0074] (explaining that the “lateral interface between a tensile stress layer and a compressive stress layer is avoided” using a single CESL over both nFETs and pFETs); *See also* Hsu823, Ex.1506, ¶[0039] (preferable to apply tensile CESL across both NMOS and PMOS devices because “the performance of PMOS devices can be easily improved with SiGe stressors, while the performance of NMOS devices is relatively difficult to improve”); Morin-2007, Ex.1528,, 355-56; Bohr, Ex.1527, ¶¶[0038]-[0039], FIG. 6.

156. In my opinion, a POSITA, would have been motivated to implement Alvarez's teaching to Wu922 and form a stress-controlling layer (Alvarez layers

226/326/426 and/or 350/450) over pFETs in certain circuit regions, including certain silicide regions (like Alvarez region 330), non-silicide regions (like Alvarez non-silicide regions 232/332), and stress-control regions (like Alvarez stress-control regions 242/342) because of benefits discussed above. Alvarez, Ex.1006, ¶¶[0037], [0049], [0061], [0074]-[0075], [0078], [0081], FIGS. 9-13. A POSITA would have identified that modifying Wu922's structure in view of Alvarez would "tun[e]" the stress in certain circuit regions such that it "is introduced or increased in some regions, but . . . is reduced or controlled" in others. Alvarez, Ex.1006, ¶¶[0026], [0080]; *See also* Alvarez, Ex.1006, ¶¶[0053]-[0055]. A POSITA would have known that different transistors in different circuit regions have distinct requirements (Alvarez, Ex.1006, ¶¶[0027], [0032]), and accordingly, a POSITA would have been motivated to apply Alvarez's teachings to Wu922's FETs to tune stress and selectively control silicide formation in a streamlined way.

(3) The Wu922-Alvarez Combination

157. A POSITA would have found the Wu922-Alvarez combination desirable because "it [wa]s important to work to improve nMOS transistors" with tensile CESL, as "other solutions [e.g., SiGe] . . . can enhance the pMOS performances," as recognized by others in the industry. Morin-2007, Ex.1528, 356; *See also* Hsu823, Ex.1506, ¶[0039] ("[T]he performance of PMOS devices can be easily improved with SiGe stressors, while the performance of NMOS devices is

relatively difficult to improve”); Bohr, Ex.1527, ¶¶[0038]-[0039], FIG. 6. Chidambaram-2004, Ex.1104, Abstract (“A highly compressive SiGe layer, in close proximity to the channel, results in large hole mobility improvements. HRTEM based lattice parameter extractions confirm the compressive strain in the channel.”). A POSITA would have recognized that the Wu922-Alvarez combination achieve this goal since it allows “stress on underlying materials [to be] introduced or increased in some regions, but wherein the stress introduced in other regions is reduced or controlled.” Alvarez, Ex.1006, ¶[0026]. Using the Wu922-Alvarez combination, a POSITA would have reasonably expected the tensile CESL to improve nFET carrier mobility and expected the stress-buffering film would balance the compressive stress in Wu922’s pFETs due to epitaxial SiGe layer 58. Alvarez, Ex.1006, ¶¶[0026], [0053]-[0055]; Wu922, Ex.1005, ¶¶[0021], [0041]; *See* Sections V.F and V.G above.

158. Alvarez teaches that stress-controlling layer 226/326/426 and/or 350/450 reduces, but does not eliminate, the stress from a tensile CESL. The CESL “tunes” the stress to achieve a balance between advantages and disadvantages across different regions. *See* Alvarez, Ex.1006, ¶¶[0049], [0053]-[0055], [0064], Tbl. 1. That is, this structure helps “achieve the amount of control desired on the stress of the underlying material layer, e.g., such as the channel regions of the transistors 222b, 224b, 222c, and 224c.” Alvarez, Ex.1006, ¶[0053]; *See also* Alvarez, Ex.1006,

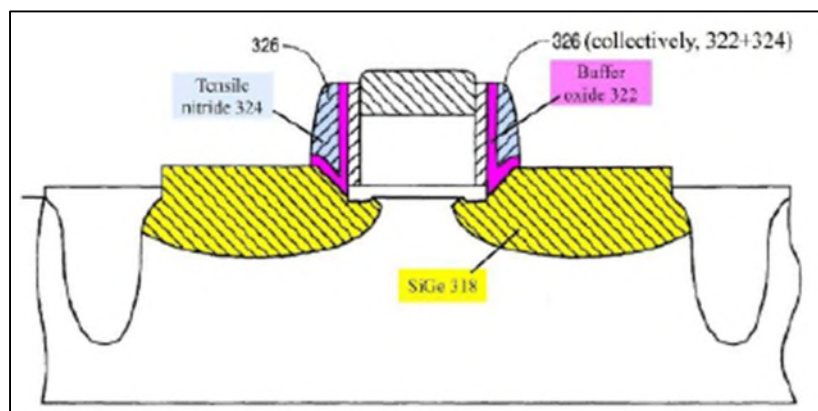
¶¶[0054]-[0055], [0080]. By precisely adjusting the stress in devices using Wu922's transistor design, a POSITA would have reasonably anticipated achieving optimal stress levels in the nFET and pFET channel regions, while effectively managing silicidation and minimizing manufacturing costs. Alvarez, Ex.1006, ¶¶[0037], [0049], [0061], [0063]-[0064], [0069]-[0075], [0078], [0081], FIGS. 9-13.

159. Alvarez demonstrates this in a few embodiments. In FIG. 9, stress-controlling film 226/326/426 extends over both nFETs 222b/222c and pFETs 224b/224c. In FIG. 10, an additional stress-controlling film 350/450 extends over both nFETs 322a/322b/322c and pFETs 324a/324b/324c. In FIG. 11, the stress-controlling film (or films) extends over only the pFETs to further enhance nFET performance. Alvarez, Ex.1006, ¶¶[0065]-[0068]. A POSITA would have readily identified these various alternatives as obvious design choices when integrating Alvarez's teachings with Wu922 or any comparable MISFET structure that incorporates a strained CESL film.

160. Alvarez, along with others in the field, advocated for the use of a tensile CESL over both nFETs and pFETs, incorporating an intermediate stress-relief layer to counteract negative impacts on pFETs—a strategy that was widely acknowledged. *See* Sections V.F-V.G above; Wu922, Ex.1005, ¶[0005]; Murthy556, Ex.1430, 9:10-29 (explaining that “[o]xide layer 322 buffers the large stress” in silicon nitride layer 324 overlying it), FIG. 8; Doris, Ex.1429, ¶[0034] (“A tensile barrier etch stop layer

80, such as CVD or PECVD SiN, is applied to the entire wafer.”), ¶[0042] (disclosing “a neutral buffer layer between the compressive spacer and the tensile etch stop layer”), Figs. 2, 14, 15; Lee870, Ex.1431, ¶[0029], ¶¶[0046]-[0067] (explaining that an intermediate stress relief layer “with neutral stress or opposite stress relative to the [CESL]” reduces or eliminates any pFET performance degradation because it “reduces the tensile stress in the channel region”), FIG. 5; Cheng810, Ex.1432, ¶¶[0022]- [0031], Fig. 1F (describing similar).

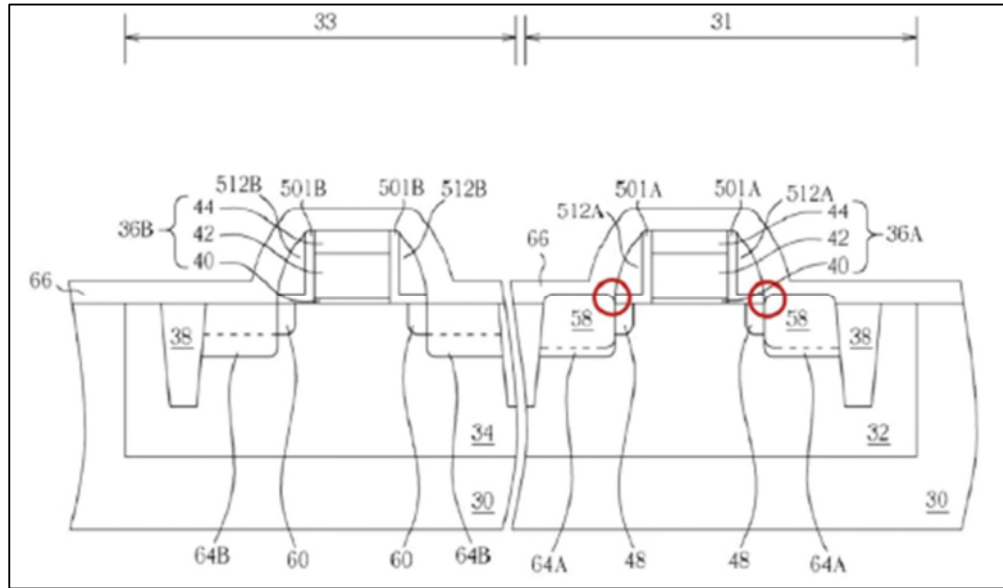
161. As one example, Murthy556 discloses an “[o]xide layer 322 [that] buffers the large stress” in an overlying silicon nitride layer 324. Murthy556, Ex.1430, 9:27-29. Murthy556’s FIGS. 7-9 show a pFET with SiGe source/drains 318. A buffer oxide layer 322 is formed in the space between the SiGe and the gate electrode spacer. Murthy556, Ex.1430, 8:59-9:43, FIGS. 7-9. In annotated FIG. 9 below, oxide buffer layer 322 mitigates the tensile effect of a tensile silicon nitride layer 324. Murthy556, Ex.1430, 9:27-33.



Murthy556, Ex.1430, FIG. 9 (annotated)

162. Doris also discloses that a silicon dioxide film formed between the SiGe and a tensile layer can “prevent[] the tension from materially adversely influencing the charge carrier mobility in the pFET 150” by “defin[ing] a neutral buffer layer between the compressive spacer [220] and the tensile etch stop layer [340].” Doris, Ex.1429, ¶[0034], ¶[0042]; *See also* Lee870, Ex.1431, ¶[0021,] ¶¶[0028]-[0029], ¶¶[0046]-[0067] (teaching that a stress buffering layer “with neutral stress or opposite stress relative to the [CESL]” effectively reduces or eliminates any pFET degradation by “reduc[ing] the tensile stress in the channel region”), FIGS. 2-5; Cheng810, Ex.1432, ¶¶[0022]-[0031], Figs. 1B-1F (describing similar).

163. As seen in Wu922 FIGS. 7 and 14 below, Wu922’s CESL 66 is formed in the space between the epitaxial SiGe layer 58 and the gate sidewalls 501A/512A. Therefore, when combining Wu922 and Alvarez, a POSTA would understand the stress-buffering film (like Alvarez 226/326/426 and/or 350/450) would be placed under Wu922’s CESL 66, such that the stress-buffering film would form in that space between the epitaxial SiGe layer 58 and the gate sidewalls 501A/512A.



Wu922, Ex.1005, FIG. 7 (annotated)

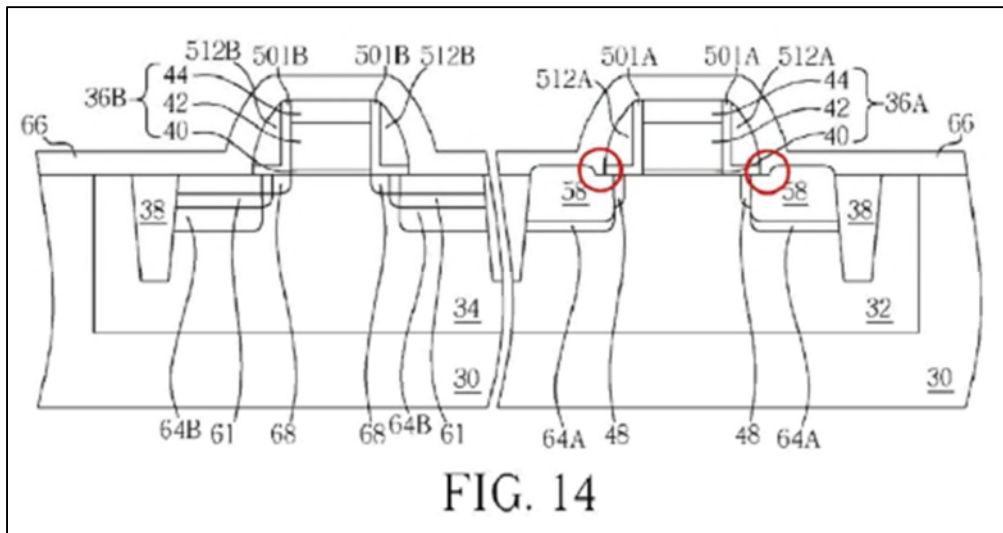
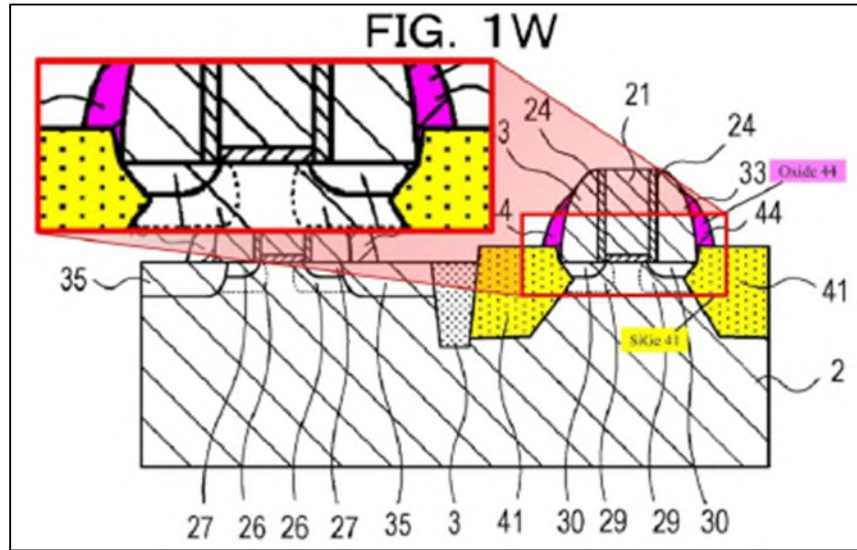


FIG. 14

Wu922, Ex.1005, FIG. 14 (annotated)

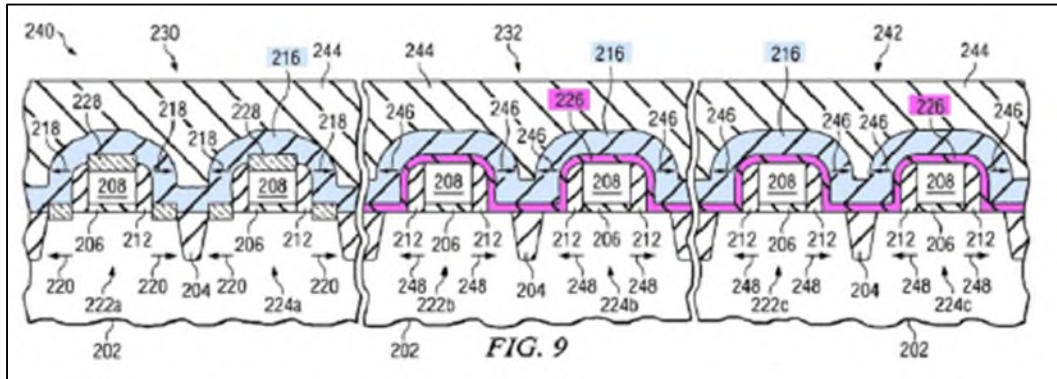
164. Still further, Miyashita also confirms this in FIGS. 1V-1W. In FIG. 1W below, the silicon oxide layer 44 is deposited in a space between a raised, faceted SiGe source/drain 41 and a gate sidewall spacer. Miyashita, Ex.1435, ¶¶[0052]-[0053], FIGS. 1V-1W; *See also* Murthy556, Ex.1430, 8:59-9:43, FIGS. 7-9.



Miyashita, Ex.1435, FIG. 1W

(4) Realization of the Wu922-Alvarez combination

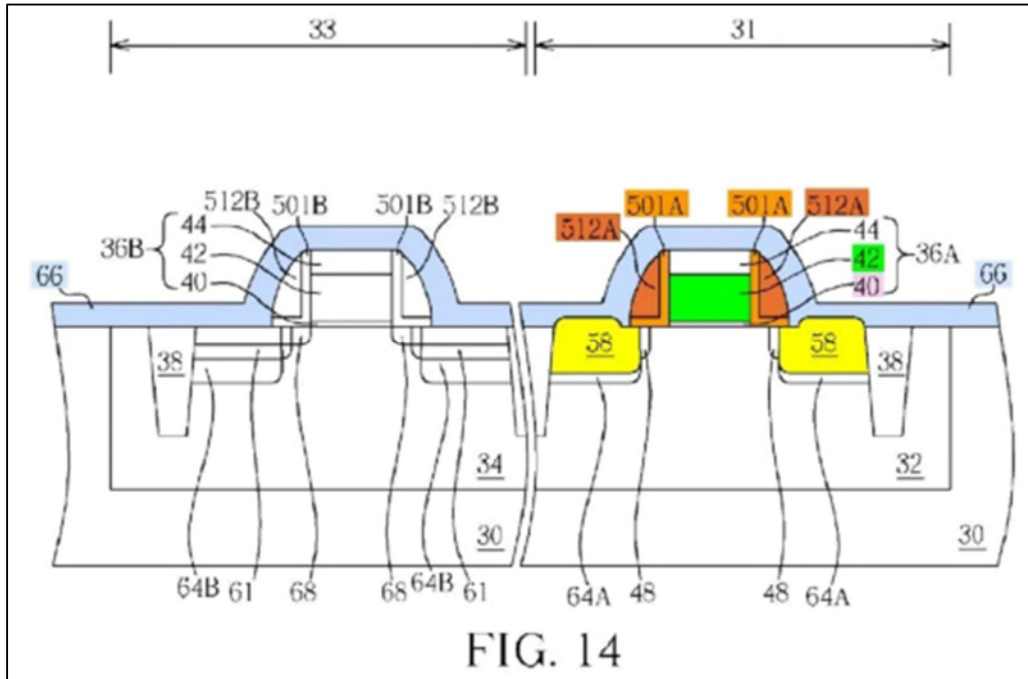
165. As explained above, a POSITA would have been motivated to add a stress-buffering layer (like Alvarez 226/326/426 and/or 350/450) to Wu922's FETs in certain circuit regions (like Alvarez's silicide region 330, non-silicide region 232/332, and stress-control region 242/342) to selectively block the formation of silicide and/or alleviate tensile CESL stress on pFETs with less steps and in a cost-effective way. *See* Alvarez, Ex.1006, ¶¶[0033], [0037], [0045], [0063]-[0075], [0078]. FIG. 9 below represents a "preferred embodiment . . . wherein a stress-controlling material [226] is disposed over some regions of a semiconductor device, but not over other regions of the semiconductor device." Alvarez, Ex.1006, ¶[0013].



Alvarez, Ex.1006, FIG. 9

166. The stress-controlling layer 226 also permits selective silicide formation and mitigates CESL stress in non-silicide region 232 and stress-control region 242 while allowing silicidation in silicide region 230. Alvarez, Ex.1006, ¶[0037]; *See also* Alvarez, Ex.1006, ¶¶[0045]-[0047], FIGS. 7-9. In silicide region 230, the tensile CESL 216 directly contacts the gate sidewalls of transistors 222a/224a in region 230, whereas in regions 232 and 242, stress-controlling layer 226 is used for “tuning” the stress applied to the FETs. *See* Alvarez, Ex.1006, ¶¶[0026], [0049], [0053]-[0055], [0061], [0081], Tbl. 1, FIG. 9.

167. In Wu922’s FIG. 14 below, the pFET is on the right and the nFET is on the left. Wu922, Ex.1005, ¶¶[0017], [0038], FIG. 14. It also shows “a [contact etch stop layer] CESL 66 on the surface of the gate structures 36A [PMOS], 36B [NMOS], the second spacers 512A [PMOS], 512B [NMOS], and the sources/drains 64A [PMOS], 64B [NMOS].” Wu922, Ex.1005, ¶[0044]. CESL 66 is “a strained silicon material, i.e. silicon nitride.” Wu922, Ex.1005, ¶[0025].



Wu922, Ex.1005 FIG. 14 (annotated)

168. The combined Wu922-Alvarez Figure A, below, shows one example of the combination. As detailed above, a POSITA would have found it obvious to deposit a stress-controlling layer (like Alvarez 226/236/426 and/or 350/450) just before forming Wu922's CESL 66 to which exerts tensile stress (like Alvarez's layer 216/316/416). Again, for the reasons noted above, the stress-controlling layer be formed under the CESL 66 and form in the space in between Wu922's epitaxial SiGe source/drain regions 58 and gate sidewall spacers 501A/512A. Figure A depicts the device in the equivalent of Alvarez's stress-control region 242 (also referred to as

third region 242).³ It would also appear in the equivalent of Alvarez's non-silicide region 232 (also referred to as second region 232).

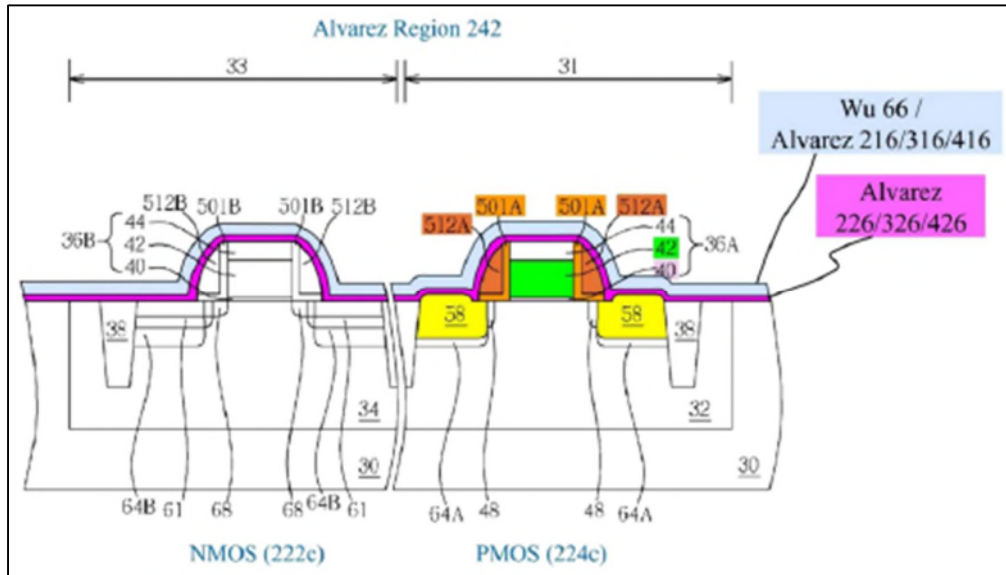


Figure A

169. Composite Wu922-Alvarez Figure B below shows an example of how this embodiment may appear in all the circuit regions described in Alvarez's FIG. 9.

³ To maximize the beneficial stress on the nFETs and pFETs, Alvarez's stress-control layer may be removed from nFETs. *See* Alvarez, Ex.1006, ¶¶[0065]-[0068], FIG. 11. This embodiment would have been obvious to a POSITA.

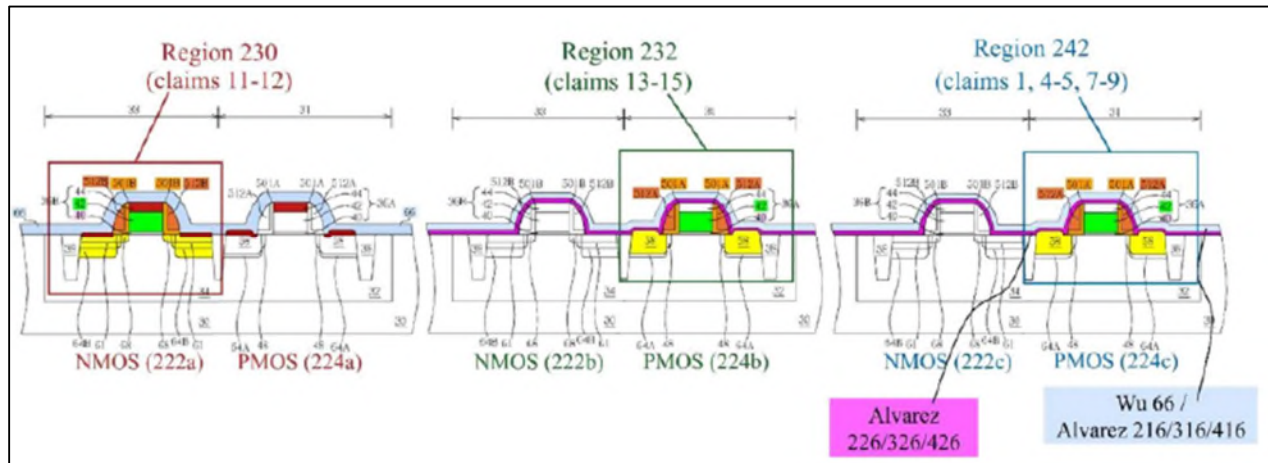
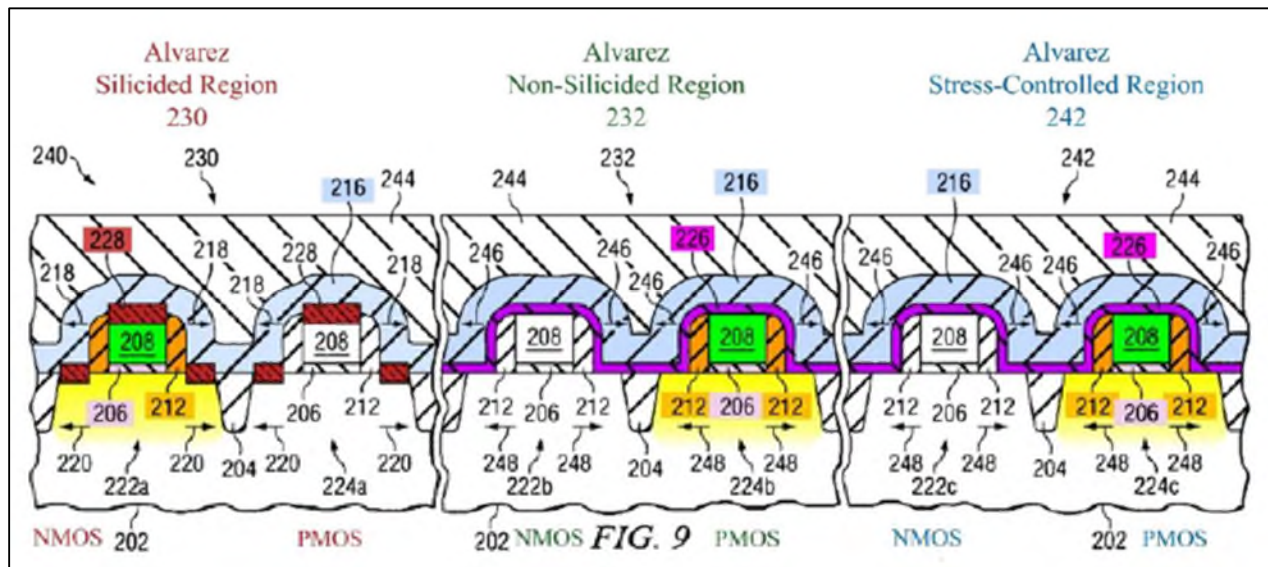


Figure B



Alvarez, Ex.1006, FIG. 9 (annotated)

170. In this Declaration, I discuss the Wu922-Alvarez combination for claims 1, 3, 4, 7, 8, and 11. For ease of understanding, the list below and the annotations at the top of Figure B above explain the relevance of each circuit region to the claims:

- **Claims 1, 4, 7, and 8** map to Figure A's exemplary implementation of pFET 224c in Alvarez's stress-control region 242, as Figure B shows above (also shown in Figure A above). *See* Section X.A.2, X.A.4-6 below.
- **Claims 1 and 3** alternatively map to the exemplary implementation of pFET 324a in Alvarez's silicide region 330, as Figure A' shows in the section below where I discuss claim 3 (similar to Figure A above, but with Wu922's optional silicide added). *See* Section X.A.2-3 below.
- **Claim 11** map to nFET 222a in silicide region 230 of Figure B above. Alternatively, claim 11 maps to nFET 222c in stress-control region 242 of Figure B above (also shown in Figure A above). *See* Section X.A.7 below.

171. When compared to a method involving a tensile CESL over nFETs and a compressive CESL over pFETs, a POSITA would have understood that the combination of Wu922 and Alvarez described earlier—which implements a single tensile CESL across both nFETs and pFETs—minimizes “stress mismatch” by removing “the lateral interface” existing between tensile and compressive CESLs. Alvarez, Ex.1006, ¶¶[0033], [0074]. Alvarez teaches that it is less “costly and time-consuming.” Alvarez, Ex.1006, ¶[0033].

172. As detailed above, a POSITA would have recognized a combination like the one shown in Figure A as beneficial. It offers a cost-effective method to meet diverse performance requirements across various circuit regions, such as tuning stress to improve both nFET and pFET mobility and selectively blocking silicide in specific areas. Alvarez, Ex.1006, ¶¶[0027], [0032]-[0033], [0037], [0053]-[0055], [0074]; *See also* Morin-2007, Ex.1528, 355-56 (explaining that it “is important to work to improve the nMOS transistors since other solutions . . . can enhance the pMOS performances”); Hsu823, Ex.1506, ¶[0039] (“[T]he performance of PMOS devices can be easily improved with SiGe stressors, while the performance of NMOS devices is relatively difficult to improve”); Bohr, Ex.1527, ¶¶[0038]-[0039], FIG. 6.

b. A POSITA would have reasonably expected to succeed in combining Wu922 and Alvarez

173. As discussed earlier in Section X.A.1.a(1), a POSITA would have been motivated to (1) incorporate a stress-controlling layer, such as Alvarez’s layer 226/326/426 and/or 350/450, into Wu922’s FETs and (2) modify Wu922’s CESL 66 to be tensile stress inducing (like Alvarez’s layer 216/316/416). It is my opinion that a POSITA would have reasonably expected to succeed in combining Wu922 and Alvarez.

174. The embodiments of the Wu922-Alvarez combination illustrated in Figures A and B above would have required only standard, conventional procedures of (1) forming a layer (like Alvarez's layer 226/326/426 and/or 350/450) in the desired circuit regions (*see* Alvarez, Ex.1006, ¶¶[0027], [0032], [0035], [0045], [0063]-[0068], [0074], [0078], FIGS. 7-11); and (2) depositing Wu922's silicon nitride CESL 66 under conditions that would make it tensile (like Alvarez's layer 216/316/416) (*see* Jung, Ex.1529, ¶[0090], ¶¶[0099]-[0100], Tbl. V). Both of these steps were standard and widely recognized and are conventional and well known in the art. *See* Sections V.F and V.G above.

175. A POSITA also would have understood how to mask certain circuit regions (like Alvarez's silicide region 230) to selectively deposit the stress-controlling film (like Alvarez's non-silicide region 232 and stress-control region 242). *See* Alvarez, Ex.1006, ¶¶[0044], [0052]-[0053], [0063]-[0068]. Other references, like Alvarez, Murthy556, and Miyashita, for example, support that the stress-controlling layer would form in the space between the facets of Wu922's raised SiGe source/drain regions 58 and gate sidewalls 501A/512A. *See* Section X.A.1.a.(3) above; Wu922, Ex.1005, ¶[0042], FIGS. 7, 14; Alvarez, Ex.1006, ¶¶[0043]-[0049], [0052], [0063]-[0068], [0070]- [0071], [0073]-[0075], [0078], FIGS. 6-11; Murthy556, Ex.1430, 9:10-29, FIG. 8; Miyashita, Ex.1435, ¶¶[0052]-[0053], FIGS. 1U-1W.

176. A POSITA would have recognized the process of forming the stress-controlling layer (like Alvarez's layer 226/326/426 and/or 350/450) before forming the tensile CESL 66 (like Alvarez's layer 216/316/416) would have required nothing beyond a standard deposition process (e.g., SiO₂ deposition). *See* Alvarez, Ex.1006, ¶¶[0026], [0033], [0037], [0043]-[0049], [0053]-[0055], [0063]-[0068], [0070]-[0071], [0073]-[0075], [0078], FIGS. 6-11 (depositing oxide stress-controlling layer 226/326/426 and/or 350/450 just before depositing a tensile silicon nitride layer 216/316/416); Murthy556, Ex.1430, 9:10-29, FIG. 8 (same).

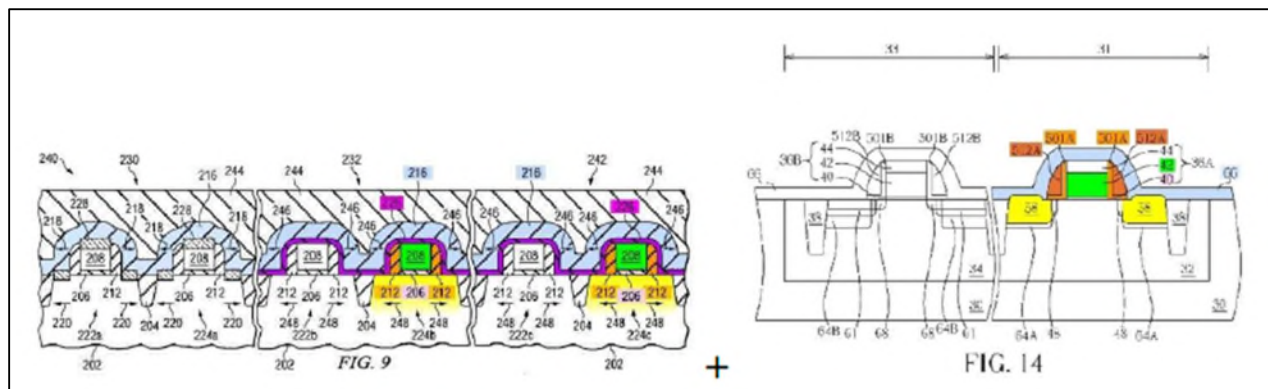
177. Wu922's CESL 66 is made of a "strained silicon material, i.e. silicon nitride." Wu922, Ex.1005, ¶[0025]. Like detailed above, forming a tensile silicon nitride CESL also would have required nothing beyond a standard and well-known deposition process. *See* Section V.F above; Jung, Ex.1529, ¶[0090], ¶¶[0099]-[0100], Tbl. V; Alvarez, Ex.1006, ¶[0047]; Wu922, Ex.1005, ¶[0005]; Doris, Ex.1429, ¶¶[0016]-[0017], ¶¶[0029]-[0030], ¶[0038], ¶[0042], ¶[0051], Figs. 1, 2, 14, 15; James, Ex.1012, 2, 5, Fig. 6; Morin-2007, Ex.1528, 355-56; Hsu823, Ex.1506, ¶[0003]; Ke, Ex.1531, ¶[0003] (explaining that "applying stress to the channel region [by] forming a stressed contact etch stop layer (CESL) on a MOS device" was "commonly used" to "introduce stress into the channel region" and improve carrier mobility). A POSITA would have been knowledgeable about these processes and thus reasonably anticipated success in making Wu922's CESL 66 cause a tensile

stress. This method was already recognized and extensively implemented in commercial devices to achieve similar advantages discussed herein. *See* Section V.F above; James, Ex.1012, 2, 5, Fig. 6.

178. A POSITA also would have known how to use a stress buffer layer to mitigate the effects of a tensile CESL on pFETs. For example, Alvarez teaches that stress-controlling layer 226 “controls, screens, or limits the effect of the stress of the second material 216 on the channel regions of the transistors 222b, 224b, 222c, and 224c.” Alvarez, Ex.1006, ¶[0050]; *See also* Alvarez, Ex.1006,, FIGS. 9-11. Moreover, “[t]he stress-controlling material 226 reduces the amount that the stress-increasing material 216 increases the first amount of stress by about the second amount of stress 218 less the third amount of stress 246, for example.” Alvarez, Ex.1006, ¶[0049]; *See also* Murthy556, Ex.1430, 9:10-29 (“Oxide layer 322 buffers the large stress inherent silicon nitride layer 324 and provides an etch step for silicon nitride layer 324 during a subsequent spacer etch.”), FIG. 8; Doris, Ex.1429, ¶[0042] (“The stress level along with the thickness of the film also defines a neutral buffer layer between the compressive spacer and the tensile etch stop layer.”), Figs. 14, 15; Lee870, Ex.1431, ¶[0029], ¶¶[0046]-[0067], ¶[0049] (explaining that an intermediate stress relief layer “with neutral stress or opposite stress relative to the [CESL]” reduces or eliminates any pFET performance degradation because it “reduces the tensile stress in the channel region”), FIGS. 2-5; Cheng810, Ex.1432,

¶¶[0022]-[0031], Figs. 1B-1F (describing similar). A POSITA would have reasonably anticipated achieving similar effects by placing a stress-controlling layer, such as Alvarez's layer 226/326/426 and/or 350/450, beneath Wu922's CESL 66.

179. In Section X.A.1.a.(4), as discussed earlier, I conclude that a POSITA would have considered it obvious to first deposit a stress-controlling layer, similar to Alvarez's layer 226/326/426 and/or 350/450, and then deposit Wu922's CESL 66 as a tensile film akin to Alvarez's layer 216/316/416. This concept is illustrated below in Figure A.



Alvarez, Ex.1006, FIG. 9 (annotated)

Wu922, Ex.1005 FIG. 14
(annotated)

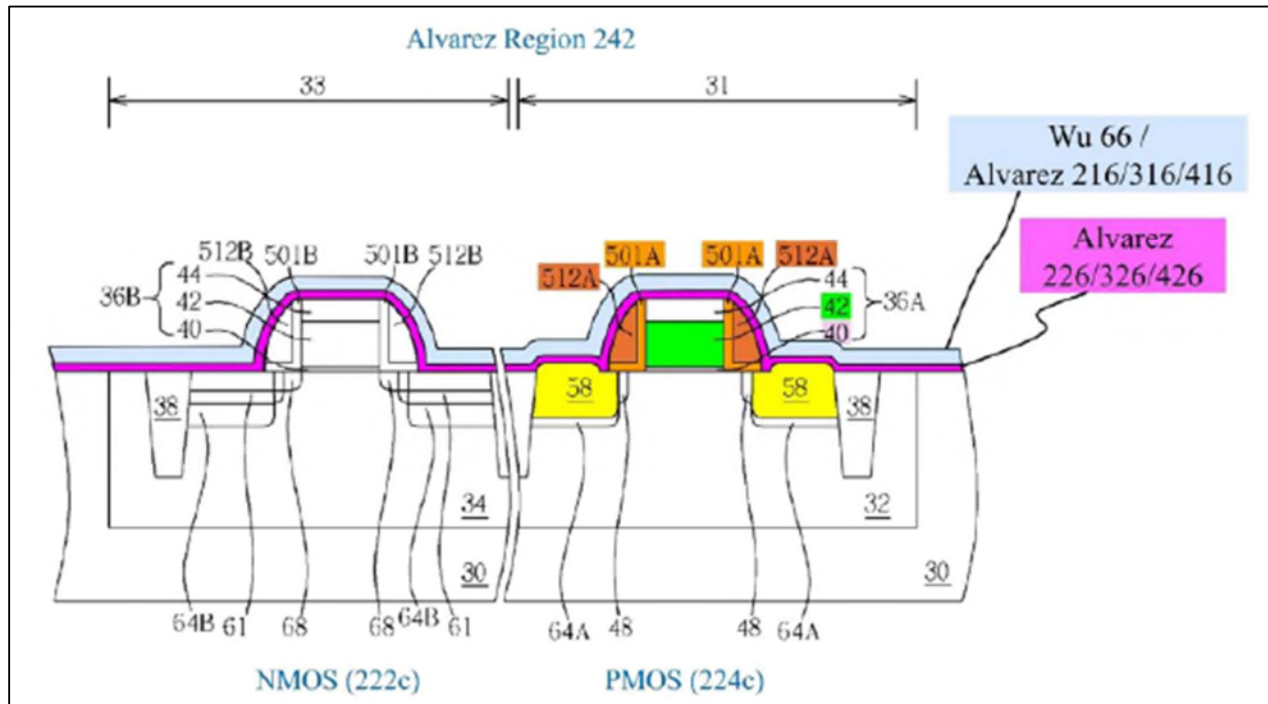


Figure A

180. A POSITA would have reasonably expected to succeed in forming a stress-buffering film, such as silicon oxide, in a space between the facets of Wu922's epitaxial SiGe layer 58 and gate sidewalls 501A/512A and then forming a tensile stress inducing CESL 66, because this approach was expected to deliver the usual and anticipated benefits outlined in I explain in Sections V.F, V.G, and X.A.1.a. above, including (i) mitigating the negative side effects from a tensile CESL 66 on pFETs by controlling the stress; (ii) selectively forming silicide in certain circuit regions (regions like Alvarez's non-silicide region 232/332 and stress-control region 242/342); and (iii) streamline the manufacturing steps and therefore reducing

manufacturing costs. *See* Alvarez, Ex.1006, ¶¶[0037], [0043], [0049], [0061], [0063]-[0064], [0069]-[0075], [0078], [0081], FIGS. 9-13.

c. Summary of the Wu922-Alvarez combination

181. In summary, it is my opinion that a POSITA would have found the Wu922-Alvarez combination obvious for at least the reasons below:

- It combines known prior art elements (e.g., Wu922's MOSFET structures with Alvarez's teachings to use a tensile CESL and intermediate stress-controlling layer) according to known methods (silicon oxide deposition followed by tensile silicon nitride deposition) to yield predictable results (a tensile CESL over both nFETs and pFETs with a buffer oxide to tune the stress and selectively form silicide in certain circuit regions).
- It uses known techniques (e.g., forming a stress-controlling layer like Alvarez's layer 226/326/426 and/or 350/450 and then forming a tensile CESL like Alvarez's layer 216/316/416) to improve similar devices (Wu922's FETs) in the same way as known in the prior art (e.g., by selectively forming silicide in certain circuit regions, improving nFET and pFET carrier mobility through stress tuning, and reducing manufacturing steps and costs).

- It applies known techniques (e.g., forming stress-controlling layer like Alvarez's layer 226/326/426 and/or 350/450 and then forming a tensile CESL like Alvarez's layer 216/316/416) to a known device that is ready for improvement (Wu922's FETs) to yield predictable results (matching different performance requirements in different circuit regions by adjusting nFET and pFET carrier mobility via stress tuning and selective silicide formation).
- It applies a known teaching, motivation, or suggestion in the prior art (e.g., Alvarez's teaching, motivation, and suggestion to use a tensile CESL (like layer 216/316/416) and a stress-controlling layer (like layer 226/326/426 and/or 350/450) to tune nFET and pFET stresses and selectively form silicide in a cost-effective manner) that would have led a POSITA to modify Wu922 according to, or to combine Wu922 with, the teachings of Alvarez to arrive at the claimed invention. *See* Sections V.F, V.G, and X.A.1.a. above; Alvarez, Ex.1006, ¶¶[0047], [0053]-[0055], [0065], Tbl. 1, FIG. 9; Murthy556, Ex.1430, 5:55-57; Doris, Ex.1429, ¶[0005], ¶[0008], ¶[0042]; Lee870, Ex.1431, ¶[0029], ¶¶[0046]-[0067], FIGS. 2-5; Cheng810, Ex.1432, ¶¶[0022]-[0031], Figs. 1B-1F.

2. Independent Claim 1

a. Preamble: “A semiconductor device comprising:”

182. Both Wu922 and Alvarez are directed to a semiconductor device and accordingly so is the Wu922-Alvarez combination. Specifically, Alvarez discloses “[t]he present invention relates generally to the fabrication of semiconductor devices and more particularly to introducing stress to material layers of semiconductor devices.” Alvarez, Ex.1006, ¶[0001], ¶[0019]. Wu922 is also directed toward a semiconductor device. Wu922 discloses “a strained CMOS transistor.” Wu922, Ex.1005, ¶[0009], FIGS. 1-7, 9-14. The semiconductor device taught has a first active region, the “PMOS transistor region 31,” and a second active region 33, the “NMOS transistor region 33.” Wu922, Ex.1005, ¶¶[0017], [0023]-[0024], [0038], [0042]–[0043], FIGS. 1-7, 9-14. The Wu922-Alvarez combination shown in Figure A below, primarily based on Wu922’s FIG. 14, shows an embodiment where Wu922 is modified in view of Alvarez to include a tensile CESL (highlighted light blue) and stress-controlling layer (highlighted magenta).

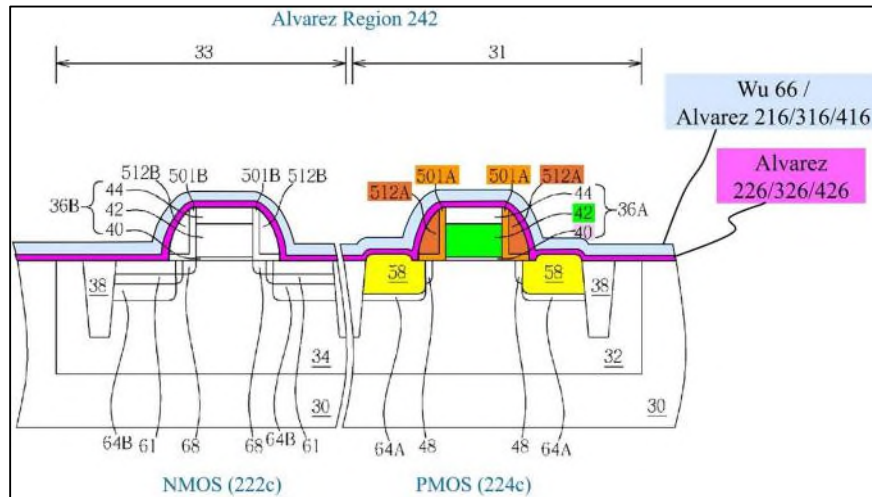


Figure A

183. Composite Figure A' is an alternative embodiment of the Wu922-Alvarez combination, which is discussed in the context of claim 3. *See* Section X.A.3 below. The alternative embodiment depicted in Figure A' closely mirrors Figure A above, with the addition of Wu922's optional silicide layer (highlighted in burgundy) formed on the source/drain and gate electrode. *See* Wu922, Ex.1005, ¶¶[0024], [0036], [0043], [0055], FIGS. 7, 14; Alvarez, Ex.1006, ¶¶[0063]-[0064], FIG. 10.

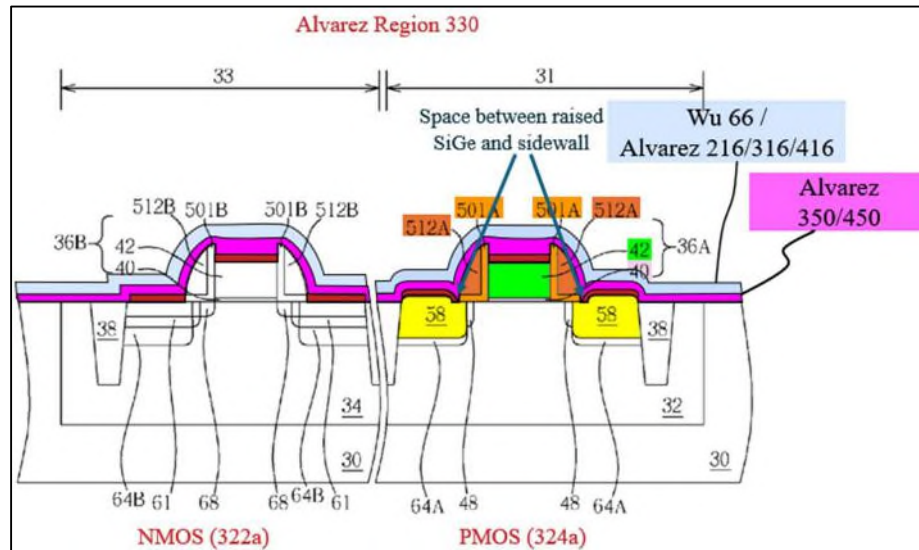


Figure A'

b. Element 1[a]: “a first MIS transistor wherein:”

184. As can be seen below in Figure A, the Wu922-Alvarez combination discloses a first MIS transistor, including claim elements [1B]-[1J] discussed below.

185. For example, Wu922 discloses a first MIS transistor, such as the pEFT in “PMOS transistor region 31.” Wu922, Ex.1005, Abstract, ¶[0002], ¶[0005], ¶[0017], ¶[0023], ¶¶[0027]-[0036], ¶[0038], ¶¶[0042]-[0043], ¶¶[0046]-[0055], FIGS. 1-7, 9-14. Further, Alvarez discloses a first transistor. *See e.g.*, Alvarez, Ex.1006, ¶[0042], FIG. 9. Figure A below shows an exemplary first MIS transistor in PMOS region 31.

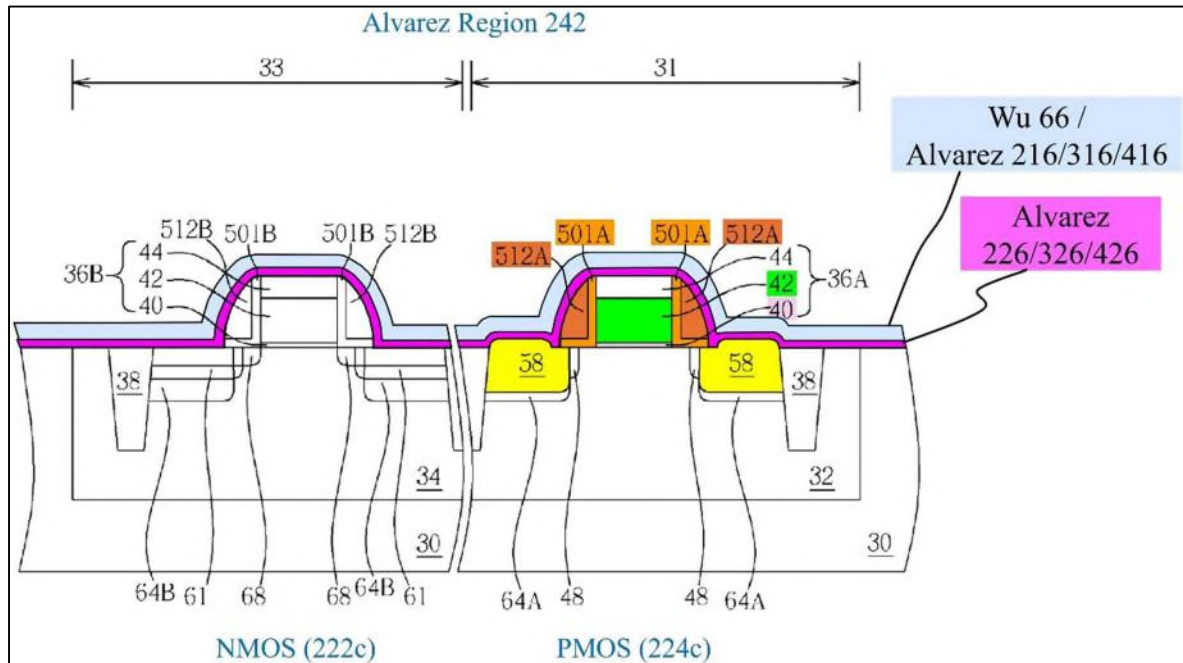


Figure A

- c. **Element 1[b]: “the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate,”**

186. As can be seen below in Figure A, the Wu922-Alvarez combination discloses the first MIS transistor including a first insulating film formed on the first active region in a semiconductor substrate. Wu922 discloses a “gate dielectric layer 40” formed on the “first active area,” e.g., “PMOS transistor region 31,” of “semiconductor substrate 30.” Wu922, Ex.1005, ¶[0017] (“the first active area is a PMOS transistor region 31”), (“Each of the gate structure 36A, 36B includes a gate dielectric layer 40 The gate dielectric layer 40 may comprise dielectric materials”), ¶¶[0038]-[0039] (describing “gate structures 36A, 36B”). Wu922's gate dielectric layer 40 serves as the gate insulating film disclosed in the '425 patent

because it is composed of dielectric materials like silicon oxide, which possess insulating properties. Wu922, Ex.1005, ¶[0017]. Wu922 discloses “silicon oxide” as one of the materials, which is also used for the “gate insulating film” in the ’425 patent. The ’425 patent, Ex.1001, 9:15-19.

187. Alvarez also discloses a “gate dielectric” layer. Alvarez, Ex.1006, ¶[0039]. Alvarez’s gate dielectric layer 206 serves as the gate insulating film disclosed in the ’425 patent because it is composed of dielectric materials like silicon dioxide or other materials, which possess insulating properties. *Id.* (“A gate dielectric materials 206 comprising an insulator such as silicon dioxide”).

188. Figure A below shows the gate dielectric layer 40 (highlighted light purple) on PMOS active region 31 of substrate 30, one embodiment of the Wu922-Alvarez combination. *See* Wu922, Ex.1005, ¶[0017], FIGS. 1-7, 9-14.

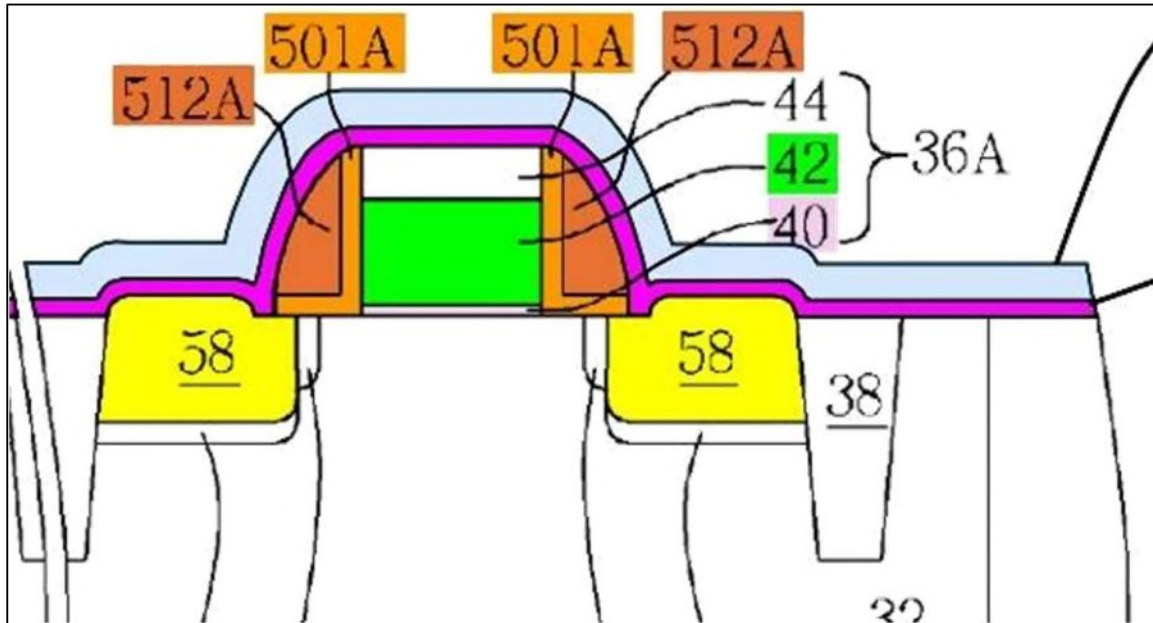


Figure A (excerpted)

d. Element 1[c]: “a first gate electrode formed on the first gate insulating film,”

189. As can be seen below in Figure A, the Wu922-Alvarez combination discloses a first gate electrode formed on the first gate insulating film. Wu922, Ex.1005, ¶[0017] (“The gate 42 may use polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof as material.”), FIGS. 7, 14.

190. Similarly, Alvarez discloses a first gate electrode. “The gate material 208 preferably comprises a semiconductor material such as silicon or polysilicon” Alvarez, Ex.1006, ¶[0039].

191. The Wu922-Alvarez combination, as illustrated in Figure A below shows the gate electrode 42 positioned on the first gate insulating film (gate dielectric film 40), similar to the depiction in Wu922's FIG. 14.

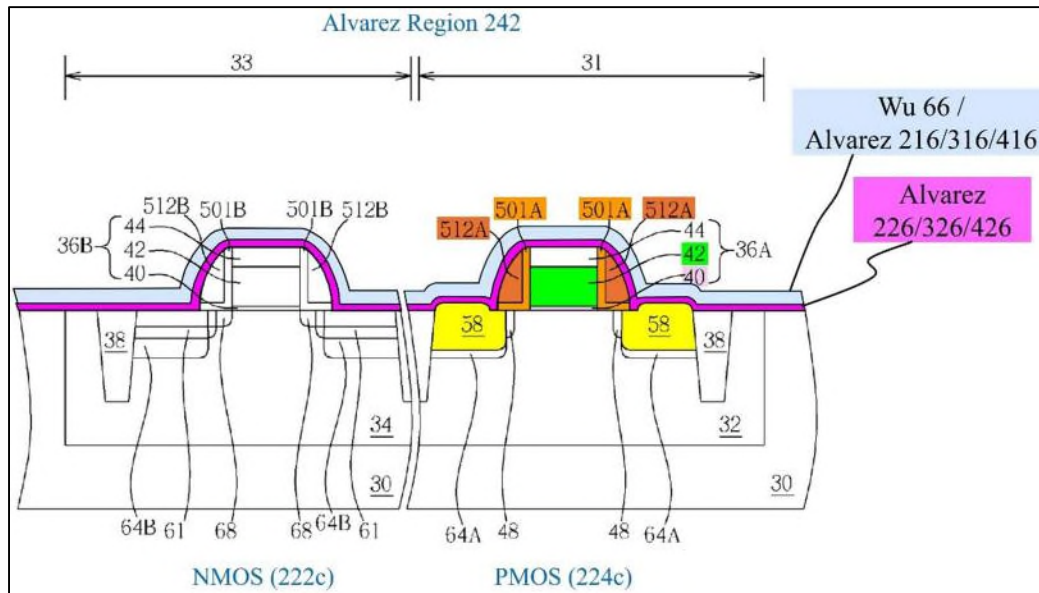


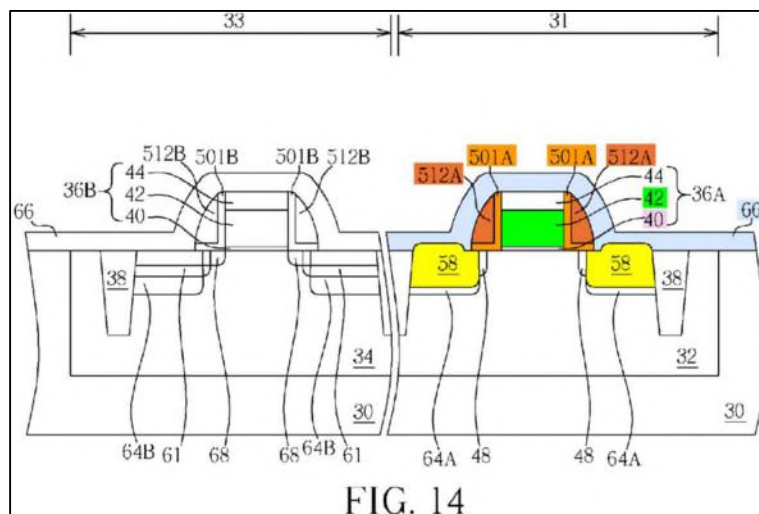
Figure A

- e. **Element 1[d]: “a first sidewall spacer formed on a side surface of the first gate electrode,”**

192. As can be seen below in Figure A, the Wu922-Alvarez combination discloses a first sidewall spacer formed on a side surface of the first gate electrode. Wu922 discloses a first sidewall spacer comprising “oxide layer 501A” and optionally “second [sidewall] spacer 512A . . . formed on the sidewalls of the gate structure[] 36A” of the pFET. Wu922, Ex.1005, ¶¶[0017], [0024], [0043], FIGS. 7, 14.

193. Similarly, Alvarez discloses a first sidewall spacer formed on a side surface of the first gate electrode. “Spacers 212 comprising an insulating material are formed on the sidewalls of the gate 208 and gate dielectric 206. The spacers 212 may comprise one or more layers of silicon oxide, silicon nitride, or SiON, as examples, although alternatively, other materials may also be used.” Alvarez, Ex.1006, ¶[0040].

194. Wu922’s FIGS. 7 and 14 show oxide layer 501A and sidewall spacer 512A, both of which sit on the sidewalls of pFET gate structure 36A. Wu922, Ex.1005, ¶¶[0017], [0024], FIGS. 7, 14. As Wu922’s FIG. 14 shows below, oxide layer 501A and optionally sidewall spacer 512A are formed on the side surfaces of gate electrode 42 in PMOS transistor region 31. The same configuration is present in the Wu922-Alvarez combination, as shown in Figure A below.



Wu922, Ex.1005 FIG. 14 (annotated)

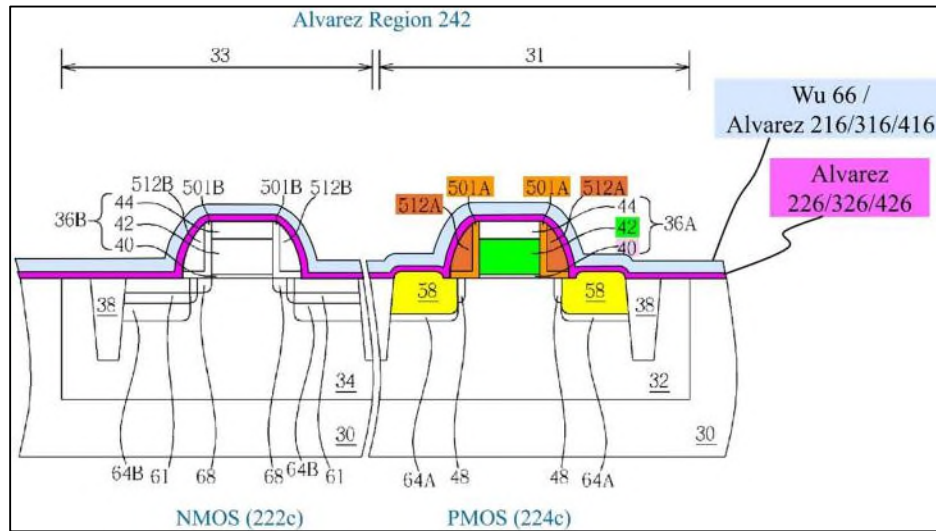


Figure A

- f. **Element 1[e]: “a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region, and”**

195. As can be seen below in Figure A, the Wu922-Alvarez combination discloses a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region. Specifically, Wu922 discloses a first source/drain region in the first active area, the “PMOS transistor region 31,” that includes “an epitaxial layer 58 of silicon germanium [SiGe]” and if of a first conductivity type, p-type. Wu922, Ex.1005, ¶¶[0019], [0021], [0041], FIGS. 7, 14.

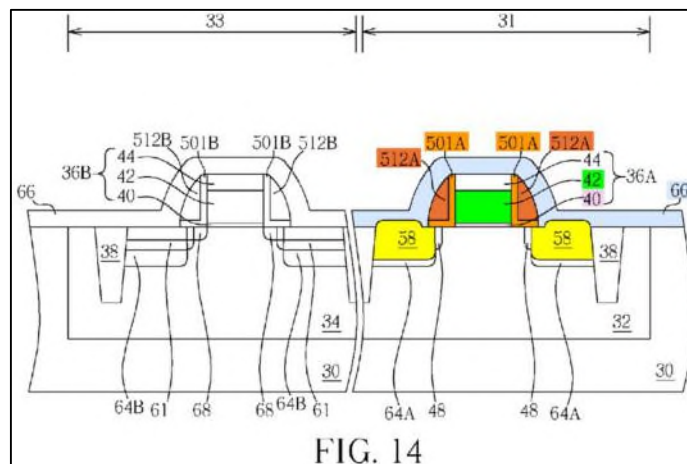
Wu922's epitaxial layer 58 is made of a silicon compound (silicon germanium [SiGe]) and which causes a first, compressive stress in the gate length direction of the pFET channel region in PMOS transistor region 31.

196. Wu922 also discloses that the epitaxial SiGe layer 58 (the silicon compound layer) is formed in a trench also known as “a recess 56 . . . formed on the surface of the N well 32 beside the gate structure 36A.” Wu922, Ex.1005, ¶¶[0020], [0031], [0040], [0050], FIGS. 3, 11. As Wu922's FIGS. 11-14 demonstrate, for instance, recess 56 is located “beside the gate structure 36A” in the “first active area” of “PMOS transistor region 31” on a lateral side of the first sidewall spacer comprising oxide layer 501A and optionally sidewall spacer 512A.⁴ Wu922, Ex.1005, ¶¶[0017], [0020], [0031], [0040], [0050], FIGS. 3-7, 11-14. As Wu922 further explains, the “preferred epitaxial [SiGe] layer 58 has a lattice constant greater than that of the semiconductor substrate 30,” and the SiGe “compress[es] the channel” (causes compressive stress (first stress) in the channel direction of the channel region) of the

⁴ Wu922's epitaxial SiGe layer 58 is formed before the sidewall spacer 512A is formed. To the extent it may be determined that the “first sidewall spacer” does not need to exist when the first source/drain region is actually formed, then the claimed “first sidewall spacer” may include Wu922's spacer 512A. *See* Wu922, Ex.1005 ¶¶[0024]-[0025], ¶¶[0043]-[0044].

pFET as a result. Wu922, Ex.1005, ¶¶[0021], [0041] (“The preferred epitaxial layer 58 has a lattice constant greater than that of the semiconductor substrate 30, and is extended approaching to the channel. In order to compress the channel and to keep the silicon layer formed in the following steps from the interface between the source/drain in a distance, the preferred epitaxial layer 58 is slightly projected from the top surface of the semiconductor substrate 30.”), FIGS. 7, 14. As explained in Section V.F , the purpose of SiGe in the source/drain regions is to cause this compressive stress in the channel region.

197. Highlighted in yellow in Wu922’s FIG. 14, below, are the SiGe layers. The embodiment of the Wu922-Alvarez combination below also shows the SiGe layers highlighted yellow.



Wu922, Ex.1005 FIG. 14 (annotated)

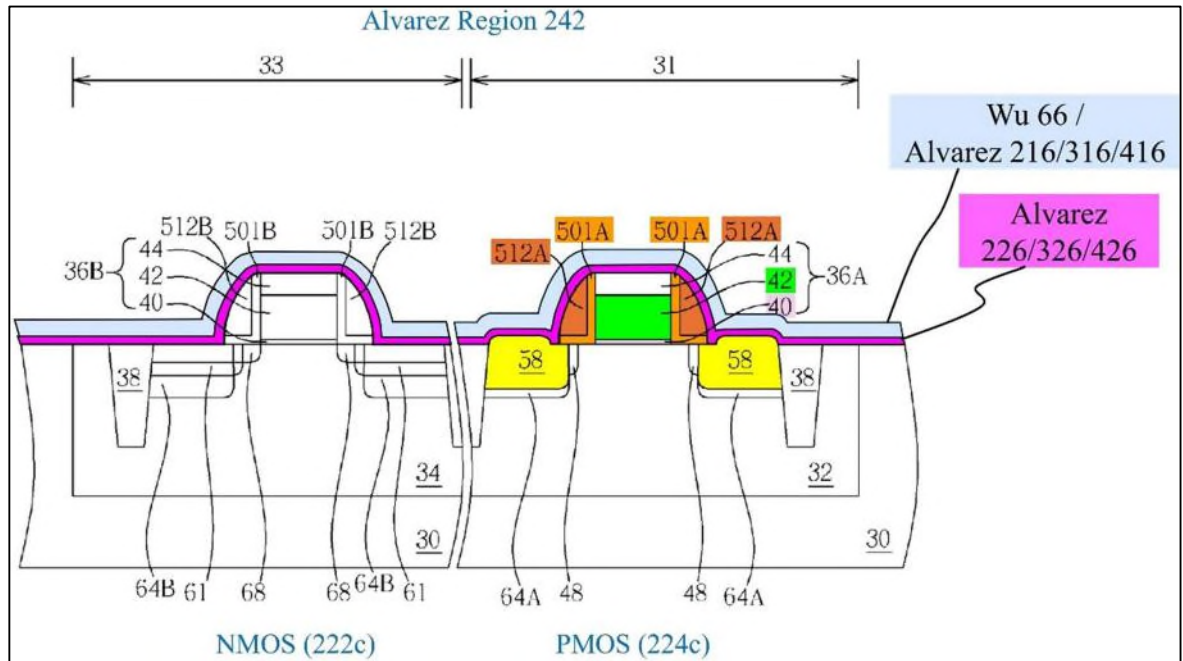


Figure A

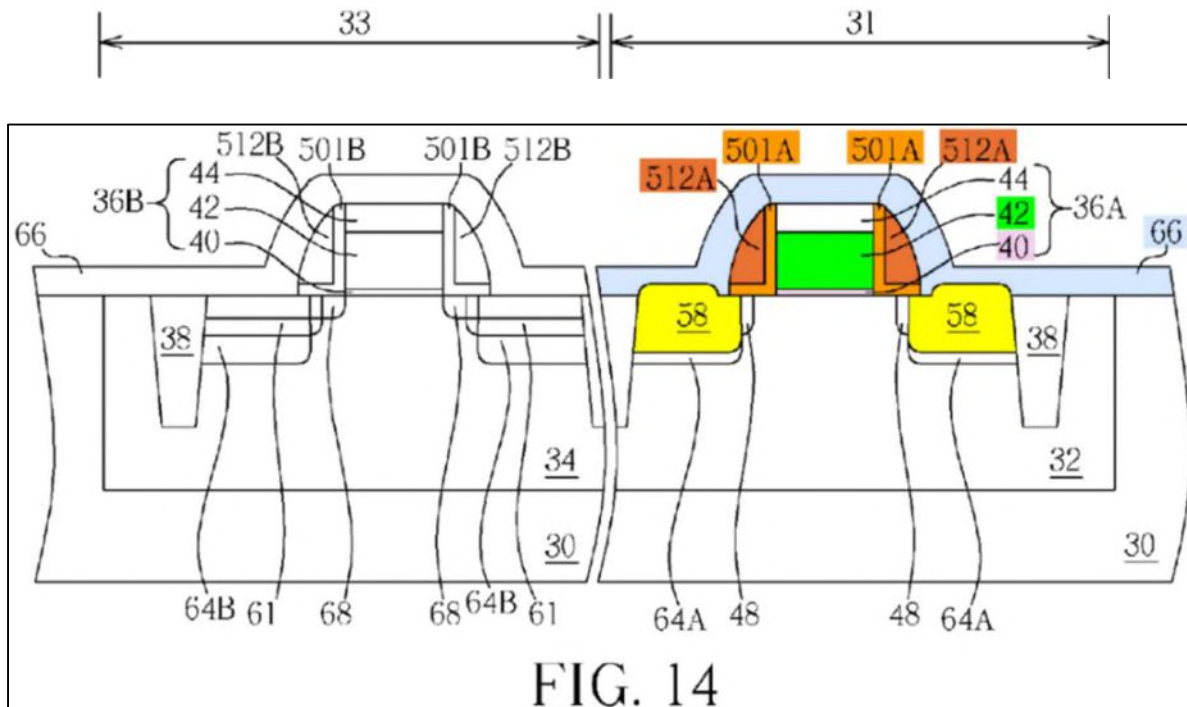
- g. **Element 1[f]: “a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress,”**

198. As can be seen below in Figure A, the Wu922-Alvarez combination discloses a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress. Wu922 discloses a stress insulating film, “a CESL 66 [formed] on the surface of the gate structures 36A, 36B, the second spacers 512A, 512B, and the sources/drains 64A, 64B.” Wu922, Ex.1005, ¶¶[0025], [0044], FIGS. 7, 14. Wu922 discloses “deposit[ing] . . . a contact etch stop layer (CESL) 66 on the surface of the gate structures 36A, 36B, the second spacers

512A, 512B, and the sources/drains 64A, 64B.” Wu922, Ex.1005, ¶¶[0025], [0044].

Wu922 explains that “CESL 66 may include . . . a strained silicon material, i.e. silicon nitride.” Wu922, Ex.1005, ¶[0025]. Because Wu922 discloses depositing CESL 66 (highlighted below in blue) over “gate structures 36A, 36B” and “[sidewall] spacers 512A, 512B,” it necessarily discloses depositing CESL 66 over oxide sidewalls 501A and 501B located between gate structures 36A and 36B, as well as sidewall spacers 512A and 512B. This structure is exemplified below in FIG.

14. See Wu922, ¶[0025], ¶[0044], FIGS. 7, 14 (annotated below).



Wu922, Ex.1005 FIG. 14 (annotated)

199. Although Wu922 describes CESL 66 as “strained,” it does not clarify whether the strain is tensile or compressive. As I explain above, a POSITA would have found it obvious to make Wu922’s CESL 66 tensile stress inducing, as disclosed in Alvarez. *See* Sections V.F and X.A.1 above; Alvarez, Ex.1006, ¶[0065] (“Stress-increasing material 416 comprises tensile stress”), Tbl. 1.

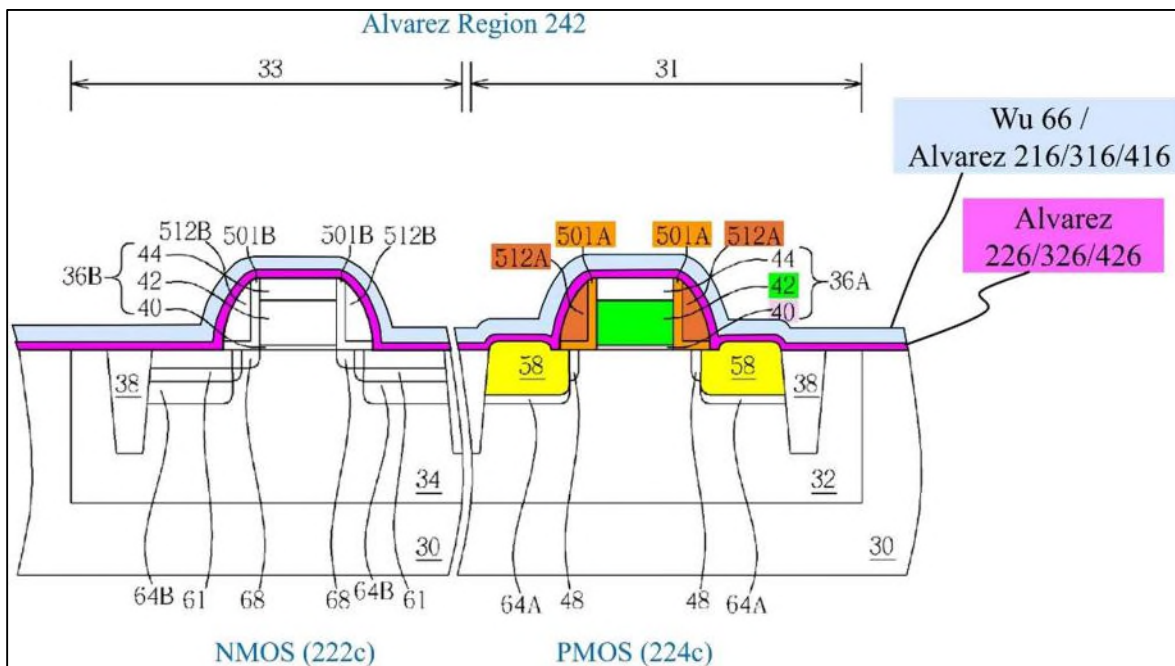


Figure A

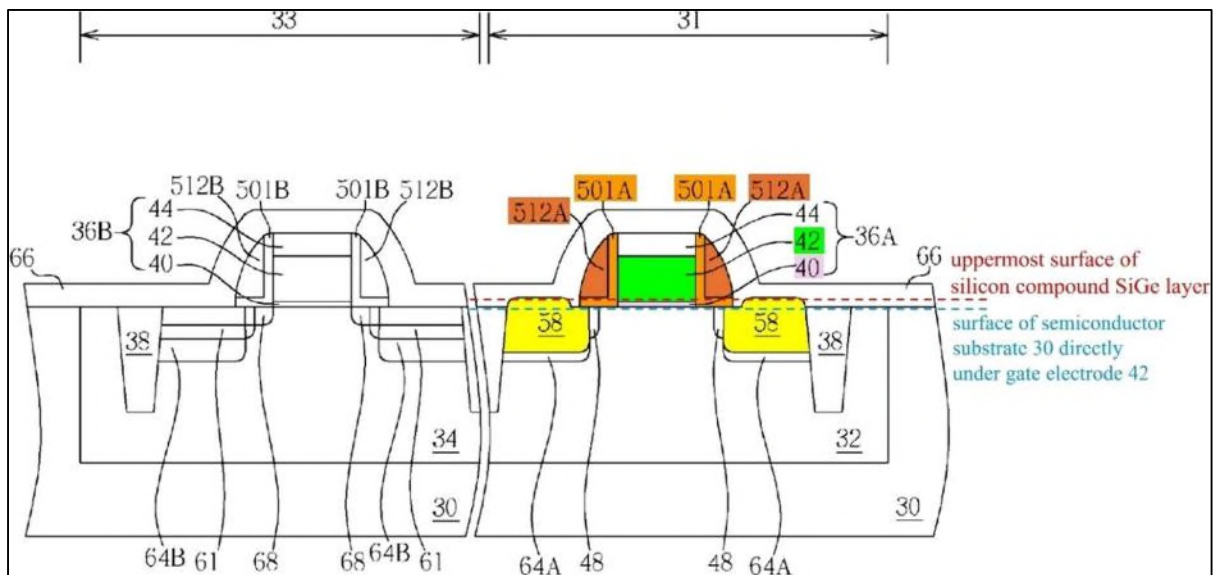
200. For the reasons I discuss in Section X.A.1 above, a POSITA would have found it obvious to make Wu922’s CESL 66 a tensile stress inducing film. In Wu922’s FIG. 14 and the embodiment of the Wu922-Alvarez combination shown in Figure A, the tensile CESL 66 in the Wu922-Alvarez combination is formed over the first gate electrode (gate 42), the first sidewall spacer (oxide layer 501A and optionally sidewall spacer 512A), and the first source/drain region (epitaxial SiGe layer 58). Due to its

tensile nature the CESL 66 in the Wu922-Alvarez combination would exert a second stress (tensile) that contrasts with the first stress (compressive), which is induced by the SiGe layer in the source/drain regions.

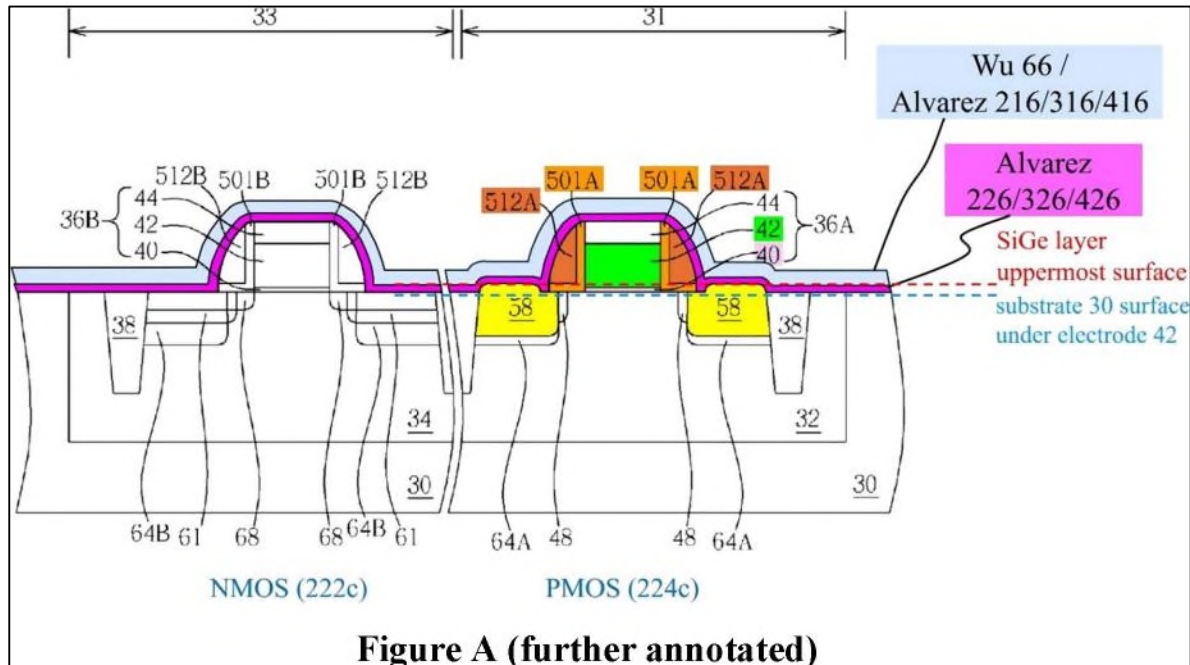
h. Element 1[g]: “an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode,”

201. As can be seen below in Figure A, the Wu922-Alvarez combination discloses an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode. Wu922 discloses “the preferred epitaxial layer 58 is slightly projected from the top surface of the semiconductor substrate 30. *See* Wu922 ¶[0041]. Wu922 further explains that this is to “to compress the channel and to keep silicon layers formed in the following steps from the interface between the source/drain in a distance.” Wu922, Ex.1005, ¶¶[0021], [0041] (“In order to compress the channel and to keep the silicon layer formed in the following steps from the interface between the source/drain in a distance, the preferred epitaxial layer 58 is slightly projected from the top surface of the semiconductor substrate 30.”), FIGS. 7, 14. A POSITA would easily recognize that Wu922's descriptions pertain to the same type of raised epitaxial SiGe layers that are well-established in the prior art. *See* Section X.A.1 above.

202. As Wu922's FIGS. 4-7 and 12-14 show, the top surface of epitaxial SiGe layer 58 (red dashed line) is higher than the top surface of substrate 30 under the gate electrode 42 (blue dashed line). See Wu922, Ex.1005, ¶¶[0021], [0041], FIGS. 4-7, 12-14. The feature is also shown in the Wu922-Alvarez combination as depicted in Figure A below.



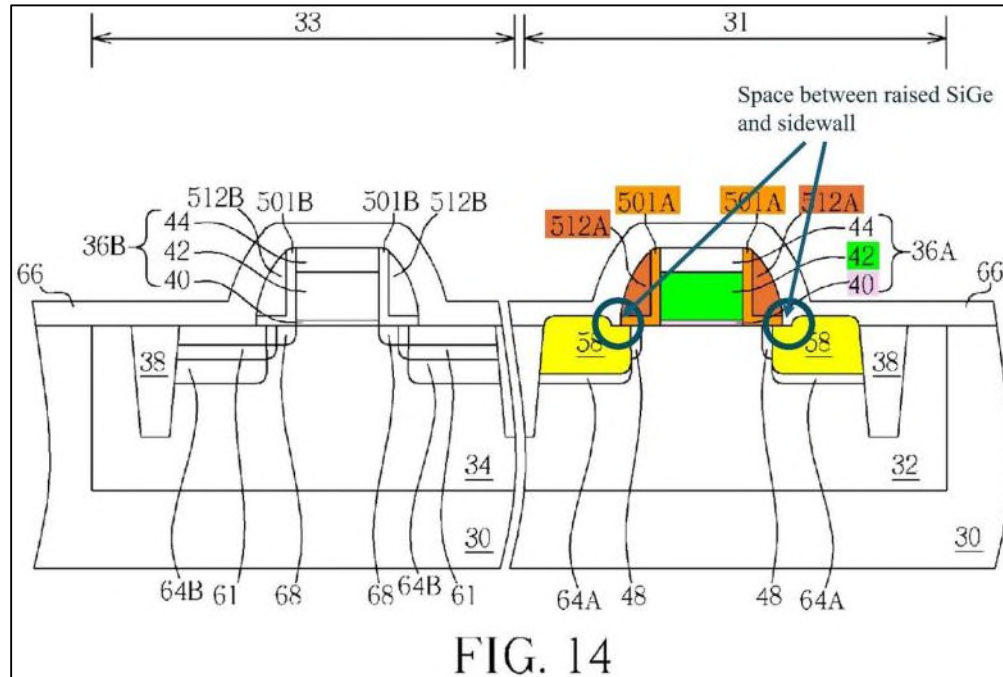
Wu922, Ex.1005 FIG. 14 (annotated)



- i. **Element 1[h]: “a first stress-relief is formed in a space between the silicon compound layer and the first sidewall spacer,”**

203. As can be seen below in Figure A, the Wu922-Alvarez combination discloses a first stress-relief is formed in a space between the silicon compound layer and the first sidewall spacer. As I explain in Section X.A.1 above, the Wu922-Alvarez combination includes a first stress-relief film formed in a space between epitaxial SiGe layer 58 and the first sidewall spacer (spacer 501A and optionally 512A). A POSITA would have recognized that, if a stress-controlling layer (highlighted magenta) like Alvarez’s layer 226/326/426 is formed over Wu922’s PMOS transistor region 31, it would have necessarily formed in the gap between raised SiGe layer 58 (highlighted yellow) and sidewall spacer layers 501A (highlighted light orange) and 512A (highlighted dark orange). See Wu922’s FIG.

14 and Figure A demonstrate this structure below. See Sections V.G and X.A.1 above; Wu922, FIGS. 7, 14.



Wu922, Ex.1005 FIG. 14 (annotated)

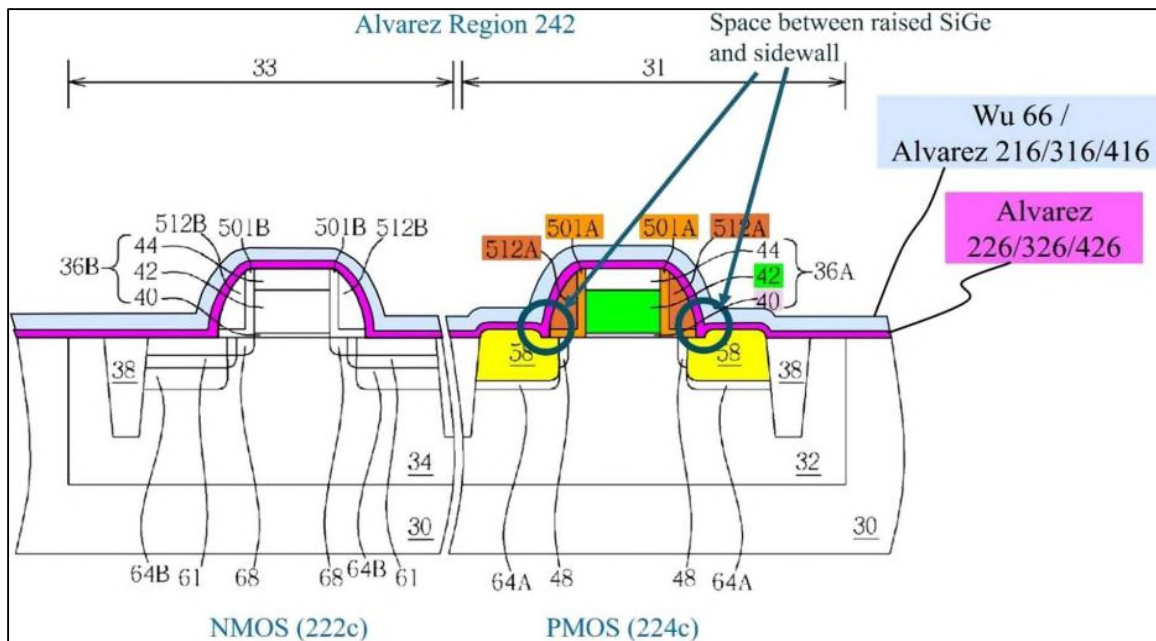


Figure A (further annotated)

j. Element 1[i]: “the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween, and”

204. As can be seen in Figure A above, the Wu922-Alvarez combination discloses the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween. As I explain above for the Wu922-Alvarez combination, the first stress-relief film (a stress-controlling film like Alvarez’s layer 226/326/426) is formed on the side surface of the first gate electrode (gate 42) of the pFET with the first sidewall spacer layer (spacer 501A and optionally 512A) interposed therebetween. *See* Section X.A.1 above. The embodiment of the Wu922-Alvarez combination shown in Figure A above demonstrates this.

205. Like stress-controlling film 226/326/426 in Alvarez’s FIG. 9, a POSITA would have understood that the stress-controlling film in the Wu922-Alvarez combination (magenta above) would blanket Wu922’s pFETs in circuit regions like Alvarez’s stress-control region 242. *See* Section X.A.1 above. A POSITA would understand that the stress-controlling layer (highlighted magenta) forms on the side surfaces of gate 42 (highlighted green), including within the gap between the first sidewall spacer layer (spacer 501A, light orange, and optionally 512A, highlighted dark orange) and the epitaxial SiGe layer 58 (highlighted yellow). *See* Sections V.G and X.A.1 above. The first sidewall spacer layer (highlighted orange) is interposed

between the stress-relief film (highlighted magenta) and the first gate electrode (highlighted green). Figure A; *See also* Sections V.G and X.A.1 above.

k. Element 1[j]: “the first stress-relief film is not in direct contact with the side surface of the first gate electrode.”

206. As can be seen in Figure A below, the Wu922-Alvarez combination discloses the first stress-relief film is not in direct contact with the side surface of the first gate electrode. As explained above for elements [1H] and [1I] and in Section X.A.1, the first stress-relief film of the Wu922-Alvarez combination (akin to Alvarez’s stress-controlling film 226/326/426 (highlighted magenta)) does not directly contact the side surface of the first gate electrode (gate 42 (highlighted green)) because the first sidewall spacer layer (oxide layer 501A (highlighted light orange) and optionally spacer 512A (highlighted dark orange)) (orange) divides the first stress-relief film from the first gate electrode. Figure A shows this below.

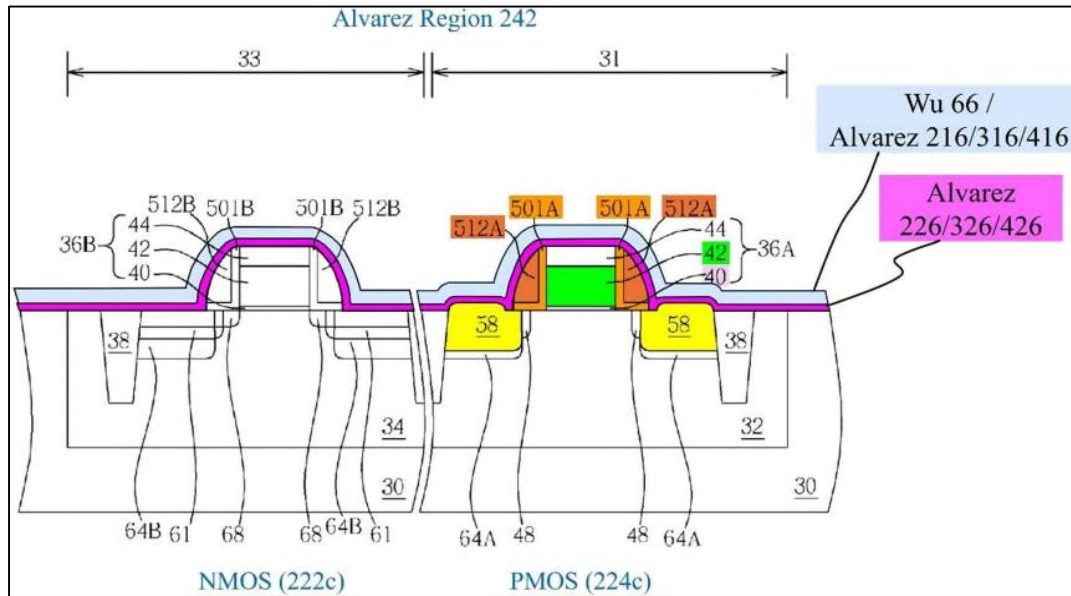
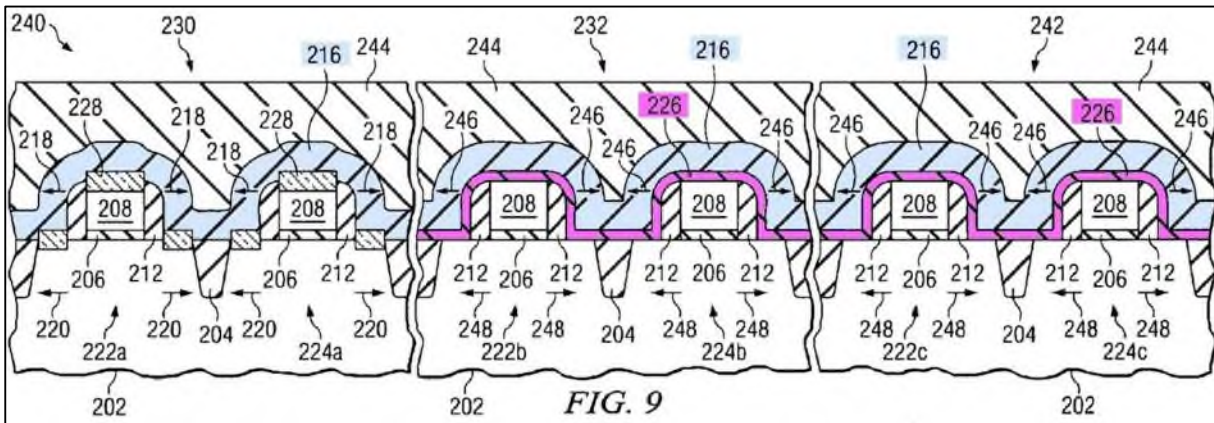


Figure A

207. Alvarez provides corroboration for this point. For instance, Alvarez's FIG. 9 shows that stress-controlling film 226 is formed over the gate electrode 208 and sidewalls 212 in stress-control region 242, such that stress-controlling film 226 is prevented from directly contacting the lateral surfaces of gate electrode 208 due to the presence of sidewall 212 positioned between them. The arrangement is maintained in the Wu922-Alvarez combination, as depicted in the embodiment shown in Figure A above. *See* Section X.A.1 above.



Alvarez, Ex.1006 FIG. 9 (annotated)

3. Dependent Claim 3

- a. **Claim 3: “the semiconductor device of claim 1, further comprising: a first silicide layer formed on the first gate electrode; and a second silicide layer formed on the first source/drain region which includes the silicon compound layer.”**

208. As can be seen in Figure A’ below and as explained further below, the Wu922-Alvarez combination discloses the semiconductor device of claim 1. This alternative embodiment shown in Figure A’ satisfies all the claim elements of claim 1.

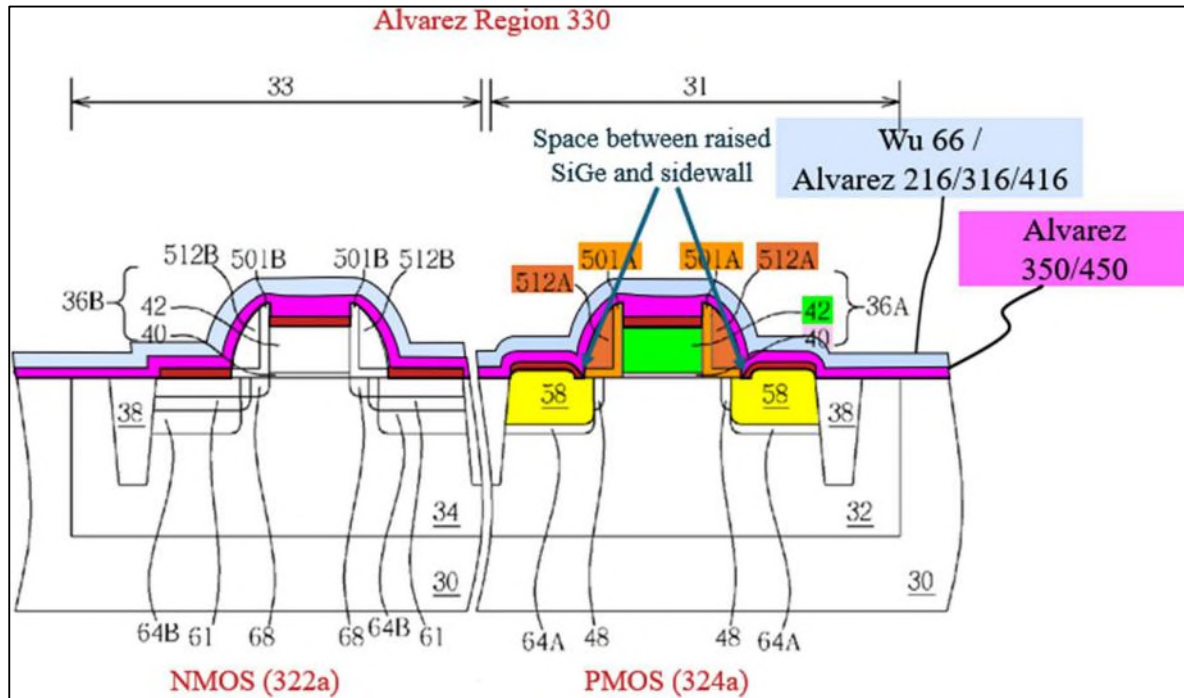
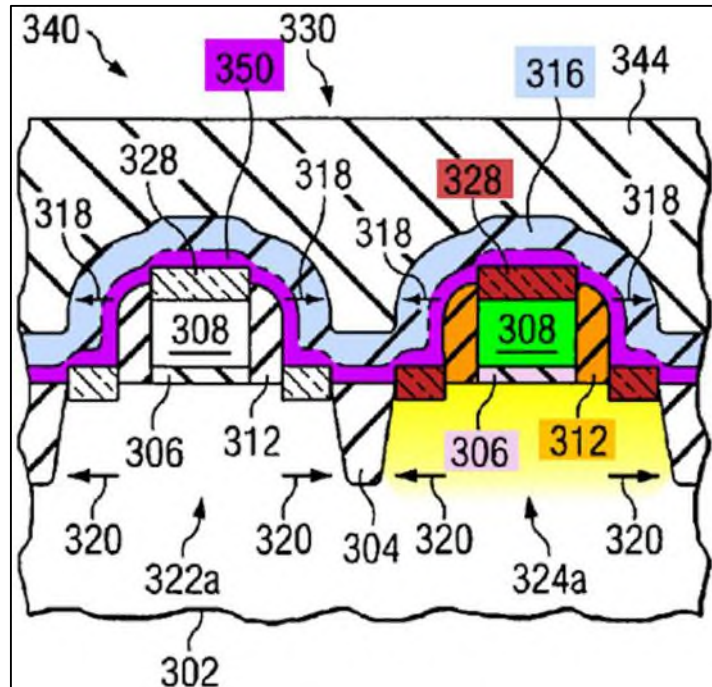


Figure A'

209. Wu922 discloses optionally forming silicide over the source/drain regions 64A and 64B and the gate electrode 42. *See* Wu922, Ex.1005, ¶[0024] (“[A] self-aligned silicide process (salicide process) is optionally performed.”); Wu922, Ex.1005, ¶[0043] (“[A] self-aligned silicide process is optionally performed to form a silicide layer (not shown) on the surfaces of the gate structures or the source/drain.”); Wu922, Ex.1005, ¶[0036] (“A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”), ¶[0055] (same). Figure A' above illustrates an embodiment of the Wu922-Alvarez combination using a silicide region like Alvarez in FIG. 10 (excerpted, annotated



210. The only material difference of the Wu922-Alvarez combination is that alternative embodiment, shown in Figure A', is that it has silicide layers (highlighted burgundy), and the Figure A embodiment does not. Given that this addition does not impact my evaluation of claim 1, I will not reiterate that analysis for Figure A. It suffices to note my analysis in Section X.A.2 applies to Figure A' with the following substitutions:

- Figure A' shows the Wu922-Alvarez combination in a region like Alvarez's silicide region 330, whereas Figure A shows the Wu922-Alvarez combination in a region like Alvarez's stress-controlling region 242.
- All references to FIG. 9 in my discussion of claim 1 in Section X.A.2 would refer to FIG. 10 instead.
- All references to Alvarez's stress controlling layer 226/326/426 in Section X.A.2 would refer to Alvarez's stress-controlling layer 350/450.⁵

See Section X.A.2 above; Wu922, Ex.1005, ¶¶[0024], [0036], [0043], [0055]; Alvarez, Ex.1006, ¶¶[0063]-[0064] ("The third material 350 preferably comprises similar materials, dimensions, and deposition methods and parameters as described for the first material 226 or stress-controlling material 226 shown in FIGS. 5 through 9, for example. . . . The third material 350 may also be formed over the first region 330 after the formation of the silicide 328, as shown in phantom."), FIGS. 9-10. Still, the Figure A' structure is fundamentally the same as the structure analyzed for claim

⁵ See Alvarez, Ex.1006, ¶[0064] ("The third material 350 preferably comprises similar materials, dimensions, and deposition methods and parameters as described for the first material 226 or stress-controlling material 226 shown in FIGS. 5 through 9, for example. . . . The third material 350 may also be formed over the first region 330 after the formation of the silicide 328, as shown in phantom.").

1 in Section X.A.2 above. The silicide layer does not materially affect my analysis, such that the PMOS structure in Figure A' also satisfies claim 1 for the same reasons.

211. The embodiment of the Wu922-Alvarez combination shown in Figure A' is the same structure as Figure A, but also includes “a first silicide layer formed on the first gate electrode; and a second silicide layer formed on the first source/drain region which includes the silicon compound layer” as claimed in Claim 3.

212. Although not illustrated in Wu922's FIG. 14, Wu922 teaches that “a self-aligned silicide process (salicide process) is optionally performed.” Wu922, Ex.1005, ¶[0024]; *See also* Wu922, Ex.1005, ¶[0043] (“[A] self-aligned silicide process is optionally performed to form a silicide layer (not shown) on the surfaces of the gate structures or the source/drain.”); Wu922, Ex.1005, ¶[0036] (“A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”), ¶[0055] (same). “A metal layer, including titanium (Ti), cobalt (Co), nickel (Ni), palladium (Pd), platinum (Pt) or the like, is deposited. And a rapid thermal process is performed to form a silicide layer (not shown) on the surfaces of the source/drain 64A, 64B.” Wu922, Ex.1005, ¶[0024].

213. Similarly, Alvarez also explains that the stress-controlling layer 350/450 may “be formed over the first region 330 *after* the formation of the silicide

328.” Alvarez, Ex.1006, ¶[0064] (emphasis added); *See also* Alvarez, Ex.1006, FIG. 10.

214. Combining Wu922 and Alvarez, a POSITA would have found the embodiment in Figure A' below obvious for the reasons explained in Section X.A.1 above.

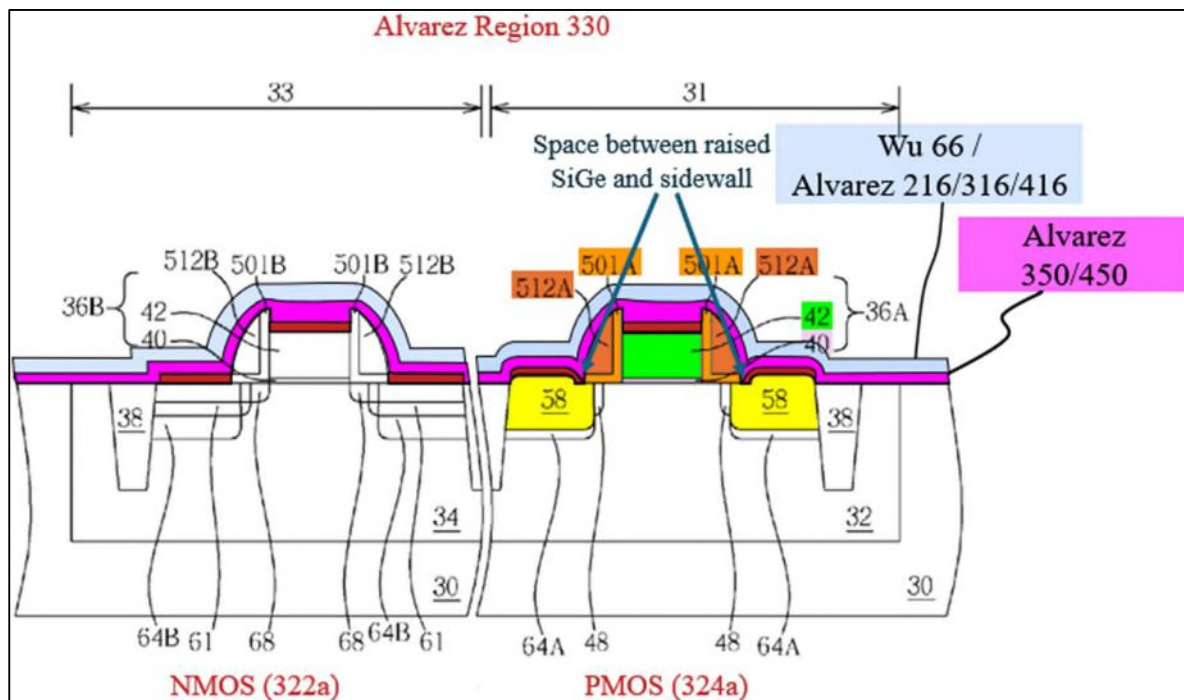


Figure A'

215. Again, this embodiment shown in Figure A' of the Wu922-Alvarez combination includes a first silicide layer (highlighted burgundy) formed on the first gate electrode (highlighted green) and a second silicide layer (also highlighted burgundy) formed on the first source/drain region (which contains the silicon compound layer (SiGe layers, highlighted yellow)). *See* Wu922, Ex.1005, ¶[0024],

[0036], [0043], [0055]; Alvarez, Ex.1006, ¶¶[0063]-[0064], FIG. 10. Therefore, it is my opinion that a POSITA would consider Claim 3 to be obvious based on the Wu922-Alvarez combination as illustrated in Figure A'.

4. Dependent Claim 4

a. Claim 4: “The semiconductor device of claim 1, wherein the first stress-relief film is formed on a side surface of the silicon compound layer”

216. As can be seen in Figure A below and as explained further below, the Wu922-Alvarez combination discloses the semiconductor device of claim 1 and where the first stress-relief film is formed on a side surface of the silicon compound layer. *See* Sections X.A.1 and X.A.2 above. As shown in the Wu922-Alvarez combination in Figure A, excerpted and further annotated below, the first stress-relief film (highlighted magenta) is formed on a side surface of epitaxial SiGe layer 58 (highlighted yellow). *See* Section X.A.1 above.

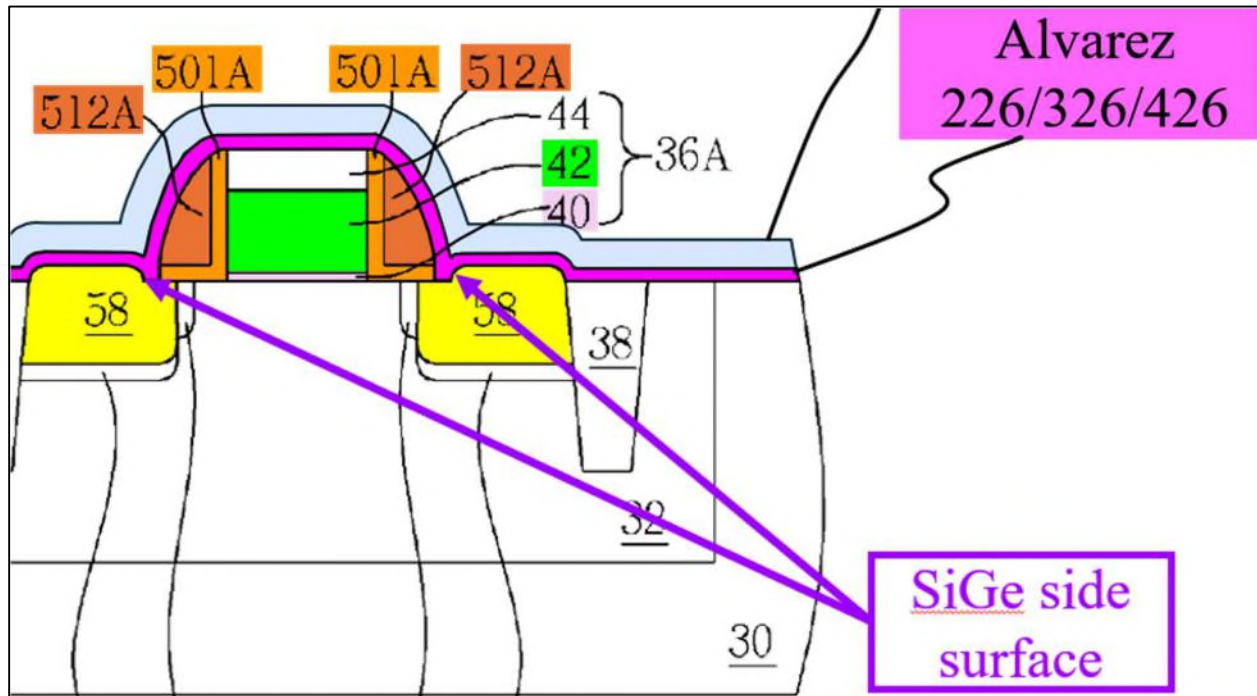


Figure A (excerpted and further annotated)

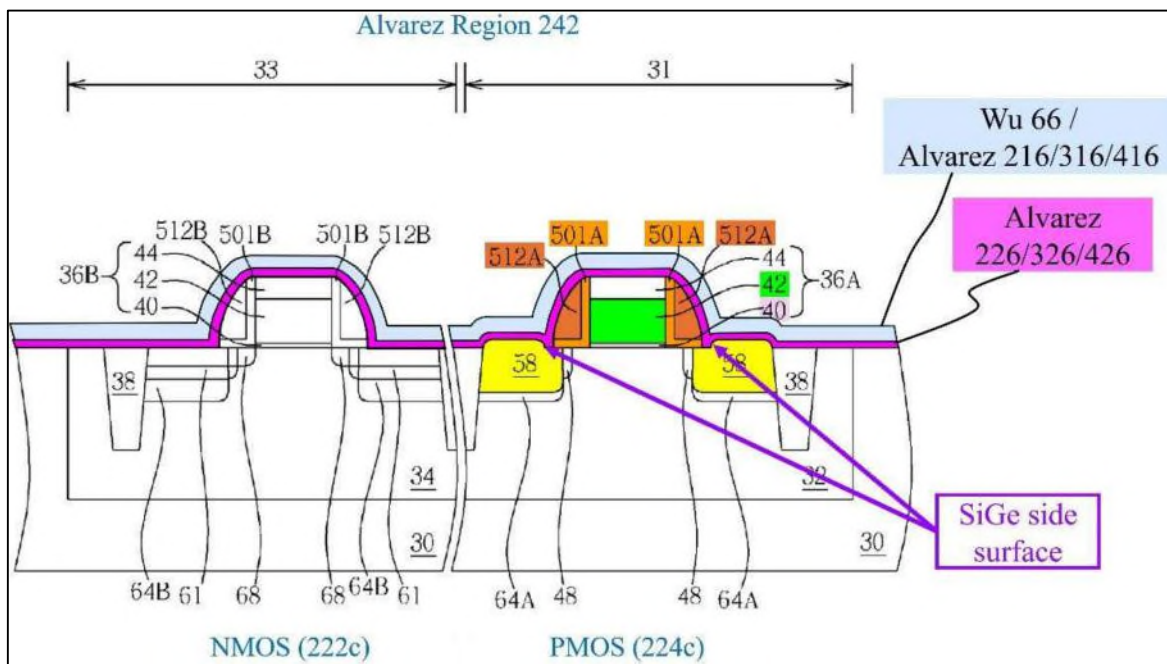


Figure A (further annotated)

5. Dependent Claim 7

a. Preamble: “The semiconductor device of claim 1,”

217. As described in Section X.A.1. and X.A.2. above, the Wu922-Alvarez combination discloses the semiconductor device of Claim 1.

b. Element 7[a]: “wherein the first MIS transistor is a p-type MIS transistor,”

218. As explained in Section X.A.1. above, Wu922 discloses that the first MIS transistor is a pFET (i.e., p-type MIS transistor) in “PMOS transistor region 31.” *See* Wu922, Ex.1005, ¶[0017]. The embodiment of the Wu922-Alvarez combination discussed for claim 1 (Figure A) includes the pFET in a region like Alvarez’s stress-control region 242. *See* Section X.A.2.b above.

c. Element 7[b]: “the first stress is a compressive stress, and”

219. As explained in Section X.A.1. above, Wu922 discloses SeGe layer causes a compressive stress to the channel because “epitaxial layer 58 has a lattice constant greater than that of the semiconductor substrate 30.” Wu922, Ex.1005, ¶¶[0021], [0041]; *See also* Wu922, Ex.1005, ¶[0005]; Section X.A.2.f above. The embodiment of the Wu922-Alvarez combination discussed for Claim 1 (Figure A) incorporates Wu922’s epitaxial SiGe regions 58, which induce a first compressive stress in the pFET channel region. *See* Sections X.A.1 and X.A.2.f above.

d. Element 7[c]: “the second stress is a tensile stress.”

220. As explained in Section X.A.1. above, the embodiment of the Wu922-Alvarez combination shown in Figure A has a tensile stress inducing CESL layer that causes a second stress on the transistor. *See* Sections X.A.1 and X.A.2.g above; Alvarez, Ex.1006, ¶¶[0022], [0054], [0065]-[0066], [0069].

6. Dependent Claim 8

a. Preamble: “The semiconductor device of claim 1,”

221. As described in Section X.A.1. and X.A.2. above, the Wu922-Alvarez combination discloses the semiconductor device of claim 1.

b. Element 8[a]: “wherein the silicon compound layer is a SiGe layer,”

222. As explained in Section X.A.1. above, Wu922 discloses that “epitaxial layer 58” may be “silicon germanium” (SiGe) when the first active area is PMOS transistor region 31. *See* Wu922, Ex.1005, ¶¶[0021], [0041], [0050]; Section X.A.1.f above. The embodiment of the Wu922-Alvarez combination discussed for claim 1 (Figure A) has Wu922’s epitaxial SiGe layer 58. *See* Sections X.A.1 and X.A.1.f above.

c. Element 8[b]: “the stress insulating film is a silicon nitride film, and”

223. As explained in Section X.A.1. above, “[t]he material of [Wu922’s] CESL 66 may include . . . a strained silicon material, i.e., silicon nitride.” Wu922,

Ex.1005, ¶[0025]; *See also* Alvarez ¶[0022], ¶[0047] (“The second material 216 preferably comprises a nitride material such as silicon nitride”); Sections X.A.1 and X.A.1.g above. I The embodiment of the Wu922-Alvarez combination discussed for claim 1 (Figure A) retains the stress insulating film (Wu922’s CESL 66) is a tensile silicon nitride film (like Alvarez’s stress-inducing layer 216/316/416). *See* Sections X.A.1 and X.A.1.f above.

d. Element 8[c]: “the first stress-relief film is a silicon oxide film.”

224. As explained in Section X.A.1. above, the embodiment of the Wu922-Alvarez combination shown in Figure A includes a stress-relief film like Alvarez’s stress-controlling film 226/326/426. *See* Sections X.A.1 and X.A.1.i above. Alvarez discloses that the film may be “an oxide such as silicon dioxide.” Alvarez, Ex.1006, ¶[0043]; *see also* Alvarez, Ex.1006, Claim 13 (claiming a “silicon dioxide” stress-controlling material); Sections X.A.1 and X.A.1.i above.

7. Dependent Claim 11

a. Preamble: “The semiconductor device of claim 1, further comprising:”

225. For the same reasons articulated in Sections X.A.1 and X.A.2 above, the Wu922-Alvarez combination renders the semiconductor device of claim obvious.

b. Element 11[a]: “a second MIS transistor, wherein:”

226. In a first mapping of the Wu922-Alvarez combination discussed in Section X.A.1 above, Figures A and B, the nFET 222c is in a “second active area [that] is an NMOS transistor region 33.” Wu922, Ex.1005, ¶¶[[0017], [0038] (“the second active area is an NMOS transistor region 33”), FIGS. 1-7, 9-14. This embodiment includes all features of the second MIS transistor recited in elements [11B]-[11F].

227. In this embodiment of the Wu922-Alvarez combination, shown below in Figure C (Figure A with additional highlighting) and Figure D (Figure B with additional highlighting), shows the second MIS transistor (nFET 222c) in what is the equivalent of Alvarez’s stress-control region 242. As shown, the second MIS transistor includes a stress-control layer (like Alvarez’s layer 226/326/426), and CESL 66 imparts a tensile stress.

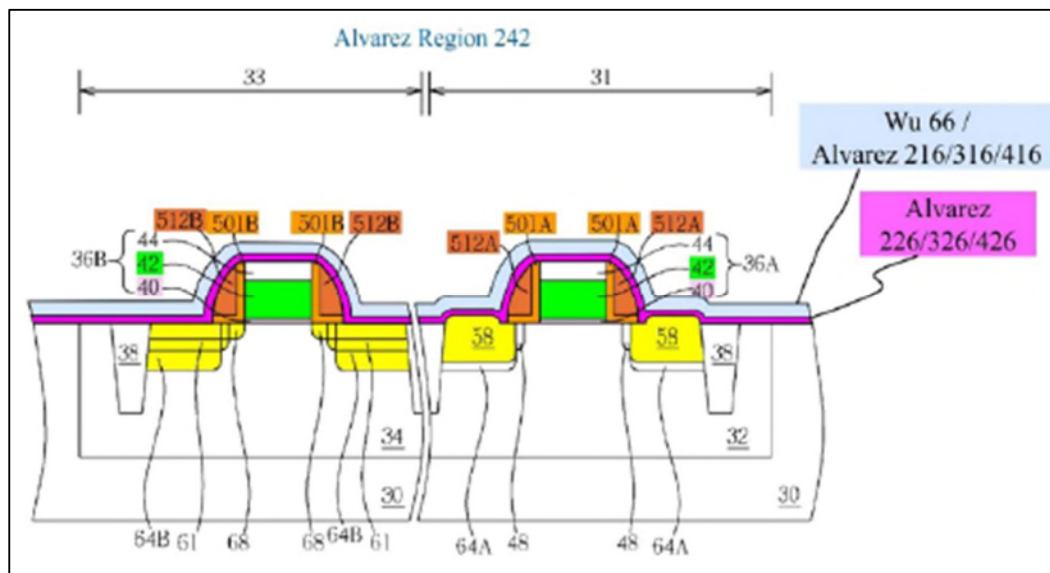
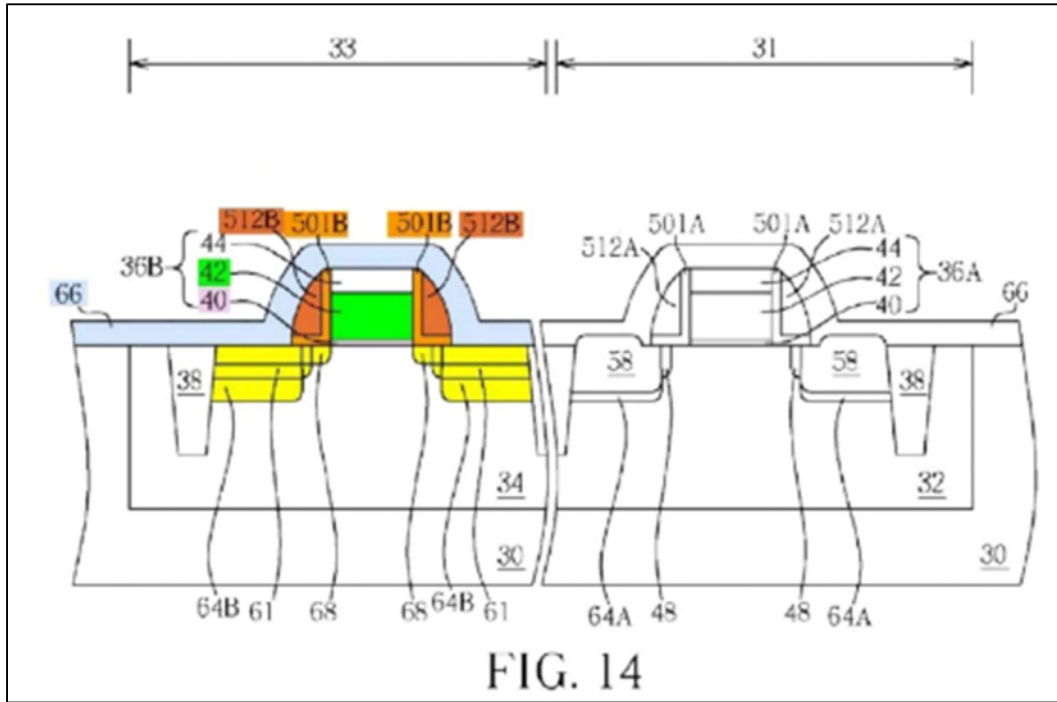


Figure C



Wu922, Ex.1005 FIG. 14 (annotated)

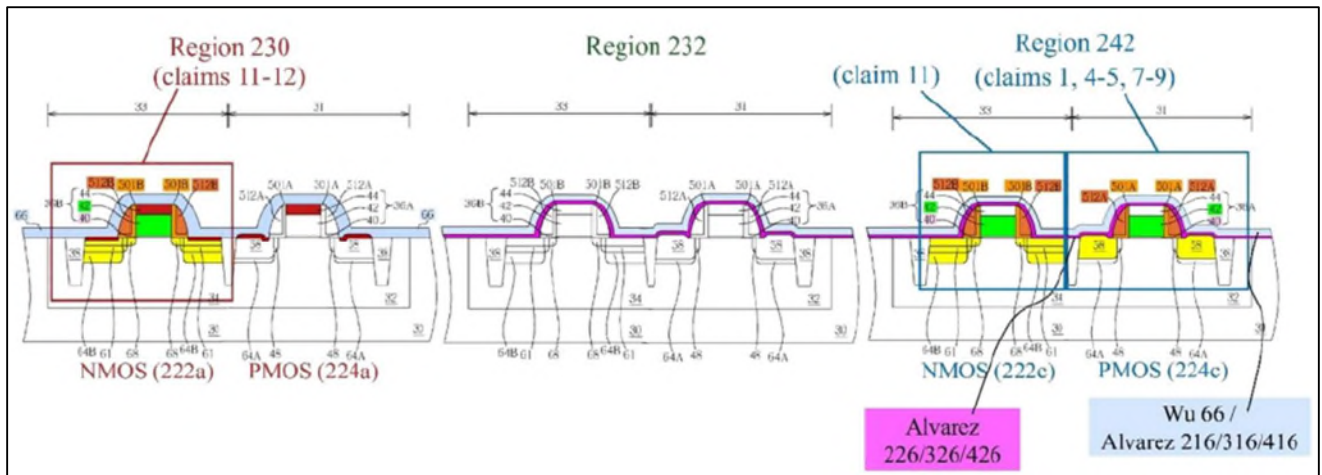
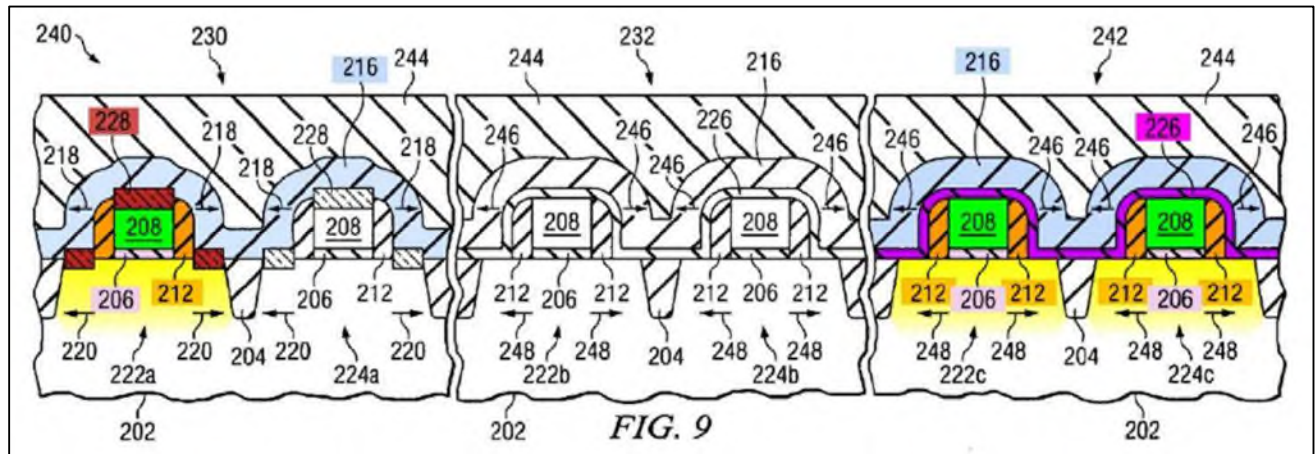


Figure D



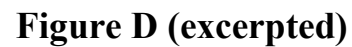
Alvarez, Ex.1006 FIG. 9 (annotated)

228. In a second mapping of the Wu922-Alvarez combination of claim 11, shown in composite Figure D above, the nFET 222a includes all features of the second MIS transistor of claim elements [11B]-[11F]. Alvarez teaches that some circuit regions, such as silicide region 230, do not include stress-control film 226/326/426 to allow silicidation. *See* Section X.A.1 above; Alvarez, Ex.1006, ¶¶[0042], [0044], [0046]-[0047], FIGS. 8-10. As previously discussed, Wu922 teaches that silicidation is an optional step. Wu922, Ex.1005, ¶[0043] (“[A] self-aligned silicide process is optionally performed to form a silicide layer (not shown) on the surfaces of the gate structures or the source/drain.”). In those cases under the Wu922-Alvarez combination, the nFET in transistor region 33 would include a tensile stress inducing CESL 66 (analogous to Alvarez’s layer 216/316/416) but would not include the stress-relief layer (analogous to Alvarez’s stress-controlling layer 226/326/426). Figure D above demonstrates this embodiment. Under this

second mapping, the nFET 222a in the region equivalent to Alvarez's silicide region 230 corresponds to the second MIS transistor of claim 11 (and claim 12). In both the first and second mappings of claim 11, the pFET 224c in a region equivalent to Alvarez's stress-control region 242 resembles the transistor of claim 1. *See* Sections X.A.1 and X.A.2 above.

c. Element 11[b]: “the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate,”

229. Applicable to both mappings discussed for claim element [11A] (see Section X.A.7.b) above), Wu922 discloses a second gate insulating film (“gate dielectric layer 40”) formed on “NMOS transistor region 33” of the “second active area” (second active region) of “semiconductor substrate 30.” Wu922, Ex.1005, ¶¶[0017] (explaining that “the second active area is an NMOS transistor region 33” having a “gate dielectric layer 40” in “gate structure[] . . . 36B”), [0038]-[0039] (describing “gate structures 36A, 36B”). A POSITA would understand that gate dielectric 40 serves as a second gate insulating film for the same reasons it functions as a first gate dielectric in claim 1. *See* Section X.A.2.c above. The only difference between the first and second gate dielectric is the location. Gate dielectric layer 40 in pFET 224c corresponds to the first gate insulating film, and gate dielectric layer 40 in nFET 222c (first mapping) or nFET 222a (second mapping) corresponds to the second gate insulating film. The gate dielectric film 40 (highlighted light purple



d. Element 11[c]: “a second gate electrode formed on a second gate insulating film,”

230. As relevant to both mappings discussed for claim element [11A] (see Section X.A.7.b above), Wu922 discloses a second gate electrode (“gate 42”) formed on gate dielectric 40. Wu922, Ex.1005, ¶[0017]. A POSITA would have understood gate 42 is a gate electrode for the same reasons it is a first gate electrode in claim 1. *See* Section X.A.2.d above. The only difference between the first and second gate electrode is the location on the pFET vs. the nFET. Gate 42 in pFET 224c of the Wu922-Alvarez combination is the first gate electrode, and gate 42 in nFET 222c (first mapping) or nFET 222a (second mapping) is the second gate electrode.

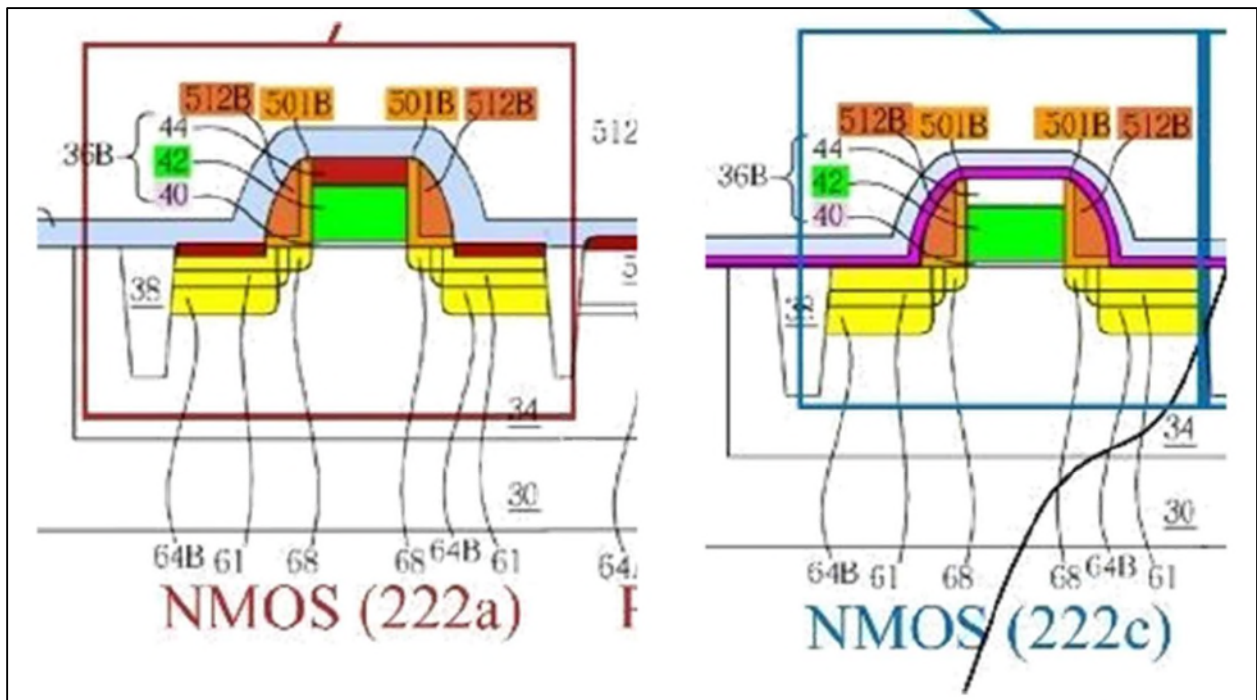


Figure D (excerpted)

Figure D (excerpted)

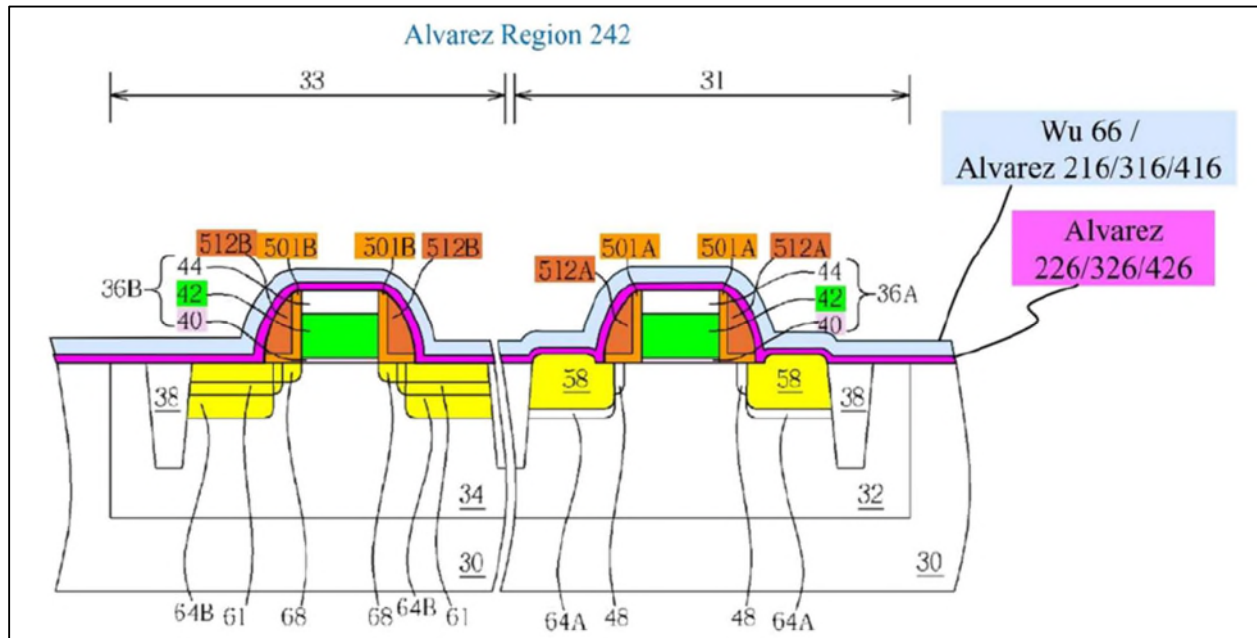


Figure C

231. Gate 42 may be made from “polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof.” Wu922, Ex.1005, ¶[0017], FIGS. 7, 14. In the Wu922-Alvarez combination, the nFETs 222a and 222c both include a gate 42 (highlighted green above) formed on the gate dielectric 40 (highlighted light purple above). *See* Figures C and D.

e. Element 11[d]: “a second sidewall spacer formed on a side surface of the second gate electrode.”

232. Applicable to both mappings discussed for claim element [11A] (see Section X.A.7.b above), Wu922 discloses a second sidewall spacer comprising “an oxide layer . . . 501B on sidewalls of the [nFET] gate structure[] . . . 36B” and

“second [sidewall] spacer . . . 512B . . . formed on the sidewalls of the [nFET] gate structure[] . . . 36B.” Wu922, Ex.1005, ¶¶[0017], [0024], FIGS. 7, 14. Thus, in the Wu922-Alvarez combination, like pFET 224c, which I discuss for claim 1, both mappings contain a second sidewall spacer comprising oxide layer 501B and second sidewall spacer 512B. *See* Section X.A.2.e above.

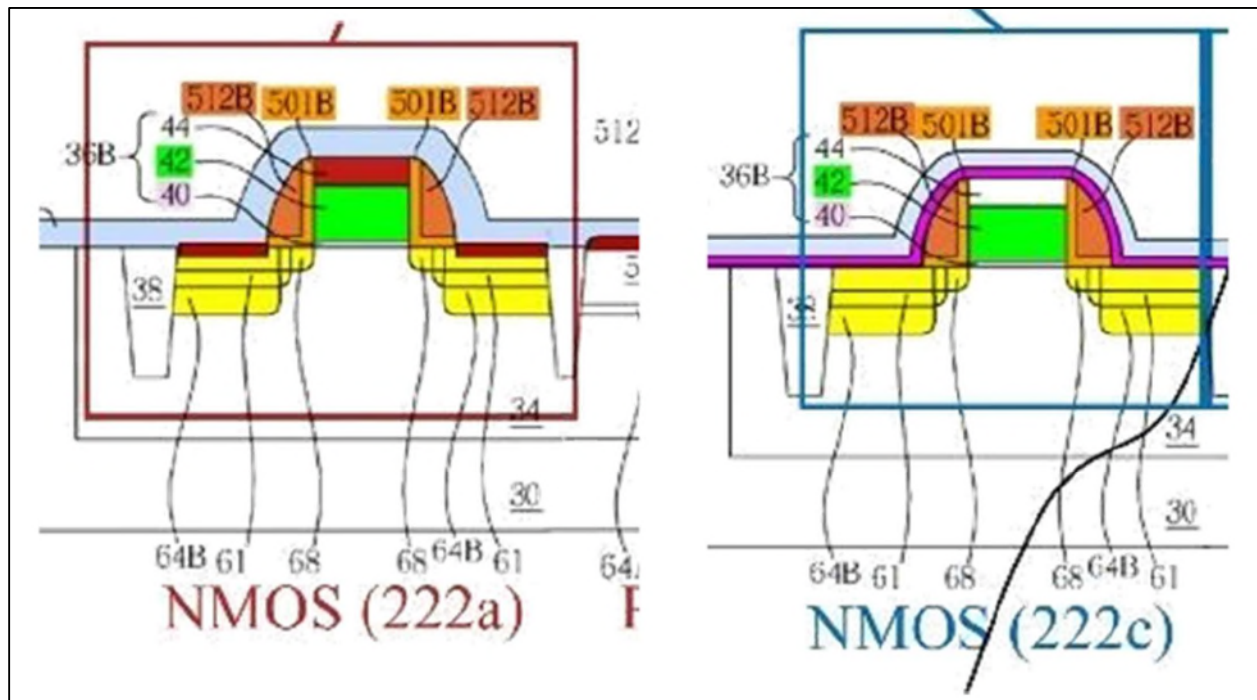


Figure D (excerpted)

Figure D (excerpted)

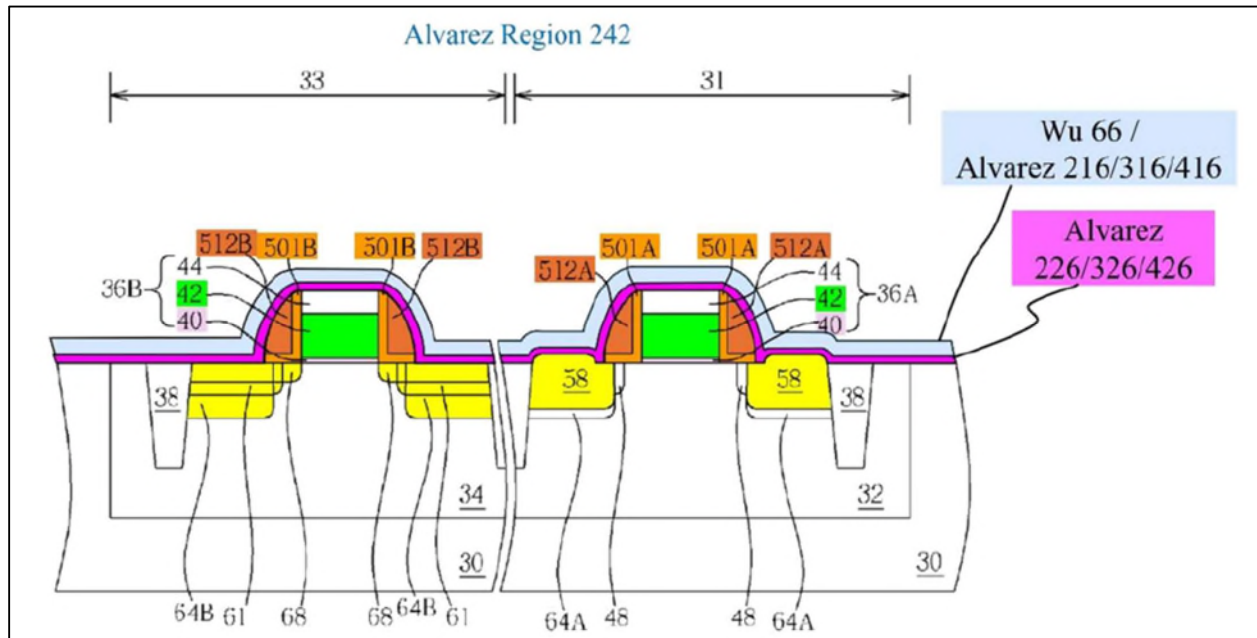


Figure C

233. Just like in the Wu922-Alvarez combination's pFET 224c, the oxide layer 501B and the sidewall spacer 512B are positioned against the side surfaces of gate 42 within the NMOS transistor region 33. *See* Section X.A.2.e above; Wu922, FIGS. 7, 14. Together or on their own, oxide layer 501B and sidewall spacer 512B disclose a second sidewall spacer formed along the side surface of the second gate electrode (gate 42) within nFETs 222c (first mapping) and 222a (second mapping). In the Wu922-Alvarez combination, both nFETs 222a and 222c feature a second sidewall spacer that includes the oxide spacer 501B (highlighted in light orange) and/or the secondary sidewall spacer 512B (highlighted in dark orange), each formed on the side surfaces of gate electrode 42 (highlighted in green) of gate structure 36B. *See* Figures C and D above.

f. Element 11[e]: “a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer, and”

234. Applicable to both mappings discussed for claim element [11A] (see Section X.A.7.b above), Wu922 discloses an n-type (the second conductivity type) second source/drain region in NMOS transistor region 33 (the second active region). Wu922 specifically discloses n-type source/drain regions 64B, n-type lightly doped drain extensions NLDD1 61, and n-type lightly doped drain extensions NLDD2 68. Wu922, Ex.1005, ¶¶[0023]-[0024], [0038]-[0039], [0042]-[0044], FIGS. 7, 14. In the Wu922-Alvarez combination, the n-type source/drain regions (highlighted yellow below) of both nFET 222c (first mapping) and nFET 222a (second mapping) are formed on a lateral side of second sidewall spacer layers 501B (highlighted light orange below) and 512B (highlighted dark orange below) and beside nFET gate structure 36B. *See* Figures C and D.

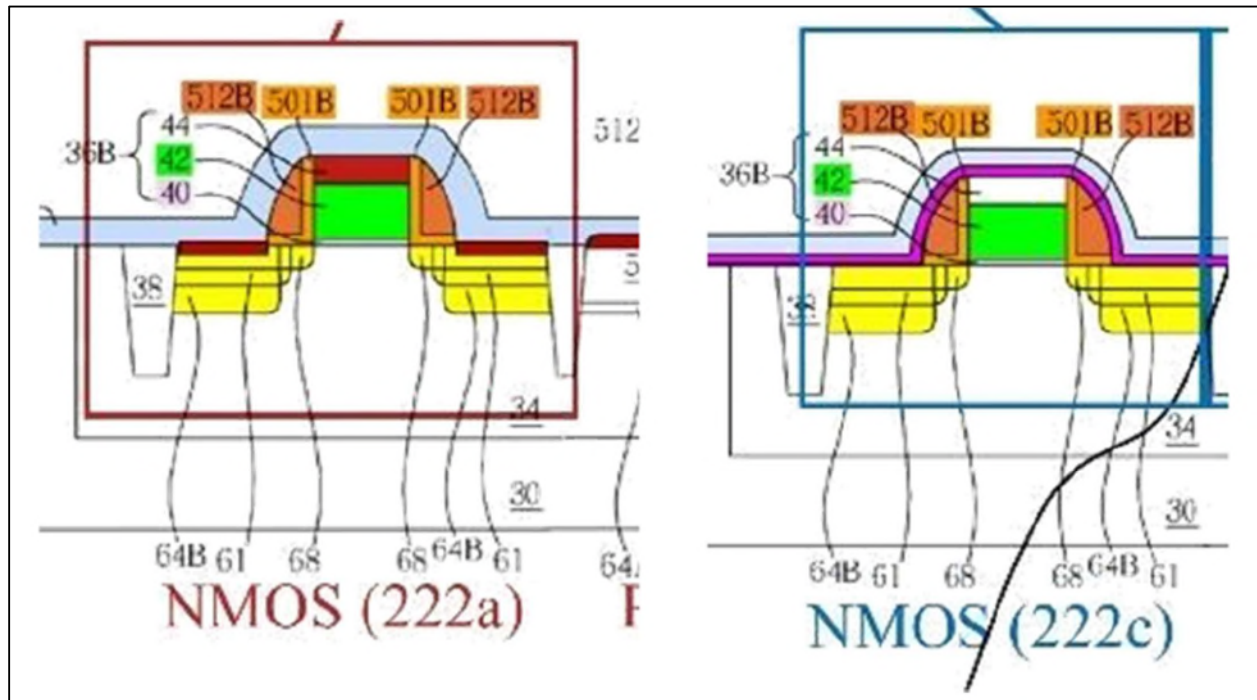


Figure D (excerpted)

Figure D (excerpted)

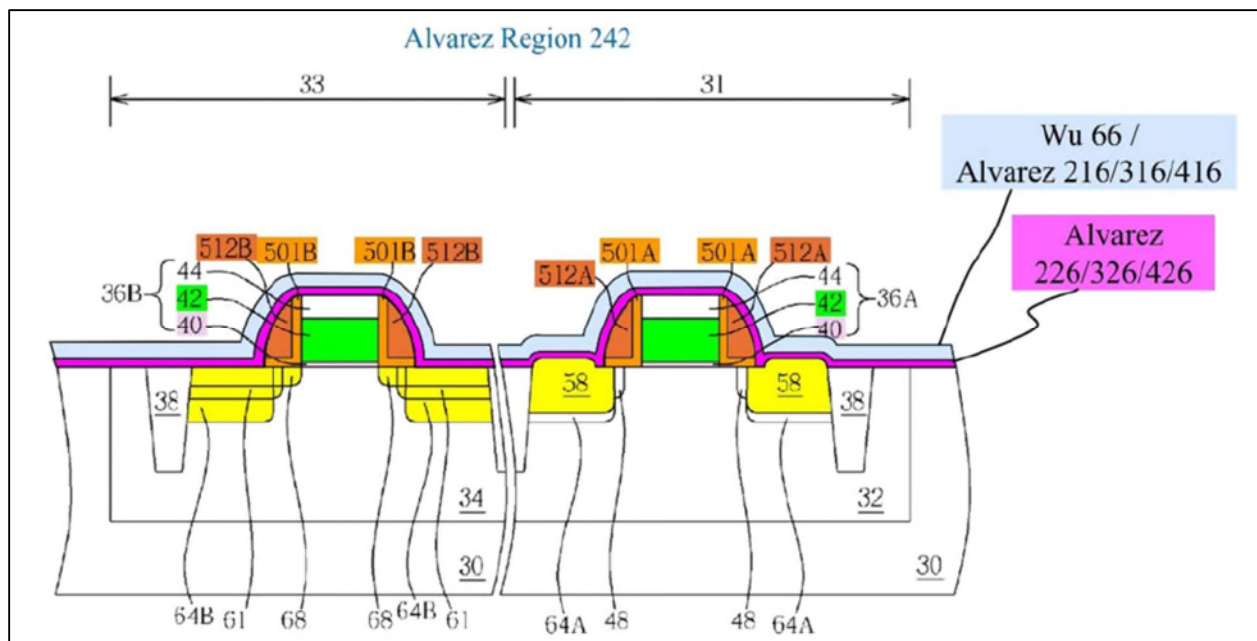


Figure C

- g. Element 11[f]: “the stress insulating film formed on the second active region to cover the second gate electrode, the second sidewall spacer, and the second source/drain region.”**

235. Applicable to both mappings discussed for claim element [11A] (see Section X.A.7.b above), the Wu922-Alvarez combination includes the stress insulating film (tensile CESL 66, highlighted light blue) formed over both the pFETs and the nFETs in circuit regions that are analogous to Alvarez’s silicide region 230 and stress-control region 242. *See* Sections X.A.1 and X.A.2.g above.

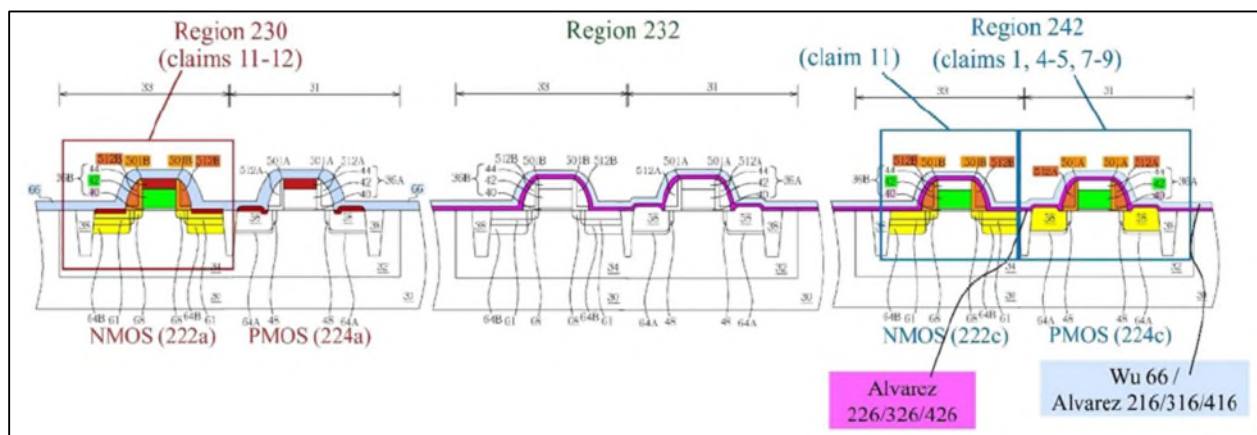
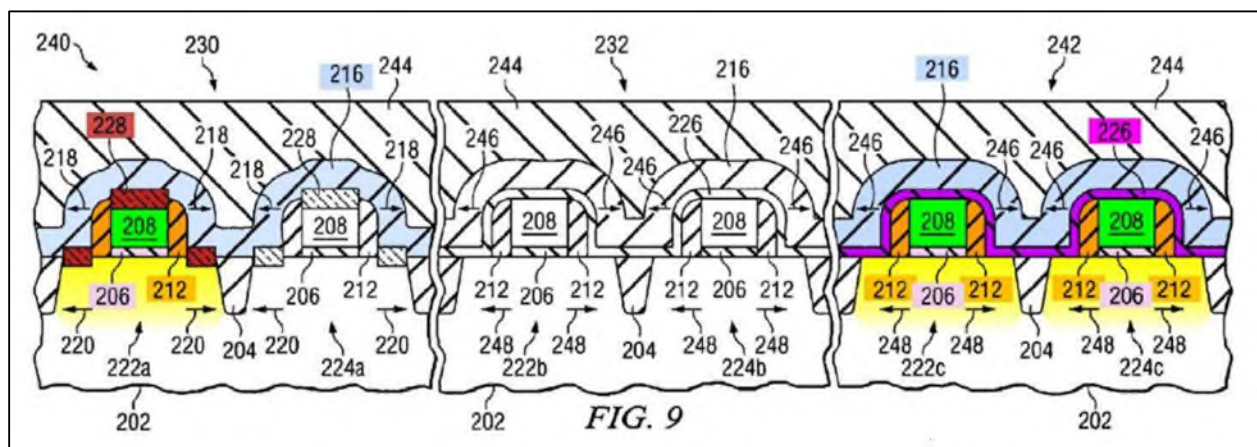


Figure D



Alvarez, Ex.1006 FIG. 9 (annotated)

236. In both mappings of the Wu922-Alvarez combination, nFET 222c (first mapping) and nFET 222a (second mapping) both include tensile CESL 66 (highlighted light blue below) covering gate electrode 42 (highlighted green below), second sidewall spacer layers 501B (highlighted light orange below) and 512B (highlighted dark orange below), and n-type source/drain regions 61/64B/68 (highlighted yellow below). See Figure C and D below. I include an annotated version of Alvarez's FIG. 9 for comparison with Figure D and an annotated version of Wu922's FIG. 14 for comparison with the general FET structures shown in Figures C and D.

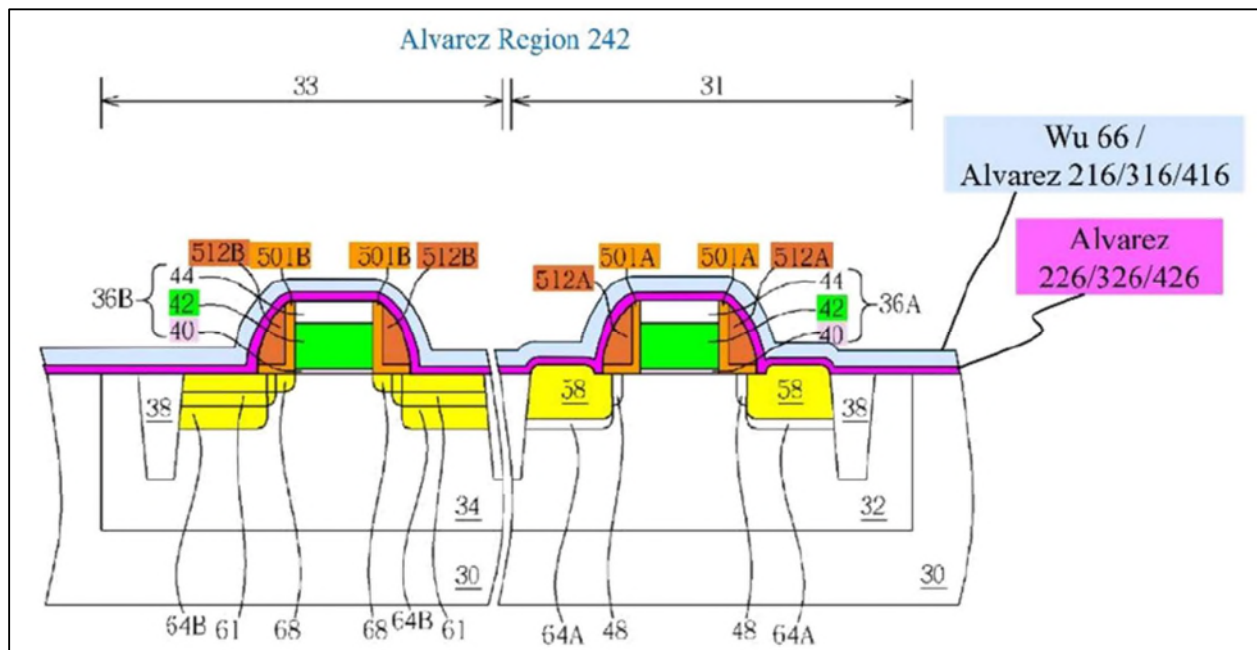
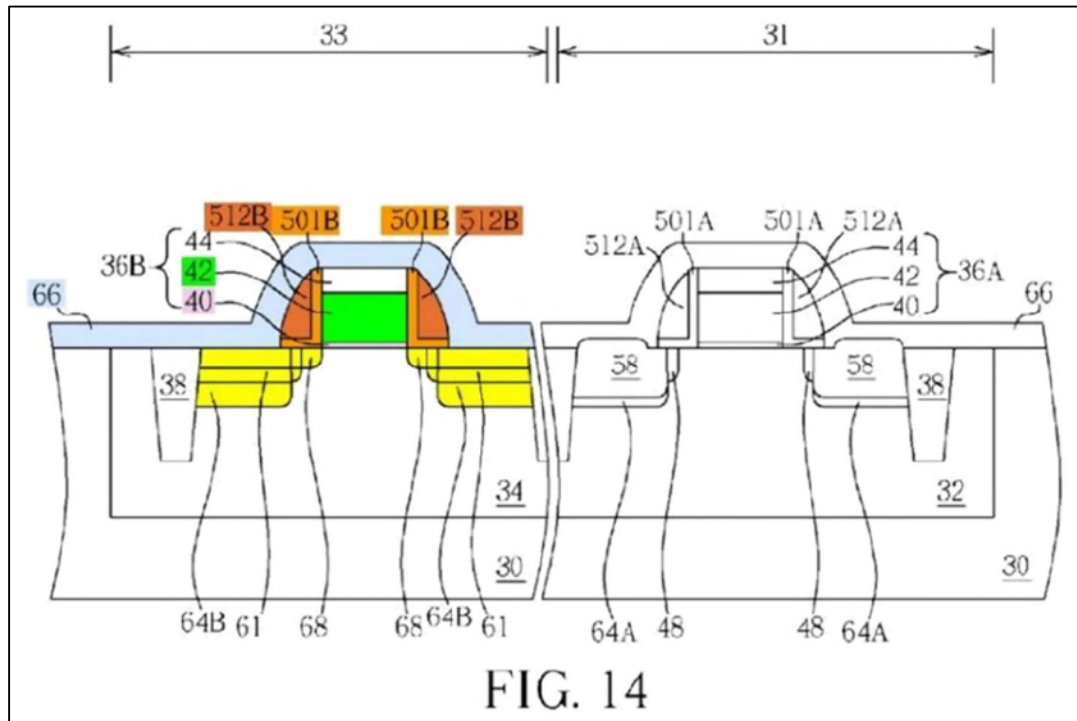


Figure C



Wu922, Ex.1005 FIG. 14 (annotated)

B. Ground 2 and 2A

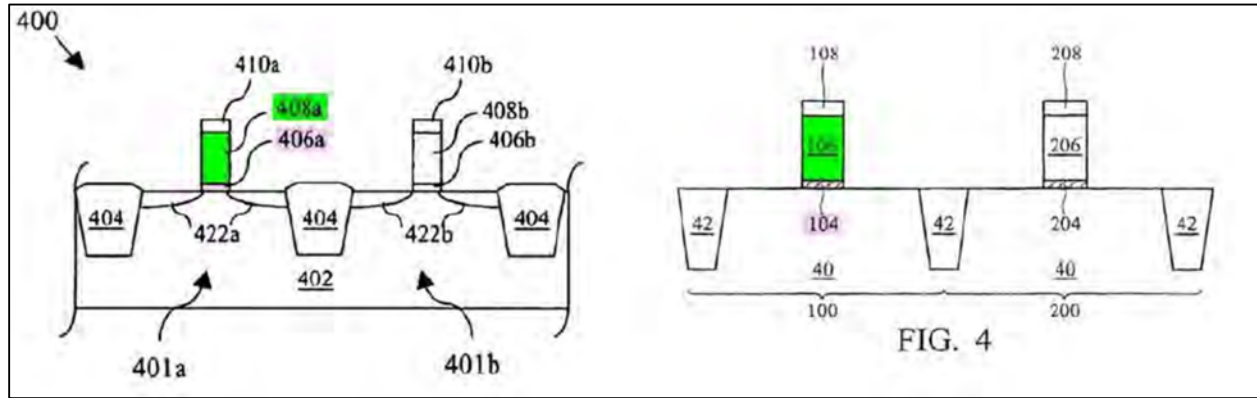
237. In my opinion, Cheng817 alone (Ground 2) and combination of Cheng817 and Wang906 (Ground 2A, *Infra* Section X.B.7) both render claims 1, 3, 4, 7, 8, and 11 of the '425 patent obvious.

238. In my opinion, a POSITA would have found Cheng817's description clear and sufficient to disclose all the claimed elements of Claims 1, 3, 4, 7, 8, and 11 of the '425 patent. However, I recognize that some of the figures do not explicitly show each feature and detail that is described in the written description of Cheng817, for example Figs. 4e-4j. Even so, a POSITA would have understood the processes clearly described in the textual description of Cheng817 and would have

understood how Cheng817 figures, for example Fig. 4j, should have appeared in the context of the written description.

239. To further support this position, Wang906 provide clear evidence on what a POSITA would have understood. Like Cheng817, Wang906 describes a MOS device formed using similar processes as Cheng817. Accordingly, a POSTA would have understood that Wang906's figures illustrate how a POSITA would have understood Cheng817's textual descriptions. *Compare* Cheng817, Ex.1008, ¶¶[0056]-[0070], Figs. 4a-4j, *with* Wang906, Ex.1009, ¶¶[0023]-[0032], FIGS. 4-9.

240. Cheng817 explains that Figs. 4a-4j show “sectional views . . . for making semiconductor devices 401a and 401b.” Cheng817, Ex.1008, ¶[0056]. Likewise, Wang906's FIGS. 4-9 show “cross-sectional views of intermediate stages in the fabrication of” a pMOS device. Wang906, Ex.1009, ¶[0019]. Cheng817's Fig. 4a mirrors Wang906's FIG. 4. Both figures show the formation of a gate dielectric film (layer 406a in Cheng817 and layer 104 in Wang906, both highlighted light purple below) and a gate electrode (layer 408a in Cheng817 and layer 106 in Wang906, both highlighted green below) as shown below. *Compare* Cheng817, Ex.1008, ¶[0056], Fig. 4a, *with* Wang906, Ex.1009, ¶[0023], FIG. 4.

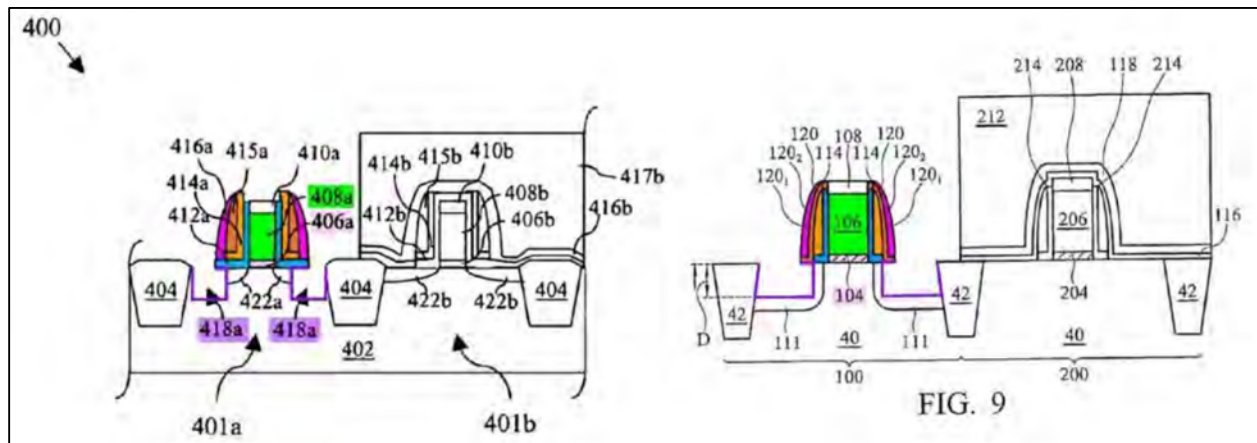


**Cheng817, Ex.1008, Fig. 4a
(annotated)**

**Wang906, Ex.1009 FIG. 4
(annotated)**

241. Cheng817's Figs. 4b-4d and Wang906's FIGS. 5-8 show the same processes including forming the gate electrode sidewalls (highlighted orange and blue, respectively, below) and dummy spacers (highlighted magenta below), then etching recesses (outlined purple below) into the substrate for subsequent epitaxial SiGe growth, as shown below. *Compare* Cheng817, Ex.1008, ¶¶[0061]-[0063], Figs. 4b-4c, *with* Wang906, Ex.1009, ¶¶[0025]-[0028], FIGS. 5-8. Wang906's FIG. 9 on the right below has been modified to remove the epitaxially grown SiGe to correspond to Cheng817's process step shown in Fig. 4d. In Cheng817's pFET 401a of Fig. 4d (on the left below), the sidewall dielectric layer 412a (highlighted blue below) sits beneath the dummy spacer 416a (highlighted magenta below). Because of the way in which it is formed, sidewall dielectric layer 412a (also highlighted blue below) stops laterally at the outer edge of dummy spacer 416a (also highlighted magenta below). Cheng817, Ex.1008, ¶[0064], Fig. 4d. Likewise, Wang906's

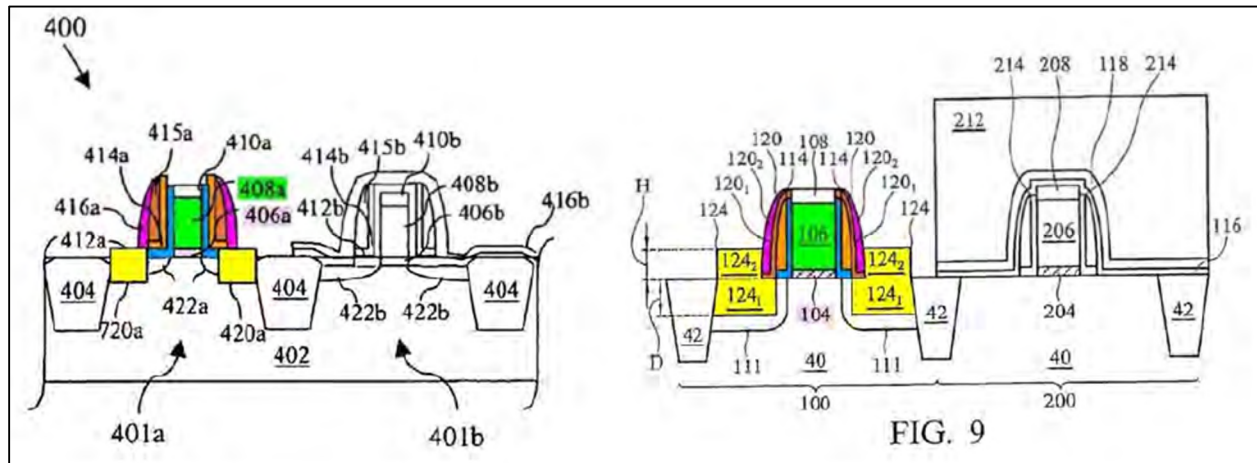
sidewall spacer inner portion 120₁ (highlighted burnt orange below) also sits beneath sidewall spacer outer portion 120₂ (highlighted magenta below). Based on the steps above, sidewall spacer inner portion 120₁ (highlighted burnt orange below) stops laterally at the outer edge of sidewall spacer outer portion 120₂ (highlighted magenta below). *See* Wang906, Ex.1009, ¶[0030], FIG. 9.



Cheng817, Ex.1008, Fig. 4d (annotated) Modified Wang906, Ex.1009 FIG. 9 (modified, annotated)

242. As shown below, both Cheng817's Fig. 4e and Wang906's FIG. 9 show growing epitaxial SiGe layers (Cheng817's layers 420a⁶ and Wang906's layers 1241, 1242, both highlighted yellow below) in trenches of the substrate, where they are formed such that the top of the SiGe layers extend above the top surface of the semiconductor substrate. *Compare* Cheng817, Ex.1008, ¶[0022], ¶[0065], Fig. 4e, *with* Wang906, Ex.1009, ¶¶[0030]-[0032], FIG. 9.

⁶ The layer mislabeled "720a" on the left of Cheng817's Fig. 4e should read "420a."



**Cheng817, Ex.1008, Fig. 4e
(annotated)**

**Wang906, Ex.1009 FIG. 9
(annotated)**

243. A POSITA, upon reviewing Cheng817's textual description and Figs. 4a-4e, would recognize that Cheng817's Fig. 4e contains an error. Comparing Cheng817's Figs. 4d and 4e, the epitaxial SiGe regions in Fig. 4e (720a [sic:420a] and 420a, both highlighted in yellow) are illustrated in a way that suggests they replace portions of the non-crystalline sidewall structures 412a (highlighted blue). with knowledge of how epitaxial SiGe grows, would recognize that in Cheng817's Fig. 4e, the epitaxial SiGe regions would selectively grow on the crystalline surfaces within the recesses. Subsequently, these regions would extend upward and around the non-crystalline sidewalls 412a and 416a located on the outer side of Cheng817's pFET. This understanding has been used to modify Cheng817's Fig. 4e below (left). Wang906's FIG. 9 demonstrates Wang906 and Cheng817's descriptions are similar.



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of the trench. Cheng817, Ex.1008, ¶¶[0018], [0022]. Wang906 confirms this and explains that “raised [SiGe] portions 1242 [(yellow)] preferably have a height H of less than the height of the gate electrode 106 [(green)], and more preferably between about 100 Å and about 700 Å [10-70 nm].” Wang906, Ex.1009, ¶[0031]. Accordingly, both Cheng817 and Wang906 disclose that the epitaxial SiGe (highlighted yellow above) is grown above the height of the lower, horizontal portion of the “L”-shaped sidewall (highlighted blue above) such that it grows up and around Cheng817’s dummy spacer 416a or Wang906’s comparable sidewall spacer outer portion 1202 (both highlighted magenta above).

245. A POSITA would have understood that the correction to Cheng817’s Fig. 4e above would also apply to Cheng817’s Figs. 4f-4j as the method of forming the device continues. The subsequent steps do not alter the shape of the epitaxially grown SiGe regions, the sidewalls, or dummy spacer 416a. *See* Cheng817, Ex.1008, ¶¶[0066]-[0070].

246. The final product of Cheng817’s Figs. 4a-4j, based on modifying Cheng817’s Fig. 4j as described above, is shown in Figure I. This shows how the correction of element 420a would carry through Cheng817’s final pFET structure. A POSITA would have readily understood and found it obvious—reasonably based on Cheng817’s textual disclosures alone or in view of Wang906 (which just confirm a POSITA’s understanding of Cheng817’s textual descriptions)—that Cheng817

teaches a pFET shown in Figure I below (correcting Cheng817's Fig. 4j). In other words, Figure I more accurately illustrates the result of the manufacturing process described in Cheng817. *See* Cheng817, Ex.1008, ¶¶[0056]-[0070].

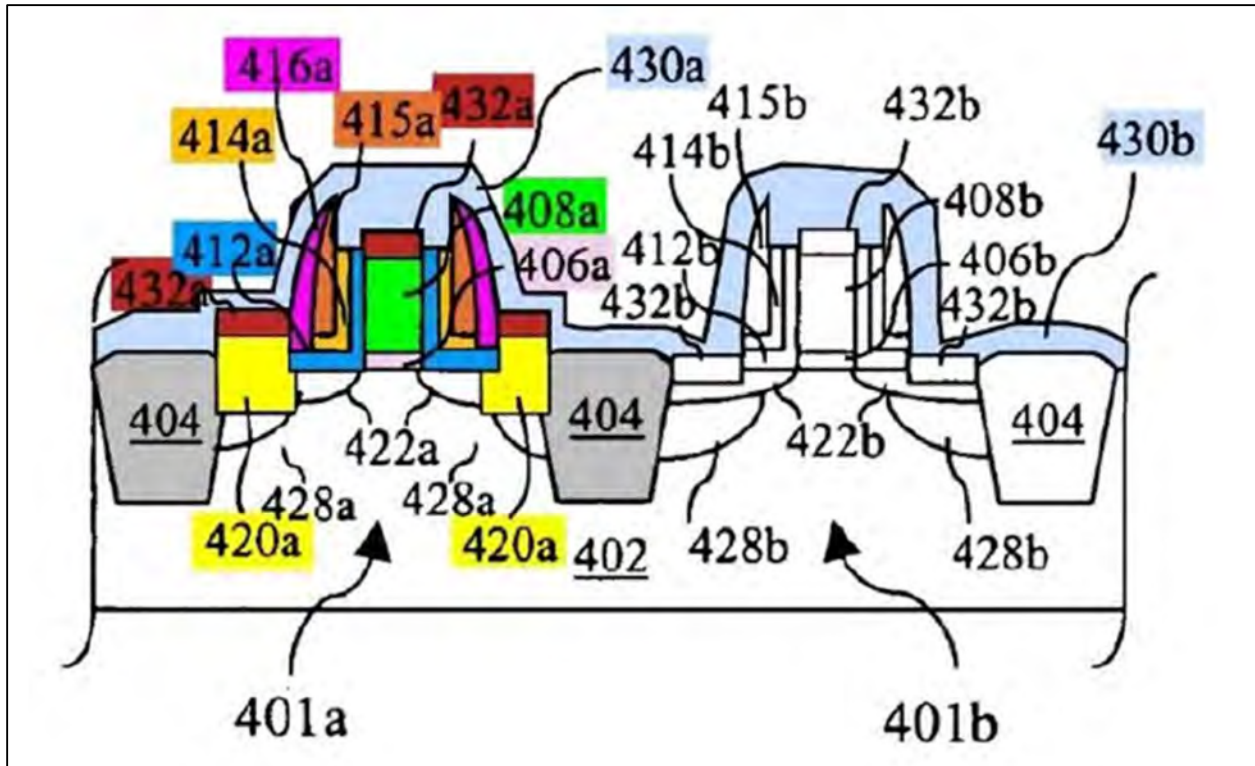


Figure I (annotating and correcting Cheng817, Ex.1008 Fig. 4j)

247. Accordingly, it is my opinion that a POSITA would have found the structure shown in Figure I obvious based either solely on Cheng817's textual disclosures, or further in view of Wang906, because it is an example of applying a known teaching, motivation, or suggestion in the prior art (Cheng817's express disclosures relating to Figs. 4a-4j, either alone or in view of Wang906's express disclosures in conjunction with FIGS. 4-9) to make it to the claimed invention (as

illustrated in the more accurate Figure I shown above, rather than as depicted in Cheng817's Fig. 4j.).

248. In summary, a POSITA would have understood that Figure I above more accurately reflects the end result of the process Cheng817 describes in connection with Figs. 4a-4j for the reasons described above. A POSITA would have come to this conclusion whether reviewing only Cheng817's textual descriptions alone or in conjunction with Wang906.

249. To summarize, in my opinion, a POSITA would have found the structure of Figure I obvious based either on Cheng817's text alone or in combination with Wang906, because the correction of Cheng817's Fig. 4j reflected in Figure I to element 420a is an example of the following:

- It combines known prior art elements (Cheng817's epitaxial SiGe source/drains 420a being formed to height well above the surface of the substrate, as Cheng817 expressly describes and Wang906 confirms) according to known methods (growing SiGe in a trench of the substrate for enough time that it extends to a height above the top of the substrate using well known deposition techniques) to yield predictable results (conventional raised SiGe layers like the ones used in several generations of high-volume commercial products).

- It uses a known technique (epitaxially growing SiGe in a trench of the substrate to a height above the top of the substrate, as Cheng817 expressly describes and Wang906 confirms) to improve similar devices (Cheng817's own MOSFETs) in the same way (by applying compressive stress to the pFET channel region to boost hole mobility).
- It applies a known technique (epitaxially growing SiGe in a trench of the substrate to a height above the top of the substrate, as Cheng817 expressly describes and Wang906 confirms) to a known device ready for improvement (Cheng817's own MOSFETs) to yield predictable results (conventional raised SiGe layers like the ones used in several generations of high-volume commercial products).
- It applies a known teaching, motivation, or suggestion in the prior art (Cheng817's and/or Wang906's express disclosures, as discussed above, about growing conventional, raised SiGe layers) that would have led a POSITA to modify Cheng817 according to, or to combine Cheng817 with, its own textual descriptions and/or the teachings of Wang906 to arrive at the claimed invention.

1. Independent Claim 1

a. Preamble: “A semiconductor device comprising:”

250. Cheng817 discloses a semiconductor device. *See* Cheng817, Ex.1008, ¶¶[0056]-[0071], Fig. 4j. For example, Cheng817 is directed to an “embodiment of a method for making semiconductor devices 401a and 401b with high drive current.” Cheng817, Ex.1008, ¶[0056], FIGS. 4a-4j. As Cheng817 states, “[t]he semiconductor device 401a may be a P-type MOS device and the semiconductor device 401b may be an N-type MOS device.” Cheng817, Ex.1008, ¶[0056], Figs. 4a-4j.

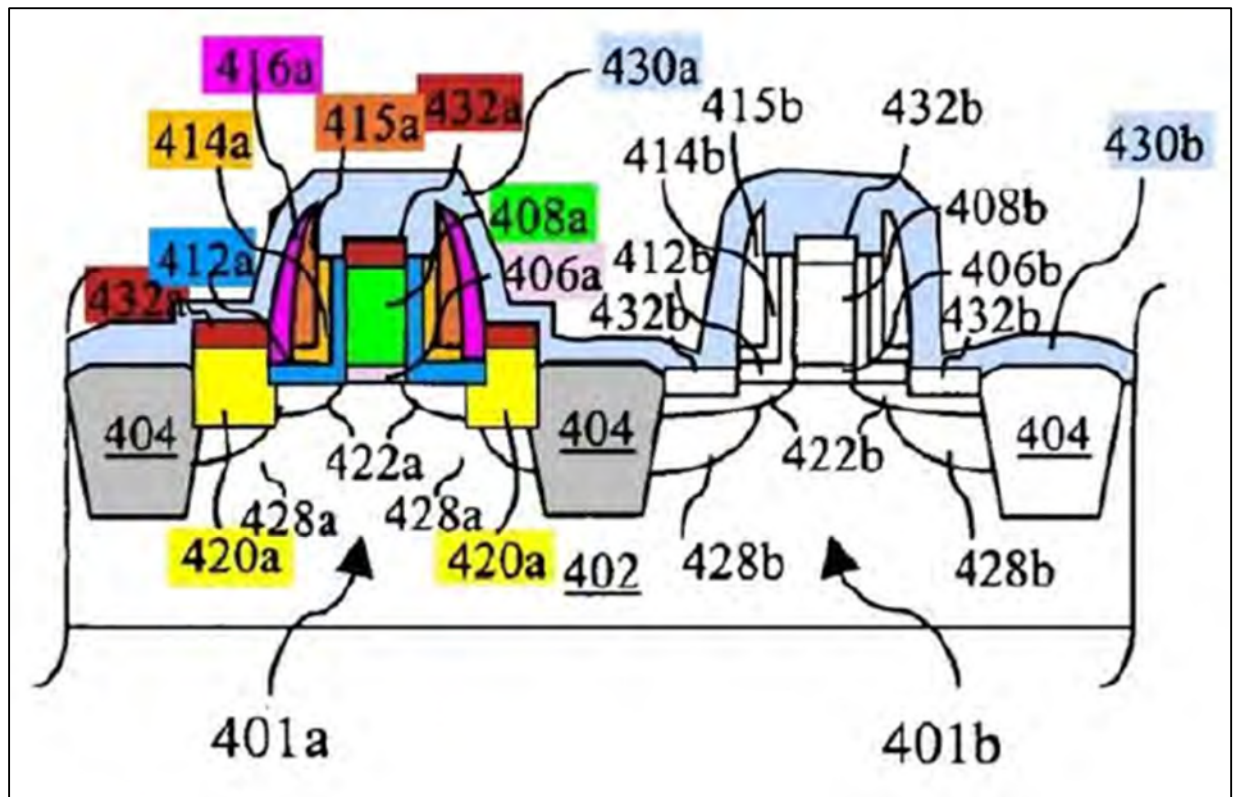


Figure I

b. Element 1[a]: “a first MIS transistor wherein:”

251. Cheng817 discloses a first MIS transistor. *See* Cheng817, Ex.1008, ¶¶[0056]-[0071], Fig. 4j. Namely, Cheng817 discloses that “semiconductor device 401a may be a P-type MOS device,” i.e., a pFET. Cheng817, Ex.1008, ¶[0056], Figs. 4a-4j. The “P-type MOS device” 401a (first MISFET transistor) of Cheng817’s semiconductor device is shown above in Figure I. *See* Section X.B above.

c. Element 1[b]: “a first gate insulating film formed on a first active region in a semiconductor substrate”

252. Cheng817 discloses a first gate insulating film formed on a first active region in a semiconductor substrate. For example, Cheng817’s “gate dielectric 406a [PMOS] and 406b [NMOS] are formed over a substrate 402 for devices [PMOS] 401a and [NMOS] 401b, respectively.” Cheng817, Ex.1008, ¶[0056], Figs. 4a-4j. Cheng817’s gate dielectric layer 406a corresponds to a first gate insulating film because it is made of materials such as “silicon oxide” or “SiO₂” (i.e., silicon dioxide), just as the ’425 patent. Cheng817, Ex.1008, ¶¶[0058], [0020]; *see also* The ’425 patent, Ex.1001, 9:15-19.

253. Cheng817’s gate dielectric 406a is formed on substrate 402, which contains an active region. It is well understood in the art that an active region is the area a MIS transistor (e.g., PMOS device 401a) is located on the semiconductor substrate. Cheng817 discloses the active region and states: “lightly doped regions 422a” having “P-type . . . dopants,” “doped source and drain regions 420a,” and

“heavily doped . . . regions 428a.” Cheng817, Ex.1008, ¶¶[0056], [0060], [0065]-[0068], Fig. 4j.

254. In Figure I below, pFET 401a is the first MISFET transistor. *See* Section X.B (introduction) above. As shown here, the insulating film 406a (highlighted light purple) of pFET 401a is formed on the active region, the portion of the substrate between the two lightly doped regions 422a.

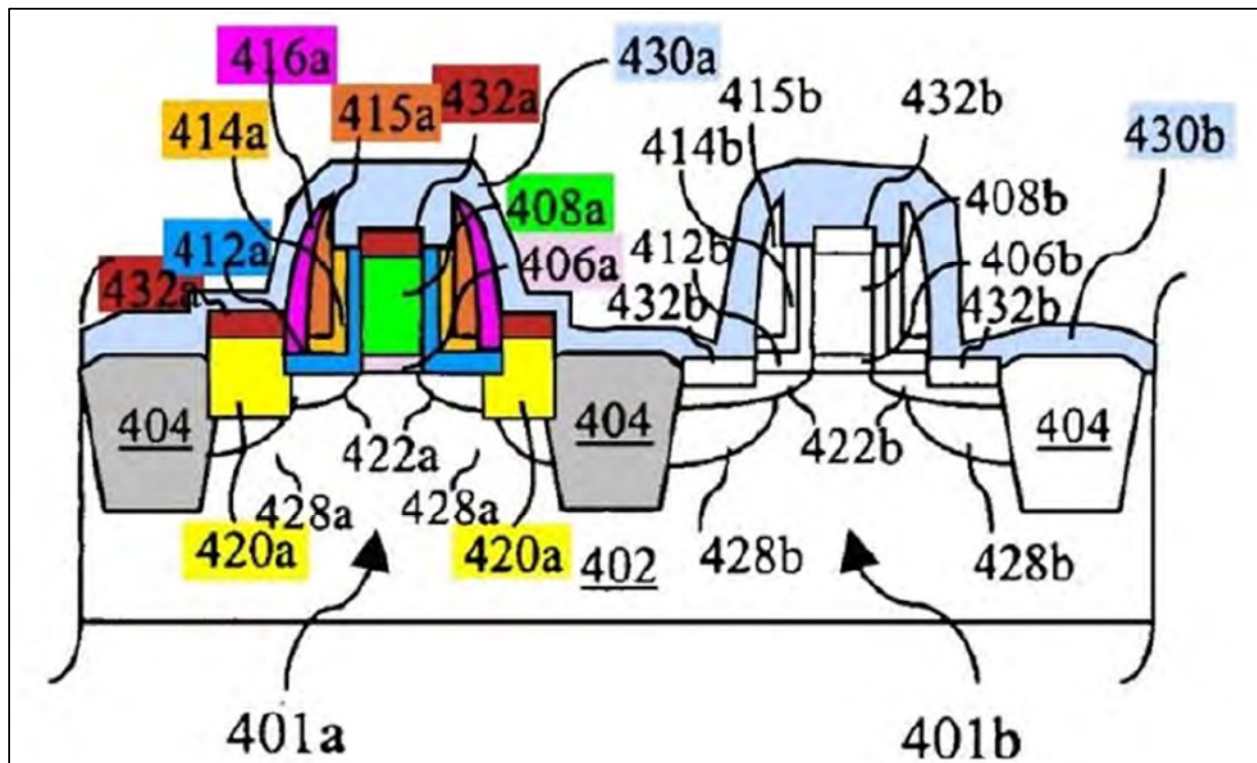


Figure I

- d. **Element 1[c]: “a first gate electrode formed on the first gate insulating film,”**

255. Cheng817 discloses a first gate electrode formed on the first gate insulating film. Cheng817 teaches “[g]ate electrodes 408a and 408b are formed over

the gate dielectric layer [406a, 406b].” Cheng817, Ex.1008, ¶[0056]. The gate electrode 408a (highlighted green above) is formed on the first gate dielectric 406a (highlighted light purple above) of Cheng817’s pFET 401a as seen above in in Figure I. *See* Section X.B above.

e. Element 1[d]: “a first sidewall spacer formed on a side surface of the first gate electrode,”

256. Cheng817 discloses a first sidewall spacer formed on a side surface of the first gate electrode. Cheng817 teaches a first sidewall spacer that includes “sidewall dielectric layer [] . . . 414[] and spacer material 415 . . . disposed over the semiconductor device(s) 410a [sic:401a] and 401b.” Cheng817, Ex.1008, ¶[0061]. Cheng817 teaches that then “subsequent process[ing], such as by etching,” occurs where the dielectric layer 414 and spacer material 415 layer are etched and formed into “sidewall dielectric structures” 414a and “spacers” 415a, as Cheng817’s Fig. 4c shows. Cheng817, Ex.1008, ¶[0061], Figs. 4b-4c. As Cheng817’s Fig. 4c shows, dielectric structure 414a and spacer 415a (together, the sidewall spacer of Claim element 1[d]) are formed on a vertical side surface of gate electrode 408a because, like the ’425 patent. *Compare* Cheng817, Ex.1008, ¶[0061], Fig. 4c, *with* The ’425 patent, Ex.1001, FIG. 6B (transistor pTr1, sidewall 19A).

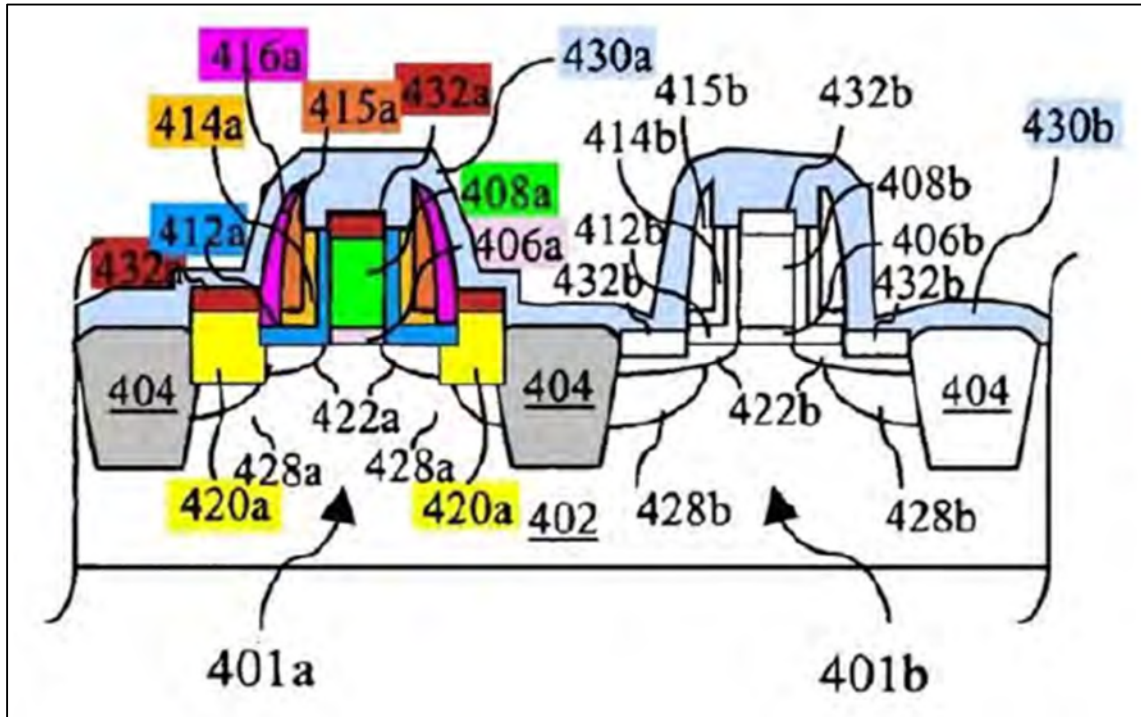


Figure I

257. As discussed in Section X.B (introduction), a POSITA would have considered Cheng817's textual descriptions, alone or in view of Wang906, and found it obvious that the first sidewall spacer would be carried through the rest of the device processing to arrive at Figure I. Figure I shows above, the first sidewall spacer (sidewall dielectric structure 414a (highlighted light orange) and spacer 415a (highlighted dark orange), collectively) is formed on the sides of gate electrode 408a (highlighted green) in Cheng817's pFET 401a.

- f. Element 1[e]: “a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region, and”**

258. Cheng817 discloses a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region. As discussed in Section X.B, Cheng817 discloses recessed trench regions 418a formed in substrate 402. Recessed regions 418a are trenches “formed by a process such as chemical etch, focused ion beam (FIB), and/or plasma etch.” Cheng817, Ex.1008, ¶[0064], Fig. 4d. Cheng817 further teaches that “doped source and drain regions 420a are formed or built-up in the recessed regions 418a.” Cheng817, Ex.1008, ¶[0065], Fig. 4e. They “may be formed by selective epitaxial growth (SEG)” of “silicon germanium.” Cheng817, Ex.1008, ¶[0065], Fig. 4e; *See* Section X.B above. Cheng817’s SiGe source/drain regions 420a are part of the pFET source/drain region and are of a p-type conductivity type. Cheng817, Ex.1008, ¶[0065]; *See also* Miyashita, Ex.1435, ¶¶[0050]-[0051]; Chen729, Ex.1421 ¶[0021]; Bohr, Ex.1527, ¶[0028], FIGS. 4-7.

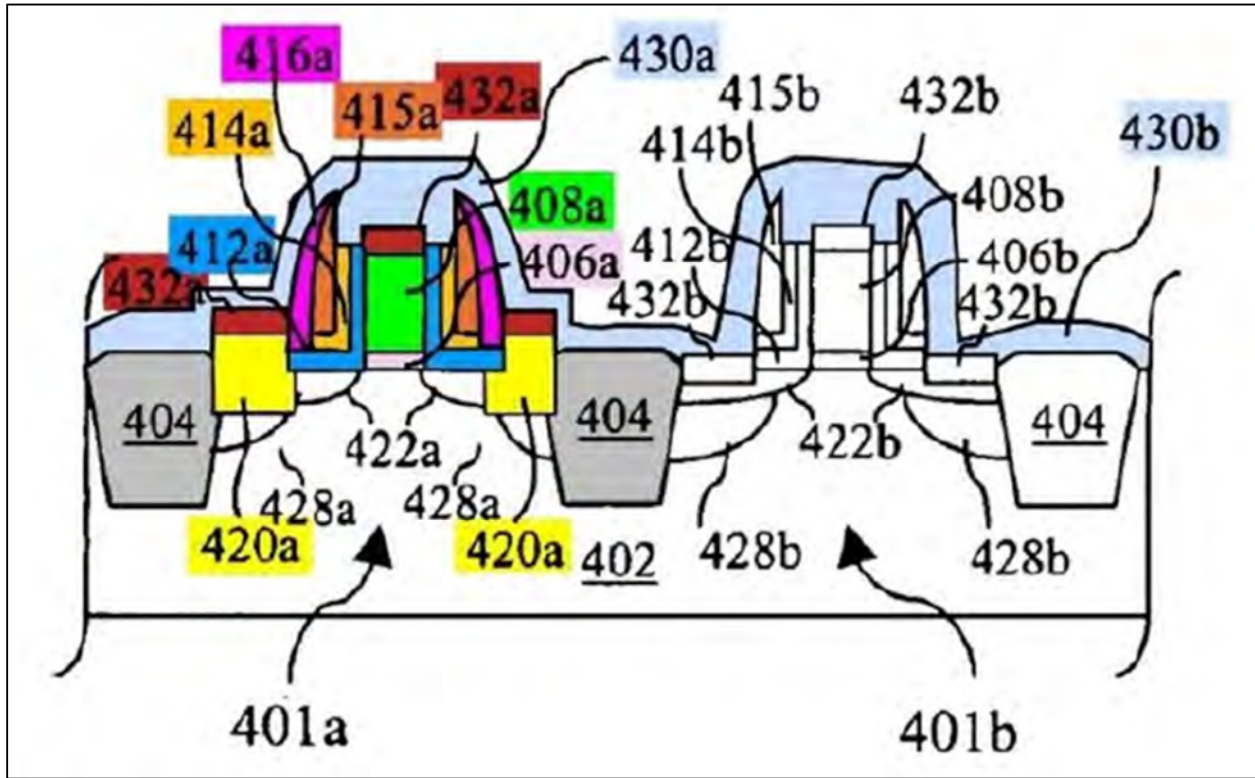


Figure I

259. Cheng817's SiGe source/drain region 420a induce a compressive stress along the gate length direction of the channel region of the pFET 401a. Cheng817, Ex.1008, ¶[0065]; *See also* Section V.F above (strained SiGe background); Wang906, Ex.1009, ¶¶[0030]-[0032], FIG. 9; Thompson-2004, 1790-96; Sun-2007, Ex.1524, 2; Bohr, Ex.1527, ¶[0024], ¶[0026], ¶[0028], FIGS. 4, 6, 7; Miyashita, Ex.1435, ¶[0051]; Fukutome, Ex.1011, ¶[0110], FIGS. 5E-5G. As I detail in Section X.B, and shown in Figure I, a POSITA would have recognized that Cheng817's SiGe source/drain regions 420a (highlighted yellow above)—which are part of the pFET active region—are located laterally on the side of the first sidewall spacers

(layers 414a (highlighted light orange above) and 415a (highlighted dark orange above))

- g. Element 1[f]: “a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress,”**

260. Cheng817 discloses a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress. Cheng817 teaches “formed over the semiconductor device(s) 401a and 401b” a stress insulating film, such as tensile etch stop layer 430a/430b. Cheng817, Ex.1008, ¶[0070], Fig. 4j. As Fig. 4j shows, etch stop layer 430a/430b formed over the gate electrode 408a, the sidewall spacer layers 414a and 415a, and the raised SiGe source/drain regions 420a of Cheng817’s pFET 401a. Cheng817, Ex.1008, ¶[0070], Fig. 4j. Cheng817 further explains that the etch stop layer 430a/430b may be a tensile stress inducing silicon nitride film and that the “stress level . . . may range between about +0.001 and about +50 GPa for [a] tensile film.” Cheng817, Ex.1008, ¶[0070]. This tensile stress of the etch stop layer 430a/430b is opposite to the compressive stress caused by epitaxial SiGe layers 420a discussed above.

261. As annotated in Figure I, the tensile etch stop film 430a/430b (highlighted light blue below) is formed over the gate electrode 408a (highlighted

green below), first sidewall spacer layers 414a (highlight light orange below) and 415a (highlighted dark orange below), and source/drain regions 420a (highlighted yellow below) of Cheng817's pFET 401a. *See* Section X.B above.

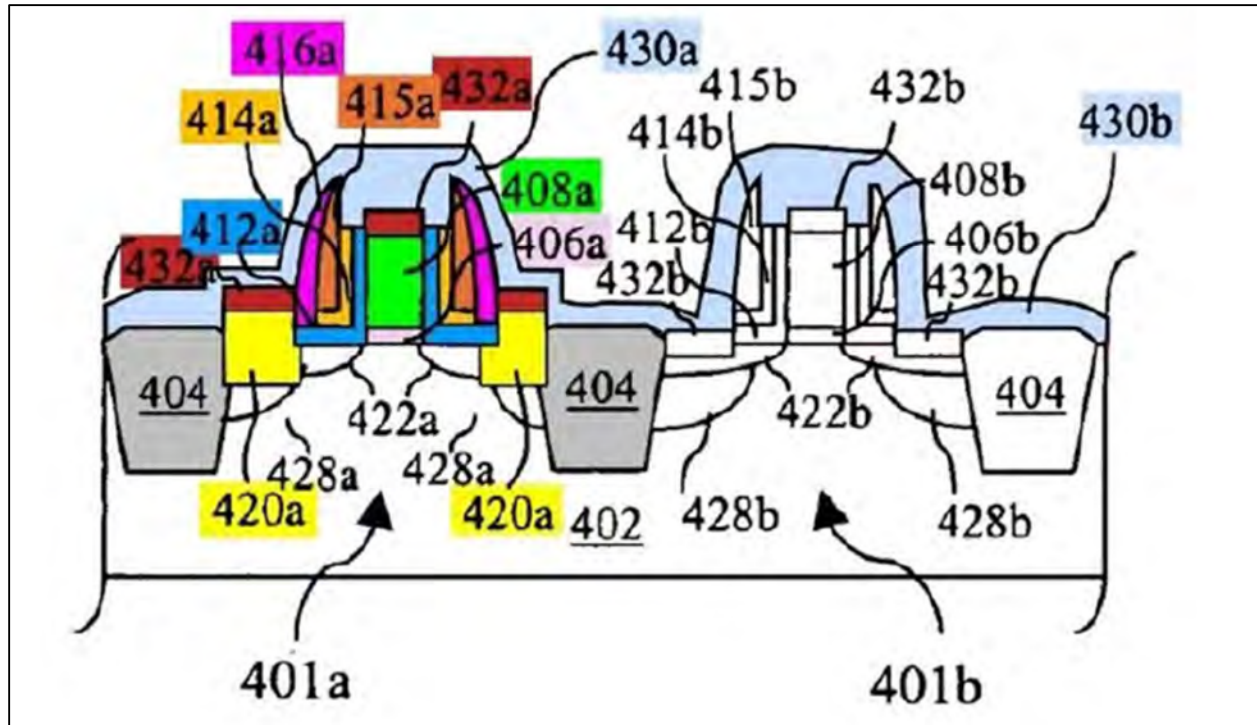


Figure I

262. Cheng817 expressly discloses that etch stop layer 430a/430b may be a tensile-stress inducing layer as discussed above. However, a POSITA would have also independently selected to make Chen's etch stop layer 430a/430b to impart tensile stress, which would cover both pFET 401a and nFET 401b, as Figure I shows above. *See* Cheng817, Ex.1008, Fig. 4j. It was well known in the prior art, before the invention of the '425 patent, that a tensile CESL improves electron mobility in nFETs without significantly impacting the beneficial compressive stress in pFETs

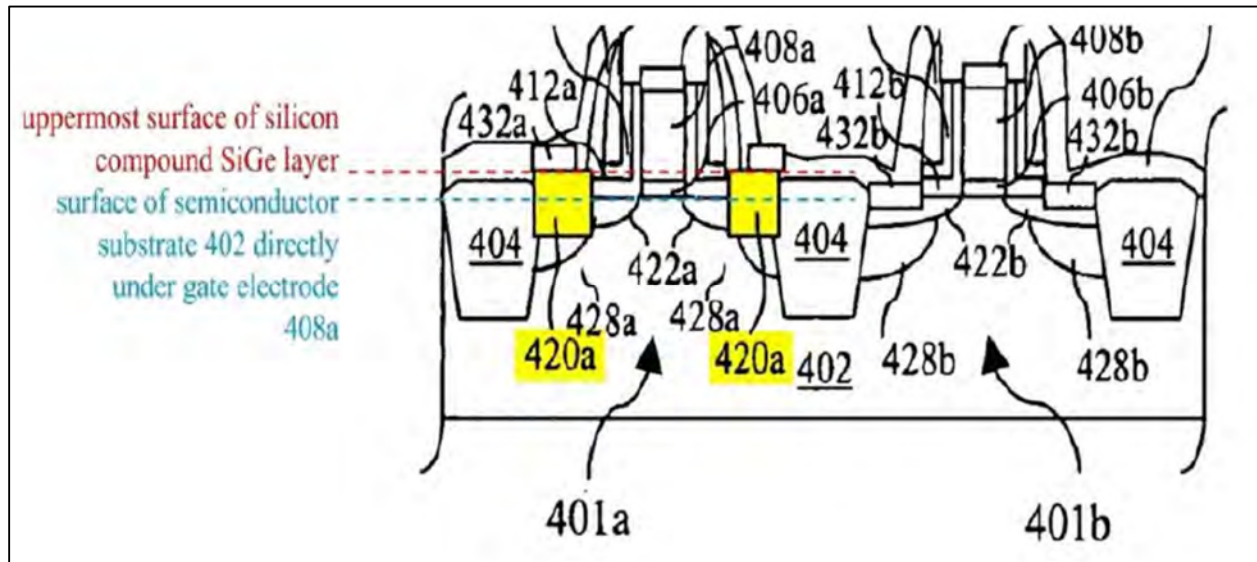
caused by epitaxial SiGe source/drain layers. *See* Sections V.F and V.G above; Hsu823, Ex.1506, ¶[0039] (preferable to apply tensile CESL across both NMOS and PMOS devices because “the performance of PMOS devices can be easily improved with SiGe stressors, while the performance of NMOS devices is relatively difficult to improve”); Morin-2007, Ex.1528, 355-56; Bohr, Ex.1527, ¶¶[0038]-[0039], FIG. 6.

h. Element 1[g]: “an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode,”

263. Cheng817 discloses or renders obvious an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode. Cheng817 teaches that “the source/drain regions 136 may extend above the substrate surface 106.” Cheng817, Ex.1008, ¶¶[0022], [0065]. In forming the device disclosed in Cheng817, the “recesses 144” in the substrate “may be filled to a height above the surface 106 of the substrate 104, such that the source/drain regions 136 may be raised source/drain regions.” Cheng817, Ex.1008, ¶¶[0022], [0065]. “The height of raised source/drain regions may range between about 5 nm and about 100 nm.” Cheng817, Ex.1008, ¶[0022].

264. Cheng817's Figs. 4e-4j similarly show the top of the source/drain regions 420a extend above the surface of the substrate 402. Cheng817, Ex.1008, ¶[0065], Figs. 4e-4j. A POSITA would have understood from reading Cheng817 that SiGe source/drain regions 420a of P-type MOS device 401a being "built-up" above the surface of the substrate describes the source/drains 420a being raised above the surface of the substrate 402. *See* Cheng817, Ex.1008, ¶[0054] (explaining that "a P-type MOS device[] comprises raised source and drain regions"), ¶[0065], Abstract, claims 1, 5,7, 8, 22-28, Figs. 4e-4j.

265. Annotated Cheng817's Fig. 4j below shows how Cheng817's raised SiGe source/drain region 420 (dashed red line) extend above the height of the surface of the substrate 402 under the gate electrode (dashed blue line). As can be seen, the top surface of raised SiGe source/drain region 420 is higher than the top surface of substrate 402, extending up above the bottom of the gate electrode (i.e., "built-up" over it).



Cheng817, Ex.1008 Fig. 4j (excerpt and annotated)

266. As I detail in Section X.B, a POSITA would recognize that Figure I below provides a more accurate representation of the pFET depicted in Cheng817's Fig. 4j. This aspect of Cheng817's pFET, as explicitly described in the text, would be understood to be retained throughout the process taught by Cheng817.

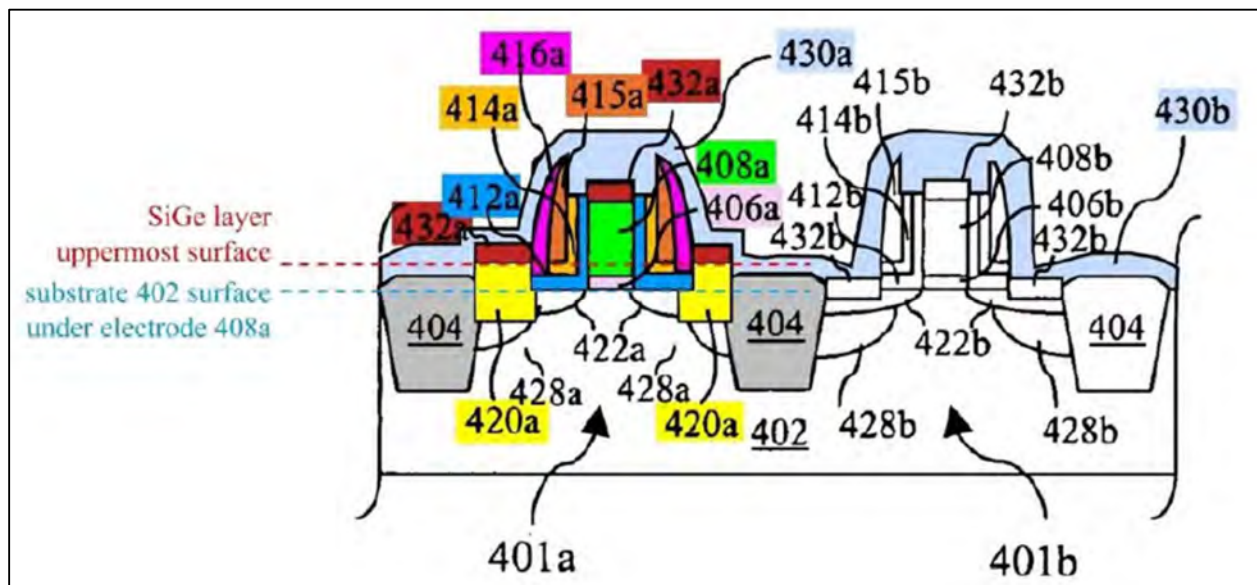


Figure I (further annotated)

i. Element 1[h]: “a first stress-relief is formed in a space between the silicon compound layer and the first sidewall spacer,”

267. Cheng817 discloses that a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer. Cheng817 details that “dummy spacers 416a,” formed of “silicon dioxide (SiO₂),” and are formed in between the raised SiGe source/drain regions 420a and the sidewall spacers 414a/415a. Cheng817, Ex.1008, ¶[0063]. As explained in Section X.B, a POSITA reading Cheng817 would have found it obvious that by forming SiGe source/drain regions 420a (highlighted yellow), which are raised to a height above bottom of the gate dielectric 406a (highlighted light purple), the SiGe source/drain regions 420a grow around and next to the dummy spacer 416a (highlighted magenta). *See* Section X.B above and Figure I below.

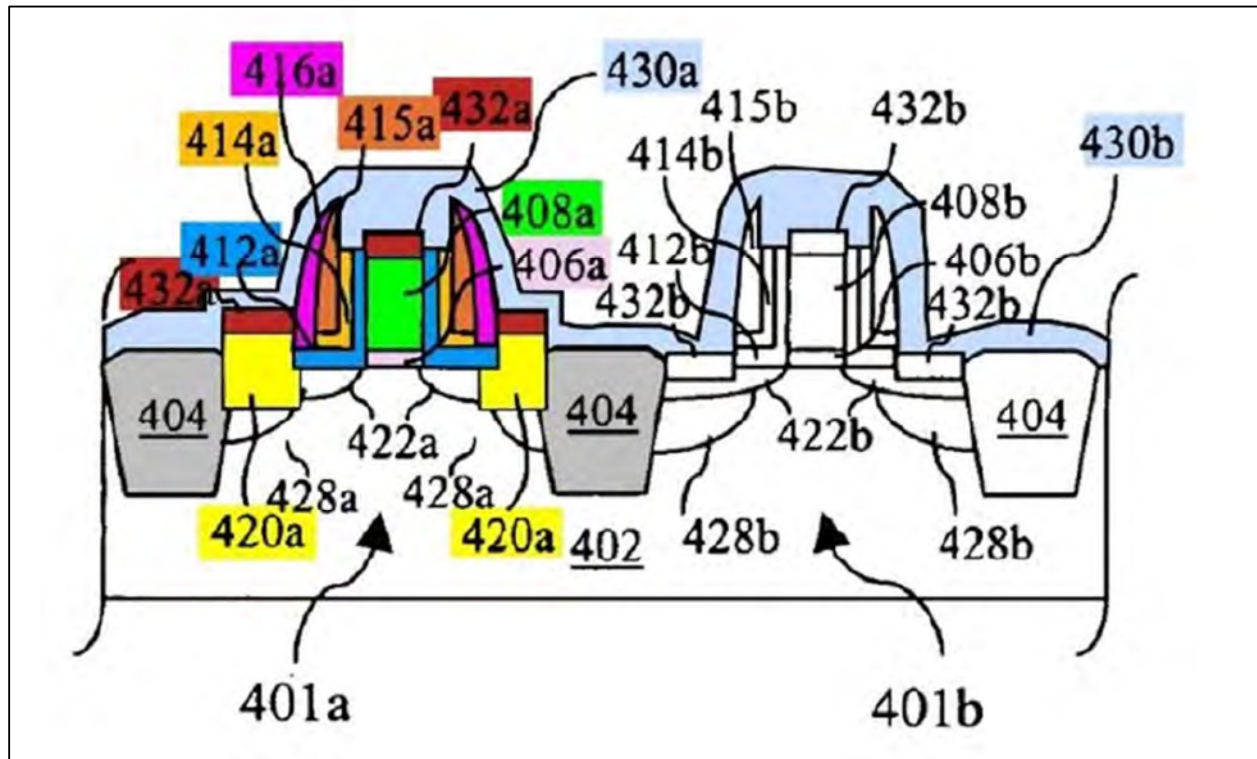


Figure I

268. This mirrors the description of the stress-relief film of the '425 patent. The '425 patent describes that the “first stress-relief film 28a is formed in the space 24 between the silicon compound layer 23 and the first sidewall 19A.” The '425 patent, Ex.1001, 14:51-54. Like the '425 patent's stress-relief film 28a made of silicon oxide, Cheng817's dummy spacer 416a is also made of silicon oxide. *See* The '425 patent, Ex.1001, 12:59-62; Cheng817, Ex.1008, ¶[0063].

269. As seen above in Figure I, Cheng817's dummy spacer 416a (first stress-relief film, highlighted magenta) is formed in a space between SiGe silicon compound layer 420a (highlighted yellow) and the first sidewall spacer (comprising both the

layers highlighted light and dark orange, 414a and 415a respectively) of pFET 401a.
See Section X.B above.

j. Element 1[i]: “the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween, and”

270. Cheng817 discloses that the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween. As discussed for element [1H], Cheng817’s Fig. 4j shows that dummy spacers 416a are formed on laterally on the side surfaces of gate electrode 408a with the first sidewall spacer (sidewall layers 414a and 415a, collectively) located between the dummy spacer and the gate electrode. As explained in Section X.B, it is my opinion that a POSITA would have understood from Cheng817’s disclosures, either alone or in combination of Wang906, that Figure I represents a more accurate description of the device formed from Cheng817’s disclose than Cheng817’s Fig. 4j. As Figure I shows below, Cheng817’s stress-relief film (dummy spacer 416a, highlighted magenta) is formed on the side surface of gate electrode 408a (highlighted green) with the first sidewall spacer (highlighted light and dark orange layers 414a and 415a) formed between the dummy spacer and the gate electrode. *See* Section X.B above.

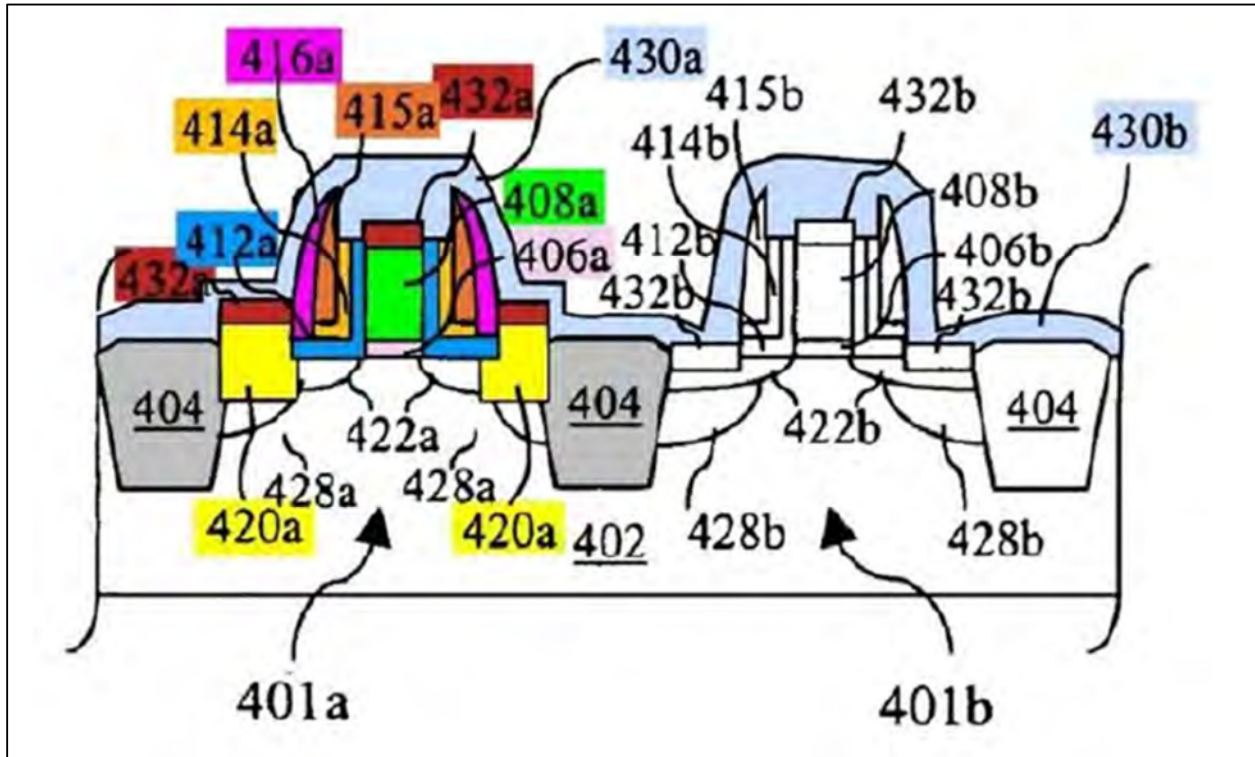


Figure I

- k. **Element 1[j]: “the first stress-relief film is not in direct contact with the side surface of the first gate electrode.”**

271. Cheng817 discloses that the first stress-relief film is not in direct contact with the side surface of the first gate electrode. As discussed for claim elements [1H] and [1I], Cheng817’s Fig. 4j shows that dummy spacers 416a are not in direct contact with the gate electrode 408a because the first sidewall spacer (sidewall dielectric structure 414a and spacer 415a, collectively) is interposed between them. As I explain above in Section X.B, a POSITA would have understood from Cheng817’s disclosures, either alone or in view of Wang906, that Figure I below represents a more accurate description of Cheng817’s pFET than Cheng817’s Fig. 4j.

As Figure I shows below, Cheng817's stress-relief film (dummy spacer 416a, highlighted magenta) does not come in directly contact with the side surface of the gate electrode 408a (highlighted green) because the first sidewall spacer (highlighted light and dark orange layers 414a and 415a) lies between them. *See* Section X.B above.

2. Dependent Claim 3

- a. **Claim 3 “the semiconductor device of claim 1, further comprising: a first silicide layer formed on the first gate electrode; and a second silicide layer formed on the first source/drain region which includes the silicon compound layer.”**

272. It is my opinion that Cheng817 renders claim 3 obvious. First, Cheng817 renders the semiconductor of Claim 1 obvious for the same reason explained in Sections X.B.1.a-k above.

273. Cheng817 also makes it obvious to form a first silicide layer on the first gate electrode and a second silicide layer on the first source/drain region, which includes the silicon compound layer. Cheng817 teaches “salicided⁷ contacts 432a . . . are formed over the gate [408a]” and the “source and drain [420a].” Cheng817, Ex.1008, ¶[0069]; *see also* Cheng817, Ex.1008, Figs. 4i, 4j. Cheng817 explains that “salicided contacts 432a and 432b may include the formation of a metal silicide such as . . . nickel silicide” or others. Cheng817, Ex.1008, ¶[0069], Figs. 4i, 4j. As I

⁷ “Salicide” means a self-aligned silicide layer.

previously explained regarding claim 1, Cheng817's pFET gate 408a corresponds to the first gate electrode, and the claimed source and drain region corresponds to the epitaxial SiGe layer 420a. *See* Sections X.B.1.d. and X.B.1.f above.

274. As described in Section X.B., a POSITA would understand from Cheng817's disclosures, whether considered alone or alongside Wang906's similar disclosures, that Figure I provides a more accurate representation of Cheng817's pFET than Cheng817's Fig. 4j. As seen in Figure I, a first silicide layer 432a (highlighted red) is formed on the first gate electrode 408a (highlighted green), and a second silicide layer 432a (highlighted red) is formed on the epitaxial SiGe source/drain regions 420a (highlighted yellow). *See* Section X.B.1 above; Cheng817, Ex.1008, Fig. 4j.

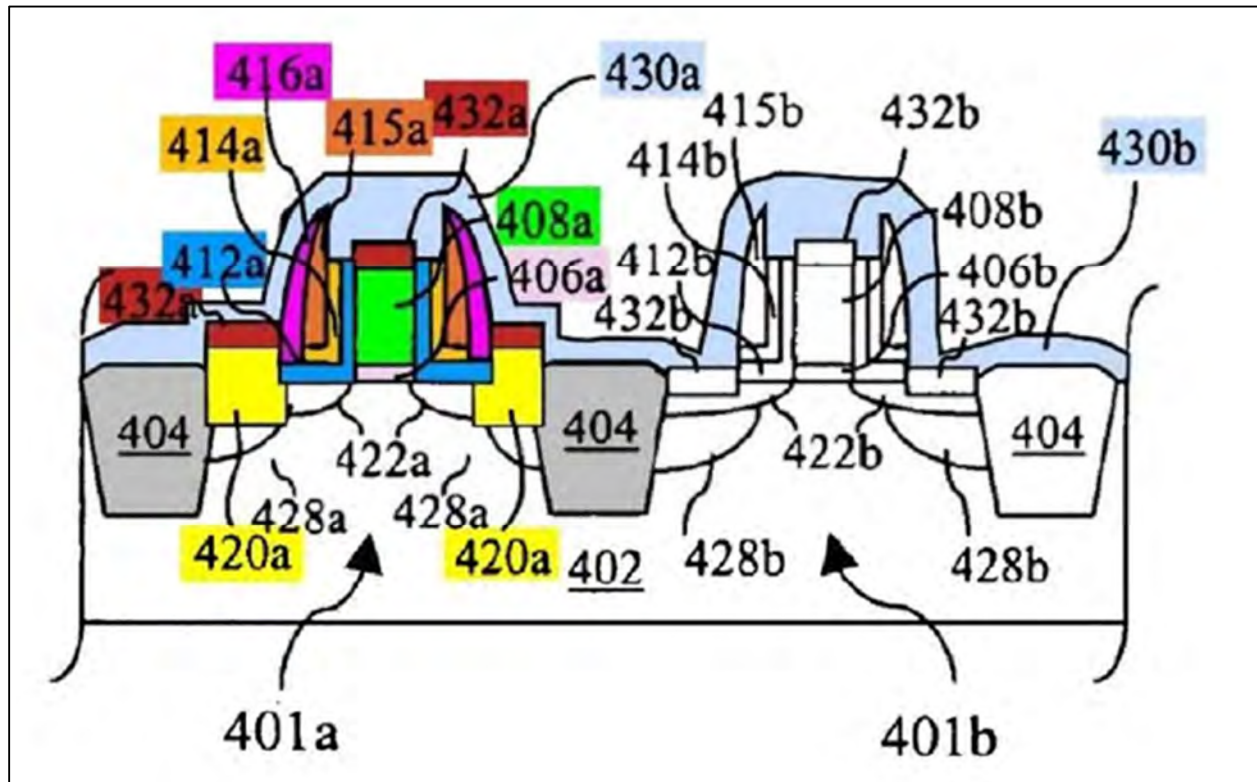


Figure I

3. Dependent Claim 4

- a. **Claim 4:** “The semiconductor device of claim 1, wherein the first stress-relief film is formed on a side surface of the silicon compound layer.”

275. It is my opinion that Cheng817 renders claim 4 obvious. First, Cheng817 renders the semiconductor of Claim 1 obvious for the same reason explained in Sections X.B.1.a-k above.

276. Cheng817 further discloses that the first stress-relief film being formed on a side surface of the silicon compound layer. As I discussed for claim elements [1H]-[1J] and in Section X.B.1.i-k, Cheng817’s dummy spacer 416a (stress-relief

film) is formed on a side surface of the epitaxial SiGe source/drain regions 420a (silicon compound layer). Cheng817, Ex.1008, Fig. 4j; *See also* Sections X.B and X.B.1.i-k above. A POSITA would have therefore understood that Cheng817's SiGe layer would grow up above the surface of the semiconductor substrate and alongside the sidewall structure and dummy spacer 416a, as Figure I shows below. *See* Section X.B. above; Cheng817, Ex.1008, ¶¶[0022], [0065], Fig. 4e; Wang906, Ex.1009, ¶¶[0030]-[0032], FIG. 9.

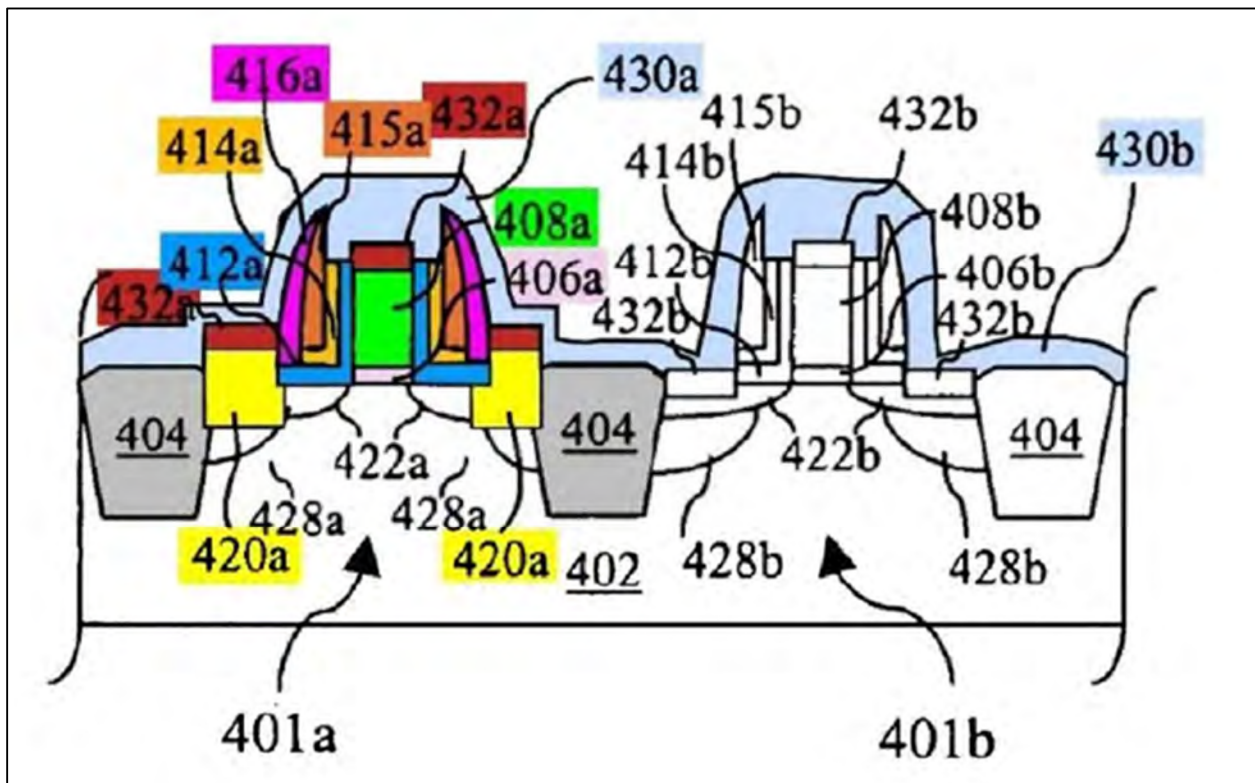


Figure I

277. A POSITA would have understood from Cheng817's textual disclosures, either alone or taken together with the disclosures of Wang906, that

Figure I provides a more accurate representation of Cheng817's pFET than Cheng817's Fig. 4j, as further discussed in Section X.B. Again, as Figure I shows above, Cheng817's stress-relief film (dummy spacer 416a, highlighted above in magenta) is next to a side surface of Cheng817's raised silicon compound layer (epitaxial SiGe source/drain layer 420a, highlighted above in yellow) as the SiGe layer (highlighted yellow) is formed such that it raises above the silicon substrate and forms adjacent to the dummy spacers 416a (highlighted magenta). *See* Section X.B above.

4. Dependent Claim 7

a. Preamble: "The semiconductor device of claim 1,"

278. It is my opinion that Cheng817 renders claim 7 obvious. First, Cheng817 renders the semiconductor of Claim 1 obvious for the same reason explained in Sections X.B.1.a-k above.

b. Element 7[a]: "wherein the first MIS transistor is a p-type MIS transistor,"

279. Cheng817 discloses that the first MIS transistor is a p-type MIS transistor. As I detail above in Section X.B.1.b, Cheng817 teaches "semiconductor device 401a may be a P-type MOS device," i.e., a p-type MIS transistor. Cheng817, Ex.1008, ¶[0056].

c. Element 7[b]: “the first stress is a compressive stress, and”

280. Cheng817 discloses the first stress is a compressive stress. As I explain for claim 1 above, Cheng817’s raised SiGe source/drain regions 420a cause a compressive stress “increasing the compressive stress in the substrate can improve the performance of p-channel metal-oxide-semiconductor (PMOS) devices.” Cheng817, Ex.1008, ¶[0002]. This stress is “first” because there is a “second” stress detailed below in Element 7[c]. Cheng817, Ex.1008, ¶[0002]; *See also* Sections V.F, X.B, and X.B.1 above.

d. Element 7[c]: “the second stress is a tensile stress.”

281. Cheng817 discloses that the second stress is a tensile stress. Again, as I explain for claim 1 above, Cheng817’s etch stop layer 430a/430b causes a tensile stress and it is “second” because the “first” is the compressive stress causes by the SiGe source/drain region. Cheng817, Ex.1008, ¶[0070]; *See* Sections V.F, X.B, and X.B.1 above.

5. Dependent Claim 8

a. Preamble: “The semiconductor device of claim 1,”

282. It is my opinion that Cheng817 renders claim 8 obvious. First, Cheng817 renders the semiconductor of Claim 1 obvious for the same reason explained in Sections X.B.1.a-k above.

b. Element 8[a]: “wherein the silicon compound layer is a SiGe layer,”

283. Cheng817 discloses that the silicon compound layer is a SiGe layer. As I detailed above in Section X.B.1.f, The silicon compound layer taught in Cheng817’s includes epitaxial source/drain layer 420a, which comprises “silicon germanium” or “SiGe.” Cheng817, Ex.1008, ¶[0065].

c. Element 8[b]: “the stress insulating film is a silicon nitride film, and”

284. Cheng817 discloses that the stress insulating film is a silicon nitride film. For the same reasons I explained in Section X.B.1.g, Cheng817’s “etch stop layer 430a and 430b may include silicon nitride (Si_xN_y).” Cheng817, Ex.1008, ¶[0070].

d. Element 8[c]: “the first stress-relief film is a silicon oxide film.”

285. Cheng817 discloses that the first stress-relief film is a silicon oxide film. For the same reasons I explained in Sections X.B.1.i-k, Cheng817’s “dummy spacer material 416,” which corresponds to the stress-relief film claimed, “may include silicon dioxide (SiO_2).” Cheng817, Ex.1008, ¶[0063].

6. Dependent Claim 11

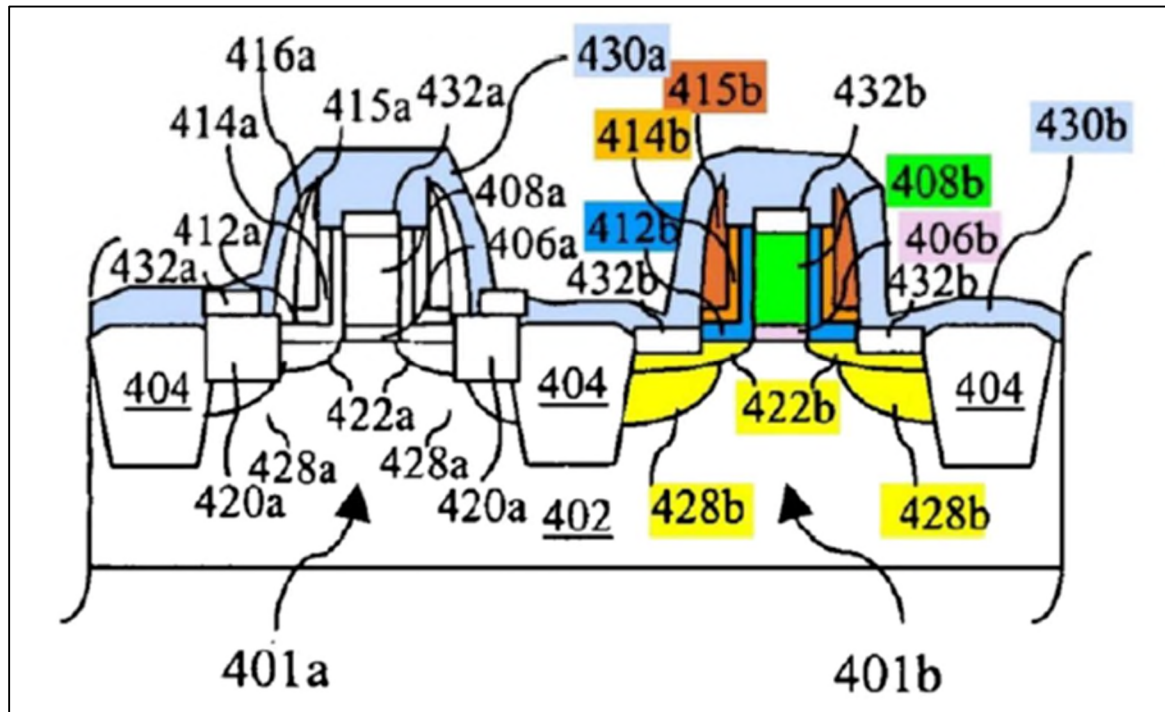
a. Preamble: “The semiconductor device of claim 1, further comprising:”

286. It is my opinion that Cheng817 renders Claim 11 obvious. First, Cheng817 renders the semiconductor of Claim 1 obvious for the same reason explained in Sections X.B.1.a-k above.

287. However, note that for Claim 11, Cheng817’s NMOS 401b in Fig. 4j does not include the same rendering errors as pFET 401a I discussed in Section X.B. Accordingly, because nFET 401b is shown as the same in Fig. 4j and Figure I, the discussion below is applicable to both scenarios.

b. Element 11[a]: “a second MIS transistor, wherein:”

288. Cheng817 discloses a second MIS transistor. Cheng817 states that “semiconductor device 401b may be an N-type MOS device,” i.e., an nFET. Cheng817, Ex.1008, ¶[0056]; *see also* Cheng817, Ex.1008, Fig. 4j.



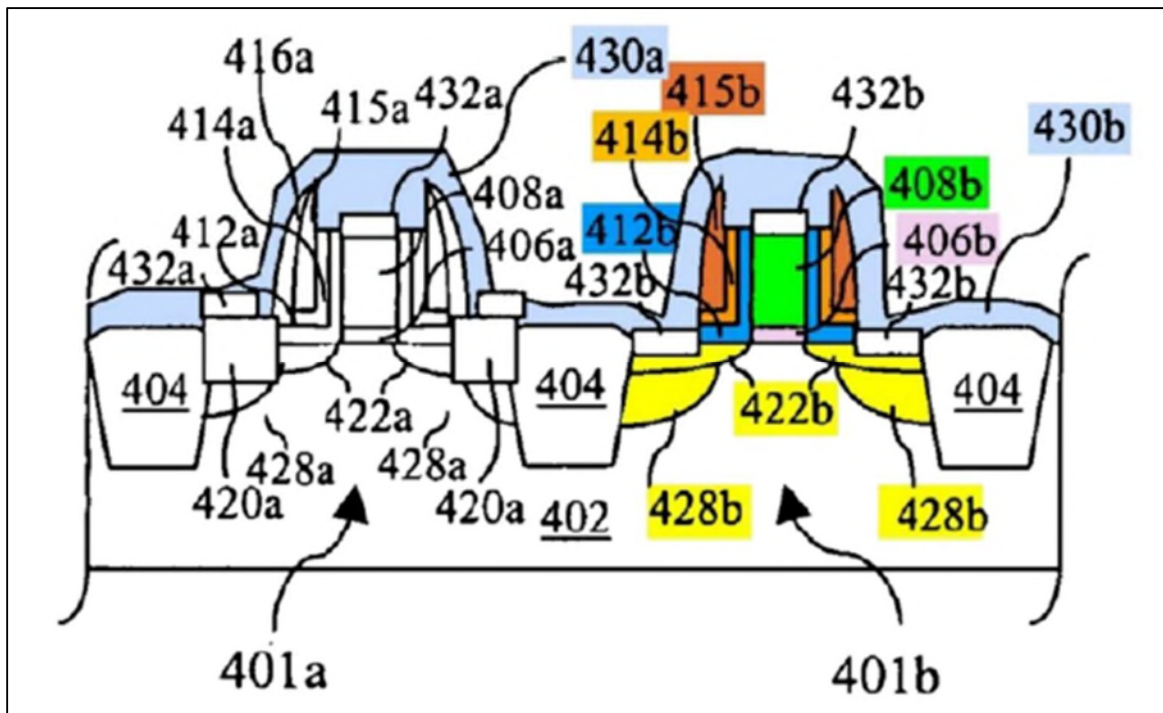
Cheng817, Ex.1008 Fig. 4j (annotated)

- c. **Element 11[b]: “the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate,”**

289. Cheng817 discloses a second gate insulating film formed on a second active region in the semiconductor substrate. Cheng817 teaches an nFET “gate dielectric . . . 406b” being “formed over a substrate 402.” Cheng817, Ex.1008, ¶[0056]; *See also* Cheng817, Ex.1008, Figs. 4a-4j. Like in Claim 1, Cheng817’s gate dielectric layer 406b corresponds to a second gate insulating film because it is made of insulating materials like “silicon oxide” or “SiO₂” (i.e., silicon dioxide), which is also the same material from ’425 patent’s disclosure. Cheng817, Ex.1008, ¶[0058]; The ’425 patent, Ex.1001, 9:15-19.

290. Again, like discussed in Claim 1, where the dielectric 406b is formed, Cheng817's substrate 402 has an active region. As expected, the nFET active region is described as having "lightly doped regions . . . 422b" having "N-type dopants" and "heavily doped regions 428b." Cheng817, Ex.1008, ¶¶[0056], [0060], [0065]-[0068], Fig. 4j.

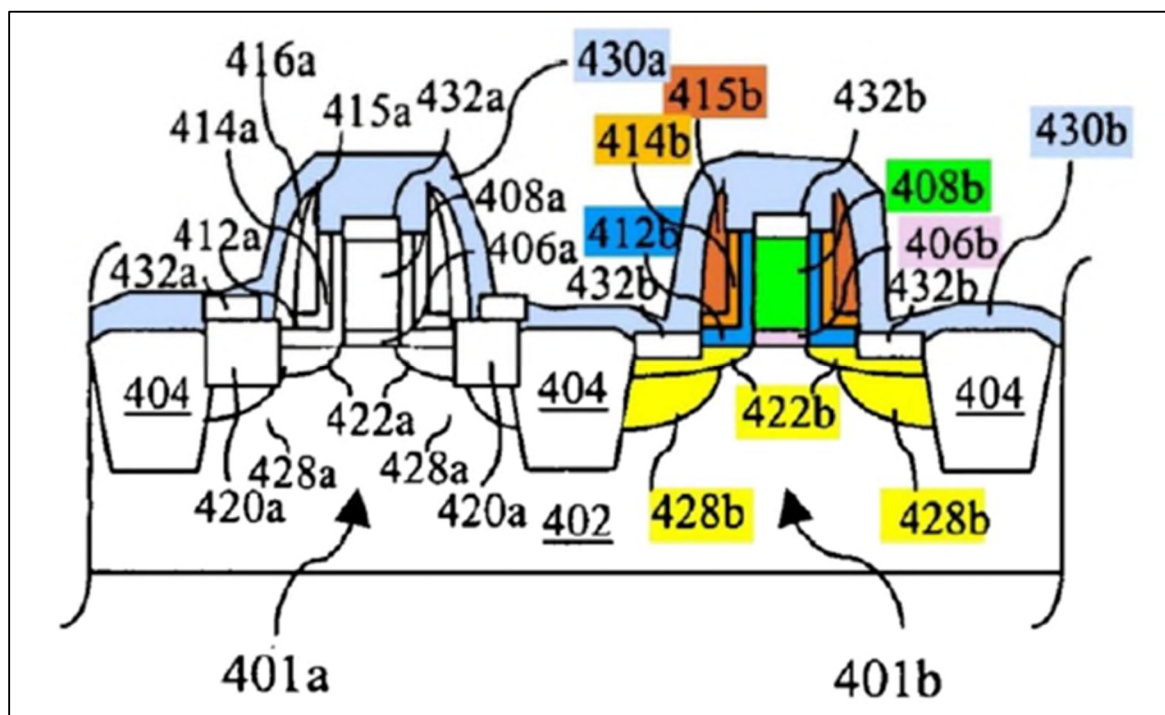
291. In the annotated Fig. 4j below, nFET 401b is the second MISFET transistor. Cheng817's gate insulating film 406b (highlighted light purple) of nFET 401b is formed on the "active region" located between two lightly doped regions 422b. It is well known this portion is the channel region, which, by definition, and as known in the prior art, is part of the "active region" of nFET 401b.



Cheng817, Ex.1008 Fig. 4j (annotated)

d. Element 11[c]: “a second gate electrode formed on a second gate insulating film,”

292. Cheng817 discloses a second gate electrode formed on the second gate insulating film. Specifically, Cheng817 teaches that “[g]ate electrode [] . . . 408b [is] formed over the gate dielectric layer [406b].” Cheng817, Ex.1008, ¶[0056]. As illustrated below, the second gate electrode 408b (highlighted green) is formed on top of the second gate dielectric 406b (highlighted light purple).



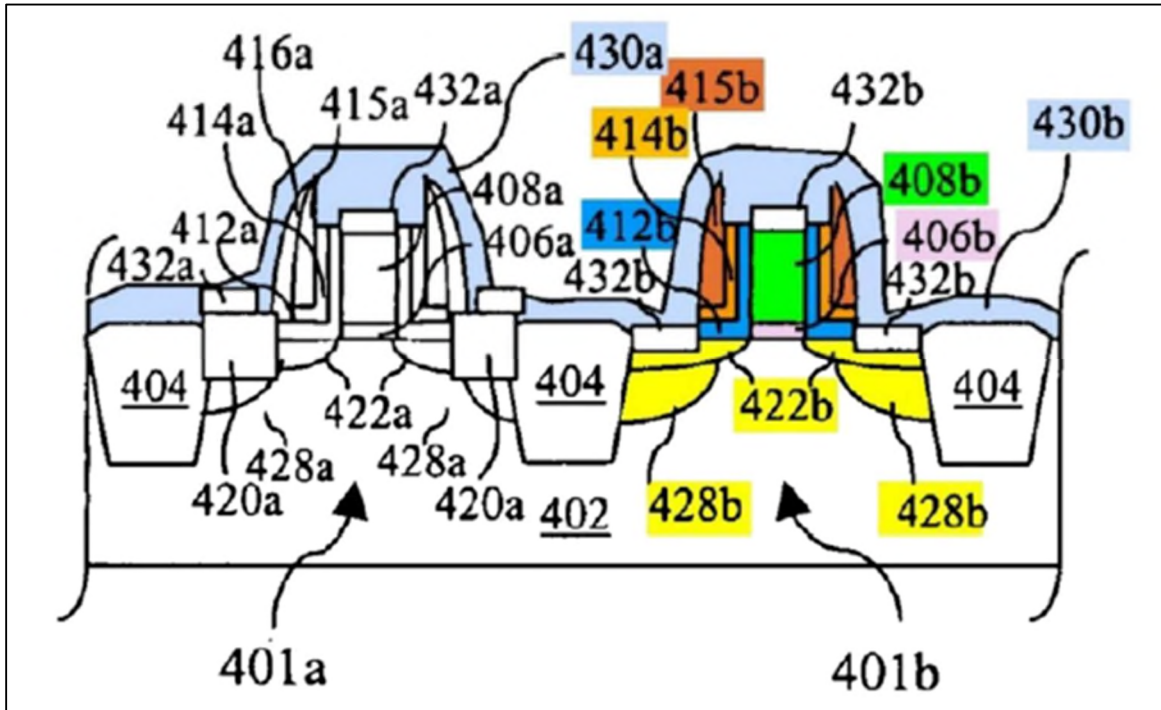
Cheng817, Ex.1008 Fig. 4j (annotated)

e. Element 11[d]: “a second sidewall spacer formed on a side surface of the second gate electrode.”

293. Cheng817 discloses a second sidewall spacer formed on a side surface of the second gate electrode. Cheng817 teaches a second sidewall spacer: “sidewall

dielectric layer [] . . . 414[] and spacer material 415 . . . disposed over the semiconductor device[] . . . 401b” (nFET). Cheng817, Ex.1008, ¶[0061]. As I explain previously for claim 1 in Section X.B.1.e, Cheng817 subsequently teaches “etching” layers 414 and 415 to form “sidewall dielectric structures . . . 414b, and spacers . . . 415b, as shown in FIG. 4c.” Cheng817, Ex.1008, ¶[0061]. As seen in Cheng817 Figs. 4c and 4j, the second sidewall spacer (collectively, dielectric structure 414b and spacer 415b) is formed on a side surface of gate electrode 408b because, like described in the ’425 patent, they are formed laterally on the sides of the second gate electrode. *See* Cheng817, Ex.1008, ¶[0061], Figs. 4c, 4j; The ’425 patent, Ex.1001, FIG. 6B (transistor NTr, sidewall 19B).

294. Cheng817 accordingly discloses that the second sidewall spacer (sidewall dielectric structure 414b (highlighted light orange) and spacer 415b (highlighted dark orange), collectively) is formed on the sides of gate electrode 408b (highlighted green) in Cheng817’s nFET 401b, as illustrated below in Fig. 4j below.



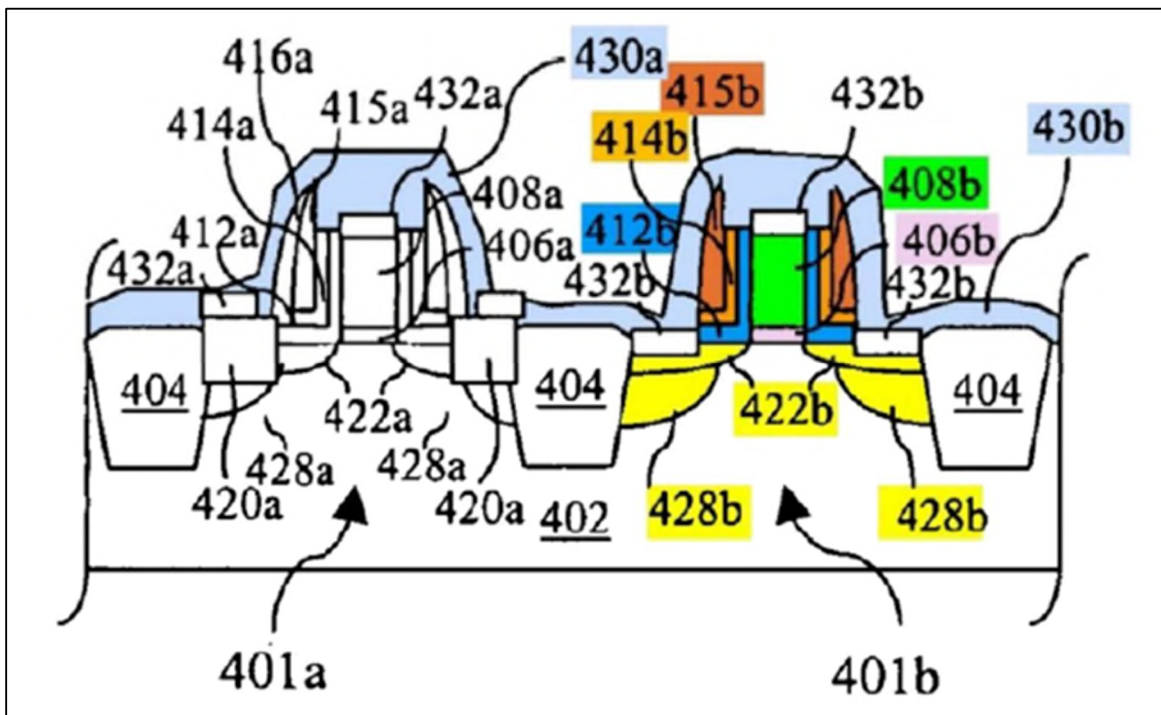
Cheng817, Ex.1008 Fig. 4j (annotated)

- f. **Element 11[e]: “a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer, and”**

295. Cheng817 discloses a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer. Cheng817 discloses that “N-type MOS device” 401b includes “lightly doped regions . . . 422b [that] may include . . . N-type dopants for the device [] . . . 401b.” Cheng817, Ex.1008, ¶[0060]. N-type MOS device 401b also includes “heavily doped regions 428b” that “include N-type impurities.” Cheng817, Ex.1008, ¶[0066]. Implanted source drain regions are well known to include the lightly doped regions 422b and heavily doped regions 428b. Additionally the second

conductivity type is of “N-type” whereas the first conductivity type of claim 1 is “P-type.” See Cheng817, Ex.1008, ¶[0060]; Section X.B.1.f above.

296. As Cheng817’s Fig. 4j shows below, source/drain regions 422b and 428b (highlighted yellow)—a part of the nFET active region—are formed on the side of the second sidewall spacers (layers 414b (highlighted light orange) and 415b (highlighted dark orange)). See Cheng817, Ex.1008, Fig. 4j.



Cheng817, Ex.1008 Fig. 4j (annotated)

- g. **Element 11[f]: “the stress insulating film formed on the second active region to cover the second gate electrode, the second sidewall spacer, and the second source/drain region.”**

297. Cheng817 discloses that the stress insulating film is formed on the second active region to cover the second gate electrode, the second sidewall spacer,

and the second source/drain region. Specifically, Cheng817 discloses that the tensile etch stop layer 430a/430b is “formed over the semiconductor device [] . . . 401b,” which, as discussed in Section X.B.1.g corresponds to the stress insulating film. Cheng817, Ex.1008, ¶[0070], Fig. 4j.

298. As Fig. 4j shows above, Cheng817’s etch stop layer 430a/430b (highlighted light blue) over the gate electrode 408b (highlighted green), sidewall spacer (collectively, layers 414b (highlighted light orange) and 415b (highlighted dark orange)), and the source/drain regions 422b and 428b (highlighted yellow) of Cheng817’s nFET 401b. Cheng817, Ex.1008, ¶[0070], Fig. 4j.

7. Ground 2A – Cheng817 and Wang906

299. In response to the possibility that the Patent Owner may contend Cheng817 alone does not make claims 1, 3,4, 7, 8, and 11 obvious based solely on the textual descriptions of Cheng817 and Cheng817 Figs. 4a-4j, I have been asked to consider Cheng817 and Wang906 combination. While I disagree the Cheng817-Wang906 combination is necessary for the reasons outlined in Section X.B, I still believe that a POSITA would find these claims obvious when considering Cheng817 in view of Wang906. This opinion is supported by the explanations provided in Sections X.B through X.B.6, as well as the well-known and accepted benefits of employing raised epitaxial SiGe stressors, as I discussed in Section V.F. Incorporating Wang906 with Cheng817 does not change my previous invalidity

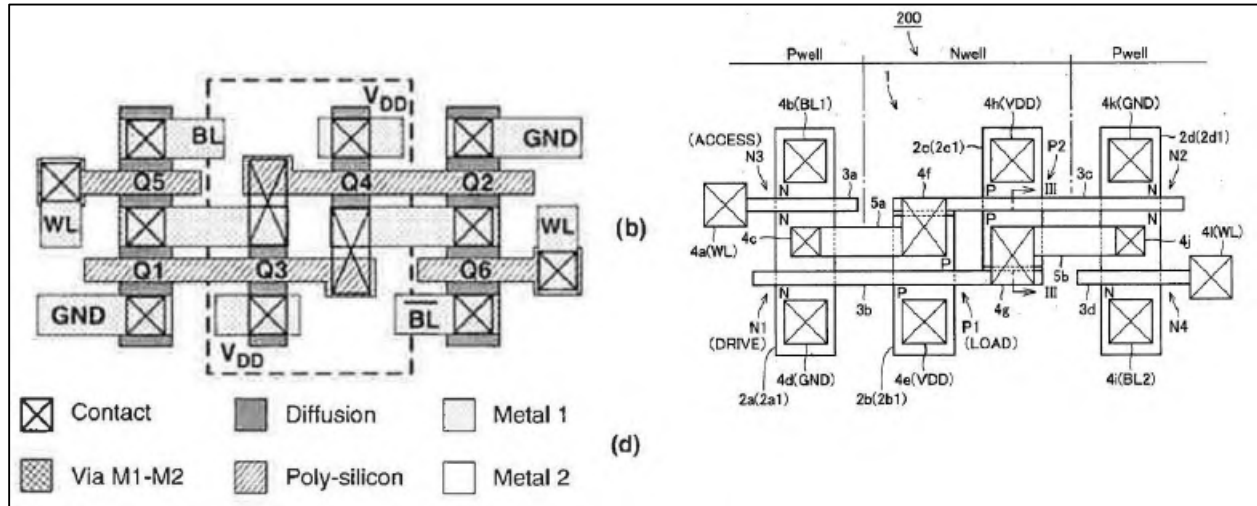
analysis of Claims 1, 3, 4, 7, 8, and 11; Wang906 merely reinforces the obviousness of the structure presented in Figure I.

C. Ground 3

1. Motivation to Combine Saito825, Fukutome, and James to Render Claims 1, 3, 4, 7, and 8 Obvious

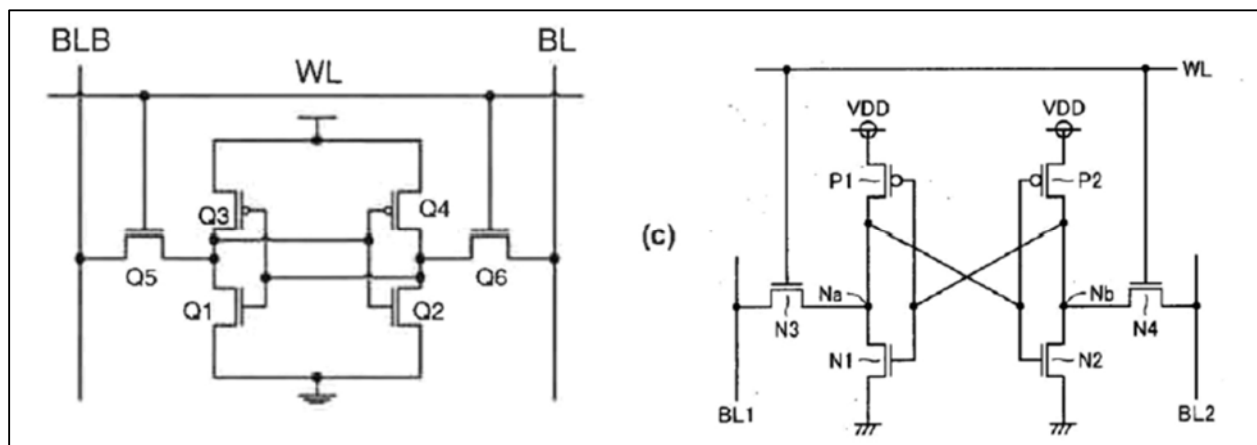
300. It is my opinion that the combination of Saito825, Fukutome, and James renders claims 1, 3, 4, 7 and 8 obvious.

301. Saito825 describes a standard Static random-access memory (SRAM) cell. *See* Saito825, Ex.1010, ¶¶[0003]-[0005], ¶¶[0049]-[0050], FIGS. 1-2; Pavlov-2008, Ex.1446, 24-25, Figs. 2.10(b)-(d); Matsui832, Ex.1447, ¶[0055], FIGS. 1-3; Ishida-1998, Ex.1448, Tbl. 1; Balobas-2015, Ex.1449, 1, Fig. 1; Thompson498, Ex.1450 ¶¶[0063]-[0065], FIGS. 39-40B. Namely, Saito825 describes a well-known 6T (6 transistor) SRAM cell. Pavlov-2008, Ex.1446, 24-25, Figs. 2.10(b)-(d). This is supported in the prior art, for example a textbook entitled “CMOS SRAM: Circuit Design and Parametric Test in Nano-Scaled Technologies” describes the same standard SRAM structure. *Compare* Pavlov-2008, Ex.1446, 24-25, Figs. 2.10(b)-(d), *with* Saito825, Ex.1010, ¶¶[0028]-[0029], FIGS. 1-2.



Pavlov-2008, Ex.1446, Figs. 2.10(b),(d)

Saito825, Ex.1010, FIG. 1

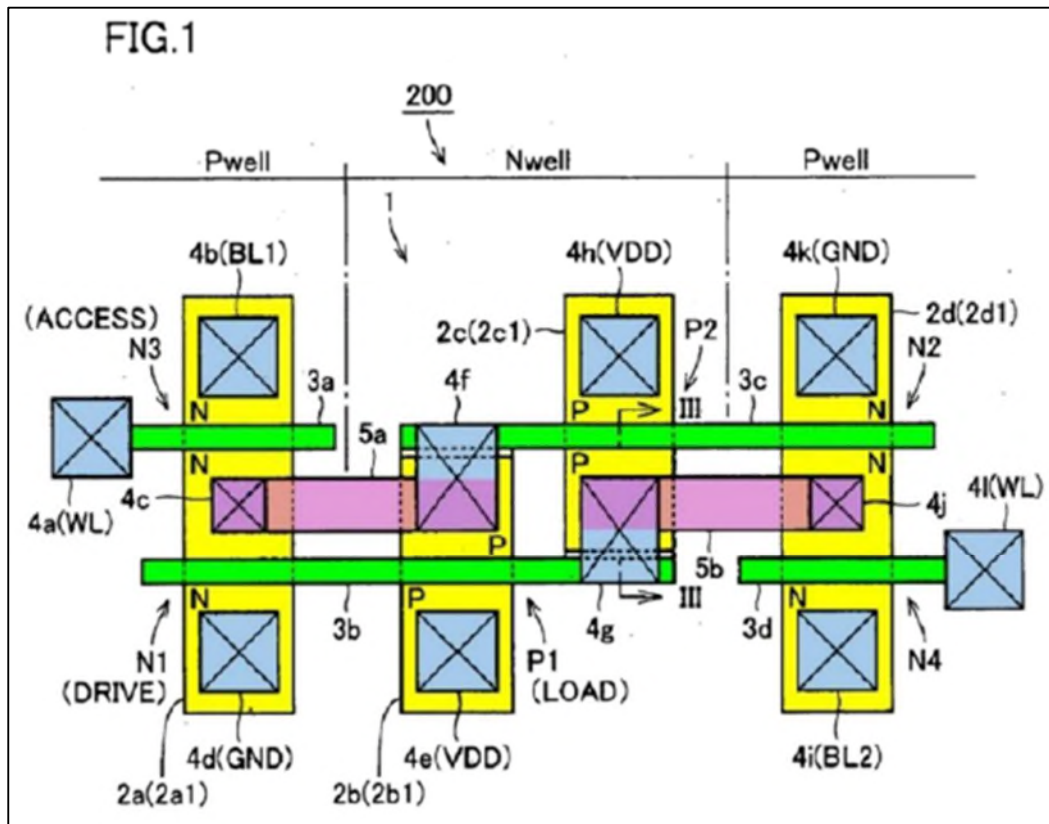


Pavlov-2008, Ex.1446, Fig. 2.10(c)

Saito825, Ex.1010, FIG. 2

302. Just as a POSITA would have expected of a standard SRAM cell, Saito825 discloses five traditional SRAM layers, with each layer sharing similar numbers (see above). Item numbers beginning with 2x correspond to one layer, while those starting with 3x represent another, and this pattern continues. Below is a list detailing each layer, including the color in which they are depicted in the annotated FIG. 1:

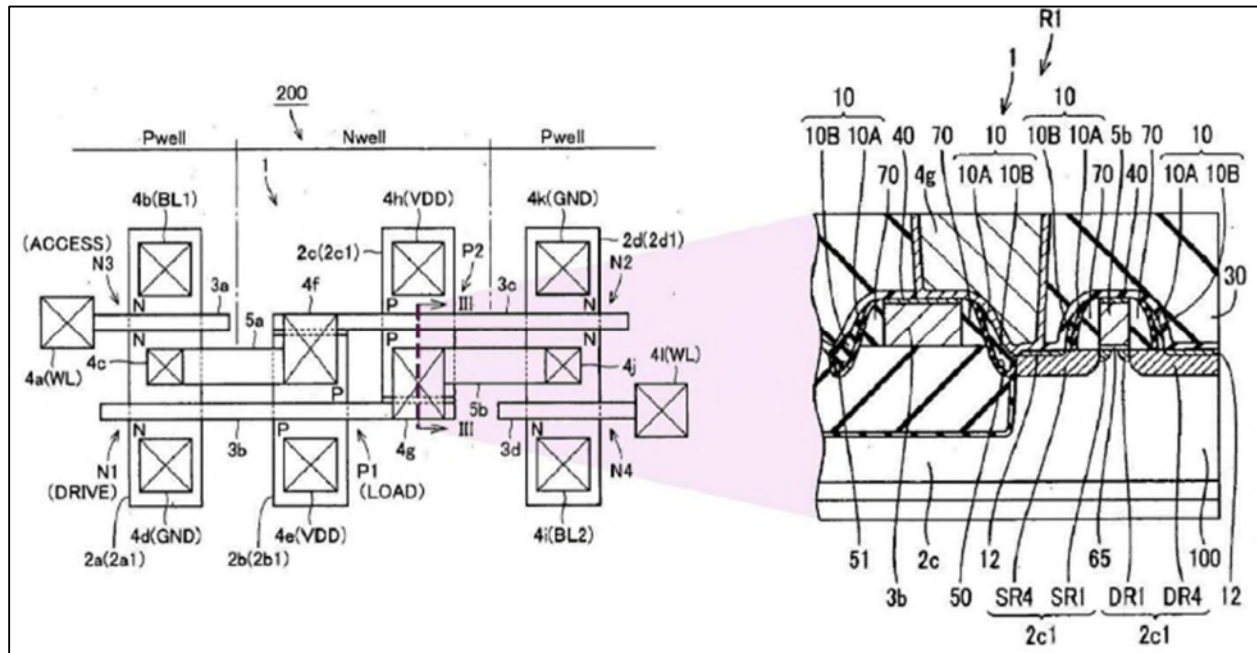
- Substrate layer: 100 (uncolored). *See* Saito825, Ex.1010, ¶[0072].
- Active regions and source/drains: 2a-2d (yellow). *See* Saito825, Ex.1010, ¶¶[0060]-[0061].
- Polysilicon wirings: 3a-3d (green). *See* Saito825, Ex.1010, ¶¶[0067]-[0068], ¶[0124].
- Contact parts: 4a-4l (blue). *See* Saito825, Ex.1010, ¶¶[0068]-[0069].
- Metal wirings: 5a-5b (purple). *See* Saito825, Ex.1010, ¶¶[0070]-[0071].



Saito825, Ex.1010, FIG. 1 (annotated)

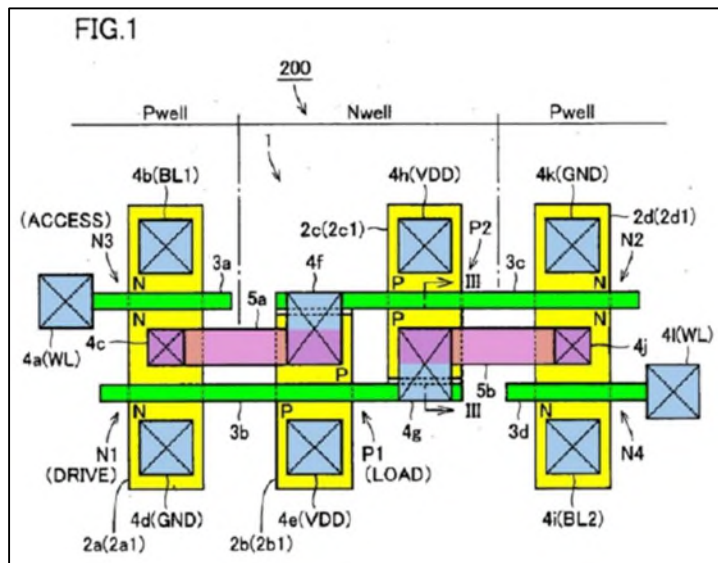
303. In Saito825, the “[p]olysilicon wirings 3a-3d constitute a gate of each MOS transistor.” Saito825, Ex.1010, ¶[0067]. “[C]ontact parts 4a-4l” provide a connection with an “upper wiring” layer. Saito825, Ex.1010, ¶[0068]. The “upper wiring” layer includes “metal wiring[s],” including “metal wiring 5b” that attaches “the drain of second [pFET] load transistor P2” at “contact part [] (common contact) 4g” and the “drain of second driver NMOS transistor N2” at “contact part 4j.” Saito825, Ex.1010, ¶[0071]; *see also* Saito825, Ex.1010,, FIG. 1.

304. From the exemplary citations above, it is clear that Saito825’s metal wiring 5b attaches contact parts 4g and 4j. Accordingly, a POSITA would have readily realized that the metal wiring layer 5b is an “upper wiring” layer that would have been formed above the cross-sections shown in Saito825’s FIGS. 12-21 (e.g., connecting the top of contacts 4g/4j as was conventional). It is only because the metal wiring 5 b deists on a layer above the contact part 4g that the cross-sections of Saito825’s FIGS. 12-21 do not expressly show the metal wiring 5b.

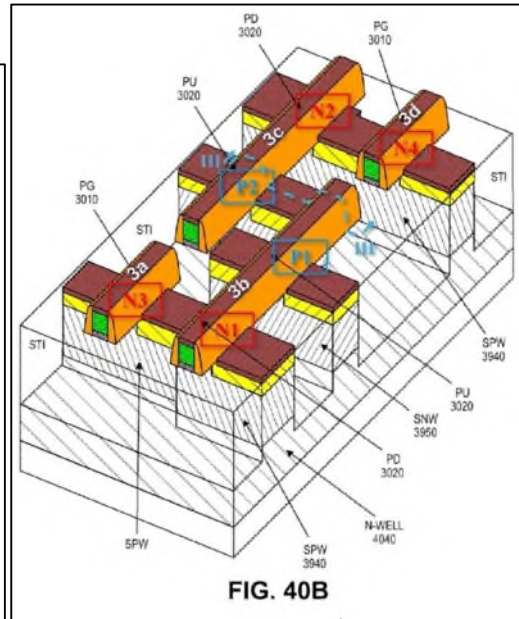


standard SRAM cell, and the gate electrode in FIGS. 12-21 is the polysilicon layer that Saito825 consistently identifies with a 3x element. Following that reasoning, all the polysilicon wirings should be identified by element 3x. Third, a POSITA would have immediately recognized that it is illogical for a polysilicon wiring to have a 5x identifier because, as Saito825 explains, the metal wirings 5x attach contact parts 4x in the upper layer metal wirings that are not shown in FIGS. 12-21. Fourth, a POSITA would have readily noticed that when this error is corrected to read “polysilicon wiring 3c” rather than “polysilicon wiring 5b” in FIGS. 12-21 and the accompanying text, Saito825’s descriptions match what would be expected along cutline III-III in FIG. 1. This confirms both that there is a typographical error, and the proposed correction makes sense and brings Saito825’s FIGS. 12-21 in line with the standard understanding of such an SRAM cell.

307. To compare annotated Saito825’s FIG. 1 with an annotated version of FIG. 40B from a SRAM cell patent (that shows a perspective view of a similar SRAM) the two are placed side by side below. *See* Thompson498, Ex.1450, FIG. 40B. The annotated from the Thompson patent shows Saito825’s layers 1x, 2x, and 3x but stops there. It does not show contact parts 4x or metal wirings 5x. As would be readily apparent to a POSTA, polysilicon wirings 3x (highlighted green) match in these two figures, as expected. Cutline III-III is also annotated onto FIG. 40B for clarity.



Saito825, Ex.1010, FIG. 1 (annotated)



Thompson498, Ex.1450 , FIG 40B (annotated)

308. Because Saito825's contact parts 4g and 4j and metal wiring 5b are conventional and well understood in the art SRAM structures, a POSITA would have understood those elements to appear as shown below in annotated Figure L (amending, annotating Thompson498, Ex.1450, FIG. 40B),⁸ with the layer for the metal wirings (5x) located above the polysilicon lines (3x) and attaching contact parts (4x) as upper-level wirings, as described in Saito825. Saito825, Ex.1010, ¶¶[0070]-[0071], FIG. 1; *see also* Pavlov-2008, Ex.1446, 24-25, Figs. 2.10(b)-(d); Balobas-2015, Ex.1449, Figs. 1-2.

⁸ For ease of review, Saito825's other contact parts 4x or metal wiring 5a are removed in Figure L.

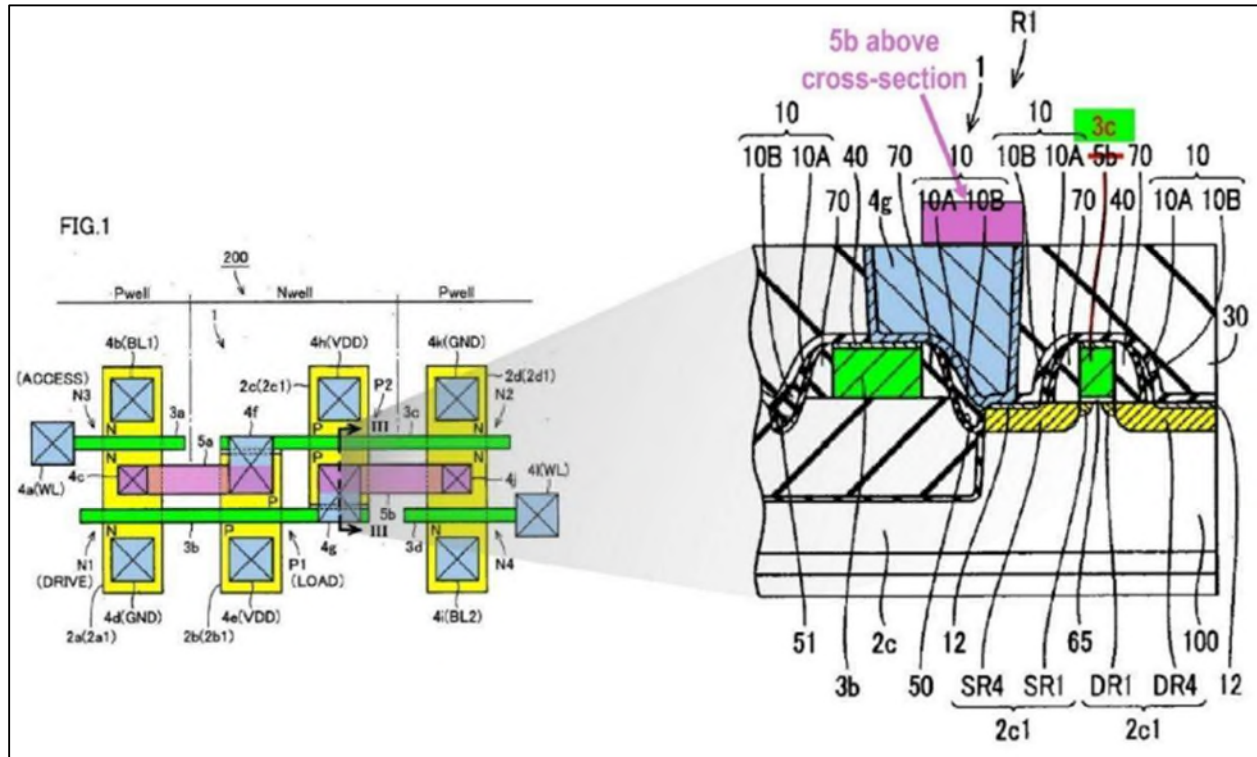
310. As Saito825's states, each of its 2x, 3x, 4x, and 5x identifiers links to a generally similar structure (e.g., source/drain, gate, contact, or metal wiring) just located on a different layer of the SRAM cell, a POSITA reading Saito825 would have recognized that "polysilicon wiring 5b" in Saito825's FIGS. 12-21 should refer to "polysilicon wiring 3c." Saito825, Ex.1010, ¶¶[0066]-[0068], ¶[0124]. A POSITA would have immediately understood that "polysilicon wirings," which are consistently designated by a 3x identifier in Saito825's specification and figures, is inconsistent with a designation of "5x" (the designation for upper metal wirings) in FIGS. 12-21. Accordingly, FIGS. 12-21 should indicate polysilicon wiring using identifier "3c" (not "5b") of FIG. 1 to match outline III-III. Saito825 itself confirms that this is a mere typographical error because it refers to "5b" correctly in other figures as a "metal wiring" that attaches contact parts 4g and 4j, not a polysilicon line like the ones in FIGS. 12-21. Saito825, Ex.1010, ¶¶[0066]-[0068], ¶[0071], ¶[0124]. It is my opinion that a POSITA would have readily identified this divergence and mentally corrected the errors in FIGS. 12-21 to change the polysilicon line "5b" to "3c."

311. The context of the Saito825's other disclosures confirms this. A POSITA also would have recognized that the "5b" label for polysilicon would not make sense in the context of Saito825's other figures because cross-section line III-III in FIG. 1 crosses two polysilicon wirings, 3b and 3c, and contact 4g touches

polysilicon wiring 3b and metal wiring 5b, but not polysilicon wiring 3c. *See* Saito825, Ex.1010, FIG. 1. Saito825's FIGS. 12-21 do not show contact part 4g touching the polysilicon wiring labeled "5b," as expected from FIG. 1. This comparison further confirms that the polysilicon gate in FIGS. 12-21 should be labeled "3c." Moreover, "polysilicon wiring 3c" is the polysilicon gate for PMOS transistor P2, as shown in FIG. 1—a gate structure. Saito825 describes "polysilicon wiring 5b" as part of a transistor, shows it as a gate structure, and does not show it touching contact 4g, all of which confirms that "polysilicon wiring 5b" should be "polysilicon wiring 3c" of PMOS transistor P2, consistent with Saito825's FIG. 1. Saito825, Ex.1010, ¶¶[0093]-[0096], [0101].

312. Moreover, if wiring "5b" indicated in FIGS. 12-21 corresponded with wiring "5b" shown in FIG. 1, then the wire that would have attached node Nb to transistor N4 in Saito825's FIG. 2 would not be connected due to the presence of "gate insulating film 65," which would prevent the follow of the current. Saito825 ¶[0051] (emphasis added); *See also* Saito825, Ex.1010, FIGS. 1-2, 12. A POSITA would have immediately recognized this structure would be nonsensical and is directly in conflict with the most fundamental basics of SRAM circuit design. *See* Saito825, Ex.1010, ¶[0071], FIGS. 1-2, 12; Pavlov-2008, Ex.1446, 24-25, Figs. 2.10(b)-(d). No one skilled in the art would have reasonably read Saito825 in that way.

313. Again, a POSITA would have immediately recognized that Saito825's polysilicon wiring labeled "5b" in FIGS. 12-21 should read "3c," as shown below.



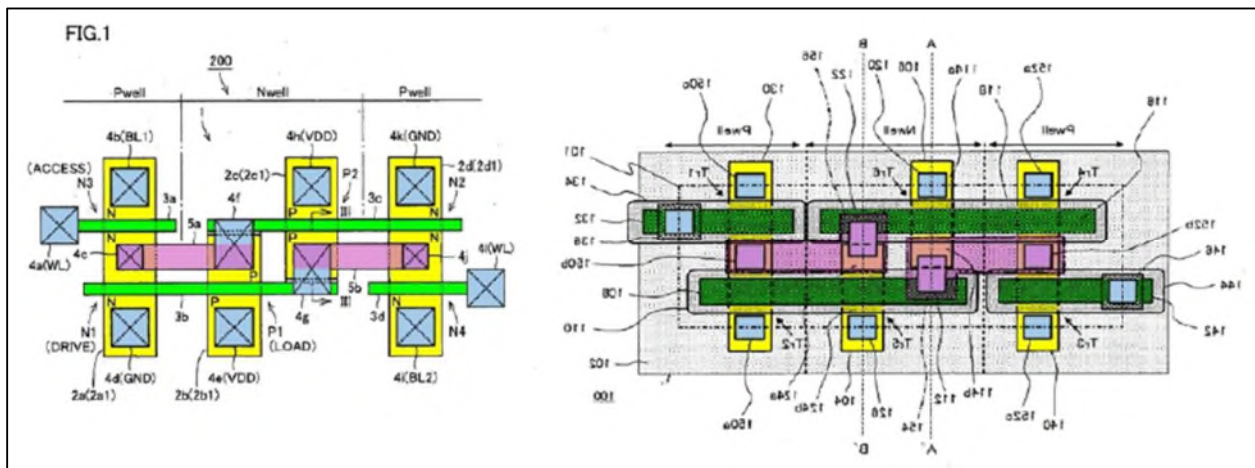
Saito825, Ex.1010, FIG. 1 (annotated)

Saito825, Ex.1010, FIG. 12
(excerpted, annotated)

314. Once fixing this blatant error, region “R1” in FIGS. 12-21 now appropriately reflects the cross-section corresponding to line III-III of FIG. 1. As illustrated above, polysilicon wiring 3b appears on the isolation region, polysilicon wiring 3c appears as the gate electrode of pFET P2, and common contact part 4g attaches polysilicon wiring 3b to the drain of pFET P2. Saito825, Ex.1010, ¶¶[0071], [0081], FIGS. 1, 12. A POSITA would have identified that “metal wiring 5b” is an “upper wiring” lying above and connected to contact parts 4g and 4j (and thus not

shown in Saito825's cross-sections of FIGS. 12-21). *See* Saito825, Ex.1010, ¶¶[0068], [0071]; Pavlov-2008, Ex.1446, 24-25, Figs. 2.10(b)-(d); Balobas-2015, Ex.1449, Figs. 1-2; Matsui832, Ex.1447, FIGS. 1-3. Again, this is standard for SRAM cells.

315. In addition to the Pavlov textbook discussed above, other prior art confirms this understanding. Below, for example, is Saito825's FIG. 1 side-by-side with Matsui's



Saito825, Ex.1010, FIG. 1 (annotated)

Matsui832, Ex.1447, FIG. 1
(annotated, flipped)

316. Matsui's cross-section lines A-A' and B-B' in FIG. 1 are similar to Saito825's cross-cut line III-III. As I explain below, Matsui's cross-sections confirm my opinion regarding Saito825's typographical error, which would have been readily apparent to a POSITA who understands standard SRAM cell technology.

317. Matsui's "FIG. 1 is a top view" of the SRAM cell. Matsui832, Ex.1447, ¶[0055]. Like Saito825's PMOS active regions 2b and 2c, Matsui's SRAM includes PMOS active regions 104 (FIG. 3) and 106 (FIG. 2). *See* Matsui832, Ex.1447, ¶[0056], FIGS. 1-3; Saito825, Ex.1010, ¶[0060], FIGS. 1, 12. Matsui's SRAM includes PMOS source/drain regions 124a/124b (FIG. 3) and 114a/114b (FIG. 2), similar to Saito825's source/drain regions 2b1 and 2c1. *See* Matsui832, Ex.1447, ¶[0062], ¶[0065], FIGS. 1-3; Saito825, Ex.1010, ¶[0060], FIGS. 1, 12. Matsui further includes PMOS gate electrodes 108 and 116, like to Saito825's polysilicon layers 3b and 3c. *See* Matsui832, Ex.1447, ¶[0062], ¶[0065], FIGS. 1-3; Saito825, Ex.1010, ¶[0066], FIGS. 1, 12. And Matsui's contacts 112 and 122 connect the source/drain regions with upper-layer interconnections 154 and 156, like to Saito825's contacts 4f and 4g. *See* Matsui832, Ex.1447, ¶[0063], ¶[0066], FIGS. 1-3; Saito825, Ex.1010, ¶[0069], FIGS. 1, 12.

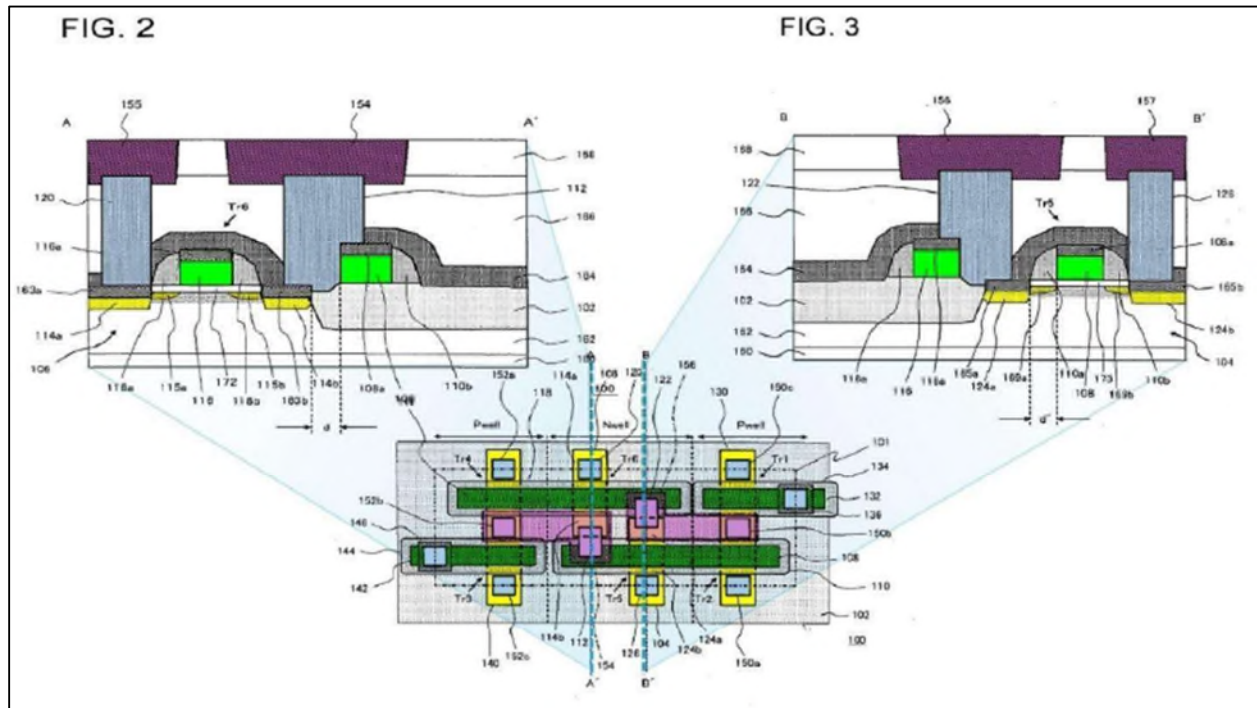


Figure O (Matsui832, Ex.1447, FIGS. 1-3 (annotated))

318. Figure O above shows Matsui's FIG. 1 with callouts to FIG. 2 (cross-section taken along FIG. 1 cutline A-A') and FIG. 3 (cross-section taken along FIG. 1 cutline B-B'). See Matsui832, Ex.1447, ¶¶[0038]-[0040], ¶¶[0060]-[0061], ¶[0064], ¶[0069], FIGS. 1-3. In both cross-sections of Saito825 and Matsui, the metal wirings 154 and 156 (highlighted purple) lie above the contact parts (highlighted light blue) and well above the polysilicon layers (highlighted green). This reiterates my earlier point about Saito825 and further validates that a POSITA would recognize Saito825's clerical mistake. To clarify, a POSITA could not interpret Saito825's disclosures in any other manner.

319. A POSITA would easily recognize the typographical mistake in Saito825's document, as Saito825's disclosure does not aim to modify the standard layout, circuit, or structure of the standard SRAM cell. Rather, it focuses on addressing problems associated with recesses (50) formed in the isolation regions adjacent to the source/drain areas. *See* Saito825, Ex.1010, Abstract, ¶¶[0011], [0022]-[0023], [0027], [0074]-[0075], FIGS. 1-3; Pavlov-2008, Ex.1446, 24-25, Figs. 2.10(b)-(d). Immediately recognizing the error in Saito825 and mentally correcting in, a POSITA would have recognized that FIGS. 12-21 show conventional SRAM cross-sections along cutline III-III of FIG. 1.

320. Putting aside Saito825's express disclosures, a POSITA would understand that the polysilicon wiring 3c in FIG. 1 shares the same structure as the element labeled "5b" in FIGS. 12-21. *See* Saito825, Ex.1010, ¶[0124] ("In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g."). In other words, a POSITA would have immediately recognized (1) that Saito825 contains a typographical error whereby "polysilicon wiring 5b" refers to and should be labeled "polysilicon wiring 3c" in FIGS. 12-21, and, regardless, (2) that the structure labeled "polysilicon wiring 5b" in FIGS. 12-21 is part of a MIS transistor with the structure relied on in my opinions below.

321. All the analysis above regarding Saito825's typographical error and disclosed structures remain true when substituting Fukutome's epitaxial SiGe source/drain regions for Saito825's non-epitaxial source/drain regions in active regions 2b and 2c.

a. The Saito825-Fukutome-James Combination Would Have Been Obvious

322. In my opinion, a POSITA would have found it obvious to incorporate epitaxial SiGe source/drain layers, as disclosed in Fukutome, into Saito825's source/drain regions 2c1 to improve pFETs P1 and P2 with compressive strain. Figure M below shows this embodiment equivalent to Saito825's FIG. 21 before the ILD layer 30 is added over CESL 13. *See* Section V.F above; Fukutome, Ex.1011, ¶[0110], FIG. 5G.⁹

⁹ Figure M is based on composite FIG. 21 for ease of reference because this figure shows an intermediate step corresponding to FIG. 11 before contact plug 4g is formed.

323. Again, Figure M below shows an embodiment of the Saito825-Fukutome-James combination.¹⁰ This combination (1) incorporates epitaxial SiGe source/drain regions (highlighted yellow), as disclosed by Fukutome and James, into Saito825's source/drain regions 2c1, and (2) modifying Saito825's "plasma nitride (SiN)" insulating film 13 in view of James for it to impart a tensile stress.

¹⁰ Figure M also reflects the correction of Saito825's typographical error to replace "5b" with "3c." *See* Section X.C.1 above. The label "3c" is in red to show it as corrected.

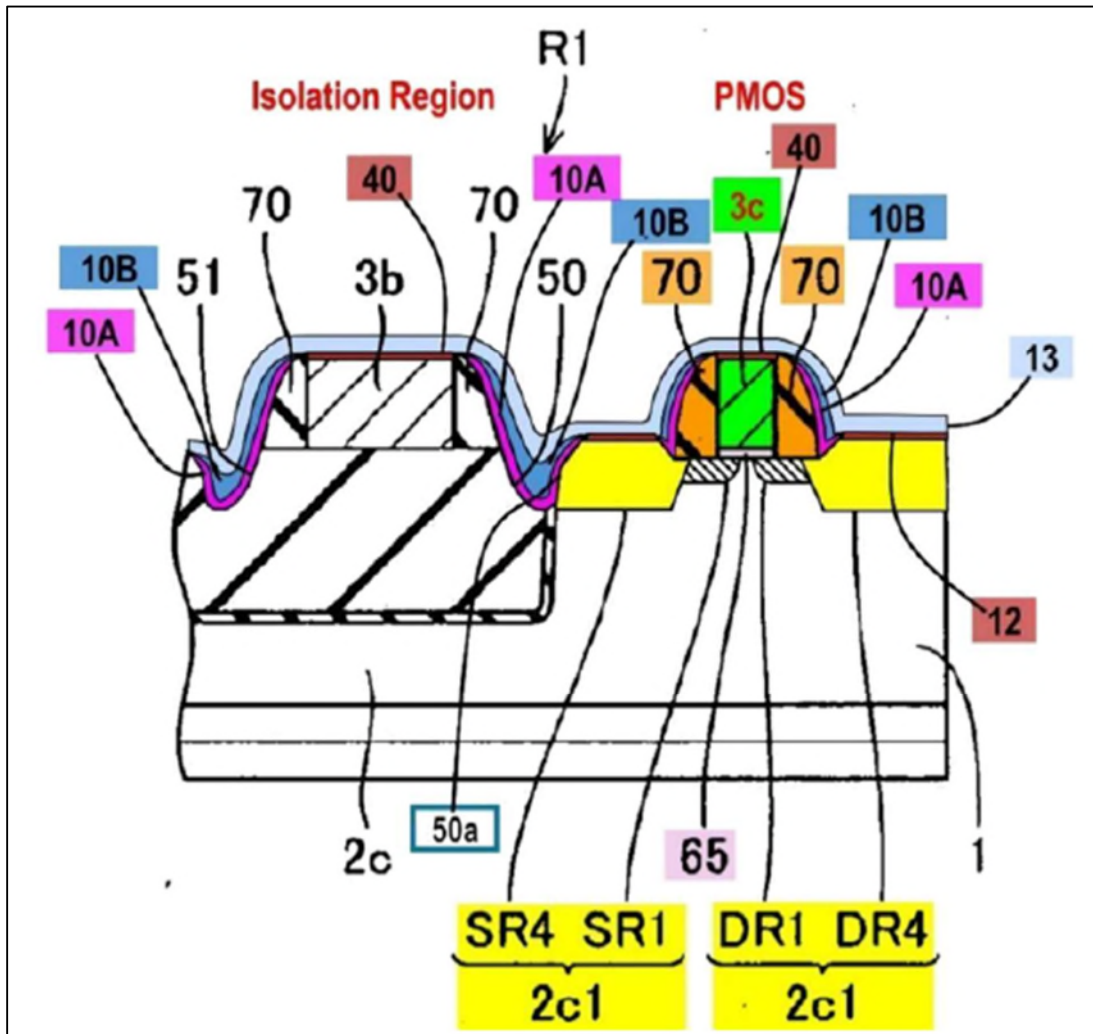


Figure M

324. Before the application for the '425 patent was filed, faceted epitaxial SiGe source/drain regions were standard industry practice to enhance pFET performance. Using SiGe source/drain regions had already been widely adopted in each of the four previous generations of high-volume commercial transistors. *See* Section V.F above; Thompson-2004, Ex.1523 1790-96 (describing Intel's 90nm devices); Bai-2004, Ex.1532, 657-58 (describing Intel's 65nm devices); Mistry2007,

Ex.1516, 247-50 (describing Intel's 45nm devices); Natarajan-2008, Ex.1428, 1 (describing Intel's 32nm devices). Accordingly, it is my opinion, a POSITA would have found it obvious to incorporate epitaxial SiGe source/drain regions (as Fukutome discloses) into Saito825's source/drain regions 2c1 because it was well-known way to improve the performance of pFET. *See* Section V.F.

325. It was equally well-known to use a tensile CESL to enhance the performance of nFETs. *See* Section V.F above; James, Ex.1012, 2, 4; Morin-2007, Ex.1528, 355-56, 367; Hsu823, Ex.1506, ¶[0003]; Jung, Ex.1529, Abstract, ¶[0090]; Ke, Ex.1531, ¶[0003]; Bohr, Ex.1527, ¶¶[0038]-[0039], FIG. 6. A POSITA would have understood that Saito825's "plasma nitride (SiN)" insulating film 13 describes a CESL. *See* Saito825, Ex.1010, ¶¶[0072], [0080]-[0084], FIGS. 3, 12, 21. Because it was so well known in the art to improve nFET performance, it is my opinion, that a POSITA would have found it obvious to modify Saito825's "plasma nitride (SiN)" insulating film 13 to cause a tensile stress, consistent with James's disclosures. *See* Sections V.F and X.A.1 above; Jung, Ex.1529, ¶[0090], ¶¶[0099]-[0100], Tbl. V.

326. A POSITA would have recognized, while incorporating epitaxial SiGe source/drain stressor layers into Saito825's source/drain regions 2c1, that Saito825's oxide layer 10A (highlighted magenta in Figure M above) would form and remain in the spaces between the facets of the raised epitaxial SiGe source/drain regions (highlighted yellow in Figure M above) and sidewalls 70 (orange in Figure M

above). *See* Murthy556, Ex.1430, 9:11-15, 9:30-35, FIGS. 7-9. This is similar to how oxide layer 10A remains in Saito825's recesses 50. *See* Saito825, Ex.1010, FIGS. 11, 12. I discuss this aspect of the Saito825- Fukutome-James combination in greater detail below.

(1) A POSITA would have been motivated to arrive at the claimed invention using the Saito825-Fukutome-James combination

(a) Compressive raised SiGe source/drain regions would have been obvious to a POSITA

327. In my opinion, a POSITA would have found it obvious to incorporate Fukutome's raised SiGe source/drain regions into Saito825's pFETs (including P2) for the purpose of improving transistor performance by boosting channel mobility and limiting junction leakage. *See* Sections V.F and X.C.1.a above.

328. Saito825 discloses PMOS source/drain regions 2c1 that comprise source/drain impurity diffused layers SR1/DR1, as well as source/drain impurity diffused layers SR4/DR4. Saito825, Ex.1010, ¶[0101]; *See also* Saito825, Ex.1010, ¶¶[0094], [0097], FIGS. 12, 16, 17, 21. As shown in Saito825 FIGS. 16 and 17 show, Saito825's source/drain diffusion regions SR1 and DR1 are formed before sidewalls 70, using polysilicon wiring "5b" [sic:3c] as an ion implantation mask. *See* Saito825, Ex.1010, ¶[0094], FIG. 16. Source/drain diffusion regions SR4 and DR4 are then formed after sidewalls 70, using both polysilicon wiring 3c and sidewalls 70 as an

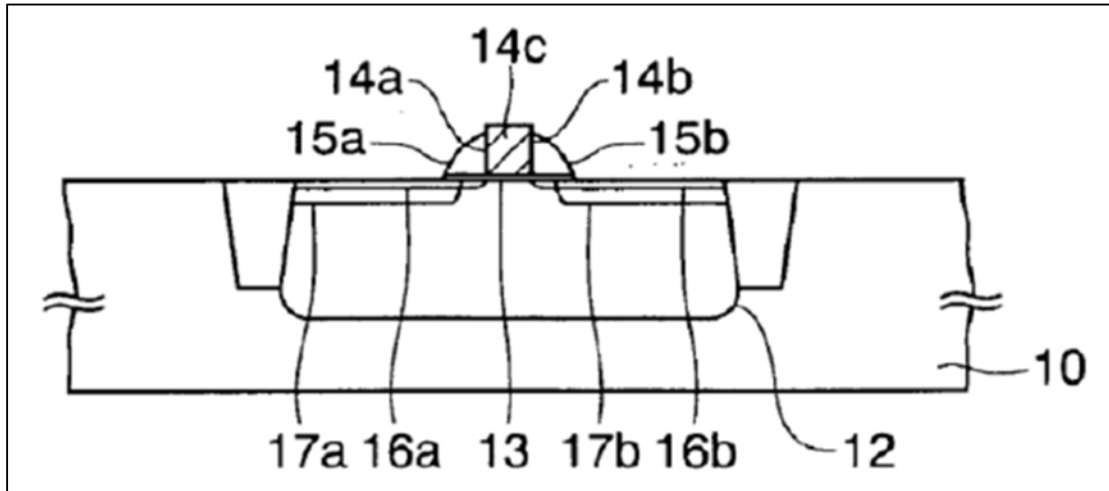
ion implantation mask. *See* Saito825, Ex.1010, ¶¶[0097], [0101] (“Then, as shown in FIG. 17, an impurity is introduced into the main front surface of semiconductor substrate 100 which adjoins polysilicon wiring 5b [sic:3c], and impurity diffused layer SR4 and DR4 are formed in it. Hereby, impurity diffused layer 2c1 which consists of impurity diffused layer SR1 and impurity diffused layer SR4 is formed in the main front surface of semiconductor substrate 100 located in one side surface side of polysilicon wiring 5b [sic:3c]. On the main front surface of semiconductor substrate 100 located in the other side surface side of polysilicon wiring 5b [sic:3c], impurity diffused layer 2c1 which consists of impurity diffused layer DR1 and impurity diffused layer DR4 is formed.”), FIG. 17.

329. Saito825 further explains the formation of source/drain regions 2c1, which are made by implanting boron impurities, demonstrating that P2 is a pFET. *See* Saito825, Ex.1010, ¶[0060] (“P type impurities, such as a boron, are selectively implanted into active regions 2b, 2c formed in [the] N well region, and impurity diffusion region 2b1 and 2c1 are formed.”), ¶[0066] (“Second access PMOS transistor P2 is formed in the intersection part of impurity diffusion region 2c1 comprising the region used as a source/drain, and polysilicon wiring 3c.”).

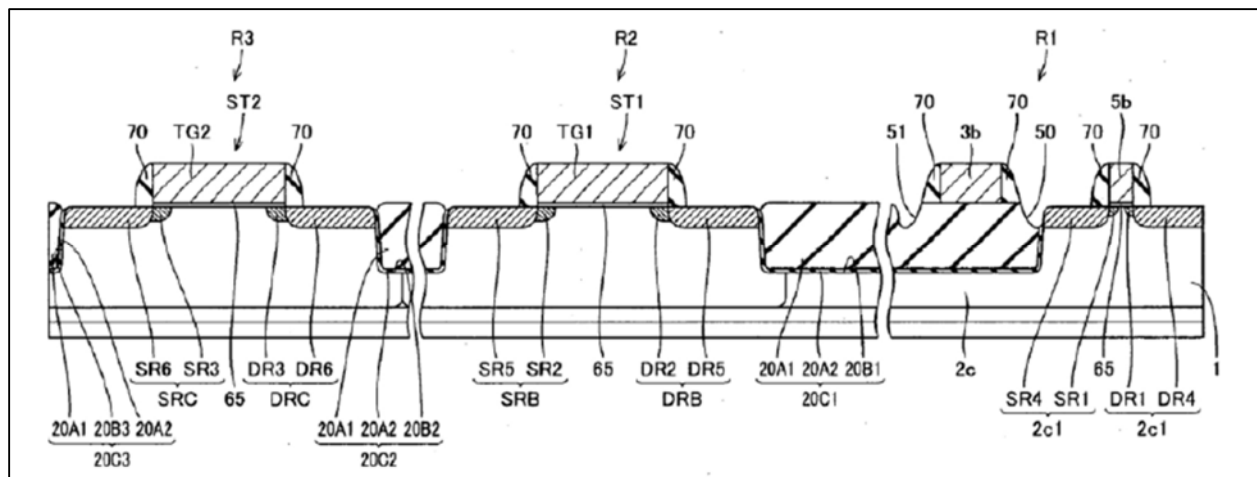
330. It is my opinion that a POSITA would have seen that that Fukutome’s FIGS. 5B-5E and Saito825’s process described above, disclose similar method of implantation. *See* Fukutome, Ex.1011, ¶¶[0083], [0087], FIGS. 5B-5C. Similar to

Saito825, Fukutome “us[es] the gate electrode 14c as a mask” to implant “boron ions as p-type impurities” to form “first and second source/drain extensions 16a and 16b [that] are shallowly formed in the silicon substrate 10 beside the first and second side surfaces 14a and 14b of the gate electrode 14c.” Fukutome, Ex.1011, ¶[0083]; *see also* Fukutome, Ex.1011, FIG. 5B. Fukutome then “us[es] the gate electrode 14c and the first sidewalls 15a and 15b as a mask” to implant “source/drain regions 17a and 17b[,] which are deeper and denser than the source/drain extensions 16a and 16b,” in substrate 10 “beside the gate electrode 14c.” Fukutome, Ex.1011, ¶[0087]; *see also* Fukutome, Ex.1011, FIG. 5C. Fukutome also implants “boron ions as p-type impurities,” it describes a pFET. *See* Fukutome, Ex.1011, ¶¶[0083], [0087].

331. Fukutome’s sidewalls 15a and 15b are formed on the side of the gate electrodes, are made of silicon oxide (like Saito’s sidewalls 70). *See* Saito825, Ex.1010, ¶[0073], FIG. 17; Fukutome, Ex.1011, ¶¶[0084]-[0086], FIG. 5C. At this point in the processing steps, Saito825’s and Fukutome’s FETs have essentially the same structure. *Compare* Saito825, Ex.1010 17, *with* Fukutome, Ex.1011, FIG. 5C.



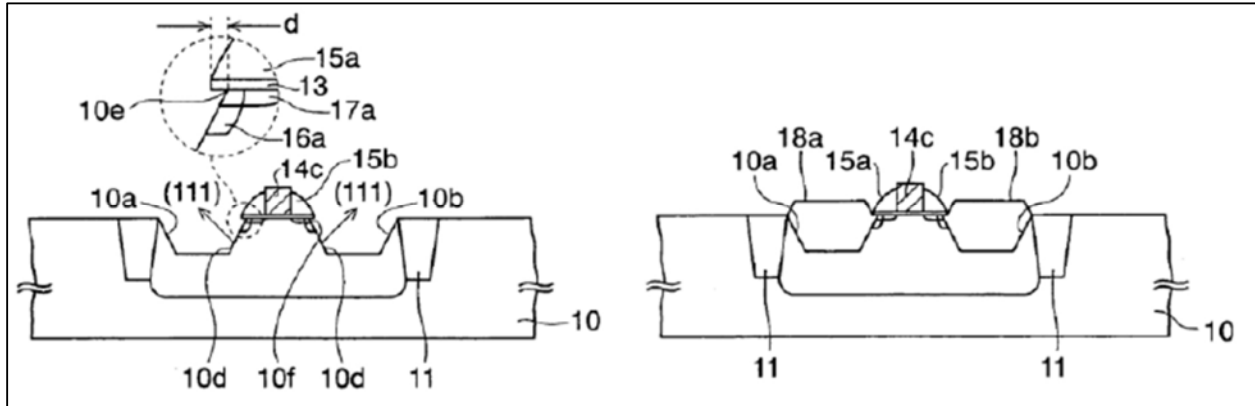
Fukutome, Ex.1011, FIG. 5C



Saito825, Ex.1010, FIG. 17

332. Fukutome then teaches etching trenches in the substrate and epitaxially growing SiGe source/drain regions 18a/18b in them. *See* Fukutome, Ex.1011, ¶¶[0089]-[0102], FIGS. 5D-5E. Namely, Fukutome teaches to form trenches by etching recesses 10a and 10b into the semiconductor substrate 10 to expose the (111)

silicon planes on side surfaces 10c and 10d of the etched substrate. *See* Fukutome, Ex.1011, ¶[0092], FIG. 5D.



Fukutome, Ex.1011, FIG. 5D

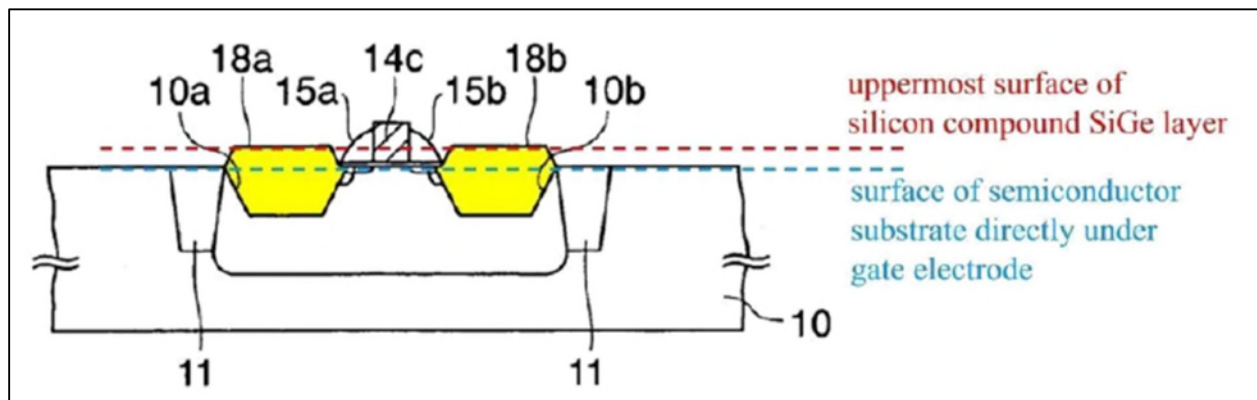
Fukutome, Ex.1011, FIG. 5E

333. Next, Fukutome teaches forming raised SiGe epitaxial layers 18a and 18b.¹¹ Fukutome, Ex.1011, ¶¶[0098]-[0102], FIG. 5E. Fukutome states “[t]he distances between the bottom surface of the n-well 12 and the upper surfaces of the

¹¹ These epitaxial SiGe source/drain regions are doped with boron either “in-situ,” (meaning in the place, or in this context, during growth) or by ion implantation and annealing heat treatment after growth. Fukutome, Ex.1011, ¶[0102]. A POSITA would have recognized both of these techniques as common and conventional design choices in the prior art. Using either design choice does not affect my opinion on unpatentability, nor would it cause a POSITA to not have found the Saito825-Fukutome-James combination obvious.

source/drain material layers 18a and 18b are increased by forming the upper surfaces of the source/drain material layers 18a and 18b at positions higher than the surface of the silicon substrate 10.” Fukutome, Ex.1011, ¶[0100]; *see also* Fukutome, Ex.1011, FIG. 5E. Fukutome explains this benefits of following these steps is to suppress source/drain contact junction leakage and improve reliability. Fukutome, Ex.1011, ¶[0100].

334. In annotated FIG. 5E below, the annotations show the uppermost surface of Fukutome’s SiGe source/drain regions 18a and 18b is above the uppermost surface of substrate 10.



Fukutome, Ex.1011, FIG. 5E (annotated)

335. Fukutome also teaches that the SiGe regions 18a and 18b “introduc[e] strain into a channel” to add compressive stress in the pFET channel region along the gate length direction “by utilizing a difference in lattice constant between silicon and SiGe.” Fukutome, Ex.1011, ¶[0005]; *see also* Fukutome, Ex.1011, ¶[0110] (“In the MOS transistor TR, [the] silicon lattice in the silicon substrate 10 is forcefully

stretched so as to match the large lattice spacing of SiGe due to a mismatch between the lattice constant of the silicon substrate 10 and those of the source/drain material layers 18a and 18b, and stress in the directions of the arrows in the drawing [is] applied to a channel under the gate electrode 14c. As a result, compared to the case where stress is not applied, the mobility of carriers in the channel is improved, and the drive capability of the MOS transistor can be improved.”), ¶[0249]. As I explain above, the lattice differences between the SiGe layers and the silicon substrate, the SiGe layers accordingly cause a compressive stress on the channel region. *See* Section V.F above. The arrows in Fukutome’s FIG. 5G indicate this stress. Fukutome, Ex.1011, ¶[0110] (“stress in the directions of the arrows in the drawing [is] applied to a channel under the gate electrode 14c”).

336. Based on the above, a POSITA would have found it obvious to incorporate Fukutome’s epitaxial SiGe source/drain regions into Saito825’s pFETs P1 and P2 for the purpose of improving “the mobility of carriers in the channel . . . and the drive capability of the MOS transistor can be improved.” Fukutome, Ex.1011, ¶[0110]. The use of SiGe in this function was a well-known and used technique in the prior art and industry for the purpose of improving PMOS carrier (hole) mobility, as I explain in Section V.F above. As Fukutome teaches, a POSITA also would have been motivated to incorporate Fukutome’s SiGe source/drain regions into Saito825’s pFETs P1 and P2 to suppress junction leakage and improve

reliability, and given the POSITA's experience they would have also found it obvious to do so. Fukutome, Ex.1011, ¶[0100].

337. The advantages of utilizing epitaxial SiGe source/drain regions, as disclosed by Fukutome, were widely recognized in the industry. *See* Section V.F above; Fukutome, Ex.1011, ¶¶[0100], [0110]; Wu922, Ex.1005, ¶[0004]; Wang906, Ex.1009, ¶¶[0004]-[0005]; Bohr, Ex.1527, ¶[0024]; James, Ex.1012, 2. This structure SiGe source/drain regions was being used in each of the four preceding high-volume commercial processes for the purpose of improving the performance of pFET. *See* Section V.F above; Thompson-2004, Ex.1523 1790-96 (describing Intel's 90nm devices); Bai-2004, Ex.1532, 657-58 (describing Intel's 65nm devices); Mistry2007, Ex.1516, 247-50 (describing Intel's 45nm devices); Natarajan-2008, Ex.1428, 1 (describing Intel's 32nm devices).

338. James states that "epitaxial SiGe source/drains . . . create compressive stress" and "improve [] hole mobility [in PMOS transistors] by as much as 50%." James, Ex.1012, 2. Further, James also explains that "[c]rystalline [SiGe] facets form raised source/drains," like those shown in Fukutome's FIGS. 5E-5G, and that these facets "reduc[e] series resistance" and "counteract []" "tensile stress from . . . nitride [etch stop] layer[s]," which also helps improve pFET performance. James, Ex.1012, 2; *See also* Fukutome, Ex.1011, FIGS. 5E-5G; Section V.F above.

339. Figure M above illustrates an intermediate structure¹² of the combination of Saito825 with Fukutome's faceted SiGe source/drain regions.¹³ It is

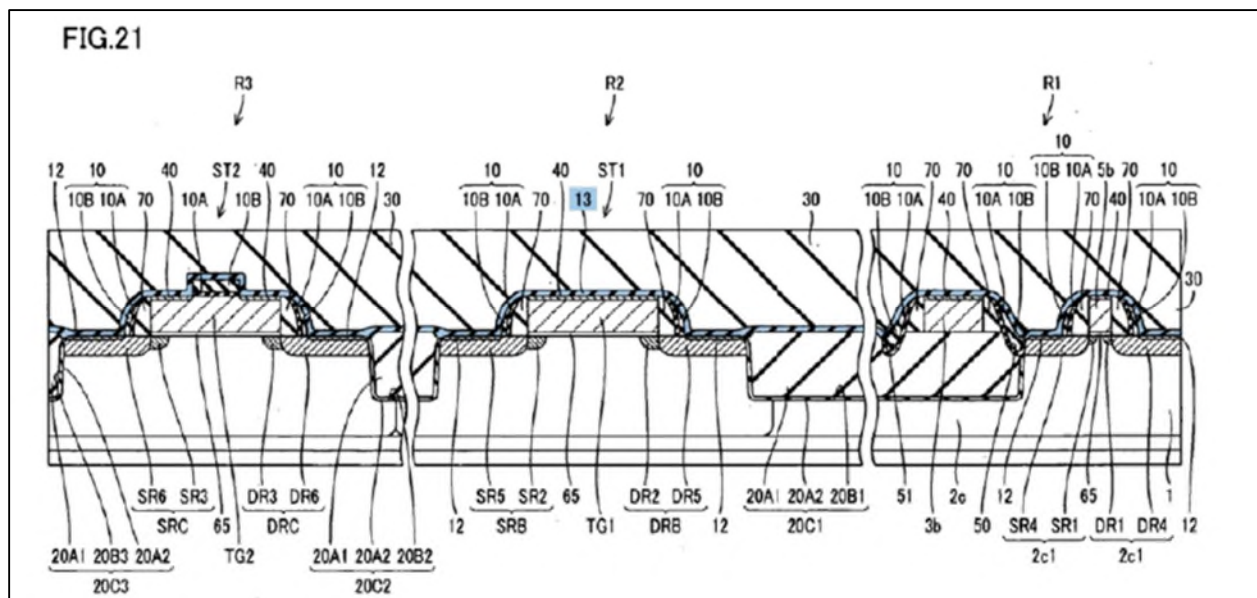
¹² This illustration serves as an intermediate step because, after integrating Fukutome's epitaxial SiGe source/drain regions 18a and 18b into Saito825's source/drain regions 2c1, the process flow for the Saito825-Fukutome-James combination proceeds as outlined in Saito825.

¹³ Figure M follows Fukutome's disclosure related to the epitaxial SiGe layers that are doped in-situ with boron, thus obviating the need to form Saito825's diffusion regions SR4 and DR4. *See* Fukutome, Ex.1011, ¶[0102] ("In the case where in-situ doping is performed when the source/drain regions 17a and 17b are formed, impurity implantation and heat treatment may be omitted."). Alternatively, the SiGe layers may be doped by ion implantation. *See* Fukutome, Ex.1011, ¶[0101] ("[T]he source/drain material layers 18a and 18b are formed after the source/drain regions 17a and 17b have been formed. However, the order of formation of these is not particularly limited. The source/drain regions 17a and 17b may be formed after the source/drain material layers 18a and 18b have been formed."). A POSITA would understand both methods as equally valid design choices, with neither affecting my analysis in a significant way.

my opinion that a POSITA would have been motivated to incorporate Fukutome's epitaxial SiGe source/drain regions into Saito825's pFETs P1 and P2 for the purpose of improving carrier (hole) mobility and reducing source/drain resistance, ultimately resulting in improved performance. *See* Fukutome, Ex.1011, ¶[0110]; James, Ex.1012, 2; Section V.F above.

(b) Implementing Saito825's SiN layer 13 with tensile strain would have been obvious

340. It is my opinion that a POSITA further would also have been motivated to modify Saito825's SiN layer 13 to cause it to impart tensile stress for the benefit of improving improve carrier (electron) mobility in Saito825's nFETs. *See* Sections V. F and X.C.1.a. above.



Saito825, Ex.1010, FIG. 21 (annotated)

341. A POSITA would have readily understood that Saito825's "plasma nitride (SiN)" "insulating film 13" is a CESL covering Saito825's entire SRAM cell, including transistors N1-N4 and P1-P2, polysilicon wirings 3b and 3c, etc. Saito825, Ex.1010, ¶[0080]; *see also* Saito825, Ex.1010, FIGS. 1, 12, 21.¹⁴ Saito825 explains that FIG. 12 shows "well region[s] of various conductivity types." Saito825, Ex.1010, ¶[0091]. As FIG. 21 shows above, insulating film 13 blankets all of those "well region[s] of various conductivity types." Saito825, Ex.1010, ¶[0091]; *see also* Saito825, Ex.1010, FIGS. 12, 21. For example, Saito825 explains that "interlayer insulation film 30 is provided with insulating film 13," both being formed over "polysilicon wiring 3b." Saito825, Ex.1010, ¶[0080]. A POSITA would have realized that the insulating film 13 and the insulation layer 30 would therefore cover the various regions of the SRAM cell because polysilicon wiring 3b (and analogous polysilicon wiring 3a) do also.

342. In Saito825, first the source/drain regions are formed, and insulating films 10A and 10B are deposited and patterned, then the insulating film 13 is deposited. *See* Saito825, Ex.1010, ¶¶[0091]-[0092], [0101], [0104], FIGS. 5-6, 15-

¹⁴ FIGS. 12 and 21 show similar cross-sections. *See* Saito825 ¶¶[0030]-[0048] (describing same embodiment for FIGS. 3-21), ¶[0049], ¶¶[0084]-[0085] (same). Discussion of either FIG. 12 or 21 is equally applicable to both figures.

18. Insulating films 10A and 10B are then etched to expose the top surfaces of the polysilicon wirings, leaving remnants of films 10A and 10B on sidewalls and in recesses. Saito825, Ex.1010, ¶[0107], FIGS. 7, 19. The polysilicon wirings are then silicided. Saito825, Ex.1010, ¶¶[0077]-[0081], [0084], [0114] (“[B]y etching into insulating film 10A, lamination insulating film 10 which consists of insulating film 10A and insulating film 10B is formed over the upper surface of sidewall 70 from the boundary region of the upper surface and the side surface of active region 2c, and it fills up with it in recess 50.”), [0116]-[0117], FIGS. 8, 20. Silicide film 12 forms on the upper surfaces of the source/drain regions and the top of the gate electrodes. Saito825, Ex.1010, ¶¶[0077]-[0079], [0117]-[0119], FIGS. 8, 20. After the silicidation step, Saito825’s insulating film 13 is deposited over the entire SRAM cell, as FIG. 21 shows above. *See* Saito825, Ex.1010, ¶¶[0080], [0091], [0120], [0124] (explaining that all polysilicon wirings “are formed similarly”), FIGS. 12, 21.

343. Even though Saito825 is silent on whether the insulating SiN layer 13 imparts stress – whether tensile or compressive strain. It is my opinion, a POSITA would be motivated to make Saito825’s SiN insulating layer 13 a tensile stress inducing layer because, as James explains, a tensile CESL improves nFET performance. *See* James, Ex.1012, 2 (explaining that “[l]ocalized tensile stress is

applied to the channels of NMOS devices by a highly stressed nitride sealant layer,” and that “[t]his increases electron mobility by ~10%”).

344. James further explains that using a tensile CESL to apply strain “involves no extra cost for either capital equipment or special substrates.” James, Ex.1012, 5 (“It is perhaps ironic that stress in silicon nitride layers, a problem in previous process generations, has now been harnessed to apply strain. So far, it has been used only to provide tensile stress to enhance NMOS performance (at least in the three examples we have shown) This technique has the noteworthy convenience that it can be accomplished by process tuning, and involves no extra cost for either capital equipment or special substrates.”); *See also* Section V.F above.

345. It was already well known in the prior art that forming SiN layers on top of P and N transistors causing channel benefits as transistors continued to decrease in size.

346. It was also well known to use the strained SiN layers followed by stress memorization technique to improve the device performance. In a 2004 article by Chen et al. titled “Stress Memorization Technique (SMT) by Selectively Strained-Nitride Capping for Sub-65nm High-Performance Strained-Si Device Application” (“In this paper, we proposed a novel stress memorized technique (SMT) to improve the device performance without PMOS degradation. A high tensile nitride capping layer acts as a temporary stressor to effectively modulate the channel stress. The

stress effect is then enhanced and memorized by well-controlled poly amorphization and re-crystallization procedures. This high tensile nitride capping layer will be removed after the annealing step. Therefore, a much thicker capping layer can be used to increase the stress level without any process limitation to impact the subsequent gap filling process steps. . . . After the silicide formation, the low temperature, high-tensile Nitride film is deposited as Contact-Etch-Stop-Layer (SIN-CESL) to add up the stress effect. Finally, the metallization is done for device characterization.”).

347. A POSITA would have recognized that modifying Saito825’s SiN insulating film 13 to cause tensile stress would improve nFET performance in an economical way.

348. A POSITA, therefore, would have been motivated to use Saito825’s insulating SiN film 13 impart tensile strain for the purpose of improve performance in nFETs N1-N4, recognizing that pFETs P1 and P2 would be similarly improved by also forming Fukutome’s epitaxial SiGe source/drain regions. *See* Sections V.F and X.C.1.a.(1)(a) above. It was well known in the art that using strained silicon methods could improve carrier mobility and performance. *See* Section V.F above; James, Ex.1012, 2, 4; Morin-2007, Ex.1528, 355-56, 367; Hsu823, Ex.1506, ¶¶[0003], ¶¶[0037]-[0038]; Jung, Ex.1529, Abstract, ¶¶[0099]-[0100], Tbls. IV, V. One of those ways is to use a contact etch stop layer (“CESL”) made of silicon nitride, that

is formed under certain conditions, can be “used . . . for applying stress to [a] channel region” to improve carrier mobility. Hsu823, Ex.1506, ¶[0003]; *See also* Jung, Ex.1529, ¶[0090], ¶¶[0099]-[0100], Tbl. V; Ke, Ex.1531, ¶[0003] (“A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device.”); Morin-2007, Ex.1528, 355-56; Bohr, Ex.1527, ¶¶[0038]-[0039], FIG. 6. For example, Morin explains that it “is important to work to improve the nMOS transistors since other solutions” like epitaxial SiGe “can enhance the pMOS performances.” Morin-2007, Ex.1528, 355-56.

349. It is my opinion that a POSITA would have been motivated to use a tensile-strain inducing layer as Saito825’s SiN layer 13 to improve nFET carrier (electron) mobility. This change is a simple an inexpensive modification to Saito825’s structure. *See* Morin-2007, Ex.1528, 355-56; James, Ex.1012, 2, 5; Hsu823, Ex.1506, ¶[0039] (preferable applying tensile CESL on both NMOS and PMOS devices because “the performance of PMOS devices can be easily improved with SiGe stressors, while the performance of NMOS devices is relatively difficult to improve”); Alvarez, Ex.1006, ¶¶[0033], [0047], [0049], [0054], [0065], Tbl. 1, FIG. 9 (explaining that using one tensile CESL layer over both NMOS and PMOS avoids “additional lithography and etch step[s] . . . , which [are] costly and time-consuming”); Ke, Ex.1531, ¶[0003] (“A commonly used method for applying stress

to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device.”); Bohr, Ex.1527, ¶¶[0038]-[0039], FIG. 6.

350. A POSITA also would have understood that any tensile stress imparted from a modified Saito825 SiN layer 13 in the PMOS region of the device would be mitigated by the presence of a buffer layer and the compressive SiGe source/drain layers. *See* Sections V.G and X.A.1 (describing benefits of Alvarez’s stress-controlling layer); James, Ex.1012, 2; Alvarez, Ex.1006, ¶¶[0047], [0049], [0054], [0065], Tbl. 1, FIG. 9; Murthy556, Ex.1430, 9:27-29; Doris, Ex.1429, ¶[0005]; Lee870, Ex.1431, ¶[0067], FIG. 5; Cheng810, Ex.1432, ¶[0030], Fig. 1F; Bohr, Ex.1527, ¶¶[0038]-[0039], FIG. 6; Baik, Ex.1433, ¶[0037]; Hsu823, Ex.1506, ¶[0039]; Morin-2007, Ex.1528, 355-56. For example, a POSITA would have understood that Saito825’s intermediate oxide layer 10A would have mitigated the tensile stress on the pFETs by acting like Alvarez’s stress-controlling layer discussed above. *See* Sections V.G and X.A.1 above.

351. In my view, a POSITA would be motivated to utilize a tensile SiN layer 13 to boost nFET performance cost-effectively, as previously discussed.

(2) A POSITA would have reasonably expected to succeed in realizing the Saito825-Fukutome-James combination

352. It is my opinion that a POSITA would have reasonably expected to have success by incorporating epitaxial SiGe source/drain regions into Saito825’s PMOS

source/drain regions (as Fukutome discloses) while also making Saito825's SiN insulating film 13 impart tensile stress (as taught by James). *See* Section X.C.1.a.(1) above.

353. Incorporating epitaxial SiGe source/drain regions like those Fukutome discloses was conventional and well known in the prior art. As stated above, it had already been used in each of the previous four generations of high-volume commercial devices (see Section V.F above) and would have required nothing more than following the conventional steps of etching trenches into the silicon substrate and growing epitaxial SiGe source/drain therein. *See* Section X.C.1.a.(1)(a) above; *compare* Saito825, Ex.1010, ¶¶[0092]-[0103], FIGS. 16-17, *with* Fukutome, Ex.1011, ¶¶[0085]-[0102], FIGS. 5C-5E. After forming faceted and raised SiGe layers, Saito825's method follows by forming layers 10A and 10B and eventually depositing insulating SiN film 13 as a tensile film (as James discloses). *See* Saito825, Ex.1010, ¶¶[0104]-[0106], FIG. 18; James, Ex.1012, 2; Section V.F above. A POSITA would have recognized that forming epitaxial SiGe source/drain regions (like disclosed in Fukutome) into Saito825's structure of its PMOS transistors P1 and P2 would have achieved the ordinary and expected result of causing compressive strain to those pFETs, which results in the ordinary and expected result of boosting carrier (hole) mobility and improve performance. *See* Section V.F above; James, Ex.1012, 2. Accordingly, the combination of Saito825, Fukutome, and James,

including the exemplary embodiment illustrated in Figure M below, exemplifies the application of established processes to achieve routine and anticipated results.

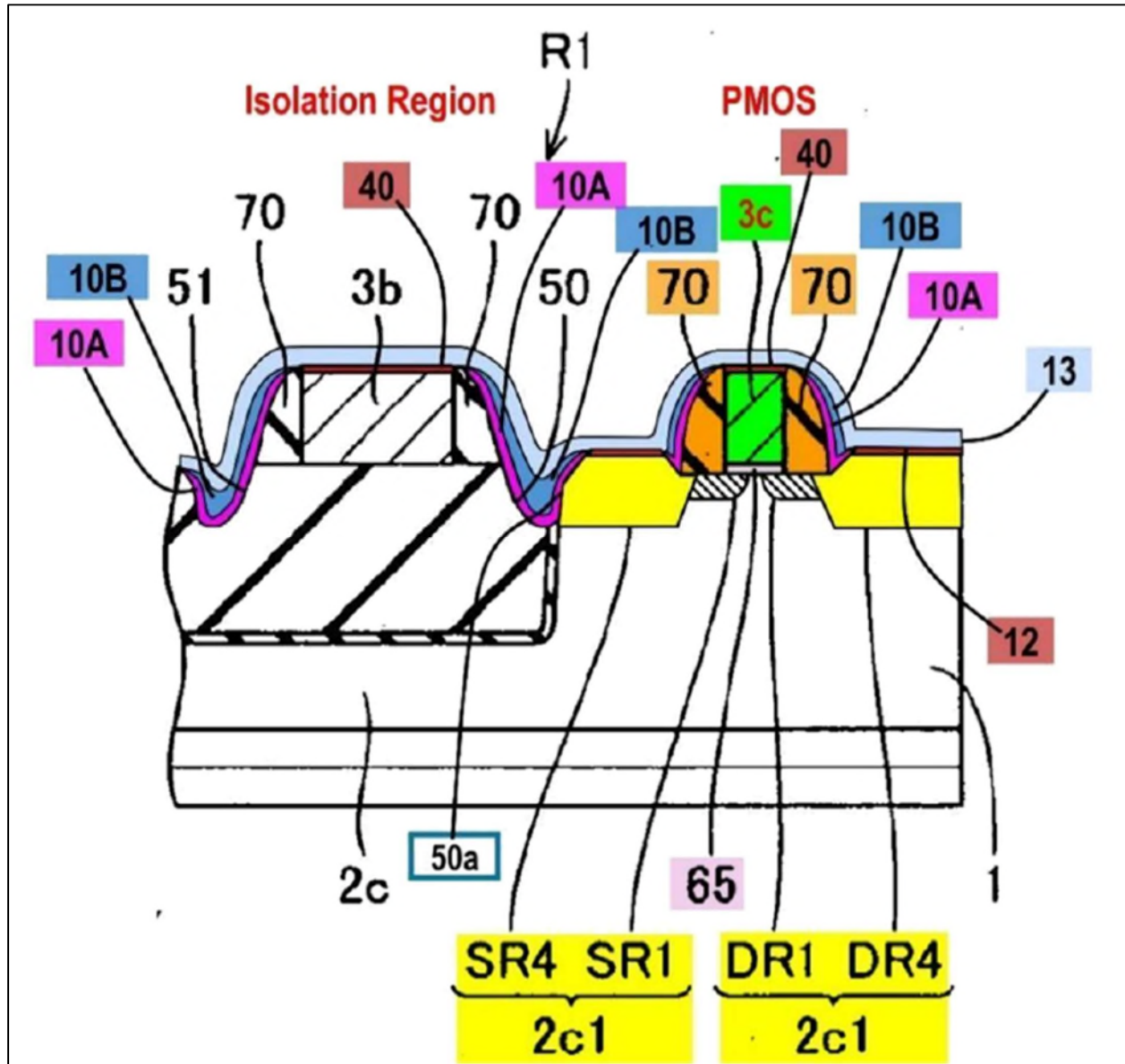


Figure M

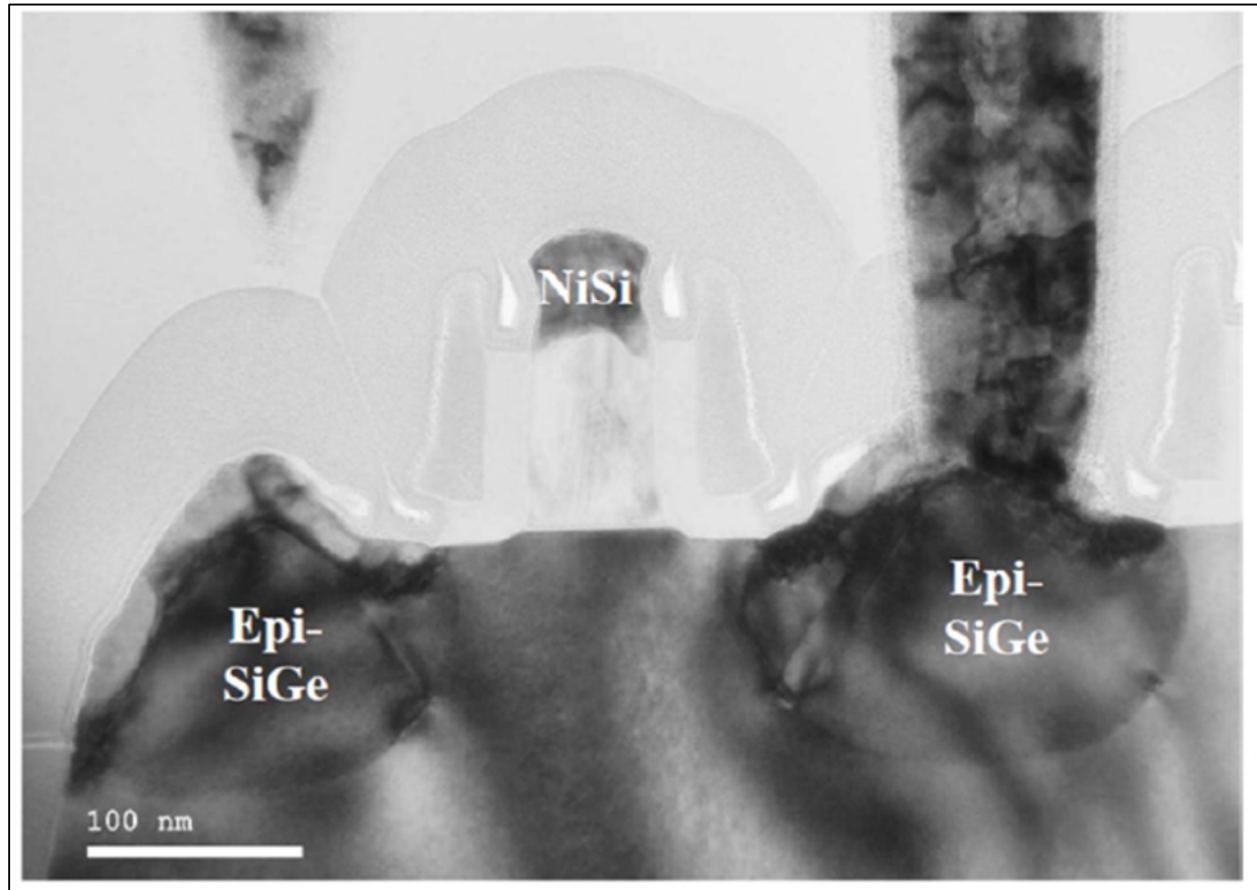
354. Additionally, a POSITA would expect success in modifying Saito825's SiN insulating layer 13 to induce tensile stress. *See* James, Ex.1012, 2, 5. A POSITA

would have to do nothing more than use conventional steps of deposit Saito825's SiN insulating layer 13 under well-known conditions known to have the SiN insulating layer 13 to cause a tensile stress in the gate length direction. *See* Jung, Ex.1529, ¶¶[0090], ¶¶[0099]- [0100], Tbl. V; Saito825, Ex.1010, ¶¶[0080], [0120]-[0121], FIGS. 12, 18; James, Ex.1012, 2, 5 ("It is perhaps ironic that stress in silicon nitride layers, a problem in previous process generations, has now been harnessed to apply strain. So far, it has been used only to provide tensile stress to enhance NMOS performance (at least in the three examples we have shown)"); Alvarez, Ex.1006, ¶¶[0054], [0065], [0069], Tbl. 1 (stress-insulating material 216 imparts tensile stress); Hsu823, Ex.1506, ¶[0039] (preferable to apply a tensile insulating layer across both NMOS and PMOS devices because "the performance of PMOS devices can be easily improved with SiGe stressors, while the performance of NMOS devices is relatively difficult to improve"); Morin-2007, Ex.1528, 355-56; Bohr, Ex.1527, ¶¶[0038]-[0039], FIG. 6. Indeed, James acknowledges that the tensile CESL, in addition to being successfully employed in commercial devices before the invention of the '425 patent, also "has the noteworthy convenience that it can be accomplished by process tuning, and involves no extra cost for either capital equipment or special substrates." James, Ex.1012, 5.

355. Thus, it is my opinion that a POSITA would have recognized that depositing Saito825's silicon nitride insulating layer 13 such to cause a tensile stress

(as James discloses) would have achieved the ordinary and expected result of improving carrier (electron) mobility and overall improve performance of Saito825's NMOS transistors N1-N4. James, Ex.1012, 2; *See also* Section V.F. above. Therefore, the combination of Saito825, Fukutome, and James merely constitutes the application of established processes to achieve typical and anticipated results.

356. James confirms this—A POSITA would have reasonably expected to succeed with incorporating raised and faceted epitaxial SiGe source/drain regions into Saito825's pFETs structure while, simultaneously, making Saito825's SiN insulating film 13 such that it causes a tensile stress. Intel had used this combination in its s high-volume 90nm process (codenamed Prescott) in countless commercial products. James's Fig. 6 below shows a micrograph of such a prior-art pFET.



James, Ex.1012, Fig. 6

357. Predictably, this combination improved both nFETs and pFETs. *See* James, Ex.1012, 2-3 (“Localized tensile stress is applied to the channels of NMOS devices by a highly stressed nitride sealant layer This increases electron mobility by ~10%. . . . The PMOS transistors (Figure 6) use epitaxial SiGe source/drains to create compressive stress – this improves hole mobility by as much as 50%. . . . Crystalline facets form raised [SiGe] source/drains, reducing the series resistance. The tensile stress from the nitride layer is counteracted by the compressive effect.”); *See* Section V.F above. James further demonstrates that the combination was well

known and in commercial use before the '425 patent and that a POSITA also would have reasonably expected this to operate as expected when applied to Saito825's MISFETs N1-N4 and P1-P2.

358. In summary, it is my opinion that a POSITA would have found the Saito825-Fukutome-James combination obvious because it is an example of the following:

- It combines known prior art elements (Saito825's SRAM cell with epitaxial SiGe source/drain regions, as Fukutome and James both disclose, and a tensile-causing silicon nitride CESL, as James discloses) according to known methods (well known epitaxial SiGe growth and tensile SiN deposition techniques) to yield predictable results (SiGe source/drain regions that impart compressive stress to pFET channels add a silicon nitride layer that imparts tensile stress to nFET channels).
- It simply substitutes one known element for another (e.g., substituting Fukutome's epitaxial SiGe source/drain regions for Saito825's non-epitaxial deep source/drain regions, and substituting James's tensile SiN CESL for Saito825's silicon nitride insulating layer 13) to obtain predictable results (SiGe

source/drain regions that impart compressive stress to pFET channels and a silicon nitride layer that imparts tensile stress to nFET channels).

- It uses known techniques (epitaxial growth of SiGe source/drain regions, as Fukutome and James disclose, and a tensile silicon nitride CESL, as James discloses) to improve similar devices (the MISFETs in Saito825's SRAM cell) in the same way (e.g., by using strain engineering to boost carrier mobility in Saito825's pFETs and nFETs).
- It applies known techniques (epitaxial growth of SiGe source/drain regions, as Fukutome and James disclose, and a tensile silicon nitride CESL, as James discloses) to a known device ready for improvement (the MISFETs in Saito825's SRAM cell) to yield predictable results (improved carrier mobility in Saito825's pFETs and nFETs).
- It applies a known teaching, motivation, or suggestion in the prior art (e.g., using epitaxial SiGe source/drain regions to improve pFET performance, as Fukutome and James teach, and a tensile SiN CESL, as James teaches, to improve nFET performance) that would have led a POSITA to modify

Saito825 according to, or to combine Saito825 with, the teachings of Fukutome and James to arrive at the claimed invention.

2. Independent Claim 1

a. Preamble: “A semiconductor device”

359. Saito825 discloses a semiconductor device. Saito825’s invention is directed toward “a semiconductor device and its manufacturing method.” Saito825, Ex.1010, ¶¶[0002], [0023]-[0026], FIGS. 1, 12, 21. “FIG. 1 is a plan view of the memory cell of the semiconductor device (static semiconductor memory device).” Saito825, Ex.1010, ¶[0028]; *see also* Saito825, Ex.1010, ¶[0049] (“FIG. 1 is the plan view of memory cell 1 of [the] full CMOSSRAM” memory device), FIG. 1. Saito825’s FIGS. 12 and 21 are described as “cross-sectional view[s]” of the “semiconductor device.” Saito825, Ex.1010, ¶¶[0039], [0048]; *see also* Saito825, Ex.1010, FIGS. 12, 21.

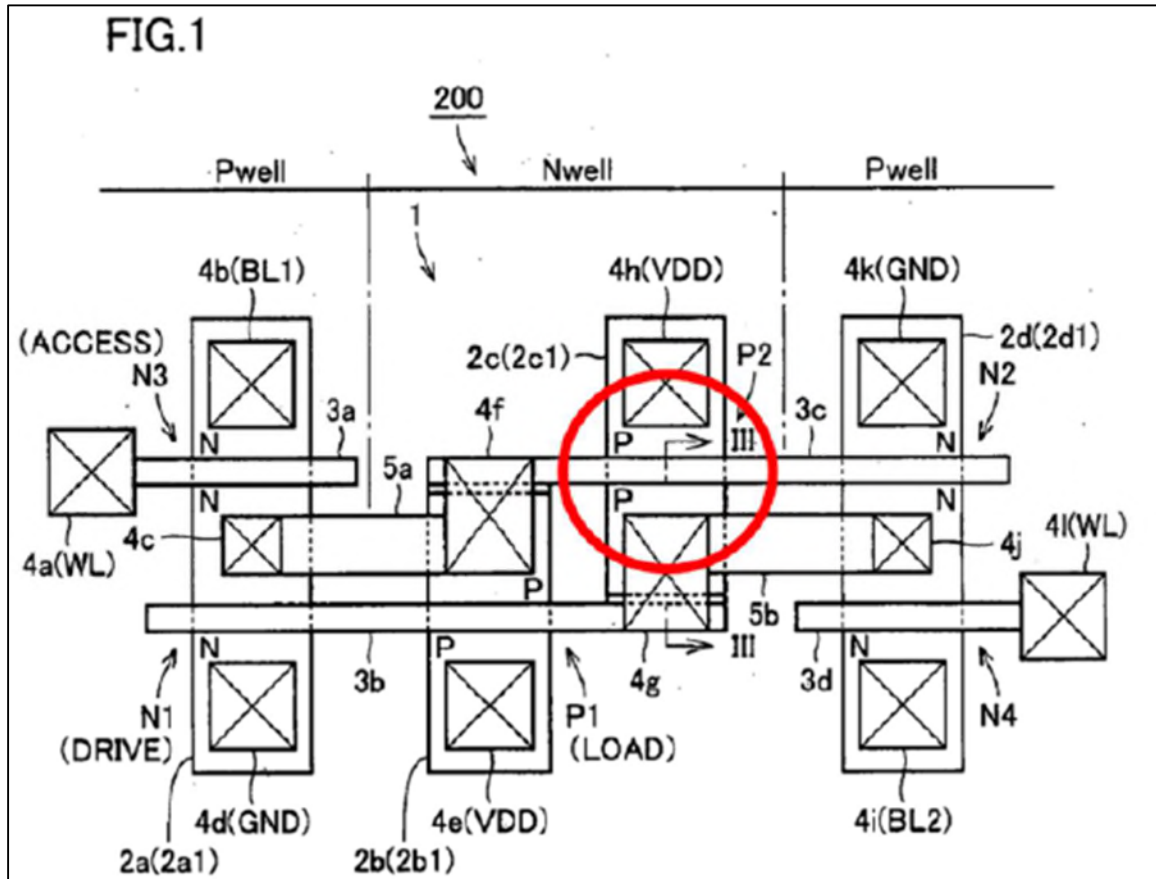
b. Element 1[a]: “a first MIS transistor . . . includ[ing]:”

360. Saito825 discloses a first MIS transistor. Specifically, Saito825 discloses a PMOS transistor P2 in active region 2c. *See* Saito825, Ex.1010, ¶[0057], FIGS. 1, 3, 12, 21.

361. Describing the first MIS transistor, Saito825 states “[s]econd access PMOS transistor P2 is formed in the intersection part of impurity diffusion region

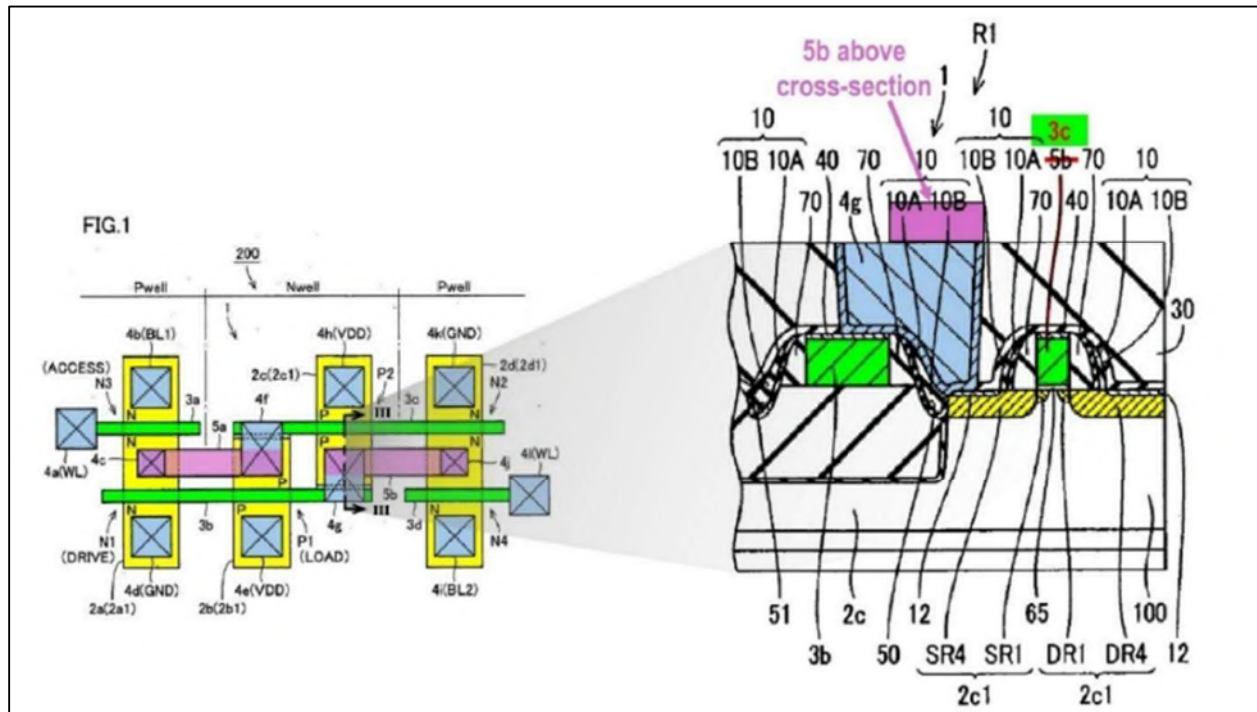
2c1 comprising the region used as a source/drain, and polysilicon wiring 3c.”

Saito825, Ex.1010, ¶[0066]. See annotated Saito825, Ex.1010, FIG. 1 below:



Saito825, Ex.1010 FIG. 1 (annotated)

362. As explained above in Section X.C.1, a POSITA would have readily realized that Saito825 has a small typographical error where polysilicon wiring 3c is incorrectly identified as polysilicon wiring “5b” in Saito825 FIGS. 12-21. The figures below reflect the correction of the typographical error. See Section X.C.1



Saito825, Ex.1010 FIG. 1

**Saito825, Ex.1010 FIG. 12
(excerpted, annotated)**

363. A POSITA would have found the Saito825-Fukutome-James combination obvious, including the embodiment shown in Figure M below. *See also* Section X.C.1.a., Claim elements [1B]-[1J], below.

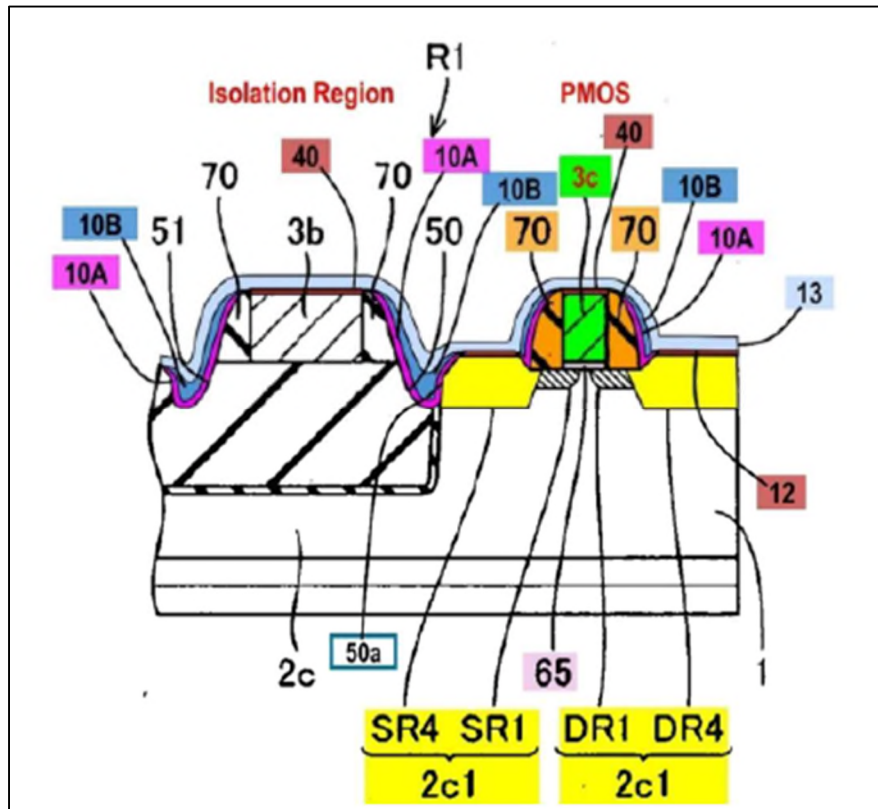


Figure M

c. Element 1[b]: “a first gate insulating film formed on a first active region in a semiconductor substrate”

364. Saito825 discloses a first gate insulating film formed on a first active region in a semiconductor substrate. Saito825 specifically identifies these elements: “gate insulating film 65,” “active region 2c,” and a “semiconductor substrate 100.” Saito825 ¶[0051] (“[O]n the main front surface of semiconductor substrate 100 in which active region 2c is located, gate insulating film 65 . . . [is] formed.”); *See also* Saito825, Ex.1010, FIG. 21. As Figure M of the Saito825-Fukutome-James combination is shown below, the gate insulating film 65 (highlighted light purple) is formed on first active region 2c of PMOS transistor P2. *See* Section X.C.1.a. above.

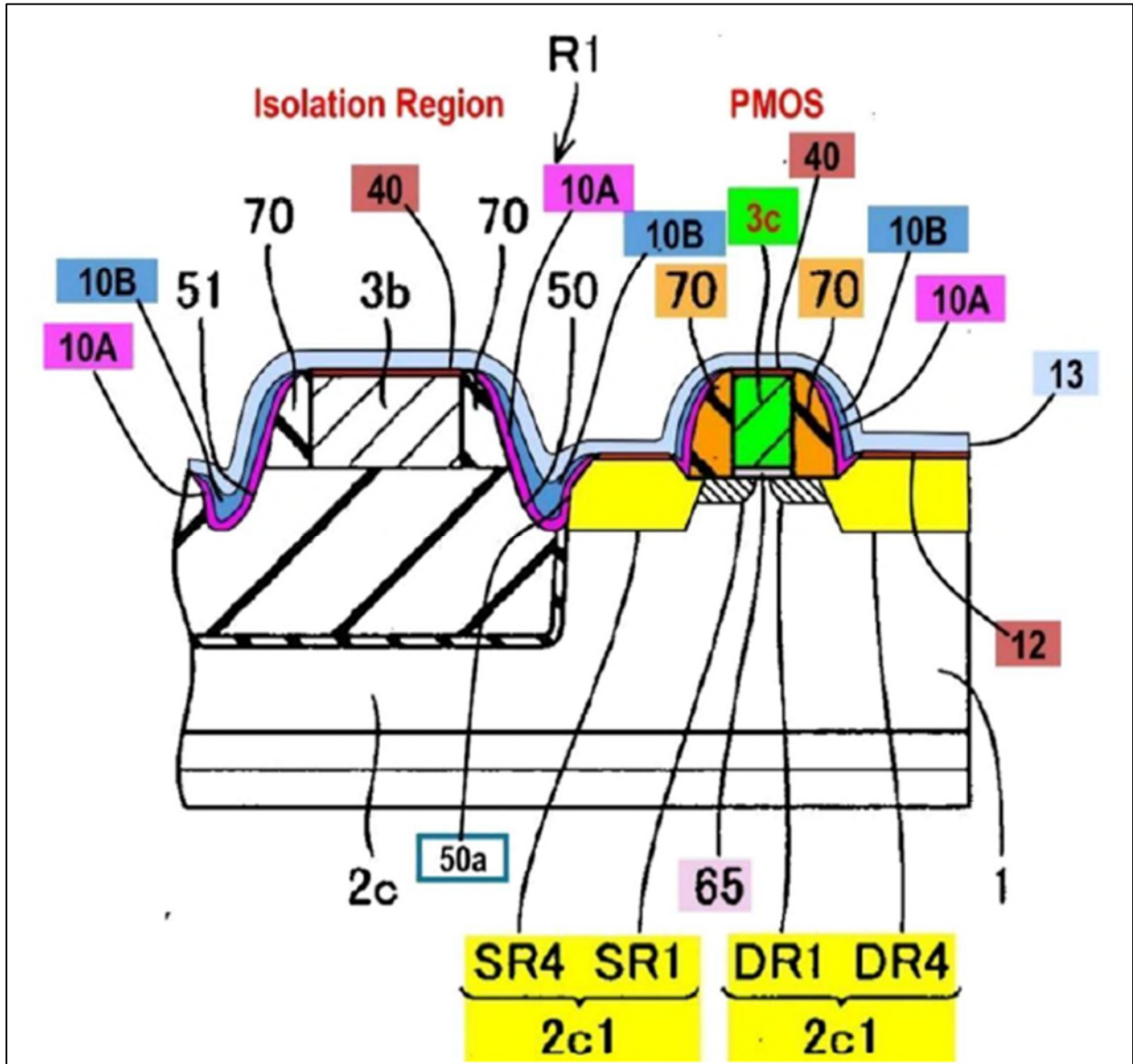


Figure M

- d. Element 1[c]: “a first gate electrode formed on the first gate insulating film”**

365. Saito825 discloses a first gate electrode formed on the first gate insulating film. Saito825 specifically identifies these elements: “active region 2c,” “gate insulating film 65,” and “polysilicon wiring 5b [sic:3c] formed on the upper

surface of this gate insulating film 65, and impurity diffused layer 2c1 located in the both sides [sic] of this polysilicon wiring 5b.” Saito825, Ex.1010, ¶[0051]; *See also* Saito825, Ex.1010, FIG. 12. Saito825 further details that “[s]econd access PMOS transistor P2 is formed in the intersection part of impurity diffusion region 2c1 comprising the region used as a source/drain, and polysilicon wiring 3c.” Saito825, Ex.1010, ¶[0066]; *see also* Saito825, Ex.1010, ¶[0124], FIGS. 1, 12.

366. As Figure M of the Saito825-Fukutome-James combination is shown below, polysilicon wiring 3c (highlighted green) is formed on gate insulating film 65 (highlighted light purple). *See* Section X.C.1.a. above.

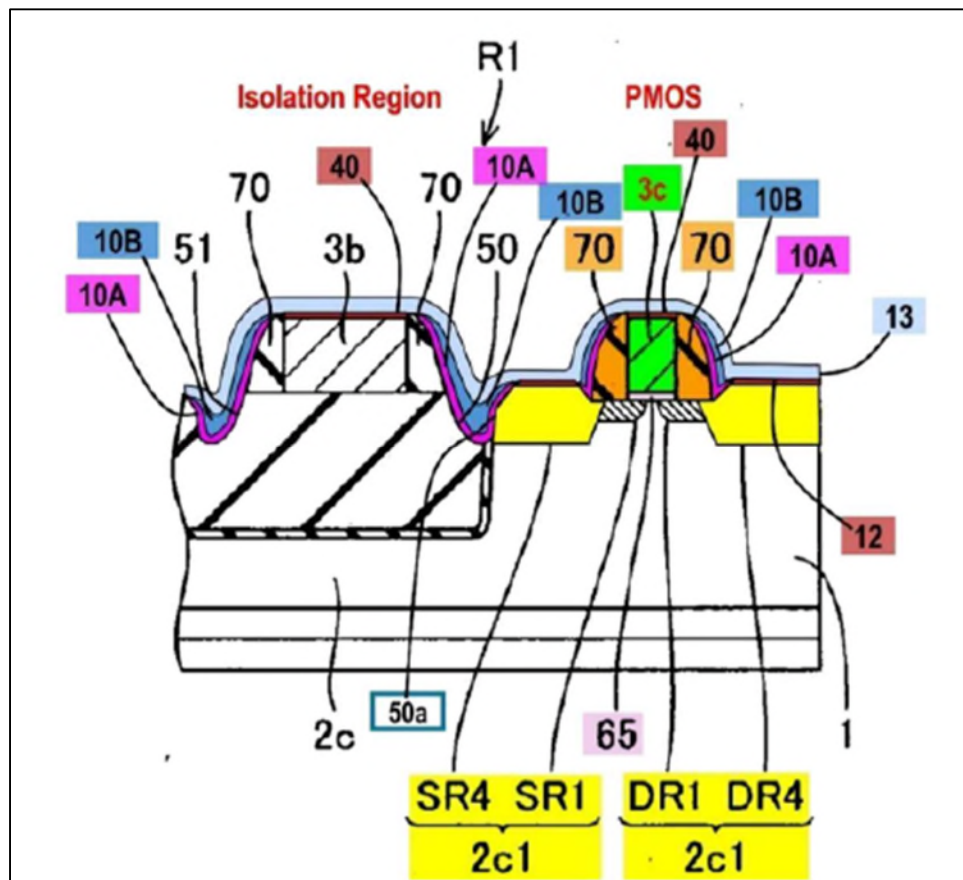


Figure M

e. Element 1[d]: “a first sidewall spacer formed on a side surface of the first gate electrode”

367. Saito825 discloses a first sidewall spacer formed on a side surface of the first gate electrode. Saito825 specifically teaches “sidewall 70 [that] is formed on the both [sic] side surfaces of . . . polysilicon wiring 5b [sic:3c], and polysilicon wiring 3b.” Saito825, Ex.1010, ¶[0096]; *see also* Saito825, Ex.1010, FIG. 17. Saito825 further details that “[t]he sidewall [70] is formed also on the side surface of th[e] polysilicon wiring 3c.” This supports my opinion that a POSITA would have readily understood that Saito825 FIGS. 12-21 show polysilicon wiring 3c. Saito825, Ex.1010, ¶[0077]; *see also* Saito825, Ex.1010, ¶[0124]; Section X.C.1. above.

368. As Figure M of the Saito825-Fukutome-James combination is shown below, the first sidewall spacer 70 (highlighted orange) is formed on the side surfaces of the first gate electrode 3c (highlighted green). *See* Section X.C.1.a. above.

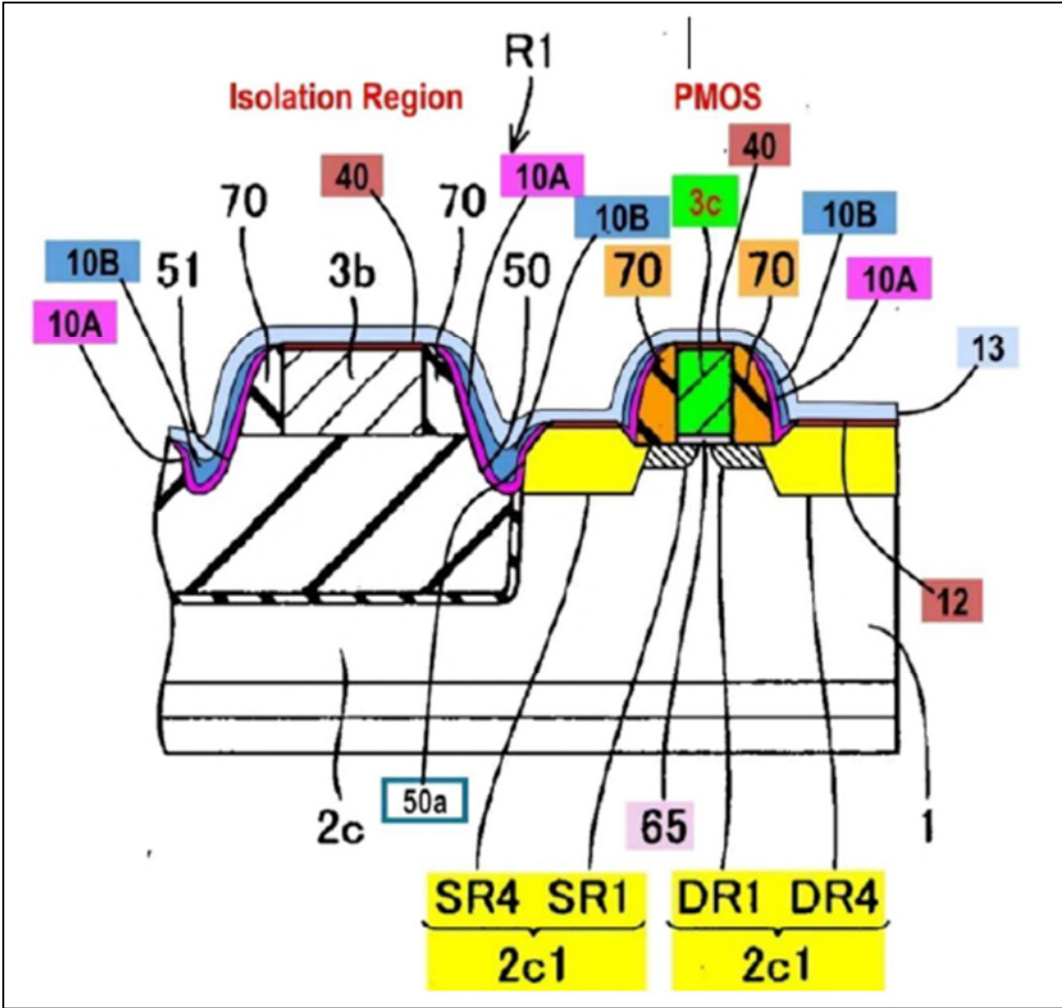


Figure M

- f. Element 1[e]: “a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region”**

369. The Saito825-Fukutome-James combination renders obvious a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which

includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region. Fukutome teaches “a SiGe layer with a Ge concentration of 3 to 30% is selectively epitaxially grown in each of the recesses [trenches] 10a and 10b.” Fukutome, Ex.1011, ¶[0098]; *see also* Fukutome, Ex.1011, ¶¶[0005], [0110]. As Figure M of the Saito825-Fukutome-James combination is shown below shows the epitaxial SiGe layers (highlighted yellow) of Fukutome into Saito825’s pFET structure. *See* Section X.C.1.a. above.

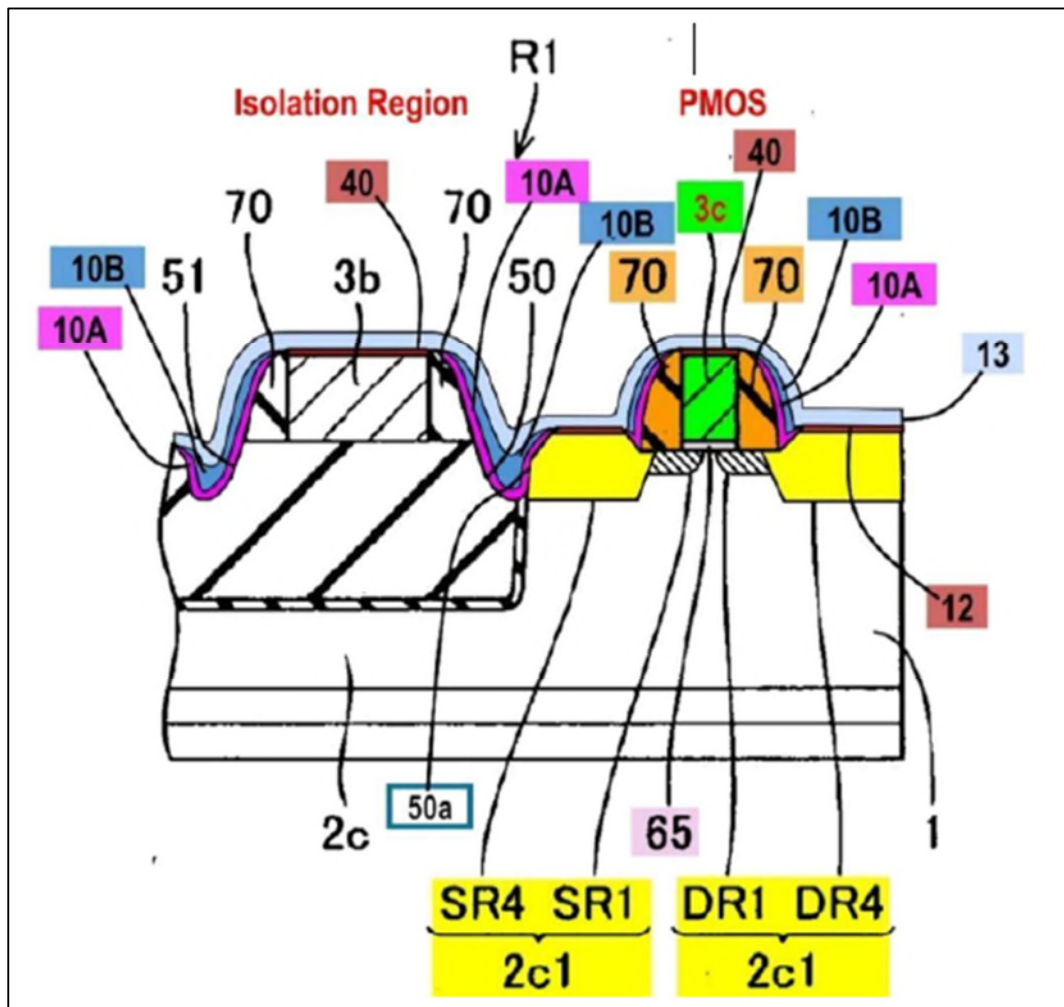


Figure M

370. Fukutome's SiGe layers cause compressive stress along the gate length direction in the channel region. Fukutome teaches that the reason for the compressive stress, as was well known in the prior art, is because the lattice spacing in the SiGe layers is larger than that of the silicon substrate. Fukutome, Ex.1011, ¶¶[0005], [0110] ("In the MOS transistor TR, [the] silicon lattice in the silicon substrate 10 is forcefully stretched so as to match the large lattice spacing of SiGe due to a mismatch between the lattice constant of the silicon substrate 10 and those of the source/drain material layers 18a and 18b, and stress in the directions of the arrows in the drawing [is] applied to a channel under the gate electrode 14c. As a result, compared to the case where stress is not applied, the mobility of carriers in the channel is improved, and the drive capability of the MOS transistor can be improved."). Fukutome's FIG. 5G indicates the compressive stress with arrows.

371. Both Saito825 and Fukutome source/drain region (including Fukutome's raised SiGe source/drains) are p-type. *See* Section X.C.1.a. above; Fukutome, Ex.1011, ¶[0102] ("[B]oron ions are implanted as p-type impurities into the source/drain material layers 18a and 18b In the case where in-situ doping is performed impurity implantation and heat treatment may be omitted."); Saito825, Ex.1010, ¶[0060] ("P type impurities, such as a boron, are selectively implanted into active regions 2b, 2c").

372. As Figure M of the Saito825-Fukutome-James combination is shown below, the SiGe silicon compound layer (highlighted yellow) of the source/drain region is formed in a trench provided in first active region 2c on a lateral side of the first sidewall spacer 70 (highlighted orange) which impart compressive stress to transistor P2 in a gate length direction of the channel region. *See* Section X.C.1.a. above; Fukutome, Ex.1011, ¶¶[0089]-[0102], FIGS. 5D-5G.

- g. Element 1[f]: “a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress”**

373. The Saito825-Fukutome-James combination renders obvious a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress. Saito825 discloses a “insulating film 13” that “consists of a plasma nitride (SiN).” As shown in Saito825 FIG. 21, insulating film 13 is deposited over the entire SRAM cell. *See* Section X.C.1.a.(1)(b) above; Saito825, Ex.1010, ¶¶[0080], [0091], [0120], [0124], FIGS. 12, 21.

374. James teaches that modifying Saito825’s insulating film 13 to cause a tensile stress would have been obvious. *See* Section X.C.1.a. above. It was well understood in the art that doing so would “increase [] electron mobility” in NMOS transistors N1-N4, for example, with “no extra cost for either capital equipment or

special substrates.” James, Ex.1012, 2, 5; *See also* James, Ex.1012, Fig. 6. The two stresses are opposite and are contrast to each other: compressive stress exerted by the epitaxial SiGe source/drain layers and tensile stress of insulating film 13.

375. As Figure M of the Saito825-Fukutome-James combination is shown below, tensile stress insulating film 13 (highlighted light blue) is formed on first active region 2c such that it covers the first sidewall spacer 70 (highlighted orange), the first gate electrode 3c (highlighted green), and the first source/drain region (epitaxial SiGe layers, highlighted yellow). *See* Section X.C.1.a. above.

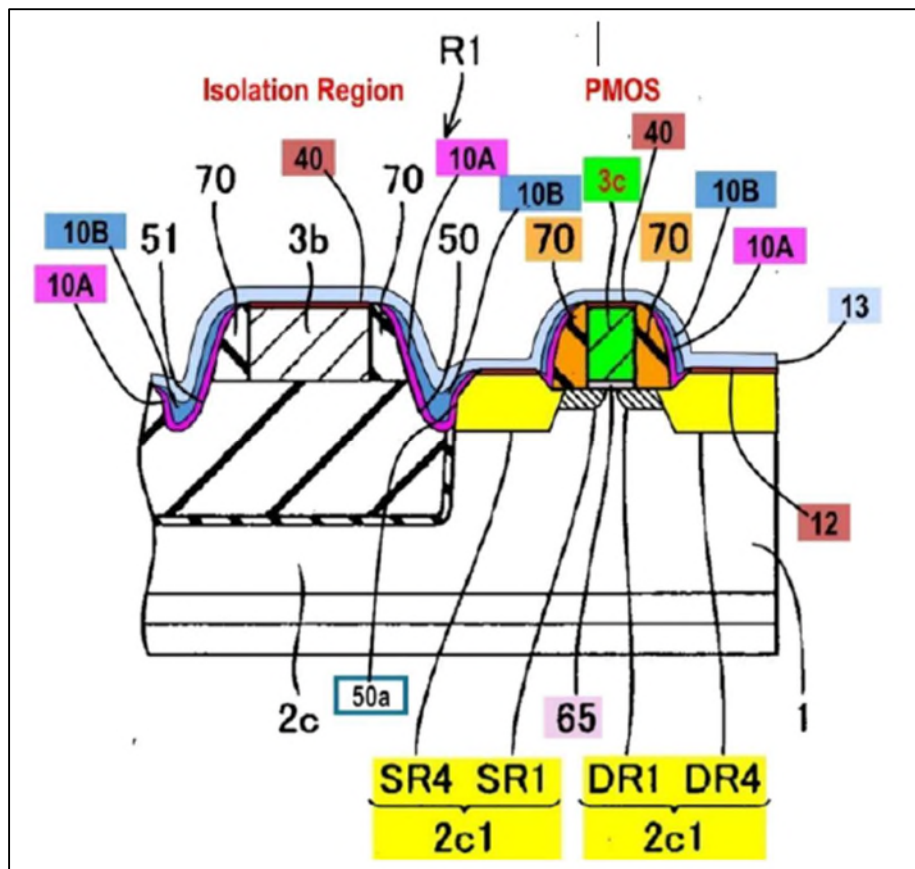
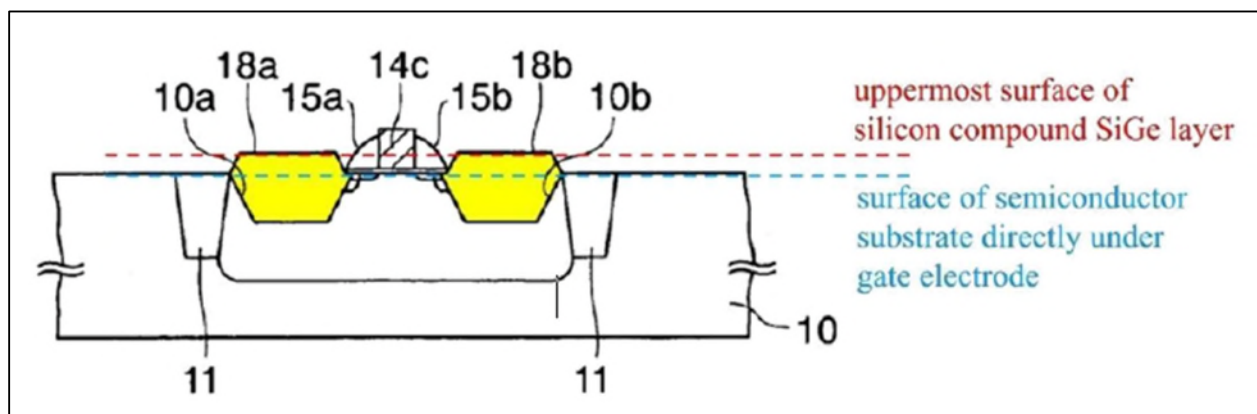


Figure M

- h. Element 1[g]: “an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode”**

376. The Saito825-Fukutome-James combination renders obvious an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode. Fukutome teaches that the epitaxial SiGe source/drain layers extend to a height above the top surface of the substrate. *See* Sections X.C.1.a. and X.C.2.f. above.



Fukutome, Ex.1011 FIG. 5E (annotated)

377. Fukutome shows and teaches “the distances between the bottom surface of the n-well 12 and the upper surfaces of the source/drain material layers 18a and 18b are increased by forming the upper surfaces of the source/drain material layers 18a and 18b at positions higher than the surface of the silicon substrate 10 as in the present embodiment.” Fukutome, Ex.1011, ¶[0100]; *see also* Fukutome, Ex.1011, FIG. 5E. These raised SiGe layers help facilitate strain transfer to the pFET channel

¶[0100], FIG. 5E; Sections V.F. and X.C.1.a. above.

higher than the top surface of the substrate (blue line).¹⁵ See Section X.C.1.a. above.

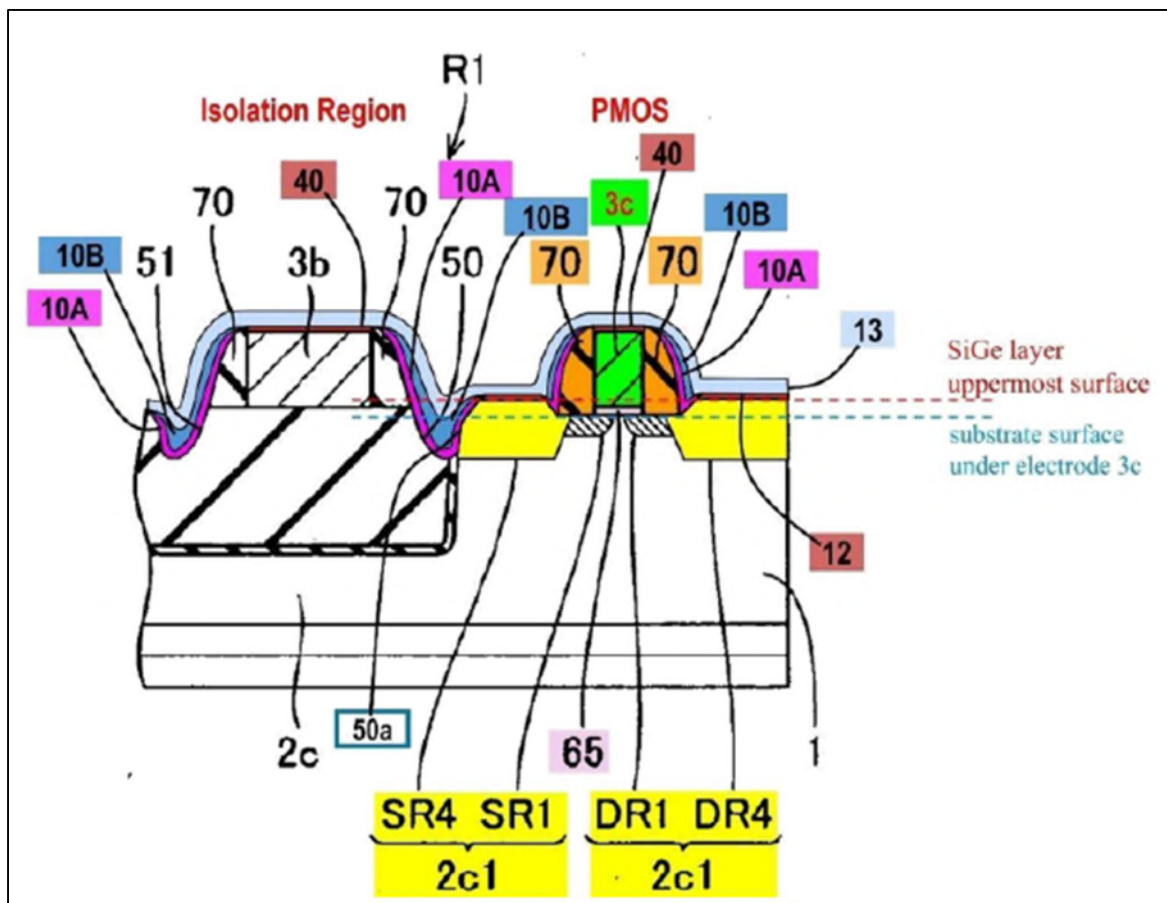
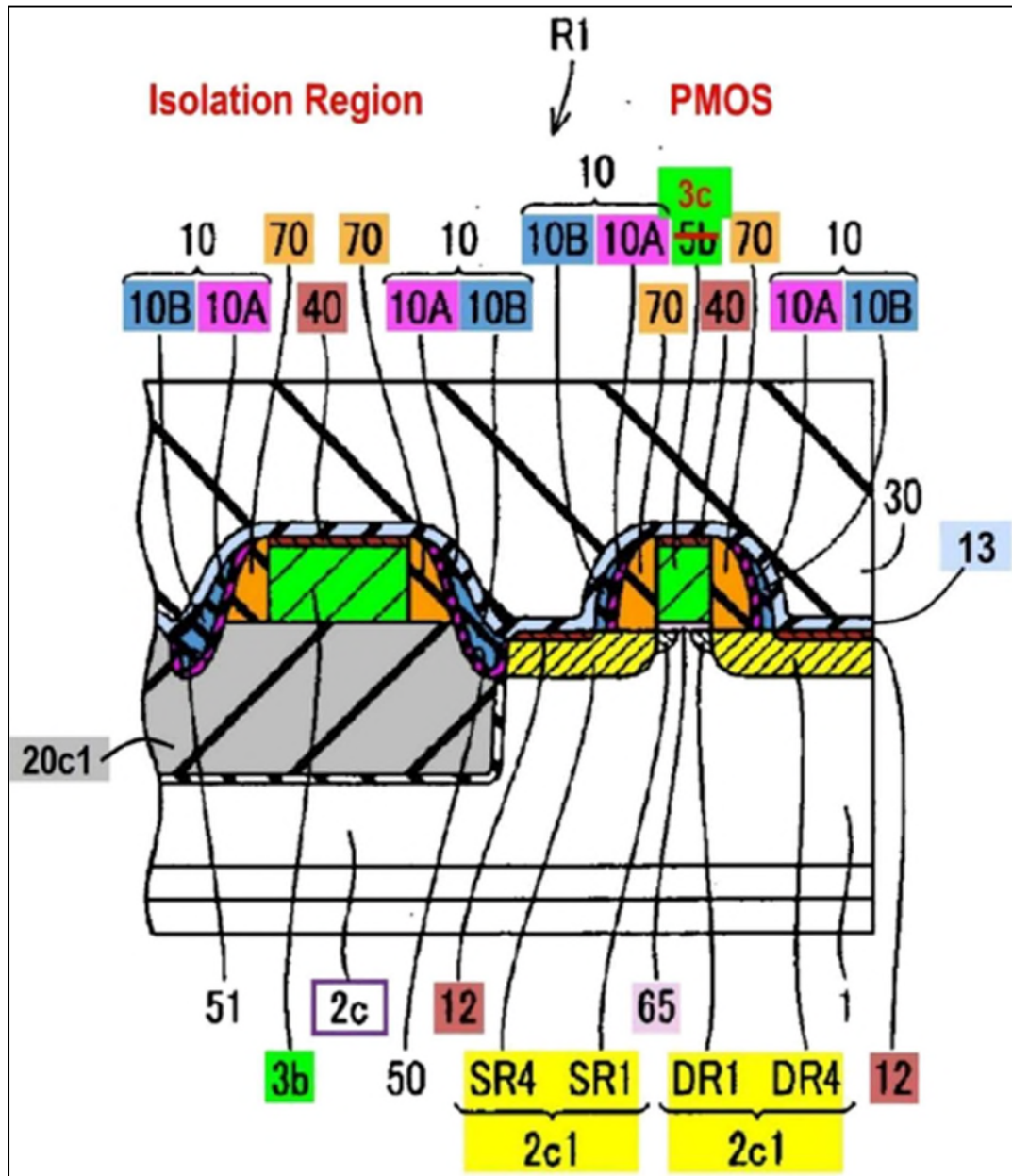


Figure M (further annotated)

formed. *See* Fukutome, Ex.1011, FIG. 5F; Section X.C.1 above.

i. Element 1[h]: “a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer”

379. Saito825 discloses a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer. Saito825 discloses forming an insulating film 10A over the semiconductor device surface, including in the recesses 50/51 of Saito825’s isolation region 20c1 before depositing the tensile CESL film 13 (see Section X.C.2.g. and (Element 1[f]) above), Saito825, Ex.1010, ¶¶[0074], [0078], [0082], [0104], [0107], [0113], FIGS. 6-12, 18-21. Saito825 demonstrates that after etching to expose the gate electrode and source/drain regions for silicidation, the first insulating film 10A (highlighted in magenta below) remains in the recesses 50/51 and along the edges of sidewalls 70 (highlighted in orange below). *See* Saito825, Ex.1010, ¶¶[0074], [0078], [0082], [0104], [0107], [0113], FIGS. 7-12, 18-21.



Saito825, Ex.1010 FIG 21 (excerpted, annotated)

380. Saito825's Insulating film 10A covers "the internal surfaces of recess 50, the front surface of impurity diffused layer 2c1, and active region 2c located under impurity diffused layer 2c1." Saito825, Ex.1010, ¶[0076]; *see* Saito825, Ex.1010, ¶¶[0078], [0082], ¶[0104], FIGS. 6-12, 18-21. The Insulating film 10A is

made of silicon oxide and “formed so that the front surface of this recess 50 may be covered” and “formed on the side surface of sidewall 70.” Saito825, Ex.1010, ¶[0074]; *see also* Saito825, Ex.1010, ¶[0076], FIG. 18. Saito825’s FIGS. 19-21 illustrate that insulating film 10A remains in the recesses 50/51 and on the gate sidewalls 70, even after etching to reveal the top surfaces of the source/drain regions and gate electrodes for silicidation. Saito825, Ex.1010, ¶¶[0075], [0089], [0107]-[0114], FIGS. 19-21.

381. As explained in Sections X.C.1.a. and V.G above, a POSITA would have found it obvious that after depositing insulating film 10A into the spaces between the raised SiGe facets and sidewalls 70, it would remain there in the final processing steps. Thus, insulating film 10A, corresponds to the stress-relief film in a space between the raised SiGe silicon compound layer and the first sidewall spacer 70 in the Saito825-Fukutome-James combination. *See* Saito825, Ex.1010, ¶[0074]; The ’425 patent, Ex.1001, 12:59-13:8.

382. Because Saito825 teaches that the first insulating film 10A made of silicon oxide, remains in the recess 50 and on the sidewalls 70, a POSITA would have recognized that first insulating film 10A would have formed in, and remained in, the space between the raised SiGe facets and sidewalls 70 in the Saito825-Fukutome-James combination, as was well known when depositing such films over contoured surfaces like this. *See* Sections X.C.1.a. and V.G above; Miyashita,

Ex.1435, ¶¶[0052]-[0053], FIGS. 1U-1W; Murthy556, Ex.1430, 2:15-24, 9:10-44, FIGS. 2, 7-9; Fukutome, Ex.1011, FIG. 5G (showing CESL 20 forming in [the] space between the facets of SiGe layers 18a/18b and sidewalls 15a/15b); Wu922, FIG. 7 (showing CESL 66 forming in the space between the facets of SiGe layers 58 and sidewalls 501A/512A).

383. It is my opinion a POSITA would have found it obvious that Saito825's silicon oxide insulating film 10A corresponds to the stress-relief film in the Saito825-Fukutome-James combination because it was well known in the prior art that silicon dioxide layers buffer stress. *See* Sections V.G and X.C.1.a. above; Murthy556, Ex.1430, 8:59-9:43, FIGS. 7-9 (illustrating an oxide buffer positioned between the raised SiGe facet and the electrode, designed to cushion the nitride layer located above the oxide.); Alvarez, Ex.1006, ¶¶[0049], [0066], [0068], [0077], FIGS. 9-11; Baik, Ex.1433, ¶[0037], FIG. 1F. Moreover, Saito825's instruction that the silicon oxide film 10A remains in the recesses and on the sidewalls even after etching is also what the '425 patent describes with respect to stress-relief film 28a. *Compare* Saito825, Ex.1010, ¶[0074], FIG. 21, and Figure M (below), *with* The '425 patent, Ex.1001, 12:59-13:8, FIG. 6B (item 28a); *See also* Section X.C.1.a. above.

384. As Figure M of the Saito825-Fukutome-James combination is shown below, Saito825's insulating film 10A (first stress-relief film, highlighted magenta) is formed in a space between the raised facets of the SiGe silicon compound layer

(highlighted yellow) and the first sidewall spacer (highlighted orange). *See* Section X.C.1.a. above; Saito825, Ex.1010, FIGS. 12, 21.

j. Element 1[i]: “the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween”

385. Saito825 discloses the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween. Saito825’s insulating film 10 is formed on the side of the polysilicon gate electrode with the sidewalls 70 formed in between. *See* Sections X.C.1.a., X.C.2.i., and IX.D.1.b(10) above; Claim elements [1H] and above.

386. As Figure M of the Saito825-Fukutome-James combination is shown below, the first stress-relief film 10A (highlighted magenta) is formed on the side of the first gate electrode (highlighted green) and the first sidewall spacer 70 (highlighted orange) is interposed between them. *See* Section X.C.1.a. above; Saito825, Ex.1010, FIGS. 12, 19-21.

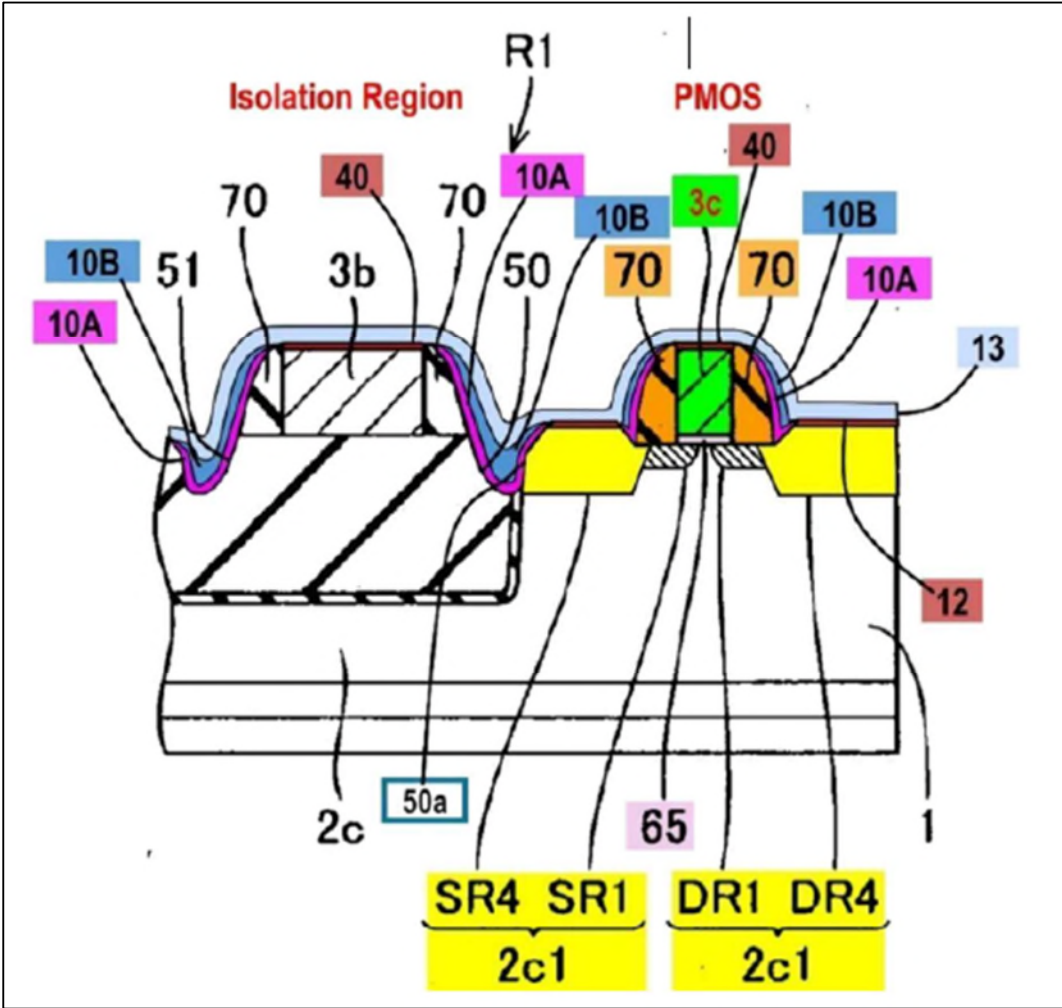


Figure M

- k. Element 1[j]: “the first stress-relief film is not in direct contact with the side surface of the first gate electrode”**

387. Saito825 discloses the first stress-relief film is not in direct contact with the side surface of the first gate electrode. Saito825's insulating film 10 is formed on the sides of the sidewalls 70 and are therefore not directly in contact with the side surfaces of the polysilicon gate electrode. *See* Sections X.C.1.a., X.C.2.i., and IX.D.1.b(10) above; Claim elements [1H] and [1I] above.

388. As Figure M of the Saito825-Fukutome-James combination is shown below, the first stress-relief film 10A (highlighted magenta) is not in direct contact with the side surfaces of the first gate electrode (highlighted green). *See* Section X.C.1.a. above.

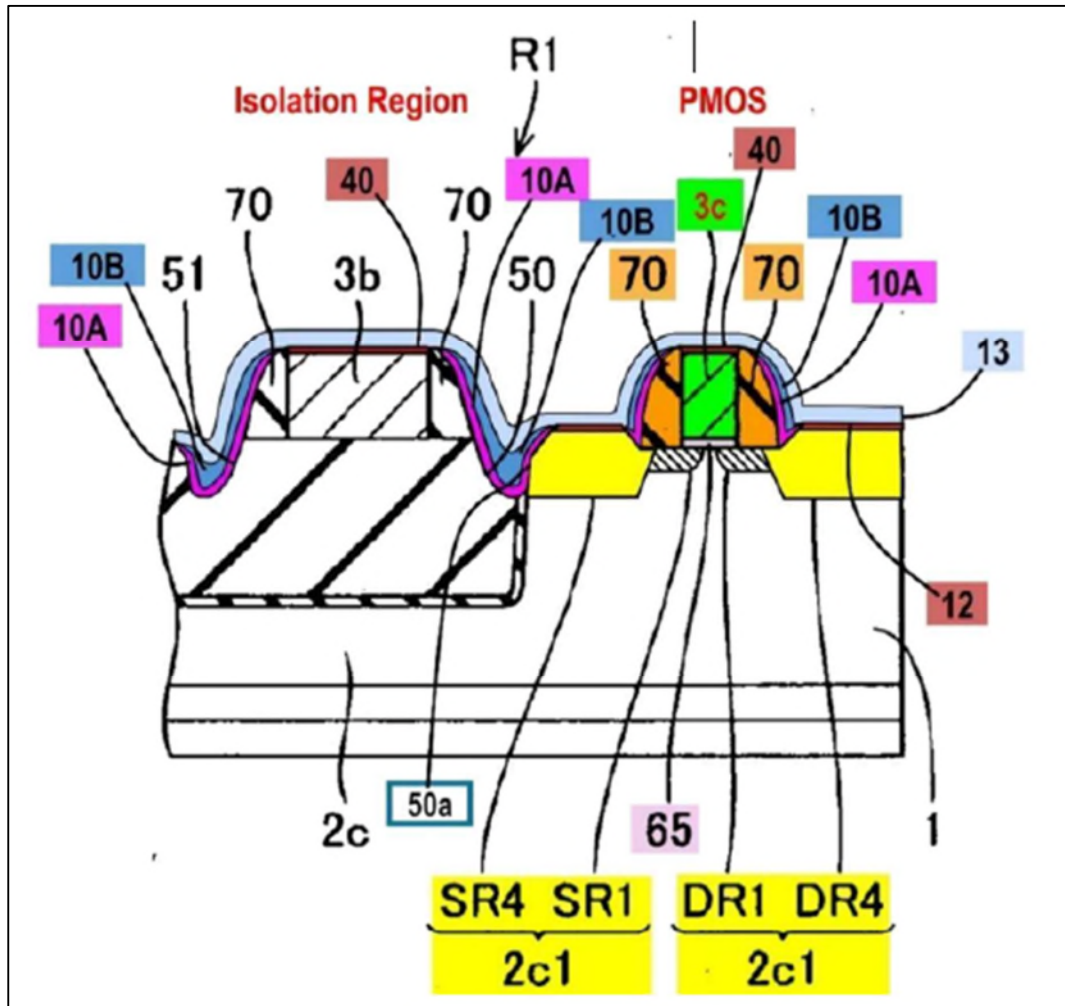


Figure M

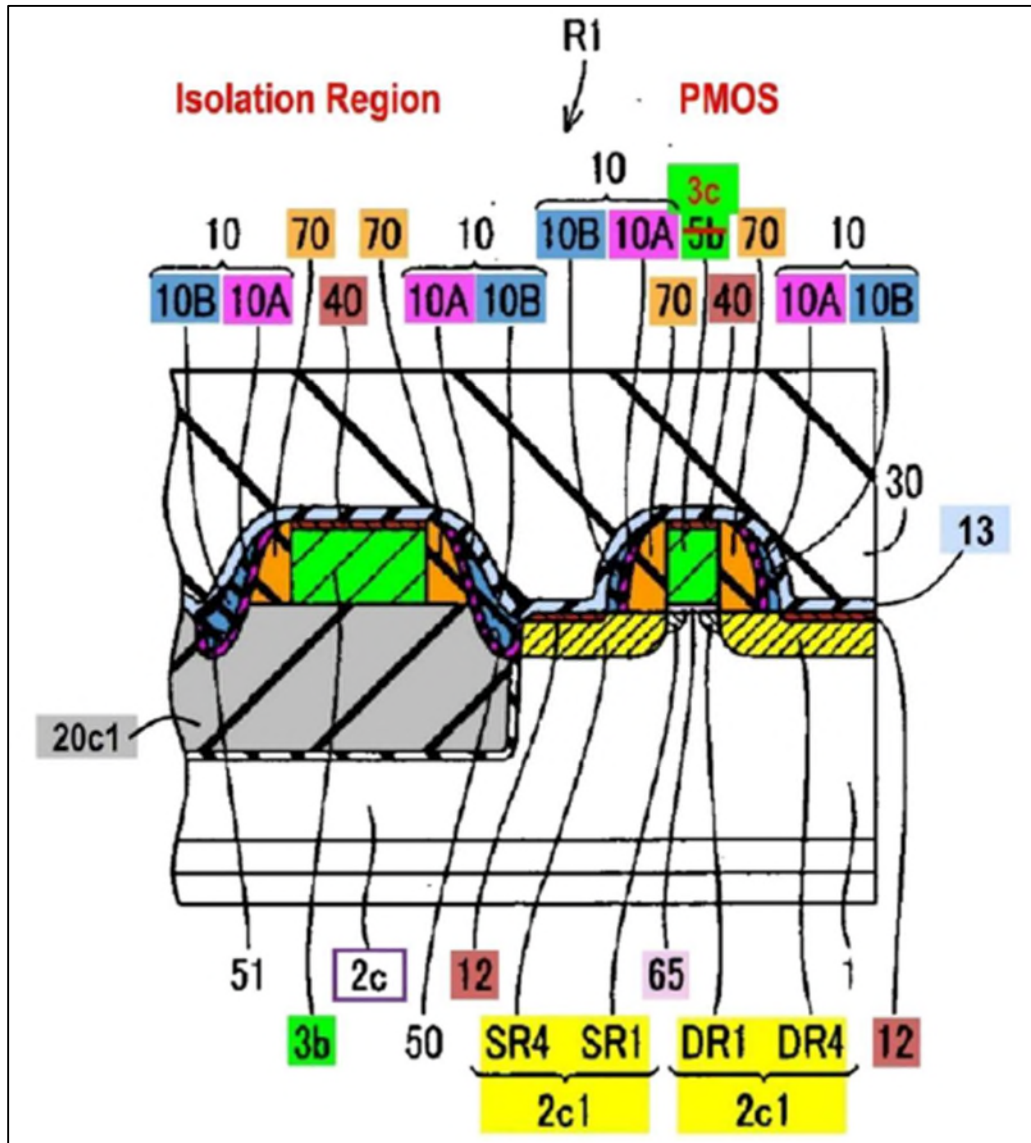
3. Dependent Claim 3

- a. Claim 3: “the semiconductor device of claim 1, further comprising: a first silicide layer formed on the first gate electrode; and a second silicide layer formed on the first source/drain region which includes the silicon compound layer.”**

389. In my opinion, the Saito825-Fukutome-James combination renders claim 3 obvious. First, The Saito825-Fukutome-James combination renders the semiconductor device of claim 1 obvious for the same reason explained in Sections X.C.2.a-k. above.

390. Saito825 further discloses a silicide film 40 (first silicide layer) formed on the polysilicon wirings and a silicide film 12 (second silicide layer) formed on source/drain regions 2c1 of PMOS transistor P2. Saito825, Ex.1010, ¶¶[0077], [0117], FIGS. 12, 20-21. Before the silicides are formed, first “metallic films, such as cobalt (Co), are deposited,” “heat treatment” is applied, and then “silicide films 12 and 40 are formed,” such that “silicide film 12 is formed on the front surface of impurity diffused layer 2c1” and “[s]ilicide film 40 is formed on the upper surface of polysilicon wiring 5b [sic:3c] and 3b” Saito825, Ex.1010, ¶¶[0116]-[0117], *see also* Saito825, Ex.1010, ¶[0077] (“On the main front surface located in the opposite side with polysilicon wiring 3b, polysilicon wiring 3c shown in FIG. 1 is formed to this silicide film 12 . . . on the main front surface of active region 2c.”), FIGS. 12, 20-21.

391. Annotated version of Saito825's FIG. 21 below shows both that the first silicide film 40 (highlighted red) is formed on the polysilicon wiring 5b [sic:3c] (highlighted green), and that the second silicide film 12 (also highlighted red) is formed on the source/drain regions 2c1 (highlighted yellow) of PMOS transistor P2.



Saito825, Ex.1010, FIG. 21 (excerpted, annotated)

392. A POSTA would integrate Fukutome's epitaxial SiGe source/drain regions into Saito825's PMOS transistors P1 and P and reasonably recognize that a silicide film 12 would form on the epitaxial SiGe regions (as taught by Fukutome) in the same manner as it forms on Saito825's non-epitaxial source/drain regions SR4 and DR4. Additionally, silicide film 40 would form on the polysilicon wirings 3b/3c, consistent with Saito825's description. *See* Sections X.C.1.a. and X.C.2 above. Fukutome also teaches the forming of silicide layers as well. *See* Fukutome, Ex.1011, ¶¶[0103]-[0104], FIGS. 5E-5G.

393. In Figure M, the combination of Saito825-Fukutome-James combination the first silicide film 40 (highlighted red) forms on the polysilicon wiring 5b [sic:3c] (highlighted green), and the second silicide film 12 (also highlighted red) forms on the top surfaces of the raised SiGe source/drain regions (highlighted yellow). *See* Section X.C.1.a. above.

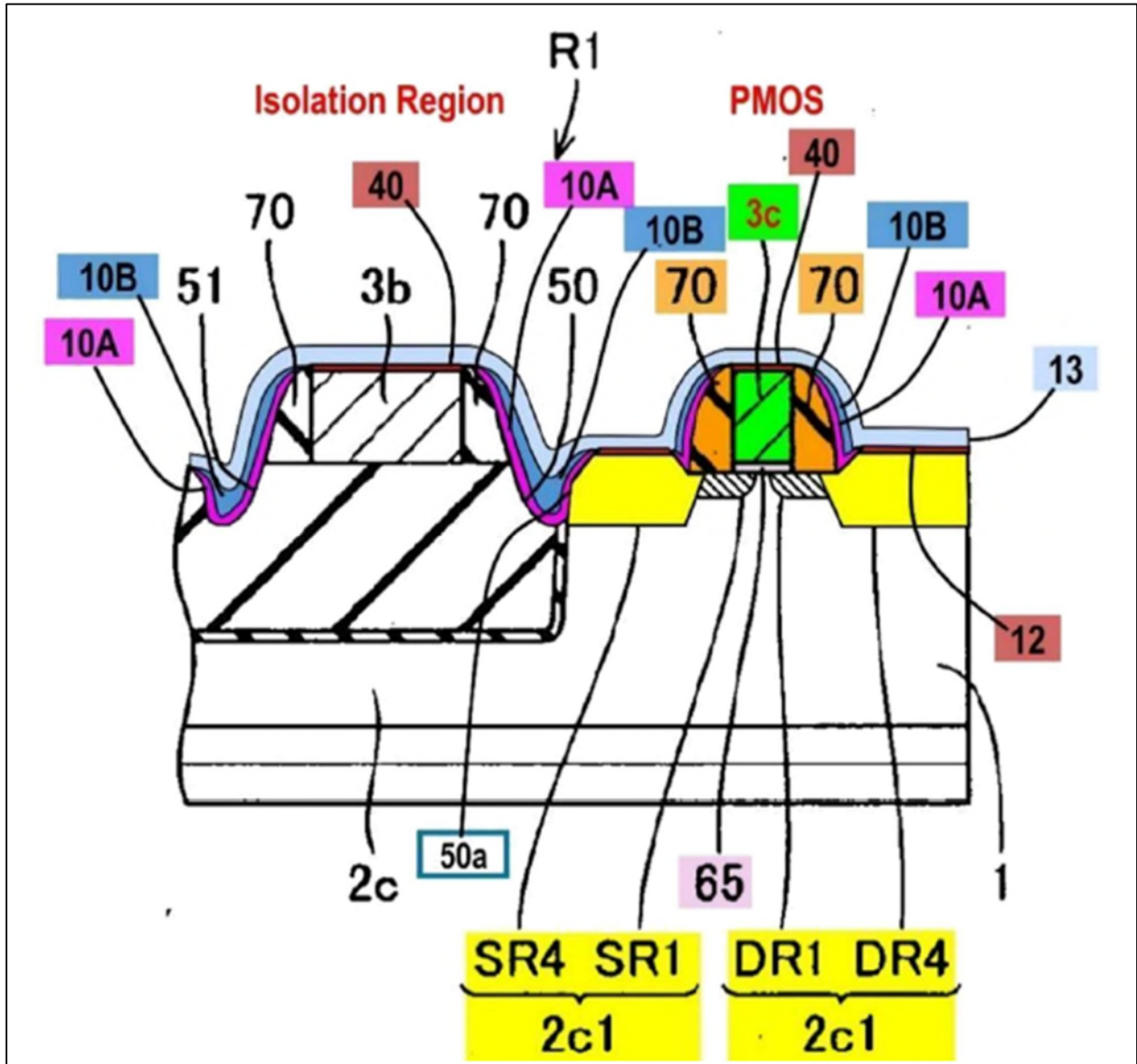


Figure M

394. In the combination, after the silicide formation on the SiGe regions, the top surface of the raised SiGe still remains above the top surface of the substrate. See Fukutome, Ex.1011, ¶¶[0103]-[0104], FIGS. 5F-5G. Fukutome teaches that the SiGe layers may grown to about 120 nm thick. On the other hand, Fukutome trenches have a maximum depth of about 20-70 nm. Accordingly, the epitaxial SiGe extends

about 50-100 nm above the substrate. *See* Fukutome, Ex.1011, ¶¶[0093], [0099]. Saito825's disclosure of the silicide layers contemplates the thickness being a standard 10nm thick. Saito825, Ex.1010, ¶[0116]. Accordingly, a POSITA would have read these dimensions and understood that they are consistent with FIGS. 5F and 5G of Fukutome, where, as can be seen, the top surface of the SiGe layers are at a height above the top surface of the substrate after silicidation. This is mirrored in James' Intel's 90 nm pFET. *See* James, Ex.1012, Fig. 6.

395. A POSITA would have found it obvious to retain the top level of the SiGe source/drains above the substrate surface to mitigate source/drain junction leakage and otherwise enhance reliability, as previously discussed. *See* Fukutome, Ex.1011, ¶[0100]; Sections X.C.1.a. and X.C.2.

4. Dependent Claim 4

- a. Claim 4: “The semiconductor device of claim 1, wherein the first stress-relief film is formed on a side surface of the silicon compound layer.”**

396. In my opinion, the Saito825-Fukutome-James combination renders claim 4 obvious. First, The Saito825-Fukutome-James combination renders the semiconductor device of claim 1 obvious for the same reason explained in Sections X.C.2.a-k. above.

397. As explained for claim element [1H], and in Figure M below, stress-relief film 10A (highlighted magenta) would have formed on the facets (side

5. Dependent Claim 7

a. Preamble: “The semiconductor device of claim 1”

398. The Saito825-Fukutome-James combination renders the semiconductor device of claim 1 obvious for the same reason explained in Sections X.C.2.a-k. above.

b. Element 7[a]: “the first MIS transistor is a p-type MIS transistor”

399. As I explain above for claim 1, Saito825 discloses that the first MIS transistor is a PMOS transistor (e.g., PMOS transistor P2). *See* Section X.C.2.b. above. The Saito825-Fukutome-James combination relies on this PMOS transistor, as modified according to the embodiment shown in Figure M, for example. *See* Section X.C.2.b. above.

c. Element 7[b]: “the first stress is a compressive stress”

400. As I explain above for claim 1, Fukutome’s raised SiGe source/drain regions added to the structure of Saito825 would cause compressive stress to the pFET channel region. *See* Sections X.C.1.a. and X.C.2.f. above. Figure M shows the Saito825-Fukutome-James combination, with the compressive stress being exerted by the raised SiGe source/drain regions. *See* Sections X.C.1.a. and X.C.2.f. above; Fukutome, Ex.1011, ¶[0110]; James, Ex.1012, 2.

d. Element 7[c]: “the second stress is a tensile stress”

401. As I explain above for claim 1, it would have been obvious to a POSITA to modify Saito825’s SiN insulating film 13 to cause a tensile stress, as James teaches. *See* Sections X.C.1.a. and X.C.2.g; James, Ex.1012, 2, 5. Figure M shows the Saito825-Fukutome-James combination, with the tensile stress caused by tensile SiN insulating film 13. *See* Sections Sections X.C.1.a. and X.C.2.g. above; James, Ex.1012, 2, 5.

6. Dependent Claim 8

a. Preamble: “The semiconductor device of claim 1”

402. The Saito825-Fukutome-James combination renders the semiconductor device of claim 1 obvious for the same reason explained in Sections X.C.2.a-k. above.

b. [8A]: “the silicon compound layer is a SiGe layer”

403. As I explain above for claim 1, the Saito825-Fukutome-James combination’s silicon compound layer is the epitaxial SiGe source/drain regions *See* Sections X.C.1.a. and X.C.2.f. above; Fukutome, Ex.1011, ¶¶[0005], [0098], [0110], FIGS. 5D-5G.

c. [8B]: “the stress insulating film is a silicon nitride film”

404. For the same reasons I explained in Section X.C.2.g., Saito825’s silicon nitride insulating film 13 is the stress insulating film of the ’425 patent. *See* Sections

X.C.1.a. and X.C.2.g. above; Saito825, Ex.1010, ¶¶[0080], [0120], FIG. 21. Figure M of the Saito825-Fukutome-James combination, the silicon nitride insulating film 13 is the stress insulating film. *See* Sections X.C.1.a. and X.C.2.g. above; Saito825, Ex.1010, ¶¶[0080], [0120], FIG. 21; James, Ex.1012, 2, 5, Fig. 6.

d. [8C]: “the first stress-relief film is a silicon oxide film”

405. For the same reasons I explained in Sections X.C.2.h.-j, Saito825’s silicon oxide film 10A is the stress-relief film of the ’425 patent. *See* Sections X.C.1.a. and X.C.2.i above. Figure M of the Saito825- Fukutome-James combination, the silicon oxide film 10A is the first stress-relief film. *See* Sections X.C.1.a. and X.C.2.i above; Saito825, Ex.1010, ¶¶[0074]-[0076], FIGS. 18-21.

XI. CONCLUSION

406. For the aforementioned reasons, in my opinion, to a POSITA, the Challenged Claims of the ’425 patent are anticipated and rendered obvious by the prior art.

407. I understand that the Patent Owner has not asserted secondary considerations of non-obviousness. I reserve the right to respond to any such assertions.

Declaration of Dr. Sanjay Banerjee
Inter Partes Review of U.S. Patent No. 8,907,425

408. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the results of the proceedings.

Date: June 6, 2025

Respectfully submitted,



Sanjay Banerjee, Ph.D.