

Filed on behalf of:

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Petitioner

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNITED MICROELECTRONICS CORPORATION,
AND
UMC GROUP (USA),
Petitioners,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,
Patent Owner.

Case No. IPR2025-01090
U.S. Patent 8,907,425

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT No. 8,907,425
UNDER 35 U.S.C. §§ 311, 312 AND 37 C.F.R. § 42.104**

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TABLE OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 8,907,425 B2 to Itou et al. (“the ’425 patent”).
1002	Prosecution History of the ’425 Patent (excerpted) (“File History”).
1003-1004	RESERVED
1005	U.S. Pat. Pub. No. 2009/0246922 A1 to Wu et al. (“Wu922”).
1006	U.S. Pat. Pub. No. 2007/0249069 A1 to Alvarez et al. (“Alvarez”).
1007	RESERVED
1008	U.S. Pat. Pub. No. 2005/0112817 A1 to Cheng et al. (“Cheng817”).
1009	U.S. Pat. Pub. No. 2007/0034906 A1 to Wang et al. (“Wang906”).
1010	U.S. Pat. Pub. No. 2008/0029825 A1 to Saito et al. (“Saito825”).
1011	U.S. Pat. Pub. No. 2005/0285203 A1 to Fukutome et al. (“Fukutome”).
1012	D. James, “2004 – The Year of 90-nm: A Review of 90 nm Devices,” 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (2005) (“James”).
1013-1100	RESERVED
1101	Declaration of Sanjay Banerjee, PhD
1102	Curriculum Vitae of Sanjay Banerjee, PhD

Exhibit No.	Description
1103	“Stress Memorization Technique (SMT) by Selectively Strained-Nitride Capping for Sub-65nm High-Performance Strained-Si Device Application,” Chen et al., 2004 Symposium on VLSI Technology Digest of Technical Papers (2004) (“Chen-2004”)
1104	“35% Drive Current Improvement from Recessed-SiGe Drain Extensions on 37 nm Gate Length PMOS,” Chidambaram et al., 2004 Symposium on VLSI Technology Digest of Technical Papers (2004) (“Chidambaram-2004”)
1105	“Self-Aligned Ultra Thin HfO ₂ CMOS Transistors with High Quality CVD TaN Gate Electrode,” Lee et al., 2002 Symposium On VLSI Technology Digest of Technical Papers (2002) (“Lee-2002”)
1106	“Delaying Forever: Uniaxial Strained Silicon Transistors in a 90nm CMOS Technology,” Mistry et al., 2004 Symposium on VLSI Technology Digest of Technical Papers (2004) (“Mistry-2004”)
1107	“Effects of High-Temperature Forming Gas Anneal on HfO ₂ MOSFET Performance,” Onishi et al., 2002 Symposium On VLSI Technology Digest of Technical Papers (2002) (“Onishi-2002”)
1108	“Low Standby Power CMOS with HfO ₂ Gate Oxide for 100-nm Generation,” 2002 Symposium On VLSI Technology Digest of Technical Papers (2002) (“Pidin-2002”)
1109	“Mobility Enhancement in Strained Si NMOSFETs with HfO ₂ Gate Dielectrics,” Rim et. al., 2002 Symposium On VLSI Technology Digest of Technical Papers (2002) (“Rim-2002”)

Exhibit No.	Description
1110	“Metal Gate MOSFETs with HfO ₂ Gate Dielectric,” Samavedam et al., 2002 Symposium On VLSI Technology Digest of Technical Papers (2002) (“Samavedam-2002”)
1111	“55nm high mobility SiGe(:C) pMOSFETs with HfO ₂ gate dielectric and TiN metal gate for advanced CMOS,” Weber et al., 2004 Symposium on VLSI Technology Digest of Technical Papers (2004) (“Weber-2004”)
1112-1210	RESERVED
1211	Van Zant, “Microchip Fabrication”(Fifth Ed. 2004) (“Van Zant”)
1212	Weste, “CMOS VLSI Design: A Circuits and Systems Perspective” (Third Edition, 2005) (“Weste”)
1213	Houssa, M., “High-k Dielectrics”to Houssa (IOP Publishing Ltd. 2004) (“Houssa”)
1214	Wolf, S., “Silicon Processing for the VLSI Era, Volume 4 – Deep-Submicron Process Technology” (“Wolf-4”)
1215	Plummer, J., et al., “Silicon VLSI Technology: Fundamentals, Practice and Modeling” (Prentice Hall 2000) (“Plummer”)
1216	“International Technology Roadmap for Semiconductors: Process Integration, Devices, and Structures” (2007 Edition) (“ITRS-PIDS”)
1217-1222	RESERVED
1223	“Semiconductor Devices: Physics and Technology” by Sze Second Edition, 2002) (“Sze-2002”)
1224-1225	RESERVED

Exhibit No.	Description
1226	U.S. Patent No. 7,709,331 to Karve, et al. (“Karve”)
1227	U.S. Patent No. 8,017,469 to Luo, et al. (“Luo”)
1228	RESERVED
1229	Wolf, “Silicon Processing for the VLSI Era, Volume 3 – The Submicron MOSFET”(1995) (“Wolf-3”)
1230-1317	RESERVED
1318	Wilk, G. D., et al., “High-k gate dielectrics: Current status and materials properties considerations,” Journal of Applied Physics, Vol. 89, No. 10, pp. 5243-5275, May 15, 2001 (“Wilk”)
1319-1322	RESERVED
1323	U.S. Patent No. 6,306,712 to Rodder, et al. (“Rodder”)
1324-1339	RESERVED
1340	Japanese Patent Publication JP2005-064190 to Ono with certified translation (“JP-Ono”)
1341-1412	RESERVED
1413	S.M. Sze, <i>Physics of Semiconductor Devices</i> (2d ed. 1981) (excerpted) (“Sze-1981”)
1414-1416	RESERVED
1417	T. Ghani et al., “A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors,” Technical Digest of the 2003 IEEE International Electron Devices Meeting (“IEDM”), pp. 978-80 (Dec. 10, 2003) (“Ghani-2003”)

Exhibit No.	Description
1418	RESERVED
1419	U.S. Pat. Pub. No. 2006/0286729 A1 to Kavalieros et al. (“Kavalieros729”)
1420	RESERVED
1421	U.S. Pat. Pub. No. 2011/0042729 A1 to Chen et al. (“Chen729”)
1422-1427	RESERVED
1428	S. Natarajan et al., “A 32nm Logic Technology Featuring 2 nd - Generation High-k + Metal-Gate Transistors, Enhanced Channel Strain and 0.171μm ² SRAM Cell Size in a 291Mb Array,” Technical Digest of the of the 2008 IEEE International Electron Devices Meeting (IEDM), pp. 1-3 (Dec. 2008) (“Natarajan-2008”)
1429	U.S. Pat. Pub. No. 2004/0262784 A1 to Doris et al. (“Doris”)
1430	U.S. Pat. No. 6,797,556 B2 to Murthy et al. (“Murthy556”)
1431	U.S. Pat. Pub. No. 2007/0134870 A1 to Lee et al. (“Lee870”)
1432	U.S. Pat. Pub. No. 2005/0260810 A1 to Cheng et al. (“Cheng810”)
1433	U.S. Pat. Pub. No. 2009/0020820 A1 to Baik et al. (“Baik”)
1434	U.S. Pat. Pub. No. 2008/0293207 A1 to Koutny et al. (“Koutny”)
1435	U.S. Pat. Pub. No. 2010/0075476 A1 to Miyashita. (“Miyashita”)
1436	Declaration of June Ann Munford
1437-1445	RESERVED

Exhibit No.	Description
1446	A. Pavlov & M. Sachdev, “CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies: Process-Aware SRAM Design and Test” (2008) (excerpted) (“Pavlov-2008”)
1447	U.S. Pat. Pub. No. 2007/0023832 A1 to Matsui (“Matsui832”)
1448	M. Ishida et al., “A Novel 6T-SRAM Cell Technology Designed with Rectangular Patterns Scalable Beyond 0.18 μm Generation and Desirable for Ultra High Speed Operation,” Proceedings of the 1998 International Electron Devices Meeting (IEDM), pp. 201-04 (1998) (“Ishida-1998”)
1449	D. Balobas & N. Konofaos, “Design and Evaluation of 6T SRAM Layout Designs at Modern Nanoscale CMOS Processes,” 4th International Conference on Modern Circuits and System Technologies (2015) (“Balobas-2015”)
1450	U.S. Pat. Pub. No. 2011/0074498 A1 to Thompson et al. (“Thompson498”)
1451-1505	RESERVED
1506	U.S. Pat. Pub. No. 2007/0235823 A1 to Hsu et al. (“Hsu823”)
1507-1511	RESERVED
1512	International Technology Roadmap for Semiconductors: Front End Processes (2007 ed.) (“ITRS_FEP”)
1513-1514	RESERVED
1515	U.S. Patent Application Publication No. 2006/0022277 A1 to Kavalieros et al. (“Kavalieros277”)

Exhibit No.	Description
1516	K. Mistry et al., “A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging,” Technical Digest of the of the 2007 IEEE International Electron Devices Meeting (IEDM), pp. 247-50 (Dec. 2007). (“Mistry2007”)
1517	K. Mistry, et al., “A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 93nm Dry Patterning, and 100% Pb-Free Packaging,” presented at 2007 IEEE International Electron Devices Meeting (IEDM), pp. 1-37 (Dec. 2007) (“Mistry_Presentation”)
1518	U.S. Patent No. 6,881,631 B2 to Saito et al. (“Saito631”)
1519	U.S. Patent No. 7,812,414 B2 to Hou et al. (“Hou”)
1520	U.S. Patent Application Publication No. 2005/0258468 A1 to Colombo et al. (“Colombo”)
1521	U.S. Patent No. 6,849,511 B2 to Iriyama et al. (“Iriyama”)
1522	U.S. Patent Application Publication No. 2002/0037615 A1 to Matsuo (“Matsuo”)
1523	S.E. Thompson et al., “A 90-nm Logic Technology Featuring Strained Silicon,” IEEE Transactions on Electron Devices, vol. 51. No. 11, pp. 1790-97 (Nov. 2004). (“Thompson-2004”)
1524	Y. Sun et al., “Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors,” Journal of Applied Physics, vol. 101, Art. No. 104503 (22 pages) (May 2007). (“Sun-2007”)
1525	RESERVED

Exhibit No.	Description
1526	U.S. Pat. Pub. No. 2006/0148151 A1 to Murthy et al. (“Murthy151”)
1527	U.S. Pat. Pub. No. 2004/0262683 A1 to Bohr et al. (“Bohr”)
1528	P. Morin et al., “Extensive Study of the Correlation between ContactEtch Stop Nitride Material Properties and Negative Bias Temperature Instabilities Measured in pMOSFETS,” ECS Transactions, vol. 6, no. 3, pp. 355-69 (2007). (“Morin-2007”)
1529	U.S. Pat. Pub. No. 2005/0170104 A1 to Jung et al. (“Jung”)
1530	RESERVED
1531	U.S. Pat. Pub. No. 2008/0145984 A1 to Ke et al. (“Ke”)
1532	P. Bai et al., “A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell,” Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 657-60 (Dec. 2004) (“Bai-2004”)

Under 35 U.S.C. §§311, 312 and 37 C.F.R. §42.104, United Microelectronics Corporation and UMC Group (USA) (collectively, “Petitioner”) request inter partes review (“IPR”) of claims 1, 3, 4, 7, 8, and 11 (“Challenged Claims”) of U.S. Patent No. 8,907,425 (Ex.1001, “the ’425 patent”).

I. Introduction

The ’425 patent relates stress-inducing and stress-relief structures for metal-insulator-semiconductor field-effect transistors (“MISFETs”).¹ These basic concepts were known before the ’425 patent. Petitioner, supported by the declaration of Dr. Sanjay Banerjee (Ex.1101, Ex.1102) demonstrates the Challenged Claims are unpatentable.

II. Grounds for Standing

Petitioner certifies under 37 C.F.R. §42.104(a) that the ’425 patent is available for IPR and Petitioner is not barred or estopped from requesting IPR of the Challenged Claims on the grounds identified in this Petition.

III. Identification of Challenge

A. Prior Art

The ’425 patent was filed on June 20, 2012 and claim priority to JP2010/002225 (“JP application”), filed on January 7, 2010. Petitioner does not

¹ MISFETs and metal-oxide-semiconductor field-effect transistors are synonymous. (Ex.1101 ¶36.)

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acquiesce the '425 patent is entitled to priority of the JP application. Regardless, each applied reference identified below was filed or published before June 20, 2012 and is prior art to the '425 patent.

1. U.S. Patent Publication No. 2009/0246922 A1 to Wu et al. (“Wu922”, Ex.1005), published October 1, 2009, is prior art under 35 U.S.C. §102(b).²
2. U.S. Patent Publication No. 2007/0249069 A1 to Alvarez et al. (“Alvarez”, Ex.1006), published October 25, 2007, is prior art under 35 U.S.C. §102(b).
3. U.S. Patent Publication No. 2005/0112817 A1 to Cheng et al. (“Cheng817”, Ex.1008), published May 26, 2005, is prior art under 35 U.S.C. §102(b).
4. U.S. Patent Publication No. 2007/0034906 A1 to Wang et al. (“Wang906”, Ex.1009), published February 15, 2007, is prior art under 35 U.S.C. §102(b).
5. U.S. Patent Publication No. 2008/0029825 A1 to Saito et al. (“Saito825”, Ex.1010), published February 7, 2008, is prior art under 35 U.S.C. §102(b).

² Pre-AIA 35 U.S.C. §102 applies.

6. U.S. Patent Publication No. 2005/0285203 A1 to Fukutome et al. (“Fukutome”, Ex.1011), published December 29, 2005, is prior art under 35 U.S.C. §102(b).
7. D. James, “2004 – The Year of 90-nm: A Review of 90 nm Devices,” 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (2005) (“James”, Ex.1012), is prior art under 35 U.S.C. §102(b).

B. Grounds for Challenge

Ground	Basis	Challenged Claims	Prior Art Reference(s)
1	§103	1, 3, 4, 7, 8, 11	Wu922 and Alvarez
2	§103	1, 3, 4, 7, 8, 11	Cheng817
2A	§103	1, 3, 4, 7, 8, 11	Cheng817 and Wang906
3	§103	1, 3, 4, 7, 8	Saito825, Fukutome, James

IV. The '425 patent

A. Technical Background

The '425 patent describes stress-relief films for metal-insulator-semiconductor field-effect transistors (“MISFETs”).³ This technology was already well-known.

1. MISFETs

MISFETs have **source/drain** regions for current input/output. (Ex.1101, ¶36; Sze-1981, Ex.1413, 9-10, Figs. 3, 6; Plummer, Ex.1215, 45-51.) Additionally, a **gate** overlies a **channel** region between source and drain. (Ex.1101, ¶¶36-39; Sze-1981, Ex.1413, 9-10, Fig. 3; Plummer, Ex.1215, 40-45.) The **gate** includes a **gate dielectric** that separates a **gate electrode** from the channel region. (Ex.1101, ¶36; Sze-1981, Ex.1413, 9-10, Fig. 3; Plummer, Ex.1215, 40-45.) Applying voltage to the gate electrode controls a conductive channel to connect or disconnect the source and drain. (Ex.1101, ¶36; Sze-1981, Ex.1413, 9-10, 14, Figs. 3, 6.)

³ “MISFET” and “MOSFET” (“Metal-Oxide-Semiconductor Field-Effect Transistor”) are interchangeable. (Ex.1101, ¶36.)

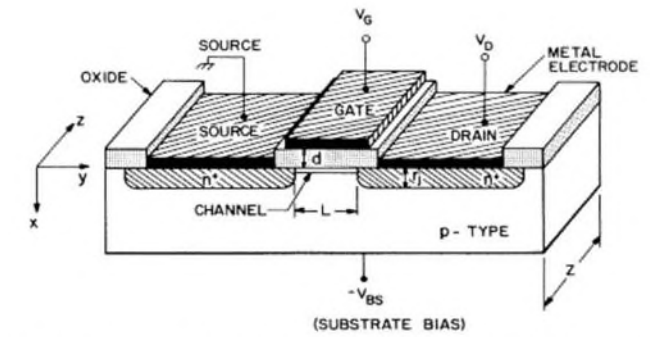
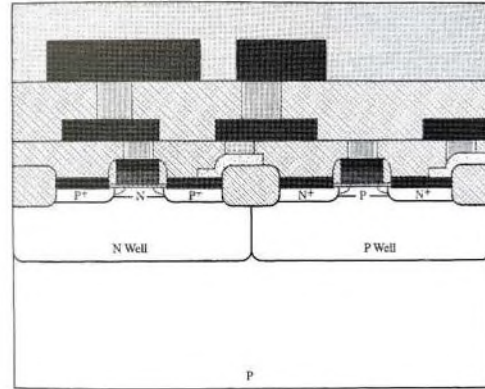


Fig. 3 Schematic diagram of a MOSFET. (After Kahng and Atalla, Ref. 4.)



Sze-1981, Ex.1413, Fig. 3

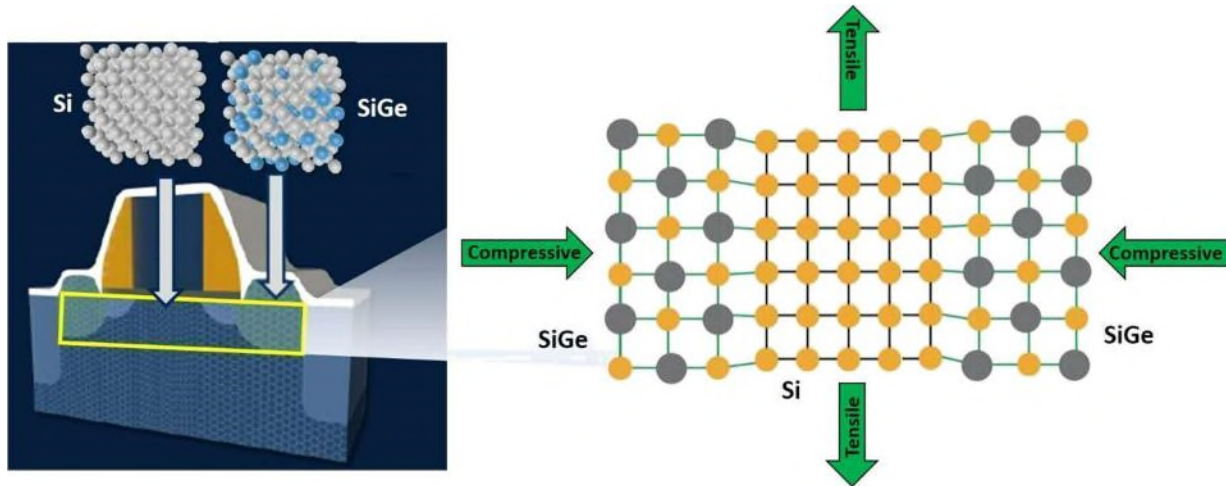
Plummer, Ex.1215, Fig. 1-11

Generally, source/drain regions are doped with p-type or n-type impurities, and channel regions are oppositely doped. (Ex.1101, ¶37; Sze-1981, Ex.1413, 9-10; Plummer, Ex.1215, 45-51.) The terms PMOS and NMOS refer to MISFETs with p-type or n-type source/drain regions, respectively. (Ex.1101, ¶37; Plummer, Ex.1215, 16-17, 19-20, Figs. 1-11, 2-2.) Typical devices are CMOS (“Complementary MOS”), which include both PMOS and NMOS. (Ex.1101, ¶37; Plummer, Ex.1215, 16, Fig. 1-11.)

2. Strained-Silicon Technology

PMOS was once much slower than NMOS. Strained-silicon technology changed that. Because germanium atoms are larger than silicon atoms, growing silicon-germanium (“SiGe”) source/drain regions *compressively* strains the silicon channel region along the current flow direction (left-to-right below). In PMOS, compressive strain improves carrier (hole) mobility and boosts operating speed. (Thompson-2004, Ex.1523, 1-7; Sun-2007, Ex.1524, 2; Ex.1101, ¶¶83.) By 2005,

this technology increased “hole mobility by as much as 50%.” (James, Ex.1012, 2; Ex.1101, ¶¶83-84.)



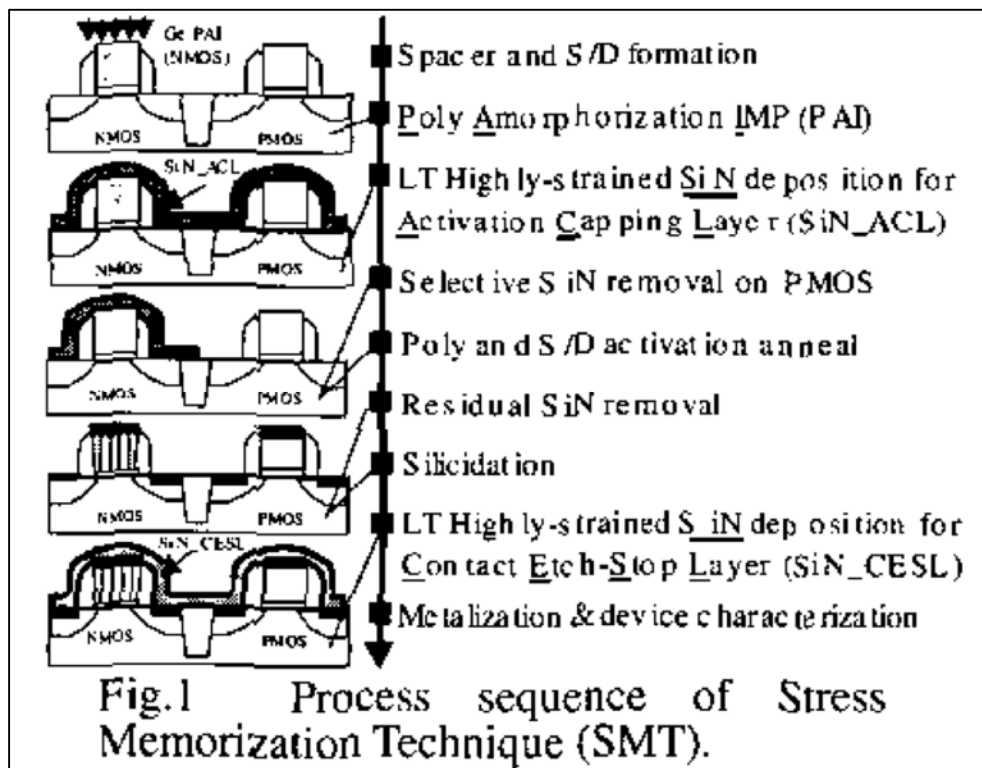
To ensure adequate strain transfer, it was common to grow SiGe source/drain regions extending above the substrate. (The '425 patent, Ex.1001, 1:31-43 (referencing Ghani-2003, Ex.1417); Ghani-2003, Ex.1417, 4, Figs. 1-4; Cheng817, Ex.1008, ¶¶[0065]-[0070], Figs. 4e-4j; Wang906, Ex.1009 ¶¶[0030]-[0032], FIG. 9; Bohr, Ex.1527, FIGS. 4-7; Kavalieros729, Ex.1419, Abstract, ¶[0025], ¶[0043], FIGS. 5, 13; Ex.1101, ¶¶84-89, ¶98) *See also*, Chidambaram-2004, Ex.1104, Introduction, Abstract (“A highly compressive SiGe layer, in close proximity to the channel, results in large hole mobility improvements.”); Mistry-2004, Ex.1106, 50, FIGS. 2-4 (“The use of strain to improve mobility has been known for 50 years,”); Raised SiGe regions further improve PMOS performance by reducing contact resistance. (James, Ex.1012, 2.)

These principles were also commonly applied to NMOS, except improving NMOS carrier (electron) mobility requires *tensile* strain, not compressive. (Ex.1101, ¶86.) Creating tensile strain with source/drain regions requires growing a material like silicon carbide (SiC) with an atom (e.g., carbon) **smaller** than silicon. (Murthy151, Ex.1526, ¶[0005], ¶[0048], ¶[0072]; Wu922, Ex.1005, ¶[0037]; James, Ex.1012, 2; Bohr, Ex.1527, ¶[0045]; Chen729, Ex.1421, ¶¶[0021]-[0022]; Ex.1101, ¶89.)

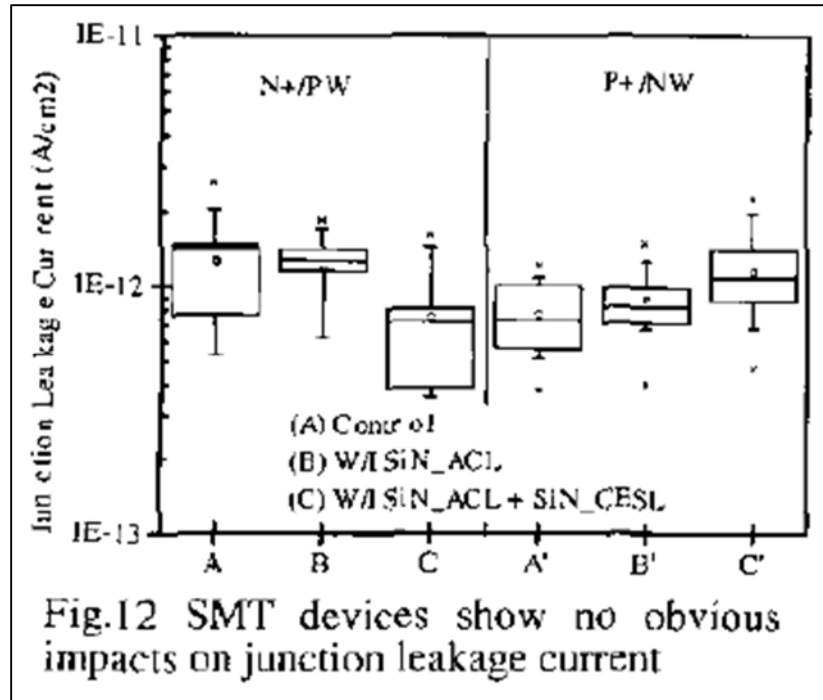
In addition to source/drain epitaxy, it was also common to induce strain by applying stressed films. (Ex.1101, ¶¶87-90; James, Ex.1012, 2, 4; Morin-2007, Ex.1528, 1-2, 13; Alvarez ¶[0022], ¶[0025], ¶[0033]; Hsu823, Ex.1506, ¶[0003]; Jung, Ex.1529, ¶[0090]; Mistry-2004, Ex.1106, FIGS. 2-4; Chen-2004, Ex.1103, Fig. 1). For example, depositing a silicon nitride contact etch-stop layer (“CESL”) can, under certain conditions, “apply[] stress to [a] channel region” to improve mobility. (Hsu823, Ex.1506, ¶[0003]; *see* Ke, Ex.1531, ¶[0003]; Morin-2007, Ex.1528, 1-2; Ex.1101, ¶¶87-90.) Depending how such a layer is prepared, it may provide tensile stress, compressive stress, or no stress. (Jung, Ex.1529, ¶[0017], ¶¶[0099]-[0100], ¶¶[0131]-[0132], Tbls. IV-V, VII, Fig. 15; Ex.1101, ¶90.)

Further, Chen-2004 demonstrates that it was well known to use tensile CESL over both the PMOS and NMOS transistors. As can be seen in Chen-2004 Fig. 1, below, the “SiN_CESL” or the “LT Highly strained SiN deposition for Contact Etch Stop Layer” is formed over both the PMOS and NMOS structures. Chen-2004,

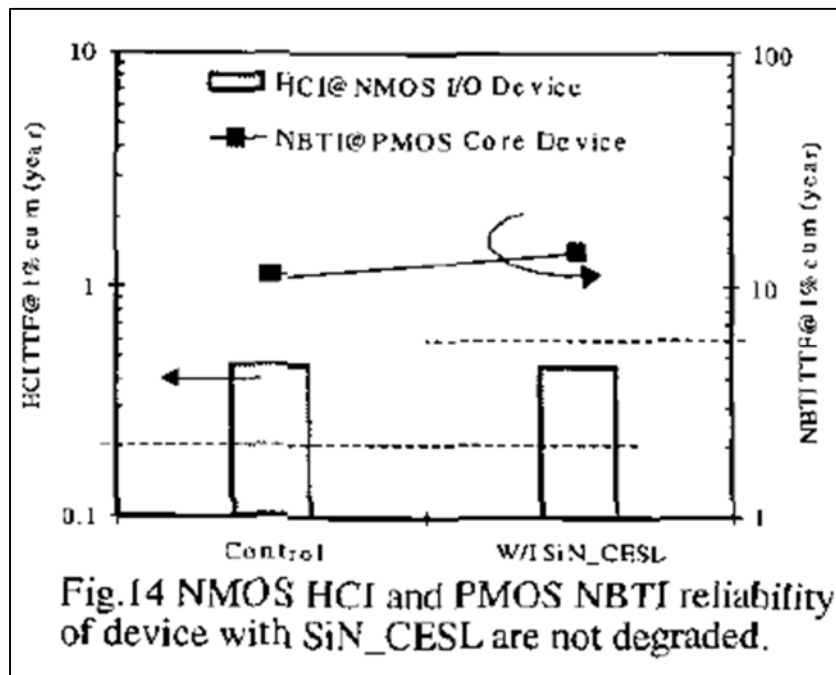
Ex.1103, Fig. 1. The CESL not only improved performance of the NMOS transistor by enhancing the tensile strain on the transistor, but it also had no significant impact on performance of the PMOS transistor, as can be seen in Figures 12 and 14. *See* Chen-2004, Ex.1103, Device Integrity and Reliability, Fig. 12 (“In addition, the SMT process induced strains do not adversely affect the gate leakage current and junction leakage, as illustrated in Fig.11 and Fig.12, respectively.”); Chen-2004, Ex.1103, Device Integrity and Reliability, Fig. 14. (“Figure 14 demonstrates that the device with SIN-CESL has no negative impacts on the hot carrier lifetime and the negative bias temperature instability even in severe criteria of 1% cumulated failure.”).



Chen-2004, Ex.1103, Fig. 1.



Chen-2004, Ex.1103, Fig. 12.

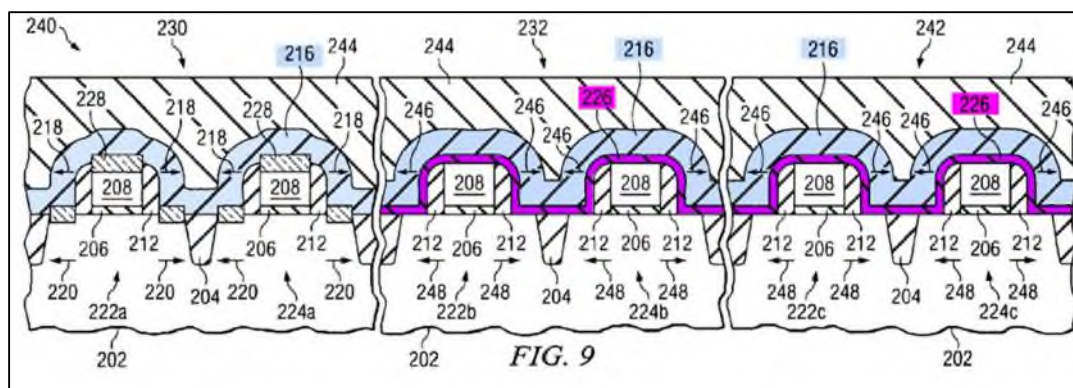


Chen-2004, Ex.1103, Fig. 14.

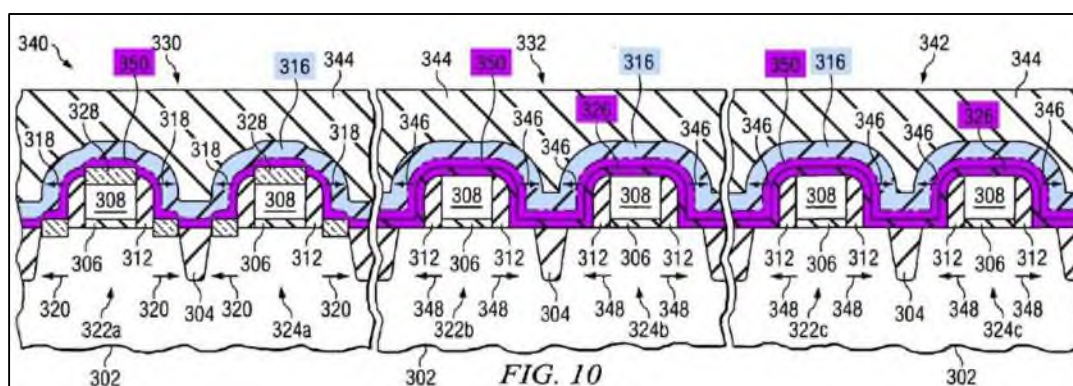
The '425 patent admits strained-silicon technology was known. (The '425 patent, Ex.1001, 1:23-2:62, FIGS. 8A-10C.) At least four generations of high-volume commercial devices already used it by 2009. (Thompson-2004, Ex.1523, 1-7 (90nm devices); Bai-2004, Ex.1532, 4-5 (65nm devices); Mistry2007, Ex.1516, 1-4 (45nm devices); Natarajan-2008, Ex.1428, 1 (32nm devices); Ex.1101, ¶85; Mistry_Presentation, Ex.1517, 1-19.)

3. Stress-Relief Layers

A tensile CESL near a PMOS channel generally applies tensile stress to the channel. (Morin-2007, Ex.1528, 1-2, 13; Doris, Ex.1429, ¶¶0005, ¶¶0013; Hsu823, Ex.1506, ¶¶0037; Ex.1101¶93.) This can oppose compressive stress from SiGe layers, lessening PMOS performance improvements. (Morin-2007, Ex.1528, 1-2, 13; Kavalieros729, Ex.1419, ¶¶0002, ¶¶0026; Doris, Ex.1429 ¶¶0005; Ex.1101, ¶93.) To reduce such unwanted stress, it was widely known to place a stress-relief film underneath the CESL. (Murthy556, Ex.1430, 9:27-29, FIGS. 2, 9, 13-15; Doris, Ex.1429 ¶¶0042, Figs. 1-2, 14-15; Lee870, Ex.1431 ¶¶0029, ¶¶0046-[0067], FIGS. 2-5; Cheng810, Ex.1432, ¶¶0022-[0031], Figs. 1B-1F; Baik, Ex.1433, ¶¶0037, Fig. 2; Koutny, Ex.1434 ¶¶0108; Alvarez, Ex.1006, Abstract, ¶¶0043, ¶¶0049, ¶¶0066, ¶¶0068, ¶¶0077, FIGS. 9-11; Ex.1101, ¶¶95-98.)



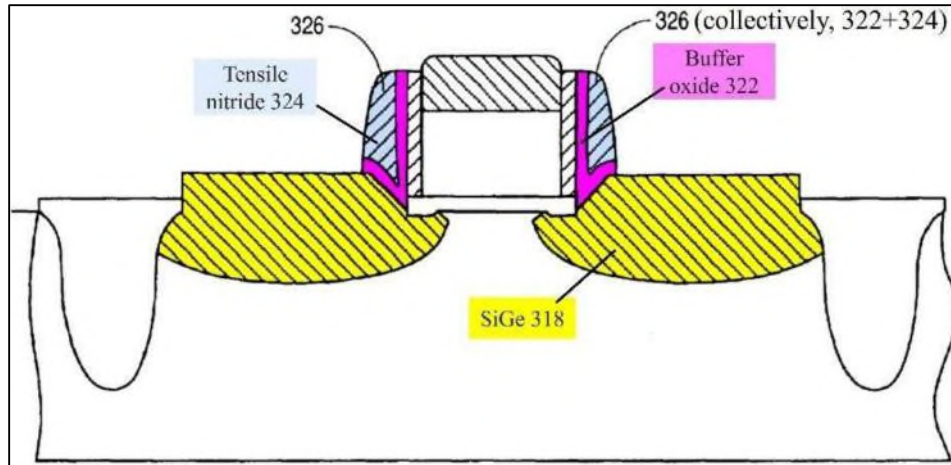
Alvarez, Ex.1006, FIG. 9 (stress buffer layer 226)⁴



Alvarez, Ex.1006, FIG. 10 (stress buffer layers 326 and 350)

With raised SiGe source/drain regions, the stress-relief layer fills the space between the SiGe and gate, as shown below. (Murthy556, Ex.1430, 9:11-15, 9:30-35, FIGS. 7-9; *see* Miyashita, Ex.1435, ¶¶[0052]-[0053], FIGS. 1U-1W; Ex.1101, ¶98.)

⁴ All colored annotations herein have been added.



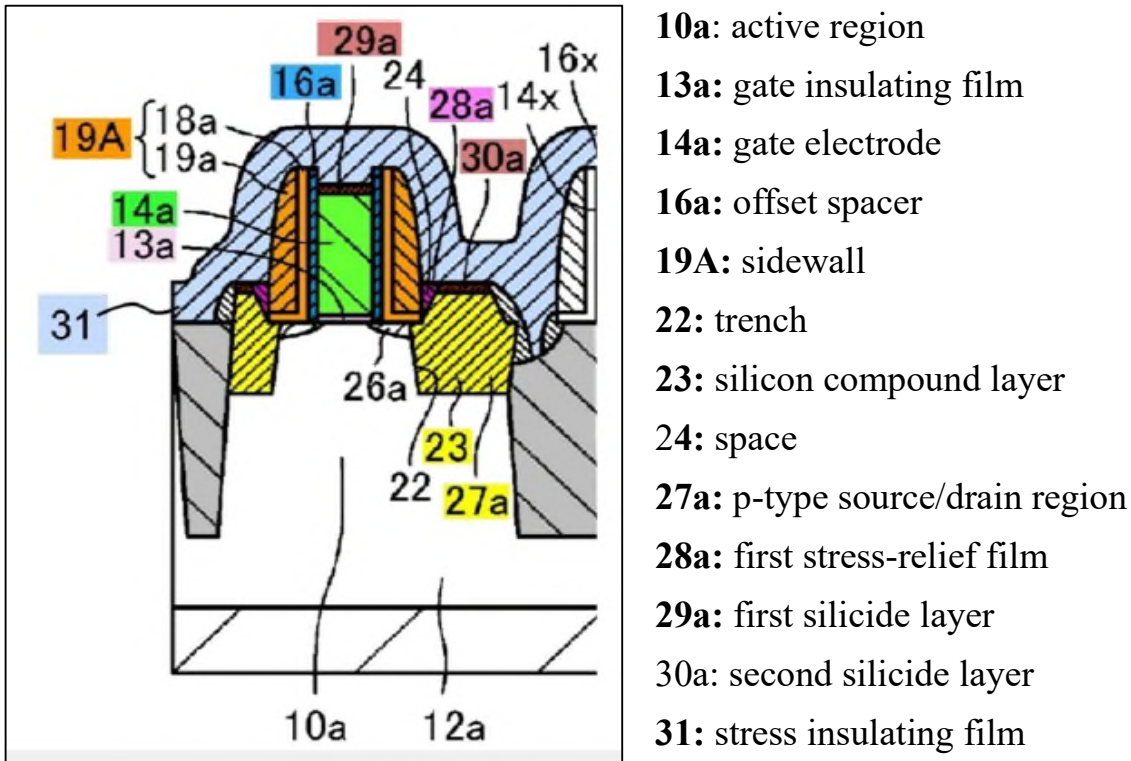
Murthy556, Ex.1430, FIG. 9, annotated

The intermediate stress-relief layer “buffers the large stress” from the CESL. (Murthy556, Ex.1430, 9:27-29; Ex.1101, ¶96.) That is, it applies a “neutral stress or opposite stress relative to the [CESL],” which “reduces the tensile stress in the channel region.” (Lee870, Ex.1431 ¶[0049], ¶[0064]; *see* Alvarez, Ex.1006, ¶[0049]; Doris, Ex.1429 ¶[0042]; Cheng810, Ex.1432, ¶[0030]; Ex.1101, ¶95.)

B. '425 patent Overview

The '425 patent acknowledges techniques for “applying a stress to [a MISFET] channel region ... to improve the performance” were known. (The '425 patent, Ex.1001, 1:23-27.) It further admits “*compressive* stress” (PMOS) or “*tensile* stress” (NMOS), when “applied to the channel region,” increases carrier mobility and device performance. (*Id.*, 1:27-43, 3:1-4.) Conversely, it admits “drive capability ... is reduced” by the opposite stress. (*Id.*, 3:1-4.) The '425 patent discloses a stress-

relief film to mitigate performance reduction in PMOS devices that include a tensile CESL. (*Id.*, 3:13-17.)



The '425 patent, Ex.1001, FIG. 6B (excerpted)

FIG. 6B above illustrates an exemplary PMOS device with known features, including a “first stress-relief film 28a ... formed in [a] space 24 located between the silicon compound layer 23 [*e.g.*, SiGe] and the first sidewall 19A.” (*Id.*, 13:6-8; *see id.*, 14:15-42, FIG. 6B.) According to the '425 patent, this makes it “possible to reduce the tensile stress applied from the stress insulating film 31 to the channel region” and “prevent a reduction in drive capability.” (*Id.*, 16:6-11.)

C. Claim Construction

Petitioner does not believe any claims require construction to resolve the patentability disputes in this proceeding. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

D. Level Of Ordinary Skill In The Art

A POSITA would have had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. Ex.1101, Section VII. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education. *Id.*

V. Prior Art

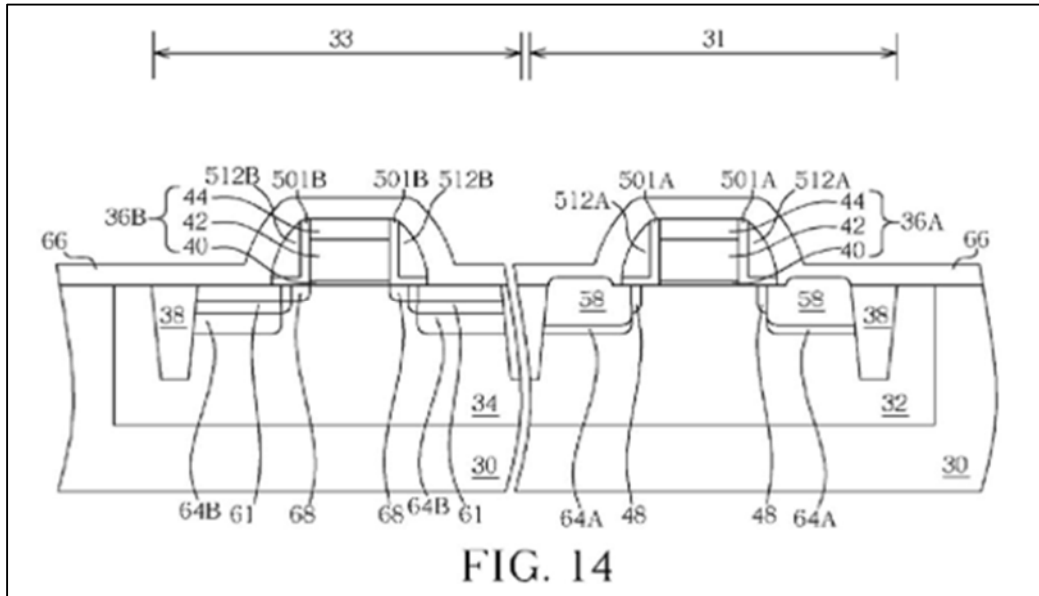
A. Wu922 et al. (Ex.1005)

Wu922 is prior art under pre-AIA §102(a), (e). Since Wu922 is in the same field (MISFETs) and reasonably pertinent to a problem the '425 patent addresses (strain engineering and device manufacturing), Wu922 is analogous. (The '425 patent, Ex.1001, 1:15-7:54; Wu922, Ex.1005 ¶¶[0001]-[0011]; Ex.1101, Section IX. A.)

Wu922 discloses “strained CMOS” structures with PMOS and NMOS regions 31 and 33. (Wu922, Ex.1005 ¶¶[0009], ¶[0017], ¶[0038], FIG. 14.) In PMOS regions 31, SiGe layer 58 projects above the top of substrate 30 and compresses the channel. (Wu922, Ex.1005 ¶¶[0021], ¶[0041], FIG. 14.) A strained “contact etch stop layer

(CESL) 66” covers the devices. (Wu922, Ex.1005 ¶[0025], ¶[0044], FIG. 14.)

Optionally, silicide may be formed before CESL 66. (Wu922, Ex.1005 ¶[0024], ¶[0043].)



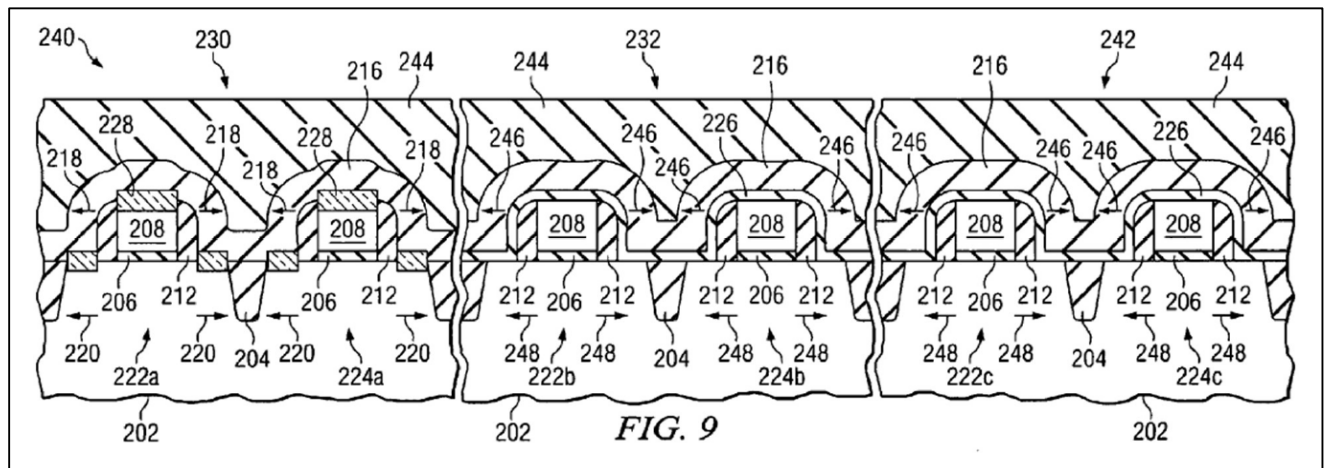
Wu922, Ex.1005, FIG. 14

B. Alvarez et al. (Ex.1006)

Alvarez is prior art under pre-AIA §102(a), (b), (e). Since Alvarez is in the same field (MISFETs) and reasonably pertinent to a problem the '425 Patent addresses (strain engineering and device manufacturing), Alvarez is analogous. (The '425 patent, Ex.1001, 1:15-7:54; Alvarez, Ex.1006 ¶[0001]-[0009]; Ex.1101, Section IX.B.)

Alvarez discloses a “semiconductor device” with “a plurality of active areas,” including silicide region 230, non-silicide region 232, and stress-control region 242,

each with a PMOS transistor 224x and NMOS transistor 222x. (Alvarez, Ex.1006, Abstract, ¶¶[0037]-[0038], FIGS. 9-11.) In regions 232 and 242, Alvarez discloses a “stress-controlling material 226” to mitigate stress caused by “stress-increasing material 216” and prevent silicidation. (Alvarez, Ex.1006 ¶[0035], ¶[0037], ¶[0045], ¶[0049], ¶[0054], ¶[0078], FIGS. 9-11.)



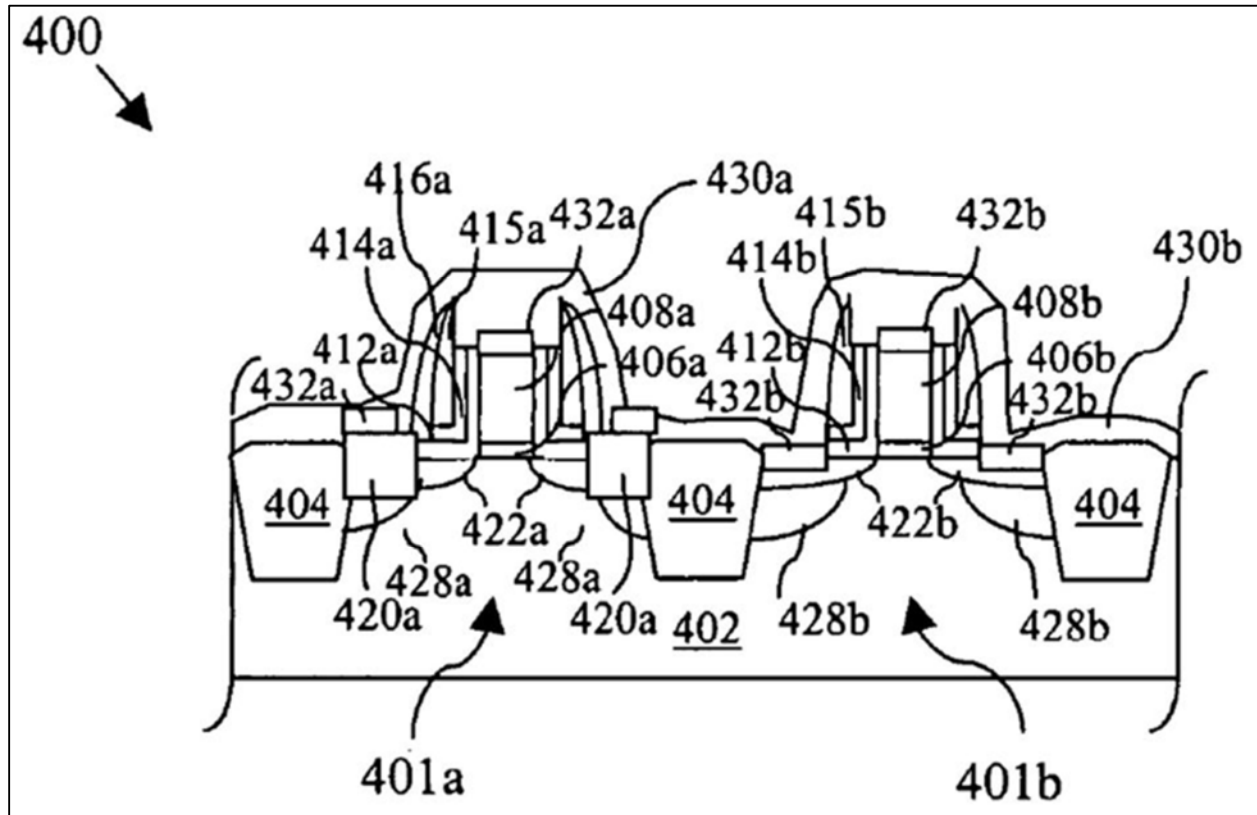
Alvarez, Ex.1006, FIG. 9

C. Cheng817 et al. (Ex.1008)

Cheng817 is prior art under pre-AIA §102(a), (b), (e). Since Cheng817 is in the same field as the '425 patent (MISFETs) and reasonably pertinent to a problem the '425 patent addresses (strain engineering and device manufacturing), Cheng817 is analogous. (The '425 patent, Ex.1001, 1:15-7:54; Cheng817, Ex.1008 ¶¶[0002]-[0003]; Ex.1101, Section IX.C.)

Cheng817's PMOS device 401a includes SiGe source/drain regions 420a that “extend above the substrate” and compressively stress the channel. (Cheng817, Ex.1008 ¶[0022], ¶[0065], Fig. 4j.) Etch stop layer 430a/430b may be a “tensile

film” or “compressive film” made of “silicon nitride (Si_xN_y).” (Cheng817, Ex.1008 ¶[0070], Fig. 4j.)



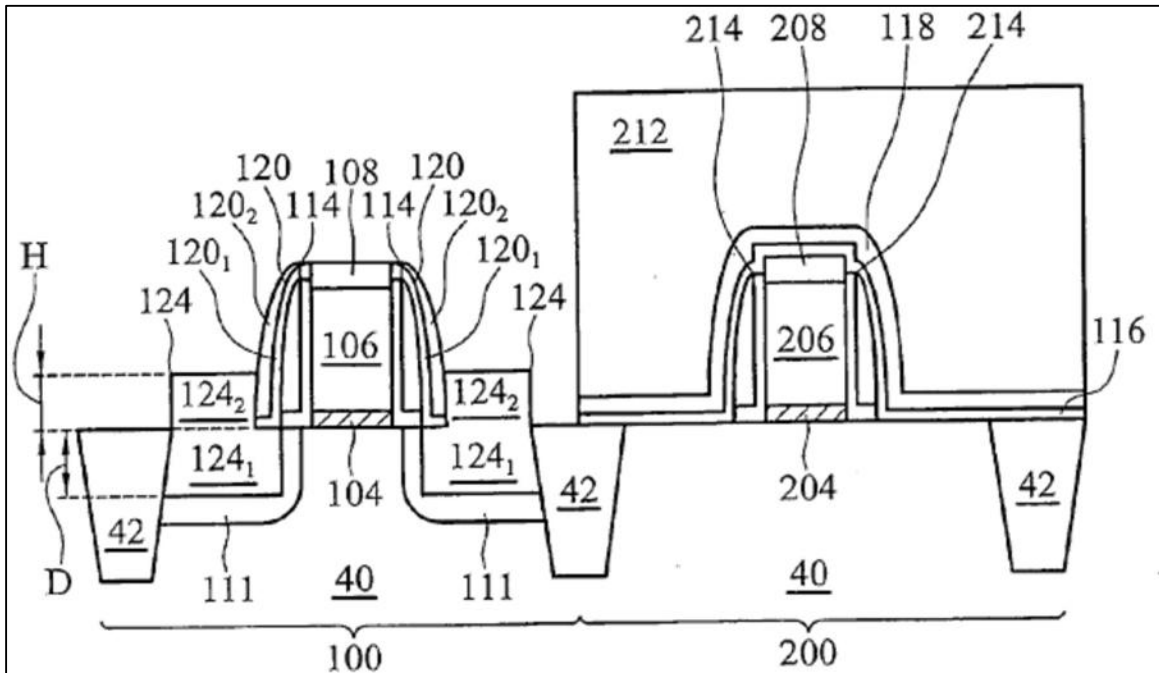
Cheng817, Ex.1008, Fig. 4j

D. Wang906 et al. (Ex.1009)

Wang906 is prior art under pre-AIA §102(a), (b), (e). Since Wang906 is in the same field (MISFETs) and reasonably pertinent to a problem the '425 patent addresses (strain engineering and device manufacturing), Wang906 is analogous. (The '425 patent, Ex.1001, 1:15-7:54; Wang906, Ex.1009 ¶¶[0002]-[0008]; Ex.1101, Section IX.D.)

Wang906 explains: “to strengthen the compressive stress applied by the silicon [SiGe] alloy regions 124 [in pMOS devices], the silicon alloy regions 124

preferably outgrow the top surface of the substrate 40, forming raised portions 1242” about 10-70 nm high. (Wang906, Ex.1009 ¶[0031], FIG. 9).



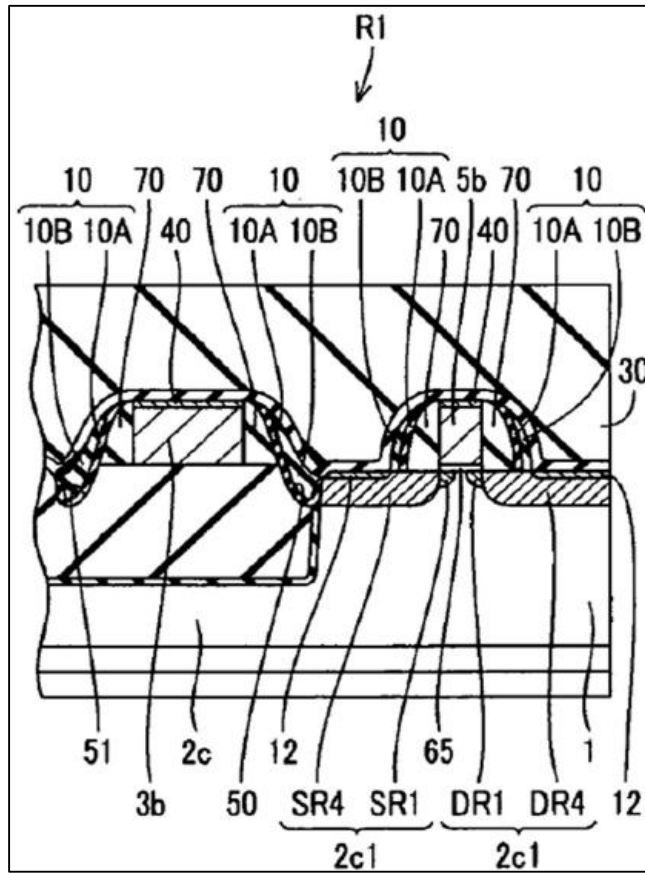
Wang906, Ex.1009, FIG. 9

E. Saito825 et al. (Ex.1010)

Saito825 is prior art under pre-AIA §102(a), (b), (e). Since Saito825 is in the same field (MISFETs) and reasonably pertinent to a problem the '425 patent addresses (recesses in the isolation region next to a gate-level interconnect), Saito825 is analogous. (The '425 patent, Ex.1001, 1:15-7:54, 10:61-11:9, 13:8-15; Saito825, Ex.1010 Abstract, ¶[0074]-[0079]; Ex.1101, Section IX.E.)

Saito825 discloses an SRAM circuit with PMOS and NMOS transistors. (Saito825, Ex.1010 ¶[0056]-[0059], FIG. 1.) To prevent junction leakage, Saito825

teaches to fill recesses 50 in isolation regions 20A1 with oxide layer 10A and nitride layer 10B. (Saito825, Ex.1010 ¶[0027], ¶¶[0074]-[0076], ¶¶[0112]-[0113], FIGS. 3, 12, 21.)

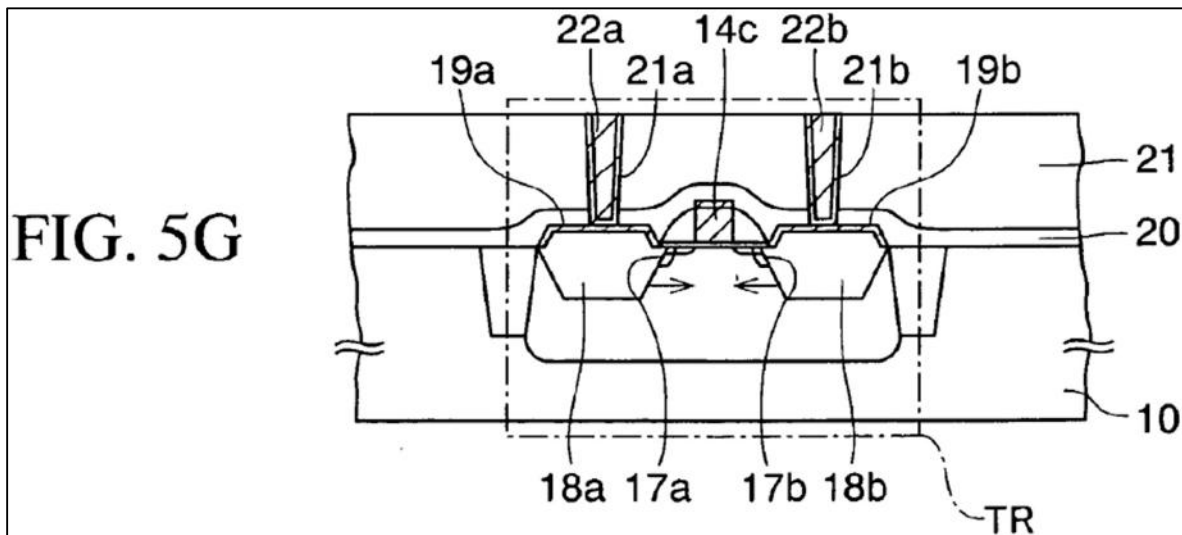


Saito825, Ex.1010, FIG. 21 (excerpted)

F. Fukutome et al. (Ex.1011)

Fukutome is prior art under pre-AIA §102(a), (b), (e). Since Fukutome is in the same field (MISFETs) and reasonably pertinent to a problem the '425 patent addresses (strain engineering and device manufacturing), Fukutome is analogous. (The '425 patent, Ex.1001, 1:15-7:54; Fukutome, Ex.1011 ¶¶[0002]-[0012]; Ex.1101, Section IX.F.)

Fukutome discloses faceted SiGe “source/drain material layers 18a and 18b” grown to “positions higher than the surface of the silicon substrate” to suppress junction leakage and improve reliability. (Fukutome, Ex.1011 ¶[0100]; *see id.*, ¶[0092]-[0096], FIGS. 5D-5G.) Silicon nitride layer 20 covers the substrate. (Fukutome, Ex.1011 ¶[0106], FIG. 5G.)



Fukutome, Ex.1011, FIG. 5G

G. James (Ex.1012)

James is prior art under pre-AIA §102(a), (b). (Ex.1436; Ex.1101, Section IX.G.) Since James is in the same field (MISFETs) and reasonably pertinent to a problem the '425 patent addresses (strain engineering and device manufacturing), James is analogous. (The '425 patent, Ex.1001, 1:15-7:54; *generally* James, Ex.1012; Ex.1101, Section IX.G.)

James describes commercial transistor structures, including in Intel's Prescott chips. (James, Ex.1012, 1-5, Figs. 1-3, 5-12.) In Prescott, “[l]ocalized tensile stress

is applied to the channels of NMOS devices by a highly stressed nitride” that “increases electron mobility.” (James, Ex.1012, 2, Figs. 5-6.) Prescott’s “PMOS transistors (Figure 6) use epitaxial SiGe source/drains to create compressive stress,” which “improves hole mobility.” (*Id.*)

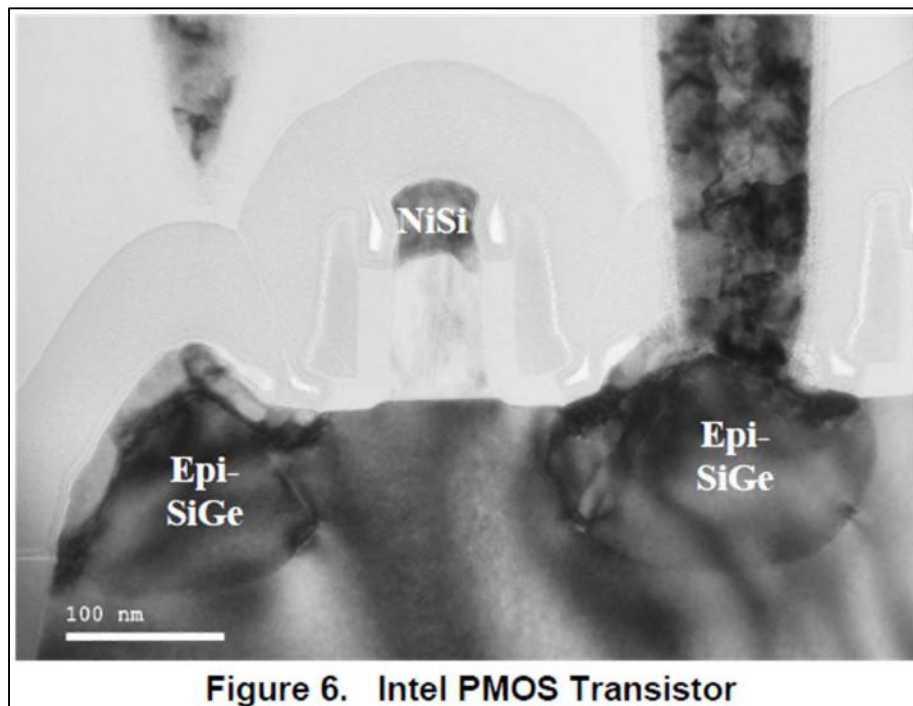


Figure 6. Intel PMOS Transistor

James, Ex.1012, Fig. 6

VI. GROUND 1: Wu922 In View of Alvarez Renders Claims 1, 3, 4, 7, 8 and 11⁵ Obvious.

A. Overview

1. A POSITA Would Have Found the Wu922-Alvarez Combination Obvious

A POSITA would have found it obvious to incorporate Alvarez's stress-relief and stress-inducing layers in Wu922's device. Ex.1101, Section X.A.1.

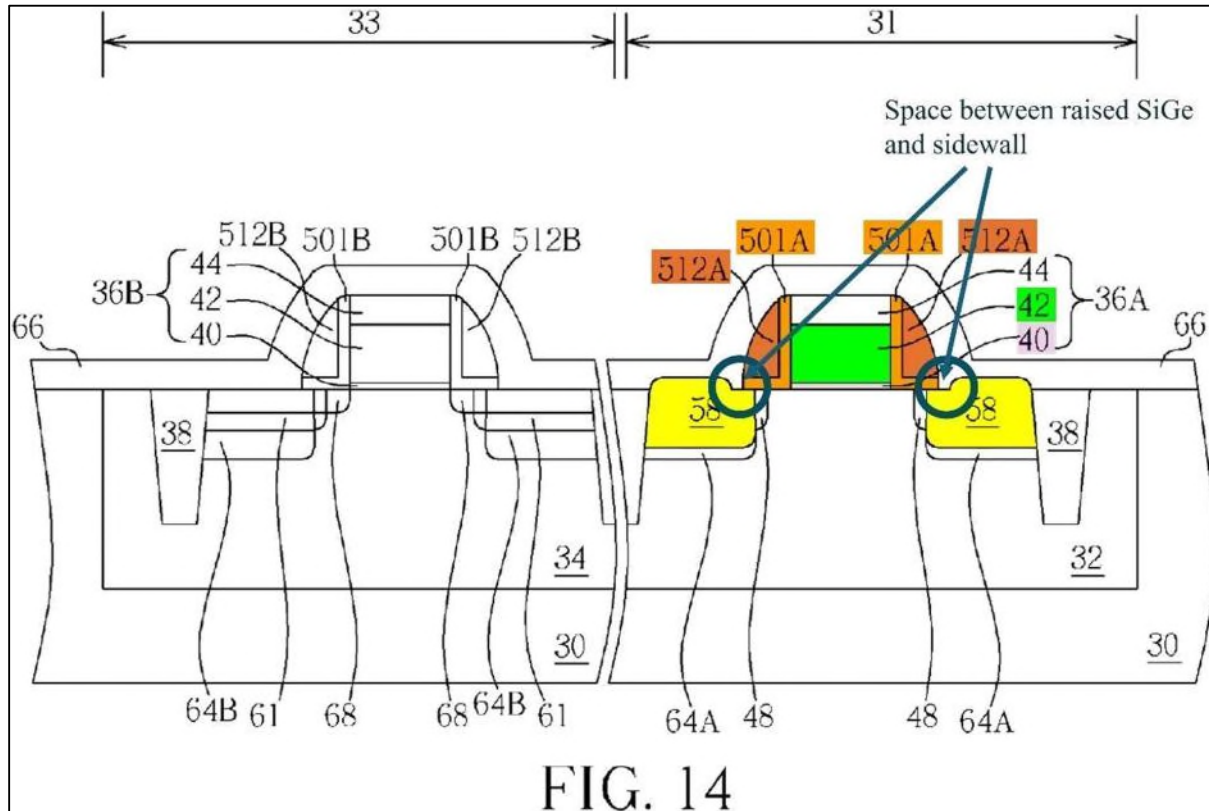
a. A POSITA would have been motivated to combine Wu922 and Alvarez

Wu922 discloses "forming a strained CMOS transistor to improve CMOS transistor performance and reliability." (Wu922, Ex.1005 ¶[0009], FIGS. 1-7, 9-14.) Wu922's PMOS regions 31 include conventional features. (Wu922, Ex.1005 ¶[0017], ¶[0023], ¶¶[0038]-[0039], ¶¶[0042]-[0043], FIGS. 1-7, 9-14.) To form PMOS source/drain regions, Wu922 teaches adding sacrificial layer 52 outside sidewalls 501A and 502A, then etching a recess 56 in which to grow SiGe layers 58 extending above the substrate. (Wu922, Ex.1005 ¶¶[0018]-[0021], ¶¶[0039]-[0041], FIGS. 2-4, 10-12.) SiGe layer 58 "compress[es] the channel" to improve mobility. (*Supra* §IV.A.2; Wu922, Ex.1005 ¶[0021], ¶[0041], FIGS. 4, 12.)

As FIG. 14 shows, Wu922 teaches to remove sacrificial layer 52 and spacer 502A before forming spacer 512A, creating a gap between SiGe layer 58 and

⁵ A listing of Challenged Claims is provided in the Appendix.

sidewalls 501A and 512A. (Wu922, Ex.1005 ¶¶[0022]-[0024], ¶¶[0042]-[0043], FIGS. 5-7, 13-14.)



Wu922, Ex.1005, FIG. 14

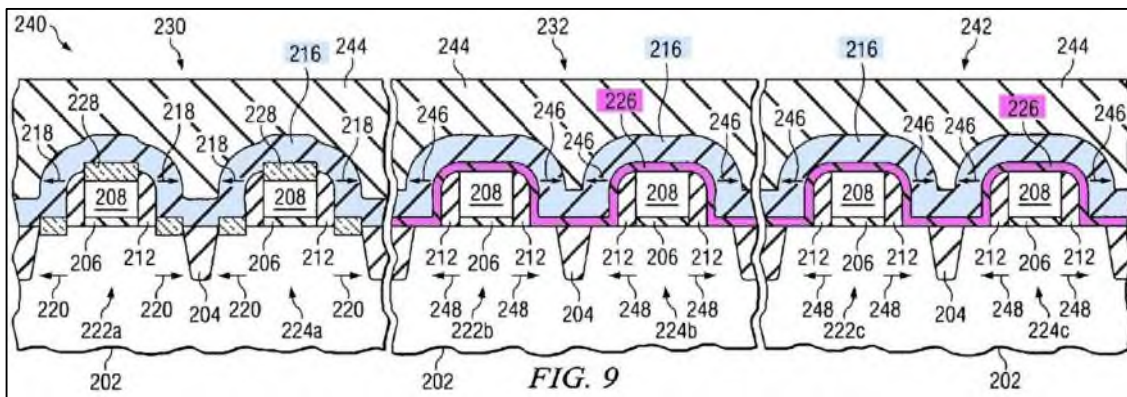
Wu922 then “form[s] a contact etch stop layer (CESL) 66” using a “strained silicon material” (SiN) over the gate structures (36A/36B), spacers (501A/501B and 512A/512B), and sources/drain regions (64A/64B). (Wu922, Ex.1005 ¶¶[0025], ¶¶[0044], FIGS. 7, 14.) CESL 66 can be “a strained thin film upon a surface of the MOS transistor that exert[s] tensile stress or compressive stress” to “improv[e] carrier mobility and MOS transistor performance.” (Wu922, Ex.1005 ¶¶[0005], ¶¶[0025]; *Supra* §IV.A.2; Ex.1101, ¶¶[138-145].) Because Wu922 describes improved

“carrier” mobility (not “electron” or “hole” mobility), CESL 66 can be either tensile or compressive. (Ex.1101, ¶¶144-145.)

As Alvarez shows, a POSITA would have found it obvious to impart tensile strain using CESL 66 to improve electron mobility (NMOS), while also including a stress-control layer to tune that tensile strain and selectively block silicide formation in certain circuit regions (e.g., non-silicide region 232 and stress-control region 242). (Ex.1101, ¶¶134-137, ¶¶146-150.) The asserted combination includes Wu922’s transistors with Alvarez’s stress-control layer underlying a tensile CESL 66.

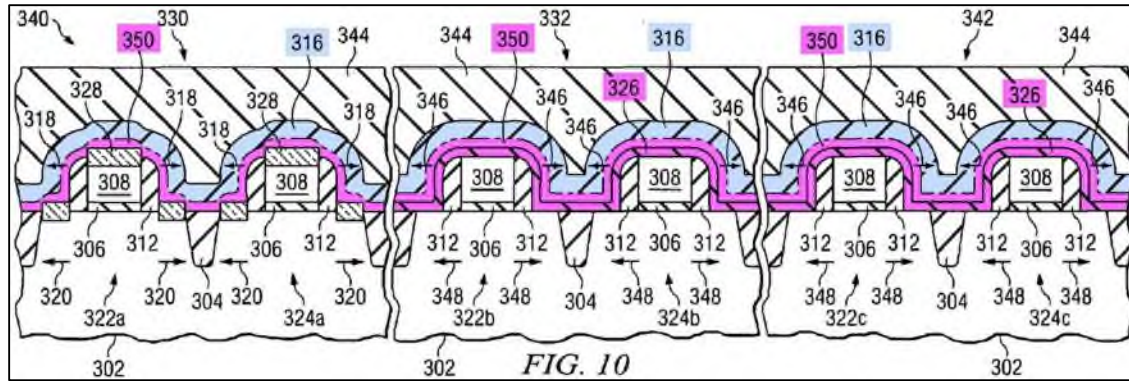
Alvarez explains: “Some NMOS FETs have demonstrated performance enhancement” by imparting “tensile stress to the channel region,” but “some PMOS FETs may suffer from decreased performance” when a tensile CESL is applied. (Alvarez, Ex.1006 ¶[0025]; Ex.1101, ¶151.) To mitigate adverse effects on PMOS, Alvarez discloses stress-controlling layers 226/326/426 and 350/450 underlying tensile CESL 216/316/416. (Alvarez, Ex.1006 ¶[0028], ¶¶[0032]-[0035], ¶¶[0045]-[0046], ¶[0055], ¶¶[0063]-[0068], ¶[0073], ¶[0075], ¶[0078], FIGS. 8-11.) This (a) reduces adverse effects from stress-inducing layer 216/316/416 on PMOS, (b) selectively blocks silicide formation, and (c) eliminates processing steps to streamline manufacturing. (Alvarez, Ex.1006 ¶[0037], ¶[0049], ¶[0061], ¶¶[0070]-[0075], ¶[0078], ¶[0081], FIGS. 9-11; Ex.1101, ¶152.)

Such benefits may be interrelated. For example, Alvarez uses stress-control layer 226/326/426 to selectively block silicide in regions 232/242 of FIGS. 9-10, thus performing two functions. (Alvarez, Ex.1006 ¶[0035], ¶[0045], ¶[0078], FIGS. 9-10.) Leaving stress-controlling layers 226/326/426 and/or 350/450 intact when depositing a tensile CESL 216/316/416, as in FIGS. 9-11, reduces the number of process steps (and manufacturing costs) while accounting for different performance requirements in circuit regions 230, 232, and 242. (Alvarez, Ex.1006 ¶[0027], ¶[0032]-[0033], ¶[0045], ¶[0074], ¶[0078]; Ex.1101, ¶153.)



Alvarez, Ex.1006, FIG. 9⁶

⁶ 222x are NMOS; 224x are PMOS. (Alvarez, Ex.1006, ¶[0025], ¶[0028], ¶[0063].)



Alvarez, Ex.1006, FIG. 10 (3xx corresponds to 2xx in FIG. 9)

To achieve these benefits, a POSITA would have found it obvious to (a) implement Wu922's strained CESL 66 with tensile strain to improve NMOS mobility and (b) include Alvarez's stress-controlling layer in selected regions (e.g., regions 232/242) to (i) mitigate the adverse effects of tensile CESL 66 on PMOS carrier mobility, (ii) prevent unwanted silicide formation in certain regions, and (iii) lower costs. (Alvarez, Ex.1006 ¶¶0037, ¶¶0045, ¶¶0049, ¶¶0061, ¶¶0070-0075], ¶¶0078], ¶¶0081], FIGS. 9-11; Ex.1101, ¶154.)

Alvarez explains: “many different types of transistors 122 and 124 are formed across a workpiece 102 surface, with the different types of transistors 122 and 124 having different operating parameters and requirements.”⁷ (Alvarez, Ex.1006 ¶¶0027[0027].) Alvarez teaches to selectively form silicides only in certain regions “due

⁷ The '425 patent similarly discloses “pMIS region[s]” and “nMIS region[s]” and explains different transistor variations may be used in different circuits, such as “analog,” “peripheral,” or “logic” circuits. (The '425 Patent, Ex.1001, 8:46-61.)

to the performance requirements of transistors in the particular regions.” (Alvarez, Ex.1006 ¶[0032].) For example, transistors in silicide regions require “increased conductivity of the gates 108, source and drain regions,” whereas others “do not ... , and thus the masking material layer 126 is used to prevent silicide 128 formation” in those regions. (*Id.*) Wu922 likewise discloses an **optional** “silicide process (salicide process).” (Wu922, Ex.1005 ¶[0024]; *see id.*, ¶[0043].) As Alvarez demonstrates, a POSITA would have recognized the benefit of siliciding Wu922’s transistors in certain circuits but not others. (Ex.1101, ¶¶152-156.)

A POSITA would have recognized “it is important to work to improve nMOS transistors” via tensile CESL. (Morin-2007, Ex.1528, 2; Ex.1101, ¶157.) Alvarez achieves this by tuning the stress-control layer to reduce, but not eliminate, tensile stress from the CESL. (Alvarez, Ex.1006 ¶[0049], ¶¶[0053]-[0055], ¶[0080], Tbl. 1; Ex.1101, ¶158.) That is, tensile strain can be applied to the NMOS without adversely affecting the PMOS by “tun[ing]” stress-inducing layer 216 and stress-controlling layer 226 “to achieve the amount of control desired on the stress of the underlying material layer, e.g., such as the channel regions of the transistors 222b, 224b, 222c, and 224c,” without incurring additional capital costs. (Alvarez, Ex.1006 ¶¶[0053]-[0055], ¶[0080], Tbl. 1; James, Ex.1012, 2, 5.) By coordinating stress-inducing and stress-controlling layers, a POSITA would have reasonably expected to achieve these

benefits. (Alvarez, Ex.1006 ¶[0037], ¶[0049], ¶[0061], ¶¶[0070]-[0075], ¶[0078], ¶[0081], FIGS. 9-11; Ex.1101, ¶¶157-159, ¶¶166-167.)

Such techniques were well-known. (Ex.1101, ¶¶160-164.) Those in the art knew to place a stress-relief layer underneath a tensile CESL to mitigate adverse effects on PMOS. (*Supra* §§IV.A.2-3; Wu922, Ex.1005 ¶[0005]; Alvarez, Ex.1006 ¶[0043], ¶[0049], ¶[0054], ¶¶[0065]-[0066], ¶[0068], ¶[0074], ¶¶[0077]-[0078], FIG. 9, , Tbl. 1; Murthy556, Ex.1430, 9:10-29; Doris, Ex.1429, ¶¶[0034]-[0035], ¶[0038], ¶[0042], Figs. 2, 14, 15; Baik, Ex.1433, ¶[0037]; Lee870, Ex.1431, ¶[0029], ¶¶[0046]-[0067], FIGS. 2-5; Cheng810, Ex.1432, ¶¶[0022]-[0031], Figs. 1B-1F.) Because Wu922's FIG. 14 shows CESL 66 near the PMOS channel, a POSITA would have been motivated to add a buffer layer like Alvarez's strain-controlling layers 226/326/426 and/or 350/450. (Alvarez, Ex.1006 ¶[0025], ¶¶[0063]-[0068], ¶¶[0070]-[0072], FIGS. 9-11; Ex.1101, ¶¶165-168.) A POSITA would have expected this to improve both NMOS and PMOS performance by "tun[ing]" stress "to achieve the amount of control desired on the stress of the underlying material layer." (Alvarez, Ex.1006 ¶[0053]; *see id.*, ¶[0049], ¶¶[0053]-[0055], ¶[0061], ¶¶[0066]-[0067], ¶¶[0078]-[0081]; Murthy556, Ex.1430, 8:59-9:43, FIGS. 7-9; Doris, Ex.1429, ¶[0034], ¶[0042], Fig. 14; Baik, Ex.1433, ¶[0037]; Lee870, Ex.1431, ¶[0067]; Cheng810, Ex.1432, ¶[0030]; Ex.1101, ¶166, ¶¶166-172.)

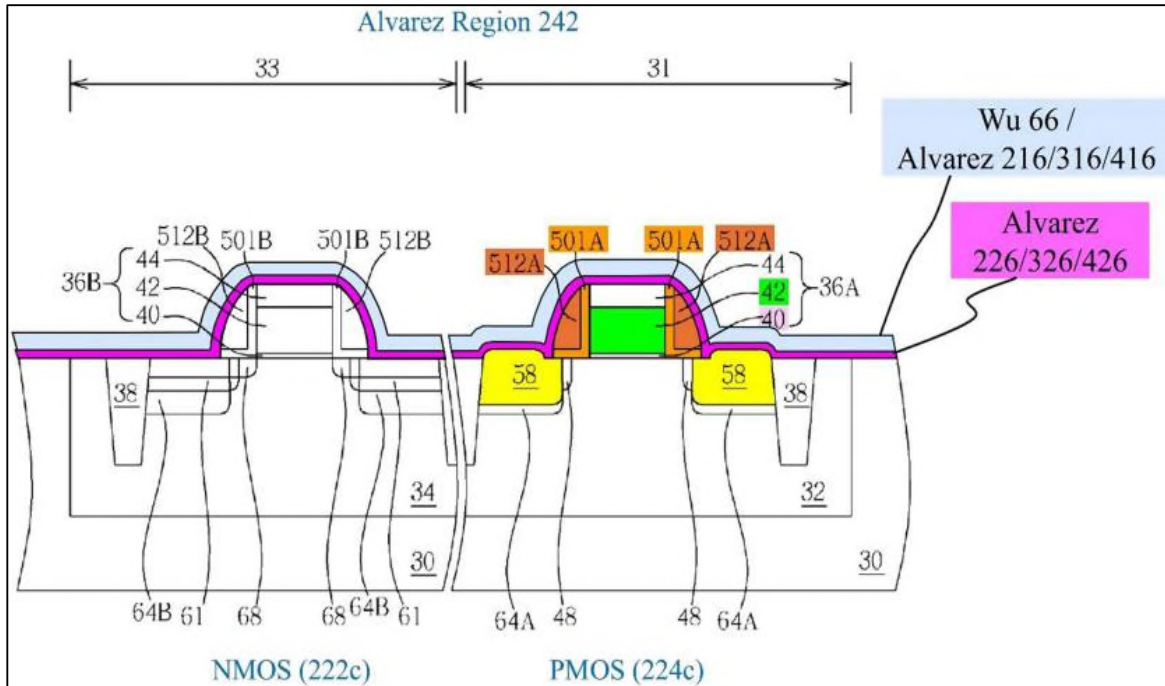


Figure A

A POSITA thus would have been motivated to add a stress-controlling layer to Wu922's MOSFETs, as Figure A shows above.⁸ (Ex.1101, ¶168.) A POSITA would have deposited the stress-controlling layer (magenta) after forming SiGe regions 58 (yellow) and gate sidewalls 512 (dark orange) but before depositing tensile CESL 66 (light blue)—the order Alvarez discloses. (*Id.*) A POSITA would have known this mitigates adverse effects of the tensile CESL on PMOS transistors and prevent silicide formation in selected circuit regions (e.g., regions 232/242),

⁸ To maximize beneficial stresses, Alvarez's stress-control layer may be removed from NMOS devices (e.g., in regions 232/242). (Alvarez, Ex.1006, ¶¶[0065]-[0068], FIG. 11.) This Petition also contemplates such embodiments. (Ex.1101, ¶168.)

while also accounting for different performance requirements (e.g., conductivity requirements) and streamlining manufacturing. (Alvarez, Ex.1006 ¶[0027], ¶¶[0032]-[0033], ¶[0037], ¶[0045], ¶¶[0063]-[0068], ¶¶[0070]-[0075], ¶[0078]; Ex.1101, ¶¶152-154, ¶¶166-167.)

A POSITA would have found the proposed combination obvious, as Figures A (above) and B (below) show, wherein Figure A applies in certain circuit regions (equivalent to Alvarez's regions 232/242) but not in others (equivalent to Alvarez's region 230/330)⁹:

- Transistor 224c in region 242 of Figures A and B maps onto claims 1, 3-4, and 7-8. (*Infra* §VI.B)
- Alternatively, transistor 324a in region 330 maps onto claims 1 and 3. (See Alvarez, Ex.1006 ¶¶[0063]-[0064], FIG. 10; Figure A' discussed *Infra* §VI.B, §VI.C)
- Transistor 222a in region 230 of Figure B (similar to transistor 222c in Figure A but with Wu922's optional silicide and no stress-controlling film) maps onto claim 11. (*Infra* §VI.G.)

(Ex.1101, ¶¶168-170.)

⁹ Alvarez's FIGS. 9 and 10 show the corresponding regions.

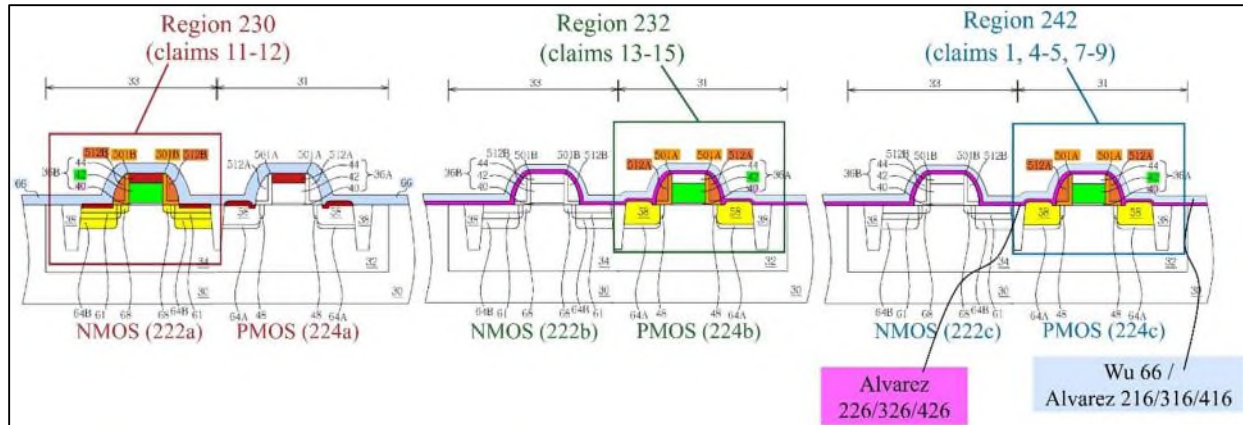
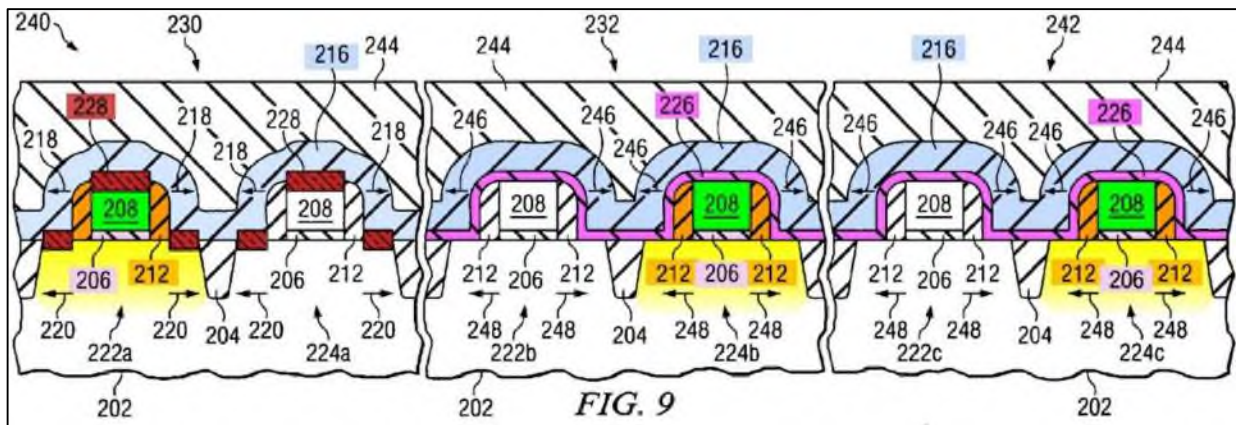


Figure B



Alvarez, Ex.1006, FIG. 9

Although the discussion above generally describes mitigating the adverse effects of tensile CESL on PMOS, Wu922 and Alvarez also disclose and render obvious mitigating adverse effects of compressive CESL on NMOS, e.g., when the NMOS employs epitaxial SiC source/drain layers. (Alvarez, Ex.1006 ¶¶0065], ¶¶0067]; Wu922, Ex.1005 ¶¶0037], ¶¶0057].) A POSITA would have understood the same benefits accrue, except the roles of compressive and tensile strain reverse. (Ex.1101, ¶172.)

b. A POSITA would have reasonably expected to succeed in combining Wu922 and Alvarez

A POSITA would have reasonably expected to succeed in (a) adding a stress-controlling layer to Wu922's devices and (b) implementing Wu922's CESL 66 with tensile strain, as in one proposed combination. (Ex.1101, ¶¶173-180.)

Such a combination requires only conventional steps: (a) forming a stress-controlling layer (as Alvarez teaches) in the desired device regions, e.g., regions 232/242 (Alvarez, Ex.1006 ¶¶[0027], ¶[0032], ¶[0035], ¶[0045], ¶¶[0063]-[0068], ¶[0078], FIGS. 8-11) and (b) forming a stress-inducing CESL 66 to impart tensile strain (as Alvarez teaches) by using appropriate deposition conditions (Jung, Ex.1529, ¶¶[0099]-[0100], Tbl. V; Ex.1101, ¶174.)

Adding a stress-controlling layer where desired would have involved nothing more than well-known deposition and patterning techniques. (Alvarez, Ex.1006 ¶[0044], ¶¶[0052]-[0053], ¶¶[0063]-[0068]; Murthy556, Ex.1430, 9:10-35; Doris, Ex.1429, ¶¶[0036]-[0037], ¶[0042], ¶[0046]; Baik, Ex.1433, ¶[0037]; Lee870, Ex.1431, ¶[0029], ¶¶[0046]-[0067], FIGS. 2-5; Cheng810, Ex.1432, ¶¶[0022]-[0031], Figs. 1B-1F; Ex.1101, ¶¶175-178.) A POSITA would have understood the result to be a stress-controlling layer formed between Wu922's raised SiGe layers and gate sidewalls because, as Alvarez shows, the stress-controlling layer would blanket the exposed PMOS devices. (Wu922, Ex.1005 ¶[0042], FIG. 14; Alvarez, Ex.1006 ¶¶[0043]-[0049], ¶[0052], ¶¶[0063]-[0068], ¶¶[0070]-[0071], ¶¶[0073]-

[0075], ¶[0078], FIGS. 6-11; Murthy556, Ex.1430, 9:10-29, FIG. 8; Miyashita, Ex.1435, ¶¶[0052]-[0053], FIGS. 1U-1W; Ex.1101, ¶175.)

Depositing a tensile (or compressive) nitride CESL was also well-known, conventional, and easily implemented. (*Supra* §IV.A.2; Jung, Ex.1529, ¶¶[0099]-[0100], Tbls. IV-V; Alvarez, Ex.1006 ¶[0047]; Wu922, Ex.1005 ¶[0005]; James, Ex.1012, 2, 5, Fig. 6; Doris, Ex.1429, ¶¶[0016][0017], ¶¶[0029]-[0030], ¶[0038], ¶[0042], ¶[0051], Figs. 1, 2, 14, 15; Morin-2007, Ex.1528, 1-2; Hsu823, Ex.1506, ¶[0003]; Ke, Ex.1531, ¶[0003]; Ex.1101, ¶177.)

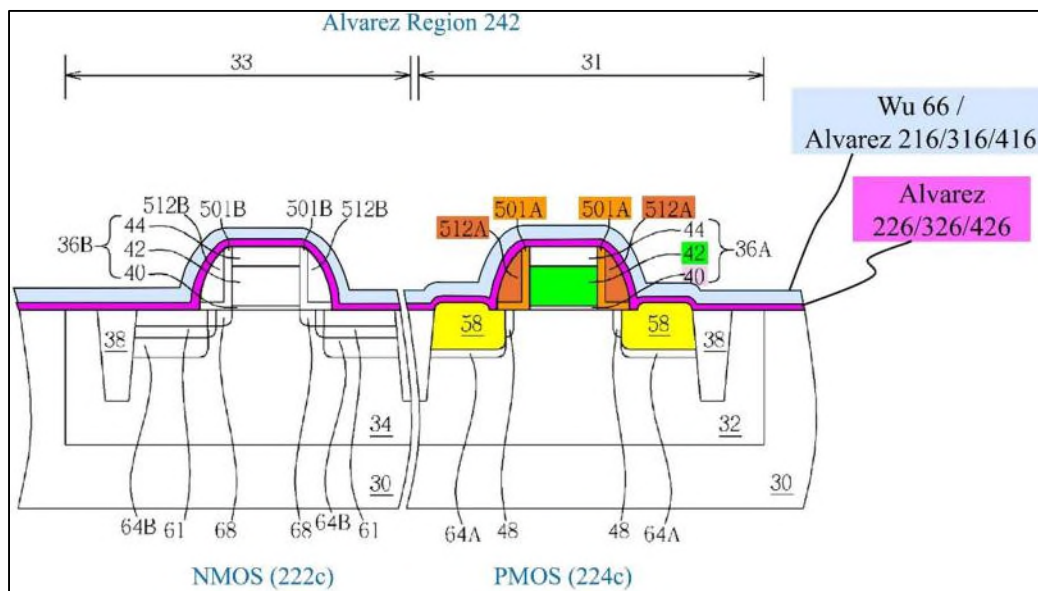


Figure A

Placing a stress-controlling layer underneath a tensile strain layer was also known. (*Supra* §§IV.A.2-3; Ex.1101, ¶178.) Consistent with Alvarez's teachings, a POSITA would have found it obvious to deposit a stress-controlling layer after forming Wu922's sidewall spacer 512A and before depositing a tensile stress-

inducing CESL 66, as Figure A shows. (Alvarez, Ex.1006 ¶¶[0043]-[0049], ¶¶[0063]-[0068], FIGS. 5-11; Wu922, Ex.1005 ¶¶[0043]-[0044], FIGS. 13-14; Ex.1101, ¶¶178-179.) Doing so would have been expected to achieve the ordinary and expected result of buffering CESL strain, among other benefits. (*Supra* §§IV.A.2-3, §VI.A.1.a; Ex.1101, ¶180.)

A POSITA would have found this combination obvious because it (a) combines known prior-art elements (Wu922's MOSFET structures and Wu922's and Alvarez's teachings to use a strained CESL and stress-controlling layer) according to known methods (oxide deposition followed by strained nitride deposition) to yield predictable results (strained CESL and a buffer oxide that mitigates stress and inhibits silicide formation); (b) using known techniques (depositing a stress-controlling layer, as Alvarez instructs, that forms in the space between raised epitaxial regions and gate sidewalls, then depositing strained CESL) to improve similar devices (Wu922's MOSFETs) in the same way (by improving carrier mobility, reducing manufacturing steps, lowering costs, and/or selectively blocking silicide); (c) applying these known techniques to improve Wu922's known device and yield predictable results (improved carrier mobility, streamlined manufacturing, reduced costs, and/or selectively blocked silicide); and (d) applying a known teaching, motivation, or suggestion in the prior art (described above) (*Supra*

§§IV.A.2-3, §VI.A.1) to arrive at the claimed invention. (*KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-21 (2007); Ex.1101, ¶181.)

B. Independent Claim 1

1. Element 1[pre]: “A semiconductor device comprising: a first MIS transistor, ... includ[ing]:”

Wu922 discloses “a strained CMOS transistor.” (Wu922, Ex.1005 ¶[0009]; *see id.*, ¶[0017], ¶¶[0023]-[0024], ¶[0038], ¶¶[0042]-[0043], FIGS. 1-7, 9-14.)

Figure A shows one embodiment of the proposed combination. (*Supra* §VI.A.1; Ex.1101, ¶182.)

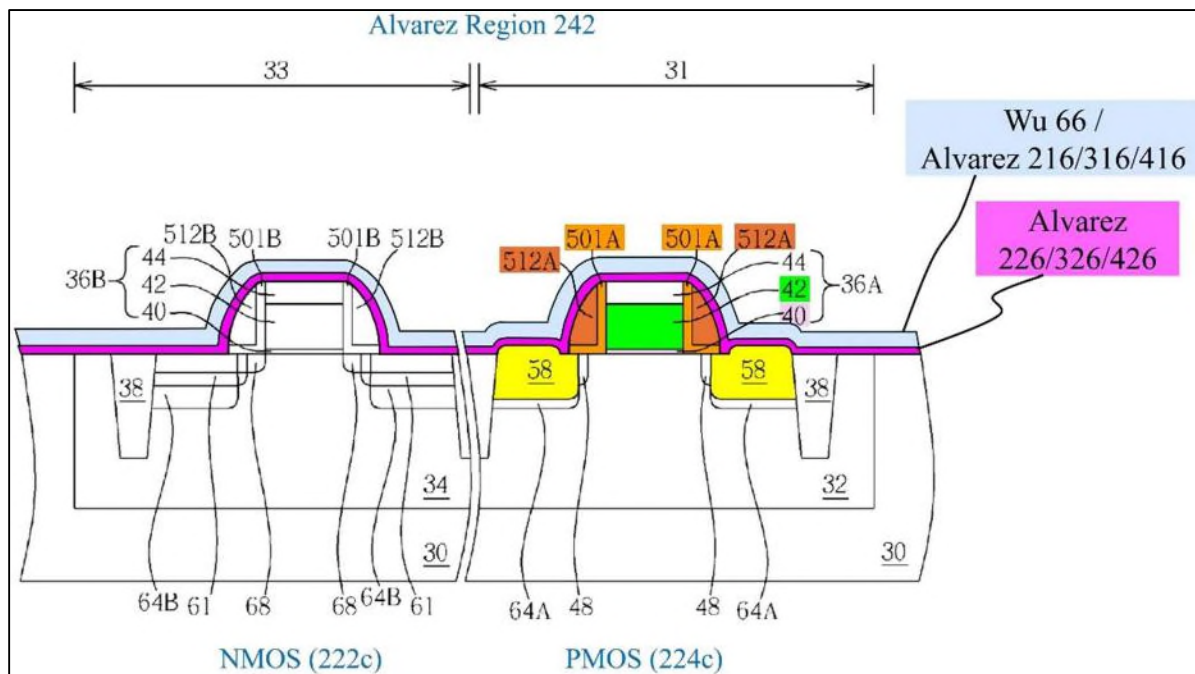


Figure A

Figure A' shows an alternative embodiment with silicided source/drain and gate electrodes. (*Infra* §VI.C (claim 3); Ex.1101, ¶183.)

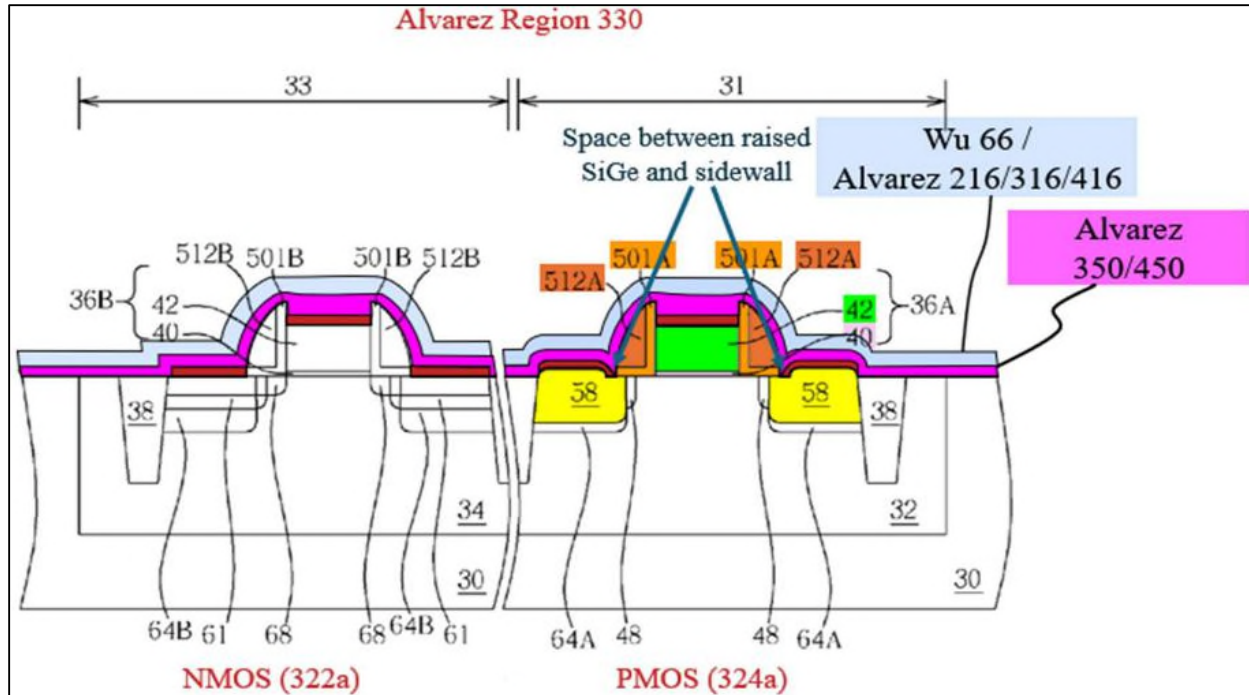


Figure A'

2. Element 1[a]: “a first MIS transistor, ... includ[ing]:”

Wu922 discloses a first MIS transistor, e.g., in PMOS regions 31. (Wu922, Ex.1005 ¶¶[0017], ¶[0023], ¶¶[0027]-[0036], ¶[0038], ¶¶[0042]-[0043], ¶¶[0046]-[0055], FIGS. 1-7, 9-14; Ex.1101, ¶¶184-185.)

3. Element 1[b]: “a first gate insulating film formed on a first active region in a semiconductor substrate”

Wu922 discloses a “gate dielectric insulating layer 40” on a first active region, e.g., PMOS regions 31, in “semiconductor substrate 30.” (Wu922, Ex.1005 ¶[0017], ¶¶[0038]-[0039], FIGS. 7, 14; Ex.1101, ¶186.)

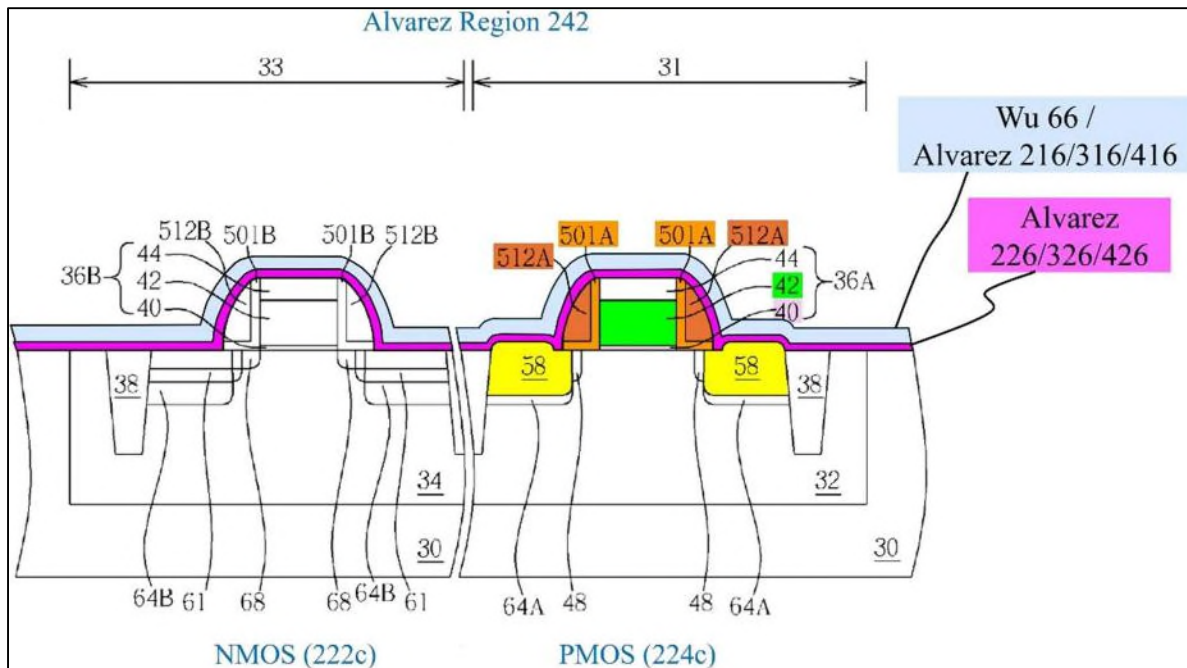


Figure A

4. Element 1[c]: “a first gate electrode formed on the first gate insulating film”

Wu922 discloses a first gate electrode (gate 42) formed on the first gate insulating film (gate dielectric 40) (*see* Figure A). (Wu922, Ex.1005 ¶[0017], FIGS. 7, 14; Ex.1101, ¶¶189-191.)

5. Element 1[d]: “a first sidewall spacer formed on a side surface of the first gate electrode”

Wu922 discloses a first sidewall spacer comprising oxide layer 501A¹⁰ “formed on the sidewalls” of PMOS gate structure 36A, including gate 42 (*see* Figure A). (Wu922, Ex.1005 ¶[0024]; *see id.*, ¶[0017], FIGS. 7, 14; Ex.1101, ¶¶192-194.)

¹⁰ *Infra* note 11.

6. **Element 1[e]: “a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region”**

Wu922 discloses a first source/drain region comprising p-type “epitaxial layer 58 of silicon germanium” in the first active area (PMOS region 31) (*see* Figure A). (Wu922, Ex.1005 ¶[0021]; *see id.*, ¶[0019], ¶[0041], FIGS. 7, 14; Ex.1101, ¶¶195-197.) SiGe (silicon compound) layer 58 grows in a trench (recess 56), located beside gate structure 36A next to first sidewall spacer 501A¹¹ in PMOS region 31, and “compress[es] the channel” (causing first, compressive stress in a gate length direction of a channel region). (Wu922, Ex.1005 ¶¶[0020]-[0021], ¶[0031], ¶¶[0040]-[0041], ¶[0050], FIGS. 3-7, 11-14; Ex.1101, ¶196.)

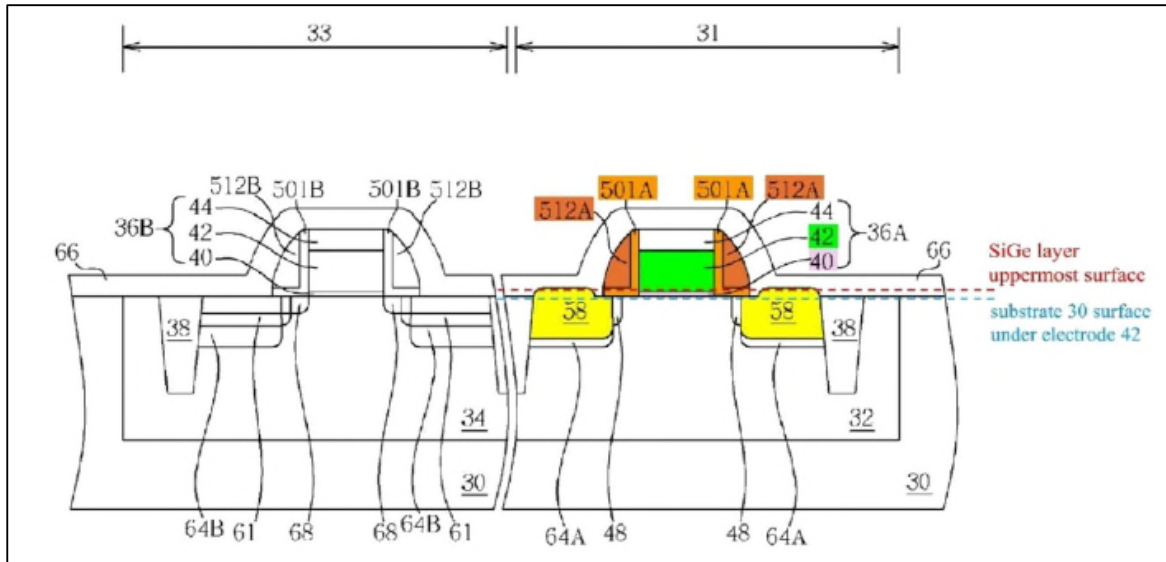
¹¹ Wu922’s SiGe layer 58 is “formed” before spacer 512A exists. If the “first sidewall spacer” need not exist when the first source/drain region is “formed,” the “first sidewall spacer” may further include Wu922’s spacer 512A. (Wu922, Ex.1005 ¶¶[0024]-[0025], ¶¶[0043]-[0044]; Ex.1101, ¶196.)

7. **Element 1[f]: “a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress”**

Wu922 discloses a strained “contact etch stop layer (CESL) 66 on the surface of the gate structures 36A, 36B, the second spacers 512A, 512B, and the sources/drains 64A, 64B” (*see* Figure A). (Wu922, Ex.1005 ¶¶[0025], ¶[0044], FIGS. 7, 14.) Both Wu922 and Alvarez teach a silicon nitride CESL. (Wu922, Ex.1005 ¶[0025]; Alvarez, Ex.1006 ¶[0047].) As Alvarez demonstrates, a POSITA would have found it obvious for Wu922’s silicon nitride CESL to cause tensile stress (opposite the SiGe compressive stress). (Alvarez, Ex.1006 ¶¶[0047]-[0049], ¶[0054], ¶¶[0065]-[0066], ¶[0069], Tbl. 1, FIGS. 9-11; *Supra* §VI.A.1; Ex.1101, ¶¶198-200.)

8. **Element 1[g]: “an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode”**

SiGe layer 58 “project[s] from the top surface of the semiconductor substrate 30.” (Wu922, Ex.1005 ¶¶[0021], ¶[0041], FIGS. 7, 14.) Wu922’s FIGS. 4-7 and 12-14 show the top surface of SiGe layer 58 extending above substrate 30 (*see* Figure A). (Wu922, Ex.1005 ¶¶[0021], ¶[0041], FIGS. 4-7, 12-14; Ex.1101, ¶¶201-202.)



Wu922, Ex.1005, FIG. 14

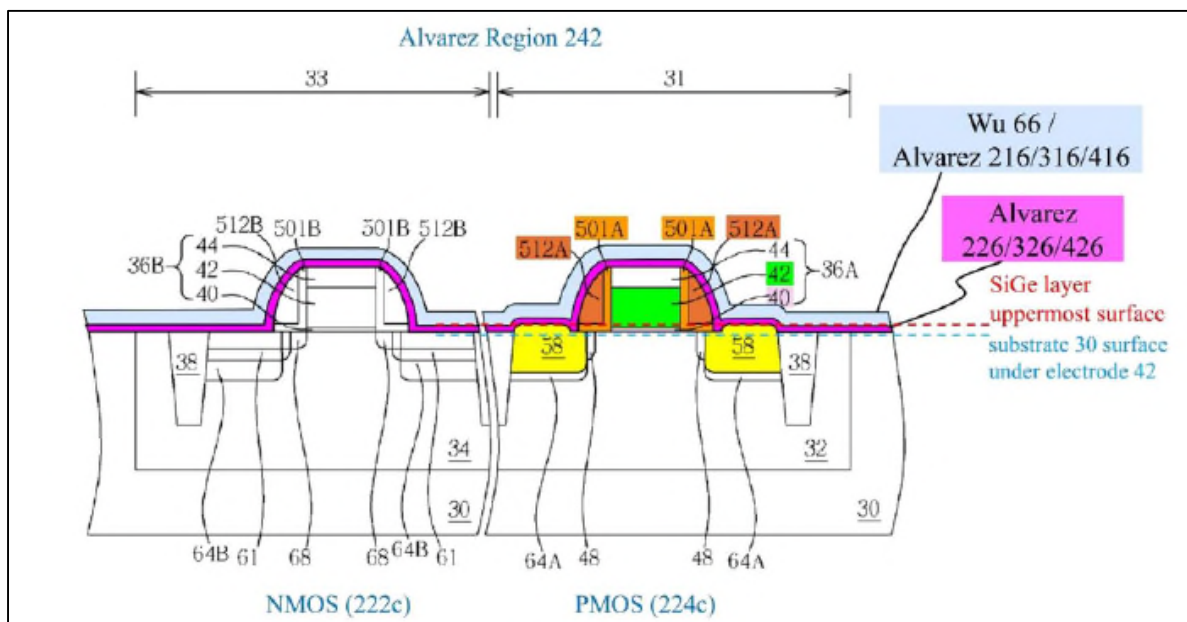


Figure A

9. Element 1[h]: “a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer”

The combination includes a first stress-relief film (magenta) (analogous to Alvarez’s stress-controlling layer(s)) formed in a space between SiGe layer 58 and first sidewall spacer 501A¹² created by removing sacrificial layer 52 (see Figure A). (Wu922, FIGS. 6, 13, 14; *Supra* §VI.A.1; Ex.1101, ¶203.) According to Alvarez, stress-control layer 226/326/426 may be silicon oxide. (Alvarez, Ex.1006 ¶[0043], ¶¶[0063]-[0065], FIGS. 9-11.)

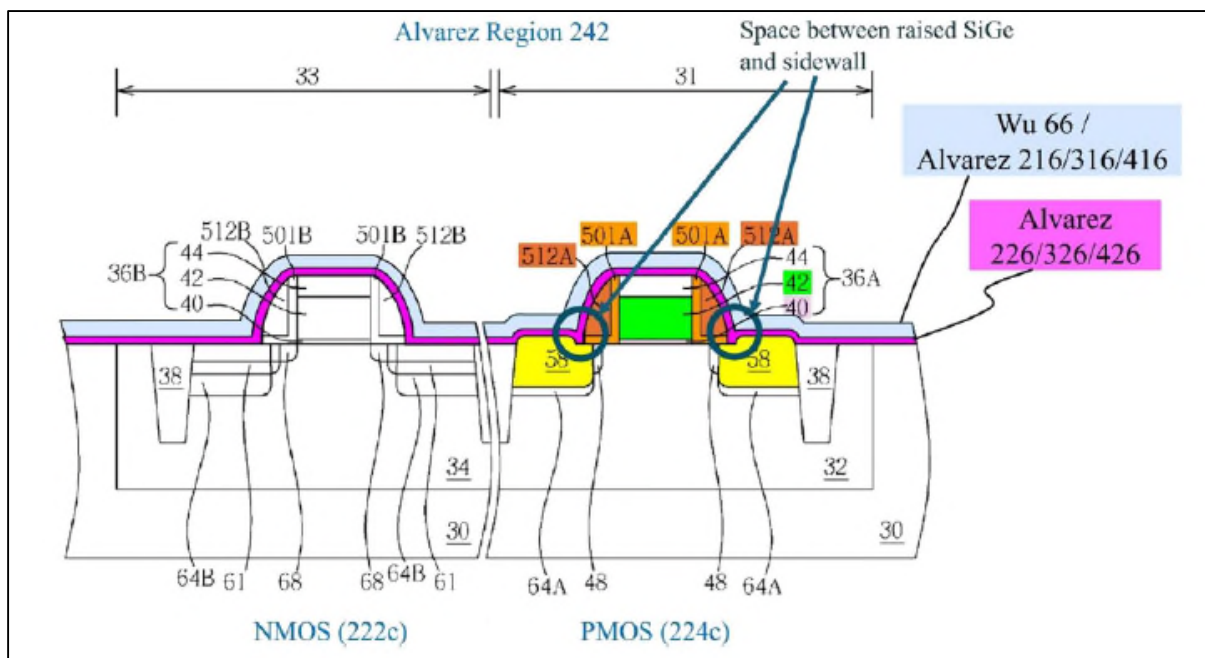


Figure A

¹² *Supra* note 11.

10. Element 1[i]: “the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween”

The combination includes the first stress-relief film (stress-controlling layer 226/326/426 (magenta)) formed on the side surface of the first gate electrode (PMOS gate electrode 42, green) with first sidewall spacer 501A¹³ (orange) interposed therebetween. (*Supra* §VI.A.1) The first stress-relief film forms on the sides of gate electrode 42, including in the space between the first sidewall spacer 501A¹⁴ and SiGe layer 58, with the sidewall spacer between the stress-relief film and gate electrode (*see* Figure A). (Ex.1101, ¶¶204-205.)

11. Element 1[j]: “the first stress-relief film is not in direct contact with the side surface of the first gate electrode”

The first stress-relief film (magenta) does not directly contact a side surface of gate electrode 42 (green) because the sidewall spacer (orange) separates them. (*see* Figure A). (*Supra* §VI.A.1, §§VI.B.9-10; Ex.1101, ¶¶206-207.)

C. Claim 3: “The semiconductor device of claim 1, further comprising: a first silicide layer formed on the first gate electrode; and a second silicide layer formed on the first source/drain region which includes the silicon compound layer”

The alternative mapping in Figure A’ (showing a silicide region like Alvarez’s region 330) includes a stress-control film 350/450 (first stress-relief film)

¹³ *Supra* note 11.

¹⁴ *Id.*

“compris[ing] similar materials, dimensions, and deposition methods and parameters as described for ... stress-controlling material 226.” (Alvarez, Ex.1006 ¶[0064].) It overlays Wu922’s optional “silicide layer[s]” (burgundy) formed both on the “gate structures” (first silicide layer) and “surfaces of the [SiGe] source/drain” regions (second silicide layer). (Wu922, Ex.1005 ¶[0024], ¶[0043]; *see* Alvarez, Ex.1006 ¶[0064], FIG. 10.) Again, stress-control film 350/450 would have been obvious for tuning stress in region 330, and the silicide reduces contact resistance. (*Supra* §VI.A.1; Ex.1101, ¶¶208-215.)

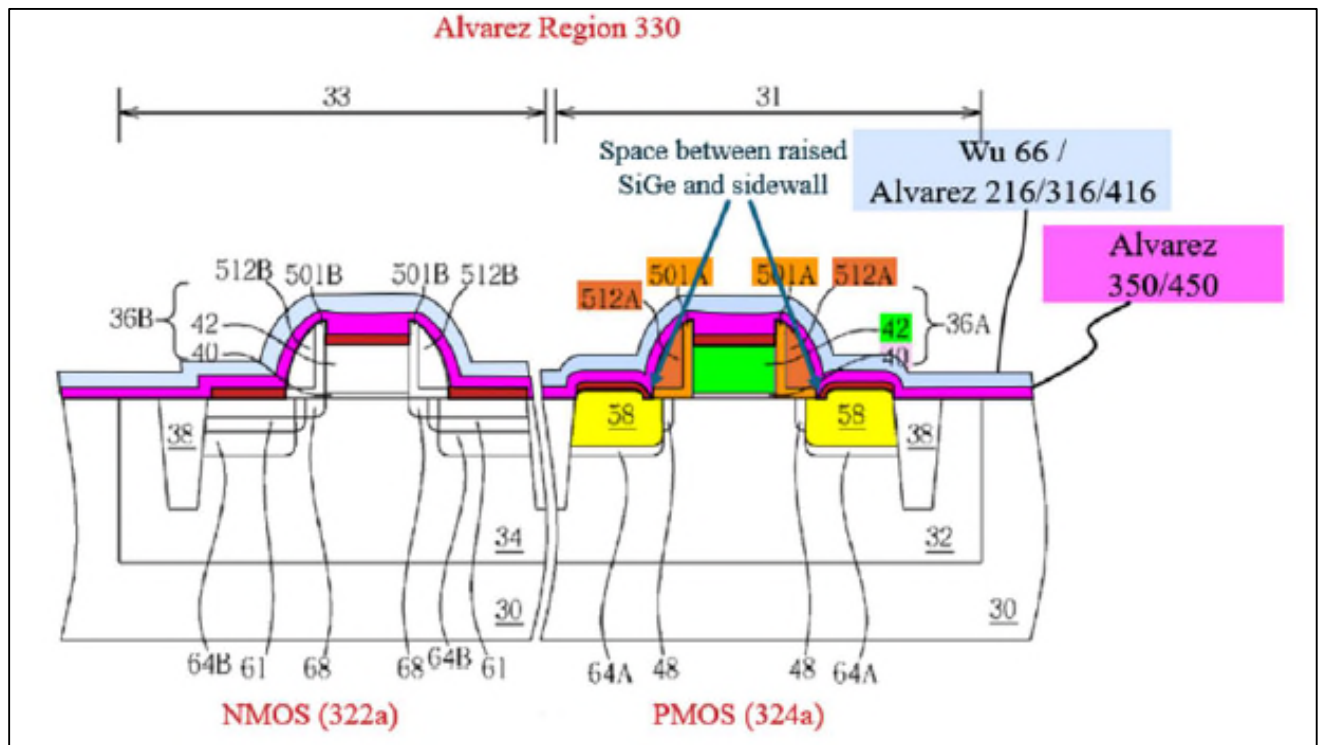
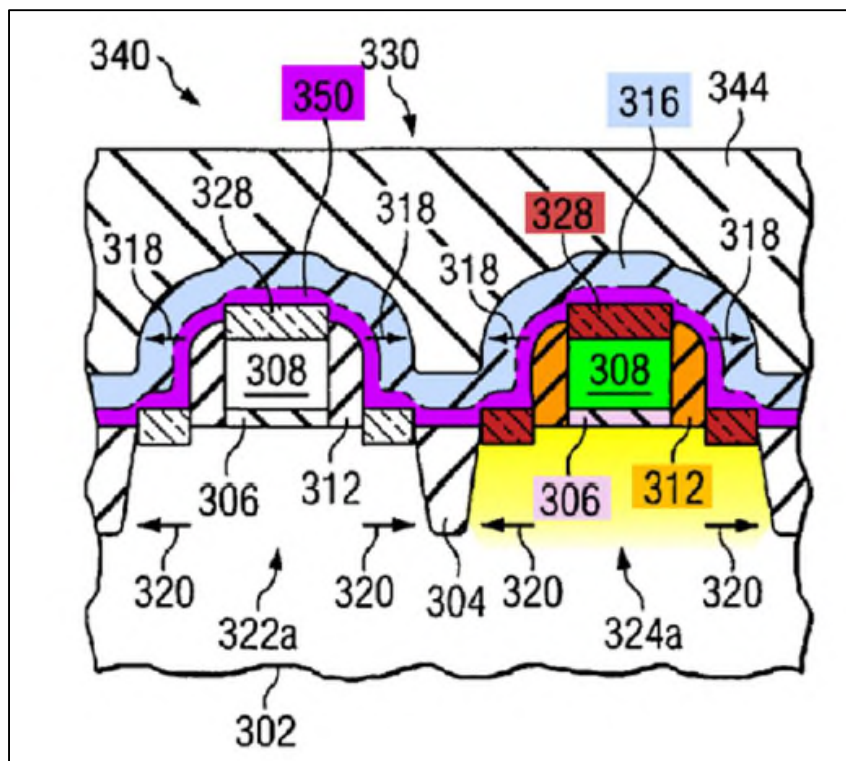


Figure A'



Alvarez, Ex.1006, FIG. 10 (excerpted)

This embodiment of the combination satisfies claim 1 for the same reasons described above (*Supra* §§VI.A.1.a-b), since including the optional silicide does not materially affect that analysis. (Alvarez, Ex.1006 ¶¶[0063]-[0064]; Ex.1101, ¶¶208-210.)

D. Claim 4: “The semiconductor device of claim 1, wherein the first stress-relief film is formed on a side surface of the silicon compound layer”

The proposed combination includes a stress-controlling film 226/326/426 (first stress-relief film) formed on a side surface of SiGe layer 58 in a space created by removing sacrificial layer 52 (*see* Figure A). (*Supra* §VI.A.1, §VI.B.9); Ex.1101, ¶¶216.)

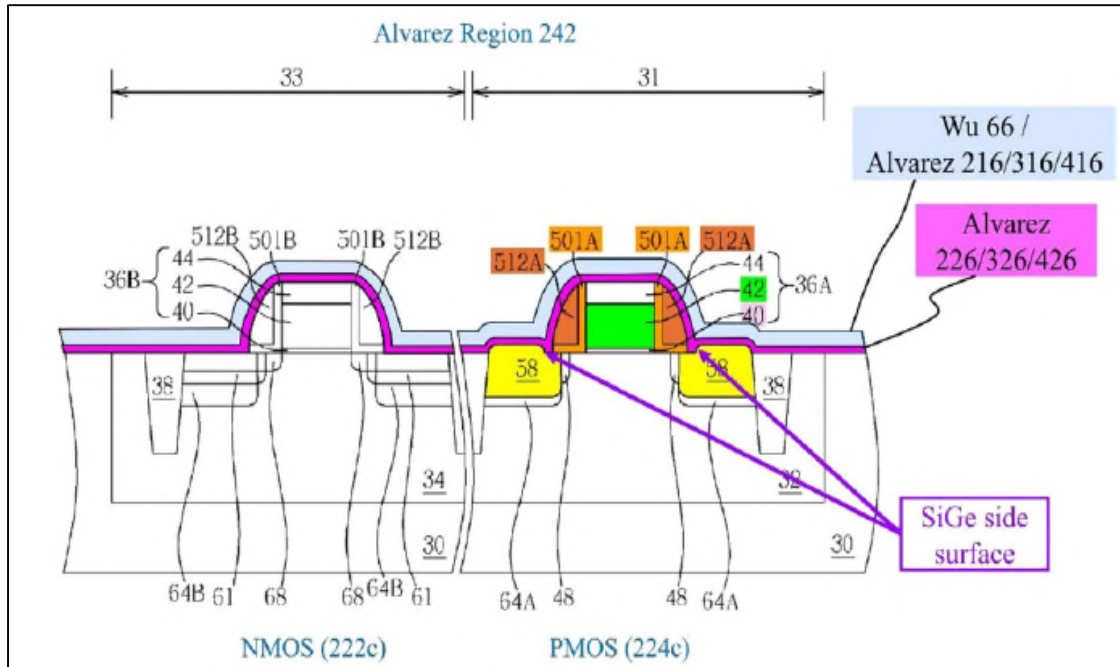


Figure A

E. Claim 7:

1. Element 7[pre]: “The semiconductor device of claim 1”

For the same reasons described in Sections VI.B.1-11, the Wu922-Alvarez combination discloses the semiconductor device of claim 1. (*Supra* §§VI.B.1-11; Ex.1101, ¶217)

2. Element 7[a]: “the first MIS transistor is a p-type MIS transistor”

Wu922 discloses that the first MIS transistor is a pFET, or a “p-type” MIS transistor, in “PMOS transistor region 31.” (Wu922, Ex.1005 ¶[0017].) The Wu922-Alvarez combination discussed for claim 1 (Figure A) includes the pFET in a region like Alvarez’s stress-control region 242. (*Supra* §VI.B.2; Ex.1101, ¶218.)

3. Element 7[b]: “the first stress is a compressive stress”

Wu922 discloses that “an epitaxial layer 58 of silicon germanium [SiGe]” layer causes that causes compressive stress to the channel because “epitaxial layer 58 has a lattice constant greater than that of the semiconductor substrate 30.” (Wu922 ¶[0005] ¶[0019], ¶[0021], ¶[0041].) The embodiment of the Wu922-Alvarez combination discussed for claim 1 (Figure A) incorporates Wu922’s epitaxial SiGe regions 58, which induce a first compressive stress in the pFET channel region. (*Supra* §VI.B.6; Ex.1101, ¶219.)

4. Element 7[c]: “the second stress is a tensile stress”

Both Wu922 and Alvarez teach a strained silicon nitride CESL and Alvarez discloses the layer causing a tensile stress. (Wu922, Ex.1005 ¶[0025]; Alvarez, Ex.1006 ¶[0047], ¶¶[0065]-[0066].) The embodiment of the Wu922-Alvarez combination shown in Figure A has a tensile stress inducing CESL layer that causes a tensile stress on the transistor (opposite the SiGe compressive stress). (Alvarez, Ex.1006 ¶¶[0048]-[0049], ¶[0022], ¶[0054], ¶¶[0065]-[0066], ¶[0069].) (*Supra* §VI.A.1 §VI.B.7; Ex.1101, ¶220.)

F. Claim 8:

1. Element 8[pre]: “The semiconductor device of claim 1”

For the same reasons described in Sections VI.B.1-11, the Wu922-Alvarez combination discloses the semiconductor device of claim 1. (*Supra* §VI.B.6; Ex.1101, ¶221.)

2. Element 8[a]: “the silicon compound layer is a SiGe layer”

Wu922 discloses that “epitaxial layer 58” may be “silicon germanium” (SiGe) when the first active area is PMOS transistor region 31. (Wu922, Ex.1005 ¶[0021], ¶[0041], ¶[0050].) The embodiment of the Wu922-Alvarez combination discussed for claim 1 (Figure A) has Wu922’s epitaxial SiGe layer 58. (*Supra* §VI.B.6; Ex.1101, ¶222.)

3. Element 8[b]: “the stress insulating film is a silicon nitride film”

Both Wu922 and Alvarez disclose that the CESL layer may be made of silicon nitride. (Wu922, Ex.1005 ¶[0025]; Alvarez ¶[0022], ¶[0047].) (*Supra* §VI.A.1, §VI.B.7; Ex.1101, ¶223.)

4. Element 8[c]: “the first stress-relief film is a silicon oxide film”

Alvarez discloses that the stress relief film, like Alvarez’s stress-controlling film 226/326/426, may be “an oxide such as silicon dioxide.” (Alvarez, Ex.1006 ¶[0043], Claim 13). (*Supra* §VI.B.9; Ex.1101, ¶224.)

G. Claim 11:

1. Element 11[pre]: “The semiconductor device of claim 1”

For the same reasons described in Sections VI.B.1-11, the Wu922-Alvarez combination discloses the semiconductor device of claim 1. (*Supra* §§VI.B.1-11; Ex.1101, ¶225.)

2. Element 11[a]: “a second MIS transistor”

Wu922 discloses “NMOS transistor region 33.” (Wu922, Ex.1005 ¶[0017], ¶[0038], FIGS. 1-7, 9-14; Ex.1101, ¶¶226-228.) As Figures C and D show, in an exemplary combination second MIS transistor 33 includes a stress-controlling layer 226/326/426 (as in Alvarez’s region 242), and CESL 66 is tensile. (*Supra* §VI.B.7.)

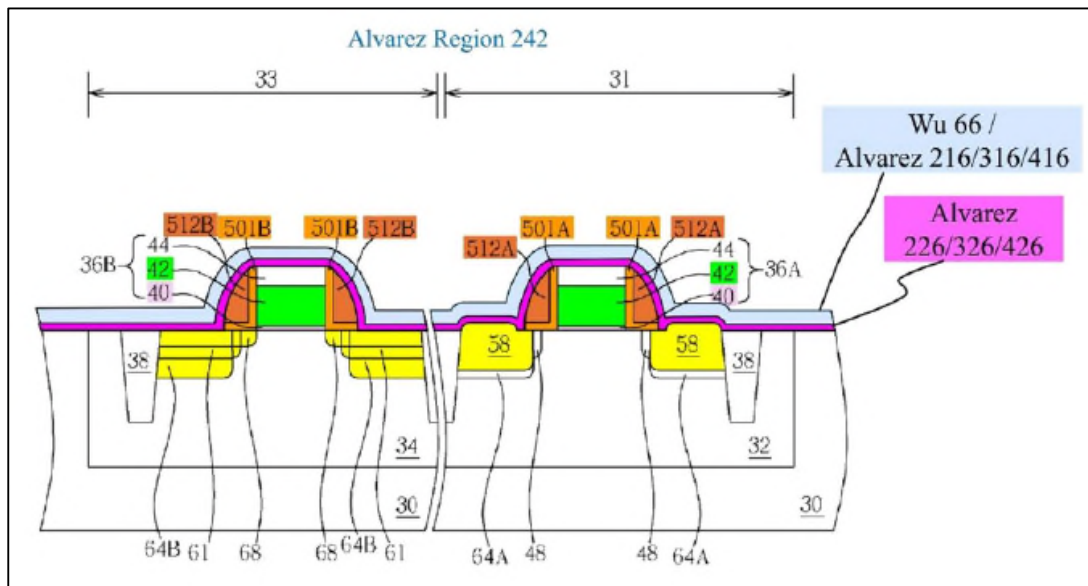


Figure C

Alternatively, an NMOS like 222a in silicide region 230 is a second MIS transistor. (Alvarez, Ex.1006 ¶[0042], ¶[0044], ¶¶[0046]-[0047], FIGS. 8-9.) There, Wu922’s transistor 33 would have a tensile CESL 66 but no stress-relief layer. (Wu922, Ex.1005 ¶[0024], ¶[0043] (silicide optional).) Figure D shows the equivalent of Alvarez’s region 230 (with silicided NMOS 222a) and region 242 (with stress-controlled NMOS 222c) in the asserted combination. (Ex.1101, ¶228.)

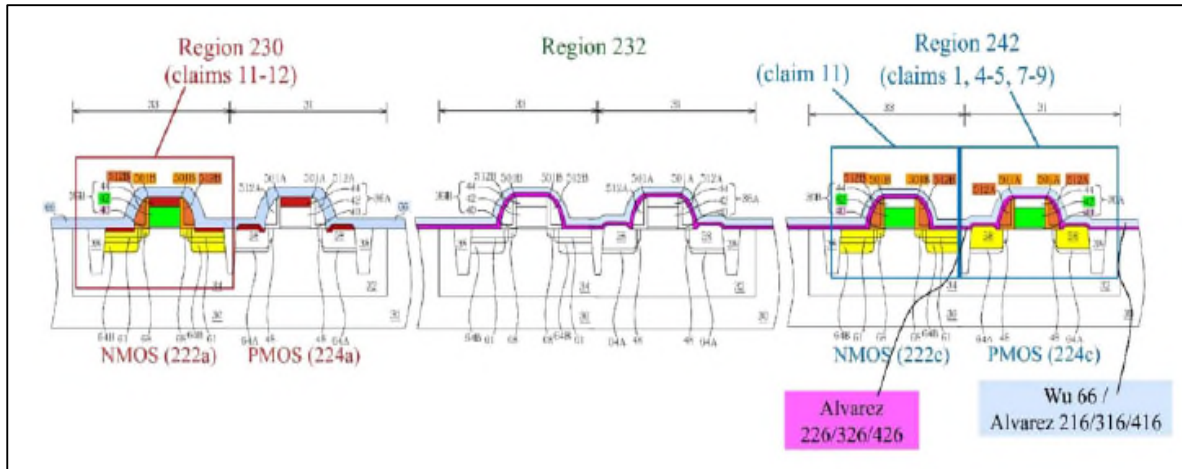
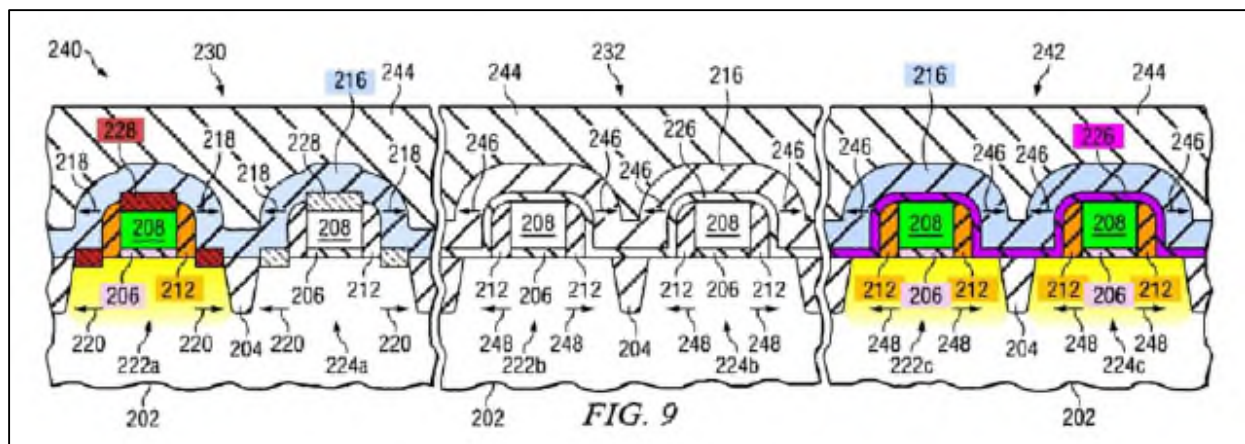


Figure D



Alvarez, Ex.1006, FIG. 9

3. Element 11[b]: “a second gate insulating film formed on a second active region in the semiconductor substrate”

For both combination embodiments regarding claim 11 (*Supra* §VI.G.2), Wu922 discloses a second gate insulating film (gate dielectric layer 40) formed on NMOS transistor region 33 of substrate 30 (*see* Figures C, D). (Wu922, Ex.1005 ¶[0017], ¶[0038]-[0039]; Ex.1101, ¶229.)

4. Element 11[c]: “a second gate electrode formed on the second gate insulating film”

For both combination embodiments regarding claim 11 (*Supra* §VI.G.2), Wu922 discloses a second gate electrode (gate 42) formed on gate dielectric 40 (*see* Figures C, D). (Wu922, Ex.1005 ¶[0017]; Ex.1101, ¶¶230-231; *Supra* §VI.A.1.)

5. Element 11[d]: “a second sidewall spacer formed on a side surface of the second gate electrode”

For both combination embodiments regarding claim 11 (*Supra* §VI.G.2), Wu922 discloses a second sidewall spacer comprising spacers 501B and/or 512B formed on a side surface of the gate electrode (gate 42) (*see* Figures C, D). (Wu922, Ex.1005 ¶[0017], ¶[0024], FIGS. 7, 14; Ex.1101, ¶¶232-233.)

6. Element 11[e]: “a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer”

For both combination embodiments regarding claim 11 (*Supra* §VI.G.2), Wu922 discloses n-type source/drain regions comprising “source/drain” 64B and “n-type lightly doped drain (NLDD) 60 [sic:61]” and “NLDD2 68,” each formed “in the P well 34 beside the gate structure 36B.” (Wu922, Ex.1005 ¶¶[0023]-[0024], ¶[0038], ¶¶[0042]-[0044], FIGS. 7, 14.) They are formed in the NMOS active region lateral to the second sidewall spacer (sidewalls 501B and/or 512B) (*see* Figures C, D). (Ex.1101, ¶234.)

7. Element 11[f]: “the stress insulating film formed on the second active region to cover the second gate electrode, the second sidewall spacer, and the second source/drain region”

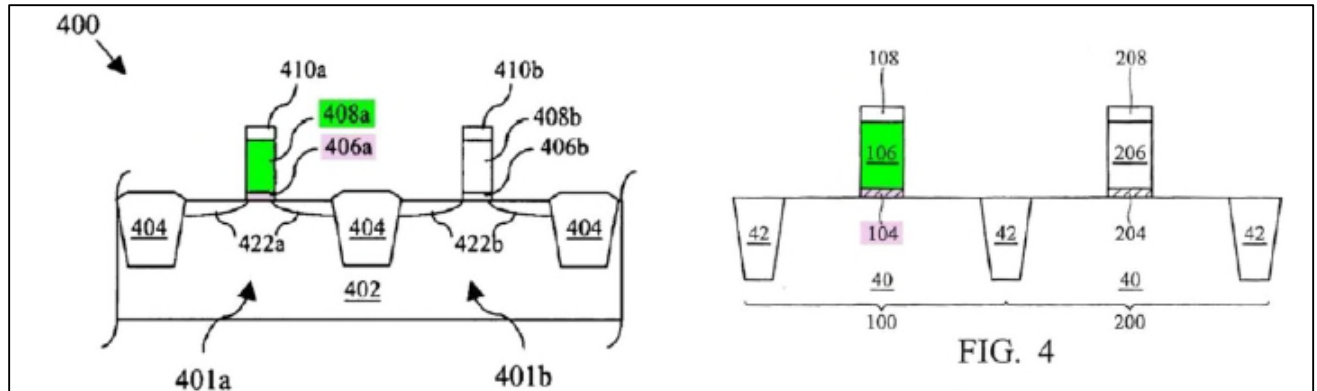
For both combination embodiments regarding claim 11 (*Supra* §VI.G.2), the stress insulating film (Wu922’s CESL 66) blankets both PMOS and NMOS devices (*see* Figures C, D). (Ex.1101, ¶¶235-236; *see* Wu922, Ex.1005 ¶[0025], ¶[0044], FIG. 14; Alvarez, Ex.1006 ¶¶[0043]-[0050], ¶[0063]-[0068], FIGS. 8-11.)

VII. GROUND 2: Cheng817 Along or in View of Wang906 Renders Claims 1, 3, 4, 7, 8 and 11 Obvious.

A. Overview

Cheng817 and Wang906 describe similar MOS devices formed using similar processes. (*Compare* Cheng817, Ex.1008 ¶¶[0056]-[0070], Figs. 4a-4j, *with* Wang906, Ex.1009 ¶¶[0023][0032], FIGS. 4-9.) Considering Cheng817’s descriptions and figures in conjunction with Wang906’s helps demonstrate how a POSITA would have understood Cheng817’s disclosures. (Ex.1101, ¶¶239-240.)

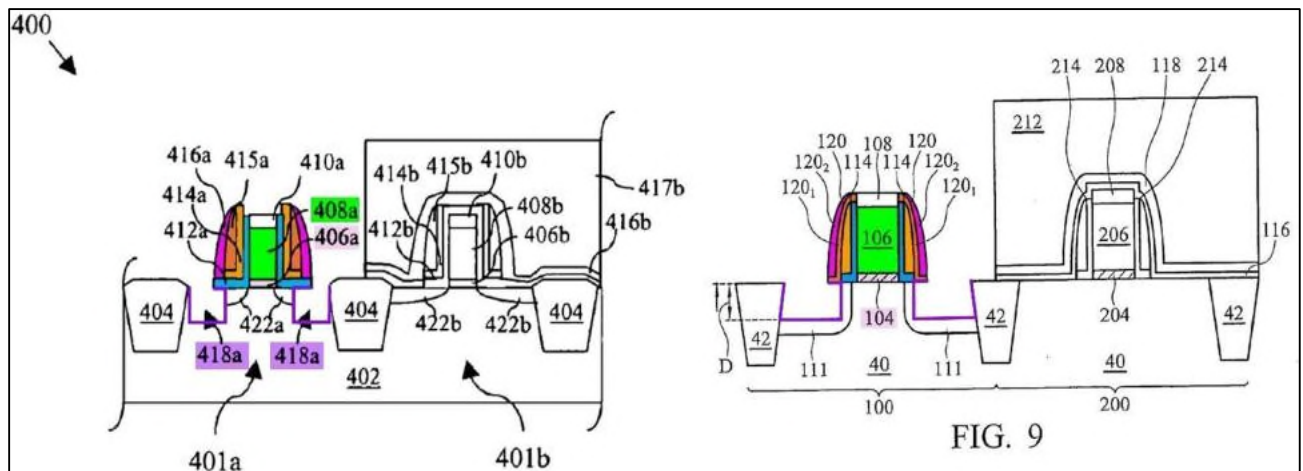
Cheng817’s Fig. 4a, like Wang906’s FIG. 4, shows forming gate dielectric and gate electrode layers. (Cheng817, Ex.1008 ¶[0056], Fig. 4a; Wang906, Ex.1009 ¶[0023], FIG. 4.)



Cheng817, Ex.1008, Fig. 4a

Wang906, Ex.1009, FIG. 4

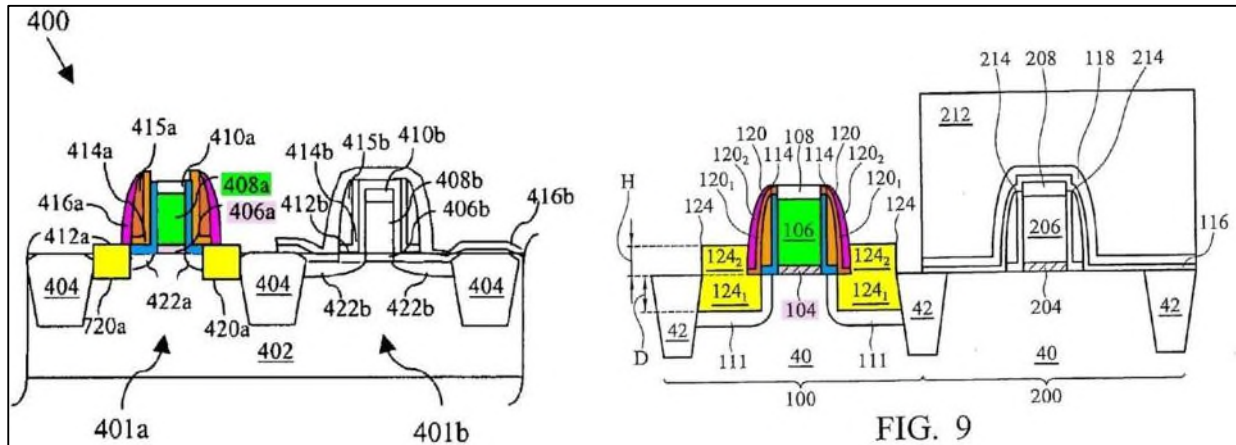
Cheng817's Figs. 4b-4d, like Wang906's FIGS. 5-8, show forming gate electrode sidewalls, then etching recesses for SiGe growth. (Cheng817, Ex.1008 ¶¶[0061]-[0063], Figs. 4b-4c; Wang906, Ex.1009 ¶¶[0025]-[0028], FIGS. 5-8.) In Cheng817's PMOS 401a of Fig. 4d, sidewall dielectric 412a (blue) lies below dummy spacer 416a (magenta), akin to how Wang906's sidewall portion 1201 lies below sidewall portion 1202 (magenta). (Cheng817, Ex.1008 ¶[0064], Fig. 4d; Wang906, Ex.1009 ¶[0029], FIG. 9; Ex.1101, ¶¶240-241.)



Cheng817, Ex.1008, Fig. 4d

**Wang906, Ex.1009, FIG. 9*
(*modified to remove SiGe)**

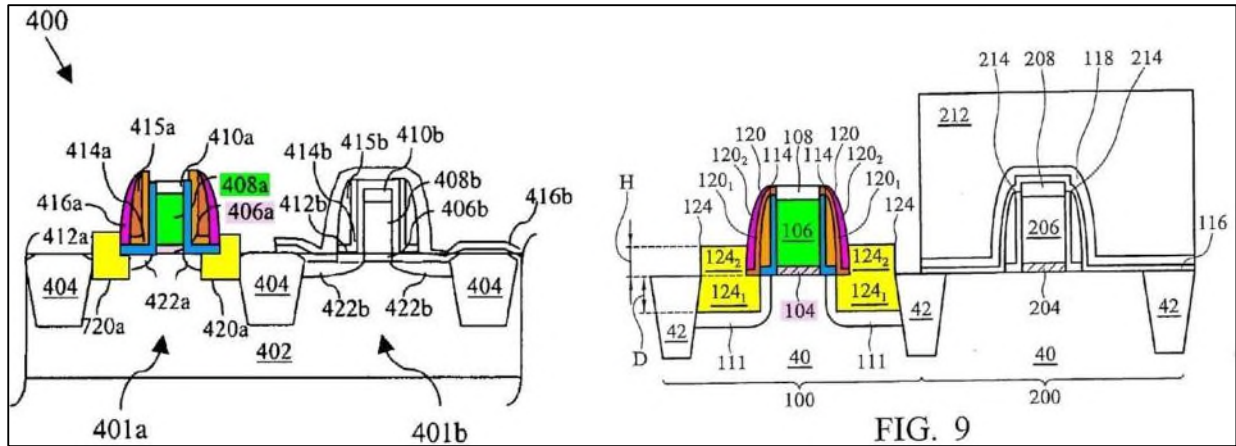
Cheng817's Fig. 4e, like Wang906's FIG. 9, shows SiGe grown in the trenches and extending above the substrate. (Cheng817, Ex.1008 ¶[0022], ¶[0065], Fig. 4e; Wang906, Ex.1009 ¶¶[0030]-[0032], FIG. 9.)



Cheng817, Ex.1008, Fig. 4d

Wang906, Ex.1009, FIG. 9*

A POSITA would have understood from Cheng817's textual descriptions that Fig. 4e contains a rendering error where the epitaxial regions (720a [sic:420a] and 420a) appear to replace part of layer 412a (blue). (Ex.1101, ¶¶242-243.) The epitaxial regions in Cheng817's Fig. 4e instead necessarily grow selectively on the crystalline trench surfaces and extend up and around the non-crystalline sidewalls, as in corrected Fig. 4e below (left). (Cheng817, Ex.1008 ¶[0065]; Wang906, Ex.1009 ¶¶[0030]-[0031], FIG. 9; Bohr, Ex.1527, ¶¶[0024]-[0028], FIGS. 4-6; Ex.1101, ¶¶239-240.) It would not replace the sidewall. (Ex.1101, ¶¶243-244.)



Cheng817, Ex.1008, Fig. 4d

Wang906, Ex.1009, FIG. 9*

Consistent with corrected Fig. 4e, “[t]he height of raised source/drain regions may” extend as much as “about 100 nm” above the substrate, substantially higher than the top of the 0.5-10 nm thick gate dielectric 406a (lavender). (Cheng817, Ex.1008 ¶¶[0018], ¶¶[0022].) Wang906 similarly explains that “raised [SiGe] portions 1242 preferably have a height H ... between about 100 Å and about 700 Å [10-70nm].” (Wang906, Ex.1009 ¶¶[0031].)

A POSITA would have recognized this correction should carry through in Cheng817’s Figs. 4f-4j. (Cheng817, Ex.1008 ¶¶[0066]-[0070]; Ex.1101, ¶245.) Figure I below modifies Cheng817’s Fig. 4j to show how this correction affects Cheng817’s final device. (Ex.1101, ¶246.) A POSITA would have found obvious, from Cheng817’s disclosures alone or in combination with Wang906’s, that Cheng817 describes a PMOS transistor consistent with Figure I, which more accurately illustrates the process Cheng817’s text describes. (Ex.1101, ¶¶246-248; Cheng817, Ex.1008 ¶¶[0056]-[0070].)

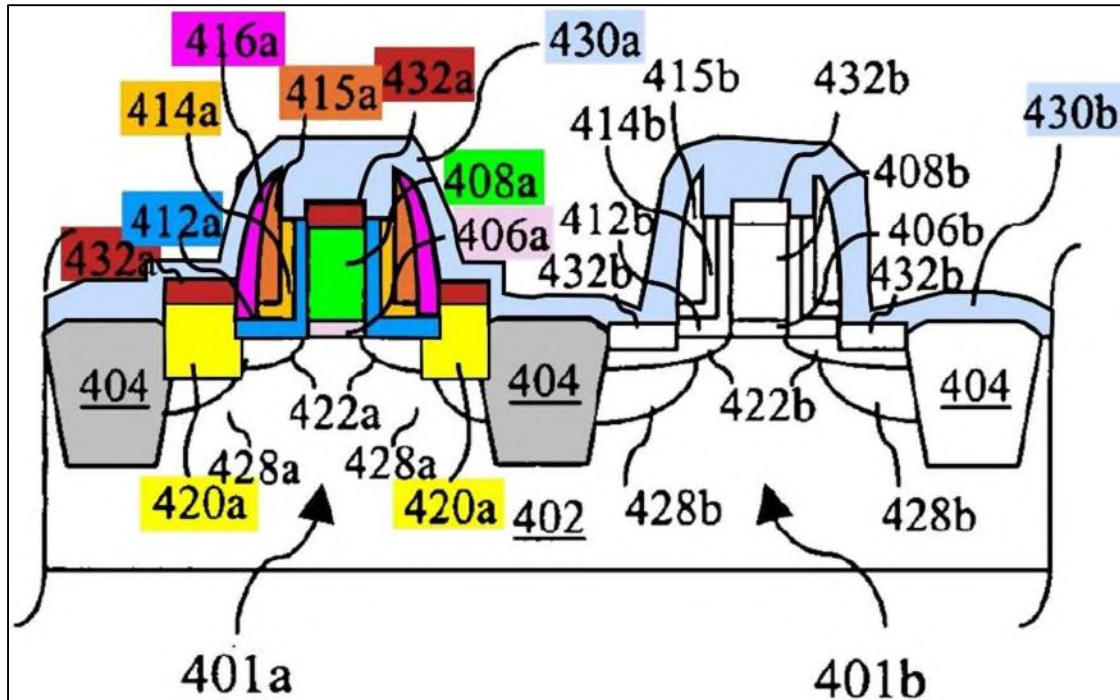


Figure I (Cheng817, Ex.1008, Fig. 4j, corrected)

A POSITA would have found this structure obvious because it applies a known teaching, motivation, or suggestion in the prior art (Cheng817’s express disclosures regarding Figs. 4a-4j, alone or in combination with Wang906’s descriptions of FIGS. 4-9) to arrive at the claimed invention (reflected in Figure I). (KSR, 550 U.S. at 416-21.) “A person of ordinary skill is ... not an automaton” and would have understood this. (*Id.*, 421; Ex.1101, ¶249.)

B. Independent Claim 1

1. **Element 1[pre]: “A semiconductor device comprising: a first MIS transistor, ... includ[ing]:”**

Cheng817 discloses “semiconductor devices 401a and 401b.” (Cheng817, Ex.1008 ¶¶[0056]-[0071], Fig. 4j; Ex.1101, ¶250.)

2. Element 1[a]: “a first MIS transistor, ... includ[ing]:”

Cheng817 discloses “a P-type MOS device” 401a. (Cheng817, Ex.1008 ¶¶[0056]-[0071],

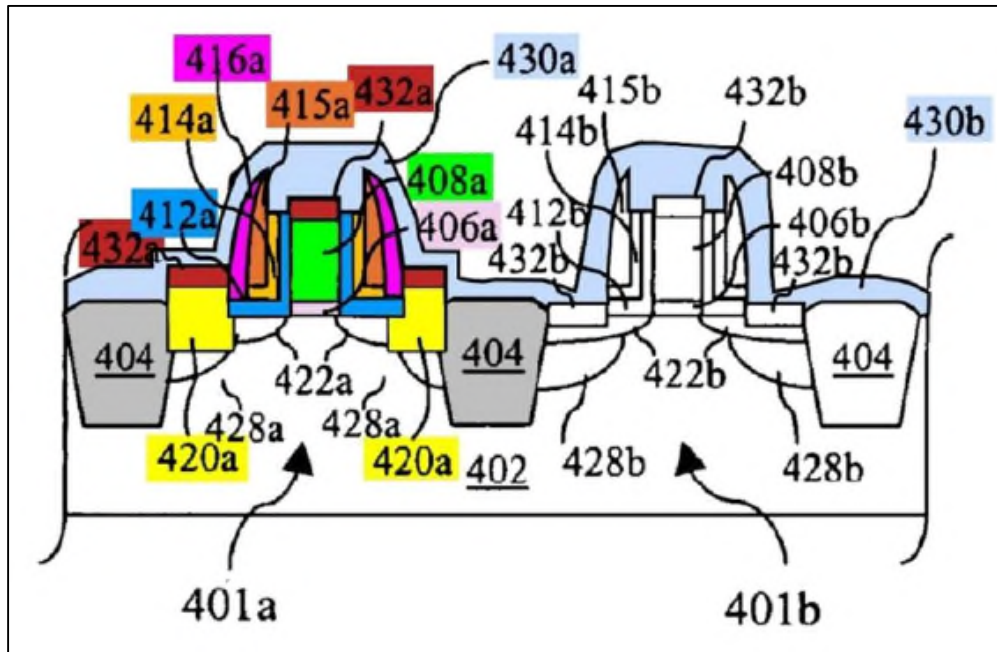


Figure I

3. Element 1[b]: “a first gate insulating film formed on a first active region in a semiconductor substrate”

Cheng817 discloses a first gate insulating film (gate dielectric 406a) “formed over a substrate 402.” (Cheng817, Ex.1008 ¶¶[0056], Fig. 4j; Ex.1101, ¶¶252-254.) Substrate 402 contains an active region comprising LDD regions 422a, source/drain regions 420a, heavily doped regions 428a, and the surrounding semiconductor regions. (Cheng817, Ex.1008 ¶¶[0060], ¶¶[0065]-[0068], Fig. 4j.)

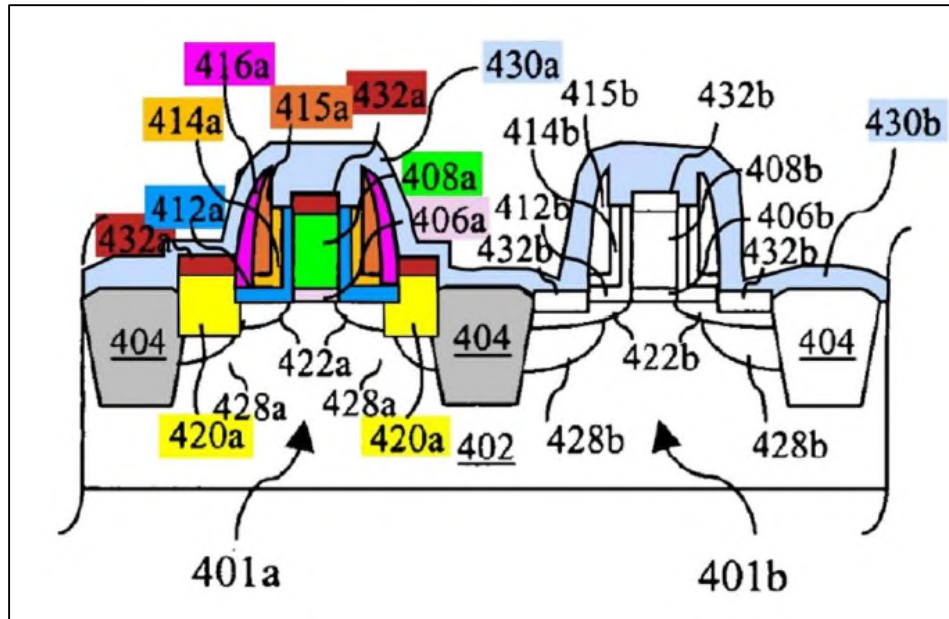


Figure I

4. Element 1[c]: “a first gate electrode formed on the first gate insulating film”

Cheng817 discloses a first gate electrode (gate electrode 408a) formed on the first gate insulating film (gate dielectric 406a). (Cheng817, Ex.1008 ¶[0056]; Ex.1101, ¶[255].)

5. Element 1[d]: “a first sidewall spacer formed on a side surface of the first gate electrode”

Cheng817 discloses a first sidewall spacer comprising sidewall structures 414a (light orange) and spacers 415a (dark orange) on the side surface of gate electrode 408a (green). (Cheng817, Ex.1008 ¶¶[0061]-[0062]; Ex.1101, ¶¶[256-257].)

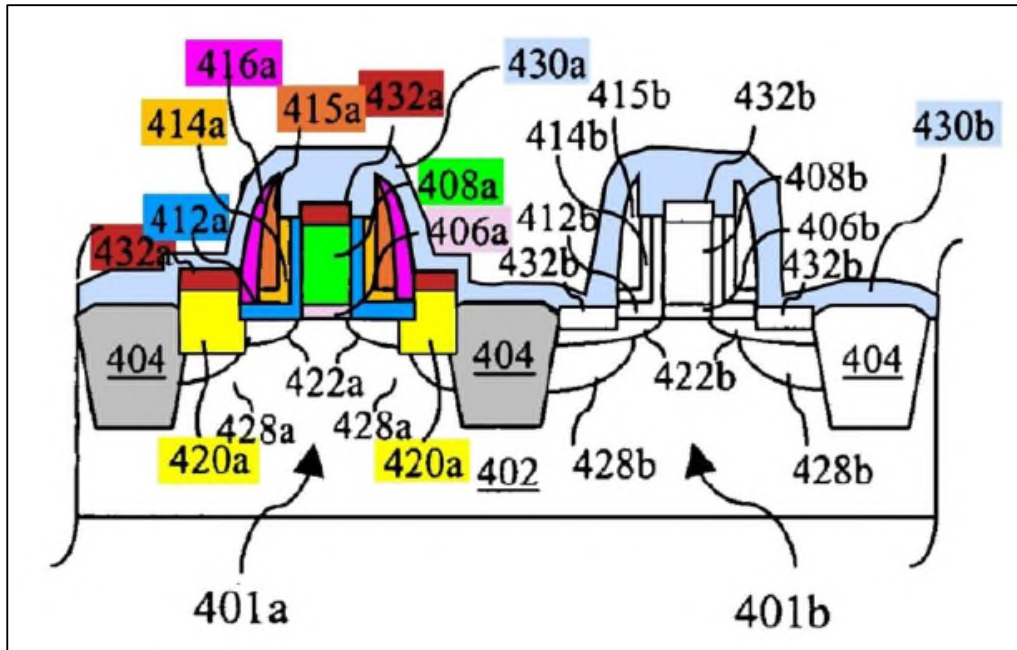


Figure I

6. **Element 1[e]: “a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region”**

Cheng817 discloses “doped source and drain regions 420a ... built-up in the recessed regions 418a.” (Cheng817, Ex.1008 ¶[0065].) Recessed regions 418a are trenches formed by etching. (Cheng817, Ex.1008 ¶[0064].) “[S]ource and drain regions 420a” may comprise “silicon germanium,” which imparts a compressive stress along the gate length direction of the channel region in PMOS 401a. (Cheng817, Ex.1008 ¶[0065]; *Supra* §IV.A.2; Wang906, Ex.1009 ¶¶[0031]-[0032]; Bohr, Ex.1527, ¶[0024], ¶[0026], ¶[0028], FIGS. 4-7; Ex.1101, ¶¶258-259.) SiGe source/drain regions 420a and LDD regions 422a have p-type conductivity because

401a is a PMOS device. (Cheng817, Ex.1008 ¶[0056], ¶[0060], ¶[0065]; Ex.1101, ¶258.)

SiGe source/drain regions 420a are provided laterally next to the first sidewall spacers (sidewalls 414a and 415a) because they grow out of recesses 418a next to the sidewall spacers (*see* Figure I). (Cheng817, Ex.1008, Figs. 4d-4j; Ex.1101, ¶259.)

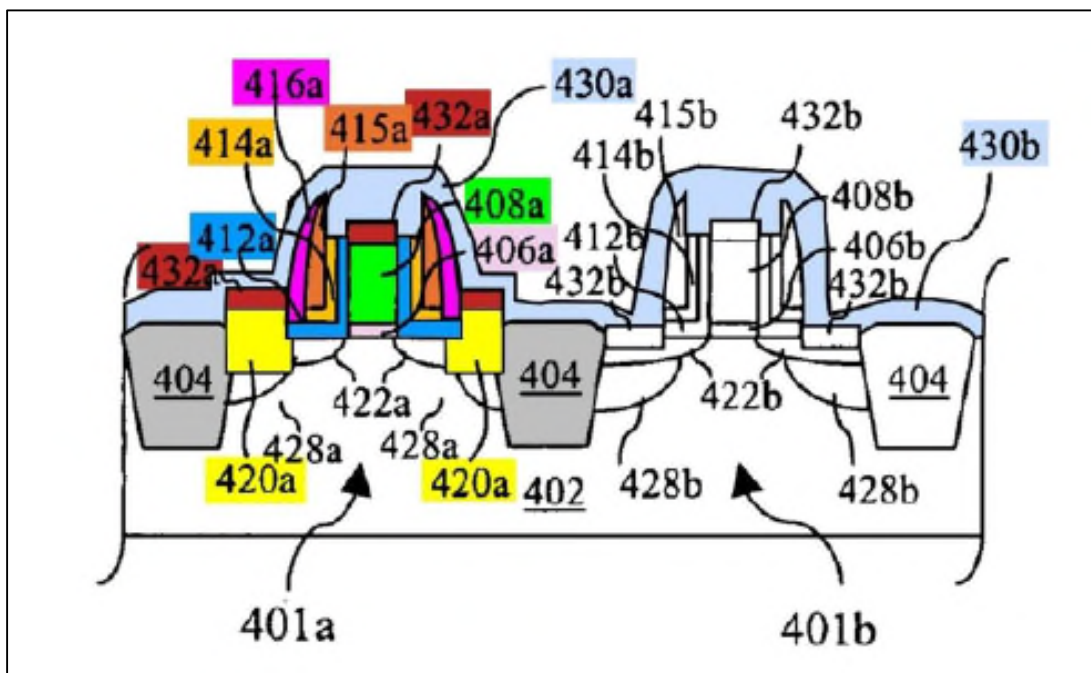


Figure I

7. **Element 1[f]: “a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress”**

Cheng817 discloses a stress insulating film, such as etch stop layer 430a/430b, formed over PMOS 401a to cover gate electrode 408a, sidewall spacers 414a and 415a, and SiGe source/drain regions 420a. (Cheng817, Ex.1008 ¶[0070], Fig. 4j;

Ex.1101, ¶¶260-261.) Etch stop layer 430a/430b may be silicon nitride and cause a tensile stress “between about +0.001 and about +50 GPa” opposite the SiGe compressive stress. (Cheng817, Ex.1008 ¶[0070].)

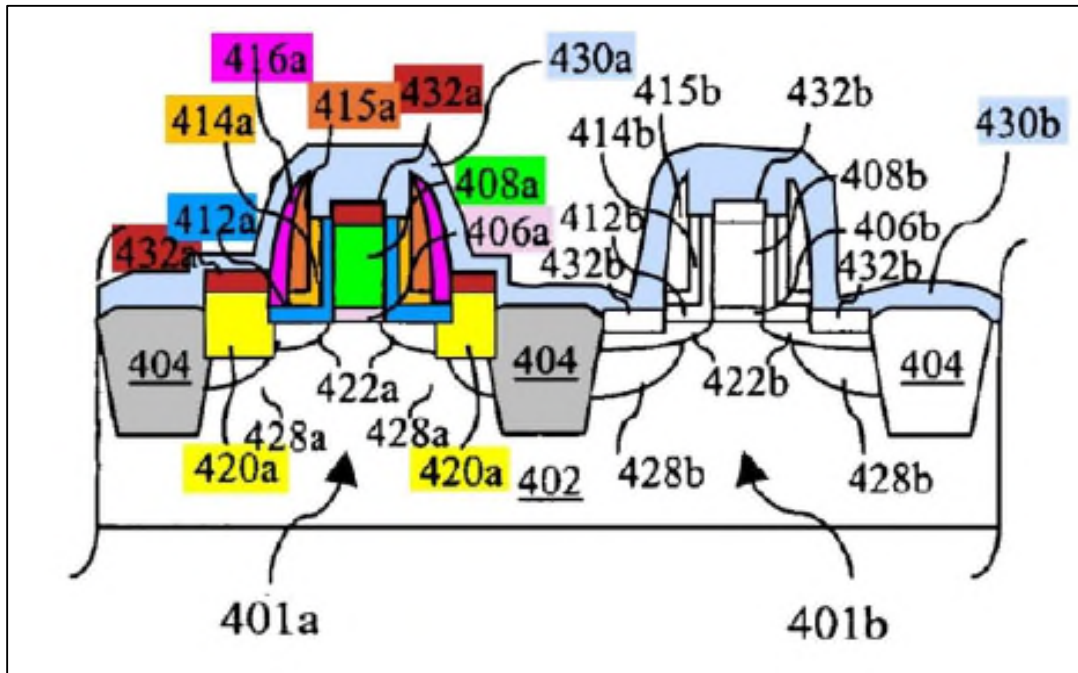
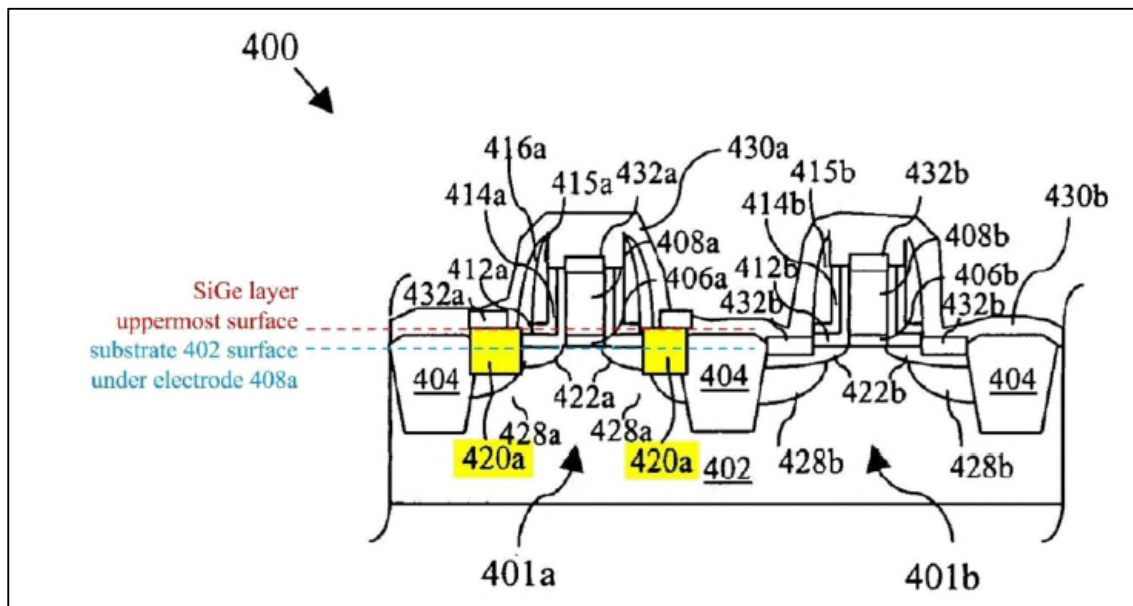


Figure I

It was well-known that a tensile CESL improves electron mobility in NMOS regions and that compressive SiGe improves PMOS region mobility. (*Supra* §IV.A.2; Hsu823, Ex.1506, ¶[0039]; Alvarez, Ex.1006 ¶[0024], ¶[0054], FIGS. 9-10 (tensile stress-inducing film 216/316/416); Doris, Ex.1429, ¶[0005], ¶¶[0034]-[0035]; Bohr, Ex.1527, ¶¶[0038]-[0039]; Murthy151, Ex.1526, ¶[0005]; Morin-2007, Ex.1528, 1-2; Ex.1101, ¶262.)

8. **Element 1[g]: “an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode”**

Cheng817 discloses that “source/drain regions 136,” analogous to source/drain regions 420a, “may extend above the substrate surface 106.” (Cheng817, Ex.1008 ¶[0022], ¶[0065].) A POSITA would have understood SiGe source/drain regions 420a likewise extend above the substrate. (*Supra* §VII.A; Cheng817, Ex.1008 ¶[0054], ¶[0065]; Ex.1101, ¶¶263-266.) Cheng817’s PMOS transistor “comprises *raised* source and drain regions” that are “built-up” and extend as much as “about 100 nm” above the substrate. Cheng817, Ex.1008 ¶[0022], ¶[0054], ¶[0065], Figs. 1, 4j.



Cheng817, Ex.1008, Fig. 4j

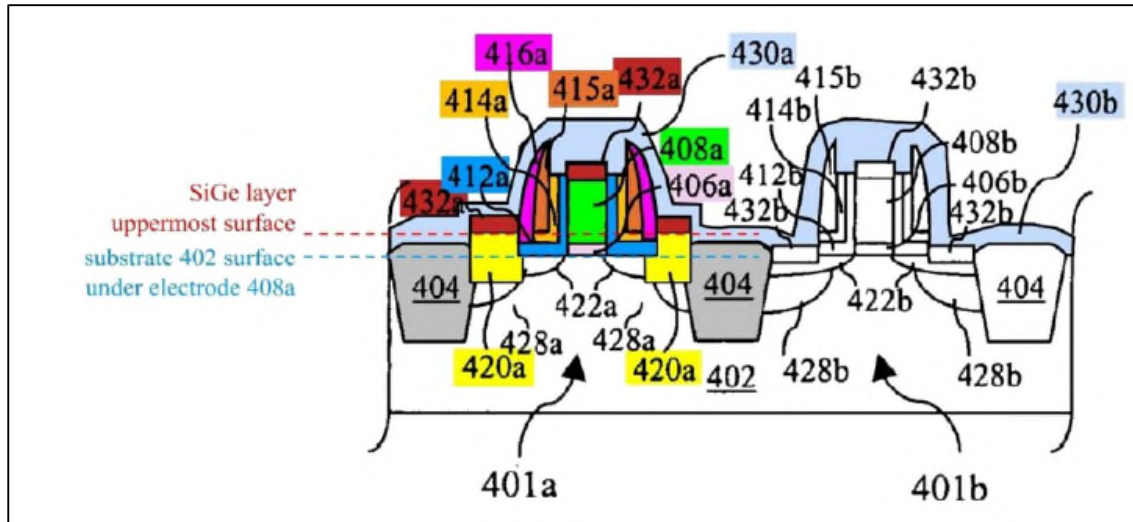


Figure I

9. Element 1[h]: “a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer”

Cheng817 discloses “dummy spacers 416a” made of “silicon dioxide (SiO₂)” formed between SiGe source/drain regions 420a (silicon compound layer) and sidewall spacers 414a and 415a, because the SiGe extends above the substrate and grows around the sidewalls. (Cheng817, Ex.1008 ¶[0063], Fig. 4j; *Supra* §VII.A, §VII.B.8; Ex.1101, ¶¶267.) Dummy spacers 416a would “prevent[] the tension” from a tensile overlayer “from materially adversely influencing the charge carrier mobility in the pFET [PMOS]” by defining “a neutral stress” buffer layer between a compressive SiGe layer and a tensile etch stop layer (e.g., Cheng817’s tensile layer 430a/430b). (Lee870, Ex.1431, ¶[0067]; Cheng810, Ex.1432, ¶[0030]; Doris, Ex.1429, ¶[0034], ¶[0042]; Ex.1101, ¶¶268-269.) This is like the ’425 patent, which describes “[a] first stress-relief film 28a ... in the space 24 between the silicon

compound layer 23 and the first sidewall 19A.” (the ’425 patent, Ex.1001, 14:51-54.)

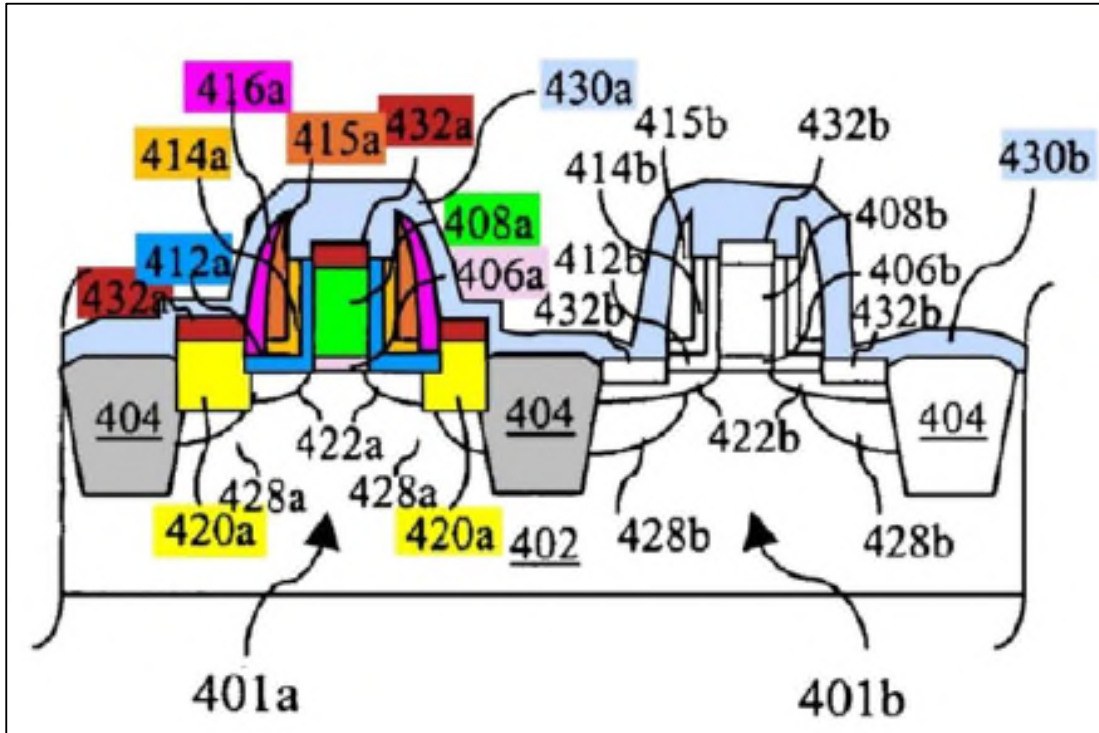


Figure I

10. Element 1[i]: “the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween”

Cheng817’s dummy spacer 416a (magenta) is formed on the side surface of gate electrode 408a (green), with the first sidewall spacer (sidewalls 414a and 415a) (orange) located between (see Figure I). (Cheng817, Ex.1008 ¶[0061], [0063], Figs. 4c-4j; *Supra* §VII.A, §VII.B.9; Ex.1101, ¶270.) SiGe source/drain regions 420a extend above the substrate surface and around the sidewall spacers. (*Supra* § VII.A, § VII.B.6; Ex.1101, ¶243.)

11. Element 1[j]: “the first stress-relief film is not in direct contact with the side surface of the first gate electrode”

The stress-relief film (spacer 416a, magenta) does not directly contact a side surface of gate electrode 408a (green) because the sidewall spacer (sidewalls 414a and 415a) (orange) separates them. (*Supra* §§VII.B.9-10; Ex.1101, ¶271.)

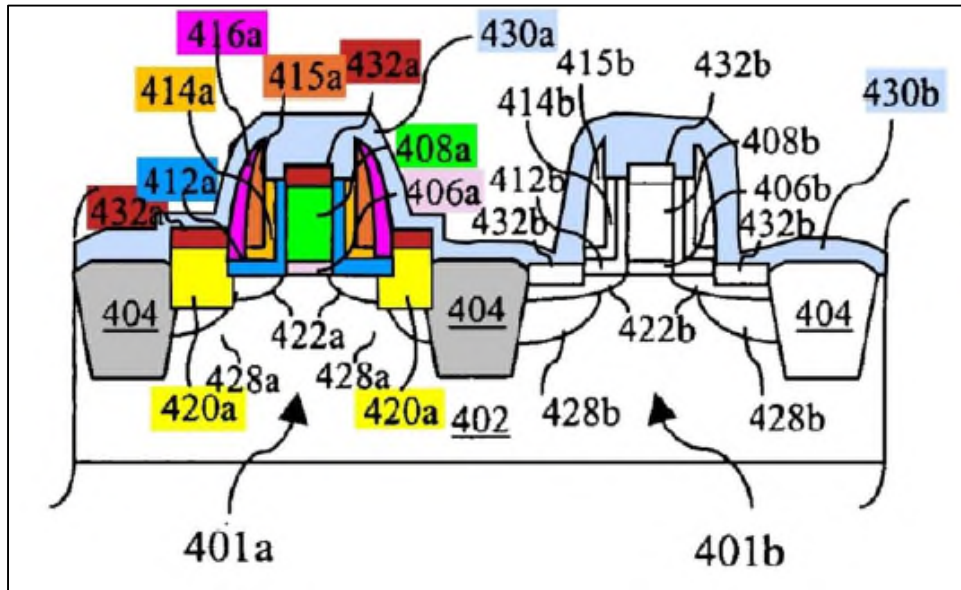


Figure I

C. Claim 3: “The semiconductor device of claim 1, further comprising: a first silicide layer formed on the first gate electrode; and a second silicide layer formed on the first source/drain region which includes the silicon compound layer”

Cheng817 discloses silicide contacts 432a (red) formed both on gate electrode 408a (green) and SiGe source/drain regions 420a (yellow). (Cheng817, Ex.1008 ¶[0069], Figs. 4i-4j.) The former is a “first silicide layer,” and the latter are “second silicide layer[s].” (Ex.1101, ¶272-274.)

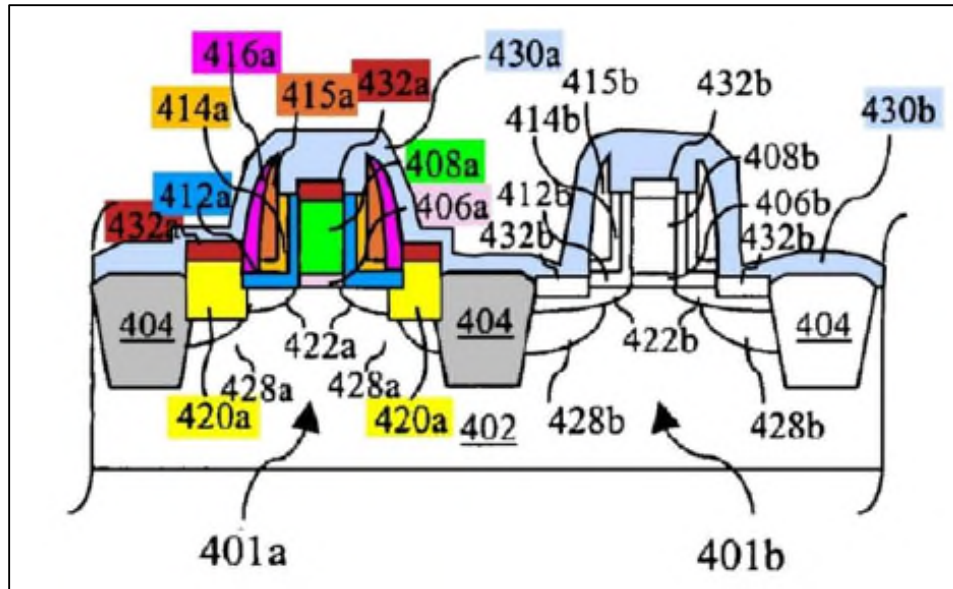


Figure I

D. Claim 4: “The semiconductor device of claim 1, wherein the first stress-relief film is formed on a side surface of the silicon compound layer”

Cheng817’s stress-relief film (dummy spacer 416a) is formed on a side surface of the silicon compound layer (SiGe source/drain regions 420a) (*see* Figure I). (Cheng817, Ex.1008, Fig. 4j; *Supra* §§VII.B.9-11; Ex.1101, ¶¶275-277.)

E. Claim 7:

1. Element 7[pre]: “The semiconductor device of claim 1”

For the same reasons described in Sections VII.B.1-11, the Cheng817 combinations disclose the semiconductor device of claim 1. (*Supra* §VII.B.2; Ex.1101, ¶278.)

2. Element 7[a]: “the first MIS transistor is a p-type MIS transistor”

Cheng817 discloses that “semiconductor device 401a may be a P-type MOS device,” i.e., a p-type MIS transistor. (Cheng817, Ex.1008 ¶[0056].) (*Supra* §VII.B.2; Ex.1101, ¶279.)

3. Element 7[b]: “the first stress is a compressive stress”

Cheng817 discloses SiGe source/drain regions 420a that cause a compressive stress “increasing the compressive stress in the substrate can improve the performance of p-channel metal-oxide-semiconductor (PMOS) devices.” (Cheng817, Ex.1008 ¶[0002]; Wang906, Ex.1009 ¶¶[0030]-[0032], FIG. 9.) (*Supra* §VII.B.6; Ex.1101, ¶280.)

4. Element 7[c]: “the second stress is a tensile stress”

Cheng817 discloses the etch stop layer 430a/430b which causes a tensile stress tensile stress “between about +0.001 and about +50 GPa” opposite the SiGe compressive stress. (Cheng817, Ex.1008 ¶[0070].) (*Supra* §VII.B.7; Ex.1101, ¶281.)

F. Claim 8:

1. Element 8[pre]: “The semiconductor device of claim 1”

For the same reasons described in Sections VII.B.1-11, the Cheng817 combinations disclose the semiconductor device of claim 1. (*Supra* §VII.B.1-11; Ex.1101, ¶282.)

2. Element 8[a]: “the silicon compound layer is a SiGe layer”

Cheng817 discloses the epitaxial source/drain layer 420a, which comprises “silicon germanium” or SiGe layer. (Cheng817, Ex.1008 ¶[0065].) (*Supra* §VII.A, §VII.B.6; Ex.1101, ¶283.)

3. Element 8[b]: “the stress insulating film is a silicon nitride film”

Cheng817 discloses that the etch stop layer 430a and 430b “may include silicon nitride (Si_xN_y).” (Cheng817, Ex.1008 ¶[0070].) (*Supra* §VII.B.7; Ex.1101, ¶284.)

4. Element 8[c]: “the first stress-relief film is a silicon oxide film”

Cheng817 discloses a dummy spacer where the “dummy spacer material 416,” which corresponds to the stress-relief film claimed, “may include silicon dioxide (SiO_2).” (Cheng817, Ex.1008 ¶[0063].) (*Supra* §VII.B.9; Ex.1101, ¶285.)

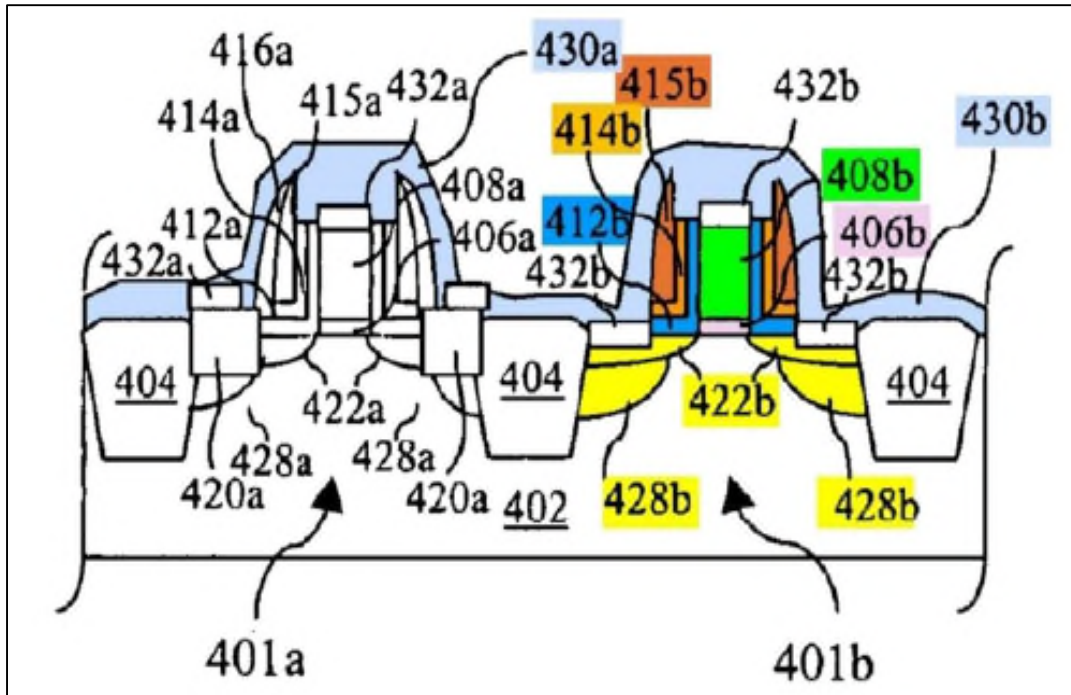
G. Claim 11:

1. Element 11[pre]: “The semiconductor device of claim 1”

For the same reasons described in Sections VII.B.1-11, the Cheng817 combinations disclose the semiconductor device of claim 1. (*Supra* §§VII.B.1-11; Ex.1101, ¶¶286-287.)

2. Element 11[a]: “a second MIS transistor”

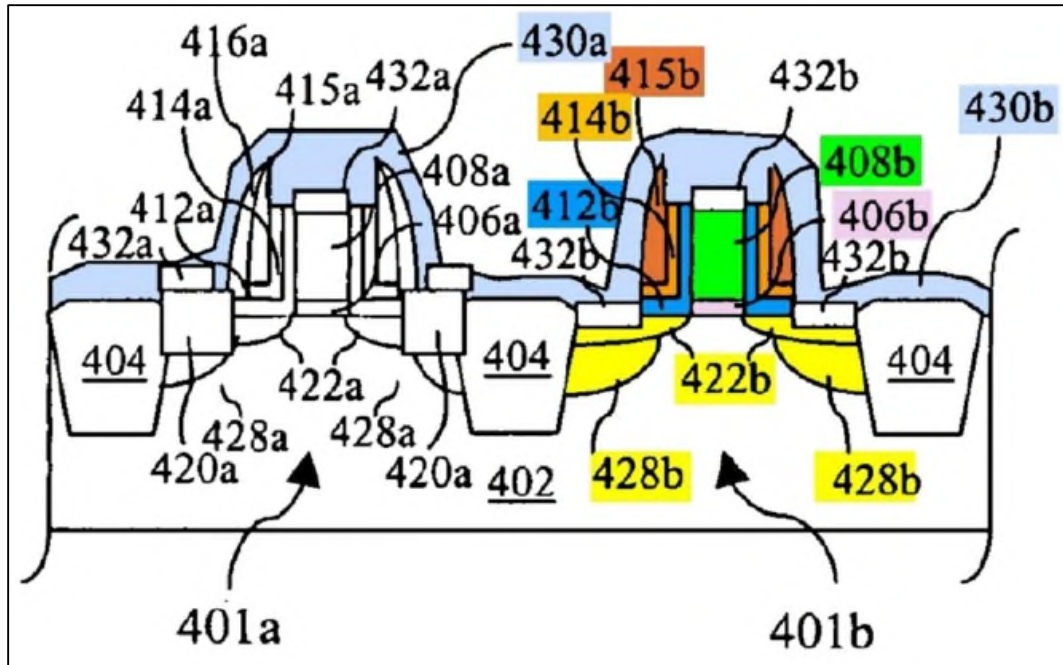
Cheng817 discloses a second MIS transistor, e.g., “N-type MOS device” 401b. (*Supra* §VII.B.2; Cheng817, Ex.1008 ¶[0056], Fig. 4j; Ex.1101, ¶¶286-288.)



Cheng817, Ex.1008, Fig. 4j

3. Element 11[b]: “a second gate insulating film formed on a second active region in the semiconductor substrate”

Cheng817’s NMOS 401b includes a second gate insulating film (gate dielectric 406b) formed over an NMOS active region comprising lightly doped regions 422b, heavily doped regions 428b, and the surrounding semiconductor regions. (Cheng817, Ex.1008 ¶[0056], ¶[0060], ¶[0066], Fig. 4j; Ex.1101, ¶¶289-291.)



Cheng817, Fig. 4j

4. **Element 11[c]: “a second gate electrode formed on the second gate insulating film”**

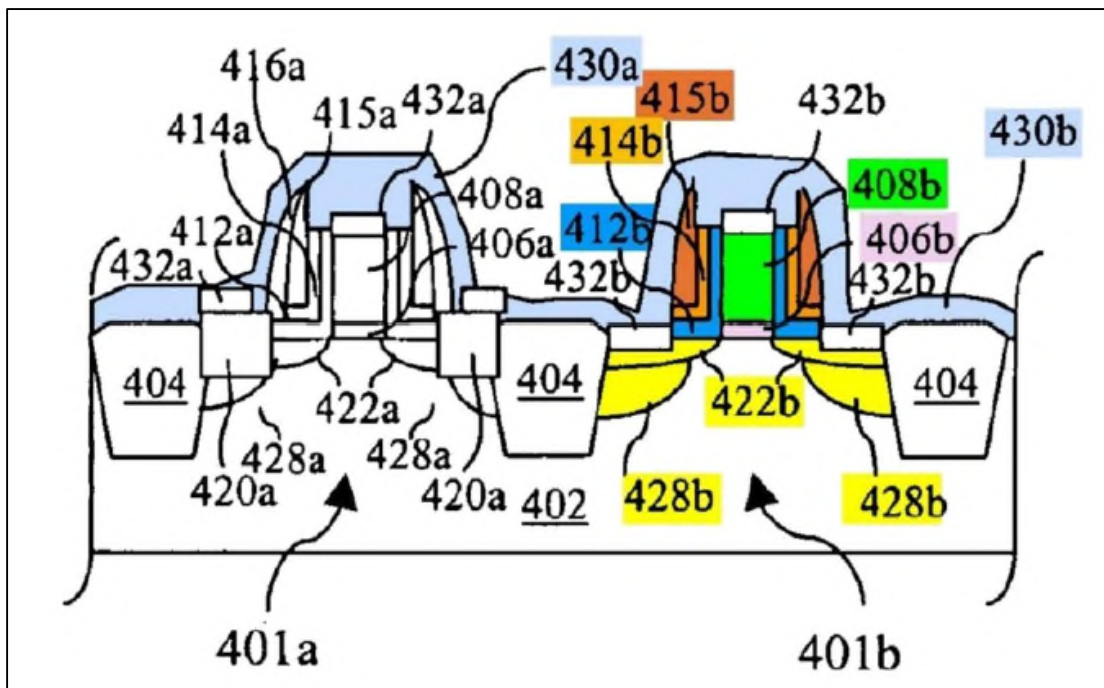
Cheng817’s NMOS 401b includes a second gate electrode (gate electrode 408b) formed over gate dielectric layer 406b. (Cheng817, Ex.1008 ¶[0056], Fig. 4j; Ex.1101, ¶[292].)

5. **Element 11[d]: “a second sidewall spacer formed on a side surface of the second gate electrode”**

Cheng817’s NMOS 401b includes a second sidewall spacer comprising sidewall structure 414b and spacer 415b. (Cheng817, Ex.1008 ¶[0061].) As Fig. 4j shows, sidewall structures 414b (light orange) and spacers 415b (dark orange) are formed on the side surface of gate electrode 408b (green). (*Id.*; Ex.1101, ¶¶[293-294].)

6. Element 11[e]: “a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer”

Cheng817’s NMOS 401b includes a second source/drain region of a second conductivity type (n-type) comprising lightly doped regions 422b and heavily doped regions 428b. (Cheng817, Ex.1008 ¶[0060], ¶[0066], Figs. 4e-4j.) As Fig. 4j shows, Cheng817’s n-type source/drain regions (yellow) are formed on a lateral side of the second sidewall spacers (414b and 415b, orange). (Cheng817, Ex.1008, Figs. 4d-4j; Ex.1101, ¶¶295-296.)



Cheng817, Ex.1008, Fig. 4j

7. Element 11[f]: “the stress insulating film formed on the second active region to cover the second gate electrode, the second sidewall spacer, and the second source/drain region”

Cheng817’s stress insulating film (etch stop layer 430a/430b) is “formed over the semiconductor device(s) 401a [PMOS] and 401b [NMOS],” as Fig. 4j shows, to cover the NMOS gate electrode 408b, sidewall spacers 414b and 415b, and NMOS source drain regions 422b and 428b. (Cheng817, Ex.1008 ¶[0070]; Ex.1101, ¶¶297-298.)

H. GROUND 2A: Cheng817 in Combination with Wang906 Renders Obvious Claims 1, 3, 4, 7, 8, and 11

A POSITA would have found claims 1, 3, 4, 7, 8, and 11 obvious based on the Cheng817-Wang906 combination for the reasons stated in Sections VII.A and VII.B.1-11 and the well-known advantages of raised SiGe. (*Supra* §IV.A.2; Ex.1101, ¶299.)

VIII. GROUND 3: Saito825 in Combination with Fukutome and James Renders Claims 1, 3, 4, 7, and 8 Obvious.

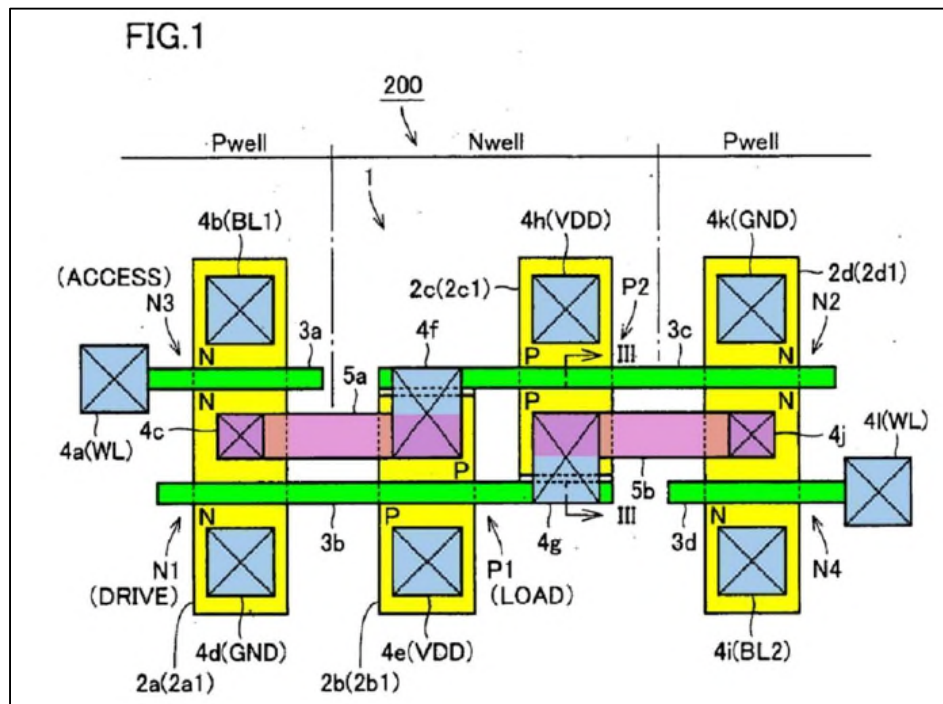
A. Overview

Saito825 discloses a textbook SRAM circuit (below) with levels 1-5 numbered in order from the bottom up:

- Substrate: 100 (uncolored). (Saito825, Ex.1010 ¶[0072].)
- Active regions: 2a-2d (yellow). (Saito825, Ex.1010 ¶¶[0060]-[0061].)
- Polysilicon wirings: 3a-3d (green). (Saito825, Ex.1010 ¶¶[0067]-[0068], ¶[0124].)

- Contact parts: 4a-4l (blue). (Saito825, Ex.1010 ¶¶[0068]-[0069].)
- Metal wirings: 5a-5b (purple). (Saito825, Ex.1010 ¶¶[0070]-[0071].)

(Ex.1101, Pb 300-302; *compare* Saito825, Ex.1010 Pb [0003]-[0005], Pb [0049]-[0050], FIGS. 1-2, *with* Pavlov-2008, Ex.1446, 19-20, Figs. 2.10(b)-(d); *see* Matsui832, Ex.1447, FIGS. 1-3; Ishida-1998, Ex.1448, Tbl. 1; Balobas-2015, Ex.1449, 1, Fig. 1; Thompson498, Ex.1450, Pb [0201], Pb [0204]-[0205], FIGS. 38-40B.)

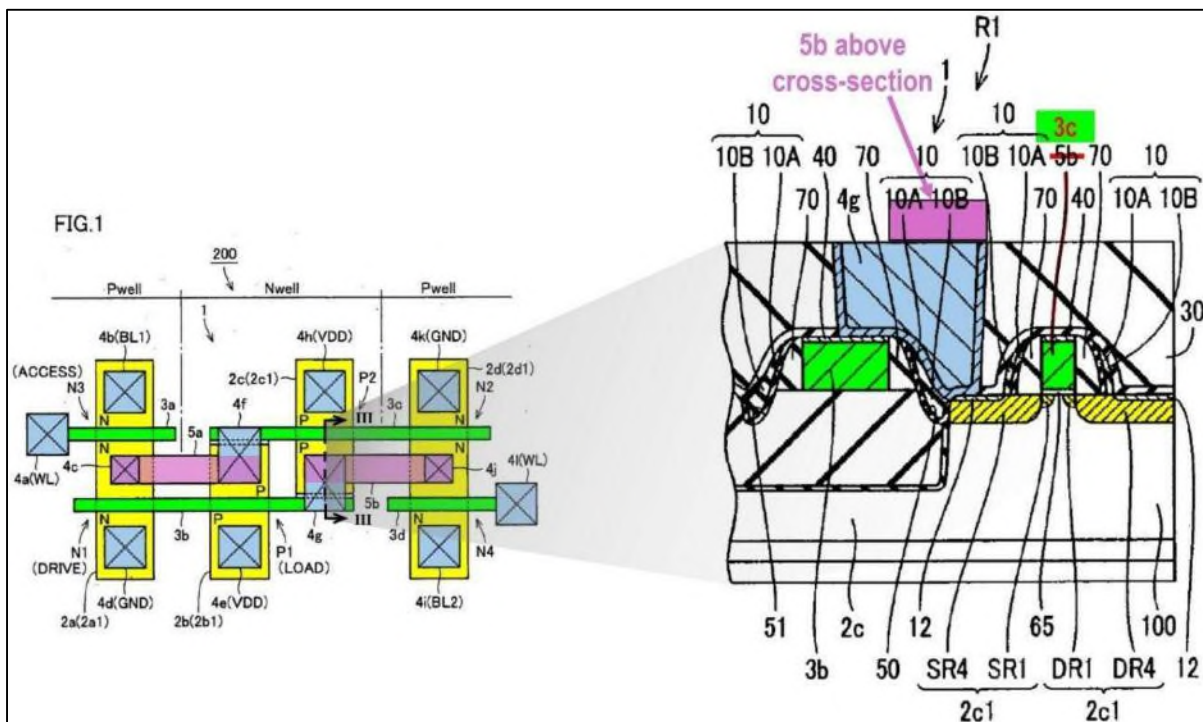


Saito825, Ex.1010, FIG. 1

Saito825 explains: “Polysilicon wirings 3a-3d [green] constitute a gate of each MOS transistor.” (Saito825, Ex.1010 ¶[0067].) Saito825’s “contact parts 4a-4l” (blue) connect the transistors with the “upper wiring” layer 5x (purple). (Saito825, Ex.1010 ¶[0068], ¶[0071].) For instance, “metal wiring 5b” connects contact part 4g

at “the drain of second load transistor P2” with “contact part 4j” at the “drain of second driver NMOS transistor N2.” (*Id.*) Because metal wiring 5b is an “upper wiring” that connects contact parts 4g and 4j, a POSITA would have understood it lies above the cross-sections in FIGS. 3-21. (Ex.1101, ¶¶303-304; Matsui832, Ex.1447, ¶¶[0038]-[0040], FIGS. 1-3.)

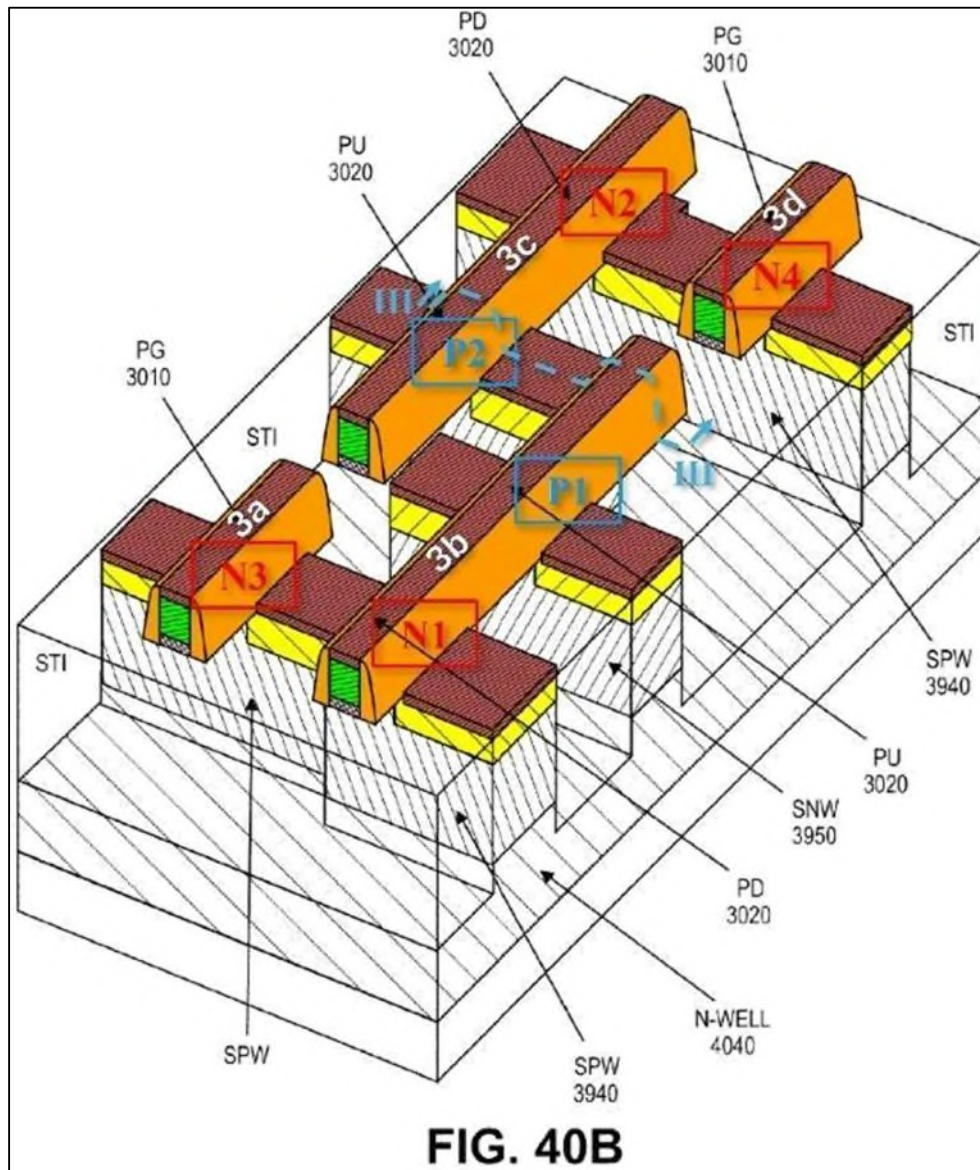
Like FIGS. 3-11, region R1 in Saito825’s FIGS. 12-21 shows cross-sections along cutline III-III in FIG. 1. (*Compare* Saito825, Ex.1010 ¶[0030], ¶[0072], FIGS. 3-11, *with* Saito825, FIGS. 12-21.) A POSITA would have recognized “5b” in FIGS. 12-21 identifies the polysilicon gate of PMOS transistor P2 and thus should be labeled “polysilicon wiring 3c.” (Ex.1101, ¶¶305-313.)



**Saito825, Ex.1010, FIG. 1
FIG. 12**

**Saito825, Ex.1010,
(excerpted, adding 5b)**

The annotated figure below shows a perspective view of an SRAM like Saito825's, up to level 3 (polysilicon, green). (Ex.1101, ¶307.)



Saito825, Ex.1010, FIG. 40B

A POSITA would have recognized that, because Saito825's contacts 4g/4j and metal wiring 5b are textbook SRAM structures, metal wirings (5x) would have been located higher than the polysilicon lines (3x) and contacts (4x), as Figure L shows

below (amending and annotating Ex.1050, FIG. 40B). (Ex.1101, ¶308; Pavlov-2008, Ex.1446, 19-20, Figs. 2.10(b)-(d); Matsui832, Ex.1447, FIGS. 1-3; Ex.1049, Figs. 1-2.)

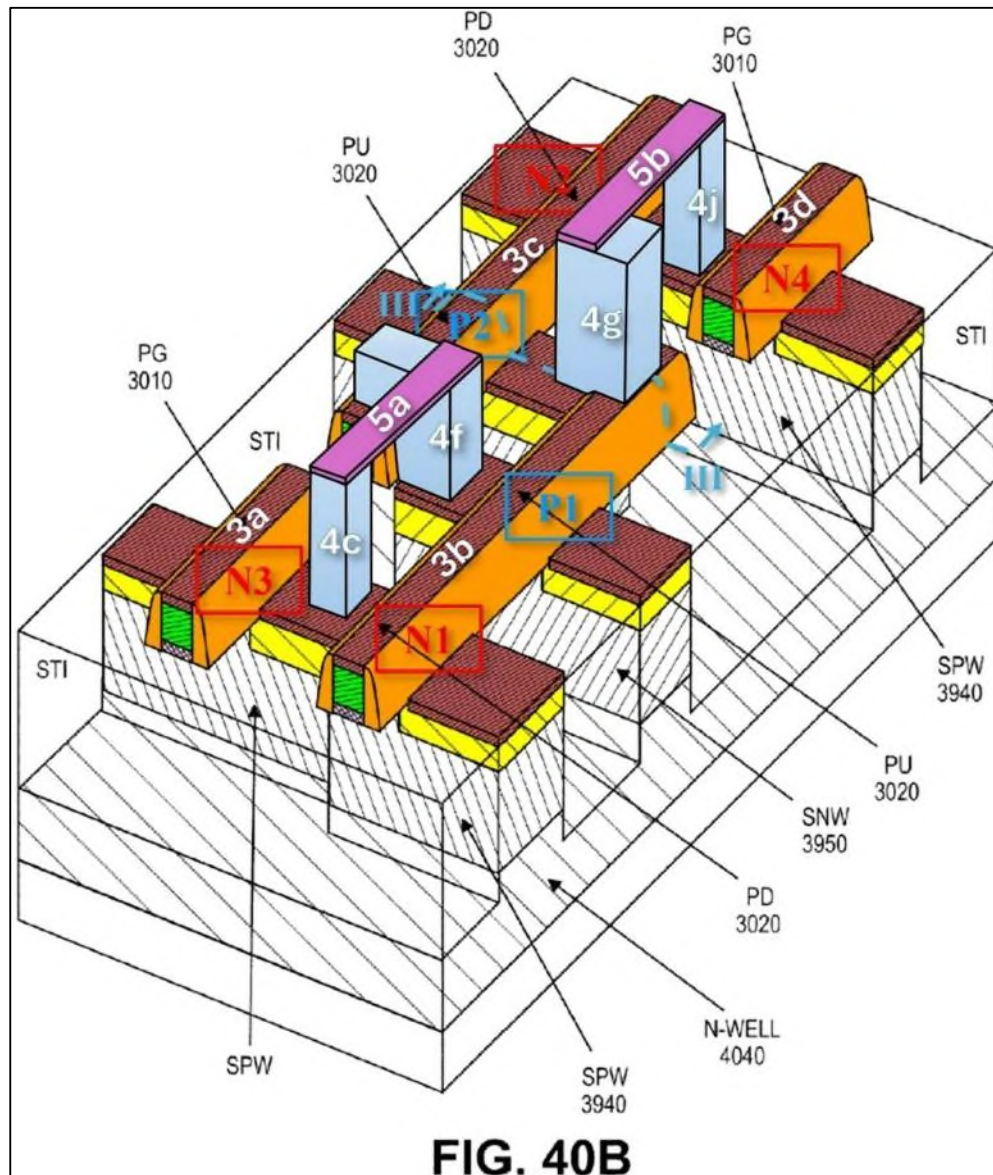


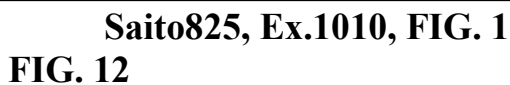
Figure L

A POSITA would have immediately recognized that “polysilicon wiring 5b” refers to “polysilicon wiring 3c” in FIGS. 12-21. (Ex.1101, ¶309; *see LG Elecs. Inc.*

v. ImmerVision, Inc., 39 F.4th 1364, 1372 (Fed. Cir. 2022) (explaining such clerical errors should be disregarded).)

Saito825 describes each of these textbook SRAM layers with a shared numeric level identifier (2x, 3x, 4x, 5x), such that a POSITA would have recognized “polysilicon wiring 5b” in Saito825’s FIGS. 12-21 correctly points to a polysilicon wiring. But it is polysilicon wiring “3c” because no polysilicon wiring “5b” exists. (Ex.1101, ¶310; *see* Pavlov-2008, Ex.1446, 19-20, Figs. 2.10(b)-(d); Saito825, Ex.1010 ¶¶[0065]-[0068], ¶[0124], FIGS. 1-2.) A POSITA would have immediately noted that “polysilicon wirings” are designated 3x, such that FIGS. 12-21 show polysilicon wiring “3c” from FIG. 1, not “metal wiring 5b.” (Saito825, Ex.1010 ¶¶[0066]-[0068], ¶[0071]; Ex.1101, ¶310.) A POSITA would have understood, as Saito825 explains, that “metal wiring 5b” is an “upper wiring” at contacts 4g/4j and is located above Saito825’s cross-sections. (Ex.1101, ¶310; Saito825, Ex.1010 ¶¶[0067]-[0071]; Pavlov-2008, Ex.1446, 19-20, Figs. 2.10(b)-(d); Matsui832, Ex.1447, FIGS. 1-3.)

Moreover, cross-section III-III in FIG. 1 shows contact part 4g intersecting polysilicon wiring 3b and metal wiring 5b, not polysilicon wiring 3c. Saito825 FIG. 1. “[P]olysilicon wiring 3c,” on the other hand, lies beside contact part 4g and serves as the polysilicon gate for PMOS transistor P2. (Ex.1101, ¶311.) Saito825’s references to “polysilicon wiring 5b” thus describe what is shown in FIG. 1 as



Saito825, Ex.1010,
 erpted, adding 5b)

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Correcting this obvious typographical error, region R1 in FIGS. 12-21 reflects the correct cross-section corresponding to cutline III-III in FIG. 1, as expected for this conventional SRAM. (Ex.1101, ¶¶314-318 (discussing Matsui832, Ex.1447); Matsui832, Ex.1447, ¶¶[0062]-[0063], ¶¶[0065]-[0066], FIGS. 1-3; Pavlov-2008, Ex.1446, 19-20, Figs. 2.10(b)-(d); Ex.1049, Figs. 1-2.)

A POSITA would have readily understood this because Saito825 does not purport to alter the wiring or structure of the textbook SRAM. (Pavlov-2008, Ex.1446, 19-20, Figs. 2.10(b)-(d); Ex.1101, ¶319.) Saito825 instead addresses problems associated with recesses 50 that form in isolation regions. (Saito825, Ex.1010, Abstract, ¶[0011], ¶¶[0022][0023], ¶[0027], ¶¶[0074]-[0075].)

At bottom, no matter how one views Saito825, a POSITA would have recognized polysilicon wiring 3c in FIG. 1 has the structure incorrectly labeled “5b” in FIGS. 12-21, because the various layers use their own respective numeric designators. (Ex.1101, ¶320.) Thus, (1) a POSITA would have immediately recognized Saito825’s clerical error that “polysilicon wiring 5b” refers to “polysilicon wiring 3c,” and, regardless, (2) the structure labeled “polysilicon wiring 5b” in FIGS. 12-21 is a MIS transistor as discussed below. (Ex.1101, ¶320.)

1. A POSITA Would Have Found the Saito825-Fukutome-James Combination Obvious

A POSITA would have understood Saito825’s “plasma nitride (SiN)” insulating film 13 is a CESL. (Saito825, Ex.1010 ¶[0072], ¶¶[0080]-[0084], FIGS.

3, 12, 21; Ex.1101, ¶322.) A POSITA would have found it obvious to make CESL 13 tensile as a known way to improve NMOS performance, consistent with James. (*Supra* §IV.A.2, §VI.A; Jung, Ex.1529 ¶[0090], ¶¶[0099]-[0100], Tbl. V; James, Ex.1012, 2; Ex.1101, ¶325.)

A POSITA also would have found it obvious to substitute Fukutome's raised epitaxial SiGe PMOS source/drain layers for Saito825's non-epitaxial PMOS source/drain layers in active regions 2b/2c to improve the P1/P2 devices through compressive strain, yielding the structure in Figure M.¹⁶ (*Supra* §IV.A.2; Fukutome, Ex.1011 ¶[0110]; Ex.1101, ¶¶322-326.)

¹⁶ Figure M corrects the 5b/3c typographical error. (*Supra* §VIII.A.)

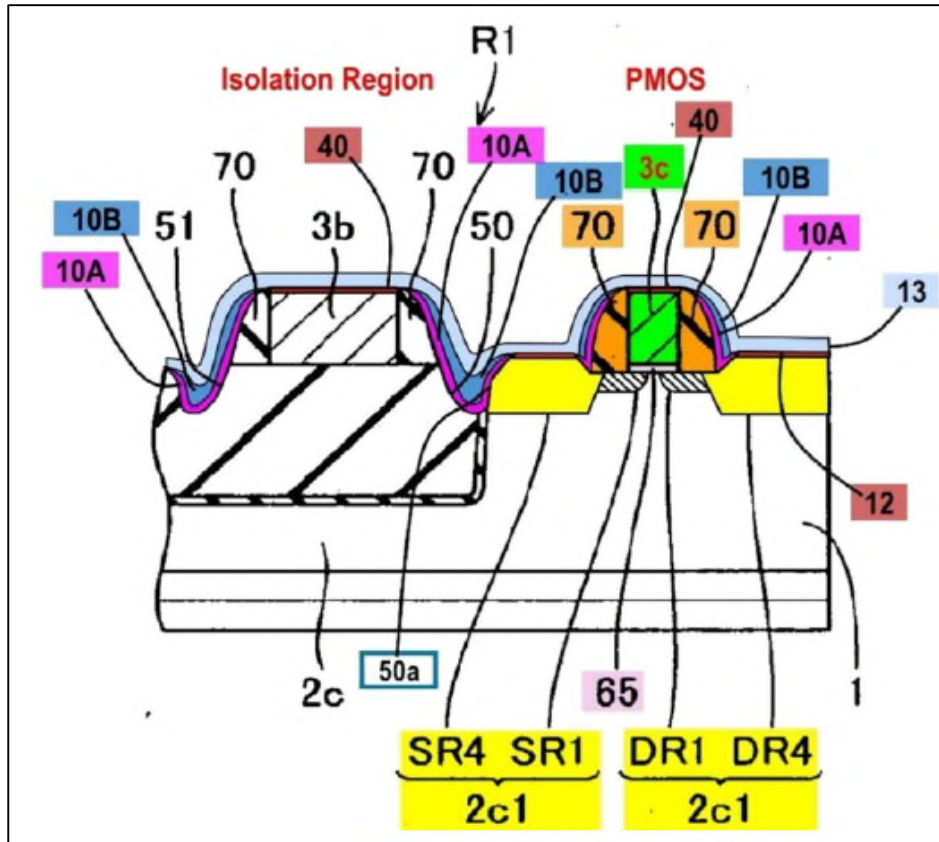


Figure M (similar to FIG. 21; Ex.1101, ¶323)

a. A POSITA would have been motivated to make the Saito825-Fukutome-James combination

(1) Raised SiGe source/drain regions

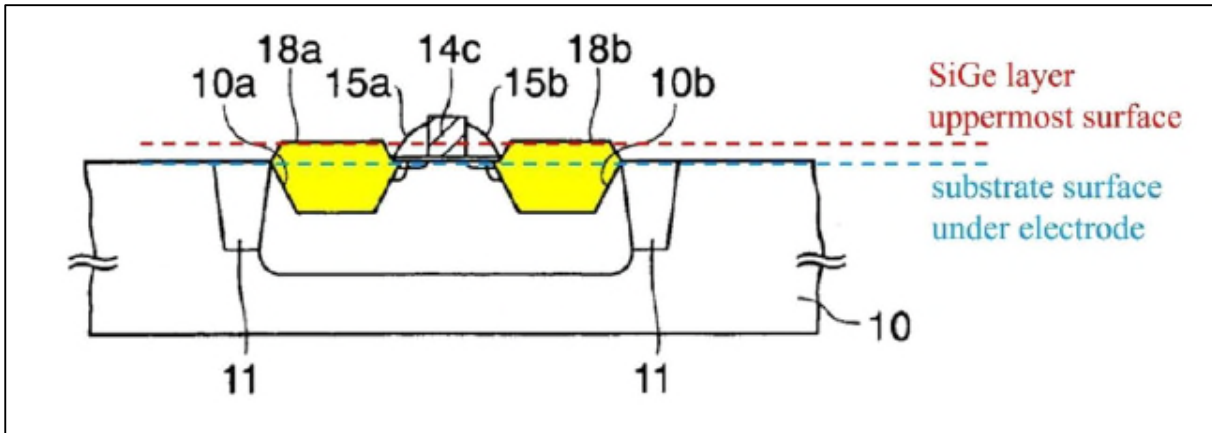
A POSITA would have found it obvious to incorporate Fukutome's raised SiGe source/drains into Saito825's PMOS devices to improve performance. (Ex.1101, ¶327; *Supra* §IV.A.2.)

Saito825 discloses source/drain regions 2c1. (Saito825, Ex.1010 ¶[0094], ¶[0097], ¶[0101], FIGS. 12, 17, 21.) Saito825's FIGS. 16-17 show shallow source/drain diffusion (extension) regions SR1/DR1 being formed before sidewalls 70 using polysilicon wiring 5b [sic:3c] as a mask. (Saito825, Ex.1010 ¶[0094], FIG.

16.) Deep source/drain diffusion regions SR4/DR4 are then formed using sidewalls 70 as a mask. (Saito825, Ex.1010 ¶¶[0097], ¶[0101], ¶[0124], FIG. 17; *Supra* §VII.A.; Ex.1101, ¶¶328-329.)

Fukutome's FIGS. 5B-5E disclose a substantially similar process to form source/drain diffusion regions 16a/16b using "gate electrode 14c as a mask," then to form source/drain diffusion regions 17a/17b using "gate electrode 14c and the first sidewalls 15a and 15b as a mask." (Fukutome, Ex.1011 ¶¶[0082]-[0083], ¶[0087], FIGS. 5B-5C; Ex.1101, ¶¶330-331.)

Fukutome discloses an improvement to this process: adding raised epitaxial SiGe source/drain regions 18a/18b. (Fukutome, Ex.1011 ¶¶[0097]-[0102], ¶[0100], ¶[0110], FIGS. 5C-5E; *Supra* §IV.A.2.) Fukutome's FIGS. 5D-5E show etching recesses 10a/10b to expose the (111) Si planes of substrate 10 and growing SiGe epitaxial layers 18a/18b extending above the substrate next to sidewalls 15a/15b. (Fukutome, Ex.1011 ¶[0092], ¶¶[0097]-[0102], FIGS. 5D-5E.) Fukutome's epitaxial SiGe layers introduce compressive stress to the PMOS channel regions. (Fukutome, Ex.1011 ¶[0005], ¶[0110], ¶[0249], FIG. 5G (arrows); *Supra* §IV.A.2.)



Fukutome, Ex.1011, FIG. 5E

For reasons in Section IV.A.2, a POSITA would have found it obvious to incorporate Fukutome's epitaxial SiGe into Saito825's PMOS devices (active regions 2b/2c) to improve "the mobility of carriers in the channel" and "the drive capability of the MOS transistor." (Fukutome, Ex.1011 ¶[0110]; *see* Ex.1101, ¶¶332-336.) Additionally, a POSITA would have found it obvious to incorporate Fukutome's SiGe layers into Saito825's PMOS devices to suppress junction leakage and improve reliability. (Fukutome, Ex.1011 ¶[0100]; Ex.1101, ¶333, ¶336.) Such benefits were well-known. (Ex.1101, ¶337.) The four most recent generations of high-volume commercial devices all used raised SiGe source/drain regions. (*Supra* §IV.A.2; James, Ex.1012, 2.)

Figure M illustrates a structure ¹⁷ incorporating Fukutome's raised SiGe source/drain regions into Saito825's active regions 2b/2c.

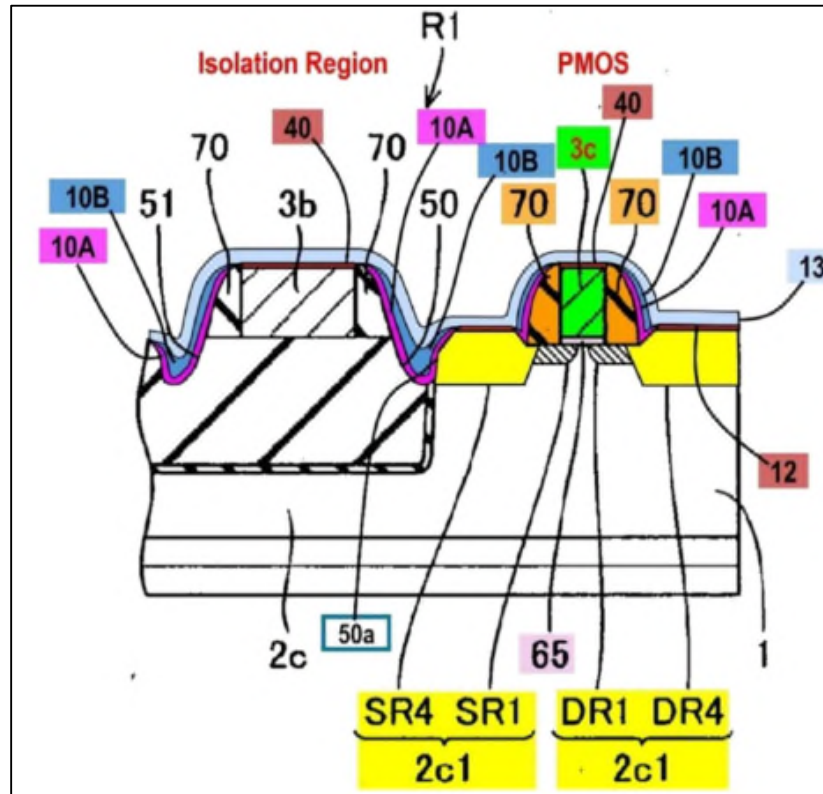


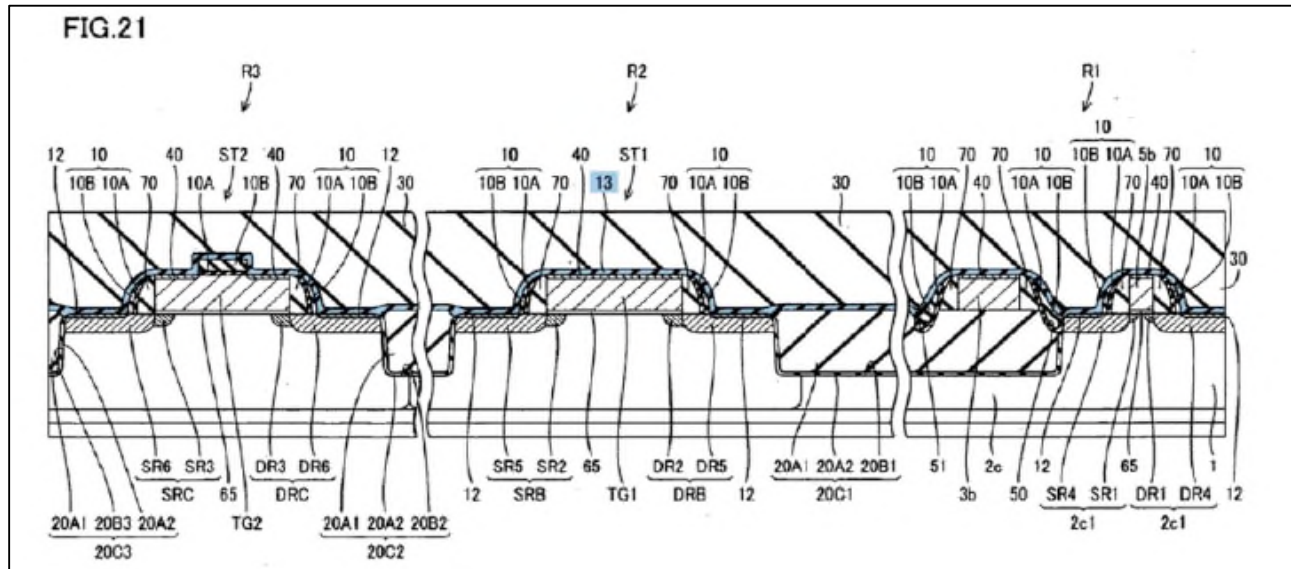
Figure M

(2) Tensile silicon nitride layer 13

Saito825's SiN layer 13 blankets the entire SRAM circuit. (Saito825, Ex.1010 ¶[0091] (explaining FIG. 15 shows "well region[s] of various conductivity types"), FIGS. 12, 21 (showing same).) A POSITA would have been motivated to make Saito825's SiN layer 13 tensile to improve electron mobility in NMOS channel

¹⁷ After forming Fukutome's SiGe source/drain layers, the process flow in the proposed combination would continue as in Saito825. (Ex.1101, ¶339.)

regions (e.g., active regions 2a/2d). (*Supra* §IV.A.2; Saito825, Ex.1010 ¶¶[0063]-[0065], FIG. 1; Ex.1101, ¶¶340-342.)



Saito825, Ex.1010, FIG. 21

Although Saito825 is silent regarding strain in SiN layer 13, James demonstrates that a POSITA would have found a tensile SiN layer 13 obvious. (Ex.1101, ¶¶343-348.) James explains “a highly stressed nitride sealant layer” (CESL) can “increase[] electron mobility” and “involves no extra cost for either capital equipment or special substrates,” which a POSITA would have found attractive. (James, Ex.1012, 2, 5.) It was well-known that a silicon nitride CESL prepared under certain conditions can “apply[] stress to [a] channel region” to improve carrier mobility. (Hsu823, Ex.1506 ¶[0003]; *see* Jung, Ex.1529 ¶[0090], ¶¶[0099]-[0100], Tbl. V; Ke, Ex.1531, ¶[0003]; James, Ex.1012, 2; Morin-2007, Ex.1528, 1-2; Ex.1101, ¶348.)

A POSITA would have been motivated make Saito825's SiN layer 13 tensile as a simple and inexpensive way to improve electron mobility in transistors N1-N4. (Ex.1101, ¶¶349, ¶351.) A POSITA further would have understood such tensile stress in PMOS devices P1/P2 would have been mitigated by the presence of a buffer layer and outweighed by compressive SiGe stress. (*Supra* §VIII.A.1.a, §IV.A.3; Morin-2007, Ex.1528, 1-2; James, Ex.1012, 2; Hsu823, Ex.1506, ¶¶0039; Alvarez, Ex.1006 ¶¶0047, ¶¶0049, ¶¶0054, ¶¶0065, Tbl. 1, FIG. 9; Ex.1101, ¶350.)

b. A POSITA would have reasonably expected to succeed in the Saito825-Fukutome-James combination

A POSITA would have reasonably expected to succeed in adding raised, compressive SiGe PMOS source/drain regions to Saito825's PMOS transistors (as Fukutome teaches) and in using a tensile silicon nitride CESL 13 (as James teaches). (Ex.1101, ¶¶348-358.)

Incorporating Fukutome's SiGe source/drains would have required nothing more than the conventional steps of trenching Saito825's silicon substrate and epitaxially growing SiGe regions after forming shallow source/drain extensions (SR1/DR1). (*Compare* Saito825, Ex.1010 ¶¶0092-[0103], FIGS. 16-17, *with* Fukutome, Ex.1011 ¶¶0085-[0102], FIGS. 5C-5E; Ex.1101, ¶353.) Then, Saito825's fabrication process would have continued as Saito825 describes by forming layers 10A/10B and making SiN layer 13 tensile as in James. (Saito825, Ex.1010 ¶¶0104-[0106], FIG. 18; James, Ex.1012, 2.) Adding Fukutome's SiGe

source/drain layers to Saito825's PMOS active regions 2b/2c would have achieved the ordinary, expected result of compressively stressing PMOS channels to boost performance. (*Supra* §IV.A.2, §VIII.A.1.a; Ex.1101, ¶353.)

Similarly, a POSITA would have reasonably expected to succeed in making Saito825's SiN insulating layer 13 tensile, which had also been in commercial use for years, by using conventional deposition steps. (*Supra* §IV.A.2; Jung, Ex.1529, ¶¶[0099][0100], Tbl. V; Saito825, Ex.1010 ¶[0080], ¶¶[0120]-[0121], FIGS. 12, 18; James, Ex.1012, 2, 5; Alvarez, Ex.1006 ¶[0054], ¶[0065], ¶[0069], Tbl. 1; Hsu823, Ex.1506, ¶[0003], ¶¶[0037]-[0039]; Morin-2007, Ex.1528, 1-2; Ex.1101, ¶354.) Depositing a tensile SiN layer 13 would have achieved the ordinary, expected result of applying tensile stress to boost electron mobility in Saito825's NMOS regions 2a/2d. (Ex.1101, ¶355.) James confirms expected success, showing a commercial device years before the '425 patent with both raised, faceted epitaxial SiGe source/drain regions and a tensile CESL. (James, Ex.1012, 2-3, Fig. 6; Ex.1101, ¶¶356-357.)

A POSITA would have found the proposed combination obvious because it (a) combines known prior-art elements (epitaxial SiGe source/drain regions and tensile SiN CESL) according to known methods (known SiGe epitaxy and SiN deposition techniques) to yield predictable results (strained-channel transistors with improved performance); (b) substitutes one known element for another (SiGe PMOS

source/drains regions for Saito825's non-epitaxial PMOS source/drain regions and a tensile CESL for Saito825's SiN CESL 13) to obtain predictable results (strained-channel transistors with improved performance); (c) using known epitaxial growth and deposition techniques to improve similar MOSFET devices in the same way; (d) applying known epitaxial growth and deposition techniques to improve Saito825's MOSFET device and yield predictable results; and (e) applying a known teaching, motivation, or suggestion in the art (as explained above) to arrive at the claimed invention. (*KSR*, 550 U.S. at 416-21; Ex.1101, ¶358.)

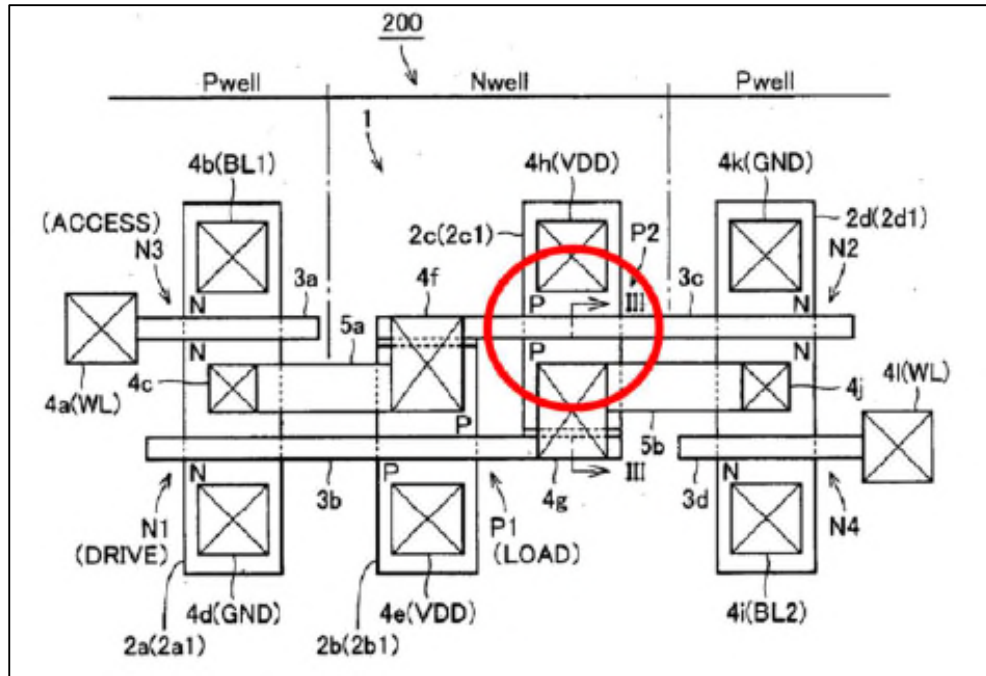
B. Independent Claim 1

1. Element 1[pre]: “A semiconductor device comprising: a first MIS transistor, ... includ[ing]:”

Saito825 discloses “a semiconductor device.” (Saito825, Ex.1010 ¶[0002]; *see id.*, ¶¶[0023]-[0026], ¶[0051], ¶[0066], FIGS. 1, 12, 21; *Supra* §VIII.A.1; Ex.1101, ¶359.)

2. Element 1[a]: “a first MIS transistor, ... includ[ing]:”

Saito825 discloses a first MIS transistor, e.g., PMOS transistor P2 in active region 2c. (Saito825, Ex.1010 ¶[0057], FIGS. 1, 3, 12, 21; *Supra* §VIII.A.1; Ex.1101, ¶¶360-363.) Saito825's “PMOS transistor P2 is formed in the intersection part of impurity diffusion region 2c1 comprising the region used as a source/drain, and polysilicon wiring 3c” (*see* Figure M). (Saito825, Ex.1010 ¶[0066]; Ex.1101, ¶361; *Supra* §VIII.A.)



3. Element 1[b]: “a first gate insulating film formed on a first active region in a semiconductor substrate”

Saito825 discloses a gate insulating film 65 formed on active region 2c of substrate 100 (*see* Figure M). (Saito825, Ex.1010 ¶[0051], FIGS. 12, 21; *Supra* §VIII.A.1; Ex.1101, ¶364.)

4. Element 1[c]: “a first gate electrode formed on the first gate insulating film”

Saito825 discloses polysilicon wiring 5b [sic:3c] “formed on the upper surface of this gate insulating film 65” (*see* Figure M). (Saito825, Ex.1010 ¶[0051], ¶[0066], ¶[0124], FIGS. 12, 21; *Supra* §VIII.A.1; Ex.1101, ¶¶365-366.)

5. Element 1[d]: “a first sidewall spacer formed on a side surface of the first gate electrode”

Saito825 discloses that “sidewall 70 is formed on the [sic] both side surfaces of... polysilicon wiring 5b [sic:3c], and polysilicon wiring 3b” (*see* Figure M). (Saito825, Ex.1010 ¶[0077], ¶[0096], ¶[0124], FIG. 17; *Supra* §VIII.A.1; Ex.1101, ¶¶367-368.)

6. Element 1[e]: “a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region”

In the combination, “SiGe layers to be used as source/drain electrodes are epitaxially grown in the recesses, thus introducing strain into a channel.” (Fukutome, Ex.1011 ¶[0005]; *see id.*, ¶[0110]; *Supra* §VIII.A.1; Ex.1101, ¶¶369-372.) The

“lattice spacing of SiGe” results in compressive stress “applied to a channel under the gate electrode.” (Fukutome, Ex.1011 ¶[0110]; *see id.*, ¶[0249], FIG. 5G; *Supra* §IV.A.2, §V.C.1.a(1)(a)). SiGe source/drain regions (yellow) would be grown in trenches etched in Saito825’s active region 2c on lateral sides of sidewalls 70 (orange) to cause compressive stress along the gate length direction of the channel regions (under gate insulating film 65) (*see* Figure M). (*Supra* §VIII.A.1.a; Ex.1101, ¶372.)

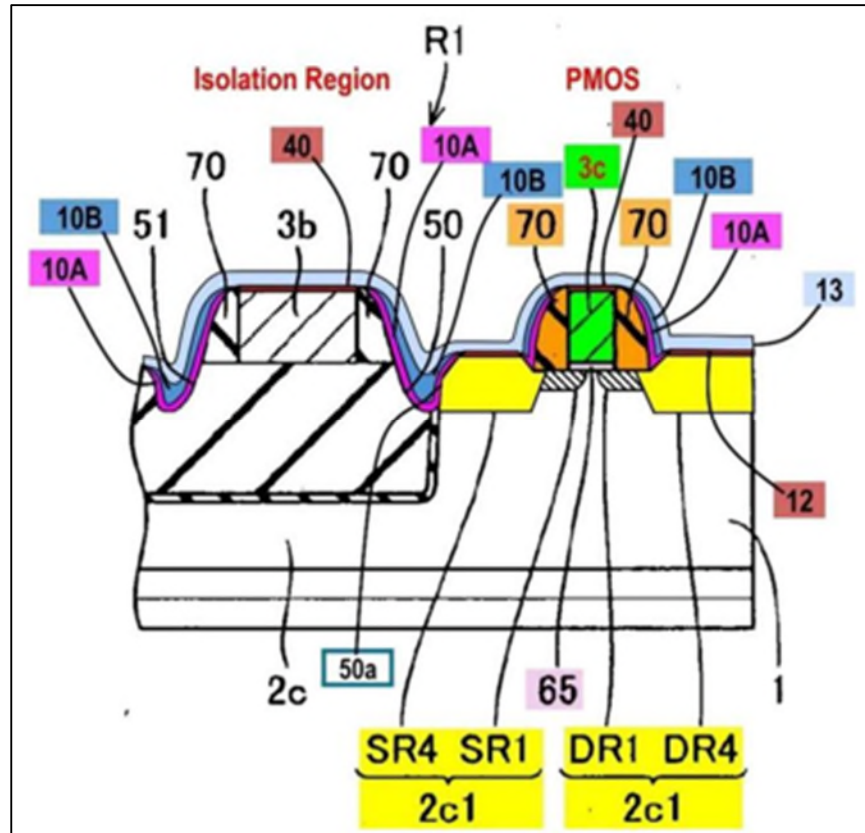


Figure M

7. **Element 1[f]: “a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress”**

Saito825’s layers 10A/10B are deposited and etched to expose wiring 5b [sic:3c] for silicidation. Then, “insulating film 13 ... is formed on silicide films 12 and 40 and consists of a plasma nitride (SiN).” (Saito825, Ex.1010 ¶[0080], ¶[0120], FIGS. 3, 9-12, 21; *see* Fukutome, Ex.1011 ¶[0106], FIG. 5G; James, Ex.1012, 2-3, Fig. 6.)

A POSITA would have found a tensile SiN insulating film 13 obvious, as James discloses, because “[l]ocalized tensile stress is applied to the channels of NMOS devices,” which can “increase[] electron mobility” and “enhance NMOS performance” without “extra cost for either capital equipment or special substrates.” (James, Ex.1012, 2, 5, Fig. 6; *Supra* §IV.A.2, §VIII.A.1b) A tensile insulating film 13 would form over “[c]rystalline facets” of the “raised [SiGe] source/drains” (*see* Figure M). (James, Ex.1012, 2; *see id.*, Fig. 6; Ex.1101, ¶¶373-375.)

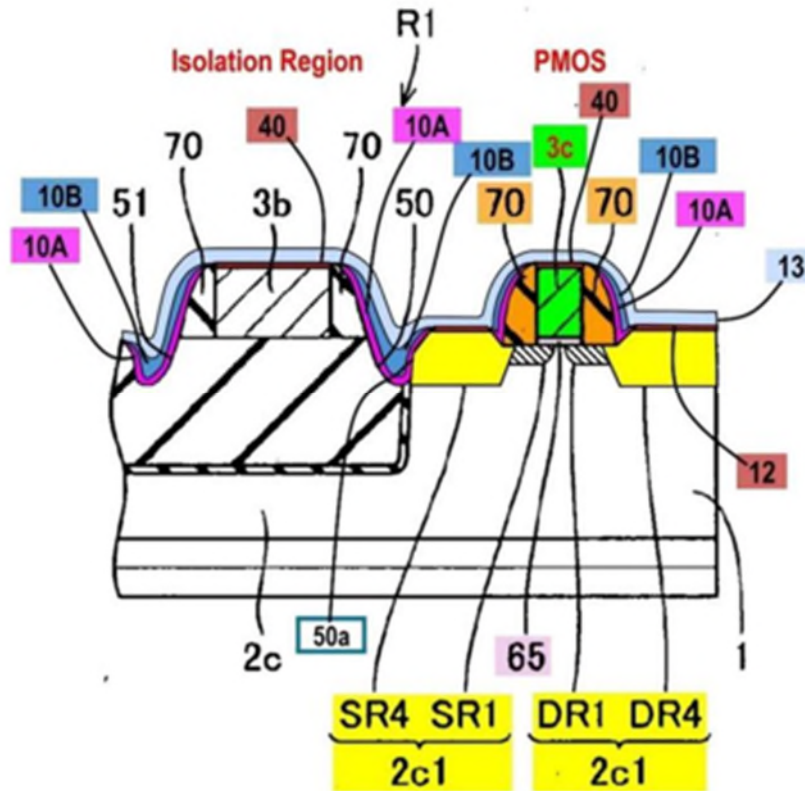


Figure M

8. Element 1[g]: “an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode”

Fukutome’s FIGS. 5D-5E teach epitaxial SiGe layers extending above the substrate. (Ex.1101, ¶¶376-378; *Supra* §VIII.A.1.a, §VIII.B.6) Fukutome teaches to “form[] the upper surfaces of the source/drain material layers 18a and 18b at positions higher than the surface of the silicon substrate 10.”¹⁸ (Fukutome, Ex.1011 ¶[0100], FIG. 5E; *Supra* §VIII.A.1.a.)

¹⁸ Figure M shows the SiGe remains higher than the substrate. (*Infra* §VIII.C.)

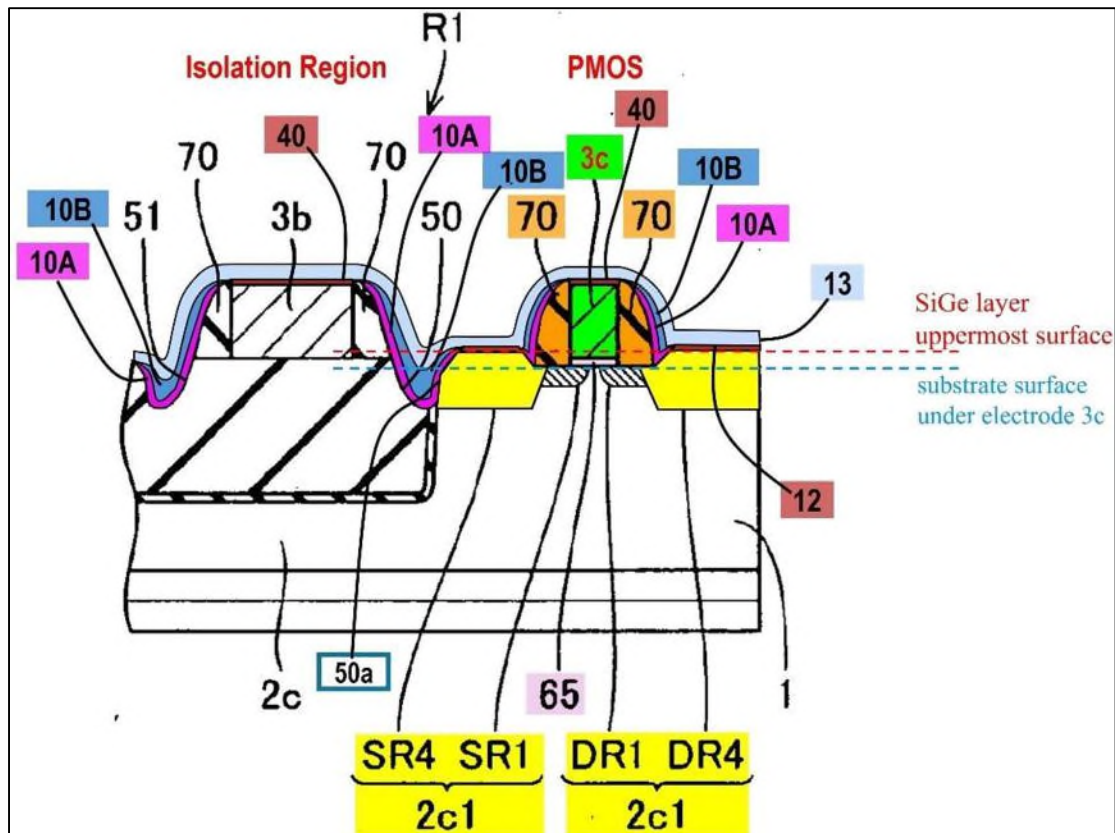
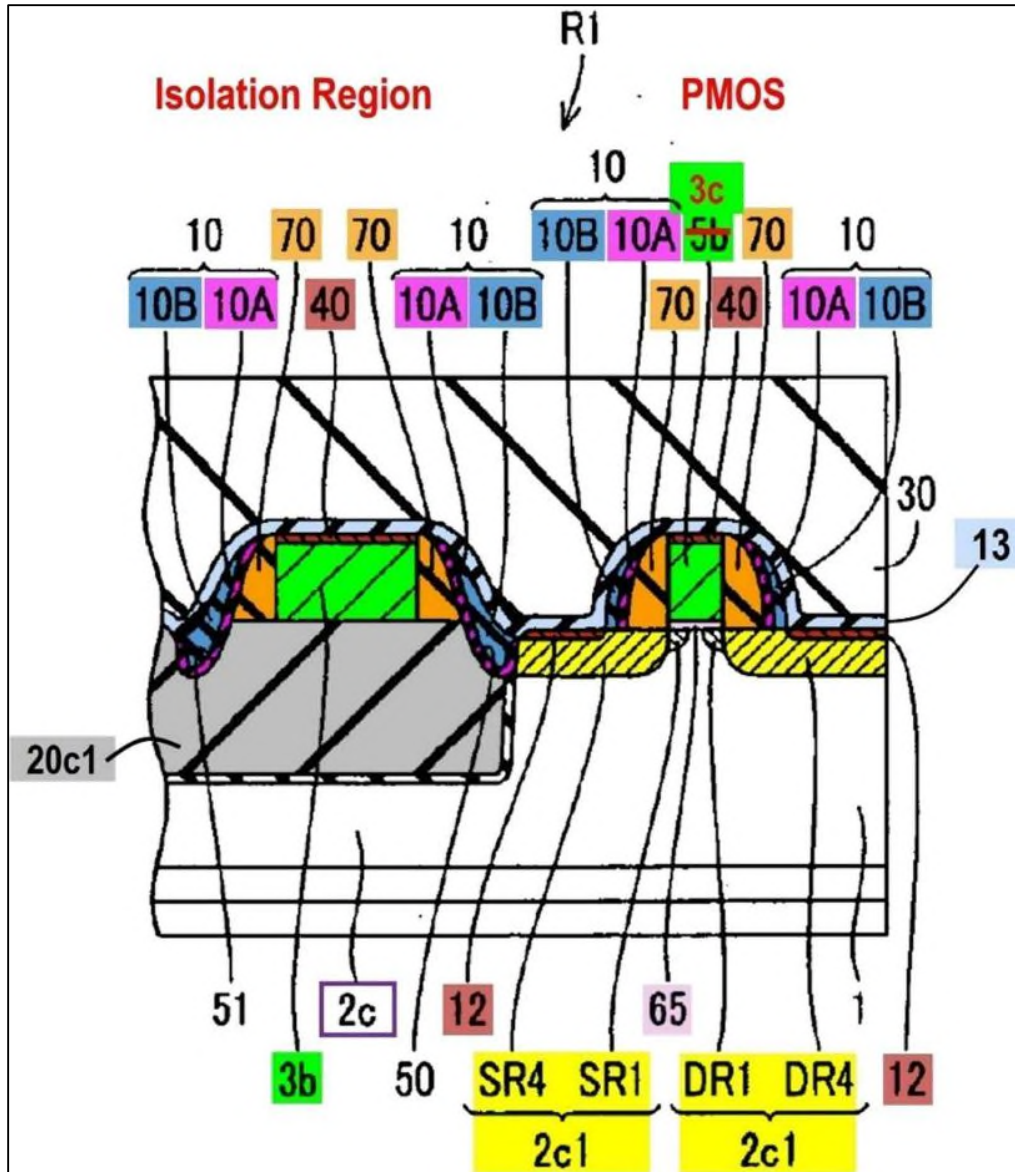


Figure M (annotated)

- 9. Element 1[h]: “a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer”**

Saito825's insulating film 10A (silicon oxide) forms in recess 50 of the isolation and remains on the edges of sidewalls 70 (*see* FIG. 21). (Saito825, Ex.1010 ¶¶[0074], ¶¶[0076], ¶¶[0078], ¶¶[0082], ¶¶[0104], ¶¶[0107], ¶¶[0113], FIGS. 6-12, 18-21; Ex.1101, ¶379.)



Saito825, Ex.1010, FIG. 21 (excerpted)

Because silicon oxide film 10A remains in recess 50 and on sidewalls 70, a POSITA would have recognized that silicon oxide film 10A in the proposed combination would form in the space between SiGe facets and sidewalls 70 and remain there, as in recesses 50 and in the prior art (*see* Figure M). (*Supra* §IV.A.3; Miyashita, Ex.1435, ¶¶[0052]-[0053], FIGS. 1U-1W; Murthy556, Ex.1430, 2:15-24, 9:10-44, FIGS. 2, 7-9; Fukutome, FIG. 5G; Ex.1101, ¶¶380-382.) A POSITA would

have recognized, and found obvious, that silicon oxide film 10A acts as a stress-relief film to buffer tensile strain from SiN layer 13 in PMOS active regions 2b/2c.

(*Supra* §IV.A.3, §VIII.A.1; Ex.1101, ¶¶383-384.)

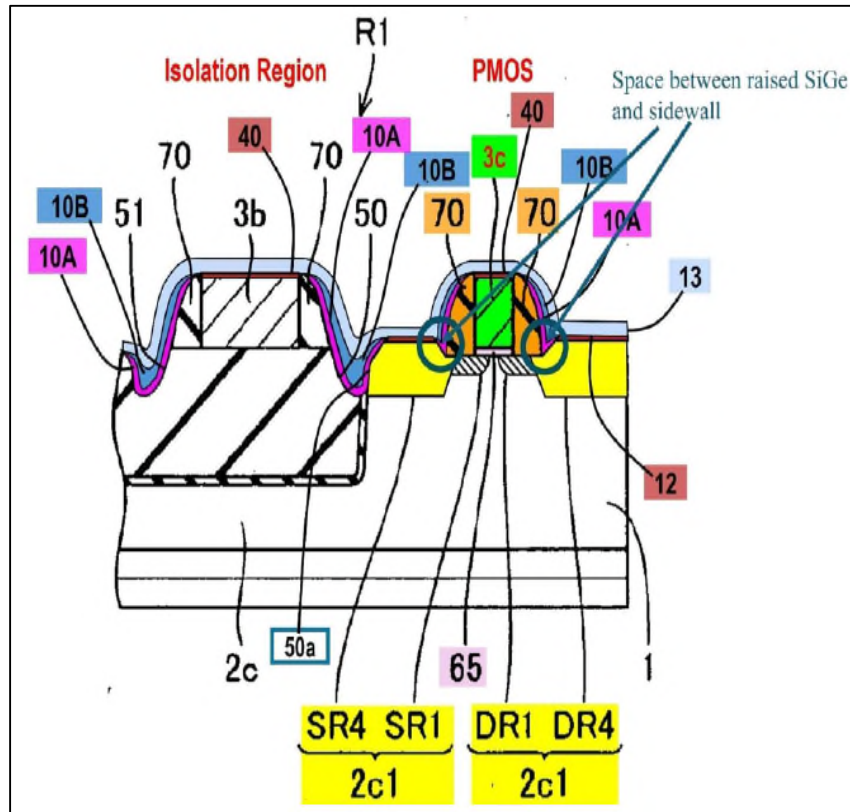


Figure M

10. Element 1[i]: “the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween”

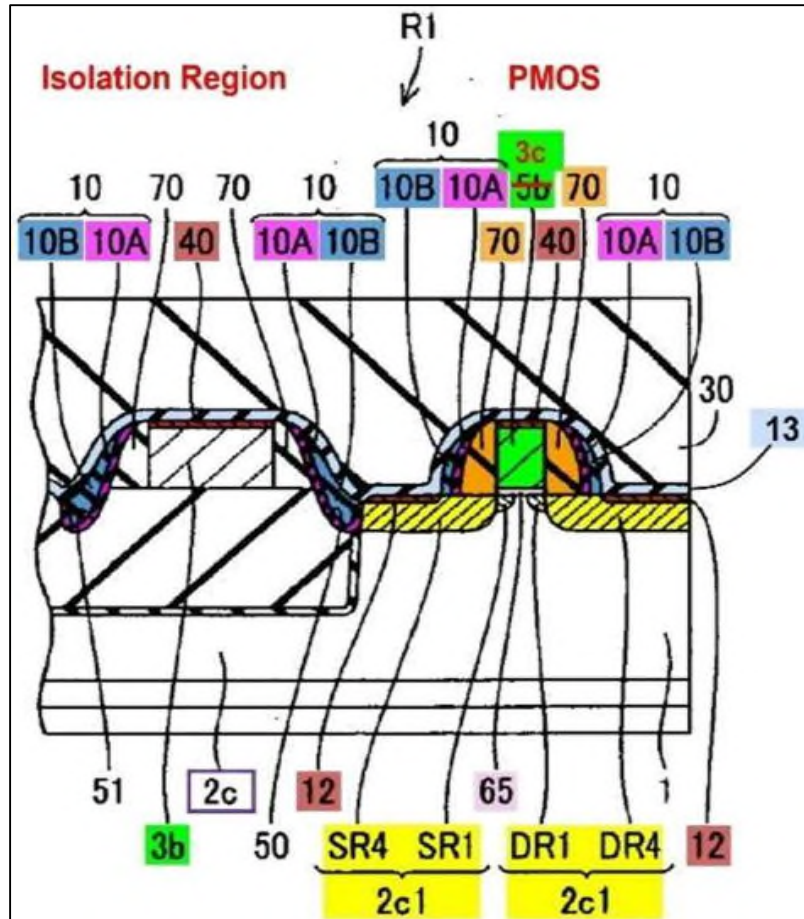
Saito825’s stress-relief film 10A (magenta) forms on side surfaces of wirings 3c (green) in PMOS transistor P2 with sidewalls 70 (orange) interposed therebetween (*see* Figure M). (*Supra* §VIII.B.9; Saito825, Ex.1010 ¶[0066]; Ex.1101, ¶¶385-386.)

11. Element 1[j]: “the first stress-relief film is not in direct contact with the side surface of the first gate electrode”

Saito825’s stress-relief film 10A (magenta) does not contact the side surface of polysilicon wiring 3c (green) since sidewalls 70 (orange) lie in between (*see* Figure M). (*Supra* §VIII.B.9-10; Saito825, Ex.1010, FIGS. 12, 21; Ex.1101, ¶¶387-388.)

C. Claim 3: “The semiconductor device of claim 1, further comprising: a first silicide layer formed on the first gate electrode; and a second silicide layer formed on the first source/drain region which includes the silicon compound layer”

Saito825 discloses a silicide film 40 (first silicide layer) formed on polysilicon wirings, including PMOS wirings 3b/3c, and a silicide film 12 (second silicide layer) formed on the source/drain regions of PMOS active region 2c. (Saito825, Ex.1010 ¶[0117]; *see id.*, ¶[0077], ¶[0124], FIGS. 3, 12, 20-21; Ex.1101, ¶¶389-391.)



Saito825, Ex.1010, FIG. 21 (excerpted)

When adding Fukutome's raised, faceted epitaxial SiGe source/drain regions to Saito825's PMOS active regions 2b/2c (*see* Figure M), a POSITA would have understood silicide film 12 forms atop the SiGe layers but not the SiGe facets (where insulating layer 10A would block silicidation), and silicide film 40 forms on polysilicon wirings 3b/3c as in Saito825. (Fukutome, Ex.1011 ¶¶[0103]-[0104], FIG. 5F; Saito825, Ex.1010 ¶¶[0107]-[0112], FIG. 19; Ex.1101, ¶¶392-393.)

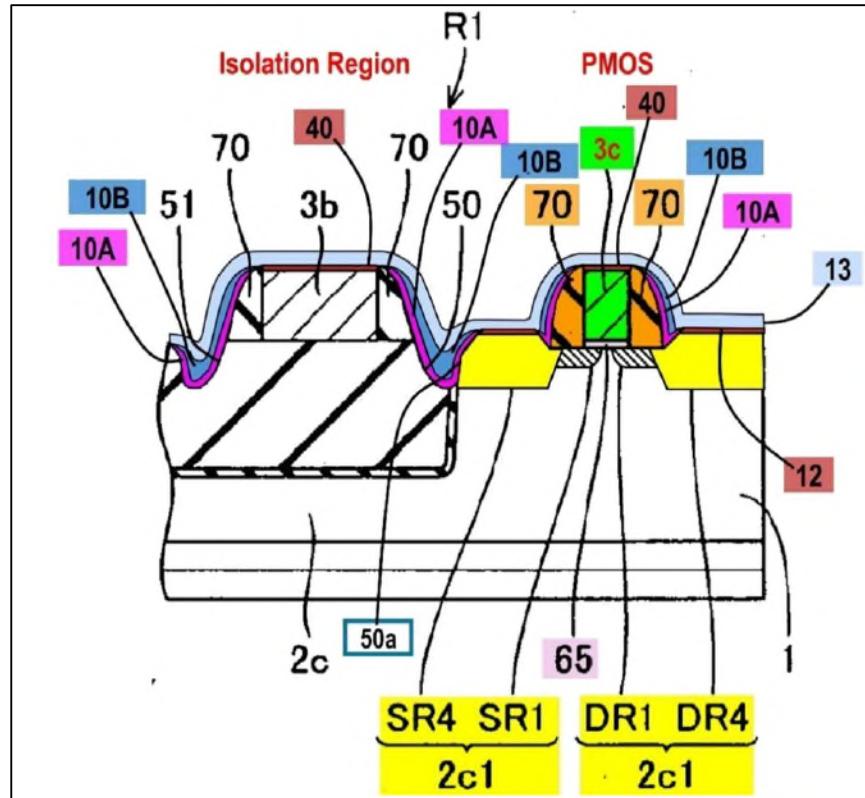


Figure M

With such silicidation, a POSITA would have found it obvious that the SiGe remains above the substrate to suppress junction leakage and improve reliability. (Fukutome, Ex.1011 ¶[0093], ¶¶[0099]-[0100], FIGS. 5F-5G; *Supra* §VIII.A.1; Ex.1101, ¶¶394-395.)

D. Claim 4: “The semiconductor device of claim 1, wherein the first stress-relief film is formed on a side surface of the silicon compound layer”

In the combination (*see* Figure M), oxide film 10A (stress-relief film, magenta) forms on a facet (side surface) of each raised SiGe layer (silicon compound layer, yellow). (*Supra* §VIII.B.9; Ex.1101, ¶¶396-397.)

E. Claim 7:

1. Element 7[pre]: “The semiconductor device of claim 1”

For the same reasons described in Sections VIII.B.1-11, the Saito825-Fukutome-James combination discloses the semiconductor device of claim 1. (*Supra* §§VIII.B.1-11; Ex.1101, ¶398.)

2. Element 7[a]: “the first MIS transistor is a p-type MIS transistor”

Saito825 discloses that the first MIS transistor is a PMOS transistor (e.g., PMOS transistor P2), “[s]econd access PMOS transistor P2.” (Saito825, Ex.1010, ¶[0066].) (*Supra* § VIII.B.2; Ex.1101, ¶398.)

3. Element 7[b]: “the first stress is a compressive stress”

Fukutome discloses raised SiGe source/drain regions, which, when added to the structure of Saito825, would cause compressive stress to the pFET channel region. (Fukutome ¶[0110]; James, Ex.1012, 2.) Figure M of the Saito825-Fukutome-James combination shows the raised SiGe source/drain regions that would cause compressive stress. (*Supra* §VIII.A.1, §VIII.B.6; Ex.1101, ¶400.)

4. Element 7[c]: “the second stress is a tensile stress”

Saito825 discloses a “insulating film 13” and James teaches that modifying the film would “increase[] electron mobility” in NMOS transistors N1-N4. (James, Ex.1012, 2, 5; Fig. 6.) Figure M of the Saito825-Fukutome-James combination

shows the tensile SiN insulating film 13 that would cause tensile stress. (*Supra* §VIII.A.1, §VIII.B.7; Ex.1101, ¶401.)

F. Claim 8:

1. Element 8[pre]: “The semiconductor device of claim 1”

For the same reasons described in Sections VIII.B.1-11, the Saito825-Fukutome-James combination discloses the semiconductor device of claim 1. (*Supra* §§VIII.A.1-11; Ex.1101, ¶402.)

2. Element 8[a]: “the silicon compound layer is a SiGe layer”

Fukutome teaches “a SiGe layer with a Ge concentration of 3 to 30% is selectively epitaxially grown in each of the recesses [trenches] 10a and 10b.” (Fukutome, Ex.1011 ¶[0005], ¶[0098], ¶[0110].) Figure M of the Saito825-Fukutome-James combination shows the raised SiGe source/drain regions. (*Supra* §§VIII.A.1 §VIII.A.6; Ex.1101, ¶403.)

3. Element 8[b]: “the stress insulating film is a silicon nitride film”

Saito825 discloses that film 13, corresponding to the stress insulating film, is made of silicon nitride. (Saito825, Ex.1010, ¶[0080], ¶[0120].) Figure M of the Saito825-Fukutome-James combination shows the silicon nitride insulating film 13. (*Supra* §VIII.A.1, §VIII.B.7; Ex.1101, ¶404.)

4. Element 8[c]: “the first stress-relief film is a silicon oxide film”

Saito825 discloses that film 10A, corresponding to the first stress-relief film, is made of silicon oxide. (Saito825, Ex.1010 ¶[0074], ¶[0076].) Figure M of the Saito825- Fukutome-James combination shows the silicon oxide film 10A. (*Supra* §§VIII.A.9; Ex.1101, ¶405.)

IX. Mandatory Notices

A. Real Party-in-Interest (37 C.F.R. §42.8(b)(1))

The Petitioner and real parties-in-interest are United Microelectronics Corporation and UMC Group (USA).

B. Related Matters (37 C.F.R. §42.8(b)(2))

To the best of Petitioner’s knowledge, the ’425 patent is subject of the following active proceedings:

- *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation*, Civil Action No. 2:24-cv-00730 in the Eastern District of Texas (Lead Case), filed September 6, 2024;
- *Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Manufacturing Company Limited*, Civil Action No. 2:24-cv-00623 in the Eastern District of Texas (Consolidated Member Case), filed August 1, 2024; and

- *Taiwan Semiconductor Manufacturing Company, Ltd. v. Advanced Integrated Circuit Process LLC*, IPR2025-00683.

C. Lead and Back-up Counsel (37 C.F.R. §42.8(b)(3))

Lead Counsel	Back Up Counsel
Tim Tingkang Xia (No. 45,242) Tim.Xia@troutman.com TROUTMAN PEPPER LOCKE LLP 600 Peachtree Street, NE, Suite 3000 Atlanta, GA 30308 Telephone: (404) 870-4698	Emma A. Bennett (No. 80,631) Emma.Bennett@troutman.com TROUTMAN PEPPER LOCKE LLP 600 Travis Street, Suite 2800 Houston, TX 77002 Telephone: (713) 226-1549

D. Service Information (37 C.F.R. §42.8(b)(4))

Service information is provided in the designation of counsel above. Petitioner consents to electronic service by email to Tim.Xia@troutman.com and Emma.Bennett@troutman.com.

E. Payment of Fees (37 C.F.R. §42.103)

The Office is authorized to charge the fee set forth in 37 C.F.R. §42.15(a)(1) for this Petition to Deposit Account No. DA201507. Review of six claims is requested. The undersigned further authorizes payment for any additional fees that may be due in connection with this Petition.

X. Conclusion

For the reasons set forth above, *Inter Partes* Review of the Challenged Claims of the '425 patent is respectfully requested.

Petition for *Inter Partes* Review of U.S. Patent No. 8,907,425

Respectfully submitted,

Date: June 6, 2025

/s/Tim Tinkang Xia
Tim Tinkang Xia (Lead Counsel)
Registration No. 45,242

Counsel for Petitioner

CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), I certify that this Petition complies with the type-volume limits of 37 C.F.R. §42.24(a)(1)(i) because it contains 12,793 words, according to the word-processing system used to prepare this Petition, excluding the parts of this Petition that are exempted by 37 C.F.R. §42.24(a)(1) (table of contents, table of authorities, mandatory notices under §42.8, certificate of service, certificate of word count, or appendix of exhibits or claim listing).

Date: June 6, 2025

/s/Tim Tingkang Xia

Tim Tingkang Xia (Lead Counsel)

Registration No. 45,242

Counsel for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §42.6(e), this is to certify that on this 6th day of June, 2025, I caused to be served on a USB thumb drive a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,907,425 Under 35 U.S.C. §§311, 312 and 37 C.F.R. §42.104 (with Exhibits 1001-1002, 1005-1006, 1008-1012, 1101-1111, 1211-1216, 1223, 1226-1227, 1229, 1318, 1323, 1340, 1413, 1417, 1419, 1421, 1428-1436, 1446-1450, 1506, 1512, 1515-1524, 1526-1529, 1531-1532) via Federal Express Priority Overnight at the Correspondence Address for Patent Owner:

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Counsel for Petitioner

Appendix: Challenged Claims Listing

1[pre] A semiconductor device, comprising: a first MIS transistor, wherein:

1[a] the first MIS transistor includes:

1[b] a first gate insulating film formed on a first active region in a semiconductor substrate,

1[c] a first gate electrode formed on the first gate insulating film,

1[d] a first sidewall spacer formed on a side surface of the first gate electrode,

1[e] a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region, and

1[f] a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress,

1[g] an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode,

1[h] a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer,

1[i] the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween, and

1[j] the first stress-relief film is not in direct contact with the side surface of the first gate electrode.

3. The semiconductor device of claim 1, further comprising: a first silicide layer formed on the first gate electrode; and a second silicide layer formed on the first source/drain region which includes the silicon compound layer.

4. The semiconductor device of claim 1, wherein the first stress-relief film is formed on a side surface of the silicon compound layer.

7[pre] The semiconductor device of claim 1, wherein

7[a] the first MIS transistor is a p-type MIS transistor,

7[b] the first stress is a compressive stress, and

7[c] the second stress is a tensile stress.

8[pre] The semiconductor device of claim 1, wherein

8[a] the silicon compound layer is a SiGe layer,

8[b] the stress insulating film is a silicon nitride film, and

8[c] the first stress-relief film is a silicon oxide film.

11[pre] The semiconductor device of claim 1,

11[a] further comprising: a second MIS transistor, wherein: the second MIS transistor includes:

11[b] a second gate insulating film formed on a second active region in the semiconductor substrate,

11[c] a second gate electrode formed on the second gate insulating film,

11[d] a second sidewall spacer formed on a side surface of the second gate electrode,

11[e] a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer, and

11[f] the stress insulating film formed on the second active region to cover the second gate electrode, the second sidewall spacer, and the second source/drain region.