

Exhibit 425-19: Wu922

U.S. Patent Application Publication No. 2009/0246922 (“Wu922”) was filed on March 27, 2008, and published on October 1, 2009. Accordingly, Wu922 constitutes prior art to U.S. Patent No. 8,907,425 (the “’425 patent”) under at least 35 U.S.C. §§ 102 (a) and (e).

Wu922, including any material incorporated by reference into Wu922, anticipates claims 1, 3-5, 7, and 11 (the “asserted claims”) of the ’425 patent under at least 35 U.S.C. §§ 102(a) and (e).

To the extent any limitation is found not to be expressly or inherently disclosed in Wu922, such a limitation would have been obvious either based on Wu922 alone, given the state of the art, or in combination with one or more of the references cited in Exhibits 425-01 through 425-18 and 425-20 through 425-21, because the ’425 patent is merely a collection of prior art elements that fails to meet the statutory requirement of non-obviousness under 35 U.S.C. § 103, and the factors delineated in *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), weigh against a finding of non-obviousness.

Any disclosures identified for each limitation of the ’425 patent in the aforementioned Exhibits may be combined with the disclosures of Wu922 identified below for the same limitation to render that limitation obvious. A POSITA would have found such a combination/modification obvious for the reasons discussed herein and in Defendant’s cover pleading.¹

The citations to portions of any reference in this chart are exemplary only. Citations to the written description should be interpreted to include the figures associated with or relevant to the cited passages. Similarly, citations to a figure should be understood to encompass any description, text, or discussion of that figure. Defendant reserves the right to use the entirety of any reference cited in this chart to show that the asserted claims are anticipated and/or are obvious. Citations presented for one claim limitation are expressly incorporated by reference into all other limitations for that claim as well as all limitations of all claims on which that claim depends.

¹ Plaintiff appears in many instances to be pursuing overly broad constructions of limitations of the asserted claims in an effort to piece together an infringement claim where none exists. This claim chart accounts for overly broad construction of the claim limitations. Any assertion that a particular limitation is disclosed by a prior art reference or references may be based on Plaintiff’s apparent constructions and is not intended to be, and is not, an admission that such constructions are supportable or proper. Defendant is investigating this prior art and has not yet completed discovery from third parties, who may have relevant information concerning the prior art. Therefore, Defendant reserves the right to supplement this chart after additional discovery is received. To the extent that any of the prior art discloses the same or similar functionality or feature(s) of any of the accused products, Defendant reserves the right to argue that said feature or functionality does not practice any limitation of any of the asserted claims, and to argue, in the alternative, that if said feature or functionality is found to practice any limitation of any of the asserted claims, then the prior art reference teaches the limitation and that the claim is not patentable.

Exemplary Disclosures

1[pre] A semiconductor device, comprising:

Defendant does not concede that the preamble is limiting. To the extent it is limiting, Wu922 discloses the preamble. For example, Wu922 discloses forming a CMOS transistor device. *See, e.g.,* the following:

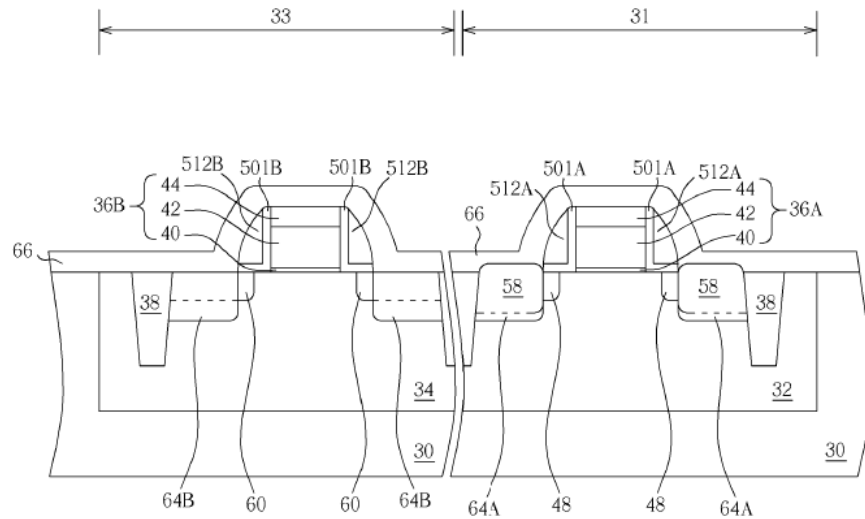


FIG. 7

FIG. 7.

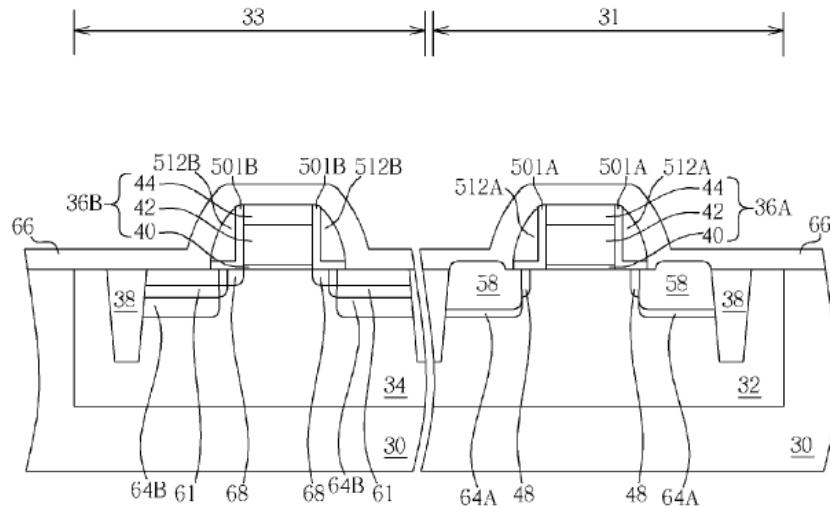


FIG. 14

FIG. 14.

Exemplary Disclosures

“A method of forming CMOS transistor is disclosed. A CMOS transistor having a first active area and a second active area is provided.”

Wu922, at Abstract.

“The present invention is related to a method of forming a CMOS transistor.”

Wu922 ¶ [0002].

“The primary objective of the present invention is to provide a method of forming a strained CMOS transistor to improve CMOS transistor performance and reliability and to overcome the drawback of conventional techniques.”

Wu922 ¶ [0009].

“Please refer to FIG. 1 to FIG. 7, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a first preferred embodiment of the present invention. Referring to FIG. 1, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the first preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. The following diagrams shows a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 for illustration. A plurality of isolation structures between the MOS transistors to prevent short circuiting, such as shallow trench isolations 38 formed between the PMOS transistor region 31 and the NMOS transistor region 33. Each of the gate structure 36A, 36B includes a gate dielectric layer 40, a gate 42, and a cap layer 44. The gate dielectric layer 40 may comprise dielectric materials including silicon oxide, oxynitride, and silicon nitride; high-k dielectric materials including metal oxide, metal silicate, metal aluminate, and metal oxynitride; or combinations thereof. The gate dielectric layer 40 may be formed by a thermal oxidation process, a nitridation process, or a chemical vapor deposition (CVD) process. The gate 42 may use polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof as material. The material of the cap layer 44 may include silicon oxide, oxynitride, silicon nitride, or silicon carbide (SiC). A thermal oxidation process is performed to form an oxide layer 501A, 501B on sidewalls of the gate structures 36A, 36B for protecting the gate structures 36A, 36B.”

Wu922 ¶ [0017].

Exemplary Disclosures

“Please refer to FIG. 8, which shows a flow diagram illustrating a method of forming a CMOS transistor in accordance with the first preferred embodiment of the present embodiment.”

Wu922 ¶ [0026].

“Moreover, the first preferred embodiment is illustrated using a PMOS transistor as the first active area, and an NMOS transistor as the second active area. In the contrast, the method of the first preferred embodiment can be modified to form a CMOS transistor having an NMOS transistor as the first active area, and a PMOS as the second active area. The first implantation process shown in FIG. 1 is performed to implant corresponding dopants, such as phosphorous (P) or other N-type dopants, into the semiconductor substrate to form a NLDD in the NMOS transistor. As shown in FIG. 4, the epitaxial layer of silicon carbide is formed. The second implantation process shown in FIG. 6 is performed to implant corresponding dopants, such as boron or other P-type dopants, into the semiconductor substrate to form a PLDD in the PMOS transistor. The following steps for forming the spacers and the source/drain in the PMOS transistors and the NMOS transistors are the same as those steps shown in the aforementioned first preferred embodiment.”

Wu922 ¶ [0037].

“Please refer to FIG. 9 to FIG. 14, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a second preferred embodiment of the present invention. Some elements are the same as those of the first preferred embodiment and are numbered as those of the first preferred embodiment. Referring to FIG. 9, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the second preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. For the simplicity of description, a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 are shown in the diagram in the following.”

Wu922 ¶ [0038].

“FIG. 15 is a flow diagram illustrating a method of forming a CMOS transistor in accordance with the second preferred embodiment of the present embodiment.”

Wu922 ¶ [0045].

Exemplary Disclosures

“Moreover, the first preferred embodiment is illustrated using a PMOS transistor as the first active area, and an NMOS transistor as the second active area. In the contrast, the method of the first preferred embodiment can be modified to form a CMOS transistor having an NMOS transistor as the first active area, and a PMOS as the second active area. The first implantation process shown in FIG. 9 is performed to implant corresponding dopants, such as boron or other P-type dopants, into the semiconductor substrate to form the PLDD1 in the PMOS transistor. As shown in FIG. 12, the epitaxial layer of silicon carbide is formed. The second implantation process shown in FIG. 14 is performed to implant P-type dopants, into the semiconductor substrate to form a PLDD2 in the PMOS transistor. The following steps of forming the spacers and the source/drain in the PMOS transistors and the NMOS transistors are the same as those steps shown in the aforementioned first preferred embodiment.”

Wu922 ¶ [0057].

To the extent that Wu922 is found not to disclose the preamble, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.

1[a] a first MIS transistor, wherein: the first MIS transistor includes:

Wu922 discloses this feature. For example, Wu922 discloses a PMOS transistor. *See, e.g.*, the following:

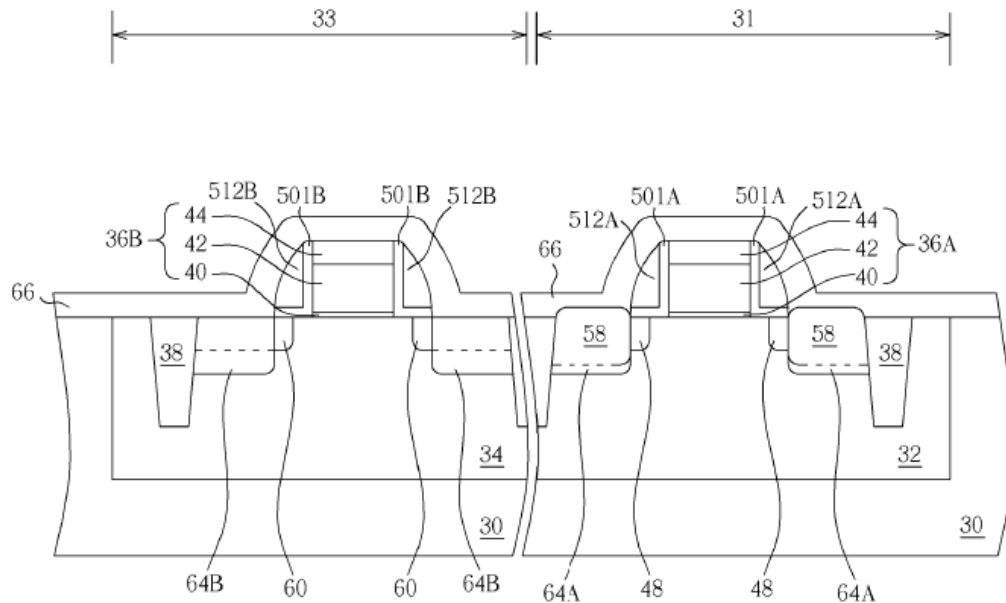
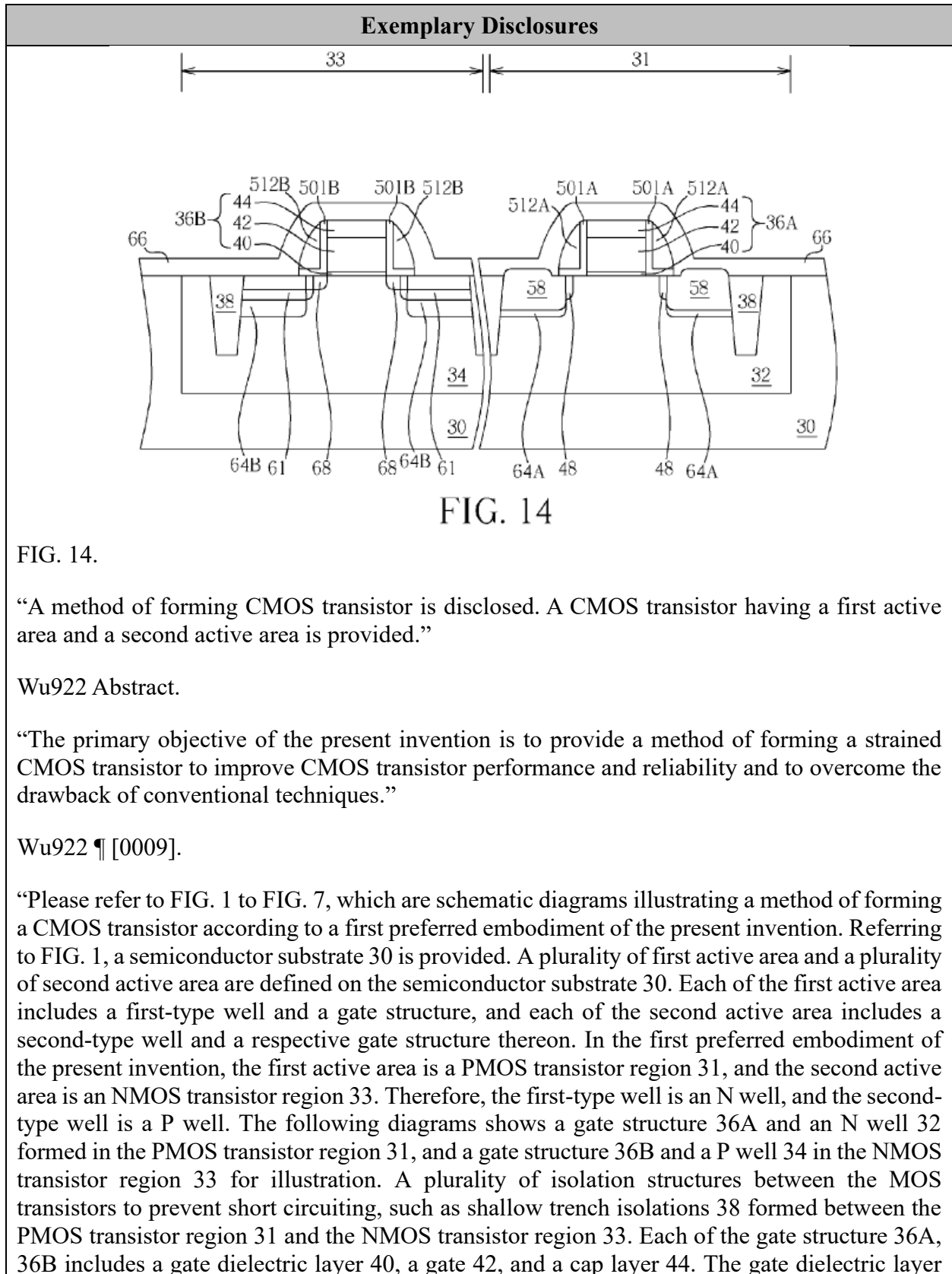


FIG. 7

FIG. 7.



Exemplary Disclosures

40 may comprise dielectric materials including silicon oxide, oxynitride, and silicon nitride; high-k dielectric materials including metal oxide, metal silicate, metal aluminate, and metal oxynitride; or combinations thereof. The gate dielectric layer 40 may be formed by a thermal oxidation process, a nitridation process, or a chemical vapor deposition (CVD) process. The gate 42 may use polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof as material. The material of the cap layer 44 may include silicon oxide, oxynitride, silicon nitride, or silicon carbide (SiC). A thermal oxidation process is performed to form an oxide layer 501A, 501B on sidewalls of the gate structures 36A, 36B for protecting the gate structures 36A, 36B.”

Wu922 ¶ [0017].

“Please refer to FIG. 8, which shows a flow diagram illustrating a method of forming a CMOS transistor in accordance with the first preferred embodiment of the present embodiment.”

Wu922 ¶ [0026].

“Step 700: providing a semiconductor substrate having a PMOS transistor, a NMOS transistor, and a plurality of gate structures formed in the PMOS transistor and the NMOS transistor[.]”

Wu922 ¶ [0027].

“Moreover, the first preferred embodiment is illustrated using a PMOS transistor as the first active area, and an NMOS transistor as the second active area. In the contrast, the method of the first preferred embodiment can be modified to form a CMOS transistor having an NMOS transistor as the first active area, and a PMOS as the second active area. The first implantation process shown in FIG. 1 is performed to implant corresponding dopants, such as phosphorous (P) or other N-type dopants, into the semiconductor substrate to form a NLDD in the NMOS transistor. As shown in FIG. 4, the epitaxial layer of silicon carbide is formed. The second implantation process shown in FIG. 6 is performed to implant corresponding dopants, such as boron or other P-type dopants, into the semiconductor substrate to form a PLDD in the PMOS transistor. The following steps for forming the spacers and the source/drain in the PMOS transistors and the NMOS transistors are the same as those steps shown in the aforementioned first preferred embodiment.”

Wu922 ¶ [0037].

“Please refer to FIG. 9 to FIG. 14, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a second preferred embodiment of the present invention. Some elements are the same as those of the first preferred embodiment and are numbered as those of the first preferred embodiment. Referring to FIG. 9, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the second preferred embodiment of the present invention,

Exemplary Disclosures

the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. For the simplicity of description, a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 are shown in the diagram in the following.”

Wu922 ¶ [0038].

“FIG. 15 is a flow diagram illustrating a method of forming a CMOS transistor in accordance with the second preferred embodiment of the present embodiment.”

Wu922 ¶ [0045].

“Step 800: providing a semiconductor substrate having a PMOS transistor, a NMOS transistor, and a plurality of gate structures formed in the PMOS transistor and the NMOS transistor[.]”

Wu922 ¶ [0046].

“Moreover, the first preferred embodiment is illustrated using a PMOS transistor as the first active area, and an NMOS transistor as the second active area. In the contrast, the method of the first preferred embodiment can be modified to form a CMOS transistor having an NMOS transistor as the first active area, and a PMOS as the second active area. The first implantation process shown in FIG. 9 is performed to implant corresponding dopants, such as boron or other P-type dopants, into the semiconductor substrate to form the PLDD1 in the PMOS transistor. As shown in FIG. 12, the epitaxial layer of silicon carbide is formed. The second implantation process shown in FIG. 14 is performed to implant P-type dopants, into the semiconductor substrate to form a PLDD2 in the PMOS transistor. The following steps of forming the spacers and the source/drain in the PMOS transistors and the NMOS transistors are the same as those steps shown in the aforementioned first preferred embodiment.”

Wu922 ¶ [0057].

See also, e.g., Wu922 ¶ [0023], ¶¶ [0028]-[0036], ¶¶ [0042]-[0043], ¶¶ [0047]-[0055], FIGS. 1-6, 9-13.

To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.

Wu922 discloses this feature. For example, Wu922 discloses a PMOS gate dielectric layer 40 formed on a PMOS active region of semiconductor substrate 30. *See, e.g.*, the following:



FIG. 14

FIG. 14.

Exemplary Disclosures

“Please refer to FIG. 1 to FIG. 7, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a first preferred embodiment of the present invention. Referring to FIG. 1, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the first preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. The following diagrams shows a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 for illustration. A plurality of isolation structures between the MOS transistors to prevent short circuiting, such as shallow trench isolations 38 formed between the PMOS transistor region 31 and the NMOS transistor region 33. Each of the gate structure 36A, 36B includes a gate dielectric layer 40, a gate 42, and a cap layer 44. The gate dielectric layer 40 may comprise dielectric materials including silicon oxide, oxynitride, and silicon nitride; high-k dielectric materials including metal oxide, metal silicate, metal aluminate, and metal oxynitride; or combinations thereof. The gate dielectric layer 40 may be formed by a thermal oxidation process, a nitridation process, or a chemical vapor deposition (CVD) process. The gate 42 may use polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof as material. The material of the cap layer 44 may include silicon oxide, oxynitride, silicon nitride, or silicon carbide (SiC). A thermal oxidation process is performed to form an oxide layer 501A, 501B on sidewalls of the gate structures 36A, 36B for protecting the gate structures 36A, 36B.”

Wu922 ¶ [0017].

“Please refer to FIG. 9 to FIG. 14, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a second preferred embodiment of the present invention. Some elements are the same as those of the first preferred embodiment and are numbered as those of the first preferred embodiment. Referring to FIG. 9, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the second preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. For the simplicity of description, a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 are shown in the diagram in the following.”

Wu922 ¶ [0038].

See also, e.g., Wu922 ¶ [0039].

Exemplary Disclosures

To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

1[c] a first gate electrode formed on the first gate insulating film,

Wu922 discloses this feature. For example, Wu922 discloses a PMOS gate electrode 42 formed on PMOS gate dielectric layer 40. *See, e.g.*, the following:

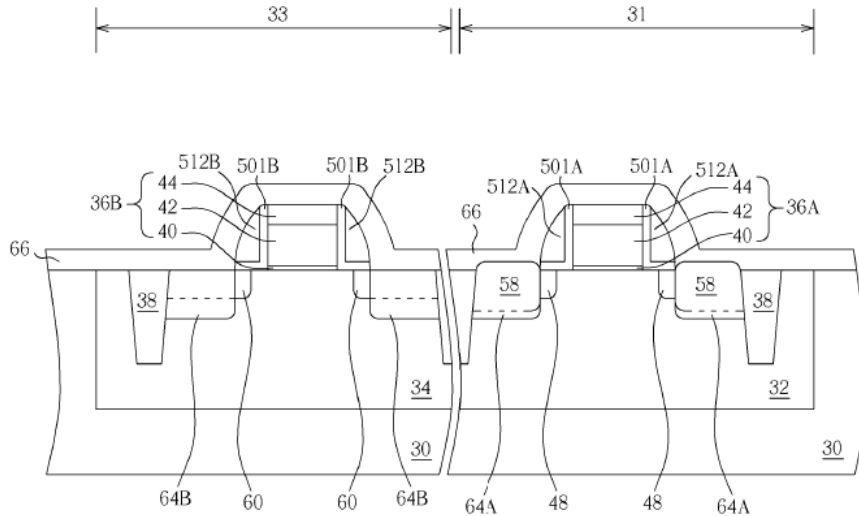


FIG. 7

FIG. 7.

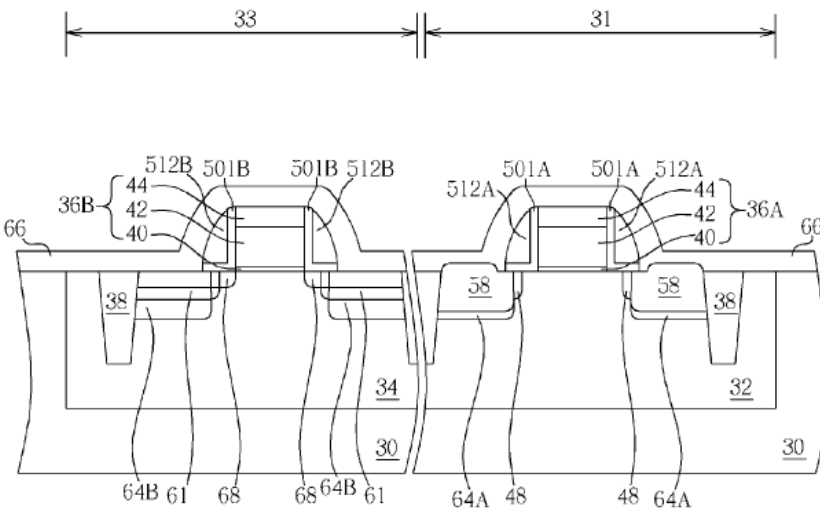


FIG. 14

FIG. 14.

Exemplary Disclosures

“Please refer to FIG. 1 to FIG. 7, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a first preferred embodiment of the present invention. Referring to FIG. 1, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the first preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. The following diagrams shows a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 for illustration. A plurality of isolation structures between the MOS transistors to prevent short circuiting, such as shallow trench isolations 38 formed between the PMOS transistor region 31 and the NMOS transistor region 33. Each of the gate structure 36A, 36B includes a gate dielectric layer 40, a gate 42, and a cap layer 44. The gate dielectric layer 40 may comprise dielectric materials including silicon oxide, oxynitride, and silicon nitride; high-k dielectric materials including metal oxide, metal silicate, metal aluminate, and metal oxynitride; or combinations thereof. The gate dielectric layer 40 may be formed by a thermal oxidation process, a nitridation process, or a chemical vapor deposition (CVD) process. The gate 42 may use polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof as material. The material of the cap layer 44 may include silicon oxide, oxynitride, silicon nitride, or silicon carbide (SiC). A thermal oxidation process is performed to form an oxide layer 501A, 501B on sidewalls of the gate structures 36A, 36B for protecting the gate structures 36A, 36B.”

Wu922 ¶ [0017].

“Please refer to FIG. 9 to FIG. 14, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a second preferred embodiment of the present invention. Some elements are the same as those of the first preferred embodiment and are numbered as those of the first preferred embodiment. Referring to FIG. 9, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the second preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. For the simplicity of description, a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 are shown in the diagram in the following.”

Wu922 ¶ [0038].

Exemplary Disclosures

Additionally, under Plaintiff's apparent interpretation of the claim language, the claimed "first gate electrode" may include a silicide film. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 11-13, 18, 20, 22, 24-25, 26, 39. Although TSMC does not necessarily agree with such an interpretation, Wu922 further discloses this element under this interpretation, as shown below.

For example, Wu922 discloses silicide layer formed on PMOS gate electrode 42. *See, e.g.*, the following:

"Please refer to FIG. 1 to FIG. 7, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a first preferred embodiment of the present invention. Referring to FIG. 1, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the first preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. The following diagrams shows a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 for illustration. A plurality of isolation structures between the MOS transistors to prevent short circuiting, such as shallow trench isolations 38 formed between the PMOS transistor region 31 and the NMOS transistor region 33. Each of the gate structure 36A, 36B includes a gate dielectric layer 40, a gate 42, and a cap layer 44. The gate dielectric layer 40 may comprise dielectric materials including silicon oxide, oxynitride, and silicon nitride; high-k dielectric materials including metal oxide, metal silicate, metal aluminate, and metal oxynitride; or combinations thereof. The gate dielectric layer 40 may be formed by a thermal oxidation process, a nitridation process, or a chemical vapor deposition (CVD) process. The gate 42 may use polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof as material. The material of the cap layer 44 may include silicon oxide, oxynitride, silicon nitride, or silicon carbide (SiC). A thermal oxidation process is performed to form an oxide layer 501A, 501B on sidewalls of the gate structures 36A, 36B for protecting the gate structures 36A, 36B."

Wu922 ¶ [0017].

"As shown in FIG. 7, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. The processes of forming the second spacers are the same as those processes for forming the first spacers 502A, 502B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source/drain 64B in the NMOS transistor region 33. The processes of forming the source/drain 64A, 64B are well known, and will not be described in detail. In addition, a self-aligned silicide process (salicide process) is optionally performed. A metal layer, including titanium (Ti), cobalt (Co), nickel (Ni), palladium (Pd), platinum (Pt) or the like, is deposited. And a rapid thermal

Exemplary Disclosures

process is performed to form a silicide layer (not shown) on the surfaces of the source/drain 64A, 64B.”

Wu922 ¶ [0024].

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”

Wu922 ¶ [0036].

“As shown in FIG. 14, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source drain 64B in the NMOS transistor region 33. In addition, a self-aligned silicide process is optionally performed to form a silicide layer (not shown) on the surfaces of the gate structures or the source/drain.”

Wu922 ¶ [0043].

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”

Wu922 ¶ [0055].

To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.

Wu922 discloses this feature. For example, Wu922 discloses L-shaped oxide spacers 501A and second spacers 512A, each formed on a side surface of PMOS gate electrode 42. L-shaped spacers 501A, alone or together with second spacers 512A, constitute a first sidewall spacer.² *See, e.g.*, the following:



FIG. 7.



FIG. 14.

² See *infra* 1[e] (explaining that the claimed “first sidewall spacer” may comprise second spacers 512A if the claimed “first source/drain region . . . on a lateral side of the first sidewall spacer” need not be formed in on a lateral side of the sidewall spacer at the time of source/drain formation).

Exemplary Disclosures

“Please refer to FIG. 1 to FIG. 7, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a first preferred embodiment of the present invention. Referring to FIG. 1, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the first preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. The following diagrams shows a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 for illustration. A plurality of isolation structures between the MOS transistors to prevent short circuiting, such as shallow trench isolations 38 formed between the PMOS transistor region 31 and the NMOS transistor region 33. Each of the gate structure 36A, 36B includes a gate dielectric layer 40, a gate 42, and a cap layer 44. The gate dielectric layer 40 may comprise dielectric materials including silicon oxide, oxynitride, and silicon nitride; high-k dielectric materials including metal oxide, metal silicate, metal aluminate, and metal oxynitride; or combinations thereof. The gate dielectric layer 40 may be formed by a thermal oxidation process, a nitridation process, or a chemical vapor deposition (CVD) process. The gate 42 may use polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof as material. The material of the cap layer 44 may include silicon oxide, oxynitride, silicon nitride, or silicon carbide (SiC). A thermal oxidation process is performed to form an oxide layer 501A, 501B on sidewalls of the gate structures 36A, 36B for protecting the gate structures 36A, 36B.”

Wu922 ¶ [0017].

“As shown in FIG. 7, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. The processes of forming the second spacers are the same as those processes for forming the first spacers 502A, 502B.”

Wu922 ¶ [0024].

“As shown in FIG. 1, a spacer formation process is optionally performed to form at least a first spacer 502A, 502B respectively beside the thermal oxide layers 501A, 501B. The preferred first spacers 502A, 502B may be a single-layered structure or a multi-layered structure. The preferred material of the first spacers 502A, 502B may use silicon oxide, silicon nitride, oxynitride, or other adoptable dielectric material. The first spacers 502A, 502B are formed by a plasma enhanced chemical vapor deposition (PECVD) process, a low-pressure chemical vapor deposition process (LPCVD), or other method for depositing the material layers of the first spacers 502A, 502B. Subsequently, an etch back process is performed to etch the material layers of the first spacers 502A, 502B.”

Wu922 ¶ [0018].

Exemplary Disclosures

“Step 701: forming at least a thermal oxide layer on the sidewalls of the gate structures[.]”

Wu922 ¶ [0028].

“Please refer to FIG. 9 to FIG. 14, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a second preferred embodiment of the present invention. Some elements are the same as those of the first preferred embodiment and are numbered as those of the first preferred embodiment. Referring to FIG. 9, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the second preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. For the simplicity of description, a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 are shown in the diagram in the following.”

Wu922 ¶ [0038].

“As shown in FIG. 9, a thermal oxidation process to form a thermal oxide layer 501A, 501B respectively formed on the sidewalls of the gate structures 36A, 36B, and a spacer formation process is performed to form at least a first spacer 502A, 502B respectively formed beside the thermal oxide layers 501A, 501B.”

Wu922 ¶ [0039].

“As shown in FIG. 14, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B.”

Wu922 ¶ [0043].

Additionally, under Plaintiff’s apparent interpretation of the claim language, the claimed “first gate electrode” may include a silicide film. *See* AICP’s P.R. 3-1 Disclosures, Ex. H, at 11-13, 18, 20, 22, 24-25, 26, 39. Although TSMC does not necessarily agree with such an interpretation, Wu922 further discloses this element under this interpretation, as shown below.

For example, Wu922 discloses silicide layer formed on PMOS gate electrode 42. *See, e.g.*, the following:

“Please refer to FIG. 1 to FIG. 7, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a first preferred embodiment of the present invention. Referring to FIG. 1, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a

Exemplary Disclosures

second-type well and a respective gate structure thereon. In the first preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. The following diagrams shows a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 for illustration. A plurality of isolation structures between the MOS transistors to prevent short circuiting, such as shallow trench isolations 38 formed between the PMOS transistor region 31 and the NMOS transistor region 33. Each of the gate structure 36A, 36B includes a gate dielectric layer 40, a gate 42, and a cap layer 44. The gate dielectric layer 40 may comprise dielectric materials including silicon oxide, oxynitride, and silicon nitride; high-k dielectric materials including metal oxide, metal silicate, metal aluminate, and metal oxynitride; or combinations thereof. The gate dielectric layer 40 may be formed by a thermal oxidation process, a nitridation process, or a chemical vapor deposition (CVD) process. The gate 42 may use polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof as material. The material of the cap layer 44 may include silicon oxide, oxynitride, silicon nitride, or silicon carbide (SiC). A thermal oxidation process is performed to form an oxide layer 501A, 501B on sidewalls of the gate structures 36A, 36B for protecting the gate structures 36A, 36B.”

Wu922 ¶ [0017].

“As shown in FIG. 7, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. The processes of forming the second spacers are the same as those processes for forming the first spacers 502A, 502B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source/drain 64B in the NMOS transistor region 33. The processes of forming the source/drain 64A, 64B are well known, and will not be described in detail. In addition, a self-aligned silicide process (salicide process) is optionally performed. A metal layer, including titanium (Ti), cobalt (Co), nickel (Ni), palladium (Pd), platinum (Pt) or the like, is deposited. And a rapid thermal process is performed to form a silicide layer (not shown) on the surfaces of the source/drain 64A, 64B.”

Wu922 ¶ [0024].

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”

Wu922 ¶ [0036].

Exemplary Disclosures

“As shown in FIG. 14, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source drain 64B in the NMOS transistor region 33. In addition, a self-aligned silicide process is optionally performed to form a silicide layer (not shown) on the surfaces of the gate structures or the source/drain.”

Wu922 ¶ [0043].

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”

Wu922 ¶ [0055].

To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.

1[e] a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and

Wu922 discloses this feature. For example, Wu922 discloses PMOS epitaxial layers 58 of a p-type conductivity which is formed in a recess 56 provided in the PMOS active region on a lateral side of L-shaped spacer 501A. PMOS epitaxial layers 58 comprise SiGe, which causes a compressive stress in a gate length direction of a channel region in the PMOS active region. *See, e.g.*, the following:

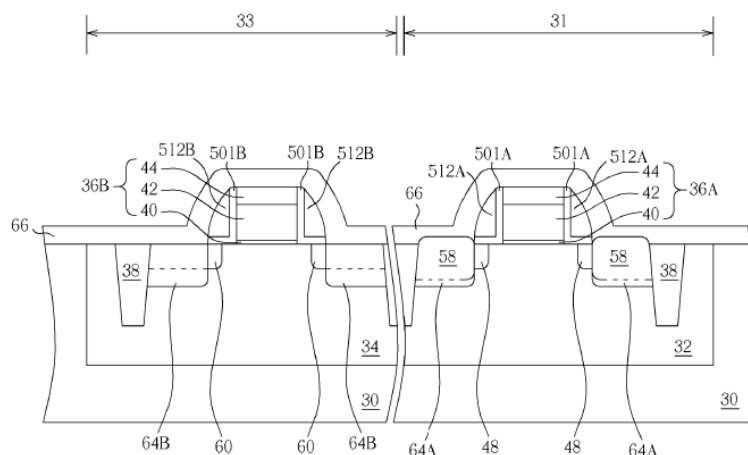


FIG. 7

FIG. 7.

Exemplary Disclosures

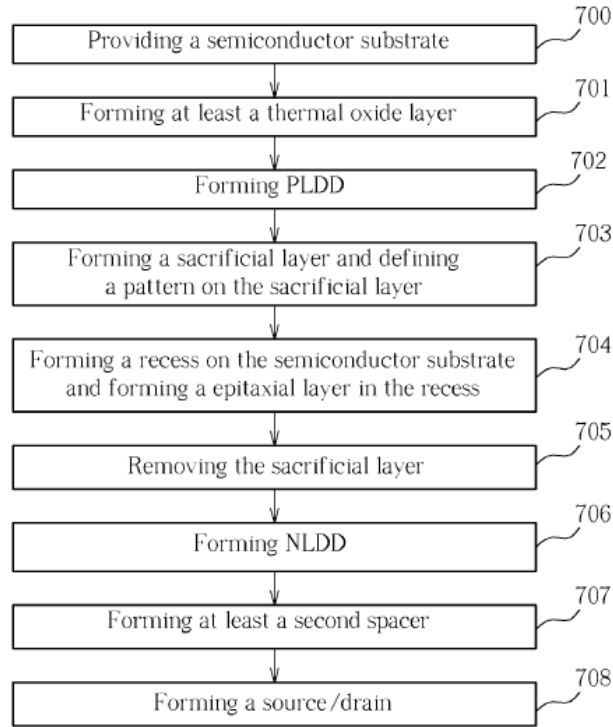


FIG. 8

FIG. 8.

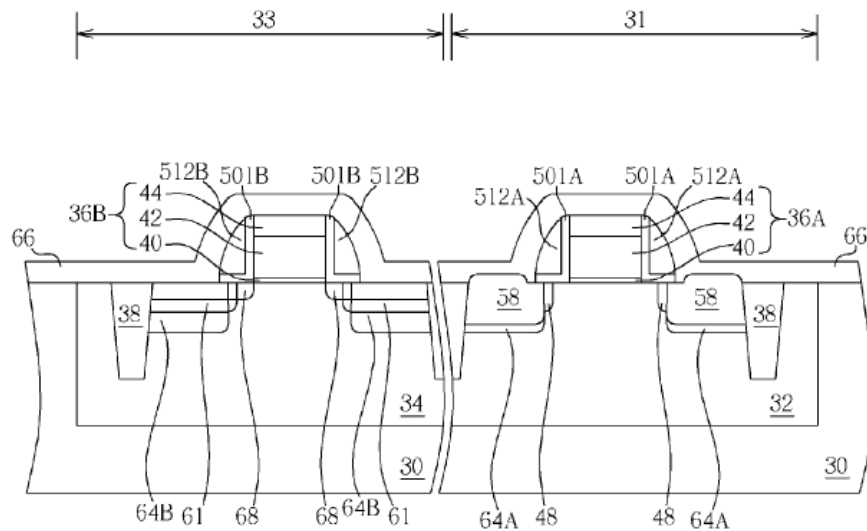


FIG. 14

FIG. 14.

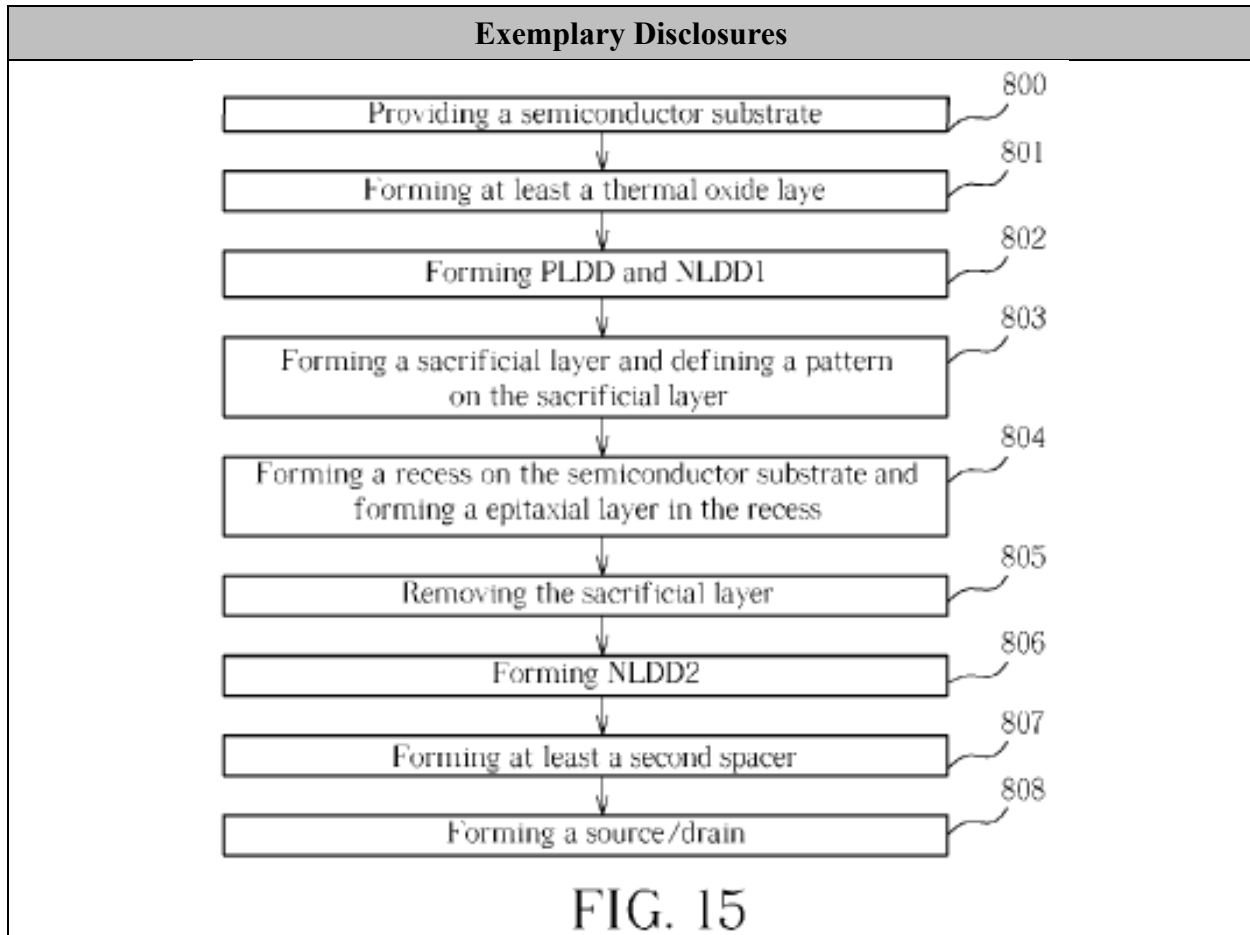


FIG. 15.

“As shown in FIG. 1, a spacer formation process is optionally performed to form at least a first spacer 502A, 502B respectively beside the thermal oxide layers 501A, 501B. The preferred first spacers 502A, 502B may be a single-layered structure or a multi-layered structure. The preferred material of the first spacers 502A, 502B may use silicon oxide, silicon nitride, oxynitride, or other adoptable dielectric material. The first spacers 502A, 502B are formed by a plasma enhanced chemical vapor deposition (PECVD) process, a low-pressure chemical vapor deposition process (LPCVD), or other method for depositing the material layers of the first spacers 502A, 502B. Subsequently, an etch back process is performed to etch the material layers of the first spacers 502A, 502B. A first patterned photoresist 46 is formed on the gate structure 36B and a surface of the N well 32. A first ion implantation process is performed to implant dopants, such as boron (B) or fluoride boron ion (BF⁺), into a region of the N well 32 beside the gate structure 36A. Therefore, a p-type light doped drain (PLDD) 48 is formed in a region of the N well 32 beside the gate structure 36A. Furthermore, a rapid thermal process is optionally performed after the formation of the PLDD 48 for diffusing and activating the dopants therein.”

Wu922 ¶ [0018].

Exemplary Disclosures

“Please refer to FIG. 4 in company with FIG. 3. The second patterned photoresist 54 is removed. A selective epitaxial growth process is performed to form an epitaxial layer, such as an epitaxial layer 58 of silicon germanium. The preferred epitaxial layer 58 has a lattice constant greater than that of the semiconductor substrate 30, and is slightly extended approaching to the channel. Preferably, the epitaxial layer 58 is slightly projected from the top surface of the semiconductor substrate 30 to compress the channel and to keep silicon layers formed in the following steps from the interface between the source/drain in a distance. The top surface of the epitaxial layer 58 may be substantially leveled with or lower than the top surface of semiconductor substrate 30.”

Wu922 ¶ [0021].

“Step 702: performing a first ion implantation process to form a PLDD in the semiconductor substrate beside the gate structures of the PMOS transistor[.]”

Wu922 ¶ [0029].

“Step 704: using the patterned sacrificial layer as an etching mask, etching the semiconductor substrate in the PMOS transistor region, and forming an epitaxial layer in the recess, preferably an epitaxial layer of silicon germanium[.]”

Wu922 ¶ [0031].

“As shown in FIG. 9, a thermal oxidation process to form a thermal oxide layer 501A, 501B respectively formed on the sidewalls of the gate structures 36A, 36B, and a spacer formation process is performed to form at least a first spacer 502A, 502B respectively formed beside the thermal oxide layers 501A, 501B. A first ion implantation process is performed to implant dopants, to form an NLDD1 61 in the NMOS transistor region 33 and a PLDD 48 in the PMOS transistor region 31. In addition, a rapid thermal process is optionally performed after the formation of the PLDD 48 in order to diffuse and to activate the dopants.”

Wu922 ¶ [0039].

“Please refer to FIG. 12 in company with FIG. 11. The second patterned photoresist 54 is removed. A selective epitaxial growth process is performed to form an epitaxial layer, such as an epitaxial layer 58 of silicon germanium. The preferred epitaxial layer 58 has a lattice constant greater than that of the semiconductor substrate 30, and is extended approaching to the channel. In order to compress the channel and to keep the silicon layer formed in the following steps from the interface between the source/drain in a distance, the preferred epitaxial layer 58 is slightly projected from the top surface of the semiconductor substrate 30. The top surface of the epitaxial layer 58 may be substantially leveled with or lower than the top surface of semiconductor substrate 30.”

Wu922 ¶ [0041].

Exemplary Disclosures

“Step 802: performing a first ion implantation process to form a PLDD in the semiconductor substrate beside the gate structures of the PMOS transistor, and an NLDD1 in the semiconductor substrate beside the gate structures of the NMOS transistor[.]”

Wu922 ¶ [0048].

“Step 804: using the patterned sacrificial layer as an etching mask, etching the semiconductor substrate beside the gate structure in the PMOS transistor region, and forming an epitaxial layer in the recess, i.e. an epitaxial layer of silicon germanium[.]”

Wu922 ¶ [0050].

See also, e.g., Wu922 Abstract, ¶ [0005], ¶ [0009], ¶¶ [0017]-[0018], ¶¶ [0020]-[0021], ¶ [0024], ¶ [0029], ¶ [0031], ¶¶ [0035]-[0036], ¶¶ [0039]-[0041], ¶ [0043], ¶ [0048], ¶ [0050], ¶¶ [0054]-[0058], FIGS. 3-8, 11-15.

Under Plaintiff’s apparent interpretation of the claim language, the claimed “first source/drain region . . . on a lateral side of the first sidewall spacer” need not be formed in on a lateral side of the sidewall spacer at the time of the source/drain formation. *See* AICP’s P.R. 3-1 Disclosures, Ex. H, at 12-13. Although TSMC disagrees with such an interpretation, Wu922’s first sidewall spacer may further include second spacer 512A (in addition to L-shaped oxide layer 501A) under this interpretation, as shown below.

“As shown in FIG. 7, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. The processes of forming the second spacers are the same as those processes for forming the first spacers 502A, 502B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source/drain 64B in the NMOS transistor region 33. The processes of forming the source/drain 64A, 64B are well known, and will not be described in detail.”

Wu922 ¶ [0024].

“Step 705: removing the sacrificial layer;

“Step 706: performing a second ion implantation process to form an NLDD in the semiconductor substrate beside the gate structure of the NMOS transistor;

“Step 707: forming at least a second spacer on the sidewalls of the gate structures; and

“Step 708: performing a third ion implantation process to form a respective source/drain in the semiconductor substrate beside the gate structures of the NMOS transistor and the PMOS transistor.”

Wu922 ¶¶ [0032]-[0035].

Exemplary Disclosures

“Please refer to FIG. 13, another etch process is performed, preferably a phosphoric acid treatment, to remove the sacrificial layer 52 and the first spacers 502A, 502B. In the present embodiment, the sacrificial layer 52 and the first spacers 502A, 502B are made of silicon nitride, and so that the sacrificial layer 52 and the first spacers 502A, 502B are removed by the phosphoric acid treatment simultaneously. A second ion implantation process is performed to form an NLDD2 68 in the P well 34 beside the gate structure 36B. The formation of the NLDD2 68 may use the same fabrication processes as the first ion implantation by means of forming a patterned photoresist formed to protect the N well 32 and the gate structure 36A in the PMOS transistor region 31. Then, the second ion implantation process is performed to implant dopants into the Pwell 34. In addition, a rapid thermal process is optionally performed after the formation of the NLDD2 68 for diffusing and activating the dopants.”

Wu922 ¶ [0042].

“As shown in FIG. 14, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source drain 64B in the NMOS transistor region 33.”

Wu922 ¶ [0043].

“Step 805: removing the sacrificial layer;

Step 806: performing a second ion implantation process to form an NLDD2 in the semiconductor substrate beside the gate structure of the NMOS transistor;

“Step 807: forming at least a second spacer on the sidewalls of the gate structures; and

“Step 808: performing a third ion implantation process to form a respective source/drain in the semiconductor substrate beside the gate structures of the NMOS transistor and the PMOS transistor.”

Wu922 ¶¶ [0051]-[0054].

To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.

Exemplary Disclosures
1[f] which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region, and
Wu922 discloses this feature. For example, PMOS epitaxial layers 58 comprise SiGe, which exerts a compressive stress on the PMOS channel region. <i>See, e.g.</i>, the following: “In order to increase the driving current of a complementary metal-oxide semiconductor (CMOS) transistor including a p-type MOS (PMOS) transistor and an n-type MOS (NMOS) transistor, the industrial circles develop a strained-silicon technique, which uses unique processes or lattice constant discrepancy to increase driving current. The strained-silicon technique substantially includes a substrate strained based method and a process-induced strain based method. The substrate-strained based system is performed with a strained-silicon substrate or a selective epitaxial growth process that results in lattice constant discrepancy. The process-induced strain based method is performed with several unique processes to form a strained thin film upon a surface of the MOS transistor that exert tensile stress or compressive stress upon the MOS transistor. Both of the strained silicon techniques introduce strain into the channel region and reduce carrier mobile resistance thereby improving carrier mobility and MOS transistor performance.” Wu922 ¶ [0005]. “The primary objective of the present invention is to provide a method of forming a strained CMOS transistor to improve CMOS transistor performance and reliability and to overcome the drawback of conventional techniques. Initially, a semiconductor substrate having at least a first active area and at least a second active area is provided. The first active area and the second active area include a respective gate structure. A first light doped drain is formed beside the gate structure in the first active area. A sacrificial layer is formed on the semiconductor substrate. An etch process is performed to etch the sacrificial layer and a surface of the semiconductor substrate beside the gate structure in the first active area to form a recess on a surface of the semiconductor substrate beside the gate structure of the first active area. A selective epitaxial process is performed to form an epitaxial layer in the recess. After that, the sacrificial layer is removed, and a second light doped drain is formed beside gate structure in the second active area.” Wu922 ¶ [0009].

Exemplary Disclosures

“Please refer to FIG. 4 in company with FIG. 3. The second patterned photoresist 54 is removed. A selective epitaxial growth process is performed to form an epitaxial layer, such as an epitaxial layer 58 of silicon germanium. The preferred epitaxial layer 58 has a lattice constant greater than that of the semiconductor substrate 30, and is slightly extended approaching to the channel. Preferably, the epitaxial layer 58 is slightly projected from the top surface of the semiconductor substrate 30 to compress the channel and to keep silicon layers formed in the following steps from the interface between the source/drain in a distance. The top surface of the epitaxial layer 58 may be substantially leveled with or lower than the top surface of semiconductor substrate 30.”

Wu922 ¶ [0021].

“Step 704: using the patterned sacrificial layer as an etching mask, etching the semiconductor substrate in the PMOS transistor region, and forming an epitaxial layer in the recess, preferably an epitaxial layer of silicon germanium[.]”

Wu922 ¶ [0031].

“Please refer to FIG. 12 in company with FIG. 11. The second patterned photoresist 54 is removed. A selective epitaxial growth process is performed to form an epitaxial layer, such as an epitaxial layer 58 of silicon germanium. The preferred epitaxial layer 58 has a lattice constant greater than that of the semiconductor substrate 30, and is extended approaching to the channel. In order to compress the channel and to keep the silicon layer formed in the following steps from the interface between the source/drain in a distance, the preferred epitaxial layer 58 is slightly projected from the top surface of the semiconductor substrate 30. The top surface of the epitaxial layer 58 may be substantially leveled with or lower than the top surface of semiconductor substrate 30.”

Wu922 ¶ [0041].

“Step 804: using the patterned sacrificial layer as an etching mask, etching the semiconductor substrate beside the gate structure in the PMOS transistor region, and forming an epitaxial layer in the recess, i.e. an epitaxial layer of silicon germanium[.]”

Wu922 ¶ [0050].

Additionally, under Plaintiff’s apparent interpretation of the claim language, the claimed “silicon compound layer” may include a silicide film. *See* AICP’s P.R. 3-1 Disclosures, Ex. H, at 15, 20, 21, 25, 26, 31. Although TSMC disagrees with such an interpretation, Wu922 further discloses [1f] under this interpretation, as shown below.

“Please refer to FIG. 1 to FIG. 7, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a first preferred embodiment of the present invention. Referring to FIG. 1, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area

Exemplary Disclosures

includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the first preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. The following diagrams shows a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 for illustration. A plurality of isolation structures between the MOS transistors to prevent short circuiting, such as shallow trench isolations 38 formed between the PMOS transistor region 31 and the NMOS transistor region 33. Each of the gate structure 36A, 36B includes a gate dielectric layer 40, a gate 42, and a cap layer 44. The gate dielectric layer 40 may comprise dielectric materials including silicon oxide, oxynitride, and silicon nitride; high-k dielectric materials including metal oxide, metal silicate, metal aluminate, and metal oxynitride; or combinations thereof. The gate dielectric layer 40 may be formed by a thermal oxidation process, a nitridation process, or a chemical vapor deposition (CVD) process. The gate 42 may use polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof as material. The material of the cap layer 44 may include silicon oxide, oxynitride, silicon nitride, or silicon carbide (SiC). A thermal oxidation process is performed to form an oxide layer 501A, 501B on sidewalls of the gate structures 36A, 36B for protecting the gate structures 36A, 36B.”

Wu922 ¶ [0017].

“As shown in FIG. 7, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. The processes of forming the second spacers are the same as those processes for forming the first spacers 502A, 502B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source/drain 64B in the NMOS transistor region 33. The processes of forming the source/drain 64A, 64B are well known, and will not be described in detail. In addition, a self-aligned silicide process (salicide process) is optionally performed. A metal layer, including titanium (Ti), cobalt (Co), nickel (Ni), palladium (Pd), platinum (Pt) or the like, is deposited. And a rapid thermal process is performed to form a silicide layer (not shown) on the surfaces of the source/drain 64A, 64B.”

Wu922 ¶ [0024].

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”

Wu922 ¶ [0036].

Exemplary Disclosures

“As shown in FIG. 14, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source drain 64B in the NMOS transistor region 33. In addition, a self-aligned silicide process is optionally performed to form a silicide layer (not shown) on the surfaces of the gate structures or the source/drain.”

Wu922 ¶ [0043].

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”

Wu922 ¶ [0055].

See also, e.g., Wu922 Abstract, ¶ [0005], ¶ [0009], ¶¶ [0017]-[0018], ¶¶ [0020]-[0021], ¶ [0024], ¶ [0029], ¶ [0031], ¶¶ [0035]-[0036], ¶¶ [0039]-[0041], ¶ [0043], ¶ [0048], ¶ [0050], ¶¶ [0054]-[0058], FIGS. 3-8, 11-15.

To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.

Exemplary Disclosures

1[g] a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and

Wu922 discloses this feature. For example, Wu922 discloses contact etch stop layer (CESL) 66 which is formed on the PMOS active region to cover PMOS gate electrode 42, L-shaped sidewall spacer 501A, second spacer 512A, and PMOS epitaxial SiGe layers 58. *See, e.g.*, the following:

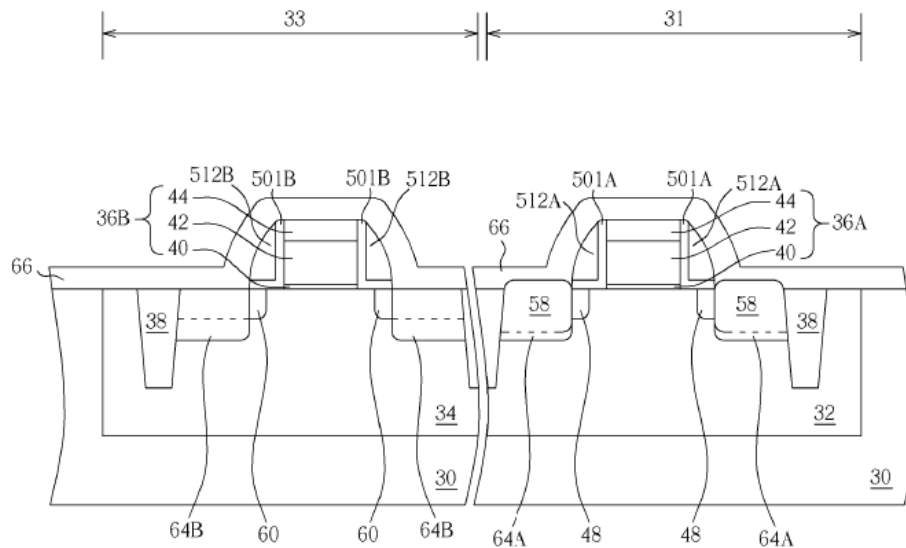


FIG. 7

FIG. 7.

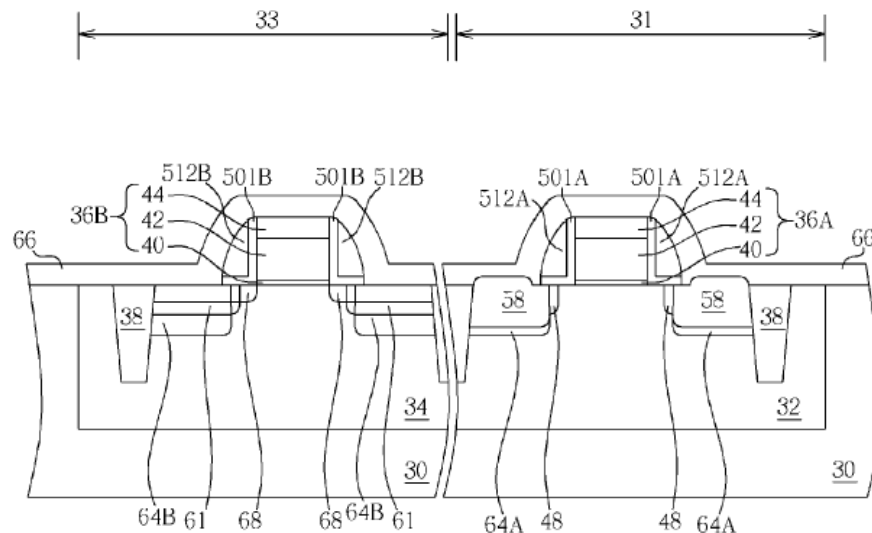


FIG. 14

FIG. 14.

Exemplary Disclosures

“In order to increase the driving current of a complementary metal-oxide semiconductor (CMOS) transistor including a p-type MOS (PMOS) transistor and an n-type MOS (NMOS) transistor, the industrial circles develop a strained-silicon technique, which uses unique processes or lattice constant discrepancy to increase driving current. The strained-silicon technique substantially includes a substrate strained based method and a process-induced strain based method. The substrate-strained based system is performed with a strained-silicon substrate or a selective epitaxial growth process that results in lattice constant discrepancy. The process-induced strain based method is performed with several unique processes to form a strained thin film upon a surface of the MOS transistor that exert tensile stress or compressive stress upon the MOS transistor. Both of the strained silicon techniques introduce strain into the channel region and reduce carrier mobile resistance thereby improving carrier mobility and MOS transistor performance.”

Wu922 ¶ [0005].

“A deposition process is performed to form a contact etch stop layer (CESL) 66 on the surface of the gate structures 36A, 36B, the second spacers 512A, 512B, and the sources/drains 64A, 64B. The material of the CESL 66 may include a dielectric material or a strained silicon material, i.e. silicon nitride.”

Wu922 ¶ [0025].

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”

Wu922 ¶ [0036].

“A deposition process is performed to form a CESL 66 on the surface of the gate structures 36A, 36B, the second spacers 512A, 512B, and the sources/drains 64A, 64B.”

Wu922 ¶ [0044].

Additionally, under Plaintiff’s apparent interpretation of the claim language, the claimed “first gate electrode” may include a silicide film. *See* AICP’s P.R. 3-1 Disclosures, Ex. H, at 11-13, 18, 20, 22, 24-25, 26, 39. Although TSMC does not necessarily agree with such an interpretation, Wu922 further discloses this element under this interpretation, as shown below.

Exemplary Disclosures

For example, Wu922 discloses silicide layer formed on PMOS gate electrode 42. *See, e.g.*, the following:

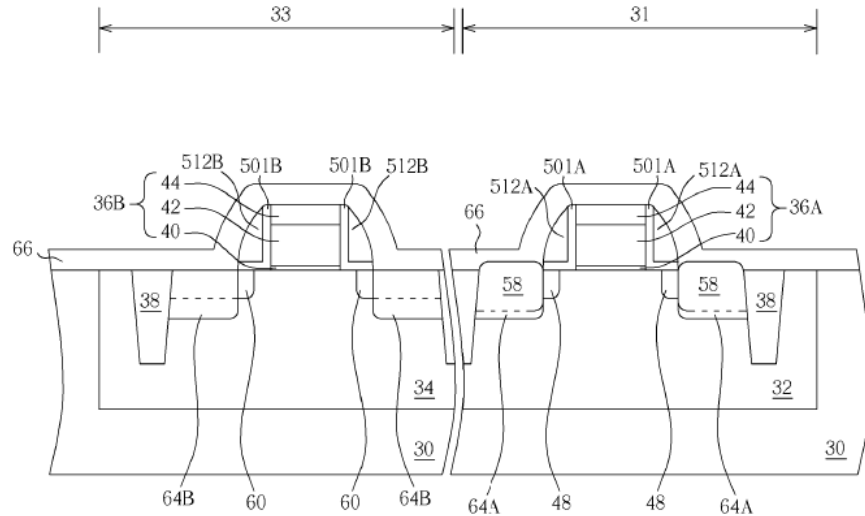


FIG. 7

FIG. 7.

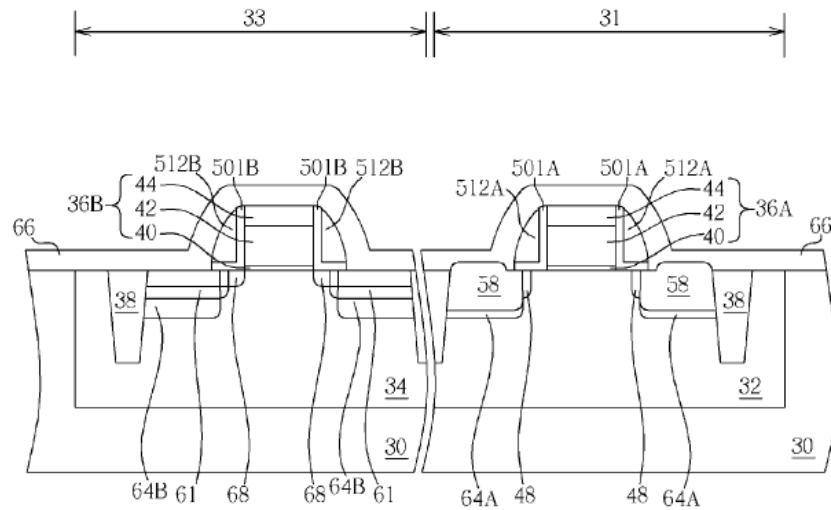


FIG. 14

FIG. 14.

“Please refer to FIG. 1 to FIG. 7, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a first preferred embodiment of the present invention. Referring to FIG. 1, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a

Exemplary Disclosures

second-type well and a respective gate structure thereon. In the first preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. The following diagrams shows a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 for illustration. A plurality of isolation structures between the MOS transistors to prevent short circuiting, such as shallow trench isolations 38 formed between the PMOS transistor region 31 and the NMOS transistor region 33. Each of the gate structure 36A, 36B includes a gate dielectric layer 40, a gate 42, and a cap layer 44. The gate dielectric layer 40 may comprise dielectric materials including silicon oxide, oxynitride, and silicon nitride; high-k dielectric materials including metal oxide, metal silicate, metal aluminate, and metal oxynitride; or combinations thereof. The gate dielectric layer 40 may be formed by a thermal oxidation process, a nitridation process, or a chemical vapor deposition (CVD) process. The gate 42 may use polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof as material. The material of the cap layer 44 may include silicon oxide, oxynitride, silicon nitride, or silicon carbide (SiC). A thermal oxidation process is performed to form an oxide layer 501A, 501B on sidewalls of the gate structures 36A, 36B for protecting the gate structures 36A, 36B.”

Wu922 ¶ [0017].

“As shown in FIG. 7, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. The processes of forming the second spacers are the same as those processes for forming the first spacers 502A, 502B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source/drain 64B in the NMOS transistor region 33. The processes of forming the source/drain 64A, 64B are well known, and will not be described in detail. In addition, a self-aligned silicide process (salicide process) is optionally performed. A metal layer, including titanium (Ti), cobalt (Co), nickel (Ni), palladium (Pd), platinum (Pt) or the like, is deposited. And a rapid thermal process is performed to form a silicide layer (not shown) on the surfaces of the source/drain 64A, 64B.”

Wu922 ¶ [0024].

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”

Wu922 ¶ [0036].

Exemplary Disclosures
“As shown in FIG. 14, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source drain 64B in the NMOS transistor region 33. In addition, a self-aligned silicide process is optionally performed to form a silicide layer (not shown) on the surfaces of the gate structures or the source/drain.” Wu922 ¶ [0043]. “Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.” Wu922 ¶ [0055]. To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.
1[h] which causes a second stress opposite to the first stress,
Wu922 discloses this feature. <i>See, e.g., supra</i> 1[g]. <i>See, e.g.,</i> the following: “In order to increase the driving current of a complementary metal-oxide semiconductor (CMOS) transistor including a p-type MOS (PMOS) transistor and an n-type MOS (NMOS) transistor, the industrial circles develop a strained-silicon technique, which uses unique processes or lattice constant discrepancy to increase driving current. The strained-silicon technique substantially includes a substrate strained based method and a process-induced strain based method. The substrate-strained based system is performed with a strained-silicon substrate or a selective epitaxial growth process that results in lattice constant discrepancy. The process-induced strain based method is performed with several unique processes to form a strained thin film upon a surface of the MOS transistor that exert tensile stress or compressive stress upon the MOS transistor. Both of the strained silicon techniques introduce strain into the channel region and reduce carrier mobile resistance thereby improving carrier mobility and MOS transistor performance.” Wu922 ¶ [0005]. “A deposition process is performed to form a contact etch stop layer (CESL) 66 on the surface of the gate structures 36A, 36B, the second spacers 512A, 512B, and the sources/drains 64A, 64B. The material of the CESL 66 may include a dielectric material or a strained silicon material, i.e. silicon nitride.” Wu922 ¶ [0025].

Exemplary Disclosures

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”

Wu922 ¶ [0036].

“A deposition process is performed to form a CESL 66 on the surface of the gate structures 36A, 36B, the second spacers 512A, 512B, and the sources/drains 64A, 64B.”

Wu922 ¶ [0044].

To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.

1[i] an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode,

Wu922 discloses this feature. For example, Wu922 discloses that an uppermost surface of PMOS epitaxial SiGe layers 58 is located higher than a surface of semiconductor substrate 30 located directly under the PMOS gate electrode 42. *See, e.g.*, the following:

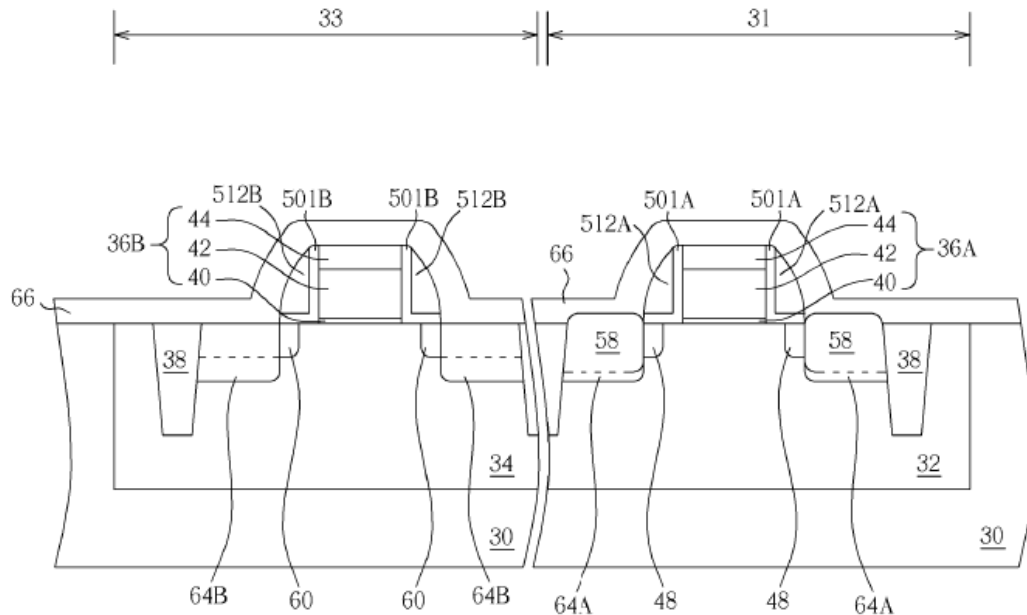


FIG. 7

FIG. 7.

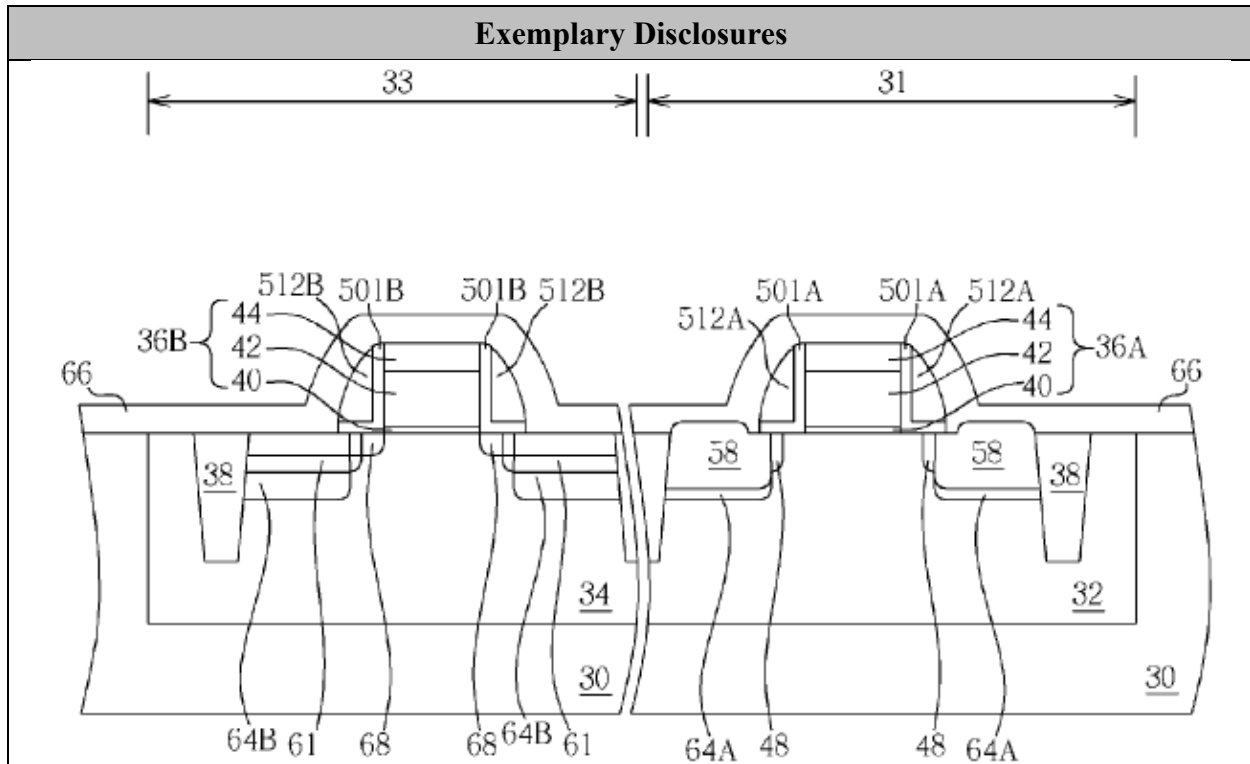


FIG. 14

FIG. 14.

“Please refer to FIG. 4 in company with FIG. 3. The second patterned photoresist 54 is removed. A selective epitaxial growth process is performed to form an epitaxial layer, such as an epitaxial layer 58 of silicon germanium. The preferred epitaxial layer 58 has a lattice constant greater than that of the semiconductor substrate 30, and is slightly extended approaching to the channel. Preferably, the epitaxial layer 58 is slightly projected from the top surface of the semiconductor substrate 30 to compress the channel and to keep silicon layers formed in the following steps from the interface between the source/drain in a distance. The top surface of the epitaxial layer 58 may be substantially leveled with or lower than the top surface of semiconductor substrate 30.”

Wu922 ¶ [0021].

“Step 704: using the patterned sacrificial layer as an etching mask, etching the semiconductor substrate in the PMOS transistor region, and forming an epitaxial layer in the recess, preferably an epitaxial layer of silicon germanium[.]”

Wu922 ¶ [0031].

Exemplary Disclosures

“Please refer to FIG. 12 in company with FIG. 11. The second patterned photoresist 54 is removed. A selective epitaxial growth process is performed to form an epitaxial layer, such as an epitaxial layer 58 of silicon germanium. The preferred epitaxial layer 58 has a lattice constant greater than that of the semiconductor substrate 30, and is extended approaching to the channel. In order to compress the channel and to keep the silicon layer formed in the following steps from the interface between the source/drain in a distance, the preferred epitaxial layer 58 is slightly projected from the top surface of the semiconductor substrate 30. The top surface of the epitaxial layer 58 may be substantially leveled with or lower than the top surface of semiconductor substrate 30.”

Wu922 ¶ [0041].

“Step 804: using the patterned sacrificial layer as an etching mask, etching the semiconductor substrate beside the gate structure in the PMOS transistor region, and forming an epitaxial layer in the recess, i.e. an epitaxial layer of silicon germanium[.]”

Wu922 ¶ [0050].

Alternatively, under Plaintiff’s apparent interpretation of the claim language, the claimed “silicon compound layer” may include a silicide film. *See* AICP’s P.R. 3-1 Disclosures, Ex. H, at 15, 20, 21, 25, 26, 31. Although TSMC disagrees with such an interpretation, Wu922 further discloses [1i] under this interpretation, as shown below.

“Please refer to FIG. 1 to FIG. 7, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a first preferred embodiment of the present invention. Referring to FIG. 1, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the first preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. The following diagrams shows a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 for illustration. A plurality of isolation structures between the MOS transistors to prevent short circuiting, such as shallow trench isolations 38 formed between the PMOS transistor region 31 and the NMOS transistor region 33. Each of the gate structure 36A, 36B includes a gate dielectric layer 40, a gate 42, and a cap layer 44. The gate dielectric layer 40 may comprise dielectric materials including silicon oxide, oxynitride, and silicon nitride; high-k dielectric materials including metal oxide, metal silicate, metal aluminate, and metal oxynitride; or combinations thereof. The gate dielectric layer 40 may be formed by a thermal oxidation process, a nitridation process, or a chemical vapor deposition (CVD) process. The gate 42 may use polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof as material. The material of the cap layer 44 may include silicon oxide, oxynitride, silicon nitride, or silicon carbide (SiC). A thermal oxidation process is performed to

Exemplary Disclosures

form an oxide layer 501A, 501B on sidewalls of the gate structures 36A, 36B for protecting the gate structures 36A, 36B.”

Wu922 ¶ [0017].

“As shown in FIG. 7, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. The processes of forming the second spacers are the same as those processes for forming the first spacers 502A, 502B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source/drain 64B in the NMOS transistor region 33. The processes of forming the source/drain 64A, 64B are well known, and will not be described in detail. In addition, a self-aligned silicide process (salicide process) is optionally performed. A metal layer, including titanium (Ti), cobalt (Co), nickel (Ni), palladium (Pd), platinum (Pt) or the like, is deposited. And a rapid thermal process is performed to form a silicide layer (not shown) on the surfaces of the source/drain 64A, 64B.”

Wu922 ¶ [0024].

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”

Wu922 ¶ [0036].

“As shown in FIG. 14, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source drain 64B in the NMOS transistor region 33. In addition, a self-aligned silicide process is optionally performed to form a silicide layer (not shown) on the surfaces of the gate structures or the source/drain.” Wu922 ¶ [0043].

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.” Wu922 ¶ [0055].

See also, e.g., Wu922 FIGS. 4-5, 12-13.

To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.

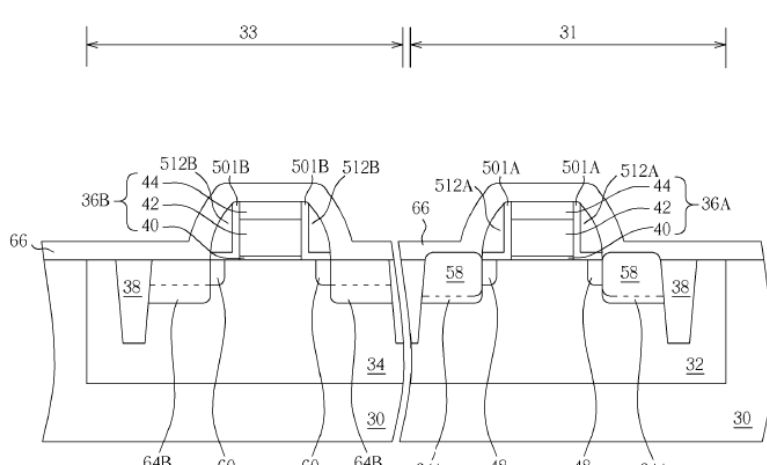
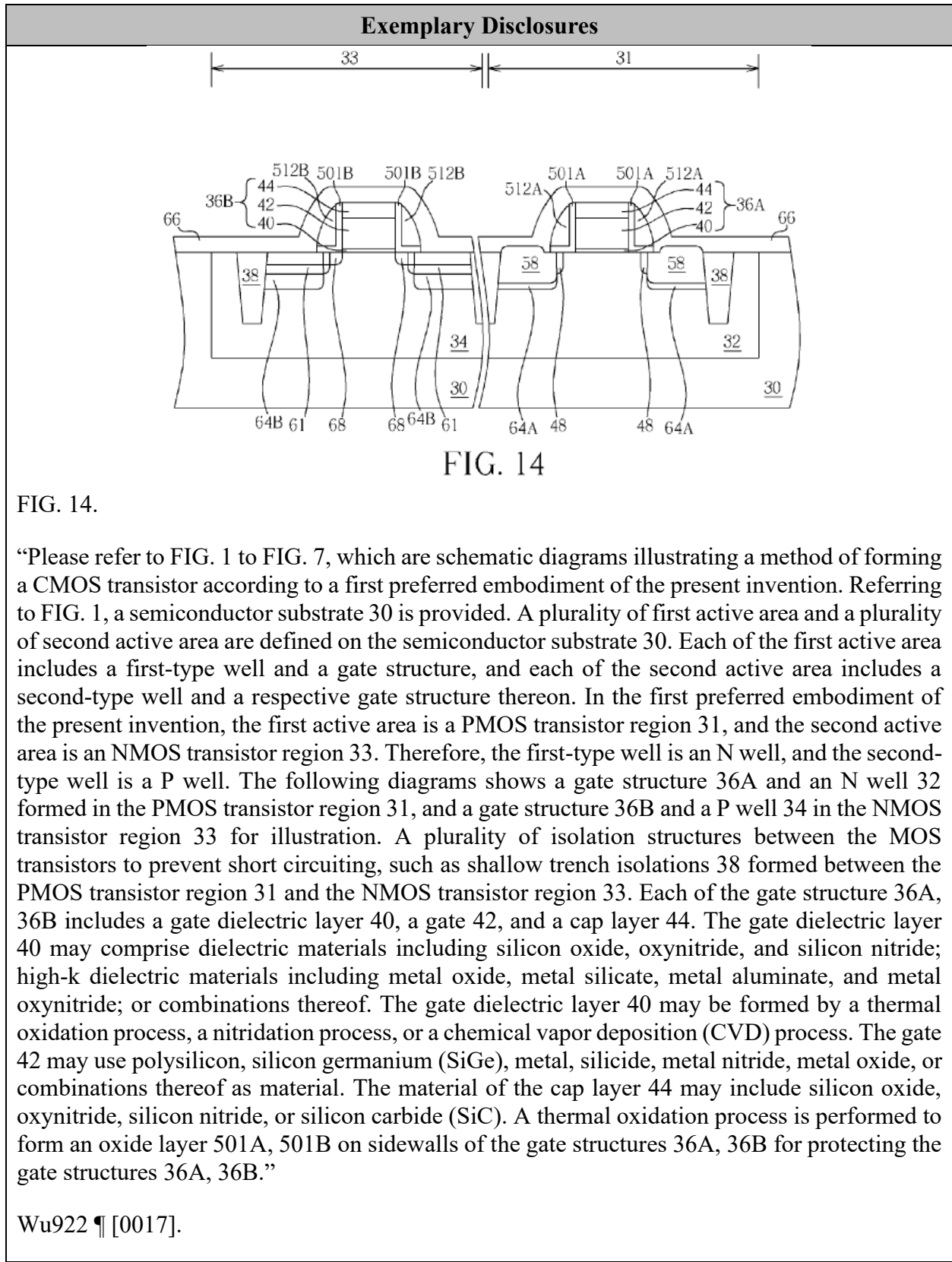
Exemplary Disclosures
1[j] a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer,
To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.
1[k] the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween, and
To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.
1[l] the first stress-relief film is not in direct contact with the side surface of the first gate electrode.
To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.
3[a] The semiconductor device of claim 1, further comprising: a first silicide layer formed on the first gate electrode; and
Wu922 discloses this feature. For example, Wu922 discloses that a self-aligned silicide process (silicide process) may be used to form a silicide layer on PMOS gate electrode 42. <i>See, e.g.</i>, the following:  FIG. 7

FIG. 7.



Exemplary Disclosures

“As shown in FIG. 7, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. The processes of forming the second spacers are the same as those processes for forming the first spacers 502A, 502B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source/drain 64B in the NMOS transistor region 33. The processes of forming the source/drain 64A, 64B are well known, and will not be described in detail. In addition, a self-aligned silicide process (salicide process) is optionally performed. A metal layer, including titanium (Ti), cobalt (Co), nickel (Ni), palladium (Pd), platinum (Pt) or the like, is deposited. And a rapid thermal process is performed to form a silicide layer (not shown) on the surfaces of the source/drain 64A, 64B.”

Wu922 ¶ [0024].

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”

Wu922 ¶ [0036].

“As shown in FIG. 14, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source drain 64B in the NMOS transistor region 33. In addition, a self-aligned silicide process is optionally performed to form a silicide layer (not shown) on the surfaces of the gate structures or the source/drain.”

Wu922 ¶ [0043].

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”

Wu922 ¶ [0055].

Under AICP’s understanding of 1[c]—whereby the gate silicide can be part of the gate electrode itself—the silicide cannot be “formed on” the gate electrode, as claimed. If such an illogical interpretation is permitted, however, this reference would additionally satisfy 3[a] under the alternative mapping of 1[c].

To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.

Exemplary Disclosures

3[b] a second silicide layer formed on the first source/drain region which includes the silicon compound layer.

Wu922 discloses this feature. For example, Wu922 discloses that a self-aligned silicide process (silicide process) may be used to form a silicide layer on PMOS epitaxial SiGe layers 58, which includes SiGe. *See, e.g.*, the following:

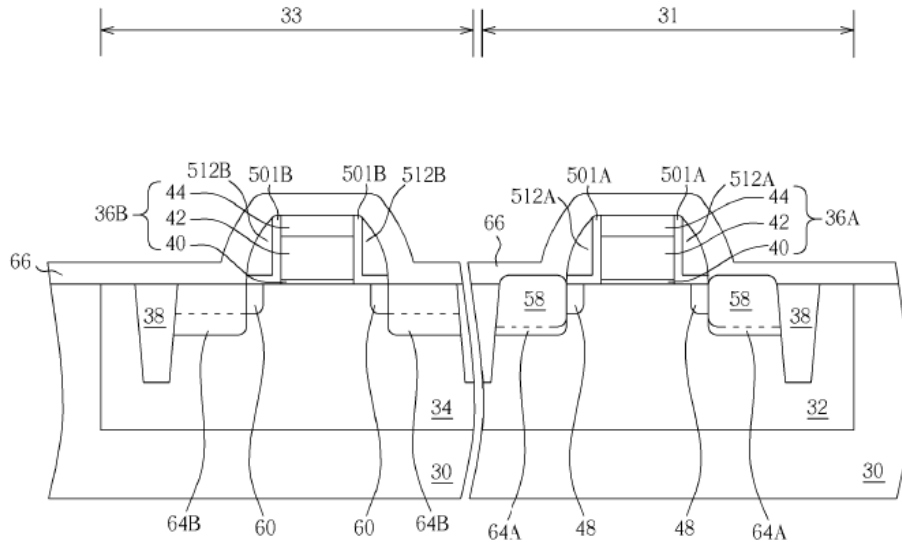


FIG. 7

FIG. 7.

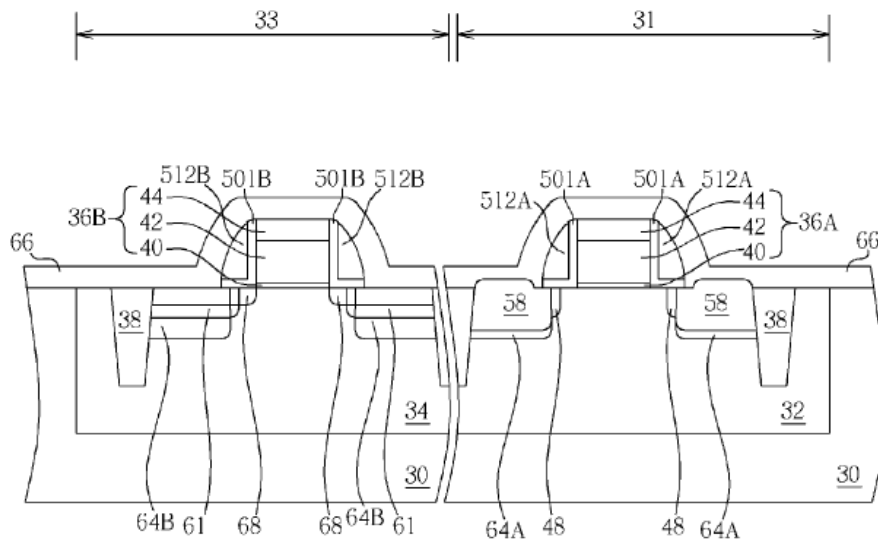


FIG. 14

FIG. 14.

Exemplary Disclosures

“Please refer to FIG. 1 to FIG. 7, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a first preferred embodiment of the present invention. Referring to FIG. 1, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the first preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. The following diagrams shows a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 for illustration. A plurality of isolation structures between the MOS transistors to prevent short circuiting, such as shallow trench isolations 38 formed between the PMOS transistor region 31 and the NMOS transistor region 33. Each of the gate structure 36A, 36B includes a gate dielectric layer 40, a gate 42, and a cap layer 44. The gate dielectric layer 40 may comprise dielectric materials including silicon oxide, oxynitride, and silicon nitride; high-k dielectric materials including metal oxide, metal silicate, metal aluminate, and metal oxynitride; or combinations thereof. The gate dielectric layer 40 may be formed by a thermal oxidation process, a nitridation process, or a chemical vapor deposition (CVD) process. The gate 42 may use polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof as material. The material of the cap layer 44 may include silicon oxide, oxynitride, silicon nitride, or silicon carbide (SiC). A thermal oxidation process is performed to form an oxide layer 501A, 501B on sidewalls of the gate structures 36A, 36B for protecting the gate structures 36A, 36B.”

Wu922 ¶ [0017].

“As shown in FIG. 7, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. The processes of forming the second spacers are the same as those processes for forming the first spacers 502A, 502B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source/drain 64B in the NMOS transistor region 33. The processes of forming the source/drain 64A, 64B are well known, and will not be described in detail. In addition, a self-aligned silicide process (salicide process) is optionally performed. A metal layer, including titanium (Ti), cobalt (Co), nickel (Ni), palladium (Pd), platinum (Pt) or the like, is deposited. And a rapid thermal process is performed to form a silicide layer (not shown) on the surfaces of the source/drain 64A, 64B.”

Wu922 ¶ [0024].

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.” Wu922 ¶ [0036].

Exemplary Disclosures
“As shown in FIG. 14, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source drain 64B in the NMOS transistor region 33. In addition, a self-aligned silicide process is optionally performed to form a silicide layer (not shown) on the surfaces of the gate structures or the source/drain.” Wu922 ¶ [0043]. “Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.” Wu922 ¶ [0055]. Under AICP’s understanding of 1[f]—whereby the source/drain silicide can be part of the silicon compound layer, which is itself part of the source/drain region—the silicide cannot be “formed on” the source/drain region, as claimed. If such an illogical interpretation is permitted, however, this reference would additionally satisfy 3[b] under the alternative mapping of 1[f]. To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.
4[a] The semiconductor device of claim 1, wherein the first stress-relief film is formed on a side surface of the silicon compound layer.
To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.
5[a] The semiconductor device of claim 1, wherein the first sidewall spacer includes an inner sidewall spacer which is formed on the side surface of the first gate electrode, and whose cross-section has an L shape, and an outer sidewall spacer formed on the inner sidewall spacer.
If the claimed “first sidewall spacer” need not exist when the source/drain regions are formed (<i>see supra</i> 1[e]), then Wu922 discloses this feature. For example, Wu922 discloses inner sidewall L-shaped spacers 501A, which are formed on the side surface of PMOS gate electrode 42 and have an L-shaped cross-section, and outer sidewall spacers 512A formed on the inner sidewall spacers 501A. <i>See, e.g.</i>, the following:

Exemplary Disclosures

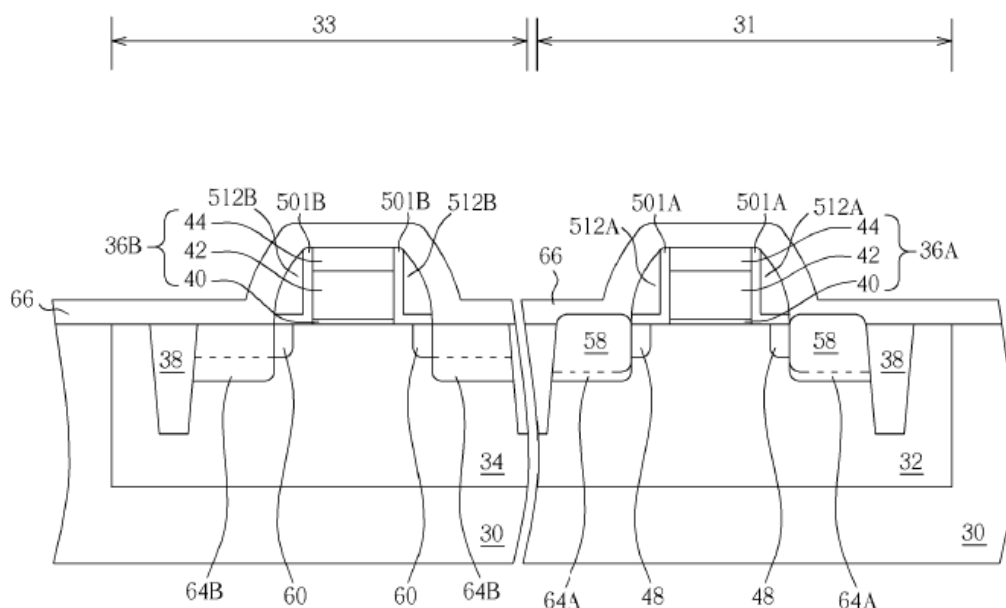


FIG. 7

FIG. 7.

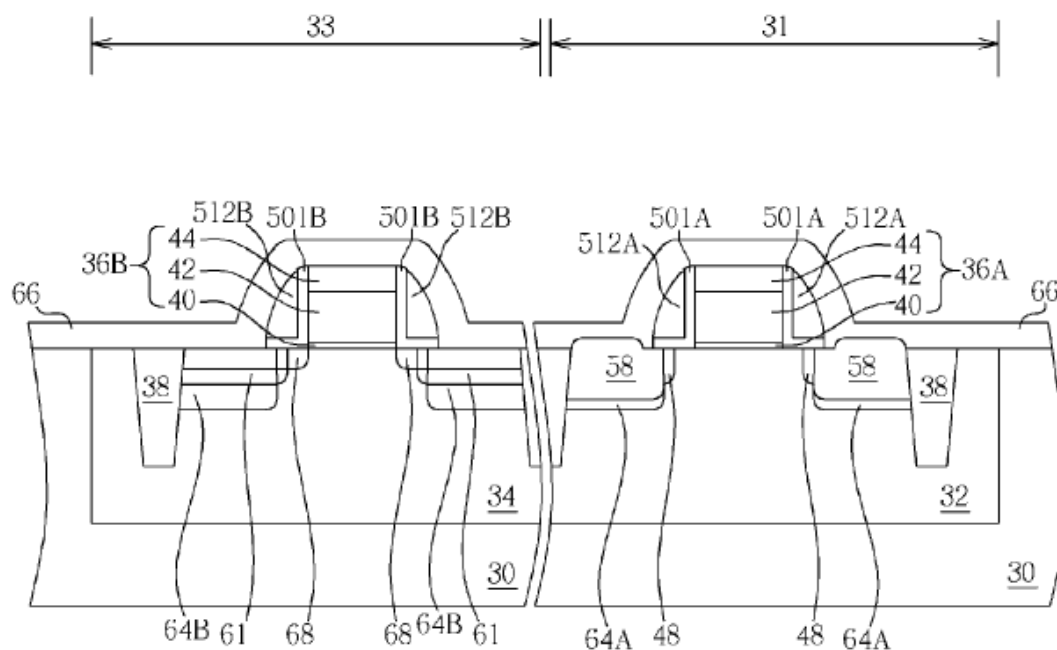


FIG. 14

FIG. 14.

Exemplary Disclosures

“Please refer to FIG. 1 to FIG. 7, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a first preferred embodiment of the present invention. Referring to FIG. 1, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the first preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. The following diagrams shows a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 for illustration. A plurality of isolation structures between the MOS transistors to prevent short circuiting, such as shallow trench isolations 38 formed between the PMOS transistor region 31 and the NMOS transistor region 33. Each of the gate structure 36A, 36B includes a gate dielectric layer 40, a gate 42, and a cap layer 44. The gate dielectric layer 40 may comprise dielectric materials including silicon oxide, oxynitride, and silicon nitride; high-k dielectric materials including metal oxide, metal silicate, metal aluminate, and metal oxynitride; or combinations thereof. The gate dielectric layer 40 may be formed by a thermal oxidation process, a nitridation process, or a chemical vapor deposition (CVD) process. The gate 42 may use polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof as material. The material of the cap layer 44 may include silicon oxide, oxynitride, silicon nitride, or silicon carbide (SiC). A thermal oxidation process is performed to form an oxide layer 501A, 501B on sidewalls of the gate structures 36A, 36B for protecting the gate structures 36A, 36B.”

Wu922 ¶ [0017].

“As shown in FIG. 7, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. The processes of forming the second spacers are the same as those processes for forming the first spacers 502A, 502B.”

Wu922 ¶ [0024].

“As shown in FIG. 1, a spacer formation process is optionally performed to form at least a first spacer 502A, 502B respectively beside the thermal oxide layers 501A, 501B. The preferred first spacers 502A, 502B may be a single-layered structure or a multi-layered structure. The preferred material of the first spacers 502A, 502B may use silicon oxide, silicon nitride, oxynitride, or other adoptable dielectric material. The first spacers 502A, 502B are formed by a plasma enhanced chemical vapor deposition (PECVD) process, a low-pressure chemical vapor deposition process (LPCVD), or other method for depositing the material layers of the first spacers 502A, 502B. Subsequently, an etch back process is performed to etch the material layers of the first spacers 502A, 502B.”

Wu922 ¶ [0018].

Exemplary Disclosures

“Step 701: forming at least a thermal oxide layer on the sidewalls of the gate structures[.]”

Wu922 ¶ [0028].

“Please refer to FIG. 9 to FIG. 14, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a second preferred embodiment of the present invention. Some elements are the same as those of the first preferred embodiment and are numbered as those of the first preferred embodiment. Referring to FIG. 9, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the second preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. For the simplicity of description, a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 are shown in the diagram in the following.”

Wu922 ¶ [0038].

“As shown in FIG. 9, a thermal oxidation process to form a thermal oxide layer 501A, 501B respectively formed on the sidewalls of the gate structures 36A, 36B, and a spacer formation process is performed to form at least a first spacer 502A, 502B respectively formed beside the thermal oxide layers 501A, 501B.”

Wu922 ¶ [0039].

“As shown in FIG. 14, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B.”

Wu922 ¶ [0043].

See also, e.g., Wu922 ¶¶ [0017]-[0018], ¶¶ [0022]-[0025], ¶ [0028], ¶ [0034], ¶¶ [0037]-[0039], ¶¶ [0042]-[0044], ¶ [0047], ¶ [0053], ¶¶ [0057]-[0058], FIGS. 1-4, 7-12, 14, 15.

To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.

Exemplary Disclosures

7[a] The semiconductor device of claim 1, wherein the first MIS transistor is a p-type MIS transistor,

Wu922 discloses this feature. For example, Wu922 discloses a PMOS transistor. *See, e.g.*, the following:

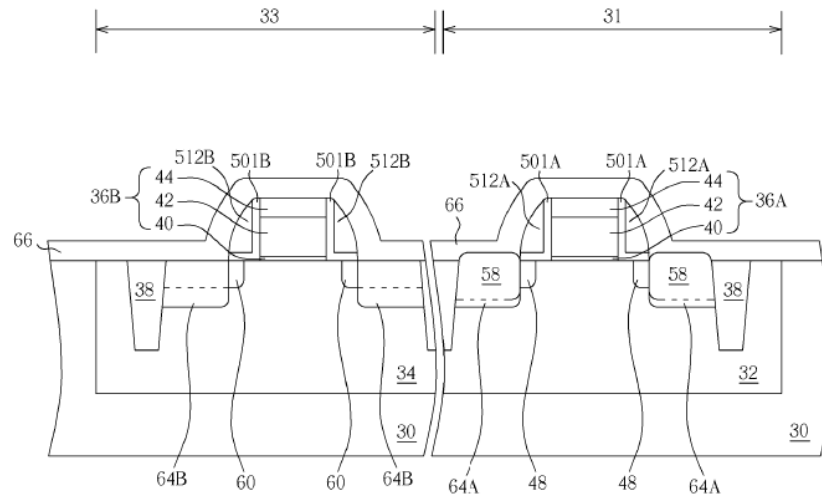


FIG. 7

FIG. 7.

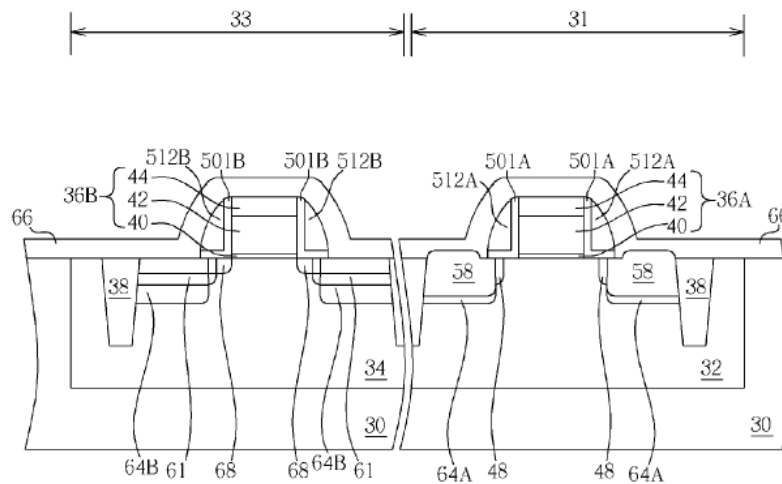


FIG. 14

FIG. 14.

“A method of forming CMOS transistor is disclosed. A CMOS transistor having a first active area and a second active area is provided.”

Wu922, at Abstract.

Exemplary Disclosures

“Please refer to FIG. 1 to FIG. 7, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a first preferred embodiment of the present invention. Referring to FIG. 1, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the first preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. The following diagrams shows a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 for illustration. A plurality of isolation structures between the MOS transistors to prevent short circuiting, such as shallow trench isolations 38 formed between the PMOS transistor region 31 and the NMOS transistor region 33. Each of the gate structure 36A, 36B includes a gate dielectric layer 40, a gate 42, and a cap layer 44. The gate dielectric layer 40 may comprise dielectric materials including silicon oxide, oxynitride, and silicon nitride; high-k dielectric materials including metal oxide, metal silicate, metal aluminate, and metal oxynitride; or combinations thereof. The gate dielectric layer 40 may be formed by a thermal oxidation process, a nitridation process, or a chemical vapor deposition (CVD) process. The gate 42 may use polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof as material. The material of the cap layer 44 may include silicon oxide, oxynitride, silicon nitride, or silicon carbide (SiC). A thermal oxidation process is performed to form an oxide layer 501A, 501B on sidewalls of the gate structures 36A, 36B for protecting the gate structures 36A, 36B.”

Wu922 ¶ [0017].

“Please refer to FIG. 4 in company with FIG. 3. The second patterned photoresist 54 is removed. A selective epitaxial growth process is performed to form an epitaxial layer, such as an epitaxial layer 58 of silicon germanium. The preferred epitaxial layer 58 has a lattice constant greater than that of the semiconductor substrate 30, and is slightly extended approaching to the channel. Preferably, the epitaxial layer 58 is slightly projected from the top surface of the semiconductor substrate 30 to compress the channel and to keep silicon layers formed in the following steps from the interface between the source/drain in a distance. The top surface of the epitaxial layer 58 may be substantially leveled with or lower than the top surface of semiconductor substrate 30.”

Wu922 ¶ [0021].

“Please refer to FIG. 8, which shows a flow diagram illustrating a method of forming a CMOS transistor in accordance with the first preferred embodiment of the present embodiment.”

Wu922 ¶ [0026].

Exemplary Disclosures
“Step 700: providing a semiconductor substrate having a PMOS transistor, a NMOS transistor, and a plurality of gate structures formed in the PMOS transistor and the NMOS transistor[.]” Wu922 ¶ [0027]. “Step 704: using the patterned sacrificial layer as an etching mask, etching the semiconductor substrate in the PMOS transistor region, and forming an epitaxial layer in the recess, preferably an epitaxial layer of silicon germanium[.]” Wu922 ¶ [0031]. “Moreover, the first preferred embodiment is illustrated using a PMOS transistor as the first active area, and an NMOS transistor as the second active area.” Wu922 ¶ [0037]. “Please refer to FIG. 9 to FIG. 14, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a second preferred embodiment of the present invention. Some elements are the same as those of the first preferred embodiment and are numbered as those of the first preferred embodiment. Referring to FIG. 9, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the second preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. For the simplicity of description, a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 are shown in the diagram in the following.” Wu922 ¶ [0038]. “Please refer to FIG. 12 in company with FIG. 11. The second patterned photoresist 54 is removed. A selective epitaxial growth process is performed to form an epitaxial layer, such as an epitaxial layer 58 of silicon germanium. The preferred epitaxial layer 58 has a lattice constant greater than that of the semiconductor substrate 30, and is extended approaching to the channel. In order to compress the channel and to keep the silicon layer formed in the following steps from the interface between the source/drain in a distance, the preferred epitaxial layer 58 is slightly projected from the top surface of the semiconductor substrate 30. The top surface of the epitaxial layer 58 may be substantially leveled with or lower than the top surface of semiconductor substrate 30.” Wu922 ¶ [0041].

Exemplary Disclosures
“FIG. 15 is a flow diagram illustrating a method of forming a CMOS transistor in accordance with the second preferred embodiment of the present embodiment.” Wu922 ¶ [0045]. “Step 800: providing a semiconductor substrate having a PMOS transistor, a NMOS transistor, and a plurality of gate structures formed in the PMOS transistor and the NMOS transistor[.]” Wu922 ¶ [0046]. “Step 804: using the patterned sacrificial layer as an etching mask, etching the semiconductor substrate beside the gate structure in the PMOS transistor region, and forming an epitaxial layer in the recess, i.e. an epitaxial layer of silicon germanium[.]” Wu922 ¶ [0050]. “Moreover, the first preferred embodiment is illustrated using a PMOS transistor as the first active area, and an NMOS transistor as the second active area.” Wu922 ¶ [0057]. To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.
7[b] the first stress is a compressive stress, and
Wu922 discloses this feature. For example, Wu922 discloses PMOS epitaxial SiGe layers 58 cause compressive stress. <i>See, e.g.</i>, the following: “In order to increase the driving current of a complementary metal-oxide semiconductor (CMOS) transistor including a p-type MOS (PMOS) transistor and an n-type MOS (NMOS) transistor, the industrial circles develop a strained-silicon technique, which uses unique processes or lattice constant discrepancy to increase driving current. The strained-silicon technique substantially includes a substrate strained based method and a process-induced strain based method. The substrate-strained based system is performed with a strained-silicon substrate or a selective epitaxial growth process that results in lattice constant discrepancy. The process-induced strain based method is performed with several unique processes to form a strained thin film upon a surface of the MOS transistor that exert tensile stress or compressive stress upon the MOS transistor. Both of the strained silicon techniques introduce strain into the channel region and reduce carrier mobile resistance thereby improving carrier mobility and MOS transistor performance.” Wu922 ¶ [0005].

Exemplary Disclosures

“The primary objective of the present invention is to provide a method of forming a strained CMOS transistor to improve CMOS transistor performance and reliability and to overcome the drawback of conventional techniques. Initially, a semiconductor substrate having at least a first active area and at least a second active area is provided. The first active area and the second active area include a respective gate structure. A first light doped drain is formed beside the gate structure in the first active area. A sacrificial layer is formed on the semiconductor substrate. An etch process is performed to etch the sacrificial layer and a surface of the semiconductor substrate beside the gate structure in the first active area to form a recess on a surface of the semiconductor substrate beside the gate structure of the first active area. A selective epitaxial process is performed to form an epitaxial layer in the recess. After that, the sacrificial layer is removed, and a second light doped drain is formed beside gate structure in the second active area.”

Wu922 ¶ [0009].

“Please refer to FIG. 4 in company with FIG. 3. The second patterned photoresist 54 is removed. A selective epitaxial growth process is performed to form an epitaxial layer, such as an epitaxial layer 58 of silicon germanium. The preferred epitaxial layer 58 has a lattice constant greater than that of the semiconductor substrate 30, and is slightly extended approaching to the channel. Preferably, the epitaxial layer 58 is slightly projected from the top surface of the semiconductor substrate 30 to compress the channel and to keep silicon layers formed in the following steps from the interface between the source/drain in a distance. The top surface of the epitaxial layer 58 may be substantially leveled with or lower than the top surface of semiconductor substrate 30.”

Wu922 ¶ [0021].

“Step 704: using the patterned sacrificial layer as an etching mask, etching the semiconductor substrate in the PMOS transistor region, and forming an epitaxial layer in the recess, preferably an epitaxial layer of silicon germanium[.]”

Wu922 ¶ [0031].

“Please refer to FIG. 12 in company with FIG. 11. The second patterned photoresist 54 is removed. A selective epitaxial growth process is performed to form an epitaxial layer, such as an epitaxial layer 58 of silicon germanium. The preferred epitaxial layer 58 has a lattice constant greater than that of the semiconductor substrate 30, and is extended approaching to the channel. In order to compress the channel and to keep the silicon layer formed in the following steps from the interface between the source/drain in a distance, the preferred epitaxial layer 58 is slightly projected from the top surface of the semiconductor substrate 30. The top surface of the epitaxial layer 58 may be substantially leveled with or lower than the top surface of semiconductor substrate 30.”

Wu922 ¶ [0041].

Exemplary Disclosures
“Step 804: using the patterned sacrificial layer as an etching mask, etching the semiconductor substrate beside the gate structure in the PMOS transistor region, and forming an epitaxial layer in the recess, i.e. an epitaxial layer of silicon germanium[.]” Wu922 ¶ [0050]. To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.
7[c] the second stress is a tensile stress.
Wu922 discloses this feature. For example, Wu922 discloses that CESL 66 may cause a tensile stress. <i>See, e.g.</i>, the following: “In order to increase the driving current of a complementary metal-oxide semiconductor (CMOS) transistor including a p-type MOS (PMOS) transistor and an n-type MOS (NMOS) transistor, the industrial circles develop a strained-silicon technique, which uses unique processes or lattice constant discrepancy to increase driving current. The strained-silicon technique substantially includes a substrate strained based method and a process-induced strain based method. The substrate-strained based system is performed with a strained-silicon substrate or a selective epitaxial growth process that results in lattice constant discrepancy. The process-induced strain based method is performed with several unique processes to form a strained thin film upon a surface of the MOS transistor that exert tensile stress or compressive stress upon the MOS transistor. Both of the strained silicon techniques introduce strain into the channel region and reduce carrier mobile resistance thereby improving carrier mobility and MOS transistor performance.” Wu922 ¶ [0005]. “A deposition process is performed to form a contact etch stop layer (CESL) 66 on the surface of the gate structures 36A, 36B, the second spacers 512A, 512B, and the sources/drains 64A, 64B. The material of the CESL 66 may include a dielectric material or a strained silicon material, i.e. silicon nitride.” Wu922 ¶ [0025]. “Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.” Wu922 ¶ [0036].

Exemplary Disclosures

“A deposition process is performed to form a CESL 66 on the surface of the gate structures 36A, 36B, the second spacers 512A, 512B, and the sources/drains 64A, 64B.”

Wu922 ¶ [0044].

To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.

11[a] The semiconductor device of claim 1, further comprising: a second MIS transistor, wherein: the second MIS transistor includes:

Wu922 discloses this feature. For example, Wu922 discloses an NMOS transistor. *See, e.g.*, the following:

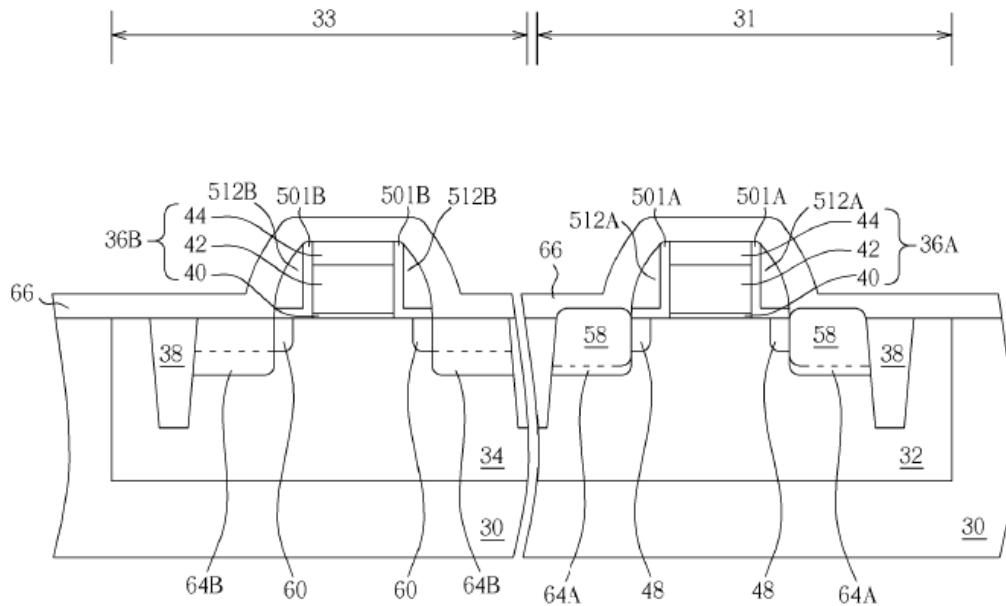


FIG. 7

FIG. 7.

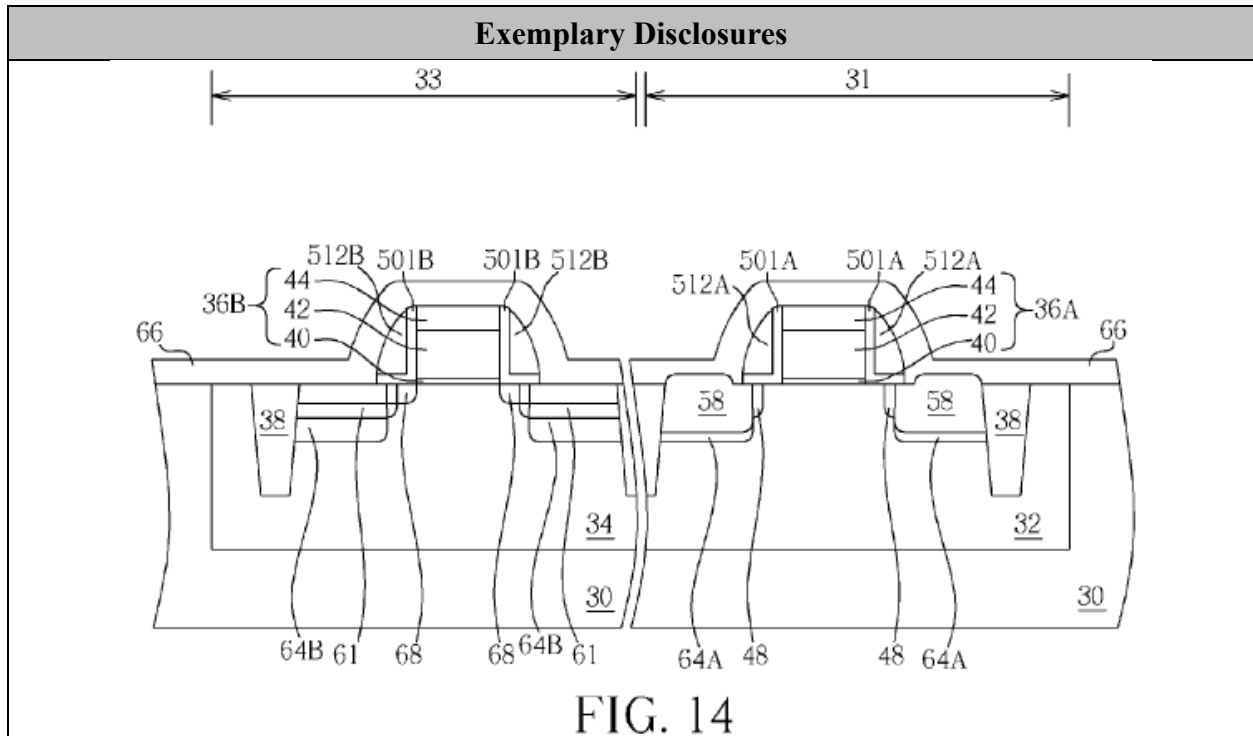


FIG. 14.

“A method of forming CMOS transistor is disclosed. A CMOS transistor having a first active area and a second active area is provided.”

Wu922 Abstract.

“The present invention is related to a method of forming a CMOS transistor.”

Wu922 ¶ [0002].

“Please refer to FIG. 1 to FIG. 7, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a first preferred embodiment of the present invention. Referring to FIG. 1, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the first preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. The following diagrams shows a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 for illustration. A plurality of isolation structures between the MOS transistors to prevent short circuiting, such as shallow trench isolations 38 formed between the PMOS transistor region 31 and the NMOS transistor region 33. Each of the gate structure 36A, 36B includes a gate dielectric layer 40, a gate 42, and a cap layer 44. The gate dielectric layer

Exemplary Disclosures

40 may comprise dielectric materials including silicon oxide, oxynitride, and silicon nitride; high-k dielectric materials including metal oxide, metal silicate, metal aluminate, and metal oxynitride; or combinations thereof. The gate dielectric layer 40 may be formed by a thermal oxidation process, a nitridation process, or a chemical vapor deposition (CVD) process. The gate 42 may use polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof as material. The material of the cap layer 44 may include silicon oxide, oxynitride, silicon nitride, or silicon carbide (SiC). A thermal oxidation process is performed to form an oxide layer 501A, 501B on sidewalls of the gate structures 36A, 36B for protecting the gate structures 36A, 36B.”

Wu922 ¶ [0017].

“As shown in FIG. 7, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. The processes of forming the second spacers are the same as those processes for forming the first spacers 502A, 502B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source/drain 64B in the NMOS transistor region 33. The processes of forming the source/drain 64A, 64B are well known, and will not be described in detail.”

Wu922 ¶ [0024].

“Step 700: providing a semiconductor substrate having a PMOS transistor, a NMOS transistor, and a plurality of gate structures formed in the PMOS transistor and the NMOS transistor[.]”

Wu922 ¶ [0027].

“Please refer to FIG. 9 to FIG. 14, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a second preferred embodiment of the present invention. Some elements are the same as those of the first preferred embodiment and are numbered as those of the first preferred embodiment. Referring to FIG. 9, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the second preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. For the simplicity of description, a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 are shown in the diagram in the following.”

Wu922 ¶ [0038].

Exemplary Disclosures

“Step 800: providing a semiconductor substrate having a PMOS transistor, a NMOS transistor, and a plurality of gate structures formed in the PMOS transistor and the NMOS transistor[.]”

Wu922 ¶ [0046].

To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.

11[b] a second gate insulating film formed on a second active region in the semiconductor substrate,

Wu922 discloses this feature. For example, Wu922 discloses an NMOS gate dielectric layer 40 formed on an NMOS active region of semiconductor substrate 30. *See, e.g.,* the following:

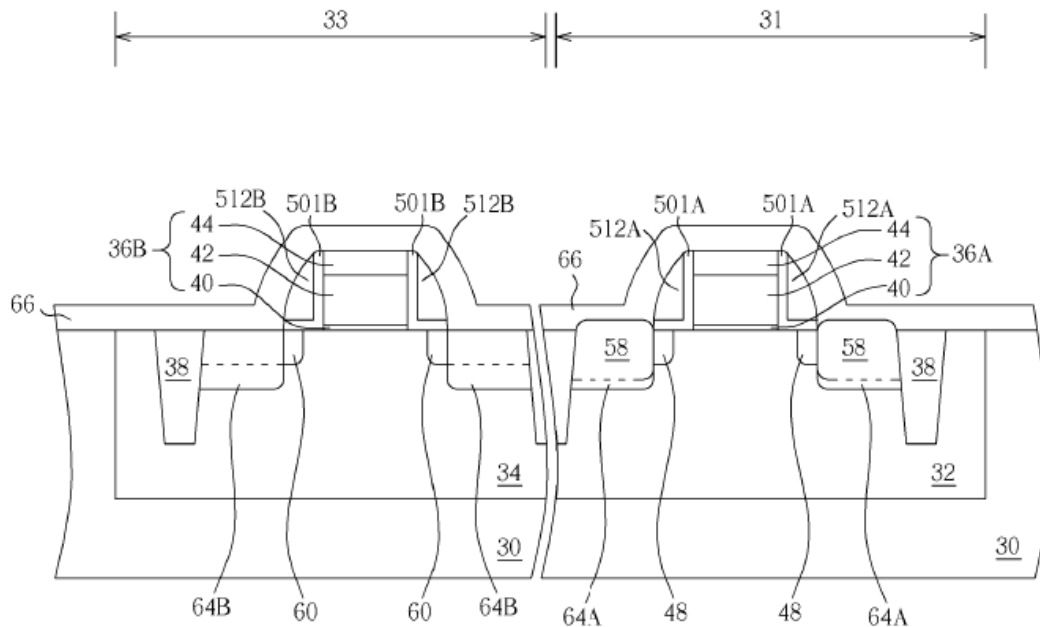
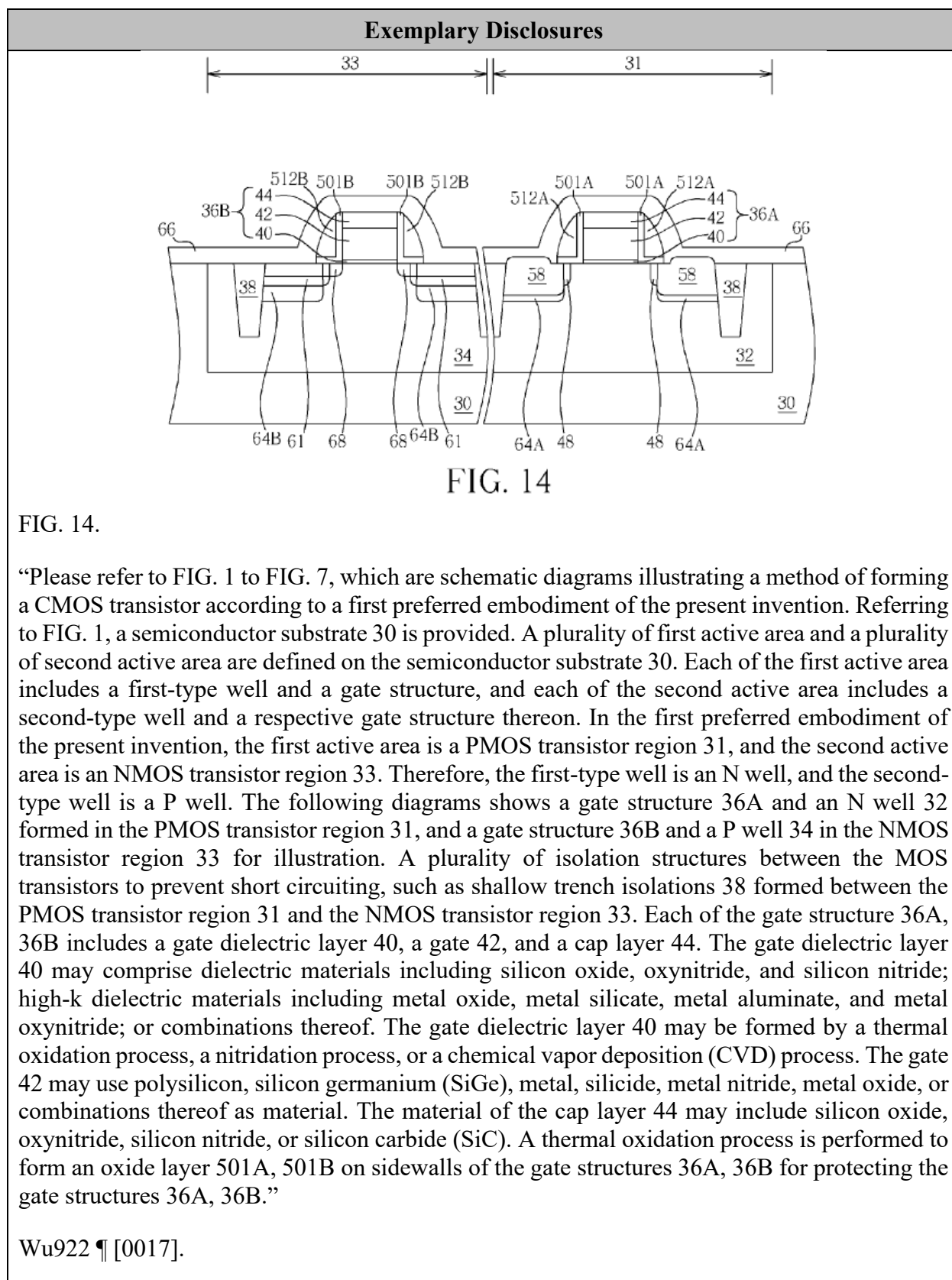


FIG. 7

FIG. 7.



Exemplary Disclosures

“Please refer to FIG. 9 to FIG. 14, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a second preferred embodiment of the present invention. Some elements are the same as those of the first preferred embodiment and are numbered as those of the first preferred embodiment. Referring to FIG. 9, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the second preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. For the simplicity of description, a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 are shown in the diagram in the following.”

Wu922 ¶ [0038].

To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.

11[c] a second gate electrode formed on the second gate insulating film,

Wu922 discloses this feature. For example, Wu922 discloses an NMOS gate electrode 42 formed on NMOS gate dielectric layer 40. *See, e.g.*, the following:

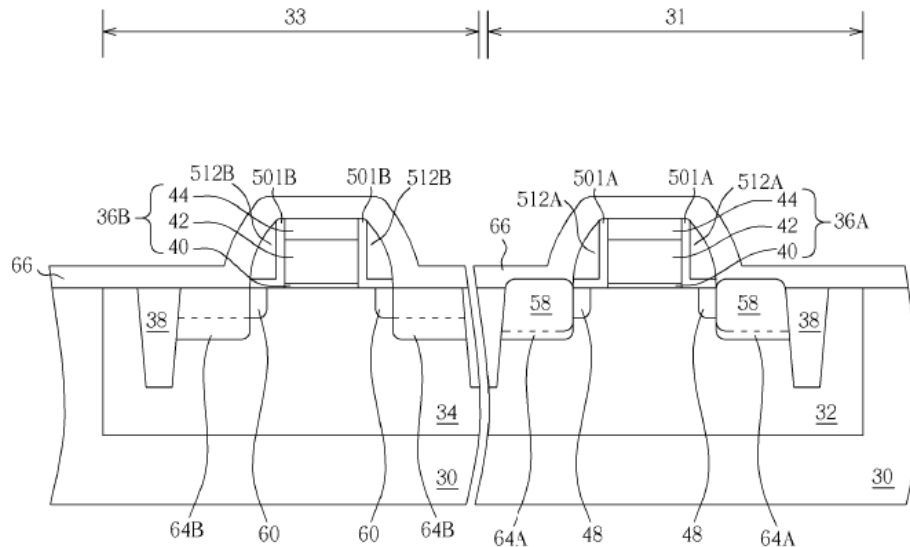
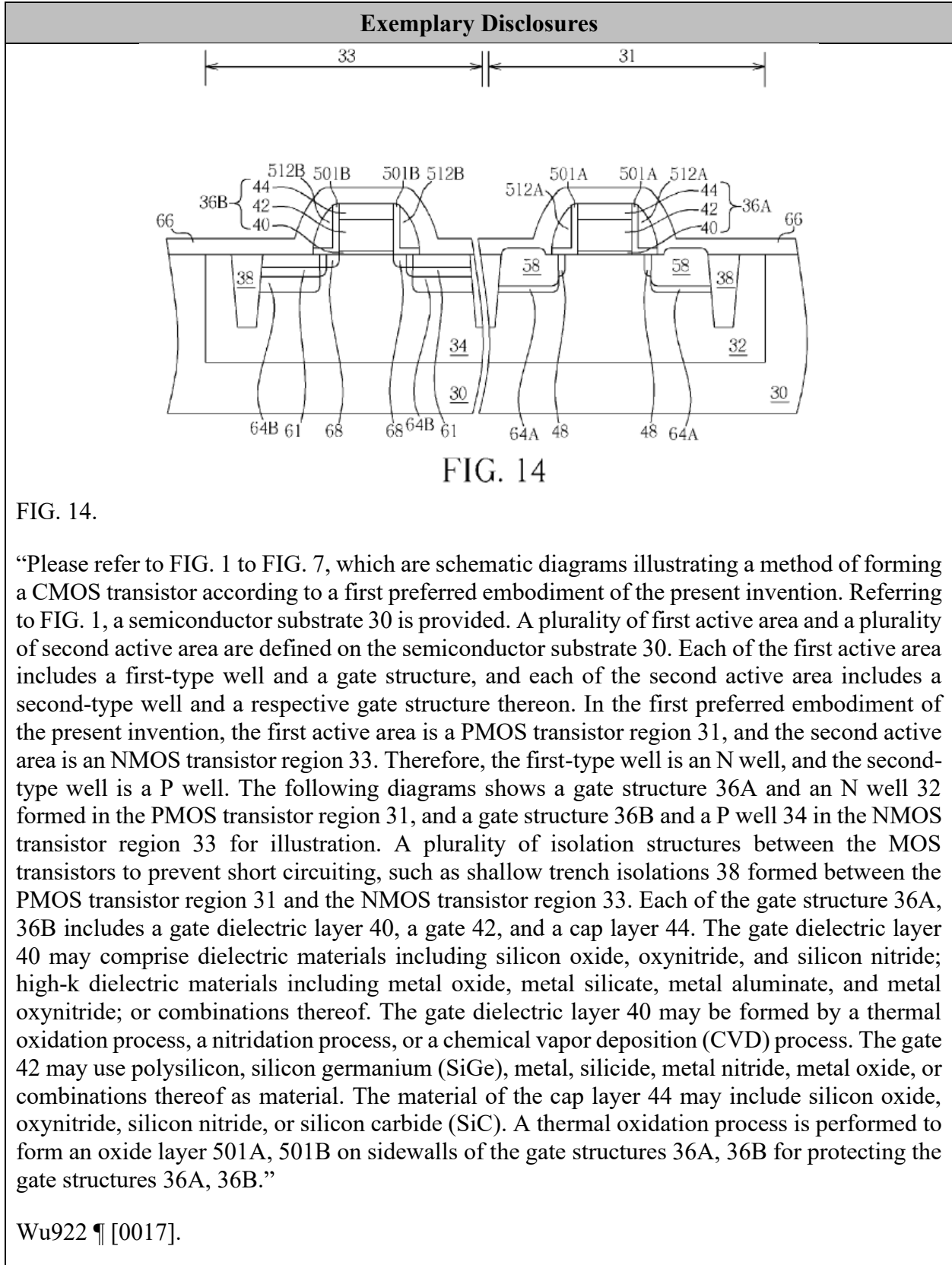


FIG. 7

FIG. 7.



Exemplary Disclosures

“Please refer to FIG. 9 to FIG. 14, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a second preferred embodiment of the present invention. Some elements are the same as those of the first preferred embodiment and are numbered as those of the first preferred embodiment. Referring to FIG. 9, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the second preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. For the simplicity of description, a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 are shown in the diagram in the following.”

Wu922 ¶ [0038].

See also, e.g., Wu922 ¶ [0039].

Additionally, under Plaintiff’s apparent interpretation of the claim language, the claimed “second gate electrode” may include a silicide film. See AICP’s P.R. 3-1 Disclosures, Ex. H, at 35-43. Although TSMC does not necessarily agree with such an interpretation, Wu922 further discloses this element under this interpretation, as shown below.

For example, Wu922 discloses silicide layer formed on NMOS gate electrode 42. See, e.g., the following:

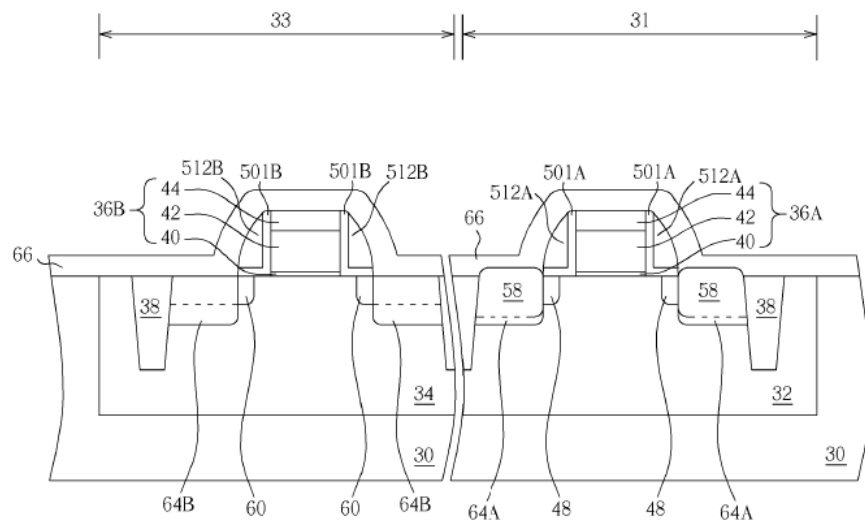
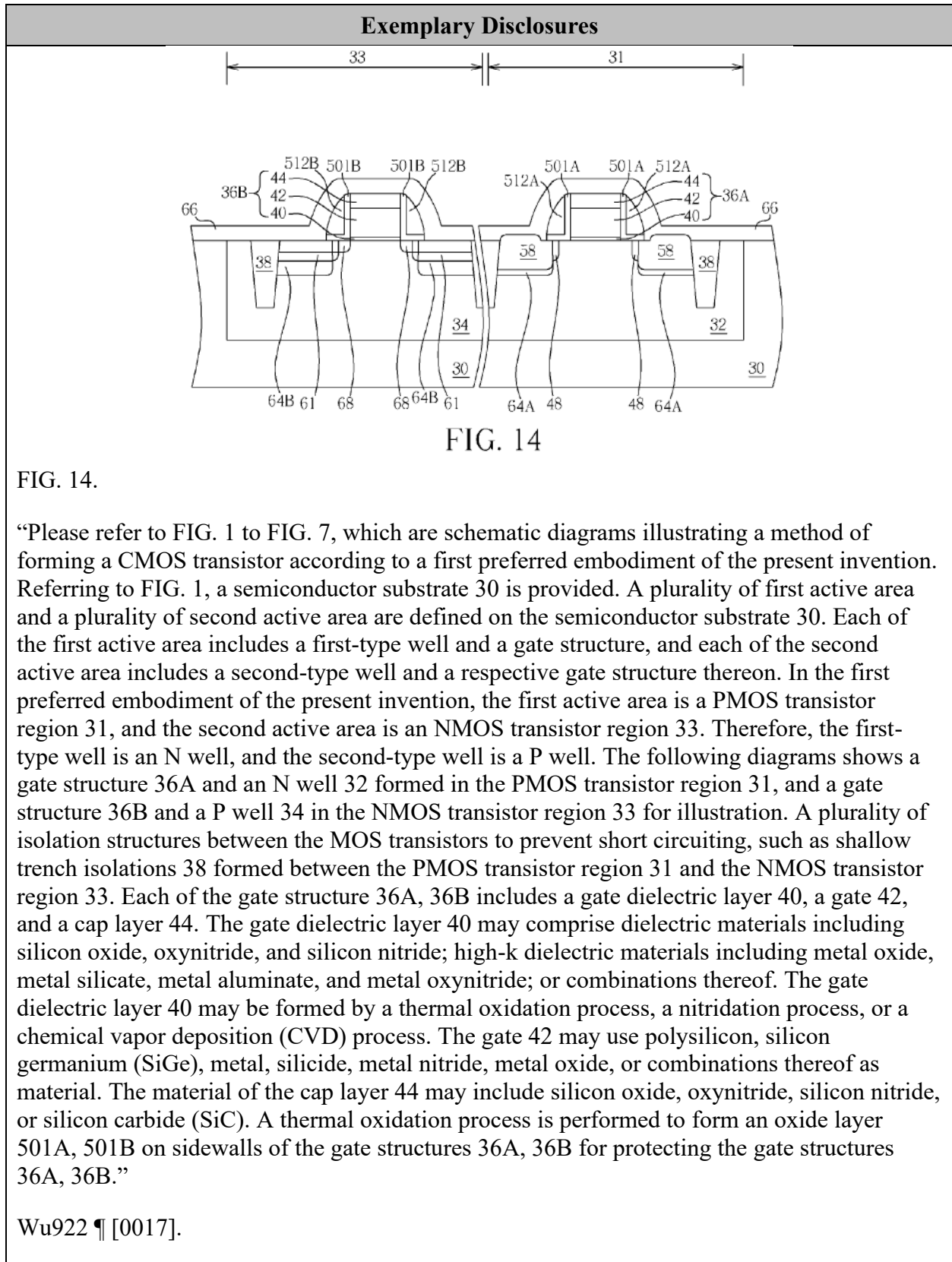


FIG. 7

FIG. 7.



Exemplary Disclosures

“As shown in FIG. 7, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. The processes of forming the second spacers are the same as those processes for forming the first spacers 502A, 502B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source/drain 64B in the NMOS transistor region 33. The processes of forming the source/drain 64A, 64B are well known, and will not be described in detail. In addition, a self-aligned silicide process (salicide process) is optionally performed. A metal layer, including titanium (Ti), cobalt (Co), nickel (Ni), palladium (Pd), platinum (Pt) or the like, is deposited. And a rapid thermal process is performed to form a silicide layer (not shown) on the surfaces of the source/drain 64A, 64B.”

Wu922 ¶ [0024].

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”

Wu922 ¶ [0036].

“As shown in FIG. 14, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source drain 64B in the NMOS transistor region 33. In addition, a self-aligned silicide process is optionally performed to form a silicide layer (not shown) on the surfaces of the gate structures or the source/drain.”

Wu922 ¶ [0043].

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”

Wu922 ¶ [0055].

To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.

Exemplary Disclosures

11[d] a second sidewall spacer formed on a side surface of the second gate electrode,

Wu922 discloses this feature. For example, Wu922 discloses L-shaped oxide spacers 501B and spacers 512B, each formed on a side surface of NMOS gate electrode 42. L-shaped spacers 501B and spacers 512B together constitute a second sidewall spacer. *See, e.g.*, the following:

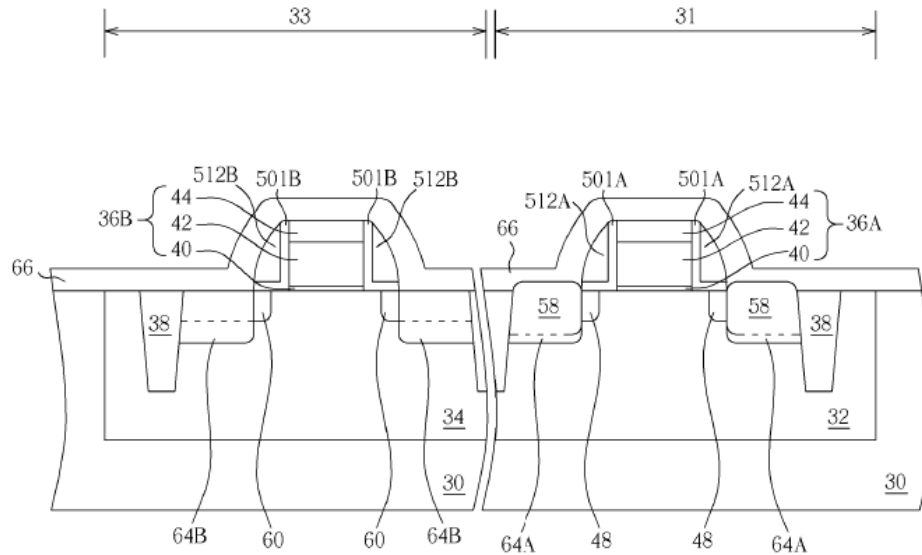


FIG. 7

FIG. 7.

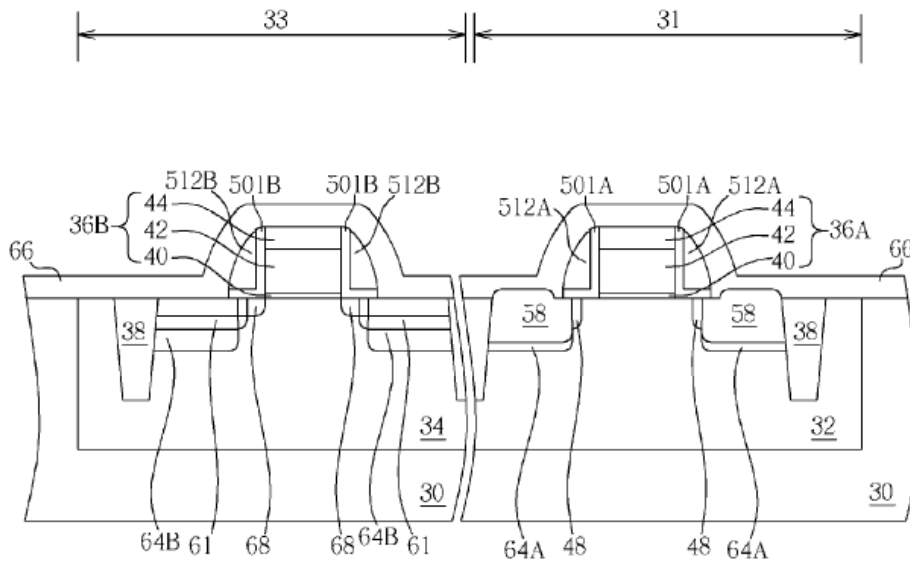


FIG. 14

FIG. 14.

Exemplary Disclosures

“Please refer to FIG. 1 to FIG. 7, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a first preferred embodiment of the present invention. Referring to FIG. 1, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the first preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. The following diagrams shows a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 for illustration. A plurality of isolation structures between the MOS transistors to prevent short circuiting, such as shallow trench isolations 38 formed between the PMOS transistor region 31 and the NMOS transistor region 33. Each of the gate structure 36A, 36B includes a gate dielectric layer 40, a gate 42, and a cap layer 44. The gate dielectric layer 40 may comprise dielectric materials including silicon oxide, oxynitride, and silicon nitride; high-k dielectric materials including metal oxide, metal silicate, metal aluminate, and metal oxynitride; or combinations thereof. The gate dielectric layer 40 may be formed by a thermal oxidation process, a nitridation process, or a chemical vapor deposition (CVD) process. The gate 42 may use polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof as material. The material of the cap layer 44 may include silicon oxide, oxynitride, silicon nitride, or silicon carbide (SiC). A thermal oxidation process is performed to form an oxide layer 501A, 501B on sidewalls of the gate structures 36A, 36B for protecting the gate structures 36A, 36B.”

Wu922 ¶ [0017].

“As shown in FIG. 7, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. The processes of forming the second spacers are the same as those processes for forming the first spacers 502A, 502B.”

Wu922 ¶ [0024].

“As shown in FIG. 1, a spacer formation process is optionally performed to form at least a first spacer 502A, 502B respectively beside the thermal oxide layers 501A, 501B. The preferred first spacers 502A, 502B may be a single-layered structure or a multi-layered structure. The preferred material of the first spacers 502A, 502B may use silicon oxide, silicon nitride, oxynitride, or other adoptable dielectric material. The first spacers 502A, 502B are formed by a plasma enhanced chemical vapor deposition (PECVD) process, a low-pressure chemical vapor deposition process (LPCVD), or other method for depositing the material layers of the first spacers 502A, 502B. Subsequently, an etch back process is performed to etch the material layers of the first spacers 502A, 502B.”

Wu922 ¶ [0018].

Exemplary Disclosures

“Step 701: forming at least a thermal oxide layer on the sidewalls of the gate structures[.]”

Wu922 ¶ [0028].

“Please refer to FIG. 9 to FIG. 14, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a second preferred embodiment of the present invention. Some elements are the same as those of the first preferred embodiment and are numbered as those of the first preferred embodiment. Referring to FIG. 9, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the second preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. For the simplicity of description, a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 are shown in the diagram in the following.”

Wu922 ¶ [0038].

“As shown in FIG. 9, a thermal oxidation process to form a thermal oxide layer 501A, 501B respectively formed on the sidewalls of the gate structures 36A, 36B, and a spacer formation process is performed to form at least a first spacer 502A, 502B respectively formed beside the thermal oxide layers 501A, 501B.”

Wu922 ¶ [0039].

“As shown in FIG. 14, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B.”

Wu922 ¶ [0043].

Additionally, under Plaintiff’s apparent interpretation of the claim language, the claimed “second gate electrode” may include a silicide film. *See* AICP’s P.R. 3-1 Disclosures, Ex. H, at 35-43. Although TSMC does not necessarily agree with such an interpretation, Wu922 further discloses this element under this interpretation, as shown below.

Exemplary Disclosures

For example, Wu922 discloses silicide layer formed on NMOS gate electrode 42. *See, e.g.*, the following:

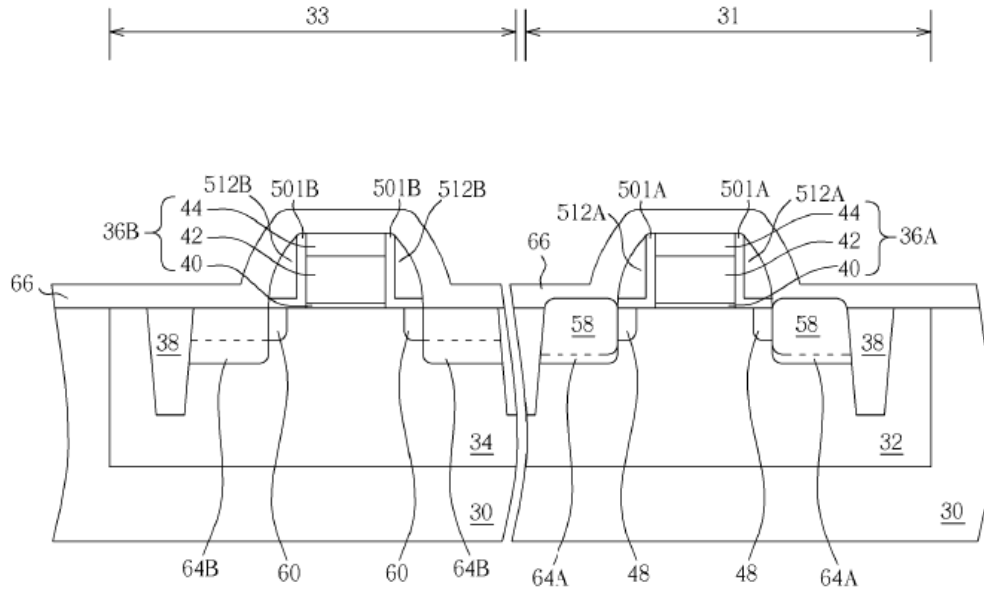


FIG. 7

FIG. 7.

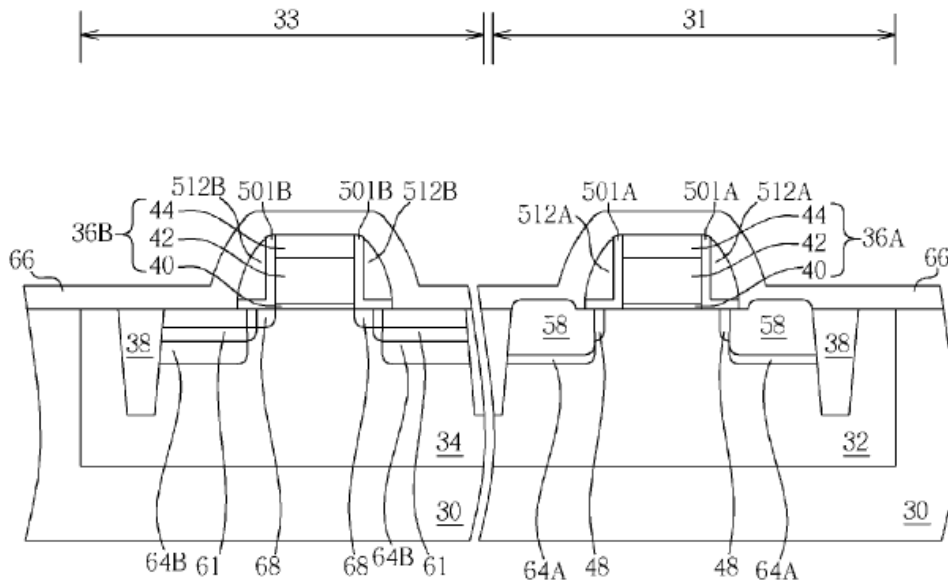


FIG. 14

FIG. 14.

Exemplary Disclosures

“Please refer to FIG. 1 to FIG. 7, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a first preferred embodiment of the present invention. Referring to FIG. 1, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the first preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-type well is a P well. The following diagrams shows a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 for illustration. A plurality of isolation structures between the MOS transistors to prevent short circuiting, such as shallow trench isolations 38 formed between the PMOS transistor region 31 and the NMOS transistor region 33. Each of the gate structure 36A, 36B includes a gate dielectric layer 40, a gate 42, and a cap layer 44. The gate dielectric layer 40 may comprise dielectric materials including silicon oxide, oxynitride, and silicon nitride; high-k dielectric materials including metal oxide, metal silicate, metal aluminate, and metal oxynitride; or combinations thereof. The gate dielectric layer 40 may be formed by a thermal oxidation process, a nitridation process, or a chemical vapor deposition (CVD) process. The gate 42 may use polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof as material. The material of the cap layer 44 may include silicon oxide, oxynitride, silicon nitride, or silicon carbide (SiC). A thermal oxidation process is performed to form an oxide layer 501A, 501B on sidewalls of the gate structures 36A, 36B for protecting the gate structures 36A, 36B.”

Wu922 ¶ [0017].

“As shown in FIG. 7, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. The processes of forming the second spacers are the same as those processes for forming the first spacers 502A, 502B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source/drain 64B in the NMOS transistor region 33. The processes of forming the source/drain 64A, 64B are well known, and will not be described in detail. In addition, a self-aligned silicide process (salicide process) is optionally performed. A metal layer, including titanium (Ti), cobalt (Co), nickel (Ni), palladium (Pd), platinum (Pt) or the like, is deposited. And a rapid thermal process is performed to form a silicide layer (not shown) on the surfaces of the source/drain 64A, 64B.”

Wu922 ¶ [0024].

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.” Wu922 ¶ [0036].

Exemplary Disclosures

“As shown in FIG. 14, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source drain 64B in the NMOS transistor region 33. In addition, a self-aligned silicide process is optionally performed to form a silicide layer (not shown) on the surfaces of the gate structures or the source/drain.”

Wu922 ¶ [0043].

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”

Wu922 ¶ [0055].

To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.

11[e] a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer, and

Wu922 discloses this feature. For example, Wu922 discloses NMOS source/drain region 64B of an n-type conductivity which is formed in the NMOS active region on a lateral side of L-shaped spacers 501B and spacers 512B. *See, e.g.*, the following:

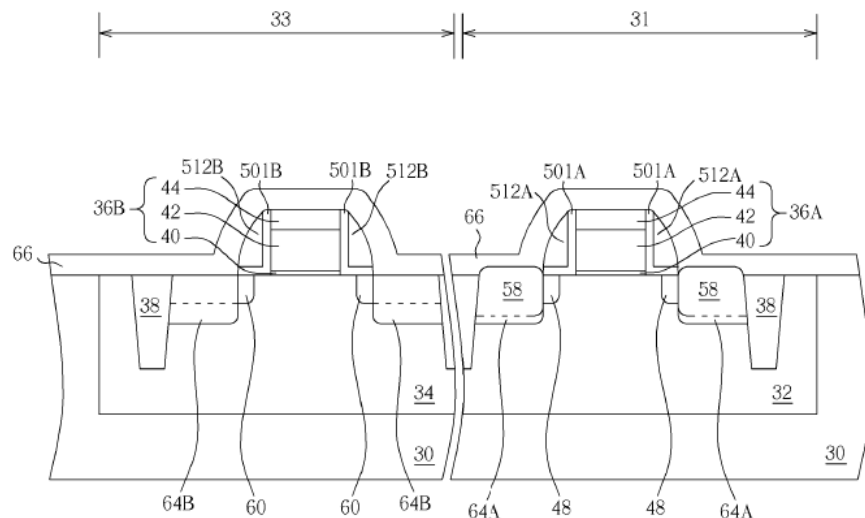
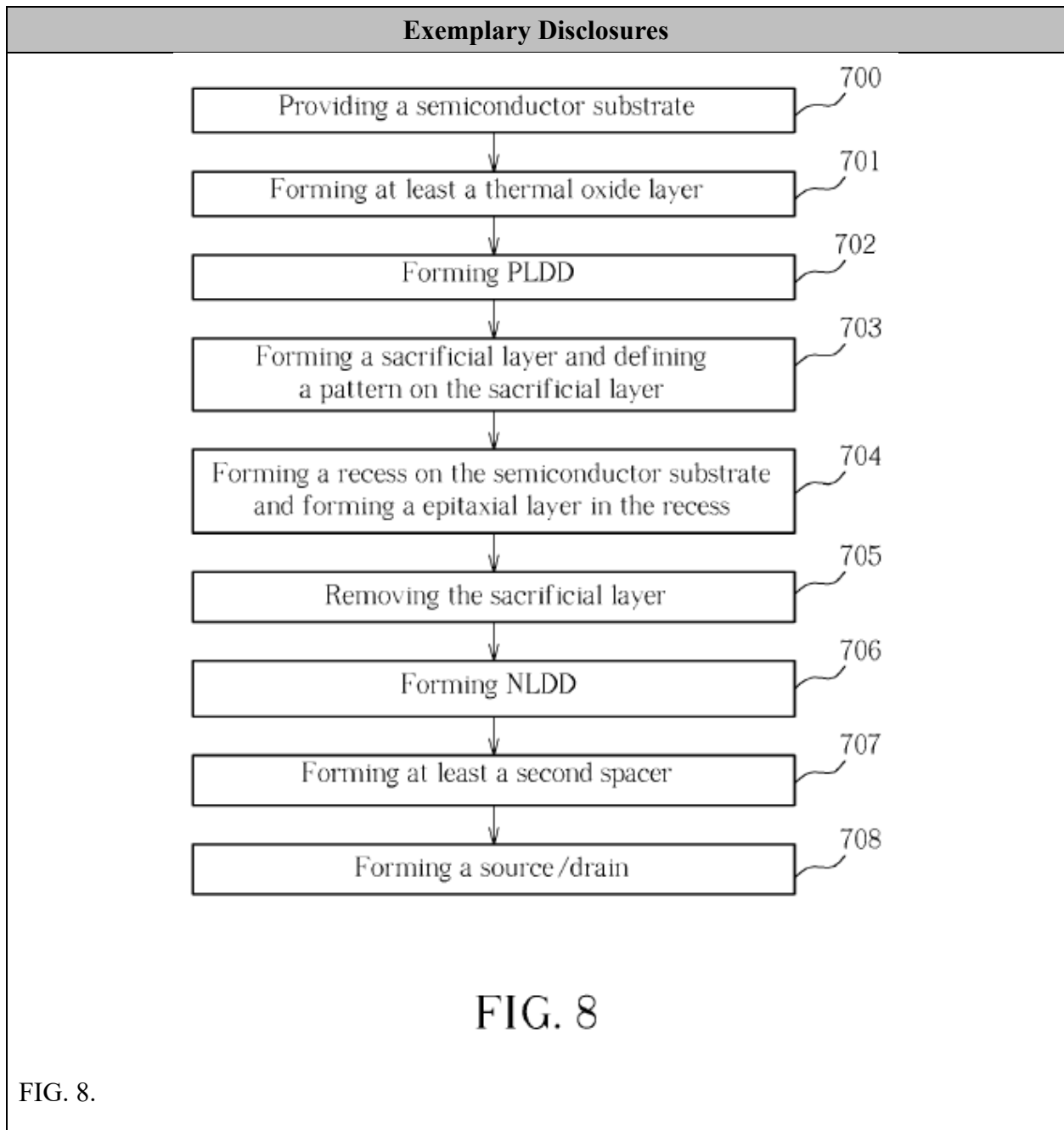
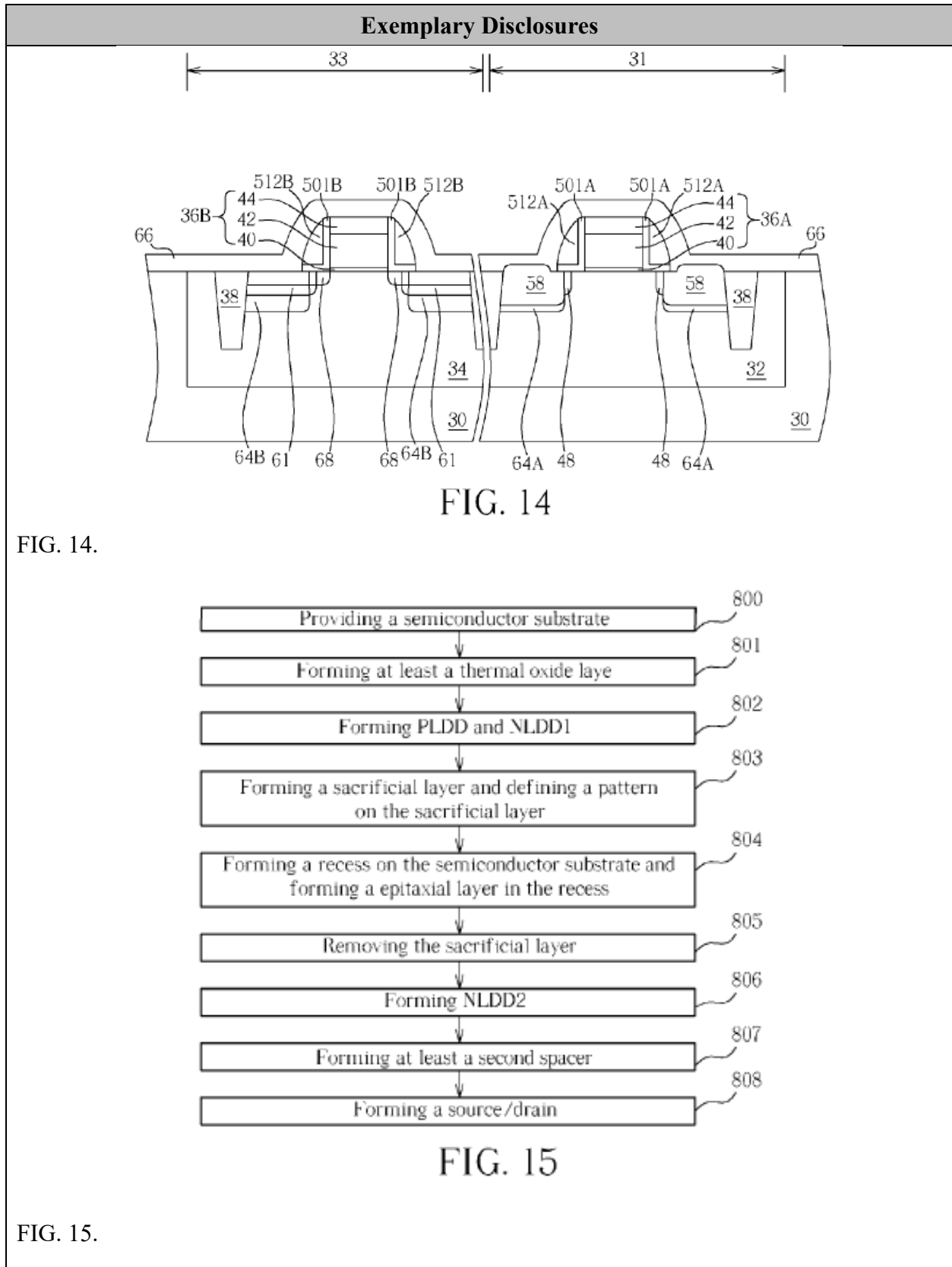


FIG. 7

FIG. 7.





Exemplary Disclosures

“As shown in FIG. 6, a second ion implantation process is performed to form an n-type lightly doped drain (NLDD) 60 beside the gate structure 36B in the P well 34. The formation of the NLDD 60 may use the same fabrication processes as the first ion implantation shown in FIG. 1. For instance, a patterned photoresist (not shown) is formed to protect the N well 32 and the gate structure 36A in the PMOS transistor region 31. Then, the second ion implantation process is performed to implant dopants into the P well 34. In addition, a rapid thermal process is optionally performed after the formation of the NLDD 60 to activate the dopants.”

Wu922 ¶ [0023].

“As shown in FIG. 7, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. The processes of forming the second spacers are the same as those processes for forming the first spacers 502A, 502B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source/drain 64B in the NMOS transistor region 33. The processes of forming the source/drain 64A, 64B are well known, and will not be described in detail.”

Wu922 ¶ [0024].

“Step 706: performing a second ion implantation process to form a NLDD in the semiconductor substrate beside the gate structure of the NMOS transistor[.]”

Wu922 ¶ [0033].

“Step 708: performing a third ion implantation process to form a respective source/drain in the semiconductor substrate beside the gate structures of the NMOS transistor and the PMOS transistor.”

Wu922 ¶ [0035].

“As shown in FIG. 9, a thermal oxidation process to form a thermal oxide layer 501A, 501B respectively formed on the sidewalls of the gate structures 36A, 36B, and a spacer formation process is performed to form at least a first spacer 502A, 502B respectively formed beside the thermal oxide layers 501A, 501B. A first ion implantation process is performed to implant dopants, to form an NLDD1 61 in the NMOS transistor region 33 and a PLDD 48 in the PMOS transistor region 31. In addition, a rapid thermal process is optionally performed after the formation of the PLDD 48 in order to diffuse and to activate the dopants.”

Wu922 ¶ [0039].

“Please refer to FIG. 13, another etch process is performed, preferably a phosphoric acid treatment, to remove the sacrificial layer 52 and the first spacers 502A, 502B. In the present embodiment, the sacrificial layer 52 and the first spacers 502A, 502B are made of silicon nitride, and so that the sacrificial layer 52 and the first spacers 502A, 502B are removed by the phosphoric acid treatment simultaneously. A second ion implantation process is performed to

Exemplary Disclosures

form an NLDD2 68 in the P well 34 beside the gate structure 36B. The formation of the NLDD2 68 may use the same fabrication processes as the first ion implantation by means of forming a patterned photoresist formed to protect the N well 32 and the gate structure 36A in the PMOS transistor region 31. Then, the second ion implantation process is performed to implant dopants into the P well 34. In addition, a rapid thermal process is optionally performed after the formation of the NLDD2 68 for diffusing and activating the dopants.”

Wu922 ¶ [0042].

“As shown in FIG. 14, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source drain 64B in the NMOS transistor region 33.”

Wu922 ¶ [0043].

“Step 802: performing a first ion implantation process to form a PLDD in the semiconductor substrate beside the gate structures of the PMOS transistor, and an NLDD1 in the semiconductor substrate beside the gate structures of the NMOS transistor[.]”

Wu922 ¶ [0048].

“Step 806: performing a second ion implantation process to form an NLDD2 in the semiconductor substrate beside the gate structure of the NMOS transistor[.]”

Wu922 ¶ [0052].

“Step 808: performing a third ion implantation process to form a respective source/drain in the semiconductor substrate beside the gate structures of the NMOS transistor and the PMOS transistor.”

Wu922 ¶ [0054]. To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.

Exemplary Disclosures

11[f] the stress insulating film formed on the second active region to cover the second gate electrode, the second sidewall spacer, and the second source/drain region.

Wu922 discloses this feature. For example, Wu922 discloses CESL 66 formed on the NMOS active region to cover the NMOS gate electrode 42, L-shaped spacers 501B and spacers 512B, and NMOS source/drain regions 64B. *See, e.g.,* the following:

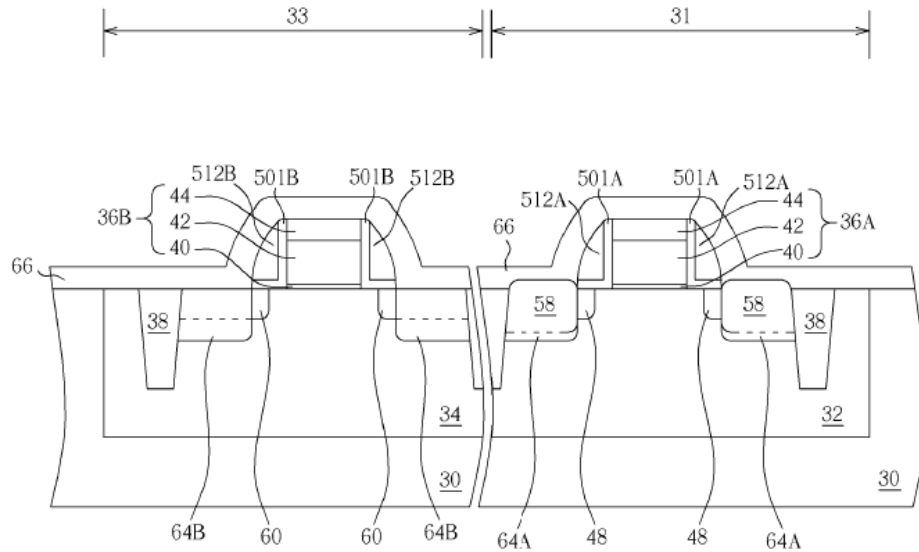


FIG. 7

FIG. 7.

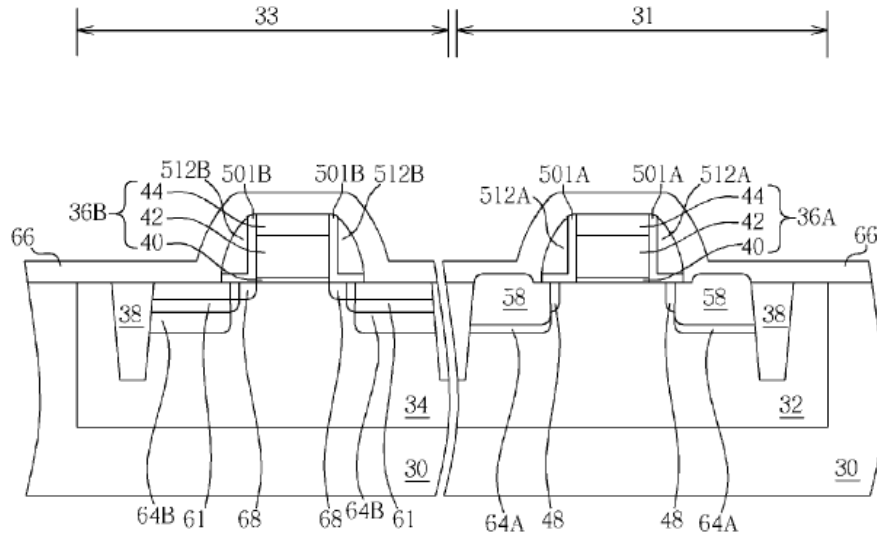


FIG. 14

FIG. 14.

Exemplary Disclosures

“In order to increase the driving current of a complementary metal-oxide semiconductor (CMOS) transistor including a p-type MOS (PMOS) transistor and an n-type MOS (NMOS) transistor, the industrial circles develop a strained-silicon technique, which uses unique processes or lattice constant discrepancy to increase driving current. The strained-silicon technique substantially includes a substrate strained based method and a process-induced strain based method. The substrate-strained based system is performed with a strained-silicon substrate or a selective epitaxial growth process that results in lattice constant discrepancy. The process-induced strain based method is performed with several unique processes to form a strained thin film upon a surface of the MOS transistor that exert tensile stress or compressive stress upon the MOS transistor. Both of the strained silicon techniques introduce strain into the channel region and reduce carrier mobile resistance thereby improving carrier mobility and MOS transistor performance.”

Wu922 ¶ [0005].

“A deposition process is performed to form a contact etch stop layer (CESL) 66 on the surface of the gate structures 36A, 36B, the second spacers 512A, 512B, and the sources/drains 64A, 64B. The material of the CESL 66 may include a dielectric material or a strained silicon material, i.e. silicon nitride.”

Wu922 ¶ [0025].

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”

Wu922 ¶ [0036].

“A deposition process is performed to form a CESL 66 on the surface of the gate structures 36A, 36B, the second spacers 512A, 512B, and the sources/drains 64A, 64B.”

Wu922 ¶ [0044].

Additionally, under Plaintiff’s apparent interpretation of the claim language, the claimed “second gate electrode” may include a silicide film. *See* AICP’s P.R. 3-1 Disclosures, Ex. H, at 35-43. Although TSMC does not necessarily agree with such an interpretation, Wu922 further discloses this element under this interpretation, as shown below.

For example, Wu922 discloses silicide layer formed on NMOS gate electrode 42. *See, e.g.*, the following:

Exemplary Disclosures

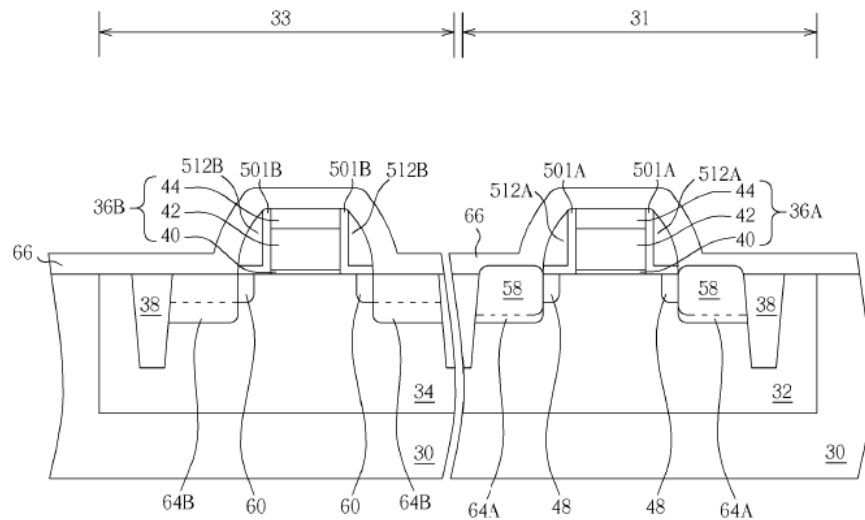


FIG. 7

FIG. 7.

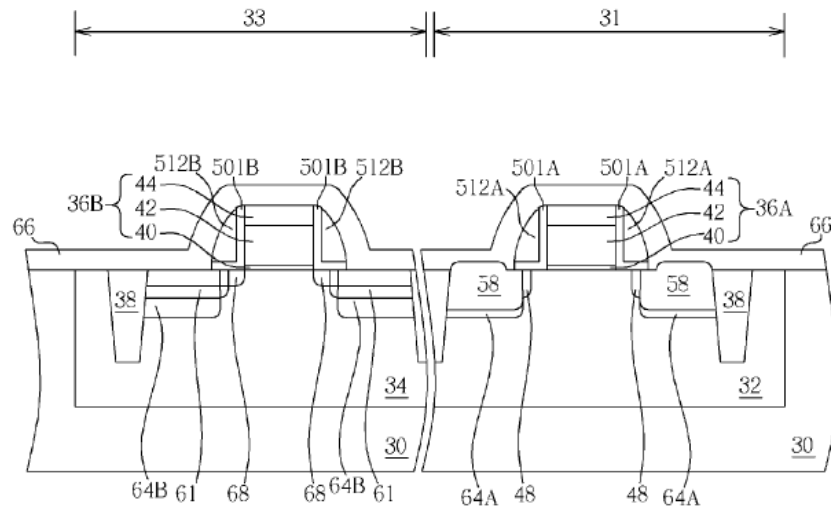


FIG. 14

FIG. 14.

“Please refer to FIG. 1 to FIG. 7, which are schematic diagrams illustrating a method of forming a CMOS transistor according to a first preferred embodiment of the present invention. Referring to FIG. 1, a semiconductor substrate 30 is provided. A plurality of first active area and a plurality of second active area are defined on the semiconductor substrate 30. Each of the first active area includes a first-type well and a gate structure, and each of the second active area includes a second-type well and a respective gate structure thereon. In the first preferred embodiment of the present invention, the first active area is a PMOS transistor region 31, and the second active area is an NMOS transistor region 33. Therefore, the first-type well is an N well, and the second-

Exemplary Disclosures

type well is a P well. The following diagrams shows a gate structure 36A and an N well 32 formed in the PMOS transistor region 31, and a gate structure 36B and a P well 34 in the NMOS transistor region 33 for illustration. A plurality of isolation structures between the MOS transistors to prevent short circuiting, such as shallow trench isolations 38 formed between the PMOS transistor region 31 and the NMOS transistor region 33. Each of the gate structure 36A, 36B includes a gate dielectric layer 40, a gate 42, and a cap layer 44. The gate dielectric layer 40 may comprise dielectric materials including silicon oxide, oxynitride, and silicon nitride; high-k dielectric materials including metal oxide, metal silicate, metal aluminate, and metal oxynitride; or combinations thereof. The gate dielectric layer 40 may be formed by a thermal oxidation process, a nitridation process, or a chemical vapor deposition (CVD) process. The gate 42 may use polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof as material. The material of the cap layer 44 may include silicon oxide, oxynitride, silicon nitride, or silicon carbide (SiC). A thermal oxidation process is performed to form an oxide layer 501A, 501B on sidewalls of the gate structures 36A, 36B for protecting the gate structures 36A, 36B.”

Wu922 ¶ [0017].

“As shown in FIG. 7, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. The processes of forming the second spacers are the same as those processes for forming the first spacers 502A, 502B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source/drain 64B in the NMOS transistor region 33. The processes of forming the source/drain 64A, 64B are well known, and will not be described in detail. In addition, a self-aligned silicide process (salicide process) is optionally performed. A metal layer, including titanium (Ti), cobalt (Co), nickel (Ni), palladium (Pd), platinum (Pt) or the like, is deposited. And a rapid thermal process is performed to form a silicide layer (not shown) on the surfaces of the source/drain 64A, 64B.”

Wu922 ¶ [0024].

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”

Wu922 ¶ [0036].

“As shown in FIG. 14, at least a second spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B. A third implant process is performed to form a respective source/drain 64A in the PMOS transistor region 31, and a respective source drain 64B in the NMOS transistor region 33. In addition, a self-aligned silicide process is optionally performed to form a silicide layer (not shown) on the surfaces of the gate structures or the source/drain.” Wu922 ¶ [0043].

Exhibit 425-19: Wu922

Exemplary Disclosures

“Accordingly, the formation of the PMOS transistor and the NMOS transistor of a CMOS transistor is nearly finished. A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor.”

Wu922 ¶ [0055].

To the extent that Wu922 is found not to disclose this feature, it would have been obvious based on the disclosures of Wu922 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-18 and 425-20 through 425-21 for the reasons discussed herein and in Defendant’s cover pleading.