

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner,

v.

Advanced Integrated Circuit Process LLC,

Patent Owner.

Patent No. 8,907,425 B2
Filing Date: June 20, 2012
Issue Date: December 9, 2014

Title: SEMICONDUCTOR DEVICE

Inter Partes Review No. IPR2025-00683

PETITION FOR *INTER PARTES* REVIEW

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Ex-1002	Prosecution History of the ’425 Patent (excerpted) (“File History”).
Ex-1003	Declaration of Scott E. Thompson, Ph.D.
Ex-1004	Curriculum Vitae of Scott E. Thompson, Ph.D.
Ex-1005	U.S. Pat. Pub. No. 2009/0246922 A1 to Wu et al. (“Wu”).
Ex-1006	U.S. Pat. Pub. No. 2007/0249069 A1 to Alvarez et al. (“Alvarez”).
Ex-1007	S. Wolf, <i>Silicon Processing for the VLSI Era: Volume 4—Deep-Submicron Process Technology</i> (2002) (excerpted) (“Wolf”).
Ex-1008	U.S. Pat. Pub. No. 2005/0112817 A1 to Cheng et al. (“Cheng”).
Ex-1009	U.S. Pat. Pub. No. 2007/0034906 A1 to Wang et al. (“Wang”).
Ex-1010	U.S. Pat. Pub. No. 2008/0029825 A1 to Saito et al. (“Saito”).
Ex-1011	U.S. Pat. Pub. No. 2005/0285203 A1 to Fukutome et al. (“Fukutome”).
Ex-1012	D. James, “2004 – The Year of 90-nm: A Review of 90 nm Devices,” 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (2005) (“James”).
Ex-1013	S.M. Sze, <i>Physics of Semiconductor Devices</i> (2d ed. 1981) (excerpted).

Exhibit	Description
Ex-1014	J.D. Plummer et al., <i>Silicon VLSI Technology: Fundamentals, Practice and Modeling</i> (2000) (excerpted).
Ex-1015	S.E. Thompson et al., “A 90-nm Logic Technology Featuring Strained Silicon,” <i>IEEE Transactions on Electron Devices</i> , vol. 51. No. 11, pp. 1790-97 (Nov. 2004).
Ex-1016	Y. Sun et al., “Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors,” <i>Journal of Applied Physics</i> , vol. 101, Art. No. 104503 (22 pages) (May 2007).
Ex-1017	T. Ghani et al., “A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors,” <i>Technical Digest of the 2003 IEEE International Electron Devices Meeting (“IEDM”)</i> , pp. 978-80 (Dec. 10, 2003).
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Ex-1019	U.S. Pat. Pub. No. 2006/0286729 A1 to Kavalieros et al.
Ex-1020	U.S. Pat. Pub. No. 2006/0148151 A1 to Murthy et al.
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Ex-1022	P. Morin et al., “Extensive Study of the Correlation between ContactEtch Stop Nitride Material Properties and Negative Bias Temperature Instabilities Measured in pMOSFETS,” <i>ECS Transactions</i> , vol. 6, no. 3, pp. 355-69 (2007).
Ex-1023	U.S. Pat. Pub. No. 2007/0235823 A1 to Hsu et al.
Ex-1024	U.S. Pat. Pub. No. 2005/0170104 A1 to Jung et al.

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Ex-1025	U.S. Pat. Pub. No. 2008/0145984 A1 to Ke et al.
Ex-1026	P. Bai et al., “A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell,” Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 657-60 (Dec. 2004).
Ex-1027	K. Mistry et al., “A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging,” Technical Digest of the of the 2007 IEEE International Electron Devices Meeting (IEDM), pp. 247-50 (Dec. 2007).
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Ex-1029	U.S. Pat. Pub. No. 2004/0262784 A1 to Doris et al.
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Ex-1031	U.S. Pat. Pub. No. 2007/0134870 A1 to Lee et al.
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Ex-1033	U.S. Pat. Pub. No. 2009/0020820 A1 to Baik et al.
Ex-1034	U.S. Pat. Pub. No. 2008/0293207 A1 to Koutny et al.
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Exhibit	Description
Ex-1036	Declaration of Shauna Wiest in support of public availability of James (2004).
Ex-1037	Declaration of Lauren Gluckman in support of public availability of Wolf (2002).
Ex-1038	Declaration of Rachel Watters in support of public availability of Wolf (2002).
Ex-1039	S. Thompson et al., “Source/Drain Extension Scaling for 0.1 μ m and Below Channel Length MOSFETS,” Digest of Technical Papers for the 1998 Symposium on VLSI Technology, pp. 132-33 (1998).
Ex-1040	D.M. Fleetwood et al., <i>Defects in Microelectronic Materials and Devices</i> (2008).
Ex-1041	U.S. Pat. Pub. No. 2006/0246641 A1 to Kammler et al.
Ex-1042	U.S. Pat. Pub. No. 2007/0228482 A1 to Wei et al.
Ex-1043	U.S. Pat. Pub. No. 2008/0203486 A1 to Wiatr et al.
Ex-1044	U.S. Pat. Pub. No. 2009/0242995 A1 to Suzuki et al.
Ex-1045	U.S. Pat. Pub. No. 2007/0090465 A1 to Suzuki et al.
Ex-1046	A. Pavlov & M. Sachdev, <i>CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies: Process-Aware SRAM Design and Test</i> (2008) (excerpted).
Ex-1047	U.S. Pat. Pub. No. 2007/0023832 A1 to Matsui.

Exhibit	Description
Ex-1048	M. Ishida et al., “A Novel 6T-SRAM Cell Technology Designed with Rectangular Patterns Scalable Beyond 0.18 μm Generation and Desirable for Ultra High Speed Operation,” Proceedings of the 1998 International Electron Devices Meeting (IEDM), pp. 201-04 (1998).
Ex-1049	D. Balobas & N. Konofaos, “Design and Evaluation of 6T SRAM Layout Designs at Modern Nanoscale CMOS Processes,” 4th International Conference on Modern Circuits and System Technologies (2015).
Ex-1050	U.S. Pat. Pub. No. 2011/0074498 A1 to Thompson et al.
Ex-1051	Second Amended Docket Control Order, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation et al.</i> , No. 2:24-cv-00730-JRG (E.D. Tex.).

LIST OF CHALLENGED CLAIMS

Claim 1	
[1Pre]	A semiconductor device, comprising:
[1A]	a first MIS transistor, wherein: the first MIS transistor includes:
[1B]	a first gate insulating film formed on a first active region in a semiconductor substrate,
[1C]	a first gate electrode formed on the first gate insulating film,
[1D]	a first sidewall spacer formed on a side surface of the first gate electrode,
[1E]	a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region, and
[1F]	a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress,
[1G]	an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode,
[1H]	a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer,
[1I]	the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween, and
[1J]	the first stress-relief film is not in direct contact with the side surface of the first gate electrode.

Claim 2	
The semiconductor device of claim 1, further comprising: a first offset spacer which is formed between the first gate electrode and the first sidewall spacer, and whose cross-section has an I shape.	
Claim 3	
The semiconductor device of claim 1, further comprising: a first silicide layer formed on the first gate electrode; and a second silicide layer formed on the first source/drain region which includes the silicon compound layer.	
Claim 4	
The semiconductor device of claim 1, wherein the first stress-relief film is formed on a side surface of the silicon compound layer.	
Claim 5	
The semiconductor device of claim 1, wherein the first sidewall spacer includes an inner sidewall spacer which is formed on the side surface of the first gate electrode, and whose cross-section has an L shape, and an outer sidewall spacer formed on the inner sidewall spacer.	
Claim 6	
[6Pre]	The semiconductor device of claim 1, wherein
[6A]	the first sidewall spacer includes an inner sidewall spacer whose cross-section has an L shape, and
[6B]	the stress insulating film is formed in contact with a surface of the inner sidewall spacer which is curved to have an L-shaped cross-section.

Claim 7	
[7Pre]	The semiconductor device of claim 1, wherein
[7A]	the first MIS transistor is a p-type MIS transistor,
[7B]	the first stress is a compressive stress, and
[7C]	the second stress is a tensile stress.
Claim 8	
[8Pre]	The semiconductor device of claim 1, wherein
[8A]	the silicon compound layer is a SiGe layer,
[8B]	the stress insulating film is a silicon nitride film, and
[8C]	the first stress-relief film is a silicon oxide film.
Claim 9	
[9Pre]	The semiconductor device of claim 1, wherein
[9A]	the first MIS transistor is an n-type MIS transistor,
[9B]	the first stress is a tensile stress, and
[9C]	the second stress is a compressive stress.
Claim 10	
[10Pre]	The semiconductor device of claim 1, further comprising:
[10A]	an isolation region formed in the semiconductor substrate to surround the first active region;
[10B]	a gate interconnect formed on the isolation region;
[10C]	an interconnect sidewall spacer formed on a side surface of the gate interconnect;

[10D]	a second stress-relief film formed on a side surface of a recessed portion provided in the isolation region on a lateral side of the interconnect sidewall spacer; and
[10E]	the stress insulating film formed on the isolation region to cover the gate interconnect, the interconnect sidewall spacer, and the second stress-relief film.
Claim 11	
[11Pre]	The semiconductor device of claim 1, further comprising:
[11A]	a second MIS transistor, wherein: the second MIS transistor includes:
[11B]	a second gate insulating film formed on a second active region in the semiconductor substrate,
[11C]	a second gate electrode formed on the second gate insulating film,
[11D]	a second sidewall spacer formed on a side surface of the second gate electrode,
[11E]	a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer, and
[11F]	the stress insulating film formed on the second active region to cover the second gate electrode, the second sidewall spacer, and the second source/drain region.
Claim 12	
The semiconductor device of claim 11, wherein no first stress-relief film is formed on the second active region.	

Claim 13	
[13Pre]	The semiconductor device of claim 1, further comprising:
[13A]	a third MIS transistor, wherein: the third MIS transistor includes:
[13B]	a third gate insulating film formed on a third active region in the semiconductor substrate,
[13C]	a third gate electrode formed on the third gate insulating film,
[13D]	a third sidewall spacer formed on a side surface of the third gate electrode,
[13E]	a third source/drain region of a first conductivity type which is formed in the third active region on a lateral side of the third sidewall spacer,
[13F]	a protective film formed on the third active region to cover the third gate electrode, the third sidewall spacer, and the third source/drain region, and
[13G]	the stress insulating film formed on the protective film.
Claim 14	
The semiconductor device of claim 13, wherein no silicide layer is formed on the third gate electrode and the third source/drain region.	
Claim 15	
The semiconductor device of claim 13, wherein the first stress-relief film and the protective film are made of a same insulating material.	

I. RELIEF REQUESTED

Applying the following grounds, Petitioner requests *inter partes* review of the '425 Patent¹ and cancellation of claims 1-15:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1A	1, 3-5, 7-9, 11-15	103	Wu, Alvarez
1B	2		Wu, Alvarez, Wolf
2A	1, 3-9, 11-12		Cheng
2B	2		Cheng, Wolf
2C	1, 3-9, 11-12		Cheng, Wang
2D	2		Cheng, Wang, Wolf
3	1, 3-4, 7-8, 10		Saito, Fukutome, James

II. STATE OF THE ART

The '425 Patent describes stress-relief films for metal-insulator-semiconductor field-effect transistors (“MISFETs”).² This technology was already well-known.

A. MISFETs

MISFETs have *source/drain* regions for current input/output. (Ex-1003 ¶49; Ex-1013, 9-10, Figs. 3, 6; Ex-1014, 45-51.) Additionally, a *gate* overlies a *channel*

¹ U.S. Patent No. 8,907,425 (Ex-1001).

² “MISFET” and “MOSFET” (“Metal-*Oxide*-Semiconductor Field-Effect Transistor”) are interchangeable. (Ex-1003 ¶49 n.8.)

region between source and drain. (Ex-1003 ¶49; Ex-1013, 9-10, Fig. 3; Ex-1014, 40-45.) The **gate** includes a **gate dielectric** that separates a **gate electrode** from the channel region. (Ex-1003 ¶49; Ex-1013, 9-10, Fig. 3; Ex-1014, 40-45.) Applying voltage to the gate electrode controls a conductive channel to connect or disconnect the source and drain. (Ex-1003 ¶49; Ex-1013, 9-10, 14, Figs. 3, 6.)

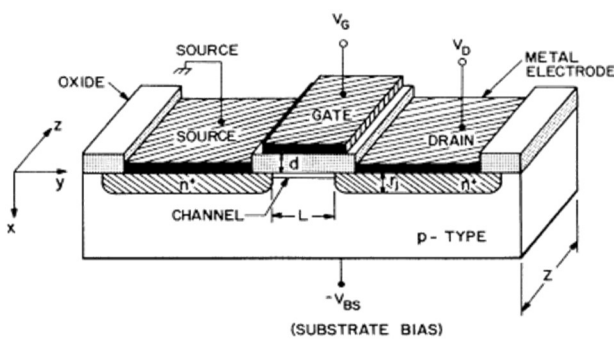
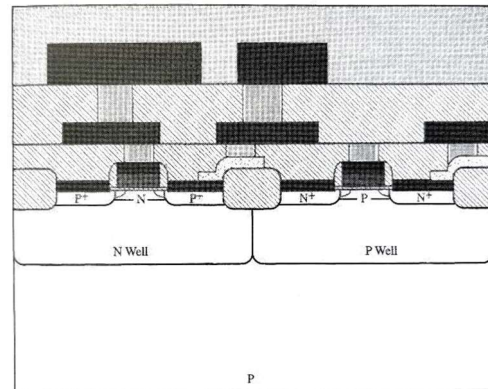


Fig. 3 Schematic diagram of a MOSFET. (After Kahng and Atalla, Ref. 4.)

Ex-1013, Fig. 3



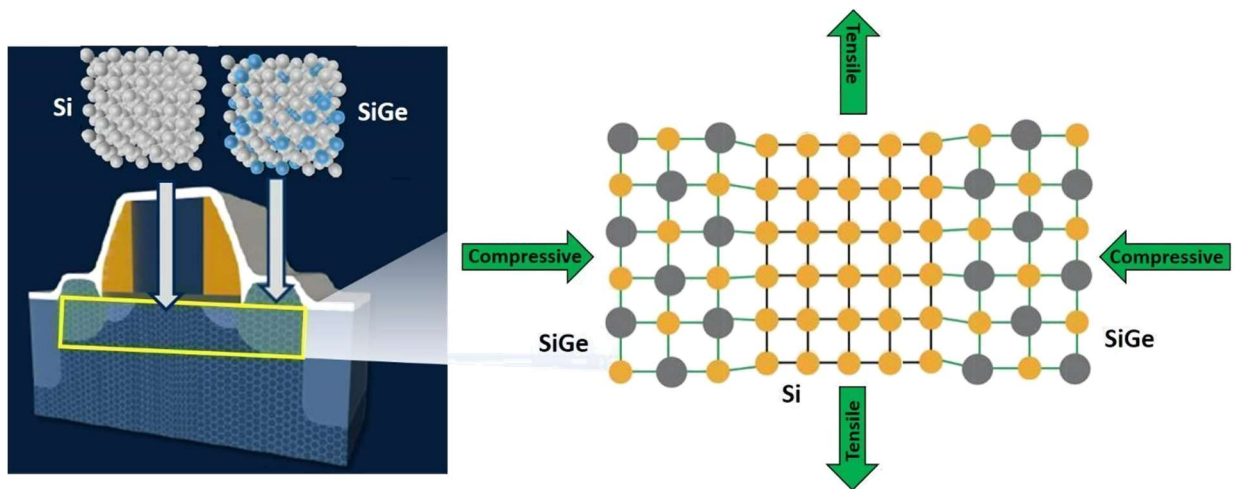
Ex-1014, Fig. 1-11

Generally, source/drain regions are **doped** with **p-type** or **n-type** impurities, and channel regions are oppositely doped. (Ex-1003 ¶50; Ex-1013, 9-10; Ex-1014, 45-51.) The terms **PMOS** and **NMOS** refer to MISFETs with p-type or n-type source/drain regions, respectively. (Ex-1003 ¶50; Ex-1014, 16-17, 19-20, Figs. 1-11, 2-2.) Typical devices are **CMOS** (“Complementary MOS”), which include both PMOS and NMOS. (Ex-1003 ¶50; Ex-1014, 16, Fig. 1-11.)

B. Strained-Silicon Technology

PMOS was once much slower than NMOS. Strained-silicon technology changed that. Because germanium atoms are **larger** than silicon atoms, growing

silicon-germanium (“SiGe”) source/drain regions *compressively* strains the silicon channel region along the current flow direction (left-to-right below). In PMOS, compressive strain improves carrier (hole) mobility and boosts operating speed. (Ex-1015, 1-7; Ex-1016, 2; Ex-1003 ¶51.) By 2005, this technology increased “hole mobility by as much as 50%.” (James, 2; Ex-1003 ¶51.)



To ensure adequate strain transfer, it was common to grow SiGe source/drain regions extending above the substrate. (Ex-1001, 1:31-43 (referencing Ex-1017); Ex-1017, 4, Figs. 1-4; Cheng, ¶¶[0065]-[0070], Figs. 4e-4j; Wang ¶¶[0030]-[0032], FIG. 9; Ex-1018, FIGS. 4-7; Ex-1019, Abstract, ¶[0025], ¶[0043], FIGS. 5, 13; Ex-1003 ¶52.) Raised SiGe regions further improve PMOS performance by reducing contact resistance. (James, 2; Ex-1003 ¶53.)

These principles were also commonly applied to NMOS, except improving NMOS carrier (electron) mobility requires *tensile* strain, not compressive. (Ex-1003 ¶54.) Creating tensile strain with source/drain regions requires growing a material

like silicon carbide (SiC) with an atom (e.g., carbon) *smaller* than silicon. (Ex-1020 ¶¶0005], ¶¶0048], ¶¶0072]; Wu ¶¶0037]; James, 2; Ex-1018 ¶¶0045]; Ex-1021 ¶¶0021]-[0022]; Ex-1003 ¶54.)

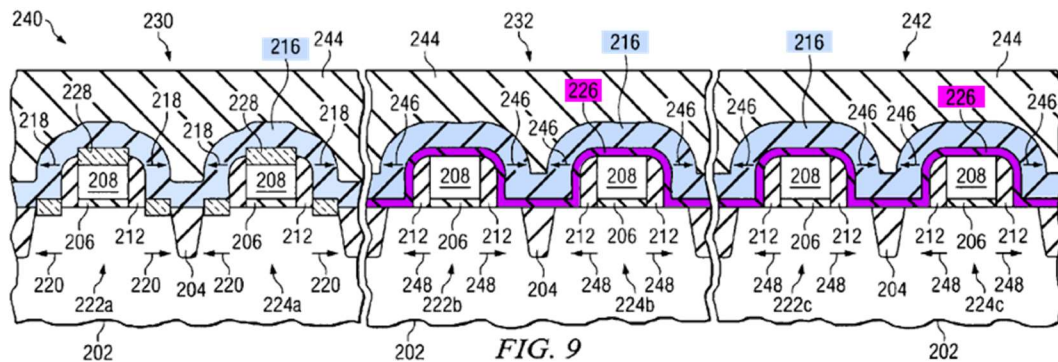
In addition to source/drain epitaxy, it was also common to induce strain by applying stressed films. (Ex-1003 ¶55; James, 2, 4; Ex-1022, 1-2, 13; Alvarez ¶¶0022], ¶¶0025], ¶¶0033]; Ex-1023 ¶¶0003]; Ex-1024 ¶¶0090].) For example, depositing a silicon nitride contact etch-stop layer (“CESL”) can, under certain conditions, “apply[] stress to [a] channel region” to improve mobility. (Ex-1023 ¶¶0003]; *see* Ex-1025 ¶¶0003]; Ex-1022, 1-2; Ex-1003 ¶55.) Depending how such a layer is prepared, it may provide tensile stress, compressive stress, or no stress. (Ex-1024 ¶¶0017], ¶¶0099]-[0100], ¶¶0131]-[0132], Tbls. IV-V, VII, Fig. 15; Ex-1003 ¶55.)

The ’425 Patent admits strained-silicon technology was known. (Ex-1001, 1:23-2:62, FIGS. 8A-10C.) At least four generations of high-volume commercial devices already used it by 2009. (Ex-1015, 1-7 (90nm devices); Ex-1026, 4-5 (65nm devices); Ex-1027, 1-4 (45nm devices); Ex-1028, 1 (32nm devices); Ex-1003 ¶48, ¶56.)

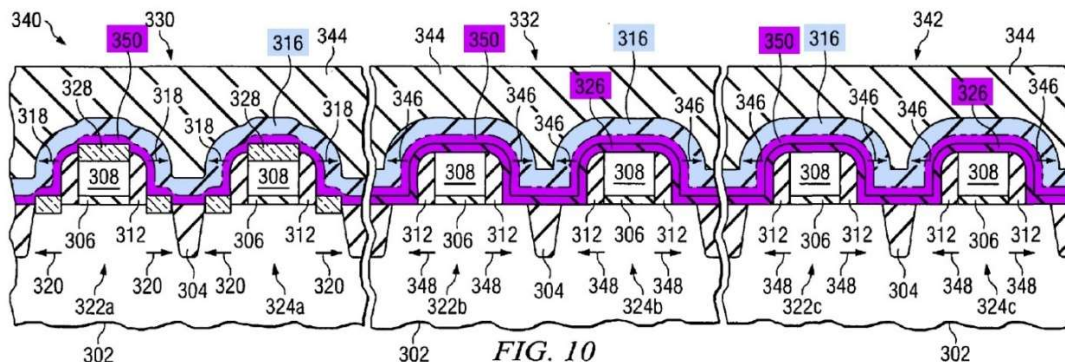
C. Stress-Relief Layers

A tensile CESL near a PMOS channel generally applies tensile stress to the channel. (Ex-1022, 1-2, 13; Ex-1029 ¶¶0005], ¶¶0013]; Ex-1023 ¶¶0037]; Ex-1003

¶57.) This can oppose compressive stress from SiGe layers, lessening PMOS performance improvements. (Ex-1022, 1-2, 13; Ex-1019 ¶[0002], ¶[0026]; Ex-1029 ¶[0005]; Ex-1003 ¶57.) To reduce such unwanted stress, it was widely known to place a stress-relief film underneath the CESL. (Ex-1030, 9:27-29, FIGS. 2, 9, 13-15; Ex-1029 ¶[0042], Figs. 1-2, 14-15; Ex-1031 ¶[0029], ¶¶[0046]-[0067], FIGS. 2-5; Ex-1032 ¶¶[0022]-[0031], Figs. 1B-1F; Ex-1033 ¶[0037], Fig. 2; Ex-1034 ¶[0108]; Alvarez, Abstract, ¶[0043], ¶[0049], ¶[0066], ¶[0068], ¶[0077], FIGS. 9-11; Ex-1003 ¶¶57-59.)



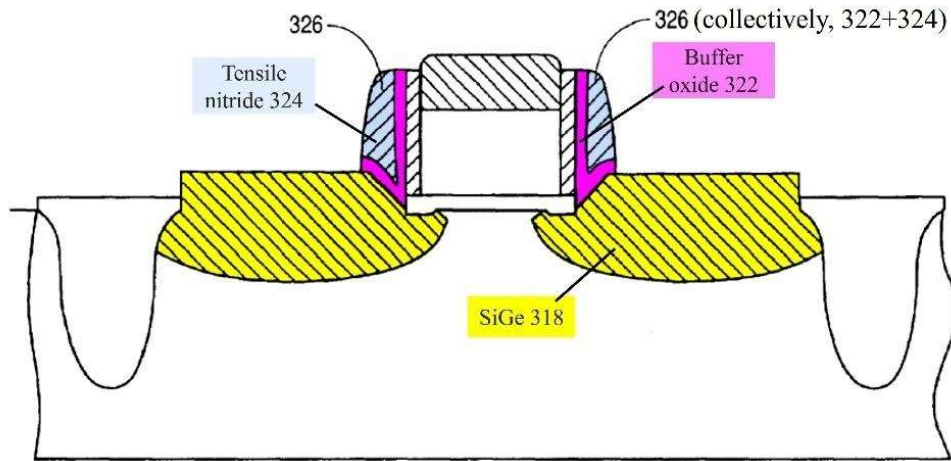
Alvarez, FIG. 9 (stress buffer layer 226)³



Alvarez, FIG. 10 (stress buffer layers 326 and 350)

³ All colored annotations herein have been added.

With raised SiGe source/drain regions, the stress-relief layer fills the space between the SiGe and gate, as shown below. (Ex-1030, 9:11-15, 9:30-35, FIGS. 7-9; *see* Ex-1035 ¶¶[0052]-[0053], FIGS. 1U-1W; Ex-1003 ¶59.)



Ex-1030, FIG. 9

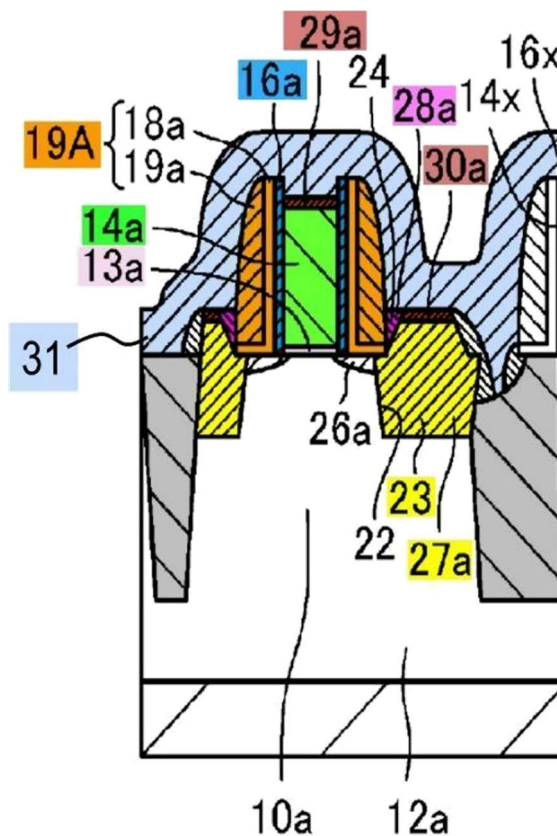
The intermediate stress-relief layer “buffers the large stress” from the CESL. (Ex-1030, 9:27-29; Ex-1003 ¶60.) That is, it applies a “neutral stress or opposite stress relative to the [CESL],” which “reduces the tensile stress in the channel region.” (Ex-1031 ¶[0049], ¶[0064]; *see* Alvarez ¶[0049]; Ex-1029 ¶[0042]; Ex-1032 ¶[0030]; Ex-1003 ¶60.)

III. '425 PATENT

A. Overview

The '425 Patent acknowledges techniques for “applying a stress to [a MISFET] channel region ... to improve the performance” were known. (Ex-1001, 1:23-27.) It further admits “*compressive* stress” (PMOS) or “*tensile* stress”

(NMOS), when “applied to the channel region,” increases carrier mobility and device performance. (*Id.*, 1:27-43, 3:1-4.) Conversely, it admits “drive capability ... is reduced” by the opposite stress. (*Id.*, 3:1-4.) The ’425 Patent discloses a stress-relief film to mitigate performance reduction in PMOS devices that include a tensile CESL. (*Id.*, 3:13-17.)



- 10a: active region
- 13a: gate insulating film
- 14a: gate electrode
- 16a: offset spacer
- 19A: sidewall
- 22: trench
- 23: silicon compound layer
- 24: space
- 27a: p-type source/drain region
- 28a: first stress-relief film
- 29a: first silicide layer
- 30a: second silicide layer
- 31: stress insulating film

Ex-1001, FIG. 6B (excerpted)

FIG. 6B above illustrates an exemplary PMOS device with known features, including a “first stress-relief film 28a ... formed in [a] space 24 located between the silicon compound layer 23 [e.g., SiGe] and the first sidewall 19A.” (*Id.*, 13:6-8; *see id.*, 14:15-42, FIG. 6B.) According to the ’425 Patent, this makes it “possible to

reduce the tensile stress applied from the stress insulating film 31 to the channel region” and “prevent a reduction in drive capability.” (*Id.*, 16:6-11.)

B. Claim Construction

Claims are construed only to the extent necessary to resolve a controversy. (*Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).) No terms require construction to resolve this controversy.⁴

C. Level of Ordinary Skill

A person ordinarily skilled in the art (“POSITA”) would have had at least a master’s degree in electrical engineering, physics, materials science, or a related field and at least three years of work experience in integrated circuit device design and manufacturing, including strained-channel MISFETs and fabrication thereof. Additional education could substitute for professional experience, and significant experience or training could substitute for formal education. (Ex-1003 ¶46.)

IV. PRIOR ART

A. Wu

Wu is prior art under pre-AIA §102(a), (e). Since Wu is in the same field (MISFETs) and reasonably pertinent to a problem the ’425 Patent addresses (strain

⁴ Certain features may be indefinite and/or require construction to resolve controversies elsewhere but not in this Petition.

engineering and device manufacturing), Wu is analogous. (Ex-1001, 1:15-7:54; Wu ¶¶[0001]-[0011]; Ex-1003 ¶75.)

Wu discloses “strained CMOS” structures with PMOS and NMOS regions 31 and 33. (Wu ¶[0009], ¶[0017], ¶[0038], FIG. 14.) In PMOS regions 31, SiGe layer 58 projects above the top of substrate 30 and compresses the channel. (Wu ¶[0021], ¶[0041], FIG. 14.) A strained “contact etch stop layer (CESL) 66” covers the devices. (Wu ¶[0025], ¶[0044], FIG. 14.) Optionally, silicide may be formed before CESL 66. (Wu ¶[0024], ¶[0043].)

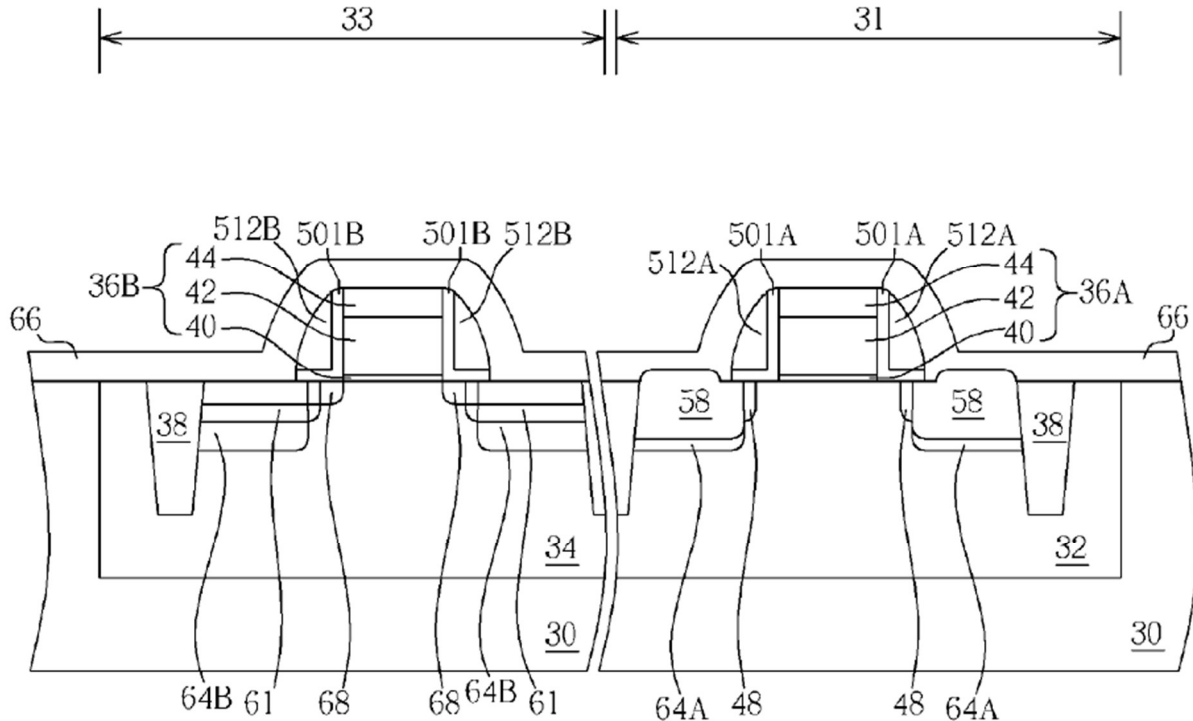


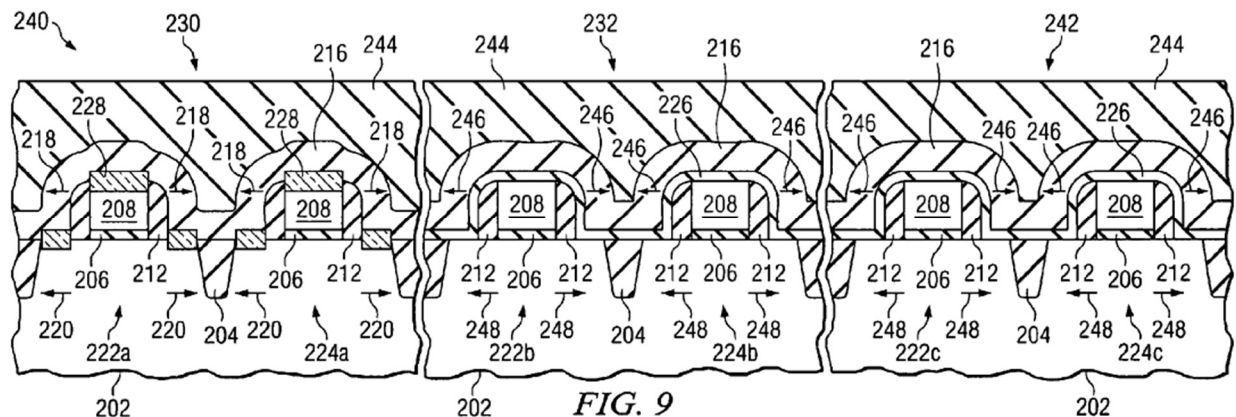
FIG. 14

Wu, FIG. 14

B. Alvarez

Alvarez is prior art under pre-AIA §102(a), (b), (e). Since Alvarez is in the same field (MISFETs) and reasonably pertinent to a problem the '425 Patent addresses (strain engineering and device manufacturing), Alvarez is analogous. (Ex-1001, 1:15-7:54; Alvarez ¶¶[0001]-[0009]; Ex-1003 ¶79.)

Alvarez discloses a “semiconductor device” with “a plurality of active areas,” including silicide region 230, non-silicide region 232, and stress-control region 242, each with a PMOS transistor 224x and NMOS transistor 222x. (Alvarez, Abstract, ¶¶[0037]-[0038], FIGS. 9-11.) In regions 232 and 242, Alvarez discloses a “stress-controlling material 226” to mitigate stress caused by “stress-increasing material 216” and prevent silicidation. (Alvarez ¶[0035], ¶[0045], ¶[0049], ¶[0054], ¶[0078], FIGS. 9-11.)

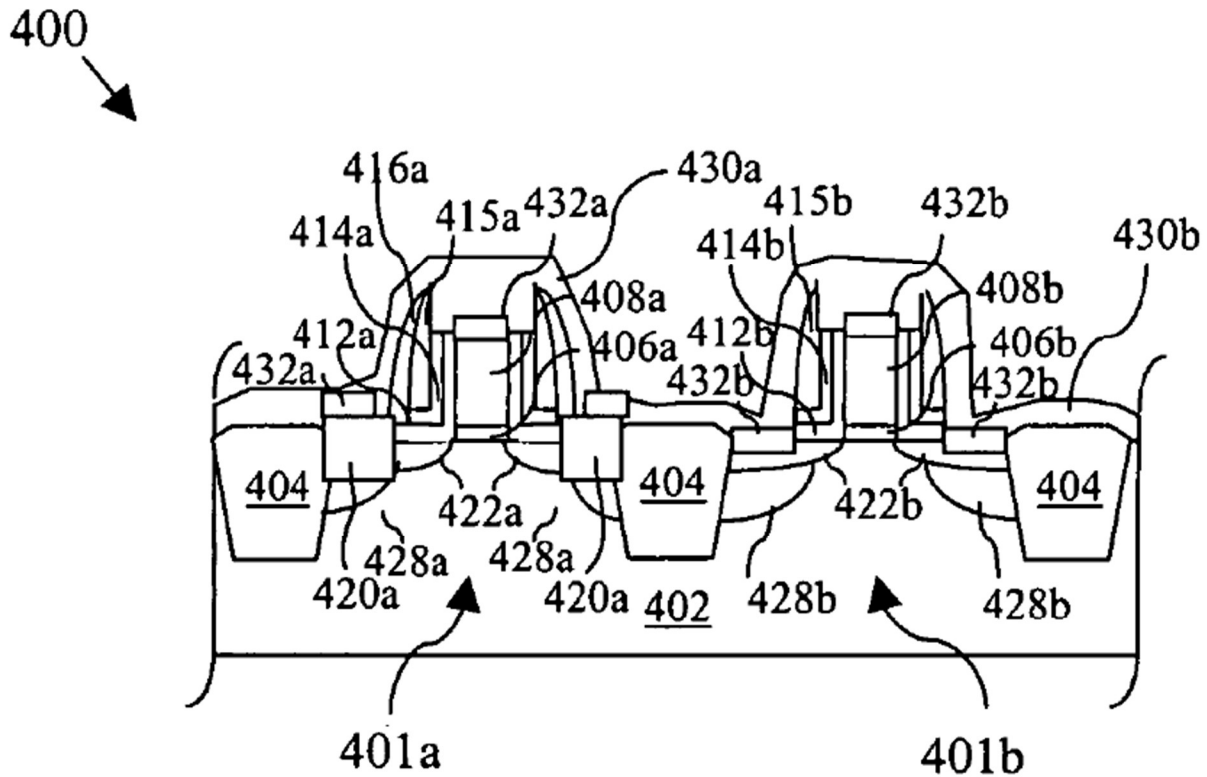


Alvarez, FIG. 9

C. Cheng

Cheng is prior art under pre-AIA §102(a), (b), (e). Since Cheng is in the same field as the '425 Patent (MISFETs) and reasonably pertinent to a problem the '425 Patent addresses (strain engineering and device manufacturing), Cheng is analogous. (Ex-1001, 1:15-7:54; Cheng ¶¶[0002]-[0003]; Ex-1003 ¶82.)

Cheng's PMOS device 401a includes SiGe source/drain regions 420a that "extend above the substrate" and compressively stress the channel. (Cheng ¶[0022], ¶[0065], Fig. 4j.) Etch stop layer 430a/430b may be a "tensile film" or "compressive film" made of "silicon nitride (Si_xN_y)."

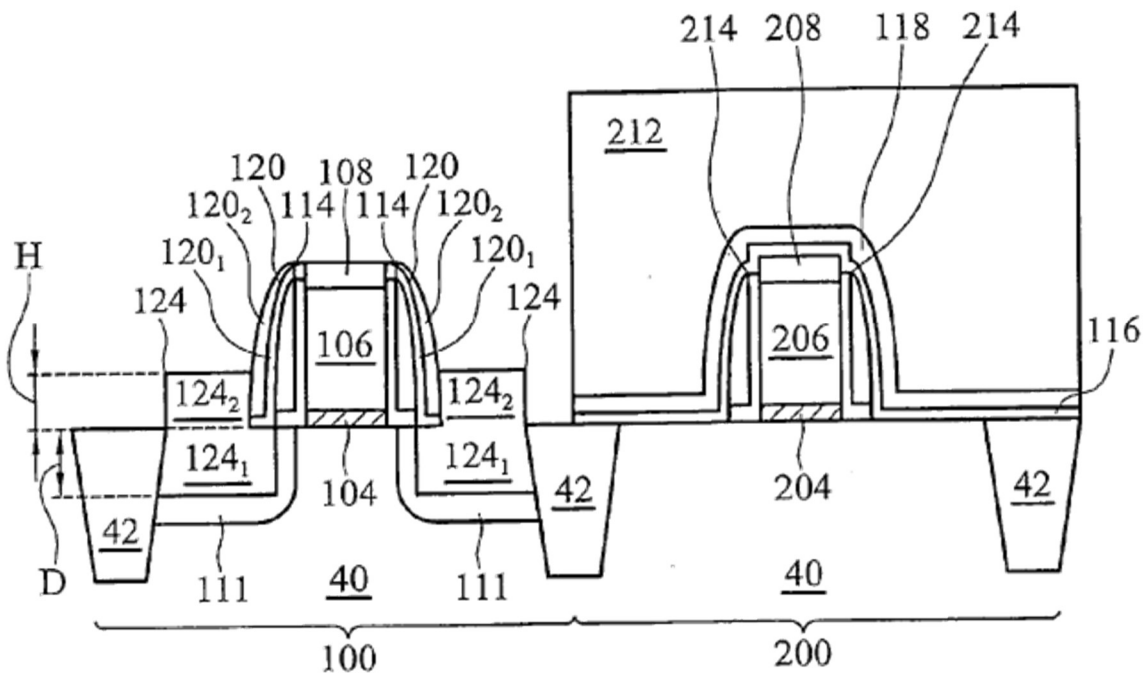


Cheng, Fig. 4j

D. Wang

Wang is prior art under pre-AIA §102(a), (b), (e). Since Wang is in the same field (MISFETs) and reasonably pertinent to a problem the '425 Patent addresses (strain engineering and device manufacturing), Wang is analogous. (Ex-1001, 1:15-7:54; Wang ¶¶[0002]-[0008]; Ex-1003 ¶85.)

Wang explains: “to strengthen the compressive stress applied by the silicon [SiGe] alloy regions 124 [in pMOS devices], the silicon alloy regions 124 preferably outgrow the top surface of the substrate 40, forming raised portions 124₂” about 10-70 nm high. (Wang ¶[0031], FIG. 9.)

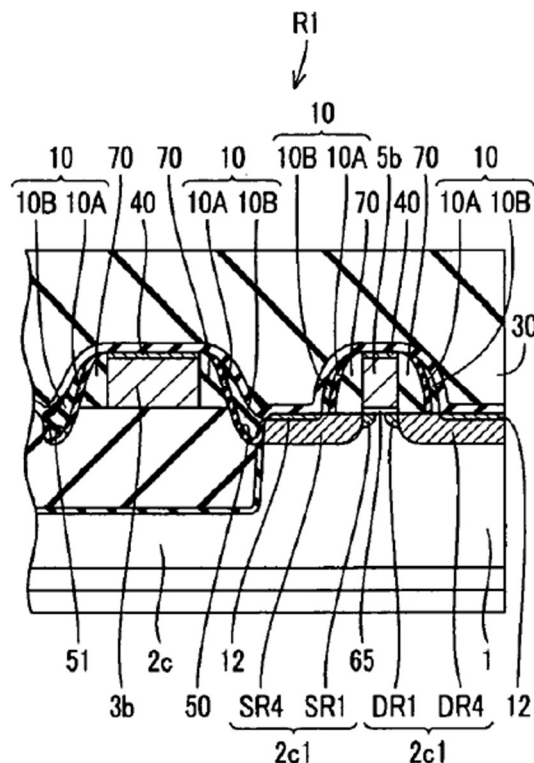


Wang, FIG. 9

E. Saito

(Ex-1001, 1:15-7:54, 10:61-11:9, 13:8-15; Saito, Abstract, ¶¶[0074]-[0079]; Ex-1003 ¶88.)

Saito discloses an SRAM circuit with PMOS and NMOS transistors. (Saito ¶¶[0056]-[0059], FIG. 1.) To prevent junction leakage, Saito teaches to fill recesses 50 in isolation regions 20A1 with oxide layer 10A and nitride layer 10B. (Saito ¶[0027], ¶¶[0074]-[0076], ¶¶[0112]-[0113], FIGS. 3, 12, 21.)

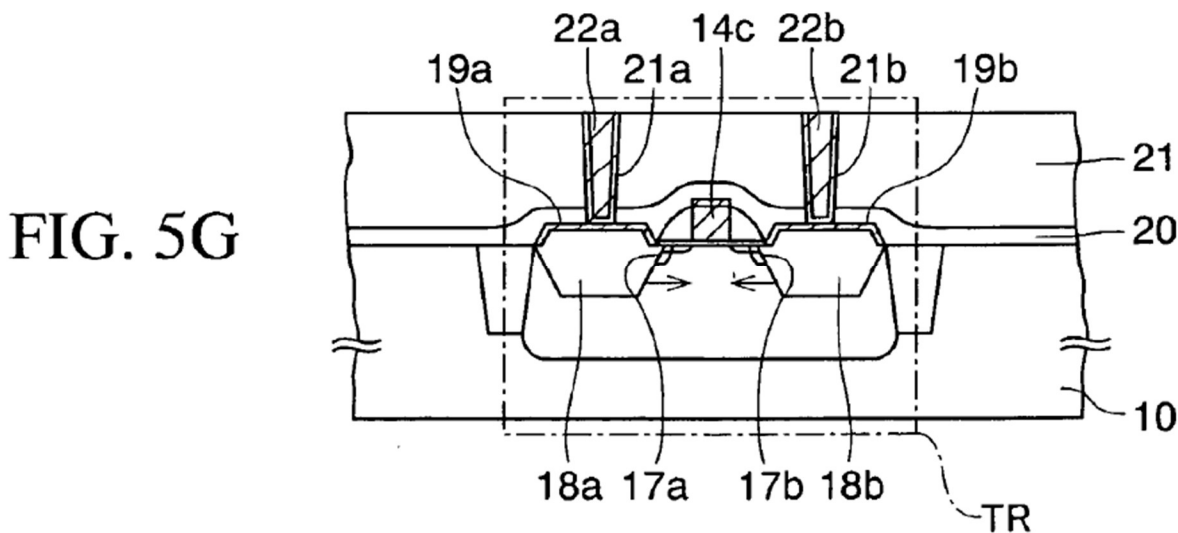


Saito, FIG. 21 (excerpted)

F. Fukutome

Fukutome is prior art under pre-AIA §102(a), (b), (e). Since Fukutome is in the same field (MISFETs) and reasonably pertinent to a problem the '425 Patent addresses (strain engineering and device manufacturing), Fukutome is analogous. (Ex-1001, 1:15-7:54; Fukutome ¶¶[0002]-[0012]; Ex-1003 ¶91.)

Fukutome discloses faceted SiGe “source/drain material layers 18a and 18b” grown to “positions higher than the surface of the silicon substrate” to suppress junction leakage and improve reliability. (Fukutome ¶[0100]; *see id.* ¶¶[0092]-[0096], FIGS. 5D-5G.) Silicon nitride layer 20 covers the substrate. (Fukutome ¶[0106], FIG. 5G.)



Fukutome, FIG. 5G

G. James

James is prior art under pre-AIA §102(a), (b). (Ex-1036; Ex-1003 ¶¶93.) Since James is in the same field (MISFETs) and reasonably pertinent to a problem the '425 Patent addresses (strain engineering and device manufacturing), James is analogous. (Ex-1001, 1:15-7:54; *generally* James; Ex-1003 ¶¶94.)

James describes commercial transistor structures, including in Intel's Prescott chips. (James, 1-5, Figs. 1-3, 5-12.) In Prescott, "[l]ocalized tensile stress is applied to the channels of NMOS devices by a highly stressed nitride" that "increases electron mobility." (James, 2, Figs. 5-6.) Prescott's "PMOS transistors (Figure 6) use epitaxial SiGe source/drains to create compressive stress," which "improves hole mobility." (*Id.*)

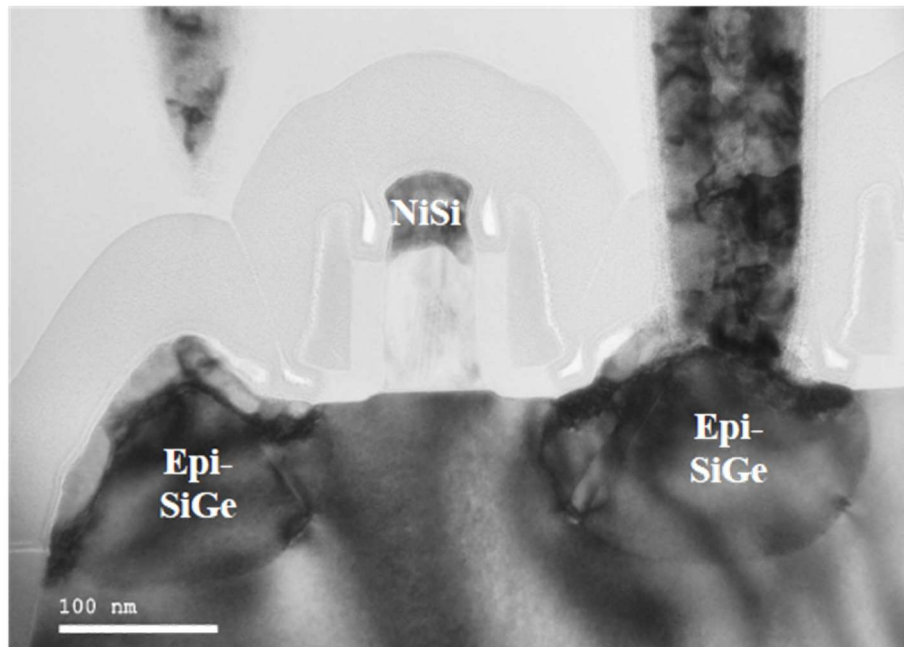


**Figure 6. Intel PMOS Transistor
James, Fig. 6**

H. Wolf

Wolf is prior art under pre-AIA §102(a), (b). (Ex-1037; Ex-1038.) Since Wolf is in the same field (MISFETs) and reasonably pertinent to a problem the '425 Patent addresses (device fabrication), Wolf is analogous. (Ex-1001, 1:15-7:54; *generally* Wolf; Ex-1003 ¶¶97.)

Wolf teaches an I-shaped “offset-spacer” to distance source-drain extensions from the channel to prevent “excessive leakage (due to larger short-channel effects that arise if the channel-length is too small)” and “yield[] optimum device characteristics.” (Wolf, 21-22, Fig. 5-25.)

V. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Grounds 1A-1B: Wu

1. Ground 1A: The Wu-Alvarez Combination Renders Obvious Claims 1, 3-5, 7-9, and 11-15

a. A POSITA Would Have Found the Wu-Alvarez Combination Obvious

A POSITA would have found it obvious to incorporate Alvarez’s stress-relief and stress-inducing layers in Wu’s device. (Ex-1003 ¶¶101-147.)

(1) A POSITA would have been motivated to combine Wu and Alvarez

Wu discloses “forming a strained CMOS transistor to improve CMOS transistor performance and reliability.” (Wu ¶[0009], FIGS. 1-7, 9-14.) Wu’s PMOS regions 31 include conventional features. (Wu ¶[0017], ¶[0023], ¶¶[0038]-[0039],

¶¶[0042]-[0043], FIGS. 1-7, 9-14.) To form PMOS source/drain regions, Wu teaches adding sacrificial layer 52 outside sidewalls 501A and 502A, then etching a recess 56 in which to grow SiGe layers 58 extending above the substrate. (Wu ¶¶[0018]-[0021], ¶¶[0039]-[0041], FIGS. 2-4, 10-12.) SiGe layer 58 “compress[es] the channel” to improve mobility. (*Supra* §II.B; Wu ¶¶[0021], ¶¶[0041], FIGS. 4, 12.)

As FIG. 14 shows, Wu teaches to remove sacrificial layer 52 and spacer 502A before forming spacer 512A, creating a gap between SiGe layer 58 and sidewalls 501A and 512A. (Wu ¶¶[0022]-[0024], ¶¶[0042]-[0043], FIGS. 5-7, 13-14.)

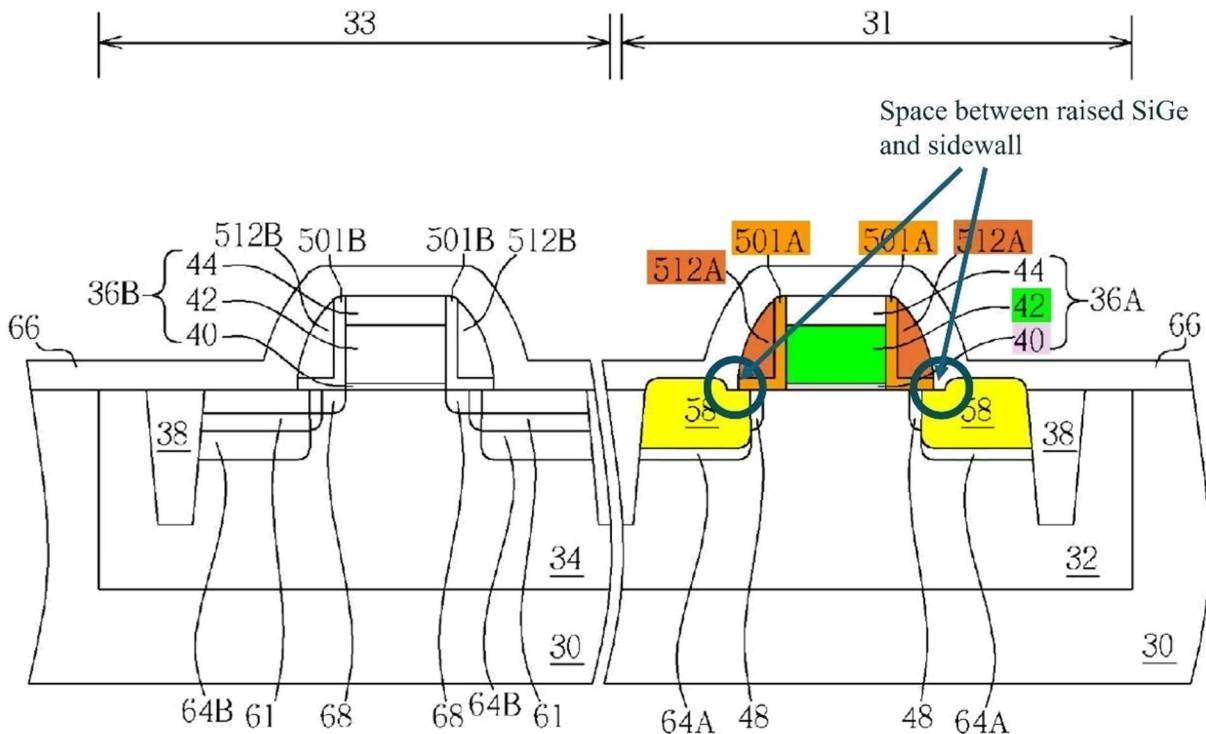


FIG. 14

Wu, FIG. 14

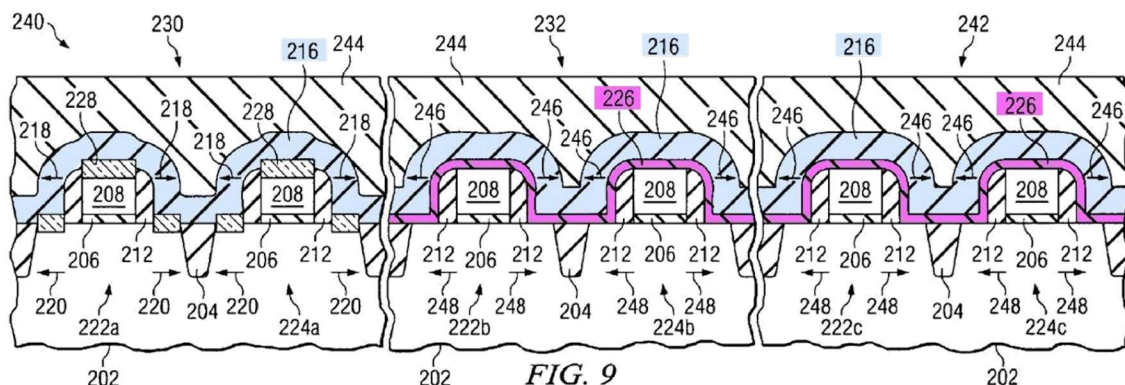
Wu then “form[s] a contact etch stop layer (CESL) 66” using a “strained silicon material” (SiN) over the gate structures (36A/36B), spacers (501A/501B and 512A/512B), and sources/drain regions (64A/64B). (Wu ¶[0025], ¶[0044], FIGS. 7, 14.) CESL 66 can be “a strained thin film upon a surface of the MOS transistor that exert[s] tensile stress or compressive stress” to “improv[e] carrier mobility and MOS transistor performance.” (Wu ¶[0005], ¶[0025]; *supra* §II.B; Ex-1003 ¶¶105-112.) Because Wu describes improved “carrier” mobility (not “electron” or “hole” mobility), CESL 66 can be either tensile or compressive. (Ex-1003 ¶¶111-112.)

As Alvarez shows, a POSITA would have found it obvious to impart tensile strain using CESL 66 to improve electron mobility (NMOS), while also including a stress-control layer to tune that tensile strain and selectively block silicide formation in certain circuit regions (e.g., non-silicide region 232 and stress-control region 242). (Ex-1003 ¶¶102-104, ¶¶113-115.) The asserted combination includes Wu’s transistors with Alvarez’s stress-control layer underlying a tensile CESL 66.

Alvarez explains: “Some NMOS FETs have demonstrated performance enhancement” by imparting “tensile stress to the channel region,” but “some PMOS FETs may suffer from decreased performance” when a tensile CESL is applied. (Alvarez ¶[0025]; Ex-1003 ¶116.) To mitigate adverse effects on PMOS, Alvarez discloses stress-controlling layers 226/326/426 and 350/450 underlying tensile CESL 216/316/416. (Alvarez ¶[0028], ¶¶[0032]-[0035], ¶¶[0045]-[0046], ¶[0055],

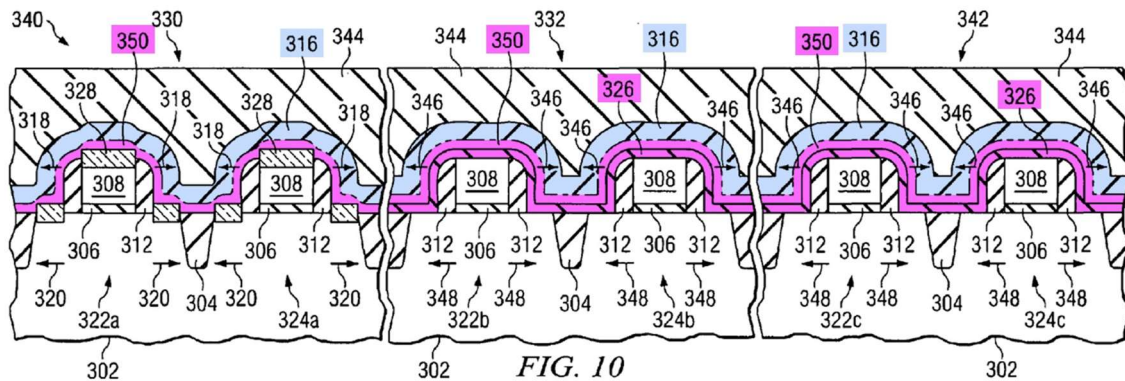
¶¶[0063]-[0068], ¶[0073], ¶[0075], ¶[0078], FIGS. 8-11.) This (a) reduces adverse effects from stress-inducing layer 216/316/416 on PMOS, (b) selectively blocks silicide formation, and (c) eliminates processing steps to streamline manufacturing. (Alvarez ¶[0037], ¶[0049], ¶[0061], ¶¶[0070]-[0075], ¶[0078], ¶[0081], FIGS. 9-11; Ex-1003 ¶117.)

Such benefits may be interrelated. For example, Alvarez uses stress-control layer 226/326/426 to selectively block silicide in regions 232/242 of FIGS. 9-10, thus performing two functions. (Alvarez ¶[0035], ¶[0045], ¶[0078], FIGS. 9-10.) Leaving stress-controlling layers 226/326/426 and/or 350/450 intact when depositing a tensile CESL 216/316/416, as in FIGS. 9-11, reduces the number of process steps (and manufacturing costs) while accounting for different performance requirements in circuit regions 230, 232, and 242. (Alvarez ¶[0027], ¶¶[0032]-[0033], ¶[0045], ¶[0074], ¶[0078]; Ex-1003 ¶118.)



Alvarez, FIG. 9⁵

⁵ 222x are NMOS; 224x are PMOS. (Alvarez ¶[0025], ¶[0028], ¶[0063].)



Alvarez, FIG. 10 (3xx corresponds to 2xx in FIG. 9)

To achieve these benefits, a POSITA would have found it obvious to (a) implement Wu’s strained CESL 66 with tensile strain to improve NMOS mobility and (b) include Alvarez’s stress-controlling layer in selected regions (e.g., regions 232/242) to (i) mitigate the adverse effects of tensile CESL 66 on PMOS carrier mobility, (ii) prevent unwanted silicide formation in certain regions, and (iii) lower costs. (Alvarez ¶[0037], ¶[0049], ¶[0061], ¶¶[0070]-[0075], ¶[0078], ¶[0081], FIGS. 9-11; Ex-1003 ¶119.)

Alvarez explains: “many different types of transistors 122 and 124 are formed across a workpiece 102 surface, with the different types of transistors 122 and 124 having different operating parameters and requirements.”⁶ (Alvarez ¶[0027].)

⁶ The ’425 Patent similarly discloses “pMIS region[s]” and “nMIS region[s]” and explains different transistor variations may be used in different circuits, such as “analog,” “peripheral,” or “logic” circuits. (Ex-1001, 8:46-61.)

Alvarez teaches to selectively form silicides only in certain regions “due to the performance requirements of transistors in the particular regions.” (Alvarez ¶[0032].) For example, transistors in silicide regions require “increased conductivity of the gates 108, source and drain regions,” whereas others “do not . . . , and thus the masking material layer 126 is used to prevent silicide 128 formation” in those regions. (*Id.*) Wu likewise discloses an *optional* “silicide process (salicide process).” (Wu ¶[0024]; *see id.* ¶[0043].) As Alvarez demonstrates, a POSITA would have recognized the benefit of siliciding Wu’s transistors in certain circuits but not others. (Ex-1003 ¶¶117-121.)

A POSITA would have recognized “it is important to work to improve nMOS transistors” via tensile CESL. (Ex-1022, 2; Ex-1003 ¶122.) Alvarez achieves this by tuning the stress-control layer to reduce, but not eliminate, tensile stress from the CESL. (Alvarez ¶[0049], ¶¶[0053]-[0055], Tbl. 1; Ex-1003 ¶123.) That is, tensile strain can be applied to the NMOS without adversely affecting the PMOS by “tun[ing]” stress-inducing layer 216 and stress-controlling layer 226 “to achieve the amount of control desired on the stress of the underlying material layer, e.g., such as the channel regions of the transistors 222b, 224b, 222c, and 224c,” without incurring additional capital costs. (Alvarez ¶¶[0053]-[0055], ¶[0080]; James, 2, 5.) By coordinating stress-inducing and stress-controlling layers, a POSITA would have

reasonably expected to achieve these benefits. (Alvarez ¶¶[0037], ¶[0049], ¶[0061], ¶¶[0070]-[0075], ¶[0078], ¶[0081], FIGS. 9-11; Ex-1003 ¶¶122-124, ¶¶136-137.)

Such techniques were well-known. (Ex-1003 ¶¶125-129.) Those in the art knew to place a stress-relief layer underneath a tensile CESL to mitigate adverse effects on PMOS. (*Supra* §§II.B-II.C; Wu ¶[0005]; Alvarez ¶[0043], ¶[0049], ¶[0054], ¶¶[0065]-[0066], ¶[0068], ¶[0074], ¶¶[0077]-[0078], FIG. 9; Ex-1030, 9:10-29; Ex-1029 ¶¶[0034]-[0035], ¶[0038], Figs. 2, 14, 15; Ex-1033 ¶[0037]; Ex-1031 ¶[0029], ¶¶[0046]-[0067], FIGS. 2-5; Ex-1032 ¶¶[0022]-[0031], Figs. 1B-1F.) Because Wu's FIG. 14 shows CESL 66 near the PMOS channel, a POSITA would have been motivated to add a buffer layer like Alvarez's strain-controlling layers 226/326/426 and/or 350/450. (Alvarez ¶[0025], ¶¶[0063]-[0068], ¶¶[0070]-[0072], FIGS. 9-11; Ex-1003 ¶¶130-133.) A POSITA would have expected this to improve both NMOS and PMOS performance by "tun[ing]" stress "to achieve the amount of control desired on the stress of the underlying material layer." (Alvarez ¶[0053]; *see id.* ¶[0049], ¶¶[0053]-[0055], ¶[0061], ¶¶[0066]-[0067], ¶¶[0078]-[0081]; Ex-1030, 8:59-9:43, FIGS. 7-9; Ex-1029 ¶[0034], ¶[0042], Fig. 14; Ex-1033 ¶[0037]; Ex-1031 ¶[0067]; Ex-1032 ¶[0030]; Ex-1003 ¶131, ¶¶136-137.)

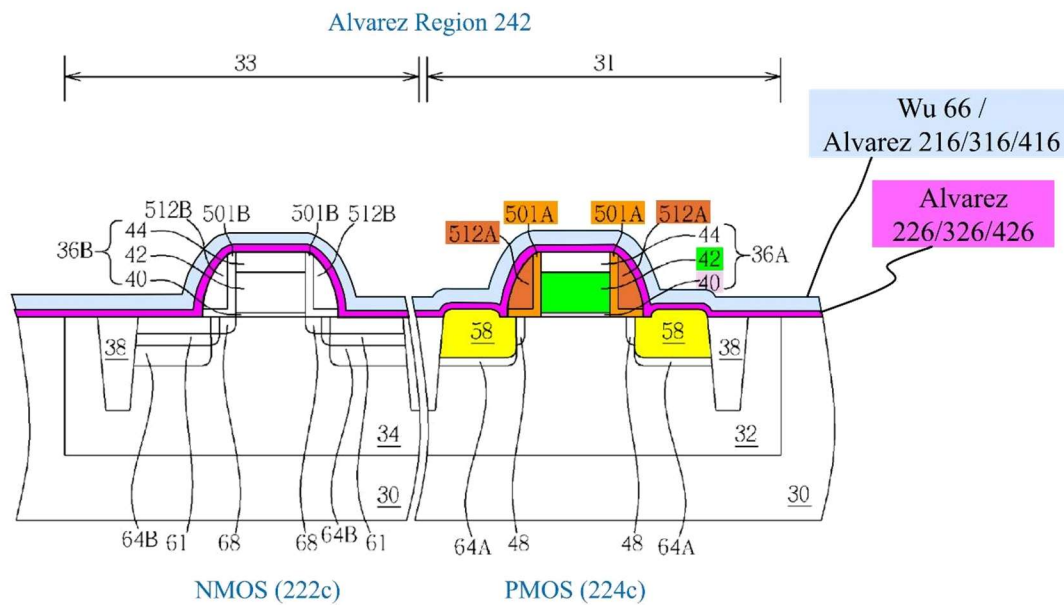


Figure A

A POSITA thus would have been motivated to add a stress-controlling layer to Wu’s MOSFETs, as Figure A shows above.⁷ (Ex-1003 ¶133.) A POSITA would have deposited the stress-controlling layer (magenta) after forming SiGe regions 58 (yellow) and gate sidewalls 512 (dark orange) but before depositing tensile CESL 66 (light blue)—the order Alvarez discloses. (*Id.*) A POSITA would have known this mitigates adverse effects of the tensile CESL on PMOS transistors and prevent silicide formation in selected circuit regions (e.g., regions 232/242), while also accounting for different performance requirements (e.g., conductivity requirements)

⁷ To maximize beneficial stresses, Alvarez’s stress-control layer may be removed from NMOS devices (e.g., in regions 232/242). (Alvarez [0065]-[0068], FIG. 11.)

This Petition also contemplates such embodiments. (Ex-1003 ¶133 n.11.)

and streamlining manufacturing. (Alvarez ¶[0027], ¶¶[0032]-[0033], ¶[0037], ¶[0045], ¶¶[0063]-[0068], ¶¶[0070]-[0075], ¶[0078]; Ex-1003 ¶¶117-119, ¶¶136-137.)

A POSITA would have found the proposed combination obvious, as Figures A (above) and B (below) show, wherein Figure A applies in certain circuit regions (equivalent to Alvarez's regions 232/242) but not in others (equivalent to Alvarez's region 230/330)⁸:

- Transistor 224c in region 242 of Figures A and B maps onto claims 1, 4-5, and 7-9. (*Infra* §V.A.1.b.)
- Alternatively, transistor 324a in region 330 maps onto claims 1 and 3. (See Alvarez ¶¶[0063]-[0064], FIG. 10; Figure A' discussed *infra* §V.A.1.b(1), §V.A.1.b.)
- Transistor 222a in region 230 of Figure B (similar to transistor 222c in Figure A but with Wu's optional silicide and no stress-controlling film) maps onto claims 11-12. (*Infra* §V.A.1.i.)
- Transistor 224b in region 232 of Figure B (similar to transistor 224c in Figure A) maps onto claims 13-15. (*Infra* §V.A.1.k.)

(Ex-1003 ¶¶133-135.)

⁸ Alvarez's FIGS. 9 and 10 show the corresponding regions.

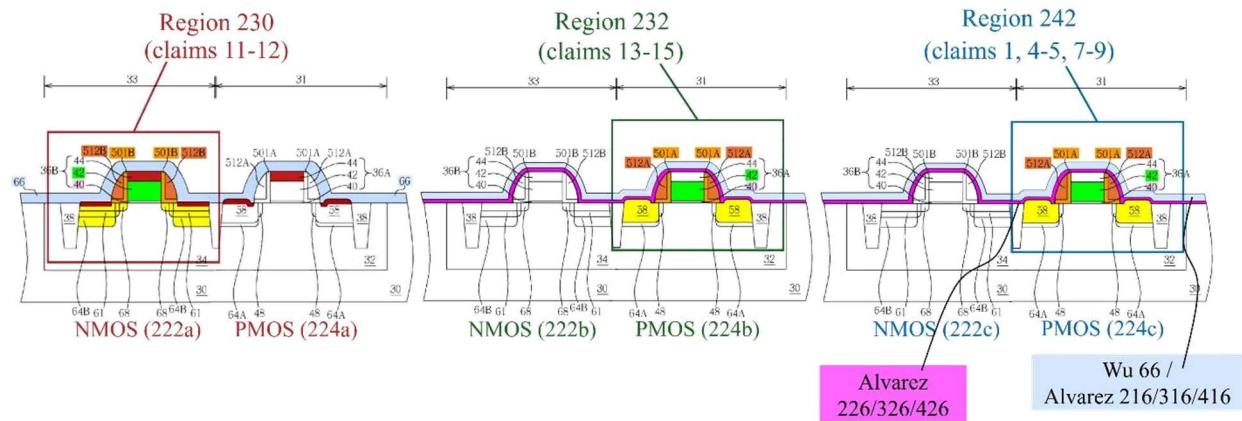
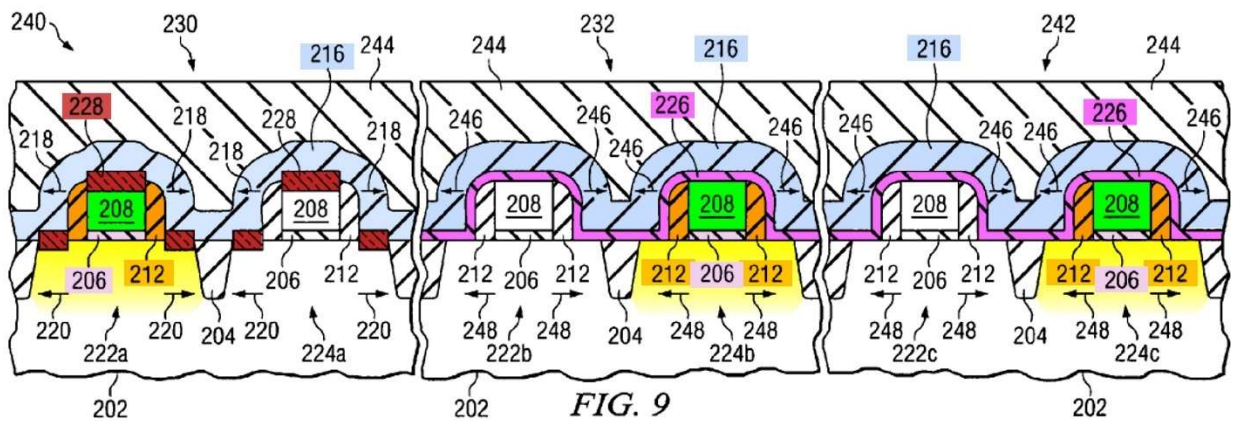


Figure B



Alvarez, FIG. 9

Although the discussion above generally describes mitigating the adverse effects of tensile CESL on PMOS, Wu and Alvarez also disclose and render obvious mitigating adverse effects of compressive CESL on NMOS, e.g., when the NMOS employs epitaxial SiC source/drain layers. (Alvarez ¶[0065], ¶[0067]; Wu, ¶[0037], ¶[0057]; *infra* §V.A.1.h.) A POSITA would have understood the same benefits accrue, except the roles of compressive and tensile strain reverse. (Ex-1003 ¶138.)

**(2) A POSITA would have reasonably expected to
succeed in combining Wu and Alvarez**

A POSITA would have reasonably expected to succeed in (a) adding a stress-controlling layer to Wu's devices and (b) implementing Wu's CESL 66 with tensile strain, as in one proposed combination. (Ex-1003 ¶¶139-146.)

Such a combination requires only conventional steps: (a) forming a stress-controlling layer (as Alvarez teaches) in the desired device regions, e.g., regions 232/242 (Alvarez ¶¶0027], ¶¶0032], ¶¶0035], ¶¶0045], ¶¶0063]-[0068], ¶¶0078], FIGS. 8-11) and (b) forming a stress-inducing CESL 66 to impart tensile strain (as Alvarez teaches) by using appropriate deposition conditions (Ex-1024 ¶¶0099]-[0100], Tbl. V; Ex-1003 ¶140.)

Adding a stress-controlling layer where desired would have involved nothing more than well-known deposition and patterning techniques. (Alvarez ¶¶0044], ¶¶0052]-[0053], ¶¶0063]-[0068]; Ex-1030, 9:10-35; Ex-1029 ¶¶0036]-[0037], ¶¶0042], ¶¶0046]; Ex-1033 ¶¶0037]; Ex-1031 ¶¶0029], ¶¶0046]-[0067], FIGS. 2-5; Ex-1032 ¶¶0022]-[0031], Figs. 1B-1F; Ex-1003 ¶¶141-144.) A POSITA would have understood the result to be a stress-controlling layer formed between Wu's raised SiGe layers and gate sidewalls because, as Alvarez shows, the stress-controlling layer would blanket the exposed PMOS devices. (Wu ¶¶0042], FIG. 14; Alvarez ¶¶0043]-[0049], ¶¶0052], ¶¶0063]-[0068], ¶¶0070]-[0071], ¶¶0073]-

[0075], ¶[0078], FIGS. 6-11; Ex-1030, 9:10-29, FIG. 8; Ex-1035 ¶¶[0052]-[0053], FIGS. 1U-1W; Ex-1003 ¶141.)

Depositing a tensile (or compressive) nitride CESL was also well-known, conventional, and easily implemented. (*Supra* §II.B; Ex-1024 ¶¶[0099]-[0100], Tbls. IV-V; Alvarez ¶[0047]; Wu ¶[0005]; James, 2, 5, Fig. 6; Ex-1029 ¶¶[0016]-[0017], ¶¶[0029]-[0030], ¶[0038], ¶[0042], ¶[0051], Figs. 1, 2, 14, 15; Ex-1022, 1-2; Ex-1023 ¶[0003]; Ex-1025 ¶[0003]; Ex-1003 ¶143.)

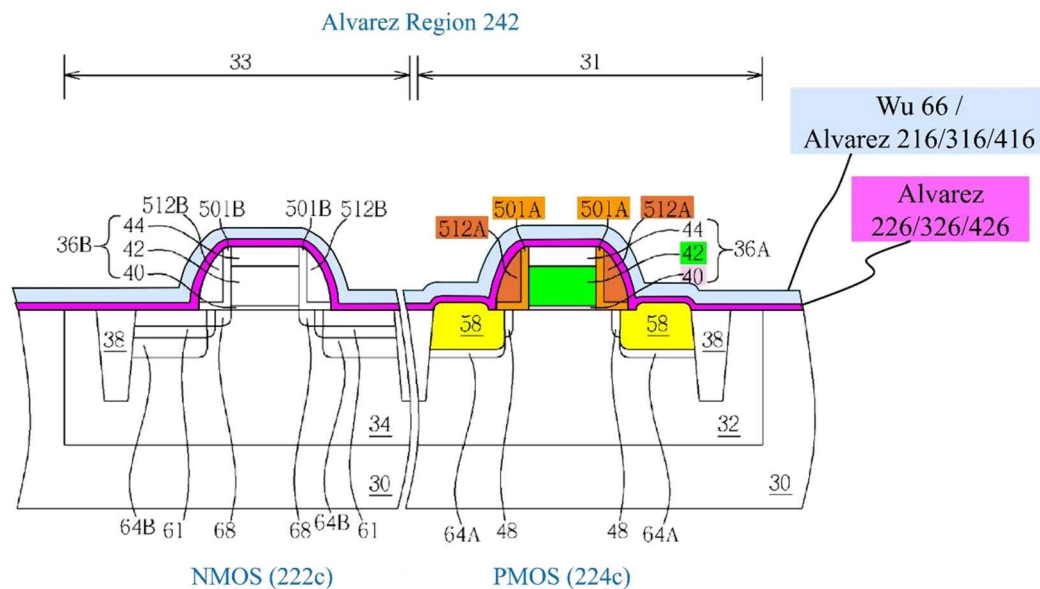


Figure A

Placing a stress-controlling layer underneath a tensile strain layer was also known. (*Supra* §§II.B-II.C; Ex-1003 ¶144.) Consistent with Alvarez's teachings, a POSITA would have found it obvious to deposit a stress-controlling layer after forming Wu's sidewall spacer 512A and before depositing a tensile stress-inducing CESL 66, as Figure A shows. (Alvarez ¶¶[0043]-[0049], ¶¶[0063]-[0068],

FIGS. 5-11; Wu ¶¶[0043]-[0044], FIGS. 13-14; Ex-1003 ¶¶144-145.) Doing so would have been expected to achieve the ordinary and expected result of buffering CESL strain, among other benefits. (*Supra* §§II.B-II.C, §V.A.1.a(1); Ex-1003 ¶146.)

A POSITA would have found this combination obvious because it (a) combines known prior-art elements (Wu's MOSFET structures and Wu's and Alvarez's teachings to use a strained CESL and stress-controlling layer) according to known methods (oxide deposition followed by strained nitride deposition) to yield predictable results (strained CESL and a buffer oxide that mitigates stress and inhibits silicide formation); (b) using known techniques (depositing a stress-controlling layer, as Alvarez instructs, that forms in the space between raised epitaxial regions and gate sidewalls, then depositing strained CESL) to improve similar devices (Wu's MOSFETs) in the same way (by improving carrier mobility, reducing manufacturing steps, lowering costs, and/or selectively blocking silicide); (c) applying these known techniques to improve Wu's known device and yield predictable results (improved carrier mobility, streamlined manufacturing, reduced costs, and/or selectively blocked silicide); and (d) applying a known teaching, motivation, or suggestion in the prior art (described above) (*supra* §§II.B-II.C, §V.A.1.a(1)) to arrive at the claimed invention. (*KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-21 (2007); Ex-1003 ¶147.)

b. Independent Claim 1

(1) [1Pre]: “A semiconductor device”

Wu discloses “a strained CMOS transistor.” (Wu ¶[0009]; *see id.* ¶[0017], ¶¶[0023]-[0024], ¶[0038], ¶¶[0042]-[0043], FIGS. 1-7, 9-14.) Figure A shows one embodiment of the proposed combination. (*Supra* §V.A.1.a; Ex-1003 ¶149.)

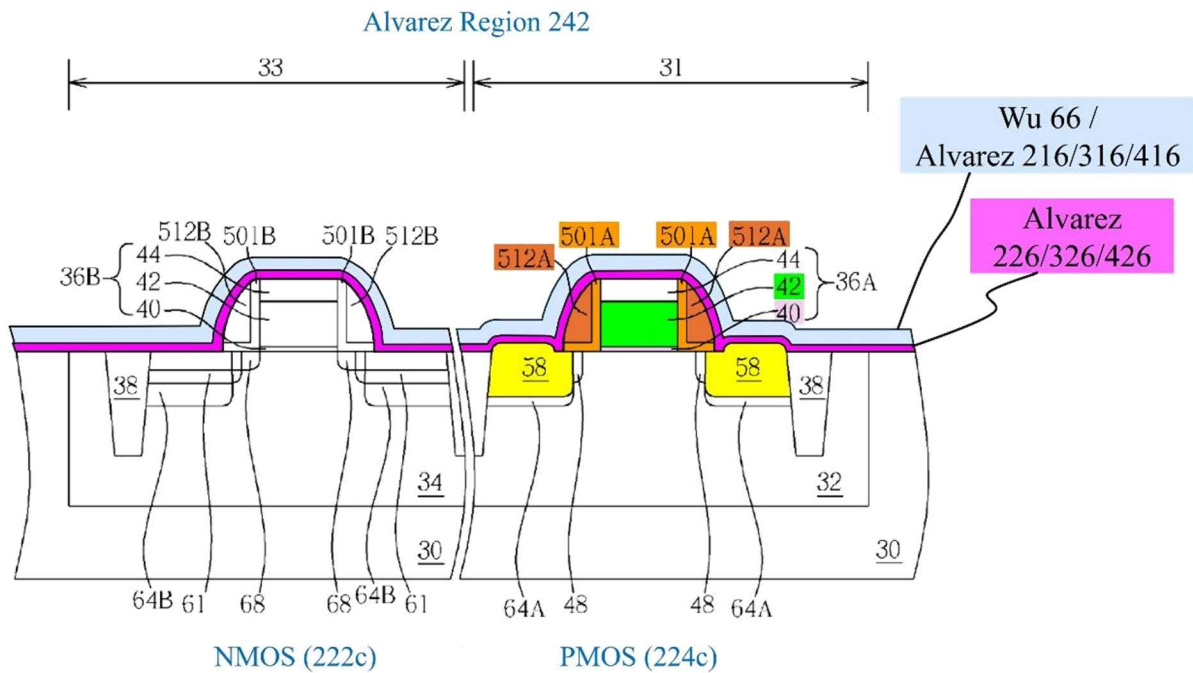


Figure A

Figure A' shows an alternative embodiment with silicided source/drain and gate electrodes. (*Infra* §V.A.1.c (claim 3); Ex-1003 ¶150.)

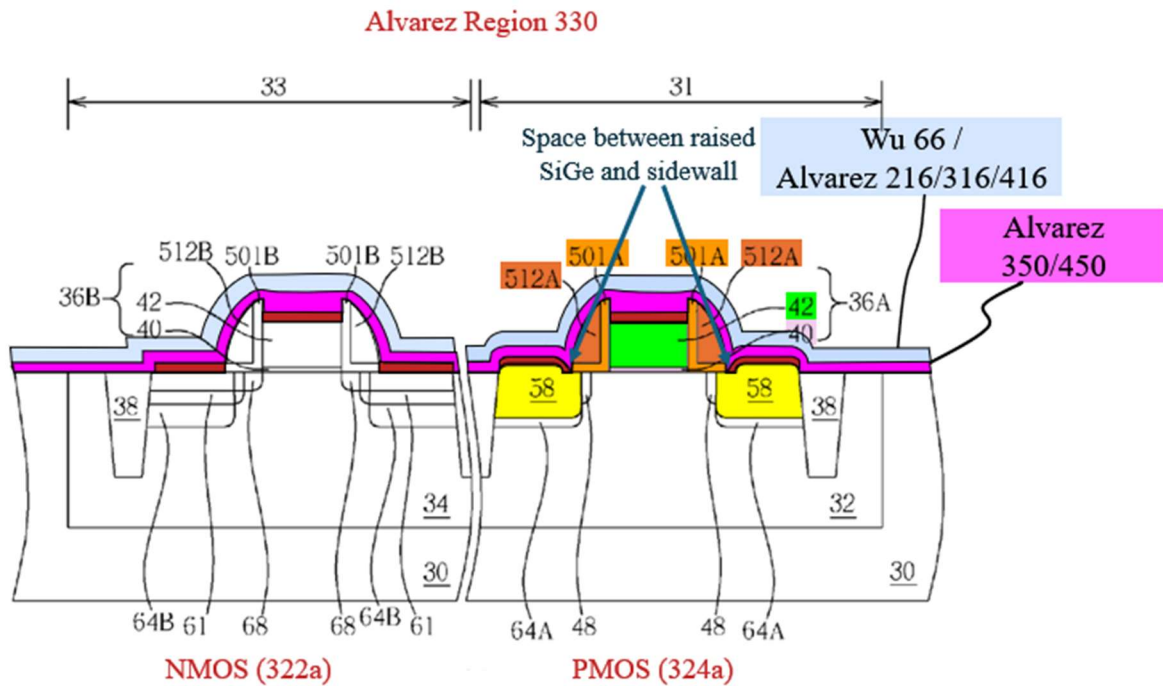


Figure A'

(2) [1A]: “a first MIS transistor, ... includ[ing]:”

Wu discloses a first MIS transistor, e.g., in PMOS regions 31. (Wu ¶[0017], ¶[0023], ¶¶[0027]-[0036], ¶[0038], ¶¶[0042]-[0043], ¶¶[0046]-[0055], FIGS. 1-7, 9-14; Ex-1003 ¶¶151-152.)

(3) [1B]: “a first gate insulating film formed on a first active region in a semiconductor substrate”

Wu discloses a “gate dielectric insulating layer 40” on a first active region, e.g., PMOS regions 31, in “semiconductor substrate 30.” (Wu ¶[0017], ¶¶[0038]-[0039], FIGS. 7, 14; Ex-1003 ¶153.)

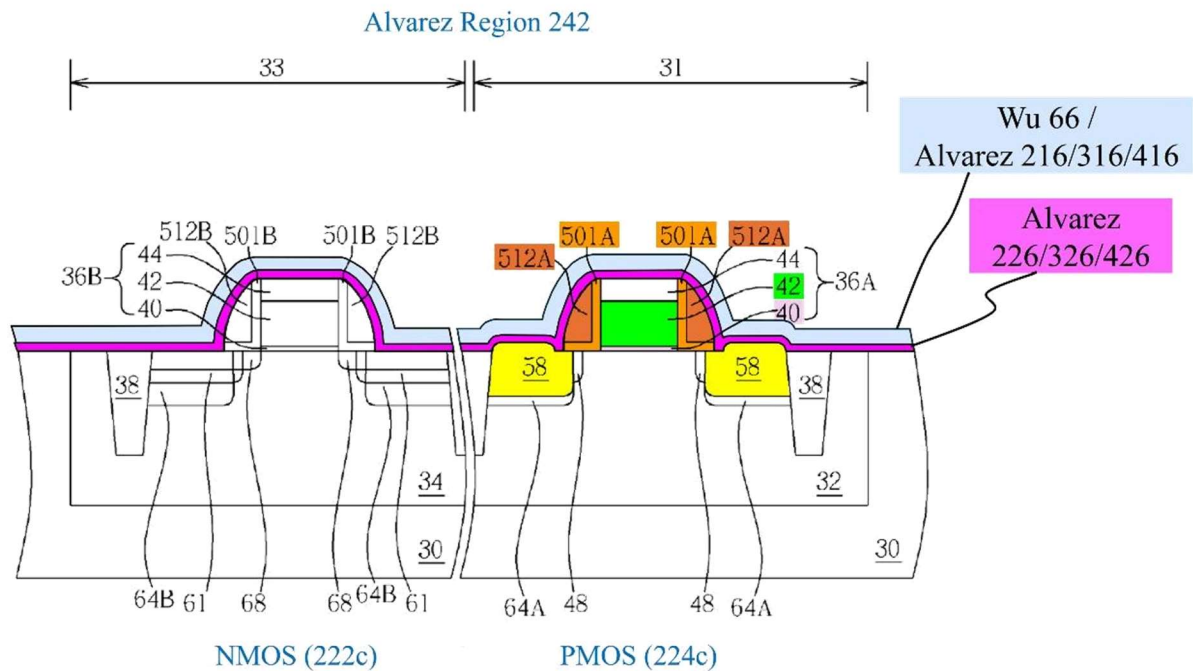


Figure A

(4) [1C]: “a first gate electrode formed on the first gate insulating film”

Wu discloses a first gate electrode (gate 42) formed on the first gate insulating film (gate dielectric 40) (*see* Figure A). (Wu ¶[0017], FIGS. 7, 14; Ex-1003 ¶¶154-155.)

(5) [1D]: “a first sidewall spacer formed on a side surface of the first gate electrode”

Wu discloses a first sidewall spacer comprising oxide layer 501A⁹ “formed on the sidewalls” of PMOS gate structure 36A, including gate 42 (*see* Figure A). (Wu ¶[0024]; *see id.* ¶[0017], FIGS. 7, 14; Ex-1003 ¶¶156-157.)

⁹ *Infra* note 10.

- (6) [1E]: “a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region”

Wu discloses a first source/drain region comprising p-type “epitaxial layer 58 of silicon germanium” in the first active area (PMOS region 31) (*see* Figure A). (Wu ¶¶0021]; *see id.* ¶¶0019], ¶¶0041], FIGS. 7, 14; Ex-1003 ¶¶158-160.) SiGe (silicon compound) layer 58 grows in a trench (recess 56), located beside gate structure 36A next to first sidewall spacer 501A¹⁰ in PMOS region 31, and “compress[es] the channel” (causing first, compressive stress in a gate length direction of a channel region). (Wu ¶¶0020]-[0021], ¶¶0031], ¶¶0040]-[0041], ¶¶0050], FIGS. 3-7, 11-14; Ex-1003 ¶¶159.)

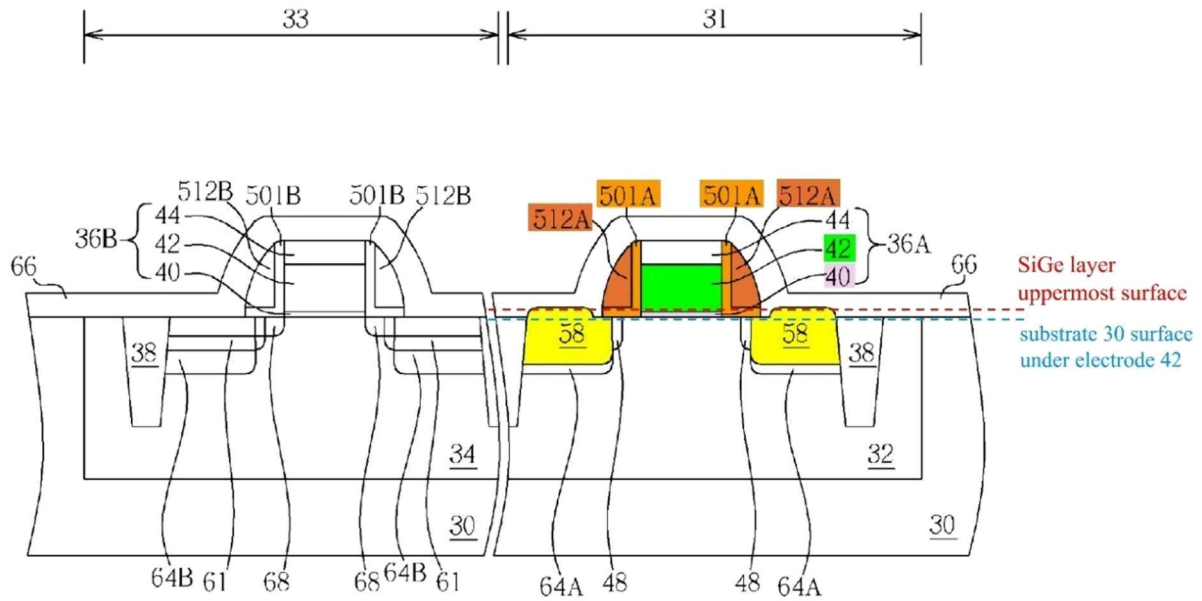
¹⁰ Wu’s SiGe layer 58 is “formed” before spacer 512A exists. If the “first sidewall spacer” need not exist when the first source/drain region is “formed,” the “first sidewall spacer” may further include Wu’s spacer 512A. (Wu ¶¶0024]-[0025], ¶¶0043]-[0044]; Ex-1003 ¶¶159 n.13.)

- (7) [1F]: “a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress”

Wu discloses a strained “contact etch stop layer (CESL) 66 on the surface of the gate structures 36A, 36B, the second spacers 512A, 512B, and the sources/drains 64A, 64B” (*see* Figure A). (Wu ¶[0025], ¶[0044], FIGS. 7, 14.) Both Wu and Alvarez teach a silicon nitride CESL. (Wu ¶[0025]; Alvarez ¶[0047].) As Alvarez demonstrates, a POSITA would have found it obvious for Wu’s silicon nitride CESL to cause tensile stress (opposite the SiGe compressive stress). (Alvarez ¶¶[0048]-[0049], ¶[0054], ¶¶[0065]-[0066], ¶[0069], Tbl. 1, FIGS. 9-11; *supra* §V.A.1.a; Ex-1003 ¶¶161-163.)

- (8) [1G]: “an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode”

SiGe layer 58 “project[s] from the top surface of the semiconductor substrate 30.” (Wu ¶[0021], ¶[0041], FIGS. 7, 14.) Wu’s FIGS. 4-7 and 12-14 show the top surface of SiGe layer 58 extending above substrate 30 (*see* Figure A). (Wu ¶[0021], ¶[0041], FIGS. 4-7, 12-14; Ex-1003 ¶¶164-165.)



Wu, FIG. 14

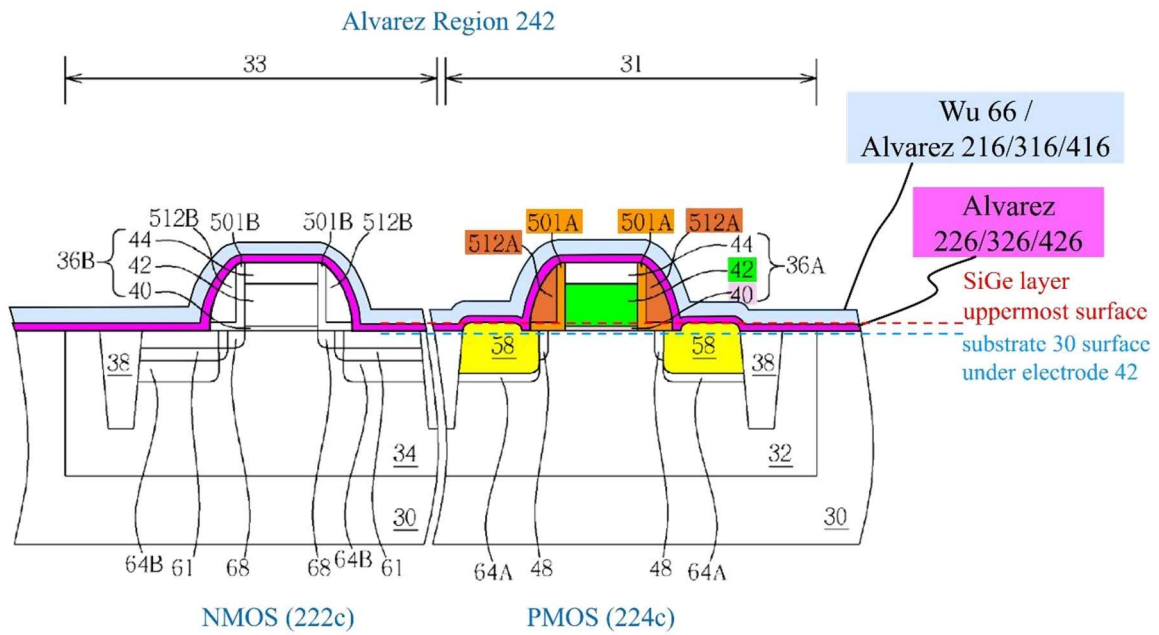


Figure A

(9) [1H]: “a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer”

The combination includes a first stress-relief film (magenta) (analogous to Alvarez’s stress-controlling layer(s)) formed in a space between SiGe layer 58 and first sidewall spacer 501A¹¹ created by removing sacrificial layer 52 (see Figure A). (Wu, FIGS. 6, 13, 14; *supra* §V.A.1.a; Ex-1003 ¶166.) According to Alvarez, stress-control layer 226/326/426 may be silicon oxide. (Alvarez ¶[0043], ¶¶[0063]-[0065], FIGS. 9-11.)

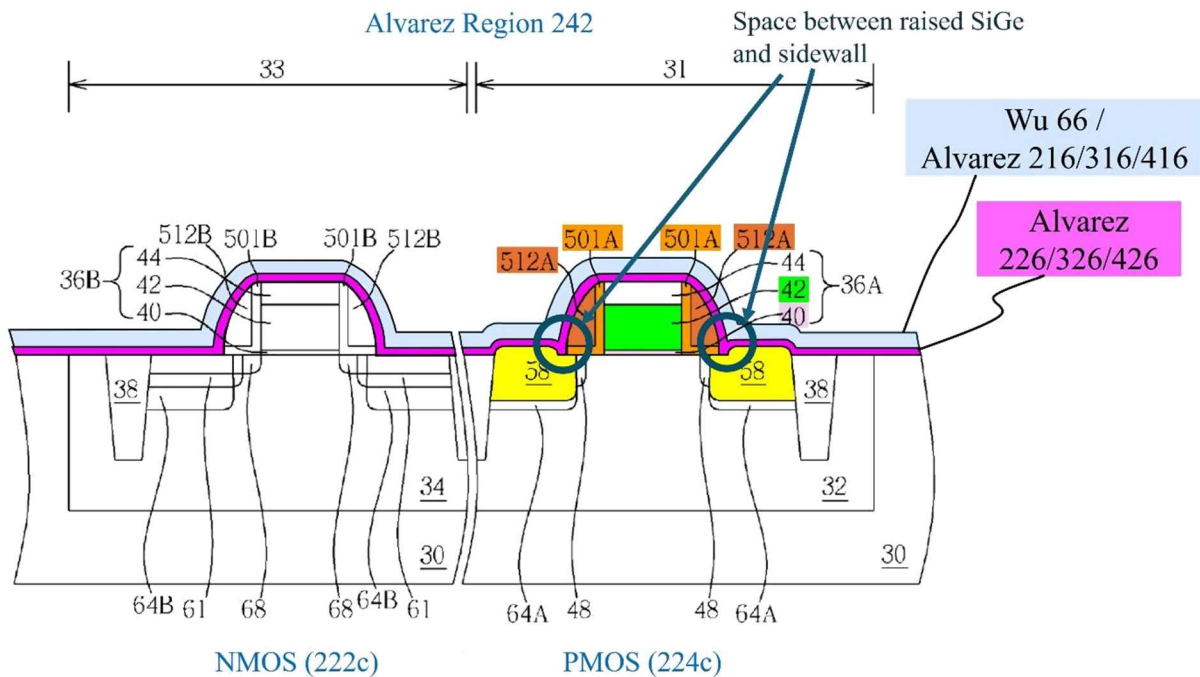


Figure A

¹¹ *Supra* note 10.

(10) [1I]: “the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween”

The combination includes the first stress-relief film (stress-controlling layer 226/326/426 (magenta)) formed on the side surface of the first gate electrode (PMOS gate electrode 42, green) with first sidewall spacer 501A¹² (orange) interposed therebetween. (*Supra* §V.A.1.a.) The first stress-relief film forms on the sides of gate electrode 42, including in the space between the first sidewall spacer 501A¹³ and SiGe layer 58, with the sidewall spacer between the stress-relief film and gate electrode (*see* Figure A). (Ex-1003 ¶¶167-168.)

(11) [1J]: “the first stress-relief film is not in direct contact with the side surface of the first gate electrode”

The first stress-relief film (magenta) does not directly contact a side surface of gate electrode 42 (green) because the sidewall spacer (orange) separates them. (*see* Figure A). (*Supra* §V.A.1.a, §§V.A.1.b(9)-V.A.1.b(10); Ex-1003 ¶¶169-170.)

¹² *Supra* note 10.

¹³ *Id.*

- c. **Claim 3: “The semiconductor device of claim 1, further comprising: a first silicide layer formed on the first gate electrode; and a second silicide layer formed on the first source/drain region which includes the silicon compound layer”**

The alternative mapping in Figure A' (showing a silicide region like Alvarez's region 330) includes a stress-control film 350/450 (first stress-relief film) “compris[ing] similar materials, dimensions, and deposition methods and parameters as described for ... stress-controlling material 226.” (Alvarez ¶[0064].) It overlays Wu's optional “silicide layer[s]” (burgundy) formed both on the “gate structures” (first silicide layer) and “surfaces of the [SiGe] source/drain” regions (second silicide layer). (Wu ¶[0024], ¶[0043]; see Alvarez ¶[0064], FIG. 10.) Again, stress-control film 350/450 would have been obvious for tuning stress in region 330, and the silicide reduces contact resistance. (*Supra* §V.A.1.a; Ex-1003 ¶¶172-179.)

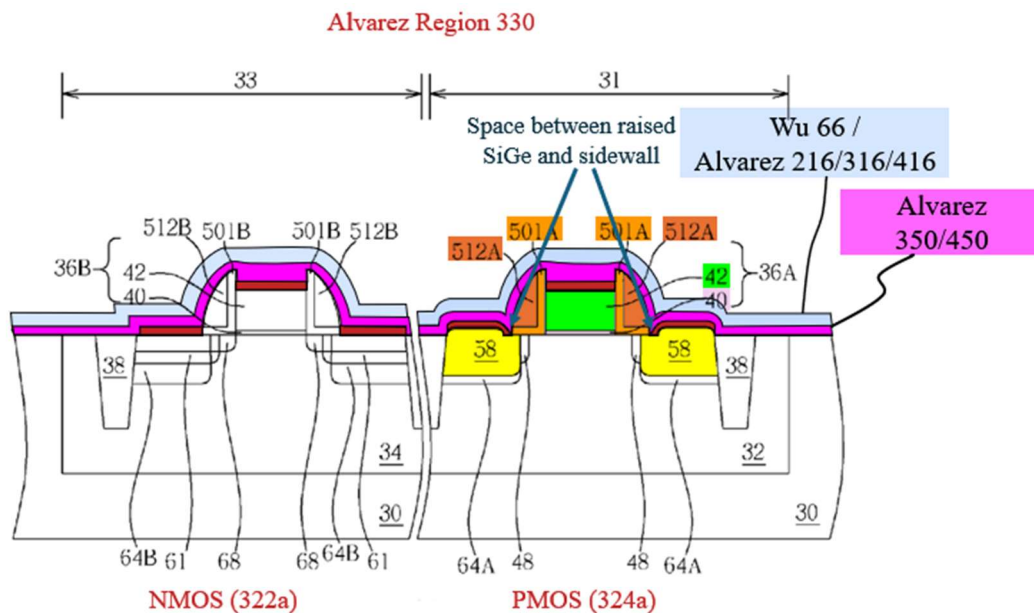
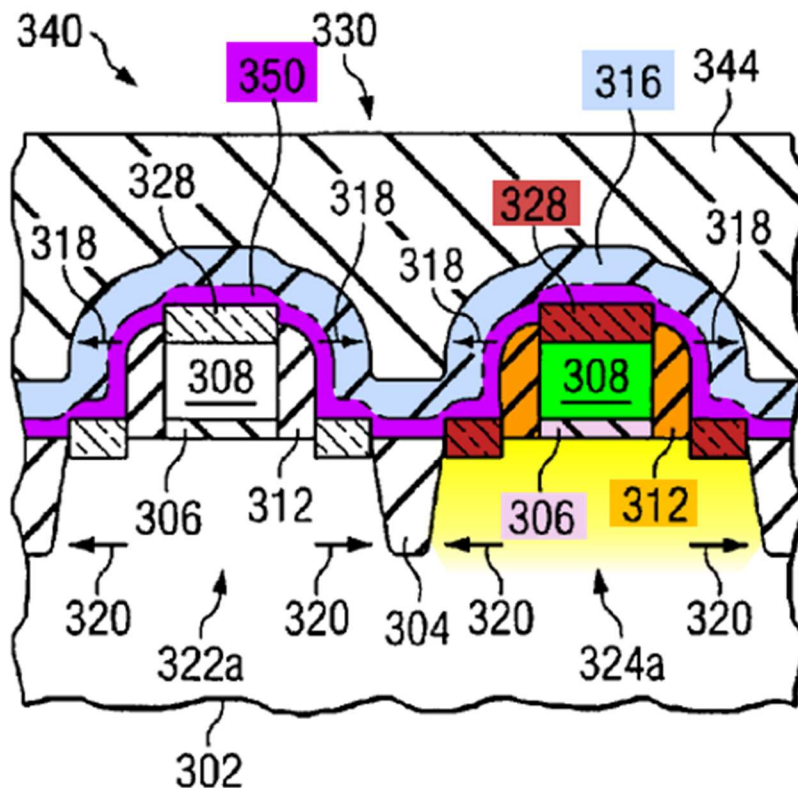


Figure A'



Alvarez, FIG. 10 (excerpted)

This embodiment of the combination satisfies claim 1 for the same reasons described above (*supra* §V.A.1.a-b), since including the optional silicide does not materially affect that analysis. (Alvarez ¶¶[0063]-[0064]; Ex-1003 ¶¶172-174.)

- d. **Claim 4: “The semiconductor device of claim 1, wherein the first stress-relief film is formed on a side surface of the silicon compound layer”**

The proposed combination includes a stress-controlling film 226/326/426 (first stress-relief film) formed on a side surface of SiGe layer 58 in a space created by removing sacrificial layer 52 (*see* Figure A). (*Supra* §V.A.1.a, §V.A.1.b(9); Ex-1003 ¶¶180-182.)

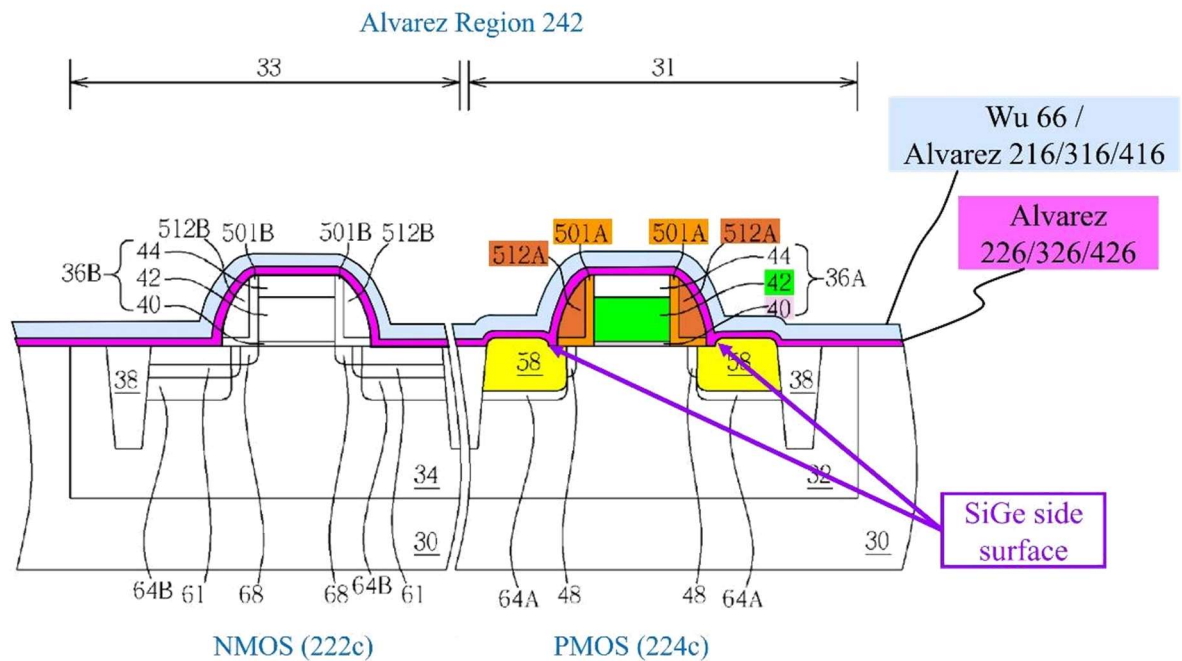


Figure A

- e. Claim 5: “The semiconductor device of claim 1, wherein the first sidewall spacer includes an inner sidewall spacer which is formed on the side surface of the first gate electrode, and whose cross-section has an L shape, and an outer sidewall spacer formed on the inner sidewall spacer”**

The first sidewall spacer comprises an “L”-shaped inner sidewall spacer (layer 501A) formed on the side of gate electrode 42 and an outer sidewall spacer (spacer 512A) formed on layer 501A (*see* Figure A).¹⁴ (Wu ¶¶[0017]-[0018], ¶[0024], FIGS. 1-7, 9-14; *supra* §V.A.1.b(5); Ex-1003 ¶¶183-188.)

¹⁴ *Supra* note 10.

f. Claim 7:

(1) [7Pre]: “The semiconductor device of claim 1”

(Supra §V.A.1.b; Ex-1003 ¶189.)

(2) [7A]: “the first MIS transistor is a p-type MIS transistor”

(Supra §V.A.1.b(2); Ex-1003 ¶190.)

(3) [7B]: “the first stress is a compressive stress”

(Supra §V.A.1.b(6); Ex-1003 ¶191.)

(4) [7C]: “the second stress is a tensile stress”

(Supra §V.A.1.a, §V.A.1.b(7); Ex-1003 ¶192.)

g. Claim 8:

(1) [8Pre]: “The semiconductor device of claim 1”

(Supra §V.A.1.b; Ex-1003 ¶194.)

(2) [8A]: “the silicon compound layer is a SiGe layer”

(Supra §V.A.1.b(6); Ex-1003 ¶195.)

(3) [8B]: “the stress insulating film is a silicon nitride film”

(Supra §V.A.1.a, §V.A.1.b(7); Ex-1003 ¶196.)

(4) [8C]: “the first stress-relief film is a silicon oxide film”

(Supra §V.A.1.b(9); Ex-1003 ¶197.)

- h. Claim 9: “[9Pre] The semiconductor device of claim 1, [9A] wherein the first MIS transistor is an n-type MIS transistor, [9B]the first stress is a tensile stress, and [9C] the second stress is a compressive stress”**

Wu describes reversing the epitaxial source/drain regions for NMOS and PMOS devices. (Wu ¶[0037], ¶[0057]; Ex-1003 ¶¶199-201.) This alternative embodiment has “an NMOS transistor as the first active area [31], and a PMOS as the second active area [33].” (Wu ¶[0037], ¶[0057].) The NMOS includes raised SiC source/drain regions 58 (not SiGe) to impart *tensile* strain along the NMOS channel. (*Id.*; *supra* §II.B; Ex-1021 ¶¶[0021]-[0022]; Ex-1018 ¶[0045]; Ex-1020 ¶[0046].) A POSITA would have expected to succeed in implementing this known technique. (Wu ¶[0037], ¶[0057]; Ex-1018 ¶[0045]; Ex-1020 ¶[0046]; *supra* §II.B; Ex-1003 ¶202.)

A POSITA would have found it obvious to implement Wu’s CESL 66 with compressive strain, not tensile, because such SiC would boost NMOS device performance, whereas the PMOS devices (now lacking SiGe) would require compressive CESL to benefit. (Wu ¶[0005], ¶[0025]; Alvarez ¶[0025], ¶[0033], ¶[0049], ¶[0065], ¶[0067], ¶[0070]; Ex-1022, 1-2; Ex-1023 ¶¶[0037]-[0038]; Ex-1003 ¶203.)

Wu’s CESL 66 may include “a strained silicon material, i.e. silicon nitride.” (Wu ¶[0005], ¶[0025], ¶[0044], FIGS. 7, 14.) Alvarez likewise explains a silicon

nitride “stress-increasing material [216/316/416]” may “comprise[] compressive stress” to improve PMOS performance, which can be offset in NMOS regions “due to the presence of the stress-controlling material 426 or 450 between the NMOS FET and the [compressive] stress-increasing material 416.” (Alvarez ¶[0067]; *see id.* ¶[0047], ¶[0049], ¶[0070]; Ex-1022, 1-2; Ex-1023 ¶¶[0037]-[0038]; Ex-1003 ¶¶204-205.)

A POSITA would have reasonably expected to succeed in forming a compressive silicon nitride CESL using known deposition conditions. (Ex-1024 ¶[0090], ¶¶[0099]-[0100], ¶[0131], Tbls. IV-V, VII; Ex-1003 ¶¶206-207.)

A POSITA thus would have found it obvious to reverse the roles of NMOS and PMOS and compressive and tensile strain. Such a combination would satisfy claim 1 for the reasons in Section V.A.1.b, but with these reversals:

- First MIS transistor 31 is NMOS rather than PMOS (Wu ¶[0037], ¶[0057]);
- Raised silicon compound layer 58 is SiC, not SiGe, and exerts tensile stress (*id.*; *supra* §II.B); and
- CESL 66 causes compressive stress, not tensile (Wu ¶[0005], ¶[0025]; Alvarez ¶[0025], ¶[0033], ¶[0049], ¶[0065], ¶[0067]; Ex-1024 ¶[0090], ¶¶[0099]-[0100], Tbls. IV-V).

(Ex-1003 ¶208.)

i. Claim 11:

(1) [11Pre]: “The semiconductor device of claim 1”

(*Supra* §V.A.1.b; Ex-1003 ¶210.)

(2) [11A]: “a second MIS transistor”

Wu discloses “NMOS transistor region 33.” (Wu ¶[0017], ¶[0038], FIGS. 1-7, 9-14; Ex-1003 ¶¶211-212.) As Figures C and D show, in an exemplary combination second MIS transistor 33 includes a stress-controlling layer 226/326/426 (as in Alvarez’s region 242), and CESL 66 is tensile. (*Supra* §V.A.1.b(7).)

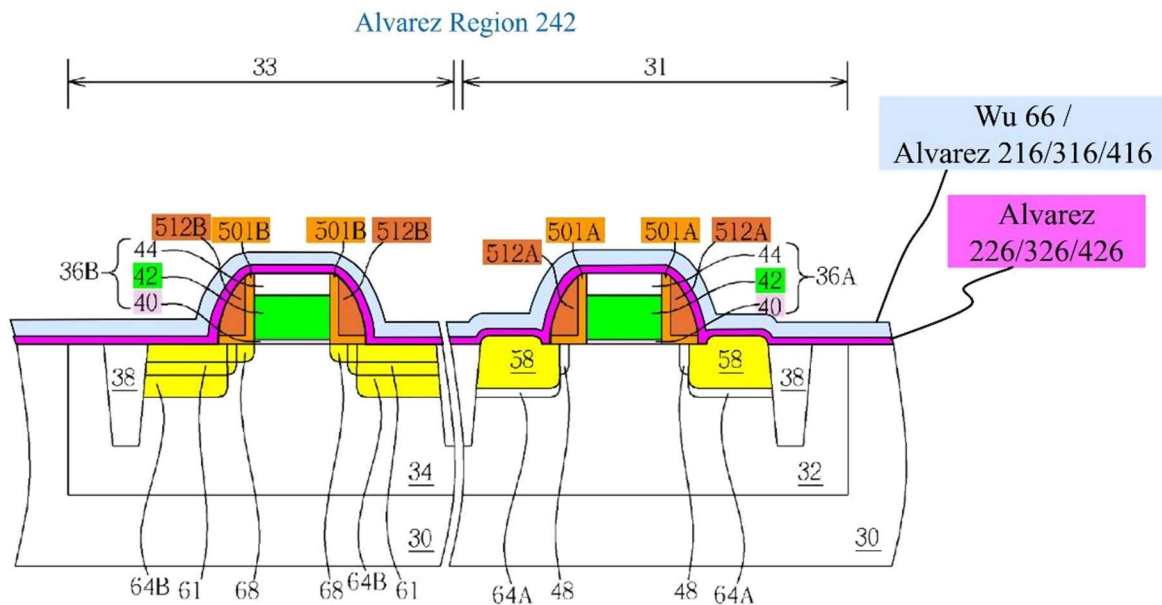


Figure C

Alternatively, an NMOS like 222a in silicide region 230 is a second MIS transistor. (Alvarez ¶[0042], ¶[0044], ¶¶[0046]-[0047], FIGS. 8-9.) There, Wu’s transistor 33 would have a tensile CESL 66 but no stress-relief layer. (Wu ¶[0024],

¶[0043] (silicide optional).) Figure D shows the equivalent of Alvarez’s region 230 (with silicided NMOS 222a) and region 242 (with stress-controlled NMOS 222c) in the asserted combination. (Ex-1003 ¶213.)

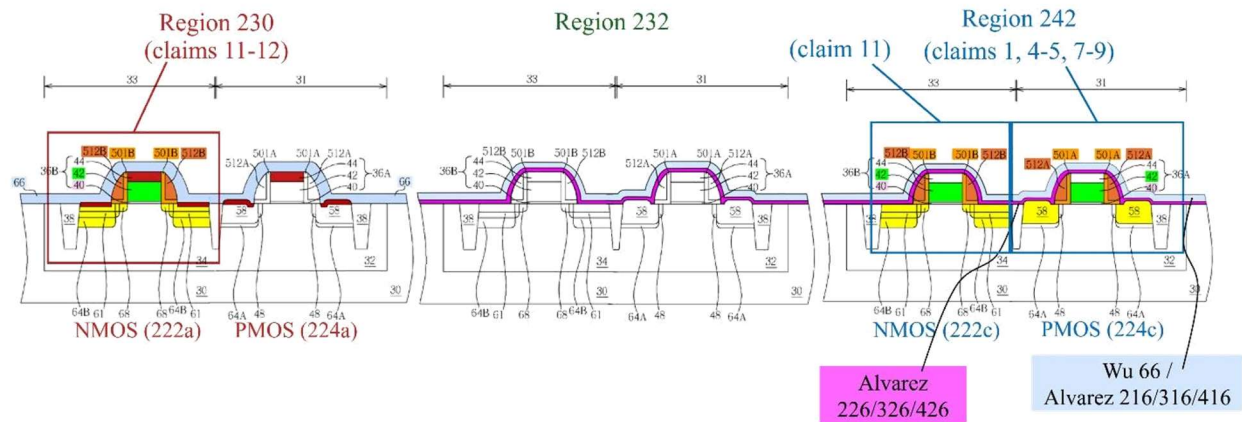
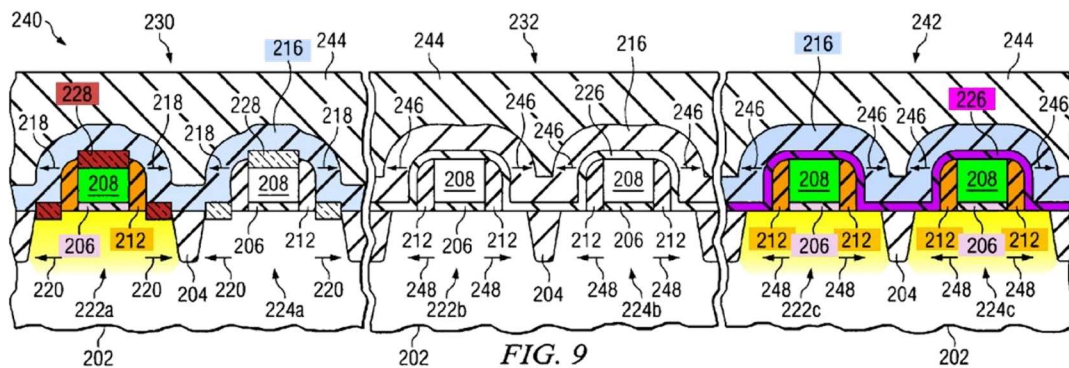


Figure D



Alvarez, FIG. 9

(3) [11B]: “a second gate insulating film formed on a second active region in the semiconductor substrate”

For both combination embodiments regarding claim 11 (*supra* §V.A.1.i(2)), Wu discloses a second gate insulating film (gate dielectric layer 40) formed on NMOS transistor region 33 of substrate 30 (*see* Figures C, D). (Wu ¶[0017], ¶[0038]-[0039]; Ex-1003 ¶214.)

(4) [11C]: “a second gate electrode formed on the second gate insulating film”

For both combination embodiments regarding claim 11 (*supra* §V.A.1.i(2)), Wu discloses a second gate electrode (gate 42) formed on gate dielectric 40 (*see* Figures C, D). (Wu ¶[0017]; Ex-1003 ¶¶215-216; *supra* §V.A.1.a.)

(5) [11D]: “a second sidewall spacer formed on a side surface of the second gate electrode”

For both combination embodiments regarding claim 11 (*supra* §V.A.1.i(2)), Wu discloses a second sidewall spacer comprising spacers 501B and/or 512B formed on a side surface of the gate electrode (gate 42) (*see* Figures C, D). (Wu ¶[0017], ¶[0024], FIGS. 7, 14; Ex-1003 ¶¶217-218.)

(6) [11E]: “a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer”

For both combination embodiments regarding claim 11 (*supra* §V.A.1.i(2)), Wu discloses n-type source/drain regions comprising “source/drain” 64B and “n-type lightly doped drain (NLDD) 60 [sic:61]” and “NLDD2 68,” each formed “in the P well 34 beside the gate structure 36B.” (Wu ¶¶[0023]-[0024], ¶[0038], ¶¶[0042]-[0044], FIGS. 7, 14.) They are formed in the NMOS active region lateral to the second sidewall spacer (sidewalls 501B and/or 512B) (*see* Figures C, D). (Ex-1003 ¶219.)

(7) [11F]: “the stress insulating film formed on the second active region to cover the second gate electrode, the second sidewall spacer, and the second source/drain region”

For both combination embodiments regarding claim 11 (*supra* §V.A.1.i(2)), the stress insulating film (Wu’s CESL 66) blankets both PMOS and NMOS devices (*see* Figures C, D). (Ex-1003 ¶¶220-221; *see* Wu ¶[0025], ¶[0044], FIG. 14; Alvarez ¶¶[0043]-[0050], ¶[0063]-[0068], FIGS. 8-11.)

j. Claim 12: “The semiconductor device of claim 11, wherein no first stress-relief film is formed on the second active region”

For claim 12, silicided NMOS transistor 222a in region 230 (*supra* §V.A.1.i(2)) does not include the first stress-relief film (stress-controlling film 226/326/426) (*see* Figure D). (Alvarez ¶[0037], ¶¶[0042]-[0047], FIGS. 8-9; *see id.* ¶¶[0065]-[0068], FIG. 11; Ex-1003 ¶¶222-224.)

k. Claim 13:

(1) [13Pre]: “The semiconductor device of claim 1”

(*Supra* §V.A.1.b.) Wu discloses “[a] plurality of first active area[s],” e.g., a plurality of PMOS regions 31. (Wu ¶[0017], ¶[0038].) A POSITA would have understood Wu’s devices are repeated many times, as Alvarez underscores by showing exemplary transistors in each of regions 230 (silicide region), 232 (non-silicide region), and 242 (stress-control region). (Alvarez ¶[0037], ¶[0042], FIGS. 9-10; Ex-1003 ¶227.) Figures E and F illustrate the combination as it relates

to claims 13-15. PMOS 224b in region 232 (claims 13-15) has the same structure as PMOS 224c in region 242 (claim 1). (Ex-1003 ¶¶228-229.)

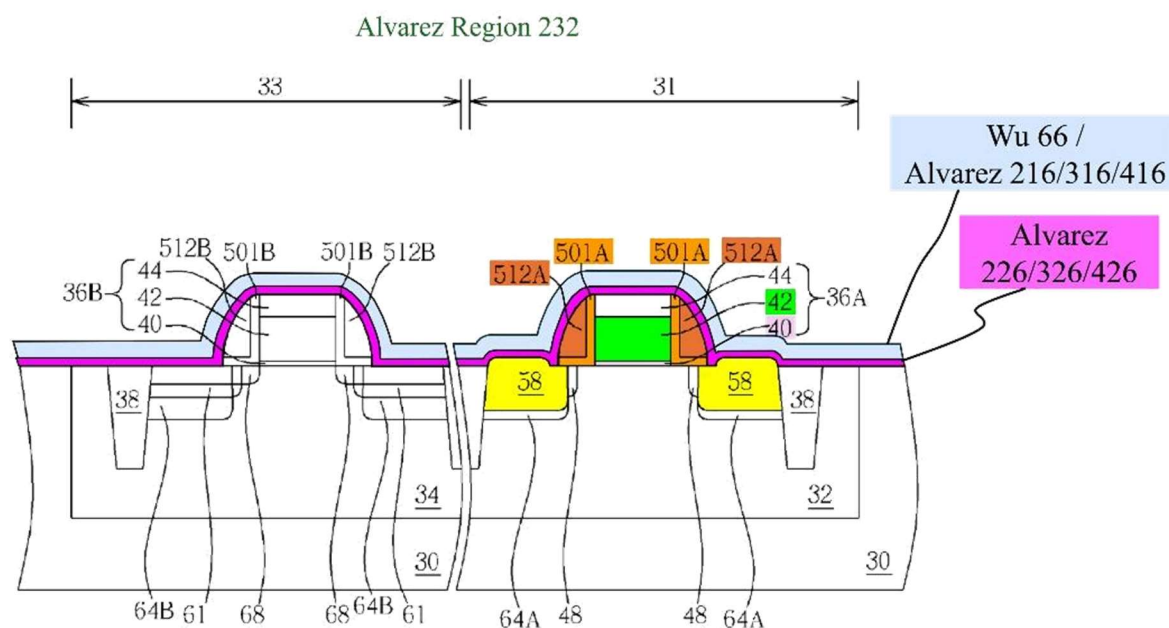


Figure E

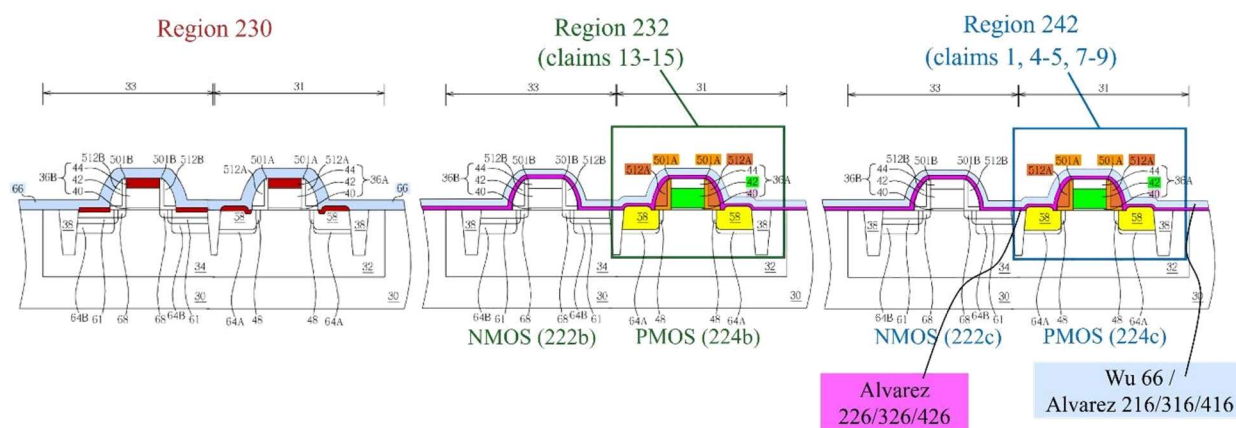
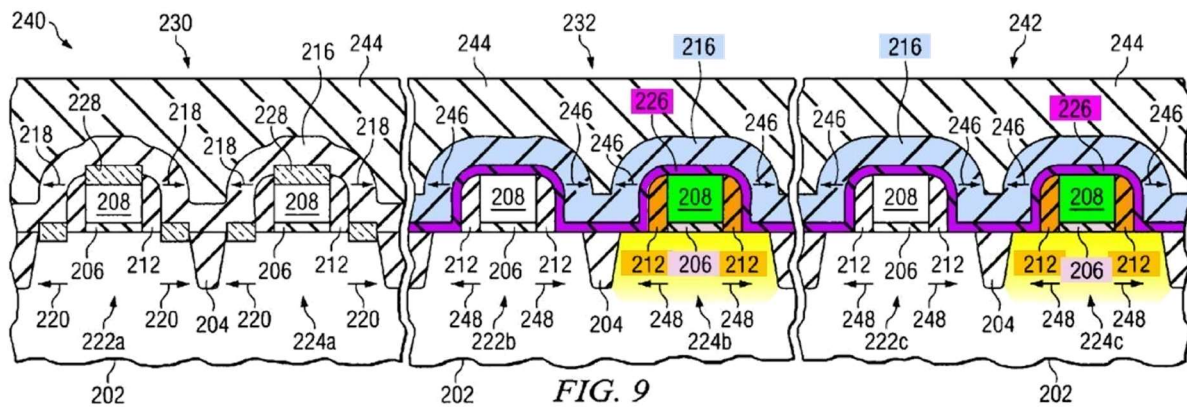


Figure F



Alvarez, FIG. 9

- (2) [13A]: “a third MIS transistor”
 [13B]: “a third gate insulating film formed on a third active region in the semiconductor substrate”
 [13C]: “a third gate electrode formed on the third gate insulating film”
 [13D]: “a third sidewall spacer formed on a side surface of the third gate electrode”
 [13E]: “a third source/drain region of a first conductivity type which is formed in the third active region on a lateral side of the third sidewall spacer”

Wu discloses “[a] plurality of first active area[s] [31].” (Wu ¶[0017], ¶[0038].)

For the same reasons the first PMOS device satisfies [1A]-[1E], the combination (see Figures E, F) discloses [13A] a third MIS transistor (PMOS 224b in region 232) having [13B] a third gate insulating film (gate dielectric layer 40), [13C] a third gate electrode (gate 42), [13D] a third sidewall spacer (comprising oxide layer 501A¹⁵), and [13E] a third source/drain region of p-type conductivity, including SiGe

¹⁵ *Supra* note 10.

layer 58, in a third active area 31. (*Supra* §§V.A.1.b(2)-V.A.1.b(6); Alvarez, FIG. 9 (PMOS 224b); Ex-1003 ¶¶230-238.)

(3) [13F]: “a protective film formed on the third active region to cover the third gate electrode, the third sidewall spacer, and the third source/drain region”

The combination includes a first stress-relief film (like Alvarez’s layer 226/326/426) acting as a protective film to selectively prevent silicidation (e.g., in regions 232 and 242). (Ex-1003 ¶¶239-240.) It covers the third MIS transistor (PMOS 224b), including the third active region, third sidewall spacer, and third source/drain regions (*see* Figures E, F). (*Id.*; *supra* §V.A.1.a, §V.A.1.k(1); Alvarez ¶¶[0034]-[0035], ¶[0037], ¶¶[0043]-[0045], ¶[0078], FIGS. 9-10.)

(4) [13G]: “the stress insulating film formed on the protective film”

The combination includes a stress-inducing film (like Wu’s CESL 66 or Alvarez’s layer 216/316/416) formed on the third MIS transistor’s protective film 226/326/426. (Ex-1003 ¶¶241-243; Alvarez ¶[0047].) The stress-inducing and protective films cover PMOS transistor 224b (*see* Figures E, F). (*Id.*; *supra* §V.A.1.a, §V.A.1.k(1); Alvarez ¶[0037], ¶¶[0043]-[0044], ¶[0047], ¶¶[0050]-[0056], ¶[0073], FIGS. 9-10.)

l. Claim 14: “The semiconductor device of claim 13, wherein no silicide layer is formed on the third gate electrode and the third source/drain region”

A POSITA would have found it obvious to block silicide formation in certain regions with a masking/stress-controlling layer (like Alvarez’s layer 226/326/426). (*Supra* §V.A.1.a, §V.A.1.k(1), §V.A.1.k(4); Alvarez ¶¶[0034]-[0035], ¶[0037], ¶¶[0043]-[0045], ¶[0078], FIGS. 9-10; Ex-1003 ¶244-246.) For example, such a layer prevents silicidation of PMOS 224b (third MIS transistor) in “non-silicide region” 232 (*see* Figures E, F). (Alvarez ¶[0037], ¶[0068], ¶[0073], ¶[0075], FIGS. 9-10; Ex-1003 ¶246.)

m. Claim 15: “The semiconductor device of claim 13, wherein the first stress-relief film and the protective film are made of a same insulating material”

The first stress-relief film and protective film are made of the same insulating material (e.g., silicon oxide) because both are formed at the same time using the same layer, just in different regions (232 and 242). (Alvarez ¶¶[0034]-[0035], ¶[0037], ¶¶[0043]-[0045], ¶¶[0063]-[0065], ¶[0078], FIGS. 9-10; *see* Ex-1001, 12:59-13:19, FIGS. 5A-6B; Ex-1003 ¶¶247-251.)

2. Ground 1B: The Wu-Alvarez-Wolf Combination Renders Obvious Claim 2

a. A POSITA Would Have Found the Wu-Alvarez-Wolf Combination Obvious

Wolf discloses an I-shaped “offset-spacer [being] fabricated on the side of the gate after the gate-poly is etched.” (Wolf, 22, Fig. 5-25.) The offset spacer “yields optimum device characteristics” by preventing “excessive leakage (due to larger short-channel effects that arise if the channel-length is too small).” (Wolf, 21-22, Fig. 5-25.) A POSITA would have found it obvious to add such an I-shaped offset spacer to Wu’s sidewalls. (Ex-1003 ¶¶252-257.)

I-shaped offset spacers were a well-known option to control source/drain extension profiles and mitigate short-channel effects. (Ex-1039, 1, Fig. 2; Ex-1040, Tbl. 3.1; Ex-1041 ¶[0024], FIGS. 1a-2; Ex-1042 ¶[0058], FIGS. 2c-2h; Ex-1043 ¶[0033]; Ex-1044 ¶[0061]; Ex-1045 ¶[0080], ¶[0088], ¶[0091], FIGS. 8A-11C; Ex-1003 ¶¶253-254.) A POSITA thus would have been motivated to include Wolf’s I-shaped offset spacers in Wu’s transistors, as Figure G shows, to mitigate short-channel effects and better control the doping profile of PLDD region 48 and NLDD regions 61. (Ex-1003 ¶255.)

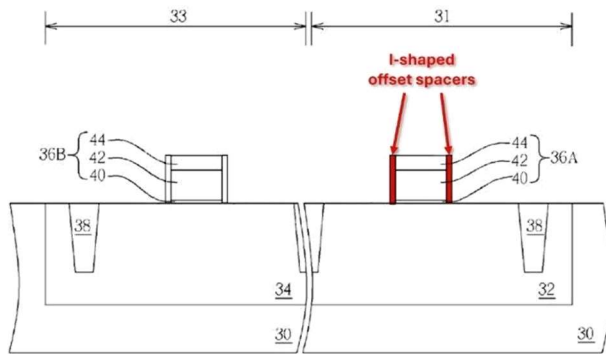
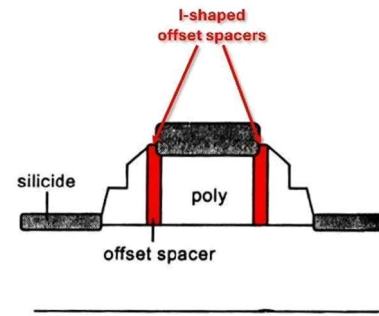


Figure G



Wolf, Fig. 5-25

A POSITA would have reasonably expected to succeed because this is a conventional use of a known technique to achieve ordinary, expected results. (Wolf, 22, Fig. 5-25; Ex-1039, 1, Fig. 2; Ex-1040, Tbl. 3.1; Ex-1041 ¶[0024], FIGS. 1a-2; Ex-1042 ¶[0058], FIGS. 2c-2h; Ex-1043 ¶[0033]; Ex-1044 ¶[0061]; Ex-1045 ¶[0080], ¶[0088], ¶[0091], FIGS. 8A-11C; Ex-1003 ¶256.) As Wolf explains and Figures G (above) and H (below) show, a POSITA would have found it obvious to form an offset spacer before forming Wu's sidewalls 501A/502A. (Wolf, 21-22, Fig. 5-25; Ex-1003 ¶256.) A POSITA would have found it obvious for Wu's processing to then proceed as it describes. (*Supra* §V.A.1.a; *see* Ex-1044 FIGS. 1(b)-2(c); Ex-1003 ¶256.)

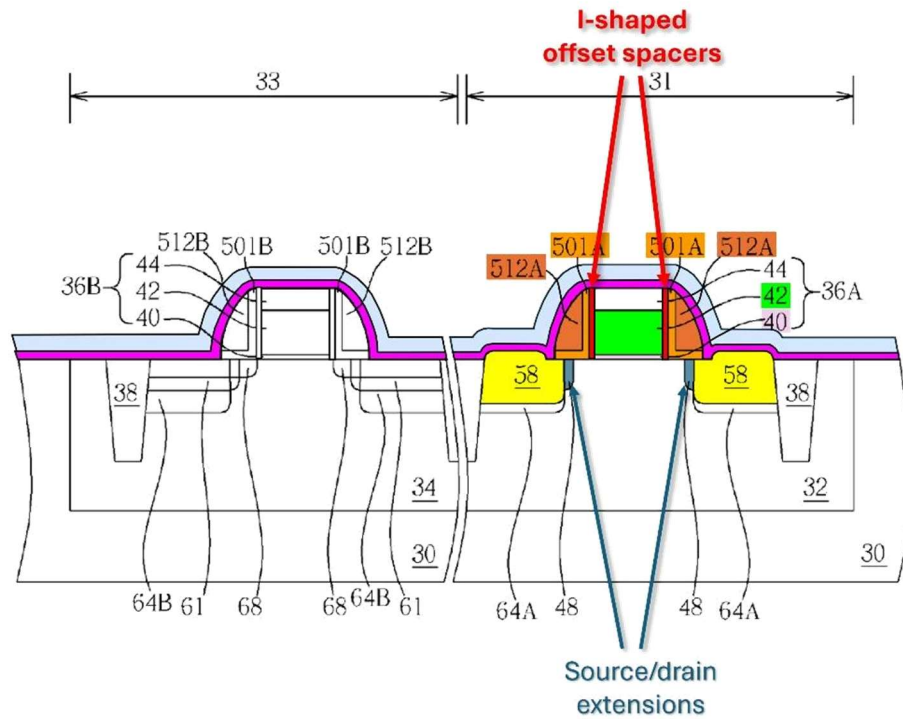
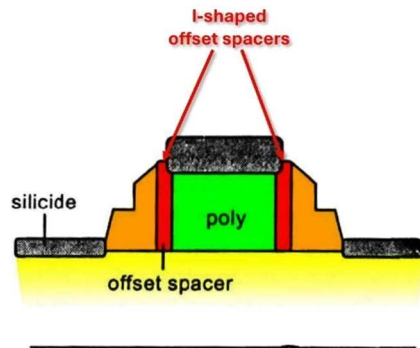


Figure H



Wolf, Fig. 5-25

A POSITA would have found this obvious because it is an example of (a) combining known prior-art elements according to known methods (forming an I-shaped offset spacer) to yield predictable results (define source/drain extensions and mitigate short-channel effects); (b) using a known technique (forming an I-shaped offset spacer) to improve similar devices (Wu's MOSFETs) in the same

way; (c) applying these same known techniques (forming the I-shaped offset spacer) to improve a known device (Wu's MOSFETs) and yield predictable results (optimal source/drain extensions and reduced short-channel effects); and (d) applying a known teaching, motivation, or suggestion in the prior art (e.g., the teachings in Wolf, Ex-1039, Ex-1040, and others described above) to arrive at the claimed invention. (*KSR*, 550 U.S. at 416-21; Ex-1003 ¶257.)

b. Claim 2: “The semiconductor device of claim 1, further comprising: a first offset spacer which is formed between the first gate electrode and the first sidewall spacer, and whose cross-section has an I shape”

A POSITA would have found it obvious to incorporate Wolf's I-shaped offset spacer between Wu's gate electrode 42 and sidewall spacer (comprising 501A) to control the profile of Wu's PLDD 48 and NLDD 61, yielding a structure like the one below. (*Supra* §V.A.2.a; Ex-1003 ¶¶258-260.)

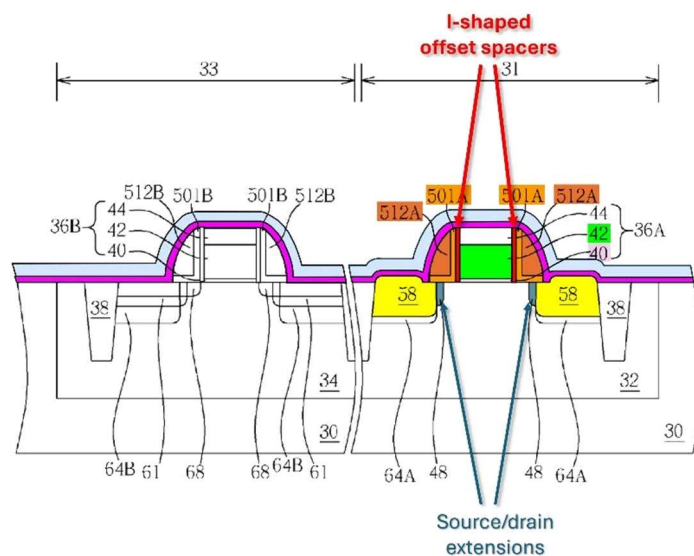
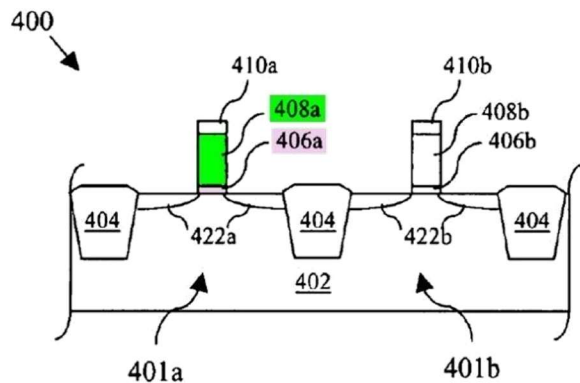


Figure H

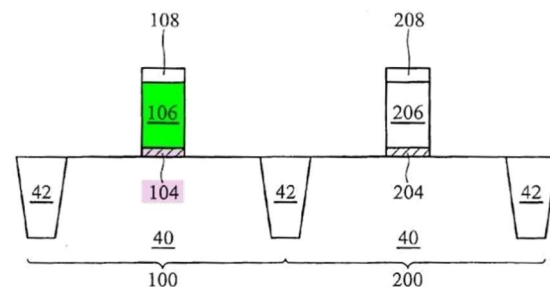
B. Grounds 2A-2D: Cheng

Cheng and Wang describe similar MOS devices formed using similar processes. (Compare Cheng ¶¶[0056]-[0070], Figs. 4a-4j, with Wang ¶¶[0023]-[0032], FIGS. 4-9.) Considering Cheng's descriptions and figures in conjunction with Wang's helps demonstrate how a POSITA would have understood Cheng's disclosures. (Ex-1003 ¶¶263-264.)

Cheng's Fig. 4a, like Wang's FIG. 4, shows forming gate dielectric and gate electrode layers. (Cheng ¶[0056], Fig. 4a; Wang ¶[0023], FIG. 4.)

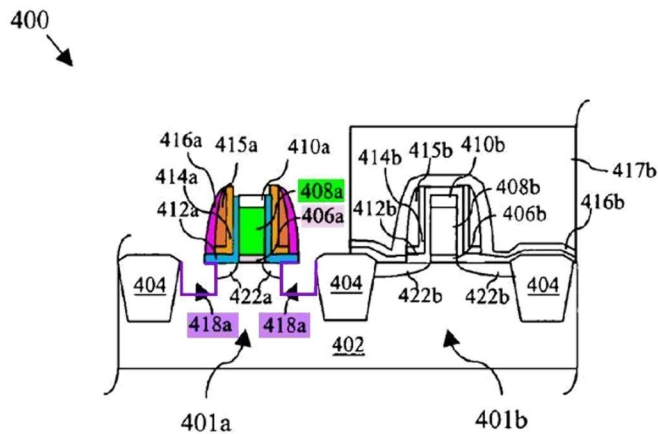


Cheng, Fig. 4a



Wang, FIG. 4

Cheng's Figs. 4b-4d, like Wang's FIGS. 5-8, show forming gate electrode sidewalls, then etching recesses for SiGe growth. (Cheng ¶¶[0061]-[0063], Figs. 4b-4c; Wang ¶¶[0025]-[0028], FIGS. 5-8.) In Cheng's PMOS 401a of Fig. 4d, sidewall dielectric 412a (blue) lies below dummy spacer 416a (magenta), akin to how Wang's sidewall portion 120₁ lies below sidewall portion 120₂ (magenta). (Cheng ¶[0064], Fig. 4d; Wang ¶[0029], FIG. 9; Ex-1003 ¶¶265-266.)



Cheng, Fig. 4d

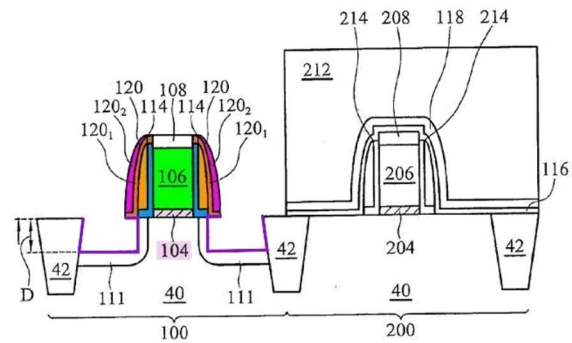
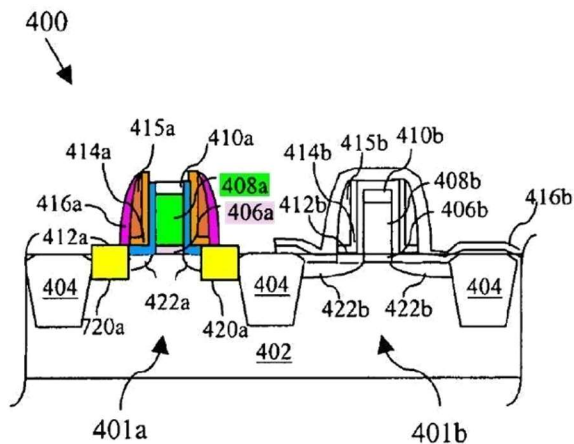


FIG. 9

Wang, FIG. 9*

(*modified to remove SiGe)

Cheng's Fig. 4e, like Wang's FIG. 9, shows SiGe grown in the trenches and extending above the substrate. (Cheng $\llbracket 0022 \rrbracket$, $\llbracket 0065 \rrbracket$, Fig. 4e; Wang $\llbracket \llbracket 0030 \rrbracket \rrbracket$ - $\llbracket 0032 \rrbracket$, FIG. 9.)



Cheng, Fig. 4e

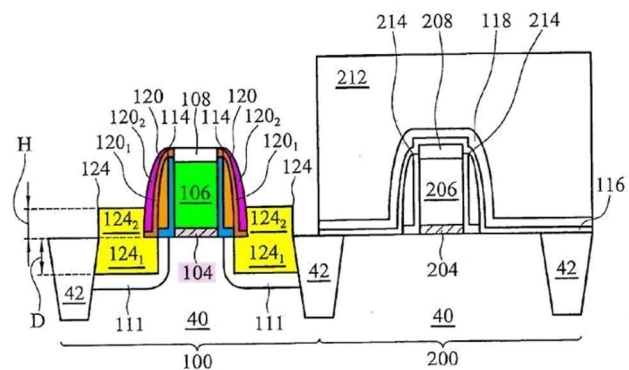
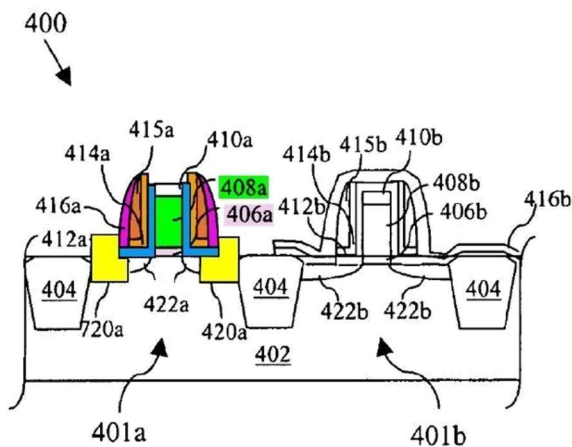


FIG. 9

Wang, FIG. 9

A POSITA would have understood from Cheng's textual descriptions that Fig. 4e contains a rendering error where the epitaxial regions (720a [sic:420a] and 420a) appear to replace part of layer 412a (blue). (Ex-1003 ¶¶267-268.) The epitaxial regions in Cheng's Fig. 4e instead necessarily grow selectively on the crystalline

trench surfaces and extend up and around the non-crystalline sidewalls, as in corrected Fig. 4e below (left). (Cheng ¶[0065]; Wang ¶¶[0030]-[0031], FIG. 9; Ex-1018 ¶¶[0024]-[0028], FIGS. 4-6; Ex-1003 ¶¶268-269.) It would not replace the sidewall. (Ex-1003 ¶¶268-269.)



Cheng, Fig. 4e (corrected)

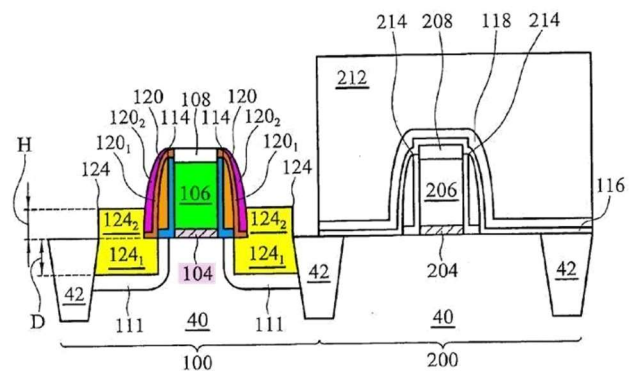


FIG. 9

Wang, FIG. 9

Consistent with corrected Fig. 4e, “[t]he height of raised source/drain regions may” extend as much as “about 100 nm” above the substrate, substantially higher than the top of the 0.5-10 nm thick gate dielectric 406a (lavender). (Cheng ¶[0018], ¶[0022].) Wang similarly explains that “raised [SiGe] portions 124₂ preferably have a height H ... between about 100 Å and about 700 Å [10-70nm].” (Wang ¶[0031].)

A POSITA would have recognized this correction should carry through in Cheng’s Figs. 4f-4j. (Cheng ¶¶[0066]-[0070]; Ex-1003 ¶270.) Figure I below modifies Cheng’s Fig. 4j to show how this correction affects Cheng’s final device. (Ex-1003 ¶271.) A POSITA would have found obvious, from Cheng’s disclosures

alone or in combination with Wang's, that Cheng describes a PMOS transistor consistent with Figure I, which more accurately illustrates the process Cheng's text describes. (Ex-1003 ¶¶271-273; Cheng ¶¶[0056]-[0070].)

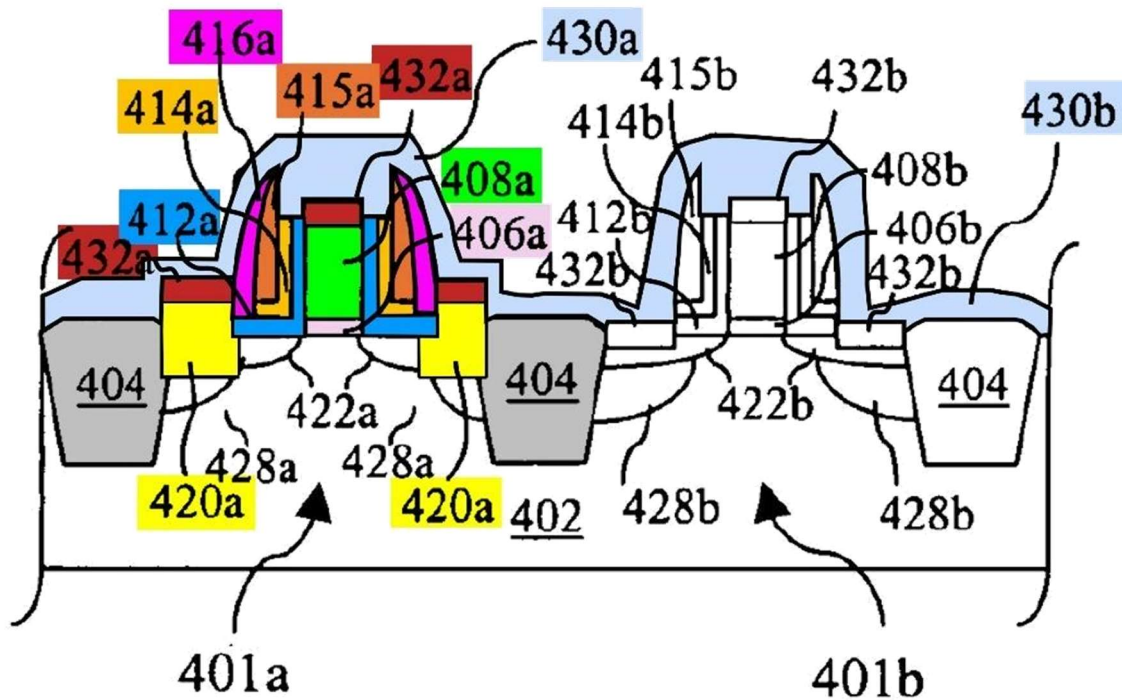


Figure I (Cheng, Fig. 4j, corrected)

A POSITA would have found this structure obvious because it applies a known teaching, motivation, or suggestion in the prior art (Cheng's express disclosures regarding Figs. 4a-4j, alone or in combination with Wang's descriptions of FIGS. 4-9) to arrive at the claimed invention (reflected in Figure I). (*KSR*, 550 U.S. at 416-21.) "A person of ordinary skill is ... not an automaton" and would have understood this. (*Id.* at 421; Ex-1003 ¶274.)

1. Ground 2A: Cheng Renders Obvious Claims 1, 3-9, and 11-12

a. Independent Claim 1

(1) [1Pre]

Cheng discloses “semiconductor devices 401a and 401b.” (Cheng ¶¶[0056]-[0071], Fig. 4j; Ex-1003 ¶276.)

(2) [1A]

Cheng discloses “a P-type MOS device” 401a.¹⁶ (Cheng ¶¶[0056]-[0071], Fig. 4j; Ex-1003 ¶277.)

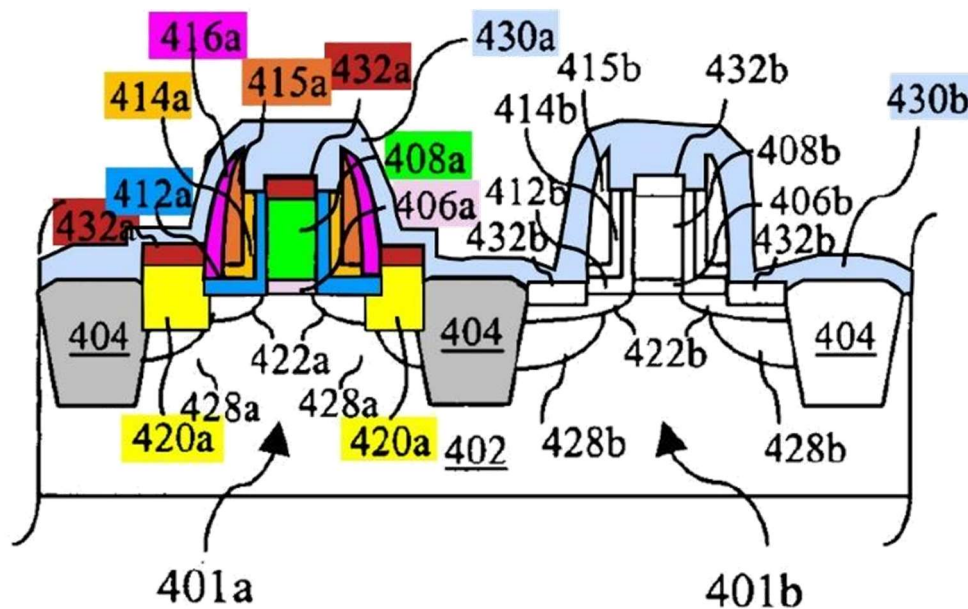


Figure I

¹⁶ As explained for claim 9, the first MIS transistor could alternatively be NMOS.

(*Infra* §V.B.1.a; Ex-1003 ¶277 n.24.)

(3) [1B]

Cheng discloses a first gate insulating film (gate dielectric 406a) “formed over a substrate 402.” (Cheng ¶[0056], Fig. 4j; Ex-1003 ¶¶278-280.) Substrate 402 contains an active region comprising LDD regions 422a, source/drain regions 420a, heavily doped regions 428a, and the surrounding semiconductor regions. (Cheng ¶[0060], ¶¶[0065]-[0068], Fig. 4j.)

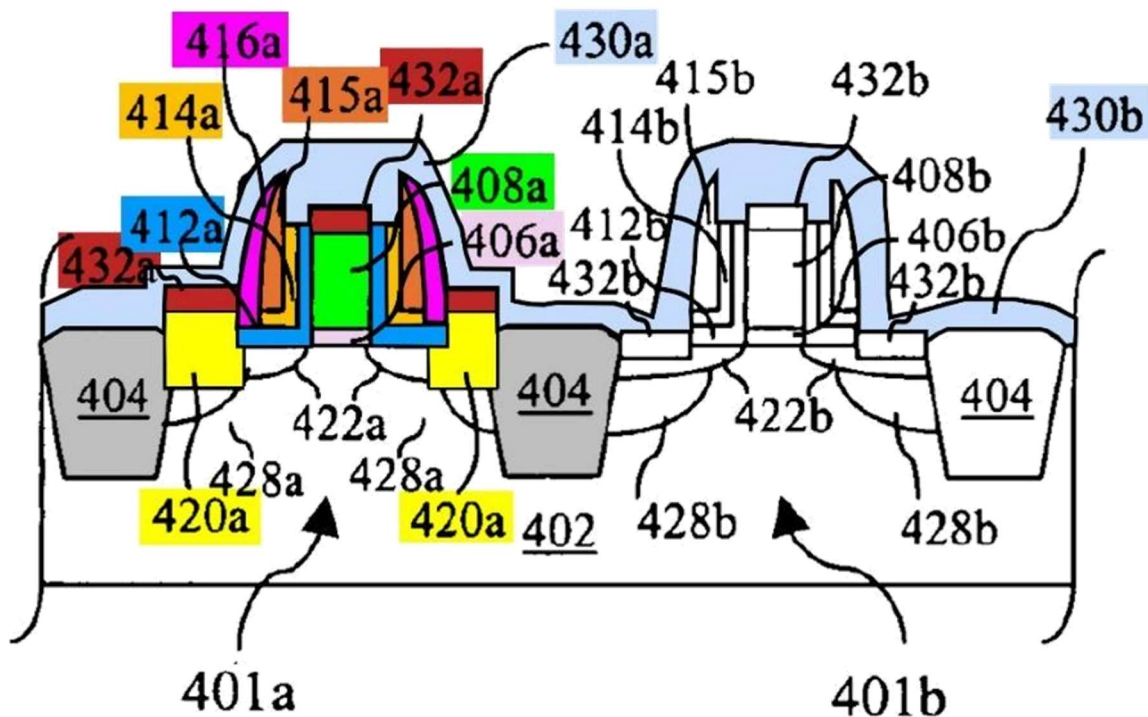


Figure I

(4) [1C]

Cheng discloses a first gate electrode (gate electrode 408a) formed on the first gate insulating film (gate dielectric 406a). (Cheng ¶[0056]; Ex-1003 ¶281.)

(5) [1D]

Cheng discloses a first sidewall spacer comprising sidewall structures 414a (light orange) and spacers 415a (dark orange) on the side surface of gate electrode 408a (green). (Cheng ¶[0061]; Ex-1003 ¶¶282-283.)

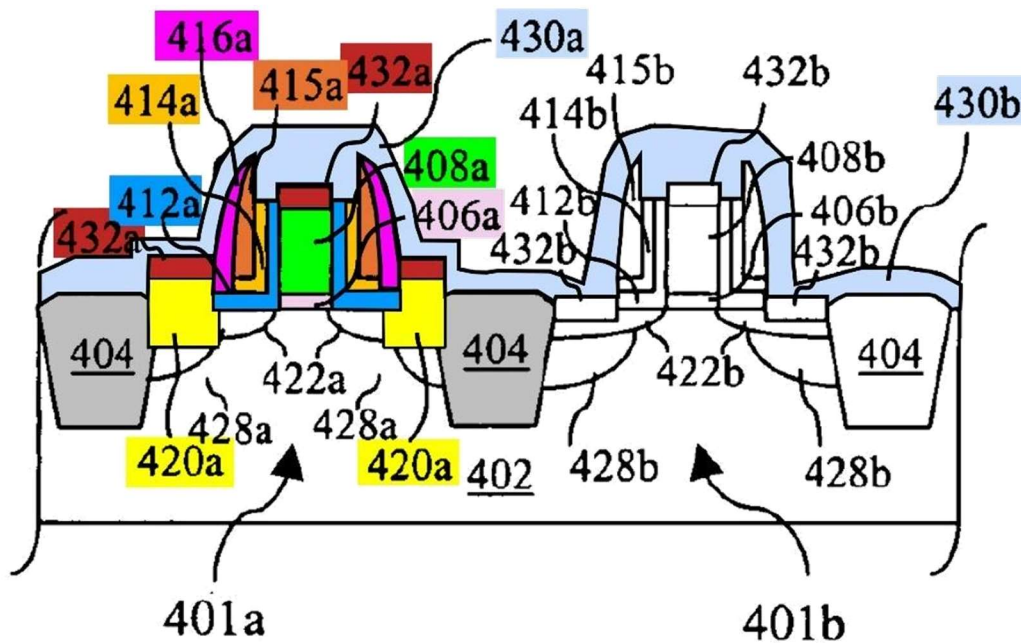


Figure I

(6) [1E]

Cheng discloses “doped source and drain regions 420a ... built-up in the recessed regions 418a.” (Cheng ¶[0065].) Recessed regions 418a are trenches formed by etching. (Cheng ¶[0064].) “[S]ource and drain regions 420a” may comprise “silicon germanium,” which imparts a compressive stress along the gate length direction of the channel region in PMOS 401a. (Cheng ¶[0065]; *supra* §II.B; Wang ¶[0031]; Ex-1018 ¶[0024], ¶[0026], ¶[0028], FIGS. 4-7; Ex-1003 ¶¶284-286.)

SiGe source/drain regions 420a and LDD regions 422a have p-type conductivity because 401a is a PMOS device. (Cheng ¶[0056], ¶[0060], ¶[0065]; Ex-1003 ¶285.)

SiGe source/drain regions 420a are provided laterally next to the first sidewall spacers (sidewalls 414a and 415a) because they grow out of recesses 418a next to the sidewall spacers (*see* Figure I). (Cheng, Figs. 4d-4j; Ex-1003 ¶286.)

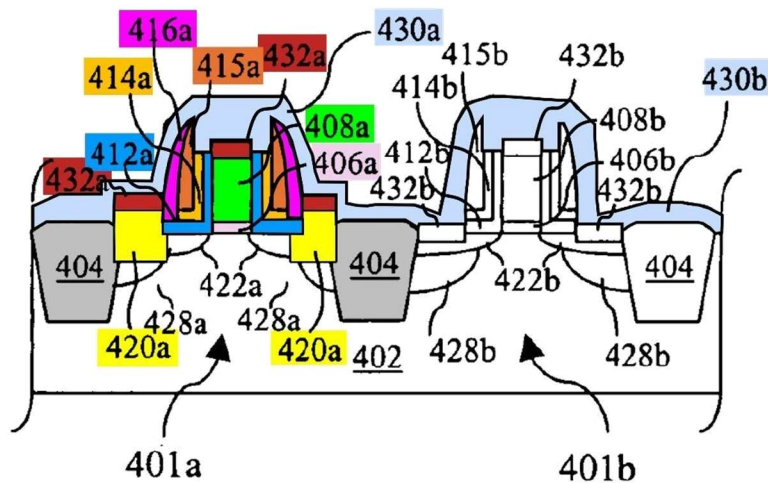


Figure I

(7) [1F]

Cheng discloses a stress insulating film, such as etch stop layer 430a/430b, formed over PMOS 401a to cover gate electrode 408a, sidewall spacers 414a and 415a, and SiGe source/drain regions 420a. (Cheng ¶[0070], Fig. 4j; Ex-1003 ¶287-289.) Etch stop layer 430a/430b may be silicon nitride and cause a tensile stress “between about +0.001 and about +50 GPa” opposite the SiGe compressive stress. (Cheng ¶[0070].)

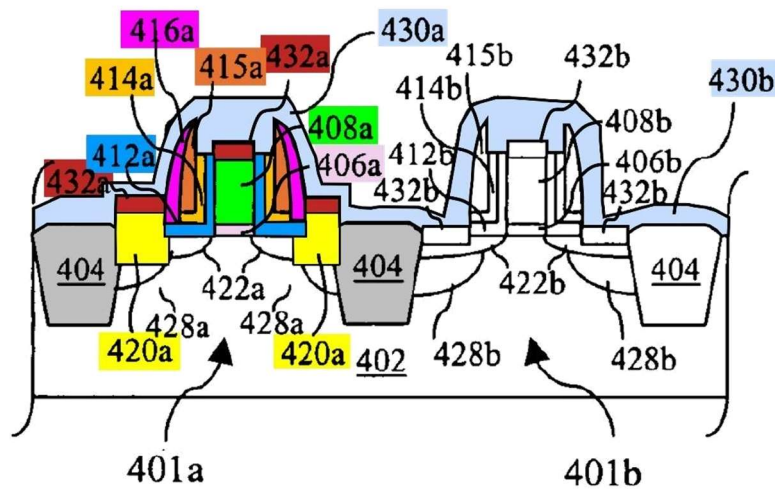
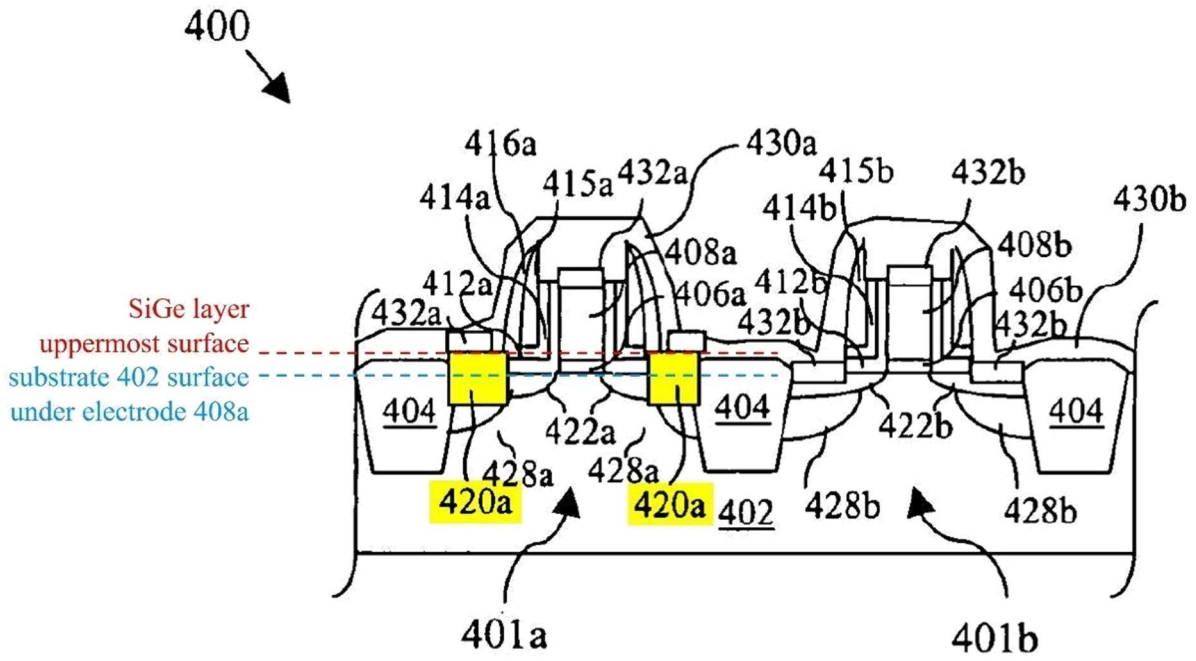


Figure I

It was well-known that a tensile CESL improves electron mobility in NMOS regions and that compressive SiGe improves PMOS region mobility. (*Supra* §II.B; Ex-1023 ¶[0039]; Alvarez ¶[0054], FIGS. 9-10 (tensile stress-inducing film 216/316/416); Ex-1029 ¶[0005], ¶¶[0034]-[0035]; Ex-1018 ¶¶[0038]-[0039]; Ex-1020 ¶[0005]; Ex-1022, 1-2; Ex-1003 ¶290.)

(8) [1G]

Cheng discloses that “source/drain regions 136,” analogous to source/drain regions 420a, “may extend above the substrate surface 106.” (Cheng ¶[0022], ¶[0065].) A POSITA would have understood SiGe source/drain regions 420a likewise extend above the substrate. (*Supra* §V.B; Cheng ¶[0054], ¶[0065]; Ex-1003 ¶¶291-295.) Cheng’s PMOS transistor “comprises *raised* source and drain regions” that are “built-up” and extend as much as “about 100 nm” above the substrate. Cheng ¶[0022], ¶[0054], ¶[0065], Figs. 1, 4j.



Cheng, Fig. 4j

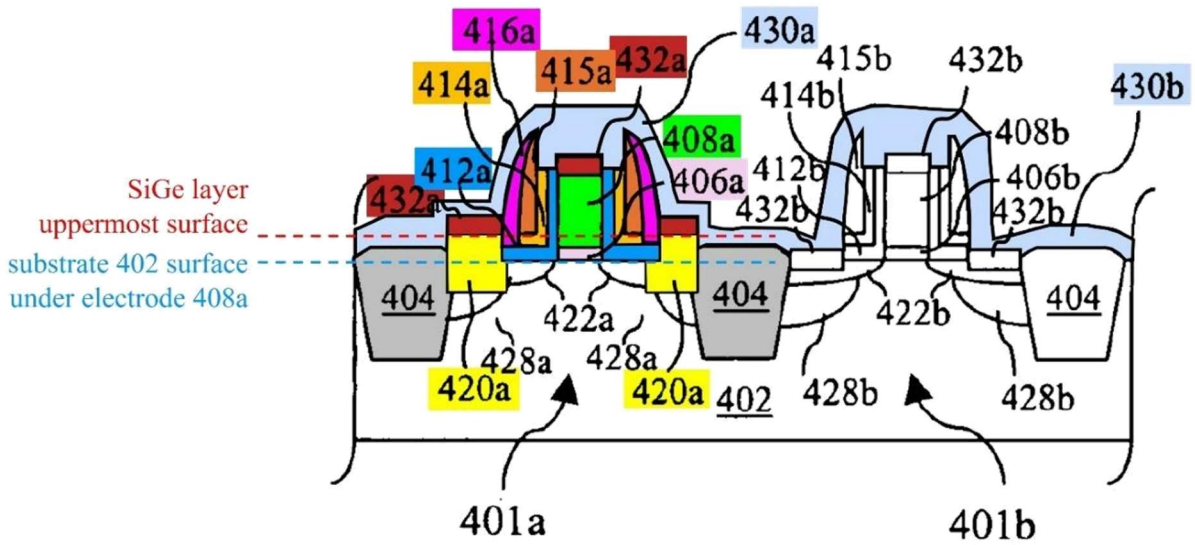


Figure I

(9) [1H]

Cheng discloses “dummy spacers 416a” made of “silicon dioxide (SiO₂)” formed between SiGe source/drain regions 420a (silicon compound layer) and sidewall spacers 414a and 415a, because the SiGe extends above the substrate and grows around the sidewalls. (Cheng ¶[0063], Fig. 4j; *supra* §V.B (introduction), §V.B.1.a(8); Ex-1003 ¶¶296-297.) Dummy spacers 416a would “prevent[] the tension” from a tensile overlayer “from materially adversely influencing the charge carrier mobility in the pFET [PMOS]” by defining “a neutral stress” buffer layer between a compressive SiGe layer and a tensile etch stop layer (e.g., Cheng’s tensile layer 430a/430b). (Ex-1031 ¶[0067]; Ex-1032 ¶[0030]; Ex-1029 ¶[0034], ¶[0042]; Ex-1003 ¶¶298-299.) This is like the ’425 Patent, which describes “[a] first stress-relief film 28a ... in the space 24 between the silicon compound layer 23 and the first sidewall 19A.” (Ex-1001, 14:51-54.)

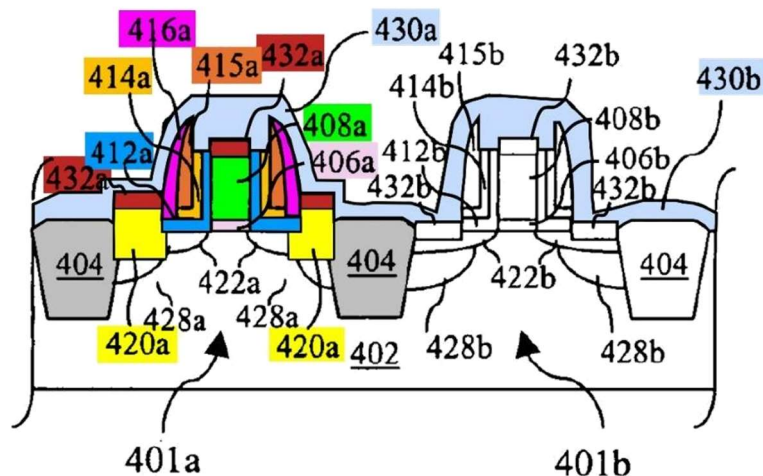


Figure I

(10) [1I]

Cheng's dummy spacer 416a (magenta) is formed on the side surface of gate electrode 408a (green), with the first sidewall spacer (sidewalls 414a and 415a) (orange) located between (*see* Figure I). (Cheng ¶[0061], [0063], Figs. 4c-4j; *supra* §V.B, §V.B.1.a(9); Ex-1003 ¶¶300-301.) SiGe source/drain regions 420a extend above the substrate surface and around the sidewall spacers. (*Supra* §V.B, §V.B.1.a(6); Ex-1003 ¶268.)

(11) [1J]

The stress-relief film (spacer 416a, magenta) does not directly contact a side surface of gate electrode 408a (green) because the sidewall spacer (sidewalls 414a and 415a) (orange) separates them. (*Supra* §§V.B.1.a(9)-V.B.1.a(10); Ex-1003 ¶¶302-303.)

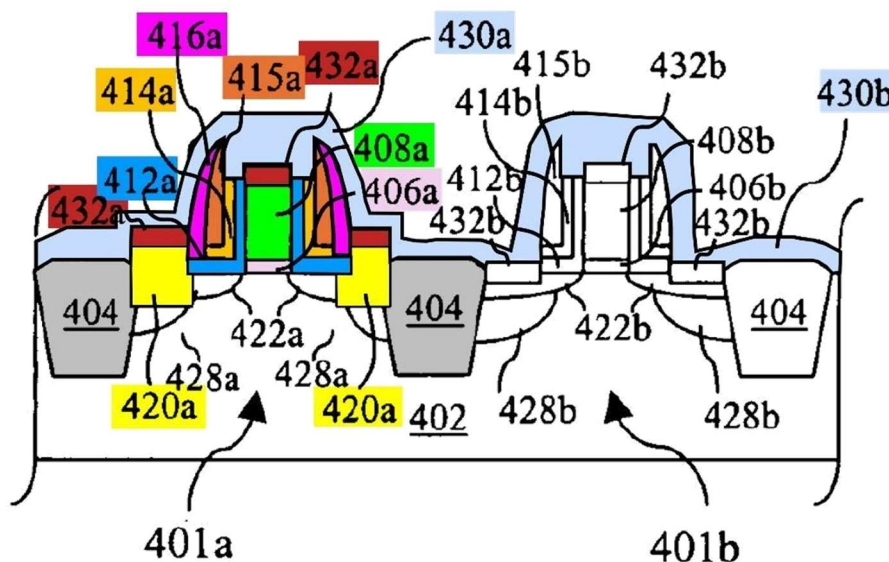


Figure I

b. Claim 3

Cheng discloses silicide contacts 432a (red) formed both on gate electrode 408a (green) and SiGe source/drain regions 420a (yellow). (Cheng ¶[0069], Figs. 4i-4j.) The former is a “first silicide layer,” and the latter are “second silicide layer[s].” (Ex-1003 ¶¶304-308.)

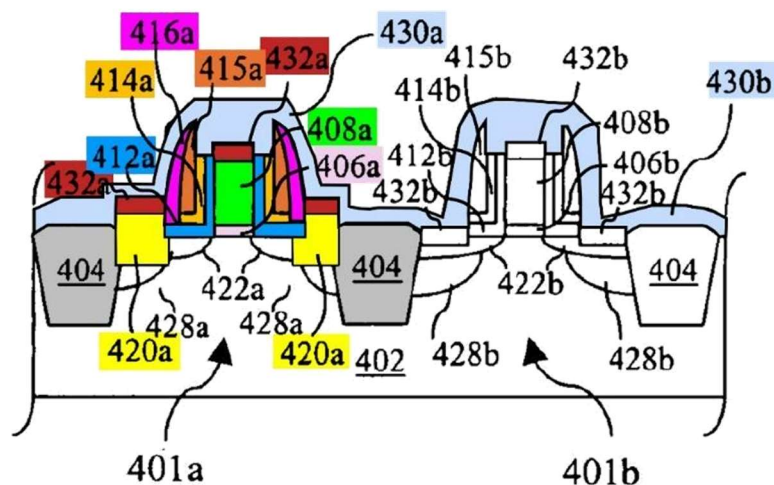


Figure I

c. Claim 4

Cheng’s stress-relief film (dummy spacer 416a) is formed on a side surface of the silicon compound layer (SiGe source/drain regions 420a) (*see* Figure I). (Cheng, Fig. 4j; *supra* §§V.B.1.a(9)-V.B.1.a(11); Ex-1003 ¶¶309-313.)

d. Claim 5

Cheng’s first sidewall spacer comprises an inner sidewall 414a (light orange) and outer sidewall spacer 415a (dark orange) (*see* Figure I). (Cheng ¶[0061]; *supra* §V.B.1.a(5).) Inner sidewall 414a, formed on a side surface of gate electrode 408a

(green), has a “substantially L-shaped” cross-section. (Cheng ¶[0061], Fig. 4j; Ex-1003 ¶¶314-318.) Cheng’s outer sidewall spacer 415a is formed on inner sidewall 414a. (Cheng ¶[0061], Fig. 4j; Ex-1003 ¶318.)

e. Claim 6:

(1) [6Pre]: “The semiconductor device of claim 1”

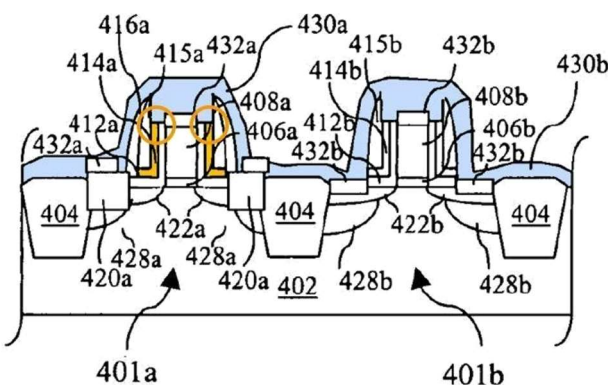
(*Supra* §V.B.1.a; Ex-1003 ¶320.)

(2) [6A]: “the first sidewall spacer includes an inner sidewall spacer whose cross-section has an L shape”

(*Supra* §V.B.1.a(5), §V.B.1.d; Ex-1003 ¶¶321-322.)

(3) [6B]: “the stress insulating film is formed in contact with a surface of the inner sidewall spacer which is curved to have an L-shaped cross-section”

Cheng’s stress insulating film (etch stop layer 430a/430b, blue) extends over both MOSFETs and contacts a top surface of inner sidewall structure 414a (light orange) having an L-shape (*see* Figure I). (Cheng ¶[0070], Fig. 4j; Ex-1003 ¶¶323-324.)



Cheng, Fig. 4j

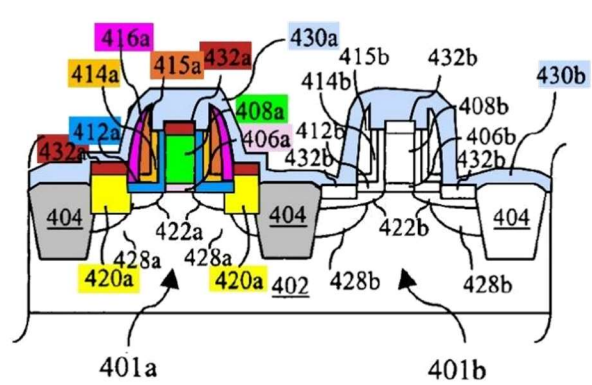


Figure I

f. Claim 7:

(1) [7Pre]

(*Supra* §V.B.1.a; Ex-1003 ¶326.)

(2) [7A]

(*Supra* §V.B.1.a(2); Ex-1003 ¶327.)

(3) [7B]

(*Supra* §V.B.1.a(6); Ex-1003 ¶328.)

(4) [7C]

(*Supra* §V.B.1.a(7); Ex-1003 ¶329.)

g. Claim 8:

(1) [8Pre]

(*Supra* §V.B.1.a; Ex-1003 ¶331.)

(2) [8A]

(*Supra* §V.B.1.a(6); Ex-1003 ¶332.)

(3) [8B]

(*Supra* §V.B.1.a(7); Ex-1003 ¶333.)

(4) [8C]

(*Supra* §V.B.1.a(9); Ex-1003 ¶334.)

h. Claim 9:

(1) [9Pre]

Cheng renders obvious the device of claim 1, which may be an NMOS device. (Cheng ¶[0036]; *supra* §V.B.1.a(2) & n.15; Ex-1003 ¶336.) Similar to Section V.A.1.h (Ground 1, claim 9), Cheng discloses the structure of claim 1 but substituting NMOS for PMOS, SiC for SiGe, and compressive CESL for tensile CESL. (Ex-1003 ¶336.)

(2) [9A]

Cheng’s NMOS transistor may comprise SiC source/drain regions. (Cheng ¶[0036]; Ex-1003 ¶¶337-341.) For claim 9, the “first MIS transistor” would be the NMOS device, modified to include raised SiC regions grown in a recess like the SiGe source/drain regions of the PMOS device. (Cheng ¶[0033], ¶[0036]; Ex-1003 ¶¶338-339.) Cheng’s “first semiconductor device” may include “a dummy spacer [first stress-relief film] on either side of the gate structure.” (Cheng, claim 5.) A POSITA would have understood that when the first MIS transistor is NMOS, it has the same structure as device 401a shown in Figure I. (Ex-1003 ¶¶339-341.)

(3) [9B]

Cheng discloses “source/drain regions located at least partially within the substrate and comprising SiC,” where “at least partially within” describes SiC source/drain regions extending above the substrate. (Cheng ¶[0036]; *see id.* ¶[0025],

¶[0033]; Ex-1003 ¶342.) SiC source/drain regions cause tensile stress along the gate length direction in Cheng's NMOS devices. (*Supra* §II.B, §V.A.1.h; Ex-1003 ¶342.)

(4) [9C]

Cheng discloses “etch stop layer 430a and 430b may include a stress level that may range ... between about -0.001 and about -50 GPa for compressive film.” (Cheng ¶[0070]; Ex-1003 ¶343.)

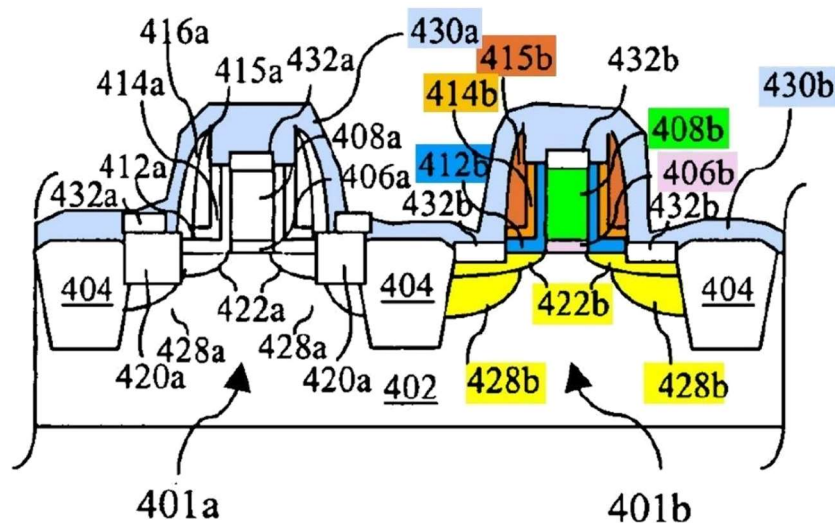
i. Claim 11:

(1) [11Pre]

(*Supra* §V.B.1.a; Ex-1003 ¶¶345-346.)

(2) [11A]

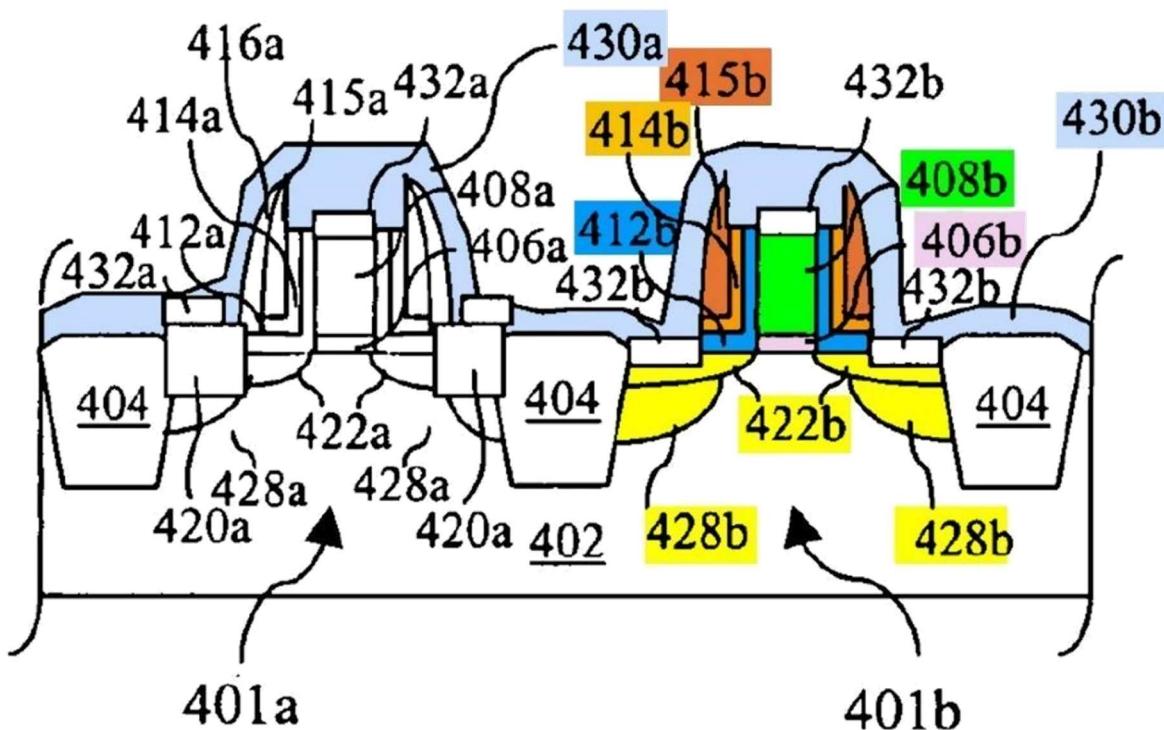
Cheng discloses a second MIS transistor, e.g., “N-type MOS device” 401b.
(Cheng ¶[0056], Fig. 4j; Ex-1003 ¶347.)



Cheng, Fig. 4j

(3) [11B]

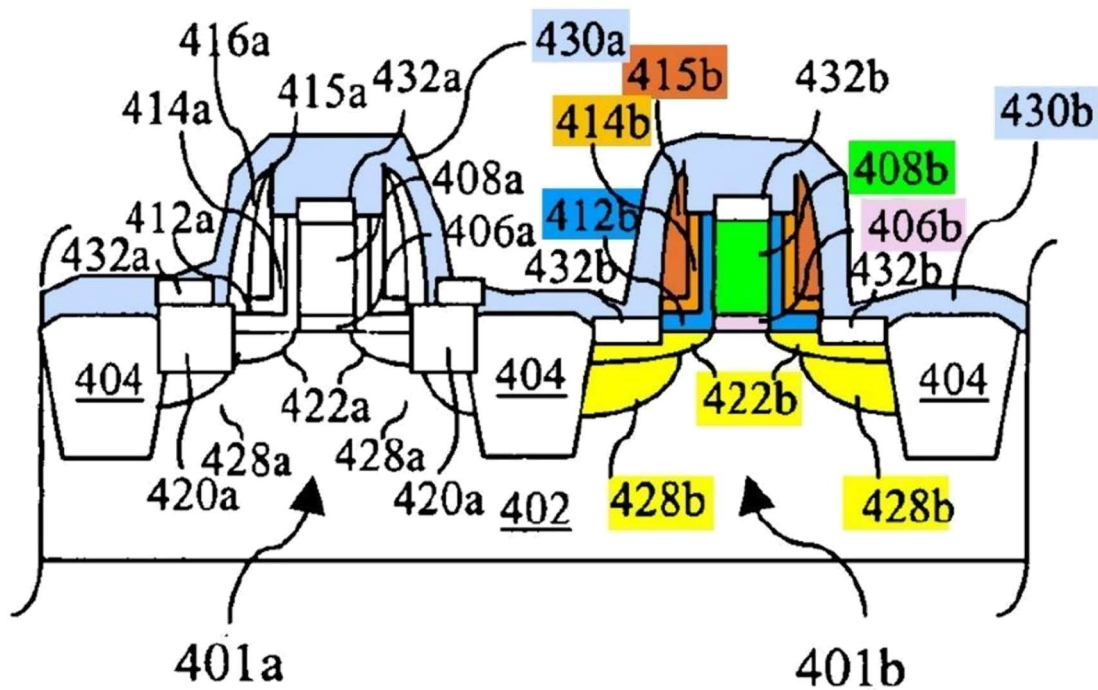
Cheng's NMOS 401b includes a second gate insulating film (gate dielectric 406b) formed over an NMOS active region comprising lightly doped regions 422b, heavily doped regions 428b, and the surrounding semiconductor regions. (Cheng ¶[0056], ¶[0060], ¶[0066], Fig. 4j; Ex-1003 ¶¶348-351.)



Cheng, Fig. 4j

(4) [11C]

Cheng's NMOS 401b includes a second gate electrode (gate electrode 408b) formed over gate dielectric layer 406b. (Cheng ¶[0056], Fig. 4j; Ex-1003 ¶¶352-353.)



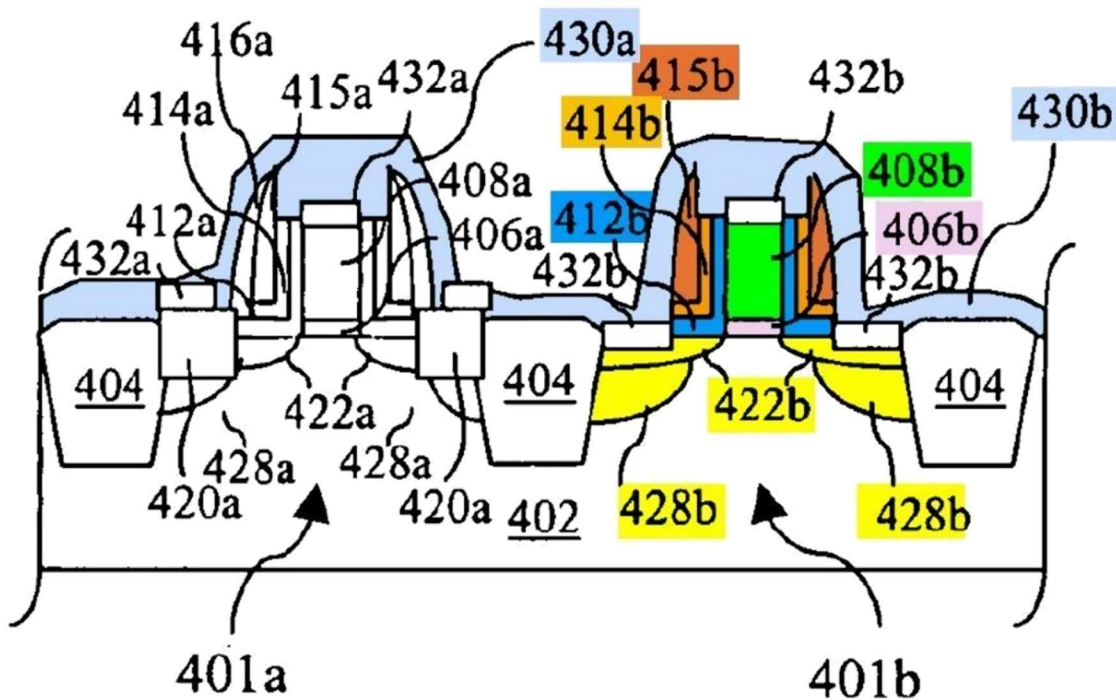
Cheng, Fig. 4j

(5) [11D]

Cheng's NMOS 401b includes a second sidewall spacer comprising sidewall structure 414b and spacer 415b. (Cheng ¶[0061].) As Fig. 4j shows, sidewall structures 414b (light orange) and spacers 415b (dark orange) are formed on the side surface of gate electrode 408b (green). (*Id.*; Ex-1003 ¶¶354-356.)

(6) [11E]

Cheng's NMOS 401b includes a second source/drain region of a second conductivity type (n-type) comprising lightly doped regions 422b and heavily doped regions 428b. (Cheng ¶[0060], ¶[0066], Figs. 4e-4j.) As Fig. 4j shows, Cheng's n-type source/drain regions (yellow) are formed on a lateral side of the second sidewall spacers (414b and 415b, orange). (Cheng, Figs. 4d-4j; Ex-1003 ¶¶357-359.)



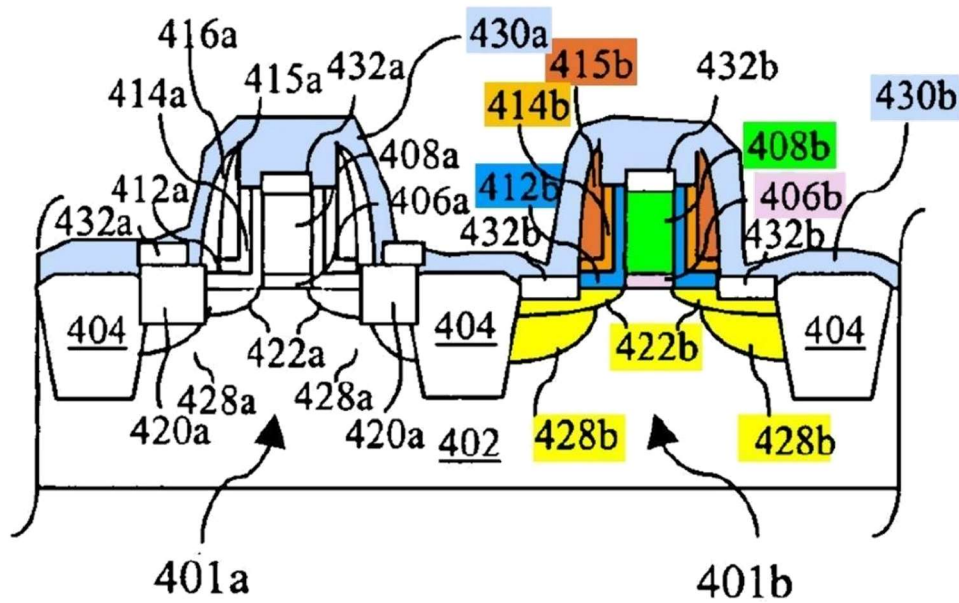
Cheng, Fig. 4j

(7) [11F]

Cheng’s stress insulating film (etch stop layer 430a/430b) is “formed over the semiconductor device(s) 401a [PMOS] and 401b [NMOS],” as Fig. 4j shows, to cover the NMOS gate electrode 408b, sidewall spacers 414b and 415b, and NMOS source drain regions 422b and 428b. (Cheng ¶[0070]; Ex-1003 ¶¶360-361.)

j. Claim 12

Cheng’s first stress-relief film, “dummy spacer 716b [sic:416b],” is “removed from the [NMOS] device 401b,” such that no stress-relief film remains on the second active region of NMOS 401b. (Cheng ¶[0066], Figs. 4e-4j; Ex-1003 ¶¶362-364.)



Cheng, Fig. 4j

2. Ground 2B: The Cheng-Wolf Combination Renders Obvious Claim 2

a. A POSITA Would Have Found the Cheng-Wolf Combination Obvious

For the reasons explained for Ground 1B, a POSITA would have been motivated to add an I-shaped offset spacer, as Wolf discloses, to Cheng's sidewall structures. (*Supra* §V.A.2; Ex-1003 ¶¶366-373; Wolf, 21-22, Fig. 5-25.) Using I-shaped offset spacers to control source/drain extension profiles and mitigate short-channel effects was well-known. (*Supra* §V.A.2.) A POSITA would have been motivated to add Wolf's I-shaped offset spacers to Cheng's transistors (*see* Figure J) to better control the doping profile of LDD region 422a and mitigate short-channel effects. (Ex-1003 ¶¶367-369.)

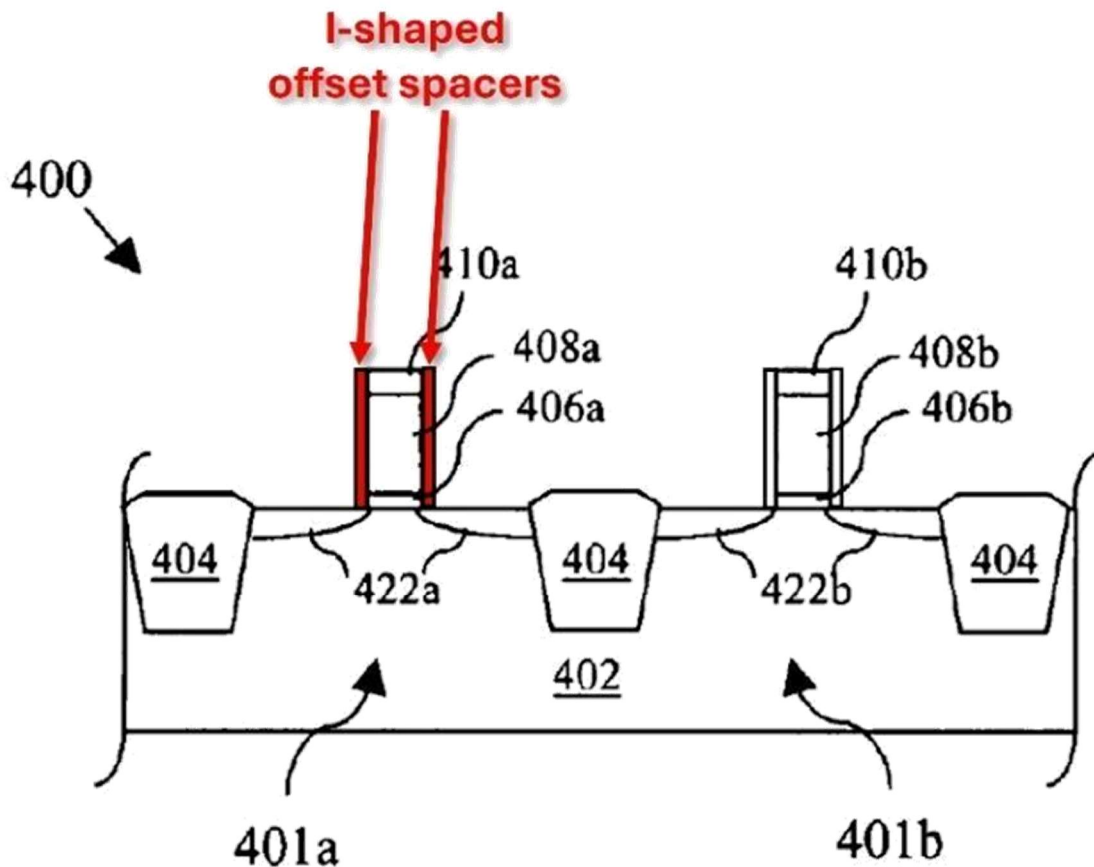


Figure J

A POSITA also would have reasonably expected to succeed because this represents a conventional use of a known technique to achieve ordinary, expected results. (Wolf, 22, Fig. 5-25; Ex-1039, 1, Fig. 2; Ex-1040, Tbl. 3.1; Ex-1041 ¶[0024], FIGS. 1a-2; Ex-1042 ¶[0058], FIGS. 2c-2h; Ex-1043 ¶[0033]; Ex-1044 ¶[0061]; Ex-1045 ¶[0080], ¶[0088], ¶[0091], FIGS. 8A-11C; Ex-1003 ¶370.) As Figure K shows, after using offset spacers to define Cheng's LDD region 422a (see Figure J above), a POSITA would have found it obvious to proceed with the remainder of Cheng's processing as it describes. (Ex-1003 ¶370.)

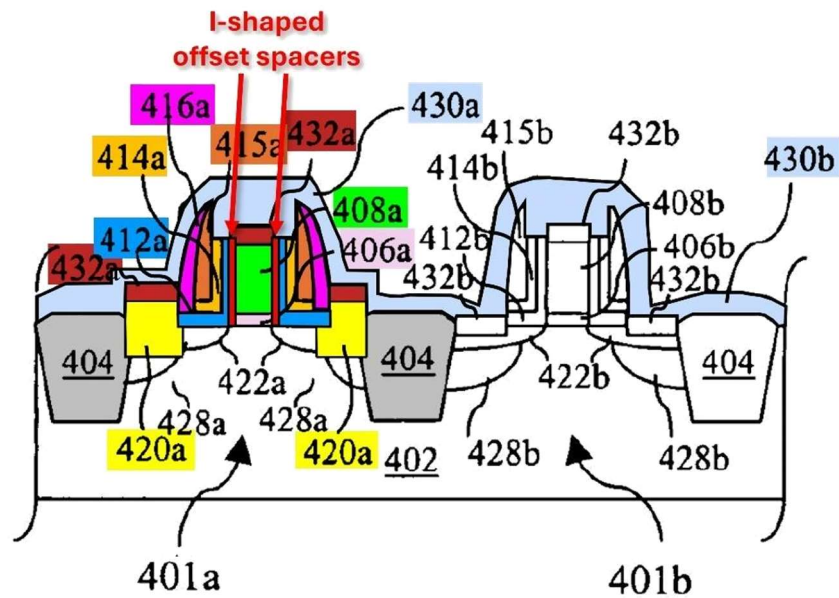


Figure K

A POSITA would have found it obvious to add I-shaped offset spacers to Cheng's transistors because it is an example of (a) combining known prior-art elements according to known methods (forming an I-shaped offset spacer) to yield predictable results (define source/drain extensions and mitigate short-channel effects); (b) using a known technique (forming an I-shaped offset spacer) to improve similar devices (Cheng's MOSFETs) in the same way; (c) applying these same known techniques (forming the I-shaped offset spacer) to improve a known device (Cheng's MOSFETs) and yield predictable results (optimal source/drain extensions and reduced short-channel effects); and (d) applying a known teaching, motivation, or suggestion in the prior art (e.g., the teachings in Wolf, Ex-1039, Ex-1040, and others noted above) to arrive at the claimed invention. (*KSR*, 550 U.S. at 416-21; Ex-1003 ¶371.)

b. Claim 2

A POSITA would have found it obvious to incorporate Wolf's I-shaped offset spacer (red) formed between Cheng's gate electrode 408a (green) and first sidewall spacer 414a and 415a (orange) to control the profile of LDD regions 422a, resulting in the structure below. (*Supra* §V.B.2.a; Ex-1003 ¶¶372-373.)

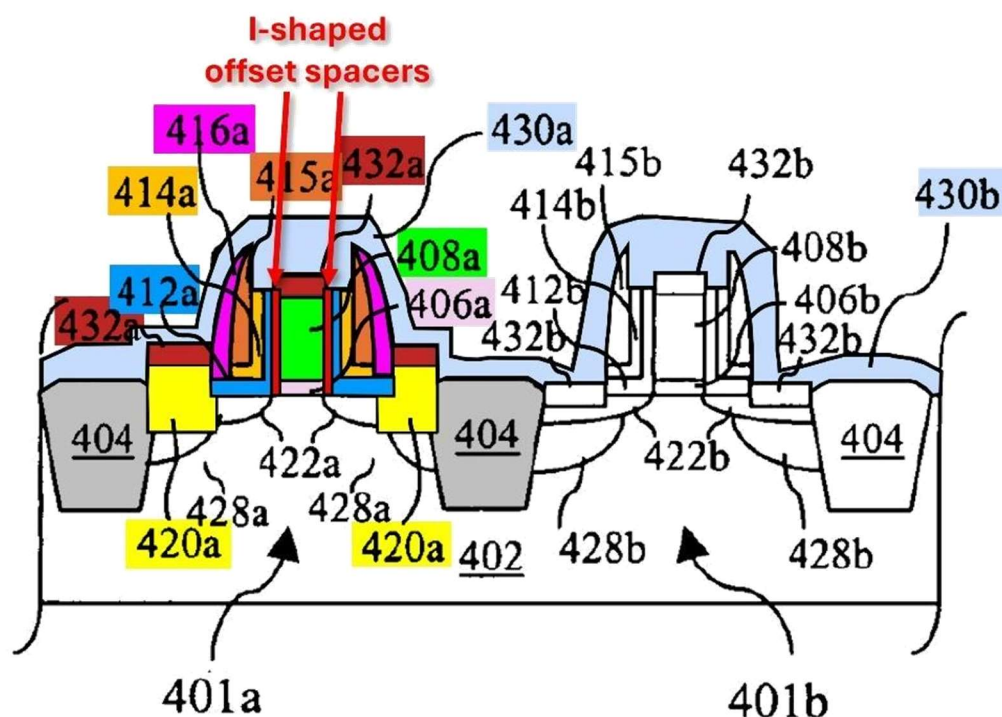


Figure K

3. Ground 2C: The Cheng-Wang Combination Renders Obvious Claims 1, 3-9, and 11-12

A POSITA would have found claims 1, 3-9, and 11-12 obvious based on the Cheng-Wang combination for the reasons stated in Sections V.B (introduction) and V.B.1 and the well-known advantages of raised SiGe. (*Supra* §II.B; Ex-1003 ¶374.)

4. Ground 2D: The Cheng-Wang-Wolf Combination Renders Obvious Claim 2

A POSITA would have found claim 2 obvious based on the Cheng-Wang-Wolf combination for the reasons stated in Sections V.B (introduction) and V.B.2. (Ex-1003 ¶375.)

C. Ground 3: Saito

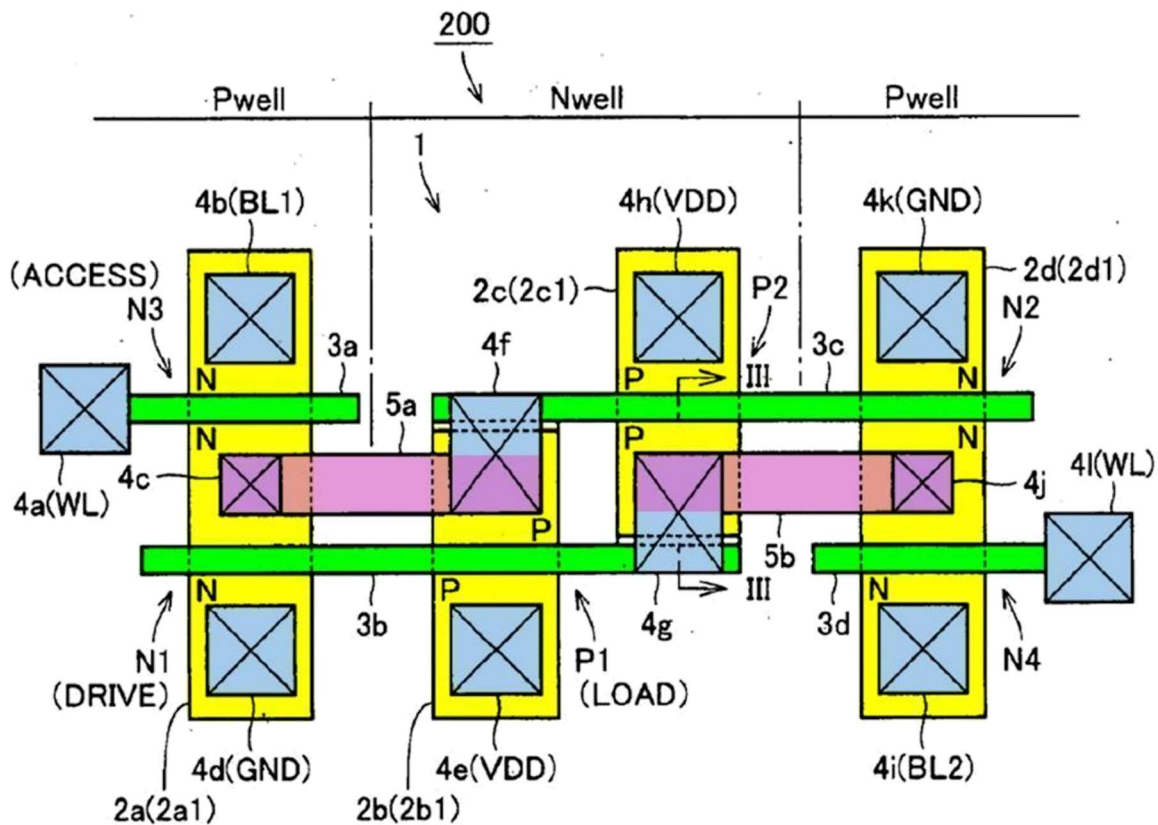
1. Ground 3: The Saito-Fukutome-James Combination Renders Obvious Claims 1, 3-4, 7-8, and 10

Saito discloses a textbook SRAM circuit (below) with levels 1-5 numbered in order from the bottom up:

- Substrate: 100 (uncolored). (Saito ¶[0072].)
- Active regions: 2a-2d (yellow). (Saito ¶¶[0060]-[0061].)
- Polysilicon wirings: 3a-3d (green). (Saito ¶¶[0067]-[0068], ¶[0124].)
- Contact parts: 4a-4l (blue). (Saito ¶¶[0068]-[0069].)
- Metal wirings: 5a-5b (purple). (Saito ¶¶[0070]-[0071].)

(Ex-1003 ¶¶377-378; *compare* Saito ¶¶[0003]-[0005], ¶¶[0049]-[0050], FIGS. 1-2, *with* Ex-1046, 19-20, Figs. 2.10(b)-(d); *see* Ex-1047, FIGS. 1-3; Ex-1048, Tbl. 1; Ex-1049, 1, Fig. 1; Ex-1050 ¶[0201], ¶¶[0204]-[0205], FIGS. 38-40B.)

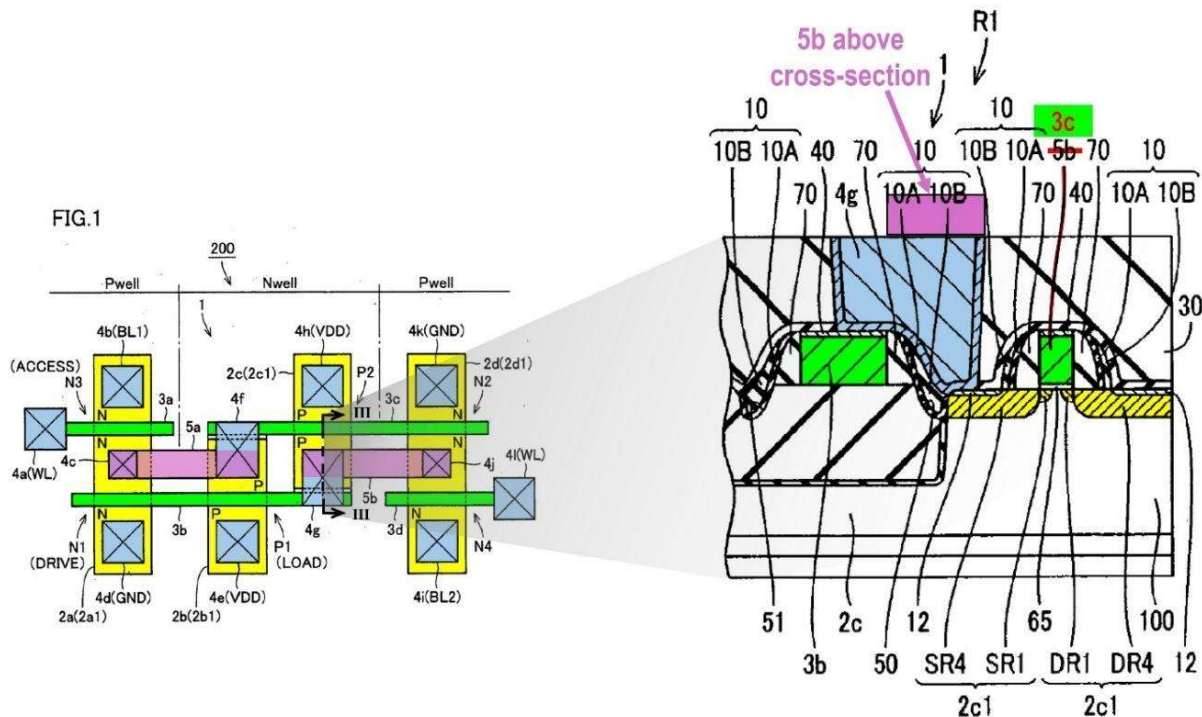
FIG.1



Saito, FIG. 1

Saito explains: “Polysilicon wirings 3a-3d [green] constitute a gate of each MOS transistor.” (Saito ¶¶[0067].) Saito’s “contact parts 4a-4l” (blue) connect the transistors with the “upper wiring” layer 5x (purple). (Saito ¶¶[0068], ¶¶[0071].) For instance, “metal wiring 5b” connects contact part 4g at “the drain of second load transistor P2” with “contact part 4j” at the “drain of second driver NMOS transistor N2.” (*Id.*) Because metal wiring 5b is an “upper wiring” that connects contact parts 4g and 4j, a POSITA would have understood it lies above the cross-sections in FIGS. 3-21. (Ex-1003 ¶¶[379-380; Ex-1047 ¶¶[0038]-[0040], FIGS. 1-3.)

Like FIGS. 3-11, region R1 in Saito's FIGS. 12-21 shows cross-sections along outline III-III in FIG. 1. (*Compare Saito ¶[0030], ¶[0072], FIGS. 3-11, with Saito, FIGS. 12-21.*) A POSITA would have recognized "5b" in FIGS. 12-21 identifies the polysilicon gate of PMOS transistor P2 and thus should be labeled "polysilicon wiring 3c." (Ex-1003 ¶¶381-389.)



Saito, FIG. 1

Saito, FIG. 12 (excerpted, adding 5b)

The annotated figure below shows a perspective view of an SRAM like Saito's, up to level 3 (polysilicon, green). (Ex-1003 ¶383.)

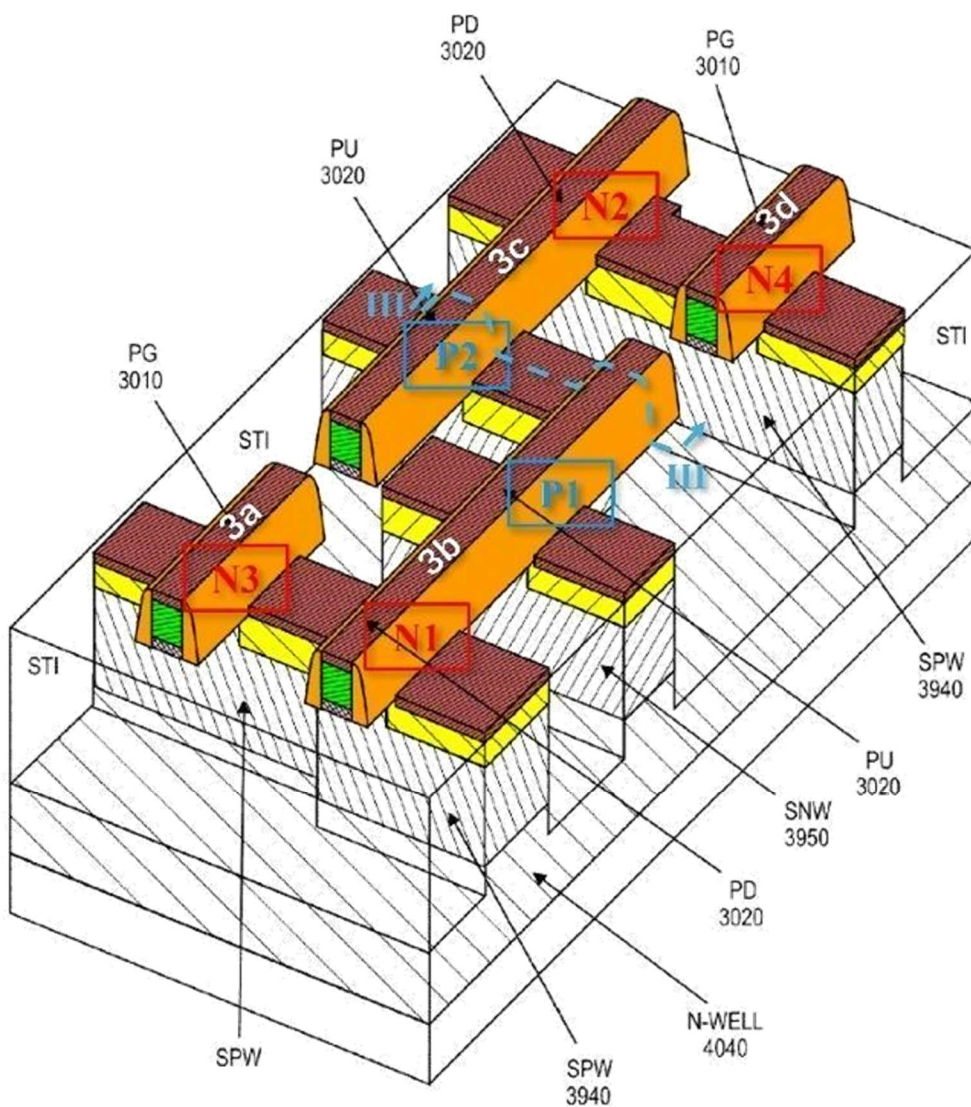


FIG. 40B

Ex-1050, FIG. 40B

A POSITA would have recognized that, because Saito's contacts 4g/4j and metal wiring 5b are textbook SRAM structures, metal wirings (5x) would have been located higher than the polysilicon lines (3x) and contacts (4x), as Figure L shows below (amending and annotating Ex-1050, FIG. 40B). (Ex-1003 ¶384; Ex-1046, 19-20, Figs. 2.10(b)-(d); Ex-1047, FIGS. 1-3; Ex-1049, Figs. 1-2.)

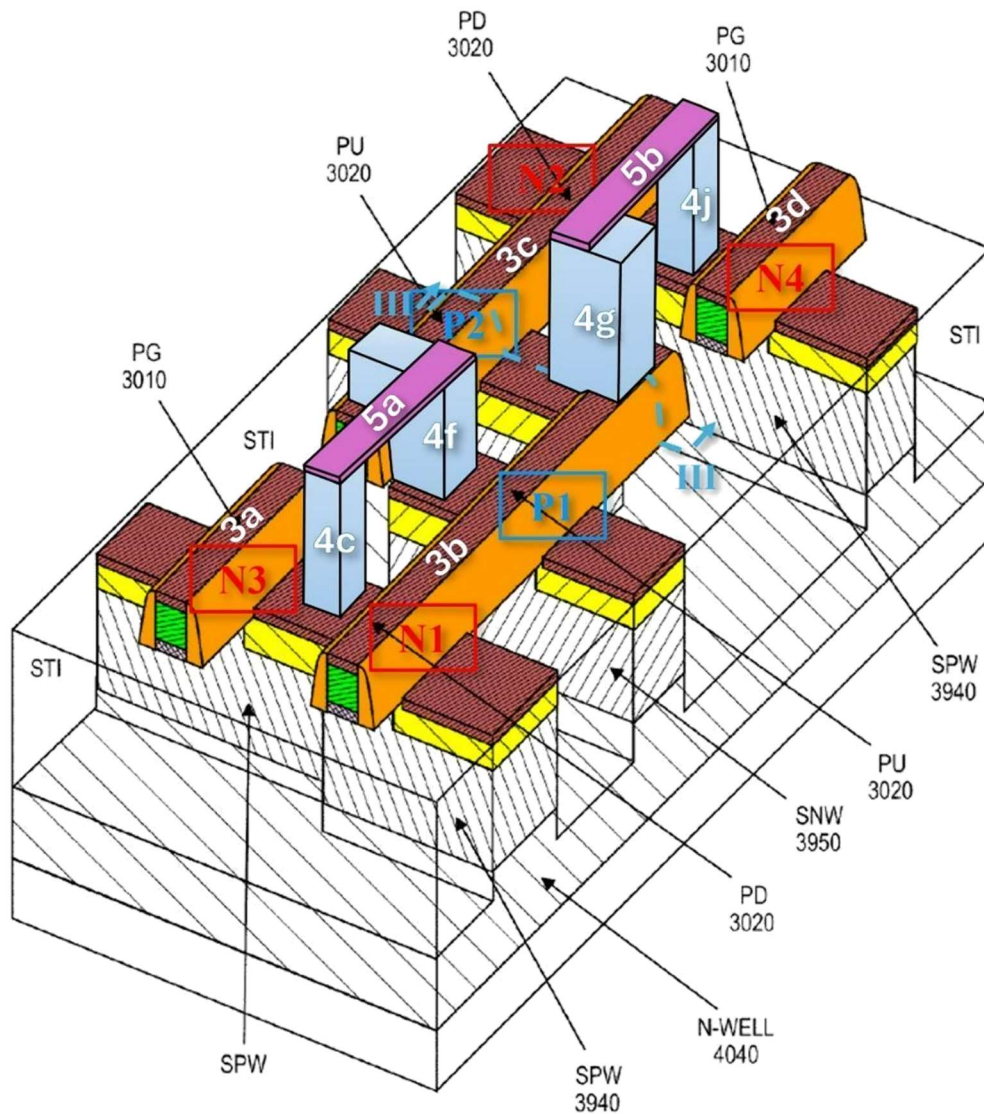


FIG. 40B

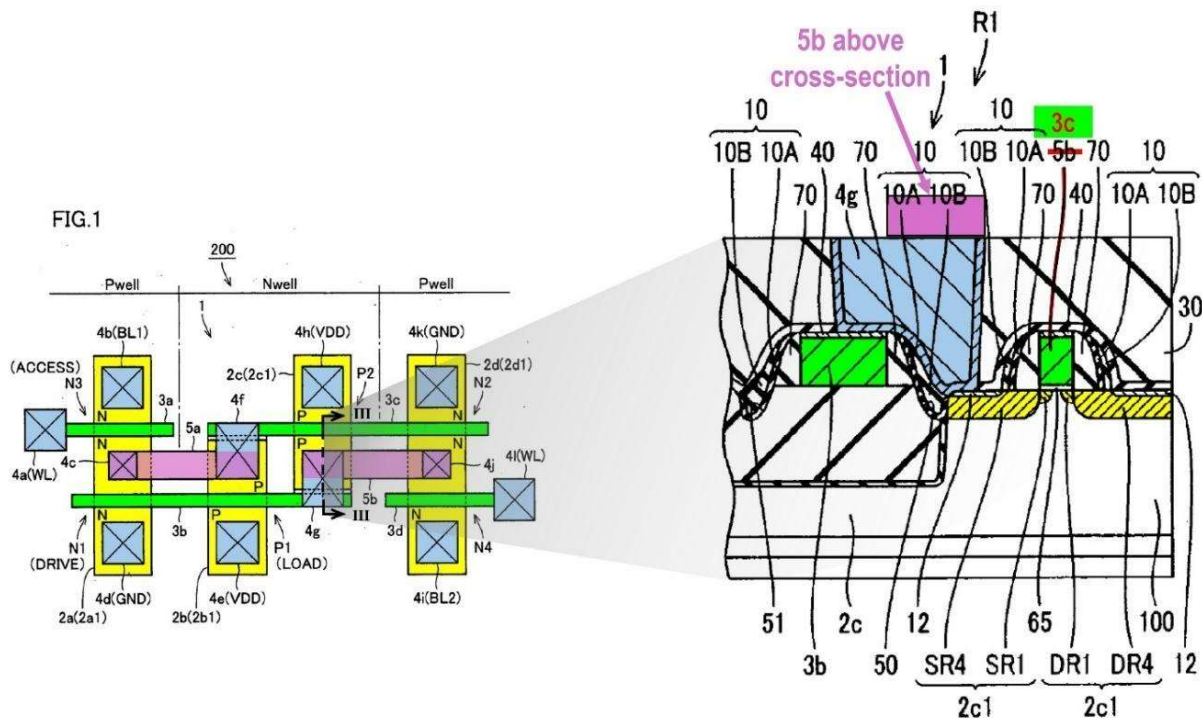
Figure L

A POSITA would have immediately recognized that “polysilicon wiring 5b” refers to “polysilicon wiring 3c” in FIGS. 12-21. (Ex-1003 ¶385; see *LG Elecs. Inc. v. ImmerVision, Inc.*, 39 F.4th 1364, 1372 (Fed. Cir. 2022) (explaining such clerical errors should be disregarded).)

Saito describes each of these textbook SRAM layers with a shared numeric level identifier (2x, 3x, 4x, 5x), such that a POSITA would have recognized “polysilicon wiring 5b” in Saito’s FIGS. 12-21 correctly points to a polysilicon wiring. But it is polysilicon wiring “3c” because no polysilicon wiring “5b” exists. (Ex-1003 ¶386; *see* Ex-1046, 19-20, Figs. 2.10(b)-(d); Saito ¶¶[0065]-[0068], ¶[0124], FIGS. 1-2.) A POSITA would have immediately noted that “polysilicon wirings” are designated 3x, such that FIGS. 12-21 show polysilicon wiring “3c” from FIG. 1, not “metal wiring 5b.” (Saito ¶¶[0066]-[0068], ¶[0071]; Ex-1003 ¶386.) A POSITA would have understood, as Saito explains, that “metal wiring 5b” is an “upper wiring” at contacts 4g/4j and is located above Saito’s cross-sections. (Ex-1003 ¶386; Saito ¶¶[0067]-[0071]; Ex-1046, 19-20, Figs. 2.10(b)-(d); Ex-1047, FIGS. 1-3.)

Moreover, cross-section III-III in FIG. 1 shows contact part 4g intersecting polysilicon wiring 3b and metal wiring 5b, not polysilicon wiring 3c. Saito FIG. 1. “[P]olysilicon wiring 3c,” on the other hand, lies beside contact part 4g and serves as the polysilicon gate for PMOS transistor P2. (Ex-1003, ¶387.) Saito’s references to “polysilicon wiring 5b” thus describe what is shown in FIG. 1 as “3c”—the gate of transistor P2, which does not touch contact 4g. This confirms polysilicon wiring “5b” is a clerical error; it is “polysilicon wiring 3c,” as shown below. (Saito ¶¶[0093]-[0096], ¶[0101], FIGS. 1, 12-21; Ex-1003, ¶387.) The element mislabeled

“5b” in FIGS. 12-21 lies above gate insulating film 65, indicating it is polysilicon gate 3c.¹⁷ (Saito ¶[0051]; Ex-1003 ¶¶388-389.)



Saito, FIG. 1

Saito, FIG. 12 (excerpted, adding 5b)

Correcting this obvious typographical error, region R1 in FIGS. 12-21 reflects the correct cross-section corresponding to outline III-III in FIG. 1, as expected for this conventional SRAM. (Ex-1003 ¶¶390-394 (discussing Ex-1047); Ex-1047

¹⁷ If it were metal wiring 5b, gate *insulating film* 65 would sever the connection between node Nb and transistor N4 in FIG. 2, which is prohibited. (Ex-1003 ¶388; see Saito, ¶[0071], FIGS. 1-2, 12; Ex-1046, 19-20, Figs. 2.10(b)-(d).)

¶¶[0062]-[0063], ¶¶[0065]-[0066], FIGS. 1-3; Ex-1046, 19-20, Figs. 2.10(b)-(d); Ex-1049, Figs. 1-2.)

A POSITA would have readily understood this because Saito does not purport to alter the wiring or structure of the textbook SRAM. (Ex-1046, 19-20, Figs. 2.10(b)-(d); Ex-1003 ¶395.) Saito instead addresses problems associated with recesses 50 that form in isolation regions. (Saito, Abstract, ¶[0011], ¶¶[0022]-[0023], ¶[0027], ¶¶[0074]-[0075].)

At bottom, no matter how one views Saito, a POSITA would have recognized polysilicon wiring 3c in FIG. 1 has the structure incorrectly labeled “5b” in FIGS. 12-21, because the various layers use their own respective numeric designators. (Ex-1003 ¶396.) Thus, (1) a POSITA would have immediately recognized Saito’s clerical error that “polysilicon wiring 5b” refers to “polysilicon wiring 3c,” and, regardless, (2) the structure labeled “polysilicon wiring 5b” in FIGS. 12-21 is a MIS transistor as discussed below. (Ex-1003 ¶396.)

a. A POSITA Would Have Found the Saito-Fukutome-James Combination Obvious

A POSITA would have understood Saito’s “plasma nitride (SiN)” insulating film 13 is a CESL. (Saito ¶[0072], ¶¶[0080]-[0084], FIGS. 3, 12, 21; Ex-1003 ¶398.) A POSITA would have found it obvious to make CESL 13 tensile as a known way

to improve NMOS performance, consistent with James. (*Supra* §II.B, §V.A.1.a; Ex-1024 ¶¶[0090], ¶¶[0099]-[0100], Tbl. V; James, 2; Ex-1003 ¶401.)

A POSITA also would have found it obvious to substitute Fukutome's raised epitaxial SiGe PMOS source/drain layers for Saito's non-epitaxial PMOS source/drain layers in active regions 2b/2c to improve the P1/P2 devices through compressive strain, yielding the structure in Figure M.¹⁸ (*Supra* §II.B; Fukutome ¶[0110]; Ex-1003 ¶¶398-402.)

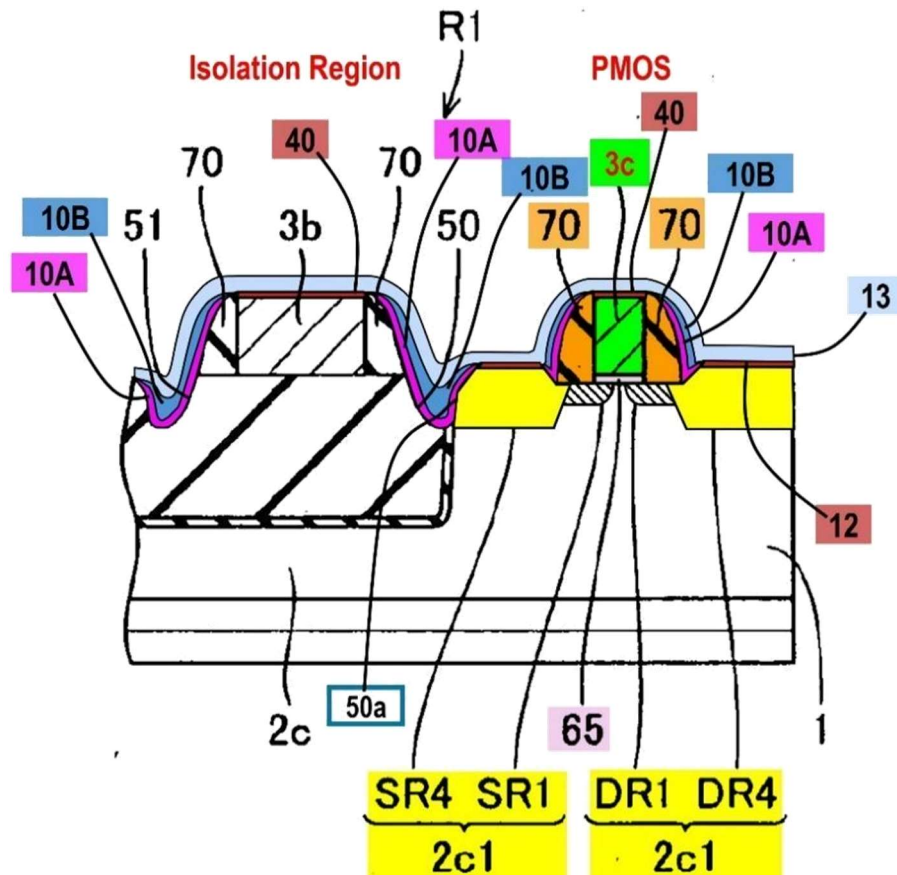


Figure M (similar to FIG. 21; Ex-1003 ¶399)

¹⁸ Figure M corrects the 5b/3c clerical error. (*Supra* §V.C.1.)

**(1) A POSITA would have been motivated to make the
Saito-Fukutome-James combination**

(a) Raised SiGe source/drain regions

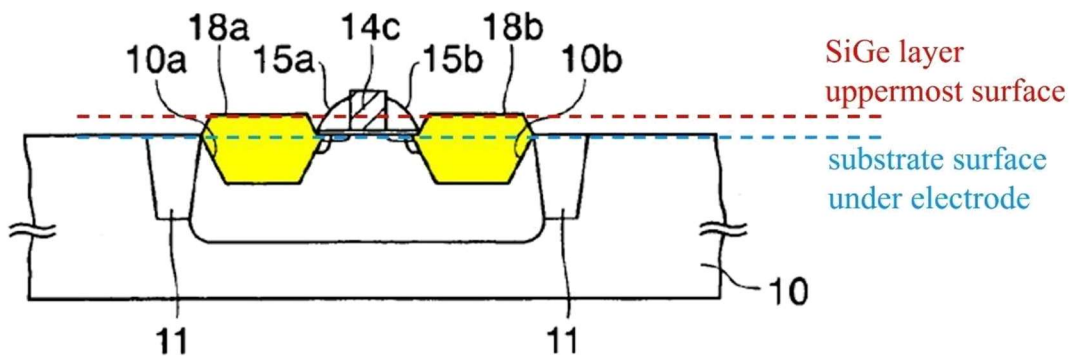
A POSITA would have found it obvious to incorporate Fukutome's raised SiGe source/drains into Saito's PMOS devices to improve performance. (Ex-1003 ¶403; *supra* §II.B.)

Saito discloses source/drain regions 2c1. (Saito ¶[0094], ¶[0097], ¶[0101], FIGS. 12, 17, 21.) Saito's FIGS. 16-17 show shallow source/drain diffusion (extension) regions SR1/DR1 being formed before sidewalls 70 using polysilicon wiring 5b [sic:3c] as a mask. (Saito ¶[0094], FIG. 16.) Deep source/drain diffusion regions SR4/DR4 are then formed using sidewalls 70 as a mask. (Saito ¶[0097], ¶[0101], ¶[0124], FIG. 17; *supra* §V.C.1; Ex-1003 ¶¶404-405.)

Fukutome's FIGS. 5B-5E disclose a substantially similar process to form source/drain diffusion regions 16a/16b using "gate electrode 14c as a mask," then to form source/drain diffusion regions 17a/17b using "gate electrode 14c and the first sidewalls 15a and 15b as a mask." (Fukutome ¶¶[0082]-[0083], ¶[0087], FIGS. 5B-5C; Ex-1003 ¶¶406-407.)

Fukutome discloses an improvement to this process: adding raised epitaxial SiGe source/drain regions 18a/18b. (Fukutome ¶¶[0097]-[0102], ¶[0110], FIGS. 5C-5E; *supra* §II.B.) Fukutome's FIGS. 5D-5E show etching recesses

10a/10b to expose the (111) Si planes of substrate 10 and growing SiGe epitaxial layers 18a/18b extending above the substrate next to sidewalls 15a/15b. (Fukutome ¶[0092], ¶¶[0097]-[0102], FIGS. 5D-5E.) Fukutome's epitaxial SiGe layers introduce compressive stress to the PMOS channel regions. (Fukutome ¶[0005], ¶[0110], ¶[0249], FIG. 5G (arrows); *supra* §II.B.)



Fukutome, FIG. 5E

For reasons in Section II.B, a POSITA would have found it obvious to incorporate Fukutome's epitaxial SiGe into Saito's PMOS devices (active regions 2b/2c) to improve "the mobility of carriers in the channel" and "the drive capability of the MOS transistor." (Fukutome ¶[0110]; *see* Ex-1003 ¶¶408-412.) Additionally, a POSITA would have found it obvious to incorporate Fukutome's SiGe layers into Saito's PMOS devices to suppress junction leakage and improve reliability. (Fukutome ¶[0100]; Ex-1003 ¶409, ¶412.) Such benefits were well-known. (Ex-1003 ¶413.) The four most recent generations of high-volume commercial devices all used raised SiGe source/drain regions. (*Supra* §II.B; James, 2.)

Figure M illustrates a structure¹⁹ incorporating Fukutome's raised SiGe source/drain regions into Saito's active regions 2b/2c.

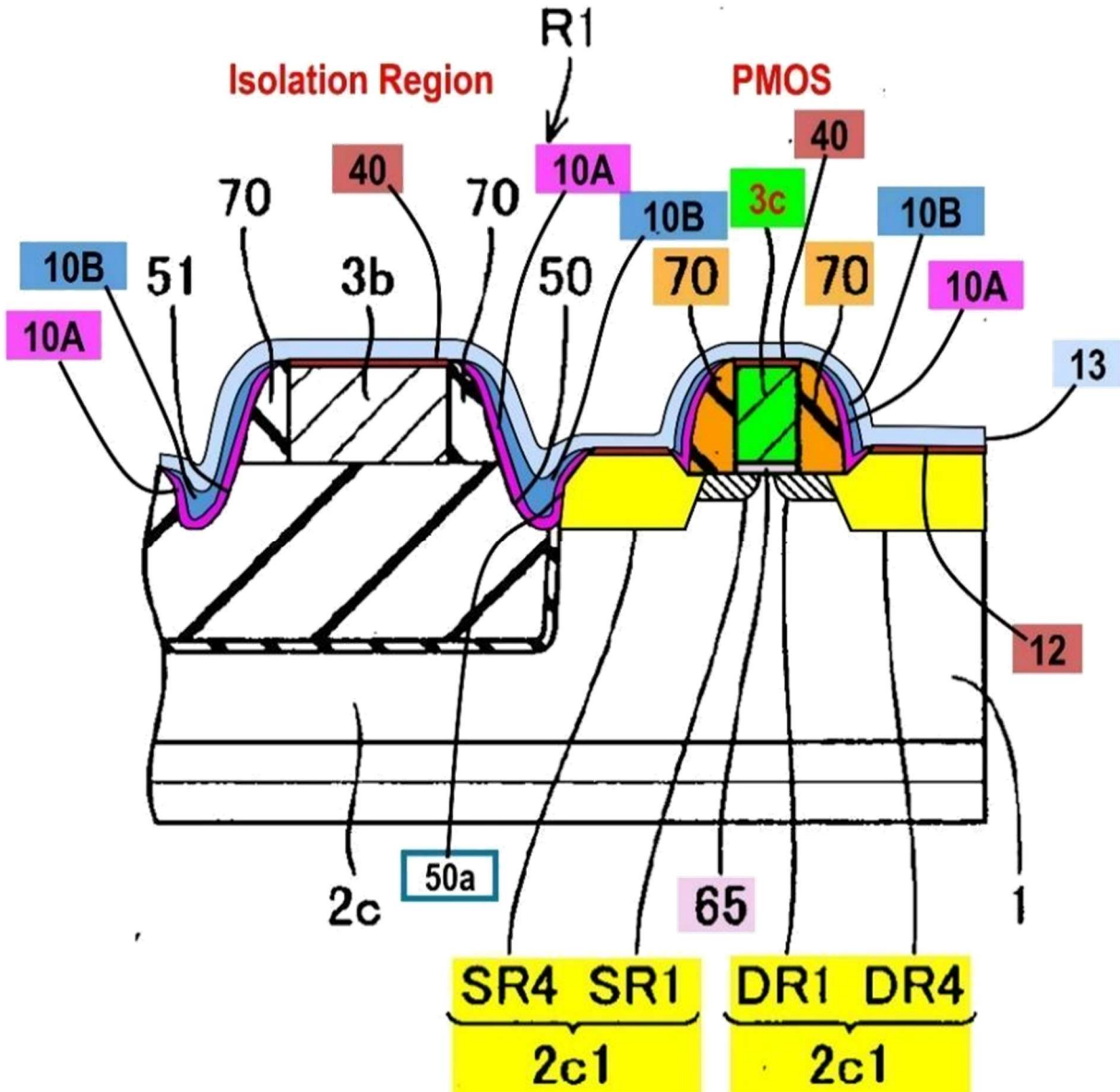


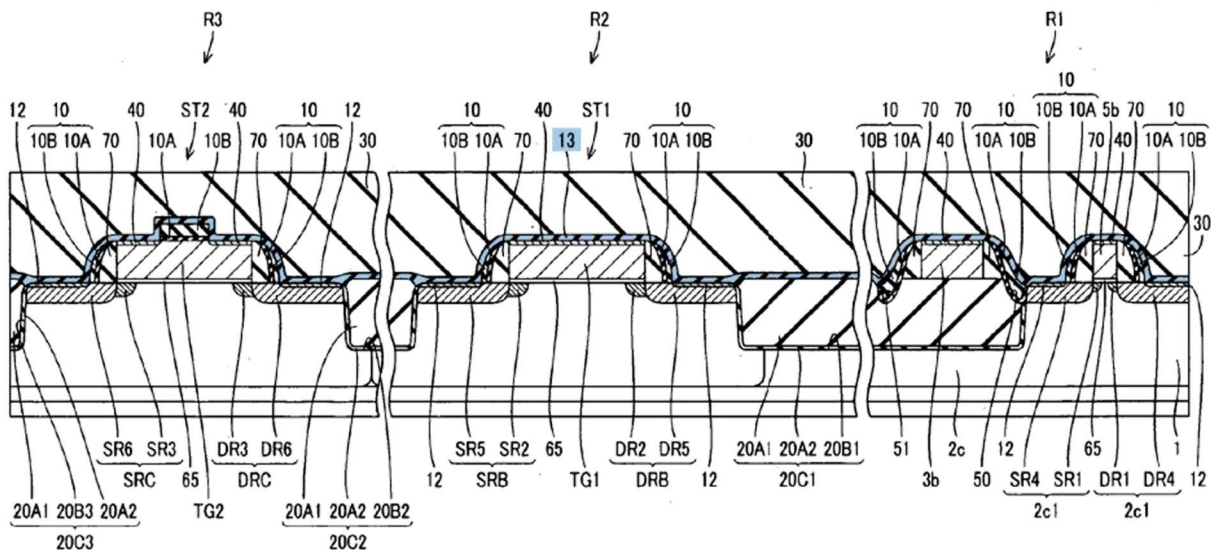
Figure M

¹⁹ After forming Fukutome's SiGe source/drain layers, the process flow in the proposed combination would continue as in Saito. (Ex-1003 ¶415 n.30.)

(b) Tensile silicon nitride layer 13

Saito’s SiN layer 13 blankets the entire SRAM circuit. (Saito ¶¶0091] (explaining FIG. 12 shows “well region[s] of various conductivity types”), FIGS. 12, 21 (showing same).) A POSITA would have been motivated to make Saito’s SiN layer 13 tensile to improve electron mobility in NMOS channel regions (e.g., active regions 2a/2d). (*Supra* §II.B; Saito ¶¶0063]-[0065], FIG. 1; Ex-1003 ¶¶416-418.)

FIG.21



Saito, FIG. 21

Although Saito is silent regarding strain in SiN layer 13, James demonstrates that a POSITA would have found a tensile SiN layer 13 obvious. (Ex-1003 ¶¶419-421.) James explains “a highly stressed nitride sealant layer” (CESL) can “increase[] electron mobility” and “involves no extra cost for either capital equipment or special substrates,” which a POSITA would have found attractive.

(James, 2, 5.) It was well-known that a silicon nitride CESL prepared under certain conditions can “apply[] stress to [a] channel region” to improve carrier mobility. (Ex-1023 ¶[0003]; *see* Ex-1024 ¶[0090], ¶¶[0099]-[0100], Tbl. V; Ex-1025 ¶[0003]; James, 2; Ex-1022, 1-2; Ex-1003 ¶422.)

A POSITA would have been motivated make Saito’s SiN layer 13 tensile as a simple and inexpensive way to improve electron mobility in transistors N1-N4. (Ex-1003 ¶423, ¶425.) A POSITA further would have understood such tensile stress in PMOS devices P1/P2 would have been mitigated by the presence of a buffer layer and outweighed by compressive SiGe stress. (*Supra* §V.C.1.a(1)(a), §II.C; Ex-1022, 1-2; James, 2; Ex-1023 ¶[0039]; Alvarez ¶[0047], ¶[0049], ¶[0054], ¶[0065], Tbl. 1, FIG. 9; Ex-1003 ¶424.)

(2) A POSITA would have reasonably expected to succeed in the Saito-Fukutome-James combination

A POSITA would have reasonably expected to succeed in adding raised, compressive SiGe PMOS source/drain regions to Saito’s PMOS transistors (as Fukutome teaches) and in using a tensile silicon nitride CESL 13 (as James teaches). (Ex-1003 ¶¶426-433.)

Incorporating Fukutome’s SiGe source/drains would have required nothing more than the conventional steps of trenching Saito’s silicon substrate and epitaxially growing SiGe regions after forming shallow source/drain extensions

(SR1/DR1). (*Compare* Saito ¶¶[0092]-[0103], FIGS. 16-17, *with* Fukutome ¶¶[0085]-[0102], FIGS. 5C-5E; Ex-1003 ¶427.) Then, Saito's fabrication process would have continued as Saito describes by forming layers 10A/10B and making SiN layer 13 tensile as in James. (Saito ¶¶[0104]-[0106], FIG. 18; James, 2.) Adding Fukutome's SiGe source/drain layers to Saito's PMOS active regions 2b/2c would have achieved the ordinary, expected result of compressively stressing PMOS channels to boost performance. (*Supra* §II.B, §V.C.1.a(1)(a); Ex-1003 ¶¶427-428.)

Similarly, a POSITA would have reasonably expected to succeed in making Saito's SiN insulating layer 13 tensile, which had also been in commercial use for years, by using conventional deposition steps. (*Supra* §II.B; Ex-1024 ¶¶[0099]-[0100], Tbl. V; Saito ¶[0080], ¶¶[0120]-[0121], FIGS. 12, 18; James, 2, 5; Alvarez ¶[0054], ¶[0065], ¶[0069], Tbl. 1; Ex-1023 ¶[0003], ¶¶[0037]-[0039]; Ex-1022, 1-2; Ex-1003 ¶429.) Depositing a tensile SiN layer 13 would have achieved the ordinary, expected result of applying tensile stress to boost electron mobility in Saito's NMOS regions 2a/2d. (Ex-1003 ¶430.) James confirms expected success, showing a commercial device years before the '425 Patent with both raised, faceted epitaxial SiGe source/drain regions and a tensile CESL. (James, 2-3, Fig. 6; Ex-1003 ¶¶431-432.)

A POSITA would have found the proposed combination obvious because it (a) combines known prior-art elements (epitaxial SiGe source/drain regions and

tensile SiN CESL) according to known methods (known SiGe epitaxy and SiN deposition techniques) to yield predictable results (strained-channel transistors with improved performance); (b) substitutes one known element for another (SiGe PMOS source/drains regions for Saito's non-epitaxial PMOS source/drain regions and a tensile CESL for Saito's SiN CESL 13) to obtain predictable results (strained-channel transistors with improved performance); (c) using known epitaxial growth and deposition techniques to improve similar MOSFET devices in the same way; (d) applying known epitaxial growth and deposition techniques to improve Saito's MOSFET device and yield predictable results; and (e) applying a known teaching, motivation, or suggestion in the art (as explained above) to arrive at the claimed invention. (*KSR*, 550 U.S. at 416-21; Ex-1003 ¶433.)

b. Independent Claim 1

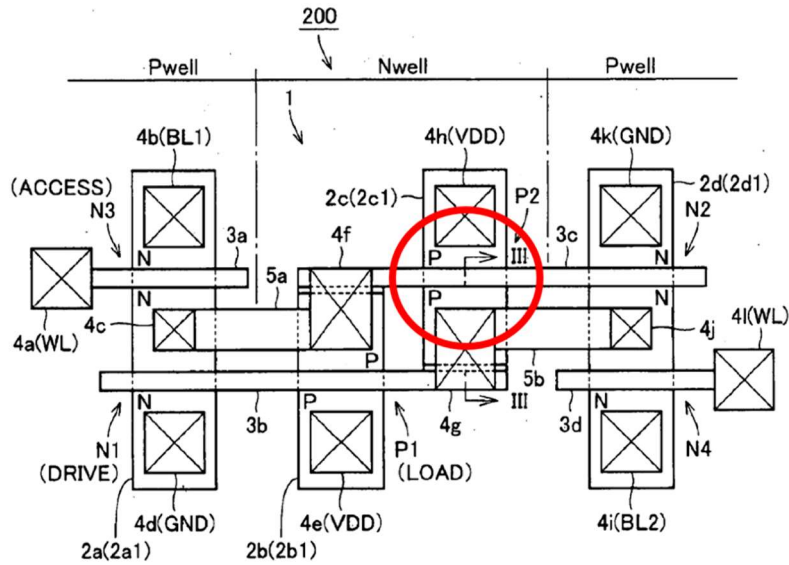
(1) [1Pre]

Saito discloses “a semiconductor device.” (Saito ¶[0002]; *see id.* ¶¶[0023]-[0026], ¶[0051], ¶[0066], FIGS. 1, 12, 21; *supra* §V.C.1.a; Ex-1003 ¶434.)

(2) [1A]

Saito discloses a first MIS transistor, e.g., PMOS transistor P2 in active region 2c. (Saito ¶[0057], FIGS. 1, 3, 12, 21; *supra* §V.C.1.a; Ex-1003 ¶¶435-438.) Saito's “PMOS transistor P2 is formed in the intersection part of impurity diffusion

region 2c1 comprising the region used as a source/drain, and polysilicon wiring 3c”
(see Figure M). (Saito ¶[0066]; Ex-1003 ¶436; *supra* §V.C.1.)



Saito, FIG. 1

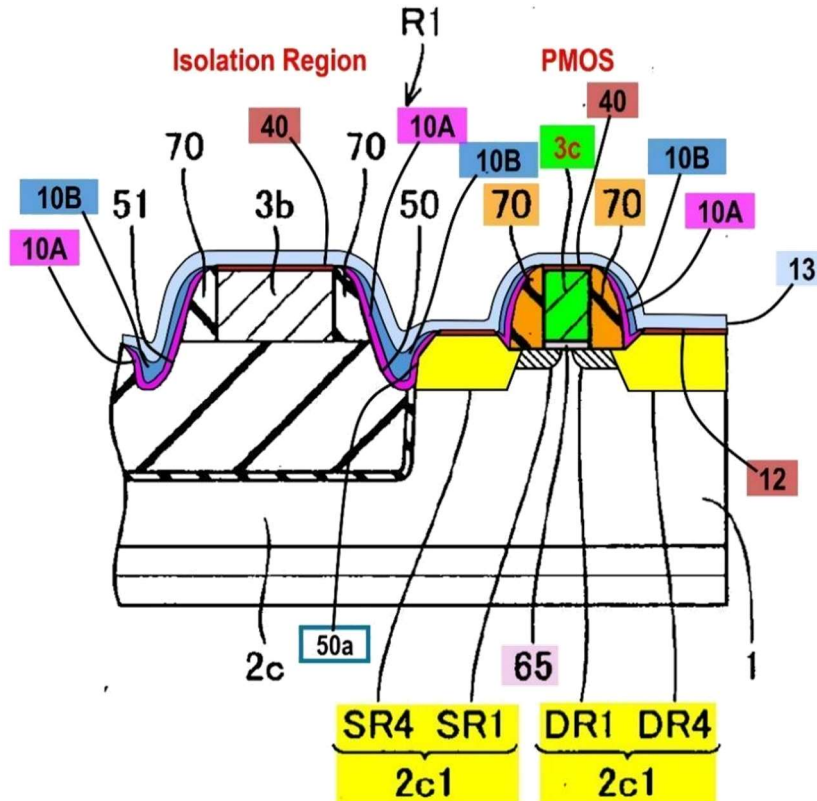


Figure M

(3) [1B]

Saito discloses a gate insulating film 65 formed on active region 2c of substrate 100 (*see* Figure M). (Saito ¶[0051], FIGS. 12, 21; *supra* §V.C.1.a; Ex-1003 ¶439.)

(4) [1C]

Saito discloses polysilicon wiring 5b [sic:3c] “formed on the upper surface of this gate insulating film 65” (*see* Figure M). (Saito ¶[0051], ¶[0066], ¶[0124], FIGS. 12, 21; *supra* §V.C.1.a; Ex-1003 ¶¶440-441.)

(5) [1D]

Saito discloses that “sidewall 70 is formed on the [sic] both side surfaces of ... polysilicon wiring 5b [sic:3c], and polysilicon wiring 3b” (*see* Figure M). (Saito ¶[0077], ¶[0096], ¶[0124], FIG. 17; *supra* §V.C.1.a; Ex-1003 ¶¶442-443.)

(6) [1E]

In the combination, “SiGe layers to be used as source/drain electrodes are epitaxially grown in the recesses, thus introducing strain into a channel.” (Fukutome ¶[0005]; *see id.* ¶[0110]; *supra* §V.C.1.a; Ex-1003 ¶¶444-447.) The “lattice spacing of SiGe” results in compressive stress “applied to a channel under the gate electrode.” (Fukutome ¶[0110]; *see id.* ¶[0249], FIG. 5G; *supra* §II.B, §V.C.1.a(1)(a)). SiGe source/drain regions (yellow) would be grown in trenches etched in Saito’s active region 2c on lateral sides of sidewalls 70 (orange) to cause

compressive stress along the gate length direction of the channel regions (under gate insulating film 65) (see Figure M). (*Supra* §V.C.1.a(1); Ex-1003 ¶447.)

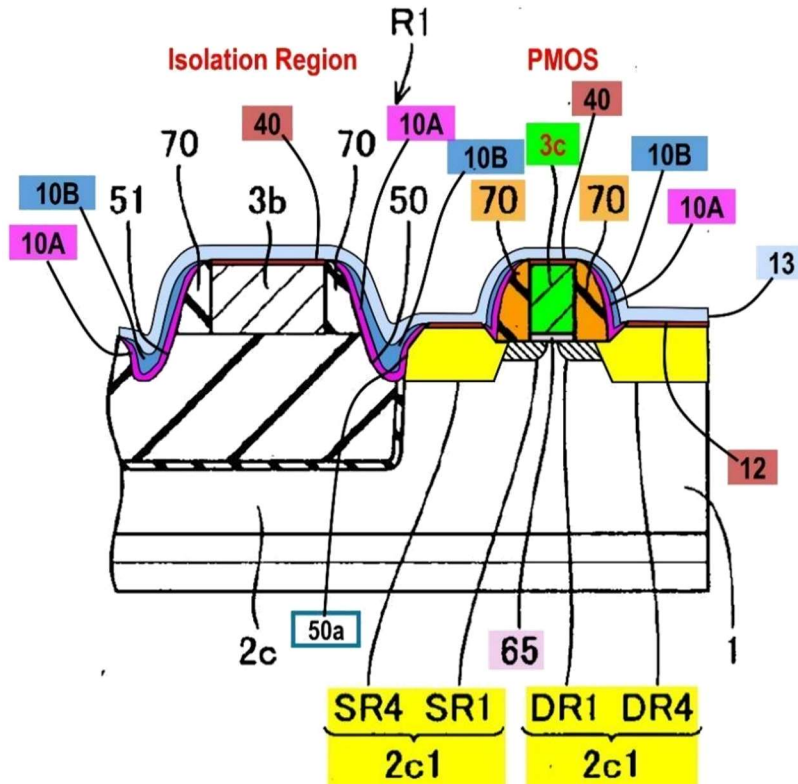


Figure M

(7) [1F]

Saito’s layers 10A/10B are deposited and etched to expose wiring 5b [sic:3c] for silicidation. Then, “insulating film 13 ... is formed on silicide films 12 and 40 and consists of a plasma nitride (SiN).” (Saito ¶[0080], ¶[0120], FIGS. 3, 9-12, 21; see Fukutome ¶[0106], FIG. 5G; James, 2-3, Fig. 6.)

A POSITA would have found a tensile SiN insulating film 13 obvious, as James discloses, because “[l]ocalized tensile stress is applied to the channels of NMOS devices,” which can “increase[] electron mobility” and “enhance NMOS

performance” without “extra cost for either capital equipment or special substrates.” (James, 2, 5, Fig. 6; *supra* §II.B, §V.C.1.a(1)(b).) A tensile insulating film 13 would form over “[c]rystalline facets” of the “raised [SiGe] source/drains” (*see* Figure M). (James, 2; *see id.*, Fig. 6; Ex-1003 ¶¶448-450.)

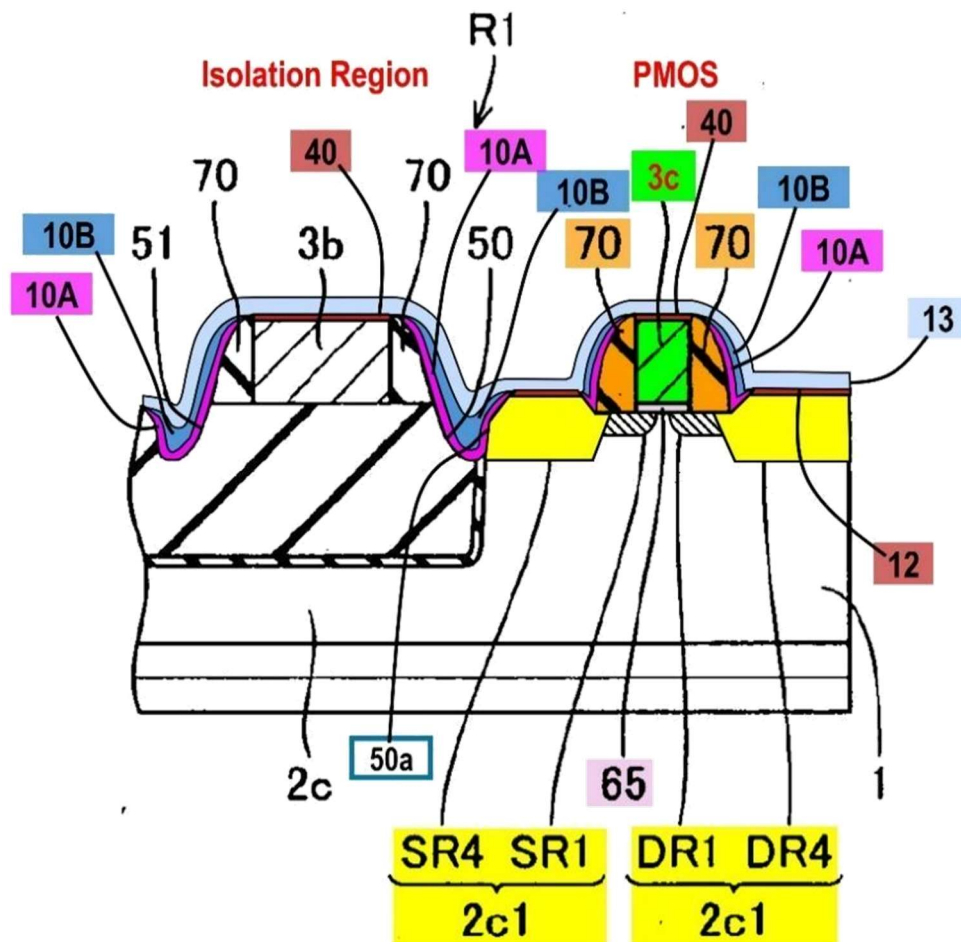


Figure M

(8) [1G]

Fukutome’s FIGS. 5D-5E teach epitaxial SiGe layers extending above the substrate. (Ex-1003 ¶¶451-453; *supra* §V.C.1.a(1)(a), §V.C.1.b(6).) Fukutome teaches to “form[] the upper surfaces of the source/drain material layers 18a and 18b

at positions higher than the surface of the silicon substrate 10.”²⁰ (Fukutome ¶[0100], FIG. 5E; *supra* §V.C.1.a(1)(a).)

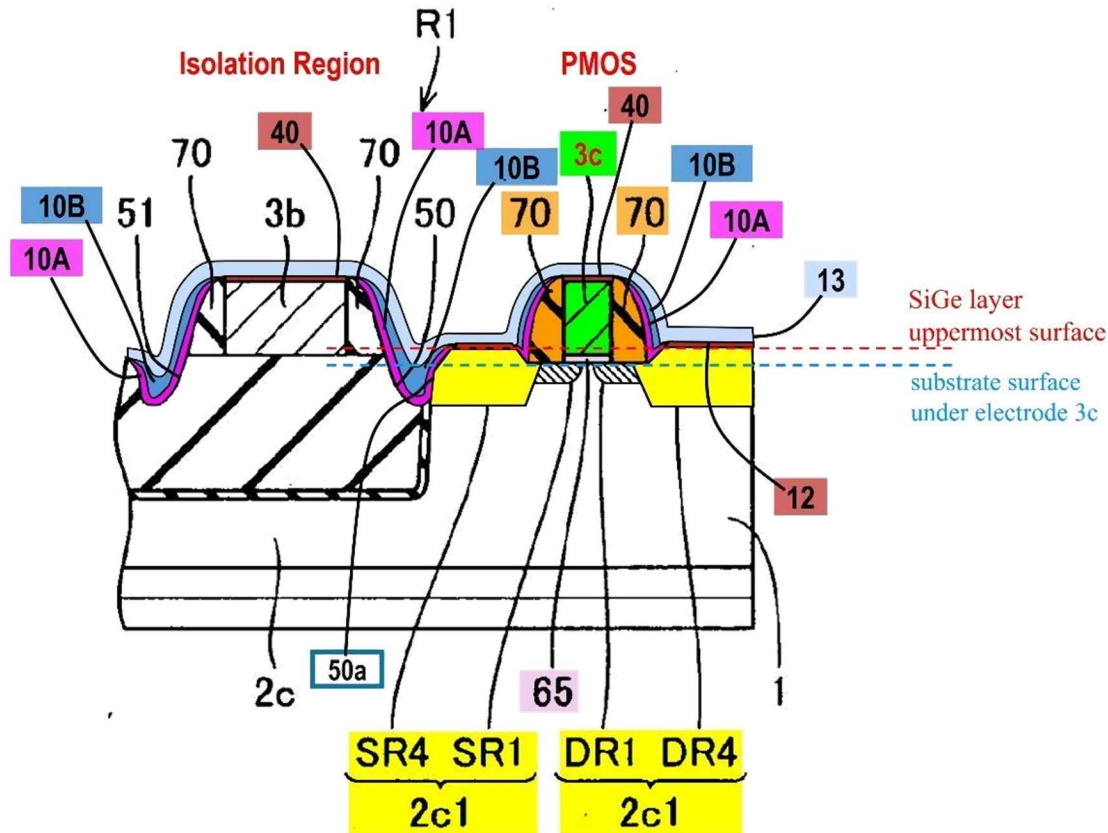
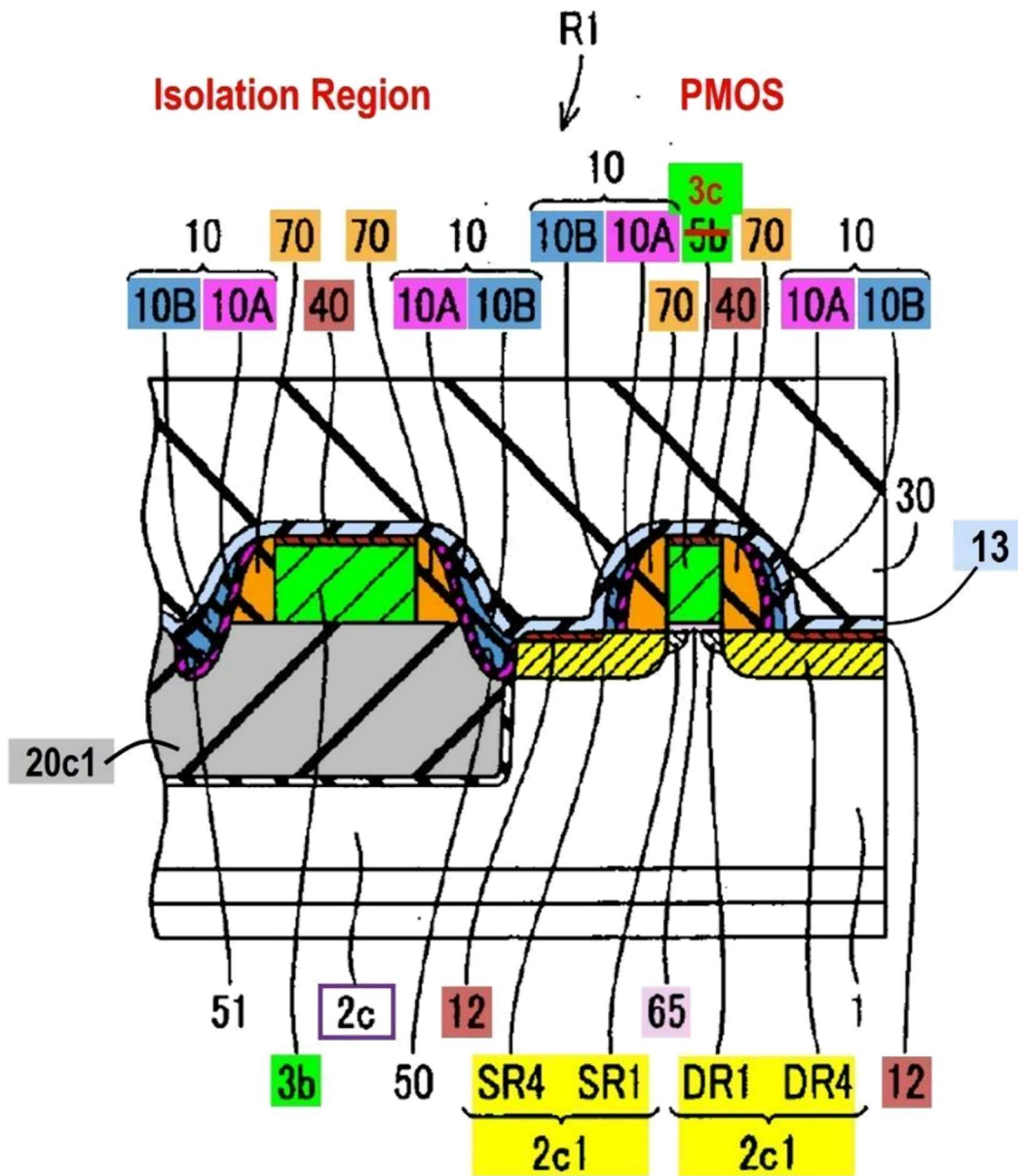


Figure M (annotated)

(9) [1H]

Saito’s insulating film 10A (silicon oxide) forms in recess 50 of the isolation and remains on the edges of sidewalls 70 (*see* FIG. 21). (Saito ¶[0074], ¶[0076], ¶[0078], ¶[0082], ¶[0104], ¶[0107], ¶[0113], FIGS. 6-12, 18-21; Ex-1003 ¶454.)

²⁰ Figure M shows the SiGe remains higher than the substrate. (*Infra* §V.C.1.c.)



Saito, FIG. 21 (excerpted)

Because silicon oxide film 10A remains in recess 50 and on sidewalls 70, a POSITA would have recognized that silicon oxide film 10A in the proposed combination would form in the space between SiGe facets and sidewalls 70 and remain there, as in recesses 50 and in the prior art (*see* Figure M). (*Supra* §II.C; Ex-1035 ¶¶[0052]-[0053], FIGS. 1U-1W; Ex-1030, 2:15-24, 9:10-44, FIGS. 2, 7-9;

Fukutome, FIG. 5G; Ex-1003 ¶¶455-457.) A POSITA would have recognized, and found obvious, that silicon oxide film 10A acts as a stress-relief film to buffer tensile strain from SiN layer 13 in PMOS active regions 2b/2c. (*Supra* §II.C, §V.C.1.a; Ex-1003 ¶¶458-459.)

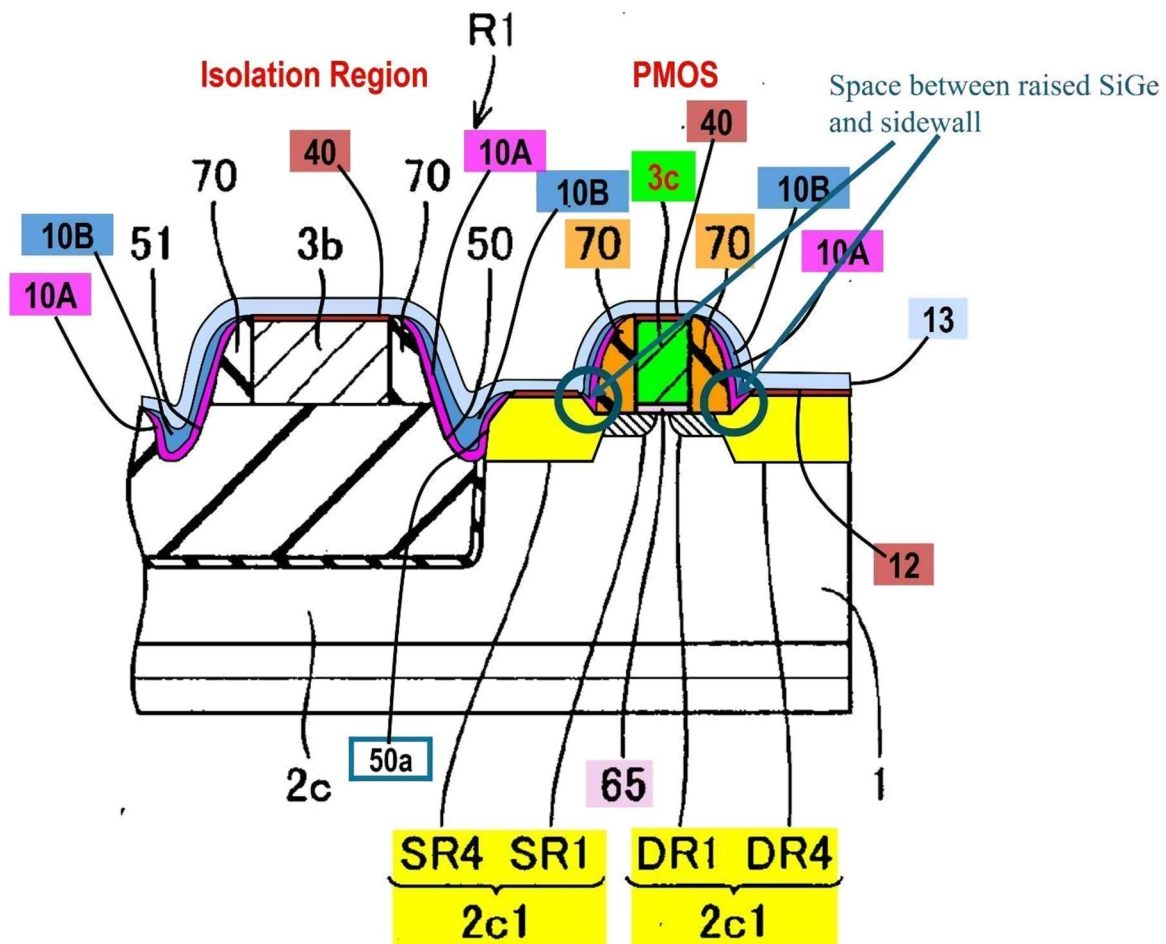


Figure M

(10) [11]

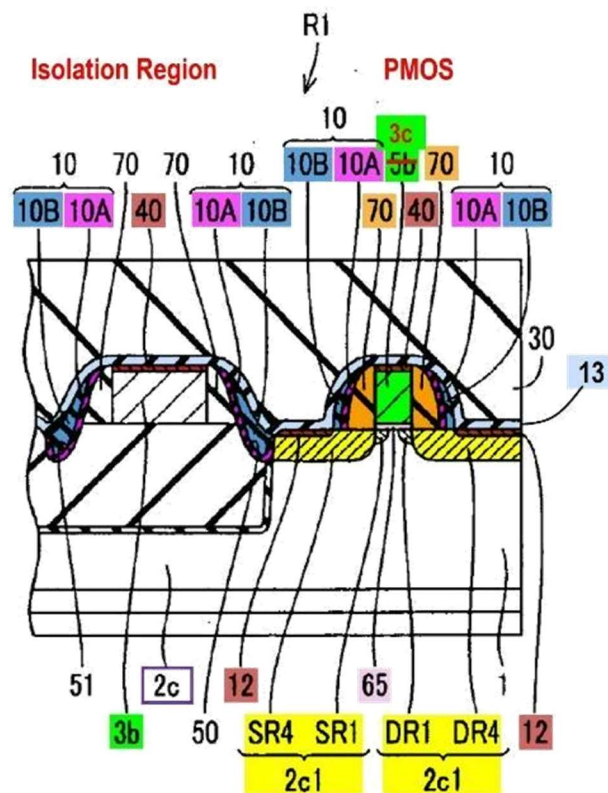
Saito's stress-relief film 10A (magenta) forms on side surfaces of wirings 3c (green) in PMOS transistor P2 with sidewalls 70 (orange) interposed therebetween (see Figure M). (*Supra* §V.C.1.b(9); Saito ¶[0066]; Ex-1003 ¶¶460-461.)

(11) [1J]

Saito's stress-relief film 10A (magenta) does not contact the side surface of polysilicon wiring 3c (green) since sidewalls 70 (orange) lie in between (*see* Figure M). (*Supra* §§V.C.1.b(9)-V.C.1.b(10); Saito, FIGS. 12, 21; Ex-1003 ¶¶462-463.)

c. Claim 3

Saito discloses a silicide film 40 (first silicide layer) formed on polysilicon wirings, including PMOS wirings 3b/3c, and a silicide film 12 (second silicide layer) formed on the source/drain regions of PMOS active region 2c. (Saito ¶[0117]; *see id.* ¶¶[0077], ¶¶[0124], FIGS. 3, 12, 20-21; Ex-1003 ¶¶466-467.)



Saito, FIG. 21 (excerpted)

When adding Fukutome's raised, faceted epitaxial SiGe source/drain regions to Saito's PMOS active regions 2b/2c (*see* Figure M), a POSITA would have understood silicide film 12 forms atop the SiGe layers but not the SiGe facets (where insulating layer 10A would block silicidation), and silicide film 40 forms on polysilicon wirings 3b/3c as in Saito. (Fukutome ¶¶[0103]-[0104], FIG. 5F; Saito ¶¶[0107]-[0112], FIG. 19; Ex-1003 ¶¶468-469.)

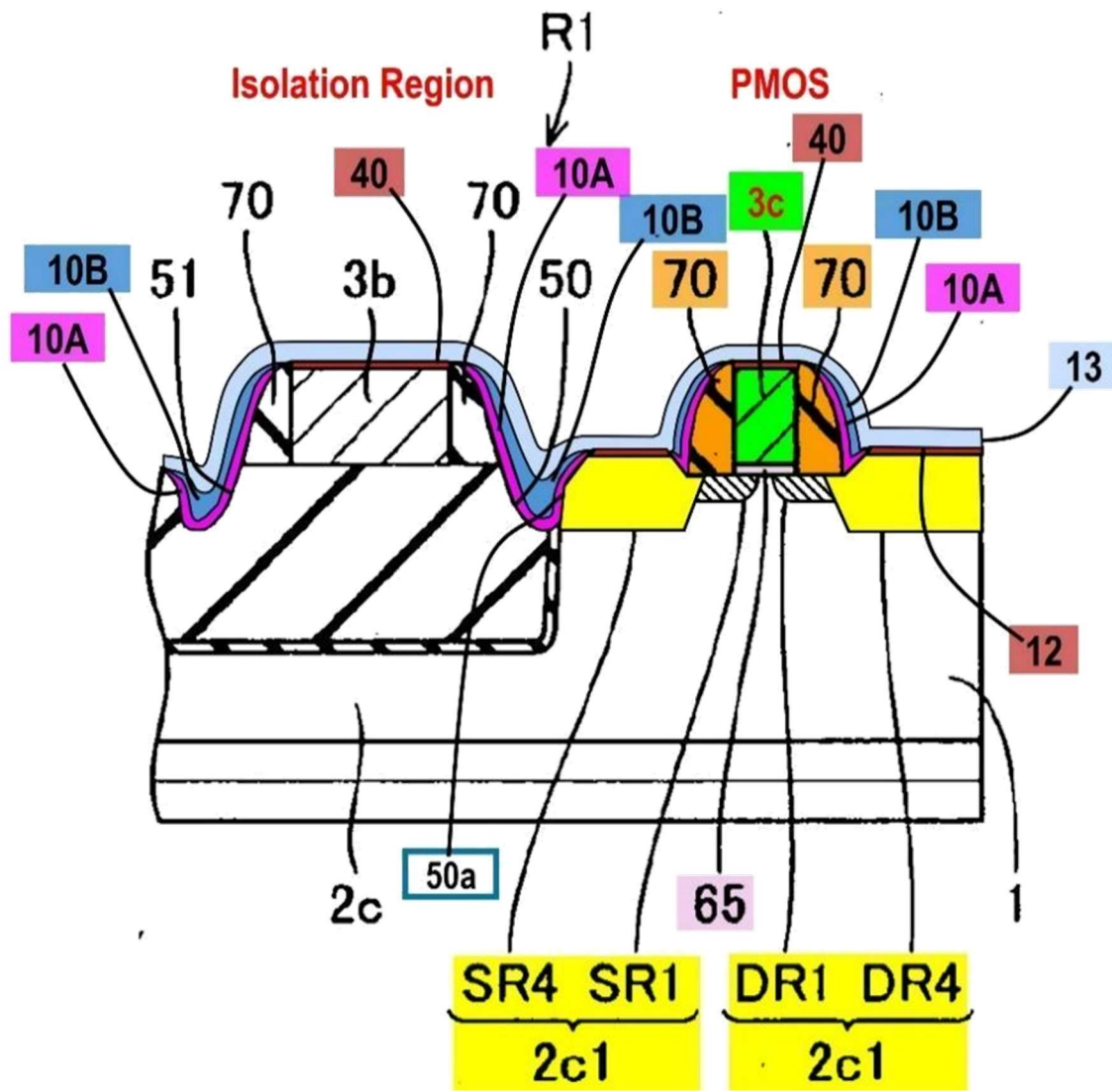


Figure M

With such silicidation, a POSITA would have found it obvious that the SiGe remains above the substrate to suppress junction leakage and improve reliability. (Fukutome ¶[0093], ¶¶[0099]-[0100], FIGS. 5F-5G; *supra* §V.C.1.a; Ex-1003 ¶¶470-471.)

d. Claim 4

In the combination (*see* Figure M), oxide film 10A (stress-relief film, magenta) forms on a facet (side surface) of each raised SiGe layer (silicon compound layer, yellow). (*Supra* §V.C.1.b(9); Ex-1003 ¶¶472-474.)

e. Claim 7:

(1) [7Pre]

(*Supra* §V.C.1.b; Ex-1003 ¶475.)

(2) [7A]

(*Supra* §V.C.1.b(2); Ex-1003 ¶476.)

(3) [7B]

(*Supra* §V.C.1.a, §V.C.1.b(6); Ex-1003 ¶477.)

(4) [7C]

(*Supra* §V.C.1.a, §V.C.1.b(7); Ex-1003 ¶478.)

f. Claim 8:

(1) [8Pre]

(*Supra* §V.C.1.b; Ex-1003 ¶479.)

(2) [8A]

(*Supra* §V.C.1.a, §V.C.1.b(6); Ex-1003 ¶480.)

(3) [8B]

(*Supra* §V.C.1.a, §V.C.1.b(7); Ex-1003 ¶481.)

(4) [8C]

(*Supra* §V.C.1.b(9); Ex-1003 ¶482).

g. Claim 10:

(1) [10Pre]: “The semiconductor device of claim 1”

(*Supra* §V.C.1.b; Ex-1003 ¶483.)

(2) [10A]: “an isolation region formed in the semiconductor substrate to surround the first active region”

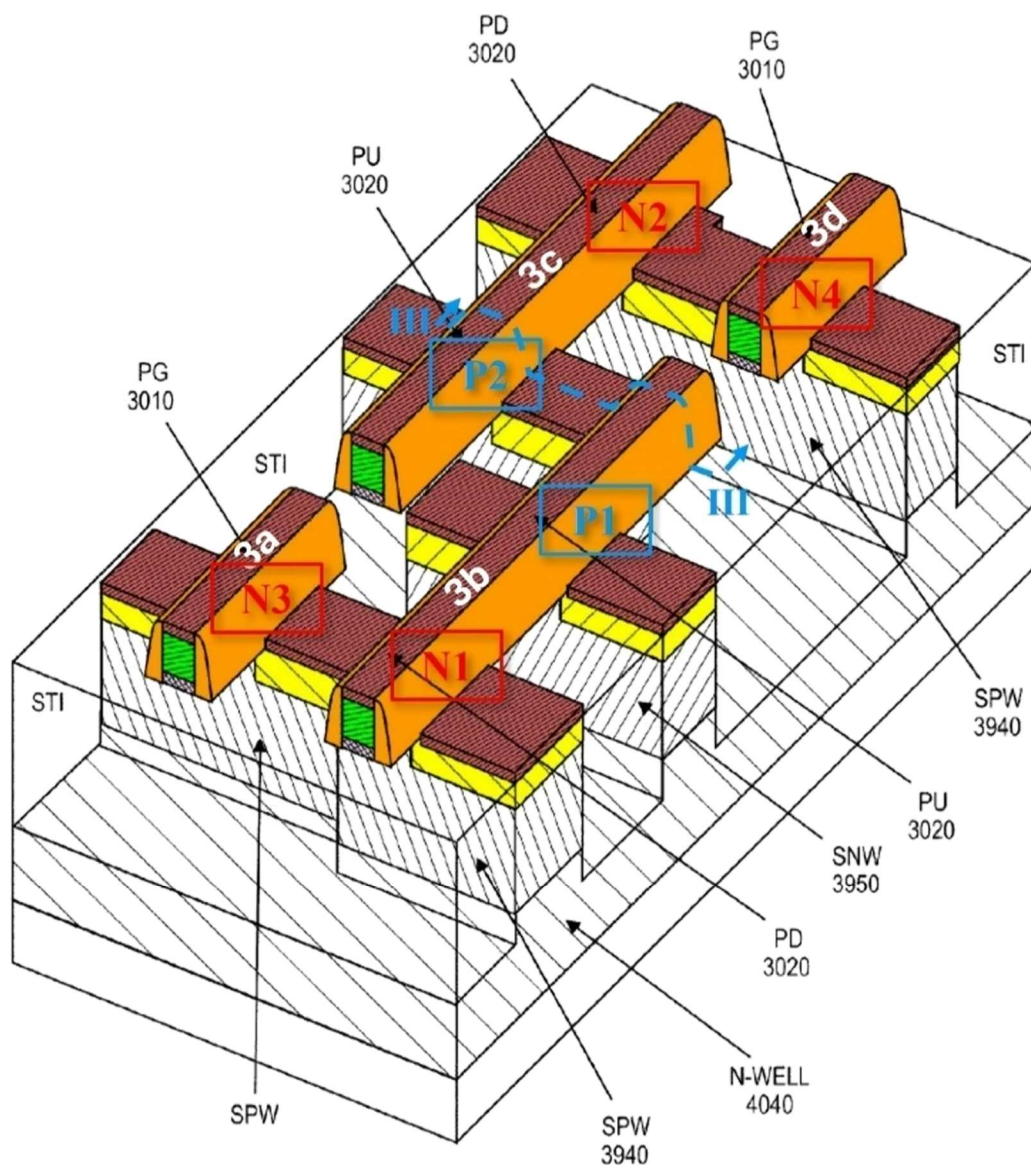
Saito discloses an isolation region 20C1—a trench 20B1 lined with silicon oxide films 20A2 and 20A1. (Saito ¶[0073], ¶¶[0088]-[0089], FIGS. 3, 11-14, 21.) As shown below, isolation region 20C1 defines the location of PMOS active regions 2b/2c in substrate 100 and surrounds active region 2c. (Saito ¶[0051], ¶¶[0072]-[0073], ¶¶[0086]-[0090], FIGS. 1, 3, 11-14, 21; Ex-1003 ¶¶484-485.) Figure N below is the same as Figure M but further annotates the isolation.



Saito, FIGS 11, 21 (excerpted)



Just as the “STI” (shallow trench isolation) regions surround the active regions below, a POSITA would have understood Saito’s isolation region 20C1 surrounds active region 2c to isolate neighboring transistors. (*Compare* Saito ¶[0049], ¶¶[0060]-[0070], FIGS. 1-2, *with* Ex-1050 ¶¶[0204]-[0205], FIGS. 39-40B; Ex-1003 ¶¶486-487.)

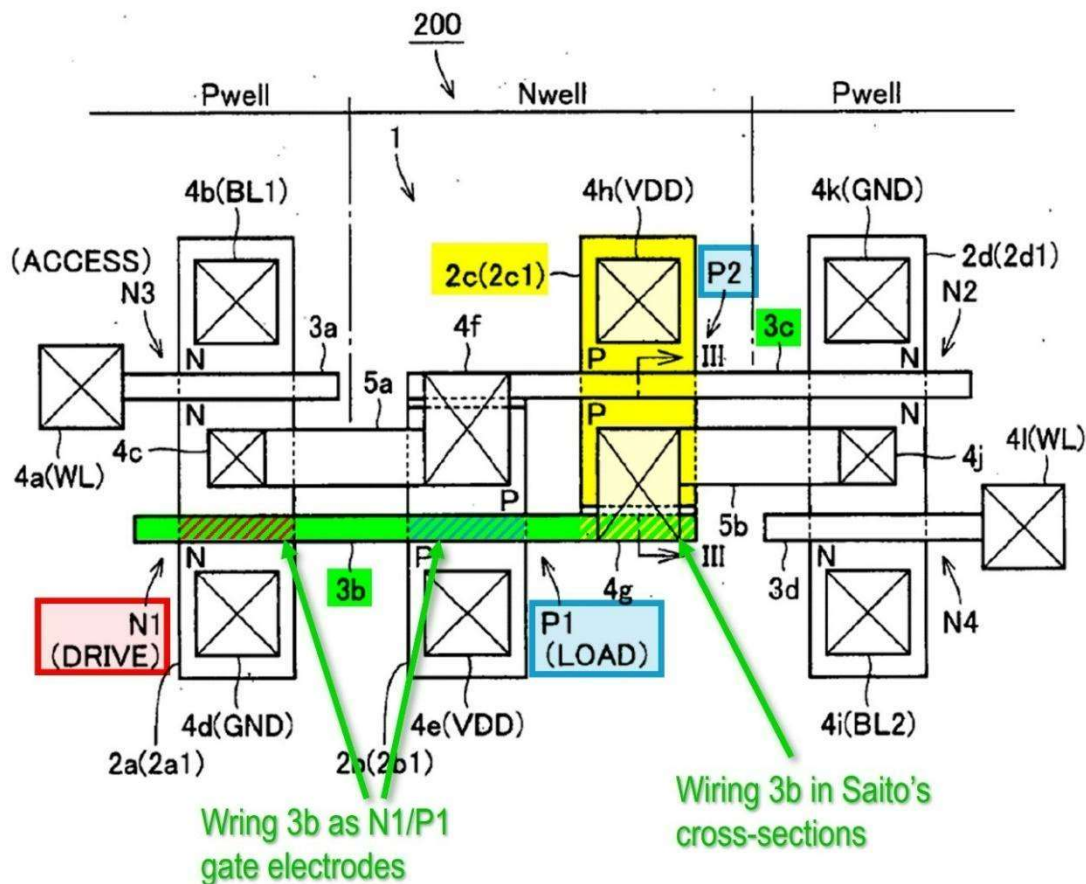


Ex-1050, FIG. 40B

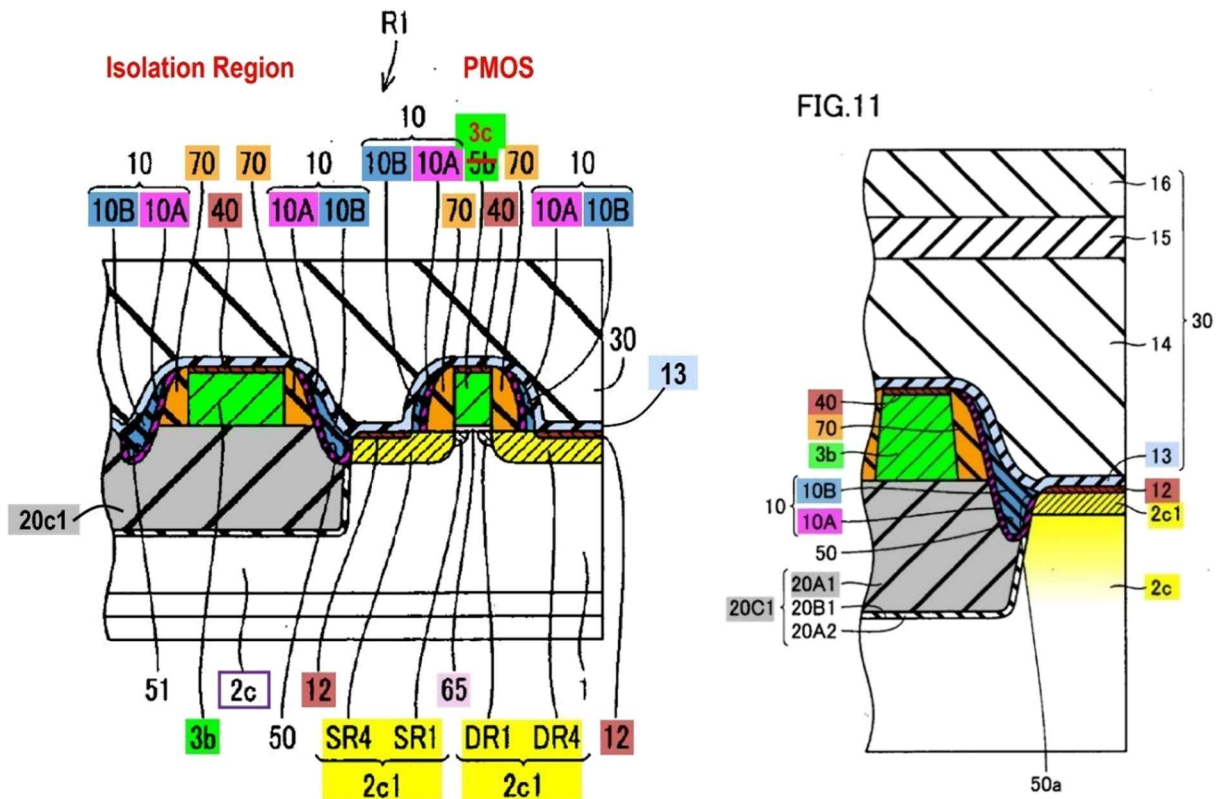
(3) [10B]: “a gate interconnect formed on the isolation region”

Saito discloses that “polysilicon wiring (wiring layer) 3b is formed” on isolation 20C1. (Saito ¶[0073]; *see id.* ¶[0093], FIGS. 1, 3, 11-12, 16, 21.) “[P]olysilicon wiring 3b” is a gate interconnect because it serves as, and interconnects, the gate electrodes of transistors N1 and P1 “formed in the intersection” of wiring 3b and active regions 2a/2b. (Saito ¶¶[0065]-[0066], FIGS. 1-2; Ex-1003 ¶¶488-489.)

FIG. 1



Saito, FIG. 1



Saito, FIGS 11, 21 (excerpted)

Wiring 3b performs the same interconnect function in the proposed combination. (*Supra* §V.C.1.a; Ex-1003 ¶490.)

(4) [10C]: “an interconnect sidewall spacer formed on a side surface of the gate interconnect”

Like the combination, Saito discloses sidewalls 70 formed on a side surface of wiring 3b (gate interconnect), as Saito’s FIGS. 11, 21 show (*see* Figure N below). (Saito ¶[0073], ¶[0096], FIGS. 3, 5, 11-12, 17, 21; Ex-1003 ¶¶491-492.)

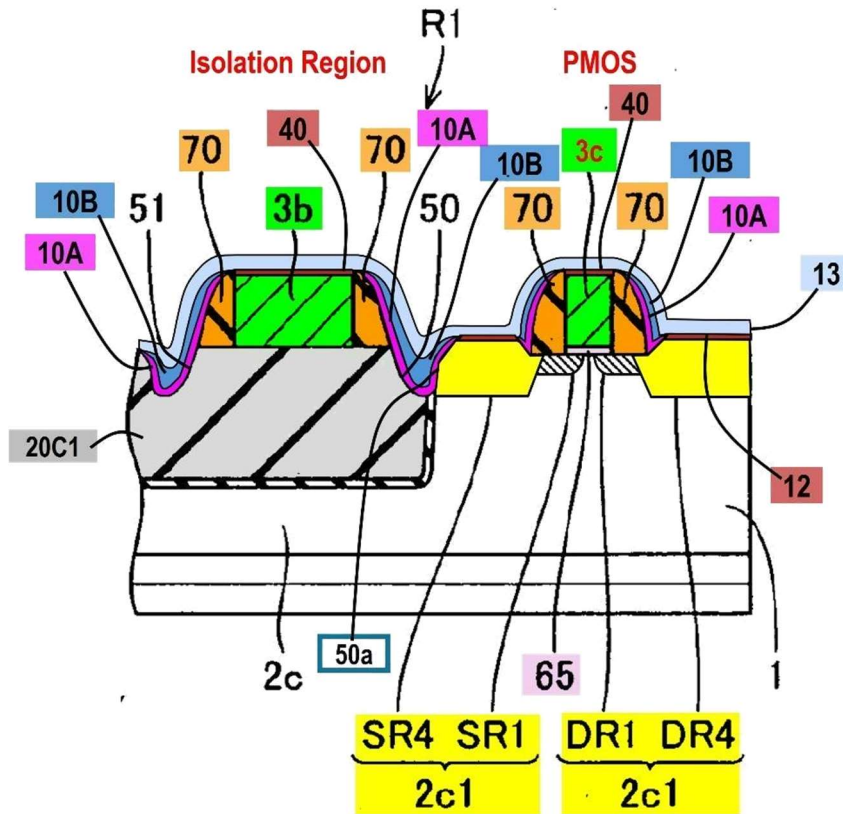


Figure N

- (5) [10D]: “a second stress-relief film formed on a side surface of a recessed portion provided in the isolation region on a lateral side of the interconnect sidewall spacer”**

Saito's insulating film 10A (magenta) forms on a side surface 50a of a recessed portion 50 in isolation region 20C1 on a lateral side of sidewall 70 (*see* Figure N). (Saito ¶¶[0074]-[0076], ¶[0082], ¶[0107], ¶¶[0113]-[0114], FIGS. 3, 6-7, 11-12, 21; Ex-1003 ¶493.) This is the same stress-relief film 10A as in [1H], except it is located on the sides of recess 50 (*see* Saito's FIGS. 11, 21). (*Supra* V.C.1.b(9); *compare* Saito ¶¶[0104]-[0107], ¶¶[0113]-[0114], FIGS. 6-7, 18-19, *with* Ex-1001, 12:59-13:12, FIGS. 5A-5B; Ex-1003 ¶¶494-497.)

Stress-relief film 10A likewise lies along the recess's edges in the combination because the same process steps are applied (*see* Figure N). (*Supra* §V.C.1.a, §V.C.1.b(9); Ex-1003 ¶497.)

(6) [10E]: “the stress insulating film formed on the isolation region to cover the gate interconnect, the interconnect sidewall spacer, and the second stress-relief film”

Saito's insulating film 13 (stress insulating film) is formed on isolation region 20C1 and covers gate interconnect wiring 3b, sidewall spacer 70, and stress-relief insulating film 10A, as Saito's FIGS. 11, 21 show (*see* Figure N). (Saito ¶[0080], ¶[0120], FIGS. 3, 9, 11-12, 21.) A POSITA would have found it obvious to form a tensile insulating film 13 as explained above. (*Supra* §V.C.1.a, §V.C.1.b(7); James, 2, 5, Fig. 6; Ex-1003 ¶¶498-500.)

VI. DISCRETIONARY DENIAL IS NOT WARRANTED

To simplify the *Fintiv* analysis, and following the precedential *Sotera* decision, Petitioner stipulates that, if IPR is instituted, Petitioner will not pursue in the related district court proceeding any ground that Petitioner raised or reasonably could have raised against the challenged claims during the instituted IPR. Petitioner also challenges nonasserted claims 2, 6, 8-10, and 12-15. Factor 4 thus heavily against denial. (IPR2020-01019, Paper 12, 19 (Dec. 1, 2020).)

Factor 3 weighs against denial because no substantive orders have issued, and few resources have been expended. (*See MED-EL Elektromedizinische Geräte Ges.m.b.H. v. Sonova AG*, IPR2020-00176, Paper 13, 12-15 (June 3, 2020) (instituting on similar facts).) *Markman* briefing does not begin until November 2025, and fact discovery just began. Petitioner diligently filed this petition after receiving infringement contentions, before serving invalidity contentions. (*See Ex-1051; Huawei Techs. Co. v. WSOU Invs., LLC*, IPR2021-00225, Paper 11, 10-11 (June 14, 2021) (expeditious filing outweighs minimal investment).)

Factor 6 favors institution because the merits are compelling.

Factors 1, 2, and 5 are at least neutral. Neither party has requested a stay. Although trial is scheduled for June 2026, that date often changes. The Board has instituted IPR on similar facts. (*See Ericsson Inc. v. XR Commc'ns LLC*, IPR2024-00613, Paper 9, 33-34 (Oct. 9, 2024); *NetNut Ltd. v. Bright Data Ltd.*, IPR2021-01492, Paper 12, 9-16 (Mar. 21, 2022).)

VII. MANDATORY NOTICES

A. Real Party-in-Interest

Taiwan Semiconductor Manufacturing Company Limited is the real party-in-interest.

B. Related Matters

The '425 Patent has been asserted against Petitioner in *Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Manufacturing Co.*, No. 2:24-cv-00623-JRG (E.D. Tex.). The '425 Patent also has been asserted against United Microelectronics Corporation (UMC), an unrelated party, in *Advanced Integrated Circuit Process LLC v. United Microelectronics Corp.*, No. 2:24-cv-00730-JRG (E.D. Tex.).

C. Lead and Back-Up Counsel

Lead Counsel	Back-Up Counsel
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D. Service Information

Petitioner consents to service by e-mail at the following addresses:

- jp.long@finnegan.com; and
- kevin.rodkey@finnegan.com.

VIII. PAYMENT OF FEES

The Office may charge additional fees to Deposit Account No. 06-0916.

IX. GROUNDS FOR STANDING

Petitioner certifies the '425 Patent is available for *inter partes* review and Petitioner is not barred or estopped from requesting review on the grounds presented.

X. CERTIFICATION UNDER 37 C.F.R. §42.24(d)

As calculated by the “Word Count” feature of Microsoft Word for Microsoft Office 365, this Petition contains 13,564 words, excluding this Certification and the following: Table of Contents, Table of Authorities, List of Exhibits, List of Challenged Claims, Mandatory Notices, and Certificate of Service.

XI. CONCLUSION

Trial should be instituted and the challenged claims cancelled.

Dated: March 26, 2025

Respectfully submitted,

/ J. Preston Long, Ph.D. /

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Lead Counsel for Petitioner

CERTIFICATE OF SERVICE

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105(a), **Petition for *Inter Partes* Review, Petitioner's Power of Attorney, and the associated Exhibits 1001-1051** were served via FedEx Priority Overnight delivery on March 26, 2025, on the correspondence address of record below indicated in the U.S. Patent Office's Patent Center for U.S. Patent No. 8,907,425.

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Courtesy copies have been concurrently served by the same means on Patent Owner's litigation counsel at:

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Houston, TX 77002

Dated: March 26, 2025

By: / William Esper /

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