Exhibit 425-08: Cheng817

U.S. Patent Application Publication No. 2005/0112817 ("Cheng817") was filed on August 11, 2004, published on May 26, 2005, and claims priority to U.S. Patent Application No. 10/722,218, which was filed on November 25, 2003. Accordingly, Cheng817 constitutes prior art to U.S. Patent No. 8,907,425 (the "'425 patent") under at least 35 U.S.C. §§ 102(a), (b), and (e).

Cheng817, including any material incorporated by reference into Cheng817, anticipates claims 1, 3-5, 7, and 11 (the "asserted claims") of the '425 patent under 35 U.S.C. §§ 102(a), (b), and (e).

To the extent any limitation is found not to be expressly or inherently disclosed in Cheng817, such a limitation would have been obvious either based on Cheng817 alone, given the state of the art, or in combination with one or more of the references cited in Exhibits 425-01 through 425-07 and 425-09 through 425-21, because the '425 patent is merely a collection of prior art elements that fails to meet the statutory requirement of non-obviousness under 35 U.S.C. § 103, and the factors delineated in *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), weigh against a finding of non-obviousness.

Any disclosures identified for each limitation of the '425 patent in the aforementioned Exhibits may be combined with the disclosures of Cheng817 identified below for the same limitation to render that limitation obvious. A POSITA would have found such a combination/modification obvious for the reasons discussed herein and in Defendant's cover pleading.[1]

The citations to portions of any reference in this chart are exemplary only. Citations to the written description should be interpreted to include the figures associated with or relevant to the cited passages. Similarly, citations to a figure should be understood to encompass any description, text, or discussion of that figure. Defendant reserves the right to use the entirety of any reference cited in this chart to show that the asserted claims are anticipated and/or are obvious. Citations presented for one claim limitation are expressly incorporated by reference into all other limitations for that claim as well as all limitations of all claims on which that claim depends.

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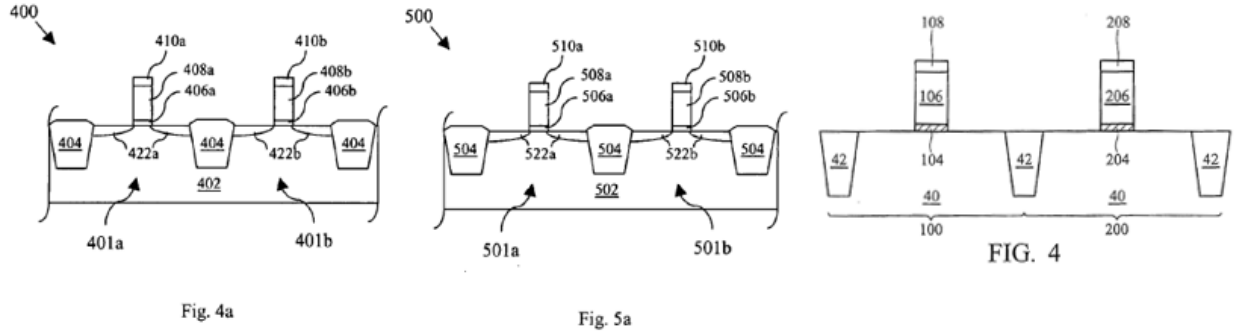
[1] Plaintiff appears in many instances to be pursuing overly broad constructions of limitations of the asserted claims in an effort to piece together an infringement claim where none exists. This claim chart accounts for overly broad construction of the claim limitations. Any assertion that a particular limitation is disclosed by a prior art reference or references may be based on Plaintiff's apparent constructions and is not intended to be, and is not, an admission that such constructions are supportable or proper. Defendant is investigating this prior art and has not yet completed discovery from third parties, who may have relevant information concerning the prior art. Therefore, Defendant reserves the right to supplement this chart after additional discovery is received. To the extent that any of the prior art discloses the same or similar functionality or feature(s) of any of the accused products, Defendant reserves the right to argue that said feature or functionality does not practice any limitation of any of the asserted claims, and to argue, in the alternative, that if said feature or functionality is found to practice any limitation of any of the asserted claims, then the prior art reference teaches the limitation and that the claim is not patentable.

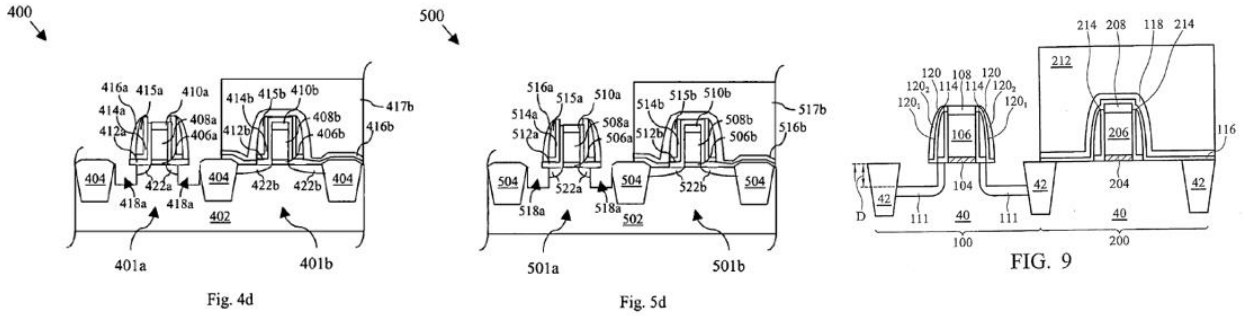
Cheng817's textual descriptions are clear and a POSITA would have understood some figures, including Figs. 4j and 5i, do not fully reflect the textual descriptions. U.S. Patent Application Publication No. 2007/0034906 ("Wang906")" describes similar MOS devices formed using similar processes. *Compare* Cheng817 ¶¶ [0056]-[0084], Figs. 4a-4j, 5a-5i, *with* Wang906 ¶¶ [0023]-[0032], FIGS. 4-9. Considering Cheng817's descriptions and figures in conjunction with Wang906's helps demonstrate how a POSITA would have understood Cheng817's disclosures.

Cheng817's Figs. 4a and 5a, like Wang906's FIG. 4, shows forming the gate dielectric and gate electrode layers. Cheng817 ¶ [0056], ¶ [0073], Figs. 4a, 5a; Wang906 ¶ [0023], FIG. 4.



Cheng817, Figs. 4a, 5a **Wang906, FIG. 4**

Cheng817's Figs. 4b-4d and 5b-5d, like Wang906's FIGS. 5-8, show forming gate electrode sidewalls, then etching recesses for epitaxial SiGe growth. Cheng817 ¶¶ [0061]-[0064], ¶ [0076]-[0079], Figs. 4b-4c, 5b-5c; Wang906 ¶¶ [0025]-[0028], FIGS. 5-8. In Cheng817's PMOS 401a of Fig. 4d and 501a of Fig. 5d, sidewall dielectric layers 412a/512a sit beneath dummy spacers 416a/516a like Wang906's sidewall spacer inner portion 120_1 sits beneath sidewall spacer outer portion 120_2. *See* Cheng817 ¶ [0064], ¶ [0079], Figs. 4d, 5d; Wang906 ¶ [0029], FIG. 9.



Cheng817, Figs. 4d, 5d **Wang906, FIG. 9 (modified to remove SiGe)**

Cheng817's Figs. 4e and 5e, like Wang906's FIG. 9, shows growing epitaxial SiGe in the trenches and extending above the substrate surface. Cheng817 ¶ [0022], ¶ [0065], ¶ [0080], Figs. 4e, 5e; Wang906 ¶¶ [0030]-[0032], FIG. 9.

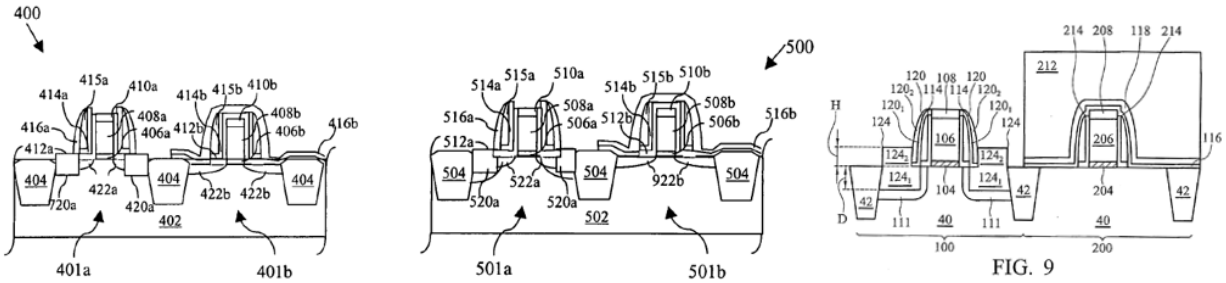


Fig. 4e Fig. 5e FIG. 9

Cheng817, Figs. 4e, 5e **Wang906, FIG. 9**

A POSITA would have understood from Cheng817's textual descriptions that Figs. 4e and 5e contains a rendering error where the epitaxial regions (720a [sic:420a], 420a, and 520a) appear to replace part of layer 412a in Fig. 4e, but also do not account for the full height described in Cheng817 in either Figs. 4e or 5e. The epitaxial regions in Cheng817's Figs. 4e and 5e would instead grow selectively on the crystalline trench surfaces, extending up and around the non-crystalline sidewalls as in corrected Figs. 4e and 5e below (left and middle). *See* Cheng817 ¶ [0065], ¶ [0080]; Wang906 ¶¶ [0030]-[0031], FIG. 9; U.S. Patent Application Publication No. 2004/0262683 ("Bohr683") ¶¶ [0024]-[0028], FIGS. 4-6.

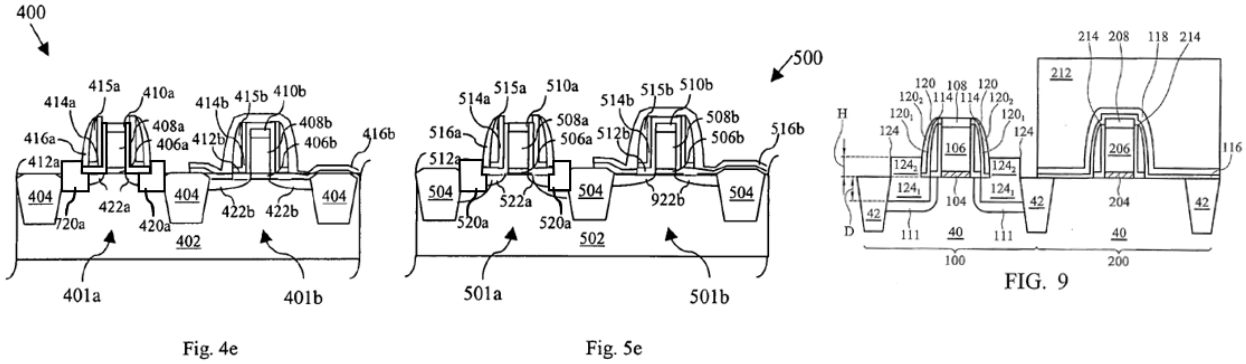


Fig. 4e Fig. 5e FIG. 9

Cheng, Figs. 4e, 5e (corrected) **Wang906, FIG. 9**

Consistent with corrected Figs. 4e and 5e of Cheng817, "[t]he height of raised source/drain regions may" extend as much as "about 100 nm" above the substrate, substantially higher than the top of the 0.5-10 nm thick gate dielectric 406a/506a. Cheng817 ¶ [0018], ¶ [0022]. Wang906 similarly explains that "raised [SiGe] portions 124_2 preferably have a height H … between about 100 Å and about 700 Å [10-70nm]." Wang906 ¶ [0031].

A POSITA would have recognized this correction carries through in Cheng817's Figs. 4f-4j and 5f-5i. Cheng817 ¶¶ [0066]-[0070], ¶¶ [0081]-[0084]. Figures A and B below modify Cheng817's Figs. 4j and 5i to show how this correction affects Cheng817's final devices. A POSITA would

have recognized, or at least found obvious, from Cheng817's disclosures alone or in view of or in combination with Wang906's and/or the disclosures of one or more of the references cited in Exhibits 425-01 through 425-07 and 425-09 through 425-21 that Cheng817 describes a PMOS transistor consistent with Figures A and B, which more accurately illustrate the process Cheng817's text describes. Cheng817 ¶¶ [0056]-[0084].

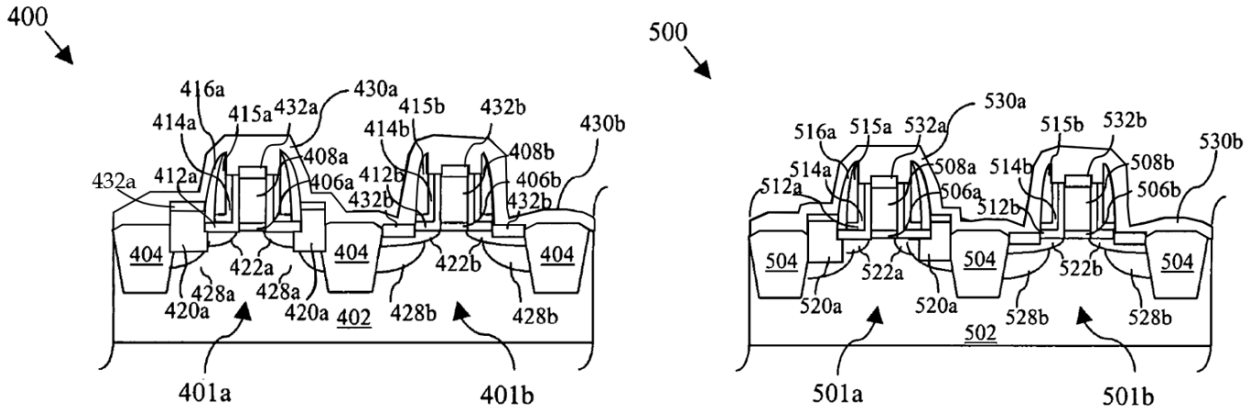


Figure A **Figure B**

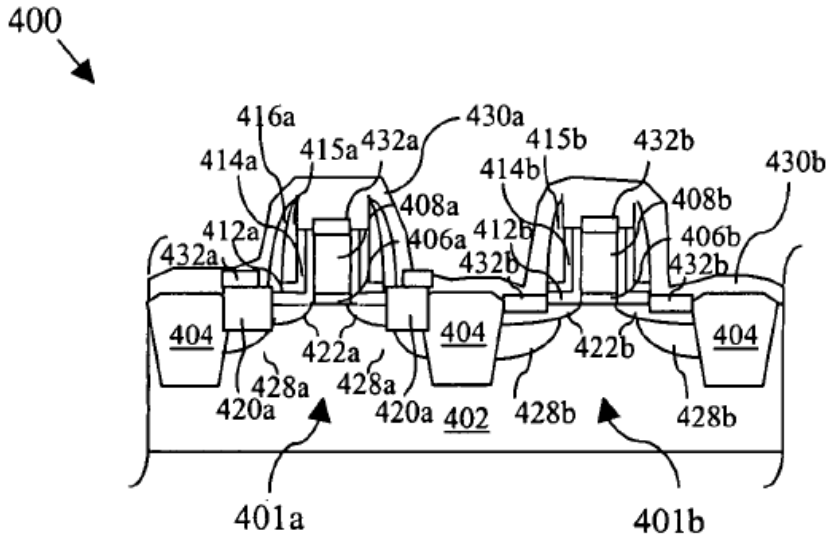
(Cheng817, Figs. 4j, 5i (corrected))

A POSITA would have found this structure obvious because it applies a known teaching, motivation, or suggestion in the prior art (Cheng817's express disclosures regarding Figs. 4a-4j and 5a-5i, alone or in view of or in combination with Wang906's or comparable disclosures of one or more of the references cited in Exhibits 425-01 through 425-07 and 425-09 through 425-21) to arrive at the claimed invention (reflected in Figures A and B).

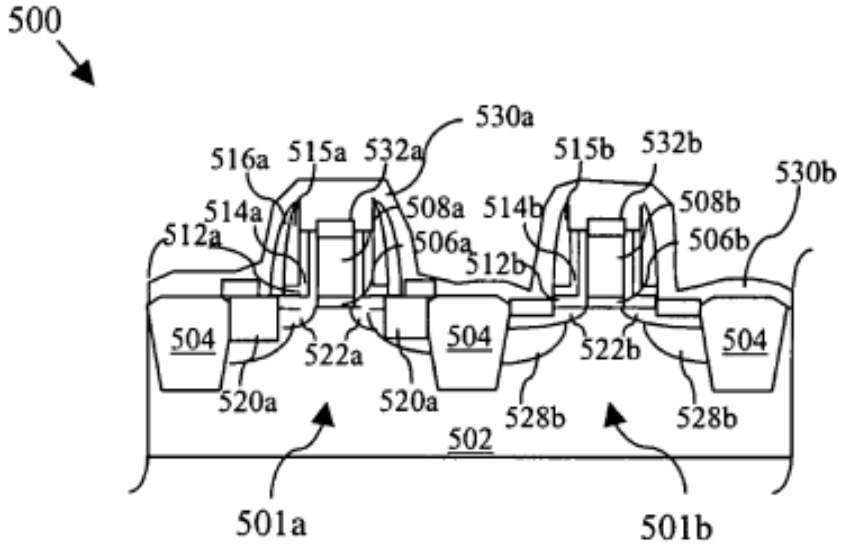
Exemplary Disclosures

1[pre] A semiconductor device, comprising:

Defendant does not concede that the preamble is limiting. To the extent it is limiting, Cheng817 discloses the preamble. For example, Cheng817 discloses semiconductor devices and the fabrication thereof. *See, e.g.*, the following:



Cheng817 Fig. 4j (showing a semiconductor device structure with NMOS and PMOS regions).



Cheng817 Fig. 5i (showing a semiconductor device structure with NMOS and PMOS regions).

Exemplary Disclosures

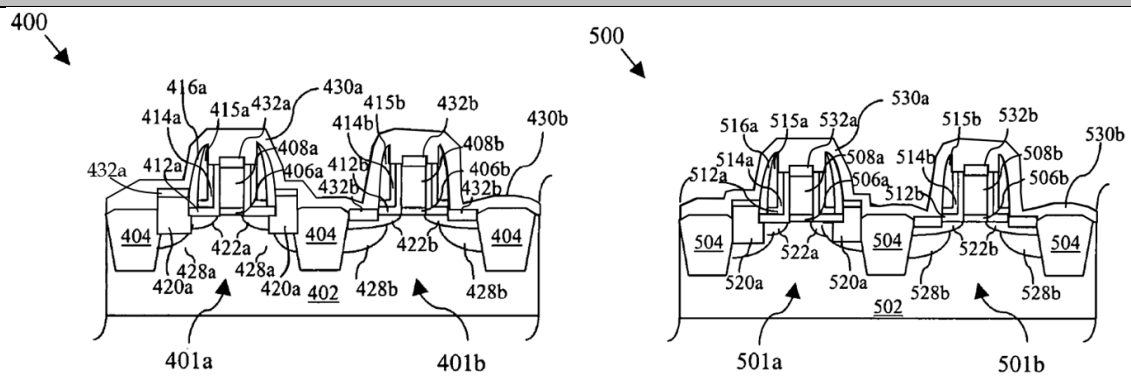


Figure A **Figure B**

(Cheng817, Figs. 4j, 5i (corrected))

"A method comprises forming a first semiconductor device in a substrate, where the first semiconductor device comprises a gate structure, a spacer disposed on sidewalls of the gate structure, the spacer having a first thickness, and raised source and drain regions disposed on either side of the gate structure. The method further comprises forming a second semiconductor device in the substrate and electrically isolated from the first semiconductor device, where the second semiconductor device comprises a gate structure, a spacer disposed on sidewalls of the gate structure, the spacer having a second thickness less than the first thickness of the spacer of the first semiconductor device, and recessed source and drain regions disposed on either side of the gate structure."

Cheng817 Abstract.

"The present disclosure relates generally to semiconductor devices and, more specifically, to a semiconductor device having a high drive current, a method of manufacture thereof, and an integrated circuit device incorporating the same."

Cheng817 ¶ [0013].

"Thus, the present disclosure introduces a semiconductor device including, in one embodiment, an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface; and (2) first source/drain regions extending from the surface. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface."

Cheng817 ¶ [0033].

Exemplary Disclosures
"In another embodiment, semiconductor device constructed according to aspects of the present disclosure comprises an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface. A second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different." Cheng817 ¶ [0034]. "Another embodiment of a semiconductor device constructed according to aspects of the present disclosure includes an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; (2) a first gate interposing the first source/drain regions; and (3) first spacers on opposing sides of the first gate and each extending from the first gate to a first width. A second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; (2) a second gate interposing the second source/drain regions; and (3) second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different." Cheng817 ¶ [0035]. "In another embodiment, a semiconductor device constructed according to aspects of the present disclosure includes an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe; (2) second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and (3) second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe." Cheng817 ¶ [0036].

Exemplary Disclosures
"The present disclosure also introduces a method of manufacturing semiconductor device. In one embodiment, the method includes forming an isolation region located in a substrate, forming an NMOS device located partially over a surface of the substrate, and forming a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface; and (2) first source/drain regions extending from the surface. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface." Cheng817 ¶ [0037]. "Referring now to FIGS. 4a-4j for sectional views of another embodiment of a method for making semiconductor devices 401a and 401b with high drive current. The semiconductor device 401a may be a P-type MOS device and the semiconductor device 401b may be an N-type MOS device. In FIG. 4a, gate dielectric 406a and 406b are formed over a substrate 402 for devices 401a and 401b, respectively, and electrically isolated from one another by isolation structures 404. The isolation structures 404 may be shallow trench isolation (STI) structures. Gate electrodes 408a and 408b are formed over the gate dielectric layer, and hard masks 410a and 410b are formed over the gate electrodes 408a and 408b, respectively." Cheng817 ¶ [0056]. "The substrate 402 may include silicon, silicon-on-insulation (SOI), germanium, germanium-on-insulation (GOI), gallium arsenide (GaAs), strained silicon, silicon germanium, silicon carbide, diamond, and/or other materials. In one embodiment, the substrate 402 may be substantially similar to the substrate 104 and 205 described above. In another embodiment, the substrate 402 may include an air gap to provide insulation for the microelectronic device 400. For example, a 'silicon-on-nothing' (SON) structure may include the semiconductor device(s) 401a and 401b each having a thin insulation layer formed by air and/or other insulators. The gate dielectric 406a and 406b and the gate electrode 408a and 408b may be substantially similar in composition to the gate dielectric layer 120 and 160 and the gate electrode 124 and 164 shown in FIG. 1 and described above." Cheng817 ¶ [0057]. "Alternatively, the gate dielectric 406a and 406b and/or gate electrode 408a and 408b may include multiple layers such as an oxide layer, a high-k dielectric later, a polysilicon layer, strained silicon, silicon germanium, silicon carbide, and/or other material layers. Other materials for the gate dielectric 406a and 406b and the gate electrode 408a and 408b may include titanium (Ti), tantalum (Ta), molybdenum (Mo), cobalt (Co), tungsten (W), titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (W_N), molybdenum silicide (MoSi), tungsten silicide (WSi), cobalt silicide (CoSi), nickel silicide ($NiSi_x$), metal silicides, germanium nanowire, silicon

Exemplary Disclosures
nanowire, and/or other materials. The gate dielectric 406a and 407b may comprise a SiO_2 layer and/or nitrided SiO_2. Alternatively, the gate dielectric 406a and 406b material may be replaced by the high-k dielectric. In one embodiment, the high-k layer may be formed from a variety of different materials, such as tantalum nitride, titanium nitride, tantoxide (Ta_2O_5), hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2), hafnium silicon oxy-nitride (HfSiON), hafnium silicide ($HfSi_x$), hafnium silicon nitride ($HfSi_xN_y$), hafnium aluminum dioxide ($HfAlO_2$), nickel silicide ($NiSi_x$), and/or other suitable materials using ALD, CVD, PECVD, evaporation, and/or other methods. Generally, the high-k layer may have a thickness between approximately 2 and 500 Angstroms. With some materials, such as HfSiON, the high-k layer of gate electrode 408a and 408b may be blanket deposited on the surface of substrate 402, while other materials may be selectively deposited. Alternatively, it may be desirable to blanket deposit some materials, including HfSiON, in some fabrication processes, while selectively depositing the same materials in other processes." Cheng817 ¶ [0058]. "The hard masks 410a and 410b may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), titanium nitride (TiN), silicon carbide (SiC), carbide, low-k dielectric, air, and/or other materials. The hard mask 410a and 410b may be formed by lithography, plasma etch, rapid thermal oxidation (RTO), CVD, PECVD, ALD, PVD, and/or other processing techniques now known or to be developed." Cheng817 ¶ [0059]. "The lightly doped regions 422a and 422b may include P-type and N-type dopants for the devices 401a and 401b, respectively. The doped regions 422a and 422b may be formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The doped regions 422a and 422b may also include lightly doped regions (LDD) and/or heavily doped regions in one embodiment. The doped regions 422a and 422b may include impurities such as phosphorous, boron, antimony, arsenic, and/or other materials. For example, the formation of the doped regions 422a and 422b by ion implantation may include an ion implant energy ranging between about 1 KeV and about 100 KeV and the dose of ion implantation of may range between about 1×10^{13} cm^{-2} and about 5×10^{16} cm^{-2}." Cheng817 ¶ [0060]. "In FIG. 4b, sidewall dielectric layers 412 and 414, and spacer material 415 are disposed over the semiconductor device(s) 410a and 401b and are subsequently processed, such as by etching, to form sidewall dielectric structures 412a, 412b, 414a and 414b, and spacers 415a and 415b, as shown in FIG. 4c. Note the dielectric structures 714a and 714b are substantially L-shaped. A dummy spacer layer 416 is formed over the semiconductor devices 401a and 401b. Low temperature processing, such as using a temperature less than 600° C., to form the sidewall dielectric and spacer materials is preferred to reduce lightly doped drain diffusion." Cheng817 ¶ [0061].

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"The sidewall dielectric layers 412 and 414 may be a liner oxide layer and a nitride layer formed over the devices by deposition. In particular, the sidewall dielectric layers 412 and 414 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), polymer and/or other materials. The sidewall dielectric layers 412 and 414 may also include multiple layers and/or may include a single layer, in one embodiment. The sidewall dielectric layers 412 and 414 may be formed by RTO, CVD, PVD, PECVD, ALD, CMP, chemical etching, plasma etching, and/or other processing techniques. The spacer material 415 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), polymer and/or other materials. The spacer material 415 may also include multiple layers and/or may include a single layer, in one embodiment. The spacer material 415 may be formed by RTO, CVD, PVD, PECVD, ALD, CMP, chemical etching, plasma etching, and/or other processing techniques. The sidewall dielectric structures 412a, 412b, 414a and 414b, and spacers 415a and 415b may be formed by chemical etching, plasma etching, CMP, focused ion beam (FIB), and/or other processing techniques." Cheng817 ¶ [0062]. "In FIG. 4d, the dummy spacer material 416 is processed to form the dummy spacers 416a and 416b. The dummy spacer material 416 may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), silicon oxy-carbide (SiOC), polymer, and/or other materials. The spacer material 416 may be formed by CVD, PECVD, ALD, spin-on coating, and/or other processing techniques, for example, and the dummy spacers 416a and 416b may be formed by chemical etch, plasma etch, CMP, focused ion beam (FIB), and/or other processing techniques. In FIG. 4d, a photoresist 417b is provided over the device 401b so that portions of the dummy spacer material 416a is removed from the device 401a, and recessed source and drain regions 418a are also formed in the substrate 402 on either side of the gate structure of the device 401a." Cheng817 ¶ [0063]. "The recessed source and drain regions 418a may be formed by a process such as chemical etch, focused ion beam (FIB), and/or plasma etch. In particular, the recessed regions 418a may be formed by a chemical etch of the exposed substrate interposed by the isolation regions 404 and the dummy spacers 416a. In one embodiment, a portion of the substrate 402 below the dummy spacers 416a may be removed, as shown in FIG. 4d." Cheng817 ¶ [0064]. "In FIG. 4e, the photoresist 417b is removed, and doped source and drain regions 420a are formed or built-up in the recessed regions 418a. The doped source and drain regions 420a may be formed by selective epitaxial growth (SEG), CVD, PECVD, PVD, PDL, ALD, spin-on formation, and/or other techniques now know or to be developed. The doped source and drain regions 420a may include materials such as amorphous silicon, polysilicon, strained silicon, germanium, silicon germanium, silicon carbide, and/or other materials. Low temperature processing, such as using a

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temperature less than 700° C., to form the doped regions 420a is preferred to reduce lightly doped drain diffusion." Cheng817 ¶ [0065]. "In FIG. 4f, a photoresist 421a is disposed over the semiconductor device 401a. Further, the dummy spacer 716b is removed from the device 401b. The spacer material 416b may be removed by chemical etch, plasma etch, CMP focused ion beam (FIB), and/or other processing techniques. Deeper and more heavily doped regions 428b are also formed in the substrate 402 in the semiconductor device 401b. The doped regions 428b may include N-type impurities, and may be formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The doped regions 428b may include heavy doped regions forming the source/drain regions of the semiconductor device 701b. The ion implantation may include an ion implant energy ranging between about 5 KeV and about 100 KeV and the dose of ion implantation of may range between about 1×10^{14} cm^{-2} and about 5×10^{18} cm^{-2}." Cheng817 ¶ [0066]. "In FIG. 4g, the photoresist 421a is removed from the device 401a. Further, the hard masks 410a and 410b are removed from the semiconductor devices 401a and 401b. The photoresist 421a may be removed by plasma etch and/or chemical etch. For example, the mask 421a may be removed by an oxygen (O_2) containing plasma environment. The hard masks 410a and 410b may be removed by chemical and/or plasma etch. For example, the hard masks 410a and 410b may be removed by hot phosphoric (H_2PO_4) acid, ammonium hydroxide ($NH_{40}H$), hydrochloric acid (HCl), hydrofluoric acid (HF), sulfuric acid (H_2SO_4), and/or other etchant chemicals. The hard masks 420a and 420b may also be removed by ion bombardment in an inert plasma comprising argon, hydrogen, xenon, and/or other gases." Cheng817 ¶ [0067]. "In FIG. 4h, a photoresist 421b is formed over the semiconductor device 401a. The mask 421b may include photoresist, silicon dioxide (SiO_2), silicon nitride (Si_xN_y), and/or other materials. The mask 421b may be formed by spin-on coating, CVD, and/or other processing techniques. Further, more heavily doped source and drain regions 428a are formed in the substrate 402 for the semiconductor device 401a. The doped regions 428a which may include P-type impurities, and may be formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The ion implantation may include an ion implant energy ranging between about 5 KeV and about 100 KeV and the dose of ion implantation of may range between about 1×10^{14} cm^{-2} and about 5×10^{18} cm^{-2} for example." Cheng817 ¶ [0068].

Exemplary Disclosures
"In FIG. 4i, the photoresist 421b is removed from the device 401b, and salicided contacts 432a and 432b are formed over the gate, source and drain of the devices 401a and 401b. The salicided contacts 432a and 432b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 732a and 732b may also include an anneal. The salicided contacts 732a and 732b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0069]. "Further in FIG. 4j, an etch stop layer 430a and 430b are formed over the semiconductor device(s) 401a and 401b. The etch stop layer 430a and 430b may include silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), and/or other materials. In one embodiment, the etch stop layer 430a and 430b may be substantially similar in composition to the etch stop layer 180 described above. Alternatively, the etch stop layer 430a and 430b may include a stress level that may range between about +0.001 and about +50 GPa for tensile film and between about −0.001 and about −50 GPa for compressive film. The etch stop layer 430a and 430b may be formed by CVD, ALD, PECVD, PDL, spin-on coating, and/or other techniques." Cheng817 ¶ [0070]. "Subsequent processing steps may be performed to the semiconductor devices 401a and 401b such as metallization, testing and packaging, etc." Cheng817 ¶ [0071]. "Referring now to FIGS. 5a-i for another embodiment of a method for manufacturing a microelectronic device 500 with high drive current. In FIG. 5a, gate structures including a gate dielectric 506a and 506b and gate electrodes 508a and 508b are formed for semiconductor devices 501a and 501b, respectively. Gate electrodes 508a and 508b may be pre-doped with appropriate P-type and N-type dopants, respectively. Hard masks 510a and 510b are also formed over each gate structure. Further, shallow doped drain and source regions 522a and 522b are formed on either sides of the gate structures of each device 501a and 501b. Isolation structures 504 are formed in the substrate 502 to electrically isolate the devices 501a and 501b." Cheng817 ¶ [0072]. "The substrate 502 may include silicon, silicon-on-insulation (SOI), germanium, germanium-on-insulation (GOI), gallium arsenide (GaAs), strained silicon, diamond, and/or other materials. In another embodiment, the substrate 502 may include an air gap to provide insulation for the microelectronic device 500. For example, a 'silicon-on-nothing' (SON) structure may include the semiconductor devices 501a and 501b each having a thin insulation layer formed by air and/or other insulator. The gate dielectric 506a and 506b and the gate electrode 508a and 508b, in one embodiment, may be substantially similar in composition to the gate dielectric layer 120 and 160 and the gate electrode 124 and 164 shown in FIG. 1. Alternatively, the gate dielectric 506a and

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506b and/or gate electrode 508a and 508b may include multiple layers such as an oxide layer, a high-k dielectric later, a polysilicon layer, strained silicon, silicon germanium, silicon carbide, and/or other material layers. Other materials for the gate dielectric 506a and 506b and the gate electrode 508a and 508b may include titanium (Ti), tantalum (Ta), molybdenum (Mo), cobalt (Co), tungsten (W), titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (W_N), molybdenum silicide (MoSi), tungsten silicide (WSi), cobalt silicide (CoSi), nickel silicide ($NiSi_x$), metal silicides, germanium nanowire, silicon nanowire, and/or other materials. The gate dielectric 506a and 506b may comprise a SiO_2 layer and/or nitrided SiO_2. In one embodiment, the high-k layer may be formed from a variety of different materials, such as tantalum nitride, titanium nitride, tantoxide (Ta_2O_5), hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2), hafnium silicon oxy-nitride (HfSiON), hafnium silicide ($HfSi_x$), hafnium silicon nitride ($HfSi_xN_y$), hafnium aluminum dioxide ($HfAlO_2$), nickel silicide ($NiSi_x$), and/or other suitable materials using ALD, CVD, PECVD, evaporation, and/or other methods. With some materials, such as HfSiON, the high-k layer of gate electrode 508a and 508b may be blanket deposited on the surface of substrate 502, while other materials may be selectively deposited. Alternatively, it may be desirable to blanket deposit some materials, including HfSiON, in some fabrication processes, while selectively depositing the same materials in other processes." Cheng817 ¶ [0073]. "The hard masks 510a and 510b may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), titanium nitride (TiN), silicon carbide (SiC), carbide, low-k dielectric, air, and/or other materials. The hard mask 510a and 510b may be formed by lithography, plasma etch, rapid thermal oxidation (RTO), CVD, PECVD, ALD, PVD, and/or processing techniques." Cheng817 ¶ [0074]. "The doped source and drain regions 522a and 522b may include N-type and/or P-type doped regions formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The doped regions 522a and 522b may be lightly doped drains (LDD) and may include impurities such as phosphorous, boron, antimony, arsenic, and/or other materials." Cheng817 ¶ [0075]. "In FIG. 5b, sidewall dielectric layers 512 and 514, and a spacer material 515 are formed over the semiconductor devices 510a and 501b, preferably using a low temperature process to reduce LDD diffusion. The sidewall dielectric layers 512 and 514 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), polymer and/or other materials. The spacer material 515 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), polymer and/or other materials. For example, dielectric layers 512 and 514 may comprise a liner oxide layer and a nitride layer, and the spacer material 515 may comprise an oxide material. The sidewall dielectric layers 512 and 514 and

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spacer layer 515 may be formed by RTO, CVD, PVD, PECVD, ALD, CMP, chemical etching, plasma etching, and/or other processing techniques." Cheng817 ¶ [0076] "In FIG. 5c, the sidewall dielectric layers 512 and 514, and a spacer material 515 are subsequently processed forming sidewall dielectric 512a, 512b, 514a and 514b, and spacers 515a and 515b. The sidewall dielectric 512a, 512b, 514a and 514b, and spacers 515a and 515b may be formed by chemical etching, plasma etching, CMP, focused ion beam (FIB), and/or other processing techniques." Cheng817 ¶ [0077]. "Further, a dummy spacer material 516 is formed over the semiconductor devices 501a and 501b, and subsequently processed forming the dummy spacers 516a and 516b. The dummy spacer material 516 may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), silicon oxy-carbide (SiOC), polymer, and/or other materials. The spacer material 516 may be formed by CVD, PECVD, ALD, spin-on coating, and/or other processing techniques, and may be formed by chemical etch, plasma etch, CMP, focused ion beam (FIB), and/or other processing techniques." Cheng817 ¶ [0078]. "In FIG. 5d, a photoresist 517b is formed over the semiconductor device 501b so that the device 501 a may be processed. An oxide etch process may be used to remove material layers above the hard mask 510a disposed over the gate structure. Another etch process may also be used to create recessed source and drain regions 518a in the substrate 502. The recessed source and drain regions 518a may be formed by a process such as chemical etch, focused ion beam (FIB), and/or plasma etch. In the embodiment shown in FIG. 5d, a portion of the substrate 502 extending partially below the spacer 516a is also removed." Cheng817 ¶ [0079]. "In FIG. 5e, the photoresist 517b is removed from the device 501b and source and drain regions 520a are built-up in the recessed regions 518a, preferably using a low temperature process to reduce LDD diffusion. The source and drain regions 520a may be formed by, for example, selective epitaxial growth (SEG), CVD, PECVD, PVD, PDL, ALD, spin-on formation, and/or other suitable techniques now know or later developed. The source and drain regions 520a may include materials such as amorphous silicon, polysilicon, strained silicon, germanium, silicon germanium, silicon carbide, and/or other materials. The source and drain regions 520a may also be doped 'in-situ' during the SEG process, for example. In this process, dopants such as boron, phosphorous, arsenic, germanium, carbon, and/or other semiconductor materials may be introduced during the SEG process. The dopants may be introduced in gaseous form, which may

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include diborane (B_2H_6), Arsine (AsH_3), phosphine (PH_3), germane (GeH_4), phosphoryl chloride ($POCL_3$), boron bromide (BBr_3), hydrocarbons, and/or other gases/chemicals." Cheng817 ¶ [0080]. "In FIG. 5f, a photoresist 521a is disposed over the semiconductor device 501a for processing of the semiconductor device 501b. The dummy spacer material 516b is removed from the device 501b, and deeper source and drain doped regions 528b are formed. The spacer material 516b may be removed by chemical etch, plasma etch, CMP focused ion beam (FIB), and/or other processing techniques, for example. The doped regions 528b may include N-type impurities, and may be formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The ion implantation process may use an ion implant energy ranging between about 5 KeV and about 100 KeV and the dose of ion implantation of may range between about 1×10^{14} cm^{-2} and about 5×10^{18} cm^{-2}, for example." Cheng817 ¶ [0081]. "In FIG. 5g, the photoresist 521a is removed from the device 501. Further, the hard masks 510a and 510b are removed from the gate structures of the semiconductor devices 501a and 501b. The hard masks 510a and 510b may be removed from the semiconductor devices by chemical and/or plasma etch. For example, the hard masks 510a and 510b may be removed by hot phosphoric (H_2PO_4) acid, ammonium hydroxide (NH_4OH), hydrochloric acid (HCl), hydrofluoric acid (HF), sulfuric acid (H_2SO_4), and/or other chemicals. The hard mask 510a and 510b may also be removed by ion bombardment in an inert plasma comprising argon, hydrogen, xenon, and/or other gases." Cheng817 ¶ [0082]. "Because the deeper doped source and drain regions were doped in-situ (FIG. 5g), a process of source and drain implantation such as that shown in FIG. 4h is not required. Therefore, salicided contacts 532a and 532b are formed for the gate, source and drains of the devices 501a and 501b, respectively, as shown in FIG. 5h. The salicided contacts 532a and 532b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 532a and 532b may also include an anneal. The salicided contacts 532a and 532b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0083].

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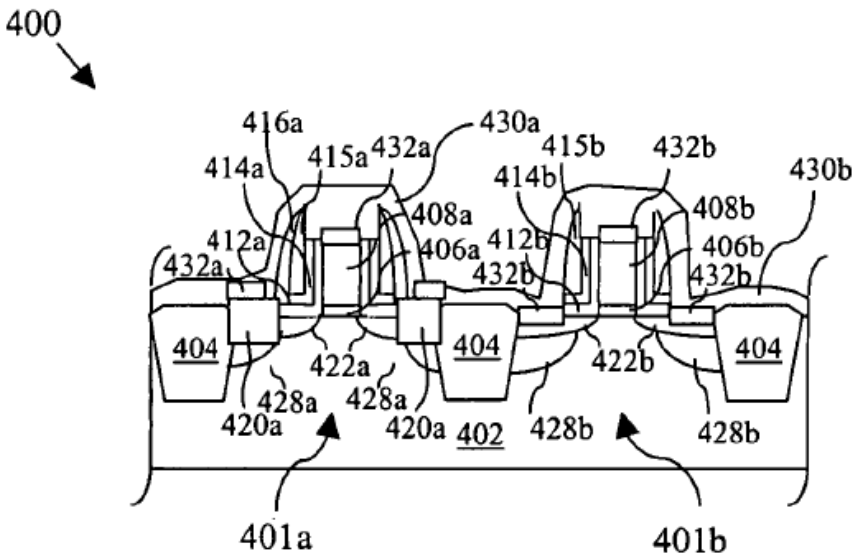
"In FIG. 5i, etch stop layer 530a and 530b are formed over the semiconductor devices 501a and 501b. The etch stop layer 530a and 530b may include silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), and/or other materials. Alternatively, the etch stop layer 530a and 530b may include a stress level that may range between about +0.001 and about +50 GPa for tensile film and between about −0.001 and about −50 GPa for compressive film. The etch stop layer 530a-b may be formed by CVD, ALD, PECVD, PDL, spin-on coating, and/or other techniques." Cheng817 ¶ [0084]. To the extent that Cheng817 is found not to disclose the preamble, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
1[a] a first MIS transistor, wherein: the first MIS transistor includes:
Cheng817 discloses this feature. For example, Cheng817 discloses a PMOS transistor 401a.[2] *See, e.g.*, the following:    Cheng817 Fig. 4j (showing PMOS transistor 401a on left-hand side).

[2] Similarly numbered items in Figs. 5a-5i (e.g., 5xx) correspond to the same structures (e.g.4xx) in Figs. 4a-4j (e.g., PMOS 401a in Figs. 4a-4j corresponds to PMOS 501a in Figs. 5a-5i, etc.). Thus, references to a structure 4xx in this chart should be understood to also encompass reference to corresponding feature 5xx.

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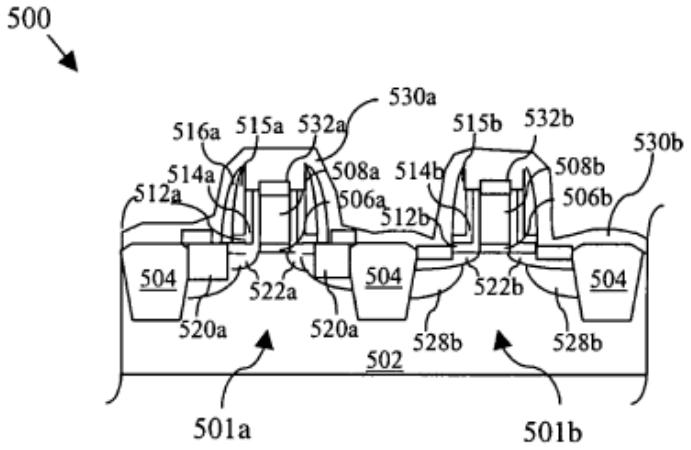
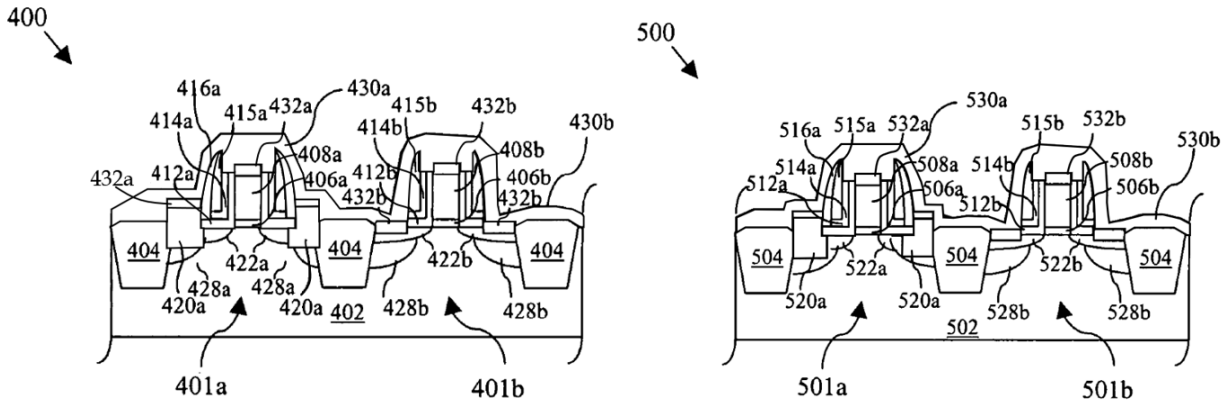
 Cheng817 Fig. 5i (showing PMOS transistor 501a on left-hand side).  **Figure A** **Figure B** **(Cheng817, Figs. 4j, 5i (corrected))** "Thus, the present disclosure introduces a semiconductor device including, in one embodiment, an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface; and (2) first source/drain regions extending from the surface. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface." Cheng817 ¶ [0033].

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"In another embodiment, semiconductor device constructed according to aspects of the present disclosure comprises an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface. A second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different." Cheng817 ¶ [0034]. "Another embodiment of a semiconductor device constructed according to aspects of the present disclosure includes an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; (2) a first gate interposing the first source/drain regions; and (3) first spacers on opposing sides of the first gate and each extending from the first gate to a first width. A second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; (2) a second gate interposing the second source/drain regions; and (3) second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different." Cheng817 ¶ [0035]. "In another embodiment, a semiconductor device constructed according to aspects of the present disclosure includes an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe; (2) second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and (3) second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe." Cheng817 ¶ [0036].

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"The present disclosure also introduces a method of manufacturing semiconductor device. In one embodiment, the method includes forming an isolation region located in a substrate, forming an NMOS device located partially over a surface of the substrate, and forming a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface; and (2) first source/drain regions extending from the surface. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface." Cheng817 ¶ [0037]. "Referring now to FIGS. 4a-4j for sectional views of another embodiment of a method for making semiconductor devices 401a and 401b with high drive current. The semiconductor device 401a may be a P-type MOS device and the semiconductor device 401b may be an N-type MOS device. In FIG. 4a, gate dielectric 406a and 406b are formed over a substrate 402 for devices 401a and 401b, respectively, and electrically isolated from one another by isolation structures 404. The isolation structures 404 may be shallow trench isolation (STI) structures. Gate electrodes 408a and 408b are formed over the gate dielectric layer, and hard masks 410a and 410b are formed over the gate electrodes 408a and 408b, respectively." Cheng817 ¶ [0056]. "The substrate 402 may include silicon, silicon-on-insulation (SOI), germanium, germanium-on-insulation (GOI), gallium arsenide (GaAs), strained silicon, silicon germanium, silicon carbide, diamond, and/or other materials. In one embodiment, the substrate 402 may be substantially similar to the substrate 104 and 205 described above. In another embodiment, the substrate 402 may include an air gap to provide insulation for the microelectronic device 400. For example, a 'silicon-on-nothing' (SON) structure may include the semiconductor device(s) 401a and 401b each having a thin insulation layer formed by air and/or other insulators. The gate dielectric 406a and 406b and the gate electrode 408a and 408b may be substantially similar in composition to the gate dielectric layer 120 and 160 and the gate electrode 124 and 164 shown in FIG. 1 and described above." Cheng817 ¶ [0057]. "Alternatively, the gate dielectric 406a and 406b and/or gate electrode 408a and 408b may include multiple layers such as an oxide layer, a high-k dielectric later, a polysilicon layer, strained silicon, silicon germanium, silicon carbide, and/or other material layers. Other materials for the gate dielectric 406a and 406b and the gate electrode 408a and 408b may include titanium (Ti), tantalum (Ta), molybdenum (Mo), cobalt (Co), tungsten (W), titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (W_N), molybdenum silicide (MoSi), tungsten silicide (WSi), cobalt silicide (CoSi), nickel silicide ($NiSi_x$), metal silicides, germanium nanowire, silicon

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nanowire, and/or other materials. The gate dielectric 406a and 407b may comprise a SiO_2 layer and/or nitrided SiO_2. Alternatively, the gate dielectric 406a and 406b material may be replaced by the high-k dielectric. In one embodiment, the high-k layer may be formed from a variety of different materials, such as tantalum nitride, titanium nitride, tantoxide (Ta_2O_5), hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2), hafnium silicon oxy-nitride (HfSiON), hafnium silicide ($HfSi_x$), hafnium silicon nitride ($HfSi_xN_y$), hafnium aluminum dioxide ($HfAlO_2$), nickel silicide ($NiSi_x$), and/or other suitable materials using ALD, CVD, PECVD, evaporation, and/or other methods. Generally, the high-k layer may have a thickness between approximately 2 and 500 Angstroms. With some materials, such as HfSiON, the high-k layer of gate electrode 408a and 408b may be blanket deposited on the surface of substrate 402, while other materials may be selectively deposited. Alternatively, it may be desirable to blanket deposit some materials, including HfSiON, in some fabrication processes, while selectively depositing the same materials in other processes." Cheng817 ¶ [0058]. "The hard masks 410a and 410b may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), titanium nitride (TiN), silicon carbide (SiC), carbide, low-k dielectric, air, and/or other materials. The hard mask 410a and 410b may be formed by lithography, plasma etch, rapid thermal oxidation (RTO), CVD, PECVD, ALD, PVD, and/or other processing techniques now known or to be developed." Cheng817 ¶ [0059]. "The lightly doped regions 422a and 422b may include P-type and N-type dopants for the devices 401a and 401b, respectively. The doped regions 422a and 422b may be formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The doped regions 422a and 422b may also include lightly doped regions (LDD) and/or heavily doped regions in one embodiment. The doped regions 422a and 422b may include impurities such as phosphorous, boron, antimony, arsenic, and/or other materials. For example, the formation of the doped regions 422a and 422b by ion implantation may include an ion implant energy ranging between about 1 KeV and about 100 KeV and the dose of ion implantation of may range between about 1×10^{13} cm^{-2} and about 5×10^{16} cm^{-2}." Cheng817 ¶ [0060]. "In FIG. 4b, sidewall dielectric layers 412 and 414, and spacer material 415 are disposed over the semiconductor device(s) 410a and 401b and are subsequently processed, such as by etching, to form sidewall dielectric structures 412a, 412b, 414a and 414b, and spacers 415a and 415b, as shown in FIG. 4c. Note the dielectric structures 714a and 714b are substantially L-shaped. A dummy spacer layer 416 is formed over the semiconductor devices 401a and 401b. Low temperature processing, such as using a temperature less than 600° C., to form the sidewall dielectric and spacer materials is preferred to reduce lightly doped drain diffusion." Cheng817 ¶ [0061].

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"The sidewall dielectric layers 412 and 414 may be a liner oxide layer and a nitride layer formed over the devices by deposition. In particular, the sidewall dielectric layers 412 and 414 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), polymer and/or other materials. The sidewall dielectric layers 412 and 414 may also include multiple layers and/or may include a single layer, in one embodiment. The sidewall dielectric layers 412 and 414 may be formed by RTO, CVD, PVD, PECVD, ALD, CMP, chemical etching, plasma etching, and/or other processing techniques. The spacer material 415 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), polymer and/or other materials. The spacer material 415 may also include multiple layers and/or may include a single layer, in one embodiment. The spacer material 415 may be formed by RTO, CVD, PVD, PECVD, ALD, CMP, chemical etching, plasma etching, and/or other processing techniques. The sidewall dielectric structures 412a, 412b, 414a and 414b, and spacers 415a and 415b may be formed by chemical etching, plasma etching, CMP, focused ion beam (FIB), and/or other processing techniques." Cheng817 ¶ [0062]. "In FIG. 4d, the dummy spacer material 416 is processed to form the dummy spacers 416a and 416b. The dummy spacer material 416 may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), silicon oxy-carbide (SiOC), polymer, and/or other materials. The spacer material 416 may be formed by CVD, PECVD, ALD, spin-on coating, and/or other processing techniques, for example, and the dummy spacers 416a and 416b may be formed by chemical etch, plasma etch, CMP, focused ion beam (FIB), and/or other processing techniques. In FIG. 4d, a photoresist 417b is provided over the device 401b so that portions of the dummy spacer material 416a is removed from the device 401a, and recessed source and drain regions 418a are also formed in the substrate 402 on either side of the gate structure of the device 401a." Cheng817 ¶ [0063]. "The recessed source and drain regions 418a may be formed by a process such as chemical etch, focused ion beam (FIB), and/or plasma etch. In particular, the recessed regions 418a may be formed by a chemical etch of the exposed substrate interposed by the isolation regions 404 and the dummy spacers 416a. In one embodiment, a portion of the substrate 402 below the dummy spacers 416a may be removed, as shown in FIG. 4d." Cheng817 ¶ [0064].

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"In FIG. 4e, the photoresist 417b is removed, and doped source and drain regions 420a are formed or built-up in the recessed regions 418a. The doped source and drain regions 420a may be formed by selective epitaxial growth (SEG), CVD, PECVD, PVD, PDL, ALD, spin-on formation, and/or other techniques now know or to be developed. The doped source and drain regions 420a may include materials such as amorphous silicon, polysilicon, strained silicon, germanium, silicon germanium, silicon carbide, and/or other materials. Low temperature processing, such as using a temperature less than 700° C., to form the doped regions 420a is preferred to reduce lightly doped drain diffusion." Cheng817 ¶ [0065]. "In FIG. 4g, the photoresist 421a is removed from the device 401a. Further, the hard masks 410a and 410b are removed from the semiconductor devices 401a and 401b. The photoresist 421a may be removed by plasma etch and/or chemical etch. For example, the mask 421a may be removed by an oxygen (O_2) containing plasma environment. The hard masks 410a and 410b may be removed by chemical and/or plasma etch. For example, the hard masks 410a and 410b may be removed by hot phosphoric (H_2PO_4) acid, ammonium hydroxide ($NH_{40}H$), hydrochloric acid (HCl), hydrofluoric acid (HF), sulfuric acid (H_2SO_4), and/or other etchant chemicals. The hard masks 420a and 420b may also be removed by ion bombardment in an inert plasma comprising argon, hydrogen, xenon, and/or other gases." Cheng817 ¶ [0067]. "In FIG. 4h, a photoresist 421b is formed over the semiconductor device 401a. The mask 421b may include photoresist, silicon dioxide (SiO_2), silicon nitride (Si_xN_y), and/or other materials. The mask 421b may be formed by spin-on coating, CVD, and/or other processing techniques. Further, more heavily doped source and drain regions 428a are formed in the substrate 402 for the semiconductor device 401a. The doped regions 428a which may include P-type impurities, and may be formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The ion implantation may include an ion implant energy ranging between about 5 KeV and about 100 KeV and the dose of ion implantation of may range between about 1×10^{14} cm^{-2} and about 5×10^{18} cm^{-2} for example." Cheng817 ¶ [0068]. "In FIG. 4i, the photoresist 421b is removed from the device 401b, and salicided contacts 432a and 432b are formed over the gate, source and drain of the devices 401a and 401b. The salicided contacts 432a and 432b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 732a and 732b may also include an anneal. The salicided contacts 732a and 732b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0069].

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"Further in FIG. 4j, an etch stop layer 430a and 430b are formed over the semiconductor device(s) 401a and 401b. The etch stop layer 430a and 430b may include silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), and/or other materials. In one embodiment, the etch stop layer 430a and 430b may be substantially similar in composition to the etch stop layer 180 described above. Alternatively, the etch stop layer 430a and 430b may include a stress level that may range between about +0.001 and about +50 GPa for tensile film and between about −0.001 and about −50 GPa for compressive film. The etch stop layer 430a and 430b may be formed by CVD, ALD, PECVD, PDL, spin-on coating, and/or other techniques." Cheng817 ¶ [0070]. "Subsequent processing steps may be performed to the semiconductor devices 401a and 401b such as metallization, testing and packaging, etc." Cheng817 ¶ [0071]. "Referring now to FIGS. 5a-i for another embodiment of a method for manufacturing a microelectronic device 500 with high drive current. In FIG. 5a, gate structures including a gate dielectric 506a and 506b and gate electrodes 508a and 508b are formed for semiconductor devices 501a and 501b, respectively. Gate electrodes 508a and 508b may be pre-doped with appropriate P-type and N-type dopants, respectively. Hard masks 510a and 510b are also formed over each gate structure. Further, shallow doped drain and source regions 522a and 522b are formed on either sides of the gate structures of each device 501a and 501b. Isolation structures 504 are formed in the substrate 502 to electrically isolate the devices 501a and 501b." Cheng817 ¶ [0072]. "The substrate 502 may include silicon, silicon-on-insulation (SOI), germanium, germanium-on-insulation (GOI), gallium arsenide (GaAs), strained silicon, diamond, and/or other materials. In another embodiment, the substrate 502 may include an air gap to provide insulation for the microelectronic device 500. For example, a 'silicon-on-nothing' (SON) structure may include the semiconductor devices 501a and 501b each having a thin insulation layer formed by air and/or other insulator. The gate dielectric 506a and 506b and the gate electrode 508a and 508b, in one embodiment, may be substantially similar in composition to the gate dielectric layer 120 and 160 and the gate electrode 124 and 164 shown in FIG. 1. Alternatively, the gate dielectric 506a and 506b and/or gate electrode 508a and 508b may include multiple layers such as an oxide layer, a high-k dielectric later, a polysilicon layer, strained silicon, silicon germanium, silicon carbide, and/or other material layers. Other materials for the gate dielectric 506a and 506b and the gate electrode 508a and 508b may include titanium (Ti), tantalum (Ta), molybdenum (Mo), cobalt (Co), tungsten (W), titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (W_N), molybdenum silicide (MoSi), tungsten silicide (WSi), cobalt silicide (CoSi), nickel silicide ($NiSi_x$), metal silicides, germanium nanowire, silicon nanowire, and/or other materials. The gate dielectric 506a and 506b may comprise a SiO_2 layer and/or nitrided SiO_2. In one embodiment, the high-k layer may be formed from a variety of different materials, such as tantalum nitride,

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titanium nitride, tantoxide (Ta_2O_5), hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2), hafnium silicon oxy-nitride (HfSiON), hafnium silicide ($HfSi_x$), hafnium silicon nitride ($HfSi_xN_y$), hafnium aluminum dioxide ($HfAlO_2$), nickel silicide ($NiSi_x$), and/or other suitable materials using ALD, CVD, PECVD, evaporation, and/or other methods. With some materials, such as HfSiON, the high-k layer of gate electrode 508a and 508b may be blanket deposited on the surface of substrate 502, while other materials may be selectively deposited. Alternatively, it may be desirable to blanket deposit some materials, including HfSiON, in some fabrication processes, while selectively depositing the same materials in other processes." Cheng817 ¶ [0073]. "The hard masks 510a and 510b may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), titanium nitride (TiN), silicon carbide (SiC), carbide, low-k dielectric, air, and/or other materials. The hard mask 510a and 510b may be formed by lithography, plasma etch, rapid thermal oxidation (RTO), CVD, PECVD, ALD, PVD, and/or processing techniques." Cheng817 ¶ [0074]. "The doped source and drain regions 522a and 522b may include N-type and/or P-type doped regions formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The doped regions 522a and 522b may be lightly doped drains (LDD) and may include impurities such as phosphorous, boron, antimony, arsenic, and/or other materials." Cheng817 ¶ [0075]. "In FIG. 5b, sidewall dielectric layers 512 and 514, and a spacer material 515 are formed over the semiconductor devices 510a and 501b, preferably using a low temperature process to reduce LDD diffusion. The sidewall dielectric layers 512 and 514 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), polymer and/or other materials. The spacer material 515 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), polymer and/or other materials. For example, dielectric layers 512 and 514 may comprise a liner oxide layer and a nitride layer, and the spacer material 515 may comprise an oxide material. The sidewall dielectric layers 512 and 514 and spacer layer 515 may be formed by RTO, CVD, PVD, PECVD, ALD, CMP, chemical etching, plasma etching, and/or other processing techniques." Cheng817 ¶ [0076] "In FIG. 5c, the sidewall dielectric layers 512 and 514, and a spacer material 515 are subsequently processed forming sidewall dielectric 512a, 512b, 514a and 514b, and spacers 515a and 515b. The sidewall dielectric 512a, 512b, 514a and 514b, and spacers 515a and 515b may be formed by chemical etching, plasma etching, CMP, focused ion beam (FIB), and/or other processing techniques." Cheng817 ¶ [0077].

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"Further, a dummy spacer material 516 is formed over the semiconductor devices 501a and 501b, and subsequently processed forming the dummy spacers 516a and 516b. The dummy spacer material 516 may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), silicon oxy-carbide (SiOC), polymer, and/or other materials. The spacer material 516 may be formed by CVD, PECVD, ALD, spin-on coating, and/or other processing techniques, and may be formed by chemical etch, plasma etch, CMP, focused ion beam (FIB), and/or other processing techniques." Cheng817 ¶ [0078]. "In FIG. 5d, a photoresist 517b is formed over the semiconductor device 501b so that the device 501 a may be processed. An oxide etch process may be used to remove material layers above the hard mask 510a disposed over the gate structure. Another etch process may also be used to create recessed source and drain regions 518a in the substrate 502. The recessed source and drain regions 518a may be formed by a process such as chemical etch, focused ion beam (FIB), and/or plasma etch. In the embodiment shown in FIG. 5d, a portion of the substrate 502 extending partially below the spacer 516a is also removed." Cheng817 ¶ [0079]. "In FIG. 5e, the photoresist 517b is removed from the device 501b and source and drain regions 520a are built-up in the recessed regions 518a, preferably using a low temperature process to reduce LDD diffusion. The source and drain regions 520a may be formed by, for example, selective epitaxial growth (SEG), CVD, PECVD, PVD, PDL, ALD, spin-on formation, and/or other suitable techniques now know or later developed. The source and drain regions 520a may include materials such as amorphous silicon, polysilicon, strained silicon, germanium, silicon germanium, silicon carbide, and/or other materials. The source and drain regions 520a may also be doped 'in-situ' during the SEG process, for example. In this process, dopants such as boron, phosphorous, arsenic, germanium, carbon, and/or other semiconductor materials may be introduced during the SEG process. The dopants may be introduced in gaseous form, which may include diborane (B_2H_6), Arsine (AsH_3), phosphine (PH_3), germane (GeH_4), phosphoryl chloride ($POCL_3$), boron bromide (BBr_3), hydrocarbons, and/or other gases/chemicals." Cheng817 ¶ [0080]. "In FIG. 5g, the photoresist 521a is removed from the device 501. Further, the hard masks 510a and 510b are removed from the gate structures of the semiconductor devices 501a and 501b. The hard masks 510a and 510b may be removed from the semiconductor devices by chemical and/or plasma etch. For example, the hard masks 510a and 510b may be removed by hot phosphoric (H_2PO_4) acid, ammonium hydroxide (NH_4OH), hydrochloric acid (HCl), hydrofluoric acid (HF), sulfuric acid (H_2SO_4), and/or other chemicals. The hard mask 510a and 510b may also be removed by ion bombardment in an inert plasma comprising argon, hydrogen, xenon, and/or other gases."Cheng817 ¶ [0082].

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"Because the deeper doped source and drain regions were doped in-situ (FIG. 5g), a process of source and drain implantation such as that shown in FIG. 4h is not required. Therefore, salicided contacts 532a and 532b are formed for the gate, source and drains of the devices 501a and 501b, respectively, as shown in FIG. 5h. The salicided contacts 532a and 532b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 532a and 532b may also include an anneal. The salicided contacts 532a and 532b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0083]. "In FIG. 5i, etch stop layer 530a and 530b are formed over the semiconductor devices 501a and 501b. The etch stop layer 530a and 530b may include silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), and/or other materials. Alternatively, the etch stop layer 530a and 530b may include a stress level that may range between about +0.001 and about +50 GPa for tensile film and between about −0.001 and about −50 GPa for compressive film. The etch stop layer 530a-b may be formed by CVD, ALD, PECVD, PDL, spin-on coating, and/or other techniques." Cheng817 ¶ [0084]. *See also*, *e.g.*, Cheng817, at ¶[0060], ¶¶ [0065]-[0068]. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

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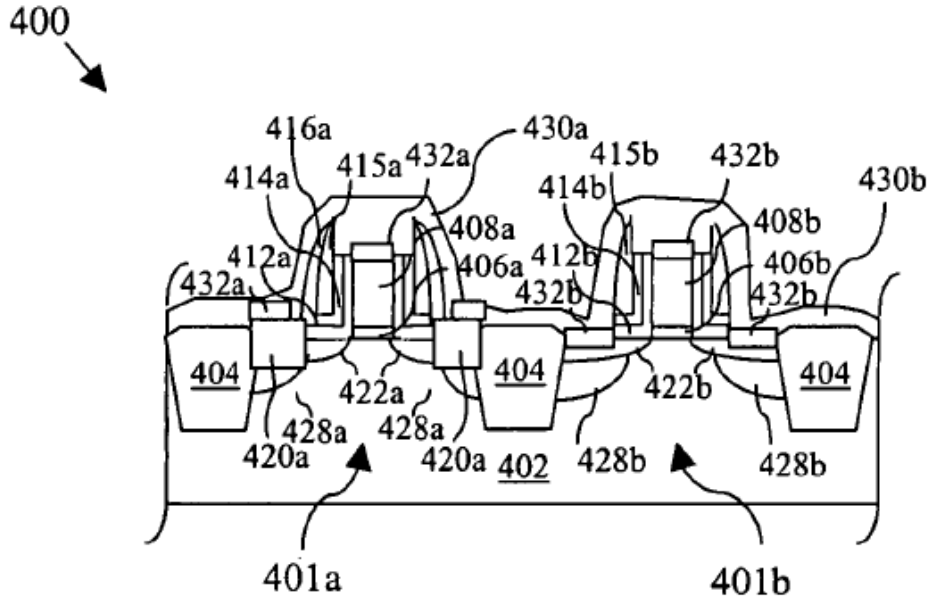
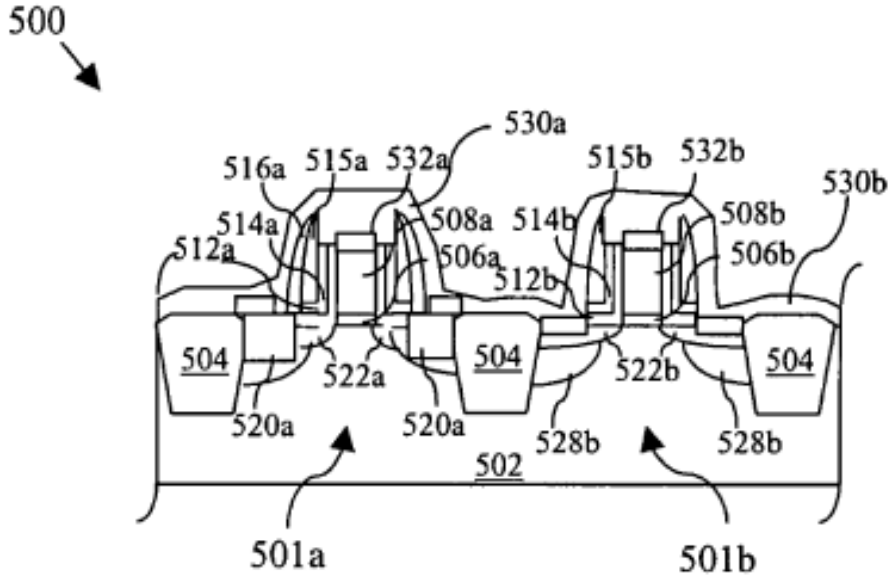
1[b] a first gate insulating film formed on a first active region in a semiconductor substrate,
Cheng817 discloses this feature. For example, Cheng817 discloses a gate dielectric 406a formed on the PMOS active region of a substrate 402. *See, e.g.*, the following:  Cheng817 Fig. 4j.  Cheng817 Fig. 5i.

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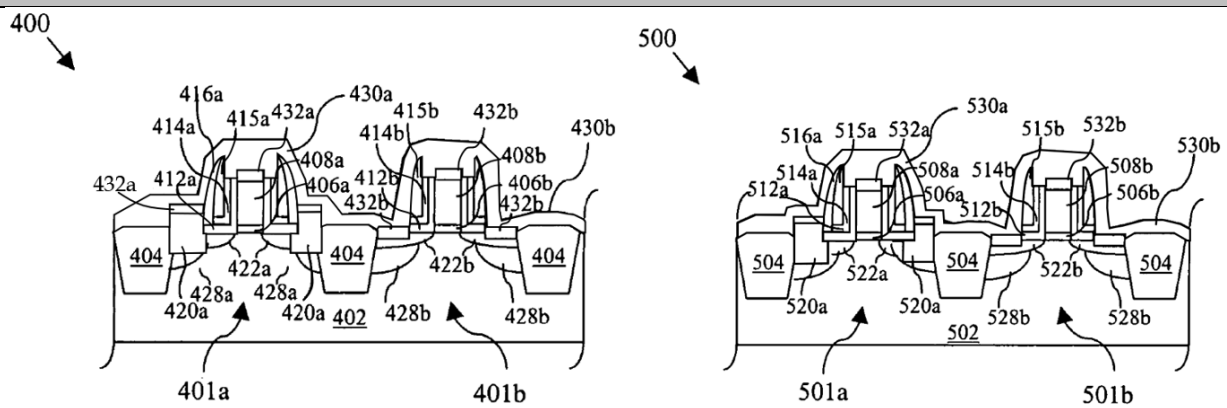

Figure A **Figure B**

(Cheng817, Figs. 4j, 5i (corrected))

"Referring now to FIGS. 4a-4j for sectional views of another embodiment of a method for making semiconductor devices 401a and 401b with high drive current. The semiconductor device 401a may be a P-type MOS device and the semiconductor device 401b may be an N-type MOS device. In FIG. 4a, gate dielectric 406a and 406b are formed over a substrate 402 for devices 401a and 401b, respectively, and electrically isolated from one another by isolation structures 404. The isolation structures 404 may be shallow trench isolation (STI) structures. Gate electrodes 408a and 408b are formed over the gate dielectric layer, and hard masks 410a and 410b are formed over the gate electrodes 408a and 408b, respectively."

Cheng817 ¶ [0056].

"The substrate 402 may include silicon, silicon-on-insulation (SOI), germanium, germanium-on-insulation (GOI), gallium arsenide (GaAs), strained silicon, silicon germanium, silicon carbide, diamond, and/or other materials. In one embodiment, the substrate 402 may be substantially similar to the substrate 104 and 205 described above. In another embodiment, the substrate 402 may include an air gap to provide insulation for the microelectronic device 400. For example, a 'silicon-on-nothing' (SON) structure may include the semiconductor device(s) 401a and 401b each having a thin insulation layer formed by air and/or other insulators. The gate dielectric 406a and 406b and the gate electrode 408a and 408b may be substantially similar in composition to the gate dielectric layer 120 and 160 and the gate electrode 124 and 164 shown in FIG. 1 and described above."

Cheng817 ¶ [0057].

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"Alternatively, the gate dielectric 406a and 406b and/or gate electrode 408a and 408b may include multiple layers such as an oxide layer, a high-k dielectric later, a polysilicon layer, strained silicon, silicon germanium, silicon carbide, and/or other material layers. Other materials for the gate dielectric 406a and 406b and the gate electrode 408a and 408b may include titanium (Ti), tantalum (Ta), molybdenum (Mo), cobalt (Co), tungsten (W), titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (W_N), molybdenum silicide (MoSi), tungsten silicide (WSi), cobalt silicide (CoSi), nickel silicide ($NiSi_x$), metal silicides, germanium nanowire, silicon nanowire, and/or other materials. The gate dielectric 406a and 407b may comprise a SiO_2 layer and/or nitrided SiO_2. Alternatively, the gate dielectric 406a and 406b material may be replaced by the high-k dielectric. In one embodiment, the high-k layer may be formed from a variety of different materials, such as tantalum nitride, titanium nitride, tantoxide (Ta_2O_5), hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2), hafnium silicon oxy-nitride (HfSiON), hafnium silicide ($HfSi_x$), hafnium silicon nitride ($HfSi_xN_y$), hafnium aluminum dioxide ($HfAlO_2$), nickel silicide ($NiSi_x$), and/or other suitable materials using ALD, CVD, PECVD, evaporation, and/or other methods. Generally, the high-k layer may have a thickness between approximately 2 and 500 Angstroms. With some materials, such as HfSiON, the high-k layer of gate electrode 408a and 408b may be blanket deposited on the surface of substrate 402, while other materials may be selectively deposited. Alternatively, it may be desirable to blanket deposit some materials, including HfSiON, in some fabrication processes, while selectively depositing the same materials in other processes." Cheng817 ¶ [0058]. "Referring now to FIGS. 5a-i for another embodiment of a method for manufacturing a microelectronic device 500 with high drive current. In FIG. 5a, gate structures including a gate dielectric 506a and 506b and gate electrodes 508a and 508b are formed for semiconductor devices 501a and 501b, respectively. Gate electrodes 508a and 508b may be pre-doped with appropriate P-type and N-type dopants, respectively. Hard masks 510a and 510b are also formed over each gate structure. Further, shallow doped drain and source regions 522a and 522b are formed on either sides of the gate structures of each device 501a and 501b. Isolation structures 504 are formed in the substrate 502 to electrically isolate the devices 501a and 501b." Cheng817 ¶ [0072]. "The substrate 502 may include silicon, silicon-on-insulation (SOI), germanium, germanium-on-insulation (GOI), gallium arsenide (GaAs), strained silicon, diamond, and/or other materials. In another embodiment, the substrate 502 may include an air gap to provide insulation for the microelectronic device 500. For example, a 'silicon-on-nothing' (SON) structure may include the semiconductor devices 501a and 501b each having a thin insulation layer formed by air and/or other insulator. The gate dielectric 506a and 506b and the gate electrode 508a and 508b, in one embodiment, may be substantially similar in composition to the gate dielectric layer 120 and 160 and the gate electrode 124 and 164 shown in FIG. 1. Alternatively, the gate dielectric 506a and 506b and/or gate electrode 508a and 508b may include multiple layers such as an oxide layer, a high-k dielectric later, a polysilicon layer, strained silicon, silicon germanium, silicon carbide,

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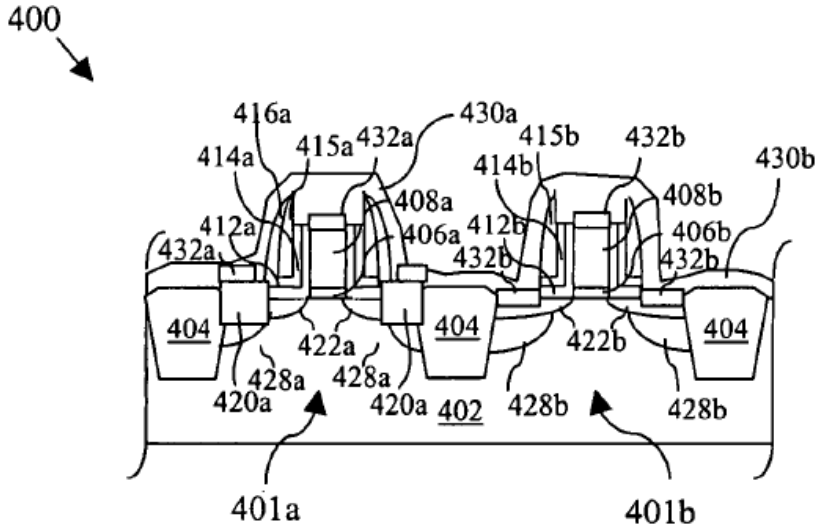
and/or other material layers. Other materials for the gate dielectric 506a and 506b and the gate electrode 508a and 508b may include titanium (Ti), tantalum (Ta), molybdenum (Mo), cobalt (Co), tungsten (W), titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (W_N), molybdenum silicide (MoSi), tungsten silicide (WSi), cobalt silicide (CoSi), nickel silicide ($NiSi_x$), metal silicides, germanium nanowire, silicon nanowire, and/or other materials. The gate dielectric 506a and 506b may comprise a SiO_2 layer and/or nitrided SiO_2. In one embodiment, the high-k layer may be formed from a variety of different materials, such as tantalum nitride, titanium nitride, tantoxide (Ta_2O_5), hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2), hafnium silicon oxy-nitride (HfSiON), hafnium silicide ($HfSi_x$), hafnium silicon nitride ($HfSi_xN_y$), hafnium aluminum dioxide ($HfAlO_2$), nickel silicide ($NiSi_x$), and/or other suitable materials using ALD, CVD, PECVD, evaporation, and/or other methods. With some materials, such as HfSiON, the high-k layer of gate electrode 508a and 508b may be blanket deposited on the surface of substrate 502, while other materials may be selectively deposited. Alternatively, it may be desirable to blanket deposit some materials, including HfSiON, in some fabrication processes, while selectively depositing the same materials in other processes." Cheng817 ¶ [0073]. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
1[c] a first gate electrode formed on the first gate insulating film,
Cheng817 discloses this feature. For example, Cheng817 discloses a PMOS gate 408a formed on the PMOS gate dielectric 406a. *See, e.g.*, the following:    Cheng817 Fig. 4j.

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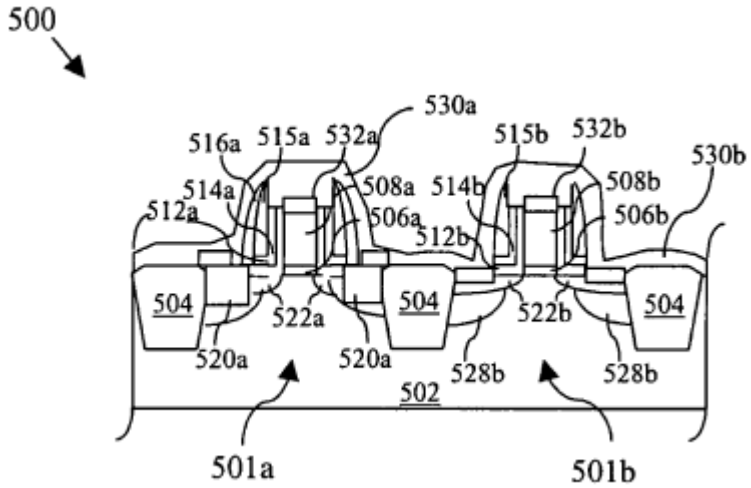
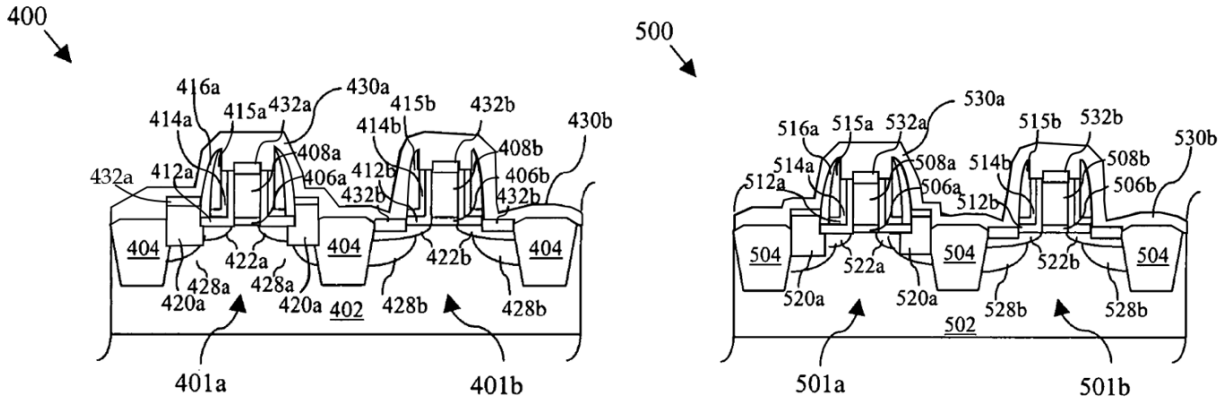
 Cheng817 Fig. 5i.  **Figure A** **Figure B** **(Cheng817, Figs. 4j, 5i (corrected))** “Referring now to FIGS. 4a-4j for sectional views of another embodiment of a method for making semiconductor devices 401a and 401b with high drive current. The semiconductor device 401a may be a P-type MOS device and the semiconductor device 401b may be an N-type MOS device. In FIG. 4a, gate dielectric 406a and 406b are formed over a substrate 402 for devices 401a and 401b, respectively, and electrically isolated from one another by isolation structures 404. The isolation structures 404 may be shallow trench isolation (STI) structures. Gate electrodes 408a and 408b are formed over the gate dielectric layer, and hard masks 410a and 410b are formed over the gate electrodes 408a and 408b, respectively.” Cheng817 ¶ [0056].

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"The substrate 402 may include silicon, silicon-on-insulation (SOI), germanium, germanium-on-insulation (GOI), gallium arsenide (GaAs), strained silicon, silicon germanium, silicon carbide, diamond, and/or other materials. In one embodiment, the substrate 402 may be substantially similar to the substrate 104 and 205 described above. In another embodiment, the substrate 402 may include an air gap to provide insulation for the microelectronic device 400. For example, a 'silicon-on-nothing' (SON) structure may include the semiconductor device(s) 401a and 401b each having a thin insulation layer formed by air and/or other insulators. The gate dielectric 406a and 406b and the gate electrode 408a and 408b may be substantially similar in composition to the gate dielectric layer 120 and 160 and the gate electrode 124 and 164 shown in FIG. 1 and described above." Cheng817 ¶ [0057]. "Alternatively, the gate dielectric 406a and 406b and/or gate electrode 408a and 408b may include multiple layers such as an oxide layer, a high-k dielectric later, a polysilicon layer, strained silicon, silicon germanium, silicon carbide, and/or other material layers. Other materials for the gate dielectric 406a and 406b and the gate electrode 408a and 408b may include titanium (Ti), tantalum (Ta), molybdenum (Mo), cobalt (Co), tungsten (W), titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (W_N), molybdenum silicide (MoSi), tungsten silicide (WSi), cobalt silicide (CoSi), nickel silicide ($NiSi_x$), metal silicides, germanium nanowire, silicon nanowire, and/or other materials. The gate dielectric 406a and 407b may comprise a SiO_2 layer and/or nitrided SiO_2. Alternatively, the gate dielectric 406a and 406b material may be replaced by the high-k dielectric. In one embodiment, the high-k layer may be formed from a variety of different materials, such as tantalum nitride, titanium nitride, tantoxide (Ta_2O_5), hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2), hafnium silicon oxy-nitride (HfSiON), hafnium silicide ($HfSi_x$), hafnium silicon nitride ($HfSi_xN_y$), hafnium aluminum dioxide ($HfAlO_2$), nickel silicide ($NiSi_x$), and/or other suitable materials using ALD, CVD, PECVD, evaporation, and/or other methods. Generally, the high-k layer may have a thickness between approximately 2 and 500 Angstroms. With some materials, such as HfSiON, the high-k layer of gate electrode 408a and 408b may be blanket deposited on the surface of substrate 402, while other materials may be selectively deposited. Alternatively, it may be desirable to blanket deposit some materials, including HfSiON, in some fabrication processes, while selectively depositing the same materials in other processes." Cheng817 ¶ [0058]. "Referring now to FIGS. 5a-i for another embodiment of a method for manufacturing a microelectronic device 500 with high drive current. In FIG. 5a, gate structures including a gate dielectric 506a and 506b and gate electrodes 508a and 508b are formed for semiconductor devices 501a and 501b, respectively. Gate electrodes 508a and 508b may be pre-doped with appropriate P-type and N-type dopants, respectively. Hard masks 510a and 510b are also formed over each gate structure. Further, shallow doped drain and source regions 522a and 522b are formed on

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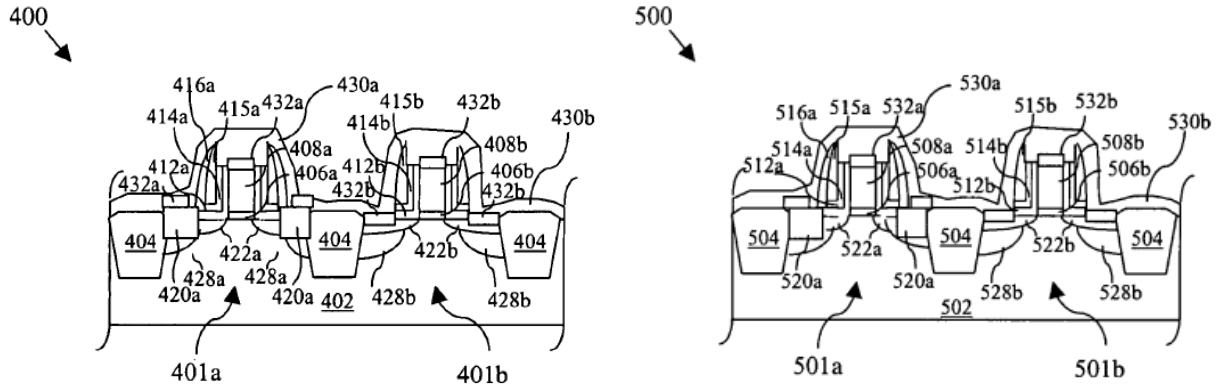
either sides of the gate structures of each device 501a and 501b. Isolation structures 504 are formed in the substrate 502 to electrically isolate the devices 501a and 501b." Cheng817 ¶ [0072]. "The substrate 502 may include silicon, silicon-on-insulation (SOI), germanium, germanium-on-insulation (GOI), gallium arsenide (GaAs), strained silicon, diamond, and/or other materials. In another embodiment, the substrate 502 may include an air gap to provide insulation for the microelectronic device 500. For example, a 'silicon-on-nothing' (SON) structure may include the semiconductor devices 501a and 501b each having a thin insulation layer formed by air and/or other insulator. The gate dielectric 506a and 506b and the gate electrode 508a and 508b, in one embodiment, may be substantially similar in composition to the gate dielectric layer 120 and 160 and the gate electrode 124 and 164 shown in FIG. 1. Alternatively, the gate dielectric 506a and 506b and/or gate electrode 508a and 508b may include multiple layers such as an oxide layer, a high-k dielectric later, a polysilicon layer, strained silicon, silicon germanium, silicon carbide, and/or other material layers. Other materials for the gate dielectric 506a and 506b and the gate electrode 508a and 508b may include titanium (Ti), tantalum (Ta), molybdenum (Mo), cobalt (Co), tungsten (W), titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (W_N), molybdenum silicide (MoSi), tungsten silicide (WSi), cobalt silicide (CoSi), nickel silicide ($NiSi_x$), metal silicides, germanium nanowire, silicon nanowire, and/or other materials. The gate dielectric 506a and 506b may comprise a SiO_2 layer and/or nitrided SiO_2. In one embodiment, the high-k layer may be formed from a variety of different materials, such as tantalum nitride, titanium nitride, tantoxide (Ta_2O_5), hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2), hafnium silicon oxy-nitride (HfSiON), hafnium silicide ($HfSi_x$), hafnium silicon nitride ($HfSi_xN_y$), hafnium aluminum dioxide ($HfAlO_2$), nickel silicide ($NiSi_x$), and/or other suitable materials using ALD, CVD, PECVD, evaporation, and/or other methods. With some materials, such as HfSiON, the high-k layer of gate electrode 508a and 508b may be blanket deposited on the surface of substrate 502, while other materials may be selectively deposited. Alternatively, it may be desirable to blanket deposit some materials, including HfSiON, in some fabrication processes, while selectively depositing the same materials in other processes." Cheng817 ¶ [0073]. Additionally, under Plaintiff's apparent interpretation of the claim language, the claimed "first gate electrode" may include a silicide film. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 11-13, 18, 20, 22, 24-25, 26, 39. Although TSMC does not necessarily agree with such an interpretation, Cheng817 further discloses this element under this interpretation, as shown below. For example, Cheng817 discloses silicide 432a formed on PMOS gate electrode 408a. *See, e.g.*, the following:

Exemplary Disclosures



Cheng817 Figs. 4j, 5i.

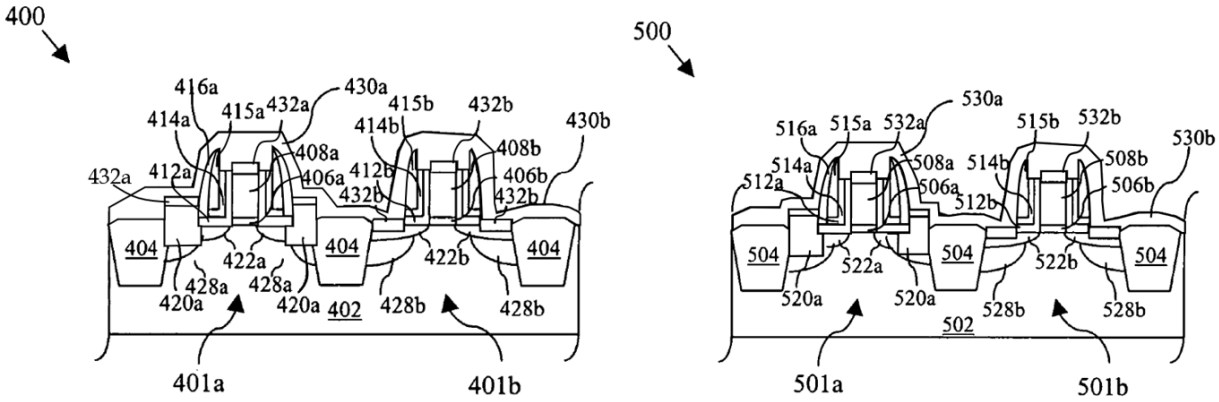


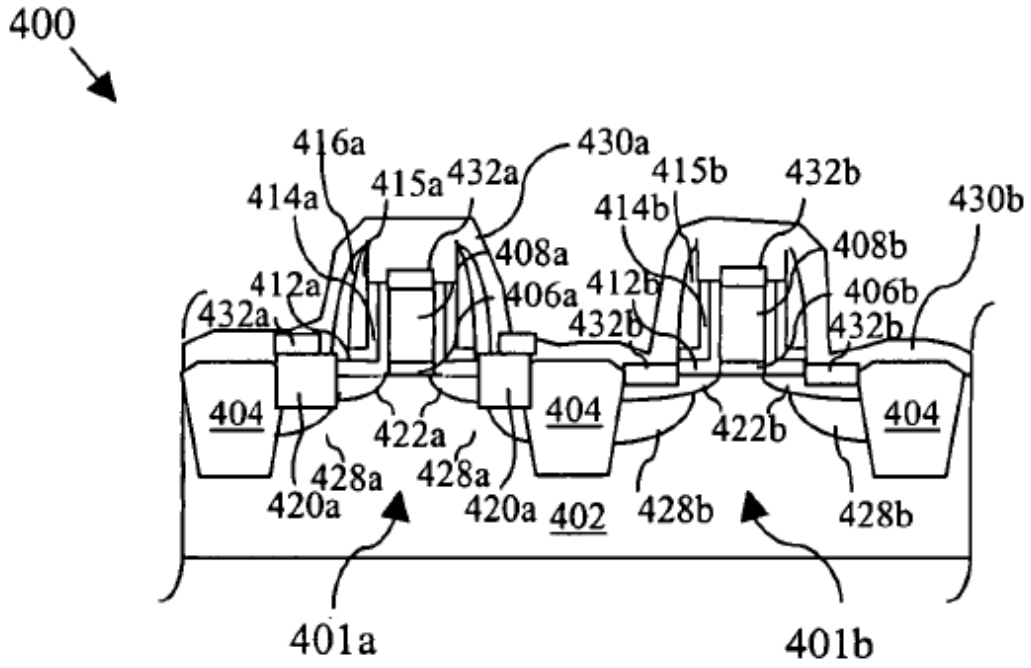
Figure A **Figure B**

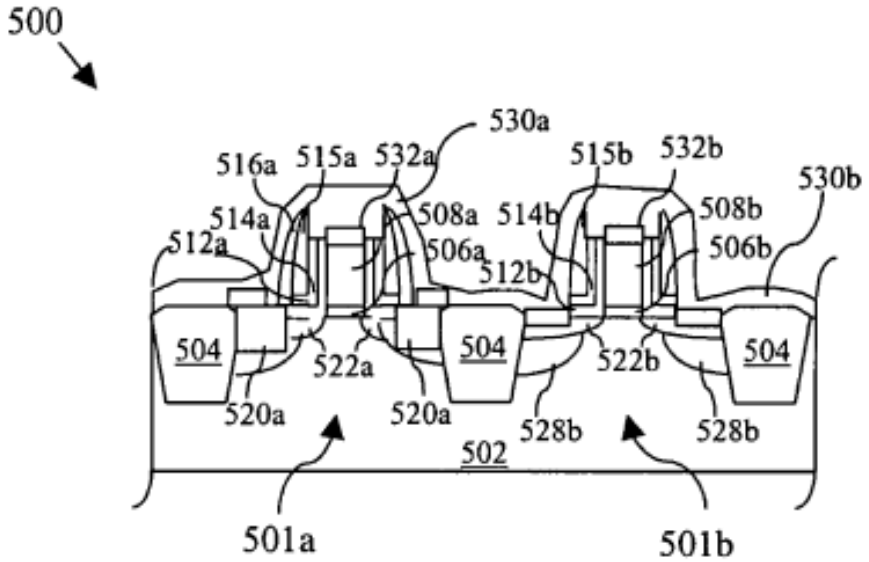
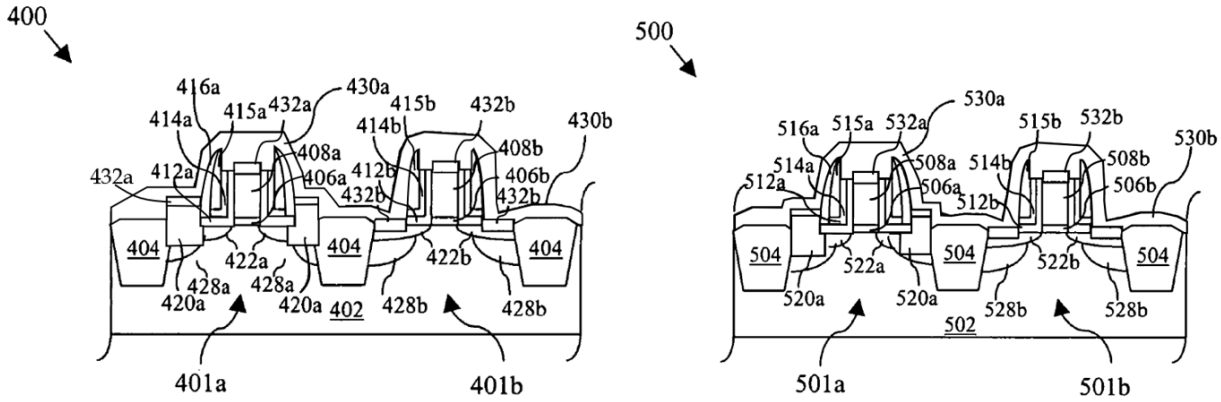
(Cheng817, Figs. 4j, 5i (corrected))

"In FIG. 4i, the photoresist 421b is removed from the device 401b, and salicided contacts 432a and 432b are formed over the gate, source and drain of the devices 401a and 401b. The salicided contacts 432a and 432b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 732a and 732b may also include an anneal. The salicided contacts 732a and 732b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques."

Cheng817 ¶ [0069].

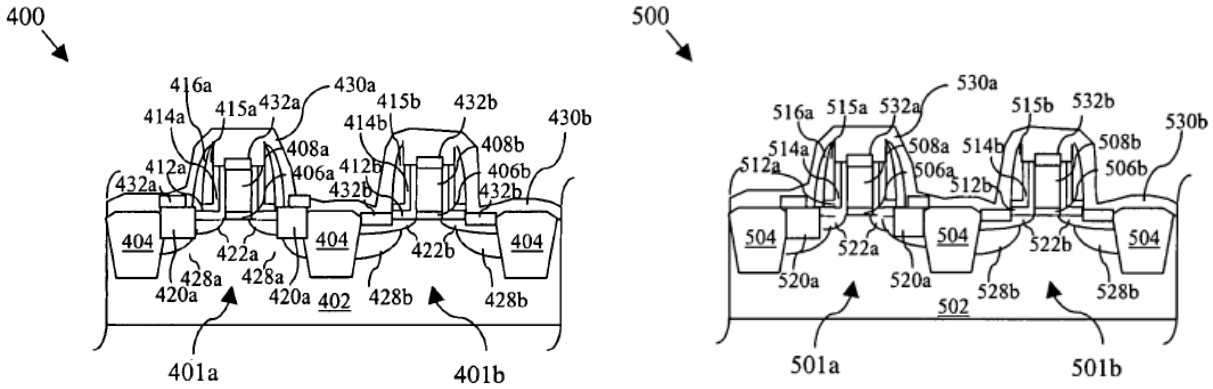
"Because the deeper doped source and drain regions were doped in-situ (FIG. 5g), a process of source and drain implantation such as that shown in FIG. 4h is not required. Therefore, salicided contacts 532a and 532b are formed for the gate, source and drains of the devices 501a and 501b, respectively, as shown in FIG. 5h. The salicided contacts 532a and 532b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel

Exemplary Disclosures
silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 532a and 532b may also include an anneal. The salicided contacts 532a and 532b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0083]. *See also, e.g.,* Cheng817 ¶ [0003], ¶ [0019], ¶ [0041], ¶ [0052], ¶ [0058], ¶ [0069], ¶ [0073], ¶ [0083], ¶ [0087], ¶ [0097], ¶ [0099], ¶ [0101], FIGS. 1, 2, 3n, 4i-4j, 5h-5i, 6h-6i, 7. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
1[d] a first sidewall spacer formed on a side surface of the first gate electrode,
Cheng817 discloses this feature. For example, Cheng817 discloses L-shaped spacers 412a, 414a and spacers 415a, each formed on a side surface of PMOS gate electrode 408a. L-shaped spacers 412a, 414a and spacers 415a, together or individually, constitute a first sidewall spacer. *See, e.g.*, the following:    Cheng817 Fig. 4j.

Exemplary Disclosures
 Cheng817 Fig. 5i.  **Figure A** **Figure B** **(Cheng817, Figs. 4j, 5i (corrected))** "In FIG. 4b, sidewall dielectric layers 412 and 414, and spacer material 415 are disposed over the semiconductor device(s) 410a and 401b and are subsequently processed, such as by etching, to form sidewall dielectric structures 412a, 412b, 414a and 414b, and spacers 415a and 415b, as shown in FIG. 4c. Note the dielectric structures 714a and 714b are substantially L-shaped. A dummy spacer layer 416 is formed over the semiconductor devices 401a and 401b. Low temperature processing, such as using a temperature less than 600° C., to form the sidewall dielectric and spacer materials is preferred to reduce lightly doped drain diffusion." Cheng817 ¶ [0061].

Exemplary Disclosures
"The sidewall dielectric layers 412 and 414 may be a liner oxide layer and a nitride layer formed over the devices by deposition. In particular, the sidewall dielectric layers 412 and 414 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), polymer and/or other materials. The sidewall dielectric layers 412 and 414 may also include multiple layers and/or may include a single layer, in one embodiment. The sidewall dielectric layers 412 and 414 may be formed by RTO, CVD, PVD, PECVD, ALD, CMP, chemical etching, plasma etching, and/or other processing techniques. The spacer material 415 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), polymer and/or other materials. The spacer material 415 may also include multiple layers and/or may include a single layer, in one embodiment. The spacer material 415 may be formed by RTO, CVD, PVD, PECVD, ALD, CMP, chemical etching, plasma etching, and/or other processing techniques. The sidewall dielectric structures 412a, 412b, 414a and 414b, and spacers 415a and 415b may be formed by chemical etching, plasma etching, CMP, focused ion beam (FIB), and/or other processing techniques." Cheng817 ¶ [0062]. "In FIG. 5b, sidewall dielectric layers 512 and 514, and a spacer material 515 are formed over the semiconductor devices 510a and 501b, preferably using a low temperature process to reduce LDD diffusion. The sidewall dielectric layers 512 and 514 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), polymer and/or other materials. The spacer material 515 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), polymer and/or other materials. For example, dielectric layers 512 and 514 may comprise a liner oxide layer and a nitride layer, and the spacer material 515 may comprise an oxide material. The sidewall dielectric layers 512 and 514 and spacer layer 515 may be formed by RTO, CVD, PVD, PECVD, ALD, CMP, chemical etching, plasma etching, and/or other processing techniques." Cheng817 ¶ [0076] "In FIG. 5c, the sidewall dielectric layers 512 and 514, and a spacer material 515 are subsequently processed forming sidewall dielectric 512a, 512b, 514a and 514b, and spacers 515a and 515b. The sidewall dielectric 512a, 512b, 514a and 514b, and spacers 515a and 515b may be formed by chemical etching, plasma etching, CMP, focused ion beam (FIB), and/or other processing techniques." Cheng817 ¶ [0077]. Additionally, under Plaintiff's apparent interpretation of the claim language, the claimed "first gate electrode" may include a silicide film. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 11-13, 18, 20, 22, 24-25, 26, 39. Although TSMC does not necessarily agree with such an interpretation, Cheng817 further discloses this element under this interpretation, as shown below.

Exemplary Disclosures
For example, Cheng817 discloses silicide 432a formed on PMOS gate electrode 408a. *See, e.g.*, the following:



Cheng817 Figs. 4j, 5i.

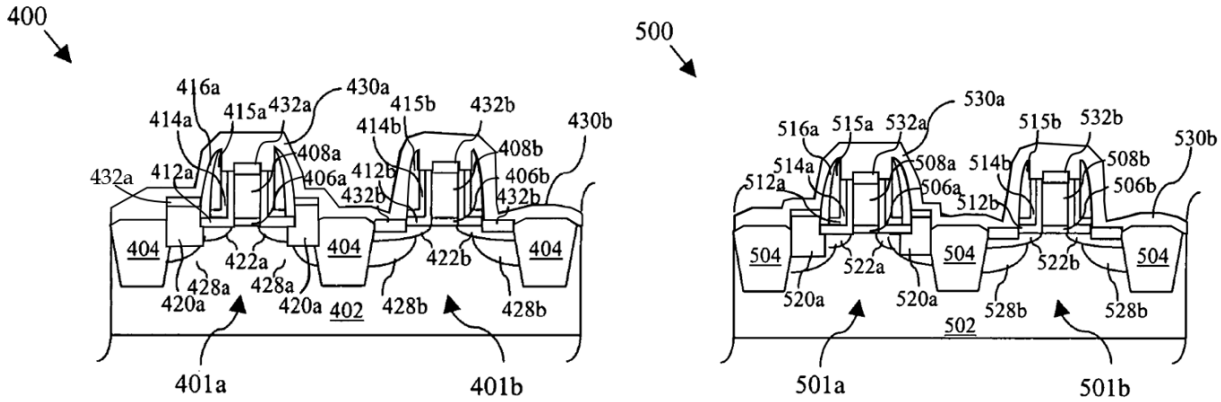
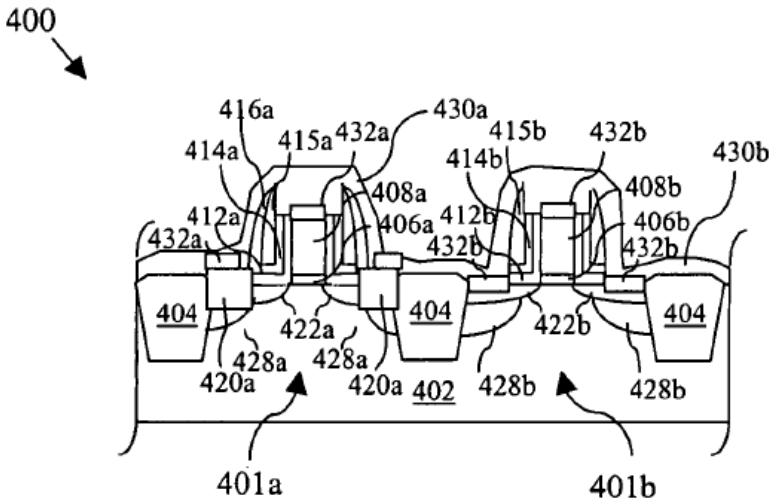


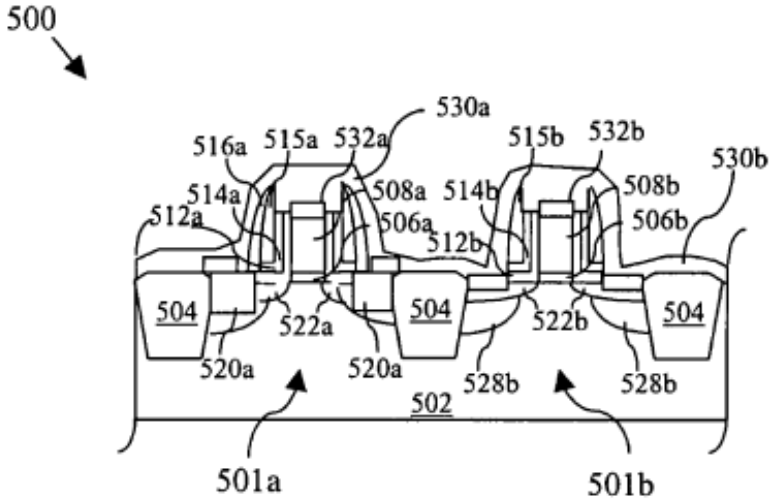
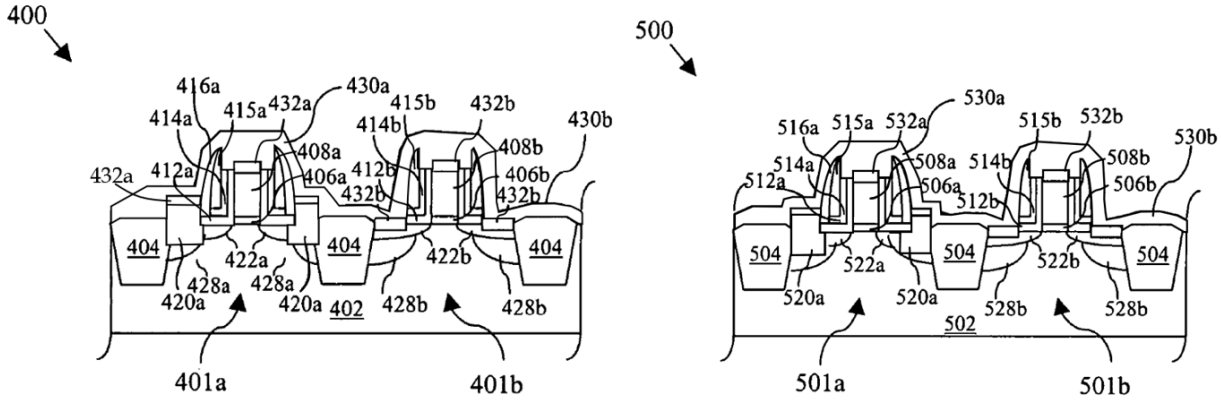
Figure A **Figure B**

(Cheng817, Figs. 4j, 5i (corrected))

"In FIG. 4i, the photoresist 421b is removed from the device 401b, and salicided contacts 432a and 432b are formed over the gate, source and drain of the devices 401a and 401b. The salicided contacts 432a and 432b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 732a and 732b may also include an anneal. The salicided contacts 732a and 732b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques."

Cheng817 ¶ [0069].

Exemplary Disclosures
"Because the deeper doped source and drain regions were doped in-situ (FIG. 5g), a process of source and drain implantation such as that shown in FIG. 4h is not required. Therefore, salicided contacts 532a and 532b are formed for the gate, source and drains of the devices 501a and 501b, respectively, as shown in FIG. 5h. The salicided contacts 532a and 532b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 532a and 532b may also include an anneal. The salicided contacts 532a and 532b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0083]. *See also, e.g.,* Cheng817 ¶ [0003], ¶ [0019], ¶ [0041], ¶ [0052], ¶ [0058], ¶ [0069], ¶ [0073], ¶ [0083], ¶ [0087], ¶ [0097], ¶ [0099], ¶ [0101], FIGS. 1, 2, 3n, 4i-4j, 5h-5i, 6h-6i, 7. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
1[e] a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and
Cheng817 discloses this feature. For example, Cheng817 discloses PMOS epitaxial doped source/drain regions 420a of a p-type conductivity which is formed in recesses 418a provided in the PMOS active region on a lateral side of L-shaped spacers 412a, 414a and spacers 415a. PMOS epitaxial source/drain regions 420a comprise SiGe, which causes a compressive stress in a gate length direction of a channel region in the PMOS active region. *See, e.g.*, the following:    Cheng817 Fig. 4j (showing epitaxial SiGe source/drain regions 420a formed in recesses 418a).

Exemplary Disclosures
 Cheng817 Fig. 5i (showing epitaxial SiGe source/drain regions 520a formed in recesses 518a).  **Figure A** **Figure B** **(Cheng817, Figs. 4j, 5i (corrected))**

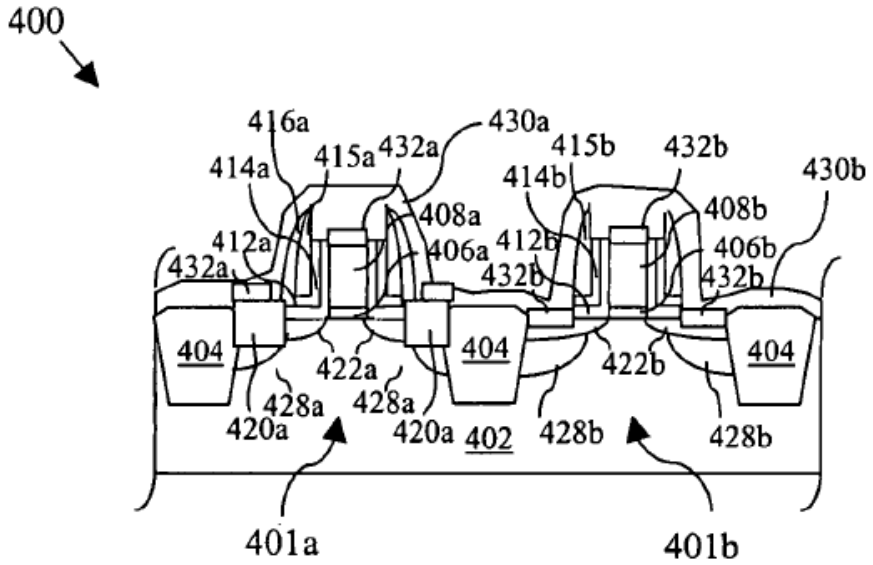
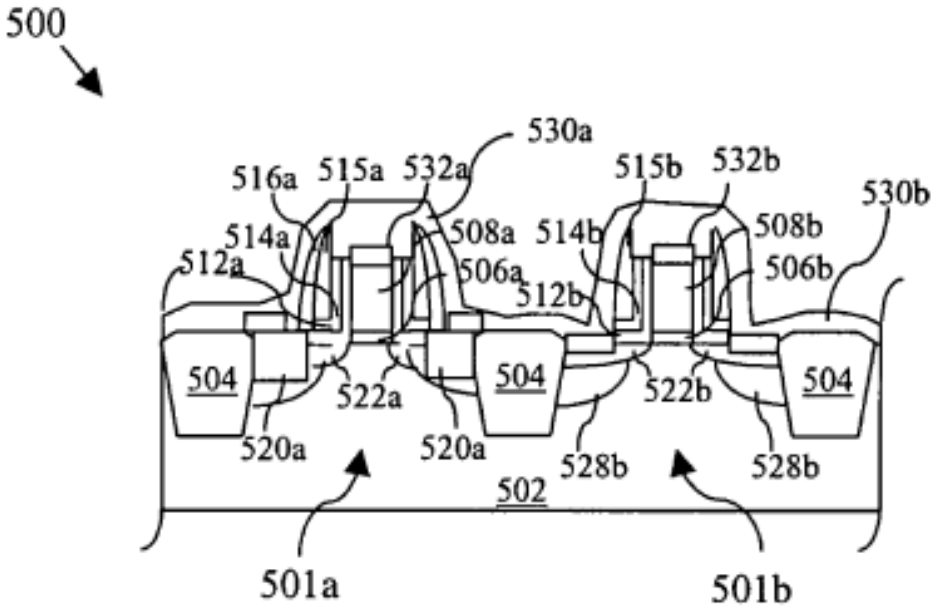
"Thus, the present disclosure introduces a semiconductor device including, in one embodiment, an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface; and (2) first source/drain regions extending from the surface. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface."

Exemplary Disclosures
Cheng817 ¶ [0033]. "In another embodiment, semiconductor device constructed according to aspects of the present disclosure comprises an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface. A second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different." Cheng817 ¶ [0034]. "Another embodiment of a semiconductor device constructed according to aspects of the present disclosure includes an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; (2) a first gate interposing the first source/drain regions; and (3) first spacers on opposing sides of the first gate and each extending from the first gate to a first width. A second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; (2) a second gate interposing the second source/drain regions; and (3) second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different." Cheng817 ¶ [0035]. "In another embodiment, a semiconductor device constructed according to aspects of the present disclosure includes an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe; (2) second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and (3) second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe." Cheng817 ¶ [0036].

Exemplary Disclosures
"The present disclosure also introduces a method of manufacturing semiconductor device. In one embodiment, the method includes forming an isolation region located in a substrate, forming an NMOS device located partially over a surface of the substrate, and forming a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface; and (2) first source/drain regions extending from the surface. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface." Cheng817 ¶ [0037]. "Referring now to FIGS. 4a-4j for sectional views of another embodiment of a method for making semiconductor devices 401a and 401b with high drive current. The semiconductor device 401a may be a P-type MOS device and the semiconductor device 401b may be an N-type MOS device. In FIG. 4a, gate dielectric 406a and 406b are formed over a substrate 402 for devices 401a and 401b, respectively, and electrically isolated from one another by isolation structures 404. The isolation structures 404 may be shallow trench isolation (STI) structures. Gate electrodes 408a and 408b are formed over the gate dielectric layer, and hard masks 410a and 410b are formed over the gate electrodes 408a and 408b, respectively." Cheng817 ¶ [0056]. "The lightly doped regions 422a and 422b may include P-type and N-type dopants for the devices 401a and 401b, respectively. The doped regions 422a and 422b may be formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The doped regions 422a and 422b may also include lightly doped regions (LDD) and/or heavily doped regions in one embodiment. The doped regions 422a and 422b may include impurities such as phosphorous, boron, antimony, arsenic, and/or other materials. For example, the formation of the doped regions 422a and 422b by ion implantation may include an ion implant energy ranging between about 1 KeV and about 100 KeV and the dose of ion implantation of may range between about 1×10^{13} cm^{-2} and about 5×10^{16} cm^{-2}." Cheng817 ¶ [0060]. "In FIG. 4d, the dummy spacer material 416 is processed to form the dummy spacers 416a and 416b. The dummy spacer material 416 may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), silicon oxy-carbide (SiOC), polymer, and/or other materials. The spacer material 416 may be formed by CVD, PECVD, ALD, spin-on coating, and/or other processing techniques, for example, and the dummy spacers 416a and 416b may be formed by chemical etch, plasma etch, CMP, focused ion beam (FIB), and/or other processing techniques.

Exemplary Disclosures
In FIG. 4d, a photoresist 417b is provided over the device 401b so that portions of the dummy spacer material 416a is removed from the device 401a, and recessed source and drain regions 418a are also formed in the substrate 402 on either side of the gate structure of the device 401a." Cheng817 ¶ [0063]. "The recessed source and drain regions 418a may be formed by a process such as chemical etch, focused ion beam (FIB), and/or plasma etch. In particular, the recessed regions 418a may be formed by a chemical etch of the exposed substrate interposed by the isolation regions 404 and the dummy spacers 416a. In one embodiment, a portion of the substrate 402 below the dummy spacers 416a may be removed, as shown in FIG. 4d." Cheng817 ¶ [0064]. "In FIG. 4e, the photoresist 417b is removed, and doped source and drain regions 420a are formed or built-up in the recessed regions 418a. The doped source and drain regions 420a may be formed by selective epitaxial growth (SEG), CVD, PECVD, PVD, PDL, ALD, spin-on formation, and/or other techniques now know or to be developed. The doped source and drain regions 420a may include materials such as amorphous silicon, polysilicon, strained silicon, germanium, silicon germanium, silicon carbide, and/or other materials. Low temperature processing, such as using a temperature less than 700° C., to form the doped regions 420a is preferred to reduce lightly doped drain diffusion." Cheng817 ¶ [0065]. "In FIG. 4h, a photoresist 421b is formed over the semiconductor device 401a. The mask 421b may include photoresist, silicon dioxide (SiO_2), silicon nitride (Si_xN_y), and/or other materials. The mask 421b may be formed by spin-on coating, CVD, and/or other processing techniques. Further, more heavily doped source and drain regions 428a are formed in the substrate 402 for the semiconductor device 401a. The doped regions 428a which may include P-type impurities, and may be formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The ion implantation may include an ion implant energy ranging between about 5 KeV and about 100 KeV and the dose of ion implantation of may range between about 1×10^{14} cm^{-2} and about 5×10^{18} cm^{-2} for example." Cheng817 ¶ [0068]. "Referring now to FIGS. 5a-i for another embodiment of a method for manufacturing a microelectronic device 500 with high drive current. In FIG. 5a, gate structures including a gate dielectric 506a and 506b and gate electrodes 508a and 508b are formed for semiconductor devices 501a and 501b, respectively. Gate electrodes 508a and 508b may be pre-doped with appropriate P-type and N-type dopants, respectively. Hard masks 510a and 510b are also formed over each gate structure. Further, shallow doped drain and source regions 522a and 522b are formed on

Exemplary Disclosures
either sides of the gate structures of each device 501a and 501b. Isolation structures 504 are formed in the substrate 502 to electrically isolate the devices 501a and 501b." Cheng817 ¶ [0072]. "The doped source and drain regions 522a and 522b may include N-type and/or P-type doped regions formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The doped regions 522a and 522b may be lightly doped drains (LDD) and may include impurities such as phosphorous, boron, antimony, arsenic, and/or other materials." Cheng817 ¶ [0075]. "In FIG. 5d, a photoresist 517b is formed over the semiconductor device 501b so that the device 501 a may be processed. An oxide etch process may be used to remove material layers above the hard mask 510a disposed over the gate structure. Another etch process may also be used to create recessed source and drain regions 518a in the substrate 502. The recessed source and drain regions 518a may be formed by a process such as chemical etch, focused ion beam (FIB), and/or plasma etch. In the embodiment shown in FIG. 5d, a portion of the substrate 502 extending partially below the spacer 516a is also removed." Cheng817 ¶ [0079]. "In FIG. 5e, the photoresist 517b is removed from the device 501b and source and drain regions 520a are built-up in the recessed regions 518a, preferably using a low temperature process to reduce LDD diffusion. The source and drain regions 520a may be formed by, for example, selective epitaxial growth (SEG), CVD, PECVD, PVD, PDL, ALD, spin-on formation, and/or other suitable techniques now know or later developed. The source and drain regions 520a may include materials such as amorphous silicon, polysilicon, strained silicon, germanium, silicon germanium, silicon carbide, and/or other materials. The source and drain regions 520a may also be doped 'in-situ' during the SEG process, for example. In this process, dopants such as boron, phosphorous, arsenic, germanium, carbon, and/or other semiconductor materials may be introduced during the SEG process. The dopants may be introduced in gaseous form, which may include diborane (B_2H_6), Arsine (AsH_3), phosphine (PH_3), germane (GeH_4), phosphoryl chloride ($POCL_3$), boron bromide (BBr_3), hydrocarbons, and/or other gases/chemicals." Cheng817 ¶ [0080]. *See also, e.g.,* Cheng817, ¶¶ [0002]-[0003], ¶¶ [0022]-[0023], ¶ [0033]-[0037], ¶ [0044], ¶ [0046], ¶ [0052], ¶ [0056], ¶ [0060], ¶¶ [0063]-[0065], ¶¶ [0068]-[0069], ¶ [0072], ¶ [0075], ¶¶ [0079]-[0080], ¶ [0083], ¶¶ [0093]-[0094], ¶ [0101], FIGS. 1, 2, 3e-3n, 4d-4j, 5d-5i, 6d-6i, 7. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

Exemplary Disclosures
1[f] which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region, and
Cheng817 discloses this feature. *See, e.g.*, *supra* 1[e]. *See, e.g.*, the following:  Cheng817 Fig. 4j. 

Exemplary Disclosures
Cheng817 Fig. 5i.

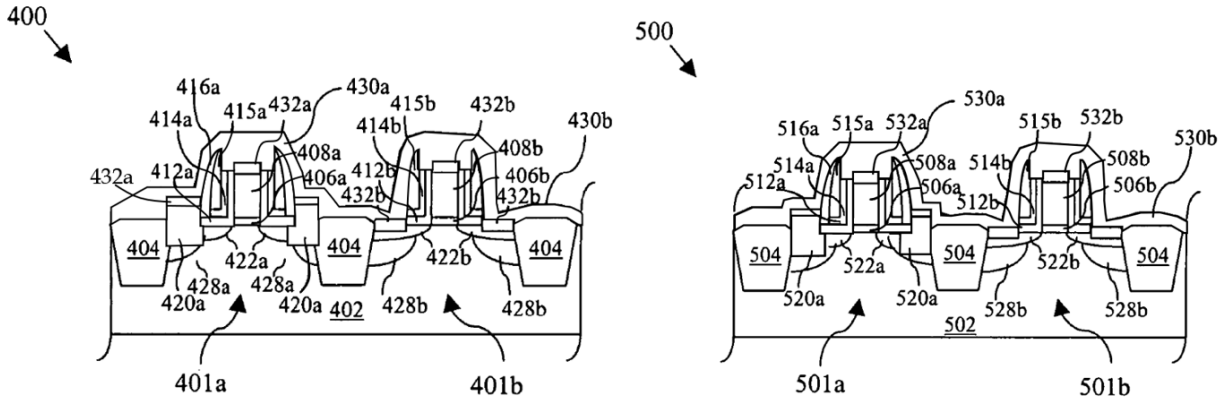


Figure A **Figure B**

(Cheng817, Figs. 4j, 5i (corrected))

"[I]ncreasing the tensile stress in the substrate can improve the performance of n-channel metal-oxide-semiconductor (NMOS) devices. Similarly, increasing the compressive stress in the substrate can improve the performance of p-channel metal-oxide-semiconductor (PMOS) devices."

Cheng817 ¶ [0002].

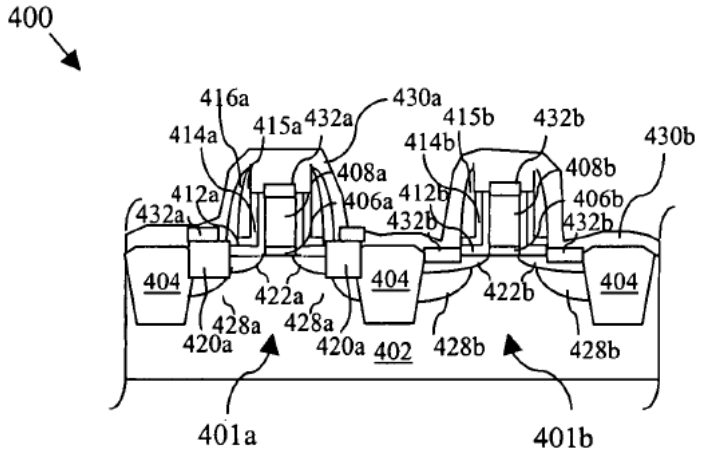
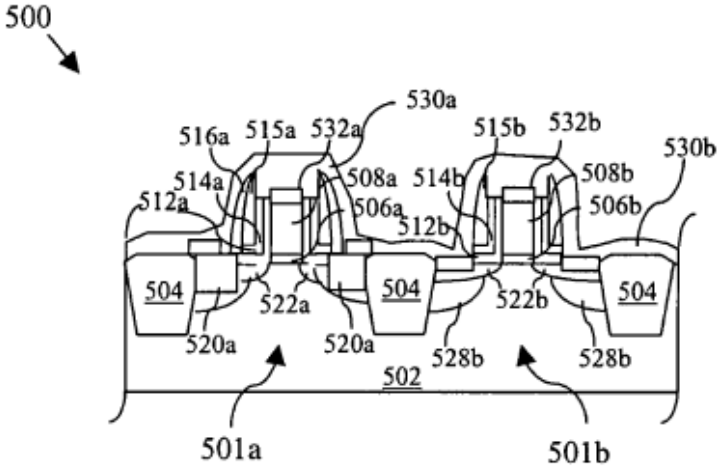
"In such embodiments, the source/drain regions 136 may comprise silicon, silicon germanium, silicon carbide, gallium arsenide and/or other materials, and may be formed by dry etching or otherwise patterning recesses in the substrate 104 and subsequently filling the recesses with such materials. For example, the recess may be epitaxially filled with silicon germanium, possibly by exposing the recesses to a precursor comprising germanium. The filled recesses are herein designated by the reference numeral 144. The depth of recessed source/drain region may range between about 5 nm and about 100 nm. Moreover, as in the illustrated embodiment, the recesses 144 may be filled to a height above the surface 106 of the substrate 104, such that the source/drain regions 136 may be raised source/drain regions. The height of raised source/drain regions may range between about 5 nm and about 100 nm."

Cheng817 ¶ [0022].

"In another embodiment, a semiconductor device constructed according to aspects of the present disclosure includes an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe. A second one of the NMOS and PMOS devices includes one of:

Exemplary Disclosures
(1) second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe; (2) second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and (3) second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe." Cheng817 ¶ [0036]. "In FIG. 3f, raised source and drain regions 320a are formed or built-up in the recesses 318a. For example, the source and drain regions 320a may be formed by selective epitaxial growth (SEG), CVD, PECVD, PVD, PDL, ALD, spin-on formation, and/or other techniques. The source and drain regions 320a may include materials such as amorphous silicon, polysilicon, strained silicon, germanium, silicon germanium, silicon carbide, and/or other materials." Cheng817 ¶ [0044]. "In FIG. 4e, the photoresist 417b is removed, and doped source and drain regions 420a are formed or built-up in the recessed regions 418a. The doped source and drain regions 420a may be formed by selective epitaxial growth (SEG), CVD, PECVD, PVD, PDL, ALD, spin-on formation, and/or other techniques now know or to be developed. The doped source and drain regions 420a may include materials such as amorphous silicon, polysilicon, strained silicon, germanium, silicon germanium, silicon carbide, and/or other materials. Low temperature processing, such as using a temperature less than 700° C., to form the doped regions 420a is preferred to reduce lightly doped drain diffusion." Cheng817 ¶ [0065]. "In FIG. 5e, the photoresist 517b is removed from the device 501b and source and drain regions 520a are built-up in the recessed regions 518a, preferably using a low temperature process to reduce LDD diffusion. The source and drain regions 520a may be formed by, for example, selective epitaxial growth (SEG), CVD, PECVD, PVD, PDL, ALD, spin-on formation, and/or other suitable techniques now know or later developed. The source and drain regions 520a may include materials such as amorphous silicon, polysilicon, strained silicon, germanium, silicon germanium, silicon carbide, and/or other materials. The source and drain regions 520a may also be doped "in-situ" during the SEG process, for example. In this process, dopants such as boron, phosphorous, arsenic, germanium, carbon, and/or other semiconductor materials may be introduced during the SEG process. The dopants may be introduced in gaseous form, which may include diborane (B_2H_6), Arsine (AsH_3), phosphine (PH_3), germane (GeH_4), phosphoryl chloride ($POCL_3$), boron bromide (BBr_3), hydrocarbons, and/or other gases/chemicals." Cheng817 ¶ [0080]. Additionally, under Plaintiff's apparent interpretation of the claim language, the claimed "silicon compound layer" may include a silicide film. See AICP's P.R. 3-1 Disclosures, Ex. H, at 15, 20,

Exemplary Disclosures
21, 25, 26, 31. Although TSMC disagrees with such an interpretation, Cheng817 further discloses [1f] under this interpretation, as shown below. "In FIG. 4i, the photoresist 421b is removed from the device 401b, and salicided contacts 432a and 432b are formed over the gate, source and drain of the devices 401a and 401b. The salicided contacts 432a and 432b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 732a and 732b may also include an anneal. The salicided contacts 732a and 732b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0069]. "Because the deeper doped source and drain regions were doped in-situ (FIG. 5g), a process of source and drain implantation such as that shown in FIG. 4h is not required. Therefore, salicided contacts 532a and 532b are formed for the gate, source and drains of the devices 501a and 501b, respectively, as shown in FIG. 5h. The salicided contacts 532a and 532b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 532a and 532b may also include an anneal. The salicided contacts 532a and 532b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0083]. *See also, e.g.,* Cheng817, ¶¶ [0002]-[0003], ¶¶ [0022]-[0023], ¶ [0033]-[0037], ¶ [0044], ¶ [0046], ¶ [0052], ¶ [0056], ¶ [0060], ¶¶ [0063]-[0065], ¶¶ [0068]-[0069], ¶ [0072], ¶ [0075], ¶¶ [0079]-[0080], ¶ [0083], ¶¶ [0093]-[0094], ¶ [0101], FIGS. 1, 2, 3e-3n, 4d-4j, 5d-5i, 6d-6i, 7. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

Exemplary Disclosures
1[g] a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and
Cheng817 discloses this feature. For example, Cheng817 discloses an etch stop layer 430a/430b (e.g., a SiN layer) which is formed on the PMOS active region to cover PMOS gate electrode 408a, L-shaped spacers 412a, 414a, spacers 415a, and PMOS epitaxial source/drain regions 420a. Etch stop layer 430a/430b causes a tensile stress opposite to the compressive stress caused by PMOS epitaxial SiGe source/drain regions 420a. *See, e.g.*, the following:  Cheng817 Fig. 4j (showing etch stop layer 430a/430b formed on the PMOS active region to cover PMOS gate electrode 408a, L-shaped spacers 412a, 414a, spacers 415a, and PMOS epitaxial source/drain regions 420a).  Cheng817 Fig. 5i (showing etch stop layer 530a/530b formed on the PMOS active region to cover PMOS gate electrode 508a, L-shaped spacers 512a, 514a, spacers 515a, and PMOS epitaxial source/drain regions 520a).

Exemplary Disclosures

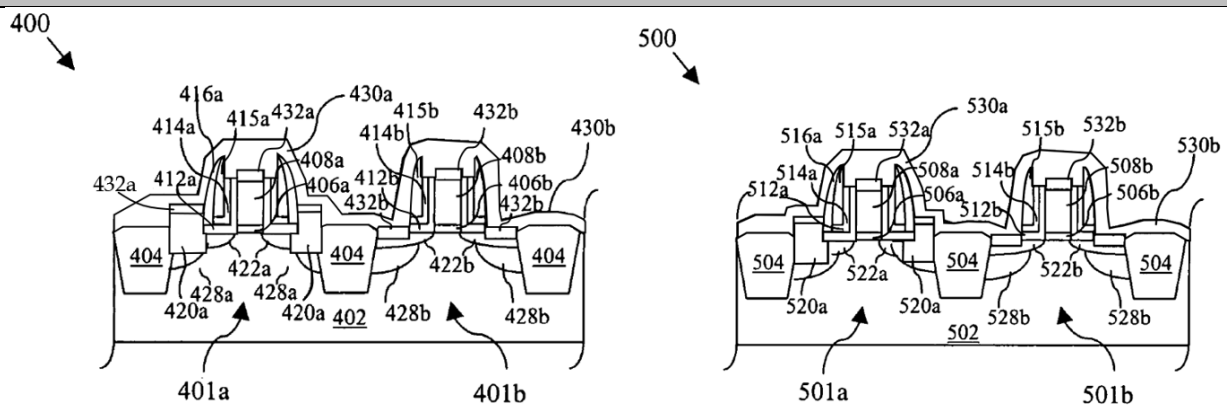


Figure A **Figure B**

(Cheng817, Figs. 4j, 5i (corrected))

"Increasing tensile or compressive stress in a semiconductor device substrate can improve drive current. For example, increasing the tensile stress in the substrate can improve the performance of n-channel metal-oxide-semiconductor (NMOS) devices. Similarly, increasing the compressive stress in the substrate can improve the performance of p-channel metal-oxide-semiconductor (PMOS) devices."

Cheng817 ¶ [0002].

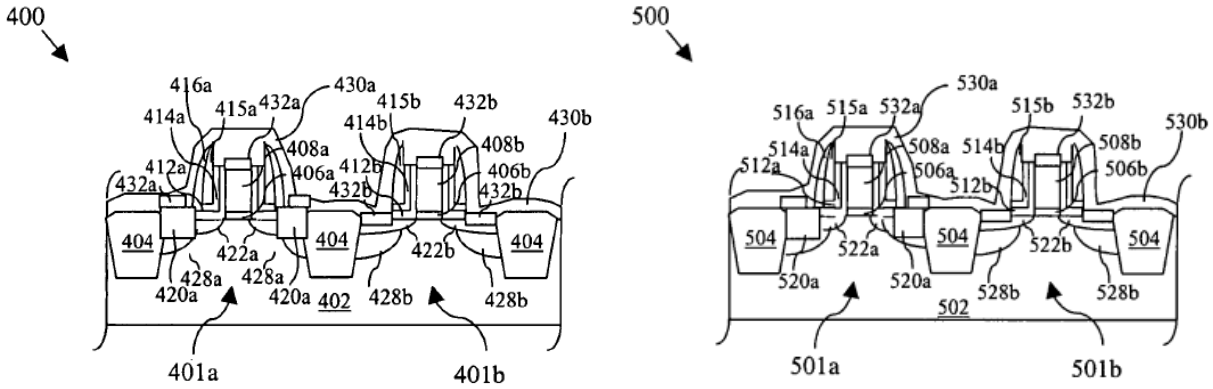
"Some applications have realized limited localized stress tuning by employing different materials for adjacent shallow trench isolation (STI) regions and other isolation structures. Stress tuning can also be accomplished by employing different materials for silicide and other contact layers. Etch stop layers remaining in the device structure after being employed as etching endpoints have also been employed for substrate stress tuning."

Cheng817 ¶ [0003].

"The semiconductor device 100 may also include an etch stop layer 180. The etch stop layer 180 may comprise silicon nitride (e.g., Si3N4), silicon oxynitride (e.g., SiON), silicon carbide, silicon dioxide and/or other materials, and may be formed by blanket or selective deposition by CVD, PVD, thermal oxidation and/or other processes. The etch stop layer 180 may be a tensile or compressive film, wherein a stress level may range between about +0.01 and about +2 GPa for tensile film and between about −0.01 and about −2 GPa for compressive film. The tensile or compressive nature of the etch stop layer 180 may impart strain within the source/ drain regions 136, 176. Moreover, the strain induced in the source/drain region 136 by the etch stop layer 180 may be substantially different in magnitude that the strain induced in the source/drain region 176 by the etch stop layer 180. For example, the strain induced in the source/ drain regions 136, 176 may vary by 10-20% in magnitude. In one embodiment, the strain induced in the source/drain regions 136 may be tensile and the strain induced in the source/drain regions 176 may be compressive. In another embodiment, the strain induced in the source/drain

Exemplary Disclosures
regions 136 may be compressive and the strain induced in the source/drain regions 176 may be tensile. The thickness of etch stop layer 180 may range between about 5 nm and about 200 nm." Cheng817 ¶ [0030]. "Further in FIG. 4j, an etch stop layer 430a and 430b are formed over the semiconductor device(s) 401a and 401b. The etch stop layer 430a and 430b may include silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), and/or other materials. In one embodiment, the etch stop layer 430a and 430b may be substantially similar in composition to the etch stop layer 180 described above. Alternatively, the etch stop layer 430a and 430b may include a stress level that may range between about +0.001 and about +50 GPa for tensile film and between about −0.001 and about −50 GPa for compressive film. The etch stop layer 430a and 430b may be formed by CVD, ALD, PECVD, PDL, spin-on coating, and/or other techniques." Cheng817 ¶ [0070]. "In FIG. 5i, etch stop layer 530a and 530b are formed over the semiconductor devices 501a and 501b. The etch stop layer 530a and 530b may include silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), and/or other materials. Alternatively, the etch stop layer 530a and 530b may include a stress level that may range between about +0.001 and about +50 GPa for tensile film and between about −0.001 and about −50 GPa for compressive film. The etch stop layer 530a-b may be formed by CVD, ALD, PECVD, PDL, spin-on coating, and/or other techniques." Cheng817 ¶ [0084]. Additionally, under Plaintiff's apparent interpretation of the claim language, the claimed "first gate electrode" may include a silicide film. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 11-13, 18, 20, 22, 24-25, 26, 39. Although TSMC does not necessarily agree with such an interpretation, Cheng817 further discloses this element under this interpretation, as shown below. For example, Cheng817 discloses silicide 432a formed on PMOS gate electrode 408a. *See, e.g.*, the following:

Exemplary Disclosures



Cheng817 Figs. 4j, 5i (showing silicides 432a and 532a on gate electrodes 408a and 508a).

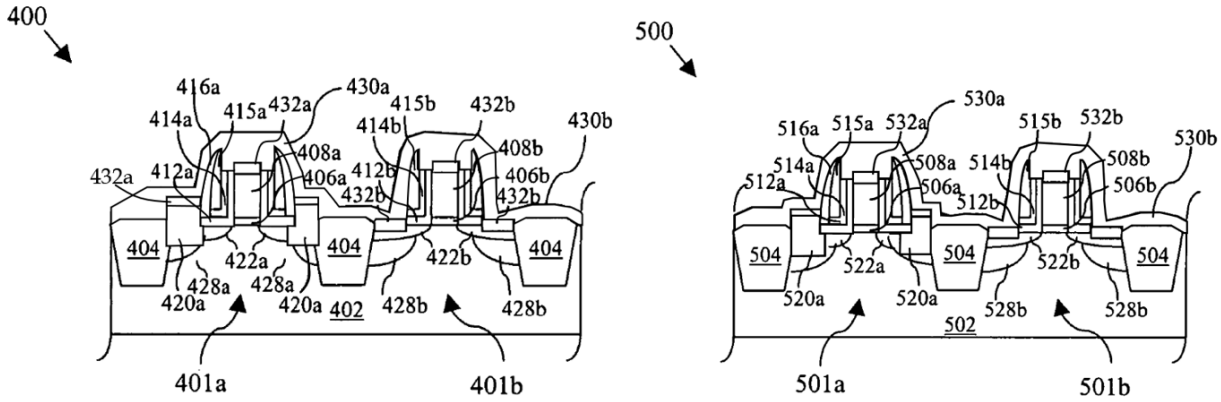


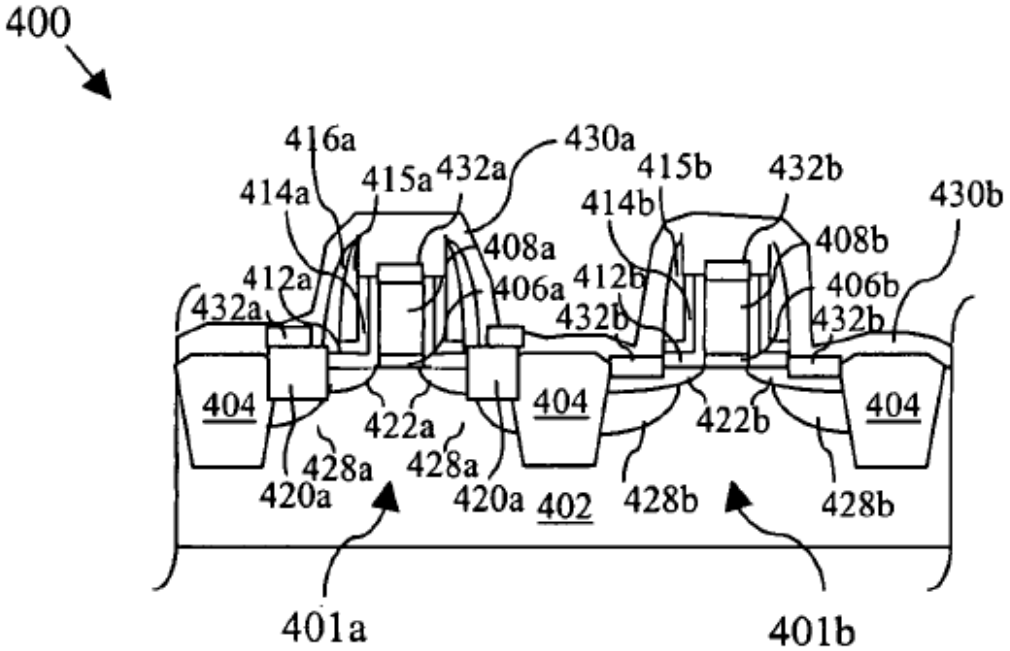
Figure A **Figure B**

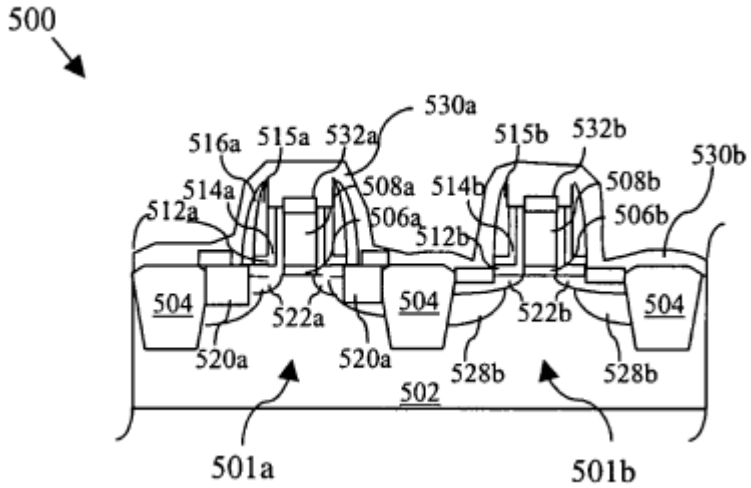
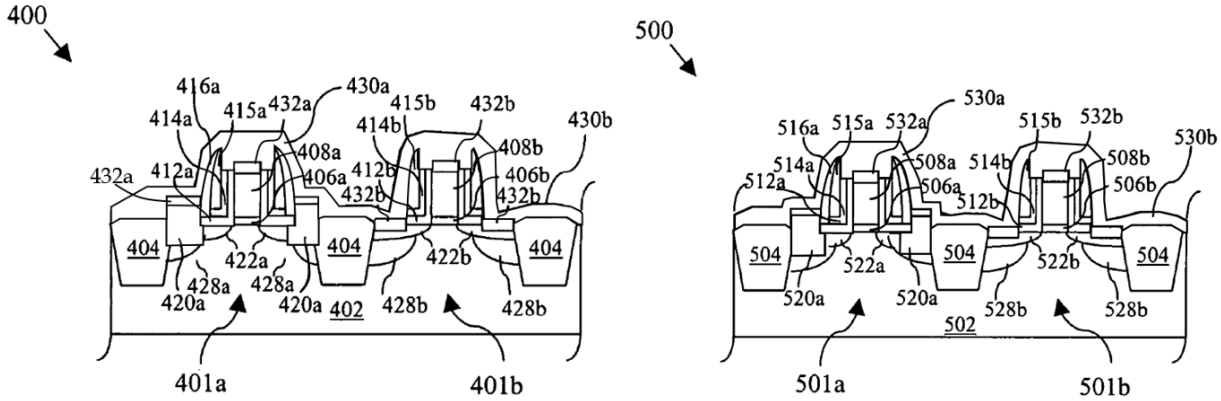
(Cheng817, Figs. 4j, 5i (corrected))

"In FIG. 4i, the photoresist 421b is removed from the device 401b, and salicided contacts 432a and 432b are formed over the gate, source and drain of the devices 401a and 401b. The salicided contacts 432a and 432b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 732a and 732b may also include an anneal. The salicided contacts 732a and 732b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques."

Cheng817 ¶ [0069].

"Because the deeper doped source and drain regions were doped in-situ (FIG. 5g), a process of source and drain implantation such as that shown in FIG. 4h is not required. Therefore, salicided contacts 532a and 532b are formed for the gate, source and drains of the devices 501a and 501b, respectively, as shown in FIG. 5h. The salicided contacts 532a and 532b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel

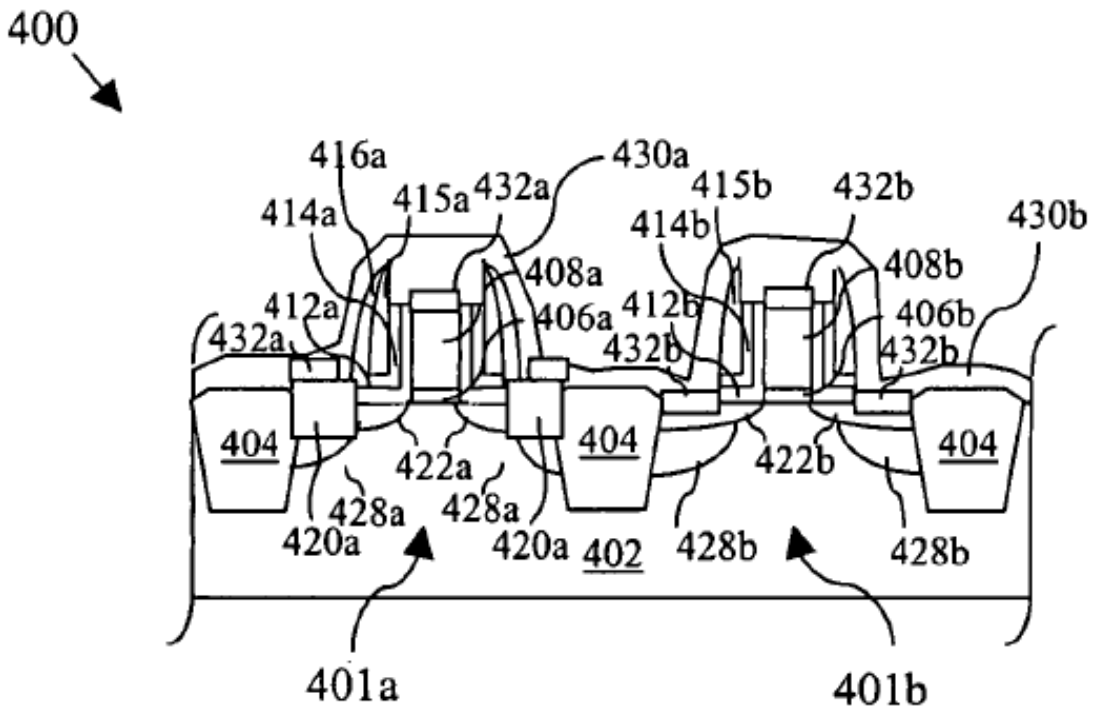
Exemplary Disclosures
silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 532a and 532b may also include an anneal. The salicided contacts 532a and 532b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0083]. *See also, e.g.,* Cheng817 ¶ [0003], ¶ [0019], ¶ [0041], ¶ [0052], ¶ [0058], ¶ [0069], ¶ [0073], ¶ [0083], ¶ [0087], ¶ [0097], ¶ [0099], ¶ [0101], FIGS. 1, 2, 3n, 4i-4j, 5h-5i, 6h-6i, 7. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
1[h] which causes a second stress opposite to the first stress,
Cheng817 discloses this feature. *See, e.g.*, *supra* 1[g]. *See, e.g.*, the following:    Cheng817 Fig. 4j (showing etch stop layer 430a/430b formed on the PMOS active region to cover PMOS gate electrode 408a, L-shaped spacers 412a, 414a, spacers 415a, and PMOS epitaxial source/drain regions 420a).

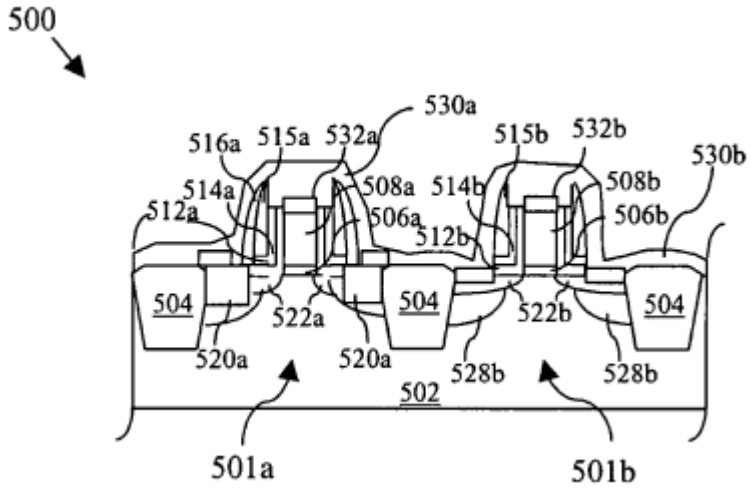
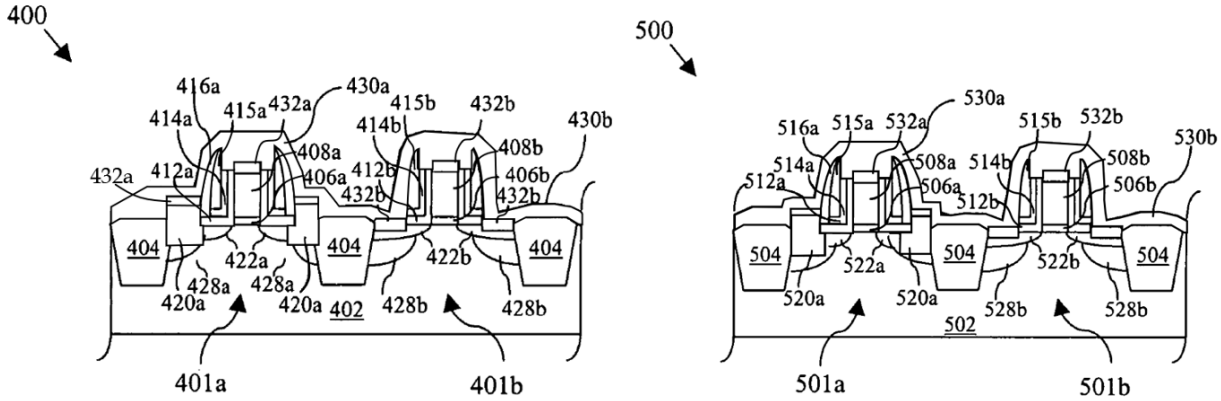
Exemplary Disclosures
 Cheng817 Fig. 5i (showing etch stop layer 530a/530b formed on the PMOS active region to cover PMOS gate electrode 508a, L-shaped spacers 512a, 514a, spacers 515a, and PMOS epitaxial source/drain regions 520a).  **Figure A** **Figure B** **(Cheng817, Figs. 4j, 5i (corrected))**

"Increasing tensile or compressive stress in a semiconductor device substrate can improve drive current. For example, increasing the tensile stress in the substrate can improve the performance of n-channel metal-oxide-semiconductor (NMOS) devices. Similarly, increasing the compressive stress in the substrate can improve the performance of p-channel metal-oxide-semiconductor (PMOS) devices."

Cheng817 ¶ [0002].

Exemplary Disclosures
"Some applications have realized limited localized stress tuning by employing different materials for adjacent shallow trench isolation (STI) regions and other isolation structures. Stress tuning can also be accomplished by employing different materials for silicide and other contact layers. Etch stop layers remaining in the device structure after being employed as etching endpoints have also been employed for substrate stress tuning." Cheng817 ¶ [0003]. "The semiconductor device 100 may also include an etch stop layer 180. The etch stop layer 180 may comprise silicon nitride (e.g., Si3N4), silicon oxynitride (e.g., SiON), silicon carbide, silicon dioxide and/or other materials, and may be formed by blanket or selective deposition by CVD, PVD, thermal oxidation and/or other processes. The etch stop layer 180 may be a tensile or compressive film, wherein a stress level may range between about +0.01 and about +2 GPa for tensile film and between about −0.01 and about −2 GPa for compressive film. The tensile or compressive nature of the etch stop layer 180 may impart strain within the source/ drain regions 136, 176. Moreover, the strain induced in the source/drain region 136 by the etch stop layer 180 may be substantially different in magnitude that the strain induced in the source/drain region 176 by the etch stop layer 180. For example, the strain induced in the source/ drain regions 136, 176 may vary by 10-20% in magnitude. In one embodiment, the strain induced in the source/drain regions 136 may be tensile and the strain induced in the source/drain regions 176 may be compressive. In another embodiment, the strain induced in the source/drain regions 136 may be compressive and the strain induced in the source/drain regions 176 may be tensile. The thickness of etch stop layer 180 may range between about 5 nm and about 200 nm." Cheng817 ¶ [0030]. "Further in FIG. 4j, an etch stop layer 430a and 430b are formed over the semiconductor device(s) 401a and 401b. The etch stop layer 430a and 430b may include silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), and/or other materials. In one embodiment, the etch stop layer 430a and 430b may be substantially similar in composition to the etch stop layer 180 described above. Alternatively, the etch stop layer 430a and 430b may include a stress level that may range between about +0.001 and about +50 GPa for tensile film and between about −0.001 and about −50 GPa for compressive film. The etch stop layer 430a and 430b may be formed by CVD, ALD, PECVD, PDL, spin-on coating, and/or other techniques." Cheng817 ¶ [0070]. "In FIG. 5i, etch stop layer 530a and 530b are formed over the semiconductor devices 501a and 501b. The etch stop layer 530a and 530b may include silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), and/or other materials. Alternatively, the etch stop layer 530a and 530b may include a stress level that may range between about +0.001 and about +50 GPa for tensile film and between about −0.001 and about −50 GPa for compressive film. The etch stop

Exemplary Disclosures
layer 530a-b may be formed by CVD, ALD, PECVD, PDL, spin-on coating, and/or other techniques." Cheng817 ¶ [0084]. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
1[i] an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode,
Cheng817 discloses this feature. For example, the uppermost surface of PMOS epitaxial source/drain regions 420a is located higher than a surface of semiconductor substrate 402 located directly under PMOS gate electrode 408a. *See, e.g.*, the following:    Cheng817 Fig. 4j (showing the uppermost surface of PMOS epitaxial source/drain regions 420a is located higher than a surface of semiconductor substrate 402 located directly under PMOS gate electrode 408a).

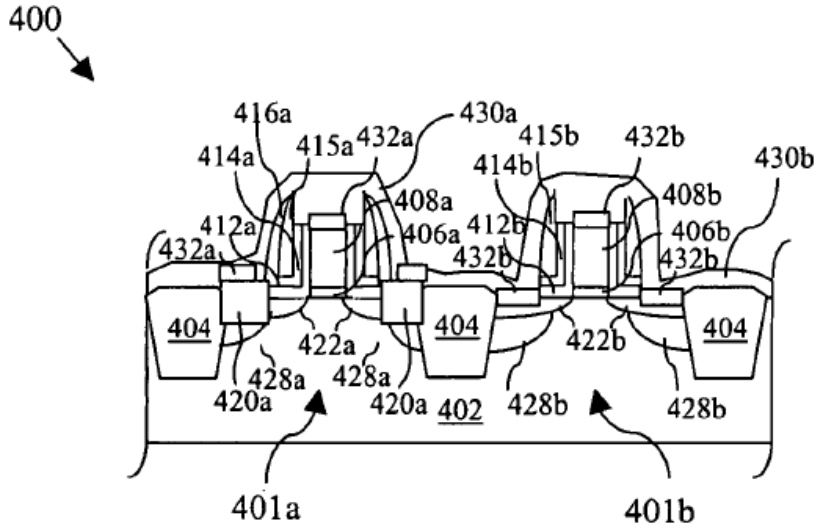
Exemplary Disclosures
 Cheng817 Fig. 5i (showing the uppermost surface of PMOS epitaxial source/drain regions 520a is located higher than a surface of semiconductor substrate 502 located directly under PMOS gate electrode 508a).  **Figure A** **Figure B** **(Cheng817, Figs. 4j, 5i (corrected))** "A method comprises forming a first semiconductor device in a substrate, where the first semiconductor device comprises a gate structure, a spacer disposed on sidewalls of the gate structure, the spacer having a first thickness, and raised source and drain regions disposed on either side of the gate structure. The method further comprises forming a second semiconductor device in the substrate and electrically isolated from the first semiconductor device, where the second semiconductor device comprises a gate structure, a spacer disposed on sidewalls of the gate structure, the spacer having a second thickness less than the first thickness of the spacer of the first semiconductor device, and recessed source and drain regions disposed on either side of the gate structure." Cheng817 Abstract.

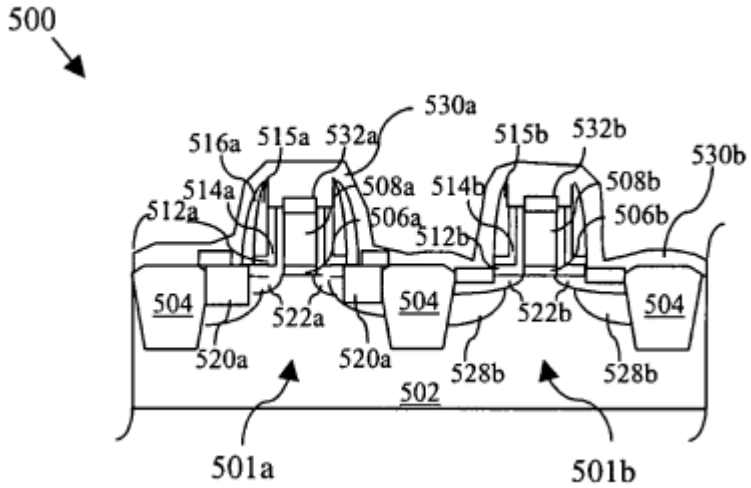
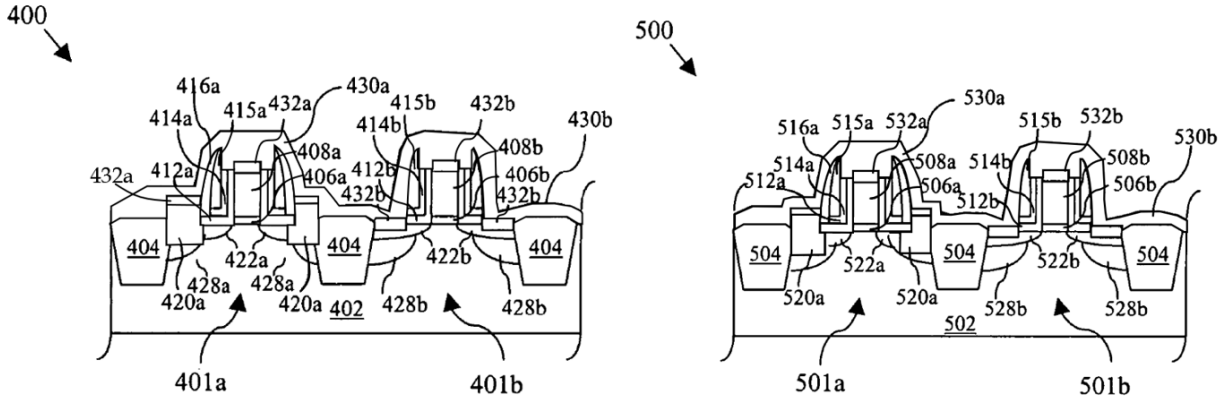
Exemplary Disclosures
"The gate dielectric layer 120 may be formed by thermal oxidation, atomic layer deposition (ALD), chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma enhanced CVD (PECVD) and/or other processes. Moreover, although not limited by the scope of the present disclosure, the gate dielectric layer 120 may comprise silicon oxide, silicon oxynitride, or a high-k dielectric, such as hafnium oxide, zirconium oxide, aluminum oxide, a hafnium dioxide-alumina (HfO2-Al2O3) alloy, and/or combinations thereof. The gate dielectric layer may have a thickness ranging between about 0.5 nm and about 10 nm." Cheng817 ¶ [0018]. "The spacers 132 may be formed by CVD, PVD, thermal oxidation and/or other processes, and may comprise one or more dielectric materials such as silicon nitride, silicon oxide, silicon carbide, silicon oxynitride and/or combinations thereof. The spacers 132 may each have a width W_P extending from the gate electrode 124. The width of spacers 132 may range between about 5 nm and about 100 nm." Cheng817 ¶ [0020]. "The source/drain regions 136 may be of conventional composition and fabrication. For example, the source/drain regions 136 may comprise doped portions of the substrate 104 which may be formed by ion implantation of boron, boron difluoride (BF2), or other dopants, and/or in-situ doped of boron or other dopants. In such embodiments, the source/drain regions 136 may be substantially coplanar with the surface 106 of the substrate 104. However, as in the illustrated embodiment, the source/drain regions 136 may extend above the substrate surface 106. In such embodiments, the source/drain regions 136 may comprise silicon, silicon germanium, silicon carbide, gallium arsenide and/or other materials, and may be formed by dry etching or otherwise patterning recesses in the substrate 104 and subsequently filling the recesses with such materials. For example, the recess may be epitaxially filled with silicon germanium, possibly by exposing the recesses to a precursor comprising germanium. The filled recesses are herein designated by the reference numeral 144. The depth of recessed source/drain region may range between about 5 nm and about 100 nm. Moreover, as in the illustrated embodiment, the recesses 144 may be filled to a height above the surface 106 of the substrate 104, such that the source/drain regions 136 may be raised source/drain regions. The height of raised source/drain regions may range between about 5 nm and about 100 nm." Cheng817 ¶ [0022]. "In one embodiment, the source/drain regions 136 may be recessed source/drain regions and the source/drain regions 176 may be raised source/drain regions, in contrast to the illustrated embodiment. In another embodiment, the source/drain regions 136 may be recessed source/drain regions and the source/drain regions 176 may be coplanar with the substrate 104. In another embodiment, the source/drain regions 136 may be raised source/drain regions and the source/drain regions 176 may be coplanar with the substrate 104. In another embodiment, the source/drain regions 176 may be recessed source/drain regions and the source/drain regions 136 may be coplanar with the substrate 104. In another embodiment, the source/drain regions 176 may be raised source/drain regions and the source/drain regions 136 may be coplanar with the substrate 104." Cheng817 ¶ [0029].

Exemplary Disclosures
"Thus, the present disclosure introduces a semiconductor device including, in one embodiment, an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface; and (2) first source/drain regions extending from the surface. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface." Cheng817 ¶ [0033]. "In another embodiment, semiconductor device constructed according to aspects of the present disclosure comprises an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface. A second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different." Cheng817 ¶ [0034]. "Another embodiment of a semiconductor device constructed according to aspects of the present disclosure includes an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; (2) a first gate interposing the first source/drain regions; and (3) first spacers on opposing sides of the first gate and each extending from the first gate to a first width. A second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; (2) a second gate interposing the second source/drain regions; and (3) second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different." Cheng817 ¶ [0035].

Exemplary Disclosures
"In another embodiment, a semiconductor device constructed according to aspects of the present disclosure includes an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe; (2) second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and (3) second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe." Cheng817 ¶ [0036]. "The present disclosure also introduces a method of manufacturing semiconductor device. In one embodiment, the method includes forming an isolation region located in a substrate, forming an NMOS device located partially over a surface of the substrate, and forming a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface; and (2) first source/drain regions extending from the surface. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface." Cheng817 ¶ [0037]. "In FIG. 3f, raised source and drain regions 320a are formed or built-up in the recesses 318a. For example, the source and drain regions 320a may be formed by selective epitaxial growth (SEG), CVD, PECVD, PVD, PDL, ALD, spin-on formation, and/or other techniques. The source and drain regions 320a may include materials such as amorphous silicon, polysilicon, strained silicon, germanium, silicon germanium, silicon carbide, and/or other materials." Cheng817 ¶ [0044]. "As shown in FIG. 3n, the semiconductor device 301a, a P-type MOS device, comprises raised source and drain regions, and the semiconductor device 301b, an N-type MOS device, comprises recessed source and drain regions." Cheng817 ¶ [0054].

Exemplary Disclosures
"In FIG. 4e, the photoresist 417b is removed, and doped source and drain regions 420a are formed or built-up in the recessed regions 418a. The doped source and drain regions 420a may be formed by selective epitaxial growth (SEG), CVD, PECVD, PVD, PDL, ALD, spin-on formation, and/or other techniques now know or to be developed. The doped source and drain regions 420a may include materials such as amorphous silicon, polysilicon, strained silicon, germanium, silicon germanium, silicon carbide, and/or other materials. Low temperature processing, such as using a temperature less than 700° C., to form the doped regions 420a is preferred to reduce lightly doped drain diffusion." Cheng817 ¶ [0065]. "In FIG. 5e, the photoresist 517b is removed from the device 501b and source and drain regions 520a are built-up in the recessed regions 518a, preferably using a low temperature process to reduce LDD diffusion. The source and drain regions 520a may be formed by, for example, selective epitaxial growth (SEG), CVD, PECVD, PVD, PDL, ALD, spin-on formation, and/or other suitable techniques now know or later developed. The source and drain regions 520a may include materials such as amorphous silicon, polysilicon, strained silicon, germanium, silicon germanium, silicon carbide, and/or other materials. The source and drain regions 520a may also be doped "in-situ" during the SEG process, for example. In this process, dopants such as boron, phosphorous, arsenic, germanium, carbon, and/or other semiconductor materials may be introduced during the SEG process. The dopants may be introduced in gaseous form, which may include diborane (B_2H_6), Arsine (AsH_3), phosphine (PH_3), germane (GeH_4), phosphoryl chloride ($POCL_3$), boron bromide (BBr_3), hydrocarbons, and/or other gases/chemicals." Cheng817 ¶ [0080]. Alternatively, under Plaintiff's apparent interpretation of the claim language, the claimed "silicon compound layer" may include a silicide film. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 15, 20, 21, 25, 26, 31. Although TSMC disagrees with such an interpretation, Cheng817 further discloses [1i] under this interpretation, as shown below. "In FIG. 4i, the photoresist 421b is removed from the device 401b, and salicided contacts 432a and 432b are formed over the gate, source and drain of the devices 401a and 401b. The salicided contacts 432a and 432b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 732a and 732b may also include an anneal. The salicided contacts 732a and 732b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0069].

Exemplary Disclosures
"Because the deeper doped source and drain regions were doped in-situ (FIG. 5g), a process of source and drain implantation such as that shown in FIG. 4h is not required. Therefore, salicided contacts 532a and 532b are formed for the gate, source and drains of the devices 501a and 501b, respectively, as shown in FIG. 5h. The salicided contacts 532a and 532b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 532a and 532b may also include an anneal. The salicided contacts 532a and 532b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0083]. *See also, e.g.,* Cheng817 ¶ [0003], ¶ [0019], ¶ [0021], ¶ [0041], ¶ [0052], ¶ [0058], ¶ [0069], ¶ [0073], ¶ [0083], ¶ [0087], ¶ [0097], ¶ [0099], ¶ [0101], FIGS. 1, 2, 3n, 4i-4j, 5h-5i, 6h-6i, 7. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
1[j] a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer,
Cheng817 discloses this feature. For example, Cheng817 discloses dummy spacer 416a is formed in a space between PMOS epitaxial source/drain region 420a and the L-shaped spacers 412a, 414a and spacers 415a. *See, e.g.*, the following:    Cheng817 Fig. 4j (showing dummy spacer 416a is formed in a space between PMOS epitaxial source/drain region 420a and the L-shaped spacers 412a, 414a and spacers 415a).

Exemplary Disclosures
 Cheng817 Fig. 5i (showing dummy spacer 516a is formed in a space between PMOS epitaxial source/drain region 520a and the L-shaped spacers 512a, 514a and spacers 515a).  **Figure A** **Figure B** **(Cheng817, Figs. 4j, 5i (corrected))** "In FIG. 4b, sidewall dielectric layers 412 and 414, and spacer material 415 are disposed over the semiconductor device(s) 410a and 401b and are subsequently processed, such as by etching, to form sidewall dielectric structures 412a, 412b, 414a and 414b, and spacers 415a and 415b, as shown in FIG. 4c. Note the dielectric structures 714a and 714b are substantially L-shaped. A dummy spacer layer 416 is formed over the semiconductor devices 401a and 401b. Low temperature processing, such as using a temperature less than 600° C., to form the sidewall dielectric and spacer materials is preferred to reduce lightly doped drain diffusion." Cheng817 ¶ [0061].

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"In FIG. 4d, the dummy spacer material 416 is processed to form the dummy spacers 416a and 416b. The dummy spacer material 416 may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), silicon oxy-carbide (SiOC), polymer, and/or other materials. The spacer material 416 may be formed by CVD, PECVD, ALD, spin-on coating, and/or other processing techniques, for example, and the dummy spacers 416a and 416b may be formed by chemical etch, plasma etch, CMP, focused ion beam (FIB), and/or other processing techniques. In FIG. 4d, a photoresist 417b is provided over the device 401b so that portions of the dummy spacer material 416a is removed from the device 401a, and recessed source and drain regions 418a are also formed in the substrate 402 on either side of the gate structure of the device 401a." Cheng817 ¶ [0063]. "Further, a dummy spacer material 516 is formed over the semiconductor devices 501a and 501b, and subsequently processed forming the dummy spacers 516a and 516b. The dummy spacer material 516 may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), silicon oxy-carbide (SiOC), polymer, and/or other materials. The spacer material 516 may be formed by CVD, PECVD, ALD, spin-on coating, and/or other processing techniques, and may be formed by chemical etch, plasma etch, CMP, focused ion beam (FIB), and/or other processing techniques." Cheng817 ¶ [0078]. Additionally, under Plaintiff's apparent interpretation of the claim language, the claimed "silicon compound layer" may include a silicide film. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 15, 20, 21, 25, 26, 31. Although TSMC disagrees with such an interpretation, Cheng817 further discloses [1j] under this interpretation (and subject to the additional caveats noted above), as the image above demonstrates. "In FIG. 4i, the photoresist 421b is removed from the device 401b, and salicided contacts 432a and 432b are formed over the gate, source and drain of the devices 401a and 401b. The salicided contacts 432a and 432b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 732a and 732b may also include an anneal. The salicided contacts 732a and 732b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0069]. "Because the deeper doped source and drain regions were doped in-situ (FIG. 5g), a process of source and drain implantation such as that shown in FIG. 4h is not required. Therefore, salicided contacts 532a and 532b are formed for the gate, source and drains of the devices 501a and 501b, respectively, as shown in FIG. 5h. The salicided contacts 532a and 532b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided

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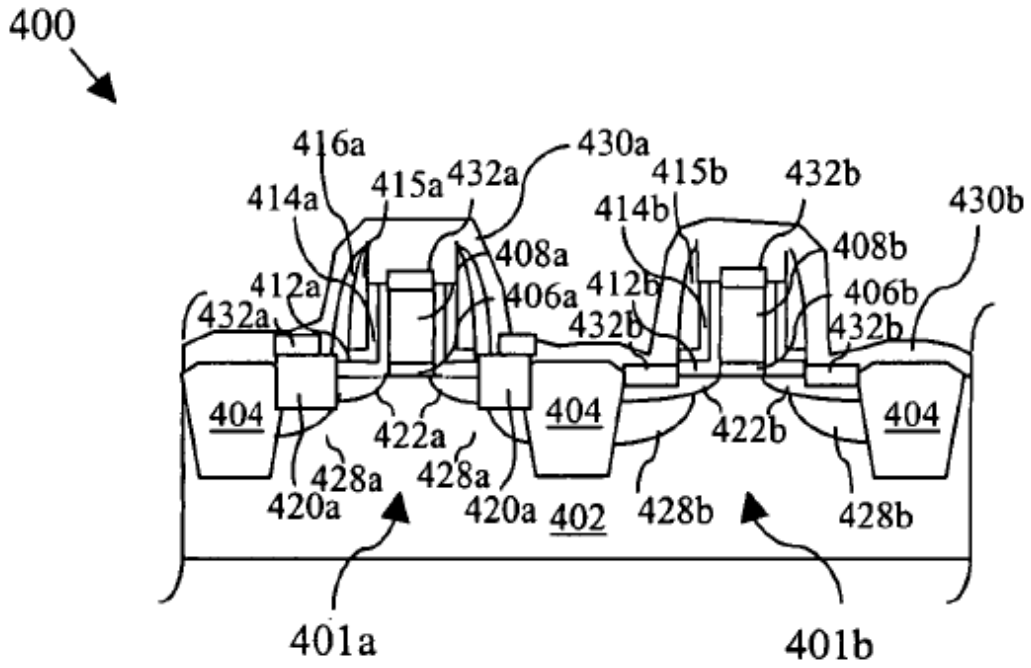
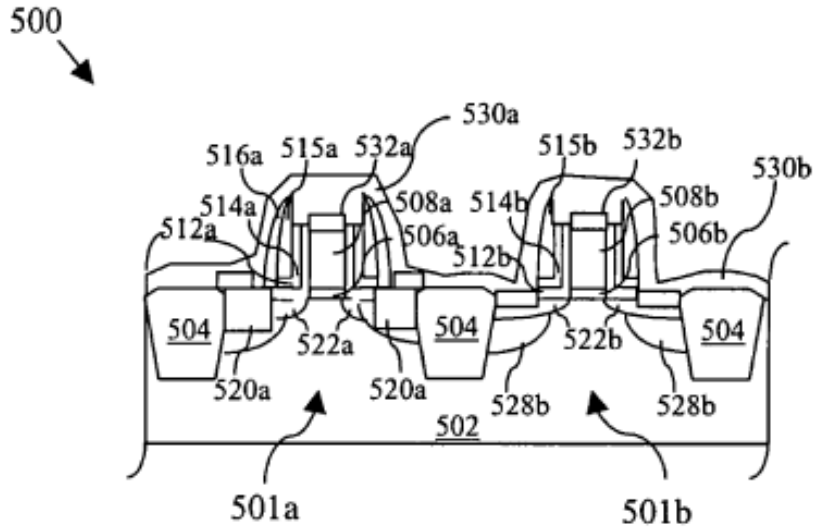
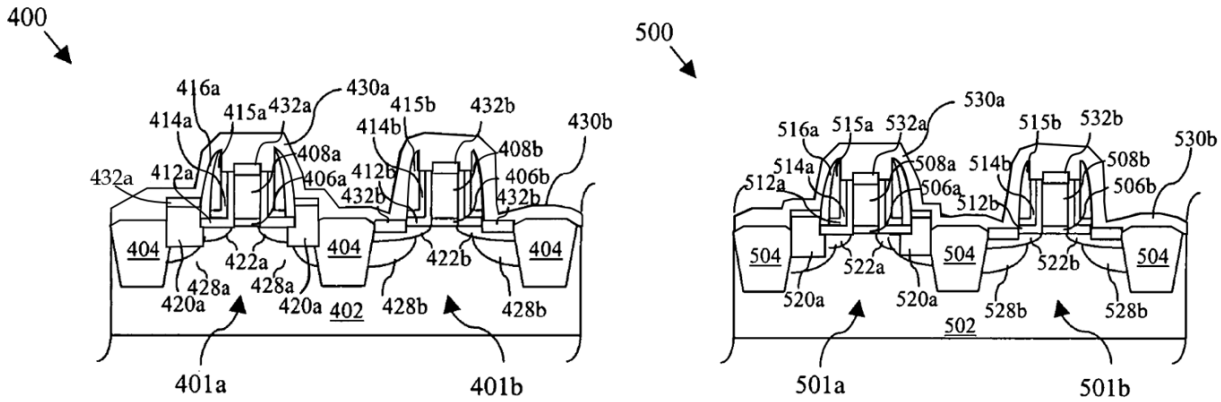
contacts 532a and 532b may also include an anneal. The salicided contacts 532a and 532b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0083]. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
1[k] the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween, and
Cheng817 discloses this feature. For example, Cheng 817 discloses that dummy spacer 416a is formed on the side surface of PMOS gate electrode 408a with the L-shaped spacers 412a, 414a and spacers 415a interposed therebetween. *See, e.g.*, the following:    Cheng817 Fig. 4j (showing dummy spacer 416a is formed on the side surface of PMOS gate electrode 408a with the L-shaped spacers 412a, 414a and spacers 415a interposed therebetween).

Exemplary Disclosures
 Cheng817 Fig. 5i (showing dummy spacer 516a is formed on the side surface of PMOS gate electrode 508a with the L-shaped spacers 512a, 514a and spacers 515a interposed therebetween).
 **Figure A** **Figure B** **(Cheng817, Figs. 4j, 5i (corrected))**
"The gate dielectric layer 120 may be formed by thermal oxidation, atomic layer deposition (ALD), chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma enhanced CVD (PECVD) and/or other processes. Moreover, although not limited by the scope of the present disclosure, the gate dielectric layer 120 may comprise silicon oxide, silicon oxynitride, or a high-k dielectric, such as hafnium oxide, zirconium oxide, aluminum oxide, a hafnium dioxide-alumina (HfO2-Al2O3) alloy, and/or combinations thereof. The gate dielectric layer may have a thickness ranging between about 0.5 nm and about 10 nm." Cheng817 ¶ [0018].

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"The spacers 132 may be formed by CVD, PVD, thermal oxidation and/or other processes, and may comprise one or more dielectric materials such as silicon nitride, silicon oxide, silicon carbide, silicon oxynitride and/or combinations thereof. The spacers 132 may each have a width W_P extending from the gate electrode 124. The width of spacers 132 may range between about 5 nm and about 100 nm." Cheng817 ¶ [0020]. "The source/drain regions 136 may be of conventional composition and fabrication. For example, the source/drain regions 136 may comprise doped portions of the substrate 104 which may be formed by ion implantation of boron, boron difluoride (BF2), or other dopants, and/or in-situ doped of boron or other dopants. In such embodiments, the source/drain regions 136 may be substantially coplanar with the surface 106 of the substrate 104. However, as in the illustrated embodiment, the source/drain regions 136 may extend above the substrate surface 106. In such embodiments, the source/drain regions 136 may comprise silicon, silicon germanium, silicon carbide, gallium arsenide and/or other materials, and may be formed by dry etching or otherwise patterning recesses in the substrate 104 and subsequently filling the recesses with such materials. For example, the recess may be epitaxially filled with silicon germanium, possibly by exposing the recesses to a precursor comprising germanium. The filled recesses are herein designated by the reference numeral 144. The depth of recessed source/drain region may range between about 5 nm and about 100 nm. Moreover, as in the illustrated embodiment, the recesses 144 may be filled to a height above the surface 106 of the substrate 104, such that the source/drain regions 136 may be raised source/drain regions. The height of raised source/drain regions may range between about 5 nm and about 100 nm." Cheng817 ¶ [0022]. "In FIG. 4b, sidewall dielectric layers 412 and 414, and spacer material 415 are disposed over the semiconductor device(s) 410a and 401b and are subsequently processed, such as by etching, to form sidewall dielectric structures 412a, 412b, 414a and 414b, and spacers 415a and 415b, as shown in FIG. 4c. Note the dielectric structures 714a and 714b are substantially L-shaped. A dummy spacer layer 416 is formed over the semiconductor devices 401a and 401b. Low temperature processing, such as using a temperature less than 600° C., to form the sidewall dielectric and spacer materials is preferred to reduce lightly doped drain diffusion." Cheng817 ¶ [0061]. "In FIG. 4d, the dummy spacer material 416 is processed to form the dummy spacers 416a and 416b. The dummy spacer material 416 may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), silicon oxy-carbide (SiOC), polymer, and/or other materials. The spacer material 416 may be formed by CVD, PECVD, ALD, spin-on coating, and/or other processing techniques, for example, and the dummy spacers 416a and 416b may be formed by chemical etch, plasma etch, CMP, focused ion beam (FIB), and/or other processing techniques. In FIG. 4d, a photoresist 417b is provided over the device 401b so that portions of the dummy

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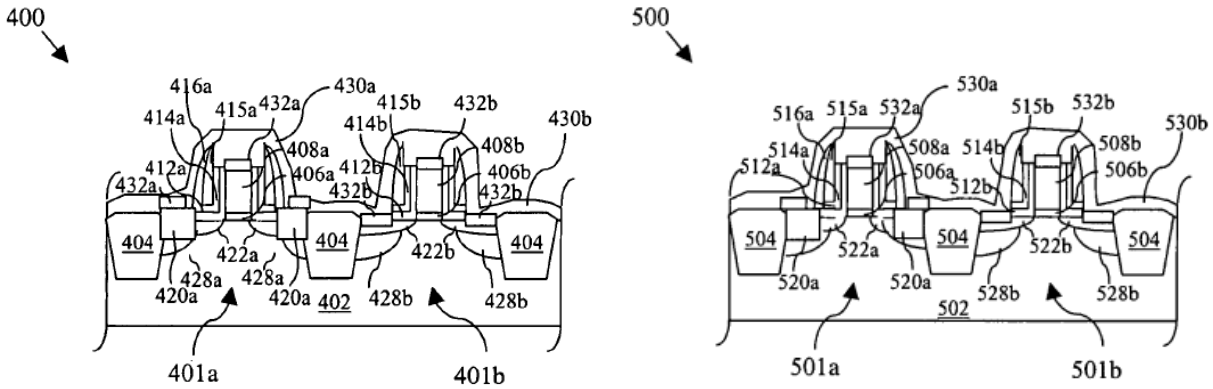
spacer material 416a is removed from the device 401a, and recessed source and drain regions 418a are also formed in the substrate 402 on either side of the gate structure of the device 401a." Cheng817 ¶ [0063]. "Further, a dummy spacer material 516 is formed over the semiconductor devices 501a and 501b, and subsequently processed forming the dummy spacers 516a and 516b. The dummy spacer material 516 may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), silicon oxy-carbide (SiOC), polymer, and/or other materials. The spacer material 516 may be formed by CVD, PECVD, ALD, spin-on coating, and/or other processing techniques, and may be formed by chemical etch, plasma etch, CMP, focused ion beam (FIB), and/or other processing techniques." Cheng817 ¶ [0078]. *See also*, *e.g.*, Cheng817, ¶ [0019], ¶ [0021], FIGS. 4c-4i. Additionally, under Plaintiff's apparent interpretation of the claim language, the claimed "first gate electrode" may include a silicide film. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 11-13, 18, 20, 22, 24-25, 26, 39. Although TSMC does not necessarily agree with such an interpretation, Cheng817 further discloses this element under this interpretation, as shown below. For example, Cheng817 discloses silicide 432a formed on PMOS gate electrode 408a. *See, e.g.*, the following:    Cheng817 Figs. 4j, 5i.(showing dummy spacers 416a and 516a is formed on the side surface of PMOS silicides 432a and 532a with the L-shaped spacers 412a/512a, 414a/514a and spacers 415a/515a interposed therebetween).

Exemplary Disclosures

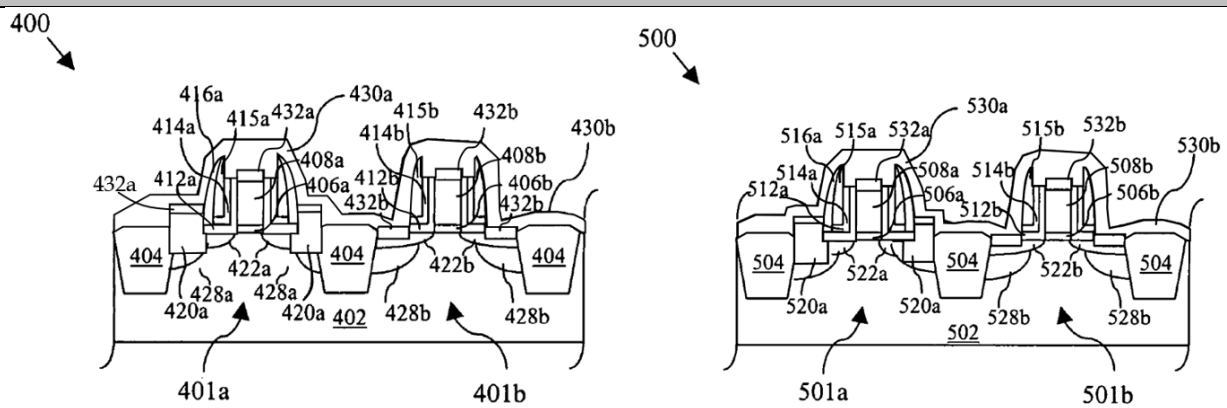


Figure A **Figure B**

(Cheng817, Figs. 4j, 5i (corrected))

"In FIG. 4i, the photoresist 421b is removed from the device 401b, and salicided contacts 432a and 432b are formed over the gate, source and drain of the devices 401a and 401b. The salicided contacts 432a and 432b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 732a and 732b may also include an anneal. The salicided contacts 732a and 732b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques."

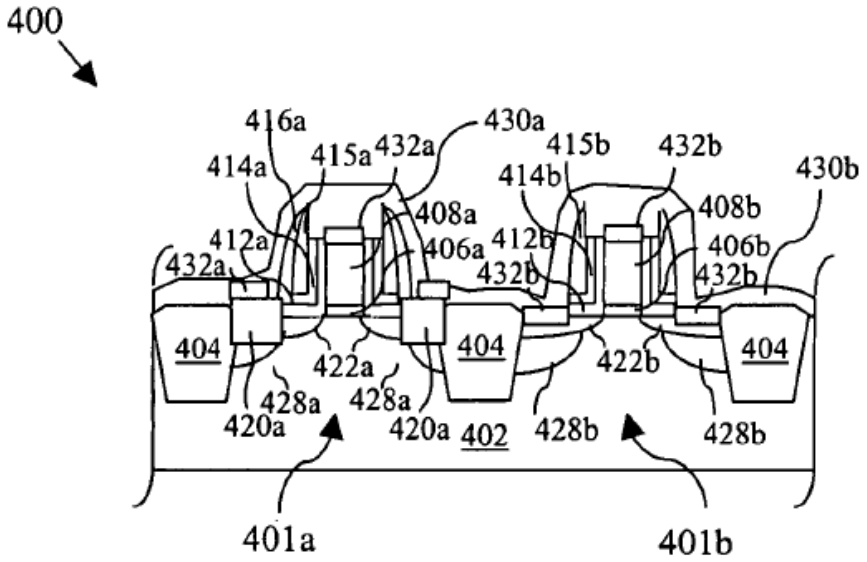
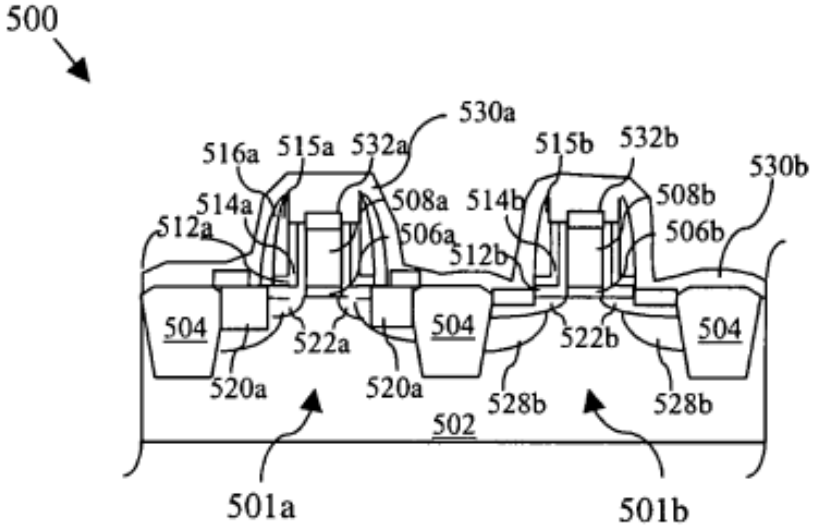
Cheng817 ¶ [0069].

"Because the deeper doped source and drain regions were doped in-situ (FIG. 5g), a process of source and drain implantation such as that shown in FIG. 4h is not required. Therefore, salicided contacts 532a and 532b are formed for the gate, source and drains of the devices 501a and 501b, respectively, as shown in FIG. 5h. The salicided contacts 532a and 532b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 532a and 532b may also include an anneal. The salicided contacts 532a and 532b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques."

Cheng817 ¶ [0083].

See also, e.g., Cheng817 ¶ [0003], ¶ [0019], ¶ [0041], ¶ [0052], ¶ [0058], ¶ [0069], ¶ [0073], ¶ [0083], ¶ [0087], ¶ [0097], ¶ [0099], ¶ [0101], FIGS. 1, 2, 3n, 4i-4j, 5h-5i, 6h-6i, 7.

To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

Exemplary Disclosures
1[l] the first stress-relief film is not in direct contact with the side surface of the first gate electrode.
Cheng817 discloses this feature. For example, Cheng817 discloses that dummy spacer 416a is not in direct contact with the side surface of PMOS gate electrode 408a. *See, e.g.*, the following:  Cheng817 Fig. 4j (showing dummy spacer 416a is not in direct contact with the side surface of PMOS gate electrode 408a).  Cheng817 Fig. 5i (showing dummy spacer 516a is not in direct contact with the side surface of PMOS gate electrode 508a).

Exemplary Disclosures

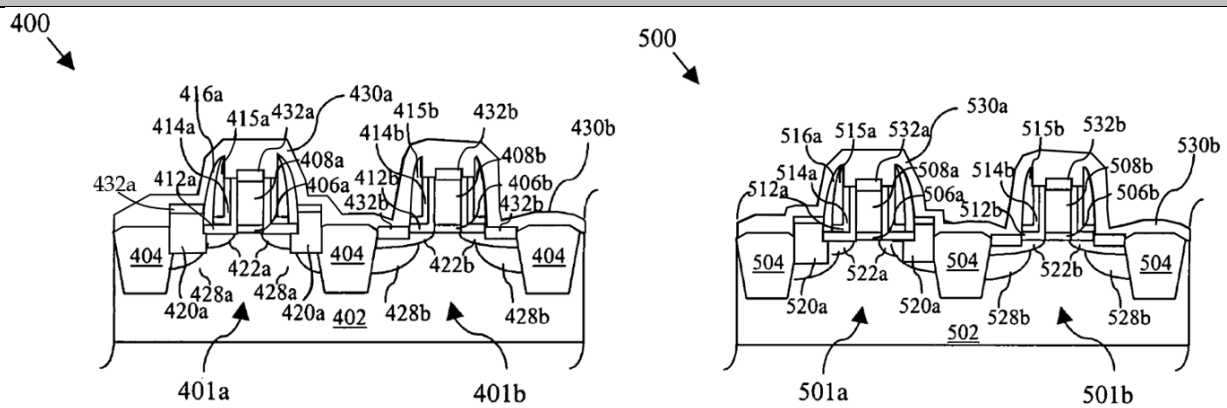


Figure A **Figure B**

(Cheng817, Figs. 4j, 5i (corrected))

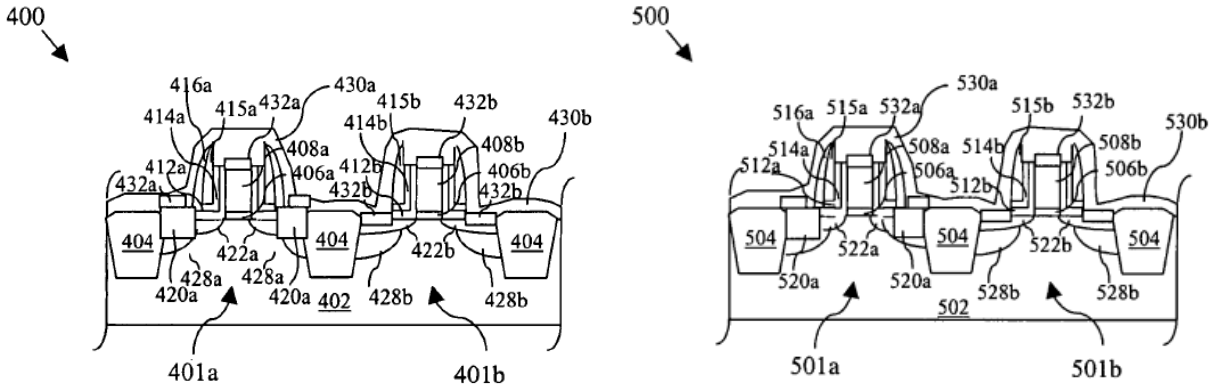
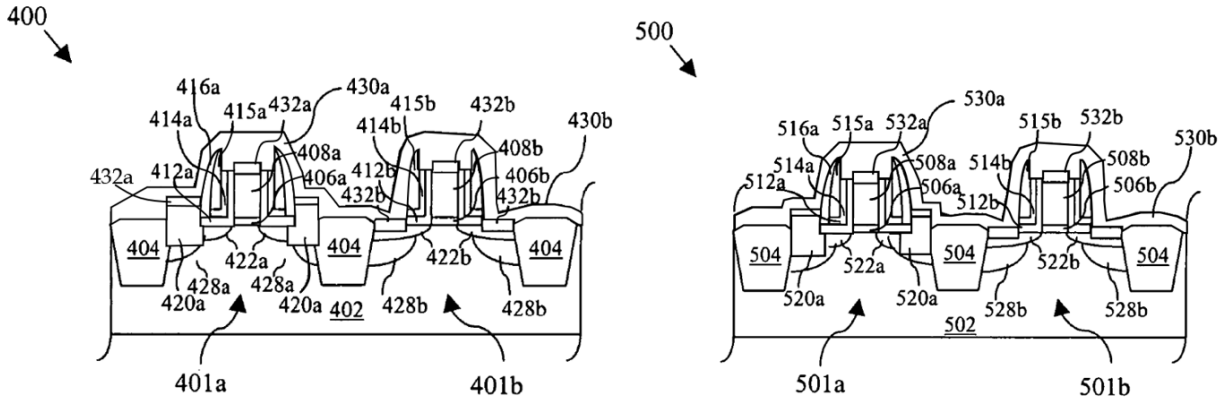
"In FIG. 4b, sidewall dielectric layers 412 and 414, and spacer material 415 are disposed over the semiconductor device(s) 410a and 401b and are subsequently processed, such as by etching, to form sidewall dielectric structures 412a, 412b, 414a and 414b, and spacers 415a and 415b, as shown in FIG. 4c. Note the dielectric structures 714a and 714b are substantially L-shaped. A dummy spacer layer 416 is formed over the semiconductor devices 401a and 401b. Low temperature processing, such as using a temperature less than 600° C., to form the sidewall dielectric and spacer materials is preferred to reduce lightly doped drain diffusion."

Cheng817 ¶ [0061].

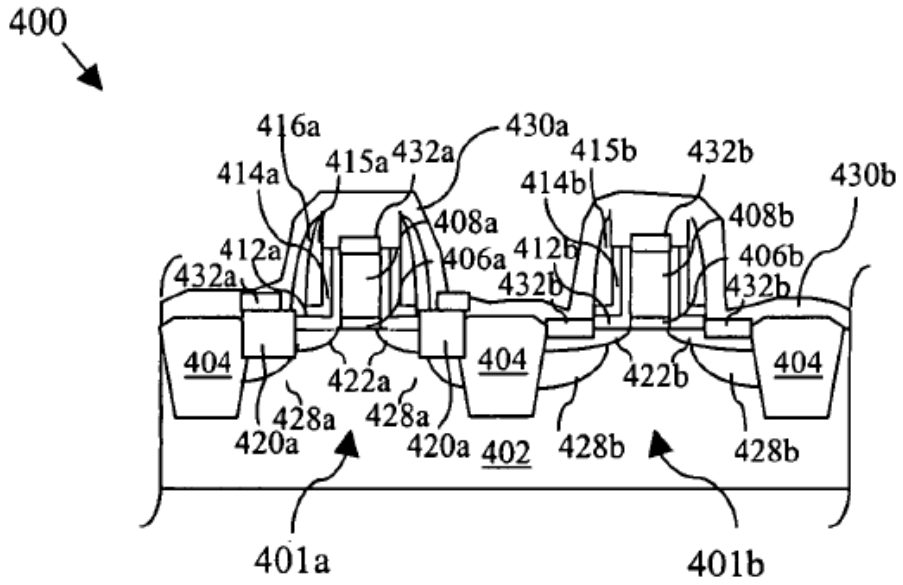
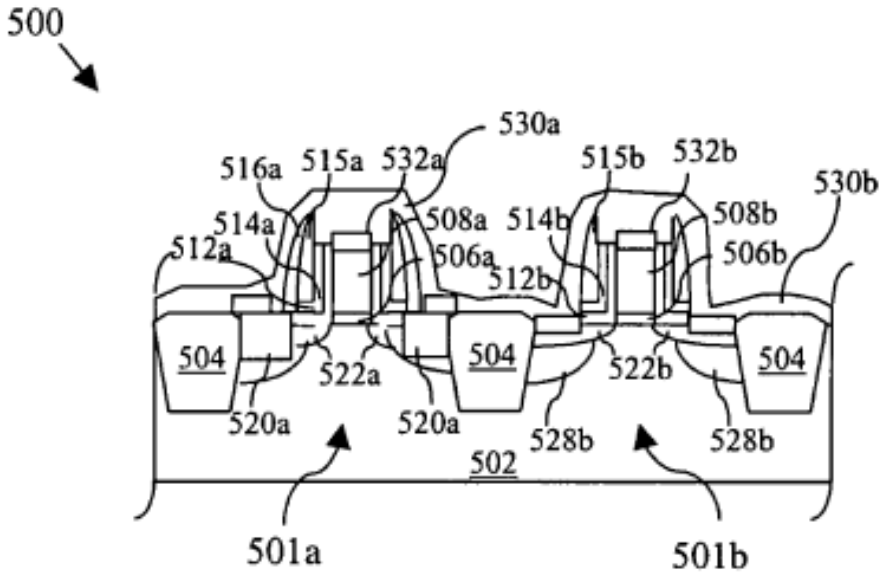
"In FIG. 4d, the dummy spacer material 416 is processed to form the dummy spacers 416a and 416b. The dummy spacer material 416 may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), silicon oxy-carbide (SiOC), polymer, and/or other materials. The spacer material 416 may be formed by CVD, PECVD, ALD, spin-on coating, and/or other processing techniques, for example, and the dummy spacers 416a and 416b may be formed by chemical etch, plasma etch, CMP, focused ion beam (FIB), and/or other processing techniques. In FIG. 4d, a photoresist 417b is provided over the device 401b so that portions of the dummy spacer material 416a is removed from the device 401a, and recessed source and drain regions 418a are also formed in the substrate 402 on either side of the gate structure of the device 401a."

Cheng817 ¶ [0063].

"Further, a dummy spacer material 516 is formed over the semiconductor devices 501a and 501b, and subsequently processed forming the dummy spacers 516a and 516b. The dummy spacer material 516 may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), silicon oxy-carbide (SiOC), polymer, and/or other materials. The spacer material 516 may be formed by CVD, PECVD, ALD, spin-on coating, and/or other processing techniques, and

Exemplary Disclosures
may be formed by chemical etch, plasma etch, CMP, focused ion beam (FIB), and/or other processing techniques." Cheng817 ¶ [0078]. Additionally, under Plaintiff's apparent interpretation of the claim language, the claimed "first gate electrode" may include a silicide film. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 11-13, 18, 20, 22, 24-25, 26, 39. Although TSMC does not necessarily agree with such an interpretation, Cheng817 further discloses this element under this interpretation, as shown below. For example, Cheng817 discloses silicide 432a formed on PMOS gate electrode 408a. *See, e.g.*, the following:    Cheng817 Figs. 4j, 5i (showing dummy spacers 416a and 516a are not in direct contact with the side surfaces of PMOS silicides 432a and 532a).      **Figure A** **Figure B** **(Cheng817, Figs. 4j, 5i (corrected))**

Exemplary Disclosures
"In FIG. 4i, the photoresist 421b is removed from the device 401b, and salicided contacts 432a and 432b are formed over the gate, source and drain of the devices 401a and 401b. The salicided contacts 432a and 432b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 732a and 732b may also include an anneal. The salicided contacts 732a and 732b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0069]. "Because the deeper doped source and drain regions were doped in-situ (FIG. 5g), a process of source and drain implantation such as that shown in FIG. 4h is not required. Therefore, salicided contacts 532a and 532b are formed for the gate, source and drains of the devices 501a and 501b, respectively, as shown in FIG. 5h. The salicided contacts 532a and 532b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 532a and 532b may also include an anneal. The salicided contacts 532a and 532b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0083]. *See also, e.g.,* Cheng817 ¶ [0003], ¶ [0019], ¶ [0041], ¶ [0052], ¶ [0058], ¶ [0069], ¶ [0073], ¶ [0083], ¶ [0087], ¶ [0097], ¶ [0099], ¶ [0101], FIGS. 1, 2, 3n, 4i-4j, 5h-5i, 6h-6i, 7. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

Exemplary Disclosures
3[a] The semiconductor device of claim 1, further comprising: a first silicide layer formed on the first gate electrode; and
Cheng817 discloses this feature. For example, Cheng817 discloses first PMOS silicide 432a formed on the PMOS gate electrode 408a. *See, e.g.*, the following:  Cheng817 Fig. 4j (showing PMOS silicide 432a formed on the PMOS gate electrode 408a).  Cheng817 Fig. 5i (showing PMOS silicide 532a formed on the PMOS gate electrode 508a).

Exemplary Disclosures

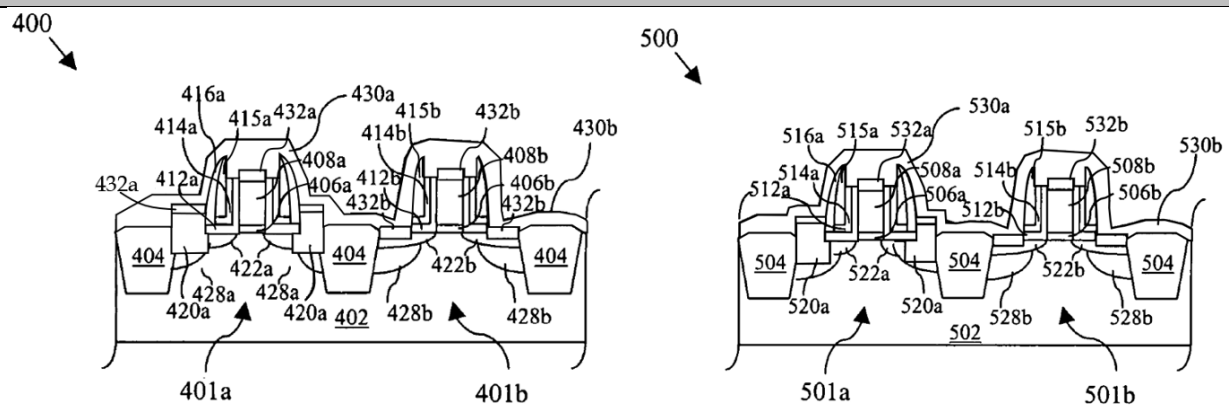


Figure A **Figure B**

(Cheng817, Figs. 4j, 5i (corrected))

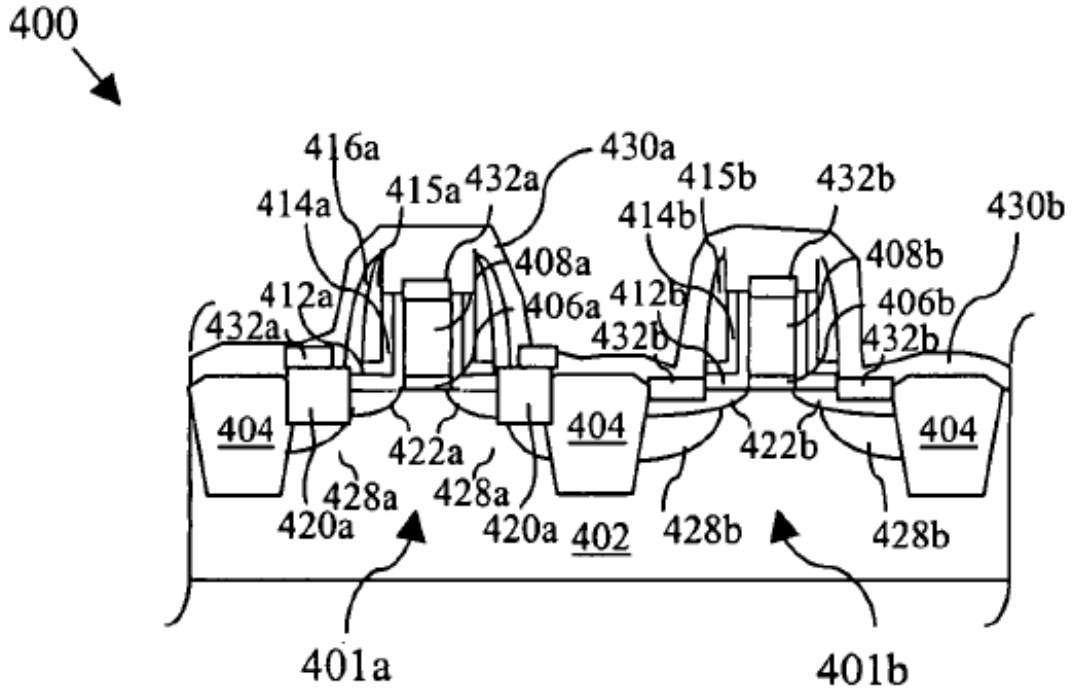
"In FIG. 4i, the photoresist 421b is removed from the device 401b, and salicided contacts 432a and 432b are formed over the gate, source and drain of the devices 401a and 401b. The salicided contacts 432a and 432b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 732a and 732b may also include an anneal. The salicided contacts 732a and 732b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques."

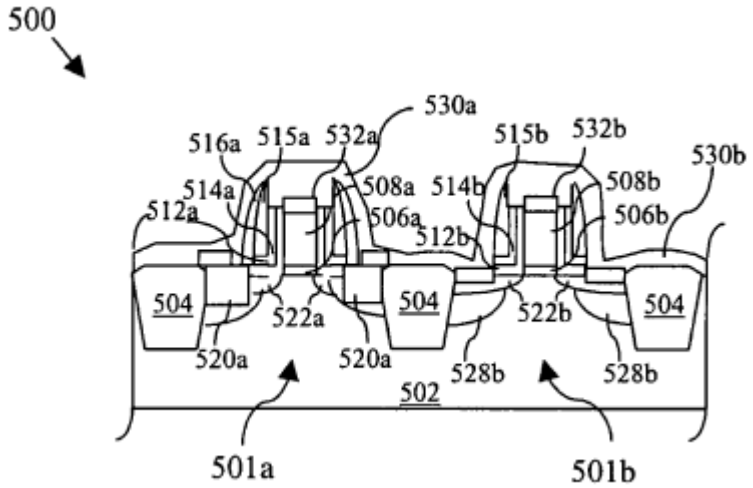
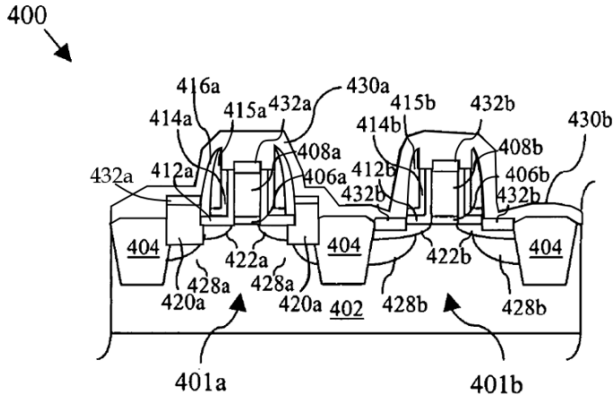
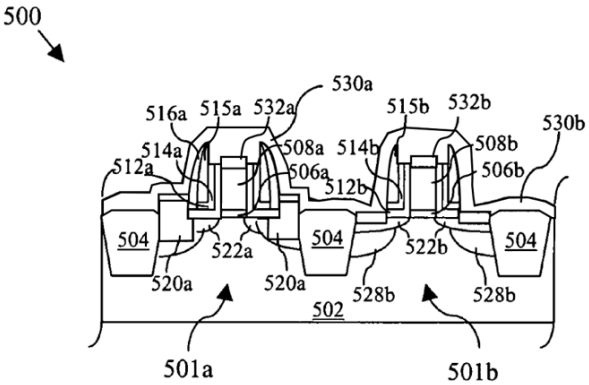
Cheng817 ¶ [0069].

"Because the deeper doped source and drain regions were doped in-situ (FIG. 5g), a process of source and drain implantation such as that shown in FIG. 4h is not required. Therefore, salicided contacts 532a and 532b are formed for the gate, source and drains of the devices 501a and 501b, respectively, as shown in FIG. 5h. The salicided contacts 532a and 532b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 532a and 532b may also include an anneal. The salicided contacts 532a and 532b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques."

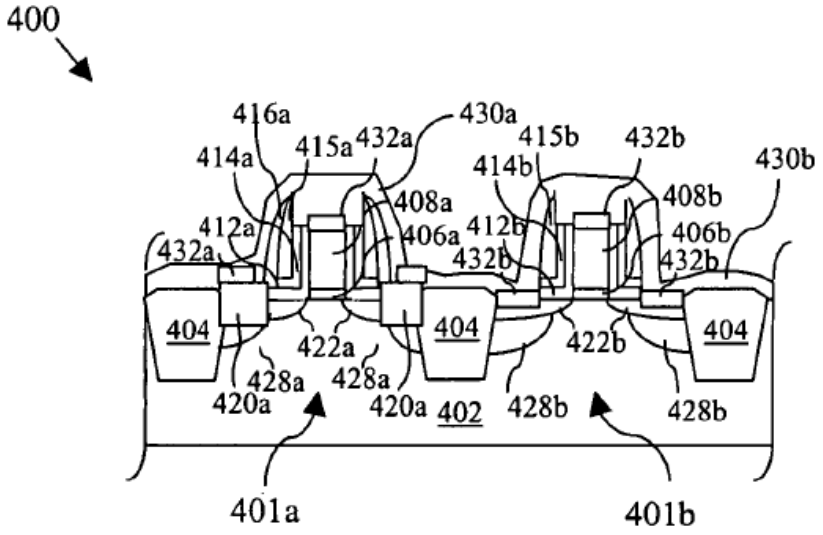
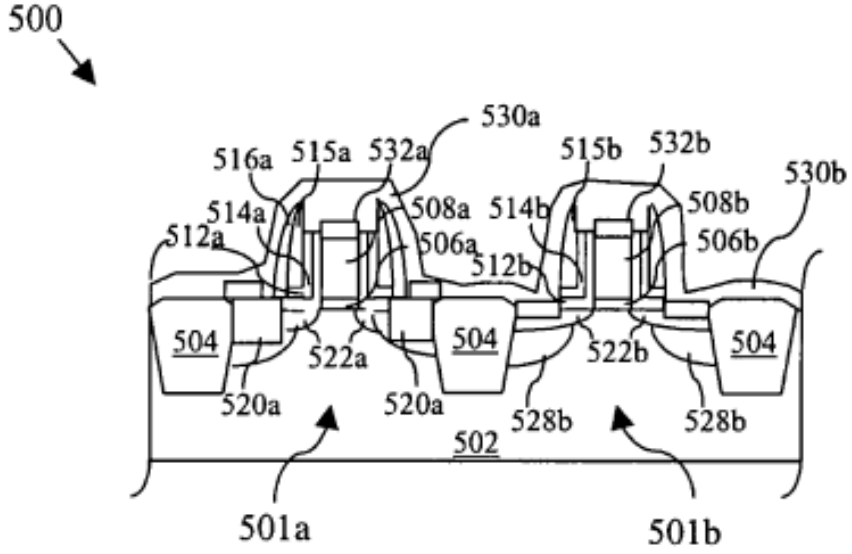
Cheng817 ¶ [0083].

Under AICP's understanding of 1[c]—whereby the gate silicide can be part of the gate electrode itself—the silicide cannot be "formed on" the gate electrode, as claimed. If such an illogical interpretation is permitted, however, this reference would additionally satisfy 3[a] under the alternative mapping of 1[c].

Exemplary Disclosures
See also, e.g., Cheng817 ¶ [0003], ¶ [0019], ¶ [0041], ¶ [0052], ¶ [0058], ¶ [0069], ¶ [0073], ¶ [0083], ¶ [0087], ¶ [0097], ¶ [0099], ¶ [0101], FIGS. 1, 2, 3n, 4i-4j, 5h-5i, 6h-6i, 7. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
3[b] a second silicide layer formed on the first source/drain region which includes the silicon compound layer.
Cheng817 discloses this feature. For example, Cheng817 discloses PMOS silicide 432a formed on the PMOS epitaxial source/drain regions 420a, which include the SiGe layer 520a. *See, e.g.*, the following:    Cheng817 Fig. 4j (showing PMOS silicide 432a formed on the PMOS epitaxial source/drain regions 420a).

Exemplary Disclosures
 Cheng817 Fig. 5i (showing PMOS silicide 532a formed on the PMOS epitaxial source/drain regions 520a).   **Figure A** **Figure B** **(Cheng817, Figs. 4j, 5i (corrected))** "In FIG. 4i, the photoresist 421b is removed from the device 401b, and salicided contacts 432a and 432b are formed over the gate, source and drain of the devices 401a and 401b. The salicided contacts 432a and 432b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 732a and 732b may also include an anneal. The salicided contacts 732a and 732b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0069].

Exemplary Disclosures
"Because the deeper doped source and drain regions were doped in-situ (FIG. 5g), a process of source and drain implantation such as that shown in FIG. 4h is not required. Therefore, salicided contacts 532a and 532b are formed for the gate, source and drains of the devices 501a and 501b, respectively, as shown in FIG. 5h. The salicided contacts 532a and 532b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 532a and 532b may also include an anneal. The salicided contacts 532a and 532b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0083]. Under AICP's understanding of 1[f]—whereby the source/drain silicide can be part of the silicon compound layer, which is itself part of the source/drain region—the silicide cannot be "formed on" the source/drain region, as claimed. If such an illogical interpretation is permitted, however, this reference would additionally satisfy 3[b] under the alternative mapping of 1[f]. *See also, e.g.*, Cheng817 ¶ [0003], ¶ [0019], ¶ [0041], ¶ [0052], ¶ [0058], ¶ [0069], ¶ [0073], ¶ [0083], ¶ [0087], ¶ [0097], ¶ [0099], ¶ [0101], FIGS. 1, 2, 3n, 4i-4j, 5h-5i, 6h-6i, 7. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

Exemplary Disclosures
4[a] The semiconductor device of claim 1, wherein the first stress-relief film is formed on a side surface of the silicon compound layer.
Cheng817 discloses this feature. For example, Cheng817 discloses that dummy spacer 416a is formed on a side surface of PMOS SiGe source/drain region 420a. *See, e.g.*, the following:  Cheng817 Fig. 4j (showing dummy spacer 416a is formed on a side surface of PMOS SiGe source/drain region 420a).  Cheng817 Fig. 5i (showing dummy spacer 516a is formed on a side surface of PMOS SiGe source/drain region 520a).

Exemplary Disclosures

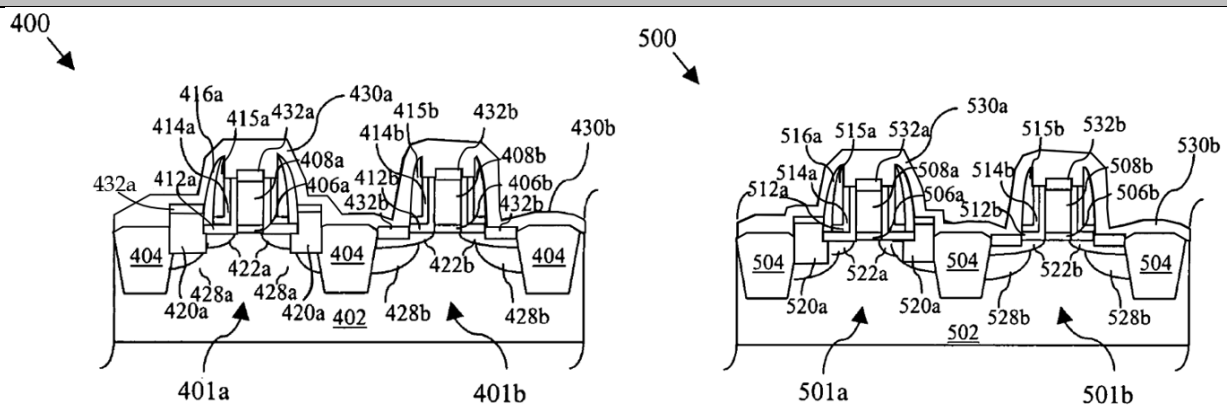


Figure A **Figure B**

(Cheng817, Figs. 4j, 5i (corrected))

"The gate dielectric layer 120 may be formed by thermal oxidation, atomic layer deposition (ALD), chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma enhanced CVD (PECVD) and/or other processes. Moreover, although not limited by the scope of the present disclosure, the gate dielectric layer 120 may comprise silicon oxide, silicon oxynitride, or a high-k dielectric, such as hafnium oxide, zirconium oxide, aluminum oxide, a hafnium dioxide-alumina (HfO2-Al2O3) alloy, and/or combinations thereof. The gate dielectric layer may have a thickness ranging between about 0.5 nm and about 10 nm."

Cheng817 ¶ [0018].

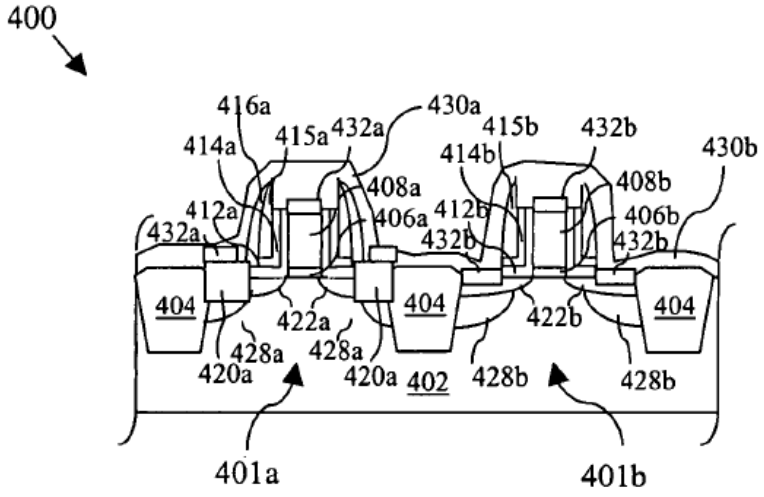
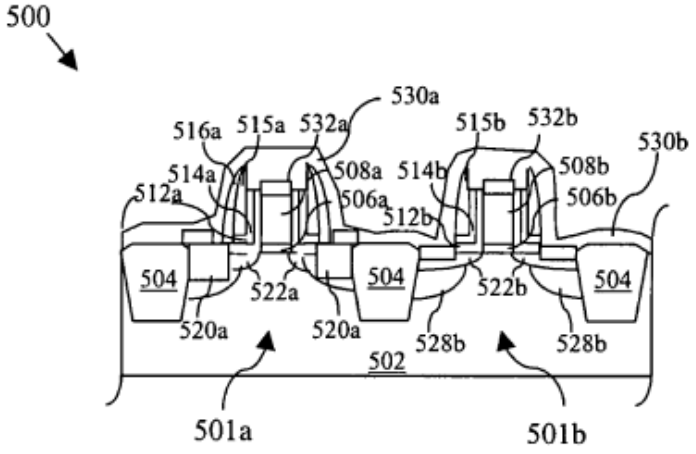
"The spacers 132 may be formed by CVD, PVD, thermal oxidation and/or other processes, and may comprise one or more dielectric materials such as silicon nitride, silicon oxide, silicon carbide, silicon oxynitride and/or combinations thereof. The spacers 132 may each have a width W_P extending from the gate electrode 124. The width of spacers 132 may range between about 5 nm and about 100 nm."

Cheng817 ¶ [0020].

"The source/drain regions 136 may be of conventional composition and fabrication. For example, the source/drain regions 136 may comprise doped portions of the substrate 104 which may be formed by ion implantation of boron, boron difluoride (BF2), or other dopants, and/or in-situ doped of boron or other dopants. In such embodiments, the source/drain regions 136 may be substantially coplanar with the surface 106 of the substrate 104. However, as in the illustrated embodiment, the source/drain regions 136 may extend above the substrate surface 106. In such embodiments, the source/drain regions 136 may comprise silicon, silicon germanium, silicon carbide, gallium arsenide and/or other materials, and may be formed by dry etching or otherwise patterning recesses in the substrate 104 and subsequently filling the recesses with such materials. For example, the recess may be epitaxially filled with silicon germanium, possibly by exposing the recesses to a precursor comprising germanium. The filled recesses are herein designated by

Exemplary Disclosures
the reference numeral 144. The depth of recessed source/drain region may range between about 5 nm and about 100 nm. Moreover, as in the illustrated embodiment, the recesses 144 may be filled to a height above the surface 106 of the substrate 104, such that the source/drain regions 136 may be raised source/drain regions. The height of raised source/drain regions may range between about 5 nm and about 100 nm." Cheng817 ¶ [0022]. "In FIG. 4b, sidewall dielectric layers 412 and 414, and spacer material 415 are disposed over the semiconductor device(s) 410a and 401b and are subsequently processed, such as by etching, to form sidewall dielectric structures 412a, 412b, 414a and 414b, and spacers 415a and 415b, as shown in FIG. 4c. Note the dielectric structures 714a and 714b are substantially L-shaped. A dummy spacer layer 416 is formed over the semiconductor devices 401a and 401b. Low temperature processing, such as using a temperature less than 600° C., to form the sidewall dielectric and spacer materials is preferred to reduce lightly doped drain diffusion." Cheng817 ¶ [0061]. "In FIG. 4d, the dummy spacer material 416 is processed to form the dummy spacers 416a and 416b. The dummy spacer material 416 may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), silicon oxy-carbide (SiOC), polymer, and/or other materials. The spacer material 416 may be formed by CVD, PECVD, ALD, spin-on coating, and/or other processing techniques, for example, and the dummy spacers 416a and 416b may be formed by chemical etch, plasma etch, CMP, focused ion beam (FIB), and/or other processing techniques. In FIG. 4d, a photoresist 417b is provided over the device 401b so that portions of the dummy spacer material 416a is removed from the device 401a, and recessed source and drain regions 418a are also formed in the substrate 402 on either side of the gate structure of the device 401a." Cheng817 ¶ [0063]. "In FIG. 4i, the photoresist 421b is removed from the device 401b, and salicided contacts 432a and 432b are formed over the gate, source and drain of the devices 401a and 401b. The salicided contacts 432a and 432b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 732a and 732b may also include an anneal. The salicided contacts 732a and 732b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0069].

Exemplary Disclosures
"Further, a dummy spacer material 516 is formed over the semiconductor devices 501a and 501b, and subsequently processed forming the dummy spacers 516a and 516b. The dummy spacer material 516 may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), silicon oxy-carbide (SiOC), polymer, and/or other materials. The spacer material 516 may be formed by CVD, PECVD, ALD, spin-on coating, and/or other processing techniques, and may be formed by chemical etch, plasma etch, CMP, focused ion beam (FIB), and/or other processing techniques." Cheng817 ¶ [0078]. "Because the deeper doped source and drain regions were doped in-situ (FIG. 5g), a process of source and drain implantation such as that shown in FIG. 4h is not required. Therefore, salicided contacts 532a and 532b are formed for the gate, source and drains of the devices 501a and 501b, respectively, as shown in FIG. 5h. The salicided contacts 532a and 532b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 532a and 532b may also include an anneal. The salicided contacts 532a and 532b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0083]. *See also, e.g.*, Cheng817 ¶ [0019], ¶ [0021]. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

Exemplary Disclosures
5[a] The semiconductor device of claim 1, wherein the first sidewall spacer includes an inner sidewall spacer which is formed on the side surface of the first gate electrode, and whose cross-section has an L shape, and an outer sidewall spacer formed on the inner sidewall spacer.
Cheng817 discloses this feature. For example, Cheng817 discloses inner sidewall spacers 412a and 414a, which are formed on the side surface of PMOS gate electrode 408a and have an L-shaped cross-section, and outer sidewall spacers 415a formed on inner sidewall spacers 412a and 414a. Sidewall spacers 414a are also outer sidewall spacers formed on inner sidewall spacers 412a. *See, e.g.*, the following:  Cheng817 Fig. 4j (showing sidewall spacers 412a, 414a, and 415a).  Cheng817 Fig. 5i (showing sidewall spacers 512a, 514a, and 515a).

Exemplary Disclosures

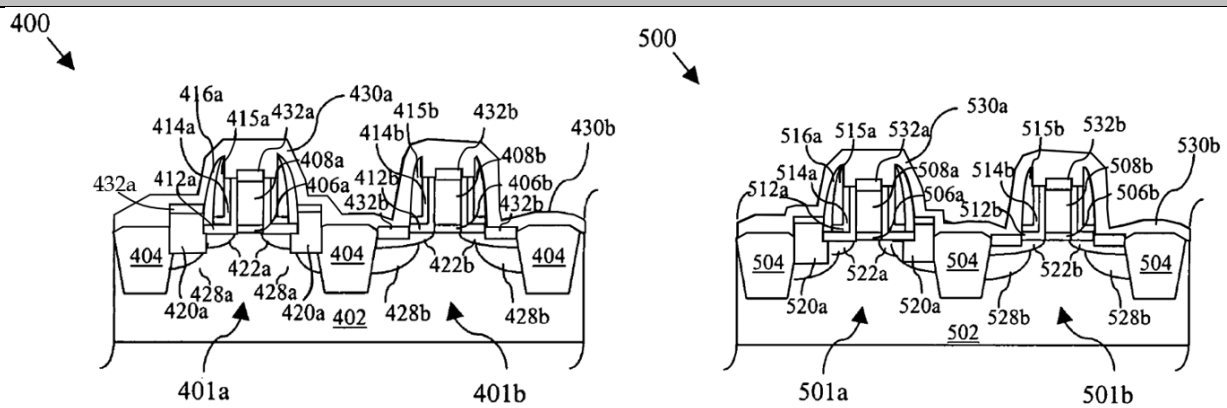


Figure A **Figure B**

(Cheng817, Figs. 4j, 5i (corrected))

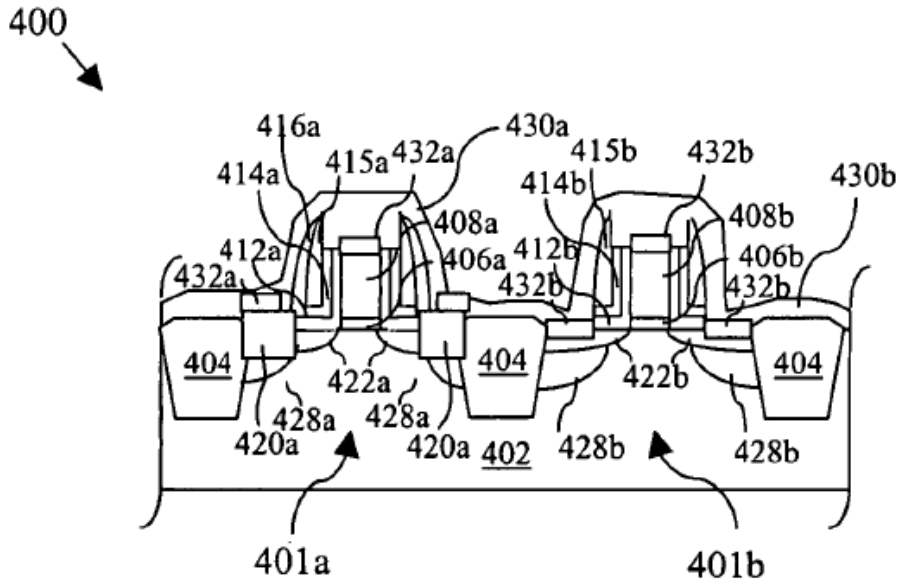
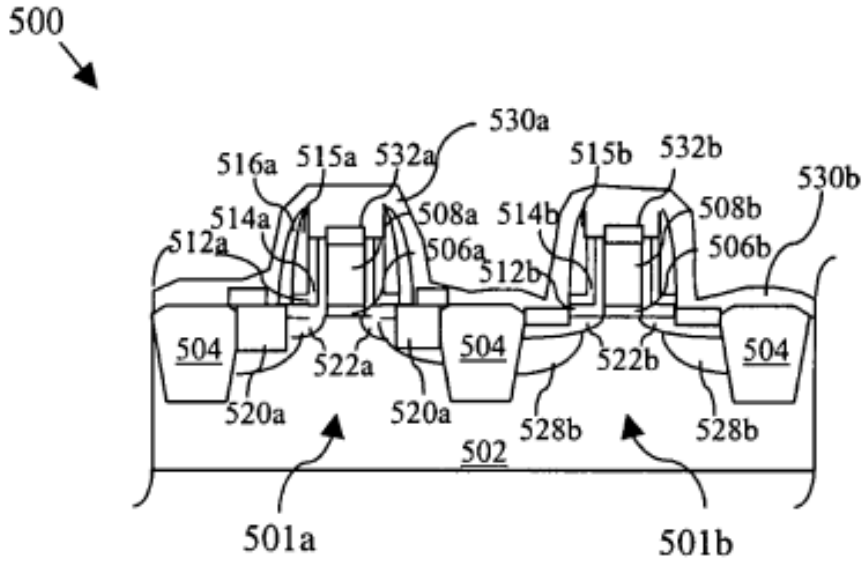
"In FIG. 4b, sidewall dielectric layers 412 and 414, and spacer material 415 are disposed over the semiconductor device(s) 410a and 401b and are subsequently processed, such as by etching, to form sidewall dielectric structures 412a, 412b, 414a and 414b, and spacers 415a and 415b, as shown in FIG. 4c. Note the dielectric structures 714a and 714b are substantially L-shaped. A dummy spacer layer 416 is formed over the semiconductor devices 401a and 401b. Low temperature processing, such as using a temperature less than 600° C., to form the sidewall dielectric and spacer materials is preferred to reduce lightly doped drain diffusion."

Cheng817 ¶ [0061].

"The sidewall dielectric layers 412 and 414 may be a liner oxide layer and a nitride layer formed over the devices by deposition. In particular, the sidewall dielectric layers 412 and 414 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), polymer and/or other materials. The sidewall dielectric layers 412 and 414 may also include multiple layers and/or may include a single layer, in one embodiment. The sidewall dielectric layers 412 and 414 may be formed by RTO, CVD, PVD, PECVD, ALD, CMP, chemical etching, plasma etching, and/or other processing techniques. The spacer material 415 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), polymer and/or other materials. The spacer material 415 may also include multiple layers and/or may include a single layer, in one embodiment. The spacer material 415 may be formed by RTO, CVD, PVD, PECVD, ALD, CMP, chemical etching, plasma etching, and/or other processing techniques. The sidewall dielectric structures 412a, 412b, 414a and 414b, and spacers 415a and 415b may be formed by chemical etching, plasma etching, CMP, focused ion beam (FIB), and/or other processing techniques."

Cheng817 ¶ [0062].

Exemplary Disclosures
"In FIG. 5b, sidewall dielectric layers 512 and 514, and a spacer material 515 are formed over the semiconductor devices 510a and 501b, preferably using a low temperature process to reduce LDD diffusion. The sidewall dielectric layers 512 and 514 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), polymer and/or other materials. The spacer material 515 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), polymer and/or other materials. For example, dielectric layers 512 and 514 may comprise a liner oxide layer and a nitride layer, and the spacer material 515 may comprise an oxide material. The sidewall dielectric layers 512 and 514 and spacer layer 515 may be formed by RTO, CVD, PVD, PECVD, ALD, CMP, chemical etching, plasma etching, and/or other processing techniques." Cheng817 ¶ [0076] "In FIG. 5c, the sidewall dielectric layers 512 and 514, and a spacer material 515 are subsequently processed forming sidewall dielectric 512a, 512b, 514a and 514b, and spacers 515a and 515b. The sidewall dielectric 512a, 512b, 514a and 514b, and spacers 515a and 515b may be formed by chemical etching, plasma etching, CMP, focused ion beam (FIB), and/or other processing techniques." Cheng817 ¶ [0077]. "… wherein the spacers of the first and second semiconductor devices are L-shaped." Cheng817 Claims 33, 42. *See also, e.g.*, Cheng817, at Abstract, ¶ [0017], ¶¶ [0020]-[0021], ¶ [0023], ¶ [0025], ¶ [0027], ¶ [0035], ¶¶ [0043]-[0045], ¶¶ [0048]-[0050], ¶ [0054], ¶¶ [0061]-[0064], ¶ [0066], ¶¶ [0076]-[0079], ¶ [0081], ¶¶ [0090]-[0093], ¶ [0095], ¶ [0097], ¶ 0099], ¶ [0101], claims 33, 42, FIGS. 1, 2, 3b-3n, 4b-4j, 5b-5i, 6b-6i, 7. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

Exemplary Disclosures
7[a] The semiconductor device of claim 1, wherein the first MIS transistor is a p-type MIS transistor,
Cheng817 discloses this feature. For example, Cheng817 discloses a PMOS transistor. *See, e.g.*, the following:  Cheng817 Fig. 4j (showing PMOS transistor 401a on the left-hand side).  Cheng817 Fig. 5i (showing PMOS transistor 501a on the left-hand side).

Exemplary Disclosures

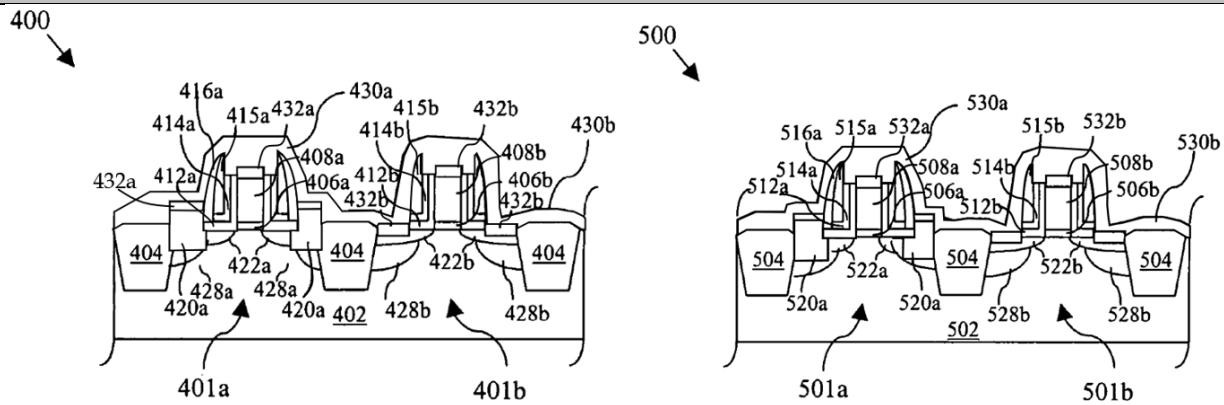


Figure A **Figure B**

(Cheng817, Figs. 4j, 5i (corrected))

"Thus, the present disclosure introduces a semiconductor device including, in one embodiment, an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface; and (2) first source/drain regions extending from the surface. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface."

Cheng817 ¶ [0033].

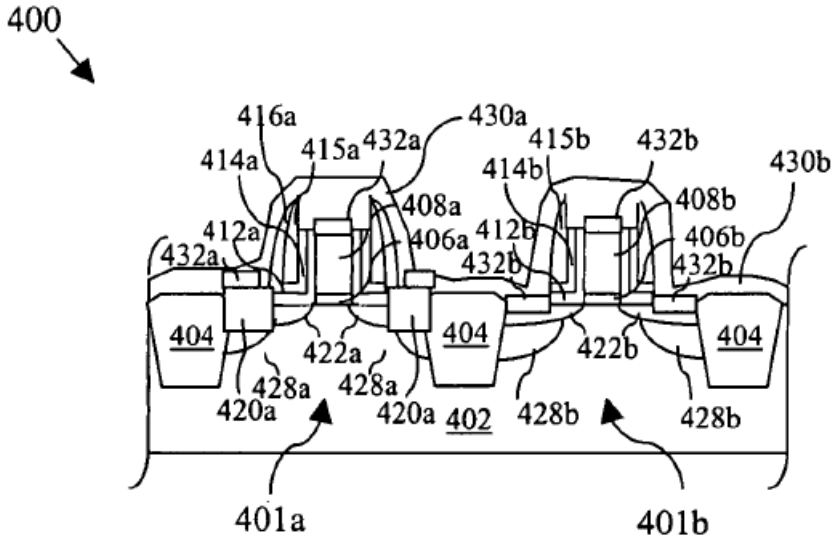
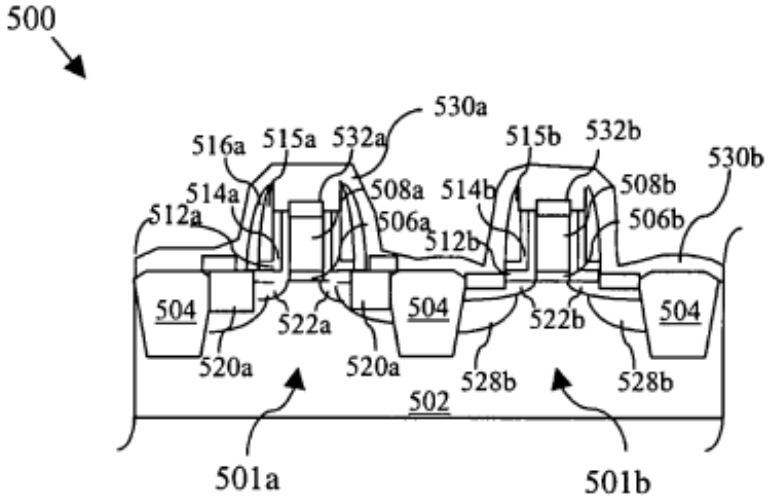
"In another embodiment, semiconductor device constructed according to aspects of the present disclosure comprises an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface. A second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different."

Cheng817 ¶ [0034].

Exemplary Disclosures
"Another embodiment of a semiconductor device constructed according to aspects of the present disclosure includes an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; (2) a first gate interposing the first source/drain regions; and (3) first spacers on opposing sides of the first gate and each extending from the first gate to a first width. A second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; (2) a second gate interposing the second source/drain regions; and (3) second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different." Cheng817 ¶ [0035]. "In another embodiment, a semiconductor device constructed according to aspects of the present disclosure includes an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe; (2) second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and (3) second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe." Cheng817 ¶ [0036]. "The present disclosure also introduces a method of manufacturing semiconductor device. In one embodiment, the method includes forming an isolation region located in a substrate, forming an NMOS device located partially over a surface of the substrate, and forming a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface; and (2) first source/drain regions extending from the surface. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface." Cheng817 ¶ [0037].

Exemplary Disclosures
"Referring now to FIGS. 4a-4j for sectional views of another embodiment of a method for making semiconductor devices 401a and 401b with high drive current. The semiconductor device 401a may be a P-type MOS device and the semiconductor device 401b may be an N-type MOS device. In FIG. 4a, gate dielectric 406a and 406b are formed over a substrate 402 for devices 401a and 401b, respectively, and electrically isolated from one another by isolation structures 404. The isolation structures 404 may be shallow trench isolation (STI) structures. Gate electrodes 408a and 408b are formed over the gate dielectric layer, and hard masks 410a and 410b are formed over the gate electrodes 408a and 408b, respectively." Cheng817 ¶ [0056]. "The lightly doped regions 422a and 422b may include P-type and N-type dopants for the devices 401a and 401b, respectively. The doped regions 422a and 422b may be formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The doped regions 422a and 422b may also include lightly doped regions (LDD) and/or heavily doped regions in one embodiment. The doped regions 422a and 422b may include impurities such as phosphorous, boron, antimony, arsenic, and/or other materials. For example, the formation of the doped regions 422a and 422b by ion implantation may include an ion implant energy ranging between about 1 KeV and about 100 KeV and the dose of ion implantation of may range between about 1×10^{13} cm^{-2} and about 5×10^{16} cm^{-2}." Cheng817 ¶ [0060]. "In FIG. 4e, the photoresist 417b is removed, and doped source and drain regions 420a are formed or built-up in the recessed regions 418a. The doped source and drain regions 420a may be formed by selective epitaxial growth (SEG), CVD, PECVD, PVD, PDL, ALD, spin-on formation, and/or other techniques now know or to be developed. The doped source and drain regions 420a may include materials such as amorphous silicon, polysilicon, strained silicon, germanium, silicon germanium, silicon carbide, and/or other materials. Low temperature processing, such as using a temperature less than 700° C., to form the doped regions 420a is preferred to reduce lightly doped drain diffusion." Cheng817 ¶ [0065]. "In FIG. 4h, a photoresist 421b is formed over the semiconductor device 401a. The mask 421b may include photoresist, silicon dioxide (SiO_2), silicon nitride (Si_xN_y), and/or other materials. The mask 421b may be formed by spin-on coating, CVD, and/or other processing techniques. Further, more heavily doped source and drain regions 428a are formed in the substrate 402 for the semiconductor device 401a. The doped regions 428a which may include P-type impurities, and may be formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The ion implantation may include an ion implant energy ranging between about 5 KeV and about 100 KeV and the dose of ion implantation of may range between about 1×10^{14} cm^{-2} and about 5×10^{18} cm^{-2} for example." Cheng817 ¶ [0068].

Exemplary Disclosures
"Further in FIG. 4j, an etch stop layer 430a and 430b are formed over the semiconductor device(s) 401a and 401b. The etch stop layer 430a and 430b may include silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), and/or other materials. In one embodiment, the etch stop layer 430a and 430b may be substantially similar in composition to the etch stop layer 180 described above. Alternatively, the etch stop layer 430a and 430b may include a stress level that may range between about +0.001 and about +50 GPa for tensile film and between about −0.001 and about −50 GPa for compressive film. The etch stop layer 430a and 430b may be formed by CVD, ALD, PECVD, PDL, spin-on coating, and/or other techniques." Cheng817 ¶ [0070]. "Referring now to FIGS. 5a-i for another embodiment of a method for manufacturing a microelectronic device 500 with high drive current. In FIG. 5a, gate structures including a gate dielectric 506a and 506b and gate electrodes 508a and 508b are formed for semiconductor devices 501a and 501b, respectively. Gate electrodes 508a and 508b may be pre-doped with appropriate P-type and N-type dopants, respectively. Hard masks 510a and 510b are also formed over each gate structure. Further, shallow doped drain and source regions 522a and 522b are formed on either sides of the gate structures of each device 501a and 501b. Isolation structures 504 are formed in the substrate 502 to electrically isolate the devices 501a and 501b." Cheng817 ¶ [0072]. "The doped source and drain regions 522a and 522b may include N-type and/or P-type doped regions formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The doped regions 522a and 522b may be lightly doped drains (LDD) and may include impurities such as phosphorous, boron, antimony, arsenic, and/or other materials." Cheng817 ¶ [0075]. "In FIG. 5e, the photoresist 517b is removed from the device 501b and source and drain regions 520a are built-up in the recessed regions 518a, preferably using a low temperature process to reduce LDD diffusion. The source and drain regions 520a may be formed by, for example, selective epitaxial growth (SEG), CVD, PECVD, PVD, PDL, ALD, spin-on formation, and/or other suitable techniques now know or later developed. The source and drain regions 520a may include materials such as amorphous silicon, polysilicon, strained silicon, germanium, silicon germanium, silicon carbide, and/or other materials. The source and drain regions 520a may also be doped 'in-situ' during the SEG process, for example. In this process, dopants such as boron, phosphorous, arsenic, germanium, carbon, and/or other semiconductor materials may be introduced during the SEG process. The dopants may be introduced in gaseous form, which may include diborane (B_2H_6), Arsine (AsH_3), phosphine (PH_3), germane (GeH_4), phosphoryl chloride ($POCL_3$), boron bromide (BBr_3), hydrocarbons, and/or other gases/chemicals." Cheng817 ¶ [0080].

Exemplary Disclosures
To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
7[b] the first stress is a compressive stress, and
Cheng817 discloses this feature. For example, Cheng817 discloses PMOS epitaxial SiGe source/drain regions 420a cause compressive stress. *See, e.g.*, the following:  Cheng817 Fig. 4j (showing discloses PMOS epitaxial SiGe source/drain regions 420a).  Cheng817 Fig. 5i (showing discloses PMOS epitaxial SiGe source/drain regions 520a).

Exemplary Disclosures

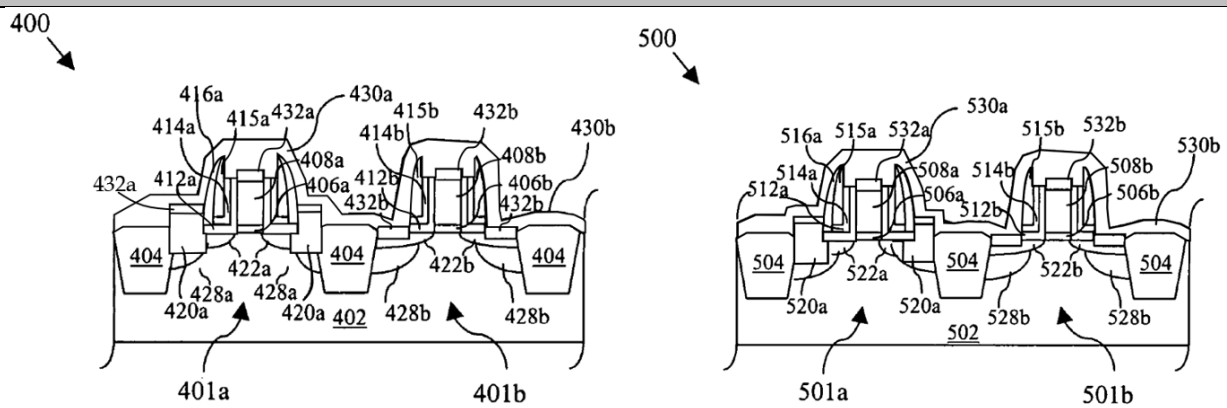


Figure A **Figure B**

(Cheng817, Figs. 4j, 5i (corrected))

"[I]ncreasing the tensile stress in the substrate can improve the performance of n-channel metal-oxide-semiconductor (NMOS) devices. Similarly, increasing the compressive stress in the substrate can improve the performance of p-channel metal-oxide-semiconductor (PMOS) devices."

Cheng817 ¶ [0002].

"In such embodiments, the source/drain regions 136 may comprise silicon, silicon germanium, silicon carbide, gallium arsenide and/or other materials, and may be formed by dry etching or otherwise patterning recesses in the substrate 104 and subsequently filling the recesses with such materials. For example, the recess may be epitaxially filled with silicon germanium, possibly by exposing the recesses to a precursor comprising germanium. The filled recesses are herein designated by the reference numeral 144. The depth of recessed source/drain region may range between about 5 nm and about 100 nm. Moreover, as in the illustrated embodiment, the recesses 144 may be filled to a height above the surface 106 of the substrate 104, such that the source/drain regions 136 may be raised source/drain regions. The height of raised source/drain regions may range between about 5 nm and about 100 nm."

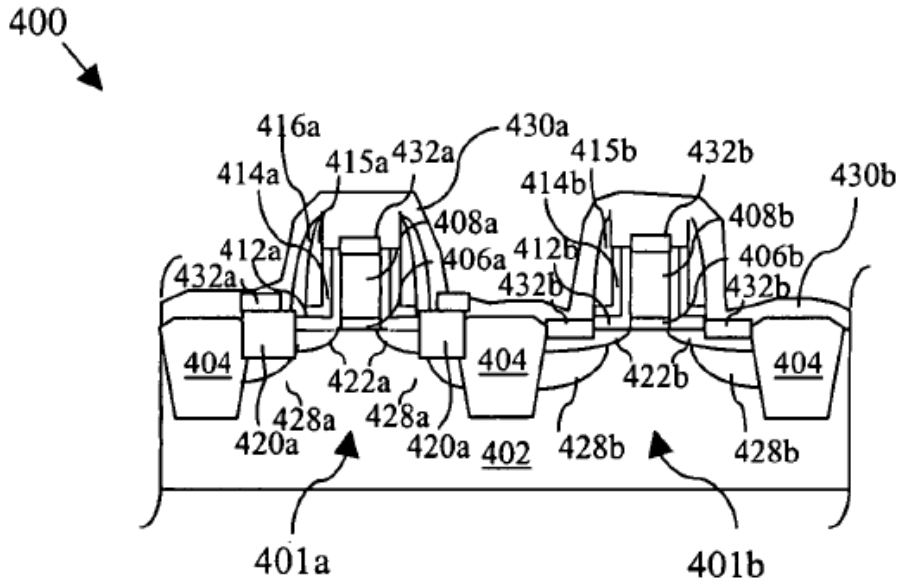
Cheng817 ¶ [0022].

"In FIG. 3f, raised source and drain regions 320a are formed or built-up in the recesses 318a. For example, the source and drain regions 320a may be formed by selective epitaxial growth (SEG), CVD, PECVD, PVD, PDL, ALD, spin-on formation, and/or other techniques. The source and drain regions 320a may include materials such as amorphous silicon, polysilicon, strained silicon, germanium, silicon germanium, silicon carbide, and/or other materials."

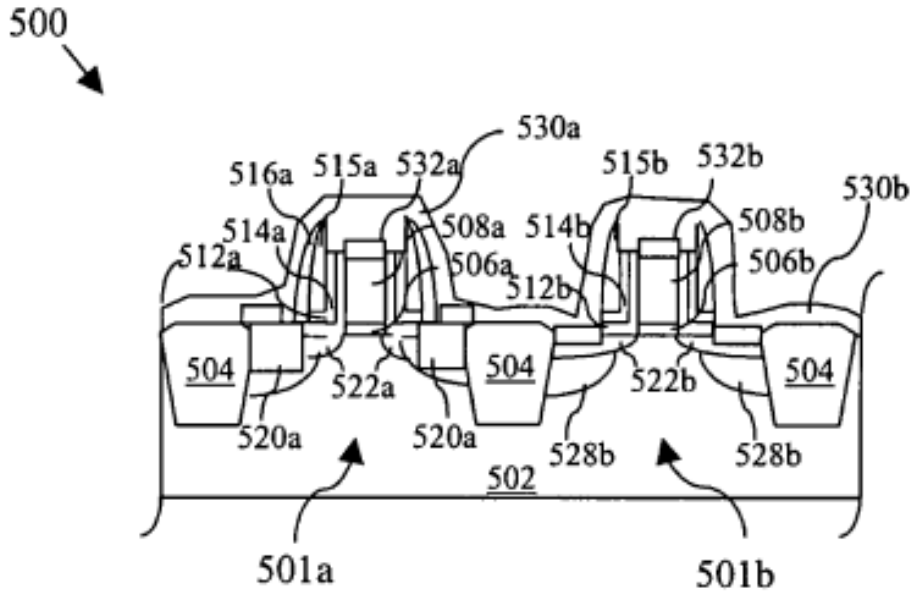
Cheng817 ¶ [0044].

Exemplary Disclosures
"In FIG. 4e, the photoresist 417b is removed, and doped source and drain regions 420a are formed or built-up in the recessed regions 418a. The doped source and drain regions 420a may be formed by selective epitaxial growth (SEG), CVD, PECVD, PVD, PDL, ALD, spin-on formation, and/or other techniques now know or to be developed. The doped source and drain regions 420a may include materials such as amorphous silicon, polysilicon, strained silicon, germanium, silicon germanium, silicon carbide, and/or other materials. Low temperature processing, such as using a temperature less than 700° C., to form the doped regions 420a is preferred to reduce lightly doped drain diffusion." Cheng817 ¶ [0065]. "In FIG. 5e, the photoresist 517b is removed from the device 501b and source and drain regions 520a are built-up in the recessed regions 518a, preferably using a low temperature process to reduce LDD diffusion. The source and drain regions 520a may be formed by, for example, selective epitaxial growth (SEG), CVD, PECVD, PVD, PDL, ALD, spin-on formation, and/or other suitable techniques now know or later developed. The source and drain regions 520a may include materials such as amorphous silicon, polysilicon, strained silicon, germanium, silicon germanium, silicon carbide, and/or other materials. The source and drain regions 520a may also be doped "in-situ" during the SEG process, for example. In this process, dopants such as boron, phosphorous, arsenic, germanium, carbon, and/or other semiconductor materials may be introduced during the SEG process. The dopants may be introduced in gaseous form, which may include diborane (B_2H_6), Arsine (AsH_3), phosphine (PH_3), germane (GeH_4), phosphoryl chloride ($POCL_3$), boron bromide (BBr_3), hydrocarbons, and/or other gases/chemicals." Cheng817 ¶ [0080]. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

Exemplary Disclosures
7[c] the second stress is a tensile stress.
Cheng817 discloses this feature. For example, Cheng817 discloses that etch stop layer 430a may cause tensile stress. *See, e.g.*, the following:



Cheng817 Fig. 4j (showing etch stop layer 430a).



Cheng817 Fig. 5i (showing etch stop layer 530a).

Exemplary Disclosures

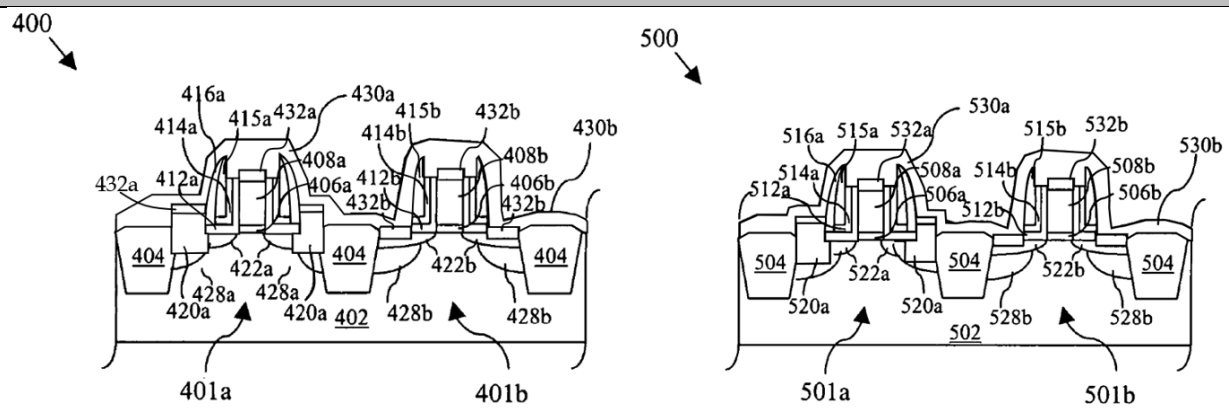


Figure A **Figure B**

(Cheng817, Figs. 4j, 5i (corrected))

"Increasing tensile or compressive stress in a semiconductor device substrate can improve drive current. For example, increasing the tensile stress in the substrate can improve the performance of n-channel metal-oxide-semiconductor (NMOS) devices. Similarly, increasing the compressive stress in the substrate can improve the performance of p-channel metal-oxide-semiconductor (PMOS) devices."

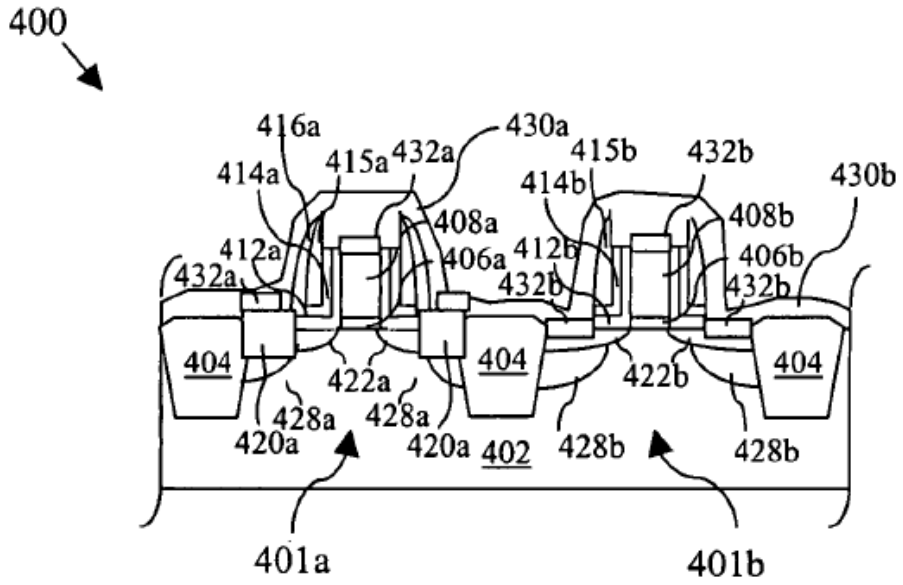
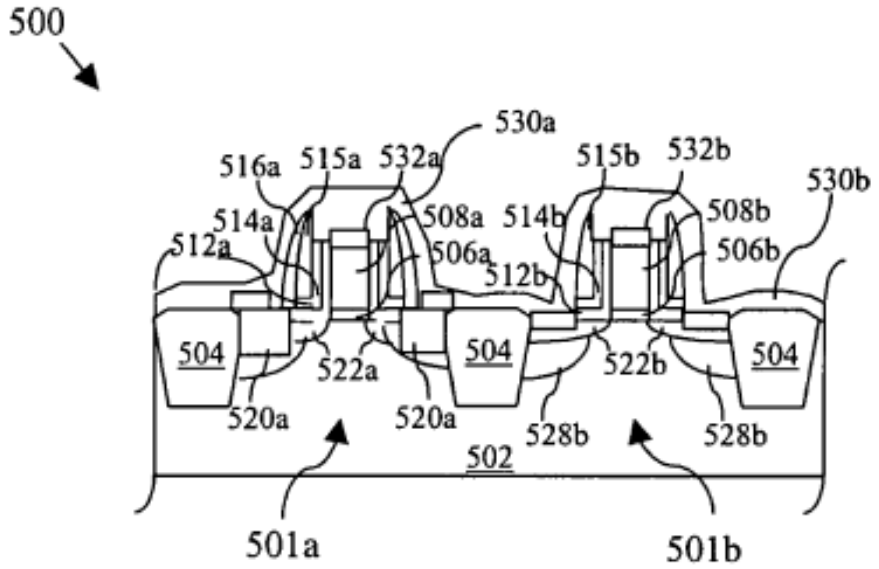
Cheng817 ¶ [0002].

"Some applications have realized limited localized stress tuning by employing different materials for adjacent shallow trench isolation (STI) regions and other isolation structures. Stress tuning can also be accomplished by employing different materials for silicide and other contact layers. Etch stop layers remaining in the device structure after being employed as etching endpoints have also been employed for substrate stress tuning."

Cheng817 ¶ [0003].

"The semiconductor device 100 may also include an etch stop layer 180. The etch stop layer 180 may comprise silicon nitride (e.g., Si3N4), silicon oxynitride (e.g., SiON), silicon carbide, silicon dioxide and/or other materials, and may be formed by blanket or selective deposition by CVD, PVD, thermal oxidation and/or other processes. The etch stop layer 180 may be a tensile or compressive film, wherein a stress level may range between about +0.01 and about +2 GPa for tensile film and between about −0.01 and about −2 GPa for compressive film. The tensile or compressive nature of the etch stop layer 180 may impart strain within the source/ drain regions 136, 176. Moreover, the strain induced in the source/drain region 136 by the etch stop layer 180 may be substantially different in magnitude that the strain induced in the source/drain region 176 by the etch stop layer 180. For example, the strain induced in the source/ drain regions 136, 176 may vary by 10-20% in magnitude. In one embodiment, the strain induced in the source/drain regions 136 may be tensile and the strain induced in the source/drain regions 176 may be compressive. In another embodiment, the strain induced in the source/drain

Exemplary Disclosures
regions 136 may be compressive and the strain induced in the source/drain regions 176 may be tensile. The thickness of etch stop layer 180 may range between about 5 nm and about 200 nm." Cheng817 ¶ [0030]. "Further in FIG. 4j, an etch stop layer 430a and 430b are formed over the semiconductor device(s) 401a and 401b. The etch stop layer 430a and 430b may include silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), and/or other materials. In one embodiment, the etch stop layer 430a and 430b may be substantially similar in composition to the etch stop layer 180 described above. Alternatively, the etch stop layer 430a and 430b may include a stress level that may range between about +0.001 and about +50 GPa for tensile film and between about −0.001 and about −50 GPa for compressive film. The etch stop layer 430a and 430b may be formed by CVD, ALD, PECVD, PDL, spin-on coating, and/or other techniques." Cheng817 ¶ [0070]. "In FIG. 5i, etch stop layer 530a and 530b are formed over the semiconductor devices 501a and 501b. The etch stop layer 530a and 530b may include silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), and/or other materials. Alternatively, the etch stop layer 530a and 530b may include a stress level that may range between about +0.001 and about +50 GPa for tensile film and between about −0.001 and about −50 GPa for compressive film. The etch stop layer 530a-b may be formed by CVD, ALD, PECVD, PDL, spin-on coating, and/or other techniques." Cheng817 ¶ [0084]. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

Exemplary Disclosures
11[a] The semiconductor device of claim 1, further comprising: a second MIS transistor, wherein: the second MIS transistor includes:
Cheng817 discloses this feature. For example, Cheng817 discloses an NMOS transistor 401b. *See, e.g.*, the following:  Cheng817 Fig. 4j (showing NMOS transistor 401b on right-hand side).  Cheng817 Fig. 5i (showing NMOS transistor 501b on right-hand side).

Exemplary Disclosures

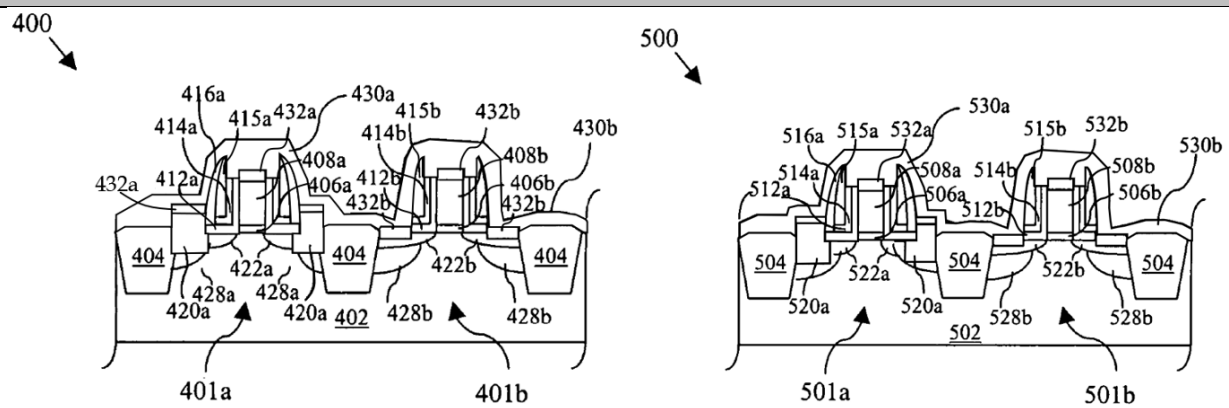


Figure A **Figure B**

(Cheng817, Figs. 4j, 5i (corrected))

"Thus, the present disclosure introduces a semiconductor device including, in one embodiment, an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface; and (2) first source/drain regions extending from the surface. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface."

Cheng817 ¶ [0033].

"In another embodiment, semiconductor device constructed according to aspects of the present disclosure comprises an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface. A second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different."

Cheng817 ¶ [0034].

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"Another embodiment of a semiconductor device constructed according to aspects of the present disclosure includes an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; (2) a first gate interposing the first source/drain regions; and (3) first spacers on opposing sides of the first gate and each extending from the first gate to a first width. A second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; (2) a second gate interposing the second source/drain regions; and (3) second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different." Cheng817 ¶ [0035]. "In another embodiment, a semiconductor device constructed according to aspects of the present disclosure includes an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe; (2) second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and (3) second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe." Cheng817 ¶ [0036]. "The present disclosure also introduces a method of manufacturing semiconductor device. In one embodiment, the method includes forming an isolation region located in a substrate, forming an NMOS device located partially over a surface of the substrate, and forming a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface; and (2) first source/drain regions extending from the surface. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface." Cheng817 ¶ [0037].

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"Referring now to FIGS. 4a-4j for sectional views of another embodiment of a method for making semiconductor devices 401a and 401b with high drive current. The semiconductor device 401a may be a P-type MOS device and the semiconductor device 401b may be an N-type MOS device. In FIG. 4a, gate dielectric 406a and 406b are formed over a substrate 402 for devices 401a and 401b, respectively, and electrically isolated from one another by isolation structures 404. The isolation structures 404 may be shallow trench isolation (STI) structures. Gate electrodes 408a and 408b are formed over the gate dielectric layer, and hard masks 410a and 410b are formed over the gate electrodes 408a and 408b, respectively." Cheng817 ¶ [0056]. "The substrate 402 may include silicon, silicon-on-insulation (SOI), germanium, germanium-on-insulation (GOI), gallium arsenide (GaAs), strained silicon, silicon germanium, silicon carbide, diamond, and/or other materials. In one embodiment, the substrate 402 may be substantially similar to the substrate 104 and 205 described above. In another embodiment, the substrate 402 may include an air gap to provide insulation for the microelectronic device 400. For example, a 'silicon-on-nothing' (SON) structure may include the semiconductor device(s) 401a and 401b each having a thin insulation layer formed by air and/or other insulators. The gate dielectric 406a and 406b and the gate electrode 408a and 408b may be substantially similar in composition to the gate dielectric layer 120 and 160 and the gate electrode 124 and 164 shown in FIG. 1 and described above." Cheng817 ¶ [0057]. "Alternatively, the gate dielectric 406a and 406b and/or gate electrode 408a and 408b may include multiple layers such as an oxide layer, a high-k dielectric later, a polysilicon layer, strained silicon, silicon germanium, silicon carbide, and/or other material layers. Other materials for the gate dielectric 406a and 406b and the gate electrode 408a and 408b may include titanium (Ti), tantalum (Ta), molybdenum (Mo), cobalt (Co), tungsten (W), titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (W_N), molybdenum silicide (MoSi), tungsten silicide (WSi), cobalt silicide (CoSi), nickel silicide ($NiSi_x$), metal silicides, germanium nanowire, silicon nanowire, and/or other materials. The gate dielectric 406a and 407b may comprise a SiO_2 layer and/or nitrided SiO_2. Alternatively, the gate dielectric 406a and 406b material may be replaced by the high-k dielectric. In one embodiment, the high-k layer may be formed from a variety of different materials, such as tantalum nitride, titanium nitride, tantoxide (Ta_2O_5), hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2), hafnium silicon oxy-nitride (HfSiON), hafnium silicide ($HfSi_x$), hafnium silicon nitride ($HfSi_xN_y$), hafnium aluminum dioxide ($HfAlO_2$), nickel silicide ($NiSi_x$), and/or other suitable materials using ALD, CVD, PECVD, evaporation, and/or other methods. Generally, the high-k layer may have a thickness between approximately 2 and 500 Angstroms. With some materials, such as HfSiON, the high-k layer of gate electrode 408a and 408b may be blanket deposited on the surface of substrate 402, while other materials may be selectively deposited. Alternatively, it may be desirable to blanket deposit some materials,

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including HfSiON, in some fabrication processes, while selectively depositing the same materials in other processes." Cheng817 ¶ [0058]. "The hard masks 410a and 410b may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), titanium nitride (TiN), silicon carbide (SiC), carbide, low-k dielectric, air, and/or other materials. The hard mask 410a and 410b may be formed by lithography, plasma etch, rapid thermal oxidation (RTO), CVD, PECVD, ALD, PVD, and/or other processing techniques now known or to be developed." Cheng817 ¶ [0059]. "The lightly doped regions 422a and 422b may include P-type and N-type dopants for the devices 401a and 401b, respectively. The doped regions 422a and 422b may be formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The doped regions 422a and 422b may also include lightly doped regions (LDD) and/or heavily doped regions in one embodiment. The doped regions 422a and 422b may include impurities such as phosphorous, boron, antimony, arsenic, and/or other materials. For example, the formation of the doped regions 422a and 422b by ion implantation may include an ion implant energy ranging between about 1 KeV and about 100 KeV and the dose of ion implantation of may range between about 1×10^{13} cm^{-2} and about 5×10^{16} cm^{-2}." Cheng817 ¶ [0060]. "In FIG. 4b, sidewall dielectric layers 412 and 414, and spacer material 415 are disposed over the semiconductor device(s) 410a and 401b and are subsequently processed, such as by etching, to form sidewall dielectric structures 412a, 412b, 414a and 414b, and spacers 415a and 415b, as shown in FIG. 4c. Note the dielectric structures 714a and 714b are substantially L-shaped. A dummy spacer layer 416 is formed over the semiconductor devices 401a and 401b. Low temperature processing, such as using a temperature less than 600° C., to form the sidewall dielectric and spacer materials is preferred to reduce lightly doped drain diffusion." Cheng817 ¶ [0061]. "The sidewall dielectric layers 412 and 414 may be a liner oxide layer and a nitride layer formed over the devices by deposition. In particular, the sidewall dielectric layers 412 and 414 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), polymer and/or other materials. The sidewall dielectric layers 412 and 414 may also include multiple layers and/or may include a single layer, in one embodiment. The sidewall dielectric layers 412 and 414 may be formed by RTO, CVD, PVD, PECVD, ALD, CMP, chemical etching, plasma etching, and/or other processing techniques. The spacer material 415 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), polymer and/or other materials. The spacer material 415 may also include multiple layers and/or may include a single layer, in one embodiment. The spacer material 415 may be formed by RTO,

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CVD, PVD, PECVD, ALD, CMP, chemical etching, plasma etching, and/or other processing techniques. The sidewall dielectric structures 412a, 412b, 414a and 414b, and spacers 415a and 415b may be formed by chemical etching, plasma etching, CMP, focused ion beam (FIB), and/or other processing techniques." Cheng817 ¶ [0062]. "In FIG. 4d, the dummy spacer material 416 is processed to form the dummy spacers 416a and 416b. The dummy spacer material 416 may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), silicon oxy-carbide (SiOC), polymer, and/or other materials. The spacer material 416 may be formed by CVD, PECVD, ALD, spin-on coating, and/or other processing techniques, for example, and the dummy spacers 416a and 416b may be formed by chemical etch, plasma etch, CMP, focused ion beam (FIB), and/or other processing techniques. In FIG. 4d, a photoresist 417b is provided over the device 401b so that portions of the dummy spacer material 416a is removed from the device 401a, and recessed source and drain regions 418a are also formed in the substrate 402 on either side of the gate structure of the device 401a." Cheng817 ¶ [0063]. "In FIG. 4f, a photoresist 421a is disposed over the semiconductor device 401a. Further, the dummy spacer 716b is removed from the device 401b. The spacer material 416b may be removed by chemical etch, plasma etch, CMP focused ion beam (FIB), and/or other processing techniques. Deeper and more heavily doped regions 428b are also formed in the substrate 402 in the semiconductor device 401b. The doped regions 428b may include N-type impurities, and may be formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The doped regions 428b may include heavy doped regions forming the source/drain regions of the semiconductor device 701b. The ion implantation may include an ion implant energy ranging between about 5 KeV and about 100 KeV and the dose of ion implantation of may range between about 1×10^{14} cm^{-2} and about 5×10^{18} cm^{-2}." Cheng817 ¶ [0066]. "In FIG. 4g, the photoresist 421a is removed from the device 401a. Further, the hard masks 410a and 410b are removed from the semiconductor devices 401a and 401b. The photoresist 421a may be removed by plasma etch and/or chemical etch. For example, the mask 421a may be removed by an oxygen (O_2) containing plasma environment. The hard masks 410a and 410b may be removed by chemical and/or plasma etch. For example, the hard masks 410a and 410b may be removed by hot phosphoric (H_2PO_4) acid, ammonium hydroxide ($NH_{40}H$), hydrochloric acid (HCl), hydrofluoric acid (HF), sulfuric acid (H_2SO_4), and/or other etchant chemicals. The hard masks 420a and 420b may also be removed by ion bombardment in an inert plasma comprising argon, hydrogen, xenon, and/or other gases." Cheng817 ¶ [0067].

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"In FIG. 4i, the photoresist 421b is removed from the device 401b, and salicided contacts 432a and 432b are formed over the gate, source and drain of the devices 401a and 401b. The salicided contacts 432a and 432b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 732a and 732b may also include an anneal. The salicided contacts 732a and 732b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0069]. "Further in FIG. 4j, an etch stop layer 430a and 430b are formed over the semiconductor device(s) 401a and 401b. The etch stop layer 430a and 430b may include silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), and/or other materials. In one embodiment, the etch stop layer 430a and 430b may be substantially similar in composition to the etch stop layer 180 described above. Alternatively, the etch stop layer 430a and 430b may include a stress level that may range between about +0.001 and about +50 GPa for tensile film and between about −0.001 and about −50 GPa for compressive film. The etch stop layer 430a and 430b may be formed by CVD, ALD, PECVD, PDL, spin-on coating, and/or other techniques." Cheng817 ¶ [0070]. "Subsequent processing steps may be performed to the semiconductor devices 401a and 401b such as metallization, testing and packaging, etc." Cheng817 ¶ [0071]. "Referring now to FIGS. 5a-i for another embodiment of a method for manufacturing a microelectronic device 500 with high drive current. In FIG. 5a, gate structures including a gate dielectric 506a and 506b and gate electrodes 508a and 508b are formed for semiconductor devices 501a and 501b, respectively. Gate electrodes 508a and 508b may be pre-doped with appropriate P-type and N-type dopants, respectively. Hard masks 510a and 510b are also formed over each gate structure. Further, shallow doped drain and source regions 522a and 522b are formed on either sides of the gate structures of each device 501a and 501b. Isolation structures 504 are formed in the substrate 502 to electrically isolate the devices 501a and 501b." Cheng817 ¶ [0072]. "The substrate 502 may include silicon, silicon-on-insulation (SOI), germanium, germanium-on-insulation (GOI), gallium arsenide (GaAs), strained silicon, diamond, and/or other materials. In another embodiment, the substrate 502 may include an air gap to provide insulation for the microelectronic device 500. For example, a 'silicon-on-nothing' (SON) structure may include the semiconductor devices 501a and 501b each having a thin insulation layer formed by air and/or other insulator. The gate dielectric 506a and 506b and the gate electrode 508a and 508b, in one embodiment, may be substantially similar in composition to the gate dielectric layer 120 and 160 and the gate electrode 124 and 164 shown in FIG. 1. Alternatively, the gate dielectric 506a and

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506b and/or gate electrode 508a and 508b may include multiple layers such as an oxide layer, a high-k dielectric later, a polysilicon layer, strained silicon, silicon germanium, silicon carbide, and/or other material layers. Other materials for the gate dielectric 506a and 506b and the gate electrode 508a and 508b may include titanium (Ti), tantalum (Ta), molybdenum (Mo), cobalt (Co), tungsten (W), titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (W_N), molybdenum silicide (MoSi), tungsten silicide (WSi), cobalt silicide (CoSi), nickel silicide ($NiSi_x$), metal silicides, germanium nanowire, silicon nanowire, and/or other materials. The gate dielectric 506a and 506b may comprise a SiO_2 layer and/or nitrided SiO_2. In one embodiment, the high-k layer may be formed from a variety of different materials, such as tantalum nitride, titanium nitride, tantoxide (Ta_2O_5), hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2), hafnium silicon oxy-nitride (HfSiON), hafnium silicide ($HfSi_x$), hafnium silicon nitride ($HfSi_xN_y$), hafnium aluminum dioxide ($HfAlO_2$), nickel silicide ($NiSi_x$), and/or other suitable materials using ALD, CVD, PECVD, evaporation, and/or other methods. With some materials, such as HfSiON, the high-k layer of gate electrode 508a and 508b may be blanket deposited on the surface of substrate 502, while other materials may be selectively deposited. Alternatively, it may be desirable to blanket deposit some materials, including HfSiON, in some fabrication processes, while selectively depositing the same materials in other processes." Cheng817 ¶ [0073]. "The hard masks 510a and 510b may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), titanium nitride (TiN), silicon carbide (SiC), carbide, low-k dielectric, air, and/or other materials. The hard mask 510a and 510b may be formed by lithography, plasma etch, rapid thermal oxidation (RTO), CVD, PECVD, ALD, PVD, and/or processing techniques." Cheng817 ¶ [0074]. "The doped source and drain regions 522a and 522b may include N-type and/or P-type doped regions formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The doped regions 522a and 522b may be lightly doped drains (LDD) and may include impurities such as phosphorous, boron, antimony, arsenic, and/or other materials." Cheng817 ¶ [0075]. "In FIG. 5b, sidewall dielectric layers 512 and 514, and a spacer material 515 are formed over the semiconductor devices 510a and 501b, preferably using a low temperature process to reduce LDD diffusion. The sidewall dielectric layers 512 and 514 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), polymer and/or other materials. The spacer material 515 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), polymer and/or other materials. For example, dielectric layers 512 and 514 may comprise a liner oxide layer and a nitride layer, and the spacer material 515 may comprise an oxide material. The sidewall dielectric layers 512 and 514 and

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spacer layer 515 may be formed by RTO, CVD, PVD, PECVD, ALD, CMP, chemical etching, plasma etching, and/or other processing techniques." Cheng817 ¶ [0076] "In FIG. 5c, the sidewall dielectric layers 512 and 514, and a spacer material 515 are subsequently processed forming sidewall dielectric 512a, 512b, 514a and 514b, and spacers 515a and 515b. The sidewall dielectric 512a, 512b, 514a and 514b, and spacers 515a and 515b may be formed by chemical etching, plasma etching, CMP, focused ion beam (FIB), and/or other processing techniques." Cheng817 ¶ [0077]. "Further, a dummy spacer material 516 is formed over the semiconductor devices 501a and 501b, and subsequently processed forming the dummy spacers 516a and 516b. The dummy spacer material 516 may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxy-nitride (SiON), silicon oxy-carbide (SiOC), polymer, and/or other materials. The spacer material 516 may be formed by CVD, PECVD, ALD, spin-on coating, and/or other processing techniques, and may be formed by chemical etch, plasma etch, CMP, focused ion beam (FIB), and/or other processing techniques." Cheng817 ¶ [0078]. "In FIG. 5f, a photoresist 521a is disposed over the semiconductor device 501a for processing of the semiconductor device 501b. The dummy spacer material 516b is removed from the device 501b, and deeper source and drain doped regions 528b are formed. The spacer material 516b may be removed by chemical etch, plasma etch, CMP focused ion beam (FIB), and/or other processing techniques, for example. The doped regions 528b may include N-type impurities, and may be formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The ion implantation process may use an ion implant energy ranging between about 5 KeV and about 100 KeV and the dose of ion implantation of may range between about 1×10^{14} cm^{-2} and about 5×10^{18} cm^{-2}, for example." Cheng817 ¶ [0081]. "In FIG. 5g, the photoresist 521a is removed from the device 501. Further, the hard masks 510a and 510b are removed from the gate structures of the semiconductor devices 501a and 501b. The hard masks 510a and 510b may be removed from the semiconductor devices by chemical and/or plasma etch. For example, the hard masks 510a and 510b may be removed by hot phosphoric (H_2PO_4) acid, ammonium hydroxide (NH_4OH), hydrochloric acid (HCl), hydrofluoric acid (HF), sulfuric acid (H_2SO_4), and/or other chemicals. The hard mask 510a and 510b may also be removed by ion bombardment in an inert plasma comprising argon, hydrogen, xenon, and/or other gases." Cheng817 ¶ [0082].

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"Because the deeper doped source and drain regions were doped in-situ (FIG. 5g), a process of source and drain implantation such as that shown in FIG. 4h is not required. Therefore, salicided contacts 532a and 532b are formed for the gate, source and drains of the devices 501a and 501b, respectively, as shown in FIG. 5h. The salicided contacts 532a and 532b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 532a and 532b may also include an anneal. The salicided contacts 532a and 532b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0083]. "In FIG. 5i, etch stop layer 530a and 530b are formed over the semiconductor devices 501a and 501b. The etch stop layer 530a and 530b may include silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), and/or other materials. Alternatively, the etch stop layer 530a and 530b may include a stress level that may range between about +0.001 and about +50 GPa for tensile film and between about −0.001 and about −50 GPa for compressive film. The etch stop layer 530a-b may be formed by CVD, ALD, PECVD, PDL, spin-on coating, and/or other techniques." Cheng817 ¶ [0084]. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

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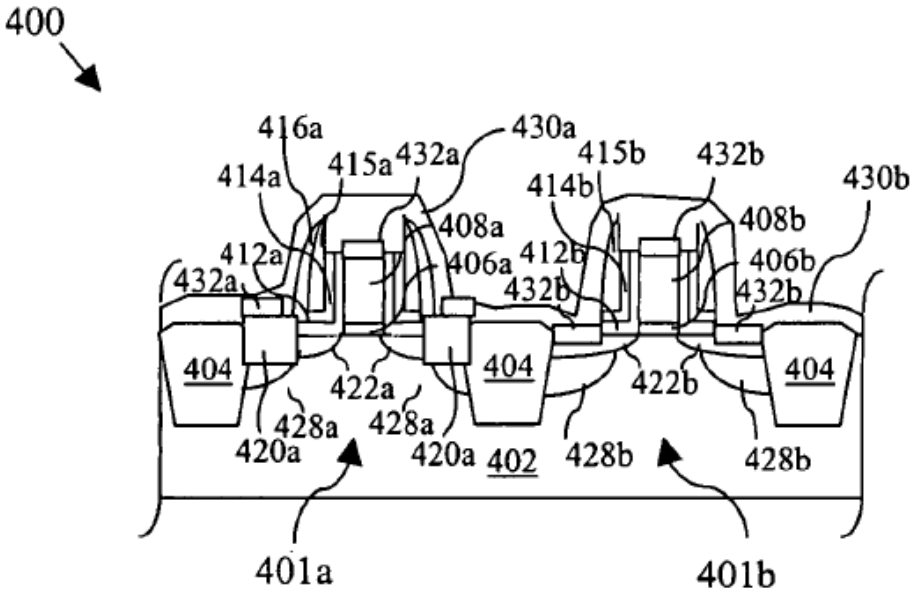
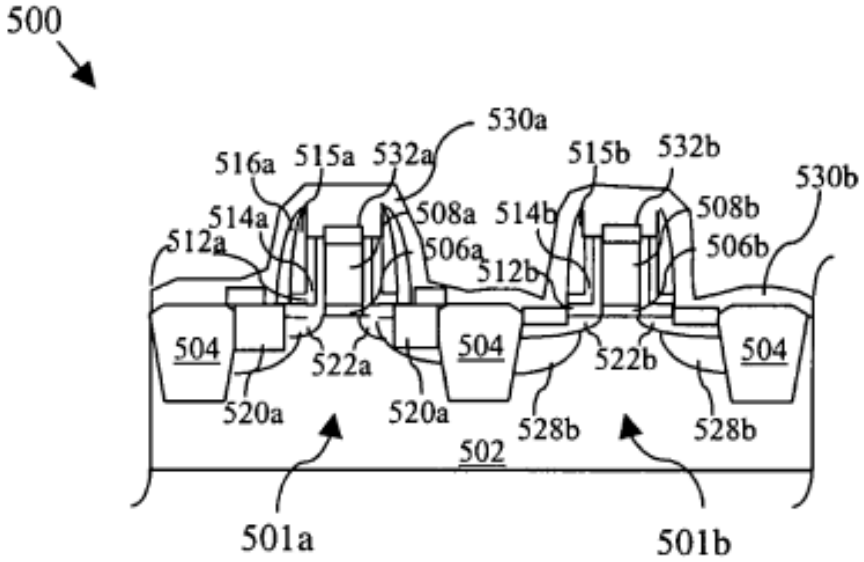
11[b] a second gate insulating film formed on a second active region in the semiconductor substrate,
Cheng817 discloses this feature. For example, Cheng817 discloses a gate dielectric 406b formed on the NMOS active region of a substrate 402. *See, e.g.*, the following:  Cheng817 Fig. 4j (showing gate dielectric 406b on the NMOS active region of substrate 402).  Cheng817 Fig. 5i (showing gate dielectric 506b on the NMOS active region of a substrate 502).

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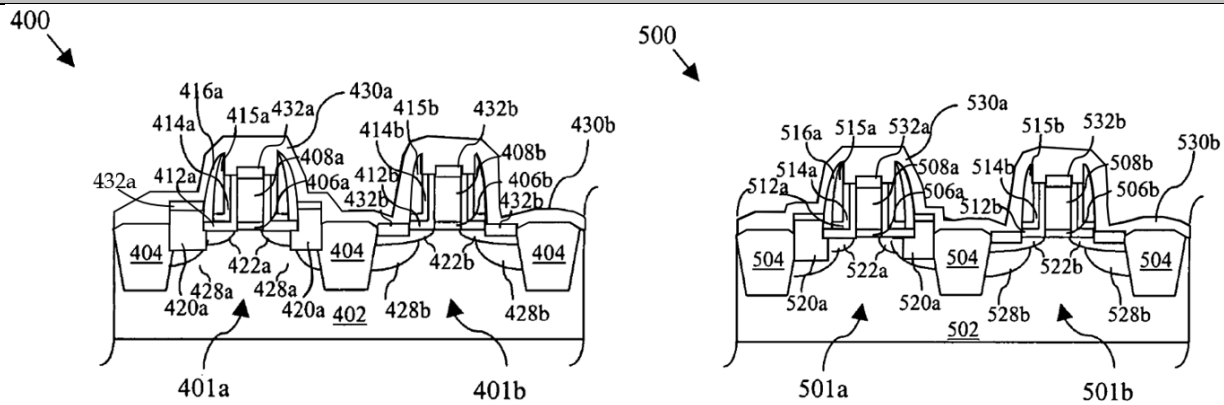

Figure A **Figure B**

(Cheng817, Figs. 4j, 5i (corrected))

"Referring now to FIGS. 4a-4j for sectional views of another embodiment of a method for making semiconductor devices 401a and 401b with high drive current. The semiconductor device 401a may be a P-type MOS device and the semiconductor device 401b may be an N-type MOS device. In FIG. 4a, gate dielectric 406a and 406b are formed over a substrate 402 for devices 401a and 401b, respectively, and electrically isolated from one another by isolation structures 404. The isolation structures 404 may be shallow trench isolation (STI) structures. Gate electrodes 408a and 408b are formed over the gate dielectric layer, and hard masks 410a and 410b are formed over the gate electrodes 408a and 408b, respectively."

Cheng817 ¶ [0056].

"The substrate 402 may include silicon, silicon-on-insulation (SOI), germanium, germanium-on-insulation (GOI), gallium arsenide (GaAs), strained silicon, silicon germanium, silicon carbide, diamond, and/or other materials. In one embodiment, the substrate 402 may be substantially similar to the substrate 104 and 205 described above. In another embodiment, the substrate 402 may include an air gap to provide insulation for the microelectronic device 400. For example, a 'silicon-on-nothing' (SON) structure may include the semiconductor device(s) 401a and 401b each having a thin insulation layer formed by air and/or other insulators. The gate dielectric 406a and 406b and the gate electrode 408a and 408b may be substantially similar in composition to the gate dielectric layer 120 and 160 and the gate electrode 124 and 164 shown in FIG. 1 and described above."

Cheng817 ¶ [0057].

"Alternatively, the gate dielectric 406a and 406b and/or gate electrode 408a and 408b may include multiple layers such as an oxide layer, a high-k dielectric later, a polysilicon layer, strained silicon, silicon germanium, silicon carbide, and/or other material layers. Other materials for the gate dielectric 406a and 406b and the gate electrode 408a and 408b may include titanium (Ti), tantalum (Ta), molybdenum (Mo), cobalt (Co), tungsten (W), titanium nitride (TiN),

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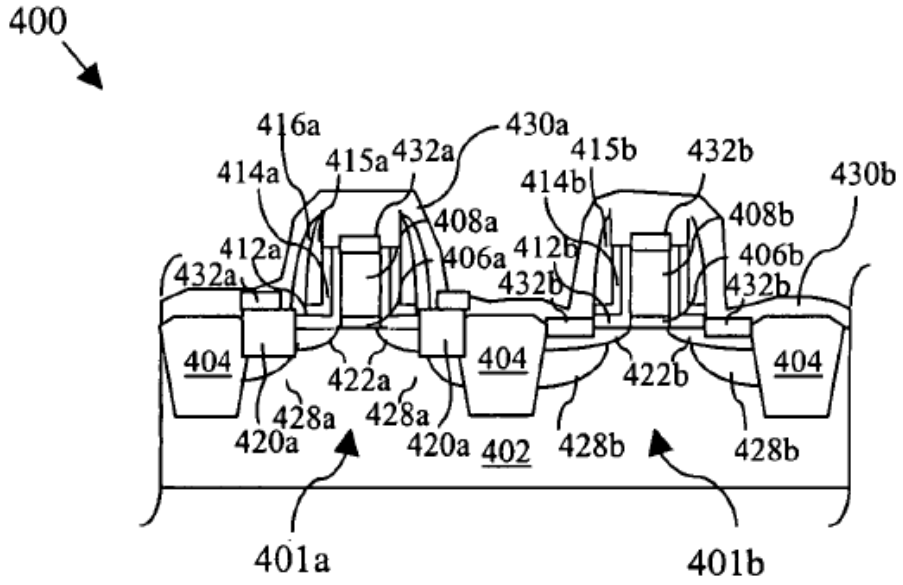
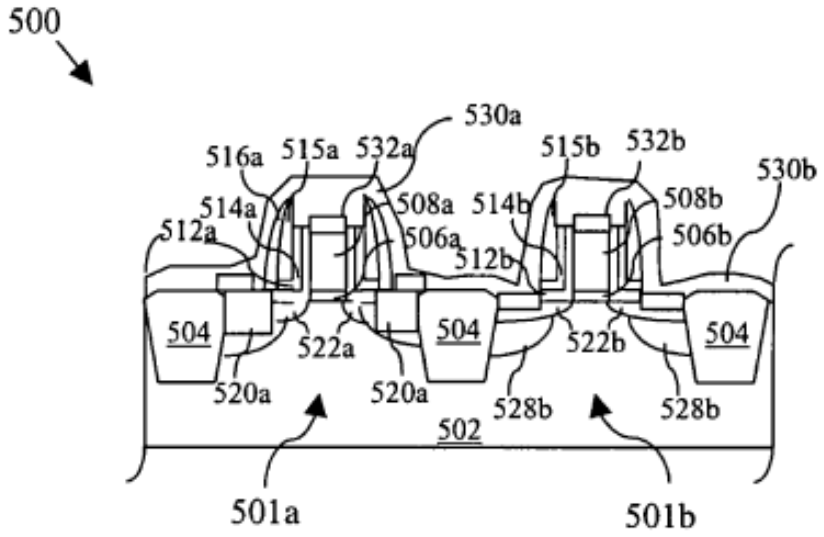
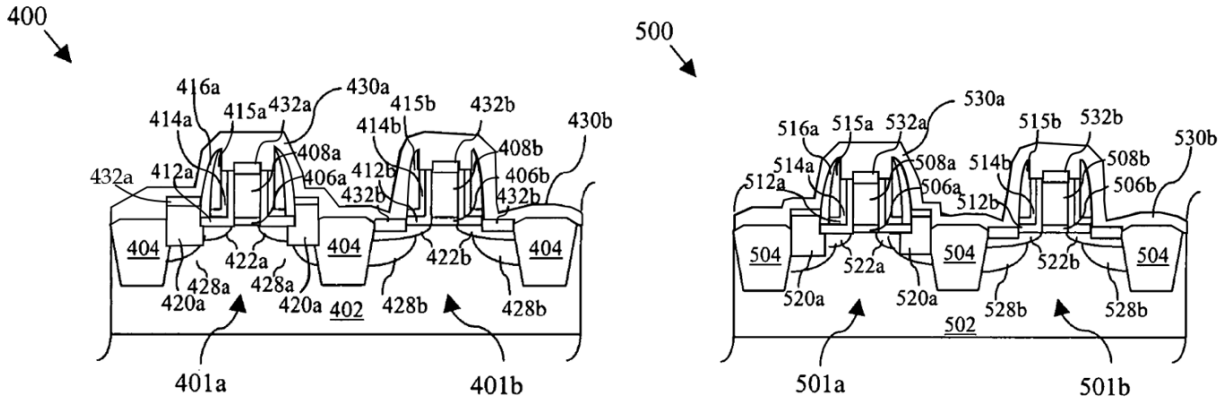
tantalum nitride (TaN), tungsten nitride (W_N), molybdenum silicide (MoSi), tungsten silicide (WSi), cobalt silicide (CoSi), nickel silicide ($NiSi_x$), metal silicides, germanium nanowire, silicon nanowire, and/or other materials. The gate dielectric 406a and 407b may comprise a SiO_2 layer and/or nitrided SiO_2. Alternatively, the gate dielectric 406a and 406b material may be replaced by the high-k dielectric. In one embodiment, the high-k layer may be formed from a variety of different materials, such as tantalum nitride, titanium nitride, tantoxide (Ta_2O_5), hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2), hafnium silicon oxy-nitride (HfSiON), hafnium silicide ($HfSi_x$), hafnium silicon nitride ($HfSi_xN_y$), hafnium aluminum dioxide ($HfAlO_2$), nickel silicide ($NiSi_x$), and/or other suitable materials using ALD, CVD, PECVD, evaporation, and/or other methods. Generally, the high-k layer may have a thickness between approximately 2 and 500 Angstroms. With some materials, such as HfSiON, the high-k layer of gate electrode 408a and 408b may be blanket deposited on the surface of substrate 402, while other materials may be selectively deposited. Alternatively, it may be desirable to blanket deposit some materials, including HfSiON, in some fabrication processes, while selectively depositing the same materials in other processes." Cheng817 ¶ [0058]. "Referring now to FIGS. 5a-i for another embodiment of a method for manufacturing a microelectronic device 500 with high drive current. In FIG. 5a, gate structures including a gate dielectric 506a and 506b and gate electrodes 508a and 508b are formed for semiconductor devices 501a and 501b, respectively. Gate electrodes 508a and 508b may be pre-doped with appropriate P-type and N-type dopants, respectively. Hard masks 510a and 510b are also formed over each gate structure. Further, shallow doped drain and source regions 522a and 522b are formed on either sides of the gate structures of each device 501a and 501b. Isolation structures 504 are formed in the substrate 502 to electrically isolate the devices 501a and 501b." Cheng817 ¶ [0072]. "The substrate 502 may include silicon, silicon-on-insulation (SOI), germanium, germanium-on-insulation (GOI), gallium arsenide (GaAs), strained silicon, diamond, and/or other materials. In another embodiment, the substrate 502 may include an air gap to provide insulation for the microelectronic device 500. For example, a 'silicon-on-nothing' (SON) structure may include the semiconductor devices 501a and 501b each having a thin insulation layer formed by air and/or other insulator. The gate dielectric 506a and 506b and the gate electrode 508a and 508b, in one embodiment, may be substantially similar in composition to the gate dielectric layer 120 and 160 and the gate electrode 124 and 164 shown in FIG. 1. Alternatively, the gate dielectric 506a and 506b and/or gate electrode 508a and 508b may include multiple layers such as an oxide layer, a high-k dielectric later, a polysilicon layer, strained silicon, silicon germanium, silicon carbide, and/or other material layers. Other materials for the gate dielectric 506a and 506b and the gate electrode 508a and 508b may include titanium (Ti), tantalum (Ta), molybdenum (Mo), cobalt (Co), tungsten (W), titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (W_N), molybdenum silicide (MoSi), tungsten silicide (WSi), cobalt silicide (CoSi), nickel silicide ($NiSi_x$), metal silicides, germanium nanowire, silicon nanowire, and/or other materials. The gate

Exemplary Disclosures
dielectric 506a and 506b may comprise a SiO_2 layer and/or nitrided SiO_2. In one embodiment, the high-k layer may be formed from a variety of different materials, such as tantalum nitride, titanium nitride, tantoxide (Ta_2O_5), hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2), hafnium silicon oxy-nitride (HfSiON), hafnium silicide ($HfSi_x$), hafnium silicon nitride ($HfSi_xN_y$), hafnium aluminum dioxide ($HfAlO_2$), nickel silicide ($NiSi_x$), and/or other suitable materials using ALD, CVD, PECVD, evaporation, and/or other methods. With some materials, such as HfSiON, the high-k layer of gate electrode 508a and 508b may be blanket deposited on the surface of substrate 502, while other materials may be selectively deposited. Alternatively, it may be desirable to blanket deposit some materials, including HfSiON, in some fabrication processes, while selectively depositing the same materials in other processes." Cheng817 ¶ [0073]. *See also*, *e.g.*, Cheng817 ¶ [0060], ¶ [0066]. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
11[c] a second gate electrode formed on the second gate insulating film,
Cheng817 discloses this feature. For example, Cheng817 discloses a NMOS gate 408b formed on the NMOS gate dielectric 406b. *See, e.g.*, the following:    Cheng817 Fig. 4j (showing NMOS gate 408b formed on the NMOS gate dielectric 406b).

Exemplary Disclosures
 Cheng817 Fig. 5i (showing NMOS gate 508b formed on the NMOS gate dielectric 506b).  **Figure A** **Figure B** **(Cheng817, Figs. 4j, 5i (corrected))**

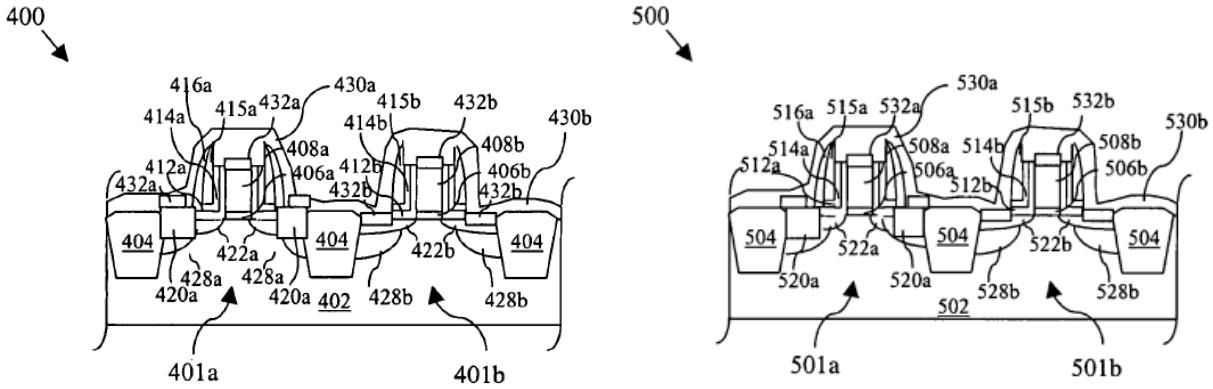
"Referring now to FIGS. 4a-4j for sectional views of another embodiment of a method for making semiconductor devices 401a and 401b with high drive current. The semiconductor device 401a may be a P-type MOS device and the semiconductor device 401b may be an N-type MOS device. In FIG. 4a, gate dielectric 406a and 406b are formed over a substrate 402 for devices 401a and 401b, respectively, and electrically isolated from one another by isolation structures 404. The isolation structures 404 may be shallow trench isolation (STI) structures. Gate electrodes 408a and 408b are formed over the gate dielectric layer, and hard masks 410a and 410b are formed over the gate electrodes 408a and 408b, respectively."

Cheng817 ¶ [0056].

Exemplary Disclosures
"The substrate 402 may include silicon, silicon-on-insulation (SOI), germanium, germanium-on-insulation (GOI), gallium arsenide (GaAs), strained silicon, silicon germanium, silicon carbide, diamond, and/or other materials. In one embodiment, the substrate 402 may be substantially similar to the substrate 104 and 205 described above. In another embodiment, the substrate 402 may include an air gap to provide insulation for the microelectronic device 400. For example, a 'silicon-on-nothing' (SON) structure may include the semiconductor device(s) 401a and 401b each having a thin insulation layer formed by air and/or other insulators. The gate dielectric 406a and 406b and the gate electrode 408a and 408b may be substantially similar in composition to the gate dielectric layer 120 and 160 and the gate electrode 124 and 164 shown in FIG. 1 and described above." Cheng817 ¶ [0057]. "Alternatively, the gate dielectric 406a and 406b and/or gate electrode 408a and 408b may include multiple layers such as an oxide layer, a high-k dielectric later, a polysilicon layer, strained silicon, silicon germanium, silicon carbide, and/or other material layers. Other materials for the gate dielectric 406a and 406b and the gate electrode 408a and 408b may include titanium (Ti), tantalum (Ta), molybdenum (Mo), cobalt (Co), tungsten (W), titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (W_N), molybdenum silicide (MoSi), tungsten silicide (WSi), cobalt silicide (CoSi), nickel silicide ($NiSi_x$), metal silicides, germanium nanowire, silicon nanowire, and/or other materials. The gate dielectric 406a and 407b may comprise a SiO_2 layer and/or nitrided SiO_2. Alternatively, the gate dielectric 406a and 406b material may be replaced by the high-k dielectric. In one embodiment, the high-k layer may be formed from a variety of different materials, such as tantalum nitride, titanium nitride, tantoxide (Ta_2O_5), hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2), hafnium silicon oxy-nitride (HfSiON), hafnium silicide ($HfSi_x$), hafnium silicon nitride ($HfSi_xN_y$), hafnium aluminum dioxide ($HfAlO_2$), nickel silicide ($NiSi_x$), and/or other suitable materials using ALD, CVD, PECVD, evaporation, and/or other methods. Generally, the high-k layer may have a thickness between approximately 2 and 500 Angstroms. With some materials, such as HfSiON, the high-k layer of gate electrode 408a and 408b may be blanket deposited on the surface of substrate 402, while other materials may be selectively deposited. Alternatively, it may be desirable to blanket deposit some materials, including HfSiON, in some fabrication processes, while selectively depositing the same materials in other processes." Cheng817 ¶ [0058].

Exemplary Disclosures
"Referring now to FIGS. 5a-i for another embodiment of a method for manufacturing a microelectronic device 500 with high drive current. In FIG. 5a, gate structures including a gate dielectric 506a and 506b and gate electrodes 508a and 508b are formed for semiconductor devices 501a and 501b, respectively. Gate electrodes 508a and 508b may be pre-doped with appropriate P-type and N-type dopants, respectively. Hard masks 510a and 510b are also formed over each gate structure. Further, shallow doped drain and source regions 522a and 522b are formed on either sides of the gate structures of each device 501a and 501b. Isolation structures 504 are formed in the substrate 502 to electrically isolate the devices 501a and 501b." Cheng817 ¶ [0072]. "The substrate 502 may include silicon, silicon-on-insulation (SOI), germanium, germanium-on-insulation (GOI), gallium arsenide (GaAs), strained silicon, diamond, and/or other materials. In another embodiment, the substrate 502 may include an air gap to provide insulation for the microelectronic device 500. For example, a 'silicon-on-nothing' (SON) structure may include the semiconductor devices 501a and 501b each having a thin insulation layer formed by air and/or other insulator. The gate dielectric 506a and 506b and the gate electrode 508a and 508b, in one embodiment, may be substantially similar in composition to the gate dielectric layer 120 and 160 and the gate electrode 124 and 164 shown in FIG. 1. Alternatively, the gate dielectric 506a and 506b and/or gate electrode 508a and 508b may include multiple layers such as an oxide layer, a high-k dielectric later, a polysilicon layer, strained silicon, silicon germanium, silicon carbide, and/or other material layers. Other materials for the gate dielectric 506a and 506b and the gate electrode 508a and 508b may include titanium (Ti), tantalum (Ta), molybdenum (Mo), cobalt (Co), tungsten (W), titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (W_N), molybdenum silicide (MoSi), tungsten silicide (WSi), cobalt silicide (CoSi), nickel silicide ($NiSi_x$), metal silicides, germanium nanowire, silicon nanowire, and/or other materials. The gate dielectric 506a and 506b may comprise a SiO_2 layer and/or nitrided SiO_2. In one embodiment, the high-k layer may be formed from a variety of different materials, such as tantalum nitride, titanium nitride, tantoxide (Ta_2O_5), hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2), hafnium silicon oxy-nitride (HfSiON), hafnium silicide ($HfSi_x$), hafnium silicon nitride ($HfSi_xN_y$), hafnium aluminum dioxide ($HfAlO_2$), nickel silicide ($NiSi_x$), and/or other suitable materials using ALD, CVD, PECVD, evaporation, and/or other methods. With some materials, such as HfSiON, the high-k layer of gate electrode 508a and 508b may be blanket deposited on the surface of substrate 502, while other materials may be selectively deposited. Alternatively, it may be desirable to blanket deposit some materials, including HfSiON, in some fabrication processes, while selectively depositing the same materials in other processes." Cheng817 ¶ [0073]. Additionally, under Plaintiff's apparent interpretation of the claim language, the claimed "second gate electrode" may include a silicide film. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 35-43. Although TSMC does not necessarily agree with such an interpretation, Cheng817 further discloses this element under this interpretation, as shown below.

Exemplary Disclosures
For example, Cheng817 discloses silicide 432b formed on NMOS gate electrode 408b. *See, e.g.*, the following:



Cheng817 Figs. 4j, 5i.

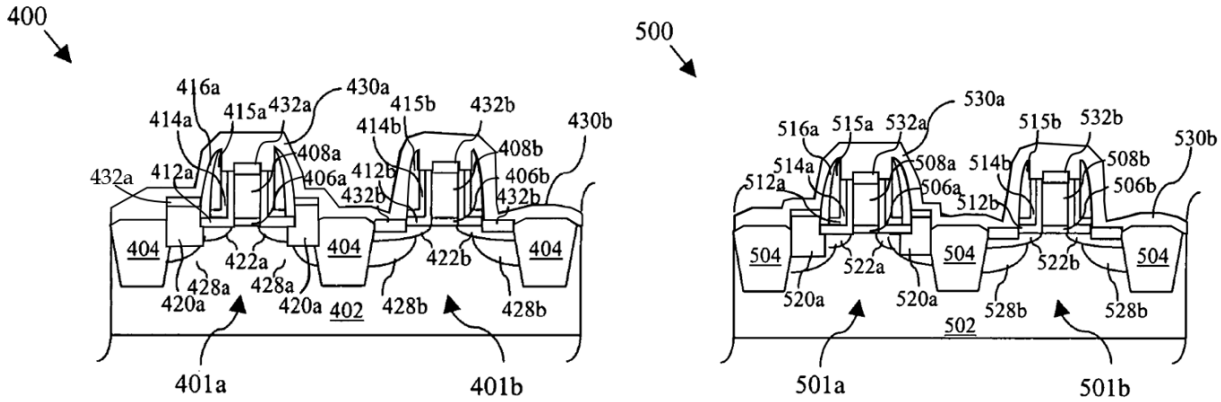
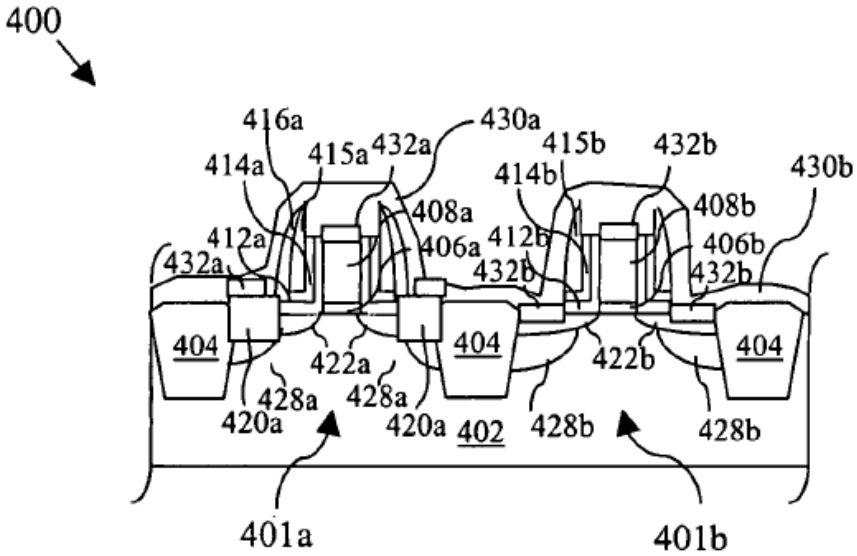


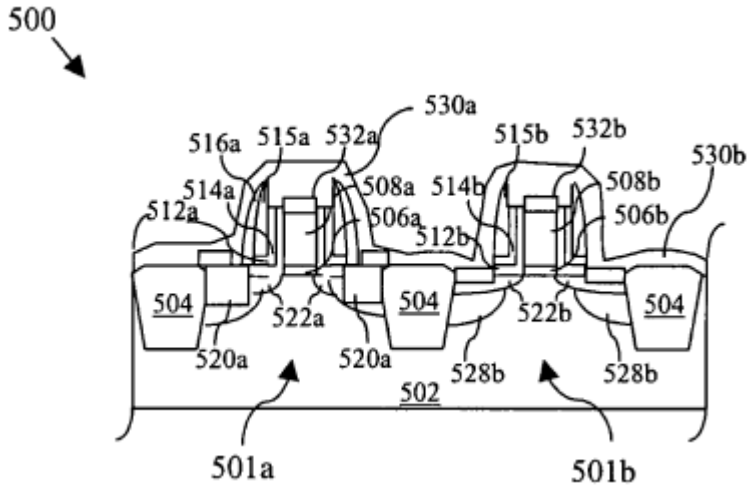
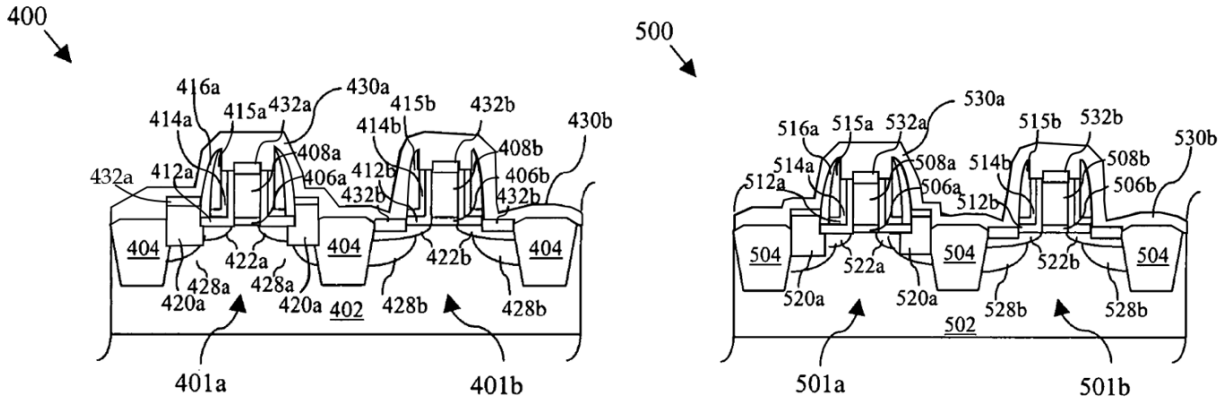
Figure A **Figure B**

(Cheng817, Figs. 4j, 5i (corrected))

"In FIG. 4i, the photoresist 421b is removed from the device 401b, and salicided contacts 432a and 432b are formed over the gate, source and drain of the devices 401a and 401b. The salicided contacts 432a and 432b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 732a and 732b may also include an anneal. The salicided contacts 732a and 732b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques."

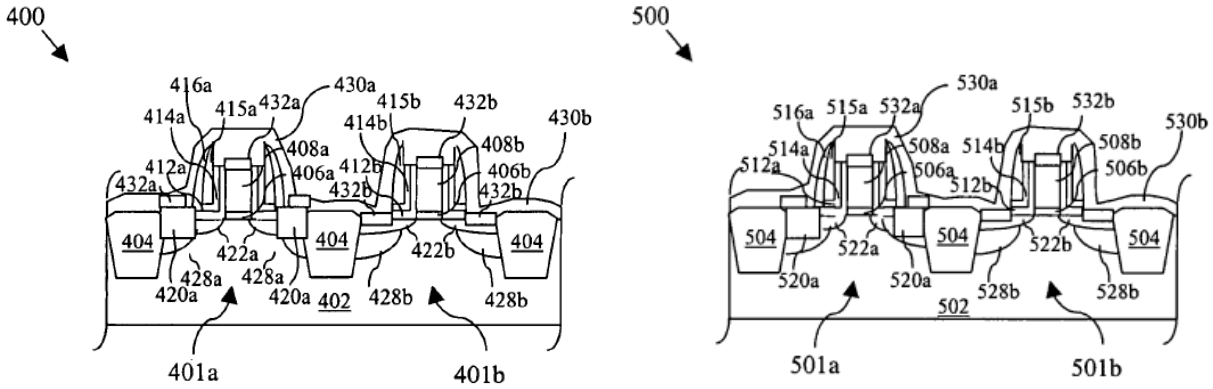
Cheng817 ¶ [0069].

Exemplary Disclosures
"Because the deeper doped source and drain regions were doped in-situ (FIG. 5g), a process of source and drain implantation such as that shown in FIG. 4h is not required. Therefore, salicided contacts 532a and 532b are formed for the gate, source and drains of the devices 501a and 501b, respectively, as shown in FIG. 5h. The salicided contacts 532a and 532b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 532a and 532b may also include an anneal. The salicided contacts 532a and 532b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0083]. *See also, e.g.,* Cheng817 ¶ [0003], ¶ [0019], ¶ [0041], ¶ [0052], ¶ [0058], ¶ [0069], ¶ [0073], ¶ [0083], ¶ [0087], ¶ [0097], ¶ [0099], ¶ [0101], FIGS. 1, 2, 3n, 4i-4j, 5h-5i, 6h-6i, 7. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
11[d] a second sidewall spacer formed on a side surface of the second gate electrode,
Cheng817 discloses this feature. For example, Cheng817 discloses sidewall spacers 412b, 414b and 415b, each formed on a side surface of NMOS gate electrode 408b. Sidewall spacers 412b, 414b, and 415b, alone or together, constitute a first sidewall spacer. *See, e.g.*, the following:    Cheng817 Fig. 4j (showing sidewall spacers 412b, 414b and 415b, each formed on a side surface of NMOS gate electrode 408b).

Exemplary Disclosures
 Cheng817 Fig. 5i (showing sidewall spacers 512b, 514b, and 515b, each formed on a side surface of NMOS gate electrode 508b).  **Figure A** **Figure B** **(Cheng817, Figs. 4j, 5i (corrected))** "In FIG. 4b, sidewall dielectric layers 412 and 414, and spacer material 415 are disposed over the semiconductor device(s) 410a and 401b and are subsequently processed, such as by etching, to form sidewall dielectric structures 412a, 412b, 414a and 414b, and spacers 415a and 415b, as shown in FIG. 4c. Note the dielectric structures 714a and 714b are substantially L-shaped. A dummy spacer layer 416 is formed over the semiconductor devices 401a and 401b. Low temperature processing, such as using a temperature less than 600° C., to form the sidewall dielectric and spacer materials is preferred to reduce lightly doped drain diffusion." Cheng817 ¶ [0061].

Exemplary Disclosures
"The sidewall dielectric layers 412 and 414 may be a liner oxide layer and a nitride layer formed over the devices by deposition. In particular, the sidewall dielectric layers 412 and 414 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), polymer and/or other materials. The sidewall dielectric layers 412 and 414 may also include multiple layers and/or may include a single layer, in one embodiment. The sidewall dielectric layers 412 and 414 may be formed by RTO, CVD, PVD, PECVD, ALD, CMP, chemical etching, plasma etching, and/or other processing techniques. The spacer material 415 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), polymer and/or other materials. The spacer material 415 may also include multiple layers and/or may include a single layer, in one embodiment. The spacer material 415 may be formed by RTO, CVD, PVD, PECVD, ALD, CMP, chemical etching, plasma etching, and/or other processing techniques. The sidewall dielectric structures 412a, 412b, 414a and 414b, and spacers 415a and 415b may be formed by chemical etching, plasma etching, CMP, focused ion beam (FIB), and/or other processing techniques." Cheng817 ¶ [0062]. "In FIG. 5b, sidewall dielectric layers 512 and 514, and a spacer material 515 are formed over the semiconductor devices 510a and 501b, preferably using a low temperature process to reduce LDD diffusion. The sidewall dielectric layers 512 and 514 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), polymer and/or other materials. The spacer material 515 may include thermal oxide (SiO_2), TEOS oxide, silicon nitride (Si_xN_y), silicon dioxide (SiO_2), polymer and/or other materials. For example, dielectric layers 512 and 514 may comprise a liner oxide layer and a nitride layer, and the spacer material 515 may comprise an oxide material. The sidewall dielectric layers 512 and 514 and spacer layer 515 may be formed by RTO, CVD, PVD, PECVD, ALD, CMP, chemical etching, plasma etching, and/or other processing techniques." Cheng817 ¶ [0076] "In FIG. 5c, the sidewall dielectric layers 512 and 514, and a spacer material 515 are subsequently processed forming sidewall dielectric 512a, 512b, 514a and 514b, and spacers 515a and 515b. The sidewall dielectric 512a, 512b, 514a and 514b, and spacers 515a and 515b may be formed by chemical etching, plasma etching, CMP, focused ion beam (FIB), and/or other processing techniques." Cheng817 ¶ [0077]. Additionally, under Plaintiff's apparent interpretation of the claim language, the claimed "second gate electrode" may include a silicide film. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 35-43. Although TSMC does not necessarily agree with such an interpretation, Cheng817 further discloses this element under this interpretation, as shown below.

Exemplary Disclosures
For example, Cheng817 discloses silicide 432b formed on NMOS gate electrode 408b. *See, e.g.*, the following:



Cheng817 Figs. 4j, 5i (showing spacers 412a/512b, 414a/514b, and 415a/515b, each formed on a side surface of NMOS silicides 432a/532b).

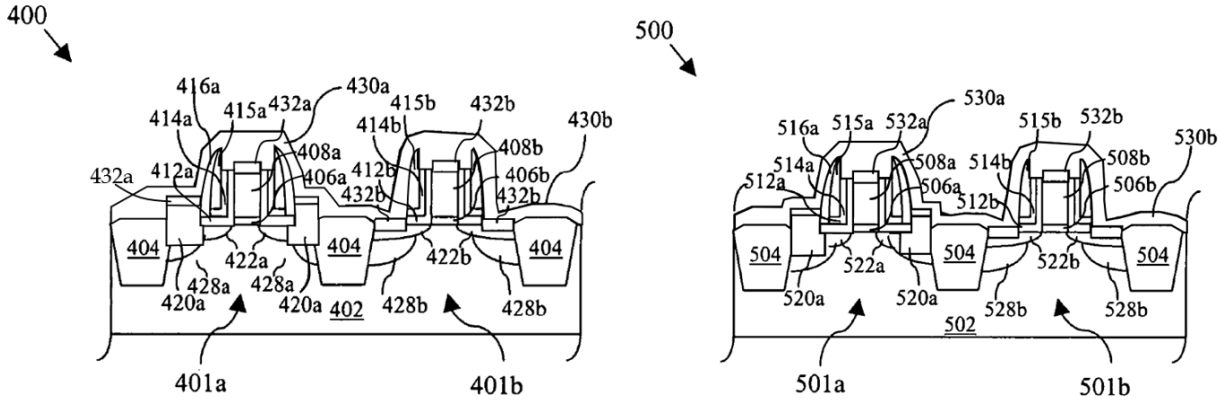
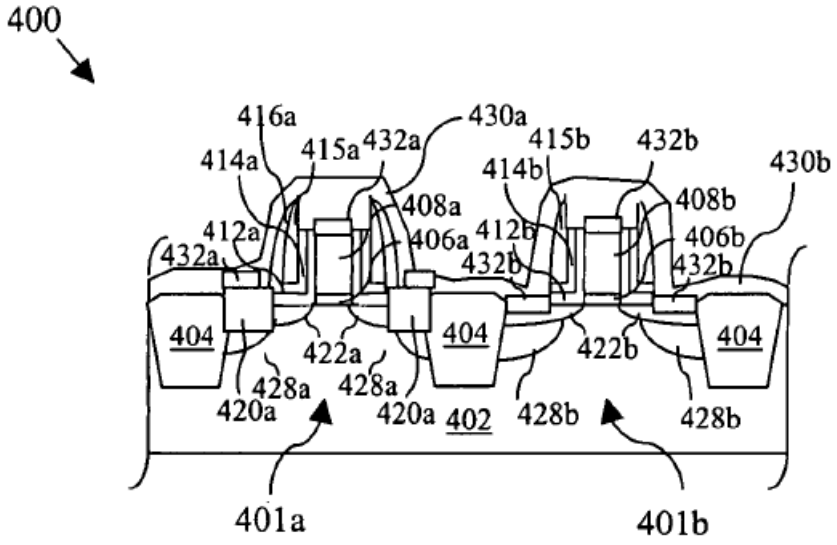


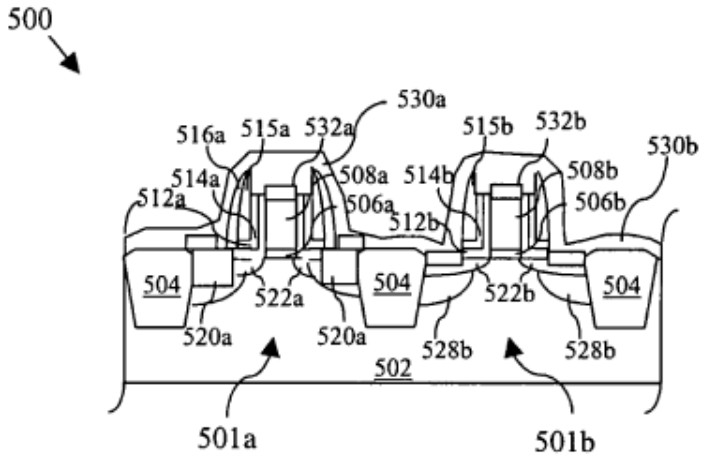
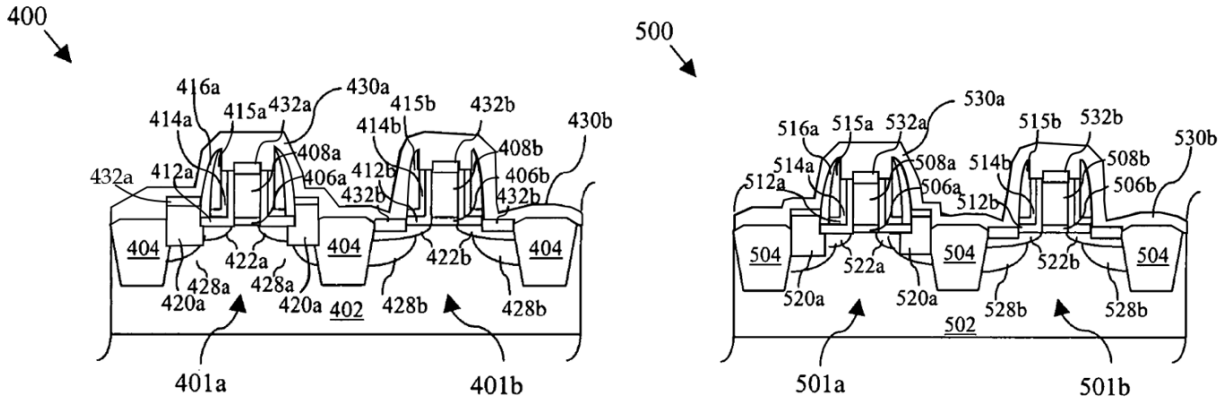
Figure A **Figure B**

(Cheng817, Figs. 4j, 5i (corrected))

"In FIG. 4i, the photoresist 421b is removed from the device 401b, and salicided contacts 432a and 432b are formed over the gate, source and drain of the devices 401a and 401b. The salicided contacts 432a and 432b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 732a and 732b may also include an anneal. The salicided contacts 732a and 732b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques."

Cheng817 ¶ [0069].

Exemplary Disclosures
"Because the deeper doped source and drain regions were doped in-situ (FIG. 5g), a process of source and drain implantation such as that shown in FIG. 4h is not required. Therefore, salicided contacts 532a and 532b are formed for the gate, source and drains of the devices 501a and 501b, respectively, as shown in FIG. 5h. The salicided contacts 532a and 532b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 532a and 532b may also include an anneal. The salicided contacts 532a and 532b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0083]. *See also, e.g.,* Cheng817 ¶ [0003], ¶ [0019], ¶ [0041], ¶ [0052], ¶ [0058], ¶ [0069], ¶ [0073], ¶ [0083], ¶ [0087], ¶ [0097], ¶ [0099], ¶ [0101], FIGS. 1, 2, 3n, 4i-4j, 5h-5i, 6h-6i, 7. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
11[e] a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer, and
Cheng817 discloses this feature. For example, Cheng817 discloses NMOS source/drain regions 422b, 428b of an n-type conductivity which are formed in the NMOS active region on a lateral side of sidewall spacers 412b, 414b, and 415b. *See, e.g.*, the following:    Cheng817 Fig. 4j (showing NMOS source/drain regions 422b, 428b of an n-type conductivity formed in the NMOS active region on a lateral side of spacers 412b, 414b, and 415b).

Exemplary Disclosures
 Cheng817 Fig. 5i (showing NMOS source/drain regions 522b, 528b of an n-type conductivity formed in the NMOS active region on a lateral side of spacers 512b, 514b, and 515b).  **Figure A** **Figure B** **(Cheng817, Figs. 4j, 5i (corrected))**

"Thus, the present disclosure introduces a semiconductor device including, in one embodiment, an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface; and (2) first source/drain regions extending from the surface. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface."

Cheng817 ¶ [0033].

Exemplary Disclosures
"In another embodiment, semiconductor device constructed according to aspects of the present disclosure comprises an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface. A second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different." Cheng817 ¶ [0034]. "Another embodiment of a semiconductor device constructed according to aspects of the present disclosure includes an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; (2) a first gate interposing the first source/drain regions; and (3) first spacers on opposing sides of the first gate and each extending from the first gate to a first width. A second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; (2) a second gate interposing the second source/drain regions; and (3) second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different." Cheng817 ¶ [0035]. "In another embodiment, a semiconductor device constructed according to aspects of the present disclosure includes an isolation region located in a substrate, an NMOS device located partially over a surface of the substrate, and a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe; (2) second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and (3) second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe." Cheng817 ¶ [0036].

Exemplary Disclosures
"The present disclosure also introduces a method of manufacturing semiconductor device. In one embodiment, the method includes forming an isolation region located in a substrate, forming an NMOS device located partially over a surface of the substrate, and forming a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface. A first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface; and (2) first source/drain regions extending from the surface. A second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface." Cheng817 ¶ [0037]. "Referring now to FIGS. 4a-4j for sectional views of another embodiment of a method for making semiconductor devices 401a and 401b with high drive current. The semiconductor device 401a may be a P-type MOS device and the semiconductor device 401b may be an N-type MOS device. In FIG. 4a, gate dielectric 406a and 406b are formed over a substrate 402 for devices 401a and 401b, respectively, and electrically isolated from one another by isolation structures 404. The isolation structures 404 may be shallow trench isolation (STI) structures. Gate electrodes 408a and 408b are formed over the gate dielectric layer, and hard masks 410a and 410b are formed over the gate electrodes 408a and 408b, respectively." Cheng817 ¶ [0056]. "The lightly doped regions 422a and 422b may include P-type and N-type dopants for the devices 401a and 401b, respectively. The doped regions 422a and 422b may be formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The doped regions 422a and 422b may also include lightly doped regions (LDD) and/or heavily doped regions in one embodiment. The doped regions 422a and 422b may include impurities such as phosphorous, boron, antimony, arsenic, and/or other materials. For example, the formation of the doped regions 422a and 422b by ion implantation may include an ion implant energy ranging between about 1 KeV and about 100 KeV and the dose of ion implantation of may range between about 1×10^{13} cm^{-2} and about 5×10^{16} cm^{-2}." Cheng817 ¶ [0060]. "In FIG. 4f, a photoresist 421a is disposed over the semiconductor device 401a. Further, the dummy spacer 716b is removed from the device 401b. The spacer material 416b may be removed by chemical etch, plasma etch, CMP focused ion beam (FIB), and/or other processing techniques. Deeper and more heavily doped regions 428b are also formed in the substrate 402 in the semiconductor device 401b. The doped regions 428b may include N-type impurities, and may be formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The doped regions 428b may include heavy doped regions forming the source/drain regions of the semiconductor device 701b. The ion implantation may include an ion implant energy ranging

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between about 5 KeV and about 100 KeV and the dose of ion implantation of may range between about 1×10^{14} cm^{-2} and about 5×10^{18} cm^{-2}." Cheng817 ¶ [0066]. "Referring now to FIGS. 5a-i for another embodiment of a method for manufacturing a microelectronic device 500 with high drive current. In FIG. 5a, gate structures including a gate dielectric 506a and 506b and gate electrodes 508a and 508b are formed for semiconductor devices 501a and 501b, respectively. Gate electrodes 508a and 508b may be pre-doped with appropriate P-type and N-type dopants, respectively. Hard masks 510a and 510b are also formed over each gate structure. Further, shallow doped drain and source regions 522a and 522b are formed on either sides of the gate structures of each device 501a and 501b. Isolation structures 504 are formed in the substrate 502 to electrically isolate the devices 501a and 501b." Cheng817 ¶ [0072]. "The doped source and drain regions 522a and 522b may include N-type and/or P-type doped regions formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The doped regions 522a and 522b may be lightly doped drains (LDD) and may include impurities such as phosphorous, boron, antimony, arsenic, and/or other materials." Cheng817 ¶ [0075]. "In FIG. 5f, a photoresist 521a is disposed over the semiconductor device 501a for processing of the semiconductor device 501b. The dummy spacer material 516b is removed from the device 501b, and deeper source and drain doped regions 528b are formed. The spacer material 516b may be removed by chemical etch, plasma etch, CMP focused ion beam (FIB), and/or other processing techniques, for example. The doped regions 528b may include N-type impurities, and may be formed by ion implantation, thermal diffusion, RTA, and/or other processing techniques. The ion implantation process may use an ion implant energy ranging between about 5 KeV and about 100 KeV and the dose of ion implantation of may range between about 1×10^{14} cm^{-2} and about 5×10^{18} cm^{-2}, for example." Cheng817 ¶ [0081]. To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

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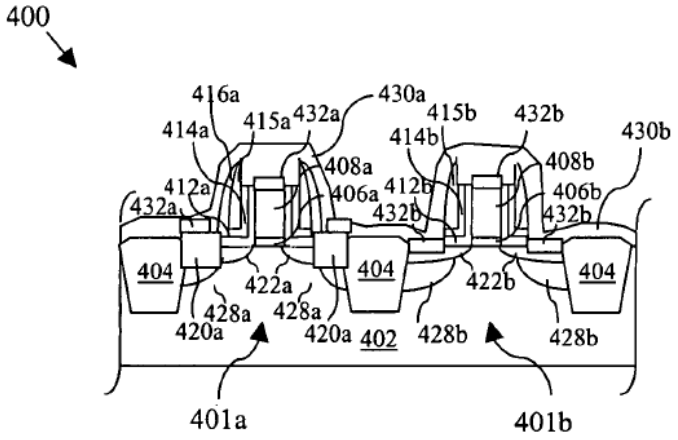
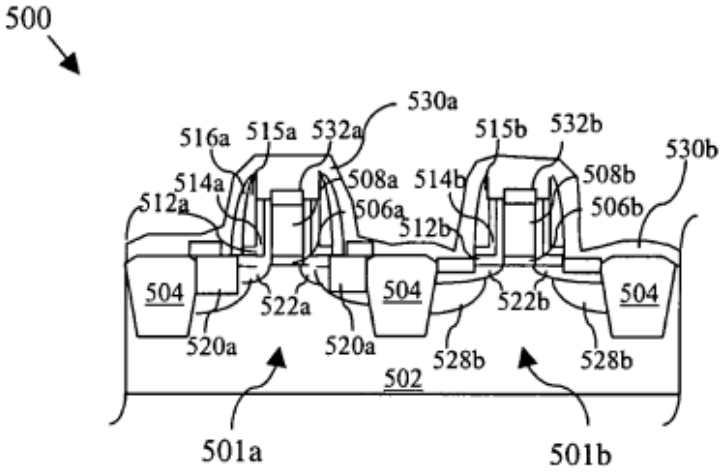
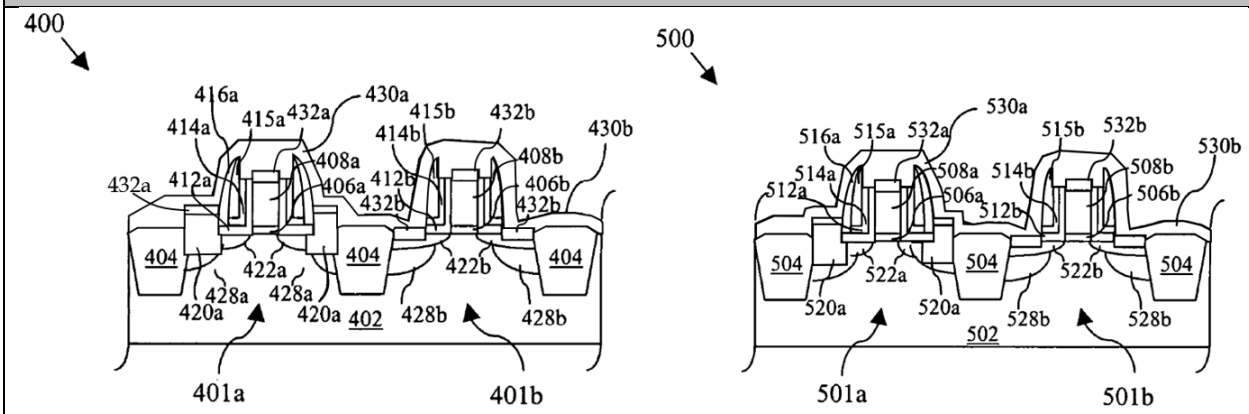
11[f] the stress insulating film formed on the second active region to cover the second gate electrode, the second sidewall spacer, and the second source/drain region.
Cheng817 discloses this feature. For example, Cheng817 discloses the etch stop layer 430a/430b (e.g., a SiN layer) formed on the NMOS active region to cover NMOS gate electrode 408b, sidewall spacers 412b, 414b, and 415b, and NMOS source/drain regions 422b and 428b. *See, e.g.*, the following:



Cheng817 Fig. 4j (showing etch stop layer 430a/430b formed on the NMOS active region to cover gate electrode 408b, sidewall spacers 412b, 414b, and 415b, and NMOS source/drain regions 422b and 428b).



Cheng817 Fig. 5i (showing etch stop layer 530a/530b formed on the NMOS active region to cover gate electrode 508b, sidewall spacers 512b, 514b, and 515b, and NMOS source/drain regions 522b and 528b).

Exemplary Disclosures
 **Figure A** **Figure B** **(Cheng817, Figs. 4j, 5i (corrected))**

"Increasing tensile or compressive stress in a semiconductor device substrate can improve drive current. For example, increasing the tensile stress in the substrate can improve the performance of n-channel metal-oxide-semiconductor (NMOS) devices. Similarly, increasing the compressive stress in the substrate can improve the performance of p-channel metal-oxide-semiconductor (PMOS) devices."

Cheng817 ¶ [0002].

"Some applications have realized limited localized stress tuning by employing different materials for adjacent shallow trench isolation (STI) regions and other isolation structures. Stress tuning can also be accomplished by employing different materials for silicide and other contact layers. Etch stop layers remaining in the device structure after being employed as etching endpoints have also been employed for substrate stress tuning."

Cheng817 ¶ [0003].

"The semiconductor device 100 may also include an etch stop layer 180. The etch stop layer 180 may comprise silicon nitride (e.g., Si3N4), silicon oxynitride (e.g., SiON), silicon carbide, silicon dioxide and/or other materials, and may be formed by blanket or selective deposition by CVD, PVD, thermal oxidation and/or other processes. The etch stop layer 180 may be a tensile or compressive film, wherein a stress level may range between about +0.01 and about +2 GPa for tensile film and between about −0.01 and about −2 GPa for compressive film. The tensile or compressive nature of the etch stop layer 180 may impart strain within the source/ drain regions 136, 176. Moreover, the strain induced in the source/drain region 136 by the etch stop layer 180 may be substantially different in magnitude that the strain induced in the source/drain region 176 by the etch stop layer 180. For example, the strain induced in the source/ drain regions 136, 176 may vary by 10-20% in magnitude. In one embodiment, the strain induced in the source/drain regions 136 may be tensile and the strain induced in the source/drain regions 176 may be compressive. In another embodiment, the strain induced in the source/drain

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regions 136 may be compressive and the strain induced in the source/drain regions 176 may be tensile. The thickness of etch stop layer 180 may range between about 5 nm and about 200 nm." Cheng817 ¶ [0030]. "Further in FIG. 4j, an etch stop layer 430a and 430b are formed over the semiconductor device(s) 401a and 401b. The etch stop layer 430a and 430b may include silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), and/or other materials. In one embodiment, the etch stop layer 430a and 430b may be substantially similar in composition to the etch stop layer 180 described above. Alternatively, the etch stop layer 430a and 430b may include a stress level that may range between about +0.001 and about +50 GPa for tensile film and between about −0.001 and about −50 GPa for compressive film. The etch stop layer 430a and 430b may be formed by CVD, ALD, PECVD, PDL, spin-on coating, and/or other techniques." Cheng817 ¶ [0070]. "In FIG. 5i, etch stop layer 530a and 530b are formed over the semiconductor devices 501a and 501b. The etch stop layer 530a and 530b may include silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), and/or other materials. Alternatively, the etch stop layer 530a and 530b may include a stress level that may range between about +0.001 and about +50 GPa for tensile film and between about −0.001 and about −50 GPa for compressive film. The etch stop layer 530a-b may be formed by CVD, ALD, PECVD, PDL, spin-on coating, and/or other techniques." Cheng817 ¶ [0084]. Additionally, under Plaintiff's apparent interpretation of the claim language, the claimed "second gate electrode" may include a silicide film. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 35-43. Although TSMC does not necessarily agree with such an interpretation, Cheng817 further discloses this element under this interpretation, as shown below. For example, Cheng817 discloses silicide 432b formed on NMOS gate electrode 408b. *See, e.g.*, the following: "In FIG. 4i, the photoresist 421b is removed from the device 401b, and salicided contacts 432a and 432b are formed over the gate, source and drain of the devices 401a and 401b. The salicided contacts 432a and 432b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 732a and 732b may also include an anneal. The salicided contacts 732a and 732b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0069].

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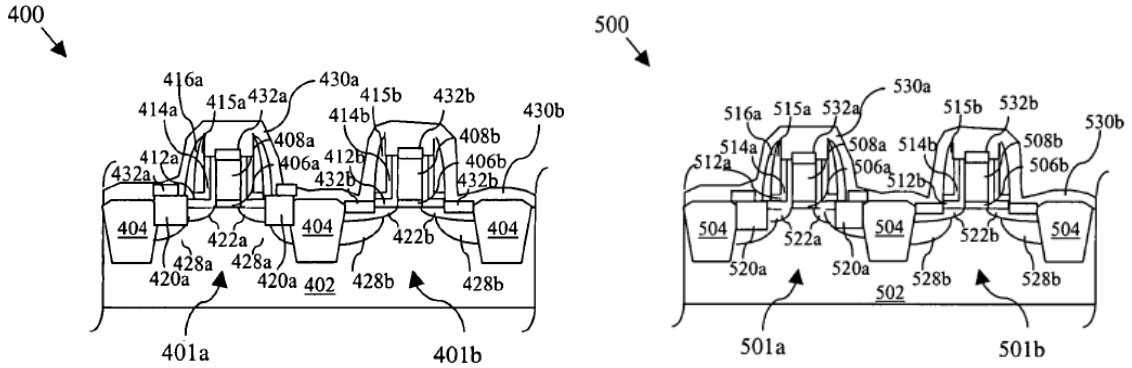
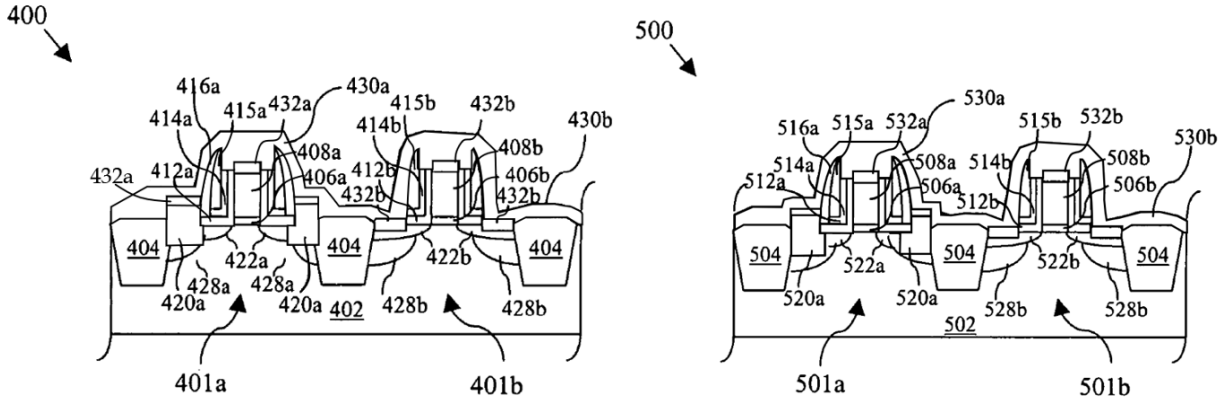
"Because the deeper doped source and drain regions were doped in-situ (FIG. 5g), a process of source and drain implantation such as that shown in FIG. 4h is not required. Therefore, salicided contacts 532a and 532b are formed for the gate, source and drains of the devices 501a and 501b, respectively, as shown in FIG. 5h. The salicided contacts 532a and 532b may include the formation of a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The formation of the salicided contacts 532a and 532b may also include an anneal. The salicided contacts 532a and 532b may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PDL, PVD, and/or other processing techniques." Cheng817 ¶ [0083].      Cheng817 Figs. 4j, 5i (showing etch stop layer 430a/430b formed on the NMOS active region to cover gate silicide 432b, sidewall spacers 412b, 414b, and 415b, and NMOS source/drain regions 422b and 428b).      **Figure A** **Figure B** **(Cheng817, Figs. 4j, 5i (corrected))** *See also, e.g.,* Cheng817 ¶ [0003], ¶ [0019], ¶ [0041], ¶ [0052], ¶ [0058], ¶ [0069], ¶ [0073], ¶ [0083], ¶ [0087], ¶ [0097], ¶ [0099], ¶ [0101], FIGS. 1, 2, 3n, 4i-4j, 5h-5i, 6h-6i, 7.

Exhibit 425-08: Cheng817

Exemplary Disclosures
To the extent that Cheng817 is found not to disclose this feature, it would have been obvious based on the disclosures of Cheng817 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-07 and 425-09 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.