Exhibit 425-16: Saito825

U.S. Patent Application Publication No. 2008/0029825 ("Saito825") was filed on August 2, 2007, published on February 7, 2008, and claims priority to Japanese Patent Application No. JP2006-213535, which was filed on August 4, 2006. Accordingly, Saito825 constitutes prior art to U.S. Patent No. 8,907,425 (the "'425 patent") under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e).

Saito825, including any material incorporated by reference into Saito825, anticipates claims 1, 3-5, 7, and 11 (the "asserted claims") of the '425 patent under pre-AIA 35 U.S.C. §§ 102(a), (b), and (e).

To the extent any limitation is found not to be expressly or inherently disclosed in Saito825, such a limitation would have been obvious either based on Saito825 alone, given the state of the art, or in combination with one or more of the references cited in Exhibits 425-01 through 425-15 and 425-17 through 425-21, because the '425 patent is merely a collection of prior art elements that fails to meet the statutory requirement of non-obviousness under 35 U.S.C. § 103, and the factors delineated in *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), weigh against a finding of non-obviousness.

Any disclosures identified for each limitation of the '425 patent in the aforementioned Exhibits may be combined with the disclosures of Saito825 identified below for the same limitation to render that limitation obvious. A POSITA would have found such a combination / modification obvious for the reasons discussed herein and in Defendant's cover pleading.[1]

The citations to portions of any reference in this chart are exemplary only. Citations to the written description should be interpreted to include the figures associated with or relevant to the cited passages. Similarly, citations to a figure should be understood to encompass any description, text, or discussion of that figure. Defendant reserves the right to use the entirety of any reference cited in this chart to show that the asserted claims are anticipated and/or are obvious. Citations presented for one claim limitation are expressly incorporated by reference into all other limitations for that claim as well as all limitations of all claims on which that claim depends.

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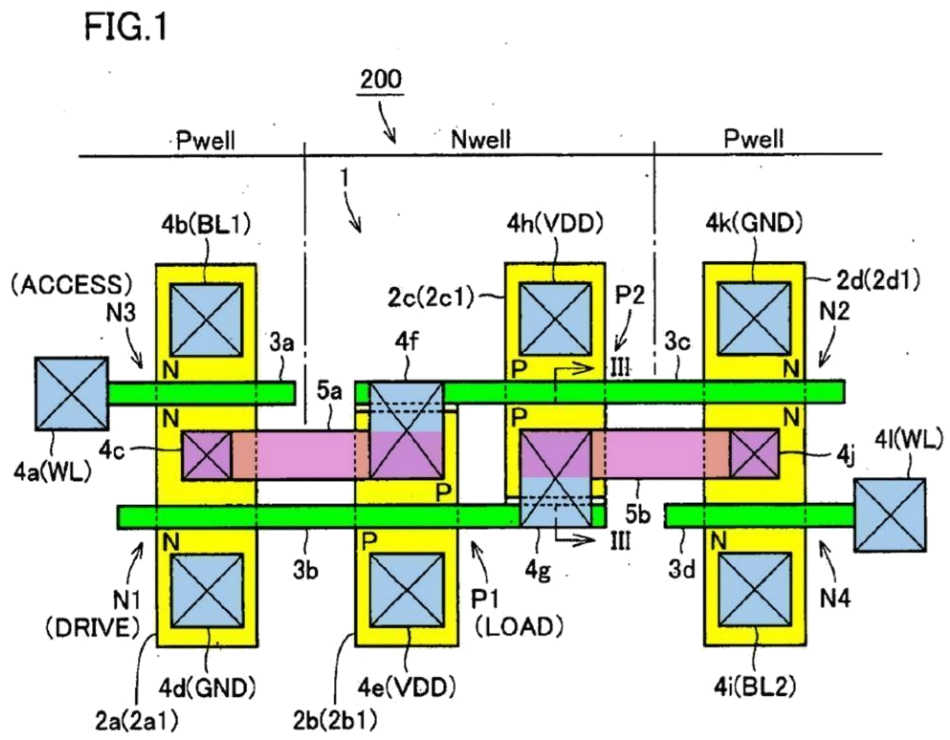
[1] Plaintiff appears in many instances to be pursuing overly broad constructions of limitations of the asserted claims in an effort to piece together an infringement claim where none exists. This claim chart accounts for overly broad construction of the claim limitations. Any assertion that a particular limitation is disclosed by a prior art reference or references may be based on Plaintiff's apparent constructions and is not intended to be, and is not, an admission that such constructions are supportable or proper. Defendant is investigating this prior art and has not yet completed discovery from third parties, who may have relevant information concerning the prior art. Therefore, Defendant reserves the right to supplement this chart after additional discovery is received. To the extent that any of the prior art discloses the same or similar functionality or feature(s) of any of the accused products, Defendant reserves the right to argue that said feature or functionality does not practice any limitation of any of the asserted claims, and to argue, in the alternative, that if said feature or functionality is found to practice any limitation of any of the asserted claims, then the prior art reference teaches the limitation and that the claim is not patentable.

Exhibit 425-16: Saito825

Saito825 discloses a conventional SRAM circuit with levels 1-5 numbered in order:

- Substrate: **1**00 (uncolored below). ¶[0072].
- Active regions: **2**a-**2**d (yellow below). ¶¶[0060]-[0061].
- Polysilicon wirings: **3**a-**3**d (green below). ¶¶[0067]-[0068], ¶[0124].
- Contact parts: **4**a-**4**l (blue below). ¶¶[0068]-[0069].
- Metal wirings: **5**a-**5**b (purple below). ¶¶[0070]-[0071].



Saito825 FIG. 1 (annotated).

Saito825 explains that "[p]olysilicon wirings 3a-3d constitute a gate of each MOS transistor."

Saito825 ¶ [0067]. Saito825's "contact parts 4a-4l" connect the transistors with the "upper wiring" layer 5*x*. ¶[0068], ¶[0071]. The "metal wiring 5b" connects contact part 4g at "the drain of second load transistor P2" with "contact part 4j" at the "drain of second driver NMOS transistor N2."

Saito825 ¶ [0068], ¶[0071]. Because metal wiring 5b is an "upper wiring" that connects contact parts 4g and 4j, a POSITA in the art would have understood it lies above the cross-sections in FIGS. 3-21.

Like FIGS. 3-11, region R1 in Saito825's FIGS. 12-21 shows cross-sections along cutline III-III in FIG. 1. *Compare* ¶[0030], ¶[0072], FIGS. 3-11, *with* FIGS. 12-21. Reading Saito825's description, a POSITA would have recognized that identifier "5b" in FIGS. 12-21 identifies the polysilicon gate of PMOS transistor P2 and thus should be labeled "polysilicon wiring 3c." ¶¶[0065]-[0067], ¶[0071], FIGS. 1, 12-21. The annotated figure below from U.S. Patent Application Publication No. 2011/0074498 A1 to Thompson et al. shows a perspective view of an SRAM like the one Saito825 describes up to level 3 (polysilicon, green), with the gate sidewalls (orange) and silicide contacts (burgundy) also shown.

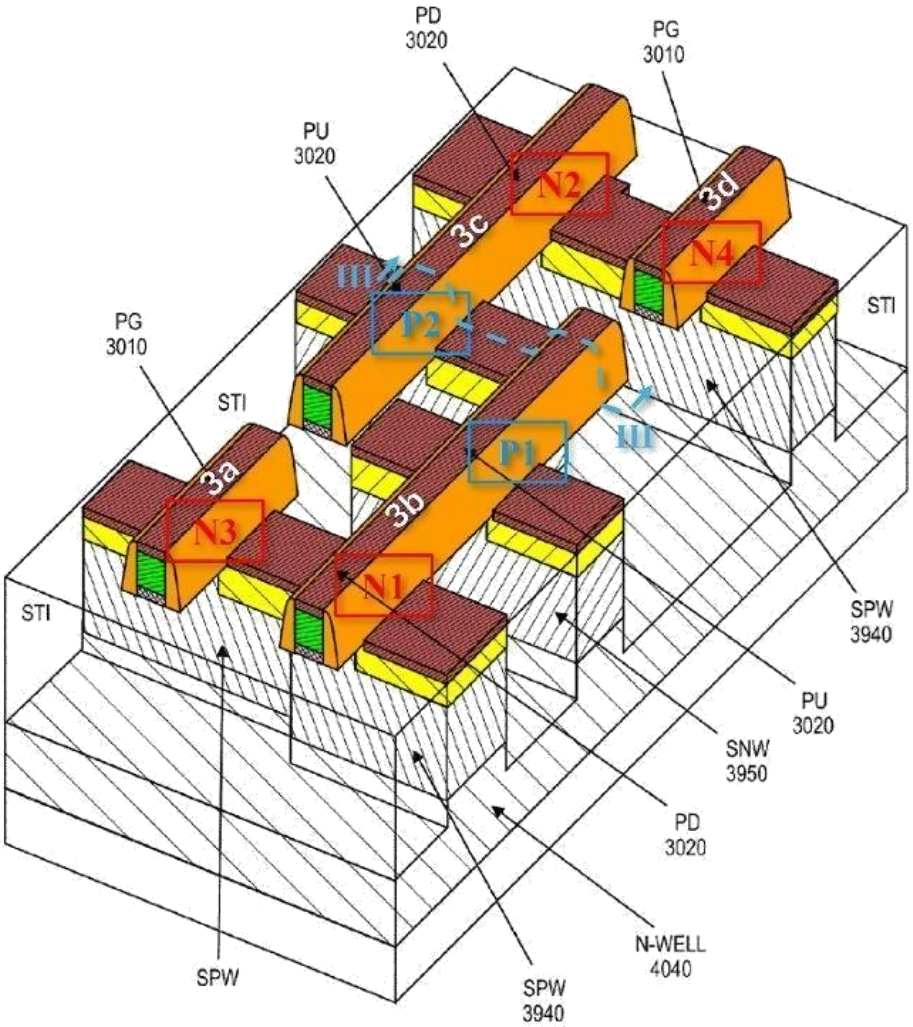


FIG. 40B

U.S. Patent Application Publication No. 2011/0074498 A1 to Thompson et al., FIG. 40B (annotated).

A POSITA would have recognized that, because Saito825's contacts 4g/4j and metal wiring 5b are textbook SRAM structures, metal wirings (5*x*) would have been located higher than the polysilicon

lines (3*x*) and contacts (4*x*), as the Composite Figure A shows below (amending and annotating U.S. Patent Application Publication No. 2011/0074498 A1 to Thompson et al., FIG. 40B).

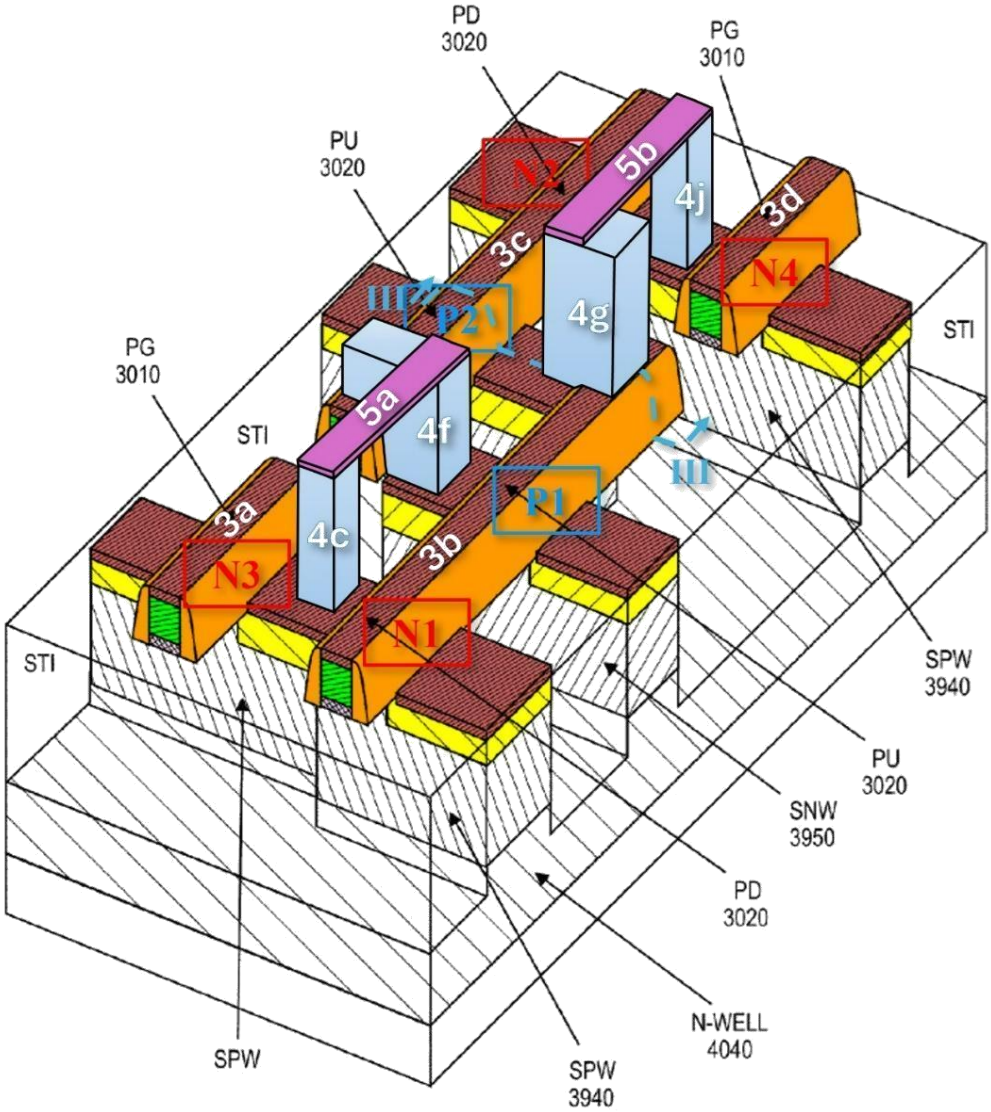


FIG. 40B

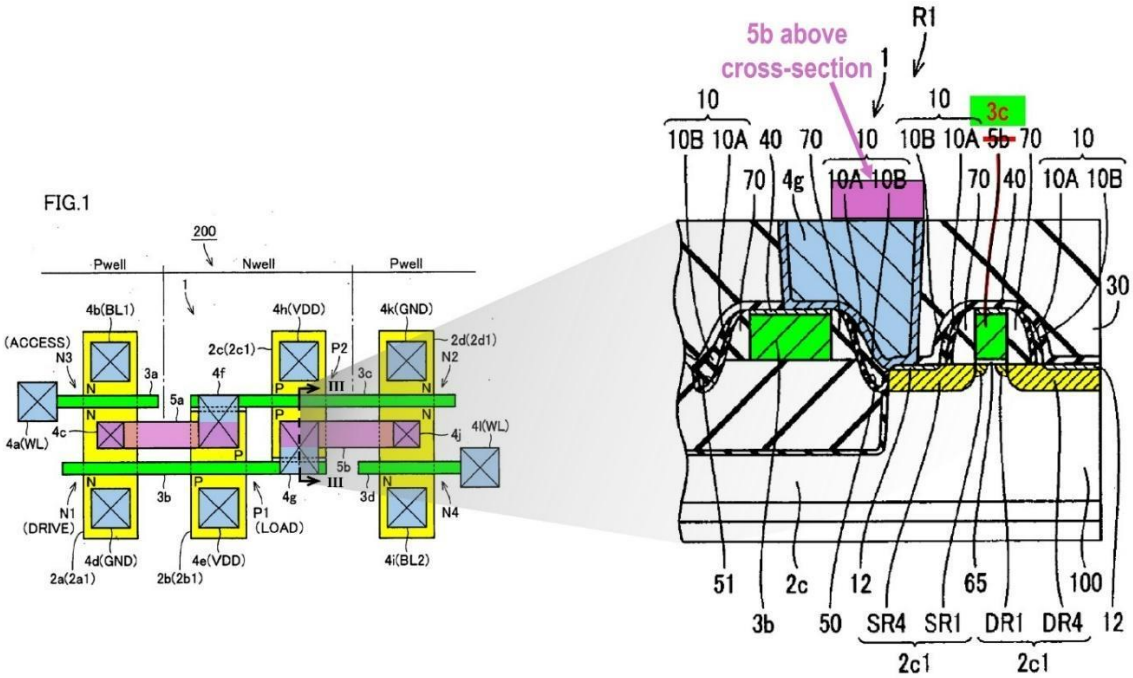
Composite Figure A.

A POSITA would have immediately recognized that "polysilicon wiring 5b" refers to "polysilicon wiring ***3c***" in FIGS. 12-21. *See LG Elecs. Inc. v. ImmerVision, Inc.*, 39 F.4th 1364, 1372 (Fed. Cir. 2022) (explaining such clerical errors should be disregarded).

Saito825 describes each of these textbook SRAM layers with a shared numeric level identifier (2*x*, 3*x*, 4*x*, 5*x*), such that a POSITA would have recognized "polysilicon wiring 5b" in Saito825's FIGS. 12-21 correctly points to a polysilicon wiring, but it is polysilicon wiring "***3c***" because no

polysilicon wiring "5b" exists. ¶¶[0065]-[0068], ¶[0124], FIGS. 1-2. A POSITA would have immediately noted that "polysilicon wirings" are designated 3*x*, such that FIGS. 12-21 show polysilicon wiring "***3c***" from FIG. 1, not "metal wiring 5b." ¶¶[0066]-[0068], ¶[0071]. A POSITA would have understood, as Saito825 explains, that "metal wiring 5b" is an "upper wiring" at contacts 4g/4j and located above Saito825's cross-sections. ¶¶[0067]-[0071].

A POSITA would have recognized labeling polysilicon as "5b" in Saito825's figures is a clerical error. Cross-section III-III in FIG. 1 includes polysilicon wirings 3b and 3c, where contact part 4g touches polysilicon wiring 3b and metal wiring 5b but not polysilicon wiring 3c. FIG. 1. "[P]olysilicon wiring 3c" is the polysilicon gate for PMOS transistor P2 and thus corresponds to a gate structure. Saito825's references to "polysilicon wiring 5b" thus describe what is shown in FIG. 1 as "3c"—the gate of transistor P2, which does not touch contact 4g. This confirms polysilicon wiring "5b" is a clerical error; it is "polysilicon wiring ***3c***," as shown below. ¶¶[0093]-[0096], ¶[0101], FIGS. 1, 12-21. Moreover, the element mislabeled item "5b" in FIGS. 12-21 sits atop gate insulating film 65, thereby indicating it is polysilicon gate 3c.[2] ¶[0051].



Saito825 FIGS. 1, 12 (excerpted, annotated)

Correcting this obvious typographical error, region R1 in FIGS. 12-21 reflects the correct cross-section corresponding to cutline III-III in FIG. 1, as expected for this conventional SRAM.

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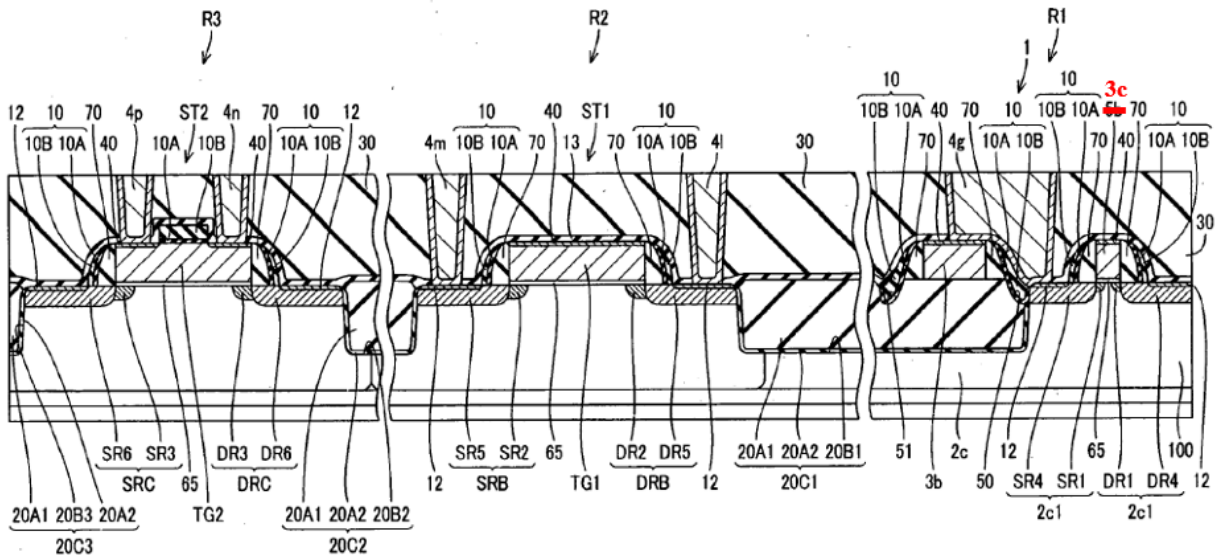
[2] If it were metal wiring 5b, gate insulating film 65 would sever the connection between node Nb and transistor N4 in FIG. 2, which is prohibited. *See* ¶[0071], FIGS. 1-2, 12.

A POSITA would have readily understood this because Saito825 does not purport to alter the wiring or structure of this textbook SRAM. Saito825 instead addresses problems associated with recesses 50 that form in isolation regions. Abstract, ¶[0011], ¶¶[0022]-[0023], ¶[0027], ¶¶[0074]-[0075].

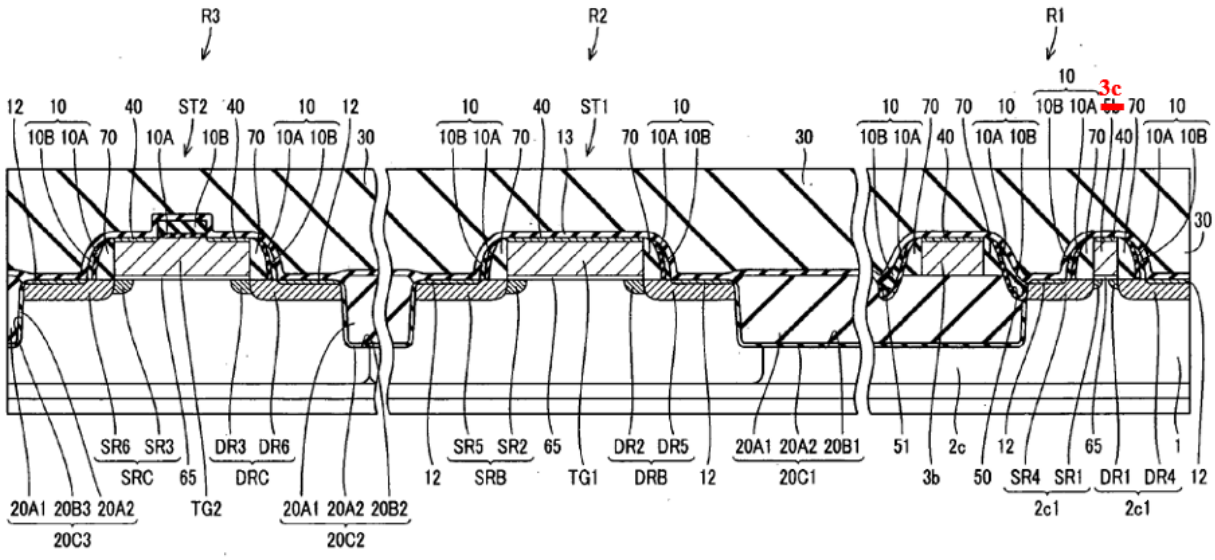
No matter how one views Saito825, a POSITA would have recognized that polysilicon wiring 3c of FIG. 1 has the structure incorrectly labeled "5b" in FIGS. 12-21, because the various layers are fabricated using the same steps. That is, (1) a POSITA would have immediately recognized Saito825's clerical error that "polysilicon wiring 5b" refers to "polysilicon wiring 3c," and, regardless, (2) the structure labeled "polysilicon wiring 5b" in FIGS. 12-21 is a MIS transistor as discussed below.

FIG.12



Saito825 FIG. 12 (corrected annotation).

FIG.21



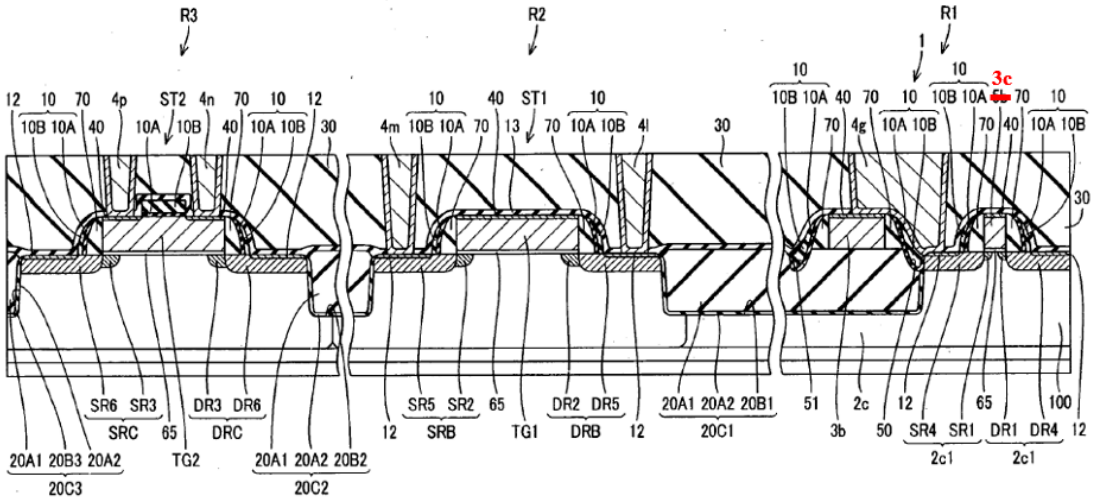
Saito825 FIG. 21 (corrected annotation).

Exemplary Disclosures

1[pre] A semiconductor device, comprising:

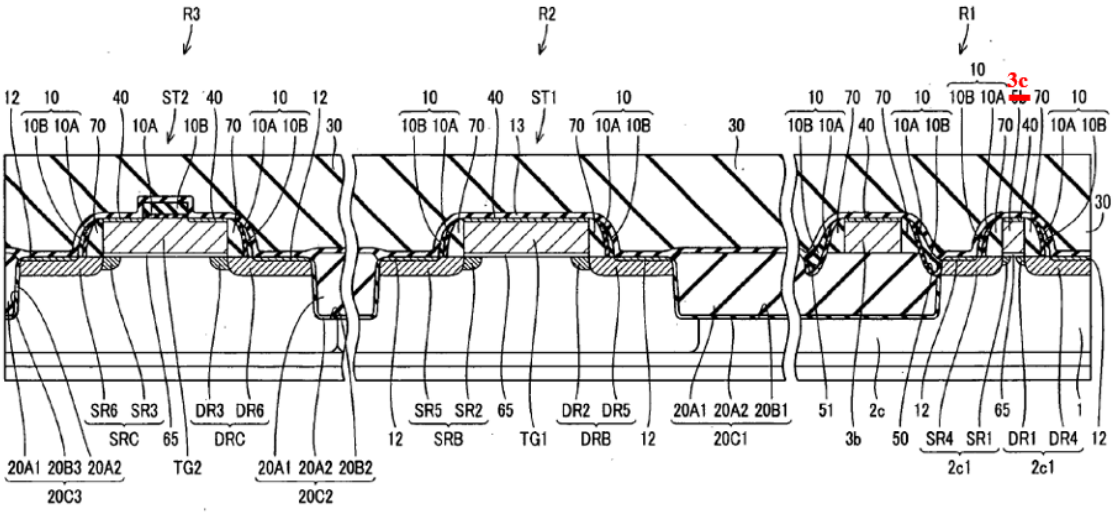
Defendant does not concede that the preamble is limiting. For example, Saito825 discloses a semiconductor device and its manufacturing method. To the extent it is limiting, Saito825 discloses the preamble. *See, e.g.*, the following:

FIG.12



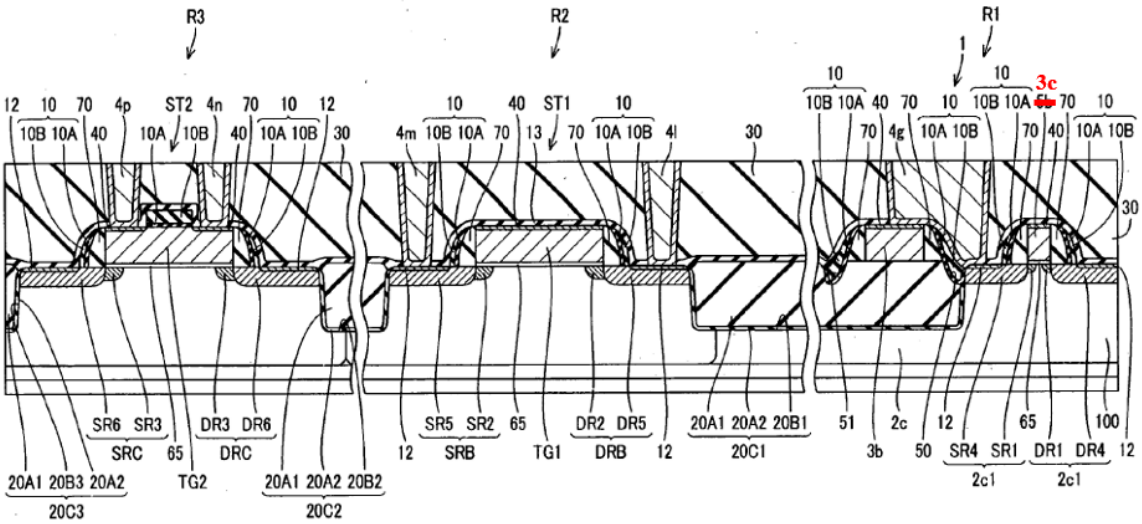
Saito825 FIG. 12 (corrected annotation).

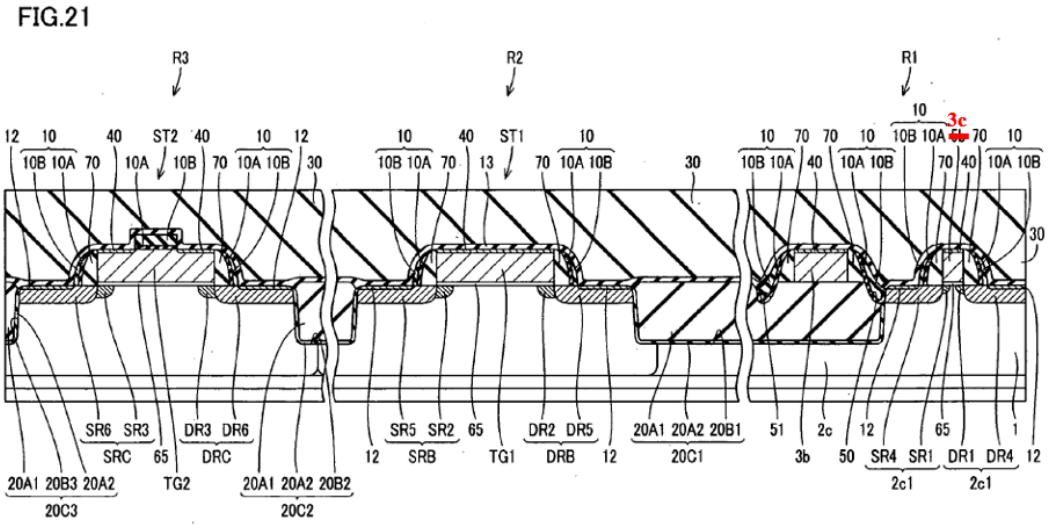
FIG.21



Saito825 FIG. 21 (corrected annotation).

Exemplary Disclosures
"Even if it is the semiconductor device provided with the wiring on an isolation insulating film, the sidewall formed on the side surface of this wiring, and the shared contact which connects the wiring and the impurity diffusion on an active region, the semiconductor device which can suppress the generation of the leakage current from shared contact to a semiconductor substrate, and its manufacturing method are offered. The semiconductor device concerning the present invention is provided with an isolation insulating film selectively formed on the main front surface of a semiconductor substrate, an active region specified by an isolation insulating film on the main front surface of a semiconductor substrate, a recess which reaches an active region on the isolation insulating film, the first insulating film formed so that a recess might be covered, the second insulating film which is formed on a first insulating film, is filled up with a recess, and differs in a material from the first insulating film, an impurity diffused layer formed on the main front surface of the active region of the position which adjoins the recess, and an electric conduction film formed on the impurity diffused layer." Saito825 Abstract. "The present invention relates to a semiconductor device and its manufacturing method." Saito825 ¶ [0002]. "Hereafter, an embodiment of the invention is explained using FIG. 21 from FIG. 1. FIG. 1 is the plan view of memory cell 1 of full CMOSSRAM (static semiconductor memory device) formed in semiconductor device 200 in an embodiment of the invention. The equivalent circuit picture of this memory cell 1 is shown in FIG. 2. And FIG. 12 is a cross-sectional view of semiconductor device 200 concerning this embodiment. First, as shown in FIG. 12, semiconductor device 200 is provided with memory cell region R1 in which memory cell 1 of full CMOSSRAM was formed, first peripheral circuit area R2 in which first peripheral circuit transistor ST1 which performs motion control of memory cell 1 was formed, and second peripheral circuit area R3 in which second peripheral circuit transistor ST2 which performs motion control of memory cell 1 was formed." Saito825 ¶ [0049]. "Memory cell region R1, and the first, second peripheral circuit area R2 and R3 are specified by isolation region 20c1, 20c2, and 20c3 which were formed on the main front surface of semiconductor substrate 100." Saito825 ¶ [0050]. "On the main front surface of semiconductor substrate 100 in which memory cell region R1 is located, isolation region 20c1 and active region 2c specified by this isolation region 20c1 are formed. And on the main front surface of semiconductor substrate 100 in which active region 2c is located, gate insulating film 65, polysilicon wiring 5b [sic 3c] formed on the upper surface

Exemplary Disclosures
of this gate insulating film 65, and impurity diffused layer 2c1 located in the both sides of this polysilicon wiring 5b [sic 3c] are formed." Saito825 ¶ [0051]. "The manufacturing method of semiconductor device 200 concerning this embodiment is explained using FIG. 4-FIG. 11, and FIG. 13-FIG. 21." Saito825 ¶ [0085]. *See also*, *e.g.*, Saito825, at ¶[0002], ¶¶ [0023]-[0026], FIGS. 1. To the extent that Saito825 is found not to disclose the preamble, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
1[a] a first MIS transistor, wherein: the first MIS transistor includes:
Saito825 discloses this feature. For example, Saito825 discloses a PMOS transistor. *See, e.g.*, the following: FIG.12    Saito825 FIG. 12 (corrected annotation).



Saito825 FIG. 21 (corrected annotation).

"On the main front surface of semiconductor substrate 100 in which memory cell region R1 is located, isolation region 20c1 and active region 2c specified by this isolation region 20c1 are formed. And on the main front surface of semiconductor substrate 100 in which active region 2c is located, gate insulating film 65, polysilicon wiring 5b [sic 3c] formed on the upper surface of this gate insulating film 65, and impurity diffused layer 2c1 located in the both sides of this polysilicon wiring 5b [sic 3c] are formed."

Saito825 ¶ [0051].

"Memory node Na is connected to bit line BL1 via first access NMOS transistor N3, and memory node Nb is connected to bit line BL2 via second access NMOS transistor N4. The gate of further the first, second access NMOS transistor N3, and N4 is connected to word line WL, and the source of the first, second load PMOS transistor P1, and P2 is connected to power supply line VDD."

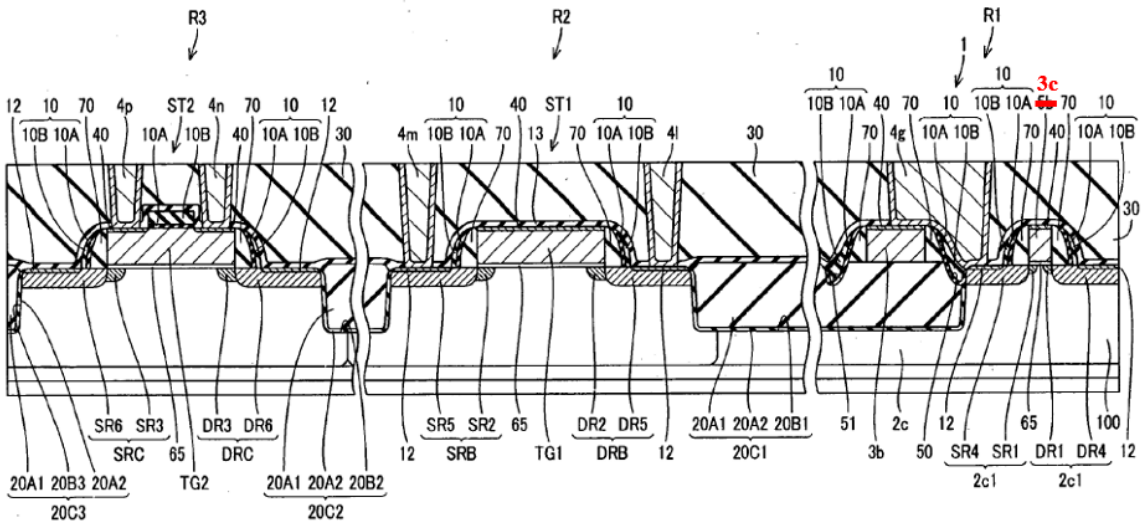
Saito825 ¶ [0057].

"Memory cell 1 in this embodiment comprises six MOS transistors. Concretely, memory cell 1 comprises the first, the second driver NMOS transistor N1, N2, and the first, the second access NMOS transistor N3, N4 and the first, the second load PMOS transistor P1, P2."

Saito825 ¶ [0062].

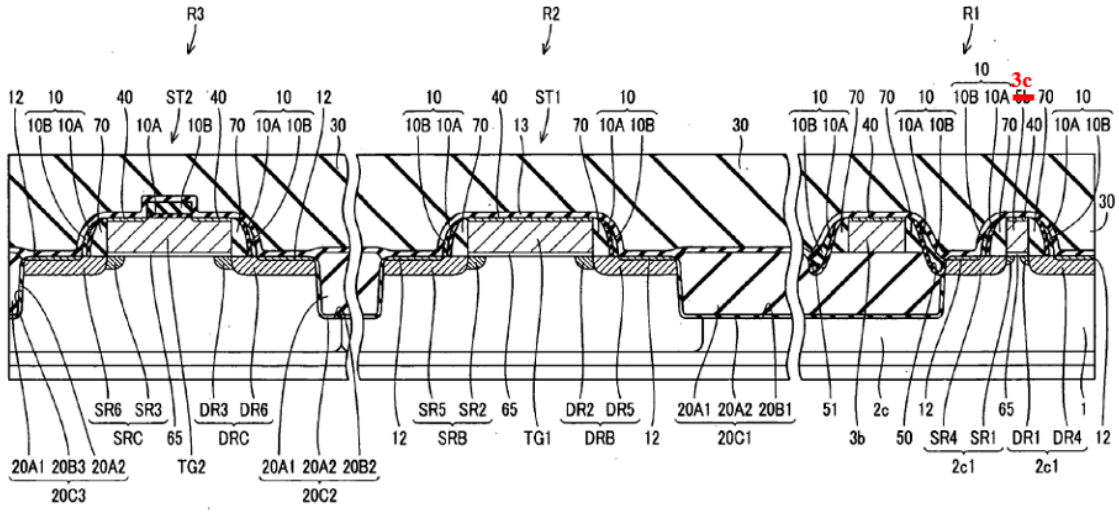
"The first, second access NMOS transistor N3, N4, and the first, second driver NMOS transistor N1 and N2 are formed on P well region of the both sides of N well region, respectively. The first, second load PMOS transistor P1, and P2 are formed on central N well region."

Saito825 ¶ [0063].

Exemplary Disclosures
"First load PMOS transistor P1 is formed in the intersection part of impurity diffusion region 2b1 comprising the region used as a source/drain, and polysilicon wiring 3b. Second access PMOS transistor P2 is formed in the intersection part of impurity diffusion region 2c1 comprising the region used as a source/drain, and polysilicon wiring 3c." Saito825 ¶ [0066]. *See also*, *e.g.*, Saito825, at FIGS. 1, 3. To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
1[b] a first gate insulating film formed on a first active region in a semiconductor substrate,
Saito825 discloses this feature. For example, Saito825 discloses a gate insulating film 65 formed on a PMOS active region in semiconductor substrate 100. *See, e.g.*, the following: FIG.12    Saito825 FIG. 12 (corrected annotation).

Exemplary Disclosures

FIG.21



Saito825 FIG. 21 (corrected annotation).

"On the main front surface of semiconductor substrate 100 in which memory cell region R1 is located, isolation region 20c1 and active region 2c specified by this isolation region 20c1 are formed. And on the main front surface of semiconductor substrate 100 in which active region 2c is located, gate insulating film 65, polysilicon wiring 5b [sic 3c] formed on the upper surface of this gate insulating film 65, and impurity diffused layer 2c1 located in the both sides of this polysilicon wiring 5b [sic 3c] are formed."

Saito825 ¶ [0051].

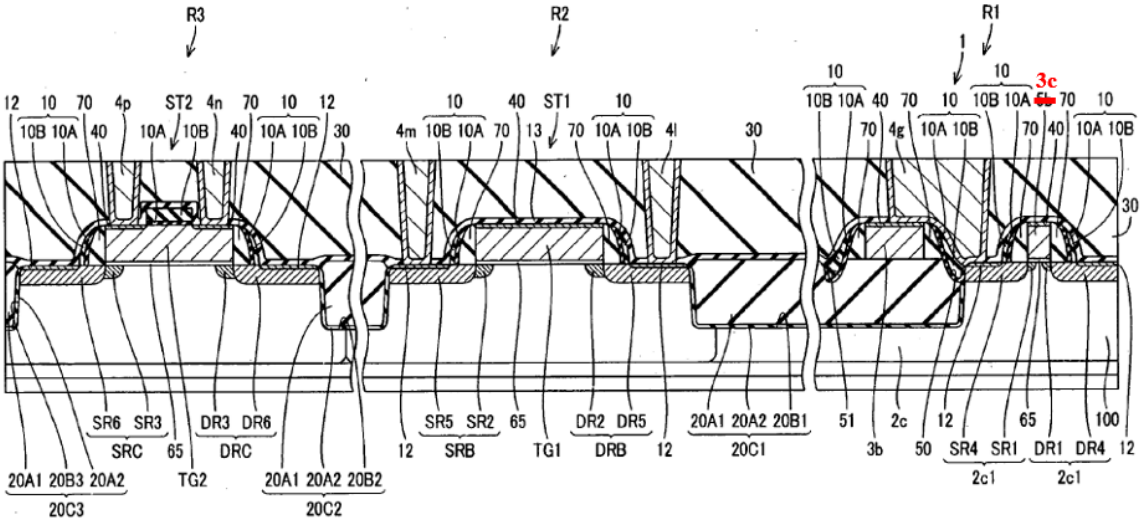
"In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g."

Saito825 ¶ [0124].

To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

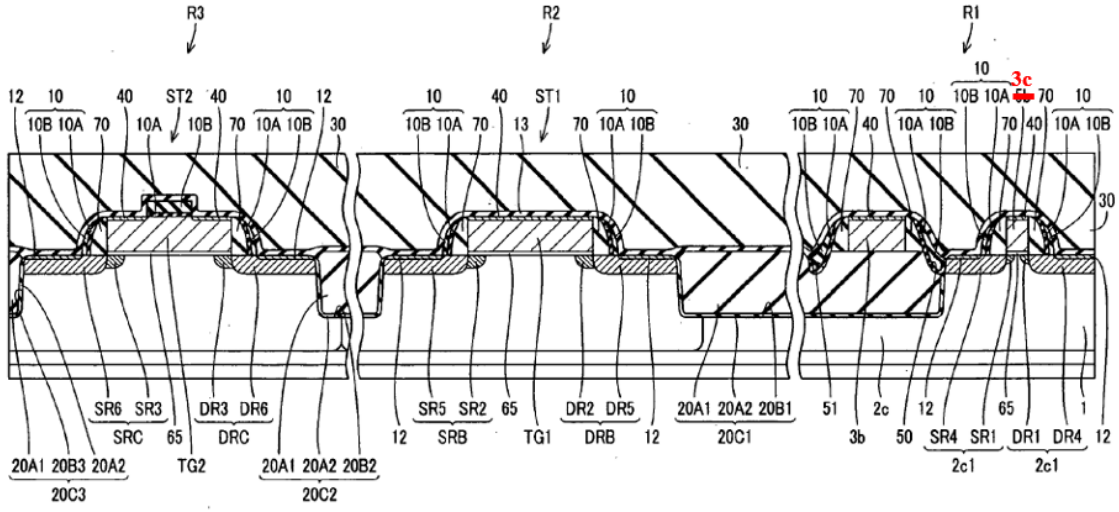
Exemplary Disclosures
1[c] a first gate electrode formed on the first gate insulating film,
Saito825 discloses this feature. For example, Saito825 discloses a PMOS gate electrode 3c (corrected from 5b) formed on the PMOS gate insulating film 65. *See, e.g.*, the following:

FIG.12



Saito825 FIG. 12 (corrected annotation).

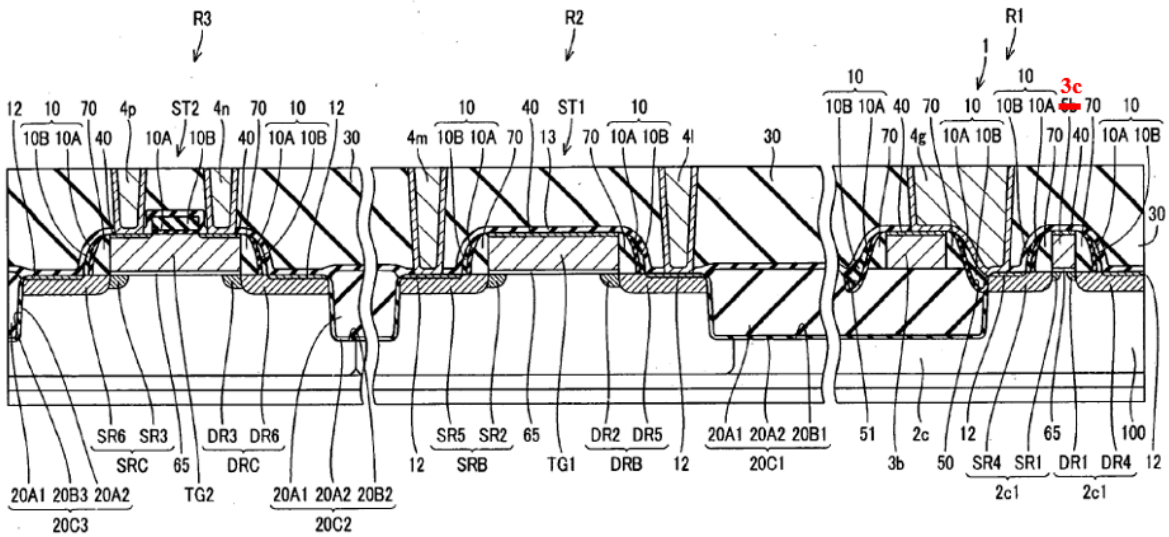
FIG.21

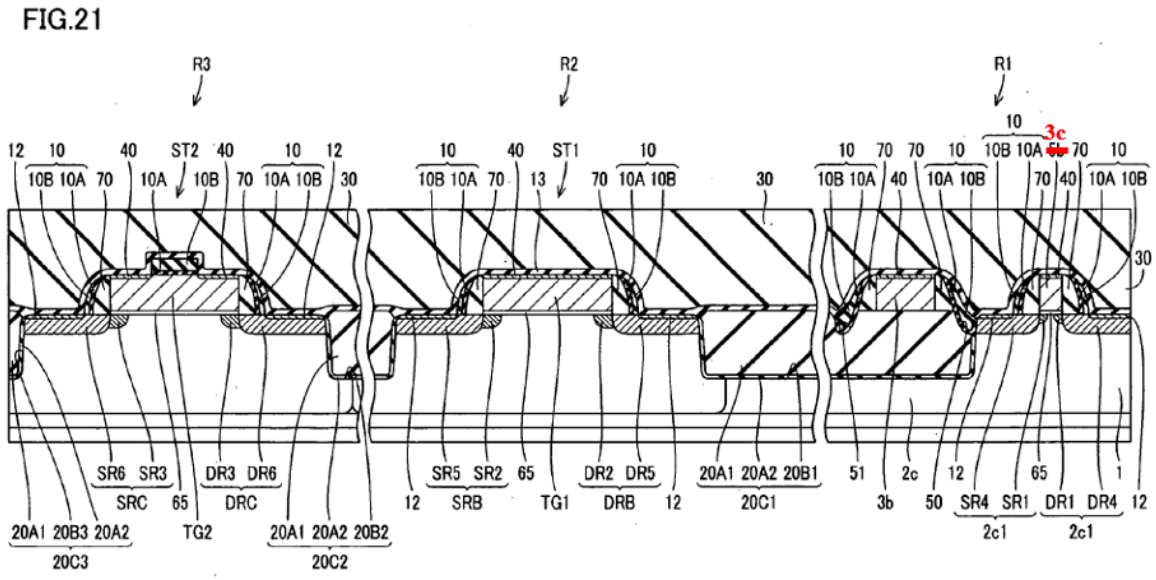


Saito825 FIG. 21 (corrected annotation).

Exemplary Disclosures
"On the main front surface of semiconductor substrate 100 in which memory cell region R1 is located, isolation region 20c1 and active region 2c specified by this isolation region 20c1 are formed. And on the main front surface of semiconductor substrate 100 in which active region 2c is located, gate insulating film 65, polysilicon wiring 5b [sic 3c] formed on the upper surface of this gate insulating film 65, and impurity diffused layer 2c1 located in the both sides of this polysilicon wiring 5b [sic 3c] are formed." Saito825 ¶ [0051]. "First load PMOS transistor P1 is formed in the intersection part of impurity diffusion region 2b1 comprising the region used as a source/drain, and polysilicon wiring 3b. Second access PMOS transistor P2 is formed in the intersection part of impurity diffusion region 2c1 comprising the region used as a source/drain, and polysilicon wiring 3c." Saito825 ¶ [0066]. "And on the main front surface of semiconductor substrate 100, a polysilicon film etc. is deposited and an impurity is introduced into this polysilicon film, for example. It patterns by using a photolithography etc. for the polysilicon film with which this impurity was introduced, and polysilicon wirings 5b [sic 3c] and 3b, and gate wiring TG1 and TG2 are formed." Saito825 ¶ [0093]. "In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g." Saito825 ¶ [0124]. Additionally, under Plaintiff's apparent interpretation of the claim language, the claimed "first gate electrode" may include a silicide film. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 11-13, 18, 20, 22, 24-25, 26, 39. Although TSMC does not necessarily agree with such an interpretation, Saito825 further discloses this element under this interpretation, as shown below. For example, Saito825 discloses silicide film 40 formed on PMOS gate electrode 3c. *See, e.g.*, the following: "Also on the upper surface of polysilicon wiring 3b, silicide film 40 which consists of a cobalt silicide film etc. is formed. And interlayer insulation film 30 is formed so that sidewall 70, polysilicon wiring 3b, and lamination insulating film 10 may be covered. This interlayer insulation film 30 is provided with insulating film 13 which is formed on silicide films 12 and 40 and consists of a plasma nitride (SiN) etc., insulating film 14 which is formed on insulating film 13 and consists of a HDP (high density plasma: High Density Plasma) film etc., insulating film 15 which is formed on this insulating film 14 and consists of a silicon oxide film formed

Exemplary Disclosures
by the CVD method using TEOS (Tetraethoxysilane) gas etc., and insulating film 16 formed on this insulating film 15." Saito825 ¶ [0080]. "FIG. 8 and FIG. 20 are the cross-sectional views showing the ninth step of the manufacturing process of semiconductor device 200. Since it fills up with lamination insulating film 10 in recess 50, it can suppress that the internal surface of recess 50 is exposed. And metallic films, such as cobalt (Co), are deposited, about 10 nm, on the main front surface of semiconductor substrate 100 by the sputtering method." Saito825 ¶ [0116]. "Then, heat treatment about more than 400° C. and below 600° C. is performed, silicon and cobalt react (silicidation), and silicide films 12 and 40 are formed. And wet etching removes unreacted cobalt. After an appropriate time, it heat-treats in the range of more than 700° C. and less than 800° C. Thus, silicide film 12 is formed on the front surface of impurity diffused layer 2c1, 2c1, SRB, DRB, SRC, and DRC. Silicide film 40 is formed on the upper surface of polysilicon wiring 5b [sic 3c] and 3b and gate wiring TG1. Since insulating films 10A and 10B remain on the upper surface of gate wiring TG2, silicide film 40 is formed on the upper surface of gate wiring TG2 which adjoins insulating films 10A and 10B." Saito825 ¶ [0117]. "Thus, when forming silicide films 12 and 40, the front surface of impurity diffused layer 2c1 exposed in recess 50 and the front surface of active region 2 located under impurity diffused layer 2c1 touch lamination insulating film 10 which consists of insulating film 10A and insulating film 10B. For this reason, it is suppressed that a silicide film is formed in the front surface of impurity diffused layer 2c1 located in recess 50 and the front surface of active region 2c located under impurity diffused layer 2c1." Saito825 ¶ [0118]. "In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g." Saito825 ¶ [0124]. *See also, e.g.*, Saito825 ¶ [0024], ¶ [0026], ¶ [0055], ¶¶ [0077]-[0084], ¶ [0104], ¶ [0107], ¶¶ [0116]-[0120], ¶¶ [0122]-[0124], FIGS. 3, 8-12, 20-21.

Exemplary Disclosures
To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
1[d] a first sidewall spacer formed on a side surface of the first gate electrode,
Saito825 discloses this feature. For example, Saito825 discloses PMOS sidewall oxide 70 formed on a side surface of PMOS gate electrode 3c (corrected from 5b). *See, e.g.*, the following: FIG.12      Saito825 FIG. 12 (corrected annotation).



Saito825 FIG. 21 (corrected annotation).

"On the main front surface of semiconductor substrate 100 in which memory cell region R1 is located, isolation region 20c1 and active region 2c specified by this isolation region 20c1 are formed. And on the main front surface of semiconductor substrate 100 in which active region 2c is located, gate insulating film 65, polysilicon wiring 5b [sic 3c] formed on the upper surface of this gate insulating film 65, and impurity diffused layer 2c1 located in the both sides of this polysilicon wiring 5b [sic 3c] are formed."

Saito825 ¶ [0051].

"Isolation region 20c1 is provided with trench 20B1 formed on the main front surface of semiconductor substrate 1, insulating film 20A2 which is formed on the internal surface of this trench 20B1, and consists of a silicon oxide film etc., and insulating film 20A1 which were formed on this insulating film 20A2 and with which it filled up in trench 20B. Insulating film 20A1 comprises a silicon oxide film etc., for example. And on isolation insulating film 20A1, polysilicon wiring (wiring layer) 3b is formed. On the both side surfaces of this polysilicon wiring 3b, sidewall (side wall oxide film) 70 which consists of a silicon oxide film etc. is formed, for example."

Saito825 ¶ [0070].

"FIG. 4 is a cross-sectional view showing the fifth step of the manufacturing process of semiconductor device 200. As shown in this FIG. 4, insulating film 70a which consists of a silicon oxide film etc. is deposited."

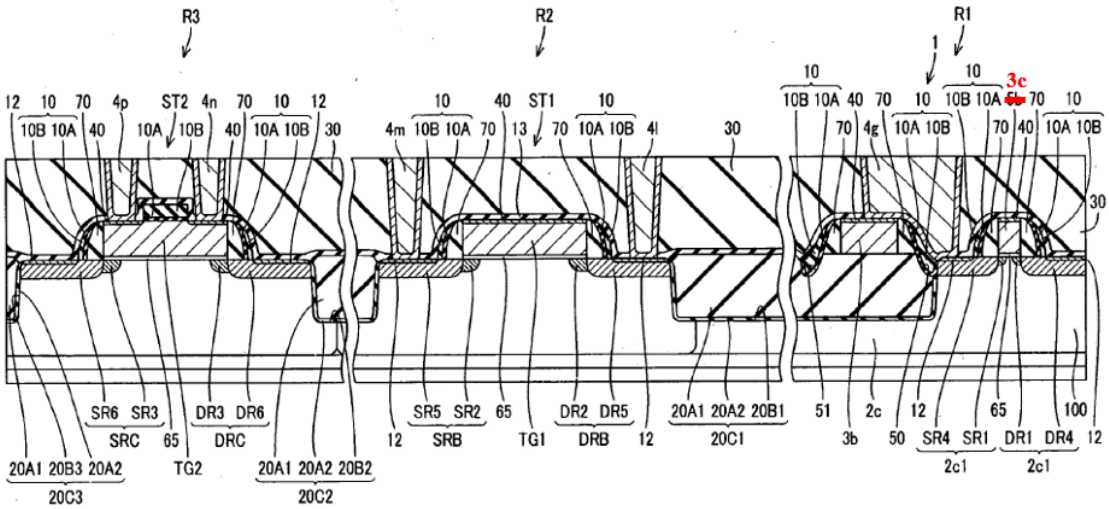
Saito825 ¶ [0095].

Exemplary Disclosures
"FIG. 5 and FIG. 17 are the cross-sectional views showing the sixth step of the manufacturing process of semiconductor device 200. As shown in this FIG. 5 and FIG. 17, it etches into insulating film 70a, and sidewall 70 is formed on the both side surfaces of gate wiring TG1, gate wiring TG2, polysilicon wiring 5b [sic 3c], and polysilicon wiring 3b." Saito825 ¶ [0096]. "On this occasion, the front surface at the side of impurity diffused layer SR1 among the front surfaces of isolation insulating film 20A1 is exposed from sidewall 70 formed on the side surface at the side of impurity diffused layer SR1 of polysilicon wiring 3b. Here, since isolation insulating film 20A1 and insulating film 20B1, and sidewall 70 comprise a homogeneous silicon oxide film etc., recess 50 is formed in the portion located in impurity diffused layer SR1 side from sidewall 70 among the front surfaces of isolation insulating film 20A1." Saito825 ¶ [0097]. "In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g." Saito825 ¶ [0124]. Additionally, under Plaintiff's apparent interpretation of the claim language, the claimed "first gate electrode" may include a silicide film. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 11-13, 18, 20, 22, 24-25, 26, 39. Although TSMC does not necessarily agree with such an interpretation, Saito825 further discloses this element under this interpretation, as shown below. For example, Saito825 discloses silicide film 40 formed on PMOS gate electrode 3c. *See, e.g.*, the following: "Also on the upper surface of polysilicon wiring 3b, silicide film 40 which consists of a cobalt silicide film etc. is formed. And interlayer insulation film 30 is formed so that sidewall 70, polysilicon wiring 3b, and lamination insulating film 10 may be covered. This interlayer insulation film 30 is provided with insulating film 13 which is formed on silicide films 12 and 40 and consists of a plasma nitride (SiN) etc., insulating film 14 which is formed on insulating film 13 and consists of a HDP (high density plasma: High Density Plasma) film etc., insulating film 15 which is formed on this insulating film 14 and consists of a silicon oxide film formed by the CVD method using TEOS (Tetraethoxysilane) gas etc., and insulating film 16 formed on this insulating film 15." Saito825 ¶ [0080].

Exemplary Disclosures
"FIG. 8 and FIG. 20 are the cross-sectional views showing the ninth step of the manufacturing process of semiconductor device 200. Since it fills up with lamination insulating film 10 in recess 50, it can suppress that the internal surface of recess 50 is exposed. And metallic films, such as cobalt (Co), are deposited, about 10 nm, on the main front surface of semiconductor substrate 100 by the sputtering method." Saito825 ¶ [0116]. "Then, heat treatment about more than 400° C. and below 600° C. is performed, silicon and cobalt react (silicidation), and silicide films 12 and 40 are formed. And wet etching removes unreacted cobalt. After an appropriate time, it heat-treats in the range of more than 700° C. and less than 800° C. Thus, silicide film 12 is formed on the front surface of impurity diffused layer 2c1, 2c1, SRB, DRB, SRC, and DRC. Silicide film 40 is formed on the upper surface of polysilicon wiring 5b [sic 3c] and 3b and gate wiring TG1. Since insulating films 10A and 10B remain on the upper surface of gate wiring TG2, silicide film 40 is formed on the upper surface of gate wiring TG2 which adjoins insulating films 10A and 10B." Saito825 ¶ [0117]. "Thus, when forming silicide films 12 and 40, the front surface of impurity diffused layer 2c1 exposed in recess 50 and the front surface of active region 2 located under impurity diffused layer 2c1 touch lamination insulating film 10 which consists of insulating film 10A and insulating film 10B. For this reason, it is suppressed that a silicide film is formed in the front surface of impurity diffused layer 2c1 located in recess 50 and the front surface of active region 2c located under impurity diffused layer 2c1." Saito825 ¶ [0118]. "In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g." Saito825 ¶ [0124]. *See also, e.g.*, Saito825 ¶ [0024], ¶ [0026], ¶ [0055], ¶¶ [0077]-[0084], ¶ [0104], ¶ [0107], ¶¶ [0116]-[0120], ¶¶ [0122]-[0124], FIGS. 3, 8-12, 17, 20-21. To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

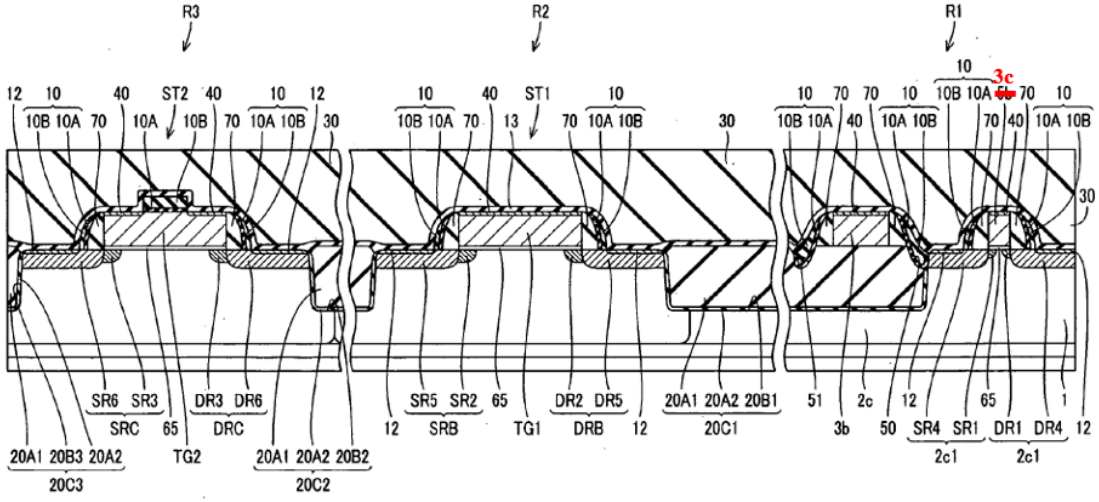
Exemplary Disclosures
1[e] a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and
Saito825 discloses a first source/drain region of a first conductivity type provided in the first active region on a lateral side of the first sidewall spacer. For example, Saito825 discloses a PMOS source/drain regions SR1, SR4, DR1, DR4 having a p-type conductivity provided in the PMOS active region on a lateral side of PMOS sidewall oxide 70. *See, e.g.*, the following:

FIG.12



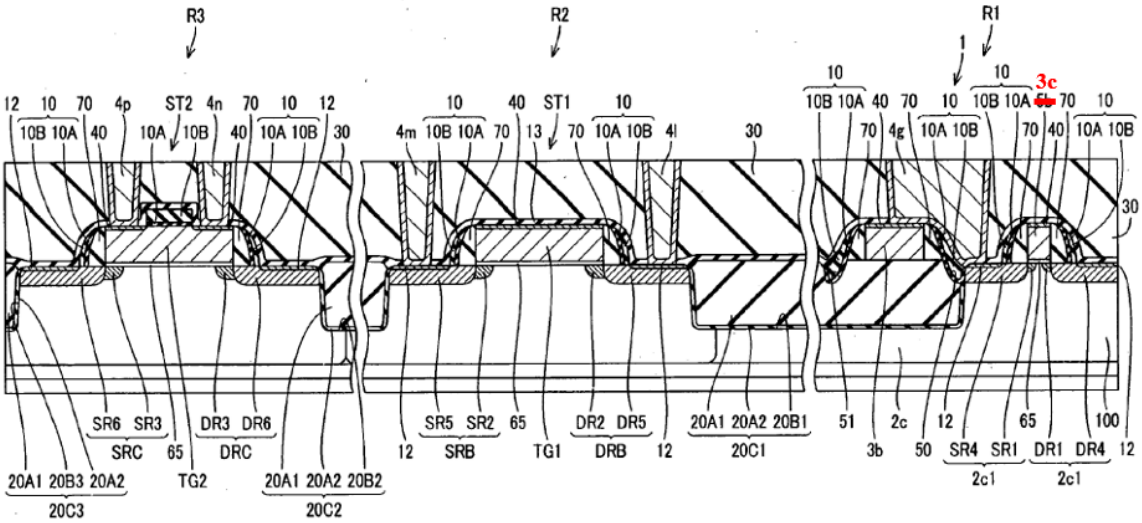
Saito825 FIG. 12 (corrected annotation).

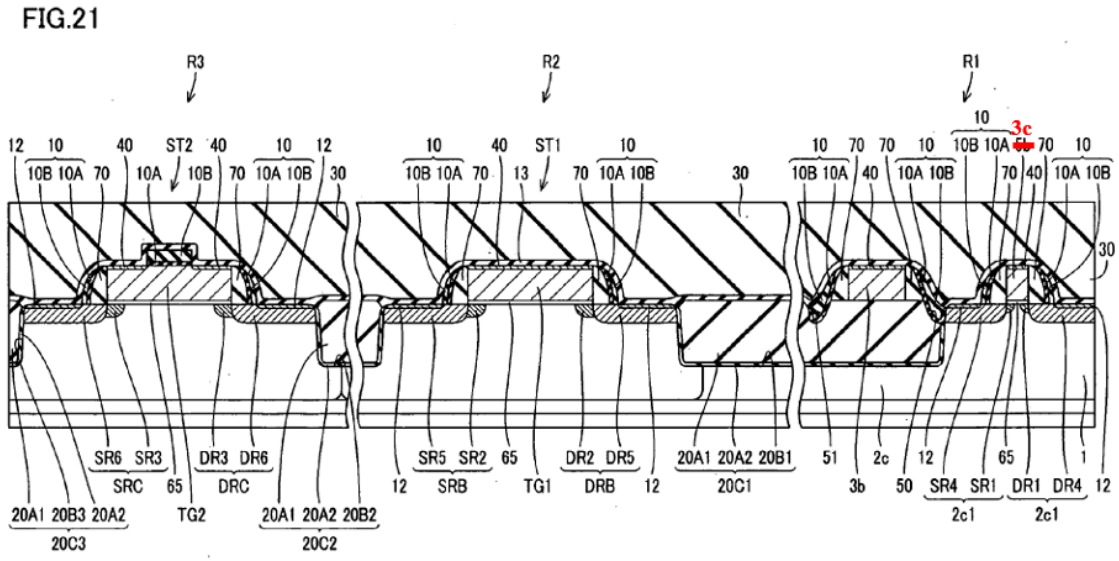
FIG.21



Saito825 FIG. 21 (corrected annotation).

Exemplary Disclosures
"On the main front surface of semiconductor substrate 100 in which memory cell region R1 is located, isolation region 20c1 and active region 2c specified by this isolation region 20c1 are formed. And on the main front surface of semiconductor substrate 100 in which active region 2c is located, gate insulating film 65, polysilicon wiring 5b [sic 3c] formed on the upper surface of this gate insulating film 65, and impurity diffused layer 2c1 located in the both sides of this polysilicon wiring 5b [sic 3c] are formed." Saito825 ¶ [0051]. "Here, each impurity diffused layer 2c1, SRB, DRB, SRC, and DRC separate a gap mutually, and are formed. In this embodiment, although silicide film 12 is formed on the upper surface of impurity diffused layer 2c1, SRB, DRB, SRC, and DRC, it is not restricted to this. For example, it is good also as forming a non-silicide region, without forming silicide film 12 in the upper surface of impurity diffused layers SRC and DRC." Saito825 ¶ [0055]. "In FIG. 5, recess 50 formed in the front surface of isolation insulating film 20A1 is formed among isolation insulating films 20A1 ranging from sidewall 70 formed on the side surface at the side of impurity diffused layer SR1 of polysilicon wiring 3b to impurity diffused layer SR1." Saito825 ¶ [0099]. "And a part of front surface of impurity diffused layer SR1 and a part of front surface of active region 2c which are located under impurity diffused layer SR1 are exposed to the internal surface of recess 50." Saito825 ¶ [0100]. "Then, as shown in FIG. 17, an impurity is introduced into the main front surface of semiconductor substrate 100 which adjoins polysilicon wiring 5b [sic 3c], and impurity diffused layer SR4 and DR4 are formed in it. Hereby, impurity diffused layer 2c1 which consists of impurity diffused layer SR1 and impurity diffused layer SR4 is formed in the main front surface of semiconductor substrate 100 located in one side surface side of polysilicon wiring 5b [sic 3c]. On the main front surface of semiconductor substrate 100 located in the other side surface side of polysilicon wiring 5b [sic 3c], impurity diffused layer 2c1 which consists of impurity diffused layer DR1 and impurity diffused layer DR4 is formed." Saito825 ¶ [0101]. To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

Exemplary Disclosures
1[f] which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region, and
Under Plaintiff's apparent interpretation of the claim language, the claimed "silicon compound layer" may include a silicide film. See AICP's P.R. 3-1 Disclosures, Ex. H, at 15, 20, 21, 25, 26, 31. Although TSMC disagrees with such an interpretation, Saito825 discloses a silicon compound layer under this interpretation, as shown below. For example, Saito825 discloses silicide films 12 formed on the PMOS source/drain regions SR4, DR4 in the PMOS active region. FIG.12    Saito825 FIG. 12 (corrected annotation).



Saito825 FIG. 21 (corrected annotation).

"Here, at least one side of insulating films 10A and 10B has covered the front surface of impurity diffused layer 2c1 located in recess 50. It is suppressed that silicide film 12 is formed in impurity diffused layer 2c1 and the front surface of active region 2c among the internal surfaces of recess 50."

Saito825 ¶ [0078].

"Thus, since it is suppressed that silicide film 12 contacts the front surface of active region 2c located in recess 50, it is suppressed that leakage current arises from silicide film 12 to semiconductor substrate 100. Thus, since it is suppressed that the leakage current from silicide film 12 to semiconductor substrate 100 occurs, reduction of consumed electric power can be aimed at and suppression of a generation of malfunction can be aimed at further."

Saito825 ¶ [0079].

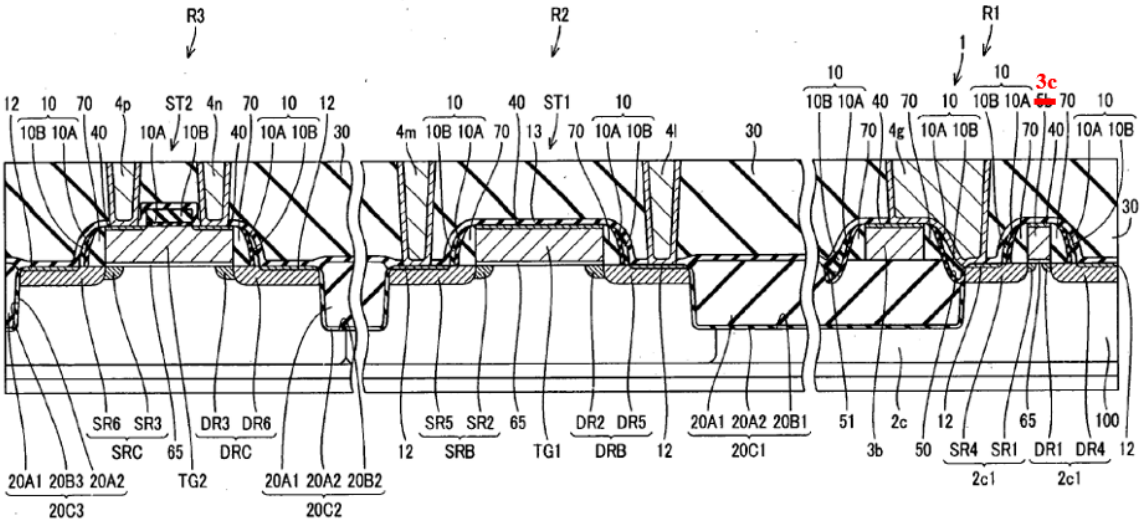
"FIG. 8 and FIG. 20 are the cross-sectional views showing the ninth step of the manufacturing process of semiconductor device 200. Since it fills up with lamination insulating film 10 in recess 50, it can suppress that the internal surface of recess 50 is exposed. And metallic films, such as cobalt (Co), are deposited, about 10 nm, on the main front surface of semiconductor substrate 100 by the sputtering method."

Saito825 ¶ [0116].

Exemplary Disclosures
"Then, heat treatment about more than 400° C. and below 600° C. is performed, silicon and cobalt react (silicidation), and silicide films 12 and 40 are formed. And wet etching removes unreacted cobalt. After an appropriate time, it heat-treats in the range of more than 700° C. and less than 800° C. Thus, silicide film 12 is formed on the front surface of impurity diffused layer 2c1, 2c1, SRB, DRB, SRC, and DRC. Silicide film 40 is formed on the upper surface of polysilicon wiring 5b [sic 3c] and 3b and gate wiring TG1. Since insulating films 10A and 10B remain on the upper surface of gate wiring TG2, silicide film 40 is formed on the upper surface of gate wiring TG2 which adjoins insulating films 10A and 10B." Saito825 ¶ [0117]. "Thus, when forming silicide films 12 and 40, the front surface of impurity diffused layer 2c1 exposed in recess 50 and the front surface of active region 2 located under impurity diffused layer 2c1 touch lamination insulating film 10 which consists of insulating film 10A and insulating film 10B. For this reason, it is suppressed that a silicide film is formed in the front surface of impurity diffused layer 2c1 located in recess 50 and the front surface of active region 2c located under impurity diffused layer 2c1." Saito825 ¶ [0118]. "That is, it is suppressed that silicide film 12 formed on the upper surface of impurity diffused layer 2c1 reaches even the front surface of active region 2c which is located under impurity diffused layer 2c1 extending and existing even over the internal surface of recess 50. For this reason, it can suppress that silicide film 12 formed and semiconductor substrate 100 are electrically connected." Saito825 ¶ [0119]. "In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g." Saito825 ¶ [0124]. To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

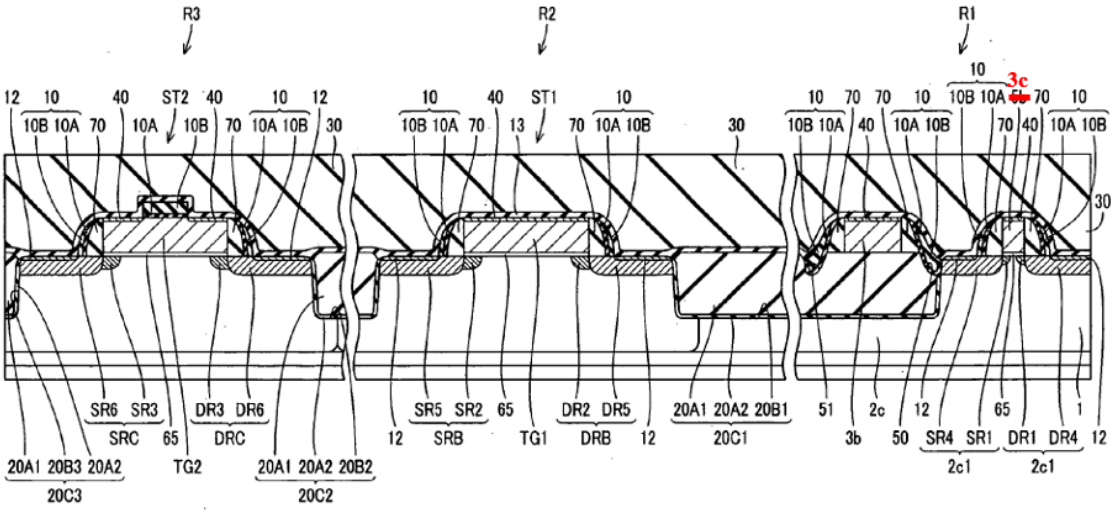
Exemplary Disclosures
1[g] a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and
Saito825 discloses this feature. For example, Saito825 discloses insulating layer 13 formed on the PMOS active region to cover PMOS gate electrode 3c (corrected from 5b), PMOS sidewall oxide 70, and PMOS source/drain regions SR4, DR4. *See, e.g.*, the following:

FIG.12



Saito825 FIG. 12 (corrected annotation).

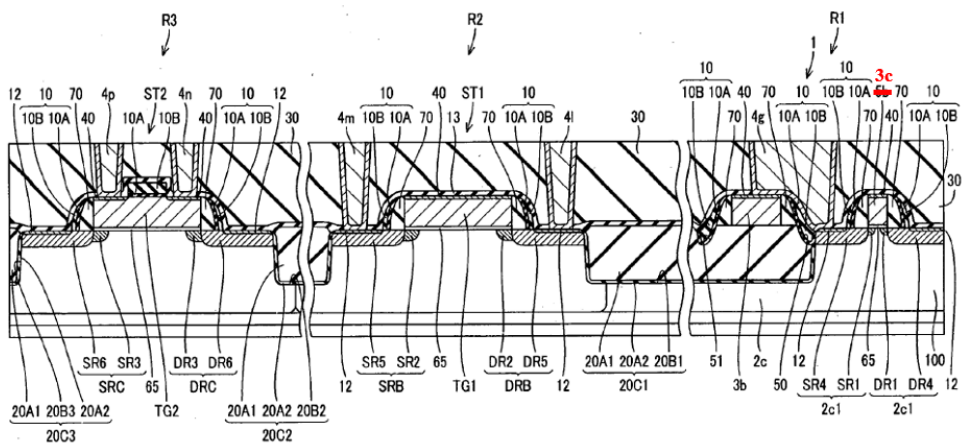
FIG.21

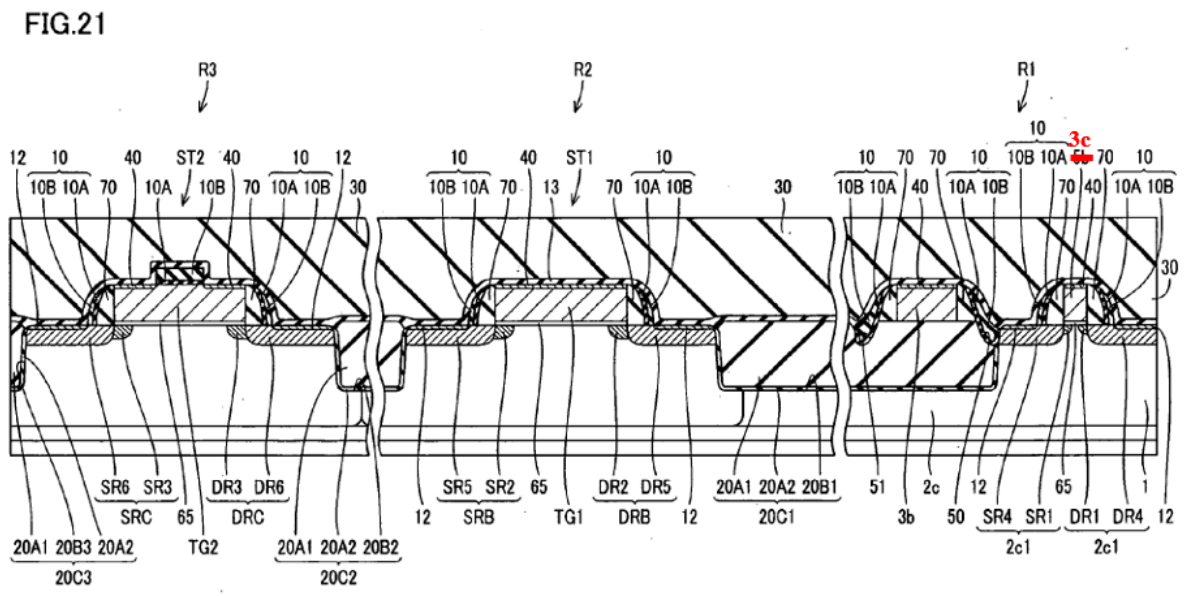


Saito825 FIG. 21 (corrected annotation).

Exemplary Disclosures
"Also on the upper surface of polysilicon wiring 3b, silicide film 40 which consists of a cobalt silicide film etc. is formed. And interlayer insulation film 30 is formed so that sidewall 70, polysilicon wiring 3b, and lamination insulating film 10 may be covered. This interlayer insulation film 30 is provided with insulating film 13 which is formed on silicide films 12 and 40 and consists of a plasma nitride (SiN) etc., insulating film 14 which is formed on insulating film 13 and consists of a HDP (high density plasma: High Density Plasma) film etc., insulating film 15 which is formed on this insulating film 14 and consists of a silicon oxide film formed by the CVD method using TEOS (Tetraethoxysilane) gas etc., and insulating film 16 formed on this insulating film 15." Saito825 ¶ [0080]. "And insulating film 14 which consists of a HDP (high density plasma: High Density Plasma) film etc. is formed on this insulating film 13. On this insulating film 14, insulating film 15 is formed with the CVD method which used for example, TEOS (Tetraethoxysilane) gas. Insulating film 16 is formed on the upper surface of insulating film 15, and interlayer insulation film 30 is formed." Saito825 ¶ [0120]. A POSITA would have understood the stress insulating layer extends over the PMOS gate electrodes and between neighboring transistors. Although the contact plugs (FIG. 12) penetrate the stress insulating film (FIG. 12) in the cross-section shown above, a POSITA would have understood the stress insulating film extends unbroken between neighboring transistors in other cross-sections, where the contact plugs are not formed, such as in cross-sections located behind and in front of the one shown above. Additionally, under Plaintiff's apparent interpretation of the claim language, the claimed "first gate electrode" may include a silicide film. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 11-13, 18, 20, 22, 24-25, 26, 39. Although TSMC does not necessarily agree with such an interpretation, Saito825 further discloses this element under this interpretation, as shown below. For example, Saito825 discloses silicide film 40 formed on PMOS gate electrode 3c. *See, e.g.*, the following: "Also on the upper surface of polysilicon wiring 3b, silicide film 40 which consists of a cobalt silicide film etc. is formed. And interlayer insulation film 30 is formed so that sidewall 70, polysilicon wiring 3b, and lamination insulating film 10 may be covered. This interlayer insulation film 30 is provided with insulating film 13 which is formed on silicide films 12 and 40 and consists of a plasma nitride (SiN) etc., insulating film 14 which is formed on insulating film 13 and consists of a HDP (high density plasma: High Density Plasma) film etc., insulating film 15 which is formed on this insulating film 14 and consists of a silicon oxide film formed by the CVD method using TEOS (Tetraethoxysilane) gas etc., and insulating film 16 formed on this insulating film 15." Saito825 ¶ [0080].

Exemplary Disclosures
"FIG. 8 and FIG. 20 are the cross-sectional views showing the ninth step of the manufacturing process of semiconductor device 200. Since it fills up with lamination insulating film 10 in recess 50, it can suppress that the internal surface of recess 50 is exposed. And metallic films, such as cobalt (Co), are deposited, about 10 nm, on the main front surface of semiconductor substrate 100 by the sputtering method." Saito825 ¶ [0116]. "Then, heat treatment about more than 400° C. and below 600° C. is performed, silicon and cobalt react (silicidation), and silicide films 12 and 40 are formed. And wet etching removes unreacted cobalt. After an appropriate time, it heat-treats in the range of more than 700° C. and less than 800° C. Thus, silicide film 12 is formed on the front surface of impurity diffused layer 2c1, 2c1, SRB, DRB, SRC, and DRC. Silicide film 40 is formed on the upper surface of polysilicon wiring 5b [sic 3c] and 3b and gate wiring TG1. Since insulating films 10A and 10B remain on the upper surface of gate wiring TG2, silicide film 40 is formed on the upper surface of gate wiring TG2 which adjoins insulating films 10A and 10B." Saito825 ¶ [0117]. "Thus, when forming silicide films 12 and 40, the front surface of impurity diffused layer 2c1 exposed in recess 50 and the front surface of active region 2 located under impurity diffused layer 2c1 touch lamination insulating film 10 which consists of insulating film 10A and insulating film 10B. For this reason, it is suppressed that a silicide film is formed in the front surface of impurity diffused layer 2c1 located in recess 50 and the front surface of active region 2c located under impurity diffused layer 2c1." Saito825 ¶ [0118]. "In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g." Saito825 ¶ [0124]. *See also, e.g.*, Saito825 ¶ [0024], ¶ [0026], ¶ [0055], ¶¶ [0077]-[0084], ¶ [0104], ¶ [0107], ¶¶ [0116]-[0120], ¶¶ [0122]-[0124], FIGS. 3, 8-12, 20-21. To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

Exemplary Disclosures
1[h] which causes a second stress opposite to the first stress,
To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
1[i] an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode,
To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
1[j] a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer,
Under Plaintiff's apparent interpretation of the claim language, the claimed "first stress-relief film . . . formed space between the silicon compound layer and the first sidewall spacer" need not be formed in a "space" at all, and a silicon oxide buffer layer located underneath the stress insulating film satisfies the claim language. See AICP's P.R. 3-1 Disclosures, Ex. H, at 21. Although TSMC disagrees with such an interpretation, Saito825 discloses [1j] under this interpretation, as shown below. For example, under Plaintiff's apparent interpretation, Saito825 discloses insulting film 10A (silicon oxide) formed in a space between silicide layers 12 on PMOS source/drain regions SR4, DR4 and PMOS sidewall oxide 70. *See, e.g.*, the following: FIG.12    Saito825 FIG. 12 (corrected annotation).



Saito825 FIG. 21 (corrected annotation).

"Even if it is the semiconductor device provided with the wiring on an isolation insulating film, the sidewall formed on the side surface of this wiring, and the shared contact which connects the wiring and the impurity diffusion on an active region, the semiconductor device which can suppress the generation of the leakage current from shared contact to a semiconductor substrate, and its manufacturing method are offered. The semiconductor device concerning the present invention is provided with an isolation insulating film selectively formed on the main front surface of a semiconductor substrate, an active region specified by an isolation insulating film on the main front surface of a semiconductor substrate, a recess which reaches an active region on the isolation insulating film, the first insulating film formed so that a recess might be covered, the second insulating film which is formed on a first insulating film, is filled up with a recess, and differs in a material from the first insulating film, an impurity diffused layer formed on the main front surface of the active region of the position which adjoins the recess, and an electric conduction film formed on the impurity diffused layer."

Saito825 Abstract.

"Recess 50 which reaches active region 2c from sidewall 70 is formed in isolation insulating film 20A1. For this reason, the internal surface of recess 50 includes a part of front surface of impurity diffused layer 2c1, a part of front surface of active region 2c located under impurity diffused layer 2c1, and a part of front surface of isolation insulating film 20A1. And insulating film 10A which consists of a silicon oxide film etc. is formed so that the front surface of this recess 50 may be covered. The thickness of insulating film 10A of the vertical direction to the main front surface of semiconductor substrate 100 is about 20 nm in the parallel portion to the main front surface of semiconductor substrate 100. This insulating film 10A is formed on the side surface of sidewall 70 while it covers the internal surface of recess 50. On this insulating

Exemplary Disclosures
film 10A, insulating film 10B from which material differs in insulating film 10A, for example, the insulating film which consists of a silicon nitride film etc., is formed." Saito825 ¶ [0074]. "It fills up with this insulating film 10B in recess 50, and fills up with insulating film 10B to opening edge 50a of recess 50. And insulating film 10B is extending and existing even on the side surface of sidewall 70 via insulating film 10A. The thickness of this insulating film 10B of the vertical direction to the main front surface of semiconductor substrate 100 is formed more thickly than the thickness of insulating film 10A, for example, is about 80 nm. This insulating film 10B is an insulating film which consists of different material from insulating film 10A, for example, consists of a silicon nitride film etc. The insulating film which differs in material from insulating film 10A in this specification means that, when etching insulating film 10A, the etch rate difference of insulating film 10A including a silicon oxide film and insulating film 10B is larger than the etch rate difference of semiconductor substrate 100 of a P type, and a silicon oxide film. Preferably, insulating film 10B is formed with material including a silicon nitride film (Si3N4)." Saito825 ¶ [0075]. "Thus, the inside of recess 50 is embedded by lamination insulating film 10 which consists of a plurality of insulating films 10A and 10B with a big difference of an etch rate. The outer edge section at the side of active region 2c of lamination insulating film 10 is located near the opening edge 50a of recess 50, and it is formed so that the upper surface of active region 2c may hardly be covered. Here, at least one side of insulating films 10A and 10B is formed so that the front surface of impurity diffused layer 2c1 may be contacted among the internal surfaces of recess 50. For this reason, the front surface of impurity diffused layer 2c1 located in recess 50 is covered with lamination insulating film 10. In particular, in Embodiment 1, among the internal surfaces of recess 50, at least, insulating film 10A is crossed to opening edge 50 a from the bottom of recess 50, and it is formed so that the internal surface of recess 50 may be contacted. For this reason, among the internal surfaces of recess 50, the front surface of impurity diffused layer 2c1, and active region 2c located under impurity diffused layer 2c1 contacts insulating film 10A, and is covered with insulating film 10A." Saito825 ¶ [0076]. "FIG. 6 and FIG. 18 are the cross-sectional views showing the seventh step of the manufacturing process of semiconductor device 200. As shown in this FIG. 6 and FIG. 18, it is a region including recess 50 and insulating film 10A which consists of a silicon oxide film etc. is formed as a silicide protection film on the main front surface of semiconductor substrate 100, for example. For example, about 20 nm-30 nm of insulating films 10A are deposited by the CVD method (Chemical Vapor Deposition) method using TEOS (Tetraethoxysilane) gas. Since the

Exemplary Disclosures
depth of recess 50 is set to about 60 nm in many cases, for example, insulating film 10A is formed so that it may go along on the front surface of recess 50." Saito825 ¶ [0104]. "And after forming insulating film 10A, about 80 nm-100 nm of insulating films 10B which consist of a silicon nitride film etc. are formed with a CVD method etc. on insulating film 10A, for example. Thus, insulating film 10B is deposited so that the thickness of deposited insulating film 10B may become thick rather than the depth of recess 50." Saito825 ¶ [0105]. "FIG. 7 and FIG. 19 are the cross-sectional views showing the eighth step of the manufacturing process of semiconductor device 200. In this FIG. 7 and FIG. 19, it patterns to a silicide protection film first. It etches into insulating film 10B by using insulating film 10A as a stopper. Here, insulating film 10A consists of a silicon oxide film etc., and insulating film 10B consists of a silicon nitride film etc. For this reason, when etching insulating film 10B, the large selection ratio of etching is taken so that the side of a silicon nitride film may become easier to etch than a silicon oxide film. For this reason, insulating film 10A can be operated good as a stopper. When etching into insulating film 10B, it can suppress etching to the main front surface of semiconductor substrate 100." Saito825 ¶ [0107]. "In this embodiment, as a combination of insulating film 10A and insulating film 10B, as mentioned above, insulating film 10A was made into the silicon oxide film, and insulating film 10B was made into the silicon nitride film. Besides it, for example, insulating film 10A is made into a silicon oxide film, and it is good also considering insulating film 10B as a silicon oxynitride (SiON) film. In order to form insulating film 10B which consists of a silicon oxynitride film, a silicon oxide film is formed on insulating film 10B, and it forms by annealing in NO and N2O atmosphere, for example." Saito825 ¶ [0108]. "As a combination of insulating film 10A and insulating film 10B, insulating film 10A is made into a silicon oxide film, and it is good also considering insulating film 10B as a SOG (liquid glass: spin on glass) film. Thus, by adopting a SOG film as insulating film 10B, SOG liquid enters easily in recess 50, and it can suppress that a seam etc. is formed." Saito825 ¶ [0109]. "As a combination of insulating film 10A and insulating film 10B, insulating film 10A is made into a silicon oxide film, and it is good also considering insulating film 10B as a plasma nitride (SiN) film. Form degradation of sidewall 70 can be suppressed by using a plasma nitride film as insulating film 10B. As insulating film 10A, a silicon oxide film is formed with the CVD

Exemplary Disclosures
method using TEOS (Tetraethoxysilane) gas etc., and it is good also considering insulating film 10B as a HDP (high density plasma: High Density Plasma) film." Saito825 ¶ [0110]. "Thus, all of insulating films 10A and 10B can distinguish between the etch rate of formed insulating films 10A and 10B with each manufacturing method. Insulating film 10A can be operated as a stopper at the time of etching insulating film 10B." Saito825 ¶ [0111]. "And when insulating film 10A formed on the upper surface of impurity diffusion region 2c1 and the upper surface of polysilicon wiring 3b is exposed, etching of insulating film 10B is stopped. Here, the thickness of insulating film 10B formed on recess 50 and sidewall 70 is formed more thickly than insulating film 10B formed on impurity diffusion region 2c1 and polysilicon wiring 3b. For this reason, when upper surface of polysilicon wiring 3b and upper surface of impurity diffusion region 2c1 is exposed, the inside of recess 50 will be in the state where insulating film 10B was filled up. It will be in the state where insulating film 10B remained also on sidewall 70." Saito825 ¶ [0112]. "Thus, after etching into insulating film 10B, it etches into insulating film 10A, and upper surface of impurity diffusion region 2c1 and upper surface of polysilicon wiring 3b is exposed. Here, since the thickness of insulating film 10A is formed in about 20 nm filmy, the upper surface of impurity diffusion region 2c1 and the upper surface of polysilicon wiring 3b can be exposed by performing light etching to insulating film 10A. For this reason, it can suppress that an etching damage is given to the upper surface of impurity diffusion region 2c1, and the upper surface of polysilicon wiring 3b. Thus, in recesses 50 and 51, insulating film 10A formed along the internal surface of recesses 50 and 51 and insulating film 10B which is formed on the upper surface of this insulating film 10A, and fills up the inside of recesses 50 and 51 are formed." Saito825 ¶ [0113]. "In FIG. 7, by etching into insulating film 10A, lamination insulating film 10 which consists of insulating film 10A and insulating film 10B is formed over the upper surface of sidewall 70 from the boundary region of the upper surface and the side surface of active region 2c, and it fills up with it in recess 50. And the edges of lamination insulating film 10 are smoothly formed successively to the upper surface of exposed impurity diffusion region 2c1. The upper surface of lamination insulating film 10 is made into the smooth curving surface ranging from the upper surface side of impurity diffusion region 2c1 to the sidewall 70 side. Here, a part of front surface of impurity diffused layer 2c1 exposed in recess 50 and a part of front surface of active region 2c which are located under impurity diffused layer 2c1 touch either insulating film 10A or insulating film 10B at least." Saito825 ¶ [0114].

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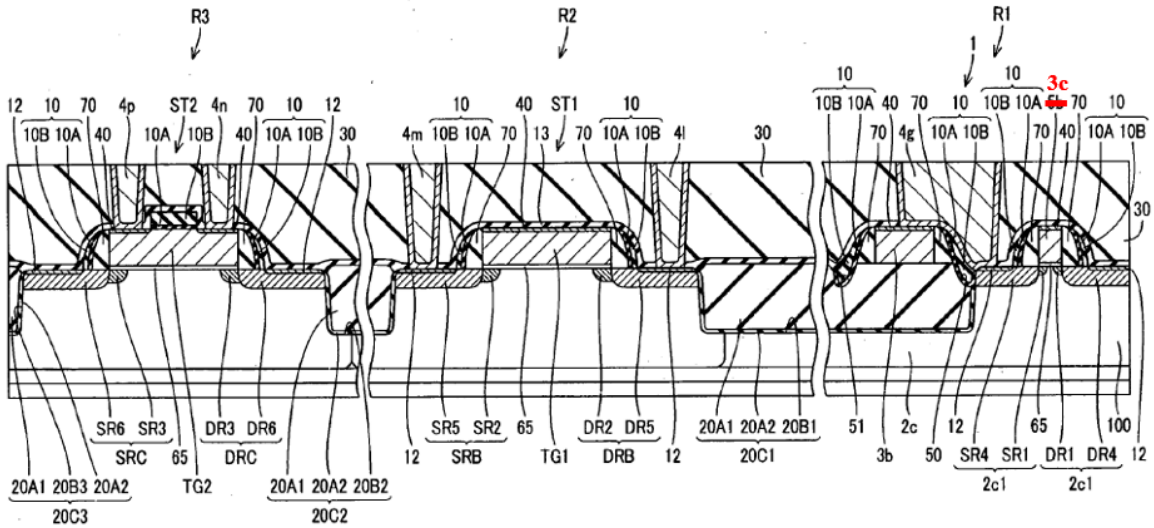
Additionally, under Plaintiff's apparent interpretation of the claim language, the claimed "silicon compound layer" may include a silicide film. See AICP's P.R. 3-1 Disclosures, Ex. H, at 15, 20, 21, 25, 26, 31. Although TSMC disagrees with such an interpretation, Saito825 further discloses [1j] under this interpretation (and subject to the additional caveats noted above), as the annotated image below demonstrates. "Here, at least one side of insulating films 10A and 10B has covered the front surface of impurity diffused layer 2c1 located in recess 50. It is suppressed that silicide film 12 is formed in impurity diffused layer 2c1 and the front surface of active region 2c among the internal surfaces of recess 50." Saito825 ¶ [0078]. "Thus, since it is suppressed that silicide film 12 contacts the front surface of active region 2c located in recess 50, it is suppressed that leakage current arises from silicide film 12 to semiconductor substrate 100. Thus, since it is suppressed that the leakage current from silicide film 12 to semiconductor substrate 100 occurs, reduction of consumed electric power can be aimed at and suppression of a generation of malfunction can be aimed at further." Saito825 ¶ [0079]. "FIG. 8 and FIG. 20 are the cross-sectional views showing the ninth step of the manufacturing process of semiconductor device 200. Since it fills up with lamination insulating film 10 in recess 50, it can suppress that the internal surface of recess 50 is exposed. And metallic films, such as cobalt (Co), are deposited, about 10 nm, on the main front surface of semiconductor substrate 100 by the sputtering method." Saito825 ¶ [0116]. "Then, heat treatment about more than 400° C. and below 600° C. is performed, silicon and cobalt react (silicidation), and silicide films 12 and 40 are formed. And wet etching removes unreacted cobalt. After an appropriate time, it heat-treats in the range of more than 700° C. and less than 800° C. Thus, silicide film 12 is formed on the front surface of impurity diffused layer 2c1, 2c1, SRB, DRB, SRC, and DRC. Silicide film 40 is formed on the upper surface of polysilicon wiring 5b [sic 3c] and 3b and gate wiring TG1. Since insulating films 10A and 10B remain on the upper surface of gate wiring TG2, silicide film 40 is formed on the upper surface of gate wiring TG2 which adjoins insulating films 10A and 10B." Saito825 ¶ [0117].

Exemplary Disclosures
"Thus, when forming silicide films 12 and 40, the front surface of impurity diffused layer 2c1 exposed in recess 50 and the front surface of active region 2 located under impurity diffused layer 2c1 touch lamination insulating film 10 which consists of insulating film 10A and insulating film 10B. For this reason, it is suppressed that a silicide film is formed in the front surface of impurity diffused layer 2c1 located in recess 50 and the front surface of active region 2c located under impurity diffused layer 2c1." Saito825 ¶ [0118]. "That is, it is suppressed that silicide film 12 formed on the upper surface of impurity diffused layer 2c1 reaches even the front surface of active region 2c which is located under impurity diffused layer 2c1 extending and existing even over the internal surface of recess 50. For this reason, it can suppress that silicide film 12 formed and semiconductor substrate 100 are electrically connected." Saito825 ¶ [0119]. "In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g." Saito825 ¶ [0124]. To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

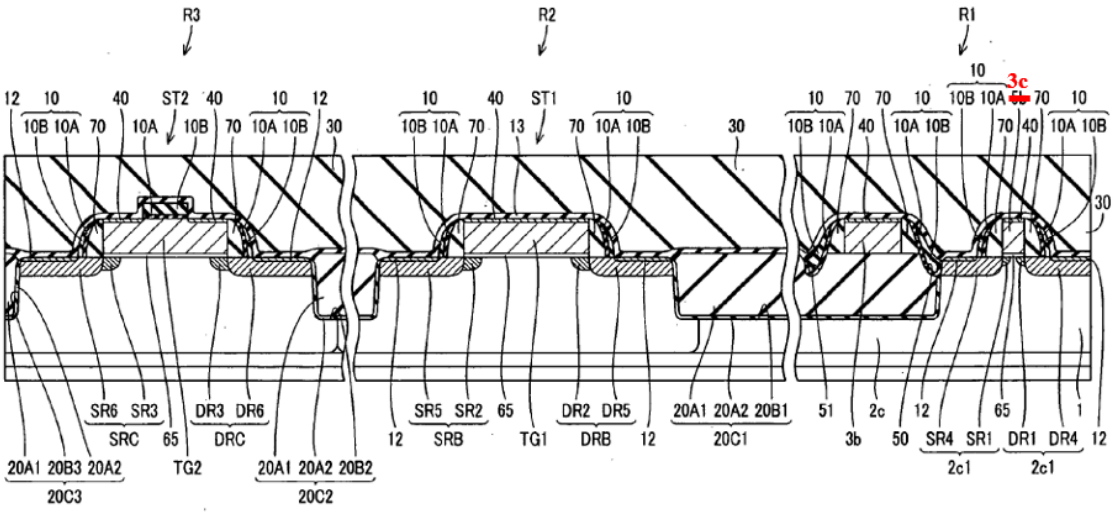
Exemplary Disclosures
1[k] the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween, and
Saito825 discloses this feature. For example, Saito825 discloses insulating film 10A formed on a side surface of PMOS gate electrode 3c (corrected from 5b) with PMOS sidewall oxide 70 therebetween. *See, e.g.*, the following:

FIG.12



Saito825 FIG. 12 (corrected annotation).

FIG.21



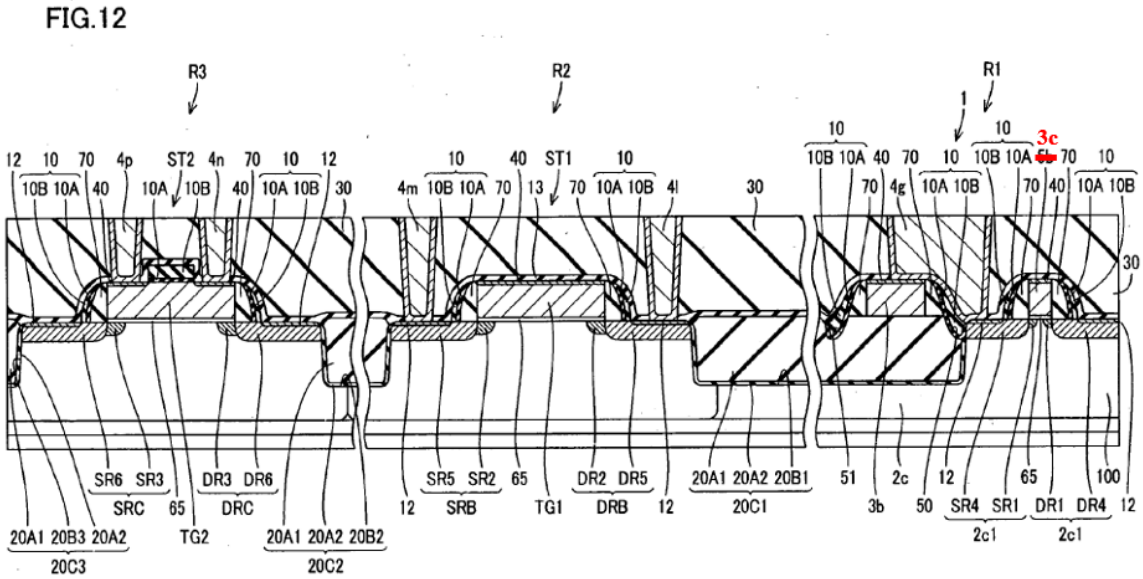
Saito825 FIG. 21 (corrected annotation).

Exemplary Disclosures
"Even if it is the semiconductor device provided with the wiring on an isolation insulating film, the sidewall formed on the side surface of this wiring, and the shared contact which connects the wiring and the impurity diffusion on an active region, the semiconductor device which can suppress the generation of the leakage current from shared contact to a semiconductor substrate, and its manufacturing method are offered. The semiconductor device concerning the present invention is provided with an isolation insulating film selectively formed on the main front surface of a semiconductor substrate, an active region specified by an isolation insulating film on the main front surface of a semiconductor substrate, a recess which reaches an active region on the isolation insulating film, the first insulating film formed so that a recess might be covered, the second insulating film which is formed on a first insulating film, is filled up with a recess, and differs in a material from the first insulating film, an impurity diffused layer formed on the main front surface of the active region of the position which adjoins the recess, and an electric conduction film formed on the impurity diffused layer." Saito825 Abstract. "Recess 50 which reaches active region 2c from sidewall 70 is formed in isolation insulating film 20A1. For this reason, the internal surface of recess 50 includes a part of front surface of impurity diffused layer 2c1, a part of front surface of active region 2c located under impurity diffused layer 2c1, and a part of front surface of isolation insulating film 20A1. And insulating film 10A which consists of a silicon oxide film etc. is formed so that the front surface of this recess 50 may be covered. The thickness of insulating film 10A of the vertical direction to the main front surface of semiconductor substrate 100 is about 20 nm in the parallel portion to the main front surface of semiconductor substrate 100. This insulating film 10A is formed on the side surface of sidewall 70 while it covers the internal surface of recess 50. On this insulating film 10A, insulating film 10B from which material differs in insulating film 10A, for example, the insulating film which consists of a silicon nitride film etc., is formed." Saito825 ¶ [0074]. "It fills up with this insulating film 10B in recess 50, and fills up with insulating film 10B to opening edge 50a of recess 50. And insulating film 10B is extending and existing even on the side surface of sidewall 70 via insulating film 10A. The thickness of this insulating film 10B of the vertical direction to the main front surface of semiconductor substrate 100 is formed more thickly than the thickness of insulating film 10A, for example, is about 80 nm. This insulating film 10B is an insulating film which consists of different material from insulating film 10A, for example, consists of a silicon nitride film etc. The insulating film which differs in material from insulating film 10A in this specification means that, when etching insulating film 10A, the etch rate difference of insulating film 10A including a silicon oxide film and insulating film 10B is larger than the etch rate difference of semiconductor substrate 100 of a P type, and a silicon oxide film. Preferably, insulating film 10B is formed with material including a silicon nitride film (Si3N4)." Saito825 ¶ [0075].

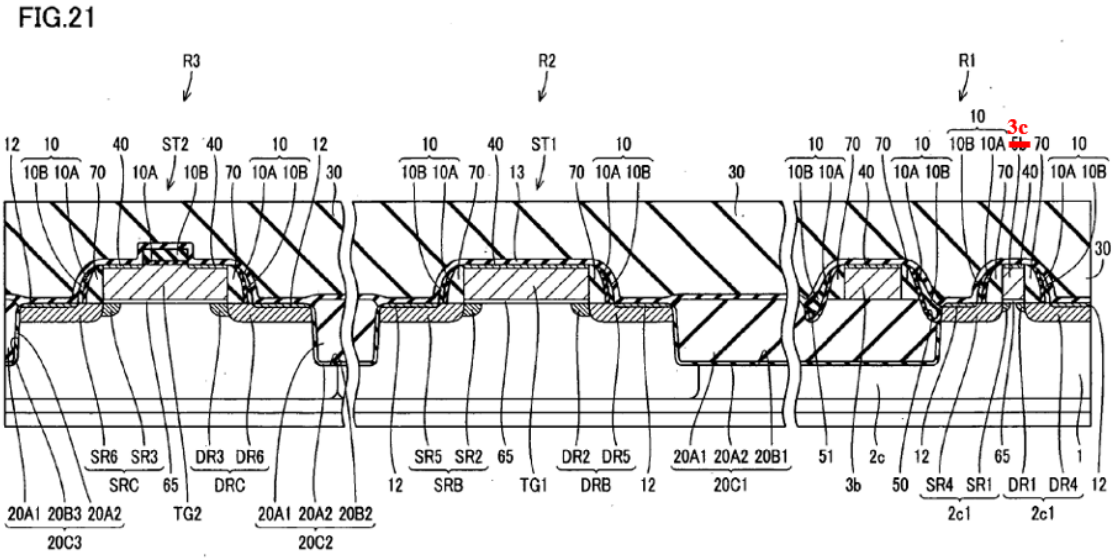
Exemplary Disclosures
"Thus, the inside of recess 50 is embedded by lamination insulating film 10 which consists of a plurality of insulating films 10A and 10B with a big difference of an etch rate. The outer edge section at the side of active region 2c of lamination insulating film 10 is located near the opening edge 50a of recess 50, and it is formed so that the upper surface of active region 2c may hardly be covered. Here, at least one side of insulating films 10A and 10B is formed so that the front surface of impurity diffused layer 2c1 may be contacted among the internal surfaces of recess 50. For this reason, the front surface of impurity diffused layer 2c1 located in recess 50 is covered with lamination insulating film 10. In particular, in Embodiment 1, among the internal surfaces of recess 50, at least, insulating film 10A is crossed to opening edge 50 a from the bottom of recess 50, and it is formed so that the internal surface of recess 50 may be contacted. For this reason, among the internal surfaces of recess 50, the front surface of impurity diffused layer 2c1, and active region 2c located under impurity diffused layer 2c1 contacts insulating film 10A, and is covered with insulating film 10A." Saito825 ¶ [0076]. "FIG. 6 and FIG. 18 are the cross-sectional views showing the seventh step of the manufacturing process of semiconductor device 200. As shown in this FIG. 6 and FIG. 18, it is a region including recess 50 and insulating film 10A which consists of a silicon oxide film etc. is formed as a silicide protection film on the main front surface of semiconductor substrate 100, for example. For example, about 20 nm-30 nm of insulating films 10A are deposited by the CVD method (Chemical Vapor Deposition) method using TEOS (Tetraethoxysilane) gas. Since the depth of recess 50 is set to about 60 nm in many cases, for example, insulating film 10A is formed so that it may go along on the front surface of recess 50." Saito825 ¶ [0104]. "And after forming insulating film 10A, about 80 nm-100 nm of insulating films 10B which consist of a silicon nitride film etc. are formed with a CVD method etc. on insulating film 10A, for example. Thus, insulating film 10B is deposited so that the thickness of deposited insulating film 10B may become thick rather than the depth of recess 50." Saito825 ¶ [0105]. "FIG. 7 and FIG. 19 are the cross-sectional views showing the eighth step of the manufacturing process of semiconductor device 200. In this FIG. 7 and FIG. 19, it patterns to a silicide protection film first. It etches into insulating film 10B by using insulating film 10A as a stopper. Here, insulating film 10A consists of a silicon oxide film etc., and insulating film 10B consists of a silicon nitride film etc. For this reason, when etching insulating film 10B, the large selection ratio of etching is taken so that the side of a silicon nitride film may become easier to etch than a silicon oxide film. For this reason, insulating film 10A can be operated good as a stopper. When etching into insulating film 10B, it can suppress etching to the main front surface of semiconductor substrate 100." Saito825 ¶ [0107].

Exemplary Disclosures
"In this embodiment, as a combination of insulating film 10A and insulating film 10B, as mentioned above, insulating film 10A was made into the silicon oxide film, and insulating film 10B was made into the silicon nitride film. Besides it, for example, insulating film 10A is made into a silicon oxide film, and it is good also considering insulating film 10B as a silicon oxynitride (SiON) film. In order to form insulating film 10B which consists of a silicon oxynitride film, a silicon oxide film is formed on insulating film 10B, and it forms by annealing in NO and N2O atmosphere, for example." Saito825 ¶ [0108]. "As a combination of insulating film 10A and insulating film 10B, insulating film 10A is made into a silicon oxide film, and it is good also considering insulating film 10B as a SOG (liquid glass: spin on glass) film. Thus, by adopting a SOG film as insulating film 10B, SOG liquid enters easily in recess 50, and it can suppress that a seam etc. is formed." Saito825 ¶ [0109]. "As a combination of insulating film 10A and insulating film 10B, insulating film 10A is made into a silicon oxide film, and it is good also considering insulating film 10B as a plasma nitride (SiN) film. Form degradation of sidewall 70 can be suppressed by using a plasma nitride film as insulating film 10B. As insulating film 10A, a silicon oxide film is formed with the CVD method using TEOS (Tetraethoxysilane) gas etc., and it is good also considering insulating film 10B as a HDP (high density plasma: High Density Plasma) film." Saito825 ¶ [0110]. "Thus, all of insulating films 10A and 10B can distinguish between the etch rate of formed insulating films 10A and 10B with each manufacturing method. Insulating film 10A can be operated as a stopper at the time of etching insulating film 10B." Saito825 ¶ [0111]. "And when insulating film 10A formed on the upper surface of impurity diffusion region 2c1 and the upper surface of polysilicon wiring 3b is exposed, etching of insulating film 10B is stopped. Here, the thickness of insulating film 10B formed on recess 50 and sidewall 70 is formed more thickly than insulating film 10B formed on impurity diffusion region 2c1 and polysilicon wiring 3b. For this reason, when upper surface of polysilicon wiring 3b and upper surface of impurity diffusion region 2c1 is exposed, the inside of recess 50 will be in the state where insulating film 10B was filled up. It will be in the state where insulating film 10B remained also on sidewall 70." Saito825 ¶ [0112].

Exemplary Disclosures
"Thus, after etching into insulating film 10B, it etches into insulating film 10A, and upper surface of impurity diffusion region 2c1 and upper surface of polysilicon wiring 3b is exposed. Here, since the thickness of insulating film 10A is formed in about 20 nm filmy, the upper surface of impurity diffusion region 2c1 and the upper surface of polysilicon wiring 3b can be exposed by performing light etching to insulating film 10A. For this reason, it can suppress that an etching damage is given to the upper surface of impurity diffusion region 2c1, and the upper surface of polysilicon wiring 3b. Thus, in recesses 50 and 51, insulating film 10A formed along the internal surface of recesses 50 and 51 and insulating film 10B which is formed on the upper surface of this insulating film 10A, and fills up the inside of recesses 50 and 51 are formed." Saito825 ¶ [0113]. "In FIG. 7, by etching into insulating film 10A, lamination insulating film 10 which consists of insulating film 10A and insulating film 10B is formed over the upper surface of sidewall 70 from the boundary region of the upper surface and the side surface of active region 2c, and it fills up with it in recess 50. And the edges of lamination insulating film 10 are smoothly formed successively to the upper surface of exposed impurity diffusion region 2c1. The upper surface of lamination insulating film 10 is made into the smooth curving surface ranging from the upper surface side of impurity diffusion region 2c1 to the sidewall 70 side. Here, a part of front surface of impurity diffused layer 2c1 exposed in recess 50 and a part of front surface of active region 2c which are located under impurity diffused layer 2c1 touch either insulating film 10A or insulating film 10B at least." Saito825 ¶ [0114]. Additionally, under Plaintiff's apparent interpretation of the claim language, the claimed "first gate electrode" may include a silicide film. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 11-13, 18, 20, 22, 24-25, 26, 39. Although TSMC does not necessarily agree with such an interpretation, Saito825 further discloses this element under this interpretation, as shown below. For example, Saito825 discloses silicide film 40 formed on PMOS gate electrode 3c. *See, e.g.*, the following:



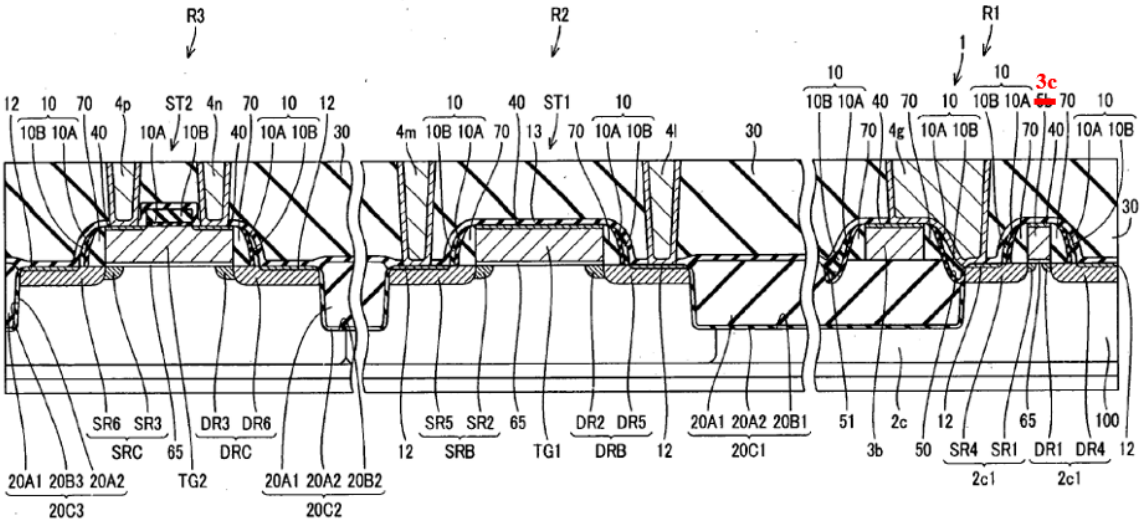
Saito825 FIG. 12 (corrected annotation).

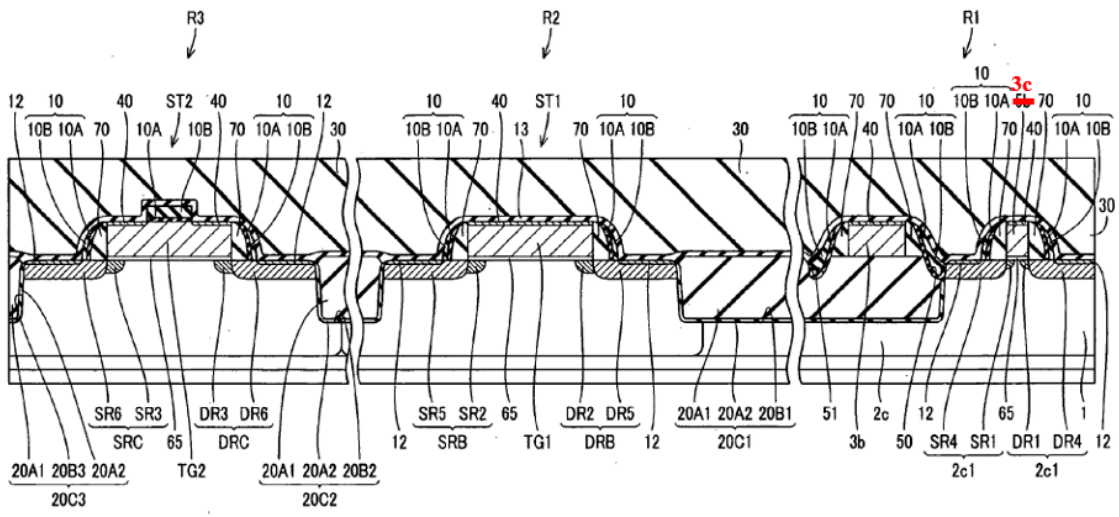


Saito825 FIG. 21 (corrected annotation).

"Also on the upper surface of polysilicon wiring 3b, silicide film 40 which consists of a cobalt silicide film etc. is formed. And interlayer insulation film 30 is formed so that sidewall 70, polysilicon wiring 3b, and lamination insulating film 10 may be covered. This interlayer insulation film 30 is provided with insulating film 13 which is formed on silicide films 12 and 40 and consists of a plasma nitride (SiN) etc., insulating film 14 which is formed on insulating film 13 and consists of a HDP (high density plasma: High Density Plasma) film etc., insulating film 15 which is formed on this insulating film 14 and consists of a silicon oxide film formed

Exemplary Disclosures
by the CVD method using TEOS (Tetraethoxysilane) gas etc., and insulating film 16 formed on this insulating film 15." Saito825 ¶ [0080]. "FIG. 8 and FIG. 20 are the cross-sectional views showing the ninth step of the manufacturing process of semiconductor device 200. Since it fills up with lamination insulating film 10 in recess 50, it can suppress that the internal surface of recess 50 is exposed. And metallic films, such as cobalt (Co), are deposited, about 10 nm, on the main front surface of semiconductor substrate 100 by the sputtering method." Saito825 ¶ [0116]. "Then, heat treatment about more than 400° C. and below 600° C. is performed, silicon and cobalt react (silicidation), and silicide films 12 and 40 are formed. And wet etching removes unreacted cobalt. After an appropriate time, it heat-treats in the range of more than 700° C. and less than 800° C. Thus, silicide film 12 is formed on the front surface of impurity diffused layer 2c1, 2c1, SRB, DRB, SRC, and DRC. Silicide film 40 is formed on the upper surface of polysilicon wiring 5b [sic 3c] and 3b and gate wiring TG1. Since insulating films 10A and 10B remain on the upper surface of gate wiring TG2, silicide film 40 is formed on the upper surface of gate wiring TG2 which adjoins insulating films 10A and 10B." Saito825 ¶ [0117]. "Thus, when forming silicide films 12 and 40, the front surface of impurity diffused layer 2c1 exposed in recess 50 and the front surface of active region 2 located under impurity diffused layer 2c1 touch lamination insulating film 10 which consists of insulating film 10A and insulating film 10B. For this reason, it is suppressed that a silicide film is formed in the front surface of impurity diffused layer 2c1 located in recess 50 and the front surface of active region 2c located under impurity diffused layer 2c1." Saito825 ¶ [0118]. "In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g." Saito825 ¶ [0124]. *See also, e.g.*, Saito825 ¶ [0024], ¶ [0026], ¶ [0055], ¶¶ [0077]-[0084], ¶ [0104], ¶ [0107], ¶¶ [0116]-[0120], ¶¶ [0122]-[0124], FIGS. 3, 8-12, 20-21.

Exemplary Disclosures
To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
1[l] the first stress-relief film is not in direct contact with the side surface of the first gate electrode.
Saito825 discloses this feature. For example, Saito825 discloses insulating film 10A is not in direct contact with a side surface of PMOS gate electrode 3c (corrected from 5b). *See, e.g.*, the following: FIG.12      Saito825 FIG. 12 (corrected annotation).



Saito825 FIG. 21 (corrected annotation).

"Even if it is the semiconductor device provided with the wiring on an isolation insulating film, the sidewall formed on the side surface of this wiring, and the shared contact which connects the wiring and the impurity diffusion on an active region, the semiconductor device which can suppress the generation of the leakage current from shared contact to a semiconductor substrate, and its manufacturing method are offered. The semiconductor device concerning the present invention is provided with an isolation insulating film selectively formed on the main front surface of a semiconductor substrate, an active region specified by an isolation insulating film on the main front surface of a semiconductor substrate, a recess which reaches an active region on the isolation insulating film, the first insulating film formed so that a recess might be covered, the second insulating film which is formed on a first insulating film, is filled up with a recess, and differs in a material from the first insulating film, an impurity diffused layer formed on the main front surface of the active region of the position which adjoins the recess, and an electric conduction film formed on the impurity diffused layer."

Saito825 Abstract.

"Recess 50 which reaches active region 2c from sidewall 70 is formed in isolation insulating film 20A1. For this reason, the internal surface of recess 50 includes a part of front surface of impurity diffused layer 2c1, a part of front surface of active region 2c located under impurity diffused layer 2c1, and a part of front surface of isolation insulating film 20A1. And insulating film 10A which consists of a silicon oxide film etc. is formed so that the front surface of this recess 50 may be covered. The thickness of insulating film 10A of the vertical direction to the main front surface of semiconductor substrate 100 is about 20 nm in the parallel portion to the main front surface of semiconductor substrate 100. This insulating film 10A is formed on the side surface of sidewall 70 while it covers the internal surface of recess 50. On this insulating

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film 10A, insulating film 10B from which material differs in insulating film 10A, for example, the insulating film which consists of a silicon nitride film etc., is formed." Saito825 ¶ [0074]. "It fills up with this insulating film 10B in recess 50, and fills up with insulating film 10B to opening edge 50a of recess 50. And insulating film 10B is extending and existing even on the side surface of sidewall 70 via insulating film 10A. The thickness of this insulating film 10B of the vertical direction to the main front surface of semiconductor substrate 100 is formed more thickly than the thickness of insulating film 10A, for example, is about 80 nm. This insulating film 10B is an insulating film which consists of different material from insulating film 10A, for example, consists of a silicon nitride film etc. The insulating film which differs in material from insulating film 10A in this specification means that, when etching insulating film 10A, the etch rate difference of insulating film 10A including a silicon oxide film and insulating film 10B is larger than the etch rate difference of semiconductor substrate 100 of a P type, and a silicon oxide film. Preferably, insulating film 10B is formed with material including a silicon nitride film (Si3N4)." Saito825 ¶ [0075]. "Thus, the inside of recess 50 is embedded by lamination insulating film 10 which consists of a plurality of insulating films 10A and 10B with a big difference of an etch rate. The outer edge section at the side of active region 2c of lamination insulating film 10 is located near the opening edge 50a of recess 50, and it is formed so that the upper surface of active region 2c may hardly be covered. Here, at least one side of insulating films 10A and 10B is formed so that the front surface of impurity diffused layer 2c1 may be contacted among the internal surfaces of recess 50. For this reason, the front surface of impurity diffused layer 2c1 located in recess 50 is covered with lamination insulating film 10. In particular, in Embodiment 1, among the internal surfaces of recess 50, at least, insulating film 10A is crossed to opening edge 50 a from the bottom of recess 50, and it is formed so that the internal surface of recess 50 may be contacted. For this reason, among the internal surfaces of recess 50, the front surface of impurity diffused layer 2c1, and active region 2c located under impurity diffused layer 2c1 contacts insulating film 10A, and is covered with insulating film 10A." Saito825 ¶ [0076]. "FIG. 6 and FIG. 18 are the cross-sectional views showing the seventh step of the manufacturing process of semiconductor device 200. As shown in this FIG. 6 and FIG. 18, it is a region including recess 50 and insulating film 10A which consists of a silicon oxide film etc. is formed as a silicide protection film on the main front surface of semiconductor substrate 100, for example. For example, about 20 nm-30 nm of insulating films 10A are deposited by the CVD method (Chemical Vapor Deposition) method using TEOS (Tetraethoxysilane) gas. Since the

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depth of recess 50 is set to about 60 nm in many cases, for example, insulating film 10A is formed so that it may go along on the front surface of recess 50." Saito825 ¶ [0104]. "And after forming insulating film 10A, about 80 nm-100 nm of insulating films 10B which consist of a silicon nitride film etc. are formed with a CVD method etc. on insulating film 10A, for example. Thus, insulating film 10B is deposited so that the thickness of deposited insulating film 10B may become thick rather than the depth of recess 50." Saito825 ¶ [0105]. "FIG. 7 and FIG. 19 are the cross-sectional views showing the eighth step of the manufacturing process of semiconductor device 200. In this FIG. 7 and FIG. 19, it patterns to a silicide protection film first. It etches into insulating film 10B by using insulating film 10A as a stopper. Here, insulating film 10A consists of a silicon oxide film etc., and insulating film 10B consists of a silicon nitride film etc. For this reason, when etching insulating film 10B, the large selection ratio of etching is taken so that the side of a silicon nitride film may become easier to etch than a silicon oxide film. For this reason, insulating film 10A can be operated good as a stopper. When etching into insulating film 10B, it can suppress etching to the main front surface of semiconductor substrate 100." Saito825 ¶ [0107]. "In this embodiment, as a combination of insulating film 10A and insulating film 10B, as mentioned above, insulating film 10A was made into the silicon oxide film, and insulating film 10B was made into the silicon nitride film. Besides it, for example, insulating film 10A is made into a silicon oxide film, and it is good also considering insulating film 10B as a silicon oxynitride (SiON) film. In order to form insulating film 10B which consists of a silicon oxynitride film, a silicon oxide film is formed on insulating film 10B, and it forms by annealing in NO and N2O atmosphere, for example." Saito825 ¶ [0108]. "As a combination of insulating film 10A and insulating film 10B, insulating film 10A is made into a silicon oxide film, and it is good also considering insulating film 10B as a SOG (liquid glass: spin on glass) film. Thus, by adopting a SOG film as insulating film 10B, SOG liquid enters easily in recess 50, and it can suppress that a seam etc. is formed." Saito825 ¶ [0109].

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"As a combination of insulating film 10A and insulating film 10B, insulating film 10A is made into a silicon oxide film, and it is good also considering insulating film 10B as a plasma nitride (SiN) film. Form degradation of sidewall 70 can be suppressed by using a plasma nitride film as insulating film 10B. As insulating film 10A, a silicon oxide film is formed with the CVD method using TEOS (Tetraethoxysilane) gas etc., and it is good also considering insulating film 10B as a HDP (high density plasma: High Density Plasma) film." Saito825 ¶ [0110]. "Thus, all of insulating films 10A and 10B can distinguish between the etch rate of formed insulating films 10A and 10B with each manufacturing method. Insulating film 10A can be operated as a stopper at the time of etching insulating film 10B." Saito825 ¶ [0111]. "And when insulating film 10A formed on the upper surface of impurity diffusion region 2c1 and the upper surface of polysilicon wiring 3b is exposed, etching of insulating film 10B is stopped. Here, the thickness of insulating film 10B formed on recess 50 and sidewall 70 is formed more thickly than insulating film 10B formed on impurity diffusion region 2c1 and polysilicon wiring 3b. For this reason, when upper surface of polysilicon wiring 3b and upper surface of impurity diffusion region 2c1 is exposed, the inside of recess 50 will be in the state where insulating film 10B was filled up. It will be in the state where insulating film 10B remained also on sidewall 70." Saito825 ¶ [0112]. "Thus, after etching into insulating film 10B, it etches into insulating film 10A, and upper surface of impurity diffusion region 2c1 and upper surface of polysilicon wiring 3b is exposed. Here, since the thickness of insulating film 10A is formed in about 20 nm filmy, the upper surface of impurity diffusion region 2c1 and the upper surface of polysilicon wiring 3b can be exposed by performing light etching to insulating film 10A. For this reason, it can suppress that an etching damage is given to the upper surface of impurity diffusion region 2c1, and the upper surface of polysilicon wiring 3b. Thus, in recesses 50 and 51, insulating film 10A formed along the internal surface of recesses 50 and 51 and insulating film 10B which is formed on the upper surface of this insulating film 10A, and fills up the inside of recesses 50 and 51 are formed." Saito825 ¶ [0113]. "In FIG. 7, by etching into insulating film 10A, lamination insulating film 10 which consists of insulating film 10A and insulating film 10B is formed over the upper surface of sidewall 70 from the boundary region of the upper surface and the side surface of active region 2c, and it fills up with it in recess 50. And the edges of lamination insulating film 10 are smoothly formed successively to the upper surface of exposed impurity diffusion region 2c1. The upper surface of lamination insulating film 10 is made into the smooth curving surface ranging from the upper surface side of impurity diffusion region 2c1 to the sidewall 70 side. Here, a part of front surface

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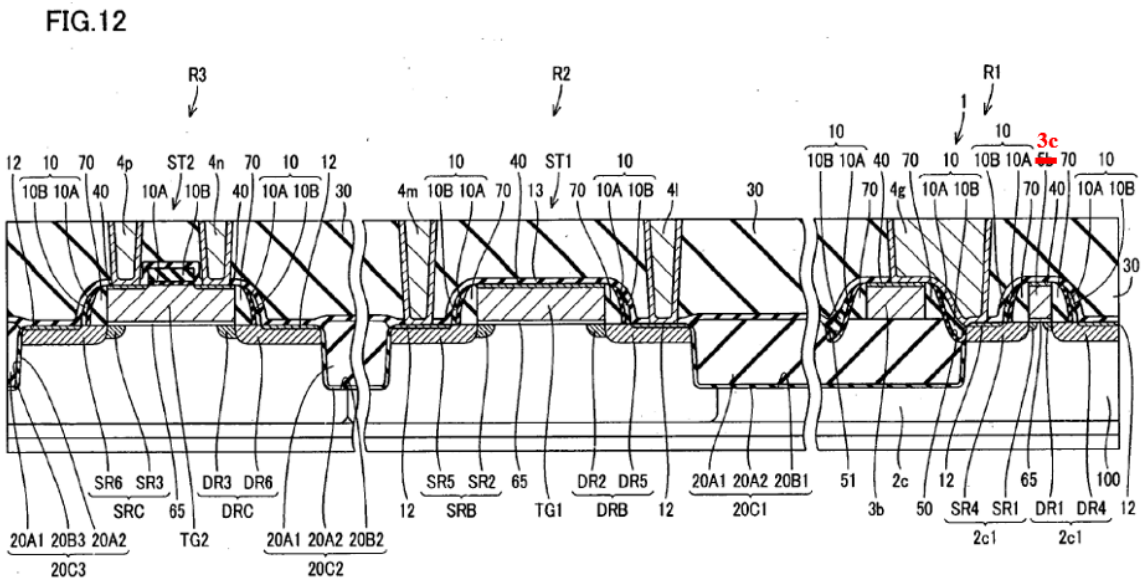
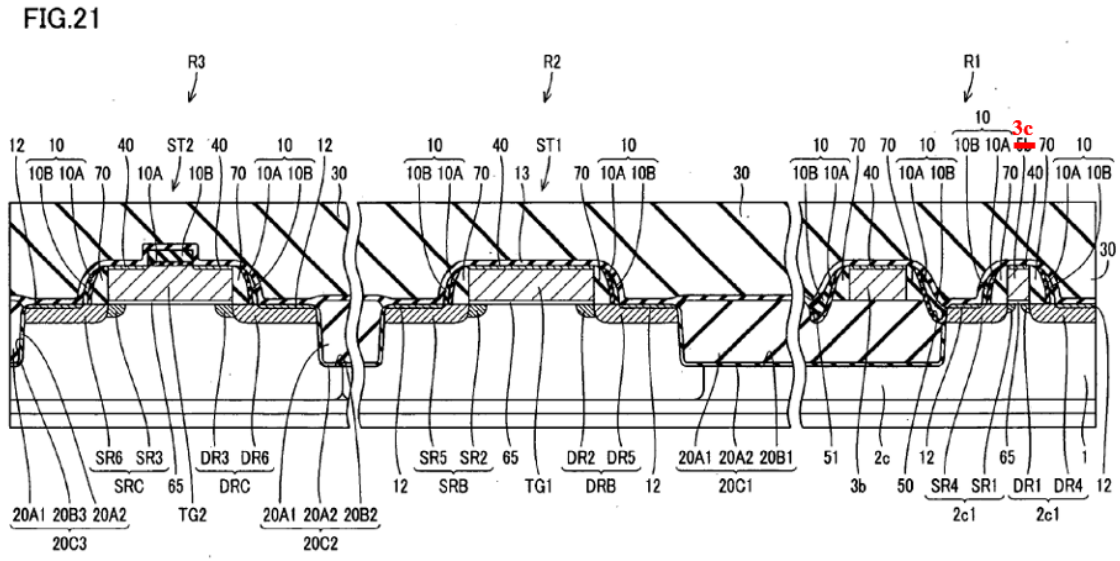
of impurity diffused layer 2c1 exposed in recess 50 and a part of front surface of active region 2c which are located under impurity diffused layer 2c1 touch either insulating film 10A or insulating film 10B at least." Saito825 ¶ [0114]. Additionally, under Plaintiff's apparent interpretation of the claim language, the claimed "first gate electrode" may include a silicide film. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 11-13, 18, 20, 22, 24-25, 26, 39. Although TSMC does not necessarily agree with such an interpretation, Saito825 further discloses this element under this interpretation, as shown below. For example, Saito825 discloses silicide film 40 formed on PMOS gate electrode 3c, which is not in direct contact with insulating film 10A. *See, e.g.*, the following:    Saito825 FIG. 12 (corrected annotation).



Saito825 FIG. 21 (corrected annotation).

"Also on the upper surface of polysilicon wiring 3b, silicide film 40 which consists of a cobalt silicide film etc. is formed. And interlayer insulation film 30 is formed so that sidewall 70, polysilicon wiring 3b, and lamination insulating film 10 may be covered. This interlayer insulation film 30 is provided with insulating film 13 which is formed on silicide films 12 and 40 and consists of a plasma nitride (SiN) etc., insulating film 14 which is formed on insulating film 13 and consists of a HDP (high density plasma: High Density Plasma) film etc., insulating film 15 which is formed on this insulating film 14 and consists of a silicon oxide film formed by the CVD method using TEOS (Tetraethoxysilane) gas etc., and insulating film 16 formed on this insulating film 15."

Saito825 ¶ [0080].

"FIG. 8 and FIG. 20 are the cross-sectional views showing the ninth step of the manufacturing process of semiconductor device 200. Since it fills up with lamination insulating film 10 in recess 50, it can suppress that the internal surface of recess 50 is exposed. And metallic films, such as cobalt (Co), are deposited, about 10 nm, on the main front surface of semiconductor substrate 100 by the sputtering method."

Saito825 ¶ [0116].

"Then, heat treatment about more than 400° C. and below 600° C. is performed, silicon and cobalt react (silicidation), and silicide films 12 and 40 are formed. And wet etching removes unreacted cobalt. After an appropriate time, it heat-treats in the range of more than 700° C. and less than 800° C. Thus, silicide film 12 is formed on the front surface of impurity diffused layer 2c1, 2c1, SRB, DRB, SRC, and DRC. Silicide film 40 is formed on the upper surface of polysilicon wiring 5b [sic 3c] and 3b and gate wiring TG1. Since insulating films 10A and 10B

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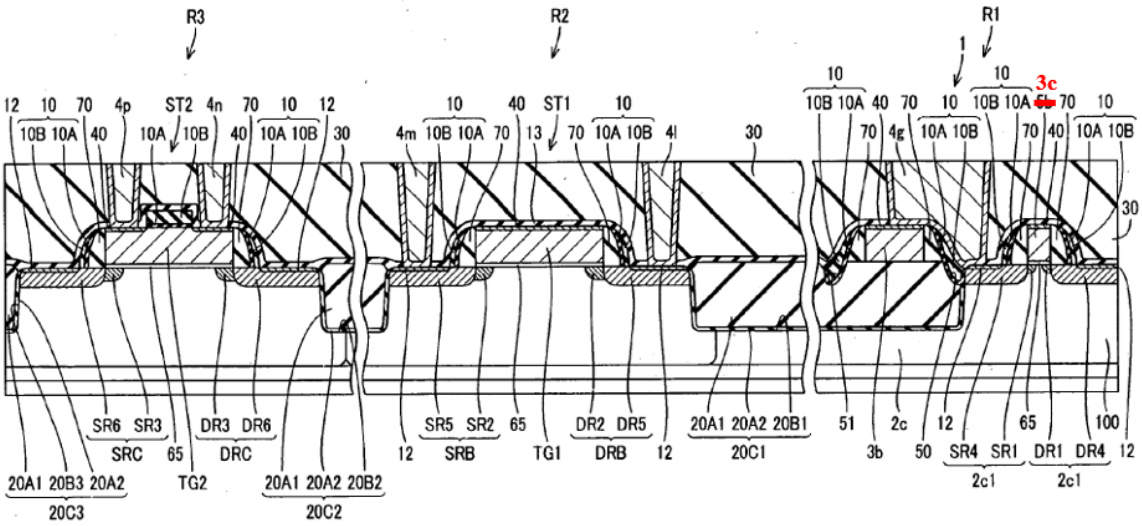
remain on the upper surface of gate wiring TG2, silicide film 40 is formed on the upper surface of gate wiring TG2 which adjoins insulating films 10A and 10B." Saito825 ¶ [0117]. "Thus, when forming silicide films 12 and 40, the front surface of impurity diffused layer 2c1 exposed in recess 50 and the front surface of active region 2 located under impurity diffused layer 2c1 touch lamination insulating film 10 which consists of insulating film 10A and insulating film 10B. For this reason, it is suppressed that a silicide film is formed in the front surface of impurity diffused layer 2c1 located in recess 50 and the front surface of active region 2c located under impurity diffused layer 2c1." Saito825 ¶ [0118]. "In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g." Saito825 ¶ [0124]. *See also, e.g.*, Saito825 ¶ [0024], ¶ [0026], ¶ [0055], ¶¶ [0077]-[0084], ¶ [0104], ¶ [0107], ¶¶ [0116]-[0120], ¶¶ [0122]-[0124], FIGS. 3, 8-12, 20-21. To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

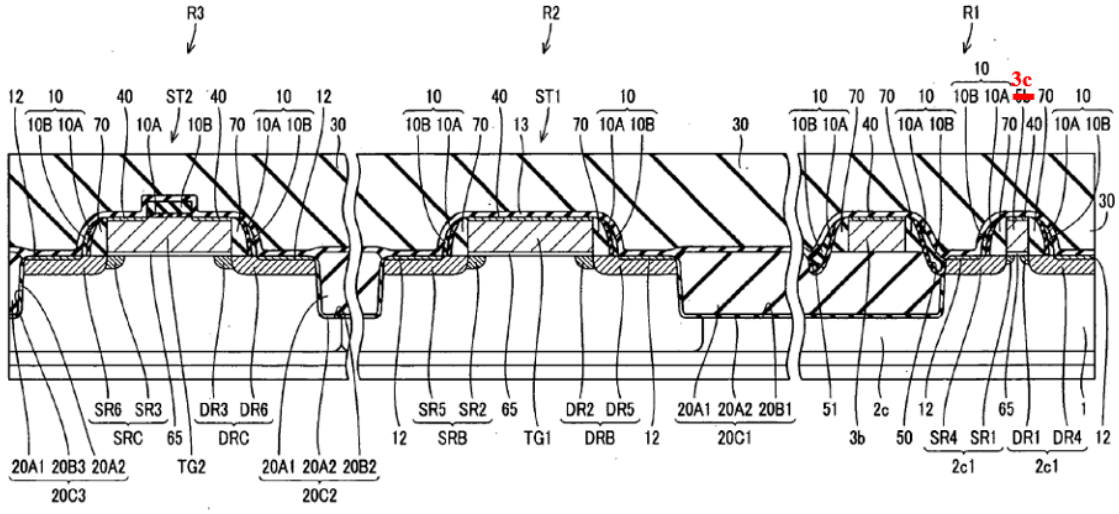
Exemplary Disclosures
3[a] The semiconductor device of claim 1, further comprising: a first silicide layer formed on the first gate electrode; and
Saito825 discloses this feature. For example, Saito825 discloses silicide layer 40 formed on PMOS gate electrode 3c (corrected from 5b). *See, e.g.*, the following:

FIG.12



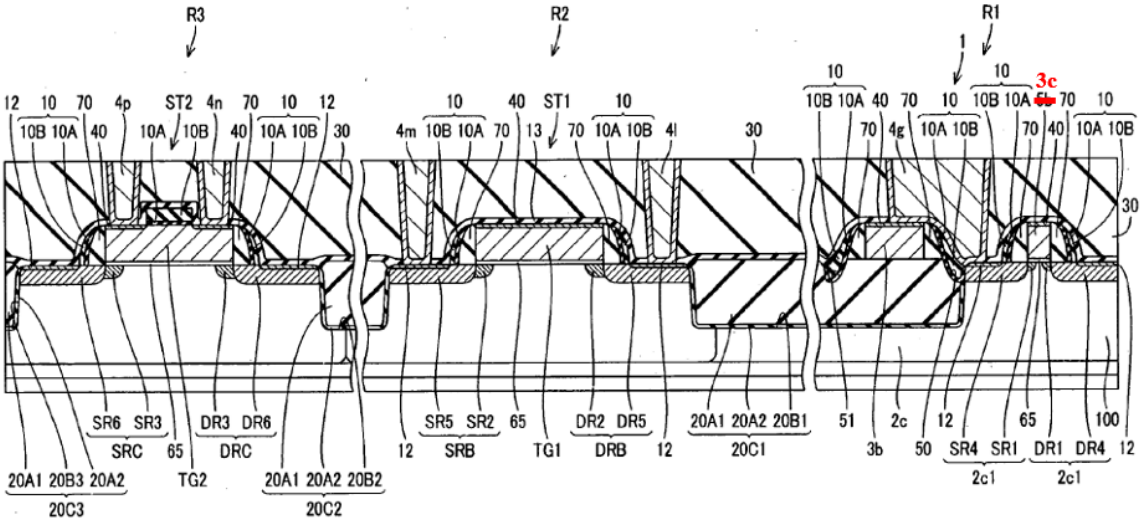
Saito825 FIG. 12 (corrected annotation).

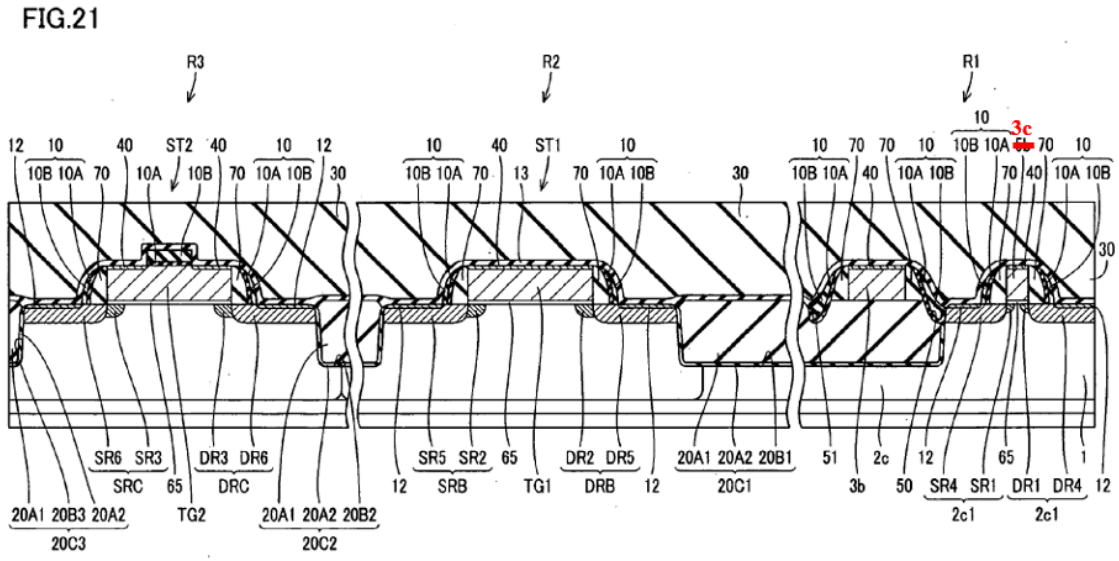
FIG.21



Saito825 FIG. 21 (corrected annotation).

Exemplary Disclosures
"Also on the upper surface of polysilicon wiring 3b, silicide film 40 which consists of a cobalt silicide film etc. is formed. And interlayer insulation film 30 is formed so that sidewall 70, polysilicon wiring 3b, and lamination insulating film 10 may be covered. This interlayer insulation film 30 is provided with insulating film 13 which is formed on silicide films 12 and 40 and consists of a plasma nitride (SiN) etc., insulating film 14 which is formed on insulating film 13 and consists of a HDP (high density plasma: High Density Plasma) film etc., insulating film 15 which is formed on this insulating film 14 and consists of a silicon oxide film formed by the CVD method using TEOS (Tetraethoxysilane) gas etc., and insulating film 16 formed on this insulating film 15." Saito825 ¶ [0080]. "FIG. 8 and FIG. 20 are the cross-sectional views showing the ninth step of the manufacturing process of semiconductor device 200. Since it fills up with lamination insulating film 10 in recess 50, it can suppress that the internal surface of recess 50 is exposed. And metallic films, such as cobalt (Co), are deposited, about 10 nm, on the main front surface of semiconductor substrate 100 by the sputtering method." Saito825 ¶ [0116]. "Then, heat treatment about more than 400° C. and below 600° C. is performed, silicon and cobalt react (silicidation), and silicide films 12 and 40 are formed. And wet etching removes unreacted cobalt. After an appropriate time, it heat-treats in the range of more than 700° C. and less than 800° C. Thus, silicide film 12 is formed on the front surface of impurity diffused layer 2c1, 2c1, SRB, DRB, SRC, and DRC. Silicide film 40 is formed on the upper surface of polysilicon wiring 5b [sic 3c] and 3b and gate wiring TG1. Since insulating films 10A and 10B remain on the upper surface of gate wiring TG2, silicide film 40 is formed on the upper surface of gate wiring TG2 which adjoins insulating films 10A and 10B." Saito825 ¶ [0117]. "Thus, when forming silicide films 12 and 40, the front surface of impurity diffused layer 2c1 exposed in recess 50 and the front surface of active region 2 located under impurity diffused layer 2c1 touch lamination insulating film 10 which consists of insulating film 10A and insulating film 10B. For this reason, it is suppressed that a silicide film is formed in the front surface of impurity diffused layer 2c1 located in recess 50 and the front surface of active region 2c located under impurity diffused layer 2c1." Saito825 ¶ [0118]. "In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g." Saito825 ¶ [0124].

Exemplary Disclosures
See also, e.g., Saito825 ¶ [0024], ¶ [0026], ¶ [0055], ¶¶ [0077]-[0084], ¶ [0104], ¶ [0107], ¶¶ [0116]-[0120], ¶¶ [0122]-[0124], FIGS. 3, 8-12, 20-21. Under AICP's understanding of 1[c]—whereby the gate silicide can be part of the gate electrode itself—the silicide cannot be "formed on" the gate electrode, as claimed. If such an illogical interpretation is permitted, however, this reference would additionally satisfy 3[a] under the alternative mapping of 1[c]. To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
3[b] a second silicide layer formed on the first source/drain region which includes the silicon compound layer.
Saito825 discloses this feature. For example, Saito825 discloses silicide layers 12 formed on PMOS source/drain regions SR4, DR4. *See, e.g.*, the following: FIG.12    Saito825 FIG. 12 (corrected annotation).



Saito825 FIG. 21 (corrected annotation).

"Here, at least one side of insulating films 10A and 10B has covered the front surface of impurity diffused layer 2c1 located in recess 50. It is suppressed that silicide film 12 is formed in impurity diffused layer 2c1 and the front surface of active region 2c among the internal surfaces of recess 50."

Saito825 ¶ [0078].

"Thus, since it is suppressed that silicide film 12 contacts the front surface of active region 2c located in recess 50, it is suppressed that leakage current arises from silicide film 12 to semiconductor substrate 100. Thus, since it is suppressed that the leakage current from silicide film 12 to semiconductor substrate 100 occurs, reduction of consumed electric power can be aimed at and suppression of a generation of malfunction can be aimed at further."

Saito825 ¶ [0079].

"FIG. 8 and FIG. 20 are the cross-sectional views showing the ninth step of the manufacturing process of semiconductor device 200. Since it fills up with lamination insulating film 10 in recess 50, it can suppress that the internal surface of recess 50 is exposed. And metallic films, such as cobalt (Co), are deposited, about 10 nm, on the main front surface of semiconductor substrate 100 by the sputtering method."

Saito825 ¶ [0116].

"Then, heat treatment about more than 400° C. and below 600° C. is performed, silicon and cobalt react (silicidation), and silicide films 12 and 40 are formed. And wet etching removes unreacted cobalt. After an appropriate time, it heat-treats in the range of more than 700° C. and less than 800° C. Thus, silicide film 12 is formed on the front surface of impurity diffused layer 2c1, 2c1, SRB, DRB, SRC, and DRC. Silicide film 40 is formed on the upper surface of

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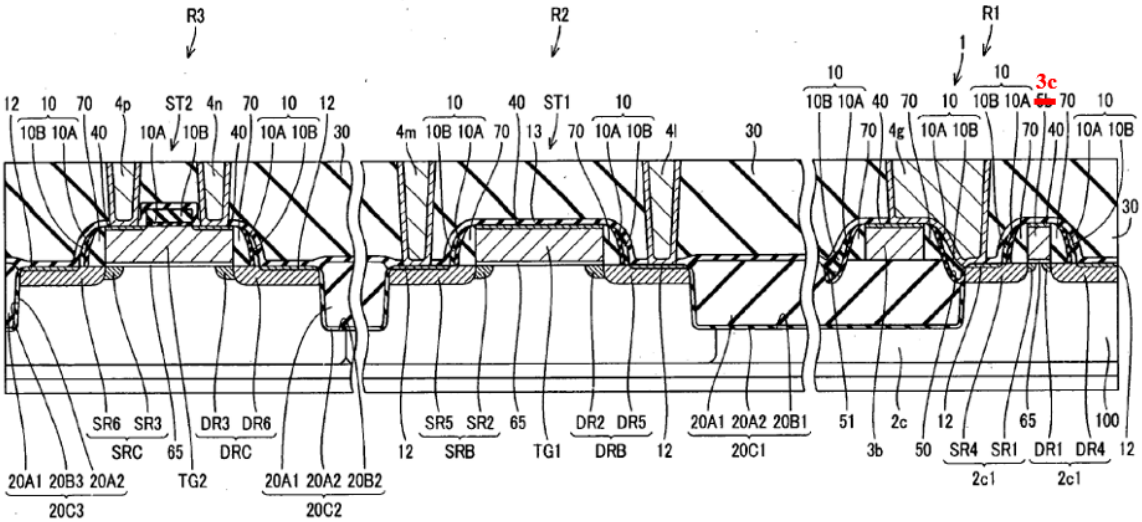
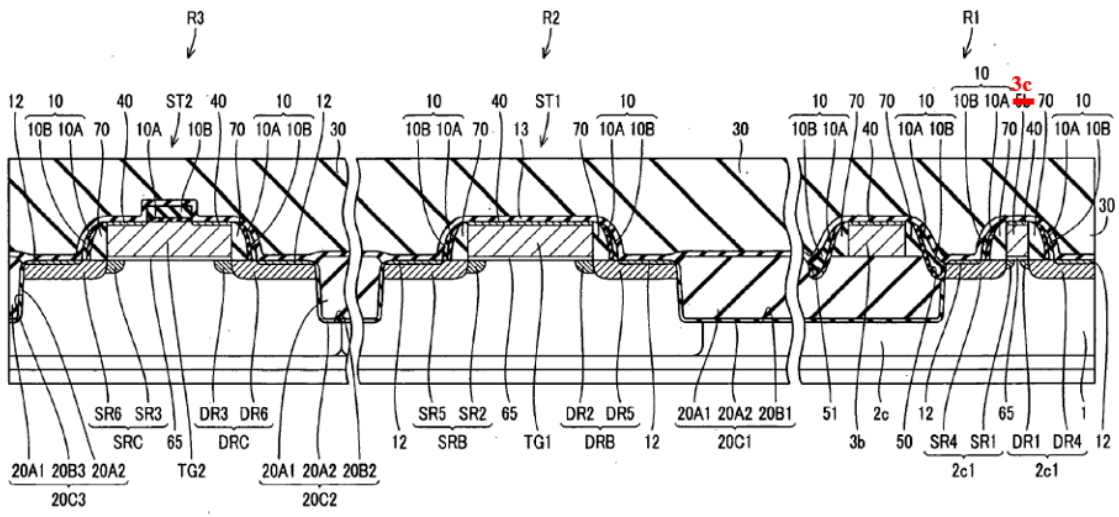
polysilicon wiring 5b [sic 3c] and 3b and gate wiring TG1. Since insulating films 10A and 10B remain on the upper surface of gate wiring TG2, silicide film 40 is formed on the upper surface of gate wiring TG2 which adjoins insulating films 10A and 10B." Saito825 ¶ [0117]. "Thus, when forming silicide films 12 and 40, the front surface of impurity diffused layer 2c1 exposed in recess 50 and the front surface of active region 2 located under impurity diffused layer 2c1 touch lamination insulating film 10 which consists of insulating film 10A and insulating film 10B. For this reason, it is suppressed that a silicide film is formed in the front surface of impurity diffused layer 2c1 located in recess 50 and the front surface of active region 2c located under impurity diffused layer 2c1." Saito825 ¶ [0118]. "That is, it is suppressed that silicide film 12 formed on the upper surface of impurity diffused layer 2c1 reaches even the front surface of active region 2c which is located under impurity diffused layer 2c1 extending and existing even over the internal surface of recess 50. For this reason, it can suppress that silicide film 12 formed and semiconductor substrate 100 are electrically connected." Saito825 ¶ [0119]. "In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g." Saito825 ¶ [0124]. *See also, e.g.*, Saito825 ¶ [0024], ¶ [0026], ¶ [0055], ¶¶ [0077]-[0084], ¶ [0104], ¶¶ [0107]-[0112], ¶¶ [0116]-[0120], ¶¶ [0122]-[0124], FIGS. 3, 8-12, 20-21. Under AICP's understanding of 1[f]—whereby the source/drain silicide can be part of the silicon compound layer, which is itself part of the source/drain region—the silicide cannot be "formed on" the source/drain region, as claimed. If such an illogical interpretation is permitted, however, this reference would additionally satisfy 3[b] under the alternative mapping of 1[f]. To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

Exemplary Disclosures
4[a] The semiconductor device of claim 1, wherein the first stress-relief film is formed on a side surface of the silicon compound layer.
Under Plaintiff's apparent interpretation of the claim language, the claimed "silicon compound layer" may include a silicide film. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 15, 20, 21, 25, 26, 31. Under Plaintiff's apparent interpretation of the claim language, the claimed "side surface of the silicon compound layer" may include an upper surface. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 25, 26. Although TSMC disagrees with such interpretations, Saito825 discloses 4[a] under these interpretations, as shown below. For example, Saito825 discloses the insulating film 10A is formed on a side surface of silicide layers 12 on PMOS source/drain regions SR4, DR4 (under Plaintiff's apparent interpretation). *See, e.g.*, the following: FIG.12    Saito825 FIG. 12 (corrected annotation).



Saito825 FIG. 21 (corrected annotation).

"Even if it is the semiconductor device provided with the wiring on an isolation insulating film, the sidewall formed on the side surface of this wiring, and the shared contact which connects the wiring and the impurity diffusion on an active region, the semiconductor device which can suppress the generation of the leakage current from shared contact to a semiconductor substrate, and its manufacturing method are offered. The semiconductor device concerning the present invention is provided with an isolation insulating film selectively formed on the main front surface of a semiconductor substrate, an active region specified by an isolation insulating film on the main front surface of a semiconductor substrate, a recess which reaches an active region on the isolation insulating film, the first insulating film formed so that a recess might be covered, the second insulating film which is formed on a first insulating film, is filled up with a recess, and differs in a material from the first insulating film, an impurity diffused layer formed on the main front surface of the active region of the position which adjoins the recess, and an electric conduction film formed on the impurity diffused layer."

Saito825 Abstract.

"Recess 50 which reaches active region 2c from sidewall 70 is formed in isolation insulating film 20A1. For this reason, the internal surface of recess 50 includes a part of front surface of impurity diffused layer 2c1, a part of front surface of active region 2c located under impurity diffused layer 2c1, and a part of front surface of isolation insulating film 20A1. And insulating film 10A which consists of a silicon oxide film etc. is formed so that the front surface of this recess 50 may be covered. The thickness of insulating film 10A of the vertical direction to the main front surface of semiconductor substrate 100 is about 20 nm in the parallel portion to the main front surface of semiconductor substrate 100. This insulating film 10A is formed on the side surface of sidewall 70 while it covers the internal surface of recess 50. On this insulating

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film 10A, insulating film 10B from which material differs in insulating film 10A, for example, the insulating film which consists of a silicon nitride film etc., is formed." Saito825 ¶ [0074]. "It fills up with this insulating film 10B in recess 50, and fills up with insulating film 10B to opening edge 50a of recess 50. And insulating film 10B is extending and existing even on the side surface of sidewall 70 via insulating film 10A. The thickness of this insulating film 10B of the vertical direction to the main front surface of semiconductor substrate 100 is formed more thickly than the thickness of insulating film 10A, for example, is about 80 nm. This insulating film 10B is an insulating film which consists of different material from insulating film 10A, for example, consists of a silicon nitride film etc. The insulating film which differs in material from insulating film 10A in this specification means that, when etching insulating film 10A, the etch rate difference of insulating film 10A including a silicon oxide film and insulating film 10B is larger than the etch rate difference of semiconductor substrate 100 of a P type, and a silicon oxide film. Preferably, insulating film 10B is formed with material including a silicon nitride film (Si3N4)." Saito825 ¶ [0075]. "Thus, the inside of recess 50 is embedded by lamination insulating film 10 which consists of a plurality of insulating films 10A and 10B with a big difference of an etch rate. The outer edge section at the side of active region 2c of lamination insulating film 10 is located near the opening edge 50a of recess 50, and it is formed so that the upper surface of active region 2c may hardly be covered. Here, at least one side of insulating films 10A and 10B is formed so that the front surface of impurity diffused layer 2c1 may be contacted among the internal surfaces of recess 50. For this reason, the front surface of impurity diffused layer 2c1 located in recess 50 is covered with lamination insulating film 10. In particular, in Embodiment 1, among the internal surfaces of recess 50, at least, insulating film 10A is crossed to opening edge 50 a from the bottom of recess 50, and it is formed so that the internal surface of recess 50 may be contacted. For this reason, among the internal surfaces of recess 50, the front surface of impurity diffused layer 2c1, and active region 2c located under impurity diffused layer 2c1 contacts insulating film 10A, and is covered with insulating film 10A." Saito825 ¶ [0076]. "FIG. 6 and FIG. 18 are the cross-sectional views showing the seventh step of the manufacturing process of semiconductor device 200. As shown in this FIG. 6 and FIG. 18, it is a region including recess 50 and insulating film 10A which consists of a silicon oxide film etc. is formed as a silicide protection film on the main front surface of semiconductor substrate 100, for example. For example, about 20 nm-30 nm of insulating films 10A are deposited by the CVD method (Chemical Vapor Deposition) method using TEOS (Tetraethoxysilane) gas. Since the

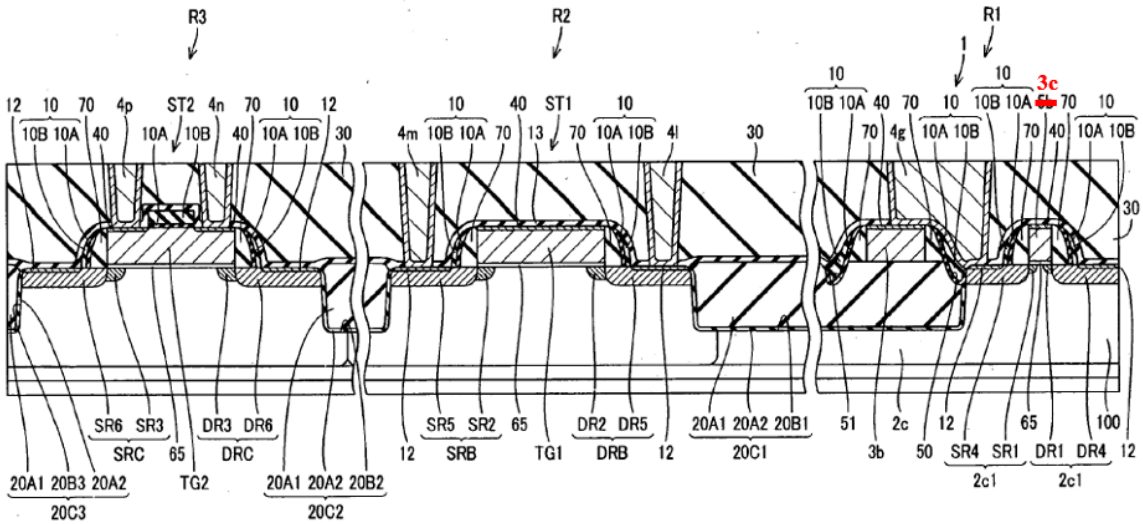
Exemplary Disclosures
depth of recess 50 is set to about 60 nm in many cases, for example, insulating film 10A is formed so that it may go along on the front surface of recess 50." Saito825 ¶ [0104]. "And after forming insulating film 10A, about 80 nm-100 nm of insulating films 10B which consist of a silicon nitride film etc. are formed with a CVD method etc. on insulating film 10A, for example. Thus, insulating film 10B is deposited so that the thickness of deposited insulating film 10B may become thick rather than the depth of recess 50." Saito825 ¶ [0105]. "FIG. 7 and FIG. 19 are the cross-sectional views showing the eighth step of the manufacturing process of semiconductor device 200. In this FIG. 7 and FIG. 19, it patterns to a silicide protection film first. It etches into insulating film 10B by using insulating film 10A as a stopper. Here, insulating film 10A consists of a silicon oxide film etc., and insulating film 10B consists of a silicon nitride film etc. For this reason, when etching insulating film 10B, the large selection ratio of etching is taken so that the side of a silicon nitride film may become easier to etch than a silicon oxide film. For this reason, insulating film 10A can be operated good as a stopper. When etching into insulating film 10B, it can suppress etching to the main front surface of semiconductor substrate 100." Saito825 ¶ [0107]. "In this embodiment, as a combination of insulating film 10A and insulating film 10B, as mentioned above, insulating film 10A was made into the silicon oxide film, and insulating film 10B was made into the silicon nitride film. Besides it, for example, insulating film 10A is made into a silicon oxide film, and it is good also considering insulating film 10B as a silicon oxynitride (SiON) film. In order to form insulating film 10B which consists of a silicon oxynitride film, a silicon oxide film is formed on insulating film 10B, and it forms by annealing in NO and N2O atmosphere, for example." Saito825 ¶ [0108]. "As a combination of insulating film 10A and insulating film 10B, insulating film 10A is made into a silicon oxide film, and it is good also considering insulating film 10B as a SOG (liquid glass: spin on glass) film. Thus, by adopting a SOG film as insulating film 10B, SOG liquid enters easily in recess 50, and it can suppress that a seam etc. is formed." Saito825 ¶ [0109].

Exemplary Disclosures
"As a combination of insulating film 10A and insulating film 10B, insulating film 10A is made into a silicon oxide film, and it is good also considering insulating film 10B as a plasma nitride (SiN) film. Form degradation of sidewall 70 can be suppressed by using a plasma nitride film as insulating film 10B. As insulating film 10A, a silicon oxide film is formed with the CVD method using TEOS (Tetraethoxysilane) gas etc., and it is good also considering insulating film 10B as a HDP (high density plasma: High Density Plasma) film." Saito825 ¶ [0110]. "Thus, all of insulating films 10A and 10B can distinguish between the etch rate of formed insulating films 10A and 10B with each manufacturing method. Insulating film 10A can be operated as a stopper at the time of etching insulating film 10B." Saito825 ¶ [0111]. "And when insulating film 10A formed on the upper surface of impurity diffusion region 2c1 and the upper surface of polysilicon wiring 3b is exposed, etching of insulating film 10B is stopped. Here, the thickness of insulating film 10B formed on recess 50 and sidewall 70 is formed more thickly than insulating film 10B formed on impurity diffusion region 2c1 and polysilicon wiring 3b. For this reason, when upper surface of polysilicon wiring 3b and upper surface of impurity diffusion region 2c1 is exposed, the inside of recess 50 will be in the state where insulating film 10B was filled up. It will be in the state where insulating film 10B remained also on sidewall 70." Saito825 ¶ [0112]. "Thus, after etching into insulating film 10B, it etches into insulating film 10A, and upper surface of impurity diffusion region 2c1 and upper surface of polysilicon wiring 3b is exposed. Here, since the thickness of insulating film 10A is formed in about 20 nm filmy, the upper surface of impurity diffusion region 2c1 and the upper surface of polysilicon wiring 3b can be exposed by performing light etching to insulating film 10A. For this reason, it can suppress that an etching damage is given to the upper surface of impurity diffusion region 2c1, and the upper surface of polysilicon wiring 3b. Thus, in recesses 50 and 51, insulating film 10A formed along the internal surface of recesses 50 and 51 and insulating film 10B which is formed on the upper surface of this insulating film 10A, and fills up the inside of recesses 50 and 51 are formed." Saito825 ¶ [0113]. "In FIG. 7, by etching into insulating film 10A, lamination insulating film 10 which consists of insulating film 10A and insulating film 10B is formed over the upper surface of sidewall 70 from the boundary region of the upper surface and the side surface of active region 2c, and it fills up with it in recess 50. And the edges of lamination insulating film 10 are smoothly formed successively to the upper surface of exposed impurity diffusion region 2c1. The upper surface of lamination insulating film 10 is made into the smooth curving surface ranging from the upper surface side of impurity diffusion region 2c1 to the sidewall 70 side. Here, a part of front surface

Exemplary Disclosures
of impurity diffused layer 2c1 exposed in recess 50 and a part of front surface of active region 2c which are located under impurity diffused layer 2c1 touch either insulating film 10A or insulating film 10B at least." Saito825 ¶ [0114]. "In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g." Saito825 ¶ [0124]. To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
5[a] The semiconductor device of claim 1, wherein the first sidewall spacer includes an inner sidewall spacer which is formed on the side surface of the first gate electrode, and whose cross-section has an L shape, and an outer sidewall spacer formed on the inner sidewall spacer.
To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

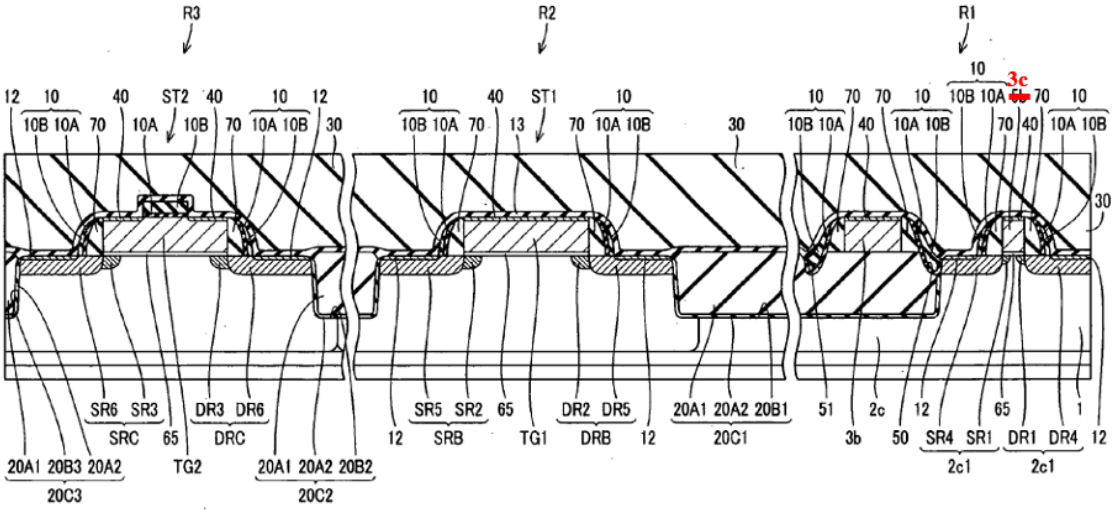
Exemplary Disclosures
7[a] The semiconductor device of claim 1, wherein the first MIS transistor is a p-type MIS transistor,
Saito825 discloses this feature. For example, Saito825 discloses a PMOS transistor. *See, e.g.*, the following:

FIG.12



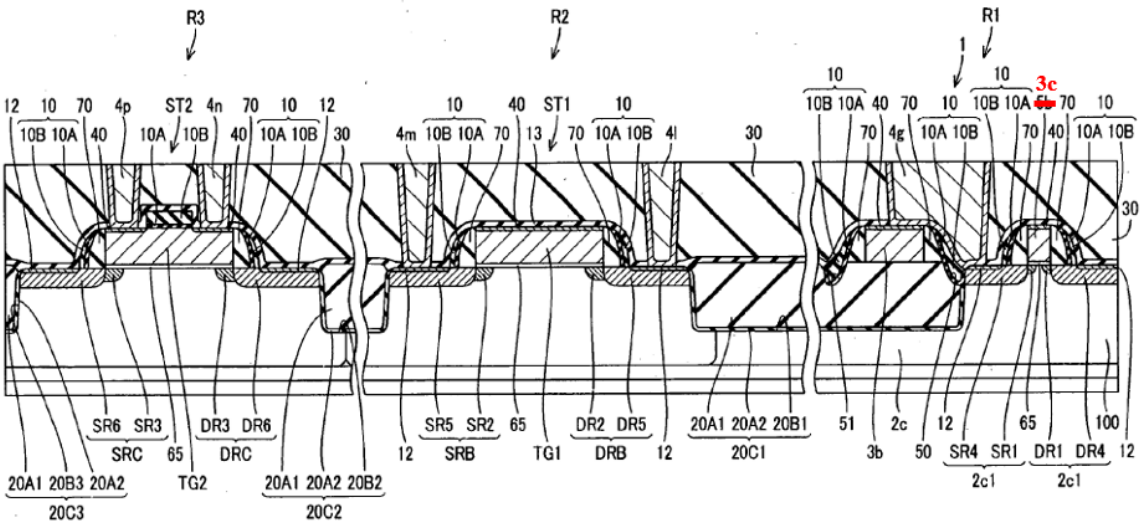
Saito825 FIG. 12 (corrected annotation).

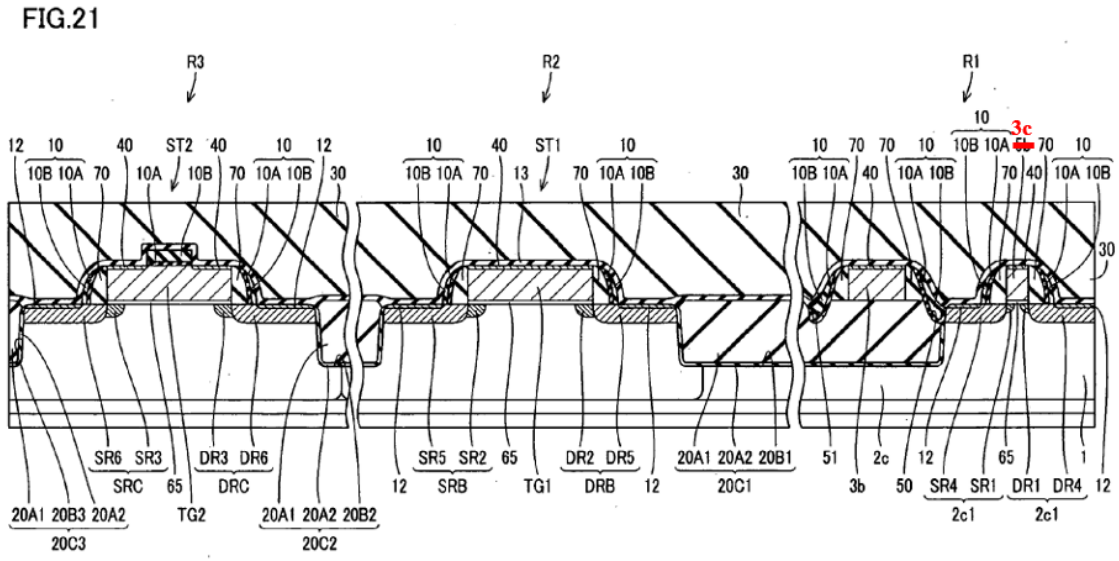
FIG.21



Saito825 FIG. 21 (corrected annotation).

Exemplary Disclosures
"On the main front surface of semiconductor substrate 100 in which memory cell region R1 is located, isolation region 20c1 and active region 2c specified by this isolation region 20c1 are formed. And on the main front surface of semiconductor substrate 100 in which active region 2c is located, gate insulating film 65, polysilicon wiring 5b [sic 3c] formed on the upper surface of this gate insulating film 65, and impurity diffused layer 2c1 located in the both sides of this polysilicon wiring 5b [sic 3c] are formed." Saito825 ¶ [0051]. "Memory node Na is connected to bit line BL1 via first access NMOS transistor N3, and memory node Nb is connected to bit line BL2 via second access NMOS transistor N4. The gate of further the first, second access NMOS transistor N3, and N4 is connected to word line WL, and the source of the first, second load PMOS transistor P1, and P2 is connected to power supply line VDD." Saito825 ¶ [0057]. "Memory cell 1 in this embodiment comprises six MOS transistors. Concretely, memory cell 1 comprises the first, the second driver NMOS transistor N1, N2, and the first, the second access NMOS transistor N3, N4 and the first, the second load PMOS transistor P1, P2." Saito825 ¶ [0062]. "The first, second access NMOS transistor N3, N4, and the first, second driver NMOS transistor N1 and N2 are formed on P well region of the both sides of N well region, respectively. The first, second load PMOS transistor P1, and P2 are formed on central N well region." Saito825 ¶ [0063]. "First load PMOS transistor P1 is formed in the intersection part of impurity diffusion region 2b1 comprising the region used as a source/drain, and polysilicon wiring 3b. Second access PMOS transistor P2 is formed in the intersection part of impurity diffusion region 2c1 comprising the region used as a source/drain, and polysilicon wiring 3c." Saito825 ¶ [0066]. To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

Exemplary Disclosures
7[b] the first stress is a compressive stress, and
To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
7[c] the second stress is a tensile stress.
To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
11[a] The semiconductor device of claim 1, further comprising: a second MIS transistor, wherein: the second MIS transistor includes:
Saito825 discloses this feature. For example, Saito825 discloses an NMOS transistor N1-N4. *See, e.g.*, the following: FIG.12      Saito825 FIG. 12 (corrected annotation).



Saito825 FIG. 21 (corrected annotation).

"Memory node Na is connected to bit line BL1 via first access NMOS transistor N3, and memory node Nb is connected to bit line BL2 via second access NMOS transistor N4. The gate of further the first, second access NMOS transistor N3, and N4 is connected to word line WL, and the source of the first, second load PMOS transistor P1, and P2 is connected to power supply line VDD."

Saito825 ¶ [0057].

"A first inverter and a second inverter form the flip-flop which connected a mutual input and a mutual output. The source of first access NMOS transistor N3 is connected to first memory node Na of a flip-flop, and the source of second access NMOS transistor N4 is connected to second memory node Nb of a flip-flop."

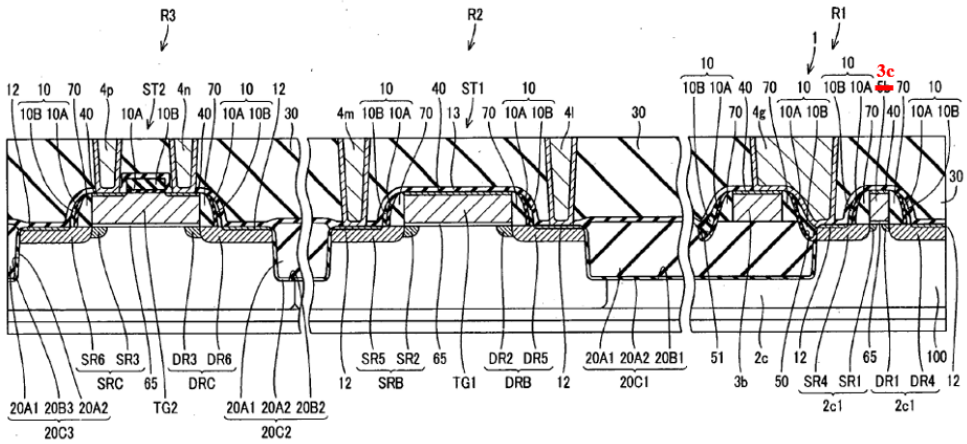
Saito825 ¶ [0058].

"Memory cell 1 in this embodiment comprises six MOS transistors. Concretely, memory cell 1 comprises the first, the second driver NMOS transistor N1, N2, and the first, the second access NMOS transistor N3, N4 and the first, the second load PMOS transistor P1, P2."

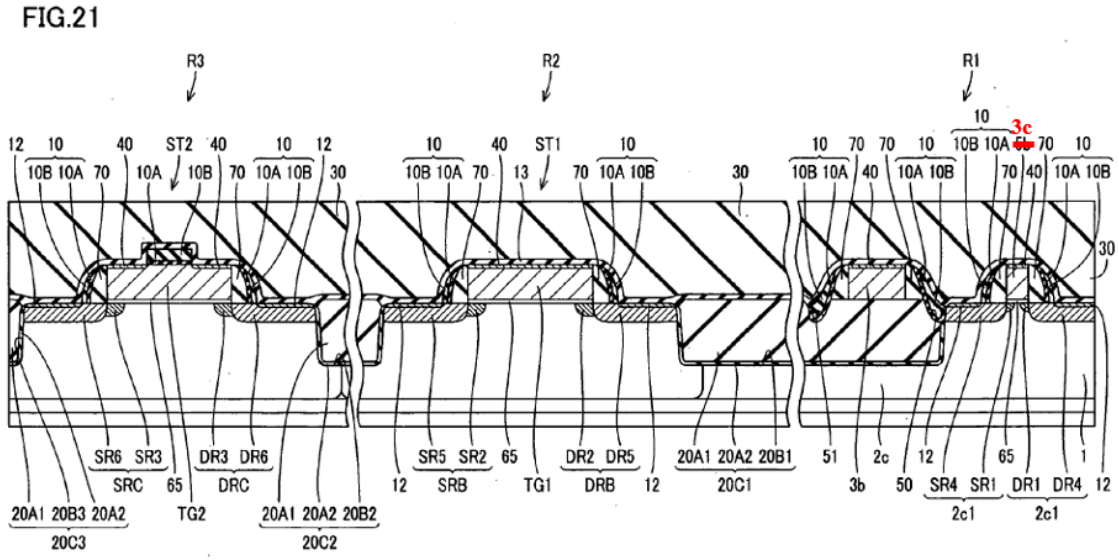
Saito825 ¶ [0062].

"The first, second access NMOS transistor N3, N4, and the first, second driver NMOS transistor N1 and N2 are formed on P well region of the both sides of N well region, respectively. The first, second load PMOS transistor P1, and P2 are formed on central N well region."

Saito825 ¶ [0063].

Exemplary Disclosures
"First access NMOS transistor N3 is formed in the intersection part of impurity diffusion region 2a1 comprising the region used as a source/drain, and polysilicon wiring 3a. Second access NMOS transistor N4 is formed in the intersection part of impurity diffusion region 2d1 comprising the region used as a source/drain, and polysilicon wirings 3d." Saito825 ¶ [0064]. "First driver NMOS transistor N1 is formed in the intersection part of impurity diffusion region 2a1 comprising the region used as a source/drain, and polysilicon wiring 3b. Second driver NMOS transistor N2 is formed in the intersection part of impurity diffusion region 2d1." Saito825 ¶ [0065]. "In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g." Saito825 ¶ [0124]. To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
11[b] a second gate insulating film formed on a second active region in the semiconductor substrate,
Saito825 discloses this feature. For example, Saito825 discloses a gate insulating film 65 formed on an NMOS active region in semiconductor substrate 100. *See, e.g.*, the following: FIG.12    Saito825 FIG. 12 (corrected annotation).

Exemplary Disclosures



Saito825 FIG. 21 (corrected annotation).

"On the main front surface of semiconductor substrate 100 in which memory cell region R1 is located, isolation region 20c1 and active region 2c specified by this isolation region 20c1 are formed. And on the main front surface of semiconductor substrate 100 in which active region 2c is located, gate insulating film 65, polysilicon wiring 5b [sic 3c] formed on the upper surface of this gate insulating film 65, and impurity diffused layer 2c1 located in the both sides of this polysilicon wiring 5b [sic 3c] are formed."

Saito825 ¶ [0051].

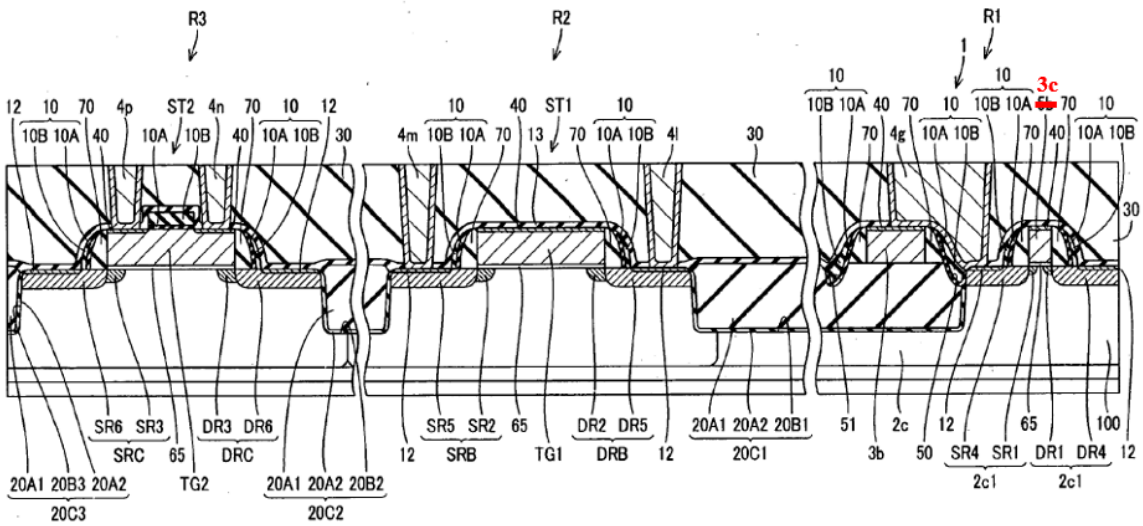
"In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g."

Saito825 ¶ [0124].

To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

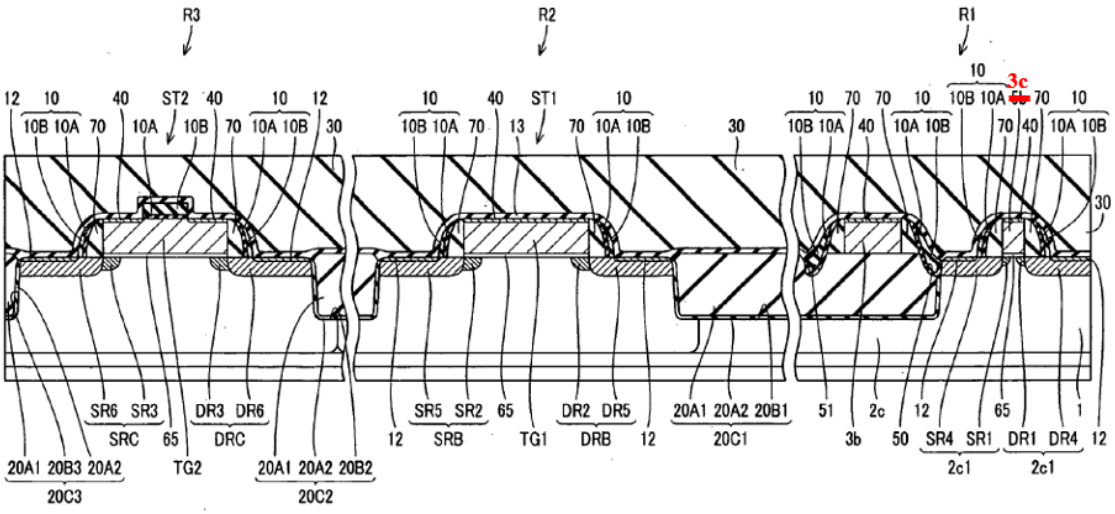
Exemplary Disclosures
11[c] a second gate electrode formed on the second gate insulating film,
Saito825 discloses this feature. For example, Saito825 discloses NMOS gate electrodes 3a-3d formed on the NMOS gate insulating film 65. *See, e.g.*, the following:

FIG.12



Saito825 FIG. 12 (corrected annotation).

FIG.21

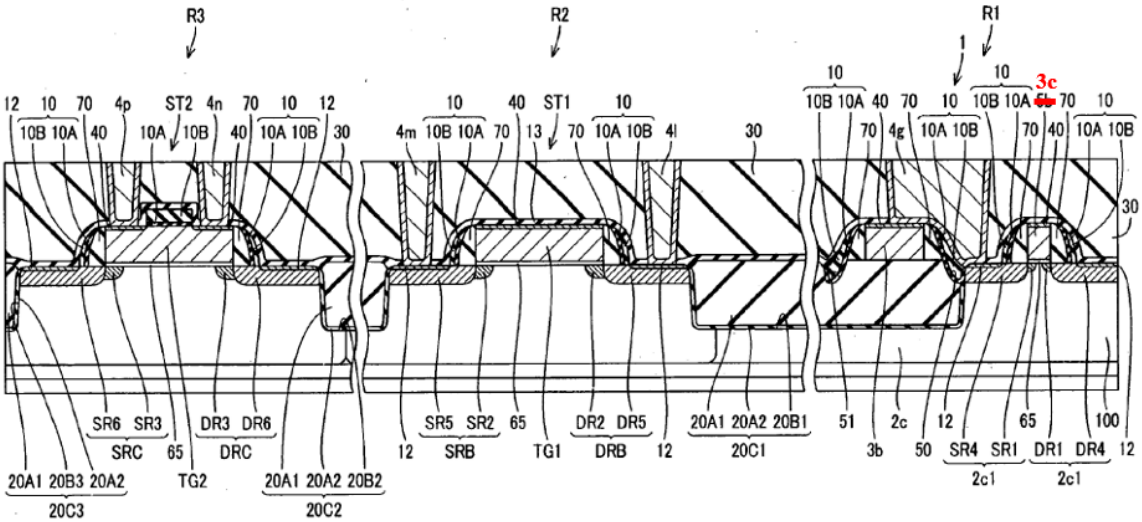


Saito825 FIG. 21 (corrected annotation).

Exemplary Disclosures
"On the main front surface of semiconductor substrate 100 in which memory cell region R1 is located, isolation region 20c1 and active region 2c specified by this isolation region 20c1 are formed. And on the main front surface of semiconductor substrate 100 in which active region 2c is located, gate insulating film 65, polysilicon wiring 5b [sic 3c] formed on the upper surface of this gate insulating film 65, and impurity diffused layer 2c1 located in the both sides of this polysilicon wiring 5b [sic 3c] are formed." Saito825 ¶ [0051]. "First load PMOS transistor P1 is formed in the intersection part of impurity diffusion region 2b1 comprising the region used as a source/drain, and polysilicon wiring 3b. Second access PMOS transistor P2 is formed in the intersection part of impurity diffusion region 2c1 comprising the region used as a source/drain, and polysilicon wiring 3c." Saito825 ¶ [0066]. "And on the main front surface of semiconductor substrate 100, a polysilicon film etc. is deposited and an impurity is introduced into this polysilicon film, for example. It patterns by using a photolithography etc. for the polysilicon film with which this impurity was introduced, and polysilicon wirings 5b [sic 3c] and 3b, and gate wiring TG1 and TG2 are formed." Saito825 ¶ [0093]. "In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g." Saito825 ¶ [0124]. Additionally, under Plaintiff's apparent interpretation of the claim language, the claimed "second gate electrode" may include a silicide film. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 35-43. Although TSMC does not necessarily agree with such an interpretation, Saito825 further discloses this element under this interpretation, as shown below. For example, Saito825 discloses silicide film 40 formed on NMOS gate electrodes 3a-3d. *See, e.g.*, the following:

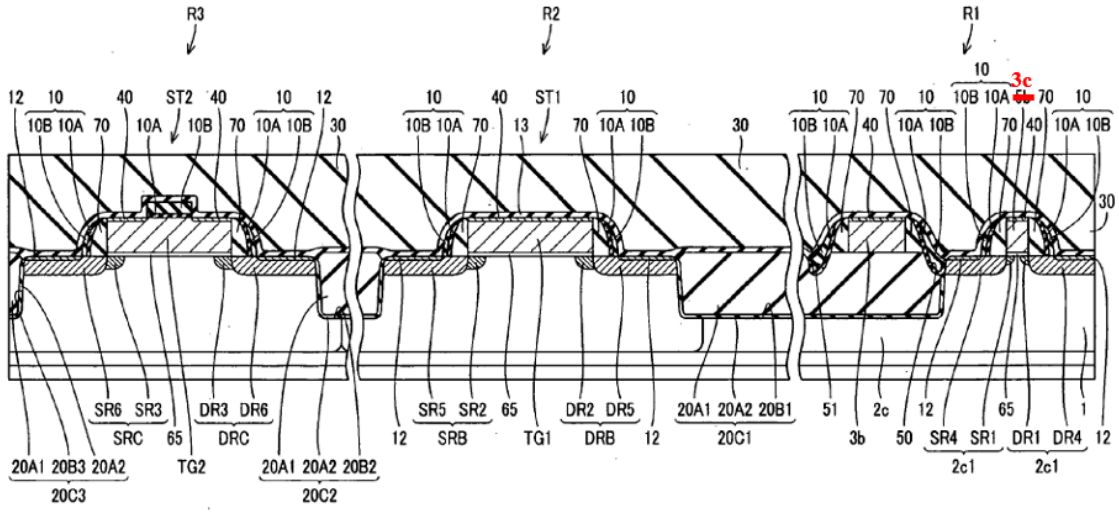
Exemplary Disclosures

FIG.12



Saito825 FIG. 12 (corrected annotation).

FIG.21



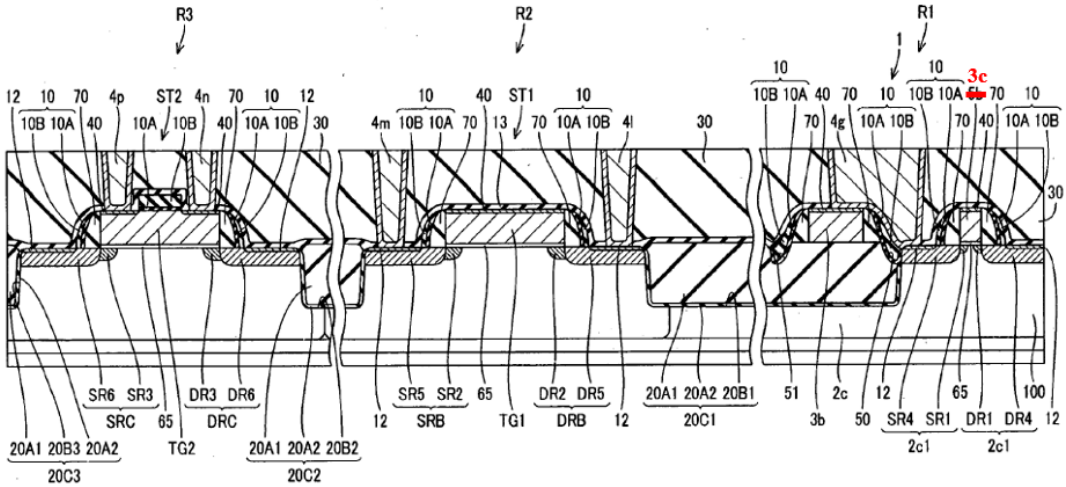
Saito825 FIG. 21 (corrected annotation).

"Also on the upper surface of polysilicon wiring 3b, silicide film 40 which consists of a cobalt silicide film etc. is formed. And interlayer insulation film 30 is formed so that sidewall 70, polysilicon wiring 3b, and lamination insulating film 10 may be covered. This interlayer insulation film 30 is provided with insulating film 13 which is formed on silicide films 12 and 40 and consists of a plasma nitride (SiN) etc., insulating film 14 which is formed on insulating film 13 and consists of a HDP (high density plasma: High Density Plasma) film etc., insulating

Exemplary Disclosures
film 15 which is formed on this insulating film 14 and consists of a silicon oxide film formed by the CVD method using TEOS (Tetraethoxysilane) gas etc., and insulating film 16 formed on this insulating film 15." Saito825 ¶ [0080]. "FIG. 8 and FIG. 20 are the cross-sectional views showing the ninth step of the manufacturing process of semiconductor device 200. Since it fills up with lamination insulating film 10 in recess 50, it can suppress that the internal surface of recess 50 is exposed. And metallic films, such as cobalt (Co), are deposited, about 10 nm, on the main front surface of semiconductor substrate 100 by the sputtering method." Saito825 ¶ [0116]. "Then, heat treatment about more than 400° C. and below 600° C. is performed, silicon and cobalt react (silicidation), and silicide films 12 and 40 are formed. And wet etching removes unreacted cobalt. After an appropriate time, it heat-treats in the range of more than 700° C. and less than 800° C. Thus, silicide film 12 is formed on the front surface of impurity diffused layer 2c1, 2c1, SRB, DRB, SRC, and DRC. Silicide film 40 is formed on the upper surface of polysilicon wiring 5b [sic 3c] and 3b and gate wiring TG1. Since insulating films 10A and 10B remain on the upper surface of gate wiring TG2, silicide film 40 is formed on the upper surface of gate wiring TG2 which adjoins insulating films 10A and 10B." Saito825 ¶ [0117]. "Thus, when forming silicide films 12 and 40, the front surface of impurity diffused layer 2c1 exposed in recess 50 and the front surface of active region 2 located under impurity diffused layer 2c1 touch lamination insulating film 10 which consists of insulating film 10A and insulating film 10B. For this reason, it is suppressed that a silicide film is formed in the front surface of impurity diffused layer 2c1 located in recess 50 and the front surface of active region 2c located under impurity diffused layer 2c1." Saito825 ¶ [0118]. "In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g." Saito825 ¶ [0124]. *See also, e.g.*, Saito825 ¶ [0024], ¶ [0026], ¶ [0055], ¶¶ [0077]-[0084], ¶ [0104], ¶ [0107], ¶¶ [0116]-[0120], ¶¶ [0122]-[0124], FIGS. 3, 8-12, 20-21.

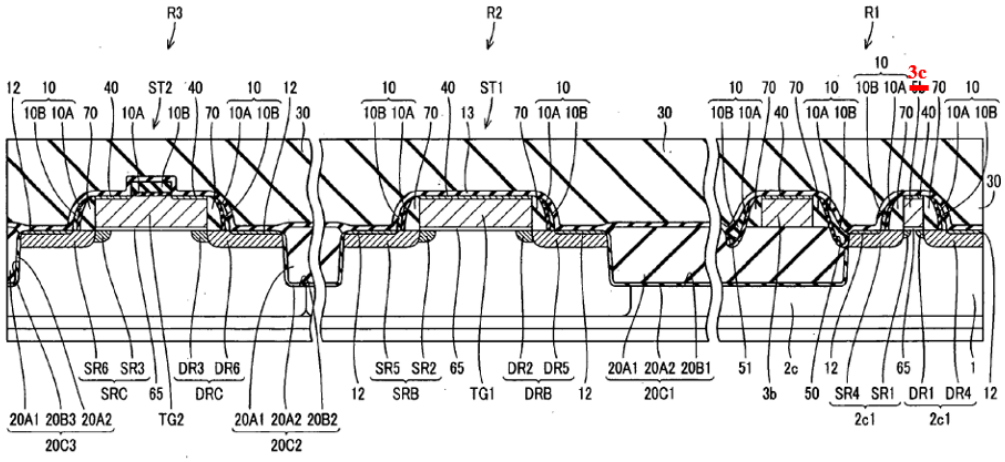
Exemplary Disclosures
To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.
11[d] a second sidewall spacer formed on a side surface of the second gate electrode,
Saito825 discloses this feature. For example, Saito825 discloses NMOS sidewall oxide 70 formed on a side surface of NMOS gate electrodes 3a-3d. *See, e.g.*, the following:

FIG.12



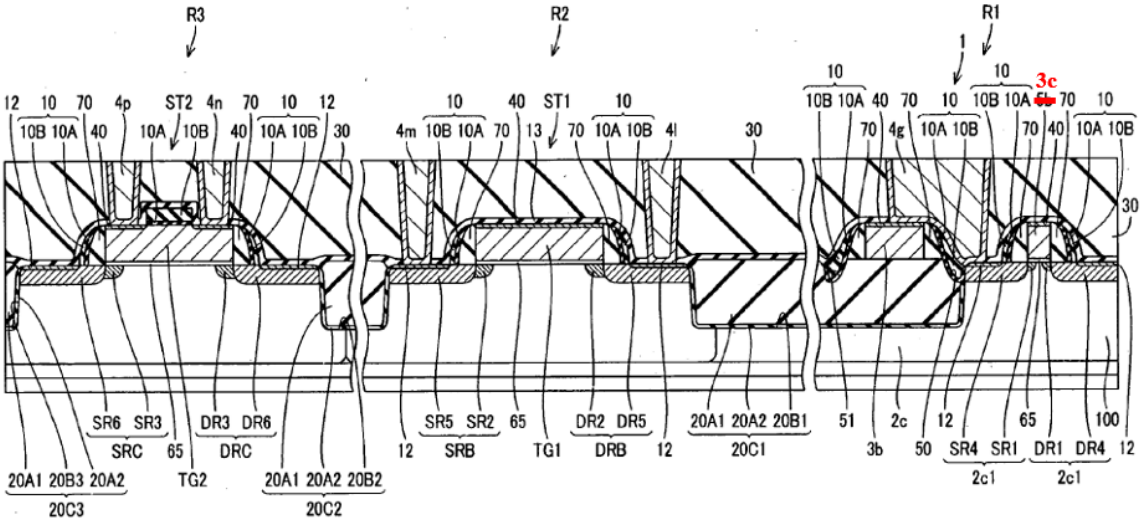
Saito825 FIG. 12 (corrected annotation).

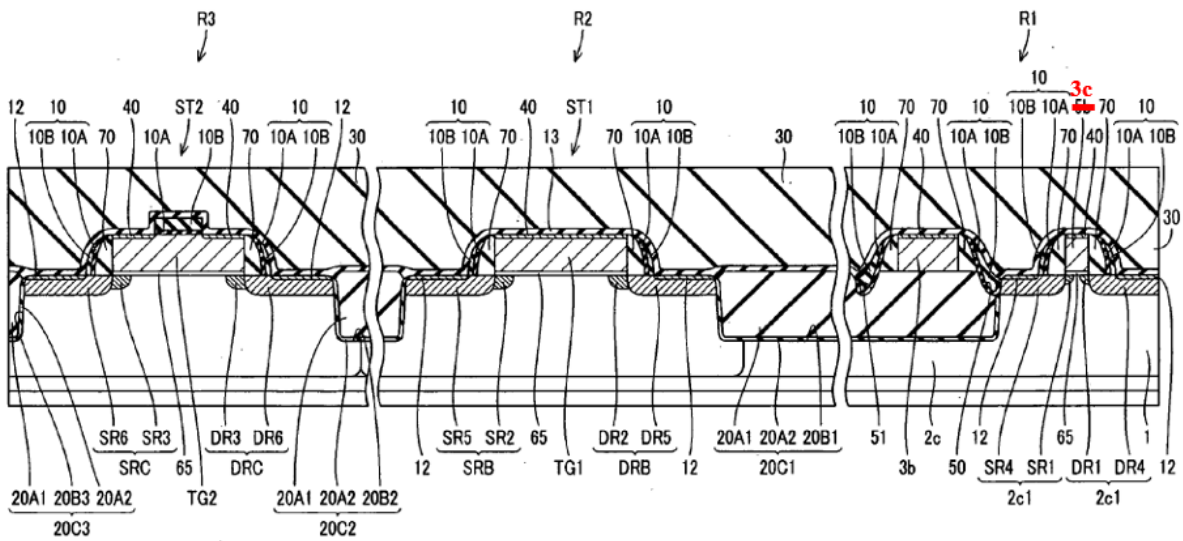
FIG.21



Saito825 FIG. 21 (corrected annotation).

Exemplary Disclosures
"On the main front surface of semiconductor substrate 100 in which memory cell region R1 is located, isolation region 20c1 and active region 2c specified by this isolation region 20c1 are formed. And on the main front surface of semiconductor substrate 100 in which active region 2c is located, gate insulating film 65, polysilicon wiring 5b [sic 3c] formed on the upper surface of this gate insulating film 65, and impurity diffused layer 2c1 located in the both sides of this polysilicon wiring 5b [sic 3c] are formed." Saito825 ¶ [0051]. "Isolation region 20c1 is provided with trench 20B1 formed on the main front surface of semiconductor substrate 1, insulating film 20A2 which is formed on the internal surface of this trench 20B1, and consists of a silicon oxide film etc., and insulating film 20A1 which were formed on this insulating film 20A2 and with which it filled up in trench 20B. Insulating film 20A1 comprises a silicon oxide film etc., for example. And on isolation insulating film 20A1, polysilicon wiring (wiring layer) 3b is formed. On the both side surfaces of this polysilicon wiring 3b, sidewall (side wall oxide film) 70 which consists of a silicon oxide film etc. is formed, for example." Saito825 ¶ [0070]. "FIG. 4 is a cross-sectional view showing the fifth step of the manufacturing process of semiconductor device 200. As shown in this FIG. 4, insulating film 70a which consists of a silicon oxide film etc. is deposited." Saito825 ¶ [0095]. "FIG. 5 and FIG. 17 are the cross-sectional views showing the sixth step of the manufacturing process of semiconductor device 200. As shown in this FIG. 5 and FIG. 17, it etches into insulating film 70a, and sidewall 70 is formed on the both side surfaces of gate wiring TG1, gate wiring TG2, polysilicon wiring 5b [sic 3c], and polysilicon wiring 3b." Saito825 ¶ [0096]. "On this occasion, the front surface at the side of impurity diffused layer SR1 among the front surfaces of isolation insulating film 20A1 is exposed from sidewall 70 formed on the side surface at the side of impurity diffused layer SR1 of polysilicon wiring 3b. Here, since isolation insulating film 20A1 and insulating film 20B1, and sidewall 70 comprise a homogeneous silicon oxide film etc., recess 50 is formed in the portion located in impurity diffused layer SR1 side from sidewall 70 among the front surfaces of isolation insulating film 20A1." Saito825 ¶ [0097].

Exemplary Disclosures
"In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g." Saito825 ¶ [0124]. Additionally, under Plaintiff's apparent interpretation of the claim language, the claimed "second gate electrode" may include a silicide film. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 35-43. Although TSMC does not necessarily agree with such an interpretation, Saito825 further discloses this element under this interpretation, as shown below. For example, Saito825 discloses silicide film 40 formed on NMOS gate electrodes 3a-3d. *See, e.g.*, the following: FIG.12    Saito825 FIG. 12 (corrected annotation).



Saito825 FIG. 21 (corrected annotation).

"Also on the upper surface of polysilicon wiring 3b, silicide film 40 which consists of a cobalt silicide film etc. is formed. And interlayer insulation film 30 is formed so that sidewall 70, polysilicon wiring 3b, and lamination insulating film 10 may be covered. This interlayer insulation film 30 is provided with insulating film 13 which is formed on silicide films 12 and 40 and consists of a plasma nitride (SiN) etc., insulating film 14 which is formed on insulating film 13 and consists of a HDP (high density plasma: High Density Plasma) film etc., insulating film 15 which is formed on this insulating film 14 and consists of a silicon oxide film formed by the CVD method using TEOS (Tetraethoxysilane) gas etc., and insulating film 16 formed on this insulating film 15."

Saito825 ¶ [0080].

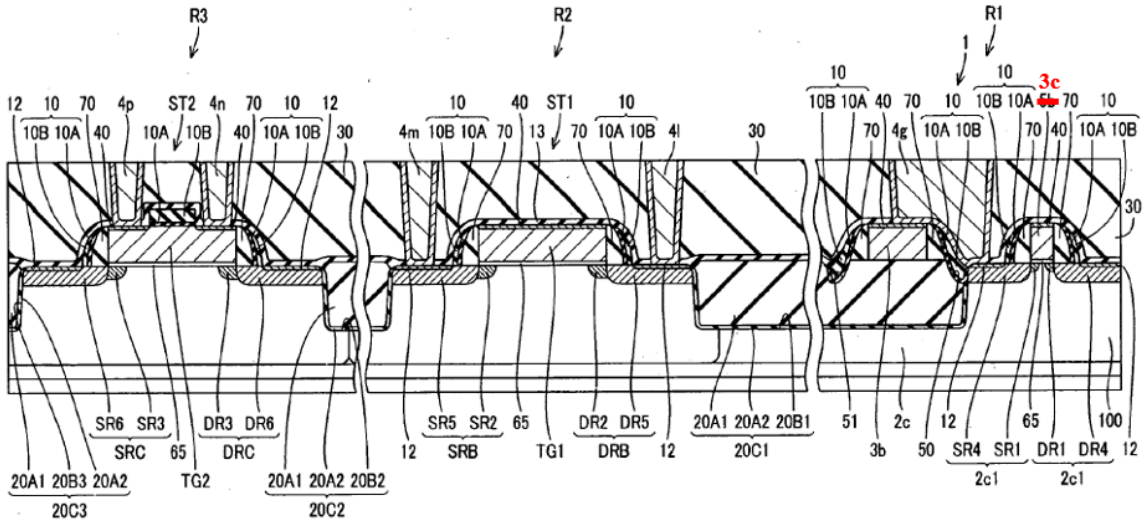
"FIG. 8 and FIG. 20 are the cross-sectional views showing the ninth step of the manufacturing process of semiconductor device 200. Since it fills up with lamination insulating film 10 in recess 50, it can suppress that the internal surface of recess 50 is exposed. And metallic films, such as cobalt (Co), are deposited, about 10 nm, on the main front surface of semiconductor substrate 100 by the sputtering method."

Saito825 ¶ [0116].

Exemplary Disclosures
"Then, heat treatment about more than 400° C. and below 600° C. is performed, silicon and cobalt react (silicidation), and silicide films 12 and 40 are formed. And wet etching removes unreacted cobalt. After an appropriate time, it heat-treats in the range of more than 700° C. and less than 800° C. Thus, silicide film 12 is formed on the front surface of impurity diffused layer 2c1, 2c1, SRB, DRB, SRC, and DRC. Silicide film 40 is formed on the upper surface of polysilicon wiring 5b [sic 3c] and 3b and gate wiring TG1. Since insulating films 10A and 10B remain on the upper surface of gate wiring TG2, silicide film 40 is formed on the upper surface of gate wiring TG2 which adjoins insulating films 10A and 10B." Saito825 ¶ [0117]. "Thus, when forming silicide films 12 and 40, the front surface of impurity diffused layer 2c1 exposed in recess 50 and the front surface of active region 2 located under impurity diffused layer 2c1 touch lamination insulating film 10 which consists of insulating film 10A and insulating film 10B. For this reason, it is suppressed that a silicide film is formed in the front surface of impurity diffused layer 2c1 located in recess 50 and the front surface of active region 2c located under impurity diffused layer 2c1." Saito825 ¶ [0118]. "In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g." Saito825 ¶ [0124]. *See also, e.g.*, Saito825 ¶ [0024], ¶ [0026], ¶ [0055], ¶¶ [0077]-[0084], ¶ [0104], ¶ [0107], ¶¶ [0116]-[0120], ¶¶ [0122]-[0124], FIGS. 3, 8-12, 20-21. To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

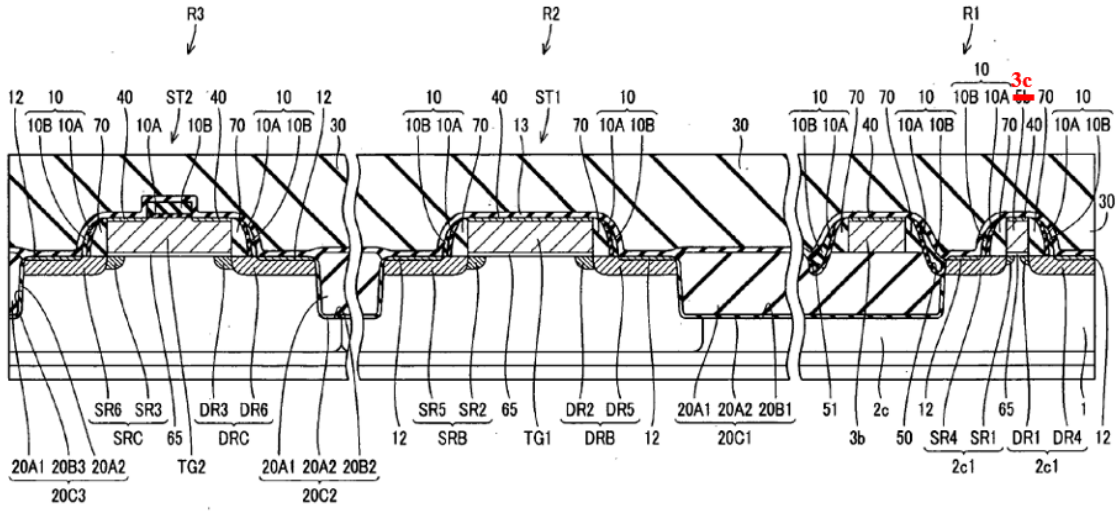
Exemplary Disclosures
11[e] a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer, and
Saito825 discloses this feature. For example, Saito825 discloses an NMOS source/drain region formed within regions 2a, 2d formed in the NMOS active region on a lateral side of NMOS sidewall oxide 70. *See, e.g.*, the following:

FIG.12



Saito825 FIG. 12 (corrected annotation).

FIG.21

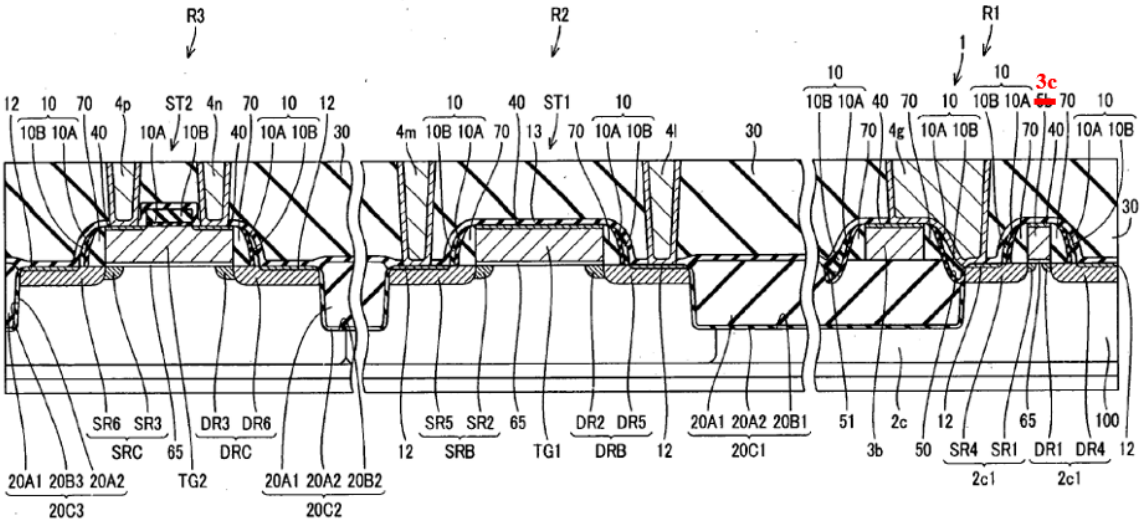


Saito825 FIG. 21 (corrected annotation).

Exemplary Disclosures
"In FIG. 1, the N type impurity diffusion region used as the drain of first driver NMOS transistor N1 and the N type impurity diffusion region used as the drain of first access NMOS transistor N3 are shared by these transistors. Via contact part 4c formed on this N type impurity diffusion region, first metal wiring 5a, and contact parts (common contact) 4f, the drain of first driver NMOS transistor N1 and the drain of first access NMOS transistor N3 are connected with the drain of first load transistor P1. This terminal constitutes memory node Na of an equivalent circuit picture shown in FIG. 2." Saito825 ¶ [0070]. "Similarly the N type impurity diffusion region which is a drain of second driver NMOS transistor N2, and the N type impurity diffusion region which is a drain of second access NMOS transistor N3 connect with the drain of second load transistor P2 via contact part 4j, first metal wiring 5b, and contact parts (common contact) 4g. This terminal constitutes memory node Nb of an equivalent circuit picture shown in FIG. 2." Saito825 ¶ [0071]. "In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g." Saito825 ¶ [0124]. To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.

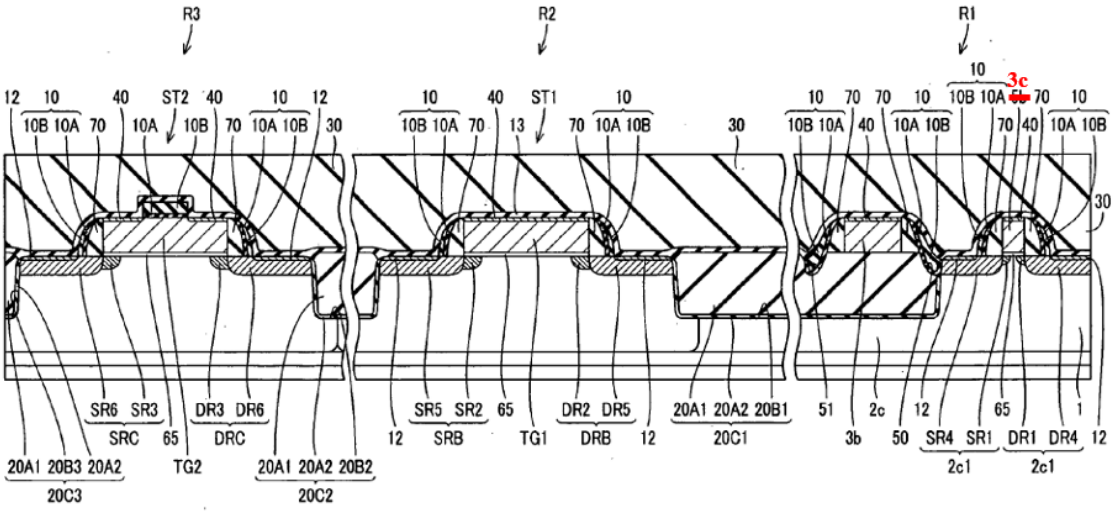
Exemplary Disclosures
11[f] the stress insulating film formed on the second active region to cover the second gate electrode, the second sidewall spacer, and the second source/drain region.
Saito825 discloses this feature. For example, Saito825 discloses insulating film 13 formed on the NMOS active region to cover NMOs gate electrodes 3a-3d, NMOS sidewall spacer 70, and NMOS source/drain regions in NMOS active regions 2a, 2d. *See, e.g.*, the following:

FIG.12



Saito825 FIG. 12 (corrected annotation).

FIG.21

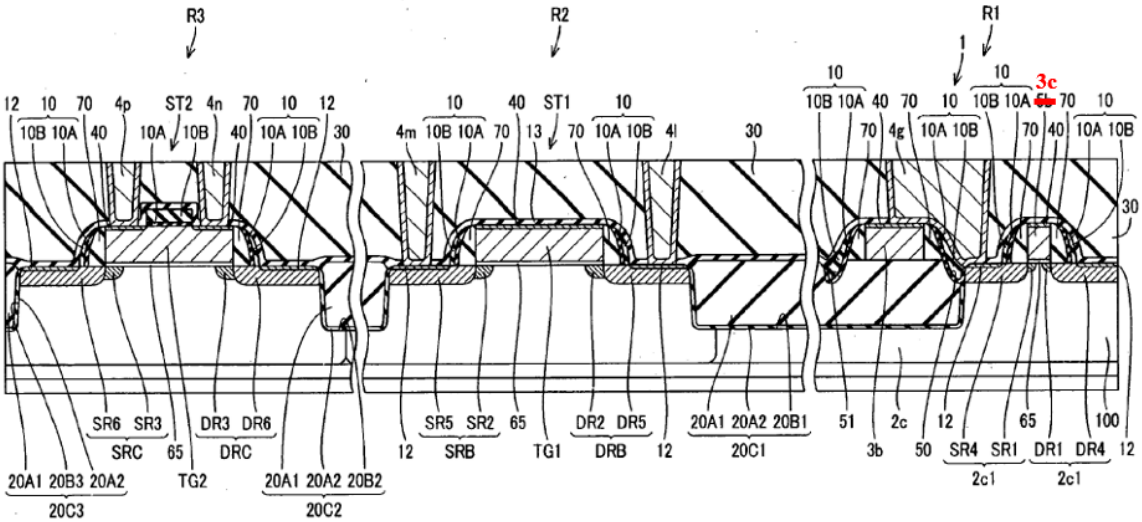


Saito825 FIG. 21 (corrected annotation).

Exemplary Disclosures
"Also on the upper surface of polysilicon wiring 3b, silicide film 40 which consists of a cobalt silicide film etc. is formed. And interlayer insulation film 30 is formed so that sidewall 70, polysilicon wiring 3b, and lamination insulating film 10 may be covered. This interlayer insulation film 30 is provided with insulating film 13 which is formed on silicide films 12 and 40 and consists of a plasma nitride (SiN) etc., insulating film 14 which is formed on insulating film 13 and consists of a HDP (high density plasma: High Density Plasma) film etc., insulating film 15 which is formed on this insulating film 14 and consists of a silicon oxide film formed by the CVD method using TEOS (Tetraethoxysilane) gas etc., and insulating film 16 formed on this insulating film 15." Saito825 ¶ [0080]. "And insulating film 14 which consists of a HDP (high density plasma: High Density Plasma) film etc. is formed on this insulating film 13. On this insulating film 14, insulating film 15 is formed with the CVD method which used for example, TEOS (Tetraethoxysilane) gas. Insulating film 16 is formed on the upper surface of insulating film 15, and interlayer insulation film 30 is formed." Saito825 ¶ [0120]. "In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g." Saito825 ¶ [0124]. A POSITA would have understood the stress insulating layer extends over the NMOS gate electrodes and between neighboring transistors. Although the contact plugs (FIG. 12) penetrate the stress insulating film (FIG. 12) in the cross-section shown above, a POSITA would have understood the stress insulating film extends unbroken between neighboring transistors in other cross-sections, where the contact plugs are not formed, such as in cross-sections located behind and in front of the one shown above. Additionally, under Plaintiff's apparent interpretation of the claim language, the claimed "second gate electrode" may include a silicide film. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 35-43. Although TSMC does not necessarily agree with such an interpretation, Saito825 further discloses this element under this interpretation, as shown below. For example, Saito825 discloses silicide film 40 formed on NMOS gate electrode 3a-3d. *See, e.g.*, the following:

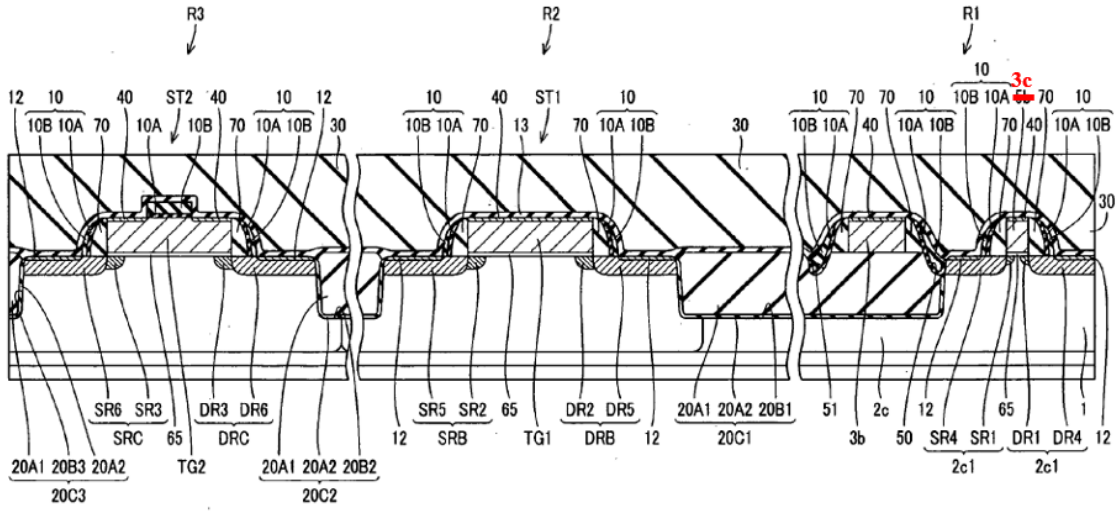
Exemplary Disclosures

FIG.12



Saito825 FIG. 12 (corrected annotation).

FIG.21



Saito825 FIG. 21 (corrected annotation).

"Also on the upper surface of polysilicon wiring 3b, silicide film 40 which consists of a cobalt silicide film etc. is formed. And interlayer insulation film 30 is formed so that sidewall 70, polysilicon wiring 3b, and lamination insulating film 10 may be covered. This interlayer insulation film 30 is provided with insulating film 13 which is formed on silicide films 12 and 40 and consists of a plasma nitride (SiN) etc., insulating film 14 which is formed on insulating film 13 and consists of a HDP (high density plasma: High Density Plasma) film etc., insulating

Exemplary Disclosures
film 15 which is formed on this insulating film 14 and consists of a silicon oxide film formed by the CVD method using TEOS (Tetraethoxysilane) gas etc., and insulating film 16 formed on this insulating film 15." Saito825 ¶ [0080]. "FIG. 8 and FIG. 20 are the cross-sectional views showing the ninth step of the manufacturing process of semiconductor device 200. Since it fills up with lamination insulating film 10 in recess 50, it can suppress that the internal surface of recess 50 is exposed. And metallic films, such as cobalt (Co), are deposited, about 10 nm, on the main front surface of semiconductor substrate 100 by the sputtering method." Saito825 ¶ [0116]. "Then, heat treatment about more than 400° C. and below 600° C. is performed, silicon and cobalt react (silicidation), and silicide films 12 and 40 are formed. And wet etching removes unreacted cobalt. After an appropriate time, it heat-treats in the range of more than 700° C. and less than 800° C. Thus, silicide film 12 is formed on the front surface of impurity diffused layer 2c1, 2c1, SRB, DRB, SRC, and DRC. Silicide film 40 is formed on the upper surface of polysilicon wiring 5b [sic 3c] and 3b and gate wiring TG1. Since insulating films 10A and 10B remain on the upper surface of gate wiring TG2, silicide film 40 is formed on the upper surface of gate wiring TG2 which adjoins insulating films 10A and 10B." Saito825 ¶ [0117]. "Thus, when forming silicide films 12 and 40, the front surface of impurity diffused layer 2c1 exposed in recess 50 and the front surface of active region 2 located under impurity diffused layer 2c1 touch lamination insulating film 10 which consists of insulating film 10A and insulating film 10B. For this reason, it is suppressed that a silicide film is formed in the front surface of impurity diffused layer 2c1 located in recess 50 and the front surface of active region 2c located under impurity diffused layer 2c1." Saito825 ¶ [0118]. "In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g." Saito825 ¶ [0124]. *See also, e.g.*, Saito825 ¶ [0024], ¶ [0026], ¶ [0055], ¶¶ [0077]-[0084], ¶ [0104], ¶ [0107], ¶¶ [0116]-[0120], ¶¶ [0122]-[0124], FIGS. 3, 8-12, 20-21.

Exhibit 425-16: Saito825

Exemplary Disclosures
To the extent that Saito825 is found not to disclose this feature, it would have been obvious based on the disclosures of Saito825 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 425-01 through 425-15 and 425-17 through 425-21 for the reasons discussed herein and in Defendant's cover pleading.