

Docket No.: 085393-0059

**REQUEST FORM FOR CONTINUATION
APPLICATION UNDER 35 USC 111(a)**

Prior Application: **International Application No. PCT/JP2009/000574**
Art Unit: **(Unassigned)**
Examiner: **(Unassigned)**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is a Request for filing a continuation or continuation-in-part application, entitled
SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME, under 35
U.S.C. 111(a) of pending prior International Application No. **PCT/JP2009/000574**, filed on **February**
13, 2009, by the following named inventors:

INVENTOR	RESIDENCE	CITIZENSHIP	POST OFFICE ADDRESS
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1. ☒ I hereby verify, to the best of my knowledge, that the enclosed copy of this prior application is a true copy of the above-identified prior application, including the oath or declaration as originally filed.
2. ☐ Preliminary Amendment is enclosed.
3. ☒ An Information Disclosure Statement and PTO1449 Form are submitted herewith.
4. ☐ Cancel claims _____.
5. ☐ Applicant is entitled to claim Small Entity status.
6. The filing fee is calculated on the basis of the claims existing in the prior application as amended above:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	20	-20	0	\$52.00	\$0.00
Independent Claims	2	-3	0	\$220.00	\$0.00
Multiple Dependent Claim(s)					\$0.00
Sheets of specification and drawing (\$260.00 for each 50 sheets in excess of 100)					\$0.00
Basic Filing Fee					\$330.00
Patent Search Fee					\$540.00
Patent Examination Fee					\$220.00
Total of Above Calculations					\$1,090.00
Less ½ for Small Entity					\$0.00
Assignment & Recording Fee					\$0.00
Total Fee					\$1,090.00

1. ☒ The Commissioner is hereby authorized to charge fees under 37 CFR 1.16 and 1.17 which may be required, including any extension of time fees including any extension of time fees or credit any overpayment to Deposit Account No. 500417.
2. ☐ Amend the specification by inserting before the first line the sentence:
3. ☒ Priority of **Japanese** Application No. **2008-064435** filed on **March 13, 2008**, in **Japan** and International Application No. PCT/JP2009/000574 filed **February 13, 2009** designating the U.S. is claimed under 35 USC 119, 120 and/or 365.
4. ☒ The prior application is assigned of record to:

PANASONIC CORPORATION
Osaka, Japan
5. ☒ The power of attorney in the prior application is to:

MAEDA PATENT OFFICE
Osaka, Japan

6. ☒ Also enclosed:

- Executed Declaration and Power of Attorney
- Copy of PCT Request
- Copy of Form PCT/IB/301
- Copy of Form PCT/IB/304
- Form PCT/ISA/210
- Form PCT/ISA/237

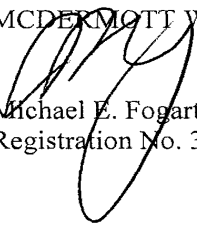
7. ☐ A petition, fee and response has been filed to extend the term in the pending prior application until _____.

8. ☒ Address all future communications to: (May only be completed by applicant, or attorney or agent of record)

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Respectfully submitted,

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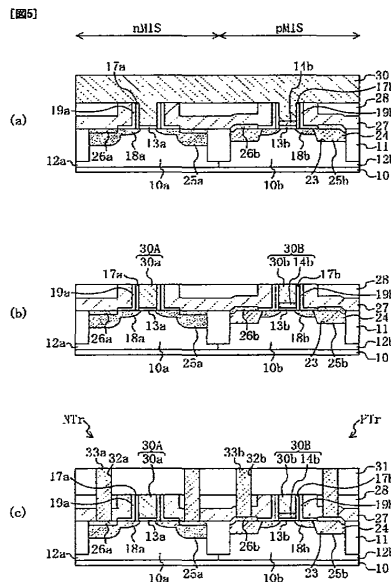
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- (81) 指定国(表示のない限り、全ての種類の国内保護が可能): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) 指定国(表示のない限り、全ての種類の広域保護が可能): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), ユーラシア (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), ヨーロッパ (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[続葉有]

(54) Title: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

(54) 発明の名称: 半導体装置及びその製造方法



(57) Abstract: A semiconductor device is provided with first and second MIS transistors. The first MIS transistor has a first gate insulating film formed on a first active region; a first gate electrode which is formed on the first gate insulating film and composed of a second metal film; and an insulating film formed over from a side surface of the first gate electrode to an upper surface of a region positioned on the side of the first gate electrode in the first active region. The second MIS transistor has a second gate insulating film formed on a second active region; a second gate electrode which is formed on the second gate insulating film and composed of a first metal film and a conductive film formed on the first metal film; and an insulating film formed over from a side surface of the second gate electrode to an upper surface in a region positioned on the side of the second gate electrode in the second active region. The first metal film and the second metal film are composed of different metal materials, respectively. No insulating film is formed on the upper surfaces of the first and the second gate electrodes.

(57) 要約: 半導体装置は、第1、第2のMISトランジスタとを備えている。第1のMISトランジスタは、第1の活性領域上に形成された第1のゲート絶縁膜と、第1のゲート絶縁膜上に形成された第2の金属膜からなる第1のゲート電極と、第1のゲート電極の側面上から第1の活性領域における第1のゲート電極の側方に位置する領域の上面上に跨って形成された絶縁膜とを有している。第2のMISトランジスタは、第2の活性領域上に形成された第2のゲート絶縁膜と、第2のゲート絶縁膜上に形成された第1の金属膜と第1の金属膜上に形成された導電膜とからなる第2のゲート電極と、第2のゲート電極の側面上から第2の活性領域における第2のゲート電極の側方に位置する領域の上面上に跨って形成された絶縁膜とを有している。第1の金属膜と第2の金属膜とは、互いに異なる金属材料からなる。第1、第2のゲート電極の各上面上には、絶縁膜が形成されていない。

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添付公開書類:

— 国際調査報告 (条約第 21 条(3))

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

This is a continuation of PCT International Application PCT/JP2009/000574 filed
5 on February 13, 2009, which claims priority to Japanese Patent Application No. 2008-064435
filed on March 13, 2008. The disclosures of the applications including the specification, the
drawings, and the claims are hereby incorporated by reference in their entirety.

BACKGROUND

10 The present disclosure relates to semiconductor devices and methods for
manufacturing the semiconductor devices. More particularly, the present disclosure relates
to a semiconductor device including a Metal Insulator Semiconductor Field Effect Transistor
(MISFET) having a gate electrode made of a metal material, and a method for manufacturing
the semiconductor device.

15 As the scale and speed of semiconductor integrated circuit devices increase, an
attempt is being made to achieve further miniaturization of MISFETs. The further
miniaturization of MISFETs is accompanied by an extremely thin thickness of the gate
insulating film, leading to problems, such as manifestation of the depletion capacitance of the
polysilicon gate electrode and penetration of boron into the channel region. To solve these
20 problems, a semiconductor device with a dual-metal gate structure has been studied in which
a metal gate electrode made of a metal material is used as the gate electrode of an n-type
MISFET (hereinafter referred to as an “n-type MIS transistor”), and a metal gate electrode
made of a metal material is used as the gate electrode of a p-type MISFET (hereinafter
referred to as a “p-type MIS transistor”).

25 In the case of the dual-metal gate semiconductor device, the gate electrodes of the

n- and p-type MIS transistors need to be made of different metal materials. For example, the gate electrode of the n-type MIS transistor is made of a metal material having a work function of 4.05 eV or more and 4.6 eV or less, and the gate electrode of the p-type MIS transistor is made of a metal material having a work function of 4.6 eV or more and 5.15 eV or less.

5 As a method for manufacturing the dual-metal gate semiconductor device, for example, a first conventional semiconductor device manufacturing method (see, for example, NON-PATENT DOCUMENT 1) and a second conventional semiconductor device manufacturing method (see, for example, NON-PATENT DOCUMENT 2) have been proposed.

10

CITATION LIST

NON-PATENT DOCUMENTS

NON-PATENT DOCUMENT 1: Z. B. Zhang et al., "Integration of Dual Metal Gate CMOS with TaSiN (NMOS) and Ru (PMOS) Gate Electrodes on HfO₂ Gate Dielectric," VLSI 2005

NON-PATENT DOCUMENT 2: S. C. Song et al., "Highly Manufacturable 45nm LSTP CMOSFETs Using Novel Dual High-k and Dual Metal Gate CMOS Integration," VLSI 2006

20 SUMMARY

However, the first and second conventional semiconductor device manufacturing methods have the following problems.

The first conventional semiconductor device manufacturing method and its problems will be described hereinafter in sequence. The first conventional semiconductor device manufacturing method will be described with reference to FIG. 13. FIG. 13 is a

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cross-sectional view showing main steps of the first conventional semiconductor device manufacturing method, as viewed in a gate width direction thereof. Note that, in FIG. 13, “nMIS” shown on the left side indicates an n-type MIS formation region where an n-type MIS transistor is formed, and “pMIS” shown on the right side indicates a p-type MIS formation region where a p-type MIS transistor is formed.

Initially, an isolation region 101 is selectively formed in an upper portion of a semiconductor substrate 100. As a result, a first active region 100a surrounded by the isolation region 101 is formed in the n-type MIS formation region, and a second active region 100b surrounded by the isolation region 101 is formed in the p-type MIS formation region. Thereafter, a p-type well region 102a is formed in the n-type MIS formation region of the semiconductor substrate 100, and an n-type well region 102b is formed in the p-type MIS formation region of the semiconductor substrate 100.

Next, a gate insulating film formation film, a first metal film made of a gate electrode material for the n-type MIS transistor (hereinafter referred to as an “nMIS metal material”), a second metal film made of a gate electrode material for the p-type MIS transistor (hereinafter referred to as a “pMIS metal material”), and a silicon film are successively formed on the semiconductor substrate 100.

Thus, as shown in FIG. 13, a first patterning portion 107A is formed in which a gate insulating film formation film 103a, a first metal film 104a, a second metal film 105a, and a silicon film 106a are successively formed on the first active region 100a, and a second patterning portion 107B is formed in which a gate insulating film formation film 103b, a second metal film 105b, and a silicon film 106b are successively formed on the second active region 100b.

Thereafter, although not shown, by dry etching using as a mask a resist having a gate pattern, which is formed on the silicon films 106a and 106b, the first patterning portion

107A is subjected to patterning to form a first gate insulating film made of the gate insulating film formation film 103a and a first gate electrode made of the first metal film 104a, the second metal film 105a and the silicon film 106a, while the second patterning portion 107B is subjected to patterning to form a second gate insulating film made of the gate insulating film formation film 103b and a second gate electrode made of the second metal film 105b and the silicon film 106b.

Here, a problem with the first conventional semiconductor device manufacturing method will be described. In the first conventional semiconductor device manufacturing method, as shown in FIG. 13, although the first and second patterning portions 107A and 107B have different structures (specifically, the first patterning portion 107A has a four-layer structure, and the second patterning portion 107B has a three-layer structure), the first and second patterning portions 107A and 107B are subjected to patterning in the same step, i.e., under the same etching condition, and therefore, the first and second gate electrodes cannot both be formed with high precision, which is a problem. For example, when an etching condition is set so that the second gate electrode can be formed with high precision, the first metal film 104a and the gate insulating film formation film 103a in the first patterning portion 107A are not etched and remain, and therefore, the first gate electrode cannot be formed with high precision. On the other hand, for example, when an etching condition is set so that the first gate electrode can be formed with high precision, the semiconductor substrate 100 and the isolation region 101 in the p-type MIS formation region are also etched, and therefore, the second gate electrode cannot be formed with high precision.

The second conventional semiconductor device manufacturing method and its problem will be described hereinafter in sequence. The second conventional semiconductor device manufacturing method will be described with reference to FIGS. 14A-14E. FIGS. 14A-14E are cross-sectional views showing main steps of the second conventional

semiconductor device manufacturing method in an order in which the steps are performed, as viewed in a gate width direction thereof. Note that, in FIGS. 14A-14E, “nMIS” shown on the left side indicates an n-type MIS formation region where an n-type MIS transistor is formed, and “pMIS” shown on the right side indicates a p-type MIS formation region where a p-type MIS transistor is formed.

Initially, an isolation region 201 is selectively formed in an upper portion of a semiconductor substrate 200. As a result, a first active region 200a surrounded by the isolation region 201 is formed in the n-type MIS formation region, and a second active region 200b surrounded by the isolation region 201 is formed in the p-type MIS formation region. Thereafter, a p-type well region 202a is formed in the n-type MIS formation region of the semiconductor substrate 200, and an n-type well region 202b is formed in the p-type MIS formation region of the semiconductor substrate 200.

Next, a first gate insulating film formation film made of a gate insulating film material for the n-type MIS transistor (hereinafter referred to as an “nMIS insulating material”), a first metal film made of an nMIS metal material, and a first mask film are successively formed on the semiconductor substrate 200. Thereafter, as shown in FIG. 14A, a resist mask 206 which covers the n-type MIS formation region is formed on the first mask film by photolithography.

Next, the first mask film is etched using the resist mask 206 as a mask to form a first mask film 205a, and thereafter, the resist mask 206 is removed. Thereafter, the first metal film 204 and the first gate insulating film formation film 203 are successively etched using the first mask film 205a as a mask.

Next, as shown in FIG. 14B, a second gate insulating film formation film 207 made of a gate insulating film material for the p-type MIS transistor (hereinafter referred to as a “pMIS insulating material”), a second metal film 208 made of a pMIS metal material, and a

second mask film 209 are successively formed on the semiconductor substrate 200. Thereafter, a resist mask 210 which covers the p-type MIS formation region is formed on the second mask film 209 by photolithography.

Next, as shown in FIG. 14C, the second mask film 209 is etched using the resist mask 210 as a mask to form a second mask film 209b, and thereafter, the resist mask 210 is removed. Thereafter, the second metal film 208 and the second gate insulating film formation film 207 are successively etched using the second mask film 209b as a mask.

Next, as shown in FIG. 14D, the first and second mask films 205a and 209b are removed, and thereafter, a silicon film 211 is formed on the first and second metal films 204 and 208.

Thus, as shown in FIG. 14D, a first patterning portion in which the first gate insulating film formation film 203, the first metal film 204 and the silicon film 211 are successively formed is formed on the first active region 200a, and a second patterning portion in which the second gate insulating film formation film 207, the second metal film 208 and the silicon film 211 are successively formed is formed on the second active region 200b.

Next, as shown in FIG. 14E, a resist (not shown) having a gate pattern is formed on the silicon film 211 by photolithography, and thereafter, etching is performed using the resist as a mask to subject the first patterning portion to patterning to form a first gate insulating film 203a, and a first gate electrode 212A including a first metal film 204a and a first silicon film 211a, and to subject the second patterning portion to patterning to form a second gate insulating film 207b, and a second gate electrode 212B including a second metal film 208b and a second silicon film 211b.

Here, a problem with the second conventional semiconductor device manufacturing method will be described with reference to FIG. 15. FIG. 15 is a plan view indicating the problem with the second conventional semiconductor device manufacturing method. Note

that line XIVe-XIVe shown in FIG. 15 is a line along which the cross-sectional view of FIG. 14E is taken.

If the resist mask 210 for covering the p-type MIS formation region is formed and deviated in the gate width direction, so that an end portion in the gate width direction of the resist mask 210 is located in the n-type MIS formation region as shown in FIG. 14B, a protruding residual portion r including a residual portion 205c of the first mask film 205a, a residual portion 207c of the second gate insulating film formation film 207, and a residual portion 208c of the second metal film 208, is formed on the isolation region 201 as shown in FIG. 14D.

If patterning is performed while the residual portion r is formed, a patterned residual portion rp extending in a gate length direction is left on the isolation region 201 as shown in FIG. 15 (note that the patterned residual portion rp includes a patterned residual portion 205cp, a patterned residual portion 207cp and a patterned residual portion 208cp as shown in FIG. 14E). In addition, a sidewall insulating film 211c made of the silicon film 211 is formed on side surfaces in the gate width direction of the patterned residual portion rp.

The patterned residual portion rp (or the sidewall insulating film 211c) electrically connects the first and second gate electrodes 212A and 212B to other first and second gate electrodes (not shown) adjacent in the gate length direction to the first and second gate electrodes 212A and 212B, and therefore, the first and second gate electrodes 212A and 212B do not function as a gate electrode. Thus, in the second conventional semiconductor device manufacturing method, the first and second gate electrodes 212A and 212B cannot be formed, which is a problem.

Note that a cause of this problem has been described using a specific example in which the resist mask 210 covering the p-type MIS formation region is deviated and formed in the n-type MIS formation region. However, even if the resist mask 210 is not deviated or

formed in the n-type MIS formation region, when the resist mask 206 covering the n-type MIS formation region is deviated and formed in the p-type MIS formation region, a problem similar to that described above arises. Specifically, if the resist mask 206 is deviated and formed in the p-type MIS formation region in the step of FIG. 14A, a protruding residual portion r is formed on the isolation region 201 as shown in FIG. 16.

Here, the aforementioned problem can be avoided by increasing a width in the gate width direction of the isolation region 201. Specifically, a matching margin (margin region) is previously provided for the isolation region 201 to increase the width in the gate width direction of the isolation region 201. As a result, even if the resist mask 206 is formed and deviated in the gate width direction when the resist mask 206 is formed in the step of FIG. 14A, an end portion in the gate width direction of the resist mask 206 can be located in the n-type MIS formation region rather than in the p-type MIS formation region. In addition, even if the resist mask 210 is formed and deviated in the gate width direction when the resist mask 210 is formed in the step of FIG. 14B, an end portion in the gate width direction of the resist mask 210 can be located in the p-type MIS formation region rather than in the n-type MIS formation region. However, in this case, the following problem arises. Specifically, a matching margin is required for the isolation region 201 both when the resist mask 206 is formed and when the resist mask 210 is formed. Therefore, the width in the gate width direction of the isolation region 201 cannot be reduced, which is a problem.

Moreover, in the second conventional semiconductor device manufacturing method, although the first and second patterning portions have different structures (specifically, the first and second patterning portions have the same silicon film 211, but have the different first and second gate insulating film formation films 203 and 207 and the different first and second metal films 204 and 208, respectively), i.e., have different etching characteristics, the first and second patterning portions are subjected to patterning under the same etching condition as

shown in FIG. 14D. Therefore, the first and second gate electrodes cannot both be formed with high precision, which is a problem.

Thus, the second conventional semiconductor device manufacturing method has the problem that the first and second gate electrodes can be formed, but not both with high precision, and in addition, the problem that the width in the gate width direction of the isolation region 201 cannot be reduced.

As described above, the first conventional semiconductor device manufacturing method has the problem that the first and second gate electrodes cannot both be formed with high precision. On the other hand, the second conventional semiconductor device manufacturing method has not only the problem that the first and second gate electrodes cannot both be formed with high precision, but also the problem that the width in the gate width direction of the isolation region cannot be reduced.

In view of the aforementioned problems, an object of the present disclosure is to provide a semiconductor device including n- and p-type MIS transistors having gate electrodes made of different metal materials, in which the gate electrodes of the n- and p-type MIS transistors are formed with high precision, and the width in the gate width direction of the isolation region is reduced.

To achieve the object, a semiconductor device according to the present disclosure includes a first MIS transistor and a second MIS transistor. The first MIS transistor includes a first gate insulating film formed on a first active region in a semiconductor substrate, a first gate electrode includes a second metal film formed on the first gate insulating film, and an insulating film formed, extending over side surfaces of the first gate electrode and upper surfaces of regions located in the first active region laterally outside the first gate electrode. The second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate, a second gate electrode including a first metal film

formed on the second gate insulating film and a conductive film formed on the first metal film, and the insulating film formed, extending over side surfaces of the second gate electrode and upper surfaces of regions located in the second active region laterally outside the second gate electrode. The first and second metal films are made of different metal materials. The
5 insulating film is not formed on any of upper surfaces of the first and second gate electrodes.

According to the semiconductor device of the present disclosure, the first and second gate electrodes can be formed with high precision. In addition, an isolation region having a reduced width in a gate width direction thereof can be achieved, whereby the semiconductor device can be further miniaturized.

10 In the semiconductor device of the present disclosure, the first metal film preferably has a thickness smaller than that of the second metal film.

In the semiconductor device of the present disclosure, the first and second metal films preferably have different work functions.

15 In the semiconductor device of the present disclosure, the insulating film preferably has a thickness smaller than that of the first gate electrode.

In the semiconductor device of the present disclosure, the conductive film is preferably made of the second metal film.

In the semiconductor device of the present disclosure, the conductive film is preferably made of a silicon film. The semiconductor device preferably further includes a
20 metal silicide film formed on the silicon film.

In the semiconductor device of the present disclosure, the first and second gate insulating films are preferably made of the same insulating material.

In the semiconductor device of the present disclosure, the first and second gate insulating films are preferably made of different insulating materials.

25 The semiconductor device of the present disclosure preferably further includes a

first inner sidewall having an L-shaped cross-section formed on each of side surfaces of the first gate electrode, and a second inner sidewall having an L-shaped cross-section formed on each of side surfaces of the second gate electrode. The insulating film is preferably formed above and in contact with the first and second inner sidewalls.

5 In the semiconductor device of the present disclosure, the insulating film is preferably a stress insulating film which causes first stress in a gate length direction of a channel region in the first active region.

 In this case, the stress insulating film can apply the first stress in the gate length direction of the channel region in the first active region, whereby the drive capability of the first MIS transistor can be improved.

10 In the semiconductor device of the present disclosure, the first MIS transistor is preferably an n-type MIS transistor. The insulating film is preferably made of a silicon nitride film. The first stress is preferably tensile stress.

 The semiconductor device of the present disclosure preferably further includes source/drain regions formed in the second active region laterally outside the second gate electrode. The source/drain regions are preferably formed in respective trenches provided in the second active region, and preferably include a silicon mixed crystal layer which causes second stress in a gate length direction of a channel region in the second active region.

 In this case, the silicon mixed crystal layer can apply the second stress in the gate length direction of the channel region in the second active region, whereby the drive capability of the second MIS transistor can be improved.

 In the semiconductor device of the present disclosure, the second MIS transistor is preferably a p-type MIS transistor. The silicon mixed crystal layer is preferably made of a SiGe layer. The second stress is preferably compressive stress.

25 In the semiconductor device of the present disclosure, the first and second gate

insulating films preferably include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.

To achieve the object, a semiconductor device manufacturing method according to the present disclosure is a method for manufacturing a semiconductor device including a first
5 MIS transistor formed on a first active region in a semiconductor substrate and a second MIS transistor formed on a second active region in the semiconductor substrate. The method includes the steps of (a) forming a first gate electrode formation portion having a first gate insulating film, a first metal film and a first silicon film on the first active region, and a second gate electrode formation portion having a second gate insulating film, a first metal
10 film and a second silicon film on the second active region, (b) after step (a), forming an insulating film on the semiconductor substrate, the insulating film covering the first and second gate electrode formation portions, (c) removing the insulating film formed on the first and second gate electrode formation portions to expose an upper surface of each of the first silicon film in the first gate electrode formation portion and the second silicon film in the
15 second gate electrode formation portion, (d) after step (c), successively removing the first silicon film and the first metal film in the first gate electrode formation portion to form a first recess surrounded by the insulating film on the first active region, and (e) forming a second metal film in the first recess. A first gate electrode of the first MIS transistor includes the second metal film. A second gate electrode of the second MIS transistor includes the first
20 metal film in the second gate electrode formation portion.

According to the semiconductor device manufacturing method of the present disclosure, after the first and second gate electrode formation portion are formed in the same step, the second metal film is formed in the first recess which has been formed by successively removing the first silicon film and the first metal film in the first gate electrode
25 formation portion, to form the first gate electrode including the second metal film. On the

other hand, the second gate electrode including the first metal film in the second gate electrode formation portion is formed. Therefore, when the first silicon film and the first metal film in the first gate electrode formation portion is replaced with the second metal film, a matching margin is required for the isolation region. On the other hand, when the first and
5 second gate electrode formation portions are formed, a matching margin is not required for the isolation region. Therefore, the number of steps in which a matching margin is required for the isolation region can be reduced, whereby a width in the gate width direction of the matching margin can be reduced, and therefore, a width in the gate width direction of the isolation region can be reduced. As a result, the semiconductor device can be further
10 miniaturized.

In addition, as the first and second gate electrode formation portions having the same structure (in other words, the first and second gate electrode formation portions having the same etching characteristic) are formed in the same step, the first and second gate electrode formation portions can be easily formed with high precision. As a result, the first
15 metal film and the first silicon film in the first gate electrode formation portion which has been formed with high precision can be replaced with the second metal film to form the first gate electrode including the second metal film. On the other hand, as the second gate electrode including the first metal film in the second gate electrode formation portion which has been formed with high precision can be formed. As a result, the first and second gate
20 electrodes can be formed with high precision.

In the semiconductor device manufacturing method of the present disclosure, step (d) preferably includes forming, on the first active region, the first recess from a bottom of which the first gate insulating film is exposed, and removing the second silicon film in the second gate electrode formation portion to form, on the second active region, a second recess
25 surrounded by the insulating film, the first metal film being exposed from a bottom of the

second recess. Step (e) preferably includes forming the second metal film on the first gate insulating film in the first recess, and forming the second metal film on the first metal film in the second recess. The second gate electrode preferably includes the first metal film in the second gate electrode formation portion and the second metal film formed on the first metal
5 film.

In this case, when the first metal film in the first gate electrode formation portion is removed, a matching margin is required for the isolation region. On the other hand, when the first and second gate electrode formation portions are formed, a matching margin is not required for the isolation region. Therefore, the number of steps in which a matching margin
10 is required for the isolation region can be suppressed to one.

In the semiconductor device manufacturing method of the present disclosure, step (d) preferably includes forming, on the first active region, the first recess from a bottom of which the first gate insulating film is exposed. Step (e) preferably includes forming the second metal film on the first gate insulating film in the first recess. The method preferably
15 further includes the step of (f) after step (e), forming a metal silicide film on the second silicon film. The second gate electrode preferably includes the first metal film and the second silicon film in the second gate electrode formation portion.

In this case, when the first silicon film and the first metal film in the first gate electrode formation portion are removed, a matching margin is required for the isolation
20 region. On the other hand, when the first and second gate electrode formation portions are formed, a matching margin is not required for the isolation region. Therefore, the number of steps in which a matching margin is required for the isolation region can be suppressed to one.

In the semiconductor device manufacturing method of the present disclosure, step
25 (d) preferably includes successively removing the first silicon film, the first metal film, and

the first gate insulating film in the first gate electrode formation portion, to form, on the first active region, the first recess from a bottom of which the first active region is exposed. Step (e) preferably includes forming a third gate insulating film in the first recess, and forming the second metal film on the third gate insulating film. The method preferably further includes the step of (f) after step (e), forming a metal silicide film on the second silicon film. The second gate electrode preferably includes the first metal film and the second silicon film in the second gate electrode formation portion.

In this case, when the first silicon film, the first metal film and the first gate insulating film in the first gate electrode formation portion are removed, a matching margin is required for the isolation region. On the other hand, when the first and second gate electrode formation portions are formed, a matching margin is not required for the isolation region. Therefore, the number of steps in which a matching margin is required for the isolation region can be suppressed to one.

The semiconductor device manufacturing method of the present disclosure preferably further includes the step of (g) after step (a) and before step (b), forming a first inner sidewall having an L-shaped cross-section on each of side surfaces of the first gate electrode formation portion, and a second inner sidewall having an L-shaped cross-section on each of side surfaces of the second gate electrode formation portion. In step (b), the insulating film is preferably formed above and in contact with the first and second inner sidewalls.

The semiconductor device manufacturing method of the present disclosure preferably further includes the steps of (h) after step (a) and before step (b), forming trenches in the second active region laterally outside the second gate electrode formation portion, and (i) forming, in the trenches, a silicon mixed crystal layer which causes stress in a gate length direction of a channel region in the second active region.

According to the semiconductor device of the present disclosure and the manufacture method of the semiconductor device, the first and second gate electrode formation portions are formed in the same step, and thereafter, the second metal film is formed in the first recess which has been formed by successively removing the first silicon film and the first metal film in the first gate electrode formation portion, to form the first gate electrode including the second metal film. On the other hand, the second gate electrode including the first metal film in the second gate electrode formation portion is formed. Therefore, when the first silicon film and the first metal film in the first gate electrode formation portion are replaced with the second metal film, a matching margin is required for the isolation region. On the other hand, when the first and second gate electrode formation portions are formed, a matching margin is not required for the isolation region. Therefore, the number of steps in which a matching margin is required for the isolation region can be reduced, whereby a width in the gate width direction of the matching margin can be reduced, and therefore, a width in the gate width direction of the isolation region can be reduced. As a result, the semiconductor device can be further miniaturized.

In addition, as the first and second gate electrode formation portions having the same structure are formed in the same step, the first and second gate electrode formation portions can be easily formed with high precision. As a result, the first gate electrode including the second metal film can be formed by replacing the first metal film and the first silicon film in the first gate electrode formation portion, which has been formed with high precision, with the second metal film. On the other hand, the second gate electrode including the first metal film in the second gate electrode formation portion, which has been formed with high precision, can be formed. As a result, the first and second gate electrodes can be formed with high precision.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A-1D are cross-sectional views showing main steps of a method for manufacturing a semiconductor device according to a first embodiment of the present disclosure in an order in which the steps are performed, as viewed in a gate length direction thereof.

FIGS. 2A-2D are cross-sectional views showing main steps of the manufacture method of the semiconductor device of the first embodiment of the present disclosure in an order in which the steps are performed, as viewed in a gate length direction thereof.

FIGS. 3A-3D are cross-sectional views showing main steps of the manufacture method of the semiconductor device of the first embodiment of the present disclosure in an order in which the steps are performed, as viewed in a gate length direction thereof.

FIGS. 4A-4C are cross-sectional views showing main steps of the manufacture method of the semiconductor device of the first embodiment of the present disclosure in an order in which the steps are performed, as viewed in a gate length direction thereof.

FIGS. 5A-5C are cross-sectional views showing main steps of the manufacture method of the semiconductor device of the first embodiment of the present disclosure in an order in which the steps are performed, as viewed in a gate length direction thereof.

FIGS. 6A and 6B are diagrams showing a structure of the semiconductor device of the first embodiment of the present disclosure.

FIGS. 7A-7C are cross-sectional views showing main steps of a method for manufacturing a semiconductor device according to a second embodiment of the present disclosure in an order in which the steps are performed, as viewed in a gate length direction thereof.

FIGS. 8A-8C are cross-sectional views showing main steps of the manufacture method of the semiconductor device of the second embodiment of the present disclosure in an

order in which the steps are performed, as viewed in a gate length direction thereof.

FIG. 9 is a cross-sectional view showing a structure of the semiconductor device of the second embodiment of the present disclosure, as viewed in a gate width direction thereof.

FIGS. 10A-10C are cross-sectional views showing main steps of a method for manufacturing a semiconductor device according to a variation of the second embodiment of the present disclosure in an order in which the steps are performed, as viewed in a gate length direction thereof.

FIGS. 11A-11C are cross-sectional views showing main steps of the manufacture method of the semiconductor device of the variation of the second embodiment of the present disclosure in an order in which the steps are performed, as viewed in a gate length direction thereof.

FIG. 12 is a cross-sectional view showing a structure of the semiconductor device of the variation of the second embodiment of the present disclosure, as viewed in a gate width direction thereof.

FIG. 13 is a cross-sectional view showing main steps of a first conventional semiconductor device manufacturing method, as viewed in a gate width direction thereof.

FIGS. 14A-14E are cross-sectional views showing main steps of a second conventional semiconductor device manufacturing method in an order in which the steps are performed, as viewed in a gate width direction thereof.

FIG. 15 is a plan view indicating a problem with the second conventional semiconductor device manufacturing method.

FIG. 16 is a cross-sectional view indicating the problem with the second conventional semiconductor device manufacturing method, as viewed in a gate width direction thereof.

DETAILED DESCRIPTION

Embodiments of the present disclosure will be described hereinafter with reference to the accompanying drawings.

(First Embodiment)

5 A semiconductor device according to a first embodiment of the present disclosure and a method for manufacturing the semiconductor device will be described with reference to the drawings.

The method for manufacturing the semiconductor device of the first embodiment of the present disclosure will be described hereinafter with reference to FIGS. 1A-1D, FIGS.
10 2A-2D, FIGS. 3A-3D, FIGS. 4A-4C, and FIGS. 5A-5C. FIGS. 1A-5C are cross-sectional views showing main steps of the manufacture method of the semiconductor device of the first embodiment of the present disclosure in an order in which the steps are performed, as viewed in a gate length direction thereof. Note that, in FIGS. 1A-5C, “nMIS” shown on the left side indicates an n-type MIS formation region where an n-type MIS transistor is formed, and
15 “pMIS” shown on the right side indicates a p-type MIS formation region where a p-type MIS transistor is formed.

Initially, as shown in FIG. 1A, an isolation region 11 which is a trench filled with an insulating film is selectively formed in an upper portion of a semiconductor substrate 10 made of, for example, p-type silicon by, for example, Shallow Trench Isolation (STI). As a
20 result, a first active region 10a made of the semiconductor substrate 10 surrounded by the isolation region 11 is formed in the n-type MIS formation region, and a second active region 10b made of the semiconductor substrate 10 surrounded by the isolation region 11 is formed in the p-type MIS formation region. Thereafter, a p-type impurity, such as B (boron) or the like, is implanted into the n-type MIS formation region of the semiconductor substrate 10 by
25 lithography and ion implantation, and an n-type impurity, such as P (phosphorus) or the like,

is implanted into the p-type MIS formation region of the semiconductor substrate 10 by lithography and ion implantation. Thereafter, the semiconductor substrate 10 is subjected to, for example, a thermal treatment at 850°C for 30 sec, to form a p-type well region 12a in the n-type MIS formation region of the semiconductor substrate 10, and the n-type well region
5 12b in the p-type MIS formation region of the semiconductor substrate 10.

Next, as shown in FIG. 1B, a surface of the semiconductor substrate 10 is cleaned by, for example, a diluted hydrofluoric acid treatment, and thereafter, an underlying film (not shown) made of a silicon oxide film having a thickness of about 0.8 to 1 nm is formed on the first active region 10a and the second active region 10b by, for example, In-Situ Steam
10 Generation (ISSG) oxidation. Thereafter, a gate insulating film formation film 13 made of, for example, a high-k film having a thickness of 2 nm is deposited on the underlying film by, for example, Metal Organic Chemical Vapor Deposition (MOCVD). Here, the gate insulating film formation film 13 desirably includes a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.

Thereafter, a first metal film 14 made of, for example, titanium nitride (TiN) is deposited by, for example, CVD (Chemical Vapor Deposition), ALD (Atomic Layer Deposition), sputtering or the like. Here, the first metal film 14 is desirably made of a metal material or a metal compound material (hereinafter referred to as a “pMIS metal material”) which is optimized for the p-type MIS transistor, and desirably has a work function of 4.6 eV
20 or more and 5.15 eV or less. Examples of the first metal film 14 include, in addition to a TiN film, metals such as titanium (Ti), ruthenium (Ru), platinum (Pt), tungsten (W) and the like, nitrides containing at least one metal of Ti, Ru, Pt and W, carbon nitride, silicon nitride, and the like. Thereafter, a silicon film 15 made of, for example, a polysilicon film having a thickness of 100 nm is deposited on the first metal film 14 by, for example, CVD, and
25 thereafter, a protective film 16 made of, for example, a silicon oxide film having a thickness

of 30 nm is formed on the silicon film 15 by, for example, CVD.

Next, as shown in FIG. 1C, a resist (not shown) having a gate pattern is formed on the protective film 16 by photolithography. Thereafter, the protective film 16, the silicon film 15, the first metal film 14 and the gate insulating film formation film 13 are successively
5 subjected to patterning by dry etching using the resist as a mask. As a result, a first gate insulating film 13a, a first metal film 14a, a first silicon film 15a and a first protective film 16a are successively formed on the first active region 10a, and a second gate insulating film 13b, a first metal film 14b, a second silicon film 15b and a second protective film 16b are successively formed on the second active region 10b.

10 Thus, a first gate electrode formation portion 14A having the first gate insulating film 13a, the first metal film 14a and the first silicon film 15a is formed on the first active region 10a, and a second gate electrode formation portion 14B having the second gate insulating film 13b, the first metal film 14b and the second silicon film 15b is formed on the second active region 10b.

15 Next, as shown in FIG. 1D, an insulating film made of, for example, a silicon oxide film having a thickness of 10 nm, which is to become an offset spacer, is deposited on an entire surface of the semiconductor substrate 10 by, for example, CVD, and thereafter, the offset spacer insulating film is subjected to anisotropic etching. As a result, a first offset spacer 17a is formed on each of side surfaces of the first gate electrode formation portion 14A,
20 and a second offset spacer 17b is formed on each of side surfaces of the second gate electrode formation portion 14B.

Thereafter, a resist (not shown) which does not cover the n-type MIS formation region and covers the p-type MIS formation region is formed on the semiconductor substrate 10, and thereafter, an n-type impurity, such as As (arsenic) or the like, is implanted into the
25 first active region 10a using the first gate electrode formation portion 14A as a mask, to form

n-type source/drain regions (LDD regions or extension regions) 18a having a relatively shallow junction depth in the first active region 10a adjacent to the channel region below the first gate electrode formation portion 14A and extending laterally away from it (or referred to as “in the first active region 10a laterally outside the first gate electrode formation portion 14A”), in a self-alignment manner. On the other hand, a resist (not shown) which covers the n-type MIS formation region and does not cover the p-type MIS formation region is formed on the semiconductor substrate 10, and thereafter, a p-type impurity, such as BF₂ or the like, is implanted into the second active region 10b using the second gate electrode formation portion 14B as a mask, to form p-type source/drain regions (LDD regions or extension regions) 18b having a relatively shallow junction depth in the second active region 10b adjacent to the channel region below the second gate electrode formation portion 14B and extending laterally away from it (or referred to as “in the second active region 10b laterally outside the second gate electrode formation portion 14B”), in a self-alignment manner.

Next, as shown in FIG. 2A, a first insulating film made of, for example, a silicon oxide film having a thickness of 10 nm and a second insulating film made of, for example, a silicon nitride film having a thickness of 30 nm are successively deposited on an entire surface of the semiconductor substrate 10 by, for example, CVD, and thereafter, the first and second insulating films are subjected to anisotropic etching. As a result, a first sidewall 20A including a first inner sidewall 19a made of the first insulating film having an L-shaped cross-section and a first outer sidewall 20a made of the second insulating film formed on the first inner sidewall 19a, is formed on each of side surfaces of the first gate electrode formation portion 14A with the first offset spacer 17a being interposed therebetween, and a second sidewall 20B including a second inner sidewall 19b made of the first insulating film having an L-shaped cross-section and a second outer sidewall 20b made of the second insulating film formed on the second inner sidewall 19b, is formed on each of side surfaces of the second

gate electrode formation portion 14B with the second offset spacer 17b being interposed therebetween.

Next, as shown in FIG. 2B, a surface protective film 21 made of, for example, a silicon oxide film having a thickness of 10 nm is deposited on an entire surface of the semiconductor substrate 10 by, for example, CVD.

Next, as shown in FIG. 2C, a resist mask 22 which covers the n-type MIS formation region and does not cover the p-type MIS formation region is formed on the surface protective film 21, and thereafter, the surface protective film 21 formed in the p-type MIS formation region is removed, leaving the surface protective film 21a in the n-type MIS formation region, by anisotropic dry etching having a selectivity ratio with respect to the second outer sidewalls 20b (silicon nitride film). As a result, surfaces of regions (i.e., source and drain formation regions) in the second active region 10b laterally outside the second sidewall 20B, are exposed.

Next, as shown in FIG. 2D, the resist mask 22 is removed, and thereafter, the second active region 10b whose surface is exposed is etched using dry etching having a selectivity ratio with respect to the surface protective film 21a (silicon oxide film), the second protective film 16b (silicon oxide film), the second offset spacer 17b (silicon oxide film), the second inner sidewall 19b (silicon oxide film) and the second outer sidewall 20b (silicon nitride film), or using a successive combination of dry etching and wet etching having a selectivity ratio with respect to these films. As a result, trenches 23 having a depth of, for example, 60 nm is formed in regions (i.e., source and drain formation regions) in the second active region 10b laterally outside the second sidewall 20B. In this case, as a surface of the first active region 10a is covered with the surface protective film 21a, the first active region 10a is not etched. Also, as an upper surface the first silicon film 15a is covered with the first protective film 16a and the surface protective film 21a successively, and an upper surface of

the second silicon film 15b is covered with the second protective film 16b, none of the first and second silicon films 15a and 15b is etched.

Next, as shown in FIG. 3A, etching residues, natural oxide film and the like in the trench 23 are removed by, for example, a hydrofluoric acid treatment, and thereafter, a silicon mixed crystal layer 24 made of a p-type SiGe layer is epitaxially grown so that the trench 23 is filled with the silicon mixed crystal layer 24, by, for example, CVD with a supply of, for example, silane gas (SiH_4) and germane gas (GeH_4) along with p-type dopant gas, such as diborane gas (B_2H_6) or the like, at a temperature of, for example, 650 to 700°C. In this case, as the surface of the first active region 10a is covered with the surface protective film 21a, a SiGe layer is not epitaxially grown on the first active region 10a. Also, as the upper surface of the first silicon film 15a is covered with the first protective film 16a and the surface protective film 21a successively, and the upper surface of the second silicon film 15b is covered with the second protective film 16b, a SiGe layer is not epitaxially grown on any of the first and second silicon films 15a and 15b.

Thereafter, the surface protective film 21a formed in the n-type MIS formation region is removed by dry etching having a selectivity ratio with respect to the semiconductor substrate 10 and the first outer sidewall 20a (silicon nitride film) or using a successive combination of dry etching and wet etching with respect to these films, whereby surfaces of regions (i.e., source and drain formation regions) in the first active region 10a laterally outside the first sidewall 20A, are exposed.

Thus, by successively performing the steps of FIGS. 2B-3A, the silicon mixed crystal layer 24 which causes compressive stress in the gate length direction of the channel region in the second active region 10b is formed in the trenches 23 formed in the second active region 10b laterally outside the second sidewall 20B.

Next, as shown in FIG. 3B, an n-type impurity, such as As (arsenic) or the like, is

implanted into the first active region 10a by lithography and ion implantation using the first gate electrode formation portion 14A, the first offset spacer 17a and the first sidewall 20A as a mask, to form n-type source/drain regions 25a having a deeper junction depth than that of the shallow n-type source/drain regions 18a (i.e., having a relatively deep junction depth), in the first active region 10a laterally outside the first sidewall 20A, in a self-alignment manner. On the other hand, a p-type impurity, such as B (boron) or the like, is implanted into the second active region 10b using the second gate electrode formation portion 14B, the second offset spacer 17b and the second sidewall 20B as a mask, to form p-type source/drain regions 25b having a deeper junction depth than that of the shallow p-type source/drain regions 18b (i.e., having a relatively deep junction depth), in the second active region 10b laterally outside the second sidewall 20B, in a self-alignment manner. Thereafter, the impurities contained in the deep n-type source/drain regions 25a and the deep p-type source/drain regions 25b are activated by a thermal treatment.

Thus, the deep p-type source/drain regions 25b include the silicon mixed crystal layer 24 formed in the trenches 23 provided in the second active region 10b.

Next, natural oxide film (not shown) formed on surfaces of the deep n-type source/drain regions 25a and the deep p-type source/drain regions 25b is removed, and thereafter, a metal film (not shown) made of, for example, nickel having a thickness of 10 nm is deposited on an entire surface of the semiconductor substrate 10 by sputtering. Thereafter, Si in the deep n-type source/drain regions 25a and the deep p-type source/drain regions 25b and Ni in the metal film are caused to react with each other by, for example, a first Rapid Thermal Annealing (RTA) treatment in nitrogen atmosphere at 320°C, thereby forming first and second metal silicide films 26a and 26b made of nickel silicide in upper portions of the deep n-type source/drain regions 25a and the deep p-type source/drain regions 25b.

Thereafter, the semiconductor substrate 10 is immersed in an etchant which is a

mixture solution of sulfuric acid and hydrogen peroxide in water, to remove unreacted metal film remaining on the isolation region 11, the first and second offset spacers 17a and 17b, the first and second sidewalls 20A and 20B and the like, followed by a second RTA treatment at a higher temperature (e.g., 550°C) than that in the first RTA treatment, thereby stabilizing the silicide composition ratio of the first and second metal silicide films 26a and 26b.

Next, as shown in FIG. 3C, the first outer sidewall 20a (silicon nitride film) and the second outer sidewall 20b (silicon nitride film) are removed by, for example, dry etching having a selectivity ratio with respect to the first and second inner sidewalls 19a and 19b (silicon oxide film).

Next, as shown in FIG. 3D, an insulating film 27 made of, for example a silicon nitride film having a thickness of 50 nm is deposited on an entire surface of the semiconductor substrate 10 by, for example, plasma CVD.

Thus, the insulating film 27 is formed, covering the first gate electrode formation portion 14A on a surface of which the first protective film 16a is formed, and the second gate electrode formation portion 14B on a surface of which the second protective film 16b is formed. Thereafter, the insulating film 27 is formed above and in contact with the first inner sidewall 19a having an L-shaped cross-section from which the first outer sidewall 20a is removed and the second inner sidewall 19b having an L-shaped cross-section from which the second outer sidewall 20b is removed.

Thereafter, a first inter-layer insulating film 28 made of a silicon oxide film is deposited on the insulating film 27 by, for example, CVD, and thereafter, the first inter-layer insulating film 28 is removed by polishing while planarizing a surface of the first inter-layer insulating film 28 by, for example, Chemical Mechanical Polishing (CMP), until an upper surface of the insulating film 27 formed on the first and second protective films 16a and 16b is exposed.

Next, as shown in FIG. 4A, the first and second protective films (silicon oxide films) 16a and 16b and the insulating film (silicon nitride film) 27 formed on the first and second gate electrode formation portions 14A and 14B are removed by dry etching or wet etching having a selectivity ratio with respect to the first and second silicon films (polysilicon films) 15a and 15b, thereby exposing upper surfaces of the first silicon film 15a in the first gate electrode formation portion 14A and the second silicon film 15b in the second gate electrode formation portion 14B. In this case, the first and second offset spacers 17a and 17b, the first and second inner sidewalls 19a and 19b, the insulating film 27, and the first inter-layer insulating film 28 formed laterally outside the first and second gate electrode formation portions 14A and 14B are removed until a height of upper surfaces thereof becomes the same as or similar to a height of upper surfaces of the first and second silicon films 15a and 15b.

Thus, the insulating film 27 is formed, extending over side surfaces of the first and second gate electrode formation portions 14A and 14B and upper surfaces of regions located in the first and second active regions 10a and 10b laterally outside the first and second gate electrode formation portions 14A and 14B, and the insulating film 27 is not formed on any of upper surfaces of the first and second gate electrode formation portions 14A and 14B.

Next, as shown in FIG. 4B, the first silicon film 15a in the first gate electrode formation portion 14A and the second silicon film 15b in the second gate electrode formation portion 14B are removed by dry etching or wet etching having a selectivity ratio with respect to the first metal films (TiN films) 14a and 14b, the first and second offset spacers 17a and 17b, the first and second inner sidewalls 19a and 19b, the insulating film 27, and the first inter-layer insulating film 28.

Next, as shown in FIG. 4C, a resist mask 29 which does not cover the n-type MIS formation region and covers the p-type MIS formation region is formed on the semiconductor

substrate 10, and thereafter, the first metal film 14a in the first gate electrode formation portion 14A is removed by wet etching having a selectivity ratio with respect to the first gate insulating film 13a, the first offset spacer 17a, the first inner sidewall 19a, the insulating film 27, and the first inter-layer insulating film 28.

5 Thus, by successively performing the steps of FIGS. 4B and 4C, the first silicon film 15a and the first metal film 14a in the first gate electrode formation portion 14A are successively removed to form, on the first active region 10a, a first recess Ca surrounded by the insulating film 27 with the first offset spacer 17a and the first inner sidewall 19a being successively interposed therebetween. The first gate insulating film 13a is exposed from a
10 bottom of the first recess Ca. In addition, by performing the step of FIG. 4B, the second silicon film 15b in the second gate electrode formation portion 14B is removed to form, on the second active region 10b, a second recess Cb surrounded by the insulating film 27 with the second offset spacer 17b and the second inner sidewall 19b being successively interposed therebetween. The first metal film 14b is exposed from a bottom of the second recess Cb.

15 Next, as shown in FIG. 5A, the resist mask 29 is removed, and thereafter, a second metal film 30 made of, for example, tantalum nitride (TaN) is formed on the semiconductor substrate 10 by, for example, CVD, ALD, sputtering or the like, filling the first and second recesses Ca and Cb. Here, the second metal film 30 is desirably made of a metal material or a metal compound material optimized for the n-type MIS transistor (hereinafter referred to as
20 an “nMIS metal material”), and desirably has a work function of 4.05 eV or more and 4.6 eV or less. Specific examples of the second metal film 30 include, in addition to TaN, metals such as tantalum (Ta), hafnium (Hf) and the like, nitrides containing at least one of Ta and Hf, carbon nitride, silicon nitride, and the like.

 Next, as shown in FIG. 5B, the second metal film 30 is removed by, for example,
25 CMP or etchback until an upper surface of the insulating film 27 is exposed. As a result, a

second metal film 30a is formed on the first gate insulating film 13a in the first recess Ca, and a second metal film 30b is formed on the first metal film 14b in the second recess Cb.

Thus, a first gate electrode 30A made of the second metal film 30a is formed on the first active region 10a with the first gate insulating film 13a being interposed therebetween, and a second gate electrode 30B made of the first and second metal films 14b and 30b is formed on the second active region 10b with the second gate insulating film 13b being interposed therebetween.

Next, as shown in FIG. 5C, a second inter-layer insulating film 31 is deposited on the first inter-layer insulating film 28 by, for example, CVD, covering the first and second gate electrodes 30A and 30B, and thereafter, a surface of the second inter-layer insulating film 31 is planarized by, for example, CMP.

Thereafter, as in a method for manufacturing a semiconductor device having a typical MIS transistor, a resist (not shown) is formed on the second inter-layer insulating film 31, and thereafter, first and second contact holes 32a and 32b reaching upper surfaces of the first and second metal silicide films 26a and 26b are formed in the insulating film 27, the first inter-layer insulating film 28 and the second inter-layer insulating film 31 by dry etching using the resist as a mask. In this case, if a two-step etching method is used in which etching is temporarily stopped at the time that the insulating film 27 is exposed, the amount of over-etching of the first and second metal silicide films 26a and 26b can be reduced.

Thereafter, titanium and titanium nitride are successively deposited on bottom portions and sidewall portions of the first and second contact holes 32a and 32b by sputtering or CVD, to form a barrier metal film. Thereafter, a tungsten film is deposited on the second inter-layer insulating film 31 by CVD, filling the first and second contact holes 32a and 32b, and thereafter, the tungsten film formed outside the first and second contact holes 32a and 32b is removed by CMP. Thus, first and second contact plugs 33a and 33b are formed by filling

the first and second contact holes 32a and 32b with the tungsten film with the barrier metal film being interposed therebetween. Thereafter, a metal wire (not shown) which electrically connects the first and second contact plugs 33a and 33b is formed on the second inter-layer insulating film 31.

5 Thus, the semiconductor device of this embodiment, i.e., a semiconductor device including an n-type MIS transistor NTr having the first gate electrode 30A made of the second metal film 30a and a p-type MIS transistor PTr having the second gate electrode 30B made of the first metal film 14b and second metal film (conductive film) 30b, can be manufactured.

10 A structure of the semiconductor device of the first embodiment of the present disclosure will be described hereinafter with reference to FIGS. 6A and 6B. FIGS. 6A and 6B are diagrams showing the structure of the semiconductor device of the first embodiment of the present disclosure. Specifically, FIG. 6A is a plan view and FIG. 6B is a cross-sectional view as viewed in a gate width direction thereof, taken along line VIb-VIb of FIG. 6A. Note
15 that line Vcl-Vcl shown in FIG. 6A corresponds to a cross-section line in the left portion of FIG. 5C, and line Vcr-Vcr shown in FIG. 6A corresponds to a cross-section line in the right portion of FIG. 5C. Note that, in FIGS. 6A and 6B, “nMIS” shown on the left side indicates an n-type MIS formation region where an n-type MIS transistor is formed, and “pMIS” shown on the right side indicates a p-type MIS formation region where a p-type MIS transistor is
20 formed.

As shown in FIG. 6A, the first active region 10a surrounded by the isolation region is formed in the n-type MIS formation region, and the second active region 10b surrounded by the isolation region is formed in the p-type MIS formation region. The first gate electrode 30A is formed on the first active region 10a with the first gate insulating film being interposed
25 therebetween, and the second gate electrode 30B is formed on the second active region 10b

with the second gate insulating film being interposed therebetween. The insulating film 27 is formed on the side surfaces of the first and second gate electrodes 30A and 30B with the first and second offset spacers 17a and 17b and the first and second inner sidewalls 19a and 19b being successively interposed therebetween. Although the first inter-layer insulating film (see 28 in FIG. 5C) and the second inter-layer insulating film (see 31 in FIG. 5C) are not shown in FIG. 6A, the first inter-layer insulating film is actually formed on the insulating film 27. Also, the second inter-layer insulating film is actually formed on the first inter-layer insulating film, covering the first and second gate electrodes 30A and 30B.

As shown in FIG. 6B, the isolation region 11 formed by filling the trench with insulating film is formed in an upper portion of the semiconductor substrate 10, separating the n-type MIS formation region from the p-type MIS formation region. The p-type well region 12a is formed in the n-type MIS formation region of the semiconductor substrate 10, and the n-type well region 12b is formed in the p-type MIS formation region of the semiconductor substrate 10. The first gate electrode 30A made of the second metal film 30a is formed on the first active region 10a with the first gate insulating film 13a being interposed therebetween, and the second gate electrode 30B made of the first metal film 14b and the second metal film (conductive film) 30b formed on the first metal film 14b are formed on the second active region 10b with the second gate insulating film 13b being interposed therebetween. The second inter-layer insulating film 31 is formed on the semiconductor substrate 10, covering the first and second gate electrodes 30A and 30B.

Here, structures of the n-type MIS transistor and the p-type MIS transistor will be described with reference to FIG. 5C.

As shown in FIG. 5C, the n-type MIS transistor NTr includes the first active region 10a surrounded by the isolation region 11 in the semiconductor substrate 10, the first gate insulating film 13a formed on the first active region 10a, the first gate electrode 30A made of

the second metal film 30a formed on the first gate insulating film 13a, the first inner sidewalls 19a having an L-shaped cross-section formed on the side surfaces of the first gate electrode 30A with the first offset spacers 17a being interposed therebetween, the shallow n-type source/drain regions 18a formed in the first active region 10a laterally outside the first gate electrode 30A, the deep n-type source/drain region 25a formed in the first active region 10a laterally outside the first inner sidewalls 19a, the insulating film 27 formed extending over the side surfaces of the first gate electrode 30A and the upper surfaces of the regions located in the first active region 10a laterally outside the first gate electrodes 30A, and the first metal silicide film 26a formed in the upper portions of the deep n-type source/drain regions 25a.

As shown in FIG. 5C, the p-type MIS transistor PTr includes the second active region 10b surrounded by the isolation region 11 in the semiconductor substrate 10, the second gate insulating film 13b formed on the second active region 10b, the second gate electrode 30B made of the first metal film 14b and second metal film (conductive film) 30b formed on the second gate insulating film 13b, the second inner sidewalls 19b having an L-shaped cross-section formed on the side surfaces of the second gate electrode 30B with the second offset spacer 17b being interposed therebetween, the shallow p-type source/drain regions 18b formed in the second active region 10b laterally outside the first gate electrode 30B, the deep p-type source/drain regions 25b including the silicon mixed crystal layer 24 formed in the second active region 10b laterally outside the second inner sidewalls 19b, the insulating film 27 formed extending over the side surfaces of the second gate electrode 30B and the upper surfaces of the regions located in the second active region 10b laterally outside the second gate electrode 30B, and the second metal silicide film 26b formed in the upper portions of the deep p-type source/drain regions 25b.

The second metal film 30a included in the first gate electrode 30A is made of a metal material (or a metal compound material) having a work function of 4.05 eV or more

and 4.6 eV or less, and the first metal film 14b included in the second gate electrode 30B is made of a metal material (or a metal compound material) having a work function of 4.6 eV or more and 5.15 eV or less. Thus, the second metal film 30a and the first metal film 14b are made of different metal materials (or metal compound materials) having different work functions.

Also, the first and second gate electrodes 30A and 30B have the upper surfaces having the same height. The first gate electrode 30A is made of the second metal film 30a, and the second gate electrode 30B is made of the first metal film 14b and the second metal film 30b. Therefore, a thickness of the second metal film 30a is larger than a thickness of each of the first metal film 14b and the second metal film (conductive film) 30b.

The insulating film 27 is formed on the side surfaces of the first and second gate electrodes 30A and 30B and the upper regions located in the first and second active regions 10a and 10b laterally outside the first and second gate electrodes 30A and 30B, and the insulating film 27 is not formed on any of the upper surfaces of the first and second gate electrodes 30A and 30B. Also, a thickness of the insulating film 27 is smaller than a thickness of each of the first and second gate electrodes 30A and 30B.

The first and second gate insulating films 13a and 13b are formed in the same step and are made of the same insulating material.

According to this embodiment, after the first and second gate electrode formation portions 14A and 14B (see FIG. 1C) are formed in the same step, the second metal film 30a is formed in the first recess Ca (see FIG. 4C) which has been formed by successively removing the first silicon film 15a and the first metal film 14a in the first gate electrode formation portion 14A, to form the first gate electrode 30A (see FIG. 5B) made of the second metal film 30a. On the other hand, the second metal film 30b is formed in the second recess Cb (see FIG. 4B) which has been formed by removing the second silicon film 15b in the second gate

electrode formation portion 14B, to form the second gate electrode 30B (see FIG. 5B) made of the first and second metal films 14b and 30b. Therefore, when the first metal film 14a in the first gate electrode formation portion 14A is removed, the resist mask 29 which does not cover one of the n-type MIS formation region and the p-type MIS formation region and
5 covers the other is formed as shown in FIG. 4C, and therefore, a matching margin is required for the isolation region 11. On the other hand, when the first and second gate electrode formation portions 14A and 14B are formed, a matching margin is not required for the isolation region 11. Therefore, the number of steps in which a matching margin is required for the isolation region 11 (hereinafter referred to as “matching margin requiring steps”) can
10 be suppressed to one, and therefore, a width in the gate width direction of the matching margin can be narrowed to reduce a width in the gate width direction of the isolation region 11 (see Wnp in FIG. 6B). Thus, the semiconductor device can be further miniaturized.

In contrast to this, in the second conventional semiconductor device manufacturing method, a matching margin is required for the isolation region 201 when the resist mask 206
15 is formed in the step of FIG. 14A, and a matching margin is required for the isolation region 201 when the resist mask 210 is formed in the step of FIG. 14B, i.e., there are two matching margin requiring steps. Therefore, as described above, the width in the gate width direction of the isolation region 201 cannot be reduced.

In addition, as shown in FIG. 1C, the same silicon film 15, the same first metal film
20 14, and the same gate insulating film formation film 13 are successively subjected to patterning in the same step to form the first and second gate electrode formation portions 14A and 14B, whereby the first and second gate electrode formation portions 14A and 14B can be easily formed with high precision. As a result, the first metal film 14a and the first silicon film 15a in the first gate electrode formation portion 14A which have been formed with high
25 precision are replaced with the second metal film 30a to form the first gate electrode 30A

made of the second metal film 30a, and the second silicon film 15b in the second gate electrode formation portion 14B which has been formed with precision is replaced with the second metal film 30b to form the second gate electrode 30B made of the first and second metal films 14b and 30b. Thus, the first and second gate electrodes 30A and 30B can be
5 formed with high precision.

In contrast to this, in the first conventional semiconductor device manufacturing method, as shown in FIG. 13, the first and second patterning portions 107A and 107B, which have different structures, are subjected to patterning in the same step. Therefore, as described above, the first and second gate electrodes cannot both be formed with high
10 precision. On the other hand, also in the second conventional semiconductor device manufacturing method, as shown in FIG. 14D, the first and second patterning portions, which have different structures, are subjected to patterning in the same step. Therefore, as described above, the first and second gate electrodes cannot both be formed with high precision.

Moreover, the deep p-type source/drain region 25b includes the silicon mixed crystal layer 24 which causes compressive stress in the gate length direction of the channel region in the second active region 10b, and therefore, compressive stress can be applied in the gate length direction of the channel region in the second active region 10b, whereby the drive capability of the p-type MIS transistor can be improved.
15

Note that, in the first embodiment, in order to improve the drive capability of the p-type MIS transistor, the steps of FIGS. 2B-3A are successively performed after the formation of the first and second sidewalls 20A and 20B (see FIG. 2A) and before the formation of the deep n- and p-type source/drain regions 25a and 25b (see FIG. 3B), thereby forming the silicon mixed crystal layer 24 made of, for example, a p-type SiGe layer in the
20 trenches 23 formed in the second active region 10b laterally outside the second sidewalls 20B.
25

The present disclosure is not limited to this specific example.

For example, as shown in FIG. 2A, after the formation of the first and second sidewalls 20A and 20B, the deep n- and p-type source/drain regions 25a and 25b may be formed as shown in FIG. 3B, without successively performing the steps of FIGS. 2B-3A, i.e.,
5 without forming the silicon mixed crystal layer 24.

Also, for example, a silicon mixed crystal layer (e.g., an n-type SiC layer) which causes tensile stress in the gate length direction of the channel region in the first active region 10a may be formed in the trenches formed in the first active region 10a laterally outside the first sidewalls 20A, after the formation of the first and second sidewalls 20A and 20B (see
10 FIG. 2A) and before the formation of the deep n- and p-type source/drain regions 25a and 25b (see FIG. 3B). In this case, the drive capability of the n-type MIS transistor can be improved rather than that of the p-type MIS transistor.

(Second Embodiment)

A semiconductor device according to a second embodiment of the present
15 disclosure and a method for manufacturing the semiconductor device will be described with reference to the drawings. Note that differences between the semiconductor device of the second embodiment and the manufacture method of the semiconductor device, and the semiconductor device of the first embodiment and the manufacture method of the semiconductor device will be mainly described, and their common points will not be
20 described unless necessary.

The manufacture method of the semiconductor device of the second embodiment of the present disclosure will be described hereinafter with reference to FIGS. 7A-7C and FIGS. 8A-8C. FIGS. 7A-8C are cross-sectional views showing main steps of the manufacture method of the semiconductor device of the second embodiment of the present disclosure in an
25 order in which the steps are performed, as viewed in a gate length direction thereof. Note

that, in FIGS. 7A-8C, the same components as those of the first embodiment are indicated by the same reference symbols as those shown in FIGS. 1A-5C of the first embodiment. Also, in FIGS. 7A-8C, “nMIS” shown on the left side indicates an n-type MIS formation region where an n-type MIS transistor is formed, and “pMIS” shown on the right side indicates a p-type MIS formation region where a p-type MIS transistor is formed.

Initially, the steps of FIGS. 1A-4A in the first embodiment are successively performed to obtain a structure shown in FIG. 7A (i.e., the same structure as that of FIG. 4A).

Next, as shown in FIG. 7B, a resist mask 29 which does not cover the n-type MIS formation region and covers the p-type MIS formation region is formed on the semiconductor substrate 10, and thereafter, the first silicon film 15a in the first gate electrode formation portion 14A is removed using dry etching or wet etching having a selectivity ratio with respect to the first metal film 14a, the first offset spacers 17a, the first inner sidewalls 19a, the insulating film 27, and the first inter-layer insulating film 28. Thereafter, the first metal film 14a in the first gate electrode formation portion 14A is removed using wet etching having a selectivity ratio with respect to the first gate insulating film 13a, the first offset spacers 17a, the first inner sidewalls 19a, the insulating film 27, and the first inter-layer insulating film 28.

Thus, the first silicon film 15a and the first metal film 14a in the first gate electrode formation portion 14A are successively removed to form, on the first active region 10a, a first recess Ca which is surrounded by the insulating film 27 with the first offset spacers 17a and the first inner sidewalls 19a being successively interposed therebetween. The first gate insulating film 13a is exposed from a bottom of the first recess Ca.

Next, as shown in FIG. 7C, the resist mask 29 is removed, and thereafter, a second metal film 30 made of, for example, TaN is formed on the semiconductor substrate 10 by, for example, CVD, ALD, sputtering or the like, filling the first recess Ca.

Next, as shown in FIG. 8A, the second metal film 30 is removed by, for example,

CMP or etchback until an upper surface of the insulating film 27 is exposed. As a result, a second metal film 30a is formed on the first gate insulating film 13a in the first recess Ca.

Thus, the first gate electrode 30A made of the second metal film 30a is formed on the first active region 10a with the first gate insulating film 13a being interposed therebetween, and the second gate electrode 30B made of the first metal film 14b and the second silicon film 15b is formed on the second active region 10b with the second gate insulating film 13b being interposed therebetween.

Next, as shown in FIG. 8B, natural oxide film (not shown) formed on a surface of the second silicon film 15b is removed, and thereafter, a metal film (not shown) made of, for example, nickel having a thickness of 10 nm is deposited on an entire surface of the semiconductor substrate 10 by, for example, sputtering. Thereafter, Si in the second silicon film 15b and Ni in the metal film are caused to react with each other by, for example, a first RTA treatment in nitrogen atmosphere at 320°C, to form a metal silicide film 34 made of nickel silicide in an upper portion of the second silicon film 15b.

Thereafter, the semiconductor substrate 10 is immersed in an etchant which is a mixture solution of sulfuric acid and hydrogen peroxide in water, to remove unreacted metal film remaining on the first inter-layer insulating film 28, the insulating film 27, the first and second inner sidewalls 19a and 19b, the first and second offset spacers 17a and 17b and the like, followed by a second RTA treatment at a higher temperature (e.g., 550°C) than that in the first RTA treatment, thereby stabilizing the silicide composition ratio of the metal silicide film 34.

Next, as shown in FIG. 8C, a second inter-layer insulating film 31 is deposited on the first inter-layer insulating film 28 by, for example, CVD, covering the first and second gate electrodes 30A and 30B, and thereafter, a surface of the second inter-layer insulating film 31 is planarized by, for example, CMP. Thereafter, as in a method for manufacturing a

semiconductor device having a typical MIS transistor, first and second contact plugs 33a and 33b which connect to the first and second metal silicide films 26a and 26b are formed in the first and second contact holes 32a and 32b in the insulating film 27, the first inter-layer insulating film 28 and the second inter-layer insulating film 31. Thereafter, a metal wire
5 (not shown) which electrically connects the first and second contact plugs 33a and 33b is formed on the second inter-layer insulating film 31.

Thus, the semiconductor device of this embodiment, i.e., a semiconductor device including the n-type MIS transistor NTr having the first gate electrode 30A made of the second metal film 30a and the p-type MIS transistor PTr having the second gate electrode
10 30B made of the first metal film 14b and the second silicon film (conductive film) 15b, can be manufactured.

Here, the manufacture methods of this embodiment and the first embodiment are different from each other in the following points.

In the first embodiment, as shown in FIG. 4B, the second metal film 30b is formed
15 in the second recess Cb which has been formed by removing the second silicon film 15b in the second gate electrode formation portion 14B, to form the second gate electrode 30B made of the first metal film 14b in the second gate electrode formation portion 14B, and the second metal film 30b.

In contrast to this, in this embodiment, the second silicon film 15b in the second
20 gate electrode formation portion 14B is not removed as is different from FIG. 4B in the first embodiment, and the second gate electrode 30B made of the first metal film 14b and the second silicon film 15b in the second gate electrode formation portion 14B is formed. In addition, after the formation of the second gate electrode 30B, the metal silicide film 34 is formed on the second silicon film 15b in the second gate electrode 30B as shown in FIG. 8B.

25 A structure of the semiconductor device of the second embodiment of the present

disclosure will be described hereinafter with reference to FIG. 9. FIG. 9 is a cross-sectional view showing the structure of semiconductor device of the second embodiment of the present disclosure, as viewed in a gate width direction thereof. Note that, in FIG. 9, the same components as those of the first embodiment are indicated by the same reference symbols as those of FIG. 6B in the first embodiment. Note that, in FIG. 9, “nMIS” shown on the left side indicates an n-type MIS formation region where an n-type MIS transistor is formed, and “pMIS” shown on the right side indicates a p-type MIS formation region where a p-type MIS transistor is formed.

As shown in FIG. 9, the first gate electrode 30A made of the second metal film 30a is formed on the first active region 10a with the first gate insulating film 13a being interposed therebetween, and the second gate electrode 30B made of the first metal film 14b and the second silicon film (conductive film) 15b formed on the first metal film 14b is formed on the second active region 10b with the second gate insulating film 13b being interposed therebetween. The metal silicide film 34 is formed on the second silicon film 15b.

Here, the structure of this embodiment is different from that of the first embodiment in the following points.

In this embodiment, the second gate electrode 30B is made of the first metal film 14b and the second silicon film 15b. Also, the metal silicide film 34 is formed on the second silicon film 15b. In contrast to this, in the first embodiment, the second gate electrode 30B is made of the first metal film 14b and the second metal film 30b.

Thus, the conductive film formed on the first metal film 14b in the second gate electrode 30B is the second silicon film 15b in this embodiment, and is the second metal film 30b in the first embodiment.

According to this embodiment, after the first and second gate electrode formation portions 14A and 14B (see FIG. 1C) are formed in the same step, the second metal film 30a is

formed in the first recess Ca (see FIG. 7B) which has been formed by successively removing the first silicon film 15a and the first metal film 14a in the first gate electrode formation portion 14A, thereby forming the first gate electrode 30A (see FIG. 8A) made of the second metal film 30a. On the other hand, the second gate electrode 30B made of the first meal film 14b and the second silicon film 15b in the second gate electrode formation portion 14B is formed. Therefore, when the first silicon film 15a and the first metal film 14a in the first gate electrode formation portion 14A are removed, a matching margin is required for the isolation region 11 so as to form the resist mask 29 which does not cover one of the n- and p-type MIS formation regions and covers the other as shown in FIG. 7B. On the other hand, when the first and second gate electrode formation portions 14A and 14B are formed, a matching margin is not required for the isolation region 11. Therefore, the number of matching margin requiring steps can be suppressed to one, and therefore, the width in the gate width direction of the isolation region 11 (see Wnp in FIG. 9) can be reduced, whereby the semiconductor device can be further miniaturized.

In addition, as shown in FIG. 1C, the same silicon film 15, the same first metal film 14, and the same gate insulating film formation film 13 are successively subjected to patterning in the same step, to form the first and second gate electrode formation portions 14A and 14B. Therefore, the first and second gate electrode formation portions 14A and 14B can be easily formed with high precision. As a result, the first metal film 14a and the first silicon film 15a in the first gate electrode formation portion 14A which have been formed with high precision are replaced with the second metal film 30a to form the first gate electrode 30A made of the second metal film 30a, and the second gate electrode 30B made of the first meal film 14b and the second silicon film 15b in the second gate electrode formation portion 14B which have been formed with high precision, can be formed. Therefore, the first and second gate electrodes 30A and 30B can be formed with high precision.

Moreover, as in the first embodiment, the deep p-type source/drain region 25b includes the silicon mixed crystal layer 24, and therefore, compressive stress can be applied in the gate length direction of the channel region in the second active region 10b, whereby the drive capability of the p-type MIS transistor can be improved.

5 (Variation of Second Embodiment)

A semiconductor device according to a variation of the second embodiment of the present disclosure and a method for manufacturing the semiconductor device will be described hereinafter with reference to the drawings. Note that differences between the semiconductor device of the variation of the second embodiment of the present disclosure and
10 a manufacture method of the semiconductor device and the semiconductor device of the second embodiment of the present disclosure and a manufacture method of the semiconductor device will be mainly described, and their common points will not be described unless necessary.

The manufacture method of the semiconductor device of the variation of the second
15 embodiment of the present disclosure will be described hereinafter with reference to FIGS. 10A-10C and 11A-11C. FIGS. 10A-11C are cross-sectional views showing main steps of the manufacture method of the semiconductor device of the variation of the second embodiment of the present disclosure in an order in which the steps are performed, as viewed in a gate length direction thereof. Note that, in FIGS. 10A-11C, the same components as
20 those of the second embodiment are indicated by the same reference symbols as those in FIGS. 7A-8C of the second embodiment. Note that, in FIGS. 10A-11C, “nMIS” shown on the left side indicates an n-type MIS formation region where an n-type MIS transistor is formed, and “pMIS” shown on the right side indicates a p-type MIS formation region where a p-type MIS transistor is formed.

25 Initially, the steps of FIGS. 1A-4A in the first embodiment are successively

performed to obtain the structure of FIG. 7A as in the second embodiment. Note that the gate insulating film formation film 13 of this variation desirably has a thickness optimized for the p-type MIS transistor and is desirably made of an insulating material optimized for the p-type MIS transistor.

5 Next, as shown in FIG. 10A, a resist mask 29 which does not cover the n-type MIS formation region and covers the p-type MIS formation region is formed on the semiconductor substrate 10, and thereafter, the first silicon film 15a in the first gate electrode formation portion 14A is removed using dry etching or wet etching having a selectivity ratio with respect to the first metal film 14a, the first offset spacers 17a, the first inner sidewalls 19a, the
10 insulating film 27, and the first inter-layer insulating film 28. Thereafter, the first metal film 14a in the first gate electrode formation portion 14A is removed using wet etching having a selectivity ratio with respect to the first gate insulating film 13a, the first offset spacers 17a, the first inner sidewalls 19a, the insulating film 27, and the first inter-layer insulating film 28. Thus, a step similar to that of FIG. 7B in the second embodiment is performed.

15 Thereafter, the first gate insulating film 13a in the first gate electrode formation portion 14A is removed using wet etching having a selectivity ratio with respect to the semiconductor substrate.

 Thus, the first silicon film 15a, the first metal film 14a, and the first gate insulating film 13a in the first gate electrode formation portion 14A are successively removed to form,
20 on the first active region 10a, a first recess Ca which is surrounded by the insulating film 27 with the first offset spacers 17a and the first inner sidewalls 19a being successively interposed therebetween. The first gate insulating film 13a is exposed from a bottom of the first recess Ca.

 Next, as shown in FIG. 10B, the resist mask 29 is removed, and thereafter, a
25 chemical oxide film (not shown) is formed on a surface of the semiconductor substrate 10 by,

for example, a Hydrochloric Acid/Hydrogen Peroxide/Water Mixture (HPM) treatment. Thereafter, a gate insulating film formation film 35 made of, for example, a high-k film having a thickness of 2 nm is deposited on the semiconductor substrate 10 by, for example, MOCVD, covering the inside of the first recess Ca. Here, the gate insulating film formation
5 film 35 desirably includes a high-k film made of a metal oxide having a relative dielectric constant of 10 or more. Moreover, the gate insulating film formation film 35 desirably has a thickness optimized for the n-type MIS transistor and is desirably made of an insulating material optimized for the n-type MIS transistor.

Thereafter, a second metal film 30 made of, for example, TaN is deposited on the
10 semiconductor substrate 10 by, for example, CVD, ALD, sputtering or the like, filling the first recess Ca with the gate insulating film formation film 35 being interposed therebetween.

Next, as shown in FIG. 10C, the second metal film 30 and the gate insulating film formation film 35 are removed by, for example, CMP or etchback until an upper surface of the insulating film 27 is exposed. As a result, a third gate insulating film 35a is formed in
15 the first recess Ca, and a second metal film 30a is formed on the third gate insulating film 35a. Here, the third gate insulating film 35a is formed, extending over an upper surface of the first active region 10a in the first recess Ca and side surfaces of the second metal film 30a. Therefore, although not shown in FIG. 10C which is a cross-sectional view in the gate length direction, the third gate insulating film 35a is formed and interposed between the second
20 metal film 30a, and the first metal film 14b and the second silicon film 15b, which are adjacent to each other in the gate width direction.

Next, as shown in FIG. 11A, an upper portion of the third gate insulating film 35a is removed by, for example, etching or a diluted hydrofluoric acid treatment having a selectivity ratio with respect to the second metal film 30a, thereby causing heights of upper ends of the
25 third gate insulating film 35a to be lower than a height of an upper surface of the second metal

film 30a, to form a groove R. Here, the groove R is formed along a periphery of the second metal film 30a, exposing side surfaces of the second metal film 30a. Therefore, although not shown in FIG. 11A which is a cross-sectional view in the gate length direction, the groove R is formed between the second metal film 30a and the second silicon film 15b, which are adjacent to each other in the gate width direction, and side surfaces in the gate width direction of the second metal film 30a and side surfaces in the gate width direction of the second silicon film 15b are exposed in the groove R.

Thus, by successively performing the steps of FIGS. 10B-11A, the third gate insulating film 35a is formed in the first recess Ca, and the second metal film 30a whose side surfaces are exposed in the groove R is formed on the third gate insulating film 35a.

Thus, the first gate electrode 30A made of the second metal film 30a is formed on the first active region 10a with the third gate insulating film 35a being interposed therebetween, and the second gate electrode 30B made of the first metal film 14b and the second silicon film 15b is formed on the second active region 10b with the second gate insulating film 13b being interposed therebetween.

Next, as shown in FIG. 11B, natural oxide film (not shown) formed on a surface of the second silicon film 15b is removed, and thereafter, a metal film (not shown) made of, for example, nickel having a thickness of 10 nm is deposited on an entire surface of the semiconductor substrate 10 by, for example, sputtering. Thereafter, Si in the second silicon film 15b and Ni in the metal film are caused to react with each other by, for example, a first RTA treatment in nitrogen atmosphere at 320°C, to form a metal silicide film 34 made of nickel silicide on the second silicon film 15b. In this case, the metal silicide film 34 of this variation is also formed in the groove R formed between the second metal film 30a and the second silicon film 15b due to expansion of its volume. Specifically, the metal silicide film 34 is formed above and in contact with side surfaces in the gate width direction of the second

metal film 30a and side surfaces in the gate width direction of the second silicon film 15b which are exposed in the groove R (see 34 in FIG. 12 described below). Therefore, the metal silicide film 34 can electrically connect the second metal film 30a and the second silicon film 15b.

5 Thereafter, the semiconductor substrate 10 is immersed in an etchant which is a mixture solution of sulfuric acid and hydrogen peroxide in water to remove unreacted metal film remaining on the first inter-layer insulating film 28, the insulating film 27, the first and second inner sidewalls 19a and 19b, the first and second offset spacers 17a and 17b and the like, followed by a second RTA treatment at a higher temperature (e.g., 550°C) than that in
10 the first RTA treatment, thereby stabilizing the silicide composition ratio of the metal silicide film 34.

Next, as shown in FIG. 11C, a second inter-layer insulating film 31 is deposited on the first inter-layer insulating film 28 by, for example, CVD, covering the first and second gate electrodes 30A and 30B, and thereafter, a surface of the second inter-layer insulating film
15 31 is planarized by, for example, CMP. Thereafter, as in a method for manufacturing a semiconductor device having a typical MIS transistor, first and second contact plugs 33a and 33b which connect to the first and second metal silicide films 26a and 26b are formed in the first and second contact holes 32a and 32b formed in the insulating film 27, the first inter-layer insulating film 28, and the second inter-layer insulating film 31. Thereafter, a
20 metal wire (not shown) which electrically connects to the first and second contact plugs 33a and 33b is formed on the second inter-layer insulating film 31. Thus, a step similar to that of FIG. 8C in the second embodiment is performed.

Thus, the semiconductor device of this embodiment, i.e., a semiconductor device including the n-type MIS transistor NTr having the first gate electrode 30A made of the
25 second metal film 30a and the p-type MIS transistor PTr having the second gate electrode

30B made of the first metal film 14b and the second silicon film (conductive film) 15b, can be manufactured.

Here, the manufacture method of this variation is different from that of the second embodiment in the following points.

5 In the second embodiment, the second metal film 30a is formed on the first gate insulating film 13a in the first recess Ca (see FIG. 7B) which has been formed by removing the first silicon film 15a and the first metal film 14a in the first gate electrode formation portion 14A.

10 In contrast to this, in this variation, the third gate insulating film 35a is formed in the first recess Ca (see FIG. 10A) which has been formed by removing the first gate insulating film 13a in addition to the first silicon film 15a and the first metal film 14a in the first gate electrode formation portion 14A, and the second metal film 30a is formed on the third gate insulating film 35a.

15 Also, in this variation, the first gate insulating film 13a in the first gate electrode formation portion 14A is replaced with the third gate insulating film 35a, and therefore, the third gate insulating film 35a is interposed between the first and second gate electrodes 30A and 30B, which are adjacent to each other in the gate width direction. Therefore, in this variation, when the metal silicide film 34 (see FIG. 11B) is formed, an upper portion of the third gate insulating film 35a is removed to form the groove R, thereby exposing, to the
20 groove R, side surfaces in the gate width direction of the second metal film 30a and side surfaces in the gate width direction of the second silicon film 15b, as shown in FIG. 11A, so as to electrically connect the first and second gate electrodes 30A and 30B. As a result, although not shown in FIG. 11B which is across-sectional view in the gate length direction, the metal silicide film 34 can be formed above and in contact with side surfaces in the gate
25 width direction of the second metal film 30a and side surfaces in the gate width direction of

the second silicon film 15b which are exposed to the inside of the groove R as shown in FIG. 12 described below. Therefore, by electrically connecting the second metal film 30a and the second silicon film 15b, the first and second gate electrodes 30A and 30B can be electrically connected.

5 A structure of the semiconductor device of the variation of the second embodiment of the present disclosure will be described hereinafter with reference to FIG. 12. FIG. 12 is a cross-sectional view showing the structure of the semiconductor device of the variation of the second embodiment of the present disclosure, as viewed in a gate width direction thereof. Note that, in FIG. 12, the same components as those in the second embodiment are indicated
10 by the same reference symbols as those of FIG. 9 in the second embodiment. Note that, in FIG. 12, “nMIS” shown on the left side indicates an n-type MIS formation region where an n-type MIS transistor is formed, and “pMIS” shown on the right side indicates a p-type MIS formation region where a p-type MIS transistor is formed.

As shown in FIG. 12, the first gate electrode 30A made of the second metal film
15 30a is formed on the first active region 10a with the third gate insulating film 35a being interposed therebetween, and the second gate electrode 30B made of the first metal film 14b and the second silicon film (conductive film) 15b formed on the first metal film 14b is formed on the second active region 10b with the second gate insulating film 13b being interposed therebetween. The metal silicide film 34 is formed on the second silicon film 15b.

20 Here, the structure of this variation is different from that of the second embodiment in the following points.

In this variation, the third gate insulating film 35a is made of an insulating material different from that of the second gate insulating film 13b. Also, as shown in FIG. 12, the third gate insulating film 35a is formed, extending over an upper surface of the first active
25 region 10a and side surfaces in the gate width direction of the second metal film 30a, and is

interposed between a lower region of the first gate electrode 30A and a lower region of the second gate electrode 30B (note that, as shown in FIG. 11C, the third gate insulating film 35a is also formed on side surfaces in the gate length direction of the second metal film 30a in addition to the side surfaces in the gate width direction thereof). Also, the metal silicide film 34 is formed above and in contact with side surfaces in the gate width direction of the second metal film 30a and side surfaces in the gate width direction of the second silicon film 15b which are exposed in the groove R. The metal silicide film 34 also electrically connects to the first and second gate electrodes 30A and 30B.

In contrast to this, in the second embodiment, the first gate insulating film 13a is made of the same insulating material as that of the second gate insulating film 13b. Also, the first gate insulating film 13a is not interposed between the first and second gate electrodes 30A and 30B.

Thus, the gate insulating film in the n-type MIS formation region and the gate insulating film in the p-type MIS formation region are made of different insulating material in this variation, and they are made of the same insulating material in the second embodiment.

According to this variation, an effect similar to that of the second embodiment can be obtained.

In addition, the third gate insulating film 35a has a thickness optimized for the n-type MIS transistor and is made of an insulating material optimized for the n-type MIS transistor (hereinafter referred to as an “nMIS insulating material”). Also, the second gate insulating film 13b has a thickness optimized for the p-type MIS transistor and is made of an insulating material optimized for the p-type MIS transistor (hereinafter referred to as a “pMIS insulating material”). Therefore, the flexibility of transistor design is increased, whereby a desired transistor characteristic can be achieved.

Note that, in the first and second embodiments, a pMIS metal film made of a pMIS

metal material is used as the first metal film 14, and an nMIS metal film made of an nMIS metal material is used as the second metal film 30. The first metal film (pMIS metal film) 14a and the first silicon film 15a in the first gate electrode formation portion 14A are replaced with the second metal film (nMIS metal film) 30a to form the first gate electrode 30A made of the second metal film 30a, and the second gate electrode 30B including the first metal film (pMIS metal film) 14b in the second gate electrode formation portion 14B is formed. The present disclosure is not limited to this specific example.

Conversely, an nMIS metal film may be used as the first metal film 14, and a pMIS metal film may be used as the second metal film 30. Note that, in this case, the first metal film (nMIS metal film) and the second silicon film in the second gate electrode formation portion are replaced with the second metal film (pMIS metal film) to form the second gate electrode made of the second metal film, and the first gate electrode including the first metal film (nMIS metal film) in the first gate electrode formation portion is formed.

Also, in the variation of the second embodiment, an nMIS metal film may be used as the first metal film 14, and a pMIS metal film may be used as the second metal film 30. Note that, in this case, an nMIS insulating film made of an nMIS insulating material is used as the gate insulating film formation film 13, and a pMIS insulating film made of a pMIS insulating material is used as the gate insulating film formation film 35.

Note that, in the first embodiment, the second embodiment and its variation, after the first and second outer sidewalls 20a and 20b are removed as shown in FIG. 3C, an underlying insulating film made of a silicon nitride film is formed as the insulating film 27 by, for example, plasma CVD as shown in FIG. 3D. The present disclosure is not limited to this specific example. For example, after the removal of the first and second outer sidewalls 20a and 20b, a stress insulating film which causes tensile stress in the gate length direction of the channel region in the first active region 10a may be formed as the insulating film 27. Here,

the stress insulating film is specifically formed as follows. A silicon nitride film containing a large amount of hydrogen is deposited by, for example, plasma CVD, followed by irradiation with ultraviolet light to remove hydrogen contained in the silicon nitride film, thereby forming an stress insulating film made of the silicon nitride film.

5 Thus, the stress insulating film applies tensile stress in the gate length direction of the channel region in the first active region 10a, whereby the drive capability of the n-type MIS transistor can be improved. Therefore, in addition to the improvement of the drive capability of the p-type MIS transistor by the silicon mixed crystal layer 24 as in the first embodiment, the second embodiment and its variation, the drive capability of the n-type MIS
10 transistor can be improved by the stress insulating film.

 In addition, the stress insulating film is formed after the first and second outer sidewalls 20a and 20b are removed, and therefore, a thickness of the stress insulating film can be increased by an amount corresponding to the removed portions of the first and second outer sidewalls 20a and 20b. As a result, tensile stress can be effectively applied in the gate
15 length direction of the channel region in the first active region 10a.

 Moreover, the stress insulating film can be formed closer to the channel region in the first active region 10a by an amount corresponding to the removed portions of the first and second outer sidewalls 20a and 20b. As a result, tensile stress can be more effectively applied in the gate length direction of the channel region in the first active region 10a.

20 Thus, when a stress insulating film is used as the insulating film 27 rather than an underlying insulating film, then if the first and second outer sidewalls 20a and 20b are previously removed before the stress insulating film is formed, tensile stress caused by the stress insulating film can be effectively applied in the gate length direction of the channel region in the first active region 10a.

25 On the other hand, when an underlying insulating film is used as the insulating film

27 as in the first embodiment, the second embodiment and its variation, it is not always necessary to remove the first and second outer sidewalls 20a and 20b before the insulating film 27 is formed as shown in FIG. 3C.

Note that, in the first embodiment, the second embodiment and its variation, the silicon mixed crystal layer 24 is used to improve the drive capability of the p-type MIS transistor. The present disclosure is not limited to this specific example. Both the drive capability of the n-type MIS transistor and the drive capability of the p-type MIS transistor may be improved. Firstly, for example, as in the first embodiment, the second embodiment and its variation, the silicon mixed crystal layer 24 may be provided, and a silicon mixed crystal layer which causes tensile stress in the gate length direction of the channel region in the first active region 10a may be provided in the trenches formed laterally outside the first sidewall 20A in the first active region 10a. Secondly, for example, a silicon mixed crystal layer which causes tensile stress in the gate length direction of the channel region in the first active region 10a may be provided in the trenches formed laterally outside the first sidewall 20A in the first active region 10a, and a stress insulating film which causes compressive stress in the gate length direction of the channel region in the second active region 10b may be provided as the insulating film 27.

Note that specific examples of the gate insulating film formation film 13 in the first and second embodiments, or the gate insulating film formation film 13 and the gate insulating film formation film 35 in the variation of the second embodiment, include hafnium-based oxides such as hafnium oxide (HfO_2), hafnium silicate (HfSiO), and hafnium silicon oxynitride (HfSiON) and the like, and oxides containing tantalum (Ta), zirconium (Zr), titanium (Ti), aluminum (Al), scandium (Sc), yttrium (Y), lanthanum (La) or the like. One of these insulating materials which is suitable for both the n-type MIS transistor and the p-type MIS transistor is used as the gate insulating film formation film 13 in the first and

second embodiments. Also, an insulating material optimized for the p-type MIS transistor and an insulating material optimized for the n-type MIS transistor are used as the gate insulating film formation film 13 and the gate insulating film formation film 35 in the variation of the second embodiment. In this case, the gate insulating film formation film 35
5 for the n-type MIS transistor and the gate insulating film formation film 13 for the p-type MIS transistor may be made of different insulating materials or the same insulating material. When the gate insulating film formation film 35 and the gate insulating film formation film 13 are made of the same insulating material, they may be optimized by changing their thicknesses or compositions (e.g., concentrations).

10 Also, although a polysilicon film is used as the silicon film 15 in the first embodiment, the second embodiment and its variation, a silicon film made of other semiconductor materials, such as an amorphous silicon film, a silicon film and the like, may be used.

Also, in the first embodiment, the second embodiment and its variation, when the
15 first and second metal silicide films 26a and 26b are formed, a metal film made of nickel is used as the metal film which is caused to react with upper portions of the deep n- and p-type source/drain regions 25a and 25b. Instead of this, a metal film made of a metal for silicidation, such as platinum, cobalt, titanium, tungsten or the like, may be used.

The present disclosure can provide gate electrodes of n- and p-type MIS transistors
20 which are formed with high precision, and an isolation region having a reduced width in the gate width direction, and therefore, is useful for a dual-metal gate semiconductor device and a method for manufacturing the semiconductor device.

CLAIMS

What is claimed is:

1. A semiconductor device comprising:
 - a first MIS transistor; and
 - 5 a second MIS transistor,wherein
 - the first MIS transistor includes
 - a first gate insulating film formed on a first active region in a semiconductor substrate,
 - 10 a first gate electrode includes a second metal film formed on the first gate insulating film, and
 - an insulating film formed, extending over side surfaces of the first gate electrode and upper surfaces of regions located in the first active region laterally outside the first gate electrode,
 - 15 the second MIS transistor includes
 - a second gate insulating film formed on a second active region in the semiconductor substrate,
 - a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film, and
 - 20 the insulating film formed, extending over side surfaces of the second gate electrode and upper surfaces of regions located in the second active region laterally outside the second gate electrode,
 - the first and second metal films are made of different metal materials, and
 - the insulating film is not formed on any of upper surfaces of the first and second
 - 25 gate electrodes.

2. The semiconductor device of claim 1, wherein
the first metal film has a thickness smaller than that of the second metal film.
- 5 3. The semiconductor device of claim 1, wherein
the first and second metal films have different work functions.
4. The semiconductor device of claim 1, wherein
the insulating film has a thickness smaller than that of the first gate electrode.
- 10 5. The semiconductor device of claim 1, wherein
the conductive film is made of the second metal film.
6. The semiconductor device of claim 1, wherein
15 the conductive film is made of a silicon film, and
the semiconductor device further comprises a metal silicide film formed on the
silicon film.
7. The semiconductor device of claim 1, wherein
20 the first and second gate insulating films are made of the same insulating material.
8. The semiconductor device of claim 1, wherein
the first and second gate insulating films are made of different insulating materials.
- 25 9. The semiconductor device of claim 1, further comprising:

a first inner sidewall having an L-shaped cross-section formed on each of side surfaces of the first gate electrode, and

a second inner sidewall having an L-shaped cross-section formed on each of side surfaces of the second gate electrode,

5 wherein

the insulating film is formed above and in contact with the first and second inner sidewalls.

10 10. The semiconductor device of claim 1, wherein
the insulating film is a stress insulating film which causes first stress in a gate length direction of a channel region in the first active region.

11. The semiconductor device of claim 10, wherein
the first MIS transistor is an n-type MIS transistor,
15 the insulating film is made of a silicon nitride film, and
the first stress is tensile stress.

12. The semiconductor device of claim 1, further comprising:
source/drain regions formed in the second active region laterally outside the second
20 gate electrode,
wherein

the source/drain regions include a silicon mixed crystal layer which is formed in trenches provided in the second active region, and causes second stress in a gate length direction of a channel region in the second active region.

25

13. The semiconductor device of claim 12, wherein
the second MIS transistor is a p-type MIS transistor,
the silicon mixed crystal layer is made of a SiGe layer, and
the second stress is compressive stress.

5

14. The semiconductor device of claim 1, wherein
the first and second gate insulating films include a high-k film made of a metal
oxide having a relative dielectric constant of 10 or more.

10 15. A method for manufacturing a semiconductor device including a first MIS
transistor formed on a first active region in a semiconductor substrate and a second MIS
transistor formed on a second active region in the semiconductor substrate, the method
comprising the steps of:

(a) forming a first gate electrode formation portion having a first gate insulating
15 film, a first metal film and a first silicon film on the first active region, and a second gate
electrode formation portion having a second gate insulating film, a first metal film and a
second silicon film on the second active region;

(b) after step (a), forming an insulating film on the semiconductor substrate, the
insulating film covering the first and second gate electrode formation portions;

20 (c) removing the insulating film formed on the first and second gate electrode
formation portions to expose an upper surface of each of the first silicon film in the first gate
electrode formation portion and the second silicon film in the second gate electrode formation
portion;

(d) after step (c), successively removing the first silicon film and the first metal film
25 in the first gate electrode formation portion to form a first recess surrounded by the insulating

film on the first active region; and

(e) forming a second metal film in the first recess,

wherein

a first gate electrode of the first MIS transistor includes the second metal film, and

5 a second gate electrode of the second MIS transistor includes the first metal film in the second gate electrode formation portion.

16. The method of claim 15, wherein

step (d) includes forming, on the first active region, the first recess from a bottom of
10 which the first gate insulating film is exposed, and removing the second silicon film in the second gate electrode formation portion to form, on the second active region, a second recess surrounded by the insulating film, the first metal film being exposed from a bottom of the second recess,

step (e) includes forming the second metal film on the first gate insulating film in
15 the first recess, and forming the second metal film on the first metal film in the second recess, and

the second gate electrode includes the first metal film in the second gate electrode formation portion and the second metal film formed on the first metal film.

20 17. The method of claim 15, wherein

step (d) includes forming, on the first active region, the first recess from a bottom of which the first gate insulating film is exposed,

step (e) includes forming the second metal film on the first gate insulating film in the first recess,

25 the method further comprises the step of

(f) after step (e), forming a metal silicide film on the second silicon film,
and

the second gate electrode includes the first metal film and the second silicon film in
the second gate electrode formation portion.

5

18. The method of claim 15, wherein

step (d) includes successively removing the first silicon film, the first metal film,
and the first gate insulating film in the first gate electrode formation portion, to form, on the
first active region, the first recess from a bottom of which the first active region is exposed,

10 step (e) includes forming a third gate insulating film in the first recess, and forming
the second metal film on the third gate insulating film,

the method further comprises the step of

(f) after step (e), forming a metal silicide film on the second silicon film,
and

15 the second gate electrode includes the first metal film and the second silicon film in
the second gate electrode formation portion.

19. The method of claim 15, further comprising the step of:

(g) after step (a) and before step (b), forming a first inner sidewall having an
20 L-shaped cross-section on each of side surfaces of the first gate electrode formation portion,
and a second inner sidewall having an L-shaped cross-section on each of side surfaces of the
second gate electrode formation portion,

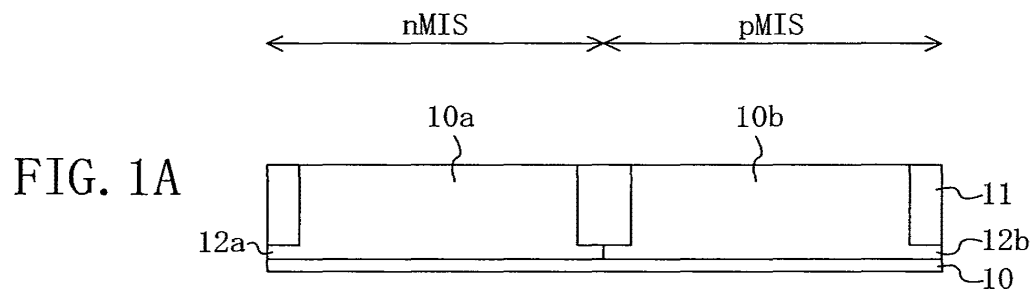
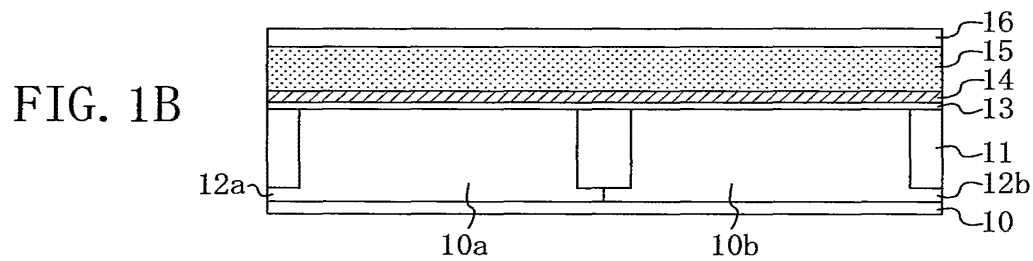
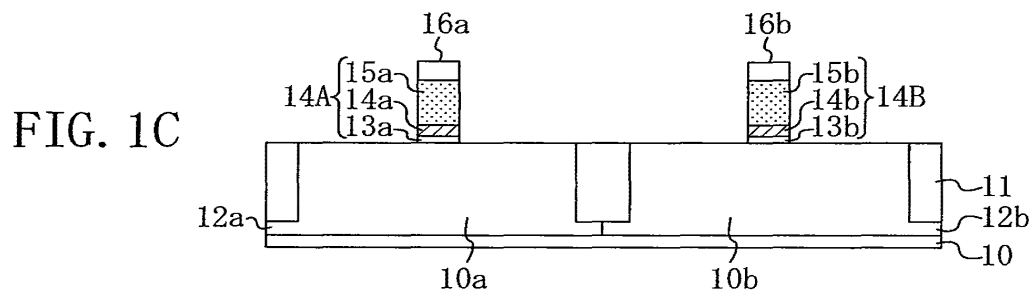
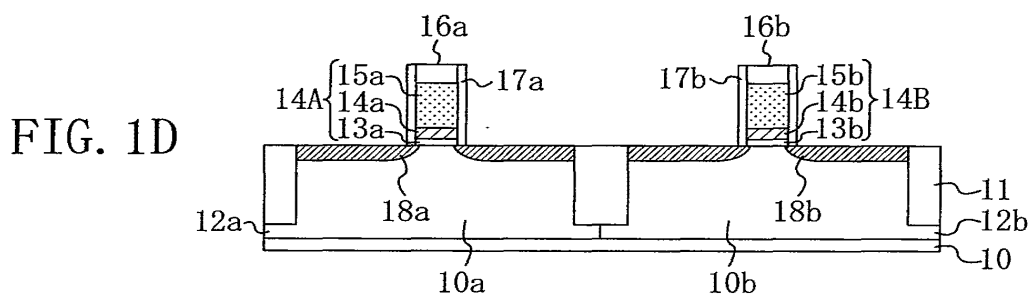
wherein

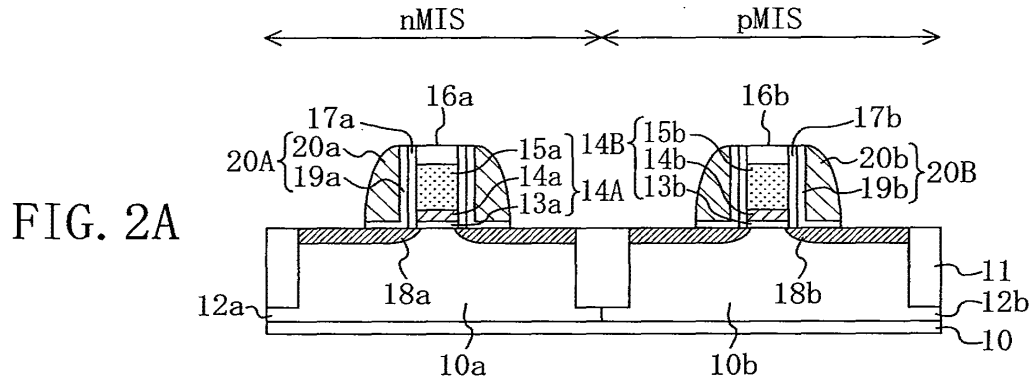
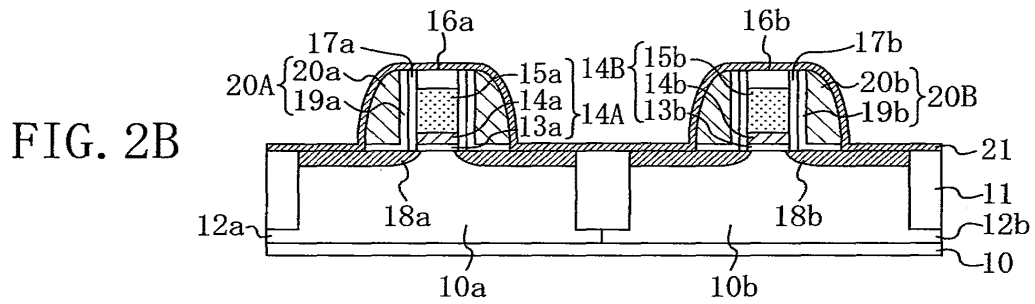
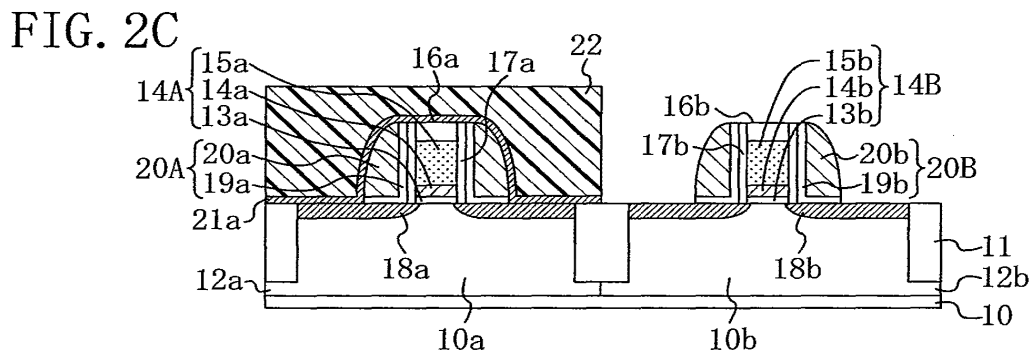
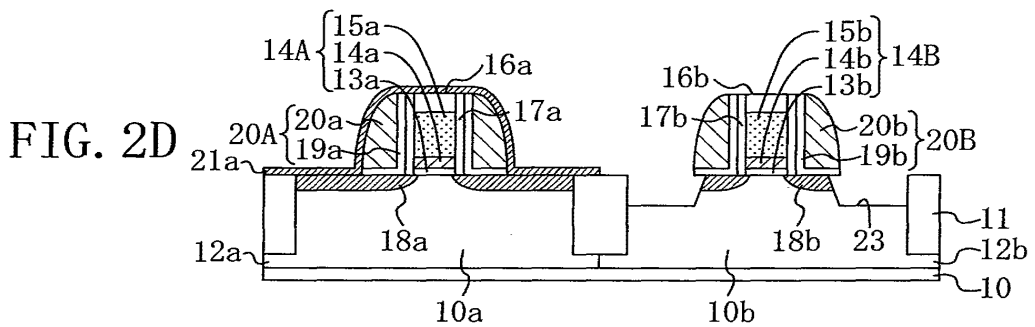
in step (b), the insulating film is formed above and in contact with the first and
25 second inner sidewalls.

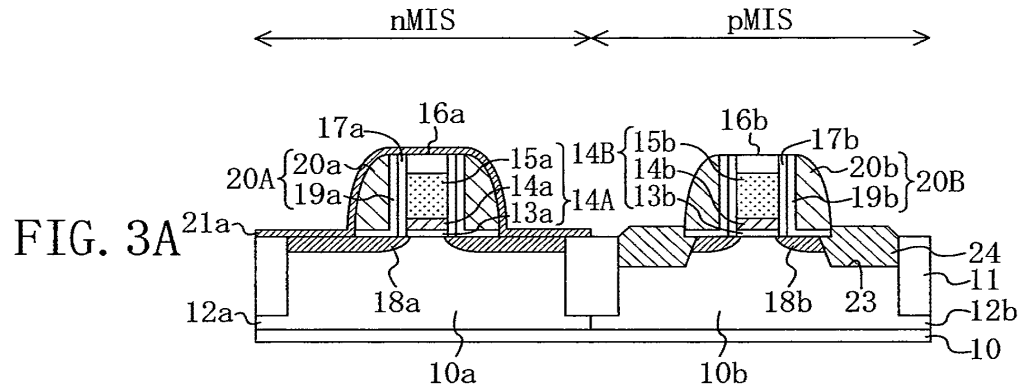
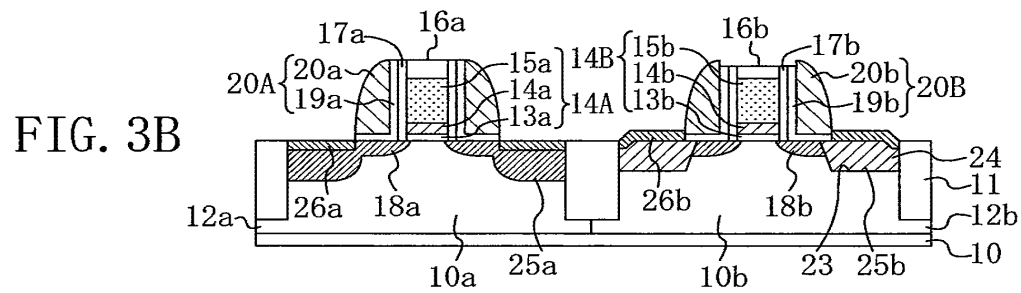
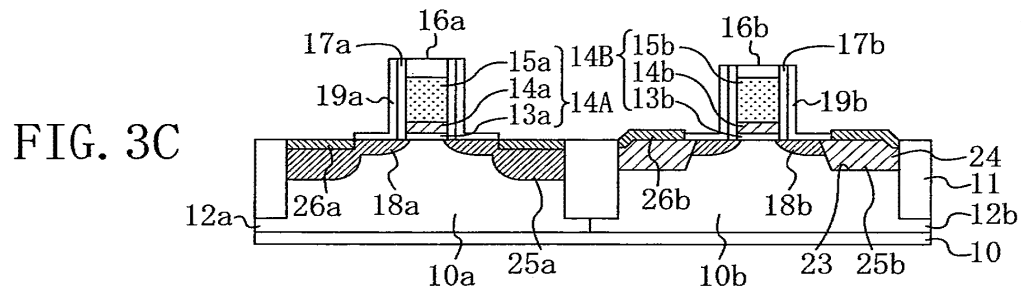
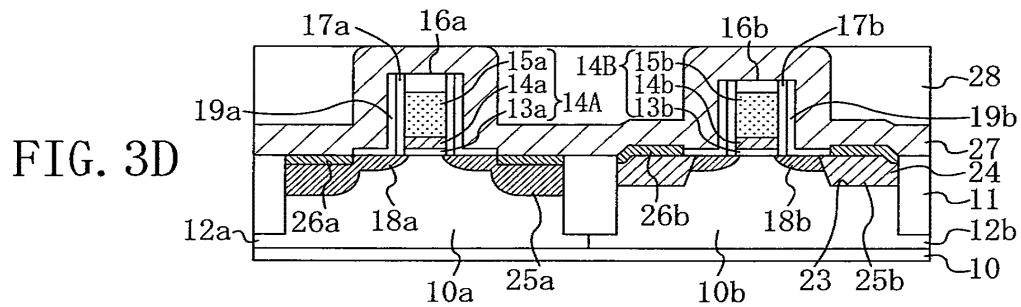
20. The method of claim 15, further comprising the steps of:
- (h) after step (a) and before step (b), forming trenches in the second active region laterally outside the second gate electrode formation portion; and
- 5 (i) forming, in the trenches, a silicon mixed crystal layer which causes stress in a gate length direction of a channel region in the second active region.

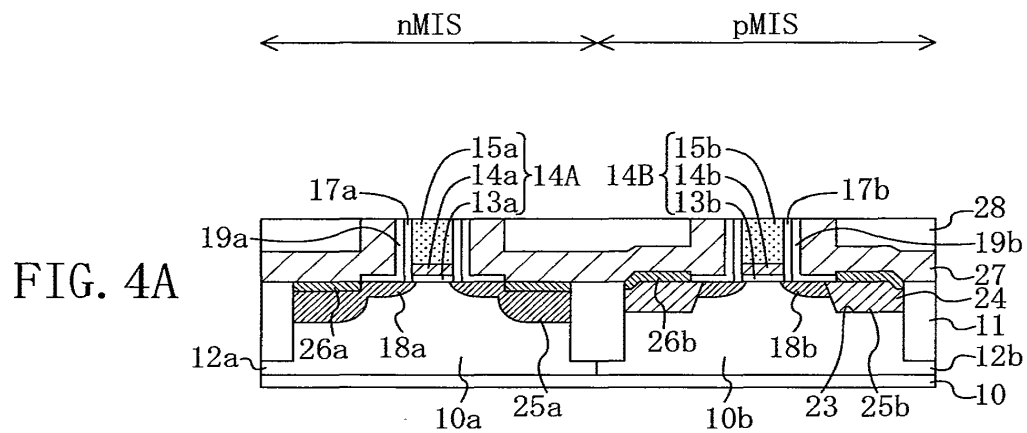
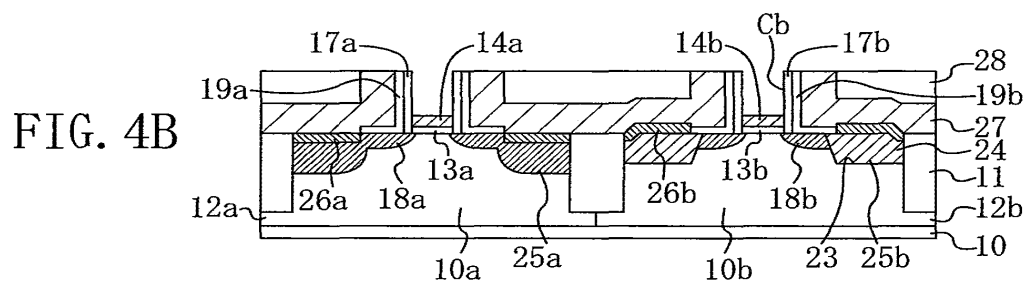
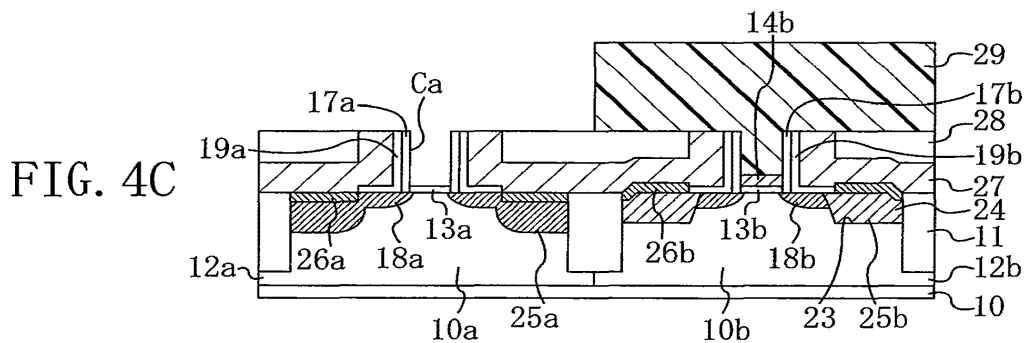
ABSTRACT

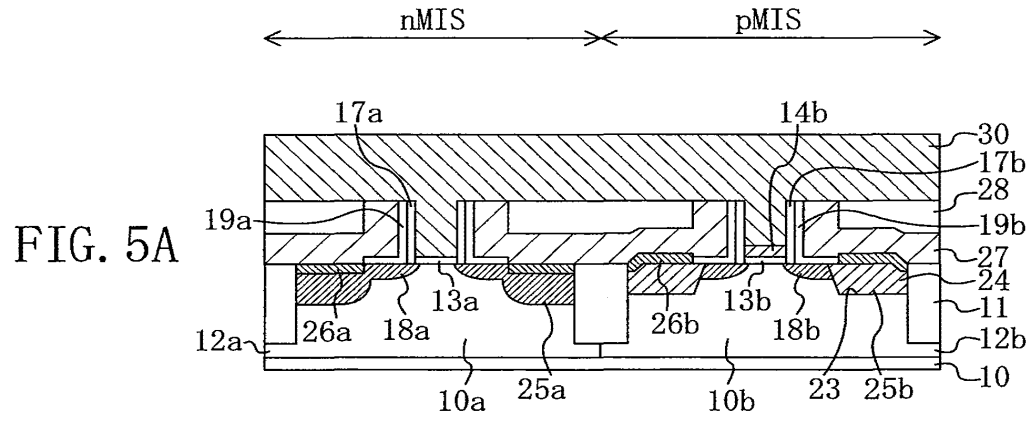
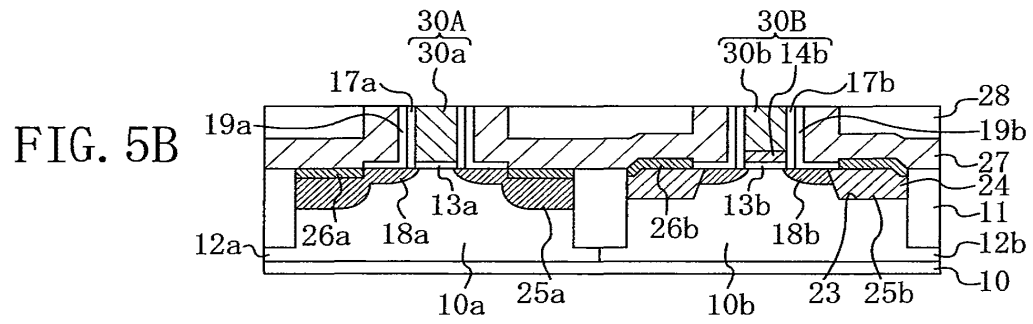
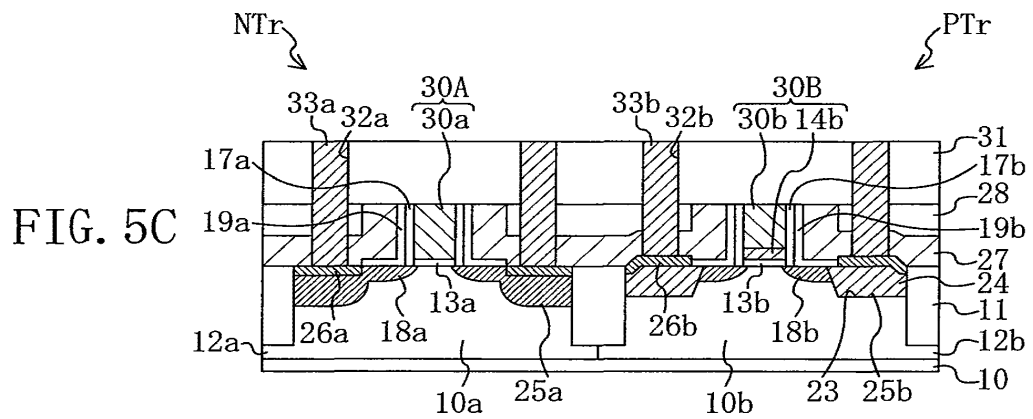
A semiconductor device includes a first MIS transistor and a second MIS transistor. The first MIS transistor includes a first gate electrode includes a second metal film formed on
5 a first gate insulating film, and an insulating film formed, extending over side surfaces of the first gate electrode and upper surfaces of regions located in the first active region laterally outside the first gate electrode. The second MIS transistor includes a second gate electrode including a first metal film formed on a second gate insulating film and a conductive film formed on the first metal film, and the insulating film formed, extending over side surfaces of
10 the second gate electrode and upper surfaces of regions located in the second active region laterally outside the second gate electrode. The first and second metal films are made of different metal materials.

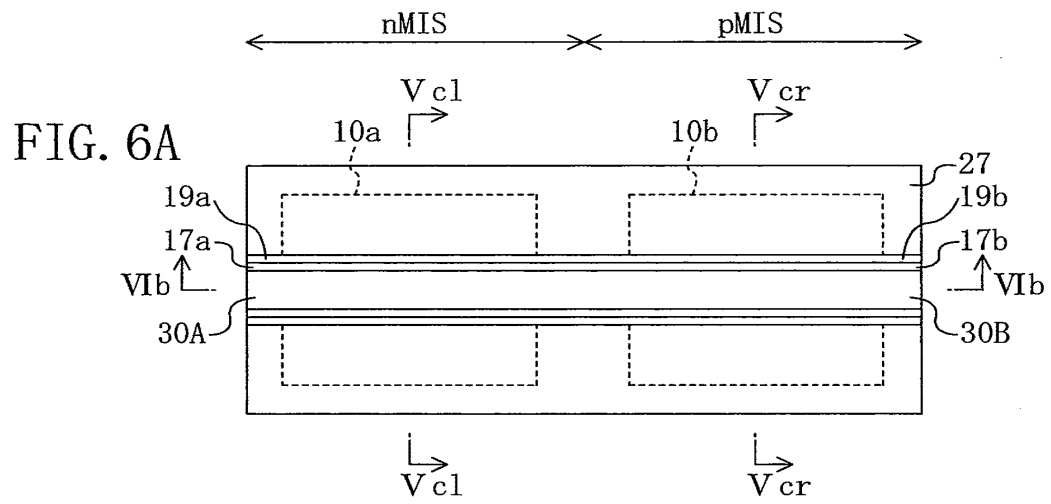
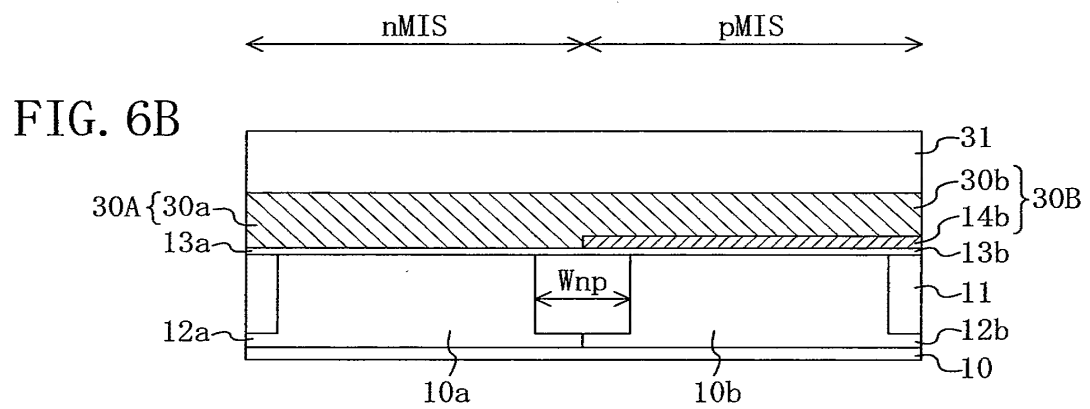


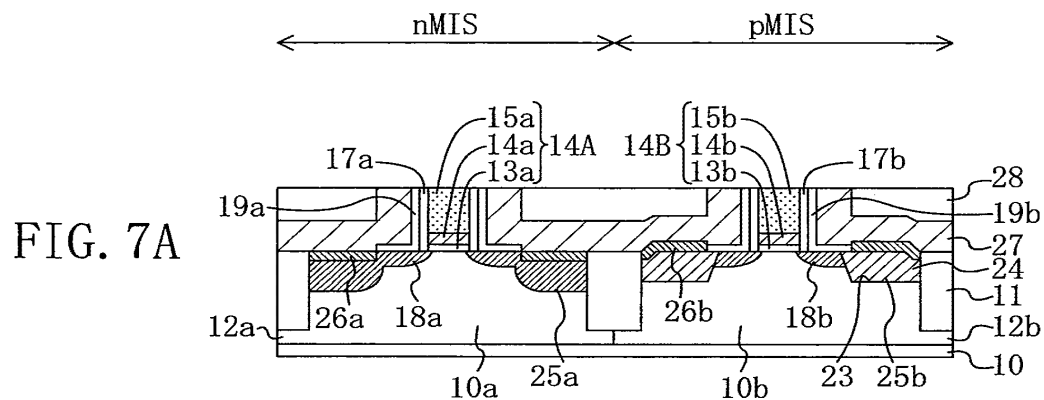
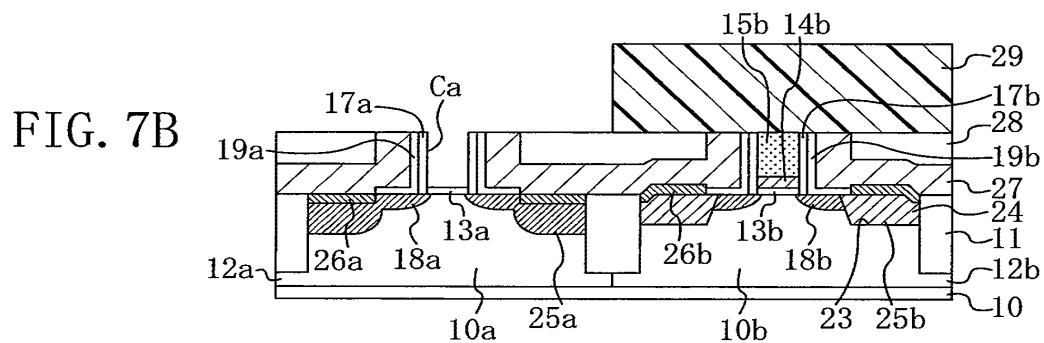
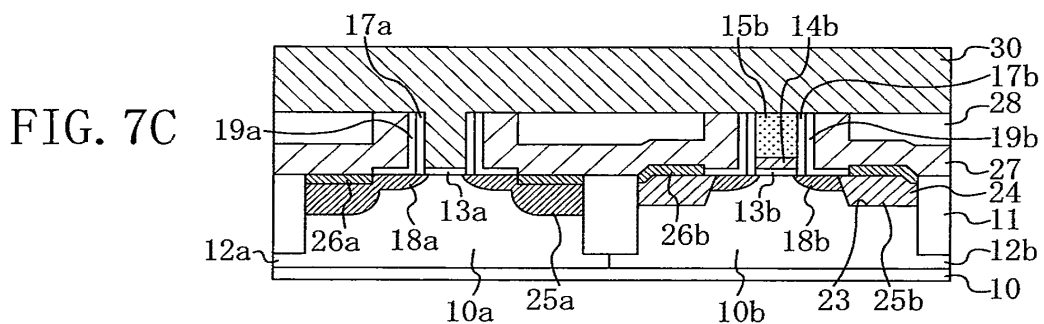


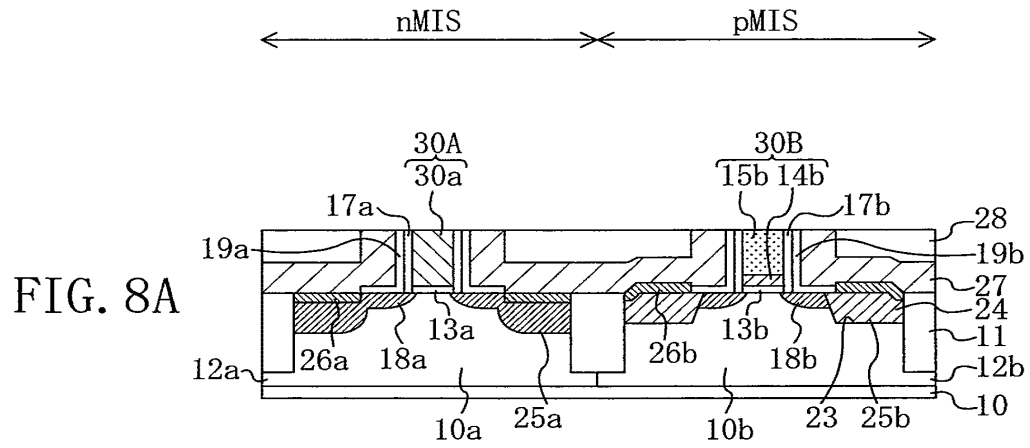
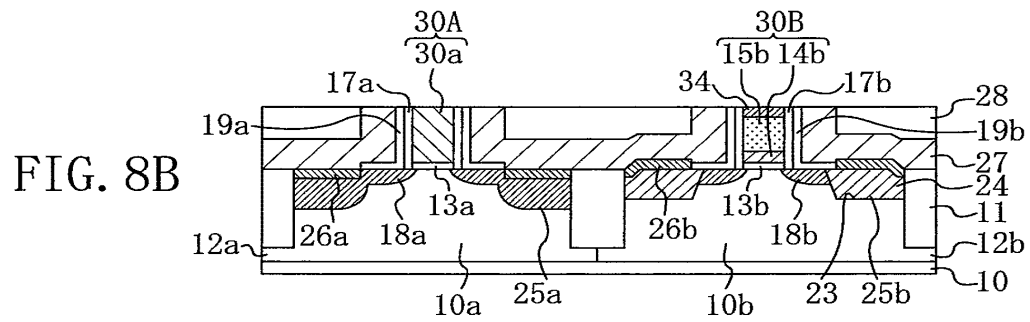
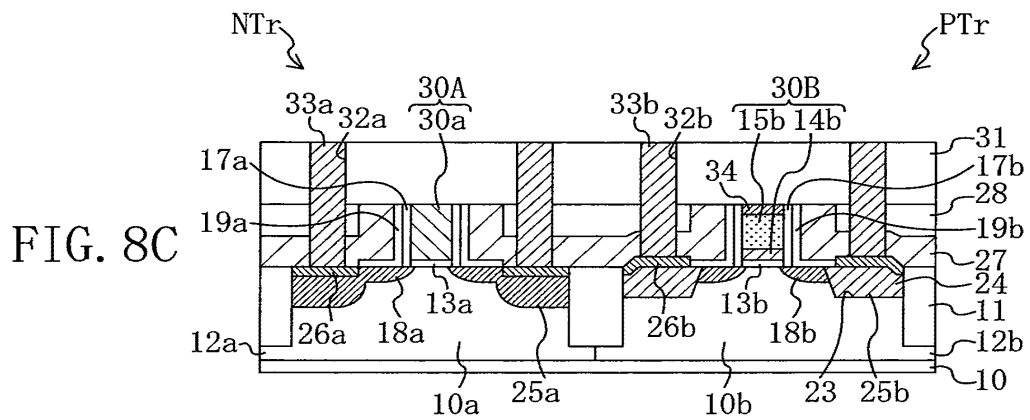






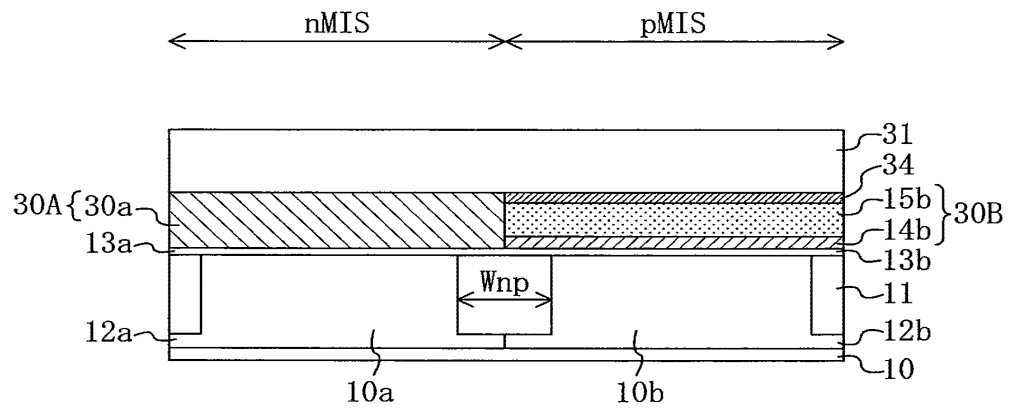


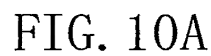
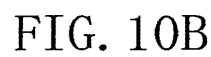
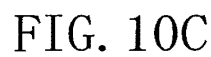




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FIG. 9





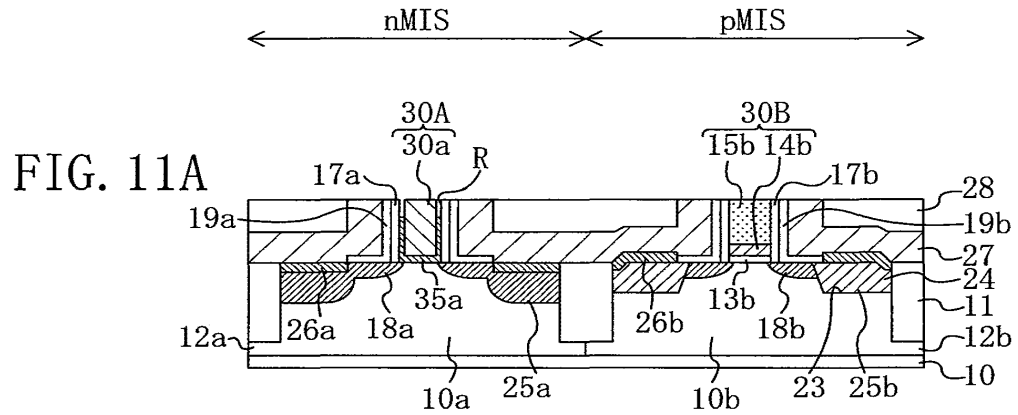
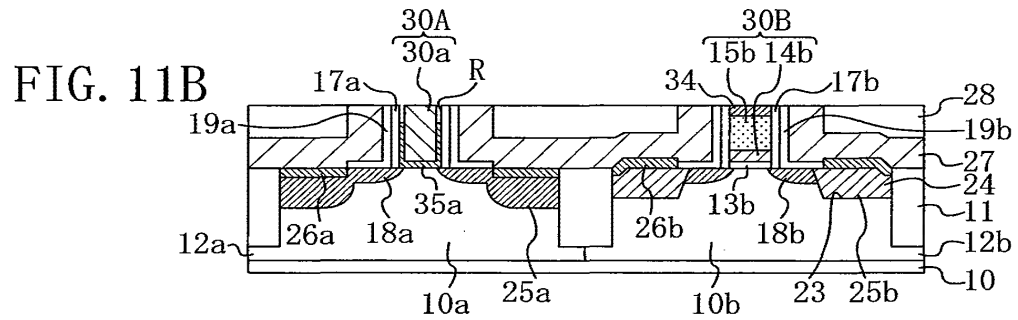
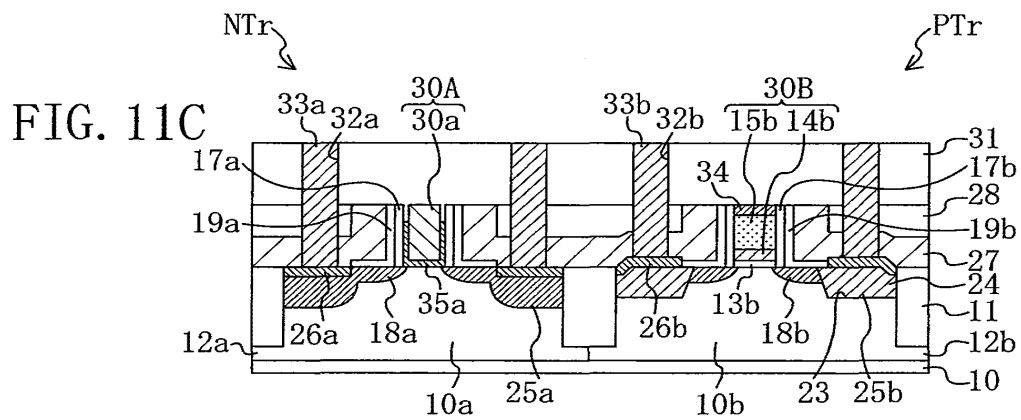


FIG. 12

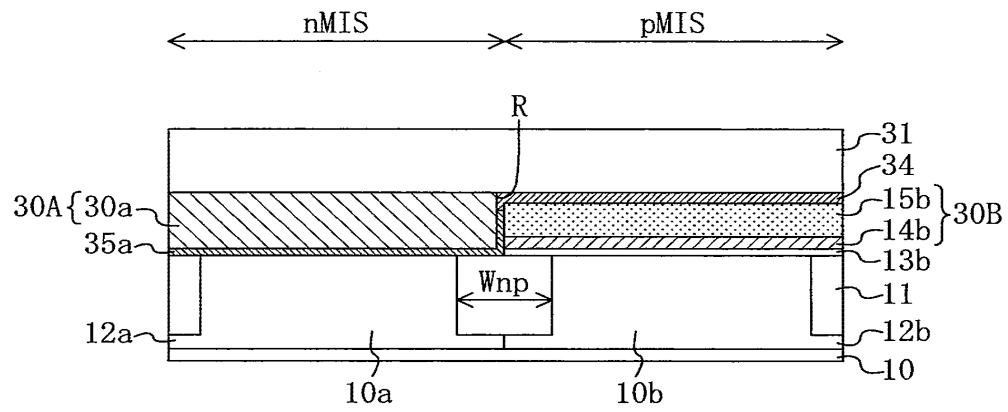
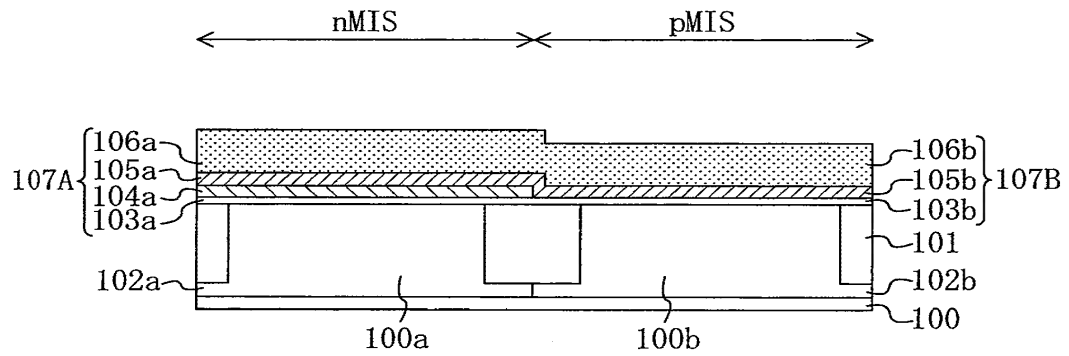
FIG. 13
PRIOR ART

FIG. 14A

PRIOR ART

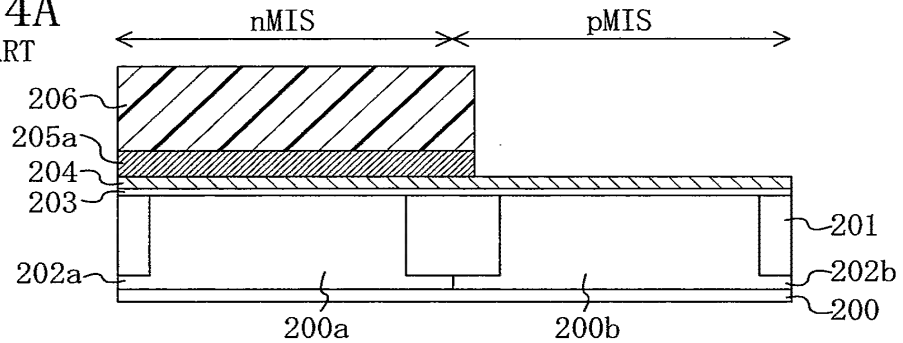


FIG. 14B

PRIOR ART

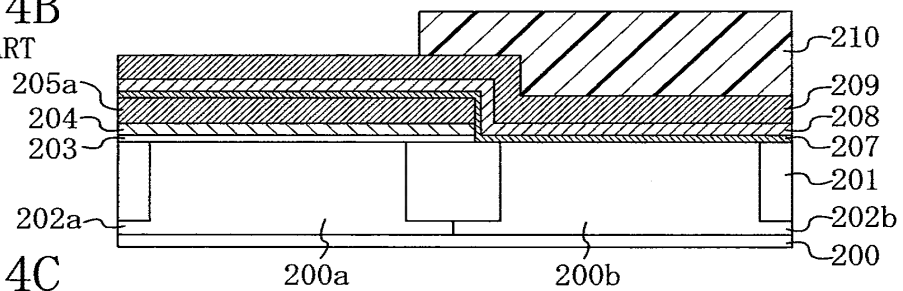


FIG. 14C

PRIOR ART

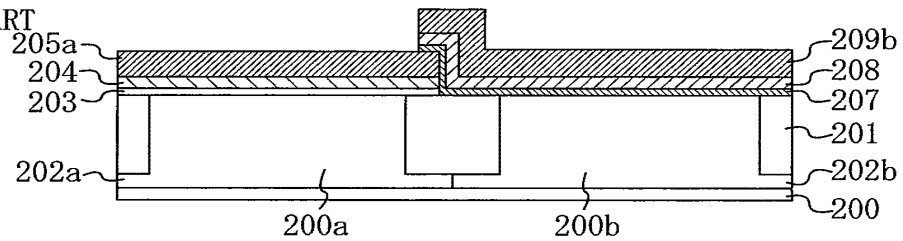


FIG. 14D

PRIOR ART

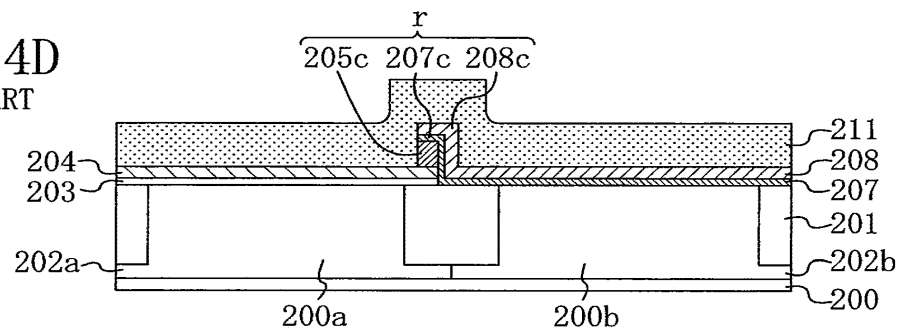


FIG. 14E

PRIOR ART

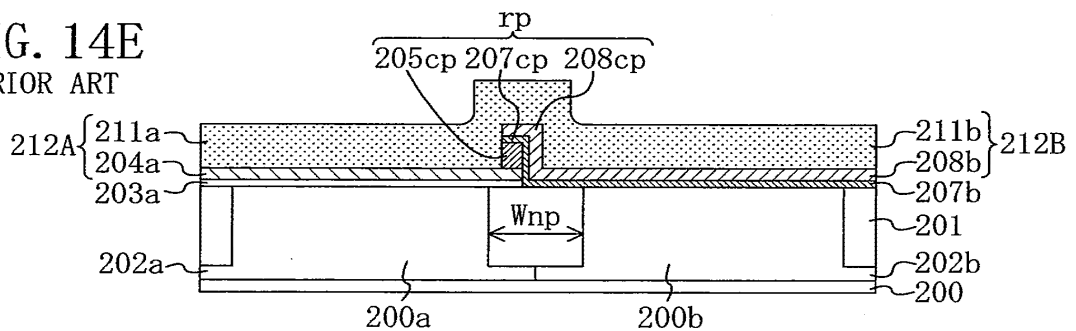


FIG. 15
PRIOR ART

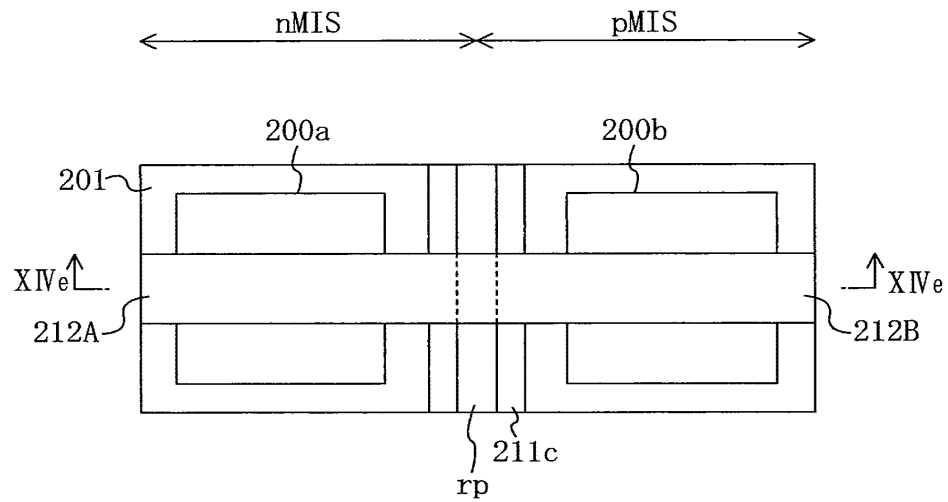
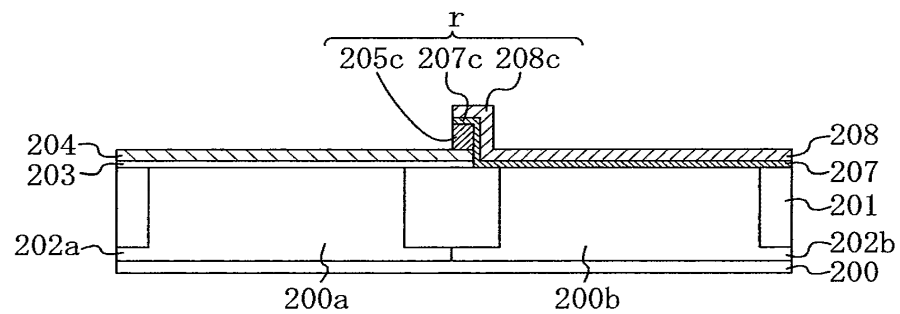


FIG. 16
PRIOR ART



Panasonic Ref*: P051653-01

(* must be filled)

Japan Firm Name: MAEDA PATENT OFFICEUS Firm Name: MWE

Application Serial No. _____

Japan Firm Ref: M08-OK585US1

US Firm Ref: _____

DECLARATION AND POWER OF ATTORNEY FOR U.S. PATENT APPLICATION(a) ☒ Original (b) ☐ Supplemental (c) ☐ Substitute (d) ☐ PCT (e) ☐ Design

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; and I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Title of Invention:

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

which is described and claimed in (if the following box is not checked, the specification of which is attached hereto):

1. For use when submitting this Declaration prior to U.S. application filing date			
(f) ☒ the attached specification, or			
2. For use when submitting this Declaration after U.S. application filing date			
(g) ☐ the specification in the U.S. Application:	Application No. (if available)		filed on: (must be filled)
	and with amendments (if applicable):		filed on _____, or
3. For PCT-US national entry under 35 U.S.C. 371 (for use when filing this Declaration before and after the U.S. national entry date)			
(h) ☐ the specification in the International Application: (Check here only for US national entry under 35 U.S.C. 371.)	PCT Application No.		filed on: (PCT filing date)
	and with amendments (if applicable):		filed on: _____

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above.

I acknowledge my duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a-d), §172, or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below, and have also identified below any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed:

(Foreign Priority Information)

COUNTRY	APPLICATION NO.	DATE OF FILING	PRIORITY CLAIMED
JAPAN	2008-064435	March 13, 2008	Yes

☐ Additional foreign or international application numbers are listed on a supplemental priority sheet attached hereto.

I hereby claim the benefit under Title 35, United States Code §119(e) of any United States Provisional application(s) listed below.

(US Provisional Application Information)

APPLICATION NO.	U.S. PROVISIONAL APPLICATION FILING DATE

☐ Additional U.S. provisional application numbers are listed on a supplemental priority sheet attached hereto.

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s), or §365(C) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

(Domestic Priority Information)

APPLICATION NO.	U.S. FILING DATE	STATUS: PATENTED, PENDING, ABANDONED
PCT/JP2009/000574	February 13, 2009	Pending

☐ Additional U.S. or international application numbers are listed on a supplemental priority sheet attached hereto.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the attorneys and agents associated with the U.S. Patent and Trademark Office Customer Number identified below to prosecute this application including divisions, continuations and reissues thereof in the United States and to transact all business in the U.S. Patent and Trademark Office connected therewith, and direct that all correspondence be addressed to that customer number.

I hereby authorize the U.S. attorneys and agents associated with the customer number to accept and follow instructions from Panasonic Corporation and any affiliated or subsidiary company thereof, received via their corporate representatives and/or their foreign patent attorneys or agents, if any, as to any action to be taken in the U.S. Patent and Trademark Office regarding this application without direct communication between the U.S. attorneys or agents and myself.

Power of Attorney given to practitioners associated with, and direct Correspondence to:

CUSTOMER NUMBER 53080

I further declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

INVENTOR (s)

Full Name of Sole or First Inventor	FIRST NAME Yoshihiro	LAST NAME SATO	SIGNATURE <i>Yoshihiro Sato</i>	DATE OF SIGNATURE <i>Nov. 2, 2009</i>
Residence & Citizenship	CITY, STATE or COUNTRY Hyogo, Japan			CITIZENSHIP JAPAN
Post office address	ADDRESS c/o Panasonic Corporation, 1006, Oaza Kadoma, Kadoma-shi, Osaka, Japan 571-8501			

Full Name of Second Inventor	FIRST NAME Hisashi	LAST NAME OGAWA	SIGNATURE <i>Hisashi Ogawa</i>	DATE OF SIGNATURE <i>Nov. 5, 2009</i>
Residence & Citizenship	CITY, STATE or COUNTRY Osaka, Japan			CITIZENSHIP JAPAN
Post office address	ADDRESS c/o Panasonic Corporation, 1006, Oaza Kadoma, Kadoma-shi, Osaka, Japan 571-8501			

Total of 2 pages are submitted.

Docket No.: 085393-0059

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Yoshihiro SATO, et al.	:	Confirmation Number: Not Yet Assigned
	:	
Application No.: Not Yet Assigned	:	Group Art Unit: Not Yet Assigned
	:	
Filed: December 02, 2009	:	Examiner: Not Yet Assigned
	:	
For: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME		

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date. No certification or fee is required.

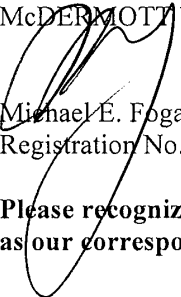
JP 2007-258267, US 2007/0215950, JP 2002-118175, JP 11-074368, US 6,184,083, US 7,361,960, WO 2006/049834 and US 2006/0094193 A1 were cited in a International Search Report issued in corresponding International Application PCT/JP2009/000574. A copy of the International Search Report is attached for the Examiner's information.

The relevance of the articles **“Integration of Dual Metal Gate CMOS with TaSiN (NMOS) and Ru (PMOS) Gate Electrodes on HfO₂ Gate Dielectric”**, by Z.B. ZHANG, et al. and **“Highly Manufacturable 45 nm LSTP CMOSFETs Using Novel Dual High-k and Dual Metal Gate CMOS Integration”**, by S.C. SONG, et al., cited on the attached form PTO-1449, is discussed in the present specification.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP


Michael E. Fogarty
Registration No. 36,139

**Please recognize our Customer No. 53080
as our correspondence address.**

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:kfm
Facsimile: 202.756.8087
Date: December 2, 2009

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Substitute for form 1449/PTO)				ATTY. DOCKET NO. 085393-0059		SERIAL NO. Not Yet Assigned	
				APPLICANT Yoshihiro SATO, et al.			
				FILING DATE December 02, 2009		GROUP Not Yet Assigned	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
		US 2007/0215950 A1	09-20-2007	AOYAMA			
		US 6,184,083 B1	02-06-2001	TSUNASHIMA et al.			
		US 7,361,960 B1	04-22-2008	TSUNASHIMA et al.			
		US 2006/0094193 A1	05-04-2006	HORSTMANN et al.			
		US 2007/0090427 A1	04-26-2007	NAKAJIMA			
		US 2007/0173025 A1	07-26-2007	AKAMATSU			
		US 2005/0167762 A1	08-04-2005	KADOSHIMA et al.			
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number & Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes No	
		JP 2007-258267	10-04-2007	TOSHIBA CORP		English Abstract Only	
		JP 2002-118175	04-19-2002	TOSHIBA CORP		JAPAN (w/English abstract)	
		JP 11-074368	03-16-1999	TOKYO SHIBAURA ELECTRIC CO		English Abstract Only	
		WO 2006/049834 A1	05-11-2006	ADVANCED MICRO DEVICES, INC.		English Original	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
		ZHANG, Z.B., et al., "Integration of Dual Metal Gate CMOS with TaSiN (NMOS) and Ru (PMOS) Gate Electrodes on HfO ₂ Gate Dielectric", Symposium on VLSI Technology Digest of Technical Papers, 2005, Pages 50-51					
		SONG, S.C., et al., "Highly Manufacturable 45 nm LSTP CMOSFETs Using Novel Dual High-k and Dual Metal Gate CMOS Integration", Symposium on VLSI Technology Digest of Technical Papers, 2006, IEEE					
		HUSSAIN, M., et al. "Compatibility of ALD Hafnium Silicate with Dual Metal Gate CMOS Integration", Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Pages 1114-1115					
		OOTSUKA, F., et al., "Full-Metal-Gate Integration of Dual-Metal-Gate HfSiON CMOS Transistors by Using Oxidation-Free Dummy-Mask Process", Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Pages 1116-1117					
EXAMINER				DATE CONSIDERED			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2009/000574

A. CLASSIFICATION OF SUBJECT MATTER

H01L21/8238(2006.01)i, H01L21/28(2006.01)i, H01L21/336(2006.01)i,
H01L27/092(2006.01)i, H01L29/423(2006.01)i, H01L29/49(2006.01)i,
H01L29/78(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L21/8238, H01L21/28, H01L21/336, H01L27/092, H01L29/423, H01L29/49,
H01L29/78

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho 1922-1996 Jitsuyo Shinan Toroku Koho 1996-2009
Kokai Jitsuyo Shinan Koho 1971-2009 Toroku Jitsuyo Shinan Koho 1994-2009

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2007-258267 A (Toshiba Corp.), 04 October, 2007 (04.10.07), Full text; all drawings &US 2007/0215950 A1	1, 2
A	JP 2002-118175 A (Toshiba Corp.), 19 April, 2002 (19.04.02), Fig. 11 (Family: none)	1, 2
A	JP 11-74368 A (Toshiba Corp.), 16 March, 1999 (16.03.99), Figs. 26 to 28 √& US 6184083 B1 Fig. 17 X& US 7361960 B1	1, 2

☒ Further documents are listed in the continuation of Box C.☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search
01 May, 2009 (01.05.09)

Date of mailing of the international search report
19 May, 2009 (19.05.09)

Name and mailing address of the ISA/
Japanese Patent Office

Authorized officer

Facsimile No.

Telephone No.

Form PCT/ISA/210 (second sheet) (April 2007)

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2009/000574

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>✓WO 2006/49834 A1 (Advanced Micro Devices, Inc.), 11 May, 2006 (11.05.06), Full text; all drawings & JP 2008-518476 A ✓& US 2006/0094193 A1 & GB 2434036 A & GB 708894 D & DE 102004052617 A & KR 10-2007-0069160 A & CN 101044614 A</p>	1, 2

Form PCT/ISA/210 (continuation of second sheet) (April 2007)

A. 発明の属する分野の分類 (国際特許分類 (IPC)) Int.Cl. H01L21/8238(2006.01)i, H01L21/28(2006.01)i, H01L21/336(2006.01)i, H01L27/092(2006.01)i, H01L29/423(2006.01)i, H01L29/49(2006.01)i, H01L29/78(2006.01)i			
B. 調査を行った分野 調査を行った最小限資料 (国際特許分類 (IPC)) Int.Cl. H01L21/8238, H01L21/28, H01L21/336, H01L27/092, H01L29/423, H01L29/49, H01L29/78			
最小限資料以外の資料で調査を行った分野に含まれるもの 日本国実用新案公報 1922-1996年 日本国公開実用新案公報 1971-2009年 日本国実用新案登録公報 1996-2009年 日本国登録実用新案公報 1994-2009年			
国際調査で使用した電子データベース (データベースの名称、調査に使用した用語)			
C. 関連すると認められる文献			
引用文献の カテゴリー*	引用文献名 及び一部の箇所が関連するときは、その関連する箇所の表示	関連する 請求項の番号	
X	JP 2007-258267 A (株式会社東芝) 2007.10.04, 全文, 全図 & US 2007/0215950 A1 ✓	1,2	
A	JP 2002-118175 A (株式会社東芝) 2002.04.19, 第11図 (ファミリーなし) ✓	1,2	
A	JP 11-74368 A (株式会社東芝) 1999.03.16, 第26-28図 & US 6184083 B1, 第17図 & US 7361960 B1 ✓	1,2	
☒ C欄の続きにも文献が列挙されている。 ☐ パテントファミリーに関する別紙を参照。			
* 引用文献のカテゴリー 「A」 特に関連のある文献ではなく、一般的技術水準を示すもの 「E」 国際出願日前の出願または特許であるが、国際出願日以後に公表されたもの 「L」 優先権主張に疑義を提起する文献又は他の文献の発行日若しくは他の特別な理由を確立するために引用する文献 (理由を付す) 「O」 口頭による開示、使用、展示等に言及する文献 「P」 国際出願日前で、かつ優先権の主張の基礎となる出願 の日の後に公表された文献 「T」 国際出願日又は優先日後に公表された文献であって出願と矛盾するものではなく、発明の原理又は理論の理解のために引用するもの 「X」 特に関連のある文献であって、当該文献のみで発明の新規性又は進歩性がないと考えられるもの 「Y」 特に関連のある文献であって、当該文献と他の1以上の文献との、当業者にとって自明である組合せによって進歩性がないと考えられるもの 「&」 同一パテントファミリー文献			
国際調査を完了した日 01.05.2009		国際調査報告の発送日 19.05.2009	
国際調査機関の名称及びあて先 日本国特許庁 (ISA/J P) 郵便番号100-8915 東京都千代田区霞が関三丁目4番3号		特許庁審査官 (権限のある職員) 宇多川 勉 電話番号 03-3581-1101 内線 3498	4L 3125

様式PCT/ISA/210 (第2ページ) (2007年4月)

C (続き) . 関連すると認められる文献		
引用文献の カテゴリー*	引用文献名 及び一部の箇所が関連するときは、その関連する箇所の表示	関連する 請求項の番号
A	WO 2006/49834 A1 (アドバンスド・マイクロ・デバイス・イン コーポレイテッド) 2006.05.11, 全文, 全図 & JP 2008-518476 A & US 2006/0094193 A1 & GB 2434036 A & GB 708894 D & DE 102004052617 A & KR 10-2007-0069160 A & CN 101044614 A	1, 2

様式PCT/ISA/210 (第2ページの続き) (2007年4月)

特許協力条約

PCT

国際調査報告

(法 8 条、法施行規則第 40、41 条)
〔PCT18 条、PCT 規則 43、44〕



出願人又は代理人 Mog-0k585CT1 書類記号 P051653P0	今後の手続きについては、様式PCT/ISA/220 及び下記5を参照すること。	
国際出願番号 PCT/J P 2009/000574	国際出願日 (日.月.年) 13. 02. 2009	優先日 (日.月.年) 13. 03. 2008
出願人 (氏名又は名称) パナソニック株式会社		

国際調査機関が作成したこの国際調査報告を法施行規則第41条 (PCT18条) の規定に従い出願人に送付する。
この写しは国際事務局にも送付される。

この国際調査報告は、全部で 4 ページである。

☐ この調査報告に引用された先行技術文献の写しも添付されている。

1. 国際調査報告の基礎

a. 言語に関し、この国際調査は以下のものに基づき行った。

☒ 出願時の言語による国際出願

☐ 出願時の言語から国際調査のための言語である _____ 語に翻訳された、
この国際出願の翻訳文 (PCT 規則12.3(a) 及び23.1(b))

b. ☐ この国際調査報告は、PCT 規則91の規定により国際調査機関が認めた又は国際調査機関に通知された明らかな誤りの訂正を考慮して作成した (PCT 規則43.6の2(a))。

c. ☐ この国際出願は、ヌクレオチド又はアミノ酸配列を含んでいる (第 I 欄参照)。

2. ☐ 請求の範囲の一部の調査ができない (第 II 欄参照)。

3. ☒ 発明の単一性が欠如している (第 III 欄参照)。

4. 発明の名称は ☒ 出願人が提出したものを承認する。

☐ 次に示すように国際調査機関が作成した。

5. 要約は ☒ 出願人が提出したものを承認する。

☐ 第IV欄に示されているように、法施行規則第47条第1項 (PCT 規則38.2) の規定により国際調査機関が作成した。出願人は、この国際調査報告の発送の日から1月以内にこの国際調査機関に意見を提出することができる。

6. 図面に関して

a. 要約書とともに公表される図は、

第 5 図とする。 ☒ 出願人が示したとおりである。

☐ 出願人は図を示さなかったので、国際調査機関が選択した。

☐ 本図は発明の特徴を一層よく表しているため、国際調査機関が選択した。

b. ☐ 要約とともに公表される図はない。

様式PCT/ISA/210 (第1ページ) (2007年4月) (改訂)

第II欄 請求の範囲の一部の調査ができないときの意見（第1ページの2の続き）

法第8条第3項（PCT17条(2)(a)）の規定により、この国際調査報告は次の理由により請求の範囲の一部について作成しなかった。

1. ☐ 請求項 _____ は、この国際調査機関が調査をすることを要しない対象に係るものである。つまり、
2. ☐ 請求項 _____ は、有意義な国際調査をすることができる程度まで所定の要件を満たしていない国際出願の部分に係るものである。つまり、
3. ☐ 請求項 _____ は、従属請求の範囲であってPCT規則6.4(a)の第2文及び第3文の規定に従って記載されていない。

第III欄 発明の単一性が欠如しているときの意見（第1ページの3の続き）

次に述べるようにこの国際出願に二以上の発明があるとこの国際調査機関は認めた。

請求の範囲に記載されている一群の発明が単一性の要件を満たすためには、その一群の発明を単一の一般的発明概念を形成するようにに関連させるための、特別な技術的特徴の存在が必要であるところ、請求項1-20に記載されている一群の発明は、請求項1に記載された事項でのみ関連している。

しかしながら、この事項は、先行技術文献、例えば、JP 2007-258267 A（株式会社東芝）2007.10.04に記載されているため、特別な技術的特徴とはなり得ない。

そうすると、請求項1-20に記載されている一群の発明の間には、単一の一般的発明概念を形成するようにに関連させるための特別な技術的特徴は存在しないこととなる。

よって、請求項1-20に記載されている一群の発明は、発明の単一性の要件を満たしていない。

1. ☐ 出願人が必要な追加調査手数料をすべて期間内に納付したので、この国際調査報告は、すべての調査可能な請求項について作成した。
2. ☐ 追加調査手数料を要求するまでもなく、すべての調査可能な請求項について調査することができたので、追加調査手数料の納付を求めなかった。
3. ☐ 出願人が必要な追加調査手数料を一部のみしか期間内に納付しなかったため、この国際調査報告は、手数料の納付のあった次の請求項のみについて作成した。
4. ☒ 出願人が必要な追加調査手数料を期間内に納付しなかったため、この国際調査報告は、請求の範囲の最初に記載されている発明に係る次の請求項について作成した。

請求項 1, 2

追加調査手数料の異議の申立てに関する注意

- ☐ 追加調査手数料及び、該当する場合には、異議申立手数料の納付と共に、出願人から異議申立てがあった。
- ☐ 追加調査手数料の納付と共に出願人から異議申立てがあったが、異議申立手数料が納付命令書に示した期間内に支払われなかった。
- ☐ 追加調査手数料の納付はあったが、異議申立てはなかった。

様式PCT/ISA/210（第1ページの続葉（2））（2007年4月）

特許協力条約に基づく国際出願願書

紙面による写し (注意 電子データが原本となります)

0	受理官庁記入欄	
0-1	国際出願番号	
0-2	国際出願日	
0-3	(受付印)	
0-4	様式 PCT/RO/101 この特許協力条約に基づく国際出願願書は、	
0-4-1	右記によって作成された。	PCT-SAFE Version 3.51.032.207 MT/FOP 20080917/0.20.5.12
0-5	申立て 出願人は、この国際出願が特許協力条約に従って処理されることを請求する。	
0-6	出願人によって指定された受理官庁	日本国特許庁 (RO/JP)
0-7	出願人又は代理人の書類記号	P051653P0
I	発明の名称	半導体装置及びその製造方法
II	出願人	
II-1	この欄に記載した者は	出願人である (applicant only)
II-2	右の指定国についての出願人である。	米国を除く全ての指定国 (all designated States except US)
II-4ja	名称	パナソニック株式会社
II-4en	Name:	PANASONIC CORPORATION
II-5ja	あて名	5718501 日本国
II-5en	Address:	大阪府門真市大字門真 1 0 0 6 番地 1006, Oaza Kadoma, Kadoma-shi, Osaka 5718501 Japan
II-6	国籍 (国名)	日本国 JP
II-7	住所 (国名)	日本国 JP
II-8	電話番号	06-6908-1473
II-9	ファクシミリ番号	06-6909-0053
III-1	その他の出願人又は発明者	
III-1-1	この欄に記載した者は	出願人及び発明者である (applicant and inventor)
III-1-2	右の指定国についての出願人である。	米国のみ (US only)
III-1-4ja	氏名 (姓名)	佐藤好弘
III-1-4en	Name (LAST, First):	SATO, Yoshihiro
III-1-5ja	あて名	
III-1-5en	Address:	
III-1-6	国籍 (国名)	
III-1-7	住所 (国名)	

特許協力条約に基づく国際出願願書

紙面による写し (注意 電子データが原本となります)

III-2	その他の出願人又は発明者	
III-2-1	この欄に記載した者は	出願人及び発明者である (applicant and inventor)
III-2-2	右の指定国についての出願人である。	米国のみ (US only)
III-2-4ja	氏名(姓名)	小川久
III-2-4en	Name (LAST, First):	OGAWA, Hisashi
III-2-5ja	あて名	
III-2-5en	Address:	
III-2-6	国籍(国名)	
III-2-7	住所(国名)	
IV-1	代理人又は共通の代表者、通知のあて名 下記の者は国際機関において右記のごとく出願人のために行動する。	代理人 (agent)
IV-1-1ja	氏名(姓名)	前田弘
IV-1-1en	Name (LAST, First):	MAEDA, Hiroshi
IV-1-2ja	あて名	5410053 日本国 大阪府大阪市中央区本町2丁目5番7号 大阪丸紅ビル
IV-1-2en	Address:	Osaka-Marubeni Bldg., 5-7, Hommachi 2-chome, Chuo-ku, Osaka-shi, Osaka 5410053 Japan
IV-1-3	電話番号	06-6125-2255
IV-1-4	ファクシミリ番号	06-6125-2288
IV-1-6	代理人登録番号	100077931
IV-2	その他の代理人	筆頭代理人と同じあて名を有する代理人 (additional agent(s) with the same address as first named agent)
IV-2-1ja	氏名	竹内宏(100110939); 今江克実(100115059); 原田智雄(100117710)
IV-2-1en	Name(s)	TAKEUCHI, Hiroshi(100110939); IMAE, Katsumi(100115059); HARADA, Tomoo(100117710)
V	国の指定	
V-1	この願書を用いてされた国際出願は、規則4.9(a)に基づき、国際出願の時点で拘束される全てのPCT締約国を指定し、取得しうるあらゆる種類の保護を求め、及び該当する場合には広域と国内特許の両方を求める国際出願となる。	
V-2	V-2欄は、国際出願が出願時に特定の国における先の国内出願を優先権主張の基礎とする場合に、この先の国内出願の効果が国内法令に基づいて消滅することを避けることを目的として、当該国の指定を除外する(取消し不可)ためにのみ使用される。これらの国々における国内法令の関連規定による法的効果については「PCT出願人の手引き」第I巻Aの附属書B1を参照。	JP
VI-1	先の国内出願に基づく優先権主張	
VI-1-1	出願日	2008年 03月 13日 (13. 03. 2008)
VI-1-2	出願番号	2008-064435
VI-1-3	国名	日本国 JP

特許協力条約に基づく国際出願願書

紙面による写し (注意 電子データが原本となります)

VI-2	優先権証明書送付の請求 上記の先の出願のうち、右記の番号のものについては、出願書類の認証謄本を作成し国際事務局へ送付することを、受理官庁に対して請求している。	VI-1	
VI-3	引用による補充： 条約第11条(1)(iii)(d)若しくは(e)に規定する国際出願の要素の全部、又は規則20.5(a)に規定する明細書、請求の範囲若しくは図面の一部がこの国際出願には含まれていないが、受理官庁が条約第11条(1)(ii)に規定する要素の1つ以上を最初に受領した日において優先権を主張する先の出願にそれが完全に含まれている場合には、規則20.6に基づく確認の手続を条件として、その要素又は部分を規則20.6の規定によりこの国際出願に引用して補充することを請求する。		
VII-1	特定された国際調査機関(ISA)	日本国特許庁 (ISA/JP)	
VIII	申立て	申立て数	
VIII-1	発明者の特定に関する申立て	—	
VIII-2	出願し及び特許を与えられる国際出願日における出願人の資格に関する申立て	—	
VIII-3	先の出願の優先権を主張する国際出願日における出願人の資格に関する申立て	—	
VIII-4	発明者である旨の申立て(米国を指定国とする場合)	—	
VIII-5	不利にならない開示又は新規性喪失の例外に関する申立て	—	
IX	照合欄	用紙の枚数	添付された電子データ
IX-1	願書(申立てを含む)	4	✓
IX-2	明細書	48	✓
IX-3	請求の範囲	6	✓
IX-4	要約	1	✓
IX-5	図面	14	✓
IX-7	合計	73	
	添付書類	添付	添付された電子データ
IX-8	手数料計算用紙	—	✓
IX-18	PCT-SAFE 電子出願	—	—
IX-20	要約とともに提示する図の番号	5	
IX-21	国際出願の使用言語名	日本語	
X-1	出願人、代理人又は代表者の記名押印	(PKCS7 デジタル署名)	
X-1-1	氏名(姓名)	前田弘	
X-1-2	署名者の氏名		
X-1-3	権限		

特許協力条約に基づく国際出願願書

紙面による写し(注意 電子データが原本となります)

受理官庁記入欄

10-1	国際出願として提出された書類 の実際の受理の日	
10-2	図面	
10-2-1	受理された	
10-2-2	不足図面がある	
10-3	国際出願として提出された書類 を補充する書類又は図面であつ てその後期間内に提出されたも のの実際の受理の日(訂正日)	
10-4	特許協力条約第11条(2)に基づ く必要な補充の期間内の受理の日	
10-5	出願人により特定された国際調査機関	ISA/JP
10-6	調査手数料未払いにつき、国際 調査機関に調査用写しを送付していない	

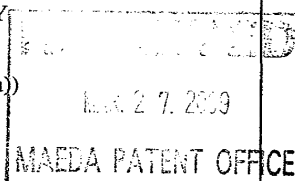
国際事務局記入欄

11-1	記録原本の受理の日	
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From the INTERNATIONAL BUREAU

PCTNOTIFICATION OF RECEIPT OF
RECORD COPY

(PCT Rule 24.2(a))



To:

MAEDA, Hiroshi
Osaka-Marubeni Bldg., 5-7, Hommachi 2-chome,
Chuo-ku, Osaka-shi, Osaka
5410053
JAPON

Date of mailing (day/month/year) 13 March 2009 (13.03.2009)	IMPORTANT NOTIFICATION
Applicant's or agent's file reference P051653P0 <i>M08OK585CT/</i>	International application No. PCT/JP2009/000574

The applicant is hereby **notified** that the International Bureau has received the record copy of the international application as detailed below.

Name(s) of the applicant(s) and State(s) for which they are applicants:

PANASONIC CORPORATION (for all designated States except US)
SATO, Yoshihiro et al (for US)

International filing date: 13 February 2009 (13.02.2009)
Priority date(s) claimed: 13 March 2008 (13.03.2008)
Date of receipt of the record copy by the International Bureau: 26 February 2009 (26.02.2009)
List of designated Offices:

AP: BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW
EA: AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
EP: AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR
OA: BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG
Additional: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW

ATTENTION: The applicant should carefully check the data appearing in this notification. In case of any discrepancy between these data and the indications in the international application, the applicant should immediately inform the International Bureau. **In addition, the applicant's attention is drawn to the information contained in the Annex, relating to:**

- time limits for entry into the national phase - **see updated important information (as of April 2002)**
- requirements regarding priority documents (if applicable)

A copy of this notification is being sent to the receiving Office and to the International Searching Authority.

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland	Authorized officer Hennequin Francoise e-mail pt08.pct@wipo.int Telephone No. +41 22 338 74 08
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Facsimile No. +41 22 338 70 10

Form PCT/IB/301 (October 2005)

1/DZM2G2OF0

INFORMATION ON ENTERING THE NATIONAL PHASE

The applicant is reminded that the **"national phase"** must be entered before each of the designated Offices indicated on the cover sheet of this notification by paying national fees and furnishing translations, as prescribed by Articles 22 and 39 and the applicable national laws. In addition, the applicant may also have to comply with **other special requirements** applicable in certain Offices. It is the **applicant's responsibility** to ensure that the necessary steps to enter the national phase are taken in a timely fashion. Most Offices do not issue reminders to applicants in connection with the entry into the national phase.

The **applicable time limit** for entering the national phase will, **subject to what is said in the following paragraph**, be **30 MONTHS** from the priority date, not only in respect of any elected Office if a demand for international preliminary examination is filed before the expiration of 19 months from the priority date (see Article 39(1)), but also in respect of any designated Office, in the absence of filing of such demand, where Article 22(1) as modified with effect from 1 April 2002 applies in respect of that designated Office. For further details, see *PCT Gazette* No. 44/2001 of 1 November 2001, pages 19926, 19932 and 19934, as well as the *PCT Newsletter*, October and November 2001 and February 2002 issues.

In practice, **time limits other than the 30-month time limit will continue to apply, for various periods of time**, in respect of certain designated or elected Offices. For **regular updates on the applicable time limits (20, 21, 30 or 31 months, or other time limit)**, Office by Office, refer to the *PCT Gazette* ("Section IV" part published on a weekly basis), to the *PCT Newsletter* (on a monthly basis) and to the relevant National Chapters in Volume II of the *PCT Applicant's Guide* (the paper version of which is updated usually twice a year and the Internet version of which is updated usually on a weekly basis). Finally, a cumulative table of all applicable time limits for entering the national phase is available from WIPO's Internet site, via links from various pages of the site, including those of the *Gazette*, *Newsletter* and *Guide*, at <http://www.wipo.int/pct/en/index.html>.

Information about the requirements for **filing a demand for international preliminary examination** is set out in the *PCT Applicant's Guide*, Volume I/A, Chapter IX. Note that only an applicant who is a national or resident of a PCT Contracting State which is bound by Chapter II has the right to file a demand for international preliminary examination (at present, all PCT Contracting States are bound by Chapter II).

REQUIREMENTS REGARDING PRIORITY DOCUMENTS

For applicants who have not yet complied with the requirements regarding priority documents, the following is recalled.

Where the priority of an earlier national, regional or international application is claimed, the applicant must submit a copy of the said earlier application, certified by the authority with which it was filed ("the priority document") to the receiving Office (which will transmit it to the International Bureau) or directly to the International Bureau, before the expiration of 16 months from the priority date, provided that any such priority document may still be submitted to the International Bureau before the date of international publication of the international application, in which case that document will be considered to have been received by the International Bureau on the last day of the 16-month time limit (Rule 17.1(a)).

Where the priority document is issued by the receiving Office, the applicant may, instead of submitting the priority document, request the receiving Office to prepare and transmit the priority document to the International Bureau. Such request must be made before the expiration of the 16-month time limit and may be subjected by the receiving Office to the payment of a fee (Rule 17.1(b)).

If the priority document concerned is not submitted to the International Bureau and if the request to the receiving Office to prepare and transmit the priority document has not been made (and the corresponding fee, if any, paid) within the applicable time limit indicated under the preceding paragraphs, any designated State may disregard the priority claim, provided that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances (Rule 17.1(c)).

Where several priorities are claimed, the priority date to be considered for the purposes of computing the 16-month time limit (and all other PCT time limits) is the filing date of the earliest application whose priority is claimed (Article 2(xi)(b)).

From the INTERNATIONAL BUREAU

PCTNOTIFICATION CONCERNING
SUBMISSION OR TRANSMITTAL
OF PRIORITY DOCUMENT

(PCT Administrative Instructions, Section 411)

To:

MAEDA, Hiroshi
Osaka-Marubeni Bldg., 5-7 Hommachi 2-chome
Chuo-ku, Osaka-shi, Osaka
5410053
JAPONRECEIVED
APR 21 2009
MAEDA PATENT OFFICE

Date of mailing (day/month/year) 06 April 2009 (06.04.2009)		
Applicant's or agent's file reference P051653P0 M08OK585CTI	IMPORTANT NOTIFICATION	
International application No. PCT/JP2009/000574	International filing date (day/month/year) 13 February 2009 (13.02.2009)	
International publication date (day/month/year) Not yet published	Priority date (day/month/year) 13 March 2008 (13.03.2008)	
Applicant PANASONIC CORPORATION et al		

- By means of this Form, which replaces any previously issued notification concerning submission or transmittal of priority documents, the applicant is hereby notified of the date of receipt by the International Bureau of the priority document(s) relating to all earlier application(s) whose priority is claimed. Unless otherwise indicated by the letters "NR", in the right-hand column or by an asterisk appearing next to a date of receipt, the priority document concerned was submitted or transmitted to the International Bureau in compliance with Rule 17.1(a) or (b).
- (If applicable)* The letters "NR" appearing in the right-hand column denote a priority document which, on the date of mailing of this Form, had not yet been received by the International Bureau under Rule 17.1(a) or (b). Where, under Rule 17.1(a), the priority document must be submitted by the applicant to the receiving Office or the International Bureau, but the applicant fails to submit the priority document within the applicable time limit under that Rule, the attention of the applicant is directed to Rule 17.1(c) which provides that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances.
- (If applicable)* An asterisk (*) appearing next to a date of receipt, in the right-hand column, denotes a priority document submitted or transmitted to the International Bureau but not in compliance with Rule 17.1(a) or (b) (the priority document was received after the time limit prescribed in Rule 17.1(a) or the request to prepare and transmit the priority document was submitted to the receiving Office after the applicable time limit under Rule 17.1(b)). Even though the priority document was not furnished in compliance with Rule 17.1(a) or (b), the International Bureau will nevertheless transmit a copy of the document to the designated Offices, for their consideration. In case such a copy is not accepted by the designated Office as the priority document, Rule 17.1(c) provides that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances.

<u>Priority date</u>	<u>Priority application No.</u>	<u>Country or regional Office or PCT receiving Office</u>	<u>Date of receipt of priority document</u>
13 March 2008 (13.03.2008)	2008-064435	JP	26 March 2009 (26.03.2009)

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland	Authorized officer Masashi Honda e-mail PT08.PCT@WIPO.INT Telephone No. +41 22 338 74 08
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Facsimile No. +41 22 338 82 70

Form PCT/IB/304 (October 2005)

1/D0HRNQ4B0

特許協力条約



発信人 日本国特許庁（国際調査機関）

代理人 前田弘 様 あて名 〒541-0053 日本国大阪府大阪市中央区本町2丁目5番7号 大 阪丸紅ビル		PCT 国際調査機関の見解書 （法施行規則第40条の2） [PCT規則43の2.1]	
		発送日 （日.月.年） 19.05.2009	
出願人又は代理人 の書類記号 P051653P0		今後の手続きについては、下記2を参照すること。	
国際出願番号 PCT/J P 2009/000574	国際出願日 （日.月.年） 13.02.2009	優先日 （日.月.年） 13.03.2008	
国際特許分類（IPC）Int.Cl. H01L21/8238(2006.01)i, H01L21/28(2006.01)i, H01L21/336(2006.01)i, H01L27/092(2006.01)i, H01L29/423(2006.01)i, H01L29/49(2006.01)i, H01L29/78(2006.01)i			
出願人（氏名又は名称） パナソニック株式会社			

1. この見解書は次の内容を含む。 ☒ 第I欄 見解の基礎 ☐ 第II欄 優先権 ☐ 第III欄 新規性、進歩性又は産業上の利用可能性についての見解の不作成 ☒ 第IV欄 発明の単一性の欠如 ☒ 第V欄 PCT規則43の2.1(a)(i)に規定する新規性、進歩性又は産業上の利用可能性についての見解、それを裏付けるための文献及び説明 ☐ 第VI欄 ある種の引用文献 ☐ 第VII欄 国際出願の不備 ☐ 第VIII欄 国際出願に対する意見	
2. 今後の手続き 国際予備審査の請求がされた場合は、出願人がこの国際調査機関とは異なる国際予備審査機関を選択し、かつ、その国際予備審査機関がPCT規則66.1の2(b)の規定に基づいて国際調査機関の見解書を国際予備審査機関の見解書とみなさない旨を国際事務局に通知していた場合を除いて、この見解書は国際予備審査機関の最初の見解書とみなされる。 この見解書が上記のように国際予備審査機関の見解書とみなされる場合、様式PCT/ISA/220を送付した日から3月又は優先日から2月のうちいずれか遅く満了する期限が経過するまでに、出願人は国際予備審査機関に、適当な場合は補正書とともに、答弁書を提出することができる。 さらに選択肢は、様式PCT/ISA/220を参照すること。	
3. さらなる詳細は、様式PCT/ISA/220の備考を参照すること。	

見解書を作成した日 01.05.2009	
名称及びあて先 日本国特許庁（ISA/J P） 郵便番号100-8915 東京都千代田区霞が関三丁目4番3号	特許庁審査官（権限のある職員） 宇多川 勉 電話番号 03-3581-1101 内線 3498

様式PCT/ISA/237（表紙）（2007年4月）

第 I 欄 見解の基礎

1. 言語に関し、この見解書は以下のものに基づき作成した。

- ☒ 出願時の言語による国際出願
☐ 出願時の言語から国際調査のための言語である _____ 語に翻訳された、この国際出願の翻訳文
(PCT規則12.3(a)及び23.1(b))

2. ☐ この見解書は、PCT規則 91 の規定により国際調査機関が認めた又は国際調査機関に通知された明らかな誤りの訂正を考慮して作成した (PCT規則 43 の 2.1(b))。

3. この国際出願で開示されたヌクレオチド又はアミノ酸配列に関して、以下に基づき見解書を作成した。

- a. タイプ ☐ 配列表
☐ 配列表に関連するテーブル
b. フォーマット ☐ 紙形式
☐ 電子形式
c. 提出時期 ☐ 出願時の国際出願に含まれていたもの
☐ この国際出願と共に電子形式により提出されたもの
☐ 出願後に、調査のために、この国際調査機関に提出されたもの

4. ☐ さらに、配列表又は配列表に関連するテーブルを提出した場合に、出願後に提出した配列若しくは追加して提出した配列が出願時に提出した配列と同一である旨、又は、出願時の開示を超える事項を含まない旨の陳述書の提出があった。

5. 補足意見：

第IV欄 発明の単一性の欠如

1. ☒ 追加手数料の納付命令書（様式PCT/ISA/206）に対して、出願人は、規定期間内に、
- ☐ 追加手数料を納付した。
- ☐ 追加手数料及び、該当する場合には、異議申立手数料の納付と共に、異議を申し立てた。
- ☐ 追加手数料の納付と共に異議を申し立てたが、規定の異議申立手数料を支払わなかった。
- ☒ 追加手数料を納付しなかった。
2. ☐ 国際調査機関は、発明の単一性の要件を満たしていないと判断したが、追加手数料の納付を出願人に求めないこととした。
3. 国際調査機関は、PCT規則13.1、13.2及び13.3に規定する発明の単一性を次のように判断する。

☐ 満足する。

☒ 以下の理由により満足しない。

請求の範囲に記載されている一群の発明が単一性の要件を満たすためには、その一群の発明を単一の一般的発明概念を形成するように連関させるための、特別な技術的特徴の存在が必要であるところ、請求項1-20に記載されている一群の発明は、請求項1に記載された事項でのみ連関している。

しかしながら、この事項は、先行技術文献、例えば、JP 2007-258267 A（株式会社東芝）2007.10.04に記載されているため、特別な技術的特徴とはなり得ない。

そうすると、請求項1-20に記載されている一群の発明の間には、単一の一般的発明概念を形成するように連関させるための特別な技術的特徴は存在しないこととなる。

よって、請求項1-20に記載されている一群の発明は、発明の単一性の要件を満たしていない。

次に、この国際出願の請求の範囲に記載されている、一般的発明概念を形成するように連関している発明の群の数、すなわち、発明の数について検討する。

請求項1-20に記載されている一群の発明の間には、上記のとおり、単一の一般的発明概念を形成するように連関させるための特別な技術的特徴は存在しない。

そうすると、この国際出願の請求の範囲には、少なくとも、請求項1、2、請求項3、請求項4、請求項5、請求項6、請求項7、請求項8、請求項9、請求項10、11、請求項12、13、請求項14、請求項15～20に区分される12個の発明が記載されている。

4. したがって、国際出願の次の部分について、この見解書を作成した。

☐ すべての部分

☒ 請求項 1, 2 に関する部分

様式PCT/ISA/237（第IV欄）（2007年4月）

第Ⅴ欄 新規性、進歩性又は産業上の利用可能性についてのPCT規則43の2.1(a)(i)に定める見解、それを裏付ける文献及び説明

1. 見解

新規性 (N)	請求項		有
	請求項	1, 2	無
進歩性 (I S)	請求項		有
	請求項	1, 2	無
産業上の利用可能性 (I A)	請求項	1, 2	有
	請求項		無

2. 文献及び説明

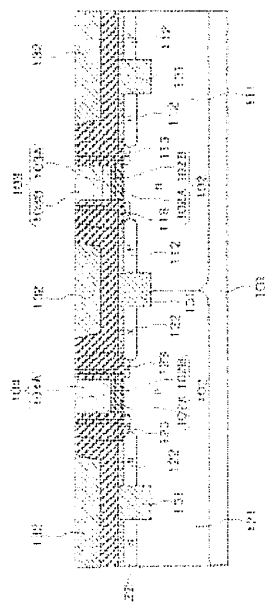
文献1 : JP 2007-258267 A (株式会社東芝) 2007.10.04, 全文, 全図

請求項1, 2に係る発明は、国際調査報告で引用された文献1に記載されているので、新規性、進歩性を有さない。

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR**Publication number:** JP2007258267 (A)**Publication date:** 2007-10-04**Inventor(s):** AOYAMA TOMONORI**Applicant(s):** TOSHIBA CORP**Classification:****- international:** H01L21/8238; H01L21/336; H01L27/092; H01L29/423;
H01L29/49; H01L29/78; H01L21/70; H01L21/02;
H01L27/085; H01L29/40; H01L29/66**- European:** H01L21/8238G4; H01L21/336U**Application number:** JP20060077525 20060320**Priority number(s):** JP20060077525 20060320**Also published as:** US2007215950 (A1)**Abstract of JP 2007258267 (A)**

PROBLEM TO BE SOLVED: To provide a semiconductor device with a p-type FET and an n-type FET that comprise a gate insulating film and a gate electrode having appropriate characteristics. ;

SOLUTION: A gate insulating film is formed on a substrate in a p-type FET formation schedule region and an n-type FET formation schedule region, and a gate electrode layer for a p-type FET is formed on the gate insulating film. The gate electrode layer for a p-type FET is processed in the p-type FET formation schedule region and the n-type FET formation schedule region, so as to form a gate electrode for a p-type FET in the p-type FET formation schedule region and to form a dummy gate electrode in the n-type FET formation schedule region. Then, the dummy gate electrode is removed from the gate insulating film in the n-type FET formation schedule to form a groove therein, and the groove is filled with a gate electrode material, thereby forming the gate electrode for an n-type FET on the gate insulating film. ; COPYRIGHT: (C) 2008,JPO&INPIT



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PATENT ABSTRACTS OF JAPAN

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(21)Application number : 2000-306457

(71)Applicant : TOSHIBA CORP

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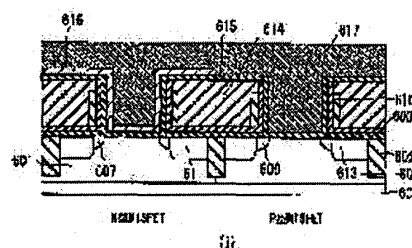
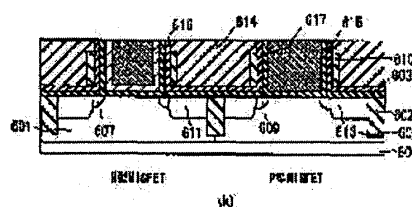
(72)Inventor : AKASAKA YASUSHI

(54) SEMICONDUCTOR DEVICE AND ITS FABRICATING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To fabricate a MISFET having a low threshold voltage by employing materials having optimal work functions in the metal gate electrode of a p-type MISFET and an n-type MISFET.

SOLUTION: The gate electrode of an N type MIS transistor has a first metal film 616 touching a gate insulation film 615 and having a work function ϕ_{mf} in the range of $V_{\text{th}}+3.9 \leq \phi_{\text{mf}} \leq V_{\text{th}}+4.1$, where V_{th} is a threshold voltage. The gate electrode of a P type MIS transistor has a second metal film 617 touching the gate insulation film 615 and having a work function ϕ_{mf} in the range of $5.1+V_{\text{th}} \leq \phi_{\text{mf}} \leq 5.3+V_{\text{th}}$, where V_{th} is the threshold voltage.



(19) 日本国特許庁 (J P)

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27/092			3 0 1 R 5 F 0 4 8
21/28		27/08	3 2 1 D
	3 0 1	29/62	G
29/43			
審査請求 未請求 請求項の数3 O L (全 10 頁)			

(21) 出願番号 特願2000-306457(P2000-306457)

(22) 出願日 平成12年10月5日 (2000. 10. 5)

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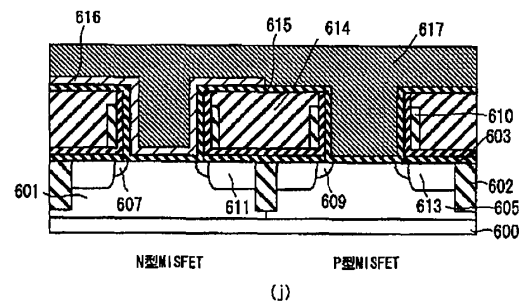
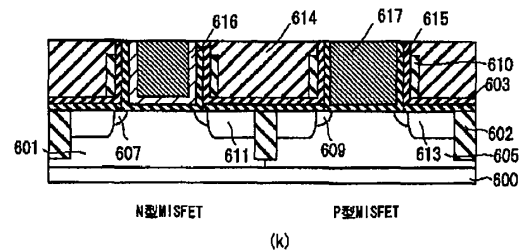
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(54) 【発明の名称】 半導体装置及びその製造方法

(57) 【要約】

【課題】 p型MISFET及びn型MISFETの金属ゲート電極として、それぞれ最適な仕事関数を有する材料を用い、低しきい値電圧のMISFETを形成する。

【解決手段】 N型MISトランジスタのゲート電極は、ゲート絶縁膜615に接し、仕事関数 ϕ_f が、閾値電圧 V_{th} に対し、 $V_{th}+3.9 \leq \phi_f \leq V_{th}+4.1$ である第1の金属膜616を具備し、P型MISトランジスタのゲート電極は、ゲート絶縁膜615に接し、仕事関数 ϕ_f が、 $5.1+V_{th} \leq \phi_f \leq 5.3+V_{th}$ である第2の金属膜617を具備してなる。



【特許請求の範囲】

【請求項1】N型MISトランジスタ及びP型MISトランジスタが形成された半導体装置であって、前記N型MISトランジスタのゲート電極は、ゲート絶縁膜に接し、仕事関数 ϕ_f [eV] が、閾値電圧 V_{th} [V] に対し、 $V_{th} + 3.9 \leq \phi_f \leq V_{th} + 4.1$ である第1の金属含有膜を具備し、前記P型MISトランジスタのゲート電極は、前記ゲート絶縁膜に接し、仕事関数 ϕ_f [eV] が、前記閾値電圧 V_{th} [V] に対し、 $5.1 + V_{th} \leq \phi_f \leq 5.3 + V_{th}$ である第2の金属含有膜を具備してなることを特徴とする半導体装置。

【請求項2】N型MISトランジスタ及びP型MISトランジスタそれぞれのゲート電極を半導体基板上の絶縁膜に形成された開口部内にゲート絶縁膜を介して形成する半導体装置の製造方法であって、前記ゲート電極を形成する工程は、N型MISトランジスタ用の第1のゲート形成領域及びP型MISトランジスタ用の第2のゲート形成領域の双方の領域の開口部内に形成されたゲート絶縁膜上に、仕事関数 ϕ_f [eV] が、閾値電圧 V_{th} [V] に対し、 $V_{th} + 3.9 \leq \phi_f \leq V_{th} + 4.1$ の条件を満たす第1の金属含有膜を形成する工程と、第2のゲート形成領域に形成された第1の金属含有膜を除去する工程と、第1のゲート形成領域の第1の金属含有膜上、及び第2のゲート形成領域のゲート絶縁膜上に、仕事関数 ϕ_f [eV] が、前記閾値電圧 V_{th} [V] に対し、 $5.1 + V_{th} \leq \phi_f \leq 5.3 + V_{th}$ の条件を満たす第2の金属含有膜を形成する工程とを含むことを特徴とする半導体装置の製造方法。

【請求項3】N型MISトランジスタ及びP型MISトランジスタそれぞれのゲート電極をシリコン基板上の絶縁膜に形成された開口部内にゲート絶縁膜を介して形成する半導体装置の製造方法であって、前記ゲート電極を形成する工程は、N型MISトランジスタ用の第1のゲート形成領域及びP型MISトランジスタ用の第2のゲート形成領域の双方の領域の開口部内に形成されたゲート絶縁膜上に、第1の金属含有膜を形成する工程と、第1及び第2のゲート形成領域の少なくとも一方の領域の第1の金属含有膜に対して所定の処理を行い、第1の金属含有膜の仕事関数 ϕ_f [eV] が、閾値電圧 V_{th} [V] に対し、第1のゲート形成領域において、 $V_{th} + 3.9 \leq \phi_f \leq V_{th} + 4.1$ 、の条件を満たすと共に、第2のゲート形成領域において、 $5.1 + V_{th} \leq \phi_f \leq 5.3 + V_{th}$ 、の条件を満たすようにすることを特徴とする半導体装置の製造方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、半導体装置及びその製造方法、特にN型MISトランジスタ及びP型MISトランジスタのゲート電極の改良に関するものである。

【0002】

【従来の技術】微細なMISFETに於いて低いしきい値を実現するために、N型MISFET、P型MISFETそれぞれに対して異なる仕事関数のゲート電極を用いることが行われている。従来、ゲート電極には多結晶シリコンが用いられており、N型MISFET、P型MISFETそれぞれの多結晶シリコン（ゲート電極）に対してドーピングし、 n^+ 、 p^- 型にし、それぞれの多結晶シリコンの仕事関数を伝導帯（Conduction Band）と価電子帯（Valence Band）の近傍に設定することで、低いしきい値を容易に実現することができる。

【0003】しかし、多結晶シリコンからなるゲート電極は、不純物濃度が導電性不純物の固溶限である 10^{20} cm^{-3} 台になるように高濃度にドーピングしても、ゲート電極側に空乏層が形成されるために、ゲート容量はその分減少する。このことは、特にP型MISFETに於いて深刻な問題になる。B（ボロン）がドーピングされた p^+ 型多結晶シリコンからは、熱工程によって、Bがゲート絶縁膜を通過してチャネル領域まで拡散することが知られている。

【0004】この現象による制約を受けるため、 p^+ 型多結晶シリコン・ゲート電極では、Bを高濃度にドーピングすることができず、ゲートの空乏化によるゲート容量の低下は n^+ 型多結晶シリコン・ゲート電極の場合より一層深刻である。

【0005】このゲート電極の空乏化を防止するために、ゲート電極に金属を用いる検討が行われている。しかし、一般に n^+ 、 p^+ 多結晶シリコンと同様の効果を得るために、シリコンのバンドギャップ中央から上下に0.56 eV程度離れた仕事関数を有する金属材料で、耐熱性、耐酸化性などの観点からLSIプロセスと整合性の良い材料を選択することは非常に難しい。

【0006】そこで、基板のバンドギャップ中央の近傍に位置する仕事関数を持った種類の金属を用いる方法が現実的と考えられている。しかしながら、上述したように仕事関数が基板のバンドギャップの中央に位置する金属ゲート電極を用いると、低いしきい値を得ることが難しい。チャネル表面に逆導電型の不純物をドーピングし（カウンタードーピング）、埋め込みチャネルを形成することにより低いしきい値を実現することができる。しかし、埋め込みチャネルでは、ゲート絶縁膜とシリコン基板の界面にチャネルが形成されるのではなく、界面から基板奥に入ったところにチャネルが形成される。これは実効的なゲート絶縁膜厚が増加していることになり、ショートチャネル効果を抑制することが難しく、また、

S-factorが劣化するという問題がある。

【0007】

【発明が解決しようとする課題】上述したように、p型MISFET及びn型MISFETの金属ゲート電極に、仕事関数が基板のバンドギャップの中央に位置する材料を用いると、低しきい値を得ることが難しいという問題があった。

【0008】本発明の目的は、p型MISFET及びn型MISFETの金属ゲート電極として、それぞれ最適な仕事関数を有する材料を用い、低しきい値電圧のMISFETを形成することが可能な半導体装置及びその製造方法を提供することにある。

【0009】

【課題を解決するための手段】〔構成〕本発明は、上記目的を達成するために以下のように構成されている。

【0010】(1)本発明(請求項1)は、N型MISトランジスタ及びP型MISトランジスタが形成された半導体装置であって、前記N型MISトランジスタのゲート電極は、ゲート絶縁膜に接し、仕事関数 ϕ_f [eV]が、閾値電圧 V_{th} [V]に対し、 $V_{th}+3.9 \leq \phi_f \leq V_{th}+4.1$ である第1の金属含有膜を具備し、前記P型MISトランジスタのゲート電極は、前記ゲート絶縁膜に接し、仕事関数 ϕ_f [eV]が、前記閾値電圧 V_{th} [V]に対し、 $5.1+V_{th} \leq \phi_f \leq 5.3+V_{th}$ である第2の金属含有膜を具備してなることを特徴とする。

【0011】(2)本発明(請求項2)は、N型MISトランジスタ及びP型MISトランジスタそれぞれのゲート電極を半導体基板上の絶縁膜に形成された開口部内にゲート絶縁膜を介して形成する半導体装置の製造方法であって、前記ゲート電極を形成する工程は、N型MISトランジスタ用の第1のゲート形成領域及びP型MISトランジスタ用の第2のゲート形成領域の双方の領域の開口部内に形成されたゲート絶縁膜上に、仕事関数 ϕ_f [eV]が、閾値電圧 V_{th} [V]に対し、 $V_{th}+3.9 \leq \phi_f \leq V_{th}+4.1$ の条件を満たす第1の金属含有膜を形成する工程と、第2のゲート形成領域に形成された第1の金属含有膜を除去する工程と、第1のゲート形成領域の第1の金属含有膜上、及び第2のゲート形成領域のゲート絶縁膜上に、仕事関数 ϕ_f [eV]が、前記閾値電圧 V_{th} [V]に対し、 $5.1+V_{th} \leq \phi_f \leq 5.3+V_{th}$ の条件を満たす第2の金属含有膜を形成する工程とを含むことを特徴とする。

【0012】(3)本発明(請求項3)は、N型MISトランジスタ及びP型MISトランジスタそれぞれのゲート電極をシリコン基板上の絶縁膜に形成された開口部内にゲート絶縁膜を介して形成する半導体装置の製造方法であって、前記ゲート電極を形成する工程は、N型MISトランジスタ用の第1のゲート形成領域及びP型MISトランジスタ用の第2のゲート形成領域の双方の領

域の開口部内に形成されたゲート絶縁膜上に、第1の金属含有膜を形成する工程と、第1及び第2のゲート形成領域の少なくとも一方の領域の第1の金属含有膜に対して所定の処理を行い、第1の金属含有膜の仕事関数 ϕ_f [eV]が、閾値電圧 V_{th} [V]に対し、第1のゲート形成領域において、 $V_{th}+3.9 \leq \phi_f \leq V_{th}+4.1$ 、

1、の条件を満たすと共に、第2のゲート形成領域において、 $5.1+V_{th} \leq \phi_f \leq 5.3+V_{th}$ の条件を満たすようにすることを特徴とする。

【0013】〔作用〕本発明は、上記構成によって以下の作用・効果を有する。

【0014】N型MISトランジスタのゲート電極は、ゲート絶縁膜に接し、仕事関数 ϕ_f が、閾値電圧 V_{th} に対し、 $V_{th}+3.9 \leq \phi_f \leq V_{th}+4.1$ eVである第1の金属含有膜を具備し、P型MISトランジスタのゲート電極は、ゲート絶縁膜に接し、仕事関数 ϕ_f が、 $5.1+V_{th} \leq \phi_f \leq 5.3+V_{th}$ である第2の金属含有膜を具備することによって、低しきい値電圧のN型及びP型MISFETを得ることができる。また、N型及びP型MISFETは、ショートチャネル効果を抑制し、S-factorの値の低い良好なMISFETを得ることができる。

【0015】

【発明の実施の形態】本発明の実施の形態を以下に図面を参照して説明する。

【0016】〔第1実施形態〕先ず、本発明者は、金属ゲート電極を用いて低しきい値電圧のMISFETに対して必要な条件を調べるために、MISFETに対してシミュレーションを行った。

【0017】シミュレーションに用いたN型MISFETの構成を図1に示す。図1は、シミュレーションに用いたトランジスタの構造を示す模式図である。

【0018】図1において、100はシリコン基板、101はソース/ドレイン、102はエクステンション領域、103はチャネル領域、104はカウンタードーピング領域、105はゲート絶縁膜、106はゲート電極、106はゲート側壁絶縁膜である。

【0019】シミュレーションに用いたパラメータを以下に示す。

【0020】ゲート長： $L=95\text{ nm}$

ゲート絶縁膜のシリコン酸化膜換算膜厚： $T_{ox}=2.4\text{ nm}$

ゲート側壁絶縁膜厚さ： 70 nm

接合深さ： $x_j=35\text{ nm}$

チャネルカウンタードープ深さ： $D_c=30\text{ nm}$

チャネルの不純物平均濃度： $N_p=5 \times 10^{18}\text{ cm}^{-3}$

ゲート電圧： $V_d=1.2\text{ V}$

図1に示す、N型MISFETに対して、ゲート電極の仕事関数を変えてトランジスタ特性のシミュレーションを行った。上述したパラメータのもとで、ゲート電極の

仕事関数 $\phi_f = 4.2 \sim 4.7$ eV の範囲全てに対し、 $V_{th} = 0.395$ V になるようにチャネルカウンタードープの不純物濃度 N_c を調節した。 $\phi_f = 4.6$ eV がバンドギャップ中央である。

【0021】図2にゲート電極の仕事関数とカウンターチャネルの濃度の関係を示す。図2の縦軸（カウンターチャネル濃度）において、+側はチャネル表面をp型にドーピングしていることを示し、-側はチャネル表面がn型にドーピングされていることを示す。チャネル表面のn型不純物濃度が増すほど、チャネル構造は埋め込み型の動作をするようになってくる。

【0022】また、図3にゲート電極の仕事関数を変えたときのゲート長 L と閾値電圧 V_{th} の関係（ショートチャネル効果）を示す。仕事関数（WF）が4.5 eV 以下の領域では、ほとんど曲線が重なっていることがわかる。

【0023】また、図4にゲート長 $L = 95$ nm の変化（ $\pm 5\%$ ）に対する閾値電圧 V_{th} の変化量 dV_{th} を示す。仕事関数が4.5 eV を越えるあたりから dV_{th} は急激に上昇するが、それ以下ではほぼ同じ値を示すことがわかる。

【0024】図5に、仕事関数を変えた場合の $V_g - I_d$ 特性を示す。ここでも、仕事関数が4.5 eV 以下になると特性がほぼ同じになることが確認される。

【0025】図6に、仕事関数に対する $S - factor$ の値を示す。仕事関数が4.5 eV 以上では $S - factor$ は急激に上昇し、特性の劣化が顕著になるが、4.5 eV 以下では、 $S - factor$ が80程度のほぼ一定の値を示すことがわかる。

【0026】これらの結果から、閾値電圧 $V_{th} = 0.4$ V のトランジスタを作成するにあたり、ゲート電極の仕事関数はバンドギャップ中央から伝導電子帯の方向に0.1 eV だけずらしたものをを用いれば、それ以上ずらしたものと同等の効果が得られることがわかった。また、0.4 V よりも低いしきい値を実現するには $(0.5 - V_{th})$ の分だけバンドギャップ中央より伝導電子帯側にずらせば、同様の効果が得られることがわかった。

【0027】この理由を調べるために、仕事関数が異なる場合のチャネルのポテンシャルを調べた。図7は、 $\phi_f = 4.2 \sim 4.7$ の間で0.1 eV 刻みで仕事関数を変化させた場合のチャネル中央の基板深さ方向へのポテンシャル変化を示す。図7において、縦軸はポテンシャル、横軸は基板深さである。

【0028】図7に示すように、 $\phi_f = 4.6, 4.7$ eV ではゲート絶縁膜との界面でのポテンシャルの傾きは-（下向き）、或いはほぼ0である。それに対し、 $\phi_f \leq 4.5$ では+（上向き）になっており、典型的な表面チャネルの特徴を備えている。このことによって、ショートチャネル効果が抑制され、また、 $S - factor$ が改善されていると考えられる。

【0029】また、再び図2に戻ってチャネル濃度について考察する。 $\phi_f = 4.5$ eV 付近では表面チャネル型の動作をするだけでなく、チャネル濃度が低くなっている。チャネル濃度が低いと、チャネルの移動度は向上し、またエクステンション領域との接合に於けるリークが少ないという利点がある。この観点からすると、ゲート絶縁膜に接するゲート電極の仕事関数は伝導電子帯端にあるよりも、シリコン基板のバンドギャップ中央に近い方が望ましい。

【0030】一般にチャネル濃度は $1 \times 10^{18} \text{ cm}^{-3}$ 以下であることが望ましいと考えられており、4.3 eV よりもバンドギャップ中央近くに位置するのが良い。

【0031】上述の条件を満たすように仕事関数を設定するならば、 $V_{th} = 0.4$ V に対しては、 $4.3 \leq \phi_f \leq 4.5$ eV が好適である。また他のしきい値に対しては、

$3.9 + V_{th} \leq \phi_f \leq 4.1 + V_{th}$
の範囲に設定すると同様の効果が得られる。

【0032】P型MISFETに関しては、シリコン基板のバンドギャップの中央に対してN型MISFETと対称と考えれば良く、 $5.1 + V_{th} \leq \phi_f \leq 5.3 + V_{th}$ ($V_{th} < 0$) の範囲に設定すると同様の効果が得られる。

【0033】多結晶シリコンをゲート電極に用いた場合にはシリコン基板のバンドギャップ中央から0.56 eV ずらす必要があった。ところが、上述したように、金属材料電極を用いることにより、しきい値電圧が0.4 V の場合には、シリコン基板のバンドギャップ中央から0.1 eV ずれた金属電極材料を用いればよいことが分かった。

【0034】シリコン基板のバンドギャップ中央から0.1 eV ずれた金属電極材料を見つけることは、0.56 eV ずれた材料を探すことより容易である。

【0035】例えば、表1に示す金属材料を用いればよい。

【0036】

【表1】

仕事関数 (eV)	金属材料
4.4	Sn, B
4.45	Fe, Hg
4.5	Sb, W, Mo
4.6	Cu
4.65	Ru
4.7	Os

【0037】表1に示す金属材料の中から、NMISFETには仕事関数が小さい材料、PMISFETには仕事関数大きいものを選択してゲート電極を形成すればよい。

【0038】次に、同一基板上に異なる仕事関数のゲート電極を形成する方法について、図8(a)～図11(k)を用いて説明する。図8～図11は、本発明の一

実施形態にかかわる半導体装置の製造工程を示す工程断面図である。

【0039】先ず、図8(a)に示すように、シリコン基板600にSTI技術を用いた素子分離絶縁膜602を形成した後、NMISFETを形成する領域にpウェル601、PMISFETを形成する領域にnウェル605を形成する。更に、シリコン基板600表面に薄いシリコン酸化膜603を形成する。そして、後にゲート電極が形成される領域のシリコン酸化膜603上に、多結晶シリコン等からなるダミーゲート604を形成する。

【0040】次いで、図8(b)に示すように、シリコン酸化膜606を形成し、PMISFET領域のシリコン酸化膜606上に選択的にレジストを形成した後、レジスト及びNMISFET領域のダミーゲート604をマスクに、イオン注入を行うことで、N型エクステンション607を形成する。さらに、NMISFET領域のシリコン酸化膜606上に選択的にレジスト608を形成した後、レジスト608及びPMISFET領域のダミーゲート604をマスクに、イオン注入を行うことことで、P型エクステンション609を形成する。なお、シリコン酸化膜606は、シリコン基板600にレジストを直接塗布することで、基板が汚染されることを防止するためのものである。

【0041】次いで、図8(c)に示すように、シリコン基板600表面にシリコン窒化膜等の絶縁膜を堆積し、公知の側壁残し工程を行うことでゲート側壁絶縁膜610を形成する。

【0042】次いで、図9(d)に示すように、PMISFET領域のシリコン酸化膜606上に選択的にレジストを形成した後、レジスト及びNMISFET領域のダミーゲート604及びゲート側壁絶縁膜610をマスクに、イオン注入を行うことことで、N型ソース/ドレイン611を形成する。さらに、NMISFET領域のシリコン酸化膜606上に選択的にレジスト612を形成した後、レジスト612及びPMISFET領域のダミーゲート604及びゲート側壁絶縁膜610をマスクに、イオン注入を行うことことで、P型ソース/ドレイン613を形成する。

【0043】次いで、図9(e)に示すように、シリコン基板600表面にシリコン酸化膜などからなる絶縁膜614をダミーゲート604の厚みより厚くなるように、堆積する。

【0044】次いで、図9(f)に示すように、CMP法等を用いて、ダミーゲート604の頂上が露出するように、絶縁膜614を平坦に研削する。

【0045】次いで、図10(g)に示すように、ダミーゲート604をCDE(ChemicalDry Etching)又はHFとHNO₃との混合液などを用いたエッチングで除去し、更にシリコン酸化膜603の露出部分を除去す

る。

【0046】次いで、図10(h)に示すように、ダミーゲート604及びシリコン酸化膜603を除去した後の溝部にゲート絶縁膜615、及び仕事関数が4.5eVより小さい金属膜616を堆積する。ゲート絶縁膜615としては、シリコン酸化窒化膜、シリコン窒化膜、又はTa₂O₅などのようなシリコン酸化膜より誘電率が高い膜などが好適である。また、金属膜616としては、NMISFET領域での仕事関数を決定するだけの物であるから、非常に薄い膜厚、例えば10nm以下で十分である。

【0047】次いで、図10(i)に示すように、PMISFET側の金属膜616を除去し、金属膜616をNMISFET側だけに残す。これはレジストをマスクにウエットエッチング等で除去すれば良い。例えば金属膜616として、W、Mo、TiNなどを用いている場合、H₂O₂溶液を用いてエッチングすることが可能である。なお、エッチングに用いる溶液は、これに限らず、エッチングする金属の種類に応じて適宜選択すればよい。ゲート絶縁膜615に損傷を与えない範囲で有れば、RIE法やCDE法を用いてエッチングしても良い。

【0048】次いで、図11(j)に示すように、仕事関数が4.7eVより大きい金属として第2の金属膜617を形成する。この第2の金属膜617は、PMISFET領域での仕事関数を決定すると共に、ゲート電極の抵抗値を決定する。従って、仕事関数が適当な値であるだけでなく、抵抗率も低いことが望ましい。

【0049】次に、図11(k)に示すように、少なくとも第2の金属膜617が完全に絶縁膜614の表面から除去されるように、CMP法等を用いて第2の金属膜617を研削する。この時、絶縁膜614上のゲート絶縁膜615を除去しても良いし、必要に応じて残しても良い。

【0050】上記の方法で、金属膜615、617は、NMISFET及びPMISFETの閾値電圧が最適になるように、表1に示した材料から選ぶことができる。表1に示す金属材料の中から、NMISFETには仕事関数が小さい材料、PMISFETには仕事関数が大きいものを選択してゲート電極を形成すればよい。

【0051】また、TiNのような導電性の金属化合物も同様に金属電極として使うことができるが、結晶配向によって、0.12~0.14eV程度の仕事関数が異なることが報告されている(Nakajima et al. 1999 Symposium on VLSI Technology Digest of Technical Papers p.96)。成膜方法や条件を変えることで、仕事関数が異なるTiNを形成し、2種の電極材料として用いることも可能である。

【0052】次に、1種の金属の仕事関数を膜を形成した後に変化させ、2種の仕事関数のゲート電極を得る方

法について、図12を用いて説明する。図12は、本発明の一実施形態にかかわる半導体装置の製造工程を示す工程断面図である。まず、図8(a)～図11(k)に説明したのと全く同様の方法でダミーゲートを除去した後にゲート絶縁膜615及び第1の金属膜616を形成する。

【0053】次に、図12(a)に示すように、P型MISFET領域にレジストマスク710を形成した後、In、Ga等の様に融点が低く、仕事関数が小さい金属をイオン注入し、第1の金属膜616を改質した第3の金属膜716を形成する。第3の金属膜716は、450℃程度の熱工程をかけることで、第3の金属膜716の粒界を介してゲート絶縁膜615との界面に仕事関数が低い金属が析出し、所望のしきい値を得ることができる。

【0054】次いで、図12(b)に示すように、W、Alなどからなる低抵抗である第2の金属膜617を堆積し、図12(c)に示すようにCMP法などを用いて絶縁膜614上に堆積した金属膜616、716、617を完全に除去する。

【0055】また、ここでは第1の金属膜616より仕事関数が低い金属をNMISFET領域に注入したが、仕事関数が高い金属をPMISFET領域に注入することも可能であり、また必要に応じて両方の領域に異なる金属を注入する事も可能である。

【0056】また、上記の例では、金属を析出させる例を挙げたが、N等の元素をイオン注入し、組成の違う化合物を形成することにより仕事関数を変化させることも可能である。この方法についてはWakabayashi et al., IEDM Technology Digest p.253 (1999)に開示されている。

【0057】なお、本発明は、上記実施形態に限定されるものではなく、その要旨を逸脱しない範囲で、種々変形して実施することが可能である。

【0058】

【発明の効果】以上説明したように本発明によれば、N型MISトランジスタのゲート電極は、ゲート絶縁膜に接し、仕事関数 ϕ_f が、閾値電圧 V_{th} に対し、 $V_{th} + 3.9 \leq \phi_f \leq V_{th} + 4.1$ eVである第1の金属含有

膜を具備し、P型MISトランジスタのゲート電極は、ゲート絶縁膜に接し、仕事関数 ϕ_f が、 $5.1 + V_{th} \leq \phi_f \leq 5.3 + V_{th}$ である第2の金属含有膜を具備することによって、低しきい値電圧のN型及びP型MISFETを得ることができる。

【図面の簡単な説明】

【図1】シミュレーションに用いたトランジスタ構造を示す図。

【図2】種々の仕事関数に対してしきい値を0.4Vに合わせるのに要するチャネルドーピングの図。

【図3】種々の仕事関数に対するゲート長としきい値の関係を示す図。

【図4】仕事関数とLの10%の変化に対するしきい値変化を示す図。

【図5】種々の仕事関数に対する、 $V_g - I_d$ を示す図。

【図6】仕事関数とS-factorの関係を示す図。

【図7】種々の仕事関数に対するチャネル中央に於けるポテンシャルを示す図。

【図8】本発明の一実施形態に係わる半導体装置の製造工程を示す図。

【図9】本発明の一実施形態に係わる半導体装置の製造工程を示す図。

【図10】本発明の一実施形態に係わる半導体装置の製造工程を示す図。

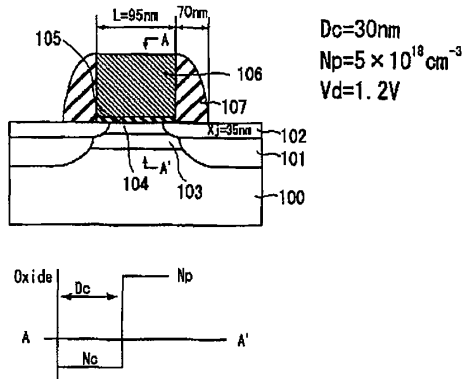
【図11】本発明の一実施形態に係わる半導体装置の製造工程を示す図。

【図12】本発明の一実施形態に係わる半導体装置の製造工程を示す図。

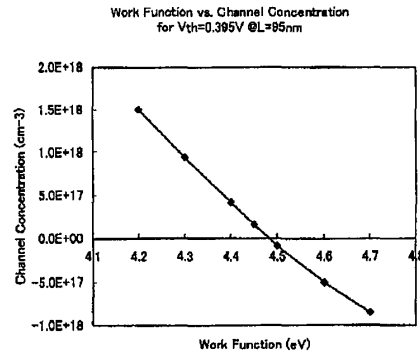
【符号の説明】

- 100…シリコン基板
- 101…ソース/ドレイン
- 102…エクステンション領域
- 103…チャネル領域
- 104…カウンタードーピング領域
- 105…ゲート絶縁膜
- 106…ゲート電極
- 106…ゲート側壁絶縁膜

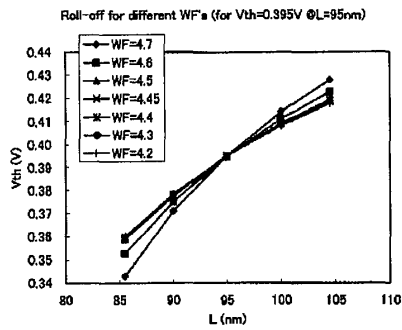
【図1】



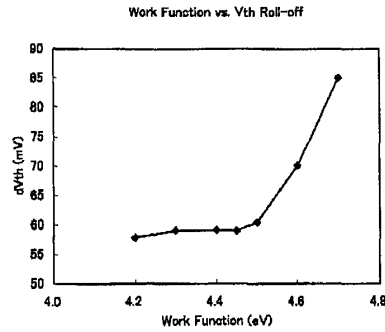
【図2】



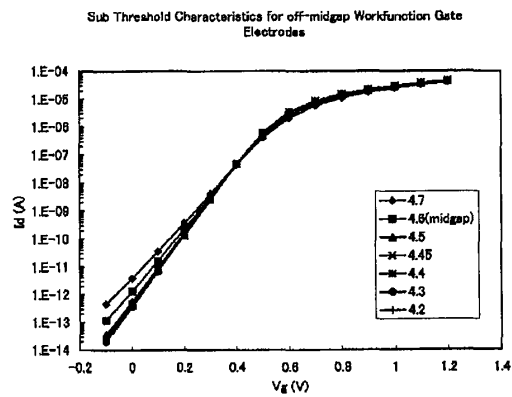
【図3】



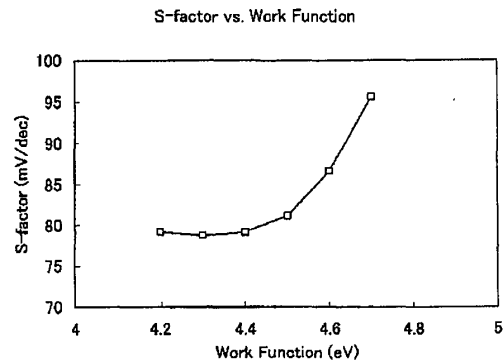
【図4】



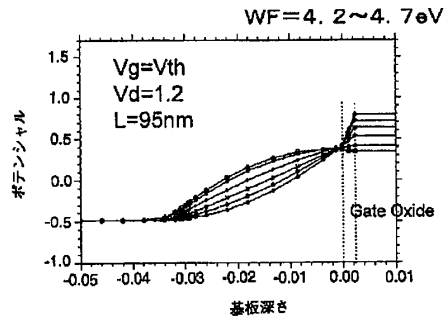
【図5】



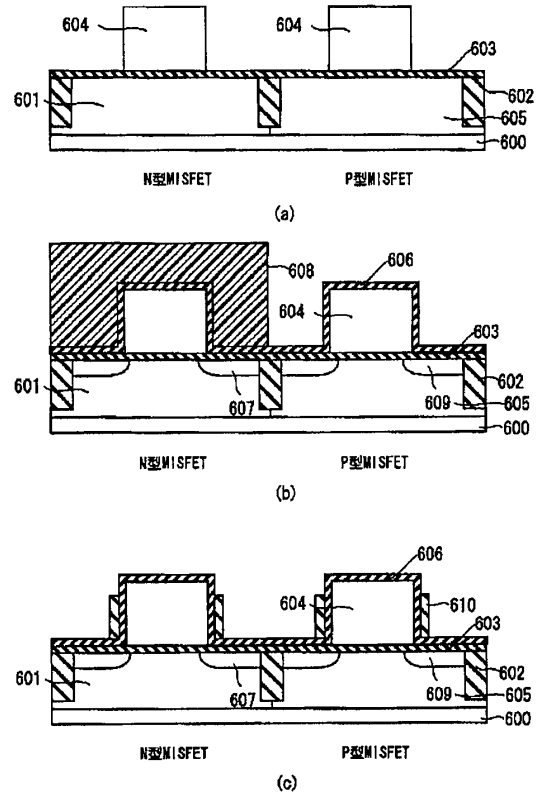
【図6】



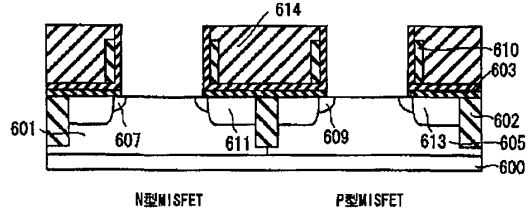
【図7】



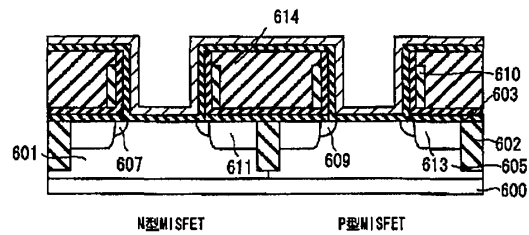
【図8】



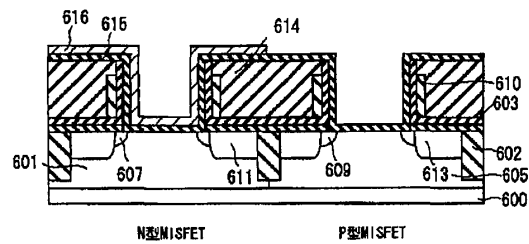
【図 10】



(g)

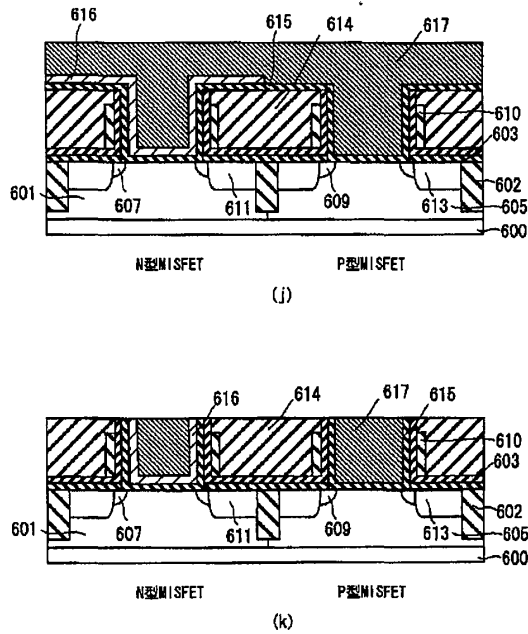


(h)

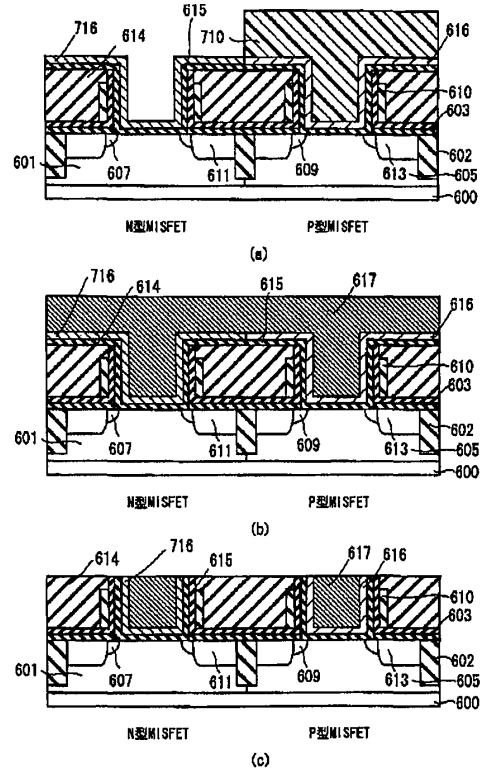


(i)

【図11】



【図12】



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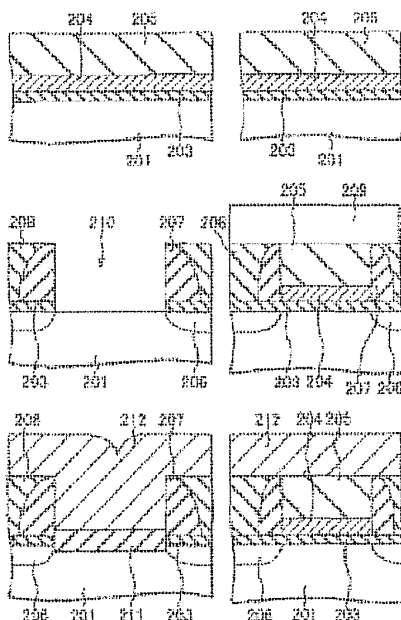
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF**Publication number:** JP11074368 (A)**Publication date:** 1999-03-16**Inventor(s):** TSUNASHIMA YOSHITAKA; MIYANO KIYOTAKA**Applicant(s):** TOKYO SHIBAURA ELECTRIC CO**Classification:**

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Application number: JP19980185116 19980630**Priority number(s):** JP19980185116 19980630; JP19970174205 19970630**Abstract of JP 11074368 (A)**

PROBLEM TO BE SOLVED: To obtain a semiconductor device in which a gate electrode and a gate insulating film in different film thicknesses and of different materials are formed on an identical substrate, by a method wherein a first film and a second film are removed from at least one region out of a plurality of regions in which gate electrodes are formed, and a first insulating film and a first gate electrode are formed in the region in which the films are removed. **SOLUTION:** A well region and an element isolation region are formed on a silicon substrate 201. A gate oxide film 203 is formed, and a poly-Si film 204 is formed on it. In a region in which a first transistor is formed mainly, the poly-Si film 204 is removed by a heated phosphoric acid solution. In succession, the gate oxide film 203 in an exposed region is removed by a dilute hydrofluoric acid solution. A gate oxide film 211 is formed on the surface of the silicon substrate 201 in the exposed region, and a tungsten film 212 is formed additionally on the whole face. In a first element region, a first gate electrode is constituted of the poly-Si film 204. In a second element region, a second gate electrode is constituted of the tungsten film 212.



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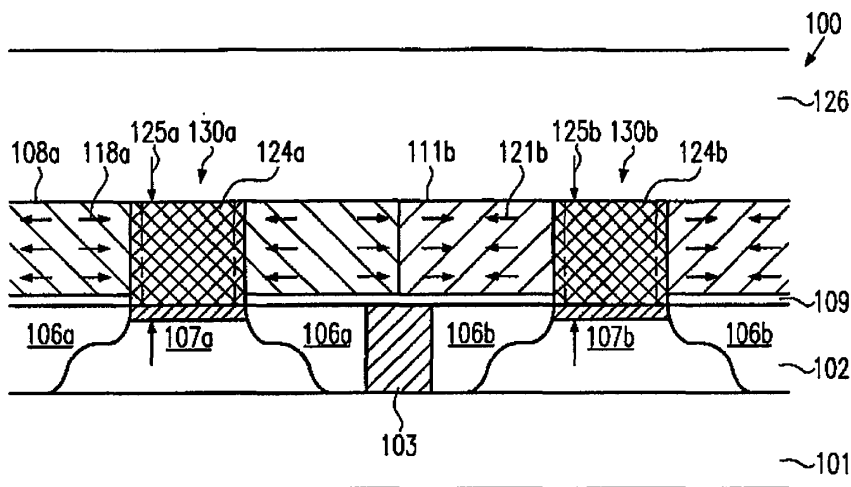
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(54) Title: A SEMICONDUCTOR DEVICE INCLUDING SEMICONDUCTOR REGIONS HAVING DIFFERENTLY
STRAINED CHANNEL REGIONS AND A METHOD OF MANUFACTURING THE SAME



(57) Abstract: By locally modifying the intrinsic stress of a dielectric layer laterally enclosing gate electrode structures of a transistor configuration formed in accordance with in-laid gate techniques, the charge carrier mobility of different transistor elements may individually be adjusted. In particular, in in-laid gate structure transistor architecture, NMOS transistors and PMOS transistors may receive a tensile and a compressive stress, respectively.

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**A SEMICONDUCTOR DEVICE INCLUDING SEMICONDUCTOR REGIONS HAVING
DIFFERENTLY STRAINED CHANNEL REGIONS AND A METHOD OF MANUFACTURING
THE SAME**

BACKGROUND OF THE INVENTION

1. TECHNICAL FIELD

Generally, the present invention relates to the formation of integrated circuits, and, more particularly, to the formation of semiconductor regions of increased charge carrier mobility, such as a channel region of a field effect transistor, by creating strain in the semiconductor region.

2. BACKGROUND ART

The fabrication of integrated circuits requires the formation of a large number of circuit elements on a given chip area according to a specified circuit layout. For this purpose, substantially crystalline semiconductor regions with or without additional dopant materials are defined at specified substrate locations to act as "active" regions, that is, to act, at least temporarily, as conductive areas. Generally, a plurality of process technologies are currently practiced, wherein for complex circuitry, such as microprocessors, storage chips and the like, MOS technology is currently the most promising approach, due to the superior characteristics in view of operating speed and/or power consumption and/or cost efficiency. During the fabrication of complex integrated circuits using MOS technology, millions of transistors, *i.e.*, N-channel transistors and/or P-channel transistors, are formed on a substrate including a crystalline semiconductor layer. A MOS transistor, irrespective of whether an N-channel transistor or a P-channel transistor is considered, comprises so-called PN junctions that are formed by an interface of highly doped drain and source regions with a slightly doped or non-doped channel region disposed between the drain region and the source region. The conductivity of the channel region, *i.e.*, the drive current capability of the conductive channel, is controlled by a gate electrode formed adjacent to the channel region and separated therefrom by a thin insulating layer. The conductivity of the channel region upon formation of a conductive channel due to the application of an appropriate control voltage to the gate electrode, depends on the dopant concentration, the mobility of the charge carriers, and, for a given extension of the channel region in the transistor width direction, on the distance between the source and drain regions, which is also referred to as channel length. Hence, in combination with the capability of rapidly creating a conductive channel below the insulating layer upon application of the control voltage to the gate electrode, the conductivity of the channel region substantially affects the performance of the MOS transistors. Thus, as the speed of creating the channel, *i.e.*, the conductivity of the gate electrode, and the channel resistivity substantially determine the transistor characteristics, the reduction of the channel length, and associated therewith the reduction of channel resistivity and increase of gate resistivity, renders the channel length a dominant design criterion for accomplishing an increase in the operating speed of the integrated circuits.

The continuing shrinkage of the transistor dimensions, however, entails a plurality of issues associated therewith that have to be addressed so as to not unduly offset the advantages obtained by steadily decreasing the channel length of MOS transistors. One major problem in this respect is the development of enhanced photolithography and etch strategies to reliably and reproducibly create circuit elements of critical dimensions, such as the gate electrode of the transistors, for a new device generation. Moreover, highly sophisticated dopant profiles, in the vertical direction as well as in the lateral direction, are required in the drain and source regions to provide low sheet and contact resistivity in combination with a desired channel controllability. In addition, the vertical location of the PN junctions with respect to the gate insulation layer also represents a critical design

crucial in view of leakage current control, as reducing the channel length also requires reducing the depth of the drain and source regions with respect to the interface formed by the gate insulation layer and the channel region, thereby requiring sophisticated implantation techniques. According to other approaches, epitaxially grown regions are formed with a specified offset to the gate electrode, which are referred to as raised drain and source regions, to provide increased conductivity of the raised drain and source regions, while at the same time maintaining a shallow PN junction with respect to the gate insulation layer.

In other conventional solutions, the problem of increased resistivity of polysilicon gate electrodes in extremely scaled devices is addressed by replacing the currently used doped polysilicon by a metal as the gate electrode material, while nevertheless maintaining a self-aligned process sequence for the formation of the drain and source regions and the gate electrode. This may be accomplished by forming a dummy gate which may, in combination with removable sidewall spacers, act as an implantation mask during the formation of the drain and source regions. After embedding the dummy gate in an interlayer dielectric, the dummy gate may be replaced by a highly conductive gate material, such as a metal. With this approach of an "in-laid" gate electrode, the transistor performance may significantly be improved. The problem of restricted channel conductivity, however, is not addressed by this approach.

Furthermore, since the continuous size reduction of the critical dimensions, *i.e.*, the gate length of the transistors, necessitates the adaptation and possibly the new development of highly complex process techniques concerning the above-identified process steps, it has been proposed to also enhance device performance of the transistor elements by increasing the charge carrier mobility in the channel region for a given channel length, thereby offering the potential for achieving a performance improvement that is comparable with the advance to a future technology node of down-sized devices while avoiding many of the above process adaptations associated with device scaling. In principle, at least two mechanisms may be used, in combination or separately, to increase the mobility of the charge carriers in the channel region. First, the dopant concentration within the channel region may be reduced, thereby reducing scattering events for the charge carriers and thus increasing the conductivity. However, reducing the dopant concentration in the channel region significantly affects the threshold voltage of the transistor device, thereby presently making a reduction of the dopant concentration a less attractive approach unless other mechanisms are developed to adjust a desired threshold voltage. Second, the lattice structure in the channel region may be modified, for instance by creating tensile or compressive stress to produce a corresponding strain in the channel region, which results in a modified mobility for electrons and holes, respectively. For example, creating tensile strain in the channel region increases the mobility of electrons, wherein, depending on the magnitude and direction of the tensile strain, an increase in mobility of up to 120% or more may be obtained, which, in turn, may directly translate into a corresponding increase in the conductivity. On the other hand, compressive strain in the channel region may increase the mobility of holes, thereby providing the potential for enhancing the performance of P-type transistors. The introduction of stress or strain engineering into integrated circuit fabrication is an extremely promising approach for further device generations, since, for example, strained silicon may be considered as a "new" type of semiconductor, which may enable the fabrication of fast powerful semiconductor devices without requiring expensive semiconductor materials and manufacturing techniques.

Consequently, it has been proposed to introduce, for instance, a silicon/germanium layer or a silicon/carbon layer in or below the channel region to create tensile or compressive stress that may result in a corresponding strain. Although the transistor performance may be considerably enhanced by the introduction of

stress-creating layers in or below the channel region, significant efforts have to be made to implement the formation of corresponding stress layers into the conventional and well-approved MOS technique. For instance, additional epitaxial growth techniques have to be developed and implemented into the process flow to form the germanium- or carbon-containing stress layers at appropriate locations in or below the channel region. Hence, process complexity is significantly increased, thereby also increasing production costs and the potential for a reduction in production yield.

In view of the above-described situation, there exists a need for an alternative technique that enables the creation of different desired stress conditions in different semiconductor regions, while providing the potential for the formation of improved transistor architectures including the introduction of highly conductive gate electrodes.

DISCLOSURE OF INVENTION

The following presents a simplified summary of the invention in order to provide a basic understanding of some aspects of the invention. This summary is not an exhaustive overview of the invention. It is not intended to identify key or critical elements of the invention or to delineate the scope of the invention. Its sole purpose is to present some concepts in a simplified form as a prelude to the more detailed description that is discussed later.

Generally, the present invention is directed to a technique that enables the combination of the process strategies having the potential for forming enhanced transistor architectures, such as transistor elements including so-called "in-laid" gate electrodes, with enhanced stress or strain engineering to provide at least two different magnitudes or types of strain in two different semiconductor regions. Consequently, different regions within a die area or across the entire substrate bearing a plurality of individual die areas may receive differently strained semiconductor regions to individually adapt the charge carrier mobility and thus the conductivity thereof to specified process and device requirements. In particular, different types of transistors, such as N-type or N-channel transistors and P-type or P-channel transistors, may receive a different type or a different magnitude of strain within the respective channel regions while at the same time the gate conductivity may be enhanced, if desired, due to the possibility of forming in-laid gate electrode structures on the basis of highly conductive materials, such as metals.

According to one illustrative embodiment of the present invention, a method comprises forming a first place holder structure above a first semiconductor region formed in a semiconductor layer that is located on a substrate. A second place holder structure is formed above a second semiconductor region which is formed in the semiconductor layer, and a dielectric layer having a specified intrinsic stress is deposited above the semiconductor layer to enclose the first and second place holder structures. Additionally, a portion of the dielectric layer enclosing the second place holder structure is modified to change the intrinsic stress within the portion. Finally, the first and second place holder structures are replaced by a conductive material.

According to another illustrative embodiment of the present invention, a method comprises forming a first place holder structure above a first channel region of a first transistor and forming a second place holder structure above a second channel region of a second transistor. Moreover, first drain and source regions are formed adjacent to the first channel region and second drain and source regions are formed adjacent to the second channel region. Furthermore, above the first drain and source regions, a first dielectric layer having a first intrinsic stress is formed, and, above the second drain and source regions, a second dielectric layer having a second intrinsic stress that differs from the first intrinsic stress is formed. Finally, the first place holder structure is replaced with a first gate electrode structure and the second place holder structure is replaced with a second gate electrode structure.

According to yet another illustrative embodiment of the present invention, a semiconductor device comprises a first transistor element having a first gate electrode with a first height and a second transistor element having a second gate electrode with a second height. The device further comprises a first dielectric layer having a first intrinsic stress and laterally enclosing the first gate electrode, wherein the first intrinsic stress acts substantially homogeneously within the first dielectric layer up to the first height. Moreover, the device comprises a second dielectric layer having a second intrinsic stress and laterally enclosing the second gate electrode, wherein the second intrinsic stress differs from the first intrinsic stress and acts substantially homogeneously within the second dielectric layer up to the second height.

BRIEF DESCRIPTION OF DRAWINGS

The invention may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

Figures 1a-1h schematically show cross-sectional views of a semiconductor device during various manufacturing stages, wherein different strain is created at different semiconductor regions by means of respective stress layers formed in the vicinity of the semiconductor regions in accordance with a process strategy that enables the formation of in-laid gate electrode structures;

Figure 2 schematically depicts a semiconductor device in cross-sectional view during a manufacturing stage in which an intrinsic stress of a stress layer is locally modified in accordance with further illustrative embodiments; and

Figures 3a and 3b schematically show a semiconductor device in cross-section in a manufacturing stage during which ion species are deposited at certain locations to enhance the stress transfer into respective semiconductor regions in accordance with further illustrative embodiments of the present invention.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

MODE(S) FOR CARRYING OUT THE INVENTION

Illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

The present invention will now be described with reference to the attached figures. Various structures, systems and devices are schematically depicted in the drawings for purposes of explanation only and so as to not obscure the present invention with details that are well known to those skilled in the art. Nevertheless, the attached drawings are included to describe and explain illustrative examples of the present invention. The words and phrases used herein should be understood and interpreted to have a meaning consistent with the understanding of those words and phrases by those skilled in the relevant art. No special definition of a term or phrase,

i.e., a definition that is different from the ordinary and customary meaning as understood by those skilled in the art, is intended to be implied by consistent usage of the term or phrase herein. To the extent that a term or phrase is intended to have a special meaning, *i.e.*, a meaning other than that understood by skilled artisans, such a special definition will be expressly set forth in the specification in a definitional manner that directly and unequivocally provides the special definition for the term or phrase.

The present invention is based on the concept that strain in a semiconductor region, such as a channel region of a transistor element, may highly efficiently be generated by a material layer having a specified intrinsic stress that is formed close to the semiconductor region of interest. By providing a process strategy that allows an effective local adjustment of strain within a die area or within different substrate areas including a plurality of die areas and even at a very small scale, such as at different channel regions of a complementary transistor pair, an enhanced strain engineering may be combined with an enhanced transistor architecture, thereby providing high gate conductivity in combination with high charge carrier mobility and thus channel conductivity even for highly scaled transistor devices. With reference to the accompanying drawings, further illustrative embodiments of the present invention will now be described in more detail.

Figure 1a schematically shows a cross-sectional view of a semiconductor device 100 that comprises a substrate 101, which may represent any appropriate substrate for forming thereon circuit elements of integrated circuits such as microprocessors, storage chips and the like. The substrate 101 may represent a bulk semiconductor substrate, such as a silicon substrate, or may represent, in particular embodiments, a silicon-on-insulator (SOI) substrate, wherein a semiconductor layer 102 may represent the crystalline silicon layer formed on an insulating layer (not shown) within the substrate 101. Since the vast majority of advanced integrated circuits fabricated in accordance with MOS techniques are fabricated on the basis of silicon, in the following detailed description it may frequently be referred to silicon with respect to the semiconductor layer 102, wherein it should be appreciated that any other suitable semiconductor materials, such as gallium arsenide, germanium, silicon/germanium, or any other III-V or II-VI semiconductor materials, may also be used with the present invention. Similarly, the semiconductor layer 102 may represent an upper portion of a bulk semiconductor substrate, although it is shown as a separate layer.

The semiconductor device 100 comprises a first place holder structure 104a formed of any appropriate material, such as silicon dioxide, amorphous carbon, and the like. The first place holder structure 104a is formed above a first semiconductor region 107a, which may represent a first channel region, if a transistor is to be formed by means of the first place holder 104a. First doped regions 106a, which may be arranged symmetrically or asymmetrically with respect to the first semiconductor region 107a, may be formed within the layer 102 and may be provided, in the embodiment shown, in the form of drain and source regions. That is, the vertical and lateral dopant profile of the first doped regions 106a may be designed in accordance with device requirements of a specified transistor type. Hence, in particular embodiments, the doped regions 106a represent first drain and source regions having included therein a dopant material that imparts a specified type of conductivity to these regions. In this embodiment, the regions 106a may be N-doped and the regions 106a in combination with the first semiconductor region 107a may have the characteristics of an N-channel transistor. Moreover, sidewall spacers 105a are formed on sidewalls of the first place holder 104a, wherein the sidewall spacer 105a may differ in material composition from the first place holder 104a to exhibit, in particular embodiments, a desired high etch selectivity in subsequent etch procedures. For example, the sidewall spacer 105a may be comprised of amorphous carbon, silicon nitride, silicon dioxide and the like.

Similarly, a second place holder structure 104b may be formed above a second semiconductor region 107b, which may, in some embodiments, represent the channel region of a second transistor element. Moreover, doped regions 106b may be formed adjacent to the second semiconductor region 107b to define, in particular embodiments, the drain and source regions and the channel region of a specified transistor type. For example, the second semiconductor region 107b enclosed by the doped regions 106b may be located next to the first semiconductor region 107a enclosed by the respective doped regions 106a, but separated therefrom by an isolation structure 103 which may be provided in the form of a trench isolation structure as is typically used in advanced semiconductor devices. When representing a transistor configuration, the regions 107b, 106b may be of the same type as the regions 107a, 106a or may represent a different type of transistor, such as a P-type or P-channel transistor. It should be appreciated, however, that the first and second semiconductor regions 107a, 107b may represent circuit elements that are located at very different positions within the same die area, but which require to receive a different type or magnitude of strain to provide different electrical characteristics. Similarly, the regions 107a, 107b may represent different circuit elements or even different die portions located at different substrate regions, such as a center region and a peripheral region, wherein the strain engineering for the first and second semiconductor regions 107a, 107b may provide more uniform electrical behavior of semiconductor devices fabricated on the central and peripheral regions of the substrate 101. Regarding the material composition of the second place holder 104b and a sidewall spacer 105b formed on sidewalls thereof, the same criteria apply as are referred to with respect to the corresponding components 104a and 105a.

A typical process flow for forming the semiconductor device 100 as shown in Figure 1a may comprise the following processes. After forming the substrate 101 including the semiconductor layer 102 or receiving the same from substrate manufacturers, implantation sequences may be performed to establish a specified vertical dopant profile within the first and second semiconductor regions 107a, 107b. Thereafter, the first and second place holders 104a, 104b may be formed by well-established deposition, photolithography and etch techniques, wherein a length of the first and second place holders 104a, 104b, that is, the horizontal dimension (or gate length dimension) of these components in Figure 1a, may be adapted to design requirements and may be approximately 100 nm and significantly less for highly advanced integrated circuits. Thereafter, dopant species may be introduced to form the doped regions 106a, 106b therein. Depending on device requirements, the device 100 may correspondingly be masked, for instance by a photoresist mask, to individually form the regions 106a, 106b with a desired type of dopant material. During these implantations, the place holders 104a, 104b act as an implantation mask to substantially avoid dopant penetration of the respective semiconductor regions 107a, 107b. Thereafter, the sidewall spacers 105a, 105b may be formed by depositing a corresponding layer of material and anisotropically etching the material layer. It should be appreciated that, typically, a liner material may be deposited prior to a spacer material so as to not unduly damage the surface of the semiconductor layer 102 when exposed to the anisotropic etch atmosphere. For convenience, a corresponding liner is not shown in Figure 1a. Then, a further implantation process may be performed, possibly on the basis of a further photoresist mask, wherein also the first and second place holders 104a, 104b in combination with the respective sidewall spacers 105a, 105b act as an implantation mask to obtain the desired lateral dopant profile in the doped regions 106a, 106b, respectively. Then, corresponding anneal cycles may be performed to activate the dopants in the regions 106a, 106b and re-crystallize damaged crystal portions. Alternatively, corresponding anneal processes may be performed after one or more of the above-described implantations.

It should be noted that in some examples when a highly sophisticated lateral dopant profile is required, additional sidewall spacers (not shown) may be formed, followed by a further implantation step to obtain a more complex dopant profile within the regions 106a, 106b. Thereafter, in particular embodiments, the sidewall spacers 105a, 105b may be removed by a selective etch process on the basis of well-established process recipes. For instance, the spacers 105a, 105b, when comprised of silicon nitride, may selectively be removed by hot phosphoric acid. In other examples, the spacers 105a, 105b may be removed by a plasma etch process, wherein, in some embodiments, the liner (not shown), typically used as an etch stop layer, may be maintained during the implantation cycle and may now be used as an etch stop layer during the removal of the spacers 105a, 105b. In other embodiments, the spacers 105a, 105b may be maintained during the further processing of the device 100.

Figure 1b schematically shows the device 100 in an advanced manufacturing stage. Here, the device 100 comprises a dielectric layer 108 having a specified intrinsic stress, which is formed to enclose the first and second place holders 104a, 104b. The term "intrinsic stress" is to be understood as specifying a certain type of stress, that is tensile or compressive, or any variation thereof, *i.e.*, orientation dependent tensile or compressive stress, as well as the magnitude of the stress. Thus, in one embodiment, the dielectric layer 108 may have an intrinsic tensile stress with a magnitude of approximately 0.1-1.0 GPa (Giga-Pascal). The dielectric layer 108 may be comprised of any appropriate material, such as silicon nitride. In one illustrative embodiment, the device 100 further comprises a conformal etch stop layer 109 having a different material composition compared to the dielectric layer 108 and having a significantly smaller thickness compared to the dielectric layer 108. For example, the etch stop layer 109 may be comprised of silicon dioxide.

The etch stop layer 109, if provided, may be formed by well-established plasma enhanced chemical vapor deposition (PECVD) techniques on the basis of precursor materials, such as TEOS or silane. The dielectric layer 108 may be formed by PECVD techniques on the basis of well-known process recipes, wherein process parameters may be adjusted to achieve the desired intrinsic stress. For example, silicon nitride may be deposited with high compressive or tensile stress, wherein the type and magnitude of the stress may readily be adjusted by controlling process parameters, such as deposition temperature, deposition pressure, tool configuration, bias power for adjusting an ion bombardment during the deposition process, plasma power, and the like. For example, increased ion bombardment, that is increased bias power, during the deposition of silicon nitride promotes the creation of compressive stress given that the remaining parameters are the same. After the deposition of the dielectric layer 108, in some particular embodiments, the resulting topography may be planarized, for instance by chemical mechanical polishing (CMP) in accordance with well-established process recipes. Thereby, excess material of the dielectric layer 108 may be removed to a specified degree to arrive at a substantially planar surface or, in some illustrative embodiments, the material removal may be continued until top surfaces of the first and second place holders 104a, 104b are exposed. In other embodiments, however, the further processing may be performed without planarizing the layer 108.

Figure 1c schematically shows the device 100 in a further advanced manufacturing stage, in which a portion of the layer 108, which has surrounded the second place holder 104b, is removed while the first place holder 104a is still embedded, at least laterally, by the remaining dielectric layer 108, which is now referred to as 108a. Furthermore, a resist mask 110 is formed on the device 100 to expose the second place holder 104b and the associated portion of the layer 102 including the etch stop layer 109, if provided.

The resist mask 110 may be formed in accordance with photolithography techniques that may also be used in differently doping P-type and N-type transistors and hence corresponding processes are well established.

Thereafter, the dielectric layer 108 may selectively be etched by an anisotropic process recipe to finally obtain the dielectric layer 108a having the specified intrinsic stress. During the anisotropic etch process, the etch stop layer 109, if provided, may prevent undue material removal and/or damage of exposed portions of the semiconductor layer 102.

Figure 1d schematically shows the device 100 with a second dielectric layer 111 having a second specified intrinsic stress, which covers the dielectric layer portion 108a and the second place holder 104b and the exposed semiconductor layer 102 or the etch stop layer 109. It should be noted that the exposed portion of the etch stop layer 109 may be removed prior to the deposition of the second dielectric layer 111, when the exposed portion of the etch stop layer 109 is considered inappropriate owing to any damage caused by the preceding anisotropic etch process of the dielectric layer 108. In this case, a further etch stop layer similar to the layer 109 may be deposited, which may then also cover the dielectric layer portion 108a (shown in dashed lines) and may cover the exposed portions of the semiconductor layer 102 and the second place holder 104b. For convenience, this portion of the etch stop layer is still denoted as 109. Providing the etch stop layer 109 on the semiconductor layer 102 may be advantageous in forming contact openings in a later manufacturing stage. In other embodiments, however, the etch stop layer 109 may be omitted.

The second dielectric layer 111, which may be comprised of any appropriate material, such as silicon nitride, may be deposited by well-established deposition recipes, wherein process parameters are controlled to provide the desired intrinsic stress in accordance with device requirements. As previously noted, silicon nitride may readily be deposited on the basis of well-known process recipes with a wide range of compressive and tensile stress, for example reaching from 1.0 GPa compressive stress to 1.0 GPa tensile stress. In one particular embodiment, the intrinsic stress of the second dielectric layer 111 is designed to impart a compressive stress to the second semiconductor region 107b, when this region is to represent the channel region of a P-type transistor. Thereafter, excess material of the dielectric layer 111 and possibly of the layer portion 108a, when the dielectric layer 108 has not been planarized or has been planarized to a level well above the first place holder 104a, as shown in Figures 1c and 1d, may be removed by a CMP process, thereby also planarizing the topography of the device 100.

Figure 1e schematically shows the device 100 after the above-described process sequence. Hence, the device 100 comprises a substantially planar topography with the layer portion 108a laterally enclosing the first place holder 104a and with a second layer portion 111b laterally enclosing the second place holder 104b. Consequently, a substantially homogeneously acting intrinsic stress of the layer portion 108a, herein shown as a tensile stress indicated as 118a, creates a respective deformation and thus strain in the first semiconductor region 107a, that is, in the present example a tensile strain, which typically increases the mobility of electrons in this region. Similarly, the layer portion 111b having the substantially homogeneously acting second intrinsic stress, in this example illustrated in the form of a compressive stress 121b, correspondingly creates a deformation or strain within the second semiconductor region 107b, which is in the present example a compressive strain, thereby increasing the mobility of holes. It should be appreciated that other configurations may be contemplated for creating different strain in the semiconductor regions 107a, 107b. For example, the intrinsic stress 118a may be compressive and the intrinsic stress 121b may be tensile, or the intrinsic stresses 118a and 121b may both be tensile or compressive and may differ in their magnitudes. In other examples, the intrinsic stress 118a or 121b may be selected to yield a substantially zero strain in the respective semiconductor region, whereas the other semiconductor region receives a desired magnitude of strain. This configuration may be advantageous in

providing more uniform electrical characteristics of P-type transistors and N-type transistors, wherein the mobility of the P-type transistors is to be increased, while the performance of the N-type transistors should not be deteriorated.

Figure 1f schematically shows the device 100 with the place holders 104a, 104b removed. Furthermore, respective gate insulation layers 113a, 113b are formed above the first and second semiconductor regions 107a, 107b, respectively.

The removal of the place holders 104a, 104b may be accomplished by a selective etch process, which may include a plasma etch process and/or a wet chemical etch process. For instance, the place holders 104a, 104b when comprised of silicon dioxide or amorphous carbon, may readily be selectively etched with respect to the layer portions 108a, 111b when for instance comprised of silicon nitride, and with respect to the material of the first and second semiconductor regions 107a, 107b on the basis of well-established process recipes. For example, the removal process may include a plasma etch process for selectively removing the essential amount of the first and second place holders 104a, 104b, while the remaining portion of these place holders may then be removed by a highly isotropic or wet chemical etch process so as to not unduly damage the regions 107a, 107b. In other embodiments, additionally or alternatively, damaged surface portions of the regions 107a, 107b may be oxidized, for instance by thermal oxidation or wet chemical oxidation, and the oxidized portion may be removed by a highly selective wet chemical etch process, for instance, on the basis of fluoric acid (HF) without significantly damaging the regions 107a, 107b.

After removing the place holders 104a, 104b, the gate insulation layers 113a, 113b may be formed by oxidation and/or deposition in accordance with design requirements. For example, the gate insulation layers 113a, 113b may be formed by thermal or wet chemical oxidation in accordance with well-established recipes to obtain a finely tuned layer thickness as required for advanced transistor devices. Thereby, a thickness of the gate insulation layer may range from 1.5 to several nanometers. In other embodiments, an extremely thin thermal oxide may be formed, followed by the deposition of an appropriate dielectric material to achieve the desired final thickness of the gate insulation layers 113a, 113b. A corresponding deposited layer is shown in dashed lines and is indicated as 112. It should be appreciated that the gate insulation layers 113a, 113b may also be formed by means of the deposited layer 112 only. In some illustrative embodiments, prior to the formation of the gate insulation layers 113a, 113b, a dielectric layer such as the layer 112 may be deposited in a highly conformal fashion and with a precisely defined layer thickness, when the initial length 112a of the opening defined by the place holder 104a is considered too great for a desired value of the gate electrode to be formed. Thereafter, the material deposited at the bottom of this opening, *i.e.*, on the region 107a, may be removed by an anisotropic etch process, similarly as is used in typical sidewall spacer techniques. In this way, the gate length of transistor structures may be fine-tuned to compensate for fluctuations in the photolithography or to extend the resolution of the photolithography. Thereafter, the respective gate insulation layers may be formed as is described above.

Figure 1g schematically shows the semiconductor device 100 with a layer of conductive material 123 formed above the structure of Figure 1f. The layer 123 may be comprised of doped polysilicon or, in embodiments for highly advanced semiconductor devices, may comprise a metal or a metal compound. For example, the layer 123 may comprise tungsten, tungsten silicide, aluminum, nickel, copper, or any compounds thereof, and the like. Depending on the type of material used for the layer 123, corresponding deposition techniques may be used. For instance, polysilicon, aluminum, tungsten, tungsten silicide, and the like may readily be deposited on the basis of well-established chemical vapor deposition (CVD) techniques. In other

cases, plating methods such as electroplating or electroless plating may be used for reliably filling the respective openings above the first and second semiconductor regions 107a, 107b. Thereafter, any excess material of the layer 123 may be removed by any appropriate technique, such as etching, chemical mechanical polishing, and any combination thereof.

Figure 1h schematically shows the semiconductor device 100 with the excess material of the layer 123 removed and with a further interlayer dielectric 126 formed as the uppermost layer of the resulting structure. Thus, the device 100 comprises a gate electrode structure 124a above the first semiconductor region 107a and a second gate electrode structure 124b above the second semiconductor region 107b, thereby defining a first transistor element 130a and a second transistor element 130b. Moreover, as shown in Figure 1h, the layer portion 108a provides the first intrinsic stress 118a acting substantially homogeneously on the gate electrode structure 124a up to a height 125a, whereas the second layer portion 111b provides the second intrinsic stress 121b that acts substantially homogeneously on the second gate electrode structure 124b up to a height 125b thereof. Consequently, depending on the stresses 118a, 121b, respective deformations or strains are achieved in the associated semiconductor regions or channel regions 107a, 107b. Hence, the charge carrier mobility in these channel regions is individually adjustable by correspondingly controlling the stress 118a, 121b. In particular, the transistor configuration as shown in Figure 1h is substantially planar and enables a self-aligned formation of the doped regions 106a, 106b, *i.e.*, the respective drain and source regions, with respect to the associated gate electrode structures 124a, 124b. Moreover, the gate electrode structures 124a, 124b may be formed of a highly conductive material, such as a metal, metal compound, highly doped polysilicon, or any combination thereof, and the like. In particular embodiments, the gate electrode structures 124a, 124b are substantially comprised of a metal.

Figure 2 schematically shows a semiconductor device 200 in an intermediate manufacturing stage in accordance with further illustrative embodiments of the present invention. In Figure 2, identical or similar components as are shown in Figures 1d and 1e are denoted by the same reference signs except for a leading "2" instead of a "1." Hence, the device 200 comprises the substrate 201 with the semiconductor layer 202 formed thereon including the first and second semiconductor regions 207a, 207b with the associated doped regions 206a, 206b. The place holders 204a, 204b are laterally embedded into the dielectric layer 208 having a specified intrinsic stress. Moreover, the resist mask 210 is formed above the dielectric layer 208 to expose that portion of the device 200 that is associated with the second semiconductor region 207b. Regarding the formation of the device 200 as shown in Figure 2, it is referred to the description with reference to Figures 1a, 1b and 1c.

Moreover, the device 200 is subjected to an ion bombardment 240 to modify the stress characteristics of a layer portion 208b of the dielectric layer 208, which is not covered by the resist mask 210. For example, heavy inert ions, such as xenon, argon, silicon, and the like, may be implanted into the portion 208b, thereby relaxing, at least partially, the specified intrinsic stress. Consequently, the layer portion 208a maintains the specified intrinsic stress, thereby creating a specified deformation within the first semiconductor region 207a, while the corresponding strain in the second semiconductor region 207b may significantly differ therefrom, depending on the degree of relaxation within the layer portion 208b. For example, the dielectric layer 208 may have been deposited with a high compressive stress, for instance when the regions 206a, 207a are to represent a P-type transistor configuration, to significantly improve the hole mobility in the first semiconductor region 207a. By relaxing the initially compressive stress in the layer portion 208b to a specified degree, the amount of reduction of electron mobility within the second semiconductor region 207b, when designed as an N-type channel region, may

then be adjusted in accordance with design requirements. As already previously stated, the first and second semiconductor regions 207a, 207b may not necessarily need to represent different types of channel regions but may also represent identical channel regions, wherein for instance a different degree of operational behavior or a desired degree for adjustment of device uniformity may be achieved by the process technique as shown in Figure 2.

The further processing of the device 200 may then be continued as is also described with reference to the device 100 depicted in Figures 1e-1h.

Figure 3a schematically shows a semiconductor device 300 in accordance with further illustrative embodiments of the present invention. The device 300 may represent a device similar to that shown in Figure 1e so that similar or identical components are denoted by the same reference numbers except for a leading "3" instead of a "1." Thus, a detailed description of these components is omitted here. Moreover, the device 300 is subjected to an ion implantation 350 for inserting a light ion species, such as hydrogen, helium or oxygen, into the semiconductor layer 302 or the substrate 301. The ion implantation 350 is performed with a high dose and an appropriate energy to achieve a high impurity concentration at a desired depth within the layer 302 and/or the substrate 301. For example, initially implanted peak concentration may be selected to achieve a concentration in the range of approximately 10^{21} - 10^{23} atoms/cm³. Typical implantation parameters for helium or hydrogen may be approximately 3-15 keV, depending on the desired penetration depth with a dose of approximately 5×10^{15} to 2×10^{16} ions per cm². Thereafter, a heat treatment may be performed, for instance at temperatures of approximately 350-1,000°C and typically at approximately 700-950°C for a time period of several minutes to create "bubbles" or "voids" 351 within the layer 302 and/or the substrate 301. Since the ion implantation 350 is performed through the layer portions 308a, 311b with the place holders 304a, 304b still being present, a substantially uniform depth for the bubbles 351 is achieved. Since a light inert species is introduced, the stop mechanism during the implantation is mainly based on an interaction with crystal electrons so that damage in the layers 308a, 311b and thus stress relaxation is negligible. Due to the bubbles 351, a certain degree of mechanical decoupling of the regions 306a, 307a, 306b, 307b from the remaining layer 302 and/or the substrate 301 is achieved, thereby significantly enhancing the transfer of stress from the layer portions 308a, 311b into the respective regions 307a, 307b. Thus, the strain engineering of the regions 307a, 307b may significantly be enhanced and thus the charge carrier mobility and the channel conductivity may be improved more efficiently.

It should be appreciated that in other embodiments the ion implantation 350 may be performed at an earlier manufacturing stage, for instance prior to the formation of the layer portions 308a, 311b and possibly prior to the formation of the place holders 304a, 304b, thereby avoiding any relaxation effects, even though they may be very small as explained above. The bubbles 351 may then be created during any anneal cycles for activating the dopants in the region 306a, 306b.

Figure 3b schematically shows the semiconductor device 300, in which the place holders 304a, 304b are removed prior to the ion implantation 350. In this case, the implantation energy may be selected to position the light ion species within the semiconductor layer 302 substantially without affecting the regions 306a, 306b. Hence, the semiconductor regions 307a, 307b may highly efficiently be decoupled from the remaining semiconductor layer 302 by means of the bubbles 351. Thus, the stress transferred to the regions 307a, 307b is also significantly increased. Moreover, the bubbles 351 themselves may act as a source of stress, thereby also creating a corresponding strain within the respective regions 307a, 307b. In this way, two effective strain-inducing mechanisms may be combined.

As a result, the present invention provides a semiconductor device and a technique for forming the same wherein different semiconductor regions may receive a different strain, while the formation process allows the formation of planar transistor architectures including highly conductive gate electrodes. For this purpose, a dielectric layer laterally enclosing the gate electrode structures of various transistor elements is locally modified such that at least two different strain components are obtained in the respective channel regions. Thus, complementary transistor pairs may be formed, each transistor having a differently strained channel region. The modification of the strain-inducing stress layer may be accomplished by removing a specified portion of the layer and replacing it with a layer portion of a different intrinsic stress and/or by relaxing the intrinsic stress to a desired degree. Furthermore, due to the combination of the enhanced stress or strain engineering technique with a process for in-laid gate electrode structures, extremely highly conductive gate electrode structures may be attained, thereby providing enhanced gate and channel conductivity even for extremely scaled devices having a gate length of 100 nm and significantly less. Additionally, the local stress modification may advantageously be combined with mechanisms for effectively decoupling the channel regions from the surrounding material, thereby remarkably enhancing the efficiency of stress transfer into the respective channel regions.

The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. For example, the process steps set forth above may be performed in a different order. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

CLAIMS**WHAT IS CLAIMED:**

1. A method, comprising:
forming a first place holder structure 104a above a first semiconductor region 107a formed in a semiconductor layer 102 located on a substrate 101;
forming a second place holder structure 104b above a second semiconductor region 107b formed in said semiconductor layer 102;
depositing a dielectric layer 108 having a specified intrinsic stress above said semiconductor layer 102 to enclose said first and second place holder structures 104a, 104b;
modifying a portion of said dielectric layer 108 enclosing said second place holder structure 104b to change said intrinsic stress of said portion; and
replacing said first and second place holder structures 104a, 104b with a conductive material.
2. The method of claim 1, further comprising forming doped regions 106a, 106b in said semiconductor layer 102 adjacent to said first and second semiconductor regions 107a, 107b.
3. The method of claim 2, wherein forming said doped regions 106a, 106b comprises introducing at least one dopant species by an ion implantation process while using said first and second place holder structures as an implantation mask.
4. The method of claim 3, wherein forming said doped regions 106a, 106b comprises forming at least one sidewall spacer element on sidewalls of each of said first and second place holder structures and using said at least one sidewall spacer as an implantation mask at least during one step of said ion implantation process.
5. The method of claim 5, further comprising removing said at least one sidewall spacer prior to depositing said dielectric layer 108.
6. The method of claim 1, wherein modifying said portion surrounding said second place holder structure 104b comprises removing said portion.
7. The method of claim 7, further comprising depositing a second dielectric layer 126 above said semiconductor layer 102, said second dielectric layer 126 having a second intrinsic stress that differs from the intrinsic stress of said dielectric layer 108.
8. The method of claim 8, further comprising removing material of said second dielectric layer 126 to expose a top surface of said second place holder structure 104b.
9. The method of claim 7, further comprising planarizing a surface of said second dielectric layer 126 prior to removing said portion surrounding said second place holder structure 104b.

10. The method of claim 1, wherein modifying said portion surrounding said second place holder structure 104b comprises selectively relaxing said intrinsic stress in said portion.

11. The method of claim 10, wherein said intrinsic stress is selectively relaxed by ion bombardment of said portion.

12. The method of claim 1, further comprising implanting an inert species into an area adjacent to at least one of said first semiconductor region 107a and said second semiconductor region 107b and heat treating said substrate to form voids caused by said inert species.

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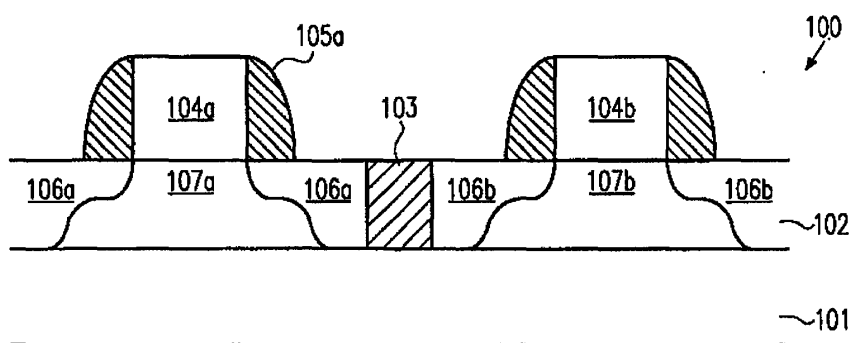


Fig.1a

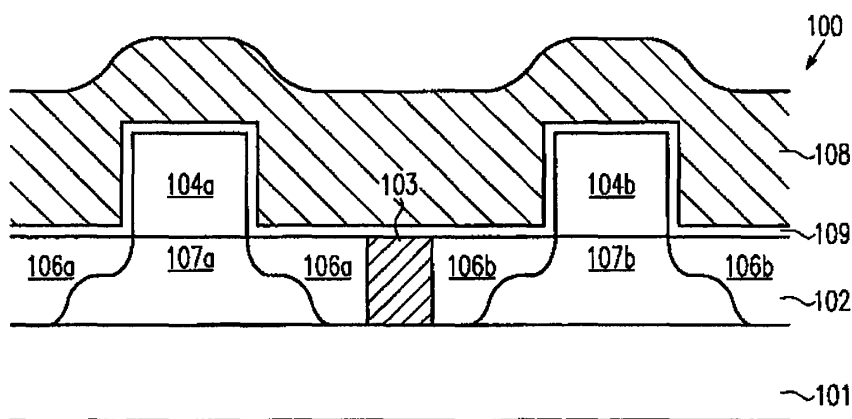


Fig.1b

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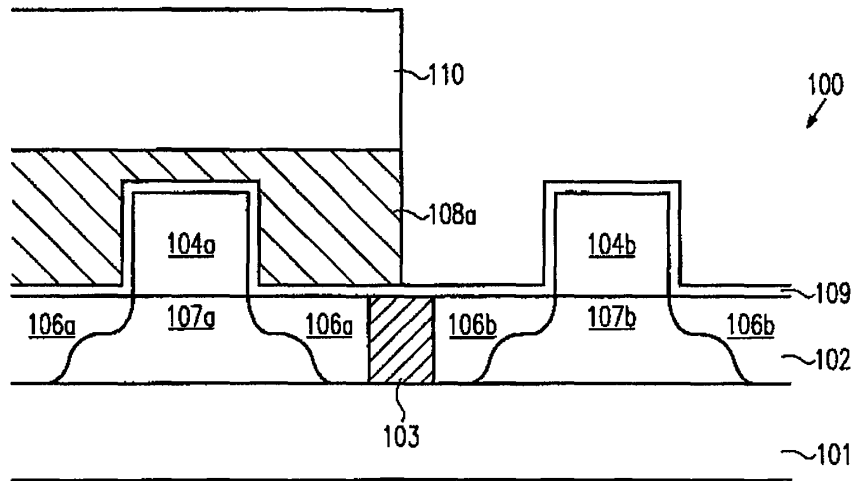


Fig.1c

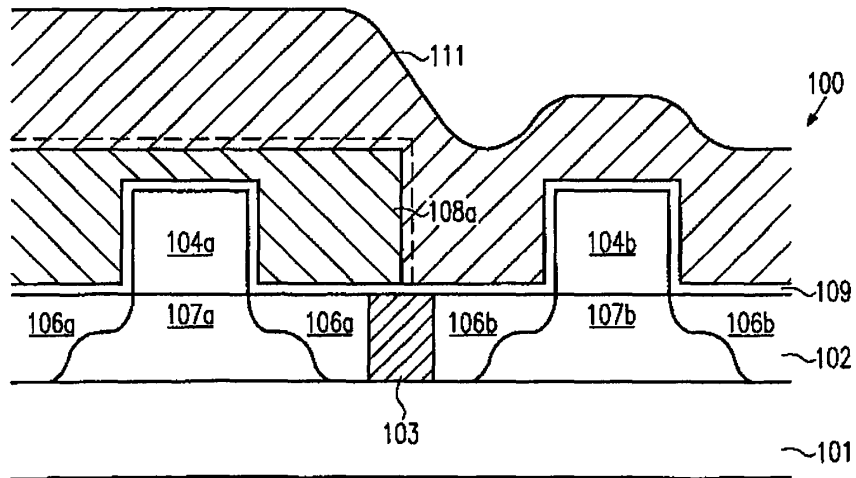
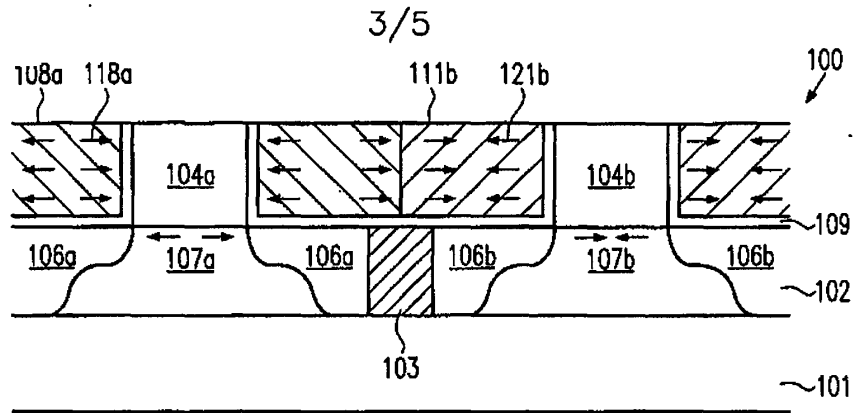
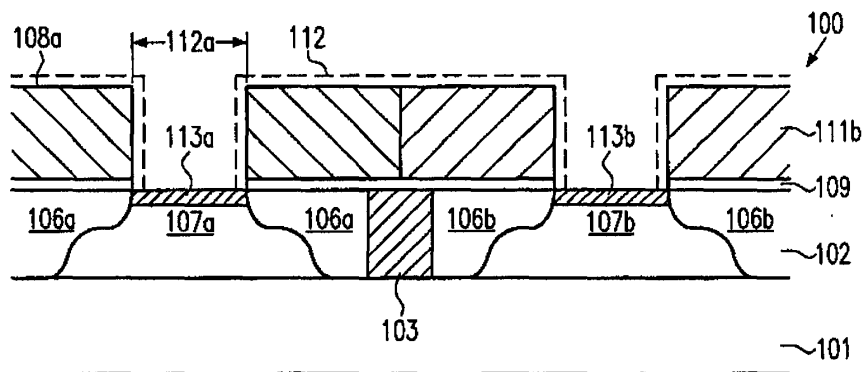
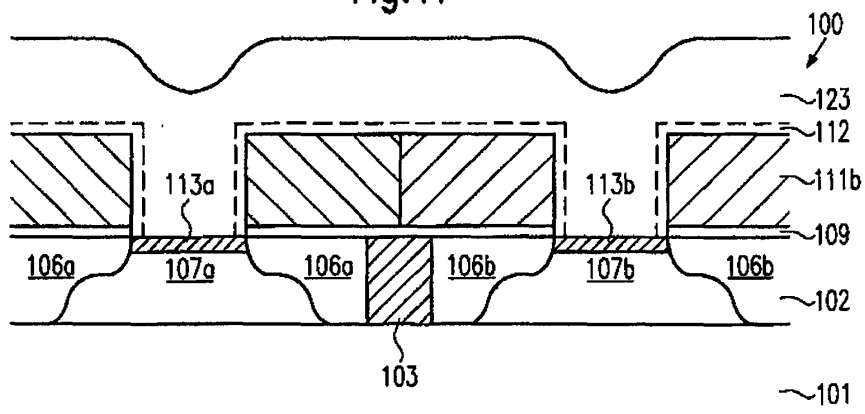


Fig.1d



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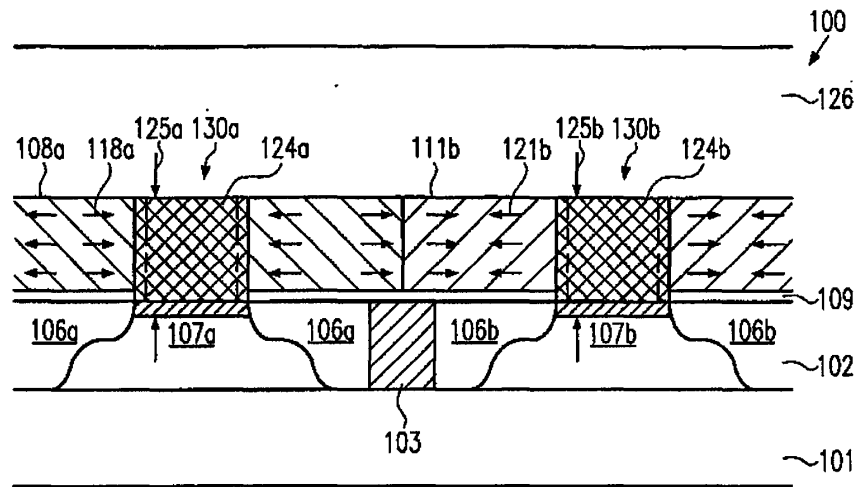


Fig.1h

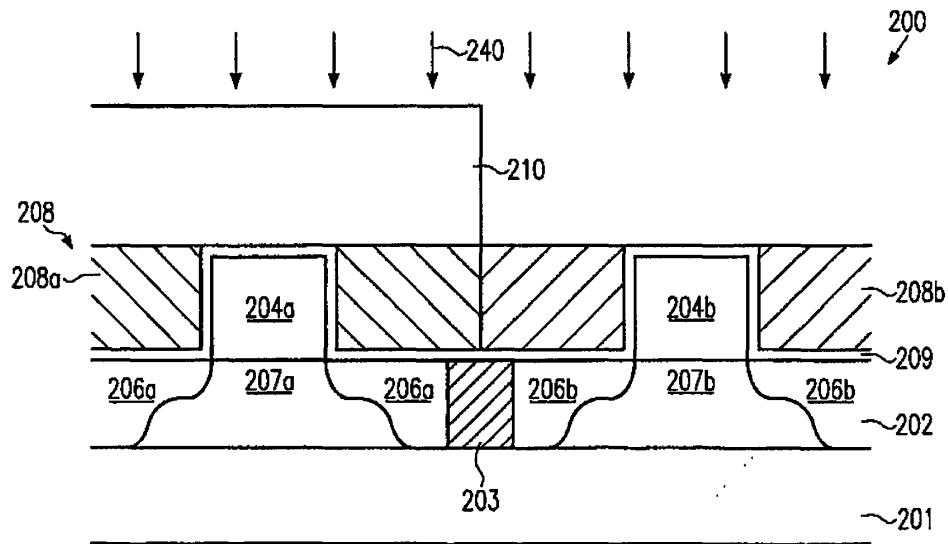


Fig.2

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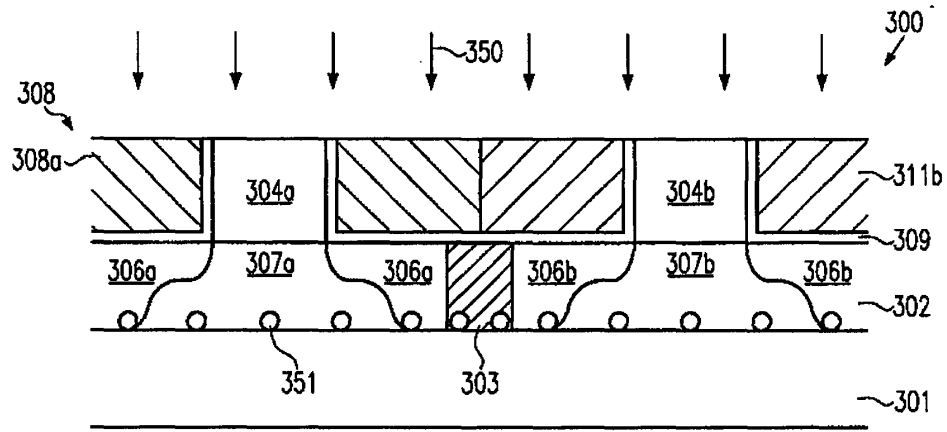


Fig.3a

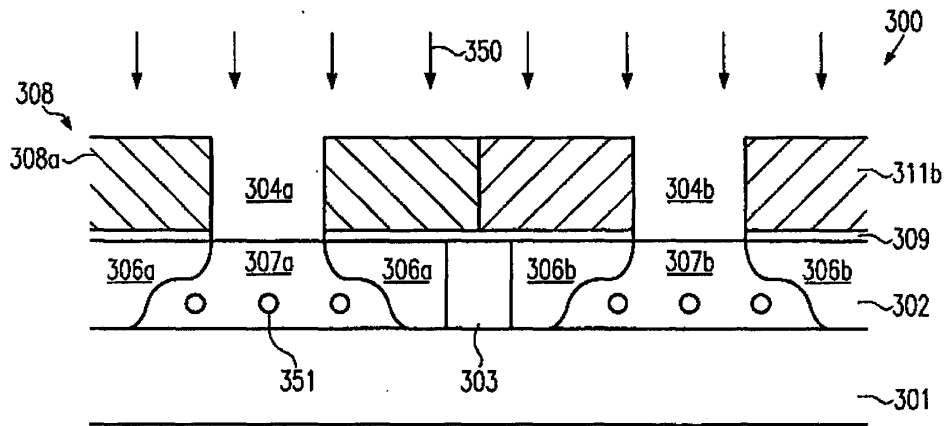


Fig.3b

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2005/036779

A. CLASSIFICATION OF SUBJECT MATTER
H01L21/8238 H01L21/336 H01L21/265

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2004/075148 A1 (KUMAGAI YUKIHIRO ET AL) 22 April 2004 (2004-04-22) figures 9-22	1-12
Y	US 6 376 888 B1 (TSUNASHIMA YOSHITAKA ET AL) 23 April 2002 (2002-04-23) figures 16-11 column 6, line 11 - line 19; figures 4-7 ----- -/-	1-12

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search

6 March 2006

Date of mailing of the international search report

14/03/2006

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Authorized officer

Nesso, S

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2005/036779

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	SHIMIZU A ED - INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS: "Local mechanical-stress control (LMC) a new technique for CMOS-performance enhancement" INTERNATIONAL ELECTRON DEVICES MEETING 2001. IEDM. TECHNICAL DIGEST. WASHINGTON, DC, DEC. 2 - 5, 2001, NEW YORK, NY : IEEE, US, 2 December 2001 (2001-12-02), pages 1941-1944, XP010575160 ISBN: 0-7803-7050-3 abstract; figure 1	10-12
A	US 2004/113217 A1 (CHIDAMBARRAO DURESETI ET AL) 17 June 2004 (2004-06-17) figures 4a,4b	5
A	US 2004/124492 A1 (MATSUO KOUJI) 1 July 2004 (2004-07-01) figures 8A-10C	1-12
A	US 2004/212035 A1 (YEO YEE-CHIA ET AL) 28 October 2004 (2004-10-28) the whole document	1-12

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2005/036779

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2004075148 A1	22-04-2004	CN 1505839 A WO 0247167 A1 JP 2003086708 A TW 518749 B	16-06-2004 13-06-2002 20-03-2003 21-01-2003
US 6376888 B1	23-04-2002	JP 2000315789 A	14-11-2000
US 2004113217 A1	17-06-2004	CN 1532912 A US 2005040460 A1	29-09-2004 24-02-2005
US 2004124492 A1	01-07-2004	JP 3651802 B2 JP 2004128491 A	25-05-2005 22-04-2004
US 2004212035 A1	28-10-2004	CN 1540757 A SG 115690 A1 TW 222715 B US 2005156274 A1	27-10-2004 28-10-2005 21-10-2004 21-07-2005

Form PCT/ISA/210 (patent family annex) (April 2005)

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME		
First Named Inventor/Applicant Name:		Yoshihiro SATO		
Filer:		Michael E. Fogarty/Kathrina Maramba		
Attorney Docket Number:		085393-0059		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1090

Electronic Acknowledgement Receipt	
EFS ID:	6558554
Application Number:	12629508
International Application Number:	
Confirmation Number:	7931
Title of Invention:	SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Yoshihiro SATO
Customer Number:	53080
Filer:	Michael E. Fogarty/Kathrina Maramba
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0059
Receipt Date:	02-DEC-2009
Filing Date:	
Time Stamp:	16:05:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1090
RAM confirmation Number	2525
Deposit Account	500417
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	P051653-01_TRN_085393-0059.PDF	192051	no	5
			b233cfabce667ceb0b484497d6b3a7184e486893		
Warnings:					
Information:					
2		P051653-01_APP_085393-0059.PDF	3184053	yes	75
			6a6492aab01160f0b37c4d7ef33f98744539a4a3		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	53	
	Claims		54	60	
	Abstract		61	61	
	Drawings-only black and white line drawings		62	75	
Warnings:					
Information:					
3	Oath or Declaration filed	P051653-01_DEC_085393-0059.PDF	132235	no	2
			896c01e8e3a5395bf4a8df5b6ef1319c2d55d46b		
Warnings:					
Information:					
4	Information Disclosure Statement (IDS) Filed (SB/08)	P051653-01_IDS_085393-0059.PDF	122347	no	3
			6a3923d3d398a9fbb8ba28efeced157e97fdb13392		
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
5	Miscellaneous Incoming Letter	085393-0059_pct.PDF	784515	no	17
			4f2119db74e2ab5cd9ffa9660032e0722e54c7a		
Warnings:					
Information:					
6		085393-0059_4refs4npl.PDF	2988393	yes	45
			89e4252937e31a0ce79d34f3a4a63c8a48eb09b3		

Multipart Description/PDF files in .zip description					
Document Description			Start	End	
Foreign Reference			1	1	
Foreign Reference			2	12	
Foreign Reference			13	13	
Foreign Reference			14	37	
NPL Documents			38	39	
NPL Documents			40	41	
NPL Documents			42	43	
NPL Documents			44	45	
Warnings:					
Information:					
7	Fee Worksheet (PTO-875)	fee-info.pdf	33013	no	2
			ba04894adedaf12ffa44846824188072a7d0b589		
Warnings:					
Information:					
Total Files Size (in bytes):			7436607		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

12/02/09

PTO/SB/06 (12-04)

Approved for use through 7/31/2006. OMB 0651-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 12/629,508	
APPLICATION AS FILED – PART I					
(Column 1)		(Column 2)		SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 = *	X 26=		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *	X 110=		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR				
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			N/A		
			TOTAL		
			OR		
			OTHER THAN SMALL ENTITY		
			RATE (\$)	FEE (\$)	
			N/A	330	
			N/A	540	
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			X 220=		
			N/A		
			TOTAL		1090
* If the difference in column 1 is less than zero, enter "0" in column 2.					
APPLICATION AS AMENDED – PART II					
(Column 1)		(Column 2)		(Column 3)	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		
	Total (37 CFR 1.16(i))	Minus **	=		
	Independent (37 CFR 1.16(h))	Minus ***	=		
	Application Size Fee (37 CFR 1.16(s))				
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))				
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				TOTAL	
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				TOTAL	
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				OTHER THAN SMALL ENTITY	
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				X =	
				X =	
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				TOTAL	
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				OR	
				OTHER THAN SMALL ENTITY	
				RATE (\$)	ADDITIONAL FEE (\$)
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/629,508	12/02/2009	2811	1090	085393-0059	20	2

CONFIRMATION NO. 7931

McDERMOTT WILL & EMERY LLP
600 13th Street, N.W.
Washington, DC 20005-3096

FILING RECEIPT



OC000000039231837

Date Mailed: 12/17/2009

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Yoshihiro SATO, Hyogo, JAPAN;
Hisashi Ogawa, Osaka, JAPAN;

Assignment For Published Patent Application

PANASONIC CORPORATION, Osaka, JAPAN

Power of Attorney: The patent practitioners associated with Customer Number 53080

Domestic Priority data as claimed by applicant

This application is a CON of PCT/JP2009/000574 02/13/2009

Foreign Applications

JAPAN 2008-064435 03/13/2008

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 12/14/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/629,508**

Projected Publication Date: 03/25/2010

Non-Publication Request: No

Early Publication Request: No

page 1 of 3

Title

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

Preliminary Class

257

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JAPAN PATENT OFFICE

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This is to certify that the annexed is a true copy of the following application as filed with this Office.

出 願 年 月 日
Date of Application: 2008年 3月13日

出 願 番 号
Application Number: 特願2008-064435

パリ条約による外国への出願
に用いる優先権の主張の基礎
となる出願の国コードと出願
番号
The country code and number
of your priority application,
to be used for filing abroad
under the Paris Convention, is

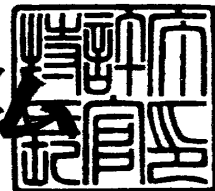
JP2008-064435

出 願 人
Applicant(s): パナソニック株式会社

2010年 1月13日

特許庁長官
Commissioner,
Japan Patent Office

細野 哲弘



【書類名】	特許願
【整理番号】	2926490199
【提出日】	平成20年 3月13日
【あて先】	特許庁長官殿
【国際特許分類】	H01L 29/78
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【弁理士】	
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【識別番号】	100113262
【弁理士】	
【氏名又は名称】	竹内 祐二
【選任した代理人】	
【識別番号】	100115059
【弁理士】	
【氏名又は名称】	今江 克実
【選任した代理人】	
【識別番号】	100115691
【弁理士】	
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【書類名】特許請求の範囲

【請求項 1】

第 1 の M I S トランジスタと第 2 の M I S トランジスタとを備えた半導体装置において

、
前記第 1 の M I S トランジスタは、
半導体基板における第 1 の活性領域上に形成された第 1 のゲート絶縁膜と、
前記第 1 のゲート絶縁膜上に形成された第 2 の金属膜からなる第 1 のゲート電極と、
前記第 1 のゲート電極の側面上から前記第 1 の活性領域における前記第 1 のゲート電極
の側方に位置する領域の上面上に跨って形成された絶縁膜とを備え、
前記第 2 の M I S トランジスタは、
前記半導体基板における第 2 の活性領域上に形成された第 2 のゲート絶縁膜と、
前記第 2 のゲート絶縁膜上に形成され第 1 の金属膜と前記第 1 の金属膜上に形成された
導電膜とからなる第 2 のゲート電極と、
前記第 2 のゲート電極の側面上から前記第 2 の活性領域における前記第 2 のゲート電極
の側方に位置する領域の上面上に跨って形成された前記絶縁膜とを備え、
前記第 1 の金属膜と前記第 2 の金属膜とは、互いに異なる金属材料からなり、
前記第 1 のゲート電極及び前記第 2 のゲート電極の各上面上には、前記絶縁膜が形成さ
れていないことを特徴とする半導体装置。

【請求項 2】

請求項 1 に記載の半導体装置において、

前記第 1 の金属膜は、前記第 2 の金属膜に比べて膜厚が薄いことを特徴とする半導体装
置。

【請求項 3】

請求項 1 又は 2 に記載の半導体装置において、

前記第 1 の金属膜と前記第 2 の金属膜とは、互いに仕事関数が異なっていることを特徴
とする半導体装置。

【請求項 4】

請求項 1 ～ 3 のうちいずれか 1 項に記載の半導体装置において、

前記絶縁膜の膜厚は、前記第 1 のゲート電極の膜厚に比べて薄いことを特徴とする半導
体装置。

【請求項 5】

請求項 1 ～ 4 のうちいずれか 1 項に記載の半導体装置において、

前記導電膜は、前記第 2 の金属膜からなることを特徴とする半導体装置。

【請求項 6】

請求項 1 ～ 4 のうちいずれか 1 項に記載の半導体装置において、

前記導電膜は、シリコン膜からなり、

前記シリコン膜上に形成された金属シリサイド膜をさらに備えていることを特徴とする
半導体装置。

【請求項 7】

請求項 1 ～ 6 のうちいずれか 1 項に記載の半導体装置において、

前記第 1 のゲート絶縁膜は、前記第 2 のゲート絶縁膜と同じ絶縁材料からなることを特
徴とする半導体装置。

【請求項 8】

請求項 1 ～ 4、6 のうちいずれか 1 項に記載の半導体装置において、

前記第 1 のゲート絶縁膜は、前記第 2 のゲート絶縁膜と異なる絶縁材料からなることを
特徴とする半導体装置。

【請求項 9】

請求項 1 ～ 8 のうちいずれか 1 項に記載の半導体装置において、

前記第 1 のゲート電極の側面上に形成された断面形状が L 字状の第 1 の内側サイドウォ
ールと、

前記第2のゲート電極の側面上に形成された断面形状がL字状の第2の内側サイドウォールとをさらに備え、

前記絶縁膜は、前記第1の内側サイドウォール及び前記第2の内側サイドウォールの上に接して形成されていることを特徴とする半導体装置。

【請求項10】

請求項1～9のうちいずれか1項に記載の半導体装置において、

前記絶縁膜は、前記第1の活性領域におけるチャネル領域のゲート長方向に第1の応力を生じさせる応力絶縁膜であることを特徴とする半導体装置。

【請求項11】

請求項10に記載の半導体装置において、

前記第1のMISトランジスタは、n型MISトランジスタであり、

前記絶縁膜は、シリコン窒化膜からなり、

前記第1の応力は、引っ張り応力であることを特徴とする半導体装置。

【請求項12】

請求項1～11のうちいずれか1項に記載の半導体装置において、

前記第2の活性領域における前記第2のゲート電極の外側下方に形成されたソースドレイン領域をさらに備え、

前記ソースドレイン領域は、前記第2の活性領域に設けられたトレンチ内に形成され、前記第2の活性領域におけるチャネル領域のゲート長方向に第2の応力を生じさせるシリコン混晶層を含むことを特徴とする半導体装置。

【請求項13】

請求項12に記載の半導体装置において、

前記第2のMISトランジスタは、p型MISトランジスタであり、

前記シリコン混晶層は、SiGe層からなり、

前記第2の応力は、圧縮応力であることを特徴とする半導体装置。

【請求項14】

請求項1～13のうちいずれか1項に記載の半導体装置において、

前記第1のゲート絶縁膜及び前記第2のゲート絶縁膜は、比誘電率が10以上の金属酸化物からなる高誘電率膜を含むことを特徴とする半導体装置。

【請求項15】

半導体基板における第1の活性領域上に形成された第1のMISトランジスタと、前記半導体基板における第2の活性領域上に形成された第2のMISトランジスタとを有する半導体装置の製造方法であって、

前記第1の活性領域上に第1のゲート絶縁膜、第1の金属膜及び第1のシリコン膜を有する第1のゲート電極形成部を形成すると共に、前記第2の活性領域上に第2のゲート絶縁膜、第1の金属膜及び第2のシリコン膜を有する第2のゲート電極形成部を形成する工程(a)と、

前記工程(a)の後に、前記半導体基板上に前記第1のゲート電極形成部及び前記第2のゲート電極形成部を覆う絶縁膜を形成する工程(b)と、

前記第1のゲート電極形成部及び前記第2のゲート電極形成部の上に形成されている前記絶縁膜を除去して、前記第1のゲート電極形成部における前記第1のシリコン膜及び前記第2のゲート電極形成部における前記第2のシリコン膜の各上面を露出する工程(c)と、

前記工程(c)の後に、前記第1のゲート電極形成部における前記第1のシリコン膜及び前記第1の金属膜を順次除去して、前記第1の活性領域上に前記絶縁膜に囲まれた第1の凹部を形成する工程(d)と、

前記第1の凹部内に第2の金属膜を形成する工程(e)とを備え、

前記第1のMISトランジスタの第1のゲート電極は、前記第2の金属膜からなり、

前記第2のMISトランジスタの第2のゲート電極は、前記第2のゲート電極形成部における前記第1の金属膜を含むことを特徴とする半導体装置の製造方法。

【請求項 16】

請求項 15に記載の半導体装置の製造方法において、

前記工程(d)は、前記第1の活性領域上に前記第1のゲート絶縁膜が底面に露出する前記第1の凹部を形成すると共に、前記第2のゲート電極形成部における前記第2のシリコン膜を除去して、前記第2の活性領域上に前記絶縁膜に囲まれ、前記第1の金属膜が底面に露出する第2の凹部を形成する工程を含み、

前記工程(e)は、前記第1の凹部内における前記第1のゲート絶縁膜上に前記第2の金属膜を形成すると共に、前記第2の凹部内における前記第1の金属膜上に前記第2の金属膜を形成する工程を含み、

前記第2のゲート電極は、前記第2のゲート電極形成部における前記第1の金属膜と、前記第1の金属膜上に形成された前記第2の金属膜とからなることを特徴とする半導体装置の製造方法。

【請求項 17】

請求項 15に記載の半導体装置の製造方法において、

前記工程(d)は、前記第1の活性領域上に前記第1のゲート絶縁膜が底面に露出する前記第1の凹部を形成する工程を含み、

前記工程(e)は、前記第1の凹部内における前記第1のゲート絶縁膜上に前記第2の金属膜を形成する工程を含み、

前記工程(e)の後に、前記第2のシリコン膜上に金属シリサイド膜を形成する工程(f)をさらに備え、

前記第2のゲート電極は、前記第2のゲート電極形成部における前記第1の金属膜及び前記第2のシリコン膜からなることを特徴とする半導体装置の製造方法。

【請求項 18】

請求項 15に記載の半導体装置の製造方法において、

前記工程(d)は、前記第1のゲート電極形成部における前記第1のシリコン膜、前記第1の金属膜及び前記第1のゲート絶縁膜を順次除去して、前記第1の活性領域上に前記第1の活性領域が底面に露出する前記第1の凹部を形成する工程を含み、

前記工程(e)は、前記第1の凹部内に第3のゲート絶縁膜を形成すると共に、前記第3のゲート絶縁膜上に前記第2の金属膜を形成する工程を含み、

前記工程(e)の後に、前記第2のシリコン膜上に金属シリサイド膜を形成する工程(f)をさらに備え、

前記第2のゲート電極は、前記第2のゲート電極形成部における前記第1の金属膜及び前記第2のシリコン膜からなることを特徴とする半導体装置の製造方法。

【請求項 19】

請求項 15～18のうちのいずれか1項に記載の半導体装置の製造方法において、

前記工程(a)の後で、前記工程(b)の前に、前記第1のゲート電極形成部の側面上に断面形状がL字状の第1の内側サイドウォールを形成すると共に、前記第2のゲート電極形成部の側面上に断面形状がL字状の第2の内側サイドウォールを形成する工程(g)をさらに備え、

前記工程(b)において、前記絶縁膜を、前記第1の内側サイドウォール及び前記第2の内側サイドウォールの上に接して形成することを特徴とする半導体装置の製造方法。

【請求項 20】

請求項 15～19のうちのいずれか1項に記載の半導体装置の製造方法において、

前記工程(a)の後で、前記工程(b)の前に、前記第2の活性領域における前記第2のゲート電極形成部の外側下方にトレンチを形成する工程(h)と、前記トレンチ内に、前記第2の活性領域におけるチャネル領域のゲート長方向に応力を生じさせるシリコン混晶層を形成する工程(i)とをさらに備えていることを特徴とする半導体装置の製造方法。

【書類名】明細書

【発明の名称】半導体装置及びその製造方法

【技術分野】

【0001】

本発明は、半導体装置及びその製造方法に関し、特に金属材料からなるゲート電極を有するMISFET (Metal Insulator Semiconductor Field Effect Transistor) を備えた半導体装置及びその製造方法に関する。

【背景技術】

【0002】

半導体集積回路装置の高集積化及び高速化に伴い、MISFETの微細化が進められている。MISFETの微細化によるゲート絶縁膜の極薄膜化に伴い、ポリシリコンゲート電極の空乏容量の顕在化及びボロンのチャネル領域への突き抜けという問題がある。この問題の解決策として、n型MISFET (以下、「n型MISトランジスタ」と称す) のゲート電極として金属材料からなるメタルゲート電極を用いると共に、p型MISFET (以下、「p型MISトランジスタ」と称す) のゲート電極として金属材料からなるメタルゲート電極を用いたデュアルメタルゲート構造の半導体装置が検討されている。

【0003】

デュアルメタルゲート構造の半導体装置の場合、n型MISトランジスタのゲート電極と、p型MISトランジスタのゲート電極とが互いに異なる金属材料からなることが必要とされる。例えば、n型MISトランジスタのゲート電極は、4.05 eV以上で4.6 eV以下の仕事関数を有する金属材料からなる一方、p型MISトランジスタのゲート電極は、4.6 eV以上で5.15 eV以下の仕事関数を有する金属材料からなることが必要とされる。

【0004】

デュアルメタルゲート構造の半導体装置の製造方法としては、例えば、第1の従来の半導体装置の製造方法 (例えば非特許文献1参照)、及び第2の従来の半導体装置の製造方法 (例えば非特許文献2参照) が提案されている。

【非特許文献1】 Z. B. Zhang et al., "Integration of Dual Metal Gate CMOS with TaSiN (NMOS) and Ru (PMOS) Gate Electrodes on HfO₂ Gate Dielectric", VLSI2005

【非特許文献2】 S. C. Song et al., "Highly Manufacturable 45nm LSTP CMOSFETs Using Novel Dual High-k and Dual Metal Gate CMOS Integration", VLSI2006

【発明の開示】

【発明が解決しようとする課題】

【0005】

しかしながら、第1、第2の従来の半導体装置の製造方法では、以下に示す問題がある。

【0006】

以下に、第1の従来の半導体装置の製造方法及びその問題点について順に説明する。第1の従来の半導体装置の製造方法について、図13を参照しながら説明する。図13は、第1の従来の半導体装置の製造方法を示すゲート幅方向の要部工程断面図である。なお、図中において、左側に示す「nMIS」とはn型MISトランジスタが形成されるn型MIS形成領域を示し、右側に示す「pMIS」とはp型MISトランジスタが形成されるp型MIS形成領域を示している。

【0007】

まず、半導体基板100の上部に素子分離領域101を選択的に形成する。これにより、n型MIS形成領域には、素子分離領域101に囲まれた第1の活性領域100aが形成され、p型MIS形成領域には、素子分離領域101に囲まれた第2の活性領域100bが形成される。その後、半導体基板100におけるn型MIS形成領域にp型ウェル領域102aを形成する一方、半導体基板100におけるp型MIS形成領域にn型ウェル

領域102bを形成する。

【0008】

次に、半導体基板100上に、ゲート絶縁膜形成膜、n型MISトランジスタ用のゲート電極材料（以下、「nMIS用金属材料」と称す）からなる第1の金属膜、p型MISトランジスタ用のゲート電極材料（以下、「pMIS用金属材料」と称す）からなる第2の金属膜、及びシリコン膜を順次形成する。

【0009】

このようにして、図13に示すように、第1の活性領域100a上に、ゲート絶縁膜形成膜103a、第1の金属膜104a、第2の金属膜105a、及びシリコン膜106aが順次形成された第1のパターニング部107Aを形成すると共に、第2の活性領域100b上に、ゲート絶縁膜形成膜103b、第2の金属膜105b、及びシリコン膜106bが順次形成された第2のパターニング部107Bを形成する。

【0010】

その後、図示しないが、シリコン膜106a、106b上に形成されたゲートパターン形状を有するレジストをマスクにして、ドライエッチング法により、第1のパターニング部107Aをパターニングして、ゲート絶縁膜形成膜103aからなる第1のゲート絶縁膜、並びに第1の金属膜104a、第2の金属膜105a、及びシリコン膜106aからなる第1のゲート電極を形成すると共に、第2のパターニング部107Bをパターニングして、ゲート絶縁膜形成膜103bからなる第2のゲート絶縁膜、並びに第2の金属膜105b及びシリコン膜106bからなる第2のゲート電極を形成する。

【0011】

ここで、第1の従来の半導体装置の製造方法における問題点について説明する。第1の従来の半導体装置の製造方法では、図13に示すように、第1のパターニング部107Aと第2のパターニング部107Bとは、互いに構成が異なるにも拘わらず（詳細には、第1のパターニング部107Aの構成は4層構成であるのに対し、第2のパターニング部107Bの構成は3層構成である）、互いに同一の工程において、すなわち、互いに同一のエッチング条件の下、パターニングされるため、第1のゲート電極及び第2のゲート電極の双方を精度良く形成することができないという問題がある。例えば、エッチング条件を、第2のゲート電極が精度良く形成されるエッチング条件にした場合、第1のパターニング部107Aにおける第1の金属膜104a及びゲート絶縁膜形成膜103aがエッチングされずに残存するため、第1のゲート電極を精度良く形成することができない。一方、例えば、エッチング条件を、第1のゲート電極が精度良く形成されるエッチング条件にした場合、p型MIS形成領域の半導体基板100及び素子分離領域101中にエッチング割れが発生するので、第2のゲート電極を精度良く形成することができない。

【0012】

以下に、第2の従来の半導体装置の製造方法及びその問題点について順に説明する。第2の従来の半導体装置の製造方法について、図14(a)～(e)を参照しながら説明する。図14(a)～(e)は、第2の従来の半導体装置の製造方法を工程順に示すゲート幅方向の要部工程断面図である。なお、図中において、左側に示す「nMIS」とはn型MISトランジスタが形成されるn型MIS形成領域を示し、右側に示す「pMIS」とはp型MISトランジスタが形成されるp型MIS形成領域を示している。

【0013】

まず、半導体基板200の上部に素子分離領域201を選択的に形成する。これにより、n型MIS形成領域には、素子分離領域201に囲まれた第1の活性領域200aが形成され、p型MIS形成領域には、素子分離領域201に囲まれた第2の活性領域200bが形成される。その後、半導体基板200におけるn型MIS形成領域にp型ウェル領域202aを形成する一方、半導体基板200におけるp型MIS形成領域にn型ウェル領域202bを形成する。

【0014】

次に、半導体基板200上に、n型MISトランジスタ用のゲート絶縁膜材料（以下、

「nMIS用絶縁材料」と称す) からなる第1のゲート絶縁膜形成膜、nMIS用金属材料からなる第1の金属膜、及び第1のマスク膜を順次形成する。その後、図14(a)に示すように、フォトリソグラフィ法により、第1のマスク膜上にn型MIS形成領域を覆うレジストマスク206を形成する。

【0015】

次に、レジストマスク206をマスクにして、第1のマスク膜をエッチングして、第1のマスク膜205aを形成した後、レジストマスク206を除去する。その後、第1のマスク膜205aをマスクにして、第1の金属膜204、及び第1のゲート絶縁膜形成膜203を順次エッチングする。

【0016】

次に、図14(b)に示すように、半導体基板200上に、p型MISトランジスタ用のゲート絶縁膜材料(以下、「pMIS用絶縁材料」と称す) からなる第2のゲート絶縁膜形成膜207、pMIS用金属材料からなる第2の金属膜208、及び第2のマスク膜209を順次形成する。その後、フォトリソグラフィ法により、第2のマスク膜209上にp型MIS形成領域を覆うレジストマスク210を形成する。

【0017】

次に、図14(c)に示すように、レジストマスク210をマスクにして、第2のマスク膜209をエッチングして、第2のマスク膜209bを形成した後、レジストマスク210を除去する。その後、第2のマスク膜209bをマスクにして、第2の金属膜208、及び第2のゲート絶縁膜形成膜207を順次エッチングする。

【0018】

次に、図14(d)に示すように、第1、第2のマスク膜205a、209bを除去した後、第1の金属膜204及び第2の金属膜208上に、シリコン膜211を形成する。

【0019】

このようにして、図14(d)に示すように、第1の活性領域200a上に、第1のゲート絶縁膜形成膜203、第1の金属膜204、及びシリコン膜211が順次形成された第1のパターニング部を形成すると共に、第2の活性領域200b上に、第2のゲート絶縁膜形成膜207、第2の金属膜208、及びシリコン膜211が順次形成された第2のパターニング部を形成する。

【0020】

次に、図14(e)に示すように、フォトリソグラフィ法により、シリコン膜211上にゲートパターン形状を有するレジスト(図示せず)を形成した後、レジストをマスクにして、エッチング法により、第1のパターニング部をパターニングして、第1のゲート絶縁膜203a、並びに第1の金属膜204a及び第1のシリコン膜211aからなる第1のゲート電極212Aを形成すると共に、第2のパターニング部をパターニングして、第2のゲート絶縁膜207b、並びに第2の金属膜208b及び第2のシリコン膜211bからなる第2のゲート電極212Bを形成する。

【0021】

ここで、第2の従来の半導体装置の製造方法における問題点について、図15を参照しながら説明する。図15は、第2の従来の半導体装置の製造方法における問題点について示す平面図である。なお、図15に示すXIVe-XIVe線は、図14(e)に示す断面図の断面線に相当する。

【0022】

p型MIS形成領域を覆うレジストマスク210が、ゲート幅方向にずれて形成されて、図14(b)に示すように、レジストマスク210のゲート幅方向の端部が、n型MIS形成領域側に位置すると、図14(d)に示すように、素子分離領域201上に、第1のマスク膜205aの残部205c、第2のゲート絶縁膜形成膜207の残部207c、及び第2の金属膜208の残部208cからなる残部rが突出して形成される。

【0023】

この残部rが形成された状態でパターニングを行うと、図15に示すように、素子分離

領域201上に、ゲート長方向に伸びるように、パターニングされた残部rp（なお、パターニングされた残部rpは、図14(e)に示すように、パターニングされた残部205cpと、パターニングされた残部207cpと、パターニングされた残部208cpとからなる）が残存する。加えて、パターニングされた残部rpのゲート幅方向の側面上に、シリコン膜211からなる側壁絶縁膜211cが形成される。

【0024】

パターニングされた残部rp（又は側壁絶縁膜211c）により、第1、第2のゲート電極212A、212Bが、第1、第2のゲート電極212A、212Bとゲート長方向に沿って隣り合う他の第1、第2のゲート電極（図示せず）と電気的に接続するため、第1、第2のゲート電極212A、212Bはゲート電極としての機能を果たさない。このように、第2の従来の半導体装置の製造方法では、第1、第2のゲート電極212A、212Bを形成することができないという問題がある。

【0025】

なお、この問題の要因として、p型MIS形成領域を覆うレジストマスク210がn型MIS形成領域側にずれて形成される場合を具体例に挙げて説明したが、仮にレジストマスク210がn型MIS形成領域側にずれて形成されることがなくとも、n型MIS形成領域を覆うレジストマスク206がp型MIS形成領域側にずれて形成されることにより、上記と同様の問題が生じる。すなわち、図14(a)に示す工程において、レジストマスク206が、p型MIS形成領域側にずれて形成された場合、図16に示すように、素子分離領域201上に残部rが突出して形成される。

【0026】

ここで、上記の問題は、素子分離領域201のゲート幅方向の幅を拡げることで回避することが可能である。すなわち、素子分離領域201に予め合わせマージン（余裕領域）を設けて、素子分離領域201のゲート幅方向の幅を拡げることで、図14(a)に示す工程において、レジストマスク206の形成の際に、レジストマスク206がゲート幅方向にずれて形成されることがあっても、レジストマスク206のゲート幅方向の端部を、p型MIS形成領域側に位置させずに、n型MIS形成領域側に位置させることができる。それと共に、図14(b)に示す工程において、レジストマスク210の形成の際に、レジストマスク210がゲート幅方向にずれて形成されることがあっても、レジストマスク210のゲート幅方向の端部を、n型MIS形成領域側に位置させずに、p型MIS形成領域側に位置させることができる。しかしながら、この場合、次に示す問題がある。すなわち、レジストマスク206の形成、及びレジストマスク210の形成の際に、素子分離領域201に合わせマージンが必要とされるため、素子分離領域201のゲート幅方向の幅を縮小化することができないという問題がある。

【0027】

さらに、第2の従来の半導体装置の製造方法では、図14(d)に示すように、第1のパターニング部と第2のパターニング部とは、互いに構成が異なるにも拘わらず（詳細には、第1、第2のパターニング部は、互いに同一のシリコン膜211を有するものの、互いに異なる第1、第2のゲート絶縁膜形成膜203、207及び第1、第2の金属膜204、208を有する）、言い換えれば、互いにエッチング特性が異なるにも拘わらず、互いに同一のエッチング条件の下、パターニングされるため、第1、第2のゲート電極の双方を精度良く形成することができないという問題もある。

【0028】

このように、第2の従来の半導体装置の製造方法では、第1、第2のゲート電極を形成することは可能なものの、第1、第2のゲート電極の双方を精度良く形成することはできず、さらに、素子分離領域201のゲート幅方向の幅を縮小化することができないという問題がある。

【0029】

以上のように、第1の従来の半導体装置の製造方法では、第1、第2のゲート電極の双方を精度良く形成することができないという問題がある。一方、第2の従来の半導体装置

の製造方法では、第1，第2のゲート電極の双方を精度良く形成することができないだけでなく、さらに、素子分離領域のゲート幅方向の幅を縮小化することができないという問題がある。

【0030】

前記に鑑み、本発明の目的は、互いに異なる金属材料からなるゲート電極を有するn型，p型MISトランジスタを備えた半導体装置において、精度良く形成されたn型，p型MISトランジスタのゲート電極を実現すると共に、ゲート幅方向の幅が縮小化された素子分離領域を実現することである。

【課題を解決するための手段】

【0031】

前記の目的を達成するために、本発明に係る半導体装置は、第1のMISトランジスタと第2のMISトランジスタとを備えた半導体装置において、第1のMISトランジスタは、半導体基板における第1の活性領域上に形成された第1のゲート絶縁膜と、第1のゲート絶縁膜上に形成された第2の金属膜からなる第1のゲート電極と、第1のゲート電極の側面上から第1の活性領域における第1のゲート電極の側方に位置する領域の上面上に跨って形成された絶縁膜とを備え、第2のMISトランジスタは、半導体基板における第2の活性領域上に形成された第2のゲート絶縁膜と、第2のゲート絶縁膜上に形成された第1の金属膜と第1の金属膜上に形成された導電膜とからなる第2のゲート電極と、第2のゲート電極の側面上から第2の活性領域における第2のゲート電極の側方に位置する領域の上面上に跨って形成された絶縁膜とを備え、第1の金属膜と第2の金属膜とは、互いに異なる金属材料からなり、第1のゲート電極及び第2のゲート電極の各上面上には、絶縁膜が形成されていないことを特徴とする。

【0032】

本発明に係る半導体装置によると、精度良く形成された第1，第2のゲート電極を実現することができる。加えて、ゲート幅方向の幅が縮小化された素子分離領域を実現することができるので、半導体装置の微細化を図ることができる。

【0033】

本発明に係る半導体装置において、第1の金属膜は、第2の金属膜に比べて膜厚が薄いことが好ましい。

【0034】

本発明に係る半導体装置において、第1の金属膜と第2の金属膜とは、互いに仕事関数が異なっていることが好ましい。

【0035】

本発明に係る半導体装置において、絶縁膜の膜厚は、第1のゲート電極の膜厚に比べて薄いことが好ましい。

【0036】

本発明に係る半導体装置において、導電膜は、第2の金属膜からなることが好ましい。

【0037】

本発明に係る半導体装置において、導電膜は、シリコン膜からなり、シリコン膜上に形成された金属シリサイド膜をさらに備えていることが好ましい。

【0038】

本発明に係る半導体装置において、第1のゲート絶縁膜は、第2のゲート絶縁膜と同じ絶縁材料からなることが好ましい。

【0039】

本発明に係る半導体装置において、第1のゲート絶縁膜は、第2のゲート絶縁膜と異なる絶縁材料からなることが好ましい。

【0040】

本発明に係る半導体装置において、第1のゲート電極の側面上に形成された断面形状がL字状の第1の内側サイドウォールと、第2のゲート電極の側面上に形成された断面形状がL字状の第2の内側サイドウォールとをさらに備え、絶縁膜は、第1の内側サイドウォ

ール及び第2の内側サイドウォールの上に接して形成されていることが好ましい。

【0041】

本発明に係る半導体装置において、絶縁膜は、第1の活性領域におけるチャネル領域のゲート長方向に第1の応力を生じさせる応力絶縁膜であることが好ましい。

【0042】

このようにすると、応力絶縁膜により、第1の活性領域におけるチャネル領域のゲート長方向に第1の応力を印加して、第1のMISトランジスタの駆動能力を向上させることができる。

【0043】

本発明に係る半導体装置において、第1のMISトランジスタは、n型MISトランジスタであり、絶縁膜は、シリコン窒化膜からなり、第1の応力は、引っ張り応力であることが好ましい。

【0044】

本発明に係る半導体装置において、第2の活性領域における第2のゲート電極の外側下方に形成されたソースドレイン領域をさらに備え、ソースドレイン領域は、第2の活性領域に設けられたトレンチ内に形成され、第2の活性領域におけるチャネル領域のゲート長方向に第2の応力を生じさせるシリコン混晶層を含むことが好ましい。

【0045】

このようにすると、シリコン混晶層により、第2の活性領域におけるチャネル領域のゲート長方向に第2の応力を印加して、第2のMISトランジスタの駆動能力を向上させることができる。

【0046】

本発明に係る半導体装置において、第2のMISトランジスタは、p型MISトランジスタであり、シリコン混晶層は、SiGe層からなり、第2の応力は、圧縮応力であることが好ましい。

【0047】

本発明に係る半導体装置において、第1のゲート絶縁膜及び第2のゲート絶縁膜は、比誘電率が10以上の金属酸化物からなる高誘電率膜を含むことが好ましい。

【0048】

前記の目的を達成するために、本発明に係る半導体装置の製造方法は、半導体基板における第1の活性領域上に形成された第1のMISトランジスタと、半導体基板における第2の活性領域上に形成された第2のMISトランジスタとを有する半導体装置の製造方法であって、第1の活性領域上に第1のゲート絶縁膜、第1の金属膜及び第1のシリコン膜を有する第1のゲート電極形成部を形成すると共に、第2の活性領域上に第2のゲート絶縁膜、第1の金属膜及び第2のシリコン膜を有する第2のゲート電極形成部を形成する工程(a)と、工程(a)の後に、半導体基板上に第1のゲート電極形成部及び第2のゲート電極形成部を覆う絶縁膜を形成する工程(b)と、第1のゲート電極形成部及び第2のゲート電極形成部の上に形成されている絶縁膜を除去して、第1のゲート電極形成部における第1のシリコン膜及び第2のゲート電極形成部における第2のシリコン膜の各上面を露出する工程(c)と、工程(c)の後に、第1のゲート電極形成部における第1のシリコン膜及び第1の金属膜を順次除去して、第1の活性領域上に絶縁膜に囲まれた第1の凹部を形成する工程(d)と、第1の凹部内に第2の金属膜を形成する工程(e)とを備え、第1のMISトランジスタの第1のゲート電極は、第2の金属膜からなり、第2のMISトランジスタの第2のゲート電極は、第2のゲート電極形成部における第1の金属膜を含むことを特徴とする。

【0049】

本発明に係る半導体装置の製造方法によると、互いに同一の工程において、第1、第2のゲート電極形成部を形成した後、第1のゲート電極形成部における第1のシリコン膜及び第1の金属膜を順次除去して形成された第1の凹部内に、第2の金属膜を形成して、第2の金属膜からなる第1のゲート電極を形成する。一方、第2のゲート電極形成部にお

る第1の金属膜を含む第2のゲート電極を形成する。そのため、第1のゲート電極形成部における第1のシリコン膜及び第1の金属膜を、第2の金属膜に置換するに当たっては、素子分離領域に合わせマージンが必要とされるものの、第1、第2のゲート電極形成部の際には、素子分離領域に合わせマージンは必要とされない。従って、素子分離領域に合わせマージンが必要とされる工程数を削減することができるため、合わせマージンのゲート幅方向の幅を狭くして、素子分離領域のゲート幅方向の幅を縮小化することができるので、半導体装置の微細化を図ることができる。

【0050】

加えて、互いに同一の工程において、互いに同一の構成の第1、第2のゲート電極形成部（言い換えれば、互いに同一のエッチング特性の第1、第2のゲート電極形成部）を形成するため、第1、第2のゲート電極形成部を容易に且つ精度良く形成することができる。これにより、精度良く形成された第1のゲート電極形成部における第1の金属膜及び第1のシリコン膜を、第2の金属膜と置換して、第2の金属膜からなる第1のゲート電極を形成することができる。一方、精度良く形成された第2のゲート電極形成部における第1の金属膜を含む第2のゲート電極を形成することができるため、精度良く形成された第1、第2のゲート電極を実現することができる。

【0051】

本発明に係る半導体装置の製造方法において、工程（d）は、第1の活性領域上に第1のゲート絶縁膜が底面に露出する第1の凹部を形成すると共に、第2のゲート電極形成部における第2のシリコン膜を除去して、第2の活性領域上に絶縁膜に囲まれ、第1の金属膜が底面に露出する第2の凹部を形成する工程を含み、工程（e）は、第1の凹部内における第1のゲート絶縁膜上に第2の金属膜を形成すると共に、第2の凹部内における第1の金属膜上に第2の金属膜を形成する工程を含み、第2のゲート電極は、第2のゲート電極形成部における第1の金属膜と、第1の金属膜上に形成された第2の金属膜とからなることが好ましい。

【0052】

このようにすると、第1のゲート電極形成部における第1の金属膜の除去の際には、素子分離領域に合わせマージンが必要とされるものの、第1、第2のゲート電極形成部の形成の際には、素子分離領域に合わせマージンは必要とされないため、素子分離領域に合わせマージンが必要とされる工程数を1回に抑えることができる。

【0053】

本発明に係る半導体装置の製造方法において、工程（d）は、第1の活性領域上に第1のゲート絶縁膜が底面に露出する第1の凹部を形成する工程を含み、工程（e）は、第1の凹部内における第1のゲート絶縁膜上に第2の金属膜を形成する工程を含み、工程（e）の後に、第2のシリコン膜上に金属シリサイド膜を形成する工程（f）をさらに備え、第2のゲート電極は、第2のゲート電極形成部における第1の金属膜及び第2のシリコン膜からなることが好ましい。

【0054】

このようにすると、第1のゲート電極形成部における第1のシリコン膜及び第1の金属膜の除去の際には、素子分離領域に合わせマージンが必要とされるものの、第1、第2のゲート電極形成部の形成の際には、素子分離領域に合わせマージンは必要とされないため、素子分離領域に合わせマージンが必要とされる工程数を1回に抑えることができる。

【0055】

本発明に係る半導体装置の製造方法において、工程（d）は、第1のゲート電極形成部における第1のシリコン膜、第1の金属膜及び第1のゲート絶縁膜を順次除去して、第1の活性領域上に第1の活性領域が底面に露出する第1の凹部を形成する工程を含み、工程（e）は、第1の凹部内に第3のゲート絶縁膜を形成すると共に、第3のゲート絶縁膜上に第2の金属膜を形成する工程を含み、工程（e）の後に、第2のシリコン膜上に金属シリサイド膜を形成する工程（f）をさらに備え、第2のゲート電極は、第2のゲート電極形成部における第1の金属膜及び第2のシリコン膜からなることが好ましい。

【0056】

このようにすると、第1のゲート電極形成部における第1のシリコン膜、第1の金属膜及び第1のゲート絶縁膜の除去の際には、素子分離領域に合わせマージンが必要とされるものの、第1、第2のゲート電極形成部の形成の際には、素子分離領域に合わせマージンは必要とされないため、素子分離領域に合わせマージンが必要とされる工程数を1回に抑えることができる。

【0057】

本発明に係る半導体装置の製造方法において、工程(a)の後で、工程(b)の前に、第1のゲート電極形成部の側面上に断面形状がL字状の第1の内側サイドウォールを形成すると共に、第2のゲート電極形成部の側面上に断面形状がL字状の第2の内側サイドウォールを形成する工程(g)をさらに備え、工程(b)において、絶縁膜を、第1の内側サイドウォール及び第2の内側サイドウォールの上に接して形成することが好ましい。

【0058】

本発明に係る半導体装置の製造方法において、工程(a)の後で、工程(b)の前に、第2の活性領域における第2のゲート電極形成部の外側下方にトレンチを形成する工程(h)と、トレンチ内に、第2の活性領域におけるチャネル領域のゲート長方向に応力を生じさせるシリコン混晶層を形成する工程(i)とをさらに備えていることが好ましい。

【発明の効果】

【0059】

本発明に係る半導体装置及びその製造方法によると、互いに同一の工程において、第1、第2のゲート電極形成部を形成した後、第1のゲート電極形成部における第1のシリコン膜及び第1の金属膜を順次除去して形成された第1の凹部内に、第2の金属膜を形成して、第2の金属膜からなる第1のゲート電極を形成する。一方、第2のゲート電極形成部における第1の金属膜を含む第2のゲート電極を形成する。そのため、第1のゲート電極形成部における第1のシリコン膜及び第1の金属膜を、第2の金属膜に置換するに当たっては、素子分離領域に合わせマージンが必要とされるものの、第1、第2のゲート電極形成部の際には、素子分離領域に合わせマージンは必要とされない。従って、素子分離領域に合わせマージンが必要とされる工程数を削減することができるため、合わせマージンのゲート幅方向の幅を狭くして、素子分離領域のゲート幅方向の幅を縮小化することができるので、半導体装置の微細化を図ることができる。

【0060】

加えて、互いに同一の工程において、互いに同一の構成の第1、第2のゲート電極形成部を形成するため、第1、第2のゲート電極形成部を容易に且つ精度良く形成することができる。これにより、精度良く形成された第1のゲート電極形成部における第1の金属膜及び第1のシリコン膜を、第2の金属膜と置換して、第2の金属膜からなる第1のゲート電極を形成することができる。一方、精度良く形成された第2のゲート電極形成部における第1の金属膜を含む第2のゲート電極を形成することができるため、精度良く形成された第1、第2のゲート電極を実現することができる。

【発明を実施するための最良の形態】

【0061】

以下に、本発明の各実施形態について、図面を参照しながら説明する。

【0062】

(第1の実施形態)

本発明の第1の実施形態に係る半導体装置及びその製造方法について図面を参照しながら説明する。

【0063】

以下に、本発明の第1の実施形態に係る半導体装置の製造方法について、図1(a)～(d)、図2(a)～(d)、図3(a)～(d)、図4(a)～(c)及び図5(a)～(c)を参照しながら説明する。図1(a)～図5(c)は、本発明の第1の実施形態に係る半導体装置の製造方法を工程順に示すゲート長方向の要部工程断面図である。なお、図中において、左側に示

す「nMIS」とはn型MISトランジスタが形成されるn型MIS形成領域を示し、右側に示す「pMIS」とはp型MISトランジスタが形成されるp型MIS形成領域を示している。

【0064】

まず、図1(a)に示すように、例えば埋め込み素子分離(Shallow Trench Isolation: STI)法により、例えばp型シリコンからなる半導体基板10の上部に、トレンチ内に絶縁膜が埋め込まれた素子分離領域11を選択的に形成する。これにより、n型MIS形成領域には、素子分離領域11に囲まれた半導体基板10からなる第1の活性領域10aが形成され、p型MIS形成領域には、素子分離領域11に囲まれた半導体基板10からなる第2の活性領域10bが形成される。その後、リソグラフィ法及びイオン注入法により、半導体基板10におけるn型MIS形成領域に、例えばB(ホウ素)等のp型不純物を注入する一方、半導体基板10におけるp型MIS形成領域に、例えばP(リン)等のn型不純物を注入した後、半導体基板10に対して例えば850℃、30秒間の熱処理を施すことにより、半導体基板10におけるn型MIS形成領域に、p型ウェル領域12aを形成する一方、半導体基板10におけるp型MIS形成領域に、n型ウェル領域12bを形成する。

【0065】

次に、図1(b)に示すように、例えば希釈フッ酸処理により、半導体基板10の表面を洗浄した後、例えばISSG(In-Situ Steam Generation)酸化法により、第1の活性領域10a及び第2の活性領域10b上に、例えば膜厚が0.8~1nm程度のシリコン酸化膜からなる下地膜(図示せず)を形成する。その後、例えば有機金属気相堆積(Metal Organic Chemical Vapor Deposition: MOCVD)法により、下地膜上に、例えば膜厚が2nmの高誘電率膜からなるゲート絶縁膜形成膜13を堆積する。ここで、ゲート絶縁膜形成膜13としては、比誘電率が10以上の金属酸化物からなる高誘電率膜を含むことが望ましい。

【0066】

その後、例えばCVD(Chemical Vapor Deposition)法、ALD(Atomic Layer Deposition)法、又はスパッタ法等により、例えば窒化チタン(TiN)からなる第1の金属膜14を堆積する。ここで、第1の金属膜14としては、p型MISトランジスタ用に最適化された金属材料又は金属化合物材料(以下、「pMIS用金属材料」と称す)からなり、4.6eV以上で5.15eV以下の仕事関数を有することが望ましい。そして、第1の金属膜14の具体例としては、TiN膜の他に、例えば、チタン(Ti)、ルテニウム(Ru)、白金(Pt)若しくはタンゲステン(W)等の金属、又はTi、Ru、Pt及びWのうち少なくとも1種以上の金属を含む窒化物、炭素窒化物若しくは珪素窒化物等が挙げられる。その後、例えばCVD法により、第1の金属膜14上に、例えば膜厚が100nmのポリシリコン膜からなるシリコン膜15を堆積した後、例えばCVD法により、シリコン膜15上に、例えば膜厚が30nmのシリコン酸化膜からなる保護膜16を堆積する。

【0067】

次に、図1(c)に示すように、フォトリソグラフィ法により、保護膜16上に、ゲートパターン形状を有するレジスト(図示せず)を形成する。その後、レジストをマスクにして、ドライエッチング法により、保護膜16、シリコン膜15、第1の金属膜14及びゲート絶縁膜形成膜13を順次パターニングする。これにより、第1の活性領域10a上に、第1のゲート絶縁膜13a、第1の金属膜14a、第1のシリコン膜15a及び第1の保護膜16aを順次形成すると共に、第2の活性領域10b上に、第2のゲート絶縁膜13b、第1の金属膜14b、第2のシリコン膜15b及び第2の保護膜16bを順次形成する。

【0068】

このようにして、第1の活性領域10a上に第1のゲート絶縁膜13a、第1の金属膜14a及び第1のシリコン膜15aを有する第1のゲート電極形成部14Aを形成すると

共に、第2の活性領域10b上に第2のゲート絶縁膜13b、第1の金属膜14b及び第2のシリコン膜15bを有する第2のゲート電極形成部14Bを形成する。

【0069】

次に、図1(d)に示すように、例えばCVD法により、半導体基板10上の全面に、例えば膜厚が10nmのシリコン酸化膜からなるオフセットスペーサ用絶縁膜を堆積した後、オフセットスペーサ用絶縁膜に対して異方性エッチングを行う。これにより、第1のゲート電極形成部14Aの側面上に第1のオフセットスペーサ17aを形成すると共に、第2のゲート電極形成部14Bの側面上に第2のオフセットスペーサ17bを形成する。

【0070】

その後、半導体基板10上にn型MIS形成領域を開口しp型MIS形成領域を覆うレジスト(図示せず)を形成した後、第1の活性領域10aに、第1のゲート電極形成部14Aをマスクにして、例えばAs(ヒ素)等のn型不純物を注入することにより、第1の活性領域10aにおける第1のゲート電極形成部14Aの側方下に接合深さが比較的浅いn型ソースドレイン領域(LDD領域又はエクステンション領域)18aを自己整合的に形成する。一方、半導体基板10上にn型MIS形成領域を覆いp型MIS形成領域を開口するレジスト(図示せず)を形成した後、第2の活性領域10bに、第2のゲート電極形成部14Bをマスクにして、例えばBF₃等のp型不純物を注入することにより、第2の活性領域10bにおける第2のゲート電極形成部14Bの側方下に接合深さが比較的浅いp型ソースドレイン領域(LDD領域又はエクステンション領域)18bを自己整合的に形成する。

【0071】

次に、図2(a)に示すように、例えばCVD法により、半導体基板10上の全面に、例えば膜厚が10nmのシリコン酸化膜からなる第1の絶縁膜、及び膜厚が30nmのシリコン窒化膜からなる第2の絶縁膜を順次堆積した後、第1の絶縁膜及び第2の絶縁膜に対して異方性エッチングを行う。これにより、第1のゲート電極形成部14Aの側面上に、第1のオフセットスペーサ17aを介して、断面形状がL字状の第1の絶縁膜からなる第1の内側サイドウォール19aと第1の内側サイドウォール19a上に形成された第2の絶縁膜からなる第1の外側サイドウォール20aとで構成された第1のサイドウォール20Aを形成すると共に、第2のゲート電極形成部14Bの側面上に、第2のオフセットスペーサ17bを介して、断面形状がL字状の第1の絶縁膜からなる第2の内側サイドウォール19bと第2の内側サイドウォール19b上に形成された第2の絶縁膜からなる第2の外側サイドウォール20bとで構成された第2のサイドウォール20Bを形成する。

【0072】

次に、図2(b)に示すように、例えばCVD法により、半導体基板10上の全面に、例えば膜厚が10nmのシリコン酸化膜からなる表面保護膜21を堆積する。

【0073】

次に、図2(c)に示すように、表面保護膜21上に、n型MIS形成領域を覆いp型MIS形成領域を開口するレジストマスク22を形成した後、第2の外側サイドウォール20b(シリコン窒化膜)と選択比のある異方性ドライエッチング法を用いて、p型MIS形成領域に形成されている表面保護膜21を除去して、n型MIS形成領域に表面保護膜21aを残存させる。これにより、第2の活性領域10bにおける第2のサイドウォール20Bの外側方下の領域、すなわち、ソースドレイン形成領域の表面を露出させる。

【0074】

次に、図2(d)に示すように、レジストマスク22を除去した後、表面保護膜21a(シリコン酸化膜)、第2の保護膜16b(シリコン酸化膜)、第2のオフセットスペーサ17b(シリコン酸化膜)、第2の内側サイドウォール19b(シリコン酸化膜)及び第2の外側サイドウォール20b(シリコン窒化膜)と選択比のあるドライエッチング法を用いる、又はこれらの膜と選択比のあるドライエッチング法及びウェットエッチング法を順次組み合わせて用いて、表面に露出されている第2の活性領域10bをエッチングする。これにより、第2の活性領域10bにおける第2のサイドウォール20Bの外側方下の

領域（すなわちソースドレイン形成領域）に、例えば深さが60nmのトレンチ23を形成する。このとき、第1の活性領域10aの表面は表面保護膜21aで覆われているため、第1の活性領域10aはエッチングされない。また、第1のシリコン膜15aの上面は第1の保護膜16a及び表面保護膜21aで順次覆われている一方、第2のシリコン膜15bの上面は第2の保護膜16bで覆われているため、第1、第2のシリコン膜15a、15bはエッチングされない。

【0075】

次に、図3(a)に示すように、例えばフッ酸処理により、トレンチ23内のエッチング残渣及び自然酸化膜等を除去した後、例えばCVD法により、例えばシランガス(SiH_4)及びゲルマンガス(GeH_4)を、例えばジボランガス(B_2H_6)等のp型ドーパントガスと共に例えば650～700℃の温度で供給することにより、トレンチ23内を充填するようにp型SiGe層からなるシリコン混晶層24をエピタキシャル成長させる。このとき、第1の活性領域10aの表面は表面保護膜21aで覆われているため、第1の活性領域10a上にSiGe層はエピタキシャル成長されない。また、第1のシリコン膜15aの上面は第1の保護膜16a及び表面保護膜21aで順次覆われている一方、第2のシリコン膜15bの上面は第2の保護膜16bで覆われているため、第1、第2のシリコン膜15a、15b上にSiGe層はエピタキシャル成長されない。

【0076】

その後、半導体基板10及び第1の外側サイドウォール20a（シリコン窒化膜）と選択比のあるドライエッチング法を用いる、又はこれらの膜と選択比のあるドライエッチング法及びウェットエッチング法を順次組み合わせ用いて、n型MIS形成領域に形成されている表面保護膜21aを除去して、第1の活性領域10aにおける第1のサイドウォール20Aの外側方下の領域、すなわち、ソースドレイン形成領域の表面を露出させる。

【0077】

このように図2(b)～図3(a)に示す工程を順次経ることにより、第2の活性領域10bにおける第2のサイドウォール20Bの外側方下に形成されたトレンチ23内に、第2の活性領域10bにおけるチャネル領域のゲート長方向に圧縮応力を生じさせるシリコン混晶層24を形成する。

【0078】

次に、図3(b)に示すように、リソグラフィ法及びイオン注入法により、第1の活性領域10aに、第1のゲート電極形成部14A、第1のオフセットスペーサ17a及び第1のサイドウォール20Aをマスクにして、例えばAs（ヒ素）等のn型不純物を注入することにより、第1の活性領域10aにおける第1のサイドウォール20Aの外側方下に、浅いn型ソースドレイン領域18aよりも深い接合深さを有し、接合深さが比較的深いn型ソースドレイン領域25aを自己整合的に形成する。一方、第2の活性領域10bに、第2のゲート電極形成部14B、第2のオフセットスペーサ17b及び第2のサイドウォール20Bをマスクにして、例えばB（ボロン）等のp型不純物を注入することにより、第2の活性領域10bにおける第2のサイドウォール20Bの外側方下に、浅いp型ソースドレイン領域18bよりも深い接合深さを有し、接合深さが比較的深いp型ソースドレイン領域25bを自己整合的に形成する。その後、熱処理により、深いn型ソースドレイン領域25a及び深いp型ソースドレイン領域25bに含まれる不純物を活性化させる。

【0079】

このように、深いp型ソースドレイン領域25bは、第2の活性領域10bに設けられたトレンチ23内に形成されたシリコン混晶層24を含むように形成される。

【0080】

次に、深いn型ソースドレイン領域25a及び深いp型ソースドレイン領域25bの表面に形成されている自然酸化膜（図示せず）を除去した後、例えばスパッタ法により、半導体基板10上の全面に、例えば膜厚が10nmのニッケルからなる金属膜（図示せず）を堆積する。その後、例えば窒素雰囲気中、320℃の下、1回目のRTA（Rapid Thermal Annealing）処理により、深いn型ソースドレイン領域25a及び深いp型ソース

ドレイン領域25bのSiと金属膜のNiとを反応させて、深いn型ソースドレイン領域25a及び深いp型ソースドレイン領域25bの上部に、ニッケルシリサイドからなる第1、第2の金属シリサイド膜26a、26bを形成する。

【0081】

その後、硫酸と過酸化水素水との混合液からなるエッチング液中に半導体基板10を浸漬することにより、素子分離領域11、第1、第2のオフセットスペーサ17a、17b及び第1、第2のサイドウォール20A、20B等の上に残存する未反応の金属膜を除去した後、1回目のRTA処理での温度よりも高い温度（例えば550℃）の下、2回目のRTA処理により、第1、第2の金属シリサイド膜26a、26bのシリサイド組成比を安定化させる。

【0082】

次に、図3(c)に示すように、例えば、第1、第2の内側サイドウォール19a、19b（シリコン酸化膜）と選択比のあるドライエッチング法を用いて、第1の外側サイドウォール20a（シリコン窒化膜）及び第2の外側サイドウォール20b（シリコン窒化膜）を除去する。

【0083】

次に、図3(d)に示すように、例えばプラズマCVD法により、半導体基板10上の全面に、例えば膜厚50nmのシリコン窒化膜からなる絶縁膜27を堆積する。

【0084】

このように、絶縁膜27は、表面に第1の保護膜16aが形成された第1のゲート電極形成部14A、及び表面に第2の保護膜16bが形成された第2のゲート電極形成部14Bを覆うように形成される。そして、絶縁膜27は、第1の外側サイドウォール20aが除去された断面形状がL字状の第1の内側サイドウォール19a、及び第2の外側サイドウォール20bが除去された断面形状がL字状の第2の内側サイドウォール19bの上に接して形成される。

【0085】

その後、例えばCVD法により、絶縁膜27上に、シリコン酸化膜からなる第1の層間絶縁膜28を堆積した後、例えばCMP（Chemical Mechanical Polishing）法により、第1の層間絶縁膜28の表面の平坦化を行いながら、第1の保護膜16a及び第2の保護膜16bの上に形成されている絶縁膜27の上面が露出するまで、第1の層間絶縁膜28を研磨除去する。

【0086】

次に、図4(a)に示すように、第1、第2のシリコン膜（ポリシリコン膜）15a、15bと選択比のあるドライエッチング法又はウェットエッチング法を用いて、第1のゲート電極形成部14A、及び第2のゲート電極形成部14Bの上に形成されている第1、第2の保護膜（シリコン酸化膜）16a、16b及び絶縁膜（シリコン窒化膜）27を除去して、第1のゲート電極形成部14Aにおける第1のシリコン膜15a、及び第2のゲート電極形成部14Bにおける第2のシリコン膜15bの上面を露出する。このとき、第1のゲート電極形成部14A及び第2のゲート電極形成部14Bの側方に形成されている第1、第2のオフセットスペーサ17a、17b、第1、第2の内側サイドウォール19a、19b、絶縁膜27、及び第1の層間絶縁膜28は、その上面高さが、第1、第2のシリコン膜15a、15bの上面高さと同じ又は同程度になるまで同時に除去される。

【0087】

このように、絶縁膜27は、第1、第2のゲート電極形成部14A、14Bの側面上から第1、第2の活性領域10a、10bにおける第1、第2のゲート電極形成部14A、14Bの側方に位置する領域の上面上に跨って形成される一方、第1、第2のゲート電極形成部14A、14Bの上面上には形成されない。

【0088】

次に、図4(b)に示すように、第1、第2の金属膜（TiN膜）14a、14b、第1、第2のオフセットスペーサ17a、17b、第1、第2の内側サイドウォール19a、

19b、絶縁膜27、及び第1の層間絶縁膜28と選択比のあるドライエッチング法又はウェットエッチング法を用いて、第1のゲート電極形成部14Aにおける第1のシリコン膜15a、及び第2のゲート電極形成部14Bにおける第2のシリコン膜15bを除去する。

【0089】

次に、図4(c)に示すように、半導体基板10上に、n型MIS形成領域を開口しp型MIS形成領域を覆うレジストマスク29を形成した後、第1のゲート絶縁膜13a、第1のオフセットスペーサ17a、第1の内側サイドウォール19a、絶縁膜27、及び第1の層間絶縁膜28と選択比のあるウェットエッチング法を用いて、第1のゲート電極形成部14Aにおける第1の金属膜14aを除去する。

【0090】

このように図4(b)～(c)に示す工程を順次経ることにより、第1のゲート電極形成部14Aにおける第1のシリコン膜15a及び第1の金属膜14aを順次除去して、第1の活性領域10a上に、第1のオフセットスペーサ17a及び第1の内側サイドウォール19aを順次介して絶縁膜27に囲まれ、第1のゲート絶縁膜13aが底面に露出する第1の凹部Caを形成する。それと共に、図4(b)に示す工程を経ることにより、第2のゲート電極形成部14Bにおける第2のシリコン膜15bを除去して、第2の活性領域10b上に、第2のオフセットスペーサ17b及び第2の内側サイドウォール19bを順次介して絶縁膜27に囲まれ、第1の金属膜14bが底面に露出する第2の凹部Cbを形成する。

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【0091】

次に、図5(a)に示すように、レジストマスク29を除去した後、半導体基板10上に、例えばCVD法、ALD法、又はスパッタ法等により、第1の凹部Ca及び第2の凹部Cb内を埋め込むように、例えば窒化タンタル(TaN)からなる第2の金属膜30を堆積する。ここで、第2の金属膜30としては、n型MISトランジスタ用に最適化された金属材料又は金属化合物材料(以下、「nMIS用金属材料」と称す)からなり、4.05eV以上で4.6eV以下の仕事関数を有することが望ましい。そして、第2の金属膜30の具体例としては、例えばTaNの他に、タンタル(Ta)若しくはハフニウム(Hf)等の金属、又はTa及びHfのうち少なくとも1種を含む窒化物、炭素窒化物若しくは珪素窒化物等が挙げられる。

【0092】

次に、図5(b)に示すように、例えばCMP法、又はエッチバック法により、絶縁膜27の上面が露出するまで、第2の金属膜30を除去する。これにより、第1の凹部Ca内における第1のゲート絶縁膜13a上に第2の金属膜30aを形成すると共に、第2の凹部Cb内における第1の金属膜14b上に第2の金属膜30bを形成する。

【0093】

このようにして、第1の活性領域10a上に、第1のゲート絶縁膜13aを介して、第2の金属膜30aからなる第1のゲート電極30Aを形成する一方、第2の活性領域10b上に、第2のゲート絶縁膜13bを介して、第1の金属膜14b及び第2の金属膜30bからなる第2のゲート電極30Bを形成する。

【0094】

次に、図5(c)に示すように、例えばCVD法により、第1の層間絶縁膜28上に、第1、第2のゲート電極30A、30Bを覆うように、第2の層間絶縁膜31を堆積した後、例えばCMP法により、第2の層間絶縁膜31の表面の平坦化を行う。

【0095】

その後、通常のMISトランジスタを有する半導体装置の製造方法と同様に、第2の層間絶縁膜31上に、レジスト(図示せず)を形成した後、レジストをマスクにして、ドライエッチング法により、絶縁膜27、第1の層間絶縁膜28及び第2の層間絶縁膜31中に、第1、第2の金属シリサイド膜26a、26bの上面に到達する第1、第2のコンタクトホール32a、32bを形成する。このとき、絶縁膜27が露出したところで一度エ

ッチングを止める２ステップのエッチング法を用いることにより、第１，第２の金属シリサイド膜２６ａ，２６ｂのオーバーエッチング量を減らすことができる。

【００９６】

その後、スパッタ法又はＣＶＤ法により、第１，第２のコンタクトホール３２ａ，３２ｂの底部及び側壁部に、チタンと窒化チタンとが順次堆積されてなるバリアメタル膜を形成する。その後、ＣＶＤ法により、第２の層間絶縁膜３１上に、第１，第２のコンタクトホール３２ａ，３２ｂ内を埋め込むように、タングステン膜を堆積した後、ＣＭＰ法により、第１，第２のコンタクトホール３２ａ，３２ｂ外に形成されているタングステン膜を除去する。このようにして、第１，第２のコンタクトホール３２ａ，３２ｂ内に、バリアメタル膜を介してタングステン膜が埋め込まれてなる第１，第２のコンタクトプラグ３３ａ，３３ｂを形成する。その後、第２の層間絶縁膜３１上に、第１，第２のコンタクトプラグ３３ａ，３３ｂと電氣的に接続する金属配線（図示せず）を形成する。

【００９７】

以上のようにして、本実施形態に係る半導体装置、すなわち、第２の金属膜３０ａからなる第１のゲート電極３０Ａを有するｎ型ＭＩＳトランジスタＮＴｒと、第１の金属膜１４ｂ及び第２の金属膜（導電膜）３０ｂからなる第２のゲート電極３０Ｂを有するｐ型ＭＩＳトランジスタＰＴｒとを備えた半導体装置を製造することができる。

【００９８】

以下に、本発明の第１の実施形態に係る半導体装置の構成について、図６（ａ）及び（ｂ）を参照しながら説明する。図６（ａ）及び（ｂ）は、本発明の第１の実施形態に係る半導体装置の構成について示す図であり、具体的には、図６（ａ）は平面図であり、図６（ｂ）は図６（ａ）に示すⅥｂ-Ⅵｂ線におけるゲート幅方向の断面図である。なお、図６（ａ）に示すⅥｌ-Ⅵｌ線は、図５（ｃ）中の左図における断面線に相当する一方、図６（ｂ）に示すⅥｒ-Ⅵｒ線は、図５（ｃ）中の右図における断面線に相当する。また、図中において、左側に示す「ｎＭＩＳ」とはｎ型ＭＩＳトランジスタが形成されるｎ型ＭＩＳ形成領域を示し、右側に示す「ｐＭＩＳ」とはｐ型ＭＩＳトランジスタが形成されるｐ型ＭＩＳ形成領域を示している。

【００９９】

図６（ａ）に示すように、ｎ型ＭＩＳ形成領域には、素子分離領域に囲まれた第１の活性領域１０ａが形成され、ｐ型ＭＩＳ形成領域には、素子分離領域に囲まれた第２の活性領域１０ｂが形成されている。第１の活性領域１０ａ上には、第１のゲート絶縁膜を介して、第１のゲート電極３０Ａが形成されていると共に、第２の活性領域１０ｂ上には、第２のゲート絶縁膜を介して、第２のゲート電極３０Ｂが形成されている。第１，第２のゲート電極３０Ａ，３０Ｂの側面上には、第１，第２のオフセットスペーサ１７ａ，１７ｂ及び第１，第２の内側サイドウォール１９ａ，１９ｂを順次介して、絶縁膜２７が形成されている。なお、図６（ａ）においては、第１の層間絶縁膜（図５（ｃ）：２８参照）、及び第２の層間絶縁膜（図５（ｃ）：３１参照）の図示を省略しているが、第１の層間絶縁膜は、絶縁膜２７上に形成されている。また、第２の層間絶縁膜は、第１，第２のゲート電極３０Ａ，３０Ｂを覆うように、第１の層間絶縁膜上に形成されている。

【０１００】

図６（ｂ）に示すように、半導体基板１０の上部には、ｎ型ＭＩＳ形成領域とｐ型ＭＩＳ形成領域とを区画するように、トレンチ内に絶縁膜が埋め込まれた素子分離領域１１が形成されている。半導体基板１０におけるｎ型ＭＩＳ形成領域には、ｐ型ウェル領域１２ａが形成されている一方、半導体基板１０におけるｐ型ＭＩＳ形成領域には、ｎ型ウェル領域１２ｂが形成されている。第１の活性領域１０ａ上には、第１のゲート絶縁膜１３ａを介して、第２の金属膜３０ａからなる第１のゲート電極３０Ａが形成されている一方、第２の活性領域１０ｂ上には、第２のゲート絶縁膜１３ｂを介して、第１の金属膜１４ｂと第１の金属膜１４ｂ上に形成された第２の金属膜（導電膜）３０ｂとからなる第２のゲート電極３０Ｂが形成されている。半導体基板１０上には、第１，第２のゲート電極３０Ａ，３０Ｂを覆うように第２の層間絶縁膜３１が形成されている。

【０１０１】

ここで、n型MISトランジスタ及びp型MISトランジスタの構成について、図5(c)を参照しながら詳細に説明する。

【0102】

n型MISトランジスタNTrは、図5(c)に示すように、半導体基板10における素子分離領域11に囲まれた第1の活性領域10aと、第1の活性領域10a上に形成された第1のゲート絶縁膜13aと、第1のゲート絶縁膜13a上に形成された第2の金属膜30aからなる第1のゲート電極30Aと、第1のゲート電極30Aの側面上に第1のオフセットスペーサ17aを介して形成され断面形状がL字状の第1の内側サイドウォール19aと、第1の活性領域10aにおける第1のゲート電極30Aの側方下に形成された浅いn型ソースドレイン領域18aと、第1の活性領域10aにおける第1の内側サイドウォール19aの外側方下に形成された深いn型ソースドレイン領域25aと、第1のゲート電極30Aの側面上から第1の活性領域10aにおける第1のゲート電極30Aの側方に位置する領域の上面上に跨って形成された絶縁膜27と、深いn型ソースドレイン領域25aの上部に形成された第1の金属シリサイド膜26aとを備えている。

【0103】

p型MISトランジスタPTrは、図5(c)に示すように、半導体基板10における素子分離領域11に囲まれた第2の活性領域10bと、第2の活性領域10b上に形成された第2のゲート絶縁膜13bと、第2のゲート絶縁膜13b上に形成され第1の金属膜14b及び第2の金属膜(導電膜)30bからなる第2のゲート電極30Bと、第2のゲート電極30Bの側面上に第2のオフセットスペーサ17bを介して形成され断面形状がL字状の第2の内側サイドウォール19bと、第2の活性領域10bにおける第1のゲート電極30Bの側方下に形成された浅いp型ソースドレイン領域18bと、第2の活性領域10bにおける第2の内側サイドウォール19bの外側方下に形成されシリコン混晶層24を含む深いp型ソースドレイン領域25bと、第2のゲート電極30Bの側面上から第2の活性領域10bにおける第2のゲート電極30Bの側方に位置する領域の上面上に跨って形成された絶縁膜27と、深いp型ソースドレイン領域25bの上部に形成された第2の金属シリサイド膜26bとを備えている。

【0104】

第1のゲート電極30Aを構成する第2の金属膜30aは、4.05eV以上で4.6eV以下の仕事関数を有する金属材料(又は金属化合物材料)からなる一方、第2のゲート電極30Bを構成する第1の金属膜14bは、4.6eV以上で5.15eV以下の仕事関数を有する金属材料(又は金属化合物材料)からなる。このように、第2の金属膜30aと第1の金属膜14bとは、互いに異なる仕事関数を有し、互いに異なる金属材料(又は金属化合物材料)からなる。

【0105】

また、第1のゲート電極30Aと第2のゲート電極30Bとは、その上面高さが互いに同じであり、第1のゲート電極30Aは、第2の金属膜30aからなる一方、第2のゲート電極30Bは、第1の金属膜14b及び第2の金属膜30bからなる。そのため、第2の金属膜30aの膜厚は、第1の金属膜14bの膜厚及び第2の金属膜(導電膜)30bの膜厚に比べて厚い。

【0106】

絶縁膜27は、第1、第2のゲート電極30A、30Bの側面上から第1、第2の活性領域10a、10bにおける第1、第2のゲート電極30A、30Bの側方に位置する領域の上面上に跨って形成されている一方、第1、第2のゲート電極30A、30Bの上面上には形成されていない。そして、絶縁膜27の膜厚は、第1、第2のゲート電極30A、30Bの膜厚に比べて薄い。

【0107】

第1のゲート絶縁膜13aと第2のゲート絶縁膜13bとは、互いに同一の工程において形成され、互いに同じ絶縁材料からなる。

【0108】

本実施形態によると、互いに同一の工程において、第1、第2のゲート電極形成部14A、14B（図1(c)参照）を形成した後、第1のゲート電極形成部14Aにおける第1のシリコン膜15a及び第1の金属膜14aを順次除去して形成された第1の凹部Ca（図4(c)参照）内に、第2の金属膜30aを形成して、第2の金属膜30aからなる第1のゲート電極30A（図5(b)参照）を形成する。一方、第2のゲート電極形成部14Bにおける第2のシリコン膜15bを除去して形成された第2の凹部Cb（図4(b)参照）内に、第2の金属膜30bを形成して、第1の金属膜14b及び第2の金属膜30bからなる第2のゲート電極30B（図5(b)参照）を形成する。そのため、第1のゲート電極形成部14Aにおける第1の金属膜14aの除去の際には、図4(c)に示すように、n型MIS形成領域及びp型MIS形成領域の一方を開口し他方を覆うレジストマスク29を形成するため、素子分離領域11に合わせマージンが必要とされるものの、第1、第2のゲート電極形成部14A、14Bの形成の際には、素子分離領域11に合わせマージンは必要とされない。従って、素子分離領域11に合わせマージンが必要とされる工程（以下、「合わせマージン必要工程」と称す）数を1回に抑えることができるので、合わせマージンのゲート幅方向の幅を狭くして、素子分離領域11のゲート幅方向の幅（図6(b)：Wnp参照）を縮小化することができるので、半導体装置の微細化を図ることができる。

【0109】

これに対し、第2の従来の半導体装置の製造方法では、図14(a)に示す工程において、レジストマスク206の形成の際に素子分離領域201に合わせマージンが必要とされると共に、図14(b)に示す工程において、レジストマスク210の形成の際に素子分離領域201に合わせマージンが必要とされるため、2回の合わせマージン必要工程があるので、既述の通り、素子分離領域201のゲート幅方向の幅を縮小化することができない。

【0110】

加えて、図1(c)に示すように、互いに同一の工程において、互いに同一のシリコン膜15、同一の第1の金属膜14、及び同一のゲート絶縁膜形成膜13が順次パターンニングされて、第1、第2のゲート電極形成部14A、14Bが形成されるため、第1、第2のゲート電極形成部14A、14Bを容易に且つ精度良く形成することができる。これにより、精度良く形成された第1のゲート電極形成部14Aにおける第1の金属膜14a及び第1のシリコン膜15aを、第2の金属膜30aと置換して、第2の金属膜30aからなる第1のゲート電極30Aを形成する一方、精度良く形成された第2のゲート電極形成部14Bにおける第2のシリコン膜15bを、第2の金属膜30bと置換して、第1の金属膜14b及び第2の金属膜30bからなる第2のゲート電極30Bを形成することができるため、精度良く形成された第1、第2のゲート電極30A、30Bを実現することができる。

【0111】

これに対し、第1の従来の半導体装置の製造方法では、図13に示すように、第1のパターニング部107Aと第2のパターニング部107Bとが、互いに構成が異なるにも拘わらず、互いに同一の工程において、パターンニングされるため、既述の通り、第1、第2のゲート電極の双方を精度良く形成することができない。一方、第2の従来の半導体装置の製造方法においても、図14(d)に示すように、第1のパターニング部と第2のパターニング部とが、互いに構成が異なるにも拘わらず、互いに同一の工程において、パターンニングされるため、既述の通り、第1、第2のゲート電極の双方を精度良く形成することができない。

【0112】

さらに、深いp型ソースドレイン領域25bが、第2の活性領域10bにおけるチャネル領域のゲート長方向に圧縮応力を生じさせるシリコン混晶層24を含むことにより、第2の活性領域10bにおけるチャネル領域のゲート長方向に圧縮応力を印加することができるので、p型MISトランジスタの駆動能力を向上させることができる。

【0113】

なお、第1の実施形態では、p型MISトランジスタの駆動能力を向上させることを目的に、第1、第2のサイドウォール20A、20Bの形成(図2(a)参照)後で、深いn型、p型ソースドレイン領域25a、25bの形成(図3(b)参照)前に、図2(b)～図3(a)に示す工程を順次行い、第2の活性領域10bにおける第2のサイドウォール20Bの外側下方に形成されたトレンチ23内に、例えばp型SiGe層からなるシリコン混晶層24を形成する場合を具体例に挙げて説明したが、本発明はこれに限定されるものではない。

【0114】

例えば、図2(a)に示すように、第1、第2のサイドウォール20A、20Bを形成した後、図2(b)～図3(a)に示す工程を順次行うことなく、すなわち、シリコン混晶層24を形成することなく、図3(b)に示すように、深いn型、p型ソースドレイン領域25a、25bを形成してもよい。

【0115】

また例えば、第1、第2のサイドウォール20A、20Bの形成(図2(a)参照)後で、深いn型、p型ソースドレイン領域25a、25bの形成(図3(b)参照)前に、第1の活性領域10aにおける第1のサイドウォール20Aの外側下方に形成されたトレンチ内に、第1の活性領域10aにおけるチャネル領域のゲート長方向に引っ張り応力を生じさせるシリコン混晶層(例えばn型SiC層)を形成してもよい。この場合、p型MISトランジスタではなく、n型MISトランジスタの駆動能力を向上させることができる。

【0116】

(第2の実施形態)

本発明の第2の実施形態に係る半導体装置及びその製造方法について図面を参照しながら説明する。なお、第2の実施形態に係る半導体装置及びその製造方法について、前述の第1の実施形態に係る半導体装置及びその製造方法と相違する点を中心に説明し、共通する点については適宜省略して説明する。

【0117】

以下に、本発明の第2の実施形態に係る半導体装置の製造方法について、図7(a)～(c)及び図8(a)～(c)を参照しながら説明する。図7(a)～図8(c)は、本発明の第2の実施形態に係る半導体装置の製造方法を工程順に示すゲート長方向の要部工程断面図である。なお、図7(a)～図8(c)において、前述の第1の実施形態における構成要素と同一の構成要素には、第1の実施形態における図1(a)～図5(c)に示す符号と同一の符号を付している。また、図中において、左側に示す「nMIS」とはn型MISトランジスタが形成されるn型MIS形成領域を示し、右側に示す「pMIS」とはp型MISトランジスタが形成されるp型MIS形成領域を示している。

【0118】

まず、第1の実施形態における図1(a)～図4(a)に示す工程を順次行い、図7(a)に示す構成(すなわち、図4(a)に示す構成と同一の構成)を得る。

【0119】

次に、図7(b)に示すように、半導体基板10上に、n型MIS形成領域を開口しp型MIS形成領域を覆うレジストマスク29を形成した後、第1の金属膜14a、第1のオフセットスペーサ17a、第1の内側サイドウォール19a、絶縁膜27、及び第1の層間絶縁膜28と選択比のあるドライエッチング法又はウェットエッチング法を用いて、第1のゲート電極形成部14Aにおける第1のシリコン膜15aを除去する。その後、第1のゲート絶縁膜13a、第1のオフセットスペーサ17a、第1の内側サイドウォール19a、絶縁膜27、及び第1の層間絶縁膜28と選択比のあるウェットエッチング法を用いて、第1のゲート電極形成部14Aにおける第1の金属膜14aを除去する。

【0120】

このようにして、第1のゲート電極形成部14Aにおける第1のシリコン膜15a及び第1の金属膜14aを順次除去して、第1の活性領域10a上に、第1のオフセットスペーサ17a及び第1の内側サイドウォール19aを順次介して絶縁膜27に囲まれ、第1

のゲート絶縁膜13aが底面に露出する第1の凹部Caを形成する。

【0121】

次に、図7(c)に示すように、レジストマスク29を除去した後、半導体基板10上に、例えばCVD法、ALD法、又はスパッタ法等により、第1の凹部Ca内を埋め込むように、例えばTa_nからなる第2の金属膜30を堆積する。

【0122】

次に、図8(a)に示すように、例えばCMP法、又はエッチバック法により、絶縁膜27の上面が露出するまで、第2の金属膜30を除去する。これにより、第1の凹部Ca内における第1のゲート絶縁膜13a上に第2の金属膜30aを形成する。

【0123】

このようにして、第1の活性領域10a上に、第1のゲート絶縁膜13aを介して、第2の金属膜30aからなる第1のゲート電極30Aを形成する一方、第2の活性領域10b上に、第2のゲート絶縁膜13bを介して、第1の金属膜14b及び第2のシリコン膜15bからなる第2のゲート電極30Bを形成する。

【0124】

次に、図8(b)に示すように、第2のシリコン膜15bの表面に形成されている自然酸化膜(図示せず)を除去した後、例えばスパッタ法により、半導体基板10上の全面に、例えば膜厚が10nmのニッケルからなる金属膜(図示せず)を堆積する。その後、例えば窒素雰囲気中、320℃の下、1回目のRTA処理により、第2のシリコン膜15bのSiと金属膜のNiとを反応させて、第2のシリコン膜15bの上部に、ニッケルシリサイドからなる金属シリサイド膜34を形成する。

【0125】

その後、硫酸と過酸化水素水との混合液からなるエッチング液中に半導体基板10を浸漬することにより、第1の層間絶縁膜28、絶縁膜27、第1、第2の内側サイドウォール19a、19b、及び第1、第2のオフセットスペーサ17a、17b等の上に残存する未反応の金属膜を除去した後、1回目のRTA処理での温度よりも高い温度(例えば550℃)の下、2回目のRTA処理により、金属シリサイド膜34のシリサイド組成比を安定化させる。

【0126】

次に、図8(c)に示すように、例えばCVD法により、第1の層間絶縁膜28上に、第1、第2のゲート電極30A、30Bを覆うように、第2の層間絶縁膜31を堆積した後、例えばCMP法により、第2の層間絶縁膜31の表面の平坦化を行う。その後、通常のMISトランジスタを有する半導体装置の製造方法と同様に、絶縁膜27、第1の層間絶縁膜28、及び第2の層間絶縁膜31中の第1、第2のコンタクトホール32a、32b内に形成され、第1、第2の金属シリサイド膜26a、26bと接続する第1、第2のコンタクトプラグ33a、33bを形成する。その後、第2の層間絶縁膜31上に、第1、第2のコンタクトプラグ33a、33bと電気的に接続する金属配線(図示せず)を形成する。

【0127】

以上のようにして、本実施形態に係る半導体装置、すなわち、第2の金属膜30aからなる第1のゲート電極30Aを有するn型MISトランジスタNT_rと、第1の金属膜14b及び第2のシリコン膜(導電膜)15bからなる第2のゲート電極30Bを有するp型MISトランジスタPT_rとを備えた半導体装置を製造することができる。

【0128】

ここで、本実施形態と第1の実施形態との製造方法上の相違点は、以下に示す点である。

【0129】

第1の実施形態では、図4(b)に示すように、第2のゲート電極形成部14Bにおける第2のシリコン膜15bを除去して形成された第2の凹部Cb内に、第2の金属膜30bを形成して、第2のゲート電極形成部14Bにおける第1の金属膜14b、及び第2の金

属膜30bからなる第2のゲート電極30Bを形成する。

【0130】

これに対し、本実施形態では、第1の実施形態における図4(b)に示すように第2のゲート電極形成部14Bにおける第2のシリコン膜15bを除去せずに、第2のゲート電極形成部14Bにおける第1の金属膜14b及び第2のシリコン膜15bからなる第2のゲート電極30Bを形成する。そして、第2のゲート電極30Bの形成後に、図8(b)に示すように、第2のゲート電極30Bにおける第2のシリコン膜15b上に金属シリサイド膜34を形成する。

【0131】

以下に、本発明の第2の実施形態に係る半導体装置の構成について、図9を参照しながら説明する。図9は、本発明の第2の実施形態に係る半導体装置の構成について示すゲート幅方向の断面図である。なお、図9において、第1の実施形態における構成要素と同一の構成要素には、第1の実施形態における図6(b)に示す符号と同一の符号を付している。また、図中において、左側に示す「nMIS」とはn型MISトランジスタが形成されるn型MIS形成領域を示し、右側に示す「pMIS」とはp型MISトランジスタが形成されるp型MIS形成領域を示している。

【0132】

図9に示すように、第1の活性領域10a上には、第1のゲート絶縁膜13aを介して、第2の金属膜30aからなる第1のゲート電極30Aが形成されている一方、第2の活性領域10b上には、第2のゲート絶縁膜13bを介して、第1の金属膜14bと第1の金属膜14b上に形成された第2のシリコン膜（導電膜）15bとからなる第2のゲート電極30Bが形成されている。第2のシリコン膜15b上には、金属シリサイド膜34が形成されている。

【0133】

ここで、本実施形態と第1の実施形態との構造上の相違点は、以下に示す点である。

【0134】

本実施形態では、第2のゲート電極30Bは、第1の金属膜14bと第2のシリコン膜15bとからなる。そして、第2のシリコン膜15b上には、金属シリサイド膜34が形成されている。これに対し、第1の実施形態では、第2のゲート電極30Bは、第1の金属膜14bと第2の金属膜30bとからなる。

【0135】

このように、第2のゲート電極30Bにおける第1の金属膜14b上に形成された導電膜が、本実施形態では第2のシリコン膜15bであるのに対し、第1の実施形態では第2の金属膜30bである。

【0136】

本実施形態によると、互いに同一の工程において、第1、第2のゲート電極形成部14A、14B（図1(c)参照）を形成した後、第1のゲート電極形成部14Aにおける第1のシリコン膜15a及び第1の金属膜14aを順次除去して形成された第1の凹部Ca（図7(b)参照）内に、第2の金属膜30aを形成して、第2の金属膜30aからなる第1のゲート電極30A（図8(a)参照）を形成する。一方、第2のゲート電極形成部14Bにおける第1の金属膜14b及び第2のシリコン膜15bからなる第2のゲート電極30Bを形成する。そのため、第1のゲート電極形成部14Aにおける第1のシリコン膜15a及び第1の金属膜14aの除去の際には、図7(b)に示すように、n型MIS形成領域及びp型MIS形成領域の一方を開ロし他方を覆うレジストマスク29を形成するため、素子分離領域11に合わせマージンが必要とされるものの、第1、第2のゲート電極形成部14A、14Bの形成の際には、素子分離領域11に合わせマージンは必要とされない。従って、合わせマージン必要工程数を1回に抑えることができるため、素子分離領域11のゲート幅方向の幅（図9：Wnp参照）を縮小化することができるので、半導体装置の微細化を図ることができる。

【0137】

加えて、図1(c)に示すように、互いに同一の工程において、互いに同一のシリコン膜15、同一の第1の金属膜14、及び同一のゲート絶縁膜形成膜13が順次パターンニングされて、第1、第2のゲート電極形成部14A、14Bが形成されるため、第1、第2のゲート電極形成部14A、14Bを容易に且つ精度良く形成することができる。これにより、精度良く形成された第1のゲート電極形成部14Aにおける第1の金属膜14a及び第1のシリコン膜15aを、第2の金属膜30aと置換して、第2の金属膜30aからなる第1のゲート電極30Aを形成する一方、精度良く形成された第2のゲート電極形成部14Bにおける第1の金属膜14b及び第2のシリコン膜15bからなる第2のゲート電極30Bを形成することができるため、精度良く形成された第1、第2のゲート電極30A、30Bを実現することができる。

【0138】

さらに、第1の実施形態と同様に、深いp型ソースドレイン領域25bがシリコン混晶層24を含むことにより、第2の活性領域10bにおけるチャネル領域のゲート長方向に圧縮応力を印加することができるので、p型MISトランジスタの駆動能力を向上させることができる。

【0139】

(第2の実施形態の変形例)

以下に、本発明の第2の実施形態の変形例に係る半導体装置及びその製造方法について図面を参照しながら説明する。なお、第2の実施形態の変形例に係る半導体装置及びその製造方法について、前述の第2の実施形態に係る半導体装置及びその製造方法と相違する点を中心に説明し、共通する点については適宜省略して説明する。

【0140】

以下に、本発明の第2の実施形態の変形例に係る半導体装置の製造方法について、図10(a)～(c)及び図11(a)～(c)を参照しながら説明する。図10(a)～図11(c)は、本発明の第2の実施形態の変形例に係る半導体装置の製造方法を工程順に示すゲート長方向の要部工程断面図である。なお、図10(a)～図11(c)において、前述の第2の実施形態における構成要素と同一の構成要素には、第2の実施形態における図7(a)～図8(c)に示す符号と同一の符号を付している。また、図中において、左側に示す「nMIS」とはn型MISトランジスタが形成されるn型MIS形成領域を示し、右側に示す「pMIS」とはp型MISトランジスタが形成されるp型MIS形成領域を示している。

【0141】

まず、第1の実施形態における図1(a)～図4(a)に示す工程を順次行い、第2の実施形態と同様に、図7(a)に示す構成を得る。但し、本変形例におけるゲート絶縁膜形成膜13としては、p型MISトランジスタ用に最適化された膜厚を有し、p型MISトランジスタ用に最適化された絶縁材料からなることが望ましい。

【0142】

次に、図10(a)に示すように、半導体基板10上に、n型MIS形成領域を開口しp型MIS形成領域を覆うレジストマスク29を形成した後、第1の金属膜14a、第1のオフセットスペーサ17a、第1の内側サイドウォール19a、絶縁膜27、及び第1の層間絶縁膜28と選択比のあるドライエッチング法又はウェットエッチング法を用いて、第1のゲート電極形成部14Aにおける第1のシリコン膜15aを除去する。その後、第1のゲート絶縁膜13a、第1のオフセットスペーサ17a、第1の内側サイドウォール19a、絶縁膜27、及び第1の層間絶縁膜28と選択比のあるウェットエッチング法を用いて、第1のゲート電極形成部14Aにおける第1の金属膜14aを除去する。このように、第2の実施形態における図7(b)に示す工程と同様の工程を行う。

【0143】

その後、半導体基板と選択比のあるウェットエッチング法を用いて、第1のゲート電極形成部14Aにおける第1のゲート絶縁膜13aを除去する。

【0144】

このようにして、第1のゲート電極形成部14Aにおける第1のシリコン膜15a、第

1の金属膜14a、及び第1のゲート絶縁膜13aを順次除去して、第1の活性領域10a上に、第1のオフセットスペーサ17a及び第1の内側サイドウォール19aを順次介して絶縁膜27に囲まれ、第1の活性領域10aが底面に露出する第1の凹部Caを形成する。

【0145】

次に、図10(b)に示すように、レジストマスク29を除去した後、例えばHPM (Hydrochloric Acid/Hydrogen Peroxide/Water Mixture) 処理により、半導体基板10の表面にケミカル酸化膜(図示せず)を形成した後、例えばMOCVD法により、半導体基板10上に、第1の凹部Ca内を覆うように、例えば膜厚が2nmの高誘電率膜からなるゲート絶縁膜形成膜35を堆積する。ここで、ゲート絶縁膜形成膜35としては、比誘電率が10以上の金属酸化物からなる高誘電率膜を含むことが望ましい。さらに、ゲート絶縁膜形成膜35としては、n型MISトランジスタ用に最適化された膜厚を有し、n型MISトランジスタ用に最適化された絶縁材料からなることが望ましい。

【0146】

その後、半導体基板10上に、例えばCVD法、ALD法、又はスパッタ法等により、ゲート絶縁膜形成膜35を介して第1の凹部Ca内を埋め込むように、例えばTaNからなる第2の金属膜30を堆積する。

【0147】

次に、図10(c)に示すように、例えばCMP法、又はエッチバック法により、絶縁膜27の上面が露出するまで、第2の金属膜30及びゲート絶縁膜形成膜35を除去する。これにより、第1の凹部Ca内に第3のゲート絶縁膜35aを形成すると共に、第3のゲート絶縁膜35a上に第2の金属膜30aを形成する。ここで、第3のゲート絶縁膜35aは、第1の凹部Ca内における第1の活性領域10a上から第2の金属膜30aの側面上に亘って形成される。そのため、図10(c)に示す図は、ゲート長方向の断面図であるため図示されないが、第3のゲート絶縁膜35aは、ゲート幅方向に沿って互いに隣り合う第2の金属膜30aと第1の金属膜14b及び第2のシリコン膜15bとの間に介在するように形成される。

【0148】

次に、図11(a)に示すように、第2の金属膜30aと選択比のあるエッチング法、又は例えば希釈フッ酸処理により、第3のゲート絶縁膜35aの上部を除去して、第3のゲート絶縁膜35aの上端高さを、第2の金属膜30aの上面高さよりも低くして、溝Rを形成する。ここで、溝Rは、第2の金属膜30aの周縁に沿って、第2の金属膜30aの側面を露出するように形成される。そのため、図11(a)に示す図は、ゲート長方向の断面図であるため図示されないが、溝Rは、ゲート幅方向に沿って互いに隣り合う第2の金属膜30aと第2のシリコン膜15bとの間に形成され、溝R内に、第2の金属膜30aのゲート幅方向の側面と、第2のシリコン膜15bのゲート幅方向の側面とが露出される。

【0149】

このように図10(b)～図11(a)に示す工程を順次経ることにより、第1の凹部Ca内に第3のゲート絶縁膜35aを形成すると共に、第3のゲート絶縁膜35a上に、溝R内に側面が露出する第2の金属膜30aを形成する。

【0150】

このようにして、第1の活性領域10a上に、第3のゲート絶縁膜35aを介して、第2の金属膜30aからなる第1のゲート電極30Aを形成する一方、第2の活性領域10b上に、第2のゲート絶縁膜13bを介して、第1の金属膜14b及び第2のシリコン膜15bからなる第2のゲート電極30Bを形成する。

【0151】

次に、図11(b)に示すように、第2のシリコン膜15bの表面に形成されている自然酸化膜(図示せず)を除去した後、例えばスパッタ法により、半導体基板10上の全面に、例えば膜厚が10nmのニッケルからなる金属膜(図示せず)を堆積する。その後、例

例えば窒素雰囲気中、320℃の下、1回目のRTA処理により、第2のシリコン膜15bのSiと金属膜のNiとを反応させて、第2のシリコン膜15bの上部に、ニッケルシリサイドからなる金属シリサイド膜34を形成する。このとき、本変形例における金属シリサイド膜34は、その体積膨張により、第2の金属膜30aと第2のシリコン膜15bとの間に形成された溝R内にも形成される。すなわち、溝R内に露出する第2の金属膜30aのゲート幅方向の側面及び第2のシリコン膜15bのゲート幅方向の側面の上に接して形成される（後述の図12：34参照）。そのため、金属シリサイド膜34により、第2の金属膜30aと第2のシリコン膜15bとを電氣的に接続することができる。

【0152】

その後、硫酸と過酸化水素水との混合液からなるエッチング液中に半導体基板10を浸漬することにより、第1の層間絶縁膜28、絶縁膜27、第1、第2の内側サイドウォール19a、19b、及び第1、第2のオフセットスペーサ17a、17b等の上に残存する未反応の金属膜を除去した後、1回目のRTA処理での温度よりも高い温度（例えば550℃）の下、2回目のRTA処理により、金属シリサイド膜34のシリサイド組成比を安定化させる。

【0153】

次に、図11(c)に示すように、例えばCVD法により、第1の層間絶縁膜28上に、第1、第2のゲート電極30A、30Bを覆うように、第2の層間絶縁膜31を堆積した後、例えばCMP法により、第2の層間絶縁膜31の表面の平坦化を行う。その後、通常のMISトランジスタを有する半導体装置の製造方法と同様に、絶縁膜27、第1の層間絶縁膜28、及び第2の層間絶縁膜31中の第1、第2のコンタクトホール32a、32b内に形成され、第1、第2の金属シリサイド膜26a、26bと接続する第1、第2のコンタクトプラグ33a、33bを形成する。その後、第2の層間絶縁膜31上に、第1、第2のコンタクトプラグ33a、33bと電氣的に接続する金属配線（図示せず）を形成する。このように、第2の実施形態における図8(c)に示す工程と同様の工程を行う。

【0154】

以上のようにして、本実施形態に係る半導体装置、すなわち、第2の金属膜30aからなる第1のゲート電極30Aを有するn型MISトランジスタNT_rと、第1の金属膜14b及び第2のシリコン膜（導電膜）15bからなる第2のゲート電極30Bを有するp型MISトランジスタPT_rとを備えた半導体装置を製造することができる。

【0155】

ここで、本変形例と第2の実施形態との製造方法上の相違点は、以下に示す点である。

【0156】

第2の実施形態では、第1のゲート電極形成部14Aにおける第1のシリコン膜15a及び第1の金属膜14aを除去して形成された第1の凹部Ca（図7(b)参照）内における第1のゲート絶縁膜13a上に、第2の金属膜30aを形成する。

【0157】

これに対し、本変形例では、第1のゲート電極形成部14Aにおける第1のシリコン膜15a及び第1の金属膜14aに加えて第1のゲート絶縁膜13aを除去して形成された第1の凹部Ca（図10(a)参照）内に第3のゲート絶縁膜35aを形成すると共に、第3のゲート絶縁膜35a上に第2の金属膜30aを形成する。

【0158】

そして、本変形例では、第1のゲート電極形成部14Aにおける第1のゲート絶縁膜13aを、第3のゲート絶縁膜35aと置換したことに伴い、ゲート幅方向に沿って互いに隣り合う第1のゲート電極30Aと第2のゲート電極30Bとの間に、第3のゲート絶縁膜35aが介在する。そのため、本変形例では、金属シリサイド膜34（図11(b)参照）の形成の際に、第1のゲート電極30Aと第2のゲート電極30Bとの電氣的接続を図ることを目的に、図11(a)に示すように、第3のゲート絶縁膜35aの上部を除去し溝Rを形成して、溝R内に、第2の金属膜30aのゲート幅方向の側面及び第2のシリコン膜15bのゲート幅方向の側面を露出させる。これにより、図11(b)に示す図は、ゲー

ト長方向の断面図であるため図示されないが、金属シリサイド膜34を、後述の図12に示すように、溝R内に露出する第2の金属膜30aのゲート幅方向の側面及び第2のシリコン膜15bのゲート幅方向の側面の上に接して形成することができるので、第2の金属膜30aと第2のシリコン膜15bとを電氣的に接続させて、第1のゲート電極30Aと第2のゲート電極30Bとの電氣的接続を図ることができる。

【0159】

以下に、本発明の第2の実施形態の変形例に係る半導体装置の構成について、図12を参照しながら説明する。図12は、本発明の第2の実施形態の変形例に係る半導体装置の構成について示すゲート幅方向の断面図である。なお、図12において、第2の実施形態における構成要素と同一の構成要素には、第2の実施形態における図9に示す符号と同一の符号を付している。また、図中において、左側に示す「nMIS」とはn型MISトランジスタが形成されるn型MIS形成領域を示し、右側に示す「pMIS」とはp型MISトランジスタが形成されるp型MIS形成領域を示している。

【0160】

図12に示すように、第1の活性領域10a上には、第3のゲート絶縁膜35aを介して、第2の金属膜30aからなる第1のゲート電極30Aが形成されている一方、第2の活性領域10b上には、第2のゲート絶縁膜13bを介して、第1の金属膜14bと第1の金属膜14b上に形成された第2のシリコン膜（導電膜）15bとからなる第2のゲート電極30Bが形成されている。第2のシリコン膜15b上には、金属シリサイド膜34が形成されている。

【0161】

ここで、本変形例と第2の実施形態との構造上の相違点は、以下に示す点である。

【0162】

本変形例では、第3のゲート絶縁膜35aは、第2のゲート絶縁膜13bと異なる絶縁材料からなる。そして、第3のゲート絶縁膜35aは、図12に示すように、第1の活性領域10a上から第2の金属膜30aのゲート幅方向の側面上に亘って形成され、第1のゲート電極30Aの下部領域と第2のゲート電極30Bの下部領域との間に介在している（なお、第3のゲート絶縁膜35aは、図11(c)に示すように、第2の金属膜30aのゲート幅方向の側面上だけでなくゲート長方向の側面上にも形成されている）。また、金属シリサイド膜34は、溝R内に露出する第2の金属膜30aのゲート幅方向の側面及び第2のシリコン膜15bのゲート幅方向の側面の上に接して形成されている。そして、金属シリサイド膜34により、第1のゲート電極30Aと第2のゲート電極30Bとが電氣的に接続している。

【0163】

これに対し、第2の実施形態では、第1のゲート絶縁膜13aは、第2のゲート絶縁膜13bと同じ絶縁材料からなる。そして、第1のゲート絶縁膜13aは、第1のゲート電極30Aと第2のゲート電極30Bとの間に介在していない。

【0164】

このように、n型MIS形成領域のゲート絶縁膜とp型MIS形成領域のゲート絶縁膜とが、本変形例では互いに異なる絶縁材料からなるのに対し、第2の実施形態では互いに同じ絶縁材料からなる。

【0165】

本変形例によると、第2の実施形態と同様の効果を得ることができる。

【0166】

加えて、第3のゲート絶縁膜35aは、n型MISトランジスタ用に最適化された膜厚を有し、n型MISトランジスタ用に最適化された絶縁材料（以下、「nMIS用絶縁材料」と称す）からなると共に、第2のゲート絶縁膜13bは、p型MISトランジスタ用に最適化された膜厚を有し、p型MISトランジスタ用に最適化された絶縁材料（以下、「pMIS用絶縁材料」と称す）からなるため、トランジスタ設計の自由度が増し、所望のトランジスタ特性を実現することができる。

【0167】

なお、第1、第2の実施形態では、第1の金属膜14としてpMIS用金属材料からなるpMIS用金属膜を用いると共に第2の金属膜30としてnMIS用金属材料からなるnMIS用金属膜を用いて、第1のゲート電極形成部14Aにおける第1の金属膜(pMIS用金属膜)14a及び第1のシリコン膜15aを、第2の金属膜(nMIS用金属膜)30aと置換して、第2の金属膜30aからなる第1のゲート電極30Aを形成する一方、第2のゲート電極形成部14Bにおける第1の金属膜(pMIS用金属膜)14bを含む第2のゲート電極30Bを形成する場合を具体例に挙げて説明したが、本発明はこれに限定されるものではない。

【0168】

その反対に、第1の金属膜14としてnMIS用金属膜を用いると共に第2の金属膜30としてpMIS用金属膜を用いてもよい。但し、この場合、第2のゲート電極形成部における第1の金属膜(nMIS用金属膜)及び第2のシリコン膜を、第2の金属膜(pMIS用金属膜)と置換して、第2の金属膜からなる第2のゲート電極を形成する一方、第1のゲート電極形成部における第1の金属膜(nMIS用金属膜)を含む第1のゲート電極を形成する。

【0169】

また、第2の実施形態の変形例においても、第1の金属膜14としてnMIS用金属膜を用いると共に第2の金属膜30としてpMIS用金属膜を用いてもよい。但し、この場合、ゲート絶縁膜形成膜13としてnMIS用絶縁材料からなるnMIS用絶縁膜を用いると共に、ゲート絶縁膜形成膜35としてpMIS用絶縁材料からなるpMIS用絶縁膜を用いる。

【0170】

なお、第1、第2の実施形態及びその変形例では、図3(c)に示すように、第1、第2の外側サイドウォール20a、20bの除去後、図3(d)に示すように、絶縁膜27として、例えばプラズマCVD法により、シリコン窒化膜からなる下地絶縁膜を形成する場合を具体例に挙げて説明したが、本発明はこれに限定されるものではない。例えば、第1、第2の外側サイドウォール20a、20bの除去後、絶縁膜27として、第1の活性領域10aにおけるチャネル領域のゲート長方向に引っ張り応力を生じさせる応力絶縁膜を形成してもよい。ここで、応力絶縁膜の形成方法の具体例としては、例えばプラズマCVD法により、水素を多量に含むシリコン窒化膜を堆積した後、紫外線照射により、シリコン窒化膜に含まれる水素を飛ばして、シリコン窒化膜からなる応力絶縁膜を形成する方法が挙げられる。

【0171】

このようにすると、応力絶縁膜により、第1の活性領域10aにおけるチャネル領域のゲート長方向に引っ張り応力を印加して、n型MISトランジスタの駆動能力を向上させることができる。そのため、第1、第2の実施形態及びその変形例のようにシリコン混晶層24によりp型MISトランジスタの駆動能力を向上させるのに加えて、応力絶縁膜によりn型MISトランジスタの駆動能力を向上させることができる。

【0172】

加えて、第1、第2の外側サイドウォール20a、20bの除去後に応力絶縁膜が形成されるため、第1、第2の外側サイドウォール20a、20bの除去分だけ、応力絶縁膜を厚く形成することができるため、第1の活性領域10aにおけるチャネル領域のゲート長方向に引っ張り応力を効果的に印加することができる。

【0173】

さらに、第1、第2の外側サイドウォール20a、20bの除去分だけ、応力絶縁膜を、第1の活性領域10aにおけるチャネル領域に近付けて形成することができるので、第1の活性領域10aにおけるチャネル領域のゲート長方向に引っ張り応力をより一層効果的に印加することができる。

【0174】

このように、絶縁膜27として、下地絶縁膜ではなく応力絶縁膜を用いた場合、応力絶縁膜の形成前に、第1、第2の外側サイドウォール20a、20bを予め除去することにより、応力絶縁膜による引っ張り応力を、第1の活性領域10aにおけるチャンネル領域のゲート長方向に効果的に印加することができる。

【0175】

一方、絶縁膜27として、第1、第2の実施形態及びその変形例のように下地絶縁膜を用いた場合、絶縁膜27の形成前に、図3(c)に示すように、第1、第2の外側サイドウォール20a、20bを除去する必要は必ずしもない。

【0176】

なお、第1、第2の実施形態及びその変形例では、シリコン混晶層24により、p型MISトランジスタの駆動能力を向上させる場合を具体例に挙げて説明したが、本発明はこれに限定されるものではなく、n型MISトランジスタの駆動能力及びp型MISトランジスタの駆動能力の双方を向上させてもよい。第1に例えば、第1、第2の実施形態及びその変形例のようにシリコン混晶層24を設ける一方、第1の活性領域10aにおける第1のサイドウォール20Aの外側下方に形成されたトレンチ内に、第1の活性領域10aにおけるチャンネル領域のゲート長方向に引っ張り応力を生じさせるシリコン混晶層を設けてもよい。第2に例えば、第1の活性領域10aにおける第1のサイドウォール20Aの外側下方に形成されたトレンチ内に、第1の活性領域10aにおけるチャンネル領域のゲート長方向に引っ張り応力を生じさせるシリコン混晶層を設ける一方、絶縁膜27として、第2の活性領域10bにおけるチャンネル領域のゲート長方向に圧縮応力を生じさせる応力絶縁膜を設けてもよい。

【0177】

なお、第1、第2の実施形態におけるゲート絶縁膜形成膜13、又は、第2の実施形態の変形例におけるゲート絶縁膜形成膜13及びゲート絶縁膜形成膜35の具体例としては、例えば酸化ハフニウム(HfO_2)、ハフニウムシリケート(HfSiO)、及び窒化ハフニウムシリケート(HfSiON)等のハフニウム系酸化物、並びにタンタル(Ta)、ジルコニウム(Zr)、チタン(Ti)、アルミニウム(Al)、スカンジウム(Sc)、イットリウム(Y)、又はランタン(La)等を含む酸化物が挙げられる。第1、第2の実施形態におけるゲート絶縁膜形成膜13として、これらの絶縁材料の中からn型MISトランジスタ及びp型MISトランジスタの双方に適した絶縁材料を使用する。また、第2の実施形態の変形例におけるゲート絶縁膜形成膜13及びゲート絶縁膜形成膜35として、p型MISトランジスタに最適化した絶縁材料及びn型MISトランジスタに最適化した絶縁材料をそれぞれ使用する。このとき、n型MISトランジスタ用のゲート絶縁膜形成膜35とp型MISトランジスタ用のゲート絶縁膜形成膜13とで、異なる絶縁材料を使用しても良いし、同じ絶縁材料でもそれぞれの膜厚又は組成(濃度)を変えて最適化して使用しても良い。

【0178】

また、第1、第2の実施形態及びその変形例では、シリコン膜15として、ポリシリコン膜を用いたが、これに代えて、例えばアモルファスシリコン膜又はシリコン膜等を含む他の半導体材料からなるシリコン膜を用いてもよい。

【0179】

また、第1、第2の実施形態及びその変形例では、第1、第2の金属シリサイド膜26a、26bの形成の際に、深いn型、p型ソースドレイン領域25a、25bの上部と反応させる金属膜として、ニッケルからなる金属膜を用いたが、これに代えて、例えば白金、コバルト、チタン、及びタンゲステン等のシリサイド化用金属からなる金属膜を用いてもよい。

【産業上の利用可能性】

【0180】

本発明は、精度良く形成されたn型、p型MISトランジスタのゲート電極を実現すると共に、ゲート幅方向の幅が縮小化された素子分離領域を実現することができるので、デ

ユアルメタルゲート構造の半導体装置及びその製造方法に有用である。

【図面の簡単な説明】

【0181】

【図1】(a)～(d)は、本発明の第1の実施形態に係る半導体装置の製造方法を工程順に示すゲート長方向の要部工程断面図である。

【図2】(a)～(d)は、本発明の第1の実施形態に係る半導体装置の製造方法を工程順に示すゲート長方向の要部工程断面図である。

【図3】(a)～(d)は、本発明の第1の実施形態に係る半導体装置の製造方法を工程順に示すゲート長方向の要部工程断面図である。

【図4】(a)～(c)は、本発明の第1の実施形態に係る半導体装置の製造方法を工程順に示すゲート長方向の要部工程断面図である。

【図5】(a)～(c)は、本発明の第1の実施形態に係る半導体装置の製造方法を工程順に示すゲート長方向の要部工程断面図である。

【図6】(a)及び(b)は、本発明の第1の実施形態に係る半導体装置の構成について示す図である。

【図7】(a)～(c)は、本発明の第2の実施形態に係る半導体装置の製造方法を工程順に示すゲート長方向の要部工程断面図である。

【図8】(a)～(c)は、本発明の第2の実施形態に係る半導体装置の製造方法を工程順に示すゲート長方向の要部工程断面図である。

【図9】本発明の第2の実施形態に係る半導体装置の構成について示すゲート幅方向の断面図である。

【図10】(a)～(c)は、本発明の第2の実施形態の変形例に係る半導体装置の製造方法を工程順に示すゲート長方向の要部工程断面図である。

【図11】(a)～(c)は、本発明の第2の実施形態の変形例に係る半導体装置の製造方法を工程順に示すゲート長方向の要部工程断面図である。

【図12】本発明の第2の実施形態の変形例に係る半導体装置の構成について示すゲート幅方向の断面図である。

【図13】第1の従来の半導体装置の製造方法を示すゲート幅方向の要部工程断面図である。

【図14】(a)～(e)は、第2の従来の半導体装置の製造方法を工程順に示すゲート幅方向の要部工程断面図である。

【図15】第2の従来の半導体装置の製造方法における問題点について示す平面図である。

【図16】第2の従来の半導体装置の製造方法における問題点について示すゲート幅方向の断面図である。

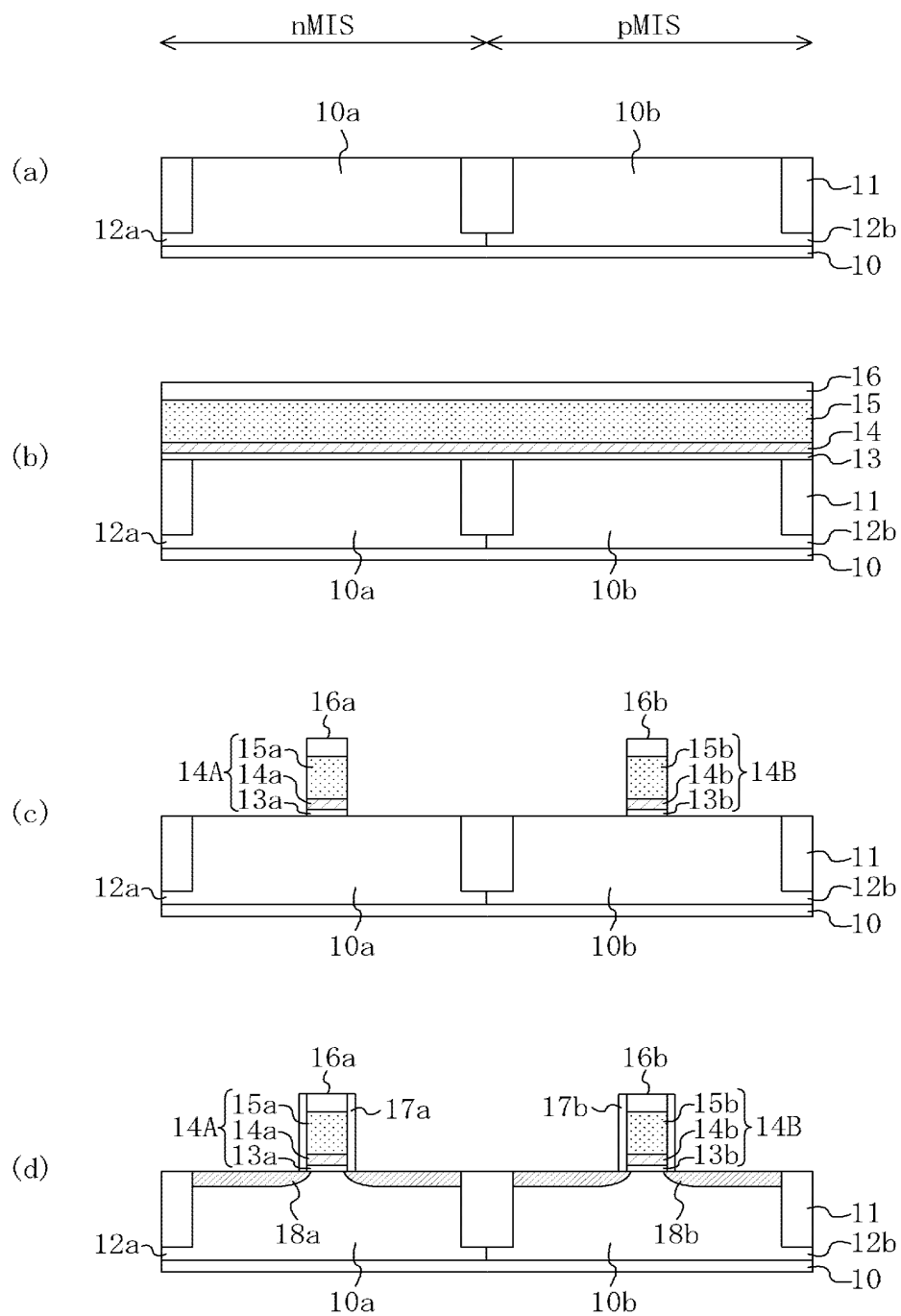
【符号の説明】

【0182】

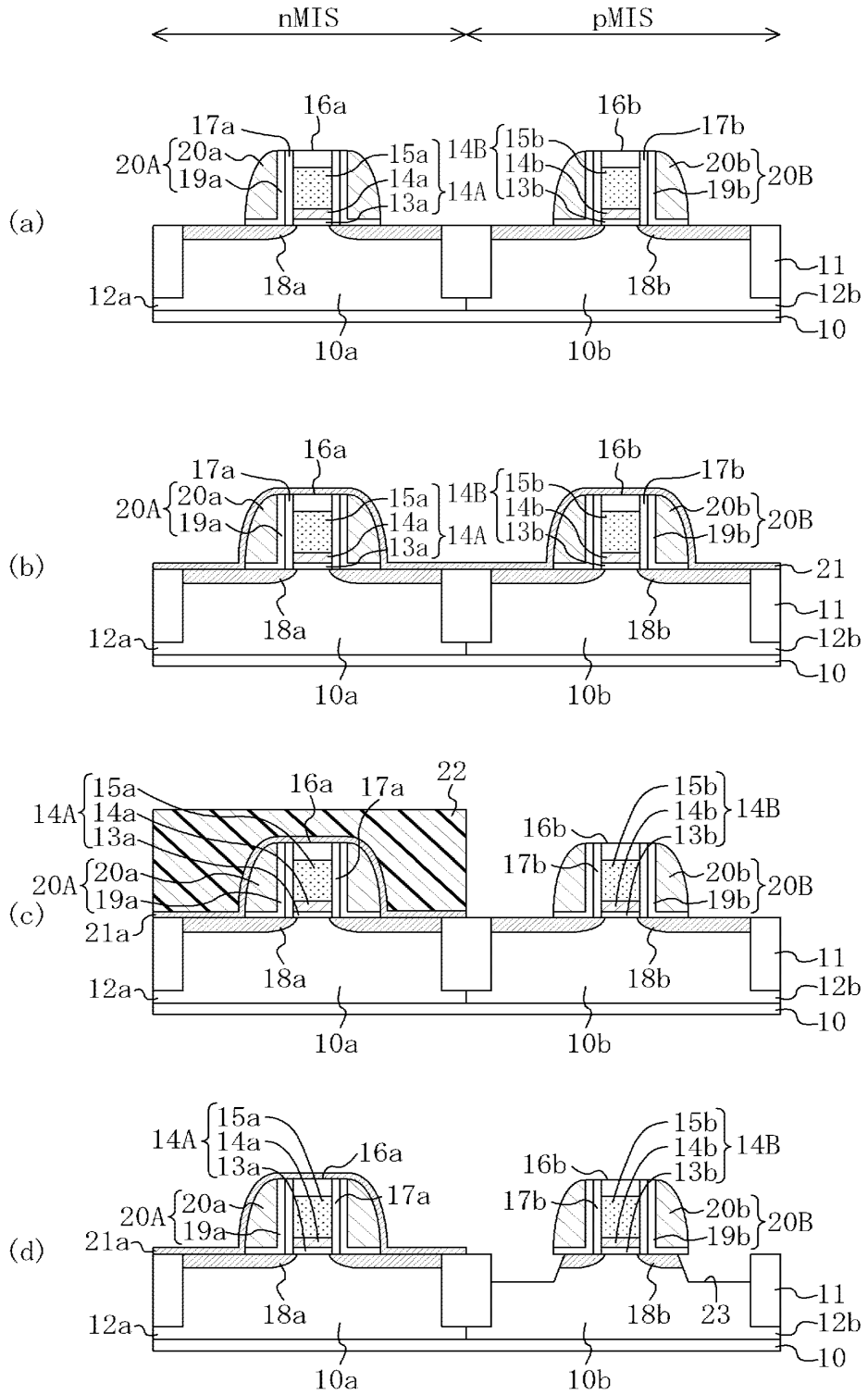
- 10 半導体基板
- 10a 第1の活性領域
- 10b 第2の活性領域
- 11 素子分離領域
- 12a p型ウェル領域
- 12b n型ウェル領域
- 13 ゲート絶縁膜形成膜
- 13a 第1のゲート絶縁膜
- 13b 第2のゲート絶縁膜
- 14, 14a, 14b 第1の金属膜
- 15 シリコン膜
- 15a 第1のシリコン膜
- 15b 第2のシリコン膜

1 6 保護膜
 1 6 a 第 1 の保護膜
 1 6 b 第 2 の保護膜
 1 7 a 第 1 のオフセットスペーサ
 1 7 b 第 2 のオフセットスペーサ
 1 8 a 浅い n 型ソースドレイン領域
 1 8 b 浅い p 型ソースドレイン領域
 1 9 a 第 1 の内側サイドウォール
 1 9 b 第 2 の内側サイドウォール
 2 0 a 第 1 の外側サイドウォール
 2 0 b 第 2 の外側サイドウォール
 2 0 A 第 1 のサイドウォール
 2 0 B 第 2 のサイドウォール
 2 1, 2 1 a 表面保護膜
 2 2 レジストマスク
 2 3 トレンチ
 2 4 シリコン混晶層
 2 5 a 深い n 型ソースドレイン領域
 2 5 b 深い p 型ソースドレイン領域
 2 6 a 第 1 の金属シリサイド膜
 2 6 b 第 2 の金属シリサイド膜
 2 7 絶縁膜
 2 8 第 1 の層間絶縁膜
 2 9 レジストマスク
 3 0, 3 0 a, 3 0 b 第 2 の金属膜
 3 0 A 第 1 のゲート電極
 3 0 B 第 2 のゲート電極
 3 1 第 2 の層間絶縁膜
 3 2 a 第 1 のコンタクトホール
 3 2 b 第 2 のコンタクトホール
 3 3 a 第 1 のコンタクトプラグ
 3 3 b 第 2 のコンタクトプラグ
 3 4 金属シリサイド膜
 3 5 ゲート絶縁膜形成膜
 3 5 a 第 3 のゲート絶縁膜
 W n p 素子分離領域のゲート幅方向の幅

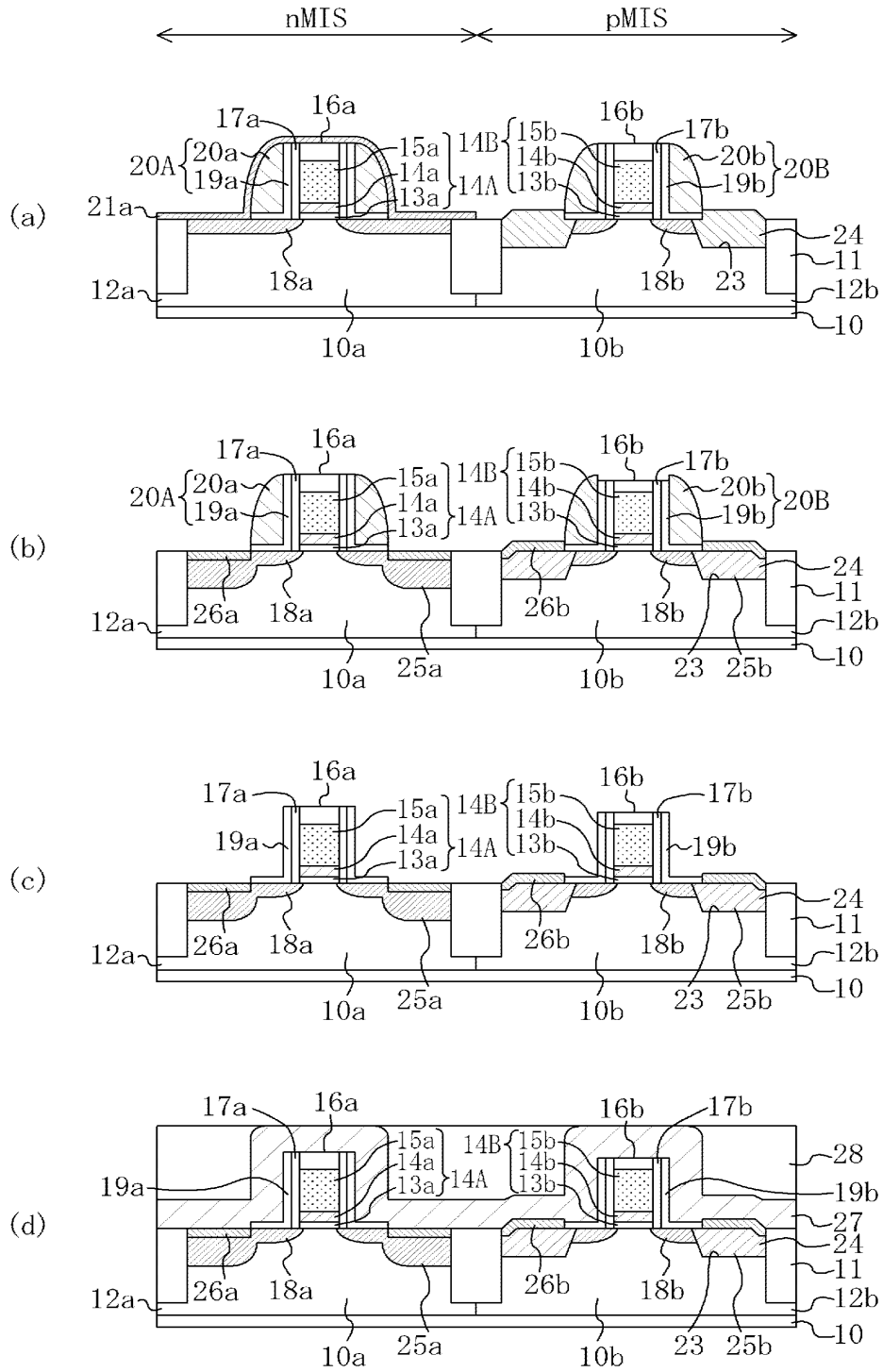
【書類名】 図面
【図 1】



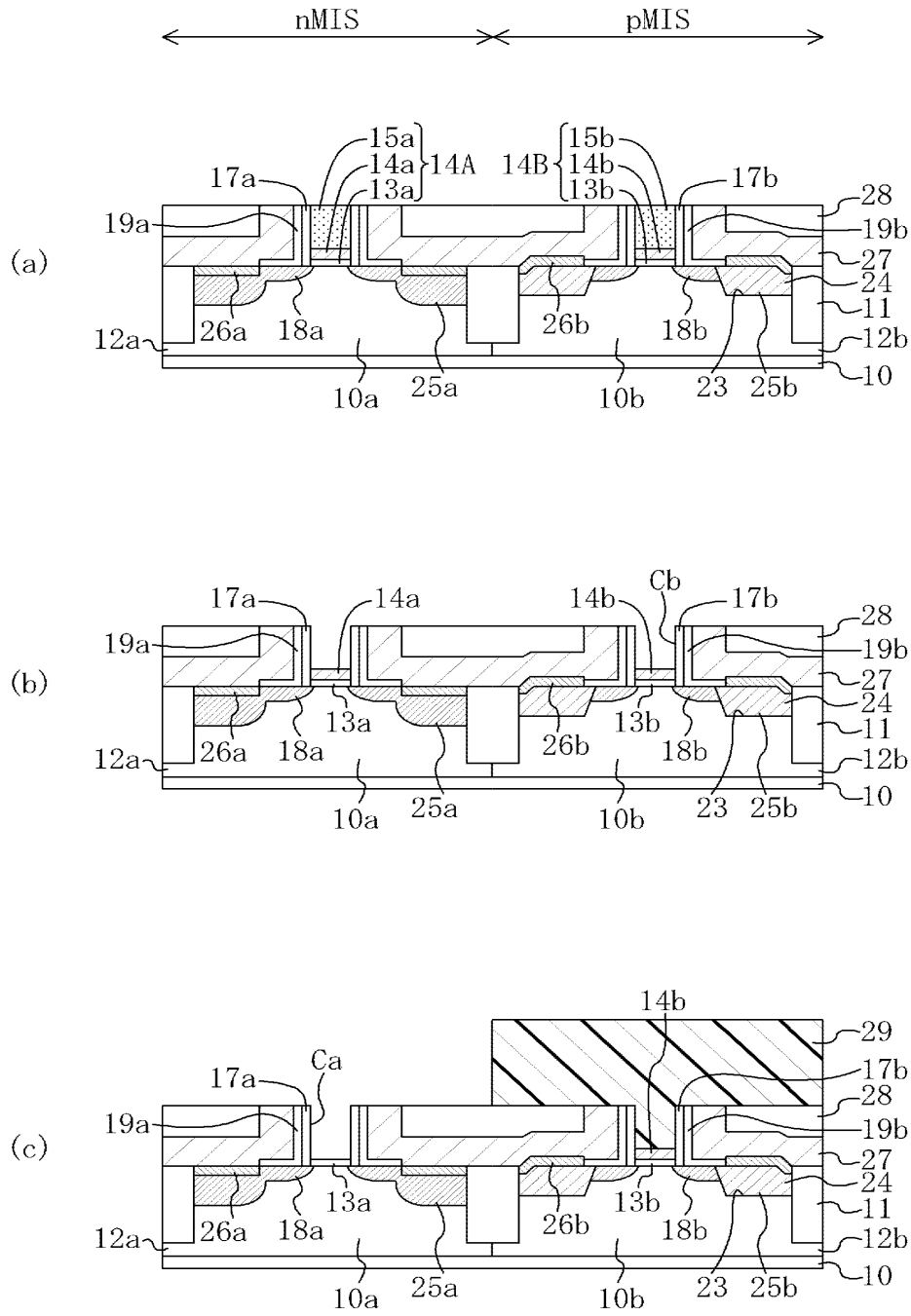
【例 2】



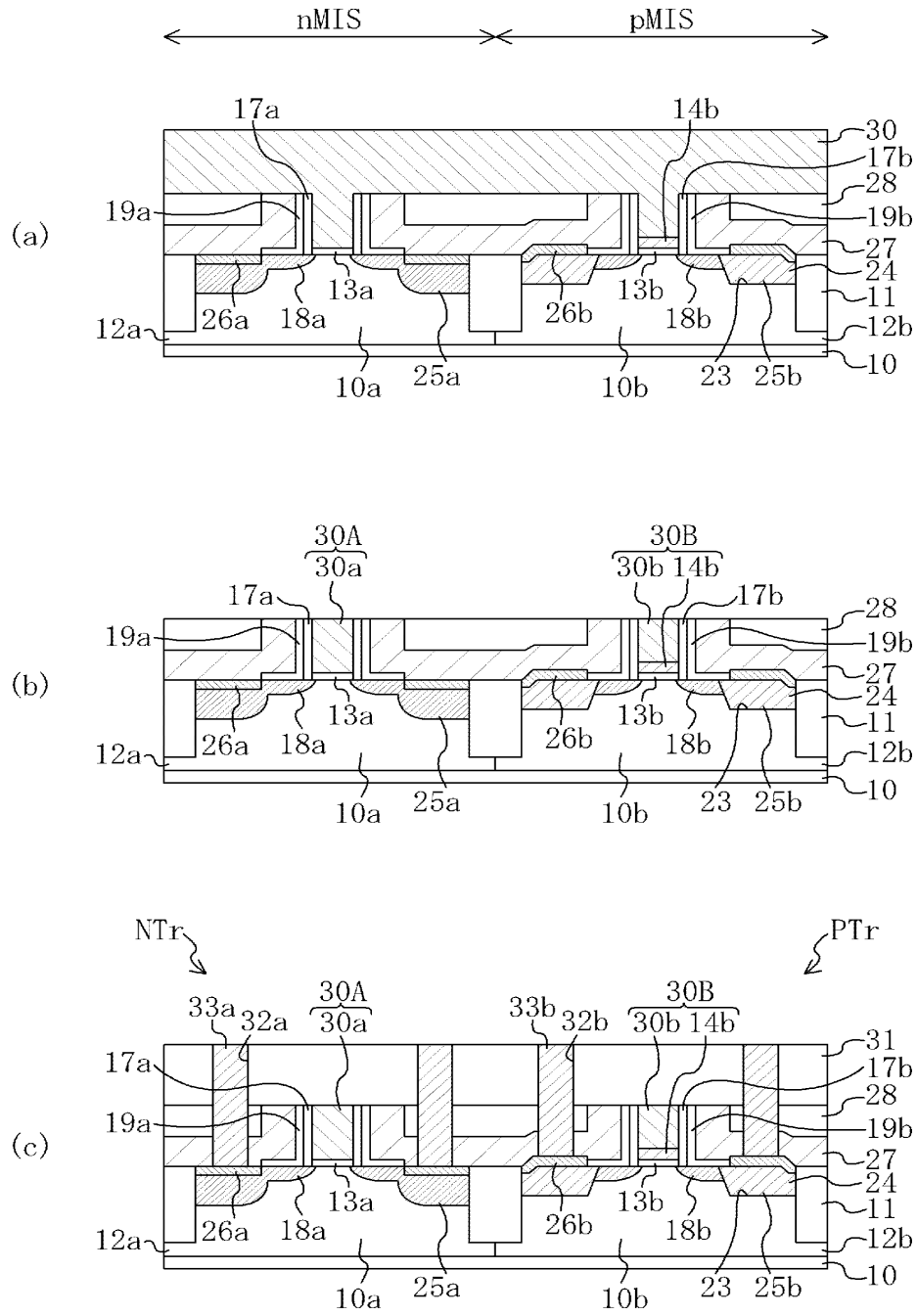
【例 3】



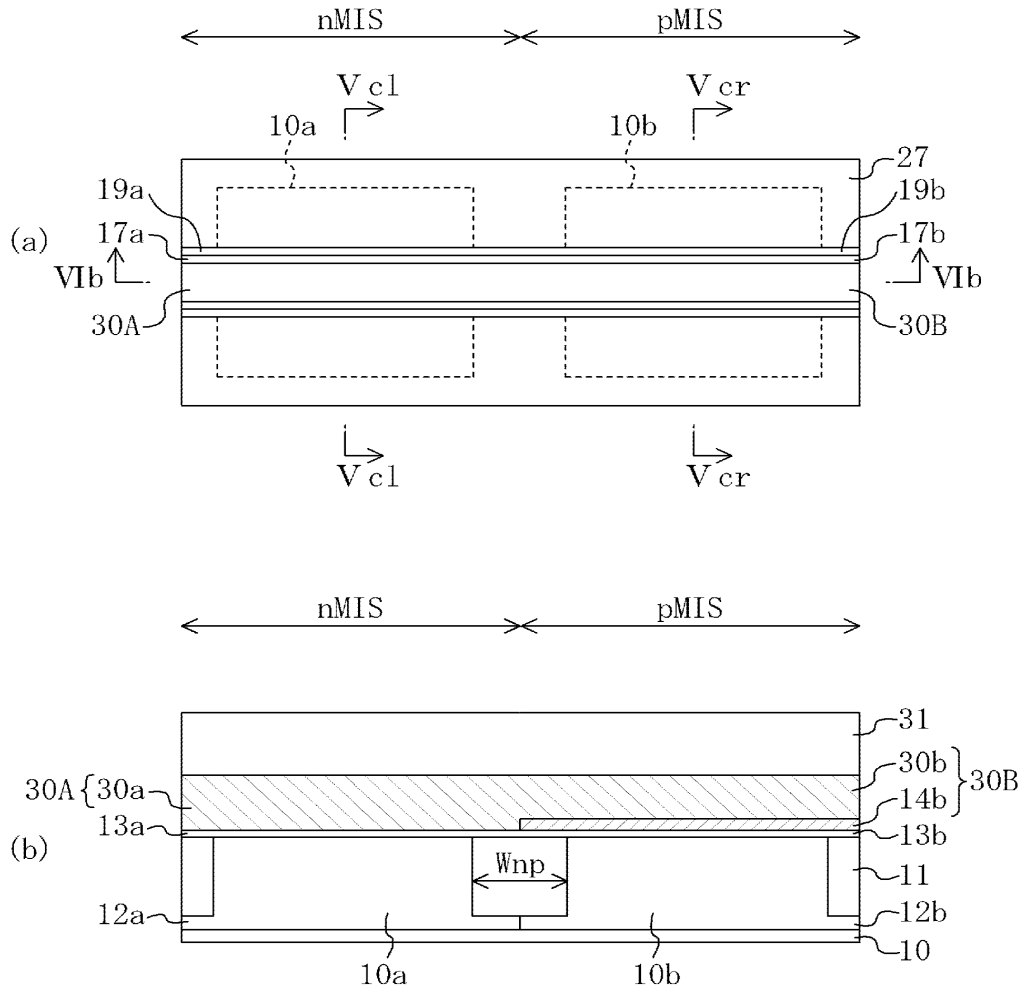
【例 4】



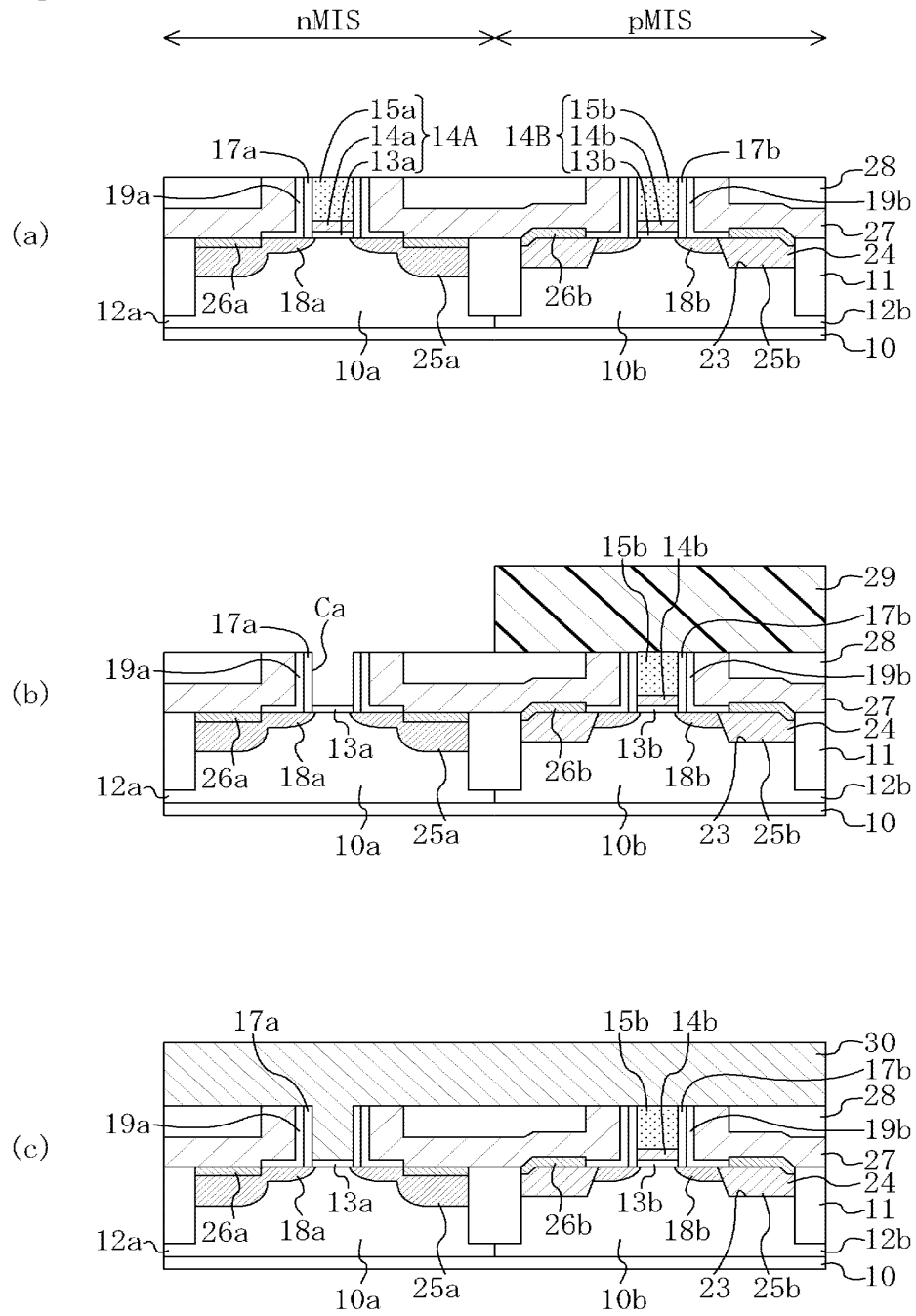
【図 5】



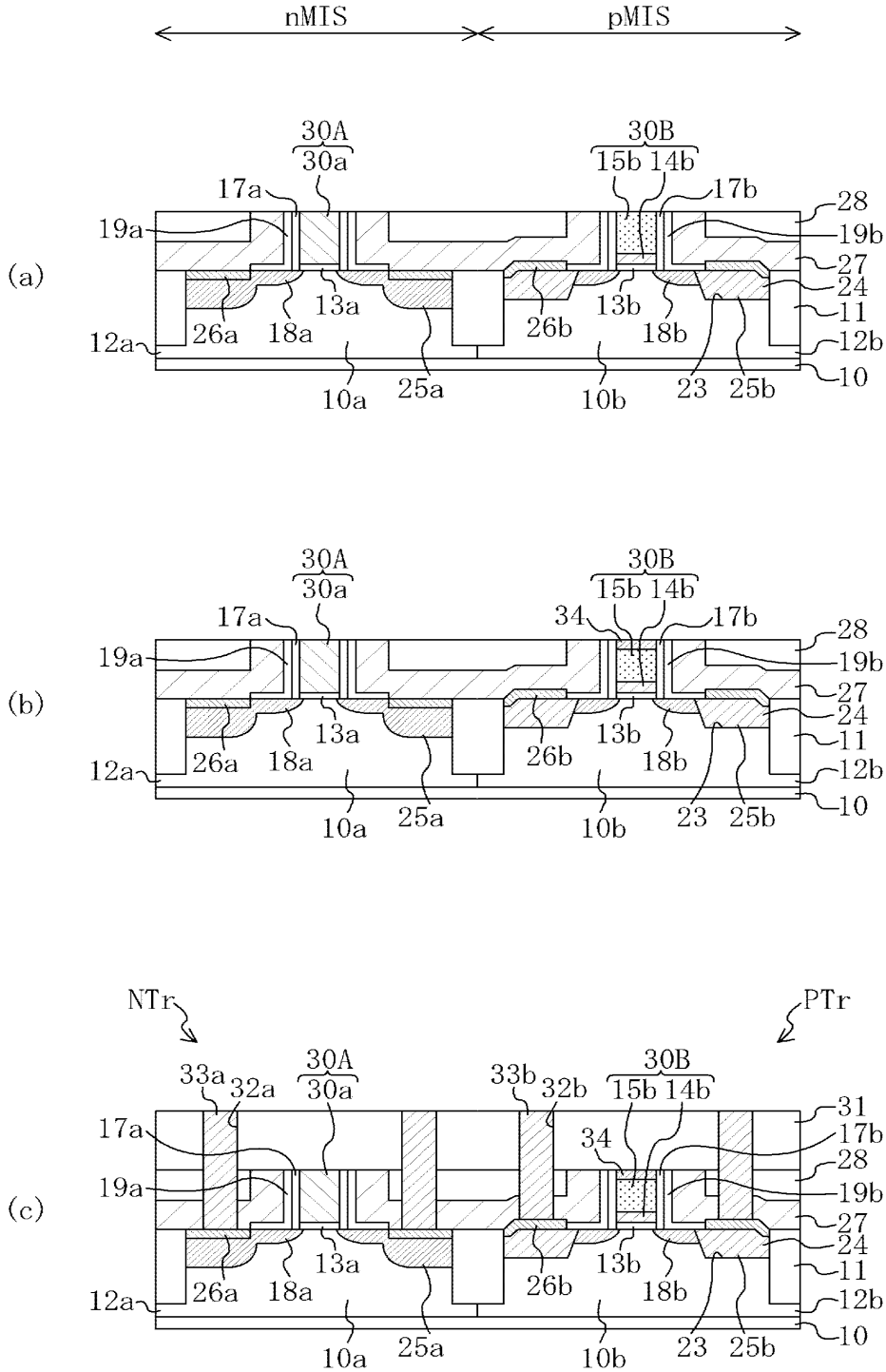
【図 6】



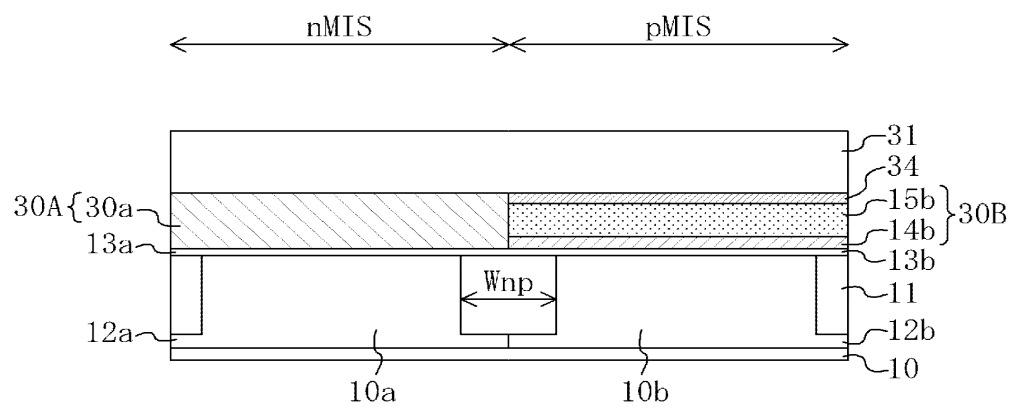
【図 7】



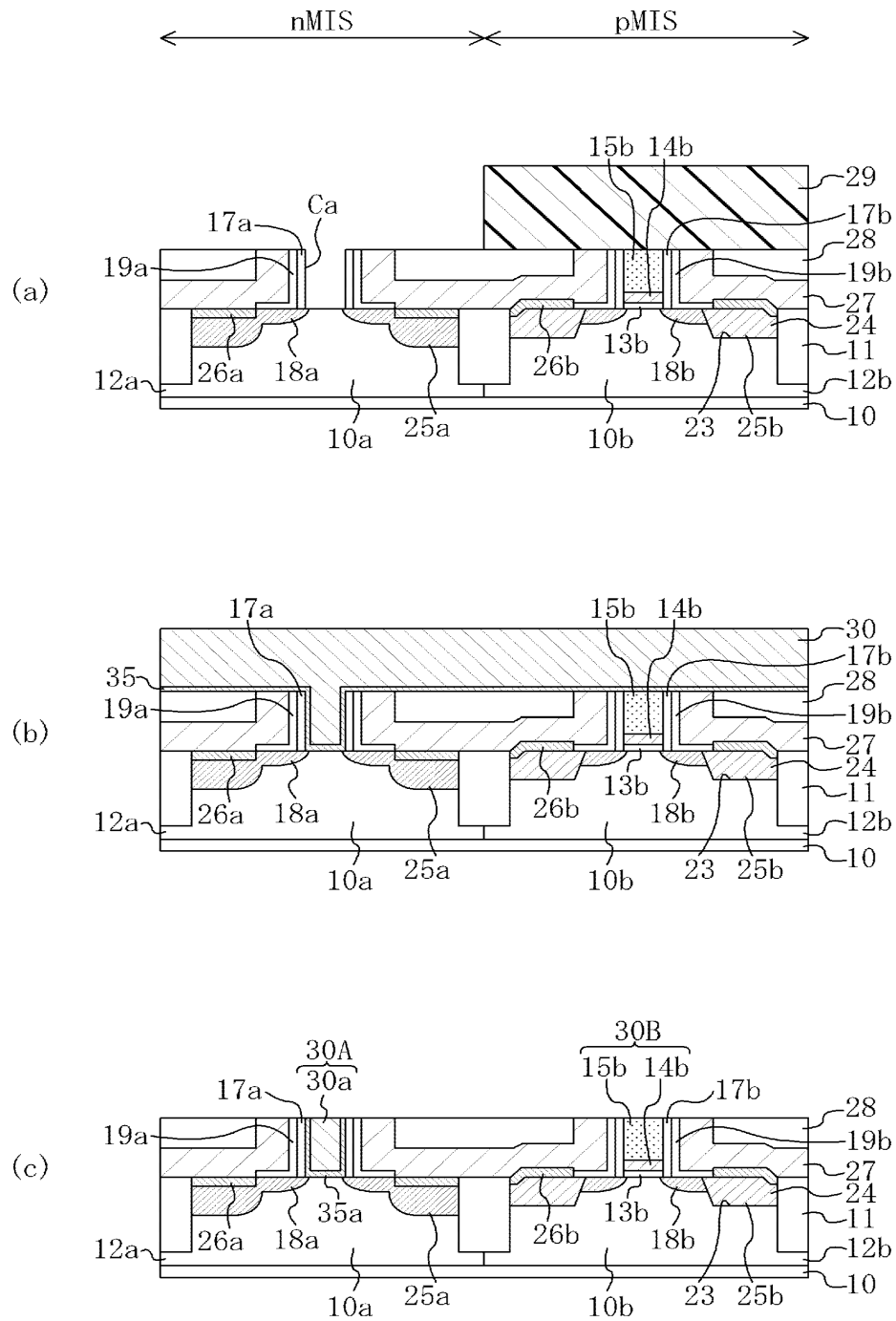
【例 8】



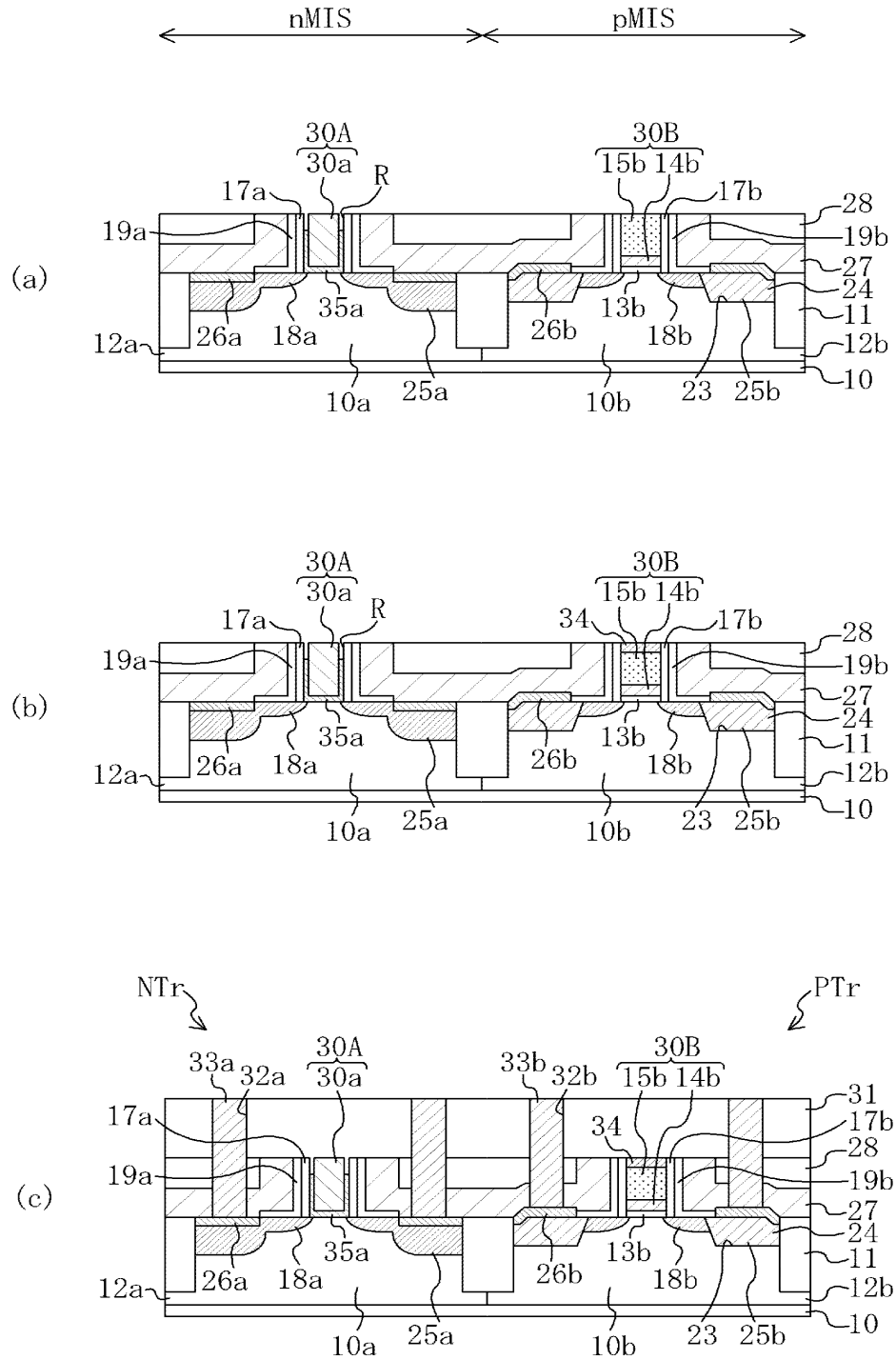
【図 9】



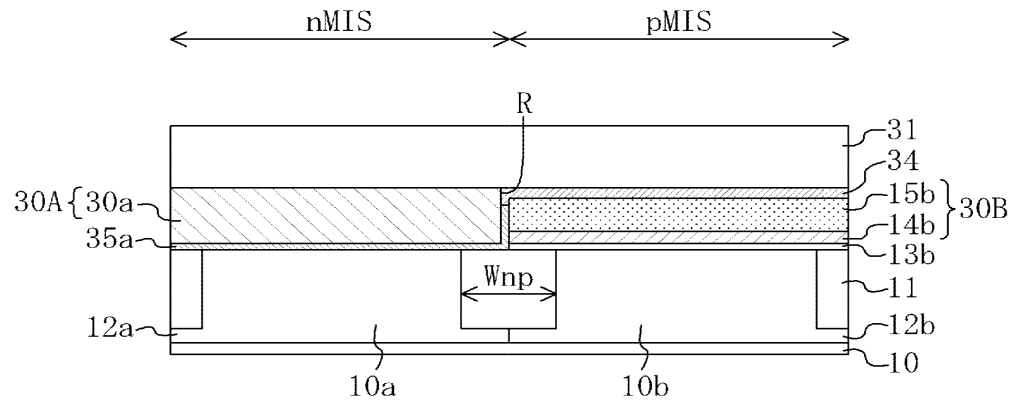
【図 10】



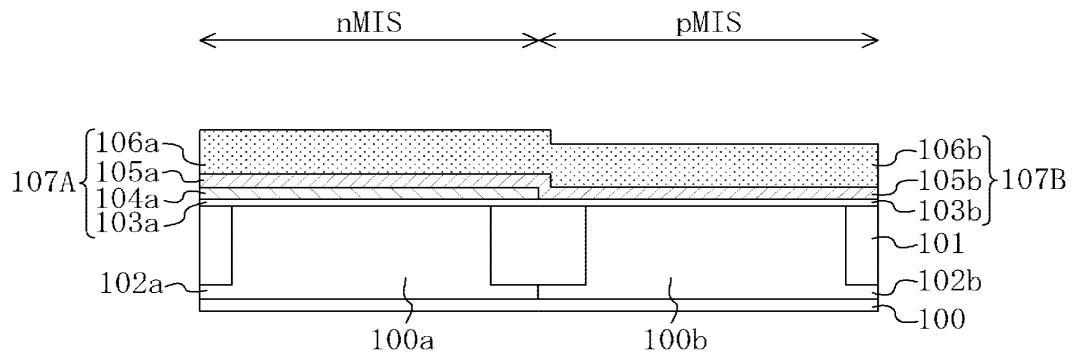
【図 1 1】

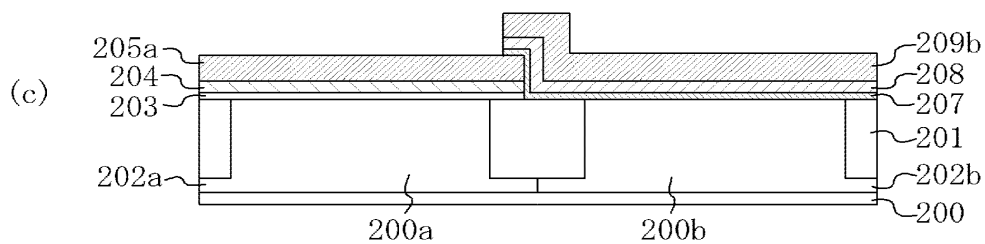
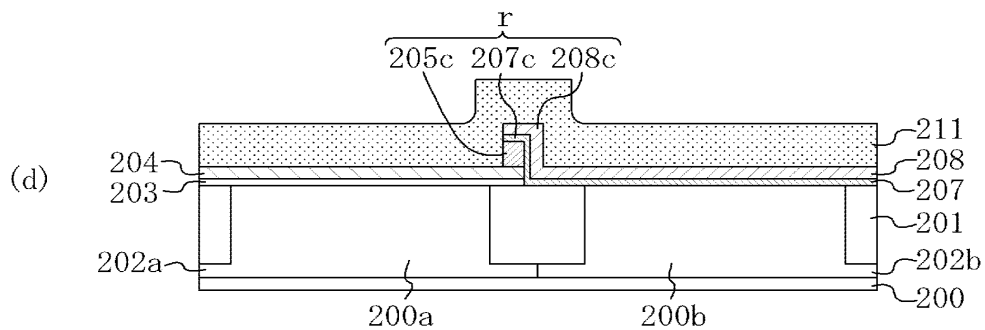
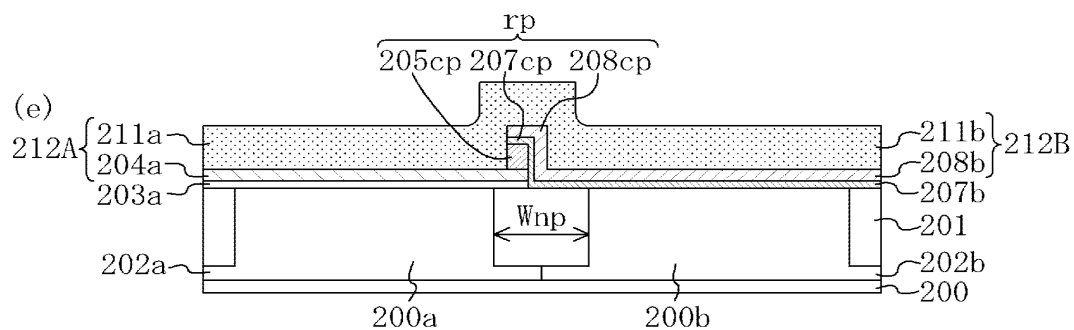


【図 1 2】

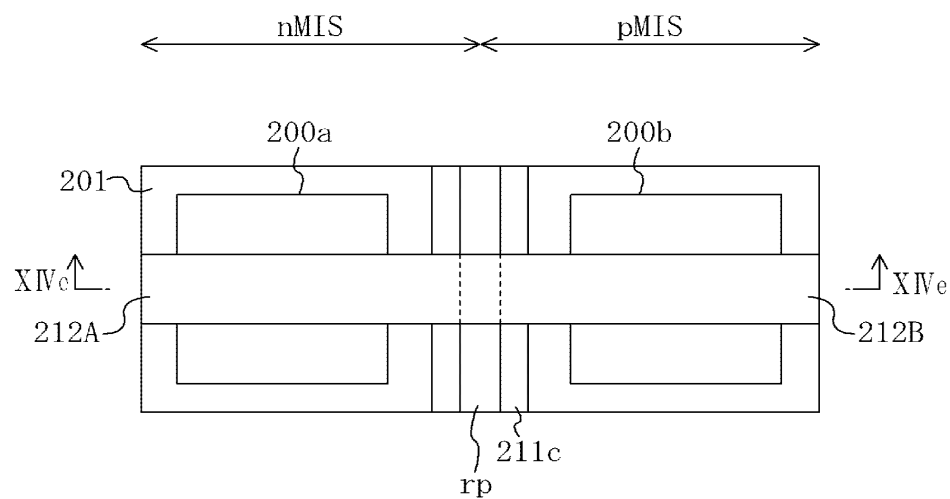


【図 1 3】

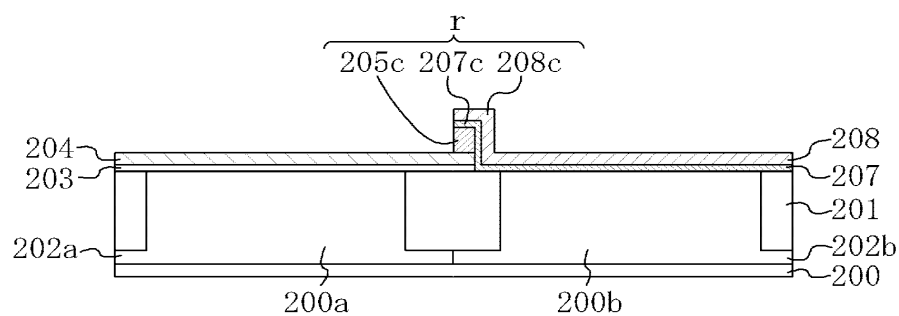


[illegible]

【図 1 5】



【図 1 6】



【書類名】要約書

【要約】

【課題】精度良く形成された第1，第2のゲート電極を実現すると共に、ゲート幅方向の幅が縮小化された素子分離領域を実現する。

【解決手段】第1のMISトランジスタは、第1のゲート絶縁膜13a上に形成された第2の金属膜30aからなる第1のゲート電極30Aと、第1のゲート電極の側面上から第1の活性領域10aにおける第1のゲート電極の側方に位置する領域の上面上に跨って形成された絶縁膜27とを備え、第2のMISトランジスタは、第2のゲート絶縁膜13b上に形成され第1の金属膜14bと第1の金属膜上に形成された導電膜30bとからなる第2のゲート電極30Bと、第2のゲート電極の側面上から第2の活性領域における第2のゲート電極の側方に位置する領域の上面上に跨って形成された絶縁膜27とを備え、第1の金属膜と第2の金属膜とは、互いに異なる金属材料からなり、第1，第2のゲート電極の上面上には絶縁膜が形成されていない。

【選択図】図5

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/629,508	12/02/2009	Yoshihiro SATO	085393-0059

CONFIRMATION NO. 7931

PUBLICATION NOTICE

McDERMOTT WILL & EMERY LLP
600 13th Street, N.W.
Washington, DC 20005-3096



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Title:SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

Publication No.US-2010-0072523-A1

Publication Date:03/25/2010

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/629,508	12/02/2009	Yoshihiro SATO	085393-0059	7931
<div>7590 02/22/2011 McDERMOTT WILL & EMERY LLP 600 13th Street, N.W. Washington, DC 20005-3096</div>			<div>EXAMINER PRENTY, MARK V</div>	
			<div>ART UNIT 2822</div>	<div>PAPER NUMBER</div>
			<div>MAIL DATE 02/22/2011</div>	<div>DELIVERY MODE PAPER</div>

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/629,508	SATO ET AL.	
	Examiner	Art Unit	
	MARK PRENTY	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 02 December 2009.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☒ Claim(s) 15-20 is/are allowed.

6) ☒ Claim(s) 1-5, 7, 9 and 14 is/are rejected.

7) ☒ Claim(s) 6, 8 and 10-13 is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on 02 December 2009 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some * c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892) 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>12/2/2009</u>	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ 5) ☐ Notice of Informal Patent Application 6) ☐ Other: _____
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This Office Action is in response to the papers filed on December 2, 2009.

Claims 1-4 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by United States Patent Application Publication 2007/0215950 to Aoyama (cited in the Information Disclosure Statement filed on December 2, 2009).

As to independent claim 1, Aoyama discloses a semiconductor device (see the entire patent, including the Fig. 1 disclosure) comprising: a first MIS transistor; and a second MIS transistor, wherein the first MIS transistor includes a first gate insulating film 102 formed on a first active region 121 in a semiconductor substrate 101, a first gate electrode 104 includes a second metal film 104A formed on the gate insulating film, and an insulating film 145 (Fig. 2J) formed, extending over side surfaces of the first gate electrode and upper surfaces of regions located in the first active region laterally outside the first gate electrode, the second MIS transistor includes a second gate insulating film 102 formed on a second active region 111 in the semiconductor substrate, a second gate electrode 103 including a first metal film 103A formed on the second gate insulating film and a conductive film 103B formed on the first metal film, and the insulating film 145 (Fig. 2J) formed, extending over side surfaces of the second gate electrode and upper surfaces of regions located in the second active region laterally outside the second gate electrode, the first and second metal films 103A and 104A are made of different metal materials (see page 4, paragraph [0049], and page 5, paragraph [0059]), and the insulating film 145 is not formed on any of upper surfaces of the first and second gate electrodes.

Claim 1 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Aoyama.

As to dependent claim 2, Aoyama's first metal film 103A has a thickness smaller than that of the second metal film 104A.

Claim 2 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Aoyama.

As to dependent claim 3, Aoyama's first and second metal films are made of different materials and thus have different work functions.

Claim 3 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Aoyama.

As to dependent claim 4, Aoyama's insulating film 145 (Fig. 2J) has a thickness smaller than that of the first gate electrode 104.

Claim 4 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Aoyama.

As to dependent claim 7, Aoyama's first and second gate insulating films 102 are made of the same insulating material (see page 4, paragraph [0052], last sentence).

Claim 7 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Aoyama.

Claims 1-3, 7 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by United States Patent Application Publication 2007/0173025 to Akamatsu (cited in the Information Disclosure Statement filed on December 2, 2009).

As to independent claim 1, Akamatsu discloses a semiconductor device (see the entire patent, including the Fig. 7 disclosure) comprising: a first MIS transistor; and a second MIS transistor, wherein the first MIS transistor includes a first gate insulating film 11a formed on a first active region in a semiconductor substrate 10, a first gate electrode includes a second metal film 36 formed on the gate insulating film, and an insulating film 22 formed, extending over side surfaces of the first gate electrode and

upper surfaces of regions located in the first active region laterally outside the first gate electrode, the second MIS transistor includes a second gate insulating film 11b formed on a second active region in the semiconductor substrate, a second gate electrode including a first metal film 37 formed on the second gate insulating film and a conductive film 35b formed on the first metal film, and the insulating film 22 formed, extending over side surfaces of the second gate electrode and upper surfaces of regions located in the second active region laterally outside the second gate electrode, the first and second metal films 36 and 37 are made of different metal materials (see paragraph [0104] bridging pages 8-9), and the insulating film 22 is not formed on any of upper surfaces of the first and second gate electrodes.

Claim 1 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Akamatsu.

As to dependent claim 2, Akamatsu's first metal film 37 has a thickness smaller than that of the second metal film 36.

Claim 2 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Akamatsu.

As to dependent claim 3, Akamatsu's first and second metal films are made of different materials and thus have different work functions.

Claim 3 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Akamatsu.

As to dependent claim 7, Akamatsu's first and second gate insulating films 11a and 11b are made of the same insulating material (see the Figs. 5A-5C disclosure).

Claim 7 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Akamatsu.

As to dependent claim 14, Akamatsu's first and second gate insulating films 11a and 11b include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more (see the sentence bridging pages 4 and 5).

Claim 14 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Akamatsu.

Claims 1-3, 5, 7 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Japanese Kokai 2002-118175 to Yasushi (cited in the Information Disclosure Statement filed on December 2, 2009).

As to independent claim 1, Yasushi discloses a semiconductor device (see the entire reference, including the English language cover page and the Fig. 11(k) disclosure) comprising: a first MIS transistor (the P MISFET); and a second MIS transistor (the N MISFET), wherein the first MIS transistor includes a first gate insulating film formed on a first active region in a semiconductor substrate, a first gate electrode includes a second metal film 617 formed on the gate insulating film, and an insulating film 614 formed, extending over side surfaces of the first gate electrode and upper surfaces of regions located in the first active region laterally outside the first gate electrode, the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate, a second gate electrode including a first metal film 616 formed on the second gate insulating film and a conductive film

617 formed on the first metal film, and the insulating film 614 formed, extending over side surfaces of the second gate electrode and upper surfaces of regions located in the second active region laterally outside the second gate electrode, the first and second metal films 616 and 617 are made of different metal materials (see the English language cover page), and the insulating film 614 is not formed on any of upper surfaces of the first and second gate electrodes.

Claim 1 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Yasushi.

As to dependent claim 2, Yasushi's first metal film 616 has a thickness smaller than that of the second metal film 617.

Claim 2 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Yasushi.

As to dependent claim 3, Yasushi's first and second metal films 616 and 617 have different work functions (see the English language cover page).

Claim 3 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Yasushi.

As to dependent claim 5, Yasushi's conductive film (over first metal film 616) is made of the second metal film 617.

Claim 5 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Yasushi.

As to dependent claim 7, Yasushi's first and second gate insulating films are made of the same insulating material (see Fig. 10(h)).

Claim 7 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Yasushi.

As to dependent claim 9, Yasushi's Fig. 11(k) device further comprises a first inner sidewall having an L-shaped cross-section formed on each of side surfaces of the first gate electrode, and a second inner sidewall having an L-shaped cross-section

formed on each of side surfaces of the second gate electrode, wherein the insulating film 614 is formed above and in contact with the first and second inner sidewalls.

Claim 9 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Yasushi.

Claims 6, 8 and 10-13 are objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 15-20 are allowable over the prior art of record.

United States Patent 6,420,279 is cited for disclosing that hafnium oxide (HfO_2) has a high dielectric constant of 20 to 25 (see column 1, lines 39-42).

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

/MARK PRENTY/
Primary Examiner, Art Unit 2822

Notice of References Cited	Application/Control No. 12/629,508	Applicant(s)/Patent Under Reexamination SATO ET AL.	
	Examiner MARK PRENTY	Art Unit 2822	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,420,279	07-2002	Ono et al.	438/785
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

SHEET 1 OF 1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Substitute for form 1449/PTO)				ATTY. DOCKET NO. 085393-0059		SERIAL NO. Not Yet Assigned	
				APPLICANT Yoshihiro SATO, et al.			
				FILING DATE December 02, 2009		GROUP Not Yet Assigned	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
		US 2007/0215950 A1	09-20-2007	AOYAMA			
		US 6,184,083 B1	02-06-2001	TSUNASHIMA et al.			
		US 7,361,960 B1	04-22-2008	TSUNASHIMA et al.			
		US 2006/0094193 A1	05-04-2006	HORSTMANN et al.			
		US 2007/0090427 A1	04-26-2007	NAKAJIMA			
		US 2007/0173025 A1	07-26-2007	AKAMATSU			
		US 2005/0167762 A1	08-04-2005	KADOSHIMA et al.			
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number & Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes No	
		JP 2007-258267	10-04-2007	TOSHIBA CORP		English Abstract Only	
		JP 2002-118175	04-19-2002	TOSHIBA CORP		JAPAN (w/English abstract)	
		JP 11-074368	03-16-1999	TOKYO SHIBAURA ELECTRIC CO		English Abstract Only	
		WO 2006/049834 A1	05-11-2006	ADVANCED MICRO DEVICES, INC.		English Original	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
		ZHANG, Z.B., et al., "Integration of Dual Metal Gate CMOS with TaSiN (NMOS) and Ru (PMOS) Gate Electrodes on HfO ₂ Gate Dielectric", Symposium on VLSI Technology Digest of Technical Papers, 2005, Pages 50-51					
		SONG, S.C., et al., "Highly Manufacturable 45 nm LSTP CMOSFETs Using Novel Dual High-k and Dual Metal Gate CMOS Integration", Symposium on VLSI Technology Digest of Technical Papers, 2006, IEEE					
		HUSSAIN, M., et al. "Compatibility of ALD Hafnium Silicate with Dual Metal Gate CMOS Integration", Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Pages 1114-1115					
		OOTSUKA, F., et al., "Full-Metal-Gate Integration of Dual-Metal-Gate HfSiON CMOS Transistors by Using Oxidation-Free Dummy-Mask Process", Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Pages 1116-1117					
EXAMINER /Mark Prenty/ (02/17/2011)				DATE CONSIDERED 02/17/2011			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.P./

Search Notes 	Application/Control No. 12629508	Applicant(s)/Patent Under Reexamination SATO ET AL.
	Examiner MARK PRENTY	Art Unit 2822

SEARCHED			
Class	Subclass	Date	Examiner
257	369, 407, 412, 413	2/17/11	mp
438	199, 592	2/17/11	mp

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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BIB DATA SHEET

CONFIRMATION NO. 7931

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
12/629,508	12/02/2009	257	2822	085393-0059		
RULE						
APPLICANTS Yoshihiro SATO, Hyogo, JAPAN; Hisashi Ogawa, Osaka, JAPAN; ** CONTINUING DATA ***** This application is a CON of PCT/JP2009/000574 02/13/2009 ** FOREIGN APPLICATIONS ***** JAPAN 2008-064435 03/13/2008 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 12/14/2009						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and Acknowledged <u>/MARK V PRENTY/</u> Examiner's Signature		☐ Met after Allowance <u> </u> Initials	STATE OR COUNTRY JAPAN	SHEETS DRAWINGS 14	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 2
ADDRESS McDERMOTT WILL & EMERY LLP 600 13th Street, N.W. Washington, DC 20005-3096 UNITED STATES						
TITLE SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME						
FILING FEE RECEIVED 1090	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Docket No.: 085393-0059

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Yoshihiro SATO, et al.	:	Confirmation Number: 7931
	:	
Application No.: 12/629,508	:	Group Art Unit: 2822
	:	
Filed: December 02, 2009	:	Examiner: PRENTY, Mark V.
	:	
For: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME	:	

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated February 22, 2011, wherein a three-month shortened statutory period for response is set to expire on May 22, 2011 (Sunday), Applicants respectfully request reconsideration of the above-identified application in view of the following amendments and remarks.

AMENDMENT TO THE CLAIMS

The following claim listing replaces all prior listings and versions of the claims:

LISTING OF CLAIMS

1. (Currently amended) A semiconductor device comprising:

a first MIS transistor; and

a second MIS transistor, wherein;

the first MIS transistor includes

a first gate insulating film formed on a first active region in a semiconductor substrate,

a first gate electrode includes a second metal film formed on the first gate insulating film, and

an insulating film formed, extending over side surfaces of the first gate electrode and upper surfaces of regions located in the first active region laterally outside the first gate electrode,

the second MIS transistor includes

a second gate insulating film formed on a second active region in the semiconductor substrate,

a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film, [[and]]

the insulating film formed, extending over side surfaces of the second gate electrode and upper surfaces of regions located in the second active region laterally outside the second gate electrode, and

source/drain regions formed in the second active region laterally outside the

second gate electrode,

the first and second metal films are made of different metal materials, [[and]]

the insulating film is not formed on any of upper surfaces of the first and second gate electrodes,

the source/drain regions include a silicon mixed crystal layer which is formed in trenches provided in the second active region, and causes first stress in a gate length direction of a channel region in the second active region.

2. (Original) The semiconductor device of claim 1, wherein
the first metal film has a thickness smaller than that of the second metal film.
3. (Original) The semiconductor device of claim 1, wherein
the first and second metal films have different work functions.
4. (Original) The semiconductor device of claim 1, wherein
the insulating film has a thickness smaller than that of the first gate electrode.
5. (Original) The semiconductor device of claim 1, wherein
the conductive film is made of the second metal film.
6. (Original) The semiconductor device of claim 1, wherein
the conductive film is made of a silicon film, and
the semiconductor device further comprises a metal silicide film formed on the silicon

film.

7. (Original) The semiconductor device of claim 1, wherein
the first and second gate insulating films are made of the same insulating material.

8. (Original) The semiconductor device of claim 1, wherein
the first and second gate insulating films are made of different insulating materials.

9. (Original) The semiconductor device of claim 1, further comprising:
a first inner sidewall having an L-shaped cross-section formed on each of side surfaces of
the first gate electrode, and
a second inner sidewall having an L-shaped cross-section formed on each of side surfaces
of the second gate electrode,
wherein
the insulating film is formed above and in contact with the first and second inner
sidewalls.

10. (Currently amended) The semiconductor device of claim 1, wherein
the insulating film is a stress insulating film which causes [[first]] second stress in a gate
length direction of a channel region in the first active region.

11. (Currently amended) The semiconductor device of claim 10, wherein
the first MIS transistor is an n-type MIS transistor,

the insulating film is made of a silicon nitride film, and
the ~~[[first]]~~ second stress is tensile stress.

12. (Cancelled)

13. (Currently amended) The semiconductor device of claim ~~[[12]]~~ 1, wherein
the second MIS transistor is a p-type MIS transistor,
the silicon mixed crystal layer is made of a SiGe layer, and
the ~~second~~ first stress is compressive stress.

14. (Original) The semiconductor device of claim 1, wherein
the first and second gate insulating films include a high-k film made of a metal oxide
having a relative dielectric constant of 10 or more.

15. (Original) A method for manufacturing a semiconductor device including a first
MIS transistor formed on a first active region in a semiconductor substrate and a second MIS
transistor formed on a second active region in the semiconductor substrate, the method
comprising the steps of:

(a) forming a first gate electrode formation portion having a first gate insulating film, a
first metal film and a first silicon film on the first active region, and a second gate electrode
formation portion having a second gate insulating film, a first metal film and a second silicon
film on the second active region;

(b) after step (a), forming an insulating film on the semiconductor substrate, the

Application No.: 12/629,508

insulating film covering the first and second gate electrode formation portions;

(c) removing the insulating film formed on the first and second gate electrode formation portions to expose an upper surface of each of the first silicon film in the first gate electrode formation portion and the second silicon film in the second gate electrode formation portion;

(d) after step (c), successively removing the first silicon film and the first metal film in the first gate electrode formation portion to form a first recess surrounded by the insulating film on the first active region; and

(e) forming a second metal film in the first recess,

wherein

a first gate electrode of the first MIS transistor includes the second metal film, and

a second gate electrode of the second MIS transistor includes the first metal film in the second gate electrode formation portion.

16. (Original) The method of claim 15, wherein

step (d) includes forming, on the first active region, the first recess from a bottom of which the first gate insulating film is exposed, and removing the second silicon film in the second gate electrode formation portion to form, on the second active region, a second recess surrounded by the insulating film, the first metal film being exposed from a bottom of the second recess,

step (e) includes forming the second metal film on the first gate insulating film in the first recess, and forming the second metal film on the first metal film in the second recess, and

the second gate electrode includes the first metal film in the second gate electrode formation portion and the second metal film formed on the first metal film.

17. (Original) The method of claim 15, wherein

step (d) includes forming, on the first active region, the first recess from a bottom of which the first gate insulating film is exposed,

step (e) includes forming the second metal film on the first gate insulating film in the first recess,

the method further comprises the step of

(f) after step (e), forming a metal silicide film on the second silicon film, and

the second gate electrode includes the first metal film and the second silicon film in the second gate electrode formation portion.

18. (Original) The method of claim 15, wherein

step (d) includes successively removing the first silicon film, the first metal film, and the first gate insulating film in the first gate electrode formation portion, to form, on the first active region, the first recess from a bottom of which the first active region is exposed,

step (e) includes forming a third gate insulating film in the first recess, and forming the second metal film on the third gate insulating film,

the method further comprises the step of

(f) after step (e), forming a metal silicide film on the second silicon film, and

the second gate electrode includes the first metal film and the second silicon film in the second gate electrode formation portion.

19. (Original) The method of claim 15, further comprising the step of:

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(g) after step (a) and before step (b), forming a first inner sidewall having an L-shaped cross-section on each of side surfaces of the first gate electrode formation portion, and a second inner sidewall having an L-shaped cross-section on each of side surfaces of the second gate electrode formation portion,

wherein

in step (b), the insulating film is formed above and in contact with the first and second inner sidewalls.

20. (Original) The method of claim 15, further comprising the steps of:

(h) after step (a) and before step (b), forming trenches in the second active region laterally outside the second gate electrode formation portion; and

(i) forming, in the trenches, a silicon mixed crystal layer which causes stress in a gate length direction of a channel region in the second active region.

21. (New) A semiconductor device comprising:

a first MIS transistor; and

a second MIS transistor, wherein:

the first MIS transistor includes

a first gate insulating film formed on a first active region in a semiconductor substrate,

a first gate electrode including a second metal film formed on the first gate insulating film, and

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an insulating film formed, extending over side surfaces of the first gate electrode and upper surfaces of regions located in the first active region laterally outside the first gate electrode,

the second MIS transistor includes

a second gate insulating film formed on a second active region in the semiconductor substrate,

a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film, and

the insulating film formed, extending over side surfaces of the second gate electrode and upper surfaces of regions located in the second active region laterally outside the second gate electrode,

the first and second metal films are made of different metal materials,

the insulating film is not formed on any of upper surfaces of the first and second gate electrodes,

the conductive film is made of a silicon film, and

the semiconductor device further comprises a metal silicide film formed on the silicon film.

22. (New) The semiconductor device of claim 21, wherein
the first metal film has a thickness smaller than that of the second metal film.

23. (New) The semiconductor device of claim 21, wherein
the first and second metal films have different work functions.

24. (New) The semiconductor device of claim 21, wherein
the insulating film has a thickness smaller than that of the first gate electrode.

25. (New) The semiconductor device of claim 21, wherein
the first and second gate insulating films are made of the same insulating material.

26. (New) The semiconductor device of claim 21, wherein
the first and second gate insulating films are made of different insulating materials.

27. (New) The semiconductor device of claim 21, further comprising:
a first inner sidewall having an L-shaped cross-section formed on each of side surfaces of
the first gate electrode, and
a second inner sidewall having an L-shaped cross-section formed on each of side surfaces
of the second gate electrode,
wherein the insulating film is formed above and in contact with the first and second inner
sidewalls.

28. (New) The semiconductor device of claim 21, wherein
the insulating film is made of a silicon nitride film.

29. (New) The semiconductor device of claim 21, further comprising:

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source/drain regions formed in the second active region laterally outside the second gate electrode,

wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.

30. (New) The semiconductor device of claim 21, wherein
the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.

31. (New) A semiconductor device comprising:
a first MIS transistor; and
a second MIS transistor, wherein:
the first MIS transistor includes
a first gate insulating film formed on a first active region in a semiconductor substrate,
a first gate electrode including a second metal film formed on the first gate insulating film, and
an insulating film formed, extending over side surfaces of the first gate electrode and upper surfaces of regions located in the first active region laterally outside the first gate electrode,
the second MIS transistor includes
a second gate insulating film formed on a second active region in the semiconductor substrate,

a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film, and

the insulating film formed, extending over side surfaces of the second gate electrode and upper surfaces of regions located in the second active region laterally outside the second gate electrode,

the first and second metal films are made of different metal materials,

the insulating film is not formed on any of upper surfaces of the first and second gate electrodes, and

the first and second gate insulating films are made of different insulating materials.

32. (New) The semiconductor device of claim 31, wherein
the first metal film has a thickness smaller than that of the second metal film.

33. (New) The semiconductor device of claim 31, wherein
the first and second metal films have different work functions.

34. (New) The semiconductor device of claim 31, wherein
the insulating film has a thickness smaller than that of the first gate electrode.

35. (New) The semiconductor device of claim 31, further comprising:
a first inner sidewall having an L-shaped cross-section formed on each of side surfaces of the first gate electrode, and

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a second inner sidewall having an L-shaped cross-section formed on each of side surfaces of the second gate electrode,

wherein the insulating film is formed above and in contact with the first and second inner sidewalls.

36. (New) The semiconductor device of claim 31, wherein the insulating film is made of a silicon nitride film.

37. (New) The semiconductor device of claim 31, further comprising: source/drain regions formed in the second active region laterally outside the second gate electrode,

wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.

38. (New) The semiconductor device of claim 31, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.

39. (New) A semiconductor device comprising:
a first MIS transistor; and
a second MIS transistor, wherein:
the first MIS transistor includes

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a first gate insulating film formed on a first active region in a semiconductor substrate,

a first gate electrode including a second metal film formed on the first gate insulating film, and

an insulating film formed, extending over side surfaces of the first gate electrode and upper surfaces of regions located in the first active region laterally outside the first gate electrode,

the second MIS transistor includes

a second gate insulating film formed on a second active region in the semiconductor substrate,

a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film, and

the insulating film formed, extending over side surfaces of the second gate electrode and upper surfaces of regions located in the second active region laterally outside the second gate electrode,

the first and second metal films are made of different metal materials,

the insulating film is not formed on any of upper surfaces of the first and second gate electrodes, and

the insulating film is a stress insulating film which causes first stress in a gate length direction of a channel region in the first active region.

40. (New) The semiconductor device of claim 39, wherein
- the first metal film has a thickness smaller than that of the second metal film.

41. (New) The semiconductor device of claim 39, wherein the first and second metal films have different work functions.

42. (New) The semiconductor device of claim 39, wherein the insulating film has a thickness smaller than that of the first gate electrode.

43. (New) The semiconductor device of claim 39, wherein the conductive film is made of the second metal film.

44. (New) The semiconductor device of claim 39, wherein:
the conductive film is made of a silicon film, and
the semiconductor device further comprises a metal silicide film formed on the silicon film.

45. (New) The semiconductor device of claim 39, wherein the first and second gate insulating films are made of the same insulating material.

46. (New) The semiconductor device of claim 39, wherein the first and second gate insulating films are made of different insulating materials.

47. (New) The semiconductor device of claim 39, further comprising:

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a first inner sidewall having an L-shaped cross-section formed on each of side surfaces of the first gate electrode, and

a second inner sidewall having an L-shaped cross-section formed on each of side surfaces of the second gate electrode,

wherein the insulating film is formed above and in contact with the first and second inner sidewalls.

48. (New) The semiconductor device of claim 39, wherein the insulating film is made of a silicon nitride film.

49. (New) The semiconductor device of claim 39, further comprising: source/drain regions formed in the second active region laterally outside the second gate electrode,

wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.

50. (New) The semiconductor device of claim 39, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.

REMARKS

Introduction

Claims 1-20 were pending, of which claims 1 and 15 are independent.

Applicants note with appreciation the indication of allowance of claims 15-20 and the indication of allowable subject matter in claims 6, 8 and 10-13 if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 1 has been amended to incorporate the allowable subject matter of claim 12. Claims 1, 10, 11 and 13 have been amended to correct informalities in the claim language and to more clearly define the claimed subject matter. Claim 12 has been cancelled.

Claims 21-50 have been added. New independent claims 21, 31 and 39 correspond to allowable claims 6, 8 and 10, respectively. Care has been taken to avoid introducing new matter.

Patentability under 35 U.S.C. § 102

Claims 1-4, and 7 were rejected under 35 U.S.C. § 102(e) as being anticipated by Aoyama (US 2007/0215950). Claims 1-3, 7 and 14 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Akamatsu (US 2007/0173025). Claims 1-3, 5, 7 and 9 were rejected under 35 U.S.C. § 102(b) as being anticipated by Yasushi (JP 2002-118175). These rejections are traversed for at least the following reasons.

Applicants submit that since claim 1 has been amended to incorporate the allowable subject matter of original claim 12, claim 1 and all claims dependent thereon are patentable over the cited references. Thus, it is requested that the Examiner withdraw the rejections of the claims under 35 U.S.C. § 102.

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New Claims

Since new independent claims 21, 31 and 39 have incorporated the allowable subject matter of allowable claims 6, 8 and 10, respectively, claims 21, 31 and 39 and all claims dependent thereon are patentable over the cited references.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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Date: May 23, 2011

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as our correspondence address.**

Electronic Patent Application Fee Transmittal				
Application Number:		12629508		
Filing Date:		02-Dec-2009		
Title of Invention:		SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME		
First Named Inventor/Applicant Name:		Yoshihiro SATO		
Filer:		Michael E. Fogarty/3328/Matilda Mason		
Attorney Docket Number:		085393-0059		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Claims in excess of 20	1202	29	52	1508
Independent claims in excess of 3	1201	2	220	440
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1948

Electronic Acknowledgement Receipt	
EFS ID:	10152500
Application Number:	12629508
International Application Number:	
Confirmation Number:	7931
Title of Invention:	SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Yoshihiro SATO
Correspondence Address:	McDERMOTT WILL & EMERY LLP - 600 13th Street, N.W. - Washington DC 20005-3096 US 2027568000 -
Filer:	Michael E. Fogarty/3328/Matilda Mason
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0059
Receipt Date:	23-MAY-2011
Filing Date:	02-DEC-2009
Time Stamp:	19:43:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1948

RAM confirmation Number	6616				
Deposit Account	500417				
Authorized User					
<p>The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:</p> <p>Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)</p> <p>Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)</p>					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		085393-0059Amendment.pdf	146923 8450d721f8e458e456b2fa5afc4d2af4642a285c	yes	18
Multipart Description/PDF files in .zip description					
	Document Description	Start	End		
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1		
	Claims	2	16		
	Applicant Arguments/Remarks Made in an Amendment	17	18		
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	31871 83762ad99d8b63fe8eb4907b6bcd60e85e29d599	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			178794		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/629,508		Filing Date 12/02/2009		☐ To be Mailed		
APPLICATION AS FILED – PART I											
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)				
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A					
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	* 0	X \$ =		OR	X \$52 =	0				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	* 0	X \$ =			X \$220 =	0				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).										
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))											
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL		0			
APPLICATION AS AMENDED – PART II											
(Column 1)			(Column 2)			(Column 3)		SMALL ENTITY OR		OTHER THAN SMALL ENTITY	
AMENDMENT	05/23/2011	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 49	Minus	** 20	= 29	X \$ =		OR	X \$52=	1508	
	Independent (37 CFR 1.16(h))	* 5	Minus	***3	= 2	X \$ =		OR	X \$220=	440	
	☐ Application Size Fee (37 CFR 1.16(s))							OR			
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
	TOTAL ADD'L FEE							OR	TOTAL ADD'L FEE 1948		
(Column 1)			(Column 2)			(Column 3)		SMALL ENTITY OR		OTHER THAN SMALL ENTITY	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =		
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =		
	☐ Application Size Fee (37 CFR 1.16(s))							OR			
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
	TOTAL ADD'L FEE							OR	TOTAL ADD'L FEE		
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".</p> <p>*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".</p> <p>The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p>											

Legal Instrument Examiner:
/GERALDINE STANLEY/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/629,508	12/02/2009	Yoshihiro SATO	085393-0059	7931
<div>7590 06/07/2011 McDERMOTT WILL & EMERY LLP 600 13th Street, N.W. Washington, DC 20005-3096</div>			<div>EXAMINER PRENTY, MARK V</div>	
			<div>ART UNIT 2822</div>	<div>PAPER NUMBER</div>
			<div>MAIL DATE 06/07/2011</div>	<div>DELIVERY MODE PAPER</div>

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/629,508	SATO ET AL.	
	Examiner	Art Unit	
	MARK PRENTY	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 May 2011.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 and 13-50 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 31-34,36-46 and 48-50 is/are allowed.
- 6) ☒ Claim(s) 1-3,6,7,9,14,15,17,19-23,25,27,30,35 and 47 is/are rejected.
- 7) ☒ Claim(s) 4,5,8,10,11,13,16,18,24,26,28 and 29 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) ☐ Information Disclosure Statement(s) (PTO/SB/08) | 5) ☐ Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) ☐ Other: _____ |

This Office Action is in response to the amendment filed on May 23, 2011.

Claims 9, 27, 35 and 47 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, device claims 9, 27, 35 and 47 are incorrect in reciting, "wherein the insulating film is formed above and in contact with the first and second inner sidewalls," because such is not the case in those devices. See the Figs. 3D-4A disclosure and note that the insulating film 27 is removed from above the first and second inner sidewalls 19a and 19b.

Claims 1-3, 6, 7, 14, 15, 17, 19-23, 25 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by newly cited United States Patent 7,812,414 to Hou et al. (Hou).

As to independent claim 1, Hou discloses a semiconductor device (see the entire patent, including the Fig. 11 disclosure) comprising: a first (right-side) MIS transistor; and a second (left-side) MIS transistor, wherein: the first MIS transistor includes a first gate insulating film 224 formed on a first active region 200 in a semiconductor substrate 20, a first gate electrode includes a second metal film 248 formed on the first gate insulating film, and an insulating film 42 formed, extending over side surfaces of the first gate electrode and upper surfaces of regions located in the first active region laterally outside the first gate electrode, the second MIS transistor includes a second gate insulating film 124 on a second active region 100 in the semiconductor substrate, a second gate electrode including a first metal film 126 formed on the second gate insulating film and a conductive film 128 formed on the first metal film, the insulating film

42 formed, extending over side surfaces of the second gate electrode and upper surfaces of regions located in the second active region laterally outside the second gate electrode, and source/drain regions 138 formed in the second active region laterally outside the second gate electrode, the first and second metal films 126 and 248 are made of different metal materials, the insulating film 42 is not formed on any of upper surfaces of the first and second gate electrodes, the source/drain regions 138 include a silicon mixed crystal layer which is formed in trenches provided in the second active region, and causes first stress in a gate length direction of a channel region in the second active region 100 (see column 5, lines 24-31).

Claim 1 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Hou.

As to dependent claim 2, Hou's first metal film 126 has a thickness smaller than that of the second metal film 248.

Claim 2 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Hou.

As to dependent claim 3, Hou's first and second metal films 126 and 248 have different work functions.

Claim 3 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Hou.

As to dependent claim 6, Hou's conductive film 128 is made of a silicon film (see column 5, lines 6-7), and the semiconductor device further comprises a metal silicide film 152 formed on the silicon film.

Claim 6 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Hou.

As to dependent claim 7, Hou's first and second gate insulating films 224 and 124 are made of the same insulating material (see the Figs. 1-2 disclosure).

Claim 7 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Hou.

As to dependent claim 14, Hou's first and second gate insulating films 224 and 124 include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more (see column 4, lines 27-33).

Claim 14 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Hou.

As to independent claim 15, Hou discloses a method for manufacturing a semiconductor device (see the entire patent, including the Figs. 1-11 disclosure) including a first MIS transistor formed on a first active region 200 in a semiconductor substrate 20 and a second MIS transistor formed on a second active region 100 in the semiconductor substrate, the method comprising the steps of: (a) forming a first gate electrode formation portion 234 (Fig. 2) having a first gate insulating film 224, a first metal film 226 and a first silicon film 228 on the first active region, and a second gate electrode formation portion 134 having a second gate insulating film 124, a first metal film 126 and a second silicon film 128 on the second active region; (b) after step (a), forming an insulating film 42 (Fig. 5) on the semiconductor substrate, the insulating film covering the first and second gate electrode formation portions; (c) removing the insulating film 42 formed on the first and second gate electrode formation portions to expose an upper surface of each of the first silicon film 228 in the first gate electrode formation portion and the second silicon film 128 in the second gate electrode formation portion (Fig. 6); (d) after step (c), successively removing the first silicon film 228 and the first metal film 226 in the first gate electrode formation portion to form a first recess surrounded by the insulating film 42 on the first active region 200 (Fig. 7); and (e)

forming a second metal film 248 (Fig. 9) in the first recess, wherein a first gate electrode of the first MIS transistor includes the second metal film 248, and a second gate electrode of the second MIS transistor includes the first metal film 126 in the second gate electrode formation portion.

Claim 15 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Hou.

As to dependent claim 17, Hou's step (d) includes forming, on the first active region 200, the first recess from a bottom of which the first gate insulating film 224 is exposed (Fig. 7), step (e) includes forming the second metal film 248 (Fig. 9) on the first gate insulating film 224 in the first recess, the method further comprises the step of (f) after step (e), forming a metal silicide film 152 (Fig. 11) on the second silicon film 128, and the second gate electrode includes the first metal film 126 and the second silicon film 128 in the second gate electrode formation portion.

Claim 17 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Hou.

As to dependent claim 19, Hou's method further comprises the step of (g) after step (a) and before step (b), forming a first inner sidewall 240 having an L-shaped cross-section on each of side surfaces of the first gate electrode formation portion, and a second inner sidewall 140 having an L-shaped cross-section on each of side surfaces of the second gate electrode formation portion, wherein in step (b), the insulating film 42 is formed above and in contact with the first and second inner sidewalls (Fig. 5).

Claim 19 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Hou.

As to dependent claim 20, Hou's method further comprises the steps of: (h) after step (a) and before step (b), forming trenches in the second active region 100 laterally

outside the second gate electrode formation; and (i) forming, in the trenches, a silicon mixed crystal layer which causes stress in a gate length direction of a channel region in the second active region (see column 5, lines 24-31).

Claim 20 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Hou.

As to independent claim 21, Hou discloses a semiconductor device (see the entire patent, including the Fig. 11 disclosure) comprising: a first (right-side) MIS transistor; and a second (left-side) MIS transistor, wherein: the first MIS transistor includes a first gate insulating film 224 formed on a first active region 200 in a semiconductor substrate 20, a first gate electrode includes a second metal film 248 formed on the first gate insulating film, and an insulating film 42 formed, extending over side surfaces of the first gate electrode and upper surfaces of regions located in the first active region laterally outside the first gate electrode, the second MIS transistor includes a second gate insulating film 124 on a second active region 100 in the semiconductor substrate, a second gate electrode including a first metal film 126 formed on the second gate insulating film and a conductive film 128 formed on the first metal film, the insulating film 42 formed, extending over side surfaces of the second gate electrode and upper surfaces of regions located in the second active region laterally outside the second gate electrode, the first and second metal films 126 and 248 are made of different metal materials, the insulating film 42 is not formed on any of upper surfaces of the first and second gate electrodes, the conductive film 128 is made of a silicon film (see column 5, lines 6-7), and the semiconductor device further comprises a metal silicide film 152 formed on the silicon film.

Claim 21 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Hou.

As to dependent claim 22, Hou's first metal film 126 has a thickness smaller than that of the second metal film 248.

Claim 22 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Hou.

As to dependent claim 23, Hou's first and second metal films 126 and 248 have different work functions.

Claim 23 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Hou.

As to dependent claim 25, Hou's first and second gate insulating films 224 and 124 are made of the same insulating material (see the Figs. 1-2 disclosure).

Claim 25 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Hou.

As to dependent claim 30, Hou's first and second gate insulating films 224 and 124 include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more (see column 4, lines 27-33).

Claim 30 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Hou.

Claims 4, 5, 8, 10, 11, 13, 16, 18, 24, 26, 28 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 31-34, 36-46 and 48-50 are allowable over the prior art of record.

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Art Unit: 2822

Page 8

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

/MARK PRENTY/
Primary Examiner, Art Unit 2822

Notice of References Cited	Application/Control No. 12/629,508	Applicant(s)/Patent Under Reexamination SATO ET AL.	
	Examiner MARK PRENTY	Art Unit 2822	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,812,414	10-2010	Hou et al.	257/412
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Docket No.: 085393-0059

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Yoshihiro SATO, et al.	:	Confirmation Number: 7931
	:	
Application No.: 12/629,508	:	Group Art Unit: 2822
	:	
Filed: December 02, 2009	:	Examiner: PRENTY, Mark V.
	:	
For: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME	:	

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated June 7, 2011, wherein a three-month shortened statutory period for response is set to expire on September 7, 2011, Applicants respectfully request reconsideration of the above-identified application in view of the following amendments and remarks.

AMENDMENT TO THE CLAIMS

The following claim listing replaces all prior listings and versions of the claims:

LISTING OF CLAIMS

1. (Currently amended) A semiconductor device comprising:
a first MIS transistor; and
a second MIS transistor, wherein:
the first MIS transistor includes
a first gate insulating film formed on a first active region in a
semiconductor substrate,
a first gate electrode includes a second metal film formed on the first gate
insulating film, and
an insulating film formed, extending over side surfaces of the first gate
electrode and upper surfaces of regions located in the first active region laterally outside the first
gate electrode,
the second MIS transistor includes
a second gate insulating film formed on a second active region in the
semiconductor substrate,
a second gate electrode including a first metal film formed on the second
gate insulating film and a conductive film formed on the first metal film,
the insulating film formed, extending over side surfaces of the second gate
electrode and upper surfaces of regions located in the second active region laterally outside the
second gate electrode, and
source/drain regions formed in the second active region laterally outside the

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second gate electrode,

the first and second metal films are made of different metal materials,

the insulating film is not formed on any of upper surfaces of the first and second gate electrodes,

the source/drain regions include a silicon mixed crystal layer which is formed in trenches provided in the second active region, and causes first stress in a gate length direction of a channel region in the second active region, and

the insulating film has a thickness smaller than that of the first gate electrode.

2. (Original) The semiconductor device of claim 1, wherein

the first metal film has a thickness smaller than that of the second metal film.

3. (Original) The semiconductor device of claim 1, wherein

the first and second metal films have different work functions.

4. (Cancelled)

5. (Original) The semiconductor device of claim 1, wherein

the conductive film is made of the second metal film.

6. (Original) The semiconductor device of claim 1, wherein

the conductive film is made of a silicon film, and

the semiconductor device further comprises a metal silicide film formed on the silicon

film.

7. (Original) The semiconductor device of claim 1, wherein
the first and second gate insulating films are made of the same insulating material.
8. (Original) The semiconductor device of claim 1, wherein
the first and second gate insulating films are made of different insulating materials.
9. (Currently Amended) The semiconductor device of claim 1, further comprising:
a first inner sidewall having an L-shaped cross-section formed on each of side surfaces of
the first gate electrode, and
a second inner sidewall having an L-shaped cross-section formed on each of side surfaces
of the second gate electrode,
wherein
the insulating film is formed ~~above and~~ in contact with surfaces of the first and second
inner sidewalls which are bent in an L-shape.
10. (Previously Presented) The semiconductor device of claim 1, wherein
the insulating film is a stress insulating film which causes second stress in a gate length
direction of a channel region in the first active region.
11. (Previously Presented) The semiconductor device of claim 10, wherein
the first MIS transistor is an n-type MIS transistor,

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the insulating film is made of a silicon nitride film, and
the second stress is tensile stress.

12. (Cancelled)

13. (Previously Presented) The semiconductor device of claim 1, wherein
the second MIS transistor is a p-type MIS transistor,
the silicon mixed crystal layer is made of a SiGe layer, and
the first stress is compressive stress.

14. (Original) The semiconductor device of claim 1, wherein
the first and second gate insulating films include a high-k film made of a metal oxide
having a relative dielectric constant of 10 or more.

15. (Currently Amended) A method for manufacturing a semiconductor device
including a first MIS transistor formed on a first active region in a semiconductor substrate and a
second MIS transistor formed on a second active region in the semiconductor substrate, the
method comprising the steps of:

(a) forming a first gate electrode formation portion having a first gate insulating film, a
first metal film and a first silicon film on the first active region, and a second gate electrode
formation portion having a second gate insulating film, a first metal film and a second silicon
film on the second active region;

(b) after step (a), forming an insulating film on the semiconductor substrate, the

insulating film covering the first and second gate electrode formation portions;

(c) removing the insulating film formed on the first and second gate electrode formation portions to expose an upper surface of each of the first silicon film in the first gate electrode formation portion and the second silicon film in the second gate electrode formation portion;

(d) after step (c), successively removing the first silicon film and the first metal film in the first gate electrode formation portion to form a first recess surrounded by the insulating film on the first active region; and

(e) forming a second metal film in the first recess,

wherein:

a first gate electrode of the first MIS transistor includes the second metal film, [[and]]

a second gate electrode of the second MIS transistor includes the first metal film in the second gate electrode formation portion, and

the insulating film has a thickness smaller than that of the first gate electrode.

16. (Original) The method of claim 15, wherein

step (d) includes forming, on the first active region, the first recess from a bottom of which the first gate insulating film is exposed, and removing the second silicon film in the second gate electrode formation portion to form, on the second active region, a second recess surrounded by the insulating film, the first metal film being exposed from a bottom of the second recess,

step (e) includes forming the second metal film on the first gate insulating film in the first recess, and forming the second metal film on the first metal film in the second recess, and

the second gate electrode includes the first metal film in the second gate electrode

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formation portion and the second metal film formed on the first metal film.

17. (Original) The method of claim 15, wherein

step (d) includes forming, on the first active region, the first recess from a bottom of which the first gate insulating film is exposed,

step (e) includes forming the second metal film on the first gate insulating film in the first recess,

the method further comprises the step of

(f) after step (e), forming a metal silicide film on the second silicon film, and

the second gate electrode includes the first metal film and the second silicon film in the second gate electrode formation portion.

18. (Original) The method of claim 15, wherein

step (d) includes successively removing the first silicon film, the first metal film, and the first gate insulating film in the first gate electrode formation portion, to form, on the first active region, the first recess from a bottom of which the first active region is exposed,

step (e) includes forming a third gate insulating film in the first recess, and forming the second metal film on the third gate insulating film,

the method further comprises the step of

(f) after step (e), forming a metal silicide film on the second silicon film, and

the second gate electrode includes the first metal film and the second silicon film in the second gate electrode formation portion.

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19. (Currently Amended) The method of claim 15, further comprising the step of:

(g) after step (a) and before step (b), forming a first inner sidewall having an L-shaped cross-section on each of side surfaces of the first gate electrode formation portion, and a second inner sidewall having an L-shaped cross-section on each of side surfaces of the second gate electrode formation portion,

wherein

in step (b), the insulating film is formed ~~above and~~ in contact with surfaces of the first and second inner sidewalls.

20. (Original) The method of claim 15, further comprising the steps of:

(h) after step (a) and before step (b), forming trenches in the second active region laterally outside the second gate electrode formation portion; and

(i) forming, in the trenches, a silicon mixed crystal layer which causes stress in a gate length direction of a channel region in the second active region.

21. (Currently Amended) A semiconductor device comprising:

a first MIS transistor; and

a second MIS transistor, wherein:

the first MIS transistor includes

a first gate insulating film formed on a first active region in a semiconductor substrate,

a first gate electrode including a second metal film formed on the first gate insulating film, and

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an insulating film formed, extending over side surfaces of the first gate electrode and upper surfaces of regions located in the first active region laterally outside the first gate electrode,

the second MIS transistor includes

a second gate insulating film formed on a second active region in the semiconductor substrate,

a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film, and

the insulating film formed, extending over side surfaces of the second gate electrode and upper surfaces of regions located in the second active region laterally outside the second gate electrode,

the first and second metal films are made of different metal materials,

the insulating film is not formed on any of upper surfaces of the first and second gate electrodes,

the conductive film is made of a silicon film, [[and]]

the semiconductor device further comprises a metal silicide film formed on the silicon film, and

the insulating film has a thickness smaller than that of the first gate electrode.

22. (Previously Presented) The semiconductor device of claim 21, wherein the first metal film has a thickness smaller than that of the second metal film.

23. (Previously Presented) The semiconductor device of claim 21, wherein

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the first and second metal films have different work functions.

24. (Cancelled)

25. (Previously Presented) The semiconductor device of claim 21, wherein the first and second gate insulating films are made of the same insulating material.

26. (Previously Presented) The semiconductor device of claim 21, wherein the first and second gate insulating films are made of different insulating materials.

27. (Currently Amended) The semiconductor device of claim 21, further comprising:
a first inner sidewall having an L-shaped cross-section formed on each of side surfaces of the first gate electrode, and
a second inner sidewall having an L-shaped cross-section formed on each of side surfaces of the second gate electrode,
wherein the insulating film is formed ~~above and~~ in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.

28. (Previously Presented) The semiconductor device of claim 21, wherein the insulating film is made of a silicon nitride film.

29. (Previously Presented) The semiconductor device of claim 21, further comprising:

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source/drain regions formed in the second active region laterally outside the second gate electrode,

wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.

30. (Previously Presented) The semiconductor device of claim 21, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.

31. (Previously Presented) A semiconductor device comprising:
a first MIS transistor; and
a second MIS transistor, wherein:
the first MIS transistor includes
a first gate insulating film formed on a first active region in a semiconductor substrate,
a first gate electrode including a second metal film formed on the first gate insulating film, and
an insulating film formed, extending over side surfaces of the first gate electrode and upper surfaces of regions located in the first active region laterally outside the first gate electrode,
the second MIS transistor includes
a second gate insulating film formed on a second active region in the semiconductor substrate,

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a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film, and

the insulating film formed, extending over side surfaces of the second gate electrode and upper surfaces of regions located in the second active region laterally outside the second gate electrode,

the first and second metal films are made of different metal materials,

the insulating film is not formed on any of upper surfaces of the first and second gate electrodes, and

the first and second gate insulating films are made of different insulating materials.

32. (Previously Presented) The semiconductor device of claim 31, wherein the first metal film has a thickness smaller than that of the second metal film.

33. (Previously Presented) The semiconductor device of claim 31, wherein the first and second metal films have different work functions.

34. (Previously Presented) The semiconductor device of claim 31, wherein the insulating film has a thickness smaller than that of the first gate electrode.

35. (Currently Amended) The semiconductor device of claim 31, further comprising:
a first inner sidewall having an L-shaped cross-section formed on each of side surfaces of the first gate electrode, and

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a second inner sidewall having an L-shaped cross-section formed on each of side surfaces of the second gate electrode,

wherein the insulating film is formed ~~above and~~ in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.

36. (Previously Presented) The semiconductor device of claim 31, wherein the insulating film is made of a silicon nitride film.

37. (Previously Presented) The semiconductor device of claim 31, further comprising:

source/drain regions formed in the second active region laterally outside the second gate electrode,

wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.

38. (Previously Presented) The semiconductor device of claim 31, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.

39. (Previously Presented) A semiconductor device comprising:

a first MIS transistor; and

a second MIS transistor, wherein:

the first MIS transistor includes

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a first gate insulating film formed on a first active region in a semiconductor substrate,

a first gate electrode including a second metal film formed on the first gate insulating film, and

an insulating film formed, extending over side surfaces of the first gate electrode and upper surfaces of regions located in the first active region laterally outside the first gate electrode,

the second MIS transistor includes

a second gate insulating film formed on a second active region in the semiconductor substrate,

a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film, and

the insulating film formed, extending over side surfaces of the second gate electrode and upper surfaces of regions located in the second active region laterally outside the second gate electrode,

the first and second metal films are made of different metal materials,

the insulating film is not formed on any of upper surfaces of the first and second gate electrodes, and

the insulating film is a stress insulating film which causes first stress in a gate length direction of a channel region in the first active region.

40. (Previously Presented) The semiconductor device of claim 39, wherein the first metal film has a thickness smaller than that of the second metal film.

41. (Previously Presented) The semiconductor device of claim 39, wherein the first and second metal films have different work functions.

42. (Previously Presented) The semiconductor device of claim 39, wherein the insulating film has a thickness smaller than that of the first gate electrode.

43. (Previously Presented) The semiconductor device of claim 39, wherein the conductive film is made of the second metal film.

44. (Previously Presented) The semiconductor device of claim 39, wherein:
the conductive film is made of a silicon film, and
the semiconductor device further comprises a metal silicide film formed on the silicon film.

45. (Previously Presented) The semiconductor device of claim 39, wherein the first and second gate insulating films are made of the same insulating material.

46. (Previously Presented) The semiconductor device of claim 39, wherein the first and second gate insulating films are made of different insulating materials.

47. (Currently Amended) The semiconductor device of claim 39, further comprising:

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a first inner sidewall having an L-shaped cross-section formed on each of side surfaces of the first gate electrode, and

a second inner sidewall having an L-shaped cross-section formed on each of side surfaces of the second gate electrode,

wherein the insulating film is formed ~~above and~~ in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.

48. (Previously Presented) The semiconductor device of claim 39, wherein the insulating film is made of a silicon nitride film.

49. (Previously Presented) The semiconductor device of claim 39, further comprising:

source/drain regions formed in the second active region laterally outside the second gate electrode,

wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.

50. (Previously Presented) The semiconductor device of claim 39, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.

REMARKS

Introduction

Claims 1-3, 5-11, 13-23 and 25-50 are pending, of which claims 1, 15, 21, 31 and 39 are independent.

Applicants note with appreciation the indication of allowance of claims 31-34, 36-46 and 48-50 and the indication of allowable subject matter in claims 4, 5, 8, 10, 11, 13, 16, 18, 24, 26, 28 and 29 if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1 and 15 have been amended to incorporate the allowable subject matter of original claim 4. Claim 21 has been amended to incorporate the allowable subject matter of original claim 24. Claims 9, 19, 27, 35 and 47 have been amended to correct informalities in the claim language and to more clearly define the claimed subject matter. Claims 4 and 24 have been cancelled. No new matter has been added.

Patentability under 35 U.S.C. § 112

Claims 9, 27, 35 and 47 were rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. Applicants submit that claims 9, 27, 35 and 47, as amended, meet the requirement under 35 U.S.C. § 112, second paragraph. As shown in, for example, FIG. 4A of the present disclosure, insulating film 27 is formed in contact with surfaces of the first and second inner sidewalls 19a and 19b which are bent in an L-shape. Thus, it is requested that the Examiner withdraw the rejection of claims 9, 27, 35 and 47 under 35 U.S.C. § 112, second paragraph.

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Patentability under 35 U.S.C. § 102

Claims 1-3, 6, 7, 14, 15, 17, 19-23 and 30 were rejected under 35 U.S.C. § 102(e) as being anticipated by Hou et al. (US 7,812,414).

These rejections are traversed for at least the following reasons.

Applicants submit that since claims 1, 15 and 21 have been amended to incorporate the allowable subject matter of original claims 4 and 24, respectively, claims 1, 15 and 21 and all claims dependent thereon are patentable over the cited reference. Thus, it is requested that the Examiner withdraw the rejections of the claims under 35 U.S.C. § 102.

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CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Date: August 19, 2011

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Electronic Acknowledgement Receipt	
EFS ID:	10777870
Application Number:	12629508
International Application Number:	
Confirmation Number:	7931
Title of Invention:	SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Yoshihiro SATO
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Filer:	Michael E. Fogarty/3328/Matilda Mason
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Time Stamp:	17:29:14
Application Type:	Utility under 35 USC 111(a)

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Submitted with Payment	no
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File Listing:

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		085393-0059Amendment2.pdf	183506 a9ac57df48b4cf00c9cd6a116218289a52498afe	yes	19
Multipart Description/PDF files in .zip description					
	Document Description		Start	End	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Claims		2	17	
	Applicant Arguments/Remarks Made in an Amendment		18	19	
Warnings:					
Information:					
Total Files Size (in bytes):			183506		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/629,508		Filing Date 12/02/2009		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))			If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).							
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL				
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			(Column 3)		SMALL ENTITY OR OTHER THAN SMALL ENTITY		
AMENDMENT	08/19/2011	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 47	Minus	** 20	= 27	X \$ =		OR	X \$52=	1404
	Independent (37 CFR 1.16(h))	* 5	Minus	***3	= 2	X \$ =		OR	X \$220=	440
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	1844
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".</p> <p>*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".</p> <p>The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p>										

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Legal Instrument Examiner:
/LINDA WISE/



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/629,508	12/02/2009	Yoshihiro SATO	085393-0059	7931
<div>7590 09/26/2011 McDERMOTT WILL & EMERY LLP 600 13th Street, N.W. Washington, DC 20005-3096</div>			<div>EXAMINER PRENTY, MARK V</div>	
			<div>ART UNIT 2822</div>	<div>PAPER NUMBER</div>
			<div>MAIL DATE 09/26/2011</div>	<div>DELIVERY MODE PAPER</div>

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/629,508	SATO ET AL.	
	Examiner	Art Unit	
	MARK PRENTY	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 19 August 2011.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5) ☒ Claim(s) 1-3,5-11,13-23 and 25-50 is/are pending in the application.

5a) Of the above claim(s) ____ is/are withdrawn from consideration.

6) ☒ Claim(s) 1-3,5-11,13-23,25-30 and 39-50 is/are allowed.

7) ☒ Claim(s) 31-33 and 38 is/are rejected.

8) ☒ Claim(s) 34-37 is/are objected to.

9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

10) ☐ The specification is objected to by the Examiner.

11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. ____.
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)	5) ☐ Notice of Informal Patent Application
Paper No(s)/Mail Date ____.	6) ☐ Other: ____.

This Office Action is in response to the amendment filed on August 19, 2011.

Claims 31-33 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 7,812,414 to Hou et al. (Hou, already of record) together with newly cited United States Patent Application Publication 2007/0284670 to Yamamoto et al. (Yamamoto).

As to independent claim 31, Hou discloses a semiconductor device (see the entire patent, including the Fig. 11 disclosure) comprising: a first (right-side) MIS transistor; and a second (left-side) MIS transistor, wherein: the first MIS transistor includes a first gate insulating film 224 formed on a first active region 200 in a semiconductor substrate 20, a first gate electrode including a second metal film 248 formed on the first gate insulating film, and an insulating film 42 formed, extending over side surfaces of the first gate electrode and upper surfaces of regions located in the first active region laterally outside the first gate electrode, the second MIS transistor includes a second gate insulating film 124 on a second active region 100 in the semiconductor substrate, a second gate electrode including a first metal film 126 formed on the second gate insulating film and a conductive film 128 formed on the first metal film, the insulating film 42 formed, extending over side surfaces of the second gate electrode and upper surfaces of regions located in the second active region laterally outside the second gate electrode, the first and second metal films 126 and 248 are made of different metal materials, the insulating film 42 is not formed on any of upper surfaces of the first and second gate electrodes, and the first and second gate insulating films 224 and 124 are made of the same insulating material.

The difference between claim 31 and Hou is claim 31's first and second gate insulating films are made of different insulating materials (Hou's first and second gate insulating films are made of the same insulating material).

Yamamoto teaches that the gate insulating films of complementary MIS transistors can be formed of the same insulating material or of different insulating materials (see the entire reference, including paragraph [0042] bridging pages 3-4).

It would have been obvious to one skilled in the art to form Hou's first and second gate insulating films 224 and 124 (corresponding to Hou's complementary first and second MIS transistors, respectively) of different insulating materials because Yamamoto teaches that the gate insulating films of complementary MIS transistors can be formed of the same insulating material or of different insulating materials.

Claim 31 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Hou together with Yamamoto.

As to dependent claim 32, Hou's first metal film 126 has a thickness smaller than that of the second metal film 248.

Claim 32 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Hou together with Yamamoto.

As to dependent claim 33, Hou's first and second metal films 126 and 248 have different work functions.

Claim 33 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Hou together with Yamamoto.

As to dependent claim 38, the Hou/Yamamoto device's first and second gate insulating films 224 and 124 include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more (see Hou at column 4, lines 27-33, and Yamamoto at paragraph [0042]).

Claim 38 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Hou together with Yamamoto.

Claims 34-37 are objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1-3, 5-11, 13-23, 25-30 and 39-50 are allowable over the prior art of record.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

/MARK PRENTY/
Primary Examiner, Art Unit 2822

Notice of References Cited	Application/Control No. 12/629,508	Applicant(s)/Patent Under Reexamination SATO ET AL.	
	Examiner MARK PRENTY	Art Unit 2822	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2007/0284670	12-2007	Yamamoto et al.	257/369
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Docket No.: 085393-0059

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Yoshihiro SATO, et al.	:	Confirmation Number: 7931
	:	
Application No.: 12/629,508	:	Group Art Unit: 2822
	:	
Filed: December 02, 2009	:	Examiner: PRENTY, Mark V.
	:	
For: SEMICONDUCTOR DEVICE (as amended)	:	

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated September 26, 2011, wherein a three-month shortened statutory period for response is set to expire on December 26, 2011, Applicants respectfully request reconsideration of the above-identified application in view of the following amendments and remarks.

DM_US 36974833-1.085393.0059

Application No.: 12/629,508

AMENDMENT TO THE SPECIFICATION

Please amend the title as follows:

~~SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME~~

AMENDMENT TO THE CLAIMS

The following claim listing replaces all prior listings and versions of the claims:

LISTING OF CLAIMS

1. (Currently Amended) A semiconductor device comprising:
a first MIS transistor; and
a second MIS transistor, wherein:
the first MIS transistor includes:
a first gate insulating film formed on a first active region in a
semiconductor substrate, and including a first high-k film made of oxide
containing hafnium and silicon;
a first gate electrode includes a second metal film formed on the first gate
insulating film;
first sidewall spacers formed on side surfaces of the first gate electrode,
the first sidewall spacers being insulative; [[,]] and
~~an insulating~~ a silicon nitride film formed, extending over the side surfaces
of the first gate electrode on which the first sidewall spacers are formed and upper
surfaces of regions located in the first active region laterally outside the first gate
~~electrode~~ sidewall spacers,
the second MIS transistor includes:
a second gate insulating film formed on a second active region in the
semiconductor substrate, and including a second high-k film made of oxide
containing hafnium and silicon;
a second gate electrode including a first metal film formed on the second

gate insulating film and a conductive film formed on the first metal film;

second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative; [[,]]

the silicon nitride insulating film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second ~~gate electrode~~ sidewall spacers; [[,]] and

source/drain regions formed in the second active region laterally outside the second ~~gate electrode~~ sidewall spacers,

the first and second metal films are made of different metal materials,

the silicon nitride insulating film is not formed on any of upper surfaces of the first and second gate electrodes,

the source/drain regions include a silicon mixed crystal layer which is formed in trenches provided in the second active region, and causes first stress in a gate length direction of a channel region in the second active region, and

the silicon nitride insulating film has a thickness smaller than that of the first gate electrode.

2. (Original) The semiconductor device of claim 1, wherein
the first metal film has a thickness smaller than that of the second metal film.

3. (Original) The semiconductor device of claim 1, wherein
the first and second metal films have different work functions.

4. (Cancelled)

5. (Original) The semiconductor device of claim 1, wherein the conductive film is made of the second metal film.

6. (Original) The semiconductor device of claim 1, wherein the conductive film is made of a silicon film, and the semiconductor device further comprises a metal silicide film formed on the silicon film.

7. (Original) The semiconductor device of claim 1, wherein the first and second gate insulating films are made of the same insulating material.

8. (Original) The semiconductor device of claim 1, wherein the first and second gate insulating films are made of different insulating materials.

9. (Currently Amended) The semiconductor device of claim 1, ~~further comprising~~ wherein:

each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section ~~formed on each of side surfaces of the first gate electrode~~, and

each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section ~~formed on each of side surfaces of the second gate electrode~~,

~~wherein~~

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the silicon nitride ~~insulating~~ film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.

10. (Currently Amended) The semiconductor device of claim 1, wherein the silicon nitride ~~insulating~~ film is a stress-insulating film which causes second stress in a gate length direction of a channel region in the first active region.

11. (Currently Amended) The semiconductor device of claim 10, wherein:
the first MIS transistor is an n-type MIS transistor,
the ~~insulating film is made of a silicon nitride film~~, and
the second stress is tensile stress.

12. (Cancelled)

13. (Previously Presented) The semiconductor device of claim 1, wherein
the second MIS transistor is a p-type MIS transistor,
the silicon mixed crystal layer is made of a SiGe layer, and
the first stress is compressive stress.

14-20. (Cancelled)

21. (Currently Amended) A semiconductor device comprising:
a first MIS transistor; and

a second MIS transistor, wherein:

the first MIS transistor includes:

a first gate insulating film formed on a first active region in a semiconductor substrate; [[,]]

a first gate electrode including a second metal film formed on the first gate insulating film; [[,]]

first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and

a silicon nitride an-insulating film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first gate electrode sidewall spacers,

the second MIS transistor includes:

a second gate insulating film formed on a second active region in the semiconductor substrate,

a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film; [[,]]

second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative; and

the silicon nitride insulating film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second gate electrode sidewall spacers,

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the first and second metal films are made of different metal materials,
the ~~silicon nitride insulating~~ film is not formed on any of upper surfaces of the first and second gate electrodes,
the conductive film is made of a silicon film,
the semiconductor device further comprises a metal silicide film formed on the silicon film, and
the ~~silicon nitride insulating~~ film has a thickness smaller than that of the first gate electrode.

22. (Previously Presented) The semiconductor device of claim 21, wherein the first metal film has a thickness smaller than that of the second metal film.

23. (Previously Presented) The semiconductor device of claim 21, wherein the first and second metal films have different work functions.

24. (Cancelled)

25. (Previously Presented) The semiconductor device of claim 21, wherein the first and second gate insulating films are made of the same insulating material.

26. (Previously Presented) The semiconductor device of claim 21, wherein the first and second gate insulating films are made of different insulating materials.

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27. (Currently Amended) The semiconductor device of claim 21, ~~further comprising~~
wherein:

each of the first sidewall spacers is made of a first inner sidewall having an L-shaped
cross-section formed on each of side surfaces of the first gate electrode, and

each of the second sidewall spacers is made of a second inner sidewall having an L-
shaped cross-section formed on each of side surfaces of the second gate electrode, and

wherein the silicon nitride insulating film is formed in contact with surfaces of the first
and second inner sidewalls which are bent in an L-shape.

28. (Cancelled)

29. (Currently Amended) The semiconductor device of claim 21, further comprising:
source/drain regions formed in the second active region laterally outside the second gate
electrode sidewall spacers,

wherein the source/drain regions include a SiGe layer which is formed in trenches
provided in the second active region.

30. (Previously Presented) The semiconductor device of claim 21, wherein
the first and second gate insulating films include a high-k film made of a metal oxide
having a relative dielectric constant of 10 or more.

31. (Currently Amended) A semiconductor device comprising:
a first MIS transistor; and

a second MIS transistor, wherein:

the first MIS transistor includes:

a first gate insulating film formed on a first active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon;

a first gate electrode including a second metal film formed on the first gate insulating film; [[,]]

first sidewall spacers formed on side surfaces of the first gate electrode,
the first sidewall spacers being insulative; and

a silicon nitride ~~an insulating~~ film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first gate electrode sidewall spacers,

the second MIS transistor includes:

a second gate insulating film formed on a second active region in the semiconductor substrate, and including a second high-k film made of oxide containing hafnium and silicon;

a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film; [[,]]

second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative; and

the silicon nitride ~~insulating~~ film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and

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upper surfaces of regions located in the second active region laterally outside the second ~~gate electrode~~ sidewall spacers,
the first and second metal films are made of different metal materials,
the silicon nitride ~~insulating~~ film is not formed on any of upper surfaces of the first and second gate electrodes, and
the first metal film is made of titanium nitride.
~~the first and second gate insulating films are made of different insulating materials.~~

32. (Previously Presented) The semiconductor device of claim 31, wherein
the first metal film has a thickness smaller than that of the second metal film.

33. (Previously Presented) The semiconductor device of claim 31, wherein
the first and second metal films have different work functions.

34. (Currently Amended) The semiconductor device of claim 31, wherein
the silicon nitride ~~insulating~~ film has a thickness smaller than that of the first gate electrode.

35. (Currently Amended) The semiconductor device of claim 31, ~~further comprising~~
wherein:
each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section ~~formed on each of side surfaces of the first gate electrode~~, and

each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section formed on each of side surfaces of the second gate electrode, and
~~wherein~~ the silicon nitride insulating film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.

36. (Cancelled)

37. (Currently Amended) The semiconductor device of claim 31, further comprising:
source/drain regions formed in the second active region laterally outside the second gate electrode sidewall spacers,

wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.

38. (Cancelled)

39. (Currently Amended) A semiconductor device comprising:

a first MIS transistor; and

a second MIS transistor, wherein:

the first MIS transistor includes:

a first gate insulating film formed on a first active region in a semiconductor substrate; [[,]]

a first gate electrode including a second metal film formed on the first gate insulating film; [[,]]

first sidewall spacers formed on side surfaces of the first gate electrode,
the first sidewall spacers being insulative; and
a silicon nitride an-insulating film formed, extending over side the surfaces of the
first gate electrode on which the first sidewall spacers are formed and upper
surfaces of regions located in the first active region laterally outside the first gate
electrode sidewall spacers,

the second MIS transistor includes:

a second gate insulating film formed on a second active region in the
semiconductor substrate; [[,]]

a second gate electrode including a first metal film formed on the second
gate insulating film and a conductive film formed on the first metal film; [[,]]

second sidewall spacers formed on side surfaces of the second gate
electrode, the second sidewall spacers being insulative; and

the silicon nitride insulating film formed, extending over the side surfaces
of the second gate electrode on which the second sidewall spacers are formed and
upper surfaces of regions located in the second active region laterally outside the
second gate electrode sidewall spacers,

the first and second metal films are made of different metal materials,

the silicon nitride insulating film is not formed on any of upper surfaces of the first and
second gate electrodes, and

the silicon nitride insulating film is a stress-insulating film which causes first stress in a
gate length direction of a channel region in the first active region.

Application No.: 12/629,508

40. (Previously Presented) The semiconductor device of claim 39, wherein the first metal film has a thickness smaller than that of the second metal film.
41. (Previously Presented) The semiconductor device of claim 39, wherein the first and second metal films have different work functions.
42. (Currently Amended) The semiconductor device of claim 39, wherein the silicon nitride ~~insulating~~ film has a thickness smaller than that of the first gate electrode.
43. (Previously Presented) The semiconductor device of claim 39, wherein the conductive film is made of the second metal film.
44. (Previously Presented) The semiconductor device of claim 39, wherein:
the conductive film is made of a silicon film, and
the semiconductor device further comprises a metal silicide film formed on the silicon film.
45. (Previously Presented) The semiconductor device of claim 39, wherein the first and second gate insulating films are made of the same insulating material.
46. (Previously Presented) The semiconductor device of claim 39, wherein the first and second gate insulating films are made of different insulating materials.

47. (Currently Amended) The semiconductor device of claim 39, ~~further comprising~~
wherein:

each of the first sidewall spacers is made of a first inner sidewall having an L-shaped
cross-section ~~formed on each of side surfaces of the first gate electrode~~, and

each of the second sidewall spacers is made of a second inner sidewall having an L-
shaped cross-section ~~formed on each of side surfaces of the second gate electrode~~,

~~wherein~~ the silicon nitride insulating film is formed in contact with surfaces of the first
and second inner sidewalls which are bent in an L-shape.

48. (Cancelled)

49. (Currently Amended) The semiconductor device of claim 39, further comprising:
source/drain regions formed in the second active region laterally outside the second ~~gate~~
~~electrode~~ sidewall spacers,

wherein the source/drain regions include a SiGe layer which is formed in trenches
provided in the second active region.

50. (Previously Presented) The semiconductor device of claim 39, wherein
the first and second gate insulating films include a high-k film made of a metal oxide
having a relative dielectric constant of 10 or more.

Application No.: 12/629,508

51. (New) The semiconductor device of claim 1, wherein the first high- film further contains titanium.

52. (New) The semiconductor device of claim 31, wherein the first high- film further contains titanium.

REMARKS

Introduction

Claims 1-3, 5-11, 13, 21-23, 25-27, 29-35, 37, 39-47 and 49-52 are pending, of which claims 1, 21, 31 and 39 are independent.

Applicants note with appreciation the indication of allowance of claims 1-3, 5-11, 13-23, 25-30 and 39-50 and the indication of allowable subject matter of claims 34-37 if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1, 9-11, 21, 27, 29, 31, 34, 37, 39, 42, 47 and 49 have been amended to correct informalities in the claim language and to more clearly define the present subject matter. The subject matter of allowable claim 36 has been incorporated into claim 31. Claims 14-20, 28, 36, 38 and 48 have been cancelled without prejudice. New claims 51 and 52 have been added. Support for the amendments and the new claims is found, for example, in the original claims and paragraphs [0085], [0121], [0122] and [0197] of the specification as published. The title of the disclosure has also been amended. No new matter has been added.

Patentability under 35 U.S.C. § 103

Claims 31-33 and 38 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hou et al. (US 7,812,414). This rejection is traversed for at least the following reasons.

Applicants respectfully submit that since claim 31 has been amended to incorporate the allowable subject matter of original claim 36, claim 31 and all claims dependent thereon are patentable over the cited reference. Thus, it is requested that the Examiner withdraw the rejection of the claims under 35 U.S.C. § 103.

Application No.: 12/629,508

New claims

Since new claims 51 and 52 depend upon claims 1 and 31, respectively, claims 51 and 52 are patentable over the cited reference.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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Date: December 6, 2011

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as our correspondence address.**

Electronic Acknowledgement Receipt	
EFS ID:	11557233
Application Number:	12629508
International Application Number:	
Confirmation Number:	7931
Title of Invention:	SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Yoshihiro SATO
Correspondence Address:	McDERMOTT WILL & EMERY LLP - 600 13th Street, N.W. - Washington DC 20005-3096 US 2027568000 -
Filer:	Michael E. Fogarty/3328/Matilda Mason
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0059
Receipt Date:	06-DEC-2011
Filing Date:	02-DEC-2009
Time Stamp:	20:07:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)				
1		085393-0059Amendment3.pdf	233242 80ef6db9210749b2ab6c0f596467a1da312a782d	yes	18				
	Multipart Description/PDF files in .zip description								
	Document Description		Start	End					
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1					
	Specification		2	2					
	Claims		3	16					
	Applicant Arguments/Remarks Made in an Amendment		17	18					
Warnings:									
Information:									
Total Files Size (in bytes):			233242						
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>									



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/629,508	12/02/2009	Yoshihiro SATO	085393-0059	7931
<div>7590 McDERMOTT WILL & EMERY LLP 600 13th Street, N.W. Washington, DC 20005-3096</div>			<div>EXAMINER PRENTY, MARK V</div>	
			<div>ART UNIT 2822</div>	<div>PAPER NUMBER</div>
			<div>MAIL DATE 12/15/2011</div>	<div>DELIVERY MODE PAPER</div>

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/629,508	SATO ET AL.	
	Examiner	Art Unit	
	MARK PRENTY	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 December 2011.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 5) ☒ Claim(s) 1-3,5-11,13,21-23,25-27,29-35,37,39-47 and 49-52 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☒ Claim(s) 1-3,5-7,9-11,13,21-23,25-27,29-35 and 37 is/are allowed.
- 7) ☒ Claim(s) 8,51 and 52 is/are rejected.
- 8) ☒ Claim(s) 39-47 and 49-52 is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 12) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☐ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____. |
| 3) ☐ Information Disclosure Statement(s) (PTO/SB/08) | 5) ☐ Notice of Informal Patent Application |
| Paper No(s)/Mail Date ____. | 6) ☐ Other: ____. |

This Office Action is in response to the amendment filed on December 6, 2011.

Independent claim 39 is objected to because "side the surfaces" (line 11) should be "the side surfaces." Correction is required. Claims 40-47, 49 and 50 depend on claim 39 and are thus similarly objected to.

Claims 51 and 52 are objected to because "the first high- film" should be "the first high-k film."

Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Dependent claim 8, which depends on independent claim 1, is incorrect in reciting "the first and second gate insulating films are made of different insulating materials" because independent claim 1 recites that the first and second gate insulating films comprise a high-k film made of oxide containing hafnium and silicon. Claim 8 should be cancelled.

Claims 51 and 52 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Specifically, the specification (including page 52, lines 18-23) does not describe claims 51 and 52 (which depend on claims 1 and 31, respectively), wherein the first gate insulating film comprises a high-k film made of oxide containing hafnium, silicon and titanium. Claims 51 and 52 should be cancelled.

Claims 1-3, 5-7, 9-11, 13, 21-23, 25-27, 29-35 and 37 are allowable over the prior art of record.

Claims 39-47, 49 and 50 would be allowable over the prior art of record if independent claim 39 is corrected (see above).

Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

/MARK PRENTY/
Primary Examiner, Art Unit 2822

Docket No.: 085393-0059

PATENT

Reply Under 37 CFR 1.116 - Expedited Procedure - Technology Center 2800

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yoshihiro SATO, et al.

Application No.: 12/629,508

Customer No.: 53080

Filed: December 02, 2009

Confirmation No.: 7931

Group Art Unit: 2822

Examiner: PRENTY, Mark V.

Title: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

AMENDMENT UNDER 37 CFR 1.116

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the final Office Action dated December 15, 2011, wherein a three-month shortened statutory period for response is set to expire on March 15, 2012, Applicants respectfully request reconsideration of the above-identified application in view of the following amendments and remarks.

DM_US 32323494-1.085393.0059

AMENDMENT TO THE CLAIMS

The following claim listing replaces all prior listings and versions of the claims:

LISTING OF CLAIMS

1. (Previously Presented) A semiconductor device comprising:
a first MIS transistor; and
a second MIS transistor, wherein:
the first MIS transistor includes:
a first gate insulating film formed on a first active region in a
semiconductor substrate, and including a first high-k film made of oxide
containing hafnium and silicon;
a first gate electrode includes a second metal film formed on the first gate
insulating film;
first sidewall spacers formed on side surfaces of the first gate electrode,
the first sidewall spacers being insulative; and
a silicon nitride film formed, extending over the side surfaces
of the first gate electrode on which the first sidewall spacers are formed and upper
surfaces of regions located in the first active region laterally outside the first sidewall
spacers,
the second MIS transistor includes:
a second gate insulating film formed on a second active region in the
semiconductor substrate, and including a second high-k film made of oxide
containing hafnium and silicon;
a second gate electrode including a first metal film formed on the second

- gate insulating film and a conductive film formed on the first metal film;
- second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative;
- the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers; and
- source/drain regions formed in the second active region laterally outside the second sidewall spacers,
- the first and second metal films are made of different metal materials,
- the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes,
- the source/drain regions include a silicon mixed crystal layer which is formed in trenches provided in the second active region, and causes first stress in a gate length direction of a channel region in the second active region, and
- the silicon nitride film has a thickness smaller than that of the first gate electrode.
2. (Original) The semiconductor device of claim 1, wherein the first metal film has a thickness smaller than that of the second metal film.
3. (Original) The semiconductor device of claim 1, wherein the first and second metal films have different work functions.

4. (Canceled)

5. (Original) The semiconductor device of claim 1, wherein the conductive film is made of the second metal film.

6. (Original) The semiconductor device of claim 1, wherein the conductive film is made of a silicon film, and the semiconductor device further comprises a metal silicide film formed on the silicon film.

7. (Original) The semiconductor device of claim 1, wherein the first and second gate insulating films are made of the same insulating material.

8. (Canceled)

9. (Previously Presented) The semiconductor device of claim 1, wherein:
each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and
each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section, the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.

10. (Previously Presented) The semiconductor device of claim 1, wherein

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the silicon nitride film causes second stress in a gate length direction of a channel region in the first active region.

11. (Previously Presented) The semiconductor device of claim 10, wherein:
the first MIS transistor is an n-type MIS transistor, and
the second stress is tensile stress.

12. (Canceled)

13. (Previously Presented) The semiconductor device of claim 1, wherein
the second MIS transistor is a p-type MIS transistor,
the silicon mixed crystal layer is made of a SiGe layer, and
the first stress is compressive stress.

14-20. (Canceled)

21. (Previously Presented) A semiconductor device comprising:
a first MIS transistor; and
a second MIS transistor, wherein:
the first MIS transistor includes:
a first gate insulating film formed on a first active region in a
semiconductor substrate;

a first gate electrode including a second metal film formed on the first gate insulating film;

first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and

a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,

the second MIS transistor includes:

a second gate insulating film formed on a second active region in the semiconductor substrate,

a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;

second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative; and

the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers,

the first and second metal films are made of different metal materials,

the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes,

the conductive film is made of a silicon film,

the semiconductor device further comprises a metal silicide film formed on the silicon film, and

the silicon nitride film has a thickness smaller than that of the first gate electrode.

22. (Previously Presented) The semiconductor device of claim 21, wherein the first metal film has a thickness smaller than that of the second metal film.

23. (Previously Presented) The semiconductor device of claim 21, wherein the first and second metal films have different work functions.

24. (Cancelled)

25. (Previously Presented) The semiconductor device of claim 21, wherein the first and second gate insulating films are made of the same insulating material.

26. (Previously Presented) The semiconductor device of claim 21, wherein the first and second gate insulating films are made of different insulating materials.

27. (Previously Presented) The semiconductor device of claim 21, wherein:
each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and

each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section, and

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the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.

28. (Canceled)

29. (Previously Presented) The semiconductor device of claim 21, further comprising:

source/drain regions formed in the second active region laterally outside the second sidewall spacers,

wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.

30. (Previously Presented) The semiconductor device of claim 21, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.

31. (Previously Presented) A semiconductor device comprising:

a first MIS transistor; and

a second MIS transistor, wherein:

the first MIS transistor includes:

a first gate insulating film formed on a first active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon;

a first gate electrode including a second metal film formed on the first gate insulating film;

first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and

a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,

the second MIS transistor includes:

a second gate insulating film formed on a second active region in the semiconductor substrate, and including a second high-k film made of oxide containing hafnium and silicon;

a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;

second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative; and

the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers,

the first and second metal films are made of different metal materials,

the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes, and

the first metal film is made of titanium nitride.

32. (Previously Presented) The semiconductor device of claim 31, wherein the first metal film has a thickness smaller than that of the second metal film.

33. (Previously Presented) The semiconductor device of claim 31, wherein the first and second metal films have different work functions.

34. (Previously Presented) The semiconductor device of claim 31, wherein the silicon nitride film has a thickness smaller than that of the first gate electrode.

35. (Previously Presented) The semiconductor device of claim 31, wherein:
each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and

each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section, and

the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.

36. (Canceled)

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37. (Previously Presented) The semiconductor device of claim 31, further comprising:

source/drain regions formed in the second active region laterally outside the second sidewall spacers,

wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.

38. (Canceled)

39. (Currently Amended) A semiconductor device comprising:

a first MIS transistor; and

a second MIS transistor, wherein:

the first MIS transistor includes:

a first gate insulating film formed on a first active region in a semiconductor substrate;

a first gate electrode including a second metal film formed on the first gate insulating film;

first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and

a silicon nitride film formed, extending over ~~side the surfaces~~ the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,

the second MIS transistor includes:

a second gate insulating film formed on a second active region in the semiconductor substrate;

a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;

second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative; and

the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers,

the first and second metal films are made of different metal materials,

the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes, and

the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region.

40. (Previously Presented) The semiconductor device of claim 39, wherein the first metal film has a thickness smaller than that of the second metal film.

41. (Previously Presented) The semiconductor device of claim 39, wherein the first and second metal films have different work functions.

42. (Previously Presented) The semiconductor device of claim 39, wherein the silicon nitride film has a thickness smaller than that of the first gate electrode.

43. (Previously Presented) The semiconductor device of claim 39, wherein the conductive film is made of the second metal film.

44. (Previously Presented) The semiconductor device of claim 39, wherein:
the conductive film is made of a silicon film, and
the semiconductor device further comprises a metal silicide film formed on the silicon film.

45. (Previously Presented) The semiconductor device of claim 39, wherein the first and second gate insulating films are made of the same insulating material.

46. (Previously Presented) The semiconductor device of claim 39, wherein the first and second gate insulating films are made of different insulating materials.

47. (Previously Presented) The semiconductor device of claim 39, wherein:
each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and
each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section,

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the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.

48. (Canceled)

49. (Previously Presented) The semiconductor device of claim 39, further comprising:

source/drain regions formed in the second active region laterally outside the second sidewall spacers,

wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.

50. (Previously Presented) The semiconductor device of claim 39, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.

51. (Canceled)

52. (Canceled)

REMARKS

Introduction

Claims 1-3, 5-11, 13, 21-23, 25-27, 29-35, 37, 39-47 and 49-52 were pending, of which claims 1, 21, 31 and 39 are independent.

Applicants note with appreciation the indication of allowance of claims 1-3, 5-7, 9-11, 13, 21-23, 25-27, 29-35 and 37, and the indication of allowable subject matter of claims 39-47 and 49-52.

Claim 39 has been amended to correct informalities in the claim language. Claims 8, 51 and 52 have been cancelled without prejudice. No new matter has been added.

Rejections under 35 U.S.C. § 112

Claim 8 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Although Applicants disagree with the Examiner's assertion, solely in order to expedite the prosecution of this application, claim 8 has been cancelled, thereby rendering this rejection moot.

Claims 51 and 52 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Although Applicants disagree with the Examiner's assertion, solely in order to expedite the prosecution of this application, claims 51 and 52 have been cancelled, thereby rendering this rejection moot.

12/629,508

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Takashi Saito
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Facsimile: 202.756.8087
Date: March 13, 2012

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as our correspondence address.**

Electronic Acknowledgement Receipt	
EFS ID:	12295466
Application Number:	12629508
International Application Number:	
Confirmation Number:	7931
Title of Invention:	SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Yoshihiro SATO
Correspondence Address:	McDERMOTT WILL & EMERY LLP - 600 13th Street, N.W. - Washington DC 20005-3096 US 2027568000 -
Filer:	Michael E. Fogarty/Lynn Cruz
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Attorney Docket Number:	085393-0059
Receipt Date:	13-MAR-2012
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Application Type:	Utility under 35 USC 111(a)

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File Listing:

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		085393_0059_AFAmendment.pdf	101952 e02a00760f64774f7d259a1507ed9c9a9135be1	yes	16
Multipart Description/PDF files in .zip description					
	Document Description		Start	End	
	Amendment After Final		1	1	
	Claims		2	14	
	Applicant Arguments/Remarks Made in an Amendment		15	16	
Warnings:					
Information:					
Total Files Size (in bytes):			101952		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/629,508	Filing Date 12/02/2009	☐ To be Mailed
APPLICATION AS FILED – PART I							
(Column 1)		(Column 2)		SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	
APPLICATION AS AMENDED – PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY OR OTHER THAN SMALL ENTITY	
AMENDMENT	03/13/2012	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 35	Minus	** 47	= 0	X \$ =	OR X \$60= 0
	Independent (37 CFR 1.16(h))	* 4	Minus	***5	= 0	X \$ =	OR X \$250= 0
☐ Application Size Fee (37 CFR 1.16(s))							
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
						TOTAL ADD'L FEE	OR TOTAL ADD'L FEE 0
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY OR OTHER THAN SMALL ENTITY	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =	OR X \$ =
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =	OR X \$ =
☐ Application Size Fee (37 CFR 1.16(s))							
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
						TOTAL ADD'L FEE	OR TOTAL ADD'L FEE
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".</p> <p>*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".</p> <p>The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p>							

Legal Instrument Examiner:
/DOROTHY BELL/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 03/20/2012
McDERMOTT WILL & EMERY LLP
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER

PRENTY, MARK V

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 03/20/2012

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/629,508	12/02/2009	Yoshihiro SATO	085393-0059	7931

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1740	\$300	\$0	\$2040	06/20/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 03/20/2012
McDERMOTT WILL & EMERY LLP
600 13th Street, N.W.
Washington, DC 20005-3096

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/629,508	12/02/2009	Yoshihiro SATO	085393-0059	7931

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1740	\$300	\$0	\$2040	06/20/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
PRENTY, MARK V	2822	257-289000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/629,508	12/02/2009	Yoshihiro SATO	085393-0059	7931

7590 McDERMOTT WILL & EMERY LLP 600 13th Street, N.W. Washington, DC 20005-3096	03/20/2012
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EXAMINER PRENTY, MARK V

ART UNIT 2822	PAPER NUMBER
------------------	--------------

DATE MAILED: 03/20/2012

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 19 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 19 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/629,508	SATO ET AL.	
	Examiner	Art Unit	
	MARK PRENTY	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed on March 13, 2012.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-3,5-7,9-11,13,21-23,25-27,29-35,37,39-47,49 and 50.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
(b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____ 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____. 7. ☐ Examiner's Amendment/Comment 8. ☐ Examiner's Statement of Reasons for Allowance 9. ☐ Other _____.
--	--

/MARK PRENTY/ Primary Examiner, Art Unit 2822	
--	--

Receipt date: 03/13/2012

12629508 - GAU: 2822

OK TO ENTER: /M.P./ (03/14/2012)

Docket No.: 085393-0059

PATENT

Reply Under 37 CFR 1.116 - Expedited Procedure - Technology Center 2800

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yoshihiro SATO, et al.

Application No.: 12/629,508

Customer No.: 53080

Filed: December 02, 2009

Confirmation No.: 7931

Group Art Unit: 2822

Examiner: PRENTY, Mark V.

Title: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

AMENDMENT UNDER 37 CFR 1.116

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the final Office Action dated December 15, 2011, wherein a three-month shortened statutory period for response is set to expire on March 15, 2012, Applicants respectfully request reconsideration of the above-identified application in view of the following amendments and remarks.

DM_US 32323494-1.085393.0059

Search Notes 	Application/Control No. 12629508	Applicant(s)/Patent Under Reexamination SATO ET AL.
	Examiner MARK PRENTY	Art Unit 2822

SEARCHED			
Class	Subclass	Date	Examiner
update	all	3/14/12	mp

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
257	369, 407, 412, 413	3/14/12	mp

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<i>Index of Claims</i> 	Application/Control No. 12629508	Applicant(s)/Patent Under Reexamination SATO ET AL.
	Examiner MARK PRENTY	Art Unit 2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47									
CLAIM		DATE							
Final	Original	03/14/2012							
	1	=							
	2	=							
	3	=							
	4	-							
	5	=							
	6	=							
	7	=							
	8	-							
	9	=							
	10	=							
	11	=							
	12	-							
	13	=							
	14	-							
	15	-							
	16	-							
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	22	=							
	23	=							
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	25	=							
	26	=							
	27	=							
	28	-							
	29	=							
	30	=							
	31	=							
	32	=							
	33	=							
	34	=							
	35	=							
	36	-							

<p align="center"><i>Index of Claims</i></p> 	Application/Control No. 12629508	Applicant(s)/Patent Under Reexamination SATO ET AL.
	Examiner MARK PRENTY	Art Unit 2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	03/14/2012								
	37	=								
	38	-								
	39	=								
	40	=								
	41	=								
	42	=								
	43	=								
	44	=								
	45	=								
	46	=								
	47	=								
	48	-								
	49	=								
	50	=								
	51	-								
	52	-								

Issue Classification 	Application/Control No. 12629508	Applicant(s)/Patent Under Reexamination SATO ET AL.
	Examiner MARK PRENTY	Art Unit 2822

ORIGINAL						INTERNATIONAL CLASSIFICATION												
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED							
257		369				H	0	1	L	21 / 70 (2006.01.01)								
CROSS REFERENCE(S)																		
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																	
257	407	412	413															

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original

NONE		Total Claims Allowed:	
		35	
(Assistant Examiner)	(Date)		
/MARK PRENTY/ Primary Examiner. Art Unit 2822	3/14/12	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5C



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/629,508	12/02/2009	2822	3038	085393-0059	20	2

CONFIRMATION NO. 7931

CORRECTED FILING RECEIPT

McDERMOTT WILL & EMERY LLP
600 13th Street, N.W.
Washington, DC 20005-3096



Date Mailed: 04/25/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Yoshihiro SATO, Hyogo, JAPAN;
Hisashi Ogawa, Osaka, JAPAN;

Assignment For Published Patent Application

PANASONIC CORPORATION, Osaka, JAPAN

Power of Attorney: The patent practitioners associated with Customer Number 53080

Domestic Priority data as claimed by applicant

This application is a CON of PCT/JP2009/000574 02/13/2009

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

JAPAN 2008-064435 03/13/2008

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 12/14/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/629,508**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

page 1 of 3

Title

SEMICONDUCTOR DEVICE

Preliminary Class

257

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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page 2 of 3

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Docket No.: 085393-0059

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yoshihiro SATO, et al.

Application No.: 12/629,508

Customer No.: 53080

Filed: December 02, 2009

Confirmation No.: 7931

Group Art Unit: 2822

Examiner: PRENTY, Mark V.

Title: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

AMENDMENT UNDER 37 C.F.R. § 1.312

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Hon. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

We are in receipt of the Notice of Allowance dated March 20, 2012, issued in connection with the above-identified application. The following Amendment and Remarks are submitted in response to the Notice of Allowance.

Amendments to the Claims, begins on page 2;

Remarks, begins on page 15.

AMENDMENT TO THE CLAIMS

The following claim listing replaces all prior listings and versions of the claims:

LISTING OF CLAIMS

1. (Currently Amended) A semiconductor device comprising:
a first MIS transistor; and
a second MIS transistor, wherein:
the first MIS transistor includes:
a first gate insulating film formed on a first active region in a
semiconductor substrate, and including a first high-k film made of oxide
containing hafnium and silicon;
a first gate electrode ~~includes~~ including a second metal film formed on the
first gate insulating film;
first sidewall spacers formed on side surfaces of the first gate electrode,
the first sidewall spacers being insulative; and
a silicon nitride film formed, extending over the side surfaces
of the first gate electrode on which the first sidewall spacers are formed and upper
surfaces of regions located in the first active region laterally outside the first sidewall
spacers,
the second MIS transistor includes:
a second gate insulating film formed on a second active region in the
semiconductor substrate, and including a second high-k film made of oxide
containing hafnium and silicon;
a second gate electrode including a first metal film formed on the second

- gate insulating film and a conductive film formed on the first metal film;
- second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative;
- the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers; and
- source/drain regions formed in the second active region laterally outside the second sidewall spacers,
- the first and second metal films are made of different metal materials,
- the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes,
- the source/drain regions include a silicon mixed crystal layer which is formed in trenches provided in the second active region, and causes first stress in a gate length direction of a channel region in the second active region, and
- the silicon nitride film has a thickness smaller than that of the first gate electrode.
2. (Original) The semiconductor device of claim 1, wherein the first metal film has a thickness smaller than that of the second metal film.
3. (Original) The semiconductor device of claim 1, wherein the first and second metal films have different work functions.

4. (Canceled)
5. (Original) The semiconductor device of claim 1, wherein the conductive film is made of the second metal film.
6. (Original) The semiconductor device of claim 1, wherein the conductive film is made of a silicon film, and the semiconductor device further comprises a metal silicide film formed on the silicon film.
7. (Original) The semiconductor device of claim 1, wherein the first and second gate insulating films are made of the same insulating material.
8. (Canceled)
9. (Currently Amended) The semiconductor device of claim 1, wherein:
each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and
each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section, and the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.
10. (Previously Presented) The semiconductor device of claim 1, wherein

the silicon nitride film causes second stress in a gate length direction of a channel region in the first active region.

11. (Previously Presented) The semiconductor device of claim 10, wherein:
the first MIS transistor is an n-type MIS transistor, and
the second stress is tensile stress.

12. (Canceled)

13. (Previously Presented) The semiconductor device of claim 1, wherein
the second MIS transistor is a p-type MIS transistor,
the silicon mixed crystal layer is made of a SiGe layer, and
the first stress is compressive stress.

14-20. (Canceled)

21. (Previously Presented) A semiconductor device comprising:
a first MIS transistor; and
a second MIS transistor, wherein:
the first MIS transistor includes:
a first gate insulating film formed on a first active region in a
semiconductor substrate;

a first gate electrode including a second metal film formed on the first gate insulating film;

first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and

a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,

the second MIS transistor includes:

a second gate insulating film formed on a second active region in the semiconductor substrate,

a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;

second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative; and

the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers,

the first and second metal films are made of different metal materials,

the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes,

the conductive film is made of a silicon film,

the semiconductor device further comprises a metal silicide film formed on the silicon film, and

the silicon nitride film has a thickness smaller than that of the first gate electrode.

22. (Previously Presented) The semiconductor device of claim 21, wherein the first metal film has a thickness smaller than that of the second metal film.

23. (Previously Presented) The semiconductor device of claim 21, wherein the first and second metal films have different work functions.

24. (Cancelled)

25. (Previously Presented) The semiconductor device of claim 21, wherein the first and second gate insulating films are made of the same insulating material.

26. (Previously Presented) The semiconductor device of claim 21, wherein the first and second gate insulating films are made of different insulating materials.

27. (Previously Presented) The semiconductor device of claim 21, wherein:
each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and

each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section, and

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the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.

28. (Canceled)

29. (Previously Presented) The semiconductor device of claim 21, further comprising:

source/drain regions formed in the second active region laterally outside the second sidewall spacers,

wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.

30. (Previously Presented) The semiconductor device of claim 21, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.

31. (Previously Presented) A semiconductor device comprising:

a first MIS transistor; and

a second MIS transistor, wherein:

the first MIS transistor includes:

a first gate insulating film formed on a first active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon;

a first gate electrode including a second metal film formed on the first gate insulating film;

first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and

a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,

the second MIS transistor includes:

a second gate insulating film formed on a second active region in the semiconductor substrate, and including a second high-k film made of oxide containing hafnium and silicon;

a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;

second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative; and

the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers,

the first and second metal films are made of different metal materials,

the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes, and

the first metal film is made of titanium nitride.

32. (Previously Presented) The semiconductor device of claim 31, wherein the first metal film has a thickness smaller than that of the second metal film.

33. (Previously Presented) The semiconductor device of claim 31, wherein the first and second metal films have different work functions.

34. (Previously Presented) The semiconductor device of claim 31, wherein the silicon nitride film has a thickness smaller than that of the first gate electrode.

35. (Previously Presented) The semiconductor device of claim 31, wherein:
each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and

each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section, and

the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.

36. (Canceled)

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37. (Previously Presented) The semiconductor device of claim 31, further comprising:

source/drain regions formed in the second active region laterally outside the second sidewall spacers,

wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.

38. (Canceled)

39. (Previously Presented) A semiconductor device comprising:

a first MIS transistor; and

a second MIS transistor, wherein:

the first MIS transistor includes:

a first gate insulating film formed on a first active region in a semiconductor substrate;

a first gate electrode including a second metal film formed on the first gate insulating film;

first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and

a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,

the second MIS transistor includes:

a second gate insulating film formed on a second active region in the semiconductor substrate;

a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;

second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative; and

the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers,

the first and second metal films are made of different metal materials,

the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes, and

the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region.

40. (Previously Presented) The semiconductor device of claim 39, wherein the first metal film has a thickness smaller than that of the second metal film.

41. (Previously Presented) The semiconductor device of claim 39, wherein the first and second metal films have different work functions.

42. (Previously Presented) The semiconductor device of claim 39, wherein the silicon nitride film has a thickness smaller than that of the first gate electrode.

43. (Previously Presented) The semiconductor device of claim 39, wherein the conductive film is made of the second metal film.

44. (Previously Presented) The semiconductor device of claim 39, wherein:
the conductive film is made of a silicon film, and
the semiconductor device further comprises a metal silicide film formed on the silicon film.

45. (Previously Presented) The semiconductor device of claim 39, wherein the first and second gate insulating films are made of the same insulating material.

46. (Previously Presented) The semiconductor device of claim 39, wherein the first and second gate insulating films are made of different insulating materials.

47. (Currently Amended) The semiconductor device of claim 39, wherein:
each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, [[and]]
each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section, and

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the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.

48. (Canceled)

49. (Previously Presented) The semiconductor device of claim 39, further comprising:

source/drain regions formed in the second active region laterally outside the second sidewall spacers,

wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.

50. (Previously Presented) The semiconductor device of claim 39, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.

51. (Canceled)

52. (Canceled)

12/629,508

REMARKS

Claims 1, 9 and 47 have been amended to correct minor informalities in the claim language. No new matter has been introduced. Entry of this amendment is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Takashi Saito
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600 13th Street, N.W.
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Phone: 202.756.8000 TS:ss
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Date: April 25, 2012

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Electronic Acknowledgement Receipt	
EFS ID:	12630038
Application Number:	12629508
International Application Number:	
Confirmation Number:	7931
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Yoshihiro SATO
Correspondence Address:	McDERMOTT WILL & EMERY LLP - 600 13th Street, N.W. - Washington DC 20005-3096 US 2027568000 -
Filer:	Stephen Alan Becker/stephanie sharrett
Filer Authorized By:	Stephen Alan Becker
Attorney Docket Number:	085393-0059
Receipt Date:	25-APR-2012
Filing Date:	02-DEC-2009
Time Stamp:	17:10:38
Application Type:	Utility under 35 USC 111(a)

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Submitted with Payment	no
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File Listing:

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment after Notice of Allowance (Rule 312)	AMD.PDF	157984 8345a1b8d0af0e23737581f29d39600741629c86	no	15
Warnings:					
Information:					
Total Files Size (in bytes):			157984		
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Receipt date: 04/25/2012

12629508 - GAU: 2822

OK TO ENTER: /M.P./ (05/01/2012)

Docket No.: 085393-0059

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yoshihiro SATO, et al.

Application No.: 12/629,508

Customer No.: 53080

Filed: December 02, 2009

Confirmation No.: 7931

Group Art Unit: 2822

Examiner: PRENTY, Mark V.

Title: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

AMENDMENT UNDER 37 C.F.R. § 1.312

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P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

We are in receipt of the Notice of Allowance dated March 20, 2012, issued in connection with the above-identified application. The following Amendment and Remarks are submitted in response to the Notice of Allowance.

Amendments to the Claims, begins on page 2;

Remarks, begins on page 15.

DM_US 33804026-1.085393.0059

Response to Rule 312 Communication	Application No.	Applicant(s)
	12/629,508	SATO ET AL.
	Examiner	Art Unit
	MARK PRENTY	2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ The amendment filed on 25 April 2012 under 37 CFR 1.312 has been considered, and has been:

a) ☐ entered.

b) ☒ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

	/MARK PRENTY/ Primary Examiner, Art Unit 2822
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/629,508	12/02/2009	Yoshihiro SATO	085393-0059	7931
<div>7590 05/04/2012 McDERMOTT WILL & EMERY LLP 600 13th Street, N.W. Washington, DC 20005-3096</div>			<div>EXAMINER PRENTY, MARK V</div>	
			<div>ART UNIT 2822</div>	<div>PAPER NUMBER</div>
			<div>MAIL DATE 05/04/2012</div>	<div>DELIVERY MODE PAPER</div>

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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
12/629,508	02 December, 2009	SATO ET AL.	085393-0059

McDERMOTT WILL & EMERY LLP 600 13th Street, N.W. Washington, DC 20005-3096		EXAMINER	
		MARK PRENTY	
		ART UNIT	PAPER
		2822	20120501

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Commissioner for Patents

PTO-90C (Rev.04-03)

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7590 03/20/2012
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(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/629,508	12/02/2009	Yoshihiro SATO	085393-0059	7931

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1740	\$300	\$0	\$2040	06/20/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
PRENTY, MARK V	2822	257-289000

<p>1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).</p> <p>☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.</p> <p>☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.</p>	<p>2. For printing on the patent front page, list</p> <p>(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,</p> <p>(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.</p>	<p>McDERMOTT WILL & EMERY LLP</p> <p>2 _____</p> <p>3 _____</p>
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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

PANASONIC CORPORATION

Osaka, Japan

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☒ Advance Order - # of Copies 4

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 500417 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____
Typed or printed name Michael E. Fogarty

Date May 10, 2012
Registration No. 36,139

This collection of information is required by 37 CFR 1.314. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Electronic Patent Application Fee Transmittal				
Application Number:		12629508		
Filing Date:		02-Dec-2009		
Title of Invention:		SEMICONDUCTOR DEVICE		
First Named Inventor/Applicant Name:		Yoshihiro SATO		
Filer:		Stephen Alan Becker/stephanie sharrett		
Attorney Docket Number:		085393-0059		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1740	1740
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Printed copy of patent - no color	8001	4	3	12
Total in USD (\$)				2052

Electronic Acknowledgement Receipt	
EFS ID:	12749395
Application Number:	12629508
International Application Number:	
Confirmation Number:	7931
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Yoshihiro SATO
Correspondence Address:	McDERMOTT WILL & EMERY LLP - 600 13th Street, N.W. - Washington DC 20005-3096 US 2027568000 -
Filer:	Stephen Alan Becker/stephanie sharrett
Filer Authorized By:	Stephen Alan Becker
Attorney Docket Number:	085393-0059
Receipt Date:	10-MAY-2012
Filing Date:	02-DEC-2009
Time Stamp:	15:05:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 2052

RAM confirmation Number	1662				
Deposit Account	500417				
Authorized User					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	IF.PDF	102978 a63ae24782f95cf8af6c5c3c06e44a22ca9b0f42	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	33583 1d10e4acb69746dda9d488457e078d11ee a4cd5b	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			136561		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/629,508	06/12/2012	8198686	085393-0059	7931

7590 05/23/2012
McDERMOTT WILL & EMERY LLP
600 13th Street, N.W.
Washington, DC 20005-3096

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 9 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Yoshihiro SATO, Hyogo, JAPAN;
Hisashi Ogawa, Osaka, JAPAN;

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CHANGE OF CORRESPONDENCE ADDRESS Patent Address to: Mail Stop Post Issue Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450	Patent Number	8,198,686
	Issue Date	June 12, 2012
	Application Number	12/629,508
	Filing Date	December 2, 2009
	First Named Inventor	Yoshihiro SATO
	Attorney Docket Number	085393-0059

Please change the Correspondence Address for the above-identified patent to:

☒ The address associated with Customer Number: 53080
OR

☐ **Firm or Individual Name**

Address

City	State	ZIP
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I am the:

☐ Patentee.

☐ Assignee of record of the entire interest. See 37 CFR 3.71.
 Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☒ Attorney or agent of record. Registration Number 36,139

☐ Patent practitioner acting in a representative capacity whose correspondence address is the correspondence address of record. Notice has been given to the patentee or owner. Registration Number _____

Signature _____

Typed or Printed Name Michael E. Fogarty

Date April 9, 2013 Telephone (202) 756-8372

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of 1 forms are submitted.

Electronic Acknowledgement Receipt	
EFS ID:	15479062
Application Number:	12629508
International Application Number:	
Confirmation Number:	7931
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Yoshihiro SATO
Correspondence Address:	McDERMOTT WILL & EMERY LLP - 600 13th Street, N.W. - Washington DC 20005-3096 US 2027568000 -
Filer:	Michael E. Fogarty/Maung Kyaw
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0059
Receipt Date:	10-APR-2013
Filing Date:	02-DEC-2009
Time Stamp:	12:07:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Change of Address	085393-0059ChangeofAddress.pdf	43311 cda4238fa8ff3c4746d5c0cc25a85eb3c253c639	no	1
Warnings:					
Information:					
Total Files Size (in bytes):			43311		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					