

Dielectric Films for Advanced Microelectronics

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Preface

The excellent dielectric properties of silicon dioxide (SiO_2) have aided the evolution of microelectronics during the past 40 years. Silicon dioxide, which can be formed by thermal oxidation, has low defect density, and provides a thermodynamically stable interface. SiO_2 is characterized by a high resistivity, excellent dielectric strength, and a large bandgap. Silica films prepared either by thermal oxidation of silicon or by deposition have been successfully used for both gate and interconnect applications in ultra-large-scale integration (ULSI) devices.

However, in a continuous drive to increase integrated circuit performance through shrinkage of the circuit elements, the dimensions of MOSFETs (metal–oxide–silicon field effect transistors) and other devices have been scaled according to a trend known as Moore’s law. Moore’s law predicts the exponential growth of chip complexity due to decreasing minimum feature size, concurrent with improvements in circuit speed, memory capacity, and cost per bit. Starting from a certain feature size, this results in opposing requirements for the properties of gate and interlayer (ILD) dielectric films. Dielectric films for gate applications need to have higher dielectric constant, while interconnect dielectric materials need to have lower dielectric constant, compared with SiO_2 .

In order to maintain the high drive current and gate capacitance required of scaled MOSFETs, SiO_2 gate dielectrics have decreased in thickness from hundreds of nanometers 40 years ago to less than 2 nm today, with a continued effort to shrink to a thickness below 1 nm. However, SiO_2 layers thinner than 1.2 nm do not have the insulating properties required of a gate dielectric. The use of ultrathin SiO_2 gate dielectrics gives rise to a number of problems, including high gate leakage current, reduced drive current, poor resistance to impurity diffusion, and reliability degradation. Therefore, alternative gate dielectric materials, with small ‘equivalent oxide thickness’ (EOT) are required. Equivalent oxide thickness, $t_{\text{ox}}(\text{eq})$, is the thickness of the SiO_2 layer ($k = 3.9$) having the same capacitance as a given physical thickness of an alternative dielectric layer, t_{diel} :

$$t_{\text{ox}}(\text{eq}) = t_{\text{diel}}(3.9/k_{\text{diel}})$$

Therefore, to obtain a small EOT while maintaining the bulk properties of the dielectric material, the k_{diel} should be significantly higher than the value typical for SiO_2 . Dielectrics with values approximately between 10 and 30 are under consideration.

In the case of dielectric materials for interconnect applications, the requirement is the opposite. Modern ULSI devices contain 10^8 – 10^9 transistors in an area smaller than 1 cm^2 , and operate at a clock frequency approaching several gigahertz. As device dimensions shrink, the switching speed of the transistor increases, a consequence of the decreasing carrier transit time across the smaller channel length. The transistors must be

interconnected to make the ULSI device functional. As the functional complexity of devices increase, the number of interconnection levels, and total metal interconnect length, continue to increase to the extent that an advanced ULSI device may consist of 8–10 levels of metal lines. For this reason, the effective speed of the device becomes ever more dominated by signal propagation through the horizontal and vertical metal interconnects. It is here that the resistance R and capacitance C characteristics of the interconnect materials become important. In fact, the rapid increase in RC delay time is one of the main bottlenecks for deep sub-micrometer devices. The RC delay is given by:

$$RC = 2\rho k\epsilon_0(4L^2/P^2 + L^2/T^2)$$

where ρ is the metal resistivity, ϵ_0 is the vacuum permittivity, k is the relative dielectric constant of the interlayer dielectric, P is the metal line pitch (sum of line width and line spacing), T is the metal thickness, and L is the metal line length. This equation demonstrates that the RC delay can be reduced using metals with low resistivity and dielectric materials with low dielectric constant. The introduction of Cu and low dielectric constant (low- k) materials improves the situation compared with conventional Al/SiO₂ technology by reducing both the resistivity and capacitance between wires. Further reduction of the signal delay, through introduction of low- k dielectrics, is one of the main challenges today.

Therefore, the present situation is that SiO₂, having been the universal dielectric material for both gate and ILD applications for many years, must be replaced by materials with a higher dielectric constant for the gate applications and a reduced dielectric constant for interconnect applications.

These tendencies have changed the material properties of both gate and interconnect dielectrics. On the one hand, several new materials such as HfO₂, ZrO₂, and Al₂O₃ are investigated for introduction as high- k dielectrics. On the other hand, the need for dielectrics with a reduced dielectric constant requires the implementation of hydrophobic porous materials. In both cases the basic material properties are quite different compared with those of traditional dense SiO₂ and these differences create many technological challenges that are the subject of intensive research. For instance, metals forming high- k dielectric materials hardly form volatile compounds with halogens, making it extremely difficult to develop selective and damage-free dry etch processes. Diffusion of active radicals through the gate dielectric modifies the interface with silicon. Therefore, not only the development of new gate materials but also re-engineering of many technological processes is needed. In the case of low- k materials, porosity drastically increases the area of the reaction zone and the effective reactivity of these materials. Active species formed during different technological processes diffuse into the pores and create severe damage. All these problems have been stimulating the development of new technological approaches that will be discussed in the integration chapters.

This book presents an in-depth overview of novel developments made by scientific leaders in the microelectronics community. It covers a broad range of related topics, from physical principles to design, fabrication, characterization, and application of novel dielectric films. This book is intended for postgraduate level students, PhD students and industrial researchers, to enable them to gain insight into this important area of research.

The chapters included in this book can be divided into four separate sections. Chapters 1–5 are related to low- k materials developed for ILD applications. Chapters 1 and 2 focus on the deposition of low- k materials by plasma enhanced chemical vapor deposition

(PECVD) and spin-on glass (SOG) technology. Both of them are important for the preparation of different generations of low- k materials. Chapter 3 discusses methods developed for the evaluation of the porosity of low- k films. Although evaluation of porosity and pore size distribution is widely used in physical chemistry and catalysis, the introduction of low- k films requires the characterization of very thin films, for which most developed methods cannot be applied. Therefore, it was necessary to develop new methods applicable to thin-film analysis. Chapter 4 discusses the mechanical and transport properties of low- k dielectrics that presently define important integration challenges and reliability of interconnect structures. The last chapter of this section, Chapter 5, discusses the integration of low- k dielectric films.

Chapters 7–10 give an overview of recent developments in the field of high- k materials for gate applications. This section starts with a detailed discussion of the fundamentals and material science of high- k dielectric materials (Chapter 7), includes methods and results of physical and electrical characterization of ultra-thin high- k dielectrics (Chapters 8, 9), and ends with the integration of high- k dielectrics (Chapter 10).

Chapter 6, located between the low- k and high- k sections, is mainly oriented towards the physics and integration of materials with a ‘medium dielectric constant’ (ONO structures).

The last chapter of the book (Chapter 11) discusses the application of thin conductive films (ACF) for advanced microelectronic interconnects.

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