

# On the Thermal Stability of Atomic Layer Deposited TiN as Gate Electrode in MOS Devices

J. Westlinder, *Student Member, IEEE*, T. Schram, L. Pantisano, E. Cartier, A. Kerber, G. S. Lujan, J. Olsson, *Member, IEEE*, and G. Groeseneken, *Senior Member, IEEE*

**Abstract**—The work function of ALD TiN was found to be above 5 eV after RTP annealing below 800 °C in nitrogen atmosphere, while higher annealing temperatures cause a drop in work function by about 0.3–0.5 eV. The effect was found for TiN metal gates on both SiO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> gate dielectrics in MOS-capacitors and was seen in C–V as well as in I–V measurements. On the contrary, annealing of SiO<sub>2</sub> capacitors in oxygen-enriched N<sub>2</sub> atmosphere increased the work function. A variation in EOT of less than 2 Å was demonstrated for the various annealing temperatures, concluding that the ALD TiN is stable in contact with the different dielectric materials. However, the decrease in work function that is found in this investigation may implicate that ALD TiN is less suitable as a metal gate for pMOSFETs.

**Index Terms**—Metal gate, RTP, titanium nitride (TiN), work function.

## I. INTRODUCTION

IN the gate stack of future CMOS technology, not only the standard silicon dioxide gate dielectric has to be substituted by a high-*k* material, but also the commonly used poly-Si gate electrode has to be replaced with a low resistive, metallic material [1]. The need for such replacement is due to issues like gate depletion, high sheet resistance, boron penetration, etc., associated with the poly-Si gate. Naturally, several requirements on the new gate material are made such as, process integration with the CMOS flow, material compatibility, proper work function, thermal stability of the gate itself and also in contact with the dielectric underneath, etc. For instance, to replace the poly-Si gate in nMOS and pMOS, the metal gate has to have a work function close to 4 and 5 eV, respectively. Lately, extensive work has been carried out on various materials and material combinations [2]–[5], in order to find a suitable metal gate, fulfilling the desired properties.

In this letter, the focus is set on the thermal stability of titanium nitride (TiN) as metal gate. Recently, it has been shown

that the work function of TiN varies between 4.8 and 5.3 eV depending on deposition method [6], proposing that ALD TiN could be suitable for replacing poly-Si in pMOSFETs. However, as will be shown in this letter, the work function of ALD TiN varies after annealing, making it less attractive as metal gate in MOSFETs. This report includes results from annealing experiments of ALD TiN MOS capacitors, from 400 to 1000 °C in N<sub>2</sub> ambient. The samples were made of both SiO<sub>2</sub> and double stack SiO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub> gate dielectrics of various thicknesses.

## II. DEVICE FABRICATION AND EXPERIMENTS

The devices used in this letter were MOS capacitors, fabricated on 8-in, p-type Si substrates using a LOCOS isolation scheme. The 10-nm-thick TiN was deposited by ALD at 350 °C using TiCl<sub>4</sub> and NH<sub>3</sub> as precursors [7], [8]. The layer thicknesses of the thermally grown SiO<sub>2</sub> were varied between 5 and 25 nm. The double-layer stack consisted of ALD Al<sub>2</sub>O<sub>3</sub> (4 to 16 nm) on top of 0.5 nm SiO<sub>2</sub>. The SiO<sub>2</sub> capacitors had a forming gas anneal at 420 °C for 30 min after the TiN deposition and gate patterning, whereas the SiO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub> capacitors had a 900 °C postdeposition anneal (PDA) in N<sub>2</sub> for 10 s prior to the TiN deposition. The capacitors were then annealed between 400 °C and 1000 °C in steps of 100 °C in an RTP furnace in N<sub>2</sub> ambient for 30 s. In addition, some samples were annealed in nitrogen diluted with 10% oxygen at 400 °C for 30 s. High-frequency capacitance–voltage (C–V) as well as quasi-static C–V measurements were carried out at each annealing temperature. Also current–voltage (I–V) measurements were performed. It is well known that Fowler–Nordheim (FN) gate current depends exponentially on the barrier height between SiO<sub>2</sub> and the gate electrode itself, see for example [9]. The current described by the FN equation was fitted and used to calculate the barrier height and from that extract the work function of the TiN gate electrode. All electrical measurements were carried out at room temperature. In addition, physical characterizations were carried out by means of TEM, X-ray diffraction (XRD), and time-of-flight secondary ion mass spectrometry (ToF-SIMS).

## III. RESULTS AND DISCUSSION

In a MOS capacitor, the flat band voltage  $V_{fb}$  is proportional to the gate material work function and the amount of charge present in the dielectric. Already at very low temperatures, the thermal treatments have a dramatic effect on the  $V_{fb}$  of all the SiO<sub>2</sub> stacks considered, see Fig. 1. Annealing in nitrogen causes

Manuscript received March 27, 2003; revised June 23, 2003. This work was supported in part by the Swedish Foundation of Strategic Research (SSF) within the High Frequency Silicon program. The review of this letter was arranged by T.-J. King.

J. Westlinder and J. Olsson are with the Material Science Department, The Ångström Laboratory, Uppsala University, SE-751 21 Uppsala, Sweden (e-mail: jorgen.westlinder@angstrom.uu.se).

T. Schram, L. Pantisano, G. S. Lujan, and G. Groeseneken are with IMEC, B-3001, Leuven, Belgium.

E. Cartier is with the IBM Research Division and International Sematech, IMEC, B-3001, Leuven, Belgium.

A. Kerber is with Infineon Technologies AG and International Sematech, IMEC, B-3001, Leuven, Belgium.

Digital Object Identifier 10.1109/LED.2003.816579

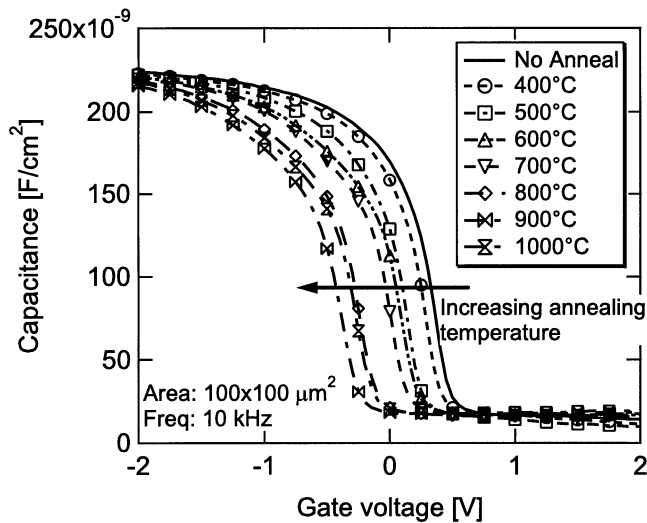


Fig. 1.  $C$ - $V$  characteristics for various  $N_2$  annealing temperatures for the 15 nm  $SiO_2$  stack. Flat band voltage shifts to lower value after annealing.

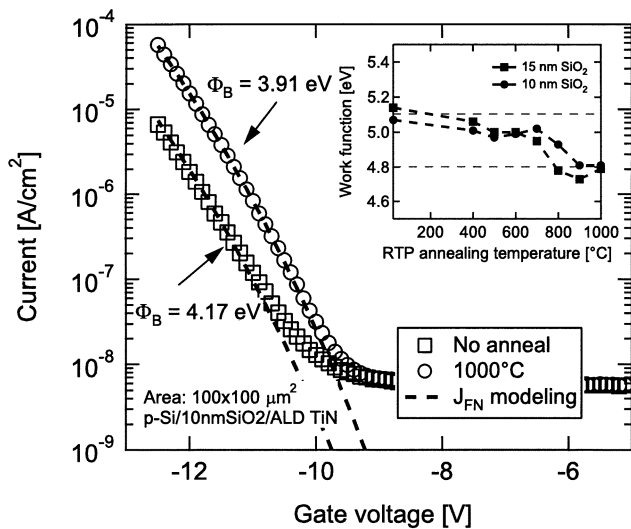


Fig. 2. Measured gate current and its FN fit in 10 nm  $SiO_2$ /TiN for several annealing temperatures. The work function was extracted by fitting the FN equation to the gate leakage current and the inset shows the work function versus annealing temperatures for 10 and 15 nm  $SiO_2$  gate stacks. The small variation in work function between the 10 and 15 nm oxide film could be due to variation in oxide charge, which will affect the extraction of the work function.

the  $V_{fb}$  to continuously shift to lower values, indicating a decrease in work function of the TiN gate and/or increase in positive charges in the oxide.

By analyzing the  $I_G$ - $V_G$  characteristics during gate injection, a change in work function is indeed confirmed. The various  $SiO_2$  gate stacks exhibit enhanced leakage current after annealing due to barrier lowering, see Fig. 2. Extracted work functions using the FN tunneling equation are summarized in the inset of Fig. 2. The work function of ALD TiN changes from a p-type gate material ( $5.1 \pm 0.1$  eV) toward a more midgap material ( $4.8 \pm 0.1$  eV) after annealing above  $\sim 800$  °C. The latter is close to what was reported recently for sputtered PVD TiN [6]. It is interesting to note that the work function remains p-type up to 700 °C.

Also worth noting is that the observed shift in  $V_{fb}$  ( $\sim 0.5$  V, see Fig. 1) is greater than the decrease in work function

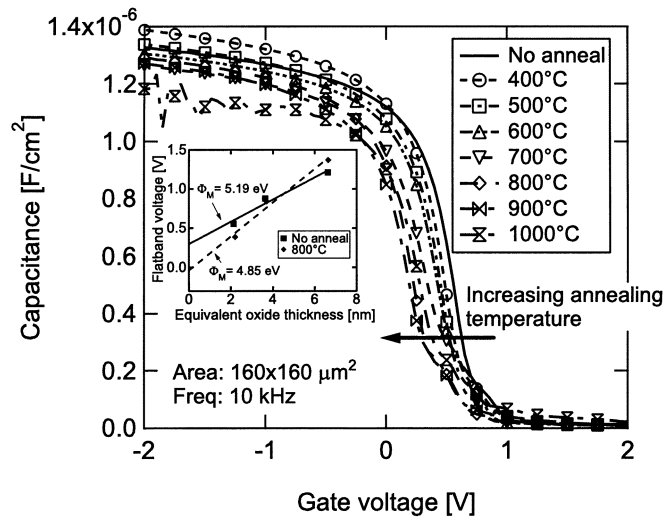


Fig. 3.  $C$ - $V$  characteristics for various  $N_2$  annealing temperatures for the  $SiO_2$ /(4 nm) $Al_2O_3$  stack. Flat band voltage shifts to lower value after annealing. The inset show  $V_{fb}$  vs. EOT for extraction of work function and fixed charge, before and after  $N_2$  annealing at 800 °C for the  $SiO_2$ / $Al_2O_3$  gate stack.

( $\sim 0.3$  eV). This is probably due to variation of the charges in the oxide, which is picked up by the  $C$ - $V$  measurement. Also, from quasi-static  $C$ - $V$  measurements, it is determined that the low temperature annealed samples have a considerable amount of interface states, which are reduced after annealing at the highest temperatures. However, the major part of the shift in  $V_{fb}$  corresponds to the change in work function. In contrast to annealing in pure nitrogen, annealing in  $N_2$  diluted with 10%  $O_2$  increases the work function. Samples were first annealed in pure  $N_2$  at 600 °C and then subsequently annealed in  $O_2$  enriched  $N_2$  at 400 °C. It was seen that the  $V_{fb}$  shifted back to its original value after the second annealing, which was also confirmed by work function extraction from  $I$ - $V$  measurements.

The  $SiO_2$ / $Al_2O_3$  stacks exhibit a similar decrease in  $V_{fb}$  value after annealing as the  $SiO_2$  stacks, see Fig. 3. By plotting  $V_{fb}$  vs. EOT for several  $Al_2O_3$  thicknesses, we find that the work function of ALD TiN decreases by about 0.35 eV after 800 °C RTP annealing, see the inset in Fig. 3. From the slope in the inset, it is determined that the fixed charge increases from  $3$  to  $5 \times 10^{12} \text{ cm}^{-2}$  after 800 °C annealing.

From the variation in accumulation capacitance (see Figs. 1 and 3) it is realized that the EOT varies by less than 2 Å for both  $SiO_2$  and  $SiO_2$ / $Al_2O_3$  gate stacks. A variation in EOT has previously been attributed to the chlorine content in the TiN film [10]. The small variations in EOT suggest that no severe reaction occurs between the gate and the gate dielectric.

It is still not clear why the work function changes during annealing. Complementary physical analysis has been used to verify the electrical results. In [11], [12] it has been reported that a change in the texture of the TiN and/or localized crystalline orientation variation at the TiN/ $SiO_2$  interface may lead to a change in the work function. XRD analysis is a powerful tool [13] to study change in the degree of crystallinity in a material. XRD patterns of the ALD TiN (111) peak showed no variation in intensity or peak shift in  $SiO_2$ /TiN and  $Al_2O_3$ /TiN stacks, concluding that no inter-reaction takes place up to 1000 °C annealing. In addition, TEM images show no changes in the

TiN gate or in the SiO<sub>2</sub>/TiN interfacial region for annealing up to 800 °C. The results from these physical methods support the electrical finding that no reaction occurs between the gate electrode and the gate dielectric. Furthermore, the XRD analysis showed no variation in the diffraction pattern during annealing, hence the texture of the ALD TiN is not the reason for the decrease in work function. Another common explanation is that the concentration of nitrogen in metal-nitrides is responsible for varying the work function of the material [14], [15], and could similarly be responsible for the decrease in work function observed in this study. With this in mind, ToF-SIMS has been used to profile the impurity concentrations in the gate electrode of the samples annealed in N<sub>2</sub> atmosphere. The results from the ToF-SIMS analysis showed no nitrogen variation in the TiN electrode after the various anneals. No nitrogen was either detected in the dielectrics. The analysis essentially displayed a small increase in oxygen concentration and slightly lowering of the chlorine concentration with increasing annealing temperature.

Still, the nitrogen concentration or more accurate, nitrogen vacancies, could be responsible for the variation in work function that is observed. Nitrogen vacancies in the TiN might be produced during the annealing leading to increased density of electron states, which in turn lowers the work function. During the subsequent annealing in the O<sub>2</sub> enriched atmosphere, oxygen fills up those nitrogen vacancies and the work function is increased. Nitrogen vacancies in the order of, say 10<sup>18</sup> cm<sup>-3</sup>, is quite a high value but would not be detected by the physical analysis methods used in this letter.

#### IV. CONCLUSION

The work function of ALD TiN depends strongly on the annealing condition. Annealing in pure N<sub>2</sub> up to 1000 °C lowers the work function by about 0.3–0.5 eV. Subsequent annealing in oxygen-enriched nitrogen increases the work function. No severe inter-reaction between the TiN gate and the under laying SiO<sub>2</sub> or Al<sub>2</sub>O<sub>3</sub> dielectric materials have been detected by means of physical analysis such as TEM and XRD or by electrical measurements, i.e., EOT comparisons from the accumulation capacitance. The variation in the work function of TiN that is evident cannot be related to either the texture of the TiN or the nitrogen concentration in the TiN. However, the concentration of nitrogen vacancies in the TiN may reduce the work function but has not been confirmed since the required amount of vacancies would be too low to be detected by the aforementioned physical analysis methods.

#### ACKNOWLEDGMENT

This work was carried out at IMEC, Leuven, Belgium. One of the authors (J. Westlinder) greatly acknowledges IMEC and the high-*k* team for all the support during his stay.

#### REFERENCES

- [1] *International Technology Roadmap for Semiconductors (ITRS)*: Semiconductor Industry Assoc., 2001.
- [2] T.-H. Cha, D.-G. Park, T.-K. Kim, S.-A. Jang, I.-S. Yeo, J.-S. Roh, and J. W. Park, "Work function and thermal stability of Ti<sub>1-x</sub>Al<sub>x</sub>N<sub>y</sub> for dual metal gate electrodes," *Appl. Phys. Lett.*, vol. 81, pp. 4192–4194, 2002.
- [3] V. Misra, H. Zhong, and H. Lazar, "Electrical properties of Ru-based alloy gate electrodes for dual metal gate Si-CMOS," *IEEE Electron Device Lett.*, vol. 23, pp. 354–356, June 2002.
- [4] I. Polishchuk, P. Ranade, T.-J. King, and C. Hu, "Dual work function metal gate CMOS technology using metal interdiffusion," *IEEE Electron Device Lett.*, vol. 22, pp. 444–446, Sept. 2001.
- [5] Y.-S. Suh, G. P. Heuss, and V. Misra, "Electrical characteristics of TaSi<sub>x</sub>N<sub>y</sub>/SiO<sub>2</sub>/Si structures by Fowler-Nordheim current analysis," *Appl. Phys. Lett.*, vol. 80, pp. 1403–1405, 2002.
- [6] G. S. Lujan, T. Schram, L. Pantisano, J. C. Hooker, S. Kubicek, E. Rohr, J. Schuhmacher, O. Kilpelä, H. Sprey, S. D. Gendt, and K. D. Meyer, "Impact of ALCVD and PVD titanium nitride deposition on metal gate capacitors," in *Proc. ESSDERC*, Firenze, Italy, 2002.
- [7] W. F. A. Besling, A. Satta, J. Schuhmacher, G. Beyer, K. Maex, O. Kilpelä, and H. Sprey, "Characterization of TiN films deposited by atomic layer deposition," in *Proc. Int. Conf. Microelectron. Interfaces*, Santa Clara, CA, 2002.
- [8] A. Satta, J. Schuhmacher, C. M. Whelan, W. Vandervorst, S. H. Brongersma, G. P. Beyer, K. Maex, A. Vantomme, M. M. Viitanen, H. H. Brongersma, and W. F. A. Besling, "Growth mechanism and continuity of atomic layer deposited TiN films on thermal SiO<sub>2</sub>," *J. Appl. Phys.*, vol. 92, pp. 7641–7646, 2002.
- [9] S. M. Sze, *Phys. Semicond. Devices*, 2nd ed. New York: Wiley, 1981.
- [10] D.-G. Park, K.-Y. Lim, H.-J. Cho, T.-H. Cha, I.-S. Yeo, J.-S. Roh, and J. W. Park, "Impact of atomic-layer-deposited TiN on the gate oxide quality of W/TiN/SiO<sub>2</sub>/Si metal-oxide-semiconductor structures," *Appl. Phys. Lett.*, vol. 80, pp. 2514–2516, 2002.
- [11] M.-F. Wang, T.-Y. Huang, Y.-C. Kao, H.-C. Lin, and C.-Y. Chang, "Impact of thermal stability on the characteristics of complementary metal oxide semiconductor transistors with TiN metal gate," *Jpn. J. Appl. Phys.*, vol. 41, pp. 546–551, 2002.
- [12] A. Yagishita, T. Saito, K. Nakajima, S. Inumiya, Y. Akasaka, Y. Ozawa, G. Minamihaba, H. Yano, K. Hieda, K. Suguro, T. Arikado, and K. Okumura, "High performance metal gate MOSFET's fabricated by CMP for 0.1 μm regime," in *IEDM Tech. Dig.*, 1998, pp. 785–788.
- [13] A. Perez-Rodriguez, A. Cornet, and J. R. Morante, "Physical techniques for silicon layer analysis," *Microelectron. Eng.*, vol. 40, pp. 223–237, 1998.
- [14] H. Wakabayashi, Y. Saito, K. Takeuchi, T. Mogami, and T. Kunio, "A dual-metal gate CMOS technology using nitrogen-concentration-controlled TiNx film," *IEEE Trans. Electron Devices*, vol. 48, pp. 2363–2369, Oct. 2001.
- [15] R. Lin, Q. Lu, P. Ranade, T.-J. King, and C. Hu, "An adjustable work function technology using Mo gate for CMOS devices," *IEEE Electron Device Lett.*, vol. 23, pp. 49–51, Jan. 2002.