

Scalability of Stress Induced by Contact-Etch-Stop Layers: A Simulation Study

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Abstract—This paper presents a study on the effectiveness of strained contact-etch-stop-layer (CESL) technologies in aggressively scaled dense structures. The focus is on nested transistors, which is a technologically very important structure that consists of a chain of gates on one active area. It will be shown that the two main channel stress components introduced by CESL, which are the vertical and parallel stresses, have a different sensitivity toward layout variations, which accordingly leads to different scaling guidelines to obtain a layout-insensitive strained CESL technology. Decreasing the CESL thickness is not enough for technology scaling; also, adapting the spacer dimensions is indispensable to scale a strained CESL technology from one technology node to the next.

Index Terms—MOSFET, strained-silicon.

I. INTRODUCTION

THE USE of mechanical strain has become a significant booster for silicon CMOS technology over the last five years. Strain changes the semiconductor's band structure and modulates the conduction mass and intervalley and interband scattering properties of electrons and holes. This in turn can improve or degrade the characteristics for n- and p-type MOSFETs.

One promising technique to introduce strain inside a transistor channel is the use of a silicon-nitride contact-etch-stop layer (CESL) with an intrinsic stress [1]–[8]. This layer is deposited in a CMOS flow after the source/drain (S/D) and gate silicidation module, and serves as a stopping layer for the contact etching between the first level of metal and the transistor's S/D and gate regions. CESL has a typical thickness of 20 nm and can contain up to 3 GPa of tensile or compressive stress, depending on the deposition conditions. The intrinsic stress inside the CESL translates into a stress state in the MOS channel. For short-channel transistors, a CESL with tensile intrinsic stress improves the nMOS performance, while a compressive intrinsic stress is beneficial for the pMOS behavior [1], [3], [7], [8].

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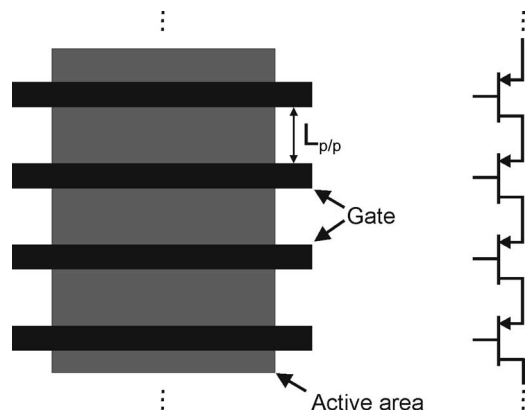


Fig. 1. Top-view layout of (left) a nested-transistor structure and (right) the corresponding electrical circuit.

Similar to the SiGe S/D-technology, which is used to generate a compressive channel stress in pMOS transistors, the CESL technology is a local stress technique. Both techniques have the advantage that the induced channel stress increases if the transistor length is scaled. On the other hand, the channel stress is a function of other structural dimensions as well. For CESL, important parameters are the CESL thickness, the transistor's gate length and height, the intrinsic stress in the CESL, the spacer thickness [5], [9], and the active-area length and width [10]. These dependences complicate technology modeling and make a thorough understanding of CESL-induced stress indispensable for the design of digital and analog circuits.

The purpose of this paper is to investigate the sensitivity of CESL-induced stress toward one specific important dimension: the active-area size and poly-to-poly length in aggressively scaled nested transistors. A nested-transistor structure is a chain of gates on one active area, which is separated by a distance of $L_{p/p}$, which is the poly-to-poly length. This structure is a basic building block in CMOS technology (Fig. 1). It is intuitively clear that in scaled nested structures, the amount of CESL between the consecutive poly lines is reduced, which may lead to a decreased effectiveness of the technology.

The stress simulations in this paper are performed with the finite-element simulator Taurus-Process of Synopsys [11]. The focus is on short-channel transistors ($L_g < 50$ nm), and we use the stress in the center of the channel, 1 nm below the silicon surface (Fig. 2), as a measure for the CESL-induced stress. The goal is to indicate how channel stress changes as a function of active-area length and to point out the essential differences between the two stress components induced by CESL in the channel, the parallel and vertical stresses. All simulated nested

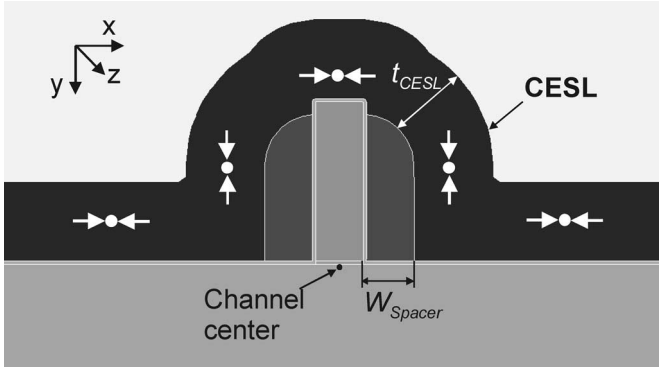


Fig. 2. Schematic cross section of a transistor with tensile strained CESL and D-shaped spacers. A tensile CESL tends to shrink, as indicated by the converging arrows.

transistors of this paper have the silicon channel in a $\langle 110 \rangle$ direction on a $\{100\}$ wafer and use polysilicon as gate material and silicon nitride as spacer material. For polysilicon and silicon nitride, a Young's modulus of 162 and 192 GPa was assumed, respectively. The silicon substrate is modeled as a mechanically anisotropic material, with the elastic constants given in [11].

This paper starts with a short overview of the principle of CESL-induced stress and then focuses on the layout dependence of the vertical and parallel channel stresses. In these sections, the gate length L_g and height are kept constant at 30 and 100 nm, respectively. Advancing toward the next technology nodes scales not only the active-area dimensions but also the poly length and height, and the spacer width. The effect on CESL-induced stress of scaling all these parameters in conjunction is presented in the last part of this paper.

II. CESL-INDUCED STRESS

Qualitatively, the principle of CESL-induced stress can be explained as follows: A CESL with an intrinsic tensile stress tends to shrink, as shown in Fig. 2. Since the CESL is bound to the S/D, gate, and spacers, the CESL shrinkage is counteracted by these regions. As a consequence, the S/D, spacer, and gate regions are stressed, which is finally translated into a transistor channel stress. For the case of tensile intrinsic stress, the CESL on the S/D regions pulls the poly regions apart, as well as the channel underneath, resulting in a tensile parallel channel stress (x -direction in Fig. 2). On the spacer sidewalls, the vertical shrinkage of the CESL compresses the poly region and leads to a compressive vertical stress in the gate material and in the transistor channel (y -direction). The CESL on top of the gate compresses the top part of the gate in the x -direction but has little or no effect on the channel stress, since, for short channels, the amount of CESL on top of the poly lines is limited. Finally, in the z -direction, for wide transistors, the "plane strain" condition applies (strain component $\varepsilon_{iz} = 0$, $i = x, y, z$), leading to a relatively small channel stress in this direction. Both the parallel and vertical stresses are generated by the interaction of the CESL with the gate topography. Stress techniques such as the $\text{Si}_{1-x}\text{Ge}_x$ and $\text{Si}_{1-x}\text{C}_x$ technique reduce the gate topography when the epitaxial layers are grown above

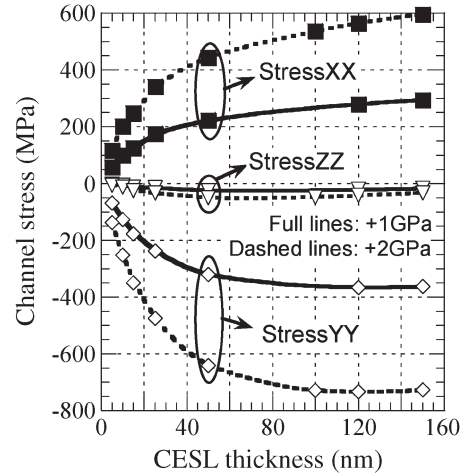


Fig. 3. Channel stress in the x -, y -, and z -directions inside an isolated transistor channel as a function of CESL thickness. The transistor has a gate length L_g of 30 nm and D-shaped spacers with a width of 30 nm. The solid line indicates the channel stress for a tensile intrinsic CESL stress of +1 GPa; the dashed lines correspond to a tensile intrinsic stress of +2 GPa. Positive stress values indicate tensile stress; negative values are compressive.

TABLE I
RELATIVE CONDUCTANCE CHANGE IN n- and p-TYPE TRANSISTORS FOR 100-MPa TENSILE STRESS APPLIED (ACCORDING TO [12]). TRANSISTOR CHANNELS ARE ASSUMED IN THE $\langle 110 \rangle$ DIRECTION ON $\langle 100 \rangle$ WAFERS (INDUSTRY STANDARD)

	n-type silicon	p-type silicon
Parallel stress (x -direction)	3.1%	-7.2%
Vertical stress (y -direction)	-5.3%	0.1%
Perpendicular stress (z -direction)	1.7%	6.6%

the original S/D regions. As a consequence, the effectiveness of a CESL is expected to decrease when used in combination with these layers.

The behavior of CESL-induced stress, as was qualitatively explained in Fig. 2, is summarized in a more quantitative way in Fig. 3. This figure shows the channel stress in the x -, y -, and z -directions for CESL with +1 GPa or +2 GPa of tensile intrinsic stress (positive stress values indicate tensile stress; negative stresses are compressive). A tensile intrinsic stress in the CESL results in a tensile parallel stress in the channel and a compressive vertical stress, while the perpendicular stress (z -direction) is negligible. Thicker CESL leads to higher channel stress, but the stress starts to saturate for CESL thicknesses above 40–50 nm. Finally, increasing the intrinsic CESL stress to +2 GPa enhances the channel stress (Fig. 3). In a similar way, changing the intrinsic CESL stress from tensile to compressive changes the sign of the channel stress: This leads to compressive parallel channel stress and tensile vertical stress.

Since a tensile parallel stress and a compressive vertical stress are favorable for the electron mobility (Table I), CESL with a tensile intrinsic stress is ideal to enhance the nMOS

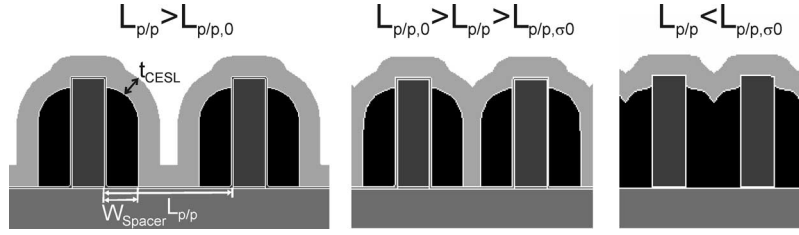


Fig. 4. Schematic cross section of a nested-transistor structure with CESL, indicating the case for (left) the CESL on the sidewalls not touching, (middle) CESL touching, and (right) spacers touching.

performance. For pMOS, only the parallel stress induced by CESL is important, since hole conduction is insensitive to vertical stress (Table I). CESL with a compressive intrinsic stress provides compressive parallel stress in the channel and, therefore, improves the mobility in pMOS transistors.

III. STRAINED CESL IN NESTED STRUCTURES: VERTICAL STRESS

As indicated in the previous section, the topography of the gate is essential to explain the stresses that are introduced in the transistor channel by the CESL technology. Layout variations that leave the topography unchanged are expected to have only minor influence on CESL-induced stress. This was demonstrated for variations of the active-area length in transistors that are surrounded by shallow-trench isolation in [13]. The qualitative assumptions made in the previous section will be used to explain the behavior of stress in nested transistors: The CESL on the S/D regions is responsible for the parallel channel stress. For the vertical stress, the CESL material on the spacer sidewalls is crucial.

For large poly-to-poly lengths, the amount of CESL on the sidewalls remains constant if $L_{p/p}$ changes. As a consequence, the vertical channel stress is independent of $L_{p/p}$ for large $L_{p/p}$. However, if the poly-to-poly spacing becomes small enough, the CESL on the spacer sidewalls starts touching. Further reduction of $L_{p/p}$ reduces the amount of CESL on the spacer sidewalls (Fig. 4, middle) and, therefore, reduces the vertical channel stress. To have a layout-insensitive vertical stress, $L_{p/p}$ needs to be larger than the “drop-off” poly-to-poly length $L_{p/p,0}$, for which the CESL on the spacer sidewalls starts touching:

$$L_{p/p} > L_{p/p,0} = 2 \cdot t_{CESL} + 2 \cdot W_{Spacer} \quad (1)$$

where t_{CESL} is the thickness of the CESL, and W_{Spacer} is the spacer width (Fig. 4).

When $L_{p/p}$ has become so small that there is no CESL left on the spacer sidewalls, the vertical channel stress is reduced to zero (Fig. 4, right). This occurs at the poly-to-poly length $L_{p/p,\sigma 0}$ when the spacers start touching

$$L_{p/p,\sigma 0} = 2 \cdot W_{Spacer}. \quad (2)$$

The dependence of vertical stress on $L_{p/p}$ is shown in Fig. 5. Fig. 5(a) shows the layout dependence of the CESL technology for different thicknesses of the CESL. The intrinsic

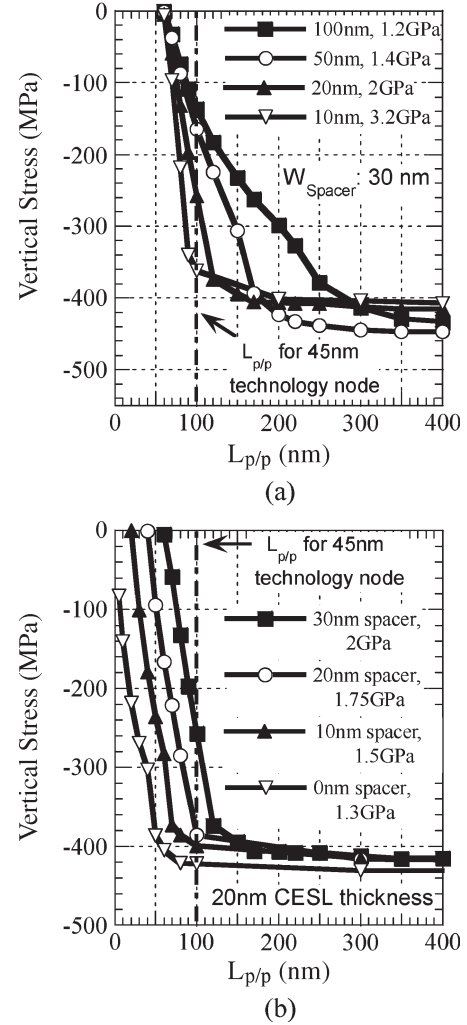


Fig. 5. Vertical channel stress as a function of poly-to-poly length $L_{p/p}$ for (a) various CESL thicknesses (constant spacer width $W_{Spacer} = 30$ nm) and (b) various spacer widths (constant CESL thickness $t_{CESL} = 20$ nm). The intrinsic stress inside the CESL has been adjusted for every curve to obtain a similar stress value for large $L_{p/p}$ (intrinsic stresses are indicated in the figure's labels). The transistors have a gate length L_g of 30-nm and D-shaped spacers.

stress in the CESL has been adapted for each t_{CESL} to obtain a similar vertical channel stress at large $L_{p/p}$. As indicated previously, the vertical stress remains relatively constant, as long as $L_{p/p}$ is larger than $L_{p/p,0}$. Thicker CESL leads to a larger $L_{p/p,0}$ (1) and is therefore more sensitive to layout variations [Fig. 5(a)]. However, $L_{p/p,\sigma 0}$ is independent of the CESL thickness, as shown in Fig. 5(a). For the 45-nm technology node [14], with a typical $L_{p/p}$ around 100 nm, even a

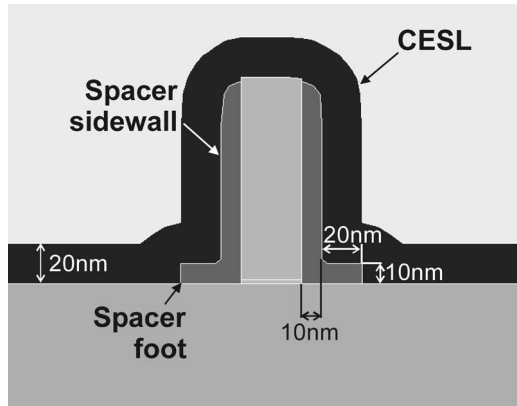


Fig. 6. Schematic cross section of a transistor with an L-shaped spacer.

20-nm-thick CESL shows a clear reduction in the channel stress for a spacer width of 30 nm. Only a very thin CESL with a very high intrinsic stress can provide an $L_{p/p}$ -insensitive channel stress [Fig. 5(a)].

$L_{p/p,0}$ is also a function of the spacer width W_{Spacer} . Fig. 5(b) plots the vertical channel stress as a function of $L_{p/p}$ for nested transistors with various spacer widths. Reducing the spacer width makes the CESL-induced channel stress less dependent of $L_{p/p}$ (1). Moreover, $L_{p/p,0}$ is reduced for thinner spacers. For 20-nm-thick CESL, a very thin spacer is needed to have a layout-insensitive technology down to poly-to-poly lengths of 100 nm [Fig. 5(b)]. Using thinner spacers has the additional advantage that it allows using a lower intrinsic stress in the CESL and still maintains the same vertical channel stress [Fig. 5(b)]. This is more advantageous than scaling the CESL thickness, since a higher intrinsic CESL stress is required in that case.

Fig. 5(b) focuses on the layout sensitivity for the case of the commonly used D-shaped spacers, as shown in Fig. 2. Another type of spacer is the L-shaped spacer. A comparison between the layout sensitivity for an L-shaped spacer (dimensions shown in Fig. 6) and the D-shaped spacer is shown in Fig. 7. Since this simulated L-shaped spacer has a sidewall thickness similar to a 10-nm-wide D-shaped spacer, but with a total foot width of 30 nm, it is compared to nested transistors with 10- and 30-nm-wide D-shaped spacers. The presence of the spacer foot reduces the effectiveness of the CESL, such that a higher intrinsic stress is needed than in a 10-nm-wide D-shaped spacer (Fig. 7). However, the L-shaped spacer is more effective in terms of CESL stress transfer than the 30-nm-wide D-shaped spacer. Since the vertical channel stress is determined by CESL on the spacer sidewalls, (1) and (2) are expected to be valid as well for the L-shaped spacers. In this case, W_{Spacer} denotes the thickness of the spacer sidewall. This is also confirmed in Fig. 7, which shows similar layout sensitivity of an L-shaped spacer with a W_{Spacer} of 10 nm and a 10-nm-wide D-shaped spacer.

IV. STRAINED CESL IN NESTED STRUCTURES: PARALLEL STRESS

As indicated in the previous sections, it is assumed that strained CESL on the S/D areas is responsible for the parallel-

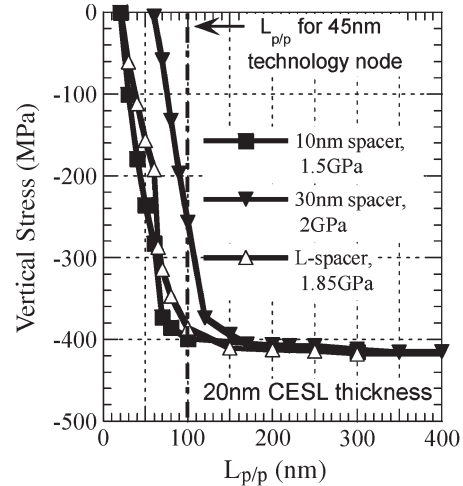


Fig. 7. Vertical channel stress as a function of poly-to-poly length $L_{p/p}$ for nested structures with a 10- and 30-nm-wide D-shaped spacer and an L-shaped spacer with dimensions shown in Fig. 6. CESL thickness $t_{\text{CESL}} = 20$ nm. The intrinsic stress inside the CESL has been adjusted for every curve to obtain a similar stress value for large $L_{p/p}$ (intrinsic stresses are indicated in the figure's labels). The transistor has a gate length L_g of 30 nm.

stress generation in a transistor channel. Unlike for the vertical stress, where the channel stress remains constant as long as the CESL on the spacer sidewalls does not touch, scaling $L_{p/p}$ reduces the amount of CESL on the S/D areas even for large $L_{p/p}$. It is therefore less trivial to define a drop-off $L_{p/p,0}$ for the parallel stress. The reduction of CESL material on the S/D areas occurs in a similar way for every CESL thickness t_{CESL} . As a consequence, it is intuitively clear that, to first order, the layout sensitivity of the parallel stress does not change as t_{CESL} is scaled. For a fixed $L_{p/p}$, increasing the spacer thickness decreases the amount of CESL on the S/D regions, which leads to decreased channel stress. This effect will be more pronounced for shorter active-area lengths and is negligible for large $L_{p/p}$. Therefore, the sensitivity is expected to change with spacer width W_{Spacer} . The condition for zero parallel stress is reached when there is no CESL material left on the S/D regions and is therefore given by (2), similar as for the case of the vertical stress.

Fig. 8 shows the dependence of the parallel channel stress on $L_{p/p}$. As indicated previously, changing the CESL thickness does not change the layout sensitivity considerably [Fig. 8(a)]. For all CESL thicknesses, the parallel channel stress starts to decrease for $L_{p/p} < 200$ nm, and it is reduced by about 50% when $L_{p/p}$ decreases to 100 nm. The layout sensitivity of the parallel stress changes with the spacer width, as shown in Fig. 8(b). However, even for an aggressively scaled spacer width of 20 nm and a 20-nm-thick CESL, the channel stress is reduced by 20% for a scaled nested transistor with an $L_{p/p}$ of 100 nm. As was also observed for the vertical stress, scaling the spacer width has the advantage that the same parallel channel stress can be obtained with a lower intrinsic stress of the CESL [Fig. 8(b)].

When an L-shaped spacer with the dimensions shown in Fig. 6 is used, the presence of the spacer foot reduces the parallel stress transfer into the channel, such that a higher intrinsic CESL stress is required than when a 10-nm-wide D-shaped

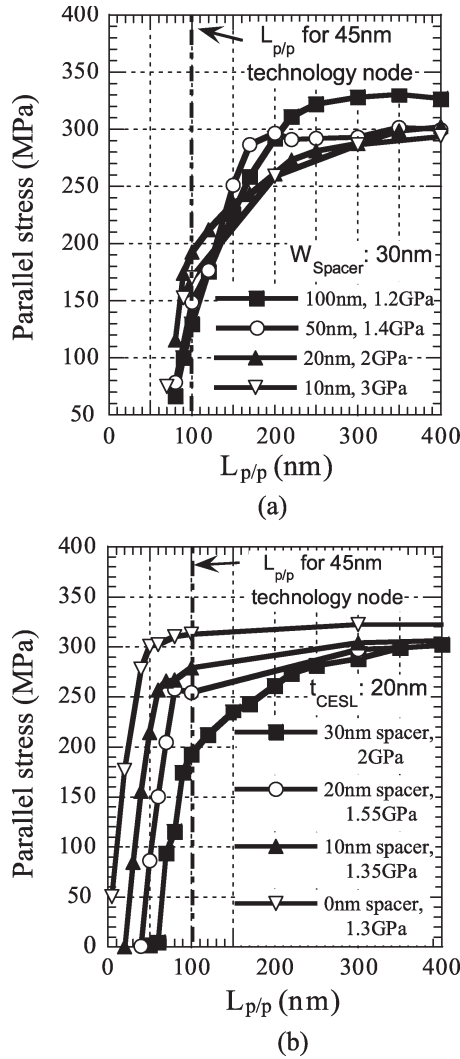


Fig. 8. Parallel channel stress as a function of poly-to-poly length $L_{p/p}$ for (a) various CESL thicknesses (constant spacer width $W_{Spacer} = 30$ nm) and (b) various spacer widths (constant CESL thickness $t_{CESL} = 20$ nm). The intrinsic stress inside the CESL has been adjusted for every curve to obtain a similar stress value for large $L_{p/p}$ (intrinsic stresses are indicated in the figure's labels). The transistors have a gate length L_g of 30 nm and D-shaped spacers.

spacer is used (Fig. 9). However, the stress transfer is more efficient than for a 30-nm-wide D-shaped spacer. The layout sensitivity of the L-shaped spacer is similar to the 10-nm-wide D-shaped spacer (Fig. 9), which indicates that a certain amount of the channel stress is generated by the CESL on top of the spacer foot.

V. SCALABILITY OF THE STRAINED CESL TECHNOLOGY

The previous sections demonstrated that the effectiveness of strained CESL reduces for shorter poly-to-poly lengths $L_{p/p}$. However, when advancing to the next CMOS technology nodes, several other transistor parameters will be scaled in conjunction. It is the purpose of this section to investigate whether the CESL-induced stress can be maintained from one technology node to another in scaled nested transistors. These simulations focus on CESL with a constant thickness of 20 nm and an intrinsic stress of 2 GPa. Typical nested transistor

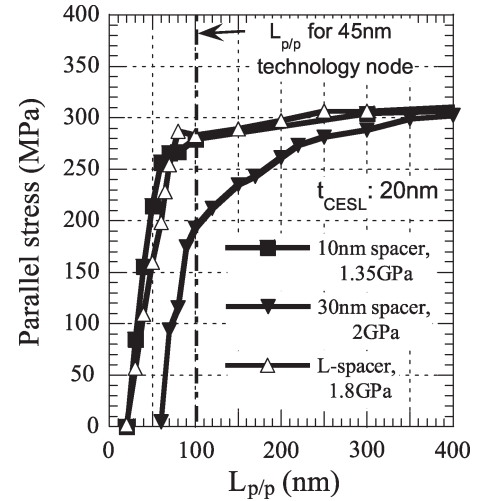


Fig. 9. Parallel channel stress as a function of poly-to-poly length $L_{p/p}$ for nested structures with a 10- and 30-nm-wide D-shaped spacer and an L-shaped spacer with dimensions shown in Fig. 6. CESL thickness $t_{CESL} = 20$ nm. The intrinsic stress inside the CESL has been adjusted for every curve to obtain a similar stress value for large $L_{p/p}$ (intrinsic stresses are indicated in the figure's labels). The transistor has a gate length L_g of 30 nm.

TABLE II
TECHNOLOGY PARAMETERS FOR THE 45-, 32-, AND 22-nm TECHNOLOGY NODES [14]

	L_g (nm)	$L_{p/p}$ (nm)	Poly Height (nm)
45nm node	18	100	100
32nm node	13	70	70
22nm node	9	50	50

dimensions for the 45-, 32-, and 22-nm technology nodes are used (Table II). As indicated in the previous sections, the spacer dimensions have a significant effect on the effectiveness of CESL-induced stress in scaled nested transistors. Therefore, three spacer scaling schemes are used in these simulations: a worst case condition, where the spacer width is kept constant between the technology nodes, a scaled spacer condition that scales W_{Spacer} with the technology node, and a best case condition, which corresponds to the technologically challenging situation where the spacer width is zero (Table III). As shown in Table II, poly-height scaling is included in these simulations. In the coming technology nodes, the poly height will be scaled either linearly with poly length, as in these simulations, or less strongly, such that the gate's aspect ratio increases. This paper focuses on the case of linear poly-height scaling, since it can be considered as worst case for the stress scalability, because CESL-induced stress decreases with poly height [9].

The bar diagram in Fig. 10 shows the absolute value of the channel stress in nested transistors of the 45-, 32-, and 22-nm technology nodes. Maintaining a constant spacer width degrades both the vertical and parallel channel stresses when moving to the next technology nodes. For constant spacers, decreasing the poly-to-poly length leads to $L_{p/p} < L_{p/p,0}$ for

TABLE III
SPACER WIDTHS W_{Spacer} USED FOR THE 45-, 32-, AND 22-nm TECHNOLOGY NODES

	Constant spacer (nm)	Scaled spacer (nm)	Best-case spacer (nm)
45nm node	30	30	0
32nm node	30	20	0
22nm node	30	15	0

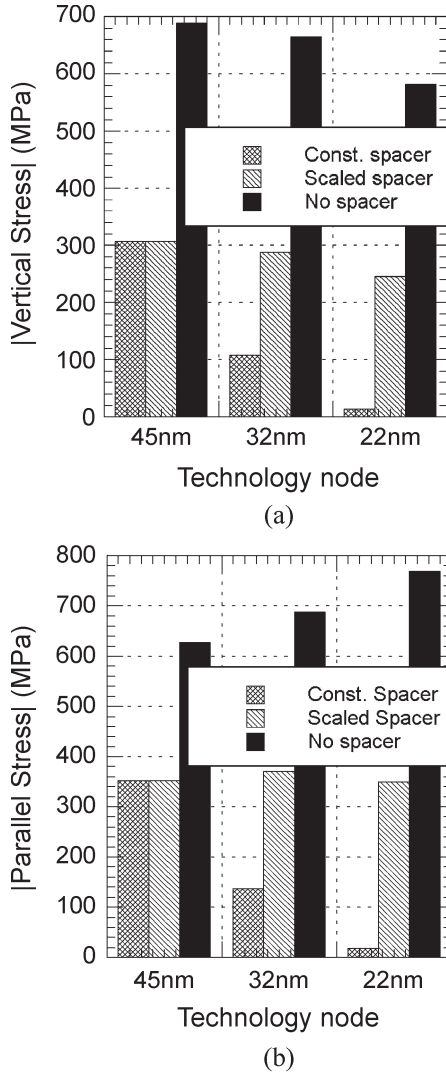


Fig. 10. Absolute values of the (a) vertical and (b) parallel channel stresses in nested transistors of the 45-, 32-, and 22-nm technology nodes with D-shaped spacers. The CESL thickness is 20 nm and has an intrinsic stress of +2 GPa. Transistor parameters are scaled according to Tables II and III.

the 32-nm node (1) and, eventually, to $L_{p/p} < L_{p/p,0}$ for the 22-nm node (2). Even for scaled spacers, $L_{p/p,0}$ does not scale to the same amount as $L_{p/p}$ when the CESL thickness is kept constant, leading to a slight decrease in vertical stress when scaling the technology node [Fig. 10(a)]. The parallel stress can be maintained however [Fig. 10(b)]. For the best case spacers, the vertical stress decreases slightly when scaling the technology, while the parallel channel stress increases.

VI. CONCLUSION

Channel stress induced by strained CESL is sensitive to the poly-to-poly length of nested transistors. This channel stress has two main components: a parallel stress, which is in the direction of the electrical conduction, and a vertical stress, which is perpendicular to the plane of the wafer. One of the main purposes of this paper was to illustrate the differences in layout sensitivity between the parallel and the vertical stress components. The assumption was made that the parallel stress is caused by CESL material on the S/D regions, while vertical channel stress is mainly generated by CESL on the spacer sidewalls. This assumption was supported by stress simulations of nested transistors with varying $L_{p/p}$, CESL thickness, and spacer width.

The layout sensitivity of the vertical stress depends both on the CESL thickness and spacer width. As long as the CESL on the spacer sidewalls from the neighboring transistors does not touch, the vertical stress is preserved. Therefore, thinner CESL and spacers both make the CESL-induced vertical stress less sensitive to active-area length variations in nested structures. While as compensation for the thinner CESL, higher intrinsic stress is needed to maintain the channel stress, thinner spacers can be combined with a lower intrinsic stress of the CESL.

Layout sensitivity of the parallel stress is a function of the spacer width but not of the CESL thickness. For 30-nm-wide spacers, the parallel stress is reduced by about 50% in scaled nested transistors of the 45-nm node ($L_{p/p} = 100$ nm), even for thin CESL with high stress. This indicates that spacer scaling is an absolute must to maintain an optimal parallel stress in scaled transistors.

For L-shaped spacers, the thickness of the spacer on the gate sidewalls determines the layout sensitivity. These spacers have the advantage over thick D-shaped spacers that a lower intrinsic stress of the CESL is required to obtain a similar channel stress. Moreover, the layout sensitivity is reduced for L-shaped spacers. Compared to thin D-shaped spacers with the same sidewall width, however, there is less stress transfer into the transistor channel.

When scaling nested transistors from one technology node to the next, it is indispensable that the spacer widths are scaled proportionally to the gate length: If the spacer width is kept constant, the effectiveness of a strained CESL technology diminishes rapidly.

For pMOS transistors, the parallel channel stress is responsible for the mobility improvement, while both the parallel and vertical stresses are important for the nMOS performance.

When using a strained CESL-based technology both for nMOS and pMOS, such as a DUAL CESL technique, using a very thin highly stressed CESL is not enough to be insensitive to layout variations. In particular, for pMOS transistors, aggressive spacer scaling is required to maintain the highest possible stress levels in the most dense layouts.

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