

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNITED MICROELECTRONICS CORPORATION,
AND
UMC GROUP (USA),
Petitioner,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,
Patent Owner.

Case IPR2025-01091
U.S. Patent No. 8,198,686

**DECLARATION OF DR. SANJAY BANERJEE IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,198,686**

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Declaration of Dr. Sanjay Banerjee
Inter Partes Review of U.S. Patent No. 8,198,686

I, Dr. Sanjay Banerjee, declare as follows:

1. My name is Sanjay Banerjee.
2. I have been retained as an expert witness on behalf of United Microelectronics Corporation and UMC Group (USA) (collectively, “Petitioner”) for the above-captioned Petition for *Inter Partes* Review (“IPR”) (“Petition”) of U.S. Patent No. 8,198,686 (“the ’686 patent”) (Ex.1001). I am being compensated for my time in connection with this Petition at my standard consulting rate of \$675 per hour. My compensation is not affected by the outcome of, or my testimony in, this IPR, or any litigation proceedings. I am informed that the assignee for the patent in the present proceeding is Advanced Integrated Circuit Process LLC (“Patent Owner”). I am also informed that the Petition names United Microelectronics Corporation and UMC Group (USA) as real-parties-in-interest.

3. I have been asked to provide my opinions regarding whether claims 25-28, 31, and 35 of the ’686 patent (the “Challenged Claims”) are invalid as anticipated, or as obvious to a person having ordinary skill in the art at the time of the alleged invention of the ’686 patent (“POSITA”).

4. The ’686 patent issued on June 12, 2012, from U.S. Patent Application No. 12/629,508, filed on December 2, 2009 as a continuation of PCT/JP2009/000574, filed on February 13, 2009. The ’686 patent claims priority to Japan Patent Application No. 2008-064435, filed on March 13, 2008.

5. I am not currently, and have not at any time in the past been, an employee of any Petitioner or any real-party-in-interest. Other than set out above, I have no affiliation, contractual connection, or financial connection with any Petitioner or any real-party-in-interest, or any of their respective subsidiaries or parents. I similarly have no financial interest in, or affiliation with the Patent Owner.

I. BACKGROUND AND QUALIFICATIONS

6. I am currently the Cockrell Family Chair Professor of Electrical and Computer Engineering at the University of Texas at Austin. At UT Austin, I was also the director of the Microelectronics Research Center from September 1999 through January 2025. I have been a faculty member at UT Austin since 1987.

7. I have also been active in industries related to the relevant field of art. As a Member of the Technical Staff, Corporate Research, Development and Engineering of Texas Instruments Incorporated from 1983–1987, I worked on polysilicon transistors and dynamic random access trench memory cells used by Texas Instruments in the world’s first 4-Megabit DRAM, for which I was co-recipient of the Best Paper Award, IEEE International Solid State Circuits Conference, 1986.

8. I received a B. Tech. degree from the Indian Institute of Technology, Kharagpur, and M.S. and Ph.D. degrees from the University of Illinois at Urbana-Champaign, all in Electrical Engineering.

9. I am a leading researcher and educator in various areas of transistor device fabrication technology, including the fabrication, characterization and application of memory devices, transistors, and nanotechnology. My research has been funded by the Texas Advanced Technology Program (ATP), the Texas Higher Education Coordinating Board, the National Science Foundation, the SEMATECH (Semiconductor Manufacturing Technology) consortium, the SRC (Semiconductor Research Corporation) consortium, DARPA, and the Department of Energy, among others.

10. At the University of Texas, I served as the director of the South West Academy of Nanoelectronics from its inception through the end (2006 - 2017), one of three centers in the United States established to develop a replacement for MOSFETs.

11. I have published over 1,200 technical articles, many related to semiconductor fabrication technology, most at highly competitive refereed conferences and rigorously reviewed journals. I have also published 8 books or chapters on transistor device physics and fabrication, and have supervised over 80 Ph.D. and 60 MS students.

12. I have been a member of scientific organizations and committees, including the IEEE Dan Noble Award Committee from 2010–2013, serving as Chair from 2012–2013, the International Technology Roadmap for Semiconductors, the

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International Conference on MEMS (Microelectromechanical Systems) and Nanotechnology, the IEEE International Conference on Communications, Computers, Devices, the International Electron Devices Meeting, the International Conference on Simulation of Semiconductor Processes and Devices, and the IEEE Symposium on VLSI (Very-Large-Scale Integration) Technology. I have served as the Session Chair for the “Device Technology” Session conducted at the IEEE International Electron Devices Meeting in 1989–1990. I have also served as the General Chairman for the IEEE University Government Industry Microelectronics Symposium in 1994–1995, and Chair of the IEEE Device Research Conference.

13. I have served on the Technical Advisory Boards of AstroWatt, DSM Semiconductors, Cambrios, Nanocoolers Inc., BeSang Memories, Organic ID and ITU Ventures; Gerson Lehmann Group, NY; Austin Community College; Asia Pacific IIT; Rochester Institute of Technology, and HSMC Foundry.

14. I received the Engineering Foundation Advisory Council Halliburton Award (1991), the Texas Atomic Energy Fellowship (1990–1997), Cullen Professorship (1997–2001) and the Hocott Research Award from UT Austin (2007). I also received the SIA/SRC University Researcher Award (2018), IEEE Grove Award (2014), Distinguished Alumnus Award, IIT (2005), Industrial R&D 100 Award (2004), ECS Callinan Award, 2003, IEEE Millennium Medal, 2000, NSF Presidential Young Investigator Award in 1988, and several SRC Inventor

Recognition and Best Paper Awards. I was a Distinguished Lecturer for IEEE Electron Devices Society, and am a Fellow of the Institute of the Electrical and Electronics Engineers (IEEE), the American Physical Society (APS) and the American Association for the Advancement of Science (AAAS).

15. I am the inventor or co-inventor of over 35 United States patents in various areas of transistor device fabrication technology. I was elected a Fellow of the National Academy of Inventors in 2021.

16. My qualifications and publications are set forth more fully in my curriculum vitae, attached as Ex.1102.

II. MATERIALS AND OTHER INFORMATION CONSIDERED

17. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art and have considered the viewpoint of a POSITA at the time of the alleged invention.

18. I have considered the materials referenced herein, including the '686 patent (Ex.1001), the file history of the '686 patent (Ex.1002), the parent and related applications, the file histories of the parent and related applications, the Petition, and other documents listed in the Exhibit List of the Petition, including:

Description	Date of Availability
U.S. Patent Application Publication No. 2007/0215950 A1 to Aoyama (“Aoyama”; Ex.1005)	Published September 20, 2007
U.S. Patent Application Publication No. 2007/0235823 A1 to Hsu823, et al. (“Hsu823”; Ex.1006)	Filed October 11, 2007
U.S. Patent Application Publication No. 2007/0066077 A1 to Akasaka, et al. (“Akasaka”; Ex.1008)	Published March 22, 2007

19. It is my understanding that the references listed above are prior art to the '686 patent, which is entitled to a priority date not earlier than March 13, 2008. Hsu823 and Akasaka (Exs. 1006 and 1008, respectively) were not discussed during the prosecution of the '686 patent.

III. UNDERSTANDING OF PATENT LAW

20. I am not an attorney. For purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law is as listed below.

A. Claim Construction

21. I understand that in an IPR petition filed after November 13, 2018, a claim must be construed under the *Phillips* standard. Under that standard, words of a claim are given their plain and ordinary meaning as understood by a POSITA at the time of invention, in light of the specification and prosecution history, unless those

sources show an intent to depart from such meaning, as well as pertinent evidence extrinsic to the patent.

22. I have applied this understanding in my declaration. I do not believe any claim terms require explicit construction in this proceeding to resolve the patentability of the Challenged Claims.

B. Anticipation and Obviousness

23. I have been informed that a patent claim is anticipated if a single prior art reference, such as a patent or a publication, discloses all the limitations of the claimed invention.

24. I have been informed and understand that a patent claim can be considered to have been obvious to a POSITA at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a POSITA at the time the application was filed. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and

- what differences, if any, existed between the claimed invention and the prior art.

25. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to a POSITA. In determining whether a combination based on either a single reference or multiple references would have been obvious, I have been informed that it is appropriate to consider at least the following factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;
- whether a POSITA could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed limitations represent one of a limited number of known design choices, and would have a reasonable expectation of success by a POSITA;
- whether a POSITA would have recognized a reason to combine known limitations in the manner described in the claim;

- whether there is some teaching or suggestion in the prior art to make the modification or combination of limitations claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

26. I understand that a POSITA has ordinary creativity and is not an automaton.

27. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

28. I understand that prior art to the '686 patent for purposes of my opinion herein includes patents and printed publications in the relevant art that predate the priority date of the '686 patent.

29. I understand that certain factors—often called “secondary considerations”—may support or rebut an assertion of obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the alleged invention, skepticism of those having ordinary skill in the art at the time of the alleged invention, unexpected results of the alleged invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged

invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field.

30. I further understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

IV. SUMMARY OF OPINIONS

31. It is my opinion that claims 25-28, 31, and 35 are obvious in view of a combination of Aoyama and Hsu823 (Ground I).

32. It is my opinion that claims 25-28, 31, and 35 are obvious in view of a combination of Akasaka and Hsu823 (Ground II).

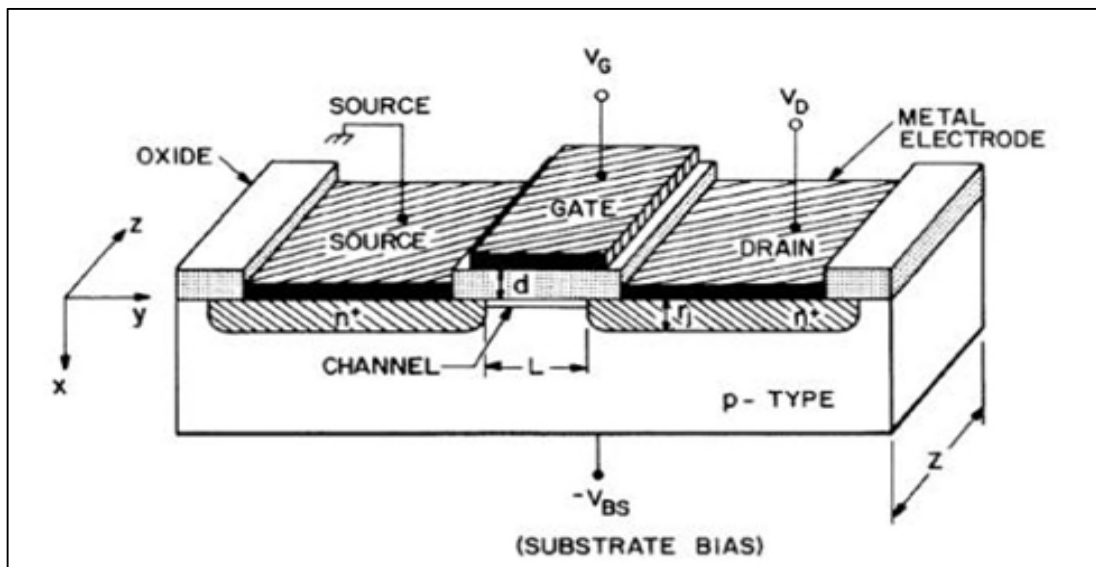
V. OVERVIEW OF THE TECHNOLOGY

33. Broadly speaking, a semiconductor device is an electrical device made of semiconductor material like silicon or germanium. This includes many types of devices like light-emitting diodes (LEDs) and metal oxide semiconductor (MOS) transistors. Field effect transistors are just one type of semiconductor devices and have been in commercial use for decades, as discussed in more detail below.

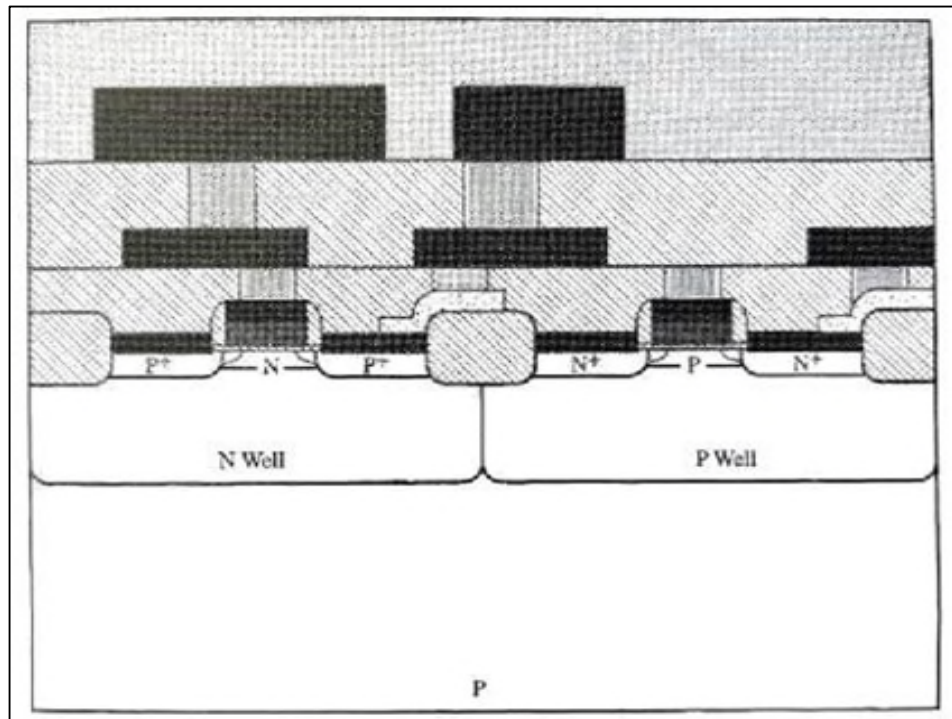
A. MISFET/MOSFET

34. A metal insulating semiconductor field-effect transistor (MISFET), commonly referred to as a metal oxide semiconductor field-effect transistor (MOSFET)

if the insulator is an oxide, is a transistor that switches from an OFF state to an ON state when a voltage greater than the threshold voltage is applied to a gate terminal. In the ON, or active state, current flows from a source to a drain through a channel region. For the transistor types at issue in this IPR, the channel region is located under the gate electrode (which can be made of stacked metal layers) and the gate insulating layer (often called a gate oxide or gate dielectric), and between the source and drain. Sze-1981, Ex.1413, 433-34, Fig. 3 (below); Plummer, Ex.1333, 71-76, Fig. 1-11 (further below).

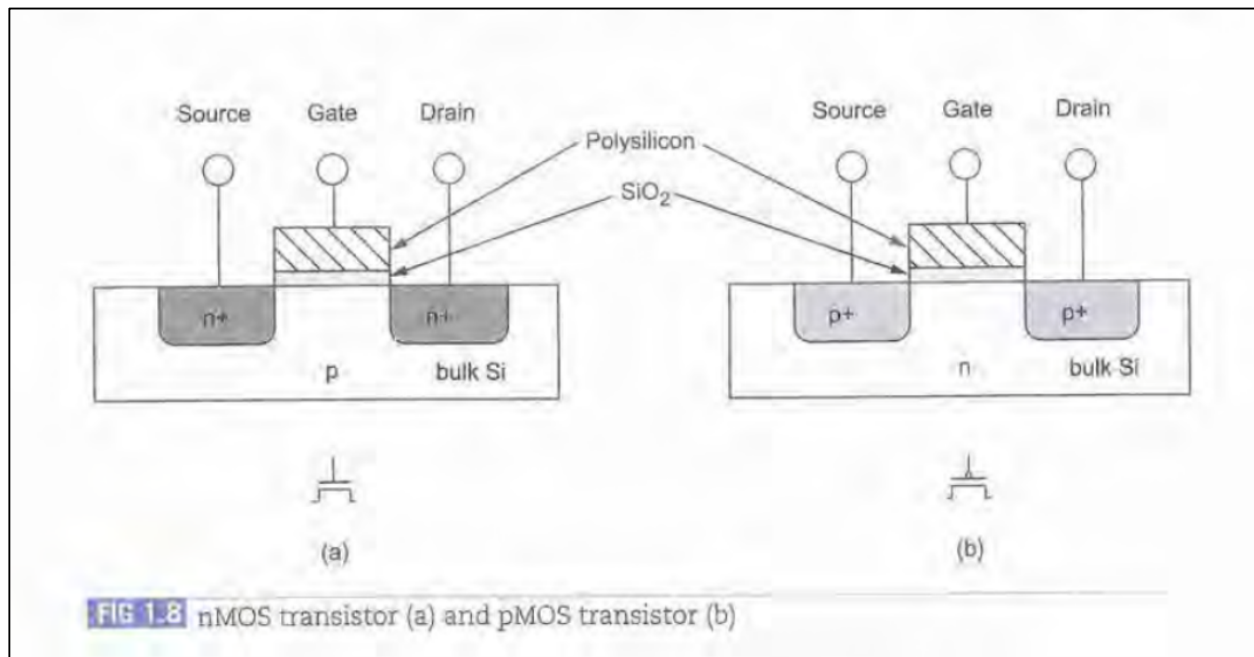


Sze-1981, Ex.1413, Fig. 3



Plummer, Ex.1333, Fig. 1-11

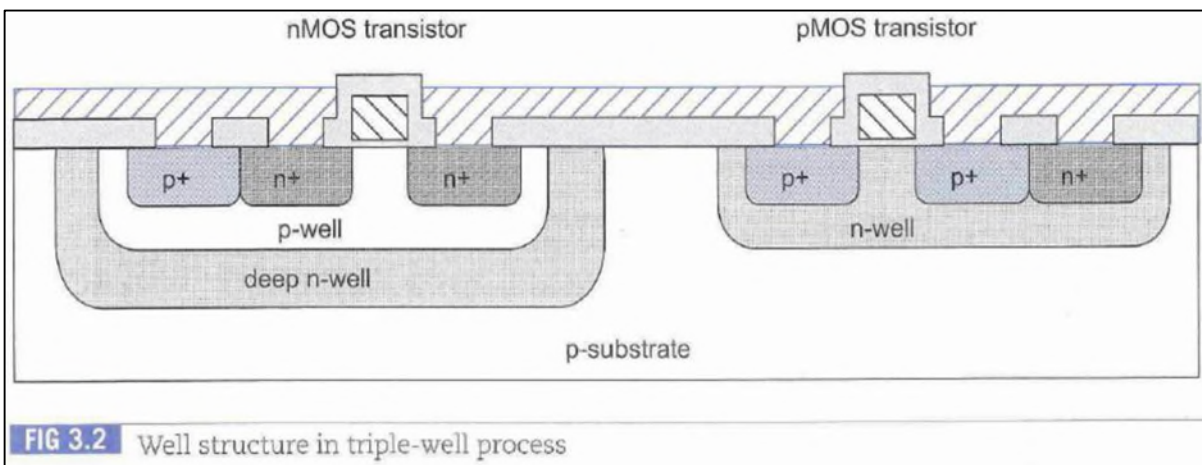
35. MOSFETs are characterized by the material used in the source and drain. A MOSFET with source/drain regions made from “p-type” material is known as a PMOS or p-FET, while a MOSFET with source/drain regions made from “n-type” material is known as a NMOS or n-FET. Thus, MOSFETs generally include a gate electrode, a gate insulating layer, and “the silicon wafer, also called the substrate, body or bulk.” Weste, Ex.1341, 8. An nMOS transistor “is built with a p-type body and has regions of n-type semiconductor adjacent to the gate called the source and drain.” *Id.*, 8 (emphasis omitted), FIG. 1.8(a). A pMOS transistor “is just the opposite, consisting of p-type source and drain regions with an n-type body.” *Id.*



Weste, Ex.1341, Fig. 1.8

Id., 8, FIG. 1.8(b) (above right).

36. In the mid-1980s, complementary MOS (CMOS) devices became popular, which have both PMOS (p-FET) and NMOS (n-FET) transistors on the same substrate or integrated circuit (IC). In such devices, the active areas (and associated transistors) are generally formed in regions called “wells,” and a transistor can even have more than one well, as seen below. See Weste, Ex.1341, 117-18, Fig. 3.2 (below).

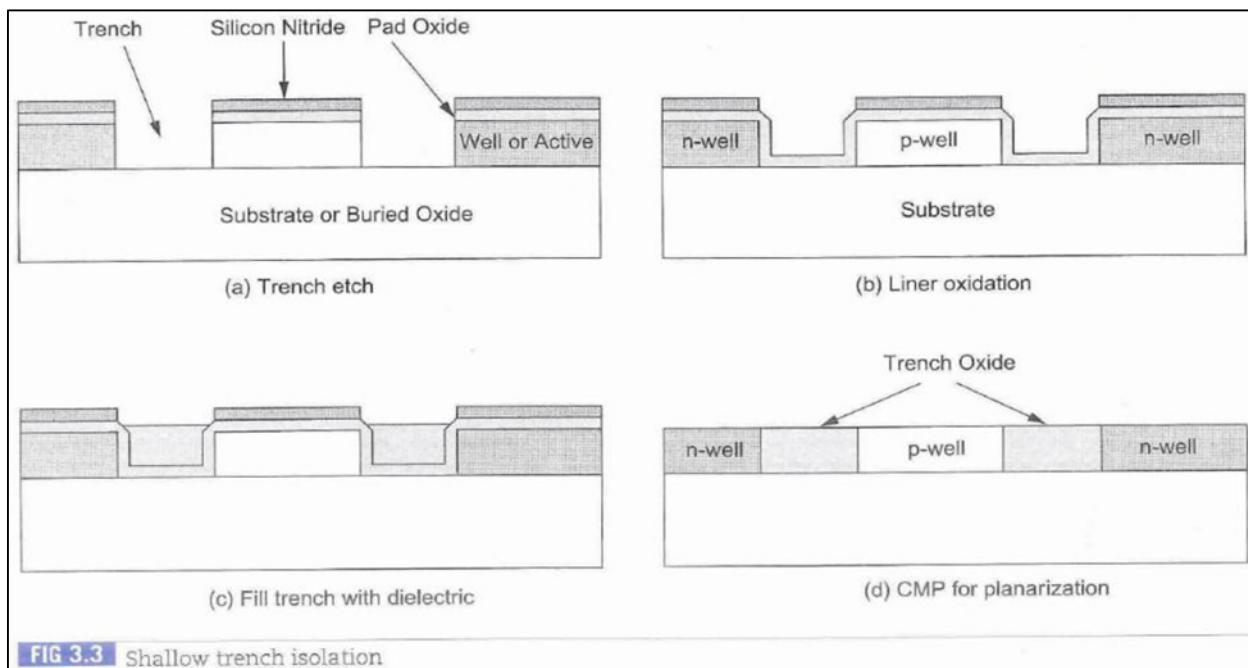


Weste, Ex.1341, Fig. 3.2

37. Impurities known as “dopants” are added to the active areas and wells to add charge carriers and tailor the electrical properties of these regions, such as their conductivity. The wells have opposite dopant types to the dopants of the source/drain. As such, an n-FET is formed in a p-well, and a p-FET is formed in an n-well. See Weste, Ex.1341, 8, Fig. 1.8(b).

38. With respect to dopants, charge carriers can be electrons (which are negatively charged) or holes (which are positively charged). When a region is doped with p-type dopants (like boron), the holes are majority carriers and the electrons are minority carriers. See Weste, Ex.1341, 7; Plummer, Ex.1333, 17. When a region is doped with n-type dopants (like arsenic), the electrons are majority carriers and the holes are minority carriers. See Weste, Ex.1341, 7; Plummer, Ex.1333, 17 (“The electrons or holes are introduced on a one for one basis by the dopants.”).

39. One issue with ICs relates to forming multiple devices on the same chip, and often it is necessary to isolate two structures from each other to ensure proper operation on the chip. One example of this isolation is forming a shallow trench isolation on the substrate between devices. *See Weste, Ex.1341, 117.* In the example below, a trench is etched between a p and n-well to form the shallow trench isolation. *Id.*, 119, Fig. 3.3 (below).



Weste, Ex.1341, Fig. 3.3

40. Once the dopants are added, or implanted, into the silicon substrate, they need to be annealed, for example to repair the silicon crystal lattice from any damage caused by the dopant implantation. Plummer, Ex.1333, 81-82. “Because the ion implantation process creates damage, most dopants are not electrically active at the end of the implantation.” *Id.*, 470. A rapid thermal anneal, often at temperatures over

1000 degrees Celsius, can activate the dopants and repair some of the damage done by implantation. *Id.*, 81. Annealing can also cause diffusion of the implanted dopants throughout the substrate (and in certain circumstances, other layers of the device). The interaction of the implanted dopants between the source/drain, the gate electrode and the gate insulating layer, and the channel were all well understood by a POSITA long before the priority date of the challenged patents. In fact, a POSITA would often use the various interactions of the manufacturing process, for example the shape of the source/drain after dopant implantation and annealing, to improve and optimize the performance of the semiconductor device, as discussed further below.

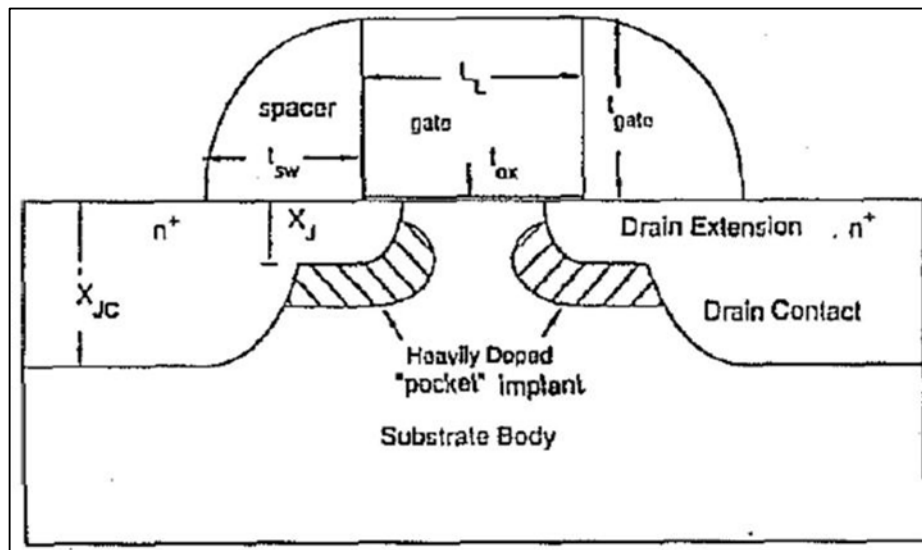
41. For example, varying the amount of dopants at different positions in the semiconductor device can have significant impacts on the device's performance. Where a source/drain may be heavily doped, other areas may only be lightly doped. As one example, the prior art has recognized that as transistors continue to scale down in size, using source and drain extensions may provide certain benefits, and these extensions can have varying dopant levels, including what are commonly referred to as lightly doped drain (LDD) and highly doped drain (HDD). Plummer, Ex.1333, 77; Rodder, Ex.1323, 2:61-62, 3:65-67.

42. Source/drain extensions were known to assist in suppressing short channel effects of scaled-down transistors by varying the dopants and having a gradual transition in the electrical field between the source, the source extension, the

channel, the drain extension, and the drain. Plummer, Ex.1333, 77-78 (using a LDD “allows the drain voltage to be dropped over larger distance than would be the case if an abrupt N⁺P junction were formed” and even “modest reductions in the field strength obtained through the LDD structure can make a significant difference in device reliability”).

43. As I discuss further below, sidewall structures placed on the edge of gate electrodes can serve many purposes, including to control the shape and position of source/drain extensions after annealing of the implanted dopants, as well as the overlap of the extension regions and the gate/gate insulating film. *See* Plummer, Ex.1333, 78.

44. As another example of varying dopants, the prior art also taught using pocket or halo implants to further mitigate the short channel effect as transistor sizes decreased. Pocket implants are placed below the channel region, as shown below. Wolf-4, Ex.1334, 219-20, Fig. 5-27 (below).



Wolf-4, Ex.1334, Fig. 5-27

45. In this example, the pocket implants are doped opposite of the source/drain and source/drain extension. *Id.*, 219 (“Precise control of the placement and dose of this implant within the transistor-structure is needed to obtain the intended enhancements.”).

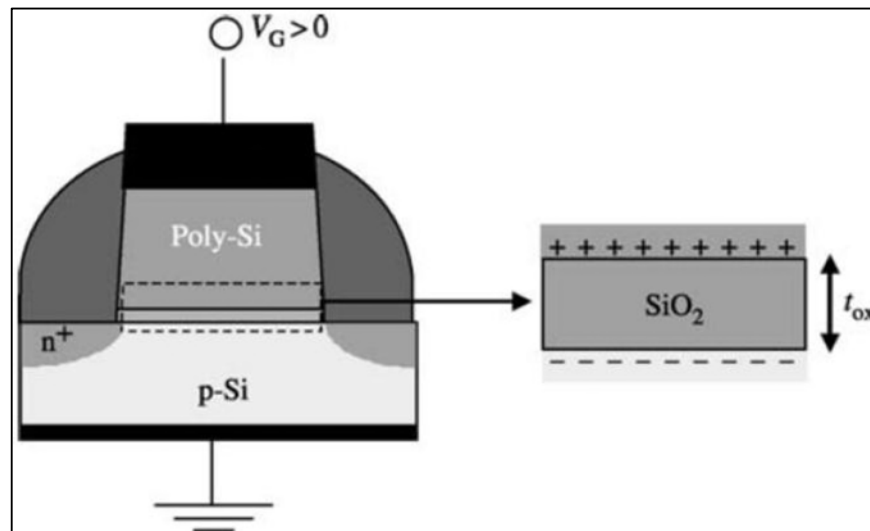
B. Gate Insulating Films & High-k Materials

46. The gate insulating film or gate dielectric isolates the gate electrode from the channel. Plummer, Ex.1333, 288. Silicon dioxide was primarily used as the gate dielectric material for many years (*id.*, 53), but silicon dioxide films presented problems when reduced in thickness for smaller and smaller transistors. In particular, “in ultrathin SiO₂ gate layers (thickness typically below 3 nm) charge carriers can flow through the gate dielectric by quantum mechanical tunnelling mechanism.” Houssa, Ex.1213, 5; *see also* Wolf-4, Ex.1334, 4-5.

47. The MOS transistor, from an electrical perspective, “behaves like parallel plate capacitor when gate voltage V_G is applied to the gate charges on the metal are compensated by opposite charges in the semiconductor, these latter charges forming the channel connecting the source and the drain of the transistor as illustrated in figure 1.1.4.” Houssa, Ex.1213, 8, Fig. 1.1.4 (below). The capacitance C can thus be represented by the following equation:

$$C = \frac{A\epsilon_r\epsilon_0}{t_{ox}} \quad (1.1.1)$$

48. In this equation, “ A is the capacitor area, ϵ_r the relative dielectric constant of the material (3.9 for SiO_2), ϵ_0 the permittivity of free space ($8.85 \times 10^{-12} \text{ F m}^{-1}$) and t_{ox} the gate oxide thickness.” Houssa, Ex.1213, 8. From this formula, the gate oxide thickness has an inverse relationship to capacitance: decreasing the gate oxide thickness increases the capacitance of the structure, with a corresponding “increase in the number of charges in the channel for a fixed value of V_G .” *Id.*



Houssa, Ex.1213, Fig. 1.1.4

49. In practical uses, however, problems occur when decreasing the gate oxide thickness of silicon dioxide past a certain point. Houssa, Ex.1213, 8. As one prior art textbook proposed, “[a]n alternative way of increasing the capacitance is to use an insulator with a higher relative dielectric constant than SiO₂ (it should be noticed that the relative dielectric constant is also represented by the letter k and one speaks about high-k materials)” *Id.*, 8-9. “One could then use a thicker gate layer and, hopefully, reduce the leakage current flowing through the structure and also improve the reliability of the gate dielectric.” *Id.*

50. Equivalent oxide thickness (EOT) is one measure of high-k gate dielectrics. The EOT of a high-k material “is defined as the thickness of the SiO₂ layer that would be required to achieve the same capacitance density as the high-k material in consideration” (Houssa, Ex.1213, 9), which can be represented by the following equation:

$$\frac{t_{eq}}{\epsilon_{r,SiO_2}} = \frac{t_{high-\kappa}}{\epsilon_{r,high-\kappa}} \quad (1.1.2)$$

51. In this equation, “ t_{high-k} and $\epsilon_{r,high-k}$ are the thickness and relative dielectric constant of the high-k material, respectively.” *Id.* In one example shown by Houssa, “using ZrO_2 as gate dielectric ($\epsilon_r \approx 20$) would allow us to use a 5.1 nm thick layer in order to achieve a capacitance equivalent to a 1 nm thick SiO_2 layer; the equivalent oxide thickness of this ZrO_2 layer is thus 1 nm.” *Id.*

52. But make no mistake, more than just a hope, the use of high-k gate dielectrics were a well-known, well-understood, and well-documented component to improve transistor performance as a substitute for silicon dioxide gate dielectrics, especially as transistors continued to decrease in size in the early 2000s. Long before 2005, numerous industry publications and other prior art readily recognized the advantages of using high-k materials as a gate dielectric.

53. In 2002, for example, numerous industry papers identified high-k materials, and hafnium oxide HfO_2 in particular, as a significant contributor to increased transistor performance. A paper by Rim et al. titled “Mobility Enhancement in Strained Si NMOSFETs with HfO_2 Gate Dielectrics” recognized that POSITAs had already been looking to high-k materials to solve known problems: “[g]ate leakage reduction in ultra thin gate dielectric is the main motivation for the search of

high-k materials.” Rim-2002, Ex.1109, Introduction; *see also id.*, Conclusion (“Strained Si NFETs with high-K dielectrics exhibit significantly enhanced NFET mobility, even over the universal mobility of the SiO₂/bulk Si devices, and hold the promise for the best trade-off between mobility and gate leakage reduction, which is especially attractive for low power, high performance CMOS technology.”). Another article at the same industry conference concluded that “[h]igh-temperature FG annealing improved channel carrier mobility as well as subthreshold slopes in both N and PMOSFET with HfO₂ gate dielectrics,” which are “advantageous in achieving large on current while suppressing off current, and give more flexibility in V_t adjustment.” Onishi-2002, Ex.1107, Conclusion.

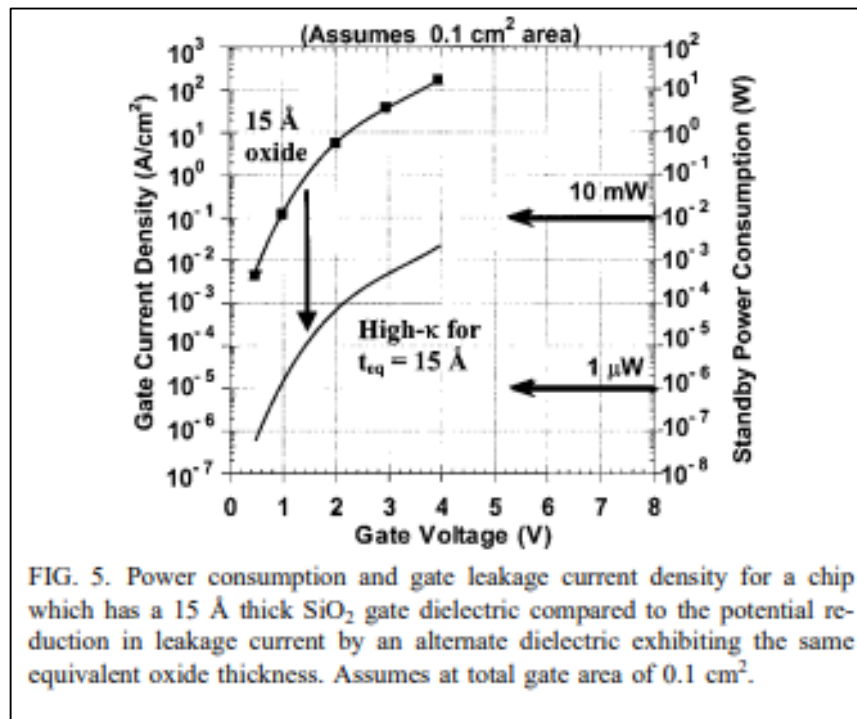
54. Yet another article at the same conference by Pidin et al., titled “Low Standby Power CMOS with HfO₂ Gate Oxide for 100-nm Generation,” concluded that HfO₂ was particularly suited for low standby current applications. Pidin-2002, Ex.1108, Conclusion (“55-nm CMOS with 3-nm HfO₂ gate dielectric was fabricated using conventional process flow with high-temperature anneal of $\geq 1000^{\circ}\text{C}$ and cobalt silicide. Gate current reduction of more than 3 orders of magnitude was achieved and low off-state current devices were obtained demonstrating very promising characteristics of HfO₂ for low standby current applications.”).

55. But more than just the structure and use of high-k materials, the industry had already begun optimizing the process for making transistors with high-k gate

dielectrics, with one article from the 2002 VLSI Symposium comparing two gate first approaches using HfO₂, one via physical vapor deposition and another via chemical vapor deposition. *See* Lee-2002, Ex.1105, Conclusion (“Compared with PVD TaN devices, the CVD TaN/HfO₂ devices exhibit lower leakage current and CV hysteresis, superior interface properties, higher transconductance, and superior effective electron and hole mobility.”).

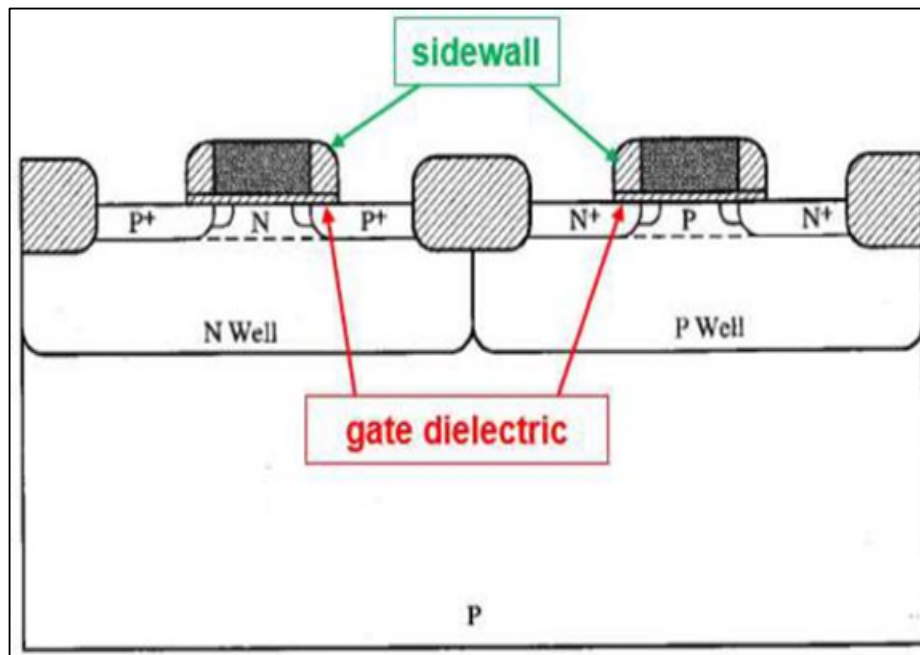
56. Numerous other prior art references recognized the ability of high-k gate dielectrics to make up for the shortcomings of too-thin silicon dioxide gate dielectrics. One article in the Journal of Applied Physics titled “High-k Gate Dielectrics: Current Status and Materials Properties Considerations” recognized that already by 2001 “much work has been done on high-k metal oxides as a means to provide a substantially thicker (physical thickness) dielectric for reduced leakage and improved gate capacitance.” Wilk, Ex.1318, 5250; *see also* Wolf-4, Ex.1334, 146-47 (“The use of high-k dielectrics as the gate dielectric in submicron MOSFET structures also improves other device characteristics,” including in threshold voltage V_t and in the subthreshold-swing S_t .”).

57. For example, as shown by Figure 5 below in Wilk, using high-k materials in place of silicon dioxide for the gate dielectric improved both power consumption and gate leakage current.



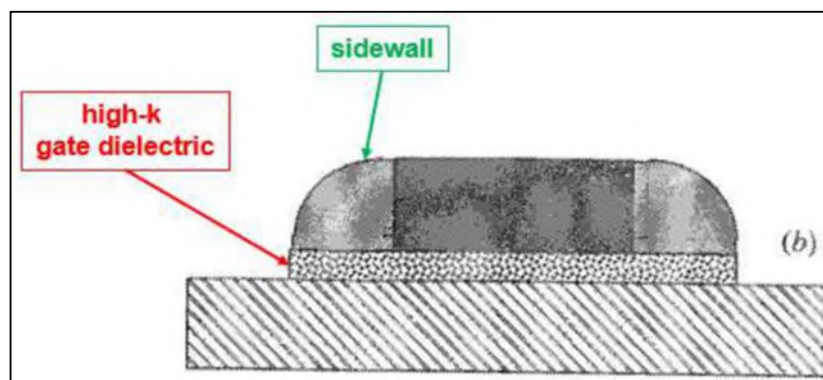
Wilk, Ex.1318, Fig. 5.

58. Not only did the prior art recognize the use of high-k materials as a substitute for silicon dioxide gate dielectrics, but the prior art also showed it was common to extend the gate dielectric out from underneath the gate electrode to underneath the sidewalls. For example, in Figure 2-34 below in Plummer, the gate dielectric is wider than the gate electrode.



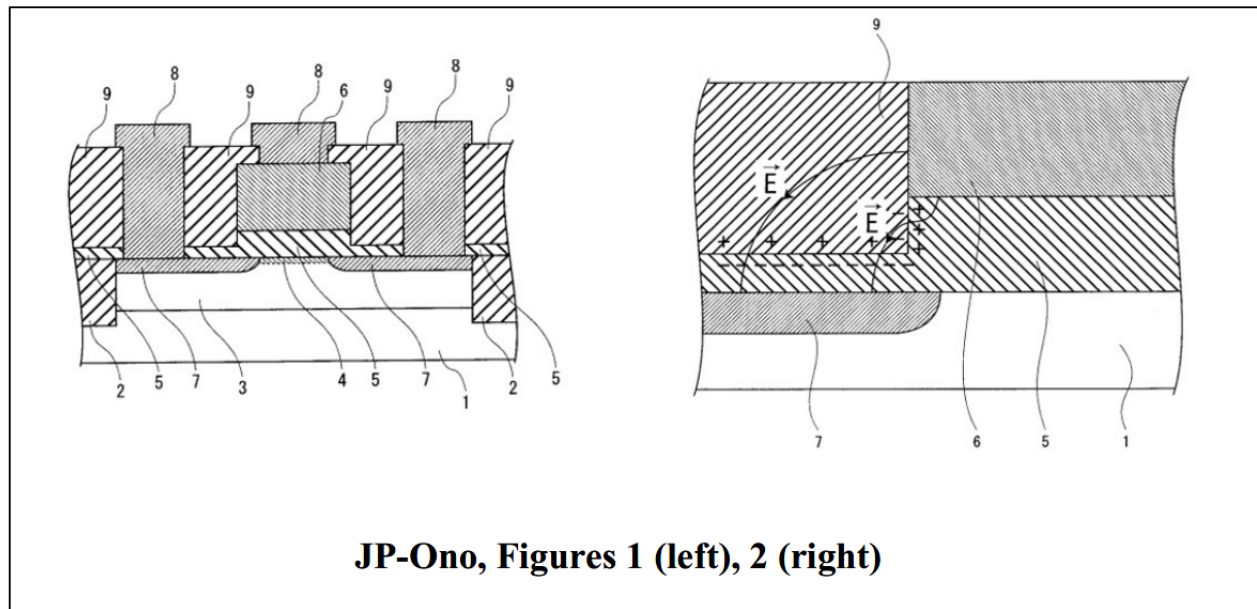
Plummer, Ex.1333, Fig. 2-34

59. As another textbook example, Houssa shows using HfO_2 as the high-k gate dielectric, with and without extending the gate dielectric underneath the sidewalls. Houssa explains that by extending the gate dielectric “with the approach of figure 5.1.9(b), the etch requirements are relaxed but they will require LDD implants through the high-k layer.” Houssa, Ex.1213, 510, Fig. 5.1.9(b).



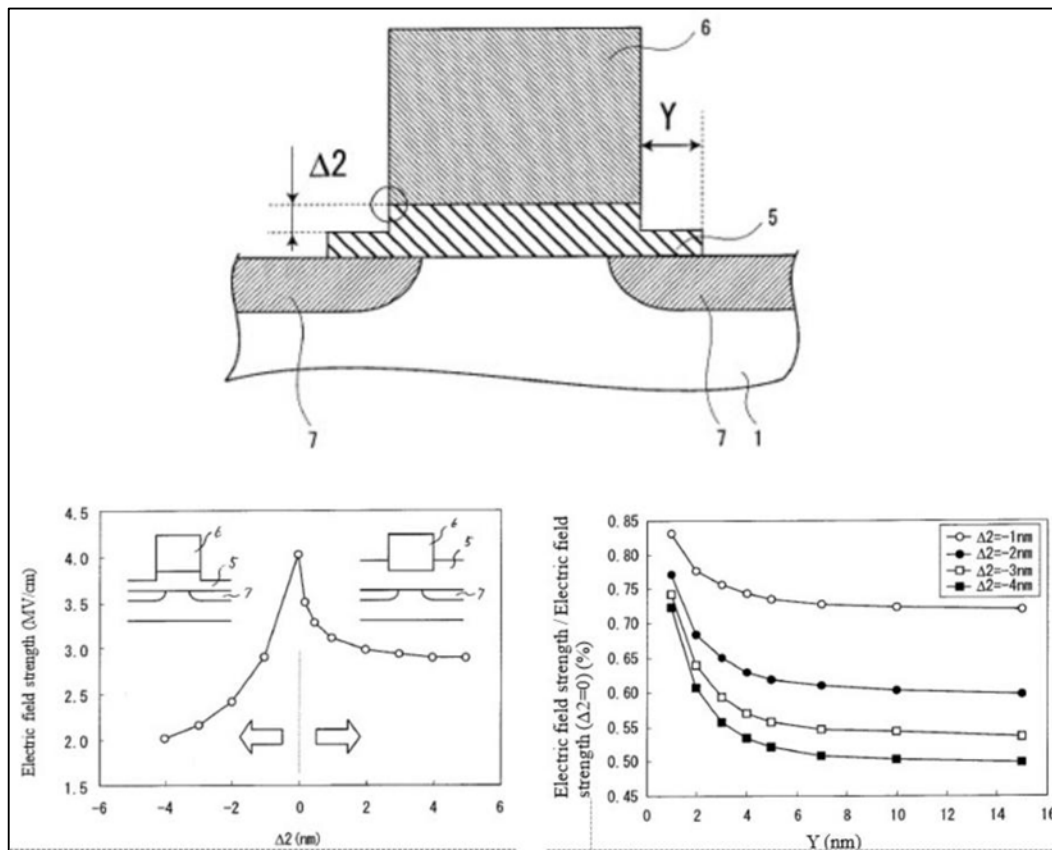
Houssa, Ex.1213, Fig. 5.1.9(b)

60. Japanese Publication No. 2005/064190 by Ono, et al. (“JP-Ono”), published on March 11, 2005 and described some of the known benefits of expanding the high-k gate dielectric wider than the gate electrode, including that “protruding the gate insulating film outside the gate electrode during processing results in higher values of the electric field.” JP-Ono, Ex.1340, ¶7. Further, JP-Ono suggests that extending the gate dielectric over the source/drain region, as well as reducing the thickness of the gate dielectric over the source/drain regions compared with under the gate electrode, “mitigate[s] the electric field at the lower end corner of the gate electrode 6” and “suppresses problems such as insulation breakdown and decreased reliability of the gate insulating film.” *Id.*, Abstract. Specifically, JP-Ono detailed how thinning the gate dielectric over the source/drain region minimizes the electric field at the edge of the gate. *Id.*, ¶¶29-32, Figs.1-2.



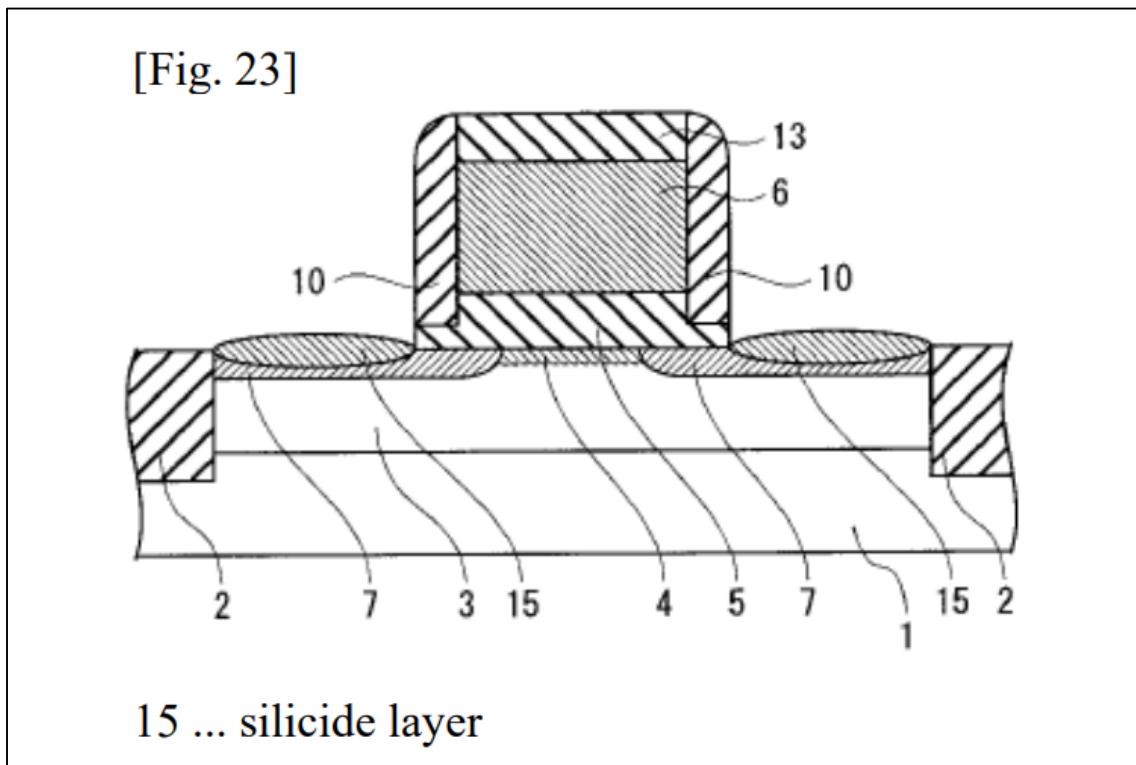
JP-Ono, Figures 1 (left), 2 (right)

61. Further, JP-Ono studied how varying the thickness and length of the gate dielectric over the source/drain regions affects the electric field distribution. Figure 4 shows that when the gate dielectric over the source/drain region is the same thickness as under the gate, *e.g.* at 0 $\Delta 2$, the electric field is strongest. JP-Ono, Ex.1340, ¶¶29-32, Figs. 1-2. As the gate dielectric becomes thinner compared with under the gate electrode, *e.g.* when $\Delta 2$ is negative, the electric field weakens more than with a thicker gate dielectric, which favors a thinner dielectric over the source/drain regions. *Id.*, ¶35. Figure 24 further shows that the electric field is further reduced as the gate dielectric protrudes farther from the corner of the gate, i.e., as Y increases. *Id.*, ¶87.



JP-Ono, Ex.1340, Figs. 3 (top), 4 (bottom-left), 24 (bottom-right)

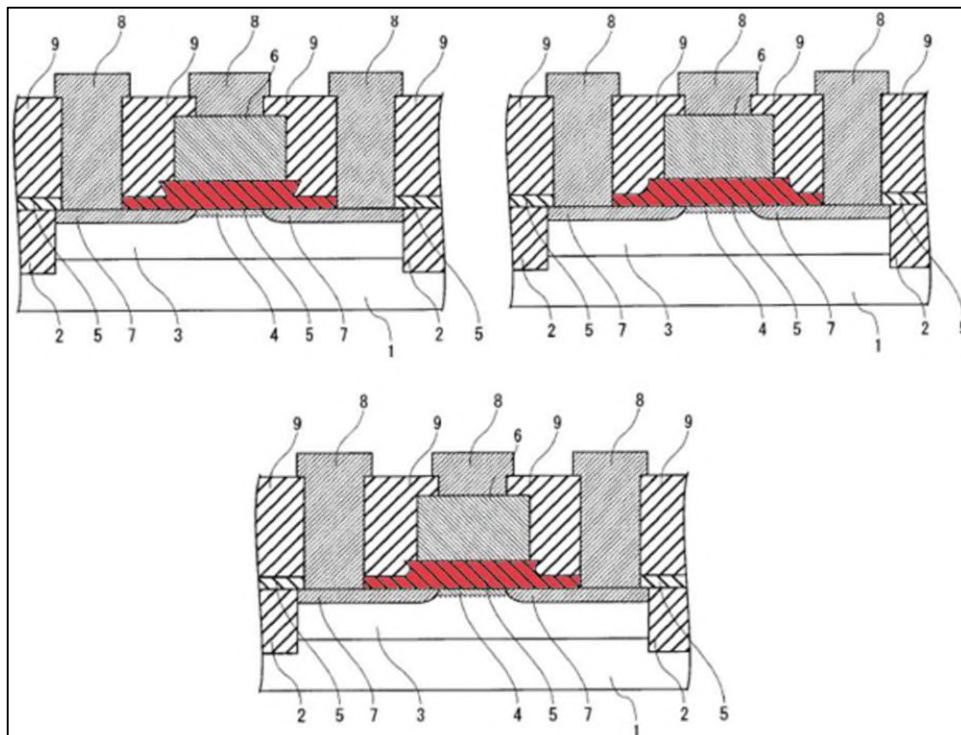
62. These improvements are explicitly taught in a FET having a gate sidewall made of “materials like silicon oxide, silicon nitride, or silicon oxynitride,” as shown Figure 23 below. JP-Ono, Ex.1340, ¶83.



JP-Ono, Ex.1340, Fig. 23

63. Thus, JP-Ono teaches a POSITA the benefits of changing not only the location of the gate dielectric, *e.g.* outside the gate electrode, but also the shape of the gate dielectric, *e.g.* with thinner ends over the source/drain regions than underneath the gate electrode. In reference to Figure 23, JP-Ono explained that “it is not essential for the side of the gate insulating film 5 to be located inside or outside of the outer surface of the gate-side wall 10,” but instead, the gate dielectric can be located both farther than the end of the sidewall, or closer than the end of the sidewall, with similar benefits. JP-Ono, Ex.1340, ¶83. (“Therefore, it is preferable that the side of the gate insulating film does not protrude too far outward [or inward] from the outer surface of the gate-side wall.”).

64. JP-Ono demonstrated several different shapes for the protruding portions of the gate dielectric in Figures 36-44, as can be seen by some examples below in red. JP-Ono, Ex.1340, Figs. 38, 41-42 (below). “By changing the shape of the gate insulating film near the lower corner of the gate electrode, as shown in the various examples here, it is possible to adjust the capacitance formed between the gate electrode 6 and the source-drain region 7, allowing for optimization.” *Id.*, ¶108. Although shown without any sidewalls, JP-Ono explained that “gate-side wall 10 may be removed after processing the gate insulating film, or it may be left as it is.” *Id.*, ¶103.



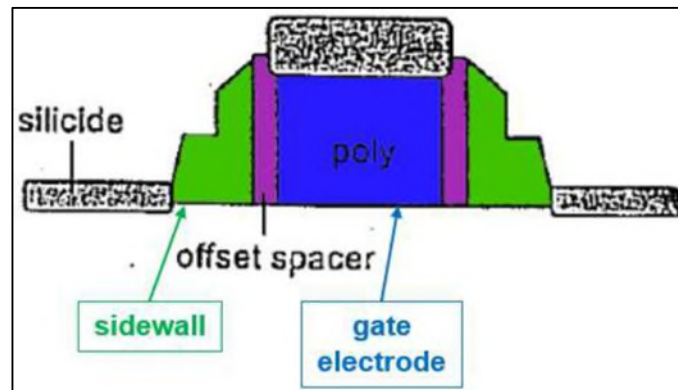
JP-Ono, Ex.1340, Figs. 38 (top-left), 41 (top-right), 42 (bottom)

C. Sidewall Structures

65. Varying the sidewall structure on the sides of the gate electrode is another way a POSITA had to further optimize device performance in the prior art. Sidewalls, also referred to as spacers or sidewall spacers, are formed on the side of the gate electrode for a variety of reasons. As discussed above, various sidewall structures may be used on the gate electrode to control the shape and position of source/drain extensions after annealing of the implanted dopants, as well as the overlap of the extension regions and the gate/gate insulating film. See Houssa, Ex.1213, 511; Weste, Ex.1341, 122; Wolf-4, Ex.1334, 9, 217, 219; Plummer, Ex.1333, 78. Alternatively, sidewall spacers can prevent shorts between the source/drain and the gate, for example if the source/drain regions have silicide portions. Plummer, Ex.1333, 742. These spacers are often made with silicon dioxide or silicon nitride, or combinations of multiple oxide and nitride layers. Houssa, Ex.1213, 511-12.

66. Varying the sidewall structure to control the source/drain extensions is one example of device optimization. As one textbook noted, “it has also been reported that the amount of overlap of the SDE-region with the gate-edge is also critical for optimum device performance.” Wolf-4, Ex.1334, 217. As shown in Wolf’s Figure 5-25 below, a POSITA knew that varying the size of the spacer at the gate electrode would affect formation of the source/drain extension and the resulting

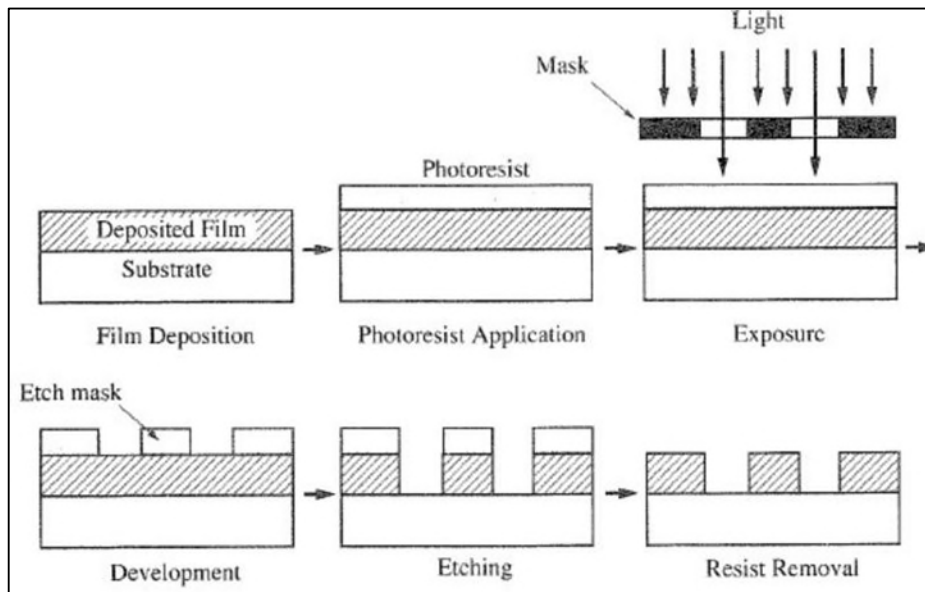
overlap with the gate edge: “an offset-spacer is fabricated on the side of the gate after the gate-poly is etched (but before the SDE implant step is carried out,” with the spacer width “varied from zero (no-spacer) to some upper-bound (e.g., 50-nm)” to control gate overlap and optimize device performance. *Id.*



Wolf-4, Ex.1334, Fig. 5-25

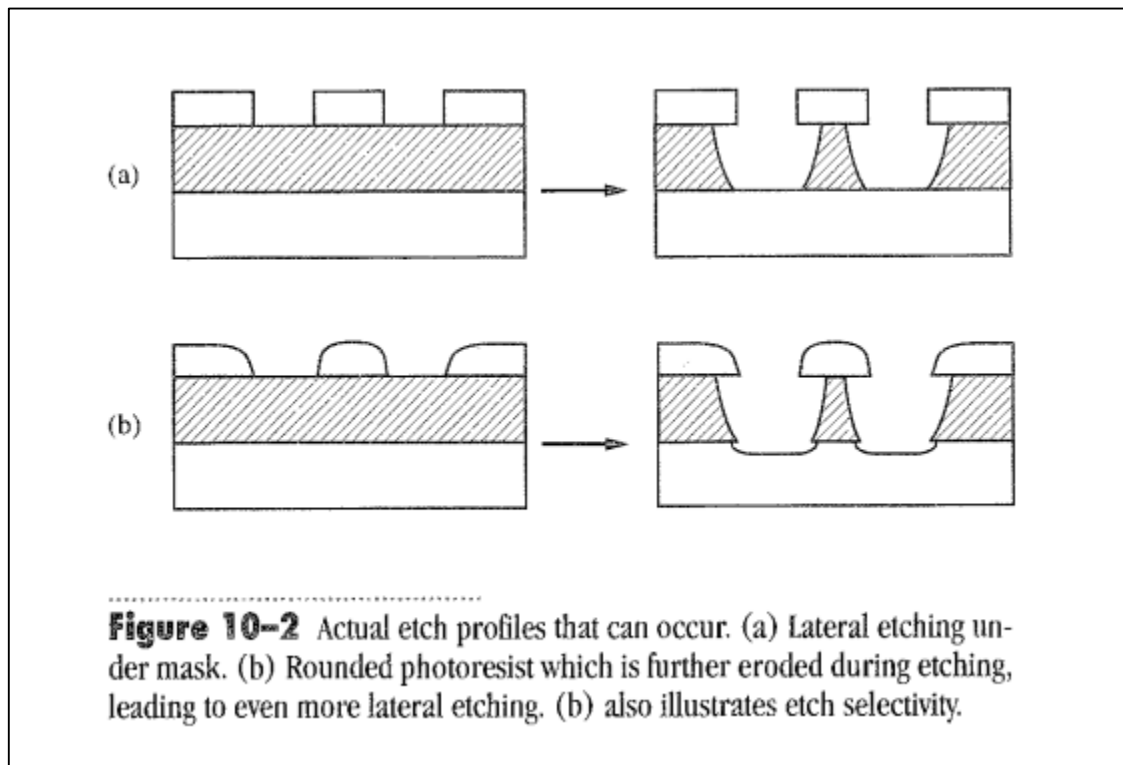
D. Etching

67. The process of manufacturing a semiconductor device, particularly one with varying transistor structures, often involves a series of material deposition and etching, including by deposition of thin films with selective etching to pattern a desired structure. Plummer, Ex.1333, 609-11. For example, a mask may be used in selective portions of a semiconductor device to “mask” or protect the underlying structure from further processing. As seen below, some areas may be masked while other areas are left unprotected such that a subsequent etching step etches the unmasked areas, while leaving the masked areas relatively intact. *Id.*, 609-10, Fig. 10-1.



Plummer, Ex.1333, Fig. 10-1

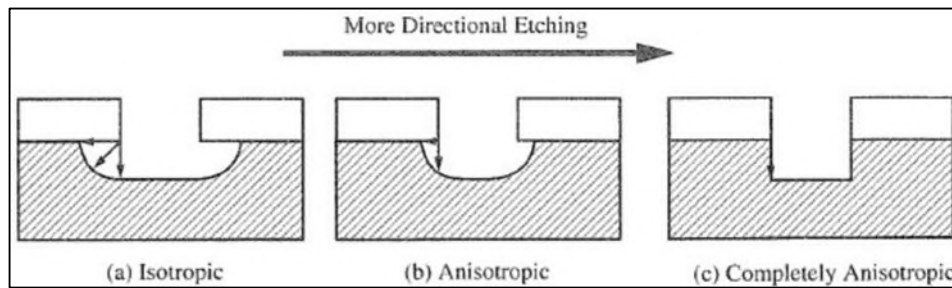
68. A POSITA can further optimize the structure of the semiconductor device by varying the etching process, as some processes are more selective than others. While the ideal etch profile “has perfectly straight sidewalls exactly under the edge of the mask,” as seen above in Figure 10-1, in practice etching has both lateral and vertical components, as seen below in Figure 10-2.



Plummer, Ex.1333, Fig. 10-2

69. Etching is accomplished through both wet and dry processes, where wet etching often entails immersing the wafers in liquid like hydrofluoric acid to perform chemical etching, while dry etching uses plasma instead to etch material through both a physical and chemical process. Plummer, Ex.1333, 609, 612.

70. Under certain circumstance, etching can also be targeted to etch directionally. Anisotropic etching, for instance, is considered a vertical etch with little to no etching in the lateral direction, while isotropic etching has more equal etching rates both vertically and laterally. Plummer, Ex.1333, 610-13. These differences can be seen below in Figure 10-3.



Plummer, Ex.1333, Fig. 10-3

E. Replacement Metal Gate Stacks

71. While the industry recognized the benefits of high-k gate dielectrics, the prior art also recognized that using metal gates on top of high-k gate dielectrics further enhanced transistor performance, particularly as transistor sizes became smaller. When formed on top of high-k gate dielectrics like HfO₂, metal gate stacks addressed issues like Fermi-level pinning, eliminated polysilicon gate depletion, provided lower resistance, enhanced switching speeds, and improved overall transistor performance.

72. For example, a 2002 article by Samavedam et al. titled “Metal Gate MOSFETs with HfO₂ Gate Dielectric” recognized “[m]etal gates will eliminate gate depletion and address other issues like boron penetration and increased gate resistance, which will be aggravated as the poly gate thickness is scaled down.”). Samavedam-2002, Ex.1110, Introduction; *see also id.*, Conclusion (“We have successfully fabricated and characterized HfO₂ n-MOSFETs with TaSiN and PVD TiN gates and p-MOSFETs with CVD and PVD TiN gates using a conventional CMOS process. Metal-gated HfO₂ n-MOSFETs show a 10⁴X gate leakage reduction

compared to poly/SiO₂ devices. Reasonable Ion/I_{off} performance and reliability were observed in PVD TiN/HfO₂ PMOS.”); *see also* Lee-2002, Ex.1105, Introduction (“As CMOS devices are scaled into sub-0.1 um regime, poly-depletion effects and boron penetration become significant concerns. Therefore, metal gate electrodes are being explored to replace the polysilicon gate.”). Just two years later, a 2004 article titled “55nm high mobility SiGe(:C) pMOSFETs with HfO₂ gate dielectric and TiN metal gate for advanced CMOS” concluded that “[f]or the first time, MOS transistors with compressively strained SiGe(:C) channel, metal gate and high-k dielectric are demonstrated down to 55nm gate length,” with significant improvements: “SiGe(:C) surface channel pMOSFETs with HfO₂ gate dielectric exhibit a 10⁴ gate leakage reduction and a 65% mobility enhancement at high transverse effective field (1MV/cm) when compared to the universal SiO₂/Si reference.” Weber-2004, Ex.1111, 42.

73. Other prior art references further recognized the problem of using polysilicon gates with high-k gate dielectrics specifically, or decreased transistor size in general. As gate dielectrics grew smaller consistent with transistor sizes, the polysilicon depletion effect worsened. Saito631, Ex.1518, 1:31-34; Hou, Ex.1519, 1:36-44. And where a high-k material is substituted for the silicon dioxide gate dielectric with a polysilicon gate electrode, diffusion of the polysilicon dopants into the high-k material can cause a large threshold voltage offset. Colombo, Ex.1520, ¶5;

Kavalieros277, Ex.1515, ¶3. As discussed above, metal gate stacks were considered the next step to address these problems. Saito631, Ex.1518, 1:31-34; Iriyama, Ex.1521, 1:28-34, 1:41-42; ITRS_FEP, Ex.1512, 2-3, 20; ITRS_PIDS, Ex.1216, 1, 3, 27, Fig. PIDS5.

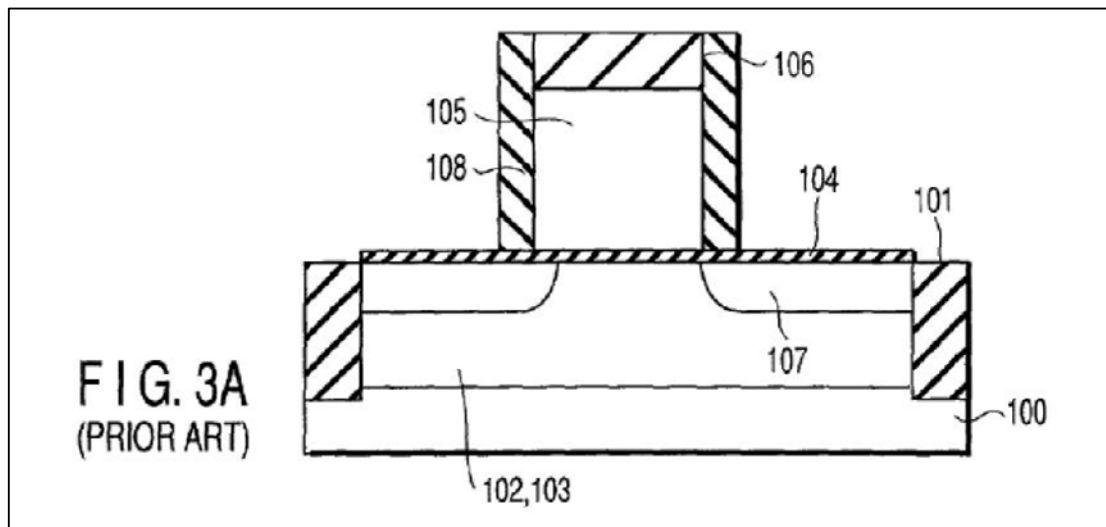
74. In particular, the prior art recognized that metal gates for PMOS and NMOS transistors would need separate metal gate stacks, and replacement metal gates (or gate-last processes) were well known to provide significant benefits compared with gate-first approaches. A material's "work function" is "the minimum energy required to bring an electron from the Fermi level to the vacuum level." Wolf-3, Ex.1229, 117. However, in MOS/MIS structures, the metal is in direct contact with a dielectric, not with the vacuum. Moreover, work functions of metal gates are highly dependent on material properties and interfaces. To differentiate this, an "effective work function" of the metal gate is commonly used to refer to the metal work function as measured (*e.g.*, through the threshold voltage of the device).

75. In a CMOS device, PMOS transistors require a work function greater than about 4.8 eV, while NMOS transistors require a work function of less than about 4.6 eV. Hou, Ex.1519, 1:17-22; Colombo, Ex.1520, ¶¶20-21; ITRS_FEP, Ex.1512, Tbl. FEP4a ($|E_{c,v}-\phi_m|$ (eV) < 0.2). Where the same polysilicon gate electrode can be doped to adjust the work function for both NMOS and PMOS transistors, this is not the case for metal gates. Different metal gate stacks must be used. *See*

Kavalieros277, Ex.1515, ¶3 (“When making a CMOS device that includes metal gate electrodes, it may be necessary to make the NMOS and PMOS gate electrodes from different materials.”).

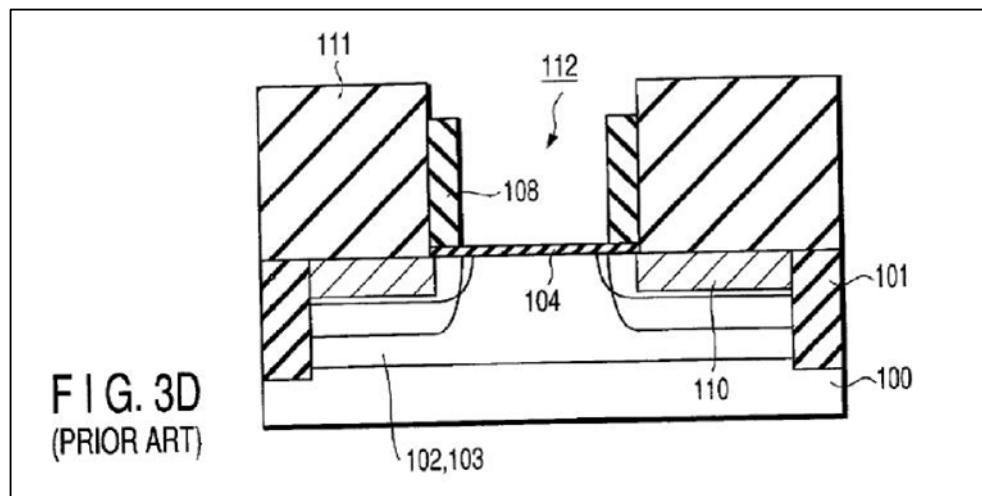
76. Some of the metals considered in the prior art for the PMOS metal gate stack showed less thermal stability than necessary, adversely affecting device performance when subjecting the metal to the high temperatures used to anneal the dopants in the source/drain regions. Hou, Ex.1519, 1:45-57; Iriyama, Ex.1521, 1:41-48.

77. One solution already considered by the prior art was replacement metal gates (“RMG”), which is a “gate-last” approach because a dummy gate is often manufactured first and then replaced by the metal gate. By making the metal gate last, the POSITA avoids subjecting the metal gate stacks to high temperatures during the source/drain annealing (because the annealing is done before placement of the metal gate). As seen below from one prior art reference, source/drain regions (107), the polysilicon dummy gate (105), a SiN film (106), and sidewalls (108) are formed for the NMOS and PMOS transistors before the replacement metal gate. Matsuo, Ex.1522, ¶¶9-10, 16, FIG. 3A.



Matsuo, Ex.1522, FIG. 3A

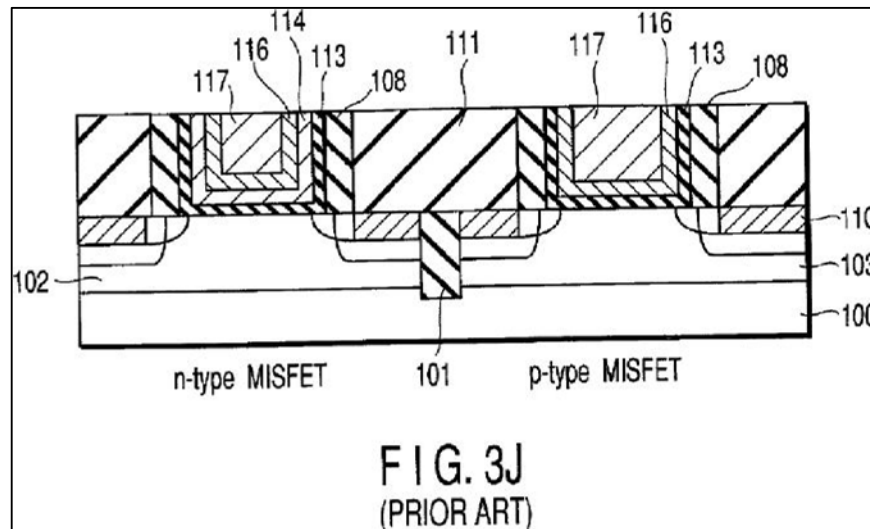
78. Before the dummy gate is replaced, the source/drain regions are doped and annealed. *See Matsuo, Ex.1522, ¶10, FIGS. 3B-C; see also Hou, Ex.1519, 2:8-11; Iriyama, Ex.1521, 1:59-2:6.* As one of the last steps, the dummy gates are removed to allow for placement of the metal gate stack. Matsuo, Ex.1522, ¶¶11-13, FIG. 3D.



Matsuo, Ex.1522, FIG. 3D

79. In this example, after removal of the dummy gate, both the NMOS and PMOS metal gate electrodes are formed, as seen below. Matsuo, Ex.1522, ¶¶12-16,

FIG. 3J. First, gate dielectric (113) is formed, and then metal layers 114, 116, and 117 after. Matsuo, Ex.1522, ¶¶12-16. This sequence can prevent damage to metal gate stacks susceptible to deterioration by high temperature annealing. Iriyama, Ex.1521, 2:22-29.



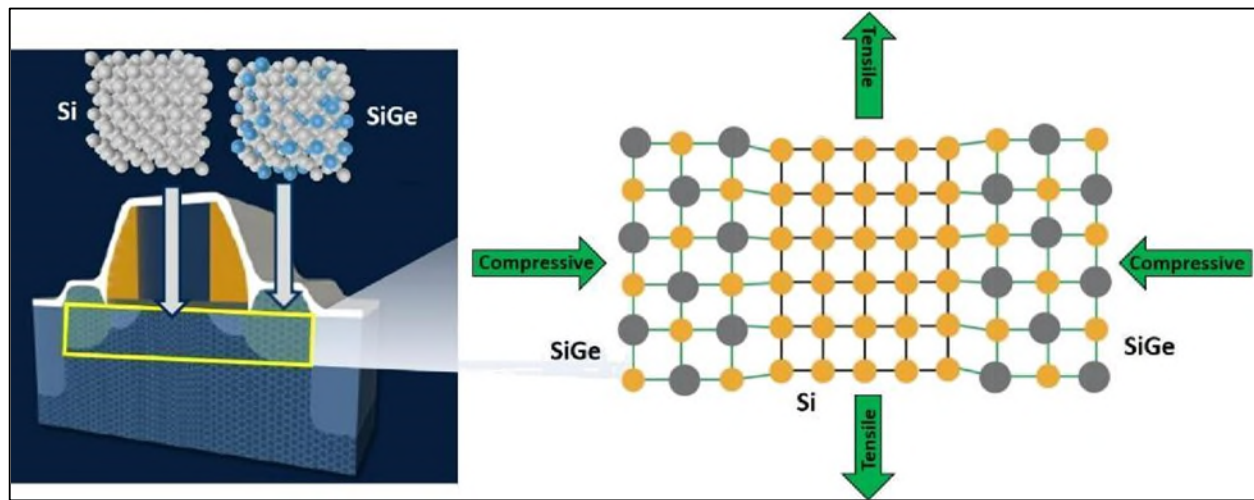
Matsuo, Ex.1522, FIG. 3J

80. In Fig. 3J above, the metal layer 114 is directly formed on the gate dielectric 113 for NMOS gate electrode (shown on the left), but a different metal gate stack is used for the PMOS gate electrode (shown on the right), which does not include metal layer 114. Matsuo, Ex.1522, ¶21. The two gate electrodes thus have different metal work functions, one for NMOS and one for PMOS. Matsuo, Ex.1522, ¶21, FIG. 3J; Hou, Ex.1519, 2:11-14; Iriyama, Ex.1521, 2:10-12; Mistry2007, Ex.1516, 247; Mistry_Presentation, Ex.1517, 16, 18.

F. Strained Silicon

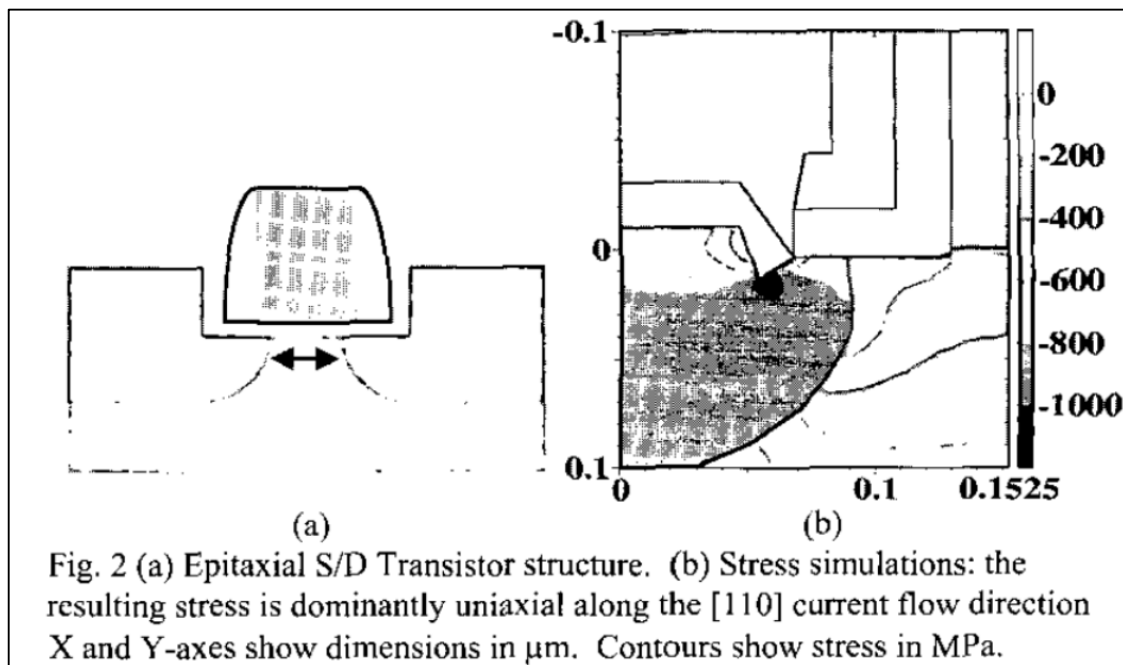
81. In the early 2000s, strained silicon technology was recognized as another mechanism to improve transistor performance as transistor sizes continued to shrink. Until the large-scale adoption of strained silicon, PMOS transistors used to be slower than NMOS transistors and much effort was spent on improving PMOS transistor performance compared with NMOS transistors. But the prior art quickly realized that compressively strained PMOS transistors could be improved by as much as 50%, leading to a reversal in efforts spent trying to improve NMOS transistors compared with PMOS transistors.

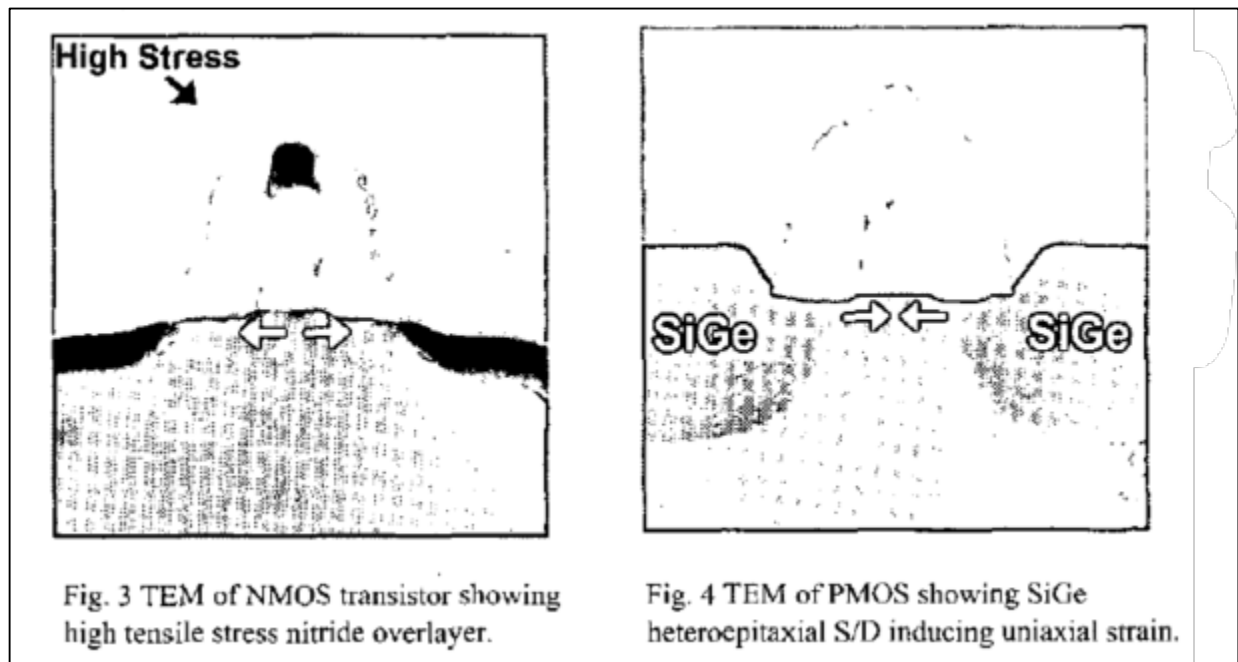
82. Germanium is one source of compressive stress in PMOS transistors. The Ge atom are larger in size than Si atoms, such that silicon-germanium (“SiGe”) can be used in the source/drain regions of PMOS transistors to apply compressive stress to the PMOS channel region. See Thompson-2004, Ex.1523, 1790-96; Sun-2007, Ex.1524, 2. By 2005, SiGe source/drain regions increased PMOS “hole mobility by as much as 50%” (James, Ex.1525, 2), doubling PMOS operating speeds.



83. Numerous prior art references recognized the benefits of strained silicon, for both PMOS and NMOS transistors. For example, in a 2004 paper titled “35% Drive Current Improvement from Recessed-SiGe Drain Extensions on 37 nm Gate Length PMOS,” Chidambaram et al. recognized that “Epitaxial SiGe, grown in recessed Si, has been used to compressively strain the PMOS channel and increase the hole mobility.” Chidambaram-2004, Ex.1104, Introduction; *see id.*, Abstract (“A highly compressive SiGe layer, in close proximity to the channel, results in large hole mobility improvements.”). Another 2004 article by Mistry et al. proclaimed that “[t]he use of strain to improve mobility has been known for 50 years,” concluding that “[u]ni-axial strained silicon has been implemented in a high volume manufacturing 90nm logic technology for the first time, with impressive performance results and improved power scaling.” Mistry-2004, Ex.1106, 50.

84. Where a PMOS transistor benefits from compressive strain, NMOS transistors benefit from tensile stress along the channel region. As seen in Figs. 2-4 from Mistry-2004 (Ex.1106), compressive stress from SiGe source/drain regions on PMOS transistors and tensile stress on NMOS transistors from a high tensile stress nitride overlayer were well known to improve transistor performance.

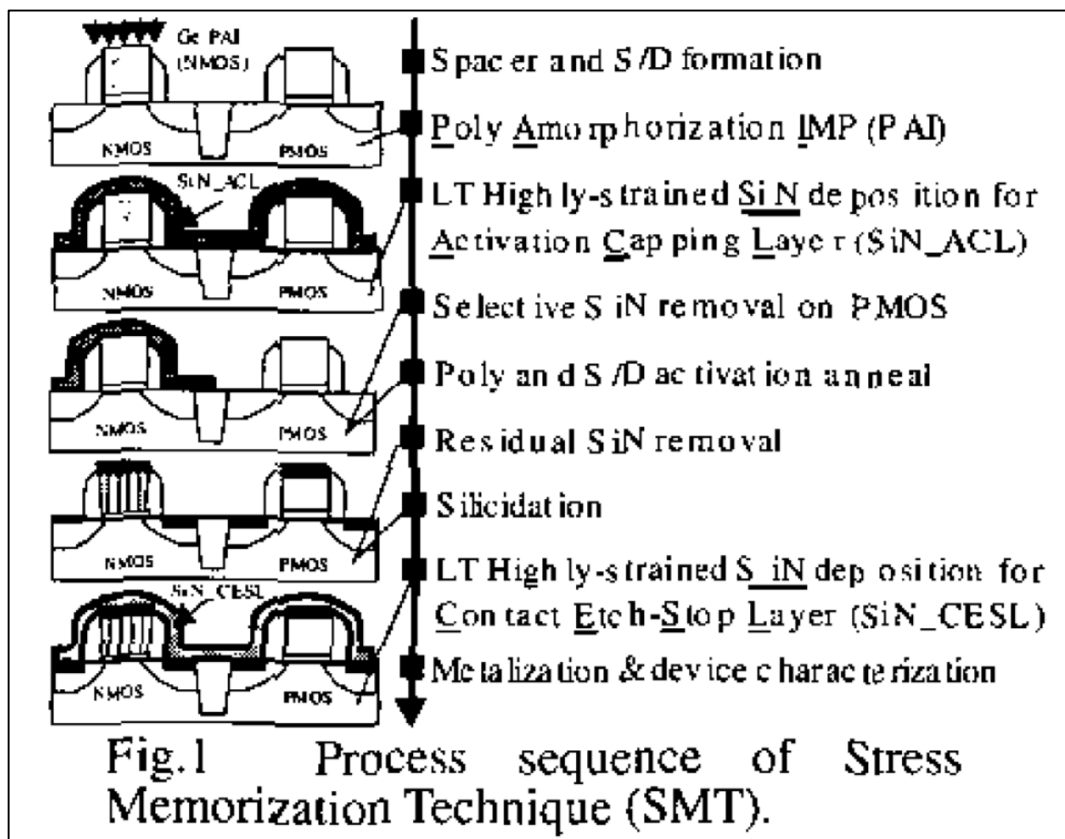




Mistry-2004, Ex.1106, Figs. 2-4

85. In another article that same year by Chen et al. titled “Stress Memorization Technique (SMT) by Selectively Strained-Nitride Capping for Sub-65nm High-Performance Strained-Si Device Application,” the prior art recognized that “[c]hannel stress control has become a critical technique for electron and hole mobility improvements as down scaling the device dimension.” Chen-2004, Ex.1103, Introduction. The article further recognized the tradeoffs inherent in stressing both PMOS and NMOS transistors on the same chip. *Id.* (“In addition, recent studies of high tensile capping layer on top of the silicide have demonstrated the NMOSFET driving current improvement capability, but with the PMOS performance degradation.”).

86. Searching for a cost-conscious method to effectively stress the NMOS transistor without degrading PMOS performance, the article proposed (1) selectively applying a high tensile nitride activation capping layer to the NMOS transistor, and (2) applying a low temperature, high-tensile nitride film as a contact etch stop layer to both the NMOS and PMOS transistors. Chen-2004, Ex.1103, Channel Stress Control by SMT; *see id.*, Introduction (“In this paper, we proposed a novel stress memorized technique (SMT) to improve the device performance without PMOS degradation. A high tensile nitride capping layer acts as a temporary stressor to effectively modulate the channel stress. The stress effect is then enhanced and memorized by well-controlled poly amorphization and re-crystallization procedures. This high tensile nitride capping layer will be removed after the annealing step. Therefore, a much thicker capping layer can be used to increase the stress level without any process limitation to impact the subsequent gap filling process steps.”); *id.*, Channel Stress Control by SMT (“After the silicide formation, the low temperature, high-tensile Nitride film is deposited as Contact-Etch-Stop-Layer (SIN-CESL) to add up the stress effect.”).



Chen-2004, Ex.1103, Fig. 1

87. Additional prior art references taught straining both PMOS and NMOS transistors. See Murthy151, Ex.1526, ¶¶5, 48, 72; James, Ex.1525, 2. For example, it was known to create tensile strain with epitaxial source/drain regions, similar to SiGe for PMOS transistors, but it requires using an atom smaller than silicon, like carbon, to grow a material like silicon carbide (SiC) instead of SiGe,. See Murthy151, Ex.1526, ¶¶5, 48, 72; James, Ex.1525, 2; Bohr, Ex.1527, ¶45.

88. As either an alternative or a supplement to source/drain epitaxy, the semiconductor industry was also already depositing compressive and tensile stress-inducing films over PMOS and NMOS devices to induce a desired strain, as shown

above. *See also* James, Ex.1525, 2, 4; Morin-2007, Ex.1528, 355-56, 367; Hsu823, Ex.1006, ¶3; Jung, Ex.1529, Abstract, ¶90 (“In addition to being deposited as part of a structure to control electron mobility, as shown in FIG. 1B, a stress-tuned silicon nitride film can be deposited for other purposes . . . , for example . . . , to provide an etch stop layer”). A contact etch stop layer (“CESL”) made of silicon nitride was frequently used, and if prepared under certain conditions, a silicon nitride CESL may apply stress to the channel and increase device performance. Hsu823, Ex.1006, ¶3; *see also* Ke, Ex.1531, ¶3 (“A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device.”); Jung, Ex.1529, ¶90 (“In addition to being deposited as part of a structure to control electron mobility, as shown in FIG. 1B, a stress-tuned silicon nitride film can be deposited for other purposes in various steps in the fabrication process, for example (and not by way of limitation), to provide an etch stop layer . . . , as well as to enhance channel mobility in various portions of the device structure.”); Morin-2007, Ex.1528, 355-56. It was well known that a silicon nitride CESL may provide tensile stress, compressive stress, or no stress at all, depending on the process used to apply the layer. *See, e.g.*, Jung, Ex.1529, ¶¶17, 99-100, 131-132, Tbls. IV-V, VII, Fig. 15.

89. As evidenced by the prior art, strained silicon has been well known long before the priority date of the challenged patents. *See, e.g.*, Sun-2007, Ex.1524, 101

(“Strain is a relatively old topic in semiconductor physics.”). In fact, strained silicon was already commercially used in at least three generations of devices by 2007. *See* Thompson-2004, Ex.1523, 1790-91 (Intel’s 90nm devices); Bai-2004, Ex.1532, 657-58 (Intel’s 65nm devices); Mistry2007, Ex.1516, 247-48 (Intel’s 45nm devices); Mistry_Presentation, Ex.1517, 1-19 (same).

G. Stress Buffering Layers

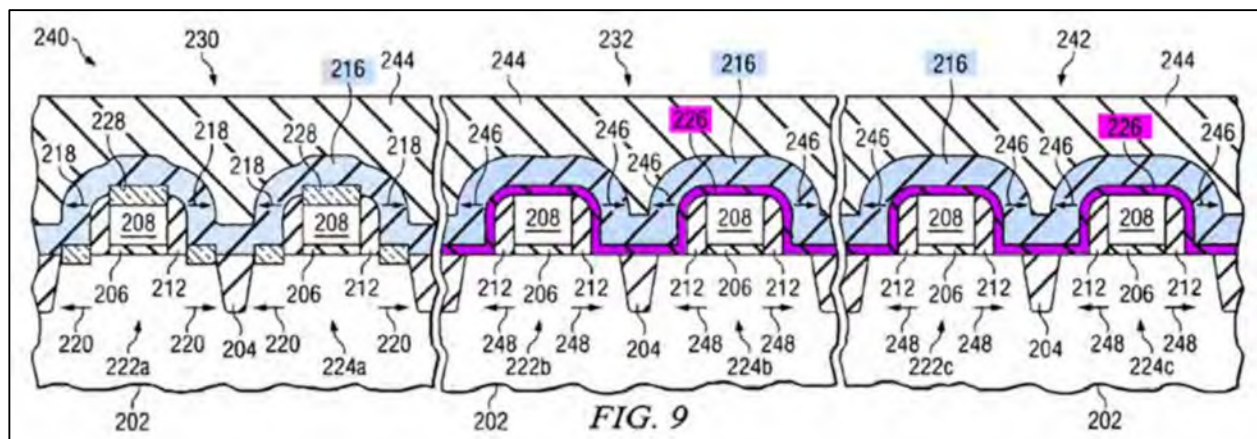
90. Not only were tensile stress contact etch stop layers and SiGe source/drains well known in the prior art, but using buffer layers to mitigate the unwanted effects of those stress layers were also well understood concepts in the prior art.

91. If a tensile contact etch stop layer is deposited over a PMOS device, it generally applies a tensile stress to the channel region. Morin-2007, Ex.1528, 355-56, 367; Doris, Ex.1429, ¶¶5, 13; Hsu823, Ex.1006, ¶37. Where the PMOS device is already compressively stressed, for example with epitaxial SiGe source/drain regions, the tensile stress from the contact etch stop layer offsets some portion of the compressive stress, reducing improvements from the SiGe. Morin-2007, Ex.1528, 355-56, 367; Kavalieros729, Ex.1419, ¶¶2, 26; Doris, Ex.1429, ¶5. The tensile stress may even degrade performance, particularly in PMOS devices without SiGe source/drains. Morin-2007, Ex.1528, 355-56, 367.

92. A POSITA would have understood how to mitigate or negate performance decreases on the PMOS devices from tensile stress. First, a POSITA may choose to apply both a SiGe source/drain to a PMOS device as well as a tensile contact etch stop layer over both the NMOS and PMOS devices to optimize performance of both devices. If the compressive stress from the SiGe is greater than the tensile stress from the contact etch stop layer, the overall compressive stress may still increase PMOS performance, though it may be lessened by the contact etch stop layer. The tradeoff is that the tensile stress improves NMOS transistor performance.

93. A POSITA knew of other ways to mitigate the performance loss. For example, the tensile stress could be reduced for the PMOS device by using a stress-relief layer as a buffer between the SiGe and the tensile contact etch stop layer. Murthy556, Ex.1430, 9:27-29, FIGS. 2, 9, 13-15; Doris, Ex.1429, ¶42, Figs. 1-2, 14-15; Alvarez, Ex.1406, Abstract, ¶43, FIG. 9; Lee870, Ex.1431, ¶¶29, 46-67 (pFET performance degradation “is reduced/eliminated due to the inclusion of the stress relief layer 64 under the nitride layer 70 that reduces the tensile stress in the channel region”), FIGS. 2-5; Cheng810, Ex.1432, ¶¶22-31, Figs. 1B-1F (describing similar); Baik, Ex.1433, ¶37 (“the tensile stresses of the [stressor layer] ha[ve] relatively little or no adverse impact [on] the adjacent PMOS device” because the intermediate layer “reduce[s] the amount of stresses induced in the PMOS device by acting as a physical barrier”).

94. A number of prior art references taught that using an intermediate layer “buffers the large stress inherent silicon nitride layer.” Murthy556, Ex.1430, 9:27-29; Alvarez, Ex.1406, ¶¶49, 66, 68, 77, FIGS. 9-11. As seen below, Alvarez depicts on example with a stress-inducing layer 216 (shown in blue below) that is buffered by stress-control layer 226 (shown in purple) to mitigate the adverse effects of the stress layer on the PMOS devices 224b and 224c (while still improving performance of the NMOS devices).

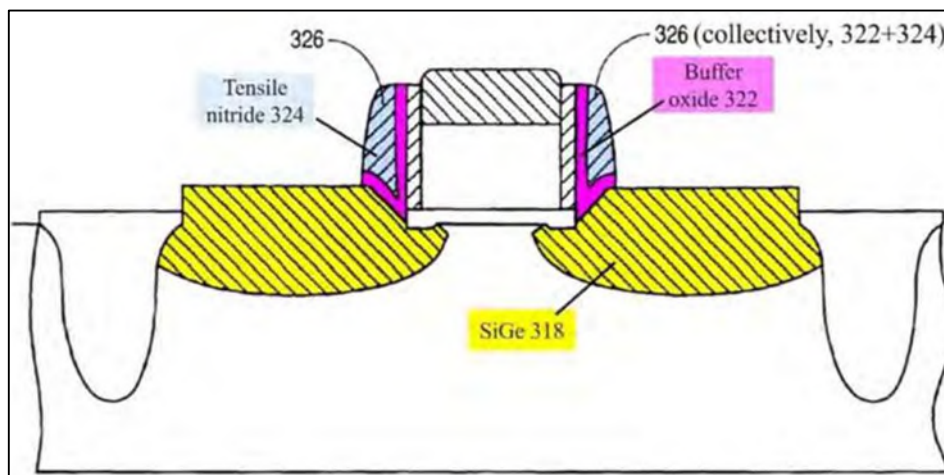


Alvarez, Ex.1406, Fig. 9

95. While the buffer layer above in Figure 9 is shown to be selectively applied, the prior art also explained that these layers could be applied to multiple areas, similar to the one Alvarez discloses (*e.g.*, dual-purpose stress-controlling and masking layer), as a way to save manufacturing cost or complexity. Alvarez, Ex.1406, ¶¶43, 45, 47, 49, 53-55, 78, FIGS. 7-9. This is particular advantageous where “different types of transistors . . . hav[e] different operating parameters and requirements” and/or “due to the performance requirements of transistors in the

particular regions.” Alvarez, Ex.1406, ¶¶27, 32, FIGS. 7-9. Leaving the buffer layer over both the NMOS and PMOS, for example, can reduce the number of fabrication steps and lower the cost of manufacturing. Alvarez, Ex.1406, ¶75; *see also* Alvarez, Ex.1406, ¶¶74, 78.

96. In another example shown below, a buffer layer can be formed immediately between the SiGe source/drain regions and the gate electrode, particularly when raised SiGe source/drain regions are used. *See* Murthy556, Ex.1430, 9:11-15, 9:30-35, FIGS. 7-9; *see also* Miyashita, Ex.1435, ¶¶52-53, FIGS. 1U-1W; Koutny, Ex.1434, ¶¶88, 108 (silicon dioxide liner 485A between tensile stress-inducing layer 504A and source/drain “reduces the cumulative stress” caused by the tensile layer); Doris, Ex.1429, ¶¶34, 42; Cheng810, Ex.1432, ¶30; Lee870, Ex.1431, ¶67.



Murthy556, Ex.1430, Fig. 9 (annotated)

97. These buffer layers can prevent “the tension from materially adversely influencing the charge carrier mobility in the pFET,” such that the pFET “experiences a performance improvement” through “enhanc[ed] hole mobility in the pFET channel” compared to no buffer layer. Doris, Ex.1429, ¶¶34-35, Figs. 2, 14, 15. Using low-stress dielectric films like silicon oxides can create “a neutral buffer layer” between a compressively stressed source/drain and a tensile contact etch stop layer, which allows the compressively stressed region “to have maximum influence on the pFET channel mobility and minimizes the influence of the tensile barrier etch stop layer.” Doris, Ex.1429, ¶42; *see also* Lee870, Ex.1431, ¶¶29, 46-67 (explaining that an intermediate stress relief layer “with neutral stress or opposite stress relative to the [CESL]” reduces or eliminates any pFET performance degradation because it “reduces the tensile stress in the channel region”), FIGS. 2-5; Cheng810, Ex.1432, ¶¶22-31, Figs. 1B-1F.

H. System-on-Chip Design Advancements

98. Threshold voltage is an important characteristic when considering what a particular transistor will be used for. Threshold voltage is the minimum voltage applied at the gate to create a conductive channel between the source and drain—i.e., the ON or active voltage of the transistor. Van Zant, Ex.1211, 526, 474 (“Every MOS transistor is designed to operate at a specific threshold voltage.”). Because PMOS and NMOS transistors use different dopants for the source/drain and source/drain extensions, a POSITA understands that PMOS and NMOS transistors have opposite gate voltages. That is, NMOS transistors require a positive voltage at the gate to induce the active state (and thus a positive threshold voltage), while PMOS transistors require a negative voltage at the gate to induce the active state (and thus a negative threshold voltage). *See, e.g.,* Weste, Ex.1341, 74, 293-296, 302.

99. Threshold voltage has three main components: flatband voltage (VFB), voltage drop across the gate oxide (V_o), and semiconductor potential at the semiconductor surface during strong inversion ($\psi_s(\text{inv})$). Sze-2002, Ex.1223, 175, 178, 194. For a given semiconductor and dielectric material, substrate doping, oxide thickness t_{ox} , and the metal work function Φ_m can be used to predictably tune a transistor’s threshold voltage. Houssa, Ex.1213, 535, 537. When the substrate doping and gate oxide thickness are carefully engineered to control channel mobility and the

gate capacitance, respectively, the gate electrode work function can be altered to optimize or fine-tune the threshold voltage further.

100. Consumer devices often have multiple transistors on the same chip, including transistors of the same conductivity types but with different threshold voltages, to cope with various demands on standby power and operation speed. For example, a device may include transistors for low operating power (LOP), transistors for low stand-by power (LSTP), and/or transistors for high performance (HP). ITRS-PIDS, Ex.1216, 5. HP transistors have the highest operating speed, the shortest gate length, the thinnest gate oxide, and the lowest threshold voltage among the three. ITRS-PIDS, Ex.1216, 11, 17, 21. LSTP transistors are designed for low performance and low leakage current and therefore have thicker gate oxides and higher threshold voltage, while LOP transistors are between the HP and LSTP devices in terms of performance, leakage current, and threshold voltage. *Id.*

101. As recognized by the prior art, instead of making different chips for different purposes, HP, LOP, and LSTP transistors can be formed on a single chip by varying the manufacturing process parameters. Because “[a]n increasing number of mixed-signal and system-on-a-chip applications require dual on-chip power-supply-voltages[,]” different transistors of the same type (*e.g.*, PMOS or NMOS) are needed for different power-supply-voltages. Wolf-4, Ex.1334, 121. For example, “[t]he higher-voltage may be used for the analog and input/output (I/O) circuitry, and the

lower-voltage for the core-digital-logic devices.” *Id.* And because analog and I/O regions must handle higher operating voltages, “the analog and I/O devices require thicker gate oxides than the core logic devices.” *Id.* As such, forming different transistors with different gate oxide thickness can be used where needed, for instance where both higher-voltage and lower-voltage transistors are desired on the same chip.

102. The prior art teaches different processes to vary oxide thickness across different transistors on the same chip. *See, e.g.,* Karve, Ex.1226, 3:45-4:36 (describing formation of nMOS with thicker gate oxide than core nMOS), Figs. 5-6, 8; Luo, Ex.1227, 5:61-7:58 (describing formation of nMOS-DGO and nMOS core devices). As explained by one textbook, one process is to include two oxidation steps “with a masked etch-step in between to remove the first oxide from regions intended to have thinner oxide.” Wolf-4, Ex.1334, 121. Yet another process uses nitrogen implants to impede oxide growth in certain areas, which occurs because “the rate of thermal-oxidation on silicon is reduced by nitrogen implants.” *Id.* “Hence, nitrogen implantation into the silicon substrate prior to the oxidation process can be used to facilitate the implementation of such “dual-gate-oxide” ICs.” *Id.*

VI. THE '686 PATENT

103. The '686 patent issued on June 12, 2012, from U.S. Patent Application No. 12/629,508, filed on December 2, 2009 as a continuation of PCT/JP2009/000574,

filed on February 13, 2009. Ex.1001, cover. The '686 patent claims priority to Japan Patent Application No. 2008-064435, filed on March 13, 2008. *Id.*

A. Claims

104. The '686 patent has 35 claims, including four independent claims numbered 1, 11, 19, and 25, and dependent claims numbered 2-10, 12-18, 20-24, and 26-35. Ex.1001, 29:60-34:41. Claims 25-28, 31, and 35 are the Challenged Claims with claims 26-28, 31, and 35 depending from claim 25.

105. The Challenged Claims are reproduced below:

25. [Preamble]: A semiconductor device comprising:

25[a]: a first MIS transistor; and

25[b]: a second MIS transistor, wherein:

25[c]: the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate;

25[d]: [the first MIS transistor includes: ...] a first gate electrode including a second metal film formed on the first gate insulating film;

25[e]: [the first MIS transistor includes: ...] first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and

25[f]: [the first MIS transistor includes: ...] a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions

located in the first active region laterally outside the first sidewall spacers,

25[g]: the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate;

25[h]: [the second MIS transistor includes: ...] a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;

25[i]: [the second MIS transistor includes: ...] second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative; and

25[j]: [the second MIS transistor includes: ...] the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers; and

25[k]: the first and second metal films are made of different metal materials,

25[l]: the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes, and

25[m]: the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region.

Ex.1001, 33:8-34:2.

26. The semiconductor device of claim 25, wherein the first metal film has a thickness smaller than that of the second metal film.

Ex.1001, 34:3-5.

27. The semiconductor device of claim 25, wherein the first and second metal films have different work functions.

Ex.1001, 34:6-8.

28. The semiconductor device of claim 25, wherein the silicon nitride film has a thickness smaller than that of the first gate electrode.

Ex.1001, 34:9-11.

31. The semiconductor device of claim 25, wherein the first and second gate insulating films are made of the same insulating material.

Ex.1001, 34:18-20.

35.: The semiconductor device of claim 25, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.

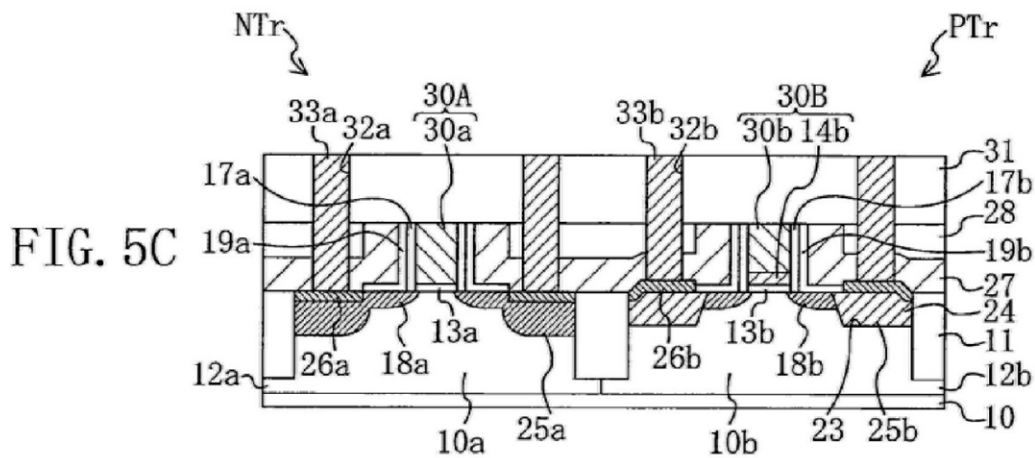
Ex.1001, 38-41.

B. Summary of the Specification

106. The '686 patent describes "a semiconductor device including n- and p-type MIS transistors having gate electrodes made of different metal materials."

Ex.1001, 5:39-45. FIG. 5C below illustrates one embodiment in which the semiconductor device includes an nMIS transistor (NTr) and a pMIS transistor (PTr).

Id., 16:55-60. The nMIS transistor includes a gate insulating film (13a) and a first gate electrode (30A) that includes a metal film (30a) formed on the gate insulating film. *Id.*, 16:16-22. The pMIS transistor includes a gate insulating film (13b) and a second gate electrode (30B) that includes a metal film (14b) and a conductive film (30b). *Id.*, 16:16-22. Insulative sidewall spacers (17a/19a, 17b/19b) line the outer surfaces of each gate electrode. *Id.*, 12:50-63. As illustrated in FIG. 5C below, sidewalls 19a/19b have an L-shaped cross-section, and an insulating film (27) and inter-layer insulating film (28) fill the space between the gates. *Id.*, 14:51-15:5, FIG. 4A.



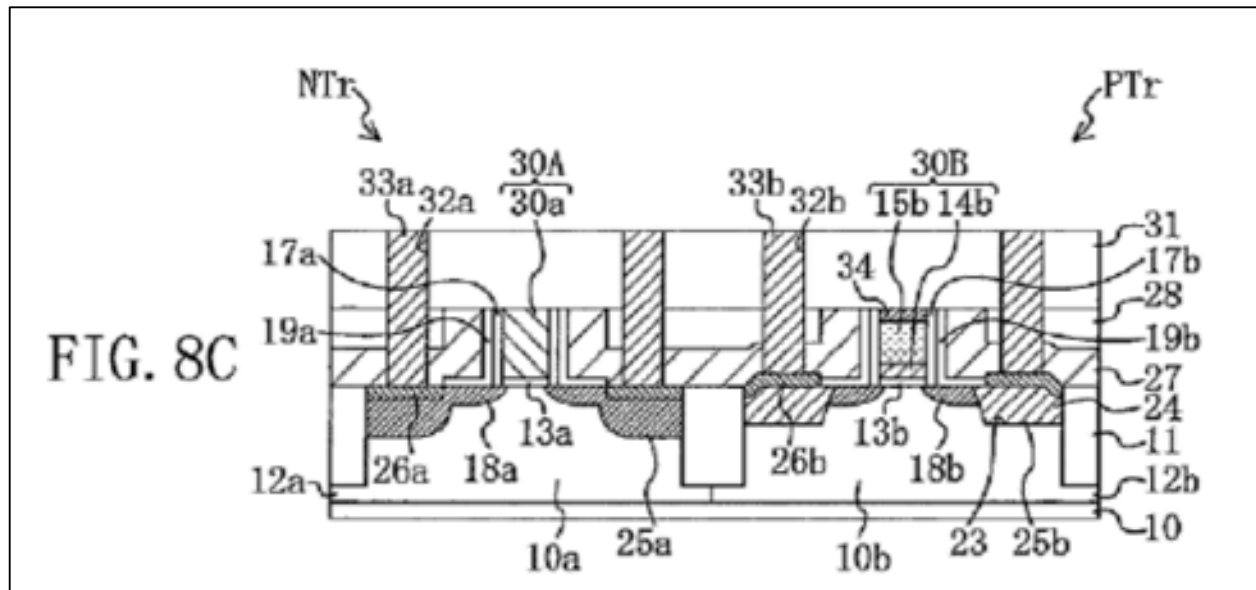
'686 Patent's FIG. 5C

NTr:	<u>nMIS transistor</u>	PTr:	<u>pMIS transistor</u>
13a:	gate insulating film	13b:	gate insulating film
30A:	first gate electrode	30B:	second gate electrode
30a:	metal film	14b:	metal film
		30b:	conductive film
17a:	insulative sidewall spacer	17b:	insulative sidewall spacer
19a:	insulative sidewall spacer	19b:	insulative sidewall spacer
<u>nMIS & pMIS Transistors</u>			
27:	insulating film	28:	inter-layer insulating film

107. The gate insulating films (13a/13b) may be formed of the same or of different materials. In some embodiments, the gate insulating films (13a/13b) are a high-k metal oxide having a relative dielectric constant k of 10 or more such as “hafnium-based oxides such as hafnium oxide (HfO_2), hafnium silicate (HfSiO), and

hafnium silicon oxynitride (HfSiON) and the like.” Ex.1001, 29:16-24; *see also id.*, 11:31-37. As shown above in FIG. 5C, the insulating film (27), made of silicon nitride, for example, does not lie on any upper surface of the gate electrodes, because the wafer has been planarized. *Id.*, 6:42-45, 14:65-15:30.

108. In some embodiments, including as illustrated in FIG. 5C above, the conductive film (30b) in the pMIS gate electrode (30B) may be a metal film formed of the same material as the metal film (30a) in the nMIS gate electrode (30A) because they are formed by patterning the same layer. Ex.1001, 15:64-16:22, FIGS. 5A-C. In other embodiments, such as illustrated in FIG. 8C below, the conductive film (15b) in the pMIS gate electrode (30B) is silicon. *Id.*, 21:61-67, FIGS. 7A-8C. In the embodiment shown in FIG. 8C, a metal silicide film (34) is formed on the silicon film (15b). *Id.*, 22:33-41, FIG. 8C.



Ex.1001, FIG. 8C

109. Additionally, the '686 patent describes causing stress in the first and second active regions (10a/10b). Ex.1001, 28:63-29:15. In the second active region (10b), for example, a silicon mixed crystal layer (24) (e.g., SiGe) may be formed in the trenches (23) to cause compressive stress in the gate length direction of the channel region. *Id.*, 13:60-65, 19:54-61, 23:28-33. In the first active region (10a), the insulating film (27) causes tensile stress in the gate length direction of the channel region. *Id.*, 28:16-43.

C. Summary of the Prosecution History

110. During prosecution of the application that led to the '686 patent, the Examiner rejected original claims 1-14 for various reasons, including rejection of claims 1-4 and 7 based on Aoyama's first embodiment described with reference to Figures 1-2N).¹ Ex.1002, 201-06. In response, the Applicant amended claim 1 to recite that "the source/drain regions include a silicon mixed crystal layer which is formed in trenches provided in the second active region, and causes first stress in a gate length direction of a channel region in the second active region." *Id.*, 213. According to the Applicant, this feature distinguished Aoyama from claim 1. *Id.*, 227. The Applicant also added new claims 21-50. *Id.*, 218-26.

¹ The Examiner never cited or relied on Aoyama's third embodiment that is relied on in the Petition and is disclosed in FIGS. 5-6Q. See Section X.A below.

111. In a second rejection, the Examiner cited different art—the Hou reference—to reject most of the new and amended claims. Ex.1002, 236. In response, the Applicant amended several independent claims, including claim 1, to further recite that “the insulating film has a thickness smaller than that of the first gate electrode.” *Id.*, 246.

112. In a third rejection, the Examiner cited the Hou reference in combination with a secondary reference, to reject pending claims 31-33 and 38. Ex.1002, 268. In response, the Applicant amended several of the claims considerably, including by reciting additional spacers and specific material requirements for various features. *Id.*, 274-75.

113. In a fourth rejection, the Examiner cited several informalities but otherwise indicated that the claims would be allowed if the Applicant resolved those issues. Ex.1002, 294-95. The Applicant complied (*id.*, 310), and the claims were allowed (*id.*, 319). After Applicant corrected another informality in the claims, the '686 patent issued. *Id.*, 329, 354.

VII. LEVEL OF ORDINARY SKILL IN THE ART

114. I understand that there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including the educational level of active workers in the field at the time of the alleged invention, the sophistication of the

technology, the type of problems encountered in the art, and the prior art solutions to those problems.

115. In determining the characteristics of a hypothetical person of ordinary skill in the art of the '686 patent at the time of the alleged invention, I considered several things, including the type of problems encountered in this field, and the rapidity with which innovations were made. I also considered the sophistication of the technology involved, and the educational background and experience of those actively working in the field, and the level of education that would be necessary to understand the '686 patent. Finally, I placed myself back in the relevant periods of time and considered the state of the art and the level of skill of the engineers working in this field in those times.

116. It is my opinion that a POSITA at the time of the '686 patent would have had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or a related field, and three years of work experience in semiconductor design and manufacturing, including with respect to planar transistors, or equivalent work experience. Additional graduate education might compensate for a deficiency in experience, and vice-versa.

117. I also note that my opinions provided in this Declaration would not change in view of any minor modifications to this level of skill.

VIII. CLAIM CONSTRUCTION

118. It is my opinion that for purposes of this proceeding, the claim terms need not be construed to resolve the prior art issues presented in this Petition.

119. Nothing in this section should be construed as expressing any opinion as to whether the claims constitute patentable subject matter under 35 U.S.C. § 101, or whether they satisfy the definiteness, enablement, best mode, or written description requirements under 35 U.S.C. § 112.

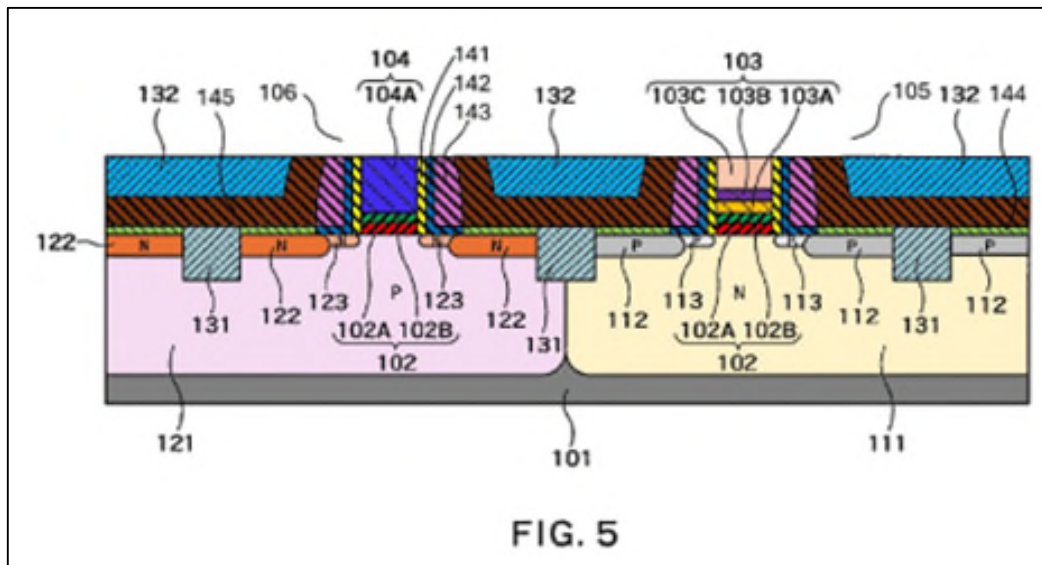
IX. OVERVIEW OF THE PRIOR ART

A. Aoyama (Ex.1005)

120. In my opinion, Aoyama is analogous art to the '686 patent because it is in the same field of endeavor as the '686 patent (i.e., semiconductor devices and methods for fabricating the same, including MISFETs). *See e.g.*, Ex.1001, 1:14-20; Ex.1005, ¶¶2-3. In my opinion, Aoyama is also analogous art to the '686 patent because a POSITA would have found it reasonably pertinent to at least one problem the '686 patent addresses, such as fabricating semiconductor devices with high-k/metal-gate structures. *See* Ex.1001, 1:14-50, 11:31-37; Ex.1005, ¶¶2-3.

121. Aoyama describes three embodiments, each of which uses a replacement metal gate (“RMG”) approach to form the gate electrodes. My Declaration focuses on Aoyama’s third embodiment, as illustrated below in FIG. 5 and disclosed in ¶¶97-121 and FIGS. 5-6Q, which was not cited or relied on by the

Examiner during prosecution of the application that led to the '686 patent. Aoyama's FIG. 5 (annotated below) illustrates Aoyama's NMOS on the left side in NMOSFET (i.e., nFET) region 106 and Aoyama's PMOS on the right side in PMOSFET (i.e., pFET) region 105. Ex.1005, Aoyama, ¶¶97-121, FIGS. 5-6Q.



Ex.1005, FIG. 5 (annotated)

122. Both NMOS and PMOS devices include an interfacial silicon oxide dielectric layer 102A, a high-k gate dielectric layer 102B, and gate sidewall spacers 141, 142, and 143. Ex.1005, ¶¶98, 111. But the NMOS and PMOS gate structures differ above the high-k gate dielectric. More specifically, the PMOS gate electrode 103 includes a first conductive layer 103A (e.g., W), a second conductive layer 103B (e.g., TiN), and a semiconductor layer (silicide layer) 103C (e.g., polysilicon capped with NiSi). *Id.*, ¶¶ 107, 114, 121. The NMOS gate electrode 104, however, includes only a third conductive layer 104A (e.g., TaCN). *Id.*, ¶118. The spaces between

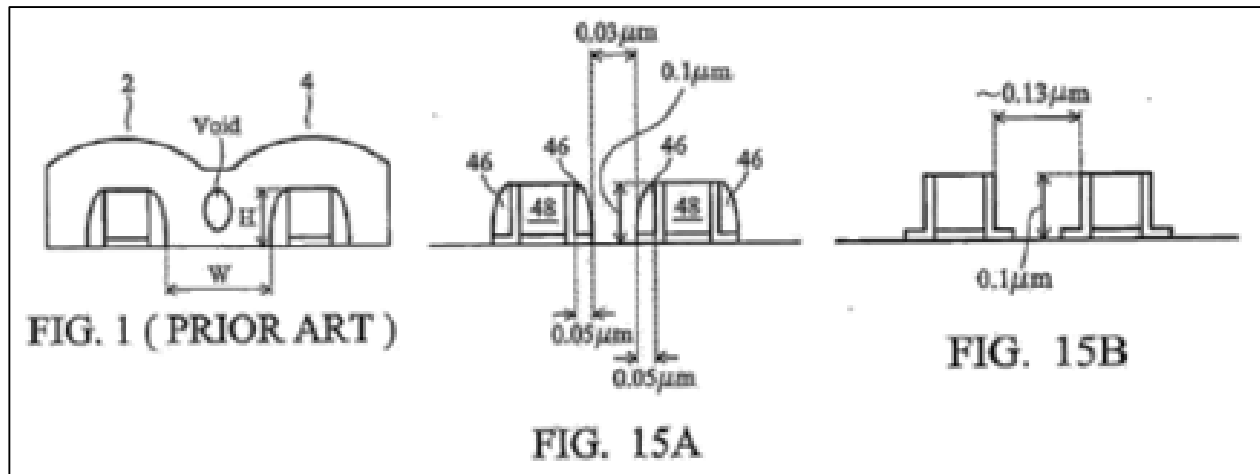
Aoyama's NMOS and PMOS gate structures are filled with a silicon nitride etch stopper 145 and a silicon oxide interlayer dielectric 132. *Id.*, ¶113.

B. Hsu823 (Ex.1006)

123. In my opinion, Hsu823 is analogous art to the '686 patent because Hsu823 is in the same field of endeavor as the '686 patent (i.e., semiconductor devices and methods for fabricating the same, including MISFETs). *See* Ex.1001, 1:14-20; Ex.1006, ¶1. In my opinion, Hsu823 is also analogous art to the '686 patent because a POSITA would have found it reasonably pertinent to at least one problem the '686 patent addresses, such as fabricating strain-engineered semiconductor devices with SiGe source/drain regions and strain-inducing CESL. *See* Ex.1001, 1:14-50, 13:33-50, 28:10-56; Ex.1006, ¶¶ 33, 36.

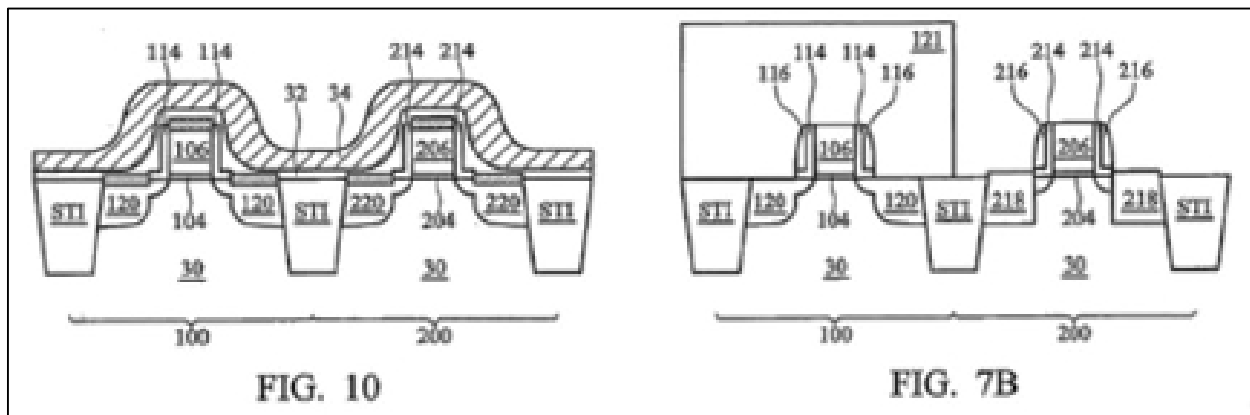
124. Hsu823 explains that “[w]hen devices become smaller, the distance between devices decreases,” and this leads to a “gap-filling problem” (also known as voiding), as FIG. 1 below illustrates. Ex.1006, ¶4. To address this problem, as FIG. 15A below shows, Hsu823 teaches to use an L-shaped spacer liner made of silicon oxide and a spacer made of silicon nitride. *Id.*, ¶¶31, 35, FIGS. 6, 15A. After using the silicon nitride spacer to define source/drain regions, Hsu823 teaches that the outer spacer may be removed, leaving only the L-shaped spacer liner as in FIG. 15B (below, right). *Id.*, ¶35, FIGS. 9, 15B. By adopting this technique, Hsu823 explains that “gap-

filling is improved and the contact etching process can be better controlled.” *Id.*, ¶¶42-43.



Ex.1006, FIGS. 1, 15A, and 15B

125. Using this technique, Hsu823 discloses MISFETs like the exemplary one illustrated in FIG. 10 (below, left). According to Hsu823, a “dielectric layer 32 is optionally formed, ”meaning it may be omitted.” See Ex.1006, ¶36. In such an embodiment, a contact etch stop layer (CESL) 34 directly contacts L-shaped spacer liners 114/214 and boosts channel stress. See *id.*, ¶¶15, 36, FIGS. 9, 14. For example, Hsu823 teaches a CESL 34 that exerts tensile stress on both NMOS and PMOS devices. *Id.*, ¶¶36-37.



Ex.1006, FIGS. 10 and 7B

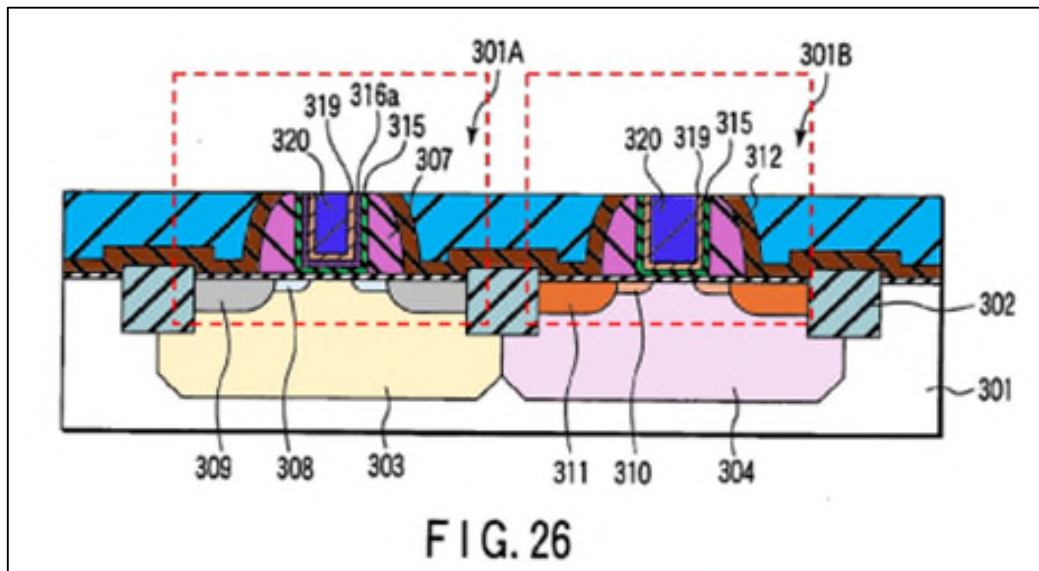
126. Additionally, Hsu823 teaches that the PMOS source/drain regions (*see* FIG. 10 (above, left) (element 220)) may be formed using epitaxial SiGe (*see* FIG. 7B (above, right) (element 218)). Ex.1006, ¶¶32-33, FIGS. 7A-B, 10. In this technique, which was well-known by 2008, a recess etch is performed to open cavities in the source/drain regions of the substrate, and those cavities are filled by growing epitaxial SiGe. *Id.*, ¶33, FIG. 7B. “This introduces compressive stresses in the respective channel regions of the resulting PMOS devices, and the device drive currents of the respective PMOS devices are increased.” *Id.*, ¶33.

C. Akasaka (Ex.1008)

127. In my opinion, Akasaka is analogous art to the '686 patent because Akasaka is in the same field of endeavor as the '686 patent (i.e., semiconductor devices and methods for fabricating the same, including MISFETs). *See* Ex.1001, 1:14-20; Ex.1008, ¶¶2-3.

128. In my opinion, Akasaka is also analogous art to the '686 patent because a POSITA would have found it reasonably pertinent to at least one problem the '686 patent addresses, such as fabricating semiconductor devices with high-k/metal-gate structures. See Ex.1001, 1:14-50, 11:31-37; Ex.1008, ¶¶2-7.

129. As illustrated below, Akasaka describes p-type MISFET and n-type MISFET devices formed using an RMG approach with respect to the gate electrodes. Ex.1008, FIG. 26 (annotated below). The left side of FIG. 26 illustrates Akasaka's pFET 301A, and the right side of FIG. 26 illustrates Akasaka's nFET 301B. *Id.*, ¶72, FIG. 26.



Ex.1008, Akasaka, FIG. 26 (annotated)

130. The pFET and nFET each use a gate dielectric 315 (e.g., hafnium silicon oxide). Ex.1008, ¶75. Above the gate dielectric, the nFET gate electrode includes conductive films 319 and 320. *Id.*, ¶¶84-86. Conductive film 319 “has a metallic band

structure with a work function close to that of *n*⁺-poly-crystalline silicon,” and conductive film 320 may be tungsten. *Id.*, ¶¶85-86 (emphasis added). The pFET gate electrode additionally includes conductive film 316, which “has a metallic band structure with a work function close to that of *p*⁺-poly-crystalline silicon”(e.g., TiN). *Id.*, ¶¶76-77 (emphasis added). The spaces between the nFET and pFET gate structures are filled with a silicon nitride film 312 and an inter-level insulating film 313. *Id.*, ¶73.

X. SPECIFIC GROUNDS FOR PETITION

131. By March 13, 2008, structures like the ones described in the '686 patent were already known and used extensively throughout the semiconductor industry. *See, e.g., generally* Ex.1516; Ex.1517. Because the relevant principles and structures were already thoroughly established and widely known, it is my opinion that a POSITA would have found the claimed structures in the '686 patent obvious, as I explain in detail below.

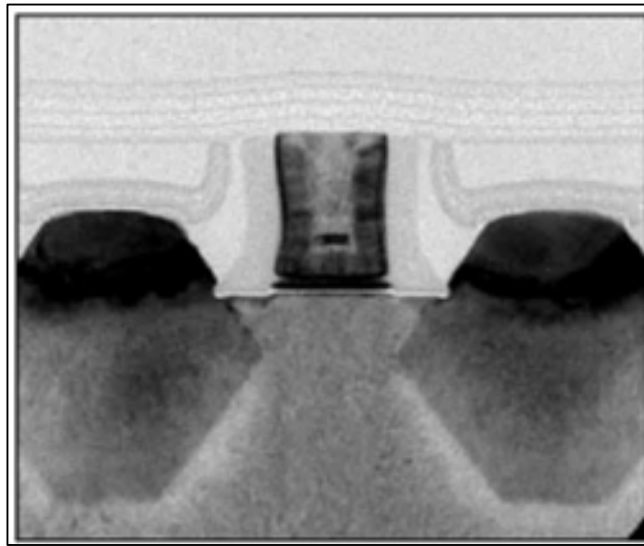
A. Ground I (Aoyama (Ex.1005), Hsu823 (Ex.1006))

132. In my opinion, Aoyama in combination with Hsu823 renders obvious the Challenged Claims of the '686 patent (Ground I).

1. A POSITA would have found it obvious to implement SiGe stressors in the source/drain regions of Aoyama's pFET

133. In my opinion, a POSITA would have been motivated to combine Aoyama and Hsu823, thereby rendering claim 25 obvious. By the time the application for the '686 patent was filed, SiGe stressors had already been known and used in three generations of high-volume commercial transistors. *See* Ex.1523, 1790-91 (describing Intel's 90nm devices); Ex.1532, 657-58 (describing Intel's 65nm devices); Ex.1516, 247-48 (describing Intel's 45nm devices); Ex.1517 (same).

134. The most recent generation prior to the filing date of the '686 patent, shown publicly in images like the one below before the application for the '686 patent, not only used SiGe stressors but also high-k gate dielectrics and metal gates in an RMG process. *See generally* Ex.1516; Ex.1517, 14-19. By the time the application for the '686 patent was filed, such SiGe stressors were standard industry practice. *See* Section V.F above.



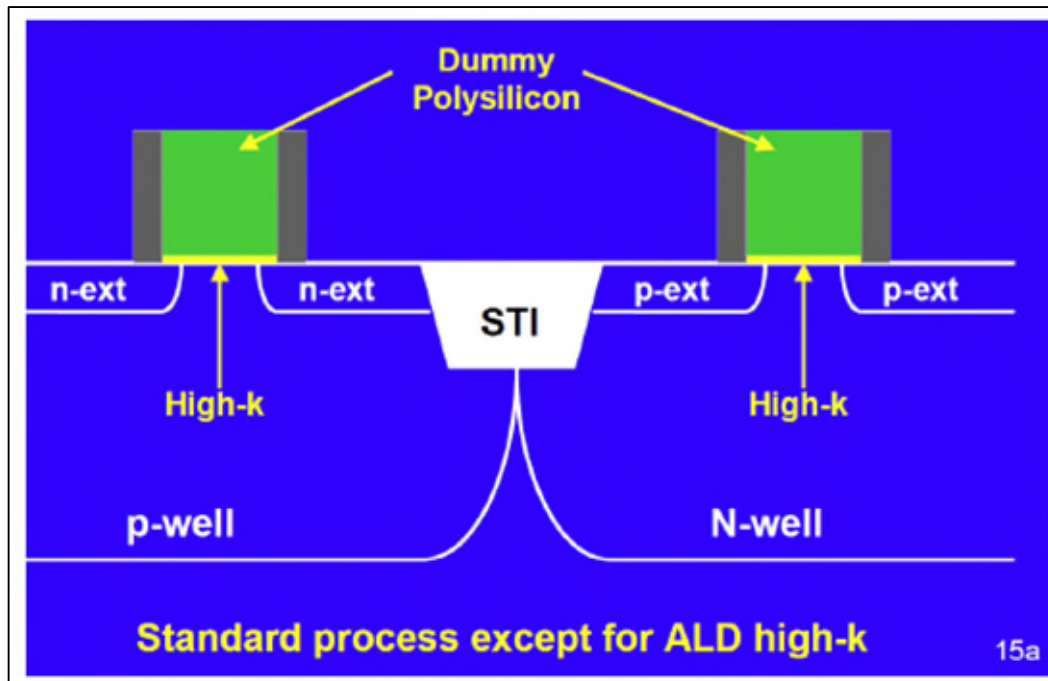
Ex.1516, Fig. 6

135. Although Aoyama may not expressly describe using SiGe stressors, it would have been obvious to use SiGe stressors in Aoyama’s FIG. 5, third embodiment transistor design, as the micrograph above—showing Intel’s high-volume 45nm generation of devices that had been in production since 2007—make clear. Ex.1516, Fig. 6; *see also* Ex.1517, 16.

136. At the December 2007 International Electron Devices Meeting (“IEDM”)² in Washington, D.C., Kaizad Mistry of Intel described Intel’s 45 nm process flow, which was a high-k/RMG process. *See generally* Ex.1517, 14-19 (in-person IEDM presentation); Ex.1516 (publication of related IEDM paper). To begin, nFET and pFET dummy gate structures are formed. The dummy gates comprise high-

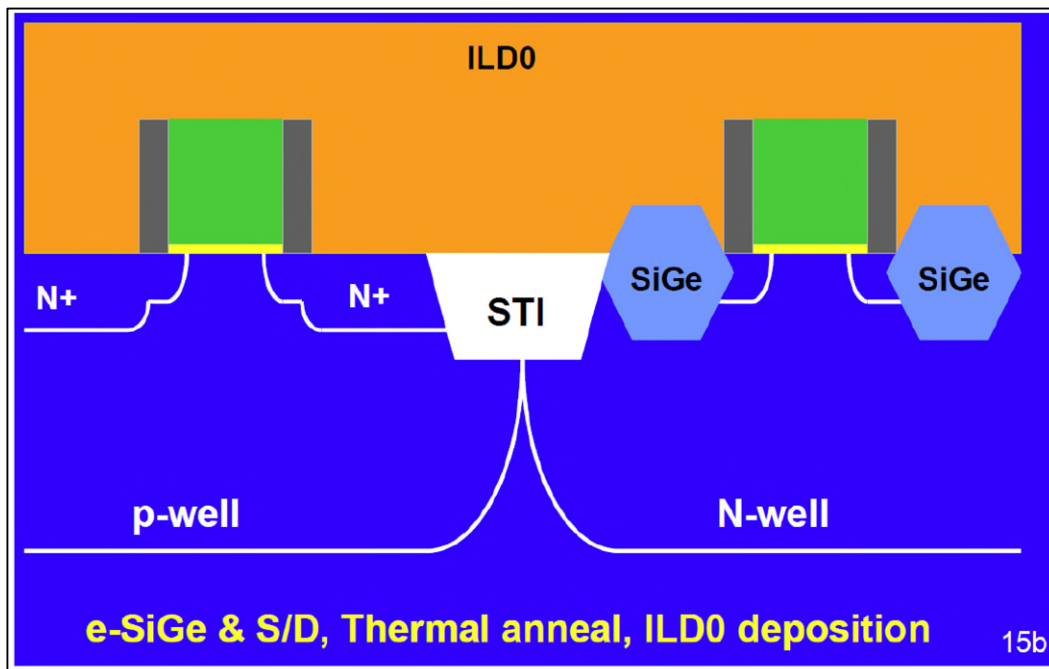
² IEDM is a very prominent and well-attended conference in the field.

k dielectrics (yellow) and dummy polysilicon gate electrodes (green). Ex.1517, 15a (below).



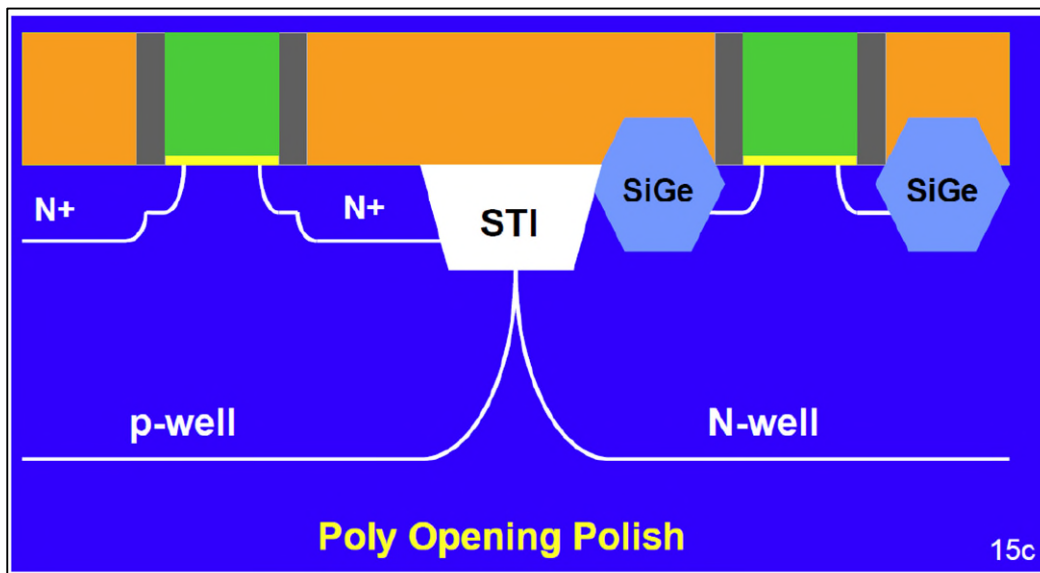
Ex.1517, 15a

137. Next, the source/drain regions are formed, including the formation of embedded epitaxial SiGe source/drain regions for the pFET (light blue hexagons). See Section V.F above. This is followed by thermal annealing to activate implanted dopants and then by a blanket deposition of interlayer dielectric ILD0 (orange), as shown below. Ex.1517, 15b (below).



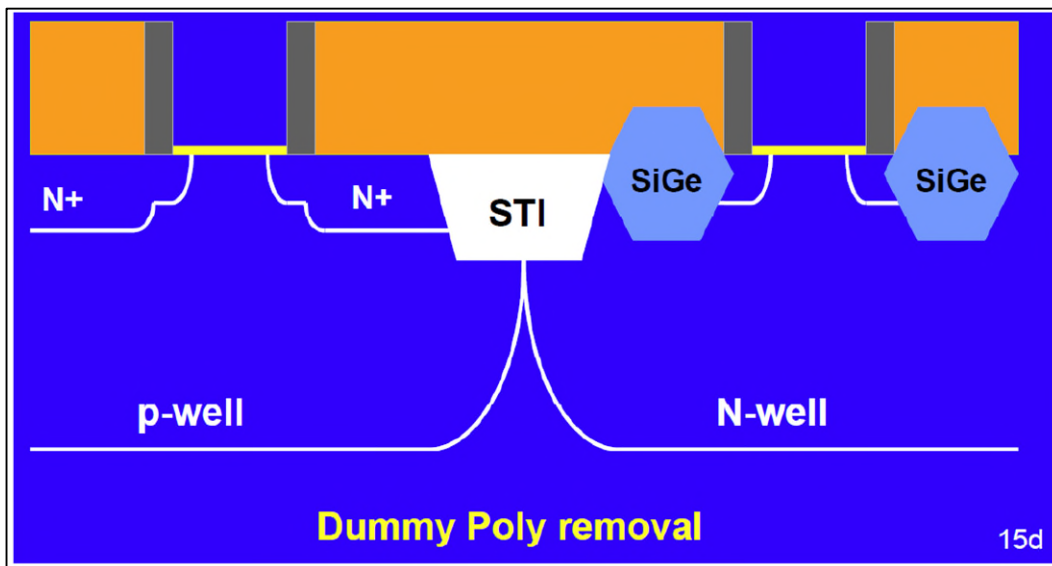
Ex.1517, 15b

138. Following this, a polishing step is performed to planarize interlayer dielectric ILD0 (orange) such that its top surface aligns with the top surfaces of the dummy polysilicon gate electrodes (green). Ex.1517, 15c (below).



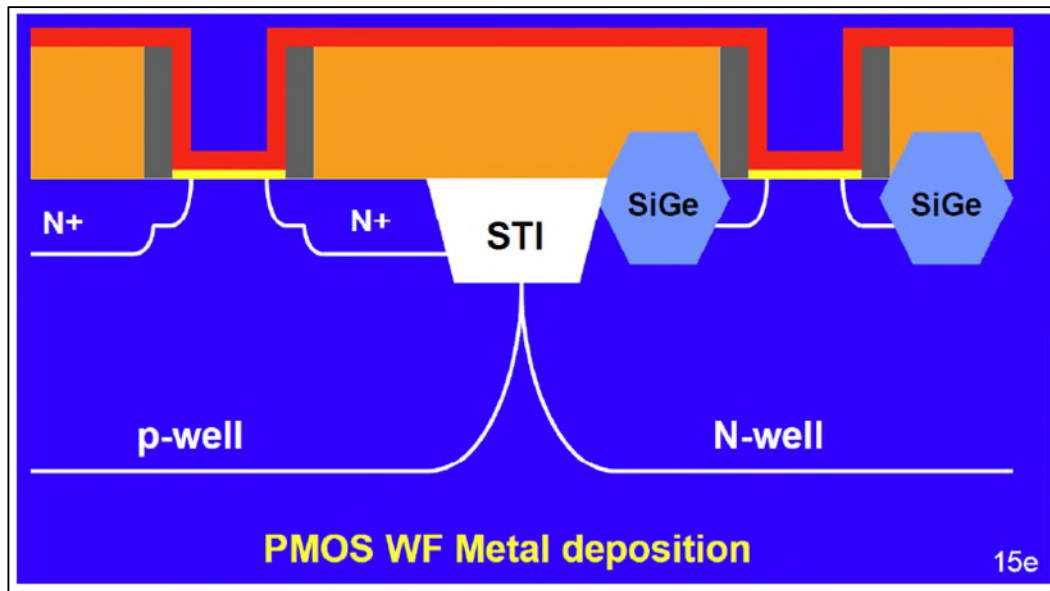
Ex.1517, 15c

139. Next, the dummy polysilicon gate electrodes (green) are removed by etching. Ex.1517, 15d (below).



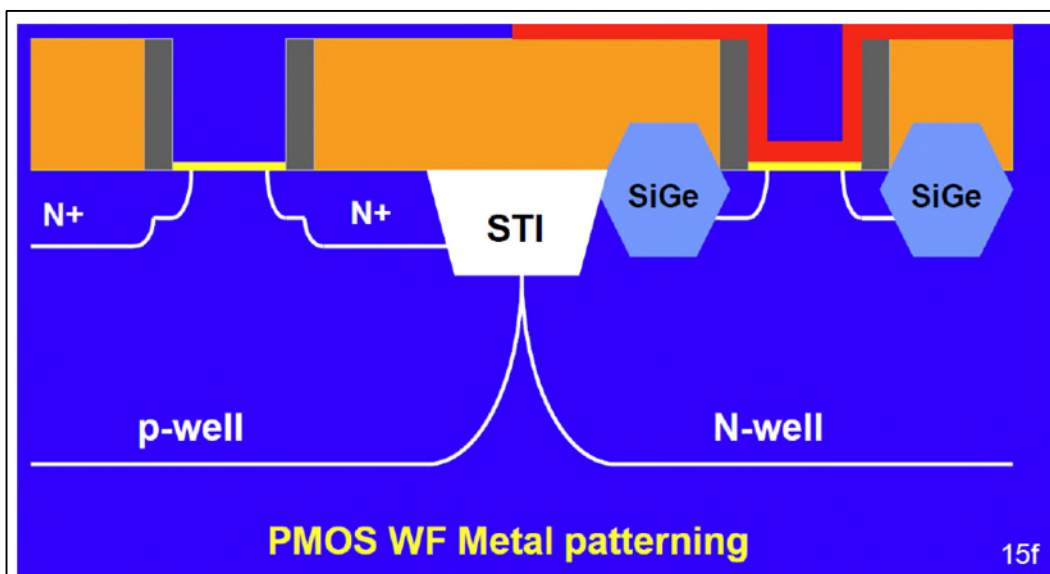
Ex.1517, 15d

140. The pFET work-function metal (red) is then deposited over the wafer, including in the void left by removing the dummy polysilicon gate electrodes. Ex.1517, 15e (below).



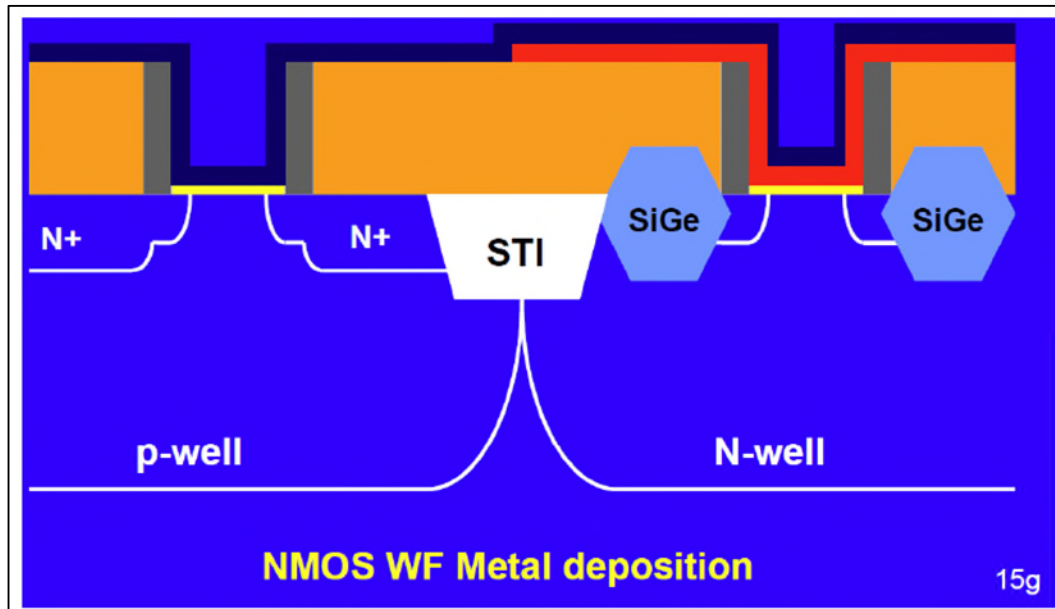
Ex.1517, 15e

141. Because this is the pFET work-function metal, it is removed from the wafer by etching everywhere except in the pFET regions. Ex.1517, 15f (below).



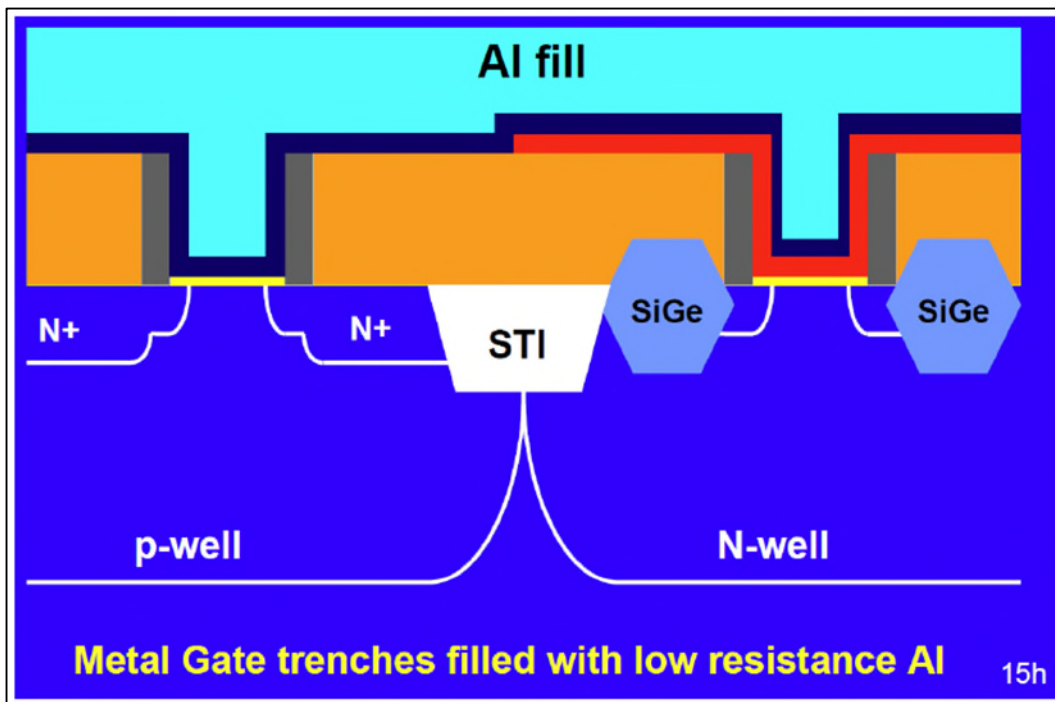
Ex.1517, 15f

142. Next, the nFET work-function metal (dark blue) is deposited over the wafer, including in the voids left by removing the dummy polysilicon gate electrodes. Ex.1517, 15g (below).



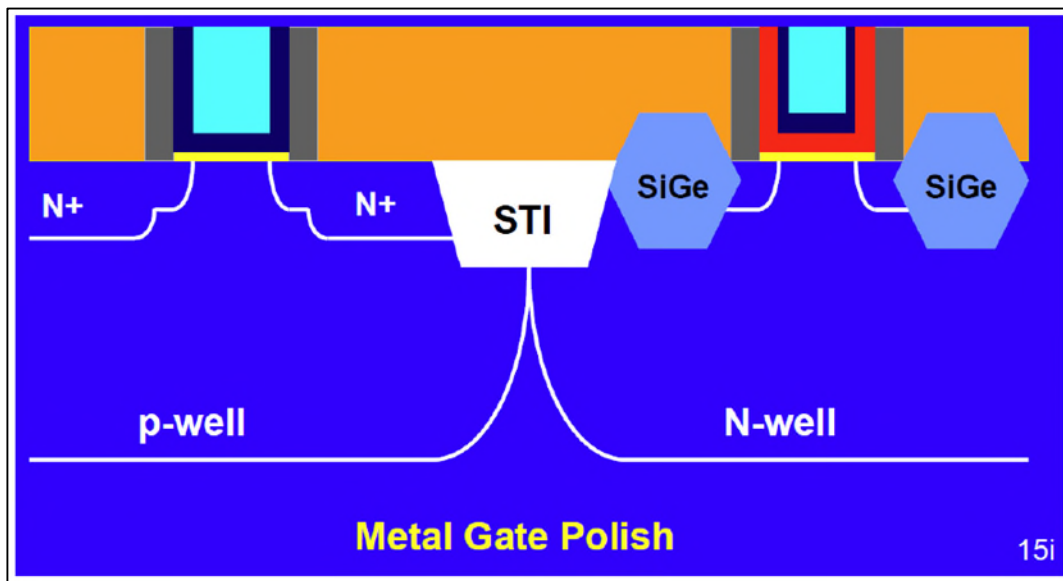
Ex.1517, 15g

143. Then, an aluminum filler (turquoise) is deposited over the entire wafer to fill the remaining voids left in the nFET and pFET gate electrode regions. Ex.1517, 15h (below).

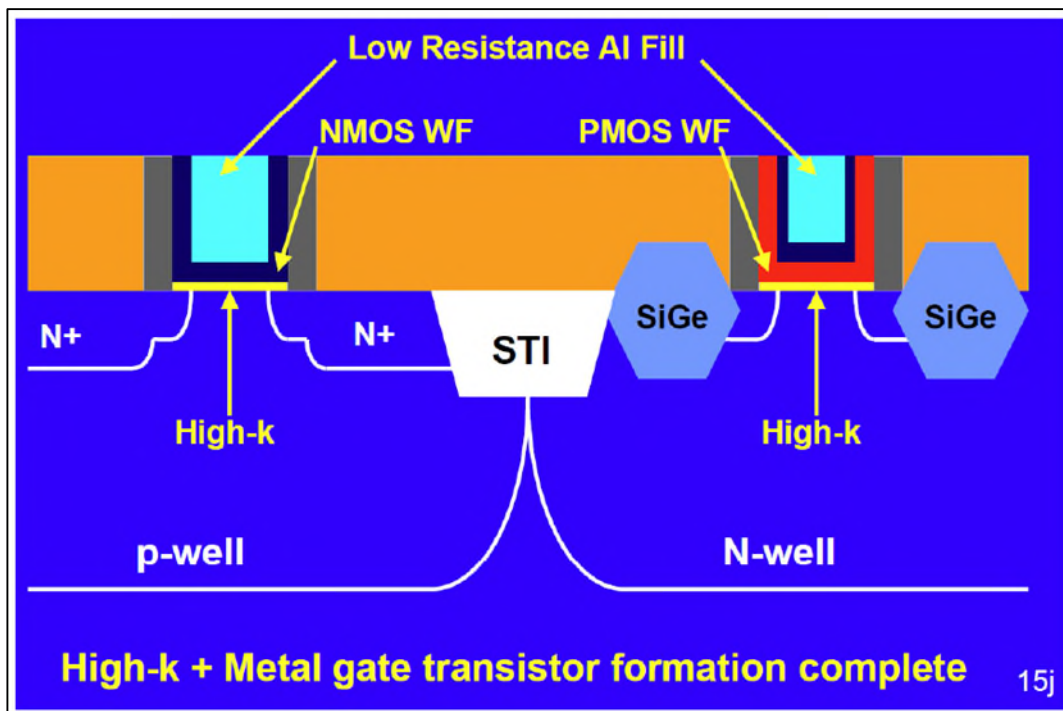


Ex.1517, 15h

144. A second polishing step is done to planarize the metal films such that the top surfaces of the replacement metal gate electrodes are aligned with the top surface of interlayer dielectric film ILD0 (orange). Ex.1517, 15i (below, top), 15j (below, bottom).



Ex.1517, 15i

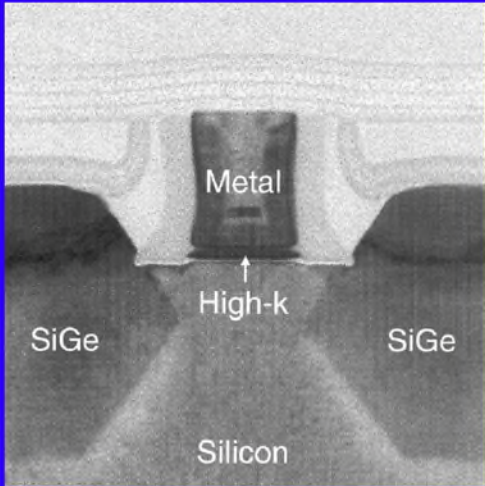


Ex.1517, 15j (same as 15i but with additional labels)

145. The final structure made using Intel's 45 nm high- κ /RMG process appears below. Ex.1517, 16, 19.

Transistor Features

- 35 nm min. gate length
- 160 nm contacted gate pitch
- 1.0 nm EOT Hi-K
- Dual workfunction metal gate electrodes
- 3RD generation of strained silicon

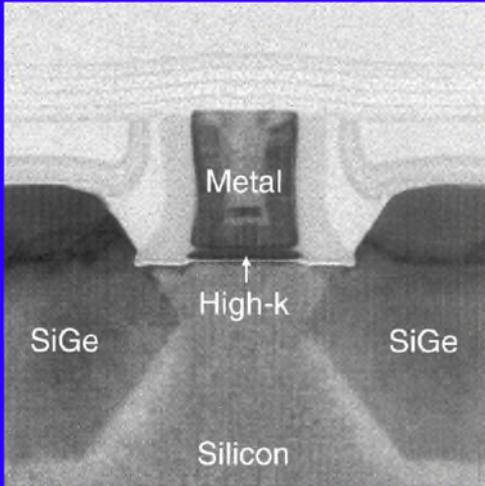


Micrograph showing a pFET transistor structure. The central gate stack is labeled "Metal" and "High-k". The gate electrodes on either side are labeled "SiGe". The substrate is labeled "Silicon".

16

Ex.1517, 16 (micrograph showing a pFET)

3RD Generation Strained Silicon



Micrograph showing a pFET transistor structure. The central gate stack is labeled "Metal" and "High-k". The gate electrodes on either side are labeled "SiGe". The substrate is labeled "Silicon".

- Increased Ge fraction
 - 90 nm: 17% Ge
 - 65 nm: 23% Ge
 - 45 nm: 30% Ge
- SiGe closer to channel

Ex.1517, 19 (micrograph showing a pFET)

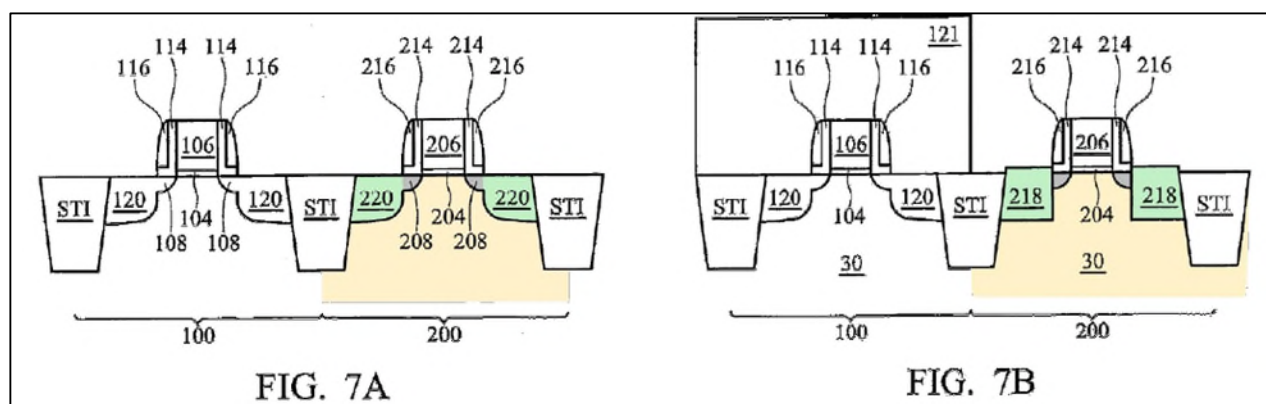
146. As the above presentation demonstrates, epitaxial SiGe had been fully integrated with high-k/RMG technology in Intel's high-volume commercial 45nm products, which was therefore common knowledge in the industry well before the application for the '686 patent was filed. *See generally* Ex.1516; Ex.1517. Given the similarity between Intel's 45 nm process above and the process used to make Aoyama's third embodiment semiconductor device (*see* Ex.1005, ¶¶97-121, FIGS. 5-6Q), a POSITA would have found it obvious to integrate epitaxial SiGe into Aoyama's third embodiment in my opinion.

147. Although the commercial adoption of SiGe stressors by Intel demonstrates both motivation to use such technology and a reasonable expectation of success for a POSITA, other literature confirms such motivation and expectation. For example, as an alternative to forming pFET source/drain regions solely by ion implantation, Hsu823 teaches forming SiGe stressors 218 in trenches of pFET active regions to induce compressive stress in the pFET channel region. Hsu823 explains that, in one embodiment, "source/drain regions 120 and 220 are formed [only] by implanting impurities into semiconductor substrate 30." Ex.1006, ¶32. As an alternative, Hsu823 teaches that SiGe stressors may be used:

In alternative embodiments, as shown in FIG. 7B, SiGe stressors 218 are formed in PMOS region 200. Preferably, a photo resist 121 is formed covering NMOS region 100.

Recesses are formed in substrate 30 along the outside edges of the spacers 216, preferably by etching. SiGe stressors 218 are then formed in the recesses. In the preferred embodiment, SiGe stressors 218 are epitaxially grown. P-type impurities such as boron are preferably doped during the epitaxial growth. The photo resist 121 is then removed. After being annealed, SiGe stressors 218 will try to restore their lattice spacing, which is greater than the lattice spacing of the substrate 30. This introduces compressive stresses in the respective channel regions of the resulting PMOS devices, and the device drive currents of the respective PMOS devices are increased.

Id., ¶33. Hsu823's FIGS. 7A (below, left) and 7B (below, right) illustrate usage of SiGe stressors.



Ex.1006, FIGS. 7A-7B (annotated)

148. In my opinion, a POSITA would have found it obvious to modify the pFET in Aoyama's FIG. 5, third embodiment semiconductor device by using epitaxial SiGe stressors, as taught by Hsu823 (and as Intel's public disclosures confirm), to form Aoyama's pFET source/drain regions 112.

149. A POSITA would have been motivated to do so in my opinion because SiGe stressors were known to increase hole mobility, thereby boosting drive current and operating speed. See Section V.F above. As Hsu823 explains, SiGe stressors "introduce[] compressive stress[] in the . . . channel region[]" such that the "device drive current[] of the . . . PMOS device[] [is] increased." Ex.1006, ¶33. Again, this was already standard industry practice when the application for the '686 patent was filed, as Hsu823 further confirms:

Among efforts made to enhance carrier mobility, forming a stressed channel region is a known practice. The performance of a MOS device can be enhanced through a stressed-surface channel. This technique allows performance to be improved at a constant gate length without adding complexity to circuit fabrication or design. Research has revealed that . . . a compressive stress parallel to the channel length direction can improve PMOS device performance.

Id., ¶¶2-3.

150. It is also my opinion that a POSITA would have reasonably expected to succeed in implementing Hsu823's SiGe stressors in Aoyama's FIG. 5, third embodiment semiconductor device because such SiGe crystal layers were known and widely used to induce compressive stress in pFETs. *See* Section V.F above. The structure in Aoyama's FIG. 6I is materially the same as the structure in Hsu823's FIG. 7A. *Compare* Ex.1005, ¶¶103-111, FIG. 6I, with Ex.1006, ¶¶28-32, FIG. 7A.

151. As I explain above, Hsu823 teaches (and the Intel disclosures confirm) that SiGe source/drain regions may be readily integrated into such a structure to boost PMOS performance. Ex.1006, ¶33; *see also* Ex.1517, 14-19. Thus, as Figure A (below, left) shows, a POSITA would have known the same process steps Hsu823 describes regarding FIG. 7B (below, right) readily integrate into Aoyama's process at FIG. 6I with the ordinary and expected result (i.e., SiGe stressors to boost pFET performance). Ex.1006, ¶33; *see also* Section V.F above.

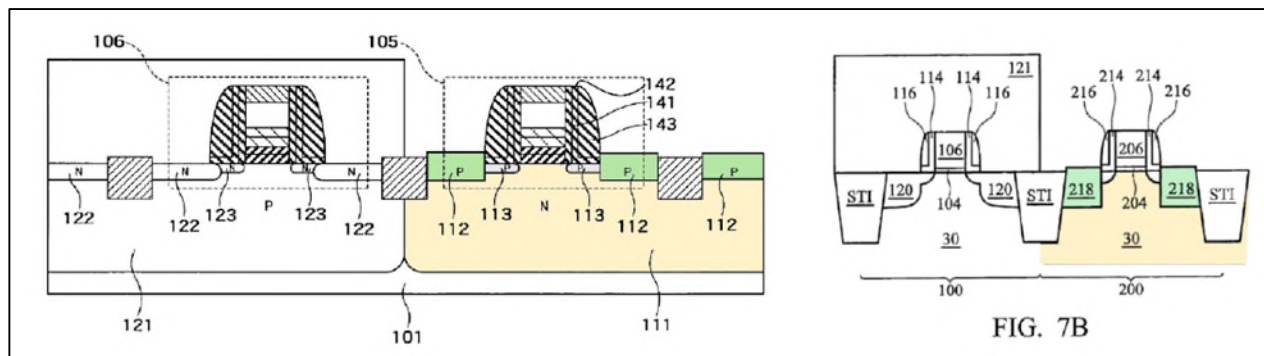
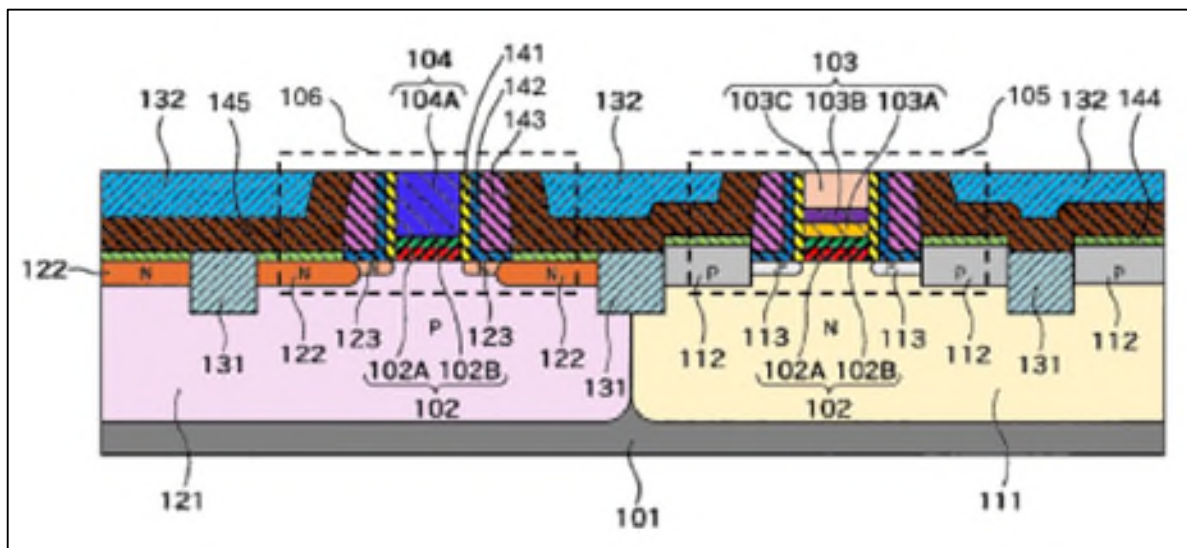


Figure A
(Ex.1005, Aoyama, FIG. 6I, modified & annotated)

Ex.1006, Hsu823, FIG. 7B
(annotated)

152. Figure B below illustrates an exemplary modification of Aoyama's semiconductor device that includes SiGe stressors like the ones Hsu823 discloses. Ex.1006, ¶33, FIG. 7B; Ex.1005, FIG. 5; Ex.1538, 6:27-31, FIGS. 3-10 (illustrating a similar implementation of SiGe stressors in an RMG device); Ex.1516, Fig. 6 (same).

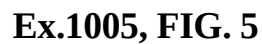


Ex.1005, Figure B (Aoyama, FIG. 5, modified and annotated)

2. Independent Claim 25

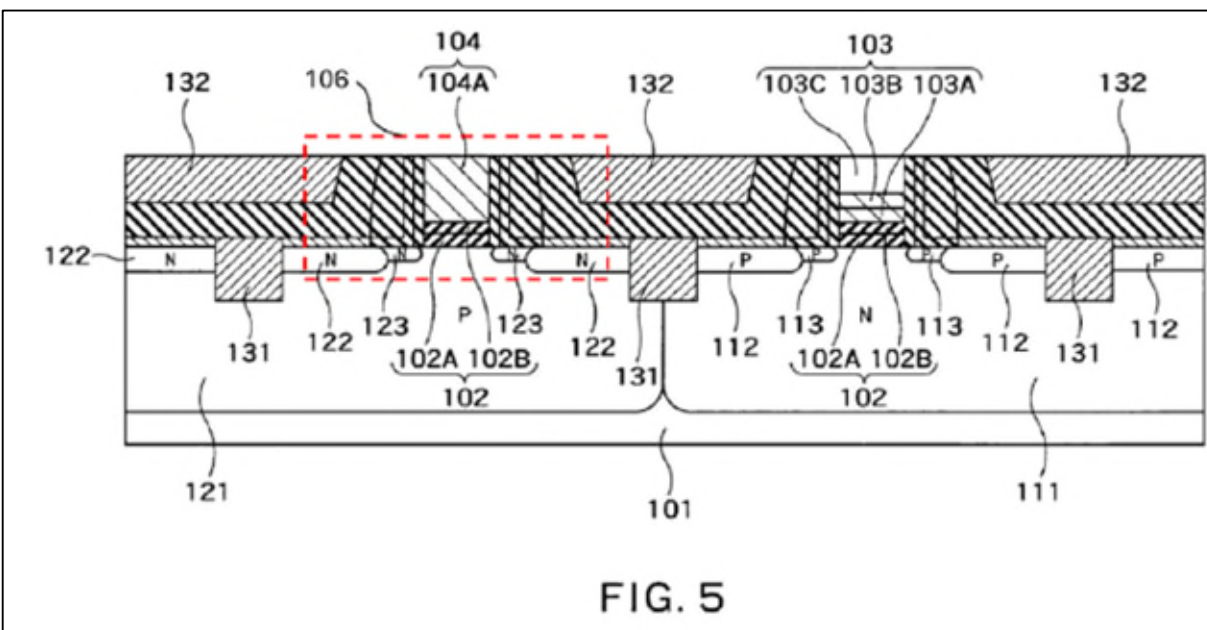
a. Preamble: “A semiconductor device comprising:”

153. Aoyama “relates to a semiconductor device and a manufacturing method thereof, for example, to a semiconductor device which includes a PMOSFET and an NMOSFET which are constituted by high-permittivity gate dielectric films (high-k gate dielectric films) and metal gate electrodes, and a manufacturing method thereof.” Ex.1005, ¶3. Aoyama’s “FIG. 5 is a side sectional view showing a semiconductor device according to a third embodiment,” which is the embodiment I

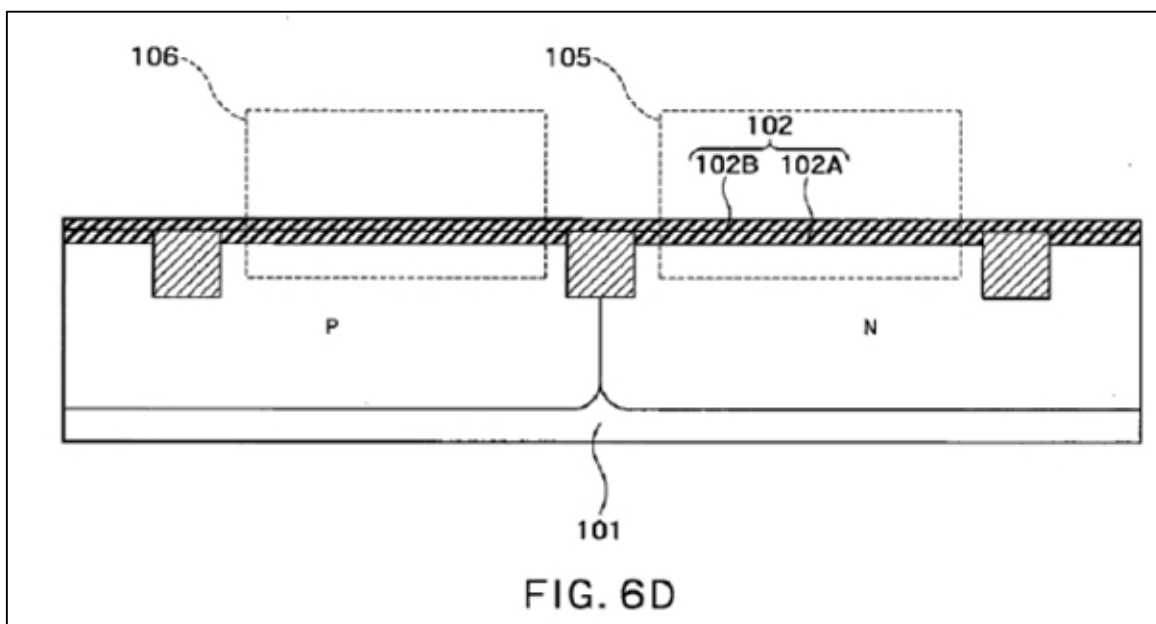


b. Limitation 25[a]: “a first MIS transistor”

155. Aoyama's FIG. 5 device includes "a NMOSFET region 106," which "is a region where the NMOSFET is to be formed" and discloses the claimed first MIS transistor. Ex.1005, ¶106, FIGS. 5 (below), 6D (below).



Ex.1005, FIG. 5 (annotated)

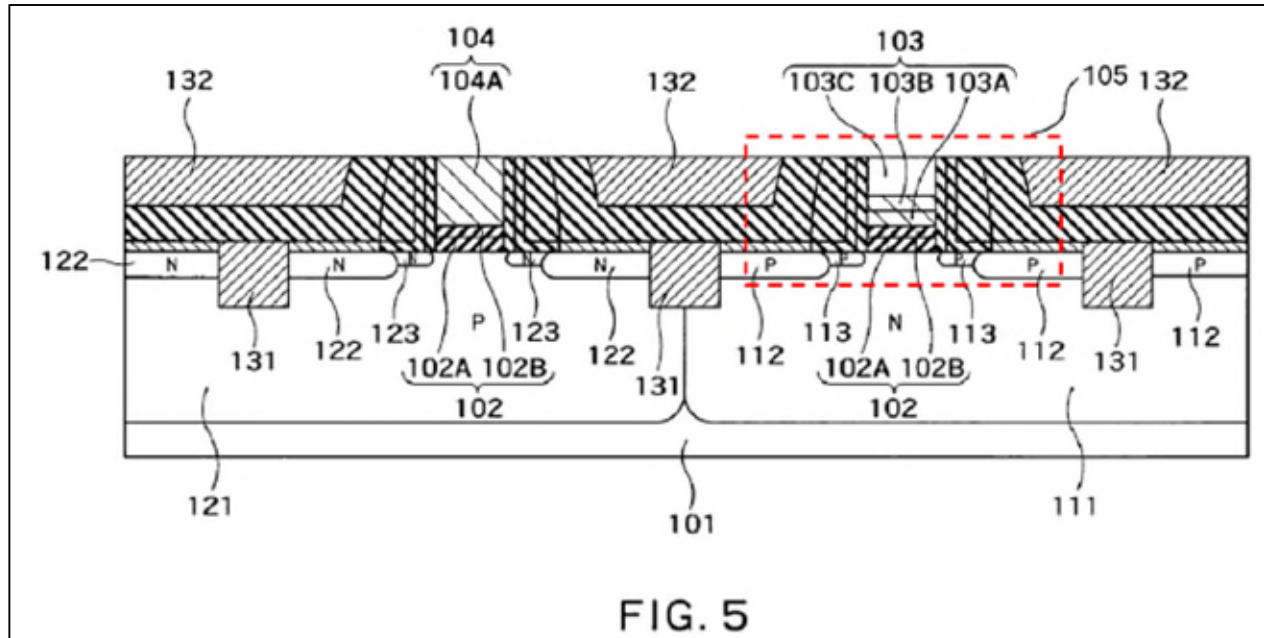


Ex.1005, FIG. 6D

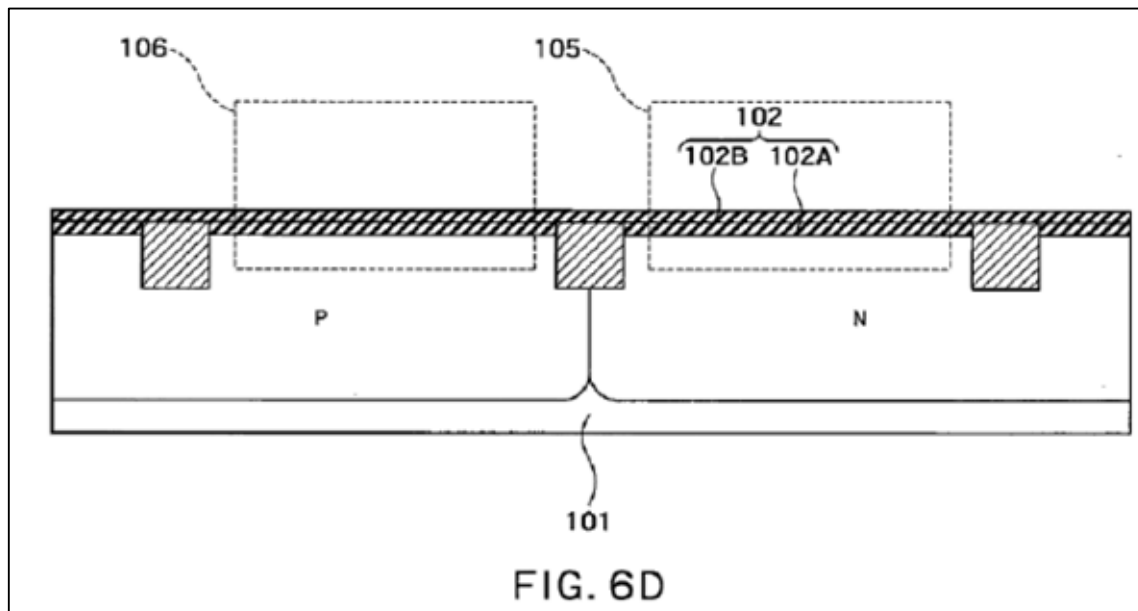
156. Therefore, it is my opinion that Aoyama combined with Hsu823 discloses this limitation of claim 25 of the '686 patent.

c. Limitation 25[b]: “a second MIS transistor”

157. Aoyama’s FIG. 5 device includes a “PMOSFET region 105,” which “is a region where the PMOSFET is to be formed” and discloses the second MIS transistor. Ex.1005, ¶106, FIGS. 5 (below), 6D (below).



Ex.1005, FIG. 5 (annotated)



Ex.1005, FIG. 6D

158. Therefore, it is my opinion that Aoyama combined with Hsu823 discloses this limitation of claim 25 of the '686 patent.

d. Limitation 25[c]: “the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate”

Limitation 25[g]: “the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate”

159. Aoyama discloses a gate insulating film 102 that in my opinion is identical to the gate insulating film the '686 patent describes in its specification (i.e., a 2 nm-thick hafnium silicon oxynitride film formed on a 0.8 nm-thick silicon oxide film. *Compare* Ex.1001, 11:25-37, 29:16-24, with Ex.1005, ¶106. Because Aoyama and the '686 patent identically disclose the same gate dielectric film structure,

Aoyama discloses the claimed “first gate insulating film” and “second gate insulating film.”

160. More specifically, gate dielectric film 102 (including both gate dielectric films 102A and 102B) in Aoyama’s nFET region 106 discloses a “first gate insulating film” and gate dielectric film 102 (including both gate dielectric films 102A and 102B) in Aoyama’s pFET region 105 discloses a “second gate insulating film.”

161. Aoyama’s gate dielectric film 102 also is identical to the gate insulating film structure disclosed by the ’686 patent (i.e., a 2 nm-thick hafnium silicon oxynitride film formed on a 0.8 nm-thick silicon oxide film. The ’686 patent discloses “an underlying film . . . made of a silicon oxide film having a thickness of about 0.8 to 1 nm” and “a gate insulating film formation film 13 made of, for example, a high-k film having a thickness of 2 nm.” Ex.1001, 11:25-37. According to the ’686 patent, “examples of the gate insulating film formation film 13 . . . include hafnium-based oxides such as . . . hafnium silicon oxynitride (HfSiON).” *Id.*, 29:16-24.

162. As FIG. 5 shows, Aoyama identically discloses “a silicon oxide film . . . 102A with a thickness of 0.5 to 0.8 nm” and “a hafnium silicon oxynitride film 102B” “with a thickness of about 2.0 nm.” Ex.1005, ¶106.

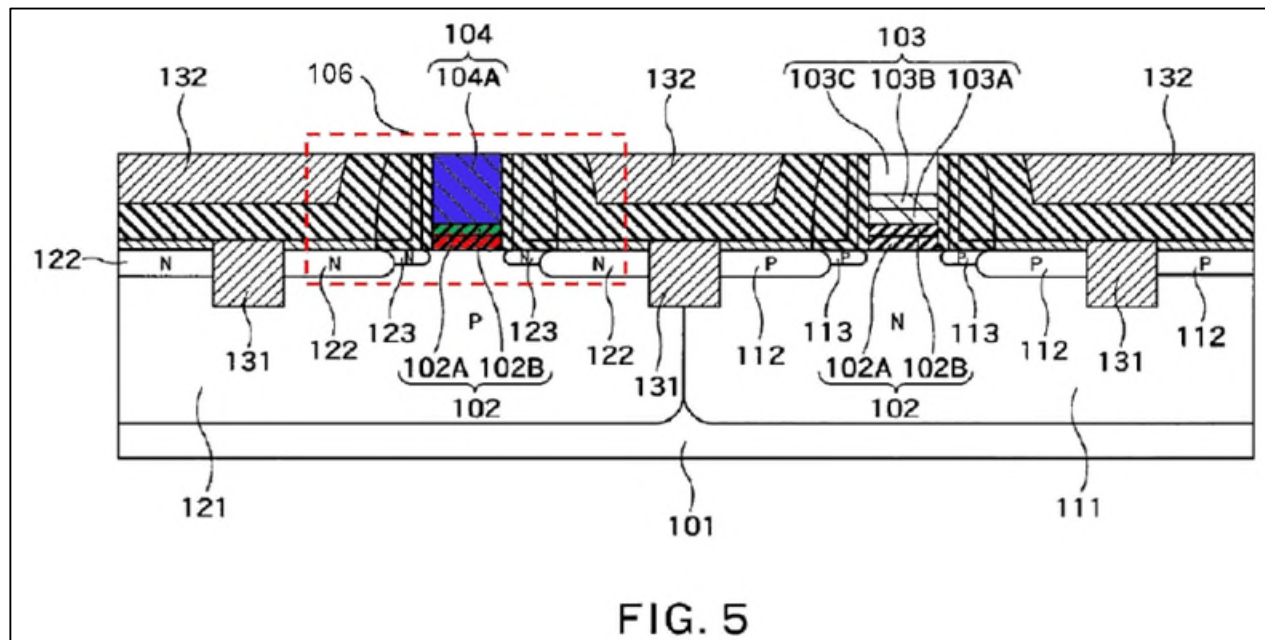
163. Should it be determined that only part of the gate dielectric film structure qualifies as the claimed “gate insulating film,” either Aoyama’s gate dielectric film

102A alone or Aoyama's gate dielectric film 102B alone in Aoyama's nFET region 106 also discloses a "first gate insulating film." Likewise, either Aoyama's gate dielectric film 102A alone or Aoyama's gate dielectric film 102B alone in Aoyama's pFET region 105 also discloses a "second gate insulating film."

164. Therefore, it is my opinion that Aoyama combined with Hsu823 discloses these limitations of claim 25 of the '686 patent.

e. Limitation 25[d]: "[the first MIS transistor includes: ...] a first gate electrode including a second metal film formed on the first gate insulating film"

165. In the semiconductor device of Aoyama's FIG. 5 (below), the nFET in region 106 has a gate electrode 104 that comprises a conductive layer 104A, which is "made of [a] conductive metal." Ex.1005, ¶98. Conductive layer 104A discloses the claimed "second metal film." As Aoyama's FIG. 5 shows below, conductive layer 104A is formed on gate dielectric film 102 in region 106, which is the claimed "first gate insulating film."



Ex.1005, FIG. 5 (annotated)

166. Therefore, it is my opinion that Aoyama combined with Hsu823 discloses this limitation of claim 25 of the '686 patent.

f. Limitation 25[e]: “[the first MIS transistor includes: ...] first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative”

167. In Aoyama's third embodiment illustrated in FIG. 5 (above), the nFET in region 106 includes "an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film," both of which "are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE." Ex.1005, ¶111. In region 106, either Aoyama's sidewall spacers 142 alone disclose the claimed "first sidewall spacers," or Aoyama's offset spacers 141

and sidewall spacers 142, collectively, disclose the claimed “first sidewall spacers” in my opinion.

168. In my opinion, a POSITA would have recognized that Aoyama’s sidewall spacers 142, which are made of silicon oxide, and Aoyama’s offset spacers 141, which are made of silicon oxide or silicon nitride, are both insulative. A POSITA would have understood silicon oxide and silicon nitride to be old and prominent insulating materials used in semiconductor manufacturing.

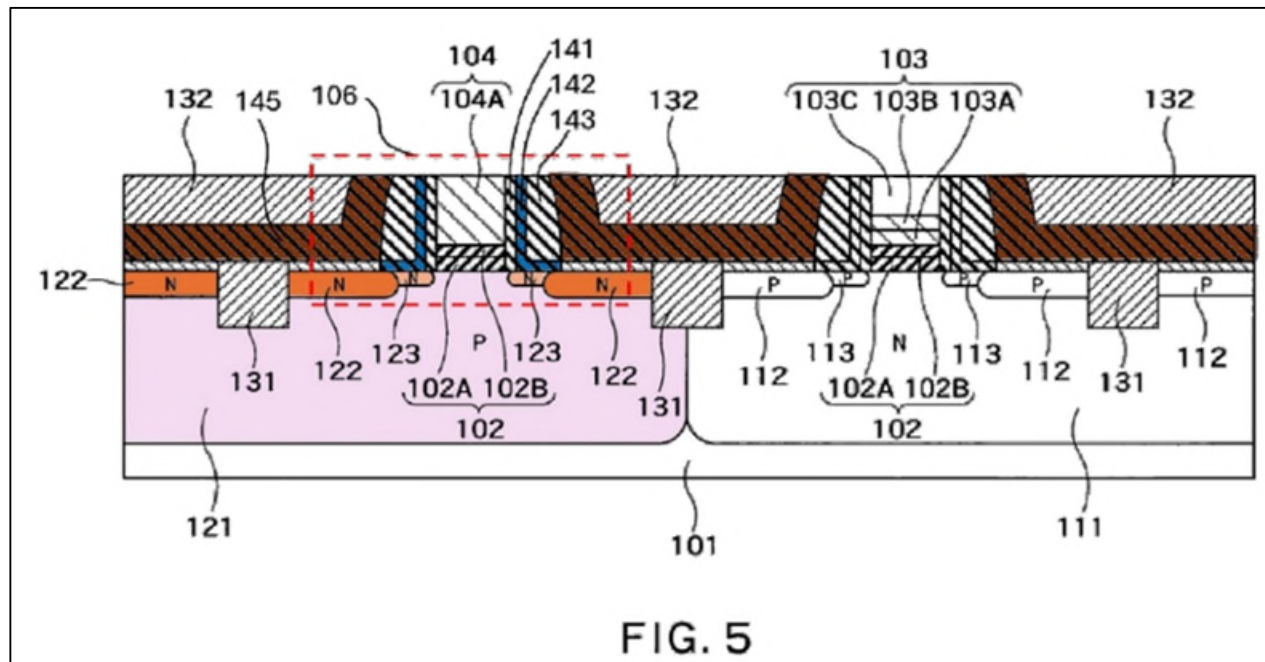
169. Therefore, it is my opinion that Aoyama combined with Hsu823 discloses this limitation of claim 25 of the ’686 patent.

- g. Limitation 25[f]: “[the first MIS transistor includes: ...] a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers”**

170. The semiconductor device of Aoyama’s FIG. 5 (below) includes an “etch stopper film 145 made of a silicon nitride film.” Ex.1005, ¶113. Etch stopper film 145 discloses the claimed “silicon nitride film” in my opinion.

171. Aoyama explains that etch stopper film 145 “is formed over the entire surface by CVD,” then “planarized by chemical mechanical polishing or etching (dry etching or wet etching)” to expose the area where the nFET and pFET gate electrodes are formed. Ex.1005, ¶113; *see also id.*, ¶¶114-119, FIGS. 5, 6K-6Q. As FIG. 5 shows

below, Aoyama's silicon nitride etch stopper film 145 (brown) extends over the side surfaces of the nFET gate electrode (gate electrode 104) on which the gate sidewalls (sidewall spacer 142 (blue) alone or together with offset spacer 141 (not colored)) are formed.



Ex.1005, FIG. 5 (annotated)

172. As FIG. 5 (above) also shows, silicon nitride etch stopper film 145 (brown) extends over upper surfaces of the first active region (NMOSFET region 106) located laterally outside of the gate sidewalls (sidewall spacer 142 (blue) alone or together with offset spacer 141 (not colored)).

173. Therefore, it is my opinion that Aoyama combined with Hsu823 discloses this limitation of claim 25 of the '686 patent.

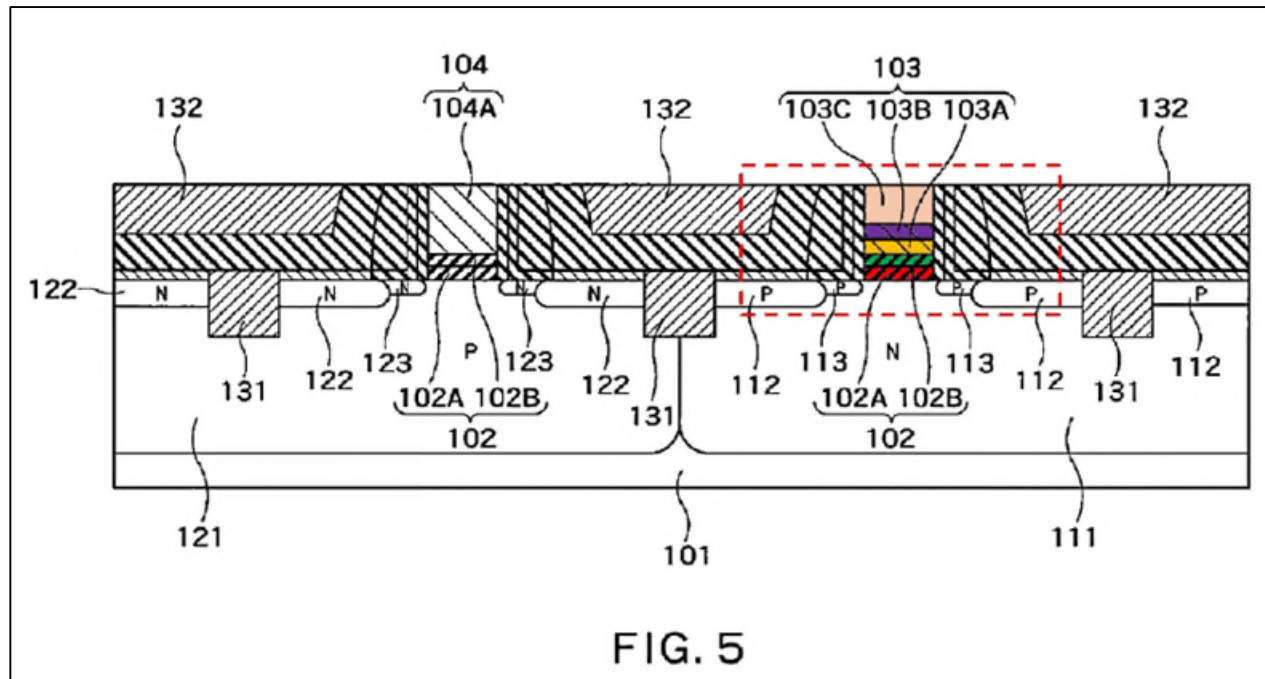
h. Limitation 25[h]: “[the second MIS transistor includes: ...] a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film”

174. In the semiconductor device of Aoyama’s FIG. 5 (below), the pFET in region 105 has a gate electrode 103 that comprises (1) a “conductive layer 103A which is made of conductive metal,” (2) a “conductive layer 103B which is made of conductive metal,” and (3) a “semiconductor layer (silicide layer) 103C” comprising a “polysilicon or amorphous silicon” layer and a “Ni monosilicide (NiSi)” layer. Ex.1005, ¶¶98, 107, 114, 121.

175. In my opinion, Aoyama’s silicon layer (silicide layer) 103C is just like the uppermost portion of gate electrode 30B in the ’686 patent (i.e., a polysilicon or amorphous silicon layer in which a nickel silicide layer is formed). See Ex.1001, 11:50-67 (disclosing “a silicon film 15 made of, for example, a polysilicon film” that is patterned into “a second silicon film 15b” in the pFET active region), 29:41-45 (“[A]lthough a polysilicon film is used as the silicon film 15 . . . , a silicon film made of other semiconductor materials, such as an amorphous silicon film, a silicon film and the like, may be used.”), 21:25-35 (explaining that “a metal silicide film 34 made of nickel silicide [is formed] in an upper portion of the second silicon film 15b”).

176. Thus, Aoyama’s “conductive layer 103B which is made of conductive metal” discloses the claimed “first metal film.” Ex.1005, ¶98. As Aoyama’s FIG. 5

105, which is the claimed “second gate insulating film.”



Ex.1005, FIG. 5 (annotated)

“conductive film” in my opinion.

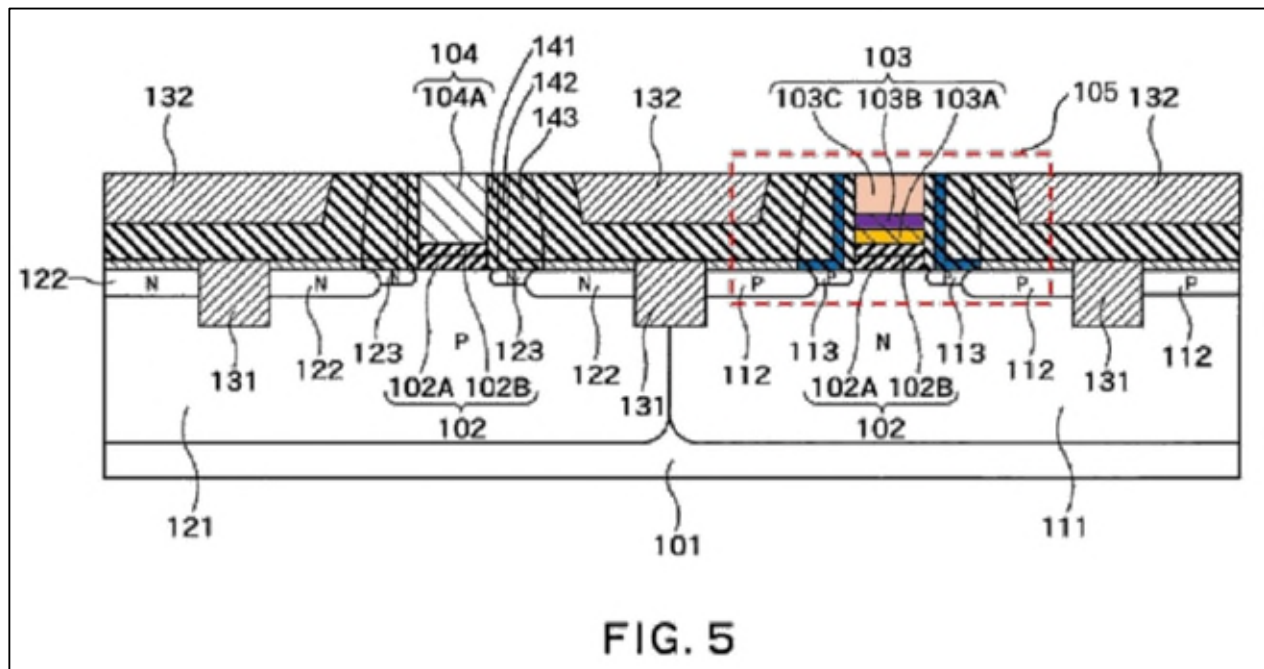
semiconductor (silicide). For this reason, in the third embodiment, the gate resistance

of the PMOSFET is relatively low.” Ex.1005, ¶121. In my opinion, a POSITA would have understood this means semiconductor layer (silicide layer) 103C is conductive.

179. Therefore, it is my opinion that Aoyama combined with Hsu823 discloses this limitation of claim 25 of the ’686 patent.

i. Limitation 25[i]: “[the second MIS transistor includes: ...] second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative”

180. In the semiconductor device of Aoyama’s FIG. 5 (below), the pFET in region 105 includes “an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film,” both of which “are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE.” Ex.1005, ¶111. In region 105, in my opinion, either Aoyama’s sidewall spacers 142 alone (shaded in blue above) disclose the claimed “second sidewall spacers,” or Aoyama’s offset spacers 141 and sidewall spacers 142, collectively, disclose the claimed “second sidewall spacers.”



Ex.1005, FIG. 5 (annotated)

181. In my opinion, a POSITA would have understood that Aoyama's sidewall spacers 142, which are made of silicon oxide, and Aoyama's offset spacers 141, which are made of silicon oxide or silicon nitride, are both insulative. A POSITA would have further understood that silicon oxide and silicon nitride are old and prominent insulating materials used in semiconductor manufacturing.

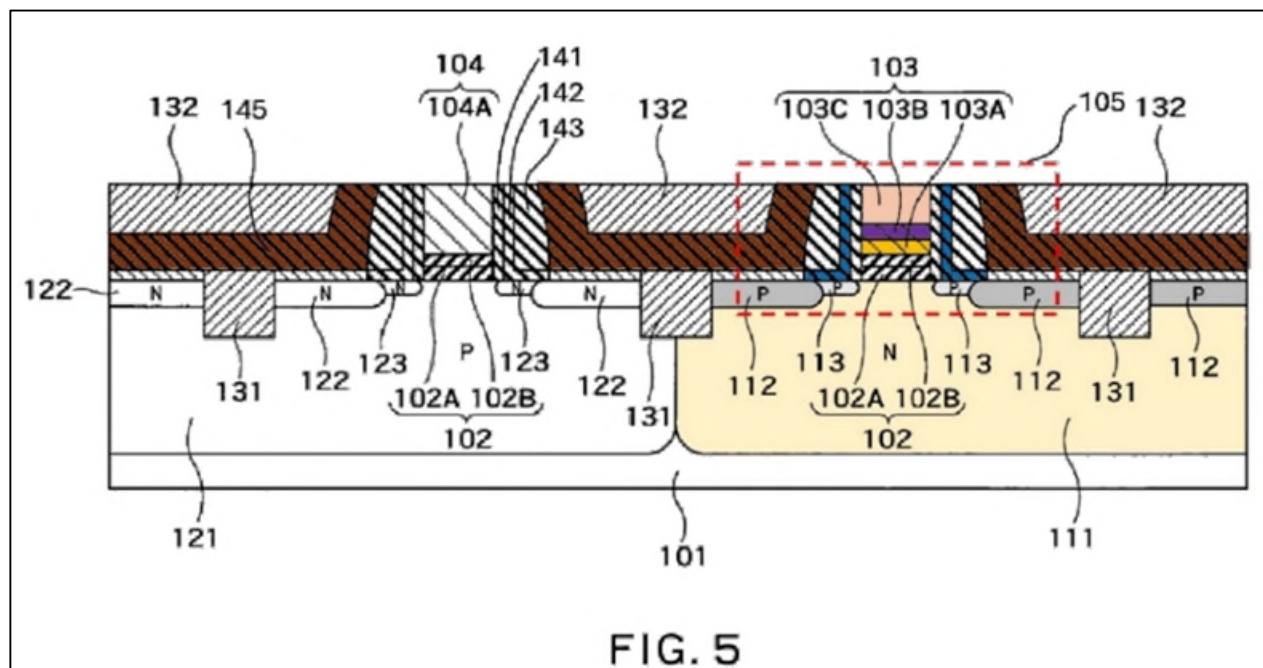
182. Therefore, it is my opinion that Aoyama combined with Hsu823 discloses this limitation of claim 25 of the '686 patent.

- j. **Limitation 25[j]: “[the second MIS transistor includes: ...] the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers”**

183. The third embodiment semiconductor device of Aoyama’s FIG. 5 includes an “etch stopper film 145 made of a silicon nitride film.” Ex.1005, ¶113. In my opinion, the etch stopper film 145 discloses the claimed “silicon nitride film.”

184. Aoyama explains that etch stopper film 145 “is formed over the entire surface by CVD,” then “planarized by chemical mechanical polishing or etching (dry etching or wet etching)” to expose the area where the nFET and pFET gate electrodes will be formed. Ex.1005, ¶113; *see also id.*, ¶¶114-119, FIGS. 5, 6K-6Q.

185. As FIG. 5 (below) shows, Aoyama’s silicon nitride etch stopper film 145 (brown) extends over the side surfaces of the pFET gate electrode (gate electrode 103) on which the gate sidewalls (sidewall spacer 142 (blue) alone or together with offset spacer 141 (not colored)) are formed. *See* Ex.1005, FIG. 5.



Ex.1005, FIG. 5 (annotated)

186. As FIG. 5 (above) also shows, silicon nitride etch stopper film 145 (brown) extends over upper surfaces of the second active region (PMOSFET region 105) located laterally outside of the gate sidewalls (sidewall spacer 142 (blue) alone or together with offset spacer 141 (not colored)).

187. Therefore, it is my opinion that Aoyama combined with Hsu823 discloses this limitation of claim 25 of the '686 patent.

k. Limitation 25[k]: “the first and second metal films are made of different metal materials”

188. As I explain above, Aoyama's conductive layer 104A discloses the claimed "second metal film" (in the nFET region). In Aoyama's third embodiment shown in FIG. 5, the exemplary metal material used to form conductive layer 104A is TaCN. Ex.1005, ¶118. As I also explain above, Aoyama's conductive layer 103B

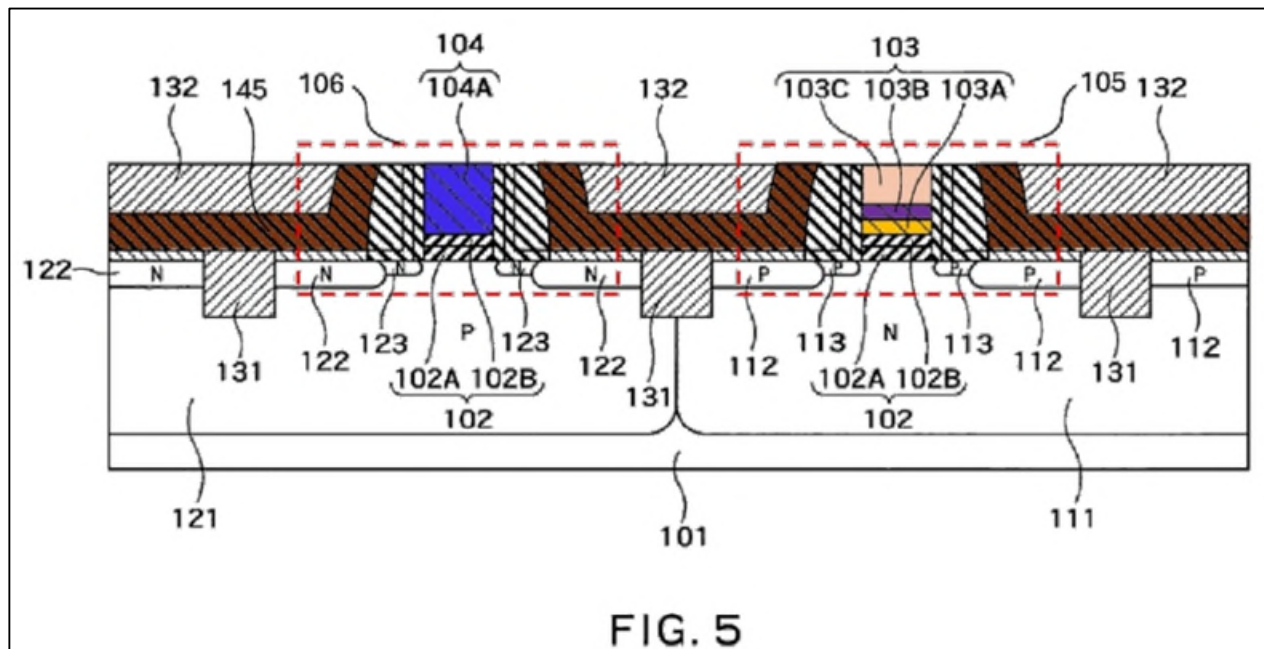
discloses the claimed “first metal film” (in the pFET region). In Aoyama’s third embodiment shown in FIG. 5, the exemplary metal material used to form conductive layer 103B is TiN. *Id.*, ¶107.

189. Thus, the first metal film (i.e., conductive layer 103B) is made of a different metal material than the second metal film (i.e., conductive layer 104B). See Ex.1005, ¶¶107, 118. Specifically, titanium nitride (TiN) and tantalum carbonitride (TaCN) are different metal materials.

190. Therefore, it is my opinion that Aoyama combined with Hsu823 discloses this limitation of claim 25 of the ’686 patent.

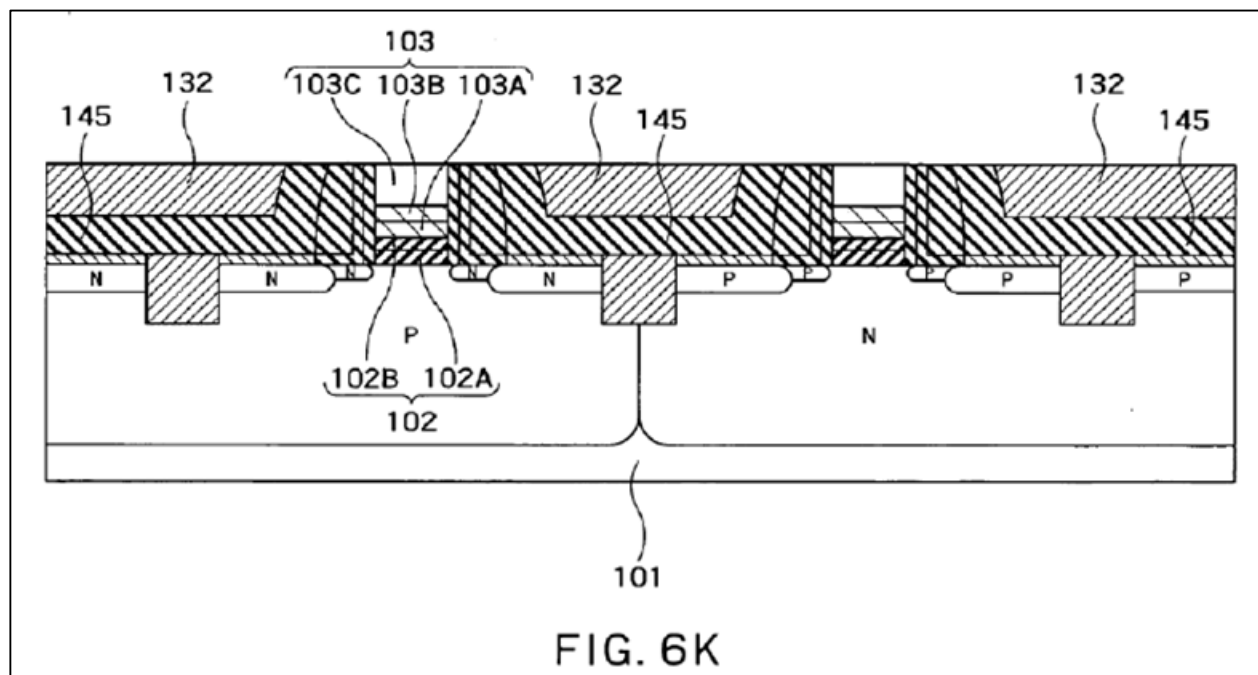
I. Limitation 25[I]: “the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes”

191. In the third embodiment semiconductor device shown in Aoyama’s FIG. 5 (below), silicon nitride etch stopper film 145 is not formed on any upper surfaces of the nFET and pFET gate electrodes 104 and 103, respectively. In my opinion, a POSITA would have recognized this from the manufacturing process Aoyama discloses.



Ex.1005, FIG. 5 (annotated)

192. As Aoyama's FIGS. 6J-6K illustrate, gate electrode 103, which serves as a pFET gate electrode as well as a dummy gate electrode for the nFET, is formed where the nFET and pFET gate electrodes will be located. Ex.1005, ¶109. As FIG. 6K (below) shows, silicon nitride etch stopper film 145 and interlayer dielectric film 132 are formed over the pFET gate electrode 103 (right side) and the nFET dummy gate electrode 103 (left side). *Id.*, ¶113.



Ex.1005, FIG. 6K

193. As Aoyama explains, etch stopper film 145 is “formed over the entire surface” of the semiconductor device, then “planarized” so that “semiconductor layer[] 103C . . . [is] exposed both in the PMOSFET region 105 and the NMOSFET region 106.” Ex.1005, ¶113. Thereafter, semiconductor layer 103C and conductive layers 103B and 103A are removed from the nFET dummy gate electrode in region 106 and replaced with conductive layer 104A, thereby forming gate electrode 104. *Id.*, ¶¶114-119, FIGS. 6M-6Q. In my opinion, a POSITA would have understood this process prevents silicon nitride etch stopper film 145 from being located on any upper surface of the first or second gate electrode.

194. Therefore, it is my opinion that Aoyama combined with Hsu823 discloses this limitation of claim 25 of the '686 patent.

m. Limitation 25[m]: “the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region”

195. As I explain above, Aoyama’s silicon nitride etch stopper film 145 discloses the claimed “silicon nitride film.” In my opinion, a POSITA would have found it obvious to implement Aoyama’s etch stopper film 145 as a tensile etch stop layer to “cause[] . . . stress in a gate length direction of a channel region in” Aoyama’s nFET, which is the claimed “first active region.”

196. In my opinion, Hsu823 discloses a similar contact etch stop layer (CESL) 34 made of silicon nitride and formed in a manner that causes tensile stress in a gate length direction of a channel region in the active region of the nFET device. Hsu823 explains why doing so would have been beneficial:

With circuits becoming smaller and faster, improvement in device driving current is becoming more important, which can be increased by improving carrier mobility. Among efforts made to enhance carrier mobility, forming a stressed channel region is a known practice. The performance of a MOS device can be enhanced through a stressed-surface channel. This technique allows performance to be improved at a constant gate length without adding complexity to circuit fabrication or design.

Research has revealed that a bi-axial, in-plane tensile stress field can improve NMOS performance, and a compressive stress parallel to the channel length direction can improve PMOS device performance. A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device. The stressed CESLs introduce stress into the

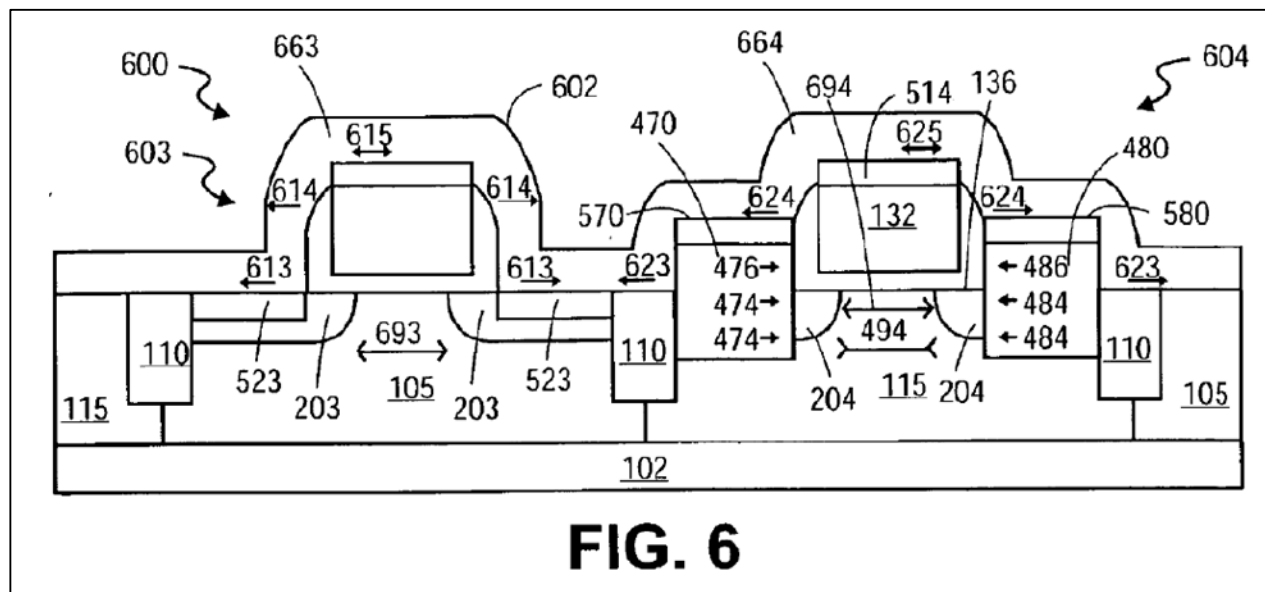
channel region. Therefore, the carrier mobility is improved.

Ex.1006, ¶¶2-3; *see also* Ex.1531, ¶103 (“A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device. The stressed CESLs introduce stress into the channel region. Therefore, the carrier mobility is improved.”).

197. In my opinion, a POSITA would have been motivated to implement Aoyama’s silicon nitride etch stopper film 145 as a tensile layer covering both pFET and nFET devices, which was well-known in the art to improve electron mobility in the nFET channel regions. *See* Section V.F above. Morin, for instance, explains that “in low cost / low power CMOS flow approaches, it is important to work to improve nMOS transistors since other solutions . . . can enhance the pMOS performances. As a result, in these technologies, process induced stress engineering is dedicated to electron mobility enhancement, so by using tensile nitride as CESL.” Ex.1528, 356; *see also* Ex.1526, ¶5 (“For n-MOS devices, carrier mobility (i.e. electron mobility) is enhanced by generating a tensile strain in the transistor’s channel region.”); Ex.1006, ¶39 (teaching the option of applying a tensile CESL over both pFET and nFET devices because “the performance of PMOS devices can be easily improved . . . , while the performance of NMOS devices is relatively difficult to improve”); Ex.1530, 1-2 (“[T]he same tensile capping layer (stress: 1GPa; thickness:

700A) was applied to both [the] USP and tensile-CESL process[es] Significant drive current enhancement of both N/PMOS is achieved with insertion of this USP in standard CMOS flow.”), Tbls. I-II, Figs. 1-7; Ex.1523, Fig. 5(c).

198. If SiGe source/drain stressors are present, as they optionally are in the semiconductor device of the Aoyama-Hsu823 combination, Bohr683 explains that a net compressive stress still exists in the pFET channel region when a tensile CESL is formed over both pFET and nFET devices to apply tensile stress to the nFET channel region. For example, Bohr683’s FIG. 6 illustrates this below.



Ex.1527, FIG. 6

Ex.1527, ¶¶[0038]-[0039], FIG. 6 (above); *see also* Ex.1006, ¶39 (teaching the option of applying a tensile CESL over both pFET and nFET devices because “the performance of PMOS devices can be easily improved with SiGe stressors, while the

performance of NMOS devices is relatively difficult to improve”); Ex.1528, 356 (“[I]t is important to work to improve nMOS transistors since other solutions . . . can enhance the pMOS performances. As a result, in these technologies, process induced stress engineering is dedicated to electron mobility enhancement, so by using tensile nitride as CESL.”); Ex.1530, 1-2 (“[T]he same tensile capping layer (stress: 1GPa; thickness: 700Å) was applied to both [the] USP and tensile-CESL process[es] Significant drive current enhancement of both N/PMOS is achieved with insertion of this USP in standard CMOS flow.”), Tbls. I-II, Figs. 1-7; Ex1.023, Fig. 5(c).

199. In my opinion, a POSITA would have reasonably expected to succeed at implementing Aoyama’s silicon nitride etch stopper film 145 as a tensile layer because such tensile CESLs were widely used to improve carrier mobility in nFETs. *See* Section V.F above. Moreover, it would have been well within a POSITA’s ability to create a tensile silicon nitride CESL film. For example, Jung explains that “a stress-tuned silicon nitride film can be deposited . . . to provide an etch stop layer. . . , as well as to enhance channel mobility in various portions of the device structure.” Ex.1529, ¶90. Jung also describes exemplary recipes for forming a tensile CESL for this purpose. *See id.*, ¶¶99-100 (“Table V shows the deposition conditions for silicon nitride films which were deposited under conditions which provided tensile stress films.”), Tbl. V.

200. Accordingly, it is my opinion that a POSITA would have reasonably expected to succeed at implementing Aoyama's silicon nitride etch stopper film 145 as a tensile layer, as such layers were ubiquitous in the industry by the time the application for the '686 patent was filed.

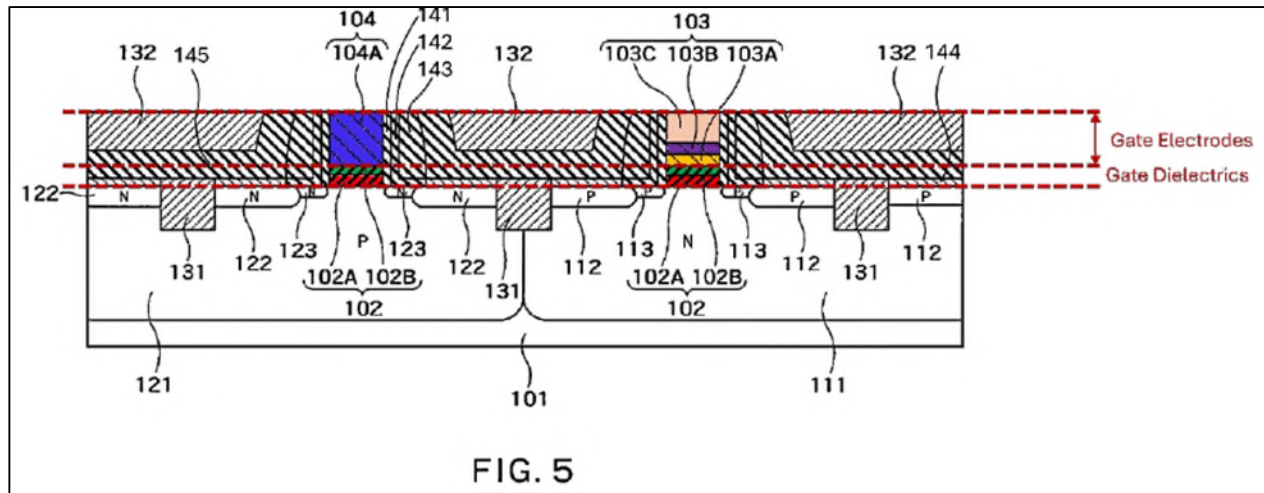
201. Therefore, it is my opinion that Aoyama combined with Hsu823 discloses this limitation of claim 25 of the '686 patent.

3. Dependent Claim 26: "The semiconductor device of claim 25, wherein the first metal film has a thickness smaller than that of the second metal film"

202. As I explain above, Aoyama's conductive layer 104A discloses the claimed "second metal film" and Aoyama's conductive layer 103B discloses the claimed "first metal film." In the third embodiment semiconductor device illustrated in FIG. 5, Aoyama discloses planarizing the device structures after forming conductive layer 104A. *See* Ex.1005, ¶119 ("[A]s shown in FIG. 6Q, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback)."), FIG. 6Q.

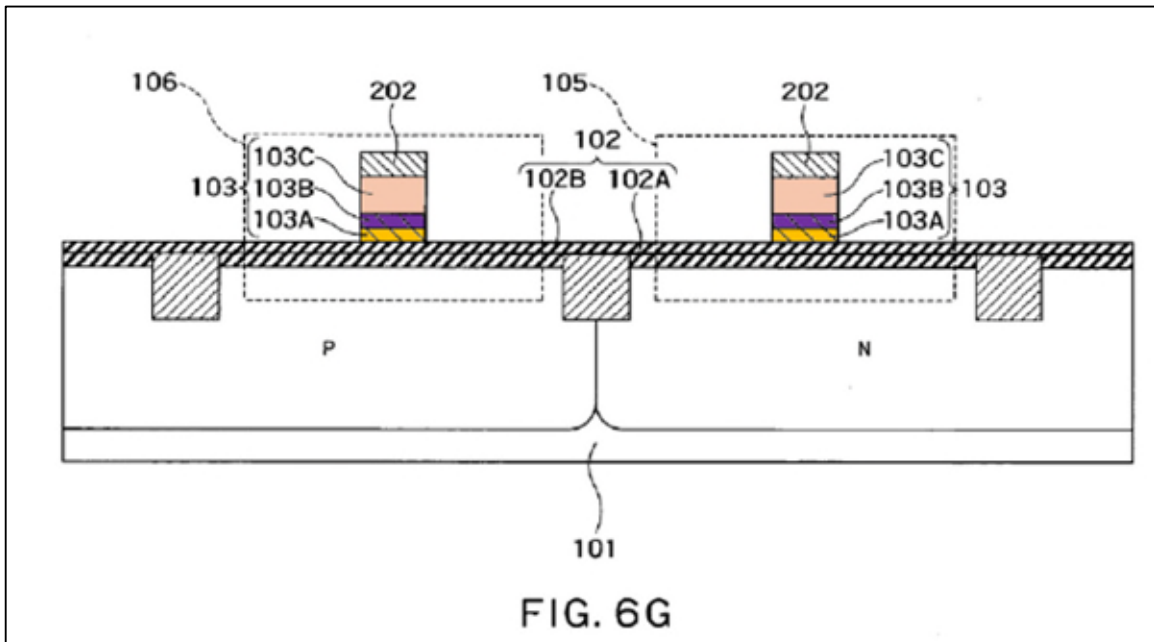
203. As FIG. 5 (below) illustrates, Aoyama's gate electrodes 103 and 104 must have the same thickness because Aoyama's gate electrodes 103 and 104 are both formed on gate dielectric films 102A and 102B, and the gate structures are both planarized to have the same total height. Thus, pFET layers 103A, 103B, and 103C, collectively, have a thickness equal to nFET layer 104A. It follows that the claimed

“first conductive layer” (i.e., conductive layer 103B) is necessarily thinner than the claimed “second conductive layer” (i.e., conductive layer 104A).



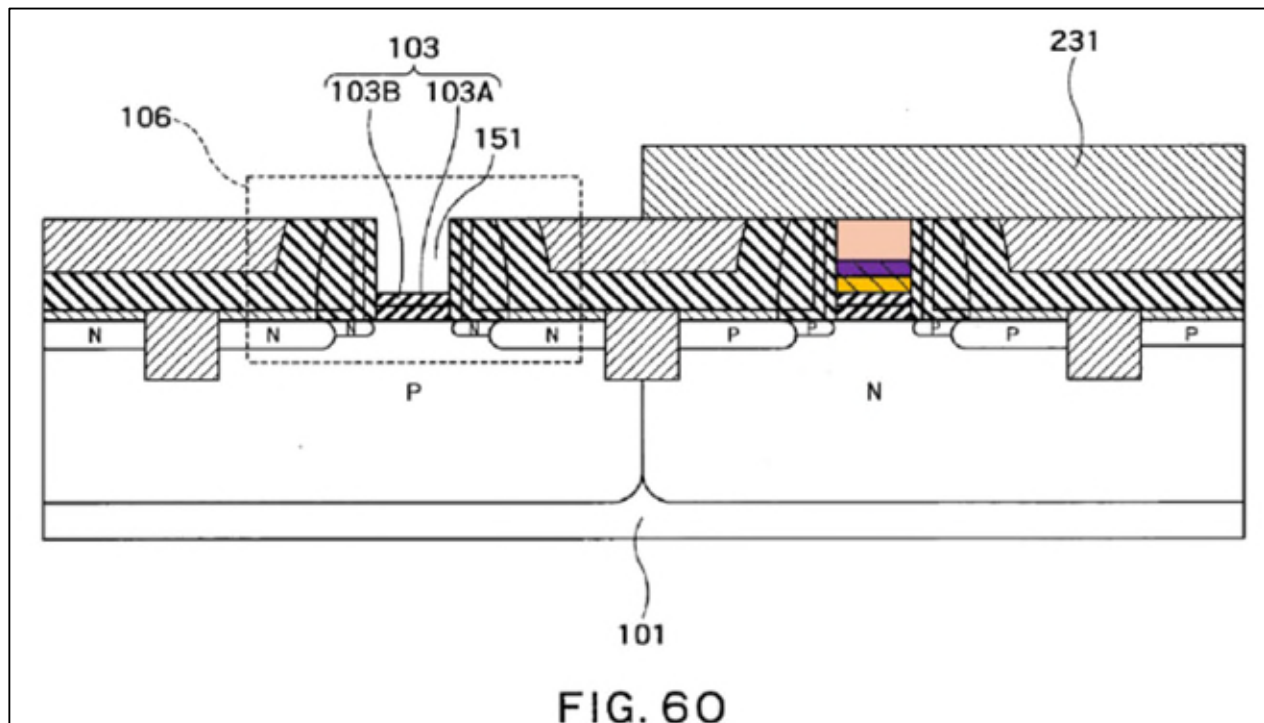
Ex.1005, FIG. 5 (annotated)

204. Aoyama’s process for forming the semiconductor device of FIG. 5 confirms this structure. As FIG. 6G (below) shows, before conductive layer 104A is formed, layers 103A, 103B, and 103C are deposited to form pFET gate electrode 103 and a “dummy gate electrode” 103 for the nFET. Ex.1005, ¶109.



Ex.1005, FIG. 6G (annotated)

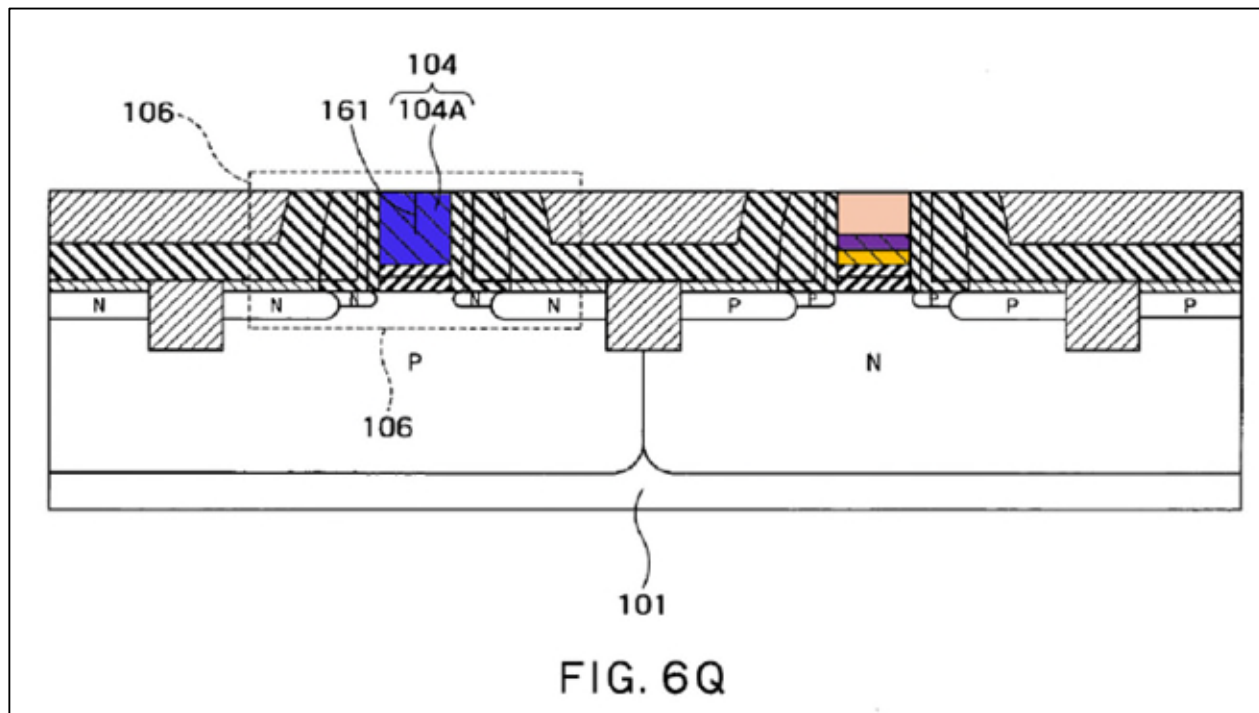
205. As Aoyama's FIGS. 6L-6O show, layers 103A, 103B, and 103C of the nFET dummy gate electrode 103 are then removed in region 106, creating a trench 151 while leaving intact films 102A and 102B comprising the gate dielectric 102. See Ex.1005, ¶¶114-117, FIG. 6O (below).



Ex.1005, FIG. 6O (annotated)

I note that in FIG. 6O, Aoyama's first gate dielectric film 102A, second gate dielectric film 102B, and gate dielectric film 102 are mislabeled 103A, 103B, and 103, respectively. *See id.*, ¶¶115-117, FIGS. 6L-6O.

206. Then, conductive layer 104A is formed in trench 151 left by removing nFET dummy gate electrode 103, thereby forming nFET gate electrode 104, as FIG. 6Q (below) shows. *See* Ex.1005, ¶119, FIG. 6Q.



Ex.1005, FIG. 6Q (annotated)

In this step, the nFET and pFET gate electrodes are planarized to have the same total height. Aoyama explains: “Next, as shown in FIG. 6Q, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback).” Ex.1005, ¶119.

207. In my opinion, a POSITA thus would have understood from Aoyama's manufacturing process Aoyama for the semiconductor device of FIG. 5 that gate electrode 104, which fills the trench 151 left by removing layers 103A, 103B, and 103C of nFET dummy gate electrode 103, has the same thickness as layers 103A, 103B, and 103C, collectively. Accordingly, it follows that the claimed "first conductive layer" (i.e., conductive layer 103B) is necessarily thinner than the claimed "second conductive layer" (i.e., conductive layer 104A).

208. Therefore, it is my opinion that Aoyama combined with Hsu823 discloses claim 26 of the '686 patent.

4. Dependent Claim 27: “The semiconductor device of claim 25, wherein the first and second metal films have different work functions”

209. As I explain above, Aoyama’s conductive layer 104A discloses the claimed “second metal film” and, in the third embodiment shown in FIG. 5, the exemplary metal material used to form conductive layer 104A is TaCN. Ex.1005, ¶118. As I also explain above, Aoyama’s conductive layer 103B discloses the claimed “first metal film” and, in the third embodiment shown in FIG. 5, the exemplary metal material used to form conductive layer 103B is titanium nitride (TiN). *Id.*, ¶107.

210. Aoyama discloses that “metals such as . . . TaCN . . . [have] a work function of 4.3 eV or less,” which increases “to about 4.5 eV” when annealed to about 1,000 °C. Ex.1005, ¶10. By adopting Aoyama’s RMG process for the nFET, however, conductive film 104A never experiences such temperatures, and “[i]t is possible to adopt, for example, a . . . TaCN layer . . . as a metal electrode layer to form the gate electrode 104 for the NMOSFET.” *Id.*, ¶69. That is, Aoyama’s TaCN conductive layer 104A has “a work function of 4.3 eV or less.” *Id.*, ¶10.

211. Further, TiN has “a work function close to that of p+- polycrystalline silicon, such as a work function of 4.8 to 5.3 eV.” Ex.1008, ¶46; *see also id.*, ¶77

(same). Westlinder explains that “[t]he work function of ALD TiN changes from a p-type gate material (5.1 ± 0.1 eV) toward a more midgap material (4.8 ± 0.1 eV) after annealing above ~ 800 °C. The latter is close to what was reported recently for sputtered PVD TiN. It is interesting to note that the work function remains p-type up to 700 °C.” Ex.1533, 551.

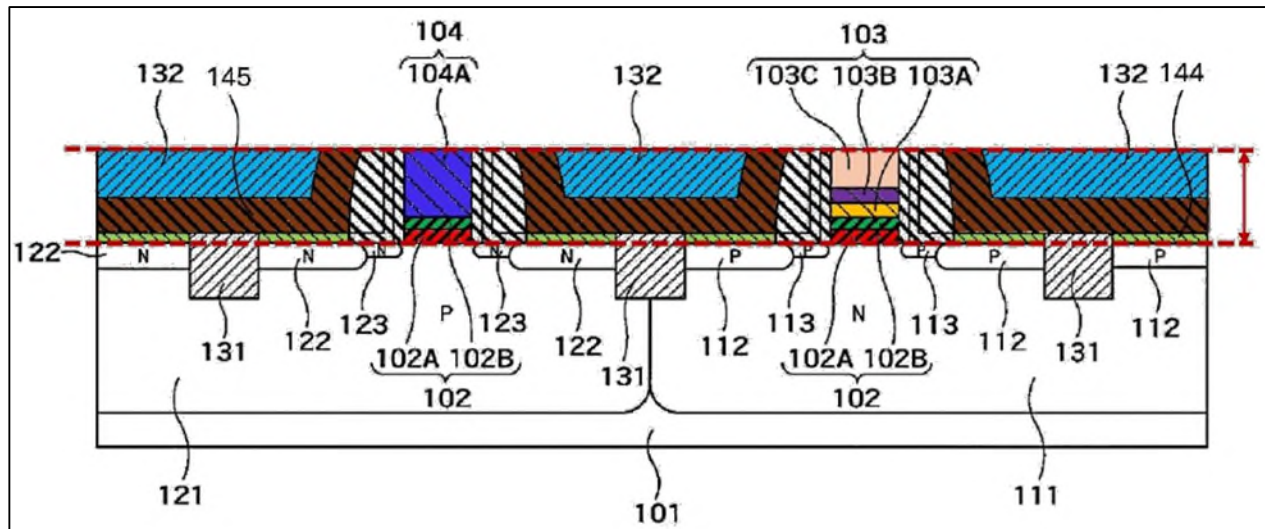
212. Thus, the work functions of TaCN (e.g., 4.3 eV or less) and TiN (e.g., 5.1 eV) are different. In my opinion, in the semiconductor device of Aoyama’s third embodiment in FIG. 5, a POSITA would have understood from Aoyama’s disclosures that the claimed “first metal film” (i.e., conductive layer 103B made of TiN) and the claimed “second metal film” (i.e., conductive layer 104A made of TaCN) have different work functions.

213. Therefore, it is my opinion that Aoyama combined with Hsu823 discloses claim 27 of the ’686 patent.

5. Dependent Claim 28: “The semiconductor device of claim 25, wherein the silicon nitride film has a thickness smaller than that of the first gate electrode”

214. As I explain above, Aoyama’s silicon nitride etch stopper film 145 discloses the claimed “silicon nitride film,” and Aoyama’s gate electrode 104 discloses the claimed “first gate electrode.” Aoyama discloses that silicon nitride etch stopper film 145 has a smaller thickness than Aoyama’s gate electrode 104 because

FIG. 5 (annotated below) shows etch stopper film 145 (brown) is much thinner than gate electrode 104 (purple), consistent with what a POSITA would have expected.



Ex.1005, FIG. 5 (annotated)

215. Moreover, assuming, *arguendo*, CESL 145 is thicker than the gate electrode 104, once interlayer dielectric (ILD) 132 is deposited and the structure planarized, the ILD 132 would have been completely polished away after CMP, contrary to FIG. 5. That is because when CESL 145 is conformally deposited, there will be a step height in CESL 145 corresponding to the height of the gate electrode 104. FIG. 5 shows that CMP to at least a thickness of CESL 145 is being done to expose the top of the gate 104. In that process, the ILD 132 would have been completely removed, contrary to what is shown in FIG. 5.

216. Thus, in my opinion, Aoyama teaches “the silicon nitride film has a thickness smaller than that of the first gate electrode,” as required by claim 28.

217. To the extent this teaching is not found to be an explicit disclosure of “the silicon nitride film has a thickness smaller than that of the first gate electrode,” a POSITA would have found it obvious that Aoyama’s silicon nitride etch stopper film 145 has a smaller thickness than Aoyama’s gate electrode 104 in my opinion.

218. A POSITA would have expected Aoyama’s etch stopper film 145 to have a smaller thickness than gate electrode 104 in my opinion. In the process Aoyama describes for manufacturing its third embodiment semiconductor device, Aoyama’s gate electrodes 103 and 104 are planarized to have the same total height. As Aoyama explains with reference to FIG. 6Q, “the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback).” Ex.1005, ¶119. As a result, and as the red arrow indicates (*see id.*, FIG. 5 (above)), the total height of etch stopper film 145 and interlayer dielectric 132 cannot exceed the total height of the gate dielectric film 102 and gate electrode 104. The following must be true:

$$T_{145} + T_{132} + T_{144} = T_{102} + T_{104} \quad (\text{Eq. 1})$$

where T_x is the thickness of layer x above the substrate. Thus, claim 28 applied to Aoyama requires:

$$T_{145} < T_{104} \quad (\text{Eq. 2})$$

$$T_{104} + T_{132} + T_{144} > T_{102} + T_{104} \quad (\text{Eq. 3})$$

219. Canceling the common variable on both sides of the inequality (i.e., T_{104}) gives the following relationship between the thickness of interlayer dielectric 132, the

thickness of the silicide film 144 extending above the substrate surface, and the thickness of gate dielectric film 102:

$$T_{132} + T_{144} > T_{102} \quad (\text{Eq. 4})$$

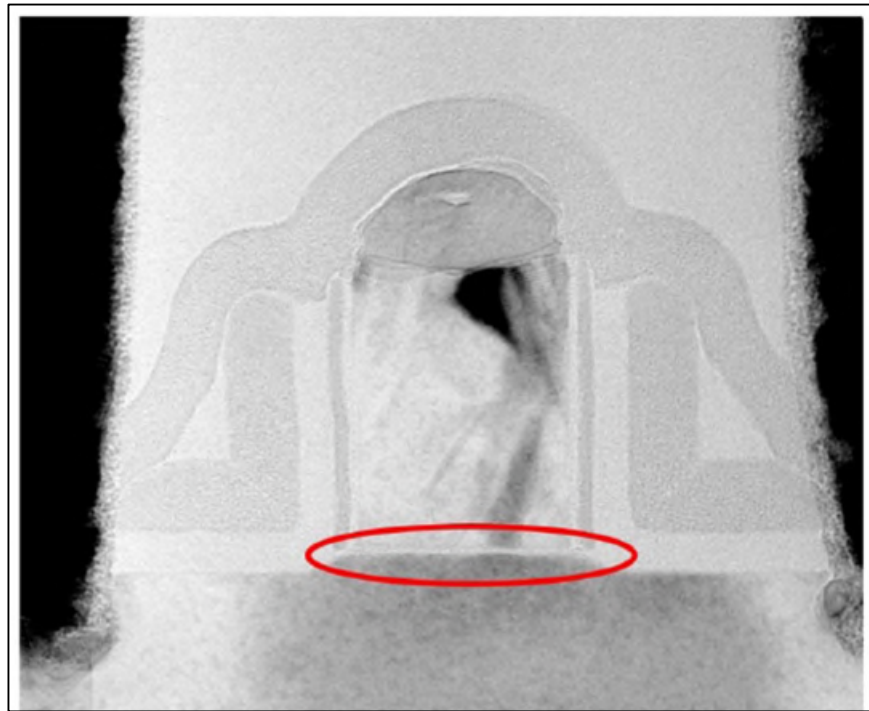
220. Thus, even completely (and improperly) ignoring the thickness of the silicide above the substrate surface (T_{144}), which itself would have been expected to exceed the thickness of gate dielectric film 102, Aoyama satisfies claim 28 so long as the thickness of interlayer dielectric 132 is greater than the thickness of gate dielectric film 102. *See, e.g.*, Ex.1527, ¶37 (“[L]ayers of silicide material 523, 513, 524, and 514 may comprise nickel silicide consuming approximately 20 nanometers of silicon alloy materials 470 and 480 beginning at surfaces 472 and 482 and extending downward, as shown in FIG. 5.”), FIG. 5.

221. This inequality illustrates why a POSITA would have expected Aoyama’s interlayer dielectric 132 to be significantly thicker than gate dielectric film 102 in my opinion and would have found it highly unusual were it otherwise. Factoring in the thickness of silicide film 144 only further confirms my opinion, as silicide film 144 and interlayer dielectric film 132 each would be expected to be thicker than gate dielectric film 102. *See, e.g.*, Ex.1534, ¶326 (providing an exemplary interlayer dielectric film thickness); Ex.1527, ¶37 (providing an exemplary NiSi film thickness). Summing their thicknesses would certainly exceed the thickness of gate dielectric film 102.

222. A POSITA would have known the thickness of a gate dielectric is negligible compared to a gate electrode in my opinion. A POSITA would have known the gate dielectric to be a thin insulating layer, which is necessary to achieve a large capacitance. *See* Ex.1511, xiii (describing “the high drive current and gate capacitance required of scaled MOSFETs”). Interlayer dielectric films, on the other hand, require small capacitance and are thus much thicker. That is, “gate and interlayer (ILD) dielectric films” have “opposing requirements” in terms of thickness. *See id.*

223. According to Aoyama, gate dielectric layer 102A is 0.5-0.8 nm thick, and gate dielectric layer 102B is about 2.0 nm thick, meaning gate dielectric film 102 has a thickness less than 3 nm. *See* Ex.1005, ¶47. Layer 102A is only about 2-3 atomic layers thick, and layer 102B is only about 6-7 atomic layers thick. Thus, Aoyama’s gate dielectric film 102, like all gate dielectric films in this technology, is extremely thin—much thinner than any interlayer dielectric film, as would have been understood by a POSITA.

224. Several semiconductor devices fabricated before the filing of the application that resulted in the ’686 patent illustrate the thickness disparity recited in claim 28 visually. *See* Ex.1525, Figs. 3 (below), 5-6, 8-10, 11 (below), 12; Ex.1516, Fig. 6 (showing Intel’s 45nm device); Ex.1517, 16 (same) (below), 19; Ex.1523, Fig. 2; Ex.1528, Fig. 1.



Ex.1525, Fig. 3 (annotated)

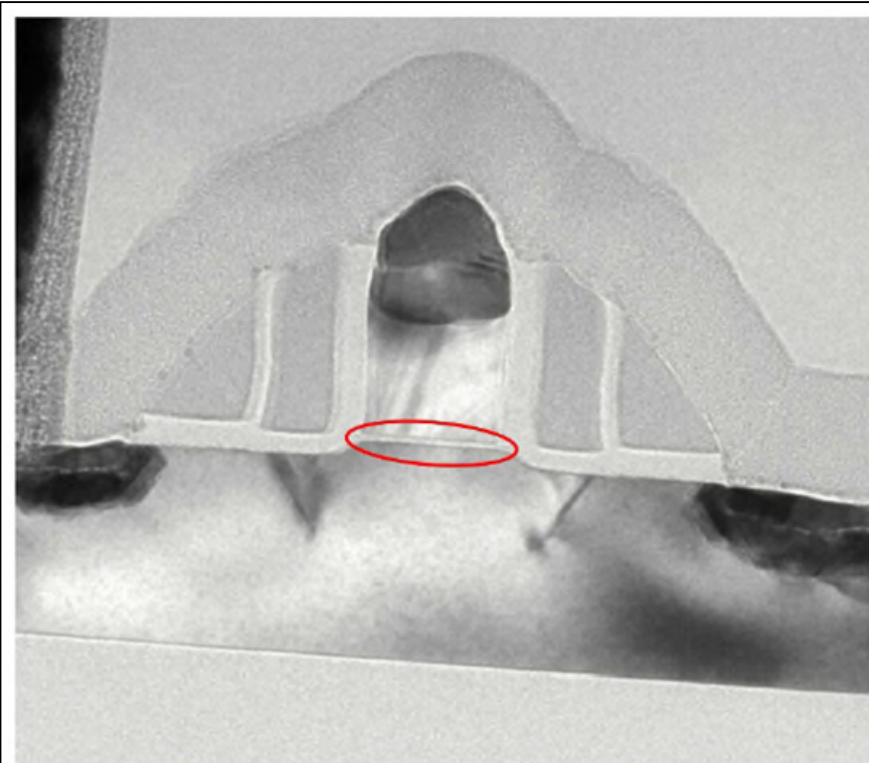
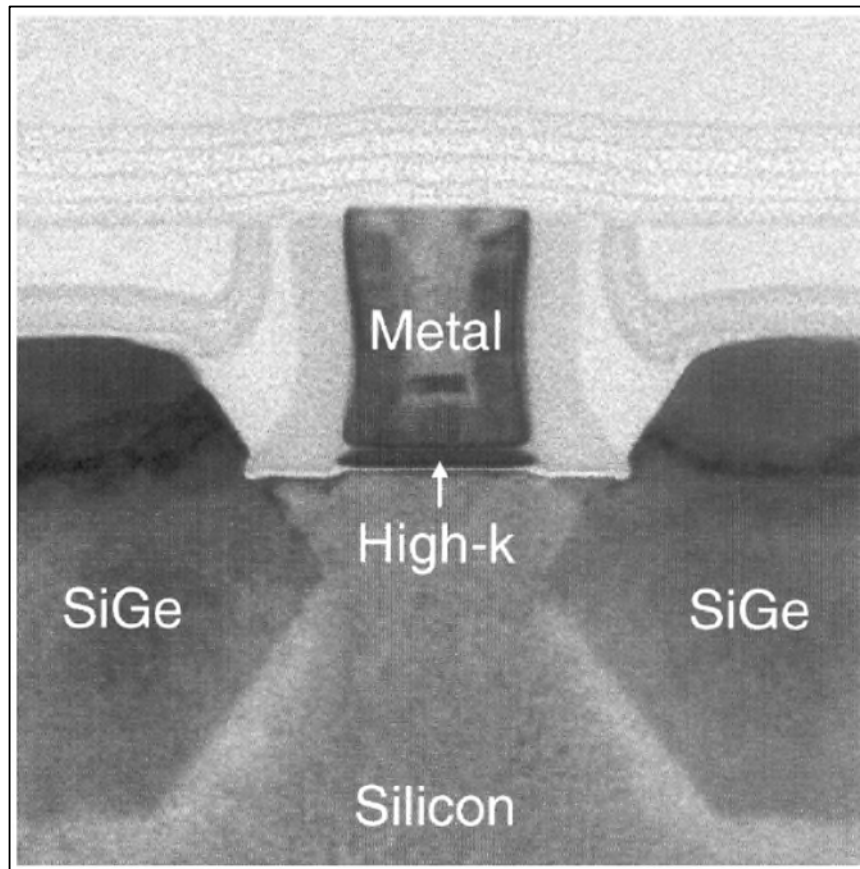


Figure 11. NMOS Transistor in AMD Athlon

Ex.1525, Fig. 11 (annotated)



Ex.1517, 16 (excerpted)

225. As another example that is similar to Aoyama, Nakajima (see FIG. 52 (below)) teaches a metal layer 403 that is 20 nm thick and a metal layer 405 that is 100 nm thick, meaning the gate electrode is at least about 120 nm thick. Ex.1534, ¶317.

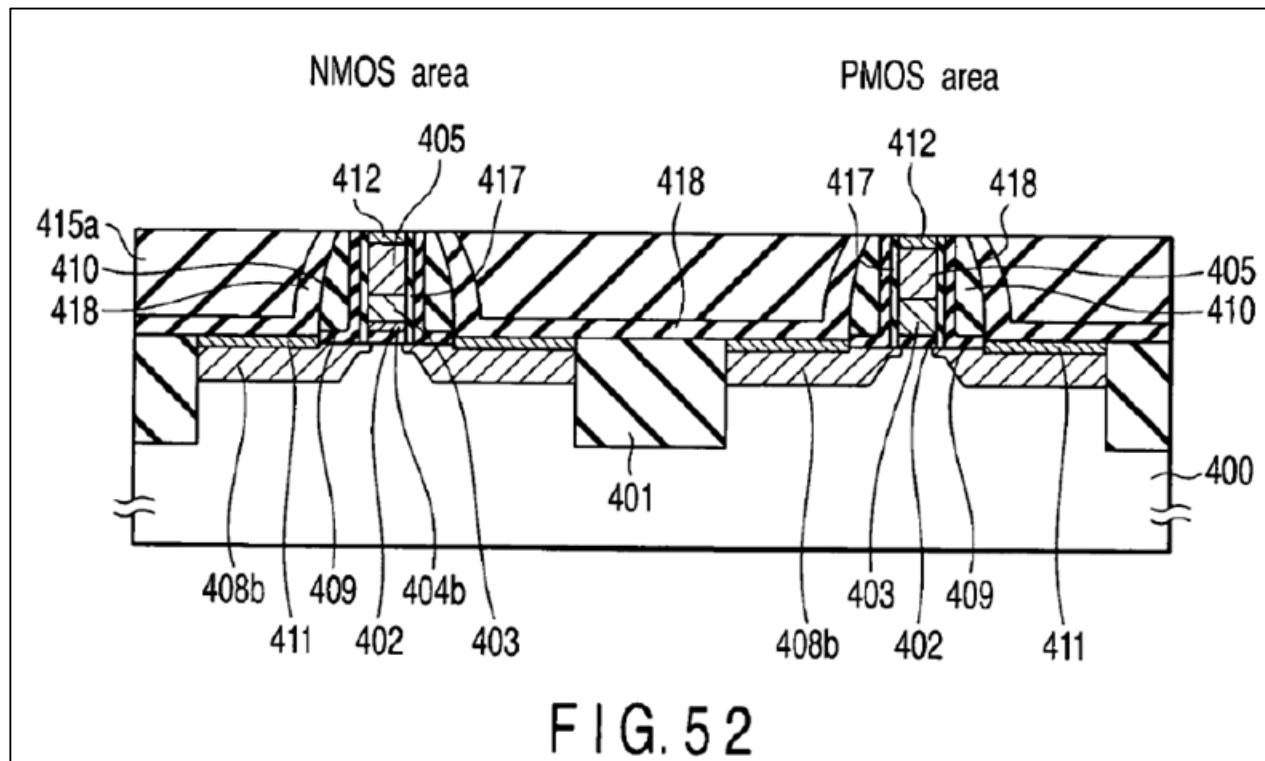


FIG. 52
Ex.1534, FIG. 52

The silicon nitride CESL 418 is only about 30 nm thick, and interlayer insulating layer 415a is initially 250 nm thick before being planarized down to what is still more than 90 nm thick (the difference between the thickness of gate electrode layers 403 and 405, minus the thickness of CESL 418). *Id.*, ¶326, FIGS. 51-52. A thickness of 90 nm is more than an order of magnitude thicker than any conceivable gate dielectric layer, which is indicative of the relative thicknesses a POSITA would have expected.

226. In my opinion, a POSITA also would have found it obvious for Aoyama's etch stopper film 145 to have a smaller thickness than gate electrode 104 is that this was one of only a small number of possibilities and the most well-known of those limited options.

227. In my opinion, there was a design need to make Aoyama's interlayer dielectric 132 thicker than Aoyama's gate dielectric film 102 because "gate and interlayer (ILD) dielectric films" have "opposing requirements" in terms of thickness. See Ex.1511, xiii. This would have indicated to a POSITA that Aoyama's interlayer dielectric 132 should be thicker than Aoyama's gate dielectric film 102. The result, as I explain above, is that Aoyama's etch stopper film 145 would be thinner than Aoyama's gate electrode 104, as required by claim 28.

228. Additionally, the design needs of Aoyama's device dictate only three options for the thickness of Aoyama's etch stopper film 145: either it is thinner than Aoyama's gate electrode 104, it is the same thickness as Aoyama's gate electrode 104, or it is thicker than Aoyama's gate electrode 104. Aoyama's planarized structure sets a restriction that the collective thickness of etch stopper film 145 and interlayer dielectric film 132 cannot exceed the height of Aoyama's gate structures. Of the finite number of identified, predictable solutions that comply with the design requirements of Aoyama's device, an etch stopper film 145 thinner than the gate electrode 104 was within the technical grasp of, and would have been expected by, a POSITA in my opinion. Numerous examples that would have been known to a POSITA before the application for the '686 patent confirm my opinion. See, *e.g.*, Ex.1516, Fig. 6; Ex.1525, Figs. 1-3, 5-6, 8-12; Ex.1528, Fig. 1; Ex.1523, Fig. 2.

229. Further, a POSITA would have found it obvious in my opinion for Aoyama's etch stopper film 145 to have a smaller thickness than gate electrode 104 because the disclosed thickness of Aoyama's gate electrode 104 significantly exceeds the typical thickness used for silicon nitride etch stopper films like Aoyama's etch stopper film 145. Aoyama discloses that gate electrode 104 is thicker than 80 nm because Aoyama's gate electrodes 103 and 104 are planarized to have the same total height. *See* Ex.1005, ¶119, FIG. 6Q.

230. Aoyama discloses that conductive layer 103A is about 20 nm thick, and conductive layer 103B is about 60 nm thick, meaning gate electrode 103 (which further includes semiconductor layer (silicide layer) 103C) is at least thicker than about 80 nm. *See* Ex.1005, ¶107. Because gate electrode 104 must have the same thickness as gate electrode 103, gate electrode 104 is also thicker than 80 nm.

231. In my opinion, a POSITA would have understood that silicon nitride etch stopper films like Aoyama's etch stopper film 145 "ha[ve] a typical thickness of 20 nm" or so, which is much less than the about 80 nm minimum thickness of Aoyama's gate electrode 104. Ex.1535, 1446. A "typical" silicon nitride CESL thickness was less than a typical gate electrode thickness in MOSFETs like Aoyama's. *See* Ex.1534, ¶¶317, 326, FIG. 52; Ex.1516, Fig. 6; Ex.1525, Figs. 1-3, 5-6, 8-12; Ex.1528, Fig. 1; Ex.1523, Fig. 2.

232. Even further, a POSITA would have found it obvious for Aoyama's etch stopper film 145 to have a smaller thickness than gate electrode 104 in my opinion because that the thickness of etch stopper film 145 affects the amount of stress and tuning that thickness would have been a matter of routine optimization. Silicon nitride CESL thickness was a variable that would have been known by a POSITA to affect stress. *See generally* Ex.1535. Eneman, for example, details "[t]he effect [of scaling] on CESL-induced stress" due to silicon nitride CESL films. *Id.*, 1447. Silicon nitride CESL thickness was thus a known, result-effective variable. *See, e.g., id.*, 1447-48, Figs. 2-3.

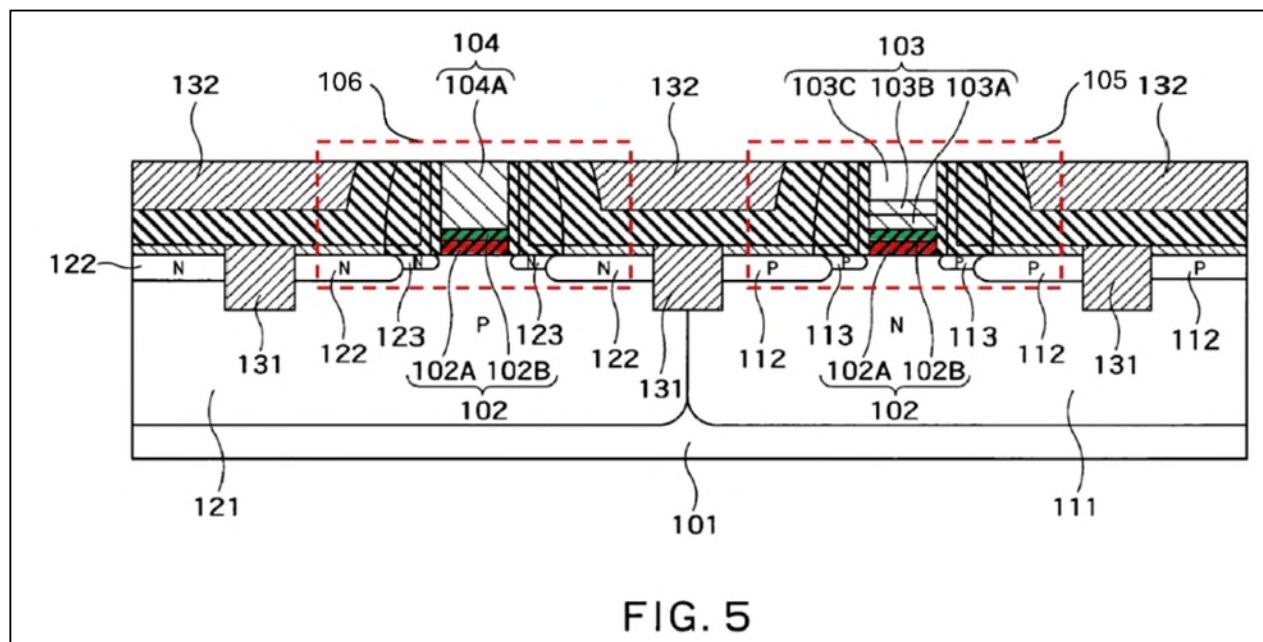
233. Implementing Aoyama's etch stopper film 145 to be thinner than Aoyama's gate electrode 104, as required by claim 28, would not have yielded any unexpected results to a POSITA in my opinion, as the relationship between silicon nitride CESL thickness and the stress it induces was known and predictable. *See generally* Ex.1535 (including Fig. 3).

234. For all of the foregoing reasons, in addition to the relative thicknesses disclosed by Aoyama's FIG. 5 explained above, it is my opinion that Aoyama combined with Hsu823 discloses claim 28 of the '686 patent.

6. Dependent Claim 31: “The semiconductor device of claim 25, wherein the first and second gate insulating films are made of the same insulating material”

235. Aoyama discloses a gate insulating film 102 identical to the gate insulating film the '686 patent describes in its specification (i.e., a 2 nm-thick hafnium silicon oxynitride film formed on a 0.8 nm-thick silicon oxide film. *Compare* Ex.1001, 11:25-37, 29:16-24, *with* Ex.1005, ¶106. Because Aoyama and the '686 Patent identically disclose the same gate dielectric stack, Aoyama discloses that “the first and second gate insulating films are made of the same insulating material” irrespective of how claim 31 is mapped.

236. However, as I explain above, gate dielectric film 102 (including both gate dielectric films 102A and 102B) in Aoyama's region 106 discloses a “first . . . gate insulating film” and gate dielectric film 102 (including both gate dielectric films 102A and 102B) in Aoyama's region 105 discloses a “second gate insulating film.” Since the claimed “first gate insulating film” and “second gate insulating film” are both disclosed by Aoyama's gate dielectric film 102 (including both gate dielectric films 102A and 102B), Aoyama's “gate insulating films are made of the same insulating material.” The gate dielectric film 102 in PMOSFET region 105 is made from the same silicon oxide film 102A and the same hafnium silicon oxynitride dielectric film 102B as the gate dielectric film 102 in NMOSFET region 106. Ex.1005, ¶¶106, 109, FIG. 5 (below).



Ex.1005, FIG. 5 (annotated)

237. Therefore, it is my opinion that Aoyama combined with Hsu823 discloses claim 31 of the '686 patent.

7. Dependent Claim 35: “The semiconductor device of claim 25, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more”

238. As I explain above, Aoyama’s gate dielectric film 102 (including both gate dielectric films 102A and 102B) in nFET region 106 discloses the claimed “first gate insulating film” and Aoyama’s gate dielectric film 102 (including both gate dielectric films 102A and 102B) in pFET region 105 discloses the claimed “second gate insulating film.” Aoyama’s gate dielectric film 102B is formed of hafnium silicon oxynitride. Ex.1005, ¶106. In my opinion, a POSITA would have understood that Aoyama’s gate dielectric film 102B discloses, or at least renders obvious, the

claimed “high-k film made of a metal oxide having a relative dielectric constant of 10 or more.”

239. In particular, in my opinion, a POSITA would have understood that hafnium silicon oxynitride is “a high-k film” because Aoyama refers to it as “a high-permittivity dielectric film,” which is synonymous with “a high-k film” (wherein k or κ being the symbol for dielectric permittivity). Ex.1005, ¶98; *see also* Ex.1514, ¶4 (explaining that “[a] high dielectric constant film made of the above-noted high-k material [referring to hafnium silicon oxynitride] has its dielectricity of more than ten (10)”).

240. The '686 patent discloses that Aoyama's hafnium silicon oxynitride is a “metal oxide having a relative dielectric constant of 10 or more” and also that hafnium silicon oxynitride is an exemplary gate dielectric film. *See* Ex.1001, 29:16-24 (“include hafnium-based oxides such as . . . hafnium silicon oxynitride (HfSiON)”) Aoyama's hafnium silicon oxynitride is “a high-permittivity dielectric film.” Ex.1005, ¶98.

241. In my opinion, a POSITA would have understood that hafnium silicon oxynitride has a dielectric constant of 10 or more. *See* Ex.1514, ¶4 (“[C]ertain films which are made of hafnium (Hf)-containing material such as HfO_2 , HfSiO_x , or HfAlO_x , and oxynitrides thereof are relatively excellent in thermal stability. . . . A high dielectric constant film made of the above-noted highk material has its

dielectricity of more than ten (10)”); Ex.1511, xiii (“Dielectrics with values approximately between 10 and 30 are under consideration.”); Ex.1515, ¶¶2 (explaining that a “high-k dielectric means having a dielectric constant higher than 10”), 8.

242. Therefore, it is my opinion that Aoyama combined with Hsu823 discloses claim 35 of the ’686 patent.

B. Ground II (Akasaka (Ex.1008), Hsu823 (Ex.1006))

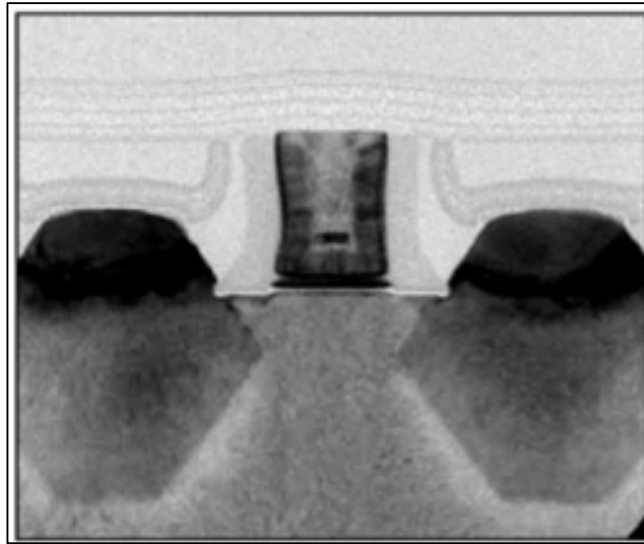
243. In my opinion, Akasaka in combination with Hsu823 renders obvious the Challenged Claims of the ’686 patent (Ground II).

1. A POSITA would have found it obvious to implement SiGe stressors in the source/drain regions of Akasaka’s pFET

244. In my opinion, a POSITA would have been motivated to combine Akasaka and Hsu823, thereby rendering claim 25 obvious. By the time the application for the ’686 patent was filed, SiGe stressors had already been known and used in three generations of high-volume commercial transistors. *See* Ex.1523, 1790-91 (describing Intel’s 90nm devices); Ex.1532, 657-58 (describing Intel’s 65nm devices); Ex.1516, 247-48 (describing Intel’s 45nm devices); Ex.1517 (same).

245. The most recent generation prior to the filing date of the ’686 patent, shown publicly in images like the one below before the application for the ’686 patent, not only used SiGe stressors but also high-K gate dielectrics and metal gates in an

RMG process. *See generally* Ex.1516; Ex.1517, 14-19. By the time the application for the '686 patent was filed, such SiGe stressors were standard industry practice. *See* Section V.F above.

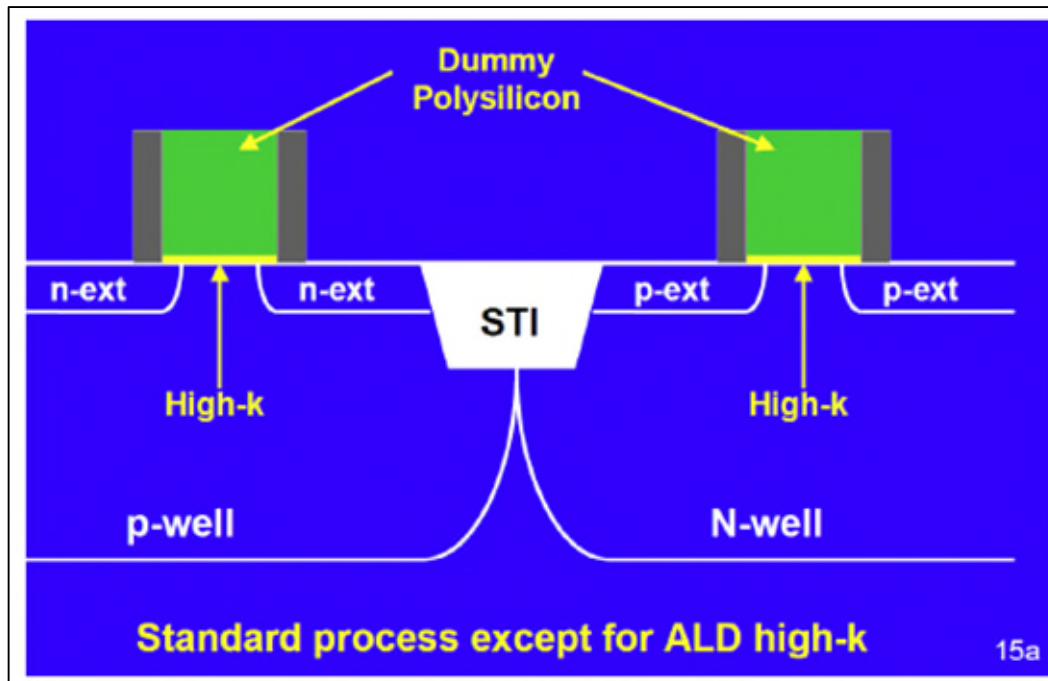


Ex.1516, Fig. 6

246. Although Akasaka may not expressly describe using SiGe stressors, it would have been obvious to use SiGe stressors in at least Akasaka's FIG. 26 transistor design, as the micrograph above—showing Intel's high-volume 45nm generation of devices that had been in production since 2007—make clear. Ex.1516, Fig. 6; *see also* Ex.1517, 16.

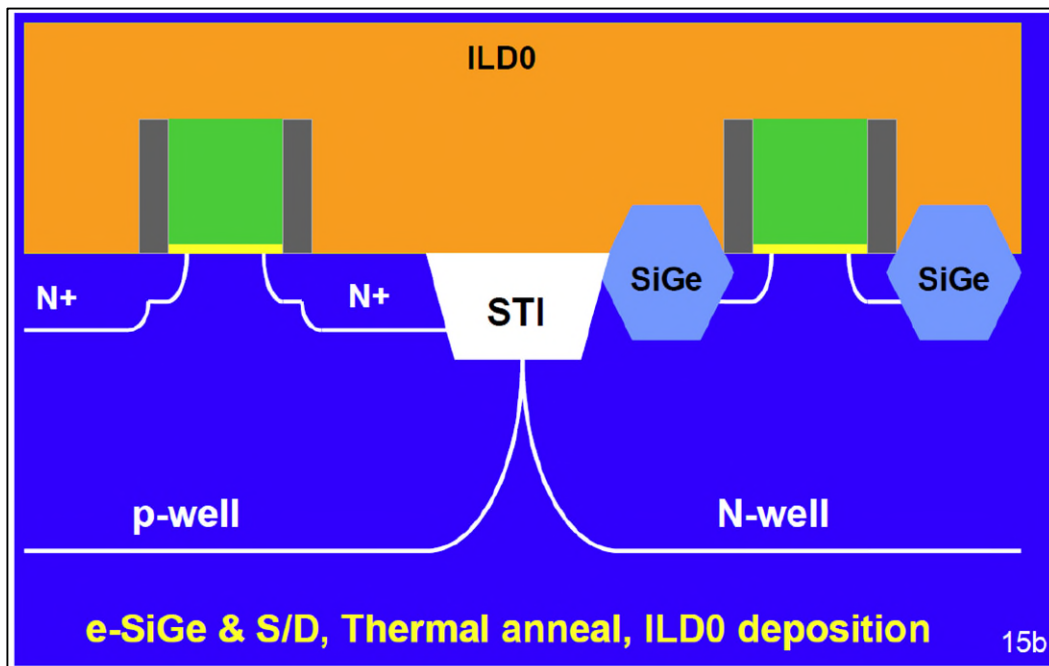
247. At the December 2007 IEDM in Washington, D.C., Kaizad Mistry of Intel described Intel's 45 nm process flow, which was a high-k/RMG process. *See generally* Ex.1517, 14-19 (in-person IEDM presentation); Ex.1516 (publication of related IEDM paper). To begin, nFET and pFET dummy gate structures are formed.

The dummy gates comprise high-k dielectrics (yellow) and dummy polysilicon gate electrodes (green). Ex.1517, 15a (below).



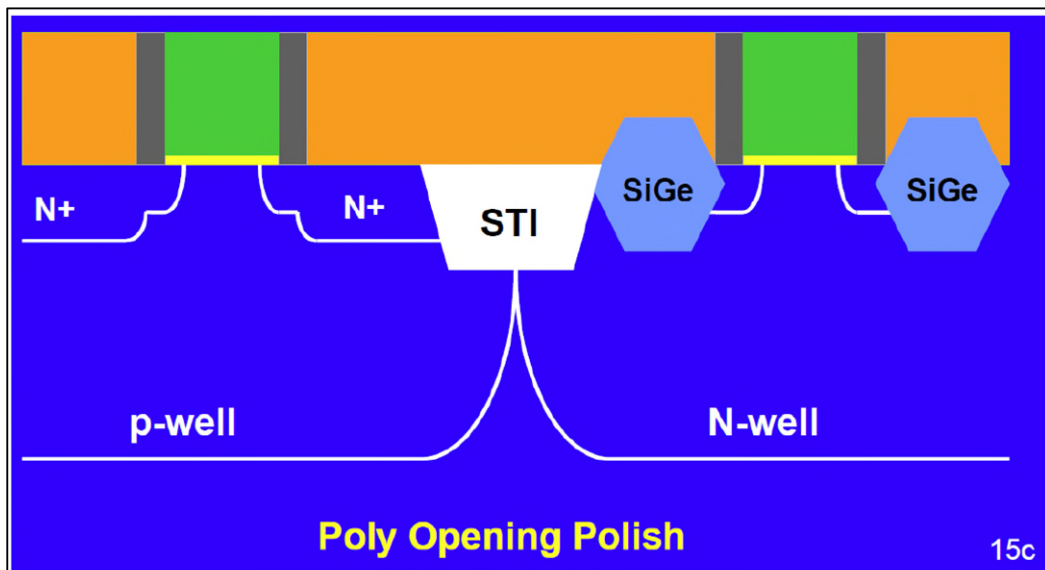
Ex.1517, 15a

248. Next, the source/drain regions are formed, including the formation of embedded epitaxial SiGe source/drain regions for the pFET (light blue hexagons). See Section V.F above. This is followed by thermal annealing to activate implanted dopants and then by a blanket deposition of interlayer dielectric ILD0 (orange), as shown below. Ex.1517, 15b (below).



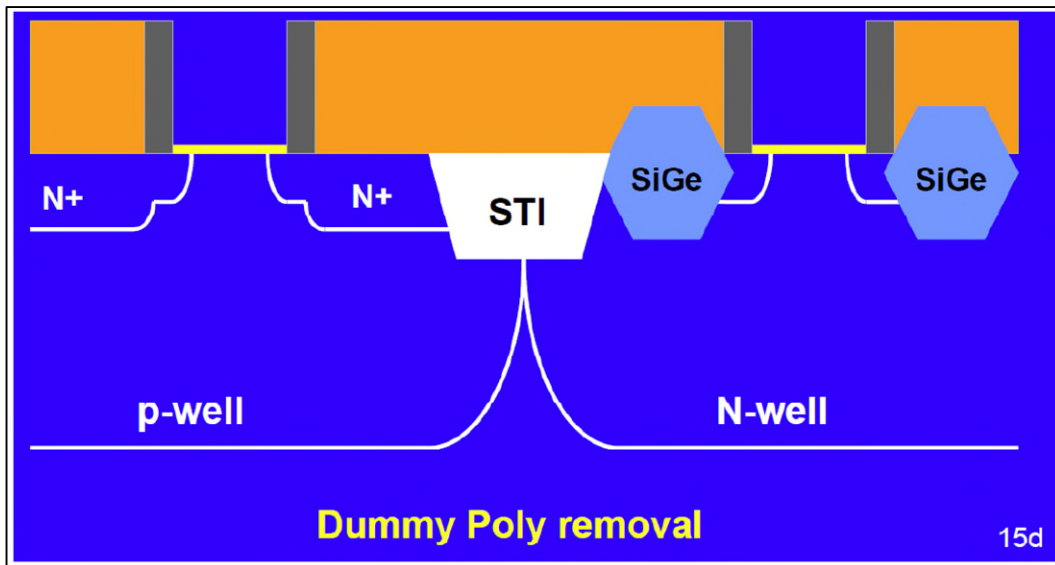
Ex.1517, 15b

249. Following this, a polishing step is performed to planarize interlayer dielectric ILD0 (orange) such that its top surface aligns with the top surfaces of the dummy polysilicon gate electrodes (green). Ex.1517, 15c (below).



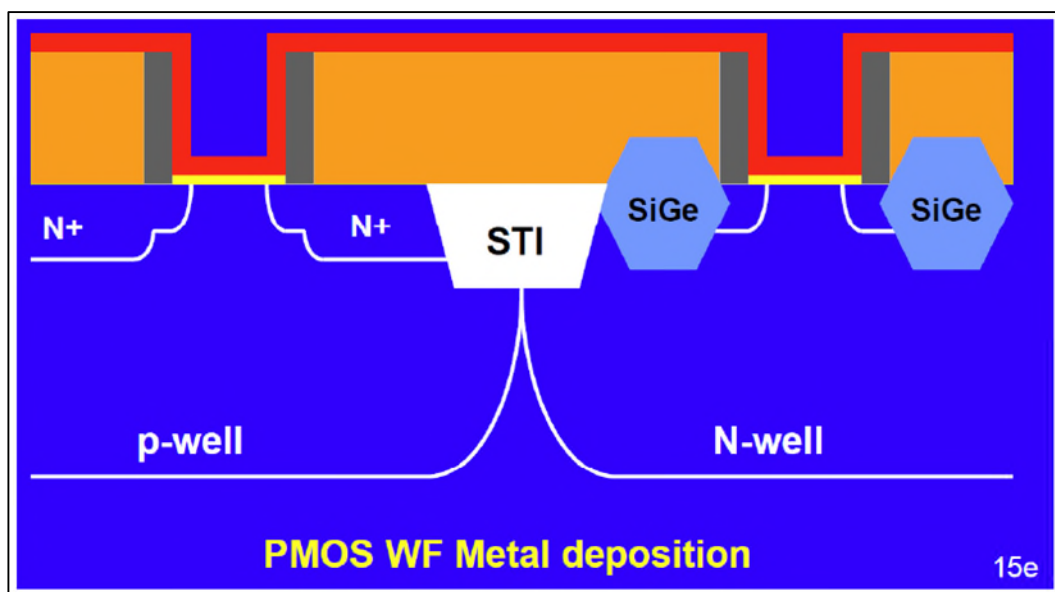
Ex.1517, 15c

250. Next, the dummy polysilicon gate electrodes (green) are removed by etching. Ex.1517, 15d (below).



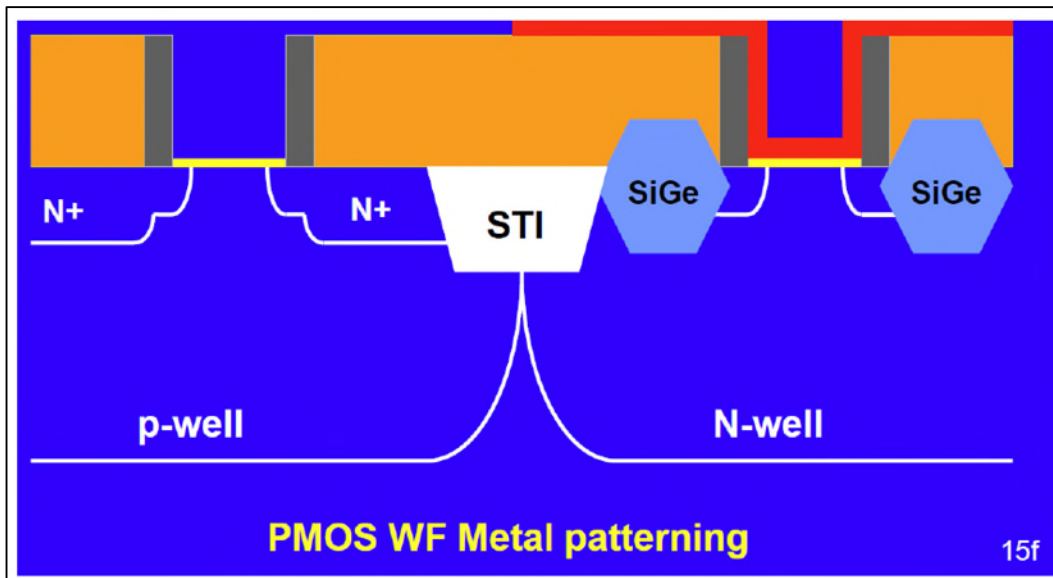
Ex.1517, 15d

251. The pFET work-function metal (red) is then deposited over the wafer, including in the void left by removing the dummy polysilicon gate electrodes. Ex.1517, 15e (below).



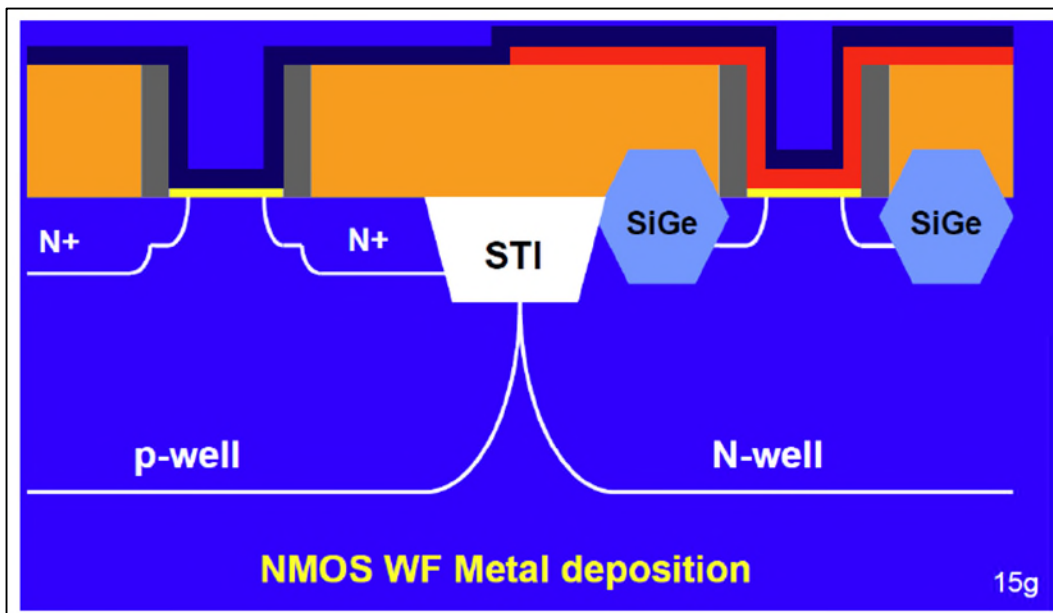
Ex.1517, 15e

252. Because this is the pFET work-function metal, it is removed from the wafer by etching everywhere except in the pFET regions. Ex.1517, 15f (below).



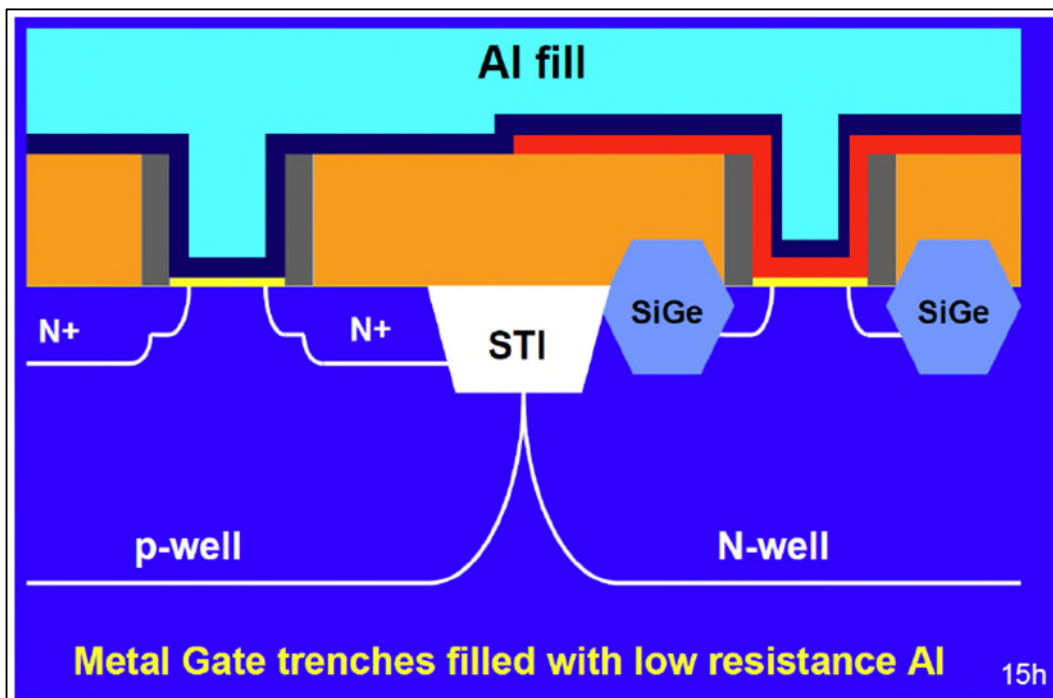
Ex.1517, 15f

253. Next, the nFET work-function metal (dark blue) is deposited over the wafer, including in the voids left by removing the dummy polysilicon gate electrodes. Ex.1517, 15g (below).



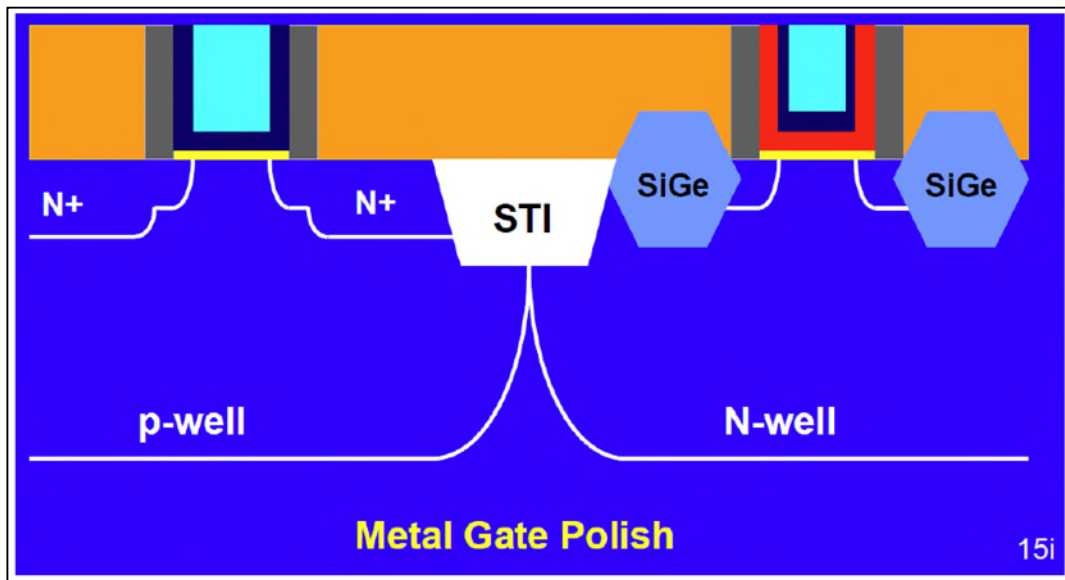
Ex.1517, 15g

254. Then, an aluminum filler (turquoise) is deposited over the entire wafer to fill the remaining voids left in the nFET and pFET gate electrode regions. Ex.1517, 15h (below).

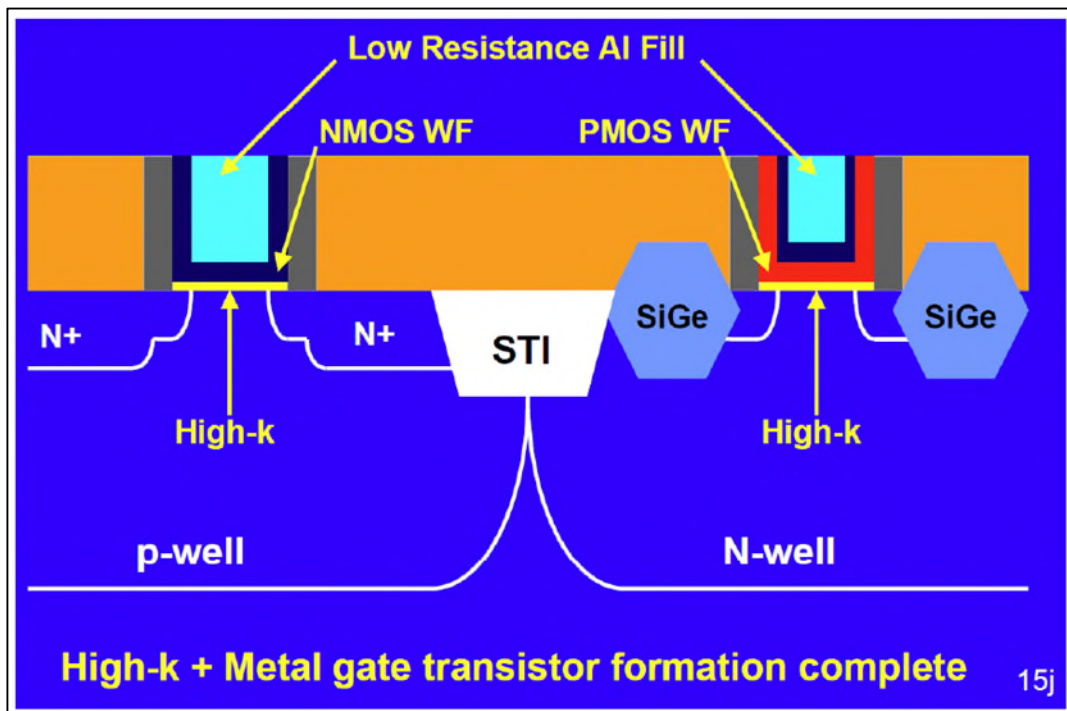


Ex.1517, 15h

255. A second polishing step is done to planarize the metal films such that the top surfaces of the replacement metal gate electrodes are aligned with the top surface of interlayer dielectric film ILD0 (orange). Ex.1517, 15i (below, top), 15j (below, bottom).



Ex.1517, 15i

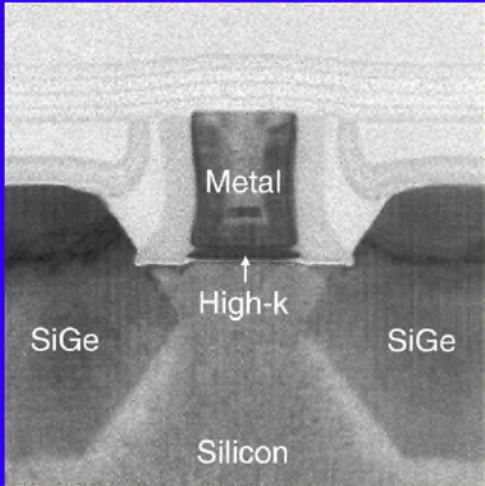


Ex.1517, 15j (same as 15i but with additional labels)

256. The final structure made using Intel's 45 nm high- κ /RMG process appears below. Ex.1517, 16, 19.

Transistor Features

- 35 nm min. gate length
- 160 nm contacted gate pitch
- 1.0 nm EOT Hi-K
- Dual workfunction metal gate electrodes
- 3RD generation of strained silicon

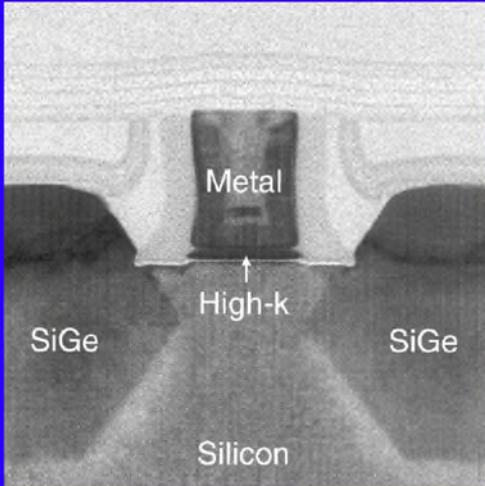


Micrograph showing a pFET transistor structure. The central gate stack is labeled "Metal" and "High-k". The gate electrodes on either side are labeled "SiGe". The substrate is labeled "Silicon".

16

Ex.1517, 16 (micrograph showing a pFET)

3RD Generation Strained Silicon



Micrograph showing a pFET transistor structure. The central gate stack is labeled "Metal" and "High-k". The gate electrodes on either side are labeled "SiGe". The substrate is labeled "Silicon".

- Increased Ge fraction
 - 90 nm: 17% Ge
 - 65 nm: 23% Ge
 - 45 nm: 30% Ge
- SiGe closer to channel

Ex.1517, 19 (micrograph showing a pFET)

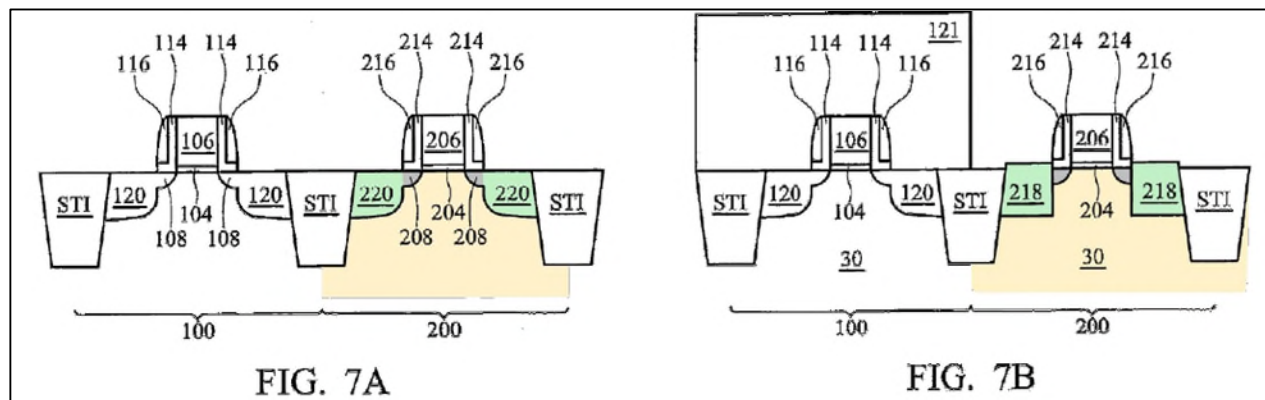
257. As the above presentation demonstrates, epitaxial SiGe had been fully integrated with high-k/RMG technology in Intel's high-volume commercial 45nm products, which was therefore common knowledge in the industry well before the application for the '686 patent was filed. *See generally* Ex.1516; Ex.1517. Given the similarity between Intel's 45 nm process above and the process used to make Akasaka's second embodiment semiconductor device (*see* Ex.1008, ¶¶72-88, FIGS. 15-26), a POSITA would have found it obvious to integrate epitaxial SiGe into Akasaka's second embodiment in my opinion.

258. Although the commercial adoption of SiGe stressors by Intel demonstrates both motivation to use such technology and a reasonable expectation of success for a POSITA, other literature confirms such motivation and expectation. For example, as an alternative to forming pFET source/drain regions solely by ion implantation, Hsu823 teaches forming SiGe stressors 218 in trenches of pFET active regions to induce compressive stress in the pFET channel region. Hsu823 explains that, in one embodiment, "source/drain regions 120 and 220 are formed [only] by implanting impurities into semiconductor substrate 30." Ex.1006, ¶32. As an alternative, Hsu823 teaches that SiGe stressors may be used:

In alternative embodiments, as shown in FIG. 7B, SiGe stressors 218 are formed in PMOS region 200. Preferably, a photo resist 121 is formed covering NMOS region 100. Recesses are formed in substrate 30 along the outside edges of the spacers 216, preferably by etching. SiGe

stressors 218 are then formed in the recesses. In the preferred embodiment, SiGe stressors 218 are epitaxially grown. P-type impurities such as boron are preferably doped during the epitaxial growth. The photo resist 121 is then removed. After being annealed, SiGe stressors 218 will try to restore their lattice spacing, which is greater than the lattice spacing of the substrate 30. This introduces compressive stresses in the respective channel regions of the resulting PMOS devices, and the device drive currents of the respective PMOS devices are increased.

Id., ¶33. Hsu823's FIGS. 7A (below, left) and 7B (below, right) illustrate usage of SiGe stressors.



Ex.1006, FIGS. 7A-7B (annotated)

259. In my opinion, a POSITA would have found it obvious to modify the pFET in Akasaka's FIG. 26, second embodiment semiconductor device by using epitaxial SiGe stressors, as taught by Hsu823 (and as Intel's public disclosures confirm), to form Akasaka's pFET source/drain regions 309.

260. A POSITA would have been motivated to do so in my opinion because SiGe stressors were known to increase hole mobility, thereby boosting drive current

and operating speed. *See* Section V.F above. As Hsu823 explains, SiGe stressors “introduce[] compressive stress[] in the . . . channel region[]” such that the “device drive current[] of the . . . PMOS device[] [is] increased.” Ex.1006, ¶33. Again, this was already standard industry practice when the application for the ’686 patent was filed, as Hsu823 further confirms:

Among efforts made to enhance carrier mobility, forming a stressed channel region is a known practice. The performance of a MOS device can be enhanced through a stressed-surface channel. This technique allows performance to be improved at a constant gate length without adding complexity to circuit fabrication or design. Research has revealed that . . . a compressive stress parallel to the channel length direction can improve PMOS device performance.

Id., ¶¶2-3.

261. It is also my opinion that a POSITA would have reasonably expected to succeed in implementing Hsu823’s SiGe stressors in Akasaka’s FIG. 26, second embodiment semiconductor device because such SiGe crystal layers were known and widely used to induce compressive stress in pFETs. *See* Section V.F above. The structure in Akasaka’s FIG. 16 is materially the same as the structure in Hsu823’s FIG. 7A. *Compare* Ex.1008, ¶¶72-73, FIG. 16, *with* Ex.1006, ¶¶28-32, FIG. 7A.

262. As I explain above, Hsu823 teaches (and the Intel disclosures confirm) that SiGe source/drain regions may be readily integrated into such a structure to boost PMOS performance. Ex.1006, ¶33; *see also* Ex.1517, 14-19. Thus, as Figure C (below, left) shows, a POSITA would have known the same process steps Hsu823 describes regarding FIG. 7B (below, right) readily integrate into Akasaka's process at FIG. 16 with the ordinary and expected result (i.e., SiGe stressors to boost pFET performance). Ex.1006, ¶33; *see also* Section V.F above.

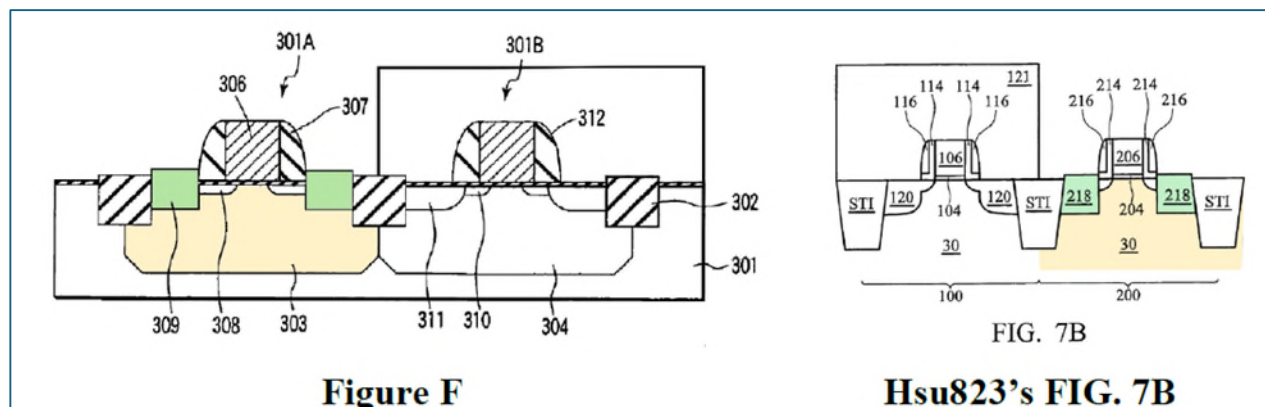


Figure C
(Ex.1008, FIG. 16, modified & annotated)

Hsu823's FIG. 7B
Ex.1006, FIG. 7B
(annotated)

263. Figure D below illustrates an exemplary modification of Akasaka's semiconductor device that includes SiGe stressors like the ones Hsu823 discloses. Ex.1006, ¶33, FIG. 7B; Ex.1008, FIG. 26; Ex.1538, 6:27-31, FIGS. 3-10 (illustrating a similar implementation of SiGe stressors in an RMG device); Ex.1516, Fig. 6 (same).

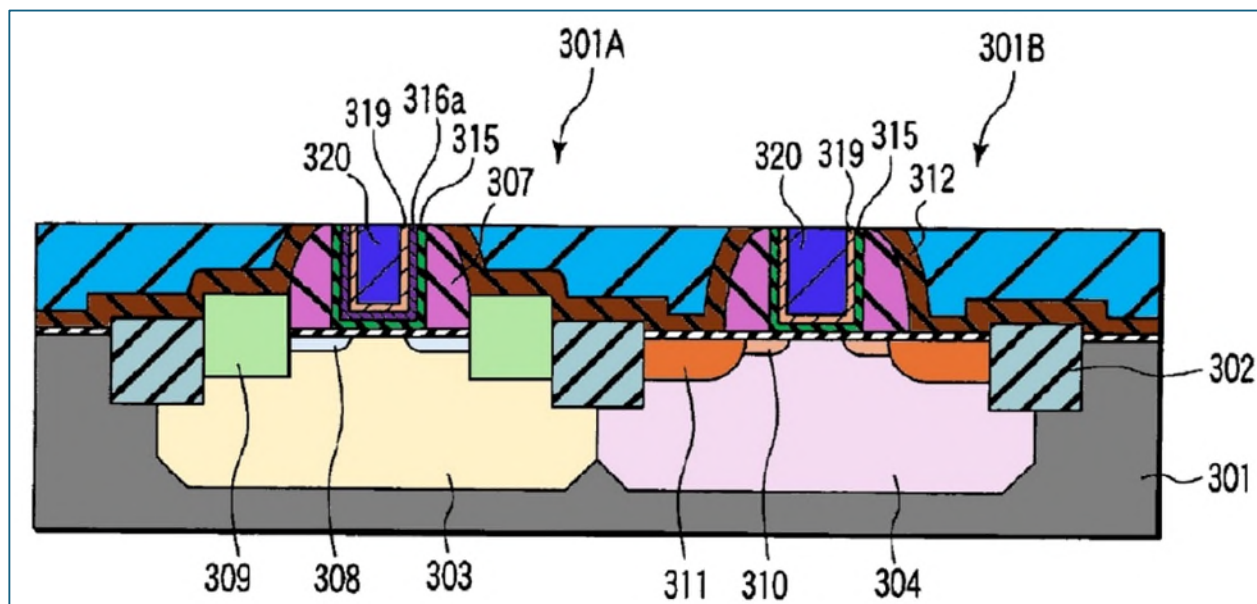
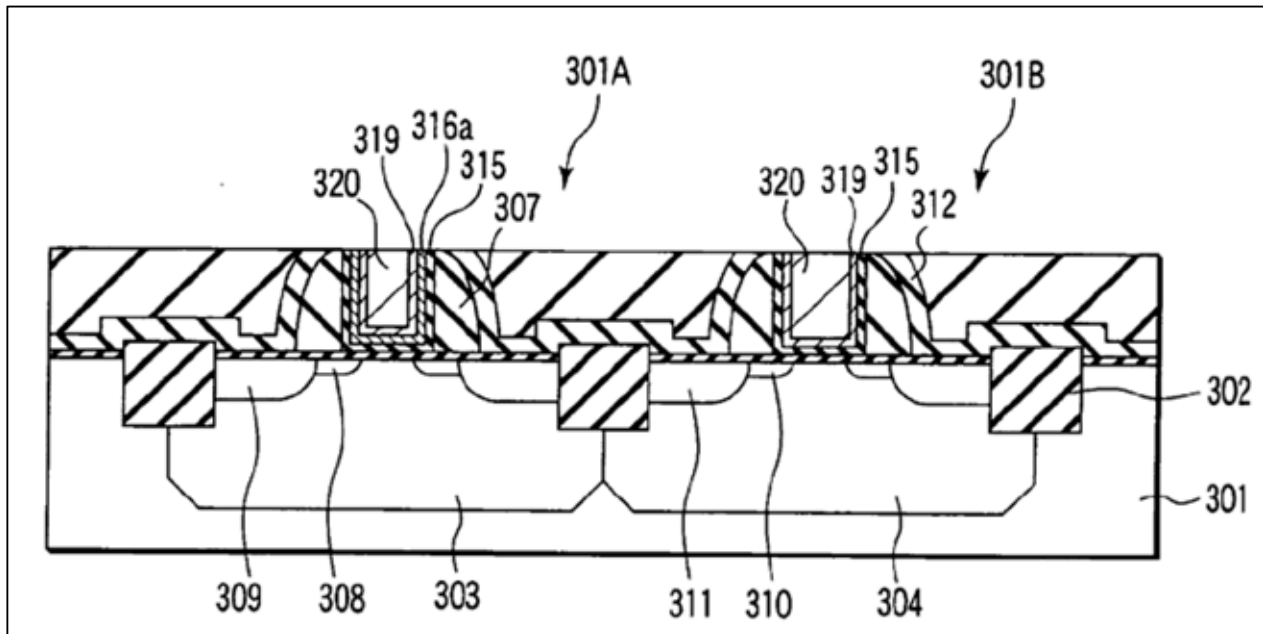


Figure D (Ex.1008, FIG. 26, modified and annotated)

2. Independent Claim 25

a. Preamble: “A semiconductor device comprising:”

264. Akasaka explains that “[t]he present invention relates to a method for manufacturing a semiconductor device, particularly an FET (Field Effect Transistor) of the MIS (Metal Insulator Semiconductor) type” Ex.1008, ¶3. Akasaka’s FIG. 26 and corresponding descriptions describe a “semiconductor device” that includes a “p-type MISFET . . . formed in . . . area 301A” and an “n-type MISFET . . . formed in . . . area 301B.” *Id.*, ¶73; *see also id.*, ¶72 (“FIGS. 15 to 26 are sectional views showing . . . a semiconductor device . . .”), FIG. 26 (below).

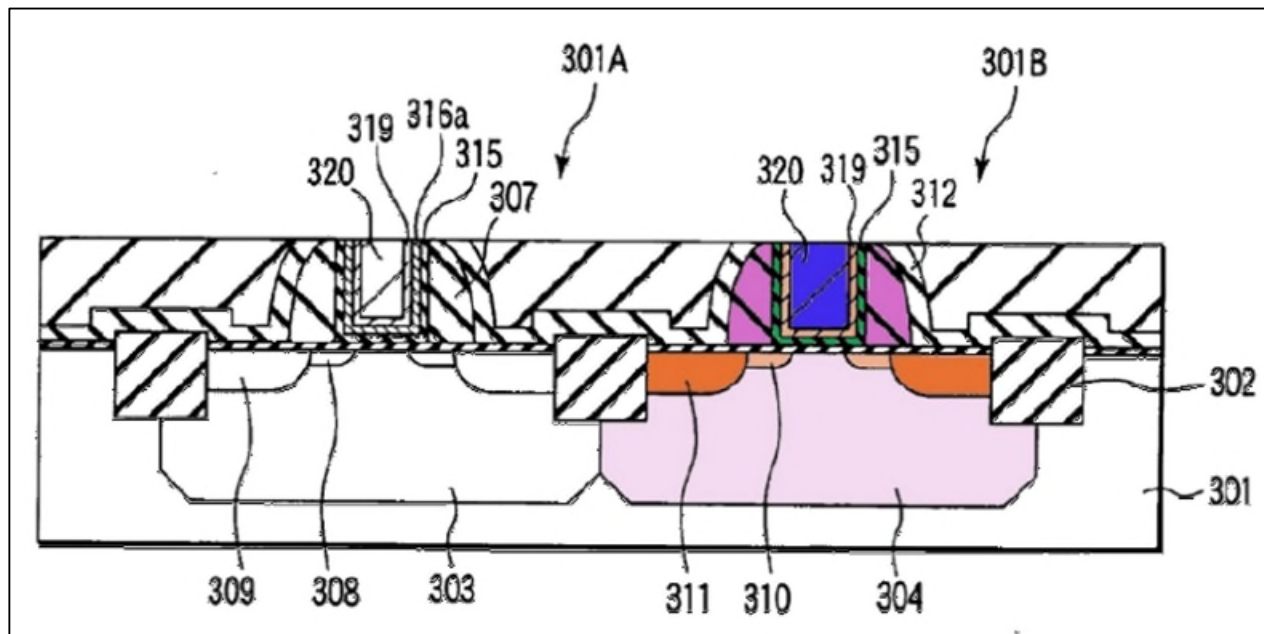


Ex.1008, FIG. 26

265. Therefore, it is my opinion that Akasaka combined with Hsu823 discloses this limitation of claim 25 of the '686 patent.

b. Limitation 25[a]: “a first MIS transistor”

266. As FIG. 26 (below) shows, Akasaka’s semiconductor device includes an “n-type MISFET . . . formed in . . . area 301B.” Ex.1008, ¶73; *see also id.*, ¶72.

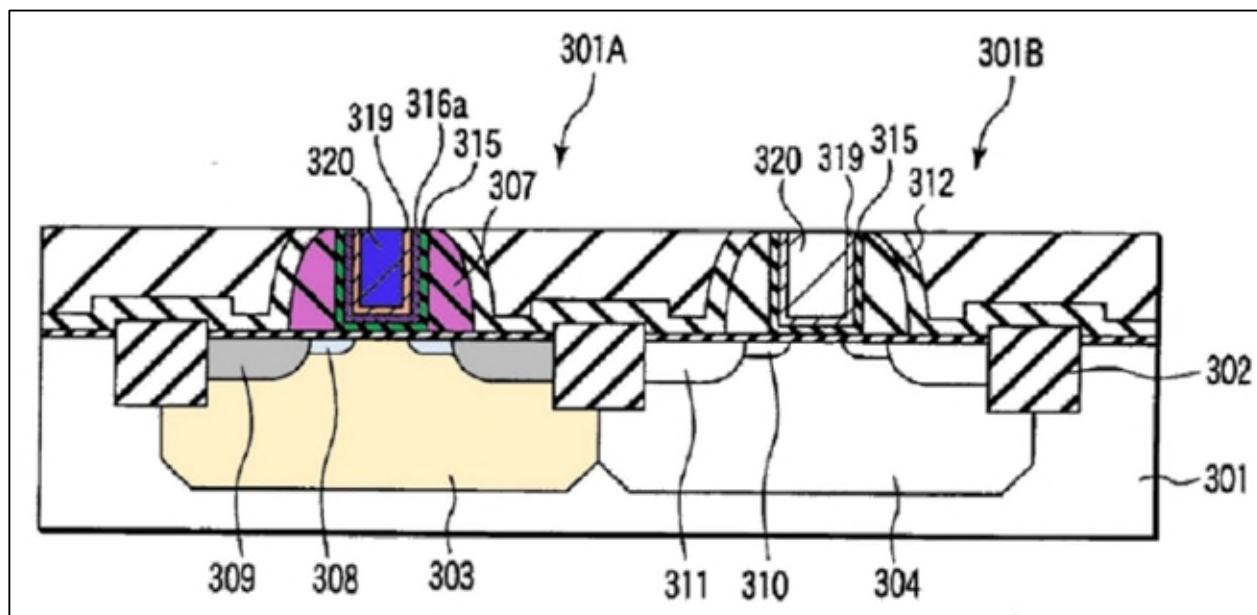


Ex.1008, FIG. 26 (annotated)

267. Therefore, it is my opinion that Akasaka combined with Hsu823 discloses this limitation of claim 25 of the '686 patent.

c. Limitation 25[b]: “a second MIS transistor”

268. As FIG. 26 (below) shows, Akasaka’s semiconductor device includes a “p-type MISFET . . . formed in . . . area 301A.” Ex.1008, ¶73; *see also id.*, ¶72.



Ex.1008, FIG. 26 (annotated)

269. Therefore, it is my opinion that Akasaka combined with Hsu823 discloses this limitation of claim 25 of the '686 patent.

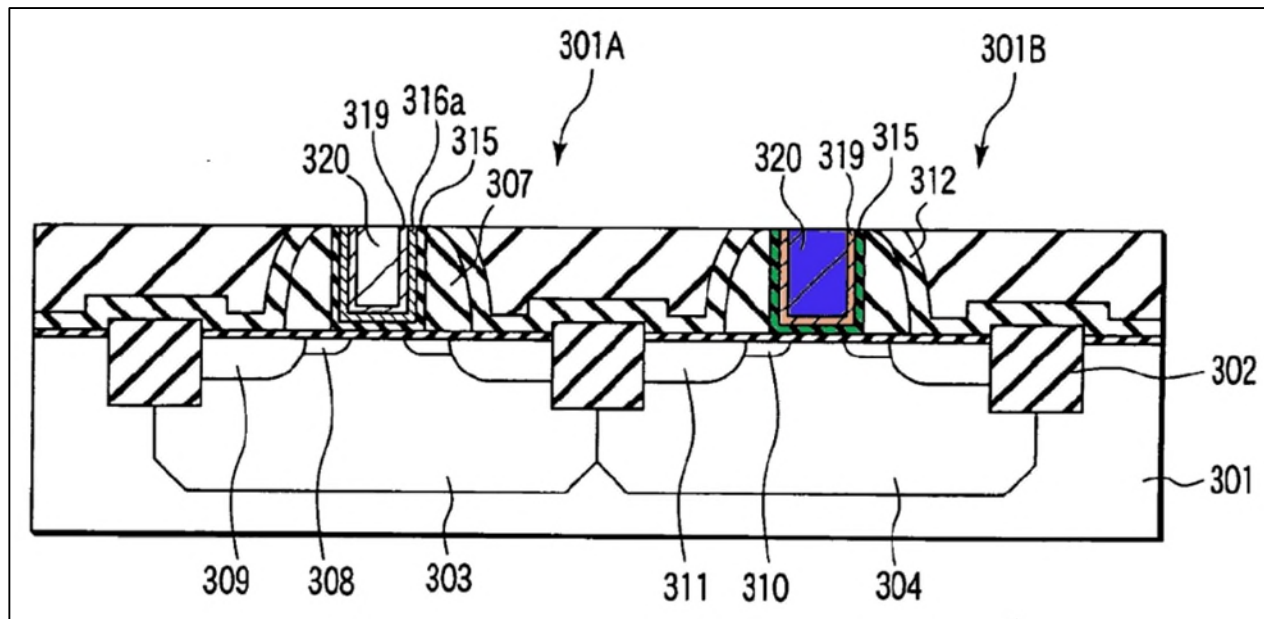
d. Limitation 25[c]: “the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate”

270. In the semiconductor device Akasaka’s FIG. 26 shows, the nFET in area 301B includes a “gate dielectric (insulating) film 315.” Ex.1008, ¶75, FIG. 26. Akasaka’s “gate dielectric film 315” is “depos[it]ed all over the substrate[301],” including area 301B, “for forming . . . an n-type MISFET,” as FIG. 26 shows. *Id.*, ¶¶72-73, 75, FIG. 26. In my opinion, a POSITA would have understood from these teachings of Akasaka that “gate dielectric film 315” is formed on a first active region in semiconductor substrate 301 (e.g., nFET area 301B).

271. Therefore, it is my opinion that Akasaka combined with Hsu823 discloses this limitation of claim 25 of the '686 patent.

e. Limitation 25[d]: “[the first MIS transistor includes: ...] a first gate electrode including a second metal film formed on the first gate insulating film”

272. As the semiconductor device in Akasaka’s FIG. 26 (below) shows, the nFET in area 301B has a gate electrode that includes conductive film 319 and conductive film 320. Ex.1008, ¶¶84-86, FIG. 26. Either or both conductive films 319/320 disclose the claimed “second metal film” in my opinion.



Ex.1008, FIG. 26 (annotated)

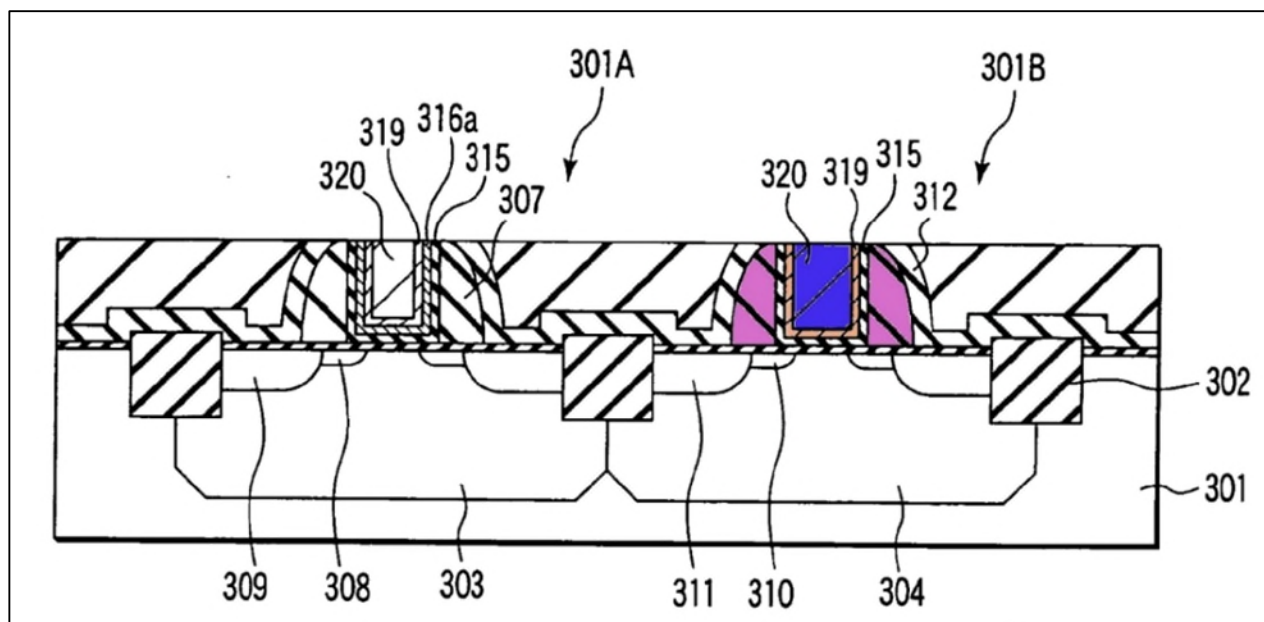
273. Conductive film 319 may be “a [Group-IVa, Group-Va, or Group-VIa] pure metal, . . . a metal silicide, a metal nitride, or another compound . . . , as long as it has a metallic band structure with a work function close to that of n+-polycrystalline silicon,” and conductive film 320 may be tungsten, which is also a metal. Ex.1008,

¶¶85-86. In one embodiment, “conductive film 319 and conductive film 320 are made of one integral film.” *Id.*, ¶86.

274. Therefore, it is my opinion that Akasaka combined with Hsu823 discloses this limitation of claim 25 of the '686 patent.

f. Limitation 25[e]: “[the first MIS transistor includes: ...] first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative”

275. As the semiconductor device Akasaka’s FIG. 26 (below) shows, the nFET in area 301B includes “[a] gate sidewall 307 formed of an insulating film, such as a silicon nitride film.” Ex.1008, ¶73, FIG. 26. As shown below, the gate sidewall 307 (pink) is formed on side surfaces of the gate electrode (conductive films 319/320) of the nFET.

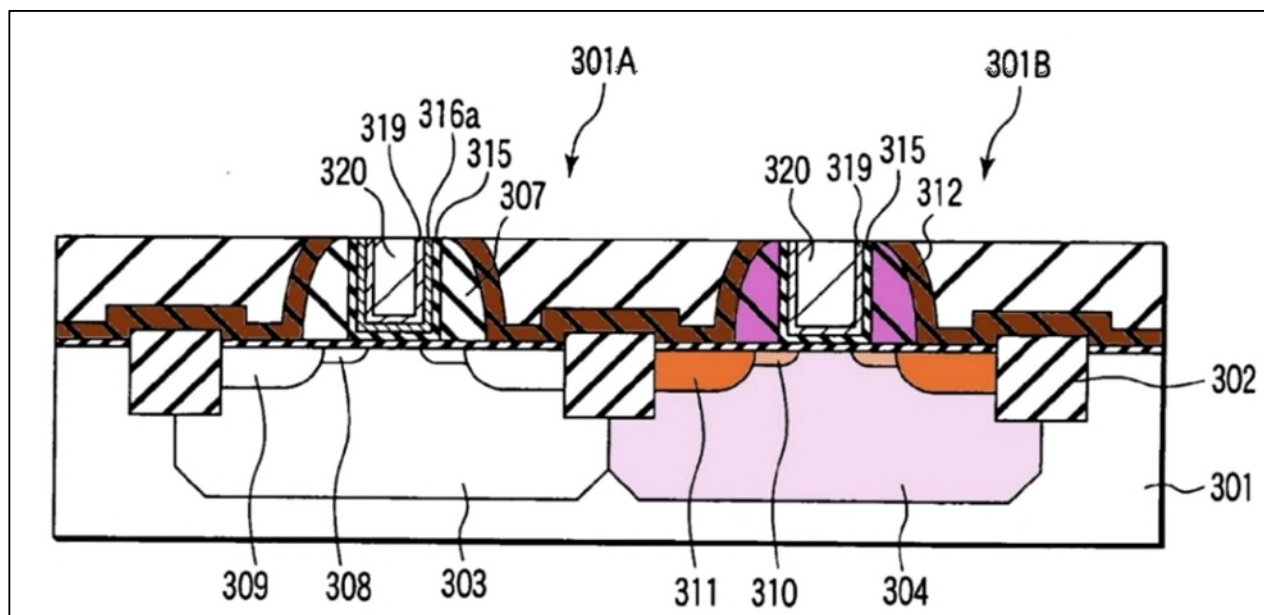


Ex.1008, FIG. 26 (annotated)

276. Therefore, it is my opinion that Akasaka combined with Hsu823 discloses this limitation of claim 25 of the '686 patent.

- g. **Limitation 25[f]: “[the first MIS transistor includes: ...] a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers”**

277. As the semiconductor device Akasaka’s FIG. 26 (below) shows, the nFET in area 301B includes a “silicon nitride film 312 serving as an etching stopper,” which therefore discloses the claimed “silicon nitride film.” Ex.1008, ¶73, FIG. 26.



Ex.1008, FIG. 26 (annotated)

278. As shown in FIG. 26 above, the gate electrode structure and its sidewalls 307 “are covered with a silicon nitride film 312,” such that Akasaka’s silicon nitride film 312 (brown) extends over the side surfaces of the nFET gate electrode (conductive

films 319/320) on which gate sidewalls 307 (purple) are formed. *See* Ex.1008, ¶73 (explaining that “gate sidewall[s] 307 are covered with a silicon nitride film 312”), FIGS. 16, 26. Then, a chemical-mechanical polishing (“CMP”) process is applied to silicon nitride film 312 to remove it from above the upper surfaces of the gate electrode structures. *See id.*, ¶¶74, 87.

279. As also shown above in FIG. 26, Akasaka’s silicon nitride film 312 (brown) extends over upper surfaces of area 301B (the first active region)—e.g., in p-type well region 304 and n-type source/drain layers 311—located laterally outside of gate sidewalls 307 (purple). In my opinion, a POSITA would have understood that gate sidewalls 307 are used to define the location of source/drain layers 311. *See, e.g.*, Ex.1006, ¶32 (“The respective spacers . . . are used as masks so that the edges of the source/drain regions . . . are substantially aligned with the respective spacers.”), FIG. 7A. As a result, the majority of source/drain layers 311 remain laterally outside of Akasaka’s gate sidewalls 307.

280. Therefore, it is my opinion that Akasaka combined with Hsu823 discloses this limitation of claim 25 of the ’686 patent.

h. Limitation 25[g]: “the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate”

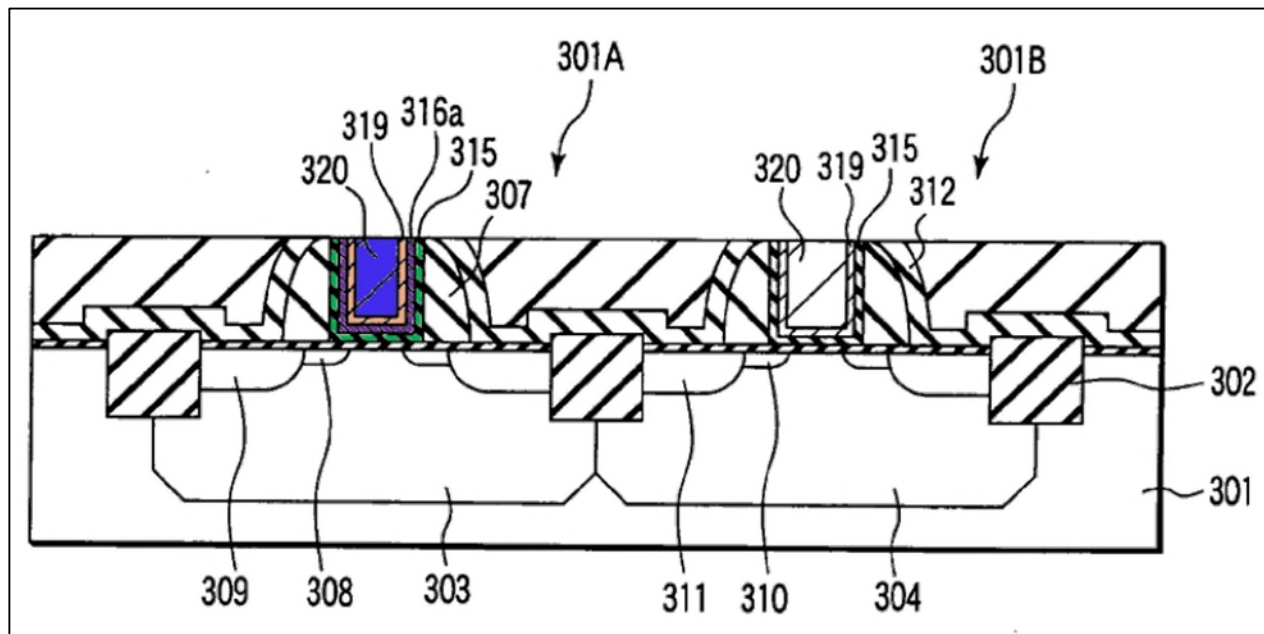
281. As the semiconductor device in Akasaka’s FIG. 26 shows, the pFET in area 301A includes a “gate dielectric (insulating) film 315.” Ex.1008, ¶75. Akasaka’s

“gate dielectric film 315” is “depos[it]ed all over the substrate[301],” including area 301A, “for forming a p-type MISFET,” as FIG. 26 shows. *Id.*, ¶¶72-73, 75, FIG. 26. In my opinion, a POSITA would have understood from these teachings of Akasaka that “gate dielectric film 315” is formed on a second active region in semiconductor substrate 301 (e.g., area pFET area 301A).

282. Therefore, it is my opinion that Akasaka combined with Hsu⁸²³ discloses this limitation of claim 25 of the ’686 patent.

- i. **Limitation 25[h]: “[the second MIS transistor includes: ...] a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film”**

283. As the semiconductor device in Akasaka’s FIG. 26 (below) shows, the pFET in area 301A has a gate electrode that includes conductive films 316a, 319, and 320. Conductive film 316a discloses the claimed “first metal film,” and either or both of conductive films 319 and 320 disclose the claimed “conductive film.” Ex.1008, ¶¶76-77, 82, 86.



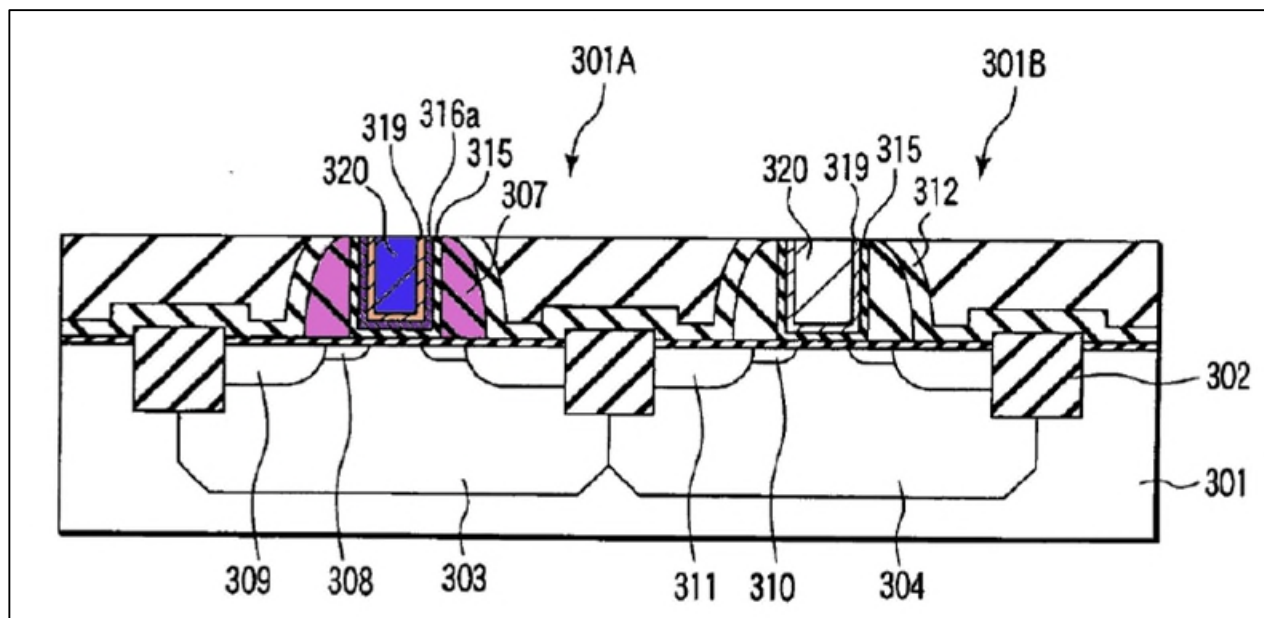
Ex.1008, FIG. 26 (annotated)

284. Conductive film 319 may be “a [Group-IVa, Group-Va, or Group-VIa] pure metal, . . . a metal silicide, a metal nitride, or another compound . . . , as long as it has a metallic band structure with a work function close to that of n⁺-polycrystalline silicon.” Ex.1008, ¶85. Akasaka also discloses that conductive film 320 may be tungsten, which is a metal, and “is preferably set to provide a sheet resistance of about 5Ω/□ or less.” *Id.*, ¶86. Additionally, in one embodiment, “conductive film 319 and conductive film 320 are made of one integral film.” *Id.*

285. Therefore, it is my opinion that Akasaka combined with Hsu823 discloses this limitation of claim 25 of the '686 patent.

- j. **Limitation 25[i]: “[the second MIS transistor includes: ...] second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative”**

286. As the semiconductor device in Akasaka’s FIG. 26 (below) shows, the pFET in area 301A includes “[a] gate sidewall 307 formed of an insulating film, such as a silicon nitride film.” Ex.1008, ¶73, FIG. 26. The gate sidewall 307 (purple) is formed on side surfaces of the gate electrode (conductive films 316a/319/320) of the pFET.

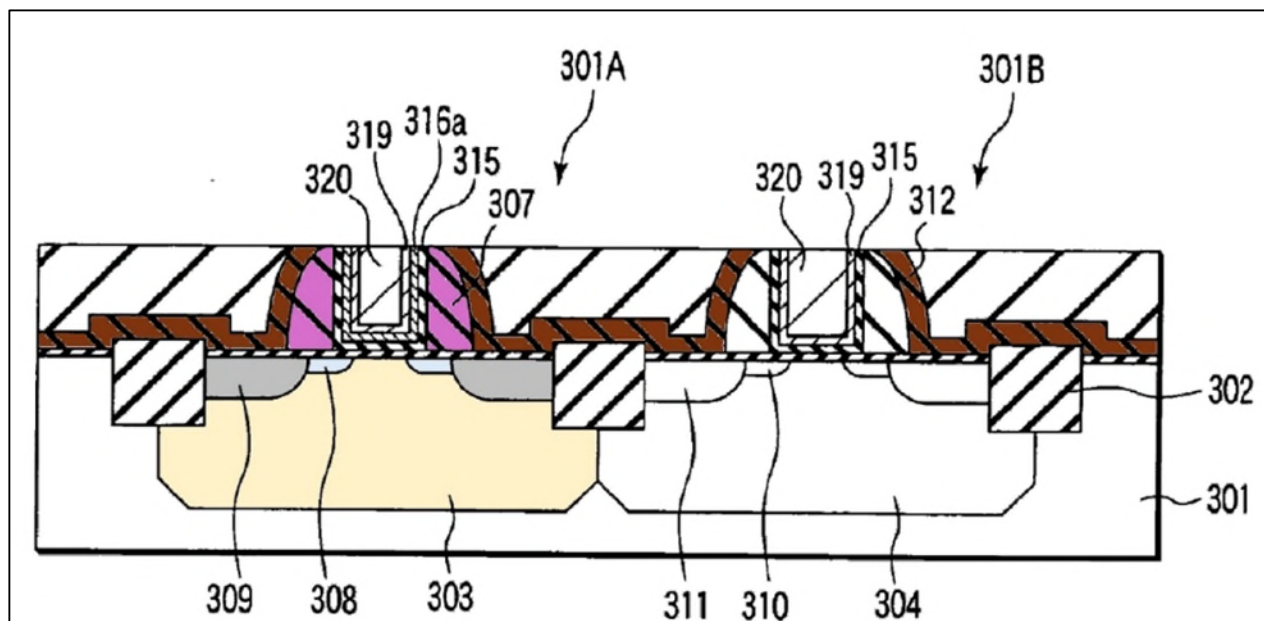


Ex.1008, FIG. 26 (annotated)

287. Therefore, it is my opinion that Akasaka combined with Hsu823 discloses this limitation of claim 25 of the '686 patent.

- k. **Limitation 25[j]: “[the second MIS transistor includes: ...] the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers”**

288. As the semiconductor device in Akasaka’s FIG. 26 (below) shows, the pFET in area 301A includes a “silicon nitride film 312 serving as an etching stopper,” which discloses the claimed “silicon nitride film.” Ex.1008, ¶73, FIG. 26.



Ex.1008, FIG. 26 (annotated)

289. As shown in FIG. 26 above, the gate electrode structure and its sidewalls 307 “are covered with silicon nitride film 312,” such that Akasaka’s silicon nitride film 312 (brown) extends over the side surfaces of the pFET gate electrode (conductive films 316a/319/320) on which gate sidewalls 307 (purple) are formed. See Ex.1008, ¶73 (explaining that “gate sidewall[s] 307 are covered with a silicon

nitride film 312”), FIGS. 16, 26. A chemical-mechanical polishing (“CMP”) process is applied to silicon nitride film 312 to remove it from above the upper surfaces of the gate electrode structures. *See id.*, ¶¶74, 87.

290. As also shown in FIG. 26 above, Akasaka’s silicon nitride film 312 (brown) extends over upper surfaces of area 301A (the second active region)—e.g., in n-type well region 303 and p-type source/drain layers 309—located laterally outside of gate sidewalls 307 (purple).

291. Therefore, it is my opinion that Akasaka combined with Hsu823 discloses this limitation of claim 25 of the ’686 patent.

I. Limitation 25[k]: “the first and second metal films are made of different metal materials”

292. As I explain above, either or both of conductive film 319 and/or conductive film 320 disclose the claimed “second metal film.” Conductive film 319 may be “a [Group-IVa, Group-Va, or Group-VIa] pure metal, . . . a metal silicide, a metal nitride, or another compound . . . , as long as it has a metallic band structure with a work function close to that of n⁺-poly-crystalline silicon,” and conductive film 320 may be tungsten, which is also a metal. Ex.1008, ¶¶85-86.

293. As I also explain above, conductive film 316a discloses the claimed “first metal film.” Conductive film 316a may be “a [Group-VIII] pure metal, . . . a metal silicide, a metal nitride, or another compound . . . as long as it has a metallic

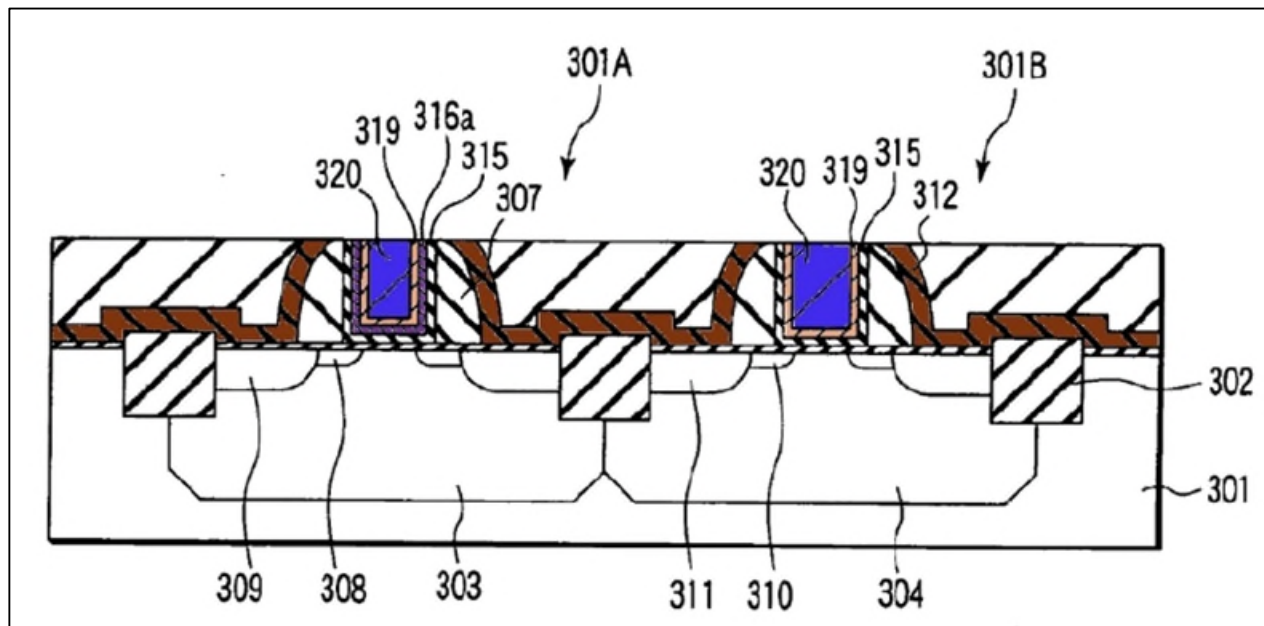
band structure with a work function close to that of p⁺-poly-crystalline silicon.”
Ex.1008, ¶77.

294. Accordingly, conductive film 316a and conductive films 319/320 are made of different metal materials chosen from different elements of the periodic table to have different metallic band structures. Ex.1008, ¶¶77, 85-86.

295. Therefore, it is my opinion that Akasaka combined with Hsu823 discloses this limitation of claim 25 of the '686 patent.

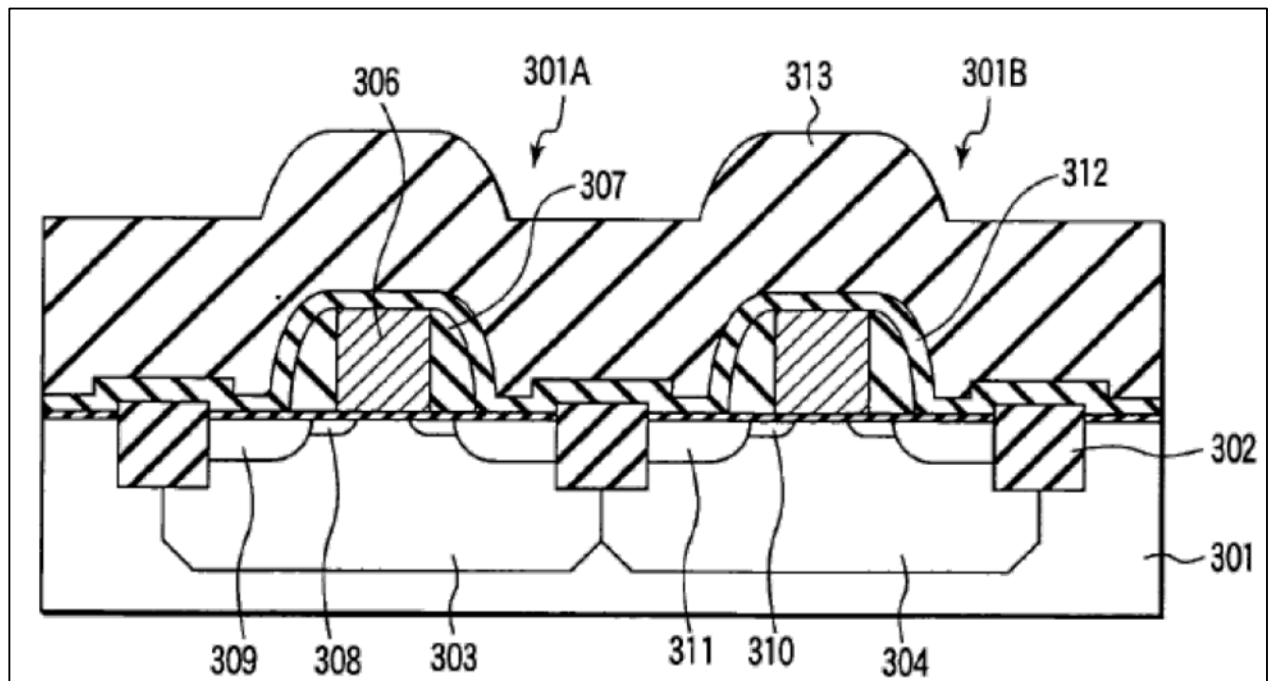
m. Limitation 25[l]: “the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes”

296. As the semiconductor device in Akasaka’s FIG. 26 (below) shows, silicon nitride film 312 is not formed on any upper surfaces of the nFET and pFET gate electrodes.



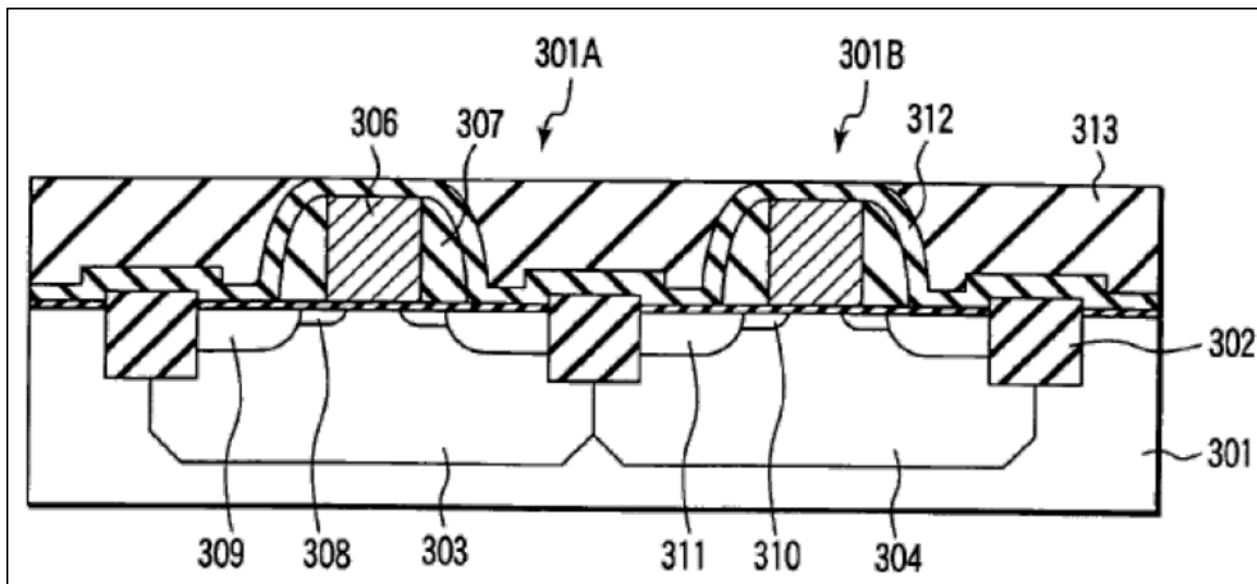
Ex.1008, FIG. 26 (annotated)

297. In my opinion, a POSITA would have understood that the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes from the manufacturing process disclosed by Akasaka. As Akasaka's FIGS. 16-18 illustrate, dummy gate electrodes 306 are formed where the nFET and pFET gate electrodes will be located. Ex.1008, ¶73. As FIG. 16 (below) shows, silicon nitride film 312 and inter-level insulating film 313 are formed over dummy gate electrodes 306. *Id.*, ¶73, FIG. 16.



Ex.1008, FIG. 16 (annotated)

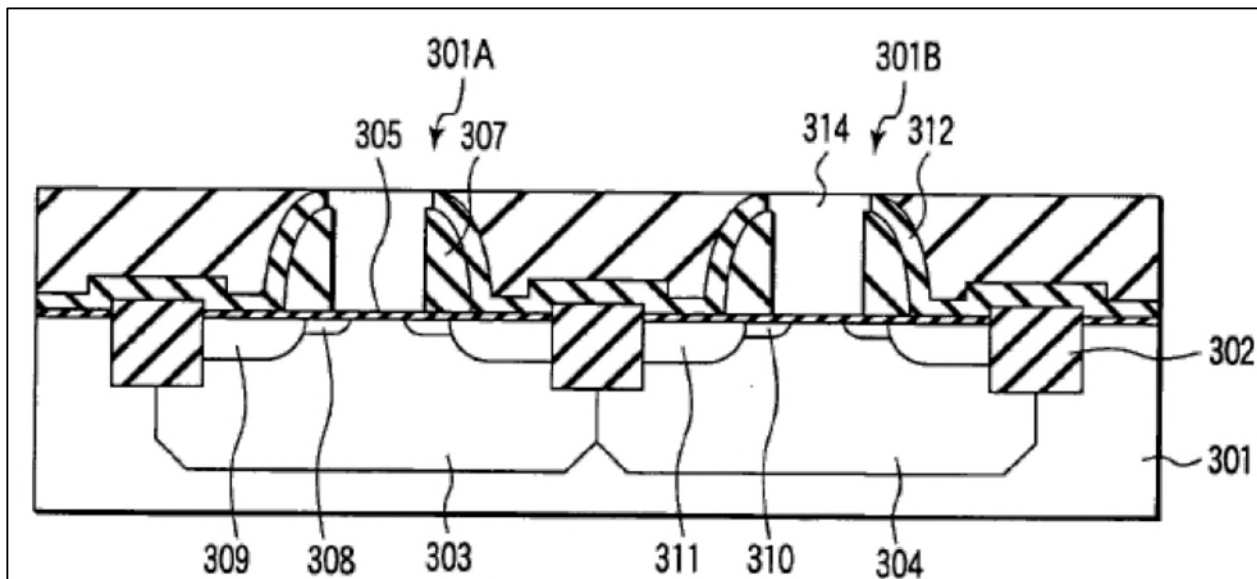
298. As illustrated in FIG. 17 (below), the inter-level insulating film is “polished from above by a CMP (Chemical Mechanical Polishing) method . . . to expose . . . the upper surface of the silicon nitride film 312 deposited on the dummy gate electrode 306.” Ex.1008, ¶74, FIG. 17.



Ex.1008, FIG. 17 (annotated)

299. Then, as shown in FIG. 18 (below), “the exposed silicon nitride film 312 and the dummy gate electrodes are selectively removed to form recess portions 314.”

Ex.1008, ¶74, FIG. 18.



Ex.1008, FIG. 18 (annotated)

300. Thereafter, conductive layers 316a, 319, and 320 are deposited into recesses 314. Ex.1008, ¶¶75-76, 84-86, FIGS. 19, 25. After forming gate electrode layers 316a, 319, and 320 for the nFET and pFET, a second CMP step ensures that nothing—including silicon nitride film 312—remains on any upper surface of the gate electrodes. *See id.*, ¶87, FIG. 26. In my opinion, a POSITA would have understood this process prevents silicon nitride film 312 from being located on any upper surface of the first or second gate electrode.

301. Therefore, it is my opinion that Akasaka combined with Hsu823 discloses this limitation of claim 25 of the '686 patent.

n. Limitation 25[m]: “the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region”

302. As I explain above, Akasaka’s silicon nitride film 312 discloses the claimed “silicon nitride film.” In my opinion, a POSITA would have found it obvious to implement Akasaka’s silicon nitride film 312 as a tensile etch stop layer to “cause[] . . . stress in a gate length direction of a channel region in” Akasaka’s nFET first active region, as I explain in detail below.

303. Akasaka teaches that “silicon nitride film 312 serv[es] as an etching stopper.” Ex1.008, ¶73. Hsu823 discloses a similar CESL 34 made of silicon nitride and formed in a manner that causes tensile stress in a gate length direction of channel

region in the active region of the nFET device. Hsu823 explains why doing so would have been beneficial:

With circuits becoming smaller and faster, improvement in device driving current is becoming more important, which can be increased by improving carrier mobility. Among efforts made to enhance carrier mobility, forming a stressed channel region is a known practice. The performance of a MOS device can be enhanced through a stressed-surface channel. This technique allows performance to be improved at a constant gate length without adding complexity to circuit fabrication or design.

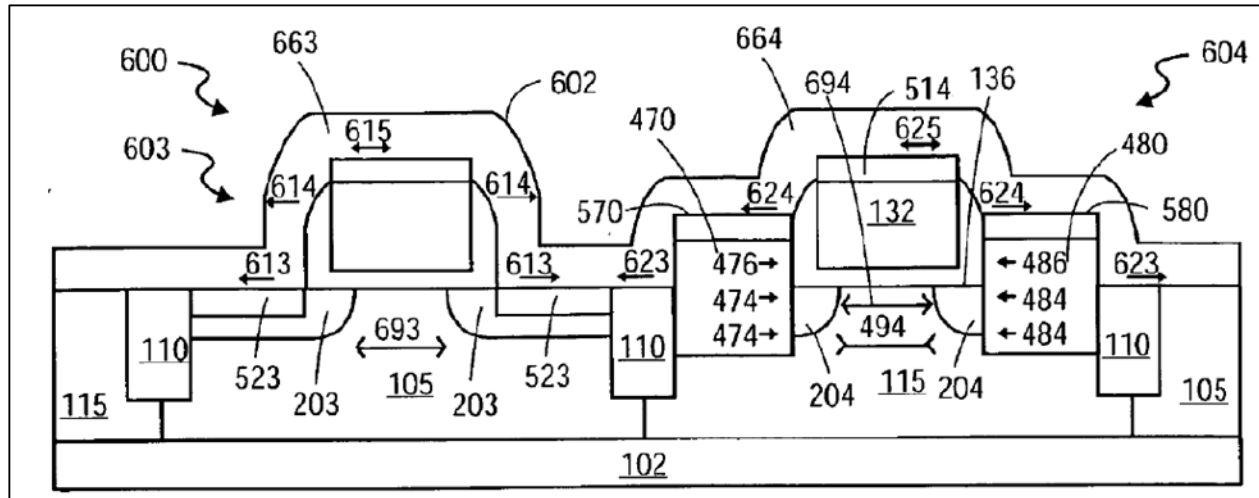
Research has revealed that a bi-axial, in-plane tensile stress field can improve NMOS performance, and a compressive stress parallel to the channel length direction can improve PMOS device performance. A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device. The stressed CESLs introduce stress into the channel region. Therefore, the carrier mobility is improved.

Ex.1006, ¶¶2-3; *see also* Ex.1031Ex.1531, ¶03 (“A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device. The stressed CESLs introduce stress into the channel region. Therefore, the carrier mobility is improved.”).

304. In my opinion, a POSITA would have been motivated to implement Akasaka’s silicon nitride film 312 as a tensile layer covering both pFET and nFET

devices, which was well-known in the art to improve electron mobility in the nFET channel regions. *See* Section V.F above. Morin, for instance, explains that “in low cost / low power CMOS flow approaches, it is important to work to improve nMOS transistors since other solutions . . . can enhance the pMOS performances. As a result, in these technologies, process induced stress engineering is dedicated to electron mobility enhancement, so by using tensile nitride as CESL.” Ex.1528, 356; *see also* Ex.1526, ¶5 (“For n-MOS devices, carrier mobility (i.e. electron mobility) is enhanced by generating a tensile strain in the transistor’s channel region.”); Ex.1006, ¶39 (teaching the option of applying a tensile CESL over both pFET and nFET devices because “the performance of PMOS devices can be easily improved . . . , while the performance of NMOS devices is relatively difficult to improve”); Ex.1530, 1-2 (“[T]he same tensile capping layer (stress: 1GPa; thickness: 700Å) was applied to both [the] USP and tensile-CESL process[es] Significant drive current enhancement of both N/PMOS is achieved with insertion of this USP in standard CMOS flow.”), Tbls. I-II, Figs. 1-7; Ex.1523, Fig. 5(c).

305. If SiGe source/drain stressors are present, as they optionally are in the semiconductor device of the Akasaka-Hsu823 combination, Bohr683 explains that a net compressive stress still obtains in the pFET channel region when a tensile CESL is formed over both pFET and nFET devices to apply tensile stress to the nFET channel region. For example, Bohr683’s FIG. 6 illustrates this below.



Ex.1527, FIG. 6

Ex.1527, ¶¶[0038]-[0039], FIG. 6 (above); *see also* Ex.1006, ¶39 (teaching the option of applying a tensile CESL over both pFET and nFET devices because “the performance of PMOS devices can be easily improved with SiGe stressors, while the performance of NMOS devices is relatively difficult to improve”); Ex.1528, 356 (“[I]t is important to work to improve nMOS transistors since other solutions . . . can enhance the pMOS performances. As a result, in these technologies, process induced stress engineering is dedicated to electron mobility enhancement, so by using tensile nitride as CESL.”); Ex.1530, 1-2 (“[T]he same tensile capping layer (stress: 1GPa; thickness: 700Å) was applied to both [the] USP and tensile-CESL process[es] Significant drive current enhancement of both N/PMOS is achieved with insertion of this USP in standard CMOS flow.”), Tbls. I-II, Figs. 1-7; Ex.1523, Fig. 5(c).

306. In my opinion, a POSITA would have reasonably expected to succeed at implementing Akasaka's silicon nitride film 312 as a tensile layer because such tensile CESLs were widely used to improve carrier mobility in nFETs. *See* Section V.F above. Moreover, it would have been well within a POSITA's ability to create a tensile silicon nitride CESL film. For example, Jung explains that "a stress-tuned silicon nitride film can be deposited . . . to provide an etch stop layer. . . , as well as to enhance channel mobility in various portions of the device structure." Ex.1529, ¶¶90. Jung also describes exemplary recipes for forming a tensile CESL for this purpose. *See id.*, ¶¶99-100 ("Table V shows the deposition conditions for silicon nitride films which were deposited under conditions which provided tensile stress films."), Tbl. V.

307. Accordingly, it is my opinion that a POSITA would have reasonably expected to succeed at implementing Akasaka's silicon nitride film 312 as a tensile layer, as such layers were ubiquitous in the industry by the time the application for the '686 patent was filed.

308. Therefore, it is my opinion that Akasaka combined with Hsu823 discloses this limitation of claim 25 of the '686 patent.

3. Dependent Claim 26: “The semiconductor device of claim 25, wherein the first metal film has a thickness smaller than that of the second metal film”

309. As I explain above, either or both of Akasaka’s conductive films 319 and 320 discloses the claimed “second metal film.” For purposes of claim 26, either conductive film 320 alone, or both conductive films 319 and 320 collectively, disclose the claimed “second metal film.” As I also explain above, Akasaka’s conductive film 316a discloses the claimed “first metal film.”

310. Akasaka discloses that conductive film 316a has a thickness “preferably set to be about 5 nm” or “a very small value of about 1 to 2 nm.” Ex.1008, ¶77. Akasaka discloses that conductive film 320 has a thickness of “about 40 to 50 nm.” *Id.*, ¶86. Thus, conductive film 316a (i.e., the claimed “first metal film”) has a thickness smaller than that of conductive film 320 alone or together with conductive film 319 (i.e., the claimed “second metal film”).

311. Therefore, it is my opinion that Akasaka combined with Hsu823 discloses claim 26 of the ’686 patent.

4. Dependent Claim 27: “The semiconductor device of claim 25, wherein the first and second metal films have different work functions”

312. As I explain above, either or both of conductive film 319 and conductive film 320 disclose the claimed “second metal film.” For purposes of claim 27, conductive film 319 alone discloses the claimed “second metal film.” As I also

explain above, Akasaka's conductive film 316a discloses the claimed "first metal film."

313. Akasaka discloses that conductive film 316a (i.e., the claimed "first metal film") "is preferably selected to have a work function close to that of p+-polycrystalline silicon, such as a work function of 4.8 to 5.3 eV." Ex1008, ¶77; *see also id.*, ¶76 ("[T]he type of the material of the conductive film 316 should be determined in consideration of its work function.").

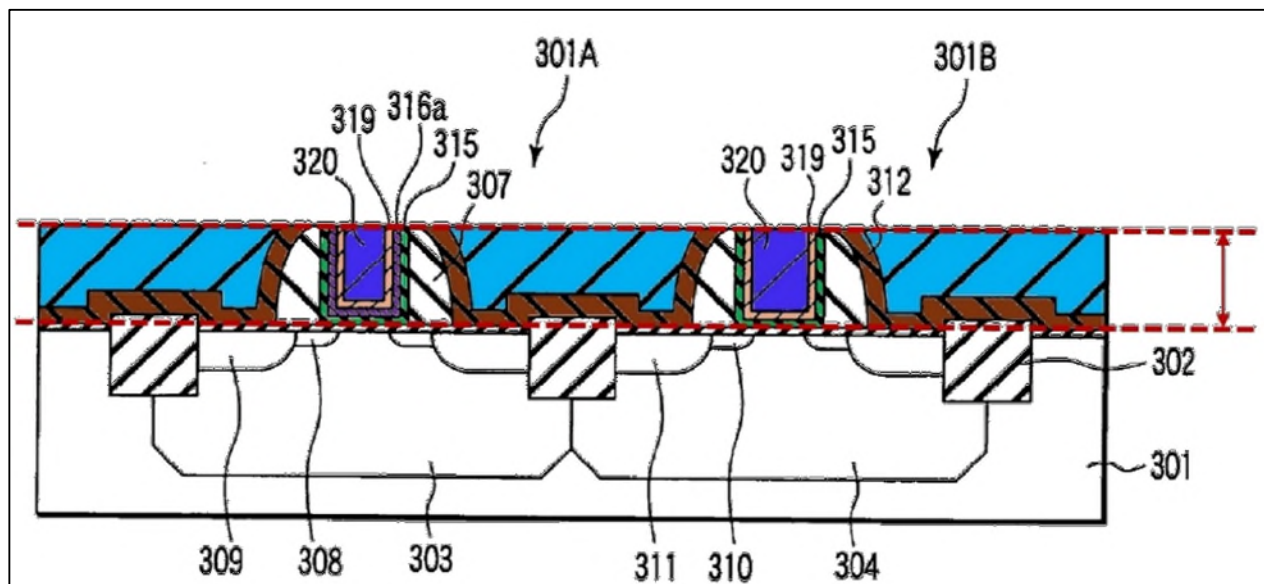
314. Akasaka also discloses that conductive film 319 (i.e., the claimed "second metal film") "is preferably selected to have a work function close to that of n+-polycrystalline silicon, such as a work function of 3.9 to 4.2 eV." Ex.1008, ¶85; *see also id.*, ¶84 ([T]he type of the material of the conductive film 319 should also be determined in consideration of its work function.").

315. Accordingly, conductive film 316a (i.e., the claimed "first metal film" with a work function of 4.8 to 5.3 eV) and conductive film 319 (i.e., the claimed "second metal film" with a work function of 3.9 to 4.2 eV) have different work functions.

316. Therefore, it is my opinion that Akasaka combined with Hsu823 discloses claim 27 of the '686 patent.

5. Dependent Claim 28: “The semiconductor device of claim 25, wherein the silicon nitride film has a thickness smaller than that of the first gate electrode”

317. As I explain above, Akasaka’s silicon nitride film 312 discloses the claimed “silicon nitride film,” and Akasaka’s conductive films 319 and 320 in nFET area 310B disclose the claimed “first gate electrode.” Akasaka discloses that silicon nitride film 312 has a smaller thickness than conductive films 319 and 320 in nFET area 301B because FIG. 26 (below) shows silicon nitride film 312 (brown) is much thinner than conductive films 319 and 320 (yellow and purple, respectively) in nFET area 301B, which is consistent with what a POSITA would have expected.



Ex.1008, FIG. 26 (annotated)

318. Thus, in my opinion, Akasaka teaches “the silicon nitride film has a thickness smaller than that of the first gate electrode,” as required by claim 28. To the extent this teaching is not found to be an explicit disclosure of “the silicon nitride film

has a thickness smaller than that of the first gate electrode,” a POSITA would have found it obvious that Akasaka’s silicon nitride film 312 has a smaller thickness than Akasaka’s conductive films 319 and 320, collectively, in area 301B (i.e., the first gate electrode 104) in my opinion.

319. The only differences between Aoyama and Akasaka regarding claim 28 are minor differences in the ranges of their respective gate dielectric and gate electrode thicknesses. As I demonstrate below, however, these differences do not meaningfully affect the analysis I provide in Section X.A.5. Thus, in my opinion, a POSITA would have found claim 28 obvious in view of Akasaka for at least the same four reasons discussed in that section, as well as the relative thicknesses depicted in Akasaka’s FIG. 26.

320. A POSITA would have expected Akasaka’s silicon nitride film 312 to have a smaller thickness than Akasaka’s conductive films 319 and 320, collectively, in area 301B in my opinion. In the process Akasaka describes for manufacturing its semiconductor device, Akasaka’s nFET and pFET gate electrodes in areas 301A and 301B are planarized to have the same total height. Ex.1008, ¶¶73-76, 84-86, FIGS. 19, 25. As a result, and as the red arrow indicates (*see id.*, FIG. 26 (above)), the thickness of silicon nitride film 312 (brown), plus the thickness of inter-level insulating film 313 (blue), is necessarily equal to the total nFET gate height (i.e., the

sum of thicknesses of gate dielectric film 315 and conductive films 319 and 320).

The following must be true:

$$T_{312} + T_{313} + T_{315} = T_{319} + T_{320} \quad (\text{Eq. 5})$$

where T_x is the thickness of layer x above the substrate. Thus, claim 28 applied to Akasaka requires:

$$T_{312} < T_{319} + T_{320} \quad (\text{Eq. 6})$$

$$T_{319} + T_{320} + T_{313} > T_{315} + T_{319} + T_{320} \quad (\text{Eq. 7})$$

321. Canceling the common variable on both sides of the inequality (i.e., $T_{319} + T_{320}$) gives the following relationship between the thickness of Akasaka's inter-level dielectric film 313 and the thickness of Akasaka's gate dielectric film 315:

$$T_{132} + T_{144} > T_{102} \quad (\text{Eq. 8})$$

Thus, Akasaka satisfies claim 28 so long as the thickness of inter-level dielectric film 313 is greater than the thickness of gate dielectric film 315.

322. This inequality illustrates why a POSITA would have expected Akasaka's inter-level dielectric film 313 to be significantly thicker than Akasaka's gate dielectric film 315 in my opinion and would have found it highly unusual were it otherwise.

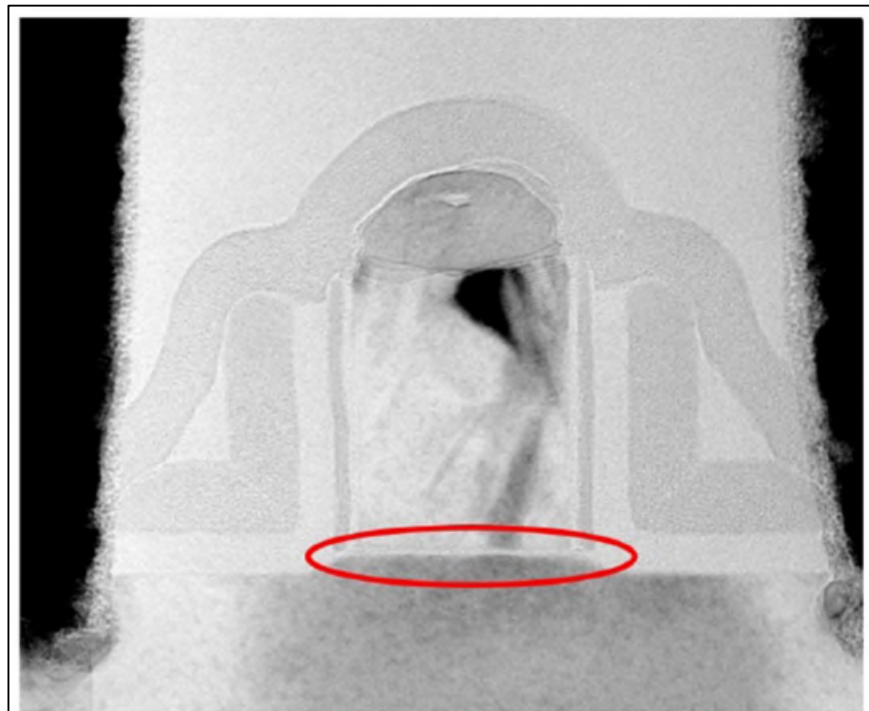
323. A POSITA would have known the thickness of a gate dielectric is negligible compared to a gate electrode in my opinion. A POSITA would have known the gate dielectric to be a thin insulating layer, which is necessary to achieve a large

capacitance. *See* Ex.1511, xiii (describing “the high drive current and gate capacitance required of scaled MOSFETs”). Interlayer dielectric films, on the other hand, require small capacitance and are thus much thicker. That is, “gate and interlayer (ILD) dielectric films” have “opposing requirements” in terms of thickness. *See id.*

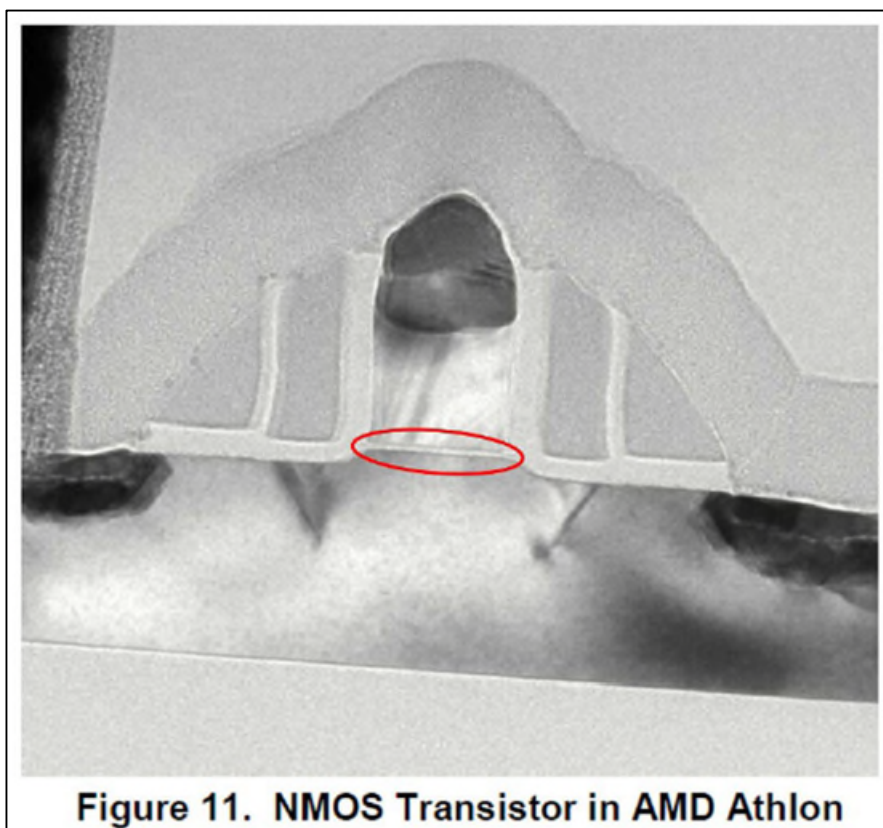
324. According to Akasaka, gate dielectric layer 315 is “is preferably set to agree with an effective film thickness (EOT) of 1.5 nm or less.” Ex.1008, ¶75. Since $EOT = \text{thickness} \times (3.9/\kappa)$, gate dielectric film 315 must have a thickness (in nm) of $(1.5/3.9)\kappa$ or less. Ex.1511, xiii (explaining that “ $t_{ox(eq)} = t_{diel}(3.9/k_{diel})$ ”). For $\kappa = 30$ (an extreme case), the thickness would be less than about 11.5 nm. *See id.*, xiii (“Dielectrics with values approximately between 10 and 30 are under consideration.”). For $\kappa = 10$, the thickness would be about 3.8 nm.

325. Being generous with the value of κ , a POSITA thus would have understood Akasaka to disclose that the gate dielectric layer 315 has a thickness at most about 12 nm, although a more realistic number would have been in the range of about 2 nm to 4 nm. *See* Ex.1514, ¶¶[0004], [0043] (less than 3.0 nm), Tbl. 1 (same); Ex.1005, ¶[0106] (2.0 nm); Ex.1001, 11:31-34 (2 nm), 24:36-39 (same). The difference between 2 nm and 12 nm is immaterial to my analysis because gate dielectric film 315, like all gate dielectric films in this technology, is extremely thin—much thinner than any interlayer dielectric film.

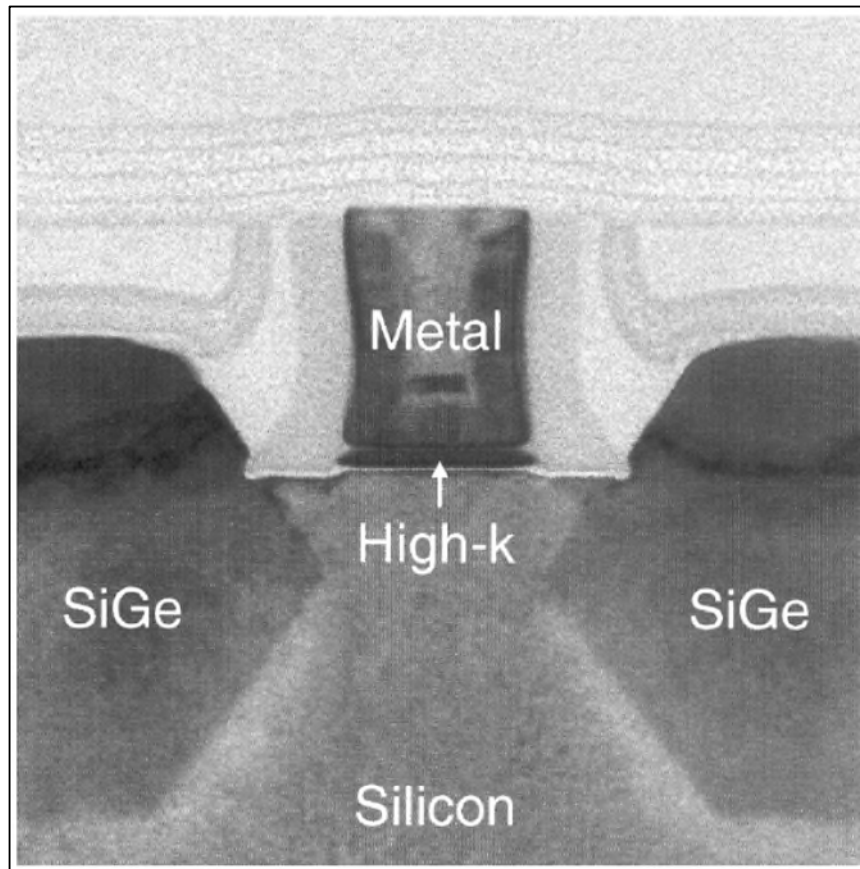
326. Several semiconductor devices fabricated before the filing of the application that resulted in the '686 patent illustrate the thickness disparity recited in claim 28 visually. See Ex.1525, Figs. 3 (below), 5-6, 8-10, 11 (below), 12; Ex.1516, Fig. 6 (showing Intel's 45nm device); Ex.1517, 16 (same) (below), 19; Ex.1523, Fig. 2; Ex.1528, Fig. 1.



Ex.1525, Fig. 3 (annotated)



Ex.1525, Fig. 11 (annotated)



Ex.1517, 16 (excerpted)

327. As another example that is similar to Akasaka, Nakajima (see FIG. 52 (below)) teaches a metal layer 403 that is 20 nm thick and a metal layer 405 that is 100 nm thick, meaning the gate electrode is at least about 120 nm thick. Ex.1534, ¶317.

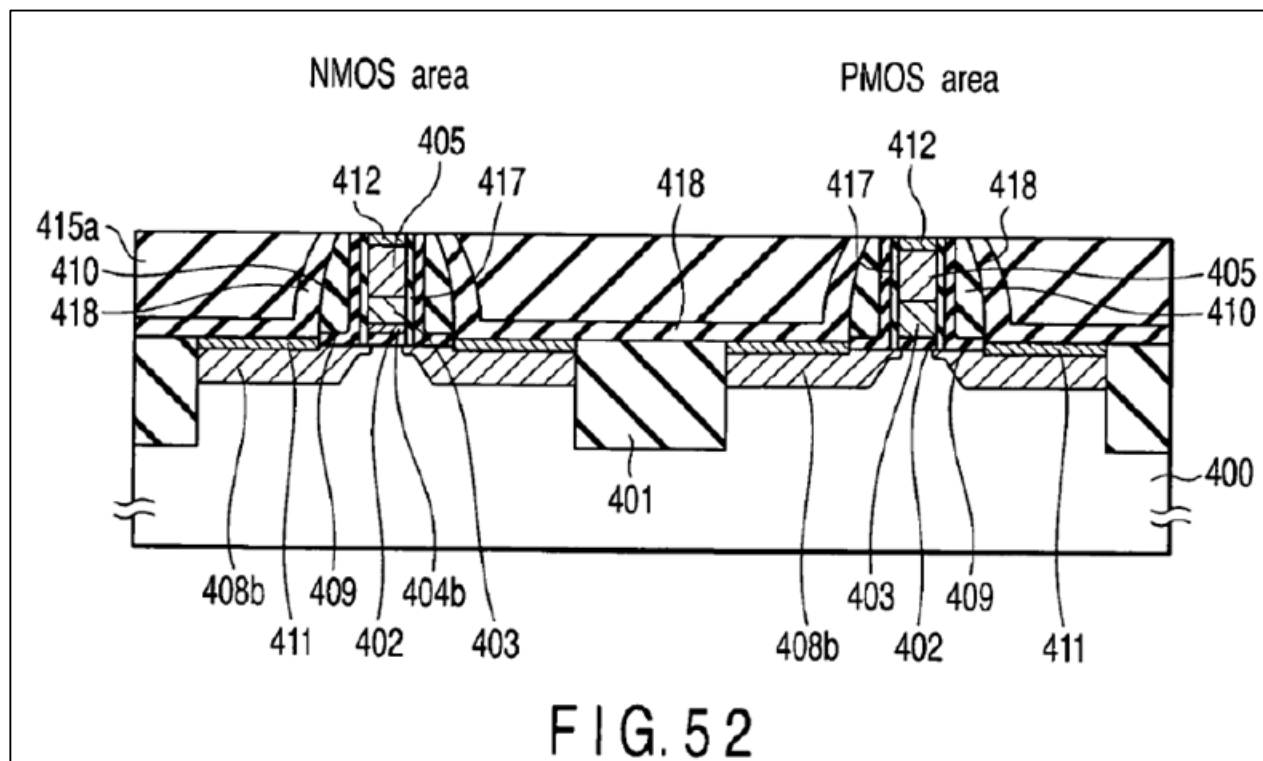


FIG. 52
Ex.1534, FIG. 52

The silicon nitride CESL 418 is only about 30 nm thick, and interlayer insulating layer 415a is initially 250 nm thick before being planarized down to what is still more than 90 nm thick (the difference between the thickness of gate electrode layers 403 and 405, minus the thickness of CESL 418). *Id.*, ¶326, FIGS. 51-52. A thickness of 90 nm is more than an order of magnitude thicker than any conceivable gate dielectric layer, which is indicative of the relative thicknesses a POSITA would have expected.

328. In my opinion, a POSITA also would have found it obvious for Akasaka's gate dielectric film 315 to have a smaller thickness than Akasaka's inter-level dielectric film 313 is that this was one of only a small number of possibilities and the most well-known of those limited options.

329. In my opinion, there was a design need to make Akasaka's inter-level dielectric film 313 thicker than Akasaka's gate dielectric film 315 because "gate and interlayer (ILD) dielectric films" have "opposing requirements" in terms of thickness. *See* Ex.1511, xiii. This would have indicated to a POSITA that Akasaka's inter-level dielectric film 313 should be thicker than Akasaka's gate dielectric film 315. The result, as I explain above, is that Akasaka's silicon nitride film 312 would be thinner than Akasaka's nFET gate electrode (i.e., the collective height of conductive films 319 and 320), as required by claim 28.

330. Additionally, the design needs of Akasaka's device dictate only three options for the thickness of Akasaka's silicon nitride film 312: either it is thinner than Akasaka's nFET gate electrode, it is the same thickness as Akasaka's nFET gate electrode, or it is thicker than Akasaka's nFET gate electrode. Akasaka's planarized structure sets a restriction that the collective thickness of silicon nitride film 312 and inter-level insulating film 313 cannot exceed the height of Akasaka's gate structures. Of the finite number of identified, predictable solutions that comply with the design requirements of Akasaka's device, a silicon nitride film 312 thinner than Akasaka's nFET gate electrode was within the technical grasp of, and would have been expected by, a POSITA in my opinion. Numerous examples that would have been known to a POSITA before the application for the '686 patent confirm my opinion. *See, e.g.*, Ex.1516, Fig. 6; Ex.1525, Figs. 1-3, 5-6, 8-12; Ex.1528, Fig. 1; Ex.1523, Fig. 2.

331. Further, a POSITA would have found it obvious in my opinion for Akasaka's silicon nitride film 312 to have a thickness smaller than the collective thickness of conductive films 319 and 320 in area 301B (i.e., the first gate electrode) is that the disclosed thickness of Akasaka's conductive films 319 and 320 significantly exceeds the typical thickness used for silicon nitride etch stopper films like Akasaka's silicon nitride film 312.

332. Akasaka discloses that conductive film 320 is "about 40 to 50 nm" and that conductive film 319 is "about 1 to 2 nm." Ex.1008, ¶¶85-86. Thus, at minimum, Akasaka's nFET gate electrode is about 41 nm to 52 nm thick. In my opinion, a POSITA would have understood that silicon nitride etch stopper films like Akasaka's silicon nitride film 312 "ha[ve] a typical thickness of 20 nm" or so—much less than the minimum thickness of Akasaka's nFET gate electrode. Ex.1535, 1446. That is, a typical silicon nitride CESL thickness was less than a typical gate electrode thickness in MOSFETs like Akasaka's. See Ex.1534, ¶¶317, 326, FIG. 52; Ex.1516, Fig. 6; Ex.1525, Figs. 1-3, 5-6, 8-12; Ex.1528, Fig. 1; Ex.1523, Fig. 2.

333. Even further, a POSITA would have found it obvious for Akasaka's silicon nitride film 312 to have a smaller thickness than the thickness of conductive films 319 and 320 in area 301B (i.e., the first gate electrode) in my opinion because that the thickness of Akasaka's silicon nitride film 312 affects the amount of stress and tuning that thickness would have been a matter of routine optimization. Silicon

nitride CESL thickness was a variable that would have been known by a POSITA to affect stress. *See generally* Ex.1535. Eneman, for example, details “[t]he effect [of scaling] on CESL-induced stress” due to silicon nitride CESL films. *Id.*, 1447. Silicon nitride CESL thickness was thus a known, result-effective variable. *See, e.g., id.*, 1447-48, Figs. 2-3.

334. Implementing Akasaka’s silicon nitride film 312 to be thinner than the thickness of conductive films 319 and 320 in area 301B (i.e., the first gate electrode), as required by claim 28, would not have yielded any unexpected results to a POSITA in my opinion, as the relationship between silicon nitride CESL thickness and the stress it induces was known and predictable. *See generally* Ex.1535 (including Fig. 3).

335. For all of the foregoing reasons, in addition to the relative thicknesses disclosed by Akasaka’s FIG. 26 explained above, it is my opinion that Akasaka combined with Hsu823 discloses claim 28 of the ’686 patent.

6. Dependent Claim 31: “The semiconductor device of claim 25, wherein the first and second gate insulating films are made of the same insulating material”

336. Akasaka’s gate dielectric film 315 “is depos[it]ed all over the substrate” at once using the same insulating material (HfSi_xO_y) for both nFET and pFET devices. *See* Ex.1008, ¶¶74-75, FIG. 19. As I explain above, the claimed first gate insulating film is disclosed by Akasaka’s gate dielectric film 315 in nFET area 301B and the claimed second gate insulating film is disclosed by Akasaka’s gate dielectric film

315 in pFET area 301A. Akasaka's gate dielectric film 315 is formed of hafnium silicon oxide (HfSi_xO_y), which is "a gate dielectric (insulating) film 315" (*id.*, ¶75) and is one of the exemplary gate dielectric films that the '686 patent identifies. Ex.1001 29:16-24 ("examples "include hafnium-based oxides such as . . . hafnium silicate (HfSiO) . . .").

337. Since Akasaka's gate dielectric film 315 is used to form both the claimed "first gate insulating film" and the claimed "second gate insulating film," Akasaka discloses "the first and second gate insulating films are made of the same insulating material," as required by claim 31.

338. Therefore, it is my opinion that Akasaka combined with Hsu823 discloses claim 31 of the '686 patent.

7. Dependent Claim 35: "The semiconductor device of claim 25, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more"

339. As I explain above, Akasaka's gate dielectric film 315 in nFET area 301B discloses the claimed "first gate insulating film" and Akasaka's gate dielectric film 315 in pFET area 301A discloses the claimed "second gate insulating film." Akasaka's gate dielectric film 315 is formed of hafnium silicon oxide (HfSi_xO_y), which, in my opinion, a POSITA would have understood to disclose a "high-k film made of a metal oxide having a relative dielectric constant of 10 or more." *See*

Ex.1008, ¶75; Ex.10014, ¶4] (listing “hafnium (Hf)-containing material such as . . . HfSiO_x” as a “high-k material [with] dielectricity of more than ten (10)”); Ex.1511, xiii (“Dielectrics with values approximately between 10 and 30 are under consideration.”); Ex.1515, ¶¶2 (explaining that a “high-k dielectric means having a dielectric constant higher than 10”), 8 (similar). In fact, hafnium silicon oxide is one of the exemplary gate dielectric films that the ’686 patent identifies. Ex.1001 29:16-24 (“examples “include hafnium-based oxides such as . . . hafnium silicate (HfSiO)” Ex.1001, 29:16-24.

340. Therefore, it is my opinion that Akasaka combined with Hsu823 discloses claim 35 of the ’686 patent.

XI. CONCLUSION

341. For the aforementioned reasons, in my opinion, to a POSITA, the Challenged Claims of the ’686 patent are rendered obvious by the prior art.

342. I understand that the Patent Owner has not asserted secondary considerations of non-obviousness. I reserve the right to respond to any such assertions.

Declaration of Dr. Sanjay Banerjee
Inter Partes Review of U.S. Patent No. 8,198,686

343. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the results of the proceedings.

Date: June 5, 2025

Respectfully submitted,



Sanjay Banerjee, Ph.D.