

Filed on behalf of:

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Petitioner

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UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNITED MICROELECTRONICS CORPORATION,
AND
UMC GROUP (USA),
Petitioner,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,
Patent Owner.

Case IPR2025-01091
U.S. Patent No. 8,198,686

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 8,198,686
UNDER 35 U.S.C. §§ 311, 312 AND 37 C.F.R. § 42.104**

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EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 8,198,686 B2 to Sato et al. (“ ’686 patent”)
1002	Prosecution History of the ’686 patent (“Prosecution History”)
1003-1004	RESERVED
1005	U.S. Patent Application Publication No. 2007/0215950 A1 to Aoyama (“Aoyama”)
1006	U.S. Patent Application Publication No. 2007/0235823 A1 to Hsu et al. (“Hsu823”)
1007	RESERVED
1008	U.S. Patent Application Publication No. 2007/0066077 A1 to Akasaka et al. (“Akasaka”)
1009-1042	RESERVED
1101	Declaration of Dr. Sanjay Banerjee
1102	Curriculum Vitae of Sanjay Banerjee, PhD
1103	“Stress Memorization Technique (SMT) by Selectively Strained-Nitride Capping for Sub-65nm High-Performance Strained-Si Device Application,” Chen et al., 2004 Symposium on VLSI Technology Digest of Technical Papers (2004) (“Chen-2004”)
1104	“35% Drive Current Improvement from Recessed-SiGe Drain Extensions on 37 nm Gate Length PMOS,” Chidambaram et al., 2004 Symposium on VLSI Technology Digest of Technical Papers (2004) (“Chidambaram-2004”)
1105	“Self-Aligned Ultra Thin HfO ₂ CMOS Transistors with High Quality CVD TaN Gate Electrode,” Lee et al., 2002 Symposium On VLSI Technology Digest of Technical Papers (2002) (“Lee-2002”)

Exhibit No.	Description
1106	“Delaying Forever: Uniaxial Strained Silicon Transistors in a 90nm CMOS Technology,”Mistry et al., 2004 Symposium on VLSI Technology Digest of Technical Papers (2004) (“Mistry-2004”)
1107	“Effects of High-Temperature Forming Gas Anneal on HfO ₂ MOSFET Performance,”Onishi et al., 2002 Symposium On VLSI Technology Digest of Technical Papers (2002) (“Onishi-2002”)
1108	“Low Standby Power CMOS with HfO ₂ Gate Oxide for 100-nm Generation,”2002 Symposium On VLSI Technology Digest of Technical Papers (2002) (“Pidin-2002”)
1109	“Mobility Enhancement in Strained Si NMOSFETs with HfO ₂ Gate Dielectrics,”Rim et. al., 2002 Symposium On VLSI Technology Digest of Technical Papers (2002) (“Rim-2002”)
1110	“Metal Gate MOSFETs with HfO ₂ Gate Dielectric,” Samavedam et al., 2002 Symposium On VLSI Technology Digest of Technical Papers (2002) (“Samavedam-2002”)
1111	“55nm high mobility SiGe(:C) pMOSFETs with HfO ₂ gate dielectric and TiN metal gate for advanced CMOS,” Weber et al., 2004 Symposium on VLSI Technology Digest of Technical Papers (2004) (“Weber-2004”)
1112-1210	RESERVED
1211	Van Zant, “Microchip Fabrication”(Fifth Ed. 2004) (“Van Zant”)
1212	RESERVED
1213	Houssa, M., “High-k Dielectrics”to Houssa (IOP Publishing Ltd. 2004) (“Houssa”)
1214-1215	RESERVED

Exhibit No.	Description
1216	“International Technology Roadmap for Semiconductors: Process Integration, Devices, and Structures” (2007 ed.) (“ITRS-PIDS”)
1217-1222	RESERVED
1223	“Semiconductor Devices: Physics and Technology” by Sze (Second Edition, 2002) (“Sze-2002”)
1224-1225	RESERVED
1226	U.S. Patent No. 7,709,331 to Karve, et al. (“Karve”)
1227	U.S. Patent No. 8,017,469 to Luo, et al. (“Luo”)
1228	RESERVED
1229	Wolf, “Silicon Processing for the VLSI Era, Volume 3 – The Submicron MOSFET”(1995) (“Wolf-3”)
1230-1317	RESERVED
1318	Wilk, G. D., et al., “High-k gate dielectrics: Current status and materials properties considerations,” Journal of Applied Physics, Vol. 89, No. 10, pp. 5243-75, May 15, 2001 (“Wilk”)
1319-1322	RESERVED
1323	U.S. Patent No. 6,306,712 to Rodder, et al. (“Rodder”)
1324-1332	RESERVED
1333	Plummer, J., et al., “Silicon VLSI Technology: Fundamentals, Practice and Modeling” (Prentice Hall 2000) (“Plummer”)
1334	Wolf, S., “Silicon Processing for the VLSI Era, Volume 4 – Deep-Submicron Process Technology” (Lattice 2002) (“Wolf-4”)
1335-1339	RESERVED

Exhibit No.	Description
1340	Japanese Patent Publication JP2005-064190 to Ono with certified translation ("JP-Ono")
1341	N. Weste and D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", Third Edition (Pearson/Addison Wesley, 2005) ("Weste")
1342-1405	RESERVED
1406	U.S. Patent Application Publication No. 2007/0249069 A1 to Alvarez et al. ("Alvarez")
1407-1412	RESERVED
1413	S.M. Sze, <i>Physics of Semiconductor Devices</i> (2d ed. 1981) (excerpted) ("Sze-1981")
1414-1418	RESERVED
1419	U.S. Patent Application Publication No. 2006/0286729 A1 to Kavalieros et al. ("Kavalieros729")
1420-1428	RESERVED
1429	U.S. Patent Application Publication 2004/0262784 A1 to Doris et al. ("Doris")
1430	U.S. Patent No. 6,797,556 B2 to Murthy et al. ("Murthy556")
1431	U.S. Patent Application Publication No. 2007/0134870 A1 to Lee et al. ("Lee870")
1432	U.S. Patent Application Publication No. 2005/0260810 A1 to Cheng et al. ("Cheng810")

Exhibit No.	Description
1433	U.S. Patent Application Publication No. 2009/0020820 A1 to Baik et al. ("Baik")
1434	U.S. Patent Application Publication No. 2008/0293207 A1 to Koutny et al. ("Koutny")
1435	U.S. Patent Application Publication No. 2010/0075476 A1 to Miyashita ("Miyashita")
1436-1510	RESERVED
1511	M. Baklanov et al., <i>Dielectric Films for Advanced Microelectronics</i> (2007) (excerpted) ("Baklanov")
1512	International Technology Roadmap for Semiconductors: Front End Processes (2007 ed.) ("ITRS_FEP")
1513	RESERVED
1514	U.S. Patent Application Publication No. 2006/0081939 A1 to Akasaka et al. ("Akasaka939")
1515	U.S. Patent Application Publication No. 2006/0022277 A1 to Kavalieros et al. ("Kavalieros277")
1516	K. Mistry, et al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging," Technical Digest of the of the 2007 IEEE International Electron Devices Meeting (IEDM), pp. 247-50 (Dec. 2007) ("Mistry2007")

Exhibit No.	Description
1517	K. Mistry, et al., “A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging,” presented at 2007 IEEE International Electron Devices Meeting (IEDM), pp. 1-37 (Dec. 2007) (“Mistry_Presentation”)
1518	U.S. Patent No. 6,881,631 B2 to Saito et al. (“Saito631”)
1519	U.S. Patent No. 7,812,414 B2 to Hou et al. (“Hou”)
1520	U.S. Patent Application Publication No. 2005/0258468 A1 to Colombo et al. (“Colombo”)
1521	U.S. Patent No. 6,849,511 B2 to Iriyama et al. (“Iriyama”)
1522	U.S. Patent Application Publication No. 2002/0037615 A1 to Matsuo (“Matsuo”)
1523	S.E. Thompson et al., “A 90-nm Logic Technology Featuring Strained Silicon,” IEEE Transactions on Electron Devices, vol. 51. No. 11, pp. 1790-97 (Nov. 2004) (“Thompson-2004”)
1524	Y. Sun et al., “Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors,” Journal of Applied Physics, vol. 101, Art. No. 104503 (22 pages) (May 2007) (“Sun-2007”)
1525	D. James, “2004 – The Year of 90-nm: A Review of 90 nm Devices,” 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 72-77 (2005) (“James”)
1526	U.S. Patent Application Publication No. 2006/0148151 A1 to Murthy et al. (“Murthy151”)

Exhibit No.	Description
1527	U.S. Patent Application Publication No. 2004/0262683 A1 to Bohr et al. ("Bohr")
1528	P. Morin et al., "Extensive Study of the Correlation between Contact Etch Stop Nitride Material Properties and Negative Bias Temperature Instabilities Measured in pMOSFETS," ECS Transactions, vol. 6, no. 3, pp. 355-69 (2007) ("Morin-2007")
1529	U.S. Patent Application Publication No. 2005/0170104 A1 to Jung et al. ("Jung")
1530	Y.C. Liu et al., "Single Stress Liner for Both NMOS and PMOS Current Enhancement By a Novel Ultimate Spacer Process," Technical Digest of the 2005 IEEE International Electron Devices Meeting (IEDM), pp. 836-39 (Dec. 2005) ("Liu")
1531	U.S. Patent Application Publication No. 2008/0145984 A1 to Ke et al. ("Ke")
1532	P. Bai et al., "A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell," Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 657-60 (Dec. 2004) ("Bai-2004")
1533	Westlinder et al., "On the Thermal Stability of Atomic Layer Deposited TiN as Gate Electrode in MOS Devices," IEEE Electron Device Letters, vol. 24, no. 9, pp. 550-552 (Sept. 2003) ("Westlinder")
1534	U.S. Patent Application Publication No. 2007/0105317 A1 to Nakajima ("Nakajima")

Exhibit No.	Description
1535	G. Eneman et al., “Scalability of Stress Induced by Contact-Etch-Stop Layers: A Simulation Study,” IEEE Transactions on Electron Devices, vol. 54, no. 6, pp. 1446-53 (June 2007) (“Eneman”)
1536	M. Quirk & J. Serda, <i>Semiconductor Manufacturing Technology</i> , Ch. 12: Metallization (2001) (excerpted) (“Quirk”)
1537	U.S. Patent No. 7,785,952 B2 to Chang et al. (“Chang”)
1538	U.S. Patent No. 8,536,660 B2 to Hsu et al. (“Hsu660”)

Under 35 U.S.C. §§311, 312 and 37 C.F.R. §42.104, United Microelectronics Corporation and UMC Group (USA) (collectively, “Petitioner”) request *inter partes* review (“IPR”) of claims 25-28, 31, and 35 (“Challenged Claims”) of U.S. Patent No. 8,198,686 Ex.1001, “the ’686 patent”).

I. Introduction

The ’686 patent relates to “a semiconductor device including n- and p-type MIS transistors having gate electrodes made of different metal materials.” Ex.1001, 5:39-45. The basic concepts claimed in the ’686 patent were known before the application for the ’686 patent, and Petitioner, supported by the Declaration of Dr. Sanjay Banerjee (Ex.1101), demonstrates the Challenged Claims are unpatentable.

II. Certification of Grounds for Standing

Petitioner certifies under 37 C.F.R. §42.104(a) that the ’686 patent is available for IPR and Petitioner is not barred or estopped from requesting IPR of the Challenged Claims on the Grounds identified in this Petition.

III. Identification of Challenge and Requested Relief

A. Prior Art

The ’686 patent issued on June 12, 2012, from U.S. Patent Application No. 12/629,508, filed on December 2, 2009 as a continuation of PCT/JP2009/000574, filed on February 13, 2009. Ex.1001, cover. The ’686 patent claims priority to Japan Patent Application No. 2008-064435, filed on March 13, 2008, although Petitioner

does not acquiesce the '686 patent is entitled to its priority claim. *Id.* Regardless, each applied reference identified below was filed or published before March 13, 2008 and is prior art to the '686 patent.

Description	Date of Availability	Prior Art Status
U.S. Patent Application Publication No. 2007/0215950 A1 to Aoyama (“Aoyama”; Ex.1005)	Published September 20, 2007	Prior art under pre-AIA 35 U.S.C. §§102(a) and (e)
U.S. Patent Application Publication No. 2007/0235823 A1 to Hsu, et al. (“Hsu823”; Ex.1006)	Filed October 11, 2007	Prior art under pre-AIA 35 U.S.C. §102(b)
U.S. Patent Application Publication No. 2007/0066077 A1 to Akasaka, et al. (“Akasaka”; Ex.1008)	Published March 22, 2007	Prior art under pre-AIA 35 U.S.C. §§102(a) and (e)

B. Grounds for Challenge

The specific Grounds of the challenge are set forth below and are supported by the Declaration of Sanjay Banerjee, Ph.D. (Ex.1101).

Ground	Claim(s) Challenged	Basis 35 U.S.C. §	Reference(s)
I	25-28, 31, and 35	103 ¹	Aoyama (Ex.1005), Hsu823 (Ex.1006)
II	25-28, 31, and 35	103	Akasaka (Ex.1008), Hsu823 (Ex.1006)

IV. The '686 patent

A. Technical Background

The '686 patent describes MISFETs (metal-insulator-semiconductor field-effect transistors) having one gate structure for p-type devices and another gate structure for n-type devices. Such MISFETS and gate structures were already known.

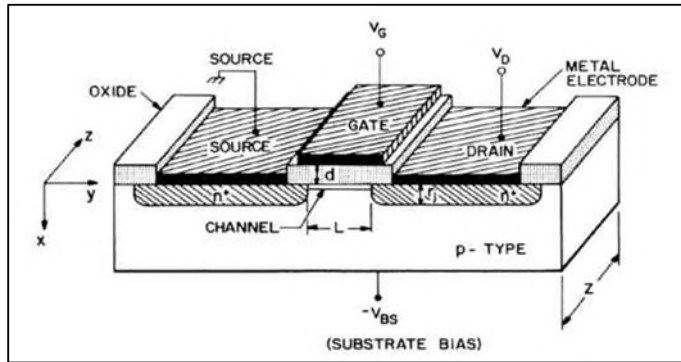
1. MISFETs

MISFETs² have **source/drain** regions for current input/output. Ex.1101, ¶34; Ex.1413, 9-10, Figs. 3, 6; Ex.1333, 45-51. Additionally, a **gate** overlies a **channel** region between source and drain. Ex.1101, ¶34; Ex.1413, 9-10, Fig. 3; Ex.1333, 40-45. The **gate** includes a **gate dielectric** that separates a **gate electrode** from the channel region. Ex.1101, ¶34; Ex.1413, 9-10, Fig. 3 (below); Ex.1333, 40-45.

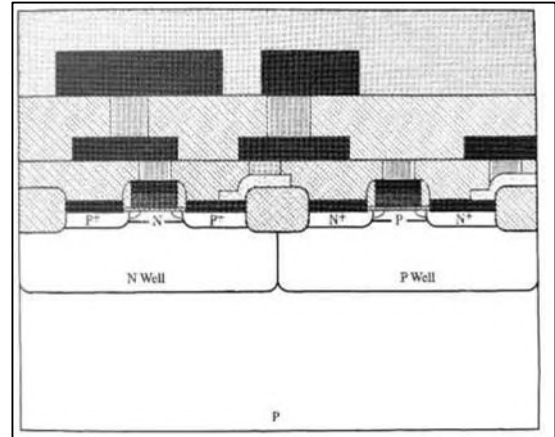
¹ Cites to 35 U.S.C. §§102 and 103 are to the pre-America Invents Act (pre-AIA).

² The terms “MISFET” and “MOSFET” (“Metal-**Oxide**-Semiconductor Field-Effect Transistor”) are interchangeable. Ex.1101, ¶34.

Applying voltage to the gate electrode controls a conductive channel to connect or disconnect the source and drain. Ex.1101, ¶34; Ex.1413, 9-10, 14, Figs. 3, 6.



Ex.1413, Fig. 3



Ex.1333, Fig. 1-11

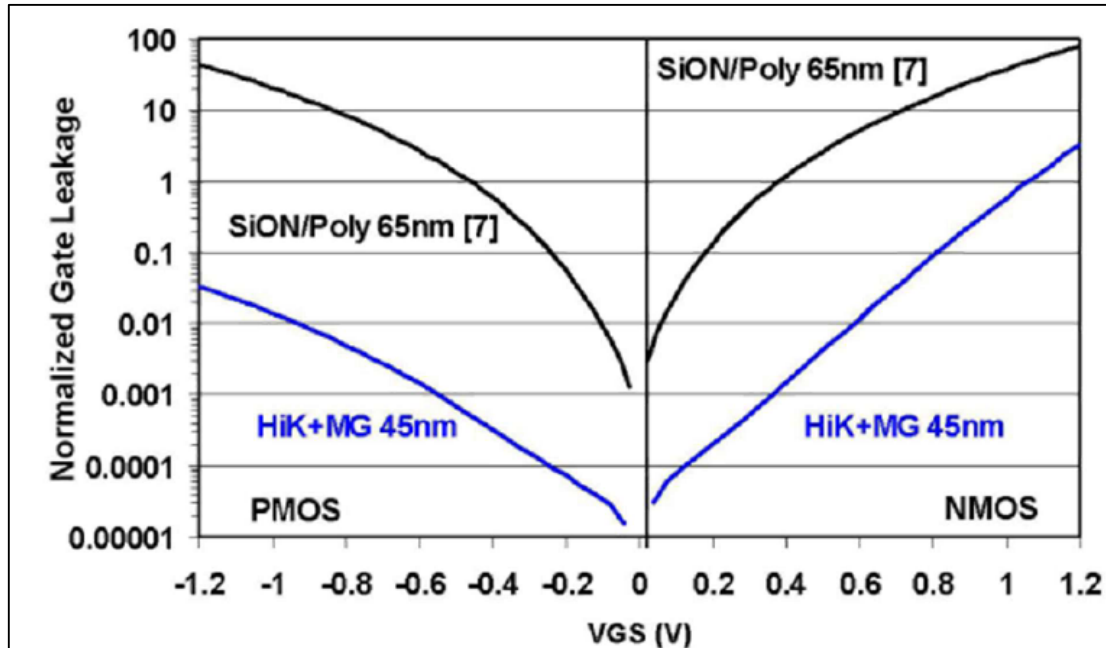
Generally, source/drain regions are **doped** with **p-type** or **n-type** impurities, and channel regions are oppositely doped. Ex.1101, ¶35; Ex.1413, 9-10; Ex.1333, 45-51. The terms **PMOS** (or “pFETs,” “pMIS,” “PMOSFETs,” or “PMISFETs”) and **NMOS** (or “nFETs,” “nMIS,” “NMOSFETs,” or “NMISFETs”) refer to MISFETs with p-type or n-type source/drain regions, respectively. Ex.1101, ¶35; Ex.1333, 16-17, 19-20, Figs. 1-11 (above), 2-2. Typical devices are **CMOS** (“Complementary MOS”), which include both PMOS and NMOS. Ex.1101, ¶36; Ex.1333, Fig. 1-11.

2. High-k Dielectrics

In early MISFETs, gate dielectrics were SiO₂. Ex.1511, 8. As MISFETs became smaller, their gate dielectrics became thinner to increase gate capacitance,

which improved drive currents and reduced power consumption. *Id.*; Ex.1512, 6, 24; Ex.1216, 5, 10, 12, 31, Fig. PIDS5; Ex.1514, ¶¶3-4. This eventually required SiO₂ layers so thin they could not reliably function. Ex.1511, 8; Ex.1514, ¶3; Ex.1515, ¶2. By 2008, the industry turned to **high-k** (a.k.a. “high-k”) dielectrics. Ex.1512, 6, 24; Ex.1216, 5, 10, 12, 31, Fig. PIDS5; Ex.1511, 8; Ex.1514, ¶4; Ex.1516, 1; Ex.1517, 25-28, 45; Ex.1101, ¶¶46-56.

High-k dielectrics have a larger **dielectric constant *k*** (“relative permittivity”) than SiO₂ ($\kappa=3.9$). Ex.1511, 8. For a given capacitance, high-k dielectrics are thicker than SiO₂, reducing gate leakage and power consumption while improving reliability. *Id.*; Ex.1101, ¶57. Examples include hafnium oxide, hafnium silicon oxide, and hafnium silicon oxynitride ($\kappa>10$). Ex.1514, ¶4; Ex.1515, ¶¶2, 8. Compared to devices with SiO₂ gate dielectrics, those with high-k dielectrics exhibit much less leakage. See Ex.1516, 2, Fig. 6 (below).



Ex.1516, Fig. 6

3. Replacement Metal Gates

In early MISFETs, the gate electrode was typically polysilicon. Ex.1518, 1:24-26. But a depletion region (effectively, an insulating barrier) forms at the polysilicon-gate dielectric interface, increasing resistance and reducing drive current. Ex.1518, 1:26-31; Ex.1519, 1:25-35; Ex.1520, ¶4. This became intolerable as gate dielectrics became thinner. Ex.1518, 1:31-34; Ex.1519, 1:36-44. With high-k gate dielectrics, a large threshold voltage offset also occurs because polysilicon dopants diffuse into them. Ex.1520, ¶5; Ex.1515, ¶3. To address these issues, the industry added metals to gate electrodes. Ex.1518, 1:31-34; Ex.1521, 1:28-34, 1:41-42; Ex.1512, 6-7, 24; Ex.1216, 5, 7, 31, Fig. PIDS5; Ex.1101, ¶71.

For example, a 2002 article by Samavedam et al. titled “Metal Gate MOSFETs with HfO₂ Gate Dielectric” recognized that “[m]etal gates will eliminate gate

depletion and address other issues like boron penetration and increased gate resistance, which will be aggravated as the poly gate thickness is scaled down.”). Samavedam-2002, Ex.1110, Introduction; *see also id.*, Conclusion (“We have successfully fabricated and characterized HfO_2 n-MOSFETs with TaSiN and PVD TiN gates and p-MOSFETs with CVD and PVD TiN gates using a conventional CMOS process. Metal-gated HfO_2 n-MOSFETs show a 104X gate leakage reduction compared to poly/ SiO_2 devices. Reasonable Ion/Ioff performance and reliability were observed in PVD TiN/ HfO_2 PMOS.”); *see also* Lee-2002, Ex.1105, Introduction (“As CMOS devices are scaled into sub-0.1 μm regime, poly-depletion effects and boron penetration become significant concerns. Therefore, metal gate electrodes are being explored to replace the polysilicon gate.”).

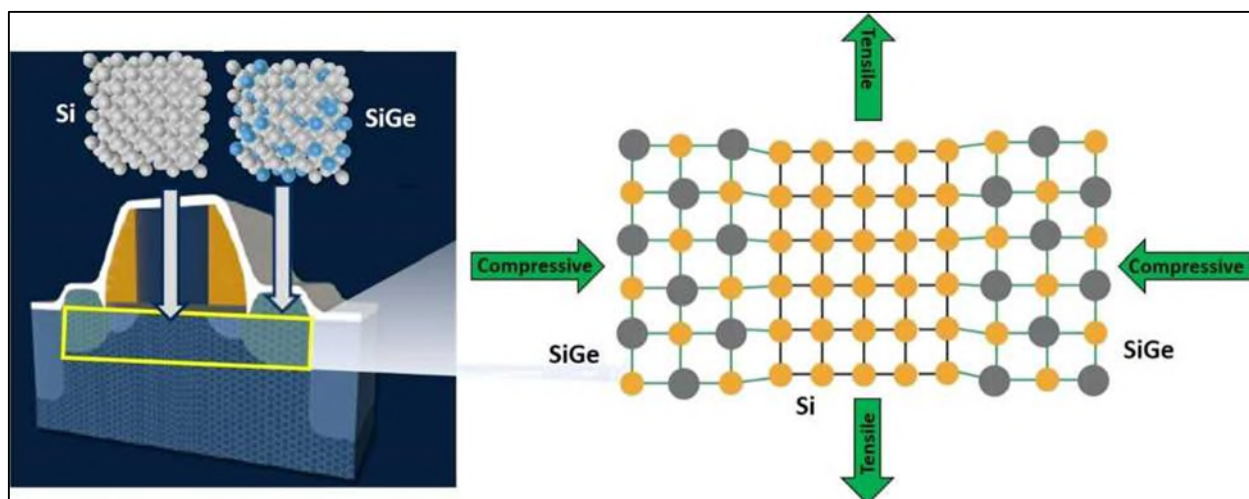
Just two years later, a 2004 article titled “55nm high mobility SiGe(:C) pMOSFETs with HfO_2 gate dielectric and TiN metal gate for advanced CMOS” concluded that “[f]or the first time, MOS transistors with compressively strained SiGe(:C) channel, metal gate and high-k dielectric are demonstrated down to 55nm gate length,” with significant improvements: “SiGe(:C) surface channel pMOSFETs with HfO_2 gate dielectric exhibit a 10^4 gate leakage reduction and a 65% mobility enhancement at high transverse effective field (1MV/cm) when compared to the universal SiO_2/Si reference.” Ex.1111, 42.

In CMOS, threshold voltage is minimized by adjusting the **work functions** of NMOS and PMOS metal gate electrodes. Ex.1519, 1:17-22; Ex.1520, ¶2. NMOS requires a work function less than about 4.6 eV; PMOS requires a work function greater than about 4.8 eV. Ex.1519, 1:17-22; Ex.1520, ¶¶20-21; Ex.1101, ¶75.

Suitable metals for NMOS devices were known, but options for PMOS devices exhibited less thermal stability. Ex.1519, 1:45-57; Ex.1521, 1:41-48. One solution was **replacement metal gates (“RMG”)**, a “gate-last” approach that avoids subjecting sensitive metal gates to high temperatures. Ex.1521, 2:22-29; Ex.1101, ¶77. This way, NMOS and PMOS gates can employ different and optimal work functions. Ex.1522, ¶21; Ex.1519, 2:11-14; Ex.1521, 2:10-12; Ex.1516, 1; Ex.1101, ¶¶78-80.

4. Strained Silicon Technology

PMOS was once much slower than NMOS. Strained-silicon technology changed that. Because germanium atoms are **larger** than silicon atoms, growing silicon-germanium (“SiGe”) source/drain regions **compressively** strains the silicon channel region along the current flow direction (left-to-right below). In PMOS, compressive strain improves carrier (hole) mobility and boosts operating speed. Ex.1523, 1-7; Ex.1524, 2 Ex.1101, ¶82. By 2005, this technology increased “hole mobility by as much as 50%.” Ex.1525, 2; Ex.1101, ¶82.



These principles were also commonly applied to NMOS, except improving NMOS carrier (electron) mobility requires **tensile** strain, not compressive. Ex.1101, ¶84. Creating tensile strain with source/drain regions requires growing a material like silicon carbide (SiC) with an atom (e.g., carbon) **smaller** than silicon. Ex.1526, ¶¶5, 48, 72; Ex.1525, 2; Ex.1527, ¶45; Ex.1101, ¶87.

Numerous prior art references recognized the benefits of strained silicon, for both PMOS and NMOS transistors. Ex.1104, Introduction (“Epitaxial SiGe, grown in recessed Si, has been used to compressively strain the PMOS channel and increase the hole mobility”), Abstract (“A highly compressive SiGe layer, in close proximity to the channel, results in large hole mobility improvements.”); Ex.1106, 50 (explaining “[t]he use of strain to improve mobility has been known for 50 years,” and concluding that “[u]ni-axial strained silicon has been implemented in a high volume manufacturing 90nm logic technology for the first time, with impressive performance results and improved power scaling.”); Ex.1101, ¶83. Thus, as seen in

Figs. 2-4 (below) from Mistry-2004 (Ex.1106), compressive stress from SiGe source/drain regions on PMOS transistors and tensile stress on NMOS transistors from a high tensile stress nitride overlayer were well known to improve transistor performance. Ex.1101, ¶84.

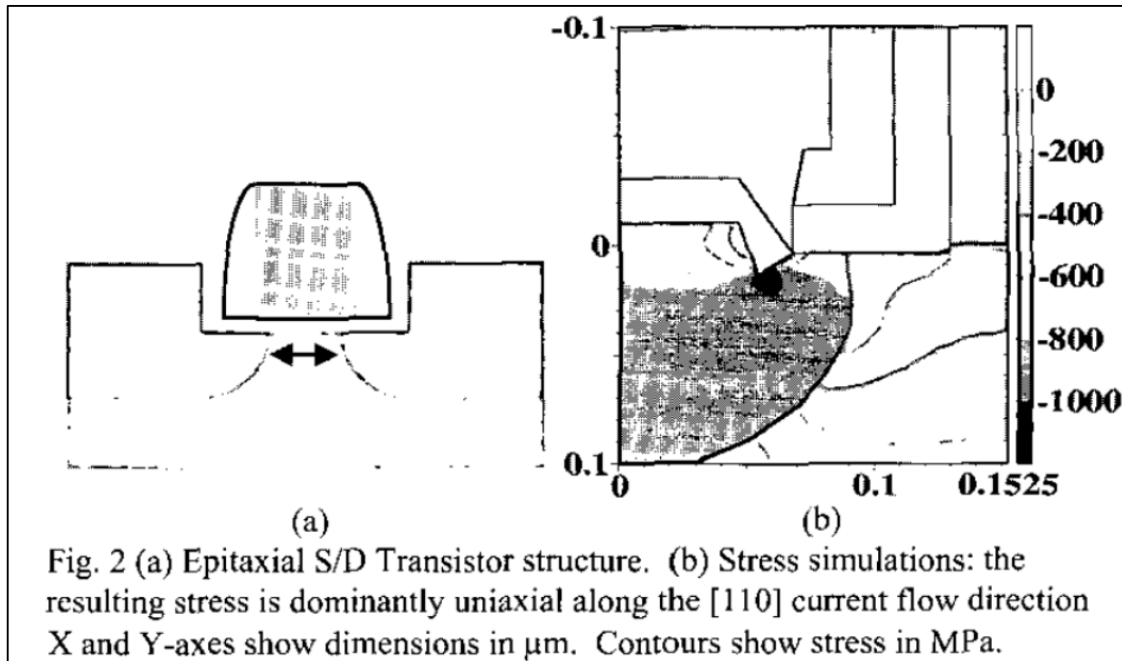


Fig. 3 TEM of NMOS transistor showing high tensile stress nitride overlayer.

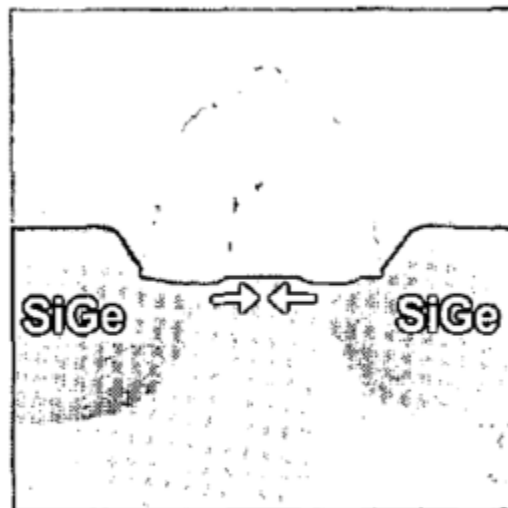


Fig. 4 TEM of PMOS showing SiGe heteroepitaxial S/D inducing uniaxial strain.

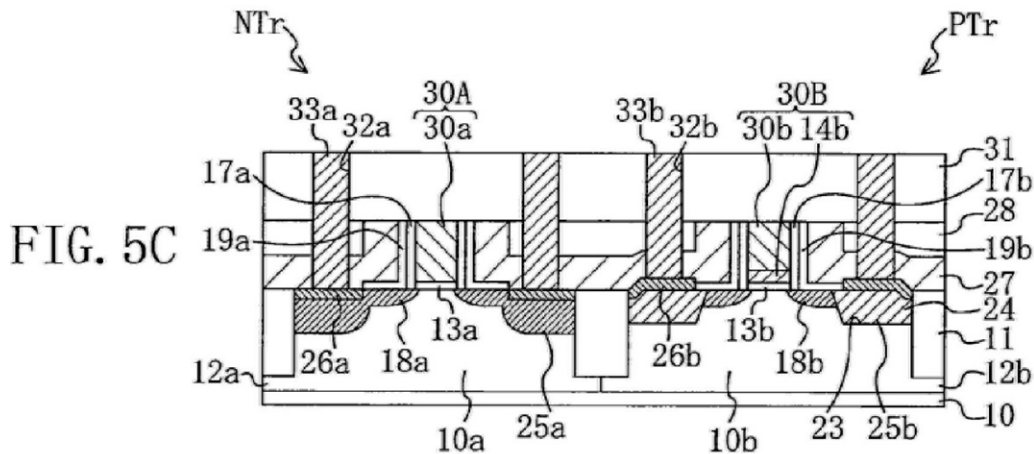
Mistry-2004, Ex.1106, Figs. 2-4

In addition to source/drain epitaxy, it was also common to induce strain by applying stressed films. Ex.1101, ¶88; Ex.1525, 2, 4; Ex.1528, 1-2, 13; Ex.1006, ¶3; Ex.1529, ¶90; Ex.1530, 1-2, Figs. 1-7; Ex.1523, Fig. 5(c). For example, depositing a silicon nitride contact etch-stop layer (“CESL”) can, under certain conditions, “apply[] stress to [a] channel region” to improve carrier mobility. Ex.1006, ¶3; see Ex.1531, ¶3; Ex.1529, ¶90; Ex.1528, 1-2; Ex.1530, 1-2; Ex.1101, ¶88. Depending how such a layer is prepared, it may be tensile, compressive, or unstrained. Ex.1529, ¶¶17, 99-100, 131-132, TBLS. IV-V, VII, FIG. 15.

Strained Si technology was well-known before the ’686 patent. Three generations of high-volume commercial devices already used it by then. Ex.1523, 1-2 (Intel 90nm devices); Ex.1532, 4-5 (Intel 65nm devices); Ex.1516, 1-2 (Intel 45nm devices); Ex.1101, ¶89.

B. ’686 patent Overview

The ’686 patent describes a known application of the technologies described above, including “n-[type] and p-type MIS transistors having gate electrodes made of different metal materials.” Ex.1001, 5:39-42. Figure 5C below illustrates one embodiment. *Id.*, 11:56-67, 12:8-17, 12:50-63, 14:51-15:5, 16:10-22, 16:55-60, FIGS. 1A-5C.

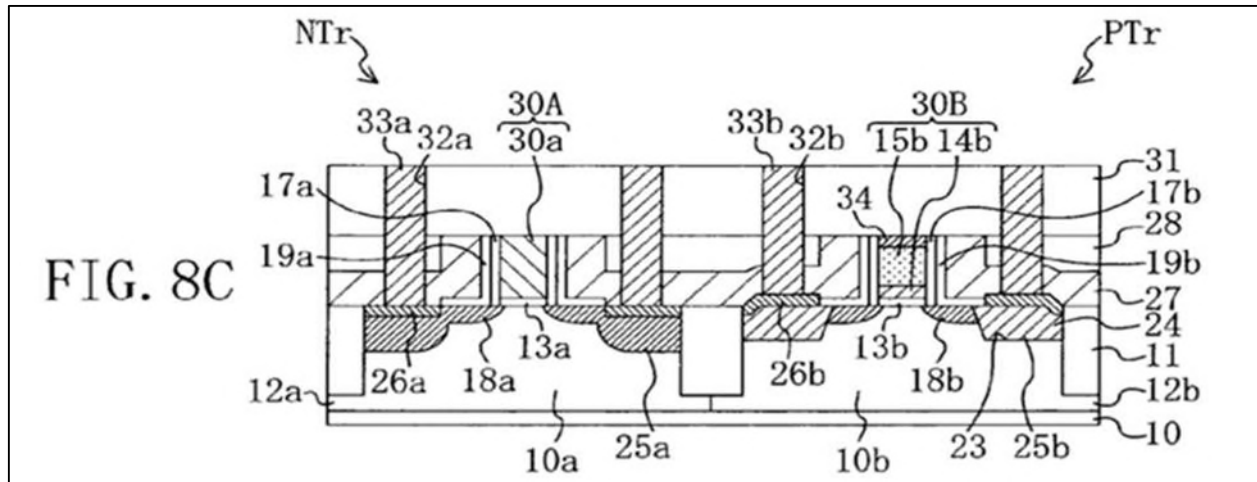


'686 Patent's FIG. 5C

NTr:	<u>nMIS transistor</u>	PTr:	<u>pMIS transistor</u>
13a:	gate insulating film	13b:	gate insulating film
30A:	first gate electrode	30B:	second gate electrode
30a:	metal film	14b:	metal film
		30b:	conductive film
17a:	insulative sidewall spacer	17b:	insulative sidewall spacer
19a:	insulative sidewall spacer	19b:	insulative sidewall spacer
<u>nMIS & pMIS Transistors</u>			
27:	insulating film	28:	inter-layer insulating film

Gate insulating films 13a/13b may be formed of the same or different materials (e.g., a high-k metal-oxide). Ex.1001, 11:31-37, 29:16-24. As shown above in Figure 5C, insulating film 27 (e.g., silicon nitride) does not overlie any upper surface of the gate electrodes. *Id.*, 6:42-45, 15:6-22, 15:23-30.

In some embodiments (e.g., FIG. 5C), pMIS conductive film 30b may be the same material as nMIS metal film 30a. In other embodiments (e.g., FIG. 8C below), pMIS conductive film 15b is silicon, and a metal silicide film 34 is formed in it. *Id.*, 21:61-67, 22:33-49.



The '686 patent describes stressed active regions 10a/10b. Ex.1001, 28:63-29:15. In second active region 10b, silicon mixed crystal layer 24 (e.g., SiGe) may be formed in trenches 23 to compressively stress the pMIS channel. *Id.*, 13:60-65, 19:54-61, 23:28-33. In first active region 10a, insulating film 27 applies tensile stress to the nMIS channel. *Id.*, 28:16-43.

C. Prosecution History

The Prosecution History includes four office actions and narrowing amendments. *See generally* Ex.1002. In a first office action, the Examiner rejected certain claims based on Aoyama's first embodiment (FIGS. 1-2N). Ex.1002, 201-

06. This Petition, however, relies on Aoyama's third embodiment, as disclosed with reference to FIGS. 5-6Q, for example, which the Examiner never addressed or cited.

D. Claim Construction

Petitioner does not believe any claims require construction to resolve the patentability disputes in this proceeding. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

E. Level of Ordinary Skill

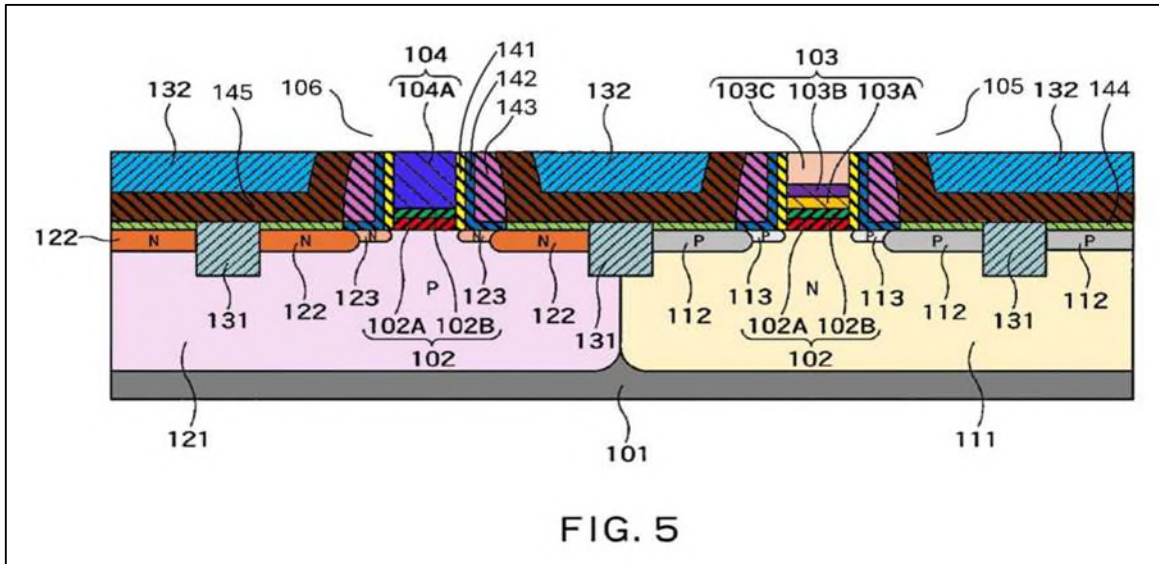
A POSITA would have had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. Ex.1101, ¶¶114-117. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education. *Id.*

V. Prior Art

A. Aoyama (Ex.1005)

Aoyama is prior art under pre-AIA §§102(a) and (e). Because Aoyama is in the same field (MISFETs) and reasonably pertinent to a problem the '686 patent addresses (high-k/metal gate design), Aoyama is analogous art. Ex.1101, ¶120.

This Petition focuses on Aoyama's third embodiment, an example of which is illustrated in Figure 5 below. Ex.1005, ¶¶97-121, FIGS. 5-6Q.



Aoyama, FIG. 5³

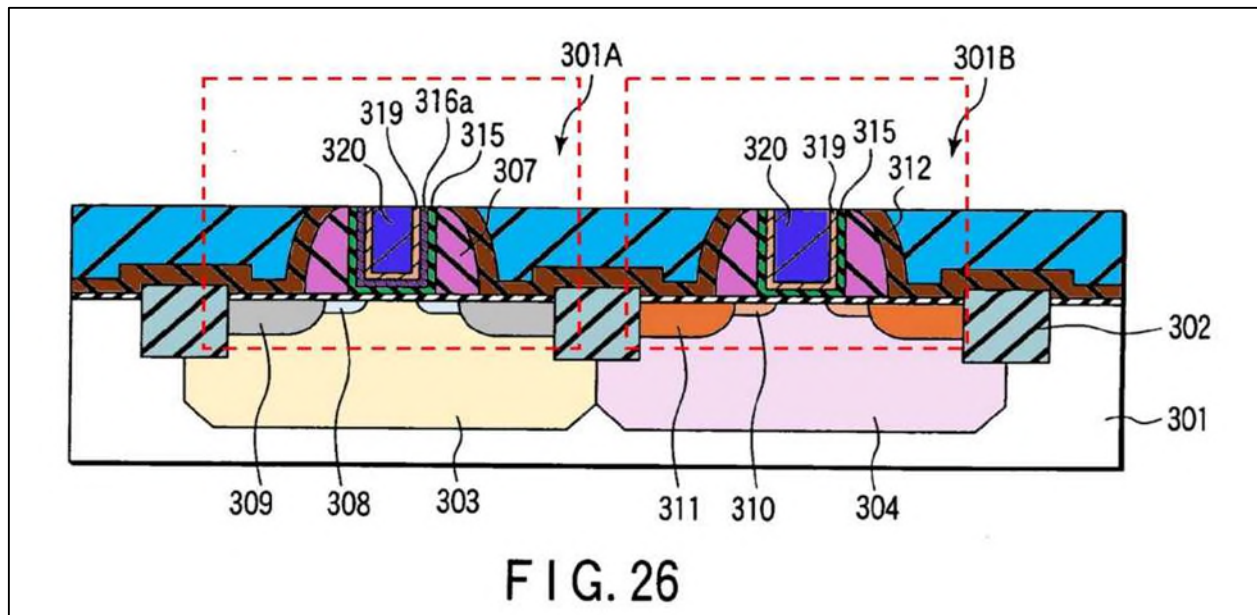
Both the NMOS (106) and PMOS (105) include a silicon oxide gate layer 102A, a high-k gate dielectric layer 102B, and spacers 141-143. *Id.*, ¶¶98, 111. Over the high-k film, their gate structures differ. Specifically, PMOS gate electrode 103 includes a first conductive layer 103A, a second conductive layer 103B, and a semiconductor layer (silicide layer) 103C. *Id.*, ¶¶107, 114, 121. NMOS gate electrode 104 includes only a third conductive layer 104A. *Id.*, ¶118. Etch stopper 145 and interlayer dielectric 132 fill the spaces between the NMOS and PMOS gate structures. *Id.*, ¶113; Ex.1101, ¶¶121-22.

³ Petitioner has added all color annotations in this Petition. Additionally, Aoyama's Figure 5 has been amended throughout to include all relevant numeric labels.

B. Akasaka (Ex.1008)

Akasaka is prior art under pre-AIA §102(b). Because Akasaka is in the same field (MISFETs) and reasonably pertinent to a problem the '686 patent addresses (high-k/metal gate design), Akasaka is analogous art. Ex.1101, ¶127.

Akasaka describes MISFETs as shown below. Ex.1008, ¶72, FIG. 26.



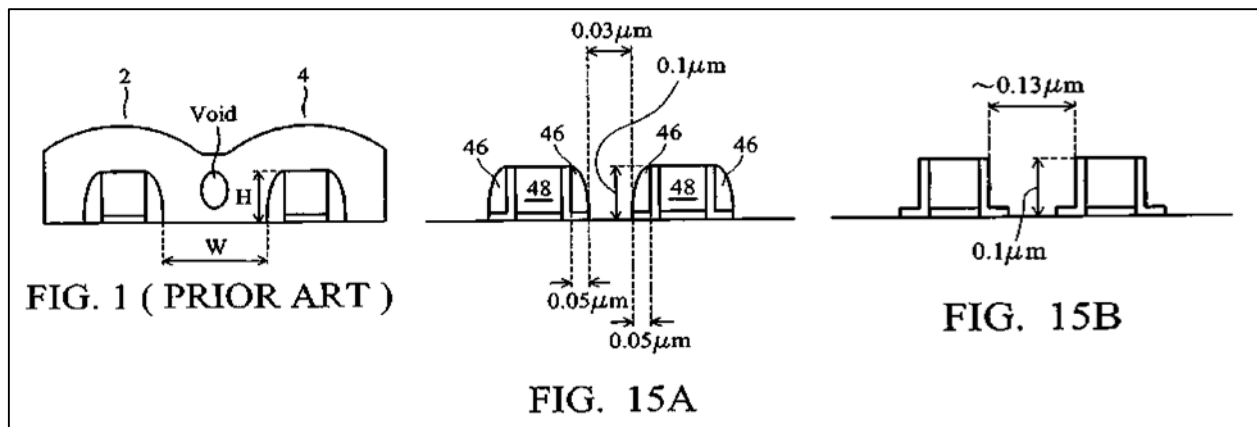
Akasaka, FIG. 26

Each PMISFET 301A and NMISFET 301B includes a gate dielectric 315 (e.g., HfSi_xO_y). *Id.*, ¶75. Over the gate dielectric, the PMISFET and NMISFET gate electrodes comprise conductive films 319 and 320. *Id.*, ¶¶84-86. The PMISFET gate electrode additionally comprises conductive film 316. *Id.*, ¶¶76-77. Silicon nitride film 312 and inter-level insulating film 313 fill the spaces between MISFETs. *Id.*, ¶73; Ex.1101, ¶¶128-130.

C. Hsu823 (Ex.1006)

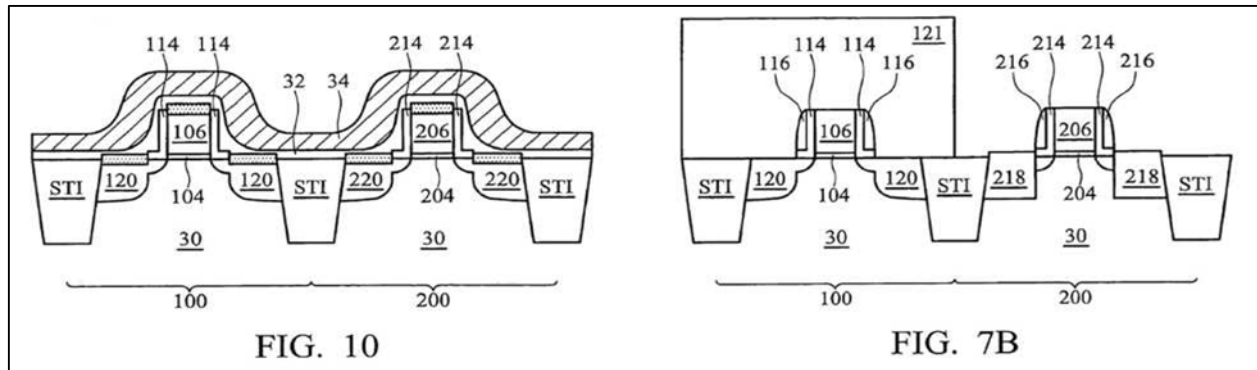
Hsu823 is prior art under pre-AIA §§102(a) and (e). Because Hsu823 is in the same field (MISFETs) and reasonably pertinent to a problem the '686 patent addresses (straining MISFET channels), Hsu823 also is analogous art. Ex.1101, ¶123.

Hsu823 explains that “[w]hen devices become smaller, the distance between devices decreases,” which leads to a “gap-filling problem” (voiding). Ex.1006, ¶4. To address this, Hsu823 teaches an L-shaped silicon oxide spacer liner and a silicon nitride spacer. *Id.*, ¶¶31, 35, FIGS. 6, 15A (below, center). After using the silicon nitride spacer to define source/drain regions, the outer spacer may be removed, leaving only the L-shaped spacer liner. *Id.*, ¶35, FIGS. 9, 15B (below, right). This way, “gap-filling is improved and the contact etching process can be better controlled.” *Id.*, ¶43; Ex.1101, ¶124.



Hsu823, FIGS. 1, 15A, 15B

Hsu823 discloses MISFET structures like the one on the left below. Ex.1006, FIG. 10. According to Hsu823, layer 32 may be omitted so that CESL 34 directly contacts L-shaped spacer liners 114/214. *Id.*, ¶¶15, 36, FIGS. 9-10, 14. CESL 34 may exert tensile stress. *Id.*, ¶¶36-37.



Hsu823, FIGS. 10, 7B

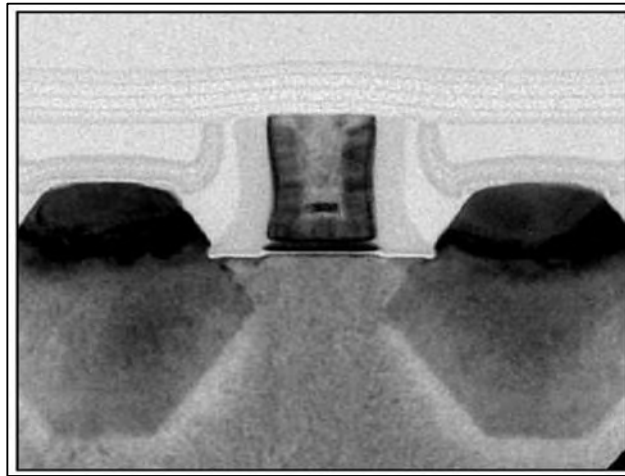
Moreover, PMOS source/drain regions (220, *see id.*, FIG. 10 (above, left)) may be formed using epitaxial SiGe (218, *see id.*, FIG. 7 (above, right)). *Id.*, ¶33, FIG. 7B. In this technique, recess etching in the source/drain regions forms trenches in which epitaxial SiGe grows. *Id.* “This introduces compressive stresses in the respective channel regions of the resulting PMOS devices, and the device drive currents of the respective PMOS devices are increased.” *Id.*, ¶33; Ex.1101, ¶¶125-26.

VI. GROUND I: Aoyama and Hsu823 Render Obvious Claims 25-28, 31, and 35

A. A POSITA would have found it obvious to implement SiGe stressors in Aoyama’s source/drain regions

SiGe stressors were known and used to improve three generations of mass-production devices before the application for the ’686 patent; it was standard

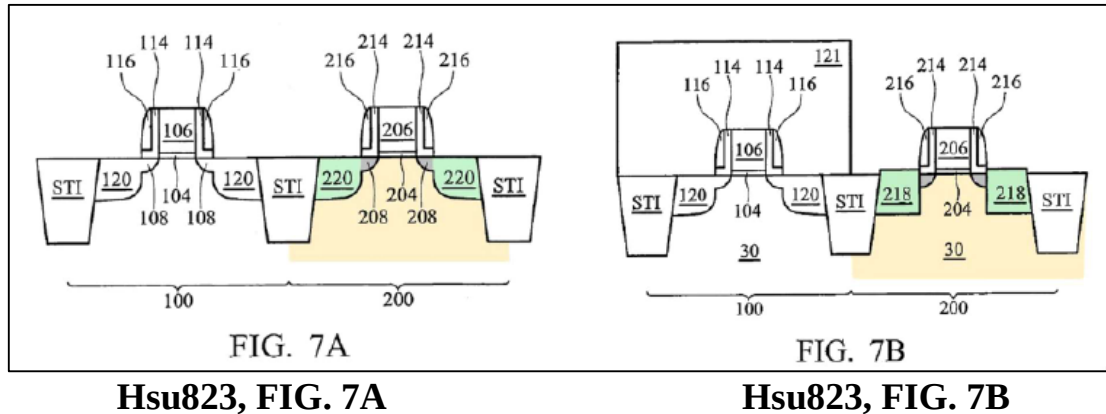
industry practice and well-known. *Supra* §IV.A.4; Ex.1101, ¶133; Ex.1538, 6:27-31. In fact, Intel had publicly described its 45nm process, which was like Aoyama’s process but with epitaxial SiGe added to the PMOSFETs (*see below*). Ex.1516, Fig. 6 (below); Ex.1517, 14-28; Ex.1101, ¶¶133-146. This alone confirms the obviousness of the asserted combination. Ex.1101, ¶146.



Ex.1516, Fig. 6

Further, Hsu823 likewise discloses⁴ epitaxial “SiGe stressors 218” grown in trenches to compressively stress the channel. Ex.1006, ¶33. The image on the left below illustrates source/drain regions 220 “formed by implanting impurities,” as in Aoyama. *Id.*, ¶32, FIG. 7A. The image on the right below illustrates another approach—“epitaxially grown” SiGe stressors 218. *Id.*, ¶¶32-33.

⁴ As used herein, a reference “discloses” what it teaches, suggests, or at least renders obvious.



A POSITA would have found it obvious to modify Aoyama's PMOSFET by replacing PMOSFET source/drain regions 112 with epitaxial SiGe stressors, as taught by Hsu823. Ex.1006, ¶¶32-33, FIGS. 7A-7B; Ex.1101, ¶148. A POSITA would have been motivated to do so since SiGe stressors were known to increase hole mobility, thereby boosting drive current and operating speed. *Supra* §IV.A.4; Ex.1006, ¶¶2-3, 33; Ex.1101, ¶149. And a POSITA would have reasonably expected to succeed because such SiGe layers were known and widely used to induce compressive stress in PMOSFETs. *Supra* §IV.A.4; Ex.1101, ¶150.

The structure in Aoyama's FIG. 6I is materially the same as the structure in Hsu823's FIG. 7A. Ex.1101, ¶151; *see* Ex.1005, ¶¶103-111, FIG. 6I; Ex.1006, ¶¶28-32, FIG. 7A. Hsu823 teaches that SiGe source/drain regions may be readily integrated into such a structure to boost PMOS performance. Ex.1006, ¶¶32-33; Ex.1101, ¶151. Thus, as Figure A below shows, a POSITA would have known the process steps Hsu823 describes regarding Figure 7B readily integrate into Aoyama's

process at FIG. 6I with the ordinary and expected result of boosted PMOSFET performance. Ex.1006, ¶33; *supra* §IV.A.4; Ex.1101, ¶151.

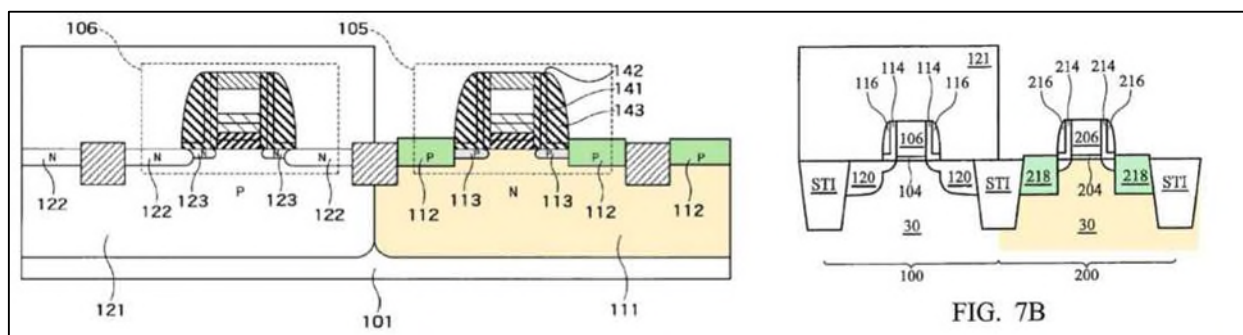


Figure A (Aoyama, FIG. 6I, modified)

Hsu823, Fig. 7B

Figure B below illustrates Aoyama's FIG. 5, modified to include such SiGe stressors. Ex.1101, ¶152; Ex.1006, ¶33, FIG. 7B; Ex.1005, FIG. 5; Ex.1538, 6:27-31, FIGS. 3-10; Ex.1516, Fig. 6; Ex.1517, 14-28.

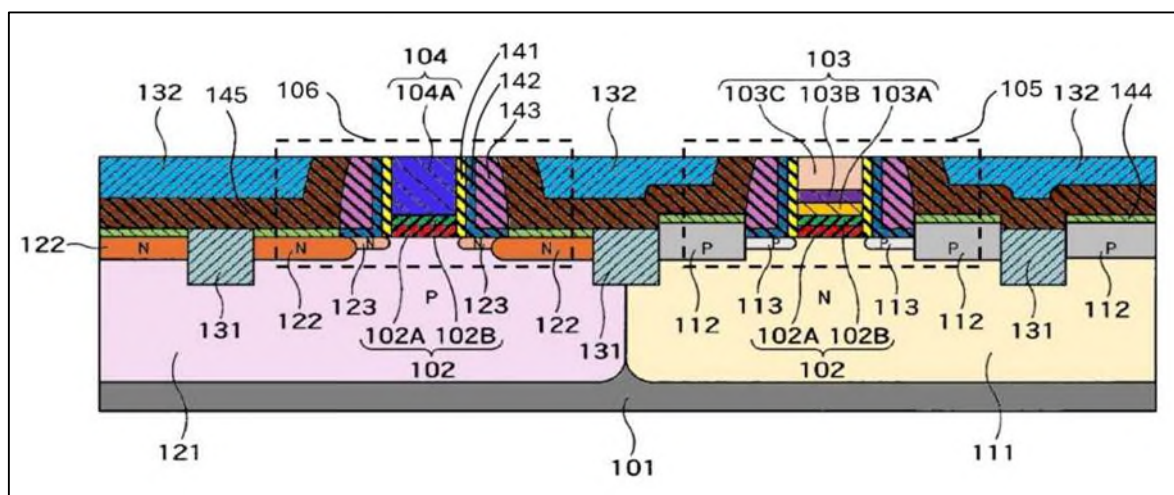
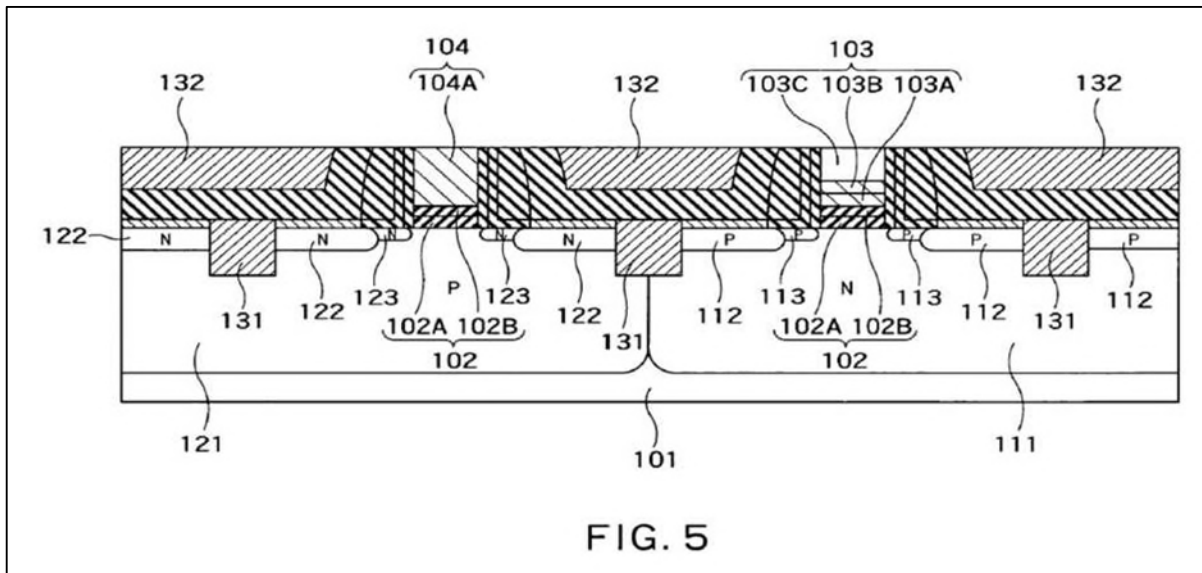


Figure B (Aoyama, FIG. 5, modified)

1. Independent Claim 25

a. 25[Pre]

Aoyama discloses “a *semiconductor device*”⁵: “The present invention relates to a **semiconductor device**....”⁶ Ex.1005, ¶3; *see id.*, ¶97, FIG. 5 (below); Ex.1101, ¶153.



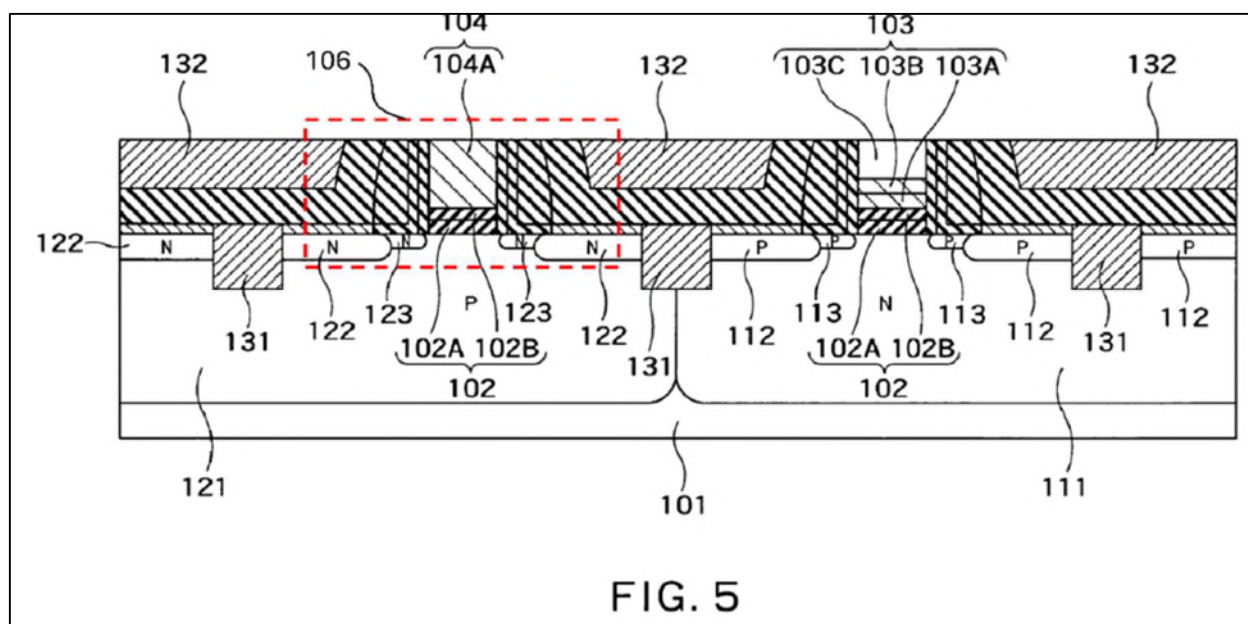
Aoyama, FIG. 5

b. 25[a]

Aoyama discloses “a *first MIS transistor*”: an “NMOSFET” (106). Aoyama, ¶106, FIG. 5 (below); Ex.1101, ¶¶155-56.

⁵ Claim language is indicated by italics throughout.

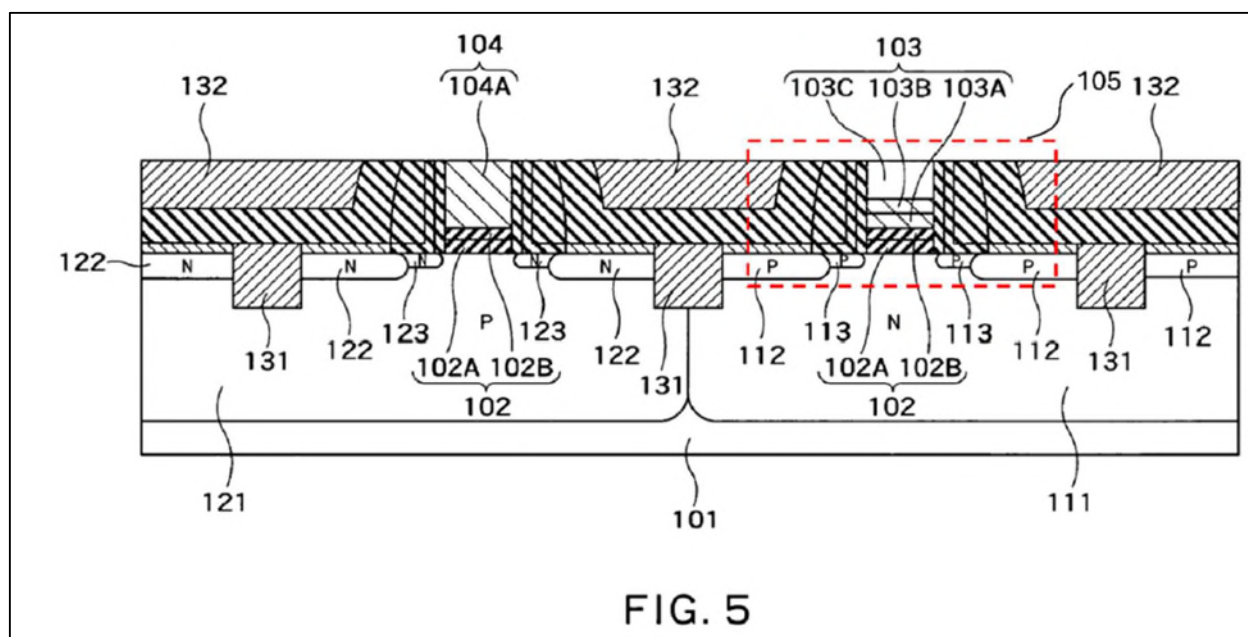
⁶ Unless otherwise noted, all emphasis added.



Aoyama, FIG. 5

c. 25[b]

Aoyama discloses “*a second MIS transistor*”: a “PMOSFET” (105). Ex.1005, ¶106, FIG. 5 (below); Ex.1101, ¶¶157-58.



Aoyama, FIG. 5

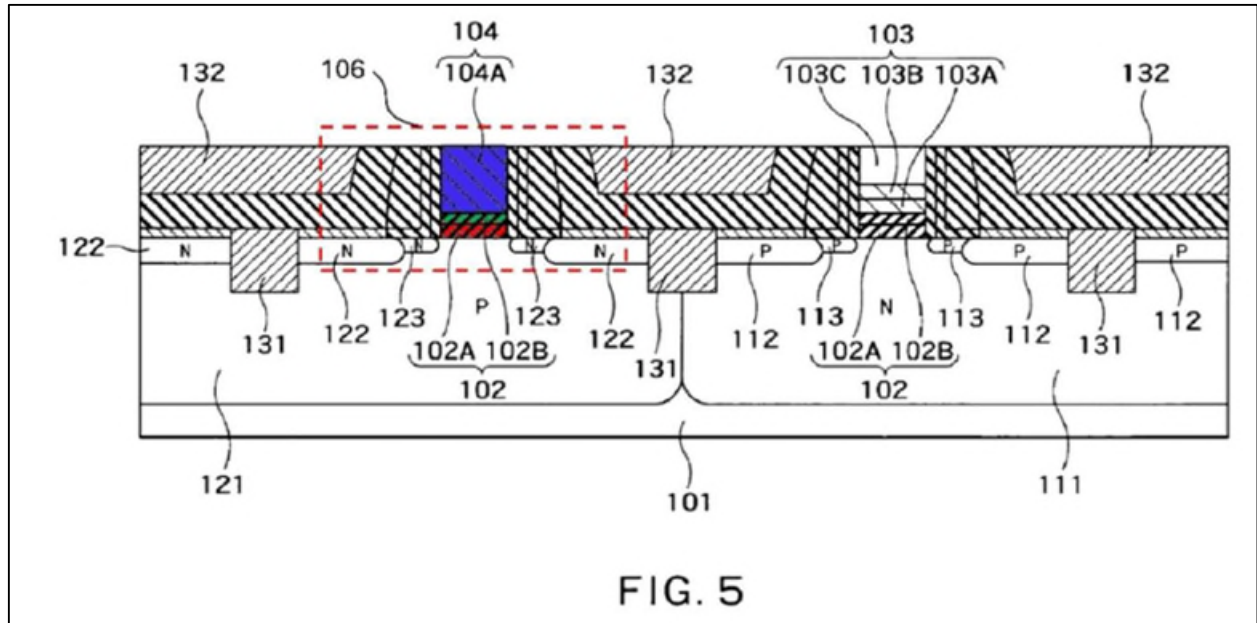
d. 25[c] and 25[g]

Aoyama discloses a “*first gate insulating film*” and a “*second gate insulating film*.” Ex.1101, ¶¶159-164. Because Aoyama discloses a gate insulating film 102 identical to the ’686 Patent, Aoyama necessarily discloses both the claimed “*first gate insulating film*” and “*second gate insulating film*.” Ex.1101, ¶159; compare Ex.1001, 11:25-37, 29:16-24, with Ex.1005, ¶106 (identical silicon oxide and hafnium silicate films). Specifically, gate dielectric film 102 (including 102A and 102B) discloses the claimed “*first gate insulating film*” in NMOSFET region 106 and “*second gate insulating film*” in PMOSFET region 105. Ex.1101, ¶¶160-62.

Alternatively, if part of a gate dielectric film structure may constitute a “gate insulating film,” either gate dielectric film 102A or 102B alone discloses the claimed “*first gate insulating film*” in NMOSFET region 106, and either gate dielectric film 102A or 102B alone discloses the claimed “*second gate insulating film*” in PMOSFET region 105. Ex.1101, ¶163.

e. 25[d]

Aoyama discloses the “*first MIS transistor*” includes “*a first gate electrode including a second metal film formed on the first gate insulating film*.” Ex.1101, ¶¶165-66. Aoyama discloses a “gate electrode 104” (first gate electrode) including a “conductive layer 104A which is made of conductive metal” (second metal film) formed on the first gate insulating film. Ex.1005, ¶98, FIG. 5 (below).

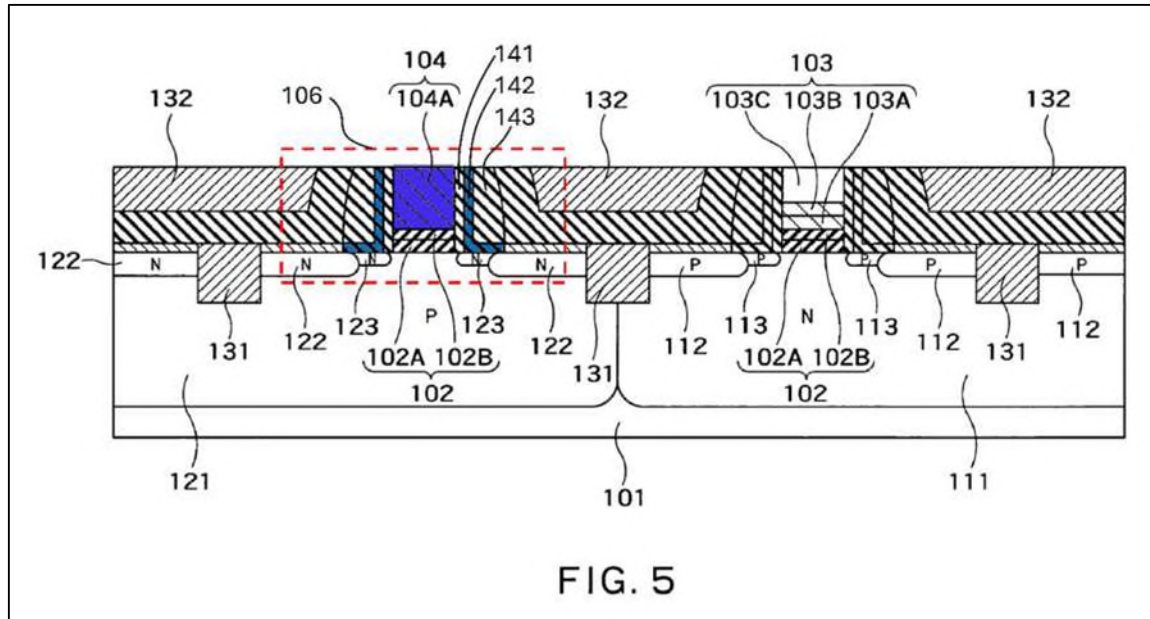


Aoyama, FIG. 5

f. 25[e]

Aoyama discloses the “*first MIS transistor*” includes “*first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative.*” Ex.1101, ¶¶167-69. Aoyama discloses “side wall spacer[s] 142” (first sidewall spacers) “made of a silicon oxide film,” which is insulative.⁷ Ex.1005, ¶111; Ex.1101, ¶168. As FIG. 5 below shows, the first sidewall spacers are formed on side surfaces of the first gate electrode (gate electrode 104).

⁷ Alternatively, Aoyama’s offset spacers 141 and sidewall spacers 142, collectively, disclose the “first sidewall spacers.” Ex.1005, ¶111. Both are “made of a silicon oxide film.” *Id.*



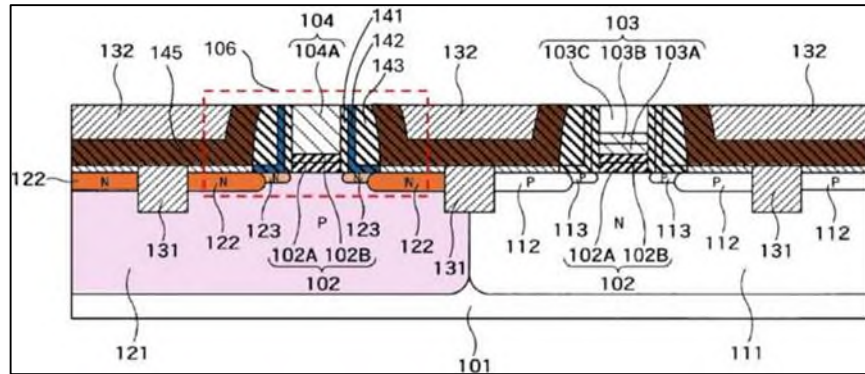
Aoyama, FIG. 5

g. 25[f]

Aoyama discloses the “first MIS transistor” includes “a silicon nitride film [etch stopper film 145] formed, extending over the side surfaces of the first gate electrode [gate electrode 104] on which the first sidewall spacers [sidewall spacers 142⁸] are formed and upper surfaces of regions [source/drain layers 122] located in the first active region [NMOSFET region 106] laterally outside the first sidewall spacers,” as FIG. 5 below shows. Ex.1101, ¶170-73; Ex.1005, ¶¶100 (disclosing “source/drain diffusion layer 122 for the NMOSFET”), 113 (“[A] silicon nitride film

⁸ Alternatively, Aoyama’s offset spacers 141 and sidewall spacers 142, collectively, disclose the “first sidewall spacers.” Ex.1005, ¶111. Both are “made of a silicon oxide film.” *Id.*

[145] is formed over the entire surface.”). Etch stopper film 145 is “formed over the entire surface,” then “planarized by chemical mechanical polishing or etching” to expose the metal gate electrodes. Ex.1005, ¶113; *see id.* ¶¶114-119, FIGS. 6K-6Q.



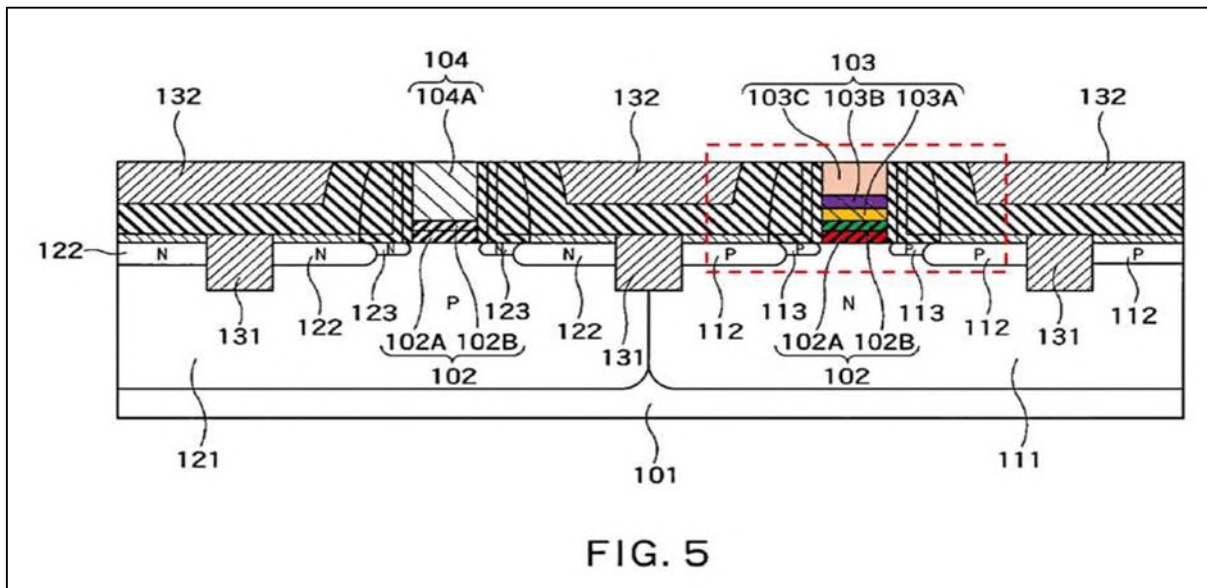
Aoyama, FIG. 5

h. 25[h]

Aoyama discloses the “second MIS transistor” includes “a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film.” Ex.1101, ¶¶174-79. Aoyama discloses a “gate electrode 103” (second gate electrode) including a “conductive layer 103B ... made of conductive metal” (first metal film) formed on the second gate insulating film. Ex.1005, ¶98, FIG. 5 (below). Aoyama further discloses a “semiconductor layer (silicide layer) 103C” formed on the first metal film (layer 103B). *Id.*, ¶121.

Like the ’686 patent, semiconductor layer (silicide layer) 103C comprises a “polysilicon or amorphous silicon” layer and a “Ni monosilicide (NiSi)” layer. *Compare* Ex.1005, ¶¶107, 114, with Ex.1001, 11:50-67, 29:41-45, 21:30-35, FIG.

8C (layers 15b and 34). Either or both parts of Aoyama's layer 103C constitutes the claimed "conductive film." Ex.1005, ¶121 ("[G]ate electrode 103 for the PMOSFET includes ... semiconductor layer (silicide layer) 103C made of the semiconductor (silicide). **For this reason**, in the third embodiment, **the gate resistance of the PMOSFET is relatively low**" (emphasis added)); Ex.1101, ¶178.

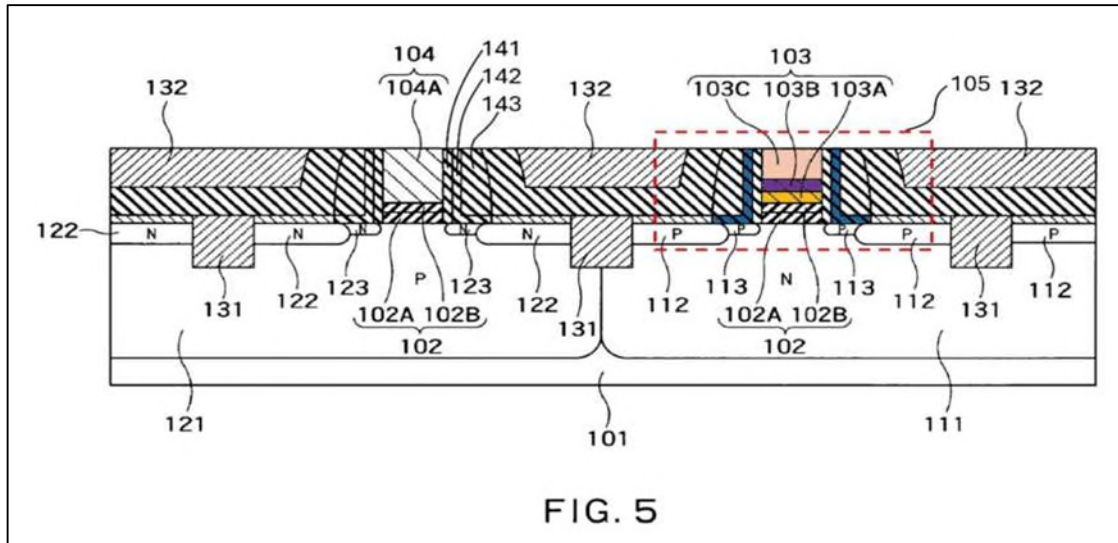


Aoyama, FIG. 5

i. 25[i]

Aoyama discloses the "second MIS transistor" includes "second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative." Ex.1101, ¶¶180-82. Aoyama discloses "side wall spacer[s] 142" (second sidewall spacers) "made of a silicon oxide film," which is

insulative.⁹ Ex.1005, ¶111; Ex.1101, ¶181. As FIG. 5 below shows, these second sidewall spacers (blue) are formed on side surfaces of the second gate electrode (gate electrode 103).



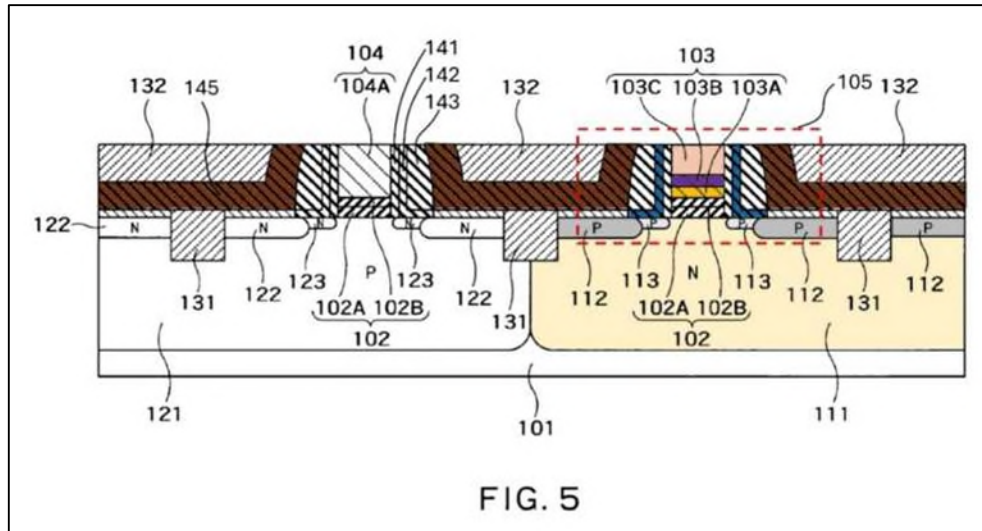
Aoyama, FIG. 5

j. 25[j]

Aoyama discloses the “second MIS transistor” includes “the silicon nitride film [etch stopper film 145] formed, extending over the side surfaces of the second gate electrode [gate electrode 103] on which the second sidewall spacers [sidewall spacers 142] are formed and upper surfaces of regions [source/drain layers 112] located in the second active region [PMOSFET region 105] laterally outside the

⁹ Alternatively, Aoyama’s offset spacers 141 and sidewall spacers 142, collectively, disclose the “second sidewall spacers.” Ex.1005, ¶111. Both are “made of a silicon oxide film.” *Id.*

second sidewall spacers,” as FIG. 5 below shows. Ex.1005, ¶¶99 (disclosing “source/drain diffusion layer 112 for the PMOSFET”), 113 (“[A] silicon nitride film [145] is formed over the entire surface.”); Ex.1101, ¶¶183-87.



Aoyama, FIG. 5

k. 25[k]

Aoyama discloses “*the first and second metal films are made of different metal materials.*” Ex.1101, ¶¶188-190. Conductive layer 104A (second metal film) is TaCN, and conductive layer 103B (first metal film) is TiN. Ex.1005, ¶¶107, 118.

l. 25[l]

Aoyama discloses “*the silicon nitride film [etch stopper film 145] is not formed on any of upper surfaces of the first and second gate electrodes.*” Ex.1101, ¶¶191-94. Etch stopper film 145 is “formed over the entire surface” and “planarized” so “semiconductor layer[] 103C ... [is] exposed both in the PMOSFET region 105 and the NMOSFET region 106.” Ex.1005, ¶113; see *id.*, ¶¶114-119, FIGS. 6K-6Q.

enhanced through a stressed-surface channel.” *Id.*, ¶2; *see id.*, ¶3 (“[A] bi-axial, in-plane tensile stress field can improve NMOS performance.”). “A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device.” *Id.*, ¶3; *see* Ex.1528, 1-2; Ex.1531, ¶3; Ex.1529, ¶90.

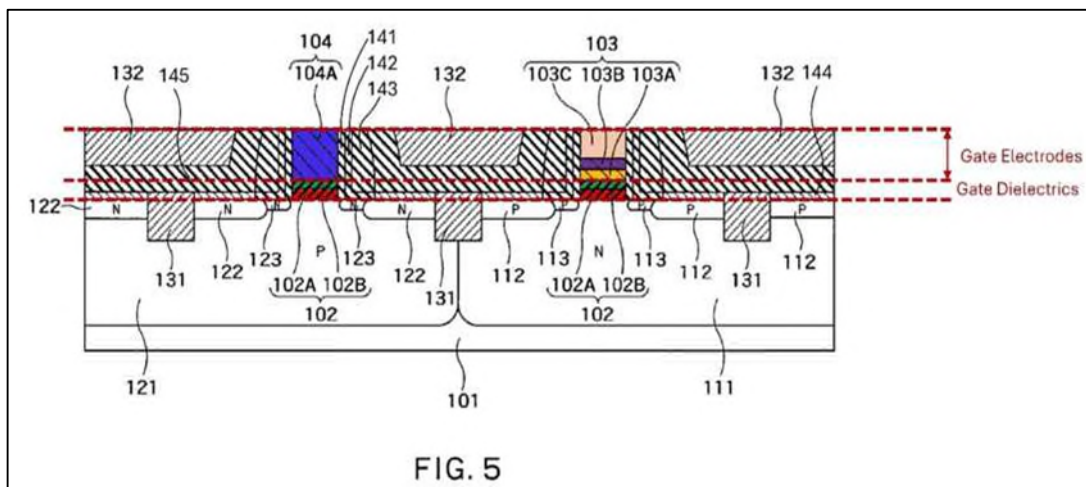
A POSITA would have selected Aoyama’s etch stopper layer 145 as a tensile etch stop layer for both PMOSFET and NMOSFET devices, which was well-known in the art, because it provides improved NMOSFET electron mobility. *Supra* IV.A.4; Ex.1006, ¶¶37-39, FIG. 10; Ex.1527, ¶¶38-39, FIG. 6; Ex.1528, 1-2; Ex.1530, 1-2; Ex.1523, Fig. 5(c); Ex.1101, ¶197.

A POSITA would have reasonably expected to succeed in implementing a tensile etch stopper film 145 because such tensile CESL films were widely used to improve carrier mobility in NMOSFET devices. *Supra* IV.A.4; Ex.1101, ¶199. It would have been well within a POSITA’s ability to create such a tensile silicon nitride CESL film simply by adjusting deposition conditions. Ex.1529, ¶¶90, 99-100, TBL. V; Ex.1101, ¶199.

2. Claim 26

Aoyama discloses “*wherein the first metal film [conductive layer 103B] has a thickness smaller than that of the second metal film [conductive layer 104A].*” Ex.1101, ¶¶202-08. Because both gate structures are planarized after forming

conductive layer 104A (Ex.1005, ¶119, FIG. 6Q), and gate electrodes 103 and 104 are both formed on gate dielectric film 102, gate electrodes 103 (layers 103A-103C, collectively) and 104 (layer 104A) have the same thickness. See Ex.1005, FIG. 5 (below); Ex.1101, ¶203. Accordingly, conductive layer 103B must be thinner than conductive layer 104A, as shown. Ex.1101, ¶203; see Ex.1005, ¶¶114-119, FIGS. 6G-6Q.



Aoyama, FIG. 5

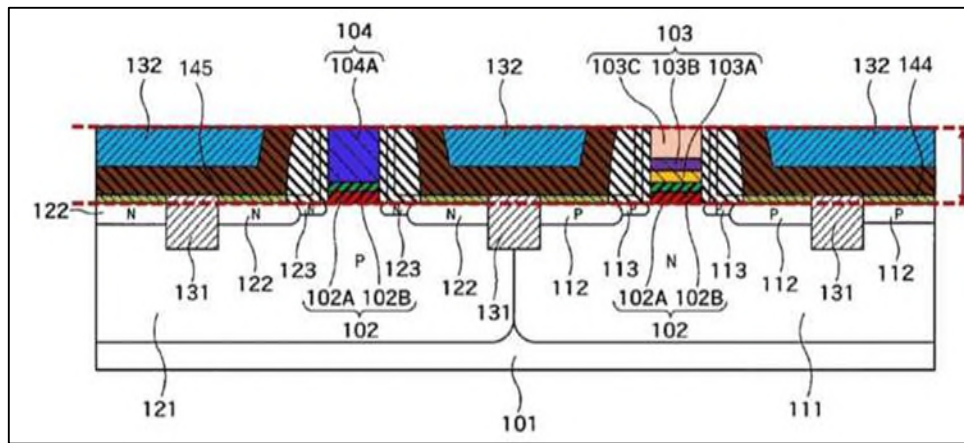
3. Claim 27

Aoyama discloses “wherein the first and second metal films have different work functions.” Ex.1101, ¶¶209-13. Conductive layer 104A (second metal film) is TaCN and conductive layer 103B (first metal film) is TiN. Ex.1005, ¶¶107, 118. The work functions of TaCN (e.g., 4.3 eV or less) and TiN (e.g., 5.1 eV) differ. Ex.1101, ¶212; see Ex.1005, ¶10; Ex.1533, 2; Ex.1008, ¶¶46, 77.

4. Claim 28

Aoyama discloses “silicon nitride film [etch stopper film 145] has a thickness

smaller than that of the first gate electrode [gate electrode 104].” Ex.1101, ¶214-34. Aoyama’s FIG. 5 below shows etch stopper film 145 much thinner than gate electrode 104. *See Koito Mfg. Co. v. Turn-Key-Tech, LLC*, 381 F.3d 1142, 1154-56 (Fed. Cir. 2004) (finding “relative dimensions” of a patent figure alone disclosed a claim limitation reciting one feature “significantly thicker and wider” than another); Ex.1101, ¶214.



Aoyama, FIG. 5

For at least four additional reasons, a POSITA also would have found claim 28 obvious. Ex.1101, ¶217.

First, Aoyama’s gate electrodes 103 and 104 are planarized. Ex.1005, ¶119, FIG. 6Q. As the red arrow above in FIG. 5 indicates, the collective thickness of etch stopper film 145 and interlayer dielectric 132 cannot exceed the gate height. Thus, even when improperly ignoring silicide film 144, etch stopper film 145 will be thinner than gate electrode 104 so long as interlayer dielectric 132 is thicker than gate dielectric film 102. Ex.1101, ¶¶218-20.

A POSITA would have expected Aoyama's interlayer dielectric 132 to be thicker than gate dielectric film 102. Ex.1101, ¶221; see Ex.1534, ¶¶317 (120 nm gate electrode), 326 (30 nm CESL & 250 nm ILD planarized to about 90 nm), FIG. 52. A POSITA would have known the thickness of a gate dielectric is negligible compared to a gate electrode. Ex.1101, ¶222; see Ex.1525, Figs. 1-3, 5-6, 8-12; Ex.1516, Fig. 6; Ex.1517, 25; Ex.1523, Fig. 2; Ex.1528, Fig. 1. The gate dielectric is famously very thin to maximize capacitance. Ex.1101, ¶222; see Ex.1511, 8. Aoyama's gate dielectric film 102 is less than 3 nm thick—only several atomic layers. Ex.1005, ¶106; Ex.1101, ¶223. Interlayer dielectrics, on the other hand, require low capacitance and are much thicker: “gate and interlayer (ILD) dielectric films” have “opposing requirements” in that regard. Ex.1511, 8; see Ex.1101, ¶223. This renders claim 28 borderline inherent and certainly obvious.

Second, when “there are a finite number of identified, predictable solutions, a [POSITA] has good reason to pursue the known options within his or her technical grasp.” *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007). Given Aoyama's planarization, a POSITA would have recognized a design need to form etch stopper film 145 and inter-layer dielectric film 132 in a limited space between the substrate surface and the top of gate electrode 104. Ex.1101, ¶226. There are only two “identified, predictable solutions”: etch stopper 145 is thinner than the first gate

electrode, or it is not.¹⁰ See *Uber Techs., Inc. v. X One, Inc.*, 957 F.3d 1334, 1339 (Fed. Cir. 2020) (holding two is a “finite number of identified, predictable solutions”); *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1331 (Fed. Cir. 2009) (same for three). Of those options, a silicon nitride CESL thinner than the gate electrode was known (in fact, expected) and therefore within the technical grasp of a POSITA and obvious. Ex.1101, ¶¶226-28; Ex.1516, Fig. 6; Ex.1517, 16; Ex.1525, Figs. 1-3, 5-6, 8-12; Ex.1528, Fig. 1; Ex.1523, Fig. 2.

Third, gate electrode 104 is thicker than 80 nm. Ex.1101, ¶229. Planarization makes gate electrodes 103 and 104 the same thickness. Ex.1005, ¶119, Fig. 6Q; Ex.1101, ¶229. Conductive layer 103A is about 20 nm, and conductive layer 103B is about 60 nm, meaning gate electrode 103 (which further includes layer 103C) is thicker than 80 nm. Ex.1005, ¶107; Ex.1101, ¶230. A POSITA would have understood that silicon nitride etch stopper films like Aoyama’s “ha[d] a typical thickness of 20 nm” or so—much less than Aoyama’s gate electrode 104. Ex.1535, 1; see Ex.1534, ¶¶317, 326, FIG. 52; Ex.1101, ¶231. A POSITA thus would have found it obvious to make stopper film 145 thinner than gate electrode 104. See *Pfizer Inc. v. Sanofi Pasteur Inc.*, 94 F.4th 1341, 1348 (Fed. Cir. 2024) (finding

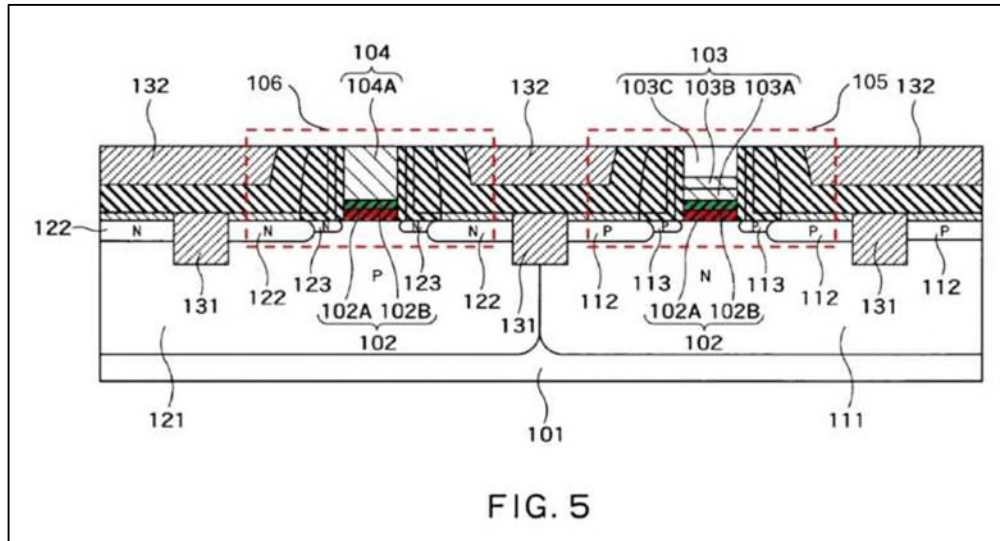
¹⁰ At most, there are three options (thicker, thinner, or equal thickness), which is immaterial here.

obviousness where “techniques and conditions were routine such that a [POSITA] would have understood the claimed [property] to be ‘typical’”).

Fourth, where claimed “dimensions were known to be result-effective variables,” “it is not inventive to discover the optimum or workable ranges by routine experimentation.” *In re Applied Materials*, 692 F.3d 1289, 1295 (Fed. Cir. 2012) (quoted source omitted). Such dimensions are only patentable if they produce a “new and unexpected result” that differs in kind, not degree, from the prior art. *Id.* at 1297; *see In re Geisler*, 116 F.3d 1465, 1469-70 (Fed. Cir. 1997). Here, silicon nitride CESL thickness was known to affect stress. *See generally* Ex.1535; Ex.1101, ¶232. Implementing etch stopper film 145 to be thinner than gate electrode 104, as claimed, would have yielded no unexpected results, as the relationship between silicon nitride thickness and stress was known and predictable. *See generally* Ex.1535; Ex.1101, ¶233.

5. Claim 31

Because Aoyama discloses a gate insulating film 102 identical to the ’686 patent, Aoyama necessarily discloses “*the first and second gate insulating films are made of the same insulating material.*” Ex.1101, ¶¶235-37. Aoyama’s gate dielectric film 102 in PMOSFET region 105 is made from the same silicon oxide dielectric film 102A and hafnium silicon oxynitride dielectric film 102B as gate dielectric film 102 in NMOSFET region 106. Ex.1005, ¶¶106, 109, FIG. 5 (below); Ex.1101, ¶236.



Aoyama, FIG. 5

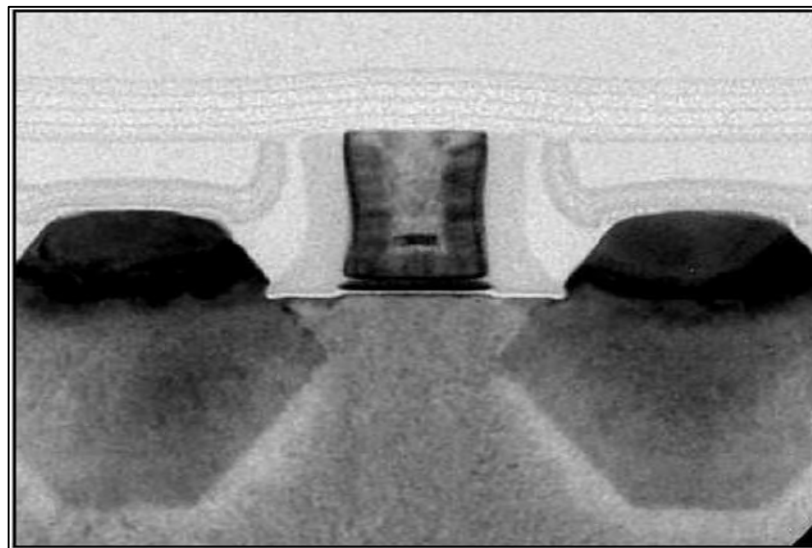
6. Claim 35

Aoyama’s “first and second gate insulating films” both “include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more”—dielectric film 102B. Ex.1101, ¶238-42. Dielectric film 102B is a “high-permittivity [high-k] dielectric film” made of “hafnium silicon oxynitride.” Ex.1005, ¶¶98, 106. According to the ’686 patent, this is “a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.” Ex.1101, ¶240; see Ex.1514, ¶4 (explaining “HfSiO_x ... and oxynitrides thereof” have “dielectricity of more than ten”); Ex.1511, 8; Ex.1515, ¶¶2, 8.

VII. GROUND II: Akasaka and Hsu823 Render Obvious Claims 25-28, 31, and 35

A. A POSITA would have found it obvious to implement SiGe stressors in Akasaka's source/drain regions

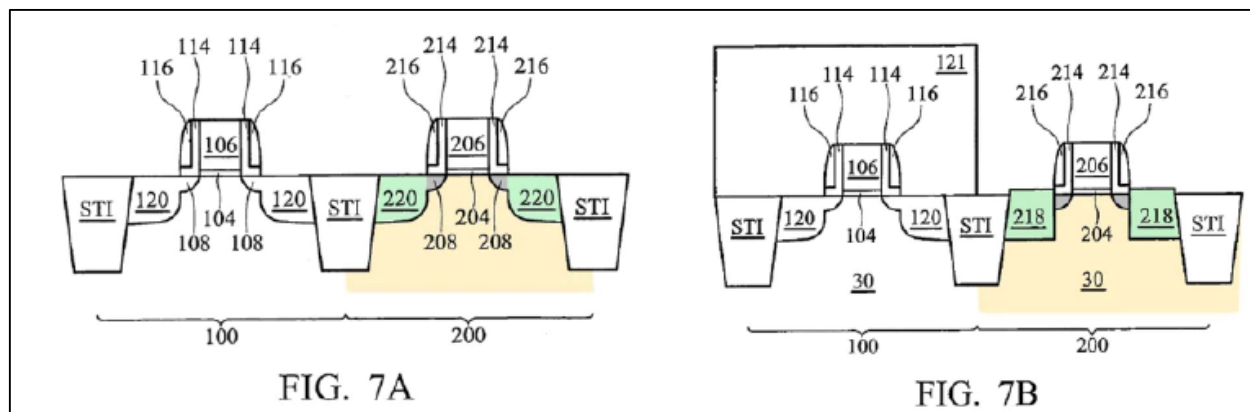
SiGe stressors had been known and used to improve PMOS performance in three generations of mass-production devices before the '686 patent; it was standard industry practice and well-known. *Supra* IV.A.4; Ex.1101, ¶¶244-45; Ex.1538, 6:27-31. In fact, Intel had publicly described the process flow for its 45nm process, which was like Akasaka's process but with epitaxial SiGe added to the PMISFETs (see below). Ex.1516, Fig. 6 (below); Ex.1517, 14-28; Ex.1538, 6:27-31; Ex.1101, ¶¶245-57. This alone confirms the obviousness of the asserted combination. Ex.1101, ¶246.



Ex.1516, Fig. 6

Further, Hsu823 likewise discloses epitaxial “SiGe stressors 218” grown in trenches to compressively stress the channel. Ex.1006, ¶33. The image on the left

below illustrates source/drain regions 220 “formed by implanting impurities,” as in Akasaka. *Id.*, ¶32, FIG. 7A (below, left). The image on the right illustrates another approach—“epitaxially grown” SiGe stressors 218. *Id.*, ¶¶32-33, FIG. 7B (below, right).



Hsu823, FIG. 7A

Hsu823, FIG. 7B

A POSITA would have found it obvious to modify Akasaka’s PMISFET by using epitaxial SiGe stressors, as Hsu823 discloses, to form Akasaka’s PMISFET source/drain regions 309. Ex.1006, ¶¶32-33, FIGS. 7A-7B; Ex.1008, ¶73, FIG. 16; Ex.1101, ¶259. A POSITA would have been motivated to do so since SiGe stressors were known to increase hole mobility, thereby boosting drive current and operating speed. *Supra* IV.A.4; Ex.1006, ¶¶2-3, 33; Ex.1101, ¶260.

A POSITA would have reasonably expected to succeed because such SiGe layers were known and widely used to compressively stress such PMISFETs. *Supra* IV.A.4; Ex.1101, ¶260. The structure in Akasaka’s FIG. 16 is materially the same as the structure in Hsu823’s FIG. 7A. Ex.1101, ¶261; see Ex.1008, ¶¶72-73, FIG. 16;

Ex.1006, ¶¶28-32, FIG. 7A. Hsu823 teaches that SiGe source/drain regions may be readily integrated into such a structure to boost PMOS performance. Ex.1006, ¶33; Ex.1101, ¶262. Thus, as Figure C shows below, a POSITA would have known the same process steps Hsu823 describes regarding Figure 7B readily integrate into Akasaka's process at FIG. 16 with the ordinary and expected result of boosted PMISFET performance. Ex.1006, ¶33; *supra* IV.A.4; Ex.1101, ¶262.

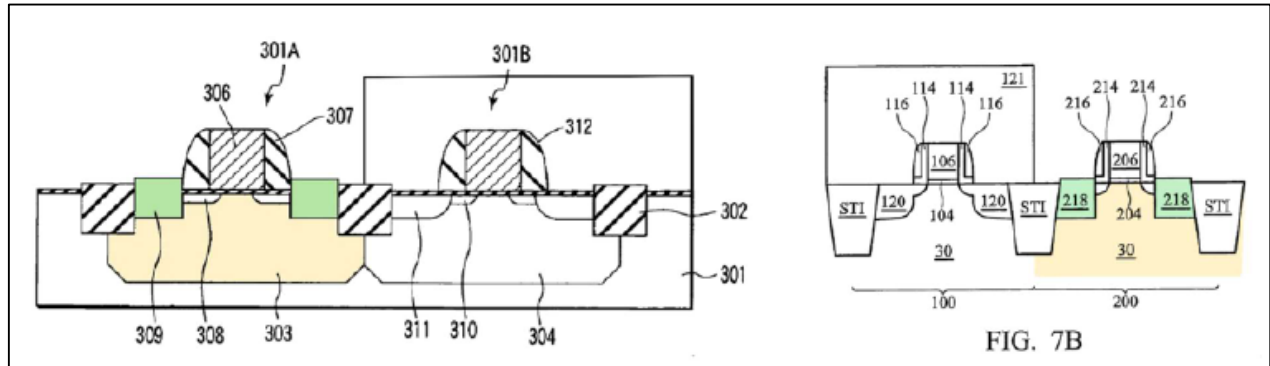


Figure C (Akasaka, FIG. 16, modified) Hsu823, Fig. 7B

Figure D illustrates Akasaka's PMISFET, modified to include SiGe stressors as Hsu823 discloses. Ex.1101, ¶263; Ex.1006, ¶33, FIG. 7B; Ex.1008, FIG. 26; Ex.1538, 6:27-31, FIGS. 3-10.

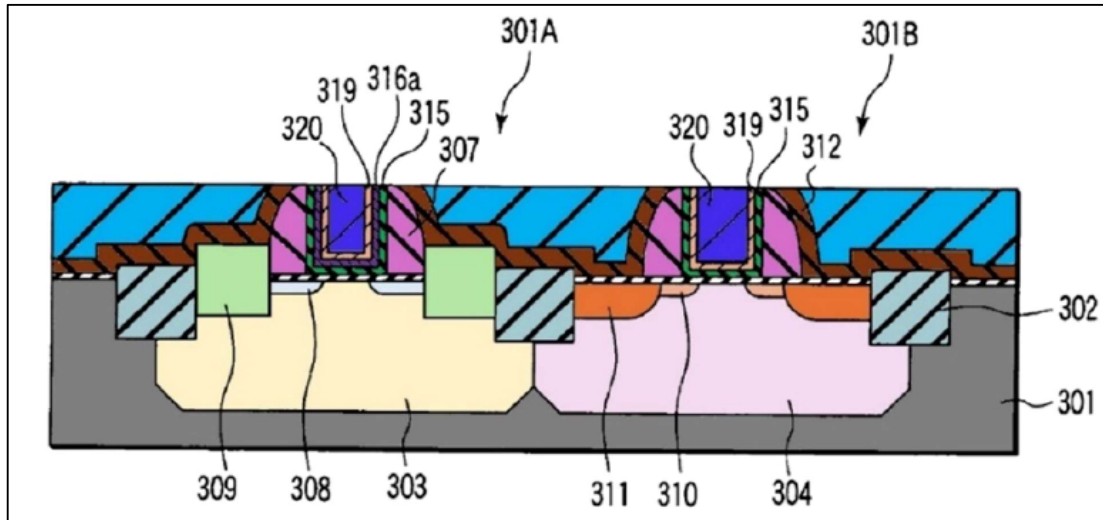
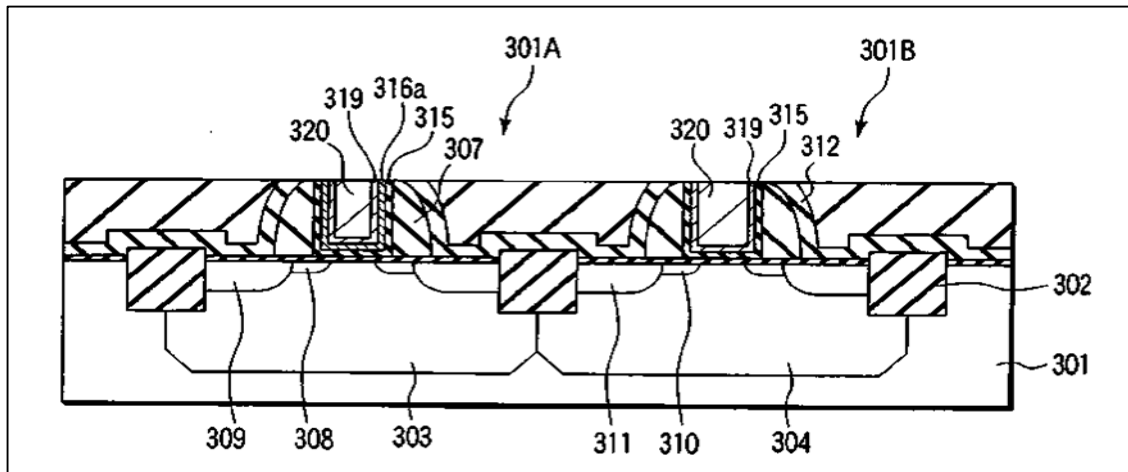


Figure D (Akasaka, FIG. 26, modified)

1. Independent Claim 25

a. 25[Pre]

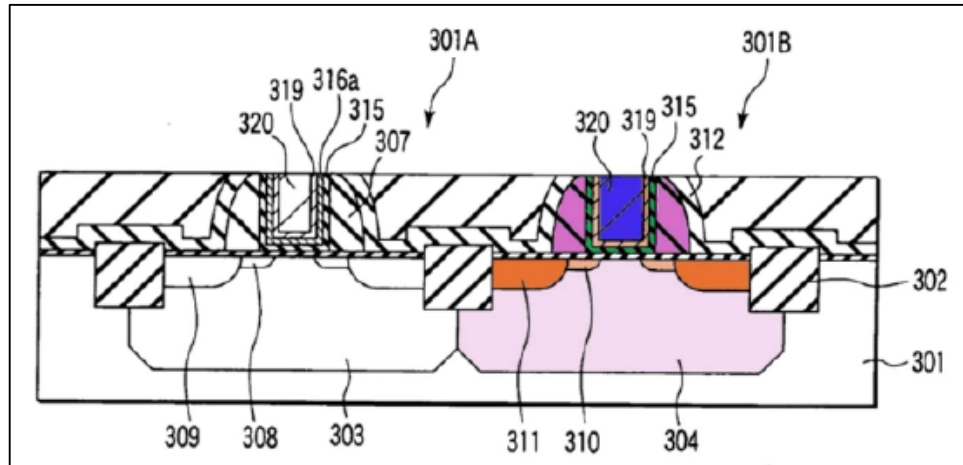
Akasaka discloses “[a] *semiconductor device*.” Ex.1008, ¶¶3, 72, FIG. 26 (below); Ex.1101, ¶¶264-65.



Akasaka, FIG. 26

b. 25[a]

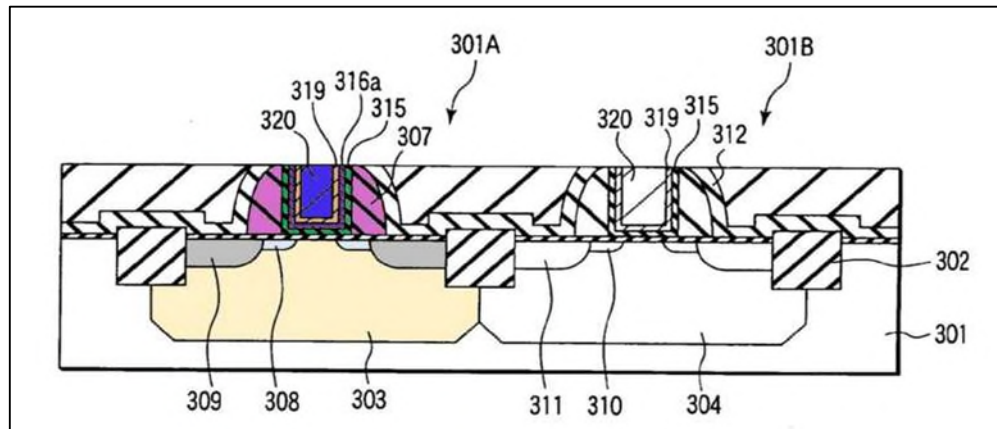
Akasaka discloses “a *first MIS transistor*”: an “n-type MISFET” (i.e., NMISFET) 301B. Ex.1008, ¶¶72-73, FIG. 26 (below); Ex.1101, ¶¶266-67.



Akasaka, FIG. 26

c. 25[b]

Akasaka discloses “a second MIS transistor”: a “p-type MISFET” (i.e., PMISFET) 301A. Ex.1008, ¶¶72-73, FIG. 26 (below); Ex.1101, ¶¶268-69.



Akasaka, FIG. 26

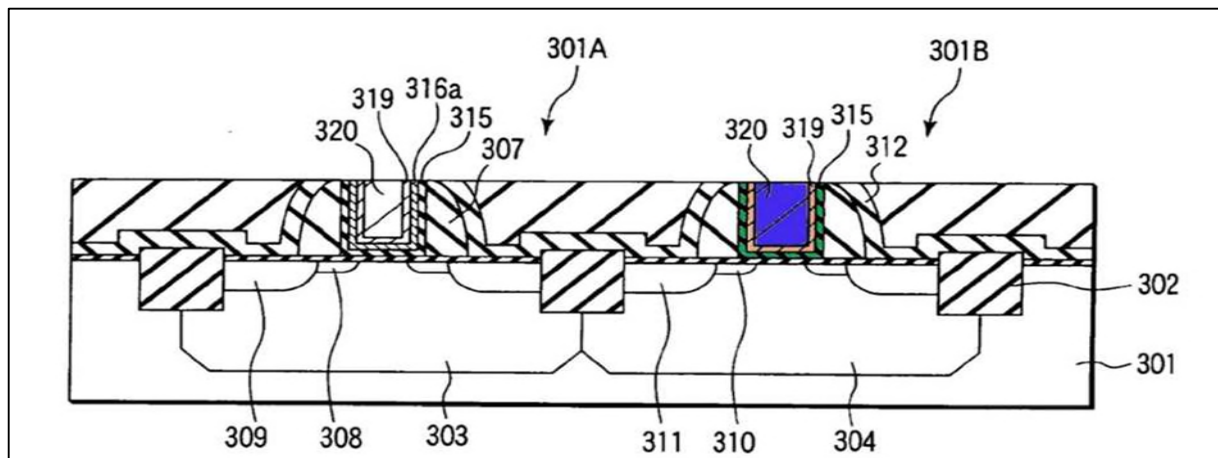
d. 25[c]

Akasaka discloses the “first MIS transistor” includes “a first gate insulating film formed on a first active region in a semiconductor substrate.” Ex.1101, ¶¶270-71. Akasaka’s gate dielectric film 315 is “depos[it]ed all over the substrate[301],” including area 301B (first active region) “for forming ... an n-type MISFET.”

Ex.1008, ¶¶72-73; *see id.*, FIG. 26 (below); Ex.1101, ¶270.

e. 25[d]

Akasaka discloses the “*first MIS transistor*” includes “*a first gate electrode including a second metal film formed on the first gate insulating film.*” Ex.1101, ¶¶272-74. Akasaka’s NMISFET gate electrode comprises conductive films 319 and 320. Ex.1008, ¶¶84-86, FIG. 26 (below). Conductive film 319 may be “a [Group-IVa, Group-Va, or Group-VIa] pure metal, ... a metal silicide, a metal nitride, or another compound ... as long as it has a metallic band structure with a work function close to that of n⁺-poly-crystalline silicon,” and conductive film 320 may be tungsten, also a metal. Ex.1008, ¶¶85-86. Either or both conductive films 319 and 320 disclose the claimed “second metal film.” Ex.1101, ¶272-73.

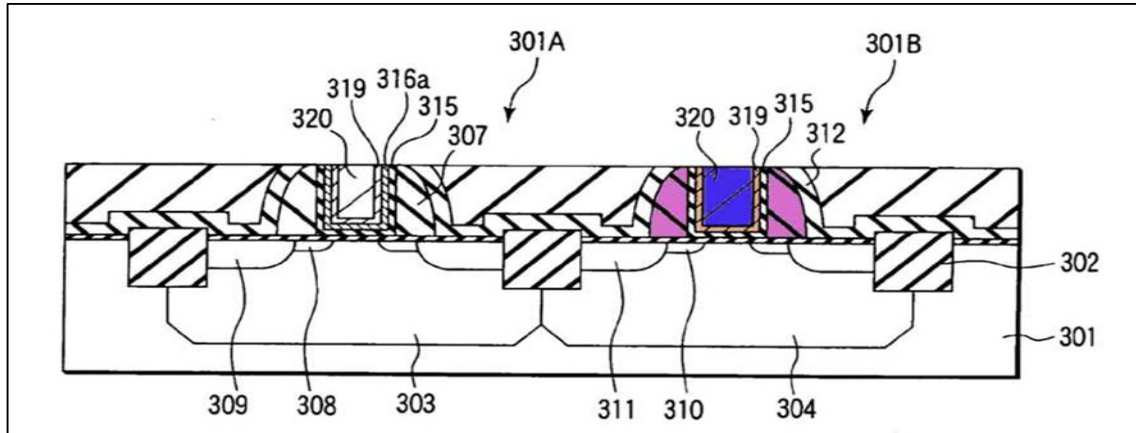


Akasaka, FIG. 26

f. 25[e]

Akasaka discloses the “*first MIS transistor*” includes “*first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being*

insulative.” Ex.1101, ¶¶275-76. Akasaka discloses “gate sidewall[s] 307” (first sidewall spacers) “formed of an insulating film, such as ... silicon nitride.” Ex.1008, ¶73. As FIG. 26 below shows, gate sidewalls 307 (pink) are formed on side surfaces of the first gate electrode. Ex.1101, ¶275.

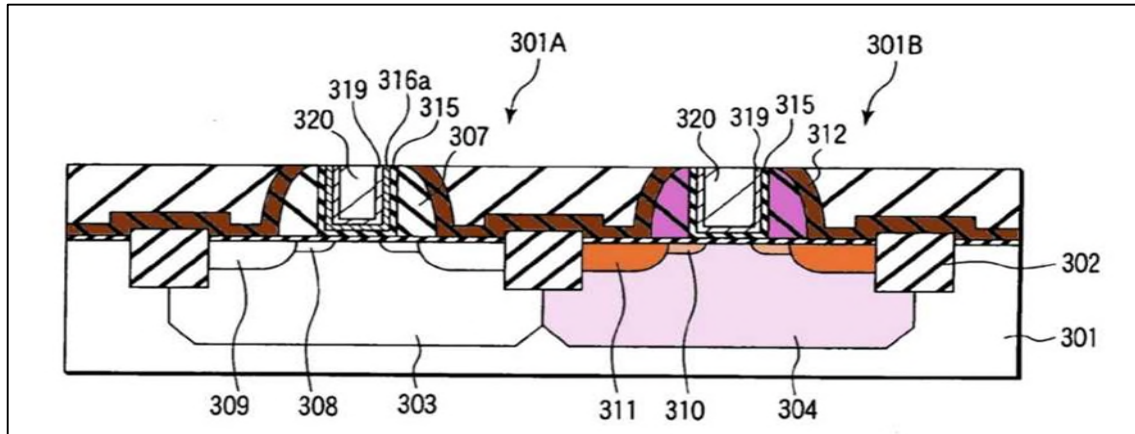


Akasaka, FIG. 26

g. 25[f]

Akasaka discloses the “*first MIS transistor*” includes “*a silicon nitride film [silicon nitride film 312] formed, extending over the side surfaces of the first gate electrode [NMISFET gate electrode] on which the first sidewall spacers [gate sidewalls 307] are formed and upper surfaces of regions [source/drain layers 311] located in the first active region [area 301B] laterally outside the first sidewall spacers,*” as FIG. 26 below shows. Ex.1008, ¶¶72-73; Ex.1101, ¶¶277-80. The gate electrode structure and its sidewalls 307 “are covered with silicon nitride film 312 serving as an etching stopper.” Ex.1008, ¶73, FIG. 16. Then, silicon nitride film 312 is polished by CMP to expose the upper surfaces of the gate electrode structures. *Id.*,

¶¶74, 87.



Akasaka, FIG. 26

h. 25[g]

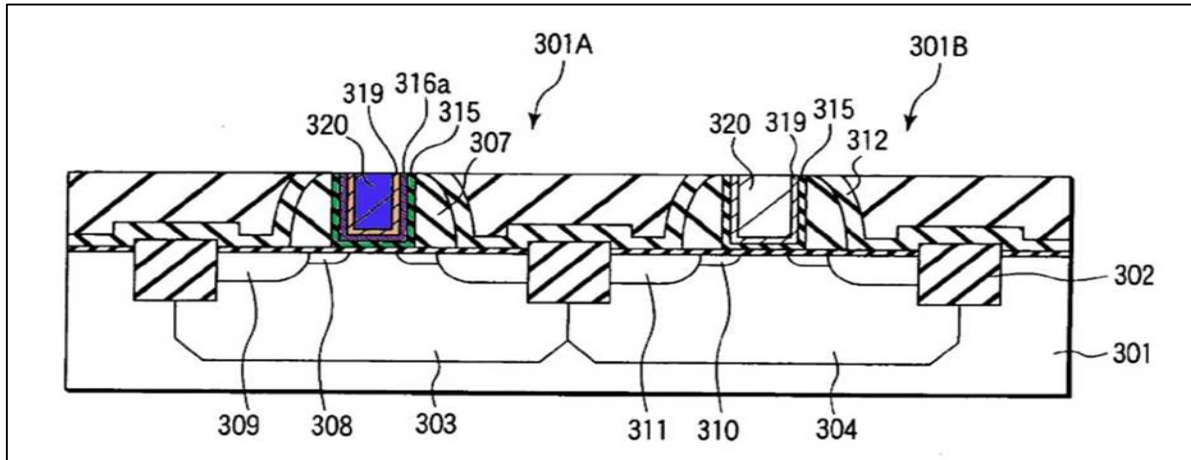
Akasaka discloses the “second MIS transistor” includes “a second gate insulating film formed on a second active region in the semiconductor substrate.” Ex.1101, ¶¶281-82. Akasaka’s gate dielectric film 315 is “depos[it]ed all over the substrate[301],” including area 301A (second active region) “for forming a p-type MISFET.” Ex.1008, ¶¶72-73; *see id.*, FIG. 26 (below); Ex.1101, ¶281.

i. 25[h]

Akasaka discloses the “second MIS transistor” includes “a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film.” Ex.1101, ¶¶283-85.

Akasaka’s PMISFET gate electrode comprises conductive films 316a, 319, and 320. Ex.1008, ¶¶76-77, 82, 86, FIG. 26 (below). Conductive film 316a (first metal film) may be “a [Group-VIII] pure metal, ... a metal silicide, a metal nitride,

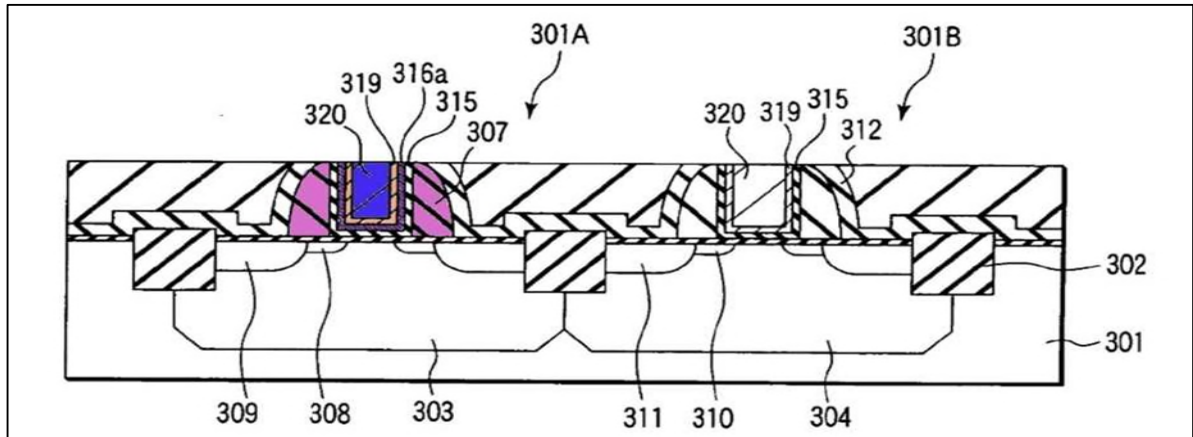
or another compound ... as long as it has a metallic band structure with a work function close to that of p⁺-poly-crystalline silicon.” *Id.*, ¶77. Conductive film 319 may be “a [Group-IVa, Group-Va, or Group-VIa] pure metal, ... a metal silicide, a metal nitride, or another compound ... as long as it has a metallic band structure with a work function close to that of n⁺-poly-crystalline silicon” and conductive film 320 may be tungsten. *Id.*, ¶¶85-86. Either or both conductive films 319 and 320 discloses the claimed “conductive film.” Ex.1101, ¶¶283-84.



Akasaka, FIG. 26

j. 25[i]

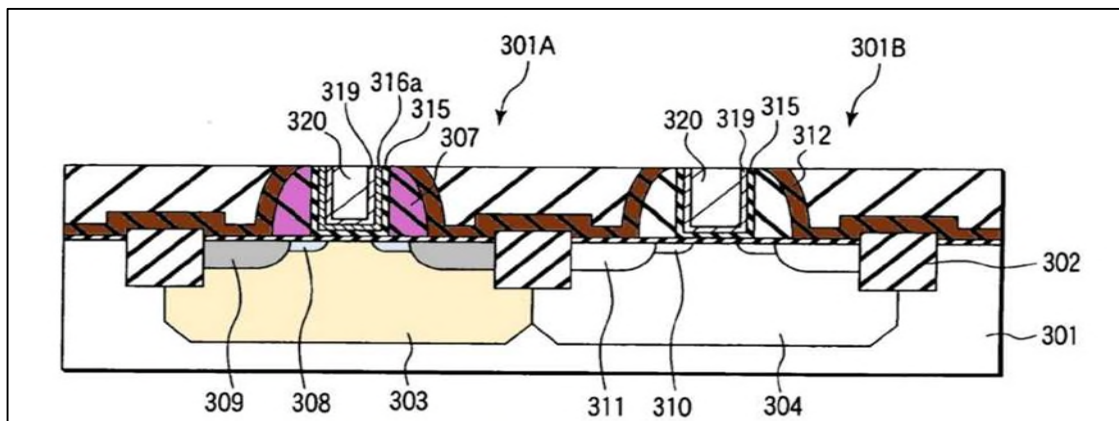
Akasaka discloses the “second MIS transistor” includes “second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative.” Ex.1101, ¶¶286-87. Akasaka discloses “gate sidewall[s] 307” (second sidewall spacers) “formed of an insulating film, such as ... silicon nitride.” Ex.1008, ¶73. As FIG. 26 below shows, gate sidewalls 307 are formed on side surfaces of the second gate electrode. Ex.1101, ¶286.



Akasaka, FIG. 26

k. 25[j]

Akasaka discloses the “second MIS transistor” includes “the silicon nitride film [silicon nitride film 312] formed, extending over the side surfaces of the second gate electrode [PMISFET gate electrode] on which the second sidewall spacers [gate sidewalls 307] are formed and upper surfaces of regions [source/drain layers 309] located in the second active region [area 301A] laterally outside the second sidewall spacers.” Ex.1008, ¶¶72-74, 87, FIGS. 16, 26; Ex.1101, ¶¶288-91.



Akasaka, FIG. 26

l. 25[k]

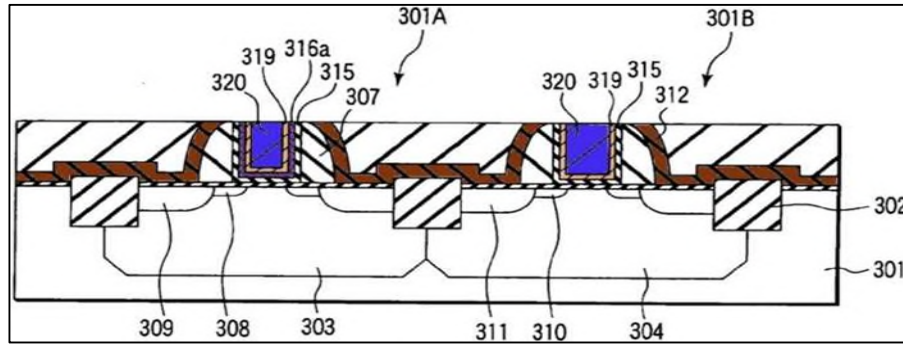
Akasaka discloses “the first and second metal films are made of different

metal materials.” Ex.1101, ¶¶292-95. Either or both conductive films 319 and 320 discloses the claimed “second metal film” with the former having “a metallic band structure with a work function close to that of n^+ -poly- crystalline silicon,” and the latter being tungsten. Ex.1008, ¶¶85-86; Ex.1101, ¶292. Conductive film 316a discloses the claimed “first metal film, ” which “has a metallic band structure with a work function close to that of p^+ -poly-crystalline silicon” (e.g., TiN) and is thus made of a different metal material. *Compare* Ex.1008, ¶77, *with id.*, ¶¶85-86.

m. 25[I]

Akasaka discloses “*the silicon nitride film [silicon nitride film 312] is not formed on any of upper surfaces of the first and second gate electrodes.*” Ex.1101, ¶¶296-301. Akasaka’s fabrication process confirms that this limitation is satisfied.

After silicon nitride film 312 and inter-level insulating film 313 are formed over dummy gate electrodes 306, inter-level insulating film 313 is “polished from above by a CMP (Chemical Mechanical Polishing) method ... to expose ... the upper surface of the silicon nitride film 312.” Ex.1008, ¶¶73-74. “[T]he exposed silicon nitride film 312 and the dummy gate electrodes are [then] selectively removed.” *Id.*, ¶74; *see id.*, ¶¶75-76, 84, 86, FIGS. 19, 25. After forming gate electrode layers 316a, 319, and 320, a second CMP ensures nothing, including silicon nitride film 312, remains on any upper surface of the gate electrodes. *Id.*, ¶87, FIG. 26 (below); Ex.1101, ¶¶297-300.



Akasaka, FIG. 26

n. 25[m]

In the Akasaka-Hsu823 combination semiconductor device, *“the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region.”* Ex.1101, ¶¶302-08.

A POSITA would have been motivated to implement Akasaka's silicon nitride etch-stop film 312 as a tensile etch layer to cause tensile stress along the gate length direction of Akasaka's NMISFET channel region. Ex.1101, ¶304. Akasaka's "silicon nitride film 312 serv[es] as an etching stopper." Ex.1008, ¶73. Hsu823 similarly discloses a tensile silicon nitride etching stopper that causes stress along the gate length direction of the NMOS channel. Ex.1006, ¶¶36-37. Hsu823 explains that "[t]he performance of a MOS device can be enhanced through a stressed-surface channel." Ex.1006, ¶2; *see id.*, ¶3 ("[A] bi-axial, in-plane tensile stress field can improve NMOS performance.")). "A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS

device.” *Id.*, ¶3; see Ex.1528, 1-2; Ex.1531, ¶3; Ex.1529, ¶90; Ex.1530, 1-2; Ex.1523, Fig. 5(c); *supra* IV.A.4.

A POSITA would have selected Akasaka’s etch-stop layer 312 as a tensile etch stop layer for both PMISFET and NMISFET devices, which was well known in the art, because it provides improved NMISFET electron mobility. See *supra* §IV.A.4; Ex.1006, ¶39; Ex.1527, ¶¶38-39; Ex.1526, ¶5; Ex.1528, 1-2; Ex.1530, 1-2; Ex.1523, Fig. 5(c); Ex.1101, ¶304.

A POSITA would have reasonably expected to succeed in implementing Akasaka’s etch stop film 312 as a tensile etch stop layer because such tensile CESL films were widely used to improve carrier mobility in NMISFET devices. *Supra* §IV.A.4; Ex.1101, ¶306. It would have been well within a POSITA’s ability to create such a tensile silicon nitride CESL film simply by adjusting deposition conditions. Ex.1529, ¶¶90, 99-100, TBL. V; Ex.1101, ¶306-07.

2. Claim 26

Akasaka discloses “*wherein the first metal film has a thickness smaller than that of the second metal film.*” Ex.1101, ¶¶309-11. Conductive film 316a (first metal film) is preferably “about 5 nm” or “about 1 to 2 nm.” Ex.1008, ¶77. Conductive film 320 (second metal film) is “about 40 to 50 nm” thick. *Id.*, ¶86.

3. Claim 27

Akasaka discloses “*wherein the first and second metal films have different work functions.*” Ex.1101, ¶¶312-16. Conductive film 316a (first metal film) “is preferably selected to have a work function ... of 4.8 to 5.3 eV.” Ex.1008, ¶¶76-77. Conductive film 319 (second metal film) “is preferably selected to have a work function ... of 3.9 to 4.2 eV.” *Id.*, ¶¶84-85.

4. Claim 28

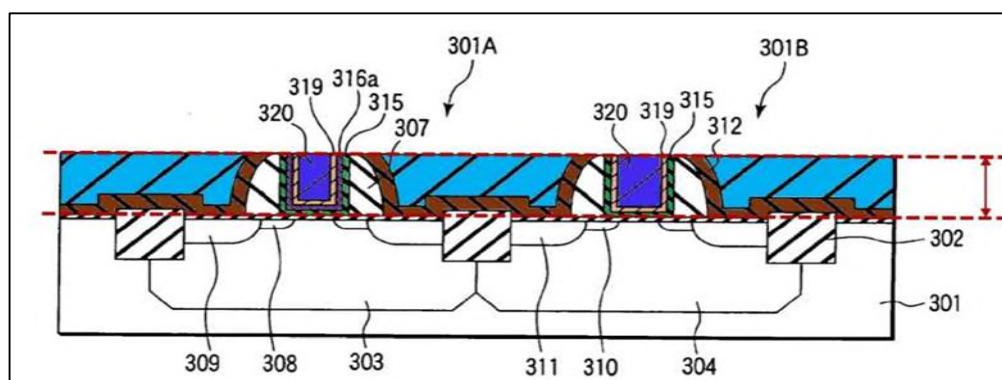
Akasaka discloses “*silicon nitride film [silicon nitride film 312] has a thickness smaller than that of the first gate electrode [NMISFET gate electrode].*” Ex.1101, ¶¶317-35. Akasaka’s FIG. 26 shows silicon nitride film 312 much thinner than the gate electrode in NMISFET region 301B. *See Koito Mfg.*, 381 F.3d at 1154-56 (finding “relative dimensions” of a patent figure sufficient disclosure of such limitation); Ex.1101, ¶317.

For essentially the same four additional reasons discussed in Section VI.A.4, a POSITA also would have found claim 28 obvious. Ex.1101, ¶318.

The only differences between Aoyama and Akasaka regarding claim 28 are that Aoyama’s gate dielectric film 102 is less than 3 nm thick, whereas Akasaka’s

gate dielectric film 315 is no more than about 12 nm thick¹¹ and Aoyama's gate electrode is thicker than 80 nm, whereas Akasaka's gate electrode is thicker than about 41-52 nm. Ex.1101, ¶319; *see* Ex.1008, ¶¶75 (“(EOT) of 1.5 nm or less”), 77, 84-86. Since these differences do not meaningfully affect the analysis in Section VI.A.4, a POSITA would have found claim 28 obvious in view of Akasaka for at least the same reasons. *See* Ex.1101, ¶319.

Like Aoyama's NMISFET and PMISFET gate electrodes 103/104, Akasaka's NMISFET and PMISFET gate electrodes are planarized. *Compare* Ex.1005, ¶119, FIG. 5, *with* Ex.1008, ¶¶73-74, 87, FIG. 26. Accordingly, as in Aoyama, Akasaka's silicon nitride film 312 (brown) is thinner than the NMISFET gate electrode (*see* FIG. 26 (below)) so long as inter-level insulating film 313 (turquoise) is thicker than gate dielectric film 315 (green). Ex.1101, ¶¶320-322.



Akasaka, FIG. 26

¹¹ Realistically, it would be thinner, e.g., about 4 nm when $\kappa=10$. Ex.1101, ¶325; see Ex.1514, ¶¶4, 43, Tbl. 1.

For at least the same reasons a POSITA would have found it obvious for Aoyama's interlayer dielectric 132 to be thicker than gate dielectric film 102 (see §VI.A.4), a POSITA also would have found it obvious for Akasaka's inter-level insulating film 313 to be thicker than gate dielectric film 315 and would have found it very unusual were it otherwise. Ex.1101, ¶¶323-35.

5. Claim 31

Akasaka discloses “*wherein the first and second gate insulating films are made of the same insulating material.*” Ex.1101, ¶¶336-38. Akasaka's gate dielectric film 315 discloses both the “first and second gate insulating films.” Gate dielectric film 315 “is depos[it]ed all over the substrate” including area 301B (first active region) “for forming an n-type MISFET” and area 301A (second active region) “for forming a p-type MISFET,” thereby using the same insulating material (HfSi_xO_y) for both NMISFET and PMISFET devices. Ex.1008, ¶¶72-75, FIGS. 19, 26.

6. Claim 35

Akasaka discloses that “*the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.*” Ex.1101, ¶¶339-40. Akasaka uses “gate dielectric (insulating) film 315,” which may comprise HfSi_xO_y , as both the first and second gate insulating films. Ex.1008, ¶75. This is “a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.” Ex.1101, ¶339; see Ex.1514, ¶4 (explaining

“HfSiO_x ... and oxynitrides thereof” have “dielectricity of more than ten”); *supra* §IV.A.2).

VIII. Mandatory Notices

A. Real Party-in-Interest (37 C.F.R. §42.8(b)(1))

The Petitioner and real parties-in-interest are United Microelectronics Corporation and UMC Group (USA).

B. Related Matters (37 C.F.R. §42.8(b)(2))

To the best of Petitioner’s knowledge, the ’686 patent is subject of the following active proceedings:

- *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation*, Civil Action No. 2:24-cv-00730 in the Eastern District of Texas (Lead Case), filed September 6, 2024;
- *Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Manufacturing Company Limited*, Civil Action No. 2:24-cv-00623 in the Eastern District of Texas (Consolidated Member Case), filed August 1, 2024; and
- *Taiwan Semiconductor Manufacturing Company, Ltd. v. Advanced Integrated Circuit Process LLC*, IPR2025-00682 in the U.S. Patent and Trademark Office, Patent Trial and Appeal Board, filed March 28, 2025.

C. Lead and Back-Up Counsel (37 C.F.R. §42.8(b)(3))

Pursuant to 37 C.F.R. §§42.8(b)(3) and 42.10(a), Petitioner appoints the following lead and back-up counsel:

Lead Counsel	Back Up Counsel
Tim Tingkang Xia (No. 45,242) Tim.Xia@troutman.com TROUTMAN PEPPER LOCKE LLP 600 Peachtree Street, NE, Suite 3000 Atlanta, GA 30308 Telephone: (404) 870-4698	Emma A. Bennett (No. 80,631) Emma.Bennett@troutman.com TROUTMAN PEPPER LOCKE LLP 600 Travis Street, Suite 2800 Houston, TX 77002 Telephone: (713) 226-1549

D. Service Information (37 C.F.R. §42.8(b)(4))

Service information is provided in the designation of counsel above. Petitioner consents to electronic service by email to Tim.Xia@troutman.com and Emma.Bennett@troutman.com.

E. Payment of Fees (37 C.F.R. §42.103)

The Office is authorized to charge the fee set forth in 37 C.F.R. §42.15(a)(1) for this Petition to Deposit Account No. DA201507. Review of five claims is requested. The undersigned further authorizes payment for any additional fees that may be due in connection with this Petition.

IX. Conclusion

For the reasons set forth above, *Inter Partes* Review of the Challenged Claims of the '686 patent is respectfully requested.

Respectfully submitted,

Date: June 6, 2025

/s/ Tim Tingkang Xia
Tim Tingkang Xia (Lead Counsel)
Registration No. 45,242

Counsel for Petitioner

CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), I certify that this Petition complies with the type-volume limits of 37 C.F.R. §42.24(a)(1)(i) because it contains 7,876 words, according to the word-processing system used to prepare this Petition, excluding the parts of this Petition that are exempted by 37 C.F.R. §42.24(a)(1) (table of contents, table of authorities, mandatory notices under §42.8, certificate of service, certificate of word count, or appendix of exhibits or claim listing).

Date: June 6, 2025

/s/ Tim Tingkang Xia
Tim Tingkang Xia (Lead Counsel)
Registration No. 45,242

Counsel for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §42.6(e), this is to certify that on this 6th day of June 2025, I caused to be served on a USB thumb drive a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,198,686 Under 35 U.S.C. §§311, 312 and 37 C.F.R. §42.104 (with Exs. 1001-1002, 1005-1006, 1008, 1101-1111, 1211, 1213, 1216, 1223, 1226-1227, 1229, 1318, 1323, 1333-1334, 1340-1341, 1406, 1413, 1419, 1429-1435, 1511-1512, 1514-1538) via Federal Express Priority Overnight at the Correspondence Address for Patent Owner:

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LIST OF CHALLENGED CLAIMS

Claim 25	
25[Pre]	A semiconductor device comprising:
25[a]	a first MIS transistor; and
25[b]	a second MIS transistor, wherein:
25[c]	the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate;
25[d]	[the first MIS transistor includes: ...] a first gate electrode including a second metal film formed on the first gate insulating film;
25[e]	[the first MIS transistor includes: ...] first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and
25[f]	[the first MIS transistor includes: ...] a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,
25[g]	the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate;
25[h]	[the second MIS transistor includes: ...] a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;
25[i]	[the second MIS transistor includes: ...] second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative; and
25[j]	[the second MIS transistor includes: ...] the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers; and

25[k]	the first and second metal films are made of different metal materials,
25[l]	the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes, and
25[m]	the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region.
Claim 26	
The semiconductor device of claim 25, wherein the first metal film has a thickness smaller than that of the second metal film.	
Claim 27	
The semiconductor device of claim 25, wherein the first and second metal films have different work functions.	
Claim 28	
The semiconductor device of claim 25, wherein the silicon nitride film has a thickness smaller than that of the first gate electrode.	
Claim 31	
The semiconductor device of claim 25, wherein the first and second gate insulating films are made of the same insulating material.	
Claim 35	
The semiconductor device of claim 25, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.	