EXHIBIT 686A1

Invalidity of U.S. Patent No. 8,198,686 in View of
U.S. Patent Application Publication No. 2007/0066077 to Akasaka et al. ("Akasaka '077")

U.S. Patent Application Publication No. 2007/0066077 to Akasaka et al. was filed as Application No. 11/523,466 on September 20, 2006 and published on March 22, 2007 as demonstrated by at least the document itself, the records of the United States Patent and Trademark Office, and/or the testimony of knowledgeable witnesses and corroborating documents. Akasaka '077 is therefore prior art to the '686 Patent under at least 35 U.S.C. § 102(a), (b), and/or (e), as discussed in greater detail in the chart that follows.[1]

To the extent that AICP alleges that Akasaka '077 does not disclose any particular limitation of claims 25, 26, 27, 28, 31, and 35 (the "Asserted Claims") of the '686 Patent, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the priority date of the '686 Patent to modify Akasaka '077 and/or combine the teachings of Akasaka '077 with other prior art references, including but not limited to, the other prior art references in Exhibits 686A1-A5 and 686B, and the relevant sections of the charts for other prior art to the '686 Patent in a manner that would have rendered the Asserted Claim invalid as obvious.

Defendants reserve the right to amend or supplement this claim chart at a later date as more fully set forth in the Preliminary Invalidity Contentions. The cited portions of the prior art references are merely illustrative, and Defendants reserve the right to rely on alternative or additional evidence, including uncited portions of the prior art references.

[1] These preliminary invalidity charts, in some instances, rely, at least in part, on AICP's apparent positions regarding the scope of its claims for purposes of asserting infringement. Defendants' assertion that a particular limitation is disclosed by a prior art reference, or Defendants' assertion that a particular limitation is disclosed by a prior art reference in a particular manner, may be based in part on AICP's apparent claim interpretations. In relying in part on AICP's apparent claim interpretations, Defendants do not admit that AICP's apparent claim interpretations are supportable or proper or that the claim limitations in question are definite or otherwise amenable to construction. Nor do Defendants admit that the claims are enabled, adequately described, or cover patentable subject matter, or that any of the Accused Instrumentalities infringe any claim of the Asserted Patents. Nor shall anything stated herein be construed as an admission or waiver of any particular construction of any claim term, or argument under 35 U.S.C. § 112. Nothing in these claim charts should be understood as an admission relating to infringement, either literally or under the doctrine of equivalents, or as an admission relating to the Defendants' understanding of the proper interpretation or scope of the Asserted Claim. Moreover, Defendants reserve the right to rely on additional citations or sources of evidence that may also be applicable, or that may become applicable in light of any Court order on claim construction, changes in AICP's Preliminary Infringement Contentions, or information obtained during discovery as the case proceeds.

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Where the chart below states that the reference "discloses" or "describes" or "teaches" a limitation, such disclosure may be express, inherent, or implicit. Unless otherwise indicated, all citations to other claim charts in the discussion of claim elements below refer specifically to the corresponding claim element of the other claim chart.

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
25 [pre]	A semiconductor device comprising:	Akasaka '077, as evidenced by the example citations below, discloses a semiconductor device. [0003] The present invention relates to a method for manufacturing a semiconductor device, particularly an FET (Field Effect Transistor) of the MIS (Metal Insulator Semiconductor) type, and to a method for forming a silicon-containing dielectric (insulating) film, utilized in, e.g., a semiconductor processing system. The term "semiconductor process" used herein includes various kinds of processes which are performed to manufacture a semiconductor device or a structure having wiring layers, electrodes, and the like to be connected to a semiconductor device, on a target substrate, such as a semiconductor wafer or a glass substrate used for an LCD (Liquid Crystal Display) or FPD (Flat Panel Display), by forming semiconductor layers, insulating layers, and conductive layers in predetermined patterns on the target substrate. [0005] In recent years, owing to the demands of increased miniaturization, CMOS (Complementary Metal Oxide Semiconductor) transistors comprising MISFETs having a dual metal gate structure have attracted attentions. For example, Samavedam et al., IEDM Tech. Digest, p. 443, 2002 (Non-Patent Document 1) discloses a process for manufacturing a CMOS transistor, as shown in FIGS. 27 to 31. [0008] An object of the present invention is to provide a method for manufacturing a semiconductor device, which can solve a problem due to etching residues of a silicon-containing dielectric film, and a method for forming a silicon-containing dielectric film with a surface having a low etching rate.

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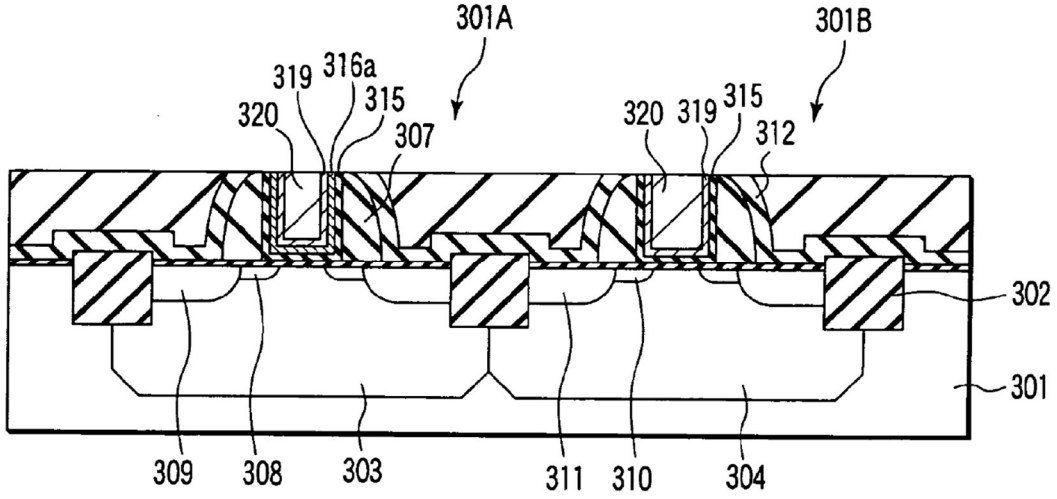
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		[0034] FIGS. 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, and 12 are sectional views showing sequentially ordered steps in a method for manufacturing a semiconductor device according to a first embodiment of the present invention. [0039] In the process of developing the present invention, the inventors studied problems caused in conventional methods for manufacturing a semiconductor device, as those disclosed in Non-Patent Document 1 and so forth. As a result, the inventors have arrived at the findings given below.  FIG. 26
25 [a]	a first MIS transistor; and	Akasaka '077, as evidenced by the example citations below, discloses a first MIS transistor. [0072] FIGS. 15 to 26 are sectional views showing sequentially ordered steps in a method for manufacturing a semiconductor device according to a second embodiment of the present

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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		invention. At first, as shown in FIG. 15, an n-type well 303 and a p-type well 304 are respectively formed in the surface of first and second areas 301A and 301B of a semiconductor substrate 301 consisting mainly of silicon. Further, a device isolation area 302 is formed in the surface of the substrate 301 to surround the first and second areas 301A and 301B. The first and second areas 301A and 301B correspond to areas for forming a p-type MISFET and an n-type MISFET, respectively.

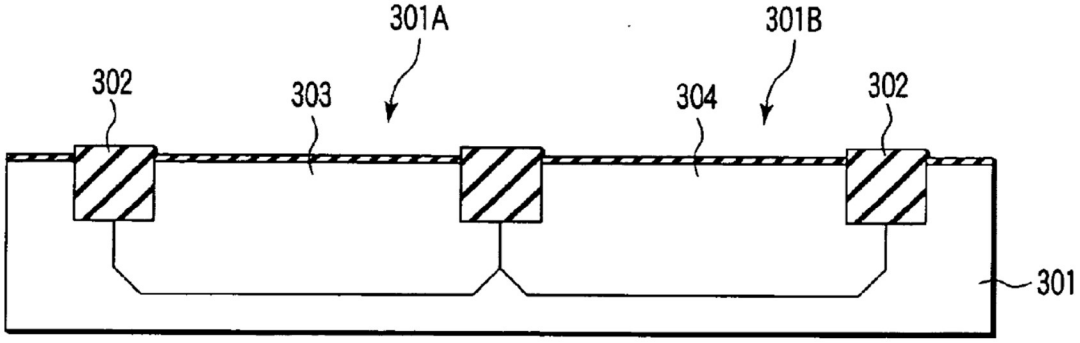

FIG. 15

[0073]Then, as shown in FIG. 16, a starting structure including a dummy gate electrode made of, e.g., poly-crystalline silicon is formed by conventional techniques for forming transistors. In this starting structure, the source/drain layers 309 and extensions 308 of the p-type MISFET are formed in the n-type well 303 within the first area 301A. Similarly, the source/drain layers 311 and extensions 310 of the n-type MISFET are formed in the p-type well 304 within the second area 301B. Further, a dummy gate electrode 306 made of poly-crystalline silicon is disposed through a dummy gate dielectric (insulating) film 305 formed of a silicon oxide film, at each of predetermined positions on the substrate within the first and second areas 301A and 301B. A gate sidewall 307 formed of an insulating film, such as a silicon nitride film is disposed on the side surface of each dummy gate electrode 306. The

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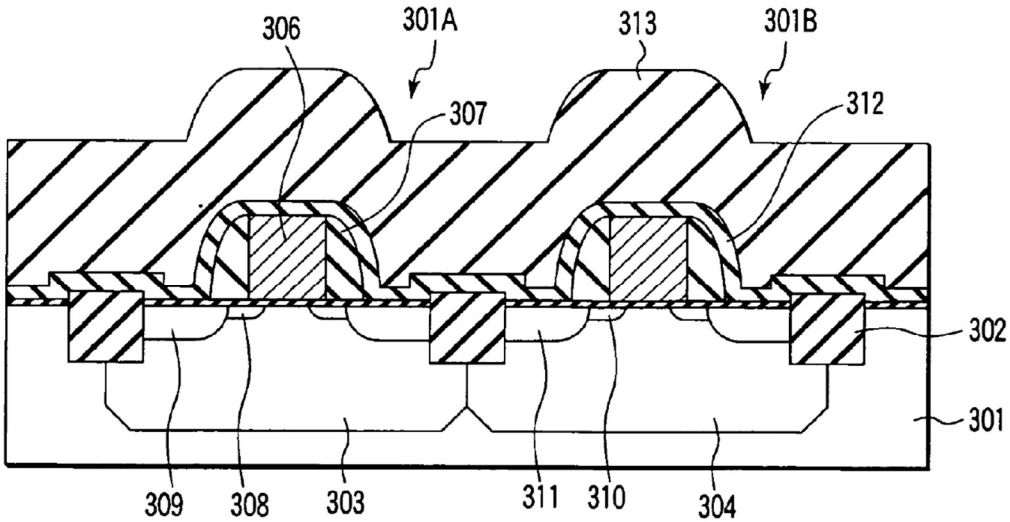
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312 serving as an etching stopper. Further, an inter-level insulating film 313 is disposed on the silicon nitride film 312.  FIG. 16 The description and annotation below are an example of a first MIS transistor. For example, as can be seen in Figs. 15-26, Akasaka '077 discloses two transistors, a p-type MISFET in 301A and an n-type MISFET in 301B. The n-type MISFET in 301B is an example of a first MIS transistor.

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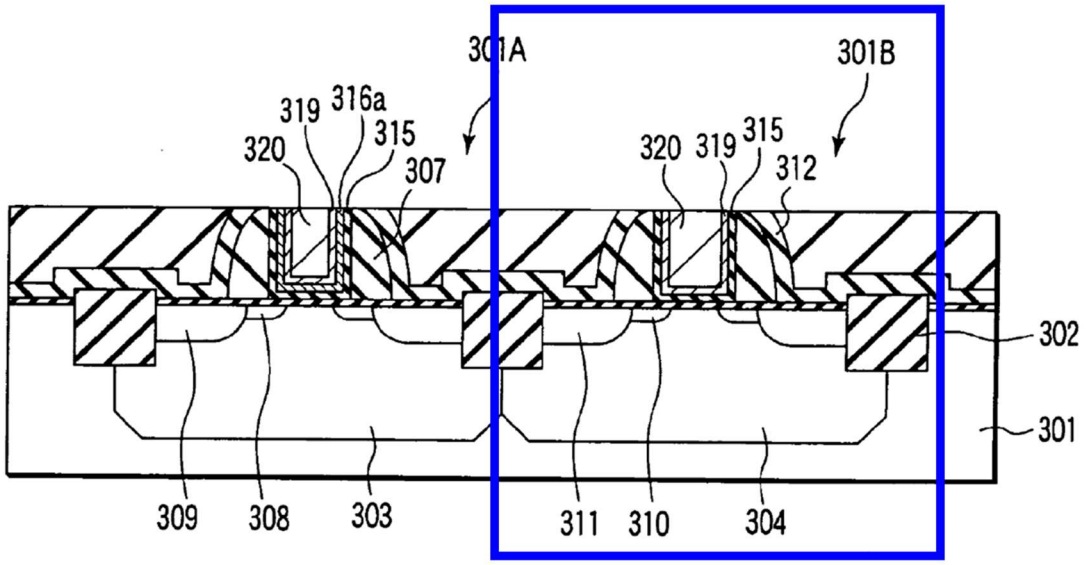
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 FIG. 26 first MIS transistor
25 [b]	a second MIS transistor,	Akasaka '077, as evidenced by the example citations below, discloses a second MIS transistor. [0072] FIGS. 15 to 26 are sectional views showing sequentially ordered steps in a method for manufacturing a semiconductor device according to a second embodiment of the present invention. At first, as shown in FIG. 15, an n-type well 303 and a p-type well 304 are respectively formed in the surface of first and second areas 301A and 301B of a semiconductor substrate 301 consisting mainly of silicon. Further, a device isolation area 302 is formed in the surface of the substrate 301 to surround the first and second areas 301A and 301B. The first and second areas 301A and 301B correspond to areas for forming a p-type MISFET and an n-type MISFET, respectively.

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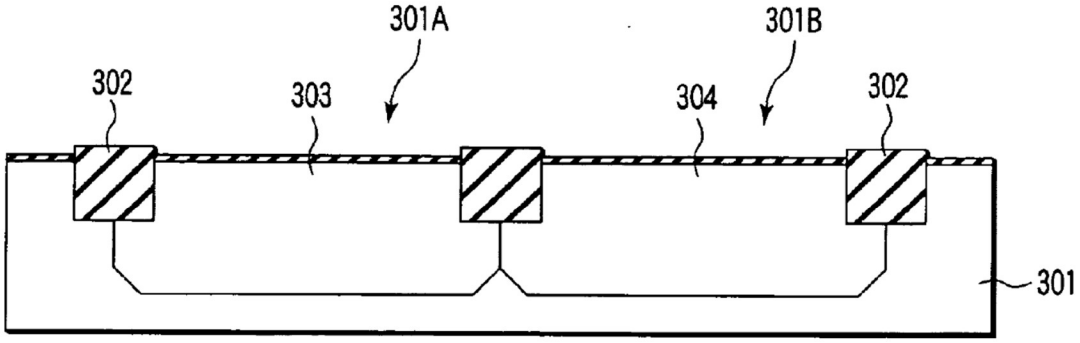
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 FIG. 15 [0073]Then, as shown in FIG. 16, a starting structure including a dummy gate electrode made of, e.g., poly-crystalline silicon is formed by conventional techniques for forming transistors. In this starting structure, the source/drain layers 309 and extensions 308 of the p-type MISFET are formed in the n-type well 303 within the first area 301A. Similarly, the source/drain layers 311 and extensions 310 of the n-type MISFET are formed in the p-type well 304 within the second area 301B. Further, a dummy gate electrode 306 made of poly-crystalline silicon is disposed through a dummy gate dielectric (insulating) film 305 formed of a silicon oxide film, at each of predetermined positions on the substrate within the first and second areas 301A and 301B. A gate sidewall 307 formed of an insulating film, such as a silicon nitride film is disposed on the side surface of each dummy gate electrode 306. The dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312 serving as an etching stopper. Further, an inter-level insulating film 313 is disposed on the silicon nitride film 312.

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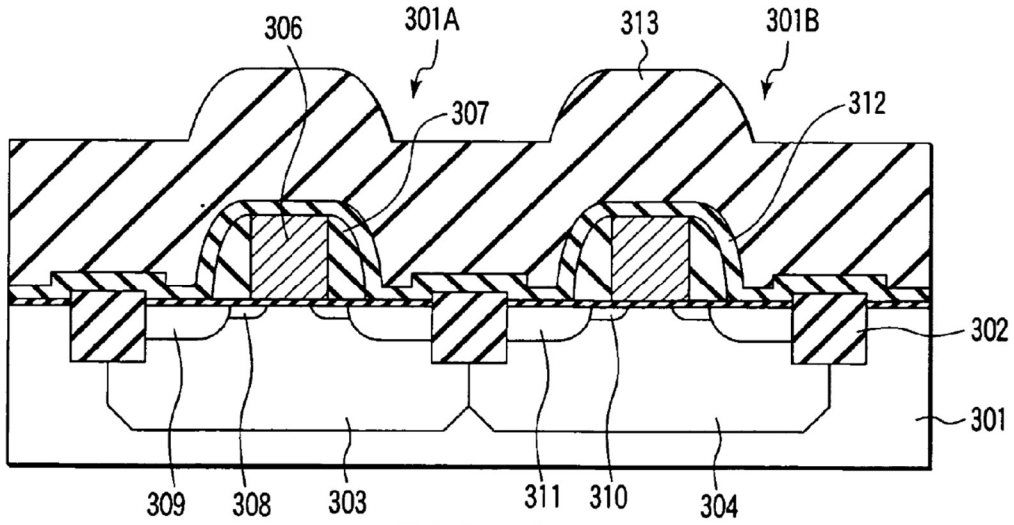
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 FIG. 16 The description and annotation below are an example of a second MIS transistor. For example, as can be seen in Figs. 15-26, Akasaka '077 discloses two transistors, a p-type MISFET in 301A and an n-type MISFET in 301B. The p-type MISFET in 301A is an example of a second MIS transistor.

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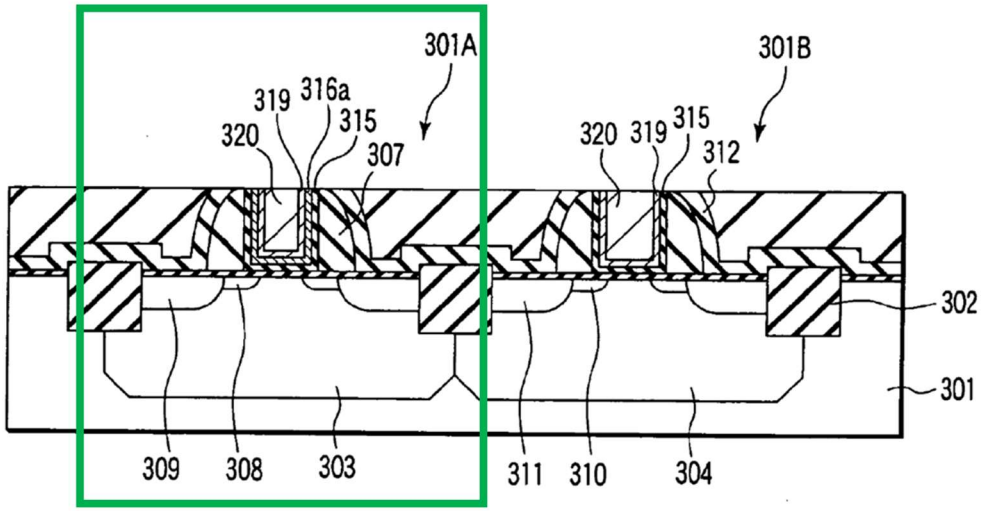
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 second MIS transistor FIG. 26 first MIS transistor
25 [c.1]	wherein: the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate;	Akasaka '077, as evidenced by the example citations below, discloses the first MIS transistor including a first gate insulating film formed on a first active region in a semiconductor substrate. [0072] FIGS. 15 to 26 are sectional views showing sequentially ordered steps in a method for manufacturing a semiconductor device according to a second embodiment of the present invention. At first, as shown in FIG. 15, an n-type well 303 and a p-type well 304 are respectively formed in the surface of first and second areas 301A and 301B of a semiconductor substrate 301 consisting mainly of silicon. Further, a device isolation area 302 is formed in the surface of the substrate 301 to surround the first and second areas 301A

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		and 301B. The first and second areas 301A and 301B correspond to areas for forming a p-type MISFET and an n-type MISFET, respectively. [0073] Then, as shown in FIG. 16, a starting structure including a dummy gate electrode made of, e.g., poly-crystalline silicon is formed by conventional techniques for forming transistors. In this starting structure, the source/drain layers 309 and extensions 308 of the p-type MISFET are formed in the n-type well 303 within the first area 301A. Similarly, the source/drain layers 311 and extensions 310 of the n-type MISFET are formed in the p-type well 304 within the second area 301B. Further, a dummy gate electrode 306 made of poly-crystalline silicon is disposed through a dummy gate dielectric (insulating) film 305 formed of a silicon oxide film, at each of predetermined positions on the substrate within the first and second areas 301A and 301B. A gate sidewall 307 formed of an insulating film, such as a silicon nitride film is disposed on the side surface of each dummy gate electrode 306. The dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312 serving as an etching stopper. Further, an inter-level insulating film 313 is disposed on the silicon nitride film 312. [0074] Then, as shown in FIG. 17, the inter-level insulating film 313 is polished from above by a CMP (Chemical Mechanical Polishing) method. This step is arranged to expose the upper surface of the dummy gate electrode 306 or the upper surface of the silicon nitride film 312 deposited on the dummy gate electrode 306. Then, as shown in FIG. 18, the exposed silicon nitride film 312 and the dummy gate electrodes are selectively removed to form recess portions 314. Then, as shown in FIG. 19, the portions of the dummy gate dielectric film 305 exposed at the bottom of the recess portions 314 are removed.

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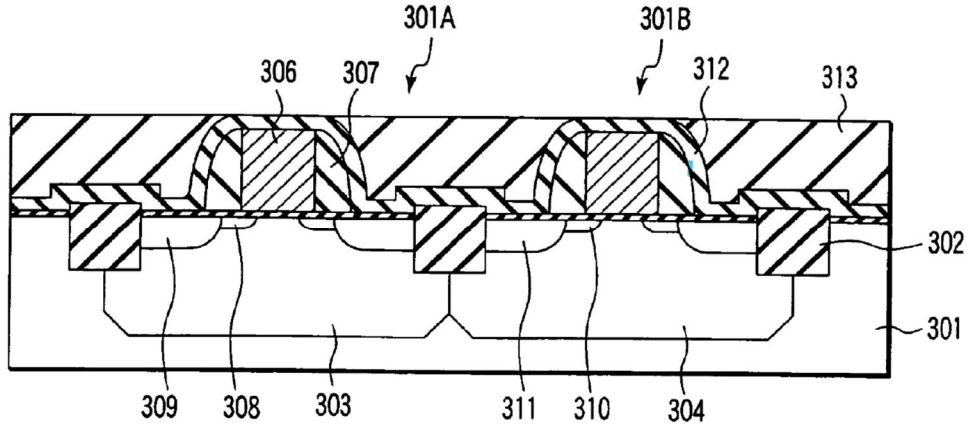
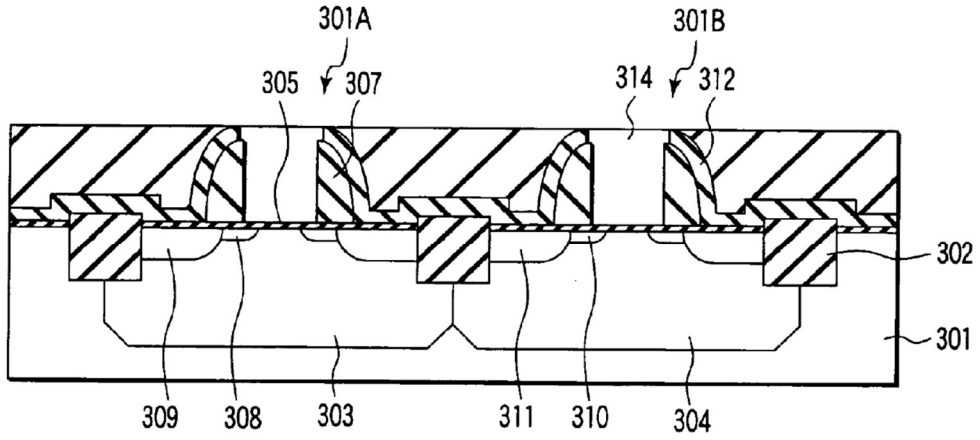
		 FIG. 17  FIG. 18 [0075] Then, a gate dielectric (insulating) film 315 is deposed all over the substrate to cover the inner surface of the recess portions 314. The gate dielectric film 315 may be preferably

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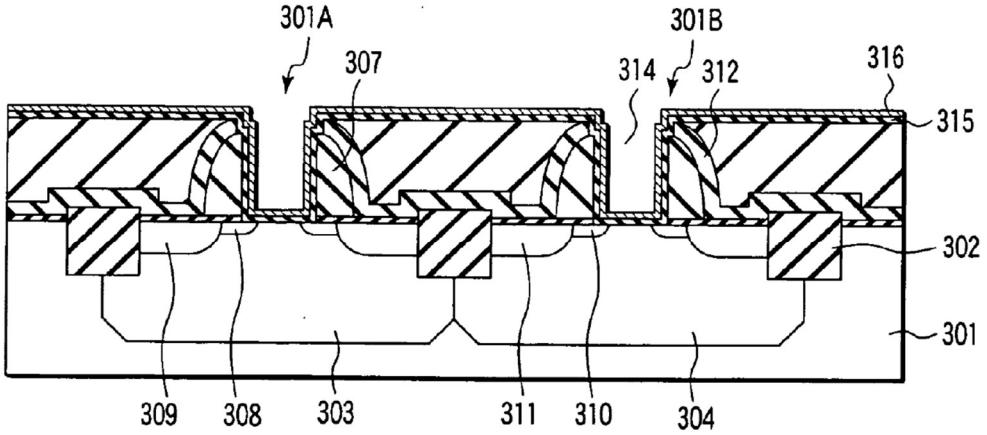
		made of a film of HfO2, HfSixOy, HfAlxOy, or SiO2 doped with nitrogen. The film thickness of the gate dielectric film 315 is preferably set to agree with an effective film thickness (EOT) of 1.5 nm or less, to manufacture a MISFET having a gate length of 100 nm or less. EOT is expressed by a value converted into the thickness of a silicon oxide film having an equivalent gate capacity.  FIG. 19 The description and annotation below are an example of a first gate insulating film formed on a first active region. For example, as can be seen in Figs. 15-26, Akasaka '077 discloses gate dielectric (insulating) film 315 is part of a first gate insulating film and p-type well 304 includes a first active region for the n-type MIS transistor.

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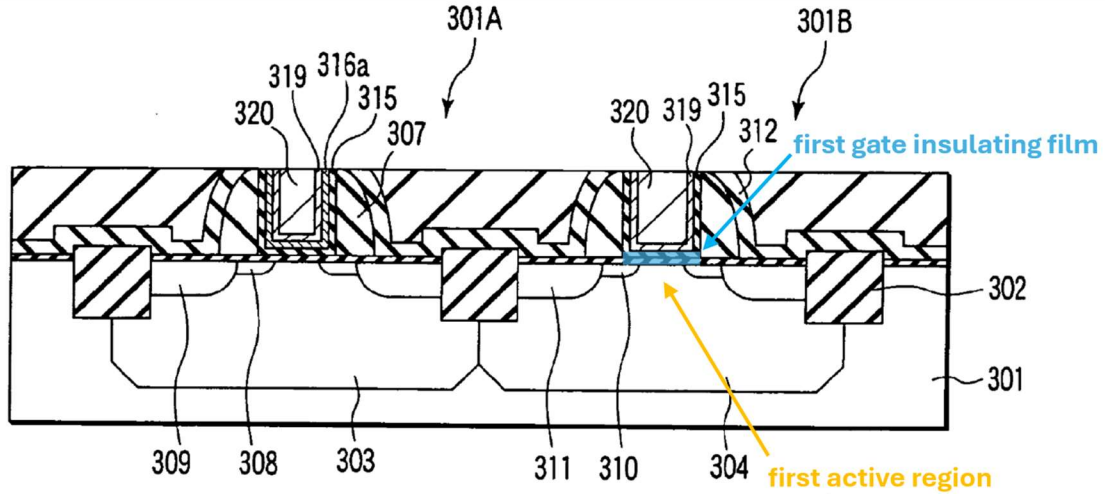
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 FIG. 26
25 [c.2]	a first gate electrode including a second metal film formed on the first gate insulating film;	Akasaka '077, as evidenced by the example citations below, discloses a first gate electrode including a second metal film formed on the first gate insulating film. [0084] Then, a conductive film 319 to define the bottom portion of the gate electrode of the n-type MISFET is formed all over the substrate. The conductive film 319 is disposed to control the work function of the gate electrode of the n-type MISFET. Accordingly, the type of the material of the conductive film 319 should also be determined in consideration of its work function. [0085] Specifically, in order to decrease the threshold voltage of the n-type MISFET, the material is preferably selected to have a work function close to that of n+-poly-crystalline silicon, such as a work function of 3.9 to 4.2 eV. For example, in the case of a pure metal, a Group-IVa element, such as Ti, Zr, or Hf, a Group-Va element, such as V, Nb, or Ta, or a Group-VIa element, such as Cr, Mo, or W, is preferably used. Alternatively, a metal silicide, a metal nitride, or another compound may be used, as long as it has a metallic band structure

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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		with a work function close to that of n+-poly-crystalline silicon. The film thickness of the conductive film 319 may be set at a very small value of about 1 to 2 nm. [0086] Then, a conductive film 320 to decrease the resistance of the gate electrode is deposited all over the substrate. The film thickness of the conductive film 320 is preferably set to provide a sheet resistance of about 5Ω/□ or less, such as about 40 to 50 nm in the case of W being used. In this embodiment, the conductive film 319 and conductive film 320 are made of different conductive materials. However, where the material selected for the conductive film 319 has a resistivity almost equal to or less than that required for the conductive film 320 and suitable for the subsequent steps, the conductive film 319 and conductive film 320 are made of one integral film. The conductive film 316 for the gate electrode of the p-type MISFET and the conductive film 319 for the gate electrode of the n-type MISFET may be deposited in an order reverse to that of the embodiment, in consideration of their workability, reactivity, and so forth. [0087] Then, as shown in FIG. 26, a CMP method or the like is used to remove those portions of the insulating film 315 and conductive films 316, 319, and 320 which are deposited outside the recess portions 314. Thereafter, inter-level insulating films, interconnections, and so forth are formed by conventional techniques to complete the MISFETs. The description and annotation below are an example of a first gate electrode including a second metal film formed on the first gate insulating film. For example, as can be seen in Figs. 15-26, Akasaka '077 discloses forming a gate electrode for the n-type MIS transistor of conductive film 319 on top of gate dielectric (insulating) film 315 and conductive film 320.

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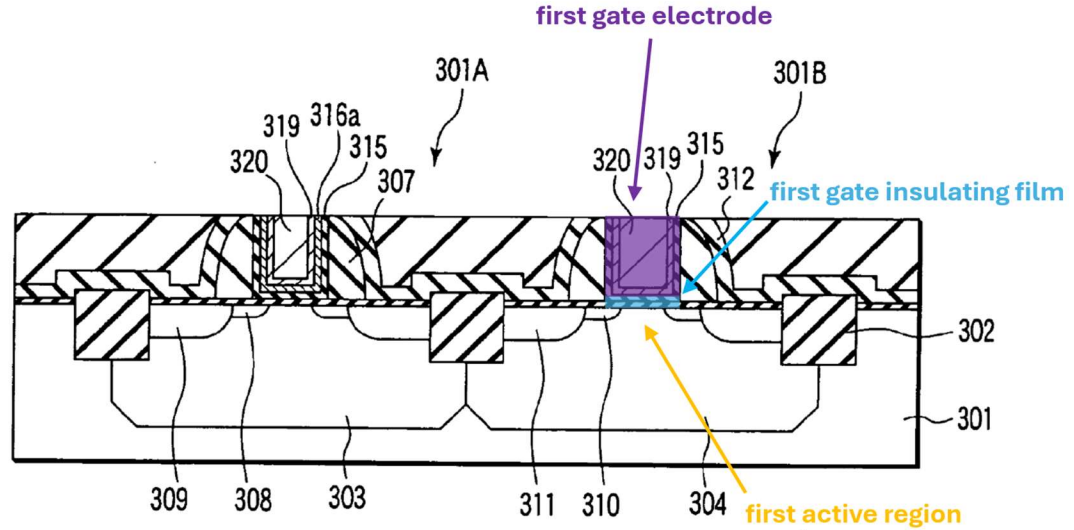
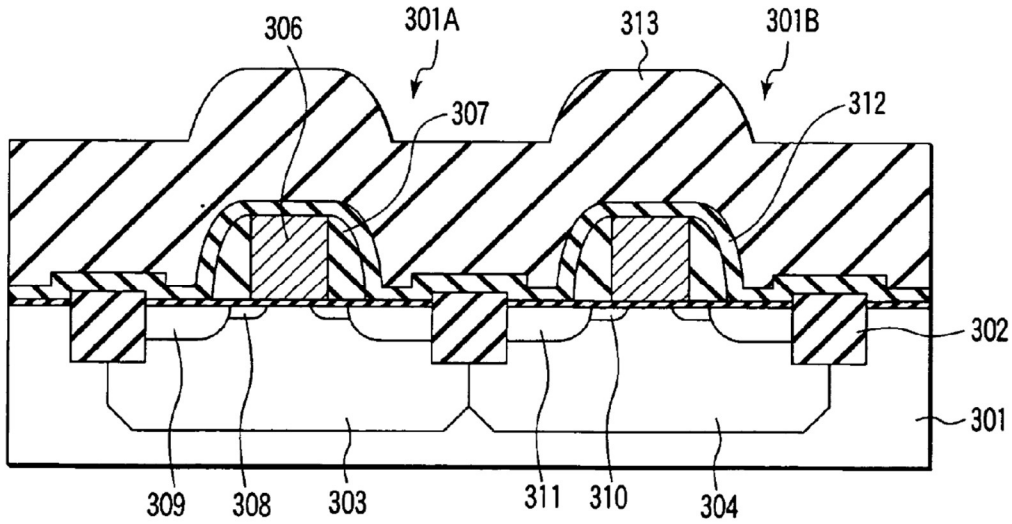
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 FIG. 26
25 [c.3]	first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and	Akasaka '077, as evidenced by the example citations below, discloses first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative. [0072] FIGS. 15 to 26 are sectional views showing sequentially ordered steps in a method for manufacturing a semiconductor device according to a second embodiment of the present invention. At first, as shown in FIG. 15, an n-type well 303 and a p-type well 304 are respectively formed in the surface of first and second areas 301A and 301B of a semiconductor substrate 301 consisting mainly of silicon. Further, a device isolation area 302 is formed in the surface of the substrate 301 to surround the first and second areas 301A and 301B. The first and second areas 301A and 301B correspond to areas for forming a p-type MISFET and an n-type MISFET, respectively. [0073] Then, as shown in FIG. 16, a starting structure including a dummy gate electrode made of, e.g., poly-crystalline silicon is formed by conventional techniques for forming

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		transistors. In this starting structure, the source/drain layers 309 and extensions 308 of the p-type MISFET are formed in the n-type well 303 within the first area 301A. Similarly, the source/drain layers 311 and extensions 310 of the n-type MISFET are formed in the p-type well 304 within the second area 301B. Further, a dummy gate electrode 306 made of poly-crystalline silicon is disposed through a dummy gate dielectric (insulating) film 305 formed of a silicon oxide film, at each of predetermined positions on the substrate within the first and second areas 301A and 301B. A gate sidewall 307 formed of an insulating film, such as a silicon nitride film is disposed on the side surface of each dummy gate electrode 306. The dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312 serving as an etching stopper. Further, an inter-level insulating film 313 is disposed on the silicon nitride film 312.  FIG. 16

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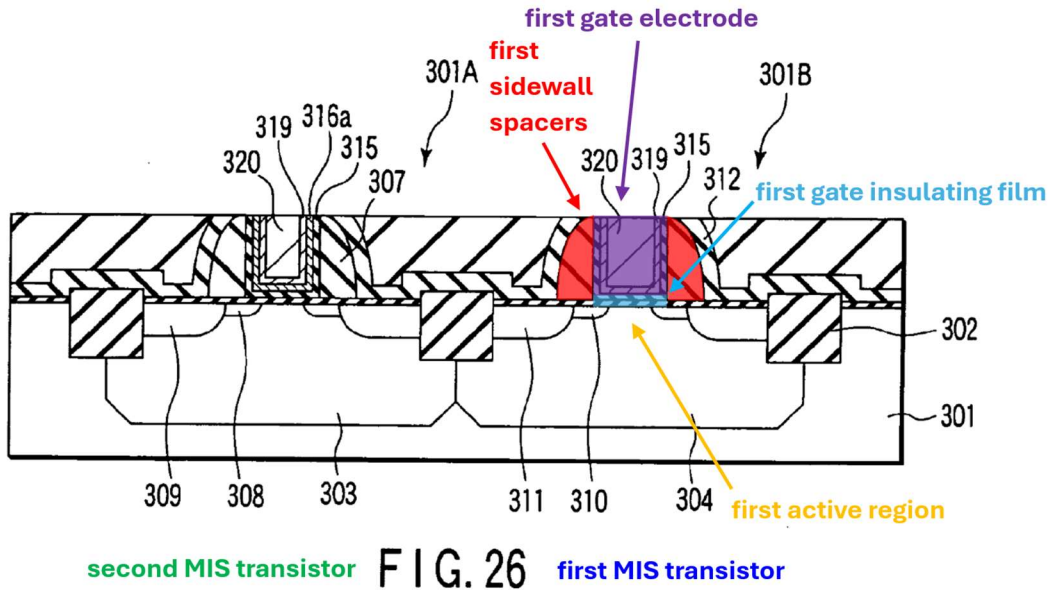
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		The description and annotation below are an example of first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative. For example, as can be seen in Figs. 15-26, Akasaka '077 discloses forming gate sidewall 307 of an insulating film, such as silicon nitride.  FIG. 26

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25 [c.4]	a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,	Akasaka '077, as evidenced by the example citations below, discloses a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers. [0073] Then, as shown in FIG. 16, a starting structure including a dummy gate electrode made of, e.g., poly-crystalline silicon is formed by conventional techniques for forming transistors. In this starting structure, the source/drain layers 309 and extensions 308 of the p-type MISFET are formed in the n-type well 303 within the first area 301A. Similarly, the source/drain layers 311 and extensions 310 of the n-type MISFET are formed in the p-type well 304 within the second area 301B. Further, a dummy gate electrode 306 made of poly-crystalline silicon is disposed through a dummy gate dielectric (insulating) film 305 formed of a silicon oxide film, at each of predetermined positions on the substrate within the first and second areas 301A and 301B. A gate sidewall 307 formed of an insulating film, such as a silicon nitride film is disposed on the side surface of each dummy gate electrode 306. The dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312 serving as an etching stopper. Further, an inter-level insulating film 313 is disposed on the silicon nitride film 312.

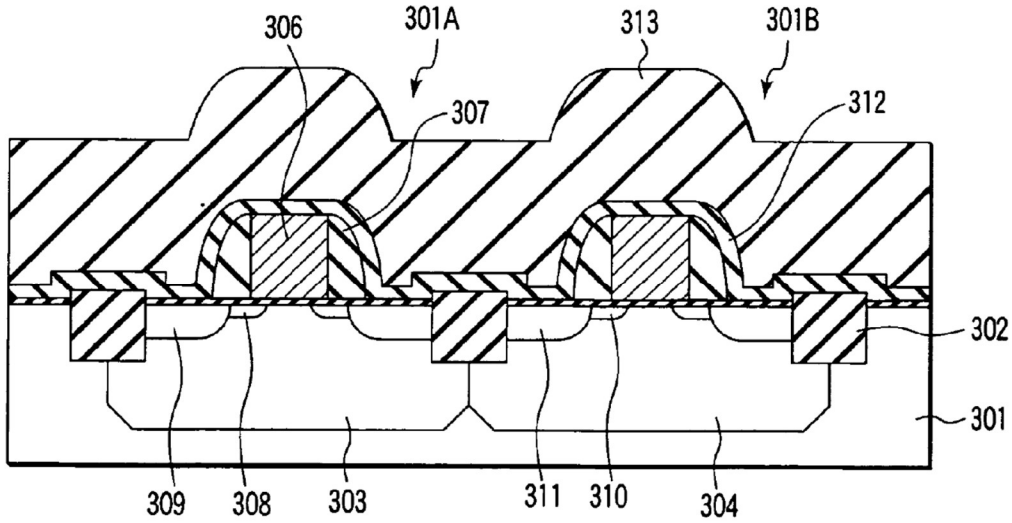

FIG. 16

[0074] Then, as shown in FIG. 17, the inter-level insulating film 313 is polished from above by a CMP (Chemical Mechanical Polishing) method. This step is arranged to expose the upper surface of the dummy gate electrode 306 or the upper surface of the silicon nitride film 312 deposited on the dummy gate electrode 306. Then, as shown in FIG. 18, the exposed silicon nitride film 312 and the dummy gate electrodes are selectively removed to form recess portions 314. Then, as shown in FIG. 19, the portions of the dummy gate dielectric film 305 exposed at the bottom of the recess portions 314 are removed.

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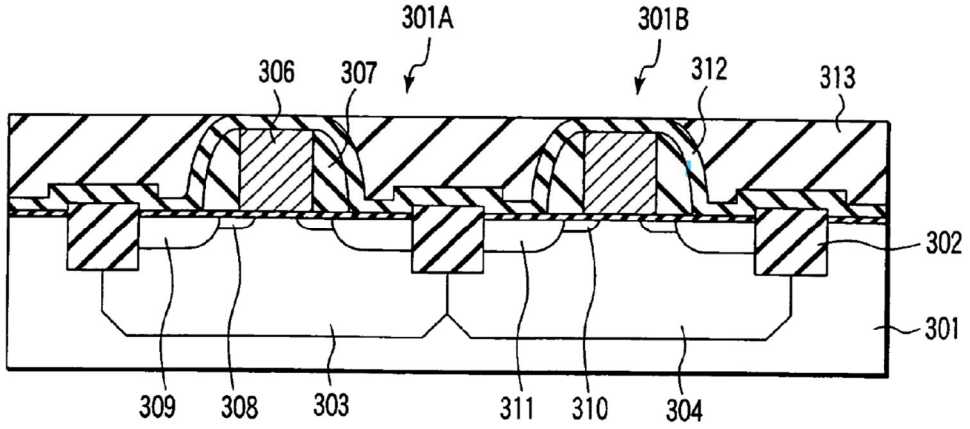
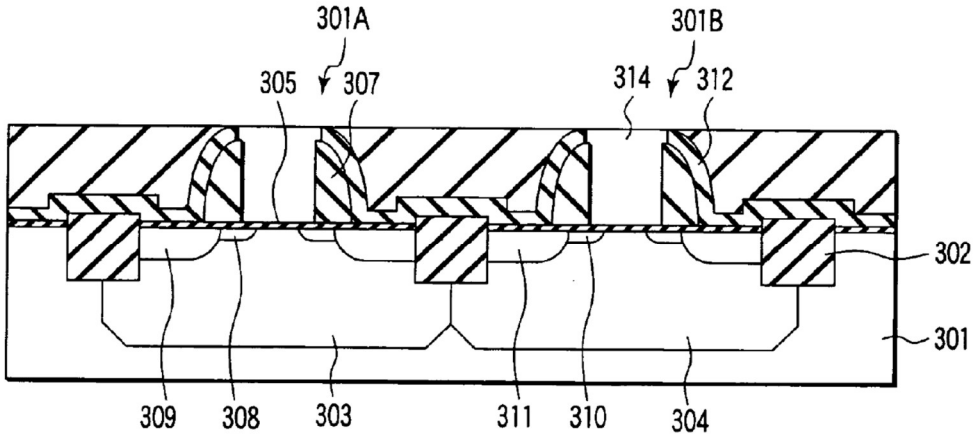
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 FIG. 17  FIG. 18

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		[0087] Then, as shown in FIG. 26, a CMP method or the like is used to remove those portions of the insulating film 315 and conductive films 316, 319, and 320 which are deposited outside the recess portions 314. Thereafter, inter-level insulating films, interconnections, and so forth are formed by conventional techniques to complete the MISFETs. The description and annotation below are an example of a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers. For example, as can be seen in Figs. 15-26, Akasaka '077 discloses forming silicon nitride film 312 over the side surfaces of the gate electrode and sidewall spacers 307 as well as over upper surfaces of regions located in the first active region laterally outside the first sidewall spacers.

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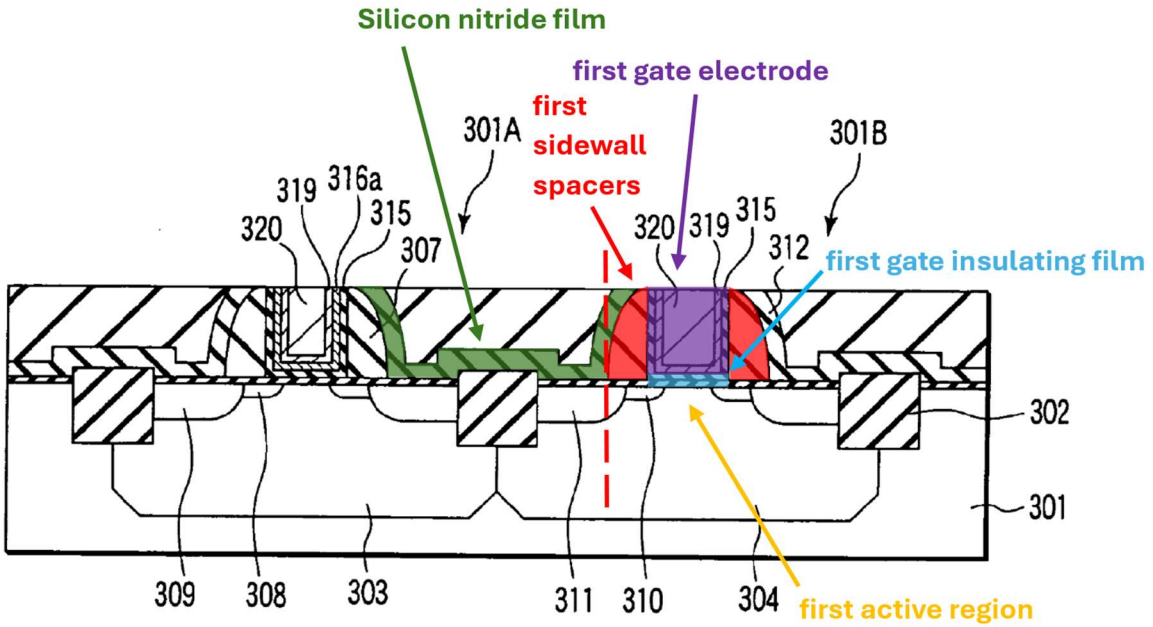
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 FIG. 26
25 [d.1]	the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate;	Akasaka '077, as evidenced by the example citations below, discloses the second MIS transistor including a second gate insulating film formed on a second active region in the semiconductor substrate. [0072] FIGS. 15 to 26 are sectional views showing sequentially ordered steps in a method for manufacturing a semiconductor device according to a second embodiment of the present invention. At first, as shown in FIG. 15, an n-type well 303 and a p-type well 304 are respectively formed in the surface of first and second areas 301A and 301B of a semiconductor substrate 301 consisting mainly of silicon. Further, a device isolation area 302 is formed in the surface of the substrate 301 to surround the first and second areas 301A

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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		and 301B. The first and second areas 301A and 301B correspond to areas for forming a p-type MISFET and an n-type MISFET, respectively. [0073] Then, as shown in FIG. 16, a starting structure including a dummy gate electrode made of, e.g., poly-crystalline silicon is formed by conventional techniques for forming transistors. In this starting structure, the source/drain layers 309 and extensions 308 of the p-type MISFET are formed in the n-type well 303 within the first area 301A. Similarly, the source/drain layers 311 and extensions 310 of the n-type MISFET are formed in the p-type well 304 within the second area 301B. Further, a dummy gate electrode 306 made of poly-crystalline silicon is disposed through a dummy gate dielectric (insulating) film 305 formed of a silicon oxide film, at each of predetermined positions on the substrate within the first and second areas 301A and 301B. A gate sidewall 307 formed of an insulating film, such as a silicon nitride film is disposed on the side surface of each dummy gate electrode 306. The dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312 serving as an etching stopper. Further, an inter-level insulating film 313 is disposed on the silicon nitride film 312. [0074] Then, as shown in FIG. 17, the inter-level insulating film 313 is polished from above by a CMP (Chemical Mechanical Polishing) method. This step is arranged to expose the upper surface of the dummy gate electrode 306 or the upper surface of the silicon nitride film 312 deposited on the dummy gate electrode 306. Then, as shown in FIG. 18, the exposed silicon nitride film 312 and the dummy gate electrodes are selectively removed to form recess portions 314. Then, as shown in FIG. 19, the portions of the dummy gate dielectric film 305 exposed at the bottom of the recess portions 314 are removed.

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.

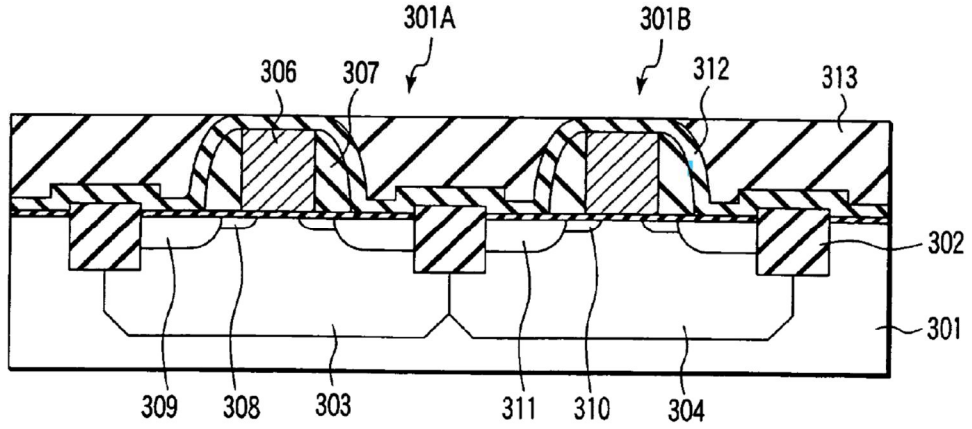

FIG. 17

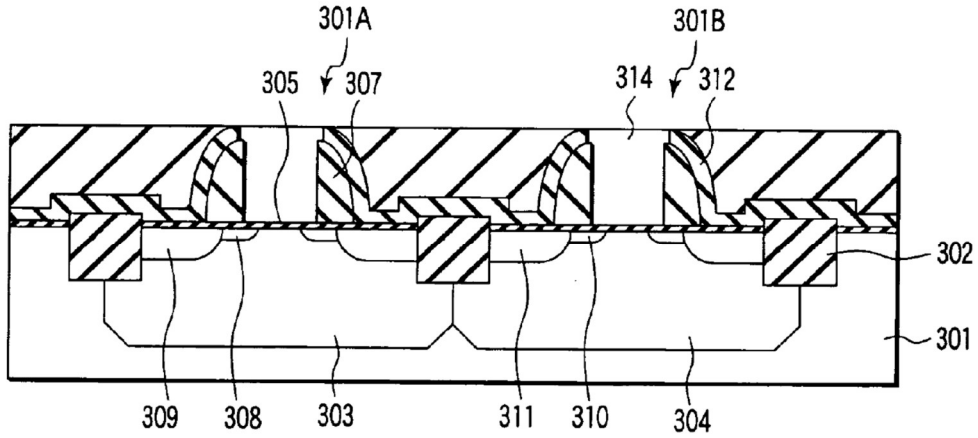

FIG. 18

[0075] Then, a gate dielectric (insulating) film 315 is deposed all over the substrate to cover the inner surface of the recess portions 314. The gate dielectric film 315 may be preferably

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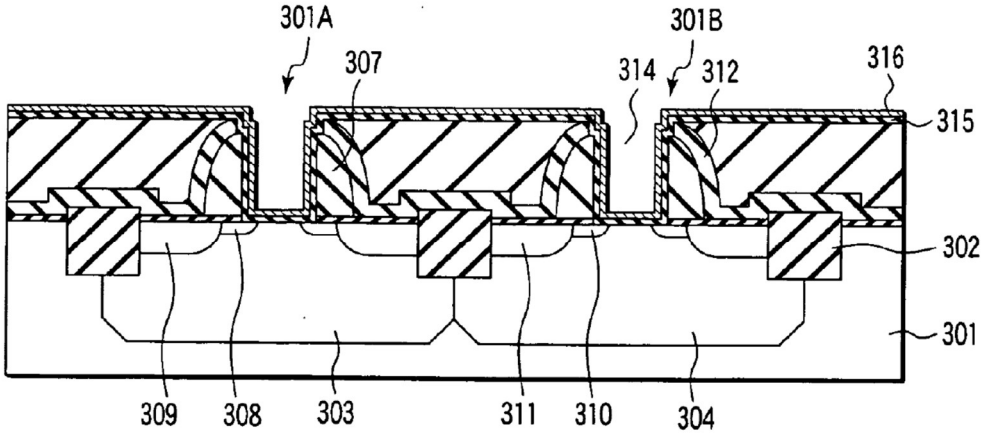
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		made of a film of HfO2, HfSixOy, HfAlxOy, or SiO2 doped with nitrogen. The film thickness of the gate dielectric film 315 is preferably set to agree with an effective film thickness (EOT) of 1.5 nm or less, to manufacture a MISFET having a gate length of 100 nm or less. EOT is expressed by a value converted into the thickness of a silicon oxide film having an equivalent gate capacity.  FIG. 19 The description and annotation below are an example of a second gate insulating film formed on a second active region in the semiconductor substrate. For example, as can be seen in Figs. 15-26, Akasaka '077 discloses gate dielectric (insulating) film 315 is part of a second gate insulating film and n-type well 303 includes a second active region for the p-type MIS transistor.

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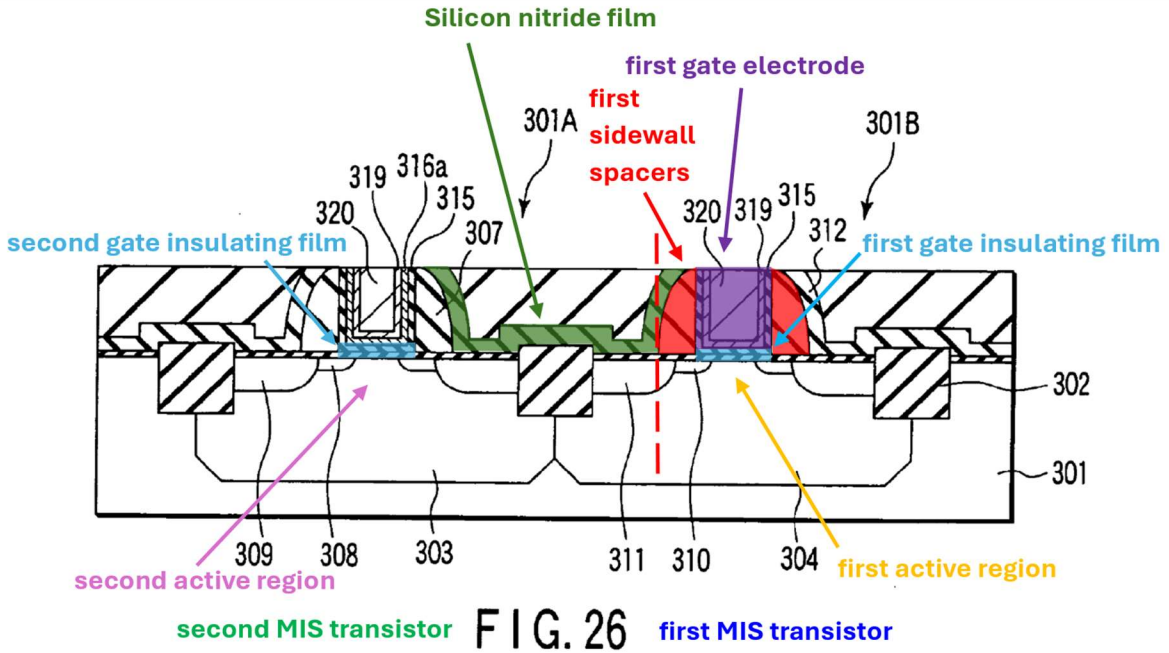
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 FIG. 26
25 [d.2]	a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;	Akasaka '077, as evidenced by the example citations below, discloses a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film.

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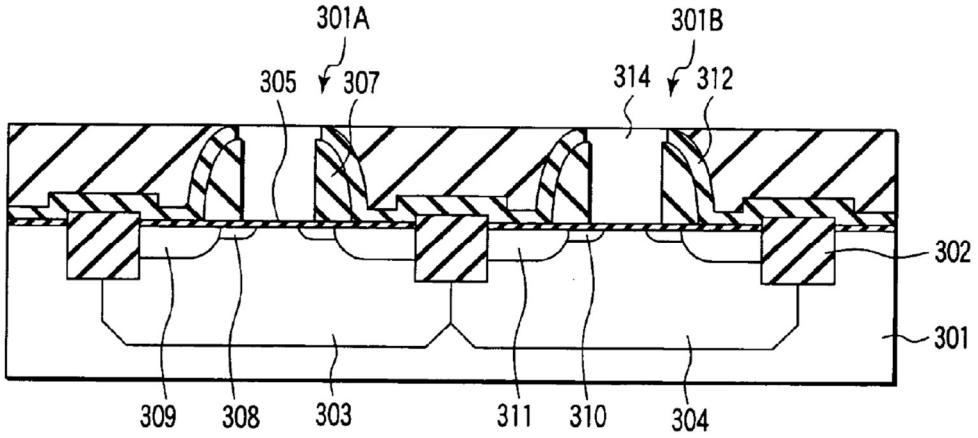
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 FIG. 18 [0076] Then, a TiN conductive film 316 to define the bottom portion of the gate electrode of the p-type MISFET is formed on the gate dielectric film 315 all over the substrate. The conductive film 316 is disposed to control the work function of the gate electrode of the p-type MISFET. Accordingly, the type of the material of the conductive film 316 should be determined in consideration of its work function. [0077] Specifically, in order to decrease the threshold voltage of the p-type MISFET, the material is preferably selected to have a work function close to that of p+-poly-crystalline silicon, such as a work function of 4.8 to 5.3 eV. For example, in the case of a pure metal, a Group-VIII element, such as Ni, Pd, Pt, Co, Rh, or Ru, is preferably used. Alternatively, a metal silicide, a metal nitride, or another compound may be used, as long as it has a metallic band structure with a work function close to that of p+-poly-crystalline silicon. The film thickness of the conductive film 316 is preferably set to be about 5 nm, but it may be set at a very small value of about 1 to 2 nm. In this embodiment, a titanium nitride (TiN) film having a work function of about 4.8 eV is used as the conductive film 316.

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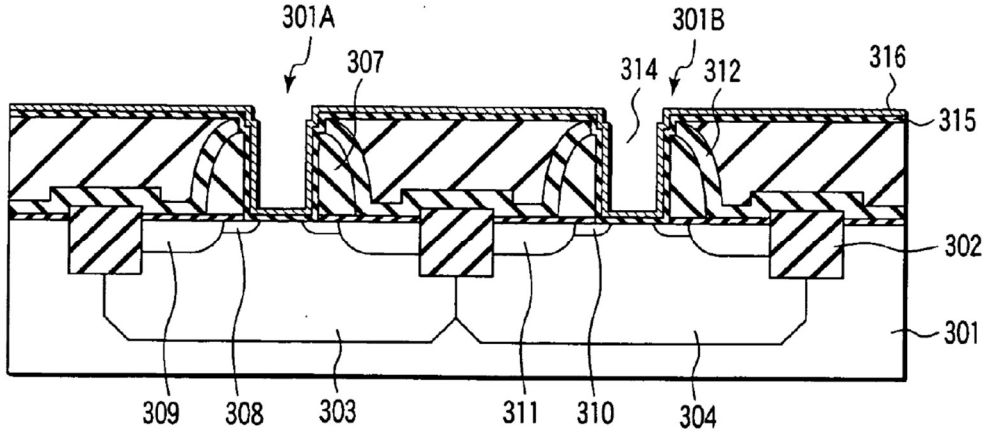
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 FIG. 19 [0078] Then, as shown in FIG. 20, a silicon-containing dielectric (insulating) film is deposited on the conductive film 316 all over the substrate. Further, the surface of the silicon-containing dielectric film is doped with nitrogen to form a reinforced silicon-containing dielectric film 317. The silicon-containing dielectric film used here may be a film selected from the group consisting of a silicon nitride film, a silicon oxynitride film, and a silicon oxide film. Such a film may be formed by CVD using a first process gas containing a silane family gas, and a second process gas containing a gas selected from the group consisting of a nitriding gas, an oxynitriding gas, and an oxidizing gas, as described in the first embodiment. [0079] The reinforced silicon-containing dielectric film 317 is obtained by doping the surface of the silicon-containing dielectric film with nitrogen to nitride only the surface. The step of doping with nitrogen may be performed by a plasma nitriding process, nitrogen ion implantation, or heating process in a nitrogen-containing atmosphere, such as ammonia, as described in the first embodiment. Of them, the plasma nitriding process is preferably used. The plasma nitriding process makes it possible to introduce nitrogen into a very thin surface region at a high concentration with high controllability. In this case, the film can easily be

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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		given a desired wet-etching resistance, and further the film can be easily removed thereafter, as needed, since the portion doped with nitrogen is very thin.

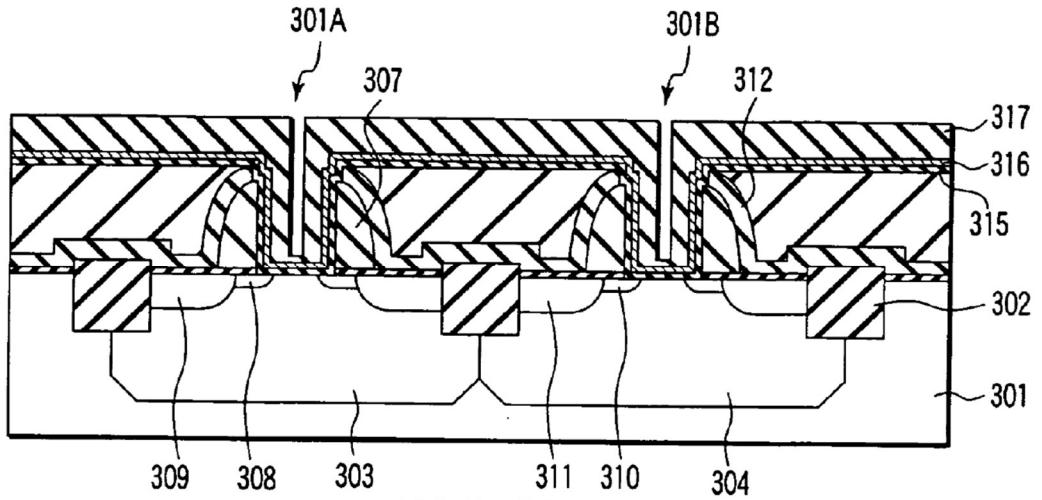

FIG. 20

[0080] Then, as shown in FIG. 21, a photo-resist mask 318 is formed by a photolithography method, so that it covers at least an area where the gate electrode of the p-type MISFET is to be formed. Then, as shown in FIG. 22, the reinforced silicon-containing dielectric film 317 is etched by anisotropic etching, such as RIE, using the photo-resist mask 318. With this step, an etching mask 317 a is formed to cover at least the area where the gate electrode of the p-type MISFET is to be formed. Then, the photo-resist mask 318 is removed. It should be noted that, after the reinforced silicon-containing dielectric film 317 is etched, residues 317 b of the silicon-containing dielectric film 317 remain on the side surface in the recess portion 314 within the second area 301B and so forth.

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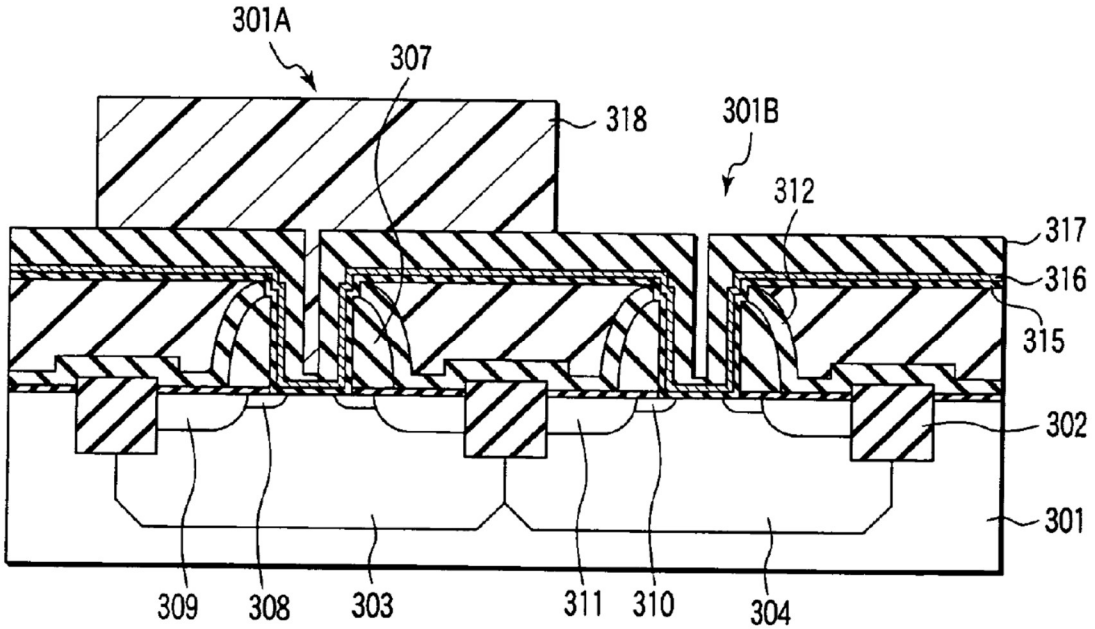
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 FIG. 21

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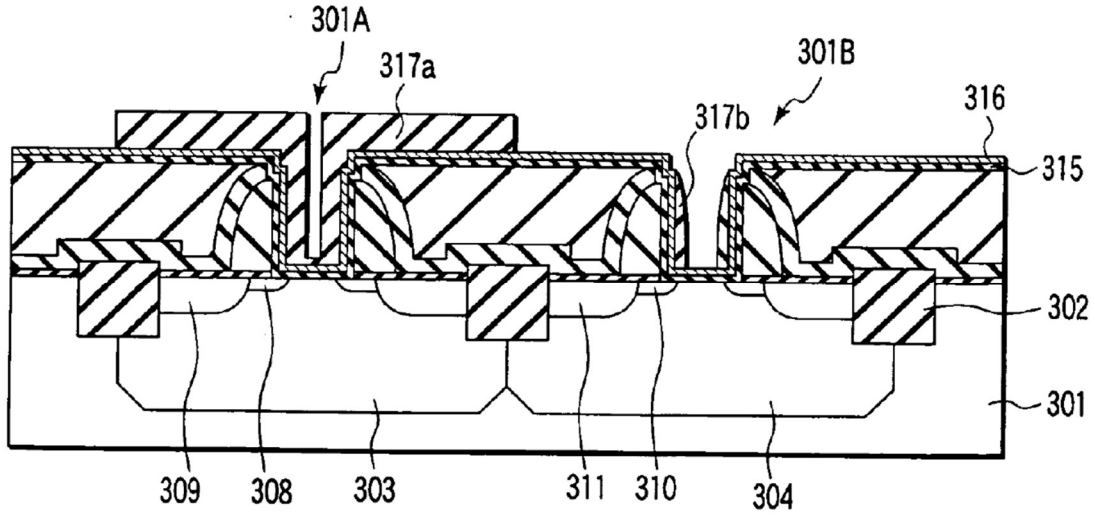
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 FIG. 22 [0081] Then, as shown in FIG. 23, the residues 317 b of the silicon-containing dielectric film 317 are removed by wet etching using a solution containing HF (hydrogen fluoride). In this respect, the residues 317 b do not correspond to the exposed surface layer of the reinforced silicon-containing dielectric film 317, but to the portion thereof undoped with nitrogen. Accordingly, the residues 317 b render a higher wet-etching rate, while the surface layer of the etching mask 317 a renders a lower etching rate, thanks to the nitriding process. Thus, the residues 317 b can be removed while the etching mask 317 a is less etched.

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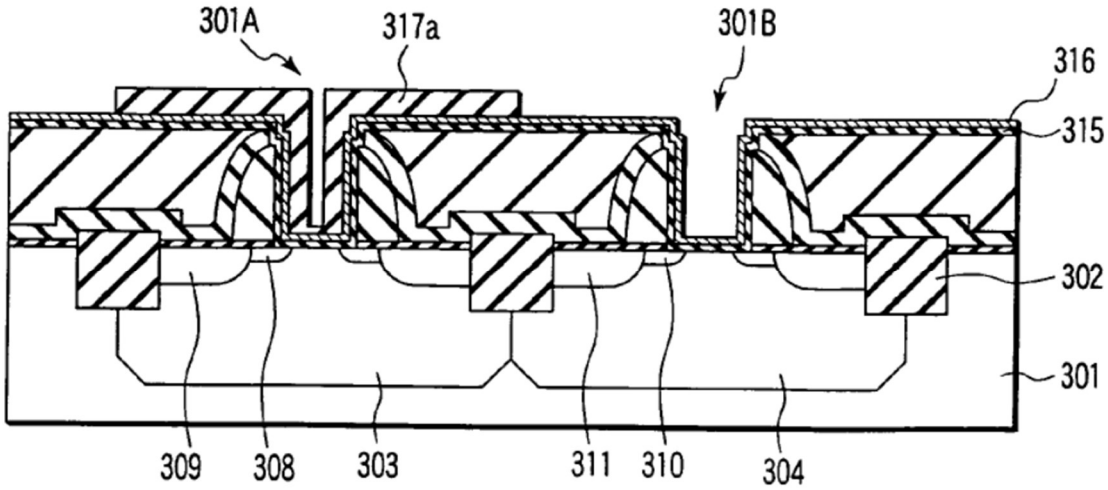
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 FIG. 23 [0082] Then, as shown in FIG. 24, wet etching using a solution of, e.g., H2O2 or a mixture of H2SO4 and H2O2 is performed thorough the etching mask 317 a used as a mask. Consequently, a pre-patterned conductive film 316a is formed by patterning of the conductive film 316. The pre-patterned conductive film 316a is shaped to cover at least that part of the gate dielectric film 315 where the gate electrode of the p-type MISFET is to be formed in the first area 301A. On the other hand, this patterning exposes that part of the gate dielectric film 315 where the gate electrode of the n-type MISFET is to be formed in the second area 301B.

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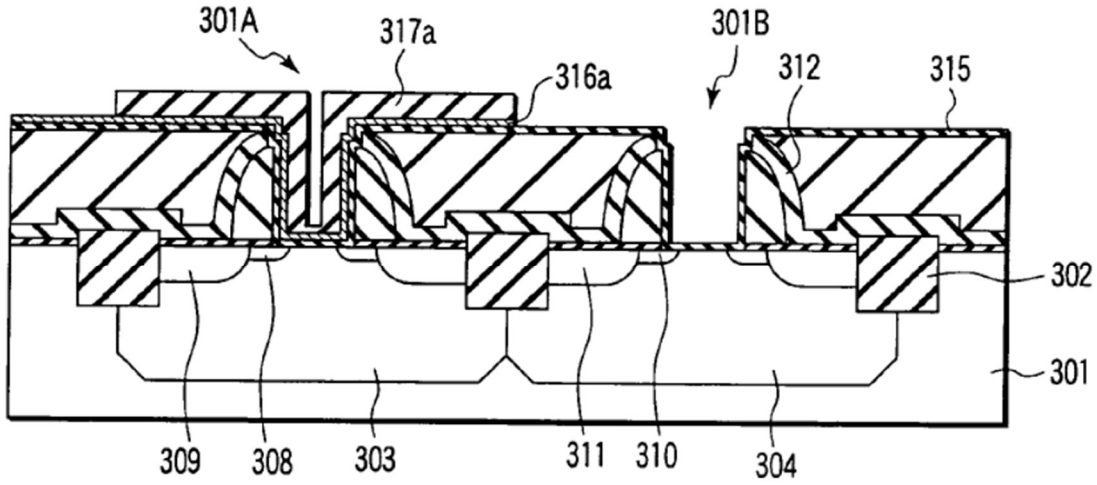
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 FIG. 24 [0083] Then, as shown in FIG. 25, the etching mask 317a is removed, using a solution containing HF and so forth. At this time, the nitrided surface layer of the etching mask has already been removed by etching for removing the residues 317b described above, and thus the remaining portion renders a higher etching rate. This makes it possible to shorten the time during which the gate dielectric film 315 is exposed to the wet etching.

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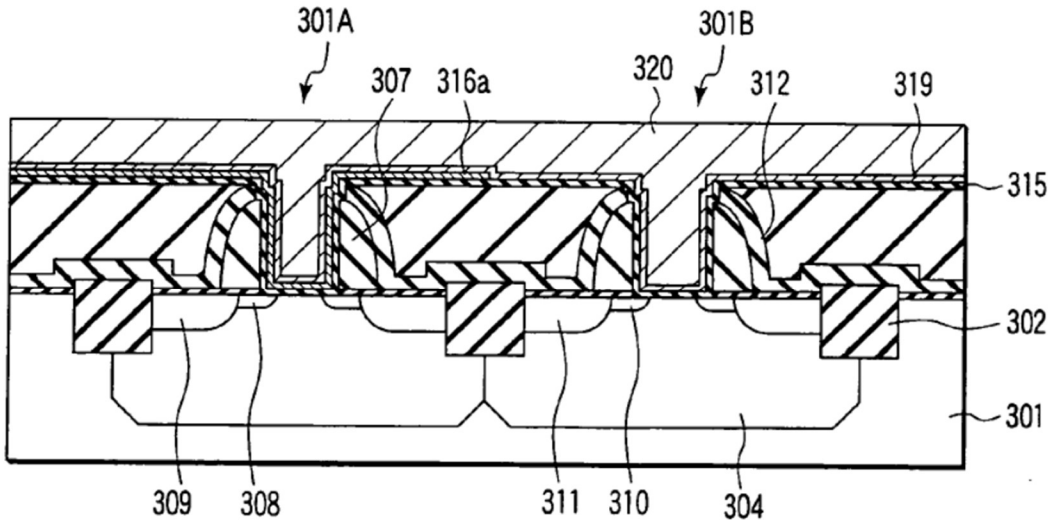
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 FIG. 25 [0084] Then, a conductive film 319 to define the bottom portion of the gate electrode of the n-type MISFET is formed all over the substrate. The conductive film 319 is disposed to control the work function of the gate electrode of the n-type MISFET. Accordingly, the type of the material of the conductive film 319 should also be determined in consideration of its work function. [0085] Specifically, in order to decrease the threshold voltage of the n-type MISFET, the material is preferably selected to have a work function close to that of n+-poly-crystalline silicon, such as a work function of 3.9 to 4.2 eV. For example, in the case of a pure metal, a Group-IVa element, such as Ti, Zr, or Hf, a Group-Va element, such as V, Nb, or Ta, or a Group-VIa element, such as Cr, Mo, or W, is preferably used. Alternatively, a metal silicide, a metal nitride, or another compound may be used, as long as it has a metallic band structure with a work function close to that of n+-poly-crystalline silicon. The film thickness of the conductive film 319 may be set at a very small value of about 1 to 2 nm.

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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		[0086] Then, a conductive film 320 to decrease the resistance of the gate electrode is deposited all over the substrate. The film thickness of the conductive film 320 is preferably set to provide a sheet resistance of about 5Ω/□ or less, such as about 40 to 50 nm in the case of W being used. In this embodiment, the conductive film 319 and conductive film 320 are made of different conductive materials. However, where the material selected for the conductive film 319 has a resistivity almost equal to or less than that required for the conductive film 320 and suitable for the subsequent steps, the conductive film 319 and conductive film 320 are made of one integral film. The conductive film 316 for the gate electrode of the p-type MISFET and the conductive film 319 for the gate electrode of the n-type MISFET may be deposited in an order reverse to that of the embodiment, in consideration of their workability, reactivity, and so forth. [0087] Then, as shown in FIG. 26, a CMP method or the like is used to remove those portions of the insulating film 315 and conductive films 316, 319, and 320 which are deposited outside the recess portions 314. Thereafter, inter-level insulating films, interconnections, and so forth are formed by conventional techniques to complete the MISFETs. The description and annotation below are an example of a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film. For example, as can be seen in Figs. 15-26, Akasaka ’077 discloses forming a gate electrode for the p-type MIS transistor of conductive film 316a on top of gate dielectric (insulating) film 315, conductive film 319, and conductive film 320.

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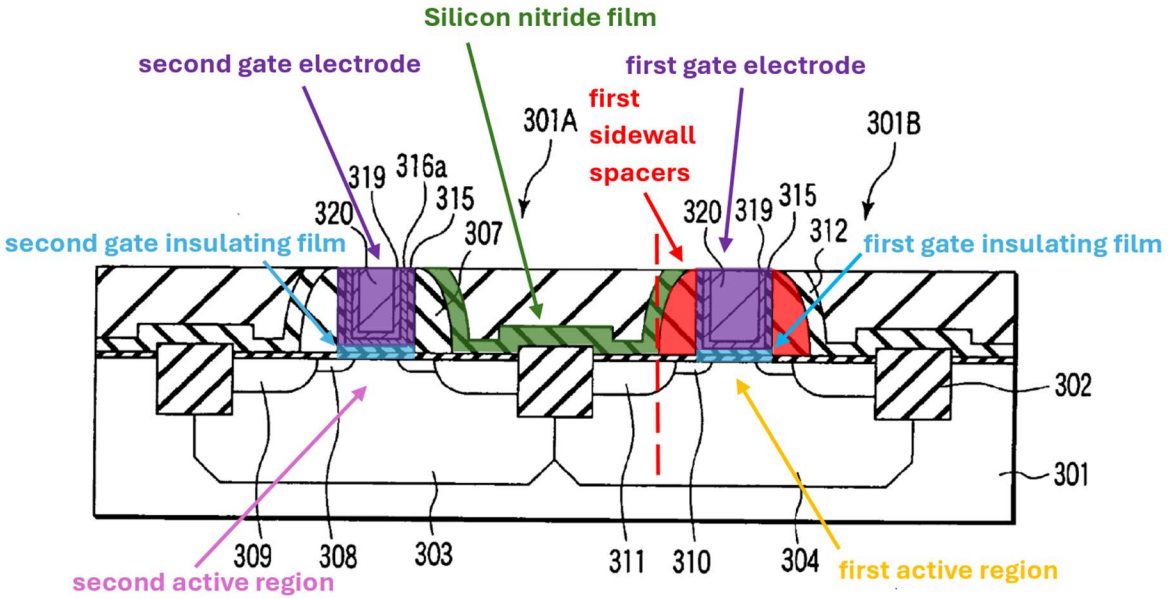
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 FIG. 26
25 [d.3]	second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative; and	Akasaka '077, as evidenced by the example citations below, discloses second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative. [0072] FIGS. 15 to 26 are sectional views showing sequentially ordered steps in a method for manufacturing a semiconductor device according to a second embodiment of the present invention. At first, as shown in FIG. 15, an n-type well 303 and a p-type well 304 are respectively formed in the surface of first and second areas 301A and 301B of a semiconductor substrate 301 consisting mainly of silicon. Further, a device isolation area 302 is formed in the surface of the substrate 301 to surround the first and second areas 301A and 301B. The first and second areas 301A and 301B correspond to areas for forming a p-type MISFET and an n-type MISFET, respectively.

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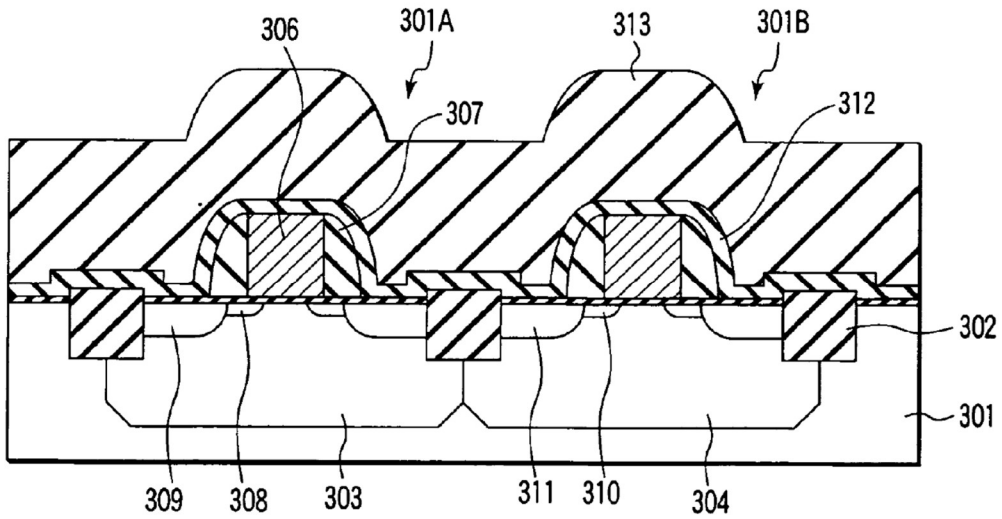
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		[0073] Then, as shown in FIG. 16, a starting structure including a dummy gate electrode made of, e.g., poly-crystalline silicon is formed by conventional techniques for forming transistors. In this starting structure, the source/drain layers 309 and extensions 308 of the p-type MISFET are formed in the n-type well 303 within the first area 301A. Similarly, the source/drain layers 311 and extensions 310 of the n-type MISFET are formed in the p-type well 304 within the second area 301B. Further, a dummy gate electrode 306 made of poly-crystalline silicon is disposed through a dummy gate dielectric (insulating) film 305 formed of a silicon oxide film, at each of predetermined positions on the substrate within the first and second areas 301A and 301B. A gate sidewall 307 formed of an insulating film, such as a silicon nitride film is disposed on the side surface of each dummy gate electrode 306. The dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312 serving as an etching stopper. Further, an inter-level insulating film 313 is disposed on the silicon nitride film 312.  FIG. 16

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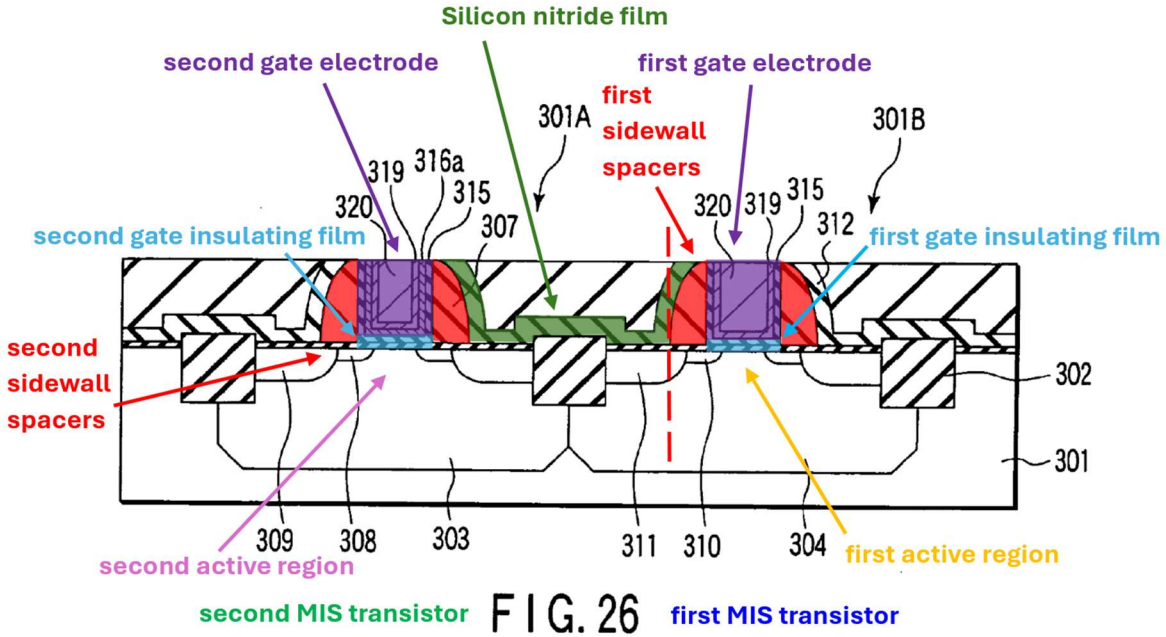
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		The description and annotation below are an example of second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative. For example, as can be seen in Figs. 15-26, Akasaka '077 discloses forming gate sidewall 307 of an insulating film, such as silicon nitride.  FIG. 26

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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
25 [d.4]	the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers,	Akasaka '077, as evidenced by the example citations below, discloses the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers.

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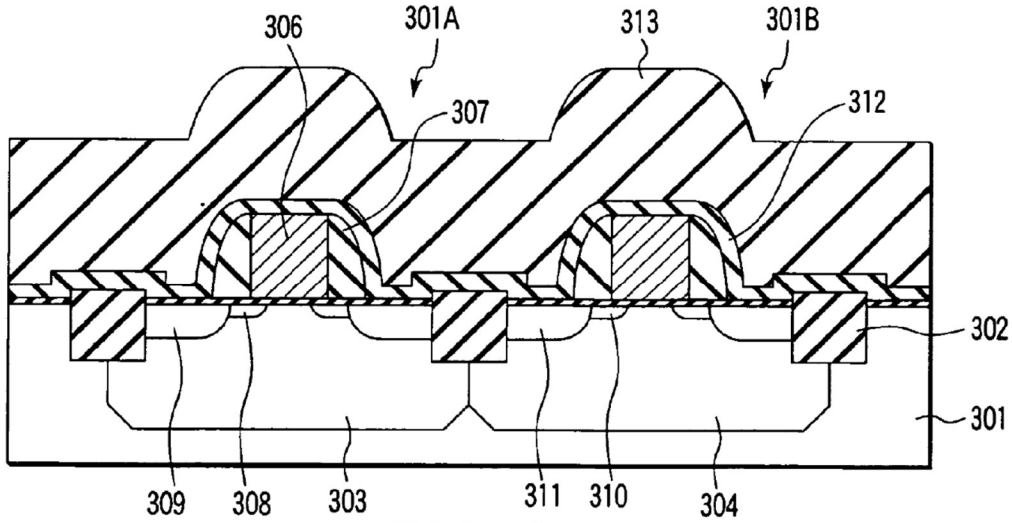
		[0073] Then, as shown in FIG. 16, a starting structure including a dummy gate electrode made of, e.g., poly-crystalline silicon is formed by conventional techniques for forming transistors. In this starting structure, the source/drain layers 309 and extensions 308 of the p-type MISFET are formed in the n-type well 303 within the first area 301A. Similarly, the source/drain layers 311 and extensions 310 of the n-type MISFET are formed in the p-type well 304 within the second area 301B. Further, a dummy gate electrode 306 made of poly-crystalline silicon is disposed through a dummy gate dielectric (insulating) film 305 formed of a silicon oxide film, at each of predetermined positions on the substrate within the first and second areas 301A and 301B. A gate sidewall 307 formed of an insulating film, such as a silicon nitride film is disposed on the side surface of each dummy gate electrode 306. The dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312 serving as an etching stopper. Further, an inter-level insulating film 313 is disposed on the silicon nitride film 312.  FIG. 16

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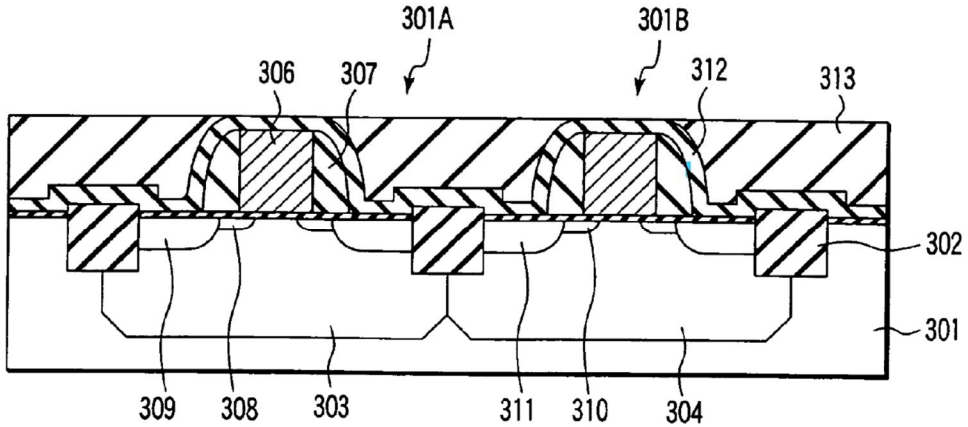
		[0074] Then, as shown in FIG. 17, the inter-level insulating film 313 is polished from above by a CMP (Chemical Mechanical Polishing) method. This step is arranged to expose the upper surface of the dummy gate electrode 306 or the upper surface of the silicon nitride film 312 deposited on the dummy gate electrode 306. Then, as shown in FIG. 18, the exposed silicon nitride film 312 and the dummy gate electrodes are selectively removed to form recess portions 314. Then, as shown in FIG. 19, the portions of the dummy gate dielectric film 305 exposed at the bottom of the recess portions 314 are removed.  FIG. 17

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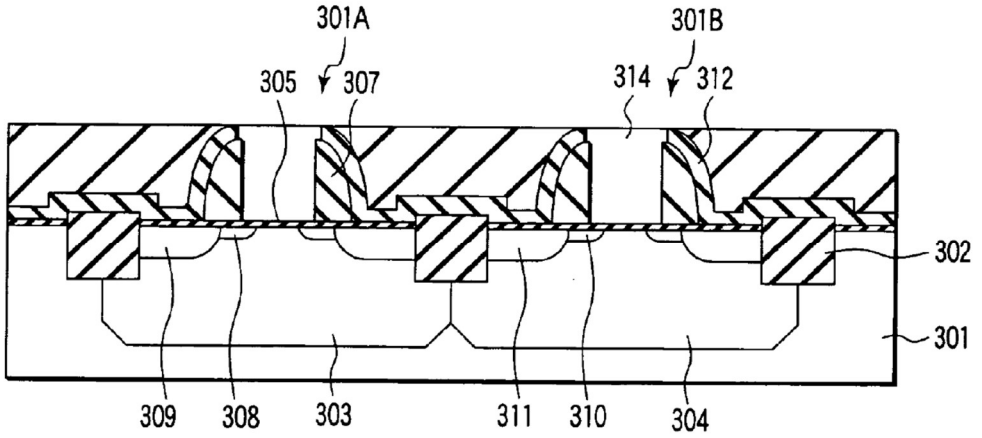
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 FIG. 18 [0087] Then, as shown in FIG. 26, a CMP method or the like is used to remove those portions of the insulating film 315 and conductive films 316, 319, and 320 which are deposited outside the recess portions 314. Thereafter, inter-level insulating films, interconnections, and so forth are formed by conventional techniques to complete the MISFETs. The description and annotation below are an example of the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers. For example, as can be seen in Figs. 15-26, Akasaka '077 discloses forming silicon nitride film 312 over the side surfaces of the gate electrode and sidewall spacers 307 as well as over upper surfaces of regions located in the second active region laterally outside the second sidewall spacer.

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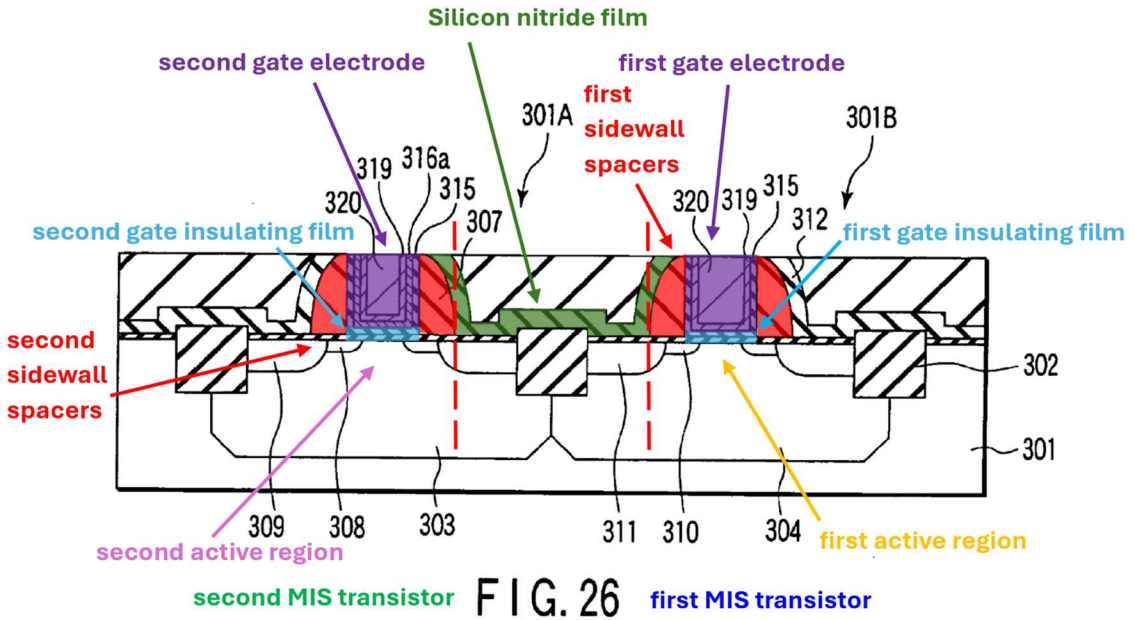
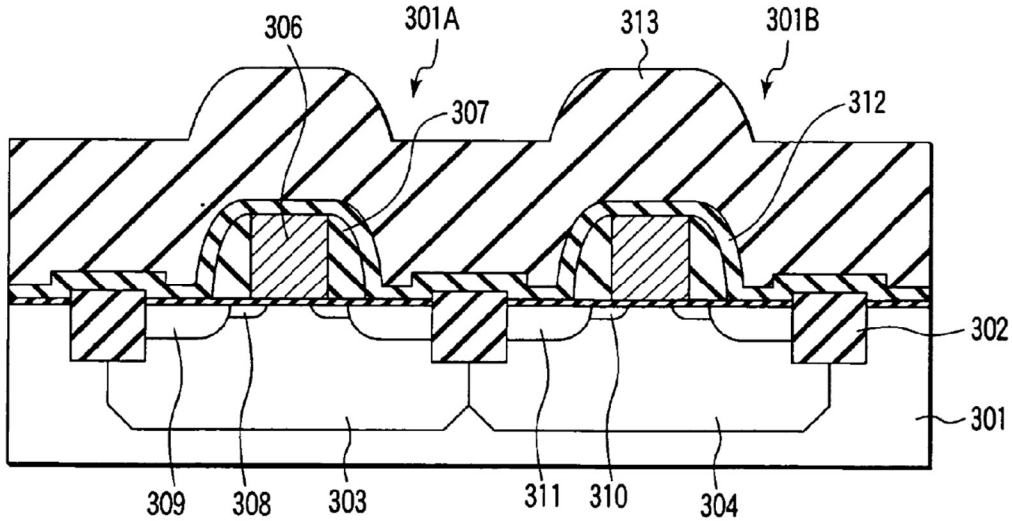
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 FIG. 26
25 [e]	the first and second metal films are made of different metal materials,	Akasaka '077, as evidenced by the example citations below, discloses the first and second metal films are made of different metal materials. Akasaka '077 discloses that the conductive film 316 for the p-type MISFET is preferably TiN and the conductive film 319 for the n-type MISFET is preferably a Group-IVa element, such as Ti, Zr, or Hf, a Group-Va element, such as V, Nb, or Ta, or a Group-VIa element, such as Cr, Mo, or W. [0076] Then, a TiN conductive film 316 to define the bottom portion of the gate electrode of the p-type MISFET is formed on the gate dielectric film 315 all over the substrate. The conductive film 316 is disposed to control the work function of the gate electrode of the p-

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		type MISFET. Accordingly, the type of the material of the conductive film 316 should be determined in consideration of its work function. [0077] Specifically, in order to decrease the threshold voltage of the p-type MISFET, the material is preferably selected to have a work function close to that of p+-poly-crystalline silicon, such as a work function of 4.8 to 5.3 eV. For example, in the case of a pure metal, a Group-VIII element, such as Ni, Pd, Pt, Co, Rh, or Ru, is preferably used. Alternatively, a metal silicide, a metal nitride, or another compound may be used, as long as it has a metallic band structure with a work function close to that of p+-poly-crystalline silicon. The film thickness of the conductive film 316 is preferably set to be about 5 nm, but it may be set at a very small value of about 1 to 2 nm. In this embodiment, a titanium nitride (TiN) film having a work function of about 4.8 eV is used as the conductive film 316. [0084] Then, a conductive film 319 to define the bottom portion of the gate electrode of the n-type MISFET is formed all over the substrate. The conductive film 319 is disposed to control the work function of the gate electrode of the n-type MISFET. Accordingly, the type of the material of the conductive film 319 should also be determined in consideration of its work function. [0085] Specifically, in order to decrease the threshold voltage of the n-type MISFET, the material is preferably selected to have a work function close to that of n+-poly-crystalline silicon, such as a work function of 3.9 to 4.2 eV. For example, in the case of a pure metal, a Group-IVa element, such as Ti, Zr, or Hf, a Group-Va element, such as V, Nb, or Ta, or a Group-VIa element, such as Cr, Mo, or W, is preferably used. Alternatively, a metal silicide, a metal nitride, or another compound may be used, as long as it has a metallic band structure with a work function close to that of n+-poly-crystalline silicon. The film thickness of the conductive film 319 may be set at a very small value of about 1 to 2 nm.

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
25 [f]	the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes, and the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region.	Akasaka '077, as evidenced by the example citations below, discloses the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes, and the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region. [0073] Then, as shown in FIG. 16, a starting structure including a dummy gate electrode made of, e.g., poly-crystalline silicon is formed by conventional techniques for forming transistors. In this starting structure, the source/drain layers 309 and extensions 308 of the p-type MISFET are formed in the n-type well 303 within the first area 301A. Similarly, the source/drain layers 311 and extensions 310 of the n-type MISFET are formed in the p-type well 304 within the second area 301B. Further, a dummy gate electrode 306 made of poly-crystalline silicon is disposed through a dummy gate dielectric (insulating) film 305 formed of a silicon oxide film, at each of predetermined positions on the substrate within the first and second areas 301A and 301B. A gate sidewall 307 formed of an insulating film, such as a silicon nitride film is disposed on the side surface of each dummy gate electrode 306. The dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312

		serving as an etching stopper. Further, an inter-level insulating film 313 is disposed on the silicon nitride film 312.  FIG. 16 [0074] Then, as shown in FIG. 17, the inter-level insulating film 313 is polished from above by a CMP (Chemical Mechanical Polishing) method. This step is arranged to expose the upper surface of the dummy gate electrode 306 or the upper surface of the silicon nitride film 312 deposited on the dummy gate electrode 306. Then, as shown in FIG. 18, the exposed silicon nitride film 312 and the dummy gate electrodes are selectively removed to form recess portions 314. Then, as shown in FIG. 19, the portions of the dummy gate dielectric film 305 exposed at the bottom of the recess portions 314 are removed.

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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.

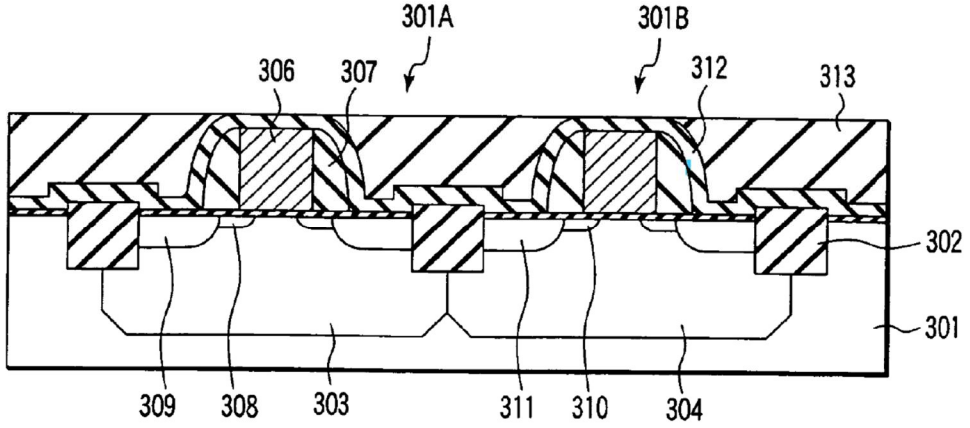

FIG. 17

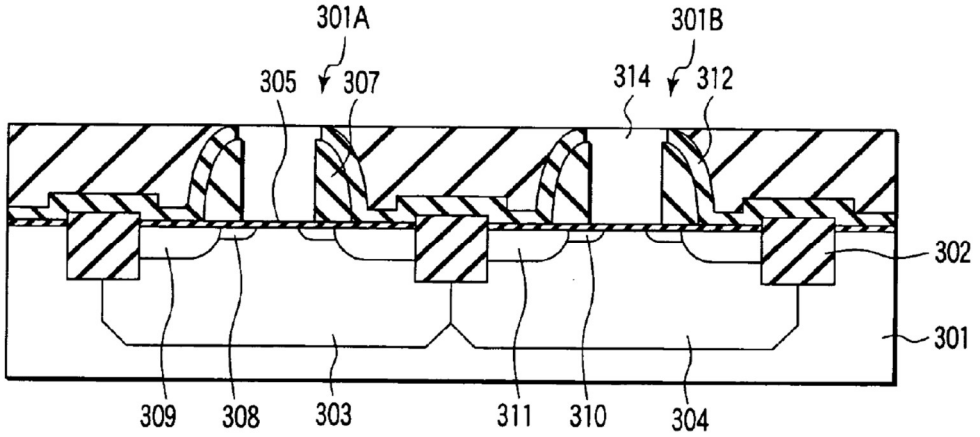

FIG. 18

[0087] Then, as shown in FIG. 26, a CMP method or the like is used to remove those portions of the insulating film 315 and conductive films 316, 319, and 320 which are deposited outside the recess portions 314. Thereafter, inter-level insulating films,

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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		interconnections, and so forth are formed by conventional techniques to complete the MISFETs. Akasaka '077's silicon nitride layer causes a first stress in a gate length direction of a channel region in the first active region due to the same reasons alleged against the accused product, e.g. due to intrinsic deposition stress, thermal mismatch, and/or lattice mismatch.
26	The semiconductor device of claim 25, wherein the first metal film has a thickness smaller than that of the second metal film.	Akasaka '077, as evidenced by the example citations below, discloses the first metal film has a thickness smaller than that of the second metal film. Akasaka '077 discloses that the conductive film 316 for the p-type MISFET is preferably TiN at 5nm thick, but may also be between 1 to 2nm. Akasaka '077 also discloses the conductive film 319 for the n-type MISFET is preferably a Group-IVa element, such as Ti, Zr, or Hf, a Group-Va element, such as V, Nb, or Ta, or a Group-VIa element, such as Cr, Mo, or W of about 1 to 2nm. [0076] Then, a TiN conductive film 316 to define the bottom portion of the gate electrode of the p-type MISFET is formed on the gate dielectric film 315 all over the substrate. The conductive film 316 is disposed to control the work function of the gate electrode of the p-type MISFET. Accordingly, the type of the material of the conductive film 316 should be determined in consideration of its work function. [0077] Specifically, in order to decrease the threshold voltage of the p-type MISFET, the material is preferably selected to have a work function close to that of p+-poly-crystalline silicon, such as a work function of 4.8 to 5.3 eV. For example, in the case of a pure metal, a Group-VIII element, such as Ni, Pd, Pt, Co, Rh, or Ru, is preferably used. Alternatively, a metal silicide, a metal nitride, or another compound may be used, as long as it has a metallic band structure with a work function close to that of p+-poly-crystalline silicon. The film thickness of the conductive film 316 is preferably set to be about 5 nm, but it may be set at a very small value of about 1 to 2 nm. In this embodiment, a titanium nitride (TiN) film having a work function of about 4.8 eV is used as the conductive film 316.

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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		[0084] Then, a conductive film 319 to define the bottom portion of the gate electrode of the n-type MISFET is formed all over the substrate. The conductive film 319 is disposed to control the work function of the gate electrode of the n-type MISFET. Accordingly, the type of the material of the conductive film 319 should also be determined in consideration of its work function. [0085] Specifically, in order to decrease the threshold voltage of the n-type MISFET, the material is preferably selected to have a work function close to that of n+-poly-crystalline silicon, such as a work function of 3.9 to 4.2 eV. For example, in the case of a pure metal, a Group-IVa element, such as Ti, Zr, or Hf, a Group-Va element, such as V, Nb, or Ta, or a Group-VIa element, such as Cr, Mo, or W, is preferably used. Alternatively, a metal silicide, a metal nitride, or another compound may be used, as long as it has a metallic band structure with a work function close to that of n+-poly-crystalline silicon. The film thickness of the conductive film 319 may be set at a very small value of about 1 to 2 nm.
27	The semiconductor device of claim 25, wherein the first and second metal films have different work functions.	Akasaka '077, as evidenced by the example citations below, discloses the first and second metal films have different work functions. Akasaka '077 discloses that the conductive film 316 for the p-type MISFET preferably has a work function of 4.8 to 5.3 eV. Akasaka '077 also discloses the conductive film 319 for the n-type MISFET preferably has a work function of 3.9 to 4.2 eV. [0076] Then, a TiN conductive film 316 to define the bottom portion of the gate electrode of the p-type MISFET is formed on the gate dielectric film 315 all over the substrate. The conductive film 316 is disposed to control the work function of the gate electrode of the p-type MISFET. Accordingly, the type of the material of the conductive film 316 should be determined in consideration of its work function. [0077] Specifically, in order to decrease the threshold voltage of the p-type MISFET, the material is preferably selected to have a work function close to that of p+-poly-crystalline silicon, such as a work function of 4.8 to 5.3 eV. For example, in the case of a pure metal, a Group-VIII element, such as Ni, Pd, Pt, Co, Rh, or Ru, is preferably used. Alternatively, a

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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		metal silicide, a metal nitride, or another compound may be used, as long as it has a metallic band structure with a work function close to that of p+-poly-crystalline silicon. The film thickness of the conductive film 316 is preferably set to be about 5 nm, but it may be set at a very small value of about 1 to 2 nm. In this embodiment, a titanium nitride (TiN) film having a work function of about 4.8 eV is used as the conductive film 316. [0084] Then, a conductive film 319 to define the bottom portion of the gate electrode of the n-type MISFET is formed all over the substrate. The conductive film 319 is disposed to control the work function of the gate electrode of the n-type MISFET. Accordingly, the type of the material of the conductive film 319 should also be determined in consideration of its work function. [0085] Specifically, in order to decrease the threshold voltage of the n-type MISFET, the material is preferably selected to have a work function close to that of n+-poly-crystalline silicon, such as a work function of 3.9 to 4.2 eV. For example, in the case of a pure metal, a Group-IVa element, such as Ti, Zr, or Hf, a Group-Va element, such as V, Nb, or Ta, or a Group-VIa element, such as Cr, Mo, or W, is preferably used. Alternatively, a metal silicide, a metal nitride, or another compound may be used, as long as it has a metallic band structure with a work function close to that of n+-poly-crystalline silicon. The film thickness of the conductive film 319 may be set at a very small value of about 1 to 2 nm.
28	The semiconductor device of claim 25, wherein the silicon nitride film has a thickness smaller than that of the first gate electrode.	Akasaka '077, as evidenced by the example citations below, discloses the silicon nitride film has a thickness smaller than that of the first gate electrode. [0073] Then, as shown in FIG. 16, a starting structure including a dummy gate electrode made of, e.g., poly-crystalline silicon is formed by conventional techniques for forming transistors. In this starting structure, the source/drain layers 309 and extensions 308 of the p-type MISFET are formed in the n-type well 303 within the first area 301A. Similarly, the source/drain layers 311 and extensions 310 of the n-type MISFET are formed in the p-type well 304 within the second area 301B. Further, a dummy gate electrode 306 made of poly-crystalline silicon is disposed through a dummy gate dielectric (insulating) film 305 formed of a silicon oxide film, at each of predetermined positions on the substrate within the first

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and second areas 301A and 301B. A gate sidewall 307 formed of an insulating film, such as a silicon nitride film is disposed on the side surface of each dummy gate electrode 306. The dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312 serving as an etching stopper. Further, an inter-level insulating film 313 is disposed on the silicon nitride film 312.

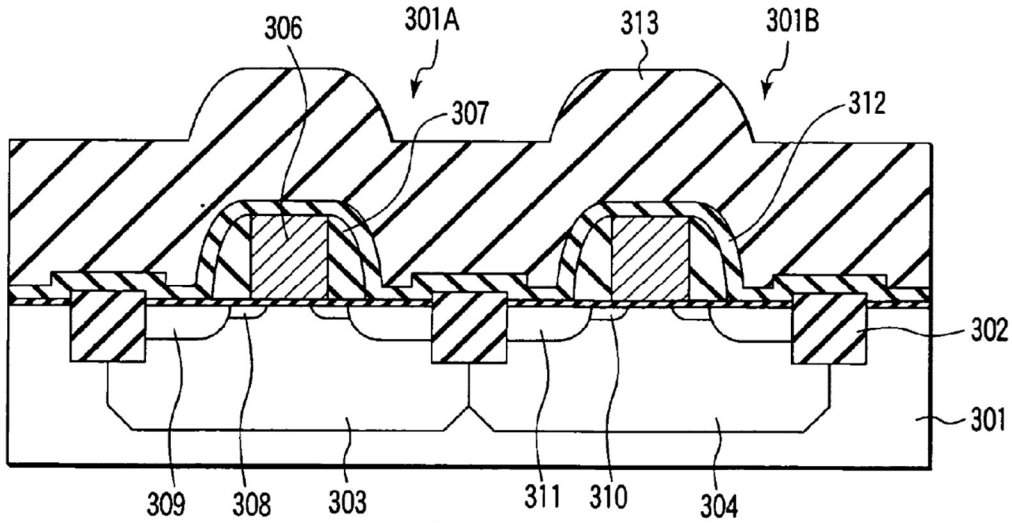

FIG. 16

[0074] Then, as shown in FIG. 17, the inter-level insulating film 313 is polished from above by a CMP (Chemical Mechanical Polishing) method. This step is arranged to expose the upper surface of the dummy gate electrode 306 or the upper surface of the silicon nitride film 312 deposited on the dummy gate electrode 306. Then, as shown in FIG. 18, the exposed silicon nitride film 312 and the dummy gate electrodes are selectively removed to form recess portions 314. Then, as shown in FIG. 19, the portions of the dummy gate dielectric film 305 exposed at the bottom of the recess portions 314 are removed.

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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.

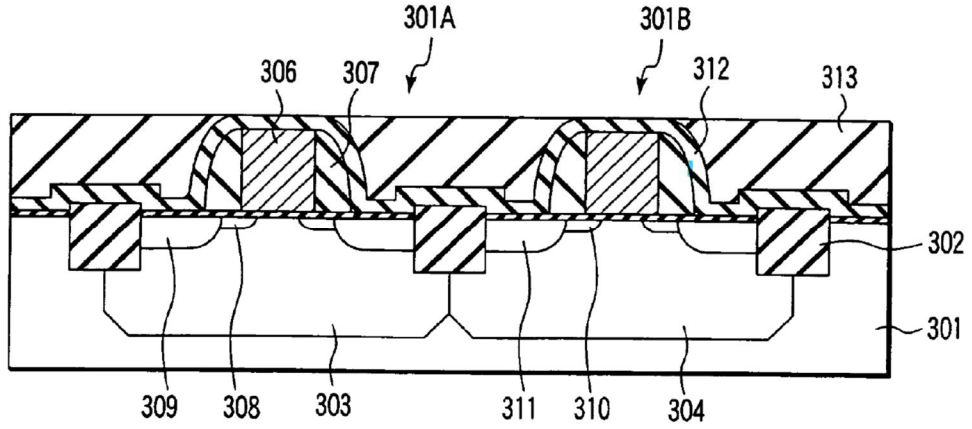

FIG. 17

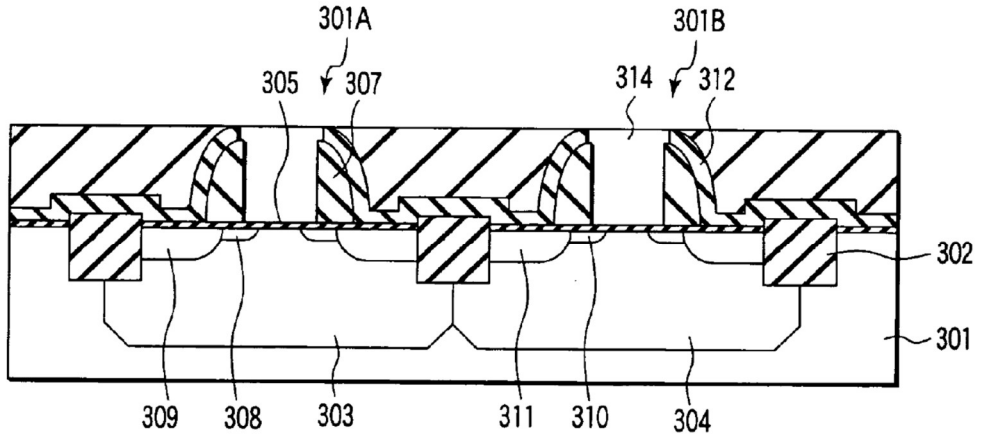

FIG. 18

[0087] Then, as shown in FIG. 26, a CMP method or the like is used to remove those portions of the insulating film 315 and conductive films 316, 319, and 320 which are deposited outside the recess portions 314. Thereafter, inter-level insulating films,

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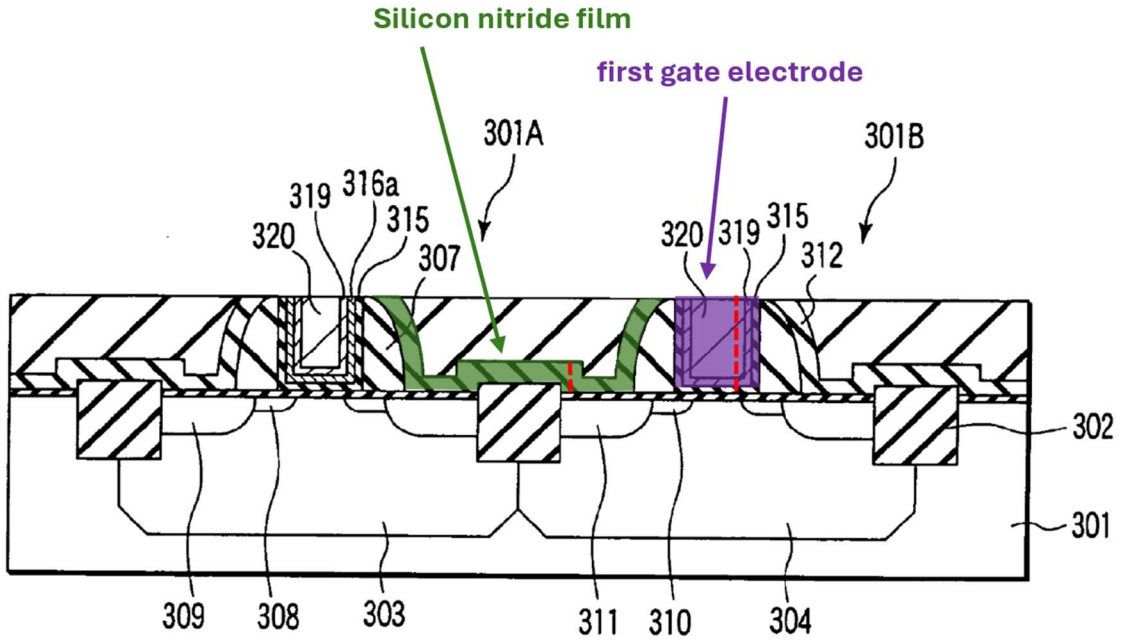
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		interconnections, and so forth are formed by conventional techniques to complete the MISFETs. The description and annotation below are an example of the silicon nitride film having a thickness smaller than that of the first gate electrode  FIG. 26 first MIS transistor

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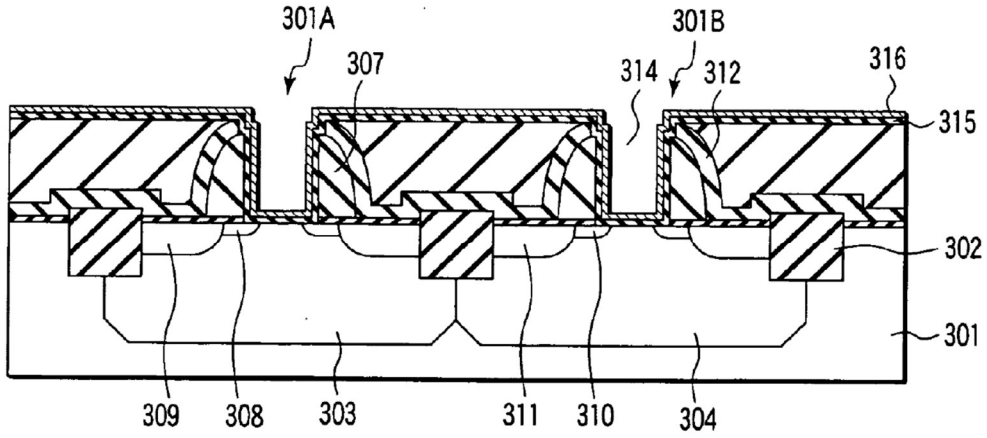
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
31	The semiconductor device of claim 25, wherein the first and second gate insulating films are made of the same insulating material.	Akasaka '077, as evidenced by the example citations below, discloses the first and second gate insulating films are made of the same insulating material. [0075] Then, a gate dielectric (insulating) film 315 is deposed all over the substrate to cover the inner surface of the recess portions 314. The gate dielectric film 315 may be preferably made of a film of HfO2, HfSixOy, HfAlxOy, or SiO2 doped with nitrogen. The film thickness of the gate dielectric film 315 is preferably set to agree with an effective film thickness (EOT) of 1.5 nm or less, to manufacture a MISFET having a gate length of 100 nm or less. EOT is expressed by a value converted into the thickness of a silicon oxide film having an equivalent gate capacity.  FIG. 19

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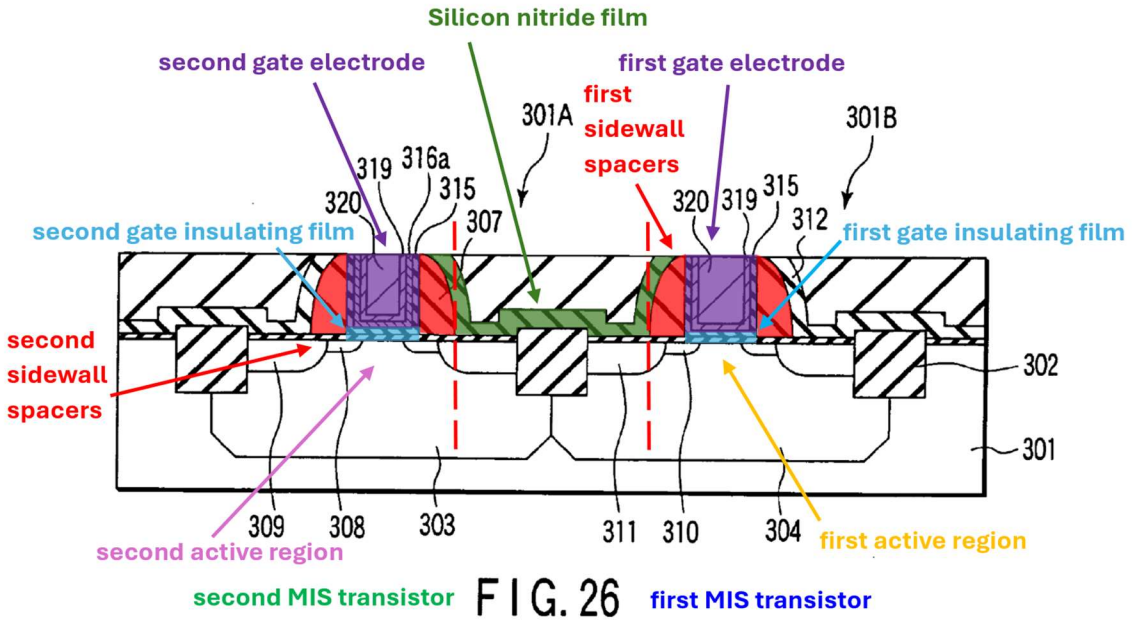
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 FIG. 26
35	The semiconductor device of claim 25, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.	Akasaka '077, as evidenced by the example citations below, discloses the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more. [0075] Then, a gate dielectric (insulating) film 315 is deposed all over the substrate to cover the inner surface of the recess portions 314. The gate dielectric film 315 may be preferably made of a film of HfO2, HfSixOy, HfAlxOy, or SiO2 doped with nitrogen. The film thickness of the gate dielectric film 315 is preferably set to agree with an effective film thickness (EOT) of 1.5 nm or less, to manufacture a MISFET having a gate length of 100 nm or less. EOT is expressed by a value converted into the thickness of a silicon oxide film having an equivalent gate capacity.

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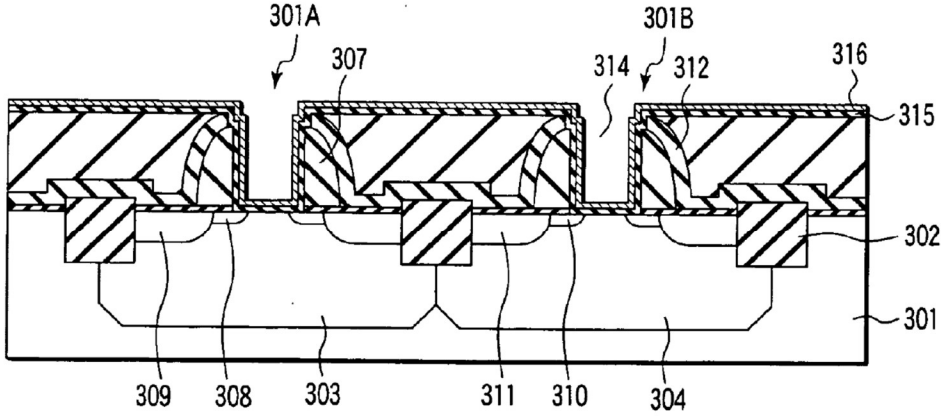
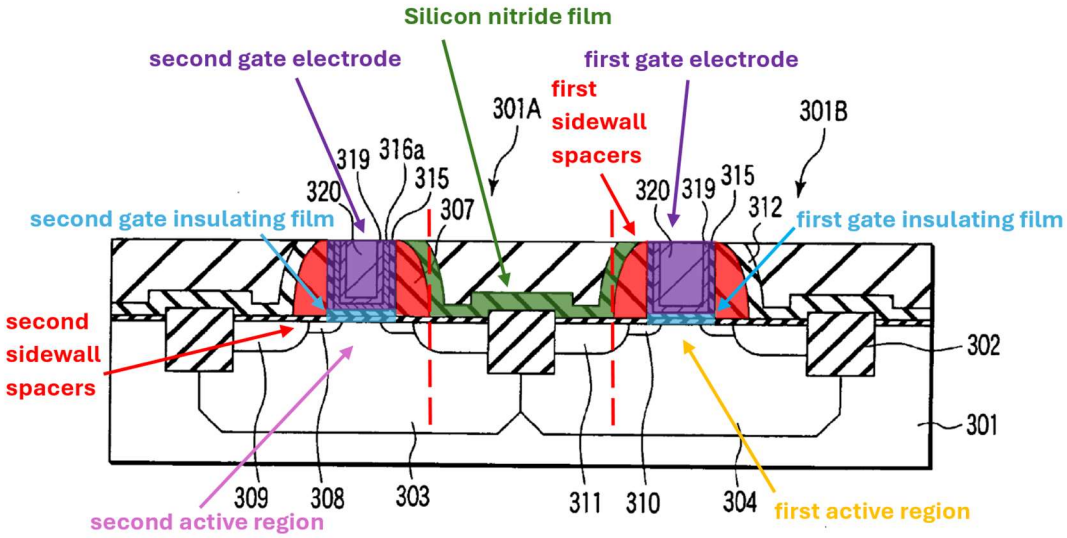
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al.
		 FIG. 19  FIG. 26

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