

EXHIBIT 686A2

Invalidity of U.S. Patent No. 8,198,686 in View of U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama

U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama was filed as Application No. 11/723,226 on March 19, 2007, and published on September 20, 2007, as demonstrated by at least the document itself, the records of the United States Patent and Trademark Office, and/or the testimony of knowledgeable witnesses and corroborating documents. Aoyama is therefore prior art to the '686 Patent under at least 35 U.S.C. § 102(a), (b), and/or (e) as discussed in greater detail in the chart that follows.¹

To the extent that AICP alleges that Aoyama does not disclose any particular limitation of claims 25, 26, 27, 28, 31, and 35 (the “Asserted Claims”) of the '686 Patent, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the priority date of the '686 Patent to modify Aoyama and/or combine the teachings of Aoyama with other prior art references, including but not limited to, the other prior art references in Exhibits 686A1-5 and 686B, and the relevant sections of the charts for other prior art to the '686 Patent in a manner that would have rendered the Asserted Claim invalid as obvious.

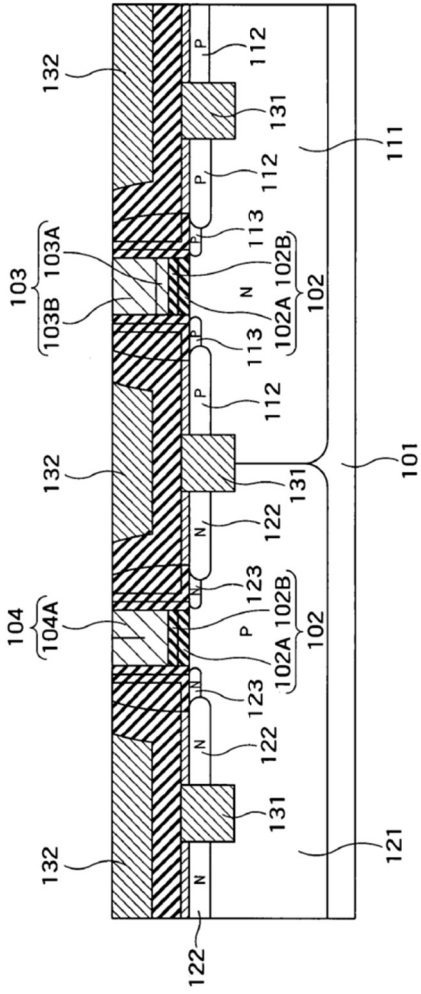
Defendants reserve the right to amend or supplement this claim chart at a later date as more fully set forth in the Preliminary Invalidation Contentions. The cited portions of the prior art references are merely illustrative, and Defendants reserve the right to rely on alternative or additional evidence, including uncited portions of the prior art references.

¹ These preliminary invalidity charts, in some instances, rely, at least in part, on AICP's apparent positions regarding the scope of its claims for purposes of asserting infringement. Defendants' assertion that a particular limitation is disclosed by a prior art reference, or Defendants' assertion that a particular limitation is disclosed by a prior art reference in a particular manner, may be based in part on AICP's apparent claim interpretations. In relying in part on AICP's apparent claim interpretations, Defendants do not admit that AICP's apparent claim interpretations are supportable or proper or that the claim limitations in question are definite or otherwise amenable to construction. Nor do Defendants admit that the claims are enabled, adequately described, or cover patentable subject matter, or that any of the Accused Instrumentalities infringe any claim of the Asserted Patents. Nor shall anything stated herein be construed as an admission or waiver of any particular construction of any claim term, or argument under 35 U.S.C. § 112. Nothing in these claim charts should be understood as an admission relating to infringement, either literally or under the doctrine of equivalents, or as an admission relating to the Defendants' understanding of the proper interpretation or scope of the Asserted Claim. Moreover, Defendants reserve the right to rely on additional citations or sources of evidence that may also be applicable, or that may become applicable in light of any Court order on claim construction, changes in AICP's Preliminary Infringement Contentions, or information obtained during discovery as the case proceeds.

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Where the chart below states that the reference “discloses” or “describes” or “teaches” a limitation, such disclosure may be express, inherent, or implicit. Unless otherwise indicated, all citations to other claim charts in the discussion of claim elements below refer specifically to the corresponding claim element of the other claim chart.

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
25 [pre]	A semiconductor device comprising:	<p>Aoyama, as evidenced by the example citations below, discloses a semiconductor device.</p> <p>[0003] The present invention relates to a semiconductor device and a manufacturing method thereof, for example, to a semiconductor device which includes a PMOSFET and an NMOSFET which are constituted by high-permittivity gate dielectric films (high-k gate dielectric films) and metal gate electrodes, and a manufacturing method thereof.</p> <p>[0005] The currently most widely used transistors are FETs (Field Effect Transistors) such as MOSFETs. Among them, a CMOSFET (Complementary MOSFET) constituted by a PMOSFET (P-channel MOSFET) and an NMOSFET (N-channel MOSFET) is particularly widely used.</p> <p>[0038] FIG. 1 is a side sectional view showing a semiconductor device according to a first embodiment. The semiconductor device in FIG. 1 includes a PMOSFET which is a specific example of a P-type FET and an NMOSFET which is a specific example of an N-type FET. The semiconductor device in FIG. 1 includes a CMOSFET which is constituted by the PMOSFET and the NMOSFET.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="735 913 768 1014">FIG. 1</p> <p data-bbox="797 216 976 1501">[0071] FIG. 3 is a side sectional view showing a semiconductor device according to the second embodiment. The semiconductor device in FIG. 3 includes a PMOSFET which is a specific example of a P-type FET and an NMOSFET which is a specific example of an N-type FET. The semiconductor device in FIG. 3 includes a CMOSFET which is constituted by the PMOSFET and the NMOSFET.</p>

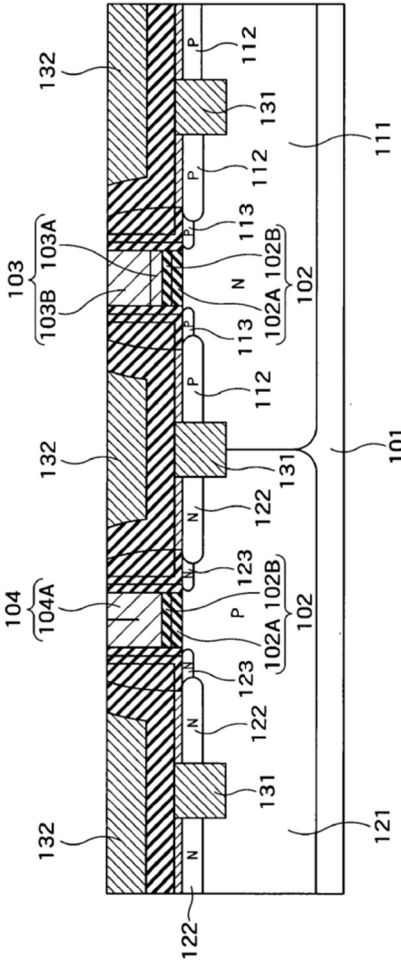
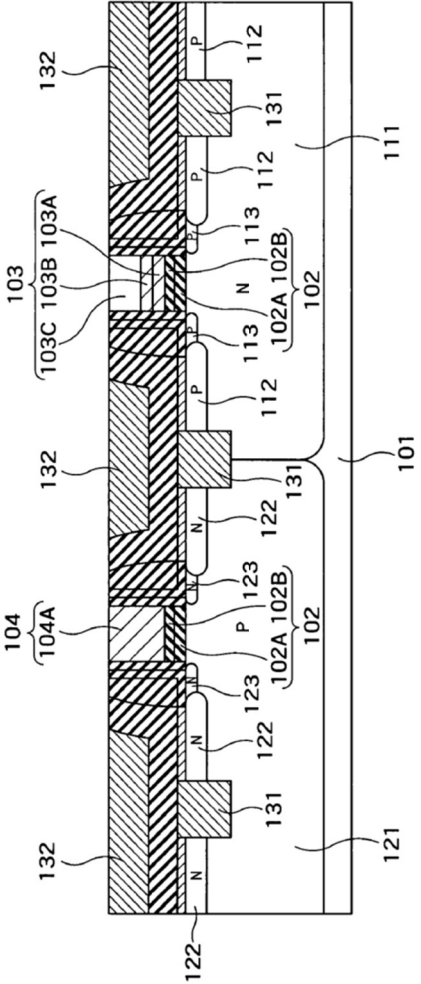
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p style="text-align: center;">FIG. 3</p> <p>[0097] FIG. 5 is a side sectional view showing a semiconductor device according to a third embodiment. The semiconductor device in FIG. 5 includes a PMOSFET which is a specific example of a P-type FET and an NMOSFET which is a specific example of an N-type FET. The semiconductor device in FIG. 5 includes a CMOSFET which is constituted by the PMOSFET and the NMOSFET.</p>

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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
25 [a]	a first MIS transistor; and	 <p>FIG. 5</p> <p>Aoyama, as evidenced by the example citations below, discloses a first MIS transistor.</p> <p>[0039] The semiconductor device shown in FIG. 1 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer 103A which is made of conductive metal and a second conductive layer 103B which is made of conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment</p>

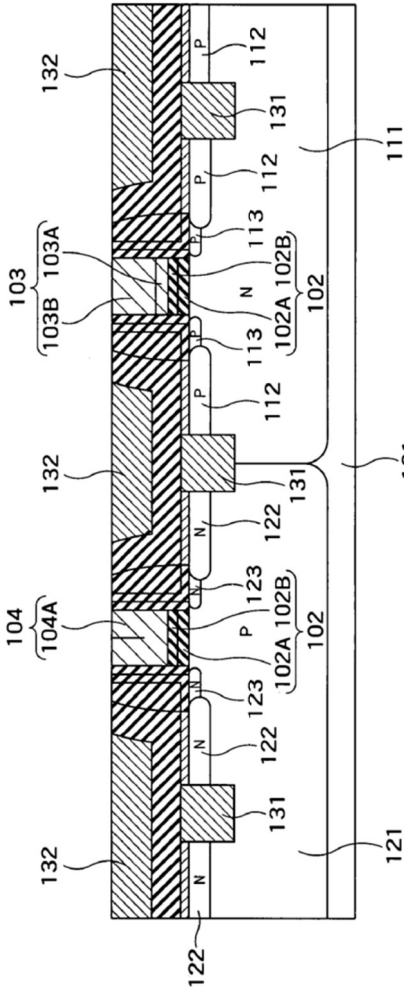
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p> <p>[0040] Additionally, the semiconductor device shown in FIG. 1 has, as diffusion layers for the PMOSFET, a well diffusion layer 111 for the PMOSFET, a source/drain diffusion layer 112 for the PMOSFET, and an extension diffusion layer 113 for the PMOSFET. The well diffusion layer 111 is an N-type diffusion layer, the source/drain diffusion layer 112 is a P-type diffusion layer, and the extension diffusion layer 113 is a P-type diffusion layer.</p> <p>[0041] Additionally, the semiconductor device shown in FIG. 1 has, as diffusion layers for the NMOSFET, a well diffusion layer 121 for the NMOSFET, a source/drain diffusion layer 122 for the NMOSFET, and an extension diffusion layer 123 for the NMOSFET. The well diffusion layer 121 is a P-type diffusion layer, the source/drain diffusion layer 122 is an N-type diffusion layer, and the extension diffusion layer 123 is an N-type diffusion layer.</p>  <p>FIG. 1</p> <p>[0072] The semiconductor device shown in FIG. 3 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate</p>

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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer 103A which is made of conductive metal and a second conductive layer 103B which is made of conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p> <p>[0073] Additionally, the semiconductor device shown in FIG. 3 has, as diffusion layers for the PMOSFET, a well diffusion layer 111 for the PMOSFET, a source/drain diffusion layer 112 for the PMOSFET, and an extension diffusion layer 113 for the PMOSFET.</p> <p>[0074] Additionally, the semiconductor device shown in FIG. 3 has, as diffusion layers for the NMOSFET, a well diffusion layer 121 for the NMOSFET, a source/drain diffusion layer 122 for the NMOSFET, and an extension diffusion layer 123 for the NMOSFET.</p>

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		<div data-bbox="289 520 695 1476"> </div> <p data-bbox="743 915 776 1020">FIG. 3</p> <p data-bbox="846 189 1393 1501">[0098] The semiconductor device shown in FIG. 5 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the NMOSFET in this embodiment includes three electrode-constituting layers: a first conductive layer 103A which is made of conductive metal, a second conductive layer 103B which is made of conductive metal, and a semiconductor layer 103C which is made of semiconductor. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>[0099] Additionally, the semiconductor device shown in FIG. 5 has, as diffusion layers for the PMOSFET, a well diffusion layer 111 for the PMOSFET, a source/drain diffusion layer 112 for the PMOSFET, and an extension diffusion layer 113 for the PMOSFET.</p> <p>[0100] Additionally, the semiconductor device shown in FIG. 5 has, as diffusion layers for the NMOSFET, a well diffusion layer 121 for the NMOSFET, a source/drain diffusion layer 122 for the NMOSFET, and an extension diffusion layer 123 for the NMOSFET.</p>
		<p style="text-align: center;">FIG. 5</p> <p>The description and annotation below are an example of a first MIS transistor. For example, as can be seen in Figs. 1-2N, Aoyama discloses two transistors, a PMOSFET and an NMOSFET. The first MIS transistor is, e.g., the NMOSFET.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<div data-bbox="321 514 755 1470"> </div> <div data-bbox="787 913 820 1333"> <p>FIG. 1</p> <p>first MIS transistor</p> </div> <div data-bbox="857 466 1312 1459"> </div> <div data-bbox="1339 598 1372 997"> <p>FIG. 1</p> <p>first MIS transistor</p> </div>

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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>As another example, as can be seen in Figs. 3-4N, Aoyama discloses a PMOSFET and an NMOSFET. The first MIS transistor is, e.g., the NMOSFET. The claimed first MIS transistor could also be the PMOSFET.</p> <p style="text-align: right;">FIG. 3</p> <p style="text-align: right;">first MIS transistor</p>

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Claim		Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
Claim Language		<p style="text-align: center;">FIG. 3 first MIS transistor</p>
Claim		As yet another example, as can be seen in Figs. 5-6N, Aoyama discloses a PMOSFET and an NMOSFET. The first MIS transistor is, e.g., the NMOSFET. The claimed first MIS transistor could also be the PMOSFET.

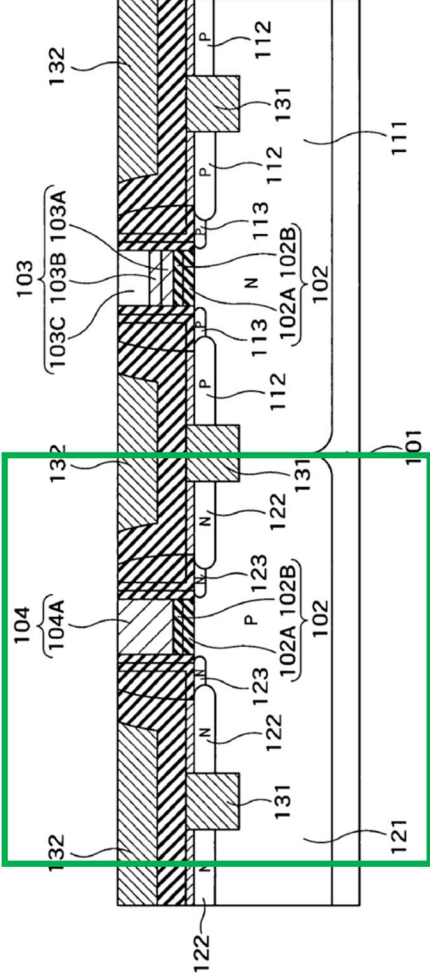
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
25 [b]	a second MIS transistor,	 <p data-bbox="776 1134 799 1333">first MIS transistor</p> <p data-bbox="768 892 799 997">FIG. 5</p> <p data-bbox="881 357 912 1501">Aoyama, as evidenced by the example citations below, discloses a second MIS transistor.</p> <p data-bbox="946 189 1421 1501">[0039] The semiconductor device shown in FIG. 1 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer 103A which is made of conductive metal and a second conductive layer 103B which is made of conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment</p>

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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p> <p>[0040] Additionally, the semiconductor device shown in FIG. 1 has, as diffusion layers for the PMOSFET, a well diffusion layer 111 for the PMOSFET, a source/drain diffusion layer 112 for the PMOSFET, and an extension diffusion layer 113 for the PMOSFET. The well diffusion layer 111 is an N-type diffusion layer, the source/drain diffusion layer 112 is a P-type diffusion layer, and the extension diffusion layer 113 is a P-type diffusion layer.</p> <p>[0041] Additionally, the semiconductor device shown in FIG. 1 has, as diffusion layers for the NMOSFET, a well diffusion layer 121 for the NMOSFET, a source/drain diffusion layer 122 for the NMOSFET, and an extension diffusion layer 123 for the NMOSFET. The well diffusion layer 121 is a P-type diffusion layer, the source/drain diffusion layer 122 is an N-type diffusion layer, and the extension diffusion layer 123 is an N-type diffusion layer.</p>
		<p style="text-align: center;">FIG. 1</p>
		<p>[0072] The semiconductor device shown in FIG. 3 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate</p>

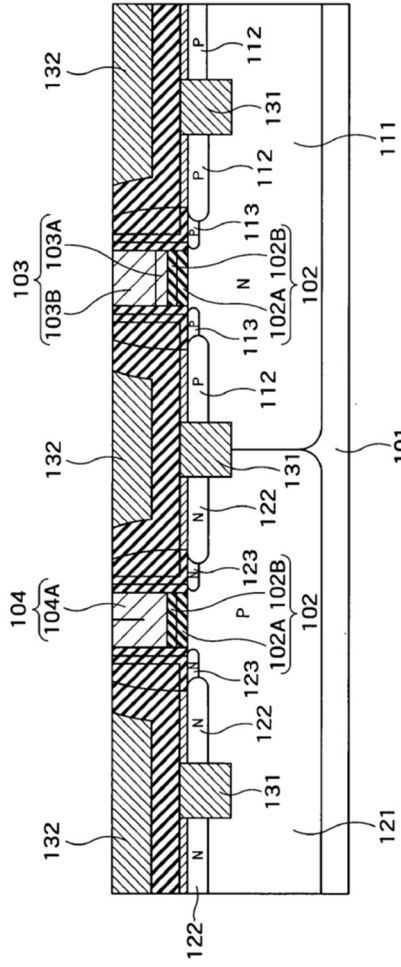
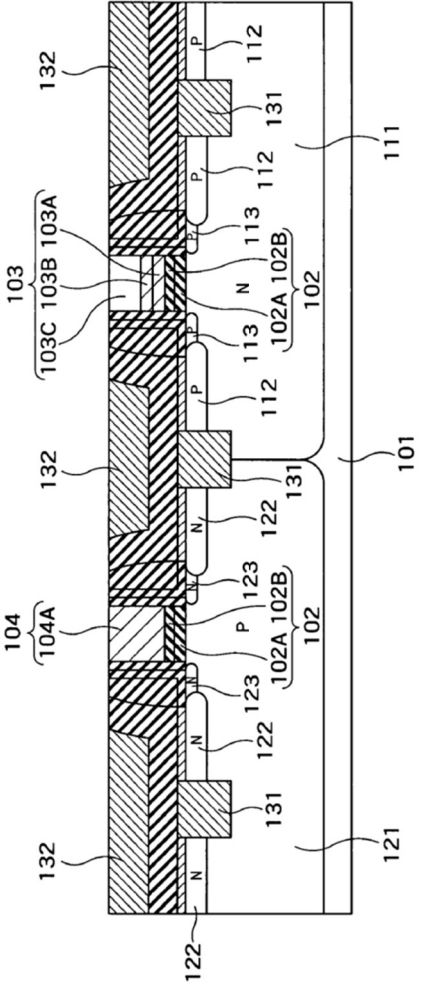
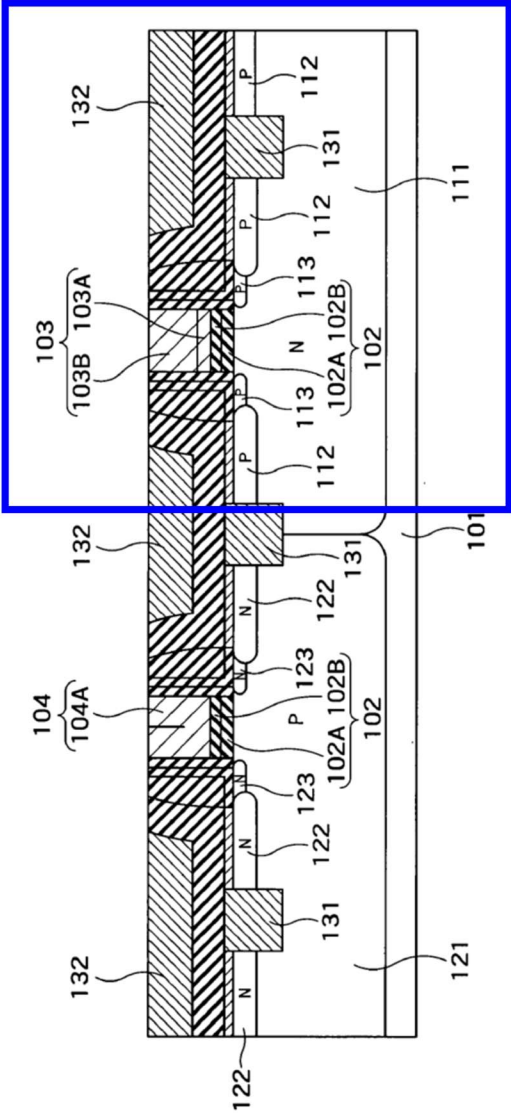
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer 103A which is made of conductive metal and a second conductive layer 103B which is made of conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p>  <p style="text-align: center;">FIG. 3</p> <p>[0098] The semiconductor device shown in FIG. 5 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate</p>

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		<p>101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes three electrode-constituting layers: a first conductive layer 103A which is made of conductive metal, a second conductive layer 103B which is made of conductive metal, and a semiconductor layer 103C which is made of semiconductor. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p> <p>[0099] Additionally, the semiconductor device shown in FIG. 5 has, as diffusion layers for the PMOSFET, a well diffusion layer 111 for the PMOSFET, a source/drain diffusion layer 112 for the PMOSFET, and an extension diffusion layer 113 for the PMOSFET.</p> <p>[0100] Additionally, the semiconductor device shown in FIG. 5 has, as diffusion layers for the NMOSFET, a well diffusion layer 121 for the NMOSFET, a source/drain diffusion layer 122 for the NMOSFET, and an extension diffusion layer 123 for the NMOSFET.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		 <p style="text-align: center;">FIG. 5</p> <p>The description and annotation below are an example of a second MIS transistor. For example, as can be seen in Figs. 1-2N, Aoyama discloses a PMOSFET and an NMOSFET. The second MIS transistor is, e.g., the PMOSFET. The claimed second MIS transistor could also be the NMOSFET.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<div data-bbox="269 506 712 1482"> <p>FIG. 1</p> <p>first MIS transistor</p> <p>second MIS transistor</p> </div> <div data-bbox="878 516 1321 1493"> <p>FIG. 1</p> <p>second MIS transistor</p> <p>first MIS transistor</p> </div>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>As another example, as can be seen in Figs. 3-4N, Aoyama discloses a PMOSFET and an NMOSFET. The second MIS transistor is, e.g., the PMOSFET. The claimed second MIS transistor could also be the NMOSFET.</p>  <p>first MIS transistor second MIS transistor</p> <p>FIG. 3</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<div data-bbox="282 365 799 1478"> </div> <div data-bbox="834 491 873 1331"> <p>second MIS transistor FIG. 3 first MIS transistor</p> </div> <p>As yet another example, as can be seen in Figs. 5-6N, Aoyama discloses a PMOSFET and an NMOSFET. The second MIS transistor is, e.g., the PMOSFET. The claimed second MIS transistor could also be the NMOSFET.</p>

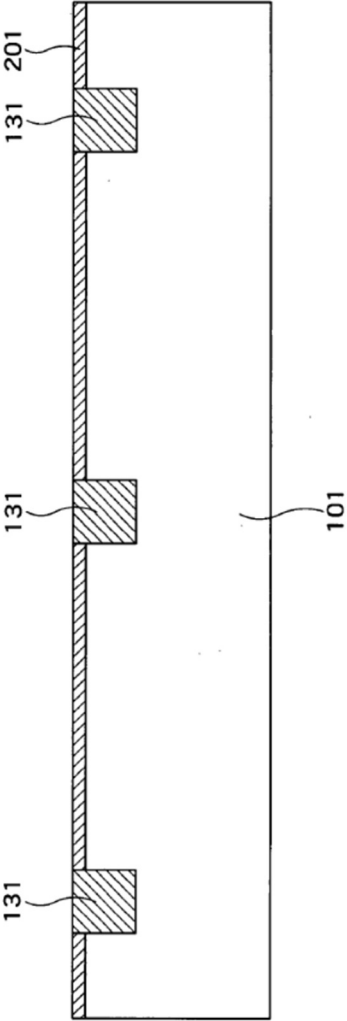
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<div data-bbox="289 516 721 1488"> <p>FIG. 5</p> <p>first MIS transistor</p> <p>second MIS transistor</p> </div> <div data-bbox="841 516 1273 1499"> <p>FIG. 5</p> <p>second MIS transistor</p> <p>first MIS transistor</p> </div>

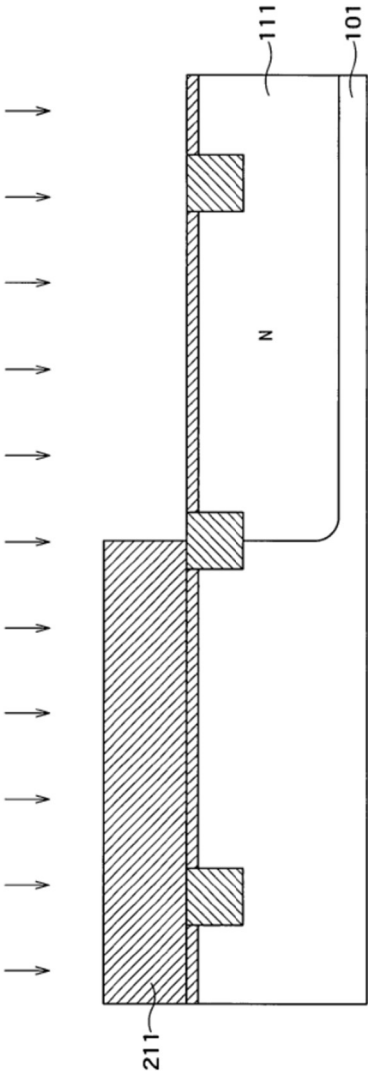
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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
25 [c.1]	wherein: the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate;	<p>Aoyama, as evidenced by the example citations below, discloses the first MIS transistor including a first gate insulating film formed on a first active region in a semiconductor substrate.</p> <p>[0039] The semiconductor device shown in FIG. 1 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer 103A which is made of conductive metal and a second conductive layer 103B which is made of conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p>

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Claim		Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
Claim Language		<p>FIG. 1</p>
		<p>[0044] First, as shown in FIG. 2A, silicon oxide films are buried in predetermined regions of a silicon substrate 101 to form isolation layers 131 of STIs. Then, as shown in FIG. 2A, a silicon oxide film (dielectric film) 201 is formed on the silicon substrate 101.</p>

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		 <p style="text-align: center;">FIG. 2A</p> <p>[0045] Next, as shown in FIG. 2B, ions of P (phosphorus) are implanted into the substrate 101 using a resist 211 as a mask. The implantation of P ions is performed to form the well diffusion layer 111 for the PMOSFET and to adjust the threshold voltage of the PMOSFET, and performed a plurality of times. In some cases, ions of B (boron), In (indium), or the like are further implanted to finely adjust the threshold voltage of the PMOSFET.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		 <p style="text-align: center;">FIG. 2B</p> <p>[0046] Next, as shown in FIG. 2C, ions of B (boron) are implanted into the substrate 101 using a resist 221 as a mask. The implantation of B ions is performed to form the well diffusion layer 121 for the NMOSFET and to adjust the threshold voltage of the NMOSFET, and performed a plurality of times. In some cases, ions of P (phosphorus), As (arsenic), or the like are further implanted to finely adjust the threshold voltage of the NMOSFET. After that, the substrate 101 is subjected to thermal diffusion processing, thereby completing the well diffusion layer 111 for the PMOSFET and the well diffusion layer 121 for the NMOSFET.</p>

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		<div data-bbox="277 428 675 1499"> </div> <p data-bbox="743 913 781 1050">FIG. 2C</p> <p data-bbox="816 191 1318 1499">[0047] Next, as shown in FIG. 2D, the dielectric film 201 is removed from the substrate 101 using an ammonium fluoride aqueous solution, and the surface of the substrate 101 is cleaned using 0.5 to 5.0% hydrofluoric acid. Then, as shown in FIG. 2D, a silicon oxide film (a first dielectric film of a gate dielectric film) 102A with a thickness of 0.5 to 0.8 nm is formed on the substrate 101 in an atmosphere containing oxygen, and a hafnium silicate film (a second dielectric film of the gate dielectric film) 102B with a thickness of about 2.0 nm is formed on the silicon oxide film 102A using tetrakis(diethylamino)hafnium, tetrakis(dimethylamino)silicon, and oxygen. After that, the substrate 101 is subjected to annealing at 600° C., thereby densifying the silicon oxide film 102A and hafnium silicate film 102B. After that, the substrate 101 is processed in a nitrogen plasma atmosphere or ammonia atmosphere and then subjected to annealing at 1,000° C., thereby reforming the hafnium silicate film 102B into a hafnium silicon oxynitride film 102B. With the above-described manufacturing steps, the gate dielectric film 102 common to the PMOSFET and the NMOSFET is formed, ranging from a PMOSFET region 105 to a NMOSFET region 106, on the substrate 101. The PMOSFET region 105 is a region where the PMOSFET is to be formed, which is a specific example</p>

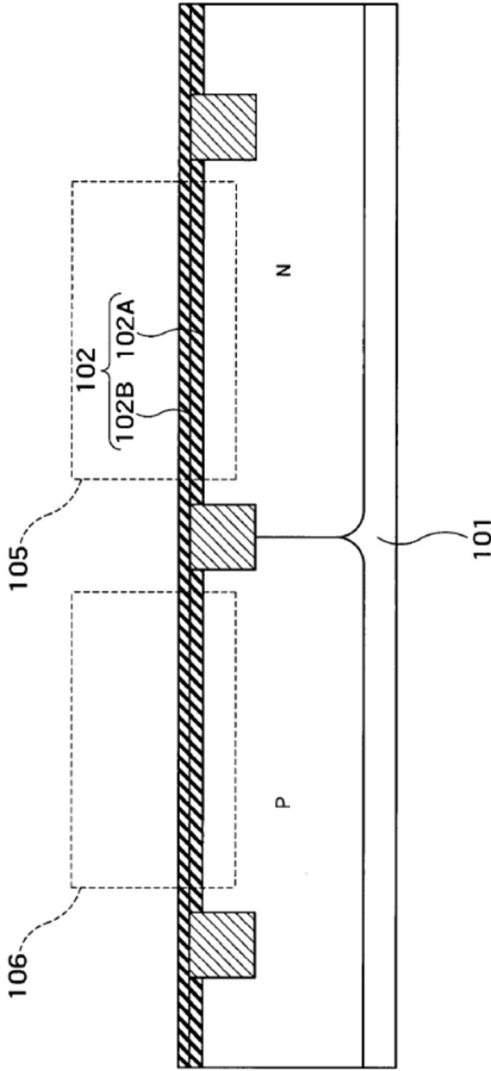
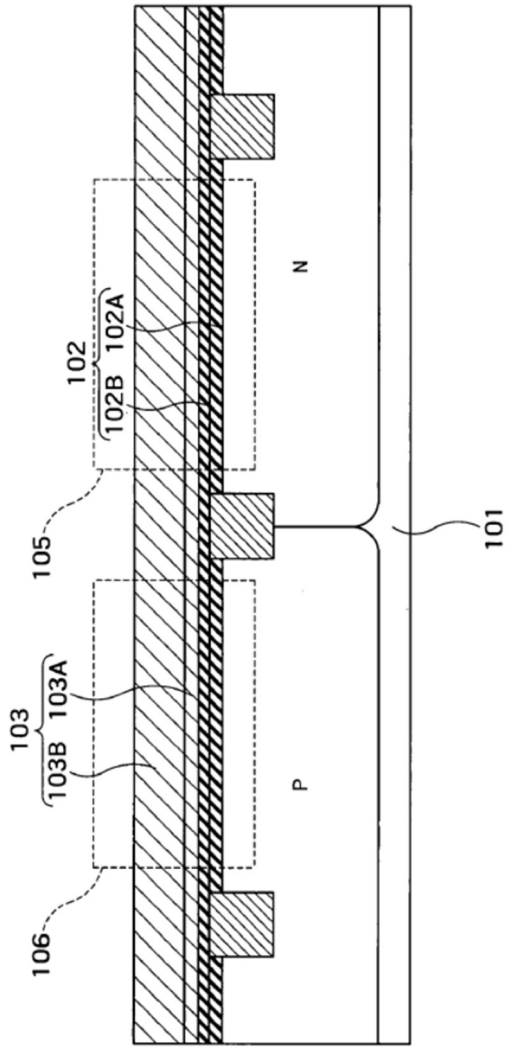
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>of a P-type FET region, and the NMOSFET region 106 is a region where the NMOSFET is to be formed, which is a specific example of an N-type FET region.</p>  <p style="text-align: center;">FIG. 2D</p> <p>[0048] Note that although the gate dielectric film 102 of the first embodiment has a two-layer structure of the silicon oxide film 102A and hafnium silicon oxynitride film 102B, it may have a one-layer structure of only a hafnium silicon oxynitride film or a laminated structure of three or more layers including a hafnium silicon oxynitride film.</p> <p>[0049] Next, as shown in FIG. 2E, a Ru (ruthenium) layer (a first conductive layer of a gate electrode for the PMOSFET) 103A with a thickness of about 20 nm is deposited on the hafnium silicon oxynitride film 102B using bis(cyclopentadienyl)ruthenium and oxygen, and a W (tungsten) layer (a second conductive layer of the gate electrode for the PMOSFET) 103B with a thickness of about 60 nm is deposited on the Ru layer 103A using tungsten hexafluoride, silane, and hydrogen. With the above-described manufacturing steps, the gate electrode layer 103 for the PMOSFET is formed,</p>

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Claim		Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>ranging from the PMOSFET region 105 to the NMOSFET region 106, on the gate dielectric film 102.</p>  <p>FIG. 2E</p> <p>[0050] Note that although the gate electrode layer 103 for the PMOSFET of the first embodiment has a two-layer structure of the Ru layer 103A and W layer 103B, it may have a one-layer structure of only a Ru layer or a laminated structure of three or more layers including a Ru layer. The two-layer structure of the gate electrode layer 103 for the PMOSFET of the first embodiment is mainly due to the thickness of the Ru layer 103A. Since Ru has not only advantages such as a high work function but also disadvantages such as costliness, the thickness of the Ru layer 103A is made small in the first embodiment. For this reason, in the first embodiment, migration and even agglomeration may occur in the Ru layer 103A, for example, at the time of activation of the source/drain diffusion layer due to the tension of the Ru layer 103A itself. To prevent these phenomena, the gate electrode layer 103 for the PMOSFET is configured to have a two-layer structure in the first embodiment.</p>

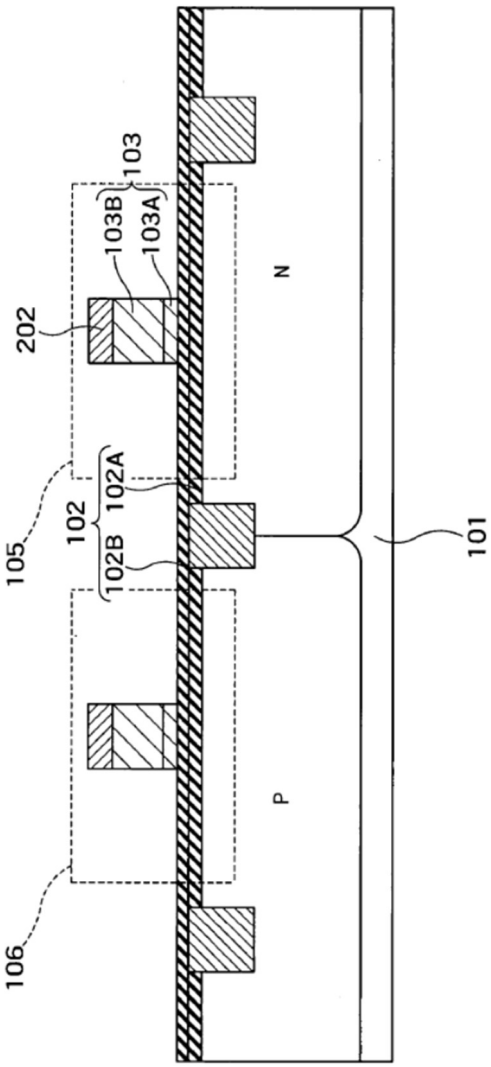
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>[0051] Next, as shown in FIG. 2F, the Ru layer 103A and W layer 103B are processed using a dielectric film 202 as a hard mask, the dielectric film 202 including a silicon oxide film or silicon nitride film. The dielectric film 202 is deposited and processed to be the hard masks in advance. With the above-described manufacturing steps, in the PMOSFET region 105 and the NMOSFET region 106, a gate electrode 103 for the PMOSFET is formed in the PMOSFET region 105, and a dummy gate electrode (a gate electrode used as a dummy) 103 with the same configuration as that of the gate electrode 103 for the PMOSFET is formed in the NMOSFET region 106.</p>  <p style="text-align: center;">FIG. 2F</p> <p>[0052] Next, as shown in FIG. 2G, the silicon oxide film 102A and hafnium silicon oxynitride film 102B are processed using the dielectric film 202 as a hard mask. Etching conditions at this time are determined by appropriately selecting an etchant and etching time in consideration of the thickness and type of the high-permittivity dielectric film such that all of each dielectric film 202 is not etched. With the above-described manufacturing steps, in the PMOSFET region 105 and the NMOSFET region 106, a gate dielectric film 102 for the PMOSFET is formed in the PMOSFET region 105, and</p>

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Claim		Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
Claim Language		a gate dielectric film 102 for the NMOSFET is formed in the NMOSFET region 106. Gate dielectric films 102 for the PMOSFET and the NMOSFET are formed from the gate dielectric film 102 common to the PMOSFET and the NMOSFET.
FIG. 2G		<p>The diagram shows a cross-section of a semiconductor device. At the base is a substrate 101, which has two distinct regions labeled 'P' and 'N'. Above the substrate, there is a gate dielectric film 102. This film is composed of two layers: a first dielectric film 102A and a second dielectric film 102B. On top of the gate dielectric film 102, there is a gate electrode 103. The gate electrode 103 consists of two layers: a first conductive layer 103A and a second conductive layer 103B. The gate electrode 103 is positioned over the gate dielectric film 102. The entire structure is shown within a dashed box 105. Other components like 106, 202, and 102B are also indicated.</p>
		[0072] The semiconductor device shown in FIG. 3 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer 103A which is made of conductive metal and a second conductive layer 103B which is made of

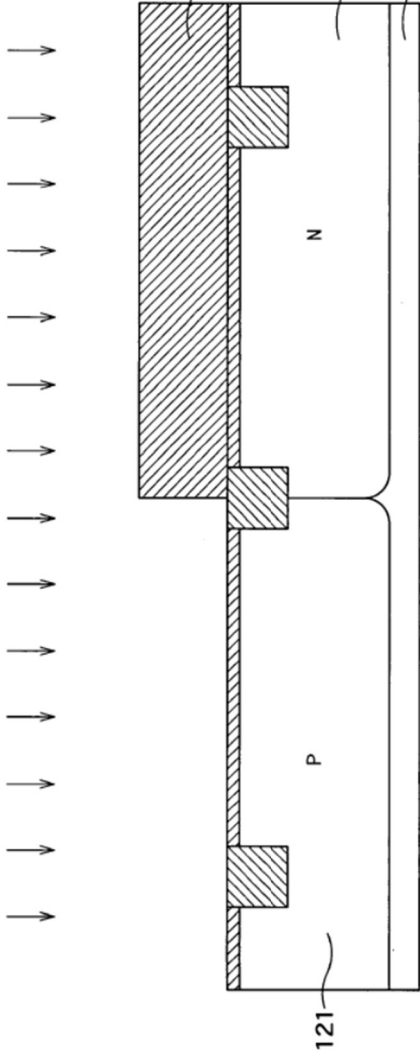
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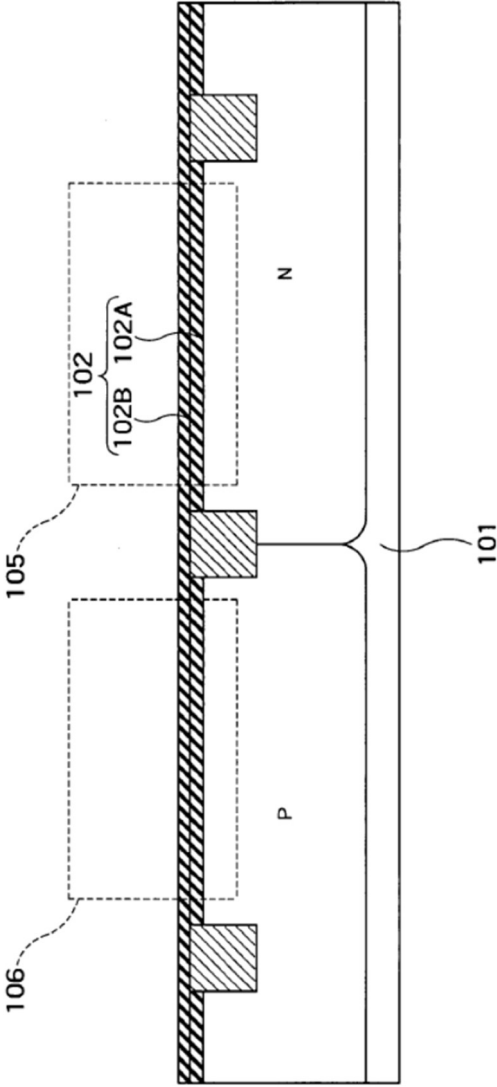
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p> <p>[0063] As described above, in the semiconductor device of the first embodiment, each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of the high-permittivity dielectric film, the gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of the conductive metal, and the gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of the conductive metal. Accordingly, in the first embodiment, it is possible to thin the gate dielectric films while suppressing an increase in leakage current, and to suppress a shift in the threshold voltage of the PMOSFET to increase the inversion capacitance of the PMOSFET.</p> <p>[0064] Moreover, in the first embodiment, since the source/drain diffusion layer 112 (and the extension diffusion layer 113) for the PMOSFET and the source/drain diffusion layer 122 (and extension diffusion layer 123) for the NMOSFET are formed after formation of the gate dielectric films 102, it is possible to improve the quality of the high-permittivity dielectric films to suppress a leakage current in them. This is because performing the process of improving the quality of the high-permittivity dielectric films before the formation of the source/drain diffusion layers (and extension diffusion layers) makes it possible, to perform the process of improving the quality of the high-permittivity dielectric films without concern about adverse effects on the source/drain diffusion layers (and extension diffusion layers).</p> <p>[0066] Therefore, in the first embodiment, gate dielectric films with preferable characteristics such as a preferable film quality, and gate electrodes with preferable characteristics such as a preferable work function, can be used as gate dielectric films and gate electrodes constituting a PMOSFET and an NMOSFET. Accordingly, in the first embodiment, it is possible to manufacture a semiconductor device including a high-performance CMOSFET.</p> <p>[0069] Although, in this embodiment, a hafnium silicon oxynitride film is adopted as a high-permittivity dielectric film to form each gate dielectric film 102, any other high-permittivity</p>

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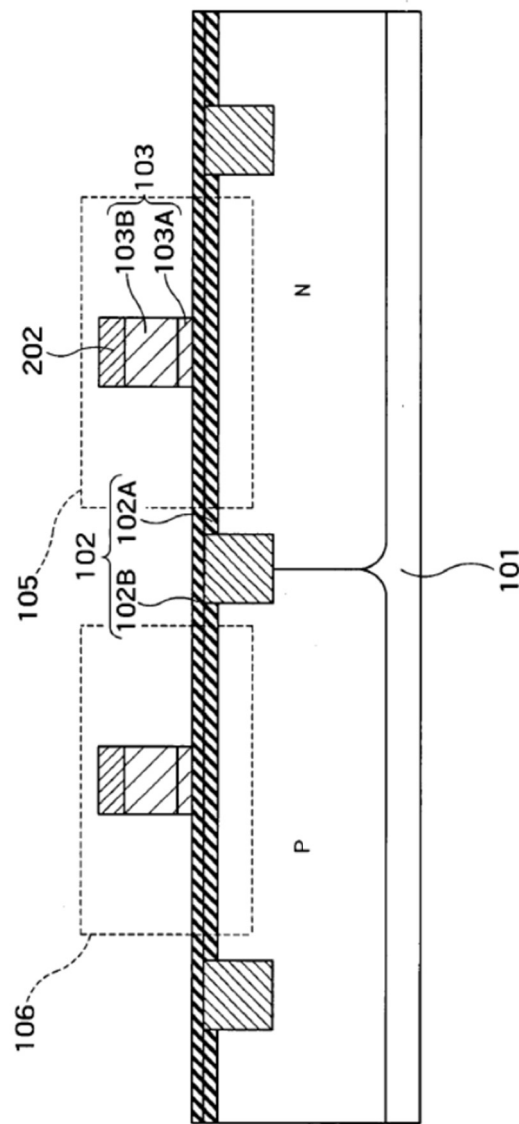
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>dielectric film may be adopted. Although, in this embodiment, the Ru layer and W layer are adopted as metal electrode layers to form the gate electrode 103 for the PMOSFET, any other metal electrode layers may be adopted. For example, a W layer, Ru layer, or Pt layer may be adopted as a metal electrode layer to form the gate electrode 103 for the PMOSFET. Although, in this embodiment, a TaSiN layer, HfN layer, and WSi layer are described as examples of metal electrode layers to form the gate electrode 104 for the NMOSFET, any other metal electrode layers may be adopted. It is possible to adopt, for example, a TaSi layer, TaSiN layer, TaC layer, TaCN layer, HfN layer, HfSi layer, HfSiN layer, WSi layer, TaHf layer, or TaHfN layer as a metal electrode layer to form the gate electrode 104 for the NMOSFET.</p> <p style="text-align: center;">FIG. 3</p> <p>[0077] First, as shown in FIG. 4A, silicon oxide films are buried in predetermined regions of a silicon substrate 101 to form isolation layers 131 of STIs. Then, as shown in FIG. 4A, a silicon oxide film (dielectric film) 201 is formed on the silicon substrate 101.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<div data-bbox="305 506 646 1493"> <p>FIG. 4A</p> </div> <div data-bbox="764 216 833 1493"> <p>[0078] Next, as shown in FIG. 4B, ions of P (phosphorus) are implanted into the substrate 101 using a resist 211 as a mask.</p> </div> <div data-bbox="881 506 1222 1493"> <p>FIG. 4B</p> </div>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>[0079] Next, as shown in FIG. 4C, ions of B (boron) are implanted into the substrate 101 using a resist 221 as a mask. After that, the substrate 101 is subjected to thermal diffusion processing, thereby completing a well diffusion layer 111 for the PMOSFET and a well diffusion layer 121 for the NMOSFET.</p>  <p style="text-align: center;">FIG. 4C</p> <p>[0080] Next, as shown in FIG. 4D, the dielectric film 201 is removed from the substrate 101 using an ammonia fluoride aqueous solution, and the surface of the substrate 101 is cleaned using 0.5 to 5.0% hydrofluoric acid. Then, as shown in FIG. 4D, a silicon oxide film (a first dielectric film of a gate dielectric film) 102A with a thickness of 0.5 to 0.8 nm is formed on the substrate 101 in an atmosphere containing oxygen, and a hafnium silicate film (a second dielectric film of the gate dielectric film) 102B with a thickness of about 2.0 nm is formed on the silicon oxide film 102A using tetrakis(diethylamino)hafnium, tetrakis(dimethylamino)silicon, and oxygen. After that, the substrate 101 is subjected to annealing at 600° C., thereby densifying the silicon oxide film 102A and hafnium silicate film 102B. After that, the substrate 101 is processed in a nitrogen plasma atmosphere or ammonia atmosphere and then subjected to annealing at 1,000° C., thereby reforming the hafnium silicate film 102B into a hafnium silicon oxynitride film 102B. With the above-described</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>manufacturing steps, the gate dielectric film 102 common to the PMOSFET and NMOSFET is formed, ranging from a PMOSFET region 105 to a NMOSFET region 106, on the substrate 101. The PMOSFET region 105 is a region where the PMOSFET is to be formed, which is a specific example of a P-type FET region, and the NMOSFET region 106 is a region where the NMOSFET is to be formed, which is a specific example of an N-type FET region.</p>  <p style="text-align: center;">FIG. 4D</p> <p>[0081] Note that although the gate dielectric film 102 of the second embodiment has a two-layer structure of the silicon oxide film 102A and hafnium silicon oxynitride film 102B, it may have a one-layer structure of only a hafnium silicon oxynitride film or a laminated structure of three or more layers including a hafnium silicon oxynitride film.</p> <p>[0082] Next, as shown in FIG. 4E, a W (tungsten) layer (a first conductive layer of a gate electrode for the PMOSFET) 103A with a thickness of about 20 nm is deposited on the hafnium silicon oxynitride film 102B by thermal CVD using tungsten hexacarbonyl or plasma CVD using tungsten hexacarbonyl and hydrogen, and a TiN (titanium nitride) layer (a second conductive layer of the gate</p>

Claim	Claim Language	<p data-bbox="207 338 245 1367">Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama</p> <p data-bbox="261 191 407 1501">electrode for the PMOSFET) 103B with a thickness of about 60 nm is deposited on the W layer 103A using titanium tetrachloride and ammonia. With the above-described manufacturing steps, the gate electrode layer 103 for the PMOSFET is formed, ranging from the PMOSFET region 105 to the NMOSFET region 106, on the gate dielectric film 102.</p> <div data-bbox="435 352 982 1486"> <p>The diagram is a cross-sectional view of a semiconductor device. It shows a substrate 101 with a P-type region (P) and an N-type region (N). A gate dielectric film 102 is formed on the substrate. On top of the gate dielectric film 102, a gate electrode layer 103 is formed. The gate electrode layer 103 is divided into two parts: 103A and 103B. 103A is located over the P-type region, and 103B is located over the N-type region. A dashed line 105 indicates the boundary between the PMOSFET region (106) and the NMOSFET region (105). The gate electrode layer 103 is formed on the gate dielectric film 102, ranging from the PMOSFET region 105 to the NMOSFET region 106. The gate electrode layer 103 is formed on the gate dielectric film 102, ranging from the PMOSFET region 105 to the NMOSFET region 106.</p> </div> <p data-bbox="1015 842 1052 1003">FIG. 4E</p> <p data-bbox="1089 216 1268 1501">[0083] Note that although the gate electrode layer 103 for the PMOSFET of the second embodiment has a two-layer structure of the W layer 103A and TiN layer 103B, it may have a one-layer structure of only a W layer or a laminated structure of three or more layers including a W layer. If the gate electrode layer 103 for the PMOSFET has a one-layer structure of only a W layer, it is desirable to reduce the thickness of the W layer to 60 nm or less because the W layer is likely to peel off.</p> <p data-bbox="1305 254 1409 1501">[0084] Next, as shown in FIG. 4F, the W layer 103A and TiN layer 103B are processed using a dielectric film 202 as a hard mask, the dielectric film 202 including a silicon oxide film or silicon nitride film. With the above-described manufacturing step, in the PMOSFET region 105 and the</p>
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Claim		Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
Claim Language		<p>NMOSFET region 106, a gate electrode 103 for the PMOSFET is formed in the PMOSFET region 105, and a dummy gate electrode (a gate electrode used as a dummy) 103 with the same configuration as that of the gate electrode 103 for the PMOSFET is formed in the NMOSFET region 106.</p>  <p>FIG. 4F</p> <p>[0085] Next, as shown in FIG. 4G, the silicon oxide film 102A and hafnium silicon oxynitride film 102B are processed using the dielectric film 202 as a hard mask. With the above-described manufacturing steps, in the PMOSFET region 105 and the NMOSFET region 106, a gate dielectric film 102 for the PMOSFET is formed in the PMOSFET region 105, and a gate dielectric film 102 for the NMOSFET is formed in the NMOSFET region 106. Gate dielectric films 102 common to the PMOSFET and the NMOSFET are formed from the gate dielectric film 102 common to the PMOSFET and the NMOSFET.</p>

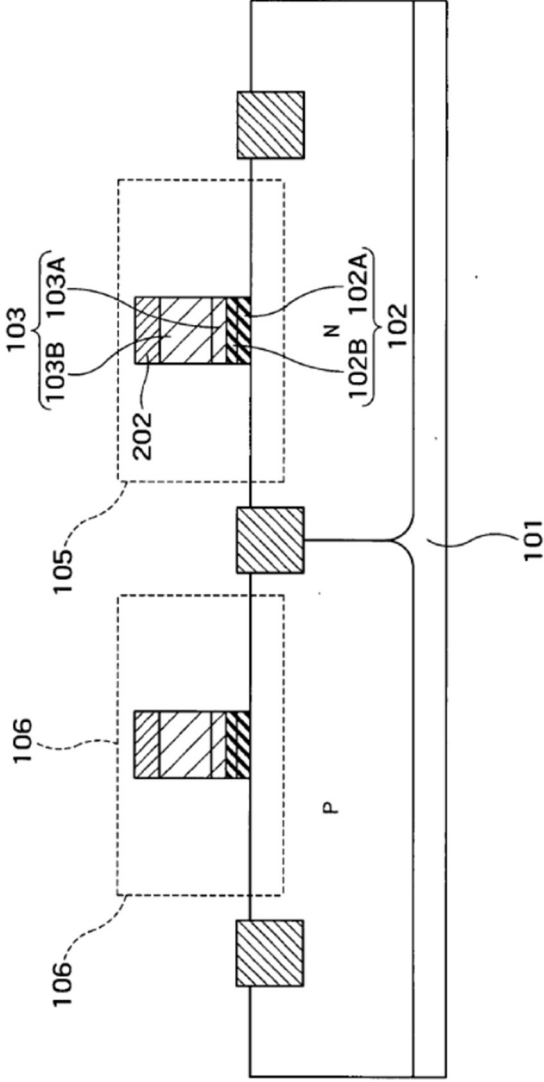
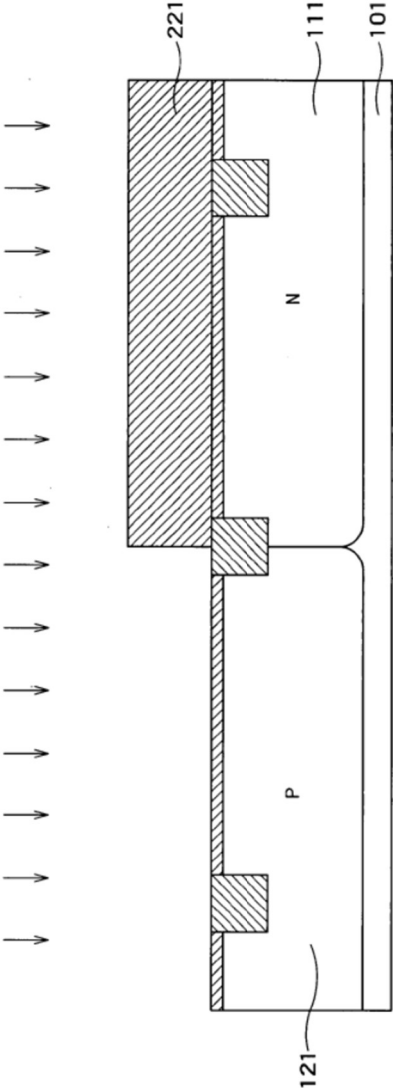
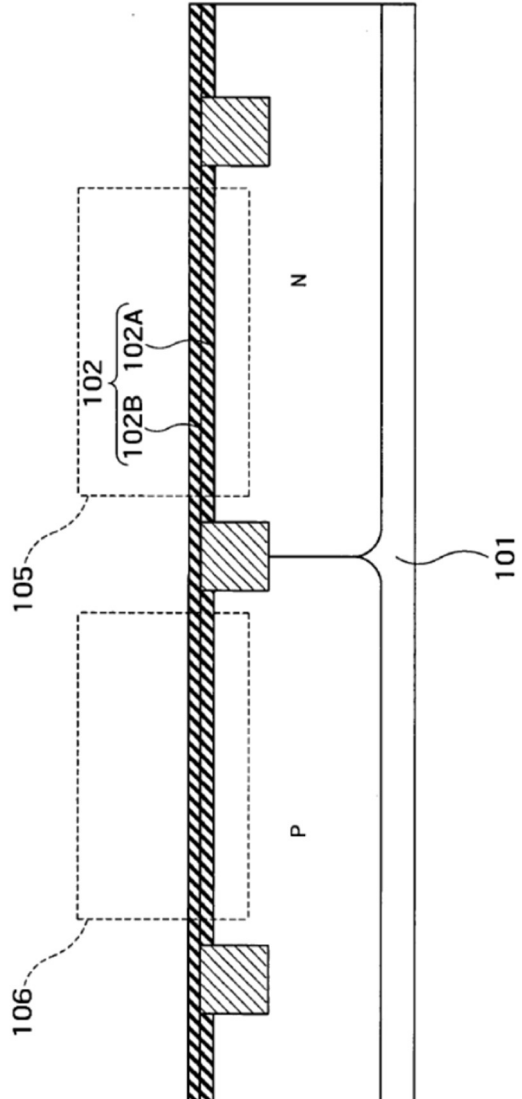
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<div data-bbox="272 401 812 1476">  </div> <div data-bbox="846 863 883 1016"> <p>FIG. 4G</p> </div> <div data-bbox="932 191 1406 1501"> <p>[0098] The semiconductor device shown in FIG. 5 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the NMOSFET in this embodiment includes three electrode-constituting layers: a first conductive layer 103A which is made of conductive metal, a second conductive layer 103B which is made of semiconductor, and a semiconductor layer 103C which is made of semiconductor. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of</p> </div>

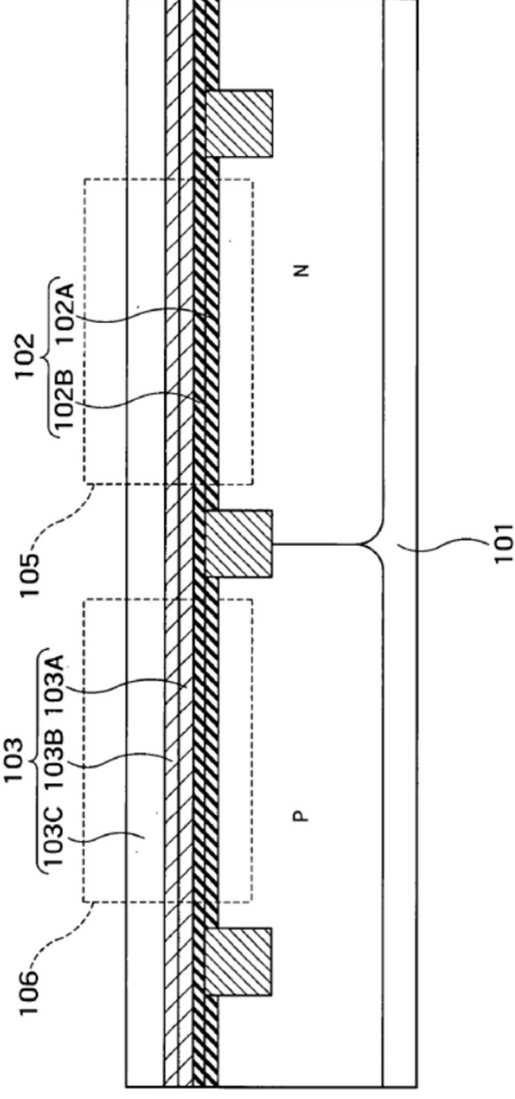
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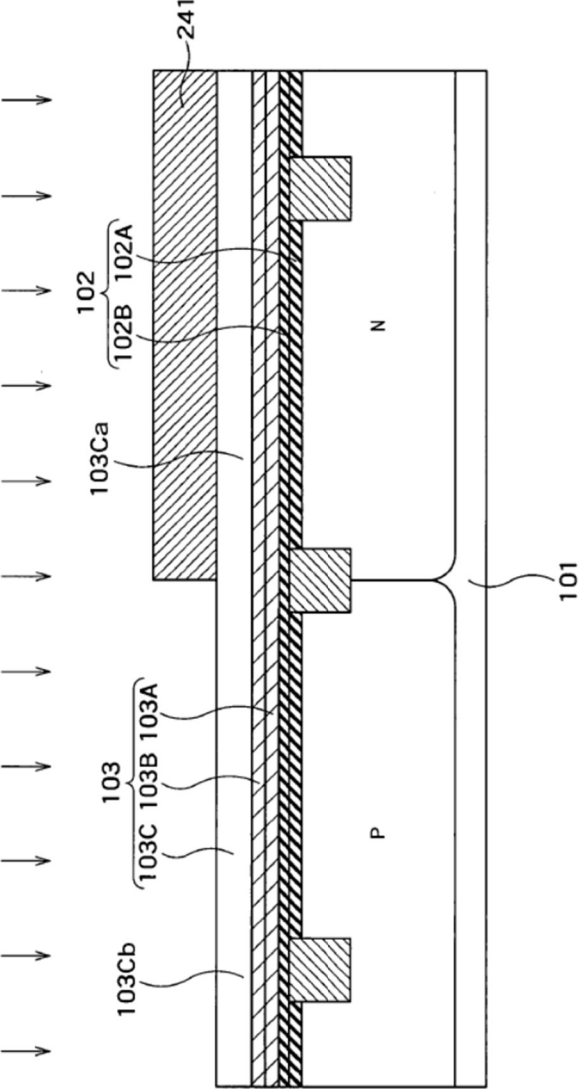
Claim		Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
Claim Language		conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<div data-bbox="277 459 634 1488"> </div> <div data-bbox="678 900 716 1052"> <p>FIG. 6A</p> </div> <div data-bbox="751 216 821 1501"> <p>[0104] Next, as shown in FIG. 6B, ions of P (phosphorus) are implanted into the substrate 101 using a resist 211 as a mask.</p> </div> <div data-bbox="870 380 1252 1488"> </div> <div data-bbox="1320 863 1357 1010"> <p>FIG. 6B</p> </div>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<p>[0105] Next, as shown in FIG. 6C, ions of B (boron) are implanted into the substrate 101 using a resist 221 as a mask. After that, the substrate 101 is subjected to thermal diffusion processing, thereby completing a well diffusion layer 111 for the PMOSFET and a well diffusion layer 121 for the NMOSFET.</p> <div data-bbox="467 405 857 1486"><p>The diagram shows a cross-section of a substrate 101. The substrate is divided into two main regions: a P-type region on the left and an N-type region on the right. A well diffusion layer 111 is formed in the P-type region, and a well diffusion layer 121 is formed in the N-type region. A resist 221 is used as a mask for ion implantation. Arrows indicate the direction of ion implantation into the substrate 101.</p></div> <p style="text-align: center;">FIG. 6C</p> <p>[0106] Next, as shown in FIG. 6D, the dielectric film 201 is removed from the substrate 101 using an ammonium fluoride aqueous solution, and the surface of the substrate 101 is cleaned using 0.5 to 5.0% hydrofluoric acid. Then, as shown in FIG. 6D, a silicon oxide film (a first dielectric film of a gate dielectric film) 102A with a thickness of 0.5 to 0.8 nm is formed on the substrate 101 in an atmosphere containing oxygen, and a hafnium silicate film (a second dielectric film of the gate dielectric film) 102B with a thickness of about 2.0 nm is formed on the silicon oxide film 102A using tetrakis(diethylamino)hafnium, tetrakis(dimethylamino)silicon, and oxygen. After that, the substrate 101 is subjected to annealing at 600° C., thereby densifying the silicon oxide film 102A and hafnium silicate film 102B. After that, the substrate 101 is processed in a nitrogen plasma atmosphere or ammonia atmosphere and then subjected to annealing at 1,000° C., thereby reforming the hafnium silicate film 102B into a hafnium silicon oxynitride film 102B. With the above-described</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>manufacturing steps, the gate dielectric film 102 common to the PMOSFET and NMOSFET is formed, ranging from a PMOSFET region 105 to a NMOSFET region 106, on the substrate 101. The PMOSFET region 105 is a region where the PMOSFET is to be formed, which is a specific example of a P-type FET region, and the NMOSFET region 106 is a region where the NMOSFET is to be formed, which is a specific example of an N-type FET region.</p>  <p style="text-align: center;">FIG. 6D</p> <p>[0107] Next, as shown in FIG. 6E, a W (tungsten) layer (a first conductive layer of a gate electrode for the PMOSFET) 103A with a thickness of about 20 nm is deposited on the hafnium silicon oxynitride film 102B by thermal CVD using tungsten hexacarbonyl or plasma CVD using tungsten hexacarbonyl and hydrogen, a TiN (titanium nitride) layer (a second conductive layer of the gate electrode for the PMOSFET) 103B with a thickness of about 60 nm is deposited on the W layer 103A using diethylaminotitanium and ammonia, and a semiconductor layer 103C made of polysilicon or amorphous silicon is deposited on the TiN (titanium nitride) layer 103B. With the above-described</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>manufacturing steps, the gate electrode 103 for the PMOSFET is formed, ranging from the PMOSFET region 105 to the NMOSFET region 106, on the gate dielectric film 102.</p>  <p style="text-align: center;">FIG. 6E</p> <p>[0108] Next, as shown in FIG. 6F, ions of P or As are implanted into the semiconductor layer 103C above the well diffusion layer 121 for the NMOSFET, using a resist 241 above the well diffusion layer 111 for the PMOSFET as a mask. After that, the substrate 101 is subjected to thermal diffusion processing, thereby completing an N-type diffusion layer inside the semiconductor layer 103C. The inside of a part of the semiconductor layer 103C above the well diffusion layer 111 for the PMOSFET becomes a non-diffusion layer 103Ca, and the inside of a part of the semiconductor layer 103C above the well diffusion layer 121 for the NMOSFET becomes a diffusion layer 103Cb.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		 <p data-bbox="885 892 933 1039">FIG. 6F</p> <p data-bbox="974 210 1234 1501">[0109] Next, as shown in FIG. 6G, the W layer 103A, TiN layer 103B, and semiconductor layer 103C (non-diffusion layer 103Ca and diffusion layer 103Cb) are processed using a dielectric film 202 as a hard mask, the dielectric film 202 including a silicon oxide film or silicon nitride film. With the above-described manufacturing steps, in the PMOSFET region 105 and the NMOSFET region 106, a gate electrode 103 for the PMOSFET is formed in the PMOSFET region 105, and a dummy gate electrode (a gate electrode used as a dummy) 103 with the same configuration as that of the gate electrode 103 for the PMOSFET is formed in the NMOSFET region 106.</p>

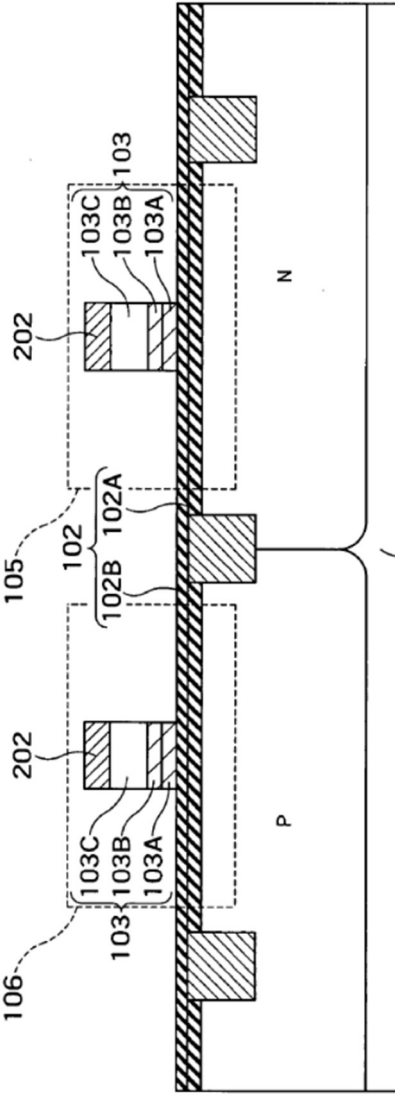
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Claim Language		
Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama		<p>FIG. 6G</p> <p>[0110] Next, as shown in FIG. 6H, the silicon oxide film 102A and hafnium silicon oxynitride film 102B are processed using the dielectric film 202 as a hard mask. With the above-described manufacturing steps, in the PMOSFET region 105 and the NMOSFET region 106, a gate dielectric film 102 for the PMOSFET is formed in the PMOSFET region 105, and a gate dielectric film 102 for the NMOSFET is formed in the NMOSFET region 106. Gate dielectric films 102 common to the PMOSFET and the NMOSFET are formed from the gate dielectric film 102 common to the PMOSFET and the NMOSFET.</p>

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Claim		Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
Claim Language		<p>FIG. 6H</p> <p>The description and annotation below are an example of a first gate insulating film formed on a first active region. For example, as can be seen in Figs. 1-2N, Aoyama discloses gate dielectric film 102 for the N and PMOSFET comprises first dielectric film 102A, a silicon oxide film, and second dielectric film 102B, a hafnium silicon oxynitride film.</p>

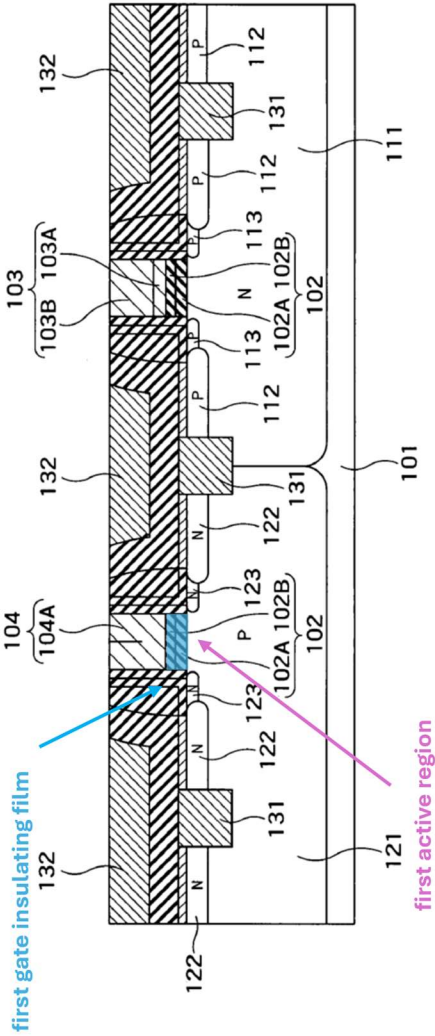
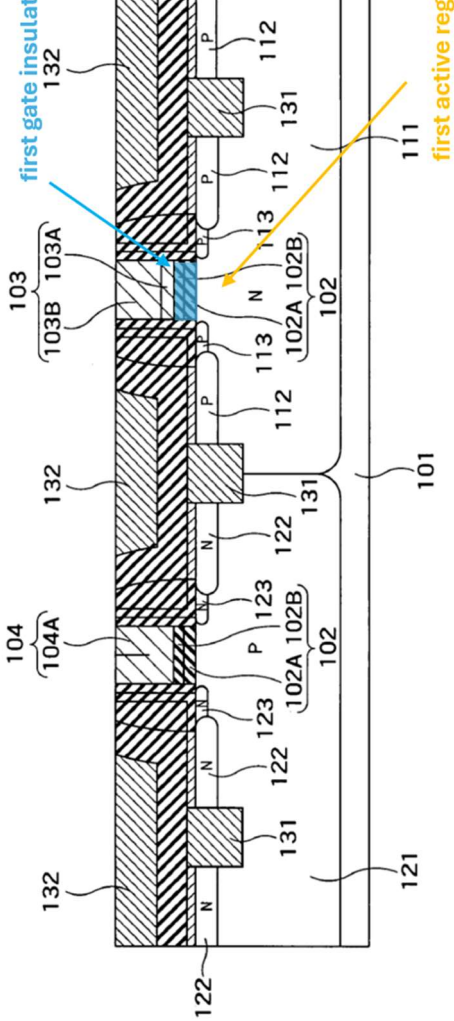
Claim	Claim Language	<p data-bbox="207 338 245 1360">Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama</p> <div data-bbox="272 451 704 1480">  <p data-bbox="743 535 764 779">FIG. 1</p> <p data-bbox="743 1098 764 1304">first MIS transistor</p> <p data-bbox="743 535 764 779">second MIS transistor</p> <p data-bbox="678 1165 699 1358">first active region</p> <p data-bbox="277 1213 298 1480">first gate insulating film</p> </div> <div data-bbox="812 363 1263 1465">  <p data-bbox="1302 535 1323 779">FIG. 1</p> <p data-bbox="1302 1073 1323 1325">second MIS transistor</p> <p data-bbox="1302 569 1323 779">first MIS transistor</p> <p data-bbox="1237 415 1258 615">first active region</p> <p data-bbox="824 363 846 636">first gate insulating film</p> </div>
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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>As another example, as can be seen in Figs. 3-4N, Aoyama discloses gate dielectric film 102 for the N and PMOSFET comprises first dielectric film 102A, a silicon oxide film, and second dielectric film 102B, a hafnium silicon oxynitride film.</p> <p>first gate insulating film</p> <p>first active region</p> <p>first MIS transistor</p> <p>second MIS transistor</p> <p>FIG. 3</p>

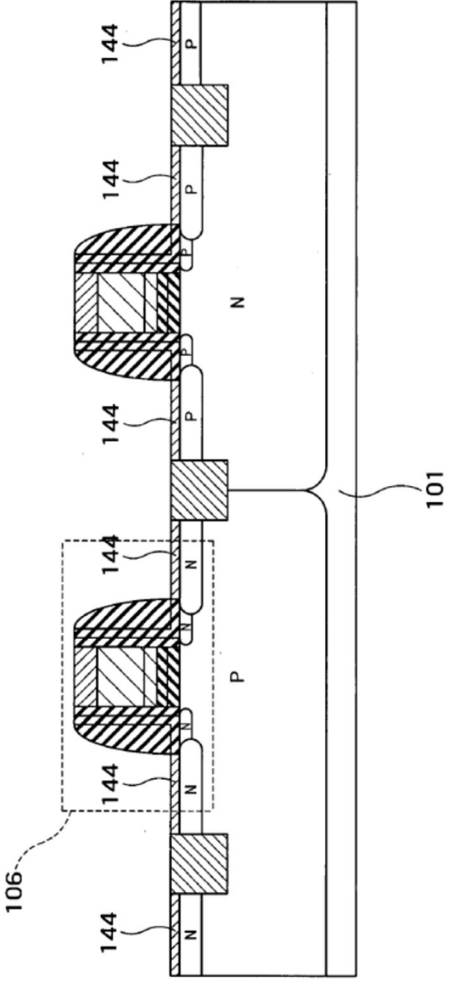
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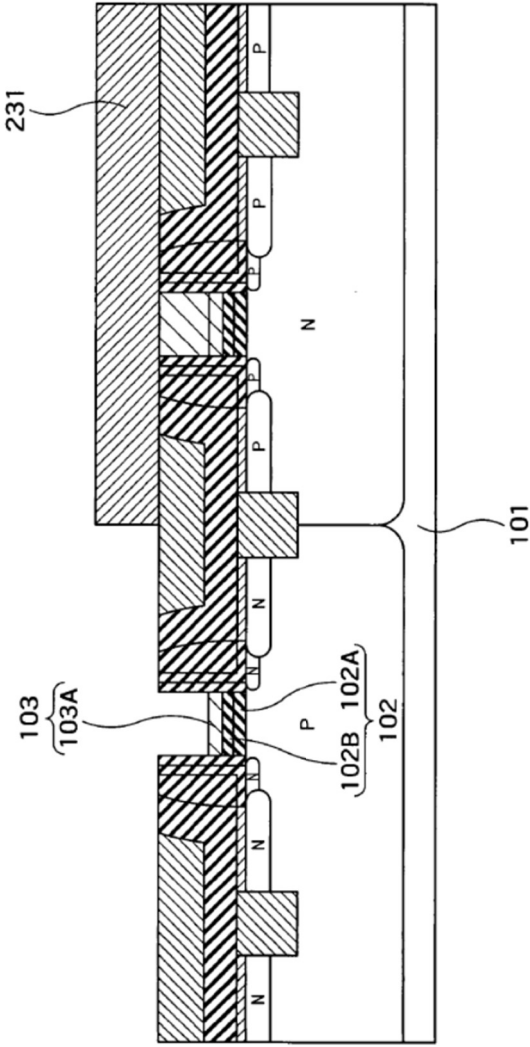
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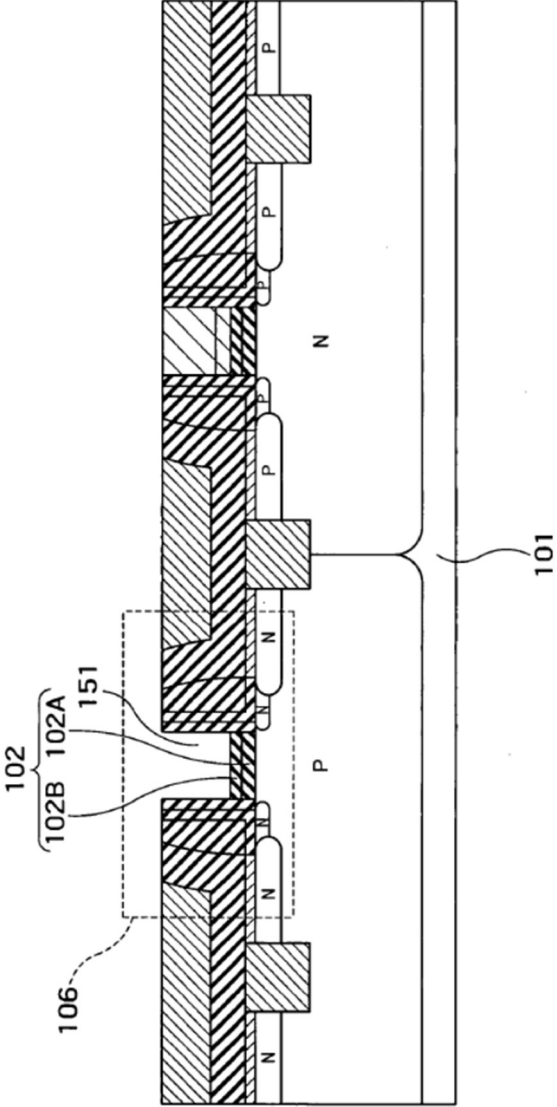
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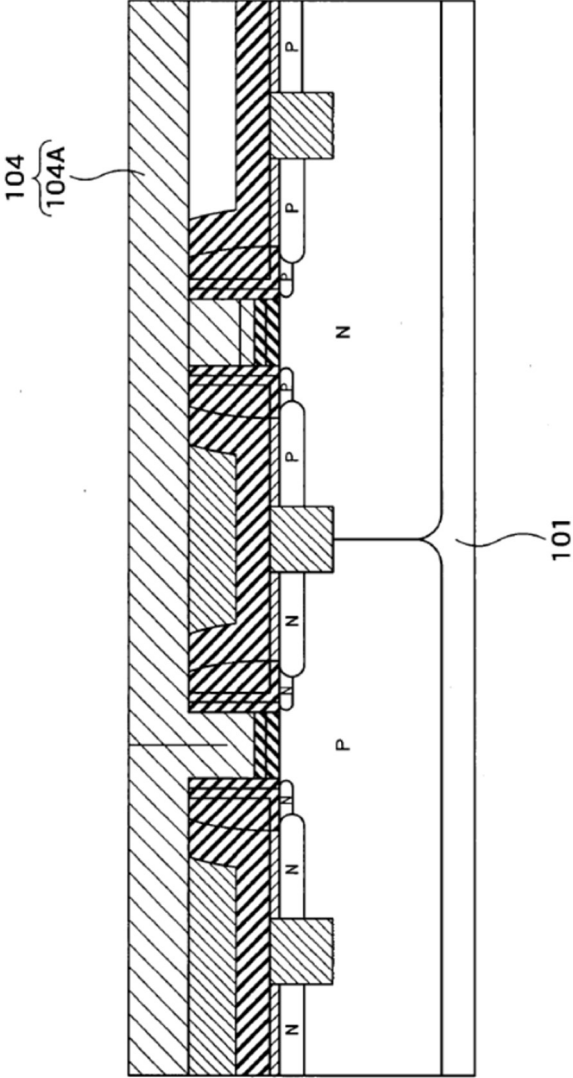
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
25 [c.2]	a first gate electrode including a second metal film formed on the first gate insulating film;	<p>Aoyama, as evidenced by the example citations below, discloses a first gate electrode including a second metal film formed on the first gate insulating film.</p> <p>[0039] The semiconductor device shown in FIG. 1 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer 103A which is made of conductive metal and a second conductive layer 103B which is made of conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p>

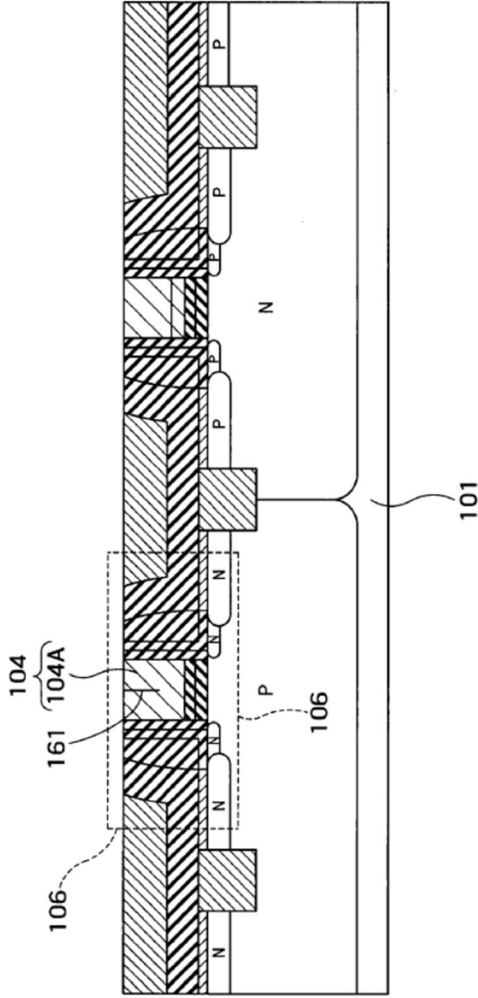
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<div data-bbox="289 499 711 1461"> </div> <p data-bbox="760 913 792 1050" style="text-align: center;">FIG. 2H</p> <p data-bbox="857 220 1036 1499">[0054] Note that although each side wall spacer of the first embodiment has a two-layer structure of the first side wall spacer 142 made of the silicon oxide film and the second side wall spacer 143 made of the silicon nitride film, it may have a one-layer structure, for example, of only a silicon nitride film or a laminated structure of three or more layers including, for example, a silicon oxide film and silicon nitride film.</p> <p data-bbox="1068 262 1250 1499">[0055] Next, as shown in FIG. 2I, silicide films 144 are formed in a self-aligned manner on the surfaces of the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET. Although NiSi films are adopted as the silicide films 144 in this embodiment, PtSi films, ErSi films, NiPtSi films, NiErSi films, or the like may be adopted as the silicide films 144 instead.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p style="text-align: center;">FIG. 2I</p> <p>[0056] Next, as shown in FIG. 2J, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 2J, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 2J, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the W layers 103B are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="829 884 867 1033">FIG. 2K</p> <p data-bbox="906 191 1162 1503">[0058] Next, as shown in FIG. 2L, in the NMOSFET region 106, the Ru layer 103A on the gate dielectric film 102 for the NMOSFET is etched in an atmosphere containing oxygen radical. With the above-described manufacturing step, the hafnium silicon oxynitride film 102B in the NMOSFET region 106 is exposed. The resist 231 may be removed before or after the removal of the Ru layer 103A. Through the above-described manufacturing steps, in the NMOSFET region 106, the dummy gate electrode 103 on the gate dielectric film 102 is removed, thereby forming a trench 151 on the gate dielectric film 102.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="852 850 901 1018">FIG. 2L</p> <p data-bbox="933 210 1193 1501">[0059] Next, as shown in FIG. 2M, conductive metal, which is a material for forming a third conductive layer 104A of the gate electrode 104 for the NMOSFET, is deposited over the entire surface by CVD. Examples of the conductive metal include TaSiN which is formed using pentakis(ethylmethylamino)tantalum, and ammonia, and ammoniac, HfN which is formed in an atmosphere containing tetrakis(ethylmethylamino)hafnium and ammonia, HfSi which is formed using tetrakis(ethylmethylamino)hafnium and tetrakis(ethylmethylamino)silicon, and WSi which is formed using tungsten hexafluoride and dichlorosilane.</p>

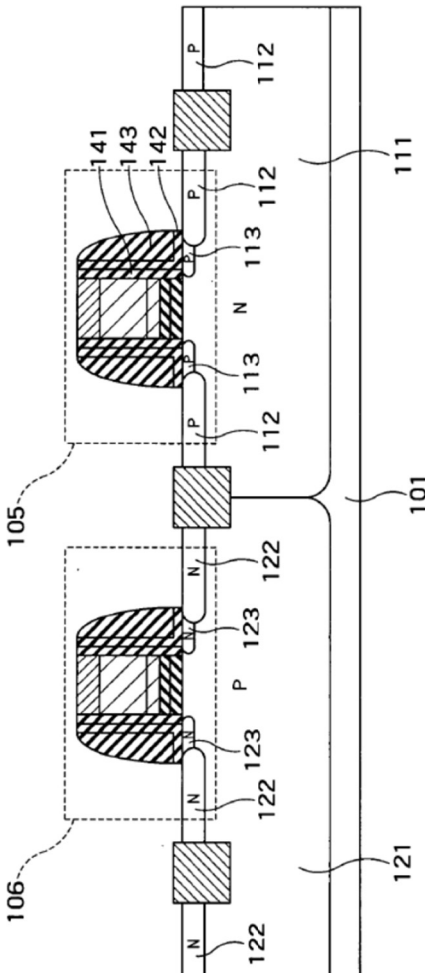
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="873 871 914 1024">FIG. 2M</p> <p data-bbox="976 247 1084 1499">[0060] Note that although the gate electrode 104 for the NMOSFET of the first embodiment has a one-layer structure of only the conductive layer 104A made of the conductive metal, it may have a laminated structure of two or more layers including a conductive layer made of conductive metal.</p> <p data-bbox="1117 212 1334 1499">[0061] Next, as shown in FIG. 2N, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback). Through the above-described manufacturing steps, in the NMOSFET region 106, the material for forming the gate electrode is buried in the trench 151 on the gate dielectric film 102, thereby forming the gate electrode 104 for the NMOSFET with a different configuration from that of the gate electrode 103 for the PMOSFET. Since the gate electrode 104 for the NMOSFET (the third conductive layer 104A) is formed in the hole by CVD, a trace of a streaky</p>

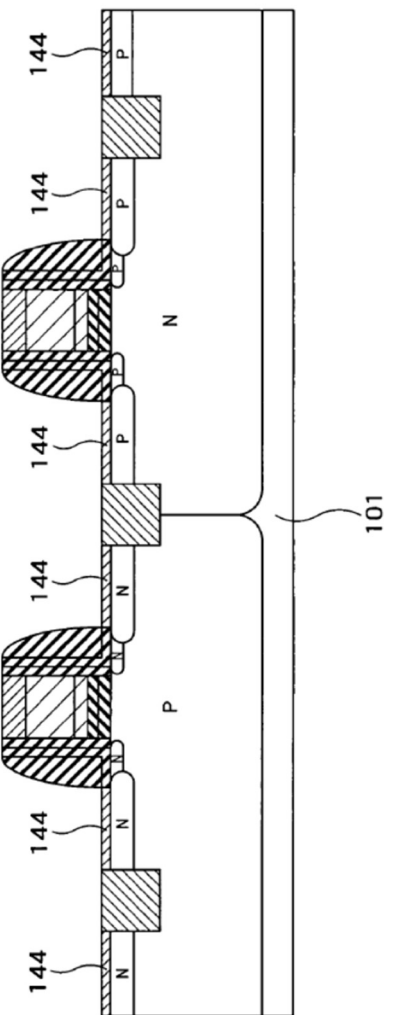
Claim	Claim Language	<p data-bbox="207 338 245 1367">Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama</p> <p data-bbox="264 216 334 1501">seam 161 which does not remain in the gate electrode 103 for the PMOSFET (the first conductive layer 103A and second conductive layer 103B) remains in the gate electrode 104 for the NMOSFET.</p> <div data-bbox="380 491 854 1482">  <p data-bbox="886 919 924 1058">FIG. 2N</p> </div> <p data-bbox="972 216 1154 1501">[0065] Moreover, in the first embodiment, the gate electrode 104 for the NMOSFET is formed after the source/drain diffusion layer 112 (and extension diffusion layer 113) for the PMOSFET and the source/drain diffusion layer 122 (and extension diffusion layer 123) for the NMOSFET are formed. Accordingly, the possibility of change in the work function of the metal electrode of the NMOSFET in the step of forming the source/drain diffusion layers (and extension diffusion layers) is reduced.</p> <p data-bbox="1174 191 1356 1501">[0066] Therefore, in the first embodiment, gate dielectric films with preferable characteristics such as a preferable film quality, and gate electrodes with preferable characteristics such as a preferable work function, can be used as gate dielectric films and gate electrodes constituting a PMOSFET and an NMOSFET. Accordingly, in the first embodiment, it is possible to manufacture a semiconductor device including a high-performance CMOSFET.</p>
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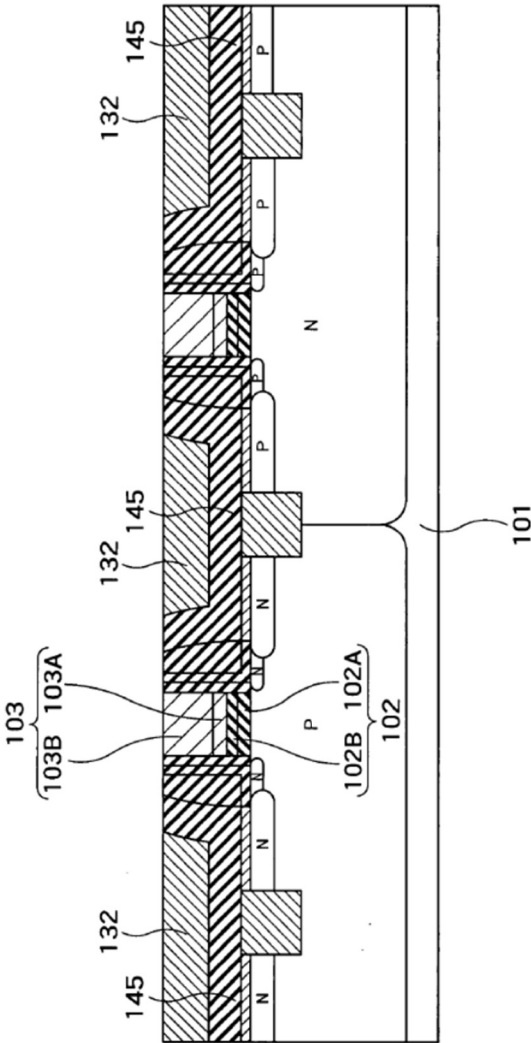
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>[0067] Additionally, in the first embodiment, the gate electrode 103 for the PMOSFET is formed by etching before formation of the inter layer dielectric film 132, and the gate electrode 104 for the NMOSFET is formed by the damascene process after formation of the inter layer dielectric film 132. Further, in the first embodiment, the gate electrode 103 for the PMOSFET formed in the NMOSFET region is used as a dummy electrode substituting for the gate electrode 104 for the NMOSFET. Therefore, in the first embodiment, the gate electrode 103 for the PMOSFET formed in the NMOSFET region is not wastefully removed in the etching step, and effectively used as the dummy electrode substituting for the gate electrode 104 for the NMOSFET until it is removed prior to the damascene process. Furthermore, in the first embodiment, since the step of forming the dummy electrode is integrated into the step of forming the gate electrode 103 for the PMOSFET, the number of steps required for the formation of the dummy electrode can be saved.</p> <p>[0068] In the damascene gate process explained as a background art, a dummy gate dielectric film (silicon oxide) is damaged in removing a dummy gate electrode (polysilicon), so it is necessary to remove also the dummy gate dielectric film in removing the dummy gate electrode. However, in the first embodiment, the dummy electrode in contact with the gate dielectric film 102 (second dielectric film 102B) made of the high-permittivity dielectric film, is the gate electrode 103 for the PMOSFET (first conductive layer 103A) made of the conductive metal. Particularly, in the first embodiment, the conductive metal is Ru, which is conductive metal capable of being removed without a chemical solution. Accordingly, in the first embodiment, it is possible to avoid unnecessary damage to the gate dielectric film 102 and unnecessary removal of the gate dielectric film 102, in removing the dummy electrode.</p> <p>[0072] The semiconductor device shown in FIG. 3 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer</p>

EXHIBIT 686A2

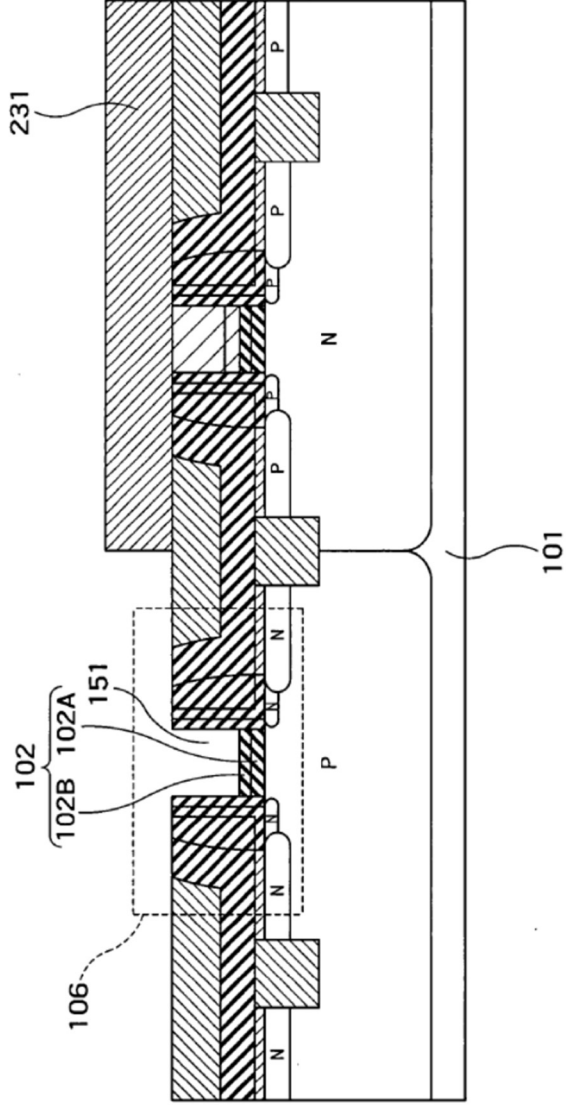
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>103A which is made of conductive metal and a second conductive layer 103B which is made of conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p> <p>FIG. 3</p> <p>[0086] Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 4H. Also, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 4H. Then, side wall spacers 143, each of which is made of a silicon nitride film, are</p>

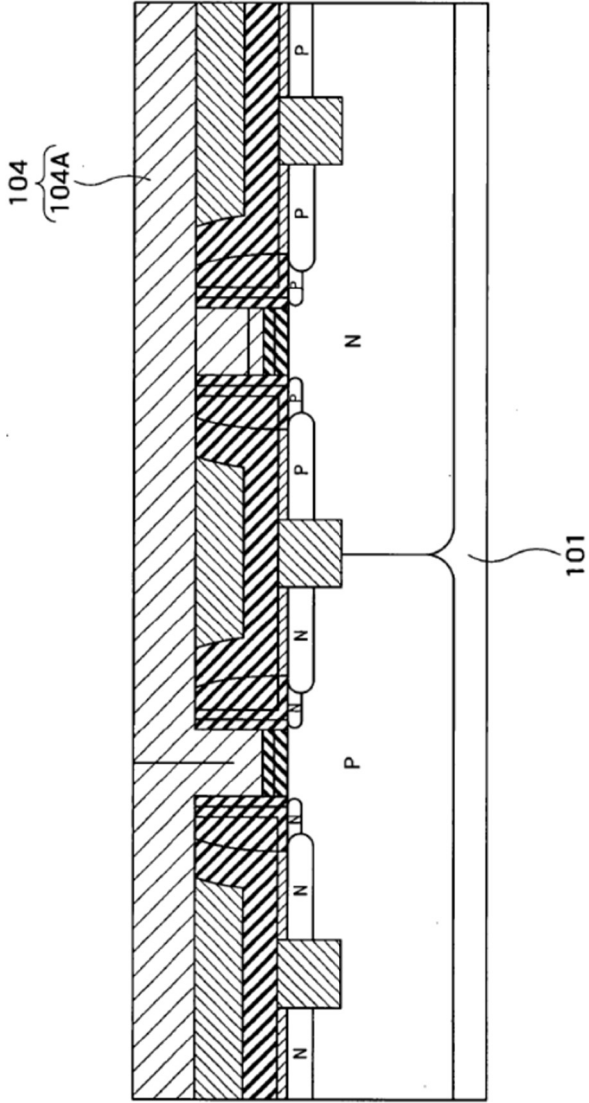
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.</p>  <p>FIG. 4H</p> <p>[0087] Next, as shown in FIG. 4I, silicide films 144 are formed in a self-aligned manner on the surfaces of the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="706 934 755 1060">FIG. 4I</p> <p data-bbox="828 199 1047 1501">[0088] Next, as shown in FIG. 4J, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 4J, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 4J, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the TiN layers 103B are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		 <p data-bbox="829 898 867 1031">FIG. 4J</p> <p data-bbox="915 218 1062 1499">[0089] Next, as shown in FIG. 4K, in the NMOSFET region 106, the TiN layer 103B above the gate dielectric film 102 for the NMOSFET is etched using a resist 231 as a mask and using a chemical solution such as a solution containing hydrogen peroxide. With the above-described manufacturing step, the W layer 103A in the NMOSFET region 106 is exposed.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<div data-bbox="277 438 797 1472"> </div> <p data-bbox="829 884 862 1031">FIG. 4K</p>

Claim	Claim Language	<p data-bbox="207 338 245 1367">Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama</p> <div data-bbox="284 380 846 1478">  <p data-bbox="878 852 915 1010">FIG. 4L</p> </div> <p data-bbox="964 279 1105 1499">[0091] Next, as shown in FIG. 4M, conductive metal, which is a material for forming a third conductive layer 104A of the gate electrode 104 for the NMOSFET, is deposited over the entire surface by CVD. Examples of the conductive metal include TaC, which is formed using pentakis(dimethylamino)tantalum and methane.</p>
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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<div data-bbox="272 384 857 1480">  </div> <div data-bbox="889 856 927 1010"> <p>FIG. 4M</p> </div> <div data-bbox="971 191 1393 1501"> <p>[0092] Note that although the gate electrode 104 for the NMOSFET of the second embodiment has a one-layer structure of only the conductive layer 104A made of the conductive metal, it may have a laminated structure of two or more layers including a conductive layer made of conductive metal.</p> <p>[0093] Next, as shown in FIG. 4N, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback). Through the above-described manufacturing steps, in the NMOSFET region 106, the material for forming the gate electrode is buried in the trench 151 on the gate dielectric film 102, thereby forming the gate electrode 104 for the NMOSFET with a different configuration from that of the gate electrode 103 for the PMOSFET. Since the gate electrode 104 for the NMOSFET (the third conductive layer 104A) is formed in the hole by CVD, a trace of a streaky seam 161 which does not remain in the gate electrode 103 for the PMOSFET (the first conductive layer 103A and second conductive layer 103B) remains in the gate electrode 104 for the NMOSFET.</p> </div>

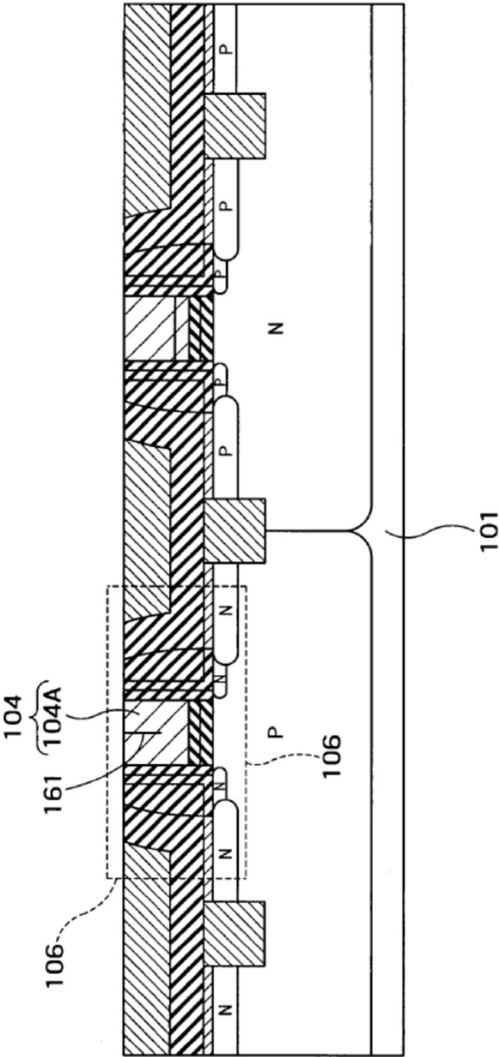
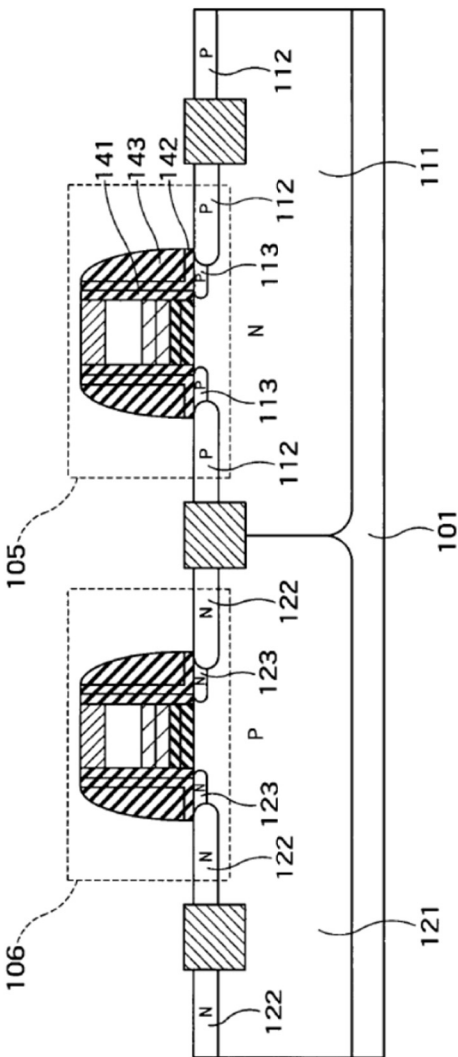
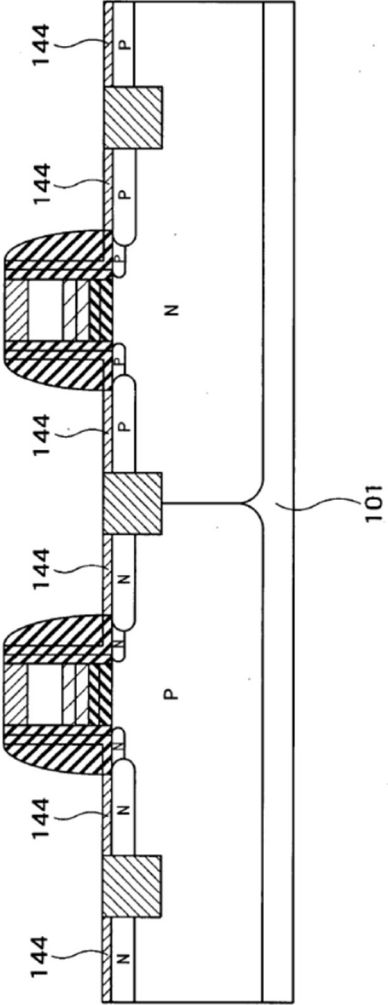
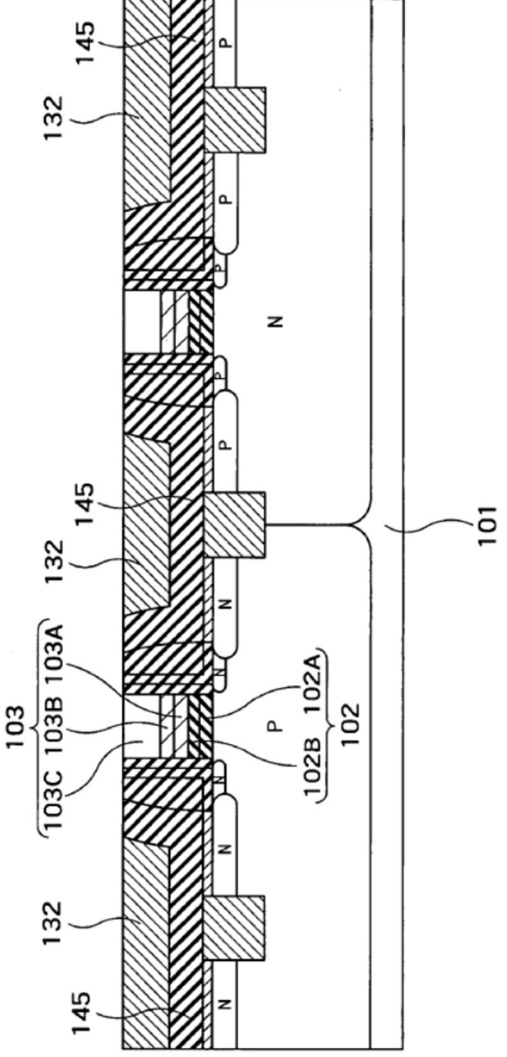
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="795 871 836 1018">FIG. 4N</p> <p data-bbox="860 210 1015 1501">[0095] In the second embodiment, the dummy electrode (the gate electrode 103 for the PMOSFET) includes the W layer 103A and TiN layer 103B made of W and TiN respectively, which are conductive metals capable of being removed using a chemical solution. For this reason, in the second embodiment, it is possible to easily remove the dummy electrode at low cost.</p> <p data-bbox="1039 210 1396 1501">[0098] The semiconductor device shown in FIG. 5 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes three electrode-constituting layers: a first conductive</p>

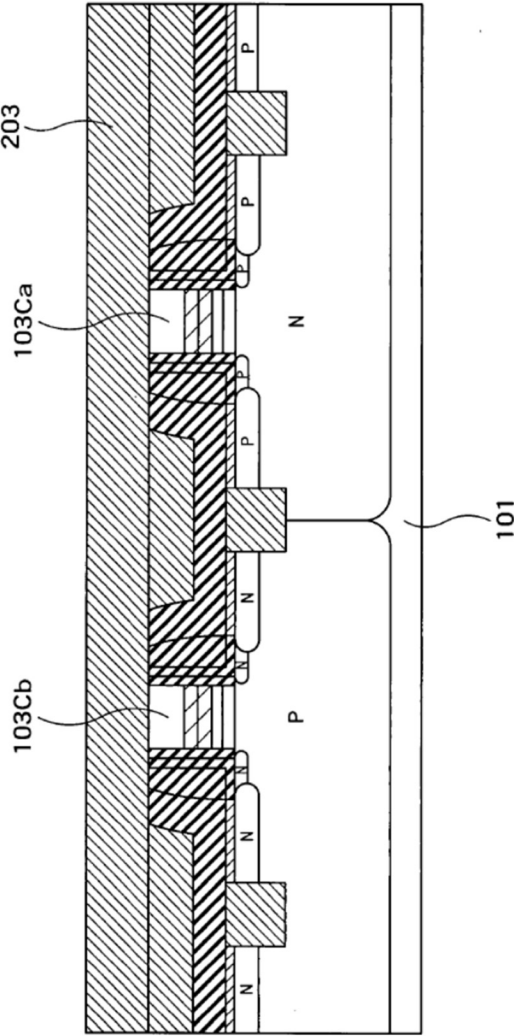
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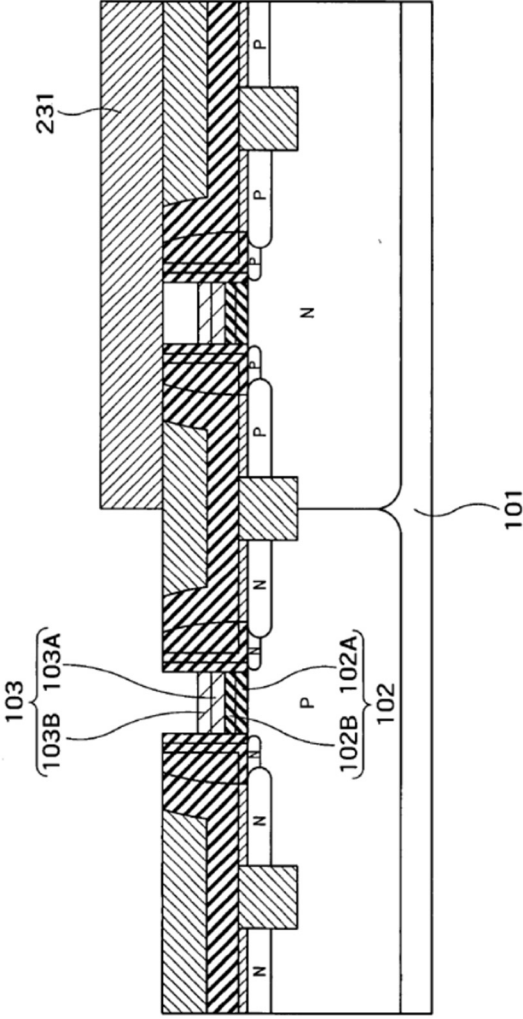
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>layer 103A which is made of conductive metal, a second conductive layer 103B which is made of conductive metal, and a semiconductor layer 103C which is made of semiconductor. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p> <p>The diagram shows a cross-section of a semiconductor device. At the bottom is a substrate 121. Above it are several layers and regions. On the left, there's a region 122 containing N-type dopants, with a P-type region 123 above it. This is followed by a well diffusion layer 122 and a PMOSFET region 101. The PMOSFET has a gate stack 103 (comprising 103A, 103B, and 103C) and a gate electrode 104 (comprising 104A). To the right of the PMOSFET is an NMOSFET region 111. It has a well diffusion layer 121, a source/drain diffusion layer 122, and a gate stack 103 (comprising 103A, 103B, and 103C). The gate electrode 104 for the NMOSFET is also shown. Various other regions like 131, 132, 112, 113, 102A, and 102B are indicated throughout the structure.</p> <p style="text-align: center;">FIG. 5</p> <p>[0111] Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 6I. Also, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 6J. Then, side wall spacers 143, each of which is made of a silicon nitride film, are</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.</p>  <p style="text-align: center;">FIG. 6I</p> <p>[0112] Next, as shown in FIG. 6J, silicide films 144 are formed in a self-aligned manner on the surfaces of the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p style="text-align: center;">FIG. 6J</p> <p>[0113] Next, as shown in FIG. 6K, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 6K, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 6K, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the semiconductor layers 103C (non-diffusion layers 103Ca and diffusion layers 103Cb) are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="787 892 836 1060">FIG. 6K</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="820 903 868 1050">FIG. 6L</p> <p data-bbox="933 199 1079 1501">[0115] Next, as shown in FIG. 6M, in the NMOSFET region 106, the semiconductor layer 103C above the gate dielectric film 102 for the NMOSFET is etched using a resist 231 as a mask and using a chemical solution such as a solution containing hydrogen peroxide. With the above-described manufacturing steps, the TiN layer 103B in the NMOSFET region 106 is exposed.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="829 888 862 1031">FIG. 6M</p> <p data-bbox="927 222 1068 1499">[0116] Next, as shown in FIG. 6N, in the NMOSFET region 106, the TiN layer 103B above the gate dielectric film 102 for the NMOSFET is etched using the resist 231 as a mask and using a chemical solution such as a solution containing hydrogen peroxide. With the above-described manufacturing step, the W layer 103A in the NMOSFET region 106 is exposed.</p>

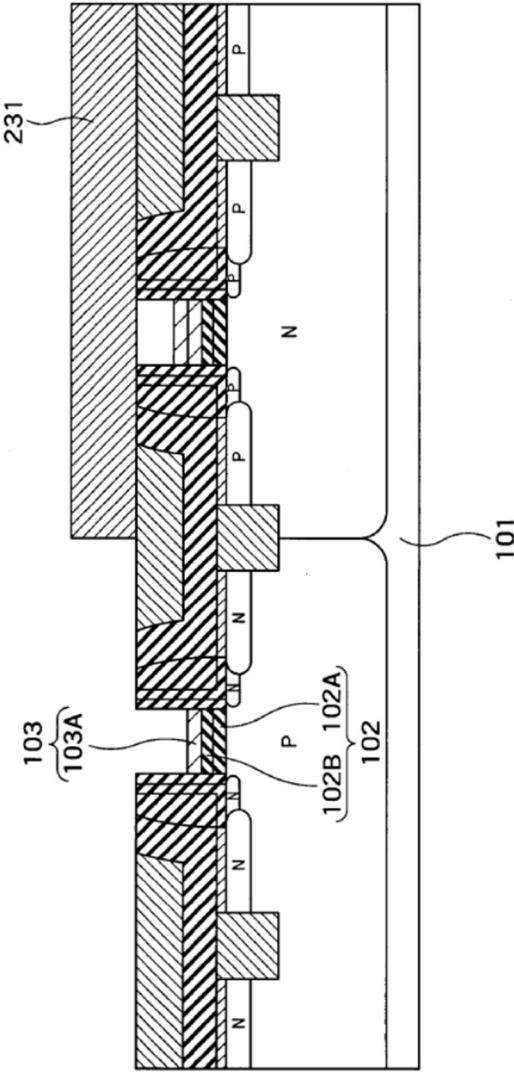
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="828 877 868 1024">FIG. 6N</p> <p data-bbox="933 210 1185 1501">[0117] Next, as shown in FIG. 6O, in the NMOSFET region 106, the W layer 103A on the gate dielectric film 102 for the NMOSFET is etched using the resist 231 as a mask and using a chemical solution such as a solution containing hydrogen peroxide. With the above-described manufacturing step, the hafnium silicon oxynitride film 102B in the NMOSFET region 106 is exposed. Through the above-described manufacturing steps, in the NMOSFET region 106, the dummy gate electrode 103 on the gate dielectric film 102 is removed, thereby forming a trench 151 on the gate dielectric film 102.</p>

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Claim	Claim Language	<p>Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama</p>
		<p>FIG. 60</p> <p>[0118] Next, as shown in FIG. 6P, conductive metal, which is a material for forming a third conductive layer 104A of the gate electrode 104 for the NMOSFET, is formed over the entire surface by CVD. Examples of the conductive metal include TaCN, which is formed using trisdimethylamino-mono-t-amyiminotantalum and monomethylamine.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<div data-bbox="272 451 812 1470"> </div> <p data-bbox="841 892 880 1039">FIG. 6P</p> <p data-bbox="928 193 1253 1501">[0119] Next, as shown in FIG. 6Q, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback). Through the above-described manufacturing steps, in the NMOSFET region 106, the material for forming the gate electrode is buried in the trench 151 on the gate dielectric film 102, thereby forming the gate electrode 104 for the NMOSFET with a different configuration from that of the gate electrode 103 for the PMOSFET. Since the gate electrode 104 for the NMOSFET (the third conductive layer 104A) is formed in the hole by CVD, a trace of a streaky seam 161 which does not remain in the gate electrode 103 for the PMOSFET (the first conductive layer 103A, second conductive layer 103B, and semiconductor layer 103C) remains in the gate electrode 104 for the NMOSFET.</p>

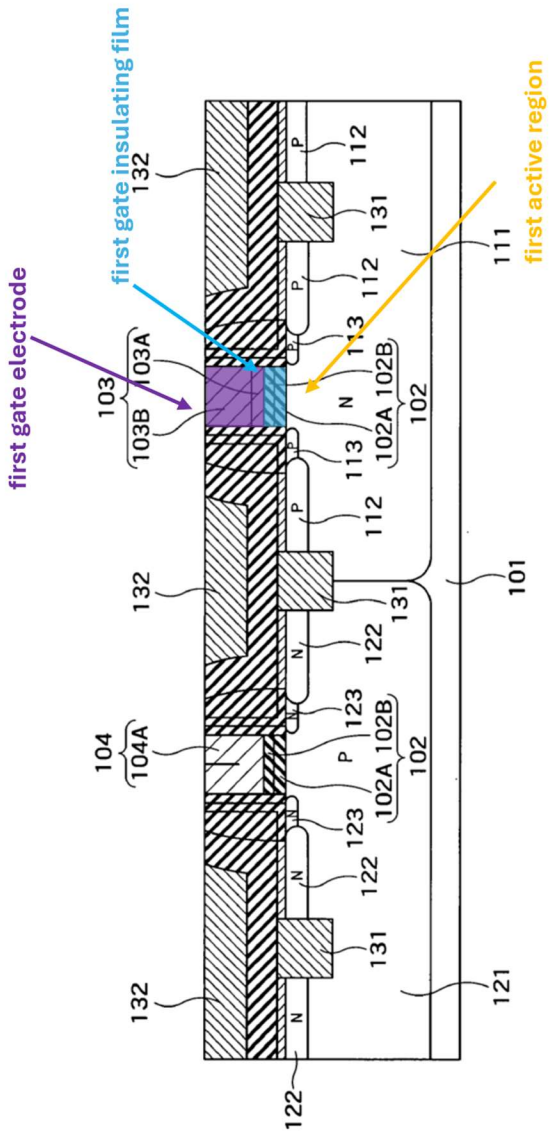
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<div data-bbox="272 449 760 1472"> </div> <p data-bbox="792 890 824 1037">FIG. 6Q</p> <p data-bbox="878 218 1052 1499">[0121] In the third embodiment, the gate electrode 103 for the PMOSFET includes the first conductive layer 103A made of the conductive metal, the second conductive layer 103B made of the conductive metal, and the semiconductor layer (silicide layer) 103C made of the semiconductor (silicide). For this reason, in the third embodiment, the gate resistance of the PMOSFET is relatively low.</p> <p data-bbox="1094 218 1305 1499">The description and annotation below are an example of a first gate electrode including a second metal film formed on the first gate insulating film. For example, as can be seen in Figs. 1-2N, Aoyama discloses a gate electrode 104 for the NMOSFET comprising conductive layer 104A, made of TaSiN, HfN, HfSi, or WSi. In this example, 104A is the second metal film. Alternatively, Aoyama discloses gate electrode 104 may be made of two or more layers including a conductive layer made of conductive metal.</p>

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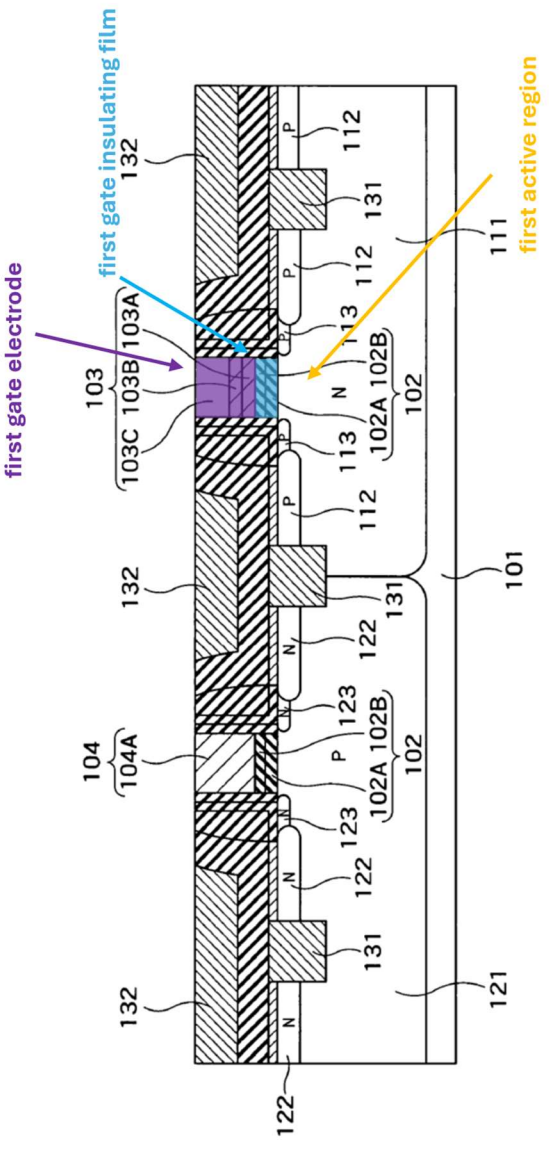
Claim		Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
Claim Language	<p>first gate electrode</p> <p>first gate insulating film</p> <p>first MIS transistor</p> <p>second MIS transistor</p> <p>FIG. 1</p>	<p>Alternatively, Aoyama discloses e.g., a gate electrode 103 for the PMOSFET includes a Ru (ruthenium) layer 103A and a W (tungsten) layer 103B. The gate electrode is also disclosed as only a Ru layer. In this example, 103A is the second metal film.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<p>first gate electrode</p> <p>first gate insulating film</p> <p>second MIS transistor</p> <p>FIG. 1</p> <p>first MIS transistor</p> <p>first active region</p> <p>As another example, as can be seen in Figs. 3-4N, Aoyama discloses a gate electrode 104 for the NMOSFET comprising conductive layer 104A, made of TaC. Alternatively, Aoyama discloses gate electrode 104 may be made of two or more layers including a conductive layer made of conductive metal. In this example, 104A is the second metal film.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<div data-bbox="267 210 933 1501"> <p>first gate electrode (104, 104A)</p> <p>first gate insulating film (132)</p> <p>first MIS transistor (102)</p> <p>second MIS transistor (103)</p> <p>first active region (121)</p> </div> <p>FIG. 3</p> <p>Alternatively, as can be seen in Figs. 3-4N, Aoyama discloses e.g., a gate electrode 103 for the PMOSFET includes a W (tungsten) layer 103A and a TiN (titanium nitride) layer 103B. The gate electrode is also disclosed as only a Ru layer. The gate electrode 103 is also disclosed as only a W layer. In this example, 103A is the second metal film.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p>FIG. 3</p> <p>second MIS transistor</p> <p>first MIS transistor</p> <p>first gate electrode</p> <p>first gate insulating film</p> <p>first active region</p> <p>As yet another example, as can be seen in Figs. 5-6N, Aoyama discloses a gate electrode 104 for the NMOSFET comprising conductive layer 104A, made of TaCN. In this example, 104A is the second metal film.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<p>first gate electrode</p> <p>first gate insulating film</p> <p>first active region</p> <p>first MIS transistor</p> <p>second MIS transistor</p> <p>FIG. 5</p> <p>In the alternative, as can be seen in Figs. 5-6N, Aoyama discloses e.g., a gate electrode 103 for the PMOSFET includes a W (tungsten) layer 103A, a TiN (titanium nitride) layer 103B, and a polysilicon or silicide layer 103C. In this example, 103A is the second metal film.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
25 [c.3]	first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and	 <p style="text-align: center;">FIG. 5 second MIS transistor first MIS transistor</p>
25 [c.3]	first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and	<p>Aoyama, as evidenced by the example citations below, discloses first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative.</p> <p>[0039] The semiconductor device shown in FIG. 1 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102A in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer</p>

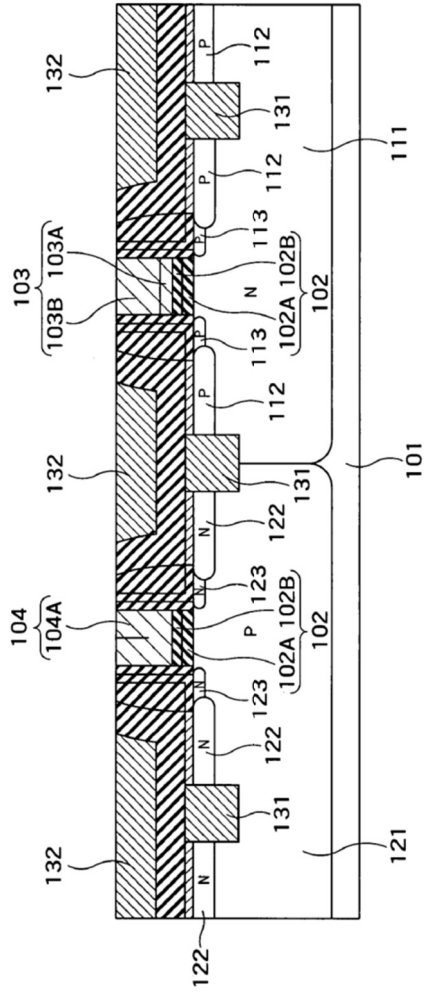
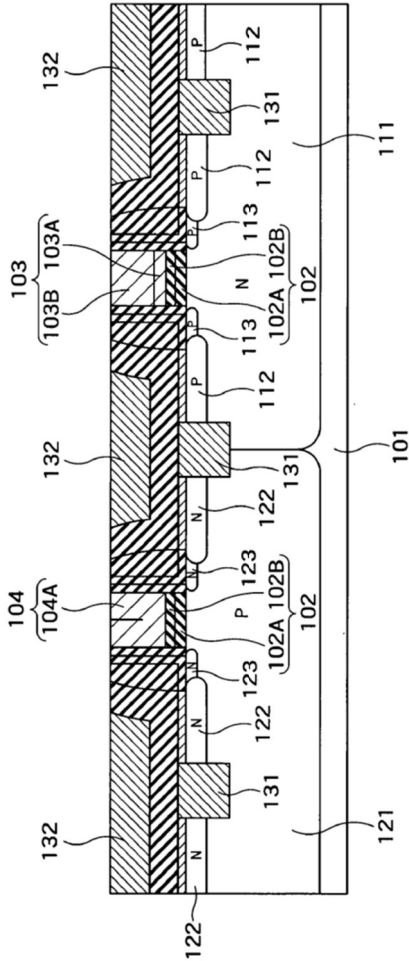
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<p>103A which is made of conductive metal and a second conductive layer 103B which is made of conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p>  <p>FIG. 1</p> <p>[0053] Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 2H. Also, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 2H. In some cases, halo implantation is further performed to suppress short channel effect.</p>

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Claim		
Claim Language		<p>Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama</p> <p>effects. Then, side wall spacers 143, each of which is made of a silicon nitride film, are formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.</p>
		<p>FIG. 2H</p> <p>[0054] Note that although each side wall spacer of the first embodiment has a two-layer structure of the first side wall spacer 142 made of the silicon oxide film and the second side wall spacer 143 made of the silicon nitride film, it may have a one-layer structure, for example, of only a silicon nitride film or a laminated structure of three or more layers including, for example, a silicon oxide film and silicon nitride film.</p> <p>[0072] The semiconductor device shown in FIG. 3 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate</p>

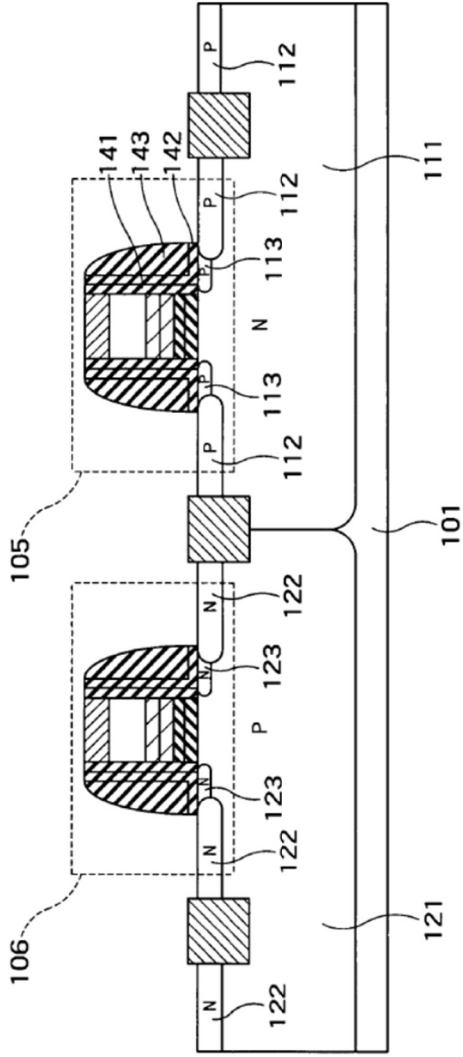
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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer 103A which is made of conductive metal and a second conductive layer 103B which is made of conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p>  <p style="text-align: center;">FIG. 3</p> <p>[0086] Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111</p>

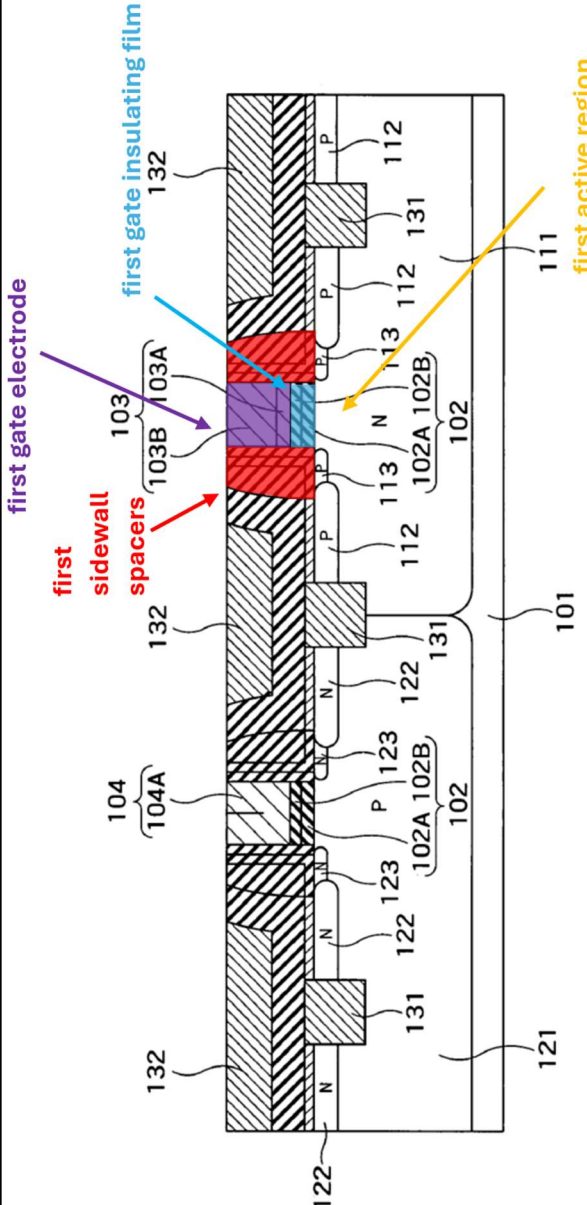
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 4H. Also, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 4H. Then, side wall spacers 143, each of which is made of a silicon nitride film, are formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.</p>

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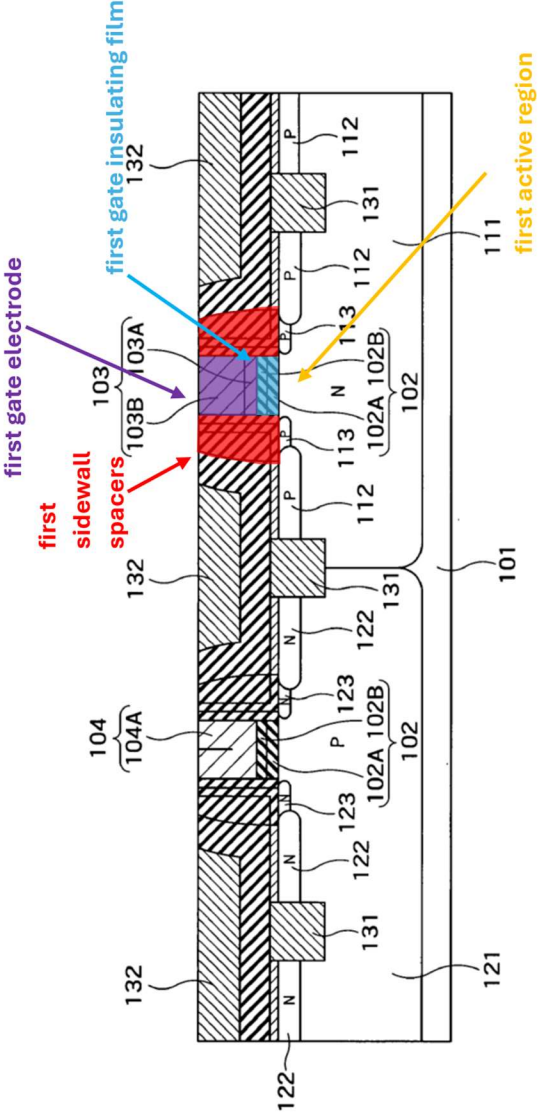
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes three electrode-constituting layers: a first conductive layer 103A which is made of conductive metal, a second conductive layer 103B which is made of conductive metal, and a semiconductor layer 103C which is made of semiconductor. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p> <p style="text-align: center;">FIG. 5</p> <p>[0111] Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the source/drain</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 6I. Also, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 6I. Then, side wall spacers 143, each of which is made of a silicon nitride film, are formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.</p>  <p style="text-align: center;">FIG. 6I</p> <p>The description and annotation below are an example of first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative. For example, as can be seen in Figs. 1-2N, Aoyama discloses first sidewall spacers, e.g., offset spacer 141, side wall spacer 142, and side wall spacer 143. Aoyama discloses the spacers may be made of either silicon oxide or</p>

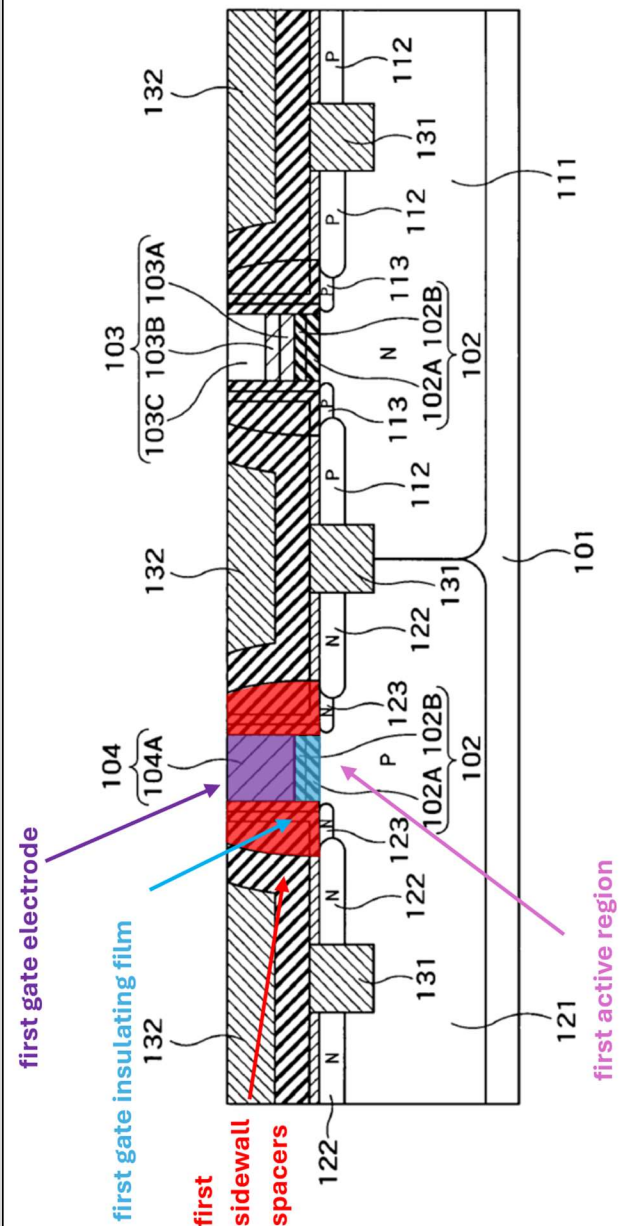
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>silicon nitride. It also discloses the sidewall spacers could have a one-layer structure or three or more layers.</p> <p>first gate electrode</p> <p>first gate insulating film</p> <p>first sidewall spacers</p> <p>first active region</p> <p>second MIS transistor</p> <p>FIG. 1</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p>first gate electrode</p> <p>first sidewall spacers</p> <p>first gate insulating film</p> <p>second MIS transistor</p> <p>first MIS transistor</p> <p>first active region</p> <p>FIG. 1</p> <p>As another example, as can be seen in Figs. 3-4N, Aoyama discloses first sidewall spacers, e.g., offset spacer 141, side wall spacer 142, and side wall spacer 143. Aoyama discloses the spacers may be made of either silicon oxide or silicon nitride.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>FIG. 3 second MIS transistor</p> <p>first MIS transistor</p> <p>first active region</p> <p>first gate electrode</p> <p>first gate insulating film</p> <p>first sidewall spacers</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p>FIG. 3</p> <p>second MIS transistor</p> <p>first MIS transistor</p> <p>first gate electrode</p> <p>first active region</p> <p>first gate insulating film</p> <p>first sidewall spacer</p>

As yet another example, as can be seen in Figs. 5-6N, Aoyama discloses first sidewall spacers, e.g., offset spacer 141, side wall spacer 142, and side wall spacer 143. Aoyama discloses the spacers may be made of either silicon oxide or silicon nitride.

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p>first gate electrode</p> <p>first gate insulating film</p> <p>first MIS transistor</p> <p>second MIS transistor</p> <p>first active region</p> <p>sidewall spacers</p> <p>FIG. 5</p>

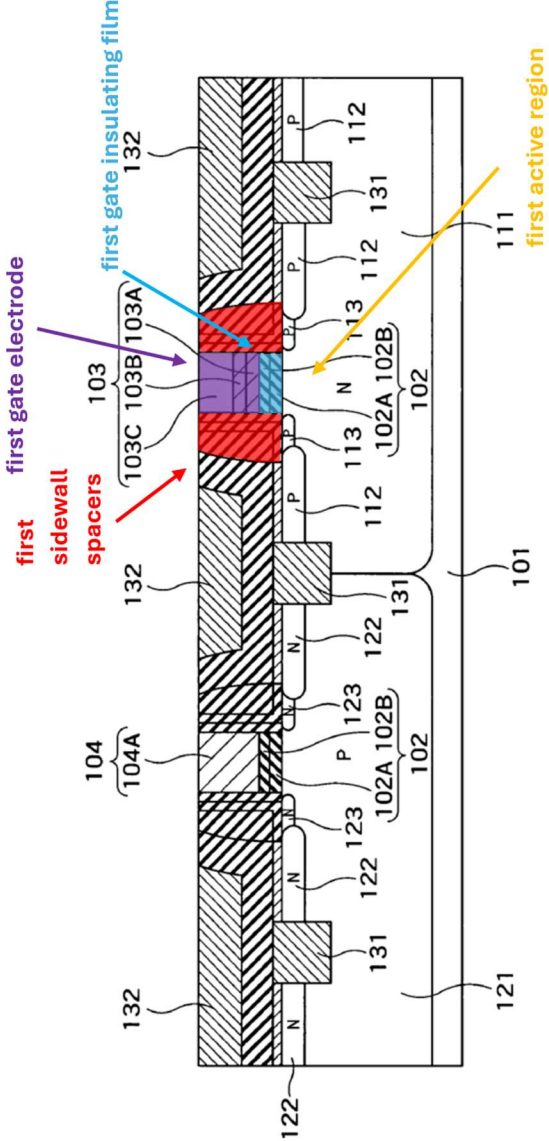
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p>first gate electrode</p> <p>first gate insulating film</p> <p>first active region</p> <p>first MIS transistor</p> <p>second MIS transistor</p>

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<p>25 [c.4]</p>	<p>a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,</p>	<p>Aoyama, as evidenced by the example citations below, discloses a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers.</p> <p>[0056] Next, as shown in FIG. 2J, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 2J, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 2J, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the W layers 103B are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p> <div data-bbox="617 462 1153 1470"> </div> <p>FIG. 2J</p> <p>[0088] Next, as shown in FIG. 4J, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 4J, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 4J, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching).</p>
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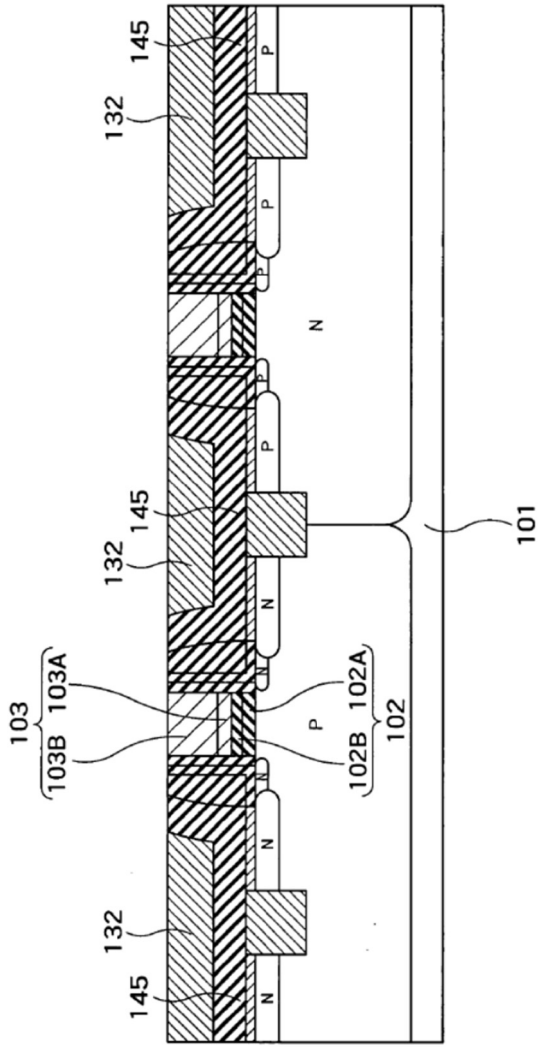
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>With the above-described manufacturing steps, the TiN layers 103B are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>  <p style="text-align: center;">FIG. 4J</p> <p>[0113] Next, as shown in FIG. 6K, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 6K, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 6K, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the semiconductor layers 103C (non-diffusion layers 103Ca and diffusion layers 103Cb) are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>

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Claim		Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
Claim Language		<p>The diagram shows a cross-section of a semiconductor device. A central layer is labeled 101. Above it are two regions labeled 102A and 102B, which are part of a larger group 102. These regions are separated by a narrow gap. To the left of the gap is a region labeled 103, which contains sub-regions 103A, 103B, and 103C. Various other layers and features are labeled with numbers 132, 145, and 148. Some areas are hatched to indicate specific materials or structures.</p>
		<p>The description and annotation below are an example of a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers. For example, as can be seen in Figs. 1-2N, Aoyama discloses etch stopper film 145 made of silicon nitride.</p>

Claim	Claim Language	<p data-bbox="207 338 245 1360">Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama</p> <div data-bbox="261 317 857 1486"> <p data-bbox="269 779 293 1335">first gate electrode</p> <p data-bbox="269 989 293 1335">silicon nitride film</p> <p data-bbox="370 1178 394 1476">first gate insulating film</p> <p data-bbox="440 1377 464 1486">first sidewall spacers</p> <p data-bbox="902 1052 927 1276">first MIS transistor</p> <p data-bbox="902 411 927 684">second MIS transistor</p> <p data-bbox="886 789 927 905">FIG. 1</p> </div>
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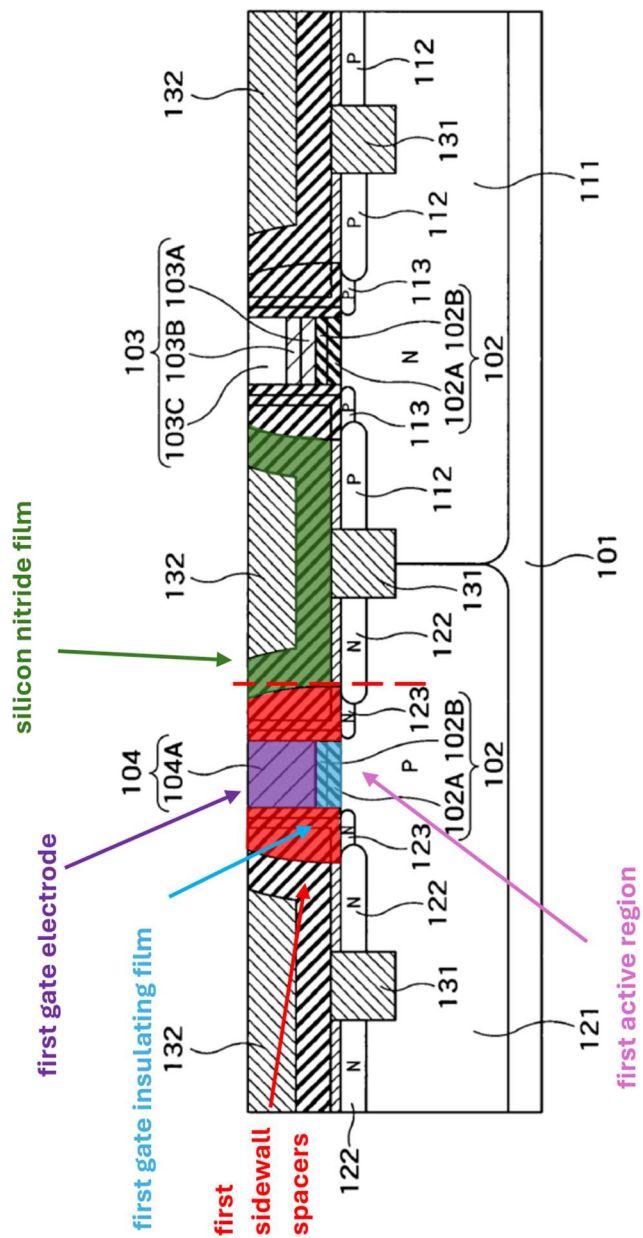
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[illegible]

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>FIG. 3</p> <p>first gate electrode</p> <p>first gate insulating film</p> <p>silicon nitride film</p> <p>first active region</p> <p>first MIS transistor</p> <p>second MIS transistor</p>

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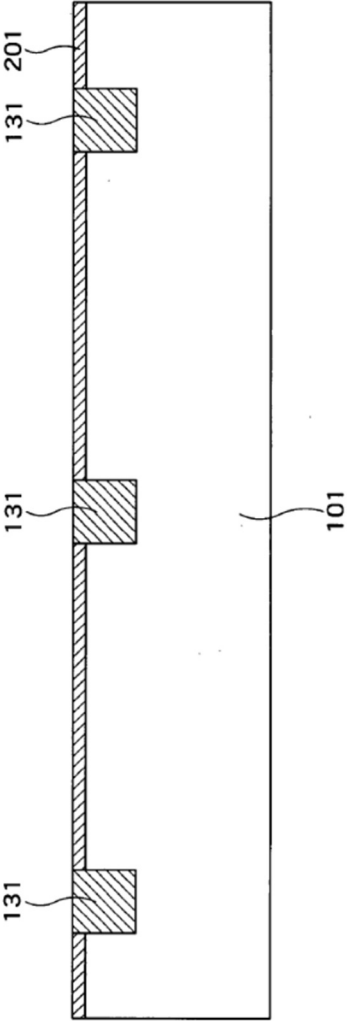
As yet another example, as can be seen in Figs. 5-6N, Aoyama discloses etch stopper film 145 made of silicon nitride.

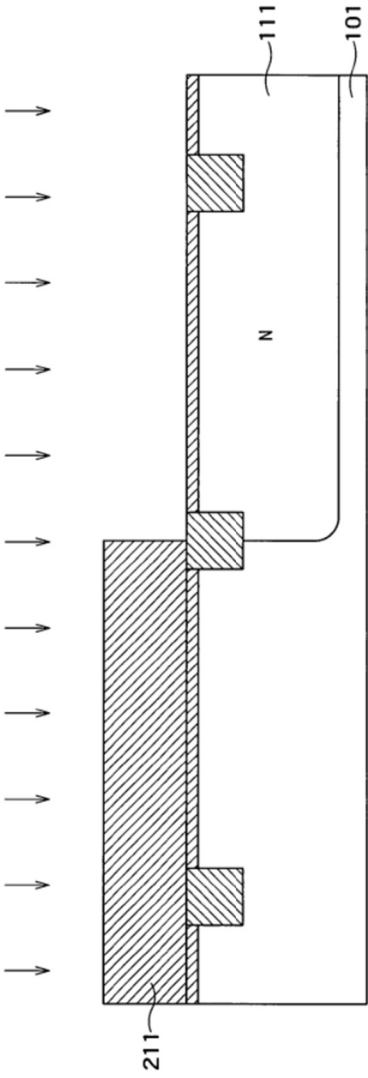


second MIS transistor

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Claim	Claim Language	<p>Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama</p> <p>conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p>
		<p>FIG. 1</p> <p>[0044] First, as shown in FIG. 2A, silicon oxide films are buried in predetermined regions of a silicon substrate 101 to form isolation layers 131 of STIs. Then, as shown in FIG. 2A, a silicon oxide film (dielectric film) 201 is formed on the silicon substrate 101.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		 <p style="text-align: center;">FIG. 2A</p> <p>[0045] Next, as shown in FIG. 2B, ions of P (phosphorus) are implanted into the substrate 101 using a resist 211 as a mask. The implantation of P ions is performed to form the well diffusion layer 111 for the PMOSFET and to adjust the threshold voltage of the PMOSFET, and performed a plurality of times. In some cases, ions of B (boron), In (indium), or the like are further implanted to finely adjust the threshold voltage of the PMOSFET.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		 <p style="text-align: center;">FIG. 2B</p> <p>[0046] Next, as shown in FIG. 2C, ions of B (boron) are implanted into the substrate 101 using a resist 221 as a mask. The implantation of B ions is performed to form the well diffusion layer 121 for the NMOSFET and to adjust the threshold voltage of the NMOSFET, and performed a plurality of times. In some cases, ions of P (phosphorus), As (arsenic), or the like are further implanted to finely adjust the threshold voltage of the NMOSFET. After that, the substrate 101 is subjected to thermal diffusion processing, thereby completing the well diffusion layer 111 for the PMOSFET and the well diffusion layer 121 for the NMOSFET.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<div data-bbox="277 428 675 1503"> </div> <p data-bbox="743 915 781 1050">FIG. 2C</p> <p data-bbox="816 191 1328 1503">[0047] Next, as shown in FIG. 2D, the dielectric film 201 is removed from the substrate 101 using an ammonium fluoride aqueous solution, and the surface of the substrate 101 is cleaned using 0.5 to 5.0% hydrofluoric acid. Then, as shown in FIG. 2D, a silicon oxide film (a first dielectric film of a gate dielectric film) 102A with a thickness of 0.5 to 0.8 nm is formed on the substrate 101 in an atmosphere containing oxygen, and a hafnium silicate film (a second dielectric film of the gate dielectric film) 102B with a thickness of about 2.0 nm is formed on the silicon oxide film 102A using tetrakis(diethylamino)hafnium, tetrakis(dimethylamino)silicon, and oxygen. After that, the substrate 101 is subjected to annealing at 600° C., thereby densifying the silicon oxide film 102A and hafnium silicate film 102B. After that, the substrate 101 is processed in a nitrogen plasma atmosphere or ammonia atmosphere and then subjected to annealing at 1,000° C., thereby reforming the hafnium silicate film 102B into a hafnium silicon oxynitride film 102B. With the above-described manufacturing steps, the gate dielectric film 102 common to the PMOSFET and the NMOSFET is formed, ranging from a PMOSFET region 105 to a NMOSFET region 106, on the substrate 101. The PMOSFET region 105 is a region where the PMOSFET is to be formed, which is a specific example</p>

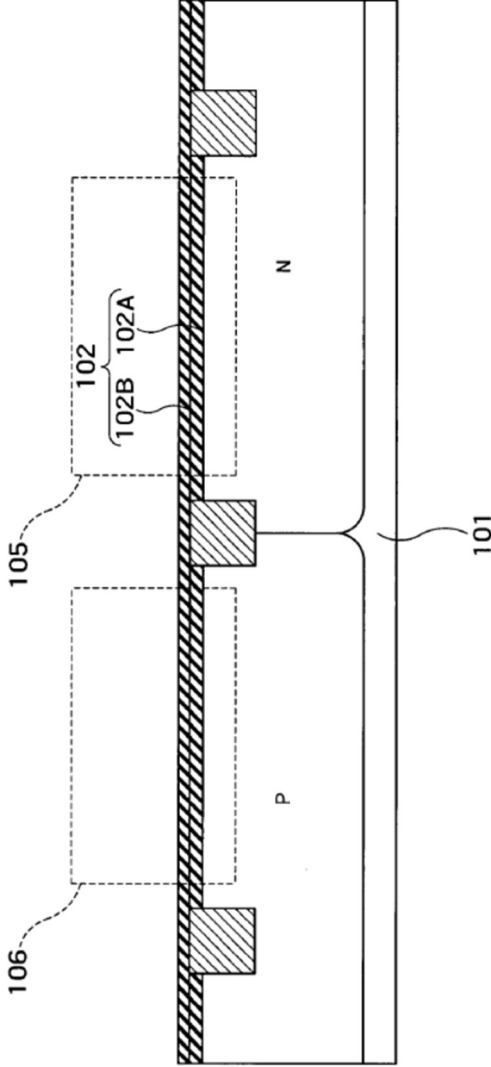
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>of a P-type FET region, and the NMOSFET region 106 is a region where the NMOSFET is to be formed, which is a specific example of an N-type FET region.</p>  <p style="text-align: center;">FIG. 2D</p> <p>[0048] Note that although the gate dielectric film 102 of the first embodiment has a two-layer structure of the silicon oxide film 102A and hafnium silicon oxynitride film 102B, it may have a one-layer structure of only a hafnium silicon oxynitride film or a laminated structure of three or more layers including a hafnium silicon oxynitride film.</p> <p>[0049] Next, as shown in FIG. 2E, a Ru (ruthenium) layer (a first conductive layer of a gate electrode for the PMOSFET) 103A with a thickness of about 20 nm is deposited on the hafnium silicon oxynitride film 102B using bis(cyclopentadienyl)ruthenium and oxygen, and a W (tungsten) layer (a second conductive layer of the gate electrode for the PMOSFET) 103B with a thickness of about 60 nm is deposited on the Ru layer 103A using tungsten hexafluoride, silane, and hydrogen. With the above-described manufacturing steps, the gate electrode layer 103 for the PMOSFET is formed,</p>

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Claim	Claim Language	<p>Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama</p>
		<p>ranging from the PMOSFET region 105 to the NMOSFET region 106, on the gate dielectric film 102.</p> <div data-bbox="394 430 898 1470"> </div> <p style="text-align: center;">FIG. 2E</p> <p>[0050] Note that although the gate electrode layer 103 for the PMOSFET of the first embodiment has a two-layer structure of the Ru layer 103A and W layer 103B, it may have a one-layer structure of only a Ru layer or a laminated structure of three or more layers including a Ru layer. The two-layer structure of the gate electrode layer 103 for the PMOSFET of the first embodiment is mainly due to the thickness of the Ru layer 103A. Since Ru has not only advantages such as a high work function but also disadvantages such as costliness, the thickness of the Ru layer 103A is made small in the first embodiment. For this reason, in the first embodiment, migration and even agglomeration may occur in the Ru layer 103A, for example, at the time of activation of the source/drain diffusion layer due to the tension of the Ru layer 103A itself. To prevent these phenomena, the gate electrode layer 103 for the PMOSFET is configured to have a two-layer structure in the first embodiment.</p>

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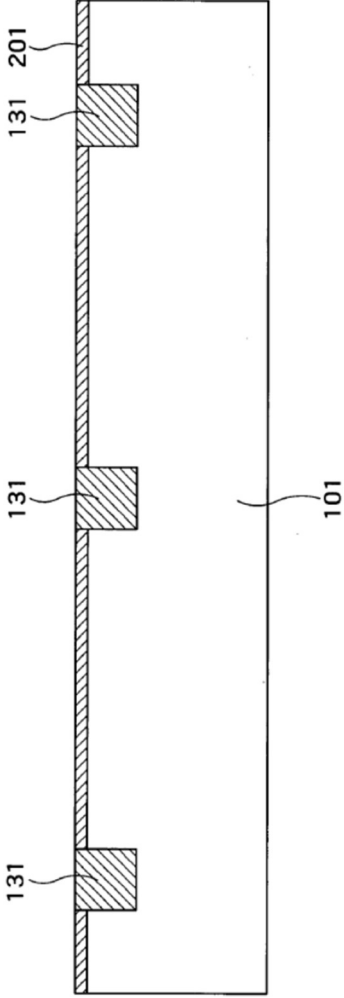
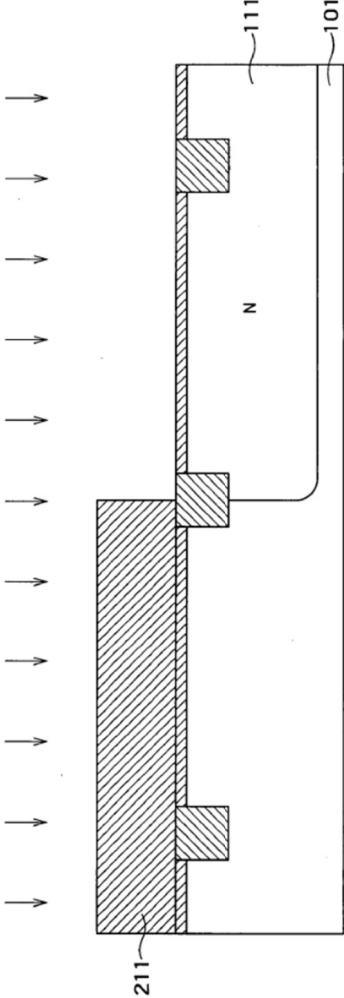
Claim		Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
Claim Language		a gate dielectric film 102 for the NMOSFET is formed in the NMOSFET region 106. Gate dielectric films 102 for the PMOSFET and the NMOSFET are formed from the gate dielectric film 102 common to the PMOSFET and the NMOSFET.
		<p style="text-align: center;">FIG. 2G</p> <p>[0072] The semiconductor device shown in FIG. 3 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer 103A which is made of conductive metal and a second conductive layer 103B which is made of</p>

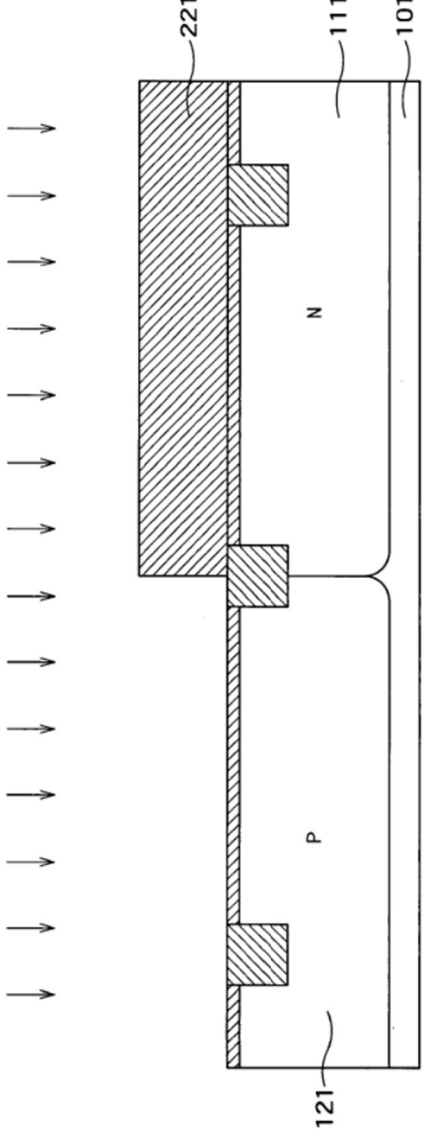
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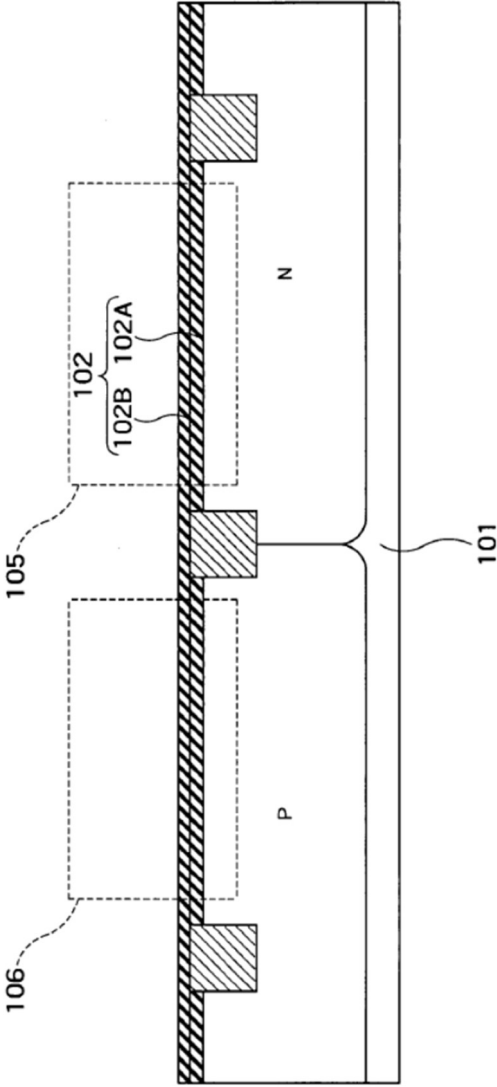
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p> <p>[0063] As described above, in the semiconductor device of the first embodiment, each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of the high-permittivity dielectric film, the gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of the conductive metal, and the gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of the conductive metal. Accordingly, in the first embodiment, it is possible to thin the gate dielectric films while suppressing an increase in leakage current, and to suppress a shift in the threshold voltage of the PMOSFET to increase the inversion capacitance of the PMOSFET.</p> <p>[0064] Moreover, in the first embodiment, since the source/drain diffusion layer 112 (and the extension diffusion layer 113) for the PMOSFET and the source/drain diffusion layer 122 (and extension diffusion layer 123) for the NMOSFET are formed after formation of the gate dielectric films 102, it is possible to improve the quality of the high-permittivity dielectric films to suppress a leakage current in them. This is because performing the process of improving the quality of the high-permittivity dielectric films before the formation of the source/drain diffusion layers (and extension diffusion layers) makes it possible, to perform the process of improving the quality of the high-permittivity dielectric films without concern about adverse effects on the source/drain diffusion layers (and extension diffusion layers).</p> <p>[0066] Therefore, in the first embodiment, gate dielectric films with preferable characteristics such as a preferable film quality, and gate electrodes with preferable characteristics such as a preferable work function, can be used as gate dielectric films and gate electrodes constituting a PMOSFET and an NMOSFET. Accordingly, in the first embodiment, it is possible to manufacture a semiconductor device including a high-performance CMOSFET.</p> <p>[0069] Although, in this embodiment, a hafnium silicon oxynitride film is adopted as a high-permittivity dielectric film to form each gate dielectric film 102, any other high-permittivity</p>

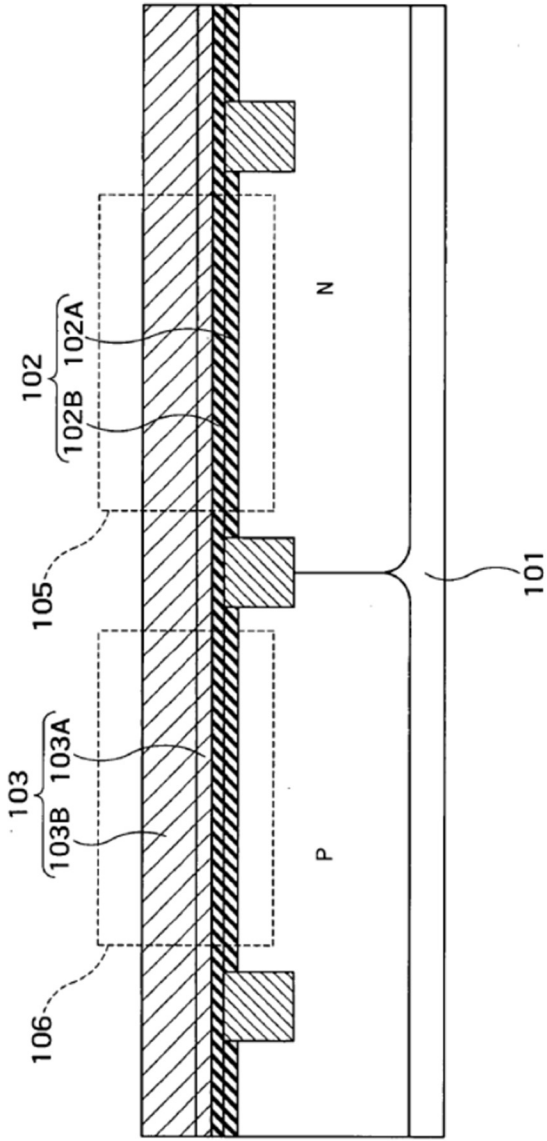
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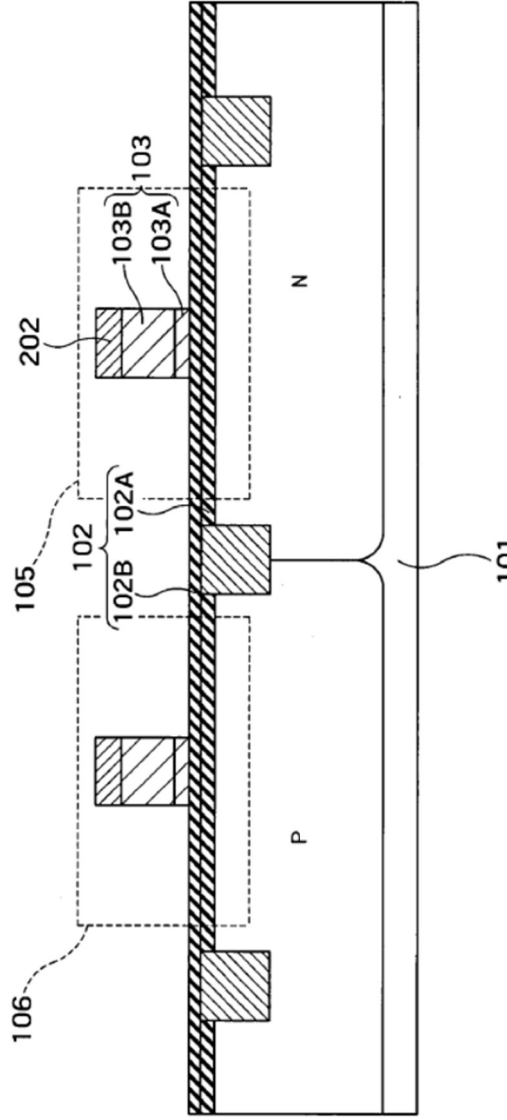
Claim	Claim Language	<p>Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama</p> <p>dielectric film may be adopted. Although, in this embodiment, the Ru layer and W layer are adopted as metal electrode layers to form the gate electrode 103 for the PMOSFET, any other metal electrode layers may be adopted. For example, a W layer, Ru layer, or Pt layer may be adopted as a metal electrode layer to form the gate electrode 103 for the PMOSFET. Although, in this embodiment, a TaSiN layer, HfN layer, and WSi layer are described as examples of metal electrode layers to form the gate electrode 104 for the NMOSFET, any other metal electrode layers may be adopted. It is possible to adopt, for example, a TaSi layer, TaSiN layer, TaC layer, TaCN layer, HfN layer, HfSi layer, HfSiN layer, WSi layer, TaHf layer, or TaHfN layer as a metal electrode layer to form the gate electrode 104 for the NMOSFET.</p>
Claim	Claim Language	<p style="text-align: center;">FIG. 3</p> <p>[0077] First, as shown in FIG. 4A, silicon oxide films are buried in predetermined regions of a silicon substrate 101 to form isolation layers 131 of STIs. Then, as shown in FIG. 4A, a silicon oxide film (dielectric film) 201 is formed on the silicon substrate 101.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<div></div> <p>FIG. 4A</p> <p>[0078] Next, as shown in FIG. 4B, ions of P (phosphorus) are implanted into the substrate 101 using a resist 211 as a mask.</p> <div></div> <p>FIG. 4B</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>[0079] Next, as shown in FIG. 4C, ions of B (boron) are implanted into the substrate 101 using a resist 221 as a mask. After that, the substrate 101 is subjected to thermal diffusion processing, thereby completing a well diffusion layer 111 for the PMOSFET and a well diffusion layer 121 for the NMOSFET.</p>  <p style="text-align: center;">FIG. 4C</p> <p>[0080] Next, as shown in FIG. 4D, the dielectric film 201 is removed from the substrate 101 using an ammonia fluoride aqueous solution, and the surface of the substrate 101 is cleaned using 0.5 to 5.0% hydrofluoric acid. Then, as shown in FIG. 4D, a silicon oxide film (a first dielectric film of a gate dielectric film) 102A with a thickness of 0.5 to 0.8 nm is formed on the substrate 101 in an atmosphere containing oxygen, and a hafnium silicate film (a second dielectric film of the gate dielectric film) 102B with a thickness of about 2.0 nm is formed on the silicon oxide film 102A using tetrakis(diethylamino)hafnium, tetrakis(dimethylamino)silicon, and oxygen. After that, the substrate 101 is subjected to annealing at 600° C., thereby densifying the silicon oxide film 102A and hafnium silicate film 102B. After that, the substrate 101 is processed in a nitrogen plasma atmosphere or ammonia atmosphere and then subjected to annealing at 1,000° C., thereby reforming the hafnium silicate film 102B into a hafnium silicon oxynitride film 102B. With the above-described</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>manufacturing steps, the gate dielectric film 102 common to the PMOSFET and NMOSFET is formed, ranging from a PMOSFET region 105 to a NMOSFET region 106, on the substrate 101. The PMOSFET region 105 is a region where the PMOSFET is to be formed, which is a specific example of a P-type FET region, and the NMOSFET region 106 is a region where the NMOSFET is to be formed, which is a specific example of an N-type FET region.</p>  <p style="text-align: center;">FIG. 4D</p> <p>[0081] Note that although the gate dielectric film 102 of the second embodiment has a two-layer structure of the silicon oxide film 102A and hafnium silicon oxynitride film 102B, it may have a one-layer structure of only a hafnium silicon oxynitride film or a laminated structure of three or more layers including a hafnium silicon oxynitride film.</p> <p>[0082] Next, as shown in FIG. 4E, a W (tungsten) layer (a first conductive layer of a gate electrode for the PMOSFET) 103A with a thickness of about 20 nm is deposited on the hafnium silicon oxynitride film 102B by thermal CVD using tungsten hexacarbonyl or plasma CVD using tungsten hexacarbonyl and hydrogen, and a TiN (titanium nitride) layer (a second conductive layer of the gate</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>electrode for the PMOSFET) 103B with a thickness of about 60 nm is deposited on the W layer 103A using titanium tetrachloride and ammonia. With the above-described manufacturing steps, the gate electrode layer 103 for the PMOSFET is formed, ranging from the PMOSFET region 105 to the NMOSFET region 106, on the gate dielectric film 102.</p>  <p>FIG. 4E</p> <p>[0083] Note that although the gate electrode layer 103 for the PMOSFET of the second embodiment has a two-layer structure of the W layer 103A and TiN layer 103B, it may have a one-layer structure of only a W layer or a laminated structure of three or more layers including a W layer. If the gate electrode layer 103 for the PMOSFET has a one-layer structure of only a W layer, it is desirable to reduce the thickness of the W layer to 60 nm or less because the W layer is likely to peel off.</p> <p>[0084] Next, as shown in FIG. 4F, the W layer 103A and TiN layer 103B are processed using a dielectric film 202 as a hard mask, the dielectric film 202 including a silicon oxide film or silicon nitride film. With the above-described manufacturing step, in the PMOSFET region 105 and the</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>NMOSFET region 106, a gate electrode 103 for the PMOSFET is formed in the PMOSFET region 105, and a dummy gate electrode (a gate electrode used as a dummy) 103 with the same configuration as that of the gate electrode 103 for the PMOSFET is formed in the NMOSFET region 106.</p>  <p style="text-align: center;">FIG. 4F</p> <p>[0085] Next, as shown in FIG. 4G, the silicon oxide film 102A and hafnium silicon oxynitride film 102B are processed using the dielectric film 202 as a hard mask. With the above-described manufacturing steps, in the PMOSFET region 105 and the NMOSFET region 106, a gate dielectric film 102 for the PMOSFET is formed in the PMOSFET region 105, and a gate dielectric film 102 for the NMOSFET is formed in the NMOSFET region 106. Gate dielectric films 102 for the PMOSFET and the NMOSFET are formed from the gate dielectric film 102 common to the PMOSFET and the NMOSFET.</p>

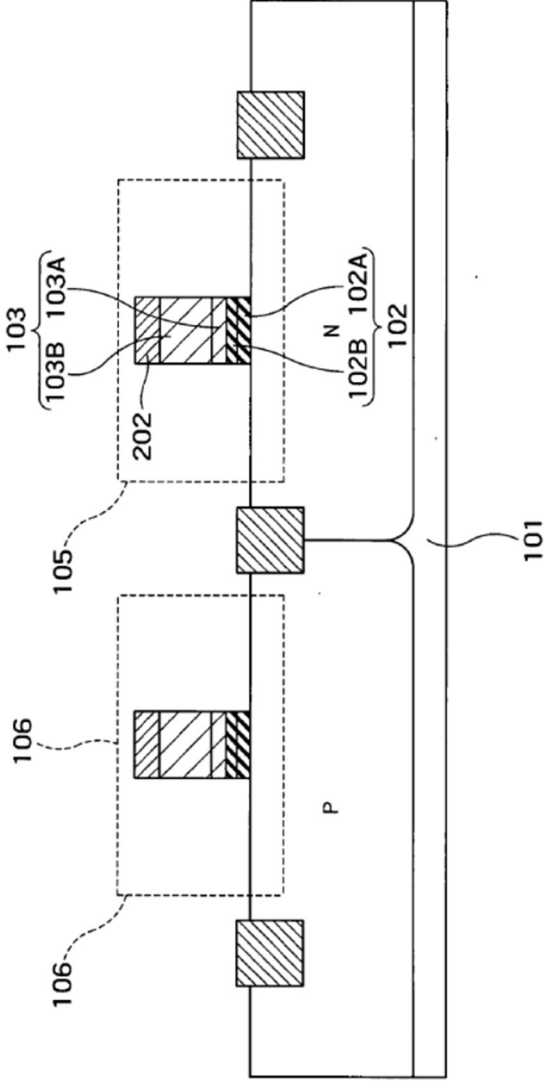
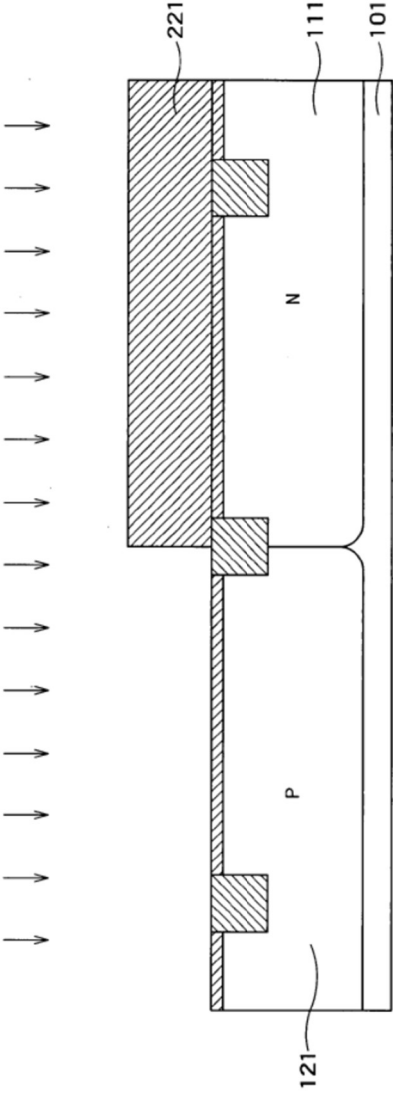
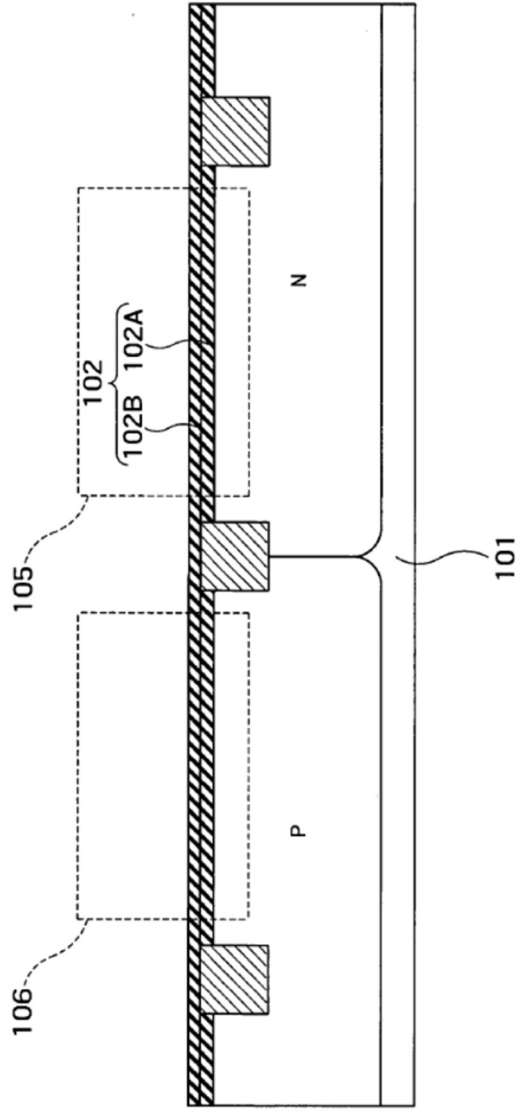
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<div data-bbox="272 401 812 1476">  </div> <div data-bbox="846 863 883 1016"> <p>FIG. 4G</p> </div> <div data-bbox="932 191 1404 1501"> <p>[0098] The semiconductor device shown in FIG. 5 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the NMOSFET in this embodiment includes three electrode-constituting layers: a first conductive layer 103A which is made of conductive metal, a second conductive layer 103B which is made of semiconductor, and a semiconductor layer 103C which is made of semiconductor. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of</p> </div>

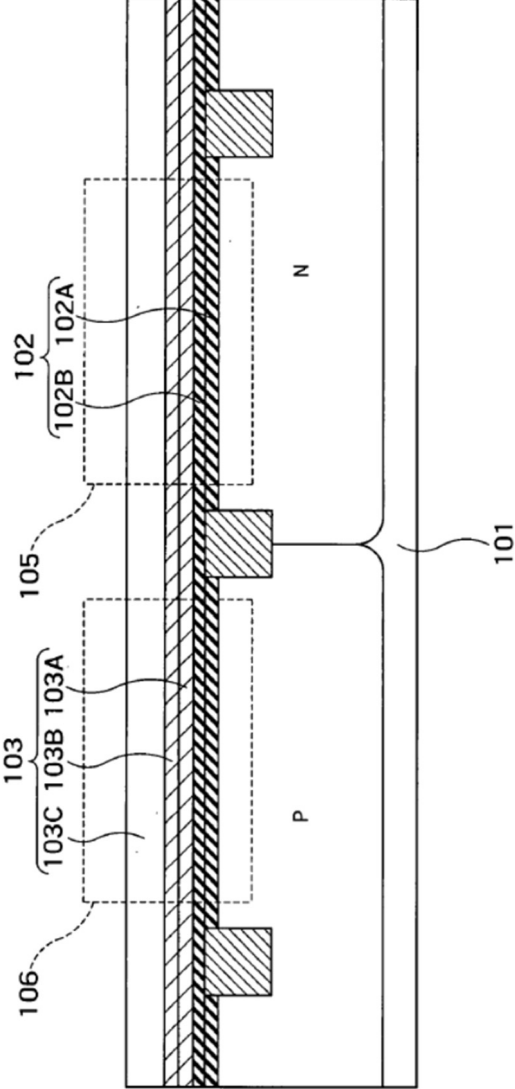
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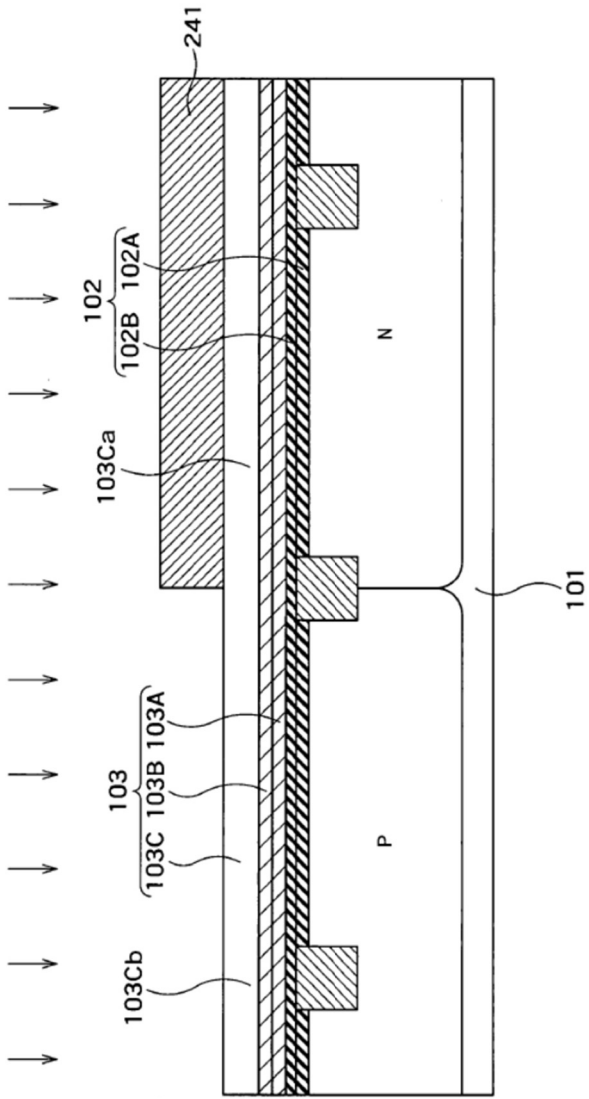
Claim	Claim Language	<p>Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama</p> <p>conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p>

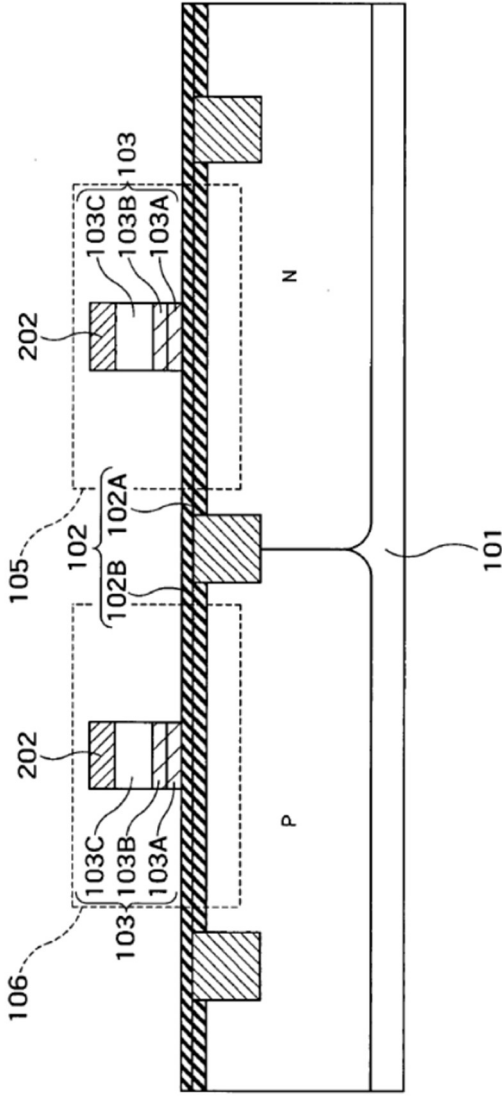
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<div data-bbox="277 459 634 1486"> </div> <div data-bbox="678 900 716 1050"> <p>FIG. 6A</p> </div> <div data-bbox="751 216 821 1501"> <p>[0104] Next, as shown in FIG. 6B, ions of P (phosphorus) are implanted into the substrate 101 using a resist 211 as a mask.</p> </div> <div data-bbox="873 382 1252 1486"> </div> <div data-bbox="1321 865 1359 1005"> <p>FIG. 6B</p> </div>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<p>[0105] Next, as shown in FIG. 6C, ions of B (boron) are implanted into the substrate 101 using a resist 221 as a mask. After that, the substrate 101 is subjected to thermal diffusion processing, thereby completing a well diffusion layer 111 for the PMOSFET and a well diffusion layer 121 for the NMOSFET.</p>  <p style="text-align: center;">FIG. 6C</p> <p>[0106] Next, as shown in FIG. 6D, the dielectric film 201 is removed from the substrate 101 using an ammonium fluoride aqueous solution, and the surface of the substrate 101 is cleaned using 0.5 to 5.0% hydrofluoric acid. Then, as shown in FIG. 6D, a silicon oxide film (a first dielectric film of a gate dielectric film) 102A with a thickness of 0.5 to 0.8 nm is formed on the substrate 101 in an atmosphere containing oxygen, and a hafnium silicate film (a second dielectric film of the gate dielectric film) 102B with a thickness of about 2.0 nm is formed on the silicon oxide film 102A using tetrakis(diethylamino)hafnium, tetrakis(dimethylamino)silicon, and oxygen. After that, the substrate 101 is subjected to annealing at 600° C., thereby densifying the silicon oxide film 102A and hafnium silicate film 102B. After that, the substrate 101 is processed in a nitrogen plasma atmosphere or ammonia atmosphere and then subjected to annealing at 1,000° C., thereby reforming the hafnium silicate film 102B into a hafnium silicon oxynitride film 102B. With the above-described</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>manufacturing steps, the gate dielectric film 102 common to the PMOSFET and NMOSFET is formed, ranging from a PMOSFET region 105 to a NMOSFET region 106, on the substrate 101. The PMOSFET region 105 is a region where the PMOSFET is to be formed, which is a specific example of a P-type FET region, and the NMOSFET region 106 is a region where the NMOSFET is to be formed, which is a specific example of an N-type FET region.</p>  <p style="text-align: center;">FIG. 6D</p> <p>[0107] Next, as shown in FIG. 6E, a W (tungsten) layer (a first conductive layer of a gate electrode for the PMOSFET) 103A with a thickness of about 20 nm is deposited on the hafnium silicon oxynitride film 102B by thermal CVD using tungsten hexacarbonyl or plasma CVD using tungsten hexacarbonyl and hydrogen, a TiN (titanium nitride) layer (a second conductive layer of the gate electrode for the PMOSFET) 103B with a thickness of about 60 nm is deposited on the W layer 103A using diethylaminotitanium and ammonia, and a semiconductor layer 103C made of polysilicon or amorphous silicon is deposited on the TiN (titanium nitride) layer 103B. With the above-described</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>manufacturing steps, the gate electrode 103 for the PMOSFET is formed, ranging from the PMOSFET region 105 to the NMOSFET region 106, on the gate dielectric film 102.</p>  <p style="text-align: center;">FIG. 6E</p> <p>[0108] Next, as shown in FIG. 6F, ions of P or As are implanted into the semiconductor layer 103C above the well diffusion layer 121 for the NMOSFET, using a resist 241 above the well diffusion layer 111 for the PMOSFET as a mask. After that, the substrate 101 is subjected to thermal diffusion processing, thereby completing an N-type diffusion layer inside the semiconductor layer 103C. The inside of a part of the semiconductor layer 103C above the well diffusion layer 111 for the PMOSFET becomes a non-diffusion layer 103Ca, and the inside of a part of the semiconductor layer 103C above the well diffusion layer 121 for the NMOSFET becomes a diffusion layer 103Cb.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="886 894 927 1041">FIG. 6F</p> <p data-bbox="976 189 1227 1501">[0109] Next, as shown in FIG. 6G, the W layer 103A, TiN layer 103B, and semiconductor layer 103C (non-diffusion layer 103Ca and diffusion layer 103Cb) are processed using a dielectric film 202 as a hard mask, the dielectric film 202 including a silicon oxide film or silicon nitride film. With the above-described manufacturing steps, in the PMOSFET region 105 and the NMOSFET region 106, a gate electrode 103 for the PMOSFET is formed in the PMOSFET region 105, and a dummy gate electrode (a gate electrode used as a dummy) 103 with the same configuration as that of the gate electrode 103 for the PMOSFET is formed in the NMOSFET region 106.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		 <p style="text-align: center;">FIG. 6G</p> <p>[0110] Next, as shown in FIG. 6H, the silicon oxide film 102A and hafnium silicon oxynitride film 102B are processed using the dielectric film 202 as a hard mask. With the above-described manufacturing steps, in the PMOSFET region 105 and the NMOSFET region 106, a gate dielectric film 102 for the PMOSFET is formed in the PMOSFET region 105, and a gate dielectric film 102 for the PMOSFET and the NMOSFET are formed from the gate dielectric film 102 common to the PMOSFET and the NMOSFET.</p>

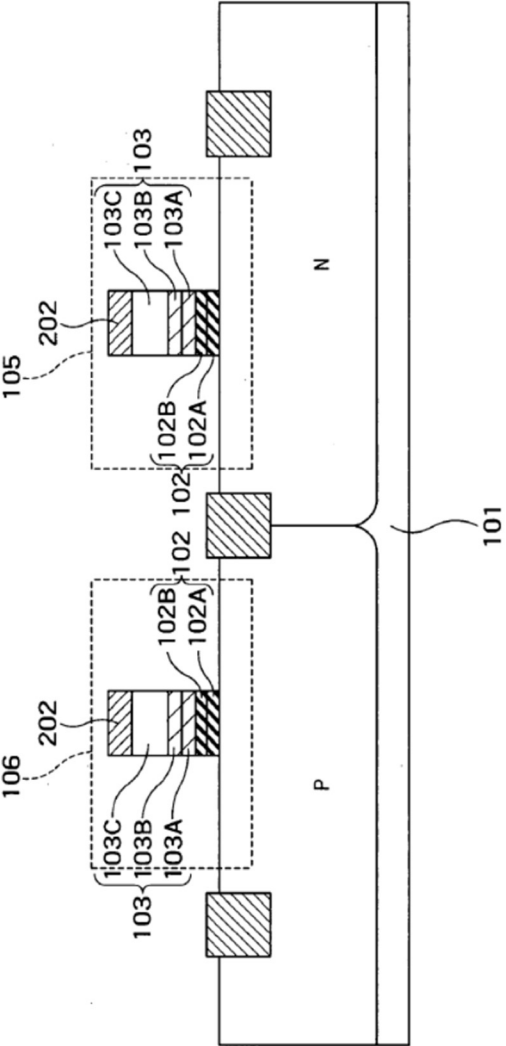
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p style="text-align: center;">FIG. 6H</p> <p>The description and annotation below are an example of a second gate insulating film formed on a second active region in the semiconductor substrate. For example, as can be seen in Figs. 1-2N, Aoyama discloses gate dielectric film 102 for the P and NMOSFET comprises first dielectric film 102A, a silicon oxide film, and second dielectric film 102B, a hafnium silicon oxynitride film.</p>

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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>first gate electrode</p> <p>silicon nitride film</p> <p>first gate insulating film</p> <p>first MIS transistor</p> <p>first active region</p> <p>first sidewall spacers</p> <p>second gate insulating film</p> <p>second MIS transistor</p> <p>second active region</p> <p>FIG. 1</p>

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[illegible]

Claim	Claim Language	<p data-bbox="207 338 245 1360">Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama</p> <div data-bbox="277 390 802 1493"> <p data-bbox="277 863 302 1136">first gate electrode</p> <p data-bbox="277 863 302 1052">silicon nitride film</p> <p data-bbox="367 1220 391 1482">first gate insulating film</p> <p data-bbox="431 1440 456 1493">first</p> <p data-bbox="464 1398 513 1493">sidewall spacers</p> <p data-bbox="537 1146 561 1304">first active region</p> <p data-bbox="570 1104 594 1304">first MIS transistor</p> <p data-bbox="618 1062 643 1220">second active region</p> <p data-bbox="643 1062 667 1220">second MIS transistor</p> <p data-bbox="675 705 699 863">second gate insulating film</p> </div> <p data-bbox="821 873 854 978">FIG. 3</p>
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Claim		Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
Claim Language		<p>As yet another example, as can be seen in Figs. 5-6N, Aoyama discloses gate dielectric film 102 for the NMOSFET comprises first dielectric film 102A, a silicon oxide film, and second dielectric film 102B, a hafnium silicon oxynitride film.</p>

As yet another example, as can be seen in Figs. 5-6N, Aoyama discloses gate dielectric film 102 for the NMOSFET comprises first dielectric film 102A, a silicon oxide film, and second dielectric film 102B, a hafnium silicon oxynitride film.

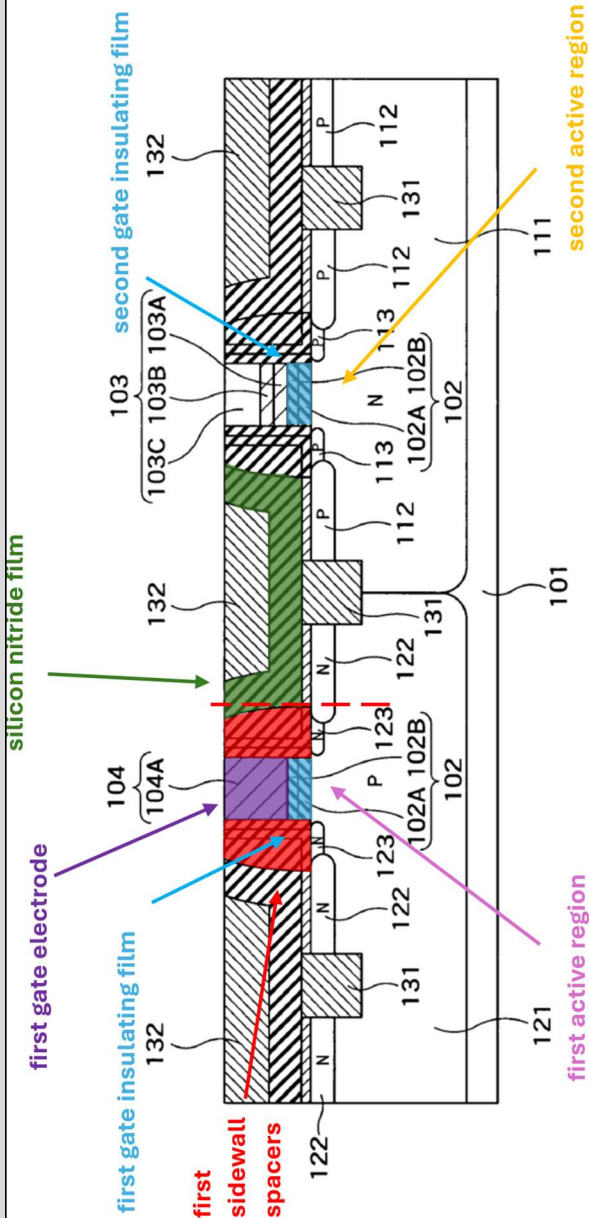
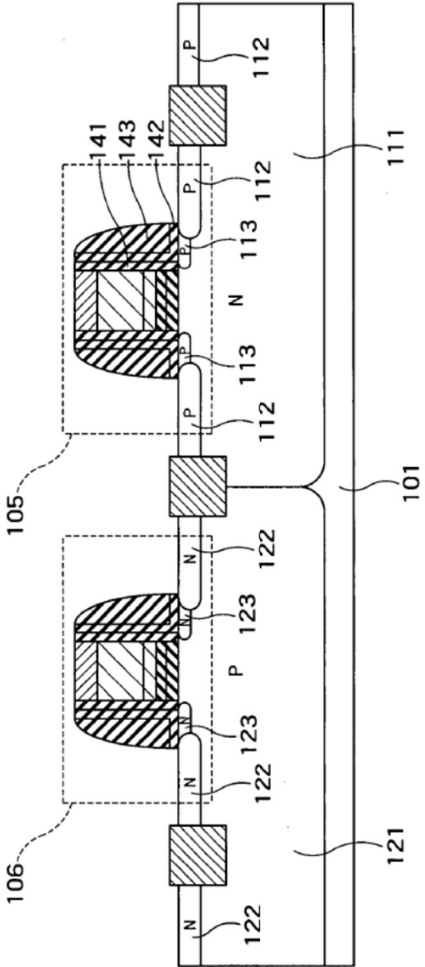
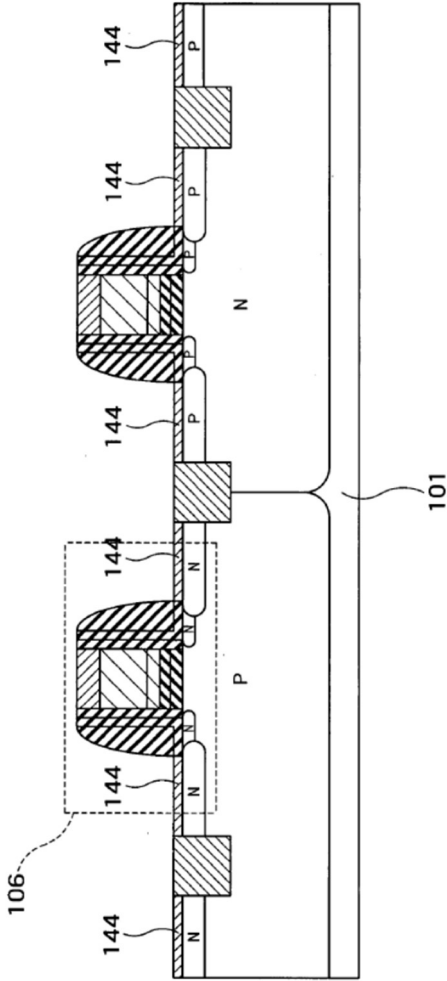
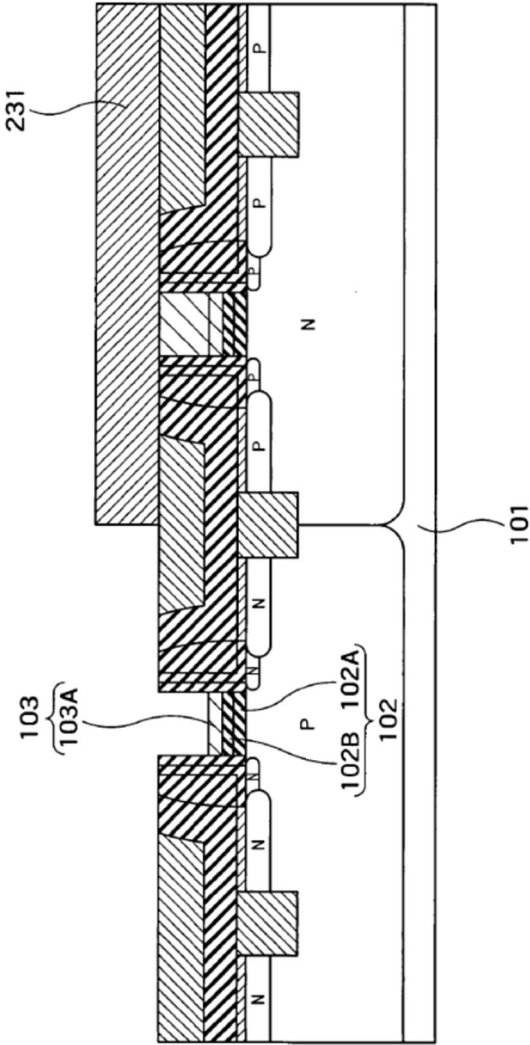
Claim	Claim Language	<p data-bbox="207 338 245 1360">Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama</p>  <p data-bbox="256 793 280 1014">silicon nitride film</p> <p data-bbox="277 1102 302 1333">first gate electrode</p> <p data-bbox="365 1186 389 1478">first gate insulating film</p> <p data-bbox="440 1375 464 1478">first sidewall spacers</p> <p data-bbox="885 1066 909 1291">first MIS transistor</p> <p data-bbox="885 436 909 695">second MIS transistor</p> <p data-bbox="812 1134 836 1344">first active region</p> <p data-bbox="812 268 836 520">second active region</p>
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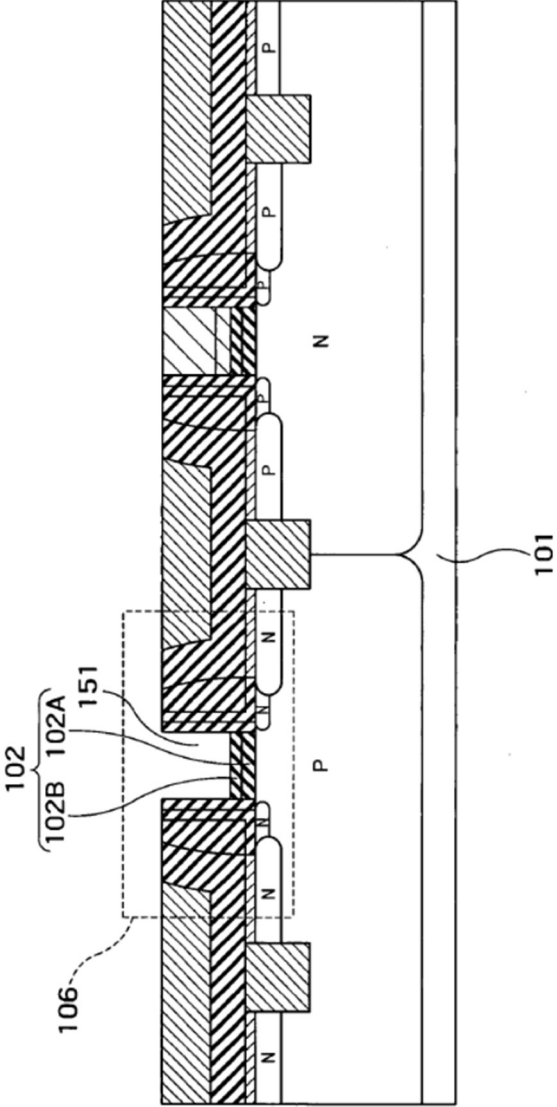
FIG. 5

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<p>the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer 103A which is made of conductive metal and a second conductive layer 103B which is made of conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p> <p>FIG. 1</p> <p>[0053] Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 2H. Also, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as</p>

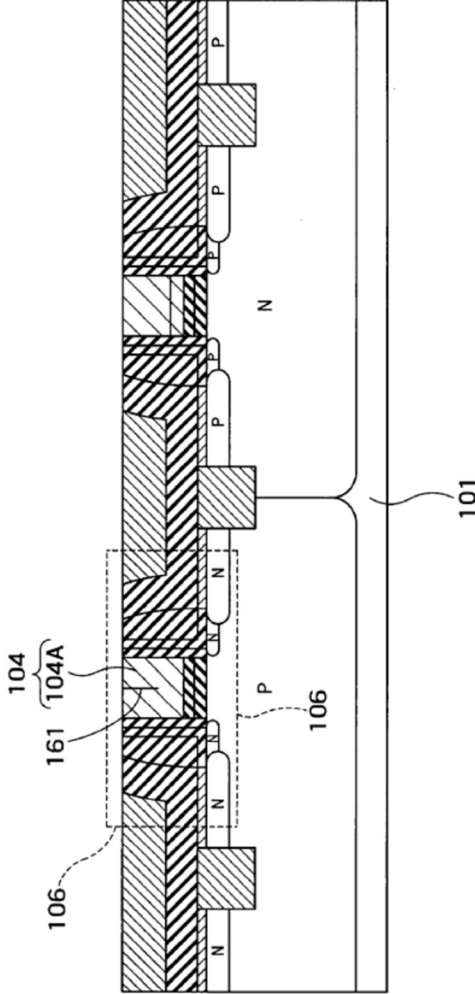
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>shown in FIG. 2H. In some cases, halo implantation is further performed to suppress short channel effects. Then, side wall spacers 143, each of which is made of a silicon nitride film, are formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.</p>  <p>FIG. 2H</p> <p>[0054] Note that although each side wall spacer of the first embodiment has a two-layer structure of the first side wall spacer 142 made of the silicon oxide film and the second side wall spacer 143 made of the silicon nitride film, it may have a one-layer structure, for example, of only a silicon nitride film or a laminated structure of three or more layers including, for example, a silicon oxide film and silicon nitride film.</p> <p>[0055] Next, as shown in FIG. 2I, silicide films 144 are formed in a self-aligned manner on the surfaces of the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<p>layer 122 for the NMOSFET. Although NiSi films are adopted as the silicide films 144 in this embodiment, PtSi films, ErSi films, NiPtSi films, NiErSi films, or the like may be adopted as the silicide films 144 instead.</p>  <p style="text-align: center;">FIG. 2I</p> <p>[0056] Next, as shown in FIG. 2J, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 2J, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 2J, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the W layers 103B are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p style="text-align: center;">FIG. 2K</p> <p>[0058] Next, as shown in FIG. 2L, in the NMOSFET region 106, the Ru layer 103A on the gate dielectric film 102 for the NMOSFET is etched in an atmosphere containing oxygen radical. With the above-described manufacturing step, the hafnium silicon oxynitride film 102B in the NMOSFET region 106 is exposed. The resist 231 may be removed before or after the removal of the Ru layer 103A. Through the above-described manufacturing steps, in the NMOSFET region 106, the dummy gate electrode 103 on the gate dielectric film 102 is removed, thereby forming a trench 151 on the gate dielectric film 102.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p style="text-align: center;">FIG. 2L</p> <p>[0059] Next, as shown in FIG. 2M, conductive metal, which is a material for forming a third conductive layer 104A of the gate electrode 104 for the NMOSFET, is deposited over the entire surface by CVD. Examples of the conductive metal include TaSiN which is formed using pentakis(ethylmethylamino)tantalum, and ammonia, and ammoniac, HfN which is formed in an atmosphere containing tetrakis(ethylmethylamino)hafnium and ammonia, HfSi which is formed using tetrakis(ethylmethylamino)hafnium and tetrakis(ethylmethylamino)silicon, and WSi which is formed using tungsten hexafluoride and dichlorosilane.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<div data-bbox="272 409 841 1486"> <p>FIG. 2M</p> </div> <p>[0060] Note that although the gate electrode 104 for the NMOSFET of the first embodiment has a one-layer structure of only the conductive layer 104A made of the conductive metal, it may have a laminated structure of two or more layers including a conductive layer made of conductive metal.</p> <p>[0061] Next, as shown in FIG. 2N, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback). Through the above-described manufacturing steps, in the NMOSFET region 106, the material for forming the gate electrode is buried in the trench 151 on the gate dielectric film 102, thereby forming the gate electrode 104 for the NMOSFET with a different configuration from that of the gate electrode 103 for the PMOSFET. Since the gate electrode 104 for the NMOSFET (the third conductive layer 104A) is formed in the hole by CVD, a trace of a streaky</p>

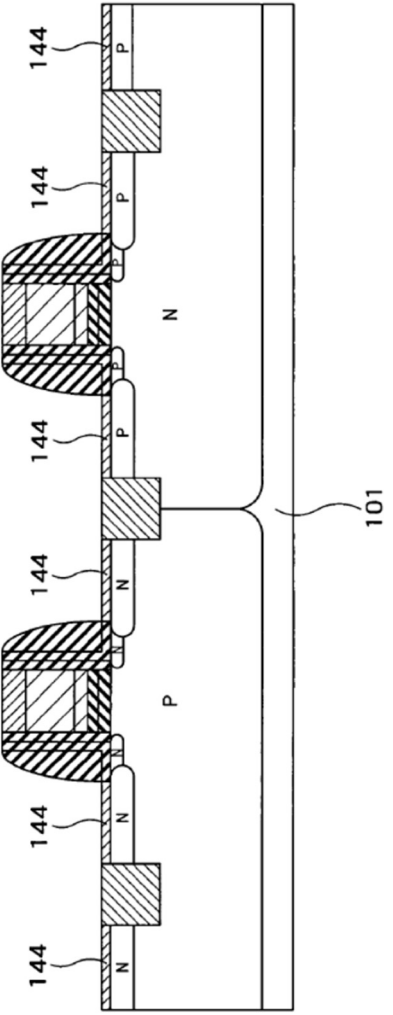
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>seam 161 which does not remain in the gate electrode 103 for the PMOSFET (the first conductive layer 103A and second conductive layer 103B) remains in the gate electrode 104 for the NMOSFET.</p>  <p style="text-align: center;">FIG. 2N</p> <p>[0065] Moreover, in the first embodiment, the gate electrode 104 for the NMOSFET is formed after the source/drain diffusion layer 112 (and extension diffusion layer 113) for the PMOSFET and the source/drain diffusion layer 122 (and extension diffusion layer 123) for the NMOSFET are formed. Accordingly, the possibility of change in the work function of the metal electrode of the NMOSFET in the step of forming the source/drain diffusion layers (and extension diffusion layers) is reduced.</p> <p>[0066] Therefore, in the first embodiment, gate dielectric films with preferable characteristics such as a preferable film quality, and gate electrodes with preferable characteristics such as a preferable work function, can be used as gate dielectric films and gate electrodes constituting a PMOSFET and an NMOSFET. Accordingly, in the first embodiment, it is possible to manufacture a semiconductor device including a high-performance CMOSFET.</p>

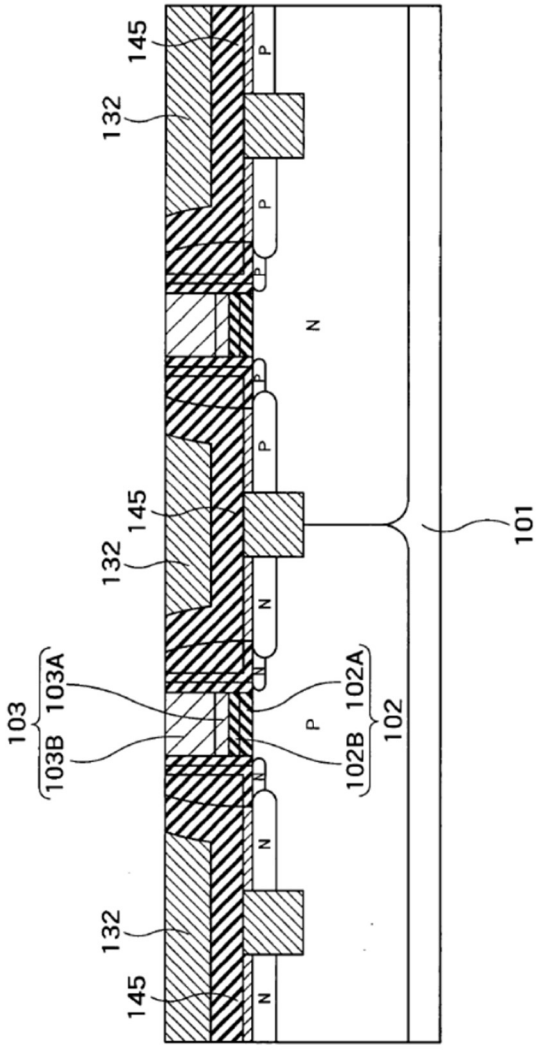
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>[0067] Additionally, in the first embodiment, the gate electrode 103 for the PMOSFET is formed by etching before formation of the inter layer dielectric film 132, and the gate electrode 104 for the NMOSFET is formed by the damascene process after formation of the inter layer dielectric film 132. Further, in the first embodiment, the gate electrode 103 for the PMOSFET formed in the NMOSFET region is used as a dummy electrode substituting for the gate electrode 104 for the NMOSFET. Therefore, in the first embodiment, the gate electrode 103 for the PMOSFET formed in the NMOSFET region is not wastefully removed in the etching step, and effectively used as the dummy electrode substituting for the gate electrode 104 for the NMOSFET until it is removed prior to the damascene process. Furthermore, in the first embodiment, since the step of forming the dummy electrode is integrated into the step of forming the gate electrode 103 for the PMOSFET, the number of steps required for the formation of the dummy electrode can be saved.</p> <p>[0068] In the damascene gate process explained as a background art, a dummy gate dielectric film (silicon oxide) is damaged in removing a dummy gate electrode (polysilicon), so it is necessary to remove also the dummy gate dielectric film in removing the dummy gate electrode. However, in the first embodiment, the dummy electrode in contact with the gate dielectric film 102 (second dielectric film 102B) made of the high-permittivity dielectric film, is the gate electrode 103 for the PMOSFET (first conductive layer 103A) made of the conductive metal. Particularly, in the first embodiment, the conductive metal is Ru, which is conductive metal capable of being removed without a chemical solution. Accordingly, in the first embodiment, it is possible to avoid unnecessary damage to the gate dielectric film 102 and unnecessary removal of the gate dielectric film 102, in removing the dummy electrode.</p> <p>[0072] The semiconductor device shown in FIG. 3 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer</p>

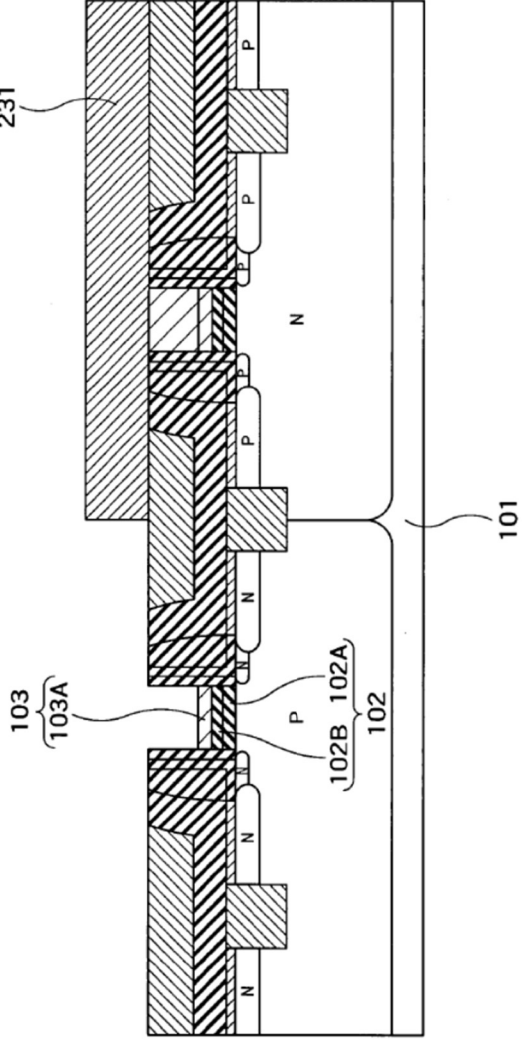
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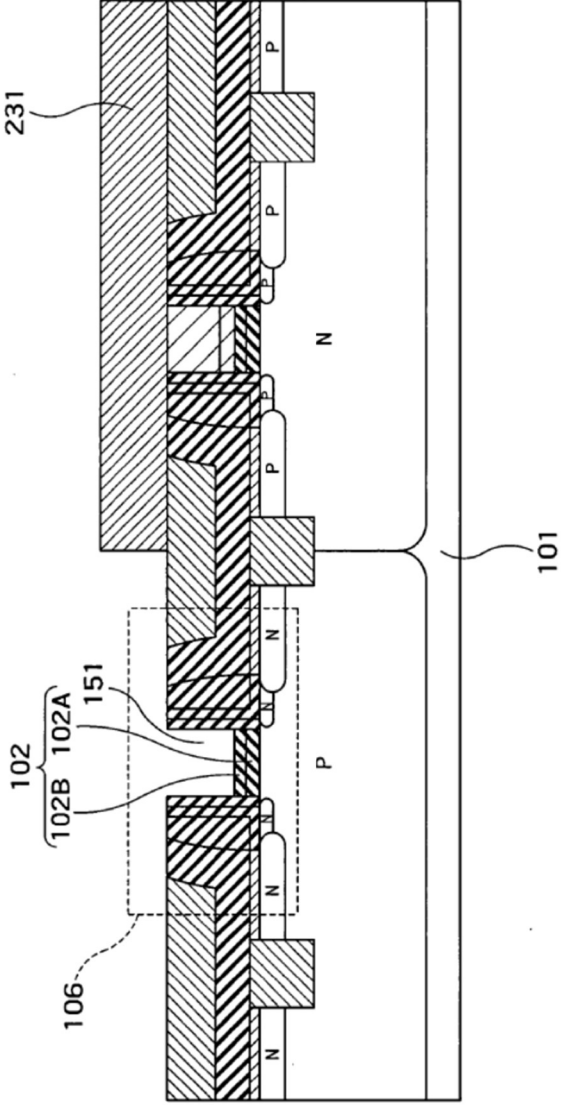
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>103A which is made of conductive metal and a second conductive layer 103B which is made of conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p> <p style="text-align: center;">FIG. 3</p> <p>[0086] Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 4H. Also, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 4H. Then, side wall spacers 143, each of which is made of a silicon nitride film, are</p>

Claim	Claim Language	<p data-bbox="207 338 245 1362">Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama</p> <p data-bbox="261 212 407 1503">formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.</p> <div data-bbox="435 464 862 1444"> </div> <p data-bbox="911 884 948 1024">FIG. 4H</p> <p data-bbox="980 264 1091 1503">[0087] Next, as shown in FIG. 4I, silicide films 144 are formed in a self-aligned manner on the surfaces of the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET.</p>
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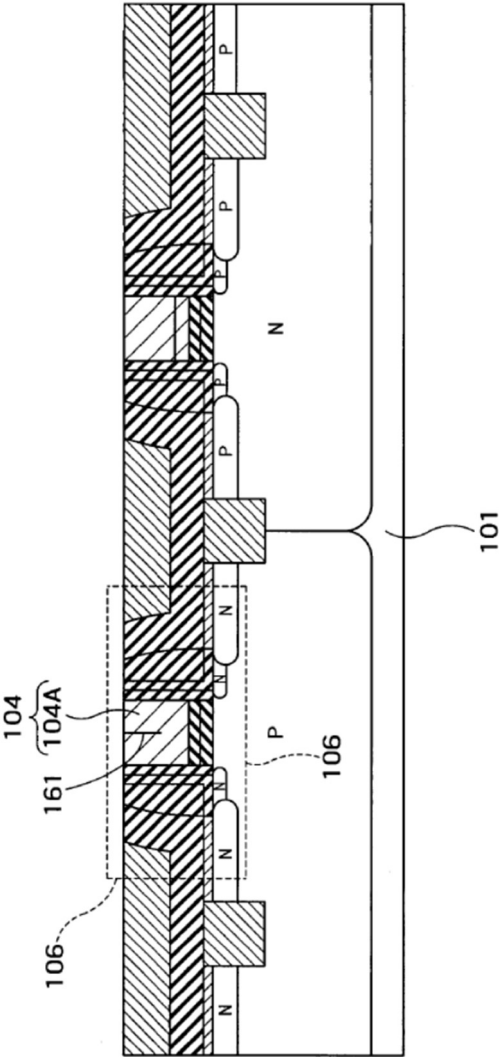
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p style="text-align: center;">FIG. 4I</p> <p>[0088] Next, as shown in FIG. 4J, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 4J, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 4J, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the TiN layers 103B are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>

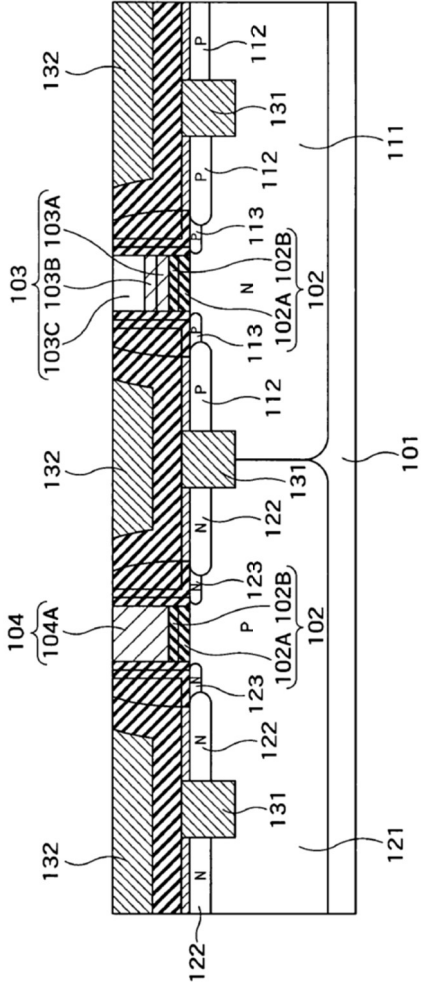
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		 <p data-bbox="828 903 868 1039">FIG. 4J</p> <p data-bbox="917 220 1063 1501">[0089] Next, as shown in FIG. 4K, in the NMOSFET region 106, the TiN layer 103B above the gate dielectric film 102 for the NMOSFET is etched using a resist 231 as a mask and using a chemical solution such as a solution containing hydrogen peroxide. With the above-described manufacturing step, the W layer 103A in the NMOSFET region 106 is exposed.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="828 882 868 1039">FIG. 4K</p> <p data-bbox="917 210 1161 1501">[0090] Next, as shown in FIG. 4L, in the NMOSFET region 106, the W layer 103A on the gate dielectric film 102 for the NMOSFET is etched using the resist 231 as a mask and using a chemical solution such as a solution containing hydrogen peroxide. With the above-described manufacturing step, the hafnium silicon oxynitride film 102B in the NMOSFET region 106 is exposed. Through the above-described manufacturing steps, in the NMOSFET region 106, the dummy gate electrode 103 on the gate dielectric film 102 is removed, thereby forming a trench 151 on the gate dielectric film 102.</p>

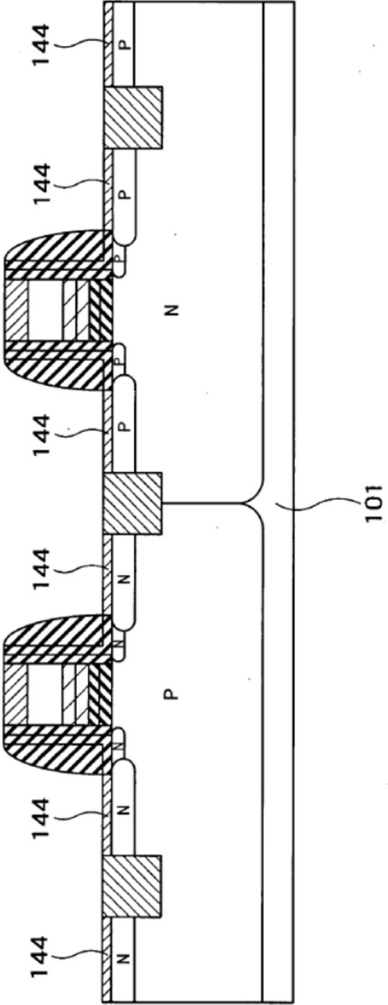
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<div><p>FIG. 4L</p><p>[0091] Next, as shown in FIG. 4M, conductive metal, which is a material for forming a third conductive layer 104A of the gate electrode 104 for the NMOSFET, is deposited over the entire surface by CVD. Examples of the conductive metal include TaC, which is formed using pentakis(dimethylamino)tantalum and methane.</p></div>

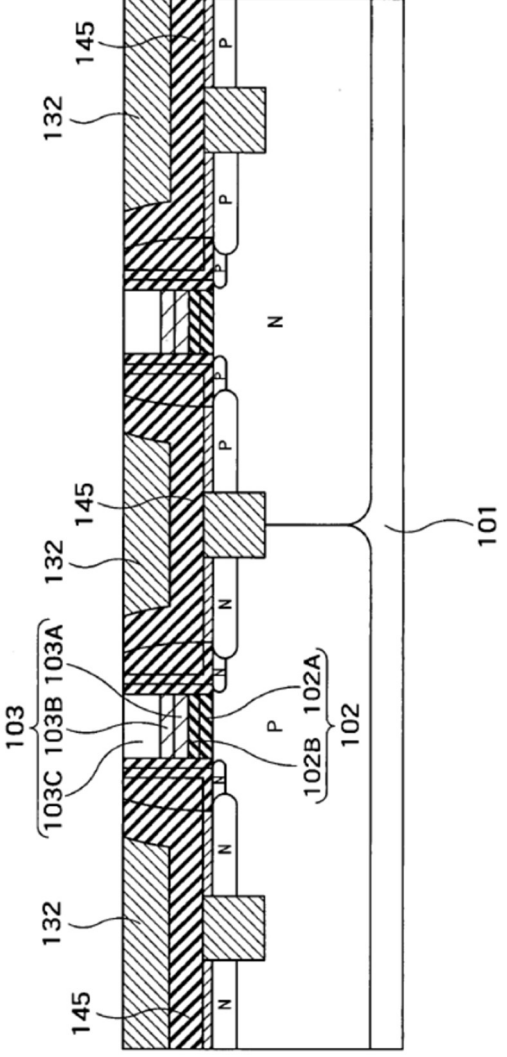
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<div data-bbox="272 384 857 1480"> </div> <div data-bbox="889 856 927 1010"> <p>FIG. 4M</p> </div> <div data-bbox="971 191 1393 1501"> <p>[0092] Note that although the gate electrode 104 for the NMOSFET of the second embodiment has a one-layer structure of only the conductive layer 104A made of the conductive metal, it may have a laminated structure of two or more layers including a conductive layer made of conductive metal.</p> <p>[0093] Next, as shown in FIG. 4N, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback). Through the above-described manufacturing steps, in the NMOSFET region 106, the material for forming the gate electrode is buried in the trench 151 on the gate dielectric film 102, thereby forming the gate electrode 104 for the NMOSFET with a different configuration from that of the gate electrode 103 for the PMOSFET. Since the gate electrode 104 for the NMOSFET (the third conductive layer 104A) is formed in the hole by CVD, a trace of a streaky seam 161 which does not remain in the gate electrode 103 for the PMOSFET (the first conductive layer 103A and second conductive layer 103B) remains in the gate electrode 104 for the NMOSFET.</p> </div>

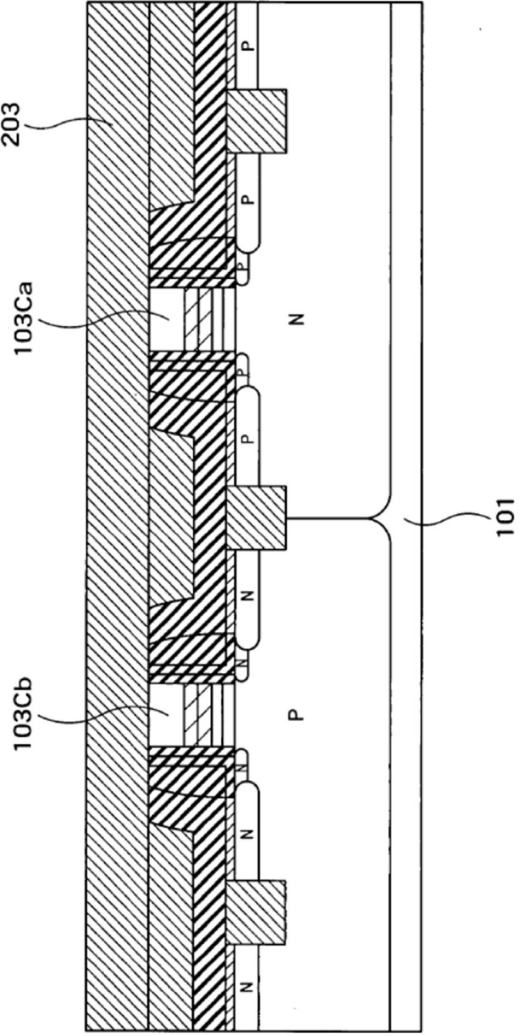
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		 <p data-bbox="795 871 836 1018">FIG. 4N</p> <p data-bbox="860 210 1015 1501">[0095] In the second embodiment, the dummy electrode (the gate electrode 103 for the PMOSFET) includes the W layer 103A and TiN layer 103B made of W and TiN respectively, which are conductive metals capable of being removed using a chemical solution. For this reason, in the second embodiment, it is possible to easily remove the dummy electrode at low cost.</p> <p data-bbox="1039 210 1404 1501">[0098] The semiconductor device shown in FIG. 5 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes three electrode-constituting layers: a first conductive</p>

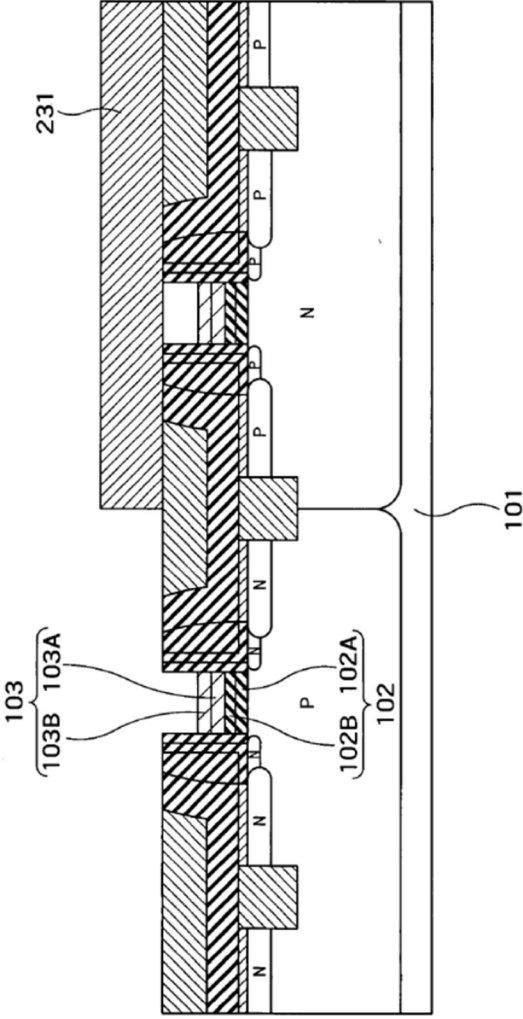
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<p>layer 103A which is made of conductive metal, a second conductive layer 103B which is made of conductive metal, and a semiconductor layer 103C which is made of semiconductor. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p>  <p>FIG. 5</p> <p>[0111] Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 6I. Also, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 6I. Then, side wall spacers 143, each of which is made of a silicon nitride film, are</p>

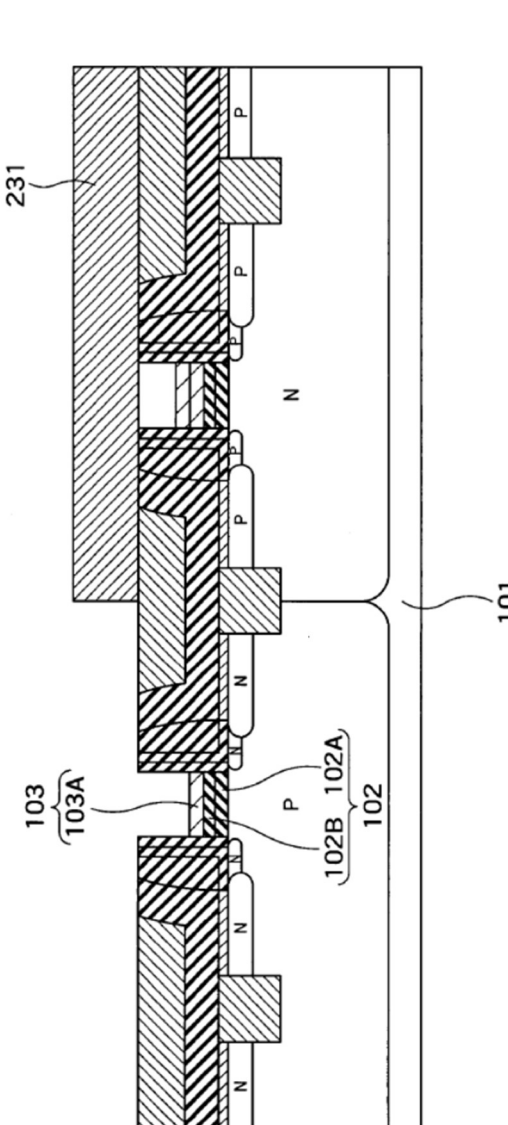
Claim	Claim Language	<p data-bbox="207 338 245 1362">Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama</p> <p data-bbox="261 210 407 1501">formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.</p> <div data-bbox="440 415 902 1465"> </div> <p data-bbox="954 884 992 1016">FIG. 6I</p> <p data-bbox="1036 264 1146 1501">[0112] Next, as shown in FIG. 6J, silicide films 144 are formed in a self-aligned manner on the surfaces of the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET.</p>
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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="714 919 755 1045">FIG. 6J</p> <p data-bbox="820 226 1071 1501">[0113] Next, as shown in FIG. 6K, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 6K, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 6K, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the semiconductor layers 103C (non-diffusion layers 103Ca and diffusion layers 103Cb) are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="787 903 836 1050">FIG. 6K</p> <p data-bbox="901 220 1128 1501">[0114] Next, as shown in FIG. 6L, a Ni (nickel) film (sacrificial film) 203 is formed over the entire surface. After that, the substrate 101 is subjected to annealing, thereby siliciding Ni in the Ni film 203. At this time, since the diffusion layer 103Cb contains P or As, the silicidation rate of the diffusion layer 103Cb becomes higher than that of the non-diffusion layer 103Ca. Accordingly, Ni monosilicide (NiSi) is formed in the non-diffusion layer 103Ca, and a Ni-rich silicide (Ni₂Si, Ni₃Si, or the like) is formed in the diffusion layer 103Cb.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="824 905 868 1052">FIG. 6L</p> <p data-bbox="938 205 1079 1501">[0115] Next, as shown in FIG. 6M, in the NMOSFET region 106, the semiconductor layer 103C above the gate dielectric film 102 for the NMOSFET is etched using a resist 231 as a mask and using a chemical solution such as a solution containing hydrogen peroxide. With the above-described manufacturing steps, the TiN layer 103B in the NMOSFET region 106 is exposed.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="824 888 862 1031">FIG. 6M</p> <p data-bbox="927 220 1073 1501">[0116] Next, as shown in FIG. 6N, in the NMOSFET region 106, the TiN layer 103B above the gate dielectric film 102 for the NMOSFET is etched using the resist 231 as a mask and using a chemical solution such as a solution containing hydrogen peroxide. With the above-described manufacturing step, the W layer 103A in the NMOSFET region 106 is exposed.</p>

Claim		Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
Claim Language		 <p style="text-align: center;">FIG. 6N</p> <p>[0117] Next, as shown in FIG. 6O, in the NMOSFET region 106, the W layer 103A on the gate dielectric film 102 for the NMOSFET is etched using the resist 231 as a mask and using a chemical solution such as a solution containing hydrogen peroxide. With the above-described manufacturing step, the hafnium silicon oxynitride film 102B in the NMOSFET region 106 is exposed. Through the above-described manufacturing steps, in the NMOSFET region 106, the dummy gate electrode 103 on the gate dielectric film 102 is removed, thereby forming a trench 151 on the gate dielectric film 102.</p>

Claim	Claim Language	<p>Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama</p>
		<p>FIG. 60</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<div data-bbox="269 449 812 1472"> </div> <p data-bbox="841 892 878 1037">FIG. 6P</p> <p data-bbox="927 191 1252 1499">[0119] Next, as shown in FIG. 6Q, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback). Through the above-described manufacturing steps, in the NMOSFET region 106, the material for forming the gate electrode is buried in the trench 151 on the gate dielectric film 102, thereby forming the gate electrode 104 for the NMOSFET with a different configuration from that of the gate electrode 103 for the PMOSFET. Since the gate electrode 104 for the NMOSFET (the third conductive layer 104A) is formed in the hole by CVD, a trace of a streaky seam 161 which does not remain in the gate electrode 103 for the PMOSFET (the first conductive layer 103A, second conductive layer 103B, and semiconductor layer 103C) remains in the gate electrode 104 for the NMOSFET.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<p>second gate electrode 104</p> <p>second gate insulating film 132</p> <p>silicon nitride film 102</p> <p>first gate electrode 103</p> <p>first gate insulating film 132</p> <p>first MIS transistor</p> <p>second MIS transistor</p> <p>second active region</p> <p>first active region</p>

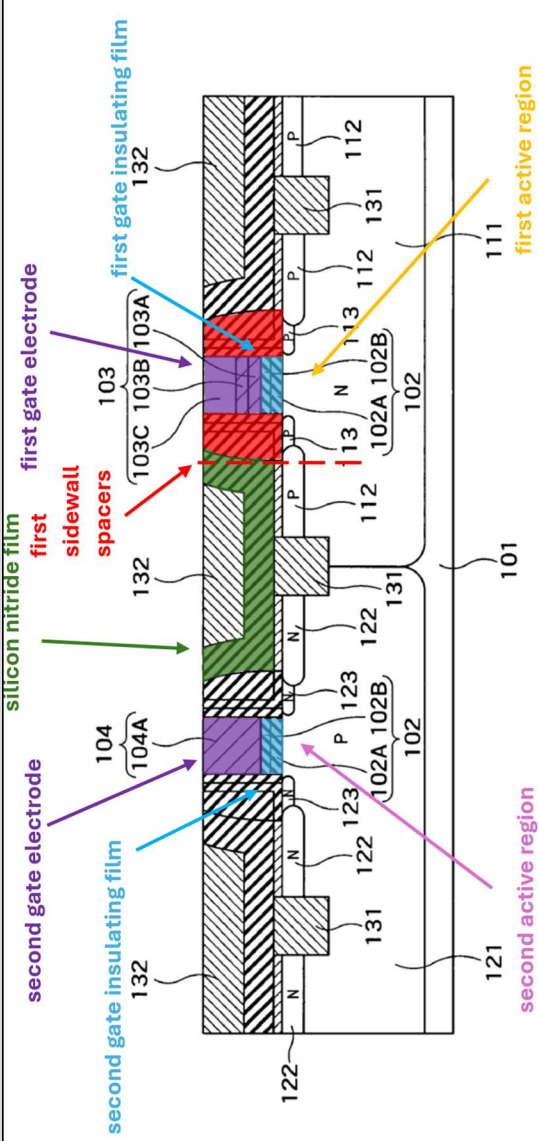
As another example, as can be seen in Figs. 3-4N, Aoyama discloses e.g., a gate electrode 103 for the PMOSFET includes a W (tungsten) layer 103A and a TiN (titanium nitride) layer 103B. The gate electrode is also disclosed as only a Ru layer. The gate electrode 103 is also disclosed as only a W layer. In this example, 103A is the first metal film and 103B is the conductive film.

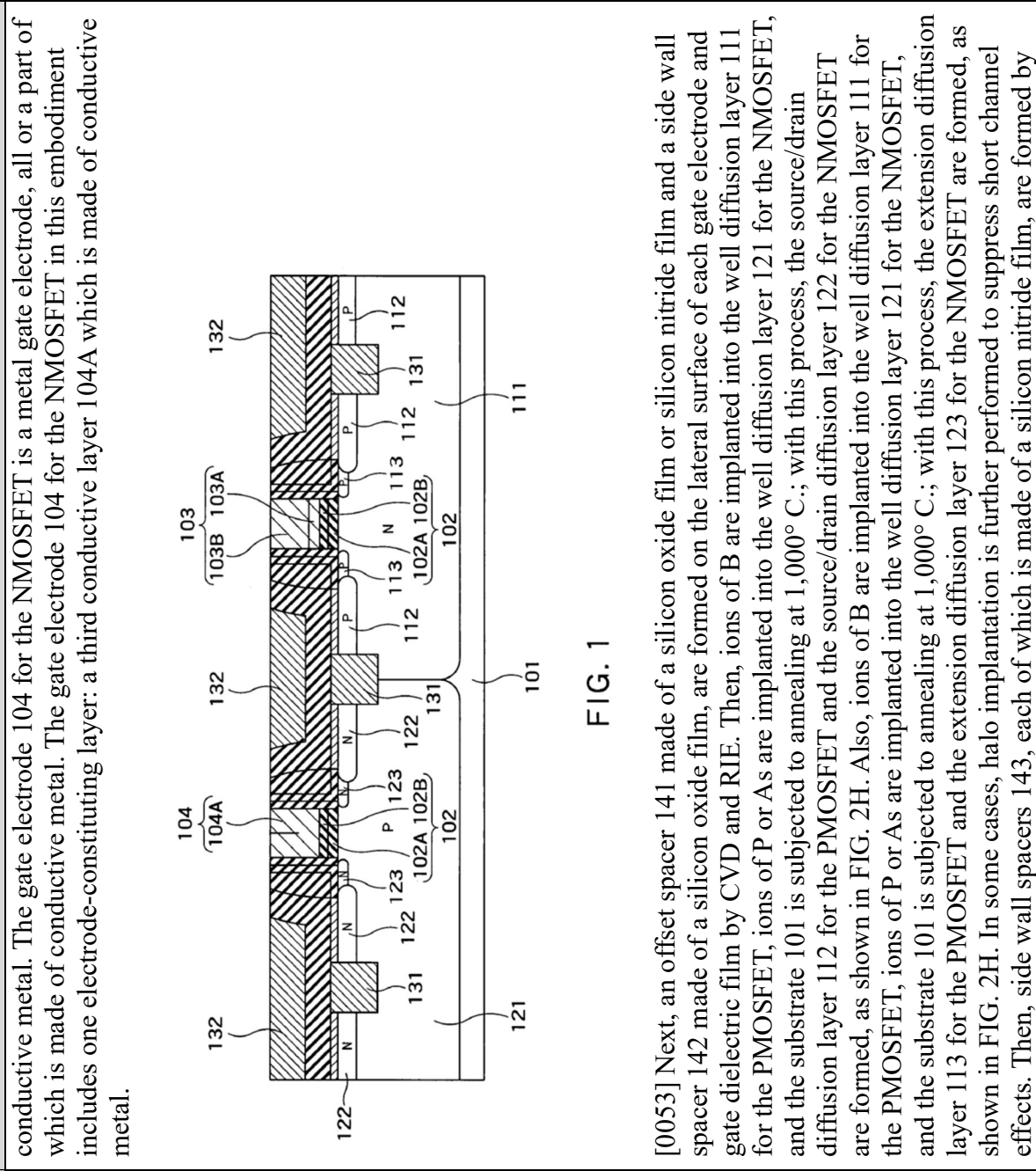
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>FIG. 3 first MIS transistor second MIS transistor</p> <p>Alternatively, as can be seen in Figs. 3-4N, Aoyama discloses a gate electrode 104 comprising conductive layer 104A, made of TaC. Alternatively, Aoyama discloses gate electrode 104 may be made of two or more layers including a conductive layer made of conductive metal. In this example, the first metal film and the conductive film are the two layers of 104A.</p>

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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>FIG. 3 first MIS transistor</p> <p>As yet another example, as can be seen in Figs. 5-6N, Aoyama discloses e.g., a gate electrode 103 for the PMOSFET includes a W (tungsten) layer 103A, a TiN (titanium nitride) layer 103B, and a polysilicon or silicide layer 103C. In this example, 103A is the first metal film and 103B is the conductive film.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<p>first gate electrode</p> <p>first gate insulating film</p> <p>silicon nitride film</p> <p>second gate electrode</p> <p>second gate insulating film</p> <p>first MIS transistor</p> <p>second MIS transistor</p> <p>first active region</p> <p>second active region</p> <p>FIG. 5</p> <p>Alternatively, as can be seen in Figs. 5-6N, Aoyama discloses a gate electrode 104 comprising conductive layer 104A, made of TaCN. A person of ordinary skill in the art would be motivated to modify 104A to include a conductive layer, similar to the first two embodiments.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
25 [d.3]	second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative; and	 <p>FIG. 5 first MIS transistor</p> <p>second MIS transistor</p> <p>second active region</p> <p>first active region</p> <p>second gate electrode</p> <p>second gate insulating film</p> <p>first gate electrode</p> <p>first gate insulating film</p> <p>sidewall spacers</p> <p>silicon nitride film</p>
25 [d.3]	second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative; and	<p>Aoyama, as evidenced by the example citations below, discloses second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative.</p> <p>[0039] The semiconductor device shown in FIG. 1 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer 103A which is made of conductive metal and a second conductive layer 103B which is made of</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<p>conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p>  <p>FIG. 1</p> <p>[0053] Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 2H. Also, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 2H. In some cases, halo implantation is further performed to suppress short channel effects. Then, side wall spacers 143, each of which is made of a silicon nitride film, are formed by</p>

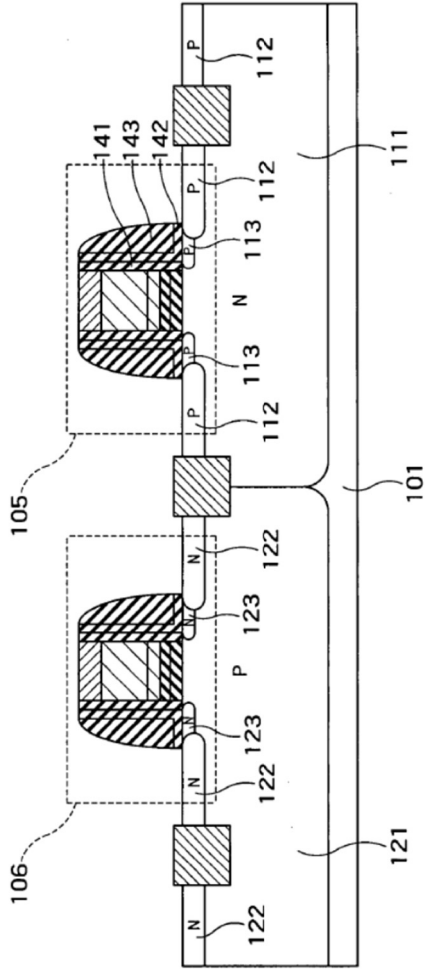
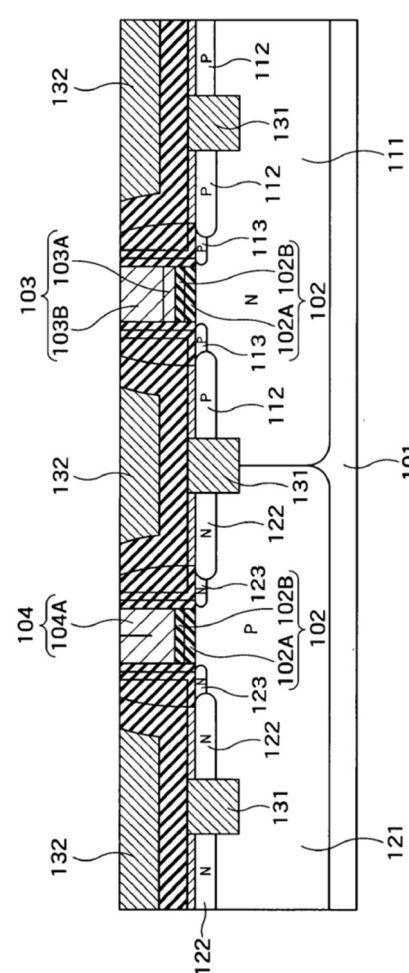
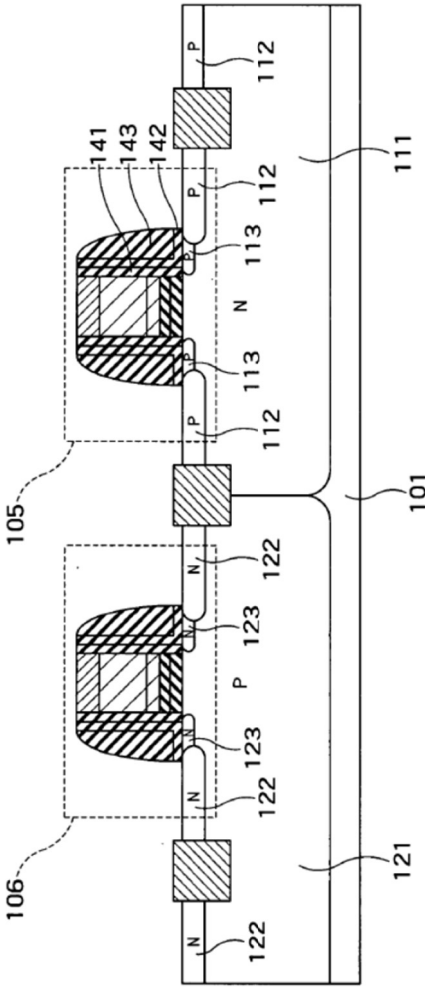
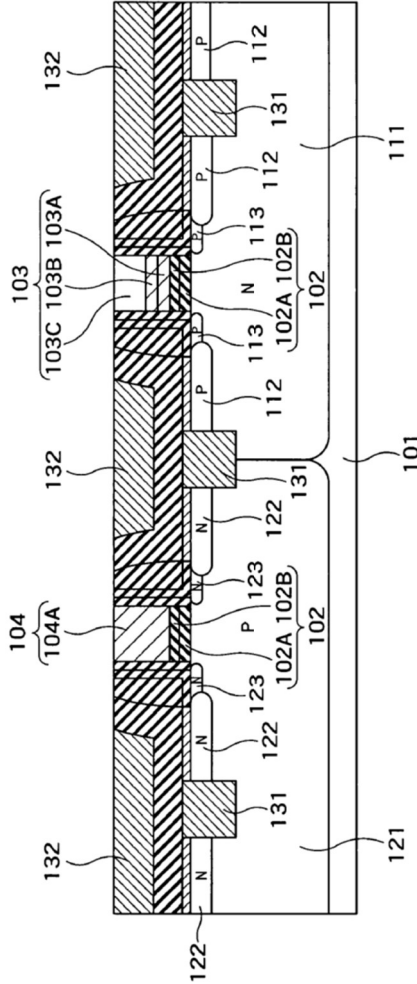
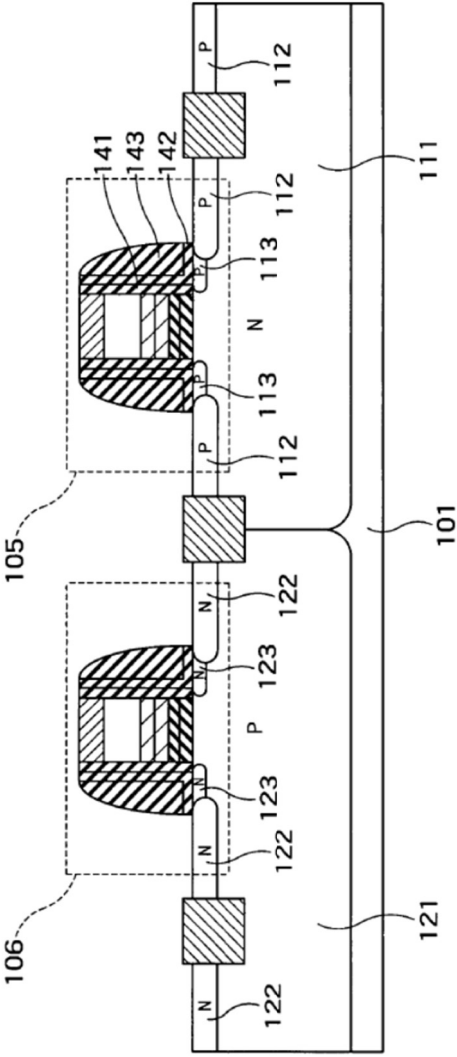
Claim	Claim Language	<p data-bbox="207 338 245 1365">Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama</p> <p data-bbox="264 191 407 1503">CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.</p> <div data-bbox="467 499 889 1461">  <p>The diagram shows a cross-section of a semiconductor device. A substrate 101 is at the base. On the left, region 106 (NMOSFET) has a gate electrode 102, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate</p> </div> <p data-bbox="938 915 976 1052">FIG. 2H</p> <p data-bbox="1036 218 1214 1503">[0054] Note that although each side wall spacer of the first embodiment has a two-layer structure of the first side wall spacer 142 made of the silicon oxide film and the second side wall spacer 143 made of the silicon nitride film, it may have a one-layer structure, for example, of only a silicon nitride film or a laminated structure of three or more layers including, for example, a silicon oxide film and silicon nitride film.</p> <p data-bbox="1252 191 1395 1503">[0072] The semiconductor device shown in FIG. 3 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate</p>
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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<p>dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer 103A which is made of conductive metal and a second conductive layer 103B which is made of conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p>  <p>FIG. 3</p> <p>[0086] Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET,</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 4H. Also, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 4H. Then, side wall spacers 143, each of which is made of a silicon nitride film, are formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.</p>  <p style="text-align: center;">FIG. 4H</p> <p>[0098] The semiconductor device shown in FIG. 5 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes three electrode-constituting layers: a first conductive layer 103A which is made of conductive metal, a second conductive layer 103B which is made of conductive metal, and a semiconductor layer 103C which is made of semiconductor. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p>  <p>FIG. 5</p> <p>[0111] Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>are formed, as shown in FIG. 6I. Also, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 6I. Then, side wall spacers 143, each of which is made of a silicon nitride film, are formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.</p>  <p>FIG. 6I</p> <p>The description and annotation below are an example of second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative. For example, as can be seen in Figs. 1-2N, Aoyama discloses second sidewall spacers, e.g., offset spacer 141, side wall spacer 142, and side wall spacer 143. Aoyama discloses the spacers may be made of either</p>

Claim	Claim Language	<p>Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama</p> <p>silicon oxide or silicon nitride. It also discloses the sidewall spacers could have a one-layer structure or three or more layers.</p> <p>FIG. 1 second MIS transistor</p>
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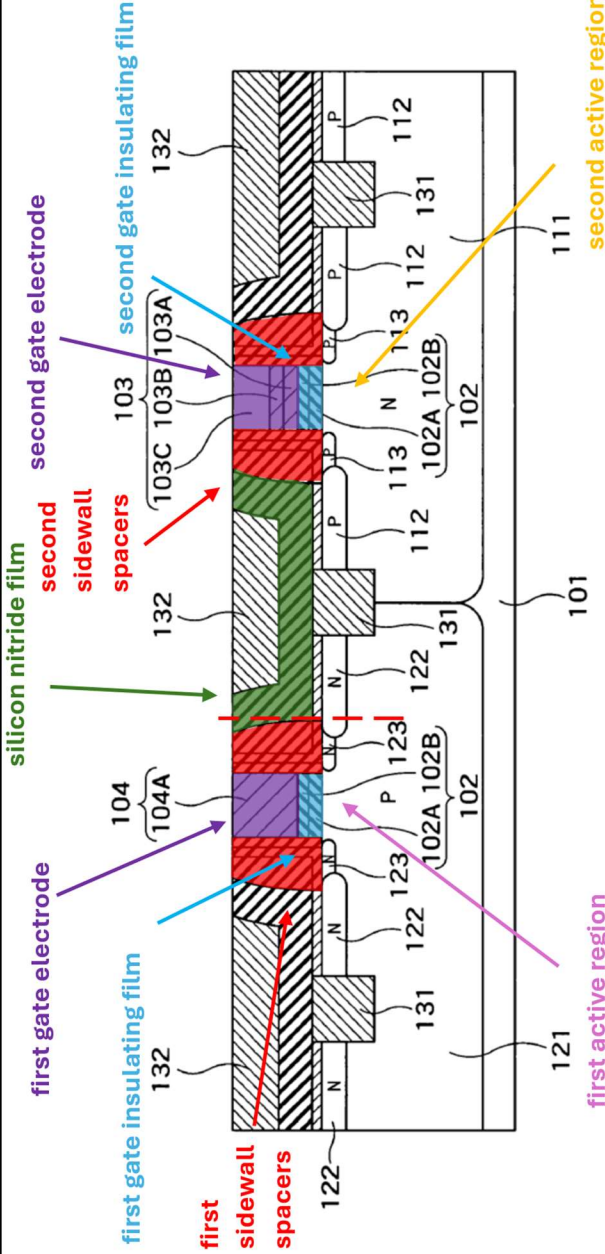
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>FIG. 1</p> <p>second gate electrode</p> <p>silicon nitride film</p> <p>first gate electrode</p> <p>second gate insulating film</p> <p>first gate insulating film</p> <p>second sidewall spacers</p> <p>first sidewall spacers</p> <p>second active region</p> <p>first active region</p> <p>second MIS transistor</p> <p>first MIS transistor</p> <p>As another example, as can be seen in Figs. 3-4N, Aoyama discloses second sidewall spacers, e.g., offset spacer 141, side wall spacer 142, and side wall spacer 143. Aoyama discloses the spacers may be made of either silicon oxide or silicon nitride.</p>

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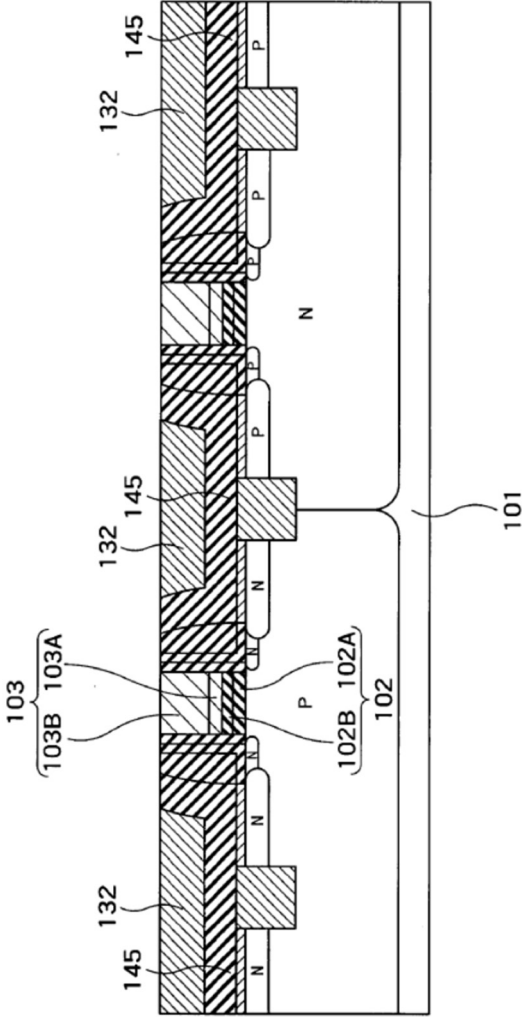
Claim		Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
Claim Language		

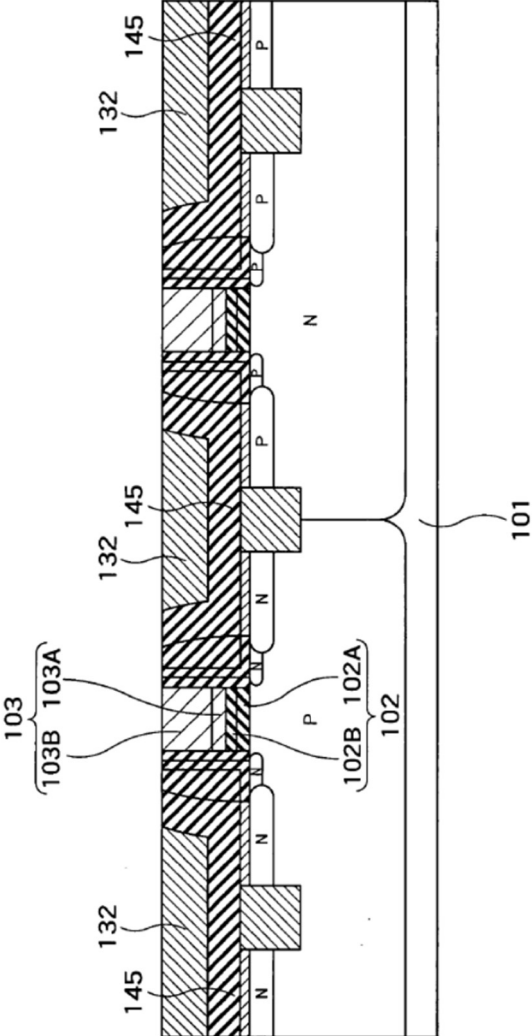
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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>second gate electrode silicon nitride film first gate electrode</p> <p>second gate insulating film first sidewall spacers first active region</p> <p>second sidewall spacers second active region first MIS transistor</p> <p>FIG. 3</p> <p>As yet another example, as can be seen in Figs. 5-6N, Aoyama discloses second sidewall spacers, e.g., offset spacer 141, side wall spacer 142, and side wall spacer 143. Aoyama discloses the spacers may be made of either silicon oxide or silicon nitride.</p>

Claim	Claim Language	<p data-bbox="207 338 245 1360">Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama</p>  <p data-bbox="285 1104 310 1339">first gate electrode</p> <p data-bbox="285 1192 310 1486">first gate insulating film</p> <p data-bbox="285 1440 310 1493">first</p> <p data-bbox="285 1381 310 1493">sidewall</p> <p data-bbox="285 1325 310 1493">spacers</p> <p data-bbox="261 789 285 1010">silicon nitride film</p> <p data-bbox="285 747 310 800">second</p> <p data-bbox="285 688 310 800">sidewall</p> <p data-bbox="285 632 310 800">spacers</p> <p data-bbox="285 443 310 716">second gate electrode</p> <p data-bbox="285 247 310 520">second gate insulating film</p> <p data-bbox="285 411 310 464">second</p> <p data-bbox="285 352 310 464">sidewall</p> <p data-bbox="285 296 310 464">spacers</p> <p data-bbox="285 247 310 300">first active region</p> <p data-bbox="285 411 310 684">second MIS transistor</p> <p data-bbox="285 247 310 520">second active region</p> <p data-bbox="902 789 927 905">FIG. 5</p>
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Claim		Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
Claim Language	<p>second gate electrode</p> <p>second gate insulating film</p> <p>second sidewall spacers</p> <p>silicon nitride film</p> <p>first gate electrode</p> <p>first gate insulating film</p> <p>first sidewall spacers</p> <p>second active region</p> <p>first active region</p> <p>FIG. 5</p> <p>second MIS transistor</p> <p>first MIS transistor</p>	

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
25 [d.4]	the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers,	<p>Aoyama, as evidenced by the example citations below, discloses the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers.</p> <p>[0056] Next, as shown in FIG. 2J, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 2J, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 2J, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the W layers 103B are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>  <p style="text-align: center;">FIG. 2J</p> <p>[0088] Next, as shown in FIG. 4J, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 4J, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 4J, the surface of the</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the TiN layers 103B are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>  <p>FIG. 4J</p> <p>[0113] Next, as shown in FIG. 6K, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 6K, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 6K, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the semiconductor layers 103C (non-diffusion layers 103Ca and diffusion layers 103Cb) are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>

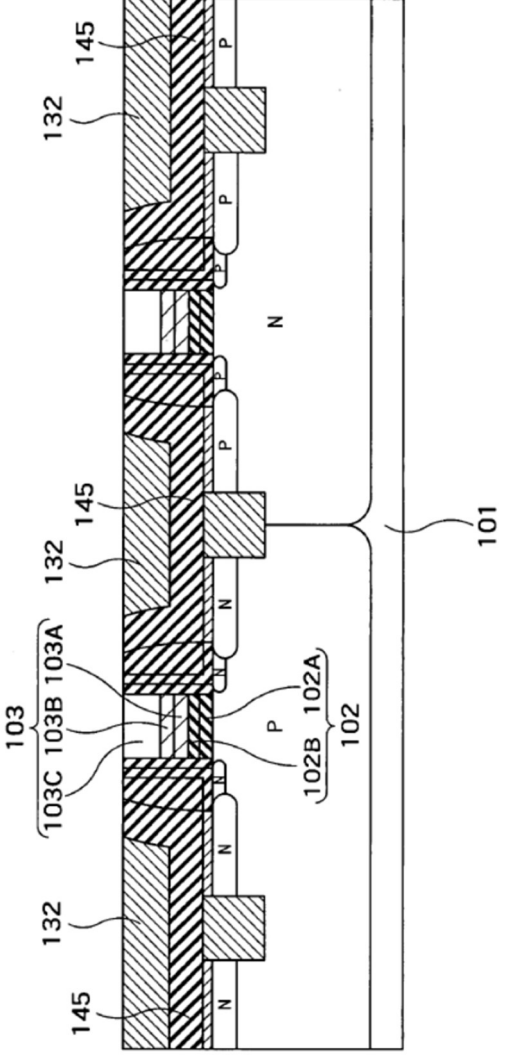
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p>The diagram shows a cross-section of a semiconductor device. A substrate 101 is at the base. A second gate electrode 102 is formed on the substrate, with regions 102A and 102B. Above the gate electrode, there are second sidewall spacers 145. The device includes regions 103, which are further divided into 103A, 103B, and 103C. Various dopants are indicated: 'N' for n-type and 'P' for p-type. A silicon nitride film 132 is formed over the side surfaces of the second gate electrode 102 and the second sidewall spacers 145. The diagram also shows a second active region 102B located laterally outside the second sidewall spacers 145.</p> <p style="text-align: center;">FIG. 6K</p> <p>The description and annotation below are an example of the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers. For example, as can be seen in Figs. 1-2N, Aoyama discloses etch stopper film 145 made of silicon nitride.</p>

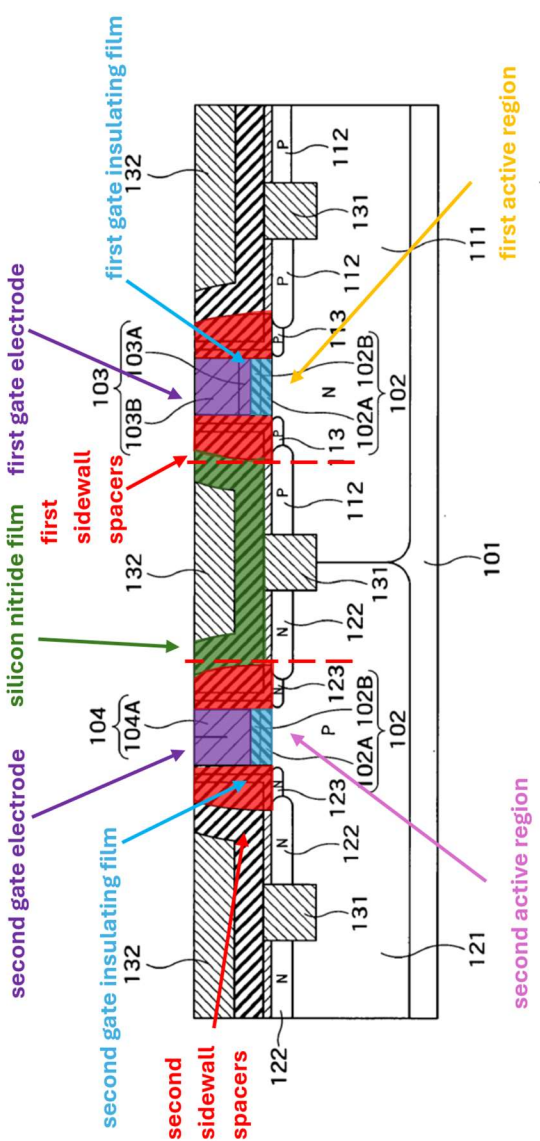
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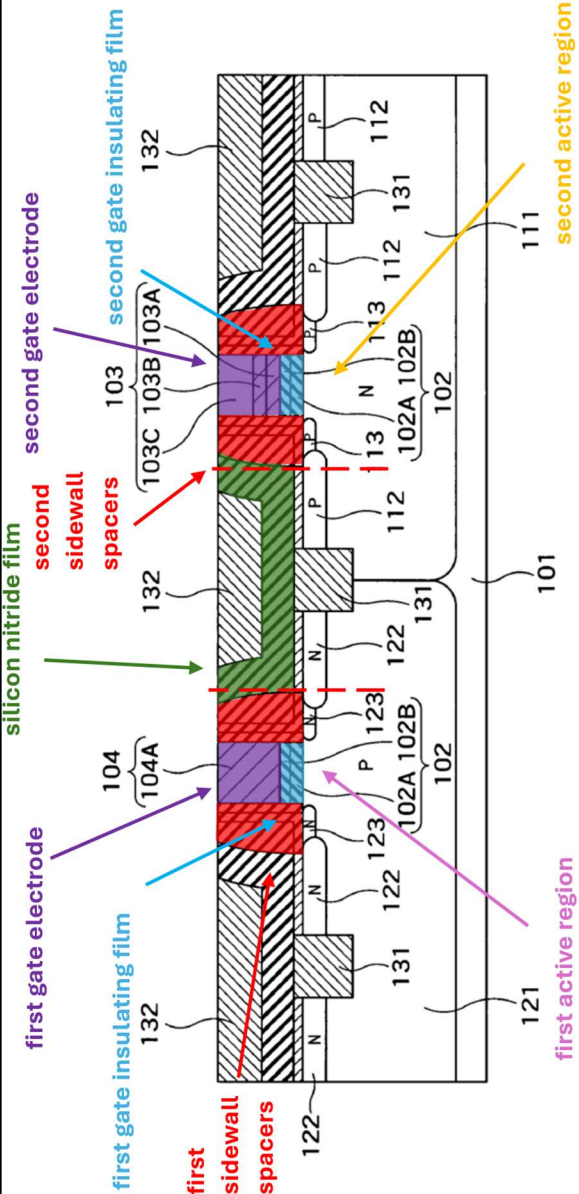
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<p>FIG. 1</p> <p>first MIS transistor</p> <p>second MIS transistor</p> <p>first active region</p> <p>second active region</p> <p>first gate electrode</p> <p>second gate electrode</p> <p>first gate insulating film</p> <p>second gate insulating film</p> <p>first sidewall spacers</p> <p>second sidewall spacers</p> <p>silicon nitride film</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<p>second gate electrode silicon nitride film first gate electrode</p> <p>second gate insulating film first sidewall spacers first gate insulating film</p> <p>second sidewall spacers first active region second active region</p> <p>second MIS transistor first MIS transistor</p> <p>FIG. 1</p> <p>As another example, as can be seen in Figs. 3-4N, Aoyama discloses etch stopper film 145 made of silicon nitride.</p>

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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>FIG. 3 second MIS transistor</p> <p>first MIS transistor</p> <p>first gate electrode silicon nitride film second gate electrode</p> <p>first gate insulating film second gate insulating film</p> <p>first sidewall spacers second sidewall spacers</p> <p>first active region second active region</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p>FIG. 3 first MIS transistor</p> <p>As yet another example, as can be seen in Figs. 5-6N, Aoyama discloses etch stopper film 145 made of silicon nitride.</p>

Claim	Claim Language	<p data-bbox="207 338 245 1360">Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama</p>  <p data-bbox="873 1066 906 1283">first MIS transistor</p> <p data-bbox="873 443 906 695">second MIS transistor</p>
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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
25 [e]	the first and second metal films are made of different metal materials,	<p>FIG. 5 first MIS transistor second MIS transistor</p> <p>Labels in diagram: second gate electrode, second gate insulating film, second sidewall spacers, silicon nitride film, first sidewall spacers, first gate electrode, first gate insulating film, first active region, second active region.</p>
		<p>Aoyama, as evidenced by the example citations below, discloses the first and second metal films are made of different metal materials.</p> <p>Among the three different embodiments, 103A and 104A are disclosed as being different metal materials. In Figs. 1-2N, 103A is a Ru layer and 104A is made of TaSiN, HfN, HfSi, or WSi. In Figs. 3-4N, 103A is a W (tungsten) layer and 104A is made of TaC. And in Figs. 5-6N, 103A is a W (tungsten) layer and 104A is made of TaCN.</p> <p>[0039] The semiconductor device shown in FIG. 1 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of</p>

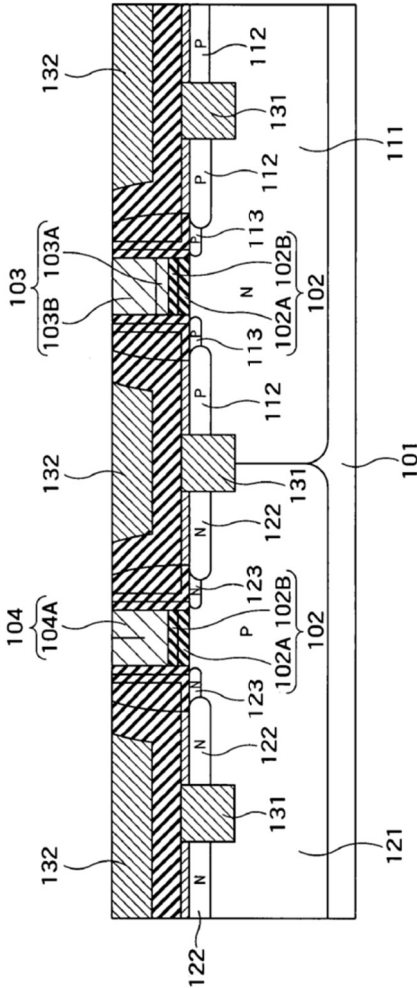
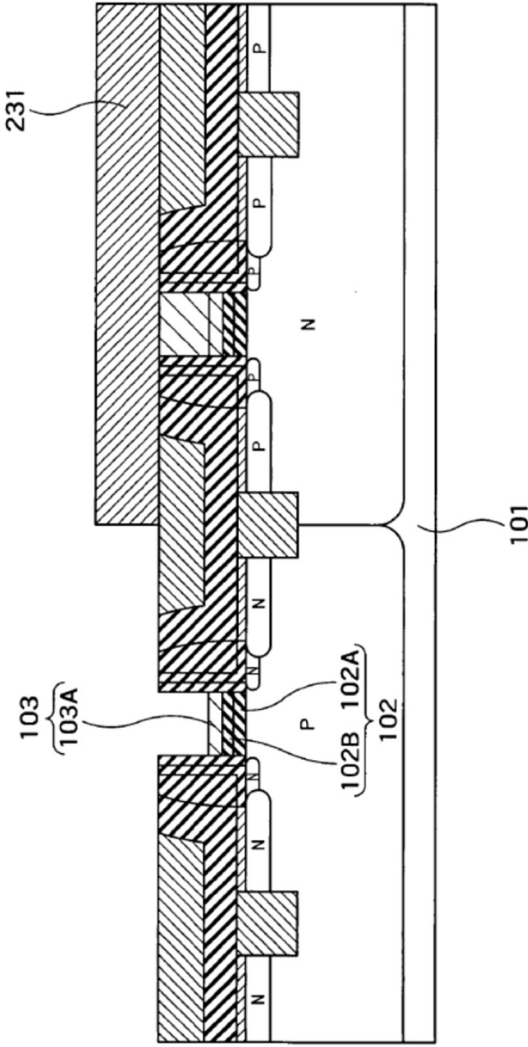
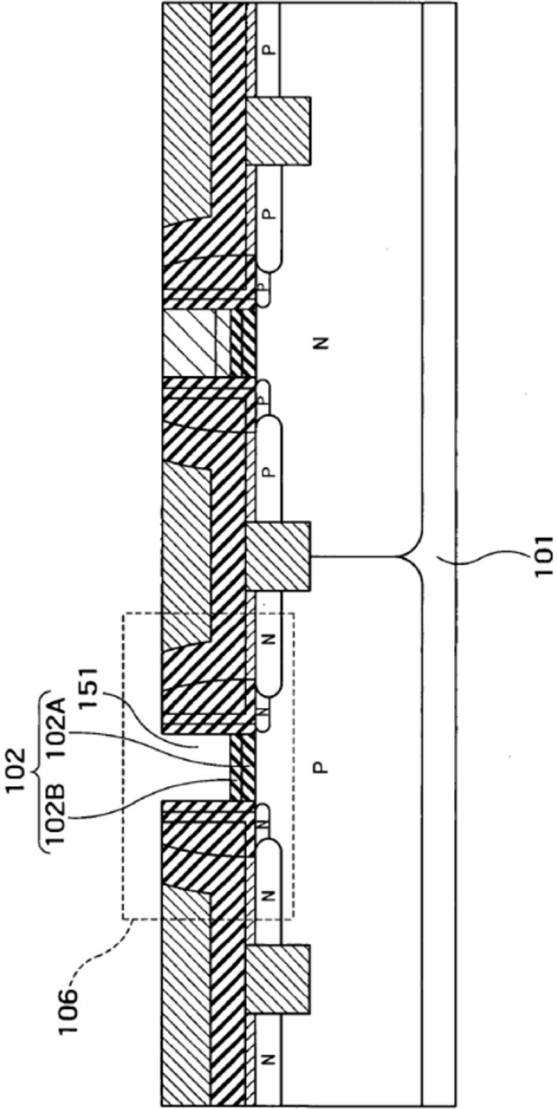
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer 103A which is made of conductive metal and a second conductive layer 103B which is made of conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p>  <p>[0053] Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 2H. Also, ions of B are implanted into the well diffusion layer 111 for</p>

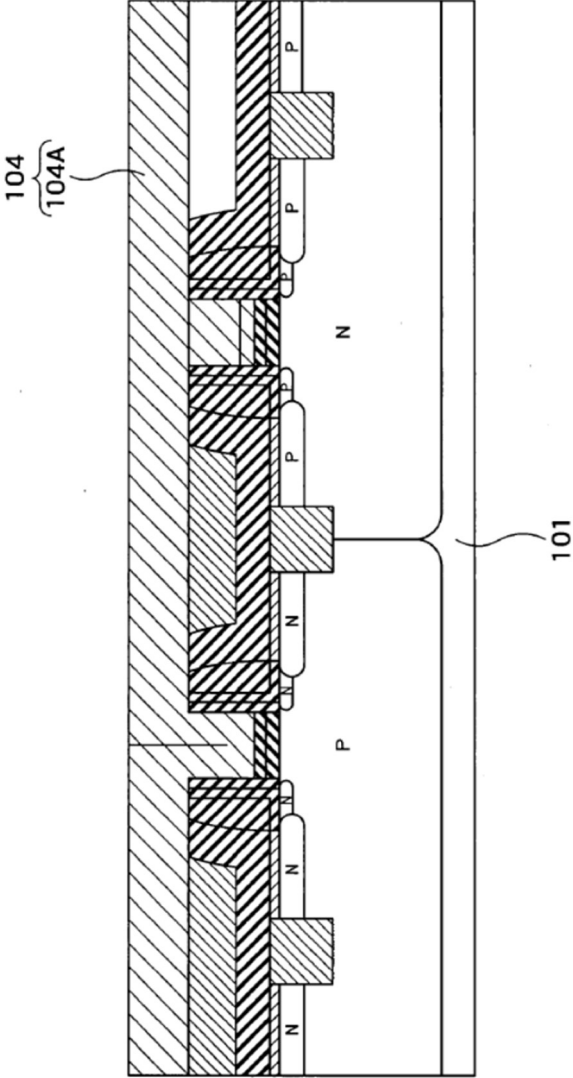
FIG. 1

Claim	Claim Language	<p data-bbox="207 338 245 1367">Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama</p> <p data-bbox="261 191 586 1503">the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 2H. In some cases, halo implantation is further performed to suppress short channel effects. Then, side wall spacers 143, each of which is made of a silicon nitride film, are formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.</p> <div data-bbox="651 499 1068 1461"> </div> <p data-bbox="1117 915 1154 1052">FIG. 2H</p> <p data-bbox="1214 218 1325 1503">[0054] Note that although each side wall spacer of the first embodiment has a two-layer structure of the first side wall spacer 142 made of the silicon oxide film and the second side wall spacer 143 made of the silicon nitride film, it may have a one-layer structure, for example, of only a silicon</p>
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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>nitride film or a laminated structure of three or more layers including, for example, a silicon oxide film and silicon nitride film.</p> <p>[0055] Next, as shown in FIG. 2I, silicide films 144 are formed in a self-aligned manner on the surfaces of the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET. Although NiSi films are adopted as the silicide films 144 in this embodiment, PtSi films, ErSi films, NiPtSi films, NiErSi films, or the like may be adopted as the silicide films 144 instead.</p> <div data-bbox="602 491 1045 1465"> <p>FIG. 2I</p> </div> <p>[0056] Next, as shown in FIG. 2J, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 2J, an interlayer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 2J, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the W layers 103B are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p style="text-align: center;">FIG. 2K</p> <p>[0058] Next, as shown in FIG. 2L, in the NMOSFET region 106, the Ru layer 103A on the gate dielectric film 102 for the NMOSFET is etched in an atmosphere containing oxygen radical. With the above-described manufacturing step, the hafnium silicon oxynitride film 102B in the NMOSFET region 106 is exposed. The resist 231 may be removed before or after the removal of the Ru layer 103A. Through the above-described manufacturing steps, in the NMOSFET region 106, the dummy gate electrode 103 on the gate dielectric film 102 is removed, thereby forming a trench 151 on the gate dielectric film 102.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="852 850 901 1018">FIG. 2L</p> <p data-bbox="933 210 1193 1501">[0059] Next, as shown in FIG. 2M, conductive metal, which is a material for forming a third conductive layer 104A of the gate electrode 104 for the NMOSFET, is deposited over the entire surface by CVD. Examples of the conductive metal include TaSiN which is formed using pentakis(ethylmethylamino)tantalum, and ammonia, and ammoniac, HfN which is formed in an atmosphere containing tetrakis(ethylmethylamino)hafnium and ammonia, HfSi which is formed using tetrakis(ethylmethylamino)hafnium and tetrakis(ethylmethylamino)silicon, and WSi which is formed using tungsten hexafluoride and dichlorosilane.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="873 871 914 1024">FIG. 2M</p> <p data-bbox="976 247 1084 1499">[0060] Note that although the gate electrode 104 for the NMOSFET of the first embodiment has a one-layer structure of only the conductive layer 104A made of the conductive metal, it may have a laminated structure of two or more layers including a conductive layer made of conductive metal.</p> <p data-bbox="1117 212 1334 1499">[0061] Next, as shown in FIG. 2N, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback). Through the above-described manufacturing steps, in the NMOSFET region 106, the material for forming the gate electrode is buried in the trench 151 on the gate dielectric film 102, thereby forming the gate electrode 104 for the NMOSFET with a different configuration from that of the gate electrode 103 for the PMOSFET. Since the gate electrode 104 for the NMOSFET (the third conductive layer 104A) is formed in the hole by CVD, a trace of a streaky</p>

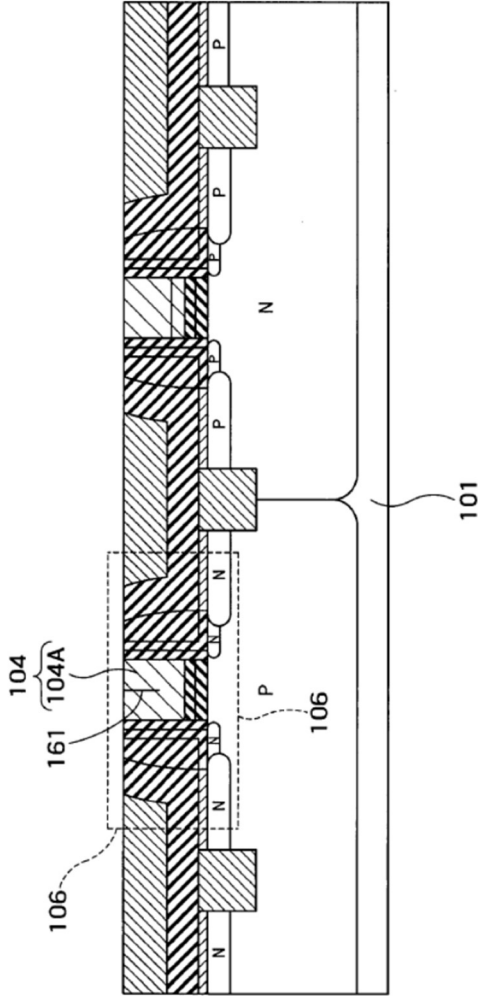
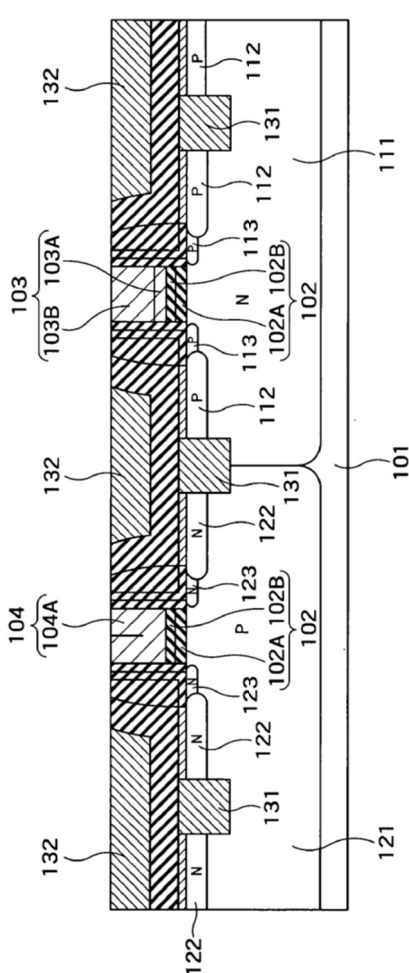
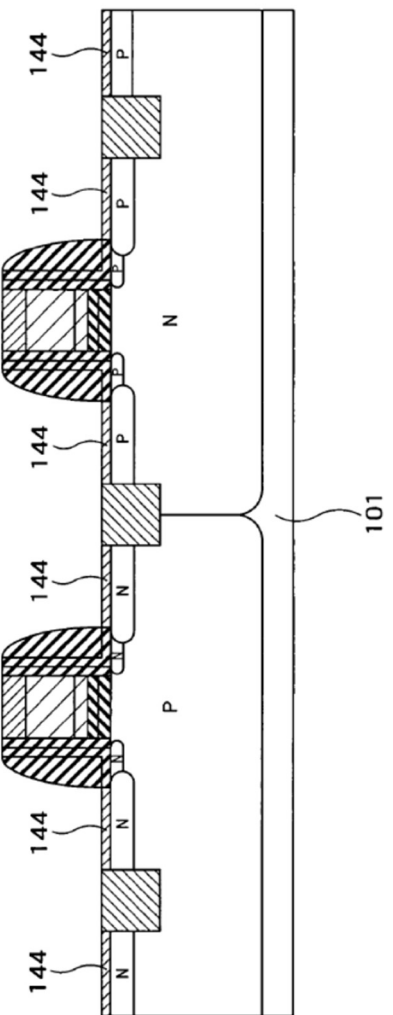
Claim	Claim Language	<p data-bbox="207 338 245 1367">Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama</p> <p data-bbox="264 216 334 1501">seam 161 which does not remain in the gate electrode 103 for the PMOSFET (the first conductive layer 103A and second conductive layer 103B) remains in the gate electrode 104 for the NMOSFET.</p> <div data-bbox="380 491 854 1480">  <p data-bbox="886 919 924 1058">FIG. 2N</p> </div> <p data-bbox="972 216 1154 1501">[0065] Moreover, in the first embodiment, the gate electrode 104 for the NMOSFET is formed after the source/drain diffusion layer 112 (and extension diffusion layer 113) for the PMOSFET and the source/drain diffusion layer 122 (and extension diffusion layer 123) for the NMOSFET are formed. Accordingly, the possibility of change in the work function of the metal electrode of the NMOSFET in the step of forming the source/drain diffusion layers (and extension diffusion layers) is reduced.</p> <p data-bbox="1174 191 1356 1501">[0066] Therefore, in the first embodiment, gate dielectric films with preferable characteristics such as a preferable film quality, and gate electrodes with preferable characteristics such as a preferable work function, can be used as gate dielectric films and gate electrodes constituting a PMOSFET and an NMOSFET. Accordingly, in the first embodiment, it is possible to manufacture a semiconductor device including a high-performance CMOSFET.</p>
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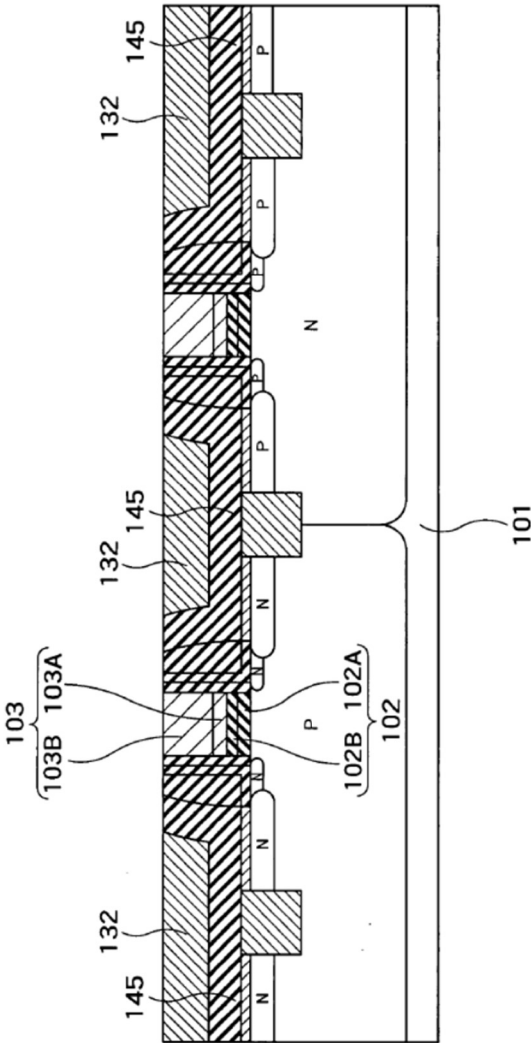
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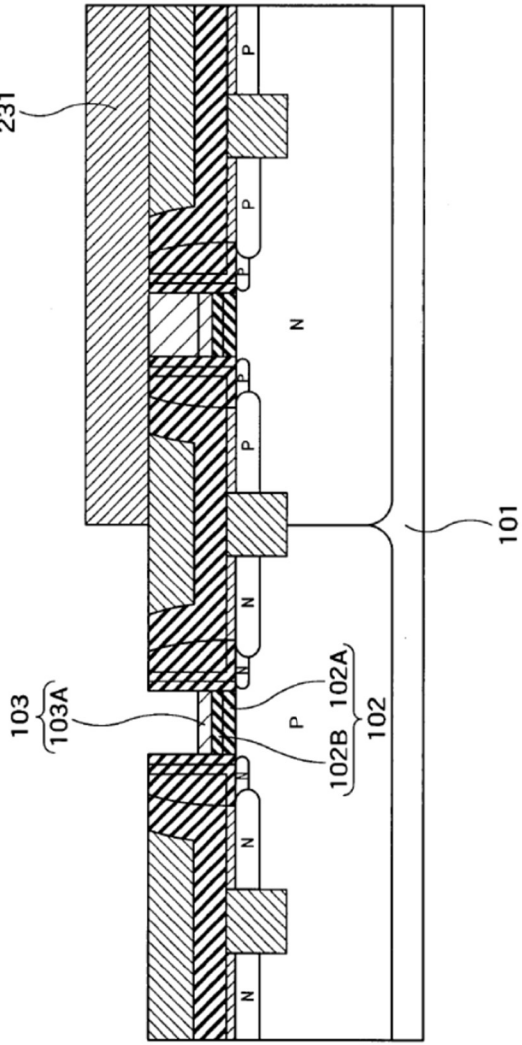
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>[0067] Additionally, in the first embodiment, the gate electrode 103 for the PMOSFET is formed by etching before formation of the inter layer dielectric film 132, and the gate electrode 104 for the NMOSFET is formed by the damascene process after formation of the inter layer dielectric film 132. Further, in the first embodiment, the gate electrode 103 for the PMOSFET formed in the NMOSFET region is used as a dummy electrode substituting for the gate electrode 104 for the NMOSFET. Therefore, in the first embodiment, the gate electrode 103 for the PMOSFET formed in the NMOSFET region is not wastefully removed in the etching step, and effectively used as the dummy electrode substituting for the gate electrode 104 for the NMOSFET until it is removed prior to the damascene process. Furthermore, in the first embodiment, since the step of forming the dummy electrode is integrated into the step of forming the gate electrode 103 for the PMOSFET, the number of steps required for the formation of the dummy electrode can be saved.</p> <p>[0068] In the damascene gate process explained as a background art, a dummy gate dielectric film (silicon oxide) is damaged in removing a dummy gate electrode (polysilicon), so it is necessary to remove also the dummy gate dielectric film in removing the dummy gate electrode. However, in the first embodiment, the dummy electrode in contact with the gate dielectric film 102 (second dielectric film 102B) made of the high-permittivity dielectric film, is the gate electrode 103 for the PMOSFET (first conductive layer 103A) made of the conductive metal. Particularly, in the first embodiment, the conductive metal is Ru, which is conductive metal capable of being removed without a chemical solution. Accordingly, in the first embodiment, it is possible to avoid unnecessary damage to the gate dielectric film 102 and unnecessary removal of the gate dielectric film 102, in removing the dummy electrode.</p> <p>[0072] The semiconductor device shown in FIG. 3 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer</p>

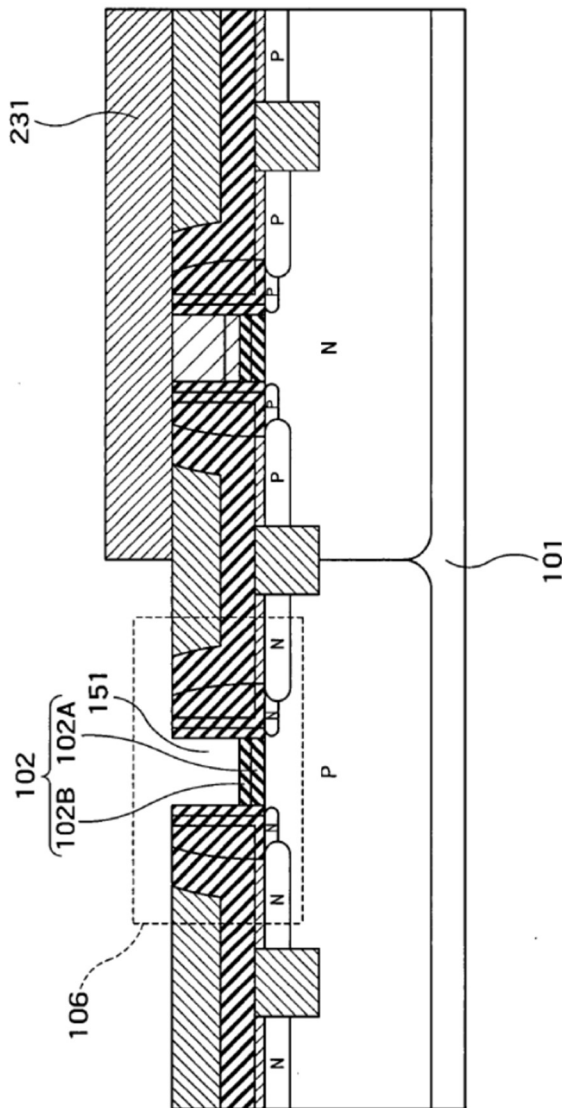
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<p>103A which is made of conductive metal and a second conductive layer 103B which is made of conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p>  <p>FIG. 3</p> <p>[0086] Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 4H. Also, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 4H. Then, side wall spacers 143, each of which is made of a silicon nitride film, are</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.</p> <p>FIG. 4H</p> <p>[0087] Next, as shown in FIG. 4I, silicide films 144 are formed in a self-aligned manner on the surfaces of the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p style="text-align: center;">FIG. 4I</p> <p>[0088] Next, as shown in FIG. 4J, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 4J, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 4J, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the TiN layers 103B are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		 <p data-bbox="829 898 867 1031">FIG. 4J</p> <p data-bbox="915 218 1062 1499">[0089] Next, as shown in FIG. 4K, in the NMOSFET region 106, the TiN layer 103B above the gate dielectric film 102 for the NMOSFET is etched using a resist 231 as a mask and using a chemical solution such as a solution containing hydrogen peroxide. With the above-described manufacturing step, the W layer 103A in the NMOSFET region 106 is exposed.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="831 884 868 1031">FIG. 4K</p> <p data-bbox="917 210 1166 1499">[0090] Next, as shown in FIG. 4L, in the NMOSFET region 106, the W layer 103A on the gate dielectric film 102 for the NMOSFET is etched using the resist 231 as a mask and using a chemical solution such as a solution containing hydrogen peroxide. With the above-described manufacturing step, the hafnium silicon oxynitride film 102B in the NMOSFET region 106 is exposed. Through the above-described manufacturing steps, in the NMOSFET region 106, the dummy gate electrode 103 on the gate dielectric film 102 is removed, thereby forming a trench 151 on the gate dielectric film 102.</p>

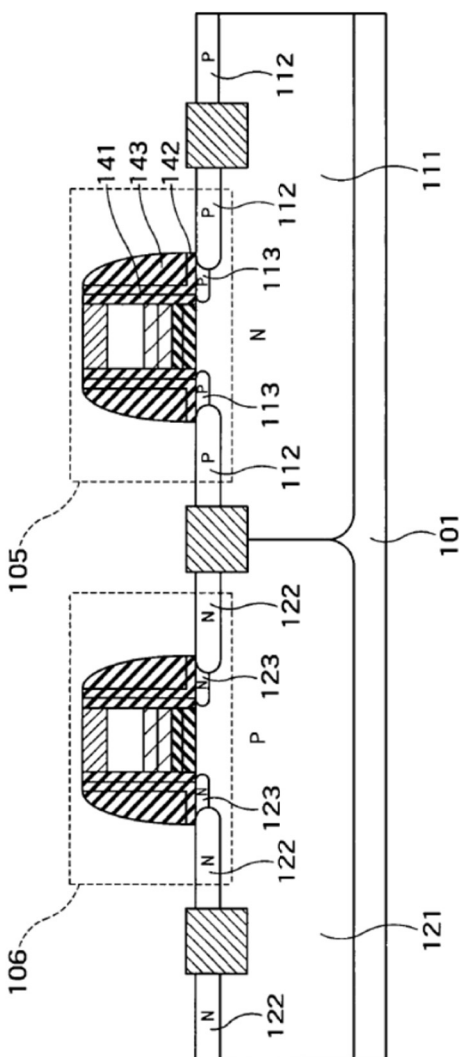
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Claim Language		
Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama		 <p>FIG. 4L</p> <p>[0091] Next, as shown in FIG. 4M, conductive metal, which is a material for forming a third conductive layer 104A of the gate electrode 104 for the NMOSFET, is deposited over the entire surface by CVD. Examples of the conductive metal include TaC, which is formed using pentakis(dimethylamino)tantalum and methane.</p>

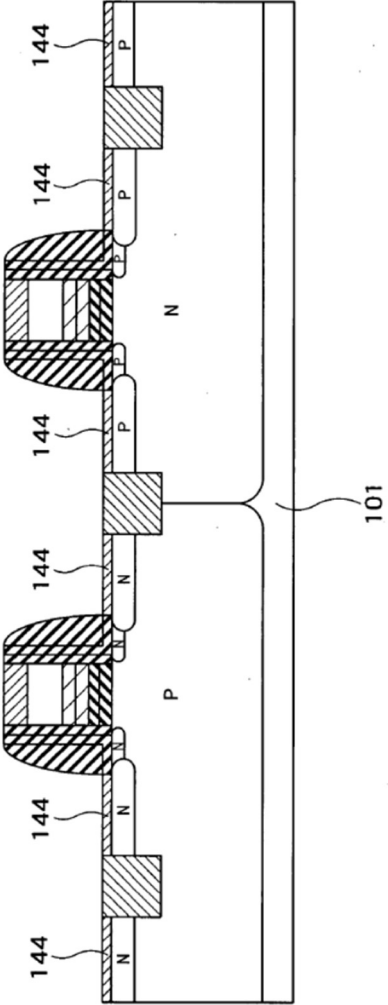
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<div data-bbox="272 384 857 1480"> </div> <div data-bbox="889 856 927 1012"> <p>FIG. 4M</p> </div> <div data-bbox="971 191 1393 1501"> <p>[0092] Note that although the gate electrode 104 for the NMOSFET of the second embodiment has a one-layer structure of only the conductive layer 104A made of the conductive metal, it may have a laminated structure of two or more layers including a conductive layer made of conductive metal.</p> <p>[0093] Next, as shown in FIG. 4N, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback). Through the above-described manufacturing steps, in the NMOSFET region 106, the material for forming the gate electrode is buried in the trench 151 on the gate dielectric film 102, thereby forming the gate electrode 104 for the NMOSFET with a different configuration from that of the gate electrode 103 for the PMOSFET. Since the gate electrode 104 for the NMOSFET (the third conductive layer 104A) is formed in the hole by CVD, a trace of a streaky seam 161 which does not remain in the gate electrode 103 for the PMOSFET (the first conductive layer 103A and second conductive layer 103B) remains in the gate electrode 104 for the NMOSFET.</p> </div>

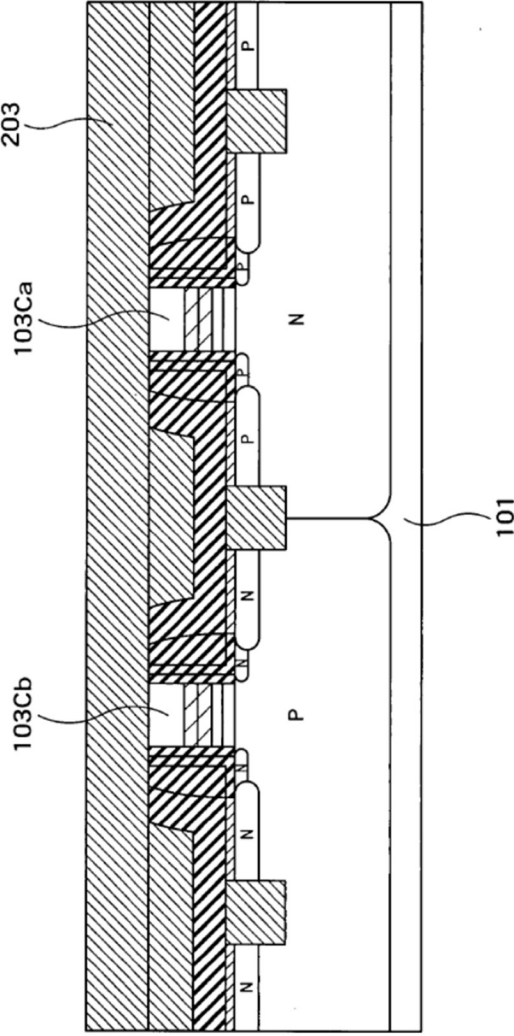
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<div data-bbox="267 422 764 1472"> </div> <p data-bbox="797 873 829 1024">FIG. 4N</p> <p data-bbox="862 212 1008 1503">[0095] In the second embodiment, the dummy electrode (the gate electrode 103 for the PMOSFET) includes the W layer 103A and TiN layer 103B made of W and TiN respectively, which are conductive metals capable of being removed using a chemical solution. For this reason, in the second embodiment, it is possible to easily remove the dummy electrode at low cost.</p> <p data-bbox="1040 212 1404 1503">[0098] The semiconductor device shown in FIG. 5 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes three electrode-constituting layers: a first conductive</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<p>layer 103A which is made of conductive metal, a second conductive layer 103B which is made of conductive metal, and a semiconductor layer 103C which is made of semiconductor. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p> <p>FIG. 5</p> <p>[0111] Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 6I. Also, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 6I. Then, side wall spacers 143, each of which is made of a silicon nitride film, are</p>

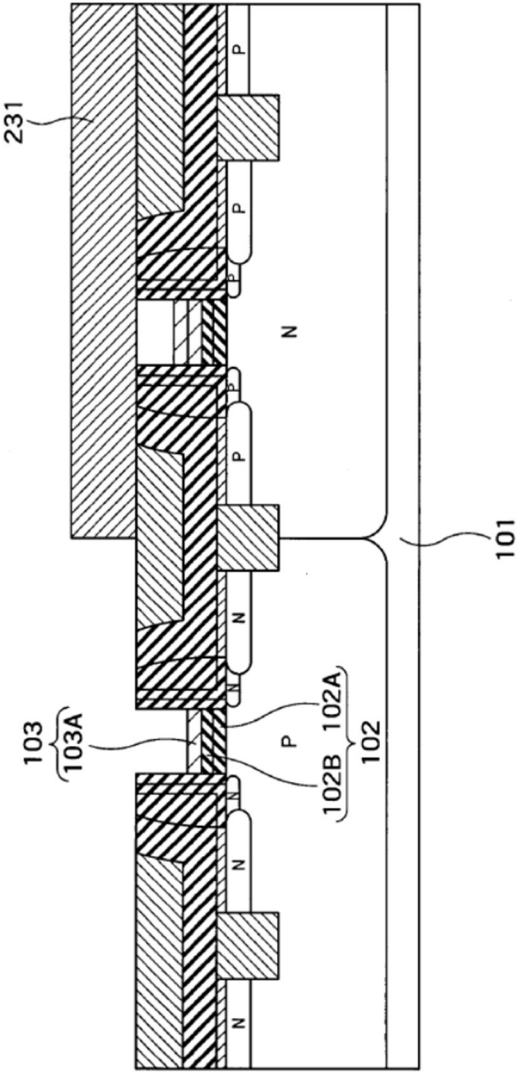
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Claim		Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
Claim Language		<p>formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.</p>  <p>FIG. 6I</p> <p>[0112] Next, as shown in FIG. 6J, silicide films 144 are formed in a self-aligned manner on the surfaces of the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="719 919 755 1045">FIG. 6J</p> <p data-bbox="820 226 1068 1501">[0113] Next, as shown in FIG. 6K, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 6K, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 6K, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the semiconductor layers 103C (non-diffusion layers 103Ca and diffusion layers 103Cb) are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>

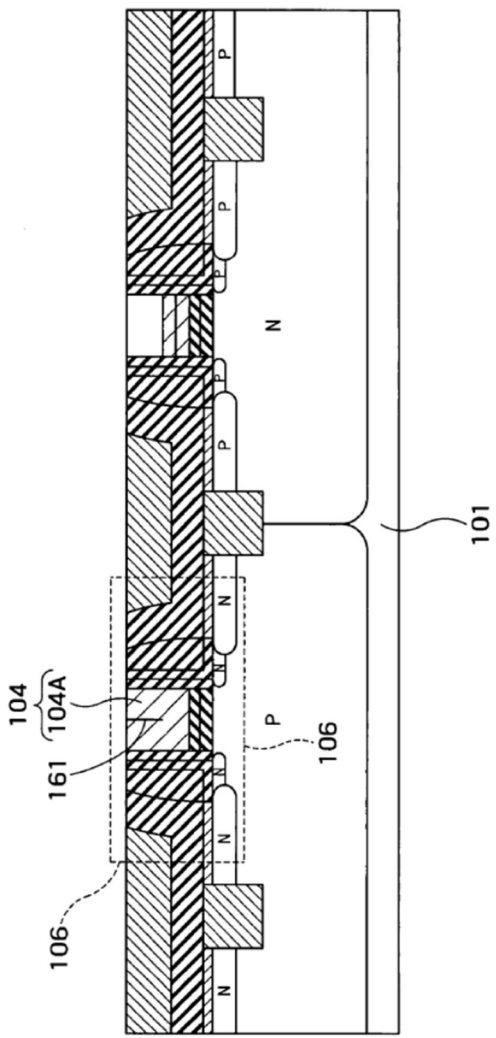
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="824 909 862 1052">FIG. 6L</p> <p data-bbox="938 193 1079 1493">[0115] Next, as shown in FIG. 6M, in the NMOSFET region 106, the semiconductor layer 103C above the gate dielectric film 102 for the NMOSFET is etched using a resist 231 as a mask and using a chemical solution such as a solution containing hydrogen peroxide. With the above-described manufacturing steps, the TiN layer 103B in the NMOSFET region 106 is exposed.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<div data-bbox="272 453 797 1465"> <p>FIG. 6M</p> </div> <p>[0116] Next, as shown in FIG. 6N, in the NMOSFET region 106, the TiN layer 103B above the gate dielectric film 102 for the NMOSFET is etched using the resist 231 as a mask and using a chemical solution such as a solution containing hydrogen peroxide. With the above-described manufacturing step, the W layer 103A in the NMOSFET region 106 is exposed.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="828 871 868 1029">FIG. 6N</p> <p data-bbox="933 210 1185 1501">[0117] Next, as shown in FIG. 6O, in the NMOSFET region 106, the W layer 103A on the gate dielectric film 102 for the NMOSFET is etched using the resist 231 as a mask and using a chemical solution such as a solution containing hydrogen peroxide. With the above-described manufacturing step, the hafnium silicon oxynitride film 102B in the NMOSFET region 106 is exposed. Through the above-described manufacturing steps, in the NMOSFET region 106, the dummy gate electrode 103 on the gate dielectric film 102 is removed, thereby forming a trench 151 on the gate dielectric film 102.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<div data-bbox="272 451 812 1470"> </div> <p data-bbox="841 892 880 1039">FIG. 6P</p> <p data-bbox="930 193 1255 1501">[0119] Next, as shown in FIG. 6Q, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback). Through the above-described manufacturing steps, in the NMOSFET region 106, the material for forming the gate electrode is buried in the trench 151 on the gate dielectric film 102, thereby forming the gate electrode 104 for the NMOSFET with a different configuration from that of the gate electrode 103 for the PMOSFET. Since the gate electrode 104 for the NMOSFET (the third conductive layer 104A) is formed in the hole by CVD, a trace of a streaky seam 161 which does not remain in the gate electrode 103 for the PMOSFET (the first conductive layer 103A, second conductive layer 103B, and semiconductor layer 103C) remains in the gate electrode 104 for the NMOSFET.</p>

EXHIBIT 686A2

Claim		Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
Claim Language		 <p>FIG. 6Q</p> <p>[0121] In the third embodiment, the gate electrode 103 for the PMOSFET includes the first conductive layer 103A made of the conductive metal, the second conductive layer 103B made of the conductive metal, and the semiconductor layer (silicide layer) 103C made of the semiconductor (silicide). For this reason, in the third embodiment, the gate resistance of the PMOSFET is relatively low.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
25 [f]	the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes, and the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region.	<p>Aoyama, as evidenced by the example citations below, discloses the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes, and the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region.</p> <p>[0056] Next, as shown in FIG. 2J, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 2J, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 2J, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the W layers 103B are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p> <p>FIG. 2J</p> <p>[0088] Next, as shown in FIG. 4J, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 4J, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 4J, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching).</p>

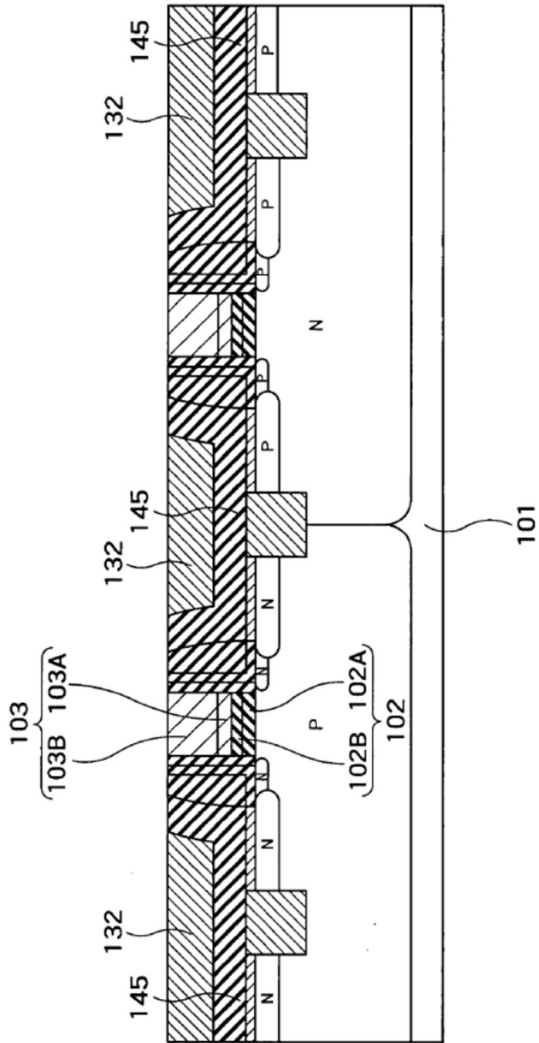
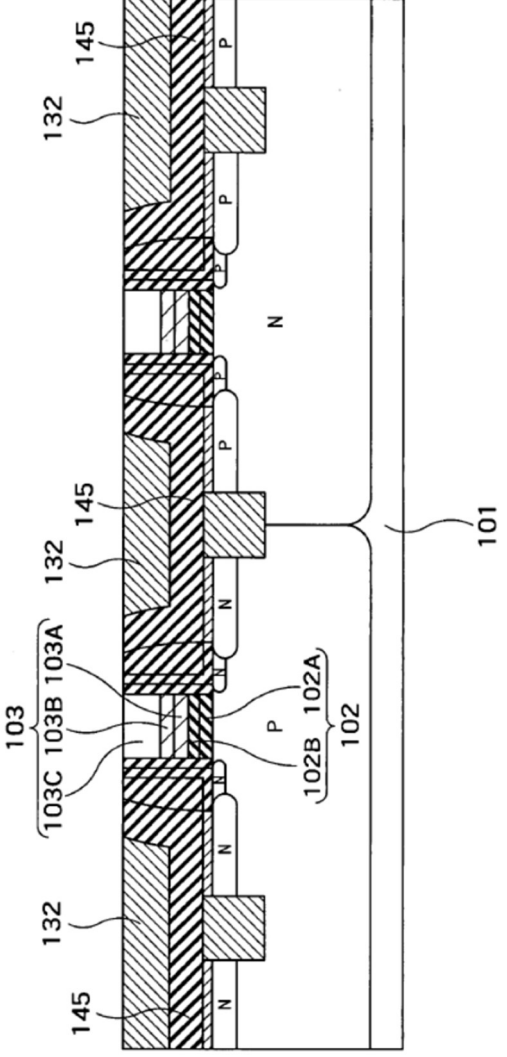
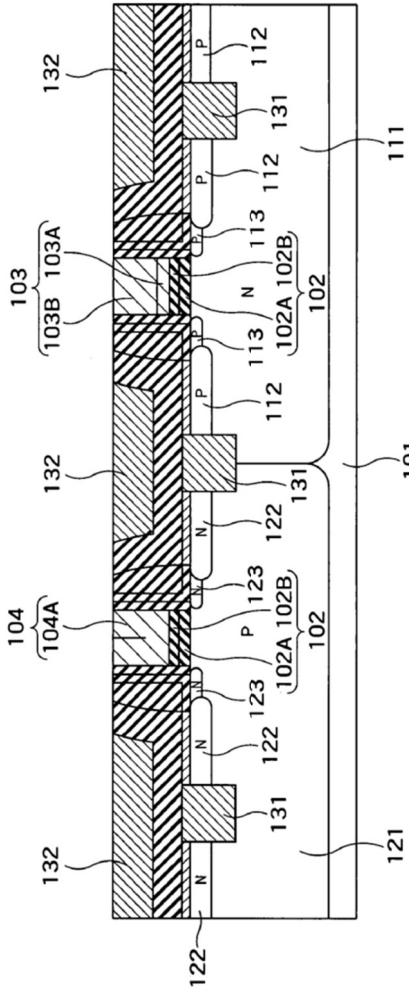
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>With the above-described manufacturing steps, the TiN layers 103B are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>  <p style="text-align: center;">FIG. 4J</p> <p>[0113] Next, as shown in FIG. 6K, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 6K, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 6K, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the semiconductor layers 103C (non-diffusion layers 103Ca and diffusion layers 103Cb) are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>

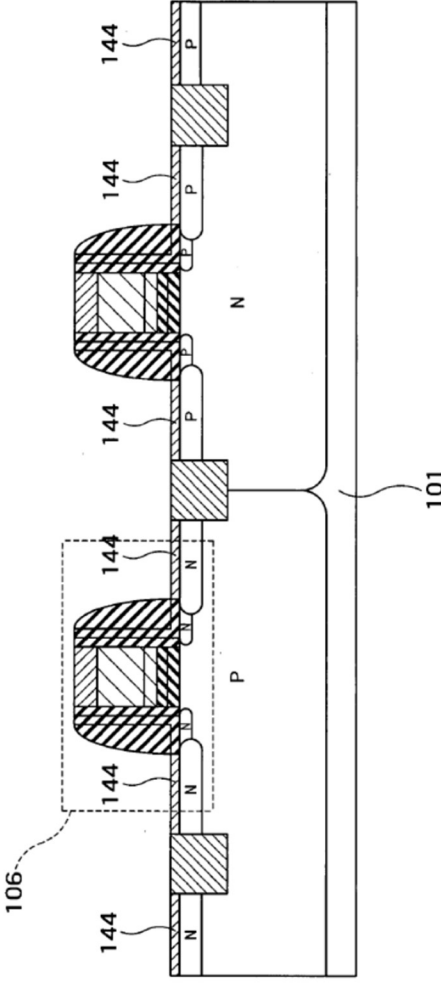
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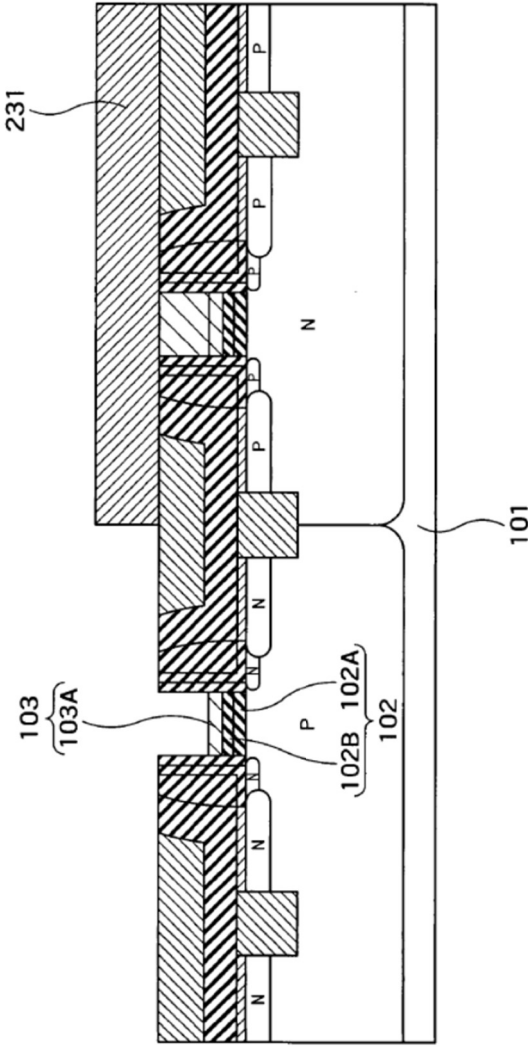
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
26	The semiconductor device of claim 25, wherein the first metal film has a thickness smaller than that of the second metal film.	 <p>Aoyama's silicon nitride layer causes a first stress in a gate length direction of a channel region in the first active region due to the same reasons alleged against the accused product, e.g. due to intrinsic deposition stress, thermal mismatch, and/or lattice mismatch. To the extent the stress is not disclosed, it would be obvious for a person of ordinary skill in the art to use a stress inducing silicon nitride film for etch stopper film 145, as discussed in more detail in UMC's Invalidity Contentions.</p>
		<p>Aoyama, as evidenced by the example citations below, discloses the first metal film has a thickness smaller than that of the second metal film. In the examples where the first metal is 103A, Aoyama discloses it is 20 nm thick and is shown as being smaller than the conductive layer 104A. For the embodiments where the second metal and conductive layer is the two-layered disclosure of 104A, a person of ordinary skill in the art would understand that using different thicknesses for metal films in P type and N type transistors would be advantageous and thus obvious, as explained in more detail in UMC's Invalidity Contentions.</p>

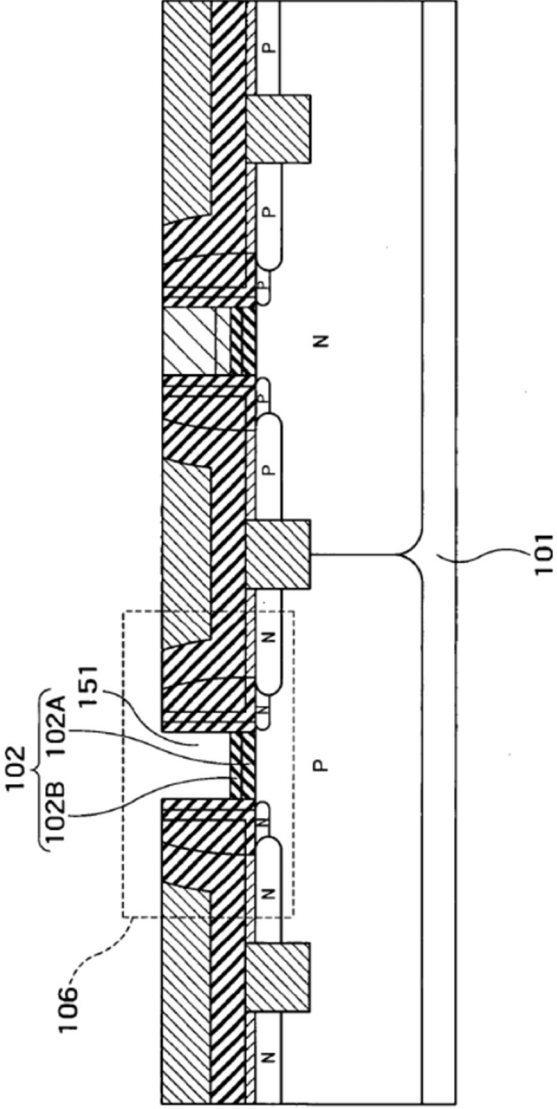
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>[0039] The semiconductor device shown in FIG. 1 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer 103A which is made of conductive metal and a second conductive layer 103B which is made of conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p>  <p style="text-align: center;">FIG. 1</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>[0053] Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 2H. Also, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 2H. In some cases, halo implantation is further performed to suppress short channel effects. Then, side wall spacers 143, each of which is made of a silicon nitride film, are formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<div data-bbox="289 499 711 1465"> </div> <p data-bbox="760 913 792 1052" style="text-align: center;">FIG. 2H</p> <p data-bbox="857 220 1036 1501">[0054] Note that although each side wall spacer of the first embodiment has a two-layer structure of the first side wall spacer 142 made of the silicon oxide film and the second side wall spacer 143 made of the silicon nitride film, it may have a one-layer structure, for example, of only a silicon nitride film or a laminated structure of three or more layers including, for example, a silicon oxide film and silicon nitride film.</p> <p data-bbox="1071 262 1250 1501">[0055] Next, as shown in FIG. 2I, silicide films 144 are formed in a self-aligned manner on the surfaces of the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET. Although NiSi films are adopted as the silicide films 144 in this embodiment, PtSi films, ErSi films, NiPtSi films, NiErSi films, or the like may be adopted as the silicide films 144 instead.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p style="text-align: center;">FIG. 2I</p> <p>[0056] Next, as shown in FIG. 2J, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 2J, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 2J, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the W layers 103B are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p style="text-align: center;">FIG. 2K</p> <p>[0058] Next, as shown in FIG. 2L, in the NMOSFET region 106, the Ru layer 103A on the gate dielectric film 102 for the NMOSFET is etched in an atmosphere containing oxygen radical. With the above-described manufacturing step, the hafnium silicon oxynitride film 102B in the NMOSFET region 106 is exposed. The resist 231 may be removed before or after the removal of the Ru layer 103A. Through the above-described manufacturing steps, in the NMOSFET region 106, the dummy gate electrode 103 on the gate dielectric film 102 is removed, thereby forming a trench 151 on the gate dielectric film 102.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="857 856 894 1010">FIG. 2L</p> <p data-bbox="938 212 1192 1499">[0059] Next, as shown in FIG. 2M, conductive metal, which is a material for forming a third conductive layer 104A of the gate electrode 104 for the NMOSFET, is deposited over the entire surface by CVD. Examples of the conductive metal include TaSiN which is formed using pentakis(ethylmethylamino)tantalum, and ammonia, and ammoniac, HfN which is formed in an atmosphere containing tetrakis(ethylmethylamino)hafnium and ammonia, HfSi which is formed using tetrakis(ethylmethylamino)hafnium and tetrakis(ethylmethylamino)silicon, and WSi which is formed using tungsten hexafluoride and dichlorosilane.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<div data-bbox="272 411 841 1482"> <p>FIG. 2M</p> </div> <p>[0060] Note that although the gate electrode 104 for the NMOSFET of the first embodiment has a one-layer structure of only the conductive layer 104A made of the conductive metal, it may have a laminated structure of two or more layers including a conductive layer made of conductive metal.</p> <p>[0061] Next, as shown in FIG. 2N, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback). Through the above-described manufacturing steps, in the NMOSFET region 106, the material for forming the gate electrode is buried in the trench 151 on the gate dielectric film 102, thereby forming the gate electrode 104 for the NMOSFET with a different configuration from that of the gate electrode 103 for the PMOSFET. Since the gate electrode 104 for the NMOSFET (the third conductive layer 104A) is formed in the hole by CVD, a trace of a streaky</p>

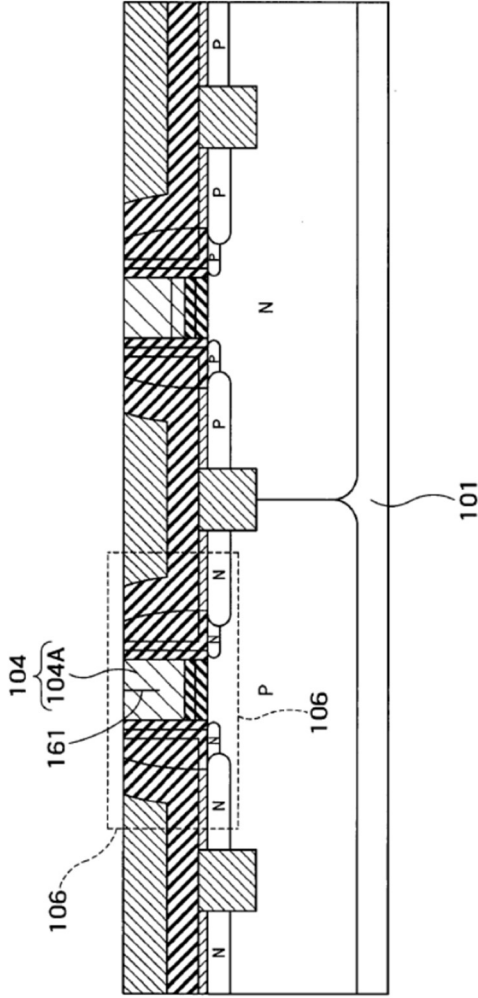
Claim	Claim Language	<p data-bbox="207 338 245 1367">Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama</p> <p data-bbox="264 216 334 1501">seam 161 which does not remain in the gate electrode 103 for the PMOSFET (the first conductive layer 103A and second conductive layer 103B) remains in the gate electrode 104 for the NMOSFET.</p> <div data-bbox="380 491 854 1482">  <p data-bbox="886 919 924 1058">FIG. 2N</p> </div> <p data-bbox="972 216 1154 1501">[0065] Moreover, in the first embodiment, the gate electrode 104 for the NMOSFET is formed after the source/drain diffusion layer 112 (and extension diffusion layer 113) for the PMOSFET and the source/drain diffusion layer 122 (and extension diffusion layer 123) for the NMOSFET are formed. Accordingly, the possibility of change in the work function of the metal electrode of the NMOSFET in the step of forming the source/drain diffusion layers (and extension diffusion layers) is reduced.</p> <p data-bbox="1174 191 1356 1501">[0066] Therefore, in the first embodiment, gate dielectric films with preferable characteristics such as a preferable film quality, and gate electrodes with preferable characteristics such as a preferable work function, can be used as gate dielectric films and gate electrodes constituting a PMOSFET and an NMOSFET. Accordingly, in the first embodiment, it is possible to manufacture a semiconductor device including a high-performance CMOSFET.</p>
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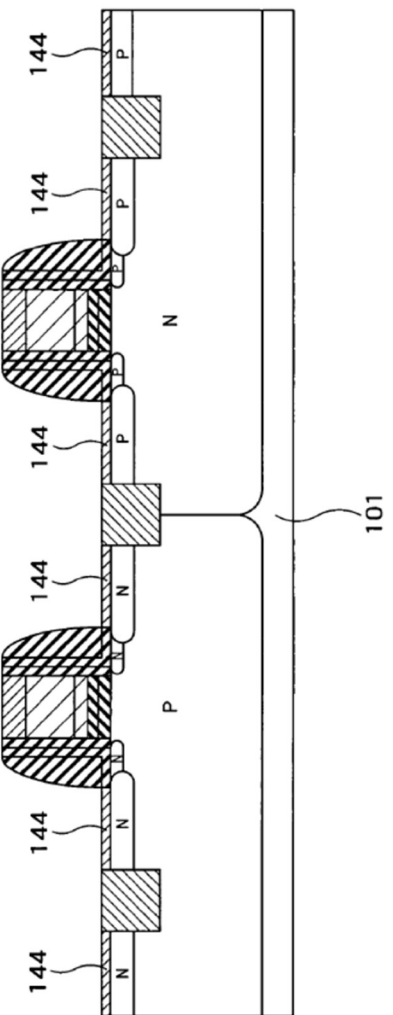
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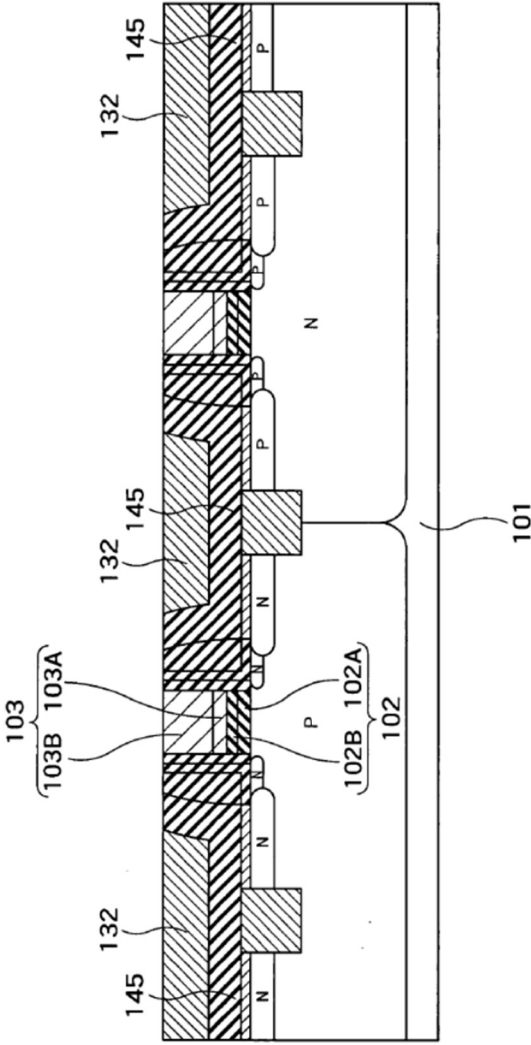
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>[0067] Additionally, in the first embodiment, the gate electrode 103 for the PMOSFET is formed by etching before formation of the inter layer dielectric film 132, and the gate electrode 104 for the NMOSFET is formed by the damascene process after formation of the inter layer dielectric film 132. Further, in the first embodiment, the gate electrode 103 for the PMOSFET formed in the NMOSFET region is used as a dummy electrode substituting for the gate electrode 104 for the NMOSFET. Therefore, in the first embodiment, the gate electrode 103 for the PMOSFET formed in the NMOSFET region is not wastefully removed in the etching step, and effectively used as the dummy electrode substituting for the gate electrode 104 for the NMOSFET until it is removed prior to the damascene process. Furthermore, in the first embodiment, since the step of forming the dummy electrode is integrated into the step of forming the gate electrode 103 for the PMOSFET, the number of steps required for the formation of the dummy electrode can be saved.</p> <p>[0068] In the damascene gate process explained as a background art, a dummy gate dielectric film (silicon oxide) is damaged in removing a dummy gate electrode (polysilicon), so it is necessary to remove also the dummy gate dielectric film in removing the dummy gate electrode. However, in the first embodiment, the dummy electrode in contact with the gate dielectric film 102 (second dielectric film 102B) made of the high-permittivity dielectric film, is the gate electrode 103 for the PMOSFET (first conductive layer 103A) made of the conductive metal. Particularly, in the first embodiment, the conductive metal is Ru, which is conductive metal capable of being removed without a chemical solution. Accordingly, in the first embodiment, it is possible to avoid unnecessary damage to the gate dielectric film 102 and unnecessary removal of the gate dielectric film 102, in removing the dummy electrode.</p> <p>[0072] The semiconductor device shown in FIG. 3 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer</p>

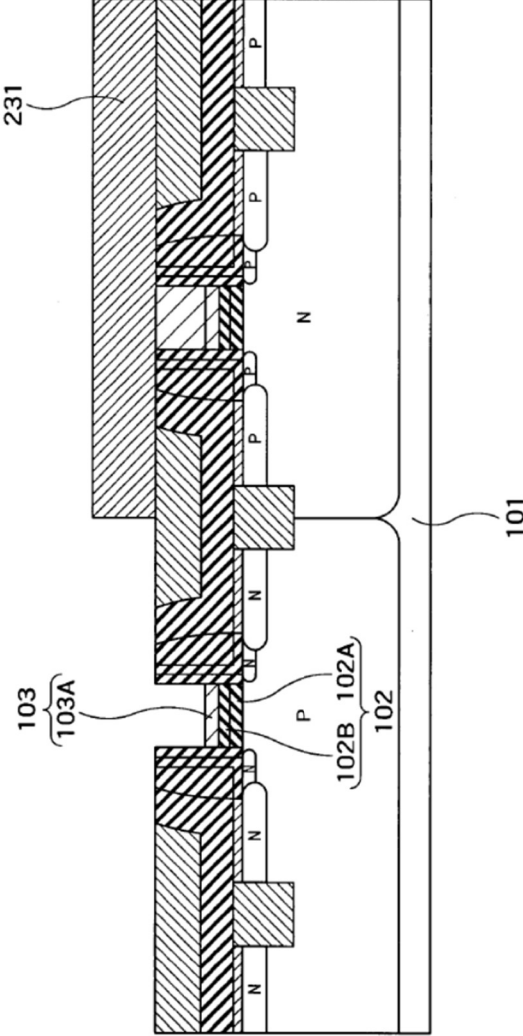
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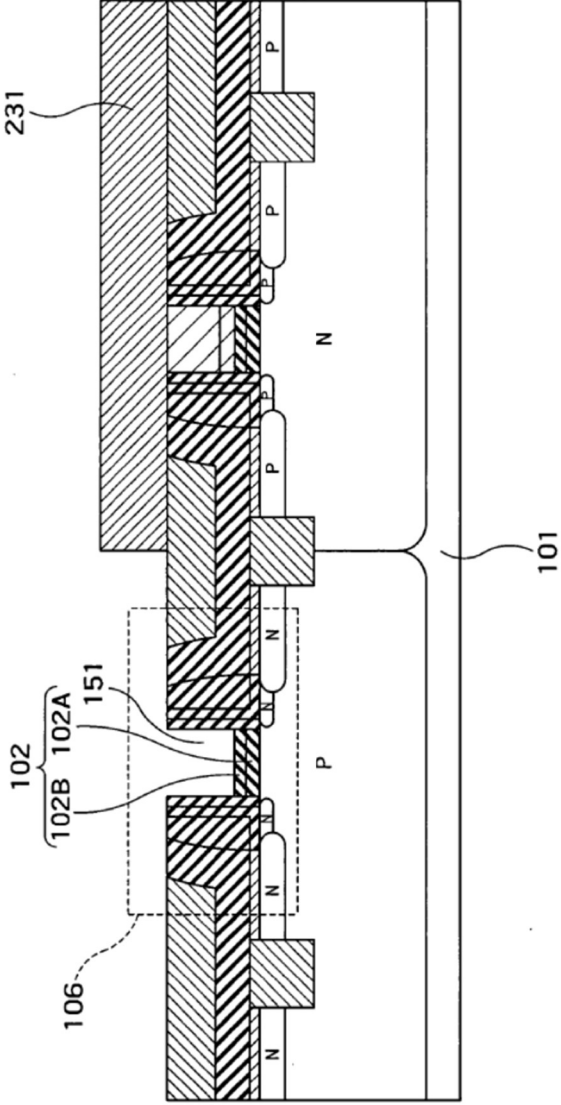
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>103A which is made of conductive metal and a second conductive layer 103B which is made of conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p> <p>FIG. 3</p> <p>[0086] Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 4H. Also, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 4H. Then, side wall spacers 143, each of which is made of a silicon nitride film, are</p>

Claim	Claim Language	<p data-bbox="212 338 245 1362">Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama</p> <p data-bbox="266 212 407 1503">formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.</p> <div data-bbox="440 464 862 1440"> </div> <p data-bbox="915 884 948 1026">FIG. 4H</p> <p data-bbox="985 264 1089 1503">[0087] Next, as shown in FIG. 4I, silicide films 144 are formed in a self-aligned manner on the surfaces of the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET.</p>
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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p style="text-align: center;">FIG. 4I</p> <p>[0088] Next, as shown in FIG. 4J, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 4J, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 4J, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the TiN layers 103B are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		 <p data-bbox="829 900 867 1035">FIG. 4J</p> <p data-bbox="915 218 1062 1499">[0089] Next, as shown in FIG. 4K, in the NMOSFET region 106, the TiN layer 103B above the gate dielectric film 102 for the NMOSFET is etched using a resist 231 as a mask and using a chemical solution such as a solution containing hydrogen peroxide. With the above-described manufacturing step, the W layer 103A in the NMOSFET region 106 is exposed.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="829 884 862 1031">FIG. 4K</p> <p data-bbox="919 212 1162 1503">[0090] Next, as shown in FIG. 4L, in the NMOSFET region 106, the W layer 103A on the gate dielectric film 102 for the NMOSFET is etched using the resist 231 as a mask and using a chemical solution such as a solution containing hydrogen peroxide. With the above-described manufacturing step, the hafnium silicon oxynitride film 102B in the NMOSFET region 106 is exposed. Through the above-described manufacturing steps, in the NMOSFET region 106, the dummy gate electrode 103 on the gate dielectric film 102 is removed, thereby forming a trench 151 on the gate dielectric film 102.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<div><p>FIG. 4L</p><p>[0091] Next, as shown in FIG. 4M, conductive metal, which is a material for forming a third conductive layer 104A of the gate electrode 104 for the NMOSFET, is deposited over the entire surface by CVD. Examples of the conductive metal include TaC, which is formed using pentakis(dimethylamino)tantalum and methane.</p></div>

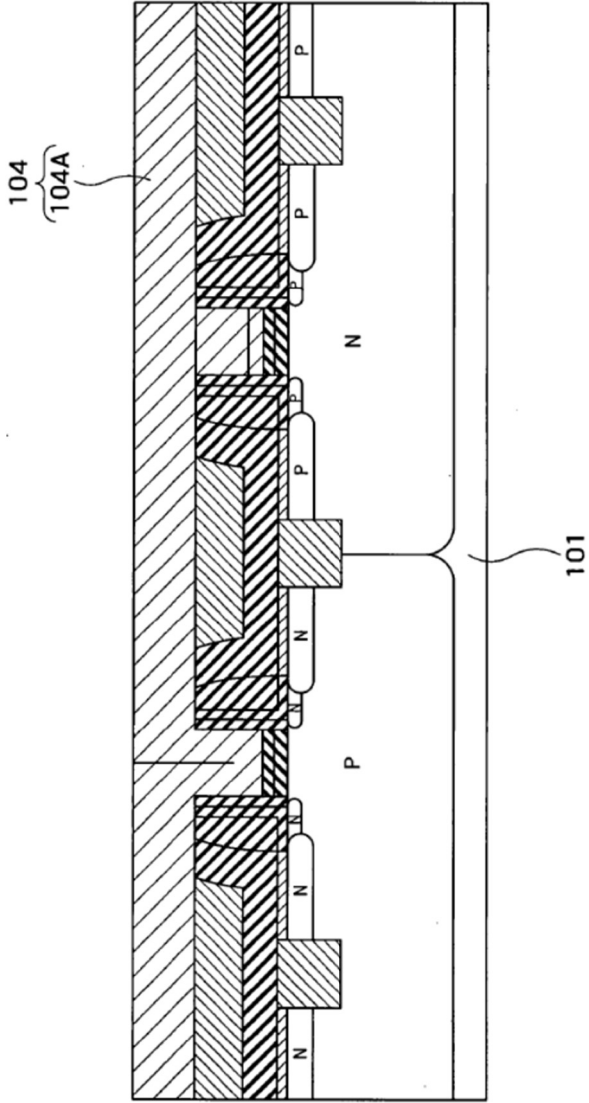
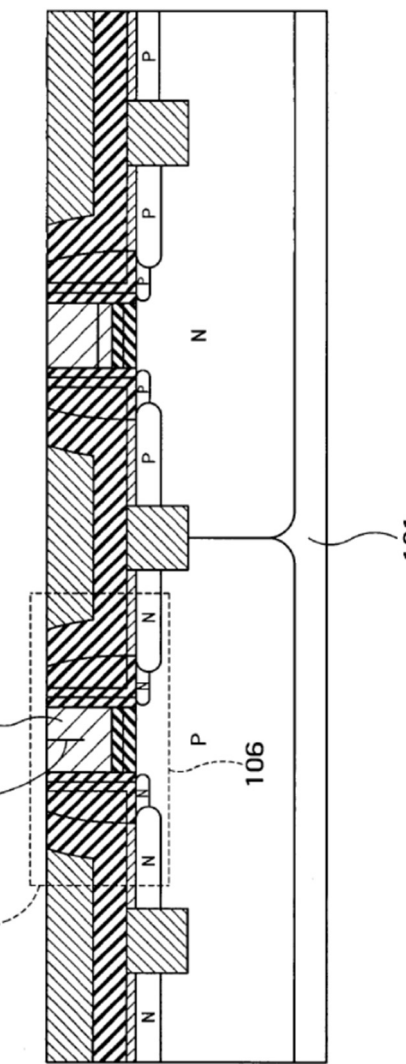
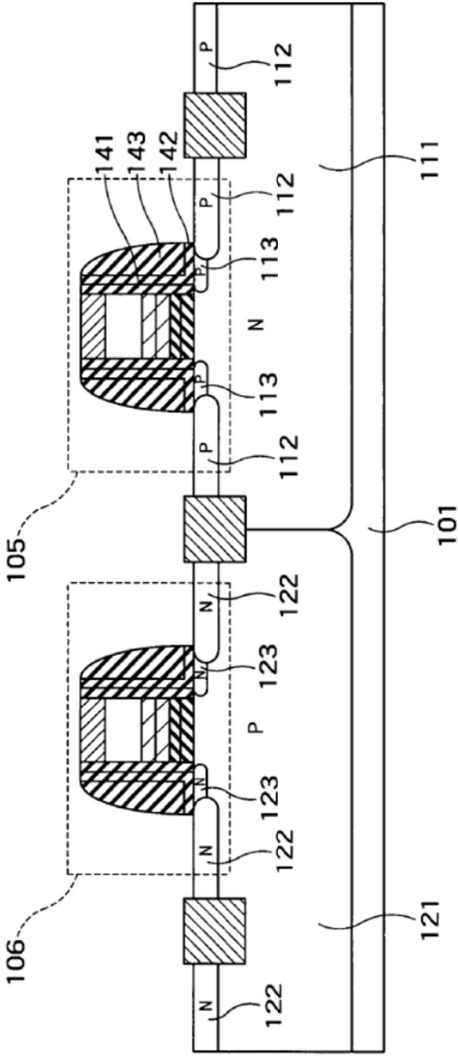
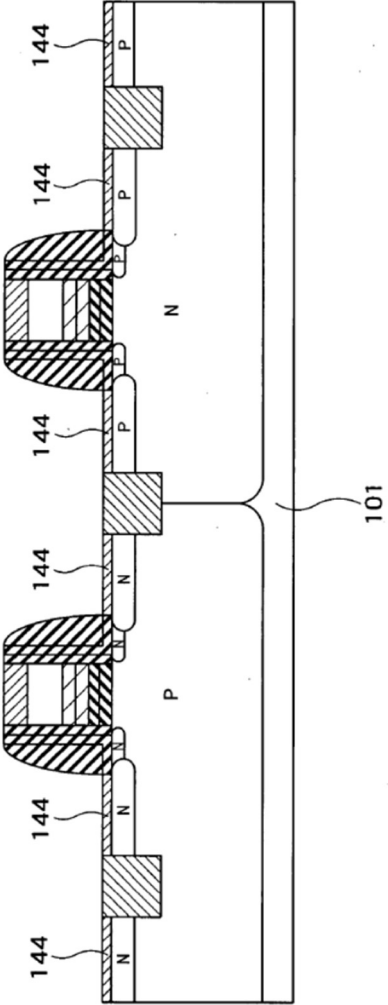
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<div data-bbox="272 384 857 1480">  </div> <div data-bbox="889 856 927 1012"> <p>FIG. 4M</p> </div> <div data-bbox="971 191 1393 1501"> <p>[0092] Note that although the gate electrode 104 for the NMOSFET of the second embodiment has a one-layer structure of only the conductive layer 104A made of the conductive metal, it may have a laminated structure of two or more layers including a conductive layer made of conductive metal.</p> <p>[0093] Next, as shown in FIG. 4N, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback). Through the above-described manufacturing steps, in the NMOSFET region 106, the material for forming the gate electrode is buried in the trench 151 on the gate dielectric film 102, thereby forming the gate electrode 104 for the NMOSFET with a different configuration from that of the gate electrode 103 for the PMOSFET. Since the gate electrode 104 for the NMOSFET (the third conductive layer 104A) is formed in the hole by CVD, a trace of a streaky seam 161 which does not remain in the gate electrode 103 for the PMOSFET (the first conductive layer 103A and second conductive layer 103B) remains in the gate electrode 104 for the NMOSFET.</p> </div>

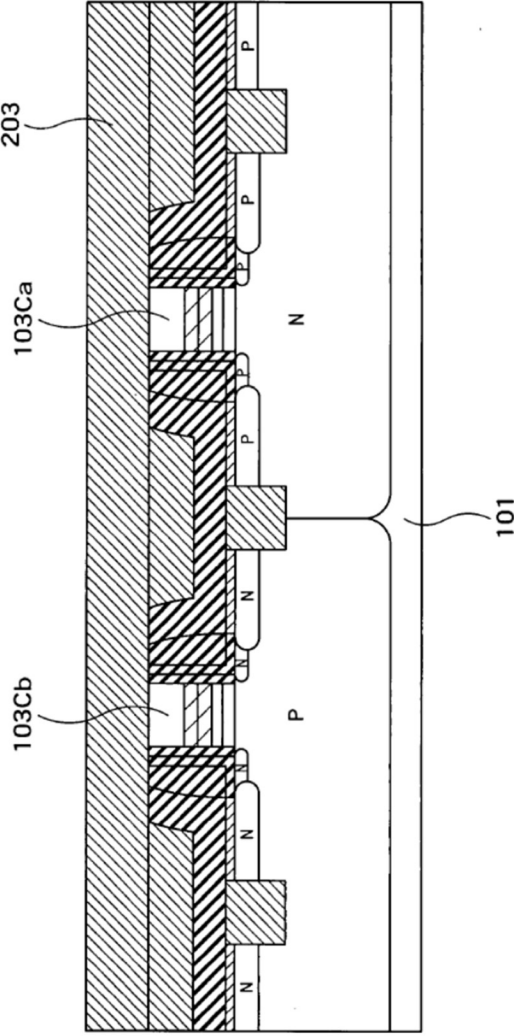
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Claim	
Claim Language	
Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama	 <p>FIG. 4N</p> <p>[0095] In the second embodiment, the dummy electrode (the gate electrode 103 for the PMOSFET) includes the W layer 103A and TiN layer 103B made of W and TiN respectively, which are conductive metals capable of being removed using a chemical solution. For this reason, in the second embodiment, it is possible to easily remove the dummy electrode at low cost.</p> <p>[0098] The semiconductor device shown in FIG. 5 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes three electrode-constituting layers: a first conductive</p>

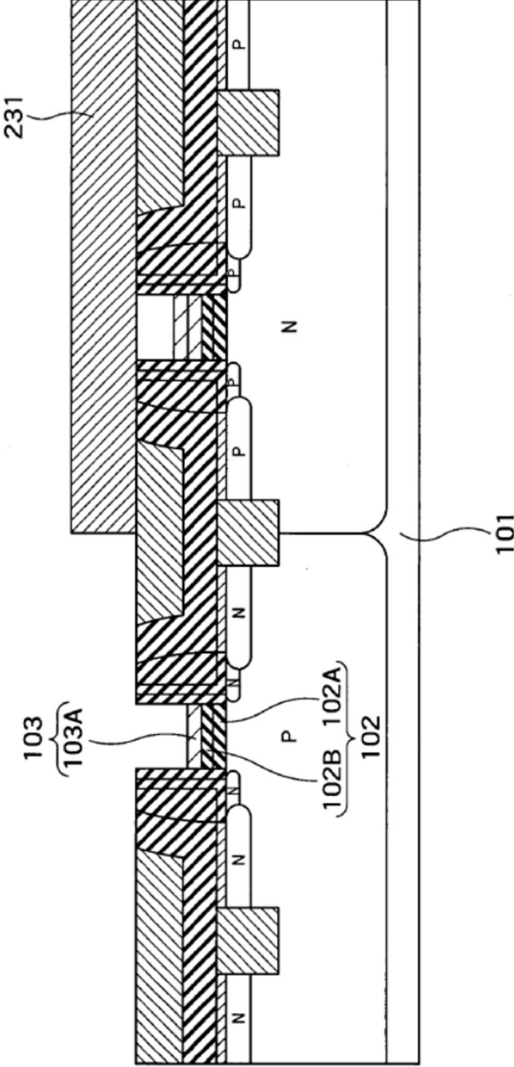
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<p>layer 103A which is made of conductive metal, a second conductive layer 103B which is made of conductive metal, and a semiconductor layer 103C which is made of semiconductor. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p> <p>FIG. 5</p> <p>[0111] Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 6I. Also, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 6I. Then, side wall spacers 143, each of which is made of a silicon nitride film, are</p>

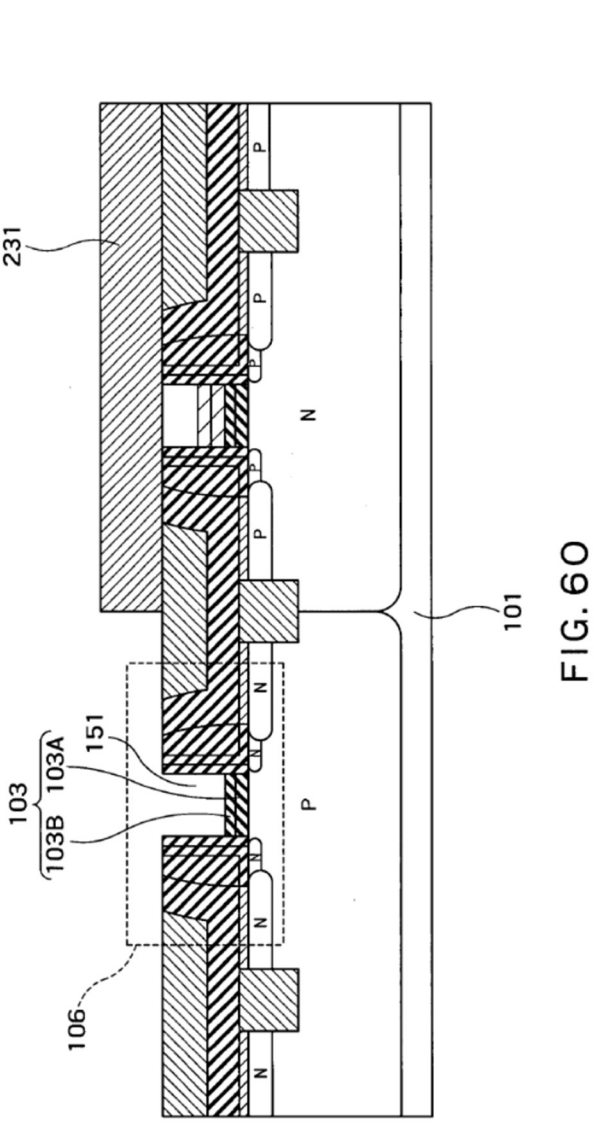
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.</p>  <p>FIG. 6I</p> <p>[0112] Next, as shown in FIG. 6J, silicide films 144 are formed in a self-aligned manner on the surfaces of the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="719 919 755 1045">FIG. 6J</p> <p data-bbox="820 226 1068 1501">[0113] Next, as shown in FIG. 6K, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 6K, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 6K, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the semiconductor layers 103C (non-diffusion layers 103Ca and diffusion layers 103Cb) are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="824 909 862 1052">FIG. 6L</p> <p data-bbox="938 193 1079 1493">[0115] Next, as shown in FIG. 6M, in the NMOSFET region 106, the semiconductor layer 103C above the gate dielectric film 102 for the NMOSFET is etched using a resist 231 as a mask and using a chemical solution such as a solution containing hydrogen peroxide. With the above-described manufacturing steps, the TiN layer 103B in the NMOSFET region 106 is exposed.</p>

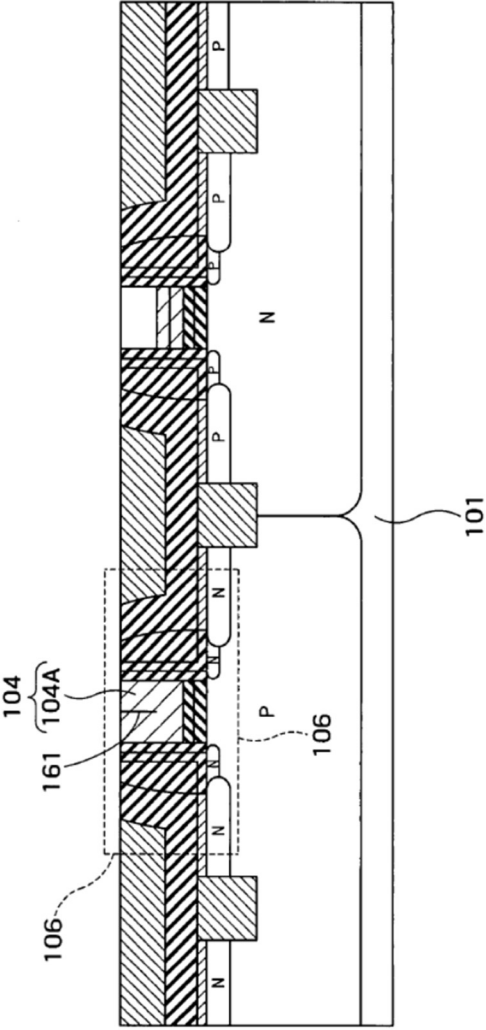
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<div data-bbox="272 451 797 1465"> </div> <p data-bbox="824 888 862 1035">FIG. 6M</p> <p data-bbox="927 220 1073 1501">[0116] Next, as shown in FIG. 6N, in the NMOSFET region 106, the TiN layer 103B above the gate dielectric film 102 for the NMOSFET is etched using the resist 231 as a mask and using a chemical solution such as a solution containing hydrogen peroxide. With the above-described manufacturing step, the W layer 103A in the NMOSFET region 106 is exposed.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="828 871 868 1029">FIG. 6N</p> <p data-bbox="933 210 1177 1501">[0117] Next, as shown in FIG. 6O, in the NMOSFET region 106, the W layer 103A on the gate dielectric film 102 for the NMOSFET is etched using the resist 231 as a mask and using a chemical solution such as a solution containing hydrogen peroxide. With the above-described manufacturing step, the hafnium silicon oxynitride film 102B in the NMOSFET region 106 is exposed. Through the above-described manufacturing steps, in the NMOSFET region 106, the dummy gate electrode 103 on the gate dielectric film 102 is removed, thereby forming a trench 151 on the gate dielectric film 102.</p>

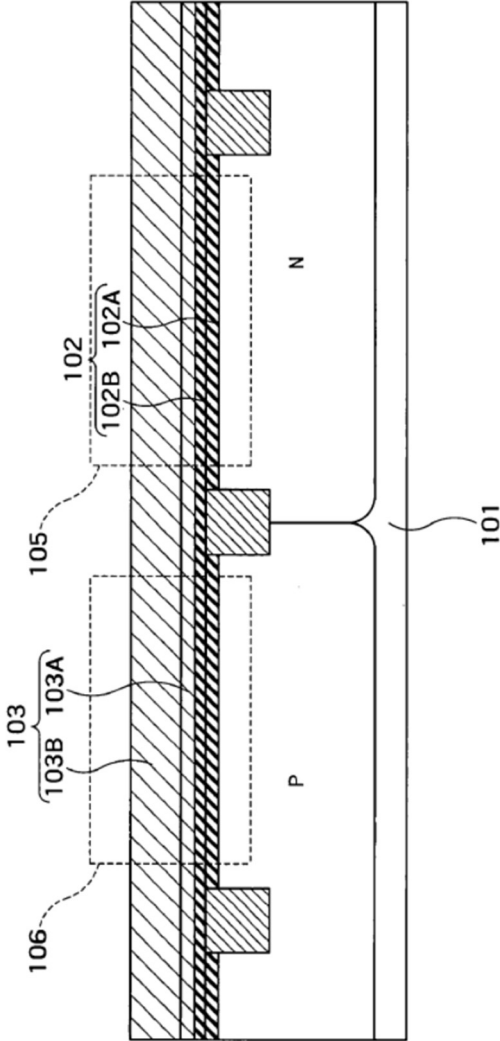
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		 <p data-bbox="824 886 862 1024">FIG. 60</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<div data-bbox="269 449 812 1472"> </div> <div data-bbox="841 892 878 1037"> <p>FIG. 6P</p> </div> <div data-bbox="927 191 1252 1499"> <p>[0119] Next, as shown in FIG. 6Q, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback). Through the above-described manufacturing steps, in the NMOSFET region 106, the material for forming the gate electrode is buried in the trench 151 on the gate dielectric film 102, thereby forming the gate electrode 104 for the NMOSFET with a different configuration from that of the gate electrode 103 for the PMOSFET. Since the gate electrode 104 for the NMOSFET (the third conductive layer 104A) is formed in the hole by CVD, a trace of a streaky seam 161 which does not remain in the gate electrode 103 for the PMOSFET (the first conductive layer 103A, second conductive layer 103B, and semiconductor layer 103C) remains in the gate electrode 104 for the NMOSFET.</p> </div>

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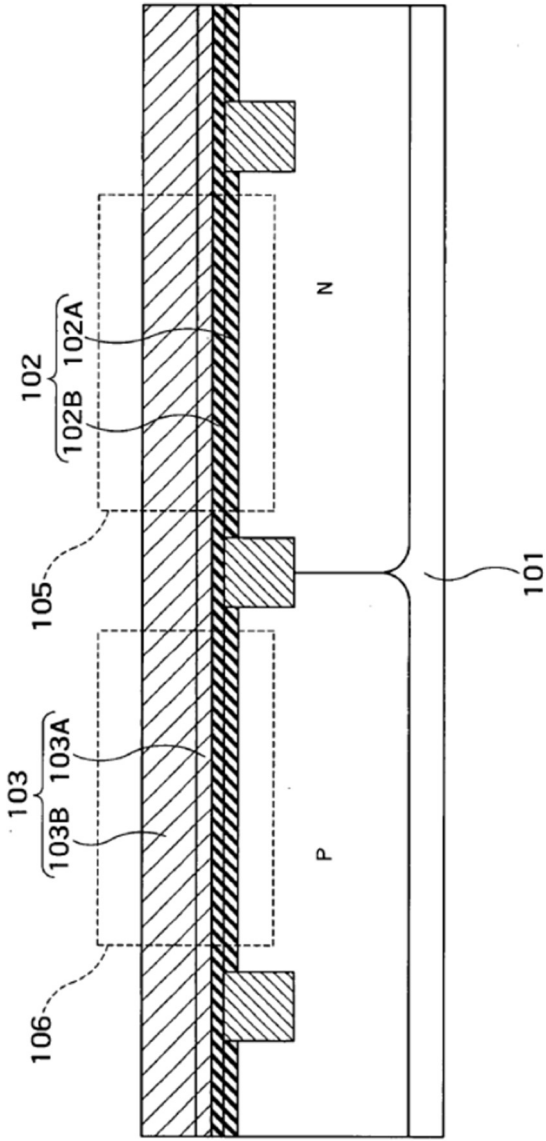
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
27	The semiconductor device of claim 25, wherein the first and second metal films have different work functions.	 <p data-bbox="792 890 824 1037">FIG. 6Q</p> <p data-bbox="878 218 1057 1499">[0121] In the third embodiment, the gate electrode 103 for the PMOSFET includes the first conductive layer 103A made of the conductive metal, the second conductive layer 103B made of the conductive metal, and the semiconductor layer (silicide layer) 103C made of the semiconductor (silicide). For this reason, in the third embodiment, the gate resistance of the PMOSFET is relatively low.</p>
		<p data-bbox="1097 264 1162 1499">Aoyama, as evidenced by the example citations below, discloses the first and second metal films have different work functions.</p> <p data-bbox="1203 205 1414 1499">[0009] For this reason, there has been proposed a method, suppressing a shift in the threshold voltage of a PMOSFET and increasing the inversion capacitance of the PMOSFET, by adopting a metal gate electrode as a gate electrode of a CMOSFET when a high-permittivity gate dielectric film is adopted as a gate dielectric film of the CMOSFET. The term “metal” in metal gate electrode refers to a simple substance metal, an alloy, and a compound including such a metal or alloy (e.g., a silicide, siliconitride, nitride, carbide, or carbonitride). If a metal gate electrode is adopted as the gate</p>

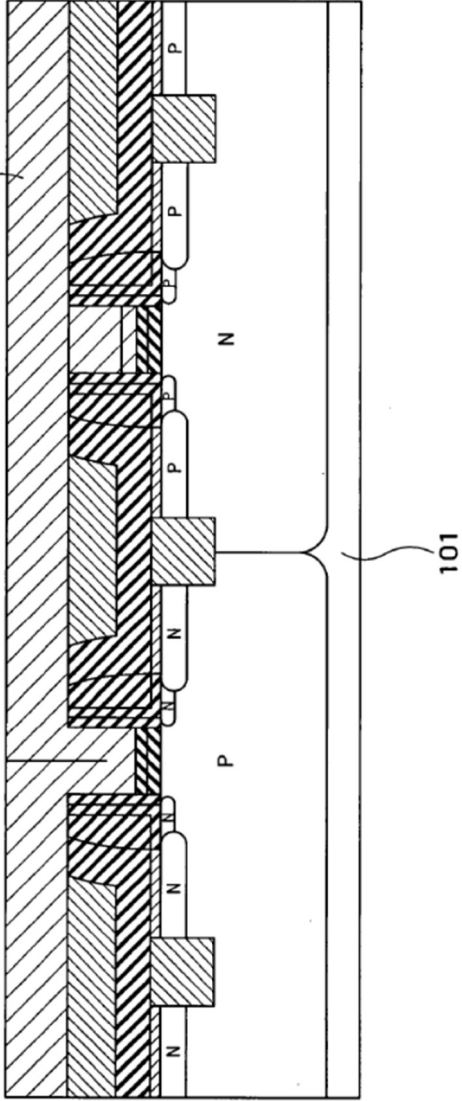
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>electrode of a PMOSFET, the following things can be ensured. Firstly, since the threshold voltage changes according to the work function of the metal used, an appropriate threshold voltage can be ensured by using a metal with an appropriate work function. Secondly, since depletion is less likely to occur in a metal than in polysilicon, a sufficient inversion capacitance can be ensured.</p> <p>[0010] A metal suitable for the metal gate electrode of a PMOSFET is a metal with a work function of 4.8 eV or more, and a metal suitable for the metal gate electrode of an NMOSFET is a metal with a work function of 4.3 eV or less. Adoption of such metals for the metal gate electrodes of a PMOSFET and an NMOSFET is preferable in terms of the design of a CMOSFET, because the work functions of the gate electrodes of the PMOSFET and the NMOSFET become same to those of conventional PMOSFET and NMOSFET. When a PMOSFET was subjected to a heat resistance test using metals such as W, Ru, and Pt with a work function of 4.8 eV or more, it turned out that it was possible to keep the work function at 4.8 eV or more even after annealing at 1,000 to 1,030° C. However, when an NMOSFET was subjected to a heat resistance test using metals such as TaSi, TaSiN, TaC, TaCN, TaSiCN, HfN, HfSi, HfSiN, WSi, TaHf, and TaHfN with a work function of 4.3 eV or less, it turned out that spike annealing at about 1,000° C. changed the work function to about 4.5 eV, and that it was impossible to keep the work function at 4.3 eV or less. Furthermore, it was impossible to measure the work function after the annealing with regard to some of the metals, so it was supposed that a reaction occurred in some of the metals. Accordingly, if a high-permittivity gate dielectric film and a metal gate electrode are adopted in a CMOSFET, it is difficult to form the CMOSFET by a forming method similar to a conventional one. This is because the work function of the metal gate electrode of an NMOSFET changes in the step of forming a source/drain diffusion layer requiring annealing at about 1,000° C.</p> <p>[0011] Therefore, there is proposed a method, forming, when a high-permittivity gate dielectric film and a metal gate electrode are adopted in a CMOSFET, a dummy gate dielectric film made of a silicon oxide film and a dummy gate electrode made of polysilicon, removing the dummy gate dielectric film and dummy gate electrode after forming a source/drain diffusion layer, and forming a real high-permittivity gate dielectric film and metal gate electrode; the method is called the “damascene gate process” (A. Chatterjee et al., IEDM Tech. Dig. 821 (1997) and A. Yagishita et al., IEDM Tech. Dig. 785 (1998)). Since, in this method, a metal gate electrode is formed after a source/drain diffusion layer is formed, the work function of the metal gate electrode of an</p>

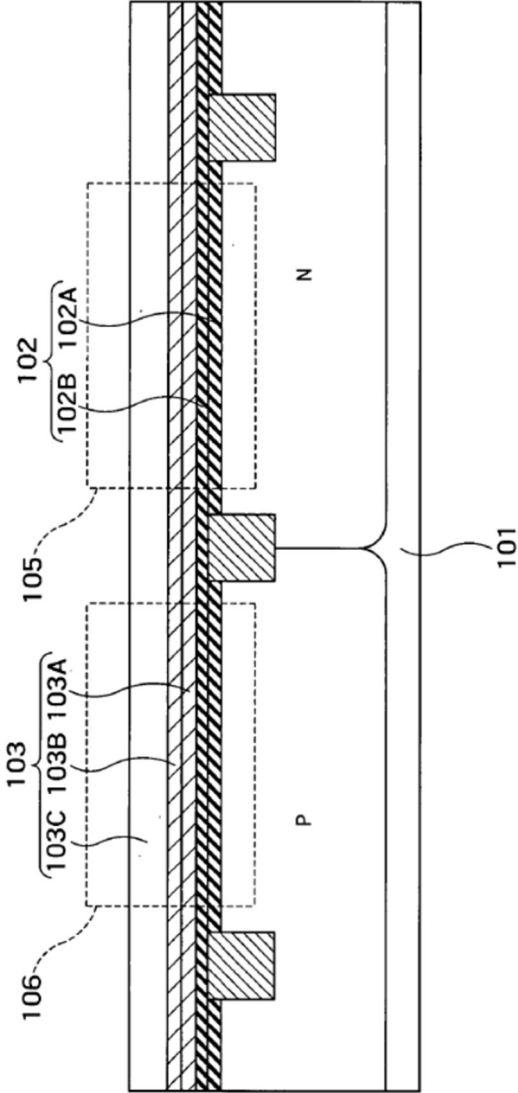
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>NMOSFET does not change in the step of forming the source/drain diffusion layer requiring annealing at about 1,000° C.</p> <p>[0049] Next, as shown in FIG. 2E, a Ru (ruthenium) layer (a first conductive layer of a gate electrode for the PMOSFET) 103A with a thickness of about 20 nm is deposited on the hafnium silicon oxynitride film 102B using bis(cyclopentadienyl)ruthenium and oxygen, and a W (tungsten) layer (a second conductive layer of the gate electrode for the PMOSFET) 103B with a thickness of about 60 nm is deposited on the Ru layer 103A using tungsten hexafluoride, silane, and hydrogen. With the above-described manufacturing steps, the gate electrode layer 103 for the PMOSFET is formed, ranging from the PMOSFET region 105 to the NMOSFET region 106, on the gate dielectric film 102.</p> <div data-bbox="722 436 1218 1470"></div> <p>FIG. 2E</p> <p>[0050] Note that although the gate electrode layer 103 for the PMOSFET of the first embodiment has a two-layer structure of the Ru layer 103A and W layer 103B, it may have a one-layer structure of</p>

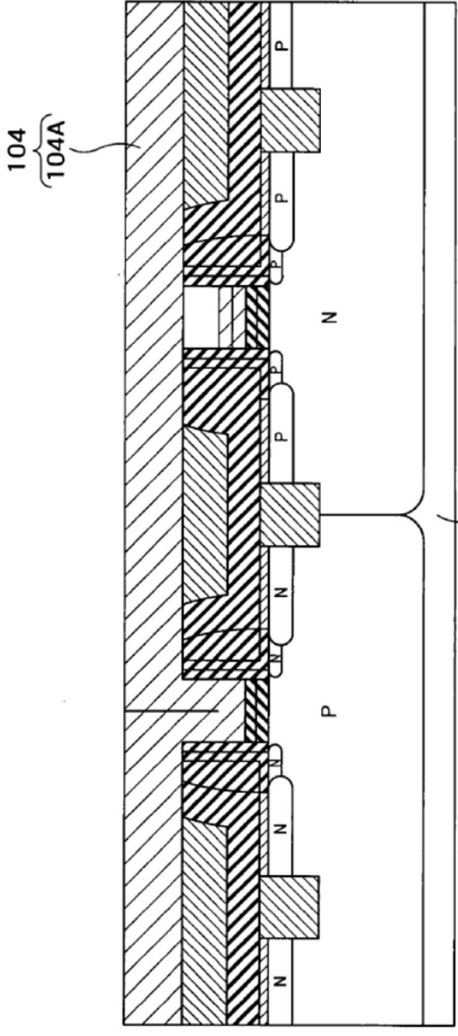
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>only a Ru layer or a laminated structure of three or more layers including a Ru layer. The two-layer structure of the gate electrode layer 103 for the PMOSFET of the first embodiment is mainly due to the thickness of the Ru layer 103A. Since Ru has not only advantages such as a high work function but also disadvantages such as costliness, the thickness of the Ru layer 103A is made small in the first embodiment. For this reason, in the first embodiment, migration and even agglomeration may occur in the Ru layer 103A, for example, at the time of activation of the source/drain diffusion layer due to the tension of the Ru layer 103A itself. To prevent these phenomena, the gate electrode layer 103 for the PMOSFET is configured to have a two-layer structure in the first embodiment.</p> <p>[0059] Next, as shown in FIG. 2M, conductive metal, which is a material for forming a third conductive layer 104A of the gate electrode 104 for the NMOSFET, is deposited over the entire surface by CVD. Examples of the conductive metal include TaSiN which is formed using pentakis(ethylmethylamino)tantalum, disilane, and ammonia, HfN which is formed in an atmosphere containing tetrakis(ethylmethylamino)hafnium and ammonia, HfSi which is formed using tetrakis(ethylmethylamino)hafnium and tetrakis(ethylmethylamino)silicon, and WSi which is formed using tungsten hexafluoride and dichlorosilane.</p>

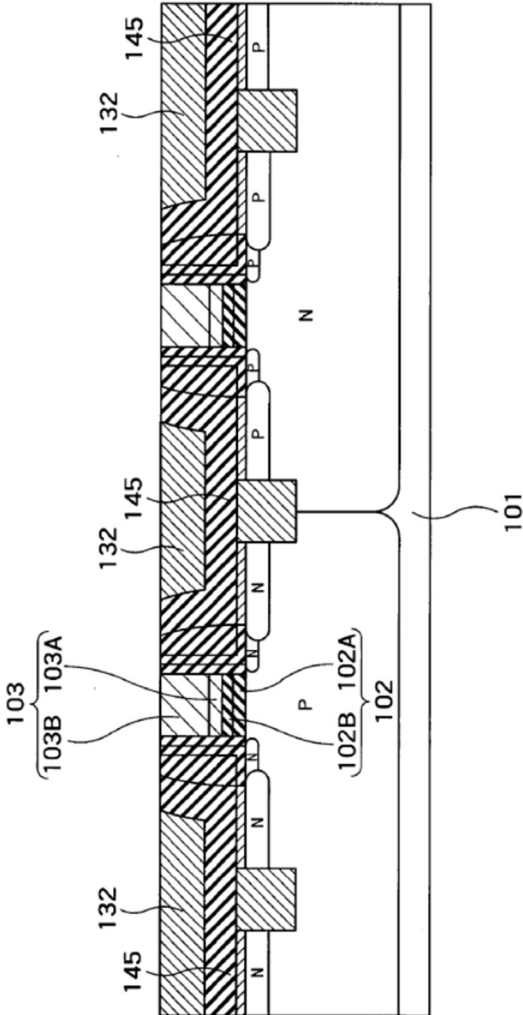
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. No. 2007/0215950 to Aoyama
		<div data-bbox="272 409 841 1480"> </div> <div data-bbox="873 871 914 1024"> <p>FIG. 2M</p> </div> <div data-bbox="976 210 1406 1501"> <p>[0060] Note that although the gate electrode 104 for the NMOSFET of the first embodiment has a one-layer structure of only the conductive layer 104A made of the conductive metal, it may have a laminated structure of two or more layers including a conductive layer made of conductive metal.</p> <p>[0069] Although, in this embodiment, a hafnium silicon oxynitride film is adopted as a high-permittivity dielectric film to form each gate dielectric film 102, any other high-permittivity dielectric film may be adopted. Although, in this embodiment, the Ru layer and W layer are adopted as metal electrode layers to form the gate electrode 103 for the PMOSFET, any other metal electrode layers may be adopted. For example, a W layer, Ru layer, or Pt layer may be adopted as a metal electrode layer to form the gate electrode 103 for the PMOSFET. Although, in this embodiment, a TaSiN layer, HfN layer, and WSi layer are described as examples of metal electrode layers to form the gate electrode 104 for the NMOSFET, any other metal electrode layers may be adopted. It is</p> </div>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>possible to adopt, for example, a TaSi layer, TaSiN layer, TaC layer, TaCN layer, TaSiCN layer, HfN layer, HfSi layer, HfSiN layer, WSi layer, TaHf layer, or TaHfN layer as a metal electrode layer to form the gate electrode 104 for the NMOSFET.</p> <p>[0082] Next, as shown in FIG. 4E, a W (tungsten) layer (a first conductive layer of a gate electrode for the PMOSFET) 103A with a thickness of about 20 nm is deposited on the hafnium silicon oxynitride film 102B by thermal CVD using tungsten hexacarbonyl or plasma CVD using tungsten hexacarbonyl and hydrogen, and a TiN (titanium nitride) layer (a second conductive layer of the gate electrode for the PMOSFET) 103B with a thickness of about 60 nm is deposited on the W layer 103A using titanium tetrachloride and ammonia. With the above-described manufacturing steps, the gate electrode layer 103 for the PMOSFET is formed, ranging from the PMOSFET region 105 to the NMOSFET region 106, on the gate dielectric film 102.</p>  <p style="text-align: center;">FIG. 4E</p>

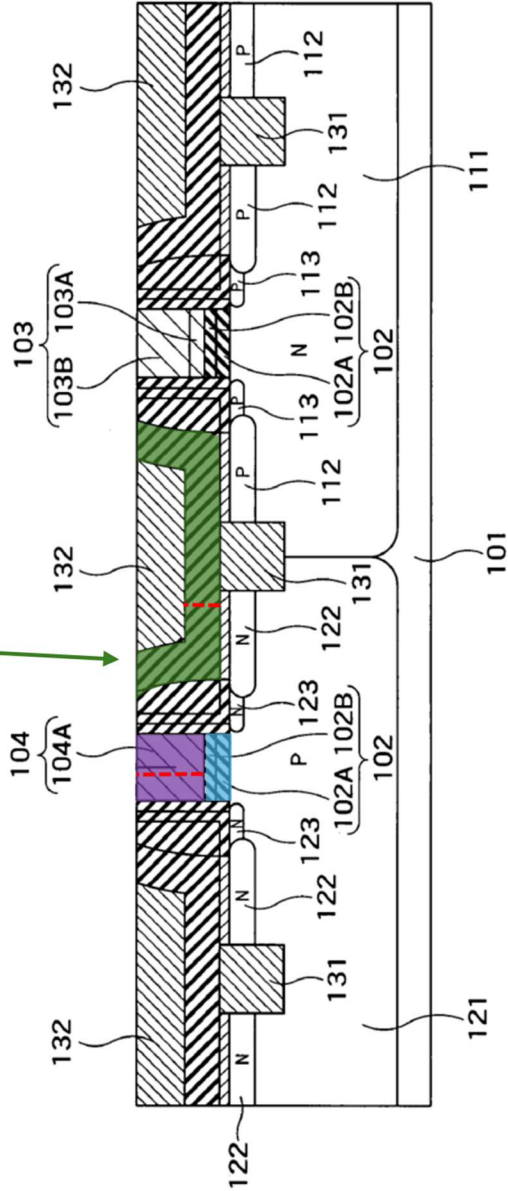
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>[0083] Note that although the gate electrode layer 103 for the PMOSFET of the second embodiment has a two-layer structure of the W layer 103A and TiN layer 103B, it may have a one-layer structure of only a W layer or a laminated structure of three or more layers including a W layer. If the gate electrode layer 103 for the PMOSFET has a one-layer structure of only a W layer, it is desirable to reduce the thickness of the W layer to 60 nm or less because the W layer is likely to peel off.</p> <p>[0091] Next, as shown in FIG. 4M, conductive metal, which is a material for forming a third conductive layer 104A of the gate electrode 104 for the NMOSFET, is deposited over the entire surface by CVD. Examples of the conductive metal include TaC, which is formed using pentakis(dimethylamino)tantalum and methane.</p>  <p style="text-align: center;">FIG. 4M</p>

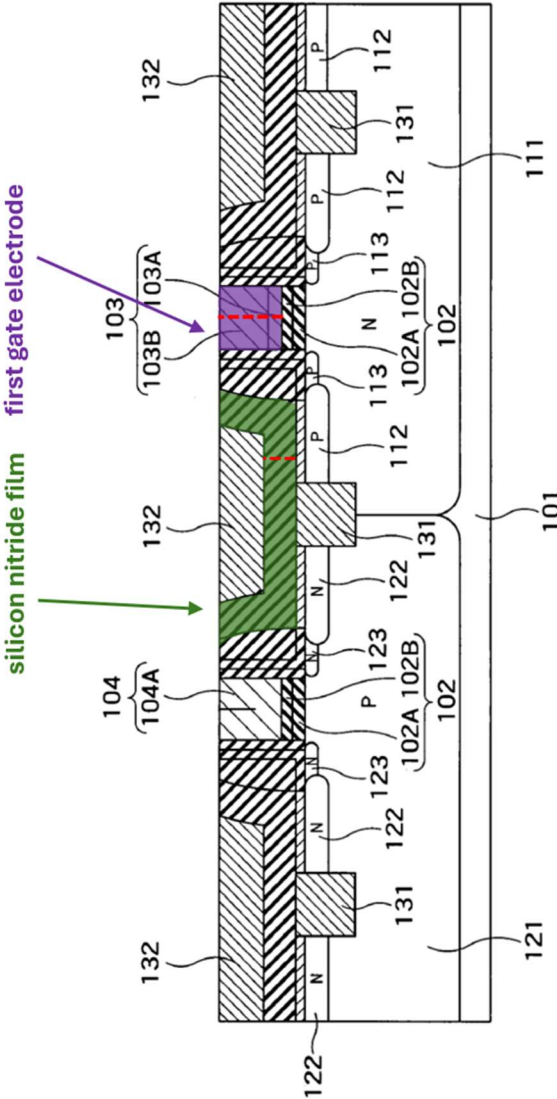
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>[0092] Note that although the gate electrode 104 for the NMOSFET of the second embodiment has a one-layer structure of only the conductive layer 104A made of the conductive metal, it may have a laminated structure of two or more layers including a conductive layer made of conductive metal.</p> <p>[0107] Next, as shown in FIG. 6E, a W (tungsten) layer (a first conductive layer of a gate electrode for the PMOSFET) 103A with a thickness of about 20 nm is deposited on the hafnium silicon oxynitride film 102B by thermal CVD using tungsten hexacarbonyl or plasma CVD using tungsten hexacarbonyl and hydrogen, a TiN (titanium nitride) layer (a second conductive layer of the gate electrode for the PMOSFET) 103B with a thickness of about 60 nm is deposited on the W layer 103A using diethylaminotitanium and ammonia, and a semiconductor layer 103C made of polysilicon or amorphous silicon is deposited on the TiN (titanium nitride) layer 103B. With the above-described manufacturing steps, the gate electrode 103 for the PMOSFET is formed, ranging from the PMOSFET region 105 to the NMOSFET region 106, on the gate dielectric film 102.</p>  <p style="text-align: center;">FIG. 6E</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>[0118] Next, as shown in FIG. 6P, conductive metal, which is a material for forming a third conductive layer 104A of the gate electrode 104 for the NMOSFET, is formed over the entire surface by CVD. Examples of the conductive metal include TaCN, which is formed using tris-dimethylamino-mono-t-amyyliminotantalum and monomethylamine.</p>  <p style="text-align: center;">FIG. 6P</p>
28	The semiconductor device of claim 25, wherein the silicon nitride film has a thickness smaller than that of the first gate electrode.	<p>Aoyama, as evidenced by the example citations below, discloses the silicon nitride film has a thickness smaller than that of the first gate electrode.</p> <p>[0056] Next, as shown in FIG. 2J, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 2J, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 2J, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching).</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>With the above-described manufacturing steps, the W layers 103B are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>  <p style="text-align: center;">FIG. 2J</p> <p>[0088] Next, as shown in FIG. 4J, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 4J, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 4J, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the TiN layers 103B are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<div data-bbox="267 438 797 1476"> </div> <p data-bbox="829 900 865 1035">FIG. 4J</p> <p data-bbox="915 228 1167 1499">[0113] Next, as shown in FIG. 6K, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 6K, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 6K, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the semiconductor layers 103C (non-diffusion layers 103Ca and diffusion layers 103Cb) are exposed both in the PMOSFET region 105 and the NMOSFET region 106.</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p data-bbox="256 772 285 1014">silicon nitride film</p>  <p data-bbox="922 785 959 905">FIG. 1</p> <p data-bbox="932 1062 959 1308">first MIS transistor</p>

Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
31	The semiconductor device of claim 25, wherein the first and second gate insulating films are made of the same insulating material.	 <p>FIG. 1 first MIS transistor</p> <p>Aoyama, as evidenced by the example citations below, discloses the first and second gate insulating films are made of the same insulating material.</p> <p>[0039] The semiconductor device shown in FIG. 1 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a</p>

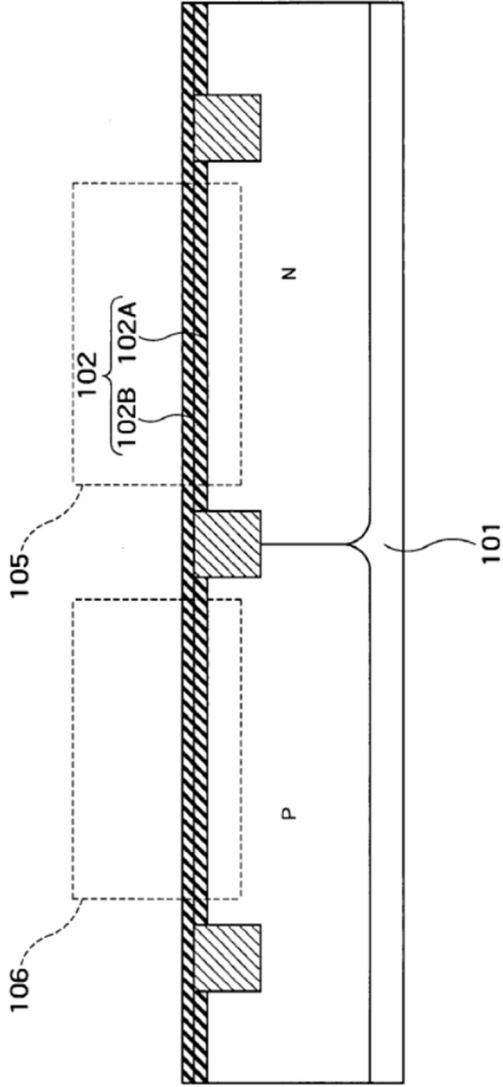
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer 103A which is made of conductive metal and a second conductive layer 103B which is made of conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p> <p>[0047] Next, as shown in FIG. 2D, the dielectric film 201 is removed from the substrate 101 using an ammonium fluoride aqueous solution, and the surface of the substrate 101 is cleaned using 0.5 to 5.0% hydrofluoric acid. Then, as shown in FIG. 2D, a silicon oxide film (a first dielectric film of a gate dielectric film) 102A with a thickness of 0.5 to 0.8 nm is formed on the substrate 101 in an atmosphere containing oxygen, and a hafnium silicate film (a second dielectric film of the gate dielectric film) 102B with a thickness of about 2.0 nm is formed on the silicon oxide film 102A using tetrakis(diethylamino)hafnium, tetrakis(dimethylamino)silicon, and oxygen. After that, the substrate 101 is subjected to annealing at 600° C., thereby densifying the silicon oxide film 102A and hafnium silicate film 102B. After that, the substrate 101 is processed in a nitrogen plasma atmosphere or ammonia atmosphere and then subjected to annealing at 1,000° C., thereby reforming the hafnium silicate film 102B into a hafnium silicon oxynitride film 102B. With the above-described manufacturing steps, the gate dielectric film 102 common to the PMOSFET and the NMOSFET is formed, ranging from a PMOSFET region 105 to a NMOSFET region 106, on the substrate 101. The PMOSFET region 105 is a region where the PMOSFET is to be formed, which is a specific example of a P-type FET region, and the NMOSFET region 106 is a region where the NMOSFET is to be formed, which is a specific example of an N-type FET region.</p>

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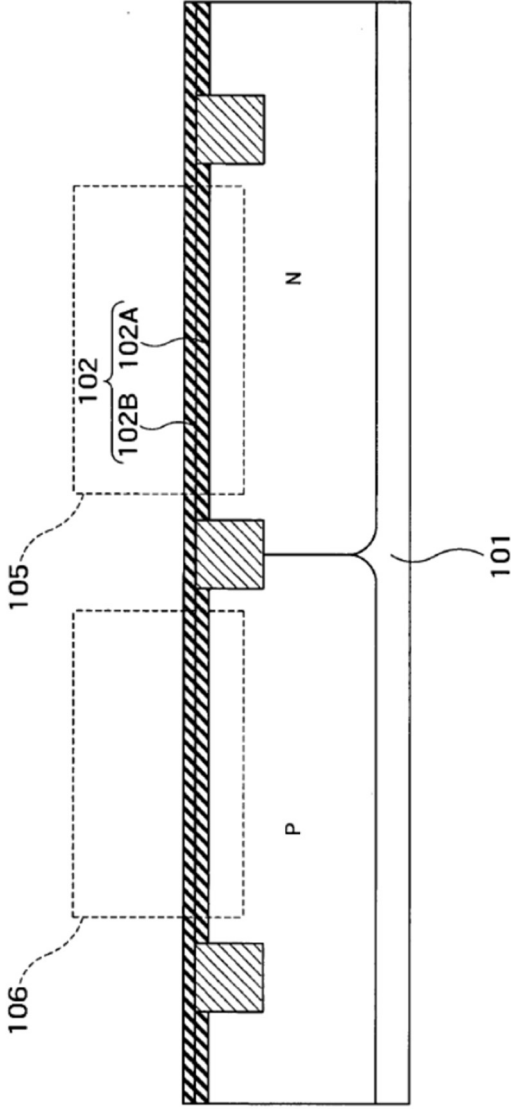
<p>Claim</p>		<p>Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama</p>
		<div data-bbox="339 405 795 1005"> </div> <div data-bbox="807 869 844 1041"> <p>FIG. 2D</p> </div> <div data-bbox="906 197 1053 1505"> <p>[0048] Note that although the gate dielectric film 102 of the first embodiment has a two-layer structure of the silicon oxide film 102A and hafnium silicon oxynitride film 102B, it may have a one-layer structure of only a hafnium silicon oxynitride film or a laminated structure of three or more layers including a hafnium silicon oxynitride film.</p> </div> <div data-bbox="1078 197 1409 1505"> <p>[0069] Although, in this embodiment, a hafnium silicon oxynitride film is adopted as a high-permittivity dielectric film to form each gate dielectric film 102, any other high-permittivity dielectric film may be adopted. Although, in this embodiment, the Ru layer and W layer are adopted as metal electrode layers to form the gate electrode 103 for the PMOSFET, any other metal electrode layers may be adopted. For example, a W layer, Ru layer, or Pt layer may be adopted as a metal electrode layer to form the gate electrode 103 for the PMOSFET. Although, in this embodiment, a TaSiN layer, HfN layer, and W/Si layer are described as examples of metal electrode layers to form the gate electrode 104 for the NMOSFET, any other metal electrode layers may be adopted. It is possible to adopt, for example, a TaSi layer, TaSiN layer, TaC layer, TaCN layer, TaSiCN layer, HfN</p> </div>

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Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>layer, HfSi layer, HfSiN layer, WSi layer, TaHf layer, or TaHfN layer as a metal electrode layer to form the gate electrode 104 for the NMOSFET.</p> <p>[0072] The semiconductor device shown in FIG. 3 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer 103A which is made of conductive metal and a second conductive layer 103B which is made of conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p> <p>[0080] Next, as shown in FIG. 4D, the dielectric film 201 is removed from the substrate 101 using an ammonia fluoride aqueous solution, and the surface of the substrate 101 is cleaned using 0.5 to 5.0% hydrofluoric acid. Then, as shown in FIG. 4D, a silicon oxide film (a first dielectric film of a gate dielectric film) 102A with a thickness of 0.5 to 0.8 nm is formed on the substrate 101 in an atmosphere containing oxygen, and a hafnium silicate film (a second dielectric film of the gate dielectric film) 102B with a thickness of about 2.0 nm is formed on the silicon oxide film 102A using tetrakis(diethylamino)hafnium, tetrakis(dimethylamino)silicon, and oxygen. After that, the substrate 101 is subjected to annealing at 600° C., thereby densifying the silicon oxide film 102A and hafnium silicate film 102B. After that, the substrate 101 is processed in a nitrogen plasma atmosphere or ammonia atmosphere and then subjected to annealing at 1,000° C., thereby reforming the hafnium silicate film 102B into a hafnium silicon oxynitride film 102B. With the above-described manufacturing steps, the gate dielectric film 102 common to the PMOSFET and NMOSFET is formed, ranging from a PMOSFET region 105 to a NMOSFET region 106, on the substrate 101. The</p>

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		<p>PMOSFET region 105 is a region where the PMOSFET is to be formed, which is a specific example of a P-type FET region, and the NMOSFET region 106 is a region where the NMOSFET is to be formed, which is a specific example of an N-type FET region.</p>  <p style="text-align: center;">FIG. 4D</p> <p>[0081] Note that although the gate dielectric film 102 of the second embodiment has a two-layer structure of the silicon oxide film 102A and hafnium silicon oxynitride film 102B, it may have a one-layer structure of only a hafnium silicon oxynitride film or a laminated structure of three or more layers including a hafnium silicon oxynitride film.</p> <p>[0098] The semiconductor device shown in FIG. 5 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of</p>

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		<p>dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes three electrode-constituting layers: a first conductive layer 103A which is made of conductive metal, a second conductive layer 103B which is made of conductive metal, and a semiconductor layer 103C which is made of semiconductor. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p> <p>[0106] Next, as shown in FIG. 6D, the dielectric film 201 is removed from the substrate 101 using an ammonium fluoride aqueous solution, and the surface of the substrate 101 is cleaned using 0.5 to 5.0% hydrofluoric acid. Then, as shown in FIG. 6D, a silicon oxide film (a first dielectric film of a gate dielectric film) 102A with a thickness of 0.5 to 0.8 nm is formed on the substrate 101 in an atmosphere containing oxygen, and a hafnium silicate film (a second dielectric film of the gate dielectric film) 102B with a thickness of about 2.0 nm is formed on the silicon oxide film 102A using tetrakis(diethylamino)hafnium, tetrakis(dimethylamino)silicon, and oxygen. After that, the substrate 101 is subjected to annealing at 600° C., thereby densifying the silicon oxide film 102A and hafnium silicate film 102B. After that, the substrate 101 is processed in a nitrogen plasma atmosphere or ammonia atmosphere and then subjected to annealing at 1,000° C., thereby reforming the hafnium silicate film 102B into a hafnium silicon oxynitride film 102B. With the above-described manufacturing steps, the gate dielectric film 102 common to the PMOSFET and NMOSFET is formed, ranging from a PMOSFET region 105 to a NMOSFET region 106, on the substrate 101. The PMOSFET region 105 is a region where the PMOSFET is to be formed, which is a specific example of a P-type FET region, and the NMOSFET region 106 is a region where the NMOSFET is to be formed, which is a specific example of an N-type FET region.</p>

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35	The semiconductor device of claim 25, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.	 <p style="text-align: center;">FIG. 6D</p> <p>Aoyama, as evidenced by the example citations below, discloses the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.</p> <p>[0039] The semiconductor device shown in FIG. 1 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer 103A which is made of conductive metal and a second conductive layer 103B which is made of</p>

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		<p>conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p> <p>[0047] Next, as shown in FIG. 2D, the dielectric film 201 is removed from the substrate 101 using an ammonium fluoride aqueous solution, and the surface of the substrate 101 is cleaned using 0.5 to 5.0% hydrofluoric acid. Then, as shown in FIG. 2D, a silicon oxide film (a first dielectric film of a gate dielectric film) 102A with a thickness of 0.5 to 0.8 nm is formed on the substrate 101 in an atmosphere containing oxygen, and a hafnium silicate film (a second dielectric film of the gate dielectric film) 102B with a thickness of about 2.0 nm is formed on the silicon oxide film 102A using tetrakis(diethylamino)hafnium, tetrakis(dimethylamino)silicon, and oxygen. After that, the substrate 101 is subjected to annealing at 600° C., thereby densifying the silicon oxide film 102A and hafnium silicate film 102B. After that, the substrate 101 is processed in a nitrogen plasma atmosphere or ammonia atmosphere and then subjected to annealing at 1,000° C., thereby reforming the hafnium silicate film 102B into a hafnium silicon oxynitride film 102B. With the above-described manufacturing steps, the gate dielectric film 102 common to the PMOSFET and the NMOSFET is formed, ranging from a PMOSFET region 105 to a NMOSFET region 106, on the substrate 101. The PMOSFET region 105 is a region where the PMOSFET is to be formed, which is a specific example of a P-type FET region, and the NMOSFET region 106 is a region where the NMOSFET is to be formed, which is a specific example of an N-type FET region.</p>

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		<div data-bbox="282 426 771 1486"> </div> <p data-bbox="803 884 841 1031">FIG. 2D</p> <p data-bbox="911 191 1052 1499">[0048] Note that although the gate dielectric film 102 of the first embodiment has a two-layer structure of the silicon oxide film 102A and hafnium silicon oxynitride film 102B, it may have a one-layer structure of only a hafnium silicon oxynitride film or a laminated structure of three or more layers including a hafnium silicon oxynitride film.</p> <p data-bbox="1089 191 1409 1499">[0069] Although, in this embodiment, a hafnium silicon oxynitride film is adopted as a high-permittivity dielectric film to form each gate dielectric film 102, any other high-permittivity dielectric film may be adopted. Although, in this embodiment, the Ru layer and W layer are adopted as metal electrode layers to form the gate electrode 103 for the PMOSFET, any other metal electrode layers may be adopted. For example, a W layer, Ru layer, or Pt layer may be adopted as a metal electrode layer to form the gate electrode 103 for the PMOSFET. Although, in this embodiment, a TaSiN layer, HfN layer, and WSi layer are described as examples of metal electrode layers to form the gate electrode 104 for the NMOSFET, any other metal electrode layers may be adopted. It is possible to adopt, for example, a TaSi layer, TaSiN layer, TaC layer, TaSiCN layer, HfN</p>

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		<p>layer, HfSi layer, HfSiN layer, WSi layer, TaHf layer, or TaHfN layer as a metal electrode layer to form the gate electrode 104 for the NMOSFET.</p> <p>[0072] The semiconductor device shown in FIG. 3 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes two electrode-constituting layers: a first conductive layer 103A which is made of conductive metal and a second conductive layer 103B which is made of conductive metal. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p> <p>[0080] Next, as shown in FIG. 4D, the dielectric film 201 is removed from the substrate 101 using an ammonia fluoride aqueous solution, and the surface of the substrate 101 is cleaned using 0.5 to 5.0% hydrofluoric acid. Then, as shown in FIG. 4D, a silicon oxide film (a first dielectric film of a gate dielectric film) 102A with a thickness of 0.5 to 0.8 nm is formed on the substrate 101 in an atmosphere containing oxygen, and a hafnium silicate film (a second dielectric film of the gate dielectric film) 102B with a thickness of about 2.0 nm is formed on the silicon oxide film 102A using tetrakis(diethylamino)hafnium, tetrakis(dimethylamino)silicon, and oxygen. After that, the substrate 101 is subjected to annealing at 600° C., thereby densifying the silicon oxide film 102A and hafnium silicate film 102B. After that, the substrate 101 is processed in a nitrogen plasma atmosphere or ammonia atmosphere and then subjected to annealing at 1,000° C., thereby reforming the hafnium silicate film 102B into a hafnium silicon oxynitride film 102B. With the above-described manufacturing steps, the gate dielectric film 102 common to the PMOSFET and NMOSFET is formed, ranging from a PMOSFET region 105 to a NMOSFET region 106, on the substrate 101. The</p>

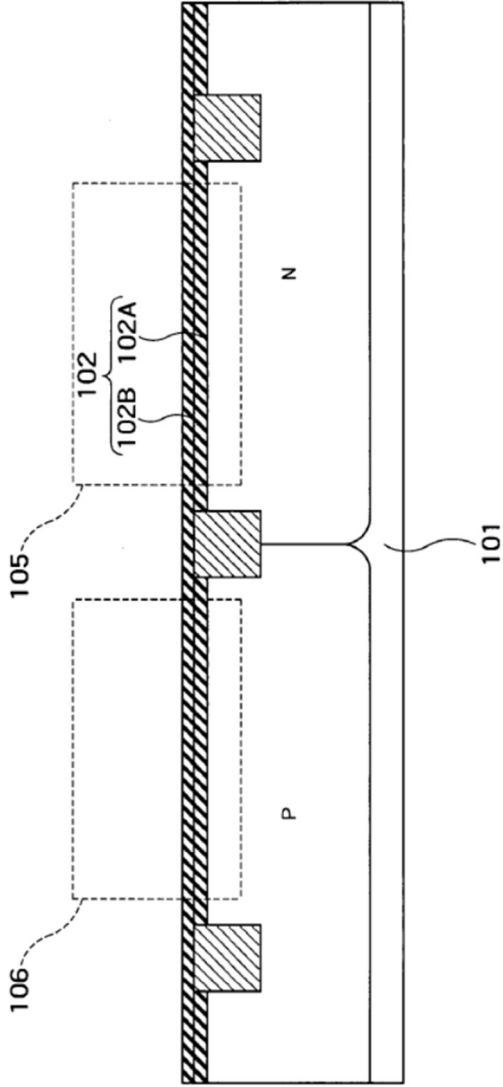
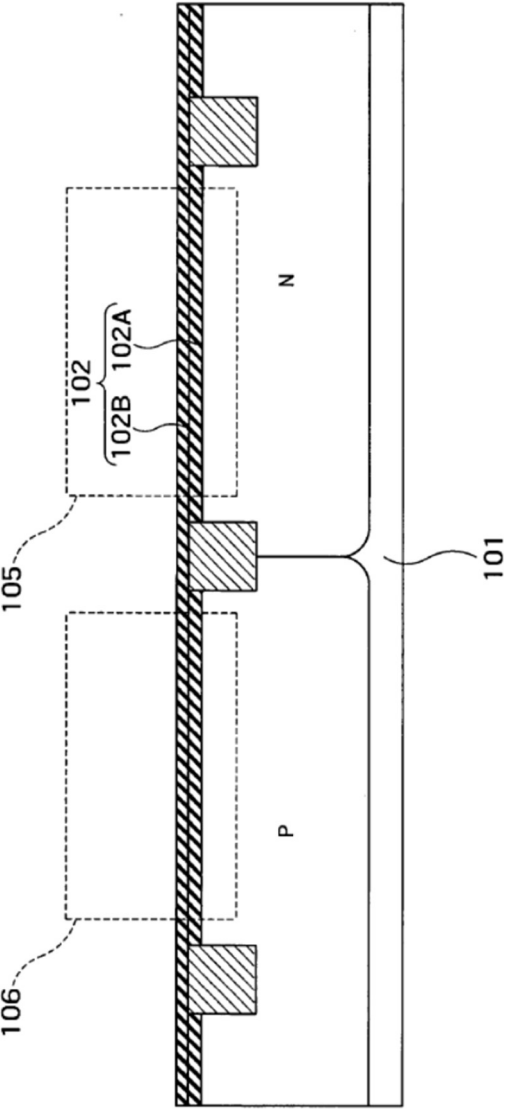
Claim	Claim Language	Exemplary Disclosures in U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama
		<p>PMOSFET region 105 is a region where the PMOSFET is to be formed, which is a specific example of a P-type FET region, and the NMOSFET region 106 is a region where the NMOSFET is to be formed, which is a specific example of an N-type FET region.</p>  <p>[0081] Note that although the gate dielectric film 102 of the second embodiment has a two-layer structure of the silicon oxide film 102A and hafnium silicon oxynitride film 102B, it may have a one-layer structure of only a hafnium silicon oxynitride film or a laminated structure of three or more layers including a hafnium silicon oxynitride film.</p> <p>[0098] The semiconductor device shown in FIG. 5 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of</p>

FIG. 4D

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		<p>dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film. The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes three electrode-constituting layers: a first conductive layer 103A which is made of conductive metal, a second conductive layer 103B which is made of conductive metal, and a semiconductor layer 103C which is made of semiconductor. The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.</p> <p>[0106] Next, as shown in FIG. 6D, the dielectric film 201 is removed from the substrate 101 using an ammonium fluoride aqueous solution, and the surface of the substrate 101 is cleaned using 0.5 to 5.0% hydrofluoric acid. Then, as shown in FIG. 6D, a silicon oxide film (a first dielectric film of a gate dielectric film) 102A with a thickness of 0.5 to 0.8 nm is formed on the substrate 101 in an atmosphere containing oxygen, and a hafnium silicate film (a second dielectric film of the gate dielectric film) 102B with a thickness of about 2.0 nm is formed on the silicon oxide film 102A using tetrakis(diethylamino)hafnium, tetrakis(dimethylamino)silicon, and oxygen. After that, the substrate 101 is subjected to annealing at 600° C., thereby densifying the silicon oxide film 102A and hafnium silicate film 102B. After that, the substrate 101 is processed in a nitrogen plasma atmosphere or ammonia atmosphere and then subjected to annealing at 1,000° C., thereby reforming the hafnium silicate film 102B into a hafnium silicon oxynitride film 102B. With the above-described manufacturing steps, the gate dielectric film 102 common to the PMOSFET and NMOSFET is formed, ranging from a PMOSFET region 105 to a NMOSFET region 106, on the substrate 101. The PMOSFET region 105 is a region where the PMOSFET is to be formed, which is a specific example of a P-type FET region, and the NMOSFET region 106 is a region where the NMOSFET is to be formed, which is a specific example of an N-type FET region.</p>

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		 <p>FIG. 6D</p>