UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner,

v.

Advanced Integrated Circuit Process LLC,

Patent Owner.

Patent No. 8,198,686 B2
Filing Date: December 2, 2009
Issue Date: June 12, 2012

Title: SEMICONDUCTOR DEVICE

Inter Partes Review No. IPR2025-00682

PETITION FOR *INTER PARTES* REVIEW

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Statutes

35 U.S.C. § 102(a), (b), (e) 1, 11, 12, 13, 15

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TABLE OF EXHIBITS

Exhibit	Description
Ex-1001	U.S. Patent No. 8,198,686 B2 to Sato et al. ("'686 Patent").
Ex-1002	Prosecution History of the '686 Patent ("Prosecution History").
Ex-1003	Declaration of Dr. Scott E. Thompson, Ph.D.
Ex-1004	Curriculum Vitae of Dr. Scott E. Thompson, Ph.D.
Ex-1005	U.S. Pat. Pub. No. 2007/0215950 A1 to Aoyama ("Aoyama").
Ex-1006	U.S. Pat. Pub. No. 2007/0235823 A1 to Hsu et al. ("Hsu823").
Ex-1007	U.S. Patent No. 6,171,910 B2 to Hobbs et al. ("Hobbs").
Ex-1008	U.S. Pat. Pub. No. 2007/0066077 A1 to Akasaka et al. ("Akasaka").
Ex-1009	S.M. Sze, *Physics of Semiconductor Devices* (2d ed. 1981) (excerpted).
Ex-1010	J.D. Plummer et al., *Silicon VLSI Technology: Fundamentals, Practice and Modeling* (2000) (excerpted).
Ex-1011	M. Baklanov et al., *Dielectric Films for Advanced Microelectronics* (2007) (excerpted).
Ex-1012	International Technology Roadmap for Semiconductors: Front End Processes (2007 ed.).
Ex-1013	International Technology Roadmap for Semiconductors: Process Integration, Devices, and Structures (2007 ed.).

Exhibit	Description
Ex-1014	U.S. Pat. Pub. No. 2006/0081939 A1 to Akasaka et al.
Ex-1015	U.S. Pat. Pub. No. 2006/0022277 A1 to Kavalieros et al.
Ex-1016	K. Mistry, et al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging," Technical Digest of the of the 2007 IEEE International Electron Devices Meeting (IEDM), pp. 247-50 (Dec. 2007).
Ex-1017	K. Mistry, et al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging," presented at 2007 IEEE International Electron Devices Meeting (IEDM), pp. 1-37 (Dec. 2007).
Ex-1018	U.S. Patent No. 6,881,631 B2 to Saito et al.
Ex-1019	U.S. Patent No. 7,812,414 B2 to Hou et al.
Ex-1020	U.S. Pat. Pub. No. 2005/0258468 A1 to Colombo et al.
Ex-1021	U.S. Patent No. 6,849,511 B2 to Iriyama et al.
Ex-1022	U.S. Pat. Pub. No. 2002/0037615 A1 to Matsuo.
Ex-1023	S.E. Thompson et al., "A 90-nm Logic Technology Featuring Strained Silicon," IEEE Transactions on Electron Devices, vol. 51. No. 11, pp. 1790-97 (Nov. 2004).
Ex-1024	Y. Sun et al., "Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors," Journal of Applied Physics, vol. 101, Art. No. 104503 (22 pages) (May 2007).

Exhibit	Description
Ex-1025	D. James, "2004 – The Year of 90-nm: A Review of 90 nm Devices," 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 72-77 (2005).
Ex-1026	U.S. Pat. Pub. No. 2006/0148151 A1 to Murthy et al.
Ex-1027	U.S. Pat. Pub. No. 2004/0262683 A1 to Bohr et al.
Ex-1028	P. Morin et al., "Extensive Study of the Correlation between Contact Etch Stop Nitride Material Properties and Negative Bias Temperature Instabilities Measured in pMOSFETS," ECS Transactions, vol. 6, no. 3, pp. 355-69 (2007).
Ex-1029	U.S. Pat. Pub. No. 2005/0170104 A1 to Jung et al.
Ex-1030	Y.C. Liu et al., "Single Stress Liner for Both NMOS and PMOS Current Enhancement By a Novel Ultimate Spacer Process," Technical Digest of the 2005 IEEE International Electron Devices Meeting (IEDM), pp. 836-39 (Dec. 2005).
Ex-1031	U.S. Pat. Pub. No. 2008/0145984 A1 to Ke et al.
Ex-1032	P. Bai et al., "A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell," Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 657-60 (Dec. 2004).
Ex-1033	Westlinder et al., "On the Thermal Stability of Atomic Layer Deposited TiN as Gate Electrode in MOS Devices," IEEE Electron Device Letters, vol. 24, no. 9, pp. 550-552 (Sept. 2003).
Ex-1034	U.S. Pat. Pub. No. 2007/0105317 A1 to Nakajima.

Exhibit	Description
Ex-1035	G. Eneman et al., "Scalability of Stress Induced by Contact-Etch-Stop Layers: A Simulation Study," IEEE Transactions on Electron Devices, vol. 54, no. 6, pp. 1446-53 (June 2007).
Ex-1036	M. Quirk & J. Serda, *Semiconductor Manufacturing Technology*, Ch. 12: Metallization (2001) (excerpted).
Ex-1037	U.S. Patent No. 7,785,952 B2 to Chang et al.
Ex-1038	U.S. Patent No. 8,536,660 B2 to Hsu et al.
Ex-1039	U.S. Patent Pub. No. 2005/0048754 A1 to Yeh et al.
Ex-1040	U.S. Patent Pub. No. 2006/0001106 A1 to Metz et al.
Ex-1041	U.S. Patent No. 8,486,789 B2 to Okazaki et al.
Ex-1042	Second Amended Docket Control Order, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation et al.*, No. 2:24-cv-00730-JRG (E.D. Tex.).

LIST OF CHALLENGED CLAIMS

Claim 1	
[1Pre]	A semiconductor device comprising:
[1A]	a first MIS transistor; and
[1B]	a second MIS transistor, wherein:
[1C]	the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon;
[1D]	[the first MIS transistor includes: …] a first gate electrode including a second metal film formed on the first gate insulating film;
[1E]	[the first MIS transistor includes: …] first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and
[1F]	[the first MIS transistor includes: …] a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,
[1G]	the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate, and including a second high-k film made of oxide containing hafnium and silicon;
[1H]	[the second MIS transistor includes: …] a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;

[1I]	[the second MIS transistor includes: …] second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative;
[1J]	[the second MIS transistor includes: …] the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers; and
[1K]	[the second MIS transistor includes: …] source/drain regions formed in the second active region laterally outside the second sidewall spacers,
[1L]	the first and second metal films are made of different metal materials,
[1M]	the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes,
[1N]	the source/drain regions include a silicon mixed crystal layer which is formed in trenches provided in the second active region, and causes first stress in a gate length direction of a channel region in the second active region, and
[1O]	the silicon nitride film has a thickness smaller than that of the first gate electrode.
Claim 2	
The semiconductor device of claim 1, wherein the first metal film has a thickness smaller than that of the second metal film.	

Claim 3
The semiconductor device of claim 1, wherein the first and second metal films have different work functions.
Claim 4
The semiconductor device of claim 1, wherein the conductive film is made of the second metal film.
Claim 5
The semiconductor device of claim 1, wherein the conductive film is made of a silicon film, and the semiconductor device further comprises a metal silicide film formed on the silicon film.
Claim 6
The semiconductor device of claim 1, wherein the first and second gate insulating films are made of the same insulating material.
Claim 7
The semiconductor device of claim 1, wherein: each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section, and the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.
Claim 8
The semiconductor device of claim 1, wherein the silicon nitride film causes second stress in a gate length direction of a channel region in the first active region.

Claim 9	
The semiconductor device of claim 8, wherein: the first MIS transistor is an n-type MIS transistor, and the second stress is tensile stress.	
Claim 10	
The semiconductor device of claim 1, wherein the second MIS transistor is a p-type MIS transistor, the silicon mixed crystal layer is made of a SiGe layer, and the first stress is compressive stress.	
Claim 11	
[11Pre]	A semiconductor device comprising:
[11A]	a first MIS transistor; and
[11B]	a second MIS transistor, wherein:
[11C]	the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate;
[11D]	[the first MIS transistor includes: …] a first gate electrode including a second metal film formed on the first gate insulating film;
[11E]	[the first MIS transistor includes: …] first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and
[11F]	[the first MIS transistor includes: …] a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,

[11G]	the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate;
[11H]	[the second MIS transistor includes: …] a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;
[11I]	[the second MIS transistor includes: …] second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative;
[11J]	[the second MIS transistor includes: …] the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers; and
[1K]	the first and second metal films are made of different metal materials,
[1L]	the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes,
[11M]	the conductive film is made of a silicon film,
[11N]	the semiconductor device further comprises a metal silicide film formed on the silicon film, and
[11O]	the silicon nitride film has a thickness smaller than that of the first gate electrode.

Claim 12
The semiconductor device of claim 11, wherein the first metal film has a thickness smaller than that of the second metal film.
Claim 13
The semiconductor device of claim 11, wherein the first and second metal films have different work functions.
Claim 14
The semiconductor device of claim 11, wherein the first and second gate insulating films are made of the same insulating material.
Claim 15
The semiconductor device of claim 11, wherein the first and second gate insulating films are made of different insulating materials.
Claim 16
The semiconductor device of claim 11, wherein: each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section, and the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.
Claim 17
The semiconductor device of claim 11, further comprising: source/drain regions formed in the second active region laterally outside the second sidewall spacers, wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.

Claim 18	
The semiconductor device of claim 1, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.	
Claim 19	
[19Pre]	A semiconductor device comprising:
[19A]	a first MIS transistor; and
[19B]	a second MIS transistor, wherein:
[19C]	the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon;
[19D]	[the first MIS transistor includes: …] a first gate electrode including a second metal film formed on the first gate insulating film;
[19E]	[the first MIS transistor includes: …] first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and
[19F]	[the first MIS transistor includes: …] a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,
[19G]	the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate, and including a second high-k film made of oxide containing hafnium and silicon;

[19H]	[the second MIS transistor includes: …] a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;
[19I]	[the second MIS transistor includes: …] second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative;
[19J]	[the second MIS transistor includes: …] the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers; and
[19K]	the first and second metal films are made of different metal materials,
[19L]	the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes, and
[19M]	the first metal film is made of titanium nitride.
Claim 20	
The semiconductor device of claim 19, wherein the first metal film has a thickness smaller than that of the second metal film.	
Claim 21	
The semiconductor device of claim 19, wherein the first and second metal films have different work functions.	

Claim 22	
The semiconductor device of claim 19, wherein the silicon nitride film has a thickness smaller than that of the first gate electrode.	
Claim 23	
The semiconductor device of claim 19, wherein: each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section, and the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.	
Claim 24	
The semiconductor device of claim 19, further comprising: source/drain regions formed in the second active region laterally outside the second sidewall spacers, wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.	
Claim 25	
[25Pre]	A semiconductor device comprising:
[25A]	a first MIS transistor; and
[25B]	a second MIS transistor, wherein:
[25C]	the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate;
[25D]	[the first MIS transistor includes: …] a first gate electrode including a second metal film formed on the first gate insulating film;

[25E]	[the first MIS transistor includes: …] first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and
[25F]	[the first MIS transistor includes: …] a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,
[25G]	the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate;
[25H]	[the second MIS transistor includes: …] a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;
[25I]	[the second MIS transistor includes: …] second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative;
[25J]	[the second MIS transistor includes: …] the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers; and
[25K]	the first and second metal films are made of different metal materials,
[25L]	the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes,
[25M]	the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region.

Claim 26
The semiconductor device of claim 25, wherein the first metal film has a thickness smaller than that of the second metal film.
Claim 27
The semiconductor device of claim 25, wherein the first and second metal films have different work functions.
Claim 28
The semiconductor device of claim 25, wherein the silicon nitride film has a thickness smaller than that of the first gate electrode.
Claim 29
The semiconductor device of claim 25, wherein the conductive film is made of the second metal film.
Claim 30
The semiconductor device of claim 25, wherein the conductive film is made of a silicon film, and the semiconductor device further comprises a metal silicide film formed on the silicon film.
Claim 31
The semiconductor device of claim 25, wherein the first and second gate insulating films are made of the same insulating material.

Claim 32
The semiconductor device of claim 25, wherein the first and second gate insulating films are made of different insulating materials.
Claim 33
The semiconductor device of claim 25, wherein: each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section, and the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.
Claim 34
The semiconductor device of claim 25, further comprising: source/drain regions formed in the second active region laterally outside the second sidewall spacers, wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.
Claim 35
The semiconductor device of claim 25, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.

I. RELIEF REQUESTED

Applying the following grounds, Petitioner requests *inter partes* review of the '686 Patent[1] and cancellation of claims 1-35:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1A	19-22	102	Aoyama
1B	11-15, 18-22	103	Aoyama
1C	1-3, 5-10, 16-17, 23-28, 30-35	103	Aoyama, Hsu823
1D	15	103	Aoyama, Hobbs
1E	32	103	Aoyama, Hsu823, Hobbs
2A	19-22	102	Akasaka
2B	19-22	103	Akasaka
2C	1-4, 6-10, 23-29, 31, 33-35	103	Akasaka, Hsu823
2D	32	103	Akasaka, Hsu832, Hobbs

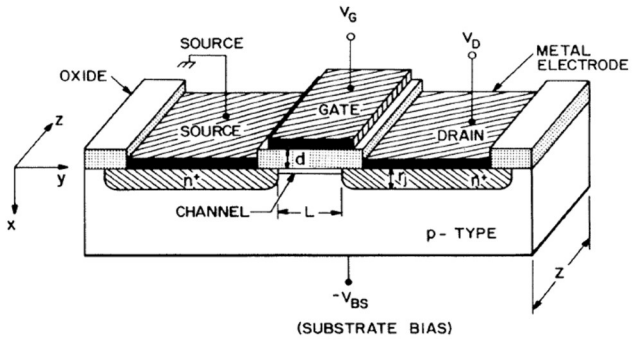
II. STATE OF THE ART

The '686 Patent describes MISFETs (metal-insulator-semiconductor field-effect transistors) having one gate structure for p-type devices and another gate structure for n-type devices. Such MISFETS and gate structures were already known.

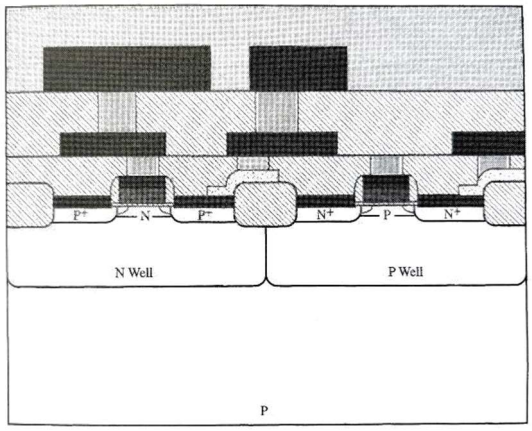
[1] U.S. Patent No. 8,198,686 (Ex-1001).

A. MISFETs

MISFETs[2] have ***source/drain*** regions for current input/output. (Ex-1003, ¶50; Ex-1009, 9-10, Figs. 3, 6; Ex-1010, 45-51.) Additionally, a ***gate*** overlies a ***channel*** region between source and drain. (Ex-1003, ¶50; Ex-1009, 9-10, Fig. 3; Ex-1010, 40-45.) The ***gate*** includes a ***gate dielectric*** that separates a ***gate electrode*** from the channel region. (Ex-1003, ¶50; Ex-1009, 9-10, Fig. 3; Ex-1010, 40-45.) Applying voltage to the gate electrode controls a conductive channel to connect or disconnect the source and drain. (Ex-1003, ¶50; Ex-1009, 9-10, 14, Figs. 3, 6.)



Ex-1009, Fig. 3



Ex-1010, Fig. 1-11

Generally, source/drain regions are ***doped*** with ***p-type*** or ***n-type*** impurities, and channel regions are oppositely doped. (Ex-1003, ¶51; Ex-1009, 9-10; Ex-1010, 45-51.) The terms ***PMOS*** (or "pFETs," "pMIS," "PMOSFETs," or "PMISFETs")

[2] The terms "MISFET" and "MOSFET" ("Metal-***Oxide***-Semiconductor Field-Effect Transistor") are interchangeable. (Ex-1003 ¶50 n.7.)

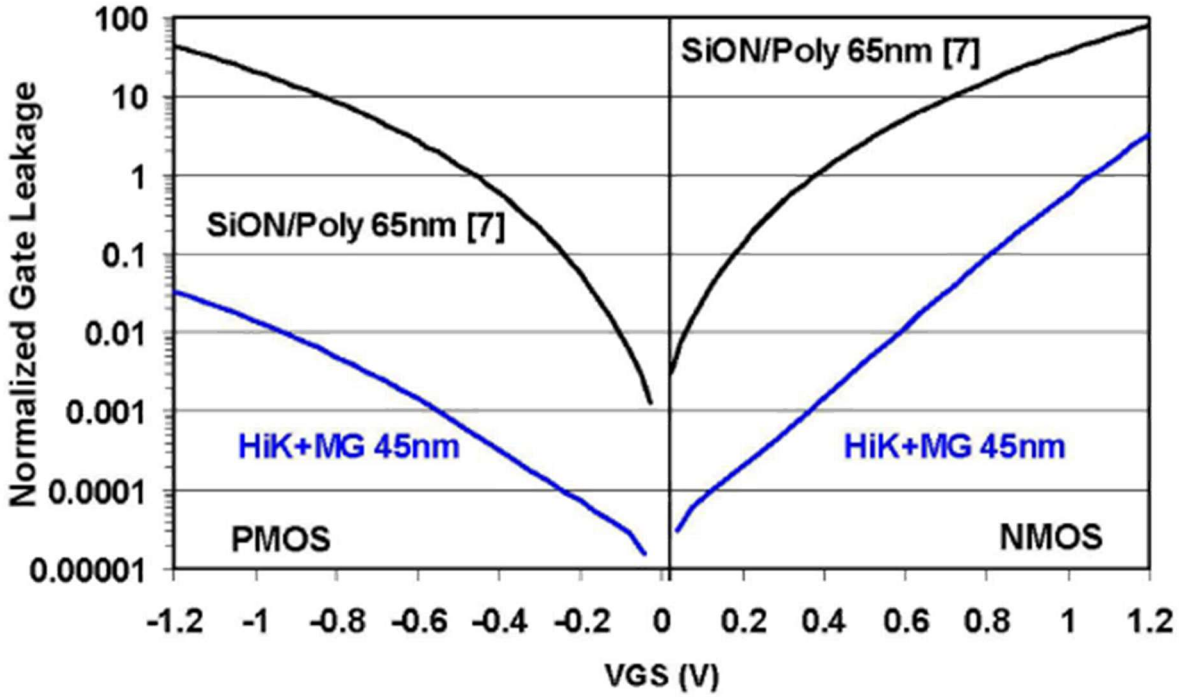
and ***NMOS*** (or "nFETs," "nMIS," "NMOSFETs," or "NMISFETs") refer to MISFETs with p-type or n-type source/drain regions, respectively. (Ex-1003, ¶51; Ex-1010, 16-17, 19-20, Figs. 1-11, 2-2.) Typical devices are ***CMOS*** ("Complementary MOS"), which include both PMOS and NMOS. (Ex-1003, ¶51; Ex-1010, Fig. 1-11.)

B. High-κ Dielectrics

In early MISFETs, gate dielectrics were SiO_2. (Ex-1011, 8.) As MISFETs became smaller, their gate dielectrics became thinner to increase gate capacitance, which improved drive currents and reduced power consumption. (*Id.*; Ex-1012, 6, 24; Ex-1013, 5, 10, 12, 31, Fig. PIDS5; Ex-1014, ¶¶[0003]-[0004].) This eventually required SiO_2 layers so thin they could not reliably function. (Ex-1011, 8; Ex-1014, ¶[0003]; Ex-1015, ¶[0002].) By 2008, the industry turned to ***high-κ*** (a.k.a. "high-k") dielectrics. (Ex-1012, 6, 24; Ex-1013, 5, 10, 12, 31, Fig. PIDS5; Ex-1011, 8; Ex-1014, ¶[0004]; Ex-1016, 1; Ex-1017, 25-28, 45; Ex-1003, ¶¶52-53.)

High-κ dielectrics have a larger ***dielectric constant κ*** ("relative permittivity") than SiO_2 (κ=3.9). (Ex-1011, 8.) For a given capacitance, high-κ dielectrics are thicker than SiO_2, reducing gate leakage and power consumption while improving reliability. (*Id.*; Ex-1003, ¶54.) Examples include hafnium oxide, hafnium silicon oxide, and hafnium silicon oxynitride (κ>10). (Ex-1014, ¶[0004]; Ex-1015, ¶[0002],

¶[0008].) Compared to devices with SiO_2 gate dielectrics, those with high-κ dielectrics exhibit much less leakage. (Ex-1016, 2, Fig. 6.)



Ex-1016, Fig. 6

C. Replacement Metal Gates

In early MISFETs, the gate electrode was typically polysilicon. (Ex-1018, 1:24-26.) But a depletion region (effectively, an insulating barrier) forms at the polysilicon-gate dielectric interface, increasing resistance and reducing drive current. (Ex-1018, 1:26-31; Ex-1019, 1:25-35; Ex-1020, ¶[0004].) This became intolerable as gate dielectrics became thinner. (Ex-1018, 1:31-34; Ex-1019, 1:36-44.) With high-κ gate dielectrics, a large threshold voltage offset also occurs because polysilicon dopants diffuse into them. (Ex-1020, ¶[0005]; Ex-1015,

¶[0003].) To address these issues, the industry added metals to gate electrodes. (Ex-1018, 1:31-34; Ex-1021, 1:28-34, 1:41-42; Ex-1012, 6-7, 24; Ex-1013, 5, 7, 31, Fig. PIDS5; Ex-1003 ¶48, ¶55.)

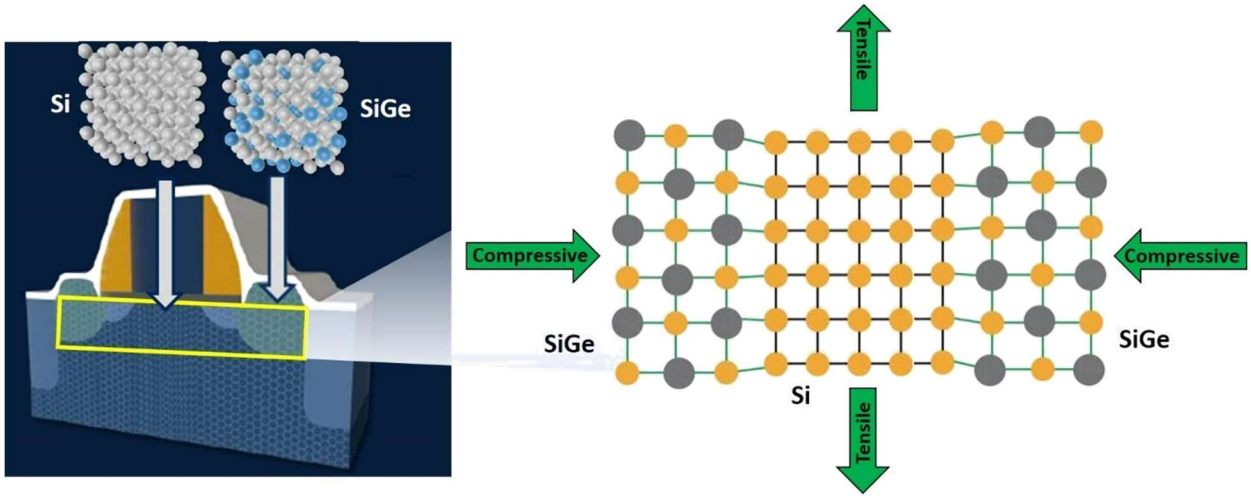
In CMOS, threshold voltage is minimized by adjusting the ***work functions*** of NMOS and PMOS metal gate electrodes. (Ex-1019, 1:17-22; Ex-1020, ¶[0020].) NMOS requires a work function less than about 4.6 eV; PMOS requires a work function greater than about 4.8 eV. (Ex-1019, 1:17-22; Ex-1020, ¶¶[0020]-[0021]; Ex-1003, ¶56.)

Suitable metals for NMOS devices were known, but options for PMOS devices exhibited less thermal stability. (Ex-1019, 1:45-57; Ex-1021, 1:41-48.) One solution was ***replacement metal gates ("RMG")***, a "gate-last" approach that avoids subjecting sensitive metal gates to high temperatures. (Ex-1021, 2:22-29; Ex-1003, ¶¶57-62.) This way, NMOS and PMOS gates can employ different and optimal work functions. (Ex-1022, ¶[0021]; Ex-1019, 2:11-14; Ex-1021, 2:10-12; Ex-1016, 1; Ex-1003, ¶¶57-62.)

D. Strained Silicon Technology

PMOS was once much slower than NMOS. Strained-silicon technology changed that. Because germanium atoms are ***larger*** than silicon atoms, growing silicon-germanium ("SiGe") source/drain regions ***compressively*** strains the silicon channel region along the current flow direction (left-to-right below). In PMOS,

compressive strain improves carrier (hole) mobility and boosts operating speed. (Ex-1023, 1-7; Ex-1024, 2 Ex-1003, ¶63.) By 2005, this technology increased "hole mobility by as much as 50%." (Ex-1025, 2; Ex-1003, ¶63.)



These principles were also commonly applied to NMOS, except improving NMOS carrier (electron) mobility requires ***tensile*** strain, not compressive. (Ex-1003, ¶65.) Creating tensile strain with source/drain regions requires growing a material like silicon carbide (SiC) with an atom (e.g., carbon) ***smaller*** than silicon. (Ex-1026, ¶[0005], ¶[0048], ¶[0072]; Ex-1025, 2; Ex-1027, ¶[0045]; Ex-1003, ¶65.)

In addition to source/drain epitaxy, it was also common to induce strain by applying stressed films. (Ex-1003, ¶66; Ex-1025, 2, 4; Ex-1028, 1-2, 13; Hsu823, ¶[0003]; Ex-1029, ¶[0090]; Ex-1030, 1-2, Figs. 1-7; Ex-1023, Fig. 5(c).) For example, depositing a silicon nitride contact etch-stop layer ("CESL") can, under certain conditions, "apply[] stress to [a] channel region" to improve carrier mobility. (Hsu823, ¶[0003]; *see* Ex-1031, ¶[0003]; Ex-1029, ¶[0090]; Ex-1028, 1-2; Ex-1030,

1-2; Ex-1003, ¶66.) Depending how such a layer is prepared, it may be tensile, compressive, or unstrained. (Ex-1029, ¶[0017], ¶¶[0099]-[0100], ¶¶[0131]-[0132], TBLS. IV-V, VII, FIG. 15; Ex-1003, ¶66.)

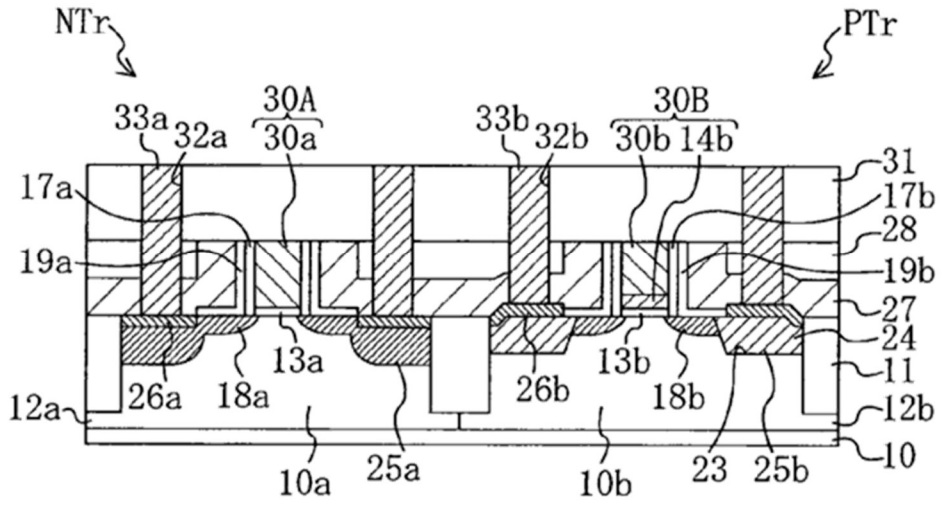
Strained Si technology was well-known before the '686 Patent. Three generations of high-volume commercial devices already used it by then. (Ex-1023, 1-2 (Intel 90nm devices); Ex-1032, 4-5 (Intel 65nm devices); Ex-1016, 1-2 (Intel 45nm devices); Ex-1003, ¶48, ¶64.)

III. THE '686 PATENT

A. Overview

The '686 Patent describes a known application of the technologies described above, including "n-[type] and p-type MIS transistors having gate electrodes made of different metal materials." (Ex-1001, 5:39-42.) Figure 5C illustrates one embodiment. (*Id.*, 11:56-67, 12:8-17, 12:50-63, 14:51-15:5, 16:10-22, 16:55-60, FIGS. 1A-5C.)

FIG. 5C



NTr:	nMIS transistor	**PTr:**	pMIS transistor
13a:	gate insulating film	**13b:**	gate insulating film
30A:	first gate electrode	**30B:**	second gate electrode
30a:	metal film	**14b:**	metal film
		30b:	conductive film
17a:	insulative sidewall spacer	**17b:**	insulative sidewall spacer
19a:	insulative sidewall spacer	**19b:**	insulative sidewall spacer

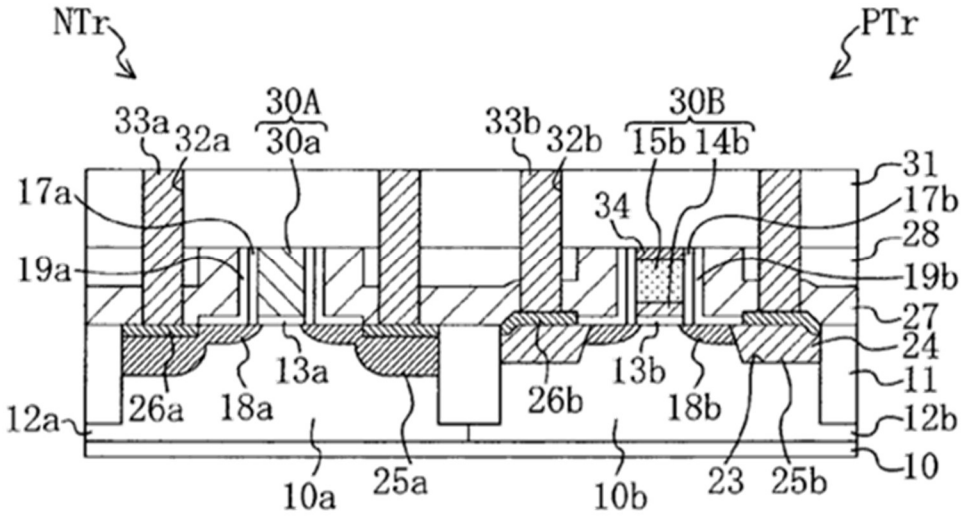
nMIS & pMIS Transistors

27: insulating film **28:** inter-layer insulating film

Gate insulating films 13a/13b may be formed of the same or different materials, e.g., a high-κ metal-oxide. (*Id.*, 11:31-37, 29:16-24.) As shown above, insulating film 27 (e.g., silicon nitride) does not overlie any upper surface of the gate electrodes. (*Id.*, 6:42-45, 15:6-22, 15:23-30.)

In some embodiments (e.g., FIG. 5C), pMIS conductive film 30b may be the same material as nMIS metal film 30a. In other embodiments (e.g., FIG. 8C below), pMIS conductive film 15b is silicon, and a metal silicide film 34 is formed in it. (*Id.*, 21:61-67, 22:33-49.)

FIG. 8C



The '686 Patent describes stressed active regions 10a/10b. (*Id.*, 28:63-29:15.) In second active region 10b, silicon mixed crystal layer 24 (e.g., SiGe) may be formed in trenches 23 to compressively stress the pMIS channel. (*Id.*, 13:60-65, 19:54-61, 23:28-33.) In first active region 10a, insulating film 27 applies tensile stress to the nMIS channel. (*Id.*, 28:16-43.)

B. Prosecution History

The Prosecution History includes four office actions and narrowing amendments. (*See generally* Ex-1002.) In a first office action, the Examiner rejected certain claims based on Aoyama's first embodiment (FIGS. 1-2N). (Ex-1002,

201-06.) This Petition, however, relies on Aoyama's third embodiment (FIGS. 5-6Q), which the Examiner never addressed or cited. Because Aoyama's third embodiment is anticipating, that constituted a material error.

C. Claim Construction

Claims are construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). No terms need construction to resolve this controversy.[3]

D. Level of Ordinary Skill

A person of ordinary skill in the art ("POSITA") would have had at least a master's degree in electrical engineering, physics, materials science, or a related field and at least three years of work experience in semiconductor device design and manufacturing, including replacement metal gates, strained-channel MISFETs, and fabrication of such devices. Additional education could substitute for professional experience, and significant work experience or training could substitute for formal education. (Ex-1003, ¶¶44-47.)

[3] Certain features may be indefinite and/or require construction to resolve controversies in other forums but not the issues in this Petition.

IV. PRIOR ART

A. Aoyama (Ex-1005)

Aoyama is prior art under pre-AIA §§102(a) and (e). Because Aoyama is in the same field (MISFETs) and reasonably pertinent to a problem the '686 Patent addresses (high-κ/metal gate design), Aoyama is analogous art. (Ex-1003, ¶98.)

This Petition focuses on Aoyama's third embodiment below. (Aoyama, ¶¶[0097]-[0121], FIGS. 5-6Q.)

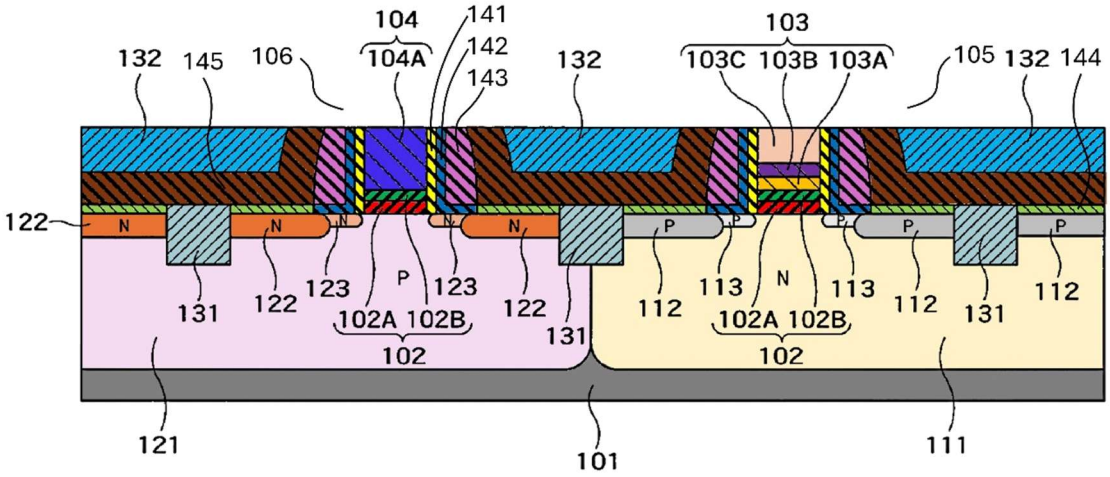


FIG. 5

Aoyama, FIG. 5[4]

Both the NMOS (106) and PMOS (105) include a silicon oxide gate layer 102A, a high-κ gate dielectric layer 102B, and spacers 141-143. (Aoyama ¶[0098], ¶[0111].)

[4] Petitioner has added all color annotations in this Petition. Additionally, Aoyama's Figure 5 has been amended throughout to include all relevant numeric labels.

Over the high-κ film, their gate structures differ. PMOS gate electrode 103 comprises a first conductive layer 103A, a second conductive layer 103B, and a semiconductor layer (silicide layer) 103C. (Aoyama, ¶[0107], ¶[0114], ¶[0121].) NMOS gate electrode 104 comprises only a third conductive layer 104A. (Aoyama, ¶[0118].) Etch stopper 145 and interlayer dielectric 132 fill the spaces between the NMOS and PMOS gate structures. (Aoyama ¶[0113].)

B. Akasaka (Ex-1008)

Akasaka is prior art under pre-AIA §102(b). Because Akasaka is in the same field (MISFETs) and reasonably pertinent to a problem the '686 Patent addresses (high-κ/metal gate design), Akasaka is analogous art. (Ex-1003, ¶102.)

Akasaka describes MISFETs as shown below. (Akasaka, ¶[0072], FIG. 26.)

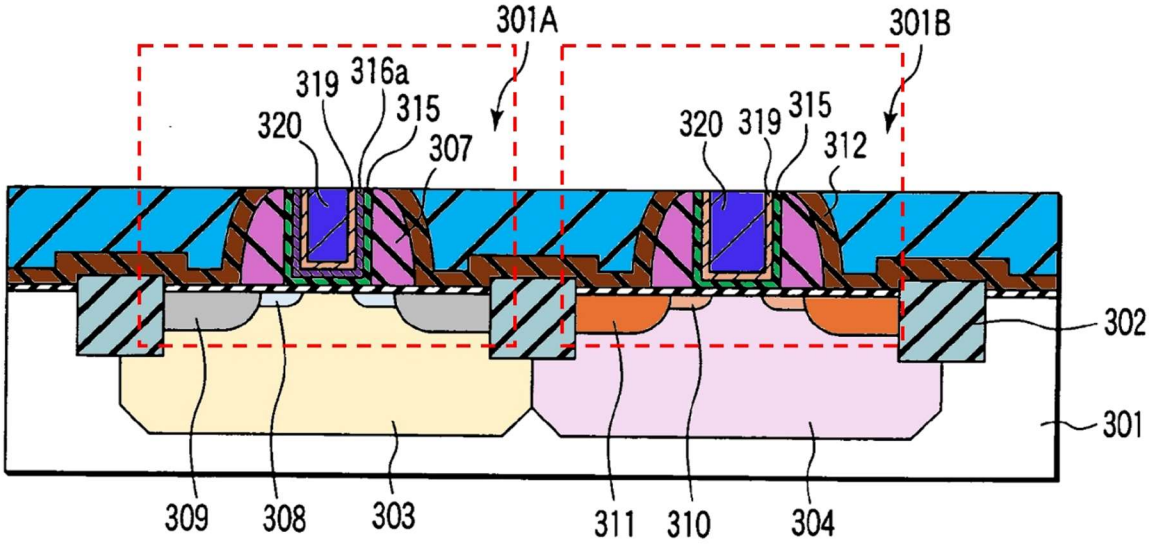


FIG. 26

Akasaka, FIG. 26

Each PMISFET 301A and NMISFET 301B includes a gate dielectric 315 (e.g., $HfSi_xO_y$). (Akasaka, ¶[0075].) Over the gate dielectric, the PMISFET and NMISFET gate electrodes comprise conductive films 319 and 320. (Akasaka, ¶¶[0084]-[0086].) The PMISFET gate electrode additionally comprises conductive film 316. (Akasaka, ¶¶[0076]-[0077].) Silicon nitride film 312 and inter-level insulating film 313 fill the spaces between MISFETs. (Akasaka, ¶[0073].)

C. Hsu823 (Ex-1006)

Hsu823 is prior art under pre-AIA §§102(a) and (e). Because Hsu823 is in the same field (MISFETs) and reasonably pertinent to a problem the '686 Patent addresses (straining MISFET channels), Hsu823 is analogous art. (Ex-1003, ¶106.)

Hsu823 explains: "When devices become smaller, the distance between devices decreases." This leads to a "gap-filling problem" (voiding). (Hsu823, ¶[0004].) To address this, Hsu823 teaches an L-shaped silicon oxide spacer liner and a silicon nitride spacer. (Hsu823, ¶[0031], ¶[0035], FIGS. 6, 15A.) After using the silicon nitride spacer to define source/drain regions, the outer spacer may be removed, leaving only the L-shaped spacer liner. (Hsu823, ¶[0035], FIGS. 9, 15B.) This way, "gap-filling is improved and the contact etching process can be better controlled." (Hsu823, ¶[0043].)

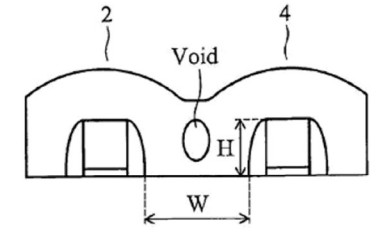
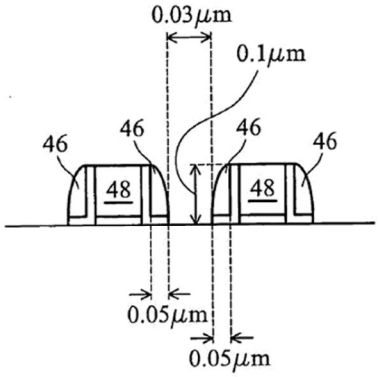


FIG. 1 (PRIOR ART)



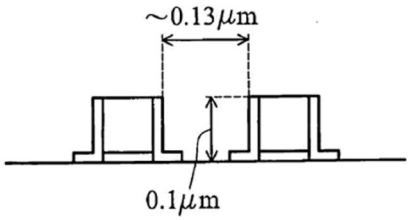


FIG. 15B

FIG. 15A

Hsu823, FIGS. 1, 15A, 15B

Hsu823 discloses MISFET structures like the one on the left below. (Hsu823, FIG. 10.) According to Hsu823, layer 32 may be omitted so that CESL 34 directly contacts L-shaped spacer liners 114/214. (Hsu823, ¶[0015], ¶[0036], FIGS. 9-10, 14.) CESL 34 may exert tensile stress. (Hsu823, ¶¶[0036]-[0037].)

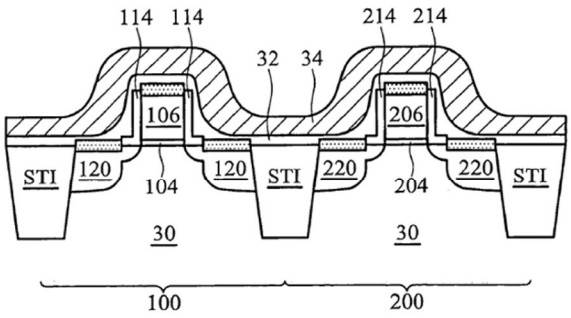


FIG. 10

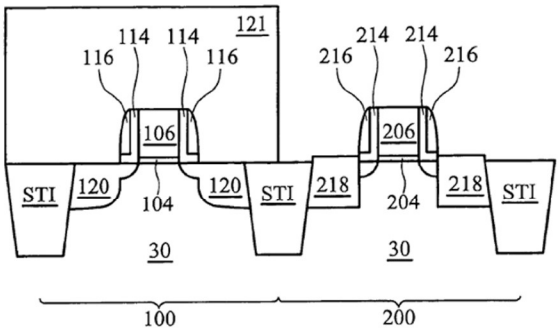


FIG. 7B

Hsu823, FIGS. 10, 7B

Moreover, PMOS source/drain regions (220, left above) may be formed using epitaxial SiGe (218, right above). (Hsu823, ¶[0033], FIG. 7B.) In this technique, recess etching in the source/drain regions forms trenches in which epitaxial SiGe

grows. (*Id.*) "This introduces compressive stresses in the respective channel regions of the resulting PMOS devices, and the device drive currents of the respective PMOS devices are increased." (Hsu823, ¶[0033].)

D. Hobbs (Ex-1007)

Hobbs is prior art under pre-AIA §§102(b). Because Hobbs is in the same field (MISFETs) and reasonably pertinent to a problem the '686 Patent addresses (replacement gate design), Hobbs is analogous art. (Ex-1003, ¶111.)

Hobbs discloses a RMG process for forming MISFETs in which both dummy gate electrodes and dummy gate dielectrics are replaced. As FIG. 5 shows, dummy structures 201/202 are formed, each of which includes polysilicon layer 164 formed on dielectric layer 162. (Hobbs, 3:19-23, 3:47-51.)

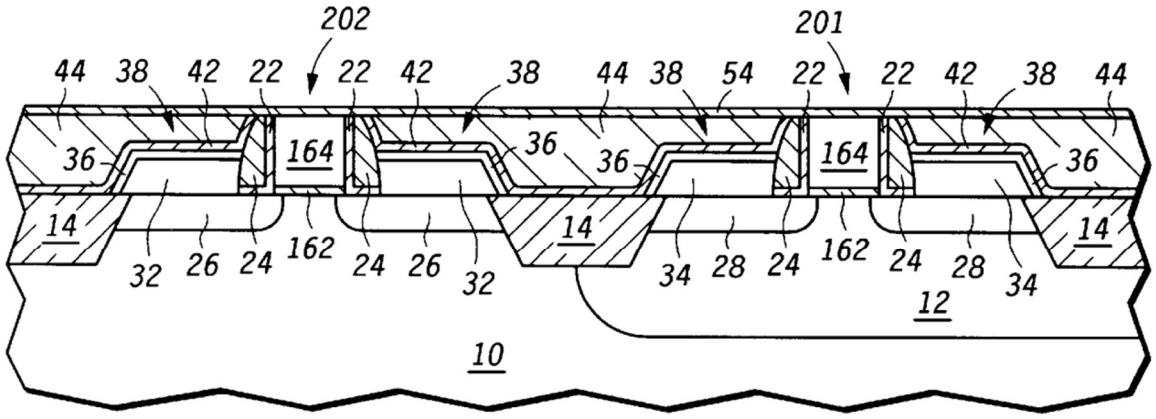


FIG. 5

Then, as FIGS. 6-10 show, both polysilicon layer 164 and dielectric layer 162 are replaced. (Hobbs, 4:42-44, 4:60-62, 5:52-56.) This allows "different gate dielectric materials and thickness as well as different gate materials [to] be selected to form a various transistors with different threshold voltages and operating characteristics." (Hobbs, 8:40-45.)

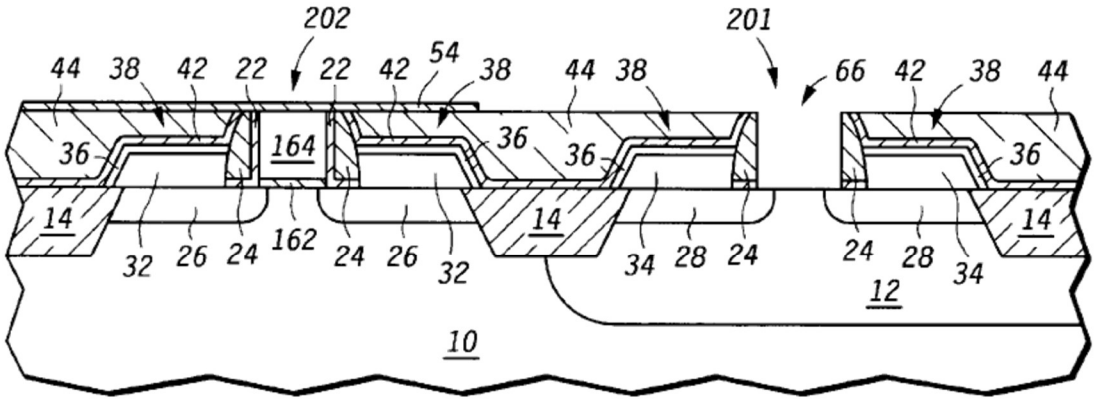


FIG.6

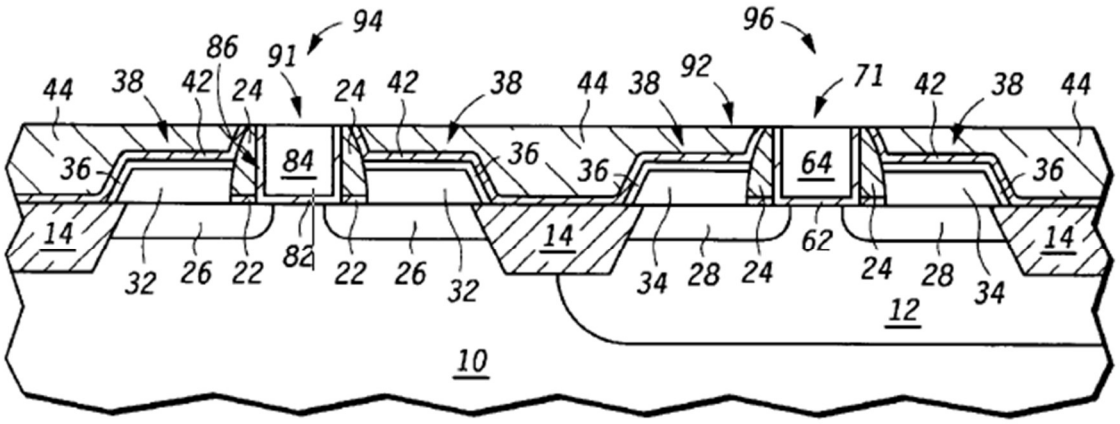


FIG.10

V. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Grounds 1A and 1B: Aoyama Anticipates (Ground 1A) or at Least Renders Obvious (Ground 1B) Claims 19-22

1. Independent Claim 19

a. [19Pre]

Aoyama discloses[5] "a semiconductor device." (Aoyama, ¶[0003], ¶[0097]; *see id.*, FIG. 5 (below); Ex-1003, ¶¶115-117.)

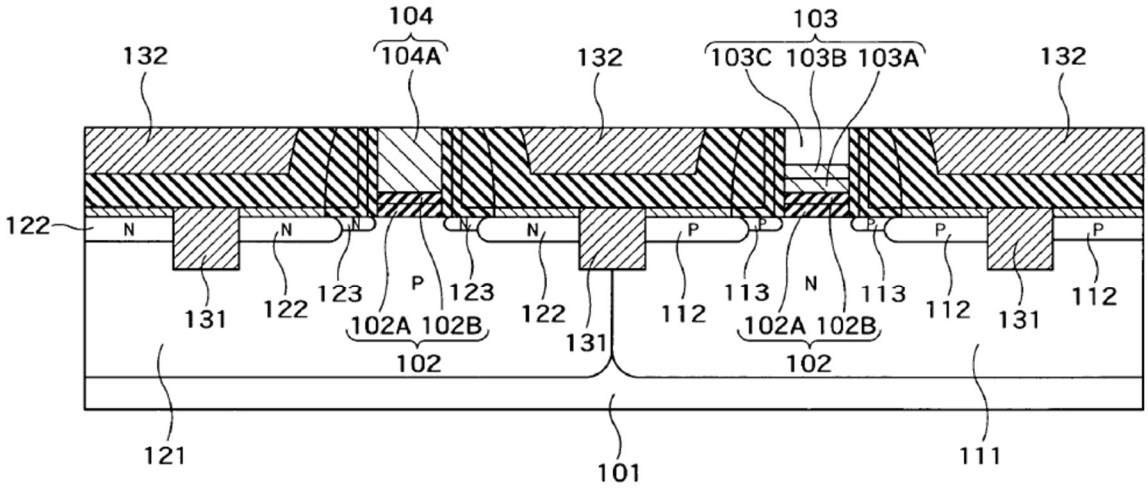


FIG. 5

b. [19A]

Aoyama discloses "a first MIS transistor": an "NMOSFET" (106). (Aoyama, ¶[0106]; Ex-1003, ¶¶118-120.)

[5] As used herein, a reference "discloses" what it teaches, suggests, or at least renders obvious.

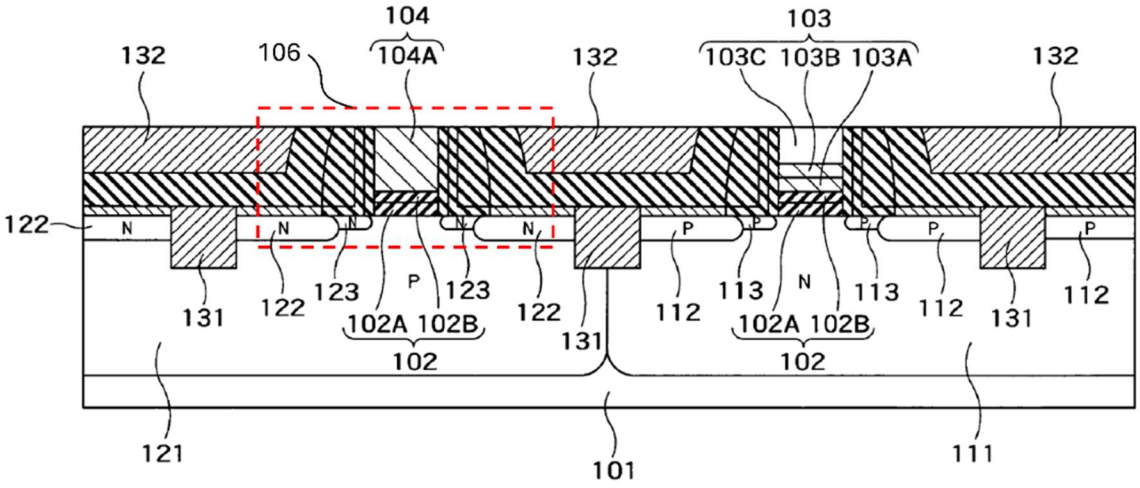


FIG. 5

Aoyama, FIG. 5

c. [19B]

Aoyama discloses "a second MIS transistor": a "PMOSFET" (105). (Aoyama, ¶[0106]; Ex-1003, ¶¶121-123.)

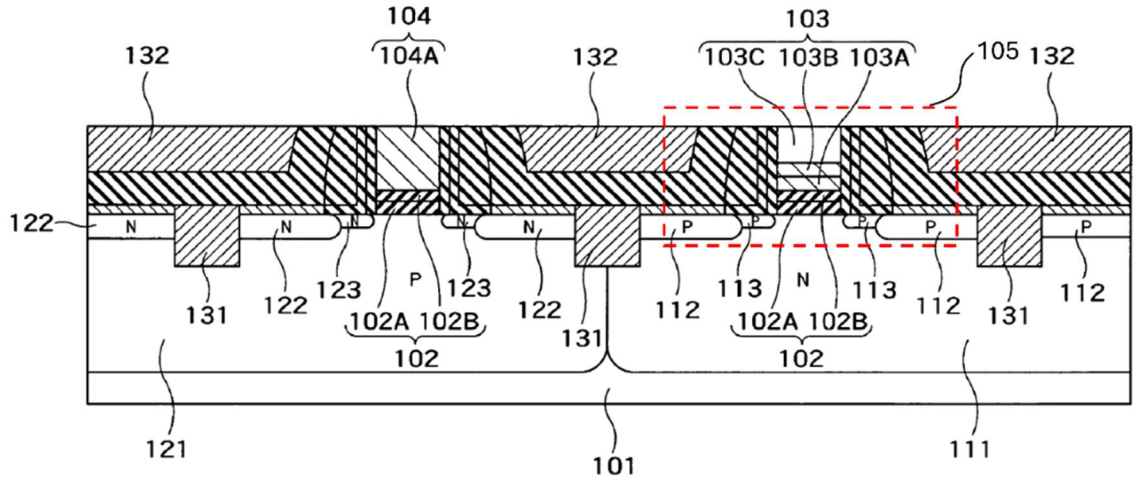


FIG. 5

Aoyama, FIG. 5

d. [19C]

Aoyama discloses the "first MIS transistor" includes "a first gate insulating film formed on a first active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon." (Ex-1003, ¶¶124-130.)

Aoyama's NMOSFET gate insulating film 102 is identical to the '686 Patent—a 2 nm-thick hafnium silicon oxynitride film 102B on a 0.8 nm-thick silicon oxide film 102A. (*Compare* Ex-1001, 11:25-37, 29:16-24, *with* Aoyama, ¶[0098], ¶[0106].) Aoyama's gate dielectric film 102 (first gate insulating film) is formed on "NMOSFET region 106" (first active region) in "substrate 101" "where the NMOSFET is to be formed." (Aoyama, ¶¶[0105]-[0106], FIGS. 6C-6D.) According to the '686 Patent, hafnium silicon oxynitride gate dielectric film 102B is an oxide containing hafnium and silicon. (Aoyama, ¶[0106]; Ex-1001, 29:16-24 (identifying "oxides such as … hafnium silicon oxynitride"); Ex-1003, ¶¶127-128.) Gate dielectric film 102 (including 102A and 102B) thus discloses the claimed "first gate insulating film." (Ex-1003, ¶¶125-128, ¶130.)

Alternatively, if part of a gate dielectric film structure may constitute a "gate insulating film," gate dielectric film 102B alone discloses the claimed "first gate insulating film." (Ex-1003, ¶129.)

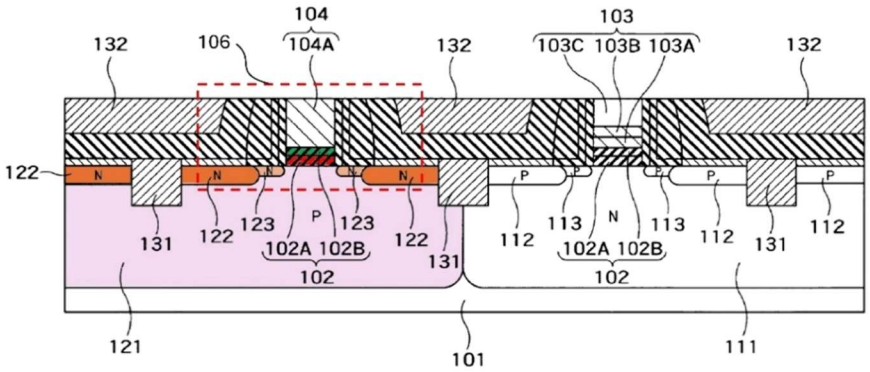


FIG. 5

Aoyama, FIG. 5

e. [19D]

Aoyama discloses the "first MIS transistor" includes "a first gate electrode including a second metal film formed on the first gate insulating film." (Ex-1003, ¶¶131-133.)

Aoyama discloses a "gate electrode 104" (first gate electrode) including a "conductive layer 104A which is made of conductive metal" (second metal film) formed on the first gate insulating film (*supra* [19C]). (Aoyama, ¶[0098], FIG. 5.)

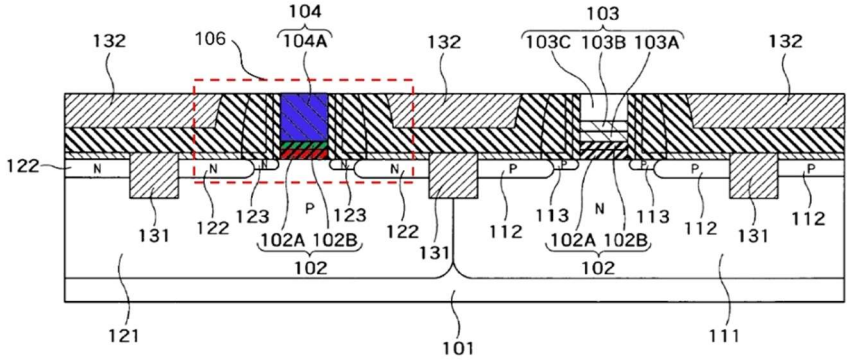


FIG. 5

Aoyama, FIG. 5

f. [19E]

Aoyama discloses the "first MIS transistor" includes "first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative." (Ex-1003, ¶¶134-137.)

Aoyama discloses "side wall spacer[s] 142" (first sidewall spacers) "made of a silicon oxide film," which is insulative.[6] (Aoyama, ¶[0111]; Ex-1003 ¶¶135-136.) As FIG. 5 shows, the first sidewall spacers are formed on side surfaces of the first gate electrode (gate electrode 104).

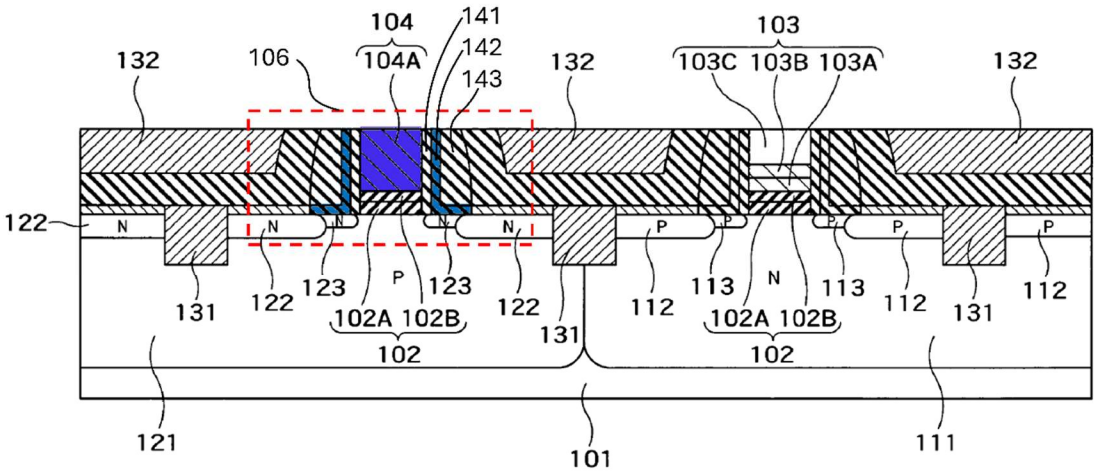


FIG. 5

Aoyama, FIG. 5

[6] Alternatively, Aoyama's offset spacers 141 and sidewall spacers 142, collectively, disclose the "first sidewall spacers." (Aoyama, ¶[0111].) Both are "made of a silicon oxide film." (*Id.*)

g. [19F]

Aoyama discloses the "first MIS transistor" includes "a silicon nitride film [etch stopper film 145] formed, extending over the side surfaces of the first gate electrode [gate electrode 104] on which the first sidewall spacers [sidewall spacers 142[7]] are formed and upper surfaces of regions [source/drain layers 122] located in the first active region [NMOSFET region 106] laterally outside the first sidewall spacers," as FIG. 5 shows. (Aoyama, ¶[0100] (disclosing "source/drain diffusion layer 122 for the NMOSFET"), ¶[0113] ("[A] silicon nitride film [145] is formed over the entire surface."); Ex-1003, ¶¶138-143.) Etch stopper film 145 is "formed over the entire surface," then "planarized by chemical mechanical polishing or etching" to expose the metal gate electrodes. (Aoyama, ¶[0113]; *see id.* ¶¶[0114]-[0119], FIGS. 6K-6Q.)

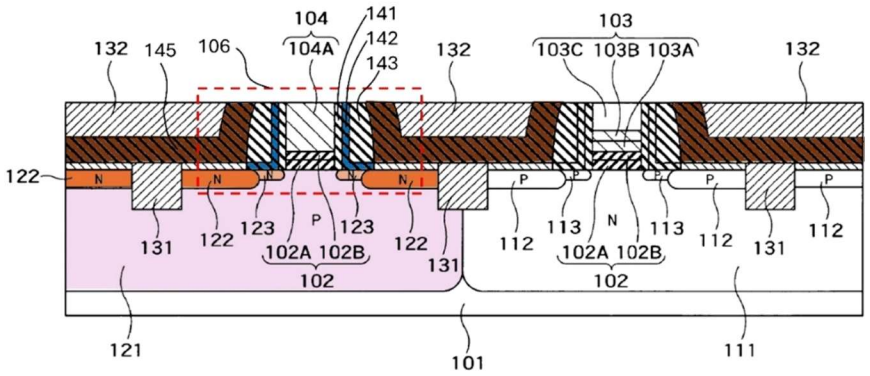


FIG. 5

Aoyama, FIG. 5

[7] *See supra* note 6.

h. [19G]

Aoyama discloses the "second MIS transistor" includes "a second gate insulating film formed on a second active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon." (Ex-1003, ¶¶144-150.)

Aoyama's PMOSFET gate insulating film 102 is identical to the '686 Patent—a 2 nm-thick hafnium silicon oxynitride film 102B on a 0.8 nm-thick silicon oxide film 102A. (*Compare* Ex-1001, 11:25-37, 29:16-24, *with* Aoyama, ¶[0098], ¶[0106].) Gate dielectric film 102 (second gate insulating film) is formed on "PMOSFET region 105" (second active region) in "substrate 101" "where the PMOSFET is to be formed." (Aoyama, ¶¶[0104]-[0106], FIGS. 5, 6B-6D.) According to the '686 Patent, hafnium silicon oxynitride gate dielectric film 102B is an oxide containing hafnium and silicon. (Aoyama, ¶[0106]; Ex-1001, 29:16-24 (identifying "oxides such as … hafnium silicon oxynitride"); Ex-1003, ¶¶147-148.) Gate dielectric film 102 (including 102A and 102B) thus discloses the claimed "second gate insulating film." (Ex-1003, ¶¶145-148, ¶150.)

Alternatively, if part of a gate dielectric film structure may constitute a "gate insulating film," gate dielectric film 102B alone discloses a "second gate insulating film." (Ex-1003, ¶149.)

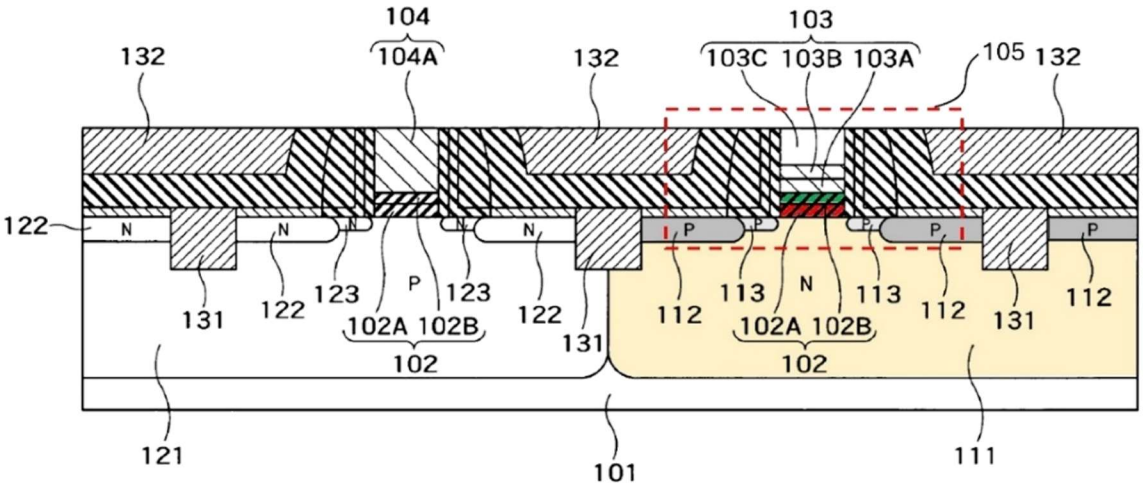


FIG. 5

Aoyama, FIG. 5

i. [19H]

Aoyama discloses the "second MIS transistor" includes "a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film." (Ex-1003, ¶¶151-155.)

Aoyama discloses a "gate electrode 103" (second gate electrode) including a "conductive layer 103B … made of conductive metal" (first metal film) formed on the second gate insulating film (*supra* [19G]). (Aoyama, ¶[0098].) Aoyama further discloses a "semiconductor layer (silicide layer) 103C" formed on the first metal film (layer 103B). (Aoyama, ¶[0121].) Like the '686 Patent, semiconductor layer (silicide layer) 103C comprises a "polysilicon or amorphous silicon" layer and a "Ni monosilicide (NiSi)" layer. (*Compare* Aoyama, ¶[0107], ¶[0114], *with* Ex-1001,

11:50-67, 29:41-45, 21:30-35, FIG. 8C (layers 15b and 34); *see infra* §V.B.1.d ([11N]).) Either or both parts of Aoyama's layer 103C constitutes the claimed "conductive film." (Aoyama, ¶[0121] ("[G]ate electrode 103 for the PMOSFET includes … semiconductor layer (silicide layer) 103C made of the semiconductor (silicide). ***For this reason,*** in the third embodiment, ***the gate resistance of the PMOSFET is relatively low.***" (emphasis added)); Ex-1003, ¶¶152-154.)

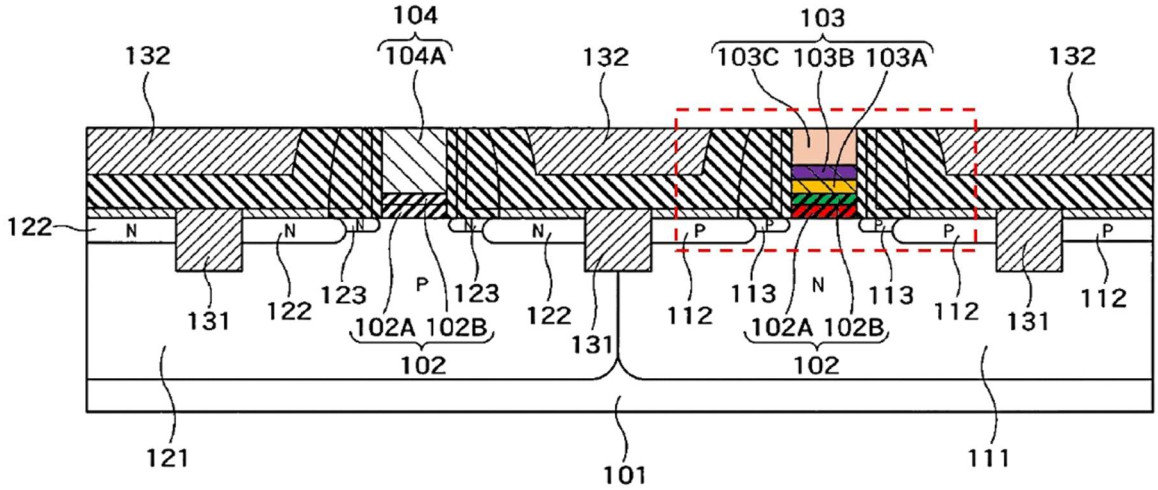


FIG. 5

Aoyama, FIG. 5

j. [19I]

Aoyama discloses the "second MIS transistor" includes "second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative." (Ex-1003, ¶¶156-159.)

Aoyama discloses "side wall spacer[s] 142" (second sidewall spacers) "made of a silicon oxide film," which is insulative.[8] (Aoyama, ¶[0111]; Ex-1003, ¶¶157-158.) As FIG. 5 shows, these second sidewall spacers (blue) are formed on side surfaces of the second gate electrode (gate electrode 103).

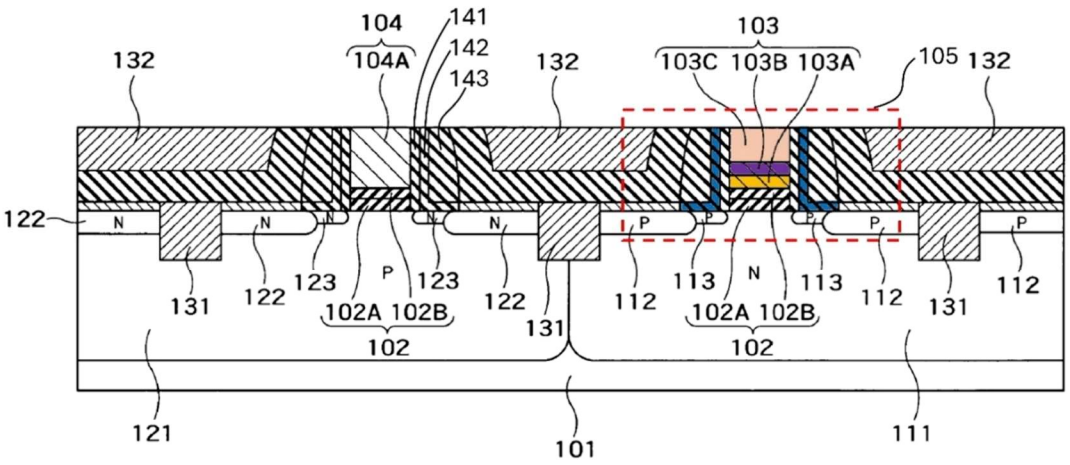


FIG. 5

Aoyama, FIG. 5

k. [19J]

Aoyama discloses the "second MIS transistor" includes "the silicon nitride film [etch stopper film 145] formed, extending over the side surfaces of the second gate electrode [gate electrode 103] on which the second sidewall spacers [sidewall

[8] Alternatively, Aoyama's offset spacers 141 and sidewall spacers 142, collectively, disclose the "second sidewall spacers." (Aoyama, ¶[0111].) Both are "made of a silicon oxide film." (*Id.*)

spacers 142[9]] are formed and upper surfaces of regions [source/drain layers 112] located in the second active region [PMOSFET region 105] laterally outside the second sidewall spacers," as FIG. 5 shows. (Aoyama, ¶[0099] (disclosing "source/drain diffusion layer 112 for the PMOSFET"), ¶[0113] ("[A] silicon nitride film [145] is formed over the entire surface."); *supra* §V.A.1.g; Ex-1003, ¶¶160-165.)

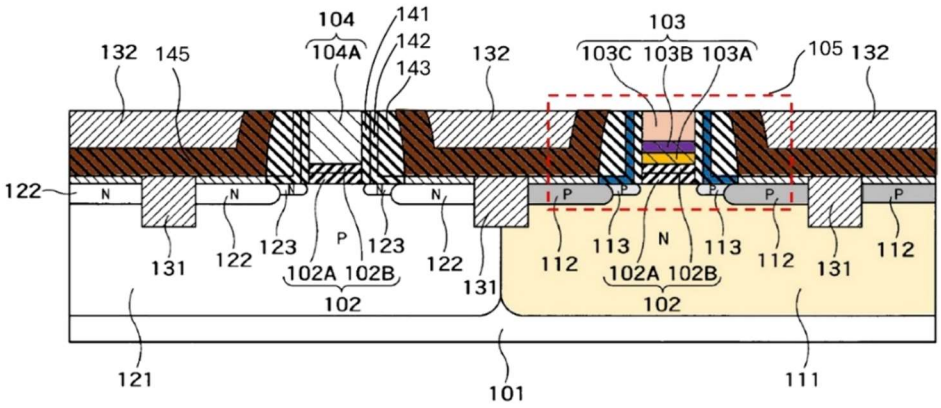


FIG. 5

Aoyama, FIG. 5

l. [19K]

Aoyama discloses "the first and second metal films are made of different metal materials." (Ex-1003, ¶¶166-170.) Conductive layer 104A (second metal film) is TaCN, and conductive layer 103B (first metal film) is TiN. (Aoyama, ¶[0107], ¶[0118].)

[9] *See supra* note 8.

m. [19L]

Aoyama discloses "the silicon nitride film [etch stopper film 145] is not formed on any of upper surfaces of the first and second gate electrodes." (Ex-1003, ¶¶171-175.) Etch stopper film 145 is "formed over the entire surface" and "planarized" so "semiconductor layer[] 103C … [is] exposed both in the PMOSFET region 105 and the NMOSFET region 106." (Aoyama ¶[0113]; *see id.* ¶¶[0114]-[0119], FIGS. 6K-6Q.) Such planarization eliminates etch stopper film 145 from the upper surfaces of gate electrodes 103 and 104, as shown below. (Ex-1003, ¶¶172-174.)

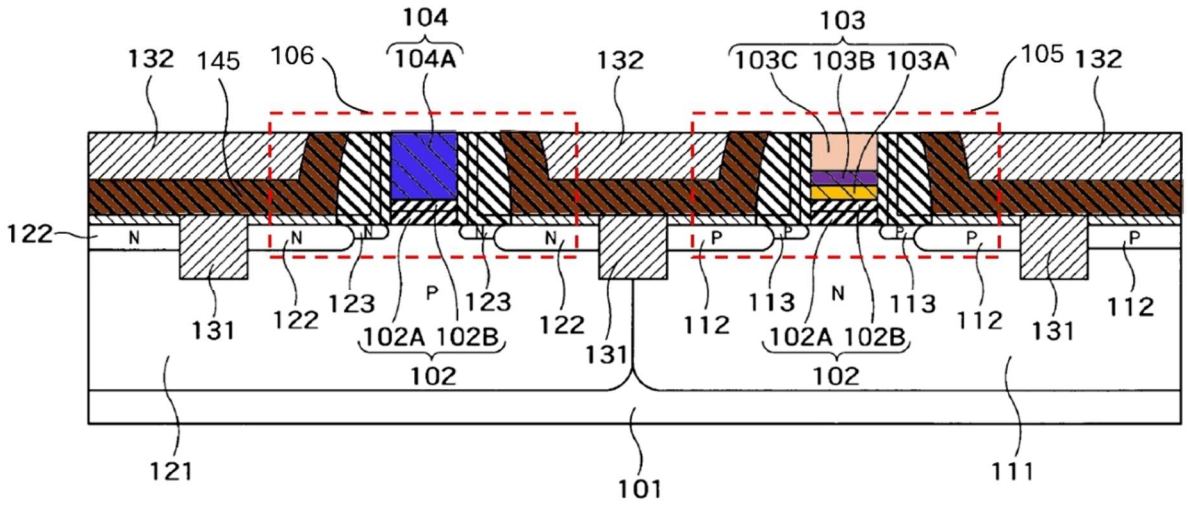


FIG. 5

Aoyama, FIG. 5

n. [19M]

Aoyama discloses "the first metal film is made of titanium nitride." (Ex-1003, ¶¶176-178.) Conductive layer 103B (first metal film) is "a TiN (titanium nitride) layer." (Aoyama, ¶[0107]; *see id.* ¶[0109], ¶¶[0115]-[0116].)

2. Claim 20

Aoyama discloses "wherein the first metal film [conductive layer 103B] has a thickness smaller than that of the second metal film [conductive layer 104A]." (Ex-1003, ¶¶179-188.) Because both gate structures are planarized after forming conductive layer 104A (Aoyama ¶[0119], FIG. 6Q), and because gate electrodes 103 and 104 are both formed on gate dielectric film 102, that means gate electrodes 103 (layers 103A-103C, collectively) and 104 (layer 104A) have the same thickness. (*See* Aoyama, FIG. 5; Ex-1003, ¶¶183-187.) Accordingly, conductive layer 103B must be thinner than conductive layer 104A, as shown. (Ex-1003, ¶187; *see* Aoyama ¶¶[0114]-[0119], FIGS. 6G-6Q.)

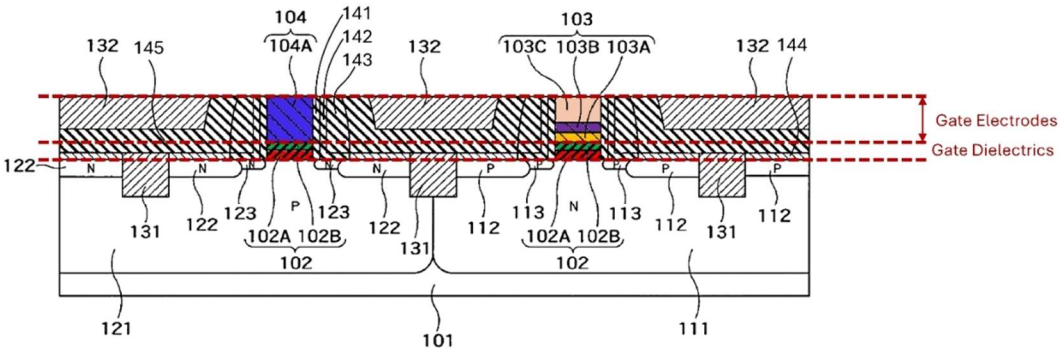


FIG. 5

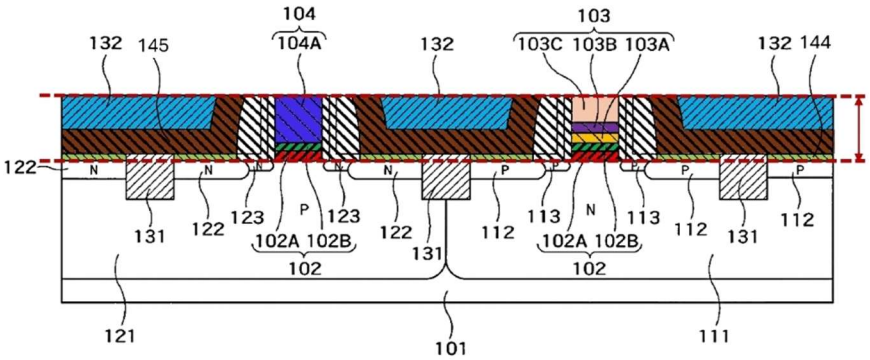
Aoyama, FIG. 5

3. Claim 21

Aoyama discloses "wherein the first and second metal films have different work functions." (Ex-1003, ¶¶189-196.) Conductive layer 104A (second metal film) is TaCN; conductive layer 103B (first metal film) is TiN. (Aoyama, ¶[0107], ¶[0118].) The work functions of TaCN (e.g., 4.3 eV or less) and TiN (e.g., 5.1 eV) differ. (Ex-1003, ¶¶193-195; *see* Aoyama, ¶[0010]; Ex-1033, 2; Akasaka, ¶[0046], ¶[0077].

4. Claim 22

Aoyama discloses "silicon nitride film [etch stopper film 145] has a thickness smaller than that of the first gate electrode [gate electrode 104]." (Ex-1003 ¶¶197-231.) Aoyama's FIG. 5 shows etch stopper film 145 much thinner than gate electrode 104. *See Koito Mfg. Co. v. Turn-Key-Tech, LLC*, 381 F.3d 1142, 1154-56 (Fed. Cir. 2004) (finding "relative dimensions" of a patent figure alone disclosed a claim limitation reciting one feature "significantly thicker and wider" than another); Ex-1003, ¶¶199-200.



Aoyama, FIG. 5

For at least four additional reasons, a POSITA also would have found claim 22 obvious. (Ex-1003, ¶¶201-231.)

First, Aoyama's gate electrodes 103 and 104 are planarized. (Aoyama, ¶[0119], FIG. 6Q.) As the red arrow above indicates, the collective thickness of etch stopper film 145 and interlayer dielectric 132 cannot exceed the gate height. Thus, even when improperly ignoring silicide film 144, etch stopper film 145 will be thinner than gate electrode 104 so long as interlayer dielectric 132 is thicker than gate dielectric film 102. (Ex-1003, ¶¶203-207.)

A POSITA would have expected Aoyama's interlayer dielectric 132 to be thicker than gate dielectric film 102; a POSITA would have found it highly unusual were it otherwise. (Ex-1003, ¶202, ¶208, ¶¶211-215; *see* Ex-1034, ¶[0317] (120 nm gate electrode), ¶[0326] (30 nm CESL & 250 nm ILD planarized to about 90 nm), FIG. 52.) A POSITA would have known the thickness of a gate dielectric is negligible compared to a gate electrode. (Ex-1003, ¶209; *see* Ex-1025, Figs. 1-3, 5-6, 8-12; Ex-1016, Fig. 6; Ex-1017, 25; Ex-1023, Fig. 2; Ex-1028, Fig. 1.) The gate dielectric is famously very thin to maximize capacitance. (Ex-1003, ¶209; *see* Ex-1011, 8.) Aoyama's gate dielectric film 102 is less than 3 nm thick—only several atomic layers. (Aoyama, ¶[0106]; Ex-1003, ¶210.) Interlayer dielectrics, on the other hand, require low capacitance and are much thicker: "gate and interlayer (ILD)

dielectric films" have "opposing requirements" in that regard. (Ex-1011, 8; *see* Ex-1003, ¶209.) This renders claim 22 borderline inherent and certainly obvious.

Second, when "there are a finite number of identified, predictable solutions, a [POSITA] has good reason to pursue the known options within his or her technical grasp." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007). Given Aoyama's planarization, a POSITA would have recognized a design need to form etch stopper film 145 and inter-layer dielectric film 132 in a limited space between the substrate surface and the top of gate electrode 104. There are only two "identified, predictable solutions": etch stopper 145 is thinner than the first gate electrode, or it is not.[10] *See Uber Techs., Inc. v. X One, Inc.*, 957 F.3d 1334, 1339 (Fed. Cir. 2020) (holding two is a "finite number of identified, predictable solutions"); *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1331 (Fed. Cir. 2009) (same for three). Of those options, a silicon nitride CESL thinner than the gate electrode was known (in fact, ***expected***) and therefore within the technical grasp of a POSITA and obvious. (Ex-1003, ¶¶216-221; Ex-1016, Fig. 6; Ex-1017, 16; Ex-1025, Figs. 1-3, 5-6, 8-12; Ex-1028, Fig. 1; Ex-1023, Fig. 2.)

[10] At most, there are three options (thicker, thinner, or equal thickness), which is immaterial here.

Third, gate electrode 104 is thicker than 80 nm. (Ex-1003, ¶¶222-225.) Planarization makes gate electrodes 103 and 104 the same thickness. (Aoyama, ¶[0119], Fig. 6Q; Ex-1003, ¶224.) Conductive layer 103A is about 20 nm, and conductive layer 103B is about 60 nm, meaning gate electrode 103 (which further includes layer 103C) is thicker than 80 nm. (Aoyama, ¶[0107]; Ex-1003, ¶224.) A POSITA would have understood that silicon nitride etch stopper films like Aoyama's "ha[d] a typical thickness of 20 nm" or so—much less than Aoyama's gate electrode 104. (Ex-1035, 1; *see* Ex-1034, ¶[0317], ¶[0326], FIG. 52; Ex-1003, ¶225.) A POSITA thus would have found it obvious to make stopper film 145 thinner than gate electrode 104. *See Pfizer Inc. v. Sanofi Pasteur Inc.*, 94 F.4th 1341, 1348 (Fed. Cir. 2024) (finding obviousness where "techniques and conditions were routine such that a [POSITA] would have understood the claimed [property] to be 'typical'").

Fourth, where claimed "dimensions were known to be result-effective variables," "it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Applied Materials*, 692 F.3d 1289, 1295 (Fed. Cir. 2012) (quoted source omitted). Such dimensions are only patentable if they produce a "new and unexpected result" that differs in kind, not degree, from the prior art. *Id.* at 1297; *see In re Geisler*, 116 F.3d 1465, 1469-70 (Fed. Cir. 1997). Here, silicon nitride CESL thickness was known to affect stress. (*See generally* Ex-1035; Ex-1003,

¶228.) Implementing etch stopper film 145 to be thinner than gate electrode 104, as claimed, would have yielded no unexpected results, as the relationship between silicon nitride thickness and stress was known and predictable. (*See generally* Ex-1035; Ex-1003, ¶¶229-230.)

B. Ground 1B (Continued): Aoyama Renders Obvious Claims 11-15 and 18

1. Independent Claim 11

a. [11Pre]-[11B], [11D]-[11F], and [11H]-[11L]

Aoyama discloses features [11Pre]-[11B], [11D]-[11F], and [11H]-[11L] as discussed for [19Pre]-[19B], [19D]-[19F], and [19H]-[19L], respectively. (*Supra* §§V.A.1.a-V.A.1.c, §§V.A.1.e-V.A.1.g, §§V.A.1.i-V.A.1.m; Ex-1003, ¶79, ¶¶232-242.)

b. [11C] and [11G]

Because Aoyama discloses a gate insulating film 102 identical to the '686 Patent, Aoyama necessarily discloses both the claimed "first gate insulating film" (11[C]) and "second gate insulating film" ([11G]). (Ex-1003, ¶¶243-244; *compare* Ex-1001, 11:25-37, 29:16-24, *with* Aoyama, ¶[0106] (identical silicon oxide and hafnium silicate films).) As explained above, gate dielectric film 102 (including 102A and 102B) thus discloses the claimed "first gate insulating film" in NMOSFET region 106 and "second gate insulating film" in PMOSFET region 105. (*Supra* §V.A.1.d ([19C]), §V.A.1.h ([19G]); Aoyama, ¶[0098], ¶[0106].)

Alternatively, if part of a gate dielectric film structure may constitute a "gate insulating film," either gate dielectric film 102A or 102B alone discloses the claimed "first gate insulating film" in NMOSFET region 106, and either gate dielectric film 102A or 102B alone discloses the claimed "second gate insulating film" in PMOSFET region 105. (Ex-1003, ¶245.)

c. [11M]

Aoyama discloses the "conductive film is made of a silicon film." (Ex-1003, ¶¶246-248.) Like the '686 Patent, Aoyama's "semiconductor layer (silicide layer) 103C" comprises a "polysilicon or amorphous silicon" layer and a "Ni monosilicide (NiSi)" layer. (*Compare* Aoyama, ¶[0107], ¶[0114], *with* Ex-1001, 11:50-67, 29:41-45, 21:30-35, FIG. 8C (layers 15b and 34); *see infra* §V.B.1.d ([11N]); Ex-1003, ¶246.) The silicon portion of layer 103C constitutes the "conductive film" of claim 11. (*Supra* §V.A.1.i ([19H]).) "[T]he gate resistance of [Aoyama's] PMOSFET is relatively low" because of layer 103C, indicating its constituent layers are conductive. (Aoyama, ¶[0121]; *see* Ex-1003, ¶248.) Likewise, a POSITA would have understood such silicon films are conductive in gate electrodes. (Aoyama, ¶[0007]; Ex-1003, ¶¶247-248.)

d. [11N]

Aoyama discloses "the semiconductor device further comprises a metal silicide film formed on the silicon film." (Ex-1003, ¶¶249-258.)

A sacrificial nickel layer 203 is formed over the entire surface, including in contact with semiconductor layer 103C in PMOSFET region 105. (Aoyama, ¶[0108], ¶[0114].) Upon annealing, "Ni monosilicide (NiSi) is formed in" semiconductor layer 103C. (*Id.* ¶[0114].)

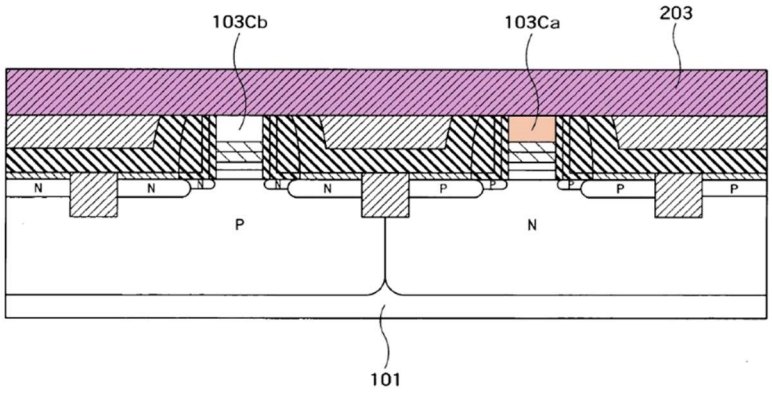


FIG. 6L

Aoyama, FIG. 6L

Thus, in Aoyama's final structure (FIG. 5), "gate electrode 103 for the PMOSFET includes … the semiconductor layer (silicide layer) 103C made of the semiconductor (silicide)." (Aoyama, ¶[0121].)

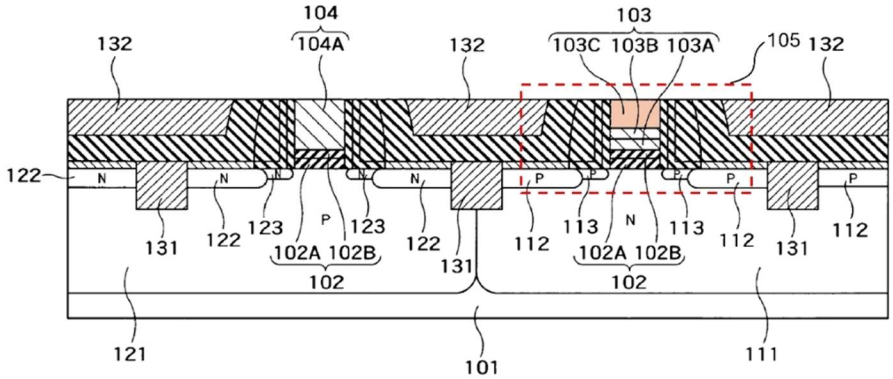


FIG. 5

Aoyama, FIG. 5

A POSITA would have recognized, or at least found obvious, that when NiSi forms "in" layer 103C, layer 103C is not entirely consumed. (Ex-1003, ¶¶252-257.) When formed, Aoyama describes layer 103C as "a semiconductor layer 103C which is made of semiconductor" (e.g., polysilicon). (Aoyama, ¶[0098]; *see id.* ¶[0107].) Then, layer 103C is silicided such that "Ni monosilicide (NiSi) is formed ***in***" layer 103C. (Aoyama, ¶[0114] (emphasis added).) In the final structure, Aoyama refers to layer 103C as "the semiconductor layer (silicide layer) 103C." (Aoyama, ¶[0121].) Because silicide forms "in" semiconductor layer 103C and Aoyama refers to layer 103C as a "semiconductor layer (silicide layer),"[11] a POSITA would have at least found obvious a silicide layer formed ***in*** the uppermost part of semiconductor layer 103C. (Aoyama, ¶[0114], ¶[0121]; Ex-1003, ¶¶253-254.) That is, a POSITA would have understood layer 103C to be a layer of, e.g., polysilicon capped by NiSi. (Ex-1003, ¶254.) The '686 Patent uses the same language to describe the silicidation of its silicon film 15b. (Ex-1001, 21:25-35 ("form a metal silicide film 34 made of nickel silicide ***in*** an upper portion of the second silicon film 15b" (emphasis added)); Ex-1003, ¶246, ¶¶255-256.)

Moreover, when only two options were available and both were known, both options would have been obvious. *See Uber*, 957 F.3d at 1339; *Perfect Web*, 587

[11] "A silicide is a metal compound[,]" not a semiconductor. (Ex-1036, 13.)

F.3d at 1331. Of the two options here (partial or complete silicidation of semiconductor layer 103C), partial silicidation was not just known but ***textbook*** and therefore obvious. (Ex-1036, FIGS. 12.9-12.10; Ex-1037, 13:39-49 ("[S]ilicon region 920 is partially silicided …. Alternatively, the entire silicon region can be silicided."), FIG. 9; Ex-1003, ¶257.)

e. [11O]

Feature [11O] would have been obvious as discussed for claim 22. (*Supra* §V.A.4; Ex-1003, ¶259.)

2. Claim 12

Aoyama discloses the features of claim 12 as discussed for claim 20. (*Supra* §V.A.2; Ex-1003, ¶260-261.)

3. Claim 13

Aoyama discloses the features of claim 13 as discussed for claim 21. (*Supra* §V.A.3; ¶262-263.)

4. Claim 14

Because Aoyama discloses a gate insulating film 102 identical to the '686 Patent, Aoyama necessarily discloses "the first and second gate insulating films are made of the same insulating material." (Ex-1003, ¶¶264-268; *see supra* §V.B.1.b.) Aoyama's gate dielectric film 102 in PMOSFET region 105 is made from the same silicon oxide dielectric film 102A and hafnium silicon oxynitride dielectric

film 102B as gate dielectric film 102 in NMOSFET region 106. (*Supra* §V.B.1.b ([11C] and [11G]); Aoyama, ¶[0106], ¶[0109]; Ex-1003, ¶¶265-268.)

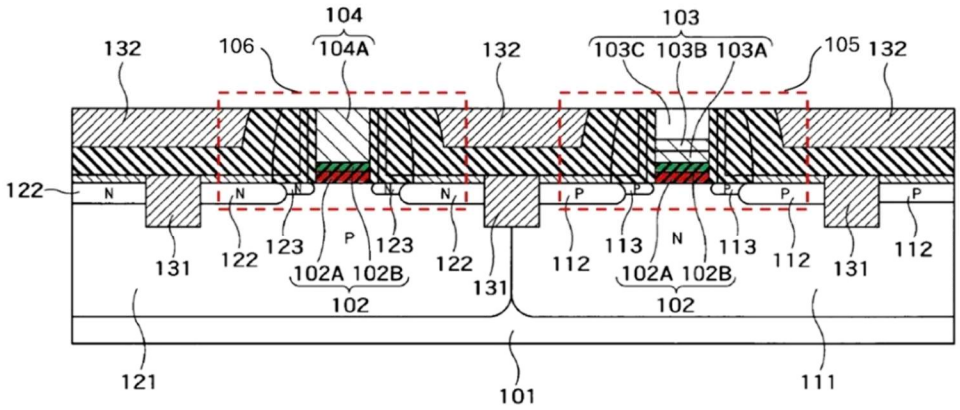


FIG. 5

Aoyama, FIG. 5

5. Claim 15

If part of a gate dielectric film structure may constitute a "gate insulating film," Aoyama's dielectric film 102A may be mapped to the claimed "first gate insulating film," and Aoyama's dielectric film 102B may be mapped to the claimed "second gate insulating film" (or vice versa). (*Supra* §V.B.1.b ([11C] and [11G]).) Under such a mapping, Aoyama's "gate insulating films are made of different insulating materials"—the silicon oxide of gate dielectric film 102A for one and the hafnium silicon oxynitride of gate dielectric film 102B for the other. (Aoyama, ¶[0106]; Ex-1003, ¶¶269-275.)

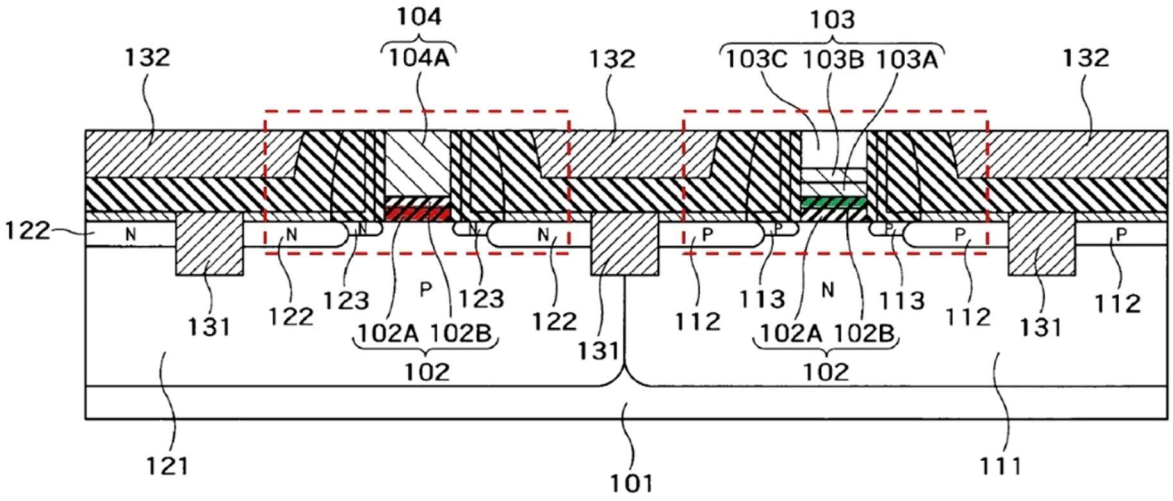


FIG. 5

Aoyama, FIG. 5

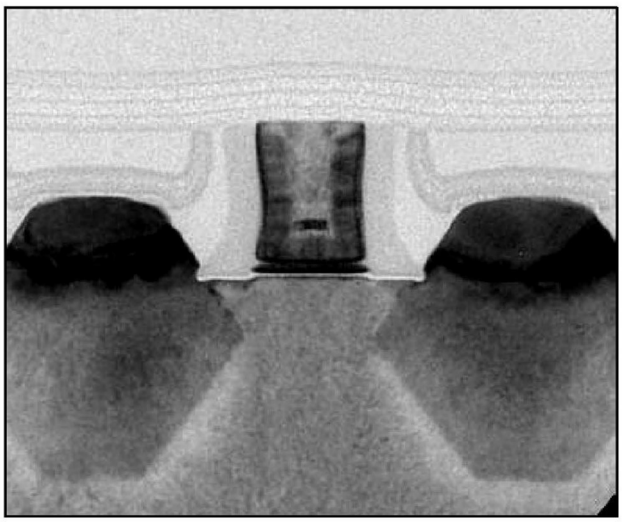
6. Claim 18

Aoyama's "gate insulating films" both "include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more"—dielectric film 102B. (*Supra* §V.B.1.b ([11C] and [11G]); Ex-1003, ¶¶276-282.) Dielectric film 102B is a "high-permittivity [high-k] dielectric film" made of "hafnium silicon oxynitride." (Aoyama, ¶[0098], ¶[0106].) According to the '686 Patent, this is "a high-k film made of a metal oxide having a relative dielectric constant of 10 or more." (Ex-1003, ¶¶280-282; *see* Ex-1014, ¶[0004] (explaining "$HfSiO_x$ … and oxynitrides thereof" have "dielectricity of more than ten"); Ex-1011, 8; Ex-1015, ¶[0002], ¶[0008]; *supra* §II.B.)

C. Ground 1C: Aoyama and Hsu823 Render Obvious Claims 1-3, 5-10, 16-17, 23-28, and 30-35

1. A POSITA would have found it obvious to implement SiGe stressors in Aoyama's source/drain regions

SiGe stressors were known and used to improve three generations of mass-production devices before the '686 Patent; it was standard industry practice and well known. (*Supra* §II.D; Ex-1003, ¶¶283-284; Ex-1038, 6:27-31.) In fact, Intel had publicly described its 45nm process (see below), which was like Aoyama's process but with epitaxial SiGe added to the PMOSFETs (see below). (Ex-1016, Fig. 6; Ex-1017, 14-28; Ex-1003, ¶¶285-295.) This alone confirms the obviousness of the asserted combination. (Ex-1003 ¶¶283-296.)



Ex-1016, Fig. 6

Further, Hsu823 likewise discloses epitaxial "SiGe stressors 218" grown in trenches to compressively stress the channel. (Hsu823, ¶[0033].) The image on the left below illustrates source/drain regions 220 "formed by implanting impurities," as

in Aoyama. (Hsu823, ¶[0032], FIG. 7A.) The image on the right illustrates another approach—"epitaxially grown" SiGe stressors 218. (Hsu823, ¶¶[0032]-[0033].)

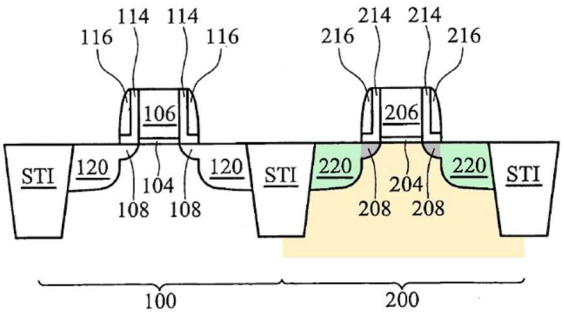


FIG. 7A

Hsu823, FIG. 7A

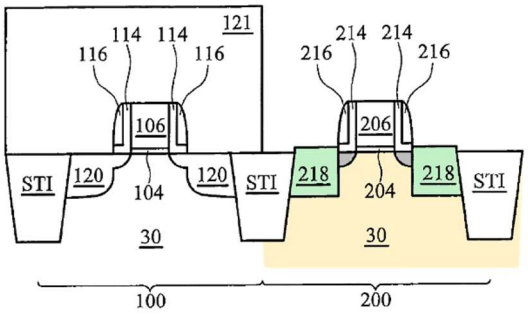


FIG. 7B

Hsu823, FIG. 7B

A POSITA would have found it obvious to modify Aoyama's PMOSFET by replacing PMOSFET source/drain regions 112 with epitaxial SiGe stressors, as Hsu823 discloses. (Hsu823, ¶¶0032]-[0033], FIGS. 7A-7B; Ex-1003 ¶¶297-298.) A POSITA would have been motivated to do so since SiGe stressors were known to increase hole mobility, thereby boosting drive current and operating speed. (*Supra* §II.D; Hsu823, ¶¶[0002]-[0003], ¶[0033]; Ex-1003, ¶299.) And a POSITA would have reasonably expected to succeed because such SiGe layers were known and widely used to induce compressive stress in PMOSFETs. (*Supra* §II.D; Ex-1003, ¶300.)

The structure in Aoyama's FIG. 6I is materially the same as the structure in Hsu823's FIG. 7A. (Ex-1003, ¶300; *see* Aoyama, ¶¶[103]-[0111], FIG. 6I; Hsu823, ¶¶[0028]-[0032], FIG. 7A.) Hsu823 teaches that SiGe source/drain regions may be

readily integrated into such a structure to boost PMOS performance. (Hsu823, ¶¶[0032]-[0033]; Ex-1003, ¶300.) Thus, as Figure A shows, a POSITA would have known the process steps Hsu823 describes regarding Figure 7B readily integrate into Aoyama's process at FIG. 6I with the ordinary and expected result: boosted PMOSFET performance. (Hsu823, ¶[0033]; *supra* §II.D; Ex-1003, ¶300.)

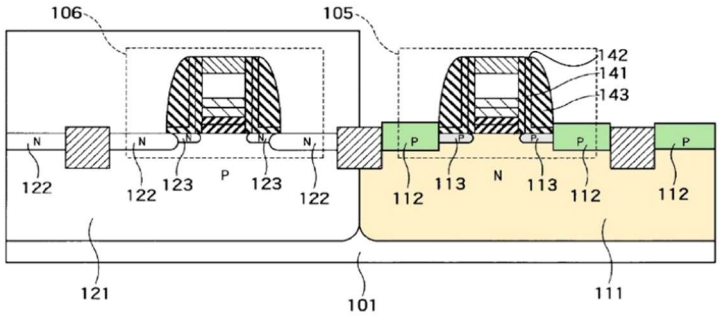


Figure A (Aoyama's FIG. 6I, modified)

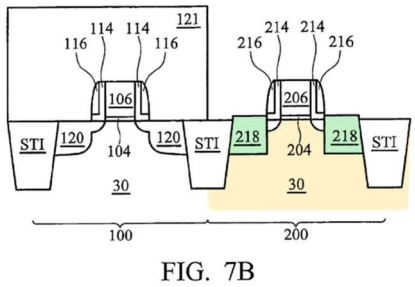


FIG. 7B

Hsu823, Fig. 7B

Figure B below illustrates Aoyama's FIG. 5, modified to include such SiGe stressors. (Ex-1003, ¶301; Hsu823, ¶[0033], FIG. 7B; Aoyama, FIG. 5; Ex-1038, 6:27-31, FIGS. 3-10; Ex-1016, Fig. 6; Ex-1017, 14-28.)

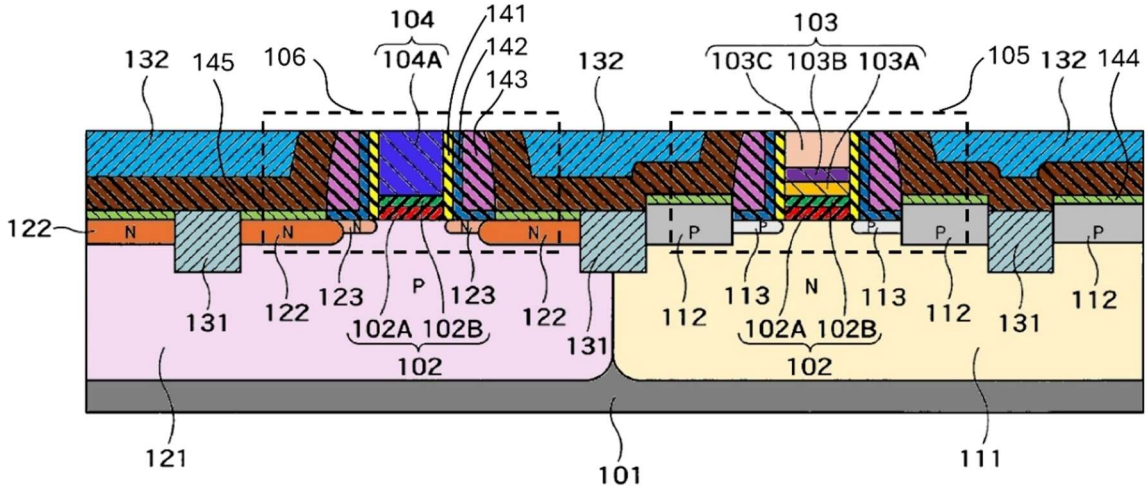


Figure B (Aoyama's FIG. 5, modified)

2. Independent Claim 1

a. [1Pre]-[1A], [1C]-[1J], and [1L]-[1M]

Aoyama discloses features [1Pre]-[1A], [1C]-[1G], [1I]-[1J], and [1L]-[1M] as discussed for [19Pre]-[19A], [19C]-[19J], and [19K]-[19L], respectively. Combining Hsu823 with Aoyama does not materially affect that analysis. (Ex-1003, ¶78, ¶¶302-313.)

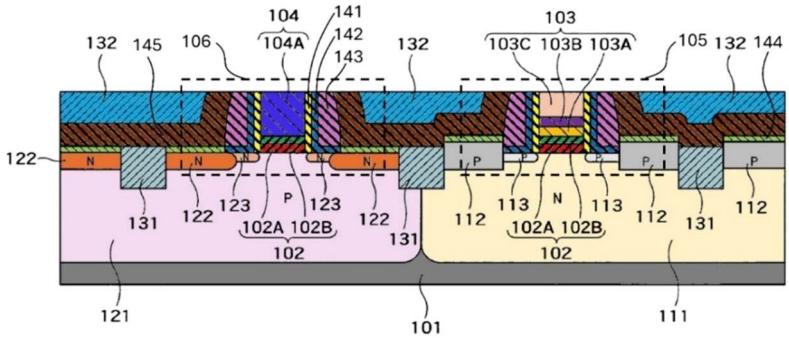


Figure B

b. [1B]

The Aoyama-Hsu823 combination includes "a second MIS transistor"—a PMOSFET (105), modified to include SiGe stressors as Hsu823 discloses. (*Supra* §V.C.1; Aoyama, ¶[0106]; Hsu823, ¶[0033], FIG. 7B; Ex-1003, ¶¶314-316.)

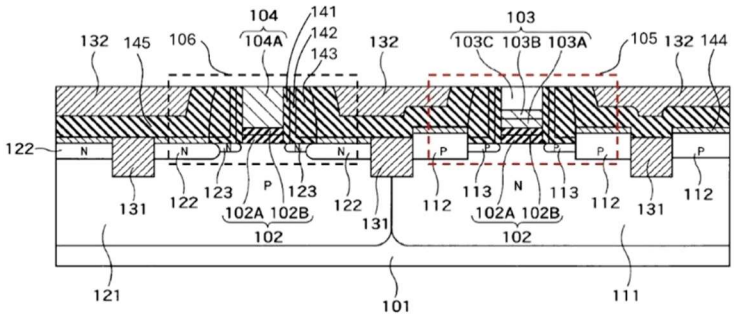


Figure B

c. [1K]

In the Aoyama-Hsu823 combination, the second MIS transistor (PMOSFET) includes "source/drain regions formed in the second active region laterally outside the second sidewall spacers." (*Supra* §V.C.1; Ex-1003, ¶¶317-321.) Hsu823 explains: "Recesses are formed in substrate … along the outside edges of the spacers" by etching. (Hsu823, ¶[0033].) "SiGe stressors … are then formed in the recesses" and "doped [by boron] during the epitaxial growth." (*Id.*; *see id.*, FIG. 7B.) In this process—the same process a POSITA would have applied to Aoyama's PMOSFETs (*supra* §V.C.1)—source/drain regions (SiGe stressors) are formed in the pFET active region laterally outside the PMOSFET sidewall spacers. (Ex-1003, ¶¶318-320.) As Figure B shows, the PMOSFET includes source/drain regions (SiGe stressors, green) formed in the active region (PMOSFET active region 105) laterally outside sidewall spacers 142 (blue). (Ex-1003, ¶321.)

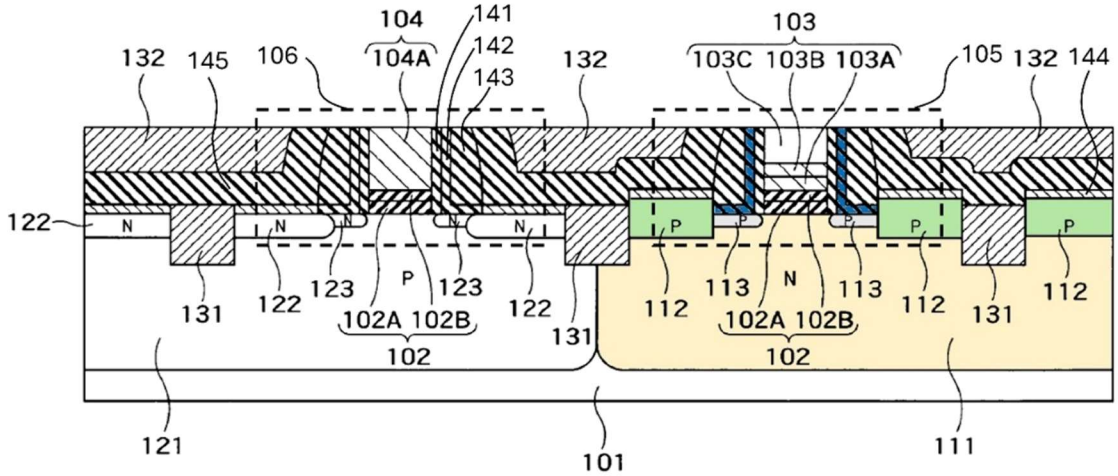


Figure B

d. [1N]

In the Aoyama-Hsu823 combination, "the source/drain regions include a silicon mixed crystal layer which is formed in trenches provided in the second active region, and causes first stress in a gate length direction of a channel region in the second active region." (Ex-1003, ¶¶322-325.)

A POSITA would have found it obvious to implement SiGe stressors as PMOSFET source/drain layers 112. (*Supra* §V.C.1.) A POSITA would have understood such SiGe stressors are "a silicon mixed crystal layer which is formed in trenches provided in" the PMOSFET active region because they comprise a mixture of silicon and germanium "epitaxially grown" (i.e., as a crystal) in "[r]ecesses [that] are formed … along the outside edges of the spacers." (Hsu823, ¶[0033]; Ex-1003, ¶324.) A POSITA also would have recognized such SiGe stressors "cause[] … stress in a gate length direction of a channel region in the … [PMOSFET] active region." (*See* Hsu823, ¶[0033] (SiGe stressors "introduce[] compressive stress[] in the … channel region[] of the resulting PMOS device"); *supra* §II.D; Ex-1003, ¶325.)

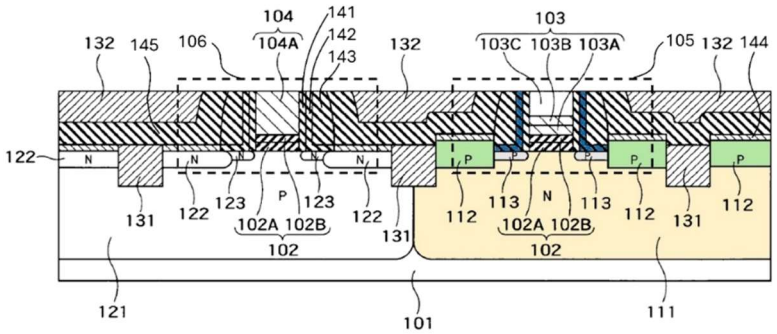


Figure B

e. [1O]

Features [1O] would have been obvious as discussed for claim 22. (*Supra* §V.A.4.) Combining Hsu823 with Aoyama does not materially affect that analysis. (Ex-1003, ¶326.)

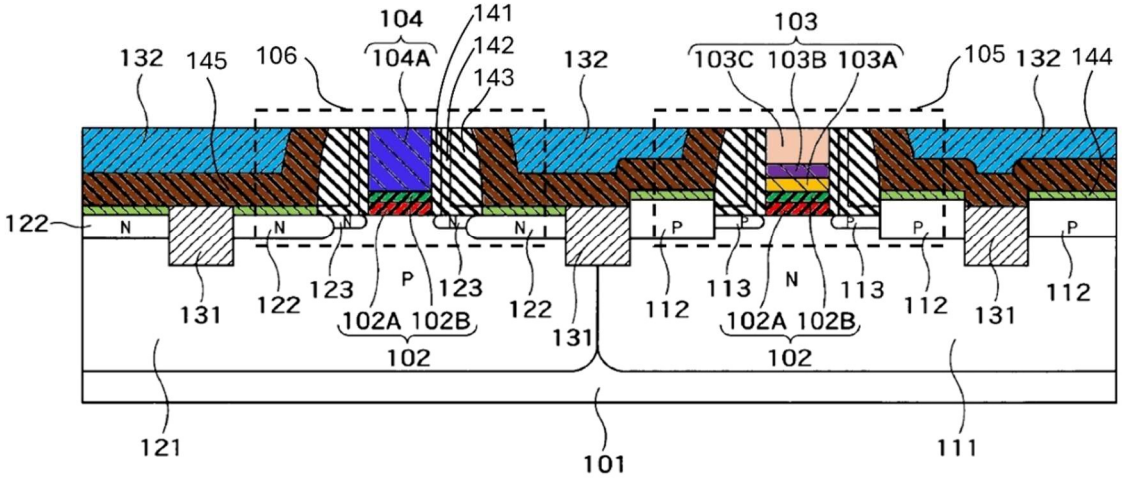


Figure B

3. Independent Claim 25

a. [25Pre]-[25L]

The Aoyama-Hsu823 combination for claim 25 only optionally includes SiGe stressors as described in Section V.C.1. Features [25Pre]-[25L] would have been obvious as discussed for [11Pre]-[11L], respectively. (*Supra* §§V.B.1.a-**Error! Reference source not found.**.) Whether SiGe stressors are present does not materially affect how the analysis of [11Pre]-[11L] applies to [25Pre]-[25L]. (Ex-1003, ¶80, ¶¶327-340.)

b. [25M]

The Aoyama-Hsu823 combination satisfies "the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region." (Ex-1003, ¶¶341-346.)

A POSITA would have been motivated to implement Aoyama's etch stopper film 145 as a tensile etch stop layer to cause tensile stress along the gate length direction of Aoyama's NMOSFET channel region. (Ex-1003, ¶¶342-345.) Aoyama's etch stopper film 145 is silicon nitride. (*Supra* §V.A.1.g ([19F]); Aoyama, ¶[0113].) Hsu823 discloses a tensile silicon nitride etch stop layer that causes stress along the gate length direction of the NMOSFET channel. (Hsu823, ¶¶[0036]-[0037] ("CESL 34 preferably ha[s] inherent tensile stress[]").) Hsu823 explains: "The performance of a MOS device can be enhanced through a stressed-surface channel." (Hsu823, ¶[0002]; *see id.* ¶[0003] ("[A] bi-axial, in-plane tensile stress field can improve NMOS performance.").) "A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device." (*Id.* ¶[0003]; *see* Ex-1028, 1-2; Ex-1031, ¶[0003]; Ex-1029, ¶[0090]; *supra* §II.D.)

A POSITA would have selected Aoyama's etch stopper layer 145 as a tensile etch stop layer for both PMOSFET and NMOSFET devices, which was well known in the art, because it provides improved NMOSFET electron mobility. (*Supra* §II.D;

Hsu823, ¶¶[0037]-[0039], FIG. 10; Ex-1027, ¶¶[0038]-[0039], FIG. 6; Ex-1028, 1-2; Ex-1030, 1-2; Ex-1023, Fig. 5(c); Ex-1003, ¶¶344-345.)

A POSITA would have reasonably expected to succeed in implementing a tensile etch stopper film 145 because such tensile CESL films were widely used to improve carrier mobility in NMOSFET devices. (*Supra* §II.D; Ex-1003, ¶346.) And it would have been well within a POSITA's ability to create such a tensile silicon nitride CESL film simply by adjusting deposition conditions. (Ex-1029, ¶[0090], ¶¶[0099]-[0100], TBL. V; Ex-1003, ¶346.)

This analysis applies regardless of whether SiGe stressors are present in the asserted combination. (Ex-1003, ¶346.)

4. Claims 2 and 26

Aoyama discloses the features of claims 2 and 26 as discussed for claim 20. (*Supra* §V.A.2; *see supra* §V.C.2, §V.C.3.) Combining Hsu823 with Aoyama does not materially affect that analysis. (Ex-1003, ¶¶347-349.)

5. Claims 3 and 27

Aoyama discloses the features of claims 3 and 27 as discussed for claim 21. (*Supra* §V.A.3; *see supra* §V.C.2, §V.C.3.) Combining Hsu823 with Aoyama does not materially affect that analysis. (Ex-1003, ¶¶350-352.)

6. Claims 5 and 30

The features of claims 5 and 30 would have been obvious as discussed for [11M] and [11N]. (*Supra* §V.B.1.c, §V.B.1.d; *see supra* §V.C.2, §V.C.3.) Combining Hsu823 with Aoyama does not materially affect that analysis. (Ex-1003, ¶¶353-355.)

7. Claims 6 and 31

Aoyama discloses the features of claims 6 and 31 as discussed for claim 14. (*Supra* §V.B.4; *see supra* §V.C.2, §V.C.3.) Combining Hsu823 with Aoyama does not materially affect that analysis. (Ex-1003, ¶¶356-358.)

8. Claims 7, 16, 23, and 33

a. A POSITA would have found it obvious to remove Aoyama's second side wall spacers

NMOSFETs and PMOSFETs in the Aoyama-Hsu823 combination include Aoyama's sidewall spacers 142 and 143, as Figure B shows. (Aoyama, ¶[0111], FIG. 5; Ex-1003, ¶364.)

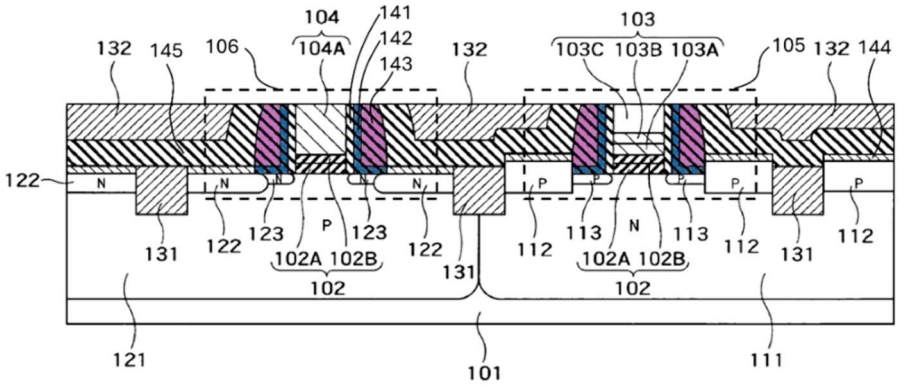


Figure B

Hsu823 likewise discloses "spacer liners" 114/214 and "spacers" 116/216, as FIG. 7B shows. (Hsu823, ¶[0031].)

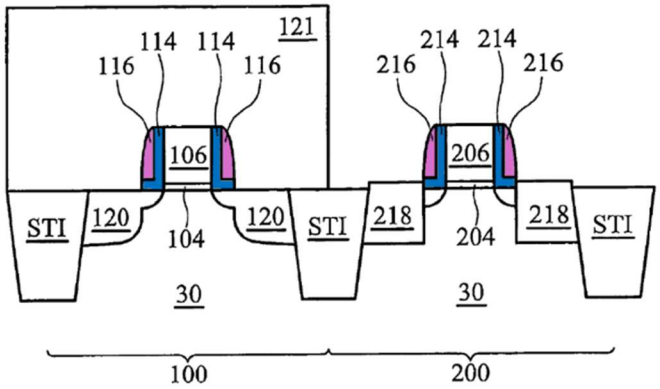
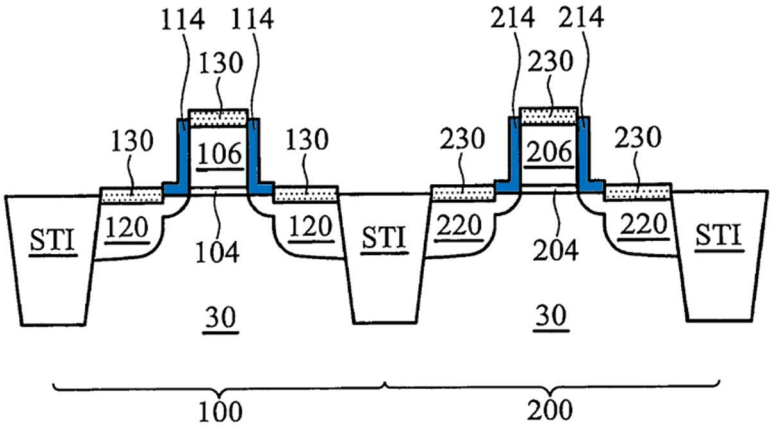


FIG. 7B

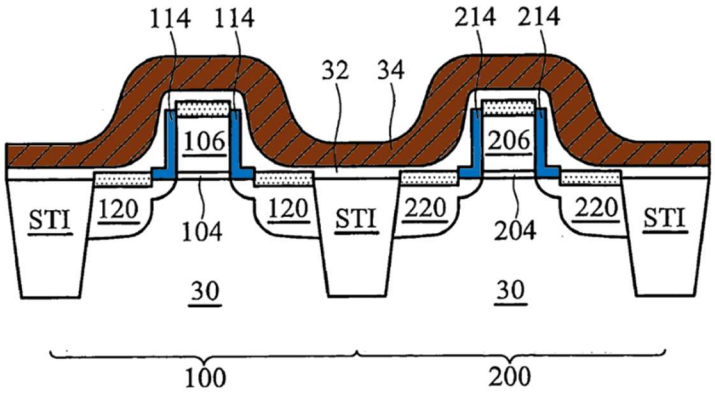
Hsu823, FIG. 7B

Hsu823 discloses removing spacers 116/216—but not spacer liners 114/214—before forming contact etch stop layer 34,[12] as FIGS. 9 and 10 illustrate. (Hsu823, ¶[0035].)



Hsu823, FIG. 9

[12] Dielectric layer 32 is "optional[]" and may be omitted. (Hsu823, ¶[0036].)



Hsu823, FIG. 10 (showing optional layer 32 to be omitted here)

Hsu823 recommends removing spacers 116/216 because it reduces the aspect ratio between gates: "With the scaling of integrated circuits, … the distance between devices decreases" and "subsequently performed gap-filling and contact etch processes suffer problems accordingly." (Hsu823, ¶[0004] (discussing "problems, such as short circuits").) By removing spacers 116/216, the aspect ratio shrinks (*see* FIGS. 15A-15B), which minimizes voids (*see* FIG. 1) and resolves such issues. (*Id.* ¶[0004], ¶¶[0042]-[0043].) Moreover, it improves stress transfer. (*Id.* ¶[0015]; Ex-1030, 836-37, Figs. 1-7; Ex-1003 ¶¶365-370.)

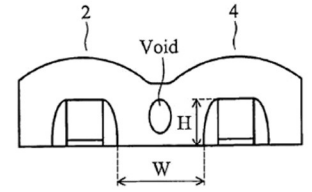


FIG. 1 (PRIOR ART)

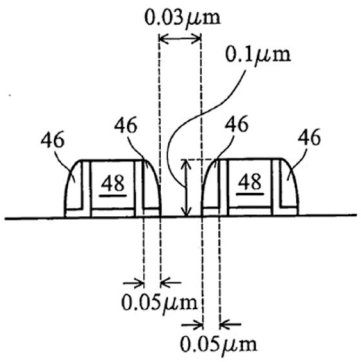


FIG. 15A

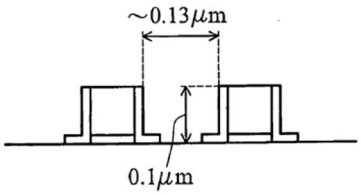


FIG. 15B

Hsu823, FIGS. 1, 15A, 15B

A POSITA thus would have found it obvious to remove sidewall spacers 143 from Aoyama's MOSFETs, leaving sidewall spacers 142. (Ex-1003, ¶¶371-377.) For instance, a POSITA would have found it obvious to remove sidewall spacers 143 just before forming etch stopper film 145 because Hsu823 teaches a direct analog: removing spacers 116/216 just before forming contact etch stop layer 34. (Hsu823, ¶¶[0035]-[0036], FIGS. 8-10; Ex-1003, ¶371.) In the resulting MOSFETs, as Figure C shows for a combination with SiGe stressors, Aoyama's etch stopper film 145 would directly contact sidewall spacers 142. (Ex-1003 ¶372.)

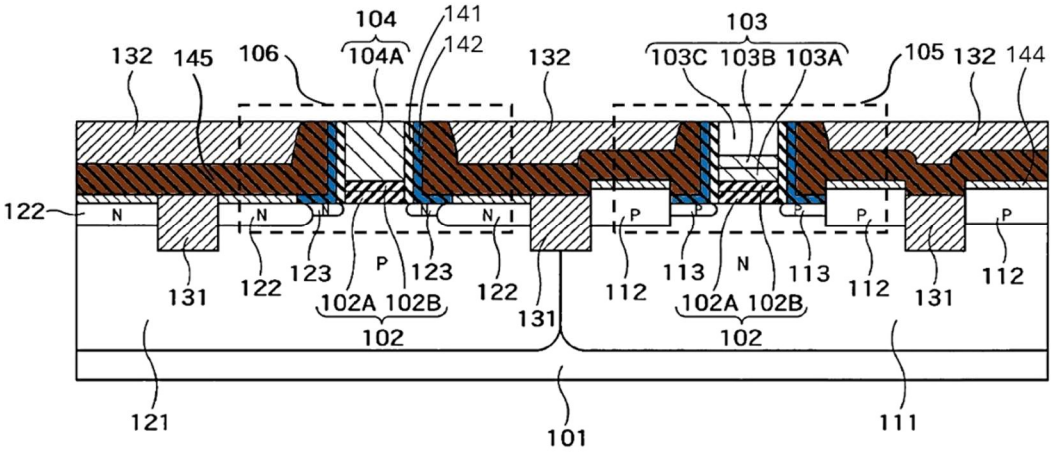


Figure C

A POSITA would have found it obvious to remove Aoyama's silicon nitride sidewall spacers 143 in this way. (Hsu823, ¶[0035]; Ex-1003, ¶373.) "The removal is preferably performed using an etchant that attacks the [sidewall spacers 143], but not the [sidewall spacers 142]." (Hsu823, ¶[0035].) Just like Hsu823, Aoyama's "[sidewall spacers 143] are formed of silicon nitride and [sidewall spacers 142] are

formed of silicon oxide." (*Id.*) Thus, "H_3PO_4 can be used to remove [sidewall spacers 143]." (*Id.*; *see* Ex-1003, ¶373.)

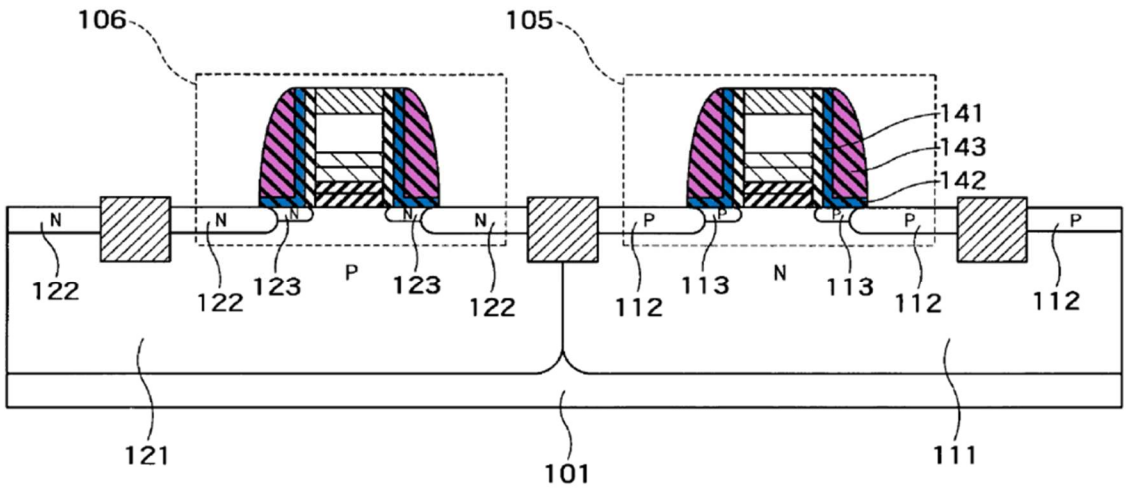


FIG. 6I

Aoyama, FIG. 6I

A POSITA would have understood this process would work equally well with Aoyama because Hsu823 and Aoyama have the same outer sidewall structures. (Ex-1003, ¶373.) Like Hsu823's sidewall spacers 114/214, Aoyama's sidewall spacers 142 are made of silicon oxide; and like Hsu823's sidewall spacers 116/216, Aoyama's sidewall spacers 143 are made of silicon nitride. (Hsu823, ¶¶[0030]-[0031], FIGS. 5-6; Aoyama, ¶[0111], FIG. 6I.) Figure D below illustrates the removal of Aoyama's sidewall spacers 143 for a combination that includes SiGe stressors. (Ex-1003, ¶373.)

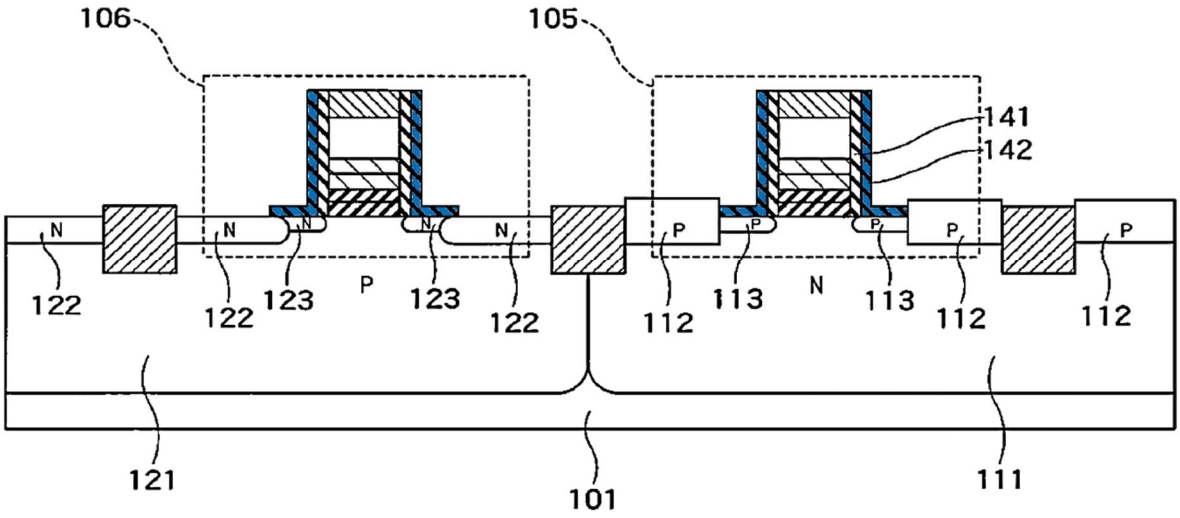


Figure D

According to the next step in Aoyama's process (*see* FIG. 6K), "etch stopper film 145 made of silicon nitride film is formed over the entire surface." (Aoyama, ¶[0113].) In a combination that includes Hsu823's SiGe stressors, the final structure would resemble Figure C. (Ex-1003, ¶374.)

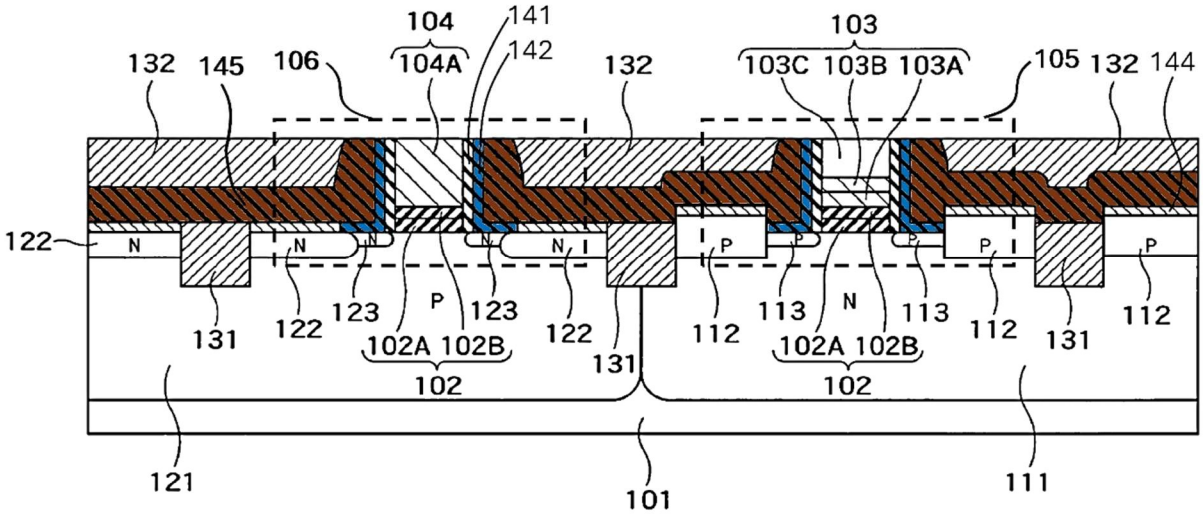


Figure C

A POSITA would have been motivated to remove Aoyama's sidewall spacers 143 to achieve the same benefits Hsu823 achieves by removing analogous spacers 116/216, i.e., reducing the aspect ratio of the gap between gates, thereby minimizing voids that cause "difficulty in subsequent processes" and "problems, such as short circuits." (Hsu823, ¶[0004]; *see id.*, FIGS. 1, 15A-15B; Ex-1003, ¶375.) It was well known that removing outer sidewalls and leaving inner L-shaped sidewalls increases packing density, simplifies gap filling, and prevents contact-to-gate shorts. (Hsu823, ¶[0004], ¶¶[0042]-[0043]; Ex-1039, Abstract, ¶¶[0018]-[0022], FIGS. 1B-1D; Ex-1003, ¶375.) Moreover, it was known to improve stress transfer. (Hsu823, ¶[0015]; Ex-1030, 1-2, Figs. 1-7; Ex-1003, ¶376.)

A POSITA would have reasonably expected to succeed at least because Hsu823 discloses that silicon nitride spacers (like Aoyama's sidewall spacers 143) can be selectively removed over silicon oxide spacers (like Aoyama's sidewall spacers 142) by using an etchant like H_3PO_4 that preferentially attacks silicon nitride. (Hsu823, ¶[0035]; Ex-1003, ¶377.)

b. Claim 7

Claim 7, which depends from claim 1 (*supra* §V.C.2), would have been obvious. In the Aoyama-Hsu823 combination, "each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and each of the second sidewall spacers is made of a second inner sidewall having an L-shaped

cross-section, and the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape." (Ex-1003, ¶¶378-380.)

A POSITA would have found it obvious to remove Aoyama's spacers 143. (*Supra* §V.C.8.a.) Upon doing so Aoyama's NMOSFET and PMOSFET would include sidewall spacers 142, each being "an inner sidewall having an L-shaped cross-section," and silicon nitride etch stop film 145 would contact surfaces of sidewall spacers 142 bent in an L-shape, as Figure C shows. (Ex-1003, ¶380.)

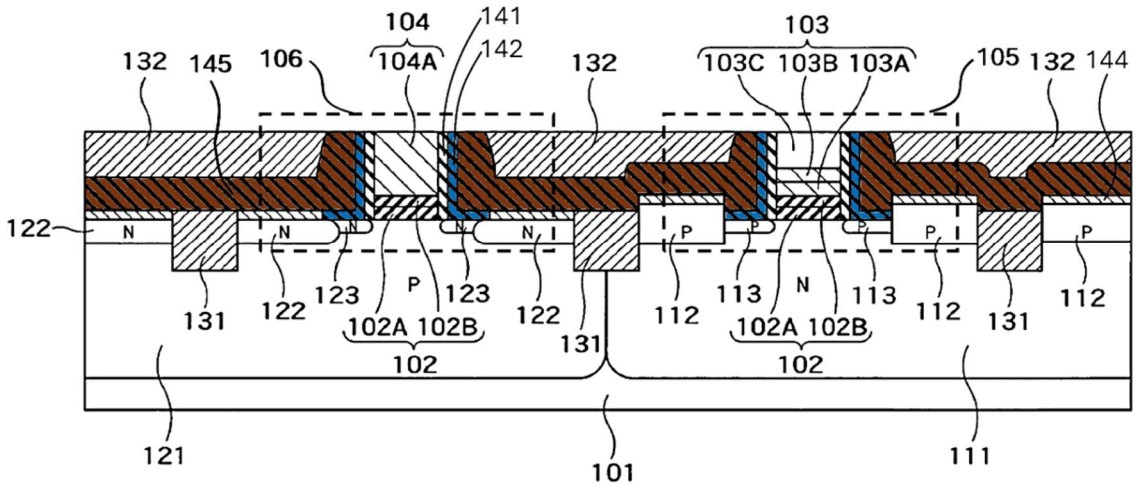


Figure C

c. Claims 16, 23, and 33

The features of claims 16, 23, and 33 would have been obvious as discussed for claim 7. (*Supra* §V.C.8; *see supra* §V.B.1, §V.A.1, §V.C.3.) Although optional for claim 33, Hsu823's SiGe stressors are not required for claims 16, 23, and 33 (*see* Figure E). (Ex-1003, ¶¶381-383.)

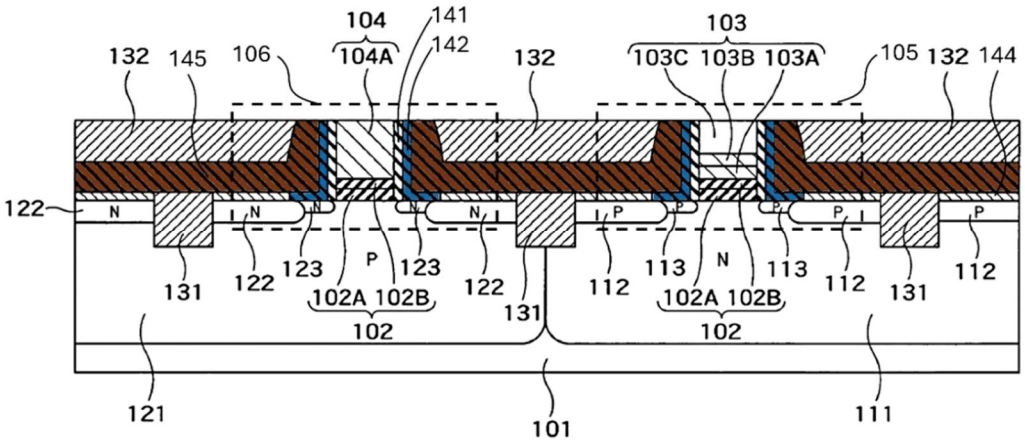


Figure E

9. Claim 8

In the Aoyama-Hsu823 combination, "the silicon nitride film causes second stress in a gate length direction of a channel region in the first active region" as discussed for [25M]. (*Supra* §V.C.3.b; *see supra* §V.C.2.) Including SiGe stressors in the Aoyama-Hsu823 combination, as claim 8 requires, does not materially affect that analysis. (*See* §V.C.1; Ex-1003 ¶¶384-386.)

10. Claim 9

In the Aoyama-Hsu823 combination, "the first MIS transistor is an n-type MIS transistor, and the second stress is tensile stress." (Ex-1003, ¶¶387-389.) As explained for claim 8, a POSITA would have found it obvious use a tensile etch stopper film 145 (second stress) to improve electron mobility in NMOSFET devices (first MIS transistor). (*Supra* §II.D; Hsu823, ¶[0003], ¶¶[0037]-[0039], FIG. 10; Ex-1028, 1-2; Ex-1030, 1-2; Ex-1023, Fig. 5(c); Ex-1003, ¶389.)

11. Claim 10

In the Aoyama-Hsu823 combination, "the second MIS transistor is a p-type MIS transistor, the silicon mixed crystal layer is made of a SiGe layer, and the first stress is compressive stress." (Ex-1003, ¶¶390-392.)

A POSITA would have found it obvious to grow SiGe stressors (a "silicon mixed crystal layer made of a SiGe layer") in the source/drain regions of Aoyama's PMOSFET. (*Supra* §V.C.2.d ([1N]); *see supra* §V.C.2, §V.B.1.) A POSITA also would have understood those SiGe stressors compressively stress adjacent PMOSFET channel regions. (*Id.*; *supra* §II.D.) SiGe stressors "introduce[] compressive stress[] in the respective channel regions of the … PMOS device[]," such that the "device drive current[] of the … PMOS device[] [is] increased." (Hsu823, ¶[0033]; *see id.* ¶[0003], ¶[0037].)

12. Claims 17, 24 and 34

The features of claims 17, 24, and 34 would have been obvious as discussed for [1K], [1N], and claim 10. (*Supra* §V.C.2.c, §V.C.2.d, §V.C.11; *see supra* §V.C.1, §V.B.1, , §V.A.1, §V.C.3; Ex-1003, ¶¶393-396.)

13. Claim 28

The features of claim 28 would have been obvious as discussed for claim 22. (*Supra* §V.A.4; *see supra* §**Error! Reference source not found.**.) Combining Hsu823 with Aoyama does not materially affect that analysis. (Ex-1003, ¶¶397-398.)

14. Claim 32

Aoyama discloses the features of claim 32 as discussed for claim 15. (*Supra* §V.B.5; *see supra* §**Error! Reference source not found.**.) Combining Hsu823 with Aoyama does not materially affect that analysis. (Ex-1003, ¶¶399-400.)

15. Claim 35

Aoyama discloses and renders obvious the features of claim 35 as discussed for claim 18. (*Supra* §V.B.6; *see supra* §**Error! Reference source not found.**.) Combining Hsu823 with Aoyama does not materially affect that analysis. (Ex-1003, ¶¶401-403.)

D. Ground 1D: Aoyama and Hobbs Render Obvious Claim 15

Claim 15, which depends from claim 11 (*supra* §V.B.1), would have been obvious. (Ex-1003, ¶¶403-418.)

1. A POSITA would have found it obvious to use different gate insulating films for NMOSFETs and PMOSFETs

A POSITA would have found it obvious to employ different gate dielectric materials for NMOSFETs and PMOSFETs. (Ex-1003 ¶¶404-416.)

The industry recognized well before the ’686 Patent that metal gate electrodes would replace polysilicon-only gate electrodes. (Hobbs, 1:50-51; *see supra* §II.C; Ex-1003, ¶405.) But, unless the gate metal has a work function close to the middle of the silicon bandgap, the same gate metal cannot be used for both NMOSFETs and PMOSFETs without disproportionately affecting the threshold voltage of one or the

other. (Hobbs, 1:53-67.) Early "efforts … focused on selecting those metals having work functions that are close to the mid band-gap of silicon." (Hobbs, 1:60-67.)

Aoyama and Hobbs take a better approach: selecting ***different*** gate metals with work functions appropriate to adjust the threshold voltages of NMOSFETs and PMOSFETs, respectively. (Aoyama, ¶¶[0009]-[0010], ¶[0066]; Hobbs, 8:37-40; *supra* §II.C.) They implement this solution using a RMG process in which a "dummy" gate is replaced with the desired gate materials near the end of device fabrication. (Aoyama, ¶[0011], FIGS. 6H-6Q; Hobbs, Figs. 4-10.)

Hobbs shows it was known to similarly replace gate dielectrics. (Ex-1003, ¶¶405-410.) As FIGS. 6-7 indicate below, Hobbs teaches to remove an nFET dummy gate dielectric, in addition to the nFET dummy gate electrode, and to replace both with materials optimized for nFETs. (Hobbs, 4:60-62.)

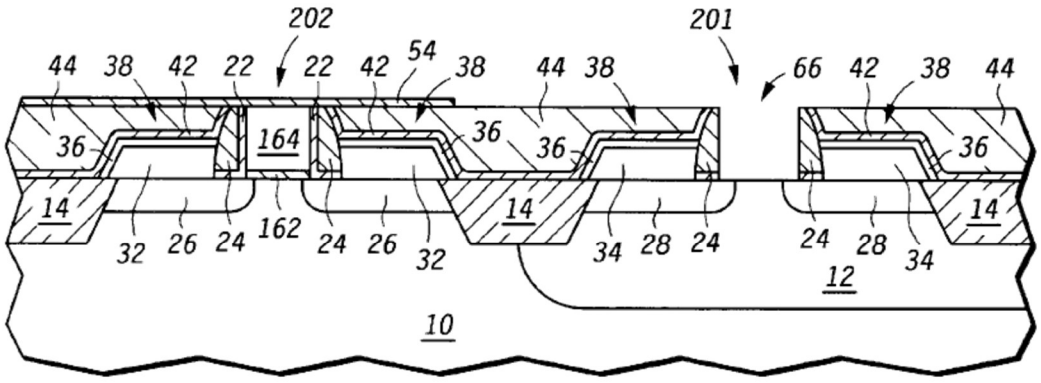


FIG.6

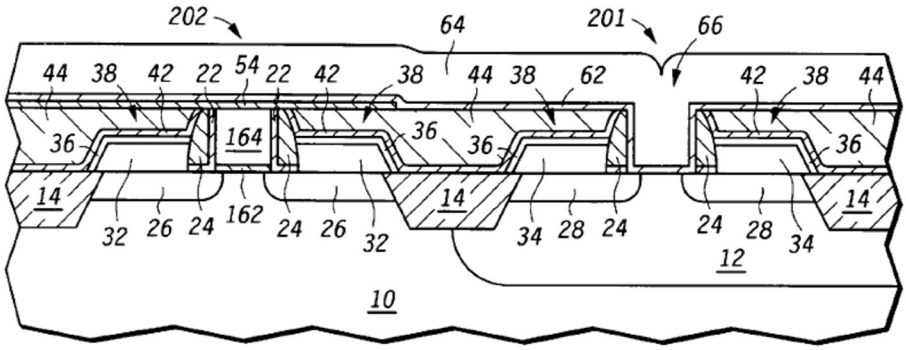


FIG. 7

Hobbs, FIGS. 6-7

As the left sides of FIGS. 8-9 indicate below, Hobbs likewise teaches to remove a pFET dummy gate dielectric, in addition to a pFET dummy gate electrode, and to replace both with materials optimized for pFETs. (Hobbs, 5:52-56.)

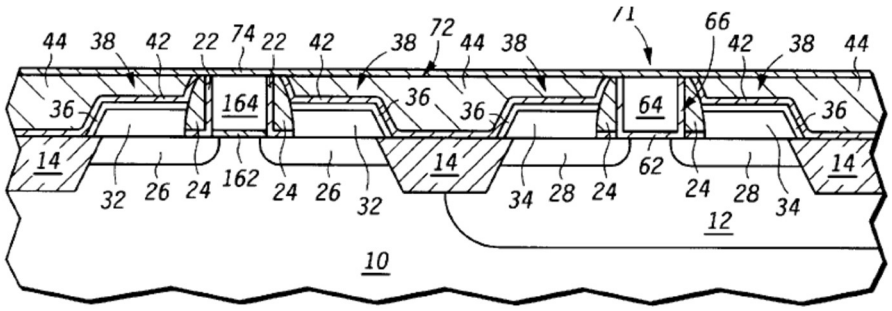


FIG. 8

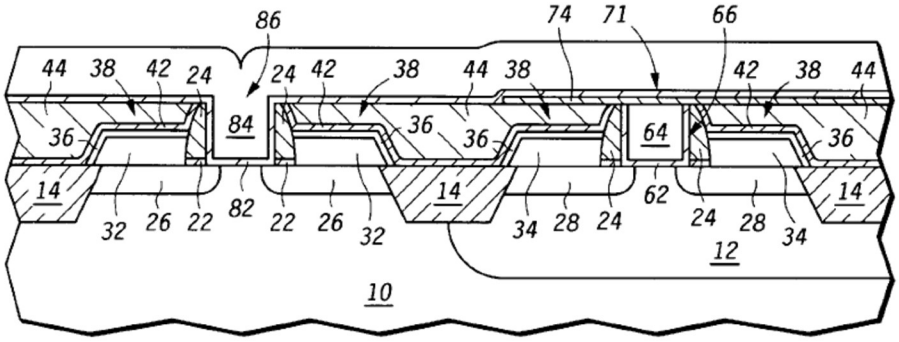


FIG. 9

Hobbs, FIGS. 8-9

Like the '686 patent, Hobbs teaches that this allows for "different gate dielectric materials and thickness as well as different gate materials [to] be selected to form a various transistors with different threshold voltages and operating characteristics." (Hobbs, 8:40-45; *see id.*, 5:66-6:5, 7:33-37; Ex-1001, 27:39-48.)

A POSITA would have understood "a single gate dielectric material may not provide the highest performance for both NMOS and PMOS structures" due to "poor band offset with conduction or valence bonds, incompatibility to the gate electrode material, incompatibility with gate electrode processing or thickness requirements." (Ex-1040, ¶[0026]; *see* Ex-1003, ¶411.) "By selecting the better candidate dielectric film for each structure, … higher performance complementary metal oxide semiconductor devices may be created …." (Ex-1040, ¶[0026].) That is, the devices "may exhibit higher mobility, higher saturation current, or better threshold voltage." (Ex-1040, ¶[0026].) For similar reasons, Hobbs teaches "the thickness and composition of the second gate dielectric and second gate electrode material can be the same ***or different*** from those of the first gate dielectric and first gate electrode material." (Hobbs, 7:65-8:2 (emphasis added); *see id.*, 5:66-6:5, 8:40-45.)

A POSITA would have understood that Hobbs's teachings equally apply to RMG devices comprising high-κ gate insulating films, such as Aoyama's MOSFETs. (Ex-1003, ¶¶411-413.) Thus, for the reasons noted above, a POSITA

would have been motivated to employ different gate dielectric films in Aoyama's NMOSFETs and PMOSFETs. (Ex-1003, ¶413.)

Moreover, a POSITA would have reasonably expected to succeed, as the successes of others indicate. (Hobbs, 7:43-47; Ex-1040, ¶¶[0016]-[0017], ¶[0019], ¶[0023], FIGS. 1-7; Ex-1041, 6:21-34, FIGS. 2B-2F; Ex-1038, 5:16-20, 5:25-30, FIGS. 10-11.) After removing Aoyama's dummy NMOSFET gate electrode (*see* Aoyama, FIG. 6O), a POSITA would have found it obvious to remove Aoyama's dielectric film 102[13] from the NMOSFET, then to form a different NMOSFET gate dielectric film such that the NMOSFET and PMOSFET gate dielectrics are uniquely tailored to each. (Ex-1003, ¶¶414-416.)

2. Claim 15

The Aoyama-Hobbs combination satisfies "wherein the first and second gate insulating films are made of different insulating materials." (Ex-1003, ¶¶417-418.) As explained above, a POSITA would have found it obvious to use different gate dielectric films for Aoyama's NMOSFET and PMOSFET devices, respectively, to improve device performance. (*Supra* §0; *see* Hobbs, 7:43-47, 7:65-8:2; Ex-1040, ¶[0019], ¶[0026]; Ex-1041, 6:21-34; Ex-1003, ¶418.)

[13] Mislabeled as "103" in FIG. 6O.

E. Ground 1E: Aoyama, Hsu823, and Hobbs Render Obvious Claim 32

Claim 32, which depends from claim 25, would have been obvious for reasons stated regarding claim 15. (*Supra* §**Error! Reference source not found.**, §V.D.) Combining Hsu823 with Aoyama and Hobbs does not change the combination's structure as it relates to claim 15. (Ex-1003, ¶¶419-420.)

F. Grounds 2A and 2B: Akasaka Anticipates or at Least Renders Obvious Claims 19-22

1. Independent Claim 19

a. [19Pre]

Akasaka discloses "[a] semiconductor device." (Akasaka, ¶[0003], ¶[0072], FIG. 26 (below); Ex-1003, ¶¶421-423.)

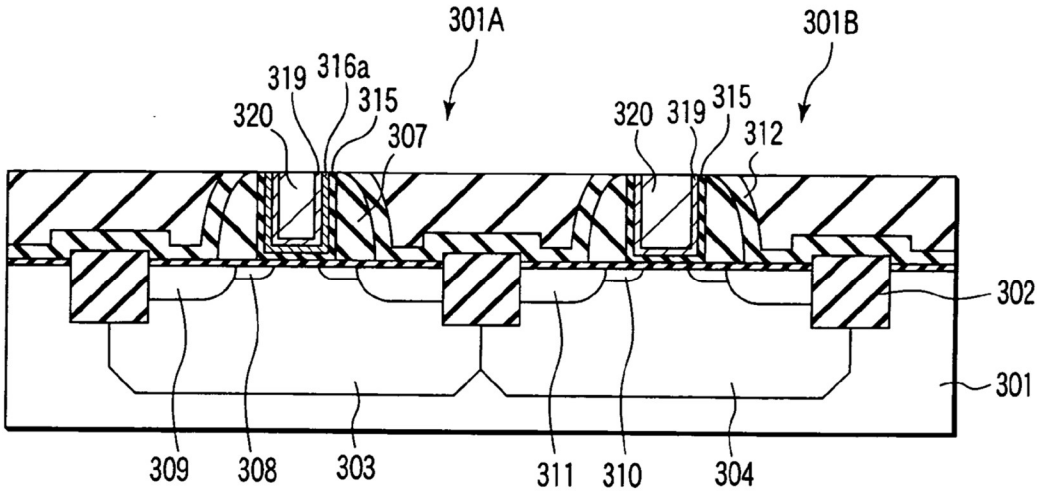


FIG. 26

Akasaka, FIG. 26

b. [19A]

Akasaka discloses "a first MIS transistor": an "n-type MISFET" (i.e., NMISFET) 301B. (Akasaka, ¶¶[0072]-[0073], FIG. 26; Ex-1003, ¶¶424-426.)

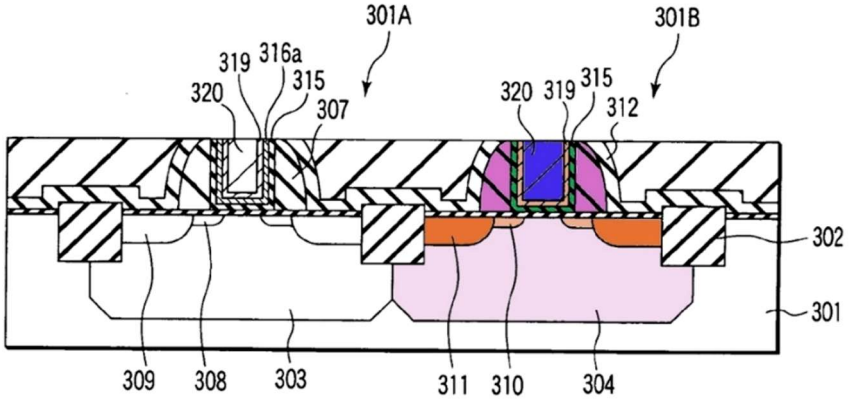


FIG. 26

Akasaka, FIG. 26

c. [19B]

Akasaka discloses "a second MIS transistor": a "p-type MISFET" (i.e., PMISFET) 301A. (Akasaka, ¶¶[0072]-[0073], FIG. 26; Ex-1003, ¶¶427-429.)

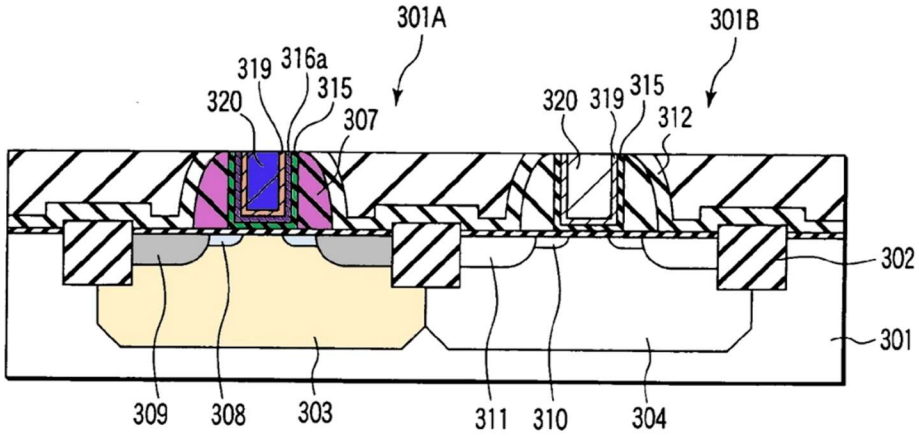


FIG. 26

Akasaka, FIG. 26

d. [19C]

Akasaka discloses the "first MIS transistor" includes "a first gate insulating film formed on a first active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon." (Ex-1003, ¶¶430-433.)

Akasaka's NMISFET includes a "gate dielectric (insulating) film 315" formed of $HfSi_xO_y$, which is an "oxide containing hafnium and silicon." (Akasaka, ¶[0075].) A POSITA would have recognized this is "a high-k film." (Ex-1003, ¶431; *see* Ex-1014, ¶[0004] (explaining "$HfSiO_x$ … and oxynitrides thereof" are "high dielectric constant film[s]").) Gate dielectric film 315 is "depos[it]ed all over the substrate[301]," including area 301B (first active region) "for forming … an n-type MISFET." (Akasaka, ¶¶[0072]-[0073]; *see id.*, FIG. 26; Ex-1003, ¶432.)

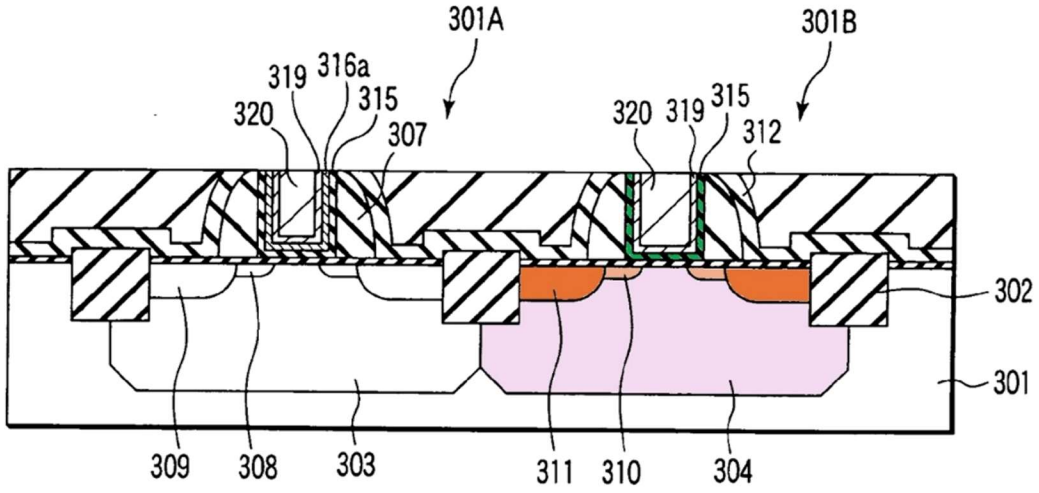


FIG. 26

Akasaka, FIG. 26

e. [19D]

Akasaka discloses the "first MIS transistor" includes "a first gate electrode including a second metal film formed on the first gate insulating film." (Ex-1003, ¶¶434-437.) Akasaka's NMISFET gate electrode comprises conductive films 319 and 320. (Akasaka, ¶¶[0084]-[0086], FIG. 26.) Conductive film 319 may be "a [Group-IVa, Group-Va, or Group-VIa] pure metal, … a metal silicide, a metal nitride, or another compound … as long as it has a metallic band structure with a work function close to that of n^+-poly-crystalline silicon," and conductive film 320 may be tungsten, also a metal. (Akasaka, ¶¶[0085]-[0086].) Either or both conductive films 319 and 320 disclose the claimed "second metal film."

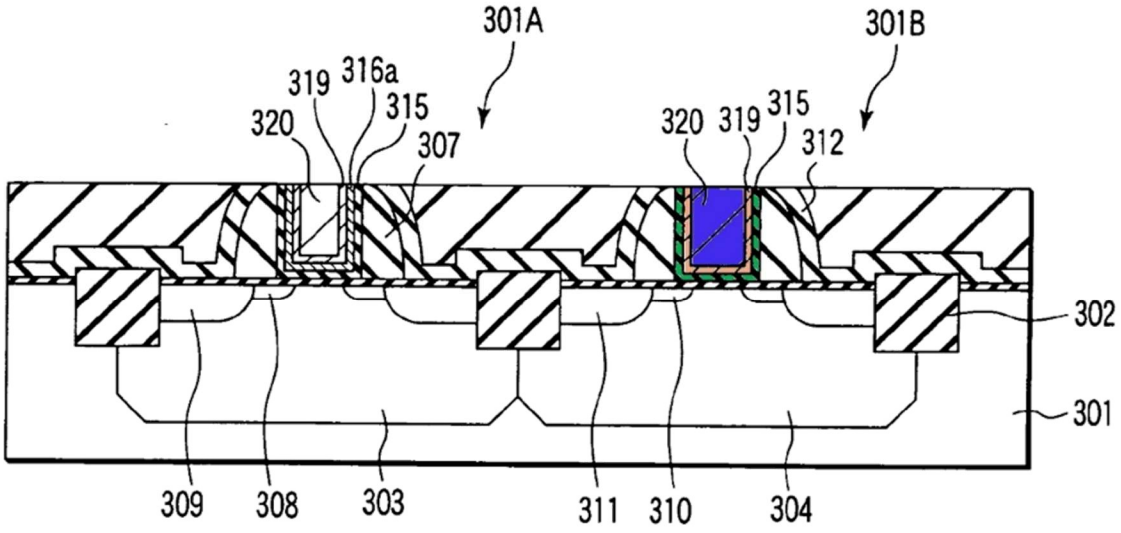


FIG. 26

Akasaka, FIG. 26

f. [19E]

Akasaka discloses the "first MIS transistor" includes "first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative." (Ex-1003, ¶¶438-440.)

Akasaka discloses "gate sidewall[s] 307" (first sidewall spacers) "formed of an insulating film, such as … silicon nitride." (Akasaka ¶[0073].) As FIG. 26 shows, gate sidewalls 307 (pink) are formed on side surfaces of the first gate electrode. (Ex-1003, ¶439.)

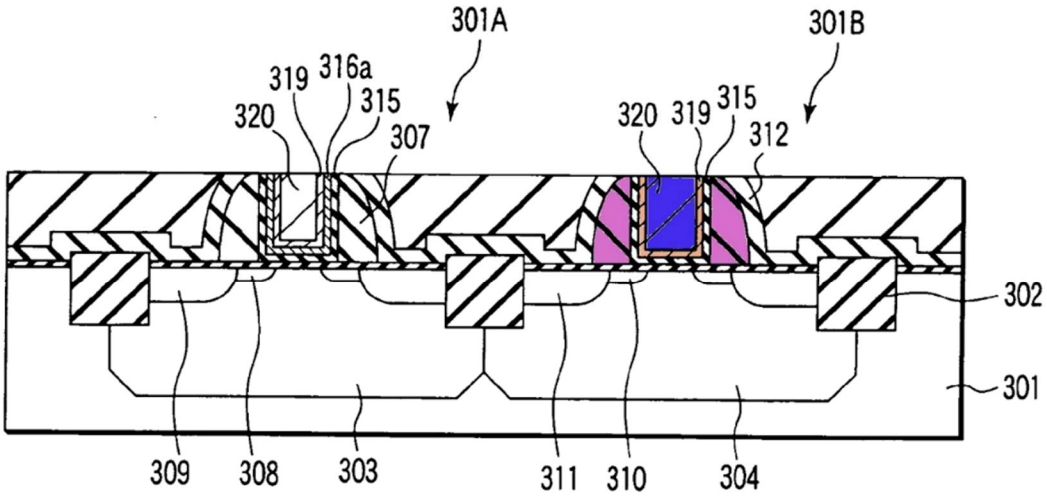


FIG. 26

Akasaka, FIG. 26

g. [19F]

Akasaka discloses the "first MIS transistor" includes "a silicon nitride film [silicon nitride film 312] formed, extending over the side surfaces of the first gate electrode [NMISFET gate electrode] on which the first sidewall spacers [gate

sidewalls 307] are formed and upper surfaces of regions [source/drain layers 311] located in the first active region [area 301B] laterally outside the first sidewall spacers," as FIG. 26 shows. (Akasaka, ¶¶[0072]-[0073]; Ex-1003, ¶¶441-445.) The gate electrode structure and its sidewalls 307 "are covered with silicon nitride film 312 serving as an etching stopper." (Akasaka, ¶[0073], FIG. 16.) Then, silicon nitride film 312 is polished by CMP to expose the upper surfaces of the gate electrode structures. (*Id.* ¶[0074], ¶[0087].)

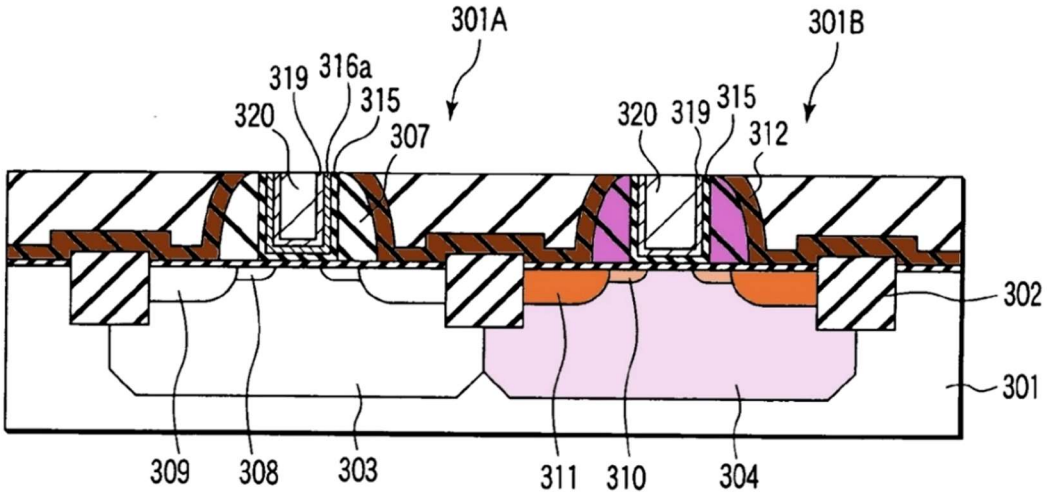


FIG. 26

Akasaka, FIG. 26

h. [19G]

Akasaka discloses the "second MIS transistor" includes "a second gate insulating film formed on a second active region in the semiconductor substrate, and including a second high-k film made of oxide containing hafnium and silicon." (Ex-1003, ¶¶446-449.)

Akasaka's PMISFET includes a "gate dielectric (insulating) film 315" formed of $HfSi_xO_y$, which is an "oxide containing hafnium and silicon." (Akasaka ¶[0075].) A POSITA would have recognized this is "a high-k film." (Ex-1003, ¶447; *see* Ex-1014, ¶[0004] (explaining "$HfSiO_x$ … and oxynitrides thereof" are "high dielectric constant film[s]").) Gate dielectric film 315 is "depos[it]ed all over the substrate[301]," including area 301A (second active region) "for forming a p-type MISFET." (Akasaka, ¶¶[0072]-[0073]; *see id.*, FIG. 26; Ex-1003, ¶448.)

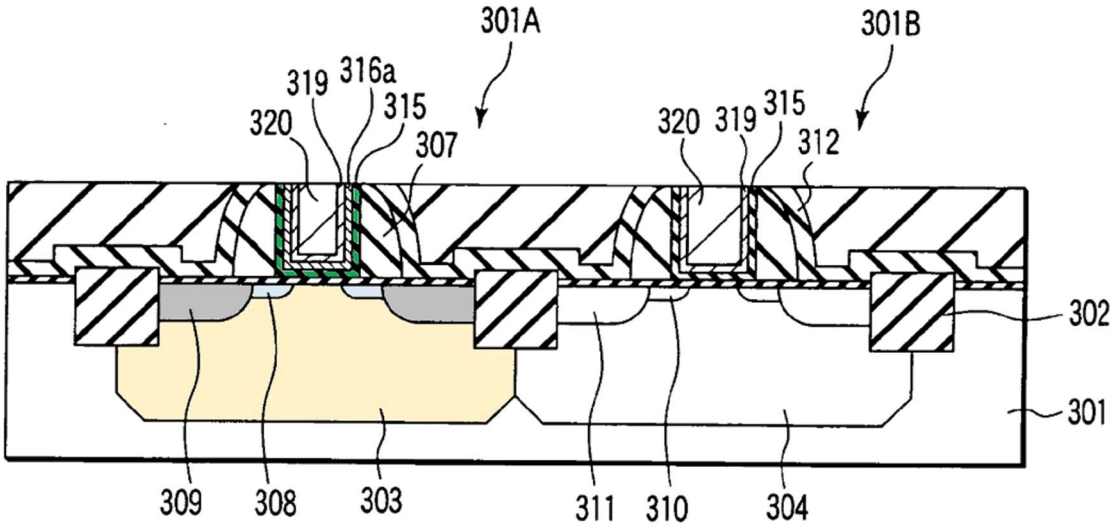


FIG. 26

Akasaka, FIG. 26

i. [19H]

Akasaka discloses the "second MIS transistor" includes "a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film." (Ex-1003, ¶¶450-454.)

Akasaka's PMISFET gate electrode comprises conductive films 316a, 319, and 320. (Akasaka, ¶¶[0076]-[0077], ¶[0082], ¶[0086], FIG. 26.) Conductive film 316a (first metal film) may be "a [Group-VIII] pure metal, … a metal silicide, a metal nitride, or another compound … as long as it has a metallic band structure with a work function close to that of p^+-poly-crystalline silicon." (Akasaka, ¶[0077].) Conductive film 319 may be "a [Group-IVa, Group-Va, or Group-VIa] pure metal, … a metal silicide, a metal nitride, or another compound … as long as it has a metallic band structure with a work function close to that of n^+-poly-crystalline silicon." (Akasaka, ¶[0085].) And conductive film 320 may be tungsten. (Akasaka, ¶[0086].) Either or both conductive films 319 and 320 discloses the claimed "conductive film." (Ex-1003, ¶¶451-453.)

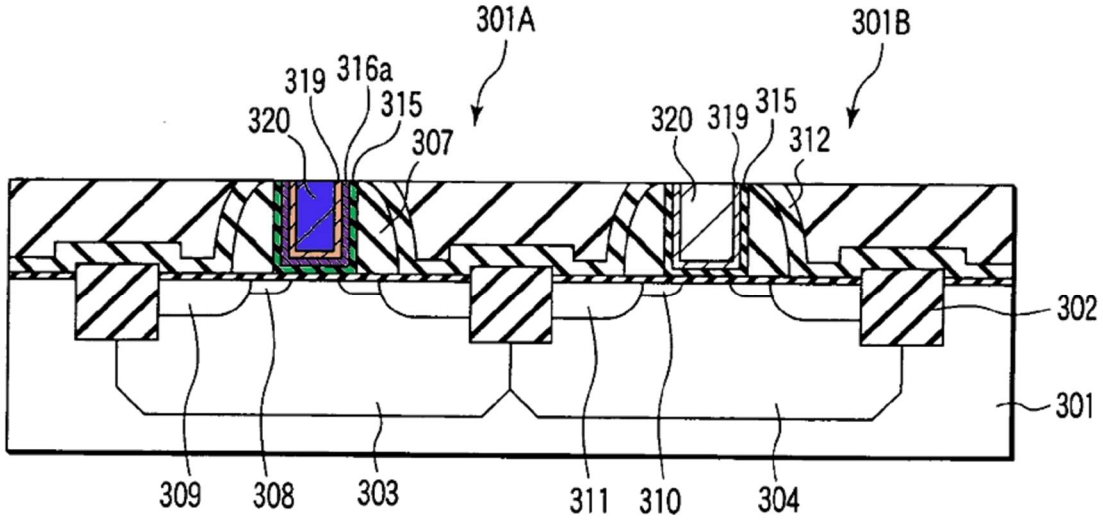


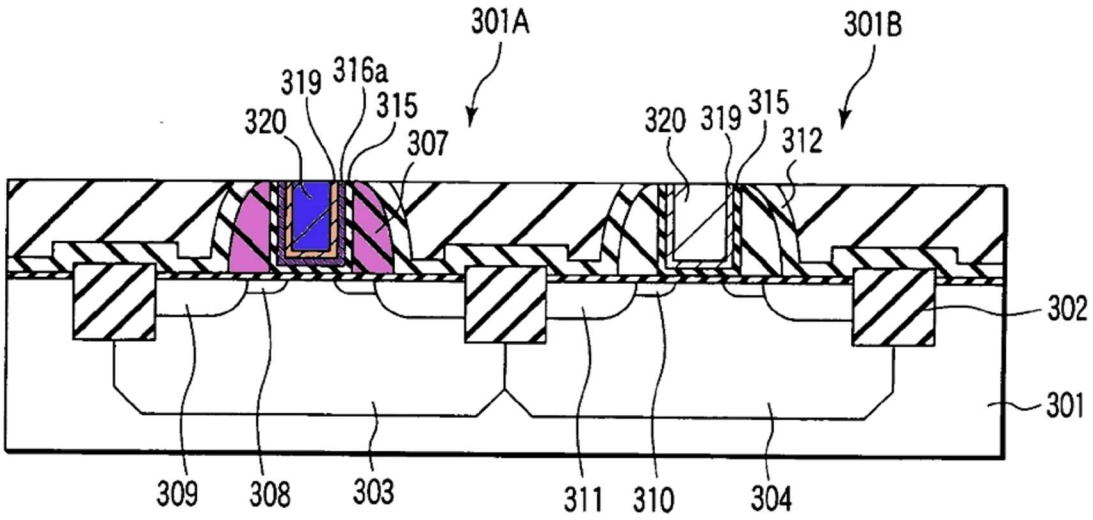
FIG. 26

Akasaka, FIG. 26

j. [19I]

Akasaka discloses the "second MIS transistor" includes "second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative." (Ex-1003, ¶¶455-457.)

Akasaka discloses "gate sidewall[s] 307" (second sidewall spacers) "formed of an insulating film, such as … silicon nitride." (Akasaka, ¶[0073].) As FIG. 26 shows, gate sidewalls 307 are formed on side surfaces of the second gate electrode). (Ex-1003, ¶456.)

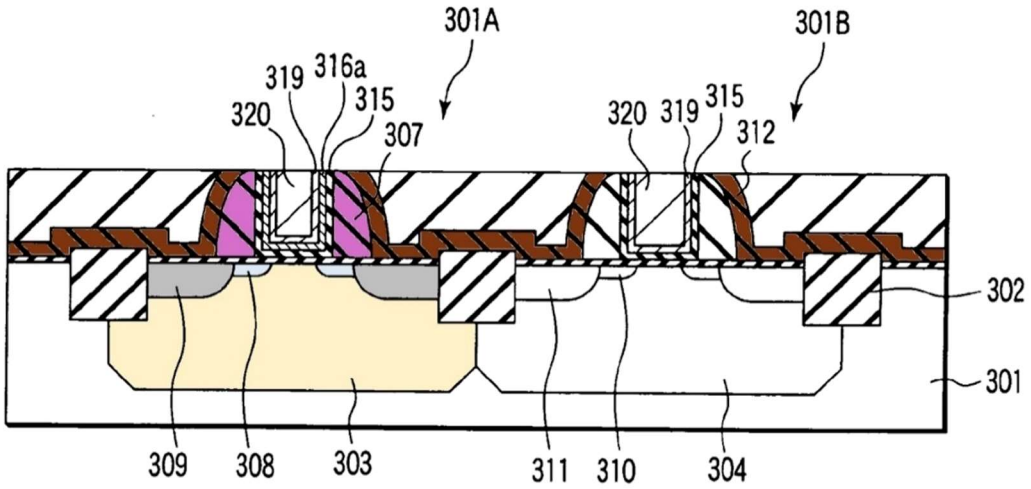


Akasaka, FIG. 26

k. [19J]

Akasaka discloses the "second MIS transistor" includes "the silicon nitride film [silicon nitride film 312] formed, extending over the side surfaces of the second gate electrode [PMISFET gate electrode] on which the second sidewall spacers [gate sidewalls 307] are formed and upper surfaces of regions [source/drain layers 309]

located in the second active region [area 301A] laterally outside the second sidewall spacers." (Akasaka, ¶¶[0072]-[0074], ¶[0087], FIGS. 16, 26; *supra* §V.F.1.g; Ex-1003, ¶¶458-462.)



Aoyama, FIG. 5

l. [19K]

Akasaka discloses "the first and second metal films are made of different metal materials." (Ex-1003, ¶¶463-467.) Either or both conductive films 319 and 320 discloses the claimed "second metal film." (*Supra* §V.F.1.e ([19D]).) The former "has a metallic band structure with a work function close to that of n^+-poly-crystalline silicon," and the latter may be tungsten. (Akasaka, ¶¶[0085]-[0086].) Conductive film 316a discloses the claimed "first metal film." (*Supra* §V.F.1.i ([19H]).) It "has a metallic band structure with a work function close to that of p^+-poly-crystalline silicon" (e.g., TiN) and is thus made of a different metal material. (*Compare* Akasaka, ¶[0077], *with* Akasaka, ¶¶[0085]-[0086].)

m. [19L]

Akasaka discloses "the silicon nitride film [silicon nitride film 312] is not formed on any of upper surfaces of the first and second gate electrodes." (Ex-1003, ¶¶468-472.) Akasaka's fabrication process ensures this.

After silicon nitride film 312 and inter-level insulating film 313 are formed over dummy gate electrodes 306, inter-level insulating film 313 is "polished from above by a CMP (Chemical Mechanical Polishing) method … to expose … the upper surface of the silicon nitride film 312." (Akasaka, ¶¶[0073]-[0074].) "[T]he exposed silicon nitride film 312 and the dummy gate electrodes are [then] selectively removed." (Akasaka, ¶[0074]; *see id.* ¶¶[0075]-[0076], ¶[0084], ¶[0086], FIGS. 19, 25.) After forming gate electrode layers 316a, 319, and 320, a second CMP ensures nothing, including silicon nitride film 312, remains on any upper surface of the gate electrodes. (*Id.* ¶[0087], FIG. 26; Ex-1003, ¶¶469-471.)

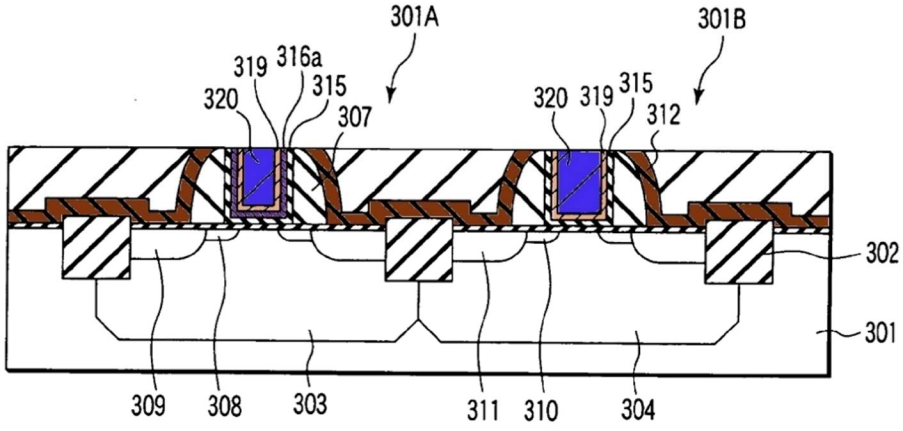


FIG. 26

Aoyama, FIG. 5

n. [19M]

Akasaka discloses "the first metal film is made of titanium nitride." (Ex-1003, ¶¶473-475.) Conductive film 316a (first metal film) may be "a titanium nitride (TiN) film." (Akasaka, ¶[0077].)

2. Claim 20

Akasaka discloses "wherein the first metal film has a thickness smaller than that of the second metal film." (Ex-1003, ¶¶476-481.) Conductive film 316a (first metal film) is preferably "about 5 nm" or "about 1 to 2 nm." (Akasaka, ¶[0077].) Conductive film 320 (second metal film) is "about 40 to 50 nm" thick. (Akasaka, ¶[0086].)

3. Claim 21

Akasaka discloses "wherein the first and second metal films have different work functions." (Ex-1003, ¶¶482-489.) Conductive film 316a (first metal film) "is preferably selected to have a work function … of 4.8 to 5.3 eV." (Akasaka, ¶¶[0076]-[0077].) Conductive film 319 (second metal film) "is preferably selected to have a work function … of 3.9 to 4.2 eV." (Akasaka, ¶¶[0084]-[0085].)

4. Claim 22

Akasaka discloses "silicon nitride film [silicon nitride film 312] has a thickness smaller than that of the first gate electrode [NMISFET gate electrode]." (Ex-1003, ¶¶490-523.)

Akasaka's FIG. 26 shows silicon nitride film 312 much thinner than the gate electrode in NMISFET region 301B. *See Koito Mfg.*, 381 F.3d at 1154-56 (finding "relative dimensions" of a patent figure sufficient disclosure of such limitation); Ex-1003, ¶¶492-493.

For essentially the same four additional reasons discussed in Section V.A.4, a POSITA also would have found claim 22 obvious. (Ex-1003, ¶¶494-523.)

The only differences between Aoyama and Akasaka regarding claim 22 are that Aoyama's gate dielectric film 102 is less than 3 nm thick, whereas Akasaka's gate dielectric film 315 is no more than about 12 nm thick[14]; and Aoyama's gate electrode is thicker than 80 nm, whereas Akasaka's gate electrode is thicker than about 41-52 nm. (Ex-1003, ¶502, ¶516; *see* Akasaka, ¶[0075] ("(EOT) of 1.5 nm or less"), ¶[0077], ¶¶[0084]-[0086].) Since these differences do not meaningfully affect the analysis in Section V.A.4, a POSITA would have found claim 22 obvious in view of Akasaka for at least the same reasons. (*See* Ex-1003, ¶494.)

Like Aoyama's NMISFET and PMISFET gate electrodes 103/104, Akasaka's NMISFET and PMISFET gate electrodes are planarized. (*Compare* Aoyama, ¶[0119], FIG. 5, *with* Akasaka, ¶¶[0073]-[0074], ¶[0087], FIG. 26.) Accordingly, as

[14] Realistically, it would be thinner, e.g., about 4 nm when κ=10. (Ex-1003, ¶502; *see* Ex-1014, ¶[0004], ¶[0043], Tbl. 1.)

in Aoyama, Akasaka's silicon nitride film 312 (brown) is thinner than the NMISFET gate electrode (*see* FIG. 26) so long as inter-level insulating film 313 (turquoise) is thicker than gate dielectric film 315 (green). (Ex-1003, ¶¶496-500.)

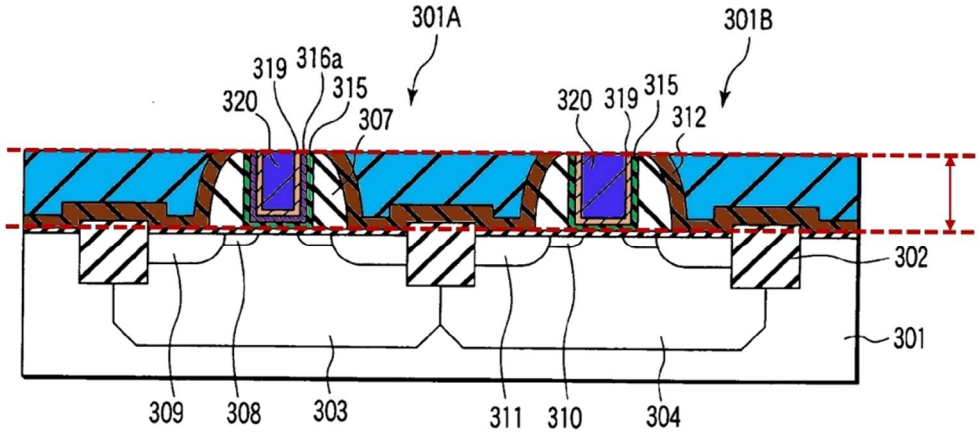


FIG. 26

Akasaka, FIG. 26

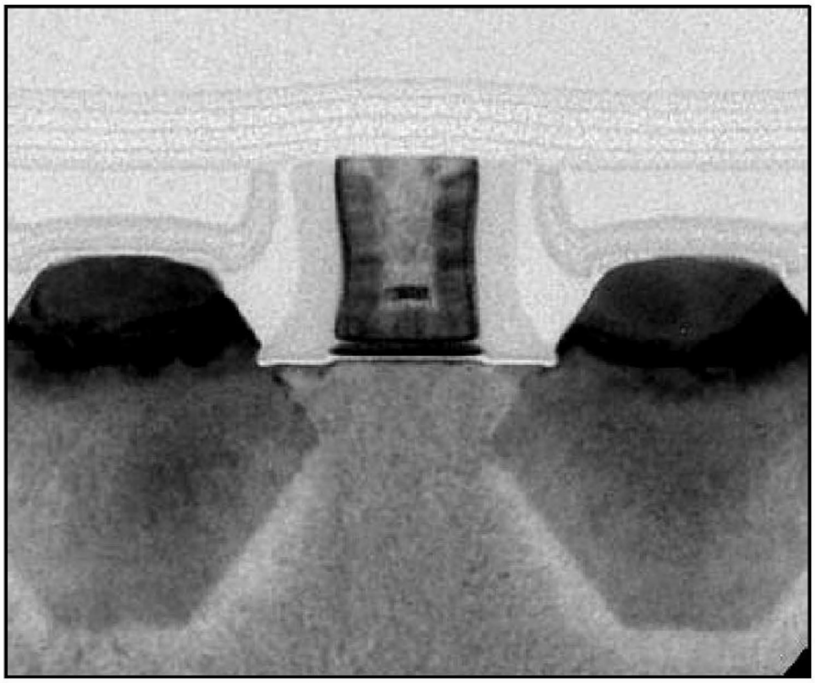
For at least the same reasons a POSITA would have found it obvious for Aoyama's interlayer dielectric 132 to be thicker than gate dielectric film 102 (*see* §V.A.4), a POSITA also would have found it obvious for Akasaka's inter-level insulating film 313 to be thicker than gate dielectric film 315 and would have found it very unusual were it otherwise. (Ex-1003, ¶¶495-507; *see id.* ¶¶494-523.)

G. Ground 2C: Akasaka and Hsu823 Render Obvious Claims 1-4, 6-10, 23-29, 31, and 33-35

1. A POSITA would have found it obvious to implement SiGe stressors in Akasaka's source/drain regions

SiGe stressors had been known and used to improve PMOS performance in three generations of mass-production devices before the '686 patent; it was standard

industry practice and well known. (*Supra* §II.D; Ex-1003, ¶¶524-525; Ex-1038, 6:27-31.) In fact, Intel had publicly described the process flow for its 45nm process, which was like Akasaka's process but with epitaxial SiGe added to the PMISFETs (see below). (Ex-1016, Fig. 6; Ex-1017, 14-28; Ex-1038, 6:27-31; Ex-1003, ¶¶526-537). This alone confirms the obviousness of the asserted combination. (Ex-1003, ¶¶525-538.)



Ex-1016, Fig. 6

Further, Hsu823 likewise discloses epitaxial "SiGe stressors 218" grown in trenches to compressively stress the channel. (Hsu823, ¶[0033].) The image on the left below illustrates source/drain regions 220 "formed by implanting impurities," as in Akasaka. (Hsu823, ¶[0032], FIG. 7A.) The image on the right illustrates another approach—"epitaxially grown" SiGe stressors 218. (Hsu823, ¶¶[0032]-[0033].)

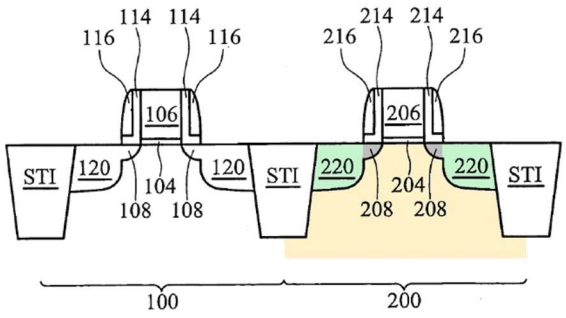


FIG. 7A

Hsu823, FIG. 7A

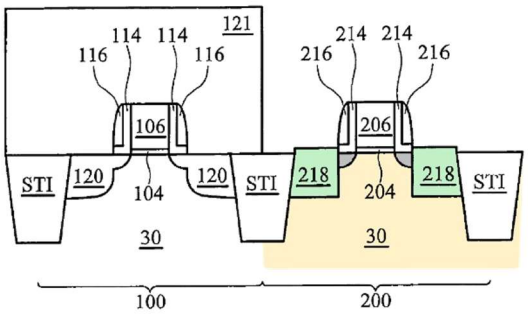


FIG. 7B

Hsu823, FIG. 7B

A POSITA would have found it obvious to modify Akasaka's PMISFET by using epitaxial SiGe stressors, as Hsu823 discloses, to form Akasaka's PMISFET source/drain regions 309. (Hsu823, ¶¶0032]-[0033], FIGS. 7A-7B; Akasaka, ¶[0073], FIG. 16; Ex-1003, ¶¶538-542.) A POSITA would have been motivated to do so since SiGe stressors were known to increase hole mobility, thereby boosting drive current and operating speed. (*Supra* §II.D; Hsu823, ¶¶[0002]-[0003], ¶[0033]; Ex-1003, ¶540.)

A POSITA would have reasonably expected to succeed because such SiGe layers were known and widely used to compressively stress such PMISFETs. (*Supra* §II.D; Ex-1003, ¶541.) The structure in Akasaka's FIG. 16 is materially the same as the structure in Hsu823's FIG. 7A. (Ex-1003, ¶541; *see* Akasaka, ¶¶[0072]-[0073], FIG. 16; Hsu823, ¶¶[0028]-[0032], FIG. 7A.) Hsu823 teaches that SiGe source/drain regions may be readily integrated into such a structure to boost PMOS performance. (Hsu823, ¶[0033]; Ex-1003, ¶541.) Thus, as Figure F shows below, a POSITA

would have known the same process steps Hsu823 describes regarding Figure 7B readily integrate into Akasaka's process at FIG. 16 with the ordinary and expected result: boosted PMISFET performance. (Hsu823, ¶[0033]; *supra* §II.D; Ex-1003, ¶541.)

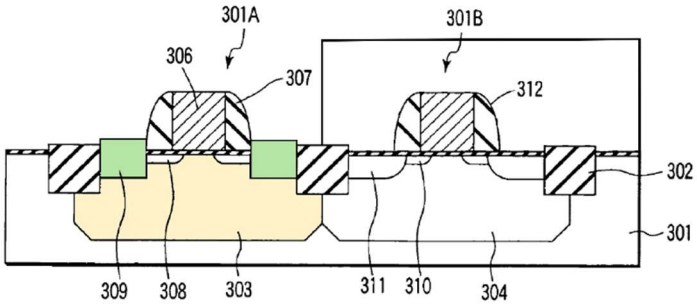


Figure F (Akasaka's FIG. 16, modified)

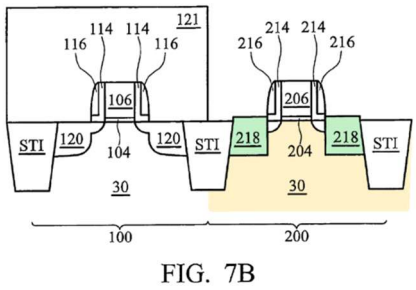


FIG. 7B

Hsu823, Fig. 7B

Figure G illustrates Akasaka's PMISFET, modified to include SiGe stressors as Hsu823 discloses. (Ex-1003, ¶542; Hsu823, ¶[0033], FIG. 7B; Akasaka, FIG. 26; Ex-1038, 6:27-31, FIGS. 3-10.)

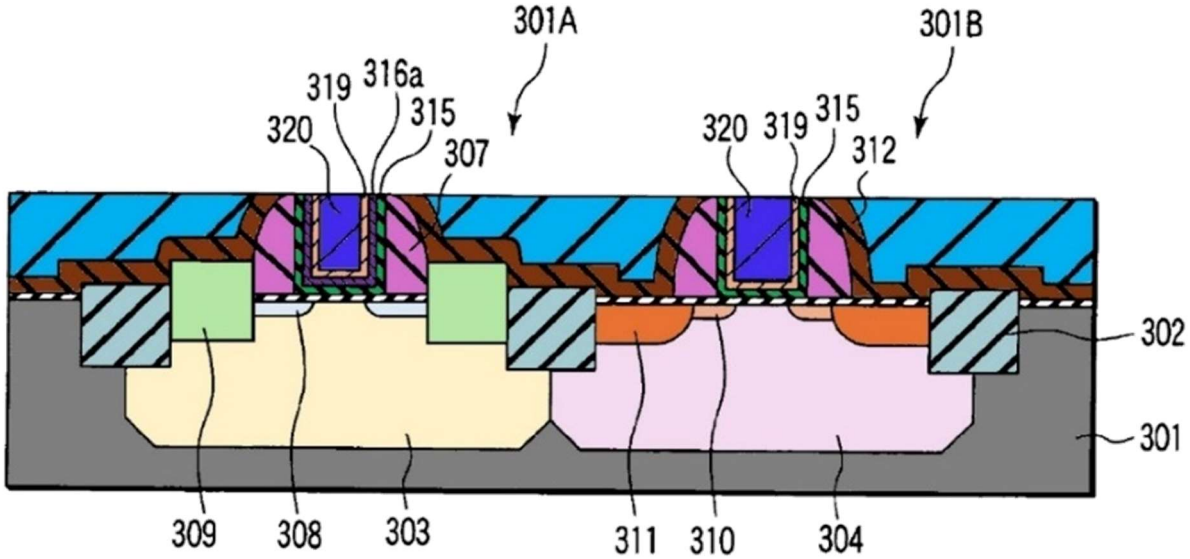


Figure G (Akasaka's FIG. 26, modified)

2. Independent Claim 1

a. [1Pre]-[1A], [1C]-[1J], and [1L]-[1M]

Akasaka discloses features [1Pre]-[1A], [1C]-[1J], and [1L]-[1M] as discussed for [19Pre]-[19A], [19C]-[19J], and [19K]-[19L], respectively. (*Supra* §§V.F.1.a-V.F.1.b, §§V.F.1.d-V.F.1.k, §§V.F.1.l-V.F.1.m.) Combining Hsu823 with Akasaka does not materially affect that analysis. (Ex-1003, ¶78, ¶¶543-554.)

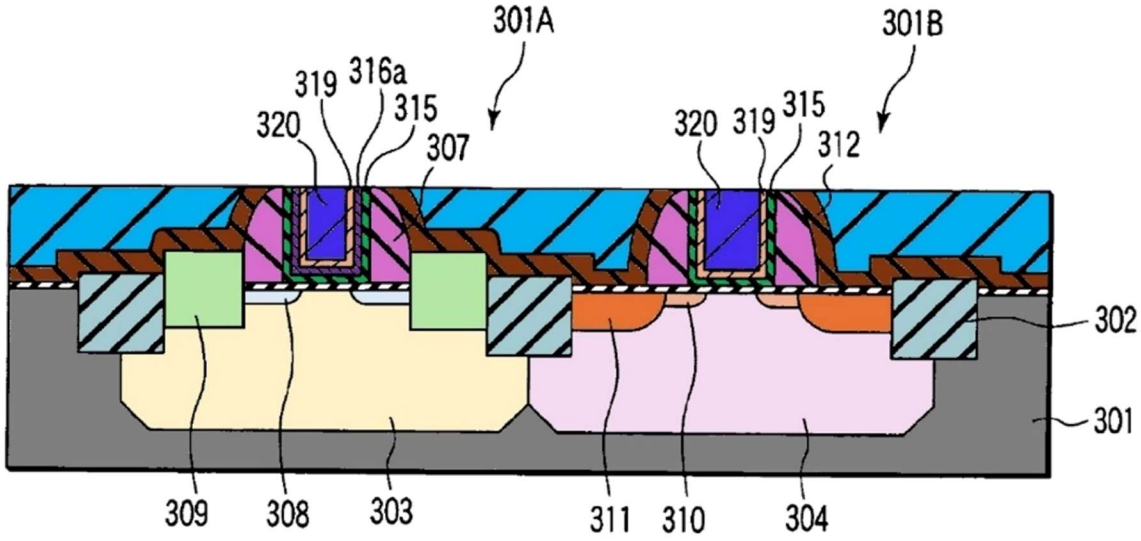


Figure G

b. [1B]

The Akasaka-Hsu823 combination includes "a second MIS transistor": "p-type MISFET" (i.e., PMISFET) 301A, modified to include epitaxial SiGe stressors as in Hsu823. (*Supra* §**Error! Reference source not found.**; Akasaka, ¶[0073], FIG. 26; Hsu823 ¶[0033], FIG. 7B; Ex-1003, ¶¶555-557.)

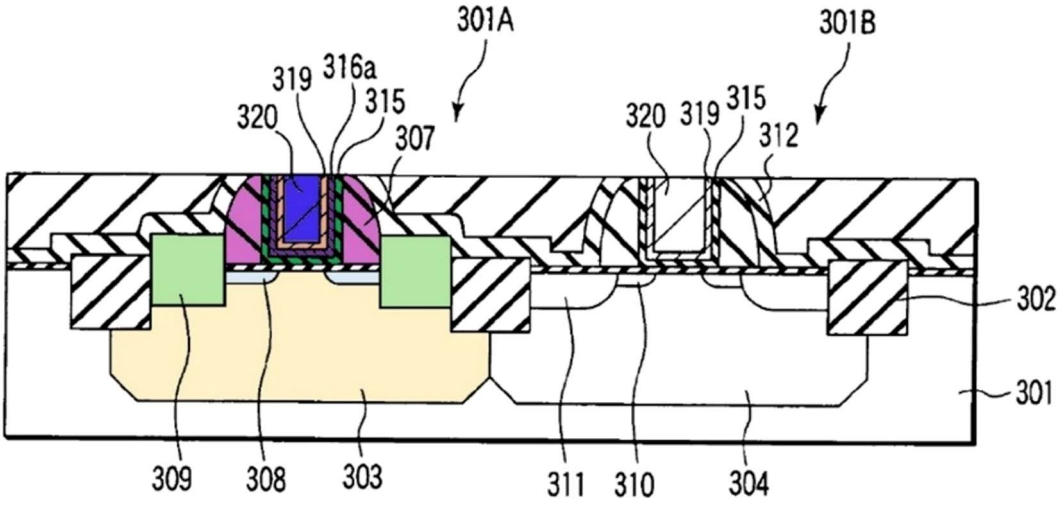


Figure G

c. [1K]

In the Akasaka-Hsu823 combination, the second MIS transistor (PMISFET) includes "source/drain regions formed in the second active region laterally outside the second sidewall spacers." (Ex-1003, ¶¶558-560.) Hsu823 explains: "Recesses are formed in substrate … along the outside edges of the spacers" by etching. (Hsu823, ¶[0033].) "SiGe stressors … are then formed in the recesses" and "doped [by boron] during the epitaxial growth." (*Id.*; *see id.*, FIG. 7B.) In this process—the same process a POSITA would have applied to Akasaka's PMISFETs (*supra* §V.G.1)—source/drain regions (SiGe stressors) are formed in the PMISFET active region laterally outside the PMISFET sidewall spacers. As Figure G shows below, the resulting PMISFET includes source/drain regions (SiGe stressors) formed in the active region (PMISFET active region) laterally outside sidewall spacers 307. (Ex-1003, ¶¶559-560.)

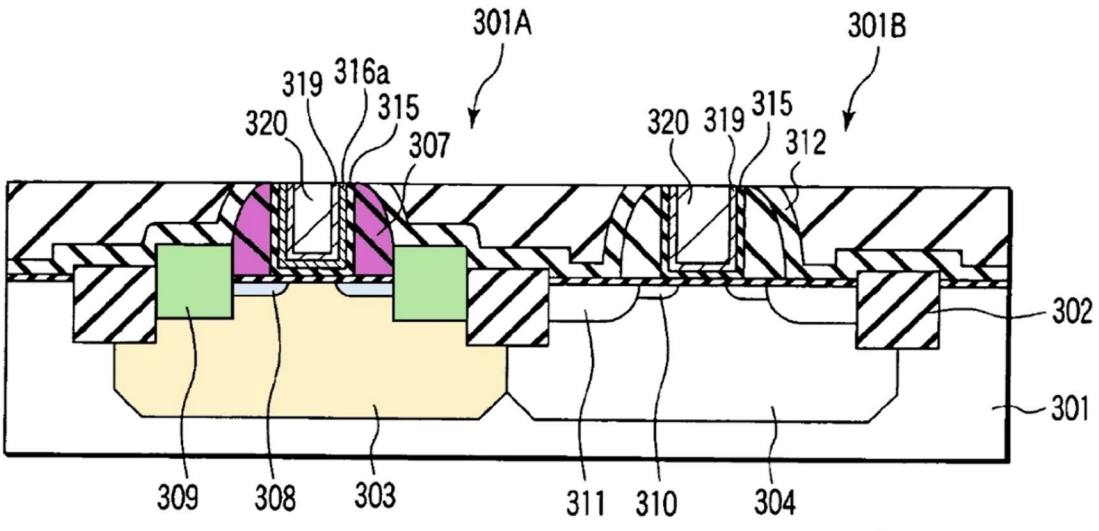


Figure G

d. [1N]

In the Akasaka-Hsu823 combination, "the source/drain regions include a silicon mixed crystal layer which is formed in trenches provided in the second active region, and causes first stress in a gate length direction of a channel region in the second active region." (Ex-1003, ¶¶561-563.) A POSITA would have found it obvious to implement SiGe stressors as Akasaka's PMISFET source/drain layers 309. (*Supra* §V.G.1.) A POSITA would have understood Hsu823's SiGe stressors are "a silicon mixed crystal layer which is formed in trenches provided in" the PMISFET active region because they are silicon mixed crystal layers "epitaxially grown" in "[r]ecesses [that] are formed … along the outside edges of the spacers." (Hsu823, ¶[0033]; Ex-1003, ¶563.) A POSITA also would have recognized such SiGe stressors "cause[] … stress in a gate length direction of a channel region in the

… [PMISFET] active region." (*See* Hsu823, ¶[0033] (SiGe stressors "introduce[] compressive stress[] in the … channel region[] of the resulting PMOS device"); *supra* §II.D; Ex-1003, ¶563.)

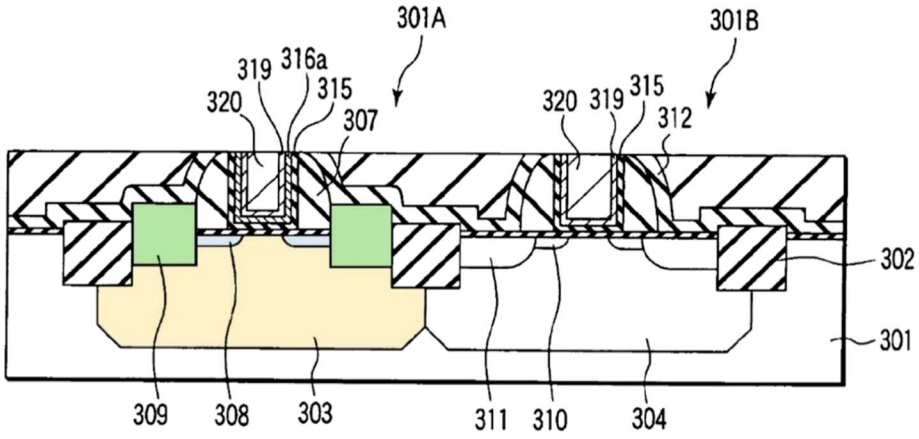


Figure G

e. [1O]

Feature [1O] would have been obvious as discussed for claim 22. (*Supra* §V.F.4.) Combining Hsu823 with Akasaka does not materially affect that analysis. (Ex-1003, ¶564.)

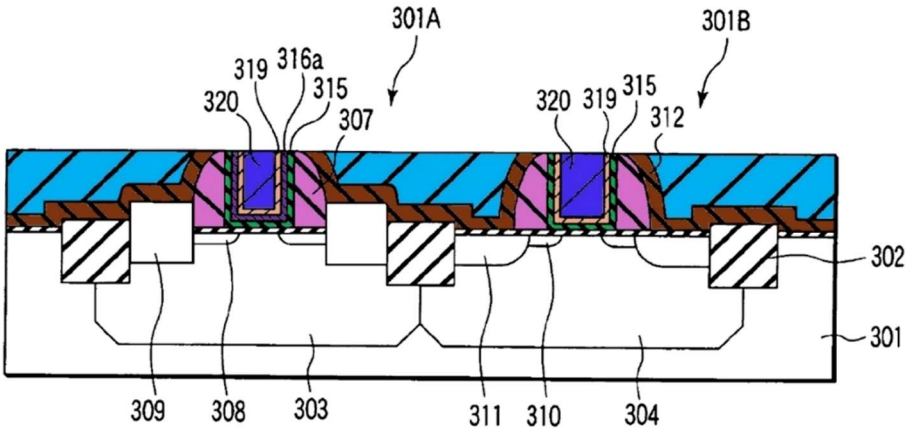


Figure G

3. Independent Claim 25

a. [25Pre]-[25L]

The Akasaka-Hsu823 combination for claim 25 only optionally includes SiGe stressors as described in Section V.G.1. Features [25Pre]-[25L] would have been obvious as discussed for [19Pre]-[19L], respectively. (*Supra* §§V.F.1.a-V.F.1.m.) Whether SiGe stressors are present does not materially affect how the analysis of [19Pre]-[19L] applies to [25Pre]-[25L]. (*See* Ex-1003, ¶80, ¶¶565-578.)

b. [25M]

In the Akasaka-Hsu823 combination, "the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region." (Ex-1003, ¶¶579-584.)

A POSITA would have been motivated to implement Akasaka's silicon nitride etch-stop film 312 as a tensile etch layer to cause tensile stress along the gate length direction of Akasaka's NMISFET channel region. (Ex-1003, ¶¶580-583.) Akasaka's "silicon nitride film 312 serv[es] as an etching stopper." (Akasaka, ¶[0073].) Hsu823 similarly discloses a tensile silicon nitride etching stopper that causes stress along the gate length direction of the NMOS channel. (Hsu823, ¶¶[0036]-[0037].) Hsu823 explains: "The performance of a MOS device can be enhanced through a stressed-surface channel." (Hsu823, ¶[0002]; *see id.* ¶[0003] ("[A] bi-axial, in-plane tensile stress field can improve NMOS performance.").) "A

commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device." (*Id.* ¶[0003]; *see* Ex-1028, 1-2; Ex-1031, ¶[0003]; Ex-1029, ¶[0090]; Ex-1030, 1-2; Ex-1023, Fig. 5(c); *supra* §II.D.)

A POSITA would have selected Akasaka's etch-stop layer 312 as a tensile etch stop layer for both PMISFET and NMISFET devices, which was well known in the art, because it provides improved NMISFET electron mobility. (*See supra* §II.D; Hsu823, ¶[0039]; Ex-1027, ¶¶[0038]-[0039]; Ex-1026, ¶[0005]; Ex-1028, 1-2; Ex-1030, 1-2; Ex-1023, Fig. 5(c); Ex-1003, ¶¶582-583.)

A POSITA would have reasonably expected to succeed in implementing Akasaka's etch stop film 312 as a tensile etch stop layer because such tensile CESL films were widely used to improve carrier mobility in NMISFET devices. (*Supra* §II.D; Ex-1003, ¶584.) And it would have been well within a POSITA's ability to create such a tensile silicon nitride CESL film simply by adjusting deposition conditions. (Ex-1029, ¶[0090], ¶¶[0099]-[0100], TBL. V; Ex-1003, ¶584.)

4. Claims 2 and 26

Akasaka discloses the features of claims 2 and 26 as discussed for claim 20. (*Supra* §V.F.2; *see supra* §V.G.2, §V.G.3.) Combining Hsu823 with Akasaka does not materially affect that analysis. (Ex-1003, ¶¶585-587.)

5. Claims 3 and 27

Akasaka discloses the features of claims 3 and 27 as discussed for claim 21. (*Supra* §V.F.3; *see supra* §V.G.2, §V.G.3.) Combining Hsu823 with Akasaka does not materially affect that analysis. (Ex-1003, ¶¶588-590.)

6. Claims 4 and 29

The Akasaka-Hsu823 combination satisfies "wherein the conductive film is made of the second metal film." (Ex-1003, ¶¶591-599.)

Akasaka's conductive film 319 and/or 320 discloses the claimed "second metal film" of NMISFET 301B. (*Supra* §V.F.1.e ([19D]), *see supra* §V.G.2, §V.G.3.) The same conductive film 319 and/or 320 discloses the "conductive film" of PMISFET 301A. (*Supra* §V.F.1.i ([19H]); *see supra* §V.G.2, §V.G.3.) Accordingly, the same film (conductive film 319 or 320, or both together) forms both the claimed "second metal film" and "conductive film." (Akasaka, FIGS. 25-26.)

7. Claims 6 and 31

The Akasaka-Hsu823 combination satisfies "wherein the first and second gate insulating films are made of the same insulating material." (Ex-1003, ¶¶600-604.)

Akasaka's gate dielectric film 315 discloses both the "first and second gate insulating films." (*Supra* §V.F.1.d ([19C]), §V.F.1.h ([19G]); *see supra* §V.G.2, §V.G.3.) Gate dielectric film 315 "is depos[it]ed all over the substrate" using the

same insulating material ($HfSi_xO_y$) for both NMISFET and PMISFET devices. (Akasaka, ¶¶[0074]-[0075], FIG. 19.)

8. Claims 7, 23, and 33

a. A POSITA would have found it obvious to implement Hsu823's L-shaped side walls

The MISFETs in the Akasaka-Hsu823 combination include "gate sidewall[s] 307," as Figure G shows. (Akasaka, ¶[0073], FIG. 26; Ex-1003, ¶¶609-622.)

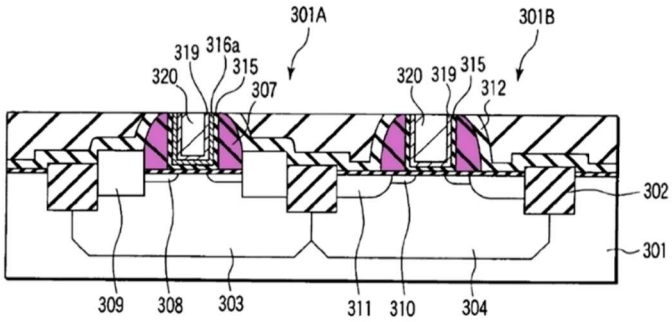


Figure G

Hsu823 similarly discloses spacer 116/216, plus spacer liners 114/214, as FIG. 7B shows. (Hsu823, ¶[0031].)

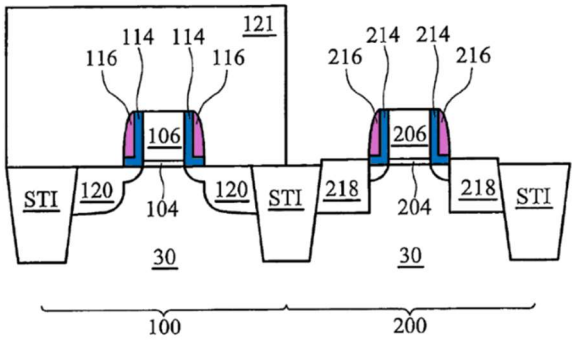


FIG. 7B

Hsu823, FIG. 7B

Hsu823 discloses removing spacers 116/216—but not spacer liners 114/214—before forming contact etch stop layer 34,[15] as FIGS. 9 and 10 illustrate. (Hsu823, ¶[0035].)

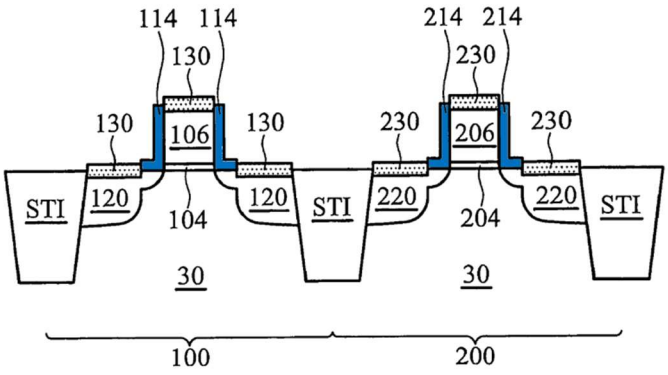


FIG. 9

Hsu823, FIG. 9

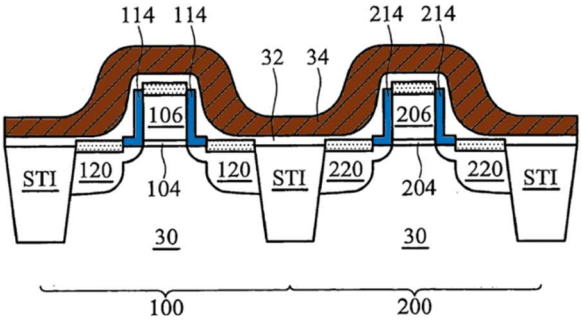


FIG. 10

Hsu823, FIG. 10 (showing optional layer 32 to be omitted here)

Hsu823 recommends removing the spacers 116/216 because it reduces the aspect ratio between gates: "With the scaling of integrated circuits, … the distance between devices decreases" and "subsequently performed gap-filling and contact

[15] Dielectric layer 32 is "optional[]" and may be omitted. (Hsu823, ¶[0036].)

etch processes suffer problems accordingly." (Hsu823, ¶[0004] (discussing "problems, such as short circuits").) By removing spacers 116/216, the aspect ratio shrinks (*see* FIGS. 15A-15B), which minimizes voids (*see* FIG. 1) and resolves such issues. (*Id.* ¶[0004], ¶¶[0042]-[0043].) Moreover, it improves stress transfer to the channel. (*Id.* ¶[0015]; Ex-1030, 1-2, Figs. 1-7; Ex-1003, ¶¶610-615.)

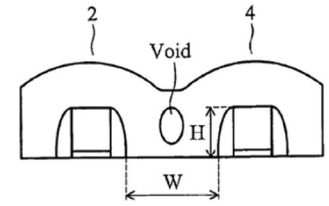


FIG. 1 (PRIOR ART)

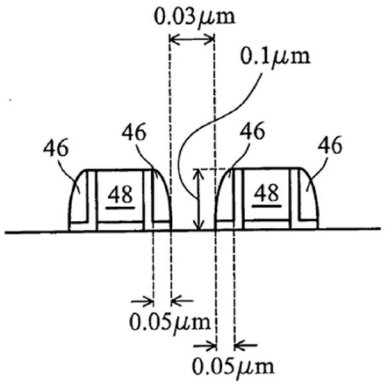


FIG. 15A

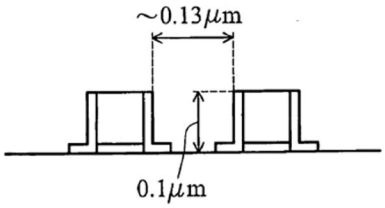


FIG. 15B

Hsu823, FIGS. 1, 15A, 15B

Because Akasaka includes prior-art sidewalls that, according to Hsu823, are susceptible to voiding, a POSITA would have found it obvious to apply Hsu823's teachings to Akasaka—i.e., to add L-shaped spacer liners like Hsu823's spacer liners 114/214 and to subsequently remove gate sidewalls 307, leaving only the L-shaped spacer liners. (Ex-1003, ¶¶616-622.) That is, to minimize voiding, a POSITA would have found it obvious to form L-shaped spacer liners in addition to Akasaka's D-shaped gate sidewalls 307, just as Hsu823 describes forming L-shaped spacer liners 114/214 in addition to D-shaped spacers 116/216. (Akasaka, ¶[0073];

Hsu823, ¶¶[0030]-[0031], FIGS. 5-6; Ex-1003, ¶¶616-617.) Figure H illustrates this modification. (Ex-1003, ¶617.)

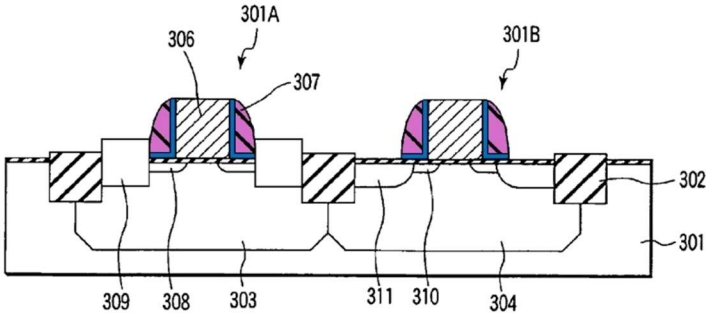


Figure H

Before forming silicon nitride film 312, a POSITA would have removed silicon nitride gate sidewalls 307, leaving the L-shaped spacer liners as Hsu823 discloses. (Hsu823, ¶[0035]; Ex-1003, ¶618.) Hsu823 explains: "The removal is preferably performed using an etchant that attacks the [sidewalls 307], but not the [L-shaped spacer liners]." (Hsu823, ¶[0035].) Since Akasaka's sidewalls 307 are silicon nitride, "H_3PO_4 can be used to remove [sidewalls 307]." (*Id.*) L-shaped spacer liners "formed of silicon oxide" will not be removed by the H_3PO_4. (*Id.*) Figure I illustrates this modification. (Ex-1003, ¶618.)

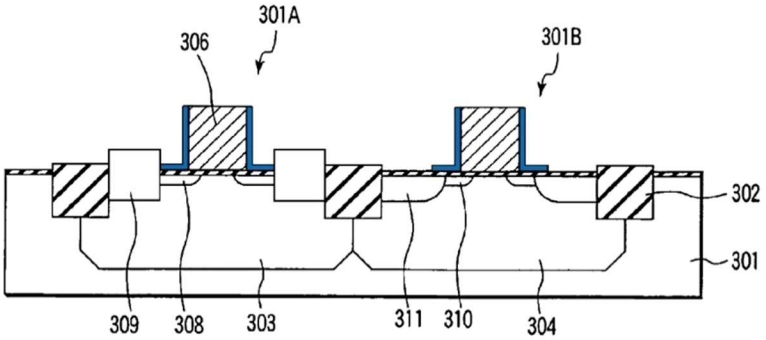


Figure I

A POSITA would have then formed Akasaka's silicon nitride film 312 over the L-shaped spacer liners, as Hsu823 discloses. (*See* Akasaka, ¶[0073]; Hsu823, ¶[0036].) Figure J illustrates this modification. (Ex-1003, ¶619.)

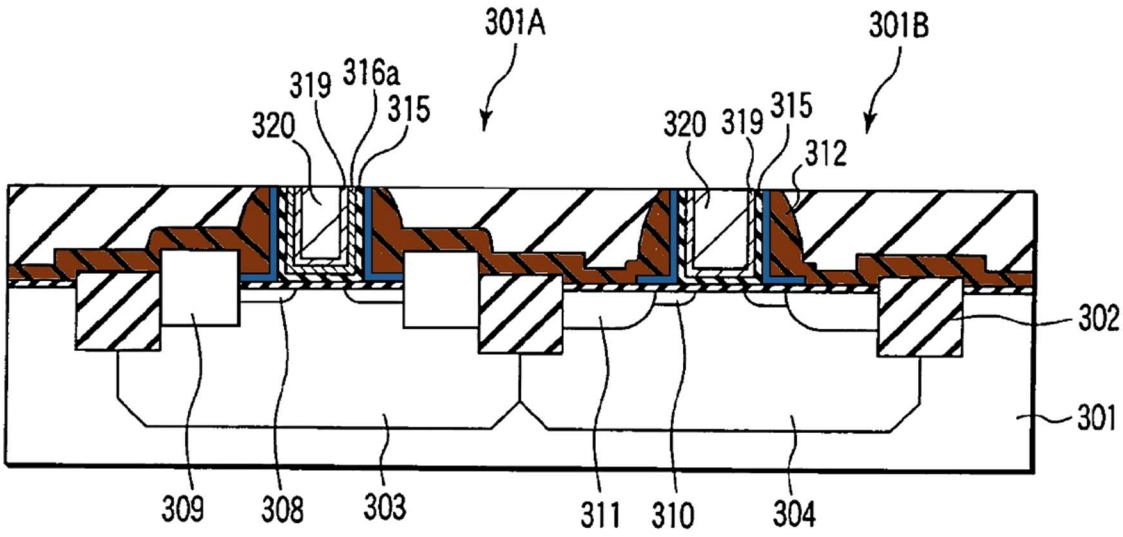


Figure J

A POSITA would have been motivated to modify Akasaka in this way to minimize gaps that cause "difficulty in subsequent processes" and "problems, such as short circuits." (Hsu823, ¶[0004]; Ex-1003, ¶620.) It was well-known that removing outer sidewalls and leaving L-shaped sidewalls, as Hsu823 discloses, increases packing density, reduces voiding, and prevents contact-to-gate shorts. (Hsu823, ¶[0004], ¶¶[0042]-[0043]; Ex-1039, Abstract, ¶¶[0018]-[0022], FIGS. 1B-1D; Ex-1003, ¶620.) Moreover, it improves stress transfer to the channel. (Hsu823, ¶[0015]; Ex-1030, 1-2, Figs. 1-7; Ex-1003, ¶621.)

A POSITA would have reasonably expected to succeed at least because Hsu823 discloses that silicon nitride spacers (like Akasaka's sidewalls 307) can be selectively removed over silicon oxide spacers (e.g., Hsu823's spacer liners 114/214) using an etchant like H_3PO_4 that preferentially attacks silicon nitride. (Hsu823, ¶[0035]; Ex-1003, ¶622.)

b. Claim 7

Claim 7, which depends from claim 1 (*supra* §V.G.2), would have been obvious. In the Akasaka-Hsu823 combination, "each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section, and the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape." (Ex-1003, ¶¶623-625.)

A POSITA would have found it obvious to incorporate Hsu823's L-shaped spacer liners 114/214 into Akasaka's MISFETs to increase packing density, reduce voiding, and prevent contact-to-gate shorts. (*Supra* §V.G.8.a.) As Figure J illustrates below, upon doing so Akasaka's NMISFET and PMISFET both include L-shaped sidewall spacers that (like Hsu823's spacer liners 114/214) form "an inner sidewall having an L-shaped cross-section." Silicon nitride film 312 directly contacts surfaces of those sidewall spacers bent in an L-shape. (Ex-1003, ¶625.)

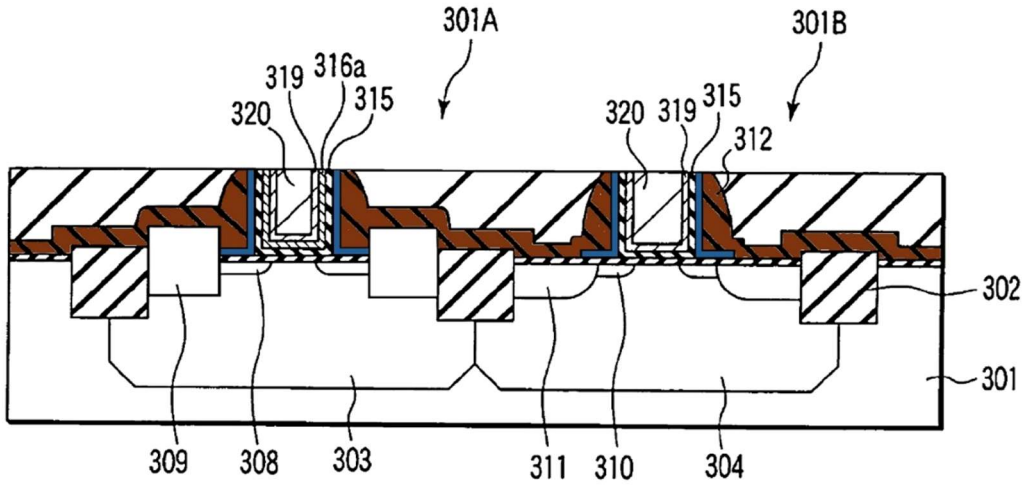


Figure J

c. Claims 23 and 33

The features of claims 23 and 33 would have been obvious as discussed for claim 7. (*Supra* §V.G.8; *see supra* §V.F.1, §V.G.3.) Although optional, Hsu823's SiGe stressors are not required for claims 23 and 33 (*see* Figure K) and do not materially affect that analysis. (Ex-1003, ¶¶626-628.)

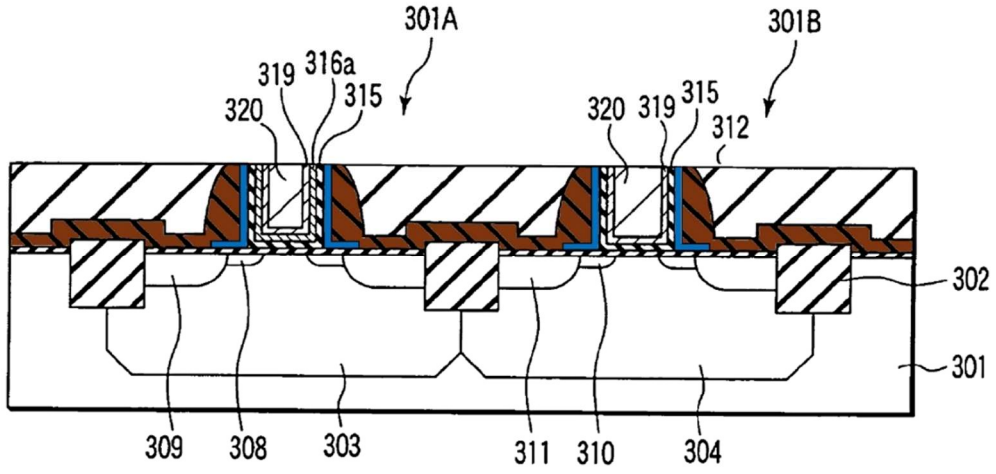


Figure K

9. Claim 8

In the Akasaka-Hsu823 combination, "the silicon nitride film causes second stress in a gate length direction of a channel region in the first active region" as discussed for [25M]. (*Supra* §V.G.3.b; *see supra* §V.G.2.) Including SiGe stressors in the Akasaka-Hsu823 combination, as claim 8 requires, does not materially affect that analysis. (*See* §V.G.1; Ex-1003, ¶¶629-631.)

10. Claim 9

In the Akasaka-Hsu823 combination, "the first MIS transistor is an n-type MIS transistor, and the second stress is tensile stress." (Ex-1003, ¶¶632-634.) As explained for claim 8, a POSITA would have found it obvious to use a tensile silicon nitride film 312 (second stress) to improve electron mobility in NMISFET devices (first MIS transistor). (*Supra* §II.D; Hsu823, ¶[0003], ¶¶[0037]-[0039]; Ex-1028, 1-2; Ex-1030, 1-2; Ex-1023, Fig. 5(c); Ex-1003, ¶634.)

11. Claim 10

In the Akasaka-Hsu823 combination, "the second MIS transistor is a p-type MIS transistor, the silicon mixed crystal layer is made of a SiGe layer, and the first stress is compressive stress." (Ex-1003, ¶¶635-637.) A POSITA would have found it obvious to grow SiGe stressors (a "silicon mixed crystal layer made of a SiGe layer") in the source/drain regions of Akasaka's PMISFET. (*Supra* §V.G.2.d ([1N]).) A POSITA also would have understood those SiGe stressors compressively

stress neighboring PMISFET channel regions. (*Id.*; *supra* §II.D.) SiGe stressors "introduce[] compressive stress[] in the respective channel regions of the … PMOS device[]," such that the "device drive current[] of the … PMOS device[] [is] increased." (Hsu823 ¶[0033]; *see id.* ¶[0003], ¶[0037].)

12. Claims 24 and 34

The features of claims 24 and 34 would have been obvious as discussed for [1K], [1N], and claim 10. (*Supra* §V.G.2.c, §V.G.2.d, §V.G.11; *see supra* §V.G.1, §V.F.1, §V.G.3; Ex-1003, ¶¶638-640.)

13. Claim 28

The features of claim 28 would have been obvious as discussed for claim 22. (*Supra* §V.F.4; *see supra* §V.G.3.) Combining Hsu823 with Akasaka does not materially affect that analysis. (Ex-1003, ¶¶641-642.)

14. Claim 35

Akasaka discloses and renders obvious the features of claim 35. In the Akasaka-Hsu823 combination, "the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more." (Ex-1003, ¶¶643-646; *see supra* §V.G.3.) Akasaka uses "gate dielectric (insulating) film 315," which may comprise $HfSi_xO_y$, as both the first and second gate insulating films. (Akasaka, ¶[0075]; *supra* §V.F.1.d ([19C]), §V.F.1.h ([19G]).) This is "a high-k film made of a metal oxide having a relative dielectric constant of

10 or more." (Ex-1003, ¶646; *see* Ex-1014, ¶[0004] (explaining "$HfSiO_x$ … and oxynitrides thereof" have "dielectricity of more than ten"); *supra* §II.B.)

H. Ground 2D: Akasaka, Hsu823, and Hobbs Render Obvious Claim 32

Claim 32, which depends from claim 25 (*supra* §V.G.3), would have been obvious. (Ex-1003, ¶¶647-663.)

1. A POSITA would have found it obvious to use different gate insulating films for NMISFETs and PMISFETs

Like Aoyama and Hobbs, Akasaka uses an RMG process to select different gate metals with work functions appropriate to adjust the threshold voltages of NMISFET and PMISFET devices, respectively. (Akasaka, ¶¶[0076]-[0077], ¶¶[0084]-[0085]; Hobbs, 8:37-40; Aoyama, ¶¶[0009]-[0010], ¶[0066]; *supra* §II.C.) For the same reasons stated in Section 0 (e.g., to obtain higher performance CMOS devices with higher mobility, higher saturation current, and/or better threshold voltage), a POSITA also would have been motivated to implement different gate insulating films in Akasaka's NMISFETs and PMISFETs. (Ex-1003, ¶¶650-658.)

Moreover, a POSITA would have reasonably expected to succeed, as the successes of others indicate. (Hobbs, 7:43-47; Ex-1040, ¶¶[0016]-[0017], ¶[0019], ¶[0023], FIGS. 1-7; Ex-1041, 6:21-34, FIGS. 2B-2F; Ex-1038, 5:16-20, 5:25-30, FIGS. 10-11.) After removing Akasaka's dummy gate electrodes (*see* Akasaka, FIG. 18), a POSITA would have found it obvious to further remove Akasaka's gate

dielectric film from one or both of the NMISFET and PMISFET gate regions, then to form a different gate dielectric film in such regions so that the NMISFET and PMISFET gate dielectrics are uniquely tailored to each type of device. (Ex-1003, ¶¶659-661.)

2. Claim 32

In the Akasaka-Hsu823-Hobbs combination, "the first and second gate insulating films are made of different insulating materials." (Ex-1003, ¶¶662-663.) A POSITA would have found it obvious to use different gate dielectric films for Akasaka's NMISFETs and PMISFETs, respectively, to improve device performance. (*Supra* §0; *see* Hobbs, 7:43-47, 7:65-8:2; Ex-1040 ¶[0019], ¶[0026]; Ex-1041, 6:21-34; Ex-1003, ¶663.)

VI. TRIAL SHOULD BE INSTITUTED

A. Discretionary Denial Is Not Warranted Under *Advanced Bionics*

Advanced Bionics favors institution. *See* IPR2019-01469, Paper 6 (Feb. 13, 2020) (precedential). When considering §325(d), the Board asks "whether the same or substantially the same art" or "the same or substantially the same arguments previously were presented to the Office." (*Id.*, 8.) If so, the Board considers "whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of the challenged claims." (*Id.*)

Here, only one reference—Aoyama—was cited during prosecution. Grounds 1C-1E combine Aoyama's teachings with additional prior art never cited during prosecution and never considered by the Examiner. Accordingly, these Grounds do not involve either "the same or substantially the same art" or "the same or substantially the same arguments." *See Howard Indus., Inc. v. Capsa Solutions LLC*, No. IPR2023-01275, Paper 9, at 44-45 (Feb. 26, 2024).

During prosecution, the Examiner discussed only Aoyama's first embodiment (FIGS. 1-2N). Because Grounds 1A-1B rely on Aoyama's third embodiment (FIGS. 5-6Q), the Examiner never addressed "the same or substantially the same arguments" made here. *See Current Lighting Sols., LLC v. Jiaxing Super Lighting Elec. Appliance Co.*, IPR2023-00270, Paper 18, at 49-50 (Aug. 16, 2023) (granting institution where petitioner presented arguments based on different embodiments of a previously considered reference); *Avaya Inc. v. Blackberry Ltd.*, IPR2017-01852, Paper 7, at 15-20 (Feb. 13, 2018) (same where Examiner overlooked an embodiment). Moreover, the Examiner only applied Aoyama to a pre-amendment version of the claims, not the version that issued.

As this Petition demonstrates, the Examiner also "erred in a manner material to the patentability of the claims." *Advanced Bionics*, IPR2019-01469, Paper 6, at 8 & n.9. The Board finds a material error, for instance, where a "Petitioner identifies where the prior art teaches the specific limitation the Examiner identified as missing

from the prior art." *See Nespresso USA, Inc. v. K-Fee System GmbH*, IPR2023-00502, Paper 9, at 33 (Sept. 13, 2023) (granting institution). Here, the Examiner overlooked Aoyama's third embodiment altogether, which anticipates certain claims. (*Supra* §§V.A-B.) That was a material error.

As to the remaining references besides Aoyama, all *Advanced Bionics* factors favor institution.

Taken together, *Advanced Bionics* favors institution.

B. Discretionary Denial Is Not Warranted Under *Fintiv*

Pursuant to the Stewart Memorandum dated March 26, 2025, titled "Interim Process for PTAB Workload Management," Petitioner will respond to any discretionary denial arguments Patent Owner may raise through the Board's bifurcated briefing process.

Nevertheless, to simplify the *Fintiv* analysis, and following the precedential *Sotera* decision, Petitioner stipulates that, if IPR is instituted, Petitioner will not pursue in the related district court proceeding any ground that Petitioner raised or reasonably could have raised against the challenged claims during the instituted IPR.

VII. MANDATORY NOTICES

A. Real Party-in-Interest

Taiwan Semiconductor Manufacturing Company Limited is the real party-in-interest.

B. Related Matters

The ’686 Patent has been asserted against Petitioner in *Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Manufacturing Co.*, No. 2:24-cv-00623-JRG (E.D. Tex.). The ’686 Patent also has been asserted against United Microelectronics Corporation (UMC), an unrelated party, in *Advanced Integrated Circuit Process LLC v. United Microelectronics Corp*, No. 2:24-cv-00730-JRG (E.D. Tex.).

C. Lead and Back-Up Counsel

Lead Counsel	Back-Up Counsel
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D. Service Information

Petitioner consents to service by e-mail at the following addresses:

- jp.long@finnegan.com; and
- kevin.rodkey@finnegan.com.

VIII. PAYMENT OF FEES

The Office may charge additional fees to Deposit Account No. 06-0916.

IX. GROUNDS FOR STANDING

Petitioner certifies the '686 Patent is available for *inter partes* review and Petitioner is not barred or estopped from requesting review on the grounds presented.

X. CERTIFICATION UNDER 37 C.F.R. §42.24(d)

As calculated by the "Word Count" feature of Microsoft Word for Microsoft 365, this Petition contains 13,809 words, excluding this Certification and the following: Table of Contents, Table of Authorities, List of Exhibits, List of Challenged Claims, Mandatory Notices, and Certificate of Service.

XI. CONCLUSION

Trial should be instituted and the challenged claims cancelled.

Dated: March 28, 2025 Respectfully submitted,

/ J. Preston Long, Ph.D. /

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Lead Counsel for Petitioner

CERTIFICATE OF SERVICE

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105(a), **Petition for *Inter Partes* Review, Petitioner's Power of Attorney, and the associated Exhibits 1001-1042** were served via FedEx Priority Overnight delivery on March 28, 2025, on the correspondence address of record below indicated in the U.S. Patent Office's Patent Center for U.S. Patent No. 8,198,686.

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Courtesy copies have been concurrently served by the same means on Patent Owner's litigation counsel at:

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Dated: March 28, 2025 By: / William Esper /

William Esper
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