

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNITED MICROELECTRONICS CORPORATION,
AND
UMC GROUP (USA),

Petitioners

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,

Patent Owner

Case IPR2025-01091
Patent 8,198,686

**PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37
C.F.R. § 42.107 TO PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 8,198,686**

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EXHIBIT LIST

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EX2001	Complaint for Patent Infringement , Dkt. No. 1, <i>Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Manufacturing Company Limited</i> , Case No. 2:24-cv-00623, (E.D. Tex. Filed August 1, 2024)
EX2002	Complaint for Patent Infringement , Dkt. No. 1, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Case No. 2:24-cv-00730, (E.D. Tex. Filed September 6, 2024)
EX2003	Consolidation Order , Dkt. No. 12, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed December 6, 2024)
EX2004	Docket Sheet , <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Case No. 2:24-cv-00730, (E.D. Tex.) (Printed August 16, 2025)
EX2005	Docket Control Order , Dkt. No. 51, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed February 14, 2025)
EX2006	Second Docket Control Order , Dkt. No. 55, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed February 21, 2025)
EX2007	First Amended Docket Control Order , Dkt. No. 59, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed February 27, 2025)
EX2008	Third Amended Docket Control Order , Dkt. No. 83, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed April 9, 2025)
EX2009	Docket Sheet , <i>Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Manufacturing Company Limited</i> , Case No. 2:24-cv-00623, (E.D. Tex. Dated April 23, 2025)

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EX2010	Notice of Compliance (re: P.R. 3-1 and 3-2 disclosures), Dkt. No. 45, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed January 30, 2025)
EX2011	Plaintiff's Unopposed Motion for Leave to Amend Infringement Contentions, Dkt. No. 54, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed February 20, 2025)
EX2012	Plaintiff's Unopposed Motion for Leave to Amend Infringement Contentions Against Defendant United Microelectronic Corporation, Dkt. No. 64, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed March 7, 2025)
EX2013	Defendant Taiwan Semiconductor Manufacturing Company Limited's Notice of Compliance and Service of Invalidity Contentions, Dkt. No. 104, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed May 1, 2025)
EX2014	Defendant United Microelectronic Corporation's Notice of Compliance and Service of Invalidity Contentions, Dkt. No. 106 <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed May 2, 2025)
EX2015	Scheduling Order, Dkt. No. 28, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Case No. 2:24-cv-00730, (E.D. Tex. Filed December 11, 2024)
EX2016	Defendant TSMC's Invalidity Contentions, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Served May 1, 2025)
EX2017	Defendant United Microelectronics Corporation's Invalidity Contentions, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Served May 1, 2025)

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EX2018	Declaration of Ravi Bhalla , dated August 20, 2025
EX2019	Protective Order , Dkt. No. 71, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed March 20, 2025)
EX2020	Joint Notice Resolving Discovery Disputes Set for Hearing (Dkt. Nos. 78, 80, 89, 90) , Dkt. No. 102, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed April 30, 2025)
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EX2022	United Microelectronics Corporation’s Motion to Dismiss Plaintiff’s Claims for Direct Infringement and Pre-Suit Indirect Infringement , Dkt. No. 15, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed December 6, 2024)
EX2023	Defendant Taiwan Semiconductor Manufacturing Company Limited’s Reply in Support of its Motion to Stay Pending <i>Inter Partes</i> Review , Dkt. No. 109, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed May 20, 2025)
EX2024	Plaintiff’s Opposition to Defendant Taiwan Semiconductor Manufacturing Company Limited’s Motion to Stay , Dkt. No. 108, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed May 12, 2025)
EX2025	Exhibit 686A1 to Defendant UMC’s Invalidity Contentions, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623 (E.D. Tex. Served May 1, 2025)

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EX2032	Exhibit A to TSMC’s Sealed Motion for Issuance of Letter Rogatory for Nuvoton Technology Corporation – Japan , Dkt. No. 116-1, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623 (E.D. Tex. Filed June 20, 2025)
EX2033	Exhibit B to TSMC’s Sealed Motion for Issuance of Letter Rogatory for Nuvoton Technology Corporation – Taiwan , Dkt. No. 114-2, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623 (E.D. Tex. Filed June 20, 2025)
EX2034	Redaction to TSMC’s Sealed Motion for Issuance of Letter Rogatory for Nuvoton Technology Corporation – Taiwan , Dkt. No. 118, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623 (E.D. Tex. Filed June 27, 2025)
EX2035	Recorded Assignment from Panasonic Corporation to Panasonic Semiconductor Solutions Co., Ltd. (August 17, 2020)
EX2036	Recorded Assignment by Change of Name from Panasonic Semiconductor Solutions Co., Ltd. to Nuvoton Technology Corporation Japan
EX2037	UMC Letter to AICP Regarding Stipulation (July 17, 2025)

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EX2038	Order Granting to Taiwan Semiconductor Manufacturing Company Ltd.’s Motion for Letters Rogatory to Nuvoton Technology Corporation (Letter Rogatory No. 1), Dkt. No. 122, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623 (E.D. Tex. Filed July 25, 2025)
EX2039	Order Granting to Taiwan Semiconductor Manufacturing Company Ltd.’s Motion for Letters Rogatory to Nuvoton Technology Corporation (Letter Rogatory No. 2), Dkt. No. 123, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623 (E.D. Tex. Filed July 25, 2025)
EX2040	TSMC Petition For <i>Inter Partes</i> Review of U.S. Patent 8,198,686 , Filed as Paper 1 in IPR2025-00682 (March 28, 2025)
EX2041	Patent Owner’s Discretionary Denial Brief Pursuant to the Board’s March 26, 2025 Interim Processes For PTAB Workload Management , Filed as Paper 6 in IPR2025-00682 (June 18, 2025)
EX2042	Patent Owner’s Discretionary Denial Brief Pursuant to the Board’s March 26, 2025 Interim Processes For PTAB Workload Management , Filed as Paper 6 in IPR2025-00683 (June 18, 2025)
EX2043	TSMC Letter to AICP Regarding Stipulation (July 17, 2025)
EX2044	Email From Director approving 5-Page Reply Brief Due July 28, 2025 (July 24, 2025)
EX2045	UMC’s Motion For Consolidation Under 35 U.S.C. § 315(d) and 37 C.F.R. § 42.122(a) With Related <i>Inter Partes</i> Review IPR2025-00832 , Filed as Paper 7 in IPR2025-01053 (June 30, 2025)
EX2046	UMC’s Motion For Joinder Under 35 U.S.C. § 315(c) and 37 C.F.R. § 42.122(b) To Related <i>Inter Partes</i> Review IPR2025-00828 , Filed as Paper 7 in IPR2025-01076 (June 30, 2025)
EX2047	UMC’s Motion For Joinder Under 35 U.S.C. § 315(c) and 37 C.F.R. § 42.122(b) To Related <i>Inter Partes</i> Review IPR2025-00829 , Filed as Paper 7 in IPR2025-01079 (June 30, 2025)

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EX2048	UMC’s Motion For Joinder Under 35 U.S.C. § 315(c) and 37 C.F.R. § 42.122(b) To Related <i>Inter Partes</i> Review IPR2025-00683 , Filed as Paper 7 in IPR2025-01090 (June 30, 2025)
EX2049	UMC’s Motion For Joinder Under 35 U.S.C. § 315(c) and 37 C.F.R. § 42.122(b) To Related <i>Inter Partes</i> Review IPR2025-00682 , Filed as Paper 7 in IPR2025-01091 (June 30, 2025)
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EX2052	Docket Navigator Time-to-Trial Statistics Report for trials before the Honorable Rodney Gilstrap, Federal District Judge in the Eastern District of Texas, during the period from August 18, 2024 to August 18, 2025
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EX2054	FAQs for Interim Processes for PTAB Workload Management from https://www.uspto.gov/patents/ptab/faqs/interim-processes-workload-management
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EX2057	Patent Owner’s Preliminary Response Under 37 C.F.R. § 42.107 to Petition For <i>Inter Partes</i> Review of U.S. Patent No. 8,198,686 , Filed as Paper 9 in IPR2025-00682 (July 18, 2025)
EX2058	Excerpt from Streetman, Ben G. and Banerjee, Sanjay Kumar, “Solid State Electronic Devices,” 7 th Ed. (2016).

Advanced Integrated Circuit Process, LLC (“AICP”) respectfully requests that the Board decline to institute *inter partes review* (“IPR”) on the petition (“the Petition”) filed by United Microelectronics Corporation and UMC Group (USA) (“UMC”) because it fails to “show[] . . . a reasonable likelihood” that UMC would prevail with respect to any of the claims at issue. 35 U.S.C. § 314(a).

I. INTRODUCTION

The Petition’s theories regarding United States Patent No. 8,198,686 (“the ’686 Patent”) lack merit. AICP has dedicated to the public all ’686 Patent claims except independent claim 25 and its dependents. The Petition concedes that neither primary reference—Aoyama or Akasaka—teaches claim 25’s limitation that “the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region.” Instead, the Petition relies on Hsu823 for this limitation in all asserted Grounds. Using a tensile silicon nitride film, as allegedly taught by Hsu823, in Aoyama or Akasaka would have impaired the performance of the PMOS transistors, which is a nonsensical sacrifice in the context of those references. In addition, Hsu823 teaches away from the claimed combination, particularly in the context of the type of devices in the primary references.

II. BACKGROUND

A. Technology Background¹

A “MISFET,” also commonly referred to as a “MOSFET,” is a metal-insulator-semiconductor field effect transistor. EX1101 ¶ 34. MOSFETs include source and drain regions for current flow. *Id.* These source/drain regions are doped with either a p-type or n-type impurity. *Id.* ¶ 35. “A MOSFET with source/drain regions made from ‘p-type’ material is known as a PMOS or p-FET, while a MOSFET with source/drain regions made from ‘n-type’ material is known as a NMOS or n-FET.” *Id.* There is a channel region located between the source and drain regions, and a gate over the channel region. *Id.* ¶ 34.

Several competing realities apply in the race to improve performance and decrease the sizes of transistors. While NMOS transistor performance may be improved by the introduction of tensile stress, there were known drawbacks to this approach. EX1528 at 7. For example, thicker layers of material and smaller spacers were generally required to impart greater tensile stress. EX1006 ¶¶ [0024]–[0026].

¹ This summary, as well as certain factual assertions in this Preliminary Response, is based on the evidence offered in support of the Petition. AICP relies on this evidence for purposes of this Preliminary Response only and reserves the right to submit evidence to clarify or correct any facts, in the event of institution.

Thicker layers create challenges for scaling down integrated circuits because thicker layers may result in voids, which may cause short circuits. *Id.* ¶¶ [0003]–[0004]. Moreover, PMOS transistor performance is degraded by tensile stress. EX1528 at 7; EX1006 ¶ [0037]. And, without the introduction of compressive stress, PMOS transistors are “slower than NMOS transistors.” EX1101 ¶ 81.

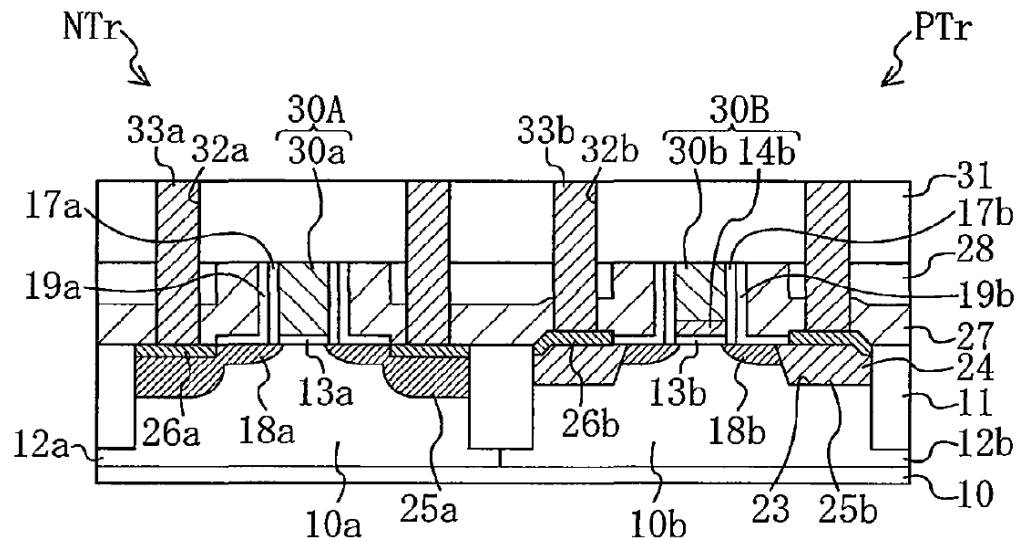
B. The '686 Patent Invention

The '686 Patent (EX1001) was invented and developed by Yoshihiro Sato and Hisashi Ogawa of Panasonic Corporation, a leader and pioneer in the development and manufacture of electronic equipment including semiconductors and cameras. The '686 Patent, which claims priority from a foreign application filed March 13, 2008, issued on June 12, 2012.

The '686 Patent relates to “a semiconductor device including a [MISFET] having a gate electrode made of a metal material, and a method for manufacturing the semiconductor device.” EX1001 at 1:16–20. After the disclaimer, the '686 Patent has eleven claims, one of which (*i.e.*, claim 25) is an independent claim and the remainder of which (*i.e.*, claims 26–35) are dependent claims. *Id.* at 33:8–34:41. Thus, all claims in the '686 Patent require the limitations of claim 25, directly or by dependency.

The '686 Patent teaches a semiconductor device, shown in Figure 5C below, that includes an n-type MIS transistor (NTr) and a p-type MIS transistor (PTr).

EX1001 at 16:55–60. The n-type MIS transistor includes a first gate insulating film 13a on a first active region 10a. *Id.* at 16:16–22. The n-type MIS transistor also includes a first gate electrode 30A comprising a second metal film 30a. *Id.* First sidewall spacers (17a or 19a) are formed on side surfaces of the first gate electrode 30A. *Id.* at 12:44–63. The p-type MIS transistor includes a second gate insulating film 13b on the second active region 10b. *Id.* at 12:1–7. The second gate electrode 30B includes a first metal film 14b and a conductive film 30b. *Id.* at 16:16–22. Second sidewall spacers (17b or 19b) are formed on side surfaces of the second gate electrode. *Id.* at 12:44–63. The first and second side wall spacers 19a, 19b are insulative. *Id.* A silicon nitride film 27 is formed over the side surfaces of the first and second gate electrodes 30A, 30B. *Id.* at 14:55–64. Further, the first and second gate electrodes 30A, 30B are made of different metal materials. *Id.* at 18:25–33.



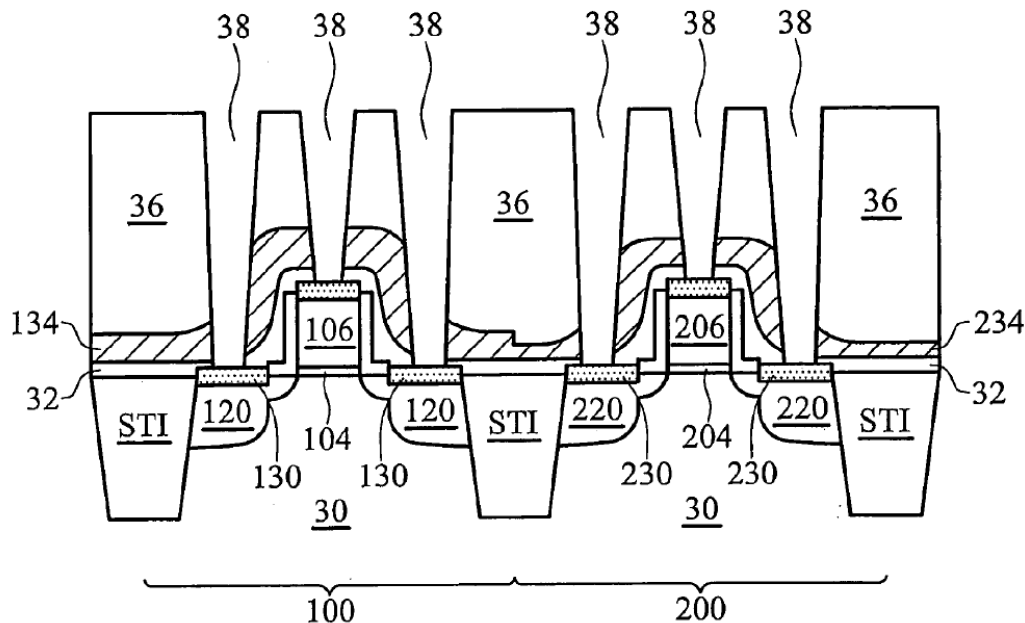
EX1001 at Fig. 5C

Although the '686 Patent includes several points of novelty, for the purposes of this preliminary response, AICP will focus on the limitation "the silicon nitride film causes first stress in a gate length direction of a channel in the first active region." EX1001 at 34:1-2 (claim 25). The '686 Patent teaches that this stress improves "the drive capability of the n-type MIS transistor." *Id.* at 28:29-30. The silicon nitride film may, for example, be created by performing a plasma chemical vapor deposition (CVD) to deposit a silicon nitride film "containing a large amount of hydrogen," and then irradiating the film with ultraviolet light to remove hydrogen contained in the silicon nitride film. *Id.* at 28:20-26.

C. UMC's Cited References

1. Hsu823 (EX1006) – All Grounds

Hsu823 is directed to “manufacturing methods of metal-oxide-semiconductor (MOS) devices with [an] improved gap-filling and contact etch process window.” EX1006 ¶ [0001]. The devices Hsu823 teaches are structurally very different from the '686 Patent's claimed device. Compare EX1006 at FIG. 12 (reproduced below) with EX1001 at FIG. 11C. UMC does not dispute this; Hsu823 is only cited as teaching a stressed CESL and is not cited for any other limitation of independent claim 25. Petition at 31-32, 50-51. As discussed in Sections II.C.2 and 3, *infra*, Hsu823 is also structurally very different from the Petition's primary references, Aoyama and Akasaka.



EX1006 at FIG. 12

Hsu823 teaches that one method for improving MOS transistor performance by “applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device.” EX1006 ¶ [0003]. Hsu823 notes, however, that “[w]ith the scaling of integrated circuits” (*i.e.*, as transistor devices decrease in size), the use of a CESL thick enough to apply stress creates problems. *Id.* ¶ [0004]. First, as the distance between transistors decreases, the “aspect ratio” of the gap between them (*i.e.*, the ratio of height H to width W) increases when a thick CESL is used. *Id.* As a result, voids can be formed in the “inter-layer dielectric layer,” “caus[ing] difficulty in subsequent processes.” *Id.* It can also “cause problems, such as short circuits, if the voids are filled with conductive materials.” *Id.* Second, as “the distance between MOS devices [] are [sic] decreased,” “the CESL [in the region between transistors] will experience great thickness variation. As a result, the subsequent contact-etch process experiences difficulty, and over-etch may occur at one location and under etching may occur at another.” *Id.* ¶ [0006].

To decrease the aspect ratio and minimize the foregoing problems, Hsu823 teaches a design in which “no [gate sidewall] spacers [are] formed” or limiting the design to “a very thin spacer.” *Id.* ¶¶ [0024]–[0027]. Accordingly, in the preferred embodiment shown in Figure 9, “spacers 116 and 216 are removed.” *Id.* ¶ [0035]; *see also id.* ¶ [0042] (“By removing spacers (refer to FIG. 15B), the spacing is increased to close to 0.13 μm , and the aspect ratio is reduced to 0.8.”). Hsu823 also

teaches how stresses that benefit the performance of one type of transistor (*e.g.*, NMOS) impair the performance of the other (*e.g.*, PMOS), and vice versa. *See Id.* ¶ [0037]. More specifically, Hsu823 teaches that if the CESL has a “tensile stress,” there will be a “detrimental effect” on the performance of the “PMOS device[s].” *Id.* And, if the CESL has a “compressive stress,” there will be a “detrimental effect” on the performance of the “NMOS device[s].” *Id.* ¶ [0038]. Hsu823 also teaches that any benefits accruing to the NMOS transistor’s performance from a tensile film will be very limited because “the performance of NMOS devices is relatively difficult to improve.” *Id.* ¶ [0039].

2. Aoyama (EX1005) – Ground I

Aoyama “relates to a semiconductor device and a manufacturing method thereof, for example, to a semiconductor device which includes a PMOSFET and an NMOSFET.” EX1005 ¶ [0003]. Aoyama does not teach a strained CESL. Petition at 31-32.

Aoyama creates a semiconductor device by utilizing dummy electrodes 103, which are later removed and replaced with functional gate electrodes 104. EX1005 ¶ [0067]. Figure 2J, shown below, illustrates the semiconductor device prior to removing the dummy electrodes 103.

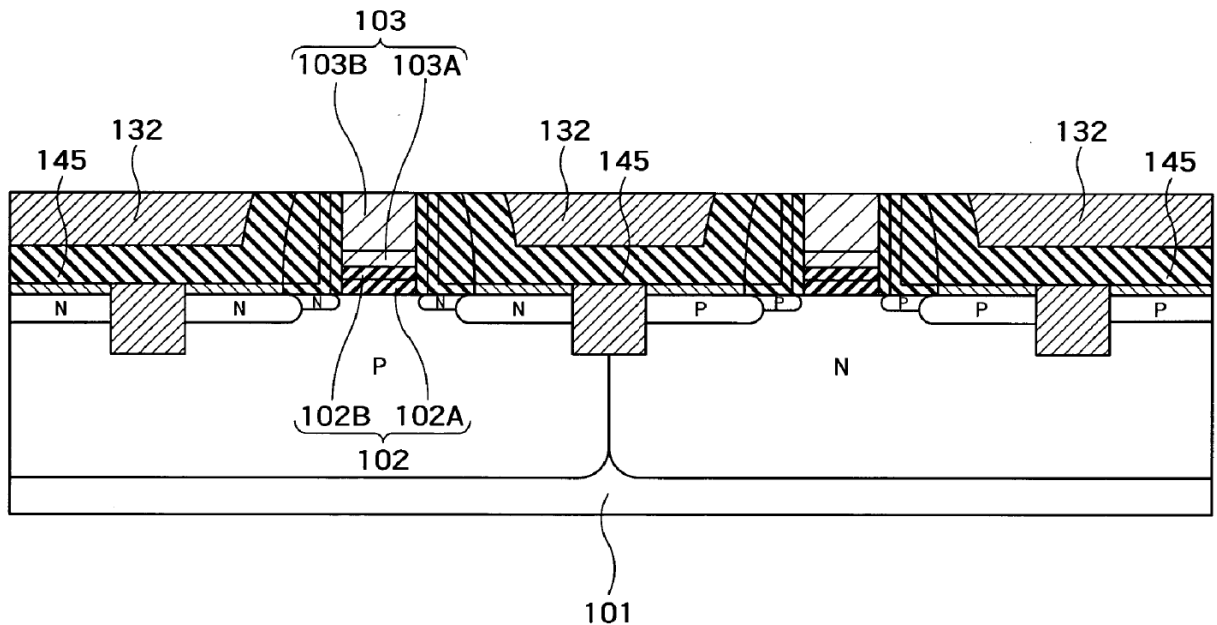


FIG. 2J

EX1005 at FIG. 2J

3. Akasaka (EX1008) – Ground II

Akasaka “relates to a method for manufacturing a semiconductor device, particularly an FET (Field Effect Transistor) of the MIS (Metal Insulator Semiconductor) type.” EX1008 ¶ [0003]. Akasaka also does not teach a strained CESL. Petition at 50-51.

Akasaka creates a semiconductor device by utilizing dummy electrodes 306, which are later removed and replaced with functional gate electrodes 320. EX1008 ¶¶ [0073]–[0086]. Figure 17, shown below, illustrates the semiconductor device prior to completing a chemical mechanical polish to expose the dummy electrodes 306, and prior to removing the dummy electrodes 306.

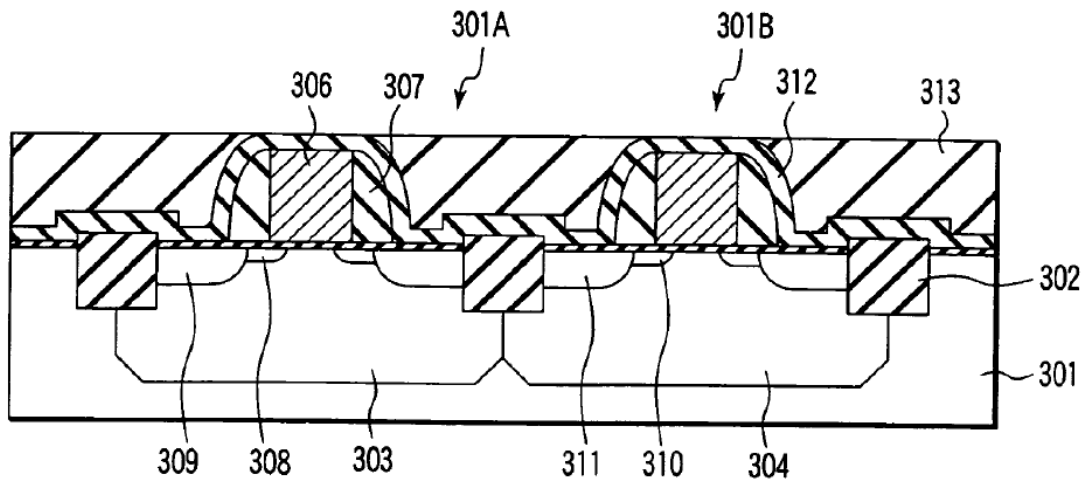


FIG. 17

EX1008 at FIG. 17

D. The Level of Ordinary Skill in the Art

UMC asserts that a person of ordinary skill in the art (“POSA”) “would have had at least a Master’s degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education.” Petition at 14 (internal citation omitted). It is unnecessary for AICP to propose a competing definition at this time because, even under UMC’s proposed definition, UMC has failed to demonstrate a reasonable likelihood of success on any of the challenged claims. AICP reserves the right to present evidence in support of a different definition of the level of ordinary skill in the art, if the Board institutes IPR.

III. LEGAL STANDARDS

“In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (noting 35 U.S.C. § 312(a)(3) requires that petitions must identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”). To meet this burden, “the petition “must specify where each element of the claim is found in the prior art patents or printed publications relied upon.” 37 C.F.R. § 42.104(b)(4). And “the Board must base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016). The burden of persuasion on the petitioner never shifts to the patent owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). Applying the foregoing substantive standards and burdens, “[t]he Director may not authorize an *inter partes* review to be instituted unless the Director determines . . . that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a).

IV. CLAIM CONSTRUCTION

Claims are construed according to *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b). UMC argues that no claim terms

require construction. Petition at 14. AICP does not propose any claim constructions at this time because the Petition fails to demonstrate a reasonable likelihood of success.²

V. ARGUMENT

The Petition fails to show a reasonable likelihood of prevailing on any claim, under either Ground. Neither Aoyama nor Akasaka teaches a silicon nitride film that causes a stress in the gate length direction, as required by claim 25 (the sole independent claim), and UMC does not contend otherwise. Instead, the Petition relies on Hsu823's teaching of a tensile silicon nitride film. UMC fails to establish that a POSA would have been motivated to combine Hsu823's teachings with either of Aoyama or Akasaka to "provide[] improved NMOSFET [or NMISFET] electron mobility," as alleged. Petition at 32 (Aoyama), 51 (Akasaka).

For at least two independent reasons, this purported motivation is not merely incorrect, but nonsensical. First, the Petition's theory is predicated on a desire to benefit NMOS transistor performance using a tensile silicon nitride film but disregards entirely the detrimental effect that such a selection would have on the PMOS transistors' performance. As explained *infra*, because the circuit's operating

² AICP reserves the right to propose constructions in the event the Board grants institution.

speed is only as fast as its slowest transistors, it makes no sense to decrease the speed of the intrinsically slower PMOS transistors to increase the speed of the intrinsically faster NMOS transistors. Second, a POSA would not combine Hsu823 with Akasaka and Aoyama because Hsu823 discourages (and therefore teaches away from) the type of design employed in Aoyama and Akasaka. Because UMC's theories on the dependent claims rely on the theories presented for claim 25, the Petition's deficiencies with respect to claim 25 are fatal as to each Ground in its entirety, and the Petition should be denied institution.

A. A POSA would not have sacrificed the PMOS transistor's performance for the benefit of the NMOS transistor's performance.

The Petition fails to establish that a POSA would have been motivated to apply Hsu823's tensile CESL to the unstrained CMOS designs of Aoyama and Akasaka for the sake of improving NMOS electron mobility. As explained below, the use of Hsu823's tensile CESL (*i.e.*, to improve the carrier mobility of NMOS transistors) would degrade the carrier mobility of PMOS transistors, which the Petition and UMC's expert assert are intrinsically slower than NMOS transistors. Moreover, based on testimony of UMC's own expert, improving the NMOS speed without corresponding PMOS improvement would have had little or no practical benefit. Neither the Petition nor UMC's expert attempts to explain why a POSA would be willing to sacrifice the PMOS transistors' performance to benefit the

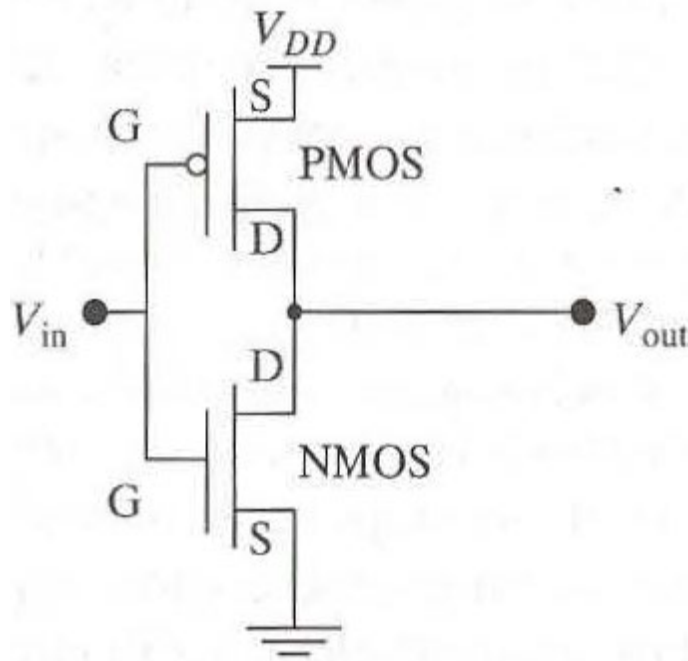
NMOS transistors. In the context of this technology, this deficiency is fatal to UMC's theory of obviousness.

When it comes to stresses in PMOS and NMOS transistors, what is good for the goose is *not* good for the gander. PMOS transistor performance is benefitted by compressive stress, whereas NMOS transistor performance is benefitted by tensile stress. Petition at 8-9. Hsu823 itself teaches that the tensile stress that benefits NMOS transistor performance has “detrimental effect[s]” on PMOS transistor performance and similarly, the compressive stress that benefits PMOS transistor performance has “detrimental effect[s]” on NMOS transistor performance. EX1006 ¶¶ [0037]–[0038]. The Petition offers no reason why a POSA would have been motivated to sacrifice PMOS transistor performance by combining Hsu823's tensile film with Aoyama's or Akasaka's transistors.

This failure to explain alone would be fatal to the Petition's obviousness theory, but the illogic is particularly stark in view of the relative performance of NMOS and PMOS in *unstrained* CMOS designs, like Aoyama's and Akasaka's. The CMOS designs taught by Aoyama and Akasaka do not use either “source-drain epitaxy” or the deposition of “stressed films,” which the Petition identifies broadly as the two kinds of techniques employed in strained-silicon technology. Petition at 8-11. The Petition further states that, absent “[s]trained-silicon technology,” PMOS is already “much slower than NMOS.” *Id.* at 8.

Accepting these allegations in the Petition as true, a POSA would have understood that the PMOS transistors in Aoyama and Akasaka would be “much slower” than their NMOS transistor counterparts. When this fact is combined with Hsu823’s teaching that “the performance of NMOS devices is relatively difficult to improve,” EX1006 ¶ [0039], the disparity becomes even starker. There is no evidence to rebut the conclusion that Hsu823’s tensile film would provide only marginal (if any) improvement to the NMOS transistors while degrading the already inferior PMOS transistor performance. Applying a tensile silicon nitride film to Aoyama or Akasaka would therefore make no sense.

If IPR is instituted, UMC’s expert will be forced to confront his own published book, which highlights why a POSA would never further sacrifice slower PMOS transistor performance to improve the faster NMOS transistor performance. Specifically, he wrote that a “particularly useful device” comprises a “combination of n-channel and p-channel MOS transistors” known as a “basic inverter circuit.” EX2058 at 3-4. And his book provides a figure (below) showing that an inverter comprises a single PMOS transistor and a single NMOS transistor.



EX2058 at 4

As his book explains, in an inverter when “the p-channel device is on, the n-channel device is off,” and vice versa. *Id.* at 4 (“The beauty of this circuit is that one of the devices is turned off for either condition. Since the devices are connected in series, no drain current flows, except for a small charging current during the switching process from one state to the other.”) Because both transistors must change states, the speed of this circuit can only function as fast as its slowest transistor. *See id.* at Fig. 9.4(a) (showing a timing diagram). Hence, it would have been nonsensical to use a tensile film to further boost the speed of the intrinsically faster NMOS transistor at the cost of impairing the speed of the intrinsically slower PMOS transistor.

B. Akasaka and Aoyama are incompatible with Hsu823's technique, which uses small or no spacers to facilitate application of a stressed film.

A POSA would not have been motivated to combine the cited art as proposed because Hsu823 discourages (and thus teaches away from) using stressed CESLs in structures like those taught by Aoyama and Akasaka. As shown below, Hsu823 identifies several problems with stressed CESLs. Hsu823 also teaches that overcoming those problems requires using small spacers (or no spacers at all) on the sides of gate electrodes, which are formed prior to the application of the CESL. A POSA would have concluded that this technique is incompatible with Aoyama's and Akasaka's devices, which use larger spacers and teach forming a gate electrode within a void that is created after applying an unstrained CESL.

The Petition implies that it would be a simple matter to substitute a stressed CESL for the unstressed CESL in Akasaka and Aoyama. Not so. Instead, Hsu823 teaches that CESLs thick enough to impart stress can cause several problems. EX1006 ¶¶ [0004]–[0006]. For example, as shown in Fig. 1 below, when such a CESL is used, “voids may be formed during the subsequent formation of an inter-layer dielectric layer. The voids may cause difficulty in subsequent processes, and may cause problems, such as short circuits, if the voids are filled with conductive materials.” *Id.* ¶ [0004], FIG. 1.

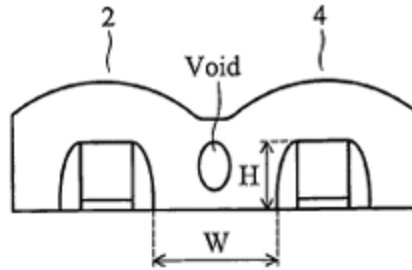


FIG. 1 (PRIOR ART)

EX1006 at FIG. 1

Thus, Hsu823 teaches a method of creating a semiconductor where very thin (or no spacers) are used to mitigate the potential adverse effects of a stressed CESL. Hsu823 teaches that spacers 116, 216 are removed and only the spacer liners 114, 214 remain. EX1006 ¶ [0035]. Hsu823's Figures 8 and 9 (reproduced below) respectively show the transistor before and after this removal.

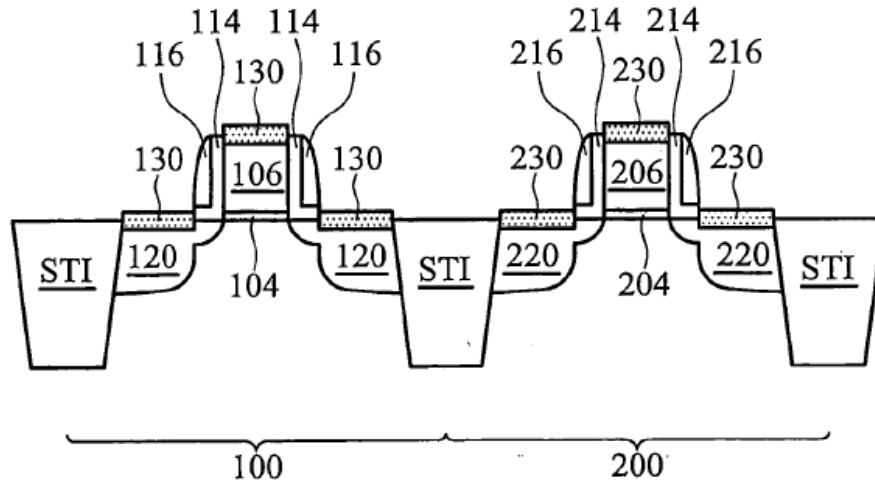


FIG. 8

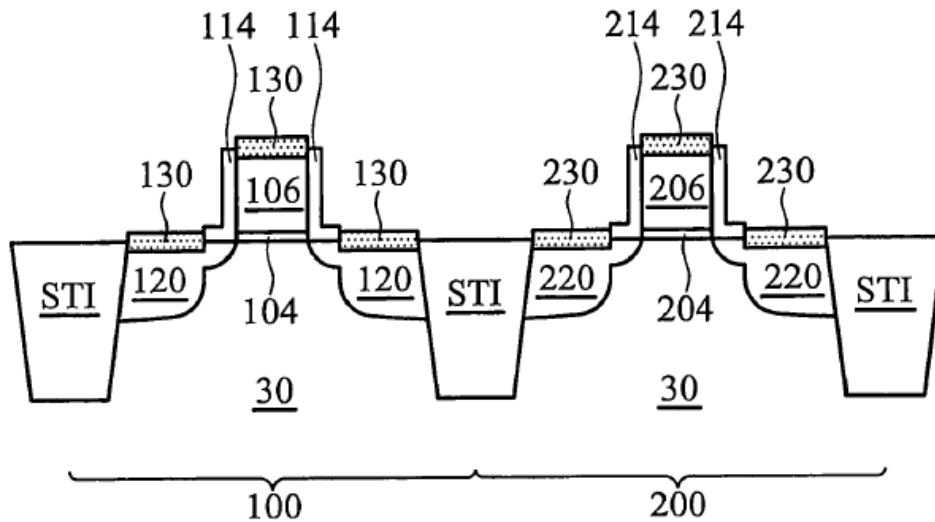
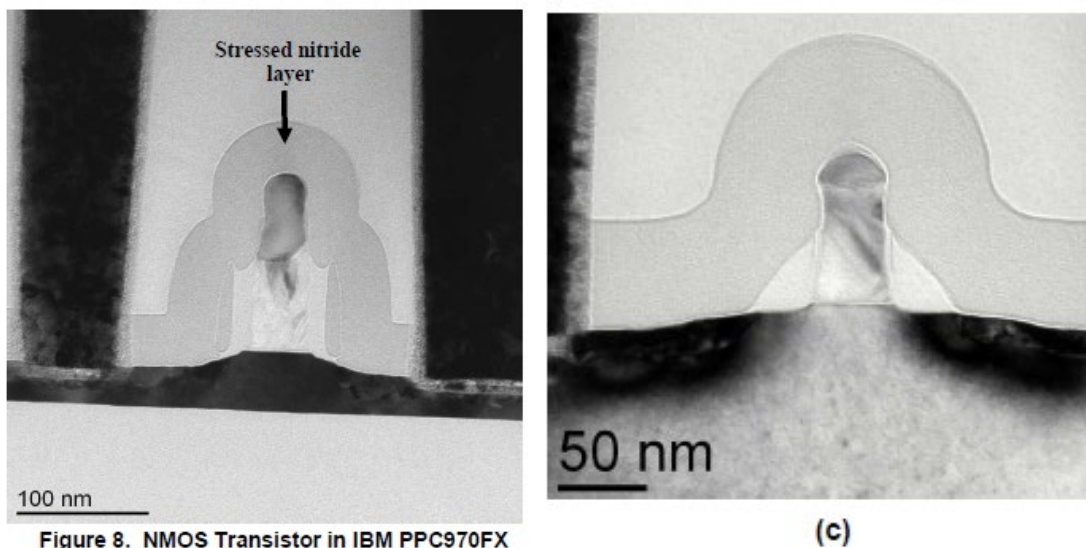


FIG. 9

EX1006 at FIGS. 8, 9

Hsu823 further teaches that “[t]he removal of spacer 116” makes the stressed CESL over the NMOS transistor “possible.” *Id.* ¶ [0037]. The relationship between minimal spacers and stressed CESLs, as taught by Hsu823, is supported by the art cited in the Petition to show a POSA would have known about stressed CESLs. Petition at 11 (citing *inter alia* EX1525 at 2, 4). For example, Exhibit 1525 (“James”)

describes analyzing several transistor structures and using the size of the sidewall spacers as evidence that the transistors include a stressed CESL. EX1525 at 3–4. Images of two analyzed transistors are reproduced below. For the transistor in Figure 8, James cites the “very slim” sidewall spacers as evidence a stressed nitride layer is used. *Id.* Similarly, James states that the transistor in Figure 10(c) includes “heavily etched sidewall spacers, [which] leads us to conclude that nitride stress is being used.” *Id.*



EX1525, Figures 8, 10(c)

A POSA would have believed from Hsu823 that using “very thin [or no] spacers” was not merely preferred, but important for the application of Hsu823’s strained CESL film. EX1006 ¶ [0026]; *see also id.* ¶ [0037]. A POSA would therefore not have combined Hsu823 with Akasaka or Aoyama because the two latter references employ intrinsically thick spacers. *See, e.g.*, EX1005 at Fig. 1; EX1008 at Fig. 26. For example, the Petition focuses on Aoyama Figure 5, which

uses a thick stack of three sidewall spacers, 141, 142, and 143. Petition at 15. The Petition also focuses on Akasaka Figure 26, which uses a thick sidewall 307. *Id.* at 16. Hsu823 teaches away from the combination of a stressed CESL with thick spacers like Aoyama's and Akasaka's, and the Petition offers no rationale as to why a POSA would have ignored Hsu823's teachings to make the proposed combination.

Although the Petition never suggests that a POSA would have further incorporated Hsu823's reduced sidewall spacers with the primary references, such a theory would not have cured the defect in the Petition. A POSA would have concerns about using a stressed CESL with very thin or no sidewall spacers in the processes taught by Akasaka and Aoyama. In Hsu823, a stressed CESL does not deform the gate structure because the gate electrodes 106, 206 are formed, small spacer liners 116, 216 are formed around the gate electrodes 106, 206, and then the stressed CESL 34 is deposited on the gate electrodes 106, 206. *See* EX1006 Figs. 9–10. In sharp contrast, Aoyama and Akasaka utilize dummy electrodes that are removed after the formation of the CESL. EX1005 ¶ 67; EX1008 ¶¶ [0073]–[0086]. The removal of the dummy gate material leaves a trench. EX1005 ¶ [0058]; EX1008 ¶ [0074]. A stressed CESL would exert force on the walls of the voided gate, which a POSA would recognize might cause the gate structure to buckle (particularly if thin spacers or no spacers are used as Hsu823 teaches).

In Aoyama, dummy gate electrodes 103 (instead of actual electrodes) are initially created on the substrate 101. EX1005 ¶¶ [0039]-[0051]. Then, multiple large sidewall spacers 141, 142, 143 are formed around the dummy electrodes 103. *Id.* ¶ [0053]. The unstrained CESL 145 is formed over the dummy electrodes 103 and the sidewall spacers 141, 142, 143. *Id.* ¶ [0056], Fig. 2J. A chemical mechanical polish (CMP) process is used to expose the dummy electrodes 103, etching down to the top of the spacers 141, 142, 143. *Id.* The dummy electrodes 103 are etched away, and the large sidewall spacers 141, 142, 143 hold open the space 151 for the gate electrode 104 to be deposited. *Id.* ¶ [0058]. Figure 2L, below, shows the Aoyama transistor after the dummy electrodes 103 have been etched away, prior to the deposition of the gate electrode 104. As is visibly evident from the figure, if a stressed CESL was deposited (particularly if the spacers were very thin as Hsu823 teaches), a POSA would believe the voided gate structure could buckle.

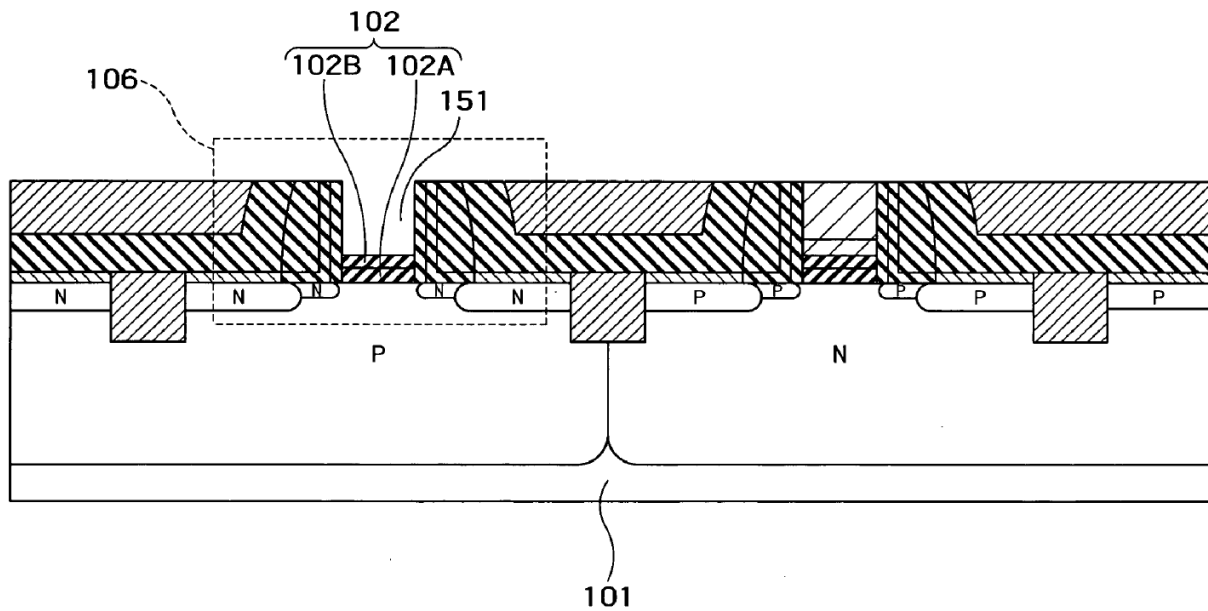


FIG. 2L
EX1005 at FIG. 2L

Akasaka utilizes a similar process to create the gate electrodes as Aoyama. EX1008 ¶¶ [0073]–[0086]. Figure 18, below, shows the transistor after etching away the dummy electrodes. The large sidewall spacers 307 are used to hold open the space for the recessed portions 314. *Id.* ¶ [0074]. Like Aoyama, the recessed portions are where the gate electrodes 320 are formed. *Id.* ¶¶ [0075]–[0086]. Again, as is visibly evident from the figure, if a stressed CESL was deposited (particularly if the spacers were very thin as Hsu823 teaches), a POSA would believe the voided gate structure could buckle.

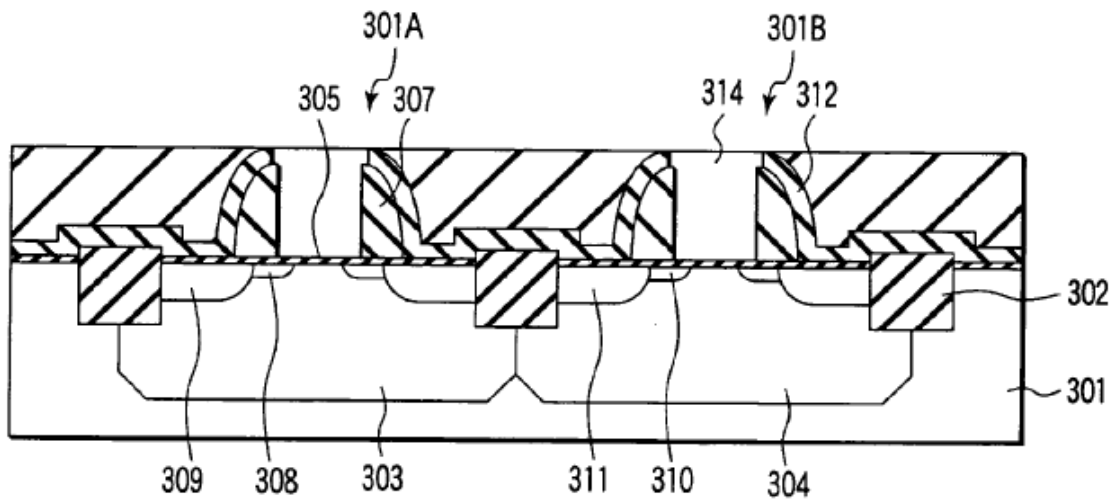


FIG. 18

EX1008 at FIG. 18

Hsu823 teaches utilizing very thin or no spacers both to avoid the circuit failing (*e.g.*, due to a short circuit) and to improve the performance of the circuit (by applying stress). EX1006 ¶¶ [0003]–[0006], [0024]–[0026]. Both Aoyama and Akasaka rely on large spacers, so a POSA would not be motivated to combine Hsu823 with either Aoyama or Akasaka.

VI. CONCLUSION

AICP respectfully requests that the Board refuse to institute *inter partes* review for the reasons stated herein.

Dated: September 25, 2025

Respectfully submitted,

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Attorney for Patent Owner

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CERTIFICATE OF SERVICE

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), copies of the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 TO PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 8,198,686 and Exhibit 2058 were served via email to counsel of record for Petitioners as follows:

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned hereby certifies that this brief complies with the type-volume limitation of 37 C.F.R. § 42.24 because this brief contains 4,133 words as calculated by Microsoft Word, excluding the items exempted under 37 C.F.R. § 42.24.

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