

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

Petitioner,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,

Patent Owner.

IPR2025-00830

U.S. Patent 8,253,180

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT 8,253,180**

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EXHIBIT LIST

Exhibit	Description
1001	U.S. Patent 8,253,180 to Hirase et al. (“the ’180 patent”)
1002	File History of U.S. Patent 8,253,180 (“’180 File History”)
1003	Declaration of Dr. Jack Lee in Support of IPR Petition
1004	CV of Dr. Jack Lee
1005	Translated Excerpts from JP File History
1006	U.S. Patent 7,579,227 to Hirase, et al. (“the ’227 patent”)
1007	U.S. Patent 7,923,764 to Hirase et al. (“the ’764 patent”)
1008	Reserved
1009	U.S. Publication 2003/0025135 to Matsumoto, et al. (“Matsumoto”)
1010	JP2003-258241 to Kajiyama (“JP-Kajiyama”)
1011	Certified Translation of JP2003-258241 to Kajiyama (“Kajiyama”)
1012	Reserved
1013	U.S. Publication 2005/0051856 to Ono, et al. (“Ono”)
1014	Reserved
1015	Reserved
1016	Reserved
1017	Reserved
1018	Wilk, G. D., et al., “High-k gate dielectrics: Current status and materials properties considerations,” Journal of Applied Physics, Vol. 89, No. 10, pp. 5243-5275, May 15, 2001 (“Wilk”)

Exhibit	Description
1019	Reserved
1020	Reserved
1021	Reserved
1022	Reserved
1023	U.S. Patent 6,306,712 to Rodder, et al. (“Rodder”)
1024	Sim, J. H., et al., “Effects of ALD HfO ₂ thickness on charge trapping and mobility,” Microelectronic Engineering, Vol. 80, pp. 218-221, June 17, 2005 (“Sim”)
1025	Reserved
1026	Declaration of June Ann Munford
1027	U.S. Publication 2002/0063299 to Kamata, et al. (“Kamata”)
1028	U.S. Publication 2006/0091432 to Guha, et al. (“Guha”)
1029	Koyama, M., et al., “Effects of Nitrogen in HfSiON Gate Dielectric on the Electrical and Thermal Characteristics,” Digest of International Electron Devices Meeting, pp. 849-852, Dec. 8-11, 2002 (“Koyama”)
1030	U.S. Patent 6,664,577 to Takayanagi (“Takayanagi”)
1031	Reserved
1032	Houssa, M., “High-k Dielectrics to Houssa” (IOP Publishing Ltd. 2004) (“Houssa”)
1033	Plummer, J., et al., “Silicon VLSI Technology: Fundamentals, Practice and Modeling” (Prentice Hall 2000) (“Plummer”)
1034	Wolf, S., “Silicon Processing for the VLSI Era, Volume 4 – Deep-Submicron Process Technology” (Lattice 2002) (“Wolf”)

Exhibit	Description
1035	Reserved
1036	Reserved
1037	Lee, S. J., et al. “High Quality Ultra Thin CVD HfO ₂ Gate Stack with Poly-Si Gate Electrode,” Digest of International Electron Devices Meeting, pp. 31-34, Dec. 10-13, 2000 (“Lee”)
1038	Campbell, “The Science and Engineering of Microelectronic Fabrication”, Second Edition (2001) (“Campbell”)
1039	Reserved
1040	JP2005-064190 to Ono with certified translation (“JP-Ono”)
1041	N. Weste and D. Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, Third Edition (Pearson/Addison Wesley, 2005) (“Weste”)
1042	Reserved
1043	Reserved
1044	Reserved
1045	U.S. Publication 2005/0093084 to Wang, et al. (“Wang”)
1046	Reserved
1047	Reserved
1048	Reserved
1049	Lee, B.H., et al., “Ultrathin Hafnium Oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application,” Digest of International Electron Devices Meeting, pp. 133-36, Dec. 5-8, 1999 (“Lee-1999”)
1050	Reserved

Exhibit	Description
1051	U.S. Publication 2005/0139932 to Cho, et al. (“Cho”)
1052	Albertin, K.F., et al., “Study of PECVD SiO _x N _y films dielectric properties with different nitrogen concentration utilizing MOS capacitors,” Microelectronic Engineering, Vol. 77, pp. 144-49 (2005)

I. Introduction

Taiwan Semiconductor Manufacturing Company, Limited (“Petitioner”) petitions for *inter partes* review of claims 1-22 of U.S. Patent 8,253,180 (“’180 patent”; TSMC-1001).

The ’180 patent purports to improve the driving power and reliability of a metal insulator semiconductor field-effect transistor by extending a high-k gate insulating film beyond the gate electrode. (TSMC-1001, 1:16-23, 2:8-19, 2:39-46.) This concept was known before the ’180 patent, a fact Applicant acquiesced to during Japanese prosecution.

Petitioner demonstrates the challenged claims are unpatentable.

II. Grounds for Standing

Petitioner certifies the ’180 patent is available for IPR and it is not barred or estopped from requesting IPR on the grounds herein.

III. Identification of Challenge

A. Prior Art

The ’180 patent, filed March 1, 2011, claims priority through divisional applications to U.S. Patent 7,579,227 (“’227 patent”) which claims priority to JP2005-227457 (“JP Application”), filed August 5, 2005. Petitioner does not acquiesce the ’180 patent is entitled to benefit of any prior U.S. patents or the JP

Application. Regardless, each applied reference was filed or published before August 5, 2005.

1. **U.S. Publication 2002/0063299 to Kamata, et al.** (“Kamata”; TSMC-1027), published May 30, 2002, is prior art under 35 U.S.C. §102(b).¹
2. **U.S. Publication 2006/0091432 to Guha, et al.** (“Guha”; TSMC-1028), filed November 2, 2004, is prior art under §102(e).
3. **U.S. Publication 2003/0025135 to Matsumoto, et al.** (“Matsumoto”; TSMC-1009), published February 6, 2003, is prior art under §102(b).
4. **U.S. Publication 2005/0093084 to Wang, et al.** (“Wang”; TSMC-1045), published May 5, 2005, is prior art under §102(b).
5. **“Effects of Nitrogen in HfSiON Gate Dielectric on the Electrical and Thermal Characteristics” to Koyama, et al.** (“Koyama”; TSMC-1029), published in 2002, is prior art under §102(b). (TSMC-1026, ¶¶22-25.)
6. **U.S. Patent 6,306,712 to Rodder, et al.** (“Rodder”; TSMC-1023), issued October 23, 2001, is prior art under §102(b).

¹ Pre-AIA 35 U.S.C. §102 applies.

7. **“Effects of ALD HfO₂ thickness on charge trapping and mobility” to Sim** (“Sim”; TSMC-1024), published June 17, 2005, is prior art under §102(b). (TSMC-1026, ¶¶18-21.)

8. **“High-k gate dielectrics: Current status and materials properties considerations” to Wilk, et al.** (“Wilk”; TSMC-1018), published in 2001, is prior art under §102(b). (TSMC-1026, ¶¶14-17.)

9. **U.S. Patent 6,664,577 to Takayanagi** (“Takayanagi”; TSMC-1030), issued December 16, 2003, is prior art under §102(b).

10. **U.S. Publication 2005/0051856 to Ono, et al.** (“Ono”; TSMC-1013), published March 10, 2005, is prior art under §102(b).

B. Grounds for Challenge

Ground		Claims	Prior Art
1	103	1-3, 5-6, 13-19, 21-22	Kamata
2	103	4, 12	Kamata-Wang
3	103	7	Kamata-Koyama
4	103	8-9	Kamata-Rodder
5	103	11	Kamata-Sim
6	103	18-19	Kamata-Wilk
7	103	20	Kamata-Takayanagi
8	103	1-6, 12-14, 16-18, 21-22	Guha
9	103	7	Guha-Koyama

Ground		Claims	Prior Art
10	103	11	Guha-Sim
11	103	1, 5, 13-20	Matsumoto
12	103	8-9	Matsumoto-Rodder
13	103	10	Matsumoto-Ono

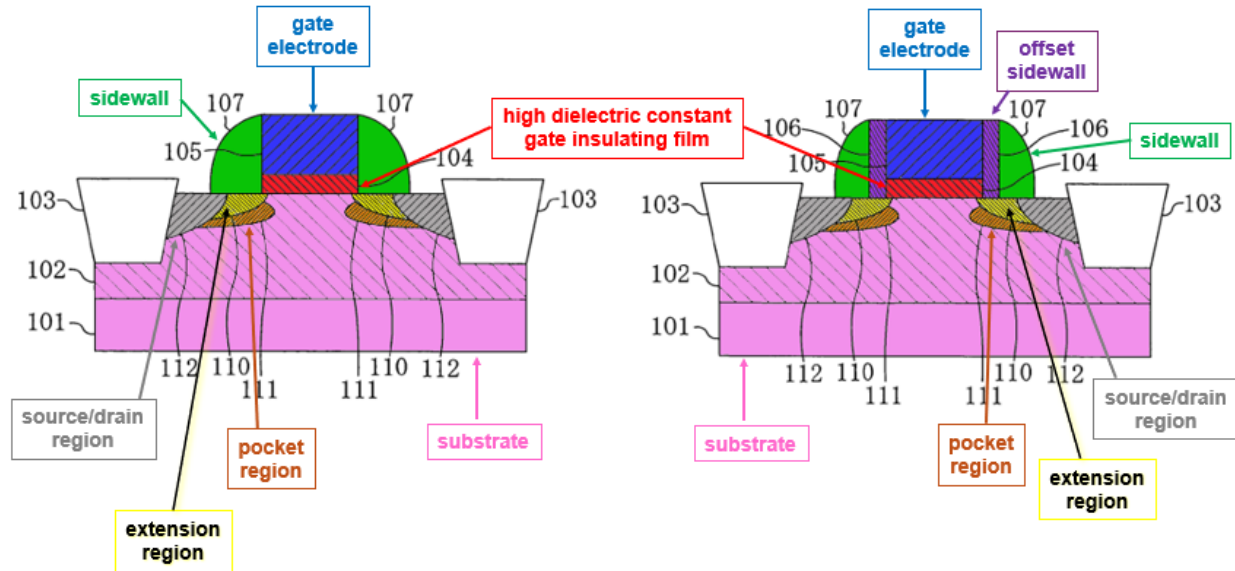
IV. '180 Patent

A. Applicant Admitted Prior Art (“AAPA”)

The '180 patent recognized that, prior to August 2005, semiconductor devices had used “a high dielectric constant film formed of a Hf based oxide, Al based oxide or the like” as a gate insulating film existed. (TSMC-1001, 1:25-33.) It describes two prior art metal insulator semiconductor field-effect transistors (MISFETs), depicted in Figures 16A-16B, each including a high dielectric constant gate insulating film² 104 (shaded red) interposed between gate electrode 105 (shaded blue) and the substrate. In the Figure 16A device, sidewall 107 (shaded green) is formed on each side of gate electrode 105. (TSMC-1001, 1:45-46.) In the

² The terms “gate dielectric” and “gate insulating film” are used interchangeably. The term “high dielectric constant” is also referred to as “high-k” in this Petition and prior art documents.

Figure 16B device, an additional offset sidewall 106 (shaded purple) is interposed between sidewall 107 and gate electrode 105. (TSMC-1001, 1:54-57.)



'180 Patent, Figure³ 16A

'180 Patent, Figure 16B

In these devices, the “side end portions” of the high-k film “are in direct contact with sidewalls.” (TSMC-1001, 1:63-66.) The '180 patent purports to address issues with this arrangement by extending the high-k film under the “sidewalls to prevent end portions of the [high-k] film from being in contact with the sidewalls.” (TSMC-1001, 2:12-18.)

³ All shading and annotations in figures added, unless otherwise noted.

The concept of extending a high-k gate insulating film from under the gate electrode to beneath sidewalls was well-known. (*E.g.*, §§IV.B.2, IV.D.2, V, XII, XV.)

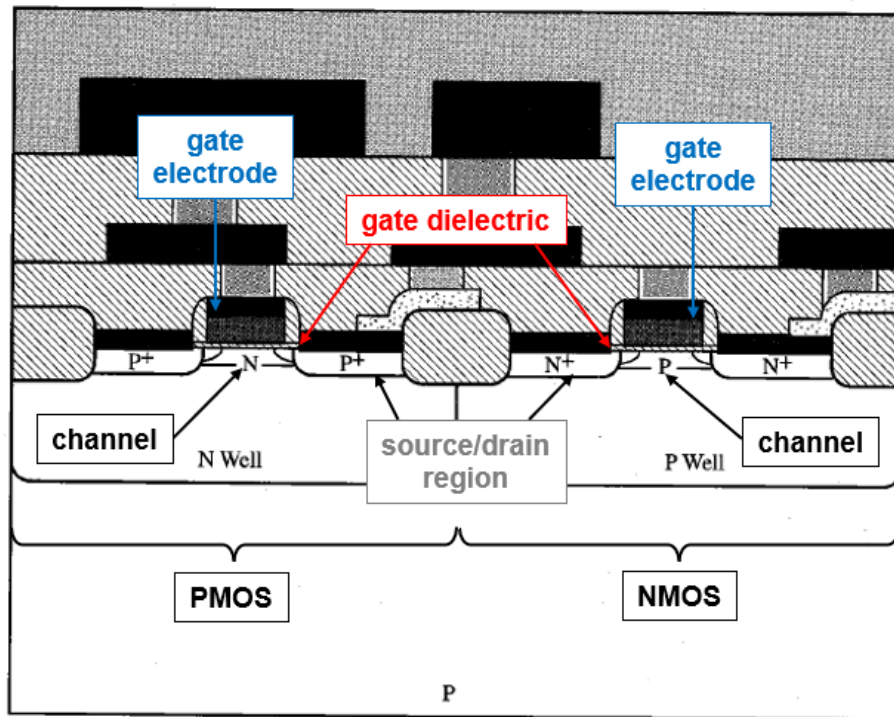
B. Technical Background

A semiconductor device, at its most basic, exploits the properties of semiconductor materials, e.g., silicon. Petitioner describes field effect transistors (FETs) in further detail below.

1. MISFET/MOSFET

MISFETs⁴ have a **source/drain** for current input/output. (TSMC-1003, ¶36; TSMC-1033, 76-82.) MISFETs also have a **gate** above a **channel** region between the source and drain. (TSMC-1003, ¶36; TSMC-1033, 71-76.) The **gate** includes a **gate electrode** and **gate dielectric** (also referred to as a gate insulating film) separating the gate electrode from the channel region. (TSMC-1003, ¶36; TSMC-1033, 71-76, Fig. 1-11.) Applying voltage to the gate electrode controls the channel region to connect (ON state) or disconnect (OFF state) the source and drain. (TSMC-1003, ¶37; TSMC-1041, 8-9.)

⁴ “MISFET” and “MOSFET” (“Metal-*Oxide*-Semiconductor Field-Effect Transistor”) are interchangeable. (TSMC-1003, ¶36.)



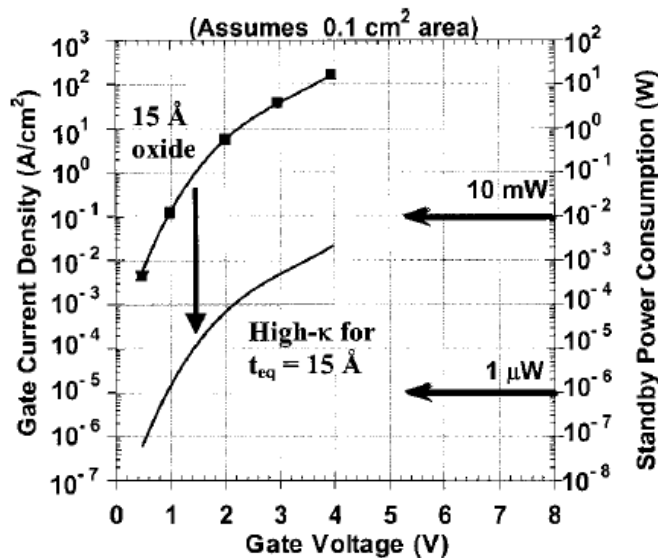
Plummer, Figure 1-11

2. Gate Insulating Film

a. Materials

For decades before the '180 patent, silicon dioxide (SiO_2) was the primary material used for gate dielectrics in MOSFETs. (TSMC-1003, ¶46; TSMC-1033, 53; TSMC-1032, 3-4.) As gate dielectrics continued to shrink in thickness (e.g., below 1.5 nm), use of SiO_2 became untenable, because the amount of gate-to-channel tunneling leakage-current passing through the gate dielectric prevents the gate electrode from effectively controlling the ON/OFF states of the FET. (TSMC-1003, ¶46; TSMC-1034, 4-5.)

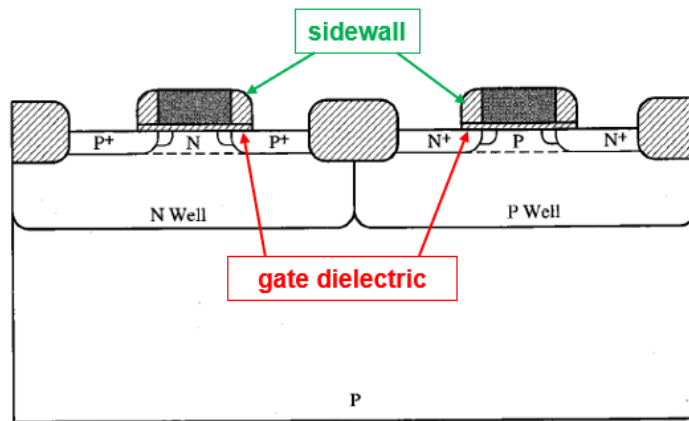
High-k dielectrics, like Hf-based oxides, Ta₂O₅, or ZrO₂, replaced SiO₂ to address these challenges. (TSMC-1003, ¶¶47-48; TSMC-1034, 146.) For example, it was known by 2005 that, as compared to SiO₂, high-k materials significantly reduce the amount of leakage current and, thus, improve energy efficiency. (TSMC-1003, ¶49; TSMC-1018, 5250, Figure 5 (below); TSMC-1034, 146-47.)



Wilk, Figure 5

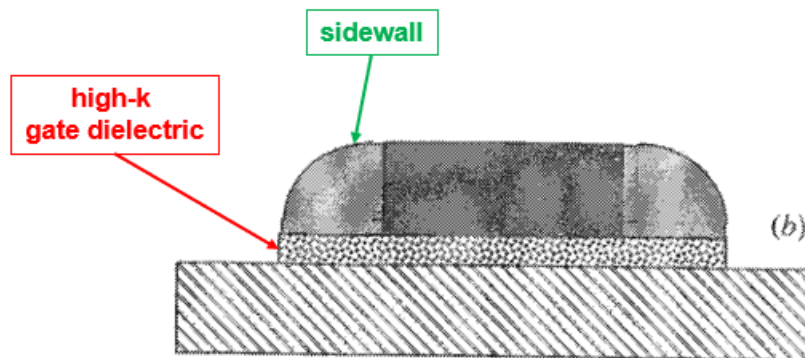
b. Extended Gate Insulating Films

Prior to 2005, it was common practice to extend the gate dielectric from under the gate electrode to under a device's sidewalls. For example, Plummer depicts a CMOS device having an extended gate dielectric in the NMOS and PMOS transistors. (TSMC-1003, ¶50; TSMC-1033, 82-83.)



Plummer, Figure 2-34

Houssa discloses another example using a high-k material as the gate insulating film that extends from under the gate electrode to under the sidewalls. (TSMC-1032, 510, Figure 5.1.9(b) (below).)

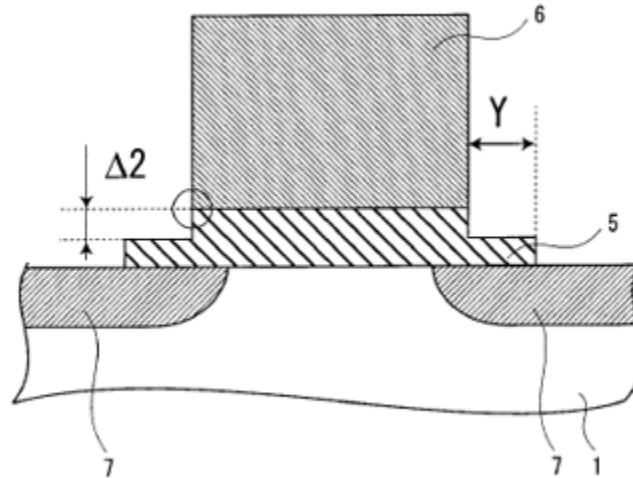


Houssa, Figure 5.1.9(b)

JP Publication 2005-064190 (“JP-Ono”⁵; TSMC-1040), filed two years before the ’180 patent, examines how adjusting the length of the gate dielectric

⁵ A certified translation of JP-Ono is included with TSMC-1040.

from the outer edge of the gate electrode (Y) (i.e., how far the gate dielectric protrudes from under the gate electrode) affects electric field distribution, noting that “increasing Y effectively suppresses the electric field intensity on the source-drain region by thinning the gate insulating film.” (TSMC-1040, ¶87.)



JP-Ono, Figure 3

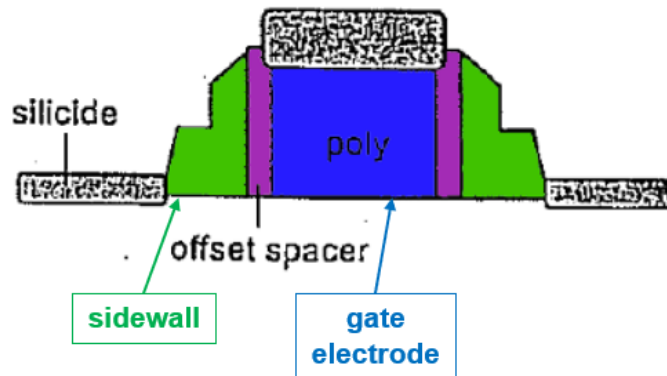
3. Sidewalls

Another common device feature is sidewalls, insulating structures formed on or proximate to a gate electrode’s side surfaces. Sometimes, the terms “sidewall,” “spacer,” and “sidewall spacer” are used interchangeably. (TSMC-1003, ¶58.) Sidewalls serve a variety of purposes and functions such as defining the source/drain region, providing isolation, protecting the gate during subsequent fabrication, and controlling the gate width in the gate length direction. (*Id.*)

As a non-limiting example, spacers may be used for “[c]ontrolling the position of the edge of the SDE [source/drain extension] region with respect to the

gate edge” to achieve optimal amount of overlap between the SDE and gate edge.

(TSMC-1034, 217.) As shown below, “an offset-spacer is fabricated on the side of the gate after the gate-poly is etched (but before the SDE implant step is carried out ...),” with offset-spacer width “varied from zero (no-spacer) to some upper-bound (e.g., 50-nm)” to achieve optimum device characteristics. (*Id.*)



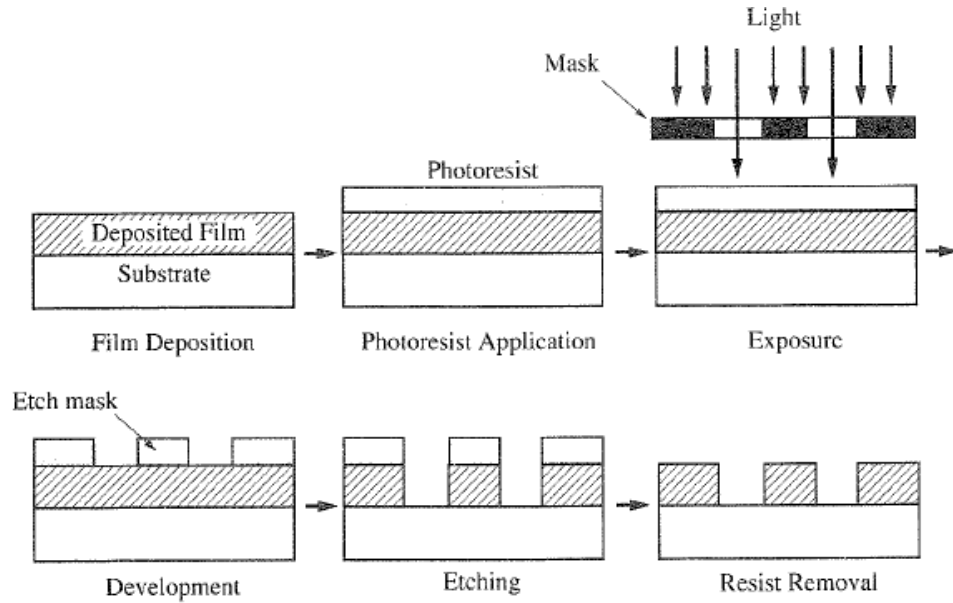
Wolf, Figure 5-25

4. Etching Properties

In semiconductor devices, thin films are often first deposited on the wafer and then selectively removed by etching to leave the desired pattern of the film.

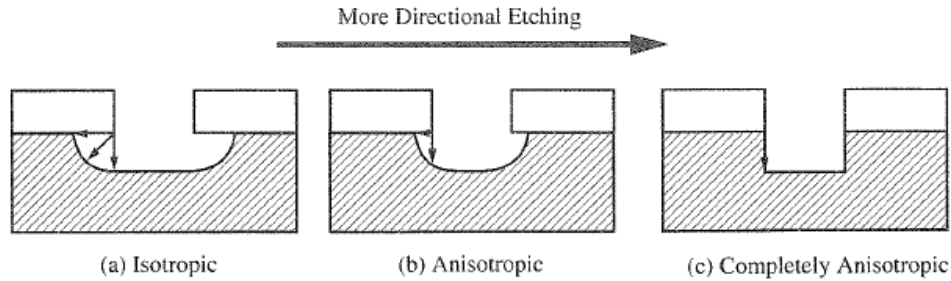
(TSMC-1003, ¶60; TSMC-1033, 609-11.) The desired pattern is often defined by placing a mask on the surface before etching; the mask is removed after etching.

(TSMC-1003, ¶60; TSMC-1033, 609-10, Figure 10-1 (below).)



Plummer, Figure 10-1

Etching is performed in a “wet” or “dry” environment. (TSMC-1003, ¶61; TSMC-1033, 609, 612-37.) Wet etching involves use of liquid etchants (e.g., hydrofluoric acid) whereas dry etching involves use of gas-phase etchants in a plasma. (TSMC-1003, ¶61; TSMC-1033, 609.) Etching processes are also described based on the relative etch rates in different directions. (TSMC-1003, ¶60; TSMC-1033, 610-11.) Isotropic etching occurs when the etch rate is the same in all directions, resulting in a semicircular etch profile as shown in Figure 10-3(a) below. Most wet chemical etchants etch isotropically. (TSMC-1033, 610-13.) Anisotropic etching occurs where there is little or no etching in the lateral direction. (TSMC-1033, 611, Figure 10-3(b), (c) (below).)



Plummer, Figure 10-3

C. '180 Patent Overview

The '180 patent presents four device embodiments (first-fourth embodiments) and their associated fabrication methods (fifth-eighth embodiments). In each embodiment, the high-k gate insulating film (shaded red) extends beyond the gate electrode to under the sidewall(s). (TSMC-1001, Figures 1-2, 5, 9 (below).) The embodiments differ in the number of sidewalls (one/two) and the presence of a buffer layer under the gate insulating film (fourth embodiment). The embodiments also vary in the relative thickness of the gate insulating film under the gate electrode and sidewalls, though this difference is not relevant to most '180 patent claims.

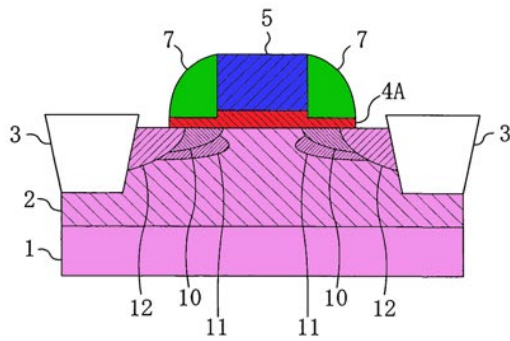


Figure 1—First Embodiment

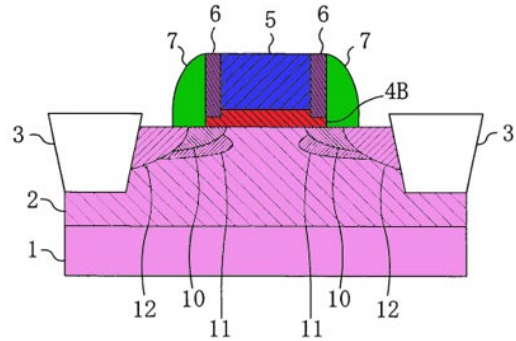


Figure 2—Second Embodiment

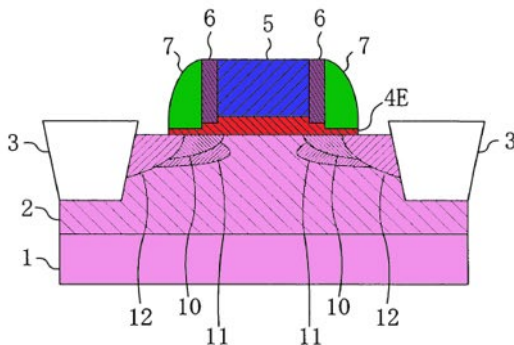


Figure 5—Third Embodiment

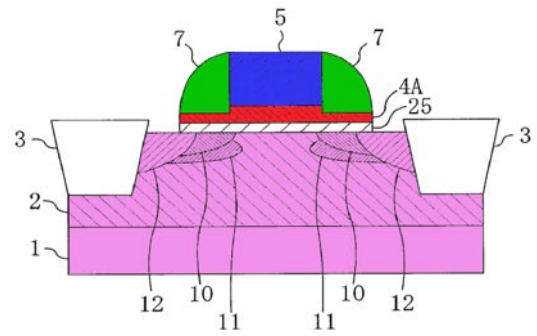


Figure 9—Fourth Embodiment

Each embodiment includes a modification in which “a side portion of the high dielectric constant gate insulating film ... is removed in a notch shape, so that a notch 20 is provided,” illustrated in Figure 6 below for the first embodiment modification. (TSMC-1001, 7:4-9, 14:28-35, Figure 6, 8:31-36, 15:58-65, Figure 7, 11:37-42, 17:61-67, Figure 8, 12:55-13:1, Figure 10.)

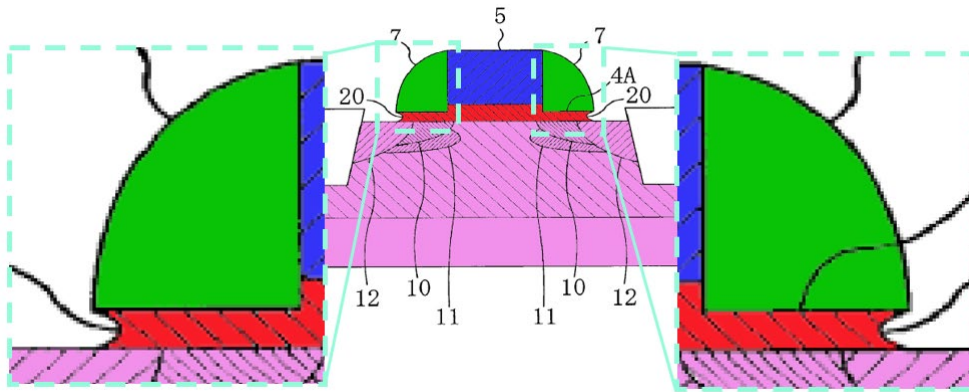


Figure 6 with enlargements

The concept of changing the shape and/or location of the end of a dielectric was known, long before the '180 patent. (*E.g.*, §§IV.D.2, V, XII, XV.)

D. Prosecution History

1. '180 Patent

The filed application claims were rejected over U.S. Patent 6,992,358 to Hieda (“Hieda”). (TSMC-1002, 123-27.) In response, Applicant argued Hieda did not disclose the “predetermined distance” limitation of prosecution claim 21 (issued claim 1) because “the high dielectric constant gate insulating film **does not extend so as to reach the outer end of the insulating sidewall.**” (TSMC-1002, 151.) Applicant repeatedly stressed this requirement for the “predetermined distance” limitation:

[T]he recited high dielectric constant gate electrode [*sic*] recited by claim 21 does not extend so far such that it is disposed beneath the outer end of the insulating sidewall, as is shown, for example, in the

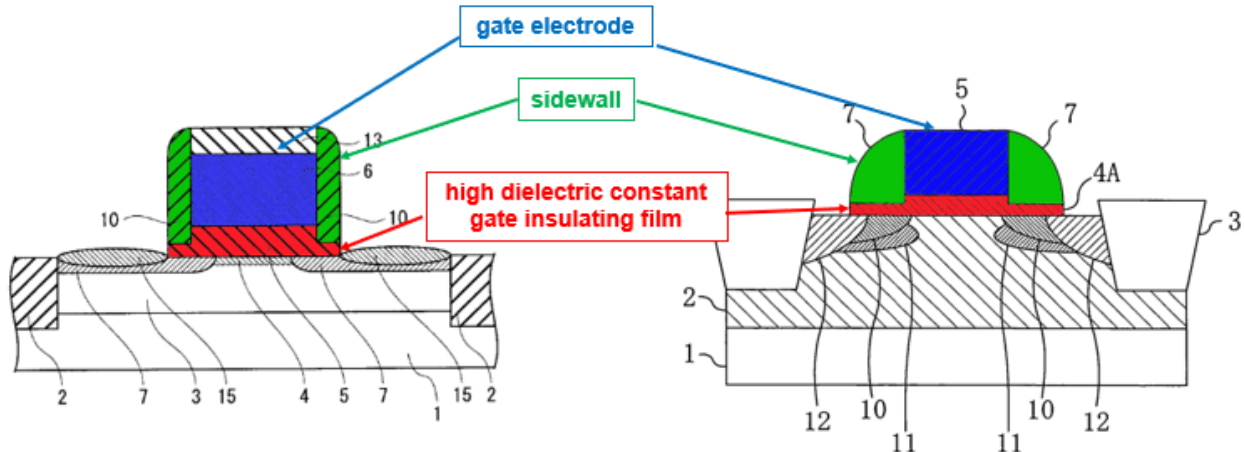
exemplary embodiments of Figs. 6 and 10. **It is disposed inwardly of the outer end of the insulating sidewall.**

(TSMC-1002, 152; *see also id.* (“high dielectric constant gate insulating film 4a is not disposed underneath the outer ends of the insulating sidewalls 7”).)

The Examiner maintained the rejection. (TSMC-1002, 193-97.) Applicant traversed, repeating the same “predetermined distance” arguments and further contending Hieda’s gate insulating film does not “extend under both the gate electrode and first insulating sidewalls.” (TSMC-1002, 215.) The Examiner subsequently allowed the claims. (TSMC-1002, 193-97, 214-15, 225-27.)

2. JP Application

The JP Application was filed with the same device claim originally filed with the U.S. application for the ’227 patent. (TSMC-1005, 1.) The JP-Examiner found this claim scope unpatentable, citing JP-Ono discussed in §IV.B.2.b (Figure 23-left) and WO2004/017418 which both disclose a high-k gate insulating film extending from under the gate electrode to under the sidewalls. (TSMC-1005, 4-6.)



JP-Ono, Figure 23

'180 Patent, Figure 1

In response, Applicant narrowed the independent claim. (TSMC-1005, 8.)

The JP-Examiner rejected the amended claim based on both JP2003-258241 ("Kajiyama") and JP2004-241755 ("JP-Matsumoto"), which both have extended gate insulating films. (TSMC-1005, 14-16.) The JP-Examiner maintained the rejection of the notch claim based on JP-Ono. (TSMC-1005, 15.) Applicant further narrowed the claim to obtain allowance. (TSMC-1005, 18.)

Despite the materiality of the JP notices of refusal, Applicant did not inform the U.S. Examiner of the rejections by the JP-Examiner during pendency of the '180 patent.

E. Claim Construction

Petitioner does not believe any claims require construction to resolve the patentability disputes in this proceeding. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

F. Level of Ordinary Skill in the Art

A POSITA would have had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. (TSMC-1003, ¶31.)

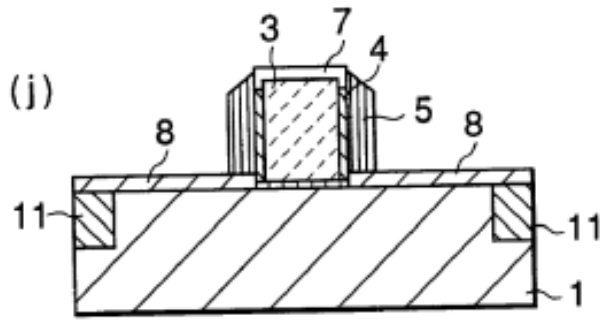
Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education. (*Id.*)

V. GROUND 1: Kamata Renders Claims 1-3, 5-6, 13-19, 21-22⁶ Obvious.

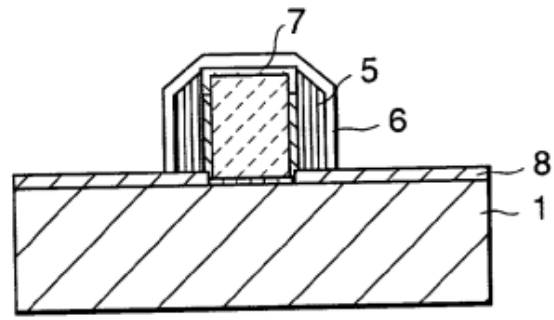
A. Overview

While numerous embodiments are invalidating, this Petition focuses on Kamata's first (Figure 1B(j)), fourth (Figure 5(c)), and ninth (Figure 10(b)) embodiments. Each embodiment's device includes a gate electrode, a gate insulating film, and a sidewall structure having first sidewall film 4 and second sidewall film 5. (TSMC-1027, ¶¶50-61 (first embodiment), 68 (fourth embodiment), 93-94 (ninth embodiment).) Each embodiment's gate insulating film extends from under the gate electrode to under only a portion of the sidewall structure.

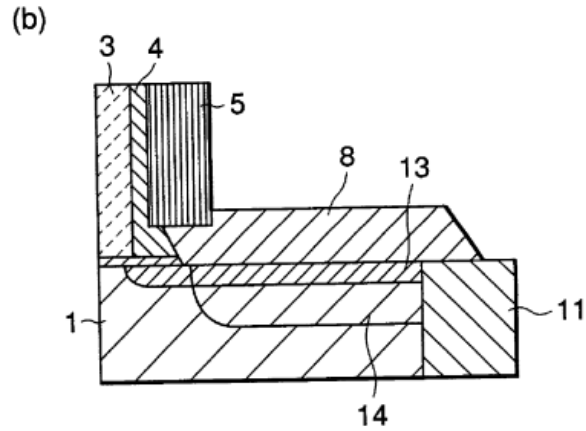
⁶ Challenged claims listing is provided in the Appendix.



Kamata, Figure 1B(j)
(First Embodiment)



Kamata, Figure 5(c)
(Fourth Embodiment)



Kamata, Figure 10(b)
(Ninth Embodiment)

B. Independent Claim 1

1. Preamble [1P]

Kamata’s first, fourth, and ninth embodiments each discloses a “*semiconductor device*”⁷: “invention relates to a **semiconductor device**.”⁸ (TSMC-1027, ¶¶3, 8; TSMC-1027, ¶¶32, 50 (first embodiment), 36, 68 (fourth embodiment), 93-94 (ninth embodiment); TSMC-1003, ¶89.)

2. Limitation [1A]

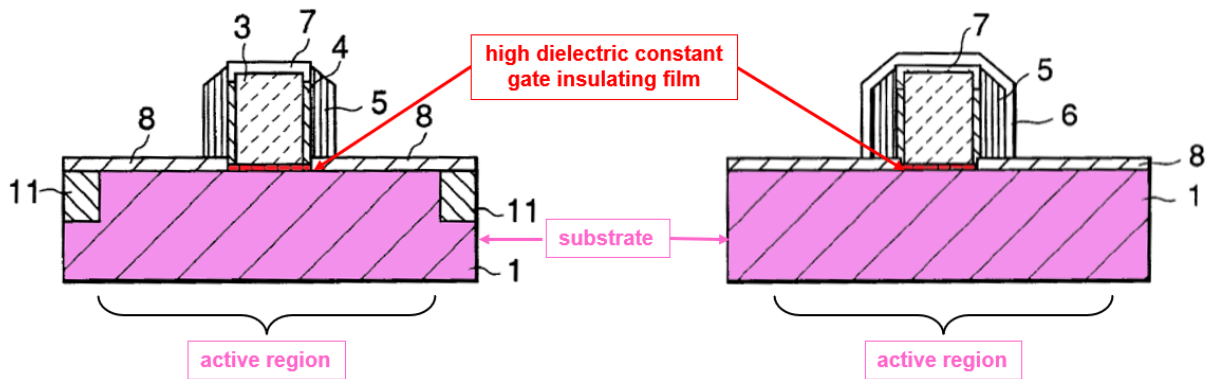
Kamata’s first, fourth, and ninth embodiments each discloses “*a high dielectric constant gate insulating film formed on an active region in a substrate*” [1A]. (TSMC-1003, ¶¶90-94.)

Each device has “semiconductor **substrate** 1 made of silicon” (shaded pink). (TSMC-1027, ¶¶50, 68 (“parts [of fourth embodiment] that are same as or similar to those of the first embodiment are denoted respectively by the same reference symbols”), 94 (“portions [of ninth embodiment] that are same as or similar to those FIGS. 1A through 2C are denoted respectively by the same reference symbols”).) Kamata explains that “shallow trench isolation zones (STI) 11” are formed on the substrate “to define an element region 1a” and refers to element region 1a as an

⁷ Claim language indicated by italics throughout.

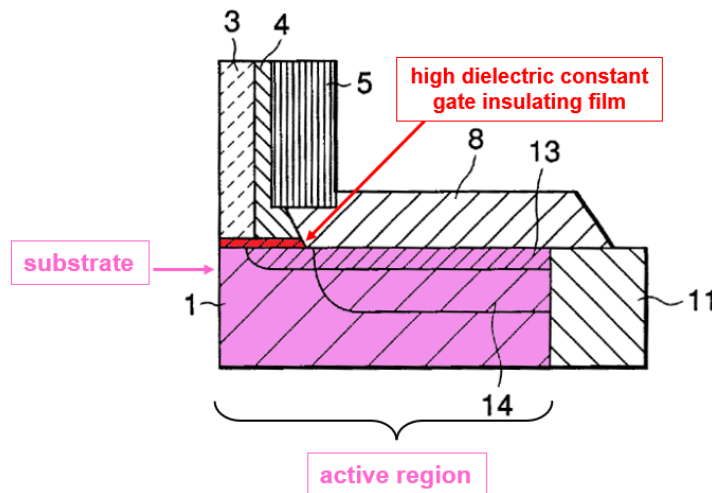
⁸ Unless otherwise noted, all emphasis added.

“active region.” (TSMC-1027, ¶¶50, 68, 94, 99-100 (referring to element region 1a of Figure 1A(a) as an “active region” and indicating same parts are “denoted ... by the same reference symbols”); *Google LLC v. Jenam Tech, LLC*, IPR2021-00630, 2022 WL 4287797, *9 n.9 (P.T.A.B. Sept. 16, 2022) (applying same disclosures where “figures refer to corresponding features using the same reference numbers”); TSMC-1001, 1:41-43 (“region of the well 102 surrounded by the STI serves as an active region of a substrate 101”); TSMC-1003, ¶91.) A POSITA would have understood element region 1a, identified by STI, is an “*active region in a substrate.*” (TSMC-1003, ¶91.)



**Kamata, Figures 1B(j)
(First Embodiment)**

**Kamata, Figure 5(c)
(Fourth Embodiment)**



**Kamata, Figure 10(b)
(Ninth Embodiment)**

Each embodiment includes film 2 (shaded red) formed on the active region under the gate electrode extending beneath the sidewall structure. (*E.g.*, TSMC-1027, ¶¶56, 68, 94; §§V.B.3-5; *Unified Pats., LLC v. Oceana Innovations LLC*, No. IPR2020-01463, 2022 WL 500391, *17 (P.T.A.B. Feb. 14, 2022) (“[A] patent

drawing may serve as prior art ‘without referring to the surrounding description’ if ‘the prior art features are clearly disclosed by the drawing.’”) (citation omitted.)

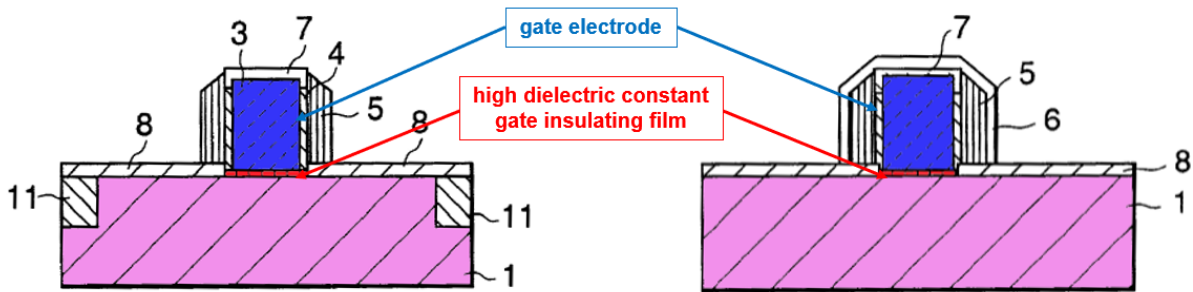
“[G]ate insulating film” 2 is disclosed as “**a high dielectric constant film** such as an oxide film with higher dielectric constant than the silicon oxide.” (TSMC-1027, ¶52; TSMC-1027, ¶53 (listing exemplary high-k films including Hf oxides or silicates).)

Kamata therefore discloses a “*high dielectric constant gate insulating film formed on an active region in a substrate.*” (E.g., TSMC-1027, ¶73 (referring to “gate insulating film 2”), ¶¶8-10 (“present invention” device includes “gate insulating film formed on a surface of the silicon substrate”), claim 1; TSMC-1003, ¶94.)

3. Limitation [1B]

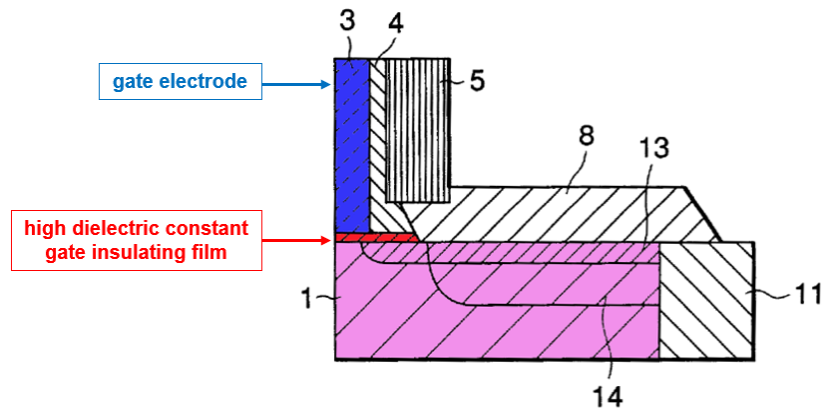
Kamata’s first, fourth, and ninth embodiments each discloses “*a gate electrode formed on the high dielectric constant gate insulating film*” [1B]. (TSMC-1003, ¶¶95-96.)

As shown below, each embodiment’s device has gate electrode 3 (shaded blue) formed on film 2 (“*gate insulating film*”). (TSMC-1003, ¶96; TSMC-1027, ¶50 (explaining gate electrode 3 is “formed by depositing polycrystalline silicon” and performing a subsequent anisotropic etch), ¶¶68, 94, Figures 1A(a)-(c), claim 1 (reciting device with “gate electrode formed on the gate insulating film”).)



**Kamata, Figures 1B(j)
(First Embodiment)**

**Kamata, Figure 5(c)
(Fourth Embodiment)**



**Kamata, Figure 10(b)
(Ninth Embodiment)**

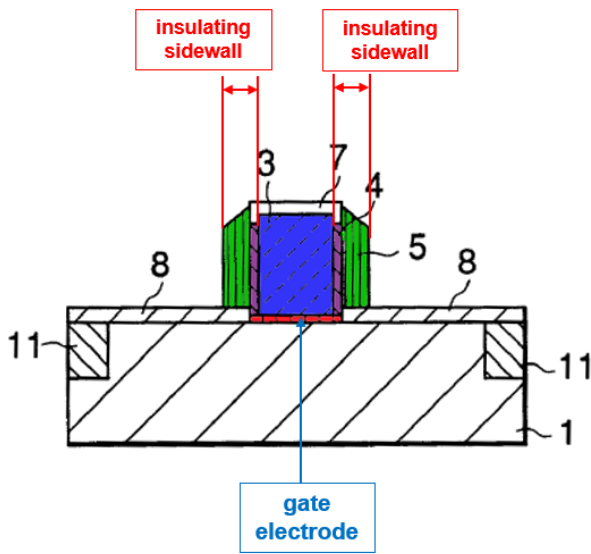
4. Limitation [1C]

Kamata's first, fourth, and ninth embodiments each discloses "*a insulating sidewall formed on each side surface of the gate electrode*" [1C]. (TSMC-1003, ¶¶97-101.)

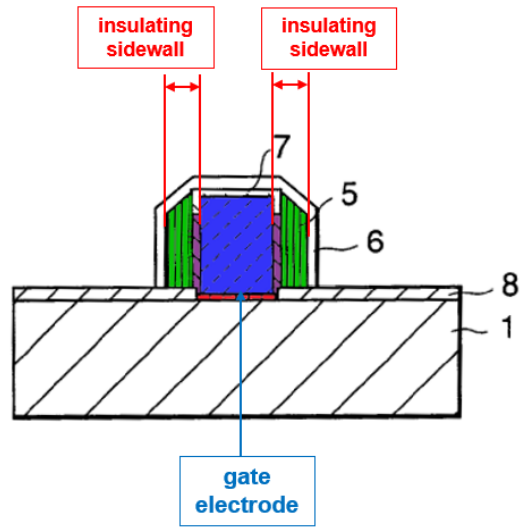
As shown in Figures 1B(j) and 5(c), each device includes sidewall film 4 (shaded purple) and sidewall film 5 (shaded green) formed on the gate electrode's side surfaces. (TSMC-1027, ¶¶8-16 ("first aspect of the present invention

[provides] a semiconductor device comprising ... multilayer type sidewall films [] formed on the respective side surfaces of the gate electrode”), 57 (referring to film 5 as “sidewall film 5”), 74 (referring to film 4 as “sidewall film 4”).) Sidewall film 4 is a silicon oxide film, and sidewall film 5 is a silicon nitride film—both are insulating films. (TSMC-1027, ¶¶50 (referring to “silicon nitride film (Si_3N_4) 5”), 58 (referring to “silicon oxide film 4”), 68.) Sidewall film 4 and sidewall film 5 are collectively an “*insulating sidewall*,” consistent with the ’180 patent’s disclosure.⁹ (TSMC-1003, ¶99.)

⁹ The ’180 patent uses the term “insulating sidewall” to refer to a single component (TSMC-1001, 6:3-4), a collective structure of two components (TSMC-1001, 2:58-63), and as a component having multiple layers (TSMC-1001, 20:43-52).

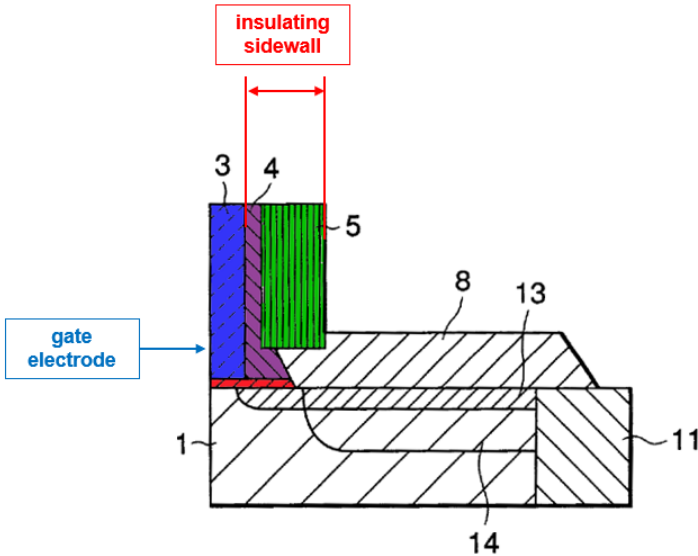


**Kamata, Figure 1B(j)
(First Embodiment)**



**Kamata, Figure 5(c)
(Fourth Embodiment)**

Figure 10(b) depicts a portion of the ninth embodiment device. As shown, the device includes sidewall film 4 (shaded purple) and sidewall film 5 (shaded green) formed on the right side surface of the gate electrode. (TSMC-1027, ¶¶8-16, 57, 74; *see also* TSMC-1027, ¶¶50, 58, 94.) A POSITA would have understood this device includes corresponding insulating sidewalls on the left side surface of the gate. (TSMC-1003, ¶101 n.4.) As above, sidewall film 4 and sidewall film 5 are collectively an “*insulating sidewall*.” (TSMC-1003, ¶101.)



Kamata, Figure 10(b) (Ninth Embodiment)

5. Limitations [1D]-[1E]

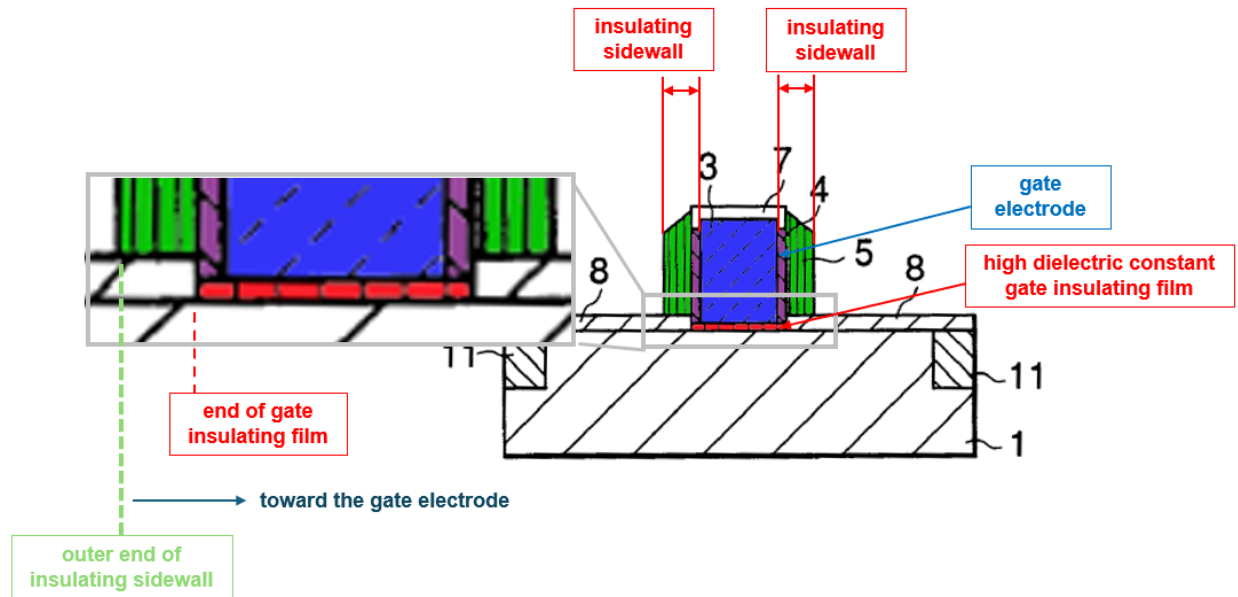
Kamata’s first, fourth, and ninth embodiments each discloses “*high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall*” [1D] and “*an end of the high dielectric constant gate insulating film under the insulating sidewall is located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode*” [1E]. (TSMC-1003, ¶¶102-08.)

a. First/Fourth Embodiments

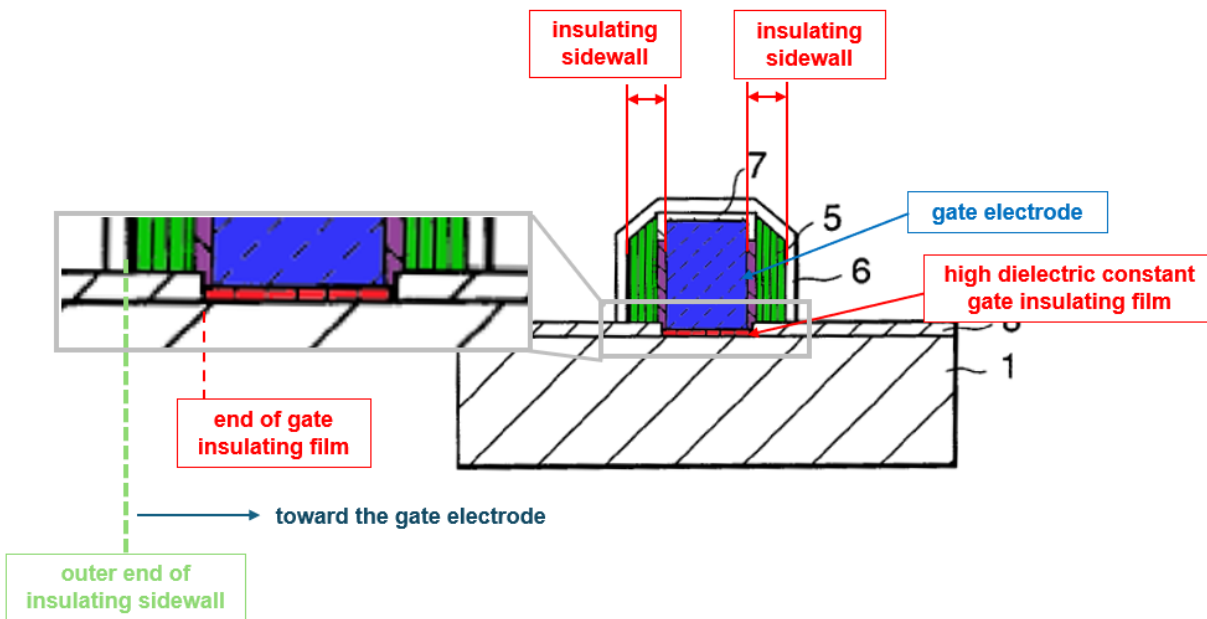
As shown in Figures 1B(j) and 5(c), high-k gate insulating film 2 is an uninterrupted layer (as evidenced by absence of gaps) extending from under the gate electrode (shaded blue) to under sidewall 4 (shaded purple), which is a portion

of the “insulating sidewall.” (TSMC-1003, ¶103; *Unified*, 2022 WL 500391, *17.)

This is confirmed by Kamata’s manufacturing process, where gate insulating film 2 is etched to its final length, extending under sidewall 4, after gate electrode 3 and sidewall 5 are formed. (TSMC-1027, Figures 1A(f), 1B(g), ¶¶50, 56, 68 (fourth embodiment); TSMC-1003, ¶105.) Gate insulating film 2 of Kamata’s first/fourth embodiments is “continuously formed so as to extend from under the gate electrode to under the insulating sidewall” [1D]. (TSMC-1003, ¶104.)



**Kamata, Figure 1B(j) with enlargement
(First Embodiment)**



**Kamata, Figure 5(c) with enlargement
(Fourth Embodiment)**

In Kamata's first and fourth embodiment devices, the end of the gate insulating film is perpendicular to the substrate surface. As shown in Figures 1B(j) and 5(c) above, the end of the gate insulating film is disposed at a distance inward from the outer end of sidewall 5 (outer end of "insulating sidewall") toward the gate electrode. (TSMC-1003, ¶106.) The distance which the end of the gate insulating film extends inward toward the gate electrode is set by Kamata's manufacturing process discussed above. (*Id.*) Thus, the end of high-k film in the first and fourth embodiments is "located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode" [1E], consistent with the '180 patent's disclosure. (TSMC-1001, 21:1-7 (high-k film's side surfaces "may be

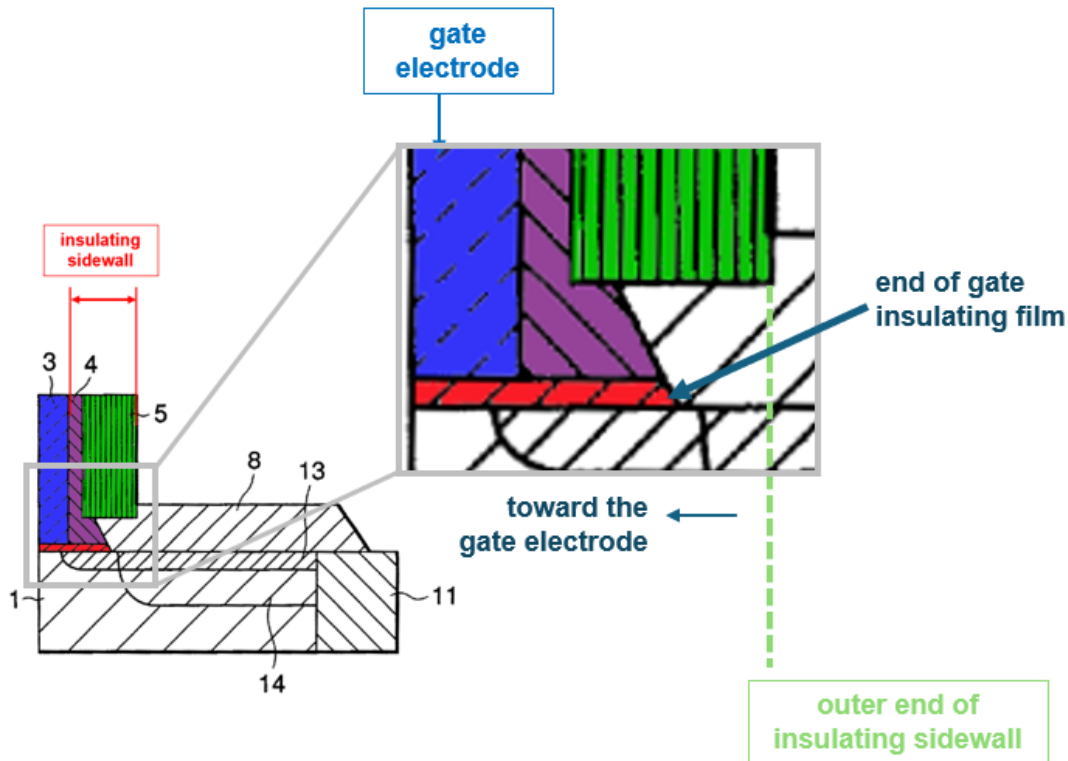
a perpendicular plane to the substrate surface,” such that the side surface “may be located at a predetermined distance from a side end surface of the sidewall 7”).) Kamata’s disclosures are also consistent with Applicant’s prosecution statements directed to this limitation: high-k gate dielectric “does not extend so far such that it is disposed beneath the outer end of the insulating sidewall It is disposed inwardly of the outer end of the insulating sidewall.” (TSMC-1002, 151-52; §IV.D.1.)

b. Ninth Embodiment

As shown in Figure 10(b), high-k gate insulating film 2 is an uninterrupted layer (as evidenced by absence of gaps) extending from under the gate electrode (shaded blue) to under sidewalls 4 (shaded purple) and 5 (shaded green), collectively the “*insulating sidewall*.” (TSMC-1003, ¶107; TSMC-1027, ¶¶50, 56 (formation of gate and sidewall 5); 93 (describing deep diffusion region 14 formation after sidewall film formation), 94.) Kamata’s ninth embodiment discloses limitation 1[D].

In the ninth embodiment, the end of gate insulating film 2 (shaded red) is tapered. As above, the end of film 2 is disposed at a distance inward from the outer end of sidewall 5 toward the gate electrode. (TSMC-1003, ¶108.) For this embodiment, the distance which the end of the gate insulating film extends inward toward the gate electrode is set by Kamata’s manufacturing process discussed

above. (*Id.*) Thus, the end of the high-k film in the ninth embodiment is “*located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode*” [1E], consistent with the ’180 patent’s disclosure and Applicant’s prosecution statements. (TSMC-1001, 20:63-21:1; §IV.D.1; TSMC-1002, 151-52.)



Kamata, Figure 10(b) with enlargement

C. Claims 2-3

Kamata’s first, fourth, and ninth embodiments each discloses “*a buffer insulating film between the substrate and the high dielectric constant gate insulating film*” [2] that “*is a silicon oxide film*” [3]. (TSMC-1003, ¶¶109-10.)

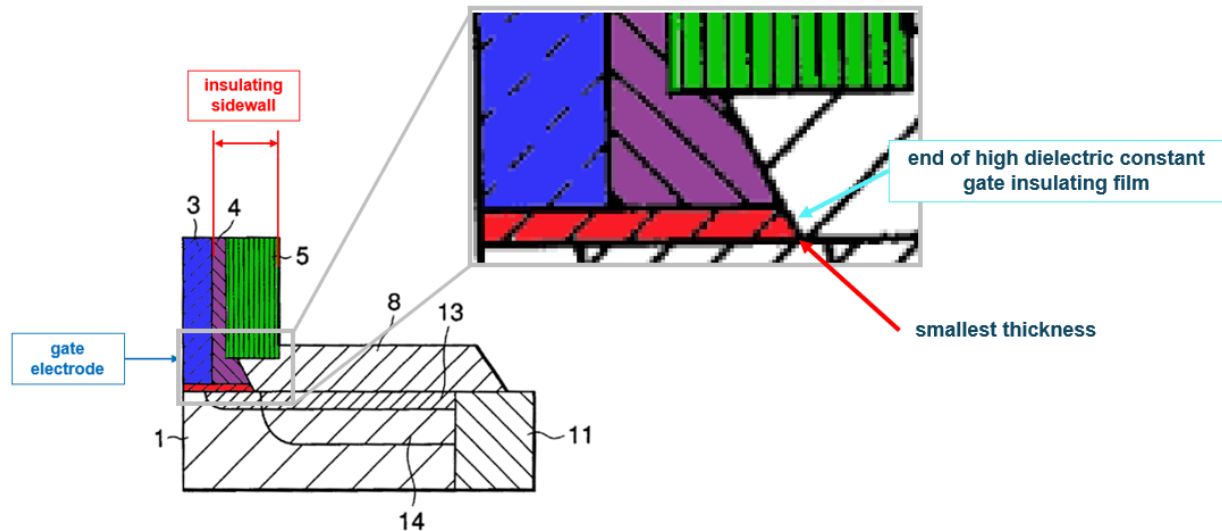
Kamata discloses “[i]t is desired that a **SiO_x ($0 < x \leq 2$) layer** ... is **interposed between the gate insulating film and the silicon substrate.**” (TSMC-1027, ¶¶54, 68 (relating fourth embodiment to first), 94 (relating ninth embodiment to first).) Therefore, in each embodiment, the SiO_x layer is a “*buffer insulating film*” formed of “*a silicon oxide film*” disposed between the substrate and high-k gate insulating film 2. (TSMC-1003, ¶110.)

D. Claims 5, 21-22

Kamata’s ninth embodiment discloses “*a smallest thickness of part of the high dielectric constant gate insulating film located under the insulating sidewall is smaller than that of part of the high dielectric constant gate insulating film located under the gate electrode*” [5], “*end of the high dielectric constant gate insulating film located under the insulating sidewall has a tapered surface*” [21] and “*high dielectric constant gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof*” [22]. (TSMC-1003, ¶¶111-14.)

Gate insulating film 2 extends from under gate electrode 3 to under sidewall films 4 and 5 (collectively the “*insulating sidewall*”). (§V.B.5.) As shown in Figure 10(b) below, the end surface of gate insulating film 2, located under the “*insulating sidewall*,” diminishes in thickness from its maximum (which is equivalent to its thickness under the gate electrode) to its smallest at its far end—it

is “*tapered*.” (TSMC-1027, ¶93; *see also* TSMC-1027, ¶¶18, 85 (describing formation of slanted surfaces in embodiment having same slanted gate dielectric and slanted epitaxially grown film 8); *Unified*, 2022 WL 500391, *17.)



**Kamata, Figure 10(b) with enlargement
(Ninth Embodiment)**

E. Claim 6

Kamata’s first, fourth, and ninth embodiments each discloses “*the high dielectric constant gate insulating film is formed of a Hf based oxide*” [6]. (TSMC-1003, ¶¶115-17.) Kamata discloses a list of exemplary materials for high-k film 2, including HfO₂, which is a “*Hf based oxide*.” (TSMC-1027, ¶¶52-53.) By 2005, a POSITA would have been motivated to select HfO₂ given its known benefits, e.g., “its superior thermal stability with poly-Si and reasonable band alignment.” (TSMC-1037, 2.4.1; TSMC-1032, 207 (HfO₂ “combines a high k (15–26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with

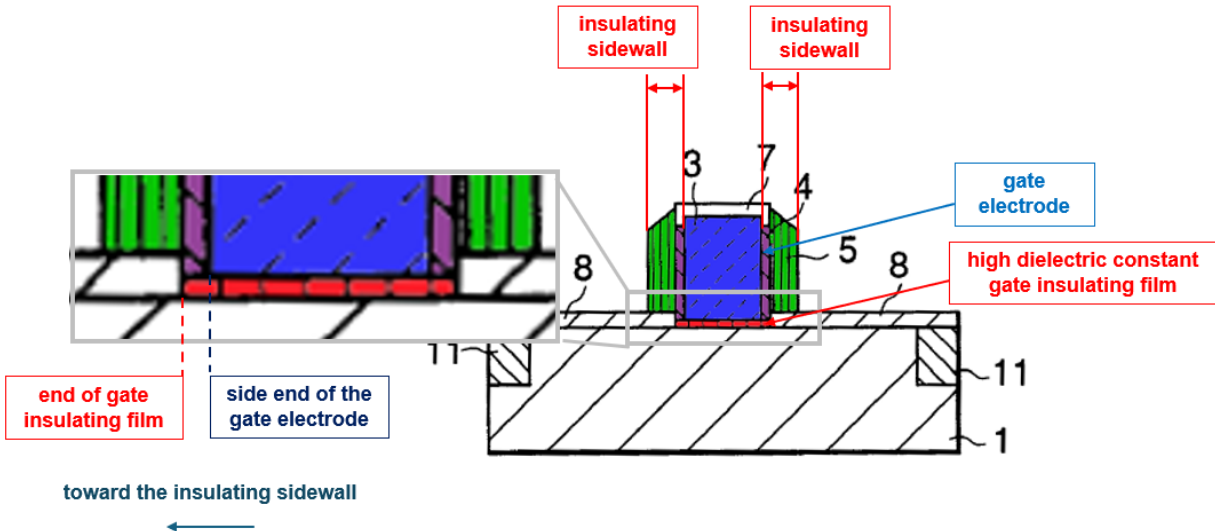
respect to Si”); TSMC-1049, 134 (“Excellent dielectric properties ... suggest that HfO₂ is a promising material for the future gate dielectric application.”); TSMC-1003, ¶117.) HfO₂ also could be scaled down to a smaller EOT. (TSMC-1032, 207; TSMC-1003, ¶117.) Thus, Kamata discloses film 2 “*is formed of a Hf based oxide.*” (TSMC-1003, ¶116.)

F. Claim 13

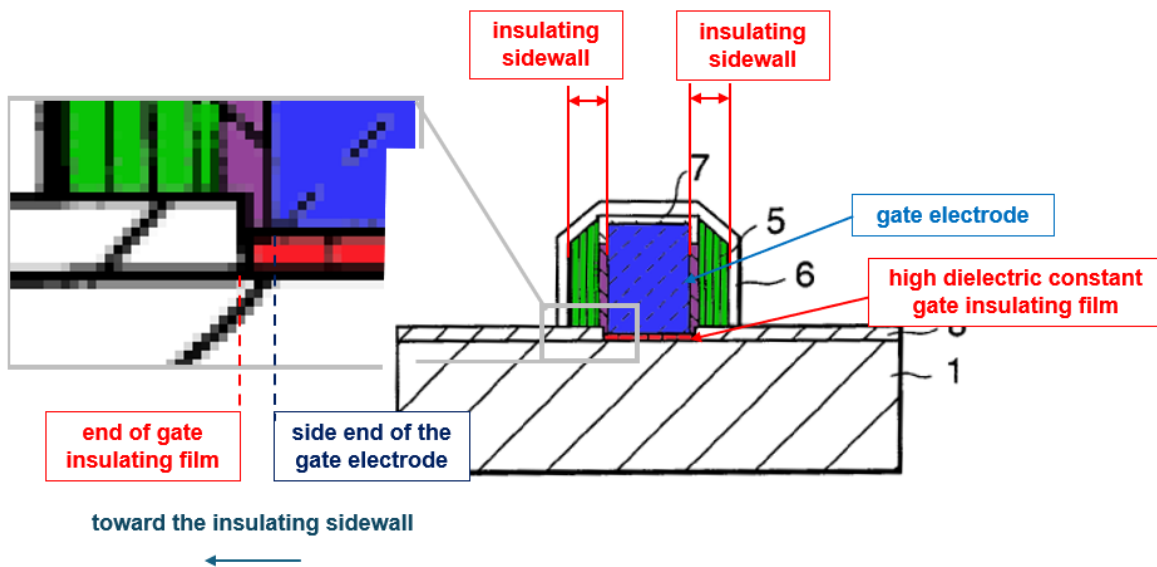
Kamata’s first, fourth, and ninth embodiments each discloses “*the end of the high dielectric constant gate insulating film is located at a predetermined distance from a side end of the gate electrode toward the insulating sidewall*” [13]. (TSMC-1003, ¶¶118-22.)

In each of the first and fourth embodiment devices, the end of gate insulating film 2 is perpendicular to the substrate surface. (§V.B.5.a.) As shown in Figures 1B(j) and 5(c) below, the end of the gate insulating film is not flush with the outer end of sidewall film 5 (outer end of “*insulating sidewall*”); it is disposed at a distance inward from the outer end of sidewall 5 which is also a distance outward from the gate electrode. (§V.B.5.a.) The distance which the end of Kamata’s gate insulating film extends outward from the gate electrode is set by Kamata’s manufacturing process discussed above. (TSMC-1003, ¶¶119, 121.) Thus, the end of gate insulating film 2 in the first and fourth embodiments is “*located at a predetermined distance from a side end of the gate electrode toward the insulating*

sidewall,” consistent with the ’180 patent’s disclosure and Applicant’s prosecution statements. (TSMC-1001, 20:63-21:7; §IV.D.1; TSMC-1003, ¶¶121-22.)

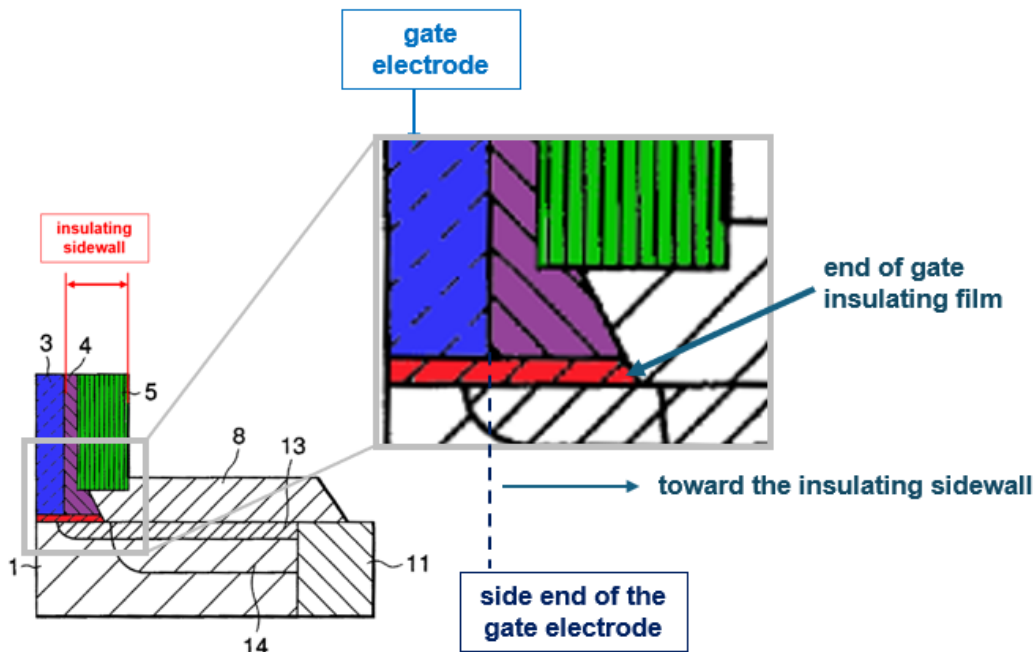


**Kamata, Figure 1B(j) with enlargement
(First Embodiment)**



**Kamata, Figure 5(c) with enlargement
(Fourth Embodiment)**

In the ninth embodiment, the end of gate insulating film 2 is slanted and disposed at a distance inward from the outer end of the sidewall 5 which is also a distance outward from the gate electrode. (§V.B.5.b.) Thus, the end of the high-k gate dielectric in the ninth embodiment is “*located at a predetermined distance from a side end of the gate electrode toward the insulating sidewall*”, consistent with the ’180 patent’s disclosure and Applicant’s prosecution statements. (TSMC-1001, 20:63-21:7, §IV.D.1; TSMC-1003, ¶¶119, 122.)



Kamata, Figure 10(b)

G. Claim 14

Kamata’s first, fourth, and ninth embodiments each discloses “*the insulating sidewall has a double layer structure including an oxide film and a nitride film*” [14]. (TSMC-1003, ¶123.)

The “*insulating sidewall*” of each embodiment includes first sidewall film 4 and second sidewall film 5. (§V.B.4.) Film 4 is an **oxide** film and film 5 is a **nitride** film. (TSMC-1027, ¶¶50, 58.) A POSITA would have understood films 4 and 5 to each be a “layer” of the collective sidewall, consistent with the ’180 patent’s disclosure. (TSMC-1027, ¶¶16 (referring to “multilayer type sidewall films”), 50, 58, 68, 94; TSMC-1001, 20:43-52; TSMC-1003, ¶123.)

H. Claim 15

Claim 15 recites “*the insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film*” [15]. Claim 15 requires no specific order for the recited films. Kamata’s first, fourth, and ninth embodiments each discloses claim 15. (TSMC-1003, ¶¶124-27.)

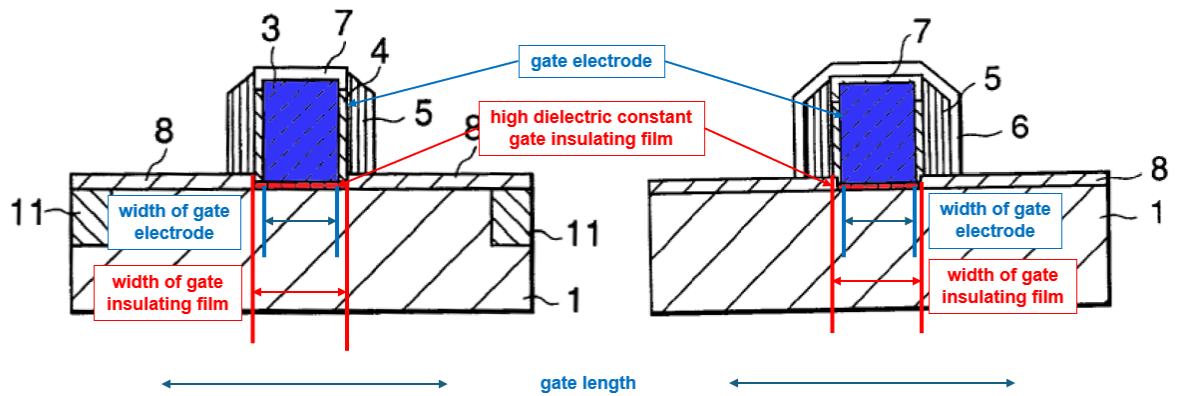
In Kamata’s embodiments, “**a liner layer** that may be a **silicon oxide film** (**SiO₂**) ... may be provided before the deposition of the silicon nitride film 5.” (TSMC-1027, ¶¶51-52; TSMC-1027, ¶¶50, 68, 94.) Accordingly, the “*insulating sidewall*” of Kamata’s first, fourth, and ninth embodiments has “*a triple layer structure*” comprising first silicon oxide sidewall 4 (“*first oxide film*”), silicon oxide liner layer (“*second oxide film*”), and Si₃N₄ second sidewall 5 (“*first nitride film*”). (TSMC-1003, ¶¶126-27; §V.G (POSITA would have considered films 4 and 5 to be “layers”).)

I. Claims 16-17

Kamata's first, fourth, and ninth embodiments each discloses "*a width of the high dielectric constant gate insulating film along a gate length¹⁰ is larger than a width of the gate electrode along the gate length*" [16] and "*a width of a bottom surface of the high dielectric constant gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length*" [17]. (TSMC-1003, ¶¶128-31.)

In the first and fourth embodiments (Figures 1B(j) and 5(c)), the width along the gate length of high-k film 2 (shaded red), including at its bottom surface, is larger than the width along the gate length of gate electrode 3 (shaded blue), including at its bottom surface. (TSMC-1003, ¶129s; *Unified*, 2022 WL 500391, *17.) This is confirmed by Kamata's manufacturing process, in which gate insulating film 2 and sidewall film 4 are etched together, with gate insulating film 2 extending beyond gate electrode 3 to under sidewall film 4. (TSMC-1027, Figures 1A(f), 1B(g), ¶¶50, 56, 68 (fourth embodiment); TSMC-1003, ¶130.)

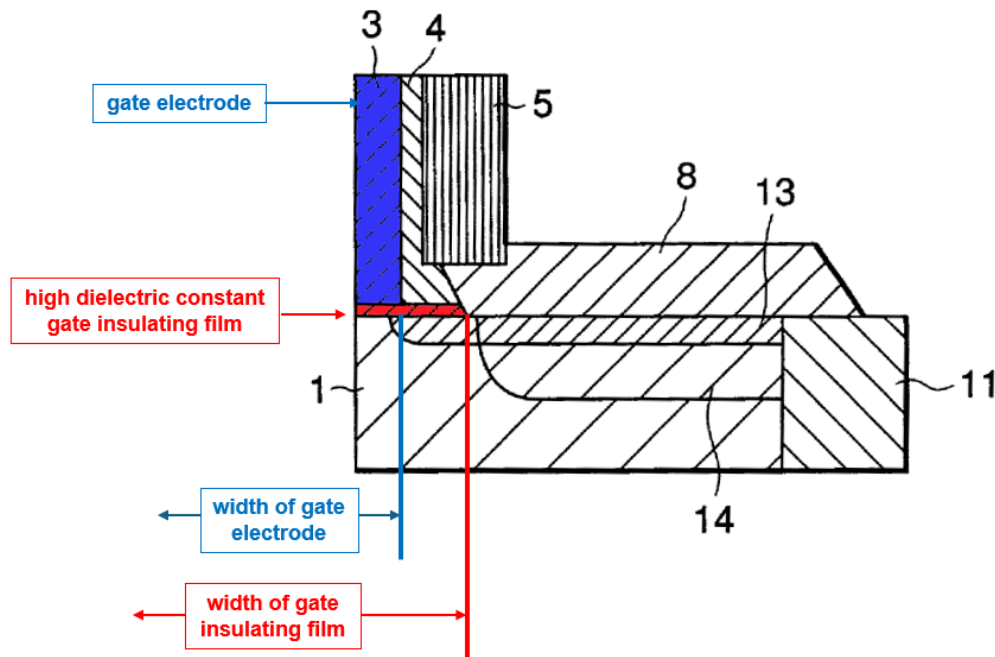
¹⁰ The '180 patent uses the term "gate length" to refer to a direction, specifically from source to drain regions. (TSMC-1003, ¶129 n.6.)



**Kamata, Figures 1B(j)
(First Embodiment)**

**Kamata, Figure 5(c)
(Fourth Embodiment)**

In the ninth embodiment (Figure 10(b)), high-k film 2 (shaded red) extends beyond (protrudes from) under the gate electrode to under sidewall films 4 and 5. (TSMC-1003, ¶131; TSMC-1027, ¶¶50 (formation of gate electrode 3), 93 (describing deep diffusion region 14 after formation of sidewalls), 94, Figure 10(b) (below).) Although Figure 10(b) only shows a right portion of the device, a POSITA would have understood the left portion has similar structure and therefore the width of high-k film 2 (shaded red), including at its bottom surface, is larger than the width of the gate electrode (shaded blue), including at its bottom surface. (TSMC-1003, ¶131.)



**Kamata, Figure 10(b)
(Ninth Embodiment)**

J. Claims 18-19

Kamata's first, fourth, and ninth embodiments each discloses "*the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more*" [18] and "*the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the insulating sidewall*" [19]. (TSMC-1003, ¶¶132-36.)

The "*relative dielectric constant*," also called the dielectric constant, is an inherent material property. (TSMC-1003, ¶133.) The '180 patent acknowledges as AAPA a "high dielectric constant film formed of a Hf based oxide, Al based oxide or the like [] **has a relative dielectric constant of 10 or more**, instead of an

SiO₂ based insulating film having a **relative dielectric constant of about 4.”**

(TSMC-1001, 1:31-33.) The dielectric constant of Si₃N₄ is 7, which a POSITA would have known. (TSMC-1018, Table I; TSMC-1052, Figure 4.)

TABLE I. Comparison of relevant properties for high- κ candidates.

Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si	Crystal structure(s)
SiO ₂	3.9	8.9	3.2	Amorphous
Si ₃ N ₄	7	5.1	2	Amorphous
Al ₂ O ₃	9	8.7	2.8 ^a	Amorphous
Y ₂ O ₃	15	5.6	2.3 ^a	Cubic
La ₂ O ₃	30	4.3	2.3 ^a	Hexagonal, cubic
Ta ₂ O ₅	26	4.5	1–1.5	Orthorhombic
TiO ₂	80	3.5	1.2	Tetrag. ^c (rutile, anatase)
HfO ₂	25	5.7	1.5 ^a	Mono. ^b , tetrag. ^c , cubic
ZrO ₂	25	7.8	1.4 ^a	Mono. ^b , tetrag. ^c , cubic

^aCalculated by Robertson (See Ref. 153).

^bMono.=monoclinic.

^cTetrag.=tetragonal.

Wilk, Table I

Kamata discloses use of, e.g., HfO₂, as a gate insulating film. (TSMC-1027, ¶¶52-53.) HfO₂’s dielectric constant is 25. (TSMC-1018, Table I.) In Kamata, sidewall 4 is a silicon oxide film (e.g., SiO₂, which has a dielectric constant of 3.9) and sidewall 5 is a silicon nitride film (e.g., Si₃N₄, which has a dielectric constant of 7); both have dielectric constants under 10. Accordingly, a POSITA would have known the relative dielectric constant of sidewalls 4 and 5 collectively is also under 10, which is smaller than the dielectric constant of high-k gate insulating film 2 (e.g., HfO₂). (TSMC-1003, ¶¶135-36.)

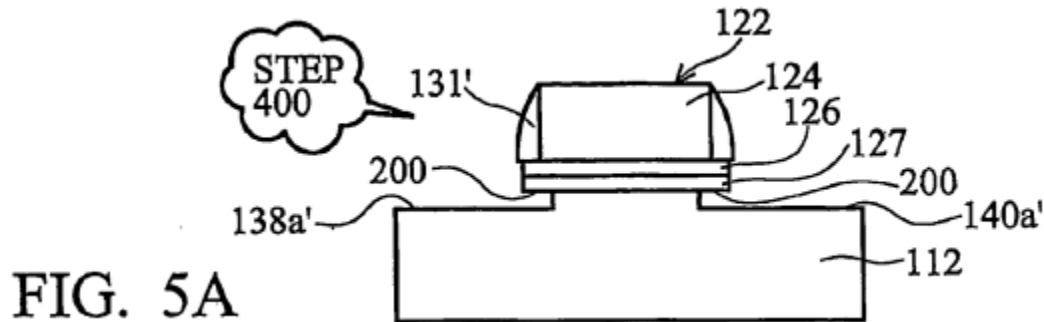
VI. GROUND 2: Kamata-Wang Combination Renders Claims 4 and 12 Obvious.

Claims 4 and 12 track the language of limitations [1D]-[1E] and [13] but refer to the “*buffer insulating film*” instead of the high-k “*gate insulating film*”: “*buffer insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall, and an end of the buffer insulating film is located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode*” [4], and “*end of the buffer insulating film is located at a predetermined distance from a side end of the gate electrode toward the insulating sidewall*” [12]. Kamata does not expressly disclose the footprint of its buffer insulating film. Wang discloses this teaching. The combined devices of Kamata and Wang render claims 4 and 12 obvious. (TSMC-1003, ¶¶137-45.)

A. Combination Overview

Wang’s MOSFET device includes buffer interface 127 between the substrate and high-k gate dielectric 126. (TSMC-1045, ¶55, Figure 5A (below).) In Wang, the buffer interface and high-k gate dielectric have the same footprint. (TSMC-1045, Figure 5A, ¶55 (“In step 400 (FIG. 5A), **the high-k gate dielectric 126, including the buffer interface 127, ... and the gate electrode 124** have been formed by deposition and patterning so that the **footprint** of the former [gate dielectric and buffer interface] is larger than that of the latter [gate electrode].”); *Unified*, 2022 WL 500391, *17). Wang and Kamata are in the same field as the

'180 patent, "a semiconductor device and a method for fabricating the semiconductor device." (TSMC-1001, 1:17-18; TSMC-1027, ¶3; TSMC-1045, Abstract; TSMC-1003, ¶140.)



Wang, Figure 5A

A POSITA would have been motivated to combine Wang's teachings regarding use of a buffer interface having a footprint that is the same as the footprint of the high-k film in Kamata's first, fourth, and ninth embodiment devices. (TSMC-1003, ¶¶142-45.) For example, a POSITA would have been motivated to align the outer edges of Kamata's buffer insulating film with the outer edges of Kamata's gate insulating film 2, as taught by Wang. (*Id.*)

Wang motivates the combination, disclosing gate dielectric 126 and buffer interface 127 are patterned together in the same step, thereby decreasing fabrication complexity and saving costs. (TSMC-1045, Figures 4B-4C (below), ¶48; TSMC-1003, ¶143.)



Wang, Figures 4B (top), 4C (bottom)

would have understood aligning the buffer interface and gate dielectric footprints

footprint) to improve similar devices in the same way for the above reasons. *KSR*

POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable because Wang uses conventional techniques and etch processes to create a buffer interface coextensive with high-k gate insulating films. (TSMC-1045, ¶55; TSMC-1003, ¶145.)

B. Claims 4 and 12

Because the footprint of the “*buffering insulating film*” and high-k “*gate insulating film*” are the same, the Kamata-Wang combination discloses claims 4 and 12 for the same reasons discussed in §§V.B.5, V.F. (TSMC-1003, ¶142.)

VII. GROUND 3: Kamata-Koyama Combination Renders Claim 7 Obvious.

Kamata’s high-k gate insulating film 2 is, e.g., Hf silicate. (TSMC-1027, ¶¶52-53.) Kamata does not explicitly disclose “*the high dielectric constant gate insulating film is formed of a HfSiON film*” [7]. Koyama discloses this. Koyama and Kamata are in the same field as the ’180 patent, “a semiconductor device and a method for fabricating the semiconductor device.” (TSMC-1001, 1:17-18; TSMC-1027, ¶3; TSMC-1029, Title; TSMC-1003, ¶150.) The Kamata-Koyama combination renders claim 7 obvious. (TSMC-1003, ¶¶146-50.)

According to Koyama, “Hf(Zr) silicates are considered to be prospective high-K materials due to their modest dielectric constants and good interface properties.” (TSMC-1029, 849.) Because a “HfSiON gate dielectric with excellent thermal stability has been proposed,” Koyama studied “the effects of nitrogen on

the improved thermal stability and electrical characteristics of this dielectric.” (*Id.*) Koyama concluded that “nitrogen [in HfSiON] enhances the dielectric constant of silicates” and “boron penetration is substantially suppressed in the HfSiON during high temperature annealing.” (*Id.*) Koyama’s experimental results “strongly suggest that HfSiON is the most probable material for first generation high-K gate dielectrics.” (TSMC-1029, 850.)

A POSITA would have therefore been motivated to combine Koyama’s teachings regarding use of HfSiON as a high-k gate dielectric with each of Kamata’s first, fourth, and ninth embodiments, thereby providing devices where gate insulating film 2 “*is formed of a HfSiON film.*” (TSMC-1003, ¶148.)

Kamata presents Hf silicate as an option for its high-k gate dielectric. (TSMC-1027, ¶52.) This suggestion would have motivated a POSITA to investigate Hf silicate options and would have led the POSITA to Koyama. (TSMC-1003, ¶149.) Koyama discloses that, among Hf silicates, HfSiON was the most probable high-k material in view of the benefits resulting from its incorporation of nitrogen. (TSMC-1029, 849.) Thus, a POSITA would have been motivated to use HfSiON for the benefits taught by Koyama to improve device operation, including improved thermal stability and electrical characteristics and enhanced dielectric constant. (TSMC-1029, 849; TSMC-1003, ¶149.)

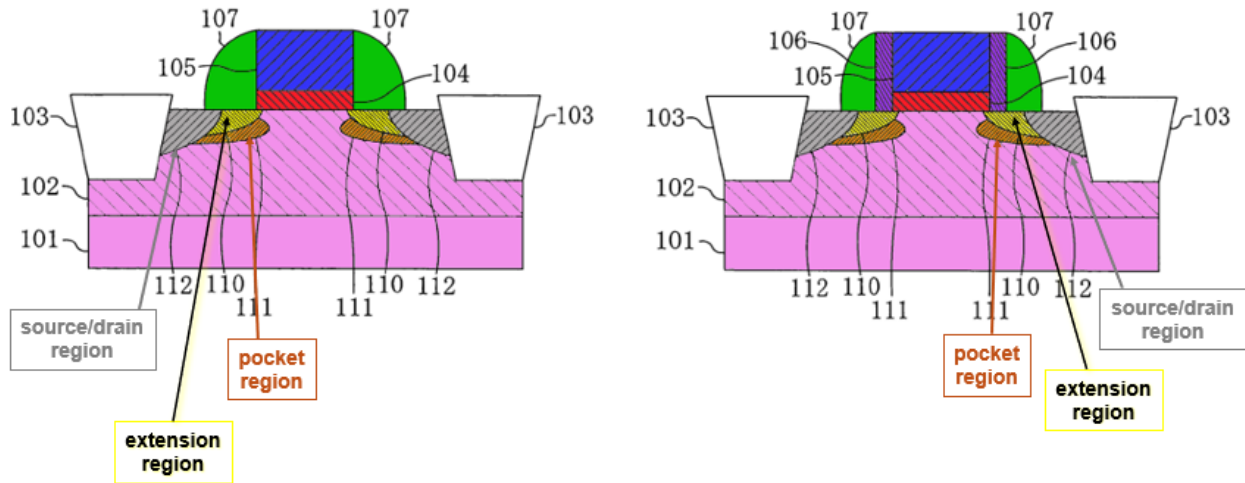
Moreover, the combination is nothing more than the use of a known technique (Koyama's use of HfSiON as a gate insulating film) to improve similar devices in the same way for the above reasons. *KSR*, 550 U.S. at 416-417; TSMC-1003, ¶150. Because techniques for the formation of a gate dielectric were well-established and formation of high-k dielectric films such as HfSiON uses these processes, a POSITA would have had a reasonable expectation of success and the combination would have yielded predictable results. (TSMC-1003, ¶150; TSMC-1032, 561-62.)

VIII. GROUND 4: Kamata-Rodder Combination Renders Claims 8-9 Obvious.

Claims 8-9 recite features common in semiconductor devices prior to the '180 patent: “*extension region[s]*”, “*pocket region[s]*”, and “*source/drain regions.*” The '180 patent admits this fact, presenting the claimed subject matter almost verbatim when describing two prior art devices:

A pocket region 111 is formed in part of the well 102 located under the extension region 110. Source/drain regions 112 are formed so that each of the source/drain regions 112 is provided in parts of the well 102 located at the external side to the extension region 110 and the pocket region 111 when viewed from the gate electrode 105.

(TSMC-1001, 1:47-53 (Background), Figures 16A-B.) Kamata alone, in view of AAPA, renders claims 8-9 obvious. Rodder also discloses these features, and the Kamata-Rodder combination renders claims 8-9 obvious.



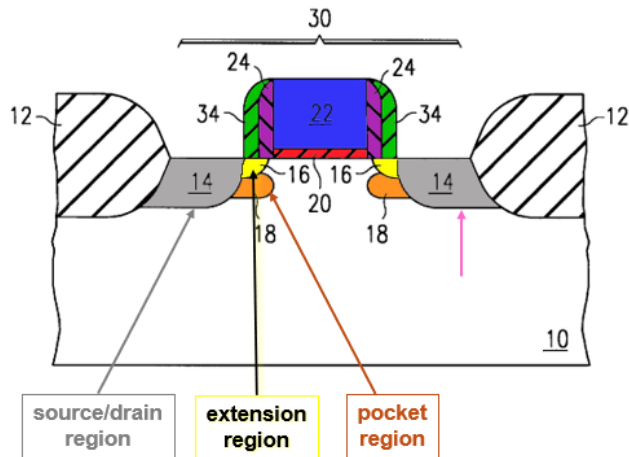
'180 Patent, Figure 16A (AAPA)

'180 Patent, Figure 16B (AAPA)

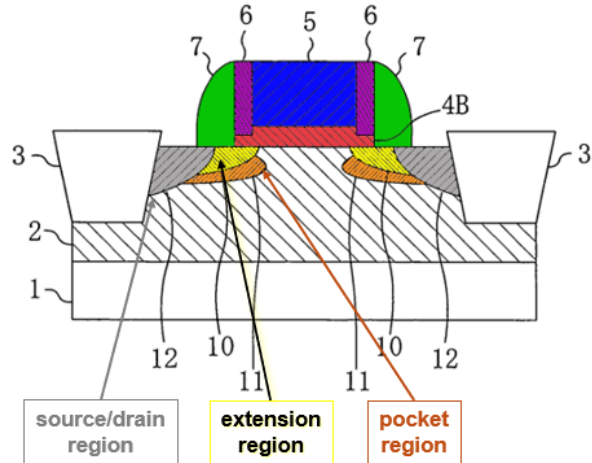
A. Rodder

Rodder describes a transistor substrate having highly doped regions (n-type) 16 (shaded yellow) “commonly referred to as drain extensions” and pocket regions 18 (shaded orange) “doped oppositely to drain extension regions 16.” (TSMC-1023, 2:61-3:1, Figure 1 (below-left).) Rodder’s substrate also includes “deep source/drain regions 14 [shaded gray].” (TSMC-1023, 2:62-63.) As shown below, Rodder’s Figure 1 has the same structure, including placement of the extension regions, pocket regions, and source/drain regions, as ’180 patent-Figure 2. (TSMC-1003, ¶155.) Kamata and Rodder are in the same field as the ’180 patent, “a semiconductor device and a method for fabricating the semiconductor device.”

(TSMC-1001, 1:17-18; TSMC-1027, ¶3; TSMC-1023, Abstract; TSMC-1003, ¶154.)



Rodder, Figure 1

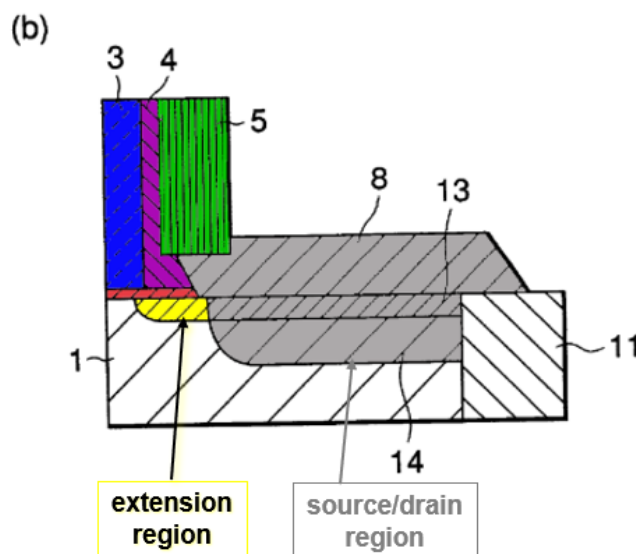


'180 Patent, Figure 2

B. Combination Overview

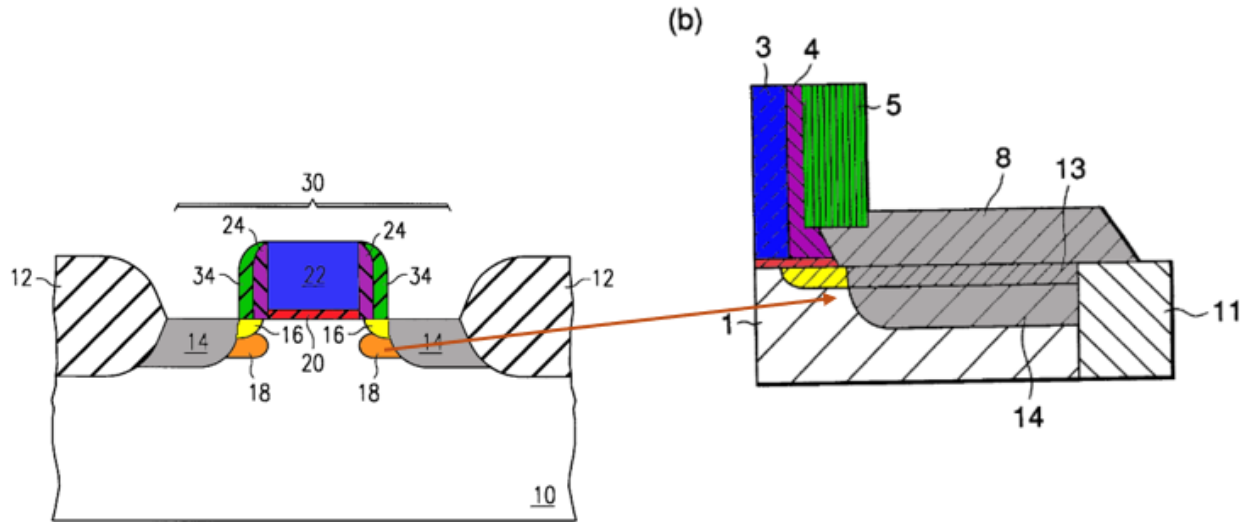
Kamata's ninth embodiment device includes extension region 13 (shaded yellow in Figure 10(b) below) "formed by implanting impurities into the silicon." (TSMC-1027, ¶93, Figure 10(a).) In Kamata's device, "deep diffusion region 14 [shaded gray] is formed by forming an elevated source/drain region 8 [shaded gray] on the side wall film 5 [shaded green]." (TSMC-1027, ¶93, Figure 10(b) (below).) Although Kamata does not specify the conductivity type of the extensions and source/drain regions, a POSITA would have known them to have the same conductivity type (e.g., n-type for NMIS, p-type for PMIS). (TSMC-1003, ¶157; TSMC-1034, 9-10, Figure 1-6.) Kamata therefore discloses "*an extension region of a first conductivity type is formed in part of the active region*

located under the insulating sidewall” [8A] and “*each of source/drain regions of a first conductivity type is formed in part of the active region ...*” [9]. (TSMC-1003, ¶157.) Kamata, however, does not disclose “*pocket regions.*”



Kamata, Figure 10(b)

A POSITA would have been motivated to combine Rodder's teachings regarding use of a pocket region below the extension region and external to the source/drain regions in the semiconductor device of Kamata's ninth embodiment, as shown below. (TSMC-1003, ¶158.)



Rodder, Figure 1

Kamata, Figure 10(b)

A POSITA would have been motivated to make the above combination to obtain the well-understood benefits of “*pocket regions*” and their locations described by Rodder, including “reduc[ing] the threshold voltage (V_t) rolloff, reduc[ing] the nominal V_t , and thus improv[ing] the nominal drive current.” (TSMC-1023, 1:22-25; TSMC-1003, ¶160; TSMC-1038, 463-64 (describing pocket implants which “reduce short-channel effects by shielding the channel from the deep source/drain diffusion”).) A POSITA would have understood obtaining these benefits was important to meet the goals of scaling devices stressed by both Kamata and Rodder. (TSMC-1027, ¶5; TSMC-1023, 1:18-22; TSMC-1003, ¶160.)

The combination is also nothing more than use of a known technique (Rodder’s formation of pocket regions below extension regions and outside of source/drain regions) to improve similar devices in the same way for the above

reasons. *KSR*, 550 U.S. at 416-417; TSMC-1003, ¶161. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable because both Kamata and Rodder use known ion implantation processes for forming doped regions, including pocket regions. (TSMC-1027, ¶93; TSMC-1023, 4:21-62; TSMC-1038, 463-64 (describing techniques for forming pocket implants); TSMC-1003, ¶161.)

C. Claims 8-9

The device of the Kamata-Rodder combination includes pocket implants having “opposite conductivity to” the conductivity of the extensions (TSMC-1023, 4:35-36), placed under the extensions such that the source/drain regions are external to the pocket region as taught by Rodder, thus providing “a *pocket region of a second conductivity type is formed in part of the active region located under the extension region*” [8B] and “*each of source/drain regions ... located in an external side to the extension region and the pocket region when viewed from the gate electrode*” [9]. (TSMC-1003, ¶159.)

Accordingly, the Kamata-Rodder combination renders claims 8-9 obvious.

IX. GROUND 5: Kamata-Sim Combination Renders Claim 11 Obvious.

Kamata discloses use of HfO₂ as a high-k gate insulating film (TSMC-1027, ¶53; §V.E) but does not expressly disclose the high-k gate dielectric “*has a thickness of 2 nm or less*” [11]. Sim, which “systematically evaluated the effects of

high-k film thickness on charge trapping and channel carrier mobility,” discloses a high-k gate insulating film with a thickness of 2 nm or less. (TSMC-1024, 218-19, 221.) Sim and Kamata are in the same field as the ’180 patent. (TSMC-1001, 1:17-18; TSMC-1027, ¶3; TSMC-1024, Abstract; TSMC-1003, ¶162.) The devices of the combination of Kamata (first/fourth/ninth embodiments) and Sim disclose “*a part of the high dielectric constant gate insulating film located under the insulating sidewall has a thickness of 2 nm or less*” [11]. (TSMC-1003, ¶¶162-64.)

A POSITA would have been motivated to adopt Sim’s solution of forming a gate insulating film with a thickness of 20Å (2 nm) or less in Kamata’s first/fourth/ninth embodiments. Sim expressly motivates the combination, finding that reducing the thickness of HfO₂ to below 20Å (2 nm) enhances mobility and reduces charge trapping, key issues in ensuring the performance and scalability of semiconductor devices. (TSMC-1024, 221 (“Scaling the physical thickness of the HfO₂ dielectric to below 20Å [2 nm] causes less charge trapping and higher mobility.”), 219 (“Even within 100µs, a 33Å HfO₂ sample shows significant current reduction while a 18Å HfO₂ sample is free from transient charging within the detection limits.”).) A POSITA would further have understood this improvement aligns with the continued miniaturization of devices, which both Kamata and Sim emphasize is crucial to advancing CMOS technology. (TSMC-1027, ¶5; TSMC-1024, 218; TSMC-1003, ¶165.)

Additionally, the combination is nothing more than the use of a known technique (Sim's HfO₂ dielectric layer with less than 20Å thickness) to improve similar devices in the same way for the above reasons. *KSR*, 550 U.S. at 416-417; TSMC-1003, ¶166. A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable because Sim uses a well-known process, atomic layer deposition (ALD), for fabricating high-k films. (TSMC-1024, 218; TSMC-1032, 17-19; TSMC-1003, ¶166.)

X. GROUND 6: Kamata-Wilk Combination Renders Claims 18-19 Obvious.

Should PO argue Kamata fails to disclose claims 18-19 despite expressly disclosing using HfO₂ as a gate insulating film (§V.J; TSMC-1027, ¶53), Wilk expressly discloses these limitations.

As of 2001, Wilk disclosed the following table of relevant properties, including dielectric constants, for various high-k materials:

TABLE I. Comparison of relevant properties for high- κ candidates.

Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si	Crystal structure(s)
SiO ₂	3.9	8.9	3.2	Amorphous
Si ₃ N ₄	7	5.1	2	Amorphous
Al ₂ O ₃	9	8.7	2.8 ^a	Amorphous
Y ₂ O ₃	15	5.6	2.3 ^a	Cubic
La ₂ O ₃	30	4.3	2.3 ^a	Hexagonal, cubic
Ta ₂ O ₅	26	4.5	1–1.5	Orthorhombic
TiO ₂	80	3.5	1.2	Tetrag. ^c (rutile, anatase)
HfO ₂	25	5.7	1.5 ^a	Mono. ^b , tetrag. ^c , cubic
ZrO ₂	25	7.8	1.4 ^a	Mono. ^b , tetrag. ^c , cubic

^aCalculated by Robertson (See Ref. 153).

^bMono.=monoclinic.

^cTetrag.=tetragonal.

Wilk, Table I

A POSITA would have been motivated to look to Wilk's teachings to understand the properties of materials discussed in Kamata, for example, to ensure the gate insulating film had a sufficiently high dielectric constant. (TSMC-1003, ¶169.) Wilk and Kamata are in the same field as the '180 patent. (TSMC-1001, 1:17-18; TSMC-1027, ¶3; TSMC-1018, Abstract; TSMC-1003, ¶168.)

In Kamata, gate insulating film 2 is, e.g., a Hf based oxide such as HfO₂, sidewall 4 is a silicon oxide film, and sidewall 5 is a silicon nitride film. (TSMC-1027, ¶¶52-53 (gate insulating film materials), ¶¶50, 58, 68 (sidewall materials).) Wilk discloses the dielectric constant for HfO₂ is 25, which is greater than 10. (TSMC-1018, Table I.) Wilk further discloses the dielectric constant for silicon oxide (SiO₂) is 3.9 and for silicon nitride (Si₃N₄) is 7; both under 10. (*Id.*)

Accordingly, a POSITA would have known the relative dielectric constant of sidewalls 4 and 5 collectively is also under 10, which is smaller than the dielectric constant of high-k gate insulating film 2 (e.g., HfO₂). (TSMC-1003, ¶171.)

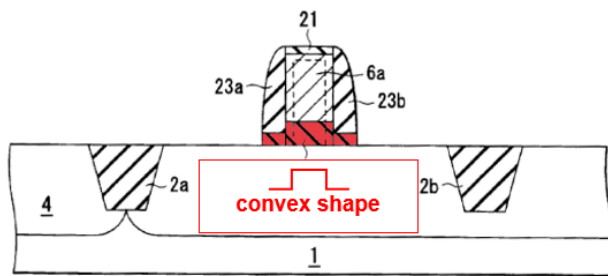
Thus, the Kamata-Wilk combination discloses “*the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more*” [18] and “*the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the insulating sidewall*” [19]. (TSMC-1003, ¶172.)

XI. GROUND 7: Kamata-Takayanagi Combination Renders Claim 20 Obvious.

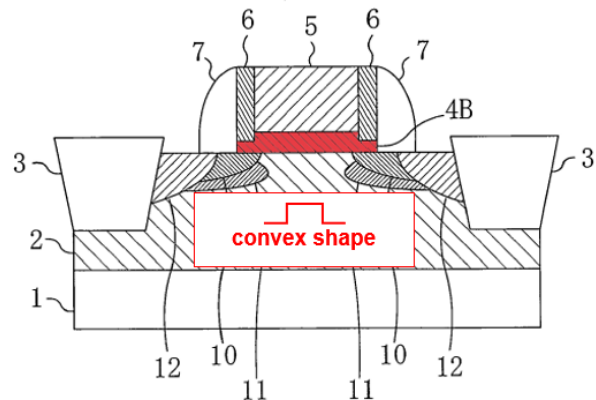
Kamata’s first, fourth, and ninth embodiments do not expressly disclose the high-k film has “*a convex cross-sectional shape*” [20]. Takayanagi discloses this feature, consistent with the ’180 patent’s disclosure. (TSMC-1003, ¶¶173-83.) Takayanagi and Kamata are in the same field as the ’180 patent, “a semiconductor device and a method for fabricating the semiconductor device.” (TSMC-1001, 1:17-18; TSMC-1027, ¶3; TSMC-1030, Abstract; TSMC-1003, ¶175.)

Takayanagi’s second embodiment device includes gate electrode 6a and Hf silicate gate insulating film 5a formed on substrate 1. (TSMC-1030, 6:12-17.) Through Takayanagi’s fabrication process, gate insulating film 5a has a reduced thickness outside the gate electrode, approximately half of its initial thickness, compared to the thickness under the gate electrode. (TSMC-1030, 6:24-26, 6:57-

62, Figures 5, 10 (below).) As shown below, Takayanagi's gate insulating film has a convex shape, similar to '180 patent-Figure 3. (TSMC-1001, 8:56-61; TSMC-1003, ¶177.) In Takayanagi's device, gate insulating film 5 has "a high dielectric constant in the center wide part and a low dielectric constant in the edges." (TSMC-1030, 6:54-56.)



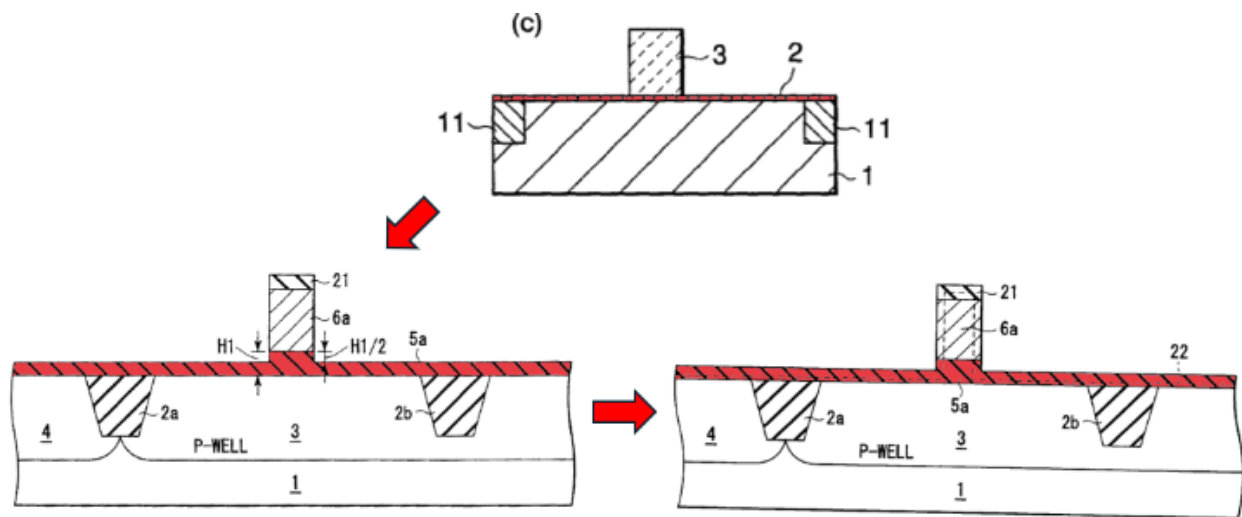
Takayanagi, Figure 10



'180 Patent, Figure 3

A POSITA would have been motivated to integrate Takayanagi's techniques for forming a gate insulating film into Kamata's first, fourth, and ninth embodiments (TSMC-1003, ¶179). Kamata discloses use of a Hf silicate as a gate dielectric, like Takayanagi. (TSMC-1027, ¶52; TSMC-1030, 6:12-13.) Accordingly, this integration involves a straightforward modification to Kamata's process of forming the gate stack in Kamata's Figure 1A(c). (TSMC-1003, ¶180.) For example, a POSITA would have understood in the combined process the insulating film outside the gate electrode would be etched to about half its initial thickness, as taught by Takayanagi. (TSMC-1030, 6:24-26, Figure 5 (bottom-left),

6:34-39, Figure 6 (bottom-right); TSMC-1003, ¶180). Once completed, the devices of the combinations of Kamata (first/fourth/ninth embodiments) and Takayanagi have a gate insulating film with a smaller thickness under the “*insulating sidewall*” than under the gate electrode—“*a convex cross-sectional shape*” [20], as taught by the ’180 patent. (TSMC-1003, ¶181.)



**Kamata, Figure 1A(c) (top);
Takayanagi, Figures 5 (bottom-left), 6 (bottom-right)**

Takayanagi motivates the combination, identifying “[t]he gate insulating film may have [] low reliability due to, for example, a small breakdown voltage, which results from the electric field concentration at the gate edge.” (TSMC-1030, 1:67-2:3.) Takayanagi explains a thicker gate insulating film under the gate electrode redistributes the electric field to the center of the gate insulating film and minimizes field concentration at the gate electrode edges. (TSMC-1030, 7:9-17.) JP-Ono corroborates this motivation, demonstrating the benefits of reducing the

thickness of an extended high-k gate dielectric outside of the gate electrode.

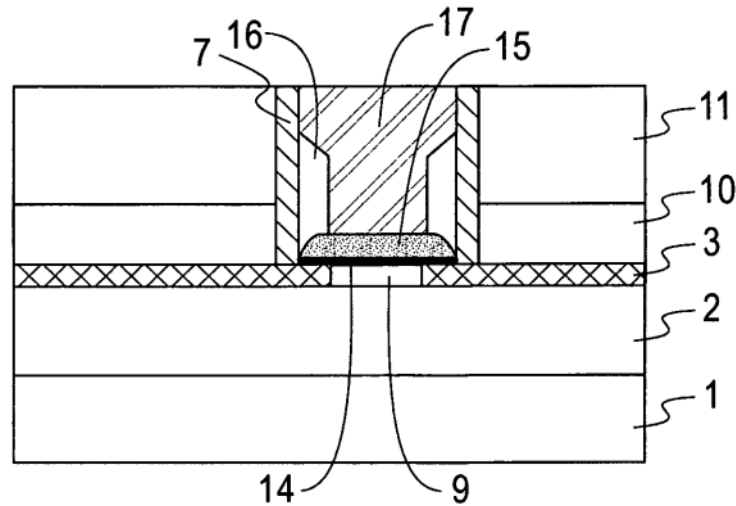
(TSMC-1040, ¶¶85-87) A POSITA would have been motivated to apply Takayanagi's teachings to enhance the reliability of Kamata's devices. (TSMC-1003, ¶182.)

The combination is nothing more than the use of a known technique (Takayanagi's use of a convex-shaped Hf silicate gate insulating film) to improve similar devices (Kamata's devices using an Hf silicate gate insulating film) in the same way. *KSR*, 550 U.S. at 416-417; TSMC-1003, ¶183. A POSITA would have had a reasonable expectation of success in combining Takayanagi's methods with Kamata's devices, and the results of the combination would have been predictable, because Takayanagi uses well-established deposition processes (e.g., MOCVD or ALD) and etching processes (RIE). (TSMC-1030, 4:49-51, 5:8-11, 6:23-29; TSMC-1003, ¶183.)

XII. GROUND 8: Guha Renders Claims 1-6, 12-14, 16-18, 21-22 Obvious.

A. Overview

Guha's Figure 12 device includes gate 17 with gate spacer 16 and isolating spacer 7. (TSMC-1028, ¶¶43-45.) Dielectric layer 15, formed on gate-isolating layer 14, extends from under gate 17 to under gate spacer 16. (TSMC-1028, ¶¶38, 43-44.)



Guha, Figure 12

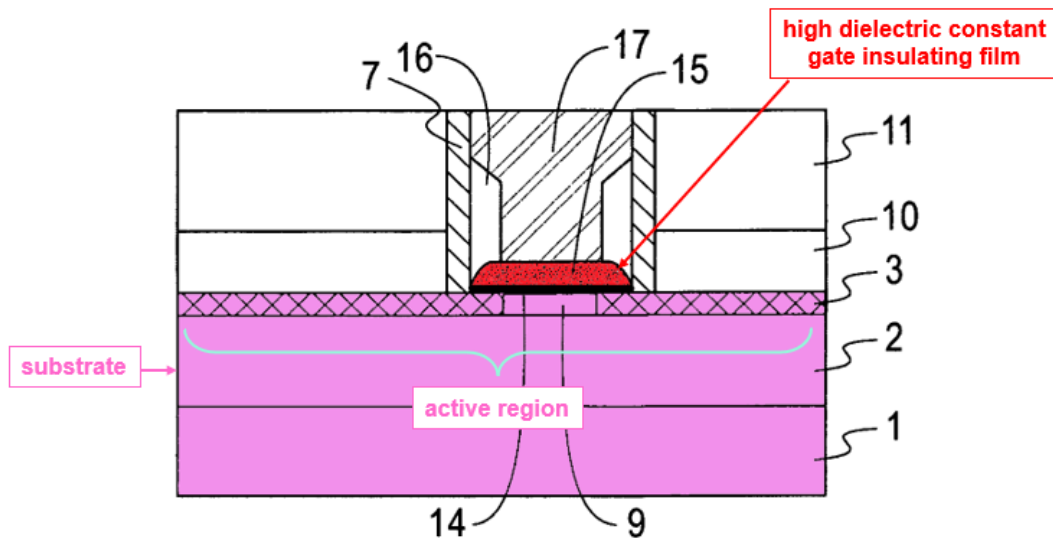
B. Independent Claim 1

1. Preamble [1P]

Guha's Figure 12 device includes substrate 1 and channel layer 3 each "compris[ing] any **semiconducting material**." (TSMC-1028, ¶¶22-23, ¶¶43-45 (relating Figure 9's first embodiment device to Figure 12 device); *Google*, 2022 WL 4287797, *9 n.9). Guha's Figure 12 device is a "*semiconductor device*" [1P]. (TSMC-1003, ¶189.)

2. Limitation [1A]

Guha's Figure 12 device, below, includes substrate 1, which "may be of the **n or p-type** depending on the desired device to be fabricated." (TSMC-1028, ¶¶22, 43.) Channel layer 3 is further provided over buried oxide layer 2 which "can be omitted." (TSMC-1028, ¶22.) Substrate 1, channel layer 3, and buried oxide layer 2 (if present) are collectively "*a substrate*" (shaded pink). (TSMC-1003, ¶190.)



Guha, Figure 12

Guha's substrate contains "active device regions." (TSMC-1028, ¶¶22, 43.)

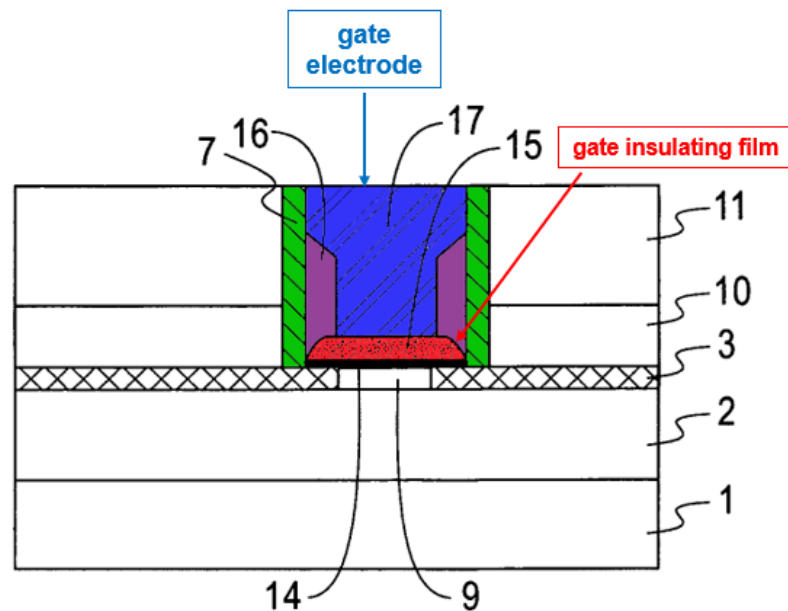
Source/drain extensions "are formed by implanting dopants ... into the channel layer 3," further indicating presence of an active region in Guha's Figure 12 device. (TSMC-1028, ¶¶26, 43.) A POSITA would have understood Guha's device has "*an active region in a substrate.*" (TSMC-1028, ¶22; TSMC-1003, ¶190.)

Guha's Figure 12 device includes gate-isolating layer 14 (shaded black) formed on a portion of channel layer 3 which is part of the "*active region in a substrate.*" (TSMC-1028, ¶¶37, 43.) Dielectric layer 15 (shaded red), "comprising a high-k dielectric material," is "formed only on the gate-isolating layer 14." (TSMC-1028, ¶¶38, 43.) Dielectric layer 15 is "*a high dielectric constant gate*

*insulating film formed on*¹¹ *an active region in a substrate.*” (TSMC-1003, ¶193; TSMC-1028, ¶37 (gate-isolating layer 14 “acts as a buffering layer between channel 9 and the” high-k dielectric).)

3. Limitation [1B]

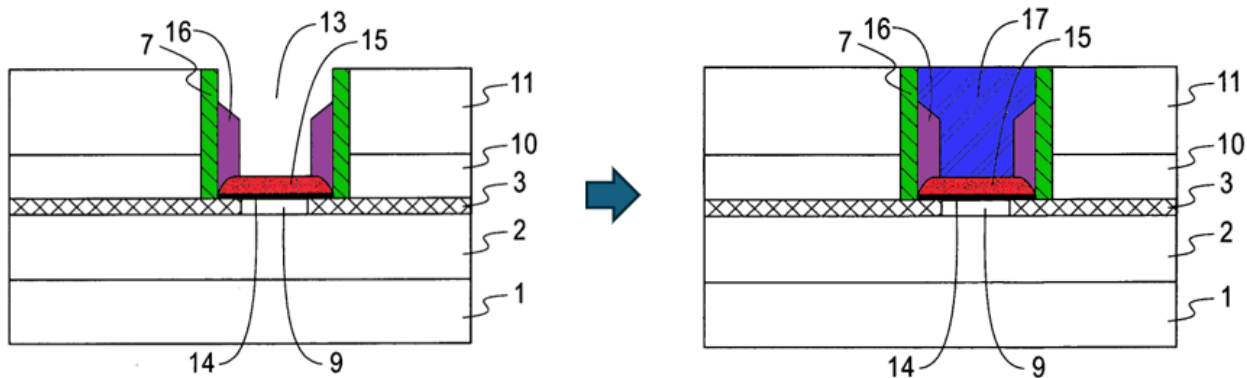
In Guha’s Figure 12, gate 17 (shaded blue) is formed on high-k dielectric layer 15 (shaded red). Gate 17 is formed of a “conductive material” and therefore is “a gate electrode formed on the high dielectric constant gate insulating film.” (TSMC-1028, ¶¶41, 45; TSMC-1003, ¶194; *Unified*, 2022 WL 500391, *17.)



Guha, Figure 12

¹¹ The '180 patent uses the term “formed on” to indicate relative position and does not require direct contact. (*E.g.*, TSMC-1001, 7:35-37.)

Guha's fabrication process confirms the Figure 12 structure. For example, Guha describes cavity 13 (Figure 11 (left)) is "filled with a conductive material to form the **gate 17**" by "depositing the material ... **onto the dielectric layer 15**", resulting in formation of the gate electrode over dielectric layer 15. (TSMC-1028, ¶¶41, 44 (associating gate formation in Figure 12 (right) with first embodiment process), 45; TSMC-1003, ¶196.)

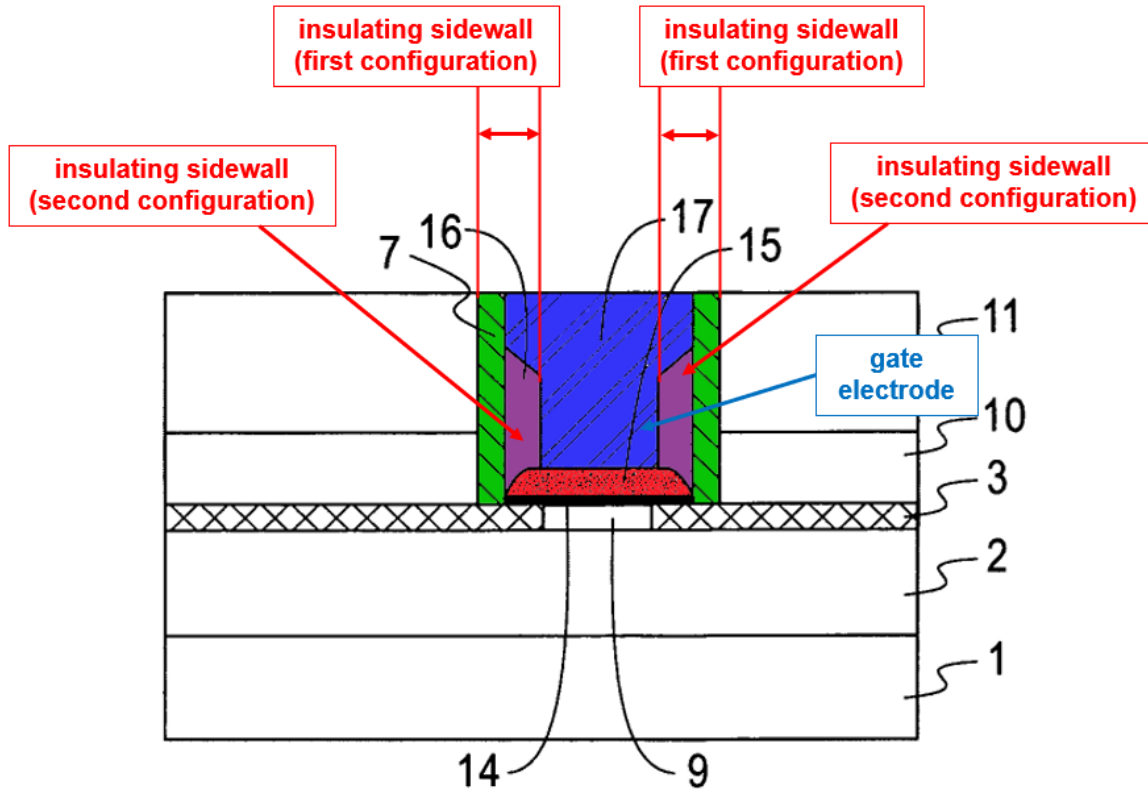


Guha, Figure 11 (left), Figure 12 (right)

4. Limitation [1C]

Guha's Figure 12 device includes gate spacers 16 (shaded purple) and isolating spacers 7 (shaded green) on gate electrode 17's (shaded blue) side surfaces. (TSMC-1028, ¶¶28 (formation of spacers 7), 44 (formation of spacers 16), 43 (associating Figure 12 to process steps associated with Figures 1-7).) Although Guha refers to each of these structures as a "spacer," as noted above, "spacer" and "sidewall" are often used interchangeably. (TSMC-1003, ¶200; §IV.B.3.) Further, a POSITA would have understood them to be "sidewalls."

(TSMC-1028, ¶¶40 (describing “gate spacer structure 16 on the sidewalls of the cavity”), 44; TSMC-1003, ¶200.)



Guha, Figure 12

Gate spacers 16 are made of “e.g. an oxide or other suitable material.” (TSMC-1028, ¶¶40, 43.) Through use of gate spacers 16, “the interface between the bottom of the gate 17 and the dielectric layer 15 is better defined and offers a better control over the channel 9.” (TSMC-1028, ¶45.) To provide such benefits, a POSITA would have understood gate spacers 16 to be formed of an insulating oxide material. (TSMC-1003, ¶¶201; TSMC-1034, 9, 75; TSMC-1033, 79-80.) Isolating spacers 7 are “composed of any insulating material including, for

example, an oxide, nitride, oxynitride or any combination thereof” with the “preferred material [being] silicon nitride.” (TSMC-1028, ¶¶28, 43.)

Gate spacers 16 and isolating spacers 7 are collectively “*a insulating sidewall formed on each side surface of the gate electrode*” [1C], consistent with the ’180 patent’s disclosure. (TSMC-1003, ¶203; TSMC-1001, 2:58-63 (“insulating sidewall” includes two sidewalls).) Petitioner refers to this as the first “*insulating sidewall*” configuration.

Alternatively, gate spacers 16 alone disclose an “*insulating sidewall formed on each side surface of the gate electrode*” [1C], consistent with the ’180 patent’s disclosure. (TSMC-1003, ¶204; TSMC-1001, 6:3-4 (“insulating sidewall” has a single component).) Petitioner refers to this as the second “*insulating sidewall*” configuration.

The first and second “*insulating sidewall*” configurations disclose limitation [1C]. (TSMC-1003, ¶¶203-05.)

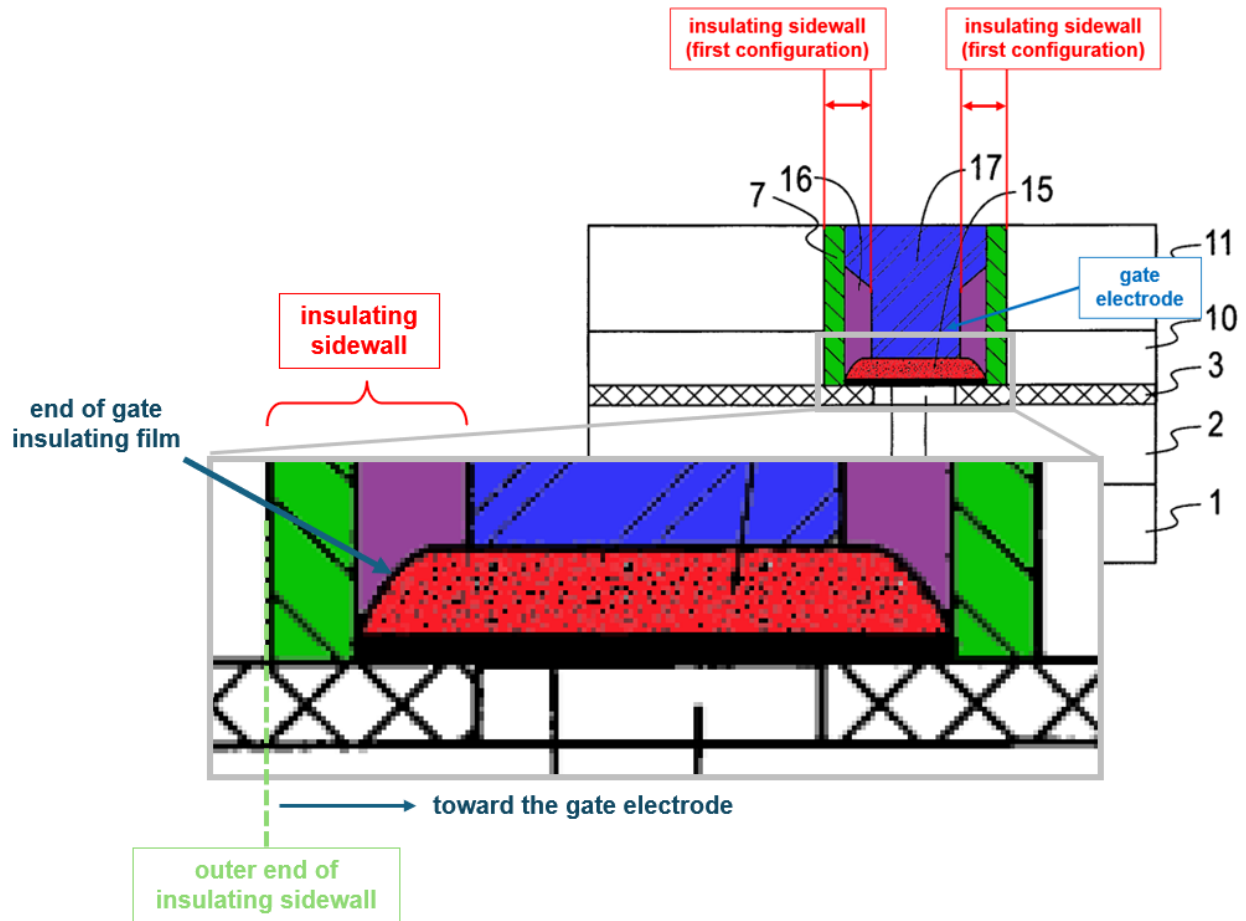
5. Limitations [1D]-[1E]

Guha discloses limitations [1D]-[1E] under the first and second “*insulating sidewall*” configurations. (TSMC-1003, ¶¶206-11.)

a. First Configuration (Spacer 16 and Spacer 7)

As shown below, dielectric layer 15 is an uninterrupted layer (as evidenced by absence of gaps) extending from under the gate electrode (shaded blue) to under

gate spacer 16 (shaded purple), which is part of the “*insulating sidewall*” of the first configuration (gate spacer 16 and spacer 7). (TSMC-1003, ¶207; *Unified*, 2022 WL 500391, *17.) This is confirmed by Guha’s manufacturing process, in which dielectric layer 15 is formed first in cavity 13, gate spacers 16 are then formed to “contact[] both the dielectric layer 15 and the isolating spacer structure 7,” and finally gate electrode 17 is formed by filling the remainder of the cavity “with a conductive material.” (TSMC-1028, ¶¶43-45; TSMC-1003, ¶207.) Guha’s first configuration discloses “*the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall*” [1D]. (TSMC-1003, ¶208.)



Guha, Figure 12 (First Configuration) with enlargement

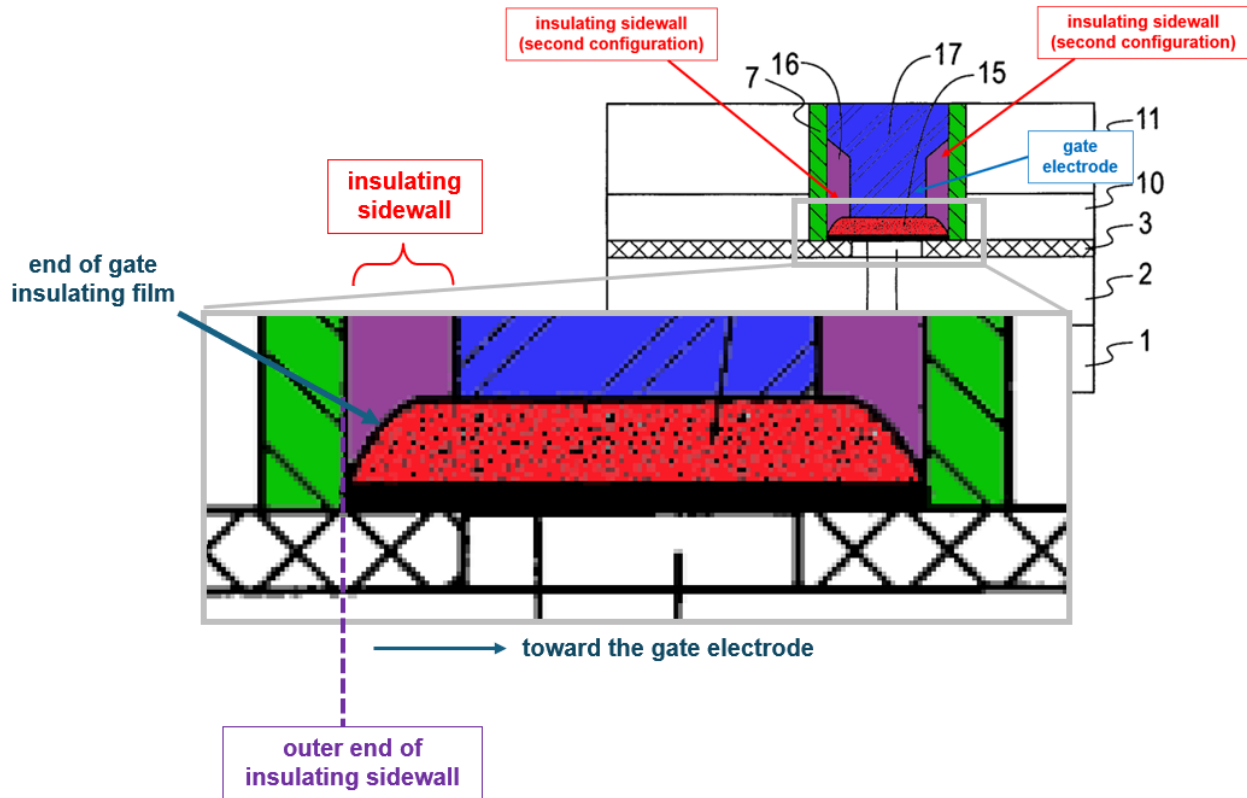
As shown above, the end of the gate insulating film is rounded and disposed at a distance inward from the outer end of the “*insulating sidewall*” (outer end of spacer 7). The distance which the end of Kamata’s gate insulating film extends inward toward the gate electrode is set by Guha’s manufacturing process discussed above. (TSMC-1003, ¶209.) Thus, the end of dielectric layer 15 (“*the high dielectric constant gate insulating film*”) is “*located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode*” [1E],

consistent with the '180 patent's disclosure and Applicant's prosecution statements. (TSMC-1001, 20:63-21:7; §IV.D.1; TSMC-1003, ¶209.)

b. Second Configuration (Spacer 16)

Similarly, dielectric layer 15 is an uninterrupted layer (as evidenced by absence of gaps) extending from under the gate electrode (shaded blue) to under gate spacers 16, which is the “*insulating sidewall*” of the second configuration. (TSMC-1003, ¶210; TSMC-1028, ¶¶43-45.) Thus, under the second configuration, Guha discloses limitation [1D]. (TSMC-1003, ¶210.)

As shown below, at least part of the end of dielectric layer 15 does not contact isolating spacer 7 (shaded green); thus, the entire end of dielectric layer 15 (“*the high dielectric constant gate insulating film*”) is not disposed beneath the outer end of the spacer 16. Additionally, the shape of the end of dielectric layer 15 and the distance which the end of dielectric layer 15 extends inward toward the gate electrode are set by Guha's deposition process. (TSMC-1003, ¶211; TSMC-1028, ¶43.) The end of dielectric layer 15 is therefore “*located at a predetermined distance from an outer end of the insulating sidewall* [outer end of spacer 16] *toward the gate electrode*” [1E]. (TSMC-1003, ¶211; TSMC-1002, 151-52.)



Guha, Figure 12 (Second Configuration) with enlargement

C. “Buffer Insulating Film” Claims

1. Claim 2

Guha’s gate-isolating layer 14 (shaded black) “acts as a buffering layer between channel 9 and the dielectric material to be deposited thereon” (i.e., high-k dielectric 15). (TSMC-1028, ¶¶37, 43, Figure 12 (below).) Channel 9 is part of the substrate. (§XII.B.2.) Gate-isolating layer 14 (“*buffer insulating film*”) is therefore “*between the substrate and the high dielectric constant gate insulating film*” [2]. (TSMC-1003, ¶¶213-14.)



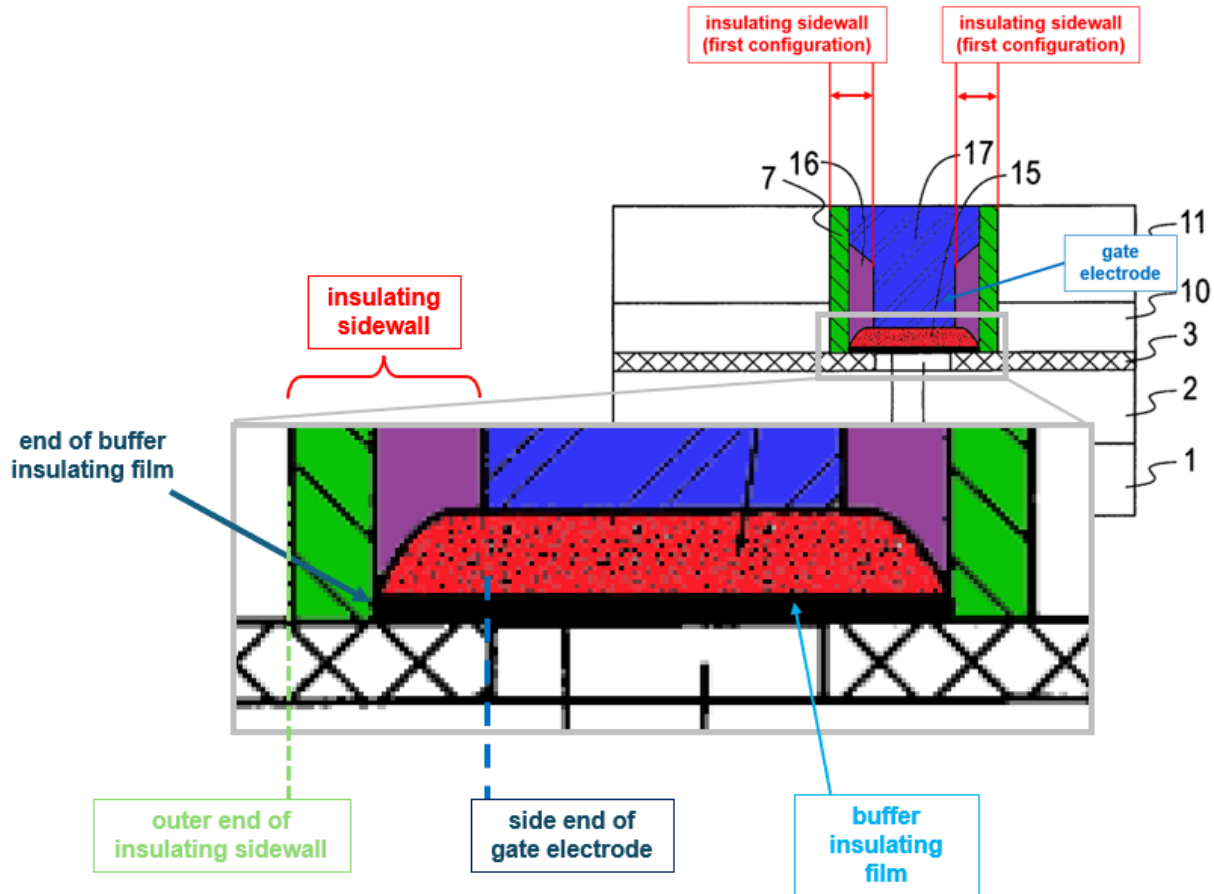
buffer insulating film

substrate

3. Claims 4, 12

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Gate-isolating layer 14 (“*buffer insulating film*”) is an uninterrupted layer of material (as evidenced by absence of gaps) formed “at the bottom” of cavity 13 which is defined by isolating spacers 7. (TSMC-1028, ¶¶28, 32-35, 37, 43.) Gate-isolating layer 14, like dielectric layer 15, extends from under the gate electrode to under spacers 16, but not under spacers 7. (TSMC-1003, ¶¶218-19; TSMC-1028, ¶¶43-45 (describing formation of gate spacers 16, dielectric layer 15, and gate electrode 17).) As shown below, the end of gate-isolating layer 14 is disposed a distance inward (“*predetermined distance*”) from the outer end of the “*insulating sidewall*” (outer end of spacers 7) which is also a distance from the side end of the gate electrode. (TSMC-1003, ¶¶218-19; §IV.D.1; *Unified*, 2022 WL 500391, *17.)



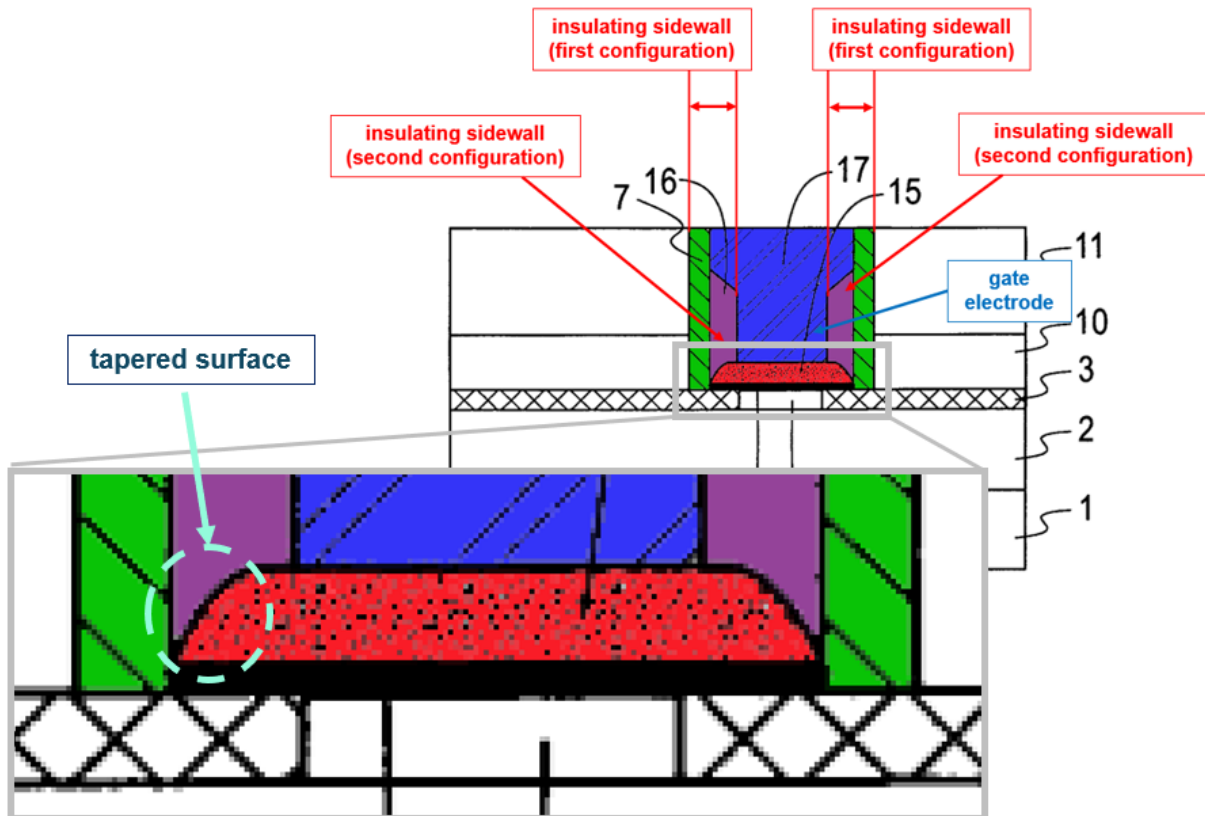
Guha, Figure 12 with enlargement

D. High-K Dielectric Claims

1. Claims 5, 21-22

Under both the first/second “*insulating sidewall*” configurations, Guha discloses the insulating film has “*a smallest thickness ... under the insulating sidewall*” that is smaller than “*under the gate electrode*” [5], “*a tapered surface*” under the insulating sidewall [21], and “*a thickness*” under the insulating sidewall [22] “*which becomes smaller toward the end thereof.*” (TSMC-1003, ¶¶220-22.)

In Guha's device, "the edge where the dielectric layer 15 meets the isolating spacer structure 7 ... is **rounded** either upwards or **downwards** (e.g., similar to a cusp)." (TSMC-1028, ¶43.) That is, dielectric layer 15 reduces in thickness at its end such that its smallest thickness is under spacer 16—i.e., it tapers. (TSMC-1003, ¶222; TSMC-1028, ¶44 (spacer 16 is formed after and on dielectric layer 15).) The tapered end of dielectric layer 15 is "*located under the insulating sidewall*" in the first configuration (**spacers 16** and spacers 7 collectively) and second configuration (**spacers 16**), and Guha discloses claims 5, 21, and 22. (TSMC-1003, ¶222.)



Guha, Figure 12

2. Claim 6

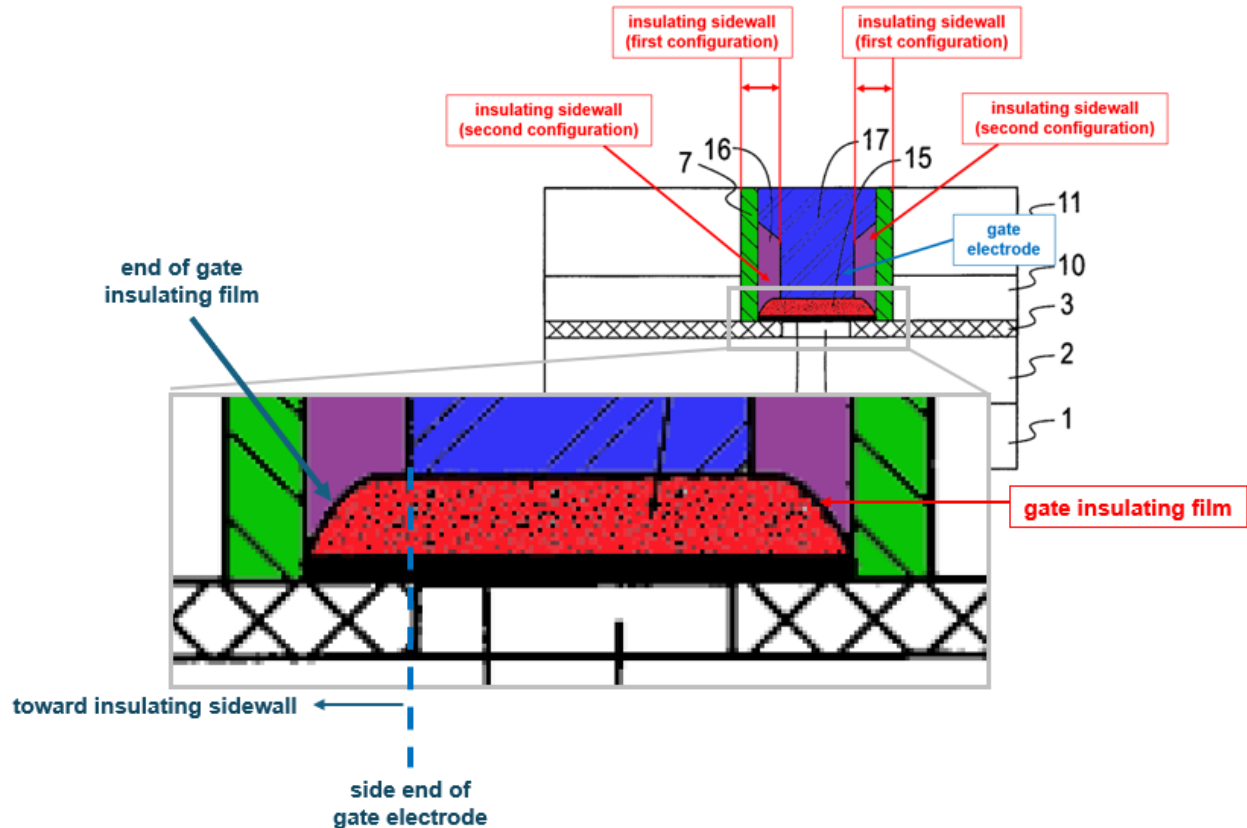
Guha's dielectric layer 15 ("*high dielectric constant gate insulating film*") "preferably compris[es] a high-K dielectric material" such as "**hafnium oxide**," which is "*a Hf based oxide*" [6]. (TSMC-1028, ¶¶38, 43.) A POSITA would have been motivated to select HfO₂ in light of its known benefits, including thermal stability, band alignment, and ability to scale. (TSMC-1037, 2.4.1; TSMC-1032, 207; TSMC-1049, 134; TSMC-1003, ¶223; §V.E.)

3. Claim 13

Guha discloses claim 13's "*predetermined distance*" limitation under the first/second "*insulating sidewall*" configurations. (TSMC-1003, ¶¶224-25.)

In Guha's device (below), the rounded end of the gate insulating film protrudes from under the gate electrode (shaded blue) and is disposed under spacers 16 (i.e., rounded end is not flush with the side end of the gate electrode). (TSMC-1003, ¶224.) In the first configuration (spacers 16 and 7), the distance which the end of Guha's gate insulating film extends outward from the gate electrode is set by Guha's manufacturing process. (TSMC-1003, ¶225.) In the second configuration (spacers 16 alone), the shape of the end of Guha's gate insulating film and the distance which the end extends outward from the gate electrode are set by Guha's deposition process. (*Id.*) Accordingly, the end of dielectric layer 15 is "*located at a predetermined distance from a side end of the*

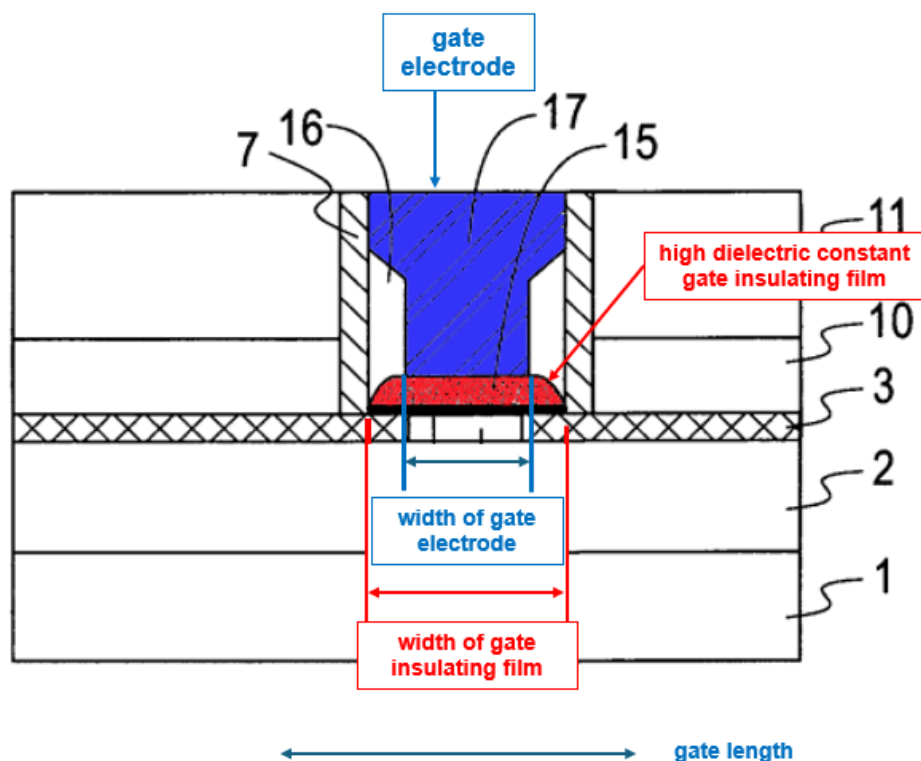
gate electrode toward the insulating sidewall” [13] in the first and second configurations. (Id.)



Guha, Figure 12 with enlargement

4. Claims 16-17

As shown in Figure 12, “a width of” and “a width of a bottom surface of” dielectric layer 15 (shaded red) is larger than “a width of” and “a width of a bottom surface of” the gate electrode (shaded blue) [16]-[17]. (TSMC-1003, ¶226; TSMC-1028, ¶¶41, 43-45 (describing formation of spacers 16 in cavity followed by deposition of gate electrode).)

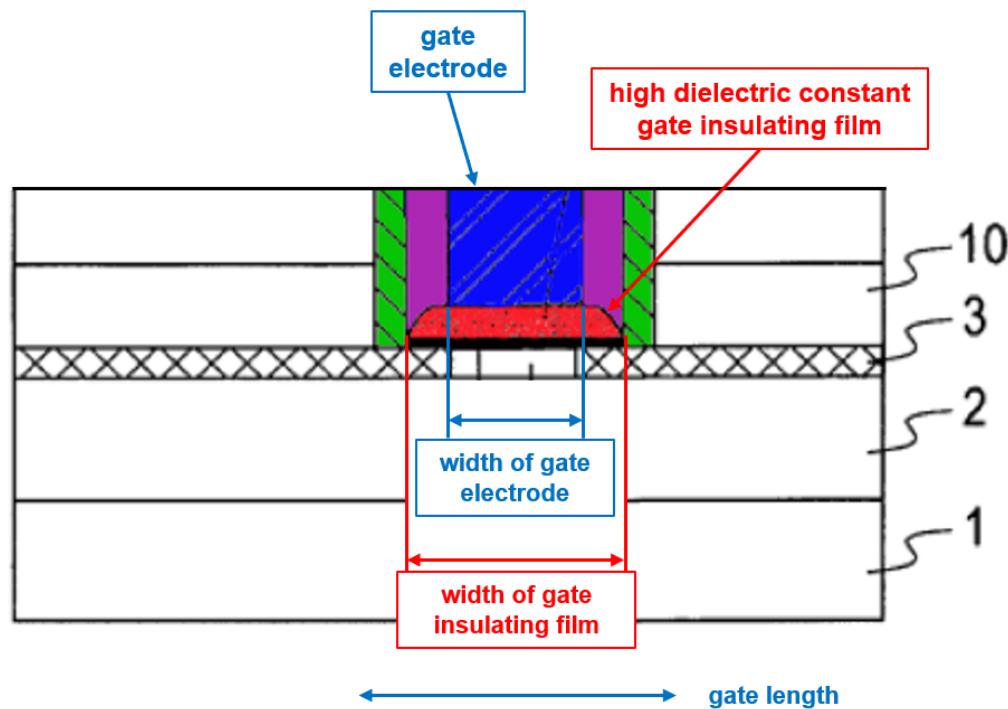


Guha, Figure 12

Should an argument be made the width of the gate electrode at its upper portion is equal to the width of dielectric layer 15 and therefore Guha fails to disclose claim 16, such an argument is improper. First, nothing in claim 16 requires the gate electrode width at all heights to be smaller than the width of the gate insulating film. (TSMC-1003, ¶227.)

Second, Guha discloses “internal spacer 16a and 16b may also have a rectangular cross-section, e.g., by polishing or removing the upper curved region to form a horizontal portion of the internal surface.” (TSMC-1028, ¶47.) A POSITA would have understood, with this teaching, the expanded upper portion of the gate

electrode is removed along with the slanted upper portion of spacers 16, resulting in a rectangular cross-section. (TSMC-1003, ¶228.) In this embodiment, shown in modified Figure 12 below, the gate electrode width is the same at the bottom and top. *Boston Sci. Scimed, Inc. v. Cordis Corp.*, 554 F. 3d 982, 991 (Fed. Cir. 2009) (“[c]ombining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness”).



Guha, Modified Figure 12

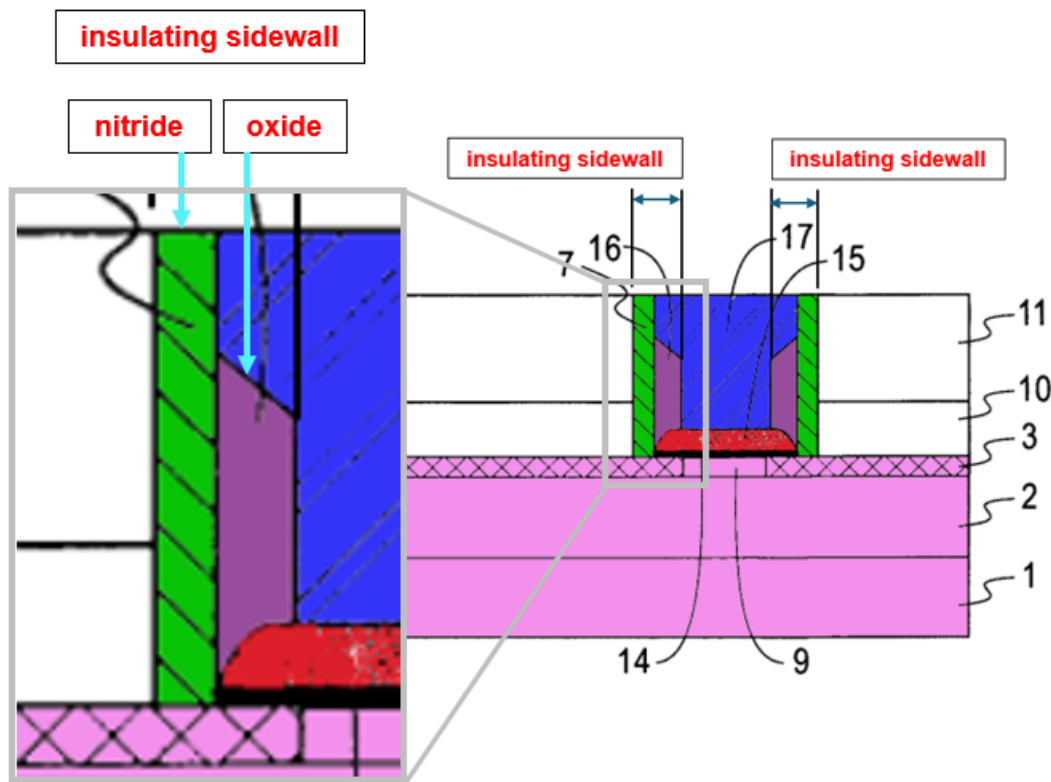
5. Claim 18

Guha discloses a “high-K material is a material that exhibits a **dielectric constant of approximately above 10 or more.**” (TSMC-1028, ¶38.) Accordingly, Guha discloses claim 18. (TSMC-1003, ¶229.)

E. “Insulating Sidewall” Claim 14

Guha discloses claim 14’s “*double layer structure*” under the first “*insulating sidewall*” configuration (spacer 16 and spacer 7). (TSMC-1003, ¶¶230-33.)

Gate spacer 16 is a “material, e.g. an **oxide** or other suitable material” and is thus “*an oxide film*.” (TSMC-1028, ¶40; TSMC-1003, ¶231.) Isolating spacer 7 “can be composed of any insulating material including, for example, an oxide, **nitride**, oxynitride or any combination thereof” with “**silicon nitride**” as the “preferred material.” (TSMC-1028, ¶28.) A POSITA would have considered gate spacer 16 and isolating spacer 7 to each be a “layer” of the collective sidewall, consistent with the ’180 patent’s disclosure. (*E.g.*, TSMC-1028, ¶¶28 (formation of spacers 7), 44 (formation of spacers 16); §XII.B.4; TSMC-1001, 20:43-52; TSMC-1003, ¶233.)



Guha, Figure 12

XIII. GROUND 9: Guha-Koyama Combination Renders Claim 7 Obvious.

Guha describes use of “**hafnium silicate**” as a high-k gate dielectric but does not expressly disclose use of “*a HfSiON film*” [7]. (TSMC-1028, ¶38.)

Koyama discloses this teaching, as discussed in §VII.

A POSITA would have been motivated to combine Koyama’s teachings regarding use of HfSiON with Guha’s Figure 12 device. (TSMC-1003, ¶¶235-36.)

Koyama and Guha are in the same field as the ’180 patent. (TSMC-1001, 1:17-18; TSMC-1028, ¶1; TSMC-1029, Abstract; TSMC-1003, ¶234.) Accordingly, the

device of the Guha-Koyama combination discloses a high-k gate dielectric “*formed of a HfSiON film*” [7]. (TSMC-1003, ¶234.)

Guha motivates the combination, indicating that high-k dielectric materials are not “limited to” the materials on its list. (TSMC-1028, ¶38.) A POSITA would have been motivated to investigate other hafnium silicate options and would have been led to Koyama. (TSMC-1003, ¶235.) A POSITA would have further been motivated to make the combination to achieve the enhanced benefits of HfSiON high-k film, e.g., improved thermal stability and electrical characteristics, described by Koyama, discussed in §VII. (TSMC-1003, ¶235.)

Moreover, the combination is nothing more than the use of a known technique (Koyama’s use of HfSiON as a gate insulating film) to improve similar devices in the same way. *KSR*, 550 U.S. at 416-417; TSMC-1003, ¶236. A POSITA would have had a reasonable expectation of success and the combination would have yielded predictable results. (TSMC-1003, ¶236; §VII.)

XIV. GROUND 10: Guha-Sim Combination Renders Claim 11 Obvious.

Guha discloses use of “hafnium oxide” as a high-k gate dielectric (TSMC-1028, ¶38) but does not expressly disclose its thickness is “*2 nm or less*” [11]. Sim discloses this teaching. (§IX.) Accordingly, the Guha-Sim combination discloses “*part of the high dielectric constant gate insulating film located under the insulating sidewall has a thickness of 2 nm or less*” [11]. (TSMC-1003, ¶¶237-41.)

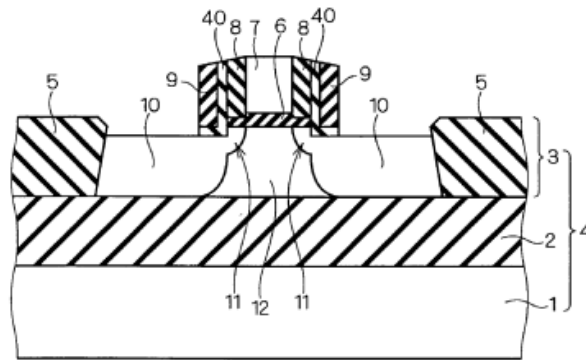
A POSITA would have been motivated to adopt Sim's solution of forming a gate insulating film with a thickness of 20Å (2 nm) or less in Guha's Figure 12 device. Sim and Guha are in the same field as the '180 patent. (TSMC-1001, 1:17-18; TSMC-1028, ¶1; TSMC-1024, Abstract; TSMC-1003, ¶237.) Sim discloses reducing the thickness of HfO₂ to below 20Å enhances mobility and reduces charge trapping, which ensures performance and scalability of semiconductor devices. (TSMC-1024, 219, 221; §IX.) Such improvements align with the continued miniaturization of devices, which Guha and Sim emphasize is crucial to advancing CMOS technology. (TSMC-1028, ¶2; TSMC-1024, 218; TSMC-1003, ¶240.)

Additionally, the combination is nothing more than use of a known technique (Sim's HfO₂ dielectric layer with less than 20Å thickness) to improve similar devices in the same way. *KSR*, 550 U.S. at 416-417; TSMC-1003, ¶241. A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable because Sim uses a well-known process, atomic layer deposition (ALD), for fabricating high-k films. (TSMC-1024, 218; TSMC-1032, 17-19; TSMC-1003, ¶241.)

XV. GROUND 11: Matsumoto Renders Obvious Claims 1, 5, 13-20.

A. Matsumoto

Matsumoto's fourth embodiment MOSFET includes gate insulating film 6 extending from under gate electrode 7 to under only film 8 formed on the gate electrode's sidewalls. (TSMC-1009, ¶¶137-140, Figure 22 (below).)



Matsumoto, Figure 22

B. Independent Claim 1

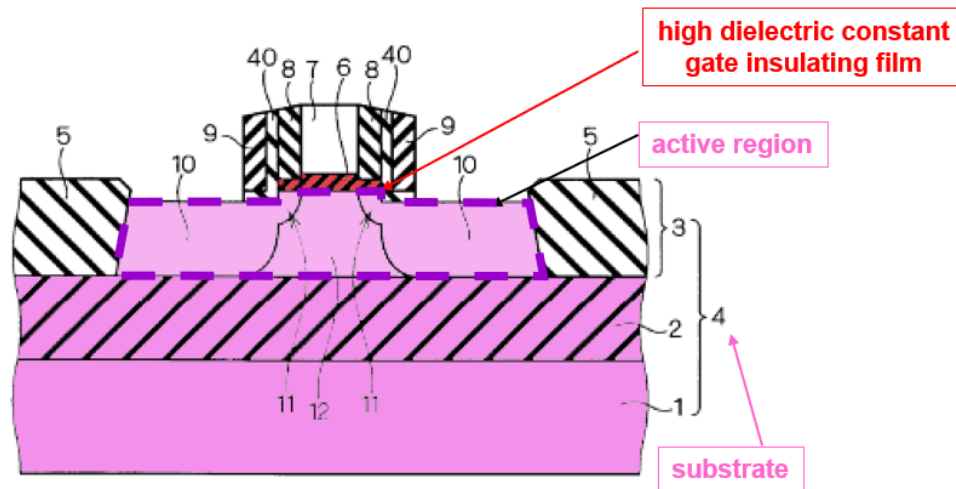
1. Preamble [1P]

Matsumoto discloses a “*semiconductor device*”: “present invention relates to a **semiconductor device**.” (TSMC-1009, ¶¶2, 137.)

2. Limitation [1A]

Matsumoto's device includes “*a substrate*.” (TSMC-1003, ¶249.) The device has multi-layer SOI **substrate** 4 (shaded pink) with silicon substrate 1, BOX layer 2 and single-crystalline silicon layer 3. (TSMC-1009, ¶102, ¶¶137, 140 (relating fourth embodiment to first embodiment), Figure 22 (below)); *Google*,

2022 WL 4287797, *9 n.9 (applying same disclosure where “figures refer to corresponding features using the same reference numbers”).)



Matsumoto, Figure 22

Isolating insulation film structures 5 extending from the upper surface of silicon layer 3 to the upper surface of BOX layer 2 define a “**device region.**” (TSMC-1009, ¶¶102-103, ¶¶137, 140.) The device region, identified by isolation regions, is an “*active region in a substrate*” and includes source/drain regions 10. (TSMC-1009, ¶139; TSMC-1003, ¶250; TSMC-1001, 1:41-42), 7:28-45.)

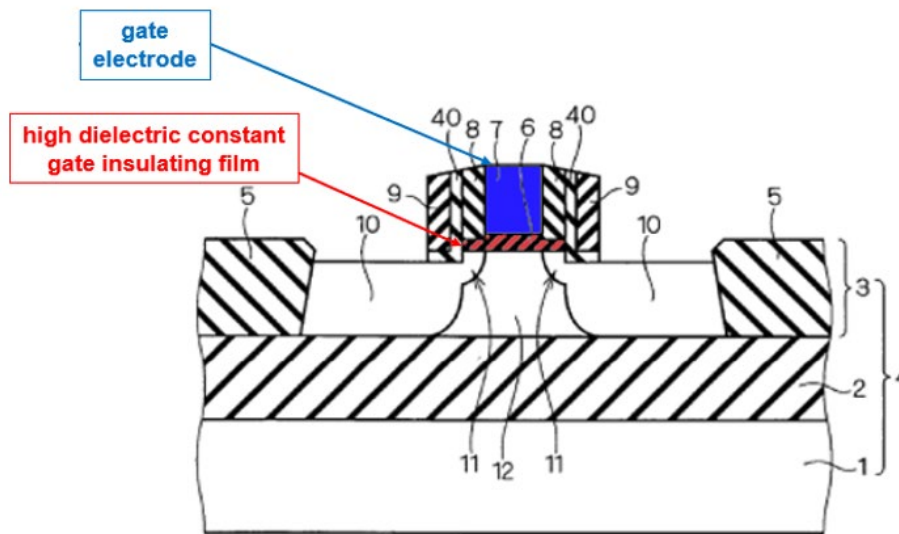
Film 6 “is formed partially on the upper surface of the silicon layer 3” in the device region with gate electrode 7 “formed partially” thereon. (TSMC-1009, ¶¶103 (first embodiment), 137 (fourth embodiment “gate electrode 7 is formed by the process described in the first preferred embodiment”).) “A silicon oxynitride film, a metal oxide film such as Al_2O_3 or a ferroelectric film such as Ta_2O_5 and

BST may be formed in place of the silicon oxide film 13,” which is etched during fabrication to form film 6. (TSMC-1009, ¶¶107, 138, Figures 18-19, 22.) Al₂O₃, Ta₂O₅, and BST are high-k dielectrics. (TSMC-1003, ¶253; TSMC-1001, 1:30-32 (“**high dielectric constant film** formed of a Hf based oxide, Al based oxide or the like”); TSMC-1018, Table I.) A POSITA would have been motivated to use a high-k dielectric in Matsumoto’s device to address the well-documented issues with scaling SiO₂ to thicknesses needed for large scale device integration. (TSMC-1032, 3-12; TSMC-1034, 4-5, 146-47; TSMC-1003, ¶254.)

Film 6 is “*a high dielectric constant gate insulating film formed on an active region in a substrate*” [1A]. (TSMC-1003, ¶255; TSMC-1009, ¶103 (referring to film 6 as “gate insulation film”).)

3. Limitation [1B]

In Matsumoto’s device, “**gate electrode 7** [shaded blue] made of polysilicon **is formed partially**” on high-k gate insulating film 6 (shaded red). (TSMC-1009, ¶¶103, 107 (describing formation of high-k gate insulating film and gate electrode), 137-138, Figure 22 (below).) Thus, Matsumoto discloses limitation [1B]. (TSMC-1003, ¶¶256-57.)

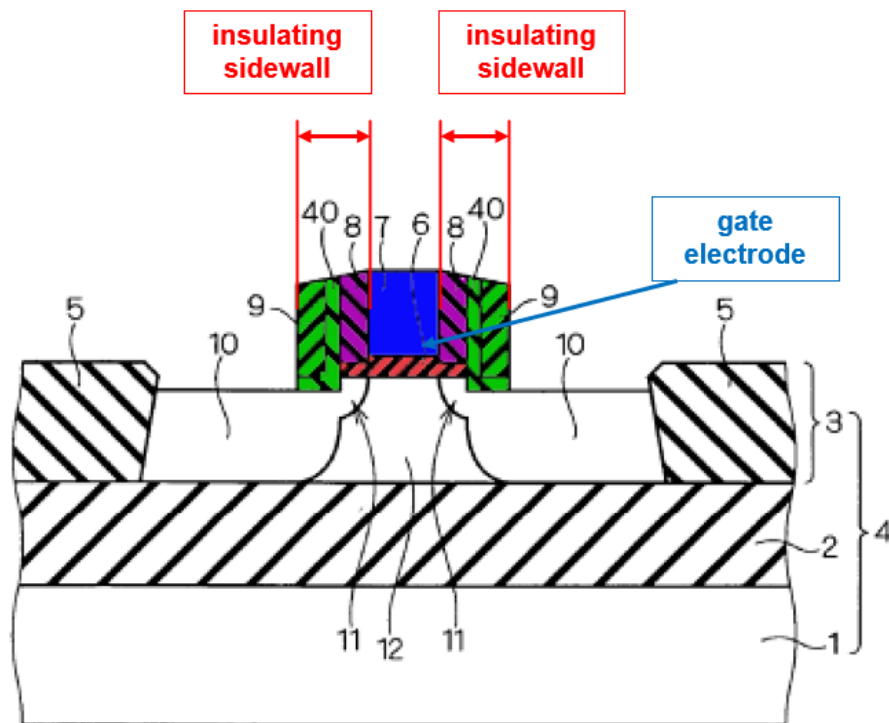


Matsumoto, Figure 22

4. Limitation [1C]

In Matsumoto's device, silicon oxide film 40 and silicon nitride film 9 are formed "on the outer side surfaces of" silicon oxide film 8. (TSMC-1009, ¶139, Figure 22 (below).) Matsumoto refers to film 9 as a "sidewall insulation film" but does not refer to films 40 or 8 as a "sidewall." (TSMC-1009, ¶114 (describing nitride films 9a/9b "serving as **sidewall** insulation films").) A POSITA would have understood films 40 and 8 also to be sidewalls. (TSMC-1009, ¶¶104, 110, 139, 40 ("semiconductor device further includes a second sidewall formed on the side surface of the gate electrode, with the first sidewall therebetween"); TSMC-1003, ¶261.) Because silicon oxide and silicon nitride are both insulators, film 8, film 40, and film 9 are collectively "*a insulating sidewall formed on each side surface of*

the gate electrode” [1C]. (TSMC-1009, ¶¶110 (describing formation of silicon oxide films 8a/8b on the side surfaces of the gate electrodes), 114, claim 1 (referring to “insulation films” formed on side surfaces of gate electrode); TSMC-1001, 2:58-63 (referring to multiple components collectively as an “insulating sidewall”); TSMC-1003, ¶261.)

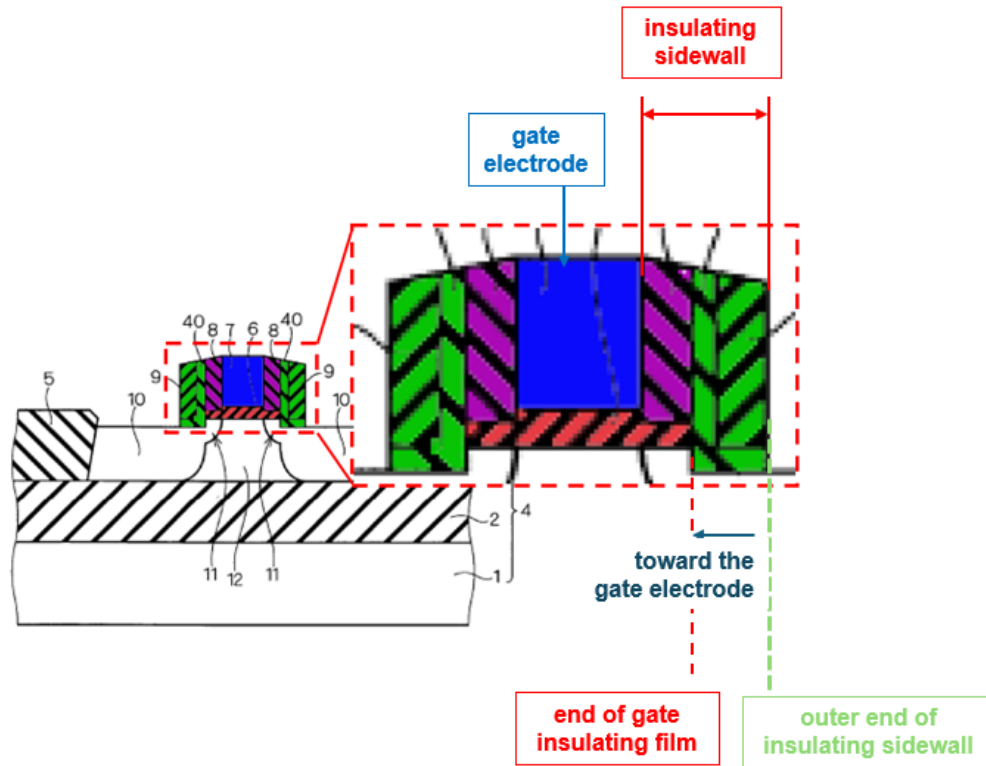


Matsumoto, Figure 22

5. Limitations [1D]-[1E]

As shown in Figure 22, Matsumoto’s gate insulating film 6 (shaded red) is an uninterrupted layer extending from under the gate electrode to under only film 8, part of the “insulating sidewall” (collectively films 8, 40, 9). (TSMC-1003, ¶262.) The end of gate insulating film 6 is perpendicular to the substrate’s surface.

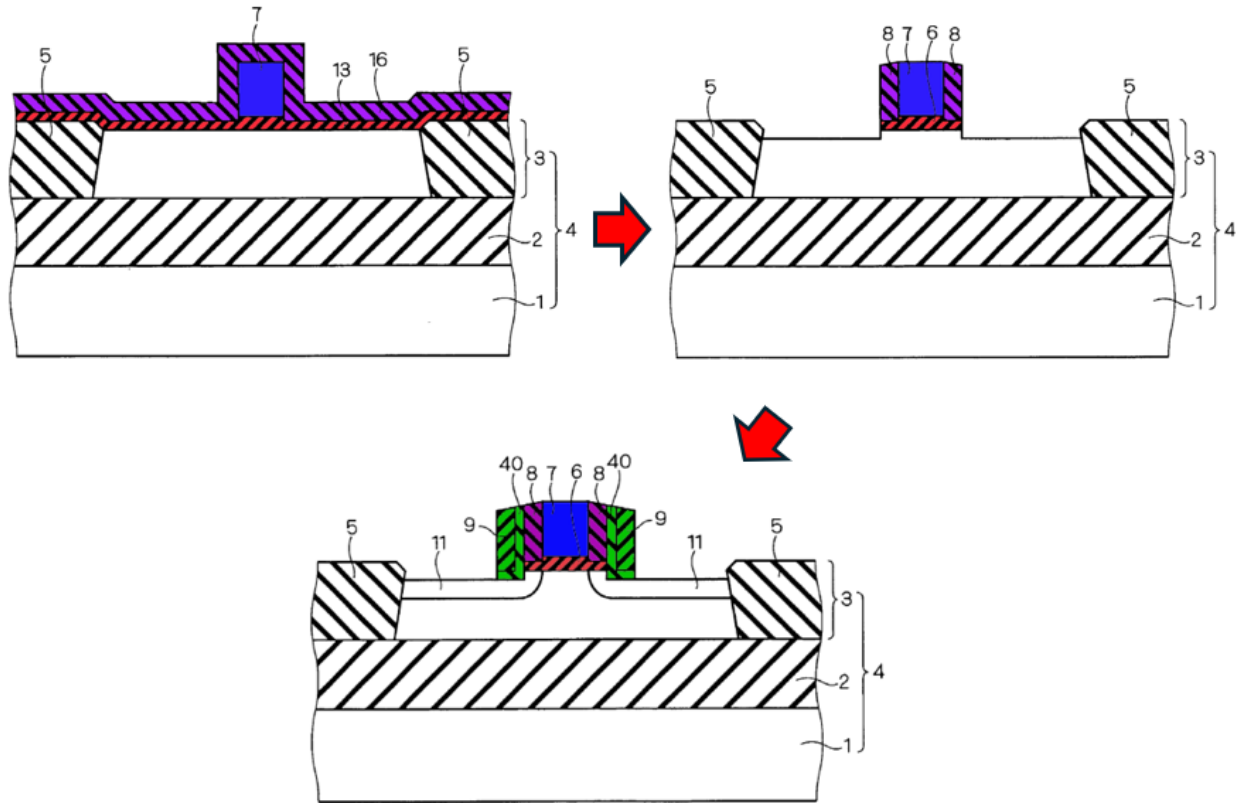
As shown below, the end of gate insulating film 6 is disposed at a distance inward from the outer end of sidewall 9 (outer end of the “*insulating sidewall*”) toward the gate electrode. (TSMC-1003, ¶263.) Further, the distance which the end of Matsumoto’s gate insulating film extends inward toward the gate electrode is set by Matsumoto’s manufacturing process, discussed below. (TSMC-1003, ¶¶263-64.) Thus, the end of the gate insulating film is “*located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode*” [1E], consistent with the ’180 patent’s disclosure and Applicant’s prosecution statements. (TSMC-1001, 21:1-7; TSMC-1002, 151-52; §IV.D.1; TSMC-1003, ¶263; *Unified*, 2022 WL 500391, at *17.) Matsumoto discloses limitations [1D]-[1E]. (TSMC-1003, ¶¶262-66.)



Matsumoto, Figure 22 with enlargement

The fabrication process confirms the presence of these features in Matsumoto’s device. After formation of gate electrode 7, high-k dielectric film 13 extends beyond the gate electrode with a larger thickness under the gate electrode. (TSMC-1009, ¶¶137, 107-08, Figure 18 (top-left); TSMC-1003, ¶265.) The etching process forming sidewall 8 (shaded purple) “overetch[es] the upper surface of the silicon layer 3” thereby leaving high-k dielectric film (shaded red) only under the gate electrode and film 8. (TSMC-1003, ¶266; TSMC-1009, ¶138, Figure 19 (top-right).) Film 40 and film 9 (shaded green) are then formed on the

outer side surfaces of film 8 and in contact with the substrate. (TSMC-1009, ¶139; Figure 21 (bottom).)



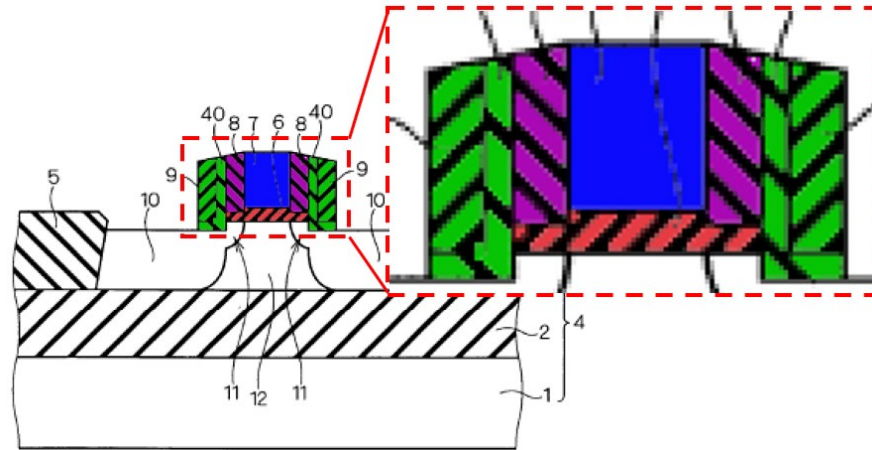
Matsumoto, Figures 18 (top-left), 19 (top-right), 21 (bottom)

C. High-K Dielectric Claims

1. Claim 5

As shown in Figure 22 and confirmed by the manufacturing process discussed above, Matsumoto’s high-k film 6 is thinner under film 8 of the “*insulating sidewall*” than it is under the gate electrode (shaded blue). (TSMC-1003, ¶¶267-69; TSMC-1009, ¶¶107-08, 137.) Matsumoto discloses the “*smallest thickness*” of the high-k film 6 under the “*insulating sidewall*” is “*smaller than*” the

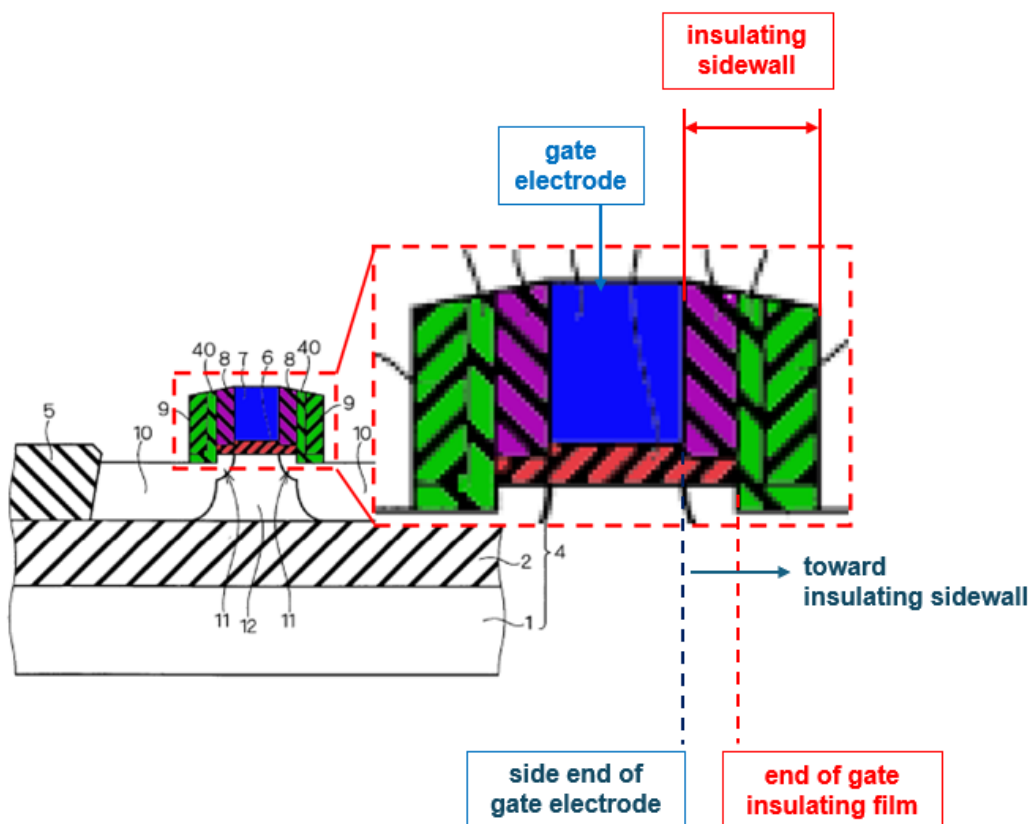
thickness of the part of the high-k film under the gate electrode [5]. (TSMC-1003, ¶¶267-69; *Unified*, 2022 WL 500391, *17.)



Matsumoto, Figure 22 with enlargement

2. Claim 13

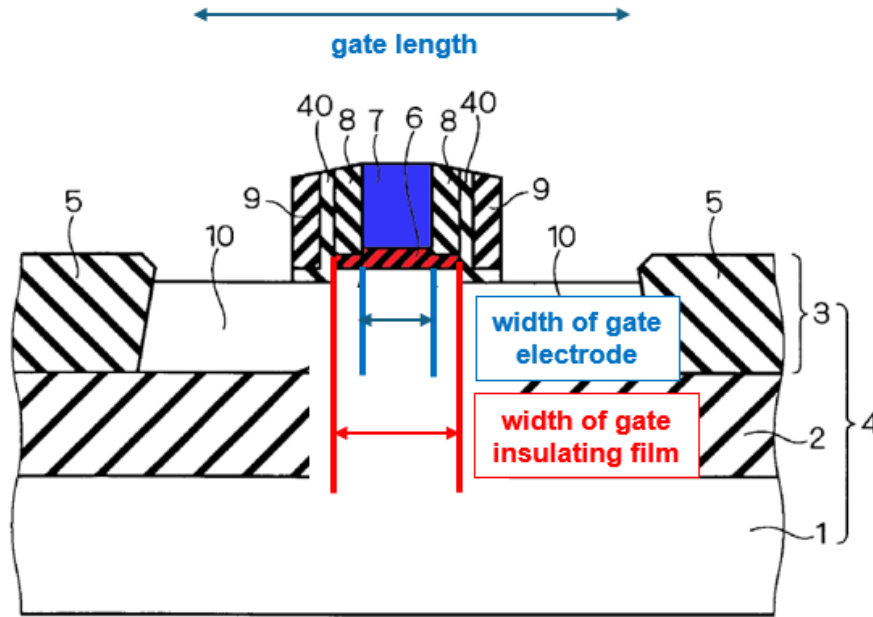
As shown in Figure 22, the end of high-k film 6 is disposed at a distance inward from the outer end of sidewall 9 which is also a distance outward from the gate electrode. (§XV.B.5.) The distance which the end of Matsumoto's gate insulating film extends outward from the gate electrode is set by Matsumoto's fabrication process. (TSMC-1003, ¶270.) Thus, the end of high-k film is "*located at a predetermined distance from a side end of the gate electrode toward the insulating sidewall,*" consistent with the '180 patent's disclosure and Applicant's prosecution statements. (TSMC-1001, 21:1-7; §IV.D.1; TSMC-1003, ¶270; *Unified*, 2022 WL 500391, *17.)



Matsumoto, Figure 22

3. Claims 16-17

As illustrated below, “*a width of*” and “*a width of a bottom surface of*” Matsumoto’s gate insulating film 6 (shaded red) is larger than “*a width of*” and “*a width of a bottom surface of*” the gate electrode (shaded blue) [16]-[17]. (§XV.B.5; TSMC-1003, ¶¶275-76; *Unified*, 2022 WL 500391, *17.) The fabrication process of Matsumoto’s device (§XV.B.5) confirms the Figure 22 structure.



Matsumoto, Figure 22

4. Claims 18-19

Matsumoto's fourth embodiment, using knowledge of a POSITA as reflected in the AAPA, renders the "*relative dielectric constant*" limitations of claims 18-19 obvious. (TSMC-1003, ¶277; TSMC-1001, 1:30-33 (AAPA).)

Matsumoto discloses use of, e.g., " Ta_2O_5 " as a gate insulating film. (TSMC-1009, ¶107.) The dielectric constant for Ta_2O_5 is 26, which is greater than 10. (TSMC-1018, Table I.) Sidewall films 8 and 40 are comprised of silicon oxide (SiO_2), having a dielectric constant of 3.9, and sidewall film 9 is comprised of silicon nitride (Si_3N_4), having a dielectric constant of 7. (TSMC-1009, ¶¶110, 114, 139; TSMC-1018, Table I; TSMC-1052, Figure 4.) Accordingly, a POSITA would have known the relative dielectric constant of sidewall films 8, 40, and 9

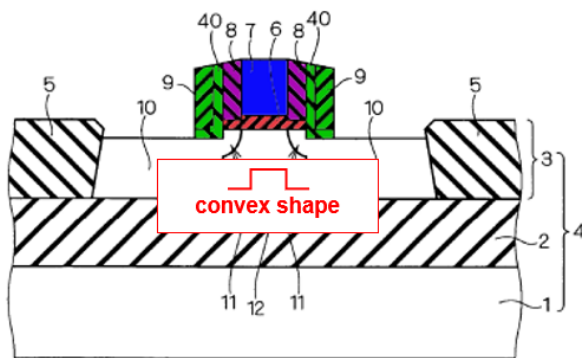
collectively is also under 10, which is smaller than the dielectric constant of Ta₂O₅.
(TSMC-1003, ¶¶278-79.)

5. Claims 20

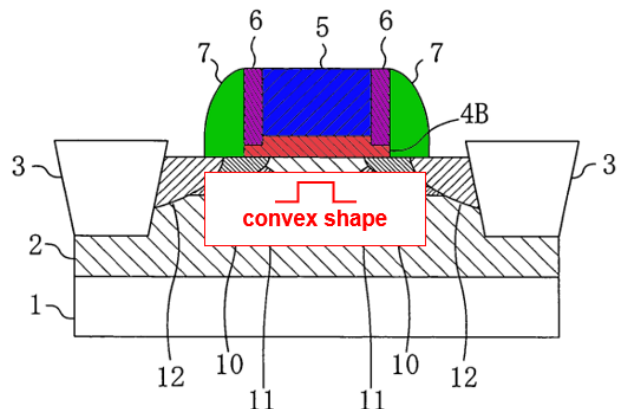
In Figure 22 (left), the gate insulating film portion under film 8 in Matsumoto's device has a smaller thickness than the gate insulating film portion under the gate electrode. (§XV.C.1.) This forms a gate insulating film having “a convex cross-sectional shape” [20], consistent with the '180 patent's disclosure:

It is a second feature of this embodiment that the thickness of the part of the high dielectric constant gate insulating film 4A located under the sidewall 7 is smaller than a thickness of the part of the high dielectric constant film 4A located under the gate electrode 5. That is, the gate insulating film 4A is formed so as to have a convex shape.

(TSMC-1001, 7:52-57 (referring to Figure 2); TSMC-1003, ¶¶281-82.)



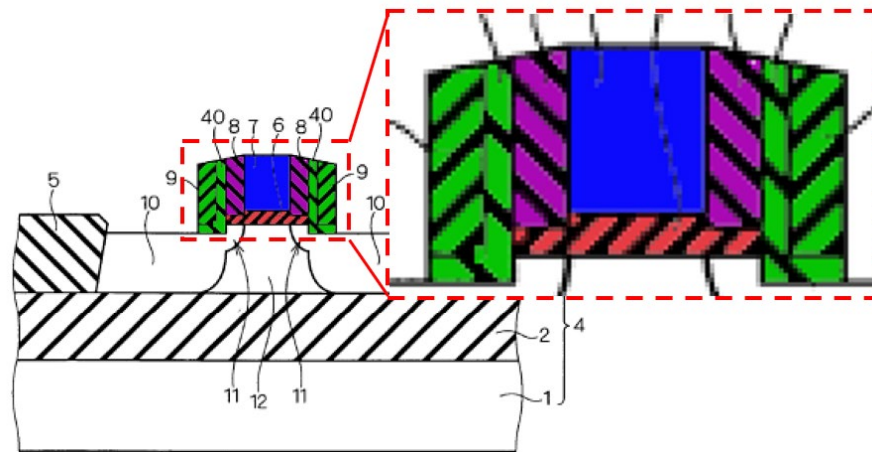
Matsumoto, Figure 22



'180 Patent, Figure 2

D. “Insulating Sidewall” Claims 14-15

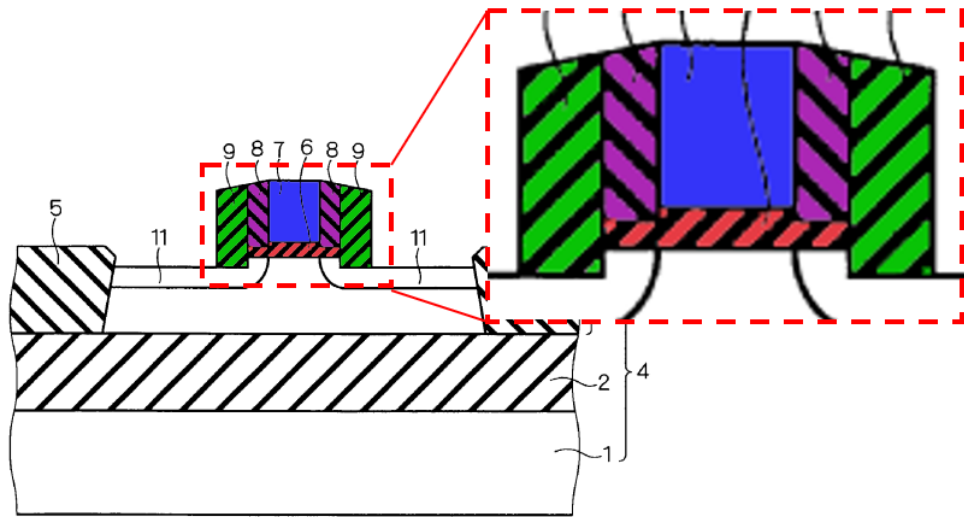
Matsumoto’s device includes an “*insulating sidewall*” comprising film 8 (shaded purple) and films 40 and 9 (shaded green). (§XV.B.4.) Films 8 and 40 are silicon oxide and film 9 is silicon nitride. (TSMC-1009, ¶139 (“This forms silicon oxide films 40 and the silicon nitride films 9 on the outer side surfaces of the silicon oxide films 8”).) A POSITA would have considered films 8, 40, and 9 to each be a “layer” of the collective sidewall, consistent with the ’180 patent’s disclosure. (TSMC-1003, ¶272; TSMC-1001, 20:43-52.) Matsumoto therefore discloses “*the insulating sidewall has a triple layer structure including a first oxide film [silicon oxide film 8], a nitride film [silicon nitride film 9], and a second oxide film [silicon oxide film 40]*” [15]. (TSMC-1003, ¶272.)



Matsumoto, Figure 22 with enlargement

Matsumoto discloses a modification of the fourth embodiment omitting layer 40. In this modification, “silicon nitride films 9 are formed directly on the upper

surface of the silicon layer 3.” (TSMC-1009, ¶141, Figure 23 (below).) Matsumoto explains this modification “is applicable to any one of the first to fourth preferred embodiments” and therefore the analysis of the fourth embodiment in §§XV.B.1-5 applies equally. *Boston Sci.*, 554 F. 3d at 991. Thus, Matsumoto’s fourth embodiment modification meets each limitation of claim 1 and further discloses “the insulating sidewall [collective structure of silicon oxide film 8 and silicon nitride film 9] has a double layer structure including an oxide film and a nitride film” [14]. (TSMC-1003, ¶¶273-74.)

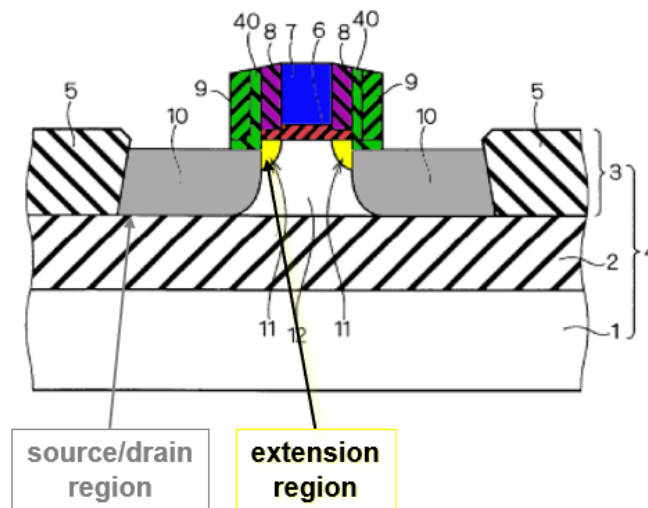


Matsumoto, Figure 23 with enlargement

XVI. GROUND 12: Matsumoto-Rodder Combination Renders Claims 8-9 Obvious.

As shown in Figure 22 (below), Matsumoto’s device includes extensions 11 (shaded yellow) located under sidewall film 8 “in the upper surface of the silicon layer 3” (part of substrate’s “active region”). (TSMC-1009, ¶139 (describing

formation of extensions 11), Figures 20-21.) Matsumoto's substrate also includes source/drain regions (shaded gray). (TSMC-1009, ¶139.) In the context of a different embodiment, Matsumoto specifies use of a pocket region having a different conductivity type than the extensions and source/drain regions, which have the same conductivity type. (TSMC-1009, ¶¶113, 116.) A POSITA would have been motivated to use these teachings in Matsumoto's fourth embodiment because the arrangement of these features was well-known in the art. (TSMC-1003, ¶288; TSMC-1041, 121-123; *Boston Sci.*, 554 F. 3d at 991.) Indeed, the '180 patent admits as AAPA that "*extension region[s]*", "*pocket region[s]*", and "*source/drain regions*" were known in prior art devices. (TSMC-1001, 1:47-53, Figures 16A-B; §VIII.) Regardless, Rodder discloses these features.

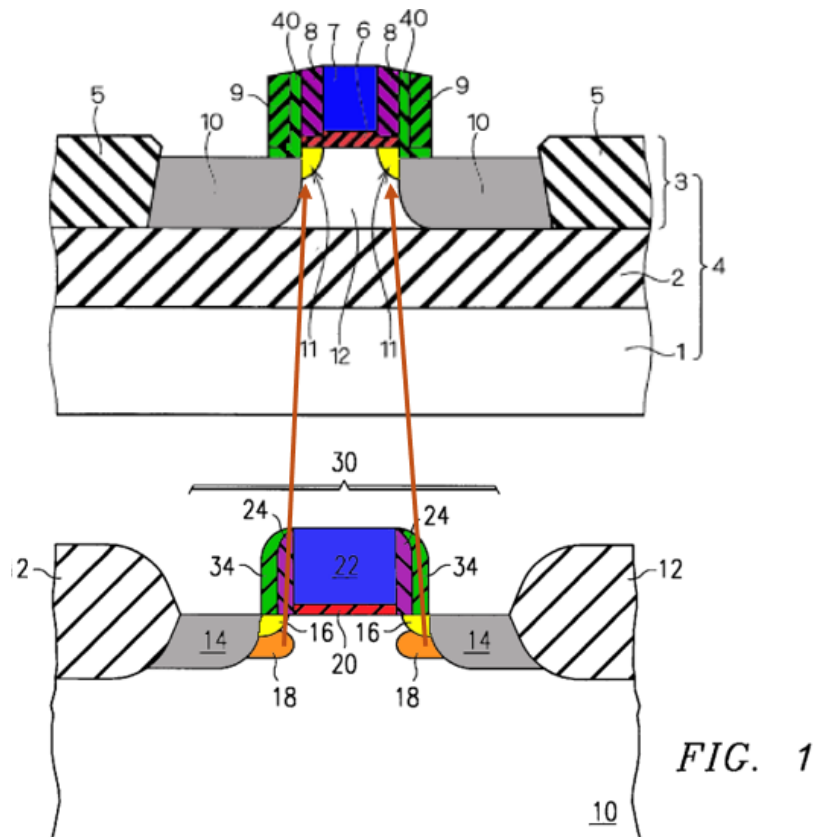


Matsumoto, Figure 22

Rodder describes “*pocket regions*” placed under its extension regions.

(TSMC-1023, 4:35-36.) Rodder also discloses its source/drain regions are located external to the extensions and pocket regions, when viewed from the gate electrode. (E.g., TSMC-1023, Figure 1.) A POSITA would have been motivated to combine Rodder’s teachings regarding placement and conductivity type of “*pocket regions*”, extension regions, and source/drain regions with Matsumoto’s device, as shown below. Rodder and Matsumoto are in the same field as the ’180 patent.

(TSMC-1001, 1:17-18; TSMC-1009, ¶2; TSMC-1023, Abstract; TSMC-1003, ¶284.)



Matsumoto, Figure 22 (top); Rodder, Figure 1 (bottom)

A POSITA would have been motivated to combine Matsumoto and Rodder to obtain the benefits of “*pocket regions*” and their location, described by Rodder. (TSMC-1023, 1:22-25; TSMC-1003, ¶¶291-94; §VIII.B.) Matsumoto also corroborates these benefits, noting pocket regions “suppress a short channel effect resulting from device size reduction.” (TSMC-1009, ¶111.) The combination is also nothing more than use of a known technique (Rodder’s formation of pocket regions below extension regions and outside of source/drain regions) to improve similar devices in the same way for the above reasons. *KSR*, 550 U.S. at 416-417; TSMC-1003, ¶294. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable for the reasons discussed in §VIII.B.

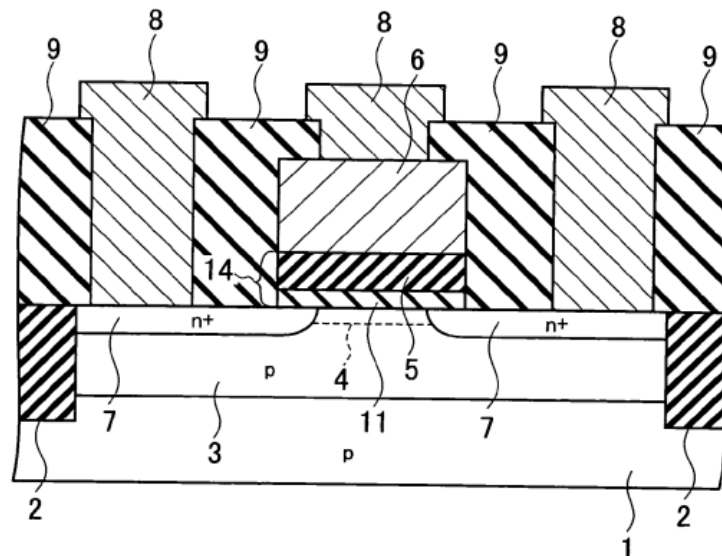
In the Matsumoto-Rodder combination, pocket regions of an opposite conductivity to Matsumoto’s extensions and source/drain regions are formed under the extensions and the source/drain regions are external to the pocket regions, as taught by Rodder. The combination therefore renders claims 8-9 obvious.

XVII. GROUND 13: Matsumoto-Ono Combination Renders Claim 10 Obvious.

Matsumoto’s fourth embodiment does not expressly disclose the high-k gate insulating film “*includes a notch at the end thereof*” [10]. Ono discloses this feature, and the Matsumoto-Ono combination renders claim 10 obvious.

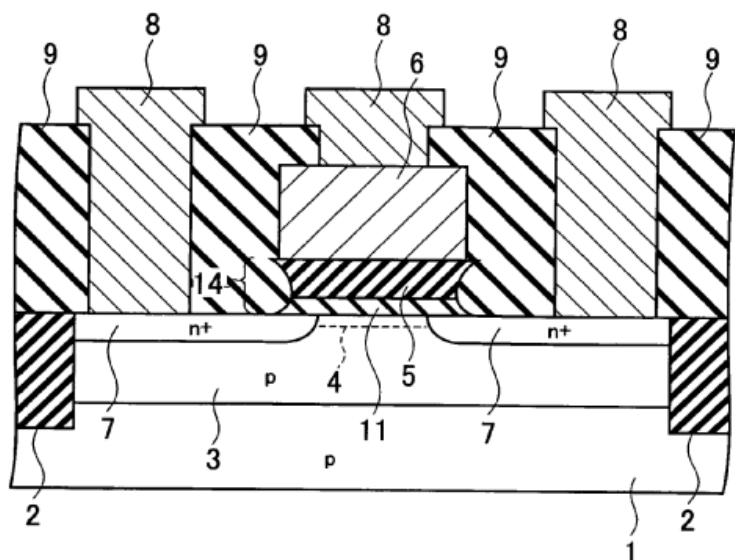
A. Ono

Ono's second embodiment FET includes a gate stack comprising gate insulator film 5 "made of a metal oxide" and gate insulator film 11 "made of a metal oxide with a higher dielectric constant than the gate insulator film 5" which is made of a "HfO₂ film." (TSMC-1013, ¶¶207, 209, Figure 77.) Gate electrode 6 is formed on gate insulator film 5 and can have gate sidewalls. (TSMC-1013, ¶¶207, 181, 210, Figure 77.)



Ono, Figure 77

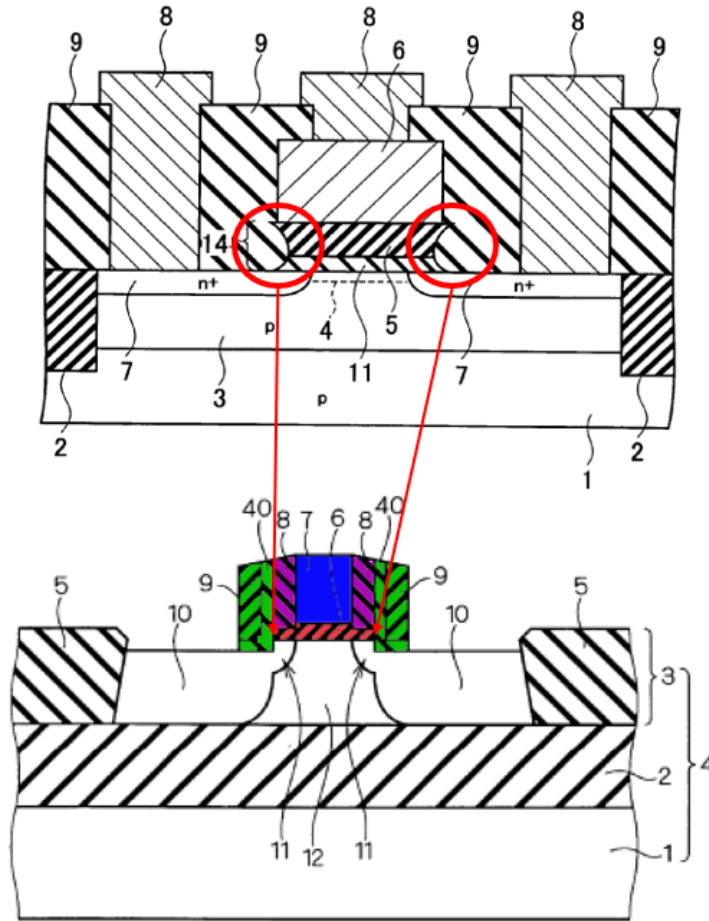
Ono discloses a modification where the side end portions of the gate insulating film "may curve." (TSMC-1013, ¶216.) Ono discloses numerous examples of such curved end portions (Figures 104-123). (*Id.*) Petitioner focuses its analysis on the structure depicted in Figure 108 (below), although other structures are equally applicable.



Ono, Figure 108

B. Motivation to Combine

A POSITA would have been motivated to apply Ono's teaching of curving the end portion of a gate insulating film to Matsumoto's fourth embodiment, shown below. (TSMC-1003, ¶¶301-05.) Ono and Matsumoto are in the same field as the '180 patent. (TSMC-1001, 1:17-18; TSMC-1009, ¶2; TSMC-1013, Abstract, ¶¶3-7; TSMC-1003, ¶296.) In the combination, the side ends of Matsumoto's gate insulating film have a semicircular shape, as taught by Ono.



Ono, Figure 108 (top); Matsumoto, Figure 22 (bottom)

Ono expressly suggests the combination, disclosing that using curved ends for the gate insulating film “reduc[es] the scattering of carriers as well as enhanc[es] the controllability of the gate electrode with respect to the potential of the channel region” and provides “an advantage of possible optimization.” (TSMC-1013, ¶216, ¶200 (noting, for first embodiment, by using curved side surfaces, “the electrical capacitance between the gate electrode 6 and the source/drain regions 7 may be adjusted,” resulting in “an advantage of optimization”). A POSITA would have been further motivated to curve the end of Matsumoto’s gate insulating film

to optimize parasitic resistance and parasitic capacitance, improving device performance. (TSMC-1003, ¶305; TSMC-1040, ¶108; §IV.B.2.)

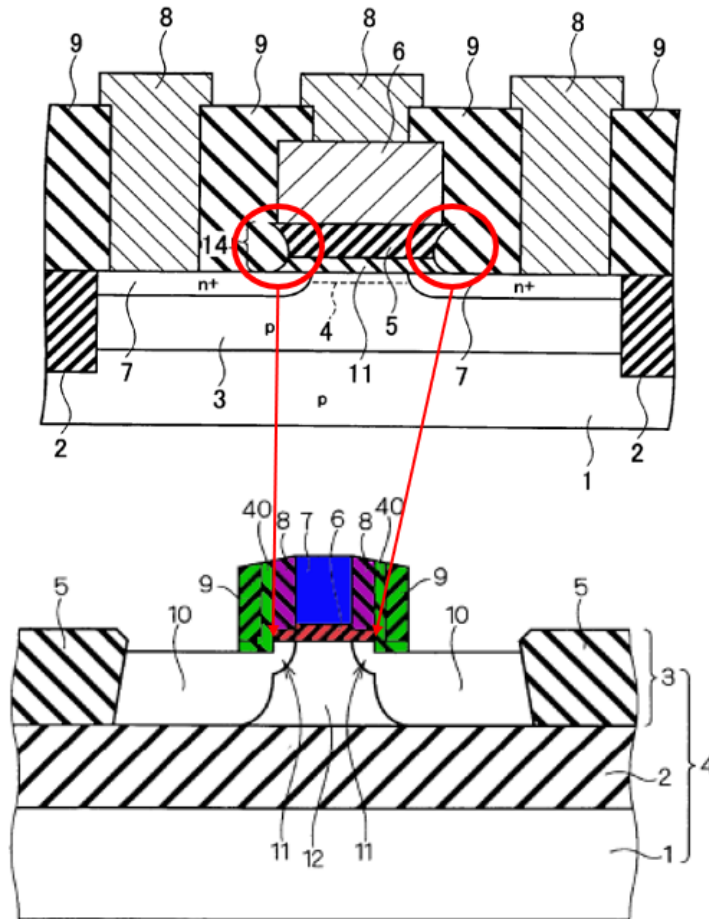
The Matsumoto-Ono combination is merely the application of a known technique (Ono’s curved film ends) to improve similar devices in the same way for the above reasons. *KSR*, 550 U.S. at 416-17; TSMC-1003, ¶306. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable. (TSMC-1003, ¶306.) Matsumoto and Ono both use high-k gate insulating films extending under the gate electrode and the insulating sidewall, a concept well-known before the ’180 patent. (§§IV.B.2.b, IV.D.2, V.B.5, XVII.A.) And both form their high-k dielectrics using conventional techniques. (TSMC-1009, ¶114; TSMC-1013, ¶167; TSMC-1003, ¶306.)

C. Claim 10

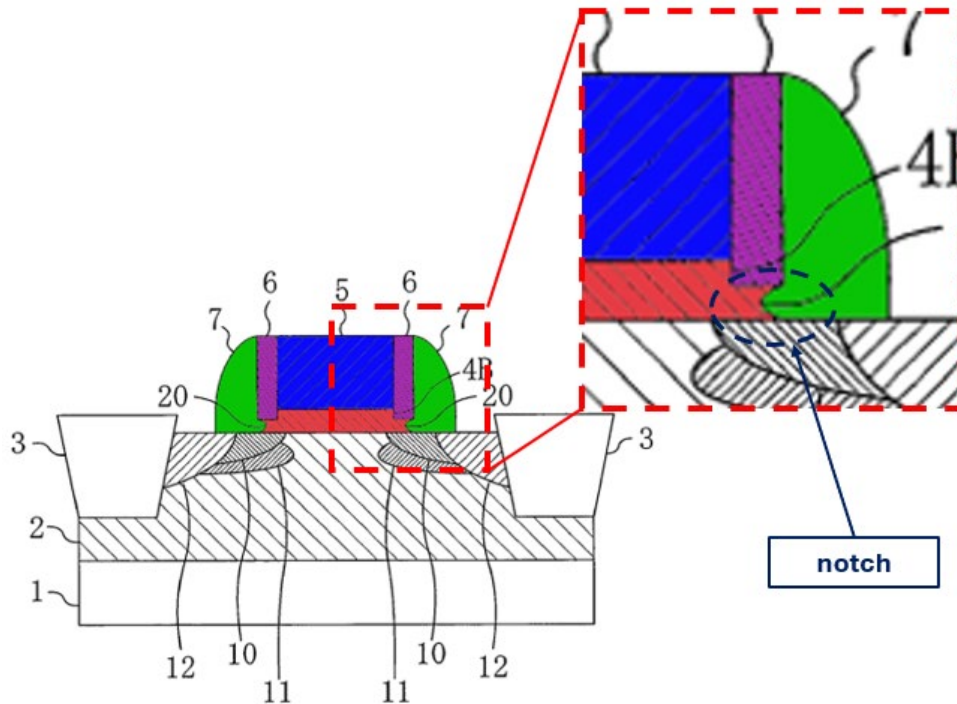
The Matsumoto-Ono combination discloses “*part of the high dielectric constant gate insulating film located under the insulating sidewall includes a notch at the end thereof*” [10]. (TSMC-1003, ¶¶301-06.)

In the Matsumoto-Ono device, the end portion of Matsumoto’s gate insulating film has a semicircular shape under film 8 (part of the “*insulating sidewall*”), as taught by Ono in, e.g., Figure 108. Consistent with the ’180 patent’s disclosure, the semicircular shape of the gate insulating film’s side end in the

combination discloses “a notch.” (E.g., TSMC-1001, 8:31-36 (referring to notch 20 of Figure 7), Figure 7 (depicting notch 20 having a semicircular shape under sidewall 6); TSMC-1003, ¶302.)



Ono, Figure 108 (top); Matsumoto, Figure 22 (bottom)



'180 Patent, Figure 7 with enlargement

XVIII. Discretionary Denial Is Not Appropriate.

A. 35 U.S.C. §314(a)

Pursuant to the Stewart Memorandum dated March 26, 2025, titled “Interim Process for PTAB Workload Management,” Petitioner will respond to any discretionary denial arguments Patent Owner may raise through the Board’s bifurcated briefing process.

Nevertheless, to simplify the *Fintiv* analysis, and following the precedential *Sotera* decision, Petitioner stipulates that, if IPR is instituted, Petitioner will not pursue in the related district court proceeding any ground that Petitioner raised or

reasonably could have raised against the challenged claims during the instituted IPR.

B. 35 U.S.C. §325(d)

The *Advanced Bionics* framework favors institution. *Advanced Bionics LLC v. MED-EL Elektromedizinische Gerate GmbH*, IPR2019-01469, Paper 6 (P.T.A.B. Feb. 13, 2020) (precedential). None of the applied references was applied by the Examiner during prosecution. Applicant cited a separate publication to Matsumoto (U.S. Publication 2004/0227185 (“Matsumoto-185”)) on an information disclosure statement. While Petitioner disputes Matsumoto-185 is sufficiently similar to Matsumoto to trigger *Advanced Bionics* Part 1, Matsumoto-185 was not applied by the Examiner and therefore was not evaluated during examination. Even assuming Matsumoto-185 was evaluated (which the record does not support), the Office erred in allowing the claims, because Matsumoto discloses the “predetermined distance” limitation argued by Applicant and determined to be allowable. (§§IV.D, XV.B.5.) Moreover, the Petition’s evidence warrants consideration because it presents a compelling case of unpatentability never considered by the Office. These circumstances weigh heavily against §325(d) discretionary denial.

XIX. Mandatory Notices

A. Real Party in Interest

The Petitioner and real party in interest is Taiwan Semiconductor Manufacturing Company Ltd.

B. Related Matters

To the best of Petitioner's knowledge, the '180 patent is involved in the following ongoing litigation:

- *Advanced Integrated Circuit Process LLC, v. Taiwan Semiconductor Manufacturing Company Limited*, No. 2:24-CV-623 (E.D.T.X.)
- *Advanced Integrated Circuit Process LLC, v. United Microelectronics Corporation*, No. 2:24-CV-730 (E.D.T.X.)

On April 15, 2025, Petitioner filed petitions for *inter partes* review of U.S. Patent No. 7,579,277 (IPR2025-00828), U.S. Patent No. 7,923,764 (IPR2025-00829), and U.S. Patent No. 8,587,076 (IPR2025-00831).

C. Notice of Counsel and Service Information

Pursuant to 37 C.F.R. §§42.8(b)(3), 42.8(b)(4) and 42.10(a), Petitioner appoints the following lead and backup counsel:

Lead Counsel	Back Up Counsel
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XX. Conclusion

IPR is respectfully requested.

Respectfully submitted,

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Date: April 15, 2025

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(a), Petitioner hereby certifies that portions of the above-captioned **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 8,253,180**, in accordance with and reliance on the word count provided by the word-processing system used to prepare this Petition, that the number of words in this paper is 13,995. Pursuant to 37 C.F.R. §42.24(a), this word count is in compliance and excludes the table of contents, table of authorities, mandatory notices under §42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing. This word count was prepared using Microsoft Word.

Respectfully submitted,

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Date: April 15, 2025

CERTIFICATE OF SERVICE

The undersigned hereby certifies, in accordance with 37 C.F.R. § 42.105, that the foregoing **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,253,180**, TSMC's Power of Attorney, and all supporting exhibits were served via FedEx Next Business Day Delivery on April 15, 2025, in their entirety on the Patent Owner as detailed below:

Michael J. Cherskov & Szymon M. Gurda
Cherskov, Flaynik & Gurda, LLC
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Courtesy copies have been concurrently served by the electronic mail on Patent Owner's litigation counsel at:

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Date: April 15, 2025

Appendix: Challenged Claims Listing

[1P] A semiconductor device comprising:

[1A] a high dielectric constant gate insulating film formed on an active region in a substrate;

[1B] a gate electrode formed on the high dielectric constant gate insulating film;

[1C] a insulating sidewall formed on each side surface of the gate electrode; and

[1D] wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall, and

[1E] an end of the high dielectric constant gate insulating film under the insulating sidewall is located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode.

[2] The semiconductor device of claim 1, further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film.

[3] The semiconductor device of claim 2, wherein the buffer insulating film is a silicon oxide film.

[4] The semiconductor device of claim 2, wherein the buffer insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall, and an end of the buffer insulating film is located at a

predetermined distance from an outer end of the insulating sidewall toward the gate electrode.

[5] The semiconductor device of claim 1, wherein a smallest thickness of part of the high dielectric constant gate insulating film located under the insulating sidewall is smaller than that of part of the high dielectric constant gate insulating film located under the gate electrode.

[6] The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a Hf based oxide.

[7] The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a HfSiON film.

[8] The semiconductor device of claim 1, wherein

[8A] an extension region of a first conductivity type is formed in part of the active region located under the insulating sidewall, and

[8B] a pocket region of a second conductivity type is formed in part of the active region located under the extension region.

[9] The semiconductor device of claim 8, wherein each of source/drain regions of a first conductivity type is formed in part of the active region located in an external side to the extension region and the pocket region when viewed from the gate electrode.

[10] The semiconductor device of claim 1, wherein a part of the high dielectric constant gate insulating film located under the insulating sidewall includes a notch at the end thereof.

[11] The semiconductor device of claim 1, wherein a part of the high dielectric constant gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.

[12] The semiconductor device of claim 2, wherein an end of the buffer insulating film is located at a predetermined distance from a side end of the gate electrode toward the insulating sidewall.

[13] The semiconductor device of claim 1, wherein the end of the high dielectric constant gate insulating film is located at a predetermined distance from a side end of the gate electrode toward the insulating sidewall.

[14] The semiconductor device of claim 1, wherein the insulating sidewall has a double layer structure including an oxide film and a nitride film.

[15] The semiconductor device of claim 1, wherein wherein *[sic]* the insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film.

[16] The semiconductor device of claim 1, wherein a width of the high dielectric constant gate insulating film along a gate length is larger than a width of the gate electrode along the gate length.

[17] The semiconductor device of claim 1, wherein a width of a bottom surface of the high dielectric constant gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length.

[18] The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more.

[19] The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the insulating sidewall.

[20] The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed to have a convex cross-sectional shape.

[21] The semiconductor device of claim 1, wherein the end of the high dielectric constant gate insulating film located under the insulating sidewall has a tapered surface.

[22] The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof.