EXHIBIT 180-03: Invalidity of U.S. Patent No. 8,253,180 (the ’180 Patent) Based on *Matsumoto 135*

The following list illustrates certain grounds for invalidity based on:

- U.S. Publication 2003/0025135 to Matsumoto (“*Matsumoto 135*”), published February 6, 2003, is prior art to U.S. Patent No. 8,253,180 (the “’180 patent”) under at least pre-AIA 35 U.S.C. §102(b).

Matsumoto 135, including any material incorporated by reference into *Matsumoto 135*, anticipates at least claims 1-3, 5-6, 11, 13-14, 16-19, and 21-22 of the ’180 patent under pre-AIA 35 U.S.C. §102(b).

To the extent any limitation is found not to be expressly or inherently disclosed in *Matsumoto 135*, such a limitation would have been obvious either based on *Matsumoto 135* alone, given the state of the art, or in combination with one or more of the references cited in Exhibits 180-01, 180-02, and 180-04 through 180-15, because the ’180 patent is merely a collection of prior art elements that fails to meet the statutory requirement of non-obviousness under 35 U.S.C. § 103, and the factors delineated in *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), weigh against a finding of non-obviousness.

In particular, any disclosures identified for each limitation of the ’180 patent in the aforementioned Exhibits may be combined with the disclosures of *Matsumoto 135* identified below for the same limitation to render that limitation obvious. A POSITA would have found such a combination / modification obvious for the reasons discussed herein and in Defendant’s cover pleading.[1]

The citations to portions of any reference in this chart are exemplary only. Citations to the written description should be interpreted to include the figures associated with or relevant to the cited passages. Similarly, citations to a figure should be understood to encompass any description, text, or discussion of that figure. Defendant reserves the right to use the entirety of any reference cited in this chart to

[1] Plaintiff appears in many instances to be pursuing overly broad constructions of limitations of the asserted claims in an effort to piece together an infringement claim where none exists. This claim chart accounts for overly broad construction of the claim limitations. Any assertion that a particular limitation is disclosed by a prior art reference or references may be based on Plaintiff’s apparent constructions and is not intended to be, and is not, an admission that such constructions are supportable or proper. Defendant is investigating this prior art and has not yet completed discovery from third parties, who may have relevant information concerning the prior art. Therefore, Defendant reserves the right to supplement this chart after additional discovery is received. To the extent that any of the prior art discloses the same or similar functionality or feature(s) of any of the accused products, Defendant reserves the right to argue that said feature or functionality does not practice any limitation of any of the asserted claims, and to argue, in the alternative, that if said feature or functionality is found to practice any limitation of any of the asserted claims, then the prior art reference teaches the limitation and that the claim is not patentable.

show that the asserted claims are anticipated and/or are obvious. Citations presented for one claim limitation are expressly incorporated by reference into all other limitations for that claim as well as all limitations of all claims on which that claim depends.

U.S. Patent No. 8,253,180	**Exemplary Disclosures Relevant to *Matsumoto 135***
Claim 1	
[1pre] A semiconductor device comprising:	*Matsumoto 135*, alone or in combination with one or more references, discloses or suggests a semiconductor device. For example, *Matsumoto 135* discloses the following at Title: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SAME *Matsumoto 135* discloses the following at Abstract: A semiconductor device which achieves reductions in malfunctions and operating characteristic variations by reducing the gain of a parasitic bipolar transistor, and a method of manufacturing the same are provided. *Matsumoto 135* discloses the following at claims 1, 10, 13: A semiconductor device comprising: ... *Matsumoto 135* discloses the following at ¶ 2: The present invention relates to a semiconductor device and a method of manufacturing the same. More particularly, the invention relates to a MOSFET (Metal Oxide Semiconductor Field Effect Transistor) employing an SOI (Silicon-On-Insulator) substrate and a method of manufacturing the same. *Matsumoto 135* discloses the following at ¶ 13:

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	It is an object of the present invention to provide a semiconductor device which achieves reductions in malfunctions and operating characteristic variations by reducing the gain of a parasitic bipolar transistor, and a method of manufacturing the same. *Matsumoto 135* discloses the following at ¶ 14: According to a first aspect of the present invention, the semiconductor device includes an SOI substrate, a first insulation film, a gate electrode, a pair of second insulation films, a pair of third insulation films, a body region, and a pair of source/drain regions. *See also, e.g., Matsumoto 135* at ¶¶ 15-46, 60, 62, 64, 68-69. *Matsumoto 135* discloses the following at ¶¶ 77 and 102: FIG. 1 is a sectional view showing a structure of a semiconductor device according to a first preferred embodiment of the present invention *Matsumoto 135* discloses the following at ¶ 137: FIGS. 18 through 22 are sectional views showing a method of manufacturing a semiconductor device in a step-by-step manner according to a fourth preferred embodiment of the present invention. *See also, e.g., Matsumoto 135* at ¶¶ 79-82, 85-86.
[1A] a high dielectric constant gate insulating film formed on an active region in a substrate;	*Matsumoto 135*, alone or in combination with one or more references, discloses or suggests a high dielectric constant gate insulating film formed on an active region in a substrate. For example:

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	Matsumoto 135 discloses the following at Abstract: A silicon oxide film (6) is formed partially on the upper surface of a silicon layer (3). A gate electrode (7) of polysilicon is formed partially on the silicon oxide film (6). A portion of the silicon oxide film (6) underlying the gate electrode (7) functions as a gate insulation film. A silicon nitride film (9) is formed on each side surface of the gate electrode (7), with a silicon oxide film (8) therebetween. *Matsumoto 135* discloses the following at claim 1: an SOI substrate having a multi-layer structure including a semiconductor substrate, an insulation layer and a semiconductor layer stacked in the order named; a first insulation film formed on a main surface of said semiconductor layer; *Matsumoto 135* discloses the following at claim 10: a substrate having a first region with a digital circuit formed therein, and a second region with an analog or RF (radio frequency) circuit formed therein; a first semiconductor element formed in said first region and constituting said digital circuit; and a second semiconductor element formed in said second region and constituting said analog or RF circuit, said first semiconductor element including a first gate electrode formed on a main surface of said substrate, with a first gate insulation film therebetween, …

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	said second semiconductor element including a second gate electrode formed on said main surface of said substrate, with a second gate insulation film therebetween, *Matsumoto 135* discloses the following at claim 13: a substrate; a semiconductor element including (a) a gate electrode formed on a main surface of said substrate, with a gate insulation film therebetween, and extending in a predetermined direction, (b) *Matsumoto 135* discloses the following at ¶ 14: According to a first aspect of the present invention, the semiconductor device includes an SOI substrate, a first insulation film, a gate electrode, a pair of second insulation films, a pair of third insulation films, a body region, and a pair of source/drain regions. The SOI substrate has a multi-layer structure including a semiconductor substrate, an insulation layer and a semiconductor layer stacked in the order named. The first insulation film is formed on a main surface of the semiconductor layer. The gate electrode is formed on the first insulation film. *Matsumoto 135* discloses the following at ¶¶ 102-103: FIG. 1 is a sectional view showing a structure of a semiconductor device according to a first preferred embodiment of the present invention An SOI substrate 4 has a multi-layer structure such that a silicon substrate 1, a BOX layer 2 and a single-crystalline silicon layer 3 are stacked in the order named. The single-crystalline silicon layer 3 may be replaced with a polycrystalline or amorphous silicon layer. A completely isolating insulation film 5 made of silicon oxide is partially formed in the silicon layer

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	3. The isolating insulation film 5 extends from the upper surface of the silicon layer 3 to the upper surface of the BOX layer 2. A MOSFET is formed in a device region defined by the isolating insulation film 5 in a manner to be specifically described below. A silicon oxide film 6 is formed partially on the upper surface of the silicon layer 3. A gate electrode 7 made of polysilicon is formed partially on the silicon oxide film 6. A portion of the silicon oxide film 6 which lies under the gate electrode 7 functions as a gate insulation film. *Matsumoto 135* discloses the following at ¶ 105: A pair of source/ drain regions 10 are formed in the silicon layer 3. A region between the pair of source/drain regions 10 is defined as a body region 12. Each of the source/drain regions 10 has an extension (or LDD when having a relatively low impurity concentration) 11 extending from under the outer side surface of a corresponding one of the silicon oxide films 8 toward the body region 12 in the upper surface of the silicon layer 3. *Matsumoto 135* discloses the following at ¶ 107: FIGS. 3 through 12 are sectional views showing a method of manufacturing the semiconductor device shown in FIG. 2 in a step-by-step manner. Referring first to FIG. 3, the SOI substrate 4 is prepared, and then the isolating insulation film 5 are formed in the silicon layer 3. Next, a silicon oxide film 13 is formed entirely on the upper surface of the silicon layer 3 and the upper surface of the isolating insulation film 5 by a CVD process or a thermal oxidation process. A silicon oxynitride film, a metal oxide film such as Al_2O_3 or a ferroelectric film such as Ta_2O_5 and BST may be formed in place of the silicon oxide film 13. *Matsumoto 135* discloses the following at ¶¶ 137-138:

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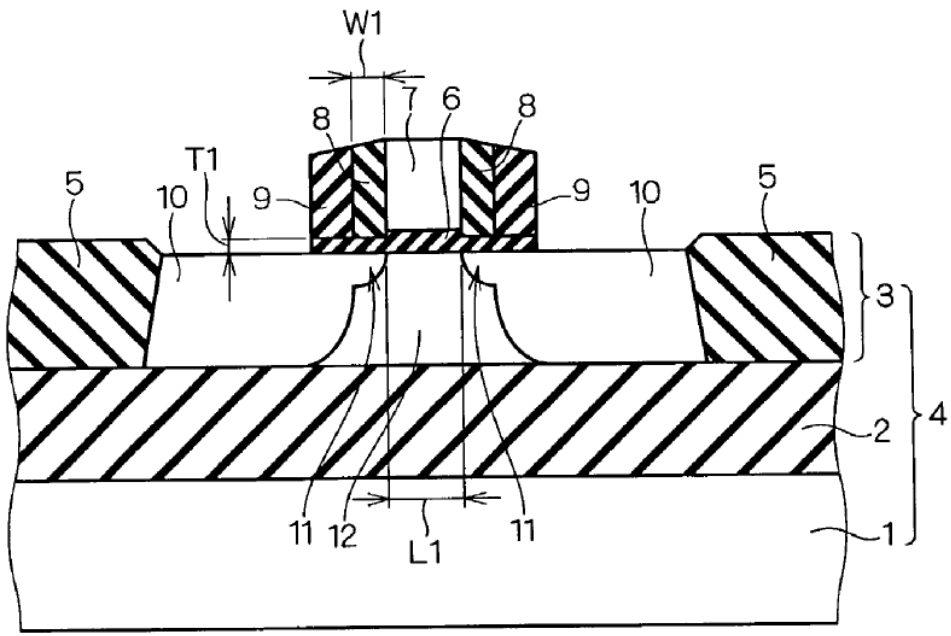
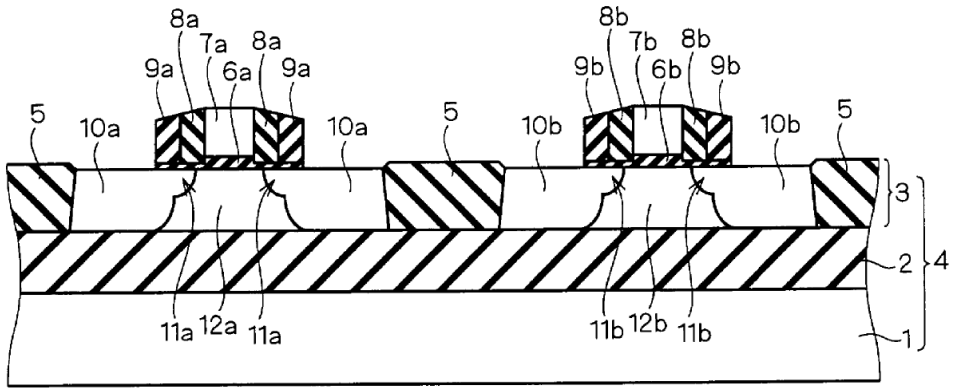
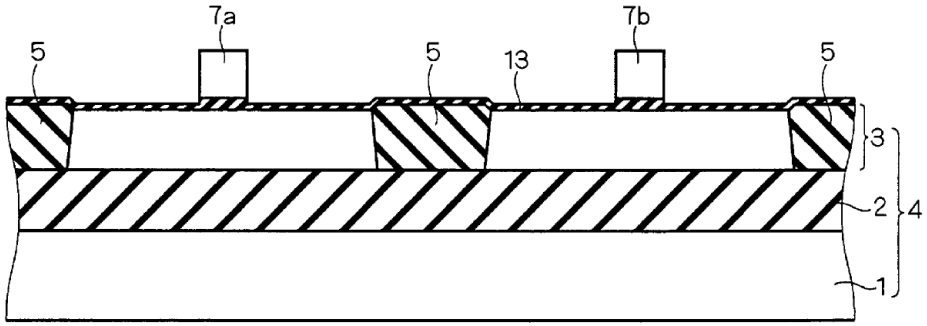
	FIGS. 18 through 22 are sectional views showing a method of manufacturing a semiconductor device in a step-by-step manner according to a fourth preferred embodiment of the present invention. Referring first to FIG. 18, the gate electrode 7 is formed by the process described in the first preferred embodiment, and thereafter the silicon oxide film 16 is formed on the entire top surface of the resultant structure by a CVD process. Referring to FIG. 19, the silicon oxide film 16 is etched by an anisotropic dry etching process which exhibits a higher etch rate in the direction of depth of the SOI substrate 4. This forms the silicon oxide films 8 on the side surfaces of the gate electrode 7. The anisotropic dry etching process for formation of the silicon oxide films 8 is continued to overetch the upper surface of the silicon layer 3 exposed by the etching of the silicon oxide film 16. The etching causes damages to create defects in the upper surface of the silicon layer 3. *Matsumoto 135* discloses the following at ¶ 140: In the method of manufacturing the semiconductor device according to the fourth preferred embodiment, as discussed above, the etching process for the formation of the silicon oxide films 8 etches the upper surface of the silicon layer 3 as well to create defects in the upper surface of the silicon layer 3. As a result, the defects act as lifetime killers for the parasitic bipolar transistor to reduce the gain of the parasitic bipolar transistor. The technique of the fourth preferred embodiment is applicable to any one of the first to third preferred embodiments. *Matsumoto 135* discloses the following at ¶ 167: With reference to FIG. 31, a silicon oxide film is formed entirely on the upper surface of the silicon layer 3 and the upper surfaces of the isolating insulation films 30, 50 by a CVD process or a thermal oxidation process. A silicon oxynitride film, a metal oxide

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	film such as Al_2O_3 or a ferroelectric film such as Ta_2O_5 and BST may be formed in place of the silicon oxide film. *See also, e.g., Matsumoto 135* at ¶¶ 32 ("a first gate electrode formed on a main surface of the substrate, with a first gate insulation film therebetween" and "a second gate electrode formed on the main surface of the substrate, with a second gate insulation film therebetween"), 38, 64. *Matsumoto 135* discloses the following at Figures 1, 2, 4, 10, 13, 19-26: F I G . 1 

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	F I G . 2  F I G . 4 

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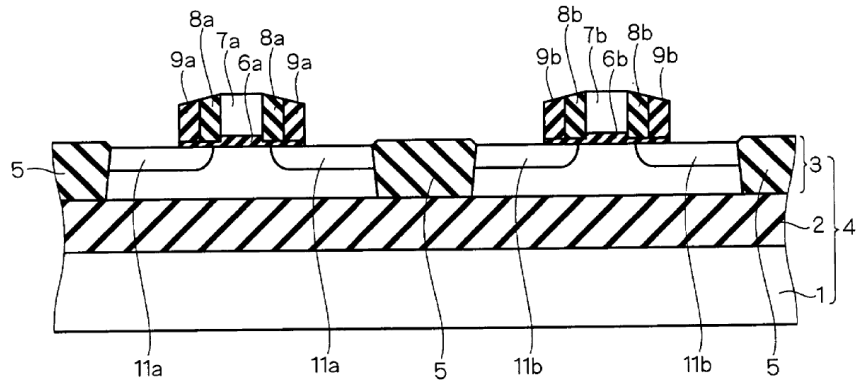
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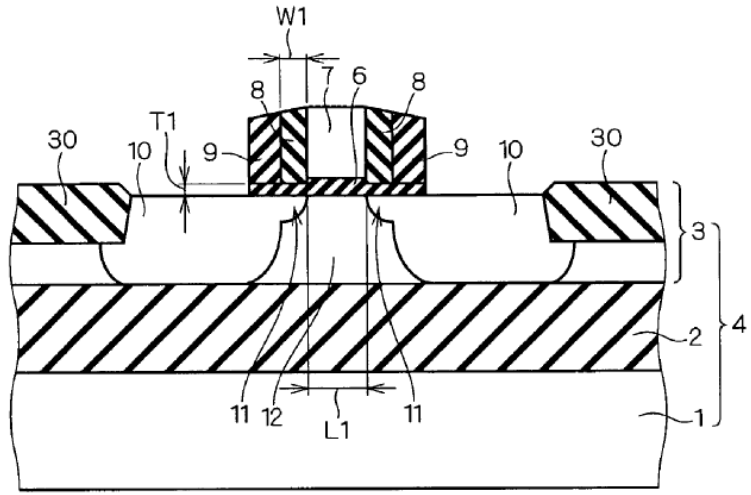
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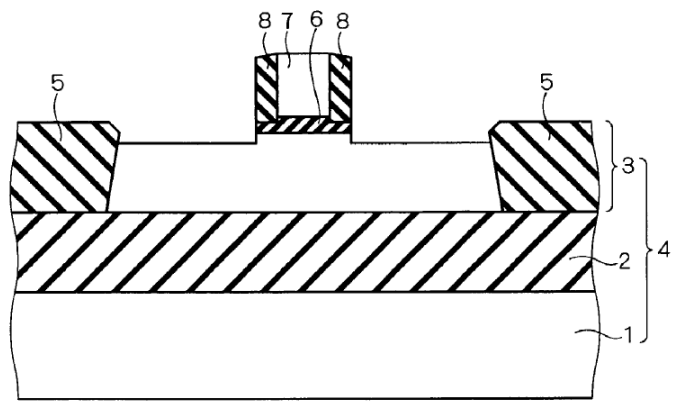
U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	FIG. 19 

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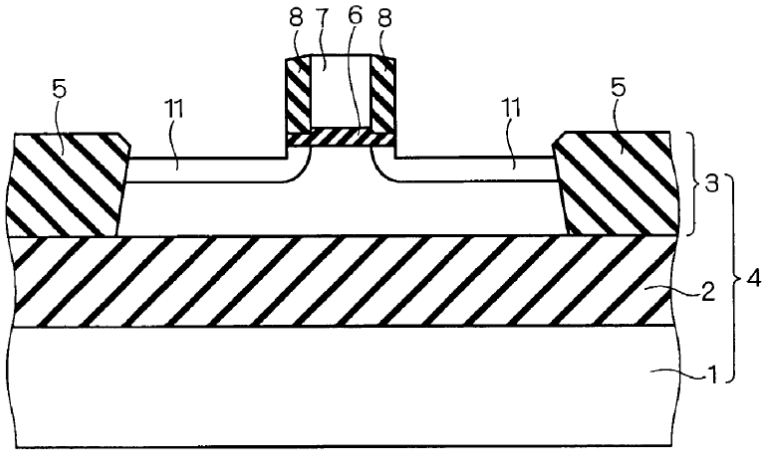

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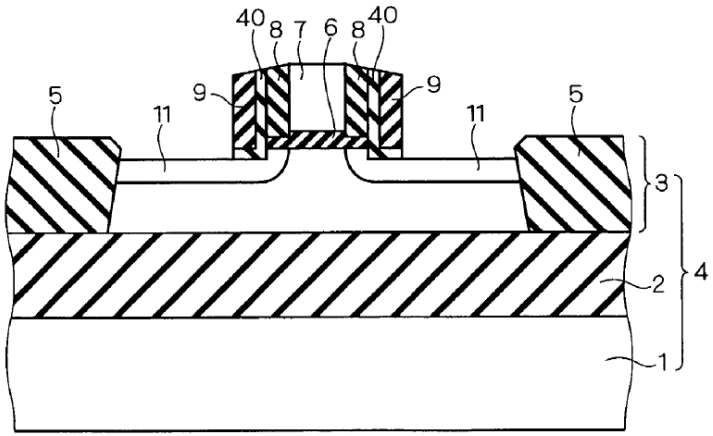


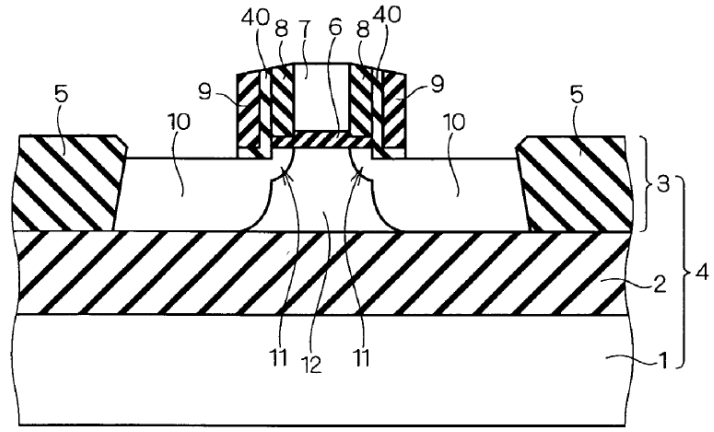
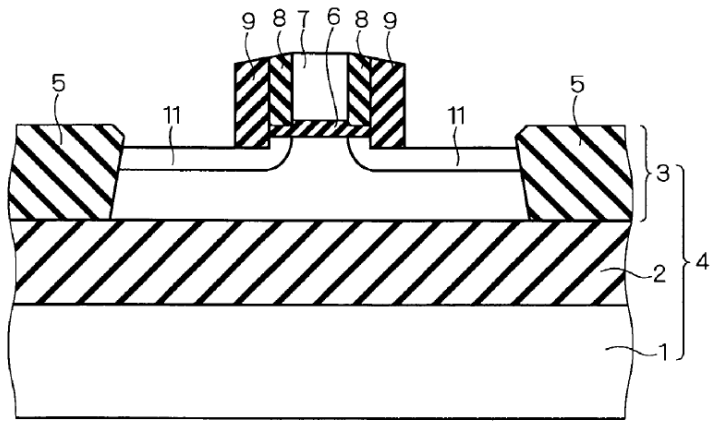
	FIG. 22  FIG. 23 

FIG. 24

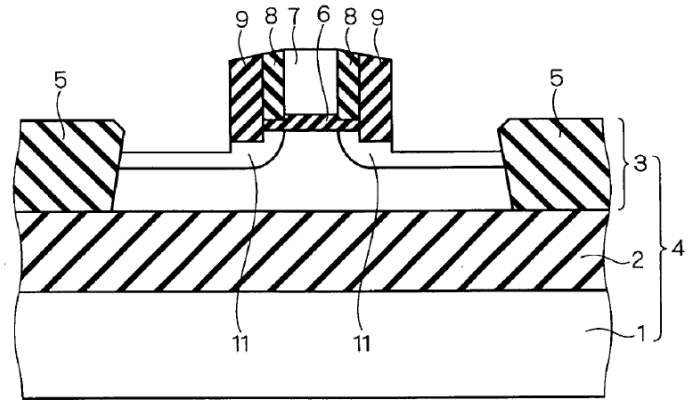
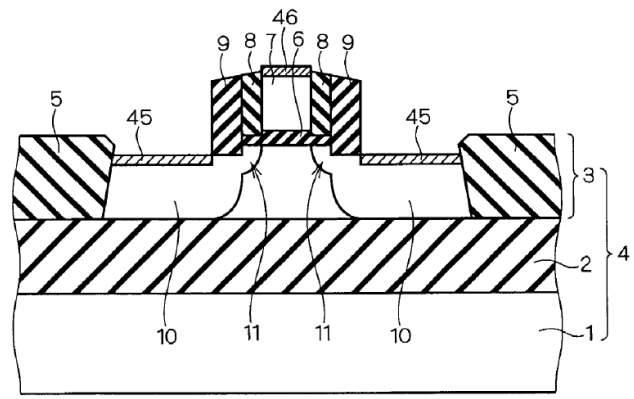
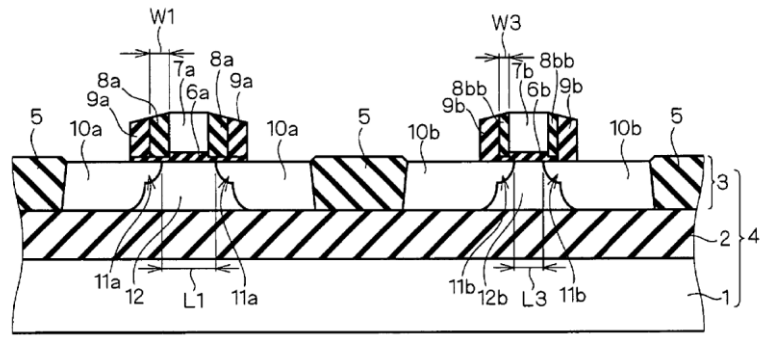


FIG. 25



U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	F I G . 2 6 
[1B] a gate electrode formed on the high dielectric constant gate insulating film;	*Matsumoto 135*, alone or in combination with one or more references, discloses or suggests a gate electrode formed on the high dielectric constant gate insulating film. For example: *Matsumoto 135* discloses the following at Abstract: > A silicon oxide film (6) is formed partially on the upper surface of a silicon layer (3). A gate electrode (7) of polysilicon is formed partially on the silicon oxide film (6). A portion of the silicon oxide film (6) underlying the gate electrode (7) functions as a gate insulation film. A silicon nitride film (9) is formed on each side surface of the gate electrode (7), with a silicon oxide film (8) therebetween. *Matsumoto 135* discloses the following at claim 1:

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	an SOI substrate having a multi-layer structure including a semiconductor substrate, an insulation layer and a semiconductor layer stacked in the order named; a first insulation film formed on a main surface of said semiconductor layer; a gate electrode formed on said first insulation film; *Matsumoto 135* discloses the following at claim 10: a substrate having a first region with a digital circuit formed therein, and a second region with an analog or RF (radio frequency) circuit formed therein; a first semiconductor element formed in said first region and constituting said digital circuit; and a second semiconductor element formed in said second region and constituting said analog or RF circuit, said first semiconductor element including a first gate electrode formed on a main surface of said substrate, with a first gate insulation film therebetween, … said second semiconductor element including a second gate electrode formed on said main surface of said substrate, with a second gate insulation film therebetween, *Matsumoto 135* discloses the following at claim 13: a substrate;

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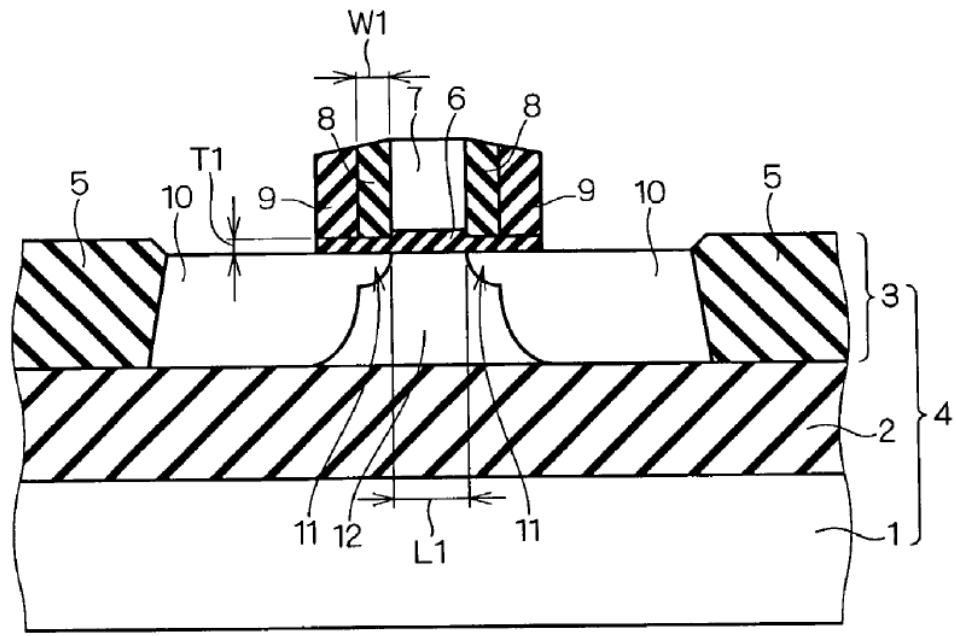
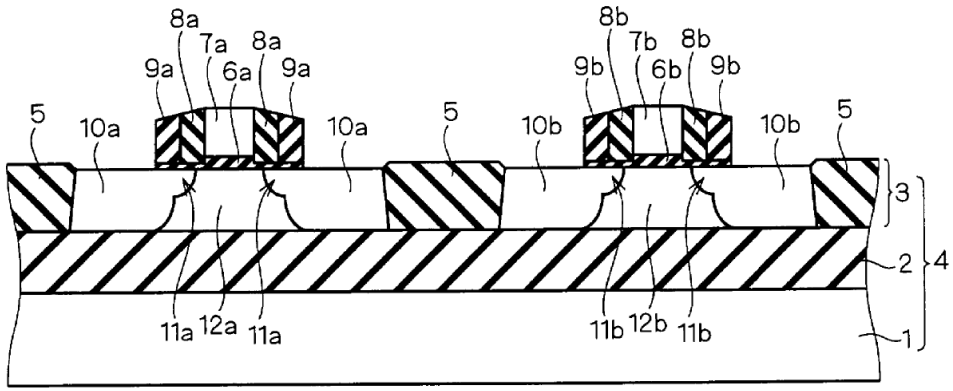
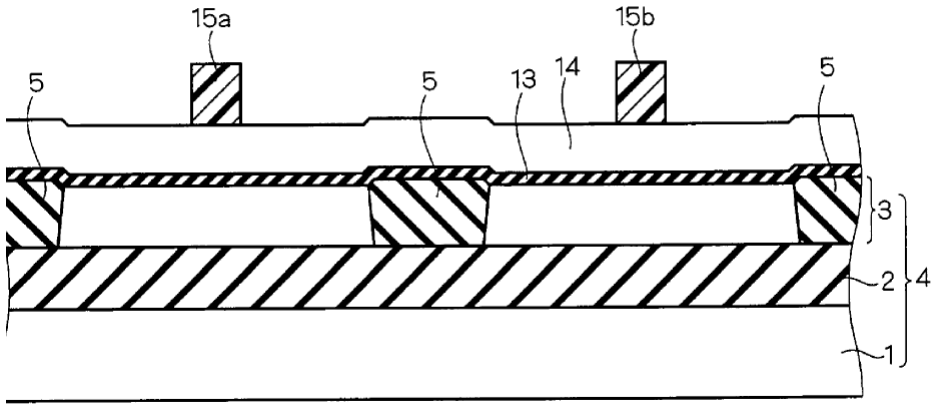
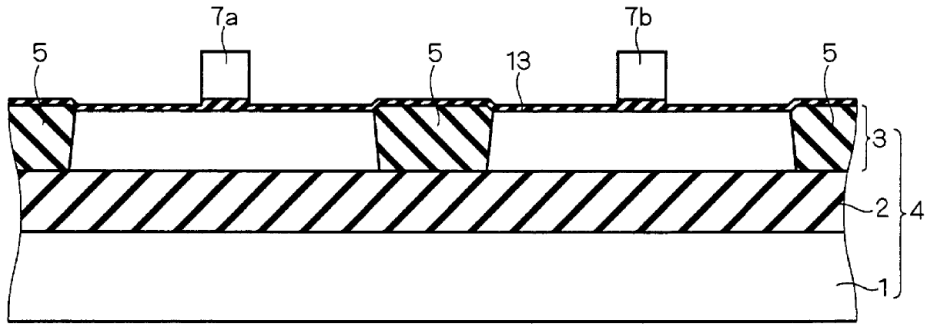
	a semiconductor element including (a) a gate electrode formed on a main surface of said substrate, with a gate insulation film therebetween, and extending in a predetermined direction, (b) *Matsumoto 135* discloses the following at ¶ 103: A MOSFET is formed in a device region defined by the isolating insulation film 5 in a manner to be specifically described below. A silicon oxide film 6 is formed partially on the upper surface of the silicon layer 3. A gate electrode 7 made of polysilicon is formed partially on the silicon oxide film 6. *Matsumoto 135* discloses the following at ¶¶ 107-108: FIGS. 3 through 12 are sectional views showing a method of manufacturing the semiconductor device shown in FIG. 2 in a step-by-step manner. Referring first to FIG. 3, the SOI substrate 4 is prepared, and then the isolating insulation film 5 are formed in the silicon layer 3. Next, a silicon oxide film 13 is formed entirely on the upper surface of the silicon layer 3 and the upper surface of the isolating insulation film 5 by a CVD process or a thermal oxidation process. A silicon oxynitride film, a metal oxide film such as Al_2O_3 or a ferroelectric film such as Ta_2O_5 and BST may be formed in place of the silicon oxide film 13. Next, a polysilicon film 14 having a thickness of about 100 nm to about 400 nm is formed entirely on the upper surface of the silicon oxide film 13 by an LPCVD process. The polysilicon film 14 may be doped with an impurity such as P and B. A metal film such as W, Ta and Al may be formed in place of the polysilicon film 14. Next, photoresists 15*a* and 15*b* are formed partially on the upper surface of the polysilicon film 14 by a photolithographic process. The photoresists 15*a* and 15*b* are formed over regions in which respective gate electrodes 7*a* and 7*b* are to be formed. With reference to FIG. 4, using the photoresists 15*a* and 15*b* as an etch mask, an anisotropic dry etching process, such as RIE (Reactive Ion Etching) or ECR (Electron Cyclotron Resonance), which exhibits a higher etch rate in a direction of depth of the

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	SOI substrate 4 is performed to etch the polysilicon film 14. This leaves unetched portions of the polysilicon film 14 which lie under the photoresists 15*a* and 15*b* to form the gate electrodes 7*a* and 7*b*. This anisotropic dry etching process slightly etches the upper surface of the silicon oxide film 13. Thereafter, the photoresists 15*a* and 15*b* are removed. The gate electrodes 7*a* and 7*b* may be formed by another technique of forming an insulation film on the upper surface of the polysilicon film 14, patterning the insulation film by a photolithographic process and an etching process, and anisotropically etching the polysilicon film 14 using the patterned insulation film as a hard mask. *Matsumoto 135* discloses the following at ¶¶ 137-138: FIGS. 18 through 22 are sectional views showing a method of manufacturing a semiconductor device in a step-by-step manner according to a fourth preferred embodiment of the present invention. Referring first to FIG. 18, the gate electrode 7 is formed by the process described in the first preferred embodiment, and thereafter the silicon oxide film 16 is formed on the entire top surface of the resultant structure by a CVD process. Referring to FIG. 19, the silicon oxide film 16 is etched by an anisotropic dry etching process which exhibits a higher etch rate in the direction of depth of the SOI substrate 4. This forms the silicon oxide films 8 on the side surfaces of the gate electrode 7. The anisotropic dry etching process for formation of the silicon oxide films 8 is continued to overetch the upper surface of the silicon layer 3 exposed by the etching of the silicon oxide film 16. The etching causes damages to create defects in the upper surface of the silicon layer 3. *Matsumoto 135* discloses the following at Figures 1-4, 10, 13, 19-26:

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	F I G . 1 

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	FIG. 2  FIG. 3 

F I G . 4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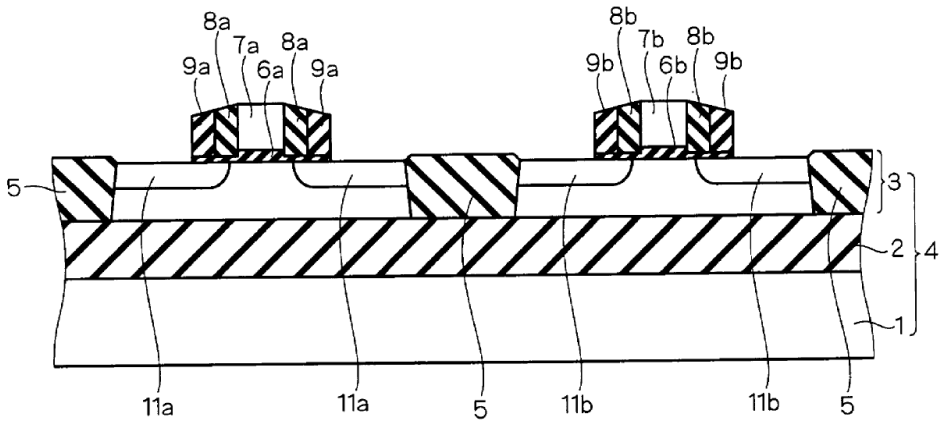
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9a
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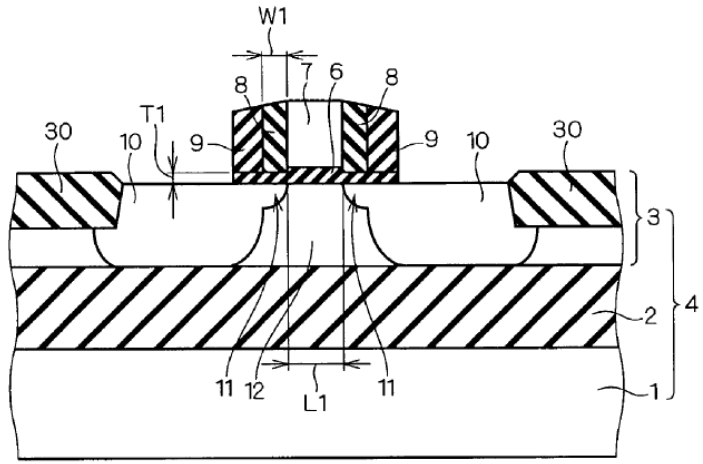
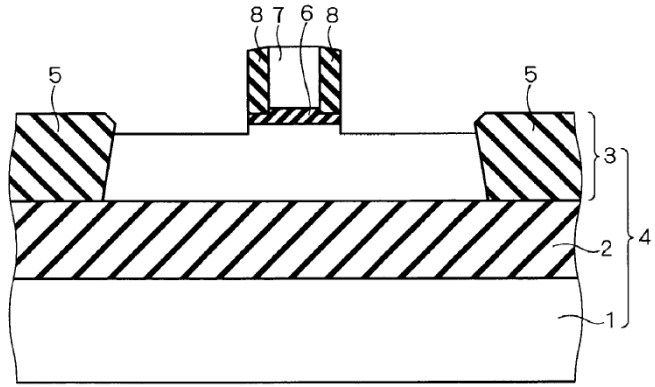
U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	FIG. 13  FIG. 19 

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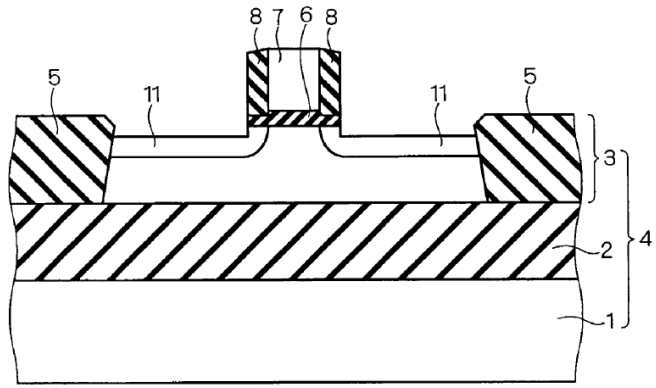

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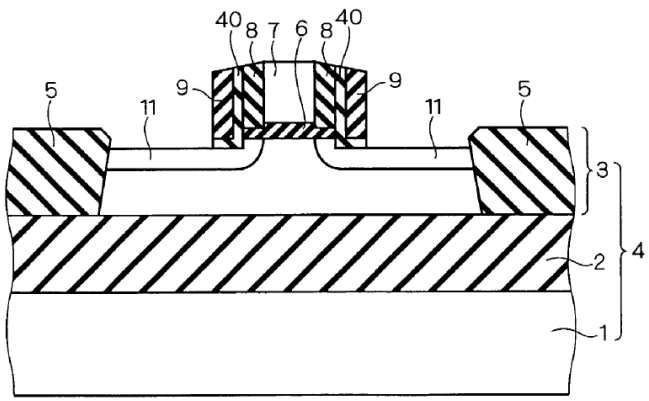
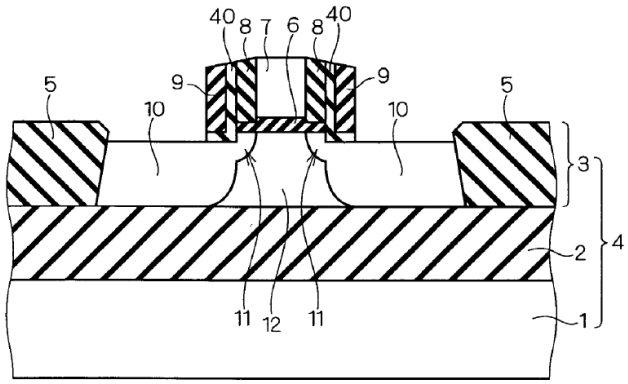
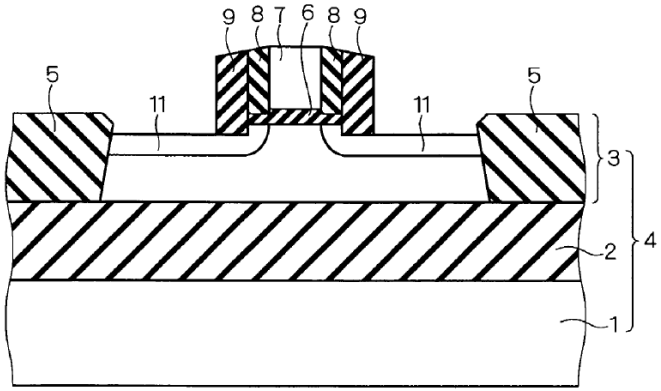
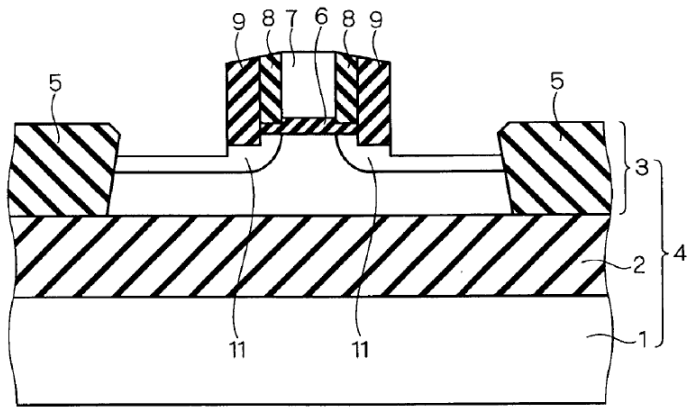
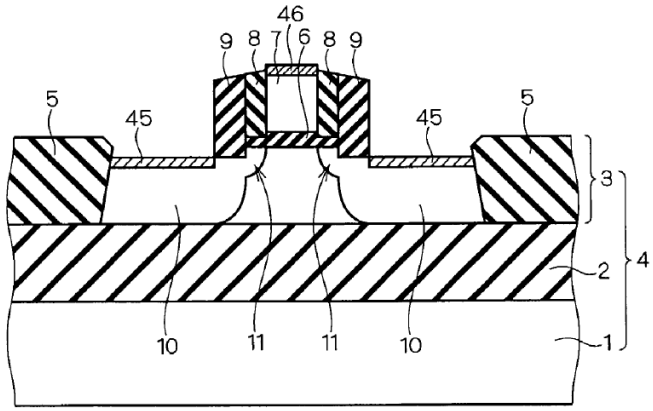
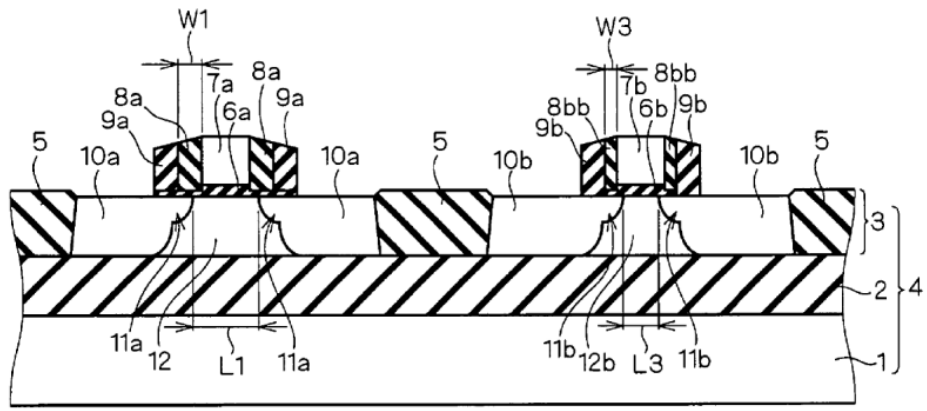


U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	FIG. 22  FIG. 23 

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	FIG. 24  FIG. 25 

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	F I G . 2 6 
[1C] a insulating sidewall formed on each side surface of the gate electrode; and	*Matsumoto 135*, alone or in combination with one or more references, discloses or suggests an insulating sidewall formed on each side surface of the gate electrode. For example: *Matsumoto 135* discloses the following at Abstract: > A silicon nitride film (9) is formed on each side surface of the gate electrode (7), with a silicon oxide film (8) therebetween. The silicon oxide film (8) and the silicon nitride film (9) are formed on the silicon oxide film (6). The width (W1) of the silicon oxide film (8) in a direction of the gate length is greater than the thickness (T1) of the silicon oxide film (6).

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	Matsumoto 135 discloses the following at claim 1: a pair of second insulation films having respective inner side surfaces in contact with side surfaces of said gate electrode and respective outer side surfaces out of contact with said side surfaces of said gate electrode, with said gate electrode disposed between said pair of second insulation films; a pair of third insulation films formed on said main surface of said semiconductor layer, with said first insulation film therebetween, and having respective inner side surfaces in contact with said outer side surfaces of said second insulation films and respective outer side surfaces out of contact with said outer side surfaces of said second insulation films, with said gate electrode and said second insulation films disposed between said pair of third insulation films; *Matsumoto 135* discloses the following at claim 11: said first semiconductor element further includes a first sidewall formed on a side surface of said first gate electrode; and said second semiconductor element further includes a first insulation film formed on a side surface of said second gate electrode, and a second sidewall formed on said side surface of said second gate electrode, with said first insulation film therebetween. *Matsumoto 135* discloses the following at claim 13: a semiconductor element including (a) a gate electrode formed on a main surface of said substrate, with a gate insulation film therebetween, and extending in a

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	predetermined direction, (b) a first sidewall formed on a side surface of said gate electrode, *Matsumoto 135* discloses the following at claim 14: The semiconductor device according to claim 13, further comprising a second sidewall formed on said side surface of said gate electrode, with said first sidewall therebetween. *Matsumoto 135* discloses the following at ¶ 34: Preferably, in the semiconductor device, the first semiconductor element further includes a first sidewall formed on a side surface of the first gate electrode. The second semiconductor element further includes a first insulation film formed on a side surface of the second gate electrode, and a second sidewall formed on the side surface of the second gate electrode, with the first insulation film therebetween. *Matsumoto 135* discloses the following at ¶ 38: The semiconductor element includes (a) a gate electrode formed on a main surface of the substrate, with a gate insulation film therebetween, and extending in a predetermined direction, (b) a first sidewall formed on a side surface of the gate electrode, ... *Matsumoto 135* discloses the following at ¶ 40: Preferably, the semiconductor device further includes a second sidewall formed on the side surface of the gate electrode, with the first sidewall therebetween. *Matsumoto 135* discloses the following at ¶ 64:

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	The step (d) is to form a first sidewall on a side surface of the first gate electrode, and a second sidewall on the side surface of the second gate electrode, with the first insulation film therebetween. *Matsumoto 135* discloses the following at ¶¶ 103-104: A silicon nitride film 9 is formed on each side surface of the gate electrode 7, with a silicon oxide film 8 therebetween. The silicon oxide film 8 and the silicon nitride film 9 are formed on the silicon oxide film 6. The width W1 of the silicon oxide film 8 in a direction of the gate length (or in the lateral direction as viewed in the drawing) is greater than the thickness T1 of the silicon oxide film 6. Side surfaces of the silicon oxide films 8 which are in contact with the side surfaces of the gate electrode 7 are herein defined as "inner side surfaces," and side surfaces thereof which are out of contact with the side surfaces of the gate electrodes 7 are defined as "outer side surfaces." Side surfaces of the silicon nitride films 9 which are in contact with the outer side surfaces of the silicon oxide films 8 are herein defined as "inner side surfaces," and side surfaces thereof which are out of contact with the outer side surfaces of the silicon oxide films 8 are defined as "outer side surfaces." *Matsumoto 135* discloses the following at ¶¶ 109-110: Next, referring to FIG. 5, a silicon oxide film 16 is formed on the entire top surface of the resultant structure by a CVD process or a thermal oxidation process. An HTO film, an LTO film, a TEOS film or a plasma oxide film may be formed in place of the silicon oxide film 16. Referring to FIG. 6, the silicon oxide film 16 is etched by an anisotropic dry etching process which exhibits a higher etch rate in the direction of depth of the SOI substrate 4. This forms silicon oxide films 8*a* and 8*b* on the side surfaces of the gate electrodes 7*a* and 7*b*. In this process, etching may be stopped before the upper surface of the

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	silicon oxide film 13 and the upper surfaces of the gate electrodes 7*a* and 7*b* are exposed, so that the silicon oxide film 16 is left thin on the upper surface of the silicon oxide film 13 and the upper surfaces of the gate electrodes 7*a* and 7*b*. *Matsumoto 135* discloses the following at ¶ 114: Referring to FIG. 9, after the photoresist 19 is removed, a silicon nitride film 21 is formed on the entire top surface of the resultant structure by a CVD process. With reference to FIG. 10, an anisotropic dry etching process which exhibits a higher etch rate in the direction of depth of the SOI substrate 4 is performed to etch the silicon nitride film 21 and the silicon oxide film 13 in the order named until the upper surface of the silicon layer 3 is exposed. This forms silicon nitride films 9*a* and 9*b* serving as sidewall insulation films on the outer side surfaces of the silicon oxide films 8*a* and 8*b*. The silicon nitride films 9*a* and 9*b* are formed on the silicon oxide films 6*a* and 6*b*. *Matsumoto 135* discloses the following at ¶¶ 137-141: Referring first to FIG. 18, the gate electrode 7 is formed by the process described in the first preferred embodiment, and thereafter the silicon oxide film 16 is formed on the entire top surface of the resultant structure by a CVD process. Referring to FIG. 19, the silicon oxide film 16 is etched by an anisotropic dry etching process which exhibits a higher etch rate in the direction of depth of the SOI substrate 4. This forms the silicon oxide films 8 on the side surfaces of the gate electrode 7. The anisotropic dry etching process for formation of the silicon oxide films 8 is continued to overetch the upper surface of the silicon layer 3 exposed by the etching of the silicon oxide film 16. The etching causes damages to create defects in the upper surface of the silicon layer 3. With reference to FIG. 20, the extensions 11 are formed in the upper surface of the silicon layer 3 by an ion implantation process. Referring to FIG. 21, a silicon oxide film and a silicon nitride film are formed in the order named on the entire top surface of the resultant structure by a CVD

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	process. Next, an anisotropic dry etching process which exhibits a higher etch rate in the direction of depth of the SOI substrate 4 is performed to etch the silicon oxide film and the silicon nitride film until the upper surface of the silicon layer 3 is exposed. This forms silicon oxide films 40 and the silicon nitride films 9 on the outer side surfaces of the silicon oxide films 8. Referring to FIG. 22, the source/drain regions 10 are formed in the silicon layer 3 by an ion implantation process. In the method of manufacturing the semiconductor device according to the fourth preferred embodiment, as discussed above, the etching process for the formation of the silicon oxide films 8 etches the upper surface of the silicon layer 3 as well to create defects in the upper surface of the silicon layer 3. As a result, the defects act as lifetime killers for the parasitic bipolar transistor to reduce the gain of the parasitic bipolar transistor. The technique of the fourth preferred embodiment is applicable to any one of the first to third preferred embodiments. FIG. 23 is a sectional view showing a first modification of the method of manufacturing the semiconductor device according to the fourth preferred embodiment. The silicon nitride films 9 shown in FIG. 21 are formed on the upper surface of the silicon layer 3, with the silicon oxide films 40 therebetween. In the first modification of the fourth preferred embodiment, on the other hand, the silicon nitride films 9 are formed directly on the upper surface of the silicon layer 3. The technique of the first modification of the fourth preferred embodiment is applicable to any one of the first to fourth preferred embodiments. *Matsumoto 135* discloses the following at ¶ 143: FIG. 24 is a sectional view showing a second modification of the method of manufacturing the semiconductor device according to the fourth preferred embodiment. The anisotropic dry etching process for the formation of the silicon nitride films 9 in the technique shown in FIGS. 22 and 23 is stopped when the upper surface of the silicon layer 3 is exposed. In the second modification of the fourth preferred embodiment, on the other hand, the anisotropic dry etching process for the formation of the silicon nitride films 9 overetches the upper surface of the

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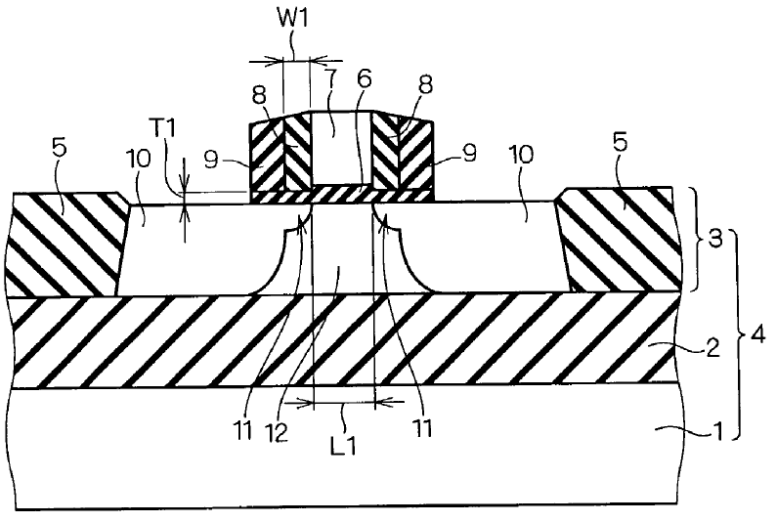
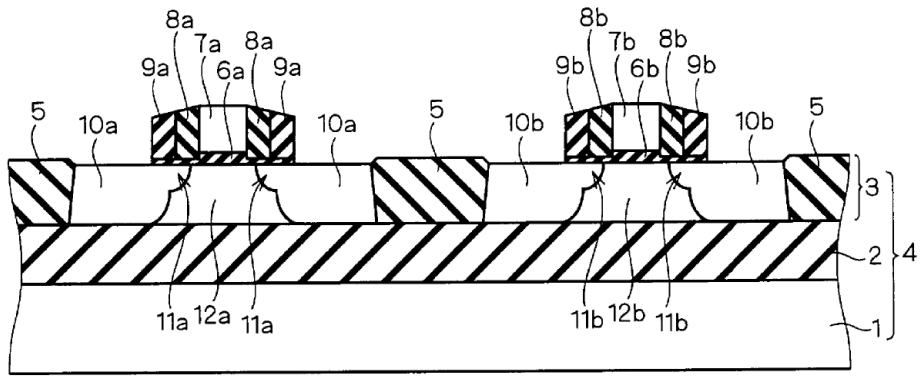
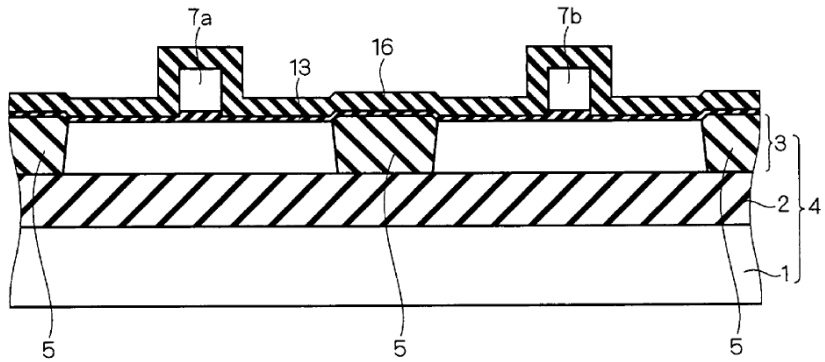
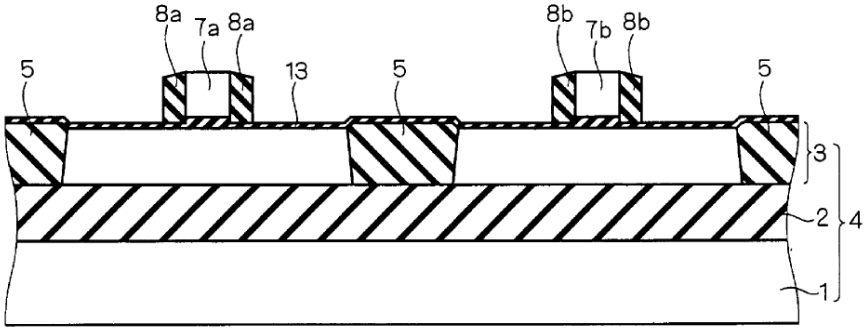
	silicon layer 3 as well. The technique of the second modification of the fourth preferred embodiment is applicable to any one of the first to fourth preferred embodiments and the first modification of the fourth preferred embodiment. *Matsumoto 135* discloses the following at Figures 1-2, 5-6, 9-10, 13, 19-26: F I G . 1 

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	FIG. 2  FIG. 5 

F I G . 6


8a
7a
8a
8b
7b
8b
5
13
5
5
3
2
4
1

F I G . 9

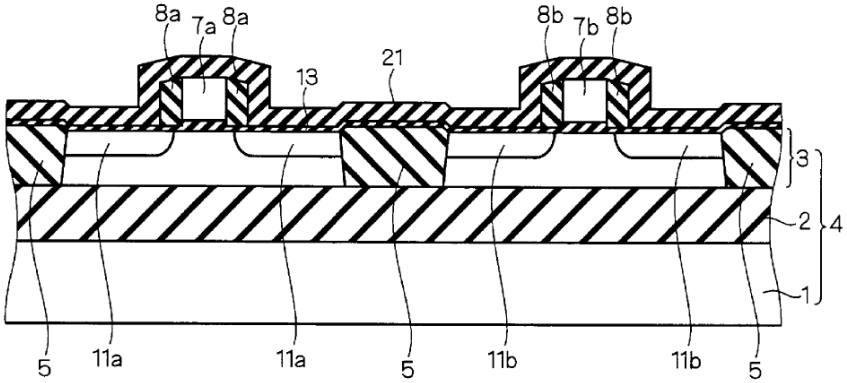

8a
7a
8a
8b
7b
8b
13
21
3
2
4
1
5
11a
11a
5
11b
11b
5

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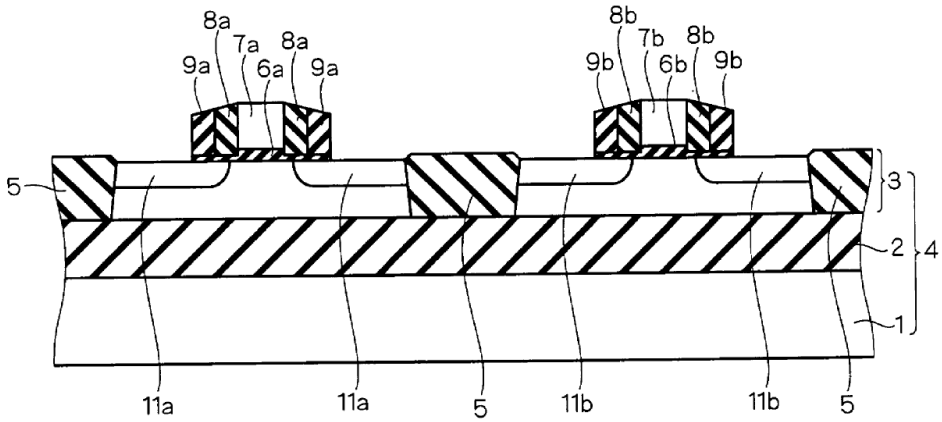
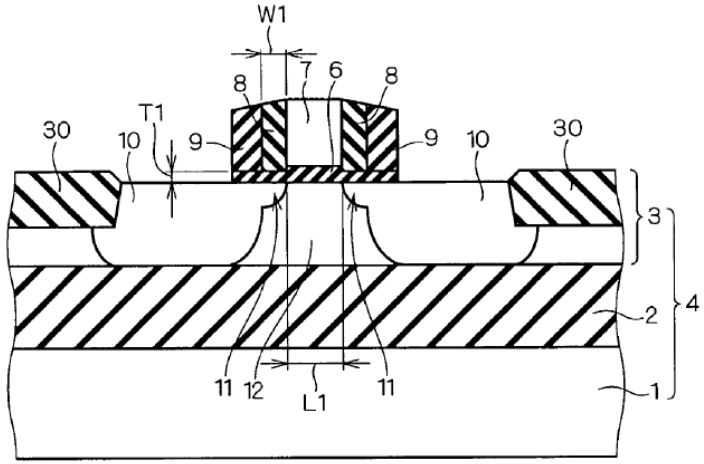
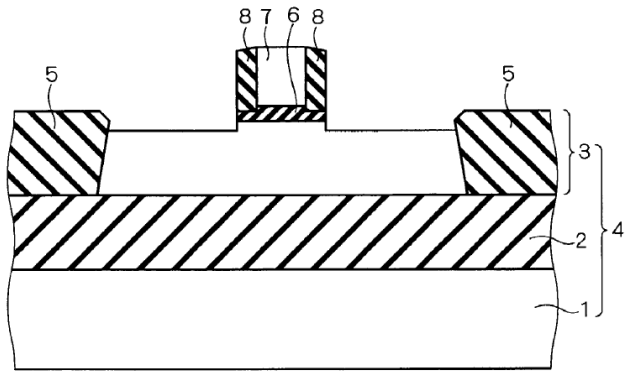
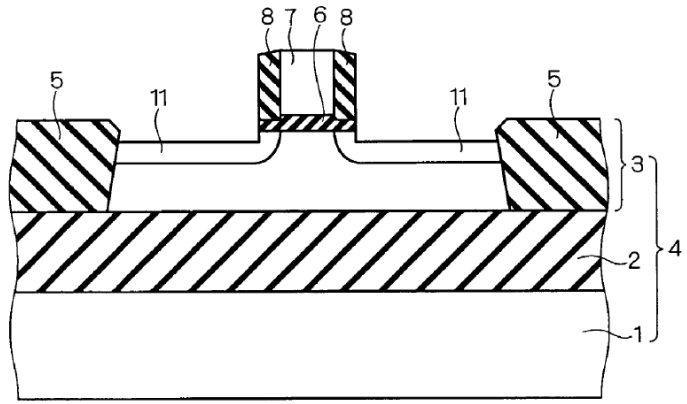
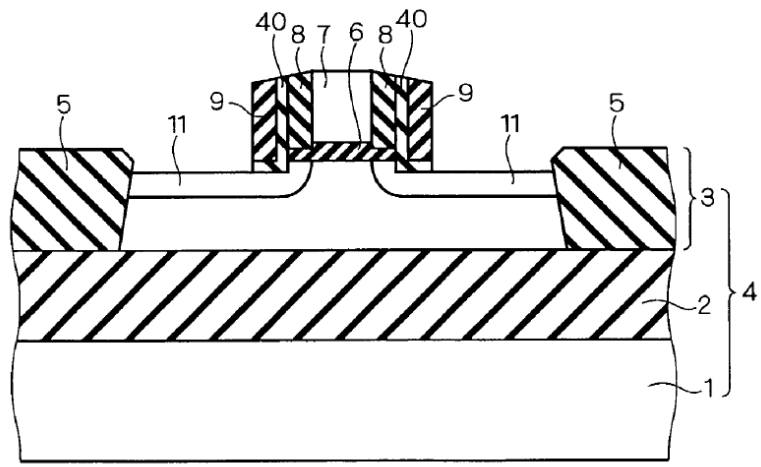
	FIG. 10  FIG. 13 

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	FIG. 19 

F I G . 2 0



F I G . 2 1



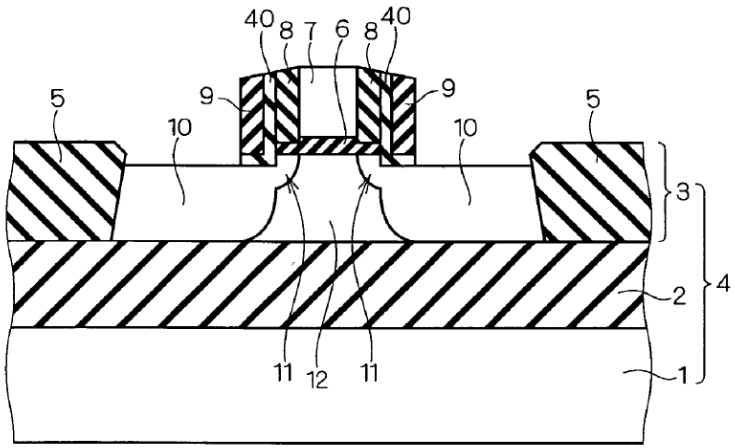
U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	FIG. 22 

FIG. 23

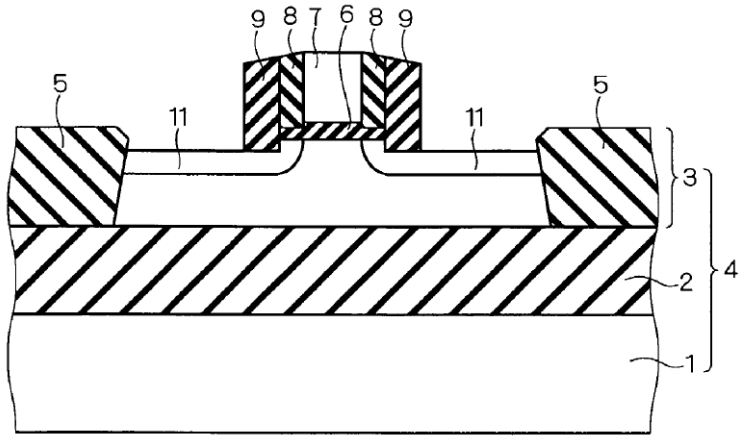


FIG. 24

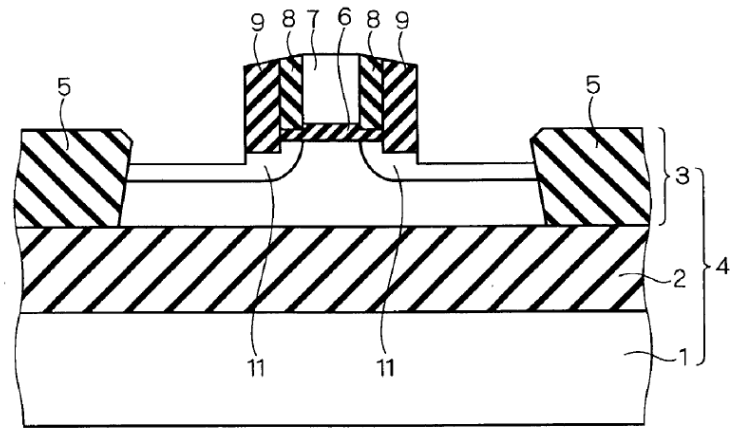


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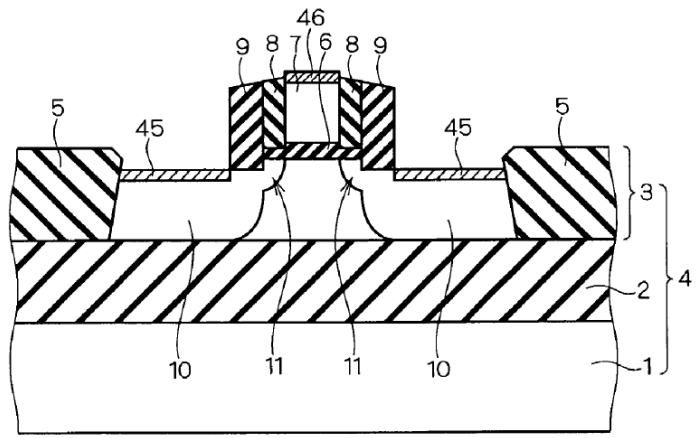
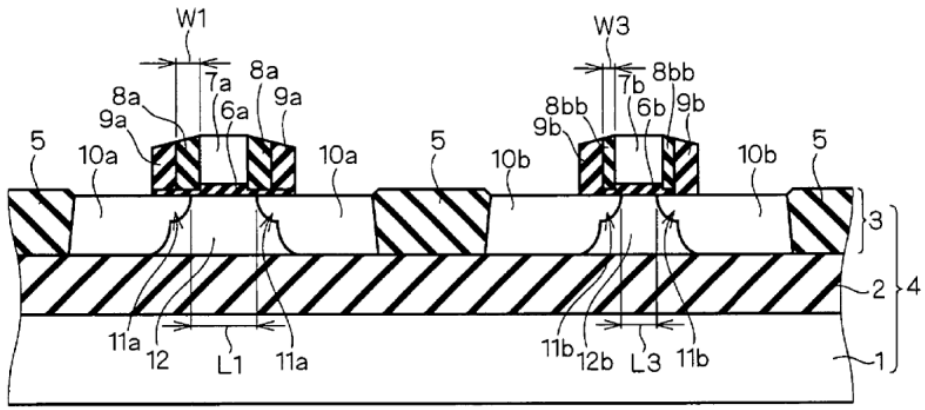
	FIG. 25  FIG. 26 

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[1D] wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall, and	*Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall. For example: *See* limitation [1C], *supra*. *Matsumoto 135* discloses the following at ¶ 103: > A MOSFET is formed in a device region defined by the isolating insulation film 5 in a manner to be specifically described below. A silicon oxide film 6 is formed partially on the upper surface of the silicon layer 3. A gate electrode 7 made of polysilicon is formed partially on the silicon oxide film 6. A portion of the silicon oxide film 6 which lies under the gate electrode 7 functions as a gate insulation film. A silicon nitride film 9 is formed on each side surface of the gate electrode 7, with a silicon oxide film 8 therebetween. The silicon oxide film 8 and the silicon nitride film 9 are formed on the silicon oxide film 6. *Matsumoto 135* discloses the following at ¶¶ 107-108: > Next, a polysilicon film 14 having a thickness of about 100 nm to about 400 nm is formed entirely on the upper surface of the silicon oxide film 13 by an LPCVD process. The polysilicon film 14 may be doped with an impurity such as P and B. A metal film such as W, Ta and Al may be formed in place of the polysilicon film 14. Next, photoresists 15*a* and 15*b* are formed partially on the upper surface of the polysilicon film 14 by a photolithographic process. The photoresists 15*a* and 15*b* are formed over regions in which respective gate electrodes 7*a* and 7*b* are to be formed. > With reference to FIG. 4, using the photoresists 15*a* and 15*b* as an etch mask, an anisotropic dry etching process, such as RIE (Reactive Ion Etching) or ECR (Electron Cyclotron Resonance), which exhibits a higher etch rate in a direction of depth of the

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	SOI substrate 4 is performed to etch the polysilicon film 14. This leaves unetched portions of the polysilicon film 14 which lie under the photoresists 15*a* and 15*b* to form the gate electrodes 7*a* and 7*b*. This anisotropic dry etching process slightly etches the upper surface of the silicon oxide film 13. Thereafter, the photoresists 15*a* and 15*b* are removed. The gate electrodes 7*a* and 7*b* may be formed by another technique of forming an insulation film on the upper surface of the polysilicon film 14, patterning the insulation film by a photolithographic process and an etching process, and anisotropically etching the polysilicon film 14 using the patterned insulation film as a hard mask. *Matsumoto 135* discloses the following at ¶¶ 137-140: Referring first to FIG. 18, the gate electrode 7 is formed by the process described in the first preferred embodiment, and thereafter the silicon oxide film 16 is formed on the entire top surface of the resultant structure by a CVD process. Referring to FIG. 19, the silicon oxide film 16 is etched by an anisotropic dry etching process which exhibits a higher etch rate in the direction of depth of the SOI substrate 4. This forms the silicon oxide films 8 on the side surfaces of the gate electrode 7. The anisotropic dry etching process for formation of the silicon oxide films 8 is continued to overetch the upper surface of the silicon layer 3 exposed by the etching of the silicon oxide film 16. The etching causes damages to create defects in the upper surface of the silicon layer 3. With reference to FIG. 20, the extensions 11 are formed in the upper surface of the silicon layer 3 by an ion implantation process. Referring to FIG. 21, a silicon oxide film and a silicon nitride film are formed in the order named on the entire top surface of the resultant structure by a CVD process. Next, an anisotropic dry etching process which exhibits a higher etch rate in the direction of depth of the SOI substrate 4 is performed to etch the silicon oxide film and the silicon nitride film until the upper surface of the silicon layer 3 is exposed. This forms silicon oxide films 40 and the silicon nitride films

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	9 on the outer side surfaces of the silicon oxide films 8. Referring to FIG. 22, the source/drain regions 10 are formed in the silicon layer 3 by an ion implantation process. In the method of manufacturing the semiconductor device according to the fourth preferred embodiment, as discussed above, the etching process for the formation of the silicon oxide films 8 etches the upper surface of the silicon layer 3 as well to create defects in the upper surface of the silicon layer 3.
[1E] an end of the high dielectric constant gate insulating film under the insulating sidewall is located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode.	*Matsumoto 135*, alone or in combination with one or more references, discloses or suggests an end of the high dielectric constant gate insulating film under the insulating sidewall is located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode. For example, *Matsumoto 135* discloses the following at ¶¶ 137-141: Referring first to FIG. 18, the gate electrode 7 is formed by the process described in the first preferred embodiment, and thereafter the silicon oxide film 16 is formed on the entire top surface of the resultant structure by a CVD process. Referring to FIG. 19, the silicon oxide film 16 is etched by an anisotropic dry etching process which exhibits a higher etch rate in the direction of depth of the SOI substrate 4. This forms the silicon oxide films 8 on the side surfaces of the gate electrode 7. The anisotropic dry etching process for formation of the silicon oxide films 8 is continued to overetch the upper surface of the silicon layer 3 exposed by the etching of the silicon oxide film 16. The etching causes damages to create defects in the upper surface of the silicon layer 3. With reference to FIG. 20, the extensions 11 are formed in the upper surface of the silicon layer 3 by an ion implantation process. Referring to FIG. 21, a silicon oxide film and a silicon nitride film are formed in the order named on the entire top surface of the resultant structure by a CVD process. Next, an anisotropic dry etching process which exhibits a higher etch rate in the direction of depth of the SOI substrate 4 is performed

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	to etch the silicon oxide film and the silicon nitride film until the upper surface of the silicon layer 3 is exposed. This forms silicon oxide films 40 and the silicon nitride films 9 on the outer side surfaces of the silicon oxide films 8. Referring to FIG. 22, the source/drain regions 10 are formed in the silicon layer 3 by an ion implantation process. In the method of manufacturing the semiconductor device according to the fourth preferred embodiment, as discussed above, the etching process for the formation of the silicon oxide films 8 etches the upper surface of the silicon layer 3 as well to create defects in the upper surface of the silicon layer 3. As a result, the defects act as lifetime killers for the parasitic bipolar transistor to reduce the gain of the parasitic bipolar transistor. The technique of the fourth preferred embodiment is applicable to any one of the first to third preferred embodiments. FIG. 23 is a sectional view showing a first modification of the method of manufacturing the semiconductor device according to the fourth preferred embodiment. The silicon nitride films 9 shown in FIG. 21 are formed on the upper surface of the silicon layer 3, with the silicon oxide films 40 therebetween. In the first modification of the fourth preferred embodiment, on the other hand, the silicon nitride films 9 are formed directly on the upper surface of the silicon layer 3. The technique of the first modification of the fourth preferred embodiment is applicable to any one of the first to fourth preferred embodiments. *Matsumoto 135* discloses the following at ¶ 143: FIG. 24 is a sectional view showing a second modification of the method of manufacturing the semiconductor device according to the fourth preferred embodiment. The anisotropic dry etching process for the formation of the silicon nitride films 9 in the technique shown in FIGS. 22 and 23 is stopped when the upper surface of the silicon layer 3 is exposed. In the second modification of the fourth preferred embodiment, on the other hand, the anisotropic dry etching process for the formation of the silicon nitride films 9 overetches the upper surface of the silicon layer 3 as well. The technique

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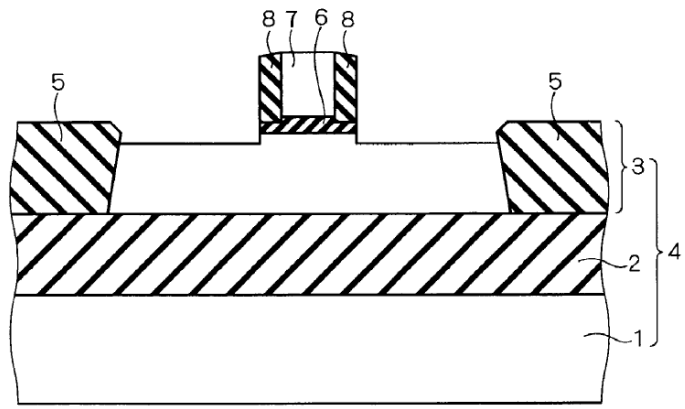
	of the second modification of the fourth preferred embodiment is applicable to any one of the first to fourth preferred embodiments and the first modification of the fourth preferred embodiment. *Matsumoto 135* discloses the following at Figures 19-26: F I G . 1 9 

FIG. 20

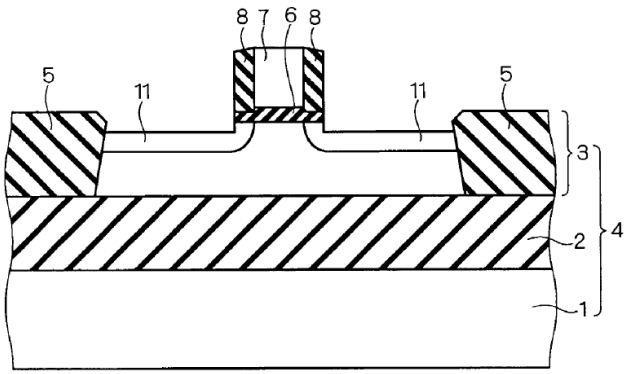


FIG. 21

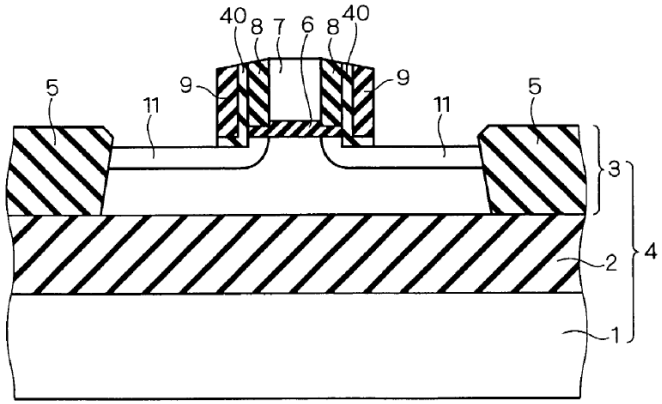
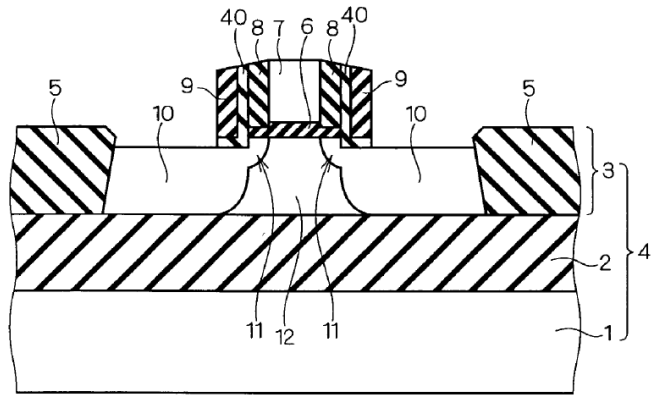
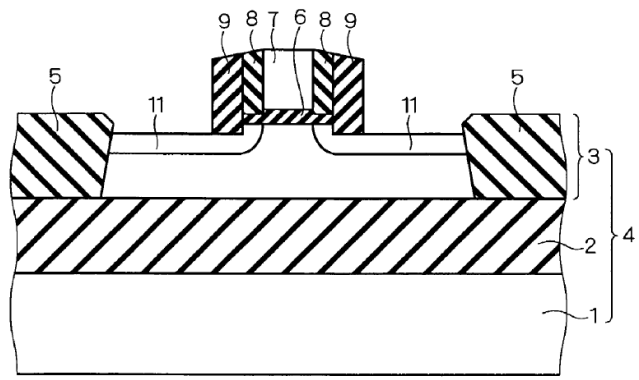
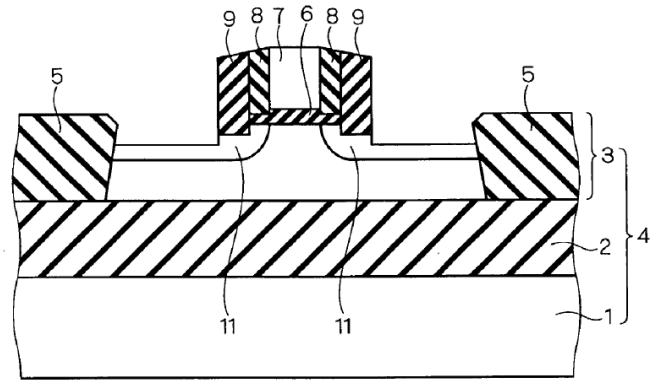
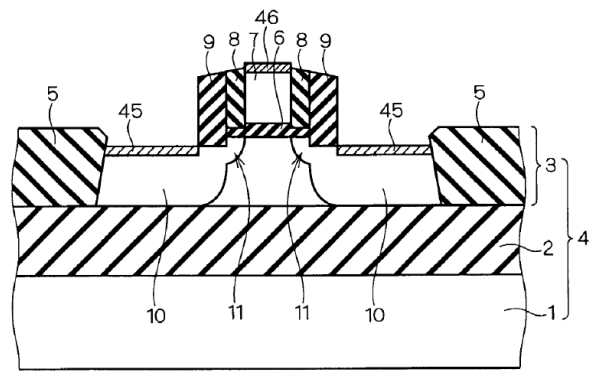
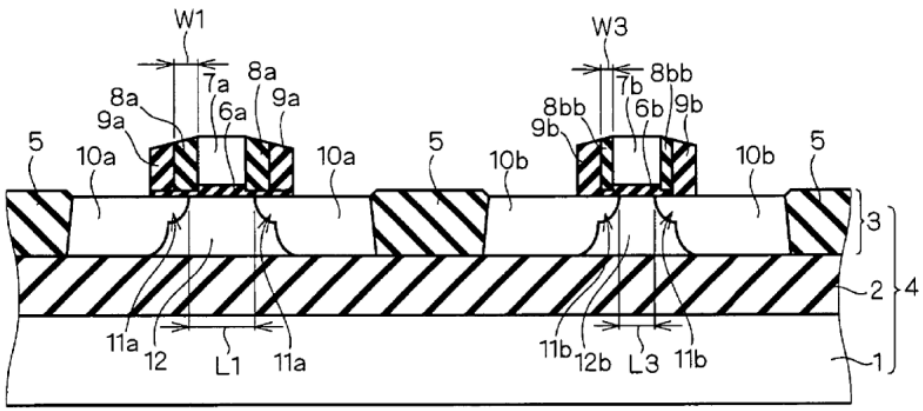


	FIG. 22  FIG. 23 

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	FIG. 24  FIG. 25 

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	F I G . 2 6  *See also* limitations 1[C] and 1[D], *supra*.
Claim 2	
2. The semiconductor device of claim 1, further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film.	*Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Matsumoto 135*, alone or in combination with one or more references, discloses or suggests a buffer insulating film between the substrate and the high dielectric constant gate insulating film.

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
Claim 3	
3. The semiconductor device of claim 2, wherein the buffer insulating film is a silicon oxide film.	*Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 2. *See* claim 2, *supra*. *Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the buffer insulating film is a silicon oxide film.
Claim 5	
5. The semiconductor device of claim 1, wherein a smallest thickness of part of the high dielectric constant gate insulating film located under the insulating sidewall is smaller than that of part of the high dielectric constant gate insulating film located under the gate electrode.	*Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Matsumoto 135*, alone or in combination with one or more references, discloses or suggests a smallest thickness of part of the high dielectric constant gate insulating film located under the insulating sidewall is smaller than that of part of the high dielectric constant gate insulating film located under the gate electrode. *See* limitations 1[B], 1[C], 1[D], *supra*. *Matsumoto 135* discloses the following at ¶¶ 107-108: > FIGS. 3 through 12 are sectional views showing a method of manufacturing the semiconductor device shown in FIG. 2 in a step-by-step manner. Referring first to FIG. 3, the SOI substrate 4 is prepared, and then the isolating insulation film 5 are formed in the silicon layer 3. Next, a silicon oxide film 13 is formed entirely on the upper surface of the silicon layer 3 and the upper surface of the isolating insulation film 5 by a CVD process or a thermal oxidation process. A silicon oxynitride film, a metal oxide film such as Al_2O_3 or a ferroelectric film such as Ta_2O_5 and BST may be formed in place of the silicon oxide film 13. Next, a polysilicon film 14 having a thickness of about 100 nm to about 400 nm is formed entirely on the upper surface of the silicon oxide film 13 by an LPCVD process. The polysilicon film 14 may be doped with an impurity such as

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	P and B. A metal film such as W, Ta and Al may be formed in place of the polysilicon film 14. Next, photoresists 15*a* and 15*b* are formed partially on the upper surface of the polysilicon film 14 by a photolithographic process. The photoresists 15*a* and 15*b* are formed over regions in which respective gate electrodes 7*a* and 7*b* are to be formed. With reference to FIG. 4, using the photoresists 15*a* and 15*b* as an etch mask, an anisotropic dry etching process, such as RIE (Reactive Ion Etching) or ECR (Electron Cyclotron Resonance), which exhibits a higher etch rate in a direction of depth of the SOI substrate 4 is performed to etch the polysilicon film 14. This leaves unetched portions of the polysilicon film 14 which lie under the photoresists 15*a* and 15*b* to form the gate electrodes 7*a* and 7*b*. This anisotropic dry etching process slightly etches the upper surface of the silicon oxide film 13. Thereafter, the photoresists 15*a* and 15*b* are removed. The gate electrodes 7*a* and 7*b* may be formed by another technique of forming an insulation film on the upper surface of the polysilicon film 14, patterning the insulation film by a photolithographic process and an etching process, and anisotropically etching the polysilicon film 14 using the patterned insulation film as a hard mask. *Matsumoto 135* discloses the following at ¶¶ 137-140: Referring first to FIG. 18, the gate electrode 7 is formed by the process described in the first preferred embodiment, and thereafter the silicon oxide film 16 is formed on the entire top surface of the resultant structure by a CVD process. Referring to FIG. 19, the silicon oxide film 16 is etched by an anisotropic dry etching process which exhibits a higher etch rate in the direction of depth of the SOI substrate 4. This forms the silicon oxide films 8 on the side surfaces of the gate electrode 7. The anisotropic dry etching process for formation of the silicon oxide films 8 is continued to overetch the upper surface of the silicon layer 3 exposed by the etching of the silicon oxide film 16. The etching causes damages to create defects in the upper surface of the silicon layer 3.

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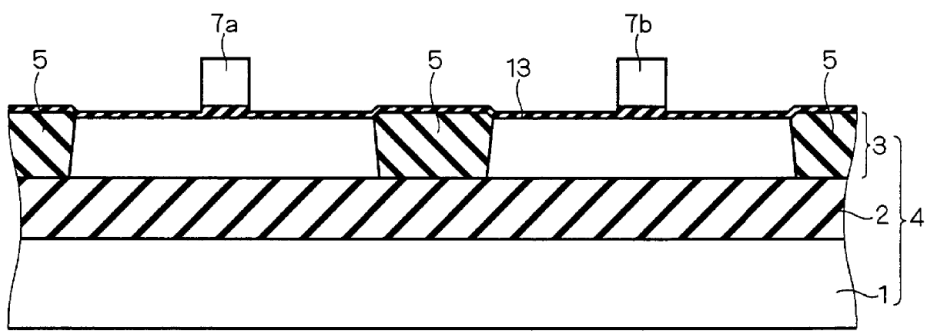
	With reference to FIG. 20, the extensions 11 are formed in the upper surface of the silicon layer 3 by an ion implantation process. Referring to FIG. 21, a silicon oxide film and a silicon nitride film are formed in the order named on the entire top surface of the resultant structure by a CVD process. Next, an anisotropic dry etching process which exhibits a higher etch rate in the direction of depth of the SOI substrate 4 is performed to etch the silicon oxide film and the silicon nitride film until the upper surface of the silicon layer 3 is exposed. This forms silicon oxide films 40 and the silicon nitride films 9 on the outer side surfaces of the silicon oxide films 8. Referring to FIG. 22, the source/drain regions 10 are formed in the silicon layer 3 by an ion implantation process. In the method of manufacturing the semiconductor device according to the fourth preferred embodiment, as discussed above, the etching process for the formation of the silicon oxide films 8 etches the upper surface of the silicon layer 3 as well to create defects in the upper surface of the silicon layer 3. *Matsumoto 135* discloses the following at Figure 4: F I G . 4 

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Claim 6	
6. The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a Hf based oxide.	*Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the high dielectric constant gate insulating film is formed of a Hf based oxide.
Claim 11	
11. The semiconductor device of claim 1, wherein a part of the high dielectric constant gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.	*Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Matsumoto 135*, alone or in combination with one or more references, discloses or suggests a part of the high dielectric constant gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.
Claim 13	
13. The semiconductor device of claim 1, wherein the end of the high dielectric constant gate insulating film is located at a predetermined distance from a side end of the gate electrode toward the insulating sidewall.	*Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the end of the high dielectric constant gate insulating film is located at a predetermined distance from a side end of the gate electrode toward the insulating sidewall. For example, *Matsumoto 135* discloses the following at ¶¶ 137-141: > Referring first to FIG. 18, the gate electrode 7 is formed by the process described in the first preferred embodiment, and thereafter the silicon oxide film 16 is formed on the entire top surface of the resultant structure by a CVD process.

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	Referring to FIG. 19, the silicon oxide film 16 is etched by an anisotropic dry etching process which exhibits a higher etch rate in the direction of depth of the SOI substrate 4. This forms the silicon oxide films 8 on the side surfaces of the gate electrode 7. The anisotropic dry etching process for formation of the silicon oxide films 8 is continued to overetch the upper surface of the silicon layer 3 exposed by the etching of the silicon oxide film 16. The etching causes damages to create defects in the upper surface of the silicon layer 3. With reference to FIG. 20, the extensions 11 are formed in the upper surface of the silicon layer 3 by an ion implantation process. Referring to FIG. 21, a silicon oxide film and a silicon nitride film are formed in the order named on the entire top surface of the resultant structure by a CVD process. Next, an anisotropic dry etching process which exhibits a higher etch rate in the direction of depth of the SOI substrate 4 is performed to etch the silicon oxide film and the silicon nitride film until the upper surface of the silicon layer 3 is exposed. This forms silicon oxide films 40 and the silicon nitride films 9 on the outer side surfaces of the silicon oxide films 8. Referring to FIG. 22, the source/drain regions 10 are formed in the silicon layer 3 by an ion implantation process. In the method of manufacturing the semiconductor device according to the fourth preferred embodiment, as discussed above, the etching process for the formation of the silicon oxide films 8 etches the upper surface of the silicon layer 3 as well to create defects in the upper surface of the silicon layer 3. As a result, the defects act as lifetime killers for the parasitic bipolar transistor to reduce the gain of the parasitic bipolar transistor. The technique of the fourth preferred embodiment is applicable to any one of the first to third preferred embodiments. FIG. 23 is a sectional view showing a first modification of the method of manufacturing the semiconductor device according to the fourth preferred embodiment. The silicon nitride films 9 shown in FIG. 21 are formed on the upper surface of the silicon layer 3, with the silicon oxide films 40 therebetween. In the first modification of the fourth preferred embodiment, on the other hand, the silicon nitride films 9 are formed directly

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	on the upper surface of the silicon layer 3. The technique of the first modification of the fourth preferred embodiment is applicable to any one of the first to fourth preferred embodiments. *Matsumoto 135* discloses the following at ¶ 143: FIG. 24 is a sectional view showing a second modification of the method of manufacturing the semiconductor device according to the fourth preferred embodiment. The anisotropic dry etching process for the formation of the silicon nitride films 9 in the technique shown in FIGS. 22 and 23 is stopped when the upper surface of the silicon layer 3 is exposed. In the second modification of the fourth preferred embodiment, on the other hand, the anisotropic dry etching process for the formation of the silicon nitride films 9 overetches the upper surface of the silicon layer 3 as well. The technique of the second modification of the fourth preferred embodiment is applicable to any one of the first to fourth preferred embodiments and the first modification of the fourth preferred embodiment. *Matsumoto 135* discloses the following at Figures 19-26:

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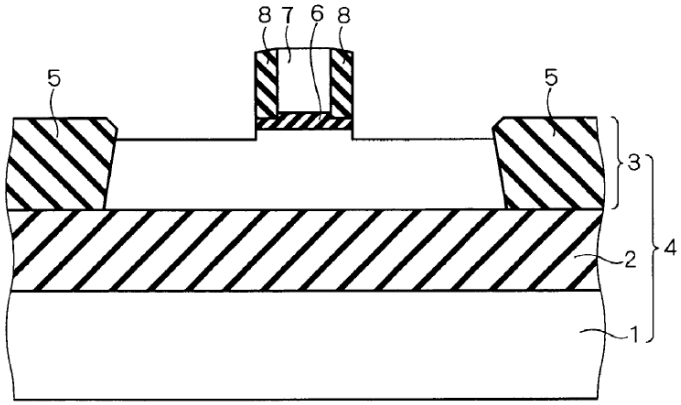
	FIG. 19 

FIG. 20

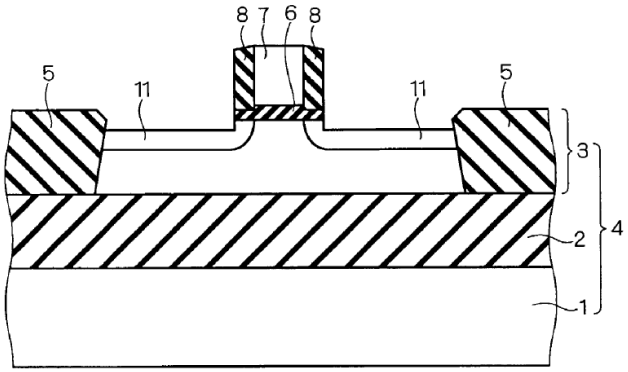
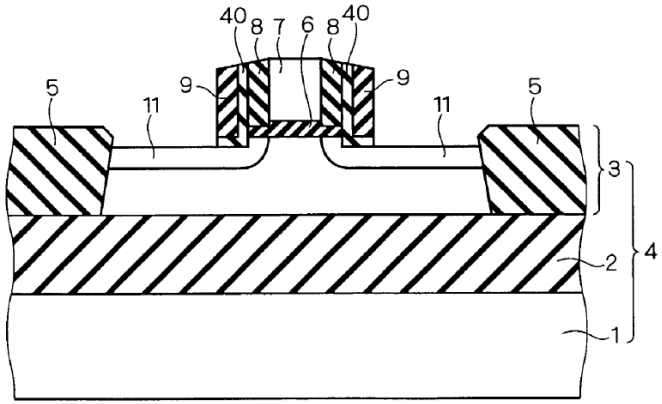
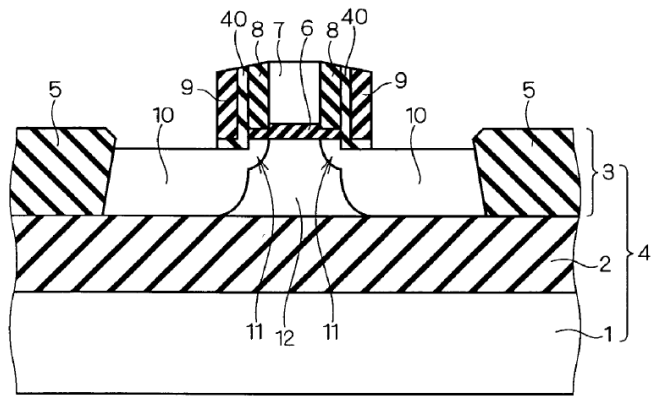


FIG. 21



F I G . 2 2



F I G . 2 3

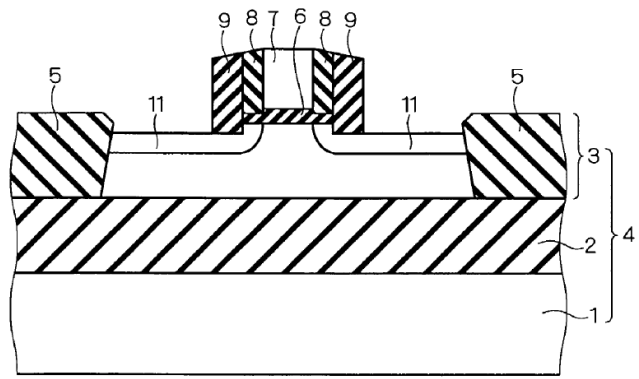


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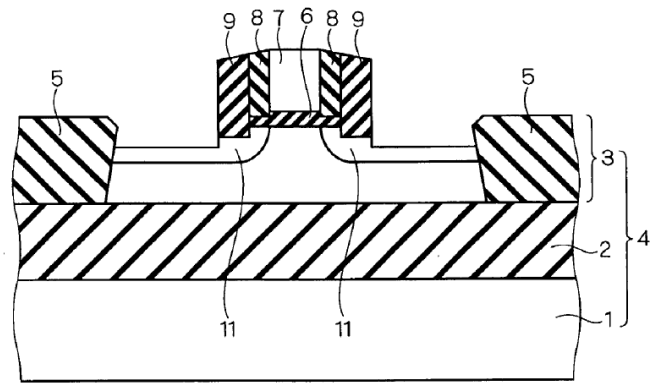
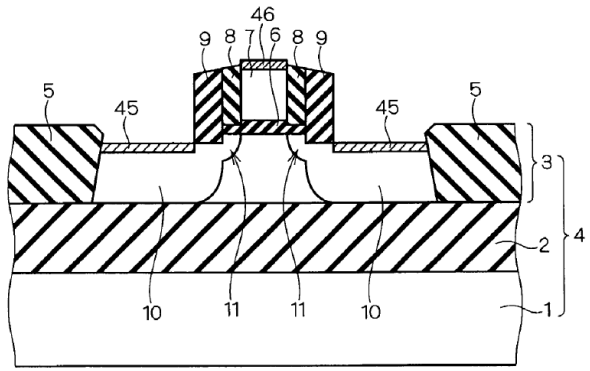
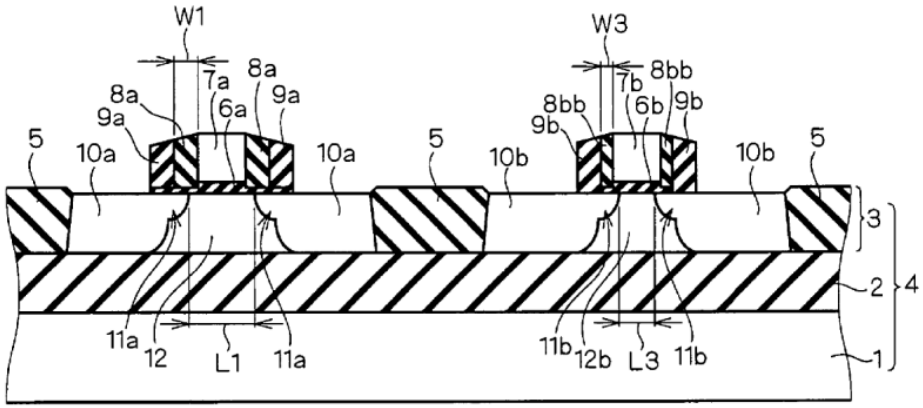
	FIG. 24  FIG. 25 

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	F I G . 2 6  *See also* limitations 1[C] and 1[D], *supra*.
Claim 14	
14. The semiconductor device of claim 1, wherein the insulating sidewall has a double layer structure including an oxide film and a nitride film.	*Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the insulating sidewall has a double layer structure including an oxide film and a nitride film. For example, *see* limitation [1C], *supra*. *Matsumoto 135* discloses the following at Abstract: A silicon nitride film (9) is formed on each side surface of the gate electrode (7), with a silicon oxide film (8) therebetween. The silicon oxide film (8) and the silicon nitride

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	film (9) are formed on the silicon oxide film (6). The width (W1) of the silicon oxide film (8) in a direction of the gate length is greater than the thickness (T1) of the silicon oxide film (6). *Matsumoto 135* discloses the following at ¶¶ 103-104: A silicon nitride film 9 is formed on each side surface of the gate electrode 7, with a silicon oxide film 8 therebetween. The silicon oxide film 8 and the silicon nitride film 9 are formed on the silicon oxide film 6. The width W1 of the silicon oxide film 8 in a direction of the gate length (or in the lateral direction as viewed in the drawing) is greater than the thickness T1 of the silicon oxide film 6. Side surfaces of the silicon oxide films 8 which are in contact with the side surfaces of the gate electrode 7 are herein defined as "inner side surfaces," and side surfaces thereof which are out of contact with the side surfaces of the gate electrodes 7 are defined as "outer side surfaces." Side surfaces of the silicon nitride films 9 which are in contact with the outer side surfaces of the silicon oxide films 8 are herein defined as "inner side surfaces," and side surfaces thereof which are out of contact with the outer side surfaces of the silicon oxide films 8 are defined as "outer side surfaces." *Matsumoto 135* discloses the following at ¶¶ 109-110: Next, referring to FIG. 5, a silicon oxide film 16 is formed on the entire top surface of the resultant structure by a CVD process or a thermal oxidation process. An HTO film, an LTO film, a TEOS film or a plasma oxide film may be formed in place of the silicon oxide film 16. Referring to FIG. 6, the silicon oxide film 16 is etched by an anisotropic dry etching process which exhibits a higher etch rate in the direction of depth of the SOI substrate 4. This forms silicon oxide films 8*a* and 8*b* on the side surfaces of the gate electrodes 7*a* and 7*b*. In this process, etching may be stopped before the upper surface of the silicon oxide film 13 and the upper surfaces of the gate electrodes 7*a* and 7*b* are

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	exposed, so that the silicon oxide film 16 is left thin on the upper surface of the silicon oxide film 13 and the upper surfaces of the gate electrodes 7*a* and 7*b*. *Matsumoto 135* discloses the following at ¶ 114: Referring to FIG. 9, after the photoresist 19 is removed, a silicon nitride film 21 is formed on the entire top surface of the resultant structure by a CVD process. With reference to FIG. 10, an anisotropic dry etching process which exhibits a higher etch rate in the direction of depth of the SOI substrate 4 is performed to etch the silicon nitride film 21 and the silicon oxide film 13 in the order named until the upper surface of the silicon layer 3 is exposed. This forms silicon nitride films 9*a* and 9*b* serving as sidewall insulation films on the outer side surfaces of the silicon oxide films 8*a* and 8*b*. The silicon nitride films 9*a* and 9*b* are formed on the silicon oxide films 6*a* and 6*b*. *Matsumoto 135* discloses the following at ¶¶ 137-141: Referring first to FIG. 18, the gate electrode 7 is formed by the process described in the first preferred embodiment, and thereafter the silicon oxide film 16 is formed on the entire top surface of the resultant structure by a CVD process. Referring to FIG. 19, the silicon oxide film 16 is etched by an anisotropic dry etching process which exhibits a higher etch rate in the direction of depth of the SOI substrate 4. This forms the silicon oxide films 8 on the side surfaces of the gate electrode 7. The anisotropic dry etching process for formation of the silicon oxide films 8 is continued to overetch the upper surface of the silicon layer 3 exposed by the etching of the silicon oxide film 16. The etching causes damages to create defects in the upper surface of the silicon layer 3. With reference to FIG. 20, the extensions 11 are formed in the upper surface of the silicon layer 3 by an ion implantation process. Referring to FIG. 21, a silicon oxide film and a silicon nitride film are formed in the order named on the entire top surface of the resultant structure by a CVD process. Next, an anisotropic dry etching process which

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	exhibits a higher etch rate in the direction of depth of the SOI substrate 4 is performed to etch the silicon oxide film and the silicon nitride film until the upper surface of the silicon layer 3 is exposed. This forms silicon oxide films 40 and the silicon nitride films 9 on the outer side surfaces of the silicon oxide films 8. Referring to FIG. 22, the source/drain regions 10 are formed in the silicon layer 3 by an ion implantation process. In the method of manufacturing the semiconductor device according to the fourth preferred embodiment, as discussed above, the etching process for the formation of the silicon oxide films 8 etches the upper surface of the silicon layer 3 as well to create defects in the upper surface of the silicon layer 3. As a result, the defects act as lifetime killers for the parasitic bipolar transistor to reduce the gain of the parasitic bipolar transistor. The technique of the fourth preferred embodiment is applicable to any one of the first to third preferred embodiments. FIG. 23 is a sectional view showing a first modification of the method of manufacturing the semiconductor device according to the fourth preferred embodiment. The silicon nitride films 9 shown in FIG. 21 are formed on the upper surface of the silicon layer 3, with the silicon oxide films 40 therebetween. In the first modification of the fourth preferred embodiment, on the other hand, the silicon nitride films 9 are formed directly on the upper surface of the silicon layer 3. The technique of the first modification of the fourth preferred embodiment is applicable to any one of the first to fourth preferred embodiments. *Matsumoto 135* discloses the following at ¶ 143: FIG. 24 is a sectional view showing a second modification of the method of manufacturing the semiconductor device according to the fourth preferred embodiment. The anisotropic dry etching process for the formation of the silicon nitride films 9 in the technique shown in FIGS. 22 and 23 is stopped when the upper surface of the silicon layer 3 is exposed. In the second modification of the fourth preferred embodiment, on the other hand, the anisotropic dry etching process for the formation of the silicon nitride films 9 overetches the upper surface of the silicon layer 3 as well. The technique

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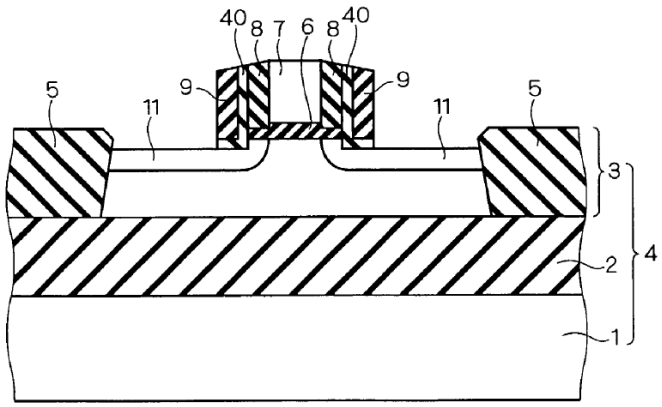
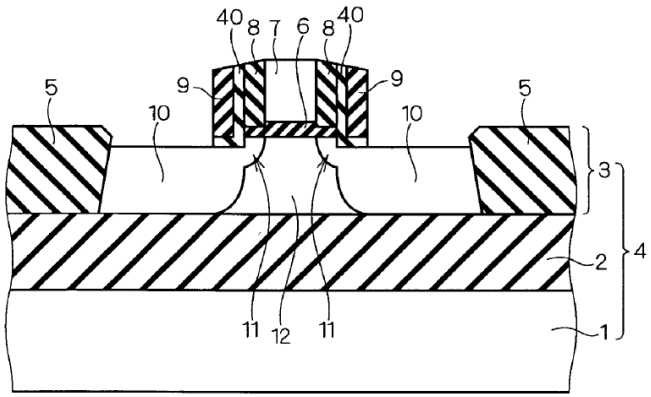
	of the second modification of the fourth preferred embodiment is applicable to any one of the first to fourth preferred embodiments and the first modification of the fourth preferred embodiment. *Matsumoto 135* discloses the following at Figures 21-26:

	FIG. 21  FIG. 22 

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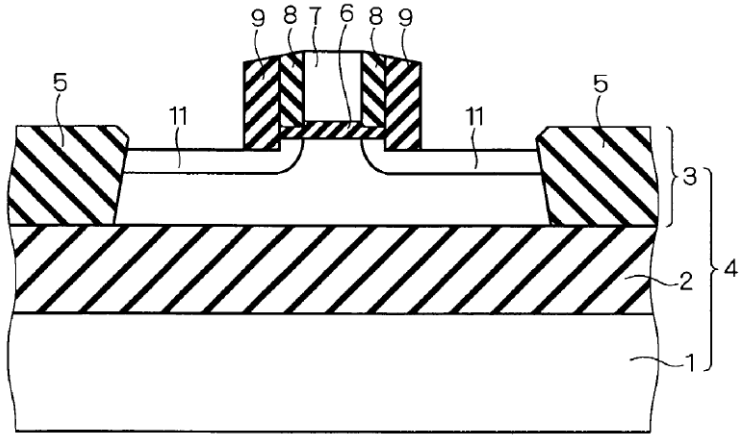
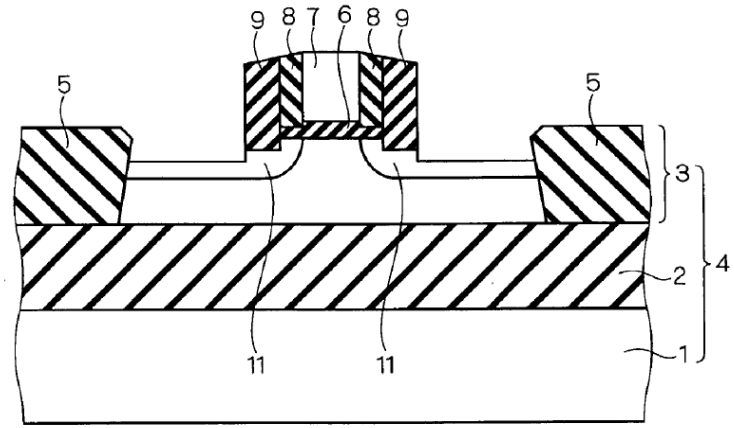
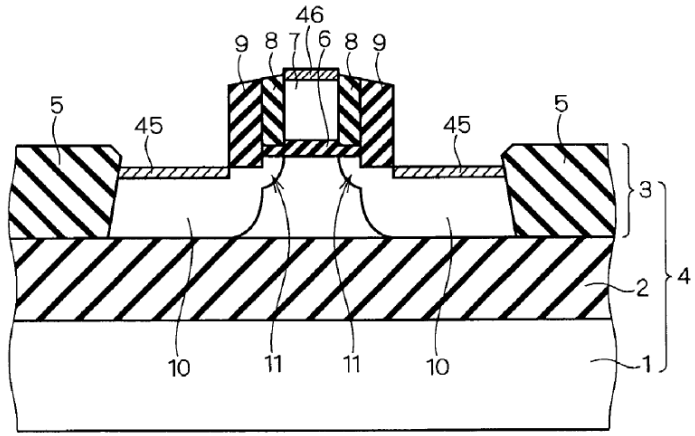
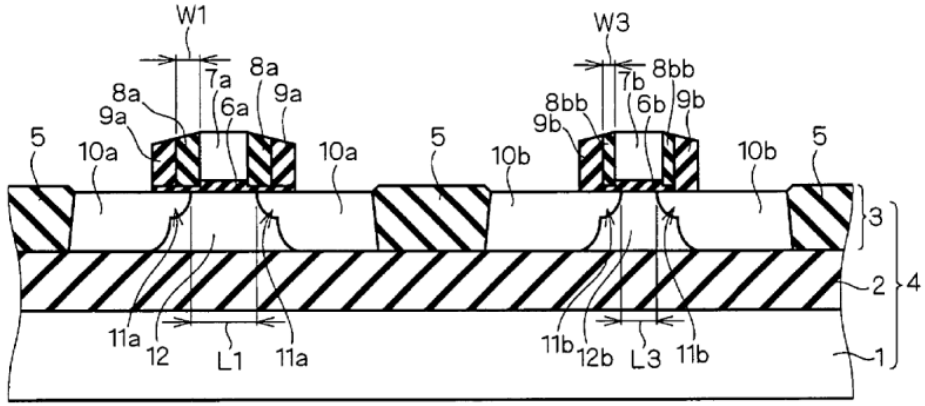


F I G . 2 4



U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
	FIG. 25  FIG. 26 

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Matsumoto 135*
Claim 16	
16. The semiconductor device of claim 1, wherein a width of the high dielectric constant gate insulating film along a gate length is larger than a width of the gate electrode along the gate length.	*Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Matsumoto 135*, alone or in combination with one or more references, discloses or suggests a width of the high dielectric constant gate insulating film along a gate length is larger than a width of the gate electrode along the gate length. For example, *see* limitation [1D], *supra*.
Claim 17	
17. The semiconductor device of claim 1, wherein a width of a bottom surface of the high dielectric constant gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length.	*Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Matsumoto 135*, alone or in combination with one or more references, discloses or suggests a width of a bottom surface of the high dielectric constant gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length. For example, *see* limitation [1D] and claim 16, *supra*.
Claim 18	
18. The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more.	*Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more.

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	For example: *See* limitation [1A], *supra*. *Matsumoto 135* discloses the following at ¶ 107: > FIGS. 3 through 12 are sectional views showing a method of manufacturing the semiconductor device shown in FIG. 2 in a step-by-step manner. Referring first to FIG. 3, the SOI substrate 4 is prepared, and then the isolating insulation film 5 are formed in the silicon layer 3. Next, a silicon oxide film 13 is formed entirely on the upper surface of the silicon layer 3 and the upper surface of the isolating insulation film 5 by a CVD process or a thermal oxidation process. A silicon oxynitride film, a metal oxide film such as Al_2O_3 or a ferroelectric film such as Ta_2O_5 and BST may be formed in place of the silicon oxide film 13. *Matsumoto 135* discloses the following at ¶ 137: > FIGS. 18 through 22 are sectional views showing a method of manufacturing a semiconductor device in a step-by-step manner according to a fourth preferred embodiment of the present invention. Referring first to FIG. 18, the gate electrode 7 is formed by the process described in the first preferred embodiment, and thereafter the silicon oxide film 16 is formed on the entire top surface of the resultant structure by a CVD process. *Matsumoto 135* discloses the following at ¶ 167: > With reference to FIG. 31, a silicon oxide film is formed entirely on the upper surface of the silicon layer 3 and the upper surfaces of the isolating insulation films 30, 50 by a CVD process or a thermal oxidation process. A silicon oxynitride film, a metal oxide film such as Al_2O_3 or a ferroelectric film such as Ta_2O_5 and BST may be formed in place of the silicon oxide film.

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Claim 19	
19. The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the insulating sidewall.	*Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the insulating sidewall. For example, *see* limitations [1A] and [1C], and claim 14, *supra*. *Matsumoto 135* discloses the following at ¶ 107: > FIGS. 3 through 12 are sectional views showing a method of manufacturing the semiconductor device shown in FIG. 2 in a step-by-step manner. Referring first to FIG. 3, the SOI substrate 4 is prepared, and then the isolating insulation film 5 are formed in the silicon layer 3. Next, a silicon oxide film 13 is formed entirely on the upper surface of the silicon layer 3 and the upper surface of the isolating insulation film 5 by a CVD process or a thermal oxidation process. A silicon oxynitride film, a metal oxide film such as Al_2O_3 or a ferroelectric film such as Ta_2O_5 and BST may be formed in place of the silicon oxide film 13. *Matsumoto 135* discloses the following at ¶ 114: > Referring to FIG. 9, after the photoresist 19 is removed, a silicon nitride film 21 is formed on the entire top surface of the resultant structure by a CVD process. With reference to FIG. 10, an anisotropic dry etching process which exhibits a higher etch rate in the direction of depth of the SOI substrate 4 is performed to etch the silicon nitride film 21 and the silicon oxide film 13 in the order named until the upper surface of the silicon layer 3 is exposed. This forms silicon nitride films 9*a* and 9*b* serving as sidewall insulation films on the outer side surfaces of the silicon oxide films 8*a* and 8*b*. The silicon nitride films 9*a* and 9*b* are formed on the silicon oxide films 6*a* and 6*b*.

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	Matsumoto 135 discloses the following at ¶¶ 137-141: Referring first to FIG. 18, the gate electrode 7 is formed by the process described in the first preferred embodiment, and thereafter the silicon oxide film 16 is formed on the entire top surface of the resultant structure by a CVD process. Referring to FIG. 19, the silicon oxide film 16 is etched by an anisotropic dry etching process which exhibits a higher etch rate in the direction of depth of the SOI substrate 4. This forms the silicon oxide films 8 on the side surfaces of the gate electrode 7. The anisotropic dry etching process for formation of the silicon oxide films 8 is continued to overetch the upper surface of the silicon layer 3 exposed by the etching of the silicon oxide film 16. The etching causes damages to create defects in the upper surface of the silicon layer 3. With reference to FIG. 20, the extensions 11 are formed in the upper surface of the silicon layer 3 by an ion implantation process. Referring to FIG. 21, a silicon oxide film and a silicon nitride film are formed in the order named on the entire top surface of the resultant structure by a CVD process. Next, an anisotropic dry etching process which exhibits a higher etch rate in the direction of depth of the SOI substrate 4 is performed to etch the silicon oxide film and the silicon nitride film until the upper surface of the silicon layer 3 is exposed. This forms silicon oxide films 40 and the silicon nitride films 9 on the outer side surfaces of the silicon oxide films 8. Referring to FIG. 22, the source/drain regions 10 are formed in the silicon layer 3 by an ion implantation process. In the method of manufacturing the semiconductor device according to the fourth preferred embodiment, as discussed above, the etching process for the formation of the silicon oxide films 8 etches the upper surface of the silicon layer 3 as well to create defects in the upper surface of the silicon layer 3. As a result, the defects act as lifetime killers for the parasitic bipolar transistor to reduce the gain of the parasitic bipolar transistor. The technique of the fourth preferred embodiment is applicable to any one of the first to third preferred embodiments.

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	FIG. 23 is a sectional view showing a first modification of the method of manufacturing the semiconductor device according to the fourth preferred embodiment. The silicon nitride films 9 shown in FIG. 21 are formed on the upper surface of the silicon layer 3, with the silicon oxide films 40 therebetween. In the first modification of the fourth preferred embodiment, on the other hand, the silicon nitride films 9 are formed directly on the upper surface of the silicon layer 3. The technique of the first modification of the fourth preferred embodiment is applicable to any one of the first to fourth preferred embodiments. *Matsumoto 135* discloses the following at ¶ 167: With reference to FIG. 31, a silicon oxide film is formed entirely on the upper surface of the silicon layer 3 and the upper surfaces of the isolating insulation films 30, 50 by a CVD process or a thermal oxidation process. A silicon oxynitride film, a metal oxide film such as Al_2O_3 or a ferroelectric film such as Ta_2O_5 and BST may be formed in place of the silicon oxide film.
Claim 21	
21. The semiconductor device of claim 1, wherein the end of the high dielectric constant gate insulating film located under the insulating sidewall has a tapered surface.	*Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the end of the high dielectric constant gate insulating film located under the insulating sidewall has a tapered surface.
Claim 22	
22. The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film located	*Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*.

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under the insulating sidewall has a thickness which becomes smaller toward the end thereof.	*Matsumoto 135*, alone or in combination with one or more references, discloses or suggests the high dielectric constant gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof.