REQUEST FORM FOR DIVISIONAL APPLICATION UNDER 37 CFR 1.53(b)

DOCKET NUMBER: 085393-0808
Prior Application:
Art Unit: 2898
Examiner: Chuong A. Luu

BOX New Application
FEE
Mail Stop New Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

This is a Request for filing a Divisional application under 37 CFR 1.53(b) of pending prior application No. 13/037,831, filed on March 1, 2011, entitled **SEMICONDUCTOR DEVICE**, by the following named inventors: Junji HIRASE, Akio SEBE, Naoki KOTANI, Gen OKAZAKI, Kazuhiko AIDA, Shinji TAKEOKA.

1. ☒ I hereby state that the enclosed application contains no new matter.

2. Oath or Declaration
   a. ☐ Newly executed (original or copy)
   b. ☒ Copy from a prior application (37 CFR 1.63(d))
      i. ☐ Deletion of inventor(s)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

3. ☒ Incorporation By Reference (useable if Box 2b is checked)
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 2b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

4. ☒ Preliminary Amendment is enclosed.

5. ☒ An Information Disclosure Statement and PTO1449 Form are submitted herewith.

6. ☒ Cancel claims 1-20.

UMC 1002
UMC v. AICP

7. The filing fee is calculated on the basis of the claims existing in the prior application as amended at 4 and 6 above:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	13	-20	0	$60.00	$0.00
Independent Claims	1	-3	0	$250.00	$0.00
				Multiple Dependent Claim(s)	$0.00
				Sheets of specification and drawing ($310.00 for each 50 sheets in excess of 100)	$0.00
				Basic Filing Fee	$380.00
				Patent Search Fee	$620.00
				Patent Examination Fee	$250.00
				Total of Above Calculations	$1,250.00
				Less ½ for Small Entity	$0.00
				Assignment & Recording Fee	$0.00
				Total Fee	$1,250.00

8. ☐ A Statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27 was filed in prior application and such status is still proper and desired.

9. ☒ **PLEASE CHARGE DEPOSIT ACCOUNT 500417 in the amount of $1,250.00**. Commissioner is authorized to charge any fees which may be required or credit any overpayment to Deposit Account No. 500417.

10. ☒ The Commissioner is hereby authorized to charge fees under 37 CFR 1.16 and 1.17 which may be required, including any extension of time fees to maintain the pendency of the parent Application No. 13/037,831 or credit any overpayment to Deposit Account No. 500417.

11. ☒ Priority of Application No. 2005-227457 filed on August 5, 2005, in Japan is claimed under 35 USC 119. The certified priority document was electronically retrieved in Application No. 13/037,831 on June 9, 2011.

12. ☒ The prior application is assigned of record to

Panasonic Corporation
Osaka, Japan

13. ☒ The power of attorney in the prior application is to:

McDermott Will & Emery LLP

14. ☐ Also enclosed:

15. ☐ A petition, fee and response has been filed to extend the term in the pending prior application until .

Address all future communications to: (May only be completed by applicant, or attorney or agent of record)

McDermott Will & Emery LLP
600 13th Street, N.W.
Washington, D.C. 20005-3096

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:ksa
Facsimile: 202.756.8087
Date: July 12, 2012

REQUEST FORM FOR DIVISIONAL APPLICATION UNDER 37 CFR 1.53(b)

DOCKET NUMBER: 085393-0808
Prior Application:
Art Unit: 2898
Examiner: Chuong A. Luu

BOX New Application
FEE
Mail Stop New Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

This is a Request for filing a Divisional application under 37 CFR 1.53(b) of pending prior application No. 13/037,831, filed on March 1, 2011, entitled **SEMICONDUCTOR DEVICE**, by the following named inventors: Junji HIRASE, Akio SEBE, Naoki KOTANI, Gen OKAZAKI, Kazuhiko AIDA, Shinji TAKEOKA.

1. ☒ I hereby state that the enclosed application contains no new matter.

2. Oath or Declaration
   a. ☐ Newly executed (original or copy)
   b. ☒ Copy from a prior application (37 CFR 1.63(d))
      i. ☐ Deletion of inventor(s)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

3. ☒ Incorporation By Reference (useable if Box 2b is checked)
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 2b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

4. ☒ Preliminary Amendment is enclosed.

5. ☒ An Information Disclosure Statement and PTO1449 Form are submitted herewith.

6. ☒ Cancel claims 1-20.

UMC 1002
UMC v. AICP

7. The filing fee is calculated on the basis of the claims existing in the prior application as amended at 4 and 6 above:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	13	-20	0	$60.00	$0.00
Independent Claims	1	-3	0	$250.00	$0.00
				Multiple Dependent Claim(s)	$0.00
				Sheets of specification and drawing ($310.00 for each 50 sheets in excess of 100)	$0.00
				Basic Filing Fee	$380.00
				Patent Search Fee	$620.00
				Patent Examination Fee	$250.00
				Total of Above Calculations	$1,250.00
				Less ½ for Small Entity	$0.00
				Assignment & Recording Fee	$0.00
				Total Fee	$1,250.00

8. ☐ A Statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27 was filed in prior application and such status is still proper and desired.

9. ☒ **PLEASE CHARGE DEPOSIT ACCOUNT 500417 in the amount of $1,250.00**. Commissioner is authorized to charge any fees which may be required or credit any overpayment to Deposit Account No. 500417.

10. ☒ The Commissioner is hereby authorized to charge fees under 37 CFR 1.16 and 1.17 which may be required, including any extension of time fees to maintain the pendency of the parent Application No. 13/037,831 or credit any overpayment to Deposit Account No. 500417.

11. ☒ Priority of Application No. 2005-227457 filed on August 5, 2005, in Japan is claimed under 35 USC 119. The certified priority document was electronically retrieved in Application No. 13/037,831 on June 9, 2011.

12. ☒ The prior application is assigned of record to

Panasonic Corporation
Osaka, Japan

13. ☒ The power of attorney in the prior application is to:

McDermott Will & Emery LLP

14. ☐ Also enclosed:

15. ☐ A petition, fee and response has been filed to extend the term in the pending prior application until .

Address all future communications to: (May only be completed by applicant, or attorney or agent of record)

McDermott Will & Emery LLP
600 13th Street, N.W.
Washington, D.C. 20005-3096

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:ksa
Facsimile: 202.756.8087
Date: July 12, 2012

Docket No.: 085393-0808 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Junji HIRASE, et al.	:	Confirmation Number: Not Yet Assigned
Application No.: Divisional of U.S. Serial No. 13/037,831	:	Group Art Unit: Not Yet Assigned
Filed: July 12, 2012	:	Examiner: Not Yet Assigned
For: SEMICONDUCTOR DEVICE	:	

PRELIMINARY AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Prior to examination of the above-referenced application, please amend the application as follows:

Amendments to the Title begin on page 2 of this paper.

Amendments to the Specification begin on page 3 of this paper.

Amendments to the Claims begin on page 4 of this paper.

Remarks/Arguments begin on page 6 of this paper.

UMC 1002
UMC v. AICP

IN THE TITLE:

Please amend the title as follows:

SEMICONDUCTOR DEVICE ~~AND METHOD FOR FABRICATING THE SAME~~

UMC 1002
UMC v. AICP

IN THE SPECIFICATION:

Please insert the following new paragraph after the Title and before the "BACKGROUND OF THE INVENTION"

-- RELATED APPLICATIONS

This application is a Divisional of U.S. Application No. 13/037,831, filed on March 1, 2011, which is a Divisional of U.S. Application No. 12/505,799, filed on July 20, 2009, now U.S. Patent No. 7,923,764, which is a Divisional of U.S. Application No. 11/491,260, filed on July 24, 2006, now U.S. Patent No. 7,579,227, claiming priority of Japanese Patent Application No. 2005-227457, filed on August 5, 2005, the entire contents of each of which are hereby incorporated by reference. --

UMC 1002
UMC v. AICP

IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application

Listing of Claims:

1-20. (Canceled)

21. (New) A semiconductor device comprising:

a gate insulating film formed on an active region in a substrate and including Hf;

a gate electrode formed on the gate insulating film;

a insulating sidewall formed on each side surface of the gate electrode; and

wherein a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length, and

an end of the gate insulating film under the insulating sidewall is located to retract from an outer end of the insulating sidewall toward the gate electrode.

22. (New) The semiconductor device of claim 21, further comprising a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film.

23. (New) The semiconductor device of claim 21, wherein

the gate insulating film is formed of a Hf based oxide.

24. (New) The semiconductor device of claim 21, wherein

the gate insulating film is formed of a HfSiON film..

25. (New) The semiconductor device of claim 21, wherein

a part of the gate insulating film located under the insulating sidewall includes a notch at the end thereof.

26. (New) The semiconductor device of claim 21, wherein

a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.

27. (New) The semiconductor device of claim 21, wherein

an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall.

28. (New) The semiconductor device of claim 21, wherein

the insulating sidewall has a double layer structure including an oxide film and a nitride film.

29. (New) The semiconductor device of claim 21, wherein

the insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film.

30. (New) The semiconductor device of claim 21, wherein

a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length.

31. (New) The semiconductor device of claim 21, wherein

the end of the gate insulating film located under the insulating sidewall has a tapered surface.

32. (New) The semiconductor device of claim 21, wherein

the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof.

33. (New) The semiconductor device of claim 21, wherein

the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length.

REMARKS

The specification in the above-referenced application has been amended to incorporate the continuity information. The title has been amended. Additionally, this amendment cancels claims 1-20, without prejudice. New claims 21-33 are pending examination in this Divisional application. No new matter has been introduced. Entry of this amendment is respectfully requested.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:ksa
Facsimile: 202.756.8087
Date: July 12, 2012

UMC 1002
UMC v. AICP

SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor device and a method for fabricating the semiconductor device. Specifically, the present invention relates to a structure of a MISFET (metal insulator semiconductor field-effect transistor) and a method for fabricating the MISFET and, more particularly, relates to techniques for improving the driving power and reliability of a MISFET.

Description of Prior Art

In recent years, as the degree of integration, function and operation speed of semiconductor integrated circuit devices have been highly improved, there have been attempts to reduce a junction depth of an extension according to a scaling rule and, at the same time, to use, as a gate insulating film of a MISFET, a high dielectric constant film formed of a Hf based oxide, Al based oxide or the like, which has a relative dielectric constant of 10 or more, instead of an SiO_2 based insulating film having a relative dielectric constant of about 4.

FIGS. **16A** and **16B** are cross-sectional views illustrating respective structures of known MISFETs using a high dielectric constant gate insulating film, respectively (see Ken Watanabe, *HfSiON-CMOS technology for achieving high performance and high reliability*, Semi. Forum Japan, 2005).

As shown in FIG. **16A**, a gate electrode **105** is formed on a region of a well **102** surrounded by a STI (shallow trench isolation) **103**. The region of the well **102** surrounded by the STI serves as an active region of a substrate **101**. The gate electrode **105** is

UMC 1002
UMC v. AICP

provided on the region with a high dielectric constant gate insulating film **104** interposed therebetween. An insulating sidewall **107** is formed on each side of the gate electrode **105**. An extension region **110** is formed in part of the well **102** located under the insulating sidewall **107**. A pocket region **111** is formed in part of the well **102** located under the extension region **110**. Source/drain regions **112** are formed so that each of the source/drain regions **112** is provided in parts of the well **102** located at the external side to the extension region **110** and the pocket region **111** when viewed from the gate electrode **105**.

A structure shown in FIG. **16B** is different from a structure shown in FIG. **16A** in that a sidewall **107** is formed on each side of a gate electrode **105** with an insulating offset sidewall **106** interposed therebetween. Thus, an overlapping amount of the gate electrode **105** and an extension region **110** can be optimized in a simple manner.

SUMMARY OF THE INVENTION

However, in a structure of a known MISFET using a high dielectric constant gate insulating film, side end portions of the high dielectric constant gate insulating film are in direct contact with sidewalls. Thus, in forming sidewalls of, for example, a silicon oxide film or the like, a composition of the side end portions of the high dielectric constant gate insulating film becomes closer to SiO_2 or like other inconvenience occurs. As a result, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film is caused at gate electrode end part, so that device characteristics of the MISFET are deteriorated and the reliability of the gate insulating film is degraded.

In view of the above-described problems, it is therefore an object of the present invention to improve characteristics of a MISFET without degrading of a high dielectric constant gate insulating film.

To achieve the above-described object, the inventors of the present application have

UMC 1002
UMC v. AICP

devised a MISFET structure in which a high dielectric constant gate insulating film is kept remaining under sidewalls to prevent end portions of the high dielectric constant gate insulating film from being in contact with the sidewalls, and a method for forming the MISFET structure. In the mean time, when the high dielectric constant gate insulating film is kept remaining under the sidewalls, a capacitance between gate/drain regions is increased, thus resulting in adverse effects on circuit speed. Also, in such cases, when extension implantation or LDD (lightly doped drain) implantation is performed, it is necessary to implant ions through a high dielectric constant film. Thus, when ion implantation is performed, expansion of an implanted impurity in the depth direction is increased, in other words, a junction point of an extension or an LDD is located at a large depth, so that desired device characteristics can not be obtained. This is because implantation acceleration energy is increased for the following reasons.

Reason 1) With use of a high dielectric constant film as a gate insulating film, a desired dielectric constant can be achieved even without having the thickness of the high dielectric constant film reduced. Therefore, the thickness of the high dielectric constant film has to be set at a large value.

Reason 2) A high dielectric constant film contains heavy metal and Rp (projection range) of implanted ions is small.

To cope with this problem, the inventors have devised a MISFET structure in which a high dielectric constant gate insulating film is kept remaining under sidewalls and part of the high dielectric constant gate insulating film located under the sidewalls is made to have a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under a gate electrode, and a method for forming the MISFET structure.

Specifically, a semiconductor device according to the present invention includes: a

high dielectric constant gate insulating film formed on an active region in a substrate; a gate electrode formed on the high dielectric constant gate insulating film; and an insulating sidewall formed on each side surface of the gate electrode. In the semiconductor device, the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall, and at least part of the high dielectric constant gate insulating film located under the insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

In the semiconductor device of the present invention, the insulating sidewall may include a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween, the high dielectric constant gate insulating film may be continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, and part of the high dielectric constant gate insulating film located under the first insulating sidewall may have a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

When the insulating sidewall includes the first insulating sidewall and the second insulating sidewall, the high dielectric constant gate insulating film may be formed so as not to be located under the second insulating sidewall.

When the insulating sidewall includes the first insulating sidewall and the second insulating sidewall, the high dielectric constant gate insulating film may be continuously formed so as to extend from under the gate electrode to under the second insulating sidewall, and part of the high dielectric constant gate insulating film located under the second insulating sidewall may have the same thickness as a thickness of part of the high dielectric constant gate insulating film located under the first insulating sidewall.

UMC 1002
UMC v. AICP

When the insulating sidewall includes the first insulating sidewall and the second insulating sidewall, the high dielectric constant gate insulating film may be continuously formed so as to extend from under the gate electrode to under the second insulating sidewall, and part of the high dielectric constant gate insulating film located under the second insulating sidewall may have a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the first insulating sidewall.

In the semiconductor device of the present invention, the insulating sidewall may include a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween, the high dielectric constant gate insulating film may be continuously formed so as to extend from under the gate electrode to under the second insulating sidewall, part of the high dielectric constant gate insulating film located under the first insulating sidewall may have the same thickness as a thickness of part of the high dielectric constant gate insulating film located under the gate electrode, and part of the high dielectric constant gate insulating film located under the second insulating sidewall may have a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

In the semiconductor device of the present invention, the high dielectric constant gate insulating film may include a notch at a side end portion.

The semiconductor device of the present invention may further include a buffer insulating film between the substrate and the high dielectric constant gate insulating film. In such a case, the buffer insulating film may be a silicon oxide film or a silicon oxynitride film.

In the semiconductor device of the present invention, the gate electrode may be a fully silicided gate electrode of which an entire region has been silicided.

UMC 1002
UMC v. AICP

A method for fabricating a semiconductor device according to the present invention includes the steps of: a) forming a high dielectric constant gate insulating film on an active region of a substrate; b) forming a gate electrode on the high dielectric constant gate insulating film; c) etching, after the step b), part of the high dielectric constant gate insulating film located in an external side to the gate electrode to reduce a thickness of the part; and d) forming, after the step c), an insulating sidewall on a side surface of the gate electrode.

The method for fabricating a semiconductor device according to the present invention may further include, after the step d), the step of removing part of the high dielectric constant gate insulating film located in an external side to the insulating sidewall.

In the method for fabricating a semiconductor device according to the present invention, the insulating sidewall may include a first insulating sidewall and a second insulating sidewall, and the step d) may include the step d1) of forming the first insulating sidewall on a side surface of the gate electrode and the step of d2) of forming the second insulating sidewall on the side surface of the gate electrode with the first insulating sidewall interposed therebetween.

When the step d) includes the step d1) and the step d2), the method for fabricating a semiconductor device according to the present invention may further include, between the step d) and the step d2), the step of removing part of the high dielectric constant gate insulating film located in the external side to the first insulating sidewall.

When the step d) includes the step d1) and the step d2), the method for fabricating a semiconductor device according to the present invention may further include, between d1) and the step d2), the step of etching part of the high dielectric gate insulating film located in an external side to the first insulating sidewall to reduce a thickness of the part; and after the step d2), the step of removing part of the high dielectric constant gate insulating film

UMC 1002
UMC v. AICP

located in an external side to the second insulating sidewall.

In the method for fabricating a semiconductor device according to the present invention, the dielectric constant gate insulating film may be selectively removed by wet etching.

In the method for fabricating a semiconductor device according to the present invention, the step b) may include the step of forming a protective film for covering an upper surface of the gate electrode, and the method may further include, after the step d), the step of siliciding a surface of part of the active region located in the external side to the insulating sidewall, removing the protective film and then fully siliciding the gate electrode.

The method for fabricating a semiconductor device according to the present invention further includes, before the step a), the step of forming a buffer insulating film on the active region, and in the step a), the high dielectric constant gate insulating film may be formed on the active region with the buffer insulating film interposed therebetween.

According to the present invention, a high dielectric constant gate insulating film is continuously formed so as to extend from under a gate electrode to under a sidewall. In other words, continuity of the high dielectric constant gate insulating film at a gate end portion is maintained. Thus, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film at the gate end portion, caused by a side end portion of the high dielectric constant gate insulating film being in direct contact with a sidewall film, can be suppressed. Moreover, the high dielectric constant gate insulating film is formed so as to have a smaller thickness in the part located under the sidewall than a thickness of the part located under gate electrode. Thus, increase in a capacitance between a gate and a drain can be suppressed, so that adverse effects on circuit speed can be reduced. Furthermore, since extension implantation or LDD implantation is performed

through the part of the high dielectric constant film which has a small thickness, increase in implantation acceleration energy can be suppressed. Accordingly, a shallow junction can be formed in an extension or a LDD in a simple manner. Therefore, device characteristics can be improved in a simple manner.

As has been described, the present invention relates to a semiconductor device and a method for fabricating the semiconductor device. Specifically, when the present invention is applied to a MISFET including a high dielectric constant gate insulating film, the effect of improving the driving power and reliability of the MISFET can be achieved and is therefore very useful.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-sectional view illustrating a structure of a semiconductor device according to a first embodiment of the present invention.

FIG. **2** is a cross-sectional view illustrating a structure of a semiconductor device according to a second embodiment of the present invention.

FIG. **3** is a cross-sectional view illustrating a structure of a semiconductor device according to a second modified example of the second embodiment of the present invention.

FIG. **4** is a cross-sectional view illustrating a structure of a semiconductor device according to a third modified example of the second embodiment of the present invention.

FIG. **5** is a cross-sectional view illustrating a structure of a semiconductor device according to a third embodiment of the present invention.

FIG. **6** is a cross-sectional view illustrating a structure of a semiconductor device according to a modified example of the first embodiment of the present invention.

FIG. **7** is a cross-sectional view illustrating a structure of a semiconductor device

UMC 1002
UMC v. AICP

according to a first modified example of the second embodiment of the present invention.

FIG. **8** is a cross-sectional view illustrating a structure of a semiconductor device according to a modified example of the third embodiment of the present invention.

FIG. **9** is a cross-sectional view illustrating a structure of a semiconductor device according to a fourth embodiment of the present invention.

FIG. **10** is a cross-sectional view illustrating a structure of a semiconductor device according to a modified example of the fourth embodiment of the present invention.

FIGS. **11A** through **11F** are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to a fifth embodiment of the present invention.

FIGS. **12A** through **12G** are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to a sixth embodiment of the present invention.

FIGS. **13A** through **13G** are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to a seventh embodiment of the present invention.

FIGS. **14A** through **14G** are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to an eighth embodiment of the present invention.

FIGS. **15A** through **15D** are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to the eighth embodiment of the present invention.

FIGS. **16A** and **16B** are cross-sectional views illustrating a structure of a known MISFET, respectively.

UMC 1002
UMC v. AICP

DESCRIPTION OF THE PREFERRED EMBODIMENTS

(First Embodiment)

Hereafter, a semiconductor device according to a first embodiment of the present invention will be described with reference to the accompanying drawings. FIG. **1** is a cross-sectional view illustrating a structure of a semiconductor device (more specifically, a single sidewall type MISFET) according to the first embodiment. In this embodiment, description will be made using an n-type MISFET as an example. However, even when the present invention is applied to a p-type MISFET, the same effects as those of this embodiment can be achieved.

As shown in FIG. **1**, a gate electrode **5** is formed on an active region of a p-type well **2** surrounded by a STI **3**. The p-type well **2** is formed in a substrate **1** made of, for example, silicon. The gate electrode **5** is formed on the active region with a high dielectric constant gate insulating film **4A** interposed therebetween. An insulating sidewall **7** is formed on each side surface of the gate electrode **5**. An n-type extension region **10** is formed in part of the p-type well **2** located under the sidewall **7**. Furthermore, a p-type pocket region **11** is formed in part of the p-type well **2** located under the n-type extension region **10**. N-type source/drain regions **12** are formed so that each of the source/drain regions **12** is provided in part of the p-type well **2** located in the external side to the n-type extension region **10** and the p-type pocket region **11** when viewed from the gate electrode **5**.

It is a first feature of this embodiment that the high dielectric constant gate insulating film **4A** is kept remaining not only under the gate electrode **5** but also under the sidewall **7**. That is, the high dielectric gate insulating film **4A** is continuously formed so as to extend from under the gate electrode **5** to under the sidewall **7**.

It is a second feature of this embodiment that the thickness of the part of the high

UMC 1002
UMC v. AICP

dielectric constant gate insulating film **4A** located under the sidewall **7** is smaller than a thickness of the part of the high dielectric constant film **4A** located under the gate electrode **5**. That is, the gate insulating film **4A** is formed so as to have a convex shape.

According to this embodiment, each side end portion of the high dielectric constant gate insulating film **4A** is not in contact with the sidewall **7** and continuity of the high dielectric constant gate insulating film **4A** at an end portion of the gate electrode **5** is maintained. Accordingly, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film **4A** at the end portion of the gate electrode **5** can be suppressed, so that deterioration of device characteristics of the MISFET and reduction in the reliability of the gate insulating film can be prevented.

According to this embodiment, the existence of the high dielectric constant gate insulating film **4A** under the sidewall **7** makes capacitive coupling between the gate electrode **5** and the n-type extension region **10** stronger in the vicinity of the end portion of the gate electrode **5**. As a result, a high overlapping effect between a gate and a drain can be achieved (see T. Hori, IEDM Tech. Dig., 1989, p. 777). Therefore, device characteristics and hot carrier reliability can be improved at the same time.

Meanwhile, in this embodiment, because of the existence of the high dielectric constant gate insulating film **4A** under the sidewall **7**, there might be cases where a capacitance particularly between the gate electrode **5** and each of the n-type source/drain regions **12** is increased and, accordingly, a circuit speed is reduced. However, as described above, in this embodiment, the high dielectric constant gate insulating film **4A** is formed so as to have a smaller thickness in the part located under the sidewall **7** than a thickness of the part located under the gate electrode **5**. Therefore, increase in a capacitance between the gate and the drain and adverse effect on the circuit speed can be suppressed.

As has been described, according to this embodiment, device/circuit characteristics

UMC 1002
UMC v. AICP

of an MISFET and the reliability of a gate insulating film, which are conventionally in the trade-off relationship, can be largely improved at the same time.

(Modified Example of First Embodiment)

Hereafter, a semiconductor device according to a modified example of the first embodiment of the present invention will be described with reference to the accompanying drawings. FIG. **6** is a cross-sectional view illustrating a structure of a semiconductor device (more specifically, a single sidewall n-type MISFET) according to the modified example of the first embodiment.

As shown in FIG. **6**, this modified example is different from the first embodiment in that part of a high dielectric constant gate insulating film **4A** located under each side end portion of a sidewall **7**, i.e., a side portion of the high dielectric constant gate insulating film **4A** is removed in a notch shape, so that a notch **20** is provided.

According to this modified example, adverse effects on circuit speed due to increase in a capacitance between a gate electrode **5** and each of n-type source/drain regions **12** can be further suppressed.

(Second Embodiment)

Hereafter, a semiconductor device according to a second embodiment of the present invention will be described with reference to the accompanying drawings. In contrast with the first embodiment in which a single sidewall type MISFET is described, a double sidewall type MISFET (see H. Sayama et al., IEDM Tech. Dig., 2000, p. 239) in which an overlapping amount between a gate electrode and an extension region can be optimized in a simple manner will be described in the second embodiment. In this embodiment, description will be made using an n-type MISFET as an example. However, even when

UMC 1002
UMC v. AICP

the present invention is applied to a p-type MISFET, the same effects as those of this embodiment can be achieved.

FIG. **2** is a cross-sectional view illustrating a structure of a semiconductor device according to the second embodiment. As shown in FIG. **2**, a gate electrode **5** is formed on an active region of a p-type well **2** surrounded by a STI **3**. The p-type well **2** is formed in a substrate **1** made of, for example, silicon. The gate electrode **5** is formed on the active region with a high dielectric constant gate insulating film **4B** interposed therebetween. An insulating sidewall **7** is formed on each side surface of the gate electrode **5** with an offset sidewall **6** interposed therebetween. An n-type extension region **10** is formed in each of parts of the p-type well **2** located under the offset sidewall **6** and the sidewall **7**. Furthermore, a p-type pocket region **11** is formed in part of the p-type well **2** located under the n-type extension region **10**. N-type source/drain regions **12** are formed so that each of the source/drain regions is provided in part of the p-type well **2** located in the external side to the n-type extension region **10** and the p-type pocket region **11** when viewed from the gate electrode **5**.

It is a first feature of this embodiment that the high dielectric constant gate insulating film **4B** is kept remaining not only under the gate electrode **5** but also under the offset sidewall **6**. That is, the high dielectric constant gate insulating film **4B** is continuously formed so as to extend from under the gate electrode **5** to under the offset sidewall **6**.

It is a second feature of this embodiment that the thickness of the part of the high dielectric constant gate insulating film **4B** located under the offset sidewall **6** is smaller than a thickness of the part of the high dielectric constant film **4B** located under the gate electrode **5**. That is, the gate insulating film **4B** is formed so as to have a convex shape.

According to this embodiment, each side end portion of the high dielectric constant

UMC 1002
UMC v. AICP

gate insulating film **4B** is not in contact with the offset sidewall **6** and continuity of the high dielectric constant gate insulating film **4B** at an end portion of the gate electrode **5** is maintained. Accordingly, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film **4B** at the end portion of the gate electrode **5** can be suppressed, so that deterioration of device characteristics of the MISFET and reduction in the reliability of the gate insulating film can be prevented.

According to this embodiment, the existence of the high dielectric constant gate insulating film **4B** under the offset sidewall **6** makes capacitive coupling between the gate electrode **5** and the n-type extension region **10** stronger in the vicinity of the end portion of the gate electrode **5**. As a result, a high overlapping effect between a gate and a drain can be achieved (see T. Hori, IEDM Tech. Dig., 1989, p. 777). Therefore, device characteristics and hot carrier reliability can be improved at the same time.

Moreover, according to this embodiment, the high dielectric constant gate insulating film **4B** does not exist under the sidewall **7**. Thus, increase in a capacitance between the gate electrode **5** and each of the n-type source/drain regions **12** can be further suppressed so that a small capacitance can be maintained. Accordingly, increase in a parasitic capacitance and adverse effects on circuit speed due to the increase can be suppressed at a minimum level.

As has been described, according to this embodiment, device/circuit characteristics of an MISFET and the reliability of a gate insulating film, which are conventionally in the trade-off relationship, can be largely improved at the same time.

(First Modified Example of Second Embodiment)

Hereafter, a semiconductor device according to a modified example of the second embodiment of the present invention will be described with reference to the accompanying

UMC 1002
UMC v. AICP

drawings. FIG. 7 is a cross-sectional view illustrating a structure of the semiconductor device (more specifically, a double sidewall type MISFET) according to the first modified example of the second embodiment.

As shown in FIG. 7, this modified example is different from the second embodiment is that part of a high dielectric constant gate insulating film **4B** located under each side end portion of the offset sidewall **6**, i.e., a side portion of the high dielectric constant gate insulating film **4B** is removed in a notch shape, so that a notch **20** is provided.

According to this modified example, adverse effects on circuit speed due to increase in a capacitance between a gate electrode **5** and each of n-type source/drain regions **12** can be further suppressed.

(Second Modified Example of Second Embodiment)

Hereafter, a semiconductor device according to a second modified example of the second embodiment of the present invention will be described with reference to the accompanying drawings. FIG. **3** is a cross-sectional view illustrating a structure of the semiconductor device (more specifically, a double sidewall type MISFET) according to the second modified example of the second embodiment.

This embodiment is different from the second embodiment in that a high dielectric constant gate insulating film **4C** is kept remaining not only under the gate electrode **5** and the offset sidewall **6** but also under the sidewall **7**. That is, the high dielectric constant gate insulating film **4C** is continuously formed so as to extend from under the gate electrode **5** to under the sidewall **7**.

In this modified example, the thickness of part of the high dielectric constant gate insulating film **4C** located under the sidewall **7** is the same as the thickness of part of the

UMC 1002
UMC v. AICP

high dielectric constant gate insulating film **4C** located under the offset sidewall **6**. That is, the high dielectric constant gate insulating film **4C** is formed so as to have a convex shape.

According to this modified embodiment, the high dielectric constant gate insulating film **4C** is continuously formed so as to extend from under the gate electrode **5** to under the sidewall **7**. Thus, even when the offset sidewall **6** has a very small width (thickness), each side end portion of the high dielectric constant gate insulating film **4C** is not in contact with the sidewall **7** and continuity of the high dielectric constant gate insulating film **4C** at an end portion of the gate electrode **5** is maintained. Accordingly, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film **4C** at the end portion of the gate electrode **5** can be suppressed, so that deterioration of device characteristics of the MISFET and reduction in the reliability of the gate insulating film can be prevented.

In this modified example, as in the first embodiment, because of the existence of the high dielectric constant gate insulating film **4C** under sidewall **7**, there might be cases where a capacitance between the gate electrode **5** and each of the n-type source/drain regions **12** is increased. However, as has been described, in this modified example, the high dielectric constant gate insulating film **4C** is formed so as to have a smaller thickness in the part located under the sidewall **7** than a thickness of the part located under the gate electrode **5**. Therefore, increase in a parasitic capacitance and adverse effects on circuit speed due to the increase can be suppressed.

(Third Modified Example of Second Embodiment)

Hereafter, a semiconductor device according to a third modified example of the second embodiment of the present invention will be described with reference to the accompanying drawings. FIG. **4** is a cross-sectional view illustrating a structure of a

UMC 1002
UMC v. AICP

semiconductor device (more specifically, a double sidewall type MISFET) according to the third modified example of the second embodiment.

A first difference between this modified example and the second embodiment is that in this modified example, a high dielectric constant gate insulating film **4D** is kept remaining not only under the gate electrode **5** and the offset sidewall **6** but also under the sidewall **7**. That is, the high dielectric constant gate insulating film **4D** is continuously formed so as to extend from under the gate electrode **5** to under the sidewall **7**.

A second difference between this modified example and the second embodiment is that in this modified example, the thickness of part of the high dielectric constant gate insulating film **4D** located under the offset sidewall **6** is the same as the thickness of part of the high dielectric constant gate insulating film **4D** located under the gate electrode **5**. The thickness of part of the high dielectric constant gate insulating film **4D** located under the sidewall **7** is smaller than the thickness of the part of the high dielectric constant gate insulating film **4D** located under the gate electrode **5**. That is, the high dielectric constant gate insulating film **4D** is formed so as to have a convex shape.

According to this modified example, the high dielectric constant gate insulating film **4D** is continuously formed so as to extend from under the gate electrode **5** to under the sidewall **7**. Thus, even when the offset sidewall **6** has a very small width (thickness), each side end portion of the high dielectric constant gate insulating film **4D** is not in contact with the sidewall **7** and continuity of the high dielectric constant gate insulating film **4D** at an end portion of the gate electrode **5** is maintained. Accordingly, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film **4D** at the end portion of the gate electrode **5** can be suppressed, so that deterioration of device characteristics of the MISFET and reduction in the reliability of the gate insulating film can be prevented.

UMC 1002
UMC v. AICP

In this modified example, as in the first embodiment, because of the existence of the high dielectric constant gate insulating film **4D** under sidewall **7**, there might be cases where a capacitance between the gate electrode **5** and each of the n-type source/drain regions **12** is increased. However, as has been described, in this modified example, the high dielectric constant gate insulating film **4D** is formed so as to have a smaller thickness in the part located under the sidewall **7** than a thickness of the part located under the gate electrode **5**. Therefore, increase in a parasitic capacitance and adverse effects on circuit speed due to the increase can be suppressed.

(Third Embodiment)

Hereafter, a semiconductor device according to a third embodiment of the present invention will be described with reference to the accompanying drawings. In contrast with the first embodiment in which a single sidewall type MISFET is described, a double sidewall type MISFET (see H. Sayama et al., IEDM Tech. Dig., 2000, p. 239) in which an overlapping amount between a gate electrode and an extension region can be optimized in a simple manner will be described in the third embodiment. In this embodiment, description will be made using an n-type MISFET as an example. However, even when the present invention is applied to a p-type MISFET, the same effects as those of this embodiment can be achieved.

FIG. **5** is a cross-sectional view illustrating a structure of a semiconductor device according to the third embodiment. As shown in FIG. **5**, a gate electrode **5** is formed on an active region of a p-type well **2** surrounded by a STI **3**. The p-type well **2** is formed in a substrate **1** made of, for example, silicon. The gate electrode **5** is formed on the active region with a high dielectric constant gate insulating film **4E** interposed therebetween. An insulating sidewall **7** is formed on each side surface of the gate electrode **5** with an offset

UMC 1002
UMC v. AICP

sidewall **6** interposed therebetween. An n-type extension region **10** is formed in each of parts of the p-type well **2** located under the offset sidewall **6** and the sidewall **7**. Furthermore, a p-type pocket region **11** is formed in part of the p-type well **2** located under the n-type extension region **10**. N-type source/drain regions **12** are formed so that each of the source/drain is provided in part of the p-type well **2** located in the external side to the n-type extension region **10** and the p-type pocket region **11** when viewed from the gate electrode **5**.

It is a first feature that the high dielectric constant gate insulating film **4E** is kept remaining not only under the gate electrode **5** and but also under each of the offset sidewall **6** and the sidewall **7**. That is, the high dielectric constant gate insulating film **4E** is continuously formed so as to extend from under the gate electrode **5** to under the sidewall **7**.

It is a second feature of this embodiment that the thickness of the part of the high dielectric constant gate insulating film **4E** located under the offset sidewall **6** is smaller than a thickness of the part of the high dielectric constant film **4E** located under the gate electrode **5** and the thickness of the high dielectric constant gate insulating film **4E** located under the sidewall **7** is smaller than the thickness of the part of the high dielectric constant film **4E** located under the offset sidewall **6**. That is, the gate insulating film **4E** is formed so as to have a double convex shape.

According to this embodiment, the high dielectric constant gate insulating film **4E** is continuously formed so as to extend from under the gate electrode **5** to under the sidewall **7**. Thus, even when the offset sidewall **6** has a very small width (thickness), each side end portion of the high dielectric constant gate insulating film **4E** is not in contact with the sidewall **7** and continuity of the high dielectric constant gate insulating film **4E** at an end portion of the gate electrode **5** is maintained. Accordingly, reduction in the

UMC 1002
UMC v. AICP

dielectric constant and insulation property of the high dielectric constant gate insulating film **4E** at the end portion of the gate electrode **5** can be suppressed, so that deterioration of device characteristics of the MISFET and reduction in the reliability of the gate insulating film can be prevented.

According to this embodiment, the existence of the high dielectric constant gate insulating film **4E** under the offset sidewall **6** makes capacitive coupling between the gate electrode **5** and the n-type extension region **10** stronger at the vicinity of the end portion of the gate electrode **5**. As a result, a high overlapping effect between a gate and a drain can be achieved (see T. Hori, IEDM Tech. Dig., 1989, p. 777). Therefore, device characteristics and hot carrier reliability can be improved at the same time.

As in the first embodiment, in this embodiment, because of the existence of the high dielectric constant gate insulating film **4E** under sidewall **7**, there might be cases where a capacitance between the gate electrode **5** and each of the n-type source/drain regions **12** is increased and, accordingly, a circuit speed is reduced. However, as has been described, in this embodiment, the high dielectric constant gate insulating film **4E** is formed so that the thickness of the high dielectric constant gate insulating film **4E** is reduced in the part located under the offset sidewall **6** and then is further reduced in the part located under the sidewall **7**. Therefore, increase in a parasitic capacitance and adverse effects on circuit speed due to the increase can be suppressed so that the parasitic capacitance is a very low level.

As has been described, according to this embodiment, device/circuit characteristics of an MISFET and the reliability of a gate insulating film, which are conventionally in the trade-off relationship, can be largely improved at the same time.

(Modified Example of Third Embodiment)

UMC 1002
UMC v. AICP

Hereafter, a semiconductor device according to a modified example of a third embodiment of the present invention will be described with reference to the accompanying drawings. FIG. **8** is a cross-sectional view illustrating a structure of a semiconductor device (more specifically, a double sidewall type MISFET) according to the modified example of the third embodiment.

As shown in FIG. **8**, this modified example is different from the first embodiment in that part of a high dielectric constant gate insulating film **4E** located under each side end portion of a sidewall **7**, i.e., a side portion of the high dielectric constant gate insulating film **4E** is removed in a notch shape, so that a notch **20** is provided.

According to this modified example, adverse effects on circuit speed due to increase in a capacitance between a gate electrode **5** and each of n-type source/drain regions **12** can be further suppressed.

(Fourth Embodiment)

Hereafter, a semiconductor device according to a fourth embodiment of the present invention will be described with reference to the accompanying drawings. FIG. **9** is a cross-sectional view illustrating a structure of a semiconductor device (more specifically, a single sidewall type MISFET) according to the fourth embodiment of the present invention. In this embodiment description will be made using an n-type MISFET as an example. However, even when the present invention is applied to a p-type MISFET, the same effects as those of this embodiment can be achieved.

As shown in FIG. **9**, this embodiment is different from the first embodiment in that, for example, a silicon oxide film, a silicon oxynitride film or the like is provided as a buffer insulating film **25** between a substrate **1** and a high dielectric constant gate insulating film **4A**.

UMC 1002
UMC v. AICP

According to this embodiment, in addition to the effects of the first embodiment, an interface between a substrate and a gate insulating film can be advantageously kept in a normal state. Specifically, by forming the high dielectric constant gate insulating film **4A** on the substrate **1** with the buffer insulating film **25** interposed therebetween, deterioration of an interface between a substrate and a gate insulating film can be suppressed, compared to the case where the high dielectric constant gate insulating film **4A** is formed directly on the substrate **1**.

In this embodiment, the buffer insulating film **25** is provided between the high dielectric constant gate insulating film **4A** of the first embodiment and the substrate **1**. However, instead of this structure, even if the buffer insulating film **25** is provided between the substrate **1** and the high dielectric constant gate insulating film **4B** of the second embodiment, the high dielectric constant gate insulating film **4C** of the second modified example of the second embodiment, the high dielectric constant gate insulating film **4D** of the third modified example of the second embodiment or the high dielectric constant gate insulating film **4E** of the third embodiment, the same effects as those of this embodiment can be achieved. Moreover, instead of providing the buffer insulating film **25** between the substrate **1** and the high dielectric constant gate insulating film **4A**, **4B**, **4C**, **4D** or **4E**, a buffer insulating film may be provided between the gate electrode **5** and the high dielectric constant gate insulating film **4A**, **4B**, **4C**, **4D** or **4E**. With such a structure, compared to the case where the gate electrode **5** is directly formed on the high dielectric constant gate insulating film **4A**, **4B**, **4C**, **4D** or **4E**, deterioration of an interface between a gate electrode and a gate insulating film can be prevented. As another alternative, a buffer insulating film may be formed between the gate electrode **5** and the high dielectric constant gate insulating film **4A**, **4B**, **4C**, **4D** or **4E** as well as forming the buffer insulating film **25** between the substrate **1** and the high dielectric constant gate insulating film **4A**, **4B**, **4C**,

UMC 1002
UMC v. AICP

4D or **4E**. With such a structure, deterioration of each of the substrate-gate insulating film interface and the gate insulating film-gate electrode interface can be prevented at the same time.

(Modified Example of Fourth Embodiment)

Hereafter, a semiconductor device according to a modified example of the fourth embodiment of the present invention will be described with reference to the accompanying drawings. FIG. **10** is a cross-sectional view illustrating a structure of a semiconductor device (more specifically, a single sidewall type MISFET) according to the modified example of the fourth embodiment.

As shown in FIG. **10**, this modified example is different from the fourth embodiment in that part of a laminated insulating film of a high dielectric constant gate insulating film **4A** and a buffer insulating film **25** located under a side end portion of each sidewall **7**, i.e., a side end portion of the laminated insulating film is removed in a notch shape, so that a notch **20** is provided.

According to this modified example, adverse effects on circuit speed due to increase in a capacitance between a gate electrode **5** and each of n-type source/drain regions **12** can be further suppressed.

In this modified example, the notch **20** is provided in the side end portion of the laminated insulating film of the high dielectric constant gate insulating film **4A** and the buffer insulating film **25** of the first embodiment. However, instead of this structure, even if a notch is provided in a side end portion of a laminated insulating film of the buffer insulating film **25** and the high dielectric constant gate insulating film **4B** of the second embodiment, the high dielectric constant gate insulating film **4C** of the second modified example of the second embodiment, the high dielectric constant gate insulating film **4D** of the third modified example of the second embodiment or the high dielectric constant gate

UMC 1002
UMC v. AICP

insulating film **4E** of the third embodiment, the same effects of the modified example can be achieved. In such cases, a buffer insulating film may be provided between the gate electrode **5** and the high dielectric constant gate insulating film **4A**, **4B**, **4C**, **4D** or **4D** as well as forming the buffer insulating film **25** between the substrate **1** and the high dielectric constant gate insulating film **4A**, **4B**, **4C**, **4D** or **4D**.

(Fifth Embodiment)

Hereafter, a method for fabricating a semiconductor device according to a fifth embodiment of the present invention will be described with reference to the accompanying drawings. In this embodiment, description will be made using a method for fabricating an n-type MISFET as an example. FIGS. **11A** through **11F** are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to the fifth embodiment.

First, as shown in FIG. **11A**, a STI **3** which is to be an isolation region is selectively formed on a substrate **1** of, for example, silicon and then, for example, B (boron) is ion implanted into the substrate **1** at an implantation energy of 300 keV and a dose of 1×10^{13} cm^{-2}. Thus, a p-type well **2** which is to be an active region is formed. Subsequently, ion implantation (of B at an implantation energy of 150 keV and a dose of 1×10^{13} cm^{-2}) for punch-through stopper formation and ion implantation (of B at an implantation energy of 20 keV and a dose of 5×10^{12} cm^{-2}) for channel formation are performed.

Next, as shown in FIG. **11B**, as a buffer insulating film, for example, a silicon oxide film (not shown) is formed on the active region of the p-type well **2** surrounded by the STI **3** so as to have a thickness of about 0.5 nm and then, as a high dielectric constant film **4**, for example, a HfSiON film is deposited thereon to a thickness of about 4 nm (i.e.,

UMC 1002
UMC v. AICP

about 1 nm in terms of an equivalent oxide thickness).

Next, as shown in FIG. **11C**, for example, a gate electrode material film **5A** is formed on the high dielectric constant gate insulating film **4** so as to have a thickness of about 100 nm.

Next, a resist pattern (not shown) is formed on the gate electrode material film **5A** so as to cover a gate electrode formation region, and then the gate electrode material film **5A** is etched using the resist pattern as a mask, thereby forming, as shown in FIG. **11D**, a gate electrode **5**. Thereafter, part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is removed by a thickness of about 2 nm by selective etching. Thus, a thickness of part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** can be reduced so that a remaining thickness of the part of the high dielectric constant gate insulating film **4** becomes about 2 nm. Subsequently, using the gate electrode **5** as a mask, for example, As (arsenic) is ion implanted into the substrate **1** at an implantation energy of 2 keV and a dose of 1×10^{15} cm $^{-2}$, thereby forming an n-type extension region **10**. Thereafter, using the gate electrode **5** as a mask, for example, B is ion implanted into the substrate **1** at an implantation energy of 10 keV and a dose of 3×10^{13} cm $^{-2}$, thereby forming a p-type pocket region **11**. In this case, the n-type extension region **10** may be formed after forming the p-type pocket region **11**.

Next, an insulating film is deposited over the substrate **1** to a thickness of about 50 nm, and then the insulating film is etched back to form, as shown in FIG. **11E**, an insulating sidewall 7 on each side surface of the gate electrode **5**.

Next, using the gate electrode **5** and the sidewall 7 as a mask, for example, As is ion implanted into the substrate **1** at an implantation energy of 10 keV and a dose of 5×10^{15} cm^{-2}, and then, for example, spike RTA (rapid thermal annealing) is performed at

UMC 1002
UMC v. AICP

a temperature of about 1050 °C, thereby activating the implanted impurity. Thus, as shown in FIG. **11F**, n-type source/drain regions **12** are formed.

According to the above-described fabrication method of this embodiment, the MISFET structure (see FIG. **1**) of the first embodiment can be realized in a relatively simple manner.

Meanwhile, the high dielectric constant gate insulating film **4** contains heavy metal and thus Rp (projection range) of implanted ions passing through the high dielectric constant gate insulating film **4** tends to be small. Therefore, in the process step of FIG. **11D**, if without reducing the thickness of the high dielectric constant gate insulating film **4**, ion implantation is performed to the substrate **1** covered with the high dielectric constant gate insulating film **4** in the external side to the gate electrode **5** to form the n-type extension region **10** or the p-type pocket region **11**, an acceleration energy has to be increased. However, in this embodiment, the part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** has a reduced thickness, so that increase in acceleration energy can be suppressed. Accordingly, a shallow junction can be formed in the n-type extension region **10** in a simple manner and thus device characteristics can be improved in a simple manner.

In this embodiment, after the sidewall **7** has been formed, for example, part of the high dielectric constant gate insulating film **4** located in the external side to the sidewall **7** may be removed by wet etching using hydrofluoric acid or the like or selective dry etching. In such a case, when wet etching is used, part of the high dielectric constant gate insulating film **4** located under each side end portion of the sidewall **7**, i.e., a side end portion of the high dielectric constant gate insulating film **4** may be removed in a notch shape, so that a notch is formed. Thus, the MISFET structure (see FIG. **6**) of the modified example of the first embodiment can be realized in a simple manner.

UMC 1002
UMC v. AICP

In this embodiment, a target thickness for reduction in the thickness of the part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is not particularly limited. However, for example, when an HfSiON film is used as the high dielectric constant gate insulating film **4**, to suppress increase in a capacitance between a gate and a grain, the thickness of part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is preferably reduced to about 2 nm or less (so that a surface of the substrate **1** is not exposed).

(Sixth Embodiment)

Hereafter, a method for fabricating a semiconductor device according to a sixth embodiment of the present invention will be described with reference to the accompanying drawings. In this embodiment, description will be made using a method for fabricating an n-type MISFET as an example. FIGS. **12A** through **12G** are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to the sixth embodiment.

First, as shown in FIG. **12A**, a STI **3** which is to be an isolation region is selectively formed on a substrate **1** of, for example, silicon and then, for example, B is ion implanted into the substrate **1** at an implantation energy of 300 keV and a dose of 1×10^{13} cm^{-2}. Thus, a p-type well **2** which is to be an active region is formed. Subsequently, ion implantation (of B at an implantation energy of 150 keV and a dose of 1×10^{13} cm^{-2}) for punch-through stopper formation and ion implantation (of B at an implantation energy of 20 keV and a dose of 5×10^{12} cm^{-2}) for channel formation are performed.

Next, as shown in FIG. **12B**, as a buffer insulating film, for example, a silicon oxide film (not shown) is formed on the active region of the p-type well **2** surrounded by the STI **3** so as to have a thickness of about 0.5 nm and then, as a high dielectric constant

UMC 1002
UMC v. AICP

film **4**, for example, a HfSiON film is deposited thereon to a thickness of about 4 nm (i.e., about 1 nm in terms of an equivalent oxide thickness).

Next, as shown in FIG. **12C**, for example, a gate electrode material film **5A** is formed on the high dielectric constant gate insulating film **4** so as to have a thickness of about 100 nm.

Next, a resist pattern (not shown) is formed on the gate electrode material film **5A** so as to cover a gate electrode formation region, and then the gate electrode material film **5A** is etched using the resist pattern as a mask, thereby forming, as shown in FIG. **12D**, a gate electrode **5**. Thereafter, part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is removed by a thickness of about 2 nm by selective etching. Thus, a thickness of the part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** can be reduced so that a remaining thickness of the part of the high dielectric constant gate insulating film **4** becomes about 2 nm.

Next, an insulating film is deposited over the substrate **1** to a thickness of about 10 nm, and then the insulating film is etched back to form, as shown in FIG. **12E**, an insulating offset sidewall **6** on each side surface of the gate electrode **5**. Thereafter, part of the high dielectric constant gate insulating film **4** located in the external side to the offset sidewall **6** is removed by wet etching using, for example, hydrofluoric acid or selective dry etching. Subsequently, using the gate electrode **5** and the offset sidewall **6** as a mask, for example, As is ion implanted into the substrate **1** at an implantation energy of 2 keV and a dose of 1×10^{15} cm^{-2}, thereby forming an n-type extension region **10**. Thereafter, using the gate electrode **5** and the offset sidewall **6** as a mask, for example, B is ion implanted into the substrate **1** at an implantation energy of 10 keV and a dose of 3×10^{13} cm^{-2}, thereby forming a p-type pocket region **11**.

UMC 1002
UMC v. AICP

Next, an insulating film is deposited over the substrate **1** to a thickness of about 50 nm, and then the insulating film is etched back to form, as shown in FIG. **12F**, an insulating sidewall **7** on each side surface of the gate electrode **5** with the offset sidewall **6** interposed therebetween.

Next, using the gate electrode **5**, the offset sidewall **6** and the sidewall **7** as a mask, for example, As is ion implanted into the substrate **1** at an implantation energy of 10 keV and a dose of 5×10^{15} cm^{-2}, and then, for example, spike RTA (rapid thermal annealing) is performed at a temperature of about 1050 °C, thereby activating the implanted impurity. Thus, as shown in FIG. **12G**, n-type source/drain regions **12** are formed.

According to the above-described fabrication method of this embodiment, the MISFET structure (see FIG. **2**) of the second embodiment can be realized in a relatively simple manner.

In this embodiment, after the offset sidewall **6** has been formed, part of the high dielectric constant gate insulating film **4** located in the external side to the offset sidewall **6** is removed , for example, by wet etching using hydrofluoric acid or the like. When this wet etching is performed, part of the high dielectric constant gate insulating film **4** located under each side end portion of the offset sidewall **6**, i.e., a side end portion of the high dielectric constant gate insulating film **4** may be removed in a notch shape, so that a notch is formed. Thus, the MISFET structure (see FIG. **7**) of the first modified example of the second embodiment can be realized in a simple manner.

In this embodiment, a target thickness for reduction in the thickness of the part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is not particularly limited. However, for example, when an HfSiON film is used as the high dielectric constant gate insulating film **4**, to suppress increase in a capacitance between a gate and a grain, the thickness of part of the high dielectric constant

UMC 1002
UMC v. AICP

gate insulating film **4** located in the external side to the gate electrode **5** is preferably reduced to about 2 nm or less (so that a surface of the substrate **1** is not exposed).

In this embodiment, after the offset sidewall **6** has been formed, part of the high dielectric constant gate insulating film **4** located in the external side to the offset sidewall **6** is removed, and then ion implantation for forming the n-type extension region **10** and the p-type pocket region **11** is performed. However, instead of performing these process steps, ion implantation for forming the n-type extension region **10** and the p-type pocket region **11** may be performed after the offset sidewall **6** is formed and with part of the high dielectric constant gate insulating film **4** having a reduced thickness remaining in the external side to the offset sidewall **6**. Even in this manner, according to this embodiment, the part of the high dielectric constant gate insulating film **4** located in the external side to the offset sidewall **6** has a reduced thickness, so that increase in acceleration energy can be suppressed. Accordingly, a shallow junction can be formed in the n-type extension region **10** in a simple manner and thus device characteristics can be improved in a simple manner. In this case, ion implantation for forming an extension region and a pocket region of an MISFET having a different channel type or another power supply system and being provided on the same substrate may be performed after ion implantation for forming the n-type extension region **10** and the p-type pocket region **11** and then removal of the part of the high dielectric constant gate insulating film **4** located in the external side to the offset sidewall **6**.

(Seventh Embodiment)

Hereafter, a method for fabricating a semiconductor device according to a seventh embodiment of the present invention will be described with reference to the accompanying drawings. FIGS. **13A** through **13G** are cross-sectional views illustrating respective steps

UMC 1002
UMC v. AICP

for fabricating a semiconductor device according to the seventh embodiment.

First, as shown in FIG. **13A**, a STI **3** which is to be an isolation region is selectively formed on a substrate **1** of, for example, silicon and then, for example, B is ion implanted into the substrate **1** at an implantation energy of 300 keV and a dose of 1×10^{13} cm^{-2}. Thus, a p-type well **2** which is to be an active region is formed. Subsequently, ion implantation (of B at an implantation energy of 150 keV and a dose of 1×10^{13} cm^{-2}) for punch-through stopper formation and ion implantation (of B at an implantation energy of 20 keV and a dose of 5×10^{12} cm^{-2}) for channel formation are performed.

Next, as shown in FIG. **13B**, as a buffer insulating film, for example, a silicon oxide film (not shown) is formed on the active region of the p-type well **2** surrounded by the STI **3** so as to have a thickness of about 0.5 nm and then, as a high dielectric constant film **4**, for example, a HfSiON film is deposited thereon to a thickness of about 4 nm (i.e., about 1 nm in terms of an equivalent oxide thickness).

Next, as shown in FIG. **13C**, for example, a gate electrode material film **5A** is formed on the high dielectric constant gate insulating film **4** so as to have a thickness of about 100 nm.

Next, a resist pattern (not shown) is formed on the gate electrode material film **5A** so as to cover a gate electrode formation region, and then the gate electrode material film **5A** is etched using the resist pattern as a mask, thereby forming, as shown in FIG. **13D**, a gate electrode **5**. Thereafter, part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is removed by a thickness of about 2 nm by selective etching. Thus, a thickness of part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** can be reduced so that a remaining thickness of the part of the high dielectric constant gate insulating film **4**

UMC 1002
UMC v. AICP

becomes about 2 nm.

Next, an insulating film is deposited over the substrate **1** to a thickness of about 5 nm, and then the insulating film is etched back to form, as shown in FIG. **13E**, an insulating offset sidewall **6** on each side surface of the gate electrode **5**. Thereafter, part of the high dielectric constant gate insulating film **4** which is not covered by the gate electrode **5** and the offset sidewall **6** is further removed by about 1 nm. Thus, the thickness of part of the high dielectric gate insulating film **4** located in the external side to the offset sidewall **6** can be reduced to a thickness of about 1 nm. Then, using the gate electrode **5** and the offset sidewall **6** as a mask, for example, As is ion implanted into the substrate **1** at an implantation energy of 2 keV and a dose of 1×10^{15} cm^{-2}, thereby forming an extension region **10**. Thereafter, using the gate electrode **5** and the offset sidewall **6** as a mask, for example, B is ion implanted into the substrate **1** at an implantation energy of 10 keV and a dose of 3×10^{13} cm^{-2}, thereby forming a p-type pocket region **11**.

Next, an insulating film is deposited over the substrate **1** to a thickness of about 50 nm, and then the insulating film is etched back to form, as shown in FIG. **13F**, an insulating sidewall **7** on each side surface of the gate electrode **5** with the offset sidewall **6** interposed therebetween.

Next, using the gate electrode **5**, the offset sidewall **6** and the sidewall **7** as a mask, for example, As is ion implanted into the substrate **1** at an implantation energy of 10 keV and a dose of 5×10^{15} cm^{-2}, and then, for example, spike RTA (rapid thermal annealing) is performed at a temperature of about 1050 °C, thereby activating the implanted impurity. Thus, as shown in FIG. **13G**, n-type source/drain regions **12** are formed.

According to the above-described fabrication method of this embodiment, the MISFET structure (see FIG. **5**) of the third embodiment can be realized in a relatively simple manner.

UMC 1002
UMC v. AICP

In this embodiment, the high dielectric constant gate insulating film **4E** is formed so that the thickness of the high dielectric constant gate insulating film **4E** is reduced in the part located under the offset sidewall **6** and then is further reduced in the part located in the external side to the offset sidewall **6**. Therefore, even when ion implantation for forming the n-type extension region **10** is performed using the gate electrode **5** and the offset sidewall **6** as a mask, increase in acceleration energy can be suppressed at a minimum level. Accordingly, a shallow junction can be formed at an even shallower depth in the n-type extension region **10** in a simple manner and thus device characteristics can be improved in a simple manner.

In this embodiment, after the sidewall **7** has been formed, the part of the high dielectric constant gate insulating film **4** located in the external side to the sidewall **7** may be removed, for example, by wet etching using hydrofluoric acid or the like or selective dry etching. Moreover, in such a case, part of the high dielectric constant gate insulating film **4** located under each side end portion of the sidewall **7**, i.e., each side end portion of the high dielectric constant gate insulating film **4** may be removed in a notch shape. Thus, the MISFET structure (see FIG. **8B**) of the modified embodiment of the third embodiment can be realized in a simple manner.

In this embodiment, a target thickness for reduction in the thickness of the part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is not particularly limited either under the offset sidewall **6** or under the sidewall **7**. However, for example, when an HfSiON film is used as the high dielectric constant gate insulating film **4**, to suppress increase in a capacitance between a gate and a grain, the thickness of part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is preferably reduced to about 2 nm or less.

UMC 1002
UMC v. AICP

(Eighth Embodiment)

Hereafter, a method for fabricating a semiconductor device according to an eighth embodiment of the present invention will be described with reference to the accompanying drawings. In this embodiment, description will be made using a method for fabricating an n-type MISFET as an example. FIGS. **14A** through **14G** and FIGS. **15A** through **15D** are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to the eighth embodiment.

First, as shown in FIG. **14A**, for example, a STI **3** which is to be an isolation region is selectively formed on a substrate **1** of, for example, silicon and then, for example, B is ion implanted into the substrate **1** at an implantation energy of 300 keV and a dose of 1×10^{13} cm^{-2}. Thus, a p-type well **2** which is to be an active region is formed. Subsequently, ion implantation (of B at an implantation energy of 150 keV and a dose of 1×10^{13} cm^{-2}) for punch-through stopper formation and ion implantation (of B at an implantation energy of 20 keV and a dose of 5×10^{12} cm^{-2}) for channel formation are performed.

Next, as shown in FIG. **14B**, as a buffer insulating film, for example, a silicon oxide film (not shown) is formed on the active region of the p-type well **2** surrounded by the STI **3** so as to have a thickness of about 0.5 nm and then, as a high dielectric constant film **4**, for example, a HfSiON film is deposited thereon to a thickness of about 4 nm (i.e., about 1 nm in terms of an equivalent oxide thickness).

Next, as shown in FIG. **14C**, as a gate electrode material film **5A**, for example, a polysilicon film is formed on the high dielectric constant gate insulating film **4** so as to have a thickness of about 100 nm, and then as a cover film (protective film) **15**, for example, a silicon oxide film is deposited over the gate electrode material film **5A** to a thickness of about 10 nm.

UMC 1002
UMC v. AICP

Next, a resist pattern (not shown) is formed on the cover film **15** so as to cover a gate electrode formation region, and then the cover film **15** and the gate electrode material film **5A** are etched in this order using the resist pattern as a mask, thereby forming, as shown in FIG. **14D**, a gate electrode **5** with its upper surface covered by the cover film **15**. Thereafter, part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is removed by a thickness of about 2 nm by selective etching. Thus, a thickness of part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** can be reduced so that a remaining thickness of the part of the high dielectric constant gate insulating film **4** becomes about 2 nm.

Next, an insulating film is deposited over the substrate **1** to a thickness of about 10 nm, and then the insulating film is etched back to form, as shown in FIG. **14E**, an insulating offset sidewall **6** on each side surface of the gate electrode **5**. Thereafter, part of the high dielectric constant gate insulating film **4** located in the external side to the offset sidewall **6** is removed, for example, by wet etching using hydrofluoric acid or the like or selective dry etching. Subsequently, using the gate electrode **5** and the offset sidewall **6** as a mask, for example, As is ion implanted into the substrate **1** at an implantation energy of 2 keV and a dose of 1×10^{15} cm^{-2}, thereby forming an n-type extension region **10**. Thereafter, using the gate electrode **5** and the offset sidewall **6** as a mask, for example, B is ion implanted into the substrate **1** at an implantation energy of 10 keV and a dose of 3×10^{13} cm^{-2}, thereby forming a p-type pocket region **11**.

Next, an insulating film (for example, a SiN film) is deposited over the substrate **1** to a thickness of about 50 nm, and then the insulating film is etched back to form, as shown in FIG. **14F**, an insulating sidewall 7 on each side surface of the gate electrode **5** with the offset sidewall **6** interposed therebetween.

Next, using the gate electrode **5**, the offset sidewall **6** and the sidewall 7 as a mask,

UMC 1002
UMC v. AICP

for example, As is ion implanted into the substrate **1** at an implantation energy of 10 keV and a dose of 5×10^{15} cm^{-2}, and then, for example, spike RTA (rapid thermal annealing) is performed at a temperature of about 1050 °C, thereby activating the implanted impurity. Thus, as shown in FIG. **14G**, n-type source/drain regions **12** are formed.

Next, a metal film (for example, a Ni film) is deposited over the substrate **1** to a thickness of about 10 nm, and RTA is performed to bring a silicon portion of the substrate **1** and the metal film into reaction. Thus, as shown in FIG. **15A**, a silicide layer **13** is formed on the n-type source/drain regions **12**. Thereafter, unreacted part of the metal film which remains on the substrate **1** is exfoliated or removed.

Next, as shown in FIG. **15B**, an interlayer insulating film **14** is deposited over the substrate **1** as well as the gate electrode **5** to a thickness of about 400 nm.

Next, as shown in FIG. **15C**, the interlayer insulating film **14** is polished, for example, by CMP (chemical mechanical polishing) so that a surface of the interlayer insulating film **14** becomes at the same level as the upper surface of the cover film **15**, and then the exposed cover film **15** is removed by etching. In this case, respective upper portions of the interlevel insulating film **14** which has undergone through CMP and the offset sidewall **6** are also removed.

Next, a metal film (for example, a Ni film) is deposited over the substrate **1** to a thickness of about 100 nm, and then RTA is performed to bring a silicon portion of the gate electrode **5** and the metal film into reaction. Thus, as shown in FIG. **15D**, a fully silicided gate electrode **16** (obtained by siliciding the entire region over the high dielectric constant gate insulating film **4**) is formed.

According to the above-described fabrication method of this embodiment, the MISFET structure (see FIG. **2**) of the second embodiment using a FUSI (full silicide) structure can be realized in a relatively simple manner.

UMC 1002
UMC v. AICP

In this embodiment, when the offset sidewall **6** has been formed and then part of the high dielectric constant gate insulating film **4** located in the external side to the offset sidewall **6** is removed, for example, by wet etching using hydrofluoric acid or the like, part of the high dielectric constant gate insulating film **4** located under each side end portion of the offset sidewall **6**, i.e., each side portion of the high dielectric constant gate insulating film **4** may be removed in a notch shape so that a notch is provided. Thus, the MISFET structure (see FIG. 7) of the first modified example of the second embodiment using a FUSI structure can be realized in a simple manner.

In this embodiment, a target thickness for reduction in the thickness of the part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is not particularly limited. However, for example, when an HfSiON film is used as the high dielectric constant gate insulating film **4**, to suppress increase in a capacitance between a gate and a grain, the thickness of part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is preferably reduced to about 2 nm or less (so that a surface of the substrate **1** is not exposed).

In this embodiment, after the offset sidewall **6** has been formed, part of the high dielectric constant gate insulating film **4** located in the external side to the offset sidewall **6** is removed, and then ion implantation for forming the n-type extension region **10** and the p-type pocket region **11** is performed. However, instead of performing these process steps, ion implantation for forming the n-type extension region **10** and the p-type pocket region **11** may be performed after the offset sidewall **6** is formed and with part of the high dielectric constant gate insulating film **4** having a reduced thickness remaining in the outer side offset sidewall **6**. Even in this manner, according to this embodiment, the part of the high dielectric constant gate insulating film **4** located in the external side to the offset sidewall **6** has a reduced thickness, so that increase in acceleration energy can be

UMC 1002
UMC v. AICP

suppressed. Accordingly, a shallow junction can be formed in the n-type extension region **10** in a simple manner and thus device characteristics can be improved in a simple manner. In this case, ion implantation for forming an extension region and a pocket region of an MISFET having a different channel type or another power supply system and formed on the same substrate may be performed after ion implantation for forming the n-type extension region **10** and the p-type pocket region **11** and then removal of the part of the high dielectric constant gate insulating film **4** located in the external side to the offset sidewall **6**.

In this embodiment, the MISFET structure of the second embodiment using a FUSI structure has been formed. However, instead of forming the MISFET structure of the second embodiment, the MISFET structure of the first embodiment, the modified example of the first embodiment, each of the modified examples of the second embodiment, the third embodiment, the modified example of the third embodiment, the fourth embodiment or the modified example of the fourth embodiment may be formed using a FUSI structure.

In each of the first through eighth embodiments, a single layer structure of a SiN film has been used as an example of the sidewall **7**. However, instead of the single layer structure of a SiN film, for example, a double layer structure of a combination of an oxide film (SiO_2 film) and a nitride film (SiN film) (for example, including a SiO_2 layer as an lower layer and a SiN film as an upper layer), a triple layer structure (for example including an SiO_2 film as a lower layer, a SiN film as a middle layer and a SiO_2 film as an upper layer) or the like may be used.

In each of the first through eighth embodiments, instead of the n-type extension region **10**, a LDD may be formed.

In each of the fifth through eighth embodiments, instead of the n-type MISFET, a p-type MISFET may be formed.

UMC 1002
UMC v. AICP

In each of the fifth through eighth embodiments, to prevent deterioration of the interface of a gate insulating film and a gate electrode, a buffer insulating film may be formed between the gate electrode **5** and the high dielectric constant gate insulating film **4** so as to have a thickness of about 0.2 nm.

In each of the first through eighth embodiments, a shape of each side surface of the high dielectric constant gate insulating film **4** in which the notch **20** is provided in the part located under each side end portion of the sidewall **7** or the offset sidewall **6** is not limited to a semicircular shape shown in FIG. **6**, **7**, **8** or **10**. For example, each side surface of the high dielectric constant gate insulating film **4** may be a perpendicular plane to the substrate surface. That is, a side surface of the high dielectric constant gate insulating film **4** may be located at a predetermined distance from a side end surface of the sidewall **7** or the offset sidewall **6** toward the gate electrode **5**.

UMC 1002
UMC v. AICP

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a high dielectric constant gate insulating film formed on an active region in a substrate;

a gate electrode formed on the high dielectric constant gate insulating film; and

an insulating sidewall formed on each side surface of the gate electrode,

wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall, and

at least part of the high dielectric constant gate insulating film located under the insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

2. The semiconductor device of claim 1, wherein the insulating sidewall includes a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween,

the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, and

part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

3. The semiconductor device of claim 2, wherein the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall.

UMC 1002
UMC v. AICP

4. The semiconductor device of claim 2, wherein the high dielectric constant gate insulating film is continuously formed so as to extend to under the second insulating sidewall, and

part of the high dielectric constant gate insulating film located under the second insulating sidewall has the same thickness as a thickness of part of the high dielectric constant gate insulating film located under the first insulating sidewall.

5. The semiconductor device of claim 2, wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the second insulating sidewall, and

part of the high dielectric constant gate insulating film located under the second insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the first insulating sidewall.

6. The semiconductor device of claim 1, wherein the insulating sidewall includes a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween,

the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the second insulating sidewall,

part of the high dielectric constant gate insulating film located under the first insulating sidewall has the same thickness as a thickness of part of the high dielectric constant gate insulating film located under the gate electrode, and

part of the high dielectric constant gate insulating film located under the second insulating sidewall has a smaller thickness than a thickness of part of the high dielectric

UMC 1002
UMC v. AICP

constant gate insulating film located under the gate electrode.

7. The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film includes a notch at a side end portion.

8. The semiconductor device of claim 1, further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film.

9. The semiconductor device of claim 8, wherein the buffer insulating film is a silicon oxide film or a silicon oxynitride film.

10. The semiconductor device of claim 1, wherein the gate electrode is a fully silicided gate electrode of which an entire region has been silicided.

11. A method for fabricating a semiconductor device, the method comprising the steps of:

a) forming a high dielectric constant gate insulating film on an active region of a substrate;

b) forming a gate electrode on the high dielectric constant gate insulating film;

c) etching, after the step b), part of the high dielectric constant gate insulating film located in an external side to the gate electrode to reduce a thickness of the part; and

d) forming, after the step c), an insulating sidewall on a side surface of the gate electrode.

12. The method of claim 11, further comprising, after the step d), the step of removing part of the high dielectric constant gate insulating film located in an external side

UMC 1002
UMC v. AICP

to the insulating sidewall.

13. The method of claim 11, wherein the insulating sidewall includes a first insulating sidewall and a second insulating sidewall, and

the step d) includes the step d1) of forming the first insulating sidewall on a side surface of the gate electrode and the step of d2) of forming the second insulating sidewall on the side surface of the gate electrode with the first insulating sidewall interposed therebetween.

14. The method of claim 13, further comprising, between the step d1) and the step d2), the step of removing part of the high dielectric constant gate insulating film located in the external side to the first insulating sidewall.

15. The method of claim 13, further comprising:

between d1) and the step d2), the step of etching part of the high dielectric gate insulating film located in an external side to the first insulating sidewall to reduce a thickness of the part; and

after the step d2), the step of removing part of the high dielectric constant gate insulating film located in an external side to the second insulating sidewall.

16. The method of claim 12, wherein the high dielectric constant gate insulating film is selectively removed by wet etching.

17. The method of claim 14, wherein the high dielectric constant gate insulating film is selectively removed by wet etching.

UMC 1002
UMC v. AICP

18. The method of claim 15, wherein the high dielectric constant gate insulating film is selectively removed by wet etching.

19. The method of claim 11, wherein the step b) includes the step of forming a protective film for covering an upper surface of the gate electrode, and

the method further includes, after the step d), the step of siliciding a surface of part of the active region located in the external side to the insulating sidewall, removing the protective film and then fully siliciding the gate electrode.

20. The method of claim 11, further comprising before the step a), the step of forming a buffer insulating film on the active region,

wherein in the step a), the high dielectric constant gate insulating film is formed on the active region with the buffer insulating film interposed therebetween.

UMC 1002
UMC v. AICP

ABSTRACT OF THE DISCLOSURE

A semiconductor device includes: a high dielectric constant gate insulating film formed on an active region in a substrate; a gate electrode formed on the high dielectric constant gate insulating film; and an insulating sidewall formed on each side surface of the gate electrode. The high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall. At least part of the high dielectric constant gate insulating film located under the insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

UMC 1002
UMC v. AICP

FIG. 1

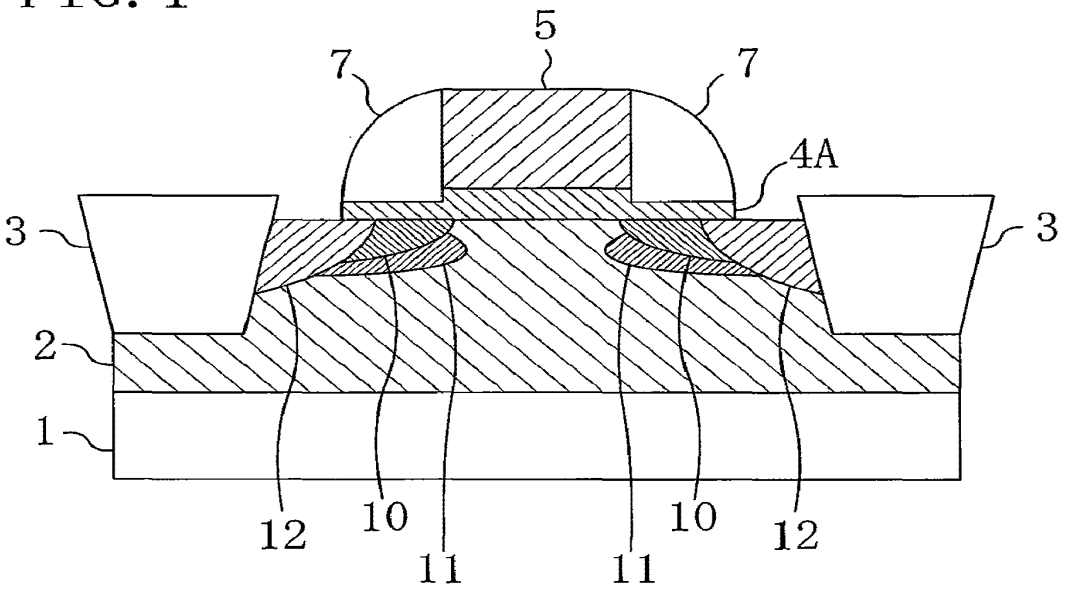
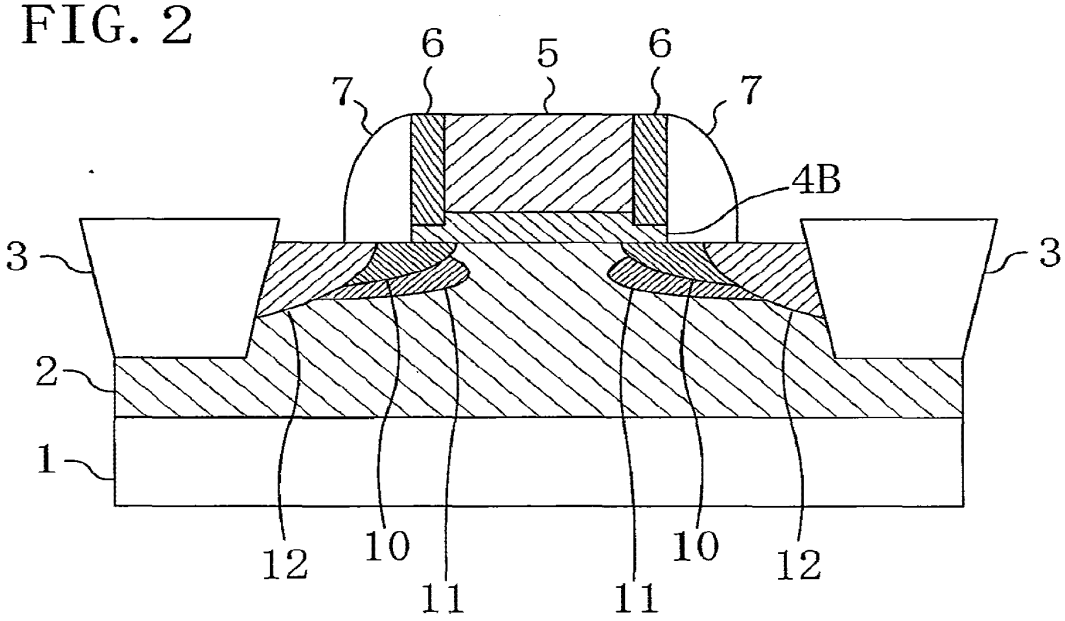


FIG. 2



UMC 1002
UMC v. AICP

FIG. 3

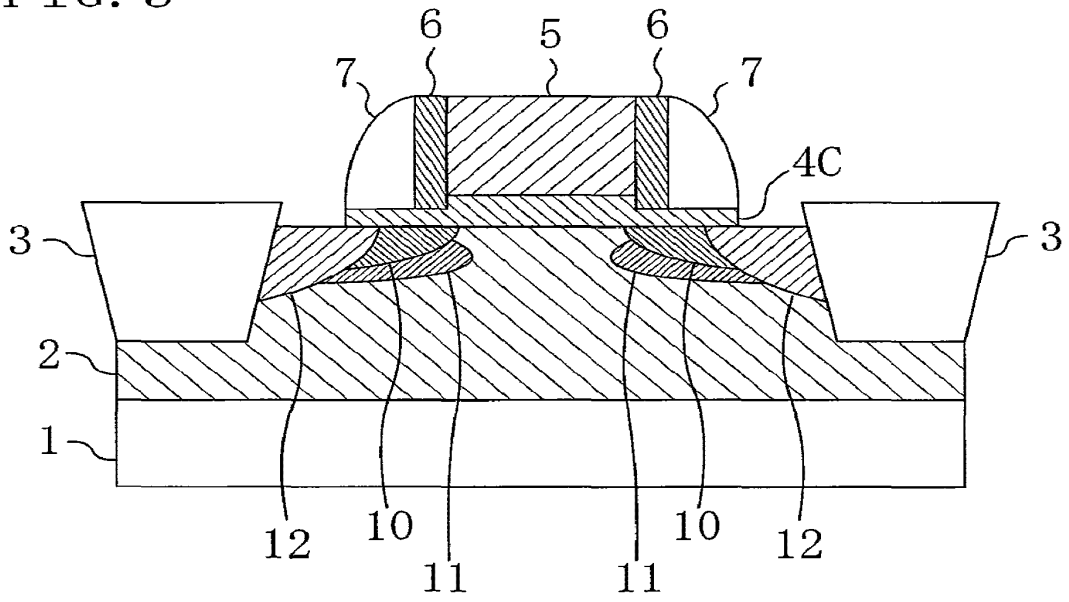
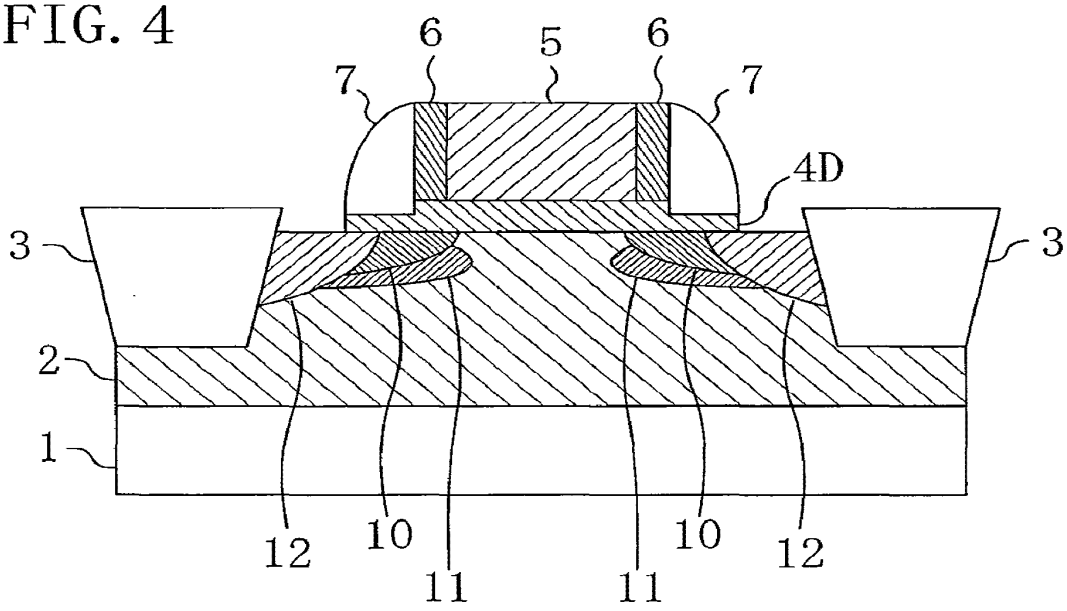


FIG. 4



UMC 1002
UMC v. AICP

FIG. 5

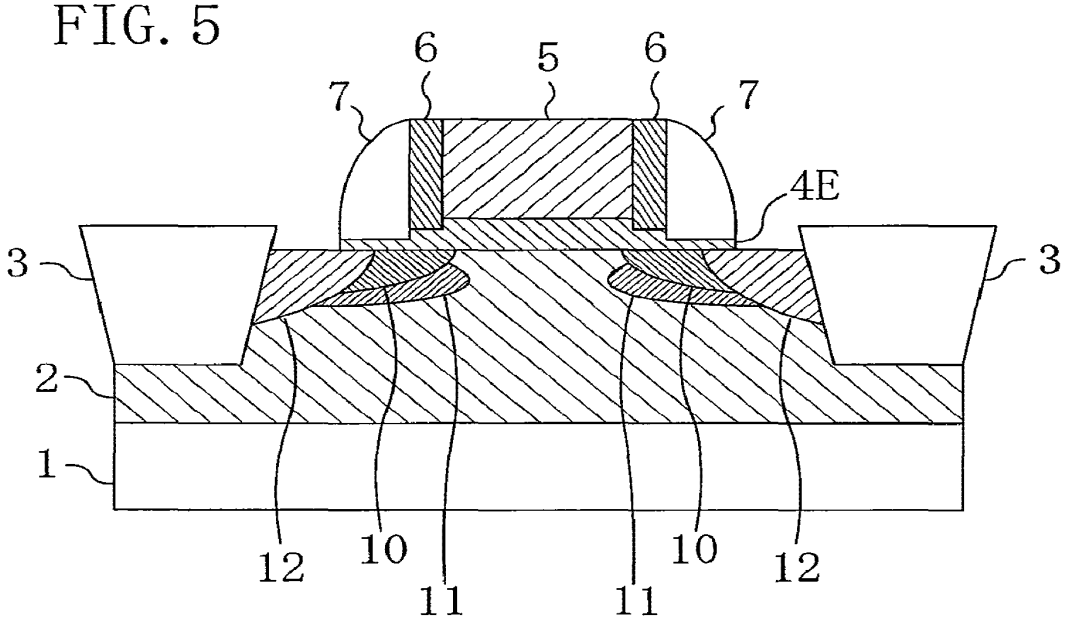
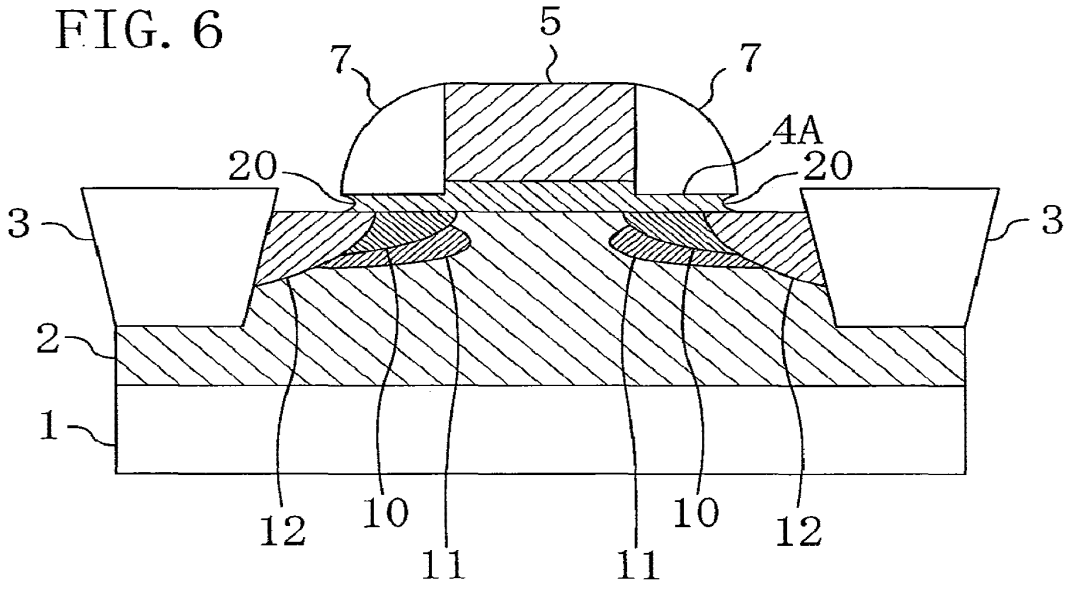


FIG. 6



UMC 1002
UMC v. AICP

FIG. 7

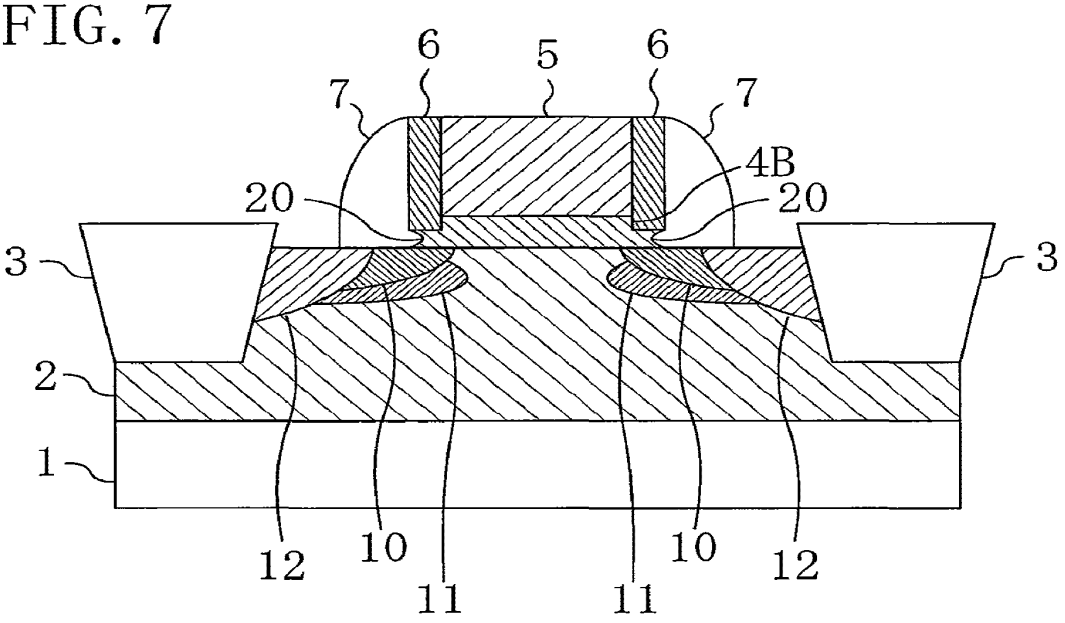
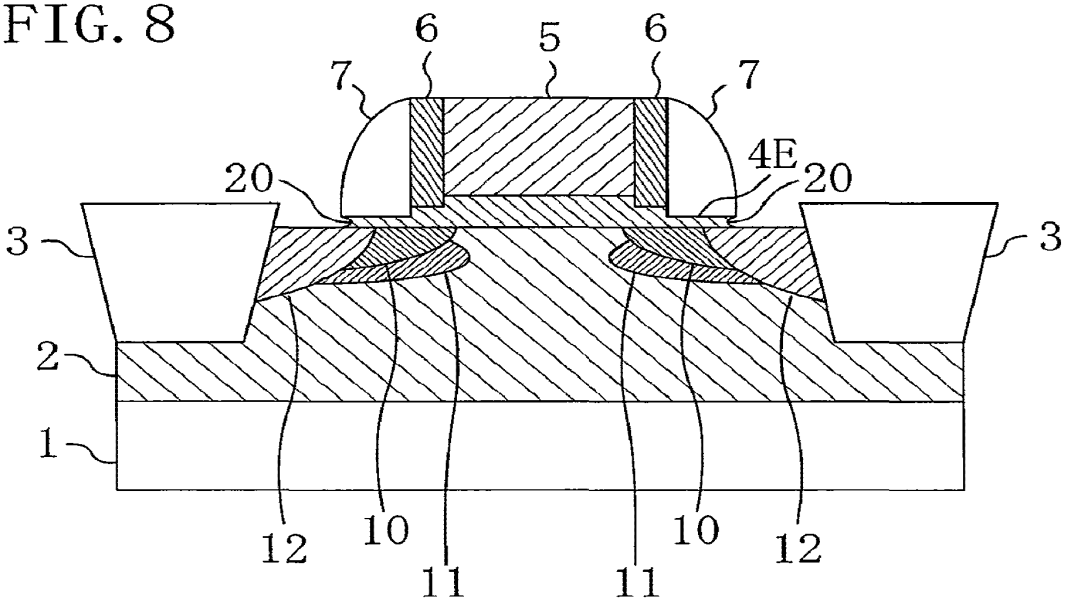


FIG. 8



UMC 1002
UMC v. AICP

FIG. 9

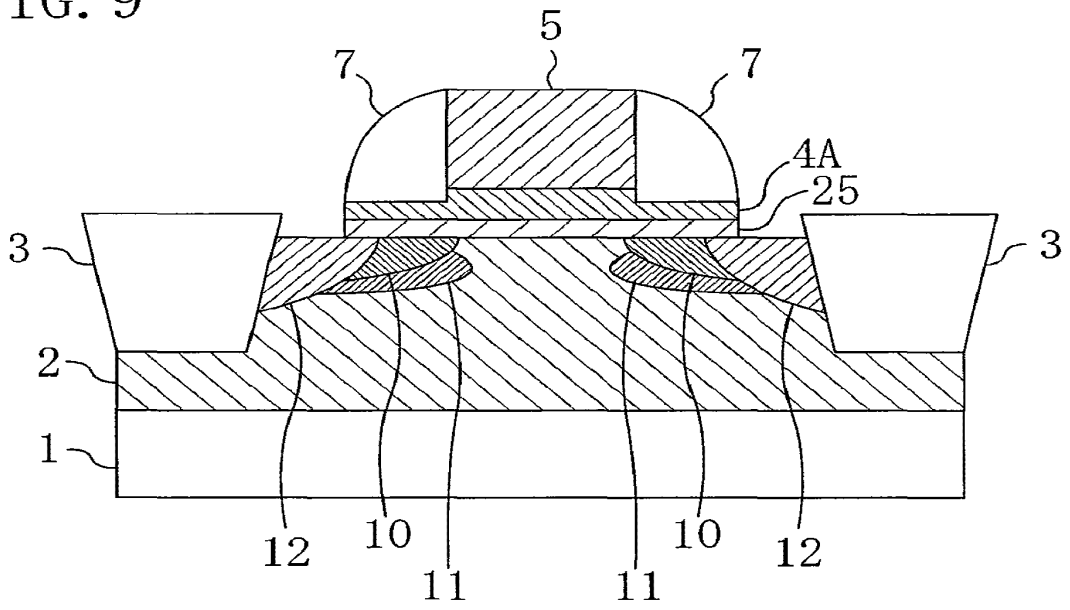
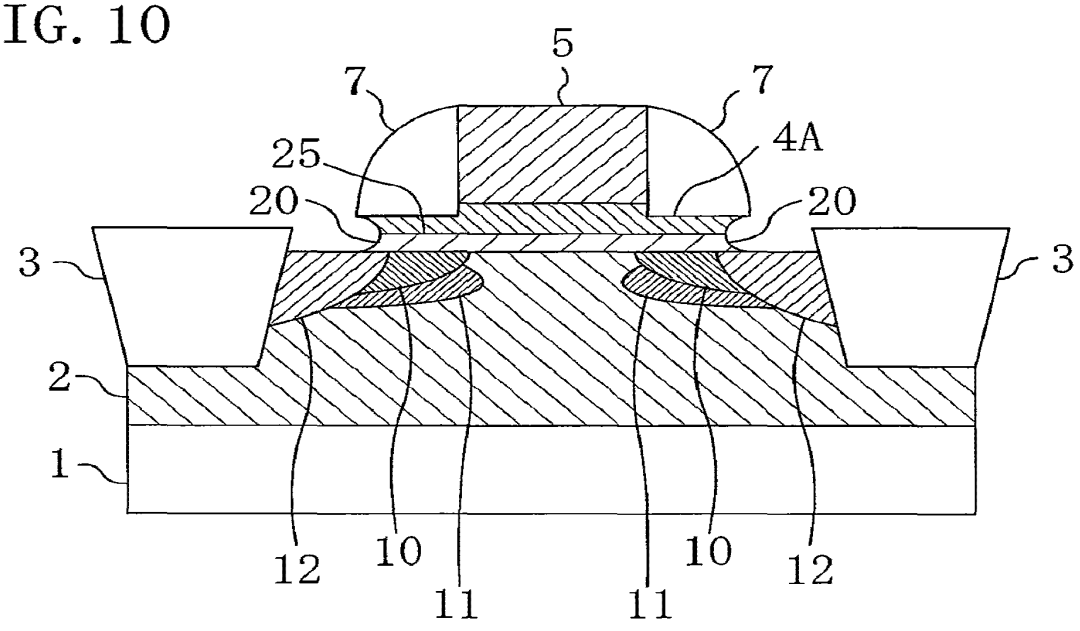


FIG. 10



UMC 1002
UMC v. AICP

FIG. 11A

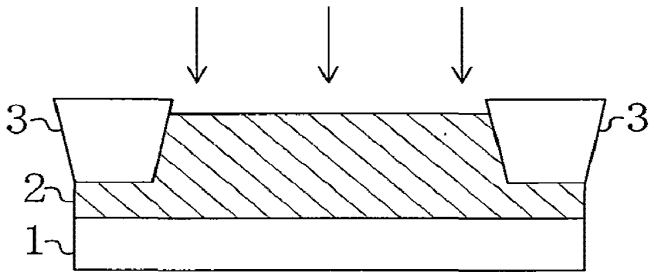


FIG. 11B

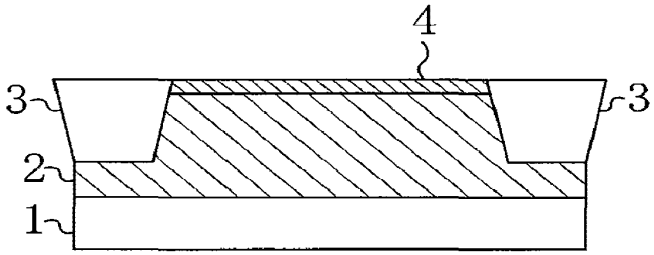


FIG. 11C

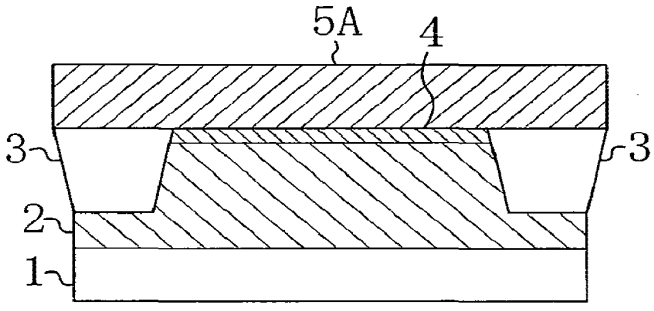


FIG. 11D

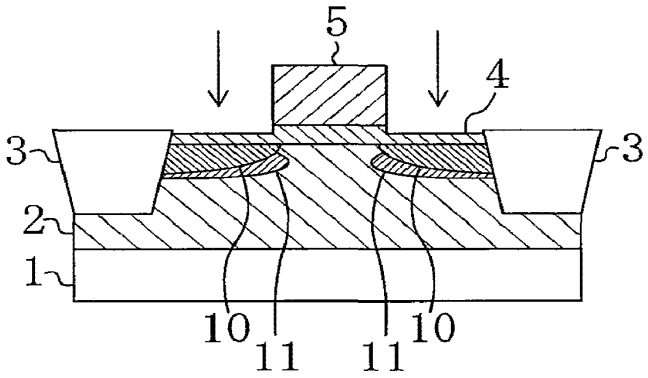


FIG. 11E

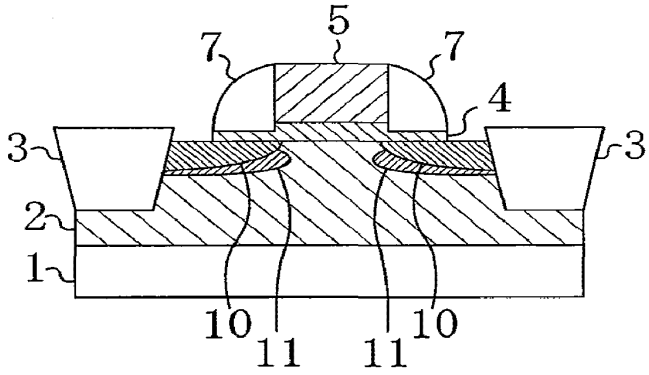
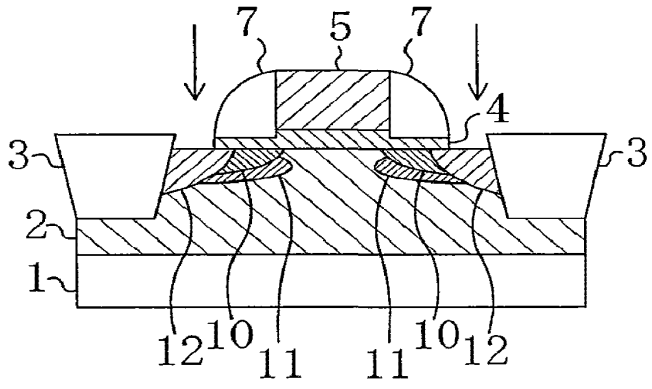


FIG. 11F



UMC 1002
UMC v. AICP

FIG. 12A

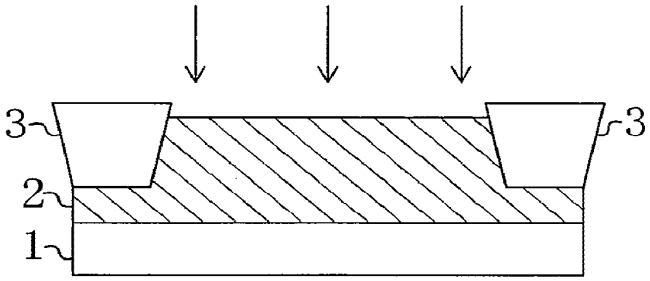


FIG. 12B

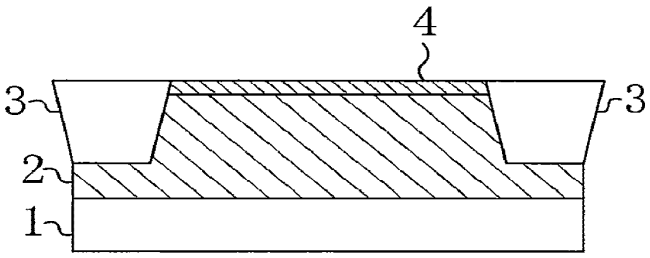


FIG. 12C

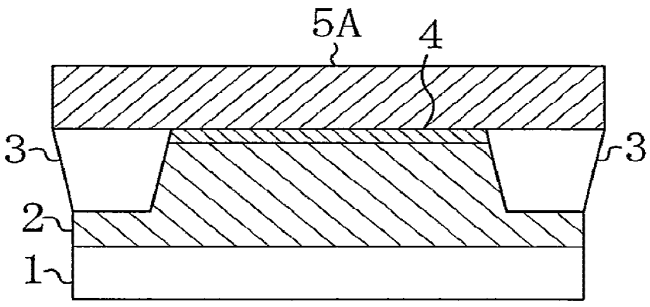


FIG. 12D

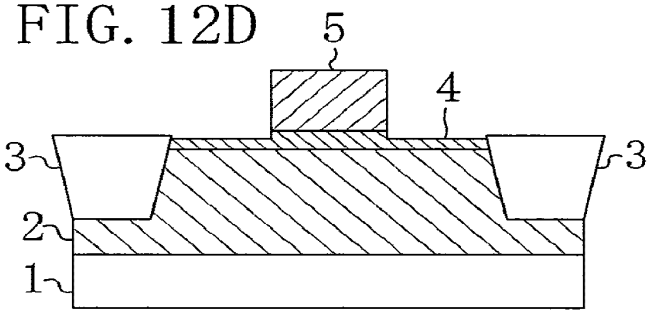


FIG. 12E

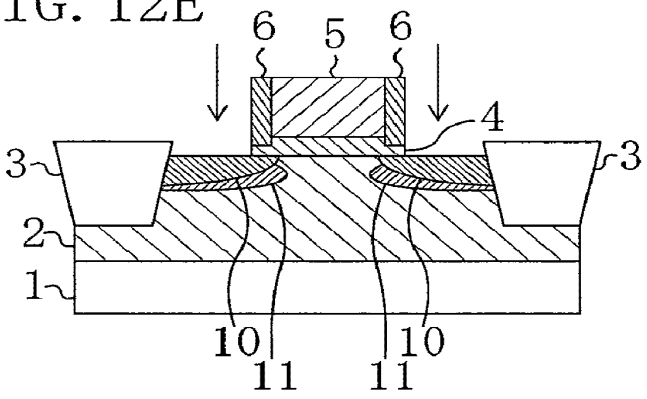


FIG. 12F

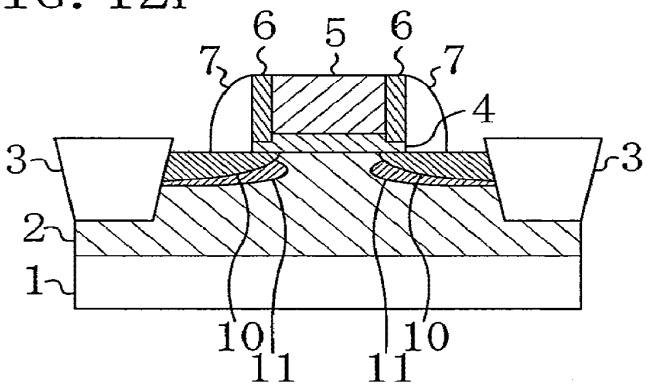
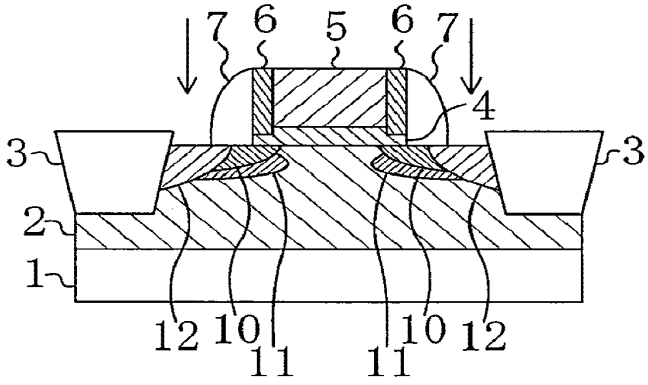


FIG. 12G



UMC 1002
UMC v. AICP

FIG. 13A

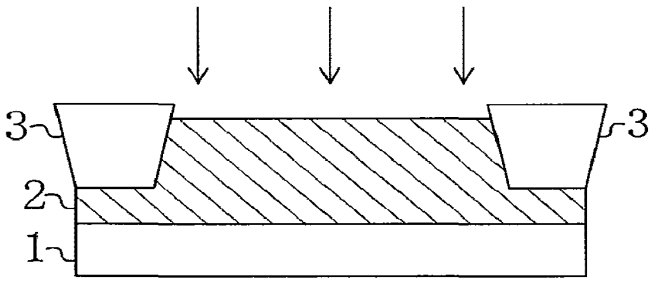


FIG. 13B

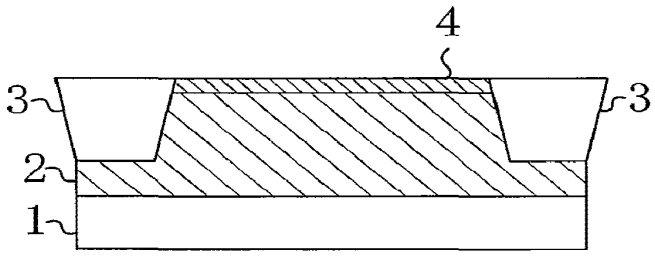


FIG. 13C

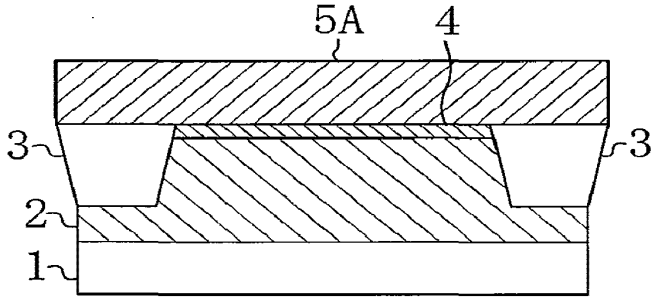


FIG. 13D

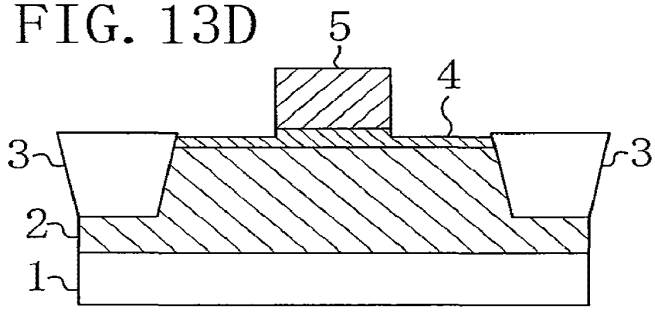


FIG. 13E

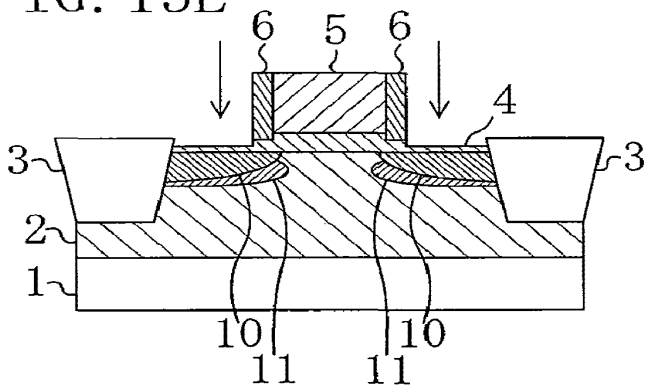


FIG. 13F

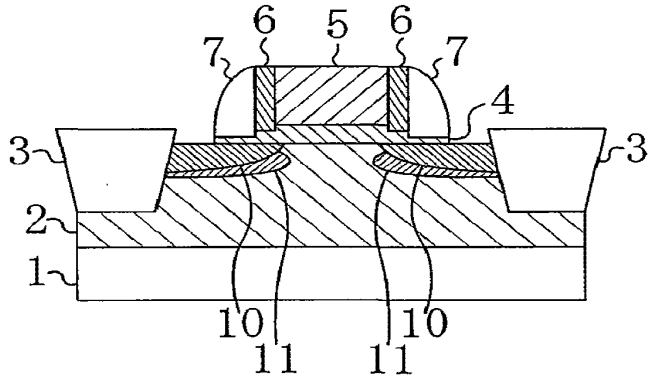
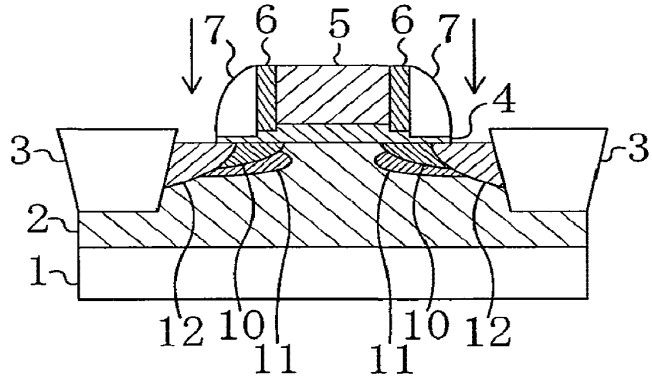


FIG. 13G



UMC 1002
UMC v. AICP

FIG. 14A

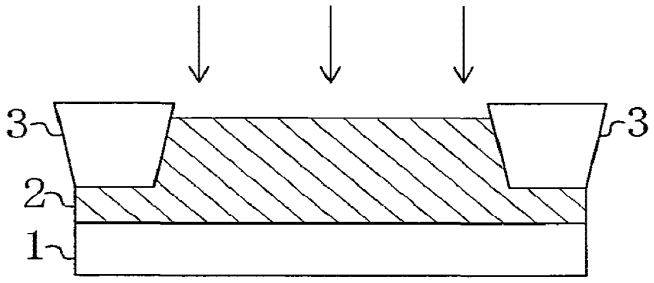


FIG. 14B

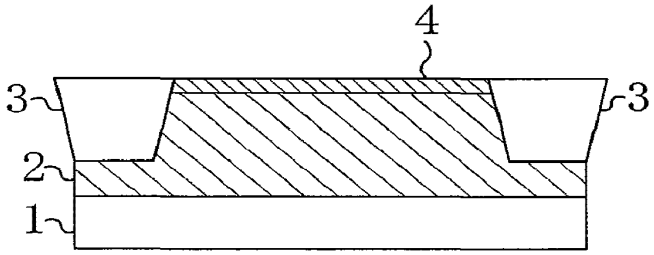


FIG. 14C

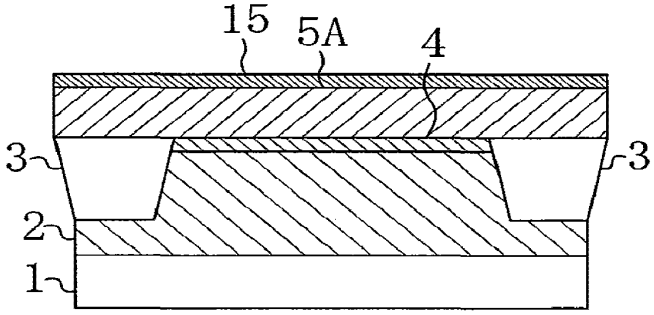


FIG. 14D

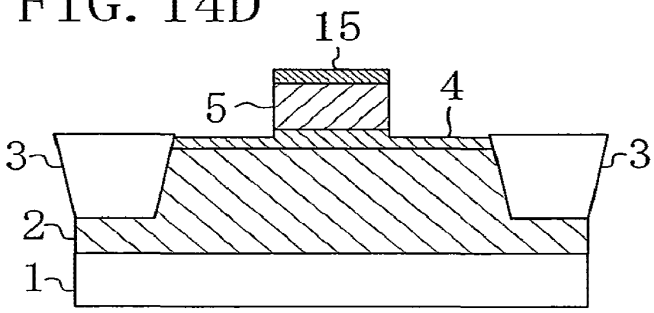


FIG. 14E

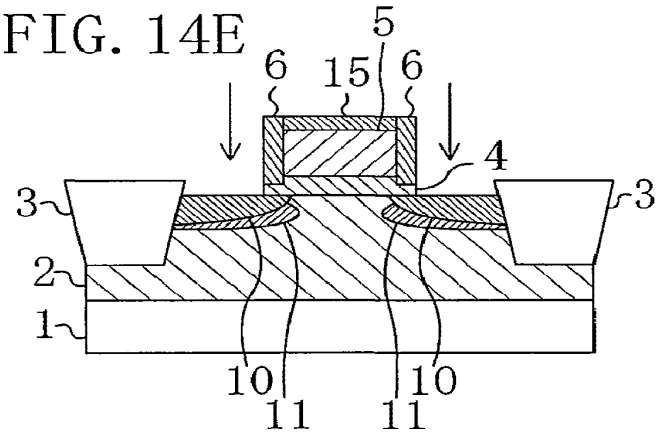


FIG. 14F

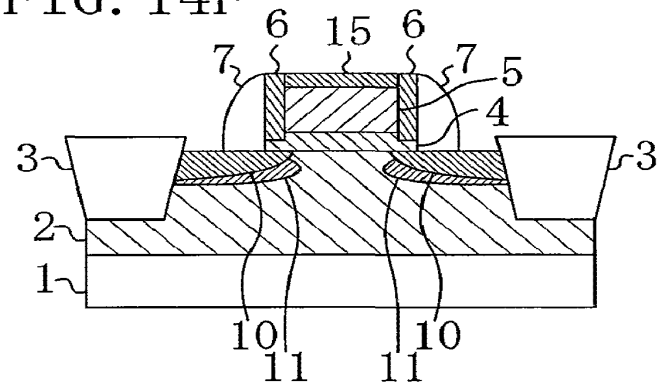
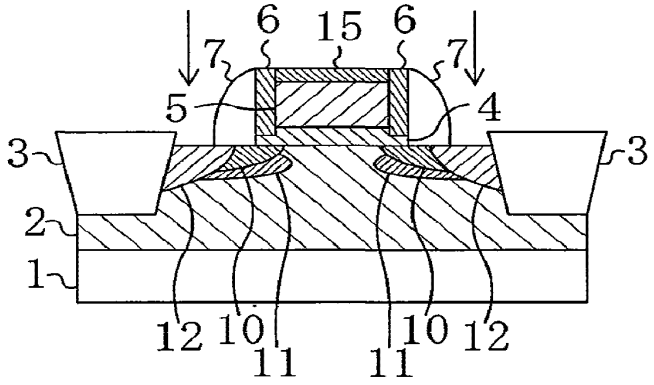


FIG. 14G



UMC 1002
UMC v. AICP

FIG. 15A

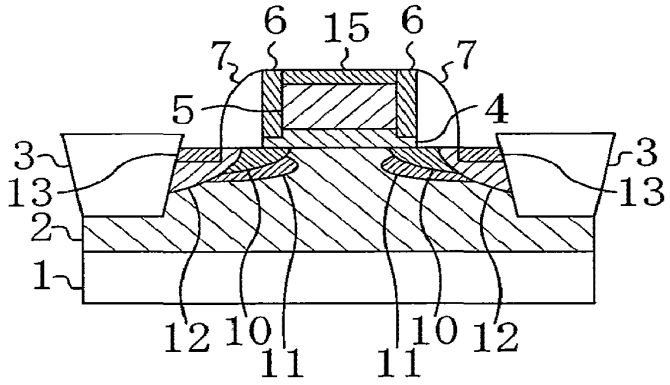


FIG. 15C

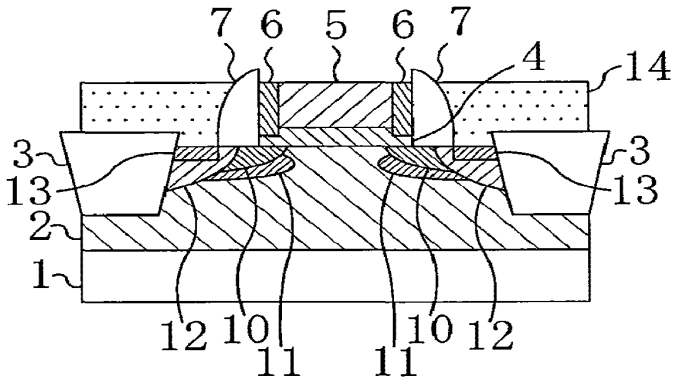


FIG. 15B

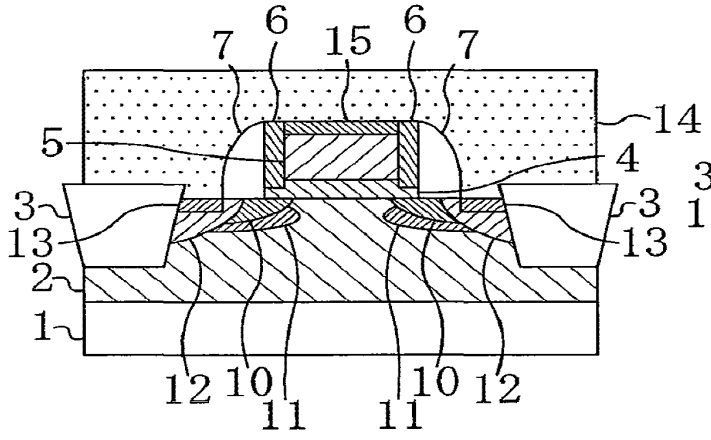
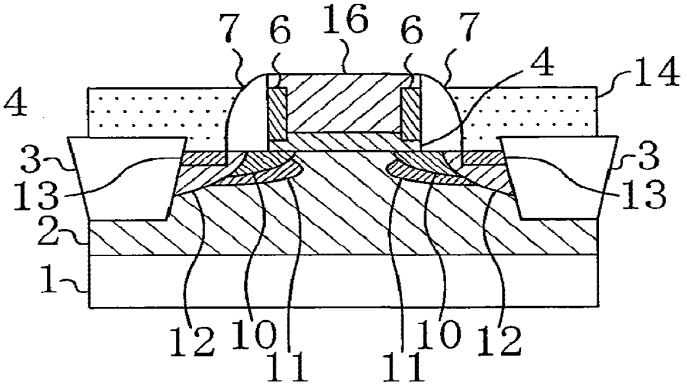


FIG. 15D



UMC 1002
UMC v. AICP

FIG. 16A
PRIOR ART

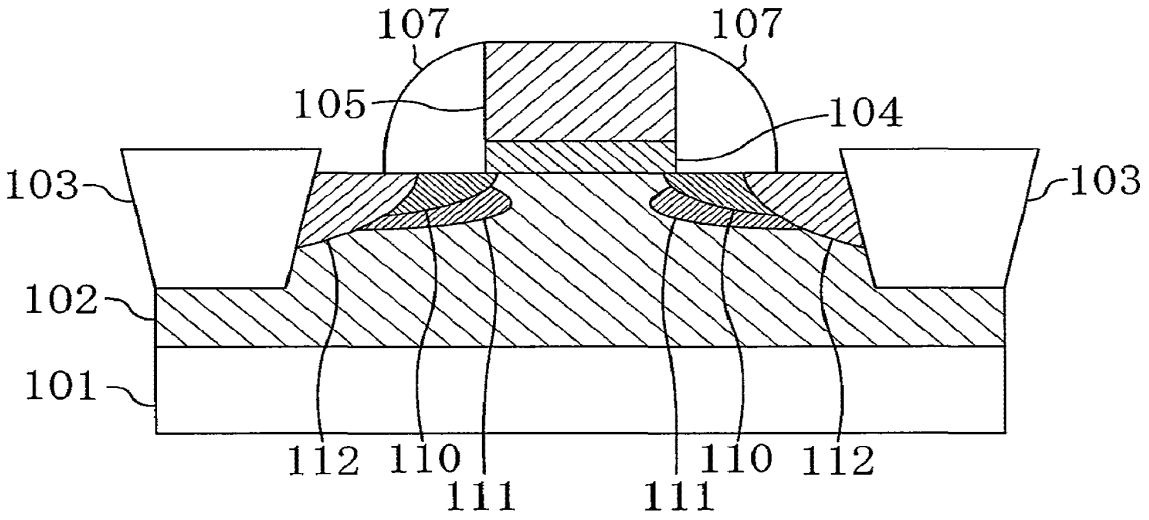
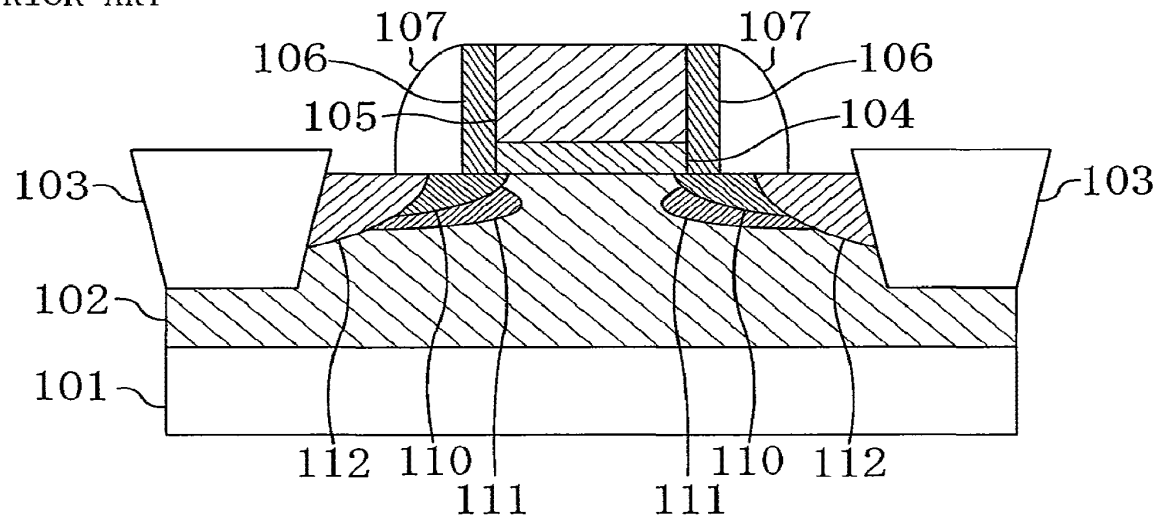


FIG. 16B
PRIOR ART



UMC 1002
UMC v. AICP

Docket No.

DECLARATION AND POWER OF ATTORNEY FOR U.S. PATENT APPLICATION

☒ Original ☐ Supplemental ☐ Substitute ☐ PCT ☐ Design

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; and I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Title: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

which is described and claimed in (if the following box is not checked, the specification of which is attached hereto):

☒ the attached specification, or

☐ the specification in the Application No._____ filed on_____;
and with amendments filed on_____ (if applicable), or

☐ the specification in International Application No. PCT/_____,
filed _____and as amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above.

I acknowledge my duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a-d), §172, or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below, and have also identified below any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NO.	DATE OF FILING	PRIORITY CLAIMED
JAPAN	2005-227457	August 5, 2005	Yes

☐ Additional foreign or international application numbers are listed on a supplemental priority sheet attached hereto.

I hereby claim the benefit under Title 35, United States Code §119(e) of any United States Provisional application(s) listed below.

Number	(Day/Month/Year Filed)

☐ Additional U.S. provisional application numbers are listed on a supplemental priority sheet attached hereto.

Docket No.

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s), or §365(C) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

APPLICATION NO.	U.S. FILING DATE	STATUS: PATENTED, PENDING, ABANDONED

□ Additional U.S. or international application numbers are listed on a supplemental priority sheet attached hereto.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the attorneys and agents associated with U.S. Patent and Trademark Office Customer Number identified bellow to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith, and direct that all correspondence be addressed to that customer number.

I hereby authorize the U.S. attorneys and agents associated with the customer number to accept and follow instructions from Matsushita Electric Industrial Co., Ltd., and any affiliated or subsidiary company thereof, received via their corporate representatives and/or their foreign patent attorneys or agents, if any, as to any action to be taken in the U.S. Patent and Trademark Office regarding this application without direct communication between the U.S. attorneys or agents and myself.

Direct Correspondence to:

CUSTOMER NUMBER 53080

I further declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Full Name of Sole or First Inventor	FIRST NAME	LAST NAME	SIGNATURE	DATE OF SIGNATURE
	Junji	HIRASE	Junji Hirase	May 11, 2006
Residence & Citizenship	**CITY**	**STATE OR COUNTRY**		**COUNTRY OF CITIZENSHIP**
	Osaka	Japan		Japan
Post Office Address	**ADDRESS**	**CITY**	**STATE OR COUNTRY**	**ZIP CODE**
	C/O Matsushita Electric Industrial Co., Ltd., 1006, Oaza Kadoma, Kadoma-shi, Osaka		Japan	571-8501

Full Name of Second Inventor	FIRST NAME	LAST NAME	SIGNATURE	DATE OF SIGNATURE
	Akio	SEBE	Akio Sebe	May. 11, 2006
Residence & Citizenship	**CITY**	**STATE OR COUNTRY**		**COUNTRY OF CITIZENSHIP**
	Osaka	Japan		Japan
Post Office Address	**ADDRESS**	**CITY**	**STATE OR COUNTRY**	**ZIP CODE**
	C/O Matsushita Electric Industrial Co., Ltd., 1006, Oaza Kadoma, Kadoma-shi, Osaka		Japan	571-8501

Docket No.

Full Name of Third Inventor	FIRST NAME	LAST NAME	SIGNATURE	DATE OF SIGNATURE
	Naoki	KOTANI	Naoki Kotani	May, 11, 2006
Residence & Citizenship	**CITY**	**STATE OR COUNTRY**		**COUNTRY OF CITIZENSHIP**
	Hyogo	Japan		Japan
Post Office Address	**ADDRESS**	**CITY**	**STATE OR COUNTRY**	**ZIP CODE**
	C/O Matsushita Electric Industrial Co., Ltd., 1006, Oaza Kadoma, Kadoma-shi, Osaka		Japan	571-8501

Full Name of Fourth Inventor	FIRST NAME	LAST NAME	SIGNATURE	DATE OF SIGNATURE
	Gen	OKAZAKI	Gen Okazaki	May 11. 2006
Residence & Citizenship	**CITY**	**STATE OR COUNTRY**		**COUNTRY OF CITIZENSHIP**
	Hyogo	Japan		Japan
Post Office Address	**ADDRESS**	**CITY**	**STATE OR COUNTRY**	**ZIP CODE**
	C/O Matsushita Electric Industrial Co., Ltd., 1006, Oaza Kadoma, Kadoma-shi, Osaka		Japan	571-8501

Full Name of Fifth Inventor	FIRST NAME	LAST NAME	SIGNATURE	DATE OF SIGNATURE
	Kazuhiko	AIDA	Kazuhiko Aida	May. 18, 2006
Residence & Citizenship	**CITY**	**STATE OR COUNTRY**		**COUNTRY OF CITIZENSHIP**
	Chiba	Japan		Japan
Post Office Address	**ADDRESS**	**CITY**	**STATE OR COUNTRY**	**ZIP CODE**
	C/O Matsushita Electric Industrial Co., Ltd., 1006, Oaza Kadoma, Kadoma-shi, Osaka		Japan	571-8501

Full Name of Sixth Inventor	FIRST NAME	LAST NAME	SIGNATURE	DATE OF SIGNATURE
	Shinji	TAKEOKA	Shinji TAKEOKA	May 11. 2006
Residence & Citizenship	**CITY**	**STATE OR COUNTRY**		**COUNTRY OF CITIZENSHIP**
	Osaka	Japan		Japan
Post Office Address	**ADDRESS**	**CITY**	**STATE OR COUNTRY**	**ZIP CODE**
	C/O Matsushita Electric Industrial Co., Ltd., 1006, Oaza Kadoma, Kadoma-shi, Osaka		Japan	571-8501

Full Name of Seventh Inventor	FIRST NAME	LAST NAME	SIGNATURE	DATE OF SIGNATURE
Residence & Citizenship	**CITY**	**STATE OR COUNTRY**		**COUNTRY OF CITIZENSHIP**
Post Office Address	**ADDRESS**	**CITY**	**STATE OR COUNTRY**	**ZIP CODE**

(If there are more than seven inventors, please add a copy of this page for identification and signature for the additional inventors)

The above application may be more particularly identified as follows:

U.S. Application No. _____ Filing Date _____

Applicant Reference Number P42042-01 Attorney Docket No. _____

UMC 1002
UMC v. AICP

Docket No.: 085393-0808 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Junji HIRASE, et al.	:	Confirmation Number: Not Yet Assigned
Application No.: Divisional of U.S. Serial No. 13/037,831	:	Group Art Unit: Not Yet Assigned
Filed: July 12, 2012	:	Examiner: Not Yet Assigned
For: SEMICONDUCTOR DEVICE	:	

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

UMC 1002
UMC v. AICP

The references were cited by or submitted to the U.S. Patent and Trademark Office in parent application Serial no. 13/037,831, filed on March 1, 2011, which is relied upon for an earlier filing date under 35 USC 120. Thus, copies of these references are not attached. 37 CFR 1.98(d).

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:ksa
Facsimile: 202.756.8087
Date: July 12, 2012

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Substitute for form 1449/PTO)

ATTY. DOCKET NO.	SERIAL NO.
085393-0808	**Divisional of U.S. Serial No. 13/037,831**
APPLICANT: **Junji HIRASE, et al.**	
FILING DATE: **July 12, 2012**	GROUP: **Not Yet Assigned**

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US	7,923,764	04-2011	Hirase et al.	
		US	2004/0227185	11-18-2004	MATSUMOTO et al.	Corresponds w/ JP 2004-241755
		US	6,992,358	01-2006	Hieda et al.	
		US	6,929,992	08-2005	Djomehri et al.	
		US	6,642,071	11-2003	Cheng, Jia-Shyong	
		US	2006/0121740 A2	6/8/2006	SAKAI et al	
		US	2003/0022422 A1	01-30-2003	TORII et al.	
		US	2004/0004234 A1	01-08-2004	YAGISHITA et al.	
		US	2004/0129997 A1	07-08-2004	MORIFUJI	
		US	2005/0121733 A1	06-09-2005	CHEN et al.	
		US	2005/0127436 A1	06-16-2005	HENSON et al.	Corresponds w/ CN 1610129 A
		US	7,579,227	08-2009	Hirase et al.	
		US	2005/0121733	06-2005	Chen et al.	
		US	6,992,358	01-2006	Hieda et al.	

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code3-Number 4-Kind Code5 (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No
		JP 2005-064190	03-10-2005	TOSHIBA CORP		English translation only	
		JP 2004-172178	06-17-2004			X	
		JP 2003-258241	09-12-2003			X	
		CN 1610129 A	04-27-2005		Corresponds w/ US 2005/0127436		
		JP 2004-356576	12-16-2004	SEMICONDUCTOR LEADING EDGE TECHNOLOGIES INC.			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
		WATANABE, Ken, Partial English Translation of "HfSiON-CMOS technology for achieving high performance and high reliability," SEMI FORUM Japan, 2005, IT System & ULSI Technology,	
		HORI, Takashi, "1/4-μm LATID (LArge-Tilt-angle Implanted Drain) TECHNOLOGY FOR 3.3-V OPERATION", CH2637-7/89/0000-0777 1989 IEEE, IEDM 89-777-780-IEDM 89	
		SAYAMA, et al., H.,, "80nm CMOSFET Technology Using Double Offset-Implanted Source/Drain Extension and Low Temperature SiN Process", IEDM 2000, IEDM 00-239-242-IEDM 00	
		U.S. Office Action issued in U.S. Patent Application No. 11/543,865 dated on November 12, 2008	
		Chinese Office Action, with English Translation, issued in Chinese Patent Application No. CN 200610093872.2, dated March 20, 2009.	
		Notice Allowance issued in United States Patent Application No. 13/037,831, mailed April 13, 2012.	
		Notice Allowance issued in United States Patent Application No. 12/505,799, mailed December 13, 2010.	
		Notice Allowance issued in United States Patent Application No. 11/491,260, mailed June 2, 2009.	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Junji HIRASE
Filer:	Michael E. Fogarty/Kayla Adkins
Attorney Docket Number:	085393-0808

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	380	380
Utility Search Fee	1111	1	620	620
Utility Examination Fee	1311	1	250	250
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1250**

Electronic Acknowledgement Receipt

EFS ID:	13240911
Application Number:	13547913
International Application Number:	
Confirmation Number:	2994
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Junji HIRASE
Customer Number:	53080
Filer:	Michael E. Fogarty/Kayla Adkins
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0808
Receipt Date:	12-JUL-2012
Filing Date:	
Time Stamp:	17:44:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1250
RAM confirmation Number	4913
Deposit Account	500417
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

UMC 1002
UMC v. AICP

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	P04204205_TRN_0853930808divisional.pdf	45677 0ec90d5fad935fde027bd7ca8eb0d085c988f874	no	3
Warnings:					
Information:					
2	Preliminary Amendment	P04204205_AMEND-P_0853930808prelimamen.pdf	55927 29e6435baf248adbf98a3809bdafa8dffdc57218	no	6
Warnings:					
Information:					
3		P04204205_SPEC_0853930800spec.pdf	1847452 2ff5ac2e16050ab7c2e8d6edaf687f492079889e	yes	45

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	39
Claims	40	44
Abstract	45	45

Warnings:					
Information:					
4	Drawings-only black and white line drawings	P04204205_DRW_0853930808drawings.pdf	340231 ee32bc694f5904251345166a4c66596ab040fdf9	no	11
Warnings:					
Information:					
5	Oath or Declaration filed	P04204205_DEC_0853930808dec.pdf	164249 92d6f2b2a47c6cac115ddf49290c9a274dad937b	no	3
Warnings:					
Information:					
6	Information Disclosure Statement (IDS) Form (SB08)	P04204205_IDS_0853930808ids.pdf	84457 10b8f704d149f93b0a4057c0f500f26f202ad5bb	no	3
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					

7	Fee Worksheet (SB06)	fee-info.pdf	32968 c1eacc1a2695781513bb17adb880ff93b39e1201	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	2570961	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/547,913	Filing Date 07/12/2012	☐ To be Mailed

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	07/12/2012	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 13	Minus	** 20	= 0	X $ =		OR	X $60=	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $ =		OR	X $250=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	**0**

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/JOY J. DOBBS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/547,913

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	380
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	620
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250
TOTAL CLAIMS (37 CFR 1.16(i))	13 minus 20 =	*			OR	x 60 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 250 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1250

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UMC 1002
UMC v. AICP

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/547,913	07/12/2012	2811	1250	085393-0808	13	1

CONFIRMATION NO. 2994

53080
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

FILING RECEIPT

OC000000055590628

Date Mailed: 07/27/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Junji Hirase, Osaka, JAPAN;
Akio Sebe, Osaka, JAPAN;
Naoki Kotani, Hyogo, JAPAN;
Gen Okazaki, Hyogo, JAPAN;
Kazuhiko Aida, Chiba, JAPAN;
Shinji Takeoka, Osaka, JAPAN;

Assignment For Published Patent Application

Panasonic Corporation, Osaka, JAPAN

Power of Attorney: The patent practitioners associated with Customer Number 53080

Domestic Priority data as claimed by applicant

This application is a DIV of 13/037,831 03/01/2011
which is a DIV of 12/505,799 07/20/2009 PAT 7923764
which is a DIV of 11/491,260 07/24/2006 PAT 7579227

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
JAPAN 2005-227457 08/05/2005

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 07/24/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/547,913**

Projected Publication Date: 11/01/2012

Non-Publication Request: No

Early Publication Request: No
Title

SEMICONDUCTOR DEVICE

Preliminary Class

257

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage, facilitate, and accelerate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

日 本 国 特 許 庁
JAPAN PATENT OFFICE

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed with this Office.

出願年月日 Date of Application:	２００５年　８月　５日
出願番号 Application Number:	特願２００５－２２７４５７
パリ条約による外国への出願に用いる優先権の主張の基礎となる出願の国コードと出願番号 The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is	ＪＰ２００５－２２７４５７
出願人 Applicant(s):	パナソニック株式会社

２０１２年　８月１４日

特許庁長官
Commissioner,
Japan Patent Office　岩井良行

UMC 1002
UMC v. AICP

【書類名】　特許願
【整理番号】　2926470035
【提出日】　平成17年 8月 5日
【あて先】　特許庁長官　殿
【国際特許分類】　H01L 21/76
【発明者】
　【住所又は居所】　大阪府門真市大字門真１００６番地　松下電器産業株式会社内
　【氏名】　平瀬　順司
【発明者】
　【住所又は居所】　大阪府門真市大字門真１００６番地　松下電器産業株式会社内
　【氏名】　瀬部　紹夫
【発明者】
　【住所又は居所】　大阪府門真市大字門真１００６番地　松下電器産業株式会社内
　【氏名】　粉谷　直樹
【発明者】
　【住所又は居所】　大阪府門真市大字門真１００６番地　松下電器産業株式会社内
　【氏名】　岡崎　玄
【発明者】
　【住所又は居所】　大阪府門真市大字門真１００６番地　松下電器産業株式会社内
　【氏名】　相田　和彦
【発明者】
　【住所又は居所】　大阪府門真市大字門真１００６番地　松下電器産業株式会社内
　【氏名】　竹岡　慎治
【特許出願人】
　【識別番号】　000005821
　【氏名又は名称】　松下電器産業株式会社
【代理人】
　【識別番号】　100077931
　【弁理士】
　【氏名又は名称】　前田　弘
【選任した代理人】
　【識別番号】　100094134
　【弁理士】
　【氏名又は名称】　小山　廣毅
　【電話番号】　06-6125-2255
　【連絡先】　担当
【選任した代理人】
　【識別番号】　100110939
　【弁理士】
　【氏名又は名称】　竹内　宏
【選任した代理人】
　【識別番号】　100110940
　【弁理士】
　【氏名又は名称】　嶋田　高久
【選任した代理人】
　【識別番号】　100113262
　【弁理士】
　【氏名又は名称】　竹内　祐二

UMC 1002
UMC v. AICP

【選任した代理人】
　【識別番号】　100115059
　【弁理士】
　【氏名又は名称】　今江　克実
【選任した代理人】
　【識別番号】　100115691
　【弁理士】
　【氏名又は名称】　藤田　篤史
【選任した代理人】
　【識別番号】　100117581
　【弁理士】
　【氏名又は名称】　二宮　克也
【選任した代理人】
　【識別番号】　100117710
　【弁理士】
　【氏名又は名称】　原田　智雄
【選任した代理人】
　【識別番号】　100121728
　【弁理士】
　【氏名又は名称】　井関　勝守
【選任した代理人】
　【識別番号】　100124671
　【弁理士】
　【氏名又は名称】　関　啓
【選任した代理人】
　【識別番号】　100131060
　【弁理士】
　【氏名又は名称】　杉浦　靖也
【手数料の表示】
　【予納台帳番号】　014409
　【納付金額】　16,000円
【提出物件の目録】
　【物件名】　特許請求の範囲　1
　【物件名】　明細書　1
　【物件名】　図面　1
　【物件名】　要約書　1
　【包括委任状番号】　0505962

UMC 1002
UMC v. AICP

【書類名】特許請求の範囲
【請求項１】
基板の活性領域上に形成された高誘電率ゲート絶縁膜と、
前記高誘電率ゲート絶縁膜上に形成されたゲート電極と、
前記ゲート電極の側面に形成された絶縁性サイドウォールとを備え、
前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記絶縁性サイドウォールの下側まで連続的に形成されており、
前記高誘電率ゲート絶縁膜における前記絶縁性サイドウォールの下側領域の少なくとも一部分の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さよりも小さいことを特徴とする半導体装置。
【請求項２】
請求項１に記載の半導体装置において、
前記絶縁性サイドウォールは、前記ゲート電極の側面に形成された第１の絶縁性サイドウォールと、前記ゲート電極の側面に前記第１の絶縁性サイドウォールを介して形成された第２の絶縁性サイドウォールとからなり、
前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第１の絶縁性サイドウォールの下側まで連続的に形成されており、
前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さよりも小さいことを特徴とする半導体装置。
【請求項３】
請求項２に記載の半導体装置において、
前記高誘電率ゲート絶縁膜は前記第２の絶縁性サイドウォールの下側には形成されていないことを特徴とする半導体装置。
【請求項４】
請求項２に記載の半導体装置において、
前記高誘電率ゲート絶縁膜は前記第２の絶縁性サイドウォールの下側まで連続的に形成されており、
前記高誘電率ゲート絶縁膜における前記第２の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さと同等であることを特徴とする半導体装置。
【請求項５】
請求項２に記載の半導体装置において、
前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第２の絶縁性サイドウォールの下側まで連続的に形成されており、
前記高誘電率ゲート絶縁膜における前記第２の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さよりも小さいことを特徴とする半導体装置。
【請求項６】
請求項１に記載の半導体装置において、
前記絶縁性サイドウォールは、前記ゲート電極の側面に形成された第１の絶縁性サイドウォールと、前記ゲート電極の側面に前記第１の絶縁性サイドウォールを介して形成された第２の絶縁性サイドウォールとからなり、
前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第２の絶縁性サイドウォールの下側まで連続的に形成されており、
前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さと同等であり、
前記高誘電率ゲート絶縁膜における前記第２の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さよりも小さいことを特徴とする半導体装置。

UMC 1002
UMC v. AICP

【請求項７】
請求項１～６のいずれか１項に記載の半導体装置において、
前記高誘電率ゲート絶縁膜の側端部にノッチが設けられていることを特徴とする半導体装置。
【請求項８】
請求項１～７のいずれか１項に記載の半導体装置において、
前記基板と前記高誘電率ゲート絶縁膜との間にバッファー絶縁膜が設けられていることを特徴とする半導体装置。
【請求項９】
請求項８に記載の半導体装置において、
前記バッファー絶縁膜はシリコン酸化膜又はシリコン酸窒化膜であることを特徴とする半導体装置。
【請求項１０】
請求項１～９のいずれか１項に記載の半導体装置において、
前記ゲート電極は、全領域がシリサイド化されたフルシリサイドゲート電極であることを特徴とする半導体装置。
【請求項１１】
基板の活性領域上に高誘電率ゲート絶縁膜を形成する工程（ａ）と、
前記高誘電率ゲート絶縁膜上にゲート電極を形成する工程（ｂ）と、
前記工程（ｂ）の後に、前記ゲート電極の外側に位置する前記高誘電率ゲート絶縁膜をエッチングして薄膜化する工程（ｃ）と、
前記工程（ｃ）の後に、前記ゲート電極の側面に絶縁性サイドウォールを形成する工程（ｄ）とを備えていることを特徴とする半導体装置の製造方法。
【請求項１２】
請求項１１に記載の半導体装置の製造方法において、
前記工程（ｄ）の後に、前記絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜を除去する工程を備えていることを特徴とする半導体装置の製造方法。
【請求項１３】
請求項１１に記載の半導体装置の製造方法において、
前記絶縁性サイドウォールは第１の絶縁性サイドウォールと第２の絶縁性サイドウォールとからなり、
前記工程（ｄ）は、前記ゲート電極の側面に前記第１の絶縁性サイドウォールを形成する工程（ｄ１）と、前記ゲート電極の側面に前記第１の絶縁性サイドウォールを介して前記第２の絶縁性サイドウォールを形成する工程（ｄ２）とを含むことを特徴とする半導体装置の製造方法。
【請求項１４】
請求項１３に記載の半導体装置の製造方法において、
前記工程（ｄ１）と前記工程（ｄ２）との間に、前記第１の絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜を除去する工程をさらに備えていることを特徴とする半導体装置の製造方法。
【請求項１５】
請求項１３に記載の半導体装置の製造方法において、
前記工程（ｄ１）と前記工程（ｄ２）との間に、前記第１の絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜をエッチングしてさらに薄膜化する工程を備え、
前記工程（ｄ２）よりも後に、前記第２の絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜を除去する工程をさらに備えていることを特徴とする半導体装置の製造方法。
【請求項１６】
請求項１２、１４又は１５のいずれか１項に記載の半導体装置の製造方法において、
前記高誘電率ゲート絶縁膜の除去は、ウェットエッチングを用いて選択的に行われるこ

UMC 1002
UMC v. AICP

とを特徴とする半導体装置の製造方法。
【請求項１７】
請求項１１～１６のいずれか１項に記載の半導体装置の製造方法において、
前記工程（ｂ）は、前記ゲート電極の上面を覆う保護膜を形成する工程を含み、
前記工程（ｄ）よりも後に、前記絶縁性サイドウォールの外側に位置する前記活性領域の表面をシリサイド化した後、前記保護膜を除去し、その後、前記ゲート電極をフルシリサイド化する工程をさらに備えていることを特徴とする半導体装置の製造方法。
【請求項１８】
請求項１１～１７のいずれか１項に記載の半導体装置の製造方法において、
前記工程（ａ）よりも前に、前記活性領域上にバッファー絶縁膜を形成する工程をさらに備え、
前記工程（ａ）では前記活性領域上に前記バッファー絶縁膜を介して前記高誘電率ゲート絶縁膜を形成することを特徴とする半導体装置の製造方法。

UMC 1002
UMC v. AICP

【書類名】明細書
【発明の名称】半導体装置及びその製造方法
【技術分野】
【０００１】
本発明は、半導体装置及びその製造方法、具体的にはＭＩＳＦＥＴ（metal insulator semiconductor field effect transistor ）の構造及び製造方法に関し、主にＭＩＳＦＥＴの駆動力及び信頼性を向上させる技術に関する。
【背景技術】
【０００２】
近年、半導体集積回路装置の高集積化、高機能化及び高速化に伴ない、スケーリング則に従ってエクステンション（Extension ）の接合深さを浅くすると同時に、ＭＩＳＦＥＴのゲート絶縁膜として比誘電率が４程度のSiO_2系の絶縁膜に代えてＨｆ系酸化物又はＡｌ系酸化物等の比誘電率が１０以上の高誘電率膜を用いようとしている。
【０００３】
図１６（ａ）及び（ｂ）はそれぞれ従来の高誘電率ゲート絶縁膜を使ったＭＩＳＦＥＴの構造を示す断面図である（非特許文献１）。
【０００４】
図１６（ａ）に示すように、基板１０１の活性領域であるウェル１０２におけるＳＴＩ（shallow trench isolation）１０３によって囲まれた領域の上に高誘電率ゲート絶縁膜１０４を介してゲート電極１０５が形成されている。ゲート電極１０５の側面には絶縁性のサイドウォール１０７が形成されている。ウェル１０２におけるサイドウォール１０７の下側にはエクステンション領域１１０が形成されていると共にウェル１０２におけるエクステンション領域１１０の下側にはポケット領域１１１が形成されている。ウェル１０２におけるゲート電極１０５から見てエクステンション領域１１０及びポケット領域１１１の外側にはソース・ドレイン領域１１２が形成されている。
【０００５】
図１６（ｂ）に示す構造が図１６（ａ）に示す構造と異なっている点は、ゲート電極１０５の側面にサイドウォール１０７が絶縁性のオフセットサイドウォール１０６を介して形成されていることである。これにより、ゲート電極１０５とエクステンション領域１１０とのオーバーラップ量の最適化を容易に図ることができる。
【非特許文献１】渡辺健、「高性能・高信頼性を実現する HfSiON-CMOS技術」、Semi. Forum Japan 2005
【非特許文献２】T.Hori、IEDM Tech. Dig. 、1989年、p.777
【非特許文献３】H.Sayama他、IEDM Tech. Dig. 、2000年、p.239
【発明の開示】
【発明が解決しようとする課題】
【０００６】
しかしながら、従来の高誘電率ゲート絶縁膜を使ったＭＩＳＦＥＴの構造においては、高誘電率ゲート絶縁膜の側端部がサイドウォールに直接接しているため、例えばシリコン酸化膜等からなるサイドウォールの形成時に高誘電率ゲート絶縁膜の側端部の組成がSiO_2に近づく等の問題が生じる。その結果、ゲート電極端部において高誘電率ゲート絶縁膜の誘電率低下や絶縁性低下が引き起こされ、それによってデバイス特性やゲート絶縁膜の信頼性が悪化してしまう。
【０００７】
前記に鑑み、本発明は、高誘電率ゲート絶縁膜を劣化させることなくＭＩＳＦＥＴの特性を向上させることを目的とする。
【課題を解決するための手段】
【０００８】
前記の目的を達成するために、本願発明者らは、サイドウォールの下側に高誘電率ゲート絶縁膜を残存させ、それにより高誘電率ゲート絶縁膜の側端部とサイドウォールとの接

UMC 1002
UMC v. AICP

触を防止したＭＩＳＦＥＴ構造及びその製造方法を想到するに至った。ところで、サイドウォールの下側に高誘電率ゲート絶縁膜を残存させた場合には、ゲート・ドレイン間の容量が上昇して回路速度に悪影響が生じる。また、この場合、エクステンション注入やＬＤＤ（lightly doped drain ）注入を実施する際に、高誘電率膜を介在させた状態でイオン注入を行う必要がある。その際、以下の理由によって注入加速エネルギーが高くなるため、注入不純物の深さ方向への拡がりが大きくなってしまい、言い換えると、エクステンションやＬＤＤの接合位置が深くなってしまい、その結果、所望のデバイス特性が得られなくなるという問題が生じる。

【０００９】

理由１）ゲート絶縁膜として高誘電膜を用いる場合、膜厚を薄くしなくても所望の誘電率が得られるため、膜厚が厚く設定される。

【００１０】

理由２）高誘電率膜は重金属を含んでいるため、注入イオン種のＲｐ（Projection Range）が小さくなる。

【００１１】

そこで、本願発明者らは、サイドウォールの下側に高誘電率ゲート絶縁膜を残存させ且つサイドウォール下側の高誘電率ゲート絶縁膜をゲート電極下側の高誘電率ゲート絶縁膜よりも薄く形成したＭＩＳＦＥＴ構造及びその製造方法を想到するに至った。

【００１２】

具体的には、本発明に係る半導体装置は、基板の活性領域上に形成された高誘電率ゲート絶縁膜と、前記高誘電率ゲート絶縁膜上に形成されたゲート電極と、前記ゲート電極の側面に形成された絶縁性サイドウォールとを備え、前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記絶縁性サイドウォールの下側まで連続的に形成されており、前記高誘電率ゲート絶縁膜における前記絶縁性サイドウォールの下側領域の少なくとも一部分の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さよりも小さい。

【００１３】

本発明の半導体装置において、前記絶縁性サイドウォールは、前記ゲート電極の側面に形成された第１の絶縁性サイドウォールと、前記ゲート電極の側面に前記第１の絶縁性サイドウォールを介して形成された第２の絶縁性サイドウォールとからなり、前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第１の絶縁性サイドウォールの下側まで連続的に形成されており、前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さよりも小さくてもよい。

【００１４】

前記絶縁性サイドウォールが前記第１の絶縁性サイドウォールと前記第２の絶縁性サイドウォールとからなる場合、前記高誘電率ゲート絶縁膜は前記第２の絶縁性サイドウォールの下側には形成されていなくてもよい。

【００１５】

前記絶縁性サイドウォールが前記第１の絶縁性サイドウォールと前記第２の絶縁性サイドウォールとからなる場合、前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第２の絶縁性サイドウォールの下側まで連続的に形成されており、前記高誘電率ゲート絶縁膜における前記第２の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さと同等であってもよい。

【００１６】

前記絶縁性サイドウォールが前記第１の絶縁性サイドウォールと前記第２の絶縁性サイドウォールとからなる場合、前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第２の絶縁性サイドウォールの下側まで連続的に形成されており、前記高誘電率ゲート絶縁膜における前記第２の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート

UMC 1002
UMC v. AICP

絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さよりも小さくてもよい。

【００１７】

本発明の半導体装置において、前記絶縁性サイドウォールは、前記ゲート電極の側面に形成された第１の絶縁性サイドウォールと、前記ゲート電極の側面に前記第１の絶縁性サイドウォールを介して形成された第２の絶縁性サイドウォールとからなり、前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第２の絶縁性サイドウォールの下側まで連続的に形成されており、前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さと同等であり、前記高誘電率ゲート絶縁膜における前記第２の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さよりも小さくてもよい。

【００１８】

本発明の半導体装置において、前記高誘電率ゲート絶縁膜の側端部にノッチが設けられていてもよい。

【００１９】

本発明の半導体装置において、前記基板と前記高誘電率ゲート絶縁膜との間にバッファー絶縁膜が設けられていてもよい。この場合、前記バッファー絶縁膜はシリコン酸化膜又はシリコン酸窒化膜であってもよい。

【００２０】

本発明の半導体装置において、前記ゲート電極は、全領域がシリサイド化されたフルシリサイドゲート電極であってもよい。

【００２１】

本発明に係る半導体装置の製造方法は、基板の活性領域上に高誘電率ゲート絶縁膜を形成する工程（ａ）と、前記高誘電率ゲート絶縁膜上にゲート電極を形成する工程（ｂ）と、前記工程（ｂ）の後に、前記ゲート電極の外側に位置する前記高誘電率ゲート絶縁膜をエッチングして薄膜化する工程（ｃ）と、前記工程（ｃ）の後に、前記ゲート電極の側面に絶縁性サイドウォールを形成する工程（ｄ）とを備えている。

【００２２】

本発明の半導体装置の製造方法において、前記工程（ｄ）の後に、前記絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜を除去する工程を備えていてもよい。

【００２３】

本発明の半導体装置の製造方法において、前記絶縁性サイドウォールは第１の絶縁性サイドウォールと第２の絶縁性サイドウォールとからなり、前記工程（ｄ）は、前記ゲート電極の側面に前記第１の絶縁性サイドウォールを形成する工程（ｄ１）と、前記ゲート電極の側面に前記第１の絶縁性サイドウォールを介して前記第２の絶縁性サイドウォールを形成する工程（ｄ２）とを含んでいてもよい。

【００２４】

前記工程（ｄ）が前記工程（ｄ１）と前記工程（ｄ２）とを含む場合、前記工程（ｄ１）と前記工程（ｄ２）との間に、前記第１の絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜を除去する工程をさらに備えていてもよい。

【００２５】

前記工程（ｄ）が前記工程（ｄ１）と前記工程（ｄ２）とを含む場合、前記工程（ｄ１）と前記工程（ｄ２）との間に、前記第１の絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜をエッチングしてさらに薄膜化する工程を備え、前記工程（ｄ２）よりも後に、前記第２の絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜を除去する工程をさらに備えていてもよい。

【００２６】

本発明の半導体装置の製造方法において、前記高誘電率ゲート絶縁膜の除去は、ウェットエッチングを用いて選択的に行われてもよい。

UMC 1002
UMC v. AICP

【００２７】
本発明の半導体装置の製造方法において、前記工程（ｂ）は、前記ゲート電極の上面を覆う保護膜を形成する工程を含み、前記工程（ｄ）よりも後に、前記絶縁性サイドウォールの外側に位置する前記活性領域の表面をシリサイド化した後、前記保護膜を除去し、その後、前記ゲート電極をフルシリサイド化する工程をさらに備えていてもよい。
【００２８】
本発明の半導体装置の製造方法において、前記工程（ａ）よりも前に、前記活性領域上にバッファー絶縁膜を形成する工程をさらに備え、前記工程（ａ）では前記活性領域上に前記バッファー絶縁膜を介して前記高誘電率ゲート絶縁膜を形成してもよい。
【発明の効果】
【００２９】
本発明によると、ゲート電極の下側からサイドウォールの下側まで高誘電率ゲート絶縁膜が連続的に形成されているため、言い換えると、ゲート端部での高誘電率ゲート絶縁膜の連続性が維持されているため、高誘電率ゲート絶縁膜の側端部がサイドウォール膜と直接接することに起因する、ゲート端部での高誘電率ゲート絶縁膜の誘電率低下及び絶縁性低下を抑制することができる。また、サイドウォール下側の高誘電率ゲート絶縁膜をゲート電極下側の高誘電率ゲート絶縁膜よりも薄く形成しているため、ゲート・ドレイン間の容量の上昇を抑制して回路速度への悪影響を低減することができる。さらに、エクステンション注入やＬＤＤ注入を実施する際に介在する高誘電率膜の膜厚が薄いため、注入加速エネルギーの増大を抑制できる。従って、エクステンションやＬＤＤにおいて浅い接合を容易に形成できるので、デバイス特性の向上を図りやすい。
【発明を実施するための最良の形態】
【００３０】
（第１の実施形態）
以下、本発明の第１の実施形態に係る半導体装置について、図面を参照しながら説明する。図１は、第１の実施形態に係る半導体装置（具体的にはシングルサイドウォール型のＭＩＳＦＥＴ）の構造を示す断面図である。尚、本実施形態ではｎ型ＭＩＳＦＥＴを用いて説明するが、本発明をｐ型ＭＩＳＦＥＴに適用した場合にも同様の効果を得ることができる。
【００３１】
図１に示すように、例えばシリコンからなる基板１に形成されたｐ型ウェル２におけるＳＴＩ３によって囲まれた活性領域の上に高誘電率ゲート絶縁膜４Ａを介してゲート電極５が形成されている。ゲート電極５の側面には絶縁性のサイドウォール７が形成されている。ｐ型ウェル２におけるサイドウォール７の下側にはｎ型エクステンション領域１０が形成されていると共にｐ型ウェル２におけるｎ型エクステンション領域１０の下側にはｐ型ポケット領域１１が形成されている。ｐ型ウェル２におけるゲート電極５から見てｎ型エクステンション領域１０及びｐ型ポケット領域１１の外側にはｎ型ソース・ドレイン領域１２が形成されている。
【００３２】
本実施形態の第１の特徴は、ゲート電極５の下側のみならずサイドウォール７の下側にも高誘電率ゲート絶縁膜４Ａが残存していることである。すなわち、高誘電率ゲート絶縁膜４Ａはゲート電極５の下側からサイドウォール７の下側まで連続的に形成されている。
【００３３】
また、本実施形態の第２の特徴は、高誘電率ゲート絶縁膜４Ａにおけるサイドウォール７の下側領域の厚さは、高誘電率ゲート絶縁膜４Ａにおけるゲート電極５の下側領域の厚さよりも小さいことである。すなわち、高誘電率ゲート絶縁膜４Ａは凸型状に形成されている。
【００３４】
本実施形態によると、高誘電率ゲート絶縁膜４Ａの側端部がサイドウォール７と接することなく、ゲート電極５端部での高誘電率ゲート絶縁膜４Ａの連続性が維持されている。

UMC 1002
UMC v. AICP

このため、ゲート電極５端部での高誘電率ゲート絶縁膜４Ａの誘電率低下及び絶縁性低下を抑制することができるので、デバイス特性の低下やゲート絶縁膜信頼性の劣化を防止することができる。

【００３５】

また、本実施形態によると、サイドウォール７の下側に高誘電率ゲート絶縁膜４Ａが存在することによって、ゲート電極５端部近傍ではゲート電極５とｎ型エクステンション領域１０との間の容量結合が強まり、その結果、高いゲート・ドレイン間オーバラップ効果を得ることができる（非特許文献２）。従って、デバイス特性の向上及びホットキャリア信頼性の向上が同時に図れる。

【００３６】

一方、本実施形態においては、サイドウォール７の下側に高誘電率ゲート絶縁膜４Ａが存在することにより、特に、ゲート電極５とｎ型ソース・ドレイン領域１２との間の容量の上昇が発生し、それによって回路速度の低下がもたらされる可能性がある。しかし、前述のように、本実施形態においては、サイドウォール７下側の高誘電率ゲート絶縁膜４Ａをゲート電極５下側の高誘電率ゲート絶縁膜４Ａよりも薄く形成しているため、ゲート・ドレイン間の容量の上昇ひいては回路速度への悪影響を抑制することができる。

【００３７】

以上に説明したように、本実施形態によると、互いにトレードオフの関係にあるデバイス特性・回路特性とゲート絶縁膜信頼性とを共に大きく向上させることができる。

【００３８】

（第１の実施形態の変形例）

以下、本発明の第１の実施形態の変形例に係る半導体装置について、図面を参照しながら説明する。図６は、第１の実施形態の変形例に係る半導体装置（具体的にはシングルサイドウォール型のｎ型ＭＩＳＦＥＴ）の構造を示す断面図である。

【００３９】

本変形例が第１の実施形態と異なっている点は、図６に示すように、サイドウォール７の側端部の下側に位置する高誘電率ゲート絶縁膜４Ａの一部つまり高誘電率ゲート絶縁膜４Ａの側端部をノッチ状に取り除くことにより、ノッチ２０が設けられていることである。

【００４０】

本変形例によると、ゲート電極５とｎ型ソース・ドレイン領域１２との間の容量の上昇に起因する回路速度への悪影響をより一層抑制することができる。

【００４１】

（第２の実施形態）

以下、本発明の第２の実施形態に係る半導体装置について、図面を参照しながら説明する。尚、第１の実施形態がシングルサイドウォール型のＭＩＳＦＥＴを対象としていたのに対して、第２の実施形態は、ゲート電極とエクステンション領域との間のオーバラップ量の最適化を図りやすいダブルサイドウォール型のＭＩＳＦＥＴ（非特許文献３）を対象とする。尚、本実施形態ではｎ型ＭＩＳＦＥＴを用いて説明するが、本発明をｐ型ＭＩＳＦＥＴに適用した場合にも同様の効果を得ることができる。

【００４２】

図２は、第２の実施形態に係る半導体装置の構造を示す断面図である。図２に示すように、例えばシリコンからなる基板１に形成されたｐ型ウェル２におけるＳＴＩ３によって囲まれた活性領域の上に高誘電率ゲート絶縁膜４Ｂを介してゲート電極５が形成されている。ゲート電極５の側面には絶縁性のオフセットサイドウォール６を介して絶縁性のサイドウォール７が形成されている。ｐ型ウェル２におけるオフセットサイドウォール６及びサイドウォール７のそれぞれの下側にはｎ型エクステンション領域１０が形成されていると共にｐ型ウェル２におけるｎ型エクステンション領域１０の下側にはｐ型ポケット領域１１が形成されている。ｐ型ウェル２におけるゲート電極５から見てｎ型エクステンション領域１０及びｐ型ポケット領域１１の外側にはｎ型ソース・ドレイン領域１２が形成さ

UMC 1002
UMC v. AICP

れている。
【００４３】
本実施形態の第１の特徴は、ゲート電極５の下側のみならずオフセットサイドウォール６の下側にも高誘電率ゲート絶縁膜４Ｂが残存していることである。すなわち、高誘電率ゲート絶縁膜４Ｂはゲート電極５の下側からオフセットサイドウォール６の下側まで連続的に形成されている。
【００４４】
また、本実施形態の第２の特徴は、高誘電率ゲート絶縁膜４Ｂにおけるオフセットサイドウォール６の下側領域の厚さは、高誘電率ゲート絶縁膜４Ｂにおけるゲート電極５の下側領域の厚さよりも小さいことである。すなわち、高誘電率ゲート絶縁膜４Ｂは凸型状に形成されている。
【００４５】
本実施形態によると、高誘電率ゲート絶縁膜４Ｂの側端部がオフセットサイドウォール６と接することなく、ゲート電極５端部での高誘電率ゲート絶縁膜４Ｂの連続性が維持されている。このため、ゲート電極５端部での高誘電率ゲート絶縁膜４Ｂの誘電率低下及び絶縁性低下を抑制することができるので、デバイス特性の低下やゲート絶縁膜信頼性の劣化を防止することができる。
【００４６】
また、本実施形態によると、オフセットサイドウォール６の下側に高誘電率ゲート絶縁膜４Ｂが存在することによって、ゲート電極５端部近傍ではゲート電極５とｎ型エクステンション領域１０との間の容量結合が強まり、その結果、高いゲート・ドレイン間オーバラップ効果を得ることができる（非特許文献２）。従って、デバイス特性の向上及びホットキャリア信頼性の向上が同時に図れる。
【００４７】
さらに、本実施形態によると、サイドウォール７の下側には高誘電率ゲート絶縁膜４Ｂが存在しないため、ゲート電極５とｎ型ソース・ドレイン領域１２との間の容量の上昇をさらに小さく抑えることができるので、寄生容量上昇とそれに伴う回路速度への悪影響を最小限に抑制することができる。
【００４８】
以上に説明したように、本実施形態によると、互いにトレードオフの関係にあるデバイス特性・回路特性とゲート絶縁膜信頼性とを共に大きく向上させることができる。
【００４９】
（第２の実施形態の第１変形例）
以下、本発明の第２の実施形態の第１変形例に係る半導体装置について、図面を参照しながら説明する。図７は、第２の実施形態の第１変形例に係る半導体装置（具体的にはダブルサイドウォール型のＭＩＳＦＥＴ）の構造を示す断面図である。
【００５０】
本変形例が第２の実施形態と異なっている点は、図７に示すように、オフセットサイドウォール６の側端部の下側に位置する高誘電率ゲート絶縁膜４Ｂの一部つまり高誘電率ゲート絶縁膜４Ｂの側端部をノッチ状に取り除くことにより、ノッチ２０が設けられていることである。
【００５１】
本変形例によると、ゲート電極５とｎ型ソース・ドレイン領域１２との間の容量の上昇に起因する回路速度への悪影響をより一層抑制することができる。
【００５２】
（第２の実施形態の第２変形例）
以下、本発明の第２の実施形態の第２変形例に係る半導体装置について、図面を参照しながら説明する。図３は、第２の実施形態の第２変形例に係る半導体装置（具体的にはダブルサイドウォール型のＭＩＳＦＥＴ）の構造を示す断面図である。
【００５３】

UMC 1002
UMC v. AICP

本変形例が第２の実施形態と異なっている点は、ゲート電極５の下側及びオフセットサイドウォール６の下側のみならずサイドウォール７の下側にも高誘電率ゲート絶縁膜４Ｃが残存していることである。すなわち、高誘電率ゲート絶縁膜４Ｃはゲート電極５の下側からサイドウォール７の下側まで連続的に形成されている。

【００５４】

尚、本変形例において、サイドウォール７の下側の高誘電率ゲート絶縁膜４Ｃの膜厚は、オフセットサイドウォール６の下側の高誘電率ゲート絶縁膜４Ｃの膜厚と同じである。すなわち、高誘電率ゲート絶縁膜４Ｃは凸型状に形成されている。

【００５５】

本変形例によると、高誘電率ゲート絶縁膜４Ｃがゲート電極５の下側からサイドウォール７の下側まで連続的に形成されているため、オフセットサイドウォール６の幅が非常に薄い場合にも、高誘電率ゲート絶縁膜４Ｃの側端部がサイドウォール７と接することなく、ゲート電極５端部での高誘電率ゲート絶縁膜４Ｃの連続性を維持することができる。このため、ゲート電極５端部での高誘電率ゲート絶縁膜４Ｃの誘電率低下及び絶縁性低下を抑制することができるので、デバイス特性の低下やゲート絶縁膜信頼性の劣化を防止することができる。

【００５６】

但し、本変形例においては、第１の実施形態と同様にサイドウォール７の下側に高誘電率ゲート絶縁膜４Ｃが存在することにより、ゲート電極５とｎ型ソース・ドレイン領域１２との間の容量の上昇が発生する可能性がある。しかし、前述のように、本変形例においては、サイドウォール７下側の高誘電率ゲート絶縁膜４Ｃをゲート電極５下側の高誘電率ゲート絶縁膜４Ｃよりも薄く形成しているため、寄生容量上昇及びそれに伴う回路速度への悪影響を抑制することができる。

【００５７】

（第２の実施形態の第３変形例）

以下、本発明の第２の実施形態の第３変形例に係る半導体装置について、図面を参照しながら説明する。図４は、第２の実施形態の第３変形例に係る半導体装置（具体的にはダブルサイドウォール型のＭＩＳＦＥＴ）の構造を示す断面図である。

【００５８】

本変形例が第２の実施形態と異なっている第１の点は、ゲート電極５の下側及びオフセットサイドウォール６の下側のみならずサイドウォール７の下側にも高誘電率ゲート絶縁膜４Ｄが残存していることである。すなわち、高誘電率ゲート絶縁膜４Ｄはゲート電極５の下側からサイドウォール７の下側まで連続的に形成されている。

【００５９】

本変形例が第２の実施形態と異なっている第２の点は、オフセットサイドウォール６の下側の高誘電率ゲート絶縁膜４Ｄの膜厚が、ゲート電極５の下側の高誘電率ゲート絶縁膜４Ｄの膜厚と同等であることである。尚、サイドウォール７の下側の高誘電率ゲート絶縁膜４Ｄの膜厚は、ゲート電極５の下側の高誘電率ゲート絶縁膜４Ｄの膜厚よりも小さい。すなわち、高誘電率ゲート絶縁膜４Ｄは凸型状に形成されている。

【００６０】

本変形例によると、高誘電率ゲート絶縁膜４Ｄがゲート電極５の下側からサイドウォール７の下側まで連続的に形成されているため、オフセットサイドウォール６の幅が非常に薄い場合にも、高誘電率ゲート絶縁膜４Ｄの側端部がサイドウォール７と接することなく、ゲート電極５端部での高誘電率ゲート絶縁膜４Ｄの連続性を維持することができる。このため、ゲート電極５端部での高誘電率ゲート絶縁膜４Ｄの誘電率低下及び絶縁性低下を抑制することができるので、デバイス特性の低下やゲート絶縁膜信頼性の劣化を防止することができる。

【００６１】

但し、本変形例においては、第１の実施形態と同様にサイドウォール７の下側に高誘電率ゲート絶縁膜４Ｄが存在することにより、ゲート電極５とｎ型ソース・ドレイン領域１

UMC 1002
UMC v. AICP

２との間の容量の上昇が発生する可能性がある。しかし、前述のように、本変形例においては、サイドウォール７下側の高誘電率ゲート絶縁膜４Ｄをゲート電極５下側の高誘電率ゲート絶縁膜４Ｄよりも薄く形成しているため、寄生容量上昇及びそれに伴う回路速度への悪影響を抑制することができる。

【００６２】

（第３の実施形態）

以下、本発明の第３の実施形態に係る半導体装置について、図面を参照しながら説明する。尚、第１の実施形態がシングルサイドウォール型のＭＩＳＦＥＴを対象としていたのに対して、第３の実施形態は、ゲート電極とエクステンション領域との間のオーバラップ量の最適化を図りやすいダブルサイドウォール型のＭＩＳＦＥＴ（非特許文献３）を対象とする。尚、本実施形態ではｎ型ＭＩＳＦＥＴを用いて説明するが、本発明をｐ型ＭＩＳＦＥＴに適用した場合にも同様の効果を得ることができる。

【００６３】

図５は、第３の実施形態に係る半導体装置の構造を示す断面図である。図５に示すように、例えばシリコンからなる基板１に形成されたｐ型ウェル２におけるＳＴＩ３によって囲まれた活性領域の上に高誘電率ゲート絶縁膜４Ｅを介してゲート電極５が形成されている。ゲート電極５の側面には絶縁性のオフセットサイドウォール６を介して絶縁性のサイドウォール７が形成されている。ｐ型ウェル２におけるオフセットサイドウォール６及びサイドウォール７のそれぞれの下側にはｎ型エクステンション領域１０が形成されていると共にｐ型ウェル２におけるｎ型エクステンション領域１０の下側にはｐ型ポケット領域１１が形成されている。ｐ型ウェル２におけるゲート電極５から見てｎ型エクステンション領域１０及びｐ型ポケット領域１１の外側にはｎ型ソース・ドレイン領域１２が形成されている。

【００６４】

本実施形態の第１の特徴は、ゲート電極５の下側のみならずオフセットサイドウォール６及びサイドウォール７のそれぞれの下側にも高誘電率ゲート絶縁膜４Ｅが残存していることである。すなわち、高誘電率ゲート絶縁膜４Ｅはゲート電極５の下側からサイドウォール７の下側まで連続的に形成されている。

【００６５】

また、本実施形態の第２の特徴は、高誘電率ゲート絶縁膜４Ｅにおけるオフセットサイドウォール６の下側領域の厚さが、高誘電率ゲート絶縁膜４Ｅにおけるゲート電極５の下側領域の厚さよりも小さく、且つ高誘電率ゲート絶縁膜４Ｅにおけるサイドウォール７の下側領域の厚さが、高誘電率ゲート絶縁膜４Ｅにおけるオフセットサイドウォール６の下側領域の厚さよりも小さいことである。すなわち、高誘電率ゲート絶縁膜４Ｅは２重凸型状に形成されている。

【００６６】

本実施形態によると、高誘電率ゲート絶縁膜４Ｅがゲート電極５の下側からサイドウォール７の下側まで連続的に形成されているため、オフセットサイドウォール６の幅が非常に薄い場合にも、高誘電率ゲート絶縁膜４Ｅの側端部がサイドウォール７と接することなく、ゲート電極５端部での高誘電率ゲート絶縁膜４Ｅの連続性を維持することができる。このため、ゲート電極５端部での高誘電率ゲート絶縁膜４Ｅの誘電率低下及び絶縁性低下を抑制することができるので、デバイス特性の低下やゲート絶縁膜信頼性の劣化を防止することができる。

【００６７】

また、本実施形態によると、オフセットサイドウォール６の下側に高誘電率ゲート絶縁膜４Ｅが存在することによって、ゲート電極５端部近傍ではゲート電極５とｎ型エクステンション領域１０との間の容量結合が強まり、その結果、高いゲート・ドレイン間オーバラップ効果を得ることができる（非特許文献２）。従って、デバイス特性の向上及びホットキャリア信頼性の向上が同時に図れる。

【００６８】

UMC 1002
UMC v. AICP

一方、本実施形態においては、第１の実施形態と同様にサイドウォール７の下側に高誘電率ゲート絶縁膜４Ｅが存在することにより、ゲート電極５とｎ型ソース・ドレイン領域１２との間の容量の上昇が発生し、その結果、回路速度の低下がもたらされる可能性がある。しかし、前述のように、本実施形態においては、オフセットサイドウォール６下側で高誘電率ゲート絶縁膜４Ｅの膜厚を一旦薄くし且つサイドウォール７下側で高誘電率ゲート絶縁膜４Ｅの膜厚をさらに薄くしているため、寄生容量上昇及びそれに伴う回路速度への悪影響を非常に低く抑制することができる。

【００６９】

以上に説明したように、本実施形態によると、互いにトレードオフの関係にあるデバイス特性・回路特性とゲート絶縁膜信頼性とを共に大きく向上させることができる。

【００７０】

（第３の実施形態の変形例）

以下、本発明の第３の実施形態の変形例に係る半導体装置について、図面を参照しながら説明する。図８は、第３の実施形態の変形例に係る半導体装置（具体的にはダブルサイドウォール型のＭＩＳＦＥＴ）の構造を示す断面図である。

【００７１】

本変形例が第３の実施形態と異なっている点は、図８に示すように、サイドウォール７の側端部の下側に位置する高誘電率ゲート絶縁膜４Ｅの一部、つまり高誘電率ゲート絶縁膜４Ｅの側端部をノッチ状に取り除くことにより、ノッチ２０が設けられていることである。

【００７２】

本変形例によると、ゲート電極５とｎ型ソース・ドレイン領域１２との間の容量の上昇に起因する回路速度への悪影響をより一層抑制することができる。

【００７３】

（第４の実施形態）

以下、本発明の第４の実施形態に係る半導体装置について、図面を参照しながら説明する。図９は、第４の実施形態に係る半導体装置（具体的にはシングルサイドウォール型のＭＩＳＦＥＴ）の構造を示す断面図である。尚、本実施形態ではｎ型ＭＩＳＦＥＴを用いて説明するが、本発明をｐ型ＭＩＳＦＥＴに適用した場合にも同様の効果を得ることができる。

【００７４】

本実施形態が第１の実施形態と異なっている点は、図９に示すように、基板１と高誘電率ゲート絶縁膜４Ａとの間に、例えばシリコン酸化膜又はシリコン酸窒化膜等がバッファー絶縁膜２５として設けられていることである。

【００７５】

本実施形態によると、第１の実施形態の効果に加えて、基板・ゲート絶縁膜界面を正常に保つことができるという効果が得られる。すなわち、基板１上にバッファー絶縁膜２５を介して高誘電率ゲート絶縁膜４Ａを形成することによって、基板１上に高誘電率ゲート絶縁膜４Ａを直接形成した場合と比べて、基板・ゲート絶縁膜界面の劣化を防止することができる。

【００７６】

尚、本実施形態において、第１の実施形態の高誘電率ゲート絶縁膜４Ａと基板１との間にバッファー絶縁膜２５を設けた。しかし、これに代えて、第２の実施形態の高誘電率ゲート絶縁膜４Ｂ、第２の実施形態の第２変形例の高誘電率ゲート絶縁膜４Ｃ、第２の実施形態の第３変形例の高誘電率ゲート絶縁膜４Ｄ又は第３の実施形態の高誘電率ゲート絶縁膜４Ｅと基板１との間にバッファー絶縁膜２５を設けても、本実施形態と同様の効果が得られる。また、高誘電率ゲート絶縁膜４Ａ～４Ｅと基板１との間にバッファー絶縁膜２５を設ける代わりに、ゲート電極５と高誘電率ゲート絶縁膜４Ａ～４Ｅとの間にバッファー絶縁膜を設けてもよい。この構成によれば、高誘電率ゲート絶縁膜４Ａ～４Ｅ上にゲート電極５を直接形成した場合と比べて、ゲート電極・ゲート絶縁膜界面の劣化を防止するこ

UMC 1002
UMC v. AICP

とができる。或いは、高誘電率ゲート絶縁膜４Ａ～４Ｅと基板１との間にバッファー絶縁膜２５を設けると共にゲート電極５と高誘電率ゲート絶縁膜４Ａ～４Ｅとの間にバッファー絶縁膜を設けてもよい。この構成によれば、基板・ゲート絶縁膜界面及びゲート絶縁膜・ゲート電極界面の両方の劣化を防止することができる。

【００７７】

（第４の実施形態の変形例）

以下、本発明の第４の実施形態の変形例に係る半導体装置について、図面を参照しながら説明する。図１０は、第４の実施形態の変形例に係る半導体装置（具体的にはシングルサイドウォール型のＭＩＳＦＥＴ）の構造を示す断面図である。

【００７８】

本変形例が第４の実施形態と異なっている点は、図１０に示すように、サイドウォール７の側端部の下側に位置する高誘電率ゲート絶縁膜４Ａ及びバッファー絶縁膜２５の積層絶縁膜の一部、つまり当該積層絶縁膜の側端部をノッチ状に取り除くことにより、ノッチ２０が設けられていることである。

【００７９】

本変形例によると、ゲート電極５とｎ型ソース・ドレイン領域１２との間の容量の上昇に起因する回路速度への悪影響をより一層抑制することができる。

【００８０】

尚、本変形例において、第１の実施形態の高誘電率ゲート絶縁膜４Ａとバッファー絶縁膜２５との積層絶縁膜の側端部にノッチ２０を設けた。しかし、これに代えて、第２の実施形態の高誘電率ゲート絶縁膜４Ｂ、第２の実施形態の第２変形例の高誘電率ゲート絶縁膜４Ｃ、第２の実施形態の第３変形例の高誘電率ゲート絶縁膜４Ｄ又は第３の実施形態の高誘電率ゲート絶縁膜４Ｅのいずれかとバッファー絶縁膜２５との積層絶縁膜の側端部にノッチを設けても、本変形例と同様の効果が得られる。このとき、高誘電率ゲート絶縁膜４Ａ～４Ｅと基板１との間にバッファー絶縁膜２５を設けると共に、ゲート電極５と高誘電率ゲート絶縁膜４Ａ～４Ｅとの間にもバッファー絶縁膜を設けてもよい。

【００８１】

（第５の実施形態）

以下、本発明の第５の実施形態に係る半導体装置の製造方法について、ｎ型ＭＩＳＦＥＴの製造方法を例として、図面を参照しながら説明する。図１１（ａ）～（ｆ）は、第５の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。

【００８２】

まず、図１１（ａ）に示すように、例えばシリコンからなる基板上１に、素子分離領域となるＳＴＩ３を選択的に形成した後、基板１に対して、例えばＢ（ボロン）を注入エネルギー３００ｋｅＶ、ドーズ量１×１０^{13}ｃｍ$^{-2}$の条件でイオン注入する。これにより、活性領域となるｐ型ウェル２が形成される。続いて、パンチスルーストッパ形成用のイオン注入（注入イオン：Ｂ、注入エネルギー１５０ｋｅＶ、ドーズ量１×１０^{13}ｃｍ$^{-2}$）及びチャネル形成用のイオン注入（注入イオン：Ｂ、注入エネルギー２０ｋｅＶ、ドーズ量５×１０^{12}ｃｍ$^{-2}$）を行う。

【００８３】

次に、図１１（ｂ）に示すように、ｐ型ウェル２におけるＳＴＩ３によって囲まれた活性領域の上に、バッファー絶縁膜として例えば膜厚０．５ｎｍ程度のシリコン酸化膜（図示省略）を形成した後、高誘電率ゲート絶縁膜４として例えば膜厚４ｎｍ程度のＨｆＳｉＯＮ膜（酸化膜換算膜厚は１ｎｍ程度）を堆積する。

【００８４】

次に、図１１（ｃ）に示すように、高誘電率ゲート絶縁膜４上に例えば膜厚１００ｎｍ程度のゲート電極材料膜５Ａを形成する。

【００８５】

次に、ゲート電極材料膜５Ａ上にゲート電極形成領域を覆うレジストパターン（図示省略）を形成した後、当該レジストパターンをマスクとしてゲート電極材料膜５Ａに対して

UMC 1002
UMC v. AICP

エッチングを行って、図１１（ｄ）に示すように、ゲート電極５を形成する。その後、ゲート電極５の外側に位置する高誘電率ゲート絶縁膜４を選択的エッチングによって膜厚２ｎｍ程度除去する。これにより、ゲート電極５の外側に位置する高誘電率ゲート絶縁膜４を残存膜厚２ｎｍ程度まで薄くすることができる。続いて、ゲート電極５をマスクとして基板１に対して、例えばＡｓ（ヒ素）を注入エネルギー２ｋｅＶ、ドーズ量１×１０^{15}ｃｍ$^{-2}$の条件でイオン注入することにより、ｎ型エクステンション領域１０を形成する。その後、ゲート電極５をマスクとして基板１に対して、例えばＢを注入エネルギー１０ｋｅＶ、ドーズ量３×１０^{13}ｃｍ$^{-2}$の条件でイオン注入することにより、ｐ型ポケット領域１１を形成する。ここで、ｐ型ポケット領域１１を形成した後、ｎ型エクステンション領域１０を形成してもよい。

【００８６】

次に、基板１の上に全面に亘って膜厚５０ｎｍ程度の絶縁膜を堆積した後、当該絶縁膜に対してエッチバックを行って、図１１（ｅ）に示すように、ゲート電極５の側面に絶縁性のサイドウォール７を形成する。

【００８７】

次に、ゲート電極５及びサイドウォール７をマスクとして基板１に対して、例えばＡｓを注入エネルギー１０ｋｅＶ、ドーズ量５×１０^{15}ｃｍ$^{-2}$の条件でイオン注入した後、例えば１０５０℃程度の温度でＳＰＩＫＥ　ＲＴＡ（rapid thermal annealing ）を行い、注入不純物を活性化する。これにより、図１１（ｆ）に示すように、ｎ型ソース・ドレイン領域１２が形成される。

【００８８】

以上に説明した本実施形態の製造方法によると、第１の実施形態のＭＩＳＦＥＴ構造（図１参照）を比較的簡単に実現することができる。

【００８９】

ところで、高誘電率ゲート絶縁膜４は重金属を含んでいるため、高誘電率ゲート絶縁膜４を通過する注入イオンのＲｐ（Projection Range ）は小さくなりやすい。従って、図１１（ｄ）に示す工程において、ｎ型エクステンション領域１０又はｐ型ポケット領域１１を形成するために、ゲート電極５の外側において高誘電率ゲート絶縁膜４に覆われた基板１に対してイオン注入する際には、加速エネルギーを大きくする必要がある。しかし、本実施形態ではゲート電極５の外側の高誘電率ゲート絶縁膜４が薄膜化されているため、加速エネルギーの増大を抑制できるので、ｎ型エクステンション領域１０において浅い接合を容易に形成でき、それによりデバイス特性の向上を図りやすい。

【００９０】

尚、本実施形態において、サイドウォール７の形成後に、サイドウォール７の外側に位置する高誘電率ゲート絶縁膜４を、例えばフッ酸を用いたウェットエッチング又は選択ドライエッチングによって除去してもよい。このとき、ウェットエッチングを用いる場合には、サイドウォール７の側端部の下側に位置する高誘電率ゲート絶縁膜４の一部、つまり高誘電率ゲート絶縁膜４の側端部をノッチ状に取り除いてノッチを設けてもよい。このようにすると、第１の実施形態の変形例のＭＩＳＦＥＴ構造（図６参照）を簡単に実現することができる。

【００９１】

また、本実施形態において、ゲート電極５の外側における高誘電率ゲート絶縁膜４の薄膜化の程度は特に限定されるものではないが、高誘電率ゲート絶縁膜４として例えばＨｆＳｉＯＮ膜を用いる場合、ゲート・ドレイン間の容量の上昇を抑制するためには、ゲート電極５の外側の高誘電率ゲート絶縁膜４を膜厚２ｎｍ程度以下に薄膜化する（但し基板１の表面が露出しないように）ことが好ましい。

【００９２】

（第６の実施形態）

以下、本発明の第６の実施形態に係る半導体装置の製造方法について、ｎ型ＭＩＳＦＥＴの製造方法を例として、図面を参照しながら説明する。図１２（ａ）～（ｇ）は、第６

UMC 1002
UMC v. AICP

の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。

【００９３】

まず、図１２（ａ）に示すように、例えばシリコンからなる基板上１に、素子分離領域となるＳＴＩ３を選択的に形成した後、基板１に対して、例えばＢを注入エネルギー３００ｋｅＶ、ドーズ量１×１０^{13}ｃｍ$^{-2}$の条件でイオン注入する。これにより、活性領域となるｐ型ウェル２が形成される。続いて、パンチスルーストッパ形成用のイオン注入（注入イオン：Ｂ、注入エネルギー１５０ｋｅＶ、ドーズ量１×１０^{13}ｃｍ$^{-2}$）及びチャネル形成用のイオン注入（注入イオン：Ｂ、注入エネルギー２０ｋｅＶ、ドーズ量５×１０^{12}ｃｍ$^{-2}$）を行う。

【００９４】

次に、図１２（ｂ）に示すように、ｐ型ウェル２におけるＳＴＩ３によって囲まれた活性領域の上に、バッファー絶縁膜として例えば膜厚０．５ｎｍ程度のシリコン酸化膜（図示省略）を形成した後、高誘電率ゲート絶縁膜４として例えば膜厚４ｎｍ程度のＨｆＳｉＯＮ膜（酸化膜換算膜厚は１ｎｍ程度）を堆積する。

【００９５】

次に、図１２（ｃ）に示すように、高誘電率ゲート絶縁膜４上に例えば膜厚１００ｎｍ程度のゲート電極材料膜５Ａを形成する。

【００９６】

次に、ゲート電極材料膜５Ａ上にゲート電極形成領域を覆うレジストパターン（図示省略）を形成した後、当該レジストパターンをマスクとしてゲート電極材料膜５Ａに対してエッチングを行って、図１２（ｄ）に示すように、ゲート電極５を形成する。その後、ゲート電極５の外側に位置する高誘電率ゲート絶縁膜４を選択的エッチングによって膜厚２ｎｍ程度除去する。これにより、ゲート電極５の外側の高誘電率ゲート絶縁膜４を残存膜厚２ｎｍ程度まで薄くすることができる。

【００９７】

次に、基板１の上に全面に亘って膜厚１０ｎｍ程度の絶縁膜を堆積した後、当該絶縁膜に対してエッチバックを行って、図１２（ｅ）に示すように、ゲート電極５の側面にオフセットサイドウォール６を形成する。その後、オフセットサイドウォール６の外側に位置する高誘電率ゲート絶縁膜４を、例えばフッ酸を用いたウェットエッチング又は選択ドライエッチングによって除去する。続いて、ゲート電極５及びオフセットサイドウォール６をマスクとして基板１に対して、例えばＡｓを注入エネルギー２ｋｅＶ、ドーズ量１×１０^{15}ｃｍ$^{-2}$の条件でイオン注入することにより、ｎ型エクステンション領域１０を形成する。その後、ゲート電極５及びオフセットサイドウォール６をマスクとして基板１に対して、例えばＢを注入エネルギー１０ｋｅＶ、ドーズ量３×１０^{13}ｃｍ$^{-2}$の条件でイオン注入することにより、ｐ型ポケット領域１１を形成する。

【００９８】

次に、基板１の上に全面に亘って膜厚５０ｎｍ程度の絶縁膜を堆積した後、当該絶縁膜に対してエッチバックを行って、図１２（ｆ）に示すように、ゲート電極５の側面にオフセットサイドウォール６を介して絶縁性のサイドウォール７を形成する。

【００９９】

次に、ゲート電極５、オフセットサイドウォール６及びサイドウォール７をマスクとして基板１に対して、例えばＡｓを注入エネルギー１０ｋｅＶ、ドーズ量５×１０^{15}ｃｍ$^{-2}$の条件でイオン注入した後、例えば１０５０℃程度の温度でＳＰＩＫＥ　ＲＴＡを行い、注入不純物を活性化する。これにより、図１２（ｇ）に示すように、ｎ型ソース・ドレイン領域１２が形成される。

【０１００】

以上に説明した本実施形態の製造方法によると、第２の実施形態のＭＩＳＦＥＴ構造（図２参照）を比較的簡単に実現することができる。

【０１０１】

尚、本実施形態において、オフセットサイドウォール６の形成後に、オフセットサイド

UMC 1002
UMC v. AICP

ウォール６の外側に位置する高誘電率ゲート絶縁膜４を、例えばフッ酸を用いたウェットエッチングによって除去する際に、オフセットサイドウォール６の側端部の下側に位置する高誘電率ゲート絶縁膜４の一部、つまり高誘電率ゲート絶縁膜４の側端部をノッチ状に取り除いてノッチを設けてもよい。このようにすると、第２の実施形態の第１変形例のＭＩＳＦＥＴ構造（図７参照）を簡単に実現することができる。

【０１０２】

また、本実施形態において、ゲート電極５の外側における高誘電率ゲート絶縁膜４の薄膜化の程度は特に限定されるものではないが、高誘電率ゲート絶縁膜４として例えばＨｆＳｉＯＮ膜を用いる場合、ゲート・ドレイン間の容量の上昇を抑制するためには、ゲート電極５の外側の高誘電率ゲート絶縁膜４を膜厚２ｎｍ程度以下に薄膜化する（但し基板１の表面が露出しないように）ことが好ましい。

【０１０３】

また、本実施形態において、オフセットサイドウォール６を形成した後、オフセットサイドウォール６の外側に位置する高誘電率ゲート絶縁膜４を除去し、その後、ｎ型エクステンション領域１０及びｐ型ポケット領域１１を形成するためのイオン注入を行った。しかし、これに代えて、オフセットサイドウォール６を形成した後、オフセットサイドウォール６の外側に薄膜化した高誘電率ゲート絶縁膜４を残存させた状態でｎ型エクステンション領域１０及びｐ型ポケット領域１１を形成するためのイオン注入を行ってもよい。このようにしても、本実施形態ではオフセットサイドウォール６の外側に位置する高誘電率ゲート絶縁膜４が薄膜化されているため、加速エネルギーの増大を抑制できるので、ｎ型エクステンション領域１０において浅い接合を容易に形成でき、それによりデバイス特性の向上を図りやすい。また、この場合、ｎ型エクステンション領域１０及びｐ型ポケット領域１１を形成するためのイオン注入を行った後、オフセットサイドウォール６の外側に位置する高誘電率ゲート絶縁膜４を除去し、その後、同一基板上における他のチャネル型又は別の電源系のＭＩＳＦＥＴのエクステンション領域及びポケット領域を形成するためのイオン注入を行ってもよい。

【０１０４】

（第７の実施形態）

以下、本発明の第７の実施形態に係る半導体装置の製造方法について、ｎ型ＭＩＳＦＥＴの製造方法を例として、図面を参照しながら説明する。図１３（ａ）～（ｇ）は、第７の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。

【０１０５】

まず、図１３（ａ）に示すように、例えばシリコンからなる基板上１に、素子分離領域となるＳＴＩ３を選択的に形成した後、基板１に対して、例えばＢを注入エネルギー３００ｋｅＶ、ドーズ量$1\times10^{13}cm^{-2}$の条件でイオン注入する。これにより、活性領域となるｐ型ウェル２が形成される。続いて、パンチスルーストッパ形成用のイオン注入（注入イオン：Ｂ、注入エネルギー１５０ｋｅＶ、ドーズ量$1\times10^{13}cm^{-2}$）及びチャネル形成用のイオン注入（注入イオン：Ｂ、注入エネルギー２０ｋｅＶ、ドーズ量$5\times10^{12}cm^{-2}$）を行う。

【０１０６】

次に、図１３（ｂ）に示すように、ｐ型ウェル２におけるＳＴＩ３によって囲まれた活性領域の上に、バッファー絶縁膜として例えば膜厚０．５ｎｍ程度のシリコン酸化膜（図示省略）を形成した後、高誘電率ゲート絶縁膜４として例えば膜厚４ｎｍ程度のＨｆＳｉＯＮ膜（酸化膜換算膜厚は１ｎｍ程度）を堆積する。

【０１０７】

次に、図１３（ｃ）に示すように、高誘電率ゲート絶縁膜４上に例えば膜厚１００ｎｍ程度のゲート電極材料膜５Ａを形成する。

【０１０８】

次に、ゲート電極材料膜５Ａ上にゲート電極形成領域を覆うレジストパターン（図示省略）を形成した後、当該レジストパターンをマスクとしてゲート電極材料膜５Ａに対して

UMC 1002
UMC v. AICP

エッチングを行って、図１３（ｄ）に示すように、ゲート電極５を形成する。その後、ゲート電極５の外側に位置する高誘電率ゲート絶縁膜４を選択的エッチングによって膜厚２ｎｍ程度除去する。これにより、ゲート電極５の外側の高誘電率ゲート絶縁膜４を残存膜厚２ｎｍ程度まで薄くすることができる。

【０１０９】

次に、基板１の上に全面に亘って膜厚５ｎｍ程度の絶縁膜を堆積した後、当該絶縁膜に対してエッチバックを行って、図１３（ｅ）に示すように、ゲート電極５の側面に絶縁性のオフセットサイドウォール６を形成する。その後、ゲート電極５及びオフセットサイドウォール６により被覆されていない高誘電率ゲート絶縁膜４をさらに膜厚１ｎｍ程度除去する。これにより、オフセットサイドウォール６の外側に位置する高誘電率ゲート絶縁膜４を残存膜厚１ｎｍ程度まで薄くすることができる。その後、ゲート電極５及びオフセットサイドウォール６をマスクとして基板１に対して、例えばＡｓを注入エネルギー２ｋｅＶ、ドーズ量１×１０^{15}ｃｍ$^{-2}$の条件でイオン注入することにより、ｎ型エクステンション領域１０を形成する。その後、ゲート電極５及びオフセットサイドウォール６をマスクとして基板１に対して、例えばＢを注入エネルギー１０ｋｅＶ、ドーズ量３×１０^{13}ｃｍ$^{-2}$の条件でイオン注入することにより、ｐ型ポケット領域１１を形成する。

【０１１０】

次に、基板１の上に全面に亘って膜厚５０ｎｍ程度の絶縁膜を堆積した後、当該絶縁膜に対してエッチバックを行って、図１３（ｆ）に示すように、ゲート電極５の側面にオフセットサイドウォール６を介して絶縁性のサイドウォール７を形成する。

【０１１１】

次に、ゲート電極５、オフセットサイドウォール６及びサイドウォール７をマスクとして基板１に対して、例えばＡｓを注入エネルギー１０ｋｅＶ、ドーズ量５×１０^{15}ｃｍ$^{-2}$の条件でイオン注入した後、例えば１０５０℃程度の温度でＳＰＩＫＥ　ＲＴＡを行い、注入不純物を活性化する。これにより、図１３（ｇ）に示すように、ｎ型ソース・ドレイン領域１２が形成される。

【０１１２】

以上に説明した本実施形態の製造方法によると、第３の実施形態のＭＩＳＦＥＴ構造（図５参照）を比較的簡単に実現することができる。

【０１１３】

また、本実施形態においては、オフセットサイドウォール６下側で高誘電率ゲート絶縁膜４Ｅの膜厚を一旦薄くし且つオフセットサイドウォール６の外側の高誘電率ゲート絶縁膜４Ｅの膜厚をさらに薄くしている。このため、ゲート電極５及びオフセットサイドウォール６をマスクとして、ｎ型エクステンション領域１０を形成するためのイオン注入を行う際にも、加速エネルギーの増大を最小限に抑制できるので、ｎ型エクステンション領域１０においてさらに浅い接合を容易に形成でき、それによりデバイス特性の向上を図りやすい。

【０１１４】

尚、本実施形態において、サイドウォール７の形成後に、サイドウォール７の外側に位置する高誘電率ゲート絶縁膜４を、例えばフッ酸を用いたウェットエッチング又は選択ドライエッチングによって除去してもよい。また、この際に、サイドウォール７端部の高誘電率ゲート絶縁膜４つまり高誘電率ゲート絶縁膜４の側端部をノッチ状に取り除いてもよい。このようにすると、第３の実施形態の変形例のＭＩＳＦＥＴ構造（図８参照）を簡単に実現することができる。

【０１１５】

また、本実施形態において、ゲート電極５の外側における高誘電率ゲート絶縁膜４の薄膜化の程度は、オフセットサイドウォール６の下側においてもサイドウォール７の下側においても特に限定されるものではない。しかし、高誘電率ゲート絶縁膜４として例えばＨｆＳｉＯＮ膜を用いる場合、ゲート・ドレイン間の容量の上昇を抑制するためには、ゲート電極５の外側の高誘電率ゲート絶縁膜４を膜厚２ｎｍ程度以下に薄膜化することが好ま

UMC 1002
UMC v. AICP

しい。

【０１１６】

（第８の実施形態）

以下、本発明の第８の実施形態に係る半導体装置の製造方法について、ｎ型ＭＩＳＦＥＴの製造方法を例として、図面を参照しながら説明する。図１４（ａ）～（ｇ）及び図１５（ａ）～（ｄ）は、第８の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。

【０１１７】

まず、図１４（ａ）に示すように、例えばシリコンからなる基板上１に、素子分離領域となるＳＴＩ３を選択的に形成した後、基板１に対して、例えばＢを注入エネルギー３００ｋｅＶ、ドーズ量１×１０^{13}ｃｍ$^{-2}$の条件でイオン注入する。これにより、活性領域となるｐ型ウェル２が形成される。続いて、パンチスルーストッパ形成用のイオン注入（注入イオン：Ｂ、注入エネルギー１５０ｋｅＶ、ドーズ量１×１０^{13}ｃｍ$^{-2}$）及びチャネル形成用のイオン注入（注入イオン：Ｂ、注入エネルギー２０ｋｅＶ、ドーズ量５×１０^{12}ｃｍ$^{-2}$）を行う。

【０１１８】

次に、図１４（ｂ）に示すように、ｐ型ウェル２におけるＳＴＩ３によって囲まれた活性領域の上に、バッファー絶縁膜として例えば膜厚０．５ｎｍ程度のシリコン酸化膜（図示省略）を形成した後、高誘電率ゲート絶縁膜４として例えば膜厚４ｎｍ程度のＨｆＳｉＯＮ膜（酸化膜換算膜厚は１ｎｍ程度）を堆積する。

【０１１９】

次に、図１４（ｃ）に示すように、高誘電率ゲート絶縁膜４上にゲート電極材料膜５Ａとして例えば膜厚１００ｎｍ程度のポリシリコン膜を形成した後、ゲート電極材料膜５Ａの上にカバー膜（保護膜）１５として例えば膜厚１０ｎｍ程度のシリコン酸化膜を堆積する。

【０１２０】

次に、カバー膜１５上にゲート電極形成領域を覆うレジストパターン（図示省略）を形成した後、当該レジストパターンをマスクとしてカバー膜１５及びゲート電極材料膜５Ａに対して順次エッチングを行って、図１４（ｄ）に示すように、カバー膜１５により上面が覆われたゲート電極５を形成する。その後、ゲート電極５の外側に位置する高誘電率ゲート絶縁膜４を選択的エッチングによって膜厚２ｎｍ程度除去する。これにより、ゲート電極５の外側の高誘電率ゲート絶縁膜４を残存膜厚２ｎｍ程度まで薄くすることができる。

【０１２１】

次に、基板１の上に全面に亘って膜厚１０ｎｍ程度の絶縁膜を堆積した後、当該絶縁膜に対してエッチバックを行って、図１４（ｅ）に示すように、ゲート電極５の側面にオフセットサイドウォール６を形成する。その後、オフセットサイドウォール６の外側に位置する高誘電率ゲート絶縁膜４を、例えばフッ酸を用いたウェットエッチング又は選択ドライエッチングによって除去する。続いて、ゲート電極５及びオフセットサイドウォール６をマスクとして基板１に対して、例えばＡｓを注入エネルギー２ｋｅＶ、ドーズ量１×１０^{15}ｃｍ$^{-2}$の条件でイオン注入することにより、ｎ型エクステンション領域１０を形成する。その後、ゲート電極５及びオフセットサイドウォール６をマスクとして基板１に対して、例えばＢを注入エネルギー１０ｋｅＶ、ドーズ量３×１０^{13}ｃｍ$^{-2}$の条件でイオン注入することにより、ｐ型ポケット領域１１を形成する。

【０１２２】

次に、基板１の上に全面に亘って膜厚５０ｎｍ程度の絶縁膜（例えばＳｉＮ膜）を堆積した後、当該絶縁膜に対してエッチバックを行って、図１４（ｆ）に示すように、ゲート電極５の側面にオフセットサイドウォール６を介して絶縁性のサイドウォール７を形成する。

【０１２３】

UMC 1002
UMC v. AICP

次に、ゲート電極５、オフセットサイドウォール６及びサイドウォール７をマスクとして基板１に対して、例えばＡｓを注入エネルギー１０ｋｅＶ、ドーズ量５×１０^{15}ｃｍ$^{-2}$の条件でイオン注入した後、例えば１０５０℃程度の温度でＳＰＩＫＥ　ＲＴＡを行い、注入不純物を活性化する。これにより、図１４（ｇ）に示すように、ｎ型ソース・ドレイン領域１２が形成される。

【０１２４】

次に、基板１の上に全面に亘って膜厚１０ｎｍ程度の金属膜（例えばＮｉ膜）を堆積した後、ＲＴＡを実施することにより基板１の露出部分と金属膜とを反応させ、それによって、図１５（ａ）に示すように、ｎ型ソース・ドレイン領域１２上にシリサイド層１３を形成する。その後、基板１上に残留する未反応の金属膜を剥離・除去する。

【０１２５】

次に、図１５（ｂ）に示すように、ゲート電極５の上を含む基板１の上に全面に亘って例えば膜厚４００ｎｍ程度の層間絶縁膜１４を堆積する。

【０１２６】

次に、図１５（ｃ）に示すように、例えばＣＭＰ（chemical mechanical polishing ）によって層間絶縁膜１４を、その表面がカバー膜１５の上面と面一になるまで削った後、当該露出したカバー膜１５をエッチングにより除去する。このとき、ＣＭＰ後の層間絶縁膜１４の上部及びオフセットサイドウォール６の上部も除去される。

【０１２７】

次に、基板１の上に全面に亘って膜厚１００ｎｍ程度の金属膜（例えばＮｉ膜）を堆積した後、ＲＴＡを実施することによりゲート電極５の露出部分と金属膜とを反応させ、それによって、図１５（ｄ）に示すように、フルシリサイド化されたゲート電極１６（高誘電率ゲート絶縁膜４上の全領域がシリサイド化されたゲート電極１６）を形成する。

【０１２８】

以上に説明した本実施形態の製造方法によると、ＦＵＳＩ（full silicide ）構造を用いた第２の実施形態のＭＩＳＦＥＴ構造（図２参照）を比較的簡単に実現することができる。

【０１２９】

尚、本実施形態において、オフセットサイドウォール６の形成後に、オフセットサイドウォール６の外側に位置する高誘電率ゲート絶縁膜４を、例えばフッ酸を用いたウェットエッチングによって除去する際に、オフセットサイドウォール６の側端部の下側に位置する高誘電率ゲート絶縁膜４の一部、つまり高誘電率ゲート絶縁膜４の側端部をノッチ状に取り除いてノッチを設けてもよい。このようにすると、ＦＵＳＩ構造を用いた第２の実施形態の第１変形例のＭＩＳＦＥＴ構造（図７参照）を簡単に実現することができる。

【０１３０】

また、本実施形態において、ゲート電極５の外側における高誘電率ゲート絶縁膜４の薄膜化の程度は特に限定されるものではないが、高誘電率ゲート絶縁膜４として例えばＨｆＳｉＯＮ膜を用いる場合、ゲート・ドレイン間の容量の上昇を抑制するためには、ゲート電極５の外側の高誘電率ゲート絶縁膜４を膜厚２ｎｍ程度以下に薄膜化する（但し基板１の表面が露出しないように）ことが好ましい。

【０１３１】

また、本実施形態において、オフセットサイドウォール６を形成した後、オフセットサイドウォール６の外側の高誘電率ゲート絶縁膜４を除去し、その後、ｎ型エクステンション領域１０及びｐ型ポケット領域１１を形成するためのイオン注入を行った。しかし、これに代えて、オフセットサイドウォール６を形成した後、オフセットサイドウォール６の外側に薄膜化した高誘電率ゲート絶縁膜４を残存させた状態でｎ型エクステンション領域１０及びｐ型ポケット領域１１を形成するためのイオン注入を行ってもよい。このようにしても、本実施形態ではゲート電極５の外側に位置する高誘電率ゲート絶縁膜４が薄膜化されているため、加速エネルギーの増大を抑制できるので、ｎ型エクステンション領域１０において浅い接合を容易に形成でき、それによりデバイス特性の向上を図りやすい。ま

UMC 1002
UMC v. AICP

た、この場合、ｎ型エクステンション領域１０及びｐ型ポケット領域１１を形成するためのイオン注入を行った後、オフセットサイドウォール６外側に位置する高誘電率ゲート絶縁膜４を除去し、その後、同一基板上における他のチャネル型又は別の電源系のＭＩＳＦＥＴのエクステンション領域及びポケット領域を形成するためのイオン注入を行ってもよい。

【０１３２】

また、本実施形態において、ＦＵＳＩ構造を用いた第２の実施形態のＭＩＳＦＥＴ構造を形成したが、これに代えて、第１の実施形態若しくはその変形例、第２の実施形態の各変形例、第３の実施形態若しくはその変形例、又は第４の実施形態若しくはその変形例のＭＩＳＦＥＴ構造をＦＵＳＩ構造を用いて形成してもよい。

【０１３３】

また、第１～第８の実施形態において、サイドウォール７として例えばＳｉＮ膜の１層構造を用いたが、これに代えて、例えば酸化膜（SiO_2 膜）と窒化膜（ＳｉＮ膜）とを組み合わせた２層構造（例えば下層SiO_2 膜と上層ＳｉＮ膜）又は３層構造（例えば下層SiO_2 膜と中層ＳｉＮ膜と上層SiO_2 膜）等を用いてもよい。

【０１３４】

また、第１～第８の実施形態において、ｎ型エクステンション領域１０に代えてＬＤＤを形成してもよい。

【０１３５】

また、第５～第８の実施形態において、ｎ型ＭＩＳＦＥＴに代えてｐ型ＭＩＳＦＥＴを形成してもよい。

【０１３６】

また、第５～第８の実施形態において、ゲート絶縁膜・ゲート電極界面の劣化を防止するために、ゲート電極５と高誘電率ゲート絶縁膜４との間に例えば膜厚０．２ｎｍ程度のバッファー絶縁膜を形成してもよい。

【０１３７】

また、第１～第８の実施形態において、サイドウォール７又はオフセットサイドウォール６の端部下側にノッチ２０が設けられた高誘電率ゲート絶縁膜４の側面形状は、図６、図７、図８又は図１０に示すような半円形状に限定されるものではない。例えば高誘電率ゲート絶縁膜４の側面形状は基板面に対して垂直な形状でもよい。すなわち、高誘電率ゲート絶縁膜４の側面は、サイドウォール７又はオフセットサイドウォール６の側端面からゲート電極５側に所定の距離だけ入り込んだ位置にあってもよい。

【産業上の利用可能性】

【０１３８】

以上に説明したように、本発明は、半導体装置及びその製造方法に関し、特に高誘電率ゲート絶縁膜を有するＭＩＳＦＥＴに適用した場合には、ＭＩＳＦＥＴの駆動力及び信頼性を向上させることができるという効果が得られ、非常に有用である。

【図面の簡単な説明】

【０１３９】

【図１】図１は本発明の第１の実施形態に係る半導体装置の構造を示す断面図である。

【図２】図２は本発明の第２の実施形態に係る半導体装置の構造を示す断面図である。

【図３】図３は本発明の第２の実施形態の第２変形例に係る半導体装置の構造を示す断面図である。

【図４】図４は本発明の第２の実施形態の第３変形例に係る半導体装置の構造を示す断面図である。

【図５】図５は本発明の第３の実施形態に係る半導体装置の構造を示す断面図である。

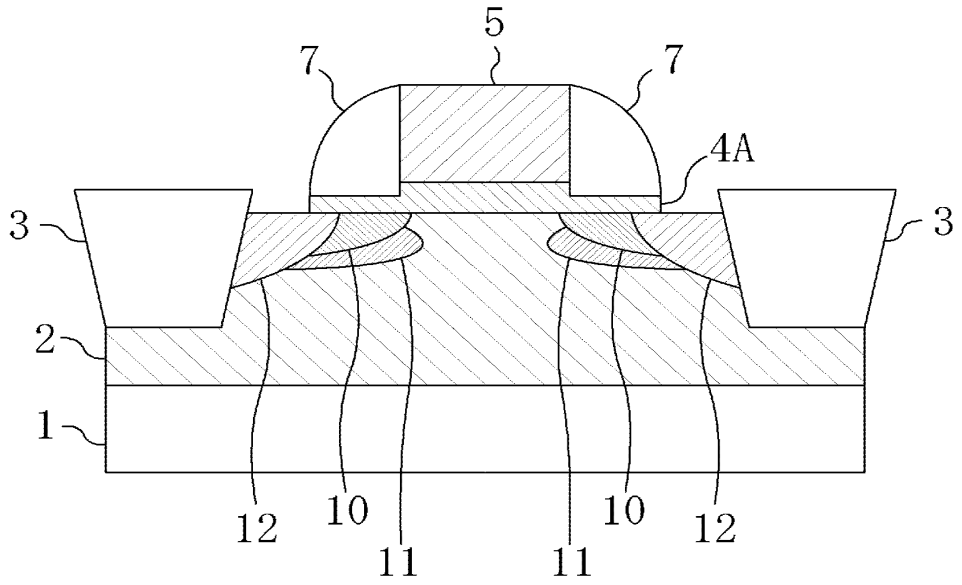
【図６】図６は本発明の第１の実施形態の変形例に係る半導体装置の構造を示す断面

UMC 1002
UMC v. AICP

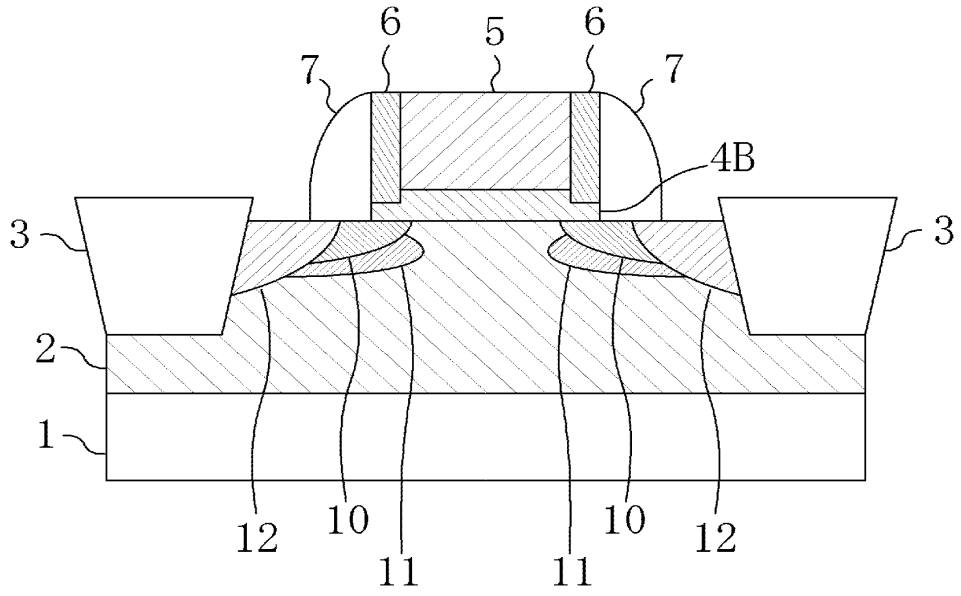
図である。
【図７】図７は本発明の第２の実施形態の第１変形例に係る半導体装置の構造を示す断面図である。
【図８】図８は本発明の第３の実施形態の変形例に係る半導体装置の構造を示す断面図である。
【図９】図９は本発明の第４の実施形態に係る半導体装置の構造を示す断面図である。
【図１０】図１０は本発明の第４の実施形態の変形例に係る半導体装置の構造を示す断面図である。
【図１１】図１１（ａ）～（ｆ）は本発明の第５の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。
【図１２】図１２（ａ）～（ｇ）は本発明の第６の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。
【図１３】図１３（ａ）～（ｇ）は本発明の第７の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。
【図１４】図１４（ａ）～（ｇ）は本発明の第８の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。
【図１５】図１５（ａ）～（ｄ）は本発明の第８の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。
【図１６】図１６（ａ）及び（ｂ）はそれぞれ従来のＭＩＳＦＥＴの構造を示す断面図である。
【符号の説明】
【０１４０】
１　基板
２　ｐ型ウェル
３　ＳＴＩ
４（４Ａ～４Ｅ）　高誘電率ゲート絶縁膜
５Ａ　ゲート電極材料膜
５　ゲート電極
６　オフセットサイドウォール
７　サイドウォール
１０　ｎ型エクステンション領域
１１　ｐ型ポケット領域
１２　ｎ型ソース・ドレイン領域
１３　シリサイド層
１４　層間絶縁膜
１５　カバー膜
１６　フルシリサイド化されたゲート電極
２０　ノッチ
２５　バッファー絶縁膜

UMC 1002
UMC v. AICP

【書類名】図面
【図１】

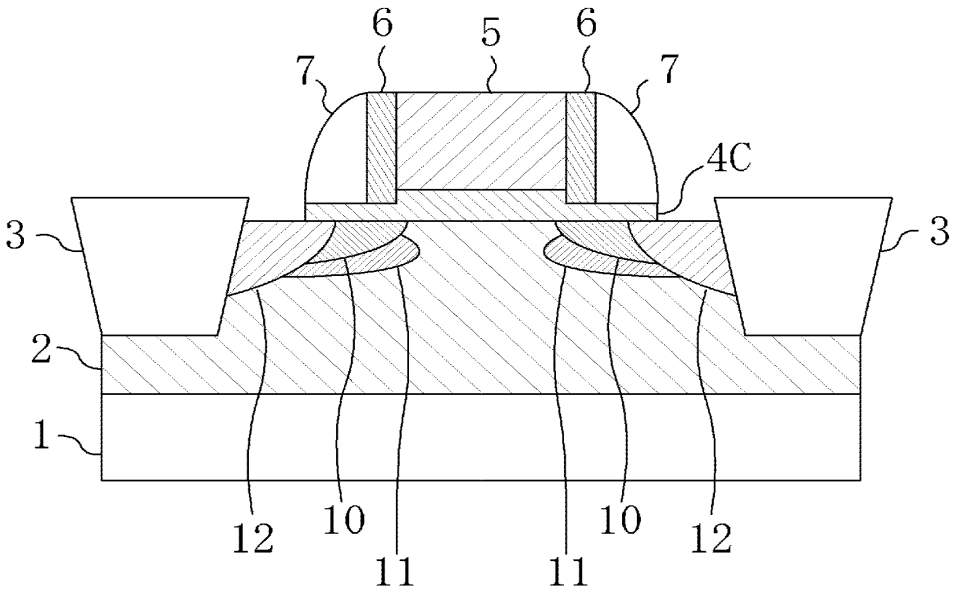


【図２】

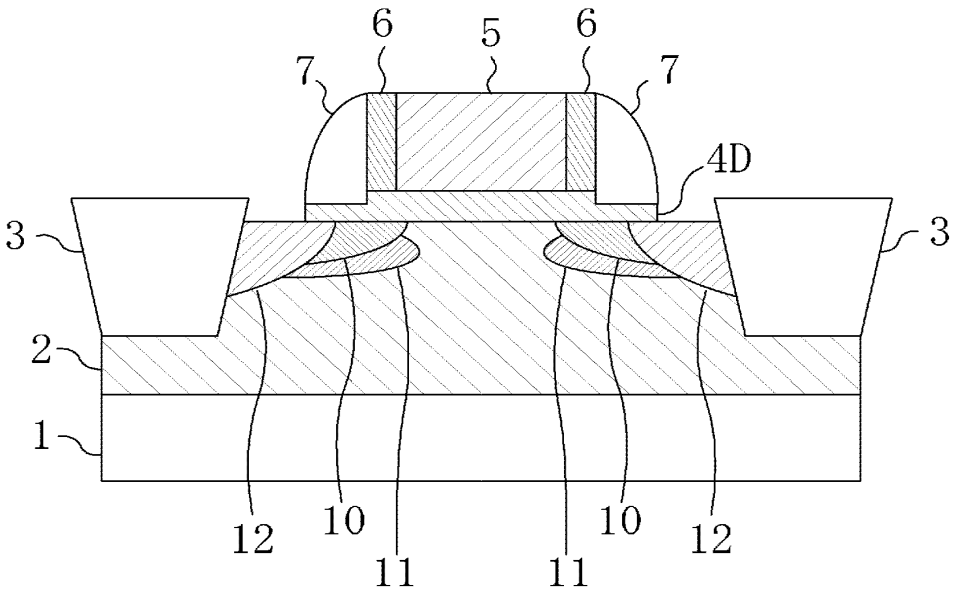


UMC 1002
UMC v. AICP

【図３】

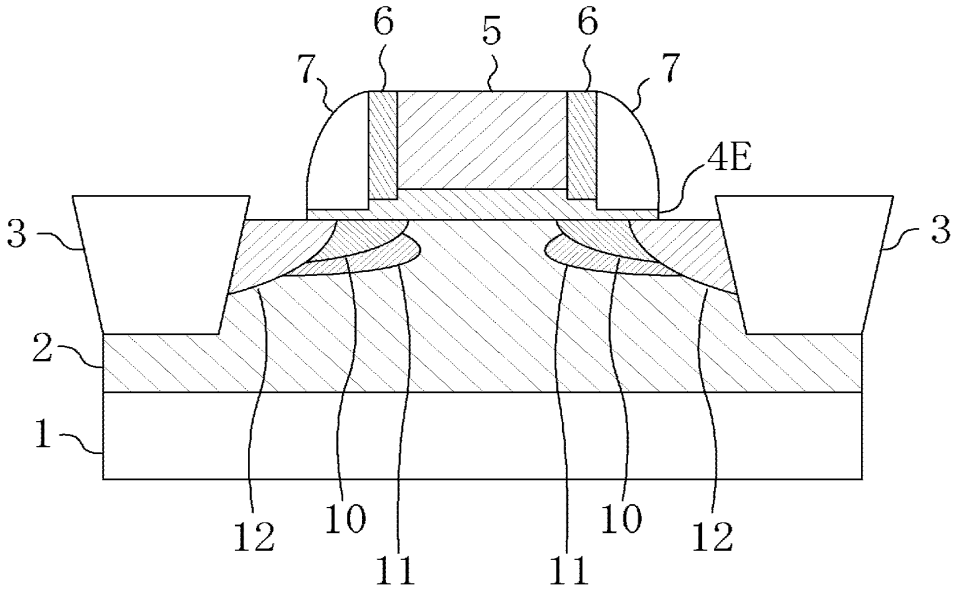


【図４】

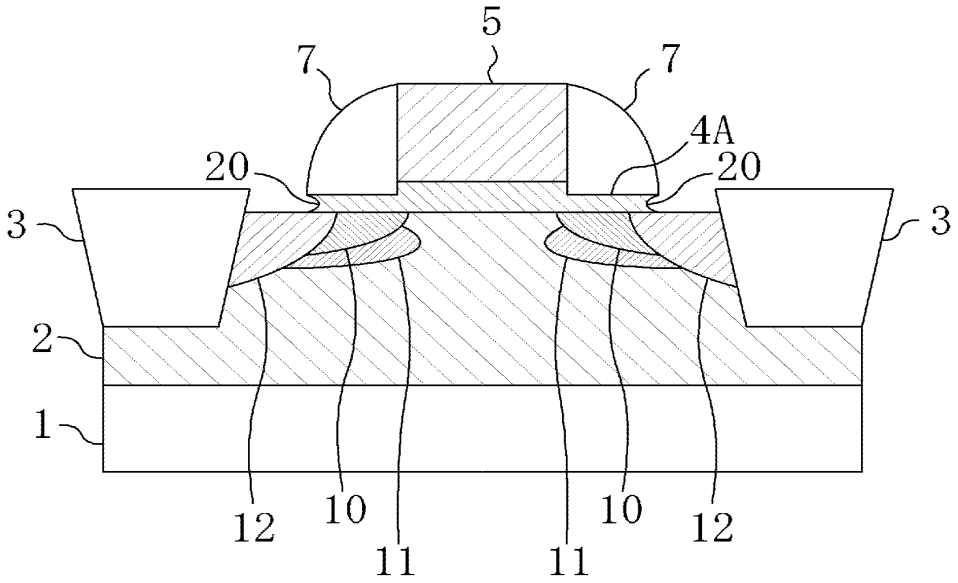


UMC 1002
UMC v. AICP

【図５】

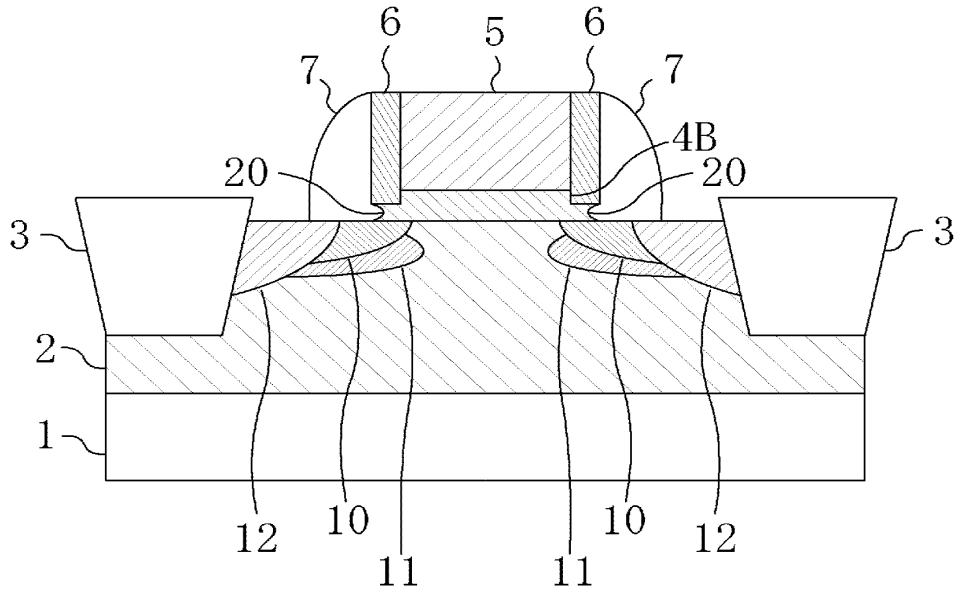


【図６】

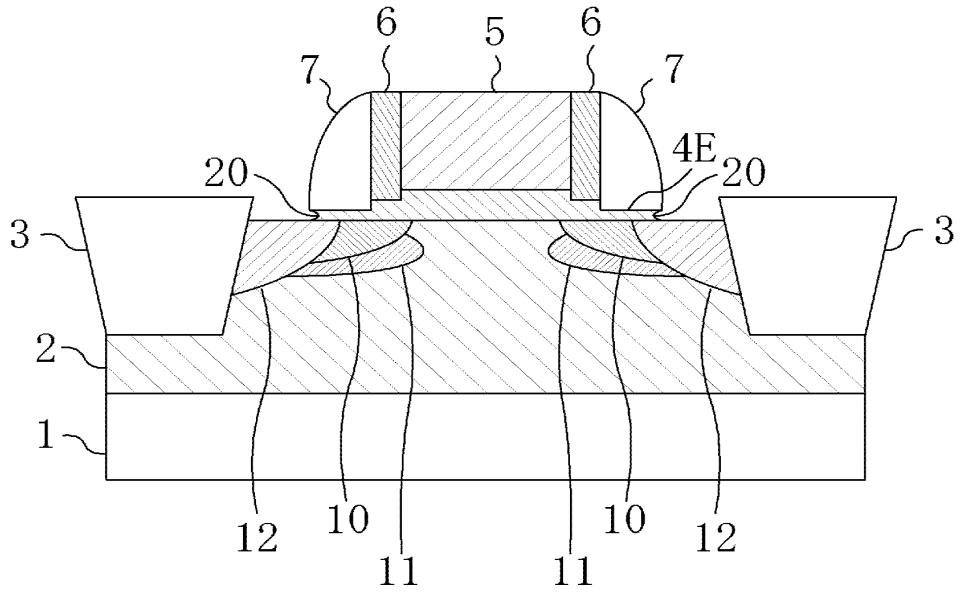


UMC 1002
UMC v. AICP

【図７】

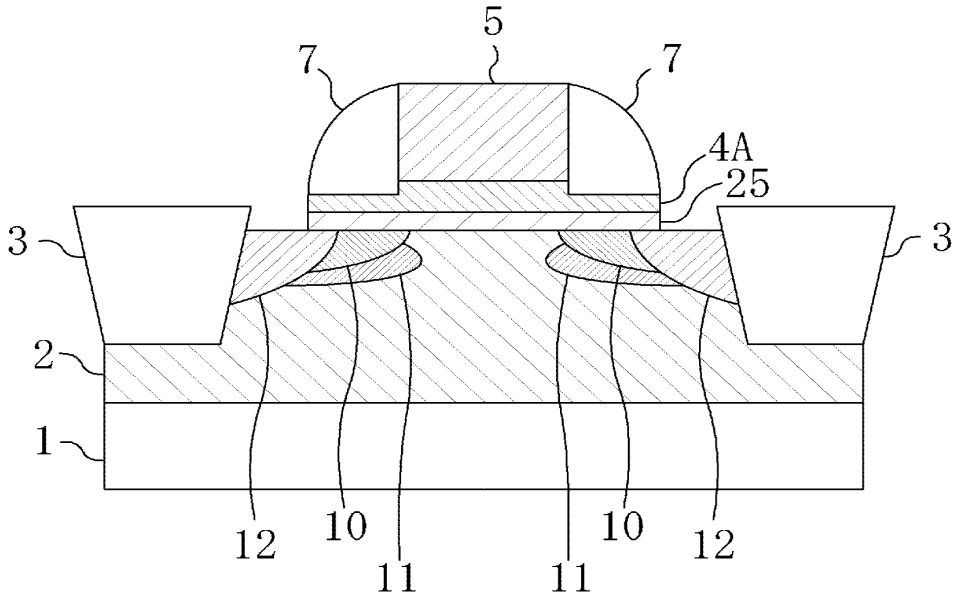


【図８】

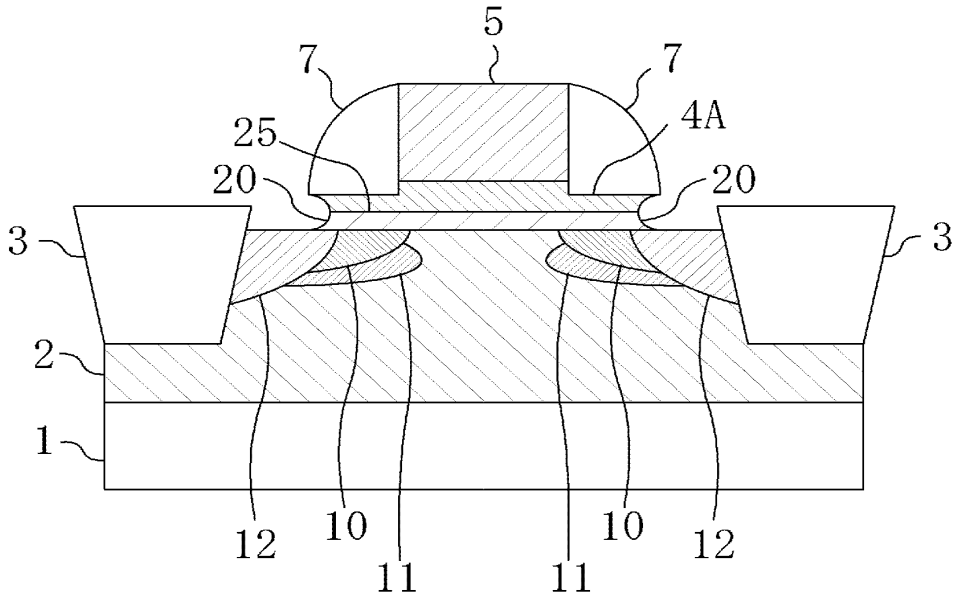


UMC 1002
UMC v. AICP

【図９】

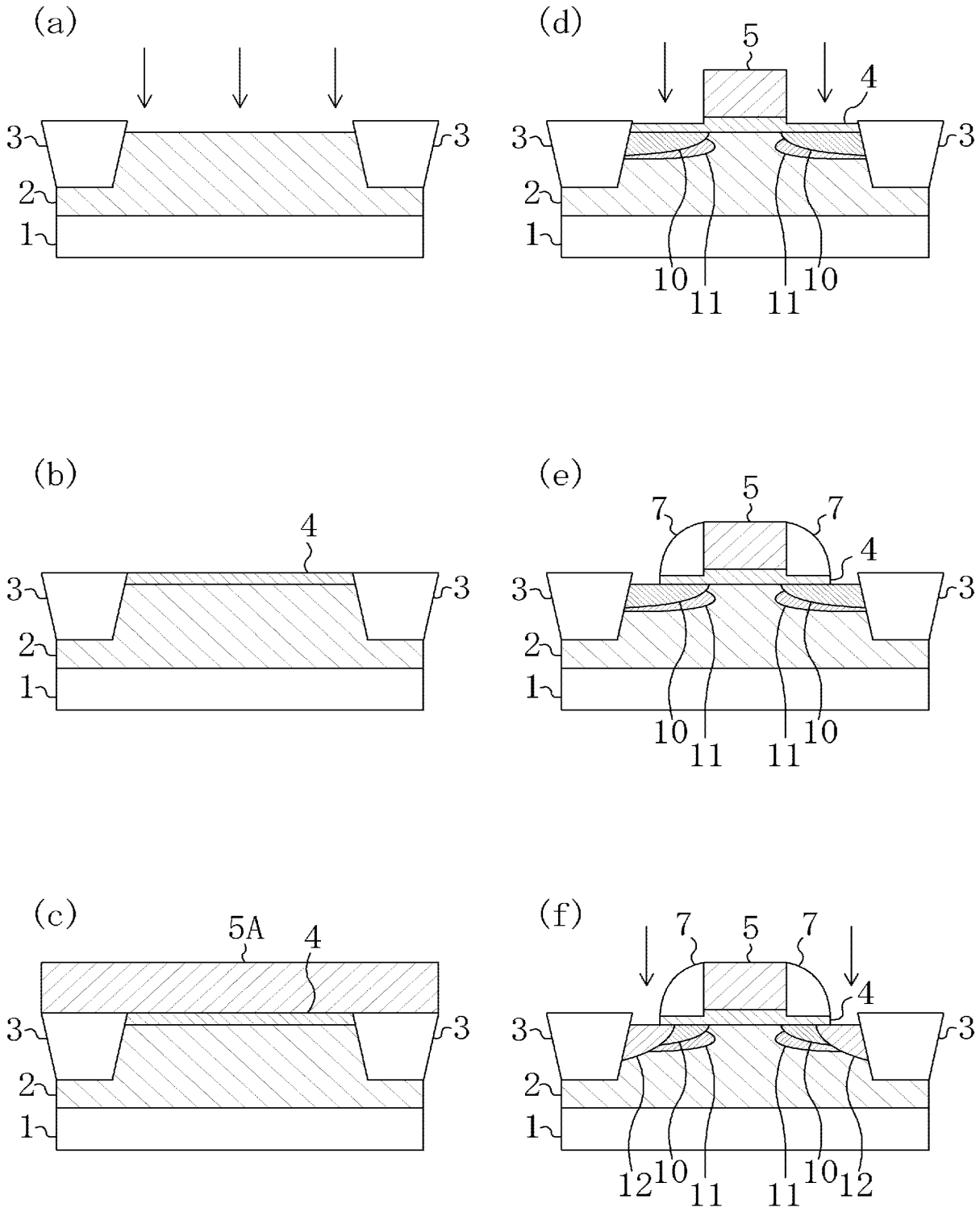


【図１０】



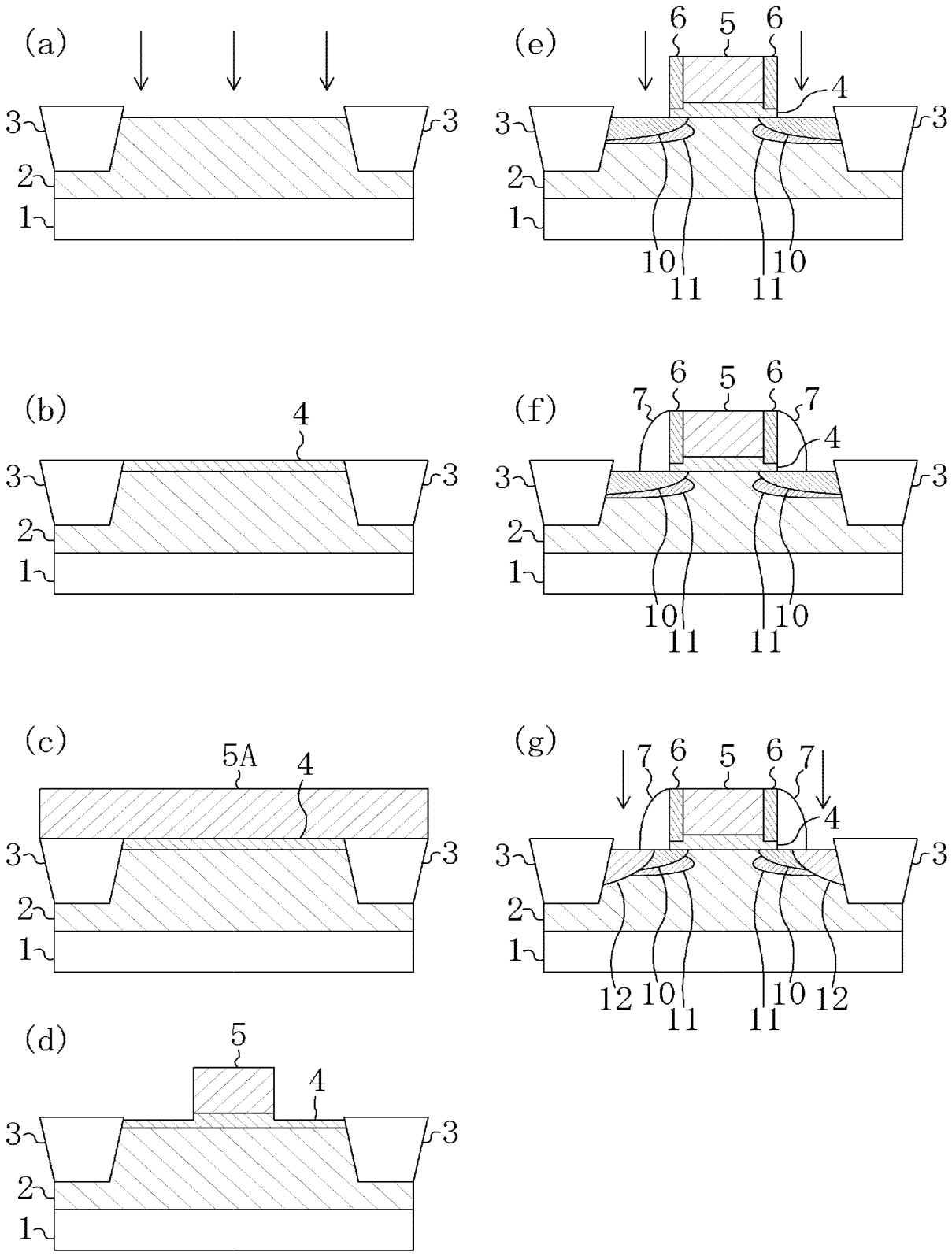
UMC 1002
UMC v. AICP

【図１１】



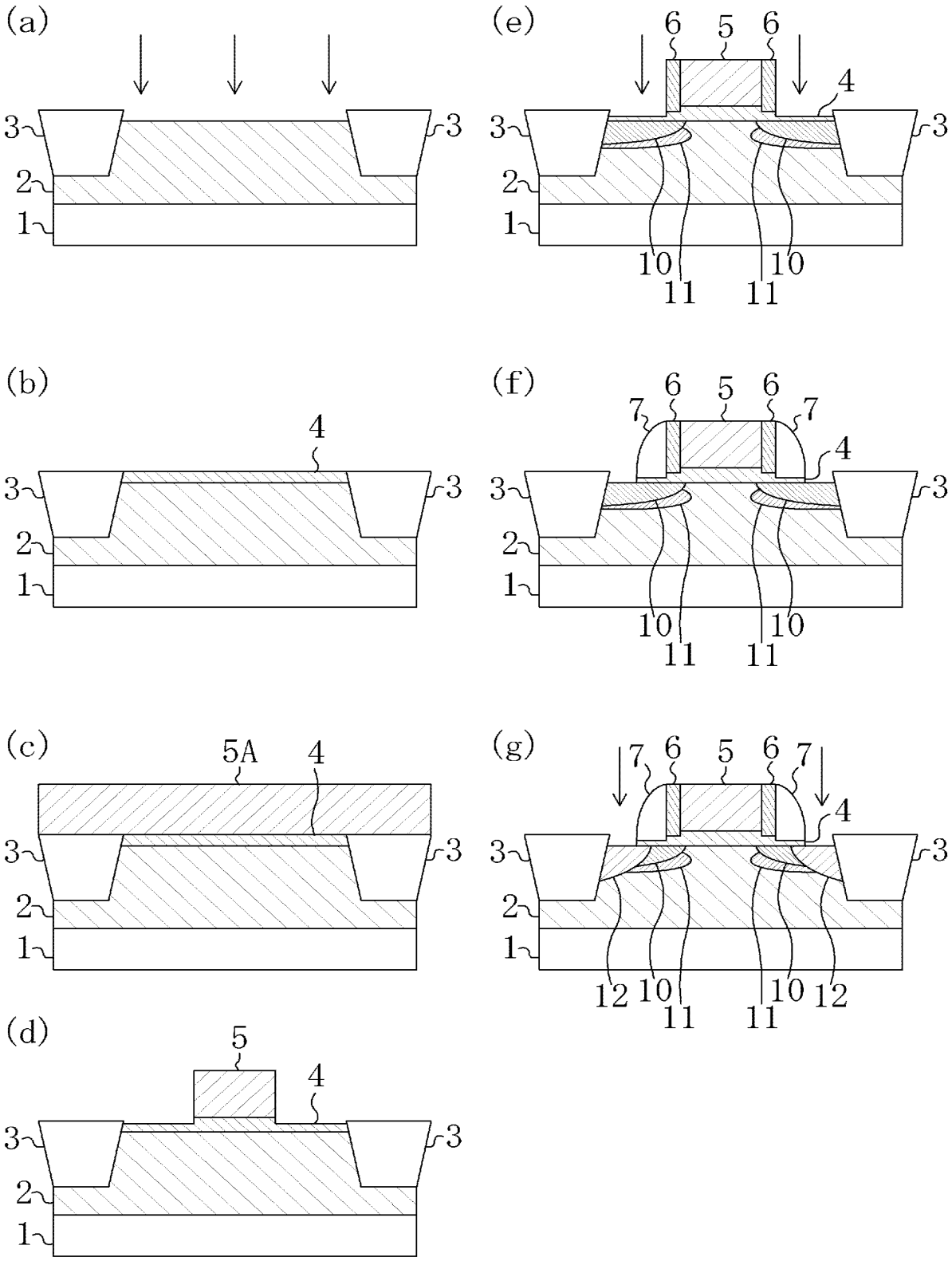
UMC 1002
UMC v. AICP

【図１２】



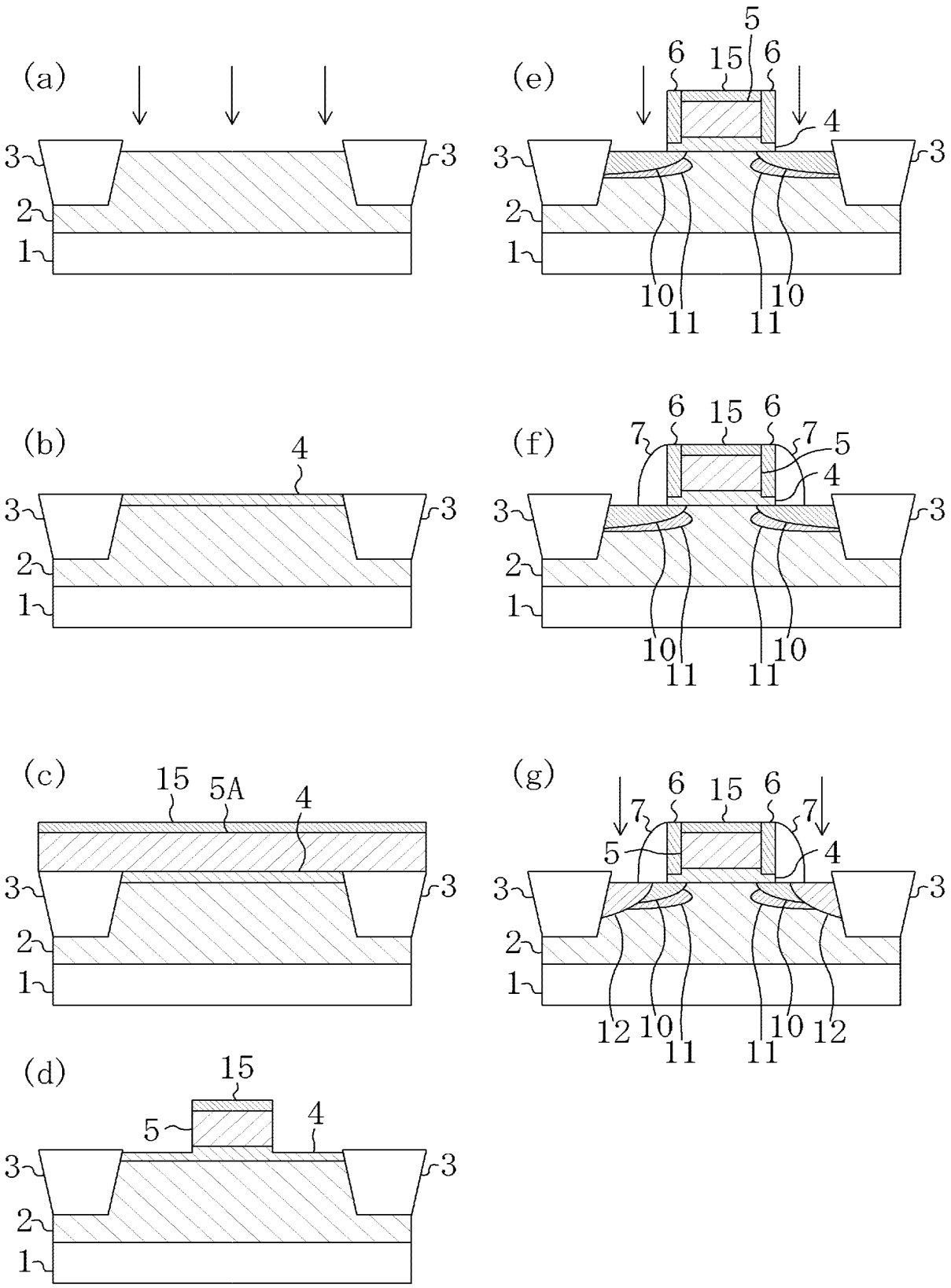
UMC 1002
UMC v. AICP

【図１３】



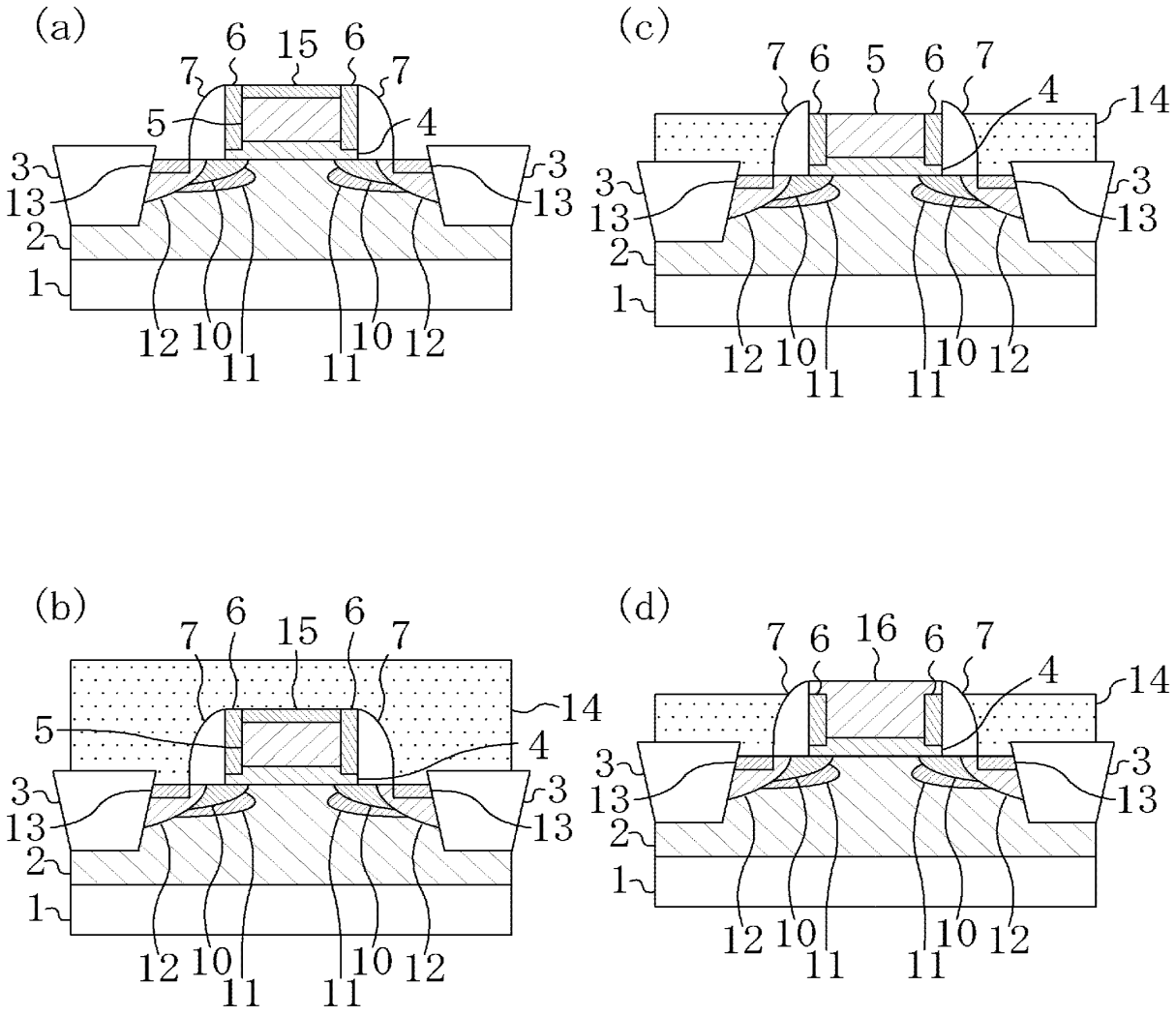
UMC 1002
UMC v. AICP

【図１４】



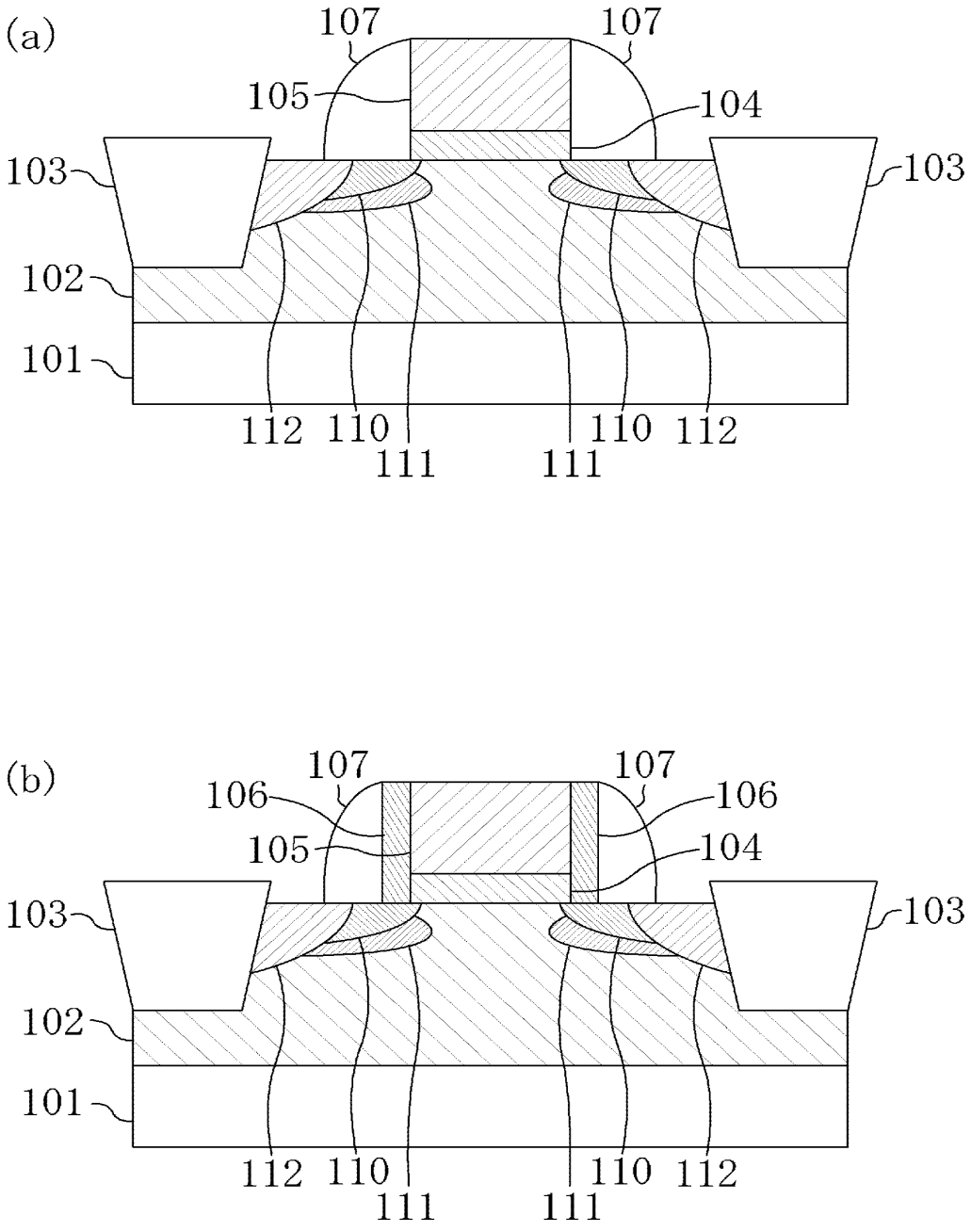
UMC 1002
UMC v. AICP

【図１５】



UMC 1002
UMC v. AICP

【図１６】



UMC 1002
UMC v. AICP

【書類名】要約書
【要約】
【課題】　高誘電率ゲート絶縁膜を使用したＭＩＳＦＥＴにおいて高誘電率ゲート絶縁膜を劣化させることなくＭＩＳＦＥＴの特性を向上させる。
【解決手段】　基板１の活性領域上に高誘電率ゲート絶縁膜４Ａを介してゲート電極５が形成されている。ゲート電極５の側面には絶縁性のサイドウォール７が形成されている。高誘電率ゲート絶縁膜４Ａはゲート電極５の下側からサイドウォール７の下側まで連続的に形成されている。高誘電率ゲート絶縁膜４Ａにおけるサイドウォール７の下側領域の厚さは、高誘電率ゲート絶縁膜４Ａにおけるゲート電極５の下側領域の厚さよりも小さい。
【選択図】　図１

UMC 1002
UMC v. AICP

【書類名】　手続補正書
【整理番号】　P53042401
【あて先】　特許庁長官　殿
【事件の表示】
　【出願番号】　特願2005-227457
【補正をする者】
　【識別番号】　000005821
　【氏名又は名称】　パナソニック株式会社
【代理人】
　【識別番号】　100077931
　【弁理士】
　【氏名又は名称】　前田　弘
【発送番号】　641602
【手続補正1】
　【補正対象書類名】　特許請求の範囲
　【補正対象項目名】　全文
　【補正方法】　変更
　【補正の内容】
　　【書類名】特許請求の範囲
　　【請求項１】
　基板の活性領域上に形成された高誘電率ゲート絶縁膜と、
　前記高誘電率ゲート絶縁膜上に形成されたゲート電極と、
　前記ゲート電極の側面に形成された絶縁性サイドウォールとを備え、
　前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記絶縁性サイドウォールの下側まで連続的に形成されており、
　前記絶縁性サイドウォールは、前記ゲート電極の側面に形成された第１の絶縁性サイドウォールと、前記ゲート電極の側面に前記第１の絶縁性サイドウォールを介して形成された第２の絶縁性サイドウォールとからなり、
　前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第１の絶縁性サイドウォールの下側まで連続的に形成されており、
　前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さよりも小さく、
　前記活性領域における前記第１の絶縁性サイドウォール及び前記第２の絶縁性サイドウォールのそれぞれの下側にエクステンション領域が形成されており、
　前記活性領域における前記ゲート電極からみて前記エクステンション領域の外側にソース・ドレイン領域が形成されていることを特徴とする半導体装置。
　　【請求項２】
　請求項１に記載の半導体装置において、
　前記高誘電率ゲート絶縁膜は前記第２の絶縁性サイドウォールの下側には形成されていないことを特徴とする半導体装置。
　　【請求項３】
　請求項１に記載の半導体装置において、
　前記高誘電率ゲート絶縁膜は前記第２の絶縁性サイドウォールの下側まで連続的に形成されており、
　前記高誘電率ゲート絶縁膜における前記第２の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さと同等であることを特徴とする半導体装置。
　　【請求項４】
　請求項１に記載の半導体装置において、
　前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第２の絶縁性サイドウォー

UMC 1002
UMC v. AICP

ルの下側まで連続的に形成されており、
前記高誘電率ゲート絶縁膜における前記第２の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さよりも小さいことを特徴とする半導体装置。
【請求項５】
請求項１～４のいずれか１項に記載の半導体装置において、
前記高誘電率ゲート絶縁膜の側端部にノッチが設けられていることを特徴とする半導体装置。
【請求項６】
請求項１～５のいずれか１項に記載の半導体装置において、
前記基板と前記高誘電率ゲート絶縁膜との間にバッファー絶縁膜が設けられていることを特徴とする半導体装置。
【請求項７】
請求項６に記載の半導体装置において、
前記バッファー絶縁膜はシリコン酸化膜又はシリコン酸窒化膜であることを特徴とする半導体装置。
【請求項８】
請求項１～７のいずれか１項に記載の半導体装置において、
前記ゲート電極は、全領域がシリサイド化されたフルシリサイドゲート電極であることを特徴とする半導体装置。
【請求項９】
請求項１～８のいずれか１項に記載の半導体装置において、
前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さは、２ｎｍ以下であることを特徴とする半導体装置。
【請求項１０】
請求項１～９のいずれか１項に記載の半導体装置において、
前記高誘電率ゲート絶縁膜は、Ｈｆ系酸化物からなることを特徴とする半導体装置。

【手続補正2】
【補正対象書類名】　明細書
【補正対象項目名】　発明の名称
【補正方法】　変更
【補正の内容】
【発明の名称】半導体装置

UMC 1002
UMC v. AICP

【書類名】　手続補正書
【整理番号】　P53042401
【あて先】　特許庁長官　殿
【事件の表示】
　【出願番号】　特願2005-227457
【補正をする者】
　【識別番号】　000005821
　【氏名又は名称】　パナソニック株式会社
【代理人】
　【識別番号】　110001427
　【氏名又は名称】　特許業務法人前田特許事務所
　【代表者】　前田　弘
　【電話番号】　06-6125-2255
【発送番号】　833248
【手続補正1】
　【補正対象書類名】　特許請求の範囲
　【補正対象項目名】　全文
　【補正方法】　変更
　【補正の内容】
　　【書類名】特許請求の範囲
　　【請求項１】
　基板の活性領域上に形成された高誘電率ゲート絶縁膜と、
　前記高誘電率ゲート絶縁膜上に形成されたゲート電極と、
　前記ゲート電極の側面に形成された絶縁性サイドウォールとを備え、
　前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記絶縁性サイドウォールの下側まで連続的に形成されており、
　前記絶縁性サイドウォールは、前記ゲート電極の側面に形成された第１の絶縁性サイドウォールと、前記ゲート電極の側面に前記第１の絶縁性サイドウォールを介して形成された第２の絶縁性サイドウォールとからなり、
　前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第１の絶縁性サイドウォールの下側まで連続的に形成されており、
　前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さよりも小さく、
　前記活性領域における前記第１の絶縁性サイドウォール及び前記第２の絶縁性サイドウォールのそれぞれの下側にエクステンション領域が形成されており、
　前記活性領域における前記ゲート電極からみて前記エクステンション領域の外側にソース・ドレイン領域が形成されており、
　前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第２の絶縁性サイドウォールの下側まで連続的に形成されており、
　前記高誘電率ゲート絶縁膜における前記第２の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さよりも小さいことを特徴とする半導体装置。
　　【請求項２】
　請求項１に記載の半導体装置において、
　前記高誘電率ゲート絶縁膜の側端部にノッチが設けられていることを特徴とする半導体装置。
　　【請求項３】
　請求項１又は２に記載の半導体装置において、
　前記基板と前記高誘電率ゲート絶縁膜との間にバッファー絶縁膜が設けられていることを特徴とする半導体装置。

UMC 1002
UMC v. AICP

【請求項４】
請求項３に記載の半導体装置において、
前記バッファー絶縁膜はシリコン酸化膜又はシリコン酸窒化膜であることを特徴とする半導体装置。
【請求項５】
請求項１～４のいずれか１項に記載の半導体装置において、
前記ゲート電極は、全領域がシリサイド化されたフルシリサイドゲート電極であることを特徴とする半導体装置。
【請求項６】
請求項１～５のいずれか１項に記載の半導体装置において、
前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さは、２ｎｍ以下であることを特徴とする半導体装置。
【請求項７】
請求項１～６のいずれか１項に記載の半導体装置において、
前記高誘電率ゲート絶縁膜は、Ｈｆ系酸化物からなることを特徴とする半導体装置。

出願人履歴

０００００５８２１

19900828

新規登録

５０６１７８４４９

大阪府門真市大字門真１００６番地

松下電器産業株式会社

０００００５８２１

20081001

名称変更

５０６１７８４４９

大阪府門真市大字門真１００６番地

パナソニック株式会社

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/547,913	07/12/2012	Junji Hirase	085393-0808

CONFIRMATION NO. 2994

53080
MCDERMOTT WILL & EMERY LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

PUBLICATION NOTICE

OC000000057382449

Title:SEMICONDUCTOR DEVICE

Publication No.US-2012-0273903-A1
Publication Date:11/01/2012

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/547,913	07/12/2012	Junji Hirase	085393-0808	2994

53080 7590 04/12/2013

MCDERMOTT WILL & EMERY LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

EXAMINER	
LUU, CHUONG A	
ART UNIT	PAPER NUMBER
2898	

NOTIFICATION DATE	DELIVERY MODE
04/12/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mweipdocket@mwe.com

PTOL-90A (Rev. 04/07)

UMC 1002
UMC v. AICP

Office Action Summary	Application No.	Applicant(s)	
	13/547,913	HIRASE ET AL.	
	Examiner	Art Unit	
	CHUONG A. LUU	2898	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *21-33* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *21-33* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 13/037,831.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

REJECTIONS BASED UPON PRIOR ARTS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The Rejections

Claims 21-25 and 27-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Hieda et al. (U.S. 6,992,358).

Hieda discloses, as shown in Figure 3C, a semiconductor device with

UMC 1002
UMC v. AICP

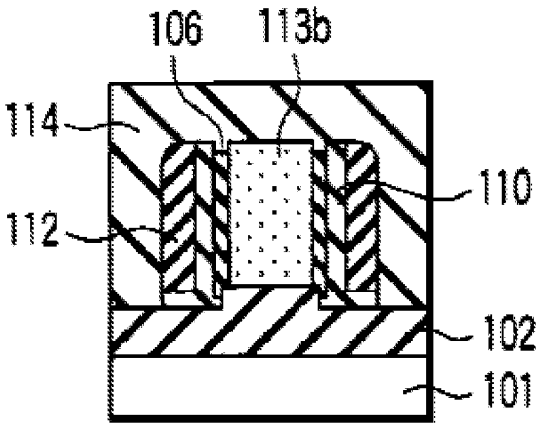


FIG. 3C

(21) a gate insulating film (102) formed on an active region in a substrate (101) and including Hf;

a gate electrode (113b) formed on the gate insulating film (102);

a insulating sidewall (106, 110, 112) formed on each side surface of the gate electrode (113b); and

wherein a width of the gate insulating film (102) along a gate length is larger than a width of the gate electrode along the gate length, and

an end of the gate insulating film (102) under the insulating sidewall (106, 110, 112) is located to retract from an outer end of the insulating sidewall (106, 110, 112) toward the gate electrode (113b) (see column 9, lines 40-64. Figure 3C);

(22) further comprising a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film (see Figure 3C);

UMC 1002
UMC v. AICP

(23) wherein the gate insulating film is formed of a Hf based oxide (see column 9, lines 40-64);

(24) wherein the gate insulating film is formed of a HfSiON film (see column 9, lines 40-64);

(25) wherein a part of the gate insulating film located under the insulating sidewall includes a notch at the end thereof (see Figure 3C);

(27) wherein an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall (see Figure 3C);

(28) wherein the insulating sidewall has a double layer structure including an oxide film and a nitride film (see Figure 3C);

(29) wherein the insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film (see Figure 3C);

(30) wherein a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length (see Figure 3C);

(31) wherein the end of the gate insulating film located under the insulating sidewall has a tapered surface (see Figure 3C);

(32) wherein the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof (see Figure 3C);

(33) wherein the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length.

UMC 1002
UMC v. AICP

REJECTIONS BASED UPON PRIOR ARTS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hieda et al. (U.S. 6,992,358).

Hieda teaches the above outlined features except for wherein a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less. Even through, Hieda does not explicitly describe wherein a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less. However, wherein a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less is considered to be obvious. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teachings of Hieda since it has been held that where the general conditions of a claim are disclosed in the prior ad, discovering the optimum or workable ranges involves only routine skill in the art and it is noted that the applicant does not disclose criticality in the ranges claimed. In re Aller, 105 USPQ 233 (see MPEP 2144.05).

UMC 1002
UMC v. AICP

Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

OBVIOUS TYPE DOUBLE PATENTING

Statutory Basis

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

The Rejections

Claims 21-33 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-22 of U.S. Patent No. 8,253,180.

Although the conflicting claims are not identical, they are claiming common subject matter, as follows: both U.S. Patent and instant application claimed a semiconductor device capable of implementing a second insulating sidewall on each

UMC 1002
UMC v. AICP

side surface of the gate electrode. Specifically, regarding claim 21 of instant application discloses a semiconductor device (claim 1 of Pat. 8,253,180, line 9) comprising: a gate insulating film formed on an active region in a substrate and including Hf (claim 1, lines 10-11 and claims 6-7); a gate electrode formed on the gate insulating film (claim 1, lines 12-13); a insulating sidewall formed on each side surface of the gate electrode (claim 1, lines 14-15); wherein the width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length (claims 16-17), and an end of the gate insulating film under the insulating sidewall is located to retract from an outer end of the insulating sidewall toward the gate electrode (claim 1, lines 19-22).

The limitations recited of the current application is broader compared with the U.S. Patent No. 8,253,180. The facts are that the claims of the U. S. Patent No. 8,253,180 and instant application have claimed the same goal and are not distinguished from each other.

For these reasons, claim 21-33 are seen as obvious variations of the patented claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHUONG A. LUU whose telephone number is (571)272-1902. The examiner can normally be reached on M-F (6:30-3:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio Maldonado can be reached on (571) 272-1864. The fax phone

UMC 1002
UMC v. AICP

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/CHUONG A LUU/
Primary Examiner, Art Unit 2898
April 07, 2013

UMC 1002
UMC v. AICP

Notice of References Cited	Application/Control No. 13/547,913	Applicant(s)/Patent Under Reexamination HIRASE ET AL.	
	Examiner CHUONG A. LUU	Art Unit 2898	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-8,253,180	08-2012	Hirase et al.	257/295
*	B	US-6,992,358	01-2006	Hieda et al.	257/407
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
13/547,913	HIRASE ET AL.
Examiner	**Art Unit**
CHUONG A. LUU	2898

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date								
Final	Original	4/7/13								
	1	-								
	2	-								
	3	-								
	4	-								
	5	-								
	6	-								
	7	-								
	8	-								
	9	-								
	10	-								
	11	-								
	12	-								
	13	-								
	14	-								
	15	-								
	16	-								
	17	-								
	18	-								
	19	-								
	20	-								
	21	√								
	22	√								
	23	√								
	24	√								
	25	√								
	26	√								
	27	√								
	28	√								
	29	√								
	30	√								
	31	√								
	32	√								
	33	√								
	34									
	35									
	36									
	37									
	38									
	39									
	40									
	41									
	42									
	43									
	44									
	45									
	46									
	47									
	48									
	49									
	50									

Claim		Date								
Final	Original									
	51									
	52									
	53									
	54									
	55									
	56									
	57									
	58									
	59									
	60									
	61									
	62									
	63									
	64									
	65									
	66									
	67									
	68									
	69									
	70									
	71									
	72									
	73									
	74									
	75									
	76									
	77									
	78									
	79									
	80									
	81									
	82									
	83									
	84									
	85									
	86									
	87									
	88									
	89									
	90									
	91									
	92									
	93									
	94									
	95									
	96									
	97									
	98									
	99									
	100									

Claim		Date								
Final	Original									
	101									
	102									
	103									
	104									
	105									
	106									
	107									
	108									
	109									
	110									
	111									
	112									
	113									
	114									
	115									
	116									
	117									
	118									
	119									
	120									
	121									
	122									
	123									
	124									
	125									
	126									
	127									
	128									
	129									
	130									
	131									
	132									
	133									
	134									
	135									
	136									
	137									
	138									
	139									
	140									
	141									
	142									
	143									
	144									
	145									
	146									
	147									
	148									
	149									
	150									

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1528	(257/410).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:37
L2	1	13/547913	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:37
L3	2	13/037831	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:37
L4	3	12/505799	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:38
L5	4	11/491260	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:38
L6	5	(("20030022422") or ("20040004234") or ("20040129997") or ("20050121733") or ("20060121740")).PN.	US-PGPUB	OR	OFF	2013/04/07 14:38
L8	3	(("8253180") or ("7923764") or ("7579227")).PN.	US-PGPUB; USPAT	OR	OFF	2013/04/07 14:39
L9	3362	(257/295).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:39
L10	3	(("7,579,227") or ("20050121733") or ("6,992,358")).PN.	US-PGPUB; USPAT	OR	OFF	2013/04/07 14:39
L11	8	(("20030022422") or ("20040004234")	US-PGPUB;	OR	OFF	2013/04/07

		or ("20040129997") or ("20050121733") or ("20060121740") or ("6,992,358") or ("6,929,992") or ("6,642,071")).PN.	USPAT			14:39
L12	2	(("7923764") or ("7579227")).PN.	US-PGPUB; USPAT	OR	OFF	2013/04/07 14:39
L13	3	(("7923764") or ("7579227") or ("6,992,358")).PN.	US-PGPUB; USPAT	OR	OFF	2013/04/07 14:40
L14	3	(("7923764") or ("7579227") or ("20040227185")).PN.	US-PGPUB; USPAT	OR	OFF	2013/04/07 14:40
L15	23	("20020053711" | "5889331" | "6314021" | "6512258" | "6518155" | "6765273" | "6777283" | "6777759").PN. OR ("2004/0227185" | "7067881").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/04/07 14:40
L16	1613	(257/411).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:41
L17	1528	(257/410).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:41
L18	5625	(257/296).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:41
L19	2769	(257/368).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:41
L20	4179	(257/369).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:41
L21	256	(257/389).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:42
L22	940	(257/392).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	OFF	2013/04/07 14:42

			JPO; DERWENT; IBM_TDB			
L23	565	(257/393).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:42
L24	206	(257/395).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:42
L25	201	(257/405).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:42
L26	255	(257/406).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:42
L27	12	("20030022422" | "20040004234" | "20040129997" | "20050121733" | "20050127436" | "20060121740" | "6642071" | "6929992" | "6992358").PN. OR ("7579227").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/04/07 14:43
L28	3	12/505799	US-PGPUB; USPAT; USOCR	OR	ON	2013/04/07 14:43
L29	3362	(257/295).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:43
L30	1623	(257/310).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:43
L31	3	09/916509	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:43

L32	19	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) adj (high adj dielectric adj constant)) and overlap$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:43
L33	18	("20030209761" | "20040150520" | "20040178451" | "20050040464" | "20050051843" | "20050110085" | "4979014" | "6437404" | "6538916" | "6580132" | "6639246" | "6646307" | "6687152" | "6724046" | "6740938" | "6744390" | "6800513" | "6822071").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/04/07 14:44
L34	1667	hirase.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:44
L35	1667	hirase.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:44
L36	95	L35 and junji	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:44
L37	0	36 and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) adj (high adj dielectric adj constant))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:45
L38	0	36 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:45
L39	332	sebe.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:45
L40	22	39 and akio	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2013/04/07 14:46

			JPO; DERWENT; IBM_TDB			
L41	0	40 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:46
L42	20513	kotani.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:46
L43	274	42 and naoki	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:46
L44	0	43 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:46
L45	41632	okazaki.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:47
L46	71	45 and gen	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:47
L47	0	46 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:47
L48	17970	aida.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:47
L49	172	48 and kazuhiko	US-PGPUB; USPAT;	OR	ON	2013/04/07 14:49

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L50	0	49 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:50
L51	2816	takeoka.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:50
L52	203	51 and shinji	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:50
L53	0	52 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:50

4/7/2013 2:51:07 PM
C:\Users\cluu\Documents\EAST\Workspaces\13547913.wsp

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 2994

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/547,913	07/12/2012	257	2898	085393-0808

APPLICANTS

Junji Hirase, Osaka, JAPAN;
Akio Sebe, Osaka, JAPAN;
Naoki Kotani, Hyogo, JAPAN;
Gen Okazaki, Hyogo, JAPAN;
Kazuhiko Aida, Chiba, JAPAN;
Shinji Takeoka, Osaka, JAPAN;

** CONTINUING DATA ********** Yes CAL

This application is a DIV of 13/037,831 03/01/2011 PAT 8253180
which is a DIV of 12/505,799 07/20/2009 PAT 7923764
which is a DIV of 11/491,260 07/24/2006 PAT 7579227

** FOREIGN APPLICATIONS ********** Yes CAL

JAPAN 2005-227457 08/05/2005

** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **

07/24/2012

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /CHUONG A LUU/ Examiner's Signature	☑ Met after Allowance CAL Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		JAPAN	11	13	1

ADDRESS

MCDERMOTT WILL & EMERY LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001
UNITED STATES

TITLE

SEMICONDUCTOR DEVICE

FILING FEE RECEIVED		
1250	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

UMC 1002
UMC v. AICP

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination
	13/547,913	HIRASE ET AL.
	Examiner	Art Unit
	CHUONG A. LUU	2898

SEARCHED			
Class	Subclass	Date	Examiner
257	410	4/7/2013	CAL

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
Please see the attachment.	4/7/2013	CAL

Doc Code: DIST.E.FILE Document Description: Electronic Terminal Disclaimer - Filed	PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	13547913
Filing Date	12-Jul-2012
First Named Inventor	Junji Hirase
Attorney Docket Number	085393-0808
Title of Invention	SEMICONDUCTOR DEVICE

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
PANASONIC CORPORATION	100%

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

8253180

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

◉ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

○	I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

○ Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

○ Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

○ Applicant(s) status remains as SMALL ENTITY.

◉ Applicant(s) status remains as other than SMALL ENTITY.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

◉ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

Registration Number 36139

○ A sole inventor

○ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors

○ A joint inventor; all of whom are signing this request

○ The assignee of record of the entire interest that has properly made itself of record pursuant to 37 CFR 3.71

Signature	/Michael E. Fogarty/
Name	Michael E. Fogarty

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	13547913
Filing Date:	12-Jul-2012
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Junji Hirase
Filer:	Michael E. Fogarty/Rosanna Pase
Attorney Docket Number:	085393-0808

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Statutory or Terminal Disclaimer	1814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**160**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 13547913

Filing Date: 12-Jul-2012

Applicant/Patent under Reexamination: Hirase et al.

Electronic Terminal Disclaimer filed on July 1, 2013

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	16205414
Application Number:	13547913
International Application Number:	
Confirmation Number:	2994
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Junji Hirase
Customer Number:	53080
Filer:	Michael E. Fogarty/Rosanna Pase
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0808
Receipt Date:	01-JUL-2013
Filing Date:	12-JUL-2012
Time Stamp:	17:00:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$160
RAM confirmation Number	4730
Deposit Account	500417
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

UMC 1002
UMC v. AICP

1	Electronic Terminal Disclaimer-Filed	eTerminal-Disclaimer.pdf	33632 3f65fb40117ef53c1f2d9bf02737e01ad3fe4ab3	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30056 dd9190f8a9b941396a49983acf959c784d402097	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	63688		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No.: 085393-0808 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Junji HIRASE, et al.	:	Confirmation Number: 2994
Application No.: 13/547,913	:	Group Art Unit: 2898
Filed: July 12, 2012	:	Examiner: Chuong A. LUU
For: SEMICONDUCTOR DEVICE	:	

AMENDMENT UNDER 37 C.F.R. § 1.111

Mail Stop - Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Madam:

In response to the Office Action dated April 12, 2013 having a shortened statutory period of response set to expire on July 12, 2013, please amend the above-identified application as follows:

An eTerminal Disclaimer is being filed concurrently herewith.

UMC 1002
UMC v. AICP

IN THE SPECIFICATION:

Please amend the following paragraph on page 1 of the specification as follows:

-- RELATED APPLICATIONS

This application is a Divisional of U.S. Application No. 13/037,831, filed on March 1, 2011, now U.S. Patent No. 8,253,180, which is a Divisional of U.S. Application No. 12/505,799, filed on July 20, 2009, now U.S. Patent No. 7,923,764, which is a Divisional of U.S. Application No. 11/491,260, filed on July 24, 2006, now U.S. Patent No. 7,579,227, claiming priority of Japanese Patent Application No. 2005-227457, filed on August 5, 2005, the entire contents of each of which are hereby incorporated by reference. --

IN THE CLAIMS:

Please amend the claims as follows:

1-20. (Canceled)

21. (Currently amended) A semiconductor device comprising:

a gate insulating film formed on an active region in a substrate and including Hf;

a gate electrode formed on the gate insulating film;

a insulating sidewall formed on each side surface of the gate electrode; and

wherein a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length, and

an end of the gate insulating film under the insulating sidewall is ~~located to retract~~ retracted from an outer end of the insulating sidewall toward the gate electrode.

22. (Previously presented) The semiconductor device of claim 21, further comprising a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film.

23. (Previously presented) The semiconductor device of claim 21, wherein the gate insulating film is formed of a Hf based oxide.

24. (Previously presented) The semiconductor device of claim 21, wherein the gate insulating film is formed of a HfSiON film.

25. (Previously presented) The semiconductor device of claim 21, wherein a part of the gate insulating film located under the insulating sidewall includes a notch at the end thereof.

26. (Previously presented) The semiconductor device of claim 21, wherein a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.

27. (Previously presented) The semiconductor device of claim 21, wherein an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall.

28. (Previously presented) The semiconductor device of claim 21, wherein the insulating sidewall has a double layer structure including an oxide film and a nitride film.

29. (Previously presented) The semiconductor device of claim 21, wherein the insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film.

30. (Previously presented) The semiconductor device of claim 21, wherein a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length.

31. (Previously presented) The semiconductor device of claim 21, wherein the end of the gate insulating film located under the insulating sidewall has a tapered surface.

32. (Previously presented) The semiconductor device of claim 21, wherein the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof.

33. (Previously presented) The semiconductor device of claim 21, wherein the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length.

REMARKS

I. Introduction

In response to the pending Office Action, the Applicants have amended the specification so as to update the priority information. Applicants have also amended claim 21 to clarify the intended subject matter. The scope of claim 21 remains the same. No new matter has been added.

Applicants and Applicants' attorney would like to thank Examiner Luu for his time and courtesy during the interview conducted on June 27, 2013 during which it was agreed that the pending claims were patentable over the cited prior art reference. A summary of the discussions conducted during the interview is set forth below.

For all of the following reasons, Applicants respectfully submits that the application is now in condition for allowance.

II. The Rejection Of The Claims Under 35 U.S.C. § 102

Claims 21-25 and 27-33 were rejected under 35 U.S.C. § 102(e) as being anticipated by USP No. 6,992,358 to Hiedi. As agreed upon during the interview, claim 21 is patentable over Hiedi for at least the following reasons.

Claim 21 relates to a semiconductor device comprising: a gate insulating film formed on an active region in a substrate and including Hf; and a gate electrode formed on the gate insulating film; a insulating sidewall formed on each side surface of the gate electrode. Claim 21 further recites that the width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length, and an end of the gate insulating film under the

insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode.

Turning to the pending rejection and the cited prior art, it is asserted that layer 102 of Hiedi shown in Fig. 3C corresponds to the recited gate insulating film. However, layer 102 of Hiedi is not a gate insulating film. It is a buried oxide film 102 as described in col. 4, line 56 of Hieda.

It is further asserted that layer 101 of Hiedi shown in Fig. 3C corresponds to the active region in the substrate. However, layer 101 of Hieda is not an active region in a substrate. It is a p-type silicon substrate 101 as described in col. 4, line 58 of Hieda.

Finally, it is asserted that layer 113b of Hiedi shown in Fig. 3C is a gate electrode. However, layer 113b of Hieda is not a gate electrode. It is a drain region 113b as described in col. 5, line 5 of Hieda.

Thus, contrary to the assertions set forth in the pending rejection, the foregoing makes clear that the elements of Fig. 3C of Hieda do not correspond to the elements recited by claim 21, and therefore claim 21 is not anticipated by Hieda.

Accordingly, as it is well known that the factual determination of lack of novelty under 35 U.S.C. § 102 requires the identical disclosure in a single reference of each element of a claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art, *Halifax Ltd. v. Blok-Look, Ltd.*, 208 F.3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048,

32 USPQ2d 1017 (Fed. Cir. 1994), and Hiedi fails to do so for at least the foregoing reasons, it is clear that Hiedi does not anticipate claim 21.

III. Double Patenting Rejection

In response to the double patenting rejection in view of USP No. 8,253,180, Applicants submit concurrently herewith a terminal disclaimer so as to overcome the double patenting rejection. Thus, it is respectfully submitted that the double patenting rejection has been overcome.

IV. Dependent Claims

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.,* 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as the pending independent claim is patentable for at least the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable.

V. Summary

Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited.

Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

/Michael E. Fogarty/

Michael E. Fogarty
Registration No. 36,139

500 North Capitol Street, N.W.
Washington, DC 20001
Phone: 202.756.8000 MEF:MWE
Facsimile: 202.756.8087
Date: July 1, 2013

Please recognize our Customer No. 53080 as our correspondence address.

DM_US 43498555-1.085393.0808

Electronic Acknowledgement Receipt

EFS ID:	16206570
Application Number:	13547913
International Application Number:	
Confirmation Number:	2994
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Junji Hirase
Customer Number:	53080
Filer:	Michael E. Fogarty
Filer Authorized By:	
Attorney Docket Number:	085393-0808
Receipt Date:	01-JUL-2013
Filing Date:	12-JUL-2012
Time Stamp:	17:06:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		085393_0808.pdf	69199 6acab95f428ed9cf48a9e67c0cf03cdd899b23ce	yes	8

UMC 1002
UMC v. AICP

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Specification	2	2
	Claims	3	4
	Applicant Arguments/Remarks Made in an Amendment	5	8
Warnings:			
Information:			
	Total Files Size (in bytes):	69199	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/547,913	Filing Date 07/12/2012	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)		
	07/01/2013	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	* 13	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)		
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/CHERYL CLARK/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/547,913	07/12/2012	Junji Hirase	085393-0808	2994

53080 7590 07/08/2013

McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

EXAMINER	
LUU, CHUONG A	
ART UNIT	PAPER NUMBER
2898	

NOTIFICATION DATE	DELIVERY MODE
07/08/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mweipdocket@mwe.com

PTOL-90A (Rev. 04/07)

UMC 1002
UMC v. AICP

Applicant-Initiated Interview Summary	Application No.	Applicant(s)	
	13/547,913	HIRASE ET AL.	
	Examiner	Art Unit	
	CHUONG A. LUU	2898	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Chuong A. Luu*.

(2) *Michael Fogarty*.

(3) *Fumiya Sano*.

(4) _____.

Date of Interview: *27 June 2013*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☒102 ☐103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *21*.

Identification of prior art discussed: *Hieda et al. (U.S. Pat. No. 6,992,358)*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

The participants discussed: 1) Non-Final Rejection of Hieda's reference (Examiner agrees with applicant's representative positon); 2) The Applicant's representative will file TD to respond to double patenting rejection.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/CHUONG A LUU/
Primary Examiner, Art Unit 2898

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

———

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

UMC 1002
UMC v. AICP

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

53080 7590 09/09/2013

McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

EXAMINER
LUU, CHUONG A

ART UNIT	PAPER NUMBER
2898	

DATE MAILED: 09/09/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/547,913	07/12/2012	Junji Hirase	085393-0808	2994

TITLE OF INVENTION: SEMICONDUCTOR DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	12/09/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

53080 7590 09/09/2013
McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/547,913	07/12/2012	Junji Hirase	085393-0808	2994

TITLE OF INVENTION: SEMICONDUCTOR DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	12/09/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
LUU, CHUONG A	2898	257-410000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29	NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
❑ Applicant asserting small entity status. See 37 CFR 1.27	NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
❑ Applicant changing to regular undiscounted fee status.	NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/547,913	07/12/2012	Junji Hirase	085393-0808	2994

53080 7590 09/09/2013

McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2898	

DATE MAILED: 09/09/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UMC 1002
UMC v. AICP

Notice of Allowability	Application No. 13/547,913	Applicant(s) HIRASE ET AL.	
	Examiner CHUONG A. LUU	Art Unit 2898	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *July 01, 2013*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *21-33*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☒ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☒ Certified copies of the priority documents have been received in Application No. *13/037,831* .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

   Interim copies:

   a) ☐ All b) ☐ Some c) ☐ None of the: Interim copies of the priority documents have been received.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 7/12/2012
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

DETAILED ACTION

Terminal Disclaimer

The terminal disclaimer filed on July 01, 2013 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of the US Patent Number 8,253,180 has been reviewed and is accepted. The terminal disclaimer has been recorded.

The assignment document filed on July 01, 2013 is acceptable as the documentary evidence required by 37 CFR 3.73. If the assignment document is not already recorded with the Patent and Trademark Office, it is suggested that the assignment document be submitted for recording among the Office assignment records. See 37 CFR 3.11 and MPEP § 302.

Allowable Subject Matter

Claims 21-33 are allowed.

The following is an examiner's statement of reasons for allowance: The invention is allowable after it was rejected as Obvious Double Patenting in the first office action. However, the applicant filed terminal disclaimer in a timely manner in compliance with 37 CFR 1.321(c). It may be used to overcome an actual patent is shown to be commonly owned with this application.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

UMC 1002
UMC v. AICP

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHUONG A. LUU whose telephone number is (571)272-1902. The examiner can normally be reached on M-F (6:30-3:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio Maldonado can be reached on (571) 272-1864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/CHUONG A LUU/
Primary Examiner, Art Unit 2898

UMC 1002
UMC v. AICP

August 25, 2013

UMC 1002
UMC v. AICP

IN THE SPECIFICATION:

Please amend the following paragraph on page 1 of the specification as follows:

-- RELATED APPLICATIONS

This application is a Divisional of U.S. Application No. 13/037,831, filed on March 1, 2011, now U.S. Patent No. 8,253,180, which is a Divisional of U.S. Application No. 12/505,799, filed on July 20, 2009, now U.S. Patent No. 7,923,764, which is a Divisional of U.S. Application No. 11/491,260, filed on July 24, 2006, now U.S. Patent No. 7,579,227, claiming priority of Japanese Patent Application No. 2005-227457, filed on August 5, 2005, the entire contents of each of which are hereby incorporated by reference. --

It is OK to enter.
CAL
08/25/2013

IN THE TITLE:

Please amend the title as follows:

SEMICONDUCTOR DEVICE ~~AND METHOD FOR FABRICATING THE SAME~~

It is OK to enter.
CAL
08/25/2013

UMC 1002
UMC v. AICP

IN THE SPECIFICATION:

Please insert the following new paragraph after the Title and before the "BACKGROUND OF THE INVENTION"

-- RELATED APPLICATIONS

This application is a Divisional of U.S. Application No. 13/037,831, filed on March 1, 2011, which is a Divisional of U.S. Application No. 12/505,799, filed on July 20, 2009, now U.S. Patent No. 7,923,764, which is a Divisional of U.S. Application No. 11/491,260, filed on July 24, 2006, now U.S. Patent No. 7,579,227, claiming priority of Japanese Patent Application No. 2005-227457, filed on August 5, 2005, the entire contents of each of which are hereby incorporated by reference. --

UMC 1002
UMC v. AICP

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S241	18	("20030209761" | "20040150520" | "20040178451" | "20050040464" | "20050051843" | "20050110085" | "4979014" | "6437404" | "6538916" | "6580132" | "6639246" | "6646307" | "6687152" | "6724046" | "6740938" | "6744390" | "6800513" | "6822071").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/03 21:10
S242	72	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) same (high adj dielectric adj constant)) and overlap$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:10
S244	9	(("6992358") or ("6929992") or ("6642071") or ("20060121740") or ("20030022422") or ("20040004234") or ("20040129997") or ("20050121733") or ("20050127436")).PN.	US-PGPUB; USPAT	OR	OFF	2012/04/03 21:10
S245	3	(("6,992,358") or ("7579227") or ("20050121733")).PN.	US-PGPUB; USPAT	OR	OFF	2012/04/03 21:10
S246	72	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) same (high adj dielectric adj constant)) and overlap$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:10
S247	1	("5473168").PN.	US-PGPUB; USPAT	OR	OFF	2012/04/03 21:11
S248	2	12/190015	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:11
S249	24	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) near (high adj dielectric adj constant)) and overlap$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:12
S250	10	"6992358"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:13
S251	1135	gate and ((gate adj (oxide or insulat$4 or dielectric)) with (notch$4 or undercut$4))	US-PGPUB; USPAT;	OR	ON	2012/04/03 21:13

			USOCR			
S252	24	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) near (high adj dielectric adj constant)) and overlap$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:13
S253	155	gate and ((gate adj (oxide or insulat$4 or dielectric)) near (notch$4 or undercut$4))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/03 21:13
S254	23	gate and ((gate adj (oxide or insulat$4 or dielectric)) adj (notch$4 or undercut$4))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/03 21:13
S255	202	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) and (high adj dielectric adj constant)) and overlap$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:14
S256	2	(("6642071") or ("6929992")).PN.	USPAT	OR	OFF	2012/04/03 21:14
S257	6	(257/296,295,310.ccls.) and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:14
S258	3	(("20070228442") or ("20040171280") or ("20030207097")).PN.	US-PGPUB; USPAT	OR	OFF	2012/04/03 21:15
S259	1632	hirase.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:15
S260	91	S259 and junji	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:15
S261	0	S260 and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) adj (high adj dielectric adj constant))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:15
S262	0	S260 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2012/04/03 21:16

			IBM_TDB			
S263	308	sebe.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:16
S264	20	S263 and akio	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:16
S265	0	S264 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:17
S266	19806	kotani.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:17
S267	258	S266 and naoki	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:18
S268	0	S267 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:18
S269	0	okazaki and gen and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:18
S270	0	aida and kazuhiko and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:18
S271	0	takeoka and shinji and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR;	OR	ON	2012/04/03 21:19

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S272	38	(((semiconductor) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) adj (high adj dielectric adj constant)))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:19
S273	22	(((semiconductor) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) adj (high adj dielectric adj constant)))).clm.	US-PGPUB	OR	ON	2012/04/03 21:19
S274	5	(("20050127436") or ("6284630") or ("20020163039") or ("20010028086") or ("5223445")).PN.	US-PGPUB; USPAT	OR	OFF	2012/04/03 21:19
S275	3	09/824672	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:19
S276	2	09/848431	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:20
S277	8	(("20050127436") or ("6284630") or ("20020163039") or ("20010028086") or ("5223445") or ("6509612") or ("6794258") or ("6614081")).PN.	US-PGPUB; USPAT	OR	OFF	2012/04/03 21:20
S278	4	10/904875	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:20
S279	2363	(257/324).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/04/03 21:23
S280	7	(257/296,295,310,324,410,411.ccls.) and (gate or electrode) and ((gate or electrode) adj (insulat$4 or dielectric or oxide)) and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:23
S281	1412	(257/410).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/04/03 21:23

S282	198	257/e29.132.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:24
S283	1713	257/e29.133.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:24
S284	1631	257/e29.137.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:25
S285	181	257/e29.138.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:25
S286	684	257/e29.162.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:25
S287	602	257/e29.165.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:25
S288	2	(257/e29.132,e29.133,e29.134,e29.135,e29.136,e29.137,e29.138,e29.138,e29.162,e29.163,e29.164,e29.164,e29.165.ccls.) and (gate or electrode) and ((gate or electrode) adj (insulat$4 or dielectric or oxide)) and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:25
S289	115	(257/296,295,310,324,410,411.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:27
S290	85	(257/296,295,310,324,410,411.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2012/04/03 21:27

			EPO; JPO; DERWENT; IBM_TDB			
S291	280	("257"/$.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:27
S292	57	(257/e29.132,e29.133,e29.134,e29.135,e29.136,e29.137,e29.138,e29.138,e29.162,e29.163,e29.164,e29.164,e29.165.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:28
S293	257	(257/e$.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:28
S294	132	("438"/$.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:28
S295	5455	(257/296,295,310,324,410,411.ccls.) and (gate or electrode) and ((gate or electrode) adj (dielectric or oxide or insulat$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:29
S296	85	(257/296,295,310,324,410,411.ccls.) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:29
S297	772	(257/296,295,310,324,410,411.ccls.) and (((gate or electrode) adj (dielectric or oxide or insulat$4)) with ((high adj dielectric adj constant) or (ferroelectric))) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:30
S298	185	(257/296,295,310,324,410,411.ccls.) and (((gate or electrode) adj (dielectric or oxide or insulat$4)) near ((high adj dielectric adj constant) or (ferroelectric))) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:30
S299	1015	(257/296,295,310,324,410,411.ccls.) and (((gate or electrode) adj (dielectric or oxide or insulat$4)) same ((high adj	US-PGPUB;	OR	ON	2012/04/03

		dielectric adj constant) or (ferroelectric))) and @ad<="20050805"	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			21:30
S300	2	10/519799	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:30
S301	2	"7186604"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:31
S302	3	11/491260	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:31
S303	1528	(257/410).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:37
S304	1	13/547913	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:37
S305	2	13/037831	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:37
S306	3	12/505799	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:38
S307	4	11/491260	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2013/04/07 14:38

			DERWENT; IBM_TDB			
S308	5	(("20030022422") or ("20040004234") or ("20040129997") or ("20050121733") or ("20060121740")).PN.	US-PGPUB	OR	OFF	2013/04/07 14:38
S310	3	(("8253180") or ("7923764") or ("7579227")).PN.	US-PGPUB; USPAT	OR	OFF	2013/04/07 14:39
S311	3362	(257/295).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:39
S312	3	(("7,579,227") or ("20050121733") or ("6,992,358")).PN.	US-PGPUB; USPAT	OR	OFF	2013/04/07 14:39
S313	8	(("20030022422") or ("20040004234") or ("20040129997") or ("20050121733") or ("20060121740") or ("6,992,358") or ("6,929,992") or ("6,642,071")).PN.	US-PGPUB; USPAT	OR	OFF	2013/04/07 14:39
S314	2	(("7923764") or ("7579227")).PN.	US-PGPUB; USPAT	OR	OFF	2013/04/07 14:39
S315	3	(("7923764") or ("7579227") or ("6,992,358")).PN.	US-PGPUB; USPAT	OR	OFF	2013/04/07 14:40
S316	3	(("7923764") or ("7579227") or ("20040227185")).PN.	US-PGPUB; USPAT	OR	OFF	2013/04/07 14:40
S317	23	("20020053711" | "5889331" | "6314021" | "6512258" | "6518155" | "6765273" | "6777283" | "6777759").PN. OR ("2004/0227185" | "7067881").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/04/07 14:40
S318	1613	(257/411).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:41
S319	1528	(257/410).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:41
S320	5625	(257/296).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:41
S321	2769	(257/368).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:41
S322	4179	(257/369).CCLS.	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2013/04/07 14:41

			EPO; JPO; DERWENT; IBM_TDB			
S323	256	(257/389).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:42
S324	940	(257/392).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:42
S325	565	(257/393).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:42
S326	206	(257/395).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:42
S327	201	(257/405).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:42
S328	255	(257/406).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:42
S329	12	("20030022422" | "20040004234" | "20040129997" | "20050121733" | "20050127436" | "20060121740" | "6642071" | "6929992" | "6992358").PN. OR ("7579227").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/04/07 14:43
S330	3	12/505799	US-PGPUB; USPAT; USOCR	OR	ON	2013/04/07 14:43
S331	3362	(257/295).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/07 14:43
S332	1623	(257/310).CCLS.	US-PGPUB;	OR	OFF	2013/04/07

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			14:43
S333	3	09/916509	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:43
S334	19	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) adj (high adj dielectric adj constant)) and overlap$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:43
S335	18	("20030209761" | "20040150520" | "20040178451" | "20050040464" | "20050051843" | "20050110085" | "4979014" | "6437404" | "6538916" | "6580132" | "6639246" | "6646307" | "6687152" | "6724046" | "6740938" | "6744390" | "6800513" | "6822071").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/04/07 14:44
S336	1667	hirase.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:44
S337	1667	hirase.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:44
S338	95	S337 and junji	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:44
S339	0	S338 and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) adj (high adj dielectric adj constant))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:45
S340	0	S338 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:45
S341	332	sebe.inv.	US-PGPUB; USPAT;	OR	ON	2013/04/07 14:45

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S342	22	S341 and akio	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:46
S343	0	S342 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:46
S344	20513	kotani.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:46
S345	274	S344 and naoki	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:46
S346	0	S345 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:46
S347	41632	okazaki.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:47
S348	71	S347 and gen	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:47
S349	0	S348 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2013/04/07 14:47

			IBM_TDB			
S350	17970	aida.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:47
S351	172	S350 and kazuhiko	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:49
S352	0	S351 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:50
S353	2816	takeoka.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:50
S354	203	S353 and shinji	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:50
S355	0	S354 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 14:50
S357	11	(("6,992,358") or ("6,929,992") or ("6,642,071") or ("20060121740") or ("20030022422") or ("20040004234") or ("20040129997") or ("20050121733") or ("20050127436") or ("7,579,227") or ("20050121733") or ("6,992,358") or ("20040227185")).PN.	US-PGPUB; USPAT	OR	OFF	2013/04/07 14:55
S358	4	(("8253180") or ("7923764") or ("7579227") or ("6992358")).PN.	US-PGPUB; USPAT	OR	OFF	2013/04/07 17:11
S360	1	13/405639	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/07 17:47
S361	205	257/e29.132.ccls.	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2013/08/25 19:39

			EPO; JPO; DERWENT; IBM_TDB			
S362	186	257/e29.138.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/25 19:39
S363	702	257/e29.162.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/25 19:39
S364	620	257/e29.165.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/25 19:40
S365	344	257/e29.164.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/25 19:40
S366	7557	257/e29.255.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/25 19:41
S367	6	(("7018873") or ("6929992") or ("6992358") or ("20060121740") or ("20050121733") or ("7579227")).PN.	US-PGPUB; USPAT	OR	OFF	2013/08/25 19:42
S368	3	(("8253180") or ("7923764") or ("7579227")).PN.	US-PGPUB; USPAT	OR	OFF	2013/08/25 19:43
S369	10	"8253180" "7923764" "7579227"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/25 19:43
S370	14	("20030022422" | "20040004234" | "20040129997" | "20040227185" | "20050121733" | "20050127436" | "20060121740" | "6642071" | "6929992" | "6992358" | "7579227" | "7923764").PN. OR ("7579227" | "7923764" | "8253180").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/25 19:43
S371	1198	257/e29.242.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/25 19:44

S372	2803	257/e29.266.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/25 19:44

8/29/2013 8:17:51 PM
C:\Users\cluu\Documents\EAST\Workspaces\13547913.wsp

7/12/2012

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Substitute for form 1449/PTO)

ATTY. DOCKET NO.	SERIAL NO.
085393-0808	~~Divisional of U.S. Serial No. 13/037,831~~ 13/547,913
APPLICANT: Junji HIRASE, et al.	
FILING DATE: July 12, 2012	GROUP: 2898 ~~Not Yet Assigned~~

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
CAL		US	7,923,764	04-2011	Hirase et al.	
		US	2004/0227185	11-18-2004	MATSUMOTO et al.	Corresponds w/ JP 2004-241755
		US	6,992,358	01-2006	Hieda et al.	
		US	6,929,992	08-2005	Djomehri et al.	
		US	6,642,071	11-2003	Cheng, Jia-Shyong	
		US	2006/0121740 A2	6/8/2006	SAKAI et al	
		US	2003/0022422 A1	01-30-2003	TORII et al.	
		US	2004/0004234 A1	01-08-2004	YAGISHITA et al.	
		US	2004/0129997 A1	07-08-2004	MORIFUJI	
		US	2005/0121733 A1	06-09-2005	CHEN et al.	
		US	2005/0127436 A1	06-16-2005	HENSON et al.	Corresponds w/ CN 1610129 A
		US	7,579,227	08-2009	Hirase et al.	
		US	2005/0121733	06-2005	Chen et al.	
CAL		US	6,992,358	01-2006	Hieda et al.	

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes3-Number4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No
CAL		JP 2005-064190	03-10-2005	TOSHIBA CORP		English translation only	
CAL		JP 2004-172178	06-17-2004			X	
CAL		JP 2003-258241	09-12-2003			X	
CAL		CN 1610129 A	04-27-2005		Corresponds w/ US 2005/0127436		
CAL		JP 2004-356576	12-16-2004	SEMICONDUCTOR LEADING EDGE TECHNOLOGIES INC.			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
CAL		WATANABE, Ken, Partial English Translation of "HfSiON-CMOS technology for achieving high performance and high reliability," SEMI FORUM Japan, 2005, IT System & ULSI Technology,
		HORI, Takashi, "1/4-μm LATID (LArge-Tilt-angle Implanted Drain) TECHNOLOGY FOR 3.3-V OPERATION", CH2637-7/89/0000-0777 1989 IEEE, IEDM 89-777-780-IEDM 89
		SAYAMA, et al., H.,, "80nm CMOSFET Technology Using Double Offset-Implanted Source/Drain Extension and Low Temperature SiN Process", IEDM 2000, IEDM 00-239-242-IEDM 00
		U.S. Office Action issued in U.S. Patent Application No. 11/543,865 dated on November 12, 2008
		Chinese Office Action, with English Translation, issued in Chinese Patent Application No. CN 200610093872.2, dated March 20, 2009.
		Notice Allowance issued in United States Patent Application No. 13/037,831, mailed April 13, 2012.
		Notice Allowance issued in United States Patent Application No. 12/505,799, mailed December 13, 2010.
CAL		Notice Allowance issued in United States Patent Application No. 11/491,260, mailed June 2, 2009.

EXAMINER	DATE CONSIDERED
/CHUONG A. LUU/	08/25/2013

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

UMC 1002
UMC v. AICP

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
13/547,913	HIRASE ET AL.
Examiner	**Art Unit**
CHUONG A. LUU	2898

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date								
Final	Original	8/25/13								
	1	-								
	2	-								
	3	-								
	4	-								
	5	-								
	6	-								
	7	-								
	8	-								
	9	-								
	10	-								
	11	-								
	12	-								
	13	-								
	14	-								
	15	-								
	16	-								
	17	-								
	18	-								
	19	-								
	20	-								
1	21	=								
2	22	=								
3	23	=								
4	24	=								
5	25	=								
6	26	=								
7	27	=								
8	28	=								
9	29	=								
10	30	=								
11	31	=								
12	32	=								
13	33	=								
	34									
	35									
	36									
	37									
	38									
	39									
	40									
	41									
	42									
	43									
	44									
	45									
	46									
	47									
	48									
	49									
	50									

Claim		Date								
Final	Original									
	51									
	52									
	53									
	54									
	55									
	56									
	57									
	58									
	59									
	60									
	61									
	62									
	63									
	64									
	65									
	66									
	67									
	68									
	69									
	70									
	71									
	72									
	73									
	74									
	75									
	76									
	77									
	78									
	79									
	80									
	81									
	82									
	83									
	84									
	85									
	86									
	87									
	88									
	89									
	90									
	91									
	92									
	93									
	94									
	95									
	96									
	97									
	98									
	99									
	100									

Claim		Date								
Final	Original									
	101									
	102									
	103									
	104									
	105									
	106									
	107									
	108									
	109									
	110									
	111									
	112									
	113									
	114									
	115									
	116									
	117									
	118									
	119									
	120									
	121									
	122									
	123									
	124									
	125									
	126									
	127									
	128									
	129									
	130									
	131									
	132									
	133									
	134									
	135									
	136									
	137									
	138									
	139									
	140									
	141									
	142									
	143									
	144									
	145									
	146									
	147									
	148									
	149									
	150									

Issue Classification	Application/Control No.	Applicant(s)/Patent under Reexamination	
	13/547,913	HIRASE ET AL.	
	Examiner	Art Unit	
	CHUONG A. LUU	2898	

ISSUE CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)							
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)						
257	410	257	411	295	310				
INTERNATIONAL CLASSIFICATION									
H 01 L 29/76									
H 01 L 29/94									
H 01 L 27/108									
H 01 L 31/119									
H 01 L 31/062									

---------- (Assistant Examiner) (Date)	/Chuong A. Luu/ August 25, 2013 (Primary Examiner) (Date)	Total Claims Allowed: 13
(Legal Instruments Examiner) (Date)		O.G. Print Claim(s): 1 / O.G. Print Fig.: 8

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1	11	31		61		91		121		151		181
	2	12	32		62		92		122		152		182
	3	13	33		63		93		123		153		183
	4		34		64		94		124		154		184
	5		35		65		95		125		155		185
	6		36		66		96		126		156		186
	7		37		67		97		127		157		187
	8		38		68		98		128		158		188
	9		39		69		99		129		159		189
	10		40		70		100		130		160		190
	11		41		71		101		131		161		191
	12		42		72		102		132		162		192
	13		43		73		103		133		163		193
	14		44		74		104		134		164		194
	15		45		75		105		135		165		195
	16		46		76		106		136		166		196
	17		47		77		107		137		167		197
	18		48		78		108		138		168		198
	19		49		79		109		139		169		199
	20		50		80		110		140		170		200
1	21		51		81		111		141		171		201
2	22		52		82		112		142		172		202
3	23		53		83		113		143		173		203
4	24		54		84		114		144		174		204
5	25		55		85		115		145		175		205
6	26		56		86		116		146		176		206
7	27		57		87		117		147		177		207
8	28		58		88		118		148		178		208
9	29		59		89		119		149		179		209
10	30		60		90		120		150		180		210

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination
	13/547,913	HIRASE ET AL.
	Examiner	Art Unit
	CHUONG A. LUU	2898

SEARCHED			
Class	Subclass	Date	Examiner
257	410 295 411 296 368 369 389 392	4/7/2013	CAL
257	393 395 405	4/7/2013	CAL
257	406 310	4/7/2013	CAL
Update	Searched	8/25/2013	CAL

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
PG PUB TEXT SEARCH, See interference search printout.		8/25/2013	CAL

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
Please see the attachment.	4/7/2013	CAL
Please see the attachment including East Search (US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB)	8/25/2013	CAL
(257/e29.132, e29.138, e29.162, e29.165, e29.164, e29.255, e29.242, e29.266).ccls.	8/25/2013	CAL

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

53080 7590 09/09/2013
McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/547,913	07/12/2012	Junji Hirase	085393-0808	2994

TITLE OF INVENTION: SEMICONDUCTOR DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	12/09/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
LUU, CHUONG A	2898	257-410000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 McDermott Will & Emery LLP
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: PANASONIC CORPORATION

(B) RESIDENCE: (CITY and STATE OR COUNTRY): OSAKA, JAPAN

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 500417 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29	NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
❑ Applicant asserting small entity status. See 37 CFR 1.27	NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
❑ Applicant changing to regular undiscounted fee status.	NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Michael E. Fogarty/ Date October 14, 2013

Typed or printed name Michael E. Fogarty Registration No. 36,139

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal

Application Number:	13547913
Filing Date:	12-Jul-2012
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Junji Hirase
Filer:	Michael E. Fogarty/Maung Kyaw
Attorney Docket Number:	085393-0808

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	1780	1780
Publ. Fee- Early, Voluntary, or Normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**2080**

Electronic Acknowledgement Receipt

EFS ID:	17118309
Application Number:	13547913
International Application Number:	
Confirmation Number:	2994
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Junji Hirase
Customer Number:	53080
Filer:	Michael E. Fogarty/Maung Kyaw
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0808
Receipt Date:	14-OCT-2013
Filing Date:	12-JUL-2012
Time Stamp:	15:03:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$2080
RAM confirmation Number	12212
Deposit Account	500417
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

UMC 1002
UMC v. AICP

1	Issue Fee Payment (PTO-85B)	IF-085393-0808.pdf	107667 26281566a644ad5adebdaf79564bb458f0d783a7	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	31970 61510016670592cb17b5753c1bf85920a666b36b	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	139637		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/547,913	11/19/2013	8587076	085393-0808	2994

53080 7590 10/30/2013

McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Junji Hirase, Osaka, JAPAN;
Akio Sebe, Osaka, JAPAN;
Naoki Kotani, Hyogo, JAPAN;
Gen Okazaki, Hyogo, JAPAN;
Kazuhiko Aida, Chiba, JAPAN;
Shinji Takeoka, Osaka, JAPAN;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.