

REQUEST FORM FOR DIVISIONAL APPLICATION UNDER 37 CFR 1.53(b)

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Examiner: LUU, CHUONG A.

BOX New Applications

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P.O. Box 1450

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Sir:

This is a Request for filing a Divisional application under 37 CFR 1.53(b) of pending prior application No. 12/505,799, filed on July 20, 2009, entitled **SEMICONDUCTOR DEVICE (as amended)**, by the following named inventor(s): Junji HIRASE, Akio SEBE, Naoki KOTANI, Gen OKAZAKI, Kazuhiko AIDA, Shinji TAKEOKA.

1. ☒ I hereby state that the enclosed application contains no new matter.
2. Oath or Declaration
 - a. ☐ Newly executed (original or copy)
 - b. ☒ Copy from a prior application (37 CFR 1.63(d))
 - i. ☐ Deletion of inventor(s)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
3. ☒ Incorporation By Reference (useable if Box 2b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 2b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
4. ☒ Preliminary Amendment is enclosed.
5. ☒ An Information Disclosure Statement and PTO1449 Form are submitted herewith.
6. ☒ Cancel claims 1-20.

7. The filing fee is calculated on the basis of the claims existing in the prior application as amended at 4 and 6 above:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	22	-20	2	\$52.00	\$104.00
Independent Claims	1	-3	0	\$220.00	\$0.00
Multiple Dependent Claim(s)					\$0.00
Sheets of specification and drawing (\$270.00 for each 50 sheets in excess of 100)					\$0.00
Basic Filing Fee					\$330.00
Patent Search Fee					\$540.00
Patent Examination Fee					\$220.00
Total of Above Calculations					\$1,194.00
Less ½ for Small Entity					\$0.00
Assignment & Recording Fee					\$0.00
Total Fee					\$1,194.00

8. ☐ A Statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27 was filed in prior application and such status is still proper and desired.
9. ☒ **PLEASE CHARGE DEPOSIT ACCOUNT 500417 in the amount of \$1,194.00.** Commissioner is authorized to charge any fees which may be required or credit any overpayment to Deposit Account No. 500417.
10. ☒ The Commissioner is hereby authorized to charge fees under 37 CFR 1.16 and 1.17 which may be required, including any extension of time fees to maintain the pendency of the parent Application No. 12/505,799 or credit any overpayment to Deposit Account No. 500417.
11. ☒ Priority of Application No. 2005-227457 filed on August 5, 2005, in Japan is claimed under 35 USC 119. The certified priority document(s) were filed in Application No. 11/491,260 on July 24, 2006.
12. ☒ The prior application is assigned of record to
- PANASONIC CORPORATION**
Osaka, Japan
13. ☒ The power of attorney in the prior application is to:
- McDermott Will & Emery LLP
14. ☐ Also enclosed:

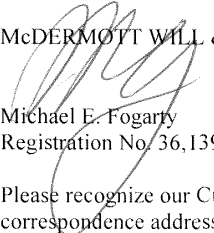
15. ☐ A petition, fee and response has been filed to extend the term in the pending prior application until .

Address all future communications to: (May only be completed by applicant, or attorney or agent of record)

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Respectfully submitted,

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SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

BACKGROUND OF THE INVENTION

5 Field of the Invention

The present invention relates to a semiconductor device and a method for fabricating the semiconductor device. Specifically, the present invention relates to a structure of a MISFET (metal insulator semiconductor field-effect transistor) and a method for fabricating the MISFET and, more particularly, relates to techniques for improving the
10 driving power and reliability of a MISFET.

Description of Prior Art

In recent years, as the degree of integration, function and operation speed of semiconductor integrated circuit devices have been highly improved, there have been attempts to reduce a junction depth of an extension according to a scaling rule and, at the
15 same time, to use, as a gate insulating film of a MISFET, a high dielectric constant film formed of a Hf based oxide, Al based oxide or the like, which has a relative dielectric constant of 10 or more, instead of an SiO₂ based insulating film having a relative dielectric constant of about 4.

FIGS. **16A** and **16B** are cross-sectional views illustrating respective structures of
20 known MISFETs using a high dielectric constant gate insulating film, respectively (see Ken Watanabe, *HfSiON-CMOS technology for achieving high performance and high reliability*, Semi. Forum Japan, 2005).

As shown in FIG. **16A**, a gate electrode **105** is formed on a region of a well **102** surrounded by a STI (shallow trench isolation) **103**. The region of the well **102** surrounded
25 by the STI serves as an active region of a substrate **101**. The gate electrode **105** is

provided on the region with a high dielectric constant gate insulating film **104** interposed therebetween. An insulating sidewall **107** is formed on each side of the gate electrode **105**. An extension region **110** is formed in part of the well **102** located under the insulating sidewall **107**. A pocket region **111** is formed in part of the well **102** located under the extension region **110**. Source/drain regions **112** are formed so that each of the source/drain regions **112** is provided in parts of the well **102** located at the external side to the extension region **110** and the pocket region **111** when viewed from the gate electrode **105**.

A structure shown in FIG. **16B** is different from a structure shown in FIG. **16A** in that a sidewall **107** is formed on each side of a gate electrode **105** with an insulating offset sidewall **106** interposed therebetween. Thus, an overlapping amount of the gate electrode **105** and an extension region **110** can be optimized in a simple manner.

SUMMARY OF THE INVENTION

However, in a structure of a known MISFET using a high dielectric constant gate insulating film, side end portions of the high dielectric constant gate insulating film are in direct contact with sidewalls. Thus, in forming sidewalls of, for example, a silicon oxide film or the like, a composition of the side end portions of the high dielectric constant gate insulating film becomes closer to SiO₂ or like other inconvenience occurs. As a result, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film is caused at gate electrode end part, so that device characteristics of the MISFET are deteriorated and the reliability of the gate insulating film is degraded.

In view of the above-described problems, it is therefore an object of the present invention to improve characteristics of a MISFET without degrading of a high dielectric constant gate insulating film.

To achieve the above-described object, the inventors of the present application have

devised a MISFET structure in which a high dielectric constant gate insulating film is kept remaining under sidewalls to prevent end portions of the high dielectric constant gate insulating film from being in contact with the sidewalls, and a method for forming the MISFET structure. In the mean time, when the high dielectric constant gate insulating film is kept remaining under the sidewalls, a capacitance between gate/drain regions is increased, thus resulting in adverse effects on circuit speed. Also, in such cases, when extension implantation or LDD (lightly doped drain) implantation is performed, it is necessary to implant ions through a high dielectric constant film. Thus, when ion implantation is performed, expansion of an implanted impurity in the depth direction is increased, in other words, a junction point of an extension or an LDD is located at a large depth, so that desired device characteristics can not be obtained. This is because implantation acceleration energy is increased for the following reasons.

Reason 1) With use of a high dielectric constant film as a gate insulating film, a desired dielectric constant can be achieved even without having the thickness of the high dielectric constant film reduced. Therefore, the thickness of the high dielectric constant film has to be set at a large value.

Reason 2) A high dielectric constant film contains heavy metal and R_p (projection range) of implanted ions is small.

To cope with this problem, the inventors have devised a MISFET structure in which a high dielectric constant gate insulating film is kept remaining under sidewalls and part of the high dielectric constant gate insulating film located under the sidewalls is made to have a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under a gate electrode, and a method for forming the MISFET structure.

Specifically, a semiconductor device according to the present invention includes: a

gate electrode formed on the high dielectric constant gate insulating film; and an insulating sidewall formed on each side surface of the gate electrode. In the semiconductor device, the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall, and at least part of the high dielectric constant gate insulating film located under the insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

In the semiconductor device of the present invention, the insulating sidewall may include a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween, the high dielectric constant gate insulating film may be continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, and part of the high dielectric constant gate insulating film located under the first insulating sidewall may have a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

When the insulating sidewall includes the first insulating sidewall and the second insulating sidewall, the high dielectric constant gate insulating film may be formed so as not to be located under the second insulating sidewall.

When the insulating sidewall includes the first insulating sidewall and the second insulating sidewall, the high dielectric constant gate insulating film may be continuously formed so as to extend from under the gate electrode to under the second insulating sidewall, and part of the high dielectric constant gate insulating film located under the second insulating sidewall may have the same thickness as a thickness of part of the high dielectric constant gate insulating film located under the first insulating sidewall.

When the insulating sidewall includes the first insulating sidewall and the second

insulating sidewall, the high dielectric constant gate insulating film may be continuously formed so as to extend from under the gate electrode to under the second insulating sidewall, and part of the high dielectric constant gate insulating film located under the second insulating sidewall may have a smaller thickness than a thickness of part of the
5 high dielectric constant gate insulating film located under the first insulating sidewall.

In the semiconductor device of the present invention, the insulating sidewall may include a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween, the high dielectric constant gate insulating
10 film may be continuously formed so as to extend from under the gate electrode to under the second insulating sidewall, part of the high dielectric constant gate insulating film located under the first insulating sidewall may have the same thickness as a thickness of part of the high dielectric constant gate insulating film located under the gate electrode, and part of the high dielectric constant gate insulating film located under the second
15 insulating sidewall may have a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

In the semiconductor device of the present invention, the high dielectric constant gate insulating film may include a notch at a side end portion.

The semiconductor device of the present invention may further include a buffer
20 insulating film between the substrate and the high dielectric constant gate insulating film. In such a case, the buffer insulating film may be a silicon oxide film or a silicon oxynitride film.

In the semiconductor device of the present invention, the gate electrode may be a fully silicided gate electrode of which an entire region has been silicided.

25 A method for fabricating a semiconductor device according to the present invention

includes the steps of: a) forming a high dielectric constant gate insulating film on an active region of a substrate; b) forming a gate electrode on the high dielectric constant gate insulating film; c) etching, after the step b), part of the high dielectric constant gate insulating film located in an external side to the gate electrode to reduce a thickness of the part; and d) forming, after the step c), an insulating sidewall on a side surface of the gate electrode.

The method for fabricating a semiconductor device according to the present invention may further include, after the step d), the step of removing part of the high dielectric constant gate insulating film located in an external side to the insulating sidewall.

10 In the method for fabricating a semiconductor device according to the present invention, the insulating sidewall may include a first insulating sidewall and a second insulating sidewall, and the step d) may include the step d1) of forming the first insulating sidewall on a side surface of the gate electrode and the step of d2) of forming the second insulating sidewall on the side surface of the gate electrode with the first insulating
15 sidewall interposed therebetween.

When the step d) includes the step d1) and the step d2), the method for fabricating a semiconductor device according to the present invention may further include, between the step d) and the step d2), the step of removing part of the high dielectric constant gate insulating film located in the external side to the first insulating sidewall.

20 When the step d) includes the step d1) and the step d2), the method for fabricating a semiconductor device according to the present invention may further include, between d1) and the step d2), the step of etching part of the high dielectric gate insulating film located in an external side to the first insulating sidewall to reduce a thickness of the part; and after the step d2), the step of removing part of the high dielectric constant gate insulating film
25 located in an external side to the second insulating sidewall.

In the method for fabricating a semiconductor device according to the present invention, the dielectric constant gate insulating film may be selectively removed by wet etching.

5 In the method for fabricating a semiconductor device according to the present invention, the step b) may include the step of forming a protective film for covering an upper surface of the gate electrode, and the method may further include, after the step d), the step of siliciding a surface of part of the active region located in the external side to the insulating sidewall, removing the protective film and then fully siliciding the gate electrode.

10 The method for fabricating a semiconductor device according to the present invention further includes, before the step a), the step of forming a buffer insulating film on the active region, and in the step a), the high dielectric constant gate insulating film may be formed on the active region with the buffer insulating film interposed therebetween.

According to the present invention, a high dielectric constant gate insulating film is
15 continuously formed so as to extend from under a gate electrode to under a sidewall. In other words, continuity of the high dielectric constant gate insulating film at a gate end portion is maintained. Thus, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film at the gate end portion, caused by a side end portion of the high dielectric constant gate insulating film being in direct contact with
20 a sidewall film, can be suppressed. Moreover, the high dielectric constant gate insulating film is formed so as to have a smaller thickness in the part located under the sidewall than a thickness of the part located under gate electrode. Thus, increase in a capacitance between a gate and a drain can be suppressed, so that adverse effects on circuit speed can be reduced. Furthermore, since extension implantation or LDD implantation is performed
25 through the part of the high dielectric constant film which has a small thickness, increase in

implantation acceleration energy can be suppressed. Accordingly, a shallow junction can be formed in an extension or a LDD in a simple manner. Therefore, device characteristics can be improved in a simple manner.

As has been described, the present invention relates to a semiconductor device and
5 a method for fabricating the semiconductor device. Specifically, when the present invention is applied to a MISFET including a high dielectric constant gate insulating film, the effect of improving the driving power and reliability of the MISFET can be achieved and is therefore very useful.

10 **BRIEF DESCRIPTION OF THE DRAWINGS**

FIG. 1 is a cross-sectional view illustrating a structure of a semiconductor device according to a first embodiment of the present invention.

FIG. 2 is a cross-sectional view illustrating a structure of a semiconductor device according to a second embodiment of the present invention.

15 FIG. 3 is a cross-sectional view illustrating a structure of a semiconductor device according to a second modified example of the second embodiment of the present invention.

FIG. 4 is a cross-sectional view illustrating a structure of a semiconductor device according to a third modified example of the second embodiment of the present invention.

20 FIG. 5 is a cross-sectional view illustrating a structure of a semiconductor device according to a third embodiment of the present invention.

FIG. 6 is a cross-sectional view illustrating a structure of a semiconductor device according to a modified example of the first embodiment of the present invention.

FIG. 7 is a cross-sectional view illustrating a structure of a semiconductor device
25 according to a first modified example of the second embodiment of the present invention.

FIG. 8 is a cross-sectional view illustrating a structure of a semiconductor device according to a modified example of the third embodiment of the present invention.

FIG. 9 is a cross-sectional view illustrating a structure of a semiconductor device according to a fourth embodiment of the present invention.

5 FIG. 10 is a cross-sectional view illustrating a structure of a semiconductor device according to a modified example of the fourth embodiment of the present invention.

FIGS. 11A through 11F are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to a fifth embodiment of the present invention.

10 FIGS. 12A through 12G are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to a sixth embodiment of the present invention.

FIGS. 13A through 13G are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to a seventh embodiment of the present
15 invention.

FIGS. 14A through 14G are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to an eighth embodiment of the present invention.

FIGS. 15A through 15D are cross-sectional views illustrating respective steps for
20 fabricating a semiconductor device according to the eighth embodiment of the present invention.

FIGS. 16A and 16B are cross-sectional views illustrating a structure of a known MISFET, respectively.

25 **DESCRIPTION OF THE PREFERRED EMBODIMENTS**

(First Embodiment)

Hereafter, a semiconductor device according to a first embodiment of the present invention will be described with reference to the accompanying drawings. FIG. 1 is a cross-sectional view illustrating a structure of a semiconductor device (more specifically, a single sidewall type MISFET) according to the first embodiment. In this embodiment, description will be made using an n-type MISFET as an example. However, even when the present invention is applied to a p-type MISFET, the same effects as those of this embodiment can be achieved.

As shown in FIG. 1, a gate electrode 5 is formed on an active region of a p-type well 2 surrounded by a STI 3. The p-type well 2 is formed in a substrate 1 made of, for example, silicon. The gate electrode 5 is formed on the active region with a high dielectric constant gate insulating film 4A interposed therebetween. An insulating sidewall 7 is formed on each side surface of the gate electrode 5. An n-type extension region 10 is formed in part of the p-type well 2 located under the sidewall 7. Furthermore, a p-type pocket region 11 is formed in part of the p-type well 2 located under the n-type extension region 10. N-type source/drain regions 12 are formed so that each of the source/drain regions 12 is provided in part of the p-type well 2 located in the external side to the n-type extension region 10 and the p-type pocket region 11 when viewed from the gate electrode 5.

It is a first feature of this embodiment that the high dielectric constant gate insulating film 4A is kept remaining not only under the gate electrode 5 but also under the sidewall 7. That is, the high dielectric gate insulating film 4A is continuously formed so as to extend from under the gate electrode 5 to under the sidewall 7.

It is a second feature of this embodiment that the thickness of the part of the high dielectric constant gate insulating film 4A located under the sidewall 7 is smaller than a

thickness of the part of the high dielectric constant film 4A located under the gate electrode 5. That is, the gate insulating film 4A is formed so as to have a convex shape.

According to this embodiment, each side end portion of the high dielectric constant gate insulating film 4A is not in contact with the sidewall 7 and continuity of the high dielectric constant gate insulating film 4A at an end portion of the gate electrode 5 is maintained. Accordingly, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film 4A at the end portion of the gate electrode 5 can be suppressed, so that deterioration of device characteristics of the MISFET and reduction in the reliability of the gate insulating film can be prevented.

According to this embodiment, the existence of the high dielectric constant gate insulating film 4A under the sidewall 7 makes capacitive coupling between the gate electrode 5 and the n-type extension region 10 stronger in the vicinity of the end portion of the gate electrode 5. As a result, a high overlapping effect between a gate and a drain can be achieved (see T. Hori, IEDM Tech. Dig., 1989, p. 777). Therefore, device characteristics and hot carrier reliability can be improved at the same time.

Meanwhile, in this embodiment, because of the existence of the high dielectric constant gate insulating film 4A under the sidewall 7, there might be cases where a capacitance particularly between the gate electrode 5 and each of the n-type source/drain regions 12 is increased and, accordingly, a circuit speed is reduced. However, as described above, in this embodiment, the high dielectric constant gate insulating film 4A is formed so as to have a smaller thickness in the part located under the sidewall 7 than a thickness of the part located under the gate electrode 5. Therefore, increase in a capacitance between the gate and the drain and adverse effect on the circuit speed can be suppressed.

As has been described, according to this embodiment, device/circuit characteristics of an MISFET and the reliability of a gate insulating film, which are conventionally in the

trade-off relationship, can be largely improved at the same time.

(Modified Example of First Embodiment)

Hereafter, a semiconductor device according to a modified example of the first
5 embodiment of the present invention will be described with reference to the accompanying
drawings. FIG. 6 is a cross-sectional view illustrating a structure of a semiconductor
device (more specifically, a single sidewall n-type MISFET) according to the modified
example of the first embodiment.

As shown in FIG. 6, this modified example is different from the first embodiment
10 in that part of a high dielectric constant gate insulating film 4A located under each side end
portion of a sidewall 7, i.e., a side portion of the high dielectric constant gate insulating
film 4A is removed in a notch shape, so that a notch 20 is provided.

According to this modified example, adverse effects on circuit speed due to
increase in a capacitance between a gate electrode 5 and each of n-type source/drain
15 regions 12 can be further suppressed.

(Second Embodiment)

Hereafter, a semiconductor device according to a second embodiment of the present
invention will be described with reference to the accompanying drawings. In contrast with
20 the first embodiment in which a single sidewall type MISFET is described, a double
sidewall type MISFET (see H. Sayama et al., IEDM Tech. Dig., 2000, p. 239) in which an
overlapping amount between a gate electrode and an extension region can be optimized in
a simple manner will be described in the second embodiment. In this embodiment,
description will be made using an n-type MISFET as an example. However, even when
25 the present invention is applied to a p-type MISFET, the same effects as those of this

embodiment can be achieved.

FIG. 2 is a cross-sectional view illustrating a structure of a semiconductor device according to the second embodiment. As shown in FIG. 2, a gate electrode 5 is formed on an active region of a p-type well 2 surrounded by a STI 3. The p-type well 2 is formed in a substrate 1 made of, for example, silicon. The gate electrode 5 is formed on the active region with a high dielectric constant gate insulating film 4B interposed therebetween. An insulating sidewall 7 is formed on each side surface of the gate electrode 5 with an offset sidewall 6 interposed therebetween. An n-type extension region 10 is formed in each of parts of the p-type well 2 located under the offset sidewall 6 and the sidewall 7. Furthermore, a p-type pocket region 11 is formed in part of the p-type well 2 located under the n-type extension region 10. N-type source/drain regions 12 are formed so that each of the source/drain regions is provided in part of the p-type well 2 located in the external side to the n-type extension region 10 and the p-type pocket region 11 when viewed from the gate electrode 5.

It is a first feature of this embodiment that the high dielectric constant gate insulating film 4B is kept remaining not only under the gate electrode 5 but also under the offset sidewall 6. That is, the high dielectric constant gate insulating film 4B is continuously formed so as to extend from under the gate electrode 5 to under the offset sidewall 6.

It is a second feature of this embodiment that the thickness of the part of the high dielectric constant gate insulating film 4B located under the offset sidewall 6 is smaller than a thickness of the part of the high dielectric constant film 4B located under the gate electrode 5. That is, the gate insulating film 4B is formed so as to have a convex shape.

According to this embodiment, each side end portion of the high dielectric constant gate insulating film 4B is not in contact with the offset sidewall 6 and continuity of the

high dielectric constant gate insulating film **4B** at an end portion of the gate electrode **5** is maintained. Accordingly, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film **4B** at the end portion of the gate electrode **5** can be suppressed, so that deterioration of device characteristics of the MISFET and
5 reduction in the reliability of the gate insulating film can be prevented.

According to this embodiment, the existence of the high dielectric constant gate insulating film **4B** under the offset sidewall **6** makes capacitive coupling between the gate electrode **5** and the n-type extension region **10** stronger in the vicinity of the end portion of the gate electrode **5**. As a result, a high overlapping effect between a gate and a drain can
10 be achieved (see T. Hori, IEDM Tech. Dig., 1989, p. 777). Therefore, device characteristics and hot carrier reliability can be improved at the same time.

Moreover, according to this embodiment, the high dielectric constant gate insulating film **4B** does not exist under the sidewall **7**. Thus, increase in a capacitance between the gate electrode **5** and each of the n-type source/drain regions **12** can be further
15 suppressed so that a small capacitance can be maintained. Accordingly, increase in a parasitic capacitance and adverse effects on circuit speed due to the increase can be suppressed at a minimum level.

As has been described, according to this embodiment, device/circuit characteristics of an MISFET and the reliability of a gate insulating film, which are conventionally in the
20 trade-off relationship, can be largely improved at the same time.

(First Modified Example of Second Embodiment)

Hereafter, a semiconductor device according to a modified example of the second embodiment of the present invention will be described with reference to the accompanying
25 drawings. FIG. 7 is a cross-sectional view illustrating a structure of the semiconductor

device (more specifically, a double sidewall type MISFET) according to the first modified example of the second embodiment.

As shown in FIG. 7, this modified example is different from the second embodiment is that part of a high dielectric constant gate insulating film **4B** located under
5 each side end portion of the offset sidewall **6**, i.e., a side portion of the high dielectric constant gate insulating film **4B** is removed in a notch shape, so that a notch **20** is provided.

According to this modified example, adverse effects on circuit speed due to increase in a capacitance between a gate electrode **5** and each of n-type source/drain
10 regions **12** can be further suppressed.

(Second Modified Example of Second Embodiment)

Hereafter, a semiconductor device according to a second modified example of the second embodiment of the present invention will be described with reference to the
15 accompanying drawings. FIG. 3 is a cross-sectional view illustrating a structure of the semiconductor device (more specifically, a double sidewall type MISFET) according to the second modified example of the second embodiment.

This embodiment is different from the second embodiment in that a high dielectric constant gate insulating film **4C** is kept remaining not only under the gate electrode **5** and
20 the offset sidewall **6** but also under the sidewall **7**. That is, the high dielectric constant gate insulating film **4C** is continuously formed so as to extend from under the gate electrode **5** to under the sidewall **7**.

In this modified example, the thickness of part of the high dielectric constant gate insulating film **4C** located under the sidewall **7** is the same as the thickness of part of the
25 high dielectric constant gate insulating film **4C** located under the offset sidewall **6**. That is,

the high dielectric constant gate insulating film 4C is formed so as to have a convex shape.

According to this modified embodiment, the high dielectric constant gate insulating film 4C is continuously formed so as to extend from under the gate electrode 5 to under the sidewall 7. Thus, even when the offset sidewall 6 has a very small width (thickness), each side end portion of the high dielectric constant gate insulating film 4C is not in contact with the sidewall 7 and continuity of the high dielectric constant gate insulating film 4C at an end portion of the gate electrode 5 is maintained. Accordingly, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film 4C at the end portion of the gate electrode 5 can be suppressed, so that deterioration of device characteristics of the MISFET and reduction in the reliability of the gate insulating film can be prevented.

In this modified example, as in the first embodiment, because of the existence of the high dielectric constant gate insulating film 4C under sidewall 7, there might be cases where a capacitance between the gate electrode 5 and each of the n-type source/drain regions 12 is increased. However, as has been described, in this modified example, the high dielectric constant gate insulating film 4C is formed so as to have a smaller thickness in the part located under the sidewall 7 than a thickness of the part located under the gate electrode 5. Therefore, increase in a parasitic capacitance and adverse effects on circuit speed due to the increase can be suppressed.

20

(Third Modified Example of Second Embodiment)

Hereafter, a semiconductor device according to a third modified example of the second embodiment of the present invention will be described with reference to the accompanying drawings. FIG. 4 is a cross-sectional view illustrating a structure of a semiconductor device (more specifically, a double sidewall type MISFET) according to the

25

third modified example of the second embodiment.

A first difference between this modified example and the second embodiment is that in this modified example, a high dielectric constant gate insulating film **4D** is kept remaining not only under the gate electrode **5** and the offset sidewall **6** but also under the
5 sidewall **7**. That is, the high dielectric constant gate insulating film **4D** is continuously formed so as to extend from under the gate electrode **5** to under the sidewall **7**.

A second difference between this modified example and the second embodiment is that in this modified example, the thickness of part of the high dielectric constant gate insulating film **4D** located under the offset sidewall **6** is the same as the thickness of part of
10 the high dielectric constant gate insulating film **4D** located under the gate electrode **5**. The thickness of part of the high dielectric constant gate insulating film **4D** located under the sidewall **7** is smaller than the thickness of the part of the high dielectric constant gate insulating film **4D** located under the gate electrode **5**. That is, the high dielectric constant gate insulating film **4D** is formed so as to have a convex shape.

15 According to this modified example, the high dielectric constant gate insulating film **4D** is continuously formed so as to extend from under the gate electrode **5** to under the sidewall **7**. Thus, even when the offset sidewall **6** has a very small width (thickness), each side end portion of the high dielectric constant gate insulating film **4D** is not in contact with the sidewall **7** and continuity of the high dielectric constant gate insulating film **4D** at
20 an end portion of the gate electrode **5** is maintained. Accordingly, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film **4D** at the end portion of the gate electrode **5** can be suppressed, so that deterioration of device characteristics of the MISFET and reduction in the reliability of the gate insulating film can be prevented.

25 In this modified example, as in the first embodiment, because of the existence of

the high dielectric constant gate insulating film **4D** under sidewall **7**, there might be cases where a capacitance between the gate electrode **5** and each of the n-type source/drain regions **12** is increased. However, as has been described, in this modified example, the high dielectric constant gate insulating film **4D** is formed so as to have a smaller thickness in the part located under the sidewall **7** than a thickness of the part located under the gate electrode **5**. Therefore, increase in a parasitic capacitance and adverse effects on circuit speed due to the increase can be suppressed.

(Third Embodiment)

Hereafter, a semiconductor device according to a third embodiment of the present invention will be described with reference to the accompanying drawings. In contrast with the first embodiment in which a single sidewall type MISFET is described, a double sidewall type MISFET (see H. Sayama et al., IEDM Tech. Dig., 2000, p. 239) in which an overlapping amount between a gate electrode and an extension region can be optimized in a simple manner will be described in the third embodiment. In this embodiment, description will be made using an n-type MISFET as an example. However, even when the present invention is applied to a p-type MISFET, the same effects as those of this embodiment can be achieved.

FIG. **5** is a cross-sectional view illustrating a structure of a semiconductor device according to the third embodiment. As shown in FIG. **5**, a gate electrode **5** is formed on an active region of a p-type well **2** surrounded by a STI **3**. The p-type well **2** is formed in a substrate **1** made of, for example, silicon. The gate electrode **5** is formed on the active region with a high dielectric constant gate insulating film **4E** interposed therebetween. An insulating sidewall **7** is formed on each side surface of the gate electrode **5** with an offset sidewall **6** interposed therebetween. An n-type extension region **10** is formed in each of

parts of the p-type well **2** located under the offset sidewall **6** and the sidewall **7**. Furthermore, a p-type pocket region **11** is formed in part of the p-type well **2** located under the n-type extension region **10**. N-type source/drain regions **12** are formed so that each of the source/drain is provided in part of the p-type well **2** located in the external side to the n-type extension region **10** and the p-type pocket region **11** when viewed from the gate electrode **5**.

It is a first feature that the high dielectric constant gate insulating film **4E** is kept remaining not only under the gate electrode **5** and but also under each of the offset sidewall **6** and the sidewall **7**. That is, the high dielectric constant gate insulating film **4E** is continuously formed so as to extend from under the gate electrode **5** to under the sidewall **7**.

It is a second feature of this embodiment that the thickness of the part of the high dielectric constant gate insulating film **4E** located under the offset sidewall **6** is smaller than a thickness of the part of the high dielectric constant film **4E** located under the gate electrode **5** and the thickness of the high dielectric constant gate insulating film **4E** located under the sidewall **7** is smaller than the thickness of the part of the high dielectric constant film **4E** located under the offset sidewall **6**. That is, the gate insulating film **4E** is formed so as to have a double convex shape.

According to this embodiment, the high dielectric constant gate insulating film **4E** is continuously formed so as to extend from under the gate electrode **5** to under the sidewall **7**. Thus, even when the offset sidewall **6** has a very small width (thickness), each side end portion of the high dielectric constant gate insulating film **4E** is not in contact with the sidewall **7** and continuity of the high dielectric constant gate insulating film **4E** at an end portion of the gate electrode **5** is maintained. Accordingly, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating

film 4E at the end portion of the gate electrode 5 can be suppressed, so that deterioration of device characteristics of the MISFET and reduction in the reliability of the gate insulating film can be prevented.

According to this embodiment, the existence of the high dielectric constant gate insulating film 4E under the offset sidewall 6 makes capacitive coupling between the gate electrode 5 and the n-type extension region 10 stronger at the vicinity of the end portion of the gate electrode 5. As a result, a high overlapping effect between a gate and a drain can be achieved (see T. Hori, IEDM Tech. Dig., 1989, p. 777). Therefore, device characteristics and hot carrier reliability can be improved at the same time.

As in the first embodiment, in this embodiment, because of the existence of the high dielectric constant gate insulating film 4E under sidewall 7, there might be cases where a capacitance between the gate electrode 5 and each of the n-type source/drain regions 12 is increased and, accordingly, a circuit speed is reduced. However, as has been described, in this embodiment, the high dielectric constant gate insulating film 4E is formed so that the thickness of the high dielectric constant gate insulating film 4E is reduced in the part located under the offset sidewall 6 and then is further reduced in the part located under the sidewall 7. Therefore, increase in a parasitic capacitance and adverse effects on circuit speed due to the increase can be suppressed so that the parasitic capacitance is a very low level.

As has been described, according to this embodiment, device/circuit characteristics of an MISFET and the reliability of a gate insulating film, which are conventionally in the trade-off relationship, can be largely improved at the same time.

(Modified Example of Third Embodiment)

Hereafter, a semiconductor device according to a modified example of a third

embodiment of the present invention will be described with reference to the accompanying drawings. FIG. 8 is a cross-sectional view illustrating a structure of a semiconductor device (more specifically, a double sidewall type MISFET) according to the modified example of the third embodiment.

5 As shown in FIG. 8, this modified example is different from the first embodiment in that part of a high dielectric constant gate insulating film 4E located under each side end portion of a sidewall 7, i.e., a side portion of the high dielectric constant gate insulating film 4E is removed in a notch shape, so that a notch 20 is provided.

According to this modified example, adverse effects on circuit speed due to
10 increase in a capacitance between a gate electrode 5 and each of n-type source/drain regions 12 can be further suppressed.

(Fourth Embodiment)

Hereafter, a semiconductor device according to a fourth embodiment of the present
15 invention will be described with reference to the accompanying drawings. FIG. 9 is a cross-sectional view illustrating a structure of a semiconductor device (more specifically, a single sidewall type MISFET) according to the fourth embodiment of the present invention. In this embodiment description will be made using an n-type MISFET as an example. However, even when the present invention is applied to a p-type MISFET, the
20 same effects as those of this embodiment can be achieved.

As shown in FIG. 9, this embodiment is different from the first embodiment in that, for example, a silicon oxide film, a silicon oxynitride film or the like is provided as a buffer insulating film 25 between a substrate 1 and a high dielectric constant gate insulating film 4A.

25 According to this embodiment, in addition to the effects of the first embodiment, an

interface between a substrate and a gate insulating film can be advantageously kept in a normal state. Specifically, by forming the high dielectric constant gate insulating film **4A** on the substrate **1** with the buffer insulating film **25** interposed therebetween, deterioration of an interface between a substrate and a gate insulating film can be suppressed, compared to the case where the high dielectric constant gate insulating film **4A** is formed directly on the substrate **1**.

In this embodiment, the buffer insulating film **25** is provided between the high dielectric constant gate insulating film **4A** of the first embodiment and the substrate **1**. However, instead of this structure, even if the buffer insulating film **25** is provided between the substrate **1** and the high dielectric constant gate insulating film **4B** of the second embodiment, the high dielectric constant gate insulating film **4C** of the second modified example of the second embodiment, the high dielectric constant gate insulating film **4D** of the third modified example of the second embodiment or the high dielectric constant gate insulating film **4E** of the third embodiment, the same effects as those of this embodiment can be achieved. Moreover, instead of providing the buffer insulating film **25** between the substrate **1** and the high dielectric constant gate insulating film **4A**, **4B**, **4C**, **4D** or **4E**, a buffer insulating film may be provided between the gate electrode **5** and the high dielectric constant gate insulating film **4A**, **4B**, **4C**, **4D** or **4E**. With such a structure, compared to the case where the gate electrode **5** is directly formed on the high dielectric constant gate insulating film **4A**, **4B**, **4C**, **4D** or **4E**, deterioration of an interface between a gate electrode and a gate insulating film can be prevented. As another alternative, a buffer insulating film may be formed between the gate electrode **5** and the high dielectric constant gate insulating film **4A**, **4B**, **4C**, **4D** or **4E** as well as forming the buffer insulating film **25** between the substrate **1** and the high dielectric constant gate insulating film **4A**, **4B**, **4C**, **4D** or **4E**. With such a structure, deterioration of each of the substrate-gate insulating film

interface and the gate insulating film-gate electrode interface can be prevented at the same time.

(Modified Example of Fourth Embodiment)

Hereafter, a semiconductor device according to a modified example of the fourth
5 embodiment of the present invention will be described with reference to the accompanying drawings. FIG. 10 is a cross-sectional view illustrating a structure of a semiconductor device (more specifically, a single sidewall type MISFET) according to the modified example of the fourth embodiment.

As shown in FIG. 10, this modified example is different from the fourth
10 embodiment in that part of a laminated insulating film of a high dielectric constant gate insulating film 4A and a buffer insulating film 25 located under a side end portion of each sidewall 7, i.e., a side end portion of the laminated insulating film is removed in a notch shape, so that a notch 20 is provided.

According to this modified example, adverse effects on circuit speed due to
15 increase in a capacitance between a gate electrode 5 and each of n-type source/drain regions 12 can be further suppressed.

In this modified example, the notch 20 is provided in the side end portion of the laminated insulating film of the high dielectric constant gate insulating film 4A and the buffer insulating film 25 of the first embodiment. However, instead of this structure, even
20 if a notch is provided in a side end portion of a laminated insulating film of the buffer insulating film 25 and the high dielectric constant gate insulating film 4B of the second embodiment, the high dielectric constant gate insulating film 4C of the second modified example of the second embodiment, the high dielectric constant gate insulating film 4D of the third modified example of the second embodiment or the high dielectric constant gate
25 insulating film 4E of the third embodiment, the same effects of the modified example can

be achieved. In such cases, a buffer insulating film may be provided between the gate electrode 5 and the high dielectric constant gate insulating film 4A, 4B, 4C, 4D or 4D as well as forming the buffer insulating film 25 between the substrate 1 and the high dielectric constant gate insulating film 4A, 4B, 4C, 4D or 4D.

5

(Fifth Embodiment)

Hereafter, a method for fabricating a semiconductor device according to a fifth embodiment of the present invention will be described with reference to the accompanying drawings. In this embodiment, description will be made using a method for fabricating an
10 n-type MISFET as an example. FIGS. 11A through 11F are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to the fifth embodiment.

First, as shown in FIG. 11A, a STI 3 which is to be an isolation region is selectively formed on a substrate 1 of, for example, silicon and then, for example, B (boron) is ion
15 implanted into the substrate 1 at an implantation energy of 300 keV and a dose of $1 \times 10^{13} \text{ cm}^{-2}$. Thus, a p-type well 2 which is to be an active region is formed. Subsequently, ion implantation (of B at an implantation energy of 150 keV and a dose of $1 \times 10^{13} \text{ cm}^{-2}$) for punch-through stopper formation and ion implantation (of B at an implantation energy of 20 keV and a dose of $5 \times 10^{12} \text{ cm}^{-2}$) for channel formation are
20 performed.

Next, as shown in FIG. 11B, as a buffer insulating film, for example, a silicon oxide film (not shown) is formed on the active region of the p-type well 2 surrounded by the STI 3 so as to have a thickness of about 0.5 nm and then, as a high dielectric constant film 4, for example, a HfSiON film is deposited thereon to a thickness of about 4 nm (i.e.,
25 about 1 nm in terms of an equivalent oxide thickness).

Next, as shown in FIG. 11C, for example, a gate electrode material film 5A is formed on the high dielectric constant gate insulating film 4 so as to have a thickness of about 100 nm.

Next, a resist pattern (not shown) is formed on the gate electrode material film 5A so as to cover a gate electrode formation region, and then the gate electrode material film 5A is etched using the resist pattern as a mask, thereby forming, as shown in FIG. 11D, a gate electrode 5. Thereafter, part of the high dielectric constant gate insulating film 4 located in the external side to the gate electrode 5 is removed by a thickness of about 2 nm by selective etching. Thus, a thickness of part of the high dielectric constant gate insulating film 4 located in the external side to the gate electrode 5 can be reduced so that a remaining thickness of the part of the high dielectric constant gate insulating film 4 becomes about 2 nm. Subsequently, using the gate electrode 5 as a mask, for example, As (arsenic) is ion implanted into the substrate 1 at an implantation energy of 2 keV and a dose of $1 \times 10^{15} \text{ cm}^{-2}$, thereby forming an n-type extension region 10. Thereafter, using the gate electrode 5 as a mask, for example, B is ion implanted into the substrate 1 at an implantation energy of 10 keV and a dose of $3 \times 10^{13} \text{ cm}^{-2}$, thereby forming a p-type pocket region 11. In this case, the n-type extension region 10 may be formed after forming the p-type pocket region 11.

Next, an insulating film is deposited over the substrate 1 to a thickness of about 50 nm, and then the insulating film is etched back to form, as shown in FIG. 11E, an insulating sidewall 7 on each side surface of the gate electrode 5.

Next, using the gate electrode 5 and the sidewall 7 as a mask, for example, As is ion implanted into the substrate 1 at an implantation energy of 10 keV and a dose of $5 \times 10^{15} \text{ cm}^{-2}$, and then, for example, spike RTA (rapid thermal annealing) is performed at a temperature of about 1050 °C, thereby activating the implanted impurity. Thus, as

shown in FIG. 11F, n-type source/drain regions 12 are formed.

According to the above-described fabrication method of this embodiment, the MISFET structure (see FIG. 1) of the first embodiment can be realized in a relatively simple manner.

5 Meanwhile, the high dielectric constant gate insulating film 4 contains heavy metal and thus R_p (projection range) of implanted ions passing through the high dielectric constant gate insulating film 4 tends to be small. Therefore, in the process step of FIG. 11D, if without reducing the thickness of the high dielectric constant gate insulating film 4, ion implantation is performed to the substrate 1 covered with the high dielectric constant
10 gate insulating film 4 in the external side to the gate electrode 5 to form the n-type extension region 10 or the p-type pocket region 11, an acceleration energy has to be increased. However, in this embodiment, the part of the high dielectric constant gate insulating film 4 located in the external side to the gate electrode 5 has a reduced thickness, so that increase in acceleration energy can be suppressed. Accordingly, a shallow junction
15 can be formed in the n-type extension region 10 in a simple manner and thus device characteristics can be improved in a simple manner.

In this embodiment, after the sidewall 7 has been formed, for example, part of the high dielectric constant gate insulating film 4 located in the external side to the sidewall 7 may be removed by wet etching using hydrofluoric acid or the like or selective dry etching.
20 In such a case, when wet etching is used, part of the high dielectric constant gate insulating film 4 located under each side end portion of the sidewall 7, i.e., a side end portion of the high dielectric constant gate insulating film 4 may be removed in a notch shape, so that a notch is formed. Thus, the MISFET structure (see FIG. 6) of the modified example of the first embodiment can be realized in a simple manner.

25 In this embodiment, a target thickness for reduction in the thickness of the part of

the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is not particularly limited. However, for example, when an HfSiON film is used as the high dielectric constant gate insulating film **4**, to suppress increase in a capacitance between a gate and a grain, the thickness of part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is preferably reduced to about 2 nm or less (so that a surface of the substrate **1** is not exposed).

(Sixth Embodiment)

Hereafter, a method for fabricating a semiconductor device according to a sixth embodiment of the present invention will be described with reference to the accompanying drawings. In this embodiment, description will be made using a method for fabricating an n-type MISFET as an example. FIGS. **12A** through **12G** are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to the sixth embodiment.

First, as shown in FIG. **12A**, a STI **3** which is to be an isolation region is selectively formed on a substrate **1** of, for example, silicon and then, for example, B is ion implanted into the substrate **1** at an implantation energy of 300 keV and a dose of $1 \times 10^{13} \text{ cm}^{-2}$. Thus, a p-type well **2** which is to be an active region is formed. Subsequently, ion implantation (of B at an implantation energy of 150 keV and a dose of $1 \times 10^{13} \text{ cm}^{-2}$) for punch-through stopper formation and ion implantation (of B at an implantation energy of 20 keV and a dose of $5 \times 10^{12} \text{ cm}^{-2}$) for channel formation are performed.

Next, as shown in FIG. **12B**, as a buffer insulating film, for example, a silicon oxide film (not shown) is formed on the active region of the p-type well **2** surrounded by the STI **3** so as to have a thickness of about 0.5 nm and then, as a high dielectric constant film **4**, for example, a HfSiON film is deposited thereon to a thickness of about 4 nm (i.e.,

about 1 nm in terms of an equivalent oxide thickness).

Next, as shown in FIG. 12C, for example, a gate electrode material film 5A is formed on the high dielectric constant gate insulating film 4 so as to have a thickness of about 100 nm.

5 Next, a resist pattern (not shown) is formed on the gate electrode material film 5A so as to cover a gate electrode formation region, and then the gate electrode material film 5A is etched using the resist pattern as a mask, thereby forming, as shown in FIG. 12D, a gate electrode 5. Thereafter, part of the high dielectric constant gate insulating film 4 located in the external side to the gate electrode 5 is removed by a thickness of about 2 nm
10 by selective etching. Thus, a thickness of the part of the high dielectric constant gate insulating film 4 located in the external side to the gate electrode 5 can be reduced so that a remaining thickness of the part of the high dielectric constant gate insulating film 4 becomes about 2 nm.

Next, an insulating film is deposited over the substrate 1 to a thickness of about
15 10 nm, and then the insulating film is etched back to form, as shown in FIG. 12E, an insulating offset sidewall 6 on each side surface of the gate electrode 5. Thereafter, part of the high dielectric constant gate insulating film 4 located in the external side to the offset sidewall 6 is removed by wet etching using, for example, hydrofluoric acid or selective dry etching. Subsequently, using the gate electrode 5 and the offset sidewall 6 as a mask, for
20 example, As is ion implanted into the substrate 1 at an implantation energy of 2 keV and a dose of $1 \times 10^{15} \text{ cm}^{-2}$, thereby forming an n-type extension region 10. Thereafter, using the gate electrode 5 and the offset sidewall 6 as a mask, for example, B is ion implanted into the substrate 1 at an implantation energy of 10 keV and a dose of $3 \times 10^{13} \text{ cm}^{-2}$, thereby forming a p-type pocket region 11.

25 Next, an insulating film is deposited over the substrate 1 to a thickness of about

50 nm, and then the insulating film is etched back to form, as shown in FIG. 12F, an insulating sidewall 7 on each side surface of the gate electrode 5 with the offset sidewall 6 interposed therebetween.

Next, using the gate electrode 5, the offset sidewall 6 and the sidewall 7 as a mask,
5 for example, As is ion implanted into the substrate 1 at an implantation energy of 10 keV and a dose of $5 \times 10^{15} \text{ cm}^{-2}$, and then, for example, spike RTA (rapid thermal annealing) is performed at a temperature of about 1050 °C, thereby activating the implanted impurity. Thus, as shown in FIG. 12G, n-type source/drain regions 12 are formed.

According to the above-described fabrication method of this embodiment, the
10 MISFET structure (see FIG. 2) of the second embodiment can be realized in a relatively simple manner.

In this embodiment, after the offset sidewall 6 has been formed, part of the high dielectric constant gate insulating film 4 located in the external side to the offset sidewall 6 is removed, for example, by wet etching using hydrofluoric acid or the like. When this
15 wet etching is performed, part of the high dielectric constant gate insulating film 4 located under each side end portion of the offset sidewall 6, i.e., a side end portion of the high dielectric constant gate insulating film 4 may be removed in a notch shape, so that a notch is formed. Thus, the MISFET structure (see FIG. 7) of the first modified example of the second embodiment can be realized in a simple manner.

20 In this embodiment, a target thickness for reduction in the thickness of the part of the high dielectric constant gate insulating film 4 located in the external side to the gate electrode 5 is not particularly limited. However, for example, when an HfSiON film is used as the high dielectric constant gate insulating film 4, to suppress increase in a capacitance between a gate and a grain, the thickness of part of the high dielectric constant
25 gate insulating film 4 located in the external side to the gate electrode 5 is preferably

reduced to about 2 nm or less (so that a surface of the substrate 1 is not exposed).

In this embodiment, after the offset sidewall 6 has been formed, part of the high dielectric constant gate insulating film 4 located in the external side to the offset sidewall 6 is removed, and then ion implantation for forming the n-type extension region 10 and the p-type pocket region 11 is performed. However, instead of performing these process steps, ion implantation for forming the n-type extension region 10 and the p-type pocket region 11 may be performed after the offset sidewall 6 is formed and with part of the high dielectric constant gate insulating film 4 having a reduced thickness remaining in the external side to the offset sidewall 6. Even in this manner, according to this embodiment, the part of the high dielectric constant gate insulating film 4 located in the external side to the offset sidewall 6 has a reduced thickness, so that increase in acceleration energy can be suppressed. Accordingly, a shallow junction can be formed in the n-type extension region 10 in a simple manner and thus device characteristics can be improved in a simple manner. In this case, ion implantation for forming an extension region and a pocket region of an MISFET having a different channel type or another power supply system and being provided on the same substrate may be performed after ion implantation for forming the n-type extension region 10 and the p-type pocket region 11 and then removal of the part of the high dielectric constant gate insulating film 4 located in the external side to the offset sidewall 6.

(Seventh Embodiment)

Hereafter, a method for fabricating a semiconductor device according to a seventh embodiment of the present invention will be described with reference to the accompanying drawings. FIGS. 13A through 13G are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to the seventh embodiment.

First, as shown in FIG. 13A, a STI 3 which is to be an isolation region is selectively formed on a substrate 1 of, for example, silicon and then, for example, B is ion implanted into the substrate 1 at an implantation energy of 300 keV and a dose of $1 \times 10^{13} \text{ cm}^{-2}$. Thus, a p-type well 2 which is to be an active region is formed. Subsequently, ion implantation (of B at an implantation energy of 150 keV and a dose of $1 \times 10^{13} \text{ cm}^{-2}$) for punch-through stopper formation and ion implantation (of B at an implantation energy of 20 keV and a dose of $5 \times 10^{12} \text{ cm}^{-2}$) for channel formation are performed.

Next, as shown in FIG. 13B, as a buffer insulating film, for example, a silicon oxide film (not shown) is formed on the active region of the p-type well 2 surrounded by the STI 3 so as to have a thickness of about 0.5 nm and then, as a high dielectric constant film 4, for example, a HfSiON film is deposited thereon to a thickness of about 4 nm (i.e., about 1 nm in terms of an equivalent oxide thickness).

Next, as shown in FIG. 13C, for example, a gate electrode material film 5A is formed on the high dielectric constant gate insulating film 4 so as to have a thickness of about 100 nm.

Next, a resist pattern (not shown) is formed on the gate electrode material film 5A so as to cover a gate electrode formation region, and then the gate electrode material film 5A is etched using the resist pattern as a mask, thereby forming, as shown in FIG. 13D, a gate electrode 5. Thereafter, part of the high dielectric constant gate insulating film 4 located in the external side to the gate electrode 5 is removed by a thickness of about 2 nm by selective etching. Thus, a thickness of part of the high dielectric constant gate insulating film 4 located in the external side to the gate electrode 5 can be reduced so that a remaining thickness of the part of the high dielectric constant gate insulating film 4 becomes about 2 nm.

Next, an insulating film is deposited over the substrate **1** to a thickness of about 5 nm, and then the insulating film is etched back to form, as shown in FIG. 13E, an insulating offset sidewall **6** on each side surface of the gate electrode **5**. Thereafter, part of the high dielectric constant gate insulating film **4** which is not covered by the gate electrode **5** and the offset sidewall **6** is further removed by about 1 nm. Thus, the thickness of part of the high dielectric gate insulating film **4** located in the external side to the offset sidewall **6** can be reduced to a thickness of about 1 nm. Then, using the gate electrode **5** and the offset sidewall **6** as a mask, for example, As is ion implanted into the substrate **1** at an implantation energy of 2 keV and a dose of $1 \times 10^{15} \text{ cm}^{-2}$, thereby forming an extension region **10**. Thereafter, using the gate electrode **5** and the offset sidewall **6** as a mask, for example, B is ion implanted into the substrate **1** at an implantation energy of 10 keV and a dose of $3 \times 10^{13} \text{ cm}^{-2}$, thereby forming a p-type pocket region **11**.

Next, an insulating film is deposited over the substrate **1** to a thickness of about 50 nm, and then the insulating film is etched back to form, as shown in FIG. 13F, an insulating sidewall **7** on each side surface of the gate electrode **5** with the offset sidewall **6** interposed therebetween.

Next, using the gate electrode **5**, the offset sidewall **6** and the sidewall **7** as a mask, for example, As is ion implanted into the substrate **1** at an implantation energy of 10 keV and a dose of $5 \times 10^{15} \text{ cm}^{-2}$, and then, for example, spike RTA (rapid thermal annealing) is performed at a temperature of about 1050 °C, thereby activating the implanted impurity. Thus, as shown in FIG. 13G, n-type source/drain regions **12** are formed.

According to the above-described fabrication method of this embodiment, the MISFET structure (see FIG. 5) of the third embodiment can be realized in a relatively simple manner.

In this embodiment, the high dielectric constant gate insulating film **4E** is formed

so that the thickness of the high dielectric constant gate insulating film **4E** is reduced in the part located under the offset sidewall **6** and then is further reduced in the part located in the external side to the offset sidewall **6**. Therefore, even when ion implantation for forming the n-type extension region **10** is performed using the gate electrode **5** and the offset
5 sidewall **6** as a mask, increase in acceleration energy can be suppressed at a minimum level. Accordingly, a shallow junction can be formed at an even shallower depth in the n-type extension region **10** in a simple manner and thus device characteristics can be improved in a simple manner.

In this embodiment, after the sidewall **7** has been formed, the part of the high
10 dielectric constant gate insulating film **4** located in the external side to the sidewall **7** may be removed, for example, by wet etching using hydrofluoric acid or the like or selective dry etching. Moreover, in such a case, part of the high dielectric constant gate insulating film **4** located under each side end portion of the sidewall **7**, i.e., each side end portion of the high dielectric constant gate insulating film **4** may be removed in a notch shape. Thus,
15 the MISFET structure (see FIG. **8B**) of the modified embodiment of the third embodiment can be realized in a simple manner.

In this embodiment, a target thickness for reduction in the thickness of the part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is not particularly limited either under the offset sidewall **6** or under the
20 sidewall **7**. However, for example, when an HfSiON film is used as the high dielectric constant gate insulating film **4**, to suppress increase in a capacitance between a gate and a grain, the thickness of part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is preferably reduced to about 2 nm or less.

25 (Eighth Embodiment)

Hereafter, a method for fabricating a semiconductor device according to an eighth embodiment of the present invention will be described with reference to the accompanying drawings. In this embodiment, description will be made using a method for fabricating an n-type MISFET as an example. FIGS. 14A through 14G and FIGS. 15A through 15D are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to the eighth embodiment.

First, as shown in FIG. 14A, for example, a STI 3 which is to be an isolation region is selectively formed on a substrate 1 of, for example, silicon and then, for example, B is ion implanted into the substrate 1 at an implantation energy of 300 keV and a dose of $1 \times 10^{13} \text{ cm}^{-2}$. Thus, a p-type well 2 which is to be an active region is formed. Subsequently, ion implantation (of B at an implantation energy of 150 keV and a dose of $1 \times 10^{13} \text{ cm}^{-2}$) for punch-through stopper formation and ion implantation (of B at an implantation energy of 20 keV and a dose of $5 \times 10^{12} \text{ cm}^{-2}$) for channel formation are performed.

Next, as shown in FIG. 14B, as a buffer insulating film, for example, a silicon oxide film (not shown) is formed on the active region of the p-type well 2 surrounded by the STI 3 so as to have a thickness of about 0.5 nm and then, as a high dielectric constant film 4, for example, a HfSiON film is deposited thereon to a thickness of about 4 nm (i.e., about 1 nm in terms of an equivalent oxide thickness).

Next, as shown in FIG. 14C, as a gate electrode material film 5A, for example, a polysilicon film is formed on the high dielectric constant gate insulating film 4 so as to have a thickness of about 100 nm, and then as a cover film (protective film) 15, for example, a silicon oxide film is deposited over the gate electrode material film 5A to a thickness of about 10 nm.

Next, a resist pattern (not shown) is formed on the cover film 15 so as to cover a

gate electrode formation region, and then the cover film 15 and the gate electrode material film 5A are etched in this order using the resist pattern as a mask, thereby forming, as shown in FIG. 14D, a gate electrode 5 with its upper surface covered by the cover film 15. Thereafter, part of the high dielectric constant gate insulating film 4 located in the external side to the gate electrode 5 is removed by a thickness of about 2 nm by selective etching. Thus, a thickness of part of the high dielectric constant gate insulating film 4 located in the external side to the gate electrode 5 can be reduced so that a remaining thickness of the part of the high dielectric constant gate insulating film 4 becomes about 2 nm.

Next, an insulating film is deposited over the substrate 1 to a thickness of about 10 nm, and then the insulating film is etched back to form, as shown in FIG. 14E, an insulating offset sidewall 6 on each side surface of the gate electrode 5. Thereafter, part of the high dielectric constant gate insulating film 4 located in the external side to the offset sidewall 6 is removed, for example, by wet etching using hydrofluoric acid or the like or selective dry etching. Subsequently, using the gate electrode 5 and the offset sidewall 6 as a mask, for example, As is ion implanted into the substrate 1 at an implantation energy of 2 keV and a dose of $1 \times 10^{15} \text{ cm}^{-2}$, thereby forming an n-type extension region 10. Thereafter, using the gate electrode 5 and the offset sidewall 6 as a mask, for example, B is ion implanted into the substrate 1 at an implantation energy of 10 keV and a dose of $3 \times 10^{13} \text{ cm}^{-2}$, thereby forming a p-type pocket region 11.

Next, an insulating film (for example, a SiN film) is deposited over the substrate 1 to a thickness of about 50 nm, and then the insulating film is etched back to form, as shown in FIG. 14F, an insulating sidewall 7 on each side surface of the gate electrode 5 with the offset sidewall 6 interposed therebetween.

Next, using the gate electrode 5, the offset sidewall 6 and the sidewall 7 as a mask, for example, As is ion implanted into the substrate 1 at an implantation energy of 10 keV

and a dose of $5 \times 10^{15} \text{ cm}^{-2}$, and then, for example, spike RTA (rapid thermal annealing) is performed at a temperature of about 1050 °C, thereby activating the implanted impurity. Thus, as shown in FIG. 14G, n-type source/drain regions 12 are formed.

Next, a metal film (for example, a Ni film) is deposited over the substrate 1 to a thickness of about 10 nm, and RTA is performed to bring a silicon portion of the substrate 1 and the metal film into reaction. Thus, as shown in FIG. 15A, a silicide layer 13 is formed on the n-type source/drain regions 12. Thereafter, unreacted part of the metal film which remains on the substrate 1 is exfoliated or removed.

Next, as shown in FIG. 15B, an interlayer insulating film 14 is deposited over the substrate 1 as well as the gate electrode 5 to a thickness of about 400 nm.

Next, as shown in FIG. 15C, the interlayer insulating film 14 is polished, for example, by CMP (chemical mechanical polishing) so that a surface of the interlayer insulating film 14 becomes at the same level as the upper surface of the cover film 15, and then the exposed cover film 15 is removed by etching. In this case, respective upper portions of the interlevel insulating film 14 which has undergone through CMP and the offset sidewall 6 are also removed.

Next, a metal film (for example, a Ni film) is deposited over the substrate 1 to a thickness of about 100 nm, and then RTA is performed to bring a silicon portion of the gate electrode 5 and the metal film into reaction. Thus, as shown in FIG. 15D, a fully silicided gate electrode 16 (obtained by siliciding the entire region over the high dielectric constant gate insulating film 4) is formed.

According to the above-described fabrication method of this embodiment, the MISFET structure (see FIG. 2) of the second embodiment using a FUSI (full silicide) structure can be realized in a relatively simple manner.

In this embodiment, when the offset sidewall 6 has been formed and then part of

the high dielectric constant gate insulating film 4 located in the external side to the offset sidewall 6 is removed, for example, by wet etching using hydrofluoric acid or the like, part of the high dielectric constant gate insulating film 4 located under each side end portion of the offset sidewall 6, i.e., each side portion of the high dielectric constant gate insulating
5 film 4 may be removed in a notch shape so that a notch is provided. Thus, the MISFET structure (see FIG. 7) of the first modified example of the second embodiment using a FUSI structure can be realized in a simple manner.

In this embodiment, a target thickness for reduction in the thickness of the part of the high dielectric constant gate insulating film 4 located in the external side to the gate
10 electrode 5 is not particularly limited. However, for example, when an HfSiON film is used as the high dielectric constant gate insulating film 4, to suppress increase in a capacitance between a gate and a grain, the thickness of part of the high dielectric constant gate insulating film 4 located in the external side to the gate electrode 5 is preferably reduced to about 2 nm or less (so that a surface of the substrate 1 is not exposed).

15 In this embodiment, after the offset sidewall 6 has been formed, part of the high dielectric constant gate insulating film 4 located in the external side to the offset sidewall 6 is removed, and then ion implantation for forming the n-type extension region 10 and the p-type pocket region 11 is performed. However, instead of performing these process steps, ion implantation for forming the n-type extension region 10 and the p-type pocket region
20 11 may be performed after the offset sidewall 6 is formed and with part of the high dielectric constant gate insulating film 4 having a reduced thickness remaining in the outer side offset sidewall 6. Even in this manner, according to this embodiment, the part of the high dielectric constant gate insulating film 4 located in the external side to the offset sidewall 6 has a reduced thickness, so that increase in acceleration energy can be
25 suppressed. Accordingly, a shallow junction can be formed in the n-type extension region

10 in a simple manner and thus device characteristics can be improved in a simple manner. In this case, ion implantation for forming an extension region and a pocket region of an MISFET having a different channel type or another power supply system and formed on the same substrate may be performed after ion implantation for forming the n-type
5 extension region 10 and the p-type pocket region 11 and then removal of the part of the high dielectric constant gate insulating film 4 located in the external side to the offset sidewall 6.

In this embodiment, the MISFET structure of the second embodiment using a FUSI structure has been formed. However, instead of forming the MISFET structure of the
10 second embodiment, the MISFET structure of the first embodiment, the modified example of the first embodiment, each of the modified examples of the second embodiment, the third embodiment, the modified example of the third embodiment, the fourth embodiment or the modified example of the fourth embodiment may be formed using a FUSI structure.

In each of the first through eighth embodiments, a single layer structure of a SiN
15 film has been used as an example of the sidewall 7. However, instead of the single layer structure of a SiN film, for example, a double layer structure of a combination of an oxide film (SiO₂ film) and a nitride film (SiN film) (for example, including a SiO₂ layer as an lower layer and a SiN film as an upper layer), a triple layer structure (for example including an SiO₂ film as a lower layer, a SiN film as a middle layer and a SiO₂ film as an
20 upper layer) or the like may be used.

In each of the first through eighth embodiments, instead of the n-type extension region 10, a LDD may be formed.

In each of the fifth through eighth embodiments, instead of the n-type MISFET, a p-type MISFET may be formed.

25 In each of the fifth through eighth embodiments, to prevent deterioration of the

interface of a gate insulating film and a gate electrode, a buffer insulating film may be formed between the gate electrode 5 and the high dielectric constant gate insulating film 4 so as to have a thickness of about 0.2 nm.

In each of the first through eighth embodiments, a shape of each side surface of the high dielectric constant gate insulating film 4 in which the notch 20 is provided in the part located under each side end portion of the sidewall 7 or the offset sidewall 6 is not limited to a semicircular shape shown in FIG. 6, 7, 8 or 10. For example, each side surface of the high dielectric constant gate insulating film 4 may be a perpendicular plane to the substrate surface. That is, a side surface of the high dielectric constant gate insulating film 4 may be located at a predetermined distance from a side end surface of the sidewall 7 or the offset sidewall 6 toward the gate electrode 5.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a high dielectric constant gate insulating film formed on an active region in a substrate;

5 a gate electrode formed on the high dielectric constant gate insulating film; and
an insulating sidewall formed on each side surface of the gate electrode,
wherein the high dielectric constant gate insulating film is continuously formed so
as to extend from under the gate electrode to under the insulating sidewall, and
at least part of the high dielectric constant gate insulating film located under the
10 insulating sidewall has a smaller thickness than a thickness of part of the high dielectric
constant gate insulating film located under the gate electrode.

2. The semiconductor device of claim 1, wherein the insulating sidewall includes a
first insulating sidewall formed on a side surface of the gate electrode and a second
15 insulating sidewall formed on the side surface of the gate electrode with the first insulating
sidewall interposed therebetween,

the high dielectric constant gate insulating film is continuously formed so as to
extend from under the gate electrode to under the first insulating sidewall, and

part of the high dielectric constant gate insulating film located under the first
20 insulating sidewall has a smaller thickness than a thickness of part of the high dielectric
constant gate insulating film located under the gate electrode.

3. The semiconductor device of claim 2, wherein the high dielectric constant gate
insulating film is formed so as not to be located under the second insulating sidewall.

25

4. The semiconductor device of claim 2, wherein the high dielectric constant gate insulating film is continuously formed so as to extend to under the second insulating sidewall, and

part of the high dielectric constant gate insulating film located under the second
5 insulating sidewall has the same thickness as a thickness of part of the high dielectric constant gate insulating film located under the first insulating sidewall.

5. The semiconductor device of claim 2, wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to
10 under the second insulating sidewall, and

part of the high dielectric constant gate insulating film located under the second insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the first insulating sidewall.

15 6. The semiconductor device of claim 1, wherein the insulating sidewall includes a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween,

the high dielectric constant gate insulating film is continuously formed so as to
20 extend from under the gate electrode to under the second insulating sidewall,

part of the high dielectric constant gate insulating film located under the first insulating sidewall has the same thickness as a thickness of part of the high dielectric constant gate insulating film located under the gate electrode, and

part of the high dielectric constant gate insulating film located under the second
25 insulating sidewall has a smaller thickness than a thickness of part of the high dielectric

constant gate insulating film located under the gate electrode.

7. The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film includes a notch at a side end portion.

5

8. The semiconductor device of claim 1, further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film.

9. The semiconductor device of claim 8, wherein the buffer insulating film is a
10 silicon oxide film or a silicon oxynitride film.

10. The semiconductor device of claim 1, wherein the gate electrode is a fully silicided gate electrode of which an entire region has been silicided.

11. A method for fabricating a semiconductor device, the method comprising the
15 steps of:

a) forming a high dielectric constant gate insulating film on an active region of a substrate;

b) forming a gate electrode on the high dielectric constant gate insulating film;

20 c) etching, after the step b), part of the high dielectric constant gate insulating film located in an external side to the gate electrode to reduce a thickness of the part; and

d) forming, after the step c), an insulating sidewall on a side surface of the gate electrode.

25 12. The method of claim 11, further comprising, after the step d), the step of removing part of the high dielectric constant gate insulating film located in an external side

to the insulating sidewall.

13. The method of claim 11, wherein the insulating sidewall includes a first insulating sidewall and a second insulating sidewall, and

5 the step d) includes the step d1) of forming the first insulating sidewall on a side surface of the gate electrode and the step of d2) of forming the second insulating sidewall on the side surface of the gate electrode with the first insulating sidewall interposed therebetween.

10 14. The method of claim 13, further comprising, between the step d1) and the step d2), the step of removing part of the high dielectric constant gate insulating film located in the external side to the first insulating sidewall.

15 15. The method of claim 13, further comprising:

between d1) and the step d2), the step of etching part of the high dielectric gate insulating film located in an external side to the first insulating sidewall to reduce a thickness of the part; and

after the step d2), the step of removing part of the high dielectric constant gate insulating film located in an external side to the second insulating sidewall.

20

16. The method of claim 12, wherein the high dielectric constant gate insulating film is selectively removed by wet etching.

17. The method of claim 14, wherein the high dielectric constant gate insulating
25 film is selectively removed by wet etching.

18. The method of claim 15, wherein the high dielectric constant gate insulating film is selectively removed by wet etching.

5 19. The method of claim 11, wherein the step b) includes the step of forming a protective film for covering an upper surface of the gate electrode, and

 the method further includes, after the step d), the step of siliciding a surface of part of the active region located in the external side to the insulating sidewall, removing the protective film and then fully siliciding the gate electrode.

10

 20. The method of claim 11, further comprising before the step a), the step of forming a buffer insulating film on the active region,

 wherein in the step a), the high dielectric constant gate insulating film is formed on the active region with the buffer insulating film interposed therebetween.

15

ABSTRACT OF THE DISCLOSURE

A semiconductor device includes: a high dielectric constant gate insulating film formed on an active region in a substrate; a gate electrode formed on the high dielectric constant gate insulating film; and an insulating sidewall formed on each side surface of the
5 gate electrode. The high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall. At least part of the high dielectric constant gate insulating film located under the insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

FIG. 1

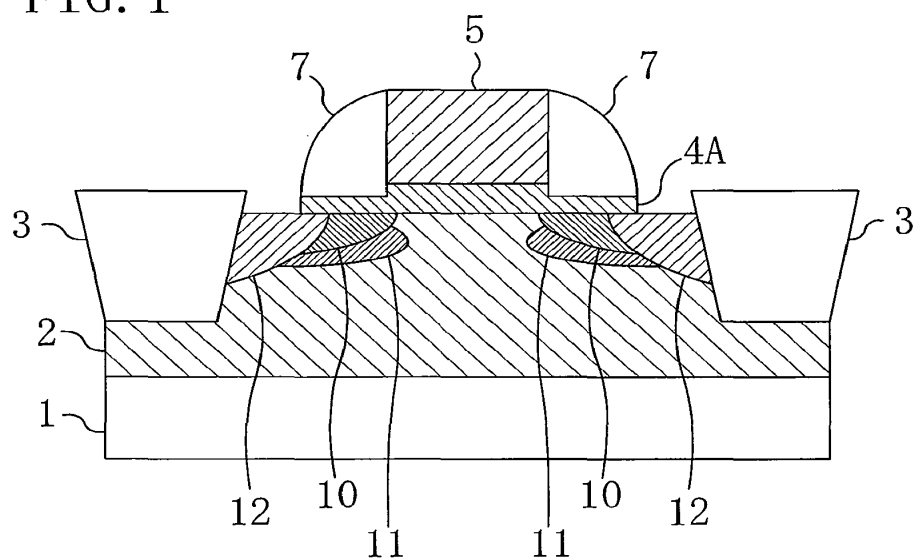


FIG. 2

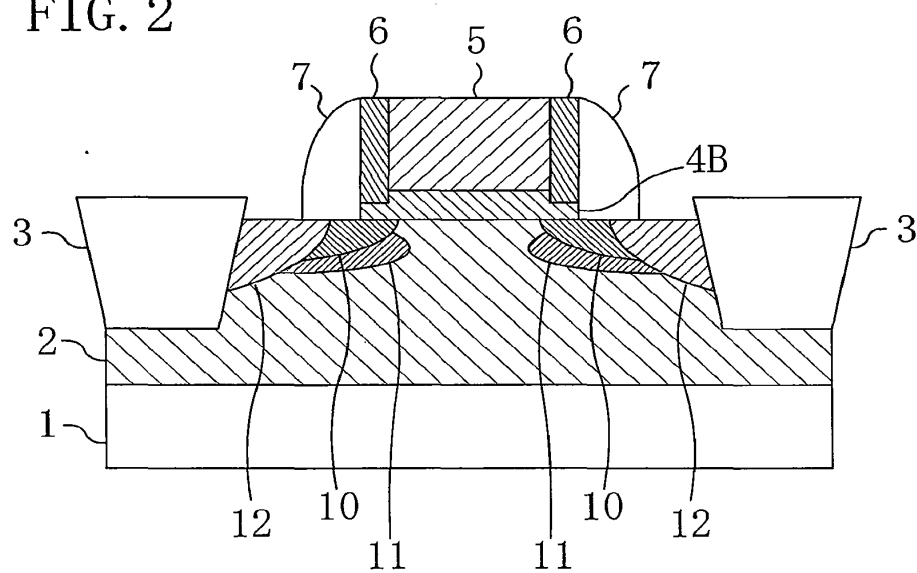


FIG. 3

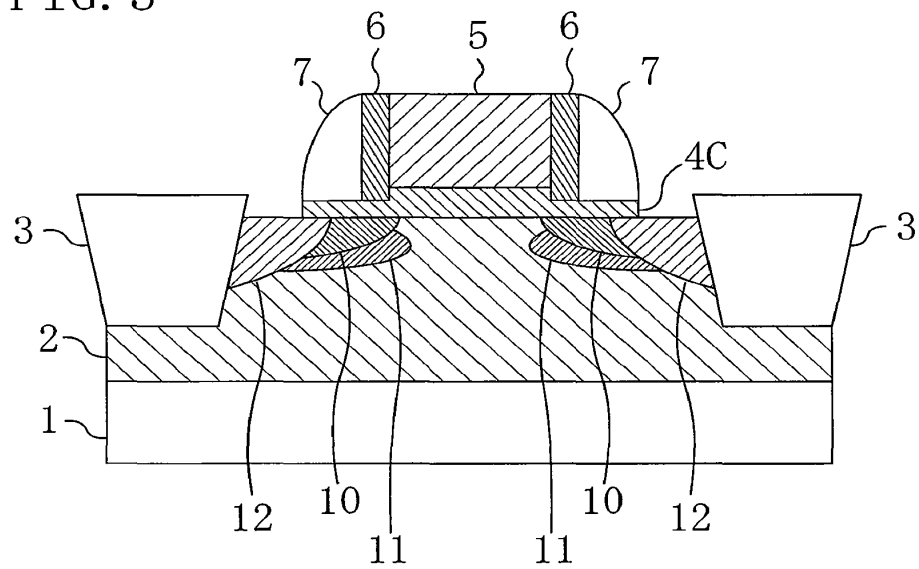


FIG. 4

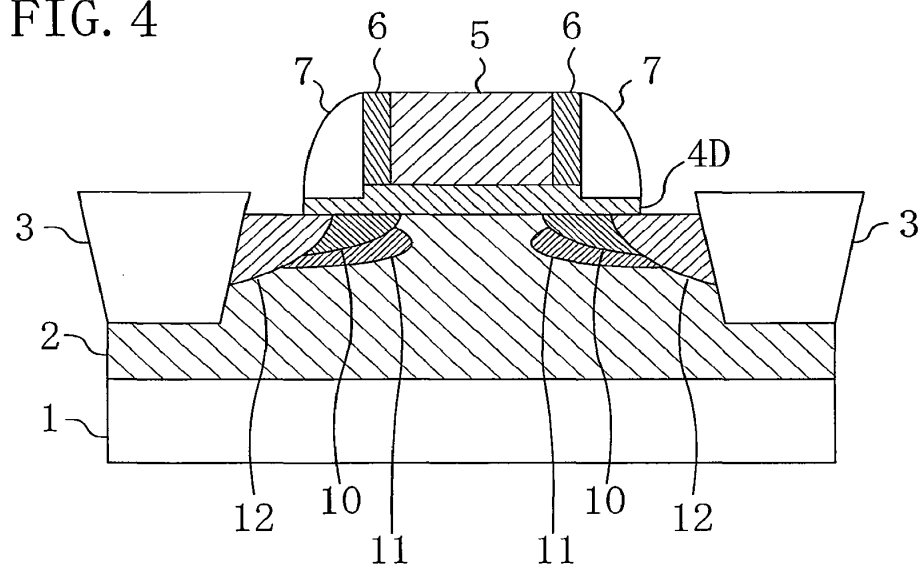


FIG. 5

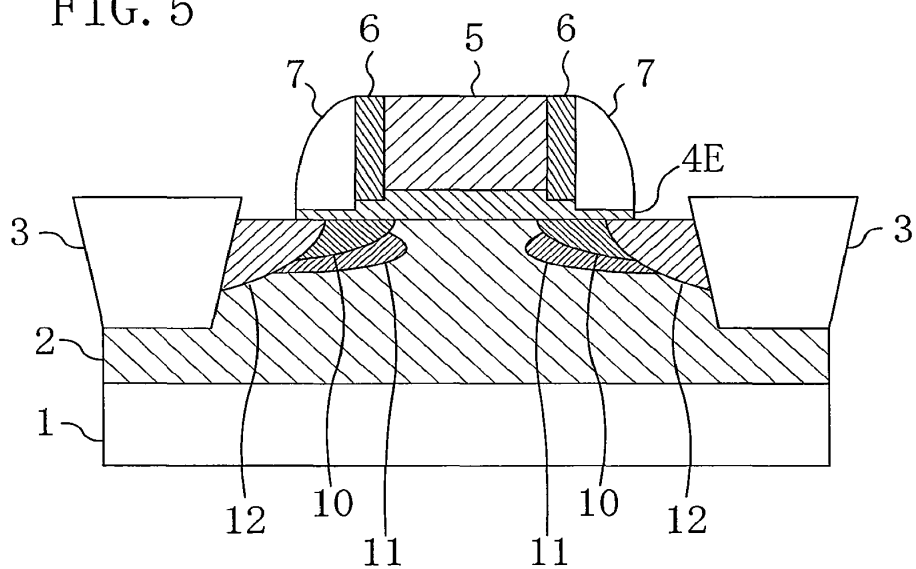


FIG. 6

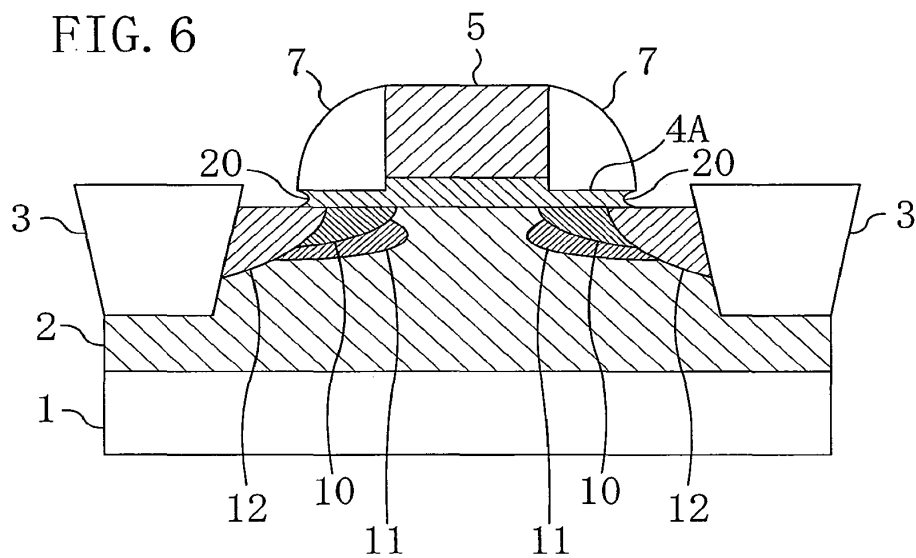


FIG. 7

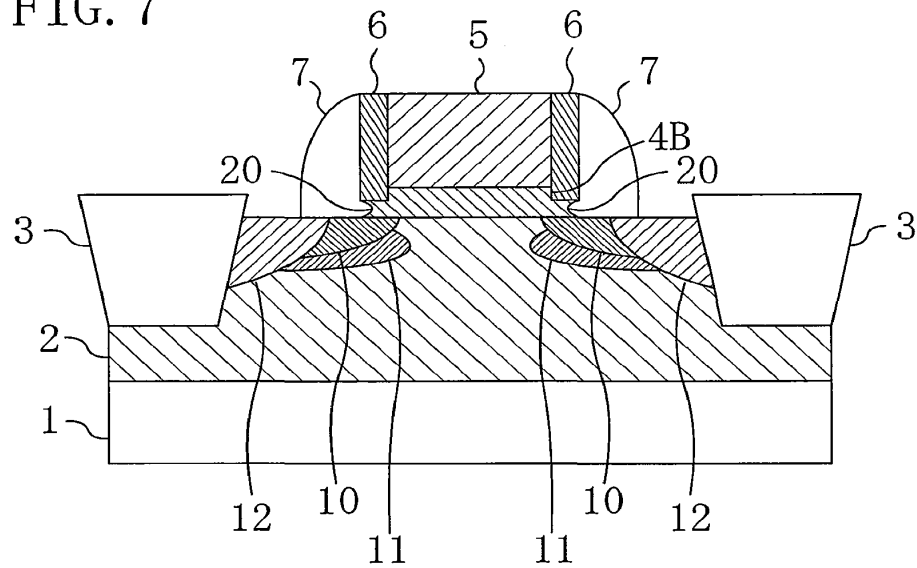


FIG. 8

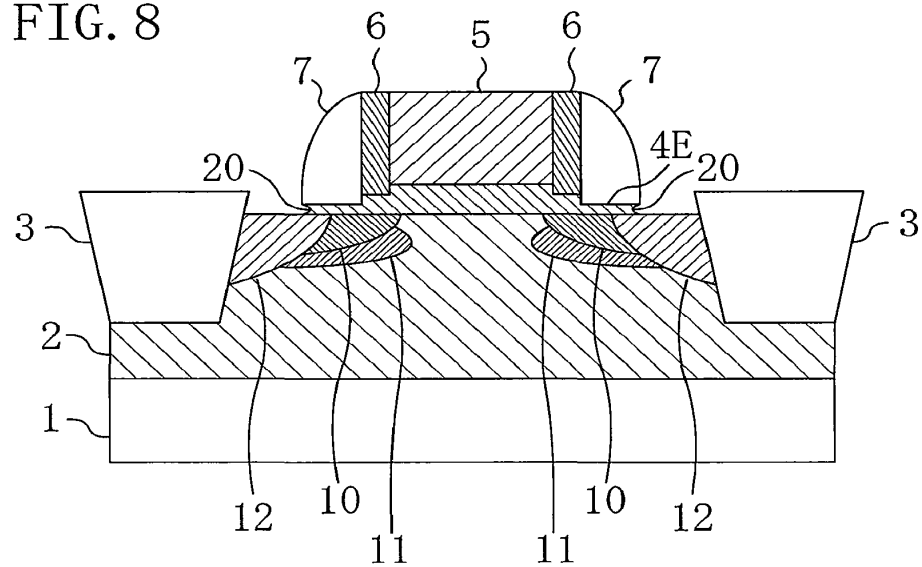


FIG. 9

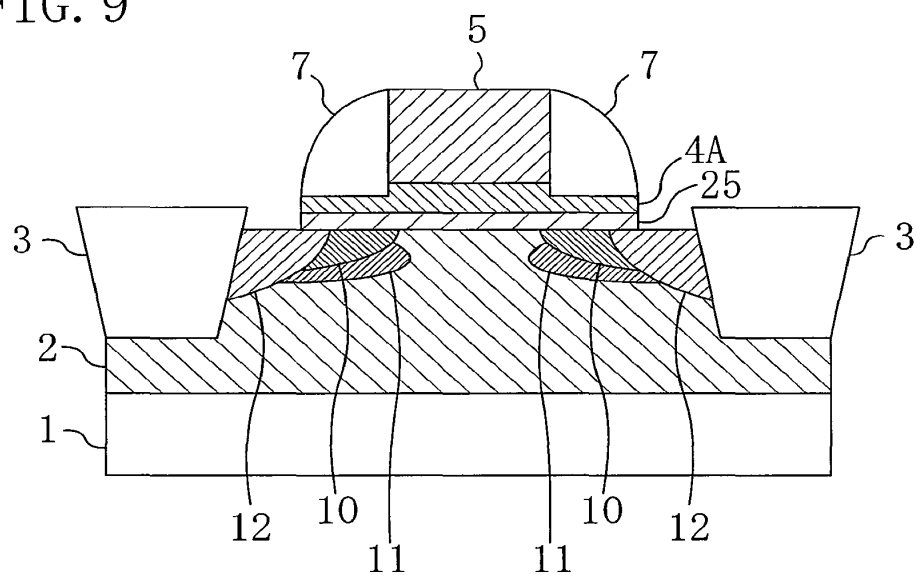


FIG. 10

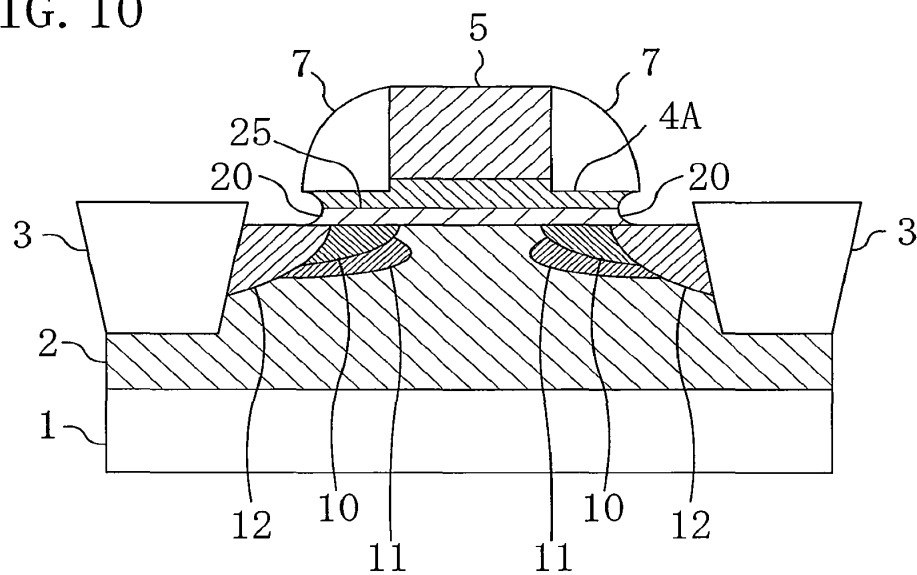


FIG. 11A

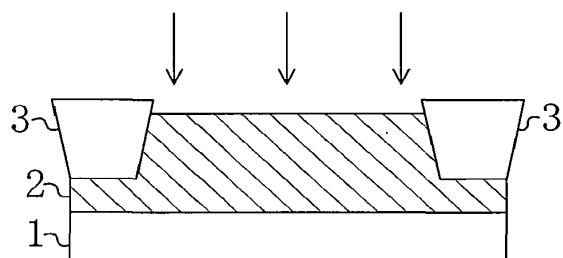


FIG. 11D

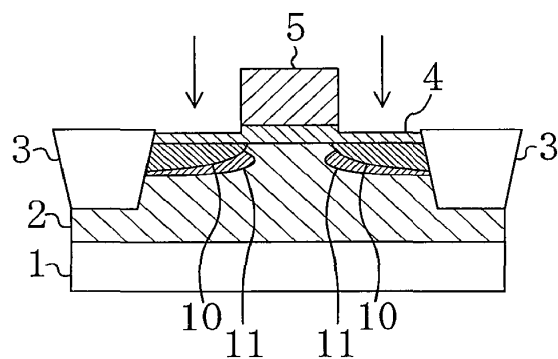


FIG. 11B

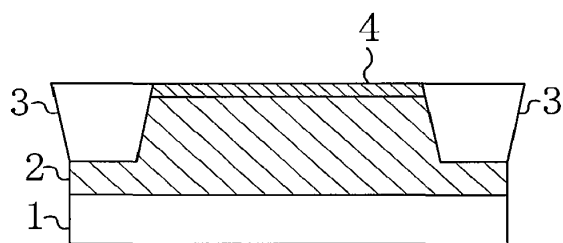


FIG. 11E

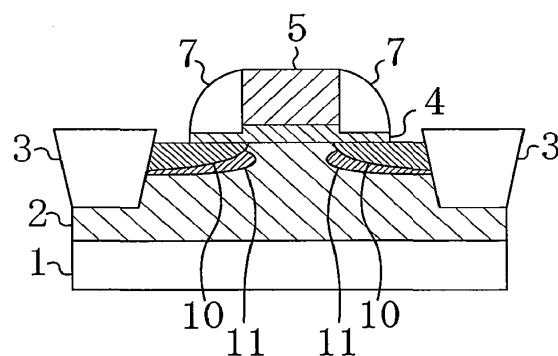


FIG. 11C

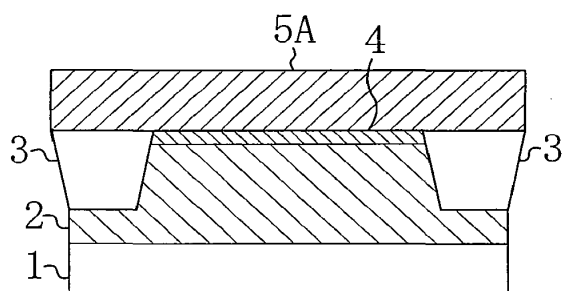


FIG. 11F

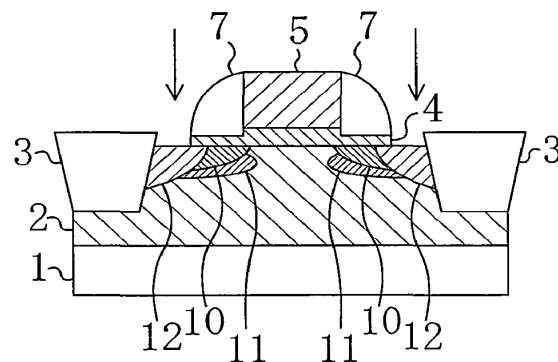


FIG. 12A

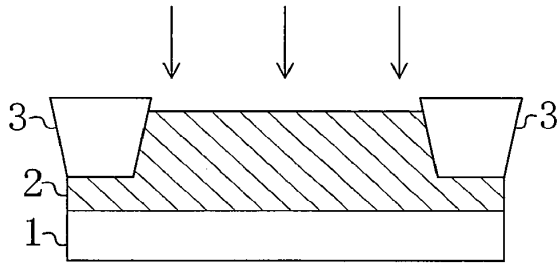


FIG. 12E

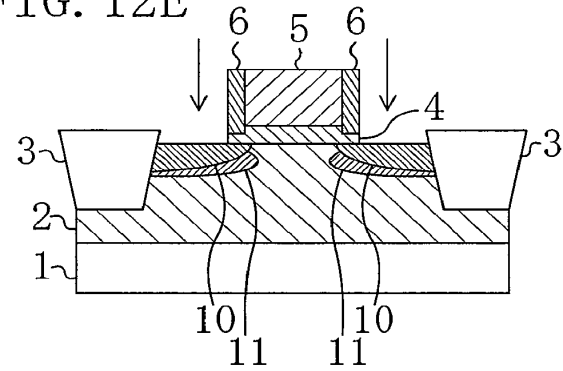


FIG. 12B

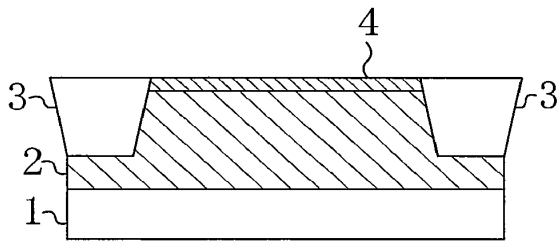


FIG. 12F

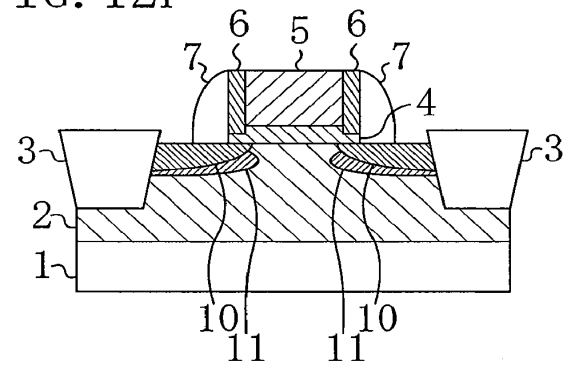


FIG. 12C

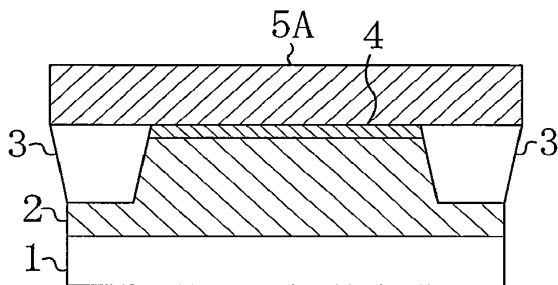


FIG. 12G

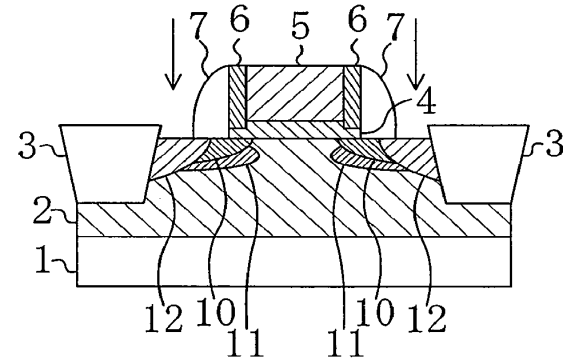


FIG. 12D

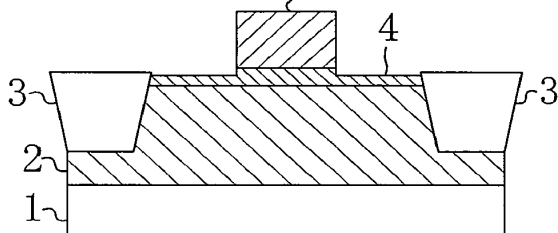


FIG. 13A

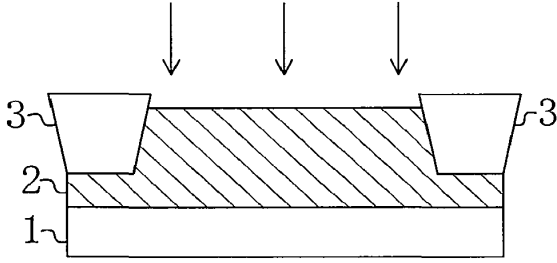


FIG. 13E

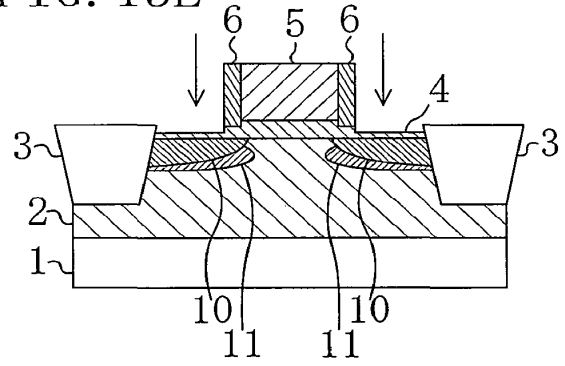


FIG. 13B

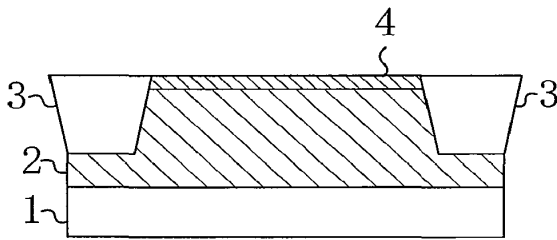


FIG. 13F

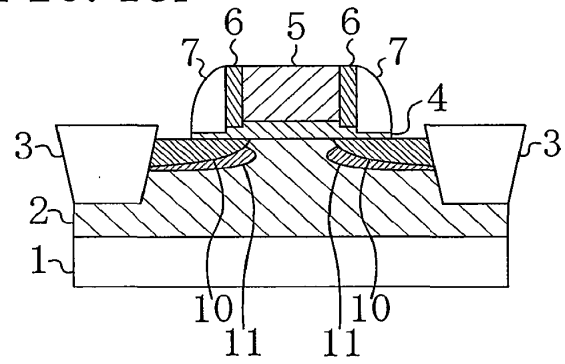


FIG. 13C

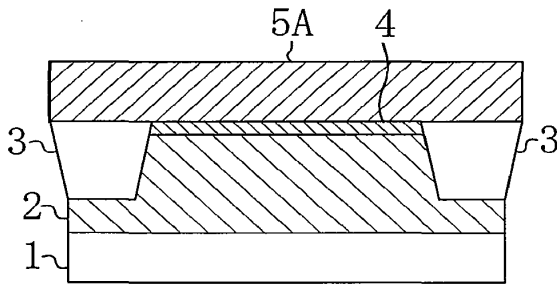


FIG. 13G

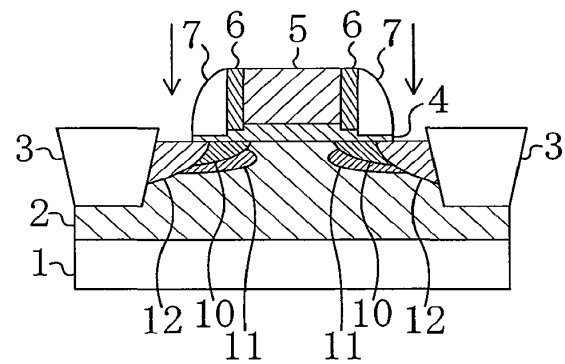


FIG. 13D

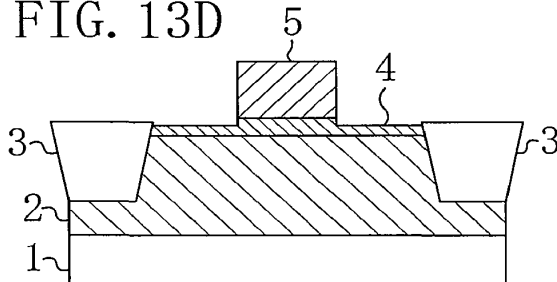


FIG. 14A

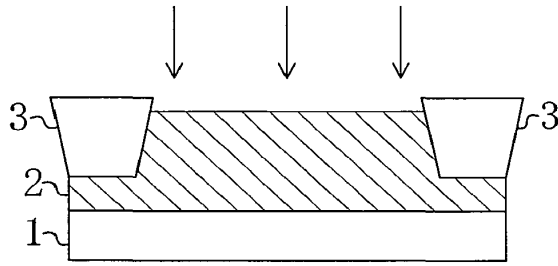


FIG. 14E

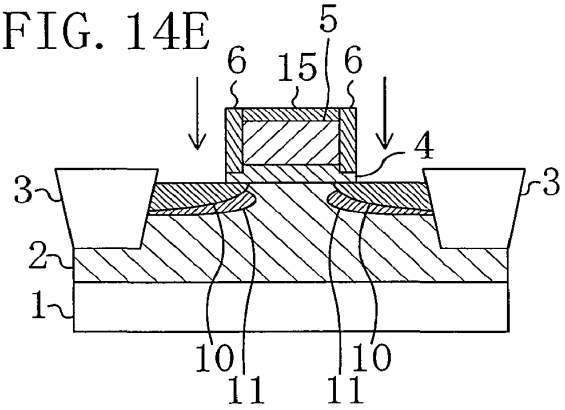


FIG. 14B

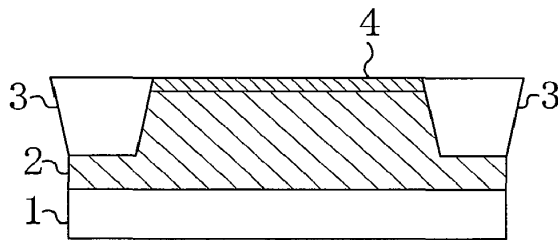


FIG. 14F

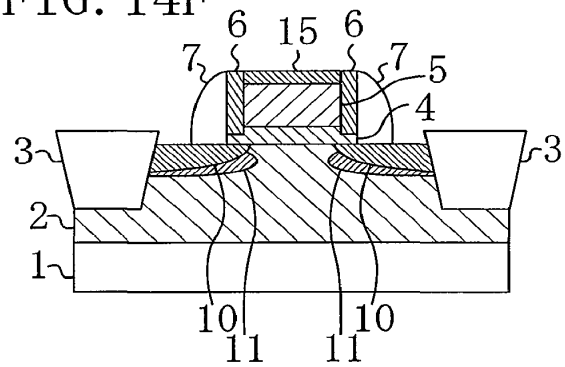


FIG. 14C

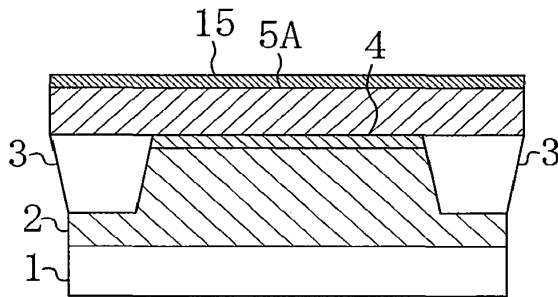


FIG. 14G

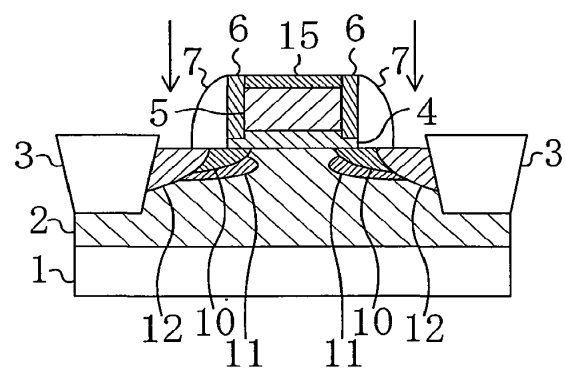


FIG. 14D

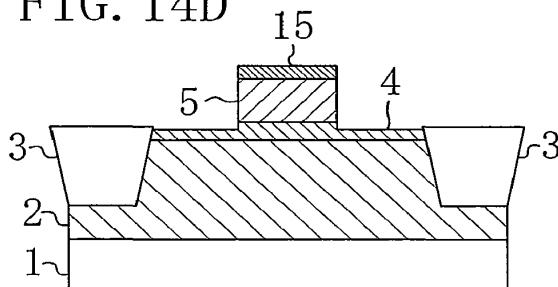


FIG. 15A

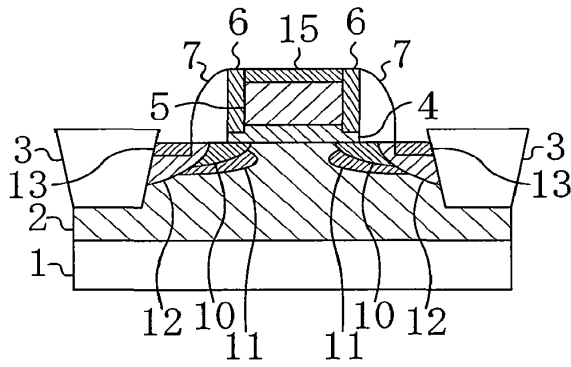


FIG. 15C

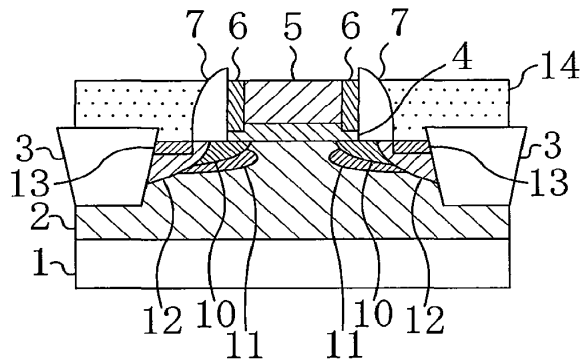


FIG. 15B

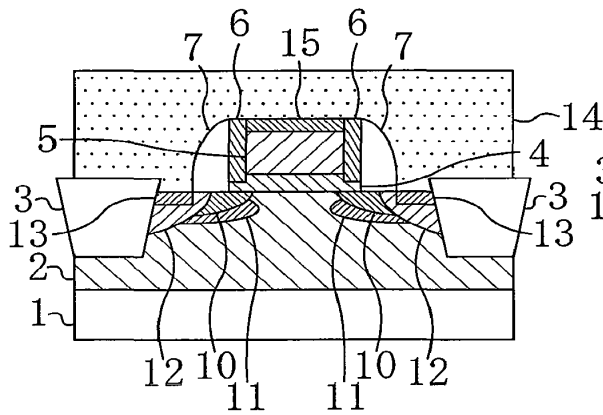


FIG. 15D

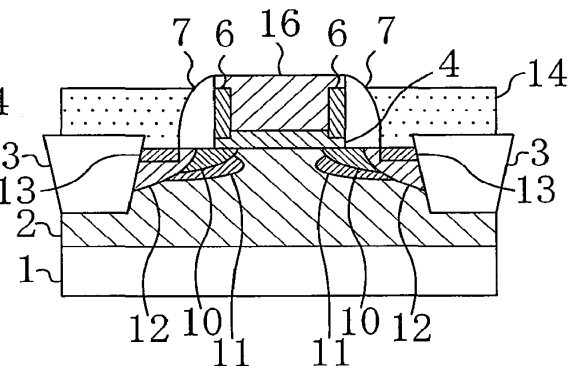


FIG. 16A
PRIOR ART

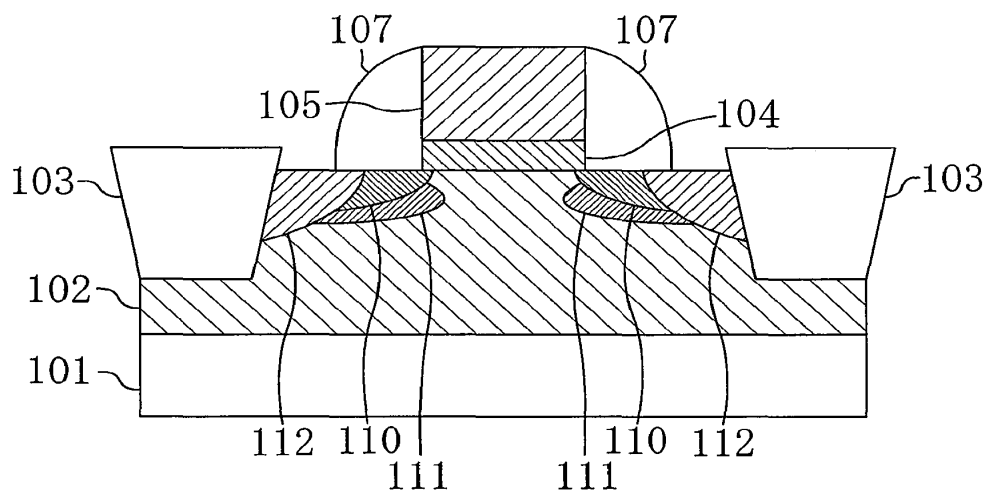
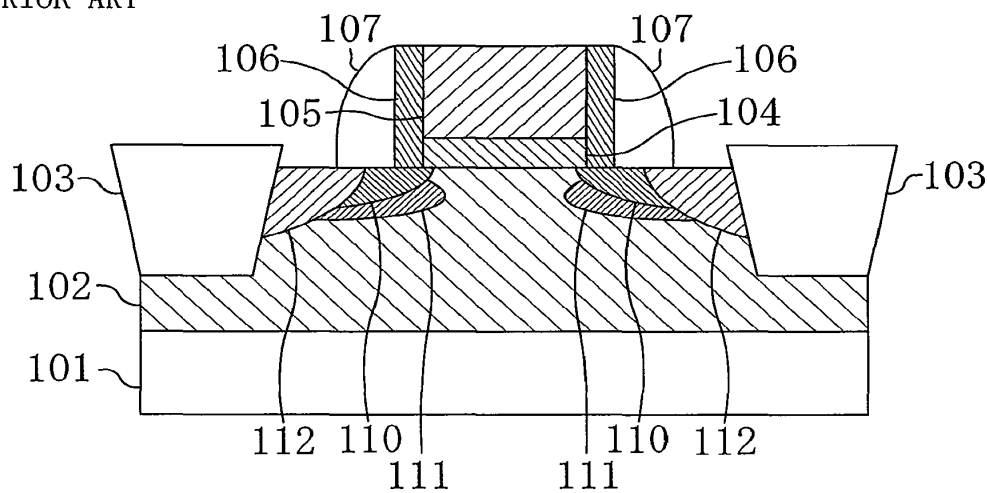


FIG. 16B
PRIOR ART



Docket No.

DECLARATION AND POWER OF ATTORNEY FOR U.S. PATENT APPLICATION
☒ Original ☐ Supplemental ☐ Substitute ☐ PCT ☐ Design

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; and I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Title: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

which is described and claimed in (if the following box is not checked, the specification of which is attached hereto):

- ☒ the attached specification, or
☐ the specification in the Application No. _____ filed on _____;
and with amendments filed on _____ (if applicable), or
☐ the specification in International Application No. PCT/ _____,
filed _____ and as amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above.

I acknowledge my duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a-d), §172, or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below, and have also identified below any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NO.	DATE OF FILING	PRIORITY CLAIMED
JAPAN	2005-227457	August 5, 2005	Yes

☐ Additional foreign or international application numbers are listed on a supplemental priority sheet attached hereto.

I hereby claim the benefit under Title 35, United States Code §119(e) of any United States Provisional application(s) listed below.

Number	(Day/Month/Year Filed)

☐ Additional U.S. provisional application numbers are listed on a supplemental priority sheet attached hereto.

Docket No.

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s), or §365(C) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

APPLICATION NO.	U.S. FILING DATE	STATUS: PATENTED, PENDING, ABANDONED

☐ Additional U.S. or international application numbers are listed on a supplemental priority sheet attached hereto.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the attorneys and agents associated with U.S. Patent and Trademark Office Customer Number identified below to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith, and direct that all correspondence be addressed to that customer number.

I hereby authorize the U.S. attorneys and agents associated with the customer number to accept and follow instructions from Matsushita Electric Industrial Co., Ltd., and any affiliated or subsidiary company thereof, received via their corporate representatives and/or their foreign patent attorneys or agents, if any, as to any action to be taken in the U.S. Patent and Trademark Office regarding this application without direct communication between the U.S. attorneys or agents and myself.

Direct Correspondence to:

CUSTOMER NUMBER 53080

I further declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Full Name of Sole or First Inventor	FIRST NAME Junji	LAST NAME HIRASE	SIGNATURE <i>Junji Hirase</i>	DATE OF SIGNATURE May 11, 2006
Residence & Citizenship	CITY Osaka	STATE OR COUNTRY Japan	COUNTRY OF CITIZENSHIP Japan	
Post Office Address	ADDRESS C/O Matsushita Electric Industrial Co., Ltd., 1006, Oaza Kadoma, Kadoma-shi, Osaka	CITY Osaka	STATE OR COUNTRY Japan	ZIP CODE 571-8501

Full Name of Second Inventor	FIRST NAME Akio	LAST NAME SEBE	SIGNATURE <i>Akio Sebe</i>	DATE OF SIGNATURE May 11, 2006
Residence & Citizenship	CITY Osaka	STATE OR COUNTRY Japan	COUNTRY OF CITIZENSHIP Japan	
Post Office Address	ADDRESS C/O Matsushita Electric Industrial Co., Ltd., 1006, Oaza Kadoma, Kadoma-shi, Osaka	CITY Osaka	STATE OR COUNTRY Japan	ZIP CODE 571-8501

Full Name of Third Inventor	FIRST NAME Naoki	LAST NAME KOTANI	SIGNATURE <i>Naoki Kotani</i>	DATE OF SIGNATURE May 11, 2006
Residence & Citizenship	CITY Hyogo	STATE OR COUNTRY Japan	COUNTRY OF CITIZENSHIP Japan	
Post Office Address	ADDRESS C/O Matsushita Electric Industrial Co., Ltd., 1006, Oaza Kadoma, Kadoma-shi, Osaka	CITY Japan	STATE OR COUNTRY Japan	ZIP CODE 571-8501

Full Name of Fourth Inventor	FIRST NAME Gen	LAST NAME OKAZAKI	SIGNATURE <i>Gen Okazaki</i>	DATE OF SIGNATURE May 11, 2006
Residence & Citizenship	CITY Hyogo	STATE OR COUNTRY Japan	COUNTRY OF CITIZENSHIP Japan	
Post Office Address	ADDRESS C/O Matsushita Electric Industrial Co., Ltd., 1006, Oaza Kadoma, Kadoma-shi, Osaka	CITY Japan	STATE OR COUNTRY Japan	ZIP CODE 571-8501

Full Name of Fifth Inventor	FIRST NAME Kazuhiko	LAST NAME AIDA	SIGNATURE <i>Kazuhiko Aida</i>	DATE OF SIGNATURE May 18, 2006
Residence & Citizenship	CITY Chiba	STATE OR COUNTRY Japan	COUNTRY OF CITIZENSHIP Japan	
Post Office Address	ADDRESS C/O Matsushita Electric Industrial Co., Ltd., 1006, Oaza Kadoma, Kadoma-shi, Osaka	CITY Japan	STATE OR COUNTRY Japan	ZIP CODE 571-8501

Full Name of Sixth Inventor	FIRST NAME Shinji	LAST NAME TAKEOKA	SIGNATURE <i>Shinji TAKEOKA</i>	DATE OF SIGNATURE May 11, 2006
Residence & Citizenship	CITY Osaka	STATE OR COUNTRY Japan	COUNTRY OF CITIZENSHIP Japan	
Post Office Address	ADDRESS C/O Matsushita Electric Industrial Co., Ltd., 1006, Oaza Kadoma, Kadoma-shi, Osaka	CITY Japan	STATE OR COUNTRY Japan	ZIP CODE 571-8501

Full Name of Seventh Inventor	FIRST NAME	LAST NAME	SIGNATURE	DATE OF SIGNATURE
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP	
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE

(If there are more than seven inventors, please add a copy of this page for identification and signature for the additional inventors)

The above application may be more particularly identified as follows:

U.S. Application No. _____ Filing Date _____

Applicant Reference Number P42042-01 Attorney Docket No. _____

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Junji HIRASE, et al.	:	Confirmation Number: Not Yet Assigned
	:	
Application No.: Divisional of U.S.	:	
Serial No. 12/505,799	:	Group Art Unit: Not Yet Assigned
	:	
Filed: March 1, 2011	:	Examiner: Not Yet Assigned
	:	
For: SEMICONDUCTOR DEVICE (as amended)	:	

PRELIMINARY AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Prior to examination of the above-referenced application, please amend the application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims begin on page 3 of this paper.

Remarks/Arguments begin on page 7 of this paper.

IN THE SPECIFICATION:

1) Please amend the Title of the Invention as follows:

~~SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME~~

2) Please insert the following new paragraph after the Title and before the “BACKGROUND OF THE INVENTION”:

-- RELATED APPLICATIONS

This application is a Divisional of U.S. Patent Application No. 12/505,799, filed on July 20, 2009, which is a Divisional of U.S. Patent Application No. 11/491,260, filed on July 24, 2006, now U.S. Patent No. 7,579,227, claiming priority of Japanese Patent Application No. 2005-227457, filed on August 5, 2005, the entire contents of each of which are incorporated by reference. --

IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application

Listing of Claims:

1-20. (Cancelled)

21. (New) A semiconductor device comprising:

a high dielectric constant gate insulating film formed on an active region in a substrate;

a gate electrode formed on the high dielectric constant gate insulating film;

a insulating sidewall formed on each side surface of the gate electrode; and

wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall, and

an end of the high dielectric constant gate insulating film under the insulating sidewall is located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode.

22. (New) The semiconductor device of claim 21, further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film.

23. (New) The semiconductor device of claim 22, wherein the buffer insulating film is a silicon oxide film.

24. (New) The semiconductor device of claim 22, wherein

the buffer insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall, and

an end of the buffer insulating film is located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode.

25. (New) The semiconductor device of claim 21, wherein

a smallest thickness of part of the high dielectric constant gate insulating film located under the insulating sidewall is smaller than that of part of the high dielectric constant gate insulating film located under the gate electrode.

26. (New) The semiconductor device of claim 21, wherein the high dielectric constant gate insulating film is formed of a Hf based oxide.

27. (New) The semiconductor device of claim 21, wherein the high dielectric constant gate insulating film is formed of a HfSiON film.

28. (New) The semiconductor device of claim 21, wherein an extension region of a first conductivity type is formed in part of the active region located under the insulating sidewall, and a pocket region of a second conductivity type is formed in part of the active region located under the extension region.

29. (New) The semiconductor device of claim 28, wherein each of source/drain regions of a first conductivity type is formed in part of the active region located in an external side to the extension region and the pocket region when viewed from the gate electrode.

30. (New) The semiconductor device of claim 21, wherein a part of the high dielectric constant gate insulating film located under the insulating sidewall includes a notch at the end thereof.

31. (New) The semiconductor device of claim 21, wherein a part of the high dielectric constant gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.

32. (New) The semiconductor device of claim 22, wherein an end of the buffer insulating film is located at a predetermined distance from a side end of the gate electrode toward the insulating sidewall.

33. (New) The semiconductor device of claim 21, wherein

the end of the high dielectric constant gate insulating film is located at a predetermined distance from a side end of the gate electrode toward the insulating sidewall.

34. (New) The semiconductor device of claim 21, wherein
the insulating sidewall has a double layer structure including an oxide film and a nitride film.

35. (New) The semiconductor device of claim 21, wherein
wherein the insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film.

36. (New) The semiconductor device of claim 21, wherein
a width of the high dielectric constant gate insulating film along a gate length is larger than a width of the gate electrode along the gate length.

37. (New) The semiconductor device of claim 21, wherein
a width of a bottom surface of the high dielectric constant gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length.

38. (New) The semiconductor device of claim 21, wherein
the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more.

39. (New) The semiconductor device of claim 21, wherein
the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the insulating sidewall.

40. (New) The semiconductor device of claim 21, wherein
the high dielectric constant gate insulating film is formed to have a convex cross-sectional shape.

41. (New) The semiconductor device of claim 21, wherein
the end of the high dielectric constant gate insulating film located under the insulating
sidewall has a tapered surface.

42. (New) The semiconductor device of claim 21, wherein
the high dielectric constant gate insulating film located under the insulating sidewall has
a thickness which becomes smaller toward the end thereof.

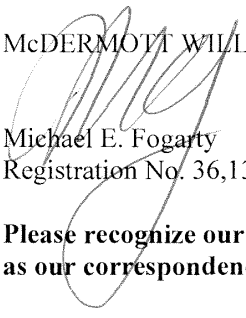
REMARKS

The title has been amended. The specification in the above-referenced application has been amended to incorporate the continuity information. Additionally, the amendment cancels claims 1-20, without prejudice. Claims 21-42 have been added and are pending for examination in this Divisional application.

No new matter has been introduced. Entry of this amendment is respectfully requested.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP


Michael E. Fogarty
Registration No. 36,139

**Please recognize our Customer No. 53080
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Date: March 1, 2011

- 7 -

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Junji HIRASE, et al.	:	Confirmation Number: Not Yet Assigned
	:	
Application No.: Divisional of U.S.	:	
Serial No. 12/505,799	:	Group Art Unit: Not Yet Assigned
	:	
Filed: March 01, 2011	:	Examiner: Not Yet Assigned
	:	
For: SEMICONDUCTOR DEVICE (as amended)	:	

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

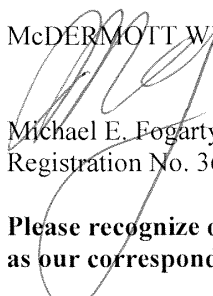
Divisional of U.S. Serial No. 12/505,799

The references were cited by or submitted to the U.S. Patent and Trademark Office in parent application Serial no. 12/505,799, filed July 20, 2009, which is relied upon for an earlier filing date under 35 USC 120. Thus, copies of these references are not attached. 37 CFR 1.98(d).

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP


Michael E. Fogarty
Registration No. 36,139

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as our correspondence address.**

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Date: March 1, 2011

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Substitute for form 1449/PTO)

 ATTY. DOCKET NO.
085393-0499

 SERIAL NO.
**Divisional of U.S.
Serial No. 12/505,799**

 APPLICANT
Junji HIRASE, et al.

 FILING DATE
March 1, 2011

 GROUP
Not Yet Assigned

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US 6,992,358	01-2006	Hieda et al.	
		US 6,929,992	08-2005	Djomehri et al.	
		US 6,642,071	11-2003	Cheng, Jia-Shyong	
		US 2006/0121740 A2	6/8/2006	SAKAI et al.	
		US 2003/0022422 A1	01-30-2003	TORII et al.	
		US 2004/0004234 A1	01-08-2004	YAGISHITA et al.	
		US 2004/0129997 A1	07-08-2004	MORIFUJI	
		US 2005/0121733 A1	06-09-2005	CHEN et al.	
		US 2005/0127436 A1	06-16-2005	HENSON et al.	Corresponds w/ CN 1610129 A
		US 7,579,227	08-2009	Hirase et al.	
		US 2005/0121733	06-2005	Chen et al.	
		US 6,992,358	01-2006	Hieda et al.	

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes - Number - Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes No
		CN 1610129 A	04-27-2005		Corresponds w/ US 2005/0127436	
		JP 2005-064190	03-10-2005	TOSHIBA CORP.		
		JP 2004-356576	12-16-2004	SEMICONDUCTOR LEADING EDGE TECHNOLOGIES INC.		

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
		WATANABE, Ken, Partial English Translation of "HfSiON-CMOS technology for achieving high performance and high reliability," SEMI FORUM Japan, 2005, IT System & ULSI Technology,
		HORI, Takashi, "1/4-μm LATID (LArge-Tilt-angle Implanted Drain) TECHNOLOGY FOR 3.3-V OPERATION", CH2637-7/89/0000-0777 1989 IEEE, IEDM 89-777-780-IEDM 89
		SAYAMA, et al., H., "80nm CMOSFET Technology Using Double Offset-Implanted Source/Drain Extension and Low Temperature SiN Process", IEDM 2000, IEDM 00-239-242-IEDM 00
		U.S. Office Action issued in U.S. Patent Application No. 11/543,865 dated on November 12, 2008
		Chinese Office Action, with English Translation, issued in Chinese Patent Application No. CN 200610093872.2, dated March 20, 2009.
		Notice Allowance issued in United States Patent Application No. 12/505,799, mailed December 13, 2010.

EXAMINER

DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		SEMICONDUCTOR DEVICE		
First Named Inventor/Applicant Name:		Junji HIRASE		
Filer:		Michael E. Fogarty/Lydia Nguyen		
Attorney Docket Number:		085393-0499		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Claims in excess of 20	1202	2	52	104
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1194

Electronic Acknowledgement Receipt	
EFS ID:	9561356
Application Number:	13037831
International Application Number:	
Confirmation Number:	7641
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Junji HIRASE
Customer Number:	53080
Filer:	Michael E. Fogarty/Lydia Nguyen
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0499
Receipt Date:	01-MAR-2011
Filing Date:	
Time Stamp:	15:43:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1194
RAM confirmation Number	2170
Deposit Account	500417
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	P04204204_TRN_085393-0499.pdf	55386	no	3
			3e10f5201d87f9f86ff543a360451bd123e3919		
Warnings:					
Information:					
2		P04204204_SPEC_085393-0499.pdf	1922108	yes	45
			154b99f4b6493d2c8ca431ef449b9cf038d9d00c		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	39	
	Claims		40	44	
	Abstract		45	45	
Warnings:					
Information:					
3	Drawings-only black and white line drawings	P04204204_DRW_085393-0499.pdf	329338	no	11
			b0ada9f7d08ecd10e42f8871134273680845a72d		
Warnings:					
Information:					
4	Oath or Declaration filed	P04204204_DEC_085393-0499.pdf	160323	no	3
			345e8dcf1d9b36c5e647c41949ff11ae27c885c2		
Warnings:					
Information:					
5	Preliminary Amendment	P04204204_AMEND-P_085393-0499.pdf	76365	no	7
			ae079f007f3fae45179a14136e5191ba5ade5065		
Warnings:					
Information:					
6	Information Disclosure Statement (IDS) Filed (SB/08)	P04204204_IDS_085393-0499.pdf	82895	no	3
			54c9cb06acae832015276e095730d0536b2Zb658		
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					

7	Fee Worksheet (PTO-875)	fee-info.pdf	36342 d148ef5c381d65779546455270dac8c3c48f4143	no	2
Warnings:					
Information:					
Total Files Size (in bytes):				2662757	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 13/037,831		Filing Date 03/01/2011		☐ To be Mailed						
APPLICATION AS FILED – PART I															
(Column 1)			(Column 2)			SMALL ENTITY ☐		OR		OTHER THAN SMALL ENTITY					
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)							
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A				N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A		N/A		N/A				N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A				N/A					
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =		*		X \$ =		OR		X \$ =					
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =		*		X \$ =		OR		X \$ =					
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).													
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))															
* If the difference in column 1 is less than zero, enter "0" in column 2.															
APPLICATION AS AMENDED – PART II															
(Column 1)			(Column 2)			(Column 3)			SMALL ENTITY		OR		OTHER THAN SMALL ENTITY		
AMENDMENT	03/01/2011		CLAIMS REMAINING AFTER AMENDMENT				HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))		* 22		Minus		** 20		= 2		X \$ =		OR X \$52=		
	Independent (37 CFR 1.16(h))		* 1		Minus		***3		= 0		X \$ =		OR X \$220=		
	☐ Application Size Fee (37 CFR 1.16(s))														
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))														
												TOTAL ADD'L FEE		OR TOTAL ADD'L FEE	
												104			
AMENDMENT			CLAIMS REMAINING AFTER AMENDMENT				HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))		*		Minus		**		=		X \$ =		OR X \$ =		
	Independent (37 CFR 1.16(h))		*		Minus		***		=		X \$ =		OR X \$ =		
	☐ Application Size Fee (37 CFR 1.16(s))														
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))														
												TOTAL ADD'L FEE		OR TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.															
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".															
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".															
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.															

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Legal Instrument Examiner:
/KIMBERLY JONES/

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/037,831			
APPLICATION AS FILED - PART I									
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)		
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	330		
SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A			N/A	540		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	220		
TOTAL CLAIMS (37 CFR 1.16(i))	22 minus 20 =	*				x 52 =	104		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 220 =	0.00		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00		
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00		
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1194		
APPLICATION AS AMENDED - PART II									
AMENDMENT A	(Column 1)	(Column 2)	(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		x =	
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
					TOTAL ADD'L FEE			TOTAL ADD'L FEE	
AMENDMENT B	(Column 1)	(Column 2)	(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		x =	
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
					TOTAL ADD'L FEE			TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.									



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
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WASHINGTON, DC 20005-3096

FILING RECEIPT



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Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

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Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)
JAPAN 2005-227457 08/05/2005

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

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page 1 of 3

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/037,831**

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SEMICONDUCTOR DEVICE

Preliminary Class

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This is to certify that the annexed is a true copy of the following application as filed with this Office.

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Date of Application: 2005年 8月 5日

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となる出願の国コードと出願
番号

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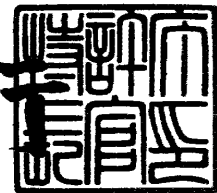
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【書類名】 特許請求の範囲

【請求項 1】

基板の活性領域上に形成された高誘電率ゲート絶縁膜と、
前記高誘電率ゲート絶縁膜上に形成されたゲート電極と、
前記ゲート電極の側面に形成された絶縁性サイドウォールとを備え、
前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記絶縁性サイドウォールの下側まで連続的に形成されており、
前記高誘電率ゲート絶縁膜における前記絶縁性サイドウォールの下側領域の少なくとも一部分の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さよりも小さいことを特徴とする半導体装置。

【請求項 2】

請求項 1 に記載の半導体装置において、
前記絶縁性サイドウォールは、前記ゲート電極の側面に形成された第 1 の絶縁性サイドウォールと、前記ゲート電極の側面に前記第 1 の絶縁性サイドウォールを介して形成された第 2 の絶縁性サイドウォールとからなり、
前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第 1 の絶縁性サイドウォールの下側まで連続的に形成されており、
前記高誘電率ゲート絶縁膜における前記第 1 の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さよりも小さいことを特徴とする半導体装置。

【請求項 3】

請求項 2 に記載の半導体装置において、
前記高誘電率ゲート絶縁膜は前記第 2 の絶縁性サイドウォールの下側には形成されていないことを特徴とする半導体装置。

【請求項 4】

請求項 2 に記載の半導体装置において、
前記高誘電率ゲート絶縁膜は前記第 2 の絶縁性サイドウォールの下側まで連続的に形成されており、
前記高誘電率ゲート絶縁膜における前記第 2 の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記第 1 の絶縁性サイドウォールの下側領域の厚さと同等であることを特徴とする半導体装置。

【請求項 5】

請求項 2 に記載の半導体装置において、
前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第 2 の絶縁性サイドウォールの下側まで連続的に形成されており、
前記高誘電率ゲート絶縁膜における前記第 2 の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記第 1 の絶縁性サイドウォールの下側領域の厚さよりも小さいことを特徴とする半導体装置。

【請求項 6】

請求項 1 に記載の半導体装置において、
前記絶縁性サイドウォールは、前記ゲート電極の側面に形成された第 1 の絶縁性サイドウォールと、前記ゲート電極の側面に前記第 1 の絶縁性サイドウォールを介して形成された第 2 の絶縁性サイドウォールとからなり、
前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第 2 の絶縁性サイドウォールの下側まで連続的に形成されており、
前記高誘電率ゲート絶縁膜における前記第 1 の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さと同等であり、
前記高誘電率ゲート絶縁膜における前記第 2 の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さよりも小さいことを特徴とする半導体装置。

【請求項 7】

請求項 1～6 のいずれか 1 項に記載の半導体装置において、
前記高誘電率ゲート絶縁膜の側端部にノッチが設けられていることを特徴とする半導体装置。

【請求項 8】

請求項 1～7 のいずれか 1 項に記載の半導体装置において、
前記基板と前記高誘電率ゲート絶縁膜との間にバッファ絶縁膜が設けられていることを特徴とする半導体装置。

【請求項 9】

請求項 8 に記載の半導体装置において、
前記バッファ絶縁膜はシリコン酸化膜又はシリコン酸窒化膜であることを特徴とする半導体装置。

【請求項 10】

請求項 1～9 のいずれか 1 項に記載の半導体装置において、
前記ゲート電極は、全領域がシリサイド化されたフルシリサイドゲート電極であることを特徴とする半導体装置。

【請求項 11】

基板の活性領域上に高誘電率ゲート絶縁膜を形成する工程（a）と、
前記高誘電率ゲート絶縁膜上にゲート電極を形成する工程（b）と、
前記工程（b）の後に、前記ゲート電極の外側に位置する前記高誘電率ゲート絶縁膜をエッチングして薄膜化する工程（c）と、
前記工程（c）の後に、前記ゲート電極の側面に絶縁性サイドウォールを形成する工程（d）とを備えていることを特徴とする半導体装置の製造方法。

【請求項 12】

請求項 11 に記載の半導体装置の製造方法において、
前記工程（d）の後に、前記絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜を除去する工程を備えていることを特徴とする半導体装置の製造方法。

【請求項 13】

請求項 11 に記載の半導体装置の製造方法において、
前記絶縁性サイドウォールは第 1 の絶縁性サイドウォールと第 2 の絶縁性サイドウォールとからなり、
前記工程（d）は、前記ゲート電極の側面に前記第 1 の絶縁性サイドウォールを形成する工程（d1）と、前記ゲート電極の側面に前記第 1 の絶縁性サイドウォールを介して前記第 2 の絶縁性サイドウォールを形成する工程（d2）とを含むことを特徴とする半導体装置の製造方法。

【請求項 14】

請求項 13 に記載の半導体装置の製造方法において、
前記工程（d1）と前記工程（d2）との間に、前記第 1 の絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜を除去する工程をさらに備えていることを特徴とする半導体装置の製造方法。

【請求項 15】

請求項 13 に記載の半導体装置の製造方法において、
前記工程（d1）と前記工程（d2）との間に、前記第 1 の絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜をエッチングしてさらに薄膜化する工程を備え、
前記工程（d2）よりも後に、前記第 2 の絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜を除去する工程をさらに備えていることを特徴とする半導体装置の製造方法。

【請求項 16】

請求項 12、14 又は 15 のいずれか 1 項に記載の半導体装置の製造方法において、
前記高誘電率ゲート絶縁膜の除去は、ウェットエッチングを用いて選択的に行われるこ

とを特徴とする半導体装置の製造方法。

【請求項 17】

請求項 11～16 のいずれか 1 項に記載の半導体装置の製造方法において、
前記工程 (b) は、前記ゲート電極の上面を覆う保護膜を形成する工程を含み、
前記工程 (d) よりも後に、前記絶縁性サイドウォールの外側に位置する前記活性領域の表面をシリサイド化した後、前記保護膜を除去し、その後、前記ゲート電極をフルシリサイド化する工程をさらに備えていることを特徴とする半導体装置の製造方法。

【請求項 18】

請求項 11～17 のいずれか 1 項に記載の半導体装置の製造方法において、
前記工程 (a) よりも前に、前記活性領域上にバッファ絶縁膜を形成する工程をさらに備え、
前記工程 (a) では前記活性領域上に前記バッファ絶縁膜を介して前記高誘電率ゲート絶縁膜を形成することを特徴とする半導体装置の製造方法。

【書類名】明細書

【発明の名称】半導体装置及びその製造方法

【技術分野】

【0001】

本発明は、半導体装置及びその製造方法、具体的にはMISFET (metal insulator semiconductor field effect transistor) の構造及び製造方法に関し、主にMISFETの駆動力及び信頼性を向上させる技術に関する。

【背景技術】

【0002】

近年、半導体集積回路装置の高集積化、高機能化及び高速化に伴ない、スケーリング則に従ってエクステンション (Extension) の接合深さを浅くすると同時に、MISFETのゲート絶縁膜として比誘電率が4程度のSiO₂系の絶縁膜に代えてHf系酸化物又はAl系酸化物等の比誘電率が10以上の高誘電率膜を用いようとしている。

【0003】

図16 (a) 及び (b) はそれぞれ従来の高誘電率ゲート絶縁膜を使ったMISFETの構造を示す断面図である (非特許文献1)。

【0004】

図16 (a) に示すように、基板101の活性領域であるウェル102におけるSTI (shallow trench isolation) 103によって囲まれた領域の上に高誘電率ゲート絶縁膜104を介してゲート電極105が形成されている。ゲート電極105の側面には絶縁性のサイドウォール107が形成されている。ウェル102におけるサイドウォール107の下側にはエクステンション領域110が形成されていると共にウェル102におけるエクステンション領域110の下側にはポケット領域111が形成されている。ウェル102におけるゲート電極105から見てエクステンション領域110及びポケット領域111の外側にはソース・ドレイン領域112が形成されている。

【0005】

図16 (b) に示す構造が図16 (a) に示す構造と異なっている点は、ゲート電極105の側面にサイドウォール107が絶縁性のオフセットサイドウォール106を介して形成されていることである。これにより、ゲート電極105とエクステンション領域110とのオーバーラップ量の最適化を容易に図ることができる。

【非特許文献1】 渡辺健、「高性能・高信頼性を実現する HfSiON-CMOS技術」、Semi . Forum Japan 2005

【非特許文献2】 T. Hori、IEDM Tech. Dig. 、1989年、p. 777

【非特許文献3】 H. Sayama他、IEDM Tech. Dig. 、2000年、p. 239

【発明の開示】

【発明が解決しようとする課題】

【0006】

しかしながら、従来の高誘電率ゲート絶縁膜を使ったMISFETの構造においては、高誘電率ゲート絶縁膜の側端部がサイドウォールに直接接しているため、例えばシリコン酸化膜等からなるサイドウォールの形成時に高誘電率ゲート絶縁膜の側端部の組成がSiO₂ に近づく等の問題が生じる。その結果、ゲート電極端部において高誘電率ゲート絶縁膜の誘電率低下や絶縁性低下が引き起こされ、それによってデバイス特性やゲート絶縁膜の信頼性が悪化してしまう。

【0007】

前記に鑑み、本発明は、高誘電率ゲート絶縁膜を劣化させることなくMISFETの特性を向上させることを目的とする。

【課題を解決するための手段】

【0008】

前記の目的を達成するために、本願発明者らは、サイドウォールの下側に高誘電率ゲート絶縁膜を残存させ、それにより高誘電率ゲート絶縁膜の側端部とサイドウォールとの接

触を防止したMISFET構造及びその製造方法を想到するに至った。ところで、サイドウォールの下側に高誘電率ゲート絶縁膜を残存させた場合には、ゲート・ドレイン間の容量が上昇して回路速度に悪影響が生じる。また、この場合、エクステンション注入やLDD (lightly doped drain) 注入を実施する際に、高誘電率膜を介在させた状態でイオン注入を行う必要がある。その際、以下の理由によって注入加速エネルギーが高くなるため、注入不純物の深さ方向への拡がりが大きくなってしまい、言い換えると、エクステンションやLDDの接合位置が深くなってしまい、その結果、所望のデバイス特性が得られなくなるといった問題が生じる。

【0009】

理由1) ゲート絶縁膜として高誘電膜を用いる場合、膜厚を薄くしなくても所望の誘電率が得られるため、膜厚が厚く設定される。

【0010】

理由2) 高誘電率膜は重金属を含んでいるため、注入イオン種のRp (Projection Range) が小さくなる。

【0011】

そこで、本願発明者らは、サイドウォールの下側に高誘電率ゲート絶縁膜を残存させ且つサイドウォール下側の高誘電率ゲート絶縁膜をゲート電極下側の高誘電率ゲート絶縁膜よりも薄く形成したMISFET構造及びその製造方法を想到するに至った。

【0012】

具体的には、本発明に係る半導体装置は、基板の活性領域上に形成された高誘電率ゲート絶縁膜と、前記高誘電率ゲート絶縁膜上に形成されたゲート電極と、前記ゲート電極の側面に形成された絶縁性サイドウォールとを備え、前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記絶縁性サイドウォールの下側まで連続的に形成されており、前記高誘電率ゲート絶縁膜における前記絶縁性サイドウォールの下側領域の少なくとも一部分の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さよりも小さい。

【0013】

本発明の半導体装置において、前記絶縁性サイドウォールは、前記ゲート電極の側面に形成された第1の絶縁性サイドウォールと、前記ゲート電極の側面に前記第1の絶縁性サイドウォールを介して形成された第2の絶縁性サイドウォールとからなり、前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第1の絶縁性サイドウォールの下側まで連続的に形成されており、前記高誘電率ゲート絶縁膜における前記第1の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さよりも小さくてもよい。

【0014】

前記絶縁性サイドウォールが前記第1の絶縁性サイドウォールと前記第2の絶縁性サイドウォールとからなる場合、前記高誘電率ゲート絶縁膜は前記第2の絶縁性サイドウォールの下側には形成されていなくてもよい。

【0015】

前記絶縁性サイドウォールが前記第1の絶縁性サイドウォールと前記第2の絶縁性サイドウォールとからなる場合、前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第2の絶縁性サイドウォールの下側まで連続的に形成されており、前記高誘電率ゲート絶縁膜における前記第2の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記第1の絶縁性サイドウォールの下側領域の厚さと同等であってもよい。

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【0016】

前記絶縁性サイドウォールが前記第1の絶縁性サイドウォールと前記第2の絶縁性サイドウォールとからなる場合、前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第2の絶縁性サイドウォールの下側まで連続的に形成されており、前記高誘電率ゲート絶縁膜における前記第2の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート

絶縁膜における前記第1の絶縁性サイドウォールの下側領域の厚さよりも小さくてもよい。

【0017】

本発明の半導体装置において、前記絶縁性サイドウォールは、前記ゲート電極の側面に形成された第1の絶縁性サイドウォールと、前記ゲート電極の側面に前記第1の絶縁性サイドウォールを介して形成された第2の絶縁性サイドウォールとからなり、前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第2の絶縁性サイドウォールの下側まで連続的に形成されており、前記高誘電率ゲート絶縁膜における前記第1の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さと同等であり、前記高誘電率ゲート絶縁膜における前記第2の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さよりも小さくてもよい。

【0018】

本発明の半導体装置において、前記高誘電率ゲート絶縁膜の側端部にノッチが設けられていてもよい。

【0019】

本発明の半導体装置において、前記基板と前記高誘電率ゲート絶縁膜との間にバッファ絶縁膜が設けられていてもよい。この場合、前記バッファ絶縁膜はシリコン酸化膜又はシリコン酸窒化膜であってもよい。

【0020】

本発明の半導体装置において、前記ゲート電極は、全領域がシリサイド化されたフルシリサイドゲート電極であってもよい。

【0021】

本発明に係る半導体装置の製造方法は、基板の活性領域上に高誘電率ゲート絶縁膜を形成する工程（a）と、前記高誘電率ゲート絶縁膜上にゲート電極を形成する工程（b）と、前記工程（b）の後に、前記ゲート電極の外側に位置する前記高誘電率ゲート絶縁膜をエッチングして薄膜化する工程（c）と、前記工程（c）の後に、前記ゲート電極の側面に絶縁性サイドウォールを形成する工程（d）とを備えている。

【0022】

本発明の半導体装置の製造方法において、前記工程（d）の後に、前記絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜を除去する工程を備えていてもよい。

【0023】

本発明の半導体装置の製造方法において、前記絶縁性サイドウォールは第1の絶縁性サイドウォールと第2の絶縁性サイドウォールとからなり、前記工程（d）は、前記ゲート電極の側面に前記第1の絶縁性サイドウォールを形成する工程（d1）と、前記ゲート電極の側面に前記第1の絶縁性サイドウォールを介して前記第2の絶縁性サイドウォールを形成する工程（d2）とを含んでいてもよい。

【0024】

前記工程（d）が前記工程（d1）と前記工程（d2）とを含む場合、前記工程（d1）と前記工程（d2）との間に、前記第1の絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜を除去する工程をさらに備えていてもよい。

【0025】

前記工程（d）が前記工程（d1）と前記工程（d2）とを含む場合、前記工程（d1）と前記工程（d2）との間に、前記第1の絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜をエッチングしてさらに薄膜化する工程を備え、前記工程（d2）よりも後に、前記第2の絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜を除去する工程をさらに備えていてもよい。

【0026】

本発明の半導体装置の製造方法において、前記高誘電率ゲート絶縁膜の除去は、ウェットエッチングを用いて選択的に行われてもよい。

【0027】

本発明の半導体装置の製造方法において、前記工程（b）は、前記ゲート電極の上面を覆う保護膜を形成する工程を含み、前記工程（d）よりも後に、前記絶縁性サイドウォールの外側に位置する前記活性領域の表面をシリサイド化した後、前記保護膜を除去し、その後、前記ゲート電極をフルシリサイド化する工程をさらに備えていてもよい。

【0028】

本発明の半導体装置の製造方法において、前記工程（a）よりも前に、前記活性領域上にバッファ絶縁膜を形成する工程をさらに備え、前記工程（a）では前記活性領域上に前記バッファ絶縁膜を介して前記高誘電率ゲート絶縁膜を形成してもよい。

【発明の効果】

【0029】

本発明によると、ゲート電極の下側からサイドウォールの下側まで高誘電率ゲート絶縁膜が連続的に形成されているため、言い換えると、ゲート端部での高誘電率ゲート絶縁膜の連続性が維持されているため、高誘電率ゲート絶縁膜の側端部がサイドウォール膜と直接接することに起因する、ゲート端部での高誘電率ゲート絶縁膜の誘電率低下及び絶縁性低下を抑制することができる。また、サイドウォール下側の高誘電率ゲート絶縁膜をゲート電極下側の高誘電率ゲート絶縁膜よりも薄く形成しているため、ゲート・ドレイン間の容量の上昇を抑制して回路速度への悪影響を低減することができる。さらに、エクステンション注入やLDD注入を実施する際に介在する高誘電率膜の膜厚が薄いため、注入加速エネルギーの増大を抑制できる。従って、エクステンションやLDDにおいて浅い接合を容易に形成できるので、デバイス特性の向上を図りやすい。

【発明を実施するための最良の形態】

【0030】

（第1の実施形態）

以下、本発明の第1の実施形態に係る半導体装置について、図面を参照しながら説明する。図1は、第1の実施形態に係る半導体装置（具体的にはシングルサイドウォール型のMISFET）の構造を示す断面図である。尚、本実施形態ではn型MISFETを用いて説明するが、本発明をp型MISFETに適用した場合にも同様の効果を得ることができる。

【0031】

図1に示すように、例えばシリコンからなる基板1に形成されたp型ウェル2におけるSTI3によって囲まれた活性領域の上に高誘電率ゲート絶縁膜4Aを介してゲート電極5が形成されている。ゲート電極5の側面には絶縁性のサイドウォール7が形成されている。p型ウェル2におけるサイドウォール7の下側にはn型エクステンション領域10が形成されていると共にp型ウェル2におけるn型エクステンション領域10の下側にはp型ポケット領域11が形成されている。p型ウェル2におけるゲート電極5から見てn型エクステンション領域10及びp型ポケット領域11の外側にはn型ソース・ドレイン領域12が形成されている。

【0032】

本実施形態の第1の特徴は、ゲート電極5の下側のみならずサイドウォール7の下側にも高誘電率ゲート絶縁膜4Aが残存していることである。すなわち、高誘電率ゲート絶縁膜4Aはゲート電極5の下側からサイドウォール7の下側まで連続的に形成されている。

【0033】

また、本実施形態の第2の特徴は、高誘電率ゲート絶縁膜4Aにおけるサイドウォール7の下側領域の厚さは、高誘電率ゲート絶縁膜4Aにおけるゲート電極5の下側領域の厚さよりも小さいことである。すなわち、高誘電率ゲート絶縁膜4Aは凸形状に形成されている。

【0034】

本実施形態によると、高誘電率ゲート絶縁膜4Aの側端部がサイドウォール7と接することなく、ゲート電極5端部での高誘電率ゲート絶縁膜4Aの連続性が維持されている。

このため、ゲート電極5端部での高誘電率ゲート絶縁膜4Aの誘電率低下及び絶縁性低下を抑制することができるので、デバイス特性の低下やゲート絶縁膜信頼性の劣化を防止することができる。

【0035】

また、本実施形態によると、サイドウォール7の下側に高誘電率ゲート絶縁膜4Aが存在することによって、ゲート電極5端部近傍ではゲート電極5とn型エクステンション領域10との間の容量結合が強まり、その結果、高いゲート・ドレイン間オーバーラップ効果を得ることができる（非特許文献2）。従って、デバイス特性の向上及びホットキャリア信頼性の向上が同時に図れる。

【0036】

一方、本実施形態においては、サイドウォール7の下側に高誘電率ゲート絶縁膜4Aが存在することにより、特に、ゲート電極5とn型ソース・ドレイン領域12との間の容量の上昇が発生し、それによって回路速度の低下がもたらされる可能性がある。しかし、前述のように、本実施形態においては、サイドウォール7下側の高誘電率ゲート絶縁膜4Aをゲート電極5下側の高誘電率ゲート絶縁膜4Aよりも薄く形成しているため、ゲート・ドレイン間の容量の上昇ひいては回路速度への悪影響を抑制することができる。

【0037】

以上に説明したように、本実施形態によると、互いにトレードオフの関係にあるデバイス特性・回路特性とゲート絶縁膜信頼性とを共に大きく向上させることができる。

【0038】

（第1の実施形態の変形例）

以下、本発明の第1の実施形態の変形例に係る半導体装置について、図面を参照しながら説明する。図6は、第1の実施形態の変形例に係る半導体装置（具体的にはシングルサイドウォール型のn型MISFET）の構造を示す断面図である。

【0039】

本変形例が第1の実施形態と異なっている点は、図6に示すように、サイドウォール7の側端部の下側に位置する高誘電率ゲート絶縁膜4Aの一部つまり高誘電率ゲート絶縁膜4Aの側端部をノッチ状に取り除くことにより、ノッチ20が設けられていることである。

【0040】

本変形例によると、ゲート電極5とn型ソース・ドレイン領域12との間の容量の上昇に起因する回路速度への悪影響をより一層抑制することができる。

【0041】

（第2の実施形態）

以下、本発明の第2の実施形態に係る半導体装置について、図面を参照しながら説明する。尚、第1の実施形態がシングルサイドウォール型のMISFETを対象としていたのに対して、第2の実施形態は、ゲート電極とエクステンション領域との間のオーバーラップ量の最適化を図りやすいダブルサイドウォール型のMISFET（非特許文献3）を対象とする。尚、本実施形態ではn型MISFETを用いて説明するが、本発明をp型MISFETに適用した場合にも同様の効果を得ることができる。

【0042】

図2は、第2の実施形態に係る半導体装置の構造を示す断面図である。図2に示すように、例えばシリコンからなる基板1に形成されたp型ウェル2におけるSTI3によって囲まれた活性領域の上に高誘電率ゲート絶縁膜4Bを介してゲート電極5が形成されている。ゲート電極5の側面には絶縁性のオフセットサイドウォール6を介して絶縁性のサイドウォール7が形成されている。p型ウェル2におけるオフセットサイドウォール6及びサイドウォール7のそれぞれの下側にはn型エクステンション領域10が形成されていると共にp型ウェル2におけるn型エクステンション領域10の下側にはp型ポケット領域11が形成されている。p型ウェル2におけるゲート電極5から見てn型エクステンション領域10及びp型ポケット領域11の外側にはn型ソース・ドレイン領域12が形成さ

れている。

【0043】

本実施形態の第1の特徴は、ゲート電極5の下側のみならずオフセットサイドウォール6の下側にも高誘電率ゲート絶縁膜4Bが残存していることである。すなわち、高誘電率ゲート絶縁膜4Bはゲート電極5の下側からオフセットサイドウォール6の下側まで連続的に形成されている。

【0044】

また、本実施形態の第2の特徴は、高誘電率ゲート絶縁膜4Bにおけるオフセットサイドウォール6の下側領域の厚さは、高誘電率ゲート絶縁膜4Bにおけるゲート電極5の下側領域の厚さよりも小さいことである。すなわち、高誘電率ゲート絶縁膜4Bは凸形状に形成されている。

【0045】

本実施形態によると、高誘電率ゲート絶縁膜4Bの側端部がオフセットサイドウォール6と接することなく、ゲート電極5端部での高誘電率ゲート絶縁膜4Bの連続性が維持されている。このため、ゲート電極5端部での高誘電率ゲート絶縁膜4Bの誘電率低下及び絶縁性低下を抑制することができるので、デバイス特性の低下やゲート絶縁膜信頼性の劣化を防止することができる。

【0046】

また、本実施形態によると、オフセットサイドウォール6の下側に高誘電率ゲート絶縁膜4Bが存在することによって、ゲート電極5端部近傍ではゲート電極5とn型エクステンション領域10との間の容量結合が強まり、その結果、高いゲート・ドレイン間オーバーラップ効果を得ることができる（非特許文献2）。従って、デバイス特性の向上及びホットキャリア信頼性の向上が同時に図れる。

【0047】

さらに、本実施形態によると、サイドウォール7の下側には高誘電率ゲート絶縁膜4Bが存在しないため、ゲート電極5とn型ソース・ドレイン領域12との間の容量の上昇をさらに小さく抑えることができるので、寄生容量上昇とそれに伴う回路速度への悪影響を最小限に抑制することができる。

【0048】

以上に説明したように、本実施形態によると、互いにトレードオフの関係にあるデバイス特性・回路特性とゲート絶縁膜信頼性とを共に大きく向上させることができる。

【0049】

（第2の実施形態の第1変形例）

以下、本発明の第2の実施形態の第1変形例に係る半導体装置について、図面を参照しながら説明する。図7は、第2の実施形態の第1変形例に係る半導体装置（具体的にはダブルサイドウォール型のMISFET）の構造を示す断面図である。

【0050】

本変形例が第2の実施形態と異なっている点は、図7に示すように、オフセットサイドウォール6の側端部の下側に位置する高誘電率ゲート絶縁膜4Bの一部つまり高誘電率ゲート絶縁膜4Bの側端部をノッチ状に取り除くことにより、ノッチ20が設けられていることである。

【0051】

本変形例によると、ゲート電極5とn型ソース・ドレイン領域12との間の容量の上昇に起因する回路速度への悪影響をより一層抑制することができる。

【0052】

（第2の実施形態の第2変形例）

以下、本発明の第2の実施形態の第2変形例に係る半導体装置について、図面を参照しながら説明する。図3は、第2の実施形態の第2変形例に係る半導体装置（具体的にはダブルサイドウォール型のMISFET）の構造を示す断面図である。

【0053】

本変形例が第2の実施形態と異なっている点は、ゲート電極5の下側及びオフセットサイドウォール6の下側のみならずサイドウォール7の下側にも高誘電率ゲート絶縁膜4Cが残存していることである。すなわち、高誘電率ゲート絶縁膜4Cはゲート電極5の下側からサイドウォール7の下側まで連続的に形成されている。

【0054】

尚、本変形例において、サイドウォール7の下側の高誘電率ゲート絶縁膜4Cの膜厚は、オフセットサイドウォール6の下側の高誘電率ゲート絶縁膜4Cの膜厚と同じである。すなわち、高誘電率ゲート絶縁膜4Cは凸形状に形成されている。

【0055】

本変形例によると、高誘電率ゲート絶縁膜4Cがゲート電極5の下側からサイドウォール7の下側まで連続的に形成されているため、オフセットサイドウォール6の幅が非常に薄い場合にも、高誘電率ゲート絶縁膜4Cの側端部がサイドウォール7と接することなく、ゲート電極5端部での高誘電率ゲート絶縁膜4Cの連続性を維持することができる。このため、ゲート電極5端部での高誘電率ゲート絶縁膜4Cの誘電率低下及び絶縁性低下を抑制することができるので、デバイス特性の低下やゲート絶縁膜信頼性の劣化を防止することができる。

【0056】

但し、本変形例においては、第1の実施形態と同様にサイドウォール7の下側に高誘電率ゲート絶縁膜4Cが存在することにより、ゲート電極5とn型ソース・ドレイン領域12との間の容量の上昇が発生する可能性がある。しかし、前述のように、本変形例においては、サイドウォール7下側の高誘電率ゲート絶縁膜4Cをゲート電極5下側の高誘電率ゲート絶縁膜4Cよりも薄く形成しているため、寄生容量上昇及びそれに伴う回路速度への悪影響を抑制することができる。

【0057】

(第2の実施形態の第3変形例)

以下、本発明の第2の実施形態の第3変形例に係る半導体装置について、図面を参照しながら説明する。図4は、第2の実施形態の第3変形例に係る半導体装置（具体的にはダブルサイドウォール型のMISFET）の構造を示す断面図である。

【0058】

本変形例が第2の実施形態と異なっている第1の点は、ゲート電極5の下側及びオフセットサイドウォール6の下側のみならずサイドウォール7の下側にも高誘電率ゲート絶縁膜4Dが残存していることである。すなわち、高誘電率ゲート絶縁膜4Dはゲート電極5の下側からサイドウォール7の下側まで連続的に形成されている。

【0059】

本変形例が第2の実施形態と異なっている第2の点は、オフセットサイドウォール6の下側の高誘電率ゲート絶縁膜4Dの膜厚が、ゲート電極5の下側の高誘電率ゲート絶縁膜4Dの膜厚と同等であることである。尚、サイドウォール7の下側の高誘電率ゲート絶縁膜4Dの膜厚は、ゲート電極5の下側の高誘電率ゲート絶縁膜4Dの膜厚よりも小さい。すなわち、高誘電率ゲート絶縁膜4Dは凸形状に形成されている。

【0060】

本変形例によると、高誘電率ゲート絶縁膜4Dがゲート電極5の下側からサイドウォール7の下側まで連続的に形成されているため、オフセットサイドウォール6の幅が非常に薄い場合にも、高誘電率ゲート絶縁膜4Dの側端部がサイドウォール7と接することなく、ゲート電極5端部での高誘電率ゲート絶縁膜4Dの連続性を維持することができる。このため、ゲート電極5端部での高誘電率ゲート絶縁膜4Dの誘電率低下及び絶縁性低下を抑制することができるので、デバイス特性の低下やゲート絶縁膜信頼性の劣化を防止することができる。

【0061】

但し、本変形例においては、第1の実施形態と同様にサイドウォール7の下側に高誘電率ゲート絶縁膜4Dが存在することにより、ゲート電極5とn型ソース・ドレイン領域1

2との間の容量の上昇が発生する可能性がある。しかし、前述のように、本変形例においては、サイドウォール7下側の高誘電率ゲート絶縁膜4Dをゲート電極5下側の高誘電率ゲート絶縁膜4Dよりも薄く形成しているため、寄生容量上昇及びそれに伴う回路速度への悪影響を抑制することができる。

【0062】

(第3の実施形態)

以下、本発明の第3の実施形態に係る半導体装置について、図面を参照しながら説明する。尚、第1の実施形態がシングルサイドウォール型のMISFETを対象としていたのに対して、第3の実施形態は、ゲート電極とエクステンション領域との間のオーバーラップ量の最適化を図りやすいダブルサイドウォール型のMISFET（非特許文献3）を対象とする。尚、本実施形態ではn型MISFETを用いて説明するが、本発明をp型MISFETに適用した場合にも同様の効果を得ることができる。

【0063】

図5は、第3の実施形態に係る半導体装置の構造を示す断面図である。図5に示すように、例えばシリコンからなる基板1に形成されたp型ウェル2におけるSTI3によって囲まれた活性領域の上に高誘電率ゲート絶縁膜4Eを介してゲート電極5が形成されている。ゲート電極5の側面には絶縁性のオフセットサイドウォール6を介して絶縁性のサイドウォール7が形成されている。p型ウェル2におけるオフセットサイドウォール6及びサイドウォール7のそれぞれの下側にはn型エクステンション領域10が形成されていると共にp型ウェル2におけるn型エクステンション領域10の下側にはp型ポケット領域11が形成されている。p型ウェル2におけるゲート電極5から見てn型エクステンション領域10及びp型ポケット領域11の外側にはn型ソース・ドレイン領域12が形成されている。

【0064】

本実施形態の第1の特徴は、ゲート電極5の下側のみならずオフセットサイドウォール6及びサイドウォール7のそれぞれの下側にも高誘電率ゲート絶縁膜4Eが残存していることである。すなわち、高誘電率ゲート絶縁膜4Eはゲート電極5の下側からサイドウォール7の下側まで連続的に形成されている。

【0065】

また、本実施形態の第2の特徴は、高誘電率ゲート絶縁膜4Eにおけるオフセットサイドウォール6の下側領域の厚さが、高誘電率ゲート絶縁膜4Eにおけるゲート電極5の下側領域の厚さよりも小さく、且つ高誘電率ゲート絶縁膜4Eにおけるサイドウォール7の下側領域の厚さが、高誘電率ゲート絶縁膜4Eにおけるオフセットサイドウォール6の下側領域の厚さよりも小さいことである。すなわち、高誘電率ゲート絶縁膜4Eは2重凸形状に形成されている。

【0066】

本実施形態によると、高誘電率ゲート絶縁膜4Eがゲート電極5の下側からサイドウォール7の下側まで連続的に形成されているため、オフセットサイドウォール6の幅が非常に薄い場合にも、高誘電率ゲート絶縁膜4Eの側端部がサイドウォール7と接することなく、ゲート電極5端部での高誘電率ゲート絶縁膜4Eの連続性を維持することができる。このため、ゲート電極5端部での高誘電率ゲート絶縁膜4Eの誘電率低下及び絶縁性低下を抑制することができるので、デバイス特性の低下やゲート絶縁膜信頼性の劣化を防止することができる。

【0067】

また、本実施形態によると、オフセットサイドウォール6の下側に高誘電率ゲート絶縁膜4Eが存在することによって、ゲート電極5端部近傍ではゲート電極5とn型エクステンション領域10との間の容量結合が強まり、その結果、高いゲート・ドレイン間オーバーラップ効果を得ることができる（非特許文献2）。従って、デバイス特性の向上及びホットキャリア信頼性の向上が同時に図れる。

【0068】

一方、本実施形態においては、第1の実施形態と同様にサイドウォール7の下側に高誘電率ゲート絶縁膜4Eが存在することにより、ゲート電極5とn型ソース・ドレイン領域12との間の容量の上昇が発生し、その結果、回路速度の低下がもたらされる可能性がある。しかし、前述のように、本実施形態においては、オフセットサイドウォール6下側で高誘電率ゲート絶縁膜4Eの膜厚を一旦薄くし且つサイドウォール7下側で高誘電率ゲート絶縁膜4Eの膜厚をさらに薄くしているため、寄生容量上昇及びそれに伴う回路速度への悪影響を非常に低く抑制することができる。

【0069】

以上に説明したように、本実施形態によると、互いにトレードオフの関係にあるデバイス特性・回路特性とゲート絶縁膜信頼性とを共に大きく向上させることができる。

【0070】

(第3の実施形態の変形例)

以下、本発明の第3の実施形態の変形例に係る半導体装置について、図面を参照しながら説明する。図8は、第3の実施形態の変形例に係る半導体装置（具体的にはダブルサイドウォール型のMISFET）の構造を示す断面図である。

【0071】

本変形例が第3の実施形態と異なっている点は、図8に示すように、サイドウォール7の側端部の下側に位置する高誘電率ゲート絶縁膜4Eの一部、つまり高誘電率ゲート絶縁膜4Eの側端部をノッチ状に取り除くことにより、ノッチ20が設けられていることである。

【0072】

本変形例によると、ゲート電極5とn型ソース・ドレイン領域12との間の容量の上昇に起因する回路速度への悪影響をより一層抑制することができる。

【0073】

(第4の実施形態)

以下、本発明の第4の実施形態に係る半導体装置について、図面を参照しながら説明する。図9は、第4の実施形態に係る半導体装置（具体的にはシングルサイドウォール型のMISFET）の構造を示す断面図である。尚、本実施形態ではn型MISFETを用いて説明するが、本発明をp型MISFETに適用した場合にも同様の効果を得ることができる。

【0074】

本実施形態が第1の実施形態と異なっている点は、図9に示すように、基板1と高誘電率ゲート絶縁膜4Aとの間に、例えばシリコン酸化膜又はシリコン酸窒化膜等がバッファ絶縁膜25として設けられていることである。

【0075】

本実施形態によると、第1の実施形態の効果に加えて、基板・ゲート絶縁膜界面を正常に保つことができるという効果が得られる。すなわち、基板1上にバッファ絶縁膜25を介して高誘電率ゲート絶縁膜4Aを形成することによって、基板1上に高誘電率ゲート絶縁膜4Aを直接形成した場合と比べて、基板・ゲート絶縁膜界面の劣化を防止することができる。

【0076】

尚、本実施形態において、第1の実施形態の高誘電率ゲート絶縁膜4Aと基板1との間にバッファ絶縁膜25を設けた。しかし、これに代えて、第2の実施形態の高誘電率ゲート絶縁膜4B、第2の実施形態の第2変形例の高誘電率ゲート絶縁膜4C、第2の実施形態の第3変形例の高誘電率ゲート絶縁膜4D又は第3の実施形態の高誘電率ゲート絶縁膜4Eと基板1との間にバッファ絶縁膜25を設けても、本実施形態と同様の効果が得られる。また、高誘電率ゲート絶縁膜4A～4Eと基板1との間にバッファ絶縁膜25を設ける代わりに、ゲート電極5と高誘電率ゲート絶縁膜4A～4Eとの間にバッファ絶縁膜を設けてもよい。この構成によれば、高誘電率ゲート絶縁膜4A～4E上にゲート電極5を直接形成した場合と比べて、ゲート電極・ゲート絶縁膜界面の劣化を防止するこ

とができる。或いは、高誘電率ゲート絶縁膜4 A～4 Eと基板1との間にバッファ絶縁膜2 5を設けると共にゲート電極5と高誘電率ゲート絶縁膜4 A～4 Eとの間にバッファ絶縁膜を設けてもよい。この構成によれば、基板・ゲート絶縁膜界面及びゲート絶縁膜・ゲート電極界面の両方の劣化を防止することができる。

【0077】

(第4の実施形態の変形例)

以下、本発明の第4の実施形態の変形例に係る半導体装置について、図面を参照しながら説明する。図10は、第4の実施形態の変形例に係る半導体装置(具体的にはシングルサイドウォール型のMISFET)の構造を示す断面図である。

【0078】

本変形例が第4の実施形態と異なっている点は、図10に示すように、サイドウォール7の側端部の下側に位置する高誘電率ゲート絶縁膜4 A及びバッファ絶縁膜2 5の積層絶縁膜の一部、つまり当該積層絶縁膜の側端部をノッチ状に取り除くことにより、ノッチ20が設けられていることである。

【0079】

本変形例によると、ゲート電極5とn型ソース・ドレイン領域12との間の容量の上昇に起因する回路速度への悪影響をより一層抑制することができる。

【0080】

尚、本変形例において、第1の実施形態の高誘電率ゲート絶縁膜4 Aとバッファ絶縁膜2 5との積層絶縁膜の側端部にノッチ20を設けた。しかし、これに代えて、第2の実施形態の高誘電率ゲート絶縁膜4 B、第2の実施形態の第2変形例の高誘電率ゲート絶縁膜4 C、第2の実施形態の第3変形例の高誘電率ゲート絶縁膜4 D又は第3の実施形態の高誘電率ゲート絶縁膜4 Eのいずれかとバッファ絶縁膜2 5との積層絶縁膜の側端部にノッチを設けても、本変形例と同様の効果が得られる。このとき、高誘電率ゲート絶縁膜4 A～4 Eと基板1との間にバッファ絶縁膜2 5を設けると共に、ゲート電極5と高誘電率ゲート絶縁膜4 A～4 Eとの間にもバッファ絶縁膜を設けてもよい。

【0081】

(第5の実施形態)

以下、本発明の第5の実施形態に係る半導体装置の製造方法について、n型MISFETの製造方法を例として、図面を参照しながら説明する。図11(a)～(f)は、第5の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。

【0082】

まず、図11(a)に示すように、例えばシリコンからなる基板上1に、素子分離領域となるSTI3を選択的に形成した後、基板1に対して、例えばB(ボロン)を注入エネルギー300keV、ドーズ量 $1 \times 10^{13} \text{ cm}^{-2}$ の条件でイオン注入する。これにより、活性領域となるp型ウェル2が形成される。続いて、パンチスルーストップ形成用のイオン注入(注入イオン:B、注入エネルギー150keV、ドーズ量 $1 \times 10^{13} \text{ cm}^{-2}$)及びチャネル形成用のイオン注入(注入イオン:B、注入エネルギー20keV、ドーズ量 $5 \times 10^{12} \text{ cm}^{-2}$)を行う。

【0083】

次に、図11(b)に示すように、p型ウェル2におけるSTI3によって囲まれた活性領域の上に、バッファ絶縁膜として例えば膜厚0.5nm程度のシリコン酸化膜(図示省略)を形成した後、高誘電率ゲート絶縁膜4として例えば膜厚4nm程度のHfSiON膜(酸化膜換算膜厚は1nm程度)を堆積する。

【0084】

次に、図11(c)に示すように、高誘電率ゲート絶縁膜4上に例えば膜厚100nm程度のゲート電極材料膜5Aを形成する。

【0085】

次に、ゲート電極材料膜5A上にゲート電極形成領域を覆うレジストパターン(図示省略)を形成した後、当該レジストパターンをマスクとしてゲート電極材料膜5Aに対して

エッチングを行って、図11(d)に示すように、ゲート電極5を形成する。その後、ゲート電極5の外側に位置する高誘電率ゲート絶縁膜4を選択的エッチングによって膜厚2nm程度除去する。これにより、ゲート電極5の外側に位置する高誘電率ゲート絶縁膜4を残存膜厚2nm程度まで薄くすることができる。続いて、ゲート電極5をマスクとして基板1に対して、例えばAs(ヒ素)を注入エネルギー2keV、ドーズ量 $1 \times 10^{15} \text{ cm}^{-2}$ の条件でイオン注入することにより、n型エクステンション領域10を形成する。その後、ゲート電極5をマスクとして基板1に対して、例えばBを注入エネルギー10keV、ドーズ量 $3 \times 10^{13} \text{ cm}^{-2}$ の条件でイオン注入することにより、p型ポケット領域11を形成する。ここで、p型ポケット領域11を形成した後、n型エクステンション領域10を形成してもよい。

【0086】

次に、基板1の上に全面に亘って膜厚50nm程度の絶縁膜を堆積した後、当該絶縁膜に対してエッチバックを行って、図11(e)に示すように、ゲート電極5の側面に絶縁性のサイドウォール7を形成する。

【0087】

次に、ゲート電極5及びサイドウォール7をマスクとして基板1に対して、例えばAsを注入エネルギー10keV、ドーズ量 $5 \times 10^{15} \text{ cm}^{-2}$ の条件でイオン注入した後、例えば1050℃程度の温度でSPIKE RTA(rapid thermal annealing)を行い、注入不純物を活性化する。これにより、図11(f)に示すように、n型ソース・ドレイン領域12が形成される。

【0088】

以上に説明した本実施形態の製造方法によると、第1の実施形態のMISFET構造(図1参照)を比較的簡単に実現することができる。

【0089】

ところで、高誘電率ゲート絶縁膜4は重金属を含んでいるため、高誘電率ゲート絶縁膜4を通過する注入イオンのRp(Projection Range)は小さくなりやすい。従って、図11(d)に示す工程において、n型エクステンション領域10又はp型ポケット領域11を形成するために、ゲート電極5の外側において高誘電率ゲート絶縁膜4に覆われた基板1に対してイオン注入する際には、加速エネルギーを大きくする必要がある。しかし、本実施形態ではゲート電極5の外側の高誘電率ゲート絶縁膜4が薄膜化されているため、加速エネルギーの増大を抑制できるので、n型エクステンション領域10において浅い接合を容易に形成でき、それによりデバイス特性の向上を図りやすい。

【0090】

尚、本実施形態において、サイドウォール7の形成後に、サイドウォール7の外側に位置する高誘電率ゲート絶縁膜4を、例えばフッ酸を用いたウェットエッチング又は選択ドライエッチングによって除去してもよい。このとき、ウェットエッチングを用いる場合には、サイドウォール7の側端部の下側に位置する高誘電率ゲート絶縁膜4の一部、つまり高誘電率ゲート絶縁膜4の側端部をノッチ状に取り除いてノッチを設けてもよい。このようにすると、第1の実施形態の変形例のMISFET構造(図6参照)を簡単に実現することができる。

【0091】

また、本実施形態において、ゲート電極5の外側における高誘電率ゲート絶縁膜4の薄膜化の程度は特に限定されるものではないが、高誘電率ゲート絶縁膜4として例えばHfSiON膜を用いる場合、ゲート・ドレイン間の容量の上昇を抑制するためには、ゲート電極5の外側の高誘電率ゲート絶縁膜4を膜厚2nm程度以下に薄膜化する(但し基板1の表面が露出しないように)ことが好ましい。

【0092】

(第6の実施形態)

以下、本発明の第6の実施形態に係る半導体装置の製造方法について、n型MISFETの製造方法を例として、図面を参照しながら説明する。図12(a)～(g)は、第6

の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。

【0093】

まず、図12(a)に示すように、例えばシリコンからなる基板上1に、素子分離領域となるSTI3を選択的に形成した後、基板1に対して、例えばBを注入エネルギー300keV、ドーズ量 $1 \times 10^{13} \text{ cm}^{-2}$ の条件でイオン注入する。これにより、活性領域となるp型ウェル2が形成される。続いて、パンチスルーストップパ形成用のイオン注入（注入イオン：B、注入エネルギー150keV、ドーズ量 $1 \times 10^{13} \text{ cm}^{-2}$ ）及びチャネル形成用のイオン注入（注入イオン：B、注入エネルギー20keV、ドーズ量 $5 \times 10^{12} \text{ cm}^{-2}$ ）を行う。

【0094】

次に、図12(b)に示すように、p型ウェル2におけるSTI3によって囲まれた活性領域の上に、バッファ絶縁膜として例えば膜厚0.5nm程度のシリコン酸化膜（図示省略）を形成した後、高誘電率ゲート絶縁膜4として例えば膜厚4nm程度のHfSiON膜（酸化膜換算膜厚は1nm程度）を堆積する。

【0095】

次に、図12(c)に示すように、高誘電率ゲート絶縁膜4上に例えば膜厚100nm程度のゲート電極材料膜5Aを形成する。

【0096】

次に、ゲート電極材料膜5A上にゲート電極形成領域を覆うレジストパターン（図示省略）を形成した後、当該レジストパターンをマスクとしてゲート電極材料膜5Aに対してエッチングを行って、図12(d)に示すように、ゲート電極5を形成する。その後、ゲート電極5の外側に位置する高誘電率ゲート絶縁膜4を選択的エッチングによって膜厚2nm程度除去する。これにより、ゲート電極5の外側の高誘電率ゲート絶縁膜4を残存膜厚2nm程度まで薄くすることができる。

【0097】

次に、基板1の上に全面に亘って膜厚10nm程度の絶縁膜を堆積した後、当該絶縁膜に対してエッチバックを行って、図12(e)に示すように、ゲート電極5の側面にオフセットサイドウォール6を形成する。その後、オフセットサイドウォール6の外側に位置する高誘電率ゲート絶縁膜4を、例えばフッ酸を用いたウェットエッチング又は選択ドライエッチングによって除去する。続いて、ゲート電極5及びオフセットサイドウォール6をマスクとして基板1に対して、例えばAsを注入エネルギー2keV、ドーズ量 $1 \times 10^{15} \text{ cm}^{-2}$ の条件でイオン注入することにより、n型エクステンション領域10を形成する。その後、ゲート電極5及びオフセットサイドウォール6をマスクとして基板1に対して、例えばBを注入エネルギー10keV、ドーズ量 $3 \times 10^{13} \text{ cm}^{-2}$ の条件でイオン注入することにより、p型ポケット領域11を形成する。

【0098】

次に、基板1の上に全面に亘って膜厚50nm程度の絶縁膜を堆積した後、当該絶縁膜に対してエッチバックを行って、図12(f)に示すように、ゲート電極5の側面にオフセットサイドウォール6を介して絶縁性のサイドウォール7を形成する。

【0099】

次に、ゲート電極5、オフセットサイドウォール6及びサイドウォール7をマスクとして基板1に対して、例えばAsを注入エネルギー10keV、ドーズ量 $5 \times 10^{15} \text{ cm}^{-2}$ の条件でイオン注入した後、例えば1050℃程度の温度でSPIKE RTAを行い、注入不純物を活性化する。これにより、図12(g)に示すように、n型ソース・ドレイン領域12が形成される。

【0100】

以上に説明した本実施形態の製造方法によると、第2の実施形態のMISFET構造（図2参照）を比較的簡単に実現することができる。

【0101】

尚、本実施形態において、オフセットサイドウォール6の形成後に、オフセットサイド

ウォール6の外側に位置する高誘電率ゲート絶縁膜4を、例えばフッ酸を用いたウェットエッチングによって除去する際に、オフセットサイドウォール6の側端部の下側に位置する高誘電率ゲート絶縁膜4の一部、つまり高誘電率ゲート絶縁膜4の側端部をノッチ状に取り除いてノッチを設けてもよい。このようにすると、第2の実施形態の第1変形例のMISFET構造(図7参照)を簡単に実現することができる。

【0102】

また、本実施形態において、ゲート電極5の外側における高誘電率ゲート絶縁膜4の薄膜化の程度は特に限定されるものではないが、高誘電率ゲート絶縁膜4として例えばHfSiON膜を用いる場合、ゲート・ドレイン間の容量の上昇を抑制するためには、ゲート電極5の外側の高誘電率ゲート絶縁膜4を膜厚2nm程度以下に薄膜化する(但し基板1の表面が露出しないように)ことが好ましい。

【0103】

また、本実施形態において、オフセットサイドウォール6を形成した後、オフセットサイドウォール6の外側に位置する高誘電率ゲート絶縁膜4を除去し、その後、n型エクステンション領域10及びp型ポケット領域11を形成するためのイオン注入を行った。しかし、これに代えて、オフセットサイドウォール6を形成した後、オフセットサイドウォール6の外側に薄膜化した高誘電率ゲート絶縁膜4を残存させた状態でn型エクステンション領域10及びp型ポケット領域11を形成するためのイオン注入を行ってもよい。このようにしても、本実施形態ではオフセットサイドウォール6の外側に位置する高誘電率ゲート絶縁膜4が薄膜化されているため、加速エネルギーの増大を抑制できるので、n型エクステンション領域10において浅い接合を容易に形成でき、それによりデバイス特性の向上を図りやすい。また、この場合、n型エクステンション領域10及びp型ポケット領域11を形成するためのイオン注入を行った後、オフセットサイドウォール6の外側に位置する高誘電率ゲート絶縁膜4を除去し、その後、同一基板上における他のチャンネル型又は別の電源系のMISFETのエクステンション領域及びポケット領域を形成するためのイオン注入を行ってもよい。

【0104】

(第7の実施形態)

以下、本発明の第7の実施形態に係る半導体装置の製造方法について、n型MISFETの製造方法を例として、図面を参照しながら説明する。図13(a)～(g)は、第7の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。

【0105】

まず、図13(a)に示すように、例えばシリコンからなる基板上1に、素子分離領域となるSTI3を選択的に形成した後、基板1に対して、例えばBを注入エネルギー300keV、ドーズ量 $1 \times 10^{13} \text{ cm}^{-2}$ の条件でイオン注入する。これにより、活性領域となるp型ウェル2が形成される。続いて、パンチスルーストップパ形成用のイオン注入(注入イオン:B、注入エネルギー150keV、ドーズ量 $1 \times 10^{13} \text{ cm}^{-2}$)及びチャンネル形成用のイオン注入(注入イオン:B、注入エネルギー20keV、ドーズ量 $5 \times 10^{12} \text{ cm}^{-2}$)を行う。

【0106】

次に、図13(b)に示すように、p型ウェル2におけるSTI3によって囲まれた活性領域の上に、バッファ絶縁膜として例えば膜厚0.5nm程度のシリコン酸化膜(図示省略)を形成した後、高誘電率ゲート絶縁膜4として例えば膜厚4nm程度のHfSiON膜(酸化膜換算膜厚は1nm程度)を堆積する。

【0107】

次に、図13(c)に示すように、高誘電率ゲート絶縁膜4上に例えば膜厚100nm程度のゲート電極材料膜5Aを形成する。

【0108】

次に、ゲート電極材料膜5A上にゲート電極形成領域を覆うレジストパターン(図示省略)を形成した後、当該レジストパターンをマスクとしてゲート電極材料膜5Aに対して

エッチングを行って、図13(d)に示すように、ゲート電極5を形成する。その後、ゲート電極5の外側に位置する高誘電率ゲート絶縁膜4を選択的エッチングによって膜厚2 nm程度除去する。これにより、ゲート電極5の外側の高誘電率ゲート絶縁膜4を残存膜厚2 nm程度まで薄くすることができる。

【0109】

次に、基板1の上に全面に亘って膜厚5 nm程度の絶縁膜を堆積した後、当該絶縁膜に対してエッチバックを行って、図13(e)に示すように、ゲート電極5の側面に絶縁性のオフセットサイドウォール6を形成する。その後、ゲート電極5及びオフセットサイドウォール6により被覆されていない高誘電率ゲート絶縁膜4をさらに膜厚1 nm程度除去する。これにより、オフセットサイドウォール6の外側に位置する高誘電率ゲート絶縁膜4を残存膜厚1 nm程度まで薄くすることができる。その後、ゲート電極5及びオフセットサイドウォール6をマスクとして基板1に対して、例えばAsを注入エネルギー2 keV、ドーズ量 $1 \times 10^{15} \text{ cm}^{-2}$ の条件でイオン注入することにより、n型エクステンション領域10を形成する。その後、ゲート電極5及びオフセットサイドウォール6をマスクとして基板1に対して、例えばBを注入エネルギー10 keV、ドーズ量 $3 \times 10^{13} \text{ cm}^{-2}$ の条件でイオン注入することにより、p型ポケット領域11を形成する。

【0110】

次に、基板1の上に全面に亘って膜厚50 nm程度の絶縁膜を堆積した後、当該絶縁膜に対してエッチバックを行って、図13(f)に示すように、ゲート電極5の側面にオフセットサイドウォール6を介して絶縁性のサイドウォール7を形成する。

【0111】

次に、ゲート電極5、オフセットサイドウォール6及びサイドウォール7をマスクとして基板1に対して、例えばAsを注入エネルギー10 keV、ドーズ量 $5 \times 10^{15} \text{ cm}^{-2}$ の条件でイオン注入した後、例えば1050℃程度の温度でSPIKE RTAを行い、注入不純物を活性化する。これにより、図13(g)に示すように、n型ソース・ドレイン領域12が形成される。

【0112】

以上に説明した本実施形態の製造方法によると、第3の実施形態のMISFET構造(図5参照)を比較的簡単に実現することができる。

【0113】

また、本実施形態においては、オフセットサイドウォール6下側で高誘電率ゲート絶縁膜4Eの膜厚を一旦薄くし且つオフセットサイドウォール6の外側の高誘電率ゲート絶縁膜4Eの膜厚をさらに薄くしている。このため、ゲート電極5及びオフセットサイドウォール6をマスクとして、n型エクステンション領域10を形成するためのイオン注入を行う際にも、加速エネルギーの増大を最小限に抑制できるので、n型エクステンション領域10においてさらに浅い接合を容易に形成でき、それによりデバイス特性の向上を図りやすい。

【0114】

尚、本実施形態において、サイドウォール7の形成後に、サイドウォール7の外側に位置する高誘電率ゲート絶縁膜4を、例えばフッ酸を用いたウェットエッチング又は選択ドライエッチングによって除去してもよい。また、この際に、サイドウォール7端部の高誘電率ゲート絶縁膜4つまり高誘電率ゲート絶縁膜4の側端部をノッチ状に取り除いてもよい。このようにすると、第3の実施形態の変形例のMISFET構造(図8参照)を簡単に実現することができる。

【0115】

また、本実施形態において、ゲート電極5の外側における高誘電率ゲート絶縁膜4の薄膜化の程度は、オフセットサイドウォール6の下側においてもサイドウォール7の下側においても特に限定されるものではない。しかし、高誘電率ゲート絶縁膜4として例えばHfSiON膜を用いる場合、ゲート・ドレイン間の容量の上昇を抑制するためには、ゲート電極5の外側の高誘電率ゲート絶縁膜4を膜厚2 nm程度以下に薄膜化することが好ま

しい。

【0116】

(第8の実施形態)

以下、本発明の第8の実施形態に係る半導体装置の製造方法について、n型MISFETの製造方法を例として、図面を参照しながら説明する。図14(a)～(g)及び図15(a)～(d)は、第8の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。

【0117】

まず、図14(a)に示すように、例えばシリコンからなる基板1に、素子分離領域となるSTI3を選択的に形成した後、基板1に対して、例えばBを注入エネルギー300keV、ドーズ量 $1 \times 10^{13} \text{ cm}^{-2}$ の条件でイオン注入する。これにより、活性領域となるp型ウェル2が形成される。続いて、パンチスルーストップパ形成用のイオン注入(注入イオン:B、注入エネルギー150keV、ドーズ量 $1 \times 10^{13} \text{ cm}^{-2}$)及びチャネル形成用のイオン注入(注入イオン:B、注入エネルギー20keV、ドーズ量 $5 \times 10^{12} \text{ cm}^{-2}$)を行う。

【0118】

次に、図14(b)に示すように、p型ウェル2におけるSTI3によって囲まれた活性領域の上に、バッファ絶縁膜として例えば膜厚0.5nm程度のシリコン酸化膜(図示省略)を形成した後、高誘電率ゲート絶縁膜4として例えば膜厚4nm程度のHfSiON膜(酸化膜換算膜厚は1nm程度)を堆積する。

【0119】

次に、図14(c)に示すように、高誘電率ゲート絶縁膜4上にゲート電極材料膜5Aとして例えば膜厚100nm程度のポリシリコン膜を形成した後、ゲート電極材料膜5Aの上にカバー膜(保護膜)15として例えば膜厚10nm程度のシリコン酸化膜を堆積する。

【0120】

次に、カバー膜15上にゲート電極形成領域を覆うレジストパターン(図示省略)を形成した後、当該レジストパターンをマスクとしてカバー膜15及びゲート電極材料膜5Aに対して順次エッチングを行って、図14(d)に示すように、カバー膜15により上面が覆われたゲート電極5を形成する。その後、ゲート電極5の外側に位置する高誘電率ゲート絶縁膜4を選択的エッチングによって膜厚2nm程度除去する。これにより、ゲート電極5の外側の高誘電率ゲート絶縁膜4を残存膜厚2nm程度まで薄くすることができる。

【0121】

次に、基板1の上に全面に亘って膜厚10nm程度の絶縁膜を堆積した後、当該絶縁膜に対してエッチバックを行って、図14(e)に示すように、ゲート電極5の側面にオフセットサイドウォール6を形成する。その後、オフセットサイドウォール6の外側に位置する高誘電率ゲート絶縁膜4を、例えばフッ酸を用いたウェットエッチング又は選択ドライエッチングによって除去する。続いて、ゲート電極5及びオフセットサイドウォール6をマスクとして基板1に対して、例えばAsを注入エネルギー2keV、ドーズ量 $1 \times 10^{15} \text{ cm}^{-2}$ の条件でイオン注入することにより、n型エクステンション領域10を形成する。その後、ゲート電極5及びオフセットサイドウォール6をマスクとして基板1に対して、例えばBを注入エネルギー10keV、ドーズ量 $3 \times 10^{13} \text{ cm}^{-2}$ の条件でイオン注入することにより、p型ポケット領域11を形成する。

【0122】

次に、基板1の上に全面に亘って膜厚50nm程度の絶縁膜(例えばSiN膜)を堆積した後、当該絶縁膜に対してエッチバックを行って、図14(f)に示すように、ゲート電極5の側面にオフセットサイドウォール6を介して絶縁性のサイドウォール7を形成する。

【0123】

次に、ゲート電極5、オフセットサイドウォール6及びサイドウォール7をマスクとして基板1に対して、例えばAsを注入エネルギー10keV、ドーズ量 $5 \times 10^{15} \text{ cm}^{-2}$ の条件でイオン注入した後、例えば1050℃程度の温度でSPIKE RTAを行い、注入不純物を活性化する。これにより、図14(g)に示すように、n型ソース・ドレイン領域12が形成される。

【0124】

次に、基板1の上に全面に亘って膜厚10nm程度の金属膜（例えばNi膜）を堆積した後、RTAを実施することにより基板1の露出部分と金属膜とを反応させ、それによって、図15(a)に示すように、n型ソース・ドレイン領域12上にシリサイド層13を形成する。その後、基板1上に残留する未反応の金属膜を剥離・除去する。

【0125】

次に、図15(b)に示すように、ゲート電極5の上を含む基板1の上に全面に亘って例えば膜厚400nm程度の層間絶縁膜14を堆積する。

【0126】

次に、図15(c)に示すように、例えばCMP (chemical mechanical polishing) によって層間絶縁膜14を、その表面がカバー膜15の上面と面一になるまで削った後、当該露出したカバー膜15をエッチングにより除去する。このとき、CMP後の層間絶縁膜14の上部及びオフセットサイドウォール6の上部も除去される。

【0127】

次に、基板1の上に全面に亘って膜厚100nm程度の金属膜（例えばNi膜）を堆積した後、RTAを実施することによりゲート電極5の露出部分と金属膜とを反応させ、それによって、図15(d)に示すように、フルシリサイド化されたゲート電極16（高誘電率ゲート絶縁膜4上の全領域がシリサイド化されたゲート電極16）を形成する。

【0128】

以上に説明した本実施形態の製造方法によると、FUSI (full silicide) 構造を用いた第2の実施形態のMISFET構造（図2参照）を比較的簡単に実現することができる。

【0129】

尚、本実施形態において、オフセットサイドウォール6の形成後に、オフセットサイドウォール6の外側に位置する高誘電率ゲート絶縁膜4を、例えばフッ酸を用いたウェットエッチングによって除去する際に、オフセットサイドウォール6の側端部の下側に位置する高誘電率ゲート絶縁膜4の一部、つまり高誘電率ゲート絶縁膜4の側端部をノッチ状に取り除いてノッチを設けてもよい。このようにすると、FUSI構造を用いた第2の実施形態の第1変形例のMISFET構造（図7参照）を簡単に実現することができる。

【0130】

また、本実施形態において、ゲート電極5の外側における高誘電率ゲート絶縁膜4の薄膜化の程度は特に限定されるものではないが、高誘電率ゲート絶縁膜4として例えばHfSiON膜を用いる場合、ゲート・ドレイン間の容量の上昇を抑制するためには、ゲート電極5の外側の高誘電率ゲート絶縁膜4を膜厚2nm程度以下に薄膜化する（但し基板1の表面が露出しないように）ことが好ましい。

【0131】

また、本実施形態において、オフセットサイドウォール6を形成した後、オフセットサイドウォール6の外側の高誘電率ゲート絶縁膜4を除去し、その後、n型エクステンション領域10及びp型ポケット領域11を形成するためのイオン注入を行った。しかし、これに代えて、オフセットサイドウォール6を形成した後、オフセットサイドウォール6の外側に薄膜化した高誘電率ゲート絶縁膜4を残存させた状態でn型エクステンション領域10及びp型ポケット領域11を形成するためのイオン注入を行ってもよい。このようにしても、本実施形態ではゲート電極5の外側に位置する高誘電率ゲート絶縁膜4が薄膜化されているため、加速エネルギーの増大を抑制できるので、n型エクステンション領域10において浅い接合を容易に形成でき、それによりデバイス特性の向上を図りやすい。ま

た、この場合、n型エクステンション領域10及びp型ポケット領域11を形成するためのイオン注入を行った後、オフセットサイドウォール6外側に位置する高誘電率ゲート絶縁膜4を除去し、その後、同一基板上における他のチャンネル型又は別の電源系のMISFETのエクステンション領域及びポケット領域を形成するためのイオン注入を行ってもよい。

【0132】

また、本実施形態において、FUSI構造を用いた第2の実施形態のMISFET構造を形成したが、これに代えて、第1の実施形態若しくはその変形例、第2の実施形態の各変形例、第3の実施形態若しくはその変形例、又は第4の実施形態若しくはその変形例のMISFET構造をFUSI構造を用いて形成してもよい。

【0133】

また、第1～第8の実施形態において、サイドウォール7として例えばSiN膜の1層構造を用いたが、これに代えて、例えば酸化膜(SiO₂膜)と窒化膜(SiN膜)とを組み合わせた2層構造(例えば下層SiO₂膜と上層SiN膜)又は3層構造(例えば下層SiO₂膜と中層SiN膜と上層SiO₂膜)等を用いてもよい。

【0134】

また、第1～第8の実施形態において、n型エクステンション領域10に代えてLDDを形成してもよい。

【0135】

また、第5～第8の実施形態において、n型MISFETに代えてp型MISFETを形成してもよい。

【0136】

また、第5～第8の実施形態において、ゲート絶縁膜・ゲート電極界面の劣化を防止するために、ゲート電極5と高誘電率ゲート絶縁膜4との間に例えば膜厚0.2nm程度のバッファ絶縁膜を形成してもよい。

【0137】

また、第1～第8の実施形態において、サイドウォール7又はオフセットサイドウォール6の端部下側にノッチ20が設けられた高誘電率ゲート絶縁膜4の側面形状は、図6、図7、図8又は図10に示すような半円形状に限定されるものではない。例えば高誘電率ゲート絶縁膜4の側面形状は基板面に対して垂直な形状でもよい。すなわち、高誘電率ゲート絶縁膜4の側面は、サイドウォール7又はオフセットサイドウォール6の側端面からゲート電極5側に所定の距離だけ入り込んだ位置にあってもよい。

【産業上の利用可能性】

【0138】

以上に説明したように、本発明は、半導体装置及びその製造方法に関し、特に高誘電率ゲート絶縁膜を有するMISFETに適用した場合には、MISFETの駆動力及び信頼性を向上させることができるという効果が得られ、非常に有用である。

【図面の簡単な説明】

【0139】

【図1】図1は本発明の第1の実施形態に係る半導体装置の構造を示す断面図である。

【図2】図2は本発明の第2の実施形態に係る半導体装置の構造を示す断面図である。

【図3】図3は本発明の第2の実施形態の第2変形例に係る半導体装置の構造を示す断面図である。

【図4】図4は本発明の第2の実施形態の第3変形例に係る半導体装置の構造を示す断面図である。

【図5】図5は本発明の第3の実施形態に係る半導体装置の構造を示す断面図である。

【図6】図6は本発明の第1の実施形態の変形例に係る半導体装置の構造を示す断面

図である。

【図 7】図 7 は本発明の第 2 の実施形態の第 1 変形例に係る半導体装置の構造を示す断面図である。

【図 8】図 8 は本発明の第 3 の実施形態の変形例に係る半導体装置の構造を示す断面図である。

【図 9】図 9 は本発明の第 4 の実施形態に係る半導体装置の構造を示す断面図である。

【図 10】図 10 は本発明の第 4 の実施形態の変形例に係る半導体装置の構造を示す断面図である。

【図 11】図 11 (a) ～ (f) は本発明の第 5 の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。

【図 12】図 12 (a) ～ (g) は本発明の第 6 の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。

【図 13】図 13 (a) ～ (g) は本発明の第 7 の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。

【図 14】図 14 (a) ～ (g) は本発明の第 8 の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。

【図 15】図 15 (a) ～ (d) は本発明の第 8 の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。

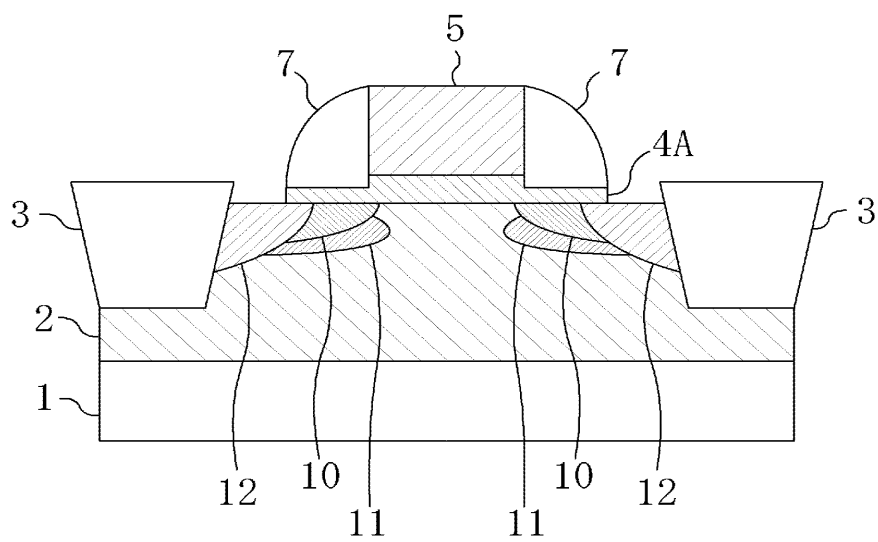
【図 16】図 16 (a) 及び (b) はそれぞれ従来の M I S F E T の構造を示す断面図である。

【符号の説明】

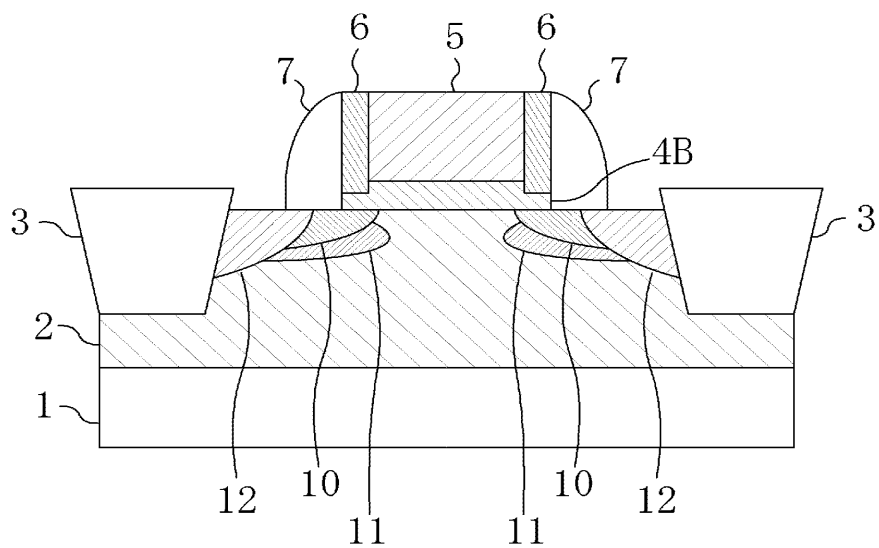
【0 1 4 0】

- 1 基板
- 2 p 型ウェル
- 3 S T I
- 4 (4 A ～ 4 E) 高誘電率ゲート絶縁膜
- 5 A ゲート電極材料膜
- 5 ゲート電極
- 6 オフセットサイドウォール
- 7 サイドウォール
- 10 n 型エクステンション領域
- 11 p 型ポケット領域
- 12 n 型ソース・ドレイン領域
- 13 シリサイド層
- 14 層間絶縁膜
- 15 カバー膜
- 16 フルシリサイド化されたゲート電極
- 20 ノッチ
- 25 バッファ絶縁膜

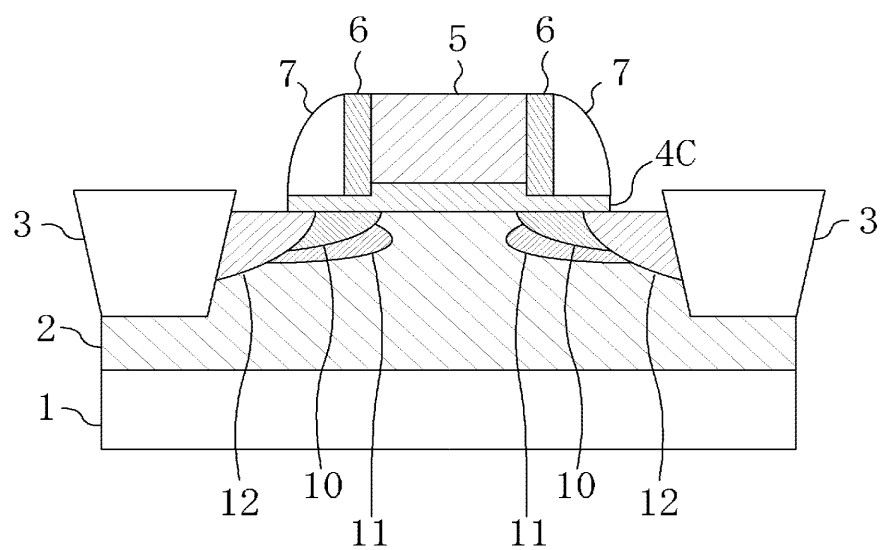
【図 1】



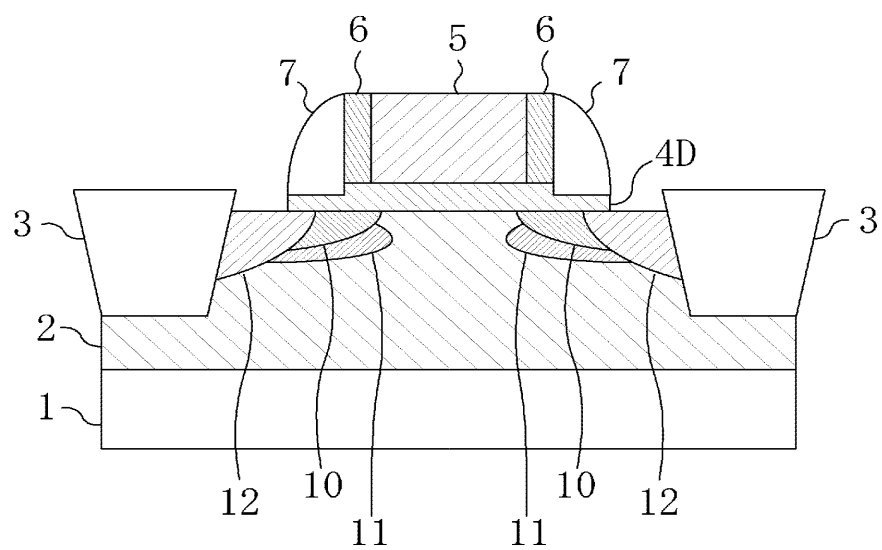
【图 2】



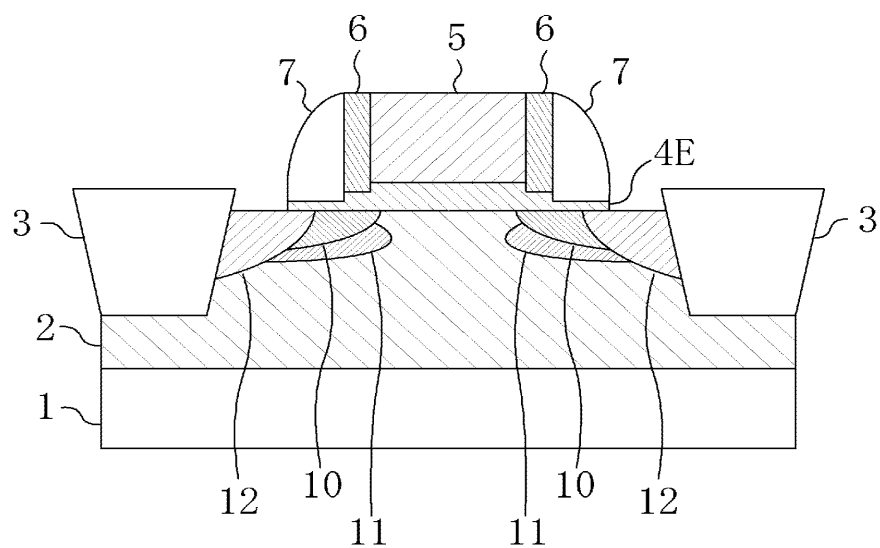
【図3】



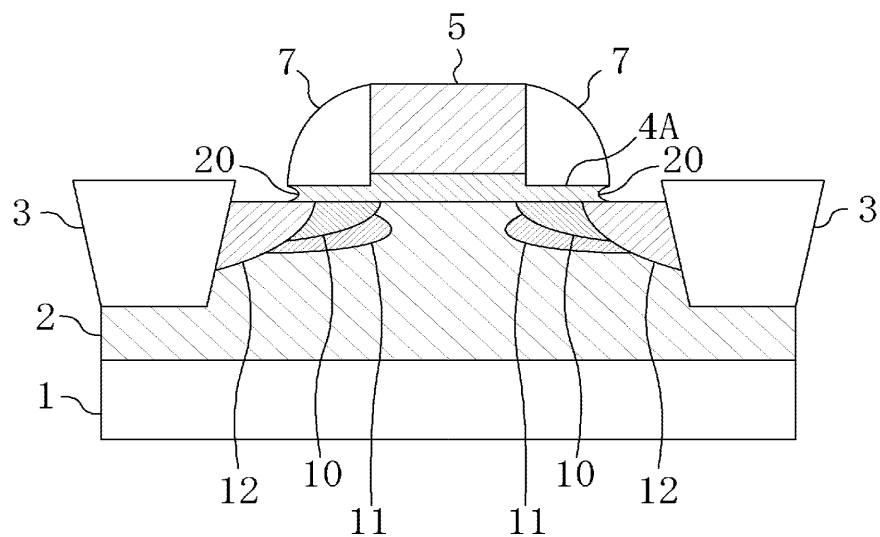
【図4】



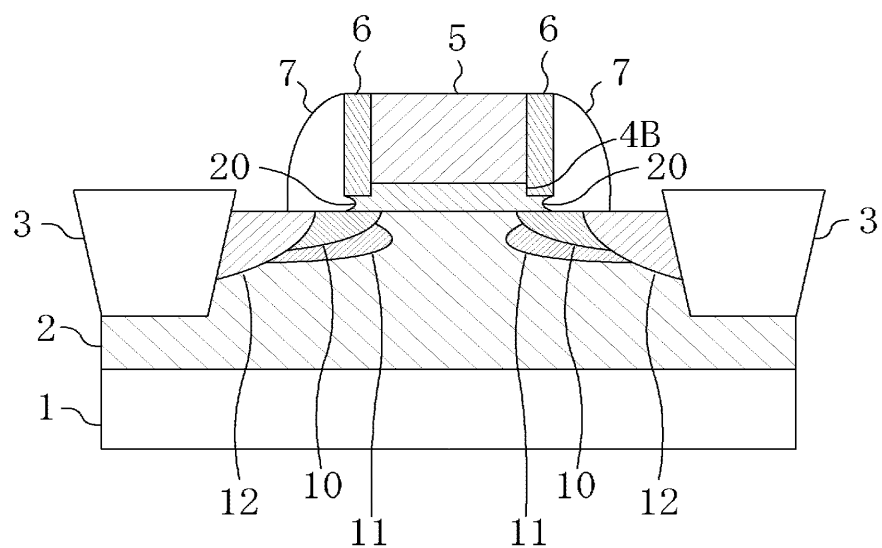
【図5】



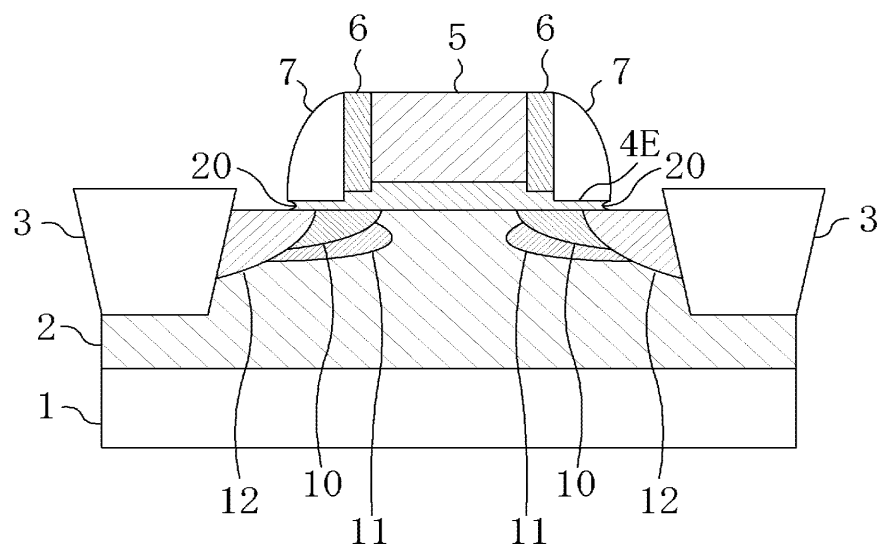
【図6】



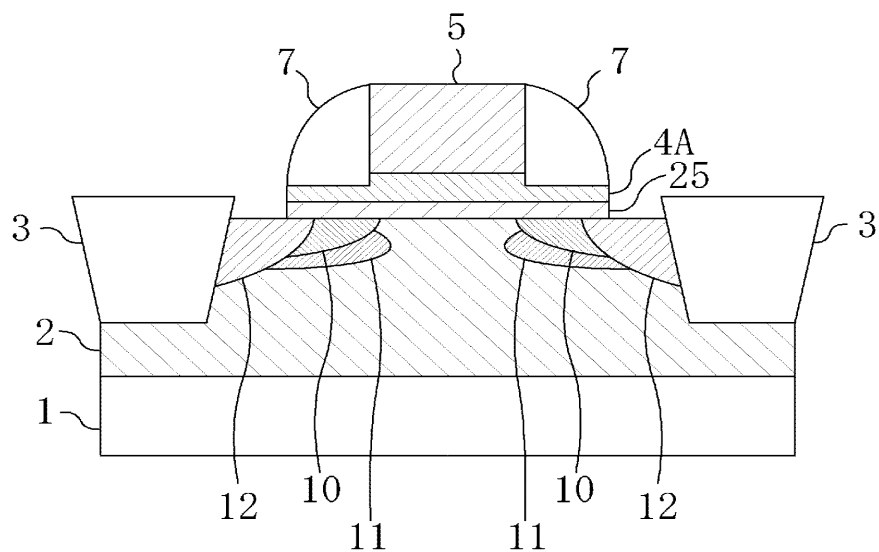
【図7】



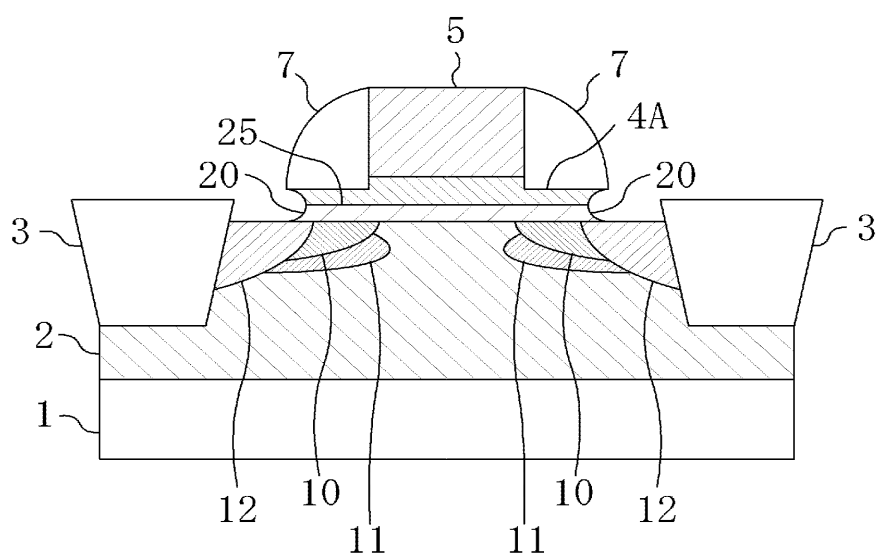
【図8】



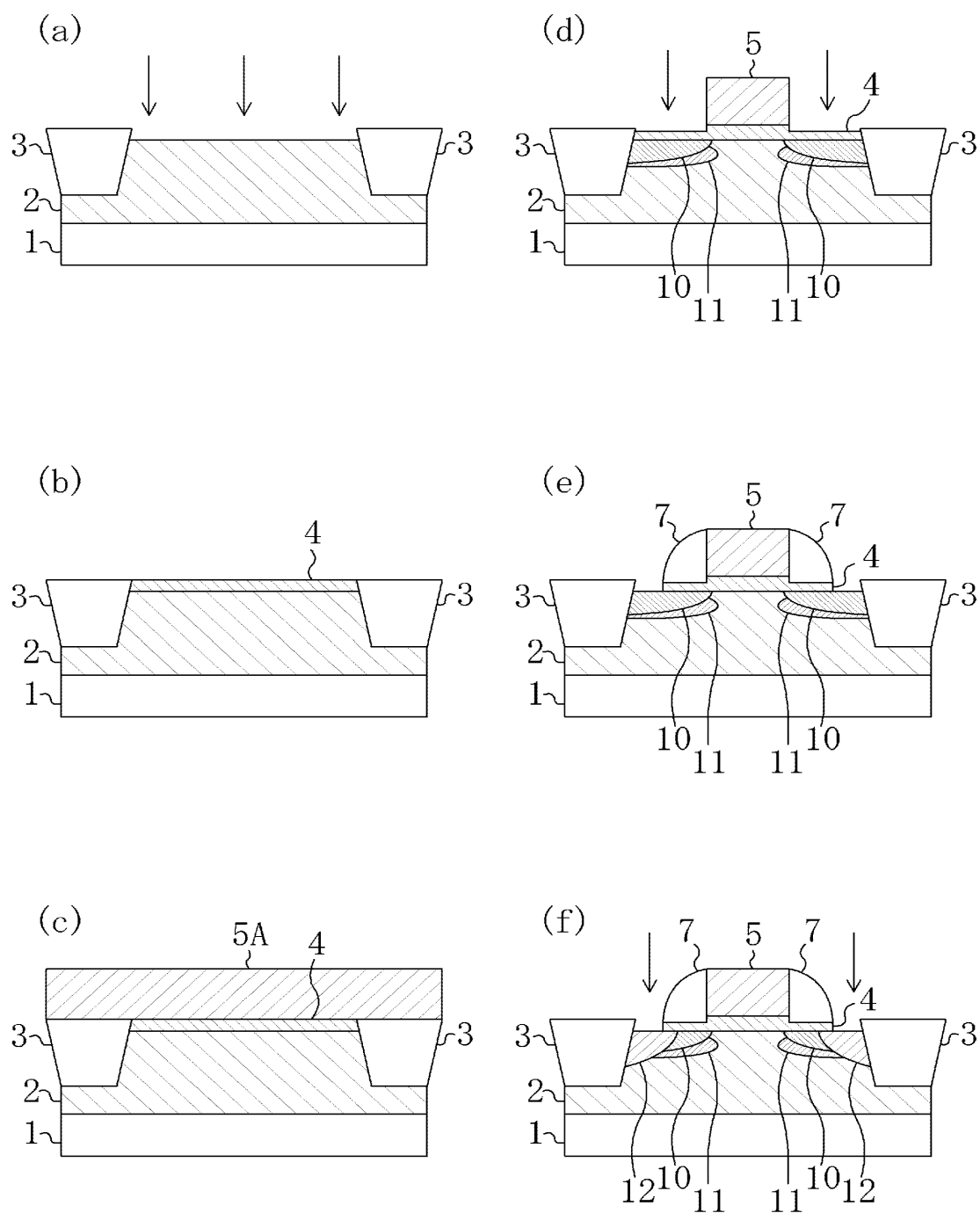
【図9】



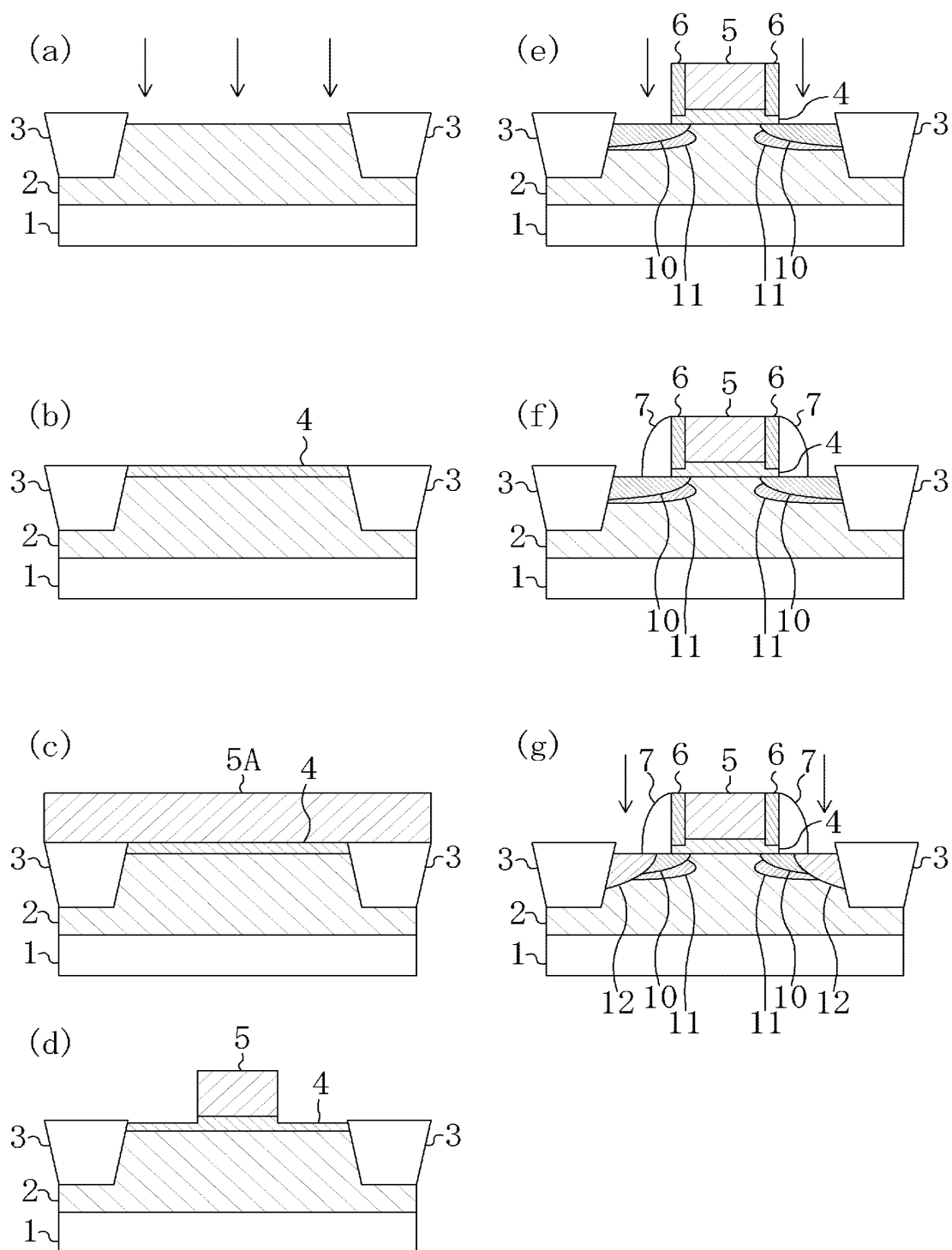
【図10】



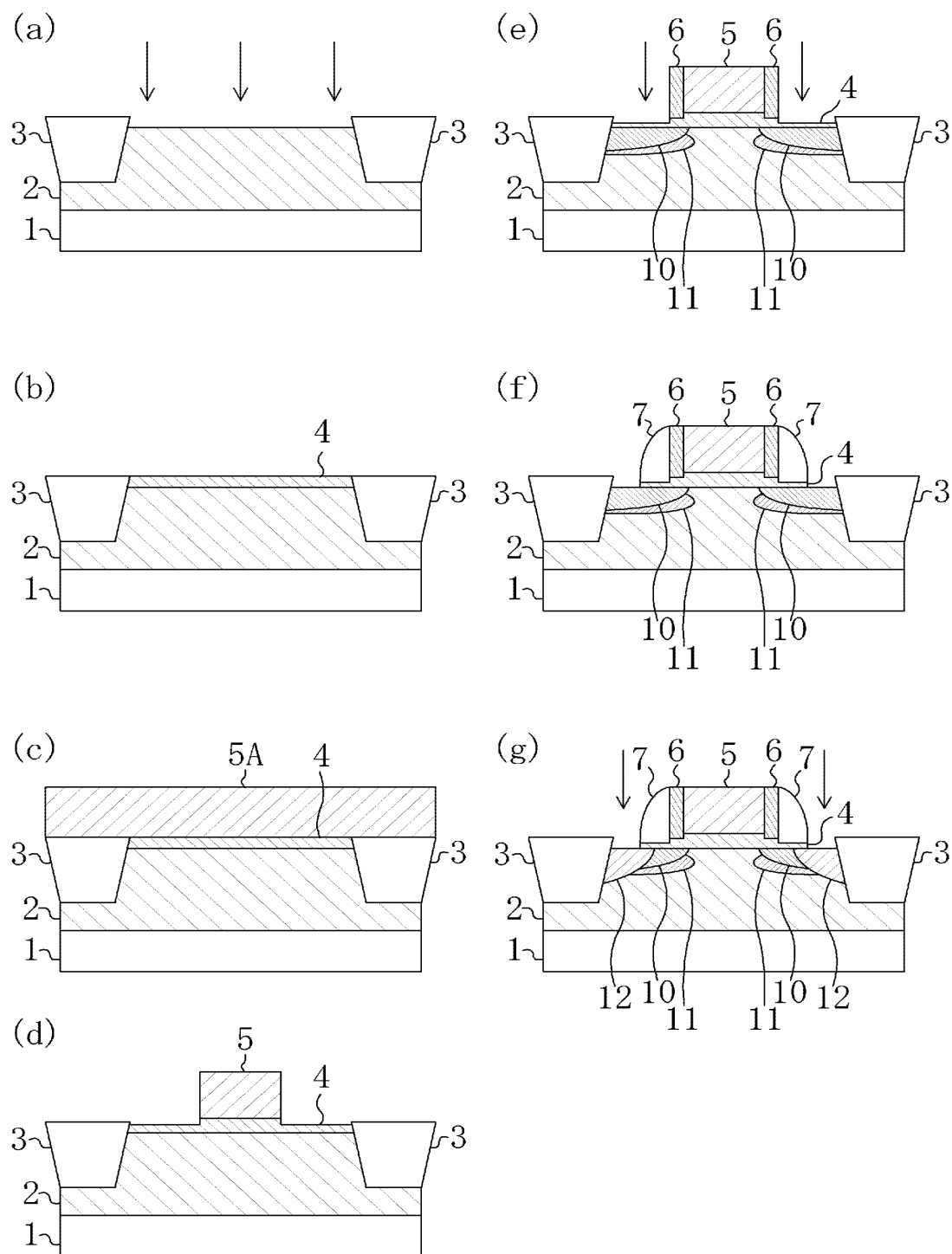
【図 11】



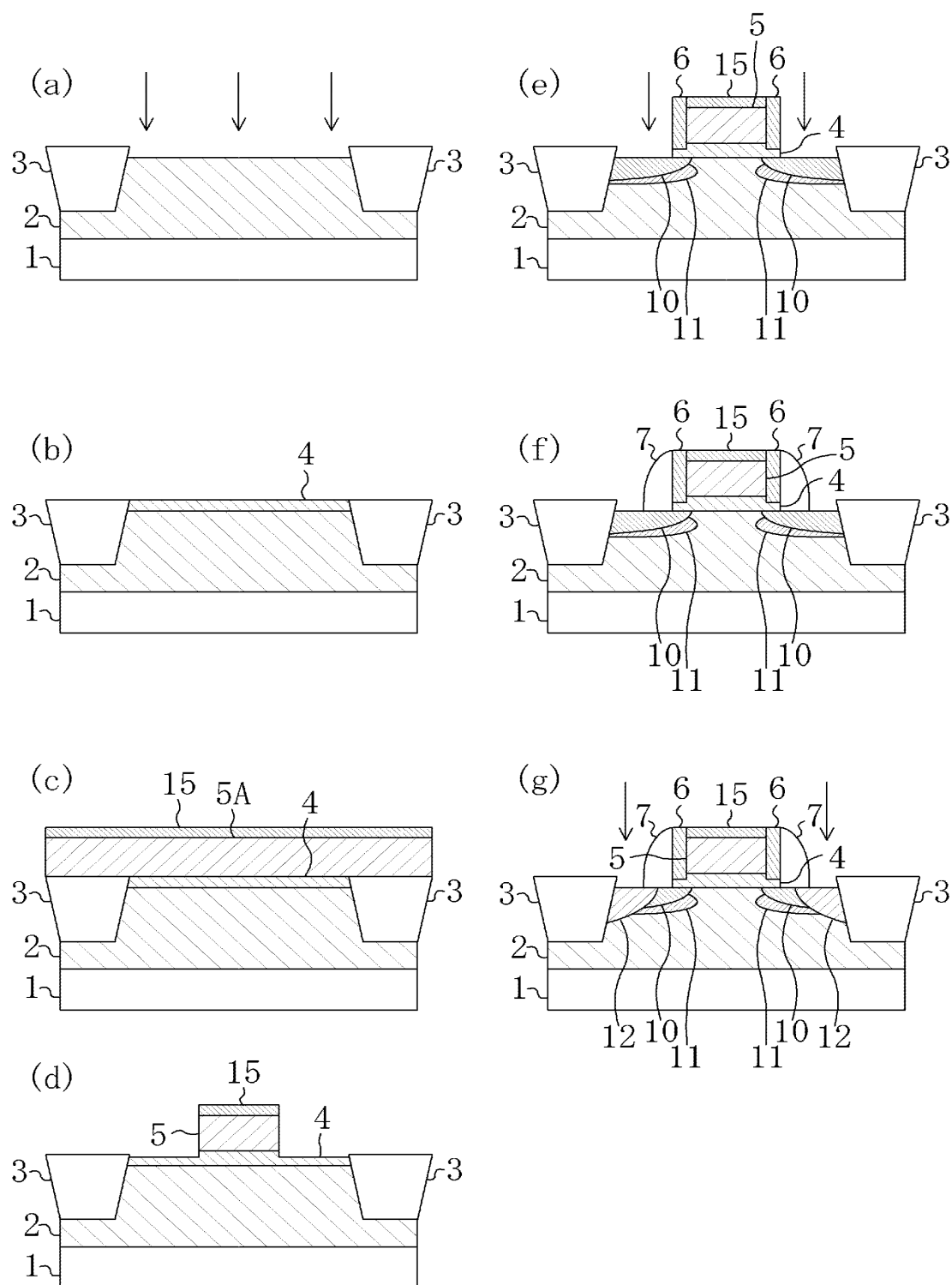
【図12】



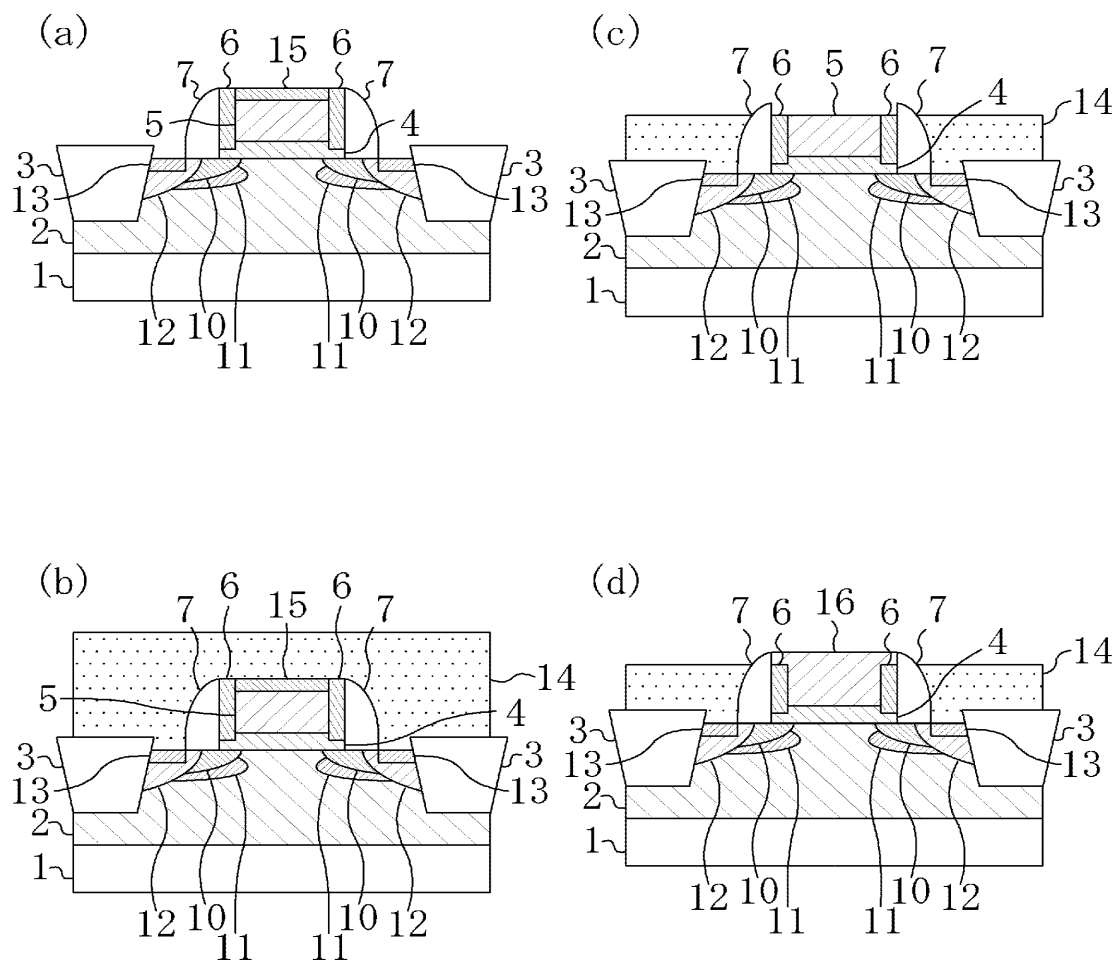
【図13】



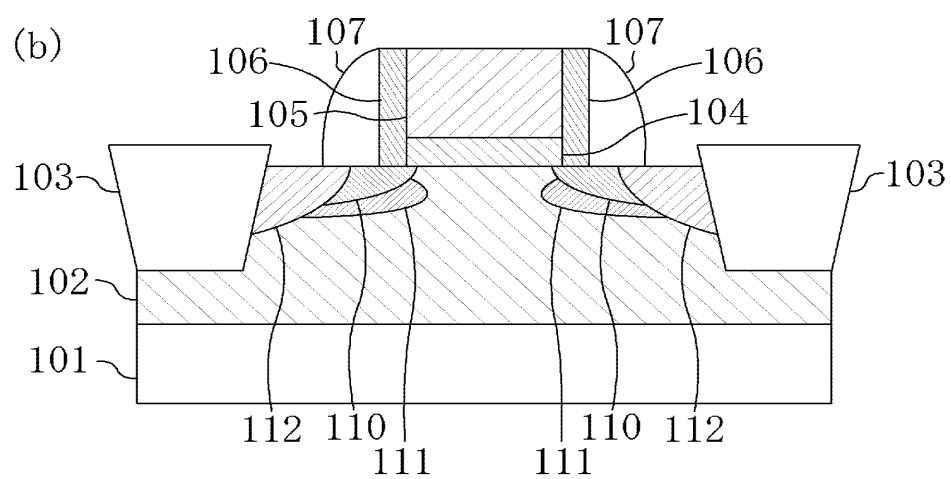
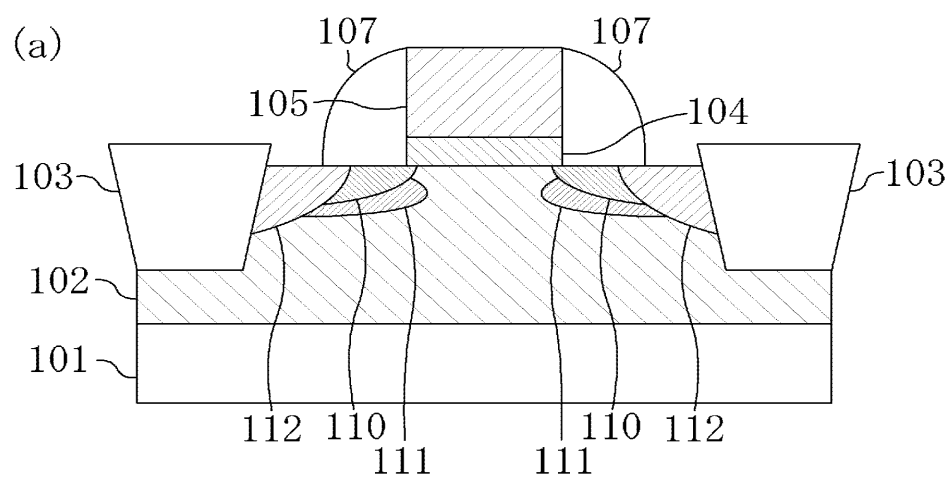
【図14】



【図15】



【图16】



【書類名】 要約書

【要約】

【課題】 高誘電率ゲート絶縁膜を使用したMISFETにおいて高誘電率ゲート絶縁膜を劣化させることなくMISFETの特性を向上させる。

【解決手段】 基板1の活性領域上に高誘電率ゲート絶縁膜4Aを介してゲート電極5が形成されている。ゲート電極5の側面には絶縁性のサイドウォール7が形成されている。高誘電率ゲート絶縁膜4Aはゲート電極5の下側からサイドウォール7の下側まで連続的に形成されている。高誘電率ゲート絶縁膜4Aにおけるサイドウォール7の下側領域の厚さは、高誘電率ゲート絶縁膜4Aにおけるゲート電極5の下側領域の厚さよりも小さい。

【選択図】 図1

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/037,831	03/01/2011	Junji HIRASE	085393-0499

CONFIRMATION NO. 7641

PUBLICATION NOTICE

53080
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096



0000000048379559

Title:SEMICONDUCTOR DEVICE

Publication No.US-2011-0147857-A1

Publication Date:06/23/2011

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/037,831	03/01/2011	Junji HIRASE	085393-0499	7641
53080	7590	09/09/2011		
MCDERMOTT WILL & EMERY LLP 600 13TH STREET, NW WASHINGTON, DC 20005-3096			EXAMINER LUU, CHUONG A	
			ART UNIT	PAPER NUMBER
			2892	
			NOTIFICATION DATE	DELIVERY MODE
			09/09/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mweipdocket@mwe.com

Office Action Summary	Application No.	Applicant(s)	
	13/037,831	HIRASE ET AL.	
	Examiner	Art Unit	
	CHUONG LUU	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 5) ☒ Claim(s) 21-42 is/are pending in the application.
- 5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 21-42 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 12) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 12/505,799.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____. |
| 3) ☒ Information Disclosure Statement(s) (PTO/SB/08) | 5) ☐ Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>3/1/2011</u> . | 6) ☐ Other: ____. |

DETAILED ACTION

REJECTIONS BASED UPON PRIOR ARTS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The Rejections

Claim 21 is rejected under 35 U.S.C. 102(e) as being anticipated by Hieda et al. (U.S. 6,992,358).

Hieda discloses a semiconductor device with

(21) a high dielectric constant gate insulating film (102-oxide) formed on an active region in a substrate (101);

a gate electrode (103) formed on the high dielectric constant gate insulating film (102-oxide);

an insulating sidewall (106) formed on each side surface of the gate electrode (103),

wherein the high dielectric constant gate insulating film (102-oxide) is continuously formed so as to extend from under the gate electrode (103) to under the insulating sidewall (106), and

at least part of the high dielectric constant gate insulating film (102-oxide) located under the insulating sidewall (106) has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film (102-oxide) located under the gate electrode (103) (see Figure 5B);

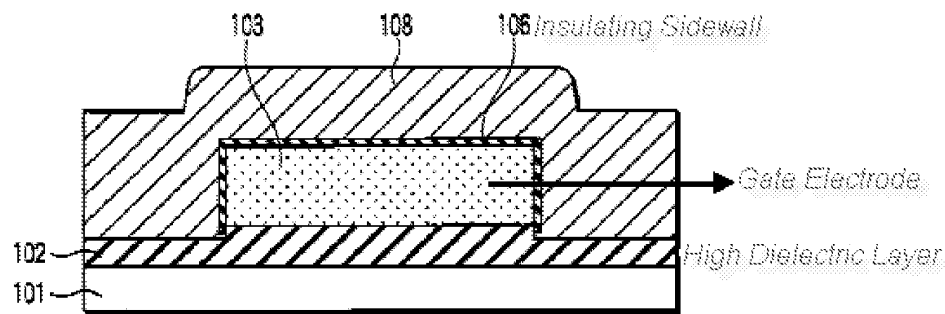


FIG. 5B

Claim 21 is rejected under 35 U.S.C. 102(e) as being anticipated by Hieda et al. (U.S. 6,992,358).

Hieda discloses, as shown in Figures 9A and 9C, a semiconductor device with

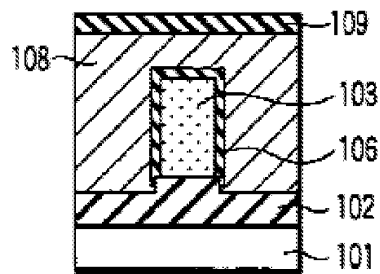


FIG. 9A

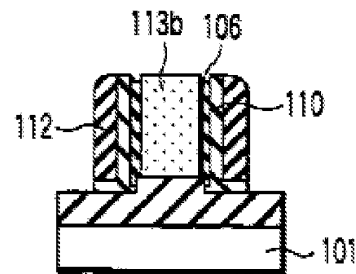


FIG. 9C

(21) a high dielectric constant gate insulating film (102-oxide) formed on an active region in a substrate (101);

a gate electrode (103) formed on the high dielectric constant gate insulating film (102-oxide);

a first insulating sidewall (106) formed on each side surface of the gate electrode (103),

a second insulating sidewall (110) formed on each side surface of the gate electrode (103) with the first insulating sidewall (106) interposed therebetween;

wherein the high dielectric constant gate insulating film (102-oxide) is continuously formed so as to extend from under the gate electrode (103) to under the first insulating sidewall (106), and

part of the high dielectric constant gate insulating film (102-oxide) located under the insulating sidewall (106) has a smaller thickness than a thickness of part of the high

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dielectric constant gate insulating film (102-oxide) located under the gate electrode

(103) (see Figures 9A and 9C);

OBVIOUS TYPE DOUBLE PATENTING

Statutory Basis

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

The Rejections

Claims 21-42 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 12-16 of U.S. Patent No. 7,923,764.

Although the conflicting claims are not identical, they are claiming common subject matter, as follows: both U.S. Patent and instant application claimed a semiconductor device capable of implementing a second insulating sidewall on each side surface of the gate electrode. Specifically, regarding claim 21 of instant application discloses a semiconductor device (claim 1 of Pat. 7,579,227, line 32) comprising: a high

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dielectric constant gate insulating film formed on an active region in a substrate (claim 1, lines 33-34); a gate electrode formed on the high dielectric constant gate insulating film (claim 1, lines 35-36); a insulating sidewall formed on each side surface of the gate electrode (claim 1, lines 37-38); wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall (claim 1, lines 42-44), and an end of the high dielectric constant gate insulating film under the insulating sidewall is located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode (claim 1, lines 45-49).

The limitations recited of the current application is broader compared with the U.S. Patent No. 7,923,764. Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the teaching of the Pat. No. 7,923,764 to fabricate a semiconductor structure as recited in the present application.

For these reasons, claim 21-42 are seen as obvious variations of the patented claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHUONG LUU whose telephone number is (571)272-1902. The examiner can normally be reached on M-F (6:30-3:00).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chuong A Luu/
Primary Examiner, Art Unit 2892
August 17, 2011

Notice of References Cited	Application/Control No. 13/037,831	Applicant(s)/Patent Under Reexamination HIRASE ET AL.	
	Examiner CHUONG LUU	Art Unit 2892	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,923,764	04-2011	Hirase et al.	257/295
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



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BIB DATA SHEET

CONFIRMATION NO. 7641

SERIAL NUMBER 13/037,831	FILING or 371(c) DATE 03/01/2011 RULE	CLASS 257	GROUP ART UNIT 2892	ATTORNEY DOCKET NO. 085393-0499		
APPLICANTS Junji HIRASE, Osaka, JAPAN; Akio Sebe, Osaka, JAPAN; Naoki Kotani, Hyogo, JAPAN; Gen Okazaki, Hyogo, JAPAN; Kazuhiko Aida, Chiba, JAPAN; Shinji Takeoka, Osaka, JAPAN; Yes, CAL						
** CONTINUING DATA ***** This application is a DIV of 12/505,799 07/20/2009 PAT 7,923,764 which is a DIV of 11/491,260 07/24/2006 PAT 7,579,227						
** FOREIGN APPLICATIONS ***** Yes, CAL JAPAN 2005-227457 08/05/2005						
** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 03/10/2011						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and /CHUONG A LUU/ Acknowledged Examiner's Signature		☒ Met after Allowance CAL Initials	STATE OR COUNTRY JAPAN	SHEETS DRAWINGS 11	TOTAL CLAIMS 22	INDEPENDENT CLAIMS 1
ADDRESS MCDERMOTT WILL & EMERY LLP 600 13TH STREET, NW WASHINGTON, DC 20005-3096 UNITED STATES						
TITLE SEMICONDUCTOR DEVICE						
FILING FEE RECEIVED 1194	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S117	2	11/491260	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30 21:31
S118	9	("20030022422" "20040004234" "20040129997" "20050121733" "20050127436" "20060121740" "6642071" "6929992" "6992358").PN. OR ("7579227").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/07/30 21:36
S119	1	12/505799	US-PGPUB; USPAT; USOCR	OR	ON	2010/07/30 21:37
S120	2925	(257/295).OCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/07/30 21:39
S121	1497	(257/310).OCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/07/30 21:39
S122	3	09/916509	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30 21:39
S123	4702	(257/296,295,310.ccls.) and (gate or electrode) and ((gate or electrode) adj (insulat\$4 or dielectric or oxide))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30 21:39
S124	587	(257/296,295,310.ccls.) and (gate or electrode) near ((gate or electrode) adj (insulat\$4 or dielectric or oxide))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30 21:39
S125	587	(257/296,295,310.ccls.) and ((gate or electrode) near ((gate or electrode) adj (insulat\$4 or dielectric or oxide)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30 21:40

S126	435	(257/296,295,310.ccls.) and ((gate or electrode) adj ((gate or electrode) adj (insulat\$4 or dielectric or oxide)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30 21:40
S127	57	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) near (high adj dielectric adj constant))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30 21:40
S128	33	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) adj (high adj dielectric adj constant))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30 21:40
S129	13	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) adj (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30 21:40
S130	19	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) near (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30 21:41
S131	6	"6992358"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30 21:41
S132	18	("20030209761" "20040150520" "20040178451" "20050040464" "20050051843" "20050110085" "4979014" "6437404" "6538916" "6580132" "6639246" "6646307" "6687152" "6724046" "6740938" "6744390" "6800513" "6822071").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/07/30 21:41
S133	55	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) same (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30 21:41
S134	6	((("7018873") or ("6929992") or ("6992358") or ("20060121740") or ("20050121733") or ("7579227")).PN.	US-PGPUB; USPAT	OR	OFF	2010/07/30 21:45
S135	9	((("6992358") or ("6929992") or ("6642071") or ("20060121740") or ("20030022422") or ("20040004234") or ("20040129997") or ("20050121733") or ("20050127436")).PN.	US-PGPUB; USPAT	OR	OFF	2010/07/30 21:52
S136	3	((("6,992,358") or ("7579227") or ("20050121733")).PN.	US-PGPUB; USPAT	OR	OFF	2010/08/02 04:43

S137	56	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) same (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/02 08:26
S138	1	("5473168").PN.	US-PGPUB; USPAT	OR	OFF	2010/12/02 09:41
S139	1	12/190015	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/02 09:42
S140	19	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) near (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/02 13:11
S141	6	"6992358"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:37
S142	1017	gate and ((gate adj (oxide or insulat\$4 or dielectric)) with (notch\$4 or undercut\$4))	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/04 20:38
S143	19	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) near (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:38
S144	137	gate and ((gate adj (oxide or insulat\$4 or dielectric)) near (notch\$4 or undercut\$4))	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/04 20:38
S145	23	gate and ((gate adj (oxide or insulat\$4 or dielectric)) adj (notch\$4 or undercut\$4))	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/04 20:38
S146	177	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) and (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:39
S147	2	((("6642071") or ("6929992")).PN.	USPAT	OR	OFF	2010/12/04 20:39
S148	6	(257/296,295,310.ccls.) and (((high adj dielectric adj constant) or (ferroelectric) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:39
S149	3	((("20070228442") or ("20040171280") or ("20030207097")).PN.	US-PGPUB; USPAT	OR	OFF	2010/12/04 20:40

S150	1555	hirase.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:40
S151	79	S150 and junji	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:41
S152	0	S151 and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) adj (high adj dielectric adj constant))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:41
S153	0	S151 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:41
S154	256	sebe.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:41
S155	18	S154 and akio	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:41
S156	0	S155 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:41
S157	18752	kotani.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:42
S158	236	S157 and naoki	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:42
S159	0	S158 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:42

S160	0	okazaki and gen and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:42
S161	0	aida and kazuhiko and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:43
S162	0	takeoka and shinji and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:43
S163	35	((((semiconductor) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) adj (high adj dielectric adj constant))))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:43
S164	21	((((semiconductor) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) adj (high adj dielectric adj constant))))).clm.	US-PGPUB	OR	ON	2010/12/04 20:43
S165	5	((("20050127436") or ("6284630") or ("20020163039") or ("20010028086") or ("5223445")).PN.	US-PGPUB; USPAT	OR	OFF	2010/12/04 20:44
S166	3	09/824672	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:44
S167	2	09/848431	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:44
S168	8	((("20050127436") or ("6284630") or ("20020163039") or ("20010028086") or ("5223445") or ("6509612") or ("6794258") or ("6614081")).PN.	US-PGPUB; USPAT	OR	OFF	2010/12/04 20:44
S169	4	10/904875	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:45
S170	1928	(257/324).OCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/04 20:46

S171	7	(257/296,295,310,324,410,411.ccls.) and (gate or electrode) and ((gate or electrode) adj (insulat\$4 or dielectric or oxide)) and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:46
S172	1290	(257/410).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/04 20:46
S173	185	257/e29.132.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:46
S174	1693	257/e29.133.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:46
S175	1606	257/e29.137.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:47
S176	181	257/e29.138.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:47
S177	676	257/e29.162.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:47
S178	570	257/e29.165.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:47
S179	2	(257/e29.132,e29.133,e29.134,e29.135,e29.136,e29.137,e29.138,e29.138,e29.162,e29.163,e29.164,e29.164,e29.165.ccls.) and (gate or electrode) and ((gate or electrode) adj (insulat\$4 or dielectric or oxide)) and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:47
S180	1375	(257/411).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/04 20:48

S181	54	(257/296,295,310,324,410,411.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:48
S182	48	(257/296,295,310,324,410,411.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:48
S183	111	("257"/\$.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:48
S184	23	(257/e29.132,e29.133,e29.134,e29.135,e29.136,e29.137,e29.138,e29.138,e29.162,e29.163,e29.164,e29.164,e29.165.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:48
S185	102	(257/e\$.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:49
S186	32	("438"/\$.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:49
S187	5444	(257/296,295,310,324,410,411.ccls.) and (gate or electrode) and ((gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:50
S188	48	(257/296,295,310,324,410,411.ccls.) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:50
S189	770	(257/296,295,310,324,410,411.ccls.) and (((gate or electrode) adj (dielectric or oxide or insulat\$4)) with ((high adj dielectric adj constant) or (ferroelectric))) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:50
S190	184	(257/296,295,310,324,410,411.ccls.) and (((gate or electrode) adj (dielectric or oxide or insulat\$4)) near ((high adj dielectric adj constant) or (ferroelectric))) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:50

S191	1011	((257/296,295,310,324,410,411.ccls.) and (((gate or electrode) adj (dielectric or oxide or insulat\$4)) same ((high adj dielectric adj constant) or (ferroelectric))) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:51
S193	2	10/519799	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:51
S194	2	"7186604"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:51
S195	2	11/491260	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:52
S196	1375	(257/411).OCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/04 21:13
S197	1	"13037831"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/17 17:43
S198	3142	(257/295).OCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/08/17 17:44
S199	3	11/491260	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/17 17:44
S200	2	12/505799	US-PGPUB; USPAT; USOCR	OR	ON	2011/08/17 17:44
S201	5	((("20030022422") or ("20040004234") or ("20040129997") or ("20050121733") or ("20060121740")).PN.	US-PGPUB	OR	OFF	2011/08/17 20:09
S202	3	((("7,579,227") or ("20050121733") or ("6,992,358")).PN.	US-PGPUB; USPAT	OR	OFF	2011/08/17 20:13
S203	8	((("20030022422") or ("20040004234") or ("20040129997") or ("20050121733") or ("20060121740") or ("6,992,358") or ("6,929,992") or ("6,642,071")).PN.	US-PGPUB; USPAT	OR	OFF	2011/08/17 20:14

S204	3	((("6,992,358") or ("6,929,992") or ("6,642,071"))).PN.	US-PGPUB; USPAT	OR	OFF	2011/08/17 20:14
S205	2	((("7923764") or ("7579227"))).PN.	US-PGPUB; USPAT	OR	OFF	2011/08/18 08:34

8/27/11 11:15:50 PM

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Search Notes

Application/Control No.

13/037,831

Examiner

CHUONG LUU

Applicant(s)/Patent under
Reexamination

HIRASE ET AL.

Art Unit

2892

SEARCHED

Class	Subclass	Date	Examiner
257	295	8/17/2011	CAL

INTERFERENCE SEARCHED

Class	Subclass	Date	Examiner

**SEARCH NOTES
(INCLUDING SEARCH STRATEGY)**

	DATE	EXMR
Please see the attachment.	8/17/2011	CAL

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Substitute for form 1449/PTO)				ATTY. DOCKET NO. 085393-0499		SERIAL NO. ~~Divisional of U.S.~~ ~~Serial No. 12/505,799~~ 13/037,831	
				APPLICANT Junji HIRASE, et al.			
				FILING DATE March 1, 2011		GROUP 2892 ~~Not Yet Assigned~~	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
↓ 		US 6,992,358	01-2006	Hieda et al.			
		US 6,929,992	08-2005	Djomehri et al.			
		US 6,642,071	11-2003	Cheng, Jia-Shyong			
		US 2006/0121740 A2	6/8-2006	SAKAI et al.			
		US 2003/0022422 A1	01-30-2003	TORII et al.			
		US 2004/0004234 A1	01-08-2004	YAGISHITA et al.			
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		US 7,579,227	08-2009	Hirase et al.			
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	US 6,992,358	01-2006	Hieda et al.				
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EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes - Number - Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes No	
/C.L./		CN 1610129 A	04-27-2005		Corresponds w/ US 2005/0127436		
/C.L./		JP 2005-064190	03-10-2005	TOSHIBA CORP.			
/C.L./		JP 2004-356576	12-16-2004	SEMICONDUCTOR LEADING EDGE TECHNOLOGIES INC.			
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
/C.L./		WATANABE, Ken, Partial English Translation of "HfSiON-CMOS technology for achieving high performance and high reliability," SEMI FORUM Japan, 2005, IT System & ULSI Technology,					
/C.L./		HORI, Takashi, "1/4-μm LATID (LArge-Tilt-angle Implanted Drain) TECHNOLOGY FOR 3.3-V OPERATION", CH2637-7/89/0000-0777 1989 IEEE, IEDM 89-777-780-IEDM 89					
/C.L./		SAYAMA, et al., H., "80nm CMOSFET Technology Using Double Offset-Implanted Source/Drain Extension and Low Temperature SIN Process", IEDM 2000, IEDM 00-239-242-IEDM 00					
/C.L./		U.S. Office Action issued in U.S. Patent Application No. 11/543,865 dated on November 12, 2008					
/C.L./		Chinese Office Action, with English Translation, issued in Chinese Patent Application No. CN 200610093872.2, dated March 20, 2009.					
/C.L./		Notice Allowance issued in United States Patent Application No. 12/505,799, mailed December 13, 2010.					
EXAMINER /Chuong Luu/				DATE CONSIDERED 08/17/2011			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

Index of Claims 	Application/Control No.		Applicant(s)/Patent under Reexamination	
	13/037,831		HIRASE ET AL.	
	Examiner		Art Unit	
	CHUONG LUU		2892	

✓	Rejected	—	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
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Claim		Date											
Final	Original	8/17/11											
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Junji HIRASE, et al.	:	Confirmation Number: 7641
	:	
Application No.: 13/037,831	:	Group Art Unit: 2892
	:	
Filed: March 01, 2011	:	Examiner: LUU, CHUONG A.
	:	
For: SEMICONDUCTOR DEVICE	:	

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection or Notice of Allowance.

CERTIFICATION PARAGRAPH

The undersigned certifies that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a

counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement as described in 37 CFR 1.97(e)(1).

Each Japanese reference was cited in a corresponding Japanese application Office Action dated September 27, 2011. Please note that the reference **JP 2005-064190** has been previously cited in an Information Disclosure Statement filed March 1, 2011; therefore, only the English translation is attached herewith.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

**Please recognize our Customer No. 53080
as our correspondence address.**

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:mjb
Facsimile: 202.756.8087
Date: October 27, 2011

INFORMATION DISCLOSURE STATEMENT BY APPLICANT		ATTY. DOCKET NO. 085393-0499		SERIAL NO. 13/037,831		
		APPLICANT Junji HIRASE, et al.				
		FILING DATE March 01, 2011		GROUP 2892		
(Substitute for form 1449/PTO)						
U.S. PATENT DOCUMENTS						
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ₂ (<i>if known</i>)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		US				
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FOREIGN PATENT DOCUMENTS						
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes - Number 4 - Kind Codes (<i>if known</i>)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes No
		JP 2005-064190	03-10-2005	TOSHIBA CORP		English translation only
		JP 2004-172178	06-17-2004			X
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)						
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.				
EXAMINER			DATE CONSIDERED			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

Electronic Acknowledgement Receipt	
EFS ID:	11282420
Application Number:	13037831
International Application Number:	
Confirmation Number:	7641
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Junji HIRASE
Customer Number:	53080
Filer:	Michael E. Fogarty/Margaret Barham
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0499
Receipt Date:	27-OCT-2011
Filing Date:	01-MAR-2011
Time Stamp:	16:26:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	P04204204_IDS_085393-0499. PDF	73364	no	3
			525a065ba9aee5a93ac5aff0abfda773b0fed6c9a		
Warnings:					
Information:					

2	Foreign Reference	P04204204_REF1_085393-0499 .PDF	311593 081c62f558f6152dff0d3ad0fb1fb58569bf6d	no	40
Warnings:					
Information:					
3	Foreign Reference	P04204204_REF2_085393-0499 .PDF	845968 d38a4ef1fca48333b13f73b9275abe6657c20c2e	no	45
Warnings:					
Information:					
Total Files Size (in bytes):			1230925		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Docket No.: 085393-0499

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Junji HIRASE, et al.	:	Confirmation Number: 7641
	:	
Application No.: 13/037,831	:	Group Art Unit: 2892
	:	
Filed: March 1, 2011	:	Examiner: Chuong A. LUU
	:	
For: SEMICONDUCTOR DEVICE	:	

AMENDMENT UNDER 37 C.F.R. § 1.111

Mail Stop – Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated September 9, 2011 having a shortened statutory period of response set to expire on December 9, 2011, please amend the above-identified application as follows:

- 1 -

IN THE SPECIFICATION:

Please amend the following paragraph on page 1 of the specification as follows:

-- RELATED APPLICATIONS

This application is a Divisional of U.S. Patent Application No. 12/505,799, filed on July 20, 2009, which is now U.S. Patent No. 7,923,764, which is a Divisional of U.S. Patent Application No. 11/491,260, filed on July 24, 2006, now U.S. Patent No. 7,579,227, claiming priority of Japanese Patent Application No. 2005-227457, filed on August 5, 2005, the entire contents of each of which are incorporated by reference. --

REMARKS

I. Introduction

In response to the pending Office Action, Applicants have amended the specification so as to update the priority information.

For at least the reasons set forth below, it is respectfully submitted that all pending claims are patentable over the cited prior art references.

II. The Rejection Of The Claim Under 35 U.S.C. § 102

Claim 21 was rejected under 35 U.S.C. § 102 as being anticipated by USP No. 6,992,358 to Hieda. For at least the following reasons, it is respectfully submitted that claim 21 is not anticipated by Hieda.

Claim 21 relates to a semiconductor device and recites in part a high dielectric constant gate insulating film formed on an active region in a substrate; a gate electrode formed on the high dielectric constant gate insulating film; and an insulating sidewall formed on each side surface of the gate electrode. Claim 21 further recites that the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall, and that **an end of the high dielectric constant gate insulating film under the insulating sidewall is located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode**. Thus, as recited by claim 21, the high dielectric constant gate insulating film does not extend so as to reach the outer end of the insulating sidewall.

For example, referring to the exemplary embodiments shown in Figs. 6 and 10, the high dielectric constant gate insulating film 4a extends under both the gate electrode 5 and the first

- 3 -

insulating sidewalls 7, however, the high dielectric constant gate insulating film 4a is not disposed underneath the outer ends of the insulating sidewalls 7. As noted, for example, in paragraph [0058] of the published application (USP Pub. No. 2011/0147857), a portion of the high dielectric constant gate insulating film 4a is removed beneath the outer ends of the insulating sidewalls 7.

Turning to the pending rejection and the cited prior art, it is asserted that the buried oxide film 102 of Hieda corresponds to the recited high dielectric constant gate insulating film, and that the oxide film 106 corresponds to the recited insulating sidewalls. First, it is noted that the pending rejection addresses the thickness of the gate insulating film 102 located under the alleged sidewall 106 relative to thickness of the gate insulating film 102 under gate electrode 103. Importantly, however, claim 21 does not recite any limitations directed to the thickness of the gate insulating film.

Moreover, Heidi does not disclose or suggest the element of claim 21 noted above which recites *an end of the high dielectric constant gate insulating film under the insulating sidewall is located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode.* In other words, the recited high dielectric constant gate electrode recited by claim 21 does not extend so far such that it is disposed beneath the outer end of the insulating sidewall, as is shown, for example, in the exemplary embodiments of Figs. 6 and 10. It is disposed inwardly of the outer end of the insulating sidewall.

In direct contrast, Heidi only discloses a device in which the alleged gate insulating film 102 extends below and beyond the outer ends of the alleged sidewall 106. Indeed, as shown in Figs. 5B, 9A and 9C, the gate insulating film 102 extends beyond the outer end of the sidewall

106, and beyond the outer ends of films 110 and 112 of Hieda. Thus, it is clear that, at a minimum, Hieda fails to disclose the foregoing element recited by claim 21.

It is well known that the factual determination of lack of novelty under 35 U.S.C. § 102 requires the identical disclosure in a single reference of each element of a claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art. *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F.3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994). For all of the foregoing reasons, it is clear that Heidi does not disclose or suggest each of the elements recited by claim 21, and therefore does not anticipate claim 21.

III. The Obvious Type Double Patenting Rejection

In response to the pending obviousness-type double patenting rejection, Applicants submit herewith a terminal disclaimer so as to overcome the pending rejection.

IV. Dependent Claims

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as the pending independent claim is patentable for at least the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable.

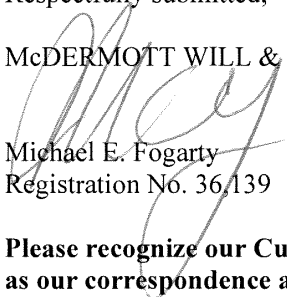
V. Summary

Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

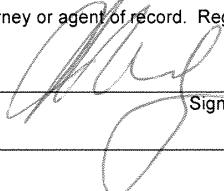
McDERMOTT WILL & EMERY LLP


Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:lcb
Facsimile: 202.756.8087
Date: November 17, 2011

**Please recognize our Customer No. 53080
as our correspondence address.**

DM_US 30776117-1.085393.0499

TERMINAL DISCLAIMER TO OBTAIN A DOUBLE PATENTING REJECTION OVER "PRIOR" PATENT		Docket Number (Optional) 085393-0499
In re Application of: Junji HIRASE, et al. Application No.: 13/037,831 Filed: March 1, 2011 For: SEMICONDUCTOR DEVICE		
The owner*, <u>Panasonic Corporation</u>, of <u>100</u> percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term prior patent No. <u>7,923,764</u> as the term of said patent is defined in 35 U.S.C. 154 and 173, and as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 and 173 of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later: - expires for failure to pay a maintenance fee; - is held unenforceable; - is found invalid by a court of competent jurisdiction; - is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321; - has all claims canceled by a reexamination certificate; - is reissued; or - is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer. Check either box 1 or 2 below, if appropriate. 1. ☐ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. 2. ☒ The undersigned is an attorney or agent of record. Reg. No. <u>36,139</u>  _____ Signature <u>November 17, 2011</u> Date <u>Michael E. Fogarty</u> Typed or printed name <u>202.756.8372</u> Telephone Number ☒ Terminal disclaimer fee under 37 CFR 1.20(d) is included ☒ Charge Deposit Account 500417 ☐ Check enclosed WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038. *Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner). Form PTO/SB/96 may be used for making this statement. See MPEP § 324.		

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

DM_US 30782254-1.085393.0499

Electronic Patent Application Fee Transmittal				
Application Number:		13037831		
Filing Date:		01-Mar-2011		
Title of Invention:		SEMICONDUCTOR DEVICE		
First Named Inventor/Applicant Name:		Junji HIRASE		
Filer:		Michael E. Fogarty/Lynn Cruz		
Attorney Docket Number:		085393-0499		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Statutory or terminal disclaimer	1814	1	160	160
Total in USD (\$)				160

Electronic Acknowledgement Receipt	
EFS ID:	11433560
Application Number:	13037831
International Application Number:	
Confirmation Number:	7641
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Junji HIRASE
Customer Number:	53080
Filer:	Michael E. Fogarty/Lynn Cruz
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0499
Receipt Date:	17-NOV-2011
Filing Date:	01-MAR-2011
Time Stamp:	16:57:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 160
RAM confirmation Number	3980
Deposit Account	500417
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		085393_0499_Amendmentand TD.pdf	106666 51393ffd4223662f5f820e07f872bb0022f4e174	yes	7
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Specification		2	2	
	Applicant Arguments/Remarks Made in an Amendment		3	6	
	Terminal Disclaimer Filed		7	7	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30103 66080d05b7f115970b491abf13d931d935881e17	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			136769		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 13/037,831		Filing Date 03/01/2011		☐ To be Mailed			
APPLICATION AS FILED – PART I												
(Column 1)			(Column 2)		SMALL ENTITY ☐		OR		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)			RATE (\$)	FEE (\$)				
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A				N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A				N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A				N/A					
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$	=	OR		X \$	=				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=			X \$	=				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).											
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))												
* If the difference in column 1 is less than zero, enter "0" in column 2.					TOTAL			TOTAL				
APPLICATION AS AMENDED – PART II												
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR		OTHER THAN SMALL ENTITY	
AMENDMENT	11/17/2011	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	* 22	Minus	** 22	=	X \$	=	OR		X \$	=	
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	=	X \$	=	OR		X \$	=	
	☐ Application Size Fee (37 CFR 1.16(s))								OR			
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								OR			
						TOTAL ADD'L FEE			OR		TOTAL ADD'L FEE	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$	=	OR		X \$	=	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$	=	OR		X \$	=	
	☐ Application Size Fee (37 CFR 1.16(s))								OR			
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								OR			
						TOTAL ADD'L FEE			OR		TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										Legal Instrument Examiner: /PEGGY YARBOROUGH/		

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Application Number 	Application/Control No. 13/037,831	Applicant(s)/Patent under Reexamination HIRASE ET AL.	
Document Code - DISQ		Internal Document – DO NOT MAIL	

TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Date Filed : 11/17/11	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:
jean proctor

U.S. Patent and Trademark Office

INFORMATION DISCLOSURE STATEMENT BY APPLICANT						ATTY. DOCKET NO. 085393-0499		SERIAL NO. 13/037,831				
(Substitute for form 1449/PTO)						APPLICANT Junji HIRASE, et al.						
						FILING DATE March 01, 2011		GROUP 2892				
U.S. PATENT DOCUMENTS												
EXAMINER'S INITIALS		CITE NO.	Document Number Number-Kind Code ² (if known)		Publication Date MM-DD-YYYY		Name of Patentee or Applicant of Cited Document		Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear			
		US	2004/0227185		11-18-2004		MATSUMOTO et al.		Corresponds to JP 2004-241755			
		US										
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EXAMINER'S INITIALS		CITE NO.	Foreign Patent Document Country Codes - Number 4 - Kind Codes (if known)		Publication Date MM-DD-YYYY		Name of Patentee or Applicant of Cited Document		Pages, Columns, Lines Where Relevant Figures Appear		Translation Yes No	
			JP 2003-258241		09-12-2003						X	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)												
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[Claim(s)]

[Claim 1] A semiconductor device which functions as an MOSFET, comprising:

Gate dielectric film which consists of a high dielectric film formed on a semiconductor substrate.

A gate electrode which consists of a conductive film formed on said gate dielectric film.

The 1st sidewall that consists of a dielectric film formed in a side attachment wall of said gate electrode.

The 2nd sidewall that consists of an oxidation-resistant film formed so that said 1st sidewall might be covered.

[Claim 2] The semiconductor device according to claim 1, wherein the upper part of said 1st sidewall is lower than height of said gate electrode.

[Claim 3] The semiconductor device according to claim 1 or 2, wherein said gate dielectric film and said 1st sidewall consist of the same dielectric film.

[Claim 4] A semiconductor device given in any 1 clause of Claims 1-3 having further a

cap film which consists of an oxidation-resistant film formed on said gate electrode.

[Claim 5]A manufacturing method of a semiconductor device which functions as an MOSFET characterized by comprising the following.

A process of forming gate dielectric film which consists of high dielectric films on a semiconductor substrate (a).

A process (b) of forming a gate electrode which consists of conductive films on said gate dielectric film.

A process (c) of forming the 1st sidewall that becomes a side attachment wall of said gate electrode from a dielectric film.

A process (d) of forming the 2nd sidewall that consists of an oxidation-resistant film so that said 1st sidewall may be covered.

[Claim 6]A manufacturing method of the semiconductor device according to claim 5 forming the upper part of said 1st sidewall so that it may become lower than height of said gate electrode.

[Claim 7]A manufacturing method of the semiconductor device according to claim 5 or 6, wherein said gate dielectric film and said 1st sidewall consist of the same dielectric film.

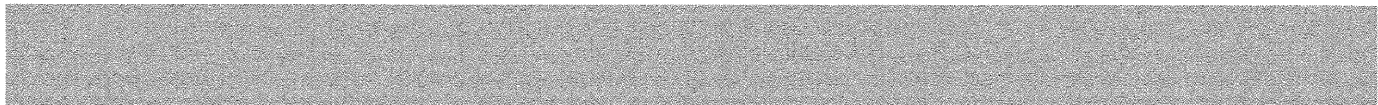
[Claim 8]A manufacturing method of a semiconductor device which functions as an MOSFET characterized by comprising the following.

A process of forming gate dielectric film which consists of high dielectric films on a semiconductor substrate (a).

A process (b) of depositing a conductive film and an oxidation-resistant film one by one on said gate dielectric film.

A process (c) of providing an etching mask, etching said oxidation-resistant film and said conductive film one by one, and forming a cap film and a gate electrode on said oxidation-resistant film.

A process (d) of forming the 1st sidewall that becomes only a side attachment wall of said gate electrode from a dielectric film.



A process of forming the 2nd sidewall that consists of an oxidation-resistant film so that said 1st sidewall may be covered (e).

[Claim 9]A manufacturing method of the semiconductor device according to claim 8 having combined the upper part of said 2nd sidewall with a side attachment wall of said cap film.

[Claim 10]A manufacturing method of the semiconductor device according to claim 8 or 9, wherein said gate dielectric film and said 1st sidewall consist of the same dielectric film.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]Especially this invention relates to the insulated-gate type field effect transistor which has gate dielectric film which consists of high dielectrics (high dielectric constant material) about a semiconductor device and a manufacturing method for the same.

[0002]

[Description of the Prior Art]In recent years, the miniaturization of the insulated-gate type field effect transistor (henceforth MOSFET) using silicon oxide (henceforth a SiO_2 film) is progressing by progress of the processing technology of a semiconductor process. However, if thin film-ization of gate dielectric film is advanced with proportionality reduction of MOSFET, increase of the gate leakage current by tunnel current will become a problem. In order to avoid this problem, research of MOSFET which has gate dielectric film (henceforth high dielectric gate dielectric film) which consists of a high dielectric which used the zirconium oxidation film (henceforth a ZrO_2 film) etc. is done. On the other hand, if micro processing of a gate electrode is advanced with reduction of an element, film decrease and damage will arise in the gate dielectric film in the ground of a gate electrode by reactive ion etching (henceforth RIE) which realizes anisotropy. This becomes a cause and the poor resisting pressure of gate

dielectric film and reliability degradation occur. By the conventional MOSFET, in order to solve this problem, after forming a gate electrode, a silicon substrate is reoxidated and a bird's beak (henceforth Gate Bird's Beak) is formed in the edge lower part of a gate electrode. What was indicated to JP,H6-204237,A is known by MOSFET which has such Gate Bird's Beak.

[0003]It explains referring to Drawings for the structure and the manufacturing method of MOSFET which has conventional Gate Bird's Beak hereafter. Drawing 4 is a sectional view showing the manufacturing process of the n type conventional MOSFET.

[0004]The semiconductor substrate which consists of a silicon single crystal of a p type [21] in drawing 4. (It is hereafter called a Si substrate), the gate dielectric film in which 22 consists of a SiO₂ film, The gate electrode in which 23 consists of a n type polycrystalline silicon film (henceforth a poly Si film), the LDD diffusion layer of a n type [24], the SiO₂ film in which, as for 25, an end becomes Gate Bird's Beak, the sidewall which 26 becomes from a TEOS film, and 27 are n⁺ type source drain diffusion layers.

[0005]First, as shown in drawing 4 (A), after forming an element isolation layer (not shown) on Si substrate 21 which consists of a p type silicon single crystal which has a field (100), the SiO₂ film 22 which oxidizes Si substrate 21 thermally and turns into gate dielectric film is formed. Then, after depositing a n type poly Si film on the SiO₂ film 22 with a CVD method, RIE is performed for a resist film (not shown) on a mask, and the gate electrode 23 is formed. At this time, film decrease also of the SiO₂ film 22 of a ground film is etched and carried out. Damage is produced on the surface of the SiO₂ film 22 by an etching damage. After removing a resist film, the ion implantation of the arsenic is carried out for the gate electrode 23 to a mask, and n type LDD diffusion layer 24 is formed in the surface of Si substrate 21.

[0006]Next, if Si substrate 21 is again oxidized thermally and the SiO₂ film 25 is formed on LDD diffusion layer 24 as shown in drawing 4 (B), Gate Bird's Beak will be formed in the edge lower part of the gate electrode 23. If it does in this way, the SiO₂ film 22 which carried out film decrease by etching will be reoxidated, and it will change

to the thick SiO₂ film 25. Damage to the surface of the SiO₂ film 22 is also recovered by reoxidation. Therefore, the poor resisting pressure of gate dielectric film and reliability degradation can be controlled.

[0007]Next, after depositing a TEOS film so that the gate electrode 23 top may be covered with a CVD method as shown in drawing 4 (C), RIE is performed to this TEOS film and the sidewall 26 is formed in the side attachment wall of the gate electrode 23.

[0008]Next, as shown in drawing 4 (D), the ion implantation of the arsenic is carried out for the gate electrode 23 and the sidewall 26 to a mask, and the n⁺ type source drain diffusion layer 27 is formed in the surface of Si substrate 21. Finally, although use well-known technology and it is not illustrated, an interlayer insulation film, a contact hole, and metallic wiring are formed one by one on Si substrate 21, and the conventional MOSFET is completed.

[0009]As mentioned above, by forming Gate Bird's Beak, the increase in gate leakage current was controlled and MOSFET which poor resisting pressure and reliability degradation do not generate is realized.

[0010]

[Problem to be solved by the invention]However, although the conventional composition could be applied to MOSFET which used the SiO₂ film, it was not able to be applied to MOSFET using the high dielectric gate dielectric film which consists of a ZrO₂ film etc. from the following Reasons.

[0011]In the oxidation process which forms Gate Bird's Beak, oxidation seeds (oxygen etc.) infiltrate into an interface with a ZrO₂ film or a Si substrate from the edge lower part of a gate electrode, the inside of a film and an interface are diffused further, the Si substrate under a gate electrode is oxidized, and a thin SiO₂ film is formed. By this, since gate dielectric film turns into a cascade screen of a ZrO₂ film and a thin SiO₂ film substantially, the specific inductive capacity of the whole gate dielectric film will fall compared with a ZrO₂ film from the first. For example, if Gate Bird's Beak is formed after specific inductive capacity forms the ZrO₂ film whose thickness is 5.0 nm by 15-20, the thin SiO₂ film whose thickness specific inductive capacity is 0.2-0.3 nm in

3.9 will be formed in an interface. In this case, the specific inductive capacity of the whole gate dielectric film is 13-17, and thickness is set to 5.2-5.3 nm. That is, although the increase in thickness of the whole gate dielectric film is only about 5%, since specific inductive capacity falls about 14%, the current capability of MOSFET declines substantially as a result. Since a SiO₂ film thick in the shape of a wedge is formed in the edge lower part of a gate electrode, effectual gate length changes and the threshold voltage of MOSFET is changed. Thus, when Gate Bird's Beak was formed in MOSFET using high dielectric gate dielectric film, there was a problem of deteriorating or changing the electrical property of MOSFET.

[0012]If heat treatment in atmosphere and the deposition of an insulator layer containing oxidation or oxygen gas are performed after forming a gate electrode even when not forming Gate Bird's Beak, Like the case where Gate Bird's Beak is formed, since an ultra-thin SiO₂ film is formed in Si interface, the specific inductive capacity of the whole gate dielectric film will fall. Therefore, there was a problem that the electrical property of MOSFET using high dielectric gate dielectric film deteriorated also in this case.

[0013]This invention was made in view of the above-mentioned problem, and is ****. The purpose is to provide a semiconductor device which controlled the poor resisting pressure of gate dielectric film, and reliability degradation, and prevented decline in high specific inductive capacity, and a manufacturing method for the same.

[0014]

[Means for solving problem]In order that this invention may attain the above-mentioned purpose, the semiconductor device of this invention is characterized by that the semiconductor device which functions as an MOSFET comprises:

Gate dielectric film which consists of a high dielectric film formed on the semiconductor substrate.

The gate electrode which consists of a conductive film formed on gate dielectric film.

The 1st sidewall that consists of a dielectric film formed in the side attachment wall of a

gate electrode.

The 2nd sidewall that consists of an oxidation-resistant film formed so that the 1st sidewall might be covered.

[0015]By this composition, the poor resisting pressure and reliability degradation by the film decrease and damage to high dielectric gate dielectric film can be controlled. Since an ultra-thin SiO₂ film is not formed in Si interface at a next process, decline in the high specific inductive capacity of high dielectric gate dielectric film can be prevented.

[0016]As for the upper part of the 1st sidewall, in the above-mentioned semiconductor device, it is preferred that it is lower than the height of a gate electrode.

[0017]In the above-mentioned semiconductor device, it is preferred that gate dielectric film and the 1st sidewall consist of the same dielectric film.

[0018]In the above-mentioned semiconductor device, it is preferred to have had further the cap film which consists of an oxidation-resistant film formed on the gate electrode.

[0019]As for this invention, the manufacturing method of the semiconductor device of this invention is characterized by that the manufacturing method of the semiconductor device which functions as an MOSFET comprises the following again.

The process of forming the gate dielectric film which consists of high dielectric films on a semiconductor substrate (a).

The process (b) of forming the gate electrode which consists of conductive films on gate dielectric film.

The process (c) of forming the 1st sidewall that becomes a side attachment wall of a gate electrode from a dielectric film.

The process (d) of forming the 2nd sidewall that consists of an oxidation-resistant film so that the 1st sidewall may be covered.

[0020]By this composition, the poor resisting pressure and reliability degradation by the film decrease and damage to high dielectric gate dielectric film can be controlled. Since an ultra-thin SiO₂ film is not formed in Si interface at a next process, decline in the high

specific inductive capacity of high dielectric gate dielectric film can be prevented.

[0021]As for the upper part of the 1st sidewall, in the manufacturing method of the above-mentioned semiconductor device, it is preferred to form so that it may become lower than the height of a gate electrode.

[0022]In the manufacturing method of the above-mentioned semiconductor device, it is preferred that gate dielectric film and the 1st sidewall consist of the same dielectric film.

[0023]As for this invention, the manufacturing method of the semiconductor device of this invention is characterized by that the manufacturing method of the semiconductor device which functions as an MOSFET comprises the following further.

The process of forming the gate dielectric film which consists of high dielectric films on a semiconductor substrate (a).

The process (b) of depositing a conductive film and an oxidation-resistant film one by one on gate dielectric film.

The process (c) of providing an etching mask, etching an oxidation-resistant film and a conductive film one by one, and forming a cap film and a gate electrode on an oxidation-resistant film.

The process (d) of forming the 1st sidewall that becomes only a side attachment wall of a gate electrode from a dielectric film, and the process of forming the 2nd sidewall that consists of an oxidation-resistant film so that the 1st sidewall may be covered (e).

[0024]By this composition, the poor resisting pressure and reliability degradation by the film decrease and damage to high dielectric gate dielectric film can be controlled. Since an ultra-thin SiO₂ film is not formed in Si interface at a next process, decline in the high specific inductive capacity of high dielectric gate dielectric film can be prevented.

[0025]As for the upper part of the 2nd sidewall, in the manufacturing method of the above-mentioned semiconductor device, it is preferred to have combined with the side attachment wall of a cap film.

[0026]In the manufacturing method of the above-mentioned semiconductor device, it is preferred that gate dielectric film and the 1st sidewall consist of the same dielectric film.

[0027]

[Mode for carrying out the invention](A 1st embodiment) A 1st embodiment of this invention is described hereafter, referring to Drawings. Drawing 1 is a sectional view showing the manufacturing process of the semiconductor device which functions as a n type MOSFET concerning a 1st embodiment of this invention.

[0028]The high dielectric gate dielectric film in which the Si substrate of a p type [1] and 2 consist of a ZrO_2 film in drawing 1, The gate electrode which consists of a poly Si film of a n type [3], the LDD diffusion layer of a n type [4], the 1st sidewall which 5 becomes from a ZrO_2 film (insulator layer), and 6 are silicon nitride films (it is an oxidation-resistant film and). The 2nd sidewall that consists of calling it an Si_3N_4 film below, and 7 are n^+ type source drain diffusion layers.

[0029]First, as shown in drawing 1 (A), after forming an element isolation layer (not shown) on Si substrate 1 which has a field (100), Reactive sputtering is performed to the metal target which consists of Zr in the atmosphere of the mixed gas of argon gas and oxygen gas, and the ZrO_2 film 2 which turns into high dielectric gate dielectric film is formed by about 5-nm thickness on Si substrate 1. Then, after depositing a n type poly Si film in about 200-300-nm thickness on the ZrO_2 film 2 with a CVD method, RIE is performed for a resist film (not shown) on a mask, and the gate electrode 3 is formed on the ZrO_2 film 2. At this time, film decrease also of the ZrO_2 film 2 of a ground film is etched and carried out like a conventional example. Damage is produced on the surface of the ZrO_2 film 2 by an etching damage. After removing a resist film, the ion implantation of the arsenic is carried out for the gate electrode 3 to a mask, and n type LDD diffusion layer 4 is formed in the surface of Si substrate 1.

[0030]The ZrO_2 film which turns into an insulator layer so that reactive sputtering may be performed and the gate electrode 3 top may be covered like the above, as shown in drawing 1 (B) Next, after [for example,] depositing in about 20-100-nm thickness, The 1st sidewall 5 that performs RIE to this ZrO_2 film, and becomes the side of the gate electrode 3 from a ZrO_2 film is formed. At this time, the ZrO_2 film 2 of a ground film is also etched simultaneously, and is removed altogether. If it does in this way, since a

ZrO₂ film accumulates again on the ZrO₂ film 2 which carried out film decrease by etching, film decrease will be canceled in the edge lower part of the gate electrode 3. Damage to the surface of the ZrO₂ film 2 is also recovered by redeposition. Therefore, the poor resisting pressure of high dielectric gate dielectric film and reliability degradation can be controlled like the conventional example in which Gate Bird's Beak was formed.

[0031]As shown in drawing 1 (C), the Si₃N₄ film which turns into an oxidation-resistant film so that the gate electrode 3 top may be covered with a CVD method Next, after [for example,] depositing in about 50-200-nm thickness, The 2nd sidewall 6 is formed so that the 1st sidewall 5 that performed RIE to this Si₃N₄ film, and was provided in the side attachment wall of the gate electrode 3 may be covered. Since the side attachment wall of the gate electrode 3 is covered by the 2nd sidewall 6 that consists of an Si₃N₄ film if it does in this way, even if it performs heat treatment in atmosphere and the deposition of an insulator layer containing oxidation or oxygen gas after this process, an ultra-thin SiO₂ film is not formed in Si interface. Therefore, the decline in the high specific inductive capacity by formation of an ultra-thin SiO₂ film which becomes with a problem in the case of high dielectric gate dielectric film can be prevented.

[0032]Next, as shown in drawing 1 (D), the ion implantation of the arsenic is carried out for the gate electrode 3, the 1st sidewall 5, and the 2nd sidewall 6 to a mask, and the n⁺ type source drain diffusion layer 7 is formed in the surface of Si substrate 1. Finally, although use well-known technology and it is not illustrated, an interlayer insulation film, a contact hole, and metallic wiring are formed one by one on Si substrate 1, and MOSFET of a 1st embodiment is completed.

[0033]As mentioned above, since according to a 1st embodiment the 1st sidewall that becomes the side attachment wall from a ZrO₂ film is formed after forming the gate electrode 3, the poor resisting pressure and reliability degradation by the film decrease and damage to high dielectric gate dielectric film can be controlled. Since the 2nd sidewall 6 that consists of an Si₃N₄ film is formed so that the 1st sidewall 5 may be covered, an ultra-thin SiO₂ film is not formed in Si interface at a next process. That is,



decline in the high specific inductive capacity of high dielectric gate dielectric film can be prevented. Therefore, a semiconductor device which functions as an MOSFET which controlled the poor resisting pressure of high dielectric gate dielectric film and reliability degradation, and prevented decline in high specific inductive capacity, and a manufacturing method for the same are realizable.

[0034](Modification of a 1st embodiment) The modification of a 1st embodiment is explained hereafter, referring to Drawings. Drawing 2 is a sectional view showing the manufacturing process of n type MOSFET concerning the modification of a 1st embodiment. Although the component of drawing 2 is the same as drawing 1, the form of the 1st sidewall 5 and the 2nd sidewall 6 differs.

[0035]First, after depositing the ZrO_2 film which turns into an insulator layer so that the gate electrode 3 top may be covered as shown in drawing 2 (B), the 1st sidewall 5 that performs RIE to this ZrO_2 film, and becomes the side of the gate electrode 3 from a ZrO_2 film is formed. Here, unlike the form of drawing 1 (B), predetermined over-etching is performed, and it forms so that the upper part of the 1st sidewall 5 may become lower about at least 50 nm than the height of the gate electrode 3. Also in this case, the film decrease and damage to the ZrO_2 film 2 are also improved by the redeposition of a ZrO_2 film in the edge lower part of the gate electrode 3 like drawing 1 (B). Therefore, the poor resisting pressure of high dielectric gate dielectric film and reliability degradation can be controlled.

[0036]After depositing the Si_3N_4 film which turns into an oxidation-resistant film so that the gate electrode 3 top may be covered as shown in drawing 2 (C), the 2nd sidewall 6 is formed so that the 1st sidewall 5 that performed RIE to this Si_3N_4 film, and was provided in the side attachment wall of the gate electrode 3 may be covered. Also in this case, unlike the form of drawing 1 (C), the upper part of the 2nd sidewall 6 is formed thickly, and only the part in which the upper part of the 1st sidewall 5 is lower than the height of the gate electrode 3 becomes a thickness of about at least 50 nm. Even if it performs heat treatment in atmosphere and the deposition of an insulator layer which contain oxidation or oxygen gas after this process like drawing 1 (C) also in this

case, an ultra-thin SiO₂ film is not formed in Si interface. Therefore, the decline in the high specific inductive capacity by formation of an ultra-thin SiO₂ film which becomes with a problem in the case of high dielectric gate dielectric film can be prevented.

[0037]As mentioned above, since according to the modification of a 1st embodiment the same effect as a 1st embodiment is acquired and also the upper part of the 1st sidewall 5 is still lower than the height of the gate electrode 3, the upper part of the 2nd sidewall 6 is thickly formed compared with the case of a 1st embodiment. For this reason, even if the formation process of a sidewall varies, the side attachment wall of the gate electrode 3 can be certainly covered by the 2nd sidewall that consists of an oxidation-resistant film. Therefore, since an ultra-thin SiO₂ film is not formed in Si interface at a next process, decline in the high specific inductive capacity of high dielectric gate dielectric film can be certainly prevented rather than a 1st embodiment.

[0038](A 2nd embodiment) A 2nd embodiment of this invention is described hereafter, referring to Drawings. Drawing 3 is a sectional view showing the manufacturing process of the semiconductor device which functions as a n type MOSFET concerning a 2nd embodiment of this invention.

[0039]The high dielectric gate dielectric film in which the Si substrate of a p type [11] and 12 consist of a ZrO₂ film in drawing 3, The gate electrode which consists of a poly Si film of a n type [13], the LDD diffusion layer of a n type [14], The 1st sidewall which 15 becomes from a ZrO₂ film (insulator layer), the 2nd sidewall which 16 becomes from an Si₃N₄ film (oxidation-resistant film), and 17 are an n⁺ type source drain diffusion layer and a cap film in which 18 consists of an Si₃N₄ film (oxidation-resistant film).

[0040]First, as shown in drawing 3 (A), after forming an element isolation layer (not shown) on Si substrate 11 which has a field (100), Reactive sputtering is performed to the metal target which consists of Zr in the atmosphere of the mixed gas of argon gas and oxygen gas, and the ZrO₂ film 12 which turns into high dielectric gate dielectric film is formed by about 5-nm thickness on Si substrate 11. Then, a n type poly Si film is deposited in about 200-300-nm thickness on the ZrO₂ film 12 with a CVD method, The

Si₃N₄ film which turns into an oxidation-resistant film. Then, after [for example,] depositing in about 50-100-nm thickness, The cap film 18 which consists of the gate electrode 13 and Si₃N₄ film which perform RIE on a mask and become it from a n type poly Si film on the ZrO₂ film 12 about a resist film (not shown) is formed. At this time, film decrease also of the ZrO₂ film 12 of a ground film is etched and carried out. Damage is produced on the surface of the ZrO₂ film 12 by an etching damage. After removing a resist film, the ion implantation of the arsenic is carried out for the gate electrode 13 to a mask, and n type LDD diffusion layer 14 is formed in the surface of Si substrate 11.

[0041]The ZrO₂ film which turns into an insulator layer so that reactive sputtering may be performed and the gate electrode 13 and cap film 18 top may be covered like the above, as shown in drawing 3 (B). Next, after [for example,] depositing in about 20-100-nm thickness, The 1st sidewall 15 that performs RIE to this ZrO₂ film, and becomes only the side of the gate electrode 13 from a ZrO₂ film is formed. At this time, the ZrO₂ film 12 of a ground film is also etched simultaneously, and is removed altogether. If it does in this way, since a ZrO₂ film accumulates again on the ZrO₂ film 12 which carried out film decrease by etching, film decrease will be canceled in the edge lower part of the gate electrode 13. Damage to the surface of the ZrO₂ film 12 is also recovered by redeposition. Therefore, the poor resisting pressure of high dielectric gate dielectric film and reliability degradation can be controlled like the conventional example in which Gate Bird's Beak was formed.

[0042]As shown in drawing 3 (C), the Si₃N₄ film which turns into an oxidation-resistant film so that the gate electrode 13 top may be covered with a CVD method. Next, after [for example,] depositing in about 50-200-nm thickness, The 2nd sidewall 16 is formed so that the 1st sidewall 15 that performed RIE to this Si₃N₄ film, and was provided in the side attachment wall of the gate electrode 13 may be covered. Since the side attachment wall of the gate electrode 13 is covered by the 2nd sidewall 16 that consists of an Si₃N₄ film if it does in this way, even if it performs heat treatment in atmosphere and the deposition of an insulator layer containing oxidation or oxygen gas

after this process, an ultra-thin SiO_2 film is not formed in Si interface. Since diffusion of the oxidation seed which led the grain boundary of the poly Si film which constitutes the gate electrode 13 since it was covered with the cap film 18 in which the upper surface of the gate electrode 13 also consists of an Si_3N_4 film is prevented, an ultra-thin SiO_2 film is not formed in Si interface. Therefore, the decline in the high specific inductive capacity by formation of an ultra-thin SiO_2 film which becomes with a problem in the case of high dielectric gate dielectric film can be prevented.

[0043]Next, as shown in drawing 3 (D), the ion implantation of the arsenic is carried out for the gate electrode 13, the cap film 18, the 1st sidewall 15, and the 2nd sidewall 16 to a mask, and the n^+ type source drain diffusion layer 17 is formed in the surface of Si substrate 11. Finally, although use well-known technology and it is not illustrated, an interlayer insulation film, a contact hole, and metallic wiring are formed one by one on Si substrate 11, and MOSFET of a 2nd embodiment is completed.

[0044]As mentioned above, since according to a 2nd embodiment the 1st sidewall that becomes the side attachment wall from a ZrO_2 film is formed after forming the gate electrode 13, the poor resisting pressure and reliability degradation by the film decrease and damage to high dielectric gate dielectric film can be controlled. Since the cap film 18 which consists of an Si_3N_4 film, and the 2nd sidewall 16 that consists of an Si_3N_4 film so that the 1st sidewall 15 may be covered are formed so that the gate electrode 13 may be covered, An ultra-thin SiO_2 film is not formed in Si interface at a next process. That is, decline in the high specific inductive capacity of high dielectric gate dielectric film can be prevented. Therefore, a semiconductor device which functions as an MOSFET which controlled the poor resisting pressure of high dielectric gate dielectric film and reliability degradation, and prevented decline in high specific inductive capacity, and a manufacturing method for the same are realizable.

[0045]In the 1st - a 2nd embodiment, although the ZrO_2 film was used and explained to high dielectric gate dielectric film, even if it replaces with this and uses other high dielectric films, for example, a HfO_2 film, a Ta_2O_5 film, or an aluminum $_2\text{O}_3$ film, it cannot be overemphasized that the effect of this invention is acquired. Even if it uses the

silicate film which turns into high dielectric gate dielectric film from 3 element system compounds of a high dielectric and silicon, the effect of this invention is acquired.

[0046]Although formed by performing reactive sputtering [film / which turns into high dielectric gate dielectric film / ZrO_2] using Zr target, it may replace with this and may form by performing sputtering using a ZrO_2 target. Or it may form by performing CVD using liquid sources, such as organic compound of Zr, for example, $\text{C}_{16}\text{H}_{26}\text{HfO}_4$, and $\text{C}_{16}\text{H}_{40}\text{N}_4\text{Zr}$.

[0047]Although explained to the 1st sidewall using the same ZrO_2 film as high dielectric gate dielectric film, even if it replaces with this and uses other dielectric films, for example, TEOS film, BPSG films, or SiON films, the effect of this invention is acquired.

[0048]Although the poly Si film was used and explained to the gate electrode, even if it replaces with this and uses a metal gate or silicide gates, such as other conductive films, for example, W film, a TiN film, and a WSi_2 film, the effect of this invention is acquired. Or even if it uses polymetal gates, such as W/TiN / poly Si film, TiSi_2 / poly Si film, the effect of this invention is acquired.

[0049]

[Effect of the Invention]As explained above, since according to a semiconductor device of this invention, and a manufacturing method for the same the 1st sidewall that becomes the side attachment wall from a dielectric film is formed after forming a gate electrode, the poor resisting pressure and reliability degradation by the film decrease and damage to high dielectric gate dielectric film can be controlled. Since the 2nd sidewall that consists of an oxidation-resistant film is formed so that the 1st sidewall may be covered, an ultra-thin SiO_2 film is not formed in Si interface at a next process. That is, decline in the high specific inductive capacity of high dielectric gate dielectric film can be prevented. Therefore, a semiconductor device which functions as an MOSFET which controlled the poor resisting pressure of high dielectric gate dielectric film and reliability degradation, and prevented decline in high specific inductive capacity, and a manufacturing method for the same are realizable.

[Brief Description of the Drawings]

[Drawing 1](A) - (D) is a sectional view showing the manufacturing process of n type MOSFET in a 1st embodiment of this invention.

[Drawing 2](A) - (D) is a sectional view showing the manufacturing process of n type MOSFET in the modification of a 1st embodiment of this invention.

[Drawing 3](A) - (D) is a sectional view showing the manufacturing process of n type MOSFET in a 2nd embodiment of this invention.

[Drawing 4](A) - (D) is a sectional view showing the manufacturing process of the n type conventional MOSFET.

[Explanations of letters or numerals]

1, the Si substrate of 11 p types

High dielectric gate dielectric film which consists of a 2 and 12 ZrO_2 film

The gate electrode which consists of 3 and a poly Si film of 13 n types

4, the LDD diffusion layer of 14 n types

The 1st sidewall that consists of 5 and a 15 ZrO_2 film (insulator layer)

The 2nd sidewall that consists of 6 and a 16 Si_3N_4 film (oxidation-resistant film)

A 7 and 17 n^+ type source drain diffusion layer

18 The cap film which consists of an Si_3N_4 film (oxidation-resistant film)

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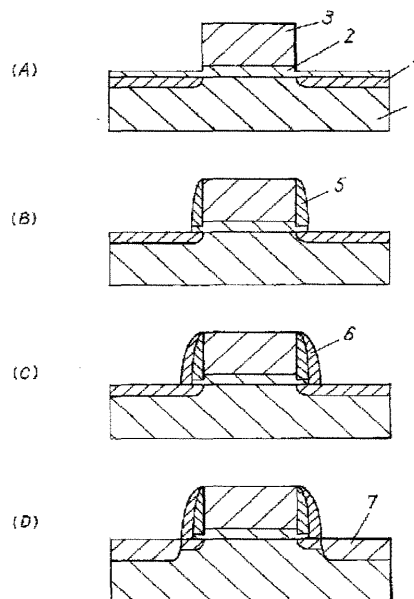
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(54)【発明の名称】 半導体装置およびその製造方法

(57)【要約】

【課題】 高誘電体ゲート絶縁膜の耐圧不良や信頼性劣化を抑制し、かつ高い比誘電率の低下を防止した半導体装置およびその製造方法を提供することを目的とする。

【解決手段】 ゲート電極を形成した後にその側壁に誘電体膜からなる第1のサイドウォールが形成されるので、高誘電体ゲート絶縁膜の膜減りや損傷による耐圧不良や信頼性劣化を抑制できる。さらに、第1のサイドウォールを覆うように耐酸化性膜からなる第2のサイドウォールが形成されるので、後の工程でS i 界面に極薄のS i O₂膜が形成されることはない。すなわち、高誘電体ゲート絶縁膜の高い比誘電率の低下を防止することができる。



【特許請求の範囲】

【請求項1】 MOSFETとして機能する半導体装置において、

半導体基板上に形成された高誘電体膜からなるゲート絶縁膜と、前記ゲート絶縁膜上に形成された導電性膜からなるゲート電極と、前記ゲート電極の側壁に形成された誘電体膜からなる第1のサイドウォールと、前記第1のサイドウォールを覆うように形成された耐酸化性膜からなる第2のサイドウォールとを備えたことを特徴とする半導体装置。

【請求項2】 前記第1のサイドウォールの上部は、前記ゲート電極の高さよりも低いことを特徴とする請求項1に記載の半導体装置。

【請求項3】 前記ゲート絶縁膜と前記第1のサイドウォールとが同一の誘電体膜からなることを特徴とする請求項1または2に記載の半導体装置。

【請求項4】 前記ゲート電極上に形成された耐酸化性膜からなるキャップ膜とをさらに備えたことを特徴とする請求項1～3の何れか1項に記載の半導体装置。

【請求項5】 MOSFETとして機能する半導体装置の製造方法において、
半導体基板上に高誘電体膜からなるゲート絶縁膜を形成する工程（a）と、
前記ゲート絶縁膜上に導電性膜からなるゲート電極を形成する工程（b）と、
前記ゲート電極の側壁に誘電体膜からなる第1のサイドウォールを形成する工程（c）と、
前記第1のサイドウォールを覆うように耐酸化性膜からなる第2のサイドウォールを形成する工程（d）とを備えたことを特徴とする半導体装置の製造方法。

【請求項6】 前記第1のサイドウォールの上部は、前記ゲート電極の高さよりも低くなるように形成することを特徴とする請求項5に記載の半導体装置の製造方法。

【請求項7】 前記ゲート絶縁膜と前記第1のサイドウォールとが同一の誘電体膜からなることを特徴とする請求項5または6に記載の半導体装置の製造方法。

【請求項8】 MOSFETとして機能する半導体装置の製造方法において、

半導体基板上に高誘電体膜からなるゲート絶縁膜を形成する工程（a）と、

前記ゲート絶縁膜上に導電性膜と耐酸化性膜とを順次堆積する工程（b）と、

前記耐酸化性膜上にエッチングマスクを設けて前記耐酸化性膜と前記導電性膜とを順次エッチングしてキャップ膜とゲート電極とを形成する工程（c）と、

前記ゲート電極の側壁にのみ誘電体膜からなる第1のサイドウォールを形成する工程（d）と、

前記第1のサイドウォールを覆うように耐酸化性膜からなる第2のサイドウォールを形成する工程（e）とを備えたことを特徴とする半導体装置の製造方法。

【請求項9】 前記第2のサイドウォールの上部は、前記キャップ膜の側壁に結合していることを特徴とする請求項8に記載の半導体装置の製造方法。

【請求項10】 前記ゲート絶縁膜と前記第1のサイドウォールとが同一の誘電体膜からなることを特徴とする請求項8または9に記載の半導体装置の製造方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、半導体装置およびその製造方法に関し、特に高誘電体（高誘電率材料）からなるゲート絶縁膜を有する絶縁ゲート型の電界効果トランジスタに関する。

【0002】

【従来の技術】近年、半導体プロセスの加工技術の進展によりシリコン酸化膜（以下、SiO₂膜と言う）を用いた絶縁ゲート型の電界効果トランジスタ（以下、MOSFETと言う）の微細化が進んでいる。しかし、MOSFETの比例縮小に伴ってゲート絶縁膜の薄膜化を進めると、トンネル電流によるゲートリーク電流の増大が問題になる。この問題を回避するために、ジルコニウム酸化膜（以下、ZrO₂膜と言う）等を用いた高誘電体からなるゲート絶縁膜（以下、高誘電体ゲート絶縁膜と言う）を有するMOSFETの研究が行われている。一方、素子の縮小に伴ってゲート電極の微細加工を進めると、異方性を実現する反応性イオンエッチング（以下、RIEと言う）により、ゲート電極の下地にあるゲート絶縁膜に膜減りや損傷が生じる。これが原因となって、ゲート絶縁膜の耐圧不良や信頼性劣化が発生する。この問題を改善するために、従来のMOSFETでは、ゲート電極を形成した後にシリコン基板を再酸化してゲート電極のエッジ下部にバースピーク（以下、ゲートバースピークと言う）を形成する。このようなゲートバースピークを有するMOSFETには、特開平6-204237号に記載されたものが知られている。

【0003】以下、従来のゲートバースピークを有するMOSFETの構造とその製造方法について図面を参照しながら説明する。図4は、従来のn型のMOSFETの製造工程を示す断面図である。

【0004】図4において、21はp型のシリコン単結晶からなる半導体基板（以下、Si基板と言う）、22はSiO₂膜からなるゲート絶縁膜、23はn型の多結晶シリコン膜（以下、ポリSi膜と言う）からなるゲート電極、24はn型のLDD拡散層、25は一端がゲートバースピークになるSiO₂膜、26はTEOS膜からなるサイドウォール、27はn型のソース・ドレイン拡散層である。

【0005】まず、図4（A）に示すように、（100）面を有するp型のシリコン単結晶からなるSi基板21上に素子分離層（図示せず）を形成した後、Si基板21を熱酸化してゲート絶縁膜になるSiO₂膜22

を形成する。その後、CVD法により SiO_2 膜22上にn型のポリ Si 膜を堆積した後、レジスト膜（図示せず）をマスクにRIEを行ってゲート電極23を形成する。この時、下地膜の SiO_2 膜22もエッチングされて膜減りする。また、エッチングダメージにより SiO_2 膜22の表面に損傷を生ずる。レジスト膜を除去した後、ゲート電極23をマスクに例えばヒ素をイオン注入して Si 基板21の表面にn型のLDD拡散層24を形成する。

【0006】次に、図4（B）に示すように、 Si 基板21を再度熱酸化してLDD拡散層24上に SiO_2 膜25を形成すると、ゲート電極23のエッジ下部にゲートバースピークが形成される。このようにすると、エッチングで膜減りした SiO_2 膜22が再酸化されて厚い SiO_2 膜25に変わる。また、 SiO_2 膜22の表面の損傷も再酸化によって回復される。したがって、ゲート絶縁膜の耐圧不良や信頼性劣化を抑制できる。

【0007】次に、図4（C）に示すように、CVD法によりゲート電極23上を覆うようにTEOS膜を堆積した後、このTEOS膜に対してRIEを行ってゲート電極23の側壁にサイドウォール26を形成する。

【0008】次に、図4（D）に示すように、ゲート電極23とサイドウォール26をマスクに例えばヒ素をイオン注入して Si 基板21の表面にn型のソース・ドレイン拡散層27を形成する。最後に、周知の技術を用いて、図示していないが Si 基板21上に層間絶縁膜、コンタクトホールおよび金属配線を順次形成して、従来のMOSFETが完成する。

【0009】以上のように、ゲートバースピークを形成することによりゲートリーク電流の増加を抑制し、耐圧不良や信頼性劣化の発生しないMOSFETを実現している。

【0010】

【発明が解決しようとする課題】しかしながら、従来の構成は SiO_2 膜を用いたMOSFETには適用できるが、以下の理由から ZrO_2 膜等からなる高誘電体ゲート絶縁膜を用いたMOSFETには適用できなかった。

【0011】ゲートバースピークを形成する酸化工程において、酸化種（酸素等）がゲート電極のエッジ下部から ZrO_2 膜または Si 基板との界面に浸入し、さらに膜中や界面を拡散し、ゲート電極下の Si 基板を酸化して薄い SiO_2 膜が形成される。これによって、ゲート絶縁膜は実質的に ZrO_2 膜と薄い SiO_2 膜の積層膜になるので、ゲート絶縁膜全体の比誘電率は元々の ZrO_2 膜に比べて低下してしまう。例えば、比誘電率が15～20で膜厚が5.0nmの ZrO_2 膜を形成した後にゲートバースピークを形成すると、界面に比誘電率が3.9で膜厚が0.2～0.3nmの薄い SiO_2 膜が形成される。この場合、ゲート絶縁膜全体の比誘電率は13～17で、膜厚は5.2～5.3nmになる。すな

わち、ゲート絶縁膜全体の膜厚増加は5%程度にすぎないが、比誘電率は14%程度も低下するので、結果としてMOSFETの電流能力は大幅に低下する。また、ゲート電極のエッジ下部にはくさび状に厚い SiO_2 膜が形成されるので、実効的なゲート長は変化してMOSFETの閾値電圧は変動する。このように、高誘電体ゲート絶縁膜を用いたMOSFETにゲートバースピークを形成すると、MOSFETの電気特性が劣化または変動するという問題があった。

【0012】また、ゲートバースピークを形成しない場合でも、ゲート電極を形成した後に酸化または酸素ガスを含む雰囲気での熱処理や絶縁膜の堆積を行うと、ゲートバースピークを形成する場合と同様に、 Si 界面に極薄の SiO_2 膜が形成されるのでゲート絶縁膜全体の比誘電率は低下してしまう。したがって、この場合にも高誘電体ゲート絶縁膜を用いたMOSFETの電気特性が劣化するという問題があった。

【0013】本発明は、上記の問題点を鑑みてなされたものであって、高誘電体ゲート絶縁膜の耐圧不良や信頼性劣化を抑制し、かつ高い比誘電率の低下を防止した半導体装置およびその製造方法を提供することを目的とする。

【0014】

【課題を解決するための手段】上記の目的を達成するために、本発明の半導体装置は、MOSFETとして機能する半導体装置において、半導体基板上に形成された高誘電体膜からなるゲート絶縁膜と、ゲート絶縁膜上に形成された導電性膜からなるゲート電極と、ゲート電極の側壁に形成された誘電体膜からなる第1のサイドウォールと、第1のサイドウォールを覆うように形成された耐酸化性膜からなる第2のサイドウォールとを備えたことを特徴とする。

【0015】この構成によって、高誘電体ゲート絶縁膜の膜減りや損傷による耐圧不良や信頼性劣化を抑制できる。さらに、後の工程で Si 界面に極薄の SiO_2 膜が形成されることがないので、高誘電体ゲート絶縁膜の高い比誘電率の低下を防止することができる。

【0016】上記の半導体装置において、第1のサイドウォールの上部は、ゲート電極の高さよりも低いことが好ましい。

【0017】上記の半導体装置において、ゲート絶縁膜と第1のサイドウォールとが同一の誘電体膜からなることが好ましい。

【0018】上記の半導体装置において、ゲート電極上に形成された耐酸化性膜からなるキャップ膜とをさらに備えたことが好ましい。

【0019】また、本発明の半導体装置の製造方法は、MOSFETとして機能する半導体装置の製造方法において、半導体基板上に高誘電体膜からなるゲート絶縁膜を形成する工程（a）と、ゲート絶縁膜上に導電性膜か

らなるゲート電極を形成する工程（b）と、ゲート電極の側壁に誘電体膜からなる第1のサイドウォールを形成する工程（c）と、第1のサイドウォールを覆うように耐酸化性膜からなる第2のサイドウォールを形成する工程（d）とを備えたことを特徴とする。

【0020】この構成によって、高誘電体ゲート絶縁膜の膜減りや損傷による耐圧不良や信頼性劣化を抑制できる。さらに、後の工程でSi界面に極薄のSiO₂膜が形成されることがないので、高誘電体ゲート絶縁膜の高い比誘電率の低下を防止することができる。

【0021】上記の半導体装置の製造方法において、第1のサイドウォールの上部は、ゲート電極の高さよりも低くなるように形成することが好ましい。

【0022】上記の半導体装置の製造方法において、ゲート絶縁膜と第1のサイドウォールとが同一の誘電体膜からなることが好ましい。

【0023】さらに、本発明の半導体装置の製造方法は、MOSFETとして機能する半導体装置の製造方法において、半導体基板上に高誘電体膜からなるゲート絶縁膜を形成する工程（a）と、ゲート絶縁膜上に導電性膜と耐酸化性膜とを順次堆積する工程（b）と、耐酸化性膜上にエッチングマスクを設けて耐酸化性膜と導電性膜とを順次エッチングしてキャップ膜とゲート電極とを形成する工程（c）と、ゲート電極の側壁にのみ誘電体膜からなる第1のサイドウォールを形成する工程（d）と、第1のサイドウォールを覆うように耐酸化性膜からなる第2のサイドウォールを形成する工程（e）とを備えたことを特徴とする。

【0024】この構成によって、高誘電体ゲート絶縁膜の膜減りや損傷による耐圧不良や信頼性劣化を抑制できる。さらに、後の工程でSi界面に極薄のSiO₂膜が形成されることがないので、高誘電体ゲート絶縁膜の高い比誘電率の低下を防止することができる。

【0025】上記の半導体装置の製造方法において、第2のサイドウォールの上部は、キャップ膜の側壁に結合していることが好ましい。

【0026】上記の半導体装置の製造方法において、ゲート絶縁膜と第1のサイドウォールとが同一の誘電体膜からなることが好ましい。

【0027】

【発明の実施形態】（第1の実施形態）以下、本発明の第1の実施形態について、図面を参照しながら説明する。図1は、本発明の第1の実施形態に係るn型のMOSFETとして機能する半導体装置の製造工程を示す断面図である。

【0028】図1において、1はp型のSi基板、2はZrO₂膜からなる高誘電体ゲート絶縁膜、3はn型のポリSi膜からなるゲート電極、4はn型のLDD拡散層、5はZrO₂膜（絶縁膜）からなる第1のサイドウォール、6はシリコン窒化膜（耐酸化性膜で、以下Si

3N₄膜と言う）からなる第2のサイドウォール、7はn⁺型のソース・ドレイン拡散層である。

【0029】まず、図1（A）に示すように、（100）面を有するSi基板1上に素子分離層（図示せず）を形成した後、アルゴンガスと酸素ガスとの混合ガスの雰囲気においてZrからなる金属ターゲットに対して反応性スパッタリングを行って、Si基板1上に高誘電体ゲート絶縁膜になるZrO₂膜2を例えば5nm程度の膜厚で形成する。その後、CVD法によりZrO₂膜2上にn型のポリSi膜を例えば200～300nm程度の膜厚で堆積した後、レジスト膜（図示せず）をマスクにRIEを行ってZrO₂膜2上にゲート電極3を形成する。この時、従来例と同様にして、下地膜のZrO₂膜2もエッチングされて膜減りする。また、エッチングダメージによりZrO₂膜2の表面に損傷を生ずる。レジスト膜を除去した後、ゲート電極3をマスクに例えばヒ素をイオン注入してSi基板1の表面にn型のLDD拡散層4を形成する。

【0030】次に、図1（B）に示すように、上記と同様にして、反応性スパッタリングを行ってゲート電極3上を覆うように絶縁膜になるZrO₂膜を例えば20～100nm程度の膜厚で堆積した後、このZrO₂膜に対してRIEを行ってゲート電極3の側面にZrO₂膜からなる第1のサイドウォール5を形成する。この時、下地膜のZrO₂膜2も同時にエッチングしてすべて除去する。このようにすると、ゲート電極3のエッジ下部ではエッチングにより膜減りしたZrO₂膜2上に再びZrO₂膜が堆積されるので膜減りは解消される。また、ZrO₂膜2の表面の損傷も再堆積によって回復される。したがって、ゲートバズビークを形成した従来例と同様にして、高誘電体ゲート絶縁膜の耐圧不良や信頼性劣化を抑制できる。

【0031】次に、図1（C）に示すように、CVD法によりゲート電極3上を覆うように耐酸化性膜になるSi₃N₄膜を例えば50～200nm程度の膜厚で堆積した後、このSi₃N₄膜に対してRIEを行ってゲート電極3の側壁に設けた第1のサイドウォール5を覆うように第2のサイドウォール6を形成する。このようにすると、ゲート電極3の側壁はSi₃N₄膜からなる第2のサイドウォール6で覆われているので、この工程の後に酸化または酸素ガスを含む雰囲気での熱処理や絶縁膜の堆積を行っても、Si界面に極薄のSiO₂膜が形成されることはない。したがって、高誘電体ゲート絶縁膜の場合に問題となる、極薄のSiO₂膜の形成による高い比誘電率の低下を防止することができる。

【0032】次に、図1（D）に示すように、ゲート電極3、第1のサイドウォール5および第2のサイドウォール6をマスクに例えばヒ素をイオン注入してSi基板1の表面にn⁺型のソース・ドレイン拡散層7を形成する。最後に、周知の技術を用いて、図示していないがS

i 基板 1 上に層間絶縁膜、コンタクトホールおよび金属配線を順次形成して、第 1 の実施形態の MOSFET が完成する。

【0033】 以上のように、第 1 の実施形態によると、ゲート電極 3 を形成した後にその側壁に ZrO_2 膜からなる第 1 のサイドウォールが形成されるので、高誘電体ゲート絶縁膜の膜減りや損傷による耐圧不良や信頼性劣化を抑制できる。さらに、第 1 のサイドウォール 5 を覆うように Si_3N_4 膜からなる第 2 のサイドウォール 6 が形成されるので、後の工程で Si 界面に極薄の SiO_2 膜が形成されることはない。すなわち、高誘電体ゲート絶縁膜の高い比誘電率の低下を防止することができる。したがって、高誘電体ゲート絶縁膜の耐圧不良や信頼性劣化を抑制し、かつ高い比誘電率の低下を防止した MOSFET として機能する半導体装置およびその製造方法を実現することができる。

【0034】 (第 1 の実施形態の変形例) 以下、第 1 の実施形態の変形例について、図面を参照しながら説明する。図 2 は、第 1 の実施形態の変形例に係る n 型の MOSFET の製造工程を示す断面図である。図 2 の構成要素は図 1 と同じであるが、第 1 のサイドウォール 5 と第 2 のサイドウォール 6 の形状が異なっている。

【0035】 まず、図 2 (B) に示すように、ゲート電極 3 上を覆うように絶縁膜になる ZrO_2 膜を堆積した後、この ZrO_2 膜に対して RIE を行ってゲート電極 3 の側面に ZrO_2 膜からなる第 1 のサイドウォール 5 を形成する。ここでは、図 1 (B) の形状とは異なり、所定のオーバーエッチを行って第 1 のサイドウォール 5 の上部がゲート電極 3 の高さよりも少なくとも 50 nm 程度低くなるように形成する。この場合も図 1 (B) と同様にして、ゲート電極 3 のエッジ下部では ZrO_2 膜の再堆積により ZrO_2 膜 2 の膜減りや損傷も改善される。したがって、高誘電体ゲート絶縁膜の耐圧不良や信頼性劣化を抑制できる。

【0036】 また、図 2 (C) に示すように、ゲート電極 3 上を覆うように耐酸化性膜になる Si_3N_4 膜を堆積した後、この Si_3N_4 膜に対して RIE を行ってゲート電極 3 の側壁に設けた第 1 のサイドウォール 5 を覆うように第 2 のサイドウォール 6 を形成する。この場合も、図 1 (C) の形状とは異なり、第 1 のサイドウォール 5 の上部がゲート電極 3 の高さよりも低い分だけ第 2 のサイドウォール 6 の上部が厚く形成され、少なくとも 50 nm 程度の厚みになる。この場合も図 1 (C) と同様にして、この工程の後に酸化または酸素ガスを含む雰囲気での熱処理や絶縁膜の堆積を行っても、 Si 界面に極薄の SiO_2 膜が形成されることはない。したがって、高誘電体ゲート絶縁膜の場合に問題となる、極薄の SiO_2 膜の形成による高い比誘電率の低下を防止することができる。

【0037】 以上のように、第 1 の実施形態の変形例に

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よると、第 1 の実施形態と同じ効果が得られる上、さらに、第 1 のサイドウォール 5 の上部はゲート電極 3 の高さよりも低いので、第 2 のサイドウォール 6 の上部は第 1 の実施形態の場合に比べて厚く形成される。このため、サイドウォールの形成工程がばらついても、確実にゲート電極 3 の側壁は耐酸化性膜からなる第 2 のサイドウォールで覆うことができる。したがって、後の工程で Si 界面に極薄の SiO_2 膜が形成されることはないの

で、第 1 の実施形態よりも確実に高誘電体ゲート絶縁膜の高い比誘電率の低下を防止することができる。

【0038】 (第 2 の実施形態) 以下、本発明の第 2 の実施形態について、図面を参照しながら説明する。図 3 は、本発明の第 2 の実施形態に係る n 型の MOSFET として機能する半導体装置の製造工程を示す断面図である。

【0039】 図 3 において、11 は p 型の Si 基板、12 は ZrO_2 膜からなる高誘電体ゲート絶縁膜、13 は n 型のポリ Si 膜からなるゲート電極、14 は n 型の LDD 拡散層、15 は ZrO_2 膜 (絶縁膜) からなる第 1 のサイドウォール、16 は Si_3N_4 膜 (耐酸化性膜) からなる第 2 のサイドウォール、17 は n 型のソース・ドレイン拡散層、18 は Si_3N_4 膜 (耐酸化性膜) からなるキャップ膜である。

【0040】 まず、図 3 (A) に示すように、(100) 面を有する Si 基板 11 上に素子分離層 (図示せず) を形成した後、アルゴンガスと酸素ガスとの混合ガスの雰囲気において Zr からなる金属ターゲットに対して反応性スパッタリングを行って、 Si 基板 11 上に高誘電体ゲート絶縁膜になる ZrO_2 膜 12 を例えば 5 nm 程度の膜厚で形成する。その後、CVD 法により ZrO_2 膜 12 上に n 型のポリ Si 膜を例えば 200 ~ 300 nm 程度の膜厚で堆積し、続いて耐酸化性膜になる Si_3N_4 膜を例えば 50 ~ 100 nm 程度の膜厚で堆積した後、レジスト膜 (図示せず) をマスクに RIE を行って ZrO_2 膜 12 上に n 型のポリ Si 膜からなるゲート電極 13 と Si_3N_4 膜からなるキャップ膜 18 とを形成する。この時、下地膜の ZrO_2 膜 12 もエッチングされて膜減りする。また、エッチングダメージにより ZrO_2 膜 12 の表面に損傷を生ずる。レジスト膜を除去した後、ゲート電極 13 をマスクに例えばヒ素をイオン注入して Si 基板 11 の表面に n 型の LDD 拡散層 14 を形成する。

【0041】 次に、図 3 (B) に示すように、上記と同様にして、反応性スパッタリングを行ってゲート電極 13 とキャップ膜 18 上を覆うように絶縁膜になる ZrO_2 膜を例えば 20 ~ 100 nm 程度の膜厚で堆積した後、この ZrO_2 膜に対して RIE を行ってゲート電極 13 の側面にのみ ZrO_2 膜からなる第 1 のサイドウォール 15 を形成する。この時、下地膜の ZrO_2 膜 12 も同時にエッチングしてすべて除去する。このようにす

ると、ゲート電極13のエッジ下部ではエッチングにより膜減りしたZrO₂膜12上に再びZrO₂膜が堆積されるので膜減りは解消される。また、ZrO₂膜12の表面の損傷も再堆積によって回復される。したがって、ゲートバースピークを形成した従来例と同様にして、高誘電体ゲート絶縁膜の耐圧不良や信頼性劣化を抑制できる。

【0042】次に、図3(C)に示すように、CVD法によりゲート電極13上を覆うように耐酸化性膜になるSi₃N₄膜を例えば50～200nm程度の膜厚で堆積した後、このSi₃N₄膜に対してRIEを行ってゲート電極13の側壁に設けた第1のサイドウォール15を覆うように第2のサイドウォール16を形成する。このようにすると、ゲート電極13の側壁はSi₃N₄膜からなる第2のサイドウォール16で覆われているので、この工程の後に酸化または酸素ガスを含む雰囲気での熱処理や絶縁膜の堆積を行っても、Si界面に極薄のSiO₂膜が形成されることはない。また、ゲート電極13の上面もSi₃N₄膜からなるキャップ膜18で覆われているので、ゲート電極13を構成するポリSi膜の粒界を通じた酸化種の拡散を防止するので、Si界面に極薄のSiO₂膜が形成されることはない。したがって、高誘電体ゲート絶縁膜の場合に問題となる、極薄のSiO₂膜の形成による高い比誘電率の低下を防止することができる。

【0043】次に、図3(D)に示すように、ゲート電極13、キャップ膜18、第1のサイドウォール15および第2のサイドウォール16をマスクに例えばヒ素をイオン注入してSi基板11の表面にn⁺型のソース・ドレイン拡散層17を形成する。最後に、周知の技術を用いて、図示していないがSi基板11上に層間絶縁膜、コンタクトホールおよび金属配線を順次形成して、第2の実施形態のMOSFETが完成する。

【0044】以上のように、第2の実施形態によると、ゲート電極13を形成した後にその側壁にZrO₂膜からなる第1のサイドウォールが形成されるので、高誘電体ゲート絶縁膜の膜減りや損傷による耐圧不良や信頼性劣化を抑制できる。さらに、ゲート電極13を覆うようにSi₃N₄膜からなるキャップ膜18と、第1のサイドウォール15を覆うようにSi₃N₄膜からなる第2のサイドウォール16とが形成されるので、後の工程でSi界面に極薄のSiO₂膜が形成されることはない。すなわち、高誘電体ゲート絶縁膜の高い比誘電率の低下を防止することができる。したがって、高誘電体ゲート絶縁膜の耐圧不良や信頼性劣化を抑制し、かつ高い比誘電率の低下を防止したMOSFETとして機能する半導体装置およびその製造方法を実現することができる。

【0045】なお、第1～第2の実施形態において、高誘電体ゲート絶縁膜にZrO₂膜を用いて説明したが、これに代えて他の高誘電体膜、例えばHfO₂膜、Ta₂O₅膜

O₅膜またはAl₂O₃膜を用いても本発明の効果が得られるのは言うまでもない。さらに、高誘電体ゲート絶縁膜に高誘電体とシリコンの3元系化合物からなるシリケート膜を用いても本発明の効果は得られる。

【0046】また、高誘電体ゲート絶縁膜になるZrO₂膜をZrターゲットを用いた反応性スパッタリングを行って形成したが、これに代えてZrO₂ターゲットを用いたスパッタリングを行って形成しても良い。あるいは、Zrの有機化合物、例えばC₁₆H₂₆HfO₄、C₁₆H₄₀N₄Zr等の液体ソースを用いたCVDを行って形成しても良い。

【0047】また、第1のサイドウォールに高誘電体ゲート絶縁膜と同じZrO₂膜を用いて説明したが、これに代えて他の誘電体膜、例えばTEOS膜、BPSG膜またはSiON膜を用いても本発明の効果は得られる。

【0048】さらに、ゲート電極にポリSi膜を用いて説明したが、これに代えて他の導電性膜、例えばW膜、TiN膜、WSi₂膜等のメタルゲートまたはシリサイドゲートを用いても本発明の効果は得られる。あるいは、W/TiN/ポリSi膜、TiSi₂/ポリSi膜等のポリメタルゲートを用いても本発明の効果は得られる。

【0049】

【発明の効果】以上説明したように、本発明の半導体装置およびその製造方法によれば、ゲート電極を形成した後にその側壁に誘電体膜からなる第1のサイドウォールが形成されるので、高誘電体ゲート絶縁膜の膜減りや損傷による耐圧不良や信頼性劣化を抑制できる。さらに、第1のサイドウォールを覆うように耐酸化性膜からなる第2のサイドウォールが形成されるので、後の工程でSi界面に極薄のSiO₂膜が形成されることはない。すなわち、高誘電体ゲート絶縁膜の高い比誘電率の低下を防止することができる。したがって、高誘電体ゲート絶縁膜の耐圧不良や信頼性劣化を抑制し、かつ高い比誘電率の低下を防止したMOSFETとして機能する半導体装置およびその製造方法を実現することができる。

【図面の簡単な説明】

【図1】(A)～(D)は本発明の第1の実施形態におけるn型のMOSFETの製造工程を示す断面図

【図2】(A)～(D)は本発明の第1の実施形態の変形例におけるn型のMOSFETの製造工程を示す断面図

【図3】(A)～(D)は本発明の第2の実施形態におけるn型のMOSFETの製造工程を示す断面図

【図4】(A)～(D)は従来のn型のMOSFETの製造工程を示す断面図

【符号の説明】

- 1、11 p型のSi基板
- 2、12 ZrO₂膜からなる高誘電体ゲート絶縁膜
- 3、13 n型のポリSi膜からなるゲート電極

4、14 n型のLDD拡散層

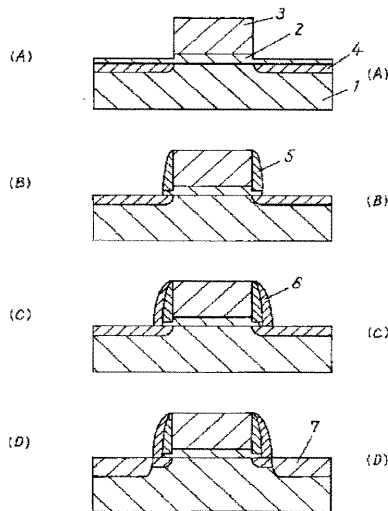
* イドウォール

5、15 ZrO_2 膜(絶縁膜)からなる第1のサイドウォール

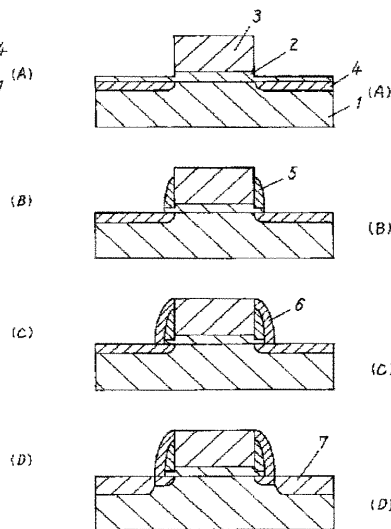
7、17 n'型のソース・ドレイン拡散層

6、16 Si_3N_4 膜(耐酸性膜)からなる第2のサ*18 Si_3N_4 膜(耐酸性膜)からなるキャップ膜

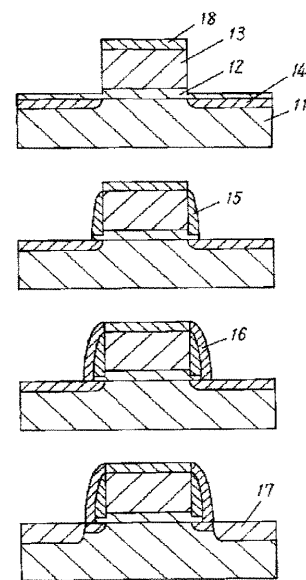
【図1】



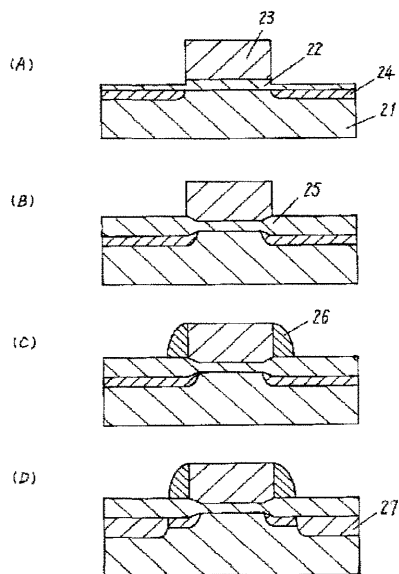
【図2】



【図3】



【図4】



フロントページの続き

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Junji HIRASE, et al.	:	Confirmation Number: 7641
	:	
Application No.: 13/037,831	:	Group Art Unit: 2892
	:	
Filed: March 01, 2011	:	Examiner: LUU, CHUONG A.
	:	
For: SEMICONDUCTOR DEVICE	:	

INFORMATION DISCLOSURE STATEMENT

Mail Stop IDS - Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection or Notice of Allowance.

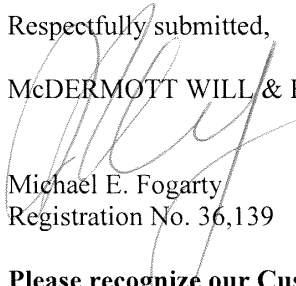
CERTIFICATION PARAGRAPH

The undersigned certifies that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in any counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement as described in 37 CFR 1.97(e)(1).

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP


Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:kaw
Facsimile: 202.756.8087
Date: January 6, 2012

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/037,831	03/01/2011	Junji HIRASE	085393-0499	7641
53080	7590	01/12/2012		
MCDERMOTT WILL & EMERY LLP 600 13TH STREET, NW WASHINGTON, DC 20005-3096			EXAMINER LUU, CHUONG A	
			ART UNIT	PAPER NUMBER
			2892	
			NOTIFICATION DATE	DELIVERY MODE
			01/12/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mweipdocket@mwe.com

Office Action Summary	Application No.	Applicant(s)	
	13/037,831	HIRASE ET AL.	
	Examiner	Art Unit	
	CHUONG LUU	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 November 2011.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 5) ☒ Claim(s) 21-42 is/are pending in the application.
- 5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 21-42 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 12) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☐ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: ____. |
| 3) ☒ Information Disclosure Statement(s) (PTO/SB/08) | 5) ☐ Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>10/27/2011</u> . | 6) ☐ Other: ____. |

DETAILED ACTION

REJECTIONS BASED UPON PRIOR ARTS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The Rejections

Claim 21 is rejected under 35 U.S.C. 102(e) as being anticipated by Hieda et al. (U.S. 6,992,358).

Hieda discloses a semiconductor device with

(21) a high dielectric constant gate insulating film (102-oxide) formed on an active region in a substrate (101);

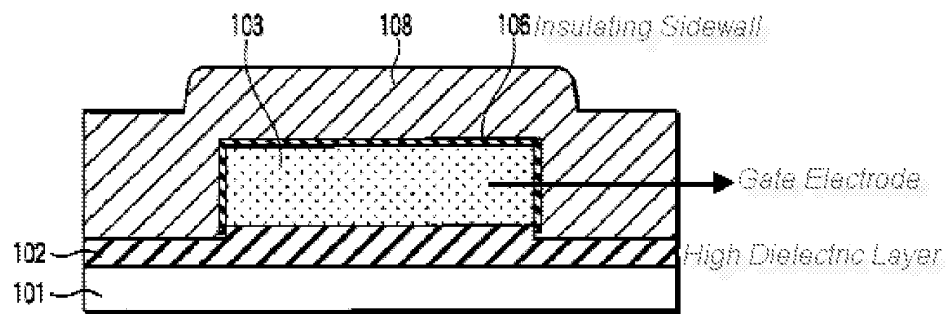
a gate electrode (103) formed on the high dielectric constant gate insulating film (102-oxide);

an insulating sidewall (106) formed on each side surface of the gate electrode (103),

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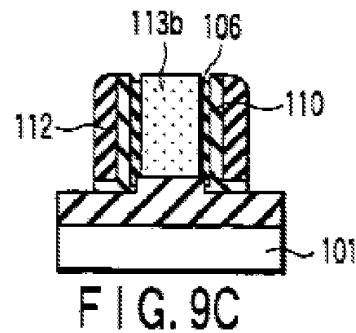
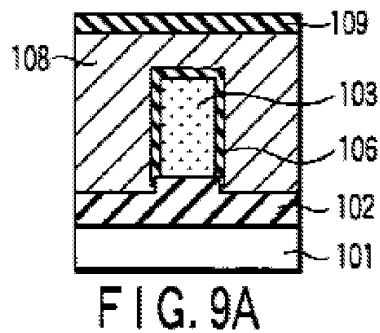
wherein the high dielectric constant gate insulating film (102-oxide) is continuously formed so as to extend from under the gate electrode (103) to under the insulating sidewall (106), and

at least part of the high dielectric constant gate insulating film (102-oxide) located under the insulating sidewall (106) has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film (102-oxide) located under the gate electrode (103) (see Figure 5B);

**FIG. 5B**

Claim 21 is rejected under 35 U.S.C. 102(e) as being anticipated by Hieda et al. (U.S. 6,992,358).

Hieda discloses, as shown in Figures 9A and 9C, a semiconductor device with



(21) a high dielectric constant gate insulating film (102-oxide) formed on an active region in a substrate (101);

a gate electrode (103) formed on the high dielectric constant gate insulating film (102-oxide);

a first insulating sidewall (106) formed on each side surface of the gate electrode (103),

a second insulating sidewall (110) formed on each side surface of the gate electrode (103) with the first insulating sidewall (106) interposed therebetween;

wherein the high dielectric constant gate insulating film (102-oxide) is continuously formed so as to extend from under the gate electrode (103) to under the first insulating sidewall (106), and

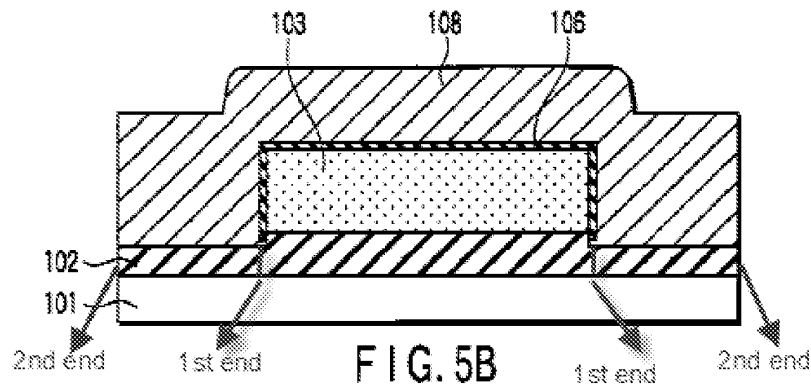
part of the high dielectric constant gate insulating film (102-oxide) located under the insulating sidewall (106) has a smaller thickness than a thickness of part of the high

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dielectric constant gate insulating film (102-oxide) located under the gate electrode (103) (see Figures 9A and 9C).

Response to Arguments

Applicant's arguments filed on November 17, 2011 have been fully considered but they are not persuasive. Applicant argues that Heidi does not disclose or suggest that "an end of the high dielectric constant gate insulating film under the insulating sidewall is located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode". This assertion is respectfully traversed. This element can be seen in Figure 5B of Heidi's reference. The insulating sidewall (106) is over at one end of the gate insulating film.



In view of the foregoing, it is believed that the rejections of claim 21 under 35 USC 102 is proper.

Also, two (2) references are submitted on November 17, 2011 could be applied to reject the independent claim 21 under USC 102. However, it will be overcome by adding claim 22 into claim 21. This request is respectfully recommended.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHUONG LUU whose telephone number is (571)272-1902. The examiner can normally be reached on M-F (6:30-3:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chuong A Luu/
Primary Examiner, Art Unit 2892
November 29, 2011

Search Notes

Application/Control No.

13/037,831

Examiner

CHUONG LUU

Applicant(s)/Patent under
Reexamination

HIRASE ET AL.

Art Unit

2892

SEARCHED

Class	Subclass	Date	Examiner
257	295	8/17/2011	CAL
Update	Searched	11/29/2011	CAL

INTERFERENCE SEARCHED

Class	Subclass	Date	Examiner

**SEARCH NOTES
(INCLUDING SEARCH STRATEGY)**

	DATE	EXMR
Please see the attachment.	8/17/2011	CAL

IN THE SPECIFICATION:

Please amend the following paragraph on page 1 of the specification as follows:

-- RELATED APPLICATIONS

This application is a Divisional of U.S. Patent Application No. 12/505,799, filed on July 20, 2009, which is now U.S. Patent No. 7,923,764, which is a Divisional of U.S. Patent Application No. 11/491,260, filed on July 24, 2006, now U.S. Patent No. 7,579,227, claiming priority of Japanese Patent Application No. 2005-227457, filed on August 5, 2005, the entire contents of each of which are incorporated by reference. --

It's OK to enter.

CAL

11/29/2011

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S117	2	11/491260	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30; 21:31
S118	9	("20030022422" "20040004234" "20040129997" "20050121733" "20050127436" "20060121740" "6642071" "6929992" "6992358").PN. OR ("7579227").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/07/30; 21:36
S119	1	12/505799	US-PGPUB; USPAT; USOCR	OR	ON	2010/07/30; 21:37
S120	2925	(257/295).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/07/30; 21:39
S121	1497	(257/310).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/07/30; 21:39
S122	3	09/916509	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30; 21:39
S123	4702	(257/296,295,310.ccls.) and (gate or electrode) and ((gate or electrode) adj (insulat\$4 or dielectric or oxide))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30; 21:39
S124	587	(257/296,295,310.ccls.) and (gate or electrode) near ((gate or electrode) adj (insulat\$4 or dielectric or oxide))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2010/07/30; 21:39

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			IBM_TDB			
S125	587	(257/296,295,310.ccls.) and ((gate or electrode) near ((gate or electrode) adj (insulat\$4 or dielectric or oxide)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30; 21:40
S126	435	(257/296,295,310.ccls.) and ((gate or electrode) adj ((gate or electrode) adj (insulat\$4 or dielectric or oxide)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30; 21:40
S127	57	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) near (high adj dielectric adj constant))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30; 21:40
S128	33	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) adj (high adj dielectric adj constant))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30; 21:40
S129	13	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) adj (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30; 21:40
S130	19	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) near (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30; 21:41
S131	6	"6992358"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30; 21:41
S132	18	("20030209761" "20040150520" "20040178451" "20050040464" "20050051843" "20050110085" "4979014" "6437404" "6538916" "6580132" "6639246" "6646307" "6687152" "6724046" "6740938" "6744390" "6800513" "6822071").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/07/30; 21:41
S133	55	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) same (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/30; 21:41

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S134	6	((("7018873") or ("6929992") or ("6992358") or ("20060121740") or ("20050121733") or ("7579227"))).PN.	US-PGPUB; USPAT	OR	OFF	2010/07/30; 21:45
S135	9	((("6992358") or ("6929992") or ("6642071") or ("20060121740") or ("20030022422") or ("20040004234") or ("20040129997") or ("20050121733") or ("20050127436"))).PN.	US-PGPUB; USPAT	OR	OFF	2010/07/30; 21:52
S136	3	((("6,992,358") or ("7579227") or ("20050121733"))).PN.	US-PGPUB; USPAT	OR	OFF	2010/08/02; 04:43
S137	56	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) same (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/02; 08:26
S138	1	("5473168").PN.	US-PGPUB; USPAT	OR	OFF	2010/12/02; 09:41
S139	1	12/190015	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/02; 09:42
S140	19	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) near (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/02; 13:11
S141	6	"6992358"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:37
S142	1017	gate and ((gate adj (oxide or insulat\$4 or dielectric)) with (notch\$4 or undercut\$4))	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/04; 20:38
S143	19	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) near (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:38
S144	137	gate and ((gate adj (oxide or insulat\$4 or dielectric)) near (notch\$4 or undercut\$4))	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/04; 20:38
S145	23	gate and ((gate adj (oxide or insulat\$4 or dielectric)) adj (notch\$4 or undercut\$4))	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/04; 20:38
S146	177	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) and (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:39

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S147	12	((("6642071") or ("6929992"))).PN.	USPAT	OR	OFF	2010/12/04 20:39
S148	16	(257/296,295,310.ccls.) and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:39
S149	13	((("20070228442") or ("20040171280") or ("20030207097"))).PN.	US-PGPUB; USPAT	OR	OFF	2010/12/04 20:40
S150	1555	hirase.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:40
S151	179	S150 and junji	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:41
S152	10	S151 and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) adj (high adj dielectric adj constant))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:41
S153	10	S151 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:41
S154	1256	sebe.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:41
S155	18	S154 and akio	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:41
S156	10	S155 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:41

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S157	18752	kotani.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:42
S158	236	S157 and naoki	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:42
S159	0	S158 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:42
S160	0	okazaki and gen and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:42
S161	0	aida and kazuhiko and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:43
S162	0	takeoka and shinji and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:43
S163	35	(((semiconductor) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) adj (high adj dielectric adj constant))))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:43
S164	21	(((semiconductor) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) adj (high adj dielectric adj constant))))).clm.	US-PGPUB	OR	ON	2010/12/04; 20:43
S165	5	((("20050127436") or ("6284630") or ("20020163039") or ("20010028086") or ("5223445"))).PN.	US-PGPUB; USPAT	OR	OFF	2010/12/04; 20:44
S166	3	09/824672	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:44

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S167	2	09/848431	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:44
S168	8	((("20050127436" or ("6284630" or ("20020163039" or ("20010028086" or ("5223445" or ("6509612" or ("6794258" or ("6614081"))).PN.	US-PGPUB; USPAT	OR	OFF	2010/12/04; 20:44
S169	4	10/904875	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:45
S170	1928	(257/324).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/04; 20:46
S171	7	(257/296,295,310,324,410,411.ccls.) and (gate or electrode) and ((gate or electrode) adj (insulat\$4 or dielectric or oxide)) and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:46
S172	1290	(257/410).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/04; 20:46
S173	185	257/e29.132.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:46
S174	1693	257/e29.133.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:46
S175	1606	257/e29.137.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:47
S176	181	257/e29.138.ccls.	US-PGPUB; USPAT;	OR	ON	2010/12/04; 20:47

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			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S177	1676	257/e29.162.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:47
S178	1570	257/e29.165.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:47
S179	12	(257/e29.132,e29.133,e29.134,e29.135,e29.136,e29.137,e29.138,e29.138,e29.162,e29.163,e29.164,e29.164,e29.165.ccls.) and (gate or electrode) and ((gate or electrode) adj (insulat\$4 or dielectric or oxide)) and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:47
S180	1375	(257/411).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/04; 20:48
S181	154	(257/296,295,310,324,410,411.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:48
S182	148	(257/296,295,310,324,410,411.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:48
S183	111	("257/"\$ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04; 20:48
S184	123	(257/e29.132,e29.133,e29.134,e29.135,e29.136,e29.137,e29.138,e29.138,e29.162,e29.163,e29.164,e29.164,e29.165.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2010/12/04; 20:48

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S185	102	(257/e\$.cls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	IBM_TDB US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:49
S186	32	"438"\$\$.cls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:49
S187	5444	(257/296,295,310,324,410,411.cls.) and (gate or electrode) and ((gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:50
S188	48	(257/296,295,310,324,410,411.cls.) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:50
S189	770	(257/296,295,310,324,410,411.cls.) and (((gate or electrode) adj (dielectric or oxide or insulat\$4)) with ((high adj dielectric adj constant) or (ferroelectric))) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:50
S190	184	(257/296,295,310,324,410,411.cls.) and (((gate or electrode) adj (dielectric or oxide or insulat\$4)) near ((high adj dielectric adj constant) or (ferroelectric))) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:50
S191	1011	(257/296,295,310,324,410,411.cls.) and (((gate or electrode) adj (dielectric or oxide or insulat\$4)) same ((high adj dielectric adj constant) or (ferroelectric))) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:51
S193	2	10/519799	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:51
S194	2	"7186604"	US-PGPUB; USPAT; USOCR;	OR	ON	2010/12/04 20:51

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			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S195	2	11/491260	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/04 20:52
S196	1375	(257/411).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/04 21:13
S198	3142	(257/295).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/08/17 17:44
S199	3	11/491260	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/17 17:44
S200	2	12/505799	US-PGPUB; USPAT; USOCR	OR	ON	2011/08/17 17:44
S201	5	((("20030022422") or ("20040004234") or ("20040129997") or ("20050121733") or ("20060121740"))).PN.	US-PGPUB	OR	OFF	2011/08/17 20:09
S202	3	((("7,579,227") or ("20050121733") or ("6,992,358"))).PN.	US-PGPUB; USPAT	OR	OFF	2011/08/17 20:13
S203	8	((("20030022422") or ("20040004234") or ("20040129997") or ("20050121733") or ("20060121740") or ("6,992,358") or ("6,929,992") or ("6,642,071"))).PN.	US-PGPUB; USPAT	OR	OFF	2011/08/17 20:14
S204	3	((("6,992,358") or ("6,929,992") or ("6,642,071"))).PN.	US-PGPUB; USPAT	OR	OFF	2011/08/17 20:14
S205	2	((("7923764") or ("7579227"))).PN.	US-PGPUB; USPAT	OR	OFF	2011/08/18 08:34
S206	1	"13037831"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/27 23:21
S207	2	((("7923764") or ("7579227"))).PN.	US-PGPUB; USPAT	OR	OFF	2011/11/29 20:21
S208	10	((("JP2005-064190") or ("JP2004-172178"))).PN.	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2011/11/29 20:22

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			EPO; JPO; DERWENT; IBM_TDB			
S209	10	JP2005-064190 JP2004-172178	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/11/29; 20:22
S210	12	JP2005064190 JP2004172178	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/11/29; 20:22

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Index of Claims 	Application/Control No.		Applicant(s)/Patent under Reexamination	
	13/037,831		HIRASE ET AL.	
	Examiner		Art Unit	
	CHUONG LUU		2892	

√	Rejected	—	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date											
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SHEET 1 OF 1

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Docket No.: 085393-0499

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Junji HIRASE, et al.	:	Confirmation Number: 7641
	:	
Application No.: 13/037,831	:	Group Art Unit: 2892
	:	
Filed: March 1, 2011	:	Examiner: Chuong A. LUU
	:	
For: SEMICONDUCTOR DEVICE	:	

RESPONSE

Mail Stop – Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated January 12, 2012 having a shortened statutory period of response set to expire on April 12, 2012, Applicants respectfully request reconsideration of the pending rejection for the reasons set forth below.

REMARKS

I. Introduction

In response to the pending Office Action, Applicants respectfully submit that the pending claims are patentable over the cited prior art reference for at least the reasons below.

II. The Rejection Of The Claim Under 35 U.S.C. § 102

Claim 21 was rejected under 35 U.S.C. § 102 as being anticipated by USP No. 6,992,358 to Hieda. For at least the following reasons, it is respectfully submitted that claim 21 is not anticipated by Hieda.

As noted in Applicants' previous response, claim 21 recites that the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall, and that **an end of the high dielectric constant gate insulating film under the insulating sidewall is located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode.** Thus, as recited by claim 21, the high dielectric constant gate insulating film does not extend so as to reach the outer end of the insulating sidewall.

For example, referring to the exemplary embodiments shown in Figs. 6 and 10, the high dielectric constant gate insulating film 4a extends under both the gate electrode 5 and the first insulating sidewalls 7, however, the high dielectric constant gate insulating film 4a is not disposed underneath the outer ends of the insulating sidewalls 7. As noted, for example, in paragraph [0058] of the published application (USP Pub. No. 2011/0147857), a portion of the high dielectric constant gate insulating film 4a is removed beneath the outer ends of the insulating sidewalls 7.

Turning to the pending rejection and the cited prior art reference, it is asserted that the buried oxide film 102 of Hieda corresponds to the recited high dielectric constant gate insulating film, and that the island-form semiconductor structure 103 of Hieda corresponds to the recited gate electrode. However, upon review of Hieda, it is clear that the foregoing elements of Hieda do NOT correspond to the recited high dielectric constant gate insulating film or gate electrode of the present disclosure.

Referring to Figs. 5A-5C and 9A-9C of Hieda, these figures illustrate the steps of the manufacturing process for manufacturing a transistor structure shown in Figs. 14A-14C. Figs. 5A-5C and 9A-9C DO NOT illustrate the final structure of a complete semiconductor device. Referring to 14B of Hieda and the specification, it is clear that element 115 corresponds to the gate insulating film and element 116 corresponds to the gate electrode (*see, also*, col. 9, lines 40-41 and col. 10, lines 38-39 of Hieda). Thus, it is clear that the “buried oxide film 102” and “semiconductor structure 103” of Heidi DO NOT correspond to a gate insulating film or a gate electrode, respectively.

More importantly, the gate insulating film 115 of Hieda DOES NOT extend under both the gate electrode and first insulating sidewalls. As shown in Fig. 14C, the gate insulating film 115 clearly does not extend under the silicon oxide film 106. Thus, at a minimum, Hieda does not disclose this element of claim 21.

It is further noted that the “semiconductor structure 103” that is asserted as corresponding to the “gate electrode” of claim 21 is an active region in which source and drains regions 113a and 113b are formed, and not a gate electrode. The “p-type silicon substrate 101” that is asserted as corresponding to the “active region in a substrate” of claim 21 is a supporting substrate which supports a semiconductor structure 103, and not an active region. The “buried oxide film 102”

that is asserted as corresponding to the “high dielectric constant gate insulating film” of claim 21 is an isolation film to isolate the “semiconductor structure 103” from the “p-type silicon substrate 101,” and not a high dielectric constant gate insulating film.

Thus, for all of the foregoing reasons, it is clear that Hieda does not disclose each of the elements recited by claim 21.

Moreover, even assuming that it was proper to rely on Figs. 5A-5C of Hieda to formulate the pending rejection (which it clearly is not), first, *it is again noted that the pending rejection addresses the thickness of the gate insulating film 102 located under the alleged sidewall 106 relative to thickness of the gate insulating film 102 under gate electrode 103. Importantly, however, claim 21 does not recite any limitations directed to the thickness of the gate insulating film.*

Second, the “1st end” of Heidi identified in page 5 of the Office Action clearly does not correspond to the recited “end of the gate insulating film”. More specifically, **the change in thickness of the gate insulating film cannot be considered “an end” of the gate insulating film. Indeed, even if it were considered an “end”, the change in thickness occurs inside of the insulating sidewall 106. In other words, the portion having a change of thickness in the gate insulating film 102 in Heidi does not occur under the end of the insulating sidewall. Thus, such an interpretation of Heidi still does not result in a device in which the high dielectric constant gate insulating film 102 extends under both the gate electrode 103 and the first insulating sidewalls 106.**

It is well known that the factual determination of lack of novelty under 35 U.S.C. § 102 requires the identical disclosure in a single reference of each element of a claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary

skill in the art. *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F.3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994).

For all of the foregoing reasons, it is clear that Heidi does not disclose or suggest each of the elements recited by claim 21, and therefore does not anticipate claim 21.

III. Dependent Claims

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as the pending independent claim is patentable for at least the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable.

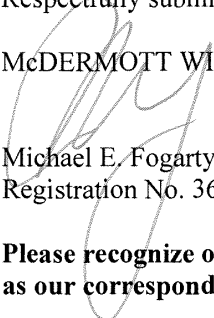
IV. Summary

Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP


Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:
Facsimile: 202.756.8087
Date: March 27, 2012

**Please recognize our Customer No. 53080
as our correspondence address.**

DM_US 32838700-1.085393.0499

Electronic Acknowledgement Receipt	
EFS ID:	12400571
Application Number:	13037831
International Application Number:	
Confirmation Number:	7641
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Junji HIRASE
Customer Number:	53080
Filer:	Michael E. Fogarty/Alexis Boyd
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0499
Receipt Date:	27-MAR-2012
Filing Date:	01-MAR-2011
Time Stamp:	13:07:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		85393-499_Resp.pdf	69567	yes	6
			5b6143e82647660d017ec7ef149375273305cd64		

Multipart Description/PDF files in .zip description			
Document Description		Start	End
Amendment/Req. Reconsideration-After Non-Final Reject		1	1
Applicant Arguments/Remarks Made in an Amendment		2	6
Warnings:			
Information:			
Total Files Size (in bytes):		69567	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

53080 7590 04/13/2012
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

EXAMINER

LUU, CHUONG A

ART UNIT

PAPER NUMBER

2898

DATE MAILED: 04/13/2012

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/037,831	03/01/2011	Junji HIRASE	085393-0499	7641

TITLE OF INVENTION: SEMICONDUCTOR DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1740	\$300	\$0	\$2040	07/13/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Page 1 of 3

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

53080 7590 04/13/2012
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/037,831	03/01/2011	Junji HIRASE	085393-0499	7641

TITLE OF INVENTION: SEMICONDUCTOR DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1740	\$300	\$0	\$2040	07/13/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
LUU, CHUONG A	2898	257-295000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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Address: COMMISSIONER FOR PATENTS
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/037,831	03/01/2011	Junji HIRASE	085393-0499	7641
53080 7590 04/13/2012 MCDERMOTT WILL & EMERY LLP 600 13TH STREET, NW WASHINGTON, DC 20005-3096			EXAMINER LUU, CHUONG A	
			ART UNIT 2898	PAPER NUMBER
DATE MAILED: 04/13/2012				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	13/037,831	HIRASE ET AL.	
	Examiner	Art Unit	
	CHUONG LUU	2898	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 3/27/2012.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 21-42.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☒ Certified copies of the priority documents have been received in Application No. 12/505,799.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.

(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached

1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.

(b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>1/6/2012</u> 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____. 7. ☐ Examiner's Amendment/Comment 8. ☒ Examiner's Statement of Reasons for Allowance 9. ☐ Other _____.
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DETAILED ACTION

Terminal Disclaimer

The terminal disclaimer filed on November 17, 2011 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of the US Patent Number 7,923,764 has been reviewed and is accepted. The terminal disclaimer has been recorded.

The assignment document filed on November 17, 2011 is acceptable as the documentary evidence required by 37 CFR 3.73. If the assignment document is not already recorded with the Patent and Trademark Office, it is suggested that the assignment document be submitted for recording among the Office assignment records. See 37 CFR 3.11 and MPEP § 302.

Allowable Subject Matter

Claims 21-42 are allowed.

The following is an examiner's statement of reasons for allowance: The invention is allowable after it was rejected as Obvious Double Patenting in the first office action. However, the applicant filed terminal disclaimer in a timely manner in compliance with 37 CFR 1.321(c). It may be used to overcome an actual patent is shown to be commonly owned with this application.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHUONG LUU whose telephone number is (571)272-1902. The examiner can normally be reached on M-F (6:30-3:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio Maldonado can be reached on (571)272-1864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chuong A Luu/
Primary Examiner, Art Unit 2898
April 3, 2012

IN THE SPECIFICATION:

1) Please amend the Title of the Invention as follows:

~~SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME~~

***2) Please insert the following new paragraph after the Title and before the “BACKGROUND
OF THE INVENTION”:***

It is OK to enter,

CAL

04/03/2012

-- RELATED APPLICATIONS

This application is a Divisional of U.S. Patent Application No. 12/505,799, filed on July 20, 2009, which is a Divisional of U.S. Patent Application No. 11/491,260, filed on July 24, 2006, now U.S. Patent No. 7,579,227, claiming priority of Japanese Patent Application No. 2005-227457, filed on August 5, 2005, the entire contents of each of which are incorporated by reference. --

Search Notes 	Application/Control No.	Applicant(s)/Patent under Reexamination	
	13/037,831	HIRASE ET AL.	
	Examiner	Art Unit	
	CHUONG LUU	2898	

SEARCHED			
Class	Subclass	Date	Examiner
257	295	8/17/2011	CAL
Update	Searched	11/29/2011	CAL
Update	Searched	4/3/2012	CAL
257	310 296 324	4/3/2012	CAL
257	410 411 368	4/3/2012	CAL
257	392 393 395	4/3/2012	CAL
257	369 389 405	4/3/2012	CAL
257	406	4/3/2012	CAL

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
PG PUB TEXT SEARCH, See interference search printout.		4/3/2012	CAL

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
Please see the attachment.	8/17/2011	CAL
Please see the attachment including East Search (US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB)	4/3/2012	CAL
257/e29.132, e29.133, e29.137, e29.138, e29.162, e29.165).ccls.	4/3/2012	CAL

SHEET 1 OF 1

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Index of Claims 	Application/Control No.		Applicant(s)/Patent under Reexamination	
	13/037,831		HIRASE ET AL.	
	Examiner		Art Unit	
	CHUONG LUU		2898	

✓	Rejected	—	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date											
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3	11/491260	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:08
L2	11	("20030022422" "20040004234" "20040129997" "20050121733" "20050127436" "20060121740" "6642071" "6929992" "6992358").PN. OR ("7579227").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/03 21:08
L3	2	12/505799	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/03 21:08
L4	3238	(257/295).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/04/03 21:08
L5	1585	(257/310).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/04/03 21:08
L6	3	09/916509	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:08
L7	5254	(257/296,295,310.ccls.) and (gate or electrode) and ((gate or electrode) adj (insulat\$4 or dielectric or oxide))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:08
L8	669	(257/296,295,310.ccls.) and (gate or electrode) near ((gate or electrode) adj (insulat\$4 or dielectric or oxide))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2012/04/03 21:08

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			IBM_TDB			
L9	669	(257/296,295,310.ccls.) and ((gate or electrode) near ((gate or electrode) adj (insulat\$4 or dielectric or oxide)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:09
L10	589	(257/296,295,310.ccls.) and ((gate or electrode) adj ((gate or electrode) adj (insulat\$4 or dielectric or oxide)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:09
L11	66	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) near (high adj dielectric adj constant))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:09
L12	41	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) adj (high adj dielectric adj constant))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:09
L13	17	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) adj (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:09
L14	24	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) near (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:09
L16	18	("20030209761" "20040150520" "20040178451" "20050040464" "20050051843" "20050110085" "4979014" "6437404" "6538916" "6580132" "6639246" "6646307" "6687152" "6724046" "6740938" "6744390" "6800513" "6822071").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/03; 21:10
L17	72	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) same (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:10
L18	6	((("7018873" or ("6929992" or ("6992358" or ("20060121740" or ("20050121733" or ("7579227"))).PN.	US-PGPUB; USPAT	OR	OFF	2012/04/03; 21:10
L19	9	((("6992358" or ("6929992" or ("6642071" or ("20060121740" or ("20030022422" or ("20040004234" or ("20040129997" or ("20050121733" or ("20050127436"))).PN.	US-PGPUB; USPAT	OR	OFF	2012/04/03; 21:10
L20	3	((("6,992,358" or ("7579227" or ("20050121733"))).PN.	US-PGPUB; USPAT	OR	OFF	2012/04/03; 21:10

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L21	72	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) same (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:10
L22	1	("5473168").PN.	US-PGPUB; USPAT	OR	OFF	2012/04/03; 21:11
L23	2	12/190015	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:11
L24	24	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) near (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:12
L25	10	"6992358"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:13
L26	1135	gate and ((gate adj (oxide or insulat\$4 or dielectric)) with (notch\$4 or undercut\$4))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/03; 21:13
L27	24	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) near (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:13
L28	155	gate and ((gate adj (oxide or insulat\$4 or dielectric)) near (notch\$4 or undercut\$4))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/03; 21:13
L29	23	gate and ((gate adj (oxide or insulat\$4 or dielectric)) adj (notch\$4 or undercut\$4))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/03; 21:13
L30	202	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) and (high adj dielectric adj constant)) and overlap\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:14
L31	2	("6642071" or ("6929992")).PN.	USPAT	OR	OFF	2012/04/03; 21:14
L32	6	(257/296,295,310.ccls.) and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2012/04/03; 21:14

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			EPO; JPO; DERWENT; IBM_TDB			
L33	3	((("20070228442") or ("20040171280") or ("20030207097"))).PN.	US-PGPUB; USPAT	OR	OFF	2012/04/03; 21:15
L34	1632	hirase.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:15
L35	91	34 and junji	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:15
L36	0	35 and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) adj (high adj dielectric adj constant))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:15
L37	0	35 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:16
L38	308	sebe.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:16
L39	20	38 and akio	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:16
L40	0	39 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:17
L41	19806	kotani.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2012/04/03; 21:17

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L42	258	41 and naoki	IBM_TDB US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:18
L43	0	42 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:18
L44	0	okazaki and gen and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:18
L45	0	aida and kazuhiko and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:18
L46	0	takeoka and shinji and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:19
L47	38	(((semiconductor) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) adj (high adj dielectric adj constant))))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:19
L48	22	(((semiconductor) and (gate or electrode) and (((gate or electrode) adj (insulat\$4 or dielectric or oxide)) adj (high adj dielectric adj constant))))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:19
L49	5	((("20050127436") or ("6284630") or ("20020163039") or ("20010028086") or ("5223445"))).PN.	US-PGPUB; USPAT	OR	OFF	2012/04/03 21:19
L50	3	09/824672	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03 21:19
L51	2	09/848431	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2012/04/03 21:20

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			DERWENT; IBM_TDB			
L52	8	((("20050127436") or ("6284630") or ("20020163039") or ("20010028086") or ("5223445") or ("6509612") or ("6794258") or ("6614081"))).PN.	US-PGPUB; USPAT	OR	OFF	2012/04/03; 21:20
L53	4	10/904875	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:20
L54	2363	(257/324).OCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/04/03; 21:23
L55	7	(257/296,295,310,324,410,411.ccls.) and (gate or electrode) and ((gate or electrode) adj (insulat\$4 or dielectric or oxide)) and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:23
L56	1412	(257/410).OCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/04/03; 21:23
L57	198	257/e29.132.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:24
L58	1713	257/e29.133.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:24
L59	1631	257/e29.137.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:25
L60	181	257/e29.138.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:25

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L61	684	257/e29.162.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:25
L62	602	257/e29.165.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:25
L63	2	(257/e29.132,e29.133,e29.134,e29.135,e29.136,e29.137,e29.138,e29.138,e29.162,e29.163,e29.164,e29.164,e29.165.ccls.) and (gate or electrode) and ((gate or electrode) adj (insulat\$4 or dielectric or oxide)) and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:25
L64	115	(257/296,295,310,324,410,411.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:27
L65	85	(257/296,295,310,324,410,411.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:27
L66	280	("257"/\$.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:27
L67	57	(257/e29.132,e29.133,e29.134,e29.135,e29.136,e29.137,e29.138,e29.138,e29.162,e29.163,e29.164,e29.164,e29.165.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:28
L68	257	(257/e\$.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:28
L69	132	("438"/\$.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2012/04/03; 21:28

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			EPO; JPO; DERWENT; IBM_TDB			
L70	5455	(257/296,295,310,324,410,411.ccls.) and (gate or electrode) and ((gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:29
L71	85	(257/296,295,310,324,410,411.ccls.) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat\$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:29
L72	772	(257/296,295,310,324,410,411.ccls.) and (((gate or electrode) adj (dielectric or oxide or insulat\$4)) with ((high adj dielectric adj constant) or (ferroelectric))) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:30
L73	185	(257/296,295,310,324,410,411.ccls.) and (((gate or electrode) adj (dielectric or oxide or insulat\$4)) near ((high adj dielectric adj constant) or (ferroelectric))) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:30
L74	1015	(257/296,295,310,324,410,411.ccls.) and (((gate or electrode) adj (dielectric or oxide or insulat\$4)) same ((high adj dielectric adj constant) or (ferroelectric))) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:30
L75	2	10/519799	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:30
L76	2	"7186604"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:31
L77	3	11/491260	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 21:31
S198	3142	(257/295) CCLS.	US-PGPUB;	OR	OFF	2011/08/17;

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			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			17:44
S199	3	11/491260	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/17 17:44
S200	2	12/505799	US-PGPUB; USPAT; USOCR	OR	ON	2011/08/17 17:44
S201	5	((("20030022422") or ("20040004234") or ("20040129997") or ("20050121733") or ("20060121740"))).PN.	US-PGPUB	OR	OFF	2011/08/17 20:09
S202	3	((("7,579,227") or ("20050121733") or ("6,992,358"))).PN.	US-PGPUB; USPAT	OR	OFF	2011/08/17 20:13
S203	8	((("20030022422") or ("20040004234") or ("20040129997") or ("20050121733") or ("20060121740") or ("6,992,358") or ("6,929,992") or ("6,642,071"))).PN.	US-PGPUB; USPAT	OR	OFF	2011/08/17 20:14
S204	3	((("6,992,358") or ("6,929,992") or ("6,642,071"))).PN.	US-PGPUB; USPAT	OR	OFF	2011/08/17 20:14
S205	2	((("7923764") or ("7579227"))).PN.	US-PGPUB; USPAT	OR	OFF	2011/08/18 08:34
S206	1	"13037831"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/27 23:21
S207	2	((("7923764") or ("7579227"))).PN.	US-PGPUB; USPAT	OR	OFF	2011/11/29 20:21
S208	0	((("JP2005-064190") or ("JP2004-172178"))).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/11/29 20:22
S209	0	JP2005-064190 JP2004-172178	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/11/29 20:22
S210	2	JP2005064190 JP2004172178	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/11/29 20:22
S211	2	("6,992,358").PN.	US-PGPUB; USPAT;	OR	OFF	2012/01/05 21:24

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			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S212	3	((("7923764") or ("7579227") or ("20040227185"))).PN.	US-PGPUB; USPAT	OR	OFF	2012/04/03; 13:27
S213	2	10/754539	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/03; 13:34
S214	18	("20020053711" "5889331" "6314021" "6512258" "6518155" "6765273" "6777283" "6777759").PN. OR ("2004/0227185" "7067881").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/03; 13:34
S215	1508	(257/411).COLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/04/03; 13:45
S216	1412	(257/410).COLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/04/03; 13:46
S217	5368	(257/296).COLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/04/03; 13:48
S218	2452	(257/368).COLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/04/03; 13:51
S219	3839	(257/369).COLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/04/03; 13:51
S220	251	(257/389).COLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/04/03; 13:52

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S221	860	(257/392) CCL.S.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/04/03; 13:52
S222	549	(257/393) CCL.S.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/04/03; 13:53
S223	199	(257/395) CCL.S.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/04/03; 13:53
S224	198	(257/405) CCL.S.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/04/03; 13:53
S225	246	(257/406) CCL.S.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/04/03; 13:53
S226	1412	(257/410) CCL.S.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/04/03; 13:54

4/ 3/ 2012 9:36:21 PM

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Issue Classification 	Application/Control No.	Applicant(s)/Patent under Reexamination	
	13/037,831	HIRASE ET AL.	
	Examiner	Art Unit	
	CHUONG LUU	2898	

ISSUE CLASSIFICATION									
ORIGINAL				CROSS REFERENCE(S)					
CLASS		SUBCLASS		CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
257		295		257	310	395	411		
INTERNATIONAL CLASSIFICATION									
H	0	1	L	29/76					
H	0	1	L	29/94					
H	0	1	L	31/062					
H	0	1	L	31/113					
H	0	1	L	31/119					
----- (Assistant Examiner) (Date)				/Chuong A. Luu/ 04/03/2012				Total Claims Allowed: 22	
(Legal Instruments Examiner) (Date)								O.G. Print Claim(s) 1	
				(Primary Examiner) (Date)					

☒ Claims renumbered in the same order as presented by applicant				☐ CPA				☒ T.D.				☐ R.1.47			
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original		
	1	11	31		61		91		121		151		181		
	2	12	32		62		92		122		152		182		
	3	13	33		63		93		123		153		183		
	4	14	34		64		94		124		154		184		
	5	15	35		65		95		125		155		185		
	6	16	36		66		96		126		156		186		
	7	17	37		67		97		127		157		187		
	8	18	38		68		98		128		158		188		
	9	19	39		69		99		129		159		189		
	10	20	40		70		100		130		160		190		
	11	21	41		71		101		131		161		191		
	12	22	42		72		102		132		162		192		
	13		43		73		103		133		163		193		
	14		44		74		104		134		164		194		
	15		45		75		105		135		165		195		
	16		46		76		106		136		166		196		
	17		47		77		107		137		167		197		
	18		48		78		108		138		168		198		
	19		49		79		109		139		169		199		
	20		50		80		110		140		170		200		
1	21		51		81		111		141		171		201		
2	22		52		82		112		142		172		202		
3	23		53		83		113		143		173		203		
4	24		54		84		114		144		174		204		
5	25		55		85		115		145		175		205		
6	26		56		86		116		146		176		206		
7	27		57		87		117		147		177		207		
8	28		58		88		118		148		178		208		
9	29		59		89		119		149		179		209		
10	30		60		90		120		150		180		210		

U.S. Patent and Trademark Office

Part of Paper No. 20120403

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

53080 7590 04/13/2012
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600 13TH STREET, NW
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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Stephanie Sherrell (Depositor's name)
Stephanie Sherrell (Signature)
July 13, 2012 (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/037,831	03/01/2011	Jung HIRASE	085393-0499	7641

TITLE OF INVENTION: SEMICONDUCTOR DEVICE

07/16/2012 MBELETE2 00000021 13037831

01 FC:1501 1740.00 DA
 02 FC:1504 300.00 DA
 03 FC:0001 12.00 DA

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	51740	5300	50	\$2040	07/13/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
LUU, CHUONG A	2898	257-295000

07/16/2012 MBELETE2 00000021 500417 13037831

01 FC:1501 1740.00 DA
 02 FC:1504 300.00 DA

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list:
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.111. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

PANASONIC CORPORATION

Osaka, Japan

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☒ Advance Order - # of Copies **4**

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- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number **500417** (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

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Authorized Signature

Date **July 13, 2012**

Typed or printed name

Michael E. Fogarty

Registration No. **36,139**

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/037,831	08/28/2012	8253180	085393-0499	7641

53080 7590 08/08/2012
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(S) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

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