

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

Petitioner,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,

Patent Owner.

IPR2025-00831

U.S. Patent 8,587,076

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT 8,587,076**

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EXHIBIT LIST

Exhibit	Description
1001	U.S. Patent 8,587,076 to Hirase et al. (“the ’076 patent”)
1002	File History of U.S. Patent 8,587,076 (“’076 File History”)
1003	Declaration of Dr. Jack Lee in Support of IPR Petition
1004	CV of Dr. Jack Lee
1005	Translated Excerpts from JP File History
1006	U.S. Patent 7,579,227 to Hirase, et al. (“the ’227 patent”)
1007	U.S. Patent 7,923,764 to Hirase et al. (“the ’764 patent”)
1008	File History of U.S. Patent 8,253,180 (“’180 File History”)
1009	U.S. Publication 2003/0025135 to Matsumoto, et al. (“Matsumoto”)
1010	JP2003-258241 to Kajiyama (“JP-Kajiyama”)
1011	Certified Translation of JP2003-258241 to Kajiyama (“Kajiyama”)
1012	Reserved
1013	U.S. Publication 2005/0051856 to Ono, et al. (“Ono”)
1014	Reserved
1015	Reserved
1016	Reserved
1017	Reserved
1018	Wilk, G. D., et al., “High-k gate dielectrics: Current status and materials properties considerations,” Journal of Applied Physics, Vol. 89, No. 10, pp. 5243-5275, May 15, 2001 (“Wilk”)

Exhibit	Description
1019	Reserved
1020	Reserved
1021	Reserved
1022	Reserved
1023	U.S. Patent 6,306,712 to Rodder, et al. (“Rodder”)
1024	Sim, J. H., et al., “Effects of ALD HfO ₂ thickness on charge trapping and mobility,” Microelectronic Engineering, Vol. 80, pp. 218-221, June 17, 2005 (“Sim”)
1025	Reserved
1026	Declaration of June Ann Munford
1027	U.S. Publication 2002/0063299 to Kamata, et al. (“Kamata”)
1028	U.S. Publication 2006/0091432 to Guha, et al. (“Guha”)
1029	Koyama, M., et al., “Effects of Nitrogen in HfSiON Gate Dielectric on the Electrical and Thermal Characteristics,” Digest of International Electron Devices Meeting, pp. 849-852, Dec. 8-11, 2002 (“Koyama”)
1030	Reserved
1031	U.S. Patent 6,911,695 to Ahmed, et al. (“Ahmed”)
1032	Houssa, M., “High-k Dielectrics to Houssa” (IOP Publishing Ltd. 2004) (“Houssa”)
1033	Plummer, J., et al., “Silicon VLSI Technology: Fundamentals, Practice and Modeling” (Prentice Hall 2000) (“Plummer”)
1034	Wolf, S., “Silicon Processing for the VLSI Era, Volume 4 – Deep-Submicron Process Technology” (Lattice 2002) (“Wolf”)

Exhibit	Description
1035	Reserved
1036	Reserved
1037	Lee, S. J., et al. “High quality ultra thin CVD HfO ₂ /sub 2/ gate stack with poly-Si gate electrode,” Digest of International Electron Devices Meeting, pp. 31-34, Dec. 10-13, 2000 (“Lee”)
1038	Campbell, “The Science and Engineering of Microelectronic Fabrication”, Second Edition (2001) (“Campbell”)
1039	Reserved
1040	JP2005-064190 to Ono with certified translation (“JP-Ono”)
1041	N. Weste and D. Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, Third Edition (Pearson/Addison Wesley, 2005) (“Weste”)
1042	Reserved
1043	Reserved
1044	Reserved
1045	Reserved
1046	Reserved
1047	Reserved
1048	U.S. Patent 6,504,214 to Yu, et al. (“Yu”)
1049	Lee, B.H., et al., “Ultrathin Hafnium Oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application,” Digest of International Electron Devices Meeting, pp. 133-36, Dec. 5-8, 1999 (“Lee-1999”)
1050	U.S. Publication 2005/0040479 to Koldiaev, et al. (“Koldiaev”)

Exhibit	Description
1051	U.S. Publication 2005/0139932 to Cho, et al. (“Cho”)

I. Introduction

Taiwan Semiconductor Manufacturing Company Ltd. (“Petitioner” or “TSMC”) petitions for *inter partes* review of claims 1-13 of U.S. Patent 8,587,076 (“the ’076 patent”; TSMC-1001).

The ’076 patent purports to improve the driving power and reliability of a metal insulator semiconductor field-effect transistor by extending a high-k gate insulating film beyond the gate electrode. (TSMC-1001, 1:18-24, 2:9-19, 2:39-46.) This concept was well known before the ’076 patent, a fact Applicant acquiesced to during Japanese prosecution.

Petitioner demonstrates the challenged claims are unpatentable.

II. Grounds for Standing

Petitioner certifies the ’076 patent is available for IPR and that it is not barred or estopped from requesting IPR of the challenged claims on the grounds in this Petition.

III. Identification of Challenge

A. Prior Art

The ’076 patent, filed July 12, 2012, claims priority through divisional applications to U.S. Patent 7,579,227 (“the ’227 patent”) which claims priority to JP2005-227457 (“JP Application”), filed August 5, 2005. Petitioner does not acquiesce the ’076 patent is entitled to benefit of any prior U.S. patents or the JP

application. Regardless, each applied reference was filed or published before August 5, 2005.

1. **U.S. Publication 2002/0063299 to Kamata, et al.** (“Kamata”; TSMC-1027), published May 20, 2002, is prior art under 35 U.S.C. §102(b).¹
2. **U.S. Publication 2006/0091432 to Guha, et al.** (“Guha”; TSMC-1028), filed November 2, 2004, is prior art under §102(e).
3. **U.S. Publication 2003/0025135 to Matsumoto, et al.** (“Matsumoto”; TSMC-1009), published February 6, 2003, is prior art under §102(b).
4. **U.S. Publication 2005/0051856 to Ono, et al.** (“Ono”; TSMC-1013), published March 10, 2005, is prior art under §102(b).
5. **“Effects of Nitrogen in HfSiON Gate Dielectric on the Electrical and Thermal Characteristics” to Koyama, et al.** (“Koyama”; TSMC-1029), published in 2002, is prior art under §102(b). (TSMC-1026, ¶¶18-21.)
6. **“Effects of ALD HfO₂ thickness on charge trapping and mobility” to Sim, et al.** (“Sim”; TSMC-1024), published June 17, 2005, is prior art under §102(b). (TSMC-1026, ¶¶14-17.)

¹ Pre-AIA 35 U.S.C. §102 applies.

7. **U.S. Patent 6,911,695 to Ahmed, et al.** (“Ahmed”; TSMC-1031), issued June 28, 2005, is prior art under §102(b).

8. **U.S. Patent 6,504,214 to Yu, et al.** (“Yu”; TSMC-1048), issued January 7, 2003, is prior art under §102(b).

B. Grounds for Challenge

Ground		Claims	Prior Art
1	103	1-3, 7-13	Kamata
2	103	4	Kamata-Koyama
3	103	6	Kamata-Sim
4	103	1-3, 7-8, 10-13	Guha
5	103	4	Guha-Koyama
6	103	6	Guha-Sim
7	103	9	Guha-Ahmed
8	103	1-3, 7-10, 13	Matsumoto-Yu
9	103	6	Matsumoto-Yu-Sim
10	103	1, 4	Matsumoto-Koyama
11	103	1, 5, 11-12	Matsumoto-Ono

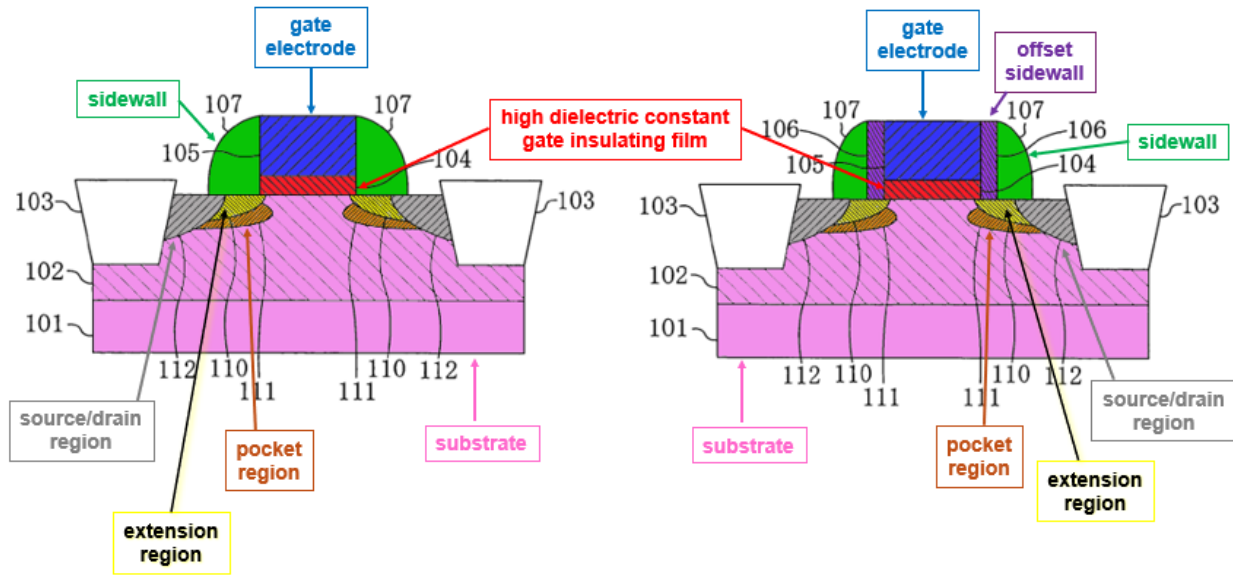
IV. '076 Patent

A. Applicant Admitted Prior Art (AAPA)

The '076 patent recognized that, prior to August 2005, semiconductor devices had used “a high dielectric constant film formed of a Hf based oxide, Al

based oxide or the like” as a gate insulating film. (TSMC-1001, 1:26-34.) It describes two prior art metal insulator semiconductor field-effect transistors (MISFETs), depicted in Figures 16A-16B, each including a high dielectric constant gate insulating film² 104 (shaded red) interposed between gate electrode 105 (shaded blue) and the substrate. In the Figure 16A device, sidewall 107 (shaded green) is formed on each side of gate electrode 105. (TSMC-1001, 1:46-47.) In the Figure 16B device, an additional offset sidewall 106 (shaded purple) is interposed between sidewall 107 and gate electrode 105. (TSMC-1001, 1:55-58.)

² The terms “gate dielectric” and “gate insulating film” are used interchangeably. The term “high dielectric constant” is also referred to as “high-k” in this Petition and the prior art documents.



'076 Patent, Figure³ 16A

'076 Patent, Figure 16B

In these prior art devices, the “side end portions” of the high-k gate insulating film “are in direct contact with sidewalls.” (TSMC-1001, 1:66-69.) The '076 patent purports to address issues with this arrangement by extending the high-k film under the “sidewalls to prevent end portions of the [high-k] film from being in contact with the sidewalls.” (TSMC-1001, 2:13-22.)

The basic concept of extending a high-k gate insulating film from under the gate electrode to beneath sidewalls was well-known. (*E.g.*, §§IV.B.2.b, IV.D.2, V, VIII, XII.)

³ All shading and annotations in figures added, unless otherwise noted.

B. Technical Background

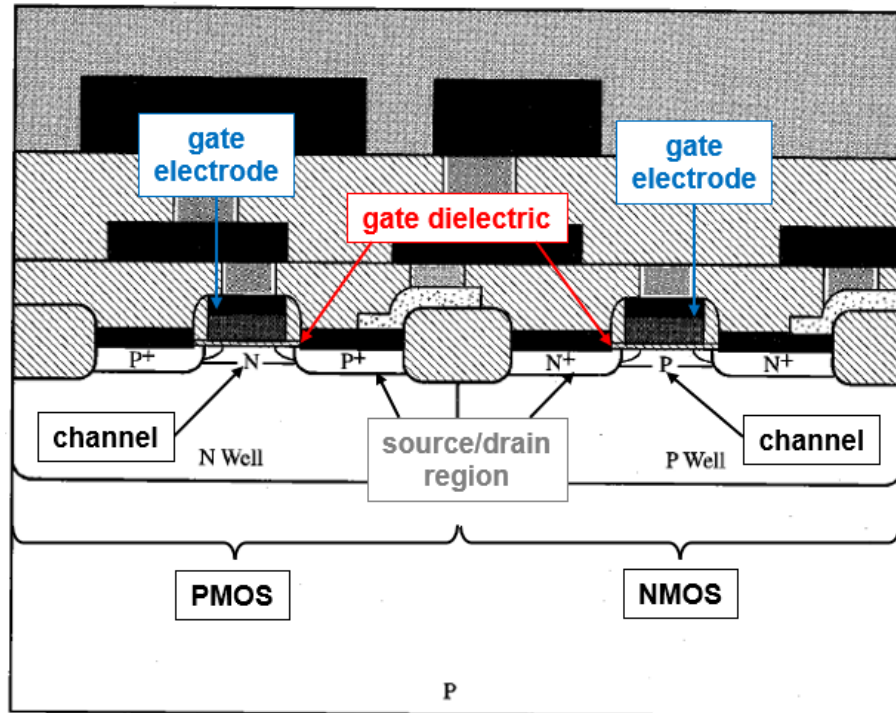
A semiconductor device, at its most basic, exploits the properties of semiconductor materials such as silicon. Many types of semiconductor devices exist including, e.g., diodes, MOS transistors (e.g., field effect transistors (FETs)), and memory devices. (*E.g.*, TSMC-1033, 33-41.) For ease of discussion, Petitioner describes FET devices in further detail. A POSITA would understand that the basic concepts discussed in §IV.B apply to other types of semiconductor devices.

1. MISFET/MOSFET

MISFETs⁴ have a **source/drain** for current input/output. (TSMC-1003, ¶36; TSMC-1033, 76-82.) MISFETs like the ones at issue here also have a **gate** above a **channel** region between the source and drain. (TSMC-1003, ¶36; TSMC-1033, 71-76.) The **gate** includes a **gate electrode** and **gate dielectric** (also referred to as a gate insulating film) separating the gate electrode from the channel region. (TSMC-1003, ¶36; TSMC-1033, 71-76.) Applying voltage to the gate electrode controls the channel region to connect (ON state) or disconnect (OFF state) the source and drain. (TSMC-1003, ¶37; TSMC-1041, 8-9.) Generally, source/drain

⁴ The terms “MISFET” and “MOSFET” (“Metal-*Oxide*-Semiconductor Field-Effect Transistor”) are interchangeable. (TSMC-1003, ¶36.)

regions are **doped** with either a **p-type** or **n-type** impurity. (TSMC-1003, ¶¶38-39; TSMC-1033, 76-82.) MISFETs with n-type source/drain regions are called **NMOS**, and MISFETs with p-type source/drain regions are called **PMOS**. (TSMC-1003, ¶44; TSMC-1033, 13, Figure 1-11.)



Plummer, Figure 1-11

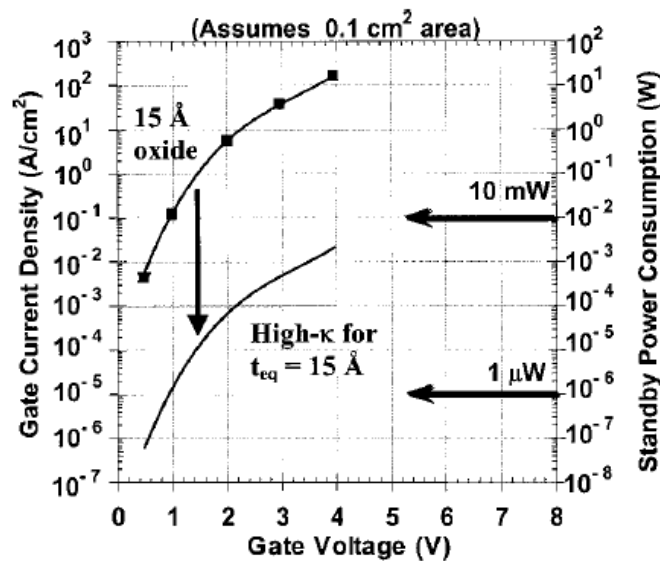
2. Gate Insulating Film

a. Materials

For decades prior to the '076 patent, silicon dioxide (SiO_2) was the primary material used for gate dielectrics in MOSFETs. (TSMC-1003, ¶46; TSMC-1033, 53 (“ SiO_2 is essentially a perfect insulator and provides the needed [electrical] isolation.”); TSMC-1032, 3-4.) As gate dielectric layers continued to shrink in

thickness (e.g., below 1.5 nm), use of SiO₂ became untenable, because the amount of gate-to-channel tunneling leakage-current passing through the gate dielectric prevents the gate electrode from effectively controlling the ON/OFF states of the FET. (TSMC-1003, ¶46; TSMC-1034, 4-5.)

High-k dielectrics, like Hf-based oxides, Ta₂O₅, or ZrO₂, replaced SiO₂ to address these challenges. (TSMC-1003, ¶¶47-48; TSMC-1034, 146.) For example, it was known by 2005 that, as compared to SiO₂, high-k materials significantly reduce the amount of leakage current and, thus, improve energy efficiency. (TSMC-1003, ¶49; TSMC-1018, 5250, Figure 5 (below); TSMC-1034, 146-47.)

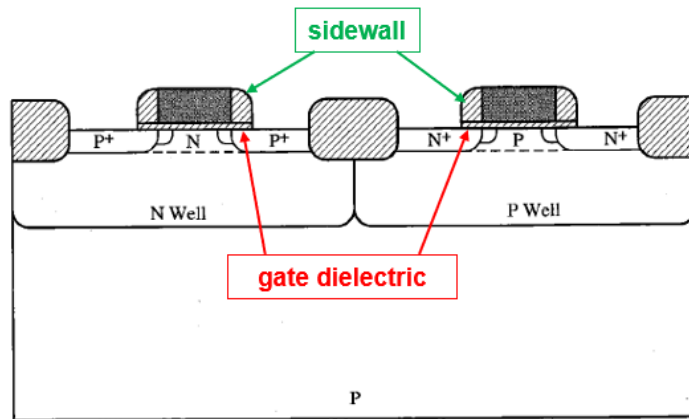


Wilk, Figure 5

b. Extended Gate Insulating Films

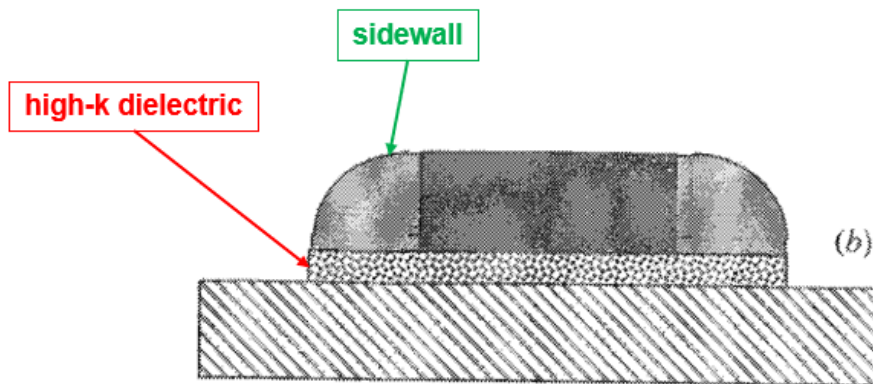
Prior to 2005, it was common practice to extend the gate dielectric from under the gate electrode to under a device's sidewalls. For example, Plummer

depicts a CMOS device having an extended gate dielectric in the NMOS and PMOS transistors. (TSMC-1003, ¶50; TSMC-1033, 82-83.)



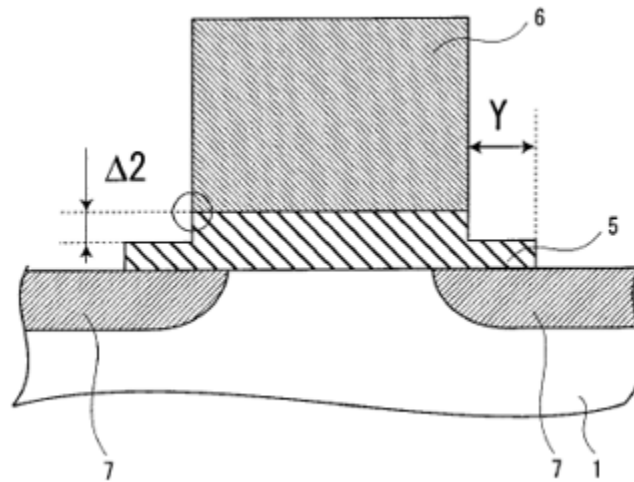
Plummer, Figure 2-34

Houssa discloses another example using a high-k material as the gate insulating film that extends from under the gate electrode to under the sidewalls. (TSMC-1032, 510, Figure 5.1.9(b) (below).)



Houssa, Figure 5.1.9(b)

JP Publication 2005-064190 (“JP-Ono”⁵; TSMC-1040), filed two years before the ’076 patent, examines how adjusting the length of the gate dielectric from the outer edge of the gate electrode (Y) (i.e., how far the gate dielectric protrudes from under the gate electrode) affects electric field distribution, noting that “increasing Y effectively suppresses the electric field intensity on the source-drain region by thinning the gate insulating film.” (TSMC-1040, ¶87.)



JP-Ono, Figure 3

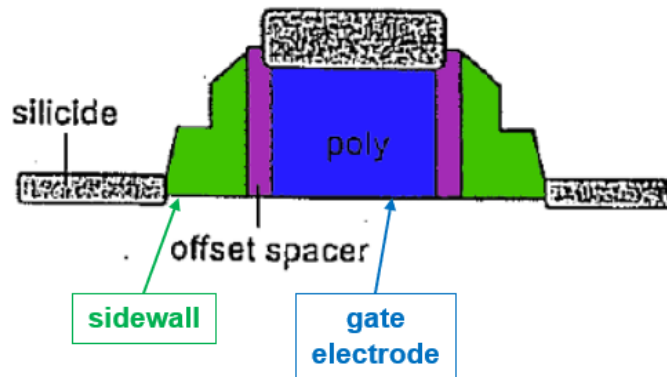
3. Sidewalls

Another common device feature is sidewalls, vertical insulating structures formed on or proximate to a gate electrode’s side surfaces. Sometimes, the terms “sidewall,” “spacer,” and “sidewall spacer” are used interchangeably. (TSMC-

⁵ A certified translation of JP-Ono is included with TSMC-1040.

1003, ¶158.) Sidewalls serve a variety of purposes and functions such as defining the source/drain region, providing isolation, protecting the gate during subsequent fabrication, and controlling the width of the gate in the gate length direction. (*Id.*)

As a non-limiting example, spacers may be used for “[c]ontrolling the position of the edge of the SDE [source/drain extension] region with respect to the gate edge” to achieve optimal amount of overlap between the SDE and gate edge. (TSMC-1034, 217.) As shown below, “an offset-spacer is fabricated on the side of the gate after the gate-poly is etched (but before the SDE implant step is carried out ...),” with offset-spacer width “varied from zero (no-spacer) to some upper-bound (e.g., 50-nm)” to achieve optimum device characteristics. (*Id.*)

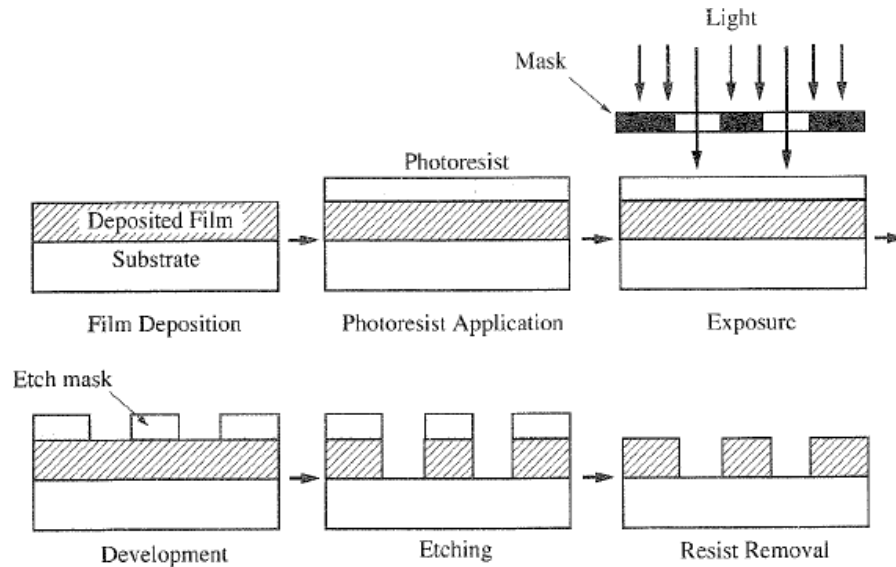


Wolf, Figure 5-25

4. Etching Properties

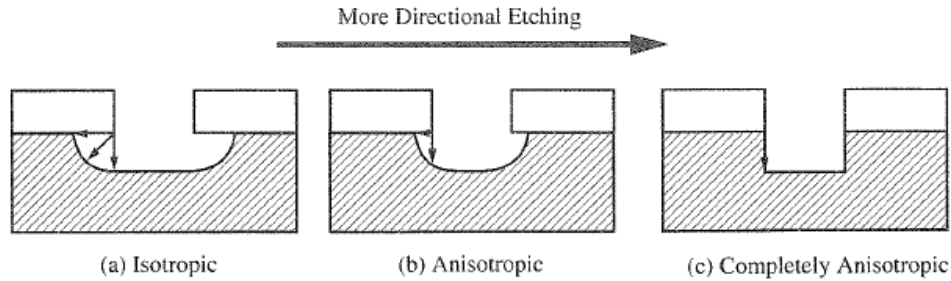
In semiconductor devices, thin films are often first deposited on the wafer surface and then selectively removed by etching to leave the desired pattern of the film. (TSMC-1003, ¶60; TSMC-1033, 609-11.) The desired pattern is often

defined by placing a mask on the surface before etching; the mask is removed after etching. (TSMC-1003, ¶60; TSMC-1033, 609-10, Figure 10-1 (below).)



Plummer, Figure 10-1

Etching is performed in a “wet” or “dry” environment. (TSMC-1003, ¶61; TSMC-1033, 609, 612-37.) Wet etching involves use of liquid etchants (e.g., hydrofluoric acid) whereas dry etching involves use of gas-phase etchants in a plasma. (TSMC-1003, ¶61; TSMC-1033, 609.) Etching processes are also described based on the relative etch rates in different directions. (TSMC-1003, ¶60; Plummer 610-11.) Isotropic etching occurs when the etch rate is the same in all directions, resulting in a semicircular etch profile as shown in Figure 10-3(a) below. Most wet chemical etchants etch isotropically. (TSMC-1033, 610-13.) Anisotropic etching occurs where there is little or no etching in the lateral direction. (TSMC-1033, 611, Figure 10-3(b), (c) (below).)



Plummer, Figure 10-3

C. '076 Patent Overview

The '076 patent presents four semiconductor device embodiments (first-fourth embodiments) and their associated fabrication methods (fifth-eighth embodiments). In each embodiment, the high-k gate insulating film (shaded red) extends beyond the gate electrode to under the sidewall(s). (TSMC-1001, Figures 1-2, 5, 9 (below).) The embodiments differ in the number of sidewalls (one/two) and the presence of a buffer layer under the gate insulating film (fourth embodiment). The embodiments also vary in the relative thickness of the gate insulating film under the gate electrode and sidewalls, though this difference is not relevant to most of '076 patent claims.

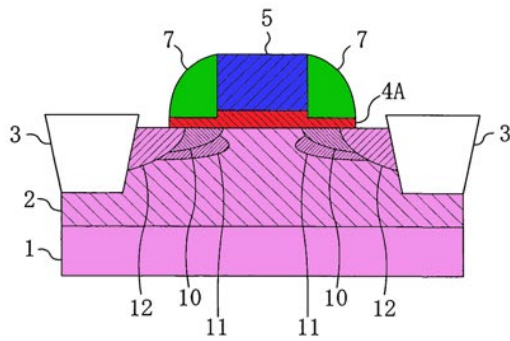


Figure 1—First Embodiment

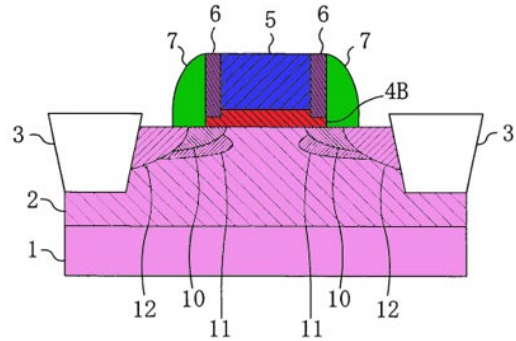


Figure 2—Second Embodiment

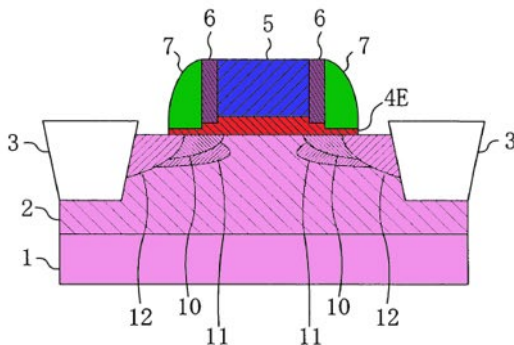


Figure 5—Third Embodiment

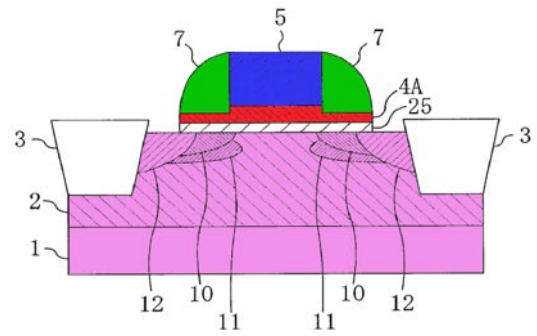
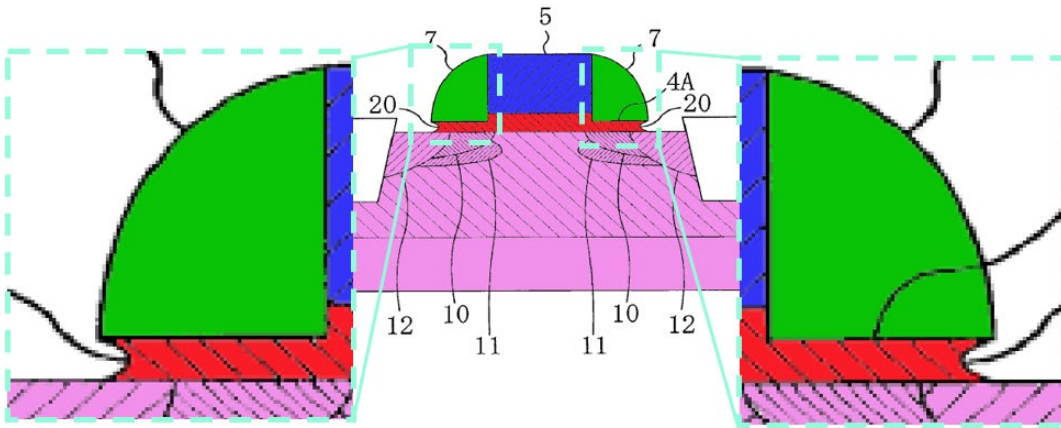


Figure 9—Fourth Embodiment

Each embodiment includes a modification in which “a side portion of the high dielectric constant gate insulating film ... is removed in a notch shape, so that a notch 20 is provided”, illustrated in Figure 6 below for the first embodiment modification. (TSMC-1001, 7:10-15, 14:49-56, Figure 6, 8:41-46, 16:14-21, Figure 7, 11:53-58, 18:22-28, Figure 8, 13:8-21, Figure 10.)



Annotated Figure 6 with enlargements

The concept of changing the shape and/or location of the end of a dielectric was known, long before the '076 patent. (*E.g.*, §§IV.D.2, V, VIII, XII, XV.)

D. Prosecution History

1. U.S. Family Prosecution

a. '076 Patent

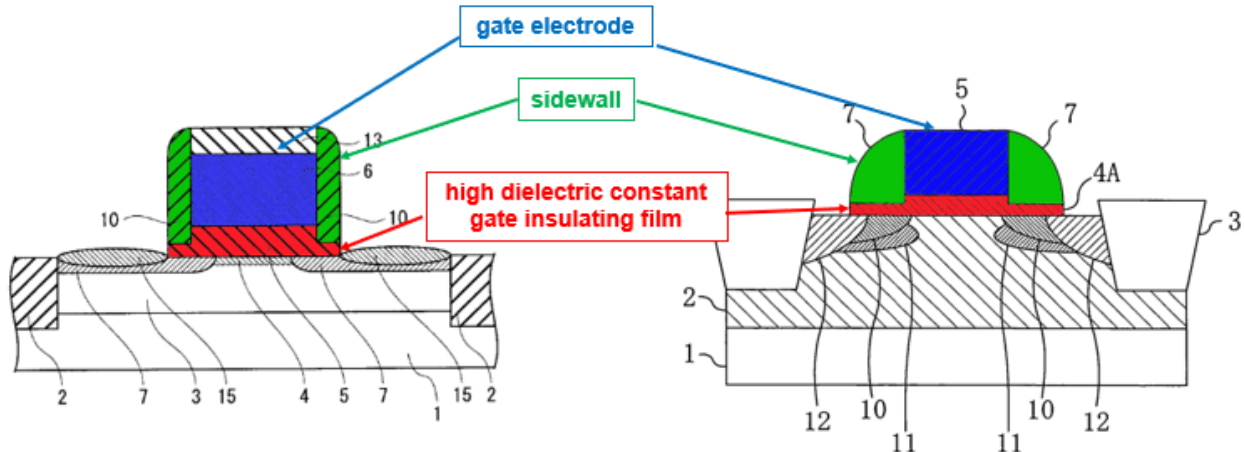
The '076 patent application was filed with 13 claims including a single independent claim corresponding to issued claim 1. The Examiner rejected the claims based on nonstatutory obviousness-type double patenting over claims 1-22 of the '180 patent (TSMC-1002, 133-34.) The Examiner also rejected the claims as unpatentable over U.S. Patent 6,992,358 to Hieda ("Hieda"). (TSMC-1002, 129-33.) Applicant submitted a terminal disclaimer and traversed the Hieda rejection. (TSMC-1002, 157-159.) The Examiner allowed the claims. (TSMC-1002, 173-74.)

b. '180 Patent

Like in the '076 prosecution, the filed '180 patent application claims were rejected as unpatentable over Hieda. (TSMC-1008, 123-27.) Applicant traversed, arguing Hieda did not disclose the “predetermined distance” limitation. (TSMC-1008, 151-52.) According to Applicant, this limitation was not met because “the high dielectric constant insulating [film] recited by claim 21 [issued claim 1] does not extend so far such that it is disposed beneath the outer end of the insulating sidewall It is disposed inwardly of the outer end of the insulating sidewall.” (TSMC-1008, 151-52.) The claims were allowed.

2. JP Application

The JP Application was filed with the same device claim originally filed with the U.S. application for the '227 patent. (TSMC-1005, 1.) On September 16, 2011 (before filing of the '076 patent), the JP-Examiner found this claim scope unpatentable, citing the JP-Ono publication discussed in §IV.B.2 (Figure 23-left) and WO2004/017418 to Sakai, et al. (“Sakai”) which both teach a high-k gate insulating film extending from under the gate electrode to under the sidewalls. (TSMC-1005, 4-6.)



JP-Ono, Figure 23

'076 Patent, Figure 1

For the claim reciting a “notch” at the end of the high-k gate insulating film, the JP-Examiner determined JP-Ono taught this limitation at ¶84 which states:

In this embodiment, the side surface of the gate insulating film 5 is aligned with the outer surface of the gate sidewall 10, but this is not essential, and the side surface of the gate insulating film 5 is inside the outer surface of the gate side wall 10. Or even if it exists outside, the effect similar to this Embodiment is acquired.

(TSMC-1040, ¶84; TSMC-1005, 5.) This disclosure from JP-Ono is also relevant to the '076 patent because it discloses the end of the extended gate dielectric is retracted from the outer end of the sidewall.

In response, Applicant narrowed the independent claim. (TSMC-1005, 8.) The JP-Examiner rejected the amended claim based on both JP2003-258241 to Kajiyama (“Kajiyama”) and JP2004-241755 to Matsumoto (“JP-Matsumoto”) which both have extended gate insulating films. (TSMC-1005, 14-16.) The JP-

Examiner maintained the rejection of the notch claim over JP-Ono combined with either Kajiyama or JP-Matsumoto. (TSMC-1005, 15.) Applicant further narrowed the claim to obtain allowance. (TSMC-1005, 18.)

Despite the materiality of the JP notices of refusal, Applicant did not inform the U.S. Examiner of the rejections by the JP-Examiner during pendency of the '076 patent.

E. Claim Construction

Petitioner does not believe any claims require construction to resolve the patentability disputes in this proceeding. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

F. Level of Ordinary Skill in the Art

A POSITA would have had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. (TSMC-1003, ¶31.)

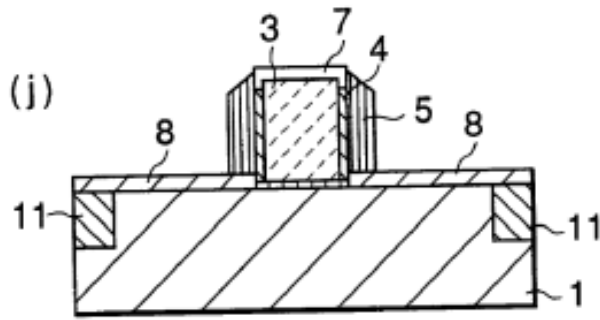
Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education. (*Id.*)

V. GROUND 1: Kamata Renders Claims 1-3, 7-13⁶ Obvious.

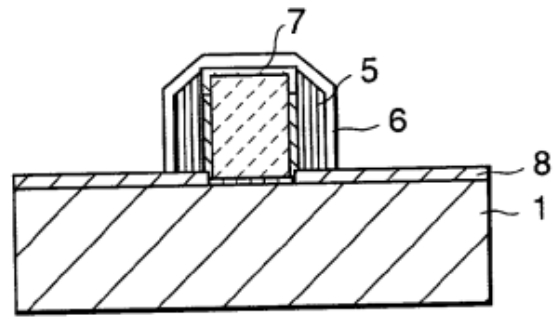
A. Overview

While numerous embodiments are relevant and invalidating, this Petition focuses on Kamata's first (Figure 1B(j)), fourth (Figure 5(c)), and ninth (Figure 10(b)) embodiments. Each embodiment's device includes a gate electrode, a gate insulating film, and a sidewall structure having first sidewall film 4 and second sidewall film 5. (TSMC-1027, ¶¶50-61 (first embodiment), 68 (fourth embodiment), 93-94 (ninth embodiment).) In each embodiment, the gate insulating film extends from under the gate electrode to under only a portion of the sidewall structure.

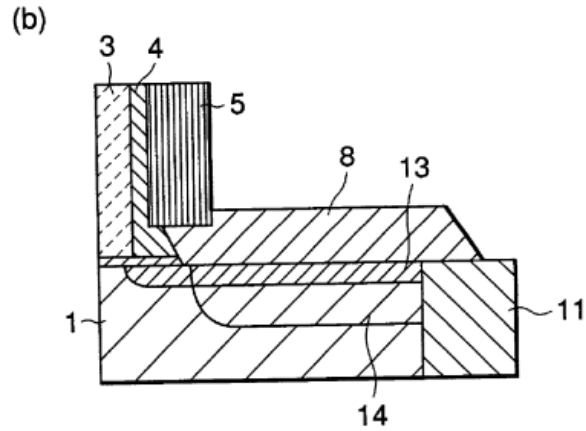
⁶ Challenged claims listing is provided in the Appendix.



Kamata, Figure 1B(j)
(First Embodiment)



Kamata, Figure 5(c)
(Fourth Embodiment)



Kamata, Figure 10(b)
(Ninth Embodiment)

B. Independent Claim 1

1. Preamble [1P]

Kamata’s first, fourth, and ninth embodiments each discloses a “*semiconductor device*”⁷: “invention relates to a **semiconductor device**.”⁸ (TSMC-1027, ¶¶3, 8; *see also* TSMC-1027, ¶¶32, 50 (first embodiment), 36, 68 (fourth embodiment), 93-94 (ninth embodiment).)

2. Limitation [1A]

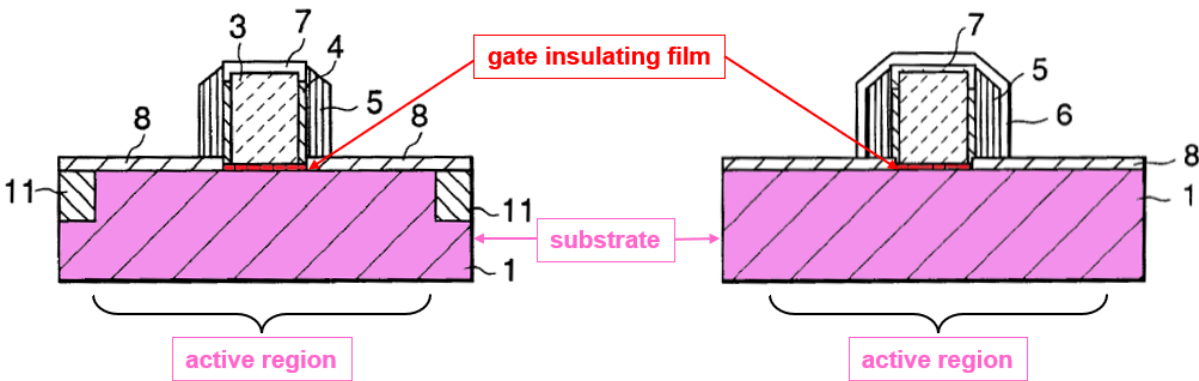
Kamata’s first, fourth, and ninth embodiment each discloses “*a gate insulating film formed on an active region in a substrate and including Hf*” [1A]. (TSMC-1003, ¶¶88-92.)

The device of each embodiment has “a semiconductor **substrate** 1 made of silicon” (shaded pink). (TSMC-1027, ¶¶50, 68 (“parts [of fourth embodiment] that are same as or similar to those of the first embodiment are denoted respectively by the same reference symbols”), 94 (“portions [of ninth embodiment] that are same as or similar to those FIGS. 1A through 2C are denoted respectively by the same reference symbols”).) Kamata explains “shallow trench isolation zones (STI) 11” are formed on the substrate “to define an element region 1a” and refers to element

⁷ Claim language is indicated by italics throughout.

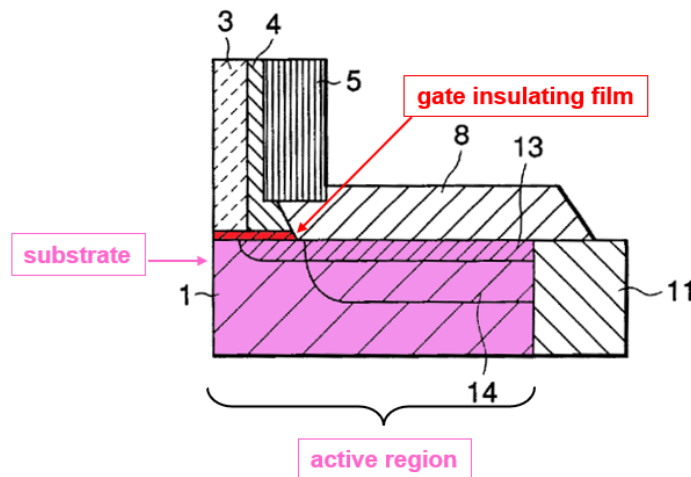
⁸ Unless otherwise noted, all emphasis added.

1a as an “active region.” (TSMC-1027, ¶¶50, 68, 94, 99-100 (referring to element 1a of Figure 1A(a) as “active region” and indicating same parts are “denoted ... by the same reference symbols”); *Google LLC v. Jenam Tech, LLC*, IPR2021-00630, 2022 WL 4287797, *9 n.9 (P.T.A.B. Sept. 16, 2022) (applying same disclosures where “figures refer to corresponding features using the same reference numbers”); TSMC-1001, 1:42-43 (“region of the well 102 surrounded by the STI serves as an active region of a substrate 101”); TSMC-1003, ¶89). A POSITA would have therefore understood element region 1a, identified by STI, is an “*active region in a substrate.*” (TSMC-1003, ¶89.)



**Kamata, Figures 1B(j)
(First Embodiment)**

**Kamata, Figure 5(c)
(Fourth Embodiment)**



**Kamata, Figure 10(b)
(Ninth Embodiment)**

The device of each embodiment includes film 2 (shaded red) formed on the active region under the gate electrode extending beneath the sidewall structure. (E.g., TSMC-1027, ¶¶56, 68, 94; §§V.B.3-5; *Unified Pats., LLC v. Oceana Innovations LLC*, No. IPR2020-01463, 2022 WL 500391, *17 (P.T.A.B. Feb. 14, 2022) (“patent drawing may serve as prior art ‘without referring to the surrounding

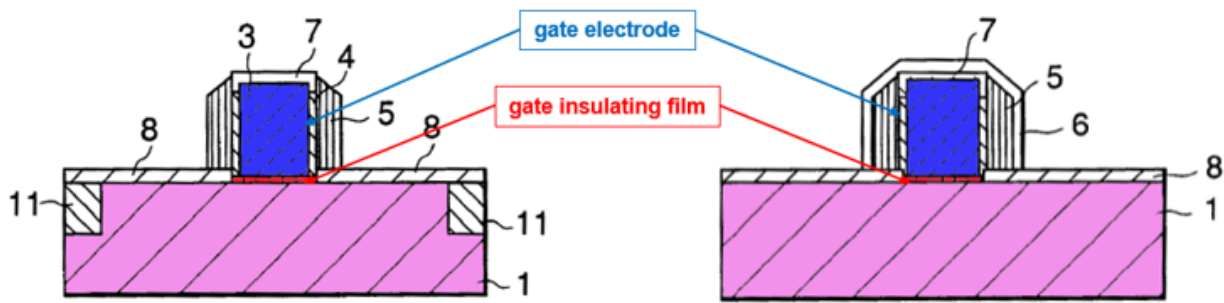
description’ if ‘the prior art features are clearly disclosed by the drawing.’”)
(citations omitted).) Gate insulating film 2 is disclosed as “**a high dielectric constant film** such as an oxide film with higher dielectric constant than the silicon oxide, containing at least an element selected from a group of Ti, Zr, Hf, Ta, La, Al Ba, Sr, Y, Pr and Gd, and a silicate film containing such an element.” (TSMC-1027, ¶52; *see also* TSMC-1027, ¶53 (listing exemplary high-k films including HfO₂).) By 2005, a POSITA would have been motivated to select HfO₂ given its known benefits, including, for example, “its superior thermal stability with poly-Si and reasonable band alignment.” (TSMC-1037, 2.4.1; *see also* TSMC-1032, 207 (HfO₂ “combines a high k (15–26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ...”); TSMC-1049, 134 (“Excellent dielectric properties ... suggest that HfO₂ is a promising material for the future gate dielectric application.”); TSMC-1003, ¶91.) HfO₂ also could be scaled down to a smaller EOT. (TSMC-1032, 207; TSMC-1003, ¶91.)

Kamata therefore discloses “*a gate insulating film [film 2] formed on an active region in a substrate and including Hf.*” (E.g., TSMC-1027, ¶73 (referring to “gate insulating film 2”), ¶¶8-10 (“present invention” device includes “a gate insulating film formed on a surface of the silicon substrate”), claim 1; TSMC-1003, ¶92.)

3. Limitation [1B]

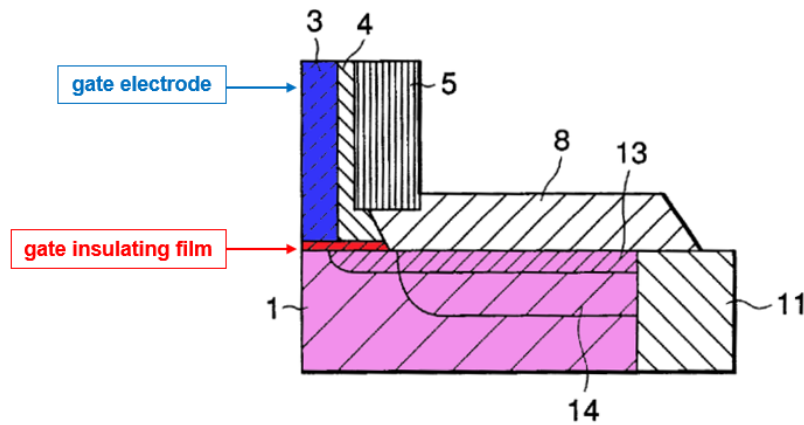
Kamata's first, fourth, and ninth embodiment each discloses "*a gate electrode formed on the gate insulating film*" [1B]. (TSMC-1003, ¶¶93-94.)

As shown below, each embodiment's device has a gate electrode (shaded blue) formed on film 2 ("*gate insulating film*"). (TSMC-1003, ¶94; TSMC-1027, ¶50 (explaining gate electrode 3 is "formed by depositing polycrystalline silicon" and performing a subsequent anisotropic etch), ¶¶68, 94, Figures 1A(a)-(c); *see also, e.g.*, TSMC-1027, claim 1 (reciting device with "gate electrode formed on the gate insulating film").)



**Kamata, Figures 1B(j)
(First Embodiment)**

**Kamata, Figure 5(c)
(Fourth Embodiment)**



**Kamata, Figure 10(b)
(Ninth Embodiment)**

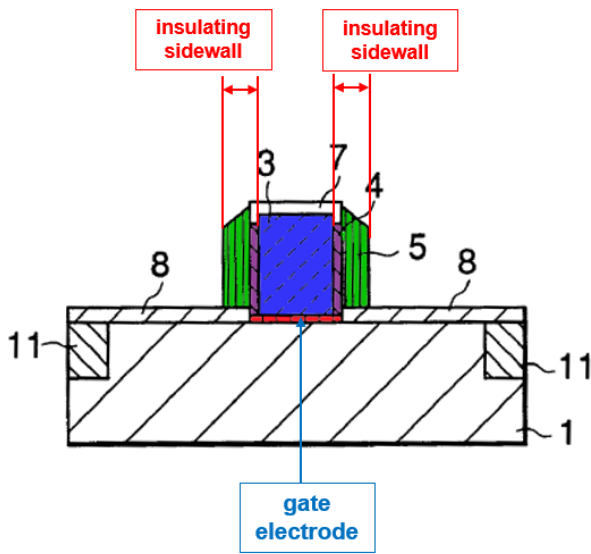
4. Limitation [1C]

Kamata's first, fourth, and ninth embodiment each discloses "*a insulating sidewall formed on each side surface of the gate electrode*" [1C]. (TSMC-1003, ¶¶95-99.)

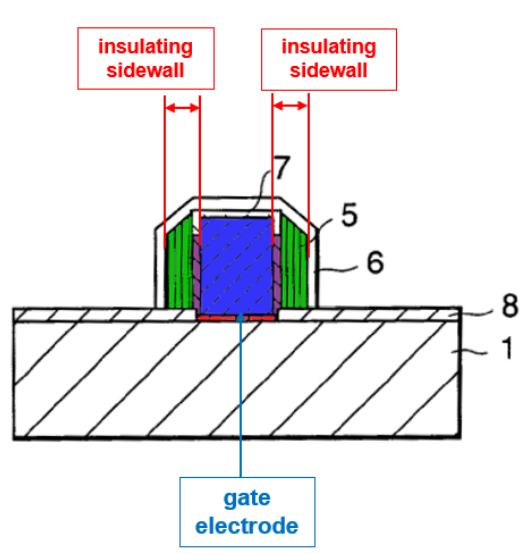
As shown in Figures 1B(j) and 5(c) below, the first and fourth embodiment devices each includes sidewall film 4 (shaded purple) and sidewall film 5 (shaded green) formed on the gate electrode's side surfaces (shaded blue). (TSMC-1027,

¶¶8-16 (“first aspect of the present invention [provides] a semiconductor device comprising ... multilayer type sidewall films [] formed on the respective side surface of the gate electrode”), 57 (referring to film 5 as “sidewall film 5”), 74 (referring to film 4 as “sidewall film 4”).) Sidewall film 4 is a silicon oxide film, and sidewall film 5 is a silicon nitride film—both are insulating films. (TSMC-1027, ¶¶50 (referring to “silicon nitride film (Si_3N_4) 5”), 58 (referring to “silicon oxide film 4”), 68.) Sidewall 4 and sidewall 5 are collectively an “*insulating sidewall*,” consistent with the ’076 patent’s disclosure.⁹ (TSMC-1003, ¶97.)

⁹ The ’076 patent uses the term “insulating sidewall” to refer to a single component (6:9), a collective structure of two components (2:60-65), and as a component having multiple layers (21:6-15).

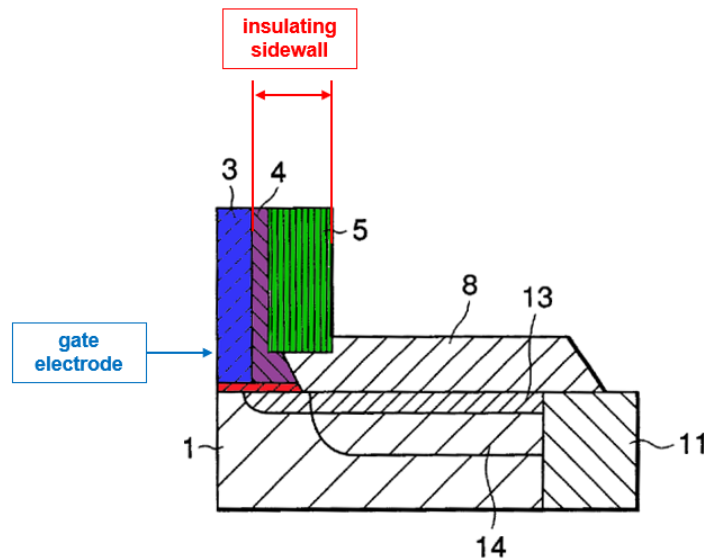


**Kamata, Figures 1B(j)
(First Embodiment)**



**Kamata, Figure 5(c)
(Fourth Embodiment)**

Figure 10(b) below depicts a portion of the ninth embodiment device. As shown, the device includes sidewall film 4 (shaded purple) and sidewall film 5 (shaded green) formed on the right side surface of the gate electrode. (TSMC-1027, ¶¶8-16, 57, 74; *see also* TSMC-1027, ¶¶50, 58, 94.) A POSITA would have understood this device includes corresponding sidewalls on the left side surface of the gate electrode. (TSMC-1003, ¶99 n.5.) Like the first/fourth embodiments, sidewall film 4 and sidewall film 5 are collectively an “*insulating sidewall*.” (TSMC-1003, ¶99.)



**Kamata, Figure 10(b)
(Ninth Embodiment)**

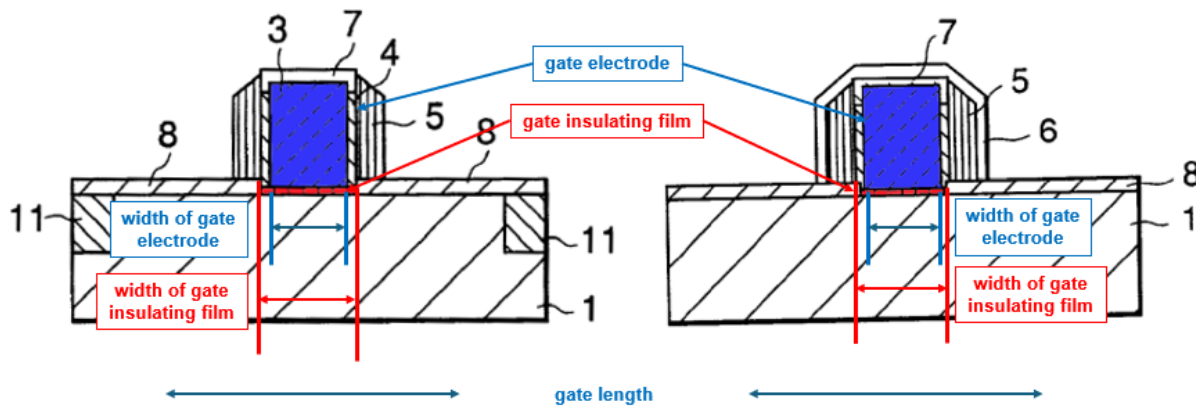
5. Limitation [1D]

Kamata’s first, fourth, and ninth embodiments each discloses “a width of the gate insulating film along a gate length¹⁰ is larger than a width of the gate electrode along the gate length” [1D]. (TSMC-1003, ¶¶100-05.)

As shown in Figures 1B(j) and 5(c) below for the first and fourth embodiments, the width along the gate length of high-k film 2 (shaded red) is larger than the width along the gate length of gate electrode 3 (shaded blue). (TSMC-1003, ¶101; *Unified*, 2022 WL 500391, *17.) This is confirmed by

¹⁰ The ’076 patent uses the term “gate length” to refer to a direction, specifically from source to drain regions. (TSMC-1003, ¶101 n.6.)

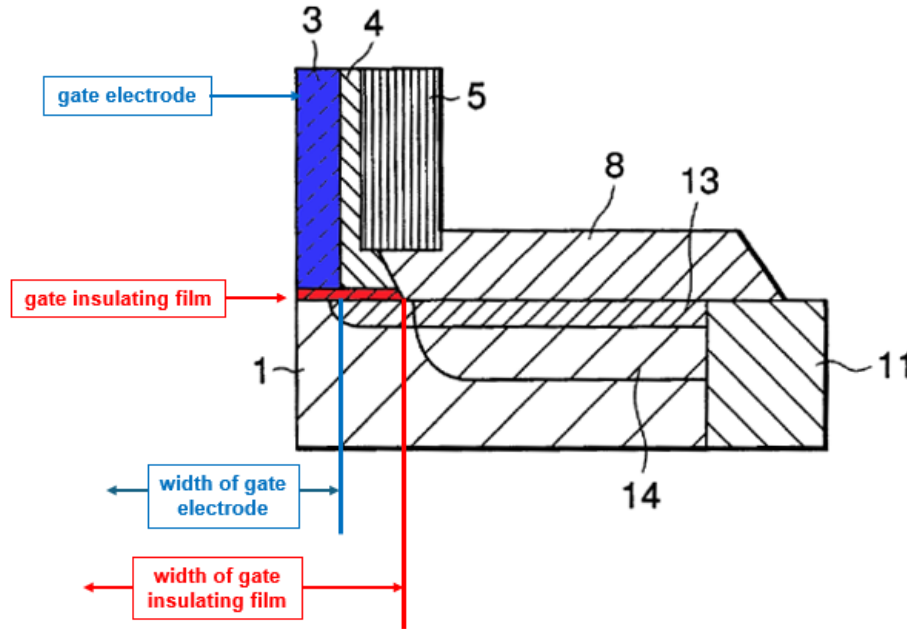
Kamata's manufacturing process, in which gate insulating film 2 and sidewall film 4 are etched together, with gate insulating film 2 extending beyond gate electrode 3 to under sidewall film 4. (TSMC-1027, Figures 1A(f), 1B(g), ¶¶50, 56, 68 (fourth embodiment); TSMC-1003, ¶102.).)



**Kamata, Figures 1B(j)
(First Embodiment)**

**Kamata, Figure 5(c)
(Fourth Embodiment)**

In the ninth embodiment, high-k film 2 (shaded red) extends beyond (protrudes from) under the gate electrode to under sidewall films 4 and 5. (TSMC-1003, ¶104; *see also* TSMC-1027, ¶50 (formation of gate electrode 3), 93 (describing deep diffusion region 14 after formation of sidewalls), 94, Figure 10(b) (below).) Although Figure 10(b) shows only a right portion of the device, a POSITA would have understood the left portion has a similar structure and therefore the width of high-k film 2 (shaded red) is larger than the width of the gate electrode (shaded blue). (TSMC-1003, ¶104.)



**Kamata, Figure 10(b)
(Ninth Embodiment)**

6. Limitation [1E]

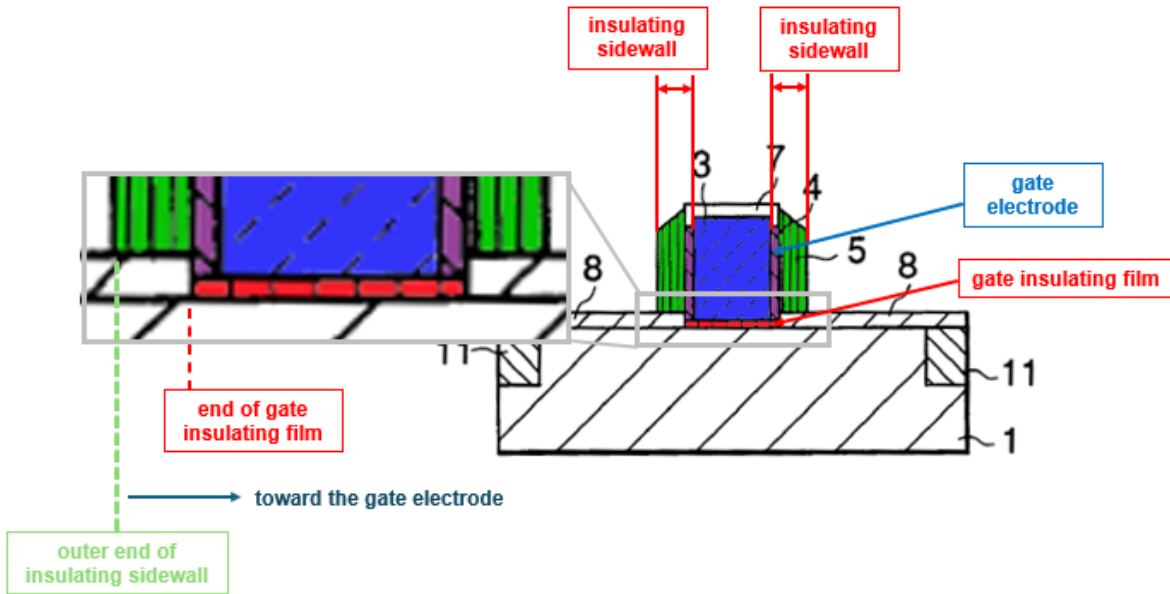
Kamata's first, fourth, and ninth embodiments each discloses "*an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode*" [1E]. (TSMC-1003, ¶¶106-11.)

The term "retract" first appeared in claim 21 of the application leading to the '076 patent (issued claim 1). The term "retract" does not appear anywhere in the '076 patent specification or any other patent in the same family. In the co-pending district court litigation, PO contends limitation [1E] is satisfied by a gate insulating film whose end is disposed inward at a distance from the outer end of the insulating sidewall and does not require any portion of the end of the gate insulating film to be in contact with the outer end of the insulating sidewall.

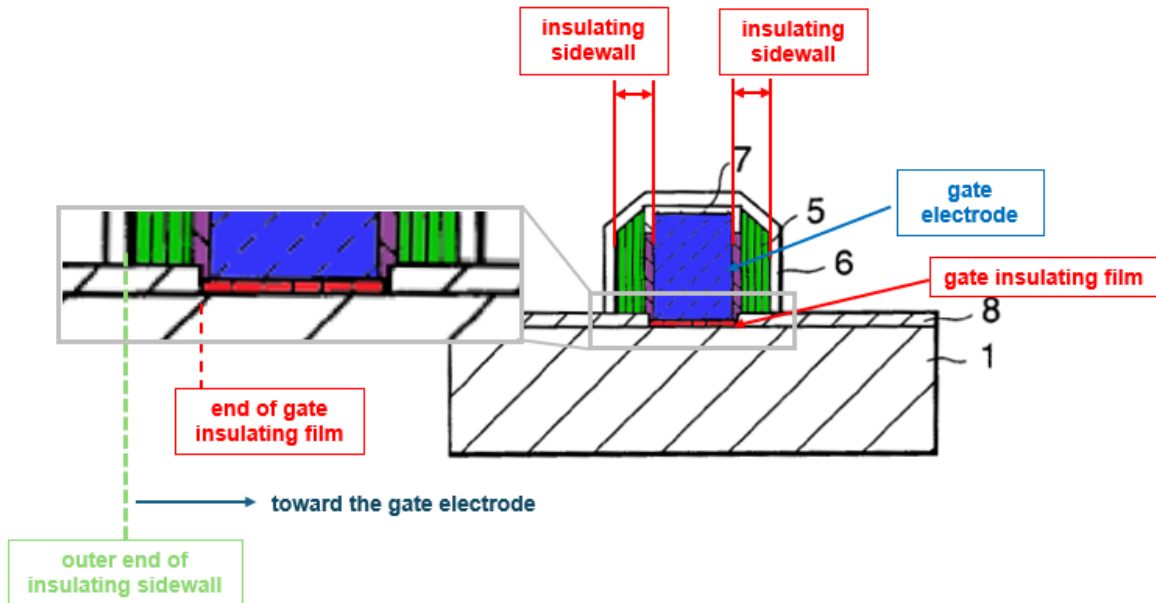
Kamata meets this limitation at least under PO's litigation allegation.¹¹ (TSMC-1003, ¶107.)

As discussed in §V.B.5, Kamata's gate insulating film 2 extends from under gate electrode 3 to under the "*insulating sidewall*" (collectively films 4 and 5). In Kamata's first and fourth embodiments, the end of the gate insulating film is perpendicular to the substrate surface. As shown in Figures 1B(j) and 5(c) below, the end of the gate insulating film is disposed inward from the outer end of sidewall film 5 (the outer end of the "*insulating sidewall*") toward the gate electrode. Accordingly, Kamata's first and fourth embodiments each discloses "*an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode*" [1E], at least under PO's litigation allegation. (TSMC-1003, ¶¶108-09; *Unified*, 2022 WL 500391, at *17.)

¹¹ PO's litigation allegations are subject to the district court's protective order. Petitioner reserves the right to seek discovery of these allegations in the present proceeding should PO take an inconsistent position.

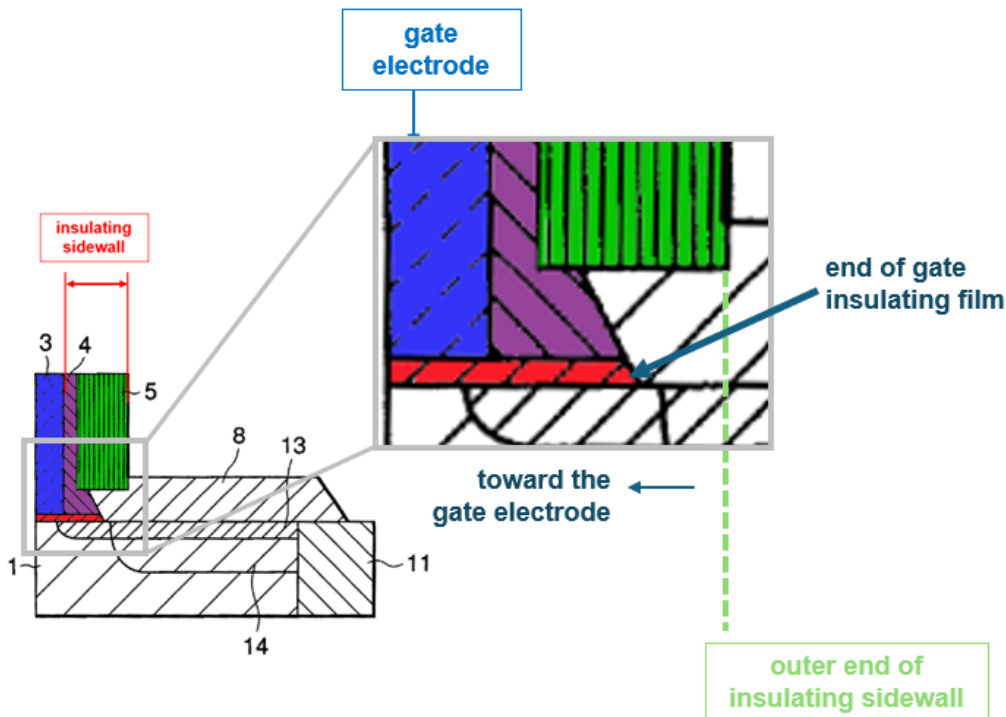


**Kamata, Figure 1B(j) with enlargement
(First Embodiment)**



**Kamata, Figure 5(c) with enlargement
(Fourth Embodiment)**

In Kamata's ninth embodiment, the end of the gate insulating film 2 (shaded red) slants upward and is not flush with the outer end of sidewall film 5; it is drawn inward from the outer end of sidewall 5 toward the gate electrode. Accordingly, Kamata's ninth embodiment discloses limitation [1E], at least under PO's litigation allegation. (TSMC-1003, ¶¶110-11; *Unified*, 2022 WL 500391, *17.)



Kamata, Figure 10(b) with enlargement

C. Claim 2

Kamata's first, fourth, and ninth embodiments each discloses "*a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film*" [2]. (TSMC-1003, ¶¶112-13.)

Kamata discloses “[i]t is desired that a **SiO_x ($0 < x \leq 2$) layer** ... is **interposed between the gate insulating film and the silicon substrate.**” (TSMC-1027, ¶¶54, 68 (relating fourth embodiment to first), 94 (relating ninth embodiment to first).) Therefore, in each embodiment, the SiO_x layer is a “*buffer insulating layer*” formed of “*a silicon oxide film*” disposed between the substrate and gate insulating film 2. (TSMC-1003, ¶113.)

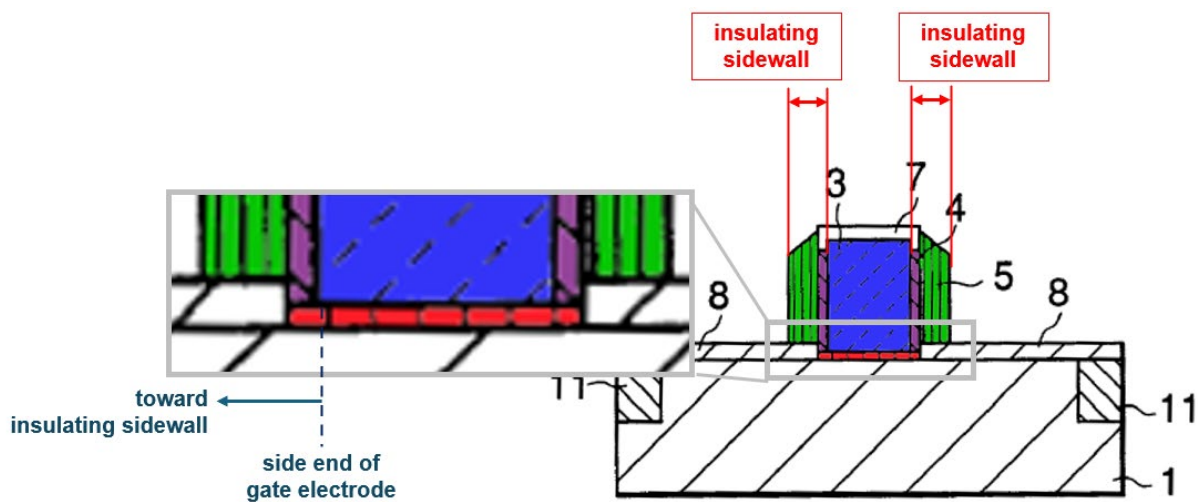
D. Claim 3

Kamata’s first, fourth, and ninth embodiments each discloses “*the gate insulating film is formed of a Hf based oxide*” [3]. (TSMC-1003, ¶¶114-16.) As discussed in §V.B.2, HfO₂ is used as Kamata’s gate insulating film 2. (TSMC-1027, ¶52; §V.B.2.) HfO₂ is a “*Hf based oxide.*” (TSMC-1003, ¶115; TSMC-1032, 207.)

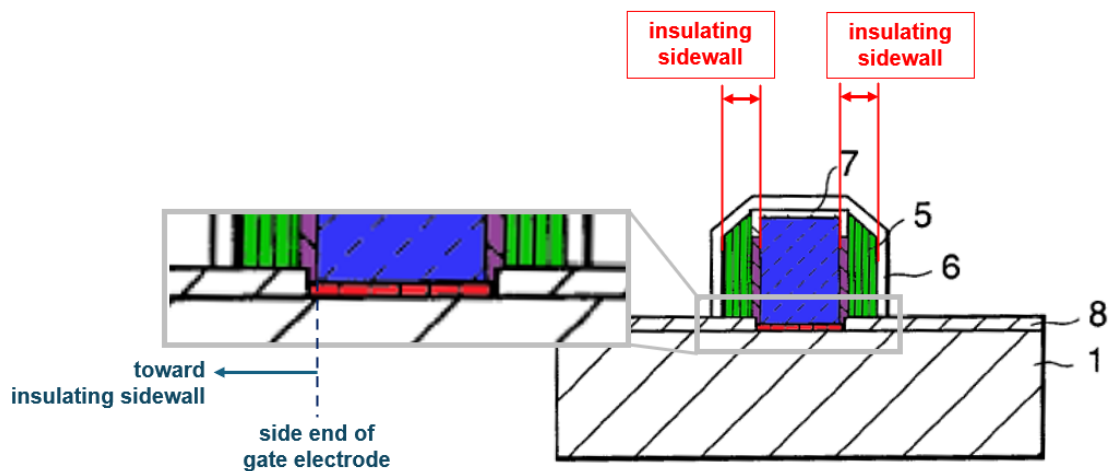
E. Claim 7

Kamata’s first, fourth, and ninth embodiments each discloses “*an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall*” [7]. (TSMC-1003, ¶¶117-18.)

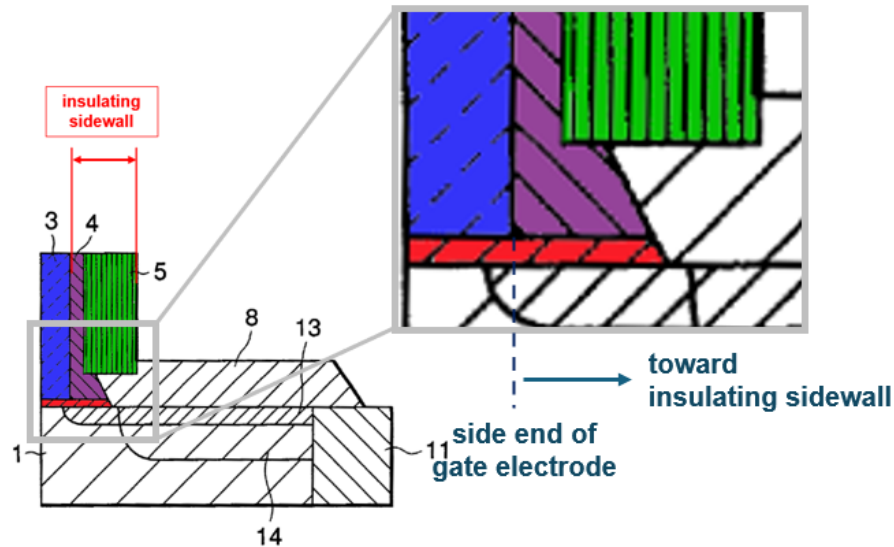
In Kamata’s devices, high-k dielectric film 2 extends (protrudes outward) from under the gate electrode to under at least first sidewall 4 which is part of the “*insulating sidewall.*” (See §V.B.5; TSMC-1027, Figures 1B(j), 5(c), 10(b)(below).)



Kamata, Figure 1B(j) with enlargement



Kamata, Figure 5(c) with enlargement



Kamata, Figure 10(b) with enlargement

F. Claim 8

Kamata’s first, fourth, and ninth embodiments each discloses “*the insulating sidewall has a double layer structure including an oxide film and a nitride film*” [8]. (TSMC-1003, ¶119.)

The “*insulating sidewall*” of each embodiment includes first sidewall film 4 and second sidewall film 5. (§V.B.4.) Film 4 is an **oxide** film and film 5 is a **nitride** film. (TSMC-1027, ¶¶50, 58.) A POSITA would have understood films 4 and 5 to each be a “layer” of the collective sidewall, consistent with the ’076 patent’s disclosure. (TSMC-1027, ¶¶16 (referring to “multilayer type sidewall films”), 50, 58; TSMC-1001, 21:6-15; TSMC-1003, ¶119.)

G. Claim 9

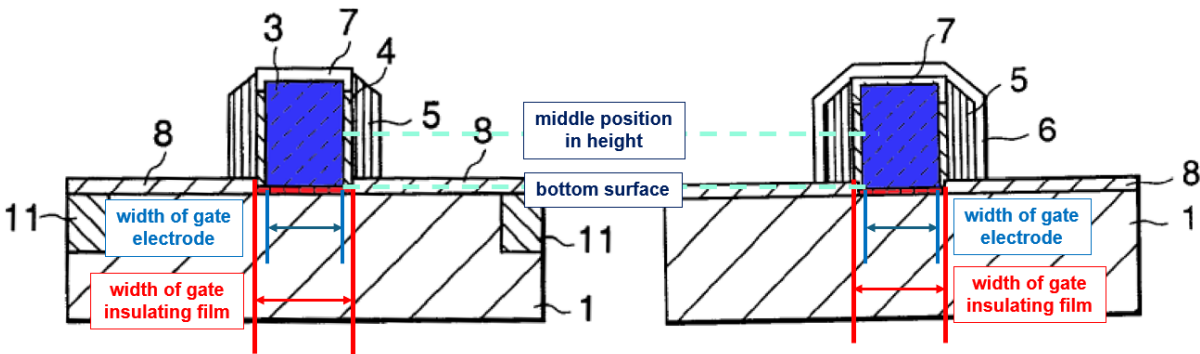
Claim 9 recites “*the insulating sidewall has a triple layer structure including a first oxide film, a nitride film, and a second oxide film*” [9]. Claim 9 requires no specific order for the recited films. Kamata’s first, fourth, and ninth embodiments each discloses claim 9. (TSMC-1003, ¶¶120-23.)

In Kamata’s embodiments, “**a liner layer** that may be a **silicon oxide film (SiO₂)** ... may be provided before the deposition of the silicon nitride film 5.” (TSMC-1027, ¶¶51-52; TSMC-1027, ¶¶50, 68, 94.) Accordingly, the “*insulating sidewall*” (first and second sidewall films) of Kamata’s first, fourth, and ninth embodiments has “*a triple layer structure*” comprising first silicon oxide sidewall 4 (“*a first oxide film*”), silicon oxide liner layer (“*a second oxide film*”), and Si₃N₄ second sidewall 5 (“*a first nitride film*”). (TSMC-1003, ¶¶121-23; §V.F (POSITA would have considered films 4 and 5 to be “layers”).)

H. Claims 10 and 13

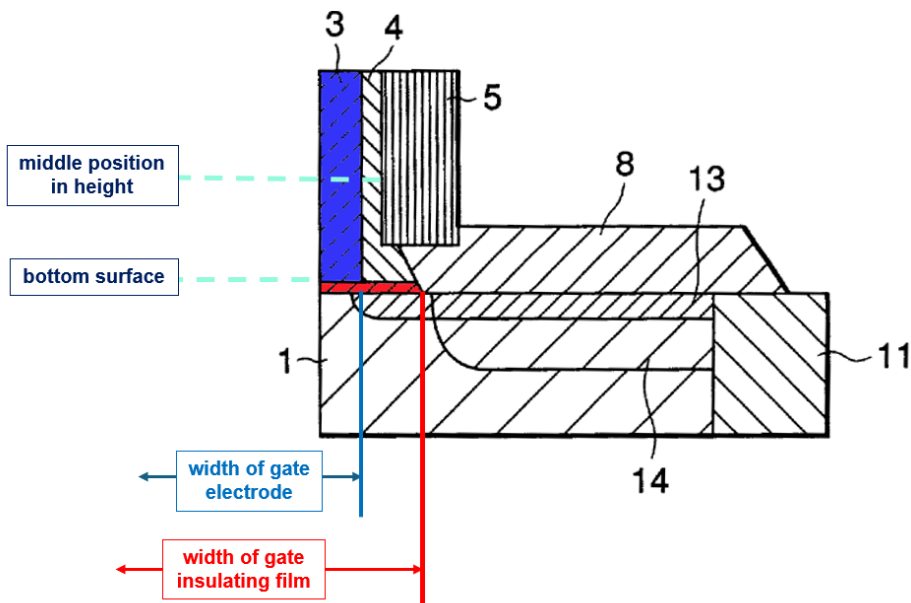
Kamata’s first, fourth, and ninth embodiments each discloses “*a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length*” [10], and “*width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length*” [13]. (TSMC-1003, ¶¶124-25.)

The width of Kamata's gate electrode is consistent across its entire height in each embodiment. Therefore, for the reasons discussed in §V.B.5, the width of the gate insulating film 2 (shaded red), including at film 2's bottom surface, is larger than the width of gate electrode 7 (shaded blue) at both the bottom surface and a middle position in height of the gate electrode. (TSMC-1003, ¶125; *Unified*, 2022 WL 500391, *17.)



Kamata, Figures 1B(j) (First Embodiment)

Kamata, Figure 5(c)
(Fourth Embodiment)



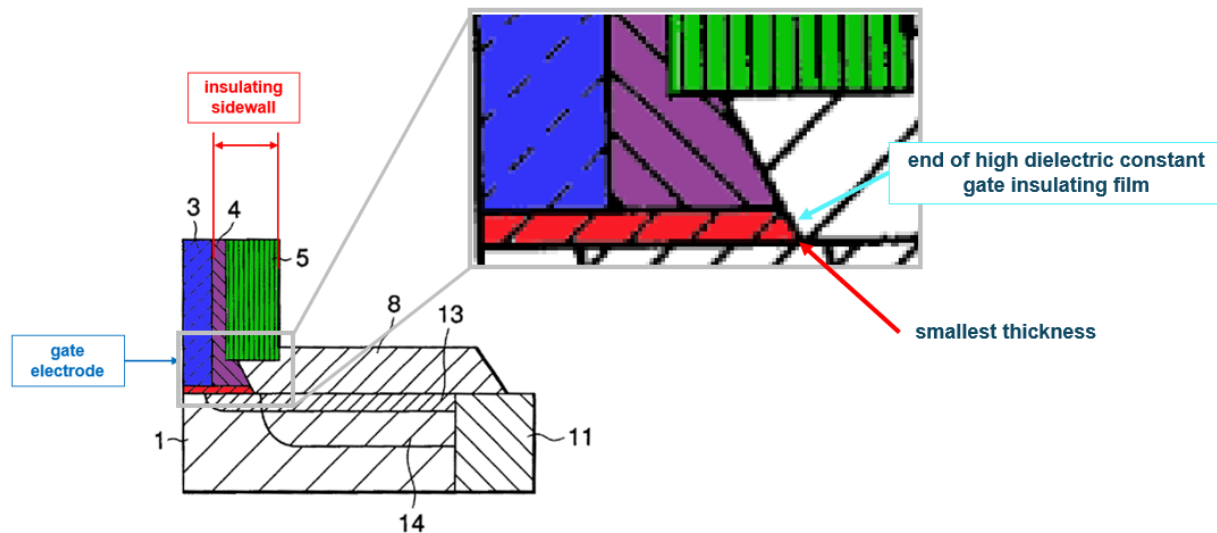
Kamata, Figure 10(b) (Ninth Embodiment)

I. Claims 11-12

Kamata's ninth embodiment discloses "*the end of the gate insulating film located under the insulating sidewall has a tapered surface*" [11] and "*the gate*

insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof [12]. (TSMC-1003, ¶¶126-28.)

Gate insulating film 2 extends from under gate electrode 3 to under sidewall films 4 and 5 (collectively the “*insulating sidewall*”). (§V.B.5.) As shown in Figure 10(b) below, the end surface of gate insulating film 2, located under the “*insulating sidewall*,” diminishes in thickness from its maximum (which is equivalent to its thickness under the gate electrode) to its smallest at its far end—it is “*tapered*.” (TSMC-1027, ¶93; *see also* TSMC-1027, ¶¶18, 85 (describing formation of slanted surfaces in embodiment having same slanted gate dielectric and slanted epitaxially grown film 8) ; *Unified*, 2022 WL 500391, *17.)



**Kamata, Figure 10(b) with enlargement
(Ninth Embodiment)**

VI. GROUND 2: Kamata-Koyama Combination Renders Claim 4 Obvious.

Kamata's high-k gate insulating film 2 is, e.g., Hf silicate. (TSMC-1027, ¶52.) Kamata does not explicitly disclose the gate insulating film "*is formed of a HfSiON film*" [4]. Koyama discloses this. The devices of the combination of Kamata (first/fourth/ninth embodiments) and Koyama render claim 4 obvious. (TSMC-1003, ¶¶129-33.)

According to Koyama, "Hf(Zr) silicates are considered to be prospective high-K materials due to their modest dielectric constants and good interface properties." (TSMC-1029, 849.) Because a "HfSiON gate dielectric with excellent thermal stability has been proposed," Koyama studied "the effects of nitrogen on the improved thermal stability and electrical characteristics of this dielectric." (*Id.*) Koyama concluded "nitrogen [in HfSiON] enhances the dielectric constant of silicates" and "boron penetration is substantially suppressed in the HfSiON during high temperature annealing." (*Id.*) Koyama's experimental results "strongly suggest that HfSiON is the most probable material for first generation high-K gate dielectrics." (TSMC-1029, 850.)

A POSITA would have been motivated to combine Koyama's teachings regarding use of HfSiON as a high-k gate dielectric with each of Kamata's first, fourth, and ninth embodiments, thereby providing devices where gate insulating film 2 "*is formed of a HfSiON film.*" (TSMC-1003, ¶131.) Koyama and Kamata are

in the same field as the '076 patent, “a semiconductor device and a method for fabricating the semiconductor device.” (TSMC-1001, 1:18-19; TSMC-1027, ¶3; TSMC-1029, Title; TSMC-1003, ¶129.)

Kamata presents Hf silicate as an option for its high-k gate dielectric. (TSMC-1027, ¶52.) This suggestion would have motivated a POSITA to investigate Hf silicate options and would have led the POSITA to Koyama. (TSMC-1003, ¶132.) Koyama discloses that, among Hf silicates, HfSiON was the most probable high-k material in view of the benefits resulting from its incorporation of nitrogen. (TSMC-1029, 849.) Thus, a POSITA would have been motivated to use HfSiON for the benefits taught by Koyama to improve device operation, including improved thermal stability and electrical characteristics and enhanced dielectric constant. (*Id.*; TSMC-1003, ¶132.)

Moreover, the combination is nothing more than use of a known technique (Koyama’s use of HfSiON as a gate insulating film) to improve similar devices in the same way for the above reasons. *KSR Int’l. Co. v. Teleflex Inc.*, 550 U.S. 398, 416-417 (2007); TSMC-1003, ¶133. Because techniques for formation of a gate dielectric were well-established and formation of high-k dielectric films such as HfSiON uses these processes, a POSITA would have had a reasonable expectation of success and the combination would have yielded predictable results. (TSMC-1003, ¶133; *see also* TSMC-1032, 561-62.)

VII. GROUND 3: Kamata-Sim Combination Renders Claim 6 Obvious.

Kamata discloses use of HfO₂ as a high-k gate insulating film (TSMC-1027, ¶53) but does not expressly disclose the high-k gate dielectric “*has a thickness of 2 nm or less*” [6]. Sim, which “systematically evaluated the effects of high-k film thickness on charge trapping and channel carrier mobility,” discloses this teaching. (TSMC-1024, 218-19, 221.) Sim and Kamata are in the same field as the ’076 patent, “a semiconductor device and a method for fabricating the semiconductor device.” (TSMC-1001, 1:18-19; TSMC-1027, ¶3; TSMC-1024, Abstract; TSMC-1003, ¶134.) The devices of the combination of Kamata (first/fourth/ninth embodiments) and Sim disclose “*a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less*” [6]. (TSMC-1003, ¶¶134-35.)

A POSITA would have been motivated to adopt Sim’s solution of forming a gate insulating film with a thickness of 20Å (2 nm) or less in Kamata’s first/fourth/ninth embodiments. Sim expressly motivates the combination, finding that reducing the thickness of HfO₂ to below 20Å (2 nm) enhances mobility and reduces charge trapping, key issues in ensuring the performance and scalability of semiconductor devices. (TSMC-1024, 221 (“Scaling the physical thickness of the HfO₂ dielectric to below 20Å [2 nm] causes less charge trapping and higher mobility.”), 219 (“Even within 100µs, a 33Å HfO₂ sample shows significant

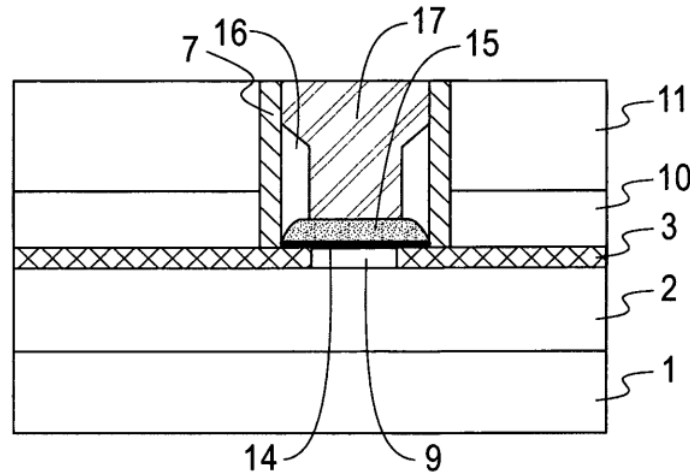
current reduction while a 18Å HfO₂ sample is free from transient charging within the detection limits.”.) A POSITA would further have understood this improvement aligns with the continued miniaturization of devices, which both Kamata and Sim emphasize is crucial to advancing CMOS technology. (TSMC-1027, ¶5; TSMC-1024, 218; TSMC-1003, ¶137.)

Additionally, the combination is nothing more than use of a known technique (Sim’s HfO₂ dielectric layer with less than 20Å thickness) to improve similar devices in the same way for the reasons above. *KSR*, 550 U.S. at 416-417; TSMC-1003, ¶138. A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable because Sim uses a well-known process, atomic layer deposition (ALD), for fabricating high-k films. (TSMC-1024, 218; TSMC-1032, 17-19; TSMC-1003, ¶138.)

VIII. GROUND 4: Guha Renders Claims 1-3, 7-8, 10-13 Obvious.

A. Overview

Guha’s Figure 12 device includes gate 17 with gate spacer structure 16 and isolating spacer 7. (TSMC-1028, ¶¶43-45.) Dielectric layer 15, formed on gate-isolating layer 14, extends from under gate 17 to under gate spacer 16. (TSMC-1028, ¶¶38, 43-44.)



Guha, Figure 12

B. Independent Claim 1

1. Preamble [1P]

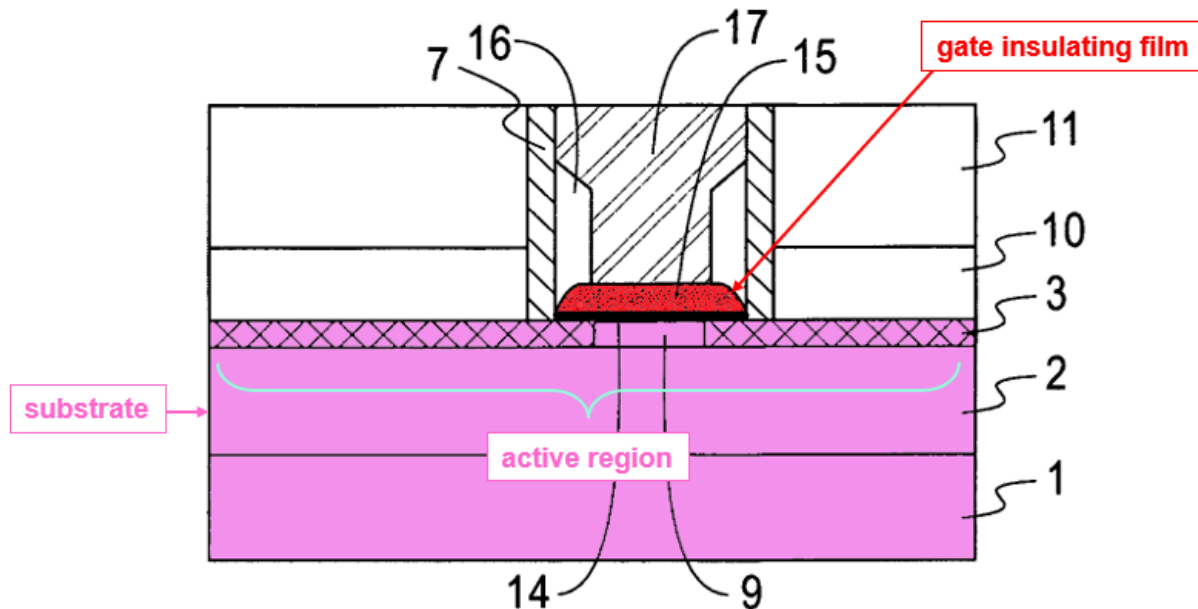
Guha's Figure 12 device includes substrate 1 and channel layer 3 each "compris[ing] any **semiconducting material**." (TSMC-1028, ¶¶22-23, ¶¶43-45 (relating Figure 9's first embodiment device to Figure 12 device); *see Google*, 2022 WL 4287797, *9 n.9). Guha's Figure 12 device is a "*semiconductor device*" [1P]. (TSMC-1003, ¶144.)

2. Limitation [1A]

Guha discloses "*a gate insulating film formed on an active region in a substrate and including Hf*" [1A]. (TSMC-1003, ¶¶145-49.)

Guha's Figure 12 device, below, includes substrate 1, which "may be of the **n or p-type** depending on the desired device to be fabricated." (TSMC-1028, ¶¶22, 43.) Channel layer 3 is further provided over buried oxide layer 2 which "can be

omitted.” (*Id.*) Substrate 1, channel layer 3, and buried oxide layer 2 (if present) are collectively “a substrate” (shaded pink). (TSMC-1003, ¶145.)



Guha, Figure 12

Guha’s substrate contains “active device regions.” (TSMC-1028, ¶¶22, 43.) Source/drain extensions “are formed by implanting dopants ... into the channel layer 3,” further indicating presence of an active region in Guha’s Figure 12 device. (TSMC-1028, ¶¶26, 43.) A POSITA would have understood Guha’s device has “an active region in a substrate.” (TSMC-1028, ¶22; TSMC-1003, ¶146.)

Guha’s Figure 12 device includes gate-isolating layer 14 (shaded black) formed on a portion of channel layer 3 which is part of the “active region in a substrate.” (TSMC-1028, ¶¶37, 43.) Dielectric layer 15 (shaded red), “comprising a high-k dielectric material,” is “formed only on the gate-isolating layer 14.”

(TSMC-1028, ¶¶38, 43.) Dielectric layer 15 is therefore “*a gate insulating film formed on*¹² *an active region in a substrate.*” (TSMC-1003, ¶¶147-49; *see also* TSMC-1028, ¶37 (gate-isolating layer 14 “acts as a buffering layer between channel 9 and the” high-k dielectric).)

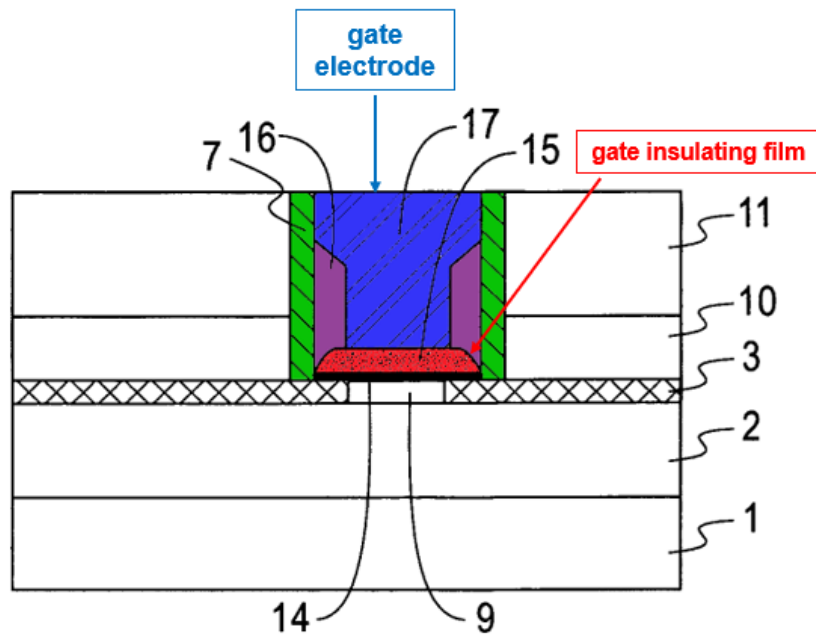
Guha discloses that high-k dielectric layer is a material such as “**hafnium oxide, hafnium silicate**, aluminum oxide or zirconium oxide.” (TSMC-1028, ¶38.) A POSITA would have been motivated to select hafnium oxide or hafnium silicate because of their known benefits, e.g., HfO₂’s “superior thermal stability with poly-Si and reasonable band alignment,” and HfSiON’s “improved thermal stability and electrical characteristics.” (TSMC-1037, 2.4.1; TSMC-1029, 849; *see also* TSMC-1032, 207 (HfO₂ “combines a high k (15–26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ...”; HfO₂ can be scaled down to a smaller EOT); TSMC-1003, ¶148.) Guha therefore discloses a “*gate insulating film [film 2] ... including Hf.*”

¹² The ’076 patent uses the term “formed on” to indicate relative position and does not require direct contact. (*E.g.*, 7:42-44 (“insulating sidewall 7 is formed on each side surface of the gate electrode 5 with an offset sidewall 6 interposed therebetween”).)

3. Limitation [1B]

Guha discloses “a gate electrode formed on the gate insulating film” [1B].
(TSMC-1003, ¶¶150-52.)

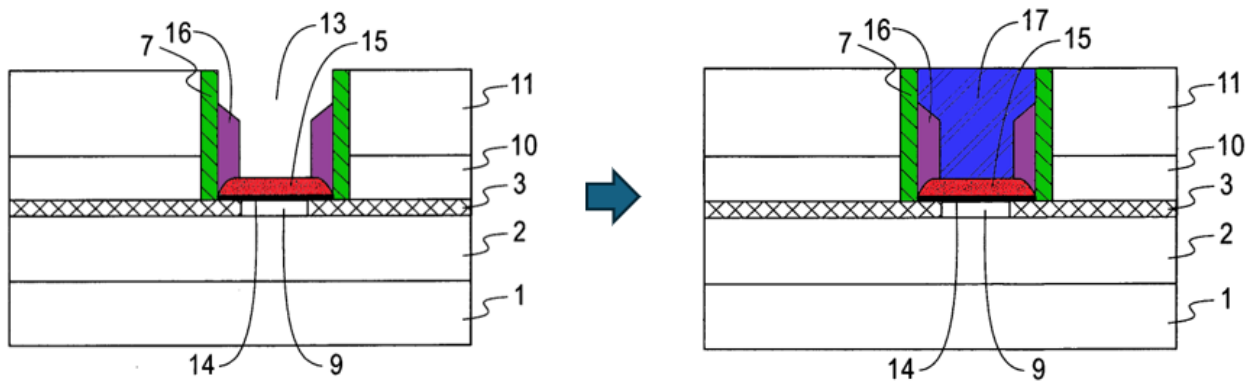
In Guha’s Figure 12 below, gate 17 (shaded blue) is formed on high-k dielectric layer 15 (shaded red). Gate 17 is formed of a “conductive material” and therefore is “a gate electrode formed on the gate insulating film.” (TSMC-1028, ¶¶41, 45; TSMC-1003, ¶¶150-51; *Unified*, 2022 WL 500391, *17.)



Guha, Figure 12

Guha’s fabrication process confirms the Figure 12 structure. For example, Guha describes cavity 13 (Figure 11 (left)) is “filled with a conductive material to form the **gate 17**” by “depositing the material ... **onto the dielectric layer 15**”, resulting in formation of the gate electrode over dielectric layer 15. (TSMC-1028,

¶¶41, 44 (associating gate formation in Figure 12 (right) with first embodiment process), 45; TSMC-1003, ¶152.)



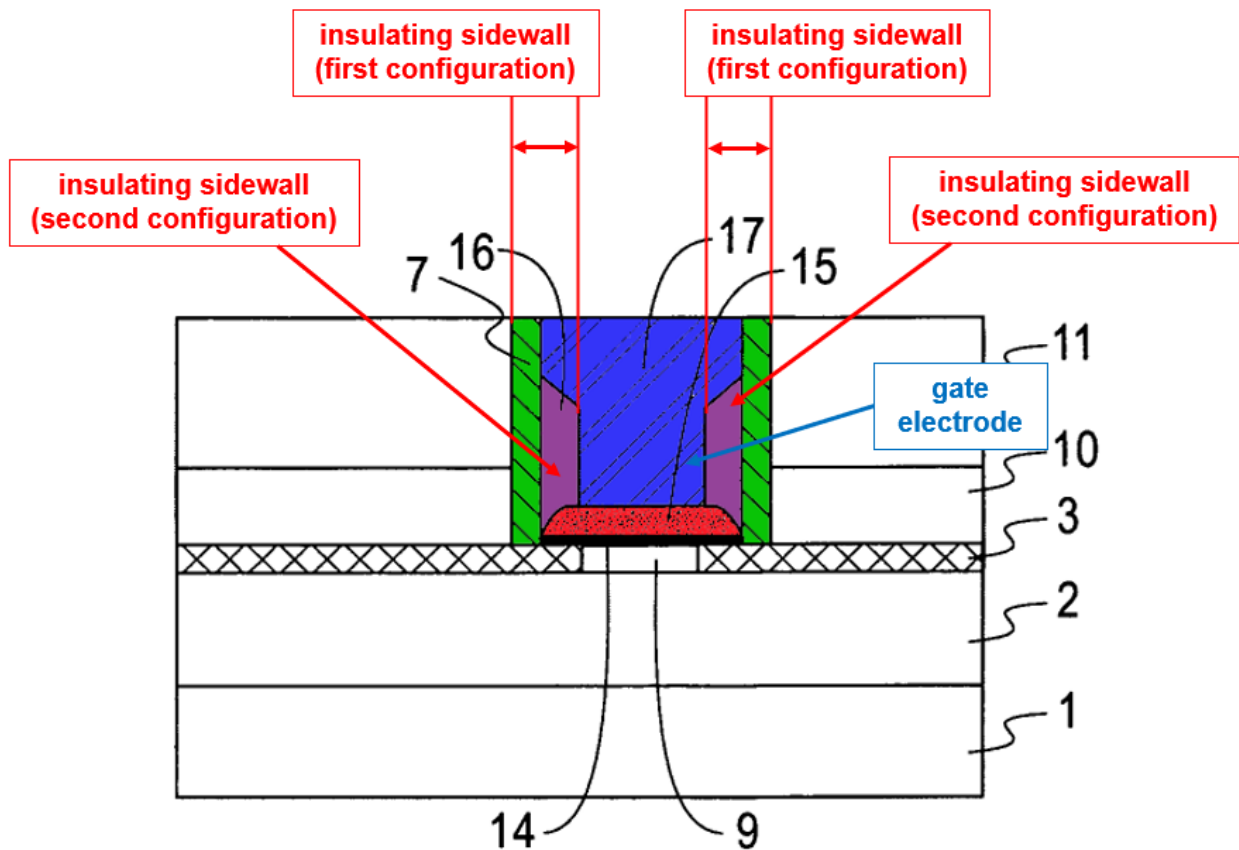
Guha, Figure 11 (left), Figure 12 (right)

4. Limitation [1C]

Guha discloses “a insulating sidewall formed on each side surface of the gate electrode” [1C]. (TSMC-1003, ¶¶153-61.)

Guha’s device includes gate spacers 16 (shaded purple) and isolating spacers 7 (shaded green) on gate electrode 17’s side surfaces (shaded blue). (TSMC-1028, ¶¶28 (formation of spacers 7), 44 (formation of spacers 16 in Figure 12 device), 43 (associating Figure 12 device to process steps associated with Figures 1-7).)

Although Guha refers to each as a “spacer,” as noted above, “spacer” and “sidewall” are often used interchangeably. (TSMC-1003, ¶156; §IV.B.3.) Further, a POSITA would thus have understood them to be “sidewalls.” (E.g., TSMC-1028, ¶¶40, 44-45; TSMC-1003, ¶156.)



Guha, Figure 12

Gate spacers 16 are made of “e.g. an oxide or other suitable material.”

(TSMC-1028, ¶¶40, 43.) Through use of gate spacers 16, “the interface between the bottom of the gate 17 and the dielectric layer 15 is better defined and offers a better control over the channel 9.” (TSMC-1028, ¶45.) To provide such benefits, a POSITA would have understood gate spacers 16 to be formed of an insulating oxide material. (TSMC-1003, ¶¶157; TSMC-1034, 9, 75; TSMC-1033, 79-80.)

Isolating spacers 7 are “composed of any insulating material including, for

example, an oxide, nitride, oxynitride or any combination thereof” with the “preferred material [being] silicon nitride.” (TSMC-1028, ¶¶28, 43.)

Gate spacers 16 and isolating spacers 7 are collectively an “*insulating sidewall formed on each side surface of the gate electrode*” [1C], consistent with the ’076 patent’s disclosure. (TSMC-1003, ¶159; TSMC-1001, 2:60-65 (“insulating sidewall” includes two sidewalls).) Petitioner refers to this as the first “*insulating sidewall*” configuration.

Alternatively, gate spacers 16 alone disclose an “*insulating sidewall formed on each side surface of the gate electrode*” [1C], consistent with the ’076 patent’s disclosure. (TSMC-1003, ¶160; TSMC-1001, 6:9 (“insulating sidewall” has a single component).) Petitioner refers to this as the second “*insulating sidewall*” configuration.

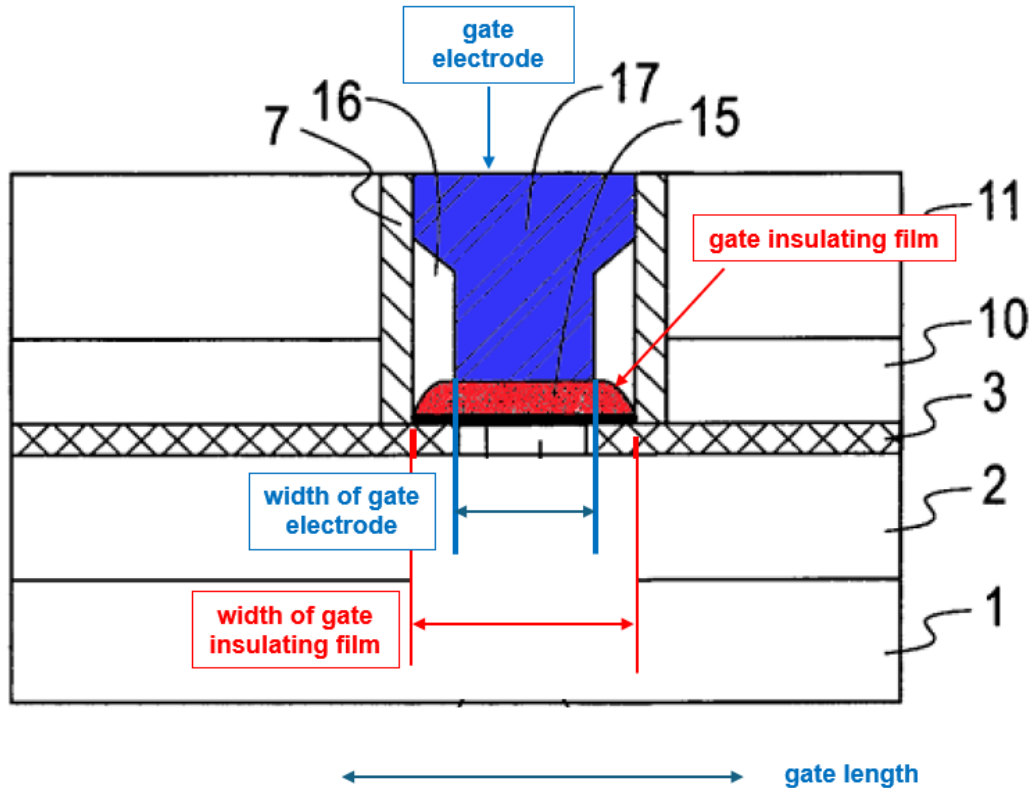
Both the first and second “*insulating sidewall*” configurations teach limitation [1C]. (TSMC-1003, ¶161.)

5. Limitation [1D]

Guha discloses “*a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length*” [1D]. (TSMC-1003, ¶¶162-64.)

As shown in Figure 12 below, the width of dielectric layer 15 (shaded red) is larger than the width of the bottom portion of the gate electrode (shaded blue).

(TSMC-1003, ¶162; *see also* TSMC-1028, ¶¶41, 43-45 (describing formation of spacers 16 in the cavity followed by deposition of the gate electrode).)

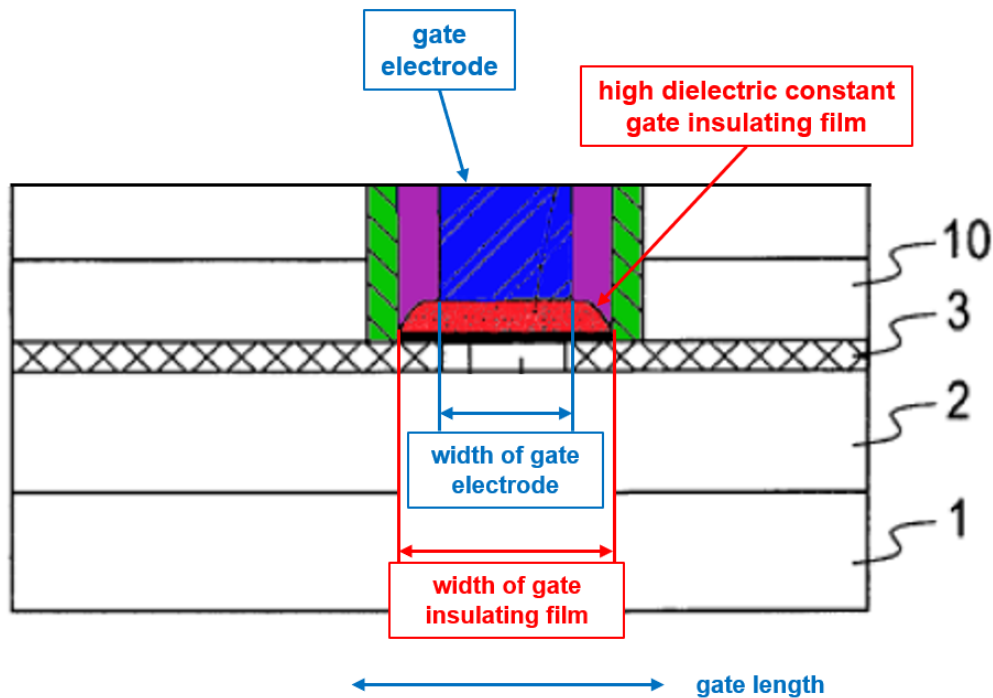


Guha, Figure 12

Should an argument be made the width of the gate electrode at its upper portion is equal to the width of dielectric layer 15 and therefore Guha fails to disclose this limitation, such an argument is improper. First, nothing in this limitation requires the gate electrode width at all heights to be smaller than the width of the gate insulating film. The limitation recites broadly “*a width of the gate electrode.*” Claim 10 narrows this limitation, reciting that “*a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a*

bottom surface of the gate electrode along the gate length,” and claim 13 also narrows this limitation, reciting “*the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length.*” (TSMC-1003, ¶163.)

Second, Guha discloses “internal spacer 16a and 16b may also have a rectangular cross-section, e.g., by polishing or removing the upper curved region to form a horizontal portion of the internal surface.” (TSMC-1028, ¶47.) A POSITA would have understood, with this teaching, the expanded upper portion of the gate electrode is removed along with the slanted upper portion of spacers 16 to obtain a rectangular cross-section. (TSMC-1003, ¶164.) In this embodiment, shown in modified Figure 12 below, the gate electrode width is the same at the bottom and the top, meeting limitation [1D], even under an impermissibly narrow interpretation. *See Boston Sci. Scimed, Inc. v. Cordis Corp.*, 554 F. 3d 982, 991 (Fed. Cir. 2009) (“[c]ombining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness”).



Guha, Modified Figure 12

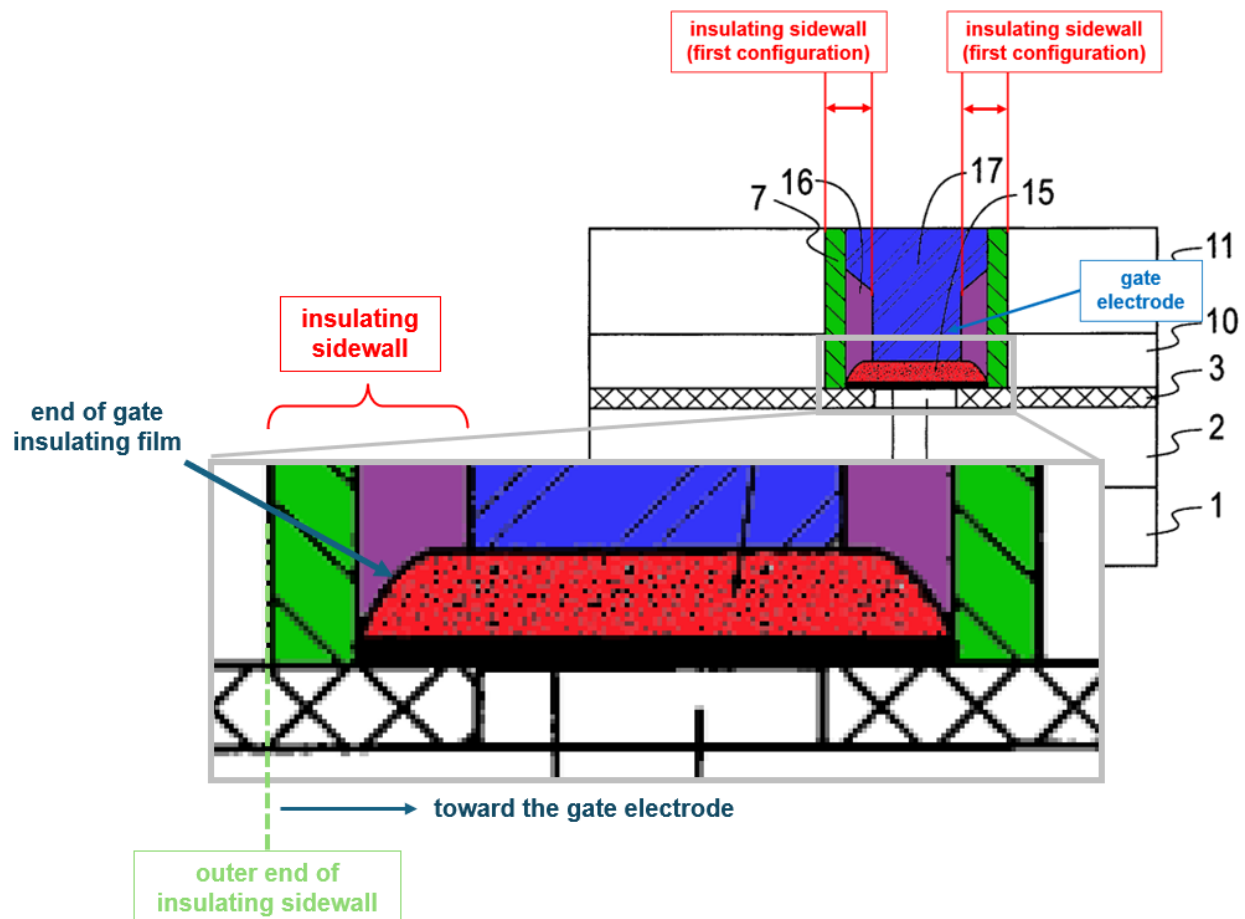
6. Limitation [1E]

Guha discloses “an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode” [1E] under both the first and second “insulating sidewall” configurations. (TSMC-1003, ¶¶165-69.)

a. First Configuration (Gate Spacer 16 and Spacer 7)

As shown below, the rounded end of dielectric layer 15 (shaded red) is under spacer 16 (shaded purple), but not under spacer 7 (shaded green). Therefore, the end of dielectric layer 15 is disposed inward at a distance from the outer end of the “insulating sidewall” (outer end of spacer 7) toward the gate electrode. (TSMC-

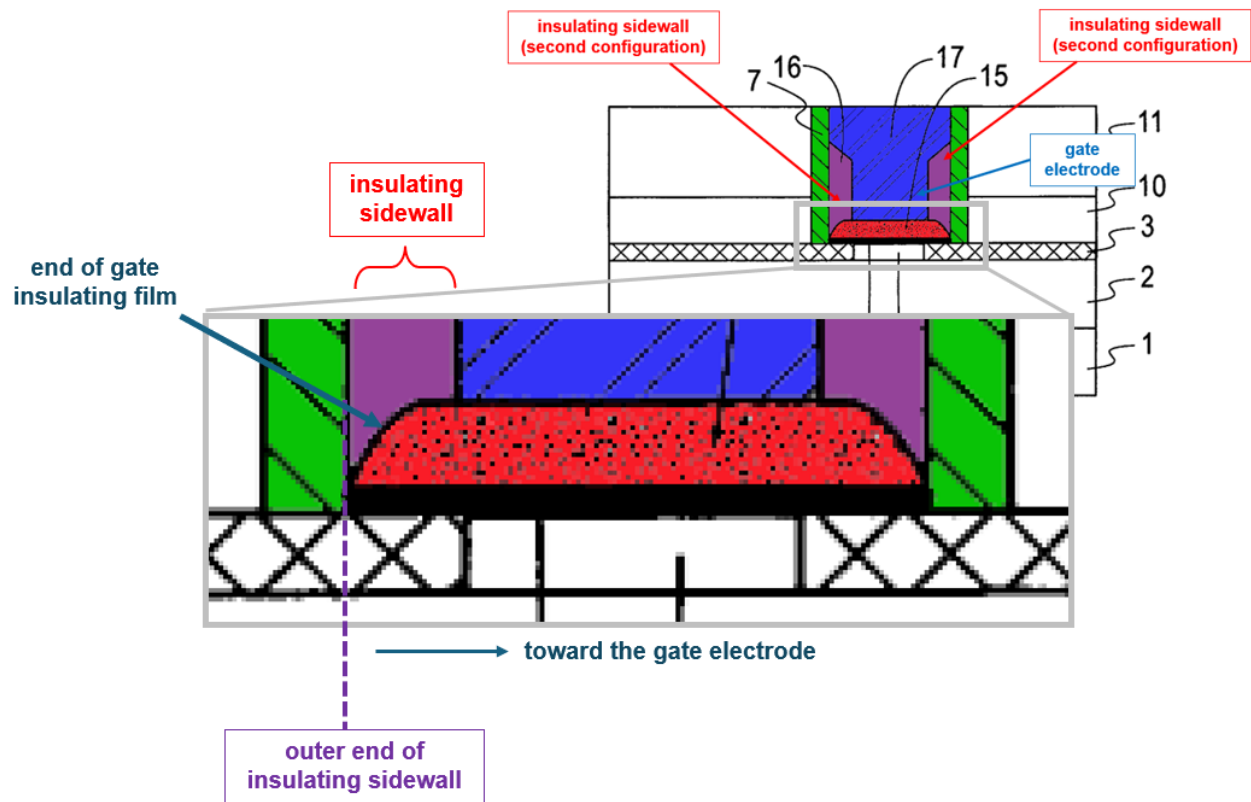
1003, ¶166.) This is confirmed by Guha’s manufacturing process, in which dielectric layer 15 is formed in cavity 13 after formation of isolating spacers 7 but before gate spacers 16. (TSMC-1028, ¶¶43-45; TSMC-1003, ¶167.) Accordingly, Guha discloses “an end of the gate insulating film under the insulating sidewall [spacer 16 and spacer 7] is retracted from an outer end of the insulating sidewall [outer end of spacer 7] toward the gate electrode” [1E], at least under PO’s litigation allegation. (TSMC-1003, ¶167; *Unified*, 2022 WL 500391, *17.)



Guha, Figure 12 with enlargement

b. Second Configuration (Gate Spacer 16)

As shown below, the point at which the gate insulating film is the thinnest contacts the outer end of the insulating sidewall (outer end of spacer 16). (TSMC-1028, Figure 12.) Due to its rounded shape, the end of gate insulating film 2 curves inward from the outer edge of spacer 16 towards the gate electrode, as shown below. Accordingly, Guha discloses an “*end of the gate insulating film under the insulating sidewall [spacer 16] is retracted from an outer end of the insulating sidewall toward the gate electrode*” [1E]. (TSMC-1003, ¶169; *Unified*, 2022 WL 500391, at *17.)

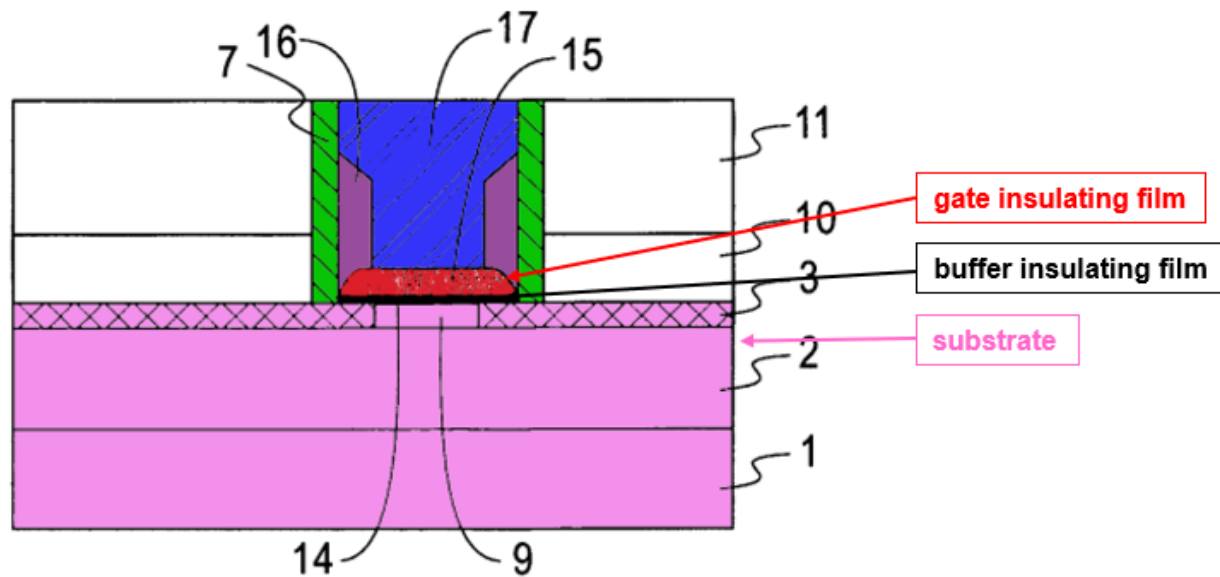


Guha, Figure 12 with enlargement

C. Claim 2

Guha discloses “*a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film*” [2]. (TSMC-1003, ¶¶170-72.)

Gate-isolating layer 14 (shaded black) “**acts as a buffering layer** between channel 9 and the dielectric material to be deposited thereon” (i.e., high-k dielectric 15). (TSMC-1028, ¶¶37, 43, Figure 12 (below).) Channel 9 is part of the substrate. (§VIII.B.2.) Gate-isolating layer 14 is therefore “*a buffer insulating film ... provided between the substrate and the gate insulating film.*” (TSMC-1003, ¶¶171-72.) The “preferred material for the gate-isolating layer 14 is silicon oxide” and therefore Guha’s gate isolating layer is “*formed of a silicon oxide film.*” (TSMC-1028, ¶¶37, 43; TSMC-1003, ¶¶171-72.)



Guha, Figure 12

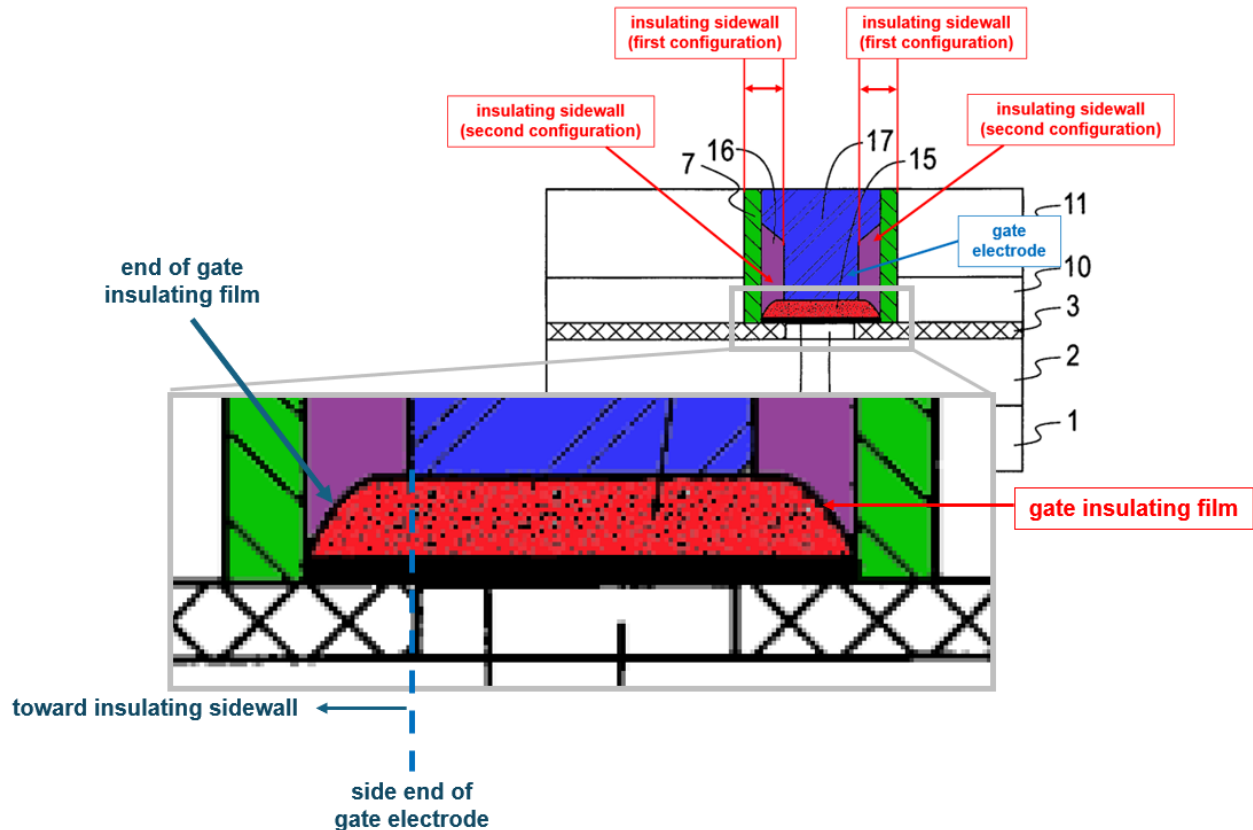
D. Claim 3

Guha discloses “*the gate insulating film is formed of a Hf based oxide*” [3]. (TSMC-1003, ¶173.) Guha’s dielectric layer 15 (“*gate insulating film*”) “preferably compris[es] a high-K dielectric material” such as “**hafnium oxide**,” which is “*a Hf based oxide*.” (TSMC-1028, ¶¶38, 43.) A POSITA would have been motivated to select HfO₂ in light of its known benefits, including thermal stability, band alignment, and ability to scale. (TSMC-1037, 2.4.1; TSMC-1032, 207; TSMC-1003, ¶173; §VIII.B.2.)

E. Claim 7

Guha discloses “*an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall*” [7], under both the first and second “*insulating sidewall*” configurations. (TSMC-1003, ¶¶174-75.)

As discussed in §§VIII.B.5-6, dielectric layer 15 in Guha’s Figure 12 device extends from under the gate electrode to under spacer 16 (i.e., it protrudes from the side end of the gate electrode). Spacer 16 alone is the recited “*insulating sidewall*” (second configuration) or alternatively spacer 16 and spacer 7 are collectively the “*insulating sidewall*” (first configuration). Therefore, in Guha’s Figure 12 device, the end of dielectric layer 15 (“*gate insulating film*”) “*protrudes from a side end of the gate electrode toward the insulating sidewall*” [7]. (TSMC-1003, ¶¶174-75.)



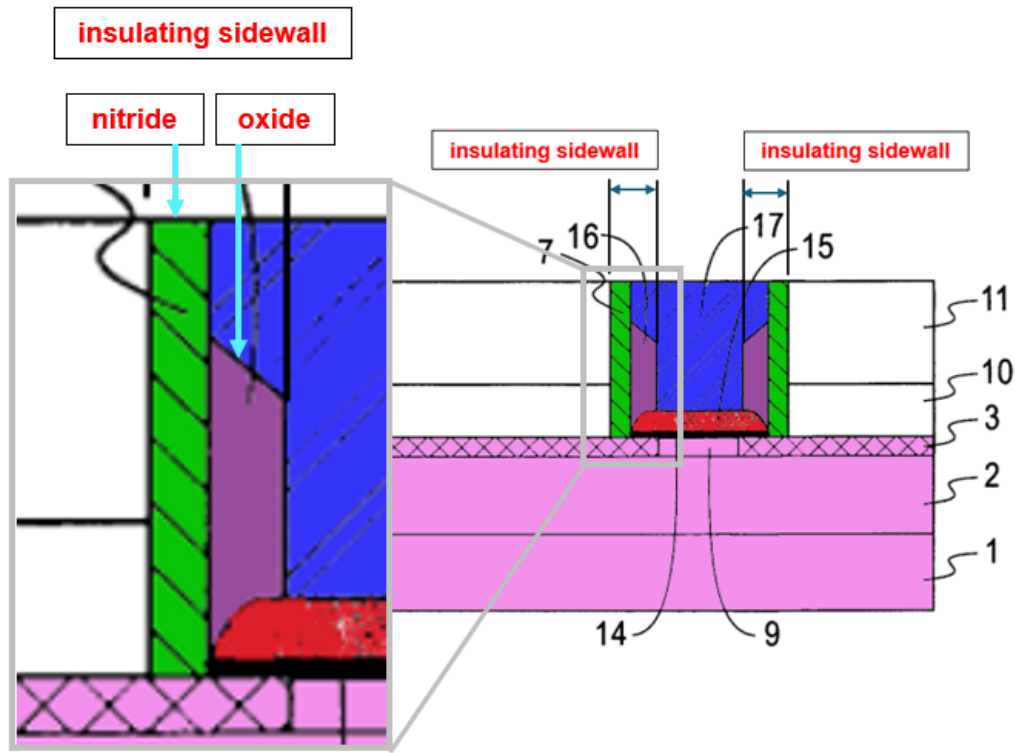
Guha, Figure 12 with enlargement

F. Claim 8

Guha discloses “the insulating sidewall has a double layer structure including an oxide film and a nitride film” [8], under the first “insulating sidewall” configuration (spacer 16 and spacer 7). (TSMC-1003, ¶¶176-79.)

Gate spacer 16 is a “material, e.g. an **oxide** or other suitable material” and is thus “an oxide film.” (TSMC-1028, ¶40; TSMC-1003, ¶177.) Isolating spacer structure 7 “can be composed of any insulating material including, for example, an oxide, **nitride**, oxynitride or any combination thereof” with “**silicon nitride**” as the “preferred material.” (TSMC-1028, ¶28.) A POSITA would have considered gate

spacer 16 and isolating spacer 7 to each be a “layer” of the collective sidewall, consistent with the ’076 patent’s disclosure. (*E.g.*, TSMC-1028, ¶¶28 (formation of spacers 7), 44 (formation of spacers 16); §VIII.B.4; TSMC-1001, 21:6-15; TSMC-1003, ¶179.)



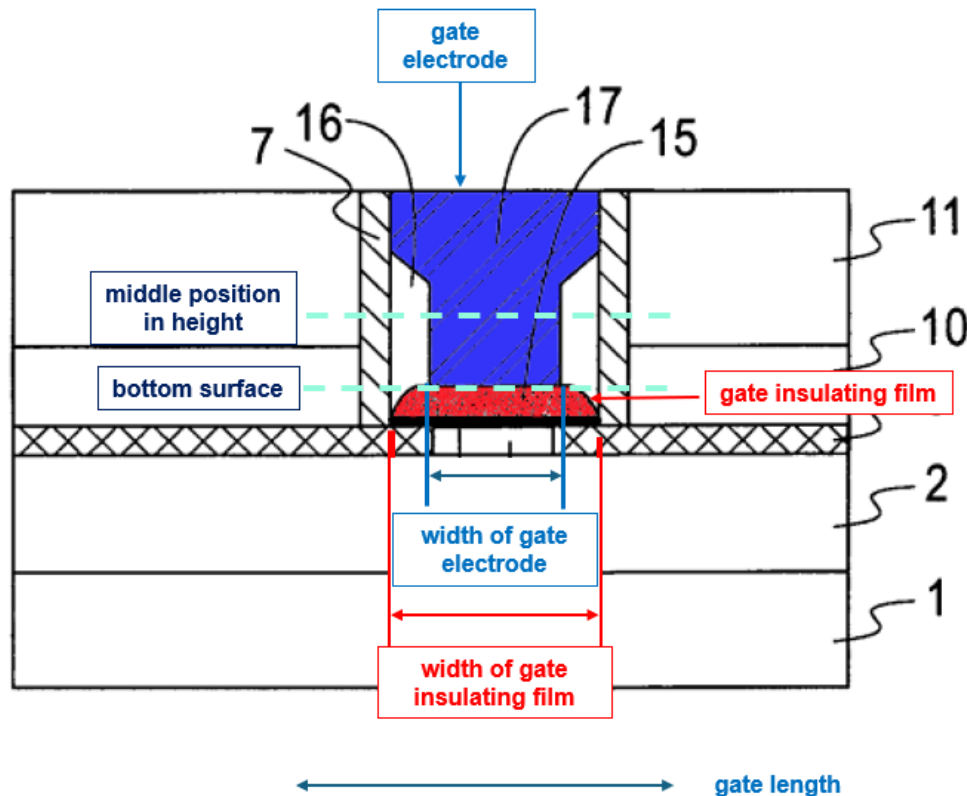
Guha, Figure 12

G. Claims 10 and 13

Guha discloses “a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length” [10] and “the width of the gate insulating film along a gate length

is larger than a width of part of the gate electrode in a middle position in height along the gate length” [13]. (TSMC-1003, ¶¶180-81.)

As shown in Figure 12 below, the width of the bottom surface of dielectric layer 15 (shaded red) is larger than the width of the bottom portion of the gate electrode (shaded blue). (TSMC-1003, ¶1801.) The width of the gate electrode is the same at its middle position as at its bottom. Therefore, the width of the dielectric layer 15 is also larger than the width of the gate electrode at its middle. (TSMC-1003, ¶181; *Unified*, 2022 WL 500391, *17.)

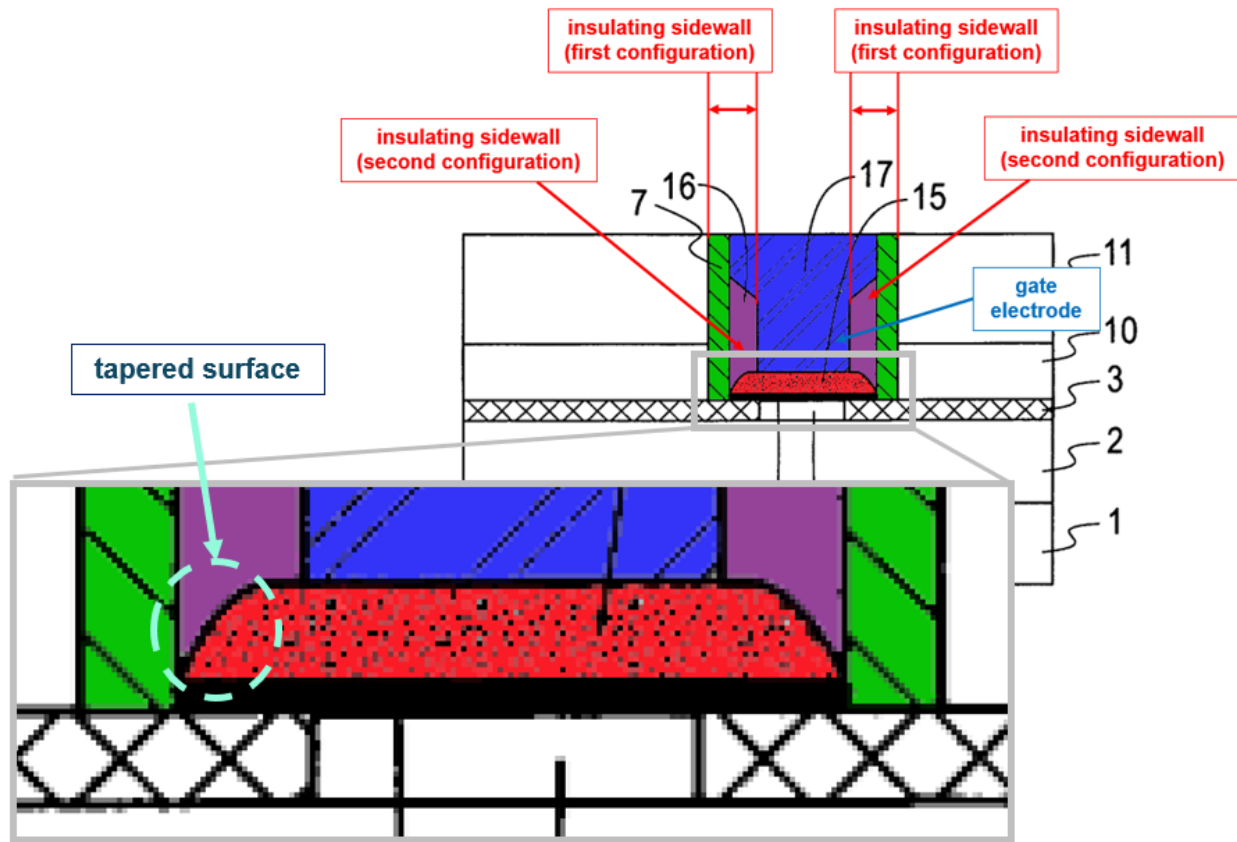


Guha, Figure 12

H. Claims 11-12

Guha discloses “*the end of the gate insulating film located under the insulating sidewall has a tapered surface*” [11] and “*the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof*” [12], under both the first and second “*insulating sidewall*” configurations. (TSMC-1003, ¶¶182-83.)

In Guha’s device, “the edge where the dielectric layer 15 meets the isolating spacer structure 7 ... is **rounded** either upwards or **downwards** (e.g., similar to a cusp).” (TSMC-1028, ¶43.) That is, the dielectric layer reduces in thickness at its end such that its smallest thickness is under spacer 16—i.e., it tapers. (TSMC-1003, ¶183; *see* TSMC-1028, ¶44 (spacer 16 is formed after and on dielectric layer 15).) Accordingly, the tapered end portion of dielectric layer 15 is “*located under the insulating sidewall*” in the first configuration (**spacers 16** and spacers 7) and second configuration (**spacers 16**). (TSMC-1003, ¶183.)



Guha, Figure 12

IX. GROUND 5: Guha-Koyama Combination Renders Claim 4 Obvious.

Guha describes use of “**hafnium silicate**,” as a high-k gate dielectric but does not expressly disclose use of “*a HfSiON film*” [4]. (TSMC-1028, ¶38.)

Koyama discloses this teaching, as discussed in §VI.

A POSITA would have been motivated to combine Koyama’s teachings regarding use of HfSiON as a high-k gate dielectric with Guha’s Figure 12 device. (TSMC-1003, ¶¶184-85.) Koyama and Guha are in the same field as the ’076 patent, “a semiconductor device and a method for fabricating the semiconductor

device.” (TSMC-1001, 1:18-19; TSMC-1028, ¶1; TSMC-1029, Abstract; TSMC-1003, ¶184.) Accordingly, the Guha-Koyama device discloses “*the gate insulating film is formed of a HfSiON film*” [4]. (TSMC-1003, ¶¶184-86.)

Guha motivates the combination indicating high-k dielectric materials are not “limited to” the materials on its list. (TSMC-1028, ¶38.) A POSITA would have been motivated to investigate other hafnium silicate options and would have been led to Koyama. (TSMC-1003, ¶185.) A POSITA would have further been motivated to make the above combination to achieve the enhanced benefits of HfSiON high-k film, e.g., improved thermal stability and electrical characteristics, described by Koyama and discussed in §VI. (*Id.*)

Moreover, the combination is nothing more than use of a known technique (Koyama’s use of HfSiON as a gate insulating film) to improve similar devices in the same way. *KSR*, 550 U.S. at 416-417; TSMC-1003, ¶186. A POSITA would have had a reasonable expectation of success and the combination would have yielded predictable results for the reasons discussed in §VI. (TSMC-1003, ¶186.)

X. GROUND 6: Guha-Sim Combination Renders Claim 6 Obvious.

Guha does not expressly disclose “*a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less*” [6]. Sim discloses this teaching, as discussed in §VII. Accordingly, the Guha-Sim combination discloses claim 6. (TSMC-1003, ¶¶187-91.) Sim and Guha are in the same field as

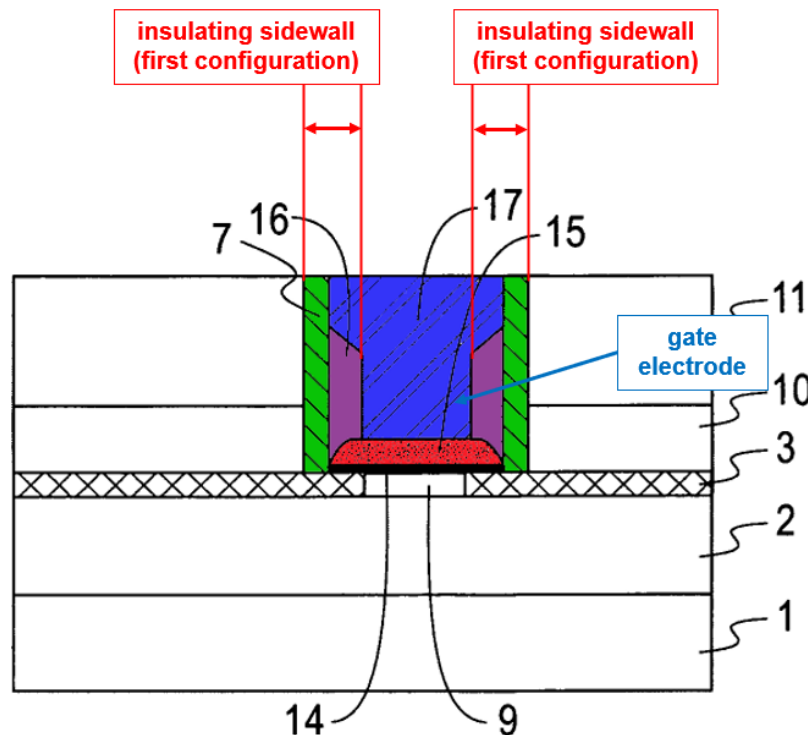
the '076 patent, “a semiconductor device and a method for fabricating the semiconductor device.” (TSMC-1001, 1:18-19; TSMC-1028, ¶1; TSMC-1024, Abstract; TSMC-1003, ¶187.)

A POSITA would have been motivated to adopt Sim’s solution of forming a gate insulating film with a thickness of 20Å (2 nm) or less in Guha’s Figure 12 device. Sim discloses reducing the thickness of HfO₂ to below 20Å enhances mobility and reduces charge trapping, which ensures the performance and scalability of semiconductor devices. (TSMC-1024, 219, 221; §VII.) Such improvements align with the continued miniaturization of devices, which both Guha and Sim emphasize is crucial to advancing CMOS technology. (TSMC-1028, ¶2; TSMC-1024, 218; TSMC-1003, ¶190.)

Additionally, the combination is nothing more than use of a known technique (Sim’s HfO₂ dielectric layer with less than 20Å thickness) to improve similar devices in the same way. *KSR*, 550 U.S. at 416-417; TSMC-1003, ¶191.) A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable because Sim uses a well-known process, atomic layer deposition (ALD), for fabricating high-k films. (TSMC-1024, 218; TSMC-1032, 17-19; TSMC-1003, ¶191.)

XI. GROUND 7: Guha-Ahmed Combination Renders Claim 9 Obvious.

Guha’s device includes gate spacer 16 and isolating spacer 7 (“*insulating sidewall*” in the first configuration). (§VIII.B.4; Figure 12 (below).) However, Guha does not expressly disclose “*the insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film*” [9]. This feature is taught by the Guha-Ahmed combination.

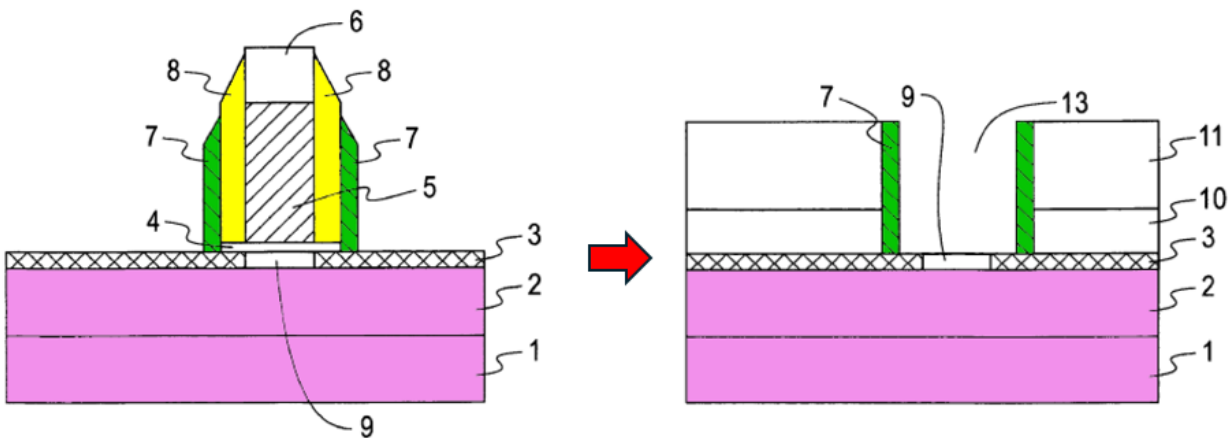


Guha, Figure 12

A. Formation of Guha's Spacers

During Guha’s fabrication, dummy spacers 8 (shaded yellow) are formed “adjacent to the dummy gate 5, extending from the pad protection layer 4 up to the dummy gate hard mask 6.” (TSMC-1028, ¶27, Figure 3 (below-left).) Pad layer 4

is “an oxide.” (TSMC-1028, ¶24.) Isolating spacer 7 (shaded green) is then “formed flanking the dummy-gate spacers 8.”¹³ (TSMC-1028, ¶28.) After formation of the source/drain contacts 10, “dummy gate 5 is removed by etching,” and “dummy gate spacer 8 is removed, e.g. using dilute HF, which also removes the pad protection layer 4,” leaving behind the structure of Figure 6 (below-right). (TSMC-1028, ¶¶33-34.) Gate-isolating layer 14, high-k dielectric layer 15, and gate spacers 16 are then formed as discussed in §§VIII.B.2, VIII.B.4. (TSMC-1028, ¶¶37-38, 43-44.)

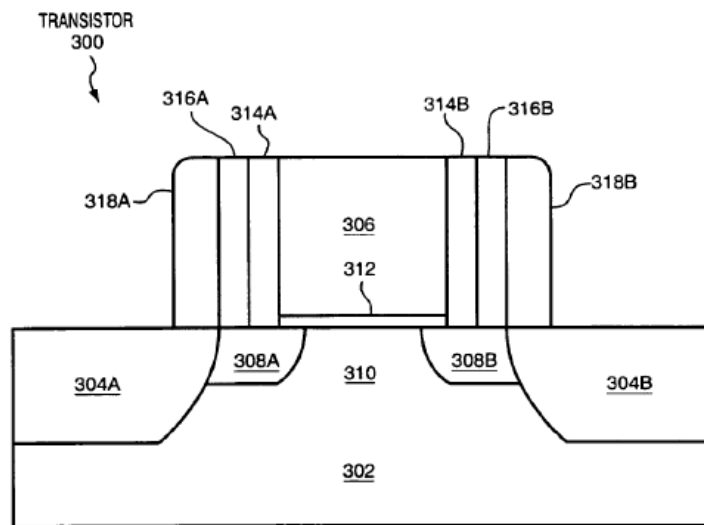


Guha, Figures 3 (left), 6 (right)

¹³ Pad protection layer 4 is partially etched before formation of isolation spacer structures 7 to arrive at the length depicted in Guha’s Figure 3. (Guha, Figures 2-3; TSMC-1003, ¶200 n.11.)

B. Ahmed

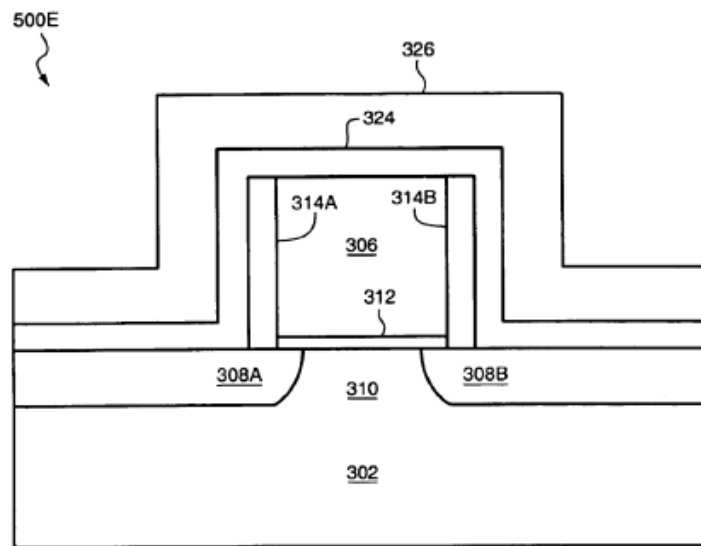
Ahmed's Figure 3 transistor includes a triple layer sidewall: (1) insulating spacers 314A/B "adjacent and ... abutting sidewalls of the gate ... to offset the extension regions from the gate," (2) source/drain spacers 318A/B "to offset the source/drain terminals from the gate," and (3) source/drain spacer liners 316A/B "disposed between and separating the source/drain spacers 318A/B and the insulating spacers 314A/B." (TSMC-1031, 4:9-17.) In an exemplary embodiment, spacer 314A/B is an oxide (TSMC-1031, 9:39-57, 10:55-60), spacer 316A/B is an oxide (TSMC-1031, 12:59-13:6), and spacer 318A/B is a nitride (TSMC-1031, 13:35-51, 13:61-66).



Ahmed, Figure 3

Ahmed discloses that using a middle layer, spacer 316, provides multiple benefits, including "serv[ing] as an etch stop for a subsequent etch to form the

source/drain spacers and thereby help protect the underlying materials.” (TSMC-1031, 12:53-58.) This is shown in Figure 3 (above) as well as Figure 5E (below), where layer 324 (which is etched to form spacer 316 (TSMC-1031, 13:61-66)) provides coverage for the underlying materials, including source/drain regions 308A/B.¹⁴ (TSMC-1003, ¶196.)

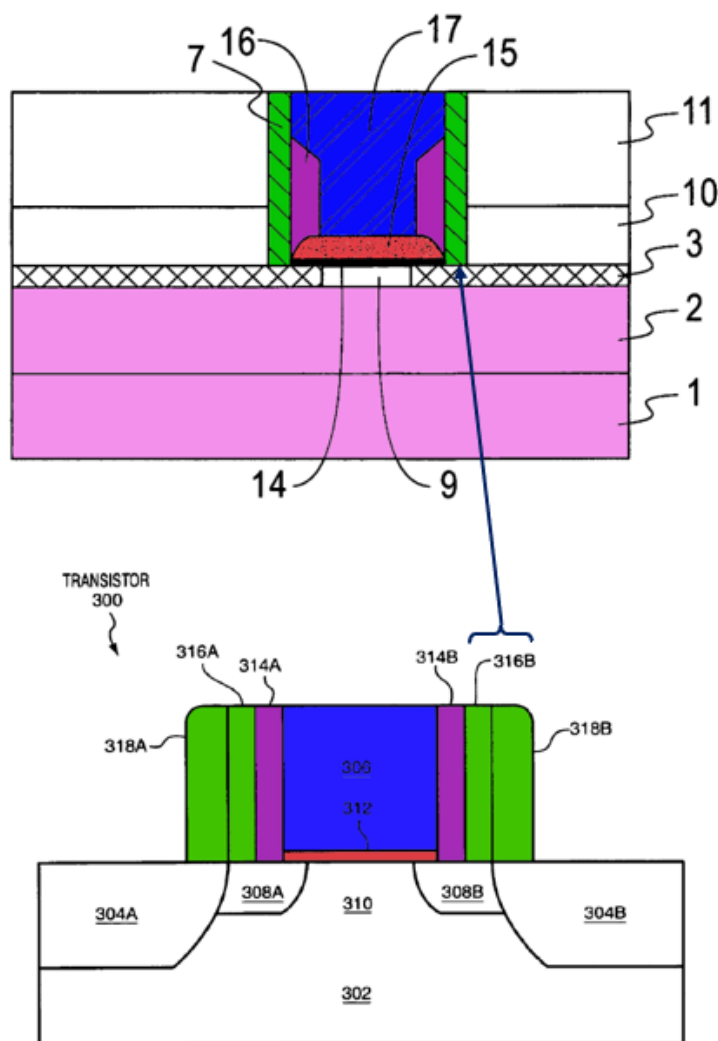


Ahmed, Figure 5E

¹⁴ Based on the deposition of layers depicted in Figure 5E before formation of spacers 316 and 318, a POSITA would have understood spacer 316 to be formed in an L-shape, though it is not depicted as such in Ahmed’s Figure 3. (TSMC-1003, ¶196 n.10.)

C. Combination Overview

A POSITA would have been motivated to apply Ahmed’s teachings of a triple layer sidewall structure, including an intermediate oxide layer between outer oxide and nitride layers, to Guha’s insulating sidewall structure comprising spacers 16 and 7, as shown below. (TSMC-1003, ¶197.) Specifically, a POSITA would have been motivated to replace Guha’s spacer 7 with spacers 316 (oxide) and 318 (nitride) before forming spacer 16. (*Id.*) Ahmed and Guha are in the same field as the ’076 patent, “a semiconductor device and a method for fabricating the semiconductor device.” (TSMC-1001, 1:18-19; TSMC-1028, ¶1; TSMC-1031, Abstract; TSMC-1003, ¶194.) Accordingly, Guha’s sidewall structure as modified by Ahmed comprises an oxide layer (Guha’s spacer 16), an oxide layer (Ahmed’s spacer 316), and a nitride layer (Ahmed’s spacer 318), resulting in an “*insulating sidewall*” with “*a triple layer structure including a first oxide film, a nitride film and a second oxide film.*” (*Id.*)



Guha, Figure 12 (top); Ahmed, Figure 3 (bottom)

In forming the combined structure, a POSITA would have been motivated to form Guha's isolating spacer 7 as a first oxide layer, equivalent to Ahmed's spacer 316, on the side surface of Guha's dummy spacer 8 and a second nitride layer, equivalent to Ahmed's spacer 318, on the side surface of the first oxide layer. (TSMC-1003, ¶203.) The process steps of Guha then proceed in the same way described above. (*Id.*)

Guha and Ahmed both explicitly motivate the combination. (TSMC-1003, ¶¶198-203.) Guha discloses isolating spacer 7 can include two materials: spacer 7 “can be composed of any insulating material including, for example, an oxide, nitride, oxynitride **or any combination thereof.**” (TSMC-1028, ¶28.) A POSITA would have known forming two discrete layers, as taught by Ahmed’s oxide spacer 316 and nitride spacer 318, best utilizes the distinct properties of two materials. (TSMC-1003, ¶199.) Thus, Guha suggests using discrete layers for spacer 7’s multiple materials. (*Id.*)

Guha further explains isolating spacer 7 is resistant to the etchant used to remove dummy-gate spacer 8, e.g., HF, so as “to protect the source/drain contacts 10 from the etchant used to remove the dummy gate spacer 8.” (TSMC-1028, ¶34.) Ahmed expressly furthers Guha’s goal. By first providing oxide spacer 316 before the outer nitride spacer (Guha’s spacer 7/Ahmed’s spacer 318), spacer 316 ensures protection of the source/drain contacts, as taught by Guha, by (1) serving as an additional layer to protect the source/drain contacts and (2) protecting the outer nitride spacer from the etchant when dummy-gate spacer 8 is removed,¹⁵ further

¹⁵ A POSITA would understand that, in the Guha-Ahmed device, the materials used to form spacer 316 (from Ahmed) and dummy-gate spacer 8 (from

ensuring the nitride layer protects the source/drain contacts during Guha's process. (TSMC-1031, 12:48-58, Figure 5E; §XI.B; TSMC-1003, ¶201.) Providing L-shaped oxide spacer 316 also can isolate Guha's outer nitride spacer 7 from the silicon substrate, thereby (a) avoiding known stresses arising at $\text{Si}_3\text{N}_4/\text{Si}$ interfaces that could induce device degradation (TSMC-1003, ¶201; TSMC-1050, ¶6) and (b) serving as an etch stop to protect Guha's underlying source/drain extensions 3a/3b when etching a deposited nitride layer to form the isolating nitride spacer 7 (TSMC-1003, ¶201; TSMC-1028, ¶28; TSMC-1031, 12:53-58.).

Ahmed also discloses spacer 316 provides additional benefits, including, to "improve adhesiveness between the source/drain spacers and the insulating spacers" and to "protect and seal the gate or gate dielectric." (TSMC-1031, 12:53-58.) In light of these known benefits and Guha's suggestion of using multiple materials for spacer 7, a POSITA would have been motivated to form Ahmed's spacers 316 and 318 in place of Guha's isolating spacer 7. (TSMC-1003, ¶202.)

Guha) must be different, so spacer 316 is not removed when dummy gate spacer 8 is removed, and a POSITA would have understood how to select such materials. (TSMC-1003, ¶201 n.12.)

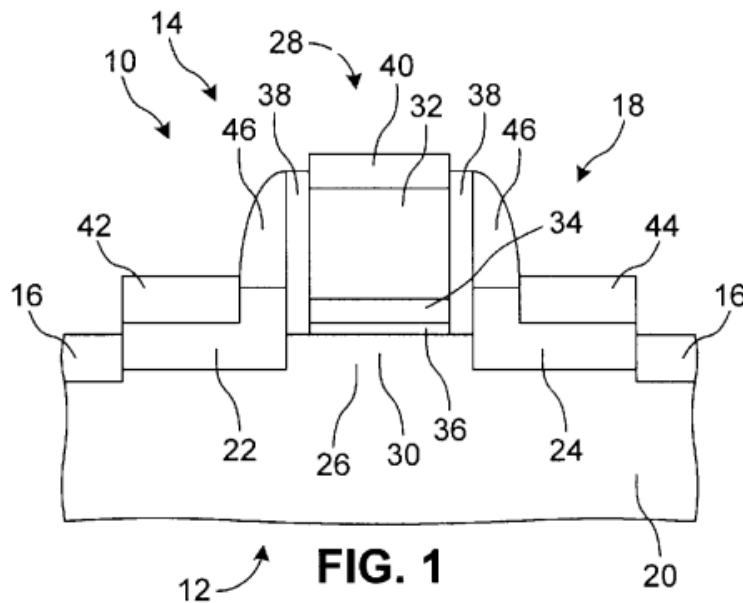
XII. GROUND 8: Matsumoto-Yu Combination Renders Claims 1-3, 7-10, 13 Obvious.

1. Matsumoto

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2. Yu

Yu's MOSFET device includes buffer interface 36 between semiconductor substrate 20 and high-k gate dielectric 34. (TSMC-1048, 3:59-62; Figure 1 (below).) Yu's gate dielectric 34 "is made from a high-K material"; examples of such high-k materials include "hafnium oxide (e.g., HfO_2), zirconium oxide (e.g., ZrO_2), cerium oxide (e.g., CeO_2), aluminum oxide (e.g., Al_2O_3), titanium oxide (e.g., TiO_2), yttrium oxide (e.g., Y_2O_3) and barium strontium titanate (BST)" (TSMC-1048, 3:15-30.) Buffer interface 36 "can be a thin layer of oxide," e.g., "a layer of silicon oxide that is about 0.5 nm to about 0.7 nm thick." (TSMC-1048, 4:58-61; *see also* TSMC-1048, 3:62-63.)



Yu, Figure 1

3. Motivation to Combine

A POSITA would have been motivated to make the following two combinations of the teachings of Yu with Matsumoto. Yu and Matsumoto are in the same field as the '076 patent, “a semiconductor device and a method for fabricating the semiconductor device.” (TSMC-1001, 1:18-19; TSMC-1009, ¶2; TSMC-1048, Abstract; TSMC-1003, ¶211.)

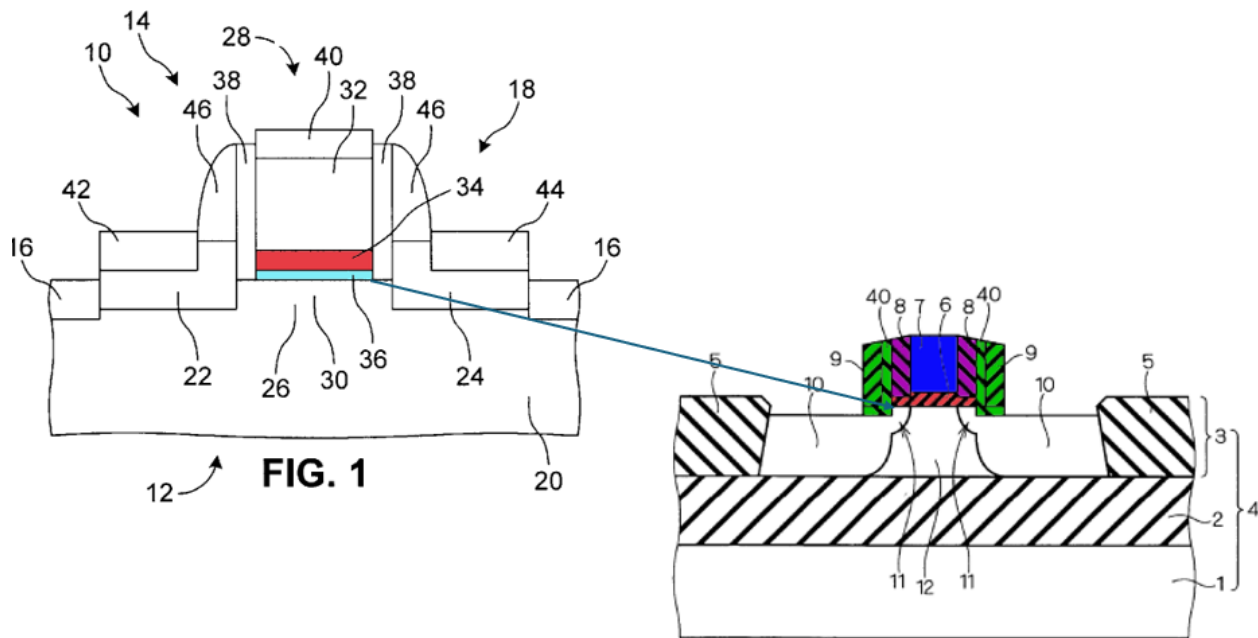
a. First Combination

A POSITA would have been motivated to select a Hf-based oxide as the gate insulating film in Matsumoto's fourth embodiment device, as taught by Yu. (TSMC-1003, ¶212.)

Matsumoto discloses a list of exemplary films, including “a metal oxide film **such as** Al_2O_3 or a ferroelectric film such as Ta_2O_5 and BST,” to use as its gate insulating film. (TSMC-1009, ¶107.) A POSITA would have understood these films to be high-k dielectrics. (E.g., TSMC-1018, Table 1; TSMC-1038, 88-89.) In addition to “aluminum oxide (e.g., Al_2O_3)” and “barium strontium titanate (BST)” as identified in Matsumoto, Yu discloses a gate dielectric 34 comprising “hafnium oxide (e.g., HfO_2),” which is also a high-k film. (TSMC-1048, 3:15-30; *see also* TSMC-1018, Table 1.) By 2005, a POSITA would have been motivated to select HfO_2 given its known benefits, discussed in §V.B.2. (TSMC-1037, 2.4.1; TSMC-1032, 207; TSMC-1049, 134; TSMC-1003, ¶¶213-14.)

b. Second Combination

A POSITA would have also been motivated to apply Yu's teaching of a buffer interface layer between a high-k gate dielectric and a substrate with Matsumoto's fourth embodiment device. (TSMC-1003, ¶215.) For example, a POSITA would have been motivated to integrate Yu's buffer interface 36 (shaded aqua) between the substrate and Matsumoto's high-k dielectric (shaded red) in the combined device, as illustrated below. (TSMC-1003, ¶216.)



Yu, Figure 1 (left); Matsumoto, Figure 22 (right)

Yu motivates the combination, teaching buffer interface (a) “acts to reduce diffusion and/or penetration of atoms from the high-K dielectric material into the layer of semiconductor material 20 that could lead to a degradation in channel mobility” and (b) “retard[s] reaction of the high-K material with the layer of

semiconductor material 20.” (TSMC-1048, 3:64-4:2; *see also* TSMC-1048, 4:65-67 (“buffer interface material layer 62 assists in reducing integration issues that may arise when attempting form a layer of high-K material on a semiconductor layer.”); TSMC-1003, ¶217.) Based on these explicit disclosures, a POSITA would have been motivated to use Yu’s buffer interface to improve channel mobility and performance of the combined device. (TSMC-1003, ¶¶217-18; TSMC-1009, ¶13 (describing objective of Matsumoto to reduce malfunctions and operating characteristic variations).)

Moreover, the combination is nothing more than use of a known technique (Yu’s buffer interface) to improve similar devices in the same way for the above reasons. *KSR*, 550 U.S. at 416-417; TSMC-1003, ¶¶219-20. A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable because Yu discloses instructions on conventional techniques to create buffer layers between the high-k gate dielectric film and substrate. (TSMC-1048, 4:61-65; TSMC-1003, ¶¶219-20.)

B. Independent Claim 1

1. Preamble [1P]

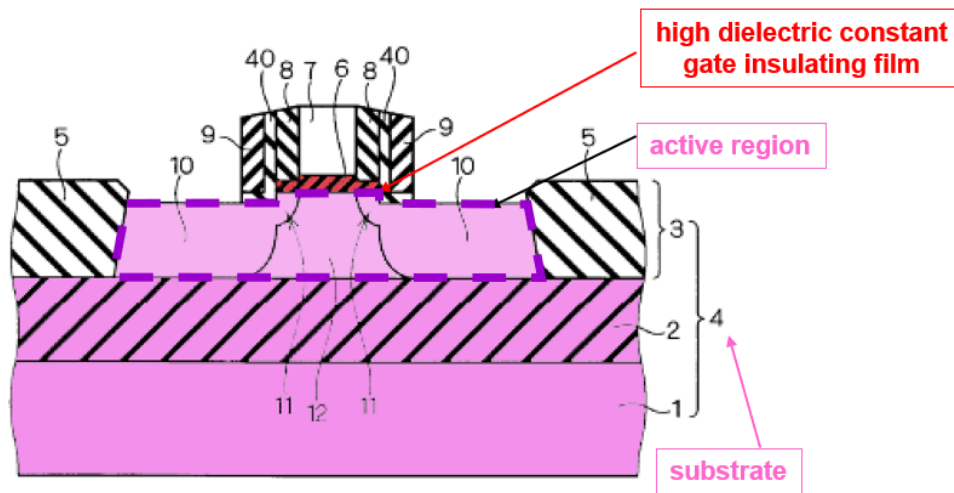
The Matsumoto-Yu combination discloses a “*semiconductor device*”:
“present invention relates to **a semiconductor device.**” (TSMC-1009, ¶¶2, 137; *see also* TSMC-1048, 1:7-11.)

2. Limitation [1A]

The Matsumoto-Yu combination discloses “*a gate insulating film formed on an active region in a substrate and including Hf*” [1A]. (TSMC-1003, ¶¶222-27.)

Matsumoto’s fourth embodiment device includes “*a substrate.*” (TSMC-1003, ¶223.) The device has a multi-layer SOI **substrate** 4 (shaded pink) with silicon substrate 1, BOX layer 2 and single-crystalline silicon layer 3. (TSMC-1009, ¶102, ¶¶137, 140 (relating fourth embodiment to first embodiment), Figure 22 (below)); *Google*, 2022 WL 4287797, *9 n.9 (applying same disclosure where “figures refer to corresponding features using the same reference numbers”).¹⁶)

¹⁶ Although Matsumoto discloses several embodiments, many of the fabrication steps are discussed in relation to the first embodiment. (TSMC-1003, ¶206 n.13; Matsumoto, ¶137.) Thus, Petitioner at times relies on disclosures from Matsumoto’s first embodiment when discussing the fourth embodiment.



Matsumoto, Figure 22

Isolating insulation film structures 5, “extend[ing] from the upper surface of the silicon layer 3 to the upper surface of the BOX layer 2,” define a “**device region.**” (TSMC-1009, ¶¶102-103, ¶¶137, 140.) The device region, identified by isolation regions, is an “*active region in a substrate*” and includes source/drain regions 10. (TSMC-1009, ¶139; TSMC-1003, ¶224; *see* TSMC-1001, 1:41-42 (“region of the well 102 surrounded by the STI serves as an active region of a substrate 101”), 7:28-45.)

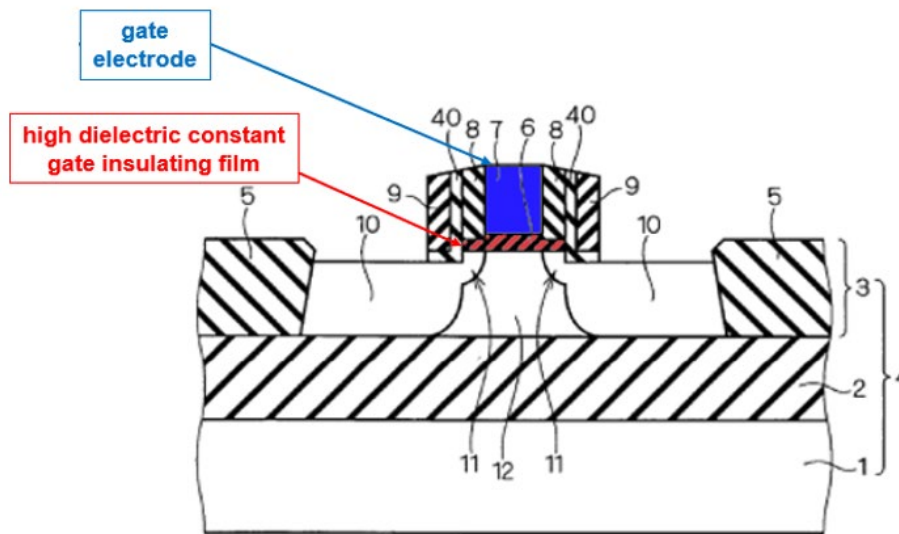
Film 6 (shaded red) “is formed partially on the upper surface of the silicon layer 3” in the device region with gate electrode 7 “formed partially” thereon. (TSMC-1009, ¶¶103 (first embodiment), 137 (fourth embodiment “gate electrode 7 is formed by the process described in the first embodiment”).) Film 6 is therefore a “*gate insulating film formed on an active region in a substrate*” [1A]. (TSMC-

1003, ¶¶225-26; *see* TSMC-1009, ¶103 (referring to film 6 as a “gate insulation film”).)

The Matsumoto-Yu combination uses HfO₂ as the gate insulting film 6 in Matsumoto’s device, as taught by Yu. (§XII.A.3.a; *see also* TSMC-1009, ¶107 (film 6 is a high-k film); TSMC-1048, 3:15-30.) Accordingly, the Matsumoto-Yu combination discloses “*a gate insulating film ... including Hf*” [1A]. (TSMC-1003, ¶227.)

3. Limitation [1B]

The Matsumoto-Yu combination discloses “*a gate electrode formed on the gate insulating film*” [1B]. (TSMC-1003, ¶¶228-29.) In Matsumoto’s device, “**gate electrode 7** [shaded blue] made of polysilicon **is formed partially**” on film 6, which in the combination is HfO₂. (TSMC-1009, ¶¶103, 107 (describing formation of film 6 and gate electrode 7), 137-138, Figure 22 (below).)



Matsumoto, Figure 22

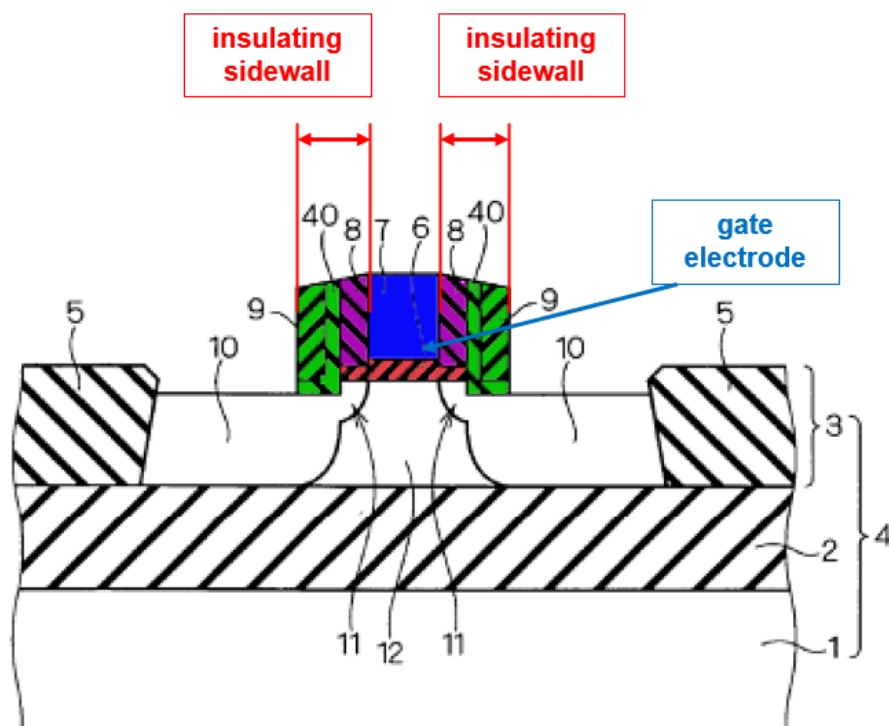
4. Limitation [1C]

The Matsumoto-Yu combination discloses “a insulating sidewall formed on each side surface of the gate electrode” [1C]. (TSMC-1003, ¶¶230-33.)

In Matsumoto’s device, silicon oxide film 40 and silicon nitride film 9 are formed “on the outer side surfaces of” silicon oxide film 8. (TSMC-1009, ¶139, Figure 22 (below).) Matsumoto refers to film 9 as a “sidewall insulation film” but does not expressly refer to films 40 or 8 as a “sidewall.” (TSMC-1009, ¶114 (describing nitride films 9a/9b “serving as **sidewall** insulation films”).) A POSITA would have understood films 40 and 8 also to be sidewalls. (TSMC-1009, ¶¶104, 110, 138 (“This forms the silicon oxide films 8 on the side surfaces of the gate electrode 7.”), 139 (“This forms silicon oxide films 40 and the silicon nitride films

9 on the outer side surfaces of the silicon oxide films 8.”), 40 (“the semiconductor device further includes a second sidewall formed on the side surface of the gate electrode, with the first sidewall therebetween”); TSMC-1003, ¶233.)

Because silicon oxide and silicon nitride are both insulators, film 8, film 40, and film 9 are collectively “*a insulating sidewall formed on each side surface of the gate electrode*” [1C]. (TSMC-1009, ¶¶110 (describing formation of silicon oxide films 8a/8b on the side surfaces of the gate electrodes), 114; TSMC-1009, claim 1 (referring to “insulation films” formed on side surfaces of gate electrode); TSMC-1001, 2:60-65 (referring to multiple components collectively as an “insulating sidewall”); TSMC-1003, ¶233.) Alternatively, film 8 alone is the claimed “*insulating sidewall*.” (TSMC-1003, ¶233; TSMC-1001, 6:9.)

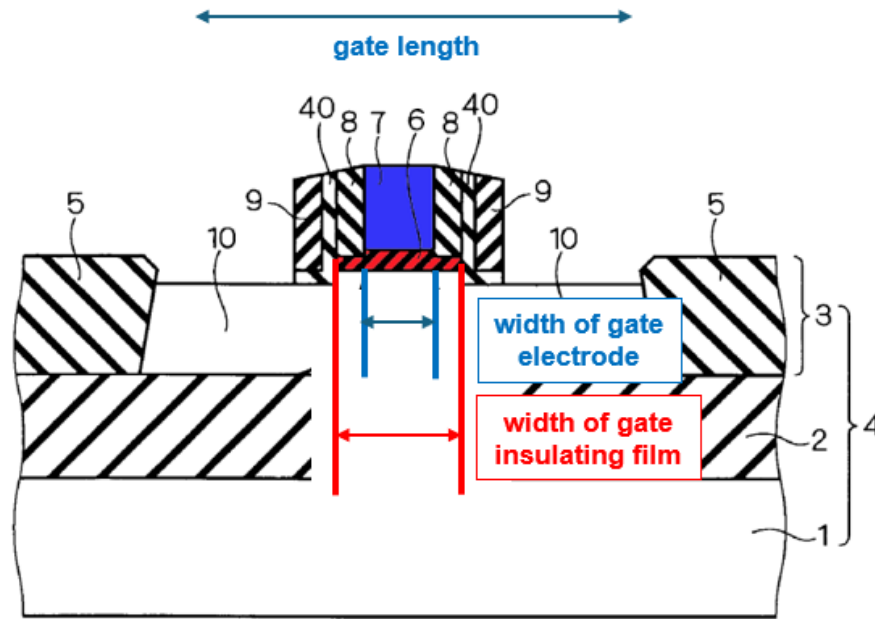


Matsumoto, Figure 22

5. Limitation [1D]

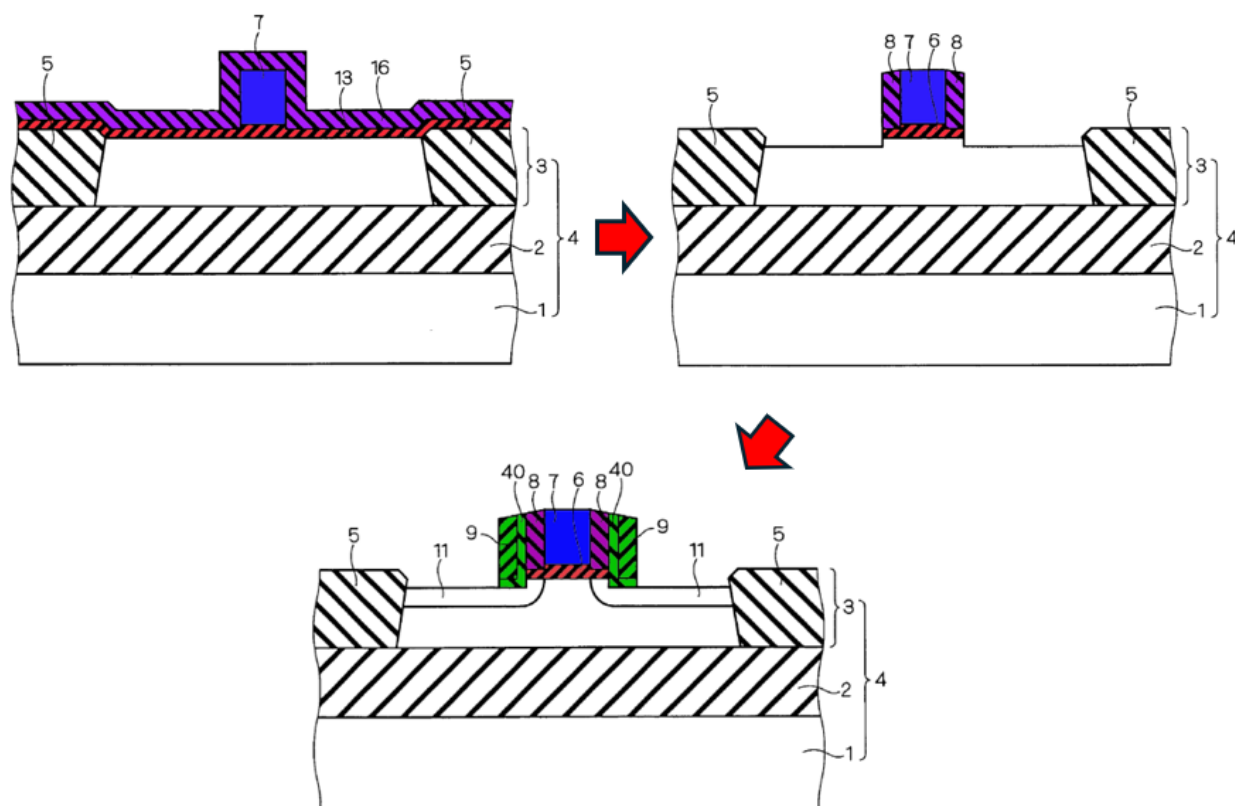
The Matsumoto-Yu combination discloses “*a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length*” [1D]. (TSMC-1003, ¶¶234-38.)

As illustrated in Matsumoto’s Figure 22 below, the width of gate insulating film 6 (shaded red) along the gate length is larger than the width of gate electrode 7 (shaded blue). (TSMC-1003, ¶235; *Unified*, 2022 WL 500391, *17.)



Matsumoto, Figure 22

Matsumoto’s fabrication process confirms this arrangement of the gate electrode and gate insulating film. After formation of gate electrode 7, high-k dielectric film 13 extends beyond the gate electrode with a larger thickness under the gate electrode. (TSMC-1009, ¶¶137, 107-08, Figure 18 (top-left); TSMC-1003, ¶236.) The etching process forming sidewall 8 (shaded purple) “overetch[es] the upper surface of the silicon layer 3” thereby leaving high-k dielectric film (shaded red) under the gate electrode and film 8. (TSMC-1003, ¶237; TSMC-1009, ¶138, Figure 19 (top-right).) Film 40 and film 9 (shaded green) are then formed on the outer side surfaces of film 8 and in contact with the substrate. (TSMC-1009, ¶139; Figure 21 (bottom).)



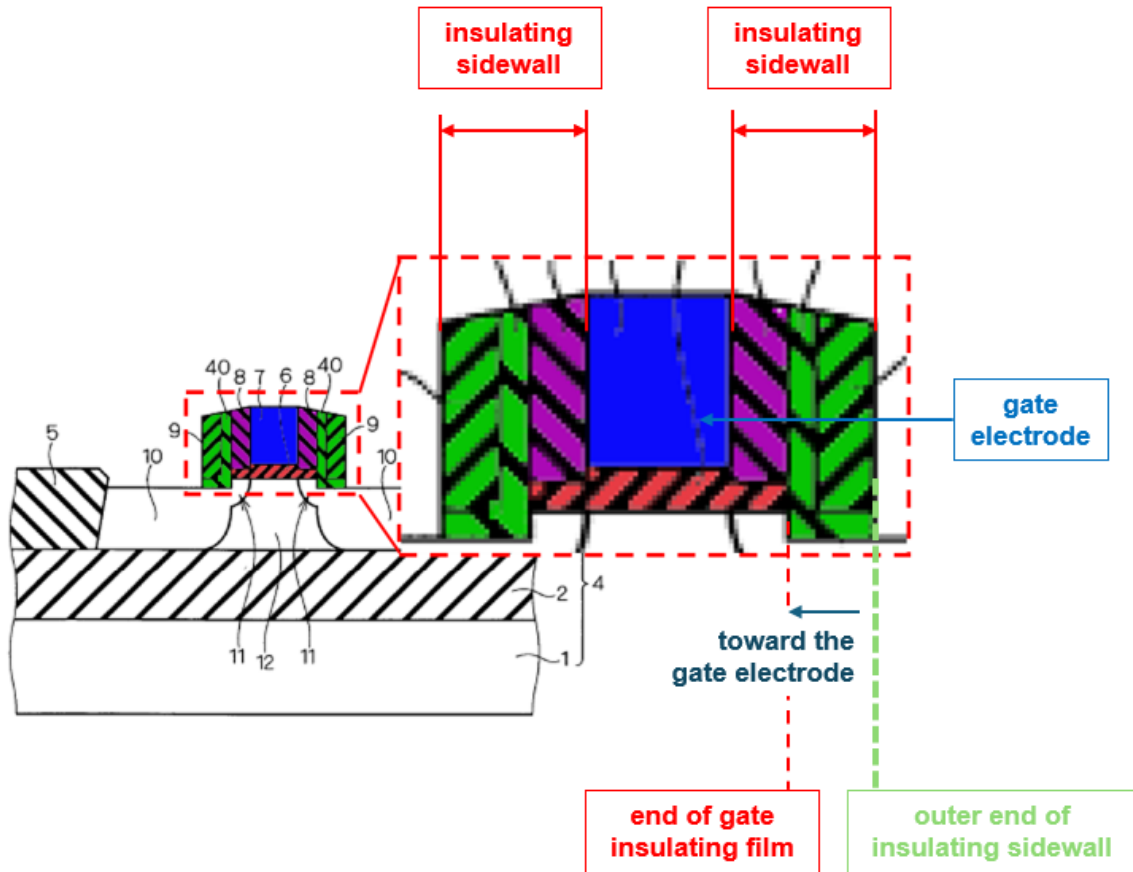
Matsumoto, Figures 18 (top-left), 19 (top-right), 21 (bottom)

6. Limitation [1E]

The Matsumoto-Yu combination includes “*an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode*” [1E]. (TSMC-1003, ¶¶239-40.)

Matsumoto’s gate insulating film 6 (shaded red) is an uninterrupted layer that extends from under the gate electrode to under only film 8, which is part of the collective “*insulating sidewall*” (collectively films 8, 40, 9). (§XII.B.2.) The end of high-k gate insulating film 6 is perpendicular to the substrate’s surface. As shown below, the end of gate insulating film 6 is disposed at a distance inward from the

“retracted from an outer end of the insulating sidewall toward the gate electrode”



Matsumoto, Figure 22 with enlargement

C. Claim 2

interface 36, which “can be a layer of **silicon oxide ...**,” between the high-k

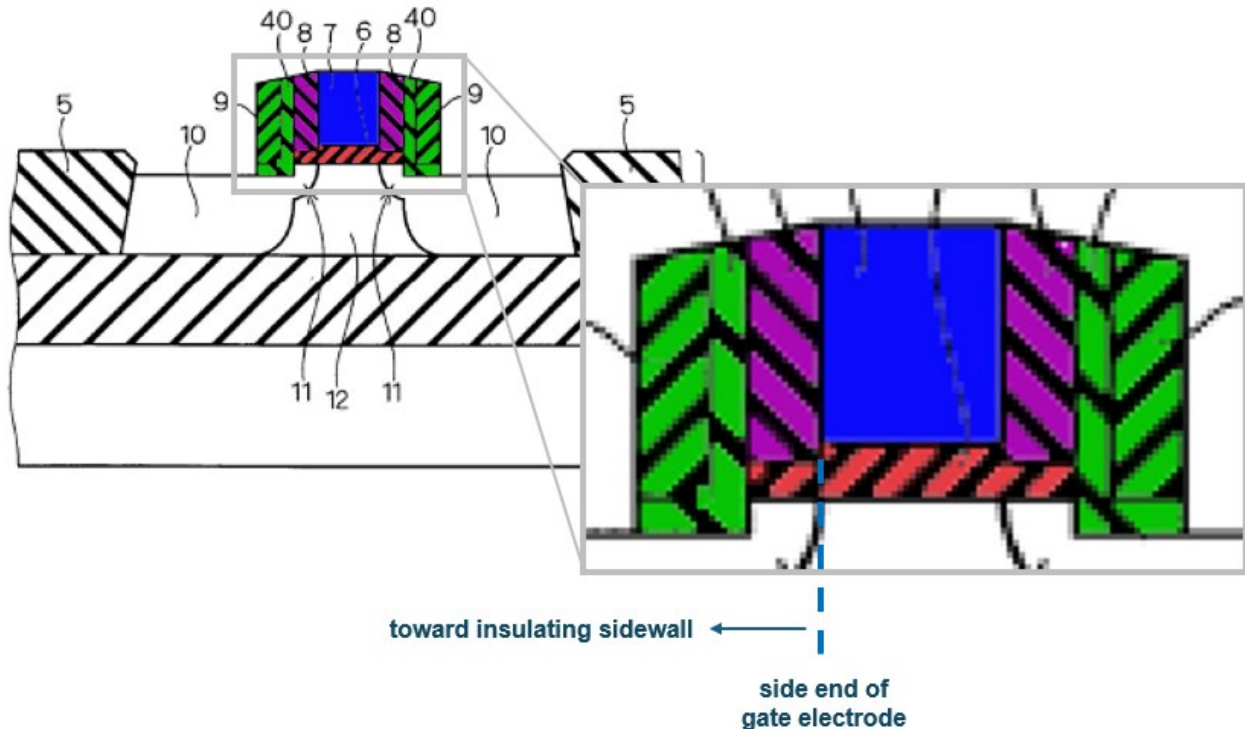
dielectric (“*gate insulating film*”) and the substrate. (TSMC-1048, 4:58-61, 3:62-63; TSMC-1003, ¶241.) The Matsumoto-Yu combination discloses “*a buffer insulating film [buffer interface 36] formed of a silicon oxide film and provided between the substrate and the gate insulating film [high-k dielectric]*” [2].

D. Claim 3

The Matsumoto-Yu combination discloses “*the gate insulating film is formed of a Hf based oxide*” [3]. (TSMC-1003, ¶242.) As discussed in §XII.B.2, the Matsumoto-Yu combination uses a Hf-based oxide as the gate insulating film in Matsumoto’s device, as taught by Yu. (TSMC-1048, 3:15-30 (identifying “hafnium oxide (e.g., HfO₂)” as example material for gate dielectric 34).)

E. Claim 7

The Matsumoto-Yu combination discloses “*an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall*” [7]. (TSMC-1003, ¶243.) As discussed in §XII.B.5, film 6 (shaded red) extends (protrudes) from under the gate electrode 7 to under sidewall 8 (part of the collective “*insulating sidewall*” comprising films 8, 40, and 9). (TSMC-1003, ¶243.)

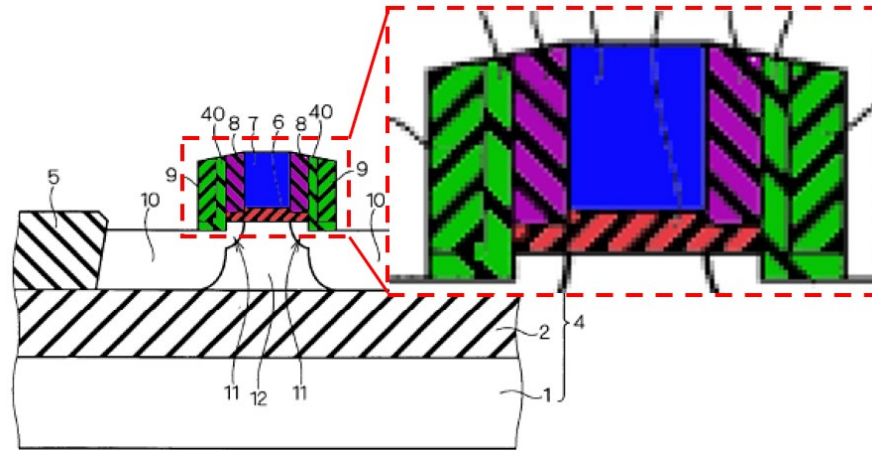


Matsumoto, Figure 22 with enlargement

F. Claims 8-9

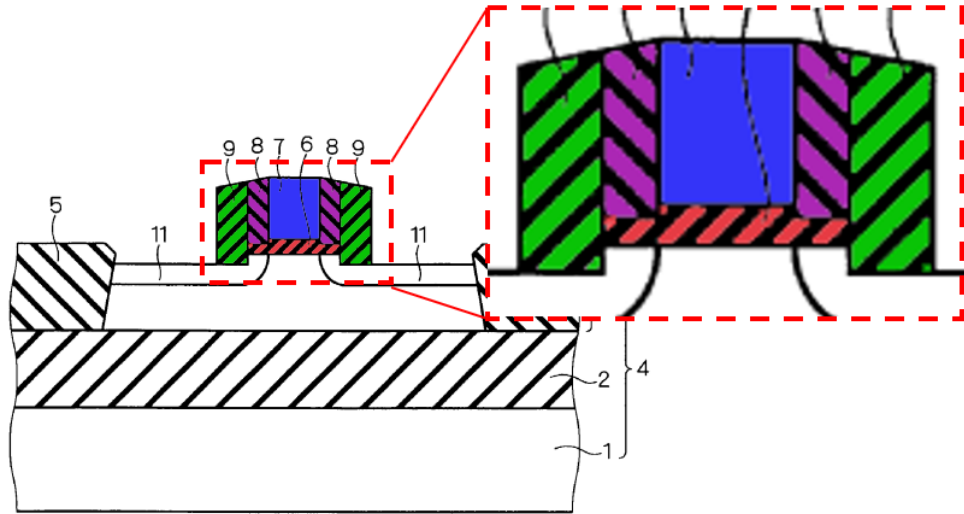
Matsumoto's device includes an "*insulating sidewall*" comprising film 8 (shaded purple) and films 40 and 9 (together shaded green). (§XII.B.4.) Films 8 and 40 are silicon oxide and film 9 is silicon nitride. (TSMC-1009, ¶139 ("This forms silicon oxide films 40 and the silicon nitride films 9 on the outer side surfaces of the silicon oxide films 8.")). A POSITA would have considered films 8, 40, and 9 to each be a "layer" of the collective sidewall, consistent with the '076 patent's disclosures. (TSMC-1003, ¶245; TSMC-1001, 21:6-15.) Matsumoto therefore discloses "*the insulating sidewall has a triple layer structure including a*

first oxide film [silicon oxide film 8], *a nitride film* [silicon nitride film 9] and a *second oxide film* [silicon oxide film 40]” [9]. (TSMC-1003, ¶245.)



Matsumoto, Figure 22 with enlargement

Matsumoto discloses a modification of the fourth embodiment that omits layer 40. In this modification, illustrated in Figure 23 below, “silicon nitride films 9 are formed directly on the upper surface of the silicon layer 3.” (TSMC-1009, ¶141.) Matsumoto motivates this modification stating it “is applicable to any one of the first to fourth preferred embodiments” and therefore the analysis of the fourth embodiment in §§XII.B.1-6 applies equally. *See Boston Sci.*, 554 F. 3d at 991. Thus, Matsumoto’s fourth embodiment modification meets each limitation of claim 1 and the combination further discloses “*the insulating sidewall* [collective structure of silicon oxide film 8 and silicon nitride film 9] *has a double layer structure including an oxide film and a nitride film*” [8]. (TSMC-1003, ¶¶246-47.)



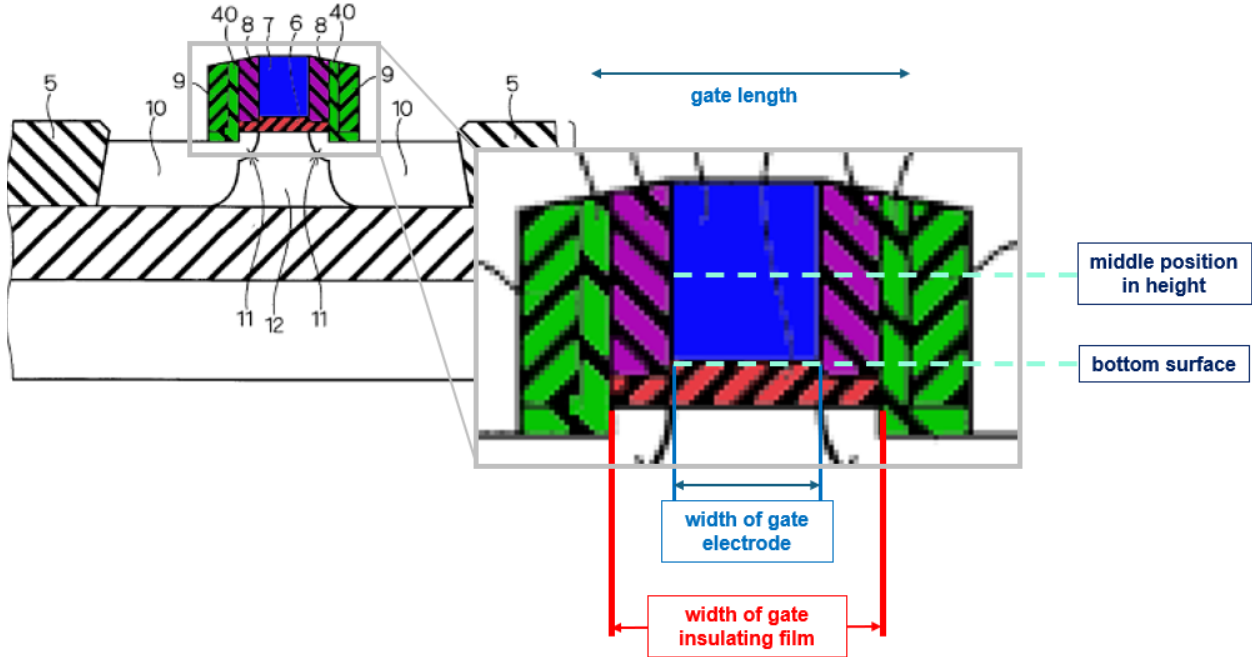
Matsumoto, Figure 23 with enlargement

G. Claims 10 and 13

The Matsumoto-Yu combination discloses “*a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length*” [10] and “*the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length*” [13]. (TSMC-1003, ¶¶248-50.)

As illustrated below, the width of Matsumoto's gate electrode 7 is constant across its entire height. Therefore, for the reasons discussed in §XII.B.5, the width of the gate insulating film 6 (shaded red), including at film 6's bottom surface, is larger than the width of gate electrode 7 (shaded blue) at both the bottom surface

*Unified, 2022 WL 500391, *17.)*



Matsumoto, Figure 22 with enlargement

XIII. GROUND 9: Matsumoto-Yu-Sim Combination Renders Claim 6 Obvious.

The Matsumoto-Yu combination discloses every limitation of claim 1 but does not explicitly disclose “*a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less*” [6]. As discussed in §VII, Sim discloses this teaching, such that the combined device of Matsumoto, Yu, and Sim renders claim 6 obvious. (TSMC-1003, ¶¶251-54.) Sim, Matsumoto, and Yu are in the same field as the ’076 patent, “a semiconductor device and a method for

fabricating the semiconductor device.” (TSMC-1001, 1:18-19; TSMC-1009, ¶2; TSMC-1024, Abstract; TSMC-1048, Abstract; TSMC-1003, ¶251.)

Although neither Matsumoto nor Yu specifically discloses a HfO₂ film that is less than 2 nm thick, a POSITA would have been motivated to use a thickness of 2 nm or less in the combined device, as taught by Sim. The resulting device of the combination includes a high-k gate dielectric having “*a thickness of 2 nm or less.*” (TSMC-1003, ¶252.)

A POSITA would have been motivated to make the above combination because Sim expressly motivates the combination, as discussed in §VII. (TSMC-1003, ¶253.) A POSITA would understand the improvements described by Sim align with Matsumoto’s goal of providing “a semiconductor device which achieves reductions in malfunctions and operating characteristic variations.” (TSMC-1009, ¶13.)

Additionally, the combination is nothing more than use of a known technique (Sim’s HfO₂ dielectric layer with less than 20Å thickness) to improve similar devices (combined device of Matsumoto and Yu with HfO₂ gate insulating film) in the same way (forming a high-k gate insulating film, with a smaller thickness) for the above reasons. *KSR*, 550 U.S. at 416-417; TSMC-1003, ¶254. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable because Sim uses a well-

known process (ALD) for fabricating high-k films. (TSMC-1024, 218; TSMC-1003, ¶254.)

XIV. GROUND 10: Matsumoto-Koyama Combination Renders Claims 1 and 4 Obvious.

As discussed in §XII.B, Matsumoto discloses each limitation of claim 1, but does not expressly disclose “*a gate insulating film ... including Hf*” [1A] or that “*the gate insulating film is formed of a HfSiON film*” [4]. (TSMC-1003, ¶255.) These limitations are disclosed by Koyama. Koyama and Matsumoto are in the same field as the ’076 patent, “a semiconductor device and a method for fabricating the semiconductor device.” (TSMC-1001, 1:18-19; TSMC-1009, ¶2; TSMC-1024, Abstract; TSMC-1029, Title; TSMC-1003, ¶255.)

A. Motivation to Combine

A POSITA would have been motivated to combine Koyama’s use of HfSiON as a gate insulating film with Matsumoto’s fourth embodiment device. (TSMC-1003, ¶¶257-59.) As discussed in §XII.A.3.a, Matsumoto discloses a list of exemplary high-k films which can be used as a gate dielectric. (TSMC-1009, ¶107.) A POSITA would have been motivated to investigate other high-k options, including hafnium-based materials, and would have been led to Koyama’s study of HfSiON. (TSMC-1003, ¶258.) A POSITA would have been motivated to make the above combination to achieve the enhanced benefits of HfSiON high-k film, e.g.,

improved thermal stability and electrical characteristics, described by Koyama.
(TSMC-1003, ¶259; §VI.)

Moreover, the combination is nothing more than use of a known technique (Koyama's use of HfSiON as a gate insulating film) to improve similar devices in the same way. *KSR*, 550 U.S. at 416-417; TSMC-1003, ¶260. A POSITA would have had a reasonable expectation of success and the combination would have yielded predictable results for the reasons discussed in §VI. (TSMC-1003, ¶260.)

B. Claims 1 and 4

In the combination of Matsumoto's fourth embodiment and Koyama, Matsumoto's gate insulating film 6 comprises HfSiON, as taught by Koyama. (TSMC-1003, ¶256.) Thus, the combination discloses "*a gate insulating film ... including Hf*" [1A] and "*formed of a HfSiON film*" [4]. For this reason and the reasons discussed in §§XII.B, XIV.A, the Matsumoto-Koyama renders obvious claims 1 and 4. (*Id.*)

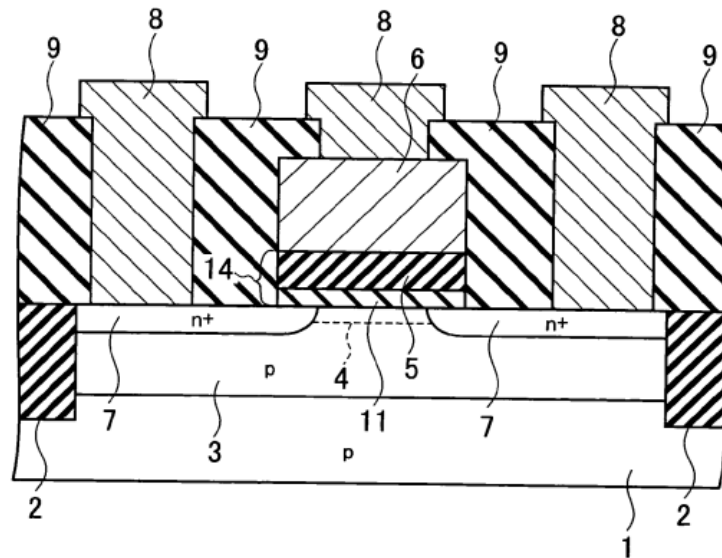
XV. GROUND 11: Matsumoto-Ono Combination Renders Claims 1, 5, and 11-12 Obvious.

A. Ono

Ono's second embodiment FET includes a gate stack comprising gate insulator film 5 "made of a metal oxide" and gate insulator film 11 "made of a metal oxide with a higher dielectric constant than the gate insulator film 5."

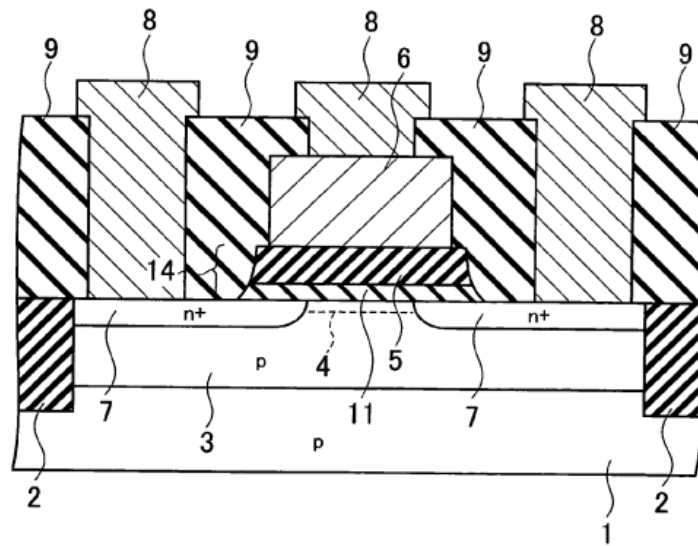
(TSMC-1013, ¶207, Figure 77.) Gate insulator film 5 is made of a "HfO₂ film."

(TSMC-1013, ¶209.) Gate electrode 6 is formed on gate insulator film 5 and can have gate sidewalls. (TSMC-1013, ¶¶207, 181, 210, Figure 77.) Ono and Matsumoto are in the same field as the '076 patent, “a semiconductor device and a method for fabricating the semiconductor device.” (TSMC-1001, 1:18-19; TSMC-1009, ¶2; TSMC-1013, Abstract, ¶¶3-7; TSMC-1003, ¶261.)

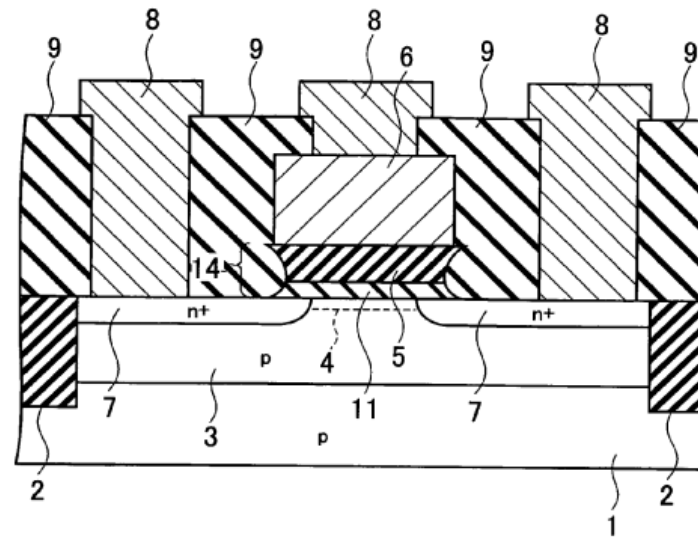


Ono, Figure 77

Ono discloses a modification of its second embodiment devices where the sidewalls of this two-layered structure “may curve.” (TSMC-1013, ¶216.) Ono discloses numerous examples of such curved end portions (Figures 104-123). (TSMC-1013, ¶200.) Petitioner focuses its analysis on the structure depicted in Figures 107 and 108 (reproduced below), although other structures are equally applicable.



Ono, Figure 107



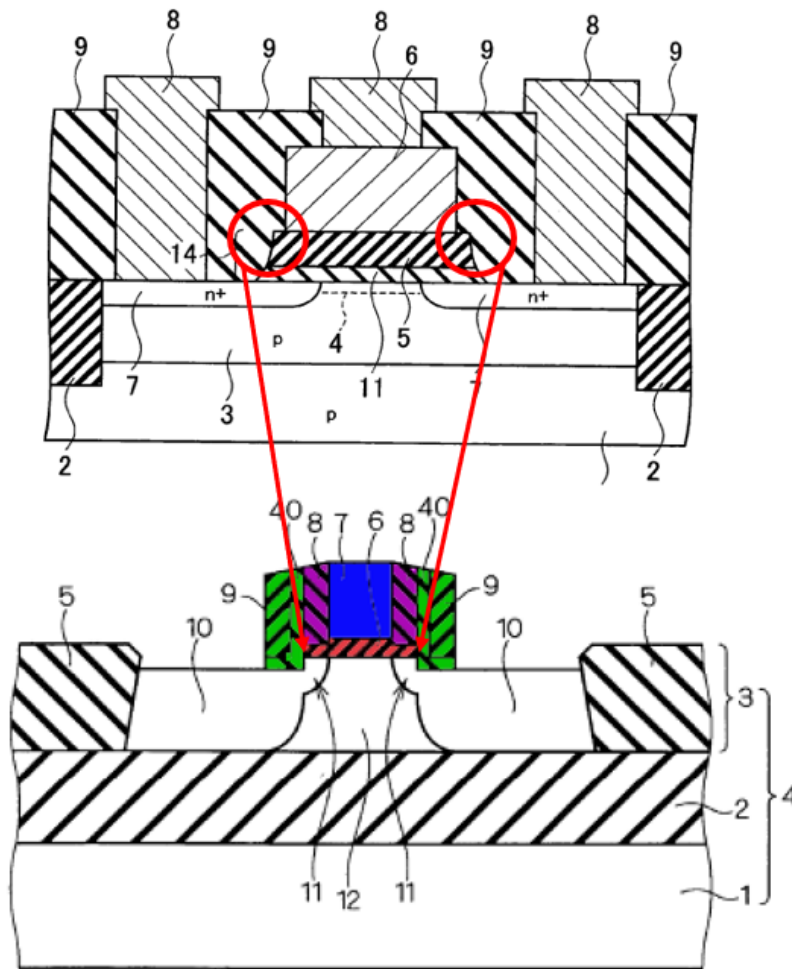
Ono, Figure 108

B. Motivation to Combine

A POSITA would have been motivated to combine the teachings of Matsumoto and Ono. First, a POSITA would have been motivated to select a Hf-based oxide as the gate insulating film in Matsumoto's device, as taught by Ono.

(TSMC-1003, ¶267; TSMC-1013, ¶209 (describing use of a “HfO₂ film”).) As discussed in §V.B.2, a POSITA would have been motivated to select HfO₂ given its known benefits. (TSMC-1037, 2.4.1; TSMC-1032, 207; TSMC-1049, 134; TSMC-1003, ¶267.)

Second, a POSITA would have also been motivated to apply Ono’s teaching of curving the end portion of a gate insulating film to Matsumoto’s device, as illustrated below. (TSMC-1003, ¶268.)



Ono, Figure 107 (top); Matsumoto, Figure 22 (bottom)

Ono expressly suggests the combination, teaching that using its curved side surfaces provides “an advantage of possible optimization ... by reducing the scattering of carriers as well as enhancing the controllability of the gate electrode with respect to the potential of the channel region.” (TSMC-1013, ¶216; *see also* TSMC-1013, ¶200 (noting, for another embodiment, by using curved side surfaces, “the electrical capacitance between the gate electrode 6 and the source/drain regions 7 may be adjusted,” resulting in “an advantage of optimization”). Ono’s curved sidewall approach therefore provides optimization—reducing carrier scattering while enhancing control of the gate electrode over the channel. (TSMC-1003, ¶¶269-70; TSMC-1013, ¶206.) A POSITA would have been further motivated to curve the end of Matsumoto’s gate insulating film to optimize parasitic resistance and parasitic capacitance, improving device performance. (TSMC-1003, ¶272; TSMC-1040, ¶108; §IV.B.2.)

The Matsumoto-Ono combination is merely the application of a known technique (Ono’s curved film ends) to improve similar devices in the same way (modifying the dielectric layer to control capacitance) for the above reasons. *KSR*, 550 U.S. at 416-17; TSMC-1003, ¶273. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable. (TSMC-1003, ¶273.) Matsumoto and Ono both use high-k gate insulating films that extend under the gate electrode and the insulating

sidewall, a concept well-known before the '076 patent. (§§IV.B.2.b, IV.D.2, XII.A.1, XV.A.) And both form their high-k dielectrics using conventional techniques. (TSMC-1009, ¶114; TSMC-1013, ¶167; TSMC-1003, ¶273.)

C. Claim 1

For the reasons discussed in §XII.B, Matsumoto discloses each limitation of claim 1, except it does not expressly disclose “*a gate insulating film ... including Hf*” [1A]. (TSMC-1003, ¶274.) In the combination, Matsumoto’s gate insulating film 6 comprises HfO₂, as taught by Ono. (TSMC-1003, ¶274; TSMC-1013, ¶200.) Accordingly, the Matsumoto-Ono combination renders obvious claim 1. (TSMC-1003, ¶274.)

D. Claims 11-12

The Matsumoto-Ono combination discloses “*the end of the gate insulating film located under the insulating sidewall has a tapered surface*” [11] and “*the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof*” [12]. (TSMC-1003, ¶¶275-77.)

As discussed above, the Matsumoto-Ono combination includes a gate insulating film with curved ends under the “*insulating sidewall.*” As shown below in the exemplary shape of Ono Figure 107, the curved shape, when used with Matsumoto’s gate insulating film, has a thickness that decreases toward the end of

film in the '076 patent's Figure 7. (TSMC-1003, ¶277; §IV.C.)



Ono, Figure 107 with enlargement

E. Claim 5

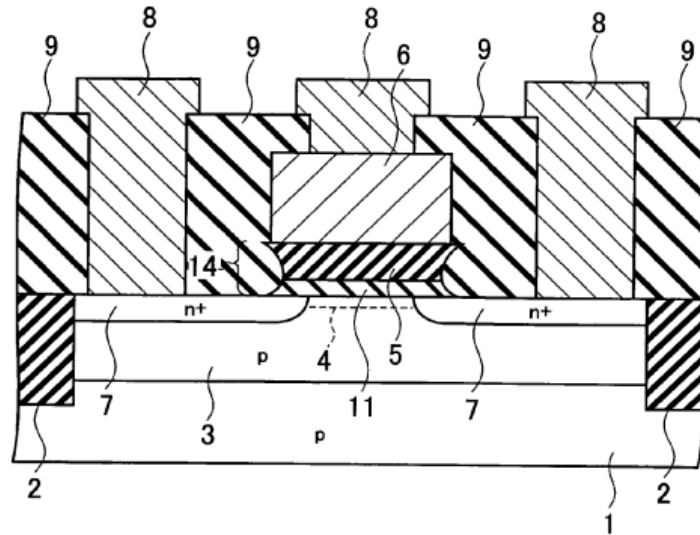
The combination of Matsumoto and Ono discloses “*part of the gate insulating film located under the insulating sidewall includes a notch at the end thereof*” [5]. (TSMC-1003, ¶¶278-81.)

The '076 patent figures depict a “*notch*” in the gate insulating film as a semicircular shape. (E.g., TSMC-1001, 8:41-46 (referring to notch 20 of Figure 7 under sidewall 6), Figure 7 (depicting notch 20 having a semicircular shape); TSMC-1003, ¶281.)



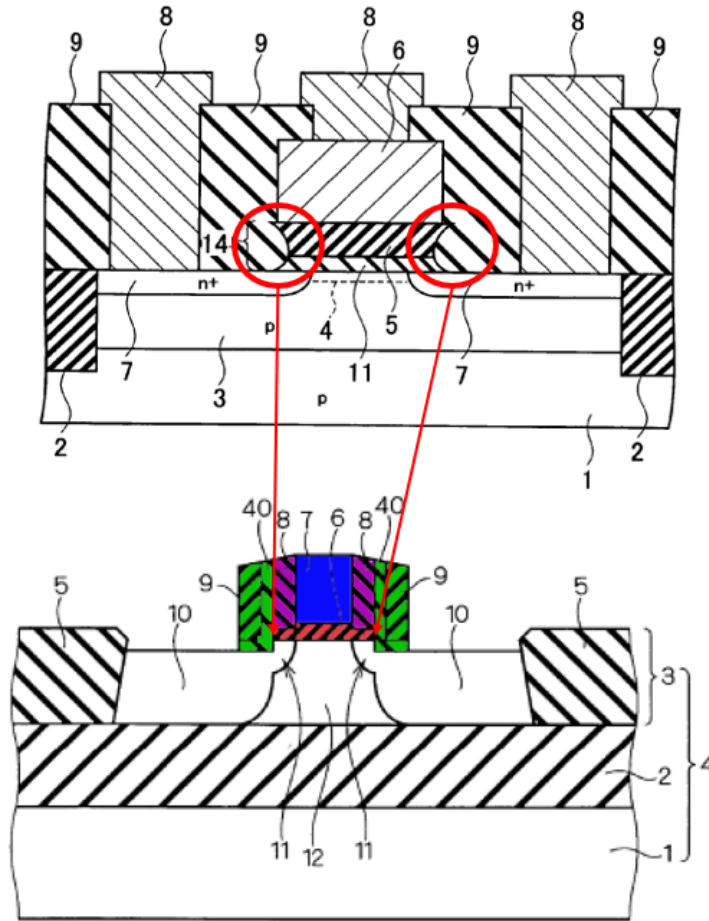
'076 Patent, Figure 7 with enlargement

As one example of a curved end in the gate insulating film, Ono discloses the same semicircular shape as the '076 patent, as shown in Figure 108 below. A POSITA would have been motivated to apply Ono's teaching of such a curved end to Matsumoto's fourth embodiment device for the same reasons discussed in §XV.B above. (TSMC-1003, ¶280.)



Ono, Figure 108

As discussed in §XII.B.5, Matsumoto’s gate insulating film 6 extends from under gate electrode 7 to under sidewall film 8 (alone, or in combination with films 40 and 9, the “*insulating sidewall*”). As illustrated below, in the device of the Matsumoto-Ono combination, the end portion of the Matsumoto’s gate insulating film has a semicircular shape under sidewall 8, as taught by Ono in, e.g., Figure 108. Consistent with the ’076 patent’s disclosure discussed above, the semicircular shape of the gate insulating film’s side end in the combination discloses “*a notch.*” (TSMC-1003, ¶281.)



Ono, Figure 108 (top); Matsumoto, Figure 22 (bottom)

XVI. Discretionary Denial Is Not Appropriate.

A. 35 U.S.C. §314(a)

Pursuant to the Stewart Memorandum dated March 26, 2025, titled “Interim Process for PTAB Workload Management,” Petitioner will respond to any discretionary denial arguments Patent Owner may raise through the Board’s bifurcated briefing process.

Nevertheless, to simplify the *Fintiv* analysis, and following the precedential *Sotera* decision, Petitioner stipulates that, if IPR is instituted, Petitioner will not

pursue in the related district court proceeding any ground that Petitioner raised or reasonably could have raised against the challenged claims during the instituted IPR.

B. 35 U.S.C. §325(d)

The *Advanced Bionics* framework favors institution. *Advanced Bionics LLC v. MED-EL Elektromedizinische Gerate GmbH*, IPR2019-01469, Paper 6 (P.T.A.B. Feb. 13, 2020) (precedential). None of the applied references was applied by the Examiner during prosecution. Applicant cited a different publication to Matsumoto, U.S. Patent Publication 2004/0227185 (“Matsumoto-185”), and a different JP publication to Ono (JP2005-064190; “JP-Ono”) on an information disclosure statement. While Petitioner disputes that Matsumoto-185 is sufficiently similar to Matsumoto or JP-Ono is sufficiently similar to Ono to trigger *Advanced Bionics* Part 1, Matsumoto 185 and JP-Ono were not applied by the Examiner and thus were not evaluated during examination. Even assuming Matsumoto-185 and JP-Ono were evaluated (which the record does not support), the Office erred in allowing the claims, because Matsumoto discloses all limitations of claim 1, including the “gate insulating film,” “active region in a substrate,” and “gate electrode” limitations argued by Applicant and determined to be allowable by the Examiner. (TSMC-1002, 6; §§XII.B.2-3.) And Ono discloses the “notch” and “tapered surface” limitations of claims 5 and 11-12. (§XV.D-E.) Moreover, the

Petitioner's evidence warrants consideration because it presents a compelling case of unpatentability never considered by the Office. These circumstances weigh heavily against §325(d) discretionary denial.

XVII. Mandatory Notices

A. Real Party in Interest

The Petitioner and real party in interest is Taiwan Semiconductor Manufacturing Company Ltd.

B. Related Matters

To the best of Petitioner's knowledge, the '076 patent is involved in the following ongoing litigation:

- *Advanced Integrated Circuit Process LLC, v. Taiwan Semiconductor Manufacturing Company Limited*, No. 2:24-CV-623 (E.D.T.X.)
- *Advanced Integrated Circuit Process LLC, v. United Microelectronics Corporation*, No. 2:24-CV-730 (E.D.T.X.)

On April 15, 2025, Petitioner filed petitions for *inter partes* review of U.S. Patent 7,579,277 (IPR2025-00828), U.S. Patent 7,923,764 (IPR2025-00829), and U.S. Patent 8,253,180 (IPR2025-00830).

C. Notice of Counsel and Service Information

Pursuant to 37 C.F.R. §§42.8(b)(3), 42.8(b)(4) and 42.10(a), Petitioner appoints the following lead and backup counsel:

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XVIII. Conclusion

Inter partes review of the challenged claims is respectfully requested.

Respectfully submitted,

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Date: April 15, 2025

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(a), Petitioner hereby certifies that portions of the above-captioned **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 8,587,076**, in accordance with and reliance on the word count provided by the word-processing system used to prepare this Petition, that the number of words in this paper is 13,917. Pursuant to 37 C.F.R. §42.24(a), this word count is in compliance and excludes the table of contents, table of authorities, mandatory notices under §42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing. This word count was prepared using Microsoft Word.

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies, in accordance with 37 C.F.R. § 42.105, that the foregoing **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 8,587,076**, TSMC's Power of Attorney, and all supporting exhibits were served via FedEx Next Business Day Delivery on April 15, 2025, in their entirety on the Patent Owner as detailed below:

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Cherskov, Flaynik & Gurda, LLC
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Courtesy copies have been concurrently served by electronic mail on Patent Owner's litigation counsel at:

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Appendix: Challenged Claims Listing

[1P] A semiconductor device comprising:

[1A] a gate insulating film formed on an active region in a substrate and including Hf;

[1B] a gate electrode formed on the gate insulating film;

[1C] a insulating sidewall formed on each side surface of the gate electrode; and

[1D] wherein a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length, and

[1E] an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode.

[2] The semiconductor device of claim 1, further comprising a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film.

[3] The semiconductor device of claim 1, wherein the gate insulating film is formed of a Hf based oxide.

[4] The semiconductor device of claim 1, wherein the gate insulating film is formed of a HfSiON film.

[5] The semiconductor device of claim 1, wherein a part of the gate insulating film located under the insulating sidewall includes a notch at the end thereof.

[6] The semiconductor device of claim 1, wherein a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.

[7] The semiconductor device of claim 1, wherein an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall.

[8] The semiconductor device of claim 1, wherein the insulating sidewall has a double layer structure including an oxide film and a nitride film.

[9] The semiconductor device of claim 1, wherein the insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film.

[10] The semiconductor device of claim 1, wherein a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length.

[11] The semiconductor device of claim 1, wherein the end of the gate insulating film located under the insulating sidewall has a tapered surface.

[12] The semiconductor device of claim 1, wherein the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof.

[13] The semiconductor device of claim 1, wherein the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length.