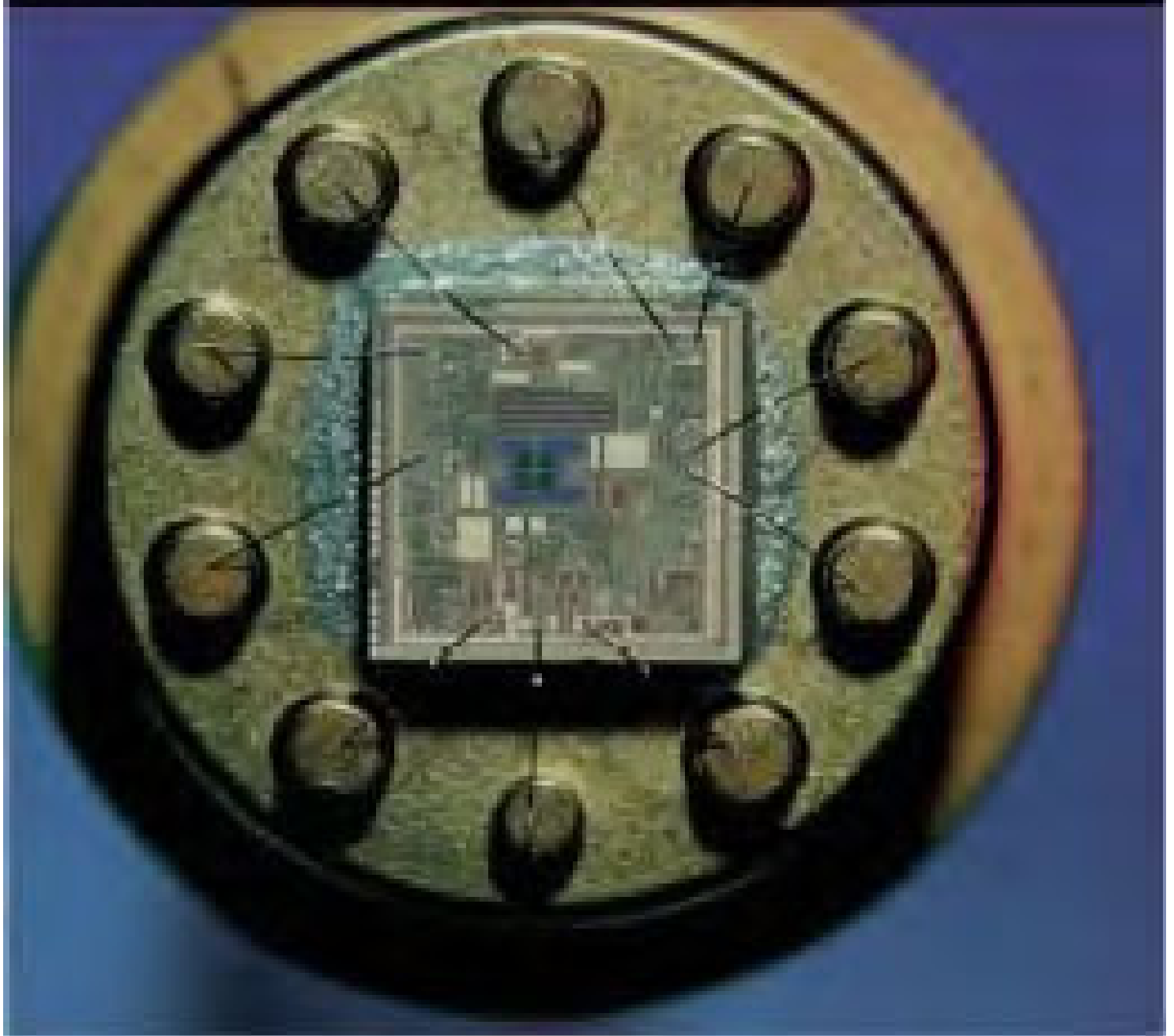


Microelectronic Circuits

FOURTH EDITION

Sedra/Smith



Oxford University Press

Oxford New York
Athens Auckland Bangkok Bogota Bombay Buenos Aires
Calcutta Cape Town Dar es Salaam Delhi Florence Hong Kong
Istanbul Karachi Kuala Lumpur Madras Madrid Melbourne
Mexico City Nairobi Paris Singapore Taipei Tokyo Toronto Warsaw

and associated companies in

Berlin Ibadan

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Published by Oxford University Press, Inc.,
198 Madison Avenue, New York, New York, 10016
<http://www.oup-usa.org>

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Library of Congress Cataloging-in-Publication Data

Sedra, Adel S.

Microelectronic circuits / Adel S. Sedra, Kenneth C. Smith. — 4th ed.

p. cm. — (Oxford series in electrical and computer engineering)

Includes bibliographical references and index.

ISBN 0-19-511663-1

1. Electronic circuits. 2. Integrated circuits. I. Smith,

Kenneth Carless. II. Title. III. Series.

TK7867.S39 1997

621.381—dc21

97-11254
CIP

9 8 7 6 5 4 3 2

Printed in the United States of America on acid-free paper

Cover Illustration: The chip shown is the ADXL-50 surface-micromachined accelerometer. For the first time, sensor and signal conditioning are combined on a single monolithic chip. In its earliest application, it was a key factor in the improved reliability and reduced cost of modern automotive airbag systems. Photo reprinted with permission of Analog Devices, Inc.



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5.38 Let the inverter specified in Exercise 5.32 be loaded by a 15-pF capacitance. Find the dynamic power dissipation that results when the inverter is switched at a frequency of 2 MHz. What is the average current drawn from the power supply?

Ans. 3 mW; 0.3 mA

5.39 Consider a CMOS VLSI chip having 100,000 gates fabricated in a 1.2- μm CMOS technology. Let the load capacitance per gate be 30 fF. If the chip is operated from a 5-V supply and is switched at a rate of 100 MHz, find (a) the power dissipation per gate, and (b) the total power dissipated in the chip assuming that only 30% of the gates are switched at any one time.

Ans. 75 μW ; 2.25 W

A Final Remark

In this section, we have provided an introduction to CMOS digital circuits. We shall return to this subject in Chapter 13, where CMOS logic gates and other CMOS digital circuits are studied.

5.9 THE MOSFET AS AN ANALOG SWITCH

The CMOS inverter studied in the previous section demonstrates an important application of the MOSFET, namely, its use as a voltage-controlled switch. Specifically, the voltage applied to the gate of each of Q_N and Q_P turns them on and off. In the off position, the MOSFET behaves as an open circuit between drain and source, whereas in the on position, the MOSFET presents a resistance r_{DS} between drain and source. The value of the on resistance of the switch depends on the location of the operating point on the triode-region i_D - v_{DS} curve, and of course, on the gate-source voltage and the device dimensions. Specifically, recall that for operation close to the origin (small v_{DS}), an n -channel MOSFET has

$$r_{DS} = \frac{1}{k'_n \left(\frac{W}{L} \right) (V_{GS} - V_t)}$$

Although it is desirable to have a low value for r_{DS} , the operation of the digital inverter is not critically affected by this value. This is usually the case in digital switches, that is, in applications in which the MOSFET is used to switch digital signals. There are many applications, however, in which the need arises for switching analog signals. Examples of such applications include the design of analog-to-digital and digital-to-analog converters (Chapter 10) and switched-capacitor filters (Chapter 11). In such applications, the switch is said to be an **analog switch**, and performance of the circuit is usually critically affected by the characteristics of the analog switch. In the following, we first consider the requirements and desirable characteristics of an analog switch. Then, we show that although a single MOS transistor can be, and indeed is, used as an analog switch, its characteristics are somewhat less than ideal. Finally, we show that an n -channel and a p -channel MOSFET connected in parallel realize an excellent analog switch. The resulting circuit can obviously be fabricated in CMOS technology and is known as the **CMOS transmission gate**.

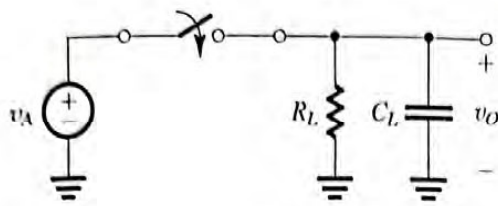


Fig. 5.61 An analog switch connects an analog signal v_A to a circuit represented by a resistance R_L in parallel with a capacitance C_L . The switch is operated by a voltage-control signal (not shown).

The Analog Switch

To appreciate the more stringent requirements placed on an analog switch as compared to a digital switch, consider the circuit in Fig. 5.61. Here, an analog signal v_A is to be connected to a load composed of a resistance R_L in parallel with a capacitance C_L . When the switch is open, we obviously wish to have it operate as close to an open circuit as possible. Thus the off-resistance of the switch should be very high and ideally infinite. In the closed position, the switch should act as close to a short circuit as possible. Observe that the on-resistance of the switch forms an impedance divider with the load network. Thus a high on-resistance would result in signal attenuation. It would also introduce a low-pass filter action (see Section 1.6) with the load capacitance. It follows that the magnitude and phase of the signal that will actually appear at the output will depend critically on the value of the switch on-resistance. An even more serious problem occurs if the value of the on-resistance depends on the magnitude of v_A . If this happens, the ratio of the voltage divider will depend on the magnitude of v_A , and the output signal will be nonlinearly distorted. Finally, note that because v_A can be positive or negative, the switch should be able to conduct current in both directions; that is, it must be a bidirectional switch.

An NMOS Analog Switch

Let's now consider the use of a single MOSFET to implement the analog switch of Fig. 5.61. Such a circuit using an NMOS transistor is depicted in Fig. 5.62. To make our discussion concrete, let v_A be in the range ± 5 V.

In order to keep the substrate-to-source and substrate-to-drain pn junctions reverse-biased at all times, the substrate terminal is connected to -5 V.

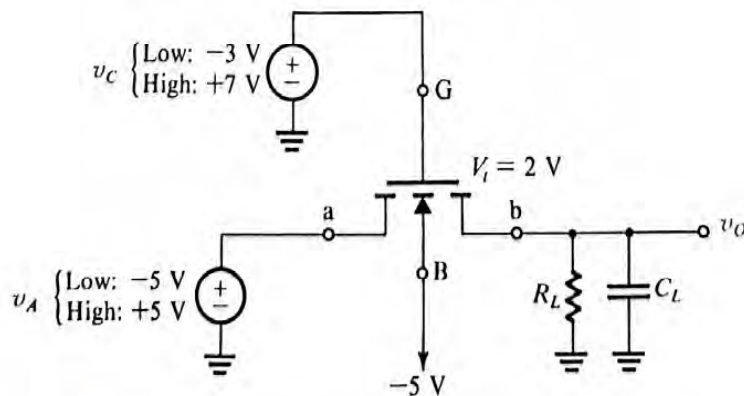


Fig. 5.62 The use of a single NMOS transistor to implement the analog switch in the circuit of Fig. 5.61.

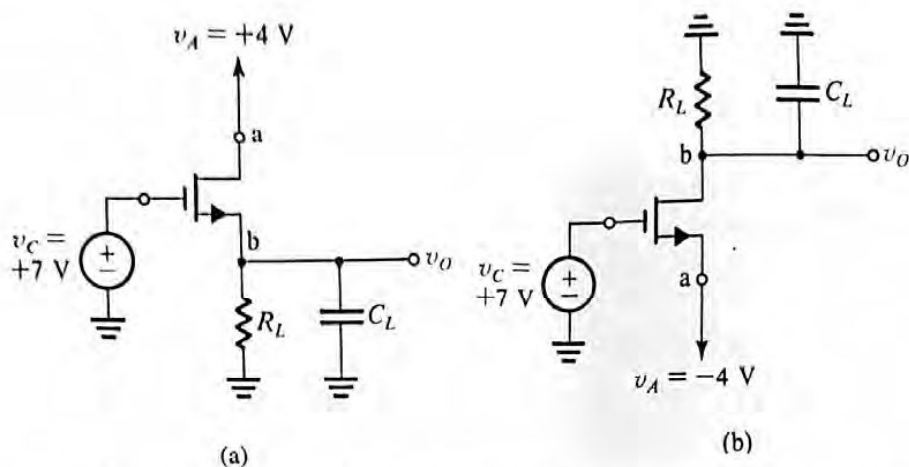


Fig. 5.63 Method for visualizing the operation of the circuit in Fig. 5.62 when v_C is high: (a) v_A is positive; (b) v_A is negative.

The purpose of the control signal v_C is to turn the switch on and off. Assume that the device has a threshold voltage $V_t = 2$ V. It follows that in order to turn the transistor on for all possible input signal levels, the high value of v_C should be at least +7 V. Similarly, to turn the transistor off for all possible input signal levels the low value of v_C should be a maximum of -3 V. Note, however, that these levels are not sufficient in practice, since the transistor will be barely on and barely off at the limits. In any case we see that the range of the control voltage has to be at least equal to the range of the analog input signal being switched. Unfortunately, though, the on resistance of the switch will depend to a large extent on the value of the analog input signal, an undesirable characteristic, as mentioned above. Another obvious disadvantage is the rather inconvenient levels required for v_C .

The reader will observe that we have not indicated in Fig. 5.62 which terminal is the source and which is the drain. We have avoided labeling them first of all because the MOSFET is a symmetric device, with the source and the drain interchangeable. More important, the operation of the device as a switch is based on this interchangeability of roles. Specifically, whichever of the two terminals is at the higher voltage acts as the drain. Thus if the analog input signal is positive, say, +4 V, then terminal *a* acts as the drain and terminal *b* as the source. For this case the circuit (when v_C is high) takes the familiar form shown in Fig. 5.63(a). It is easy to see that the device will be operating in the triode region and that v_O will be very close to the input analog signal level of +4 V. On the other hand, if the input signal is negative, say, -4 V, then terminal *b* acts as the drain and terminal *a* as the source. In this case, the circuit (for v_C high) can be redrawn in the familiar form of Fig. 5.63(b). Here again, it should be clear that the device operates in the triode region, and v_O will be only slightly higher than the input analog signal level of -4 V.

The CMOS Transmission Gate

Let us consider next the more elaborate CMOS analog switch shown in Fig. 5.64. This circuit is commonly known as a **transmission gate**. As in the previous case, we are assuming that the analog signal being switched lies in the range -5 V to +5 V. In order to prevent the substrate junctions from becoming forward-biased at any time, the substrate of the

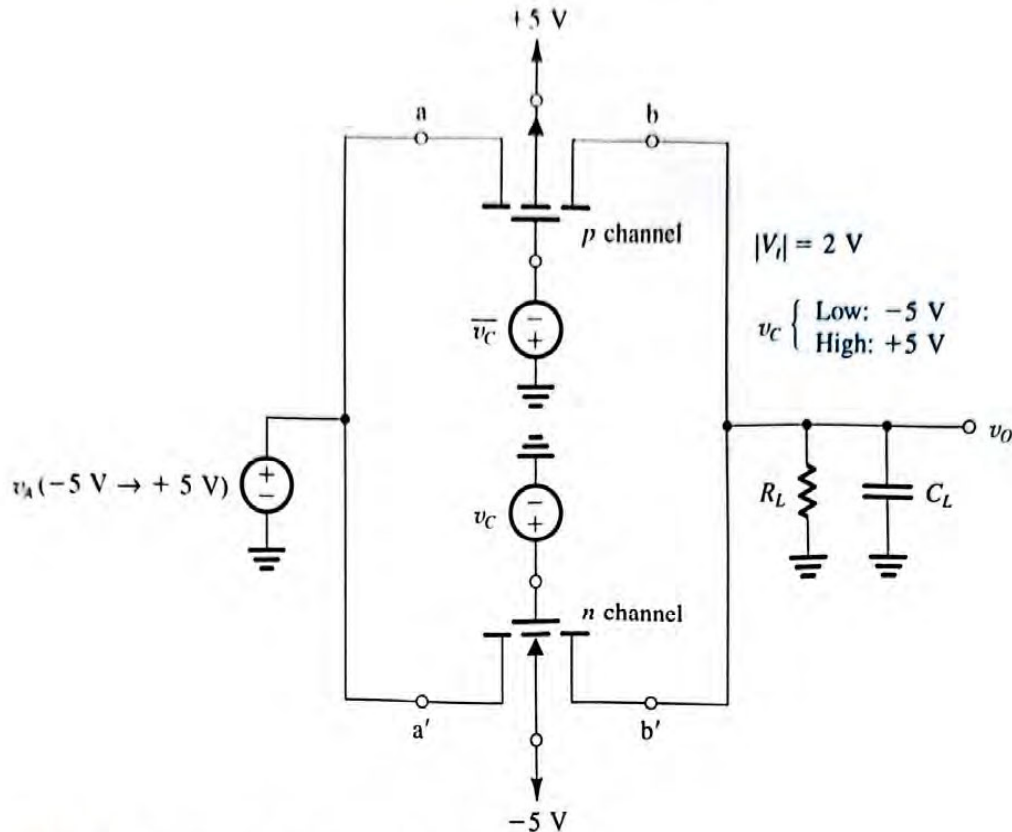


Fig. 5.64 The CMOS transmission gate.

p -channel device is connected to the most positive voltage level (+5 V) and that of the n -channel device is connected to the most negative voltage level (-5 V). The transistor gates are controlled by two complementary signals denoted v_C and $\overline{v_C}$. Unlike the single NMOS switch, here the levels of v_C can be the same as the extremes of the analog signal, +5 V and -5 V. When v_C is at the low level, the gate of the n -channel device will be at -5 V, thus preventing the n -channel device from conducting for any value of v_A (in the range -5 V to +5 V). Simultaneously, the gate of the p -channel device will be at +5 V, which prevents that device from conducting for any value of v_A (in the range -5 V to +5 V). Thus with v_C low the switch is open.

In order for us to close the switch, we have to raise the control signal v_C to the high level of +5 V. Correspondingly, the n -channel device will have its gate at +5 V and will thus conduct for any value of v_A in the range of -5 V to +3 V. Simultaneously, the p -channel device will have its gate at -5 V and will thus conduct for any value of v_A in the range -3 V to +5 V. We thus see that for v_A less than -3 V, only the n -channel device will be conducting, while for v_A greater than +3 V, only the p -channel device will be conducting. For the range $v_A = -3$ V to +3 V both devices will be conducting. Furthermore, we can see that as one device conducts more heavily, conduction in the other device is reduced. Thus as the resistance r_{DS} of one device decreases, the resistance of the other device increases, with the parallel equivalent, which is the "on" resistance of the switch, remaining approximately constant. This is clearly an advantage of the CMOS transmission gate over the single NMOS switch previously considered. This advantage applies in addition

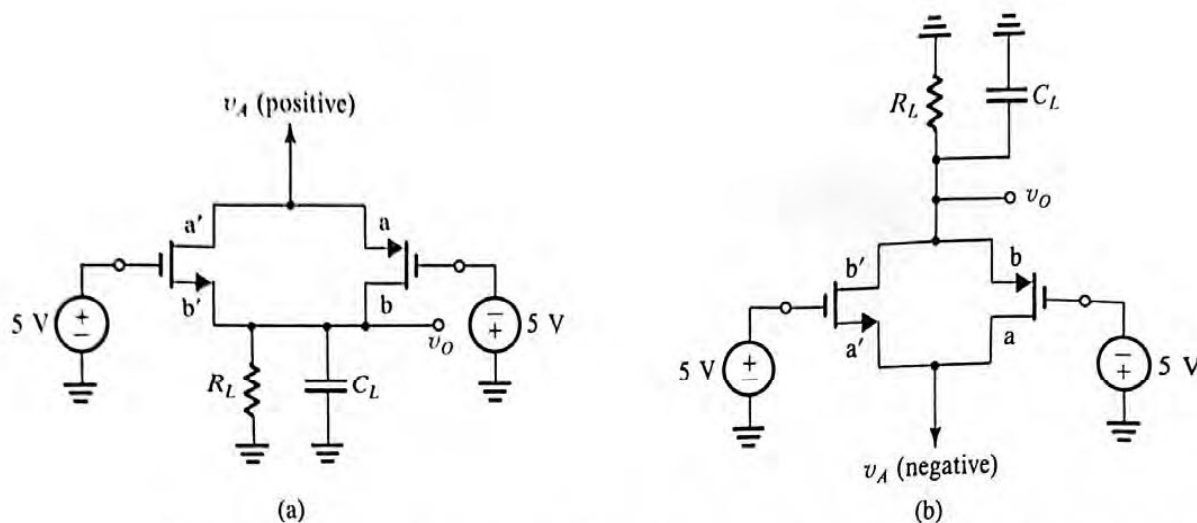


Fig. 5.65 Equivalent circuits for visualizing the operation of the transmission gate in the closed (on) position: (a) v_A is positive; (b) v_A is negative.

to the obviously more convenient levels required for the control signal in the CMOS switch.

The operation of the transmission gate (in the closed position) can be better understood from the two equivalent circuits shown in Fig. 5.65. Here, the circuit in Fig. 5.65(a) applies when v_A is positive, while that in Fig. 5.65(b) applies when v_A is negative. Note the interchangeability of the roles played by the source and drain of each of the two devices. Again, for the n -channel device, the terminal at the higher voltage acts as the drain, and the opposite is true for the p -channel device. Thus in thinking about the operation of the CMOS gate, one should consider that the drain of one device is connected to the source of the other, and vice versa.

Compared to the single NMOS switch, the transmission gate provides better performance at the expense of greater circuit complexity and chip area. Whether to use a single MOSFET or a transmission gate will depend on the requirements of the particular application.

Although basically an excellent analog switch, the CMOS transmission gate finds application also in digital circuit design, as will be shown in Chapter 13. Finally, we show in Fig. 5.66 the transmission gate together with its commonly used circuit symbol.

Exercise

5.40 Consider the CMOS transmission gate and its equivalent circuit shown in Fig. 5.65(b). Let the two devices have $|V_t| = 2$ V and $k'(W/L) = 100 \mu\text{A}/\text{V}^2$, and let $R_L = 50 \text{ k}\Omega$. For (a) $v_A = -5$ V, (b) $v_A = -2$ V, and (c) $v_A = 0$ V, calculate v_O and the total resistance of the switch.

Ans. (a) -4.878 V, $1.25 \text{ k}\Omega$; (b) -1.986 V, $1.649 \text{ k}\Omega$; (c) 0 V, $1.667 \text{ k}\Omega$

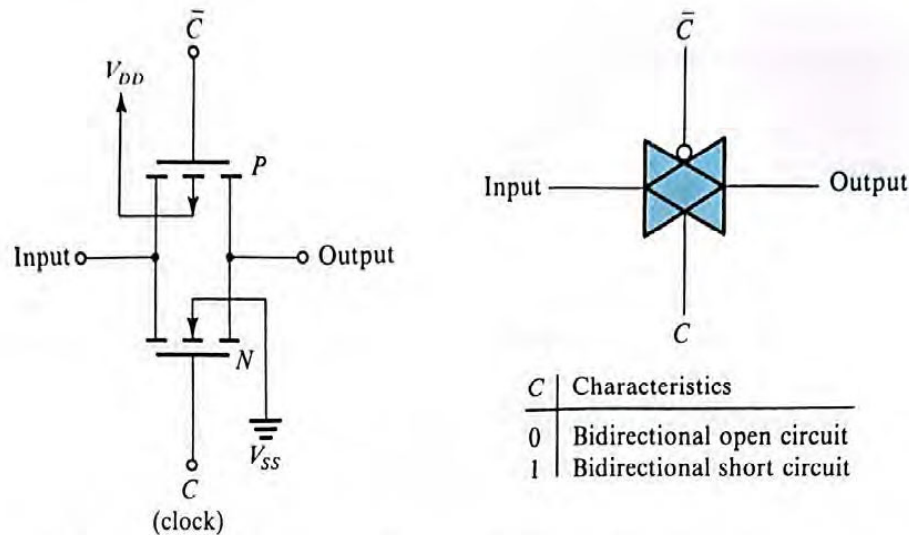


Fig. 5.66 The CMOS transmission gate together with its commonly used circuit symbol.

A Final Remark: Comparison of the MOSFET and the BJT Analog Switches

The MOSFET is much better suited to the design of analog switches than the BJT. This is mainly because the MOSFET i_D - v_{DS} characteristics pass right through the origin and extend symmetrically into the third quadrant. In contrast, the i_C - v_{CE} characteristics of the BJT intercept the v_{CE} axis at a finite, though small, voltage (≈ 0.1 V). Thus the BJT switch exhibits an offset voltage (see Section 4.12).

5.10 THE MOSFET INTERNAL CAPACITANCES AND HIGH-FREQUENCY MODEL⁷

From our study of the physical operation of the MOSFET in Section 5.1, we know that the device has internal capacitances. In fact, we used one of these, the gate-to-channel capacitance, in our derivation of the MOSFET i - v characteristics. We did, however, implicitly assume that the steady-state charges on these capacitances are acquired instantaneously. In other words, we did not account for the finite time required to charge and discharge the various internal capacitances. As a result, the device models we derived, for instance, the small-signal model, do not include any capacitances. The use of these models would predict constant amplifier gains independent of frequency. We know, however, that this is (unfortunately) not the case; in fact, the gain of every MOSFET amplifier falls off at some high frequency. Similarly, the MOSFET inverter exhibits a finite, nonzero propagation delay.⁸

⁷ The material in this section will be needed for the study of the frequency response of MOS amplifiers in Chapter 7, and the time response of MOS digital circuits in Chapter 13. Thus study of this section can be postponed to a later time.

⁸ We did in fact see this in Section 5.8, where the dynamic operation of the CMOS inverter was analyzed. Recall that a capacitance C was connected between the output node and ground, and it was mentioned that C included the transistor internal capacitances.

Exercise

12.10 A 2-MHz quartz crystal is specified to have $L = 0.52 \text{ H}$, $C_s = 0.012 \text{ pF}$, $C_p = 4 \text{ pF}$, and $r = 120 \Omega$. Find f_s , f_p , and Q .

Ans. 2.015 MHz; 2.018 MHz; 55,000

12.4 BISTABLE MULTIVIBRATORS

In this section we begin the study of the other type of waveform-generating circuits—nonlinear oscillators or function generators. These make use of a special class of circuits known as **multivibrators**. As mentioned earlier, there are three types of multivibrators: bistable, monostable and astable. This section is concerned with the first, the bistable multivibrator.

As its name indicates, the **bistable multivibrator** has *two stable states*. The circuit can remain in either stable state indefinitely and moves to the other stable state only when appropriately *triggered*.

The Feedback Loop

Bistability can be obtained by connecting an amplifier in a positive-feedback loop having a loop gain greater than unity. Such a feedback loop is shown in Fig. 12.17; it consists of an op amp and a resistive voltage divider in the positive-feedback path. To see how bistability is obtained, consider operation with the positive input terminal of the op amp near ground potential. This is a reasonable starting point since the circuit has no external excitation. Assume that the electrical noise that is inevitably present in every electronic circuit causes a small positive increment in the voltage v_+ . This incremental signal will be amplified by the large open-loop gain A of the op amp, with the result that a much greater signal will appear in the op amp's output voltage v_O . The voltage divider R_1 , R_2 will feed a fraction $\beta \equiv R_1/(R_1 + R_2)$ of the output signal back to the positive input terminal of the op amp. If $A\beta$ is greater than unity, as is usually the case, the fed-back signal will be greater than the original increment in v_+ . This *regenerative* process continues until eventually the op amp saturates with its output voltage at the positive saturation level, L_+ . When this happens the voltage at the positive input terminal, v_+ , becomes $L_+R_1/(R_1 + R_2)$, which is positive

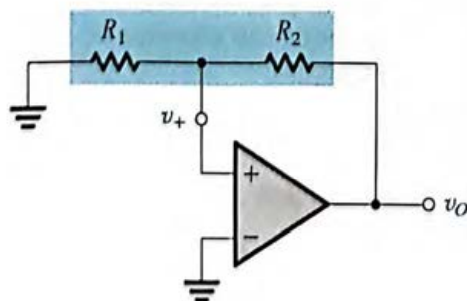


Fig. 12.17 A positive-feedback loop capable of bistable operation.

and thus keeps the op amp in positive saturation. This is one of the two stable states of the circuit.

In the description above we assumed that when v_+ was near zero volts, a positive increment occurred in v_+ . Had we assumed the equally probable situation of a negative increment, the op amp would have ended up saturated in the negative direction with $v_O = L_-$ and $v_+ = L_-R_1/(R_1 + R_2)$. This is the other stable state.

We thus conclude that the circuit of Fig. 12.17 has two stable states, one with the op amp in positive saturation and the other with the op amp in negative saturation. The circuit can exist in either of these two states indefinitely. We also note that the circuit cannot exist in the state for which $v_+ = 0$ and $v_O = 0$ for any length of time. This is a state of *unstable equilibrium* (also known as a **metastable state**); any disturbance, such as that caused by noise, causes the bistable circuit to switch to one of its two stable states. This is in sharp contrast to the case when the feedback is negative, causing a virtual short circuit to appear between the op amp's input terminals and maintaining this virtual short circuit in the face of disturbances. A physical analogy for the operation of the bistable circuit is depicted in Fig. 12.18.

Transfer Characteristics of the Bistable Circuit

The question naturally arises as to how we can make the bistable circuit of Fig. 12.17 change state. To help answer this crucial question, we derive the transfer characteristics of the bistable. Reference to Fig. 12.17 indicates that either of the two circuit nodes that are connected to ground can serve as an input terminal. We investigate both possibilities.

Figure 12.19(a) shows the bistable circuit with an input v_I applied to the inverting input terminal of the op amp. To derive the transfer characteristic v_O-v_I , assume that v_O is at one of its two possible levels, say L_+ , and thus $v_+ = \beta L_+$. Now as v_I is increased from 0 V we can see from the circuit that nothing happens until v_I reaches a value equal to v_+ (that is, βL_+). As v_I begins to exceed this value, a net negative voltage develops between the input terminals of the op amp. This voltage is amplified by the open-loop gain of the op amp, and thus v_O goes negative. The voltage divider in turn causes v_+ to go negative, thus increasing the net negative input to the op amp and keeping the regenerative process going. This process culminates in the op amp saturating in the negative direction; that is, with

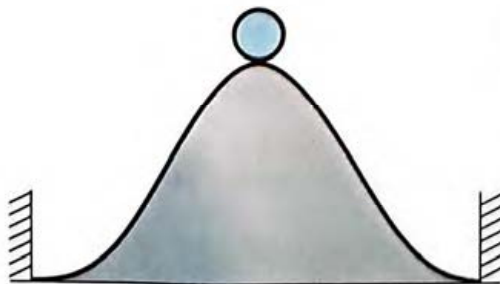


Fig. 12.18 A physical analogy for the operation of the bistable circuit. The ball cannot remain at the top of the hill for any length of time (a state of unstable equilibrium or metastability); the inevitably present disturbance will cause the ball to fall to one side or the other, where it can remain indefinitely (the two stable states).

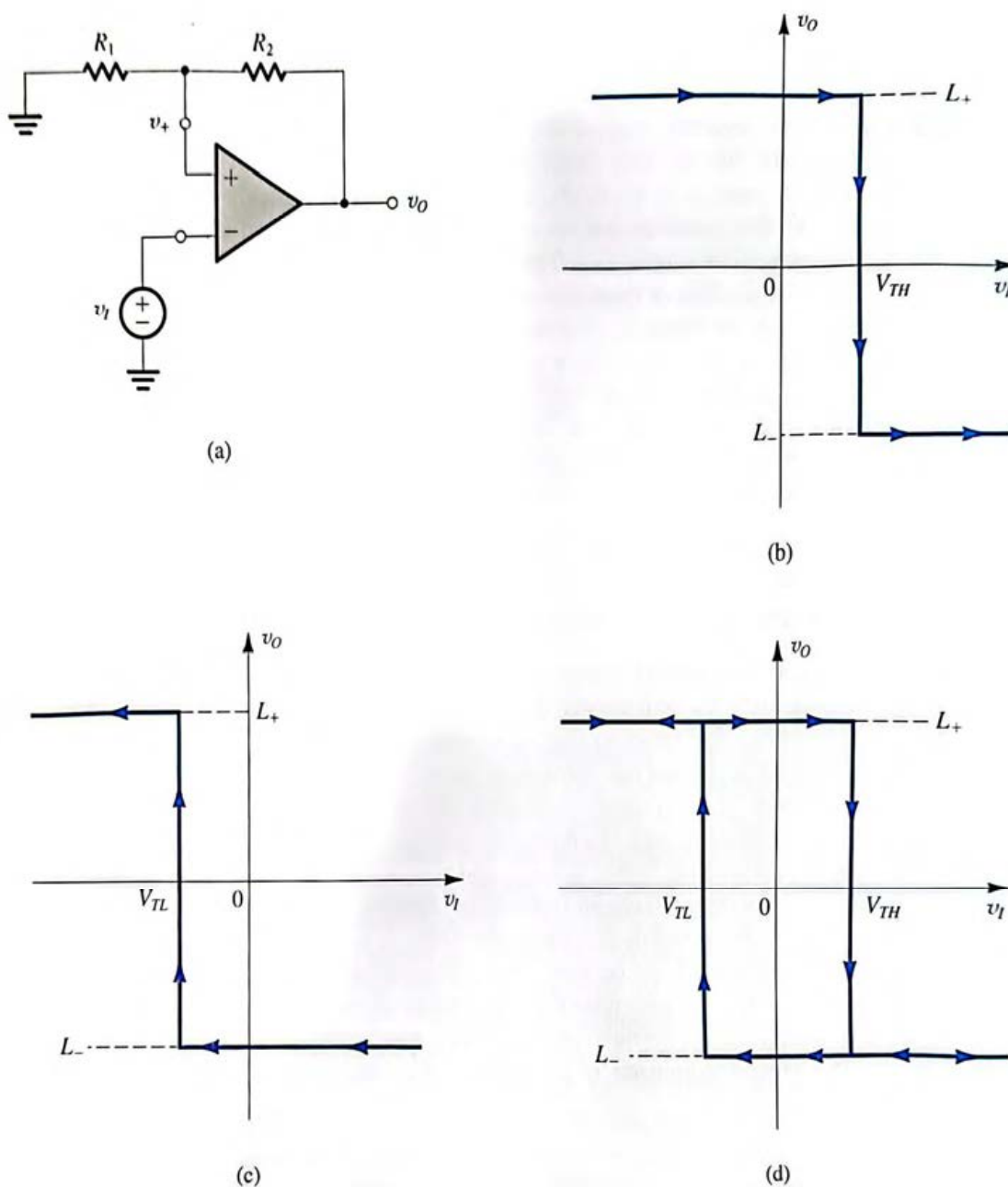


Fig. 12.19 (a) The bistable circuit of Fig. 12.17 with the negative input terminal of the op amp disconnected from ground and connected to an input signal v_I . (b) The transfer characteristic of the circuit in (a) for increasing v_I . (c) The transfer characteristic for decreasing v_I . (d) The complete transfer characteristics.

$v_O = L_-$ and, correspondingly, $v_+ = \beta L_-$. It is easy to see that increasing v_I further has no effect on the acquired state of the bistable circuit. Figure 12.19(b) shows the transfer characteristic for increasing v_I . Observe that the characteristic is that of a comparator with a threshold voltage denoted V_{TH} , where $V_{TH} = \beta L_+$.

Next consider what happens as v_I is decreased. Since now $v_+ = \beta L_-$, we see that the circuit remains in the negative-saturation state until v_I goes negative to the point that it equals βL_- . As v_I goes below this value, a net positive voltage appears between the op amp's input terminals. This voltage is amplified by the op-amp gain and thus gives rise to a positive voltage at the op amp's output. The regenerative action of the positive-feedback loop then sets in and causes the circuit eventually to go to its positive-saturation state, in which $v_O = L_+$ and $v_+ = \beta L_+$. The transfer characteristic for decreasing v_I is shown in Fig. 12.19(c). Here again we observe that the characteristic is that of a comparator, but with a threshold voltage $V_{TL} = \beta L_-$.

The complete transfer characteristics, v_O - v_I , of the circuit in Fig. 12.19(a) can be obtained by combining the characteristics in Figs. 12.19(b) and (c), as shown in Fig. 12.19(d). As indicated, the circuit changes state at different values of v_I , depending on whether v_I is increasing or decreasing. Thus the circuit is said to exhibit *hysteresis*; the width of the hysteresis is the difference between the high threshold V_{TH} and the low threshold V_{TL} . Also note that the bistable circuit is in effect a comparator with hysteresis. As will be shown shortly, adding hysteresis to a comparator's characteristics can be very beneficial in certain applications. Finally, observe that because the bistable circuit of Fig. 12.19 switches from the positive state ($v_O = L_+$) to the negative state ($v_O = L_-$) as v_I is increased past the positive threshold V_{TH} , the circuit is said to be *inverting*. A bistable with a *noninverting* transfer characteristic is presented shortly.

Triggering the Bistable Circuit

Returning now to the question of how to make the bistable circuit change state, we observe from the transfer characteristics of Fig. 12.19(d) that if the circuit is in the L_+ state it can be switched to the L_- state by applying an input v_I of value greater than $V_{TH} \equiv \beta L_+$. Such an input causes a net negative voltage to appear between the input terminals of the op amp, which initiates the regenerative cycle that culminates in the circuit switching to the L_- stable state. Here it is important to note that the input v_I merely initiates or *triggers* regeneration. Thus we can remove v_I with no effect on the regeneration process. In other words, v_I can be simply a pulse of short duration. The input signal v_I is thus referred to as a **trigger signal**, or simply a **trigger**.

The characteristics of Fig. 12.19(d) indicate also that the bistable circuit can be switched to the positive state ($v_O = L_+$) by applying a negative trigger signal v_I of magnitude greater than that of the negative threshold V_{TL} .

The Bistable Circuit as a Memory Element

We observe from Fig. 12.19(d) that for input voltages in the range $V_{TL} < v_I < V_{TH}$, the output can be either L_+ or L_- , depending on the state that the circuit is already in. Thus, for this input range, the output is determined by the *previous* value of the trigger signal (the trigger signal that caused the circuit to be in its current state). Thus the circuit exhibits *memory*. Indeed, the bistable multivibrator is the basic memory element of digital systems,

as will be seen in Chapter 13. Finally, note that in analog circuit applications, such as the ones of concern to us in this chapter, the bistable circuit is also known as a **Schmitt trigger**.

A Bistable Circuit with Noninverting Transfer Characteristics

The basic bistable feedback loop of Fig. 12.17 can be used to derive a circuit with noninverting transfer characteristics by applying the input signal v_I (the trigger signal) to the terminal of R_1 that is connected to ground. The resulting circuit is shown in Fig. 12.20(a). To obtain the transfer characteristics we first employ superposition to the linear circuit formed by R_1 and R_2 , thus expressing v_+ in terms of v_I and v_O as

$$v_+ = v_I \frac{R_2}{R_1 + R_2} + v_O \frac{R_1}{R_1 + R_2} \quad (12.28)$$

From this equation we see that if the circuit is in the positive stable state with $v_O = L_+$, positive values for v_I will have no effect. To trigger the circuit into the L_- state, v_I must be made negative and of such a value as to make v_+ decrease below zero. Thus the low threshold V_{TL} can be found by substituting in Eq. (12.28) $v_O = L_+$, $v_+ = 0$, and $v_I = V_{TL}$. The result is

$$V_{TL} = -L_+ (R_1/R_2) \quad (12.29)$$

Similarly, Eq. (12.28) indicates that when the circuit is in the negative-output state ($v_O = L_-$), negative values of v_I will make v_+ more negative with no effect on operation. To initiate the regeneration process that causes the circuit to switch to the positive state, v_+ must be made to go slightly positive. The value of v_I that causes this to happen is the high

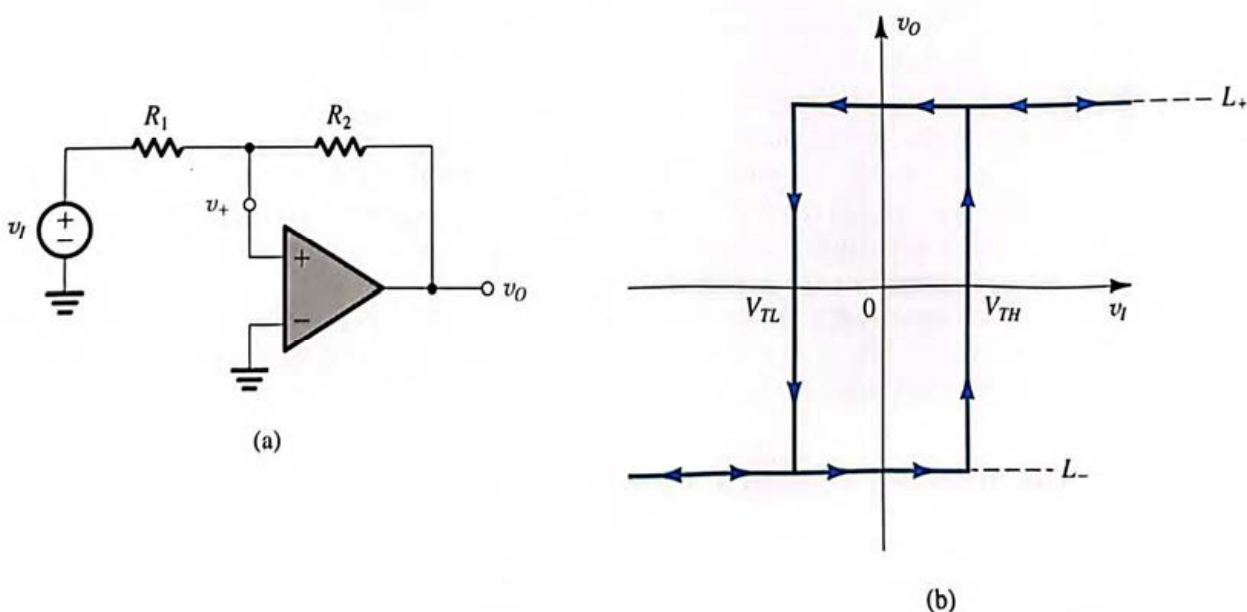


Fig. 12.20 (a) A bistable circuit derived from the positive-feedback loop of Fig. 12.17 by applying v_I through R_1 . (b) The transfer characteristic of the circuit in (a) is noninverting. (Compare it to the inverting characteristic in Fig. 12.19d.)

threshold voltage V_{TH} , which can be found by substituting in Eq. (12.28) $v_O = L_-$ and $v_+ = 0$. The result is

$$V_{TH} = -L_- (R_1/R_2) \quad (12.30)$$

The complete transfer characteristic of the circuit of Fig. 12.20(a) is displayed in Fig. 12.20(b). Observe that a positive triggering signal v_I (of value greater than V_{TH}) causes the circuit to switch to the positive state (v_O goes from L_- to L_+). Thus the transfer characteristic of this circuit is noninverting.

Application of the Bistable Circuit as a Comparator

The comparator is an analog-circuit building block that is used in a variety of applications ranging from detecting the level of an input signal relative to a preset threshold value, to the design of analog-to-digital (A/D) converters (see Section 10.11). Although one normally thinks of the comparator as having a single threshold value (see Fig. 12.21a), it is useful

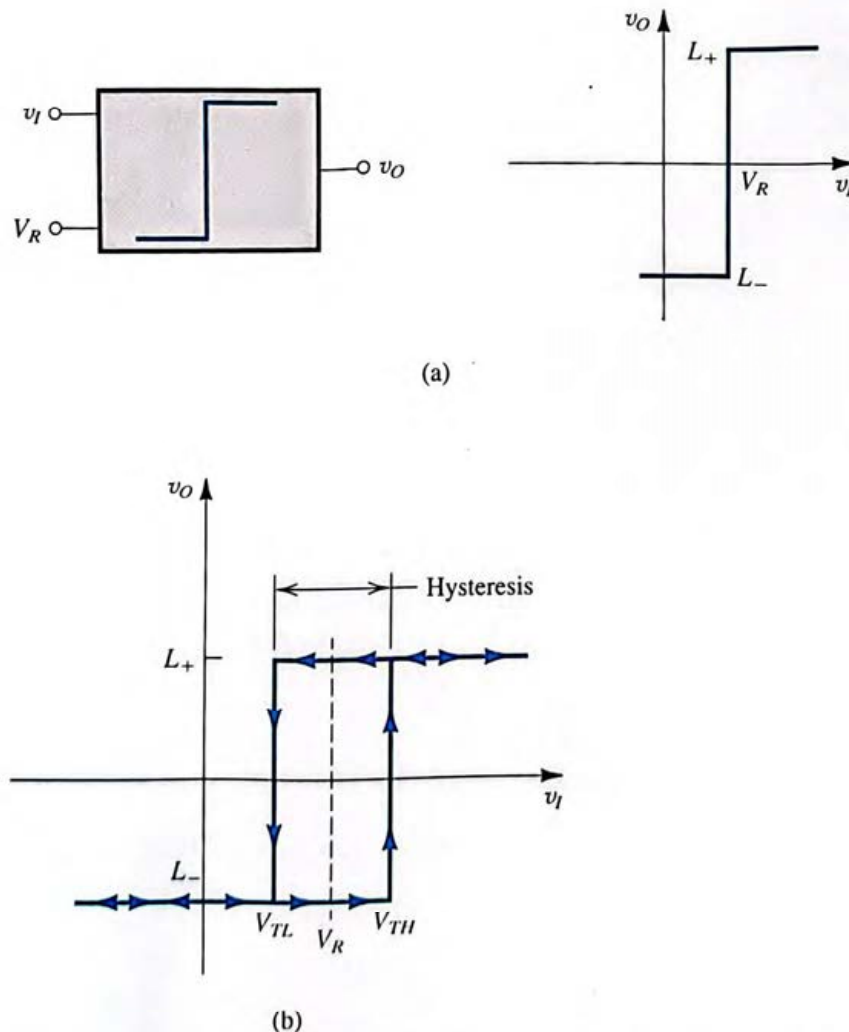


Fig. 12.21 (a) Block-diagram representation and transfer characteristic for a comparator having a reference, or threshold, voltage V_R . (b) Comparator characteristic with hysteresis.

in many applications to add hysteresis to the comparator characteristics. If this is done, the comparator exhibits two threshold values, V_{TL} and V_{TH} , symmetrically placed about the desired reference level, as indicated in Fig. 12.21(b). Usually V_{TH} and V_{TL} are separated by a small amount, say 100 mV.

To demonstrate the need for hysteresis we consider a common application of comparators. It is required to design a circuit that detects and counts the zero crossings of an arbitrary waveform. Such a function can be implemented using a comparator whose threshold is set to 0 V. The comparator provides a step change at its output every time a zero crossing occurs. Each step change can be used to generate a pulse, and the pulses are fed to a counter circuit.

Imagine now what happens if the signal being processed has—as it usually does—interference superimposed on it, say of a frequency much higher than that of the signal. It follows that the signal might cross the zero axis a number of times around each of the zero-crossing points we are trying to detect, as shown in Fig. 12.22. The comparator would thus change state a number of times at each of the zero crossings, and our count would obviously be in error. If we have an idea of the expected peak-to-peak amplitude of the interference, the problem can be solved by introducing hysteresis of appropriate width in the comparator characteristics. Then, if the input signal is increasing in magnitude, the comparator with hysteresis will remain in the low state until the input level exceeds the

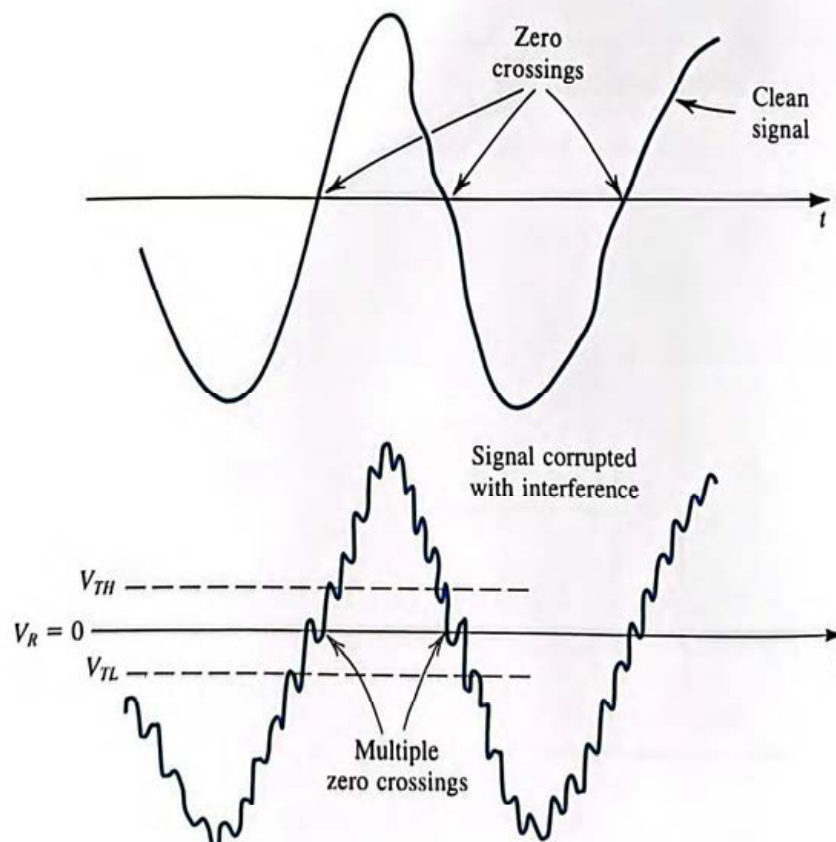
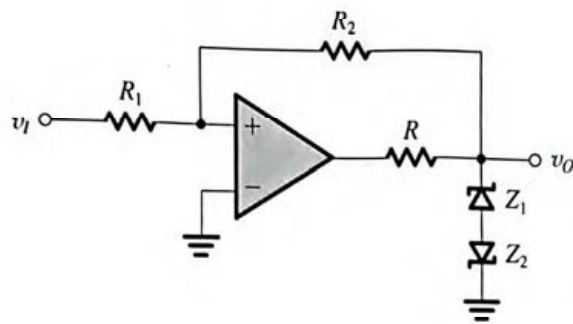
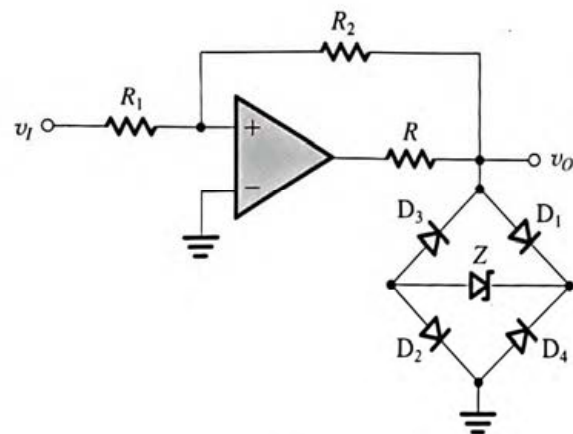


Fig. 12.22 Illustrating the use of hysteresis in the comparator characteristics as a means of rejecting interference.



(a)



(b)

Fig. 12.23 Limiter circuits are used to obtain more precise output levels for the bistable circuit. In both circuits the value of R should be chosen to yield the current required for the proper operation of the zener diodes. (a) For this circuit $L_+ = V_{Z1} + V_D$ and $L_- = -(V_{Z2} + V_D)$, where V_D is the forward diode drop. (b) For this circuit $L_+ = V_Z + V_{D1} + V_{D2}$ and $L_- = -(V_Z + V_{D3} + V_{D4})$.

high threshold V_{TH} . Subsequently the comparator will remain in the high state even if, owing to interference, the signal decreases below V_{TH} . The comparator will switch to the low state only if the input signal is decreased below the low threshold V_{TL} . The situation is illustrated in Fig. 12.22, from which we see that including hysteresis in the comparator characteristics provides an effective means for rejecting interference (thus providing another form of filtering).

Making the Output Levels More Precise

The output levels of the bistable circuit can be made more precise than the saturation voltages of the op amp are by cascading the op amp with a limiter circuit (see Section 3.8 for a discussion of limiter circuits). Two such arrangements are shown in Fig. 12.23.

Exercises

D12.11 The op amp in the bistable circuit of Fig. 12.19(a) has output saturation voltages of ± 13 V. Design the circuit to obtain threshold voltages of ± 5 V. For $R_1 = 10$ k Ω find the value required for R_2 .

Ans. 16 k Ω

D12.12 If the op amp in the circuit of Fig. 12.20(a) has ± 10 -V output saturation levels, design the circuit to obtain ± 5 -V thresholds. Give suitable component values.

Ans. Possible choice: $R_1 = 10 \text{ k}\Omega$ and $R_2 = 20 \text{ k}\Omega$

12.13 Consider a bistable circuit with a noninverting transfer characteristic, and let $L_+ = -L_- = 10 \text{ V}$ and $V_{TH} = -V_{TL} = 5 \text{ V}$. If v_I is a triangular wave with a 0-V average, a 10-V peak amplitude, and a 1-ms period, sketch the waveform of v_O . Find the time interval between the zero crossings of v_I and v_O .

Ans. v_O is a square wave with 0-V average, 10-V amplitude, 1-ms period and is delayed by $125 \mu\text{s}$ relative to v_I .

12.14 Consider an op amp having saturation levels of $\pm 12 \text{ V}$ used without feedback, with the inverting input terminal connected to $+3 \text{ V}$ and the noninverting input terminal connected to v_I . Characterize its operation as a comparator. What are L_+ , L_- , and V_R , as defined in Fig. 12.21(a)?

Ans. $+12 \text{ V}$; -12 V ; $+3 \text{ V}$

12.15 In the circuit of Fig. 12.20(a) let $L_+ = -L_- = 10 \text{ V}$ and $R_1 = 1 \text{ k}\Omega$. Find a value for R_2 that gives hysteresis of 100-mV width.

Ans. $200 \text{ k}\Omega$

12.5 GENERATION OF SQUARE AND TRIANGULAR WAVEFORMS USING ASTABLE MULTIVIBRATORS

A square waveform can be generated by arranging for a bistable multivibrator to switch states periodically. This can be done by connecting the bistable multivibrator with an RC circuit in a feedback loop, as shown in Fig. 12.24(a). Observe that the bistable multivibrator has an inverting transfer characteristic and can thus be realized using the circuit of Fig. 12.19(a). This results in the circuit of Fig. 12.24(b). We shall show shortly that this circuit has no stable states and thus is appropriately named an **astable multivibrator**.

Operation of the Astable Multivibrator

To see how the astable multivibrator operates, refer to Fig. 12.24(b) and let the output of the bistable multivibrator be at one of its two possible levels, say L_+ . Capacitor C will charge toward this level through resistor R . Thus the voltage across C , which is applied to the negative input terminal of the op amp and thus is denoted v_- , will rise exponentially toward L_+ with a time constant $\tau = CR$. Meanwhile, the voltage at the positive input terminal of the op amp is $v_+ = \beta L_+$. This situation will continue until the capacitor voltage reaches the positive threshold V_{TH} at which point the bistable multivibrator will switch to the other stable state in which $v_O = L_-$ and $v_+ = \beta L_-$. The capacitor will then start discharging, and its voltage, v_- , will decrease exponentially toward L_- . This new state will prevail until v_- reaches the negative threshold V_{TL} , at which time the bistable multivibrator switches to the positive-output state, the capacitor begins to charge, and the cycle repeats itself.

12.7 INTEGRATED-CIRCUIT TIMERS

Commercially available integrated-circuit packages exist that contain the bulk of the circuitry needed to implement monostable and astable multivibrators having precise characteristics. In this section we discuss the most popular of such ICs, the **555 timer**. Introduced in 1972 by the Signetics Corporation as a bipolar integrated circuit, the 555 is also available in CMOS technology and from a number of manufacturers.

The 555 Circuit

Figure 12.27 shows a block diagram representation of the 555 timer circuit (for the actual circuit, refer to Grebene 1984). The circuit consists of two comparators, an SR flip-flop, and a transistor Q_1 that operates as a switch. One power supply (V_{CC}) is required for operation, with the supply voltage typically 5 V. A resistive voltage divider, consisting of the three equal-valued resistors labeled R_1 , is connected across V_{CC} and establishes the reference (threshold) voltages for the two comparators. These are $V_{TH} = \frac{2}{3}V_{CC}$ for comparator 1, and $V_{TL} = \frac{1}{3}V_{CC}$ for comparator 2.

We study SR flip-flops in Chapter 13. For our purposes here we note that an SR flip-flop (also called a latch) is a bistable circuit having complementary outputs, denoted Q and $\bar{Q}$. In the *set* state, the output at Q is “high” (approximately equal to V_{CC}) and that at $\bar{Q}$ is “low” (approximately equal to 0 V). In the other stable state, termed the *reset* state, the output at Q is low and that at $\bar{Q}$ is high. The flip-flop is set by applying a high level (V_{CC}) to its set input terminal, labeled S . To reset the flip-flop, a high level is applied to

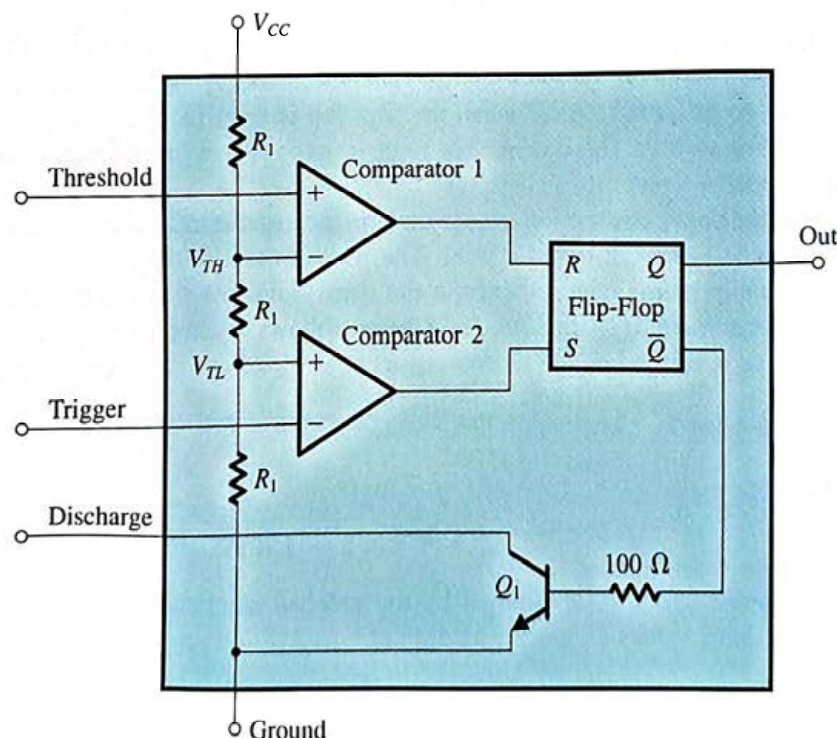


Fig. 12.27 Block diagram representation of the internal circuit of the 555 integrated-circuit timer.

the reset input terminal, labeled R . Note that the reset and set input terminals of the flip-flop in the 555 circuit are connected to the outputs of comparator 1 and comparator 2, respectively.

The positive input terminal of comparator 1 is brought out to an external terminal of the 555 package, labeled Threshold. Similarly, the negative input terminal of comparator 2 is connected to an external terminal labeled Trigger, and the collector of transistor Q_1 is connected to a terminal labeled Discharge. Finally, the Q output of the flip-flop is connected to the output terminal of the timer package, labeled Out.

Implementing a Monostable Multivibrator Using the 555 IC

Figure 12.28(a) shows a monostable multivibrator implemented using the 555 IC together with an external resistor R and an external capacitor C . In the stable state the flip-flop will be in the reset state, and thus its $\bar{Q}$ output will be high, turning on transistor Q_1 . Transistor Q_1 will be saturated, and thus v_C will be close to 0 V, resulting in a low level at the output of comparator 1. The voltage at the trigger input terminal, labeled v_{trigger} , is kept high (greater than V_{TL}), and thus the output of comparator 2 also will be low. Finally, note that since the flip-flop is in the reset state, Q will be low and thus v_O will be close to 0 V.

To trigger the monostable multivibrator, a negative input pulse is applied to the trigger input terminal. As v_{trigger} goes below V_{TL} , the output of comparator 2 goes to the high level, thus setting the flip-flop. Output Q of the flip-flop goes high, and thus v_O goes high, and output $\bar{Q}$ goes low, turning off transistor Q_1 . Capacitor C now begins to charge up through resistor R , and its voltage v_C rises exponentially toward V_{CC} , as shown in Fig. 12.28(b). The monostable multivibrator is now in its quasi-stable state. This state prevails until v_C reaches, and begins to exceed, the threshold of comparator 1, V_{TH} , at which time the output of comparator 1 goes high, resetting the flip-flop. Output $\bar{Q}$ of the flip-flop now goes high and turns on transistor Q_1 . In turn, transistor Q_1 rapidly discharges capacitor C , causing v_C to go to 0 V. Also, when the flip-flop is reset its Q output goes low, and thus v_O goes back to 0 V. The monostable multivibrator is now back in its stable state and is ready to receive a new triggering pulse.

From the above description we see that the monostable multivibrator produces an output pulse v_O as indicated in Fig. 12.28(b). The width of the pulse, T , is the time interval that the monostable multivibrator spends in the quasi-stable state; it can be determined by reference to the waveforms in Fig. 12.28(b) as follows: Denoting the instant at which the trigger pulse is applied as $t = 0$, the exponential waveform of v_C can be expressed as

$$v_C = V_{CC}(1 - e^{-t/CR}) \quad (12.38)$$

Substituting $v_C = V_{TH} = \frac{2}{3}V_{CC}$ at $t = T$ gives

$$T = CR \ln 3 \approx 1.1CR \quad (12.39)$$

Thus the pulse width is determined by the external components C and R , which can be selected to have values as precise as desired.

An Astable Multivibrator Using the 555 IC

Figure 12.29(a) shows the circuit of an astable multivibrator employing a 555 IC, two external resistors, R_A and R_B , and an external capacitor C . To see how the circuit operates

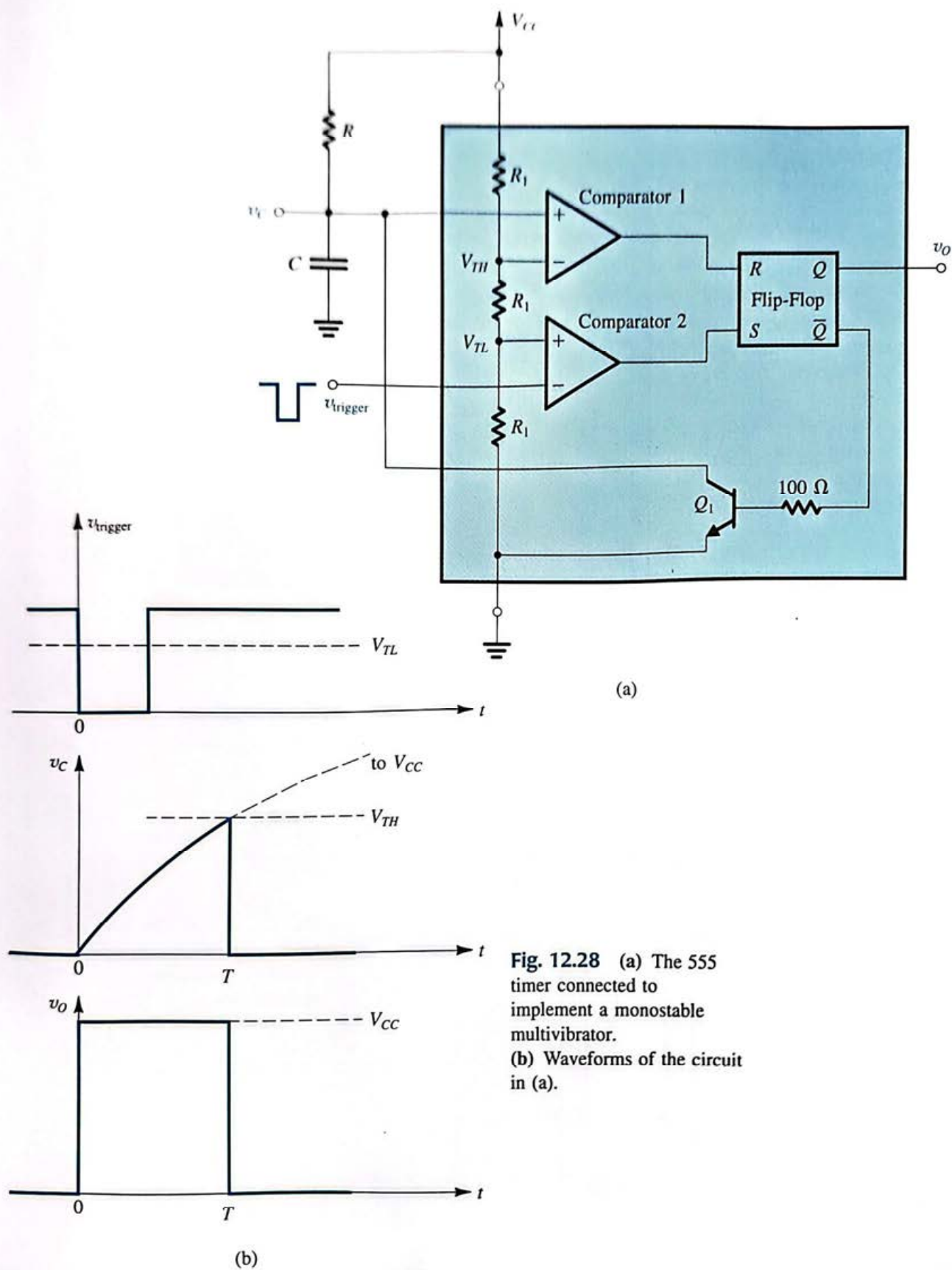
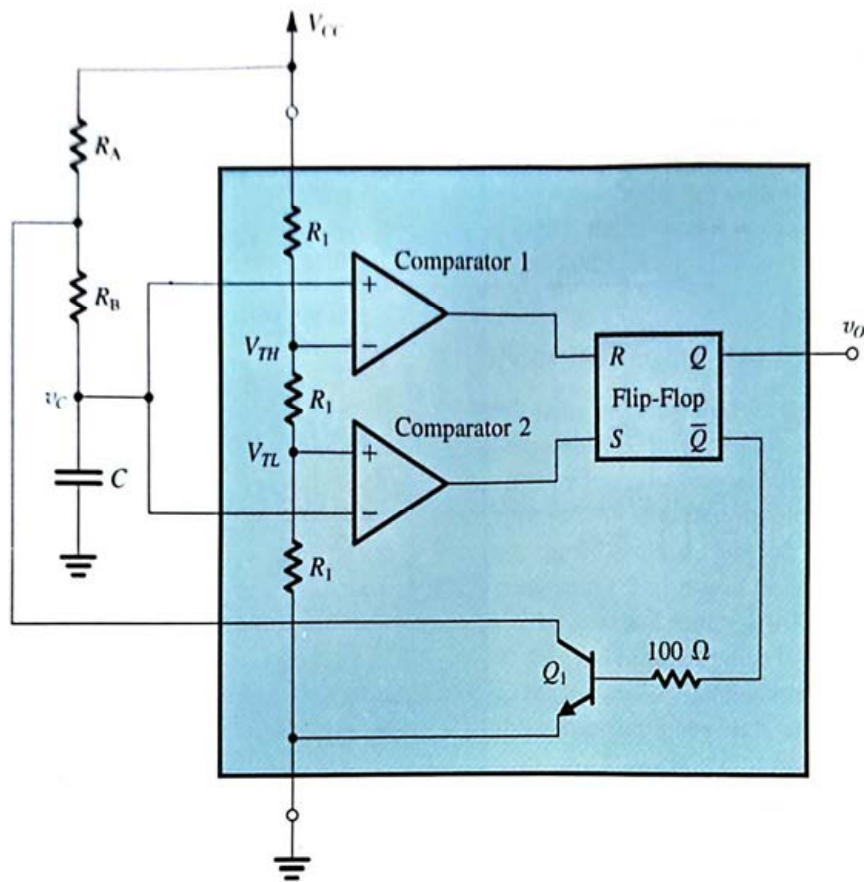
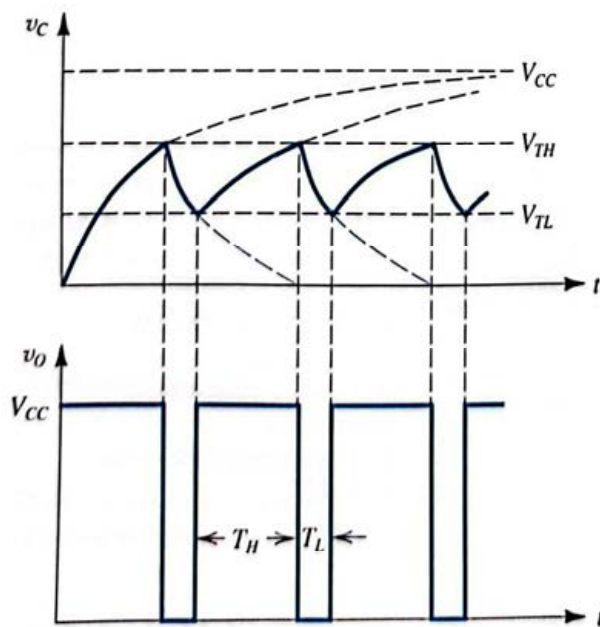


Fig. 12.28 (a) The 555 timer connected to implement a monostable multivibrator. (b) Waveforms of the circuit in (a).



(a)



(b)



Fig. 12.29 (a) The 555 timer connected to implement an astable multivibrator. (b) Waveforms of the circuit in (a).

refer to the waveforms depicted in Fig. 12.29(b). Assume that initially C is discharged and the flip-flop is set. Thus v_O is high and Q_1 is off. Capacitor C will charge up through the series combination of R_A and R_B , and the voltage across it, v_C , will rise exponentially toward V_{CC} . As v_C crosses the level equal to V_{TL} , the output of comparator 2 goes low. This, however, has no effect on the circuit operation, and the flip-flop remains set. Indeed, this state continues until v_C reaches and begins to exceed the threshold of comparator 1, V_{TH} . At this instant of time, the output of comparator 1 goes high and resets the flip-flop. Thus v_O goes low, $\bar{Q}$ goes high, and transistor Q_1 is turned on. The saturated transistor Q_1 causes a voltage of approximately zero volts to appear at the common node of R_A and R_B . Thus C begins to discharge through R_B and the collector of Q_1 . The voltage v_C decreases exponentially with a time constant CR_B toward 0 V. When v_C reaches the threshold of comparator 2, V_{TL} , the output of comparator 2, goes high and sets the flip-flop. The output v_O then goes high, and $\bar{Q}$ goes low, turning off Q_1 . Capacitor C begins to charge through the series equivalent of R_A and R_B , and its voltage rises exponentially toward V_{CC} with a time constant $C(R_A + R_B)$. This rise continues until v_C reaches V_{TH} , at which time the output of comparator 1 goes high, resetting the flip-flop, and the cycle continues.

From the above description we see that the circuit of Fig. 12.29(a) oscillates and produces a square waveform at the output. The frequency of oscillation can be determined as follows. Reference to Fig. 12.29(b) indicates that the output will be high during the interval T_H , in which v_C rises from V_{TL} to V_{TH} . The exponential rise of v_C can be described by

$$v_C = V_{CC} - (V_{CC} - V_{TL})e^{-t/C(R_A+R_B)} \quad (12.40)$$

where $t = 0$ is the instant at which the interval T_H begins. Substituting $v_C = V_{TH} = \frac{2}{3}V_{CC}$ at $t = T_H$ and $V_{TL} = \frac{1}{3}V_{CC}$ results in

$$T_H = C(R_A + R_B) \ln 2 \approx 0.69 C(R_A + R_B) \quad (12.41)$$

We also note from Fig. 12.29(b) that v_O will be low during the interval T_L , in which v_C falls from V_{TH} to V_{TL} . The exponential fall of v_C can be described by

$$v_C = V_{TH} e^{-t/CR_B} \quad (12.42)$$

where we have taken $t = 0$ as the beginning of the interval T_L . Substituting $v_C = V_{TL} = \frac{1}{3}V_{CC}$ at $t = T_L$ and $V_{TH} = \frac{2}{3}V_{CC}$ results in

$$T_L = CR_B \ln 2 \approx 0.69 CR_B \quad (12.43)$$

Equations (12.41) and (12.43) can be combined to obtain the period T of the output square wave as

$$T = T_H + T_L = 0.69 C(R_A + 2R_B) \quad (12.44)$$

Also, the **duty cycle** of the output square wave can be found from Eqs. (12.41) and (12.43):

$$\text{Duty cycle} = \frac{T_H}{T_H + T_L} = \frac{R_A + R_B}{R_A + 2R_B} \quad (12.45)$$

Note that the duty cycle will always be greater than 0.5 (50%); it approaches 0.5 if R_A is selected much smaller than R_B .

the process of designing a digital system using off-the-shelf packages of logic gates. The designer consults data sheets and books to determine the input and output characteristics of the gates, their fan-in and fan-out limitations, and so on. In connecting the gates, the designer needs to adhere to a set of rules specified by the manufacturer in the data sheets. The designer does not need to consider, in a direct way, the circuit inside the gate package. In effect, the circuit has been abstracted in the form of a functional block that can be used as a component. This greatly simplifies system design. The digital-IC designer follows a similar process. Circuit blocks are designed, characterized, and stored in a library as *standard cells*. These cells can then be used by the IC designer to assemble a larger subsystem (e.g., an adder or a multiplier), which in turn is characterized and stored as a functional block to be used in the design of an even larger system.

At every level of design abstraction, the need arises for simulation and other computer programs that help make the design process as automated as possible. Whereas SPICE is employed in circuit simulation, other software tools are utilized at other levels and in other phases of the design process. Although digital-system design and design automation are outside the scope of this book, it is important that the reader appreciate the role of design abstraction and computer aids in digital design. They are what make it humanly possible to design a 10-million-transistor digital IC. Unfortunately, analog IC design does not lend itself to the same level of abstraction and automation. Each analog IC to a large extent has to be “handcrafted.” As a result, the complexity and density of analog ICs remain much less than that possible within a digital IC.

Whatever approach or style is adopted in digital design, some familiarity with the various digital-circuit technologies and design techniques is essential. This chapter and the next aim to provide such a background.

13.2 DESIGN AND PERFORMANCE ANALYSIS OF THE CMOS INVERTER

The CMOS logic inverter was introduced and studied in Section 5.8, which we urge the reader to review before proceeding any further. In this section, we take a more comprehensive look at the inverter, investigating its performance and exploring the trade-offs available in its design. This material will serve as the foundation for the study of CMOS logic circuits in the following section.

Circuit Structure

The inverter circuit, shown in Fig. 13.4(a), consists of a pair of complementary MOSFETs switched by the input voltage v_I . Although not shown, the source of each device is connected to its body, thus eliminating the body effect. Usually, the threshold voltages V_{tn} and V_{tp} are equal in magnitude; that is, $V_{tn} = |V_{tp}| = V_t$, which is in the range of 0.2 to 1 V, with values near the lower end of this range for modern process technologies with small feature size (e.g., with channel length of 0.3–0.5 μm).

The inverter circuit can be represented by a pair of switches operated in a complementary fashion, as shown in Fig. 13.4(b). As indicated, each switch is modeled by a finite on resistance, which is the source–drain resistance of the respective transistor, evaluated near

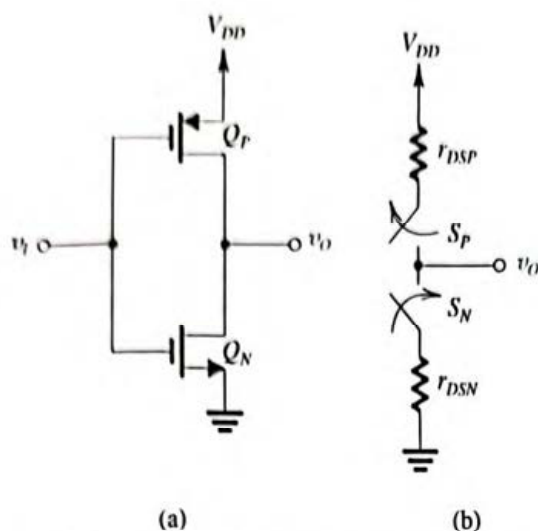


Fig. 13.4 (a) The CMOS inverter and (b) its representation as a pair of switches operated in a complementary fashion.

$$|v_{DS}| = 0,$$

$$r_{DSN} = 1 / \left[k'_n \left(\frac{W}{L} \right)_n (V_{DD} - V_t) \right] \quad (13.6)$$

$$r_{DSP} = 1 / \left[k'_p \left(\frac{W}{L} \right)_p (V_{DD} - V_t) \right] \quad (13.7)$$

Static Operation

With $v_I = 0$, $v_O = V_{OH} = V_{DD}$, and the output node is connected to V_{DD} through the resistance r_{DSP} of the pull-up transistor Q_P . Similarly, with $v_I = V_{DD}$, $v_O = V_{OL} = 0$, and the output node is connected to ground through the resistance r_{DSN} of the pull-down transistor Q_N . Thus, in steady state, no direct-current path exists between V_{DD} and ground, and the static current and the static power dissipation are both zero (leakage effects are usually negligibly small).

The voltage transfer characteristic (VTC) of the inverter is shown in Fig.13.5, from which it is confirmed that the output voltage levels are 0 and V_{DD} , and thus the output voltage swing is the maximum possible. The fact that V_{OL} and V_{OH} are independent of device dimensions makes CMOS very different from other forms of MOS logic (e.g., NMOS circuits utilizing enhancement or depletion load devices, which are based on the amplifier circuits studied in Sections 5.7.4). For these NMOS circuits, V_{OL} depends on the ratio of the transconductance parameters of the devices, that is, on the ratio $\left(k' \frac{W}{L} \right)_{\text{driver}} / \left(k' \frac{W}{L} \right)_{\text{load}}$. Such circuits are therefore known as *ratioed* logic circuits; correspondingly, CMOS is said to belong to the *ratioless* type.

The CMOS inverter can be made to switch at the midpoint of the logic swing, 0 to V_{DD} , that is, at $V_{DD}/2$, by appropriately *sizing the transistors*. Specifically, it can be shown

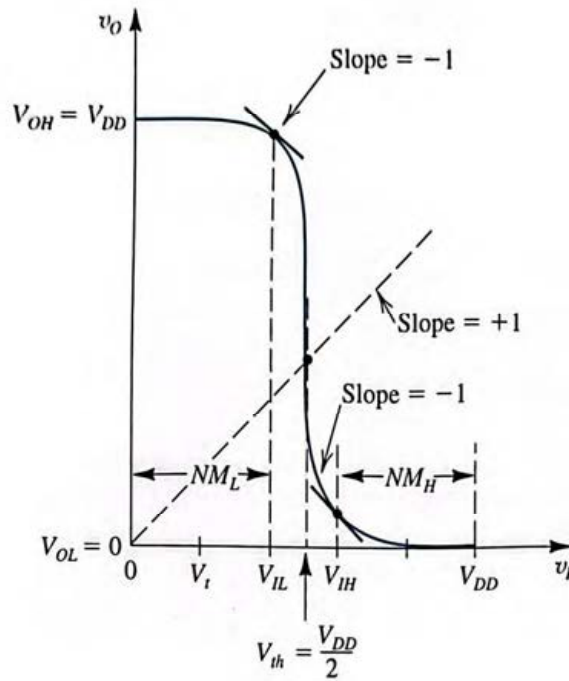


Fig. 13.5 The voltage transfer characteristic (VTC) of the CMOS inverter when Q_N and Q_P are matched.

that the switching threshold is given by

$$V_{th} = \frac{V_{DD} - |V_{tp}| + \sqrt{k_n/k_p} V_{tn}}{1 + \sqrt{k_n/k_p}} \quad (13.8)$$

where $k_n = k'_n(W/L)_n$ and $k_p = k'_p(W/L)_p$, from which we see that for the typical case where $V_{tn} = |V_{tp}|$, $V_{th} = V_{DD}/2$ for $k_n = k_p$, that is

$$k'_n(W/L)_n = k'_p(W/L)_p \quad (13.9)$$

Thus a symmetrical transfer characteristic is obtained when the devices are designed to have equal transconductance parameters, a condition we refer to as *matching*. Since μ_n is two to three times larger than μ_p , matching is achieved by making $(W/L)_p$ two to three times (i.e., μ_n/μ_p times) $(W/L)_n$.

$$\left(\frac{W}{L}\right)_p = \frac{\mu_n}{\mu_p} \left(\frac{W}{L}\right)_n \quad (13.10)$$

Normally, the two devices have the same channel length, L , which is set at the minimum allowable for the given process technology. The minimum width of the NMOS transistor is usually one and a half to two times L , and the width of the PMOS transistor two to three times that. For example, for a 1.2- μm process for which $\mu_n/\mu_p = 3$, $L = 1.2\ \mu\text{m}$, $(W/L)_n = 1.8/1.2$, and $(W/L)_p = 5.4/1.2$. As we shall discuss shortly, if the inverter is required to drive a relatively large capacitive load, the transistors are made wider. However, to conserve chip area, most of the inverters would have this "minimum size." For future purposes, we shall denote the (W/L) ratio of the NMOS transistor of this minimum-size inverter by n and the (W/L) ratio of the PMOS transistor by p . Since the inverter area can be represented by $W_n L_n + W_p L_p = (W_n + W_p)L$, the area of the minimum-size inverter

is $(n + p)L^2$, and we can use the factor $(n + p)$ as proxy for area. For the example cited earlier, $n = 1.5$, $p = 4.5$, and the area factor $n + p = 6$.

Besides placing the gate threshold at the center of the logic swing, matching the transconductance parameters of Q_N and Q_P provides the inverter with equal current-driving capability in both directions (pull-up and pull-down). Furthermore, and obviously related, it makes $r_{DSN} = r_{DSP}$. Thus an inverter with matched transistors will have equal propagation delays, t_{PLH} and t_{PHL} .

When the inverter threshold is at $V_{DD}/2$, the noise margins NM_H and NM_L are equalized and their values are maximized, such that:

$$NM_H = NM_L = \frac{3}{8} \left(V_{DD} + \frac{2}{3} V_t \right) \quad (13.11)$$

Since typically $V_t = 0.1$ to $0.2 V_{DD}$, the noise margins are approximately $0.4 V_{DD}$. This value, being close to half the power supply voltage, makes the CMOS inverter nearly ideal from a noise-immunity standpoint. Further, since the inverter dc input current is practically zero, the noise margins are not dependent on the gate fan-out.

Although we have emphasized the advantages of matching Q_N and Q_P , there are occasions in which this scaling is not adopted. One might, for instance, forego the advantages of matching in return for reducing chip area, and simply make $(W/L)_p = (W/L)_n$. There are also instances in which a deliberate mismatch is used so as to place V_{th} at a specified value other than $V_{DD}/2$. Note that by making $k_n > k_p$, V_{th} moves closer to zero, whereas $k_p > k_n$ moves V_{th} closer to V_{DD} .

As a final comment on the inverter VTC, we note that the slope in the transition region, though large, is finite and is given by $-(g_{mN} + g_{mP})(r_{oN} // r_{oP})$.

Dynamic Operation

The propagation delay of the inverter is usually determined under the condition that it is driving an identical inverter. This situation is depicted in Fig. 13.6. We wish to analyze this circuit to determine the propagation delay of the inverter comprising Q_1 and Q_2 , which is driven by a low-impedance source v_i , and is loaded by the inverter comprising Q_3 and Q_4 . Indicated in the figure are the various transistor internal capacitances that are connected to the output node of the (Q_1, Q_2) inverter. Obviously, an exact pencil-and-paper analysis of this circuit will be too complicated to yield useful design insight, and a simplification of the circuit is in order. Specifically, we wish to replace all the capacitances attached to the inverter output node with a single capacitance C connected between the output node and ground. If we are able to do that, we can utilize the results of the transient analysis performed in Section 5.8. Toward that end, we note that during t_{PLH} or t_{PHL} , the output of the first inverter changes from 0 to $V_{DD}/2$ or from $V_{DD}/2$ to 0, respectively. It follows that the second inverter remains in the same state during each of our analysis intervals. This observation will have an important bearing on our estimation of the equivalent input capacitance of the second inverter. Let's now consider the contribution of each of the capacitances in Fig. 13.6 to the value of the equivalent load capacitance C :

1. The gate-drain overlap capacitance of Q_1 , C_{gd1} , can be replaced by an equivalent capacitance between the output node and ground of $2C_{gd1}$. The factor 2 arises because of the Miller effect (Section 7.4). Specifically, note that as v_i goes high

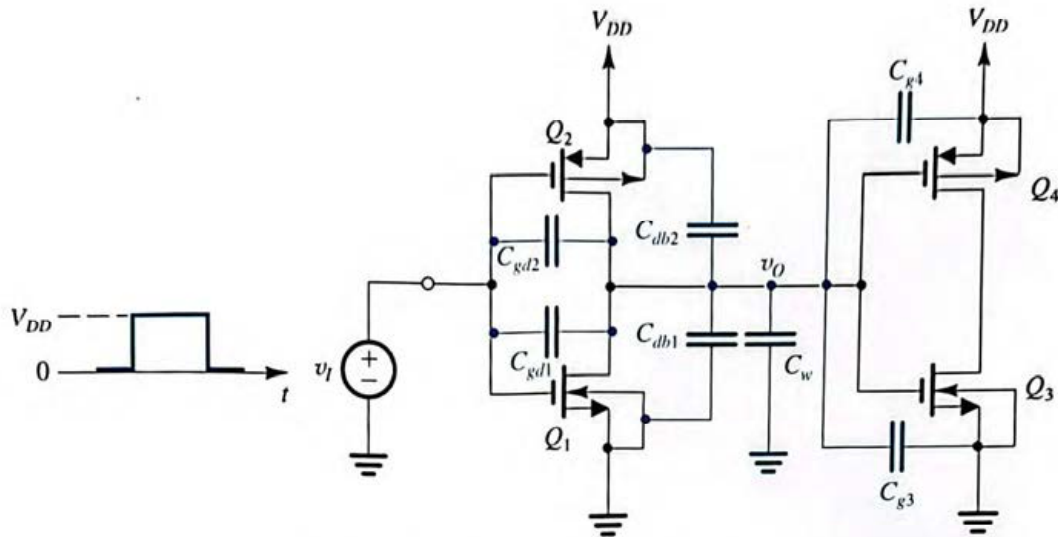


Fig. 13.6 Circuit for analyzing the propagation delay of the inverter. Here, the inverter under study is formed by Q_1 and Q_2 . It is driving an identical inverter formed by Q_3 and Q_4 .

and v_O goes low by the same amount, the change in voltage across C_{gd1} is twice that amount. Thus the output node sees in effect twice the value of C_{gd1} . The same applies for the gate-drain overlap capacitance of Q_2 , C_{gd2} , which can be replaced by a capacitance $2C_{gd2}$ between the output node and ground.

- Each of the drain-body capacitances C_{db1} and C_{db2} has a terminal at a constant voltage. Thus for the purpose of our analysis here, C_{db1} and C_{db2} can be replaced with equal capacitances between the output node and ground. Note, however, that the formulas given in Section 5.10 for calculating C_{db1} and C_{db2} are small-signal relationships, whereas the analysis here is obviously a large-signal one. A technique has been developed for finding equivalent large-signal values for C_{db1} and C_{db2} [see Hodges and Jackson (1988), and Rabaey (1996)].
- Since the second inverter does not switch states, we will assume that the input capacitances of Q_3 and Q_4 remain approximately constant and equal to the total gate capacitance WLC_{ox} . That is, the input capacitance of the load inverter will be

$$C_{g3} + C_{g4} = (WL)_3 C_{ox} + (WL)_4 C_{ox}$$

- The last component of C is the wiring capacitance C_w , which simply adds to the value of C .

Thus, the total value of C is given by

$$C = 2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2} + C_{g3} + C_{g4} + C_w \quad (13.12)$$

Having determined an approximate value for the equivalent capacitance between the inverter output node and ground, we can utilize the circuits in Figs. 13.7(a) and 13.7(b) to determine t_{PHL} and t_{PLH} , respectively. Since the two circuits are similar, we need only consider one and apply the result directly to the other. Consider the circuit in Fig. 13.7(a), which applies when v_I goes high and Q_N discharges C from its initial voltage of V_{DD} to the final value

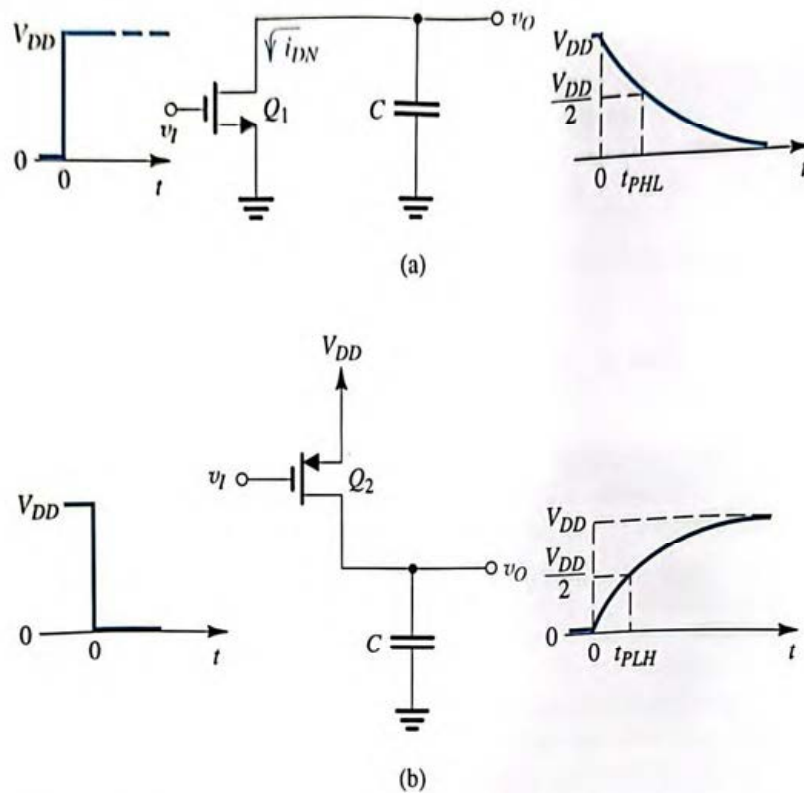


Fig. 13.7 Equivalent circuits for determining the propagation delays (a) t_{PHL} and (b) t_{PLH} of the inverter.

of 0. The analysis is somewhat complicated by the fact that initially Q_N will be in the saturation mode and then, when v_O falls below $V_{DD} - V_t$, it will go into the triode region of operation. We have in fact performed this analysis in Section 5.8 and obtained the following approximate expression for t_{PHL} :

$$t_{PHL} = \frac{1.6C}{k'_n \left(\frac{W}{L}\right)_n V_{DD}} \quad (13.13)$$

where we have assumed that $V_t \approx 0.2 V_{DD}$, which is typically the case.

There is an alternative, an approximate but simpler, method for analyzing the circuit in Fig. 13.7(a). It is based on computing an average value for the discharge current i_{DN} during the interval $t = 0$ to $t = t_{PHL}$. Specifically, at $t = 0$, Q_N will be saturated, and $i_{DN}(0)$ is given by

$$i_{DN}(0) = \frac{1}{2} k'_n \left(\frac{W}{L}\right)_n (V_{DD} - V_t)^2 \quad (13.14)$$

At $t = t_{PHL}$, Q_N will be in the triode region, and $i_{DN}(t_{PHL})$ will be

$$i_{DN}(t_{PHL}) = k'_n \left(\frac{W}{L}\right)_n \left[(V_{DD} - V_t) \frac{V_{DD}}{2} - \frac{1}{2} \left(\frac{V_{DD}}{2}\right)^2 \right] \quad (13.15)$$

The average discharge current can then be found as

$$i_{DN}|_{av} = \frac{1}{2}[i_{DN}(0) + i_{DN}(t_{PHL})] \quad (13.16)$$

and the discharge interval t_{PHL} computed from

$$t_{PHL} = \frac{C \Delta V}{i_{DN}|_{av}} = \frac{CV_{DD}/2}{i_{DN}|_{av}} \quad (13.17)$$

Utilizing Eqs. (13.14) through (13.17) and substituting $V_i \cong 0.2 V_{DD}$ gives

$$t_{PHL} \cong \frac{1.7 C}{k'_n \left(\frac{W}{L}\right)_n V_{DD}} \quad (13.18)$$

which yields a value very close to that obtained by the more precise formula of Eq. (13.13). Which formula to use is not very relevant, for we have already made many approximations. Indeed, our interest in these formulas is not in obtaining a precise value of t_{PHL} but in what they tell us about the effect of the various elements on determining the inverter delay. It is such insight that the circuit designer hopes to glean from manual analysis. Precise values for delay can be determined using computer simulation (Section 13.13).

An expression for the low-to-high inverter delay, t_{PLH} , can be written by analogy to the t_{PHL} expression in Eq. (13.17),

$$t_{PLH} \cong \frac{1.7 C}{k'_p \left(\frac{W}{L}\right)_p V_{DD}} \quad (13.19)$$

Finally, the propagation delay t_P can be found as the average of t_{PHL} and t_{PLH} ,

$$t_P = \frac{1}{2}(t_{PHL} + t_{PLH})$$

Examination of the formulas in Eqs. (13.18) and (13.19) enables us to make a number of useful observations:

1. As expected, the two components of t_P can be equalized by selecting the (W/L) ratios so as to equalize k_n and k_p , that is, by matching Q_N and Q_P .
2. Since t_P is proportional to C , the designer should strive to reduce C . This is achieved by using the minimum possible channel length and by minimizing wiring and other parasitic capacitances. Careful layout of the chip can result in significant reduction in such capacitances and in the value of C_{db} .
3. Using a process technology with larger transconductance parameter k' can result in shorter propagation delays. Keep in mind, however, that for such processes C_{ox} is increased, and thus the value of C increases at the same time.
4. Using larger (W/L) ratios can result in a reduction in t_P . Care, however, should be exercised here since increasing the size of the devices increases the value of C , and

thus the expected reduction in t_P might not materialize. Reducing t_P by increasing (W/L), however, is an effective strategy in situations where C is dominated by components not directly related to the size of the driving device.

5. A larger supply voltage V_{DD} results in a lower t_P . However, V_{DD} is determined by the process technology and thus is often not under the control of the designer. Furthermore, modern process technologies in which device sizes are reduced require lower V_{DD} . At the time of this writing (1997), a new standard value for V_{DD} has emerged, namely, 3.3 V (or 3.0 V) replacing the 5-V standard of the past many years. A motivating factor for lowering V_{DD} is the need to keep the dynamic power dissipation at acceptable levels, especially in very-high-density chips. We will have more to say on this point shortly.

These observations clearly illustrate the conflicting requirements and the trade-offs available in the design of a CMOS digital integrated circuit (and indeed in any engineering design problem).

Dynamic Power Dissipation

The negligible static power dissipation of CMOS has been a significant factor in motivating its replacing NMOS as the technology of choice in implementing high-density VLSI circuits. However, as the number of gates per chip steadily increases, the dynamic power dissipation has become a serious issue. The dynamic power dissipated in the CMOS inverter is given by Eq. (13.4), which we repeat here as

$$P_D = fCV_{DD}^2 \quad (13.20)$$

where f is the frequency at which the gate is switched. It follows that minimizing C is an effective means for reducing dynamic power dissipation. An even more effective strategy is the use of a lower power supply voltage. As we mentioned, new CMOS process technologies utilize V_{DD} of 3.3 V. In fact, some recently reported designs employ V_{DD} of 2–2.5 V internal to the chip while keeping the external voltage at the 3.3-V standard value. These newer chips, however, pack much more circuitry on the chip (as many as 10 million transistors) and operate at higher frequencies (microprocessor clock frequencies as high as 500 MHz have recently been reported). The dynamic power dissipation of such high-density chips can be in the range of tens of watts.

EXAMPLE 13.1

Consider a CMOS inverter fabricated in a process for which $C_{ox} = 0.9 \text{ fF}/\mu\text{m}^2$, $\mu_n C_{ox} = 50 \mu\text{A}/\text{V}^2$, $\mu_p C_{ox} = 20 \mu\text{A}/\text{V}^2$, $V_{in} = -V_{ip} = 1 \text{ V}$, and $V_{DD} = 5 \text{ V}$. The W/L ratio of Q_N is $4 \mu\text{m}/2 \mu\text{m}$, and that for Q_P is $10 \mu\text{m}/2 \mu\text{m}$. The gate-drain overlap capacitance is specified to be $0.5 \text{ fF}/\mu\text{m}$ of gate width. Further, the effective value of drain-body capacitances are $C_{dbn} = 10 \text{ fF}$ and $C_{dbp} = 15 \text{ fF}$. The wiring capacitance $C_w = 5 \text{ fF}$. Find t_{PHL} , t_{PLH} and t_P .

SOLUTION

First, we determine the value of the equivalent capacitance C using Eq. (13.12),

$$C = 2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2} + C_{g3} + C_{g4} + C_w$$

where

$$C_{gd1} = 0.5 \times W_n = 0.5 \times 4 = 2 \text{ fF}$$

$$C_{gd2} = 0.5 \times W_p = 0.5 \times 10 = 5 \text{ fF}$$

$$C_{db1} = 10 \text{ fF}$$

$$C_{db2} = 15 \text{ fF}$$

$$C_{g3} = W_n LC_{ox} = 4 \times 2 \times 0.9 = 7.2 \text{ fF}$$

$$C_{g4} = W_p LC_{ox} = 10 \times 2 \times 0.9 = 18 \text{ fF}$$

$$C_w = 5 \text{ fF}$$

Thus,

$$C = 2 \times 2 + 2 \times 5 + 10 + 15 + 7.2 + 18 + 5 = 69.2 \text{ fF}$$

Next, although we can use the formula in Eq. (13.18) to determine t_{PHL} , we shall take an alternative route. Specifically, we shall consider the discharge of C through Q_N and determine the average discharge current using Eqs. (13.14) through (13.16):

$$\begin{aligned} i_{DN}(0) &= \frac{1}{2} k'_n \left(\frac{W}{L} \right)_n (V_{DD} - V_t)^2 \\ &= \frac{1}{2} \times 50 \left(\frac{4}{2} \right) (5 - 1)^2 = 800 \mu\text{A} \end{aligned}$$

$$\begin{aligned} i_{DN}(t_{PHL}) &= k'_n \left(\frac{W}{L} \right)_n \left[(V_{DD} - V_t) \frac{V_{DD}}{2} - \frac{1}{2} \left(\frac{V_{DD}}{2} \right)^2 \right] \\ &= 50 \times \frac{4}{2} \left[(5 - 1) \frac{5}{2} - \frac{1}{2} \left(\frac{5}{2} \right)^2 \right] \\ &= 687.5 \mu\text{A} \end{aligned}$$

Thus

$$i_{DN}|_{av} = \frac{800 + 687.5}{2} = 744 \mu\text{A}$$

and

$$t_{PHL} = \frac{C(V_{DD}/2)}{i_{DN}|_{av}} = \frac{69.2 \times 10^{-15} \times 2.5}{744 \times 10^{-6}} = 233 \text{ ps}$$

Since $\frac{W_p}{W_n} = 2.5 = \frac{\mu_n}{\mu_p}$, the inverter is matched and will have equal propagation delays in both directions, thus

$$t_{PLH} = 233 \text{ ps}$$

$$t_p = \frac{1}{2}(t_{PHL} + t_{PLH}) = 233 \text{ ps}$$

Finally, we note that an identical value would have been obtained had we used the formula in Eq. (13.18) and a slightly lower value (221 ps) would have resulted by using the formula in Eq. (13.13).

Exercises

13.1 Consider the inverter specified in Example 13.1 when loaded with an additional 0.1-pF capacitance. What will the propagation delay become?

Ans. 570 ps

13.2 In an attempt to decrease the area of the inverter in Example 13.1, $(W/L)_p$ is made equal to $(W/L)_n$. What is the percentage reduction in area achieved? Find the new values of C , t_{PHL} , t_{PLH} , and t_p . Assume that C_{dbp} reduces to 10 fF.

Ans. 43%; 47.4 fF; 159 ps; 398 ps; 279 ps

13.3 For the inverter of Example 13.1, find the dynamic power dissipation when clocked at a 100-MHz rate.

Ans. 173 μ W

13.3 CMOS LOGIC-GATE CIRCUITS

In this section, we build on our knowledge of inverter design and consider the design of CMOS circuits that realize combinational logic functions. In combinational circuits, the output at any time is a function only of the values of input signals at that time. Thus, these circuits do not have memory and do not employ feedback. Combinational logic circuits are used in large quantities in a multitude of applications; indeed, every digital system contains large numbers of combinational logic circuits.

Basic Structure

A CMOS logic circuit is in effect an extension, or a generalization, of the CMOS inverter: The inverter consists of an NMOS pull-down transistor, and a PMOS pull-up transistor, operated by the input voltage in a complementary fashion. The CMOS logic gate consists of two networks: the pull-down network (PDN) constructed of NMOS transistors, and the pull-up network (PUN) constructed of PMOS transistors (see Fig. 13.8). The two networks are operated by the input variables, in a complementary fashion. Thus, for the three-input