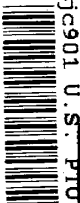


08/12/02



Please type a plus sign (+) inside this box ➔ +

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

PTO/SB/05 (03-01)

Approved for use through 10/31/2002 OMB 0651-0032

U.S. Patent and Trademark Office U.S. DEPARTMENT OF COMMERCE

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 3771P003

First Inventor Daniel E. Grupp, et al.

Title Method For Depinning The Fermi Level of a Semiconductor at an Electrical

Express Mail Label No. EV060610698US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☐ Applicant claims small entity status.
See 37 CFR 1.27.
3. ☒ Specification [Total Pages 42]
(preferred arrangement set forth below)
 - Descriptive title of the Invention
 - Cross References to Related Applications
 - Statement Regarding Fed sponsored R & D
 - Reference to sequence listing, a table, or a computer program listing appendix
 - Background of the Invention
 - Brief Summary of the Invention
 - Brief Description of the Drawings (if filed)
 - Detailed Description
 - Claim(s)
 - Abstract of the Disclosure
4. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 6]
5. Oath or Declaration (signed) [Total Pages 5]
 - a. ☐ Newly executed (original or copy)
 - b. ☐ Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 18 completed)
 - i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
6. ☐ Application Data Sheet. See 37 CFR 1.76
7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix)
8. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all of the following are necessary)
 - a. ☐ Computer Readable Form (CRF)
 - b. Specification Sequence Listing on:
 - i. ☐ CD-ROM or CD-R (2 copies); or
 - ii. ☐ paper
 - c. ☐ Statements verifying identity of above copies
9. ☒ Assignment Papers (cover sheet & document(s))
10. ☐ 37 C.F.R. § 3.73(b) Statement ☒ Power of Attorney
(when there is an assignee)
11. ☐ English Translation Document (if applicable)
12. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
13. ☐ Preliminary Amendment
14. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
15. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16. ☒ Nonpublication Request under 35 U.S.C. 122 (b)(2)(B)(i).
Applicant must attach form PTO/SB/35 or its equivalent.
17. ☐ Other: _____

18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP)

of prior application No: _____

Prior application Information: Examiner _____

Group/Art Unit: _____

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

18. CORRESPONDENCE ADDRESS

☒ Customer Number or Bar Code Label

08791

or ☒ Correspondence address below

Name	Tarek N. Fahmi				
	Blakely, Sokoloff, Taylor & Zafman LLP				
Address	12400 Wilshire Boulevard, Seventh Floor				
City	Los Angeles	State	California	Zip Code	90025-1030
Country	USA	Telephone	(408) 947-8200	Fax	(408) 947-8280

Name (Print/Type)	Tarek N. Fahmi	Registration No. (Attorney/Agent)	41,402
Signature		Date	08/12/02

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

FEE TRANSMITTAL FOR FY 2002

TOTAL AMOUNT OF PAYMENT (\$) \$1,938.00

Complete if Known:

Application No. Not Yet Assigned
Filing Date Herewith
First Named Inventor Daneil E. Grupp
Group Art Unit Not Yet Assigned
Examiner Name Not Yet Assigned
Attorney Docket No. 3771P003

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number 02-2666
Deposit Account Name _____

- ☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

- ☐ Applicant claims small entity status. See 37 CFR 1.27

2. ☒ Payment Enclosed: ☒ Check
Money Order
Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
101	740	201	370	Utility application filing fee	<u>\$740.00</u>
106	330	206	165	Design application filing fee	_____
107	510	207	255	Plant filing fee	_____
108	740	208	370	Reissue filing fee	_____
114	160	214	80	Provisional application filing fee	_____
SUBTOTAL (1)					<u>\$ 740.00</u>

2. EXTRA CLAIM FEES

			Extra Claims	Fee from below	Fee Paid
Total Claims	<u>61</u>	- 20** =	<u>41</u>	X \$18 =	<u>\$738</u>
Independent Claims	<u>8</u>	- 3** =	<u>5</u>	X \$84 =	<u>\$420</u>
Multiple Dependent					

**Or number previously paid, if greater; For Reissues, see below.

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
103	18	203	9	Claims in excess of 20	_____
102	84	202	42	Independent claims in excess of 3	_____
104	280	204	140	Multiple dependent claim, if not paid	_____
109	84	209	42	**Reissue independent claims over original patent	_____
110	18	210	9	**Reissue claims in excess of 20 and over original patent	_____
SUBTOTAL (2)					<u>\$ 1,158.00</u>

10/04/01

FEE CALCULATION (continued)

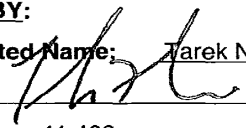
3. ADDITIONAL FEES

<u>Large Entity</u>		<u>Small Entity</u>		<u>Fee Description</u>	<u>Fee Paid</u>
<u>Code</u>	<u>Fee (\$)</u>	<u>Code</u>	<u>Fee (\$)</u>		
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for ex parte reexamination	
099	8,800	099	8,800	Request for inter parties reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	920	217	460	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifth month	
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,280	241	640	Petition to revive - unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CFR 1.17(q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	\$40
146	740	246	370	For filing a submission after final rejection (see 37 CFR 1.129(a))	
148	110	248	55	Statutory Disclaimer	
149	740	249	370	For each additional invention to be examined (see 37 CFR 1.129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	
195	300	195	300	Publication fee for early, voluntary, or normal pub.	
196	300	196	300	Publication fee for republication	
194	130	194	130	Request for voluntary publication or republication	
098	130	098	130	Processing fee under 37 CFR 1.17(i) (except provisionals)	
091	1,280	091	1,280	Acceptance of unintentionally delayed claim for priority	
Other fee (specify) _____					
Other fee (specify) _____					
SUBTOTAL (3)					\$ 40.00

*Reduced by Basic Filing Fee Paid

SUBMITTED BY:

Typed or Printed Name: Tarek N. Fahmi

Signature:  Date: August 12, 2002

Reg. Number: 41,402 Telephone Number: 408.947.8200

PTO/SB/35 (11-00)
 Approved for use through 10/31/2002 OMB 0651-0031
 Patent and Trademark Office U.S. DEPARTMENT OF COMMERCE
 Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

NONPUBLICATION REQUEST UNDER 35 U.S.C. 122(b)(2)(B)(i)	First Named Inventor	Daniel E. Grupp
	Title	Method For Depinning The Fermi Level of a Semiconductor at an Electrical Junction and
	Attorney Docket Number	3771P003

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing.

I hereby request that the attached application not be published under 35 U.S.C. 122(b).

08/12/02

Date



Signature

Tarek N. Fahmi, Reg. No. 41,402

Typed or printed name

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing**.

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 112(b)(2)(B)(iii)).**

Burden Hour Statement This collection of information is required by 37 CFR 1.213(a). This information is used by the public to request that an application not be published under 35 U.S.C. 122(b) (and the PTO to process that request). Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This form is estimated to take 6 minutes to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO Assistant Commissioner for Patents, Washington, DC 20231

Attorney Docket No.: 03771P003

Patent Application

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**METHOD FOR DEPINNING THE FERMIL LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL
JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS**

INVENTORS

**DANIEL E. GRUPP
DANIEL J. CONNELLY**

Prepared by

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1026
408-947-8200

EXPRESS MAIL CERTIFICATE OF MAILING

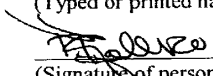
"Express Mail" mailing label number: EV060610698US

Date of Deposit: August 12, 2002

I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Commissioner of Patents and Trademarks, Washington, D. C. 20231

Patricia A. Balero

(Typed or printed name of person mailing paper or fee)



(Signature of person mailing paper or fee)

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

RELATED APPLICATIONS

[0001] The present application is related to co-pending U.S. Patent Application No._____, entitled "INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL", filed on_____, 2002, by the present inventors and assigned to the same assignee as the present application. This related patent application is hereby incorporated by reference in its entirety.

FIELD OF THE INVENTION

[0002] The invention relates generally to semiconductor processing and semiconductor devices. More particularly, the invention relates to a process for depinning the Fermi level of a semiconductor at a metal-interface layer-semiconductor junction and to devices that employ such a junction.

BACKGROUND

[0003] One of the most basic electrical junctions used in modern devices is the metal-semiconductor junction. In these junctions, a metal (such as aluminum) is brought in contact with a semiconductor (such as silicon). This forms a device (a diode) which can be inherently rectifying; that is, the junction will tend to conduct current in one direction more favorably than in the other direction. In other cases, depending on the materials used, the junction may be ohmic in nature (i.e., the contact may have negligible resistance regardless of the direction of current flow). Grondahl and Geiger first studied the rectifying form of these junctions in

1926, and by 1938 Schottky had developed a theoretical explanation for the rectification that was observed.

[0004] Schottky's theory explained the rectifying behavior of a metal-semiconductor contact as depending on a barrier at the surface of contact between the metal and the semiconductor. In this model, the height of the barrier (as measured by the potential necessary for an electron to pass from the metal to the semiconductor) was postulated as the difference between the work function of the metal (the work function is the energy required to free an electron at the Fermi level of the metal, the Fermi level being the highest occupied energy state of the metal at $T = 0$) and the electron affinity of the semiconductor (the electron affinity is the difference between the energy of a free electron and the conduction band edge of the semiconductor). Expressed mathematically:

$$\phi_B = \phi_M - \chi_S \quad [1]$$

where Φ_B is the barrier height, Φ_M is the work function of the metal and χ_S is the electron affinity of the semiconductor.

[0005] Not surprisingly, many attempts were made to verify this theory experimentally. If the theory is correct, one should be able to observe direct variations in barrier heights for metals of different work functions when put in contact with a common semiconductor. What is observed, however, is not direct scaling, but instead only a much weaker variation of barrier height with work function than implied by the model.

[0006] Bardeen sought to explain this difference between theoretical prediction and experimental observation by introducing the concept that surface states of the semiconductor play a role in determining the barrier height. Surface states are energy states (within the bandgap between the valence and conduction bands) at the edge of the semiconductor crystal that arise from incomplete covalent bonds, impurities, and other effects of crystal termination.

Figure 1 shows a cross-section of an un-passivated silicon surface labeled 100. The particular silicon surface shown is an Si(100) 2x1 surface. As shown, the silicon atoms at the surface, such as atom 110, are not fully coordinated and contain un-satisfied dangling bonds, such as

dangling bond 120. These dangling bonds may be responsible for surface states that trap electrical charges.

[0007] Bardeen's model assumes that surface states are sufficient to pin the Fermi level in the semiconductor at a point between the valence and conduction bands. If true, the barrier height at a metal-semiconductor junction should be independent of the metal's work function. This condition is rarely observed experimentally, however, and so Bardeen's model (like Schottky's) is best considered as a limiting case.

[0008] For many years, the cause underlying the Fermi level pinning of the semiconductor at a metal-semiconductor junction remained unexplained. Indeed, to this day no one explanation satisfies all experimental observations regarding such junctions. Nevertheless, in 1984, Tersoff proposed a model that goes a long way towards explaining the physics of such junctions. See J. Tersoff, "Schottky Barrier Heights and the Continuum of Gap States," Phys. Rev. Lett. 52 (6), Feb. 6, 1984.

[0009] Tersoff's model (which is built on work by Heine and Flores & Tejedor, and see also Louie, Chelikowsky, and Cohen, "Ionicity and the theory of Schottky barriers," Phys. Rev. B 15, 2154 (1977)) proposes that the Fermi level of a semiconductor at a metal-semiconductor interface is pinned near an effective "gap center", which is related to the bulk semiconductor energy band structure. The pinning is due to so-called metal induced gap states (MIGS), which are energy states in the bandgap of the semiconductor that become populated due to the proximity of the metal. That is, the wave functions of the electrons in the metal do not terminate abruptly at the surface of the metal, but rather decay in proportion to the distance from that surface (i.e., extending inside the semiconductor). To maintain the sum rule on the density of states in the semiconductor, electrons near the surface occupy energy states in the gap derived from the valence band such that the density of states in the valence band is reduced. To maintain charge neutrality, the highest occupied state (which defines the Fermi level of the semiconductor) will then lie at the crossover point from states derived from the valence band to those derived from the conduction band. This crossover occurs at the branch

point of the band structure. Although calculations of barrier heights based on Tersoff's model do not satisfy all experimentally observed barrier heights for all metal-semiconductor junctions, there is generally good agreement for a number of such junctions.

[0010] One final source of surface effects on diode characteristics is inhomogeneity. That is, if factors affecting the barrier height (e.g., density of surface states) vary across the plane of the junction, the resulting properties of the junction are found not to be a linear combination of the properties of the different regions. In summary then, a classic metal-semiconductor junction is characterized by a Schottky barrier, the properties of which (e.g., barrier height) depend on surface states, MIGS and inhomogeneities.

[0011] The importance of the barrier height at a metal-semiconductor interface is that it determines the electrical properties of the junction. Thus, if one were able to control or adjust the barrier height of a metal-semiconductor junction, one could produce electrical devices of desired characteristics. Such barrier height tuning may become even more important as device sizes shrink even further. Before one can tune the barrier height, however, one must depin the Fermi level of the semiconductor. As discussed in detail below, the present inventors have achieved this goal in a device that still permits substantial current flow between the metal and the semiconductor.

SUMMARY OF THE INVENTION

[0012] The present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal – interface layer – semiconductor junction, there exist corresponding minimum specific contact resistances. The interface layer thickness corresponding to this minimum specific contact resistance will vary depending upon the materials used, however, it is a thickness that allows for depinning the Fermi level of the semiconductor while still permitting current to flow between the metal and the semiconductor when the junction is biased (e.g., forward or reverse biased). By depinning the Fermi level, the present inventors mean a condition wherein all, or substantially all, dangling bonds that may otherwise be present at the semiconductor surface have been terminated, and the effect of MIGS has been overcome, or at least reduced, by displacing the semiconductor a sufficient distance from the metal. Minimum specific contact resistances of less than or equal to approximately $10 \Omega - \mu m^2$ or even less than or equal to approximately $1 \Omega - \mu m^2$ may be achieved for such junctions in accordance with the present invention.

[0013] Thus, in one embodiment, the present invention provides an electrical device in which an interface layer is disposed between and in contact with a metal and a silicon-based semiconductor and is configured to depin the Fermi level of the semiconductor while still permitting current flow between the metal and the semiconductor when the electrical device is biased. The specific contact resistance of the electrical device is less than approximately $10 \Omega - \mu m^2$. The interface layer may include a passivating material (e.g., a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride) and sometimes also includes a separation layer. In some cases, the interface layer may be essentially a monolayer (or several monolayers) of a semiconductor passivating material.

[0014] In another embodiment, the interface layer is made up of a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material, for example ammonia

(NH₃), nitrogen (N₂) or unbound gaseous nitrogen (N) generated from a plasma process. In such cases, the interface layer may be fabricated by heating the semiconductor while in a vacuum chamber and exposing the semiconductor to the nitrogenous material.

[0015] A further embodiment of the present invention provides for depinning the Fermi level of a semiconductor in an electrical junction through the use of an interface layer disposed between a surface of the semiconductor and a conductor. The interface layer preferably (i) is of a thickness sufficient to reduce effects of MIGS in the semiconductor, and (ii) passivates the surface of the semiconductor. Despite the presence of the interface layer, significant current may flow between the conductor and the semiconductor because the thickness of the interface layer may be chosen to provide a minimum (or near minimum) specific contact resistance for the junction. As indicated above, the interface layer may include a passivating material such as a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride.

[0016] Further embodiments of the present invention provide a junction between a semiconductor and a conductor separated from the semiconductor by an interface layer configured to allow a Fermi level of the conductor to (i) align with a conduction band of the semiconductor, (ii) align with a valence band of the semiconductor, or (iii) to be independent of the Fermi level of the semiconductor. In some or all of these cases, current may flow between the conductor and the semiconductor when the junction is biased because the interface layer has a thickness corresponding to a minimum or near minimum specific contact resistance for the junction. For example, specific contact resistances of less than or equal to approximately 2500 $\Omega-\mu m^2$, 1000 $\Omega-\mu m^2$, 100 $\Omega-\mu m^2$, 50 $\Omega-\mu m^2$, 10 $\Omega-\mu m^2$ or even less than or equal to 1 $\Omega-\mu m^2$ may be achieved.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0017] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0018] **Figure 1** shows a cross-section of an un-passivated silicon surface containing surface silicon atoms with dangling bonds.

[0019] **Figure 2** illustrates various energy levels for metals and semiconductors and is labeled to show the work function of a metal and the electron affinity of a semiconductor.

[0020] **Figure 3** shows an energy band diagram for a conventional metal – *n*-type semiconductor junction and also illustrates the concept of a depletion region formed in the semiconductor when the materials are brought into contact with one another.

[0021] **Figure 4** illustrates band bending at a conventional metal – *n*-type semiconductor junction.

[0022] **Figure 5** shows a semiconductor device containing a semiconductor material having a surface across which electrical current flows during operation of the semiconductor device, and containing an interface layer formed on the surface according to one embodiment of the present invention.

[0023] **Figure 6** shows an electrical junction containing an interface layer that is disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

[0024] **Figures 7a, 7b, 7c and 7d** show relationships between Fermi energy, conduction-band energy, and valence-band energy for an unpassivated Schottky diode, a passivated Schottky diode in which MIGS are not removed, an unpassivated Schottky diode in which

MIGS are removed and a passivated Schottky diode in which MIGS are removed according to one embodiment of the present invention, respectively.

[0025] **Figure 8** shows a curve of interface layer resistance versus interface layer thickness for an electrical junction containing an interface layer disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

[0026] Described herein are processes for depinning the Fermi level of a silicon-based semiconductor (e.g., Si, SiC or SiGe) at a metal-semiconductor junction as well as devices that use such a junction. As more fully discussed below, an interface layer is introduced between the semiconductor and the metal. The interface layer functions to passivate the semiconductor surface (that is, terminate dangling bonds that may otherwise be present at the semiconductor surface so as to assure chemical stability of the surface) and to displace the semiconductor from the metal so as to reduce the effect of MIGS.

[0027] As discussed more fully below, the present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal – interface layer – semiconductor junction, there exist corresponding minimum specific contact resistances. Indeed, minimum specific contact resistances of less than or equal to approximately $10 \Omega - \mu m^2$ or even less than or equal to approximately $1 \Omega - \mu m^2$ may be achieved for such junctions in accordance with the present invention. To achieve such low contact resistances, a metal that has a work function near the conduction band of the semiconductor for n-type semiconductors, or a work function that is near the valence band for p-type semiconductors, is selected.

[0028] The Schottky barrier in such junctions is already minimized, meaning that it is much less than the Schottky barrier presented by a junction in which the Fermi level is pinned, generally near the middle of the semiconductor's bandgap. The current versus voltage (IV) characteristic of these junctions is non-linear, generally having a slope that increases as the voltage increases, such that the derivative of current with respect to voltage is increasing with voltage. This results in a decreasing differential resistance (dV/dI) and a decreasing resistance (V/I). Thus, a junction that has high resistance or high differential resistance near the origin of the IV characteristic (zero volts) may have significantly lower resistance or lower differential resistance at higher voltages.

[0029] The present invention achieves low resistance and low differential resistance near the origin of the current-voltage characteristic for a metal – interface layer – semiconductor junction. Generally, the voltage around the origin should be less than about 100 mV, or more preferably less than about 10 mV for purposes of measuring, determining, or utilizing such junctions of low resistance. At higher voltages, the junction resistance will be even lower. It is thus a feature of the present invention to set an upper bound on the resistance of a contact, where the upper bound occurs at low voltages.

[0030] It is further noted that in junctions where the Schottky barrier is minimized as described above, such that the Fermi level at the junction interface at zero volts lies at or near the conduction band edge or valence band edge (for *n*- and *p*-type semiconductors, respectively), the *IV* characteristic will be nearly symmetric, especially at low voltage. In this case, the term “forward bias” is not defined in the usual sense of a diode wherein forward bias corresponds to the direction of bias for which greater current flows. Thus, in determining or utilizing low resistance junctions of the present invention, the voltage may be either positive or negative.

[0031] It is also possible (in accordance with a further embodiment of the present invention) to make junctions where the Schottky barrier is higher than it would be if the Fermi level at the junction interface were pinned, usually around mid-gap of the semiconductor. Such junctions are formed in the present invention between a metal with a workfunction near or substantially equal to the conduction band edge of a *p*-type semiconductor, or between a metal with a workfunction near or substantially equal to the valence band edge of an *n*-type semiconductor. These junctions are diodes, in that little current will flow if the *n*-type (*p*-type) semiconductor is biased positive (negative) with respect to the metal, and large currents will flow if the voltage is reversed. The low-current flow state is referred to as reverse bias, and the high-current flow state is referred to as positive bias.

[0032] Low resistance in the case of a diode is only relevant in forward bias conditions. In junctions created in accordance with the present invention the resistance contribution of the

interface layer is smaller than the resistance due to the Schottky barrier. That is, in forward bias conditions for junctions created in accordance with the present invention, the transport of charge is limited mainly by the thermal emission of carriers from the semiconductor over the barrier at the interface, and not by the tunneling through the interface dielectric. Thus, low resistance in the case of a diode refers to a resistance lower than the resistance presented by the Schottky barrier.

[0033] In certain applications of diodes, the ability to withstand high reverse biases may be more desirable than high current flow in forward bias. These applications would be considered high voltage/low power applications. In such cases, a low resistance is not essential, and junctions created in accordance with still another embodiment of the present invention provide high-voltage diodes capable of withstanding voltages higher than could otherwise be achieved if the Fermi level of the semiconductor in the junction were pinned.

[0034] The present invention is discussed below in terms of presently preferred embodiments thereof, however, this discussion is not meant to limit the scope of the invention. By studying the present disclosure, others of ordinary skill in the art may recognize equivalent procedures, materials or structures that can be substituted for those described herein to achieve the same effect. The reader is advised and reminded that the use of such equivalents is deemed to be within the scope of the present invention. For example, where the discussion refers to well-known structures and devices, block diagrams are used, in part to demonstrate the broad applicability of the present invention to a wide range of such structures and devices.

I. Introduction and Definitions

[0035] The present discussion makes use of terms that, although well known in the art, may not be familiar to all readers. Therefore, before beginning a detailed discussion of the present invention, it is helpful to define certain terms and concepts. To understand the properties of metal-semiconductor junctions and the impact of the present invention, one must refer to some important energy scales, which are shown graphically in **Figure 2**. The so-called vacuum

[0036] As illustrated in the diagram, semiconductors also have a Fermi level (E_F) and a work function (Φ_S), however, the work function is not an invariant property of the semiconductor. Because the Fermi level varies depending on the doping level in the semiconductor (i.e., the relative amounts of impurities introduced into the semiconductor crystal which change the electron and hole carrier concentrations), a separate parameter, the electron affinity (χ_S), is defined. The electron affinity is an invariant property of the semiconductor and is the difference between the vacuum level and the conduction band edge of the semiconductor. In a semiconductor, almost all energy states are filled in the valence band (E_V) while the conduction band (E_C) is almost empty.

[0037] Now consider a conventional junction between a metal and an n -type semiconductor that has a work function smaller than the work function of the metal (i.e., $\Phi_S < \Phi_M$). An n -type semiconductor is one in which electrons are the majority charge carriers (in p -type semiconductors, holes are the majority charge carrier). As shown in **Figure 3**, because the Fermi level in the semiconductor is higher than the Fermi level in the metal, electrons transfer from the semiconductor 310 to the metal 320 when the materials are brought into contact. Thus, a depletion region (i.e., a region in which there are no free charge carriers) 330 forms near the junction interface 340.

[0038] The formation of the depletion region gives rise to an electric field and so-called “band bending”, as one approaches the junction interface from the semiconductor side (see **Figure 4**). The band bending creates an energy barrier (discussed above) that blocks further

transfer of electrons into or out of the semiconductor. Similar barriers are formed for a junction between a metal and a *p*-type semiconductor when the work function of the metal is less than the work function of the semiconductor. However, in the case of a metal-*n*-type semiconductor junction in which the work function of the semiconductor is greater than that of the metal or a metal-*p*-type semiconductor junction in which the work function of the semiconductor is less than that of the metal, no such energy barriers are created and the contact is said to be ohmic in nature.

[0039] As discussed above, although Schottky first postulated that the height of the energy barrier (Φ_b) formed at a metal-semiconductor junction was simply the difference between the work function of the metal and the electron affinity of the semiconductor, experiments have not verified this relationship. Instead a more complex explanation that takes into account the effects of surface defect states, inhomogeneities and MIGS appears to provide more accurate estimates of barrier heights by explaining the pinning of the Fermi level in the semiconductor. The present inventors have created a technique which is believed to depin the Fermi level of a Si-based semiconductor at a junction with a metal (and thus allow for control or tuning of the barrier height) by both passivating the semiconductor surface (to eliminate or at least reduce the effects of surface states and possibly inhomogeneities) and displacing the metal from the semiconductor (to eliminate or at least reduce the effects of MIGS). This depinning is achieved by introducing an interface layer between the semiconductor and the metal to create a semiconductor -- interface layer -- metal junction, which still permits significant current to flow between the metal and the semiconductor when the junction is forward biased.

[0040] This latter point is important. As discussed further below, for contacts where the energy bands of the semiconductor and the conductor align (i.e., where the Fermi level of the conductor aligns with the conduction or valence band of the semiconductor depending on semiconductor type and/or contact application), if the interface layer is too thin, the specific contact resistance of the junction increases because of the presence of MIGS, resulting in an increased barrier height; thus, current flow is hampered. Conversely, if the interface layer is

too thick, the specific contact resistance is again increased and one gets low current across the junction because of tunneling limitations. The present invention achieves an interface layer that is thick enough to reduce or eliminate the effect of MIGS, while still thin enough to permit significant current flow.

II. Passivation of Semiconductor Surfaces

[0041] A common processing operation performed during semiconductor device fabrication is silicon surface passivation. Surface passivation (whether by an oxide or another material) chemically neutralizes and physically protects the underlying silicon. For example, exposing a silicon surface to oxygen (under the appropriate conditions to grow a protective film of silicon dioxide) will allow the oxygen to react with the dangling bonds of the silicon surface to form covalent bonds that satisfy the surface silicon atoms' valency and render the surface fully coordinated. These covalent bonds provide chemical stability to the silicon surface. The covalent bonds also tie up unbound charges that exist on the silicon surface as a result of the discontinuation of the semiconductor crystal at the surface.

[0042] However, passivation with silicon dioxide has several significant disadvantages. For example, silicon dioxide is a dielectric insulator that poses a significant barrier to the flow of current. Accordingly, a layer of silicon dioxide deposited or grown on a silicon surface may significantly reduce the ability for electrical current to flow through that surface. As a result, the use of silicon dioxide has been limited in practicality to surfaces external to the active region of semiconductor devices through which current passes during device operation (e.g., as a gate oxide layer). This disadvantage is compounded by the fact that the silicon dioxide grows very rapidly and readily on the silicon surface so that it is difficult to limit the growth to a thin layer. Silicon dioxide is also a poor diffusion barrier to semiconductor dopants such as boron.

[0043] Instead of making use of silicon dioxide then, in one embodiment the present inventors utilize a nitrided semiconductor surface to provide chemical passivation. That is, a

nitride layer is introduced to passivate the semiconductor surface by eliminating or at least reducing the effects of surface states and possibly inhomogeneities. The nitride layer also displaces the metal from the semiconductor and eliminates or at least reduces the effects of MIGS. The result of introducing the nitride layer as an interface between the semiconductor and the metal is a depinning of the Fermi level of the semiconductor. When the Fermi level of the semiconductor is depinned, the Fermi level of the metal at the interface will be that of the bulk metal, and will not be dependent upon the interface. In addition to the above, the present inventors propose techniques for providing non-insulating, passivated semiconductor surfaces using materials other than nitrogen; for example, oxides, hydrides, arsenides and/or fluorides.

[0044] These developments have wide applicability in connection with the fabrication of Schottky diodes, Schottky-barrier transistors and other electrical components. For example, in Schottky diodes, the ability to control the energy barrier height at the diode junction is important if the device is to be tailored to specific applications. Use of the present techniques allows for tuning of the barrier height. Further, for other three-terminal devices with Schottky-barrier-isolated channels, control of device characteristics is made possible through the present invention by allowing *n*- and *p*-type devices to be fabricated without dopants, relying instead on the use of metals with different work functions.

[0045] **Figure 5** shows a semiconductor device 510 that contains a semiconductor 530 and an interface layer 520 formed on a surface 540 of the semiconductor in accordance with the present invention. The terms semiconductor device, microelectronic device, monolithic device, chip, and integrated circuit are often used interchangeably in this field. Any or all such devices may each contain an interface layer formed on a semiconductor surface in accordance with the present invention.

[0046] The semiconductor 530 contains a semiconductor material. The term semiconductor material refers to a material having a bandgap that is greater than about 0.1 eV and less than about 4 eV. The term bandgap refers to an energy gap of forbidden energy levels separating the conduction band, which is an upper energy band that is mostly devoid of electrons and

wherein electrons can conduct, and the valence band, which is an energy band that is mostly filled with electrons and wherein electrons cannot conduct. The semiconductor material may have a wide range of doping levels including no doping at all.

[0047] The semiconductor 530 has a surface 540 that is passivated by the interface layer 520. In this context (and as used elsewhere herein) the term passivation means the elimination or at least the reduction of the effects of surface states due to defects or dangling bonds of the semiconductor surface 540. Note that passivation does not, as a practical matter, require that all surface states be eliminated. Rather, it is the effect of surface states on the device properties that is limited or eliminated in passivation. Note further that the presence of MIGS may be regarded as a surface state, however, as used herein the term passivation is not meant to infer the elimination of MIGS (though in some cases, a passivation layer may have sufficient thickness to provide a separation layer between the semiconductor and the metal sufficient to reduce or eliminate MIGS). The semiconductor 530 is operable to be electrically coupled with a first voltage associated with the semiconductor device 510 and to conduct electrical current 550 across the passivated surface 540.

[0048] The interface layer 520 is formed on the semiconductor 530 and may contain a passivation material that bonds to the semiconductor material by way of a covalent (or other) bond formed between the passivation material and the semiconductor material. For example, an atom of passivation material may covalently bond with a dangling bond of a surface silicon atom to fully coordinate the silicon atom and thereby help passivate the silicon atom. In some cases, the passivation material may be the sole component of the interface layer 520, while in other cases the interface layer 520 may be a compound layer that includes both a passivation layer and a separation layer. That is, the interface layer serves to (i) chemically passivate the semiconductor surface 540, and (ii) displace the semiconductor from the metal sufficiently to eliminate or at least reduce the effect of MIGS. As explained below, this may necessitate including a separation layer in addition to a passivation layer within the interface layer, depending on the passivation material selected. Of course, the combination of the passivation

layer and the separation layer must be sufficiently thin to permit the low specific contact resistances described herein.

[0049] Different passivation materials are contemplated. According to one embodiment, the interface layer 520 is formed using a material that is preferably selected from the group consisting of hydrogen (H), oxygen (O), nitrogen (N), arsenic (As), and fluorine (F) (that is, the interface layer 520 may include a nitride, an oxide, a hydride, an arsenide and/or a fluoride). Other materials having chemical characteristics or valences similar to these materials may also be used. Note that distinct separation layers (i.e., in addition to the passivation layer(s)) may be needed where H, As, or F passivation layers are used, as these tend to form monolayer coverage, rather than a layer of a compound with Si of process-dependent thickness. In contrast, passivation layers made using N and/or O may not require distinct separation layers, as these elements may form a layer of a compound of Si with a thickness that can be varied depending on processing.

[0050] Different amounts of passivation material are contemplated to be useful for different embodiments of the present invention. Often, the interface layer 520 includes or is made up of a passivation layer with a thickness of between approximately 0.1 nm and about 5 nm. For example, depending upon the particular implementation, the thickness may be less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, may be the thickness corresponding to a single layer or monolayer of passivation material that is bonded to the semiconductor surface, or may even be the number of atoms of passivation material required to passivate substantially all the dangling bonds associated with the semiconductor surface 540.

[0051] In some cases, passivation of the semiconductor surface 540 will include removing (or terminating) dangling bonds located proximate to the surface of the semiconductor material, including those at the surface as well as those within a few molecular dimensions from the surface. This process may stabilize the surface of the semiconductor material and may improve the controllability of subsequent fabrication operations. Passivation may also reduce the density of surface states that may exist at the semiconductor surface as a result of the

discontinuation of the semiconductor crystal at the surface. This may improve consistency and performance of the semiconductor device, inasmuch as such states are known to interfere with proper device operation. For example, they may provide surface charge states that result in a pinning of the Fermi level.

III. Forming Interface Layers

[0052] Exemplary methods for forming interface layers to provide (i) passivation of semiconductor surfaces, and (ii) displacement of the semiconductor from the metal to eliminate or at least reduce of the effects of MIGS within the semiconductor when in the presence of the metal (collectively referred to herein as depinning the Fermi level of the semiconductor) with hydrogen, fluorine or nitrogen are presented below to further illustrate the concepts of the present invention. Other passivation materials may include arsenic, oxygen or an oxynitride, and in some cases such passivation layers are combined with separation layers (e.g., made of an oxide) to complete the interface layer.

A. Hydrogen And Fluorine

[0053] An interface layer may contain hydrogen, fluorine, or both hydrogen and fluorine (e.g., in the form of a hydride and/or a fluoride). One method for forming an interface layer on a semiconductor surface with hydrogen and fluorine includes cleaning the semiconductor substrate with a cleaning solution, immersing the cleaned substrate in a hydrogen fluoride solution (or other liquid containing hydrogen and fluorine ions) having an effective concentration typically between about 1%-50% by weight, waiting an effective period of time, typically between about several seconds and about 5 minutes, removing the substrate from the hydrogen fluoride solution, optionally rinsing the substrate in deionized water, and blow-drying the substrate with nitrogen. Such a method may form an interface layer containing hydrogen and fluorine that are bonded (e.g., covalently) to the semiconductor surface.

[0054] It should be noted that long rinses in deionized water, generally longer than about 30 seconds, might remove the hydrogen passivation. Thus, deionized water rinses might advantageously be kept to less than about 30 seconds to maintain the hydrogen passivation of the surface. Also, the higher the concentration of the hydrogen fluoride during the immersion, the greater the concentration of fluorine passivation. Finally, methods are also contemplated where the ratio of hydrogen to fluorine passivation is altered by removing either the hydrogen or the fluorine.

[0055] An interface layer formed in this fashion may be best suited for applications where a subsequent metal layer is deposited over the interface layer in a generally non-invasive fashion, for example using a thermally evaporated source. Experiments by the present inventors to date suggest that using other approaches (e.g., plasma deposition) may cause damage to the thin (e.g., monolayer thick) interface layer contemplated as part of the present invention.

B. Nitrogen

[0056] In a further embodiment, an interface layer may contain nitrogen (e.g., in the form of silicon nitride). One method for forming an interface over a semiconductor surface with nitrogen includes heating a substrate containing the semiconductor surface in the presence of a nitrogenous material (that is, a gas or other material containing nitrogen). For example, a substrate containing an exposed silicon surface may be annealed at a temperature between about 300°C and about 750°C, which is lower than temperatures conventionally used for Rapid Thermal Nitridation (RTN), under a gaseous ambient having, for example, ammonia (NH₃) at some effective partial pressure. By exposed, we mean a clean surface, free of everything except silicon. Such a method may form an interface layer containing nitrogen, often in the form of a nitride, bonded to the semiconductor surface. Note that the present inventors have observed indications suggesting that in these low temperature conditions interface layer growth is self-limiting, depending only on temperature.

[0057] According to another embodiment, an interface layer that includes nitrogen may be formed on an exposed surface of a semiconductor material by a method that includes heating a semiconductor material to a substantially high temperature under vacuum and exposing the semiconductor material to a substantially small amount of a nitrogenous material, such as ammonia. The method may include placing a semiconductor having an exposed semiconductor surface in a heating chamber, pulling a vacuum of less than about one millionth of a Torr, or more favorably an ultra high vacuum of less than 10^{-9} Torr, and then heating the semiconductor in the heating chamber to a substantially high temperature. The higher the vacuum, the longer the substrate may be heated without growth of an oxide from residual oxygen or water in the chamber. Thus, the process may include heating the semiconductor to a temperature that is between about 900°C and about 1000°C, or higher, in an inert ambient. As desired, the semiconductor may be exposed to hydrogen gas, or an equivalent, to reduce any native oxide on the semiconductor. These high temperatures may provide for greater passivation of the semiconductor surface as compared with results that may be achieved at lower temperatures.

[0058] Then, the heated semiconductor may be exposed to a substantially small amount of a nitrogenous material, such as ammonia. This may include exposing the semiconductor surface to ammonia for a substantially short period of time. For example, the surface may be subjected to a burst or pulse of ammonia lasting for a time period between about 0.5 seconds and about 5 seconds. Alternatively, the surface may be exposed to a controlled, small amount of ammonia over an arbitrarily longer period of time. In this way, the substantially small amount of ammonia will react with the surface to form a nitrogenous interface layer, such as a nitride layer, thereon and then further growth of the interface layer will cease. Then the semiconductor may be cooled from the substantially high temperature to ambient temperature and removed from the heating chamber. Further annealing of the substrate and the grown nitride layer may also be performed in the vacuum chamber before removal, at a substantially elevated temperature between about 700°C and 1000°C, or higher.

[Faint, illegible markings]

IV. Diodes Containing Passivated Semiconductor Surfaces

Attorney Docket No.: 003771.P003

[0062] As mentioned above, the present inventors have devised a scheme to control or adjust a Schottky barrier height by forming an interface layer (which includes or sometimes consists of a passivation layer that includes an oxide, oxynitride, nitride, arsenide, hydride, fluoride, or an equivalent) between a metal and a semiconductor. This scheme differs from past attempts by others to control barrier height, which attempts generally involved either using a silicide as a contact metal (and thus limiting the choices of available contact metals to those that can form silicides), or using esoteric substrates that exhibit wide bandgaps. Further, in previous devices the Fermi level of the semiconductor remains pinned, with the barrier height being virtually independent of the metal used. Finally, doping of substrates has also been attempted, however, it has not been shown to truly affect the barrier height of the substrate material. For example, PtSi contacts have reduced resistance due to high silicon doping such that the current across the junction is dominated by tunneling through the barrier. Doping may thus lead to cases where the top of the barrier may be so thin as to be essentially transparent to electrons, however, doping does not appear to allow actual tuning of the barrier height.

[0064] The conductor 630 contains a conductive material such as a metal or an alloy of a metal. The terms metal, conductive material, and conductor are all related and appear in order from specific at the left to general at the right. In general, the terms refer to a highly electrically conductive substance that has a Fermi energy level that sits in a partially filled band. Unless otherwise specified, conductors include metals (e.g., pure metals and alloys),

and other conductors such as doped polysilicon (a nonporous silicon containing randomly oriented crystallites), doped single crystal silicon, and metal silicides. Note that alloys may have workfunctions different than their constituents and may be designed to have specific workfunctions though selective use of ratios of the constituent metals.

[0065] Often, the conductor is a metal since metals may offer advantages over conductive semiconductors including lower resistance, higher carrier mobilities that provide superior high frequency performance and switching, favorable low power characteristics, and ease of manufacturing control. Use of metals may also avoid the need to perform semiconductor doping, which may simplify manufacturing and improve quality control.

[0066] Metals that are contemplated include pure metals, alloys, refractory metals, metals that do not form silicides, metals physically deposited by substantially non-invasive processes such as by condensation of a thermally evaporated metal vapor, and metals having a predetermined work function. The use of non-invasively deposited metals may allow for forming the metal on a thin interface layer without disrupting the passivation properties of the layer.

[0067] A metal having a predetermined work function may be a metal having a work function smaller or greater than that of the semiconductor, depending on the desired application. Often, the semiconductor will be silicon. In this case by the work function of a semiconductor or silicon we mean the energy in the middle of the semiconductor bandgap. Exemplary metals that have a work function smaller than silicon include Group 3A elements, aluminum (Al), indium (In), titanium (Ti), chromium (Cr), tantalum (Ta), cesium (Cs), magnesium (Mg), erbium (Er), ytterbium (Yb), manganese (Mn), lead (Pb), silver (Ag), yttrium (Y), and zinc (Zn). Exemplary metals that have a work function greater than silicon include platinum (Pt), gold (Au), tungsten (W), nickel (Ni), molybdenum (Mo), copper (Cu), cobalt (Co), and palladium (Pd).

[0068] The semiconductor-interface layer-conductor configuration illustrated in **Figure 6** defines what the present inventors have chosen to call a “passivated Schottky barrier”. The

passivated Schottky barrier is a naturally formed electrical potential barrier to an electron or hole at the Fermi energy (the electrochemical potential) in the conductor due to a depletion region formed in the semiconductor adjacent the conductor. The passivated Schottky barrier may deviate in barrier height from a standard un-passivated Schottky barrier that would form naturally at a contact junction between the semiconductor and the conductor without the interface layer disposed therebetween. That is, the passivated Schottky barrier may have a barrier height that depends predominantly upon the bulk characteristics of the semiconductor and the conductor, rather than on surface properties, and may depend in part on the characteristics of the interface layer.

[0069] Indeed, the present inventors have determined that changes in barrier height are approximately monotonic and continuous for variations in surface passivation thickness by nitridation of the semiconductor substrate. More specifically, experiments by the present inventors in a regime where the nitride layer is sufficiently thick to remove MIGS show that temperature of interface layer formation has the strongest effect on barrier height. In other regimes, thickness may be critical. Ideally, if all surface states are removed, barrier height should be controllable simply by the choice of metal used.

[0070] To understand why thickness of the interface layer is important, refer briefly to **Figure 8** where a graph of interface-specific contact resistance versus interface thickness is shown. The graph is for a structure where the workfunction of the metal is the same as the electron affinity in the semiconductor, such that the Fermi level of the metal lines up with the conduction band of the semiconductor. At large thicknesses, the interface layer poses significant resistance to current. As thickness decreases, resistance falls due to increased tunneling current. However, there comes a point where even as the interface layer continues to get thinner, resistance increases. This is due to the effect of MIGS, which increasingly pull the Fermi level of the metal down towards mid-gap of the semiconductor, creating a Schottky barrier. The present inventors have discovered that this competition results in an optimum thickness, as shown in the illustration, where the resistance is a minimum. At this thickness

the effect of MIGS has been sufficiently reduced to depin the metal and lower the Schottky barrier, and the layer is still sufficiently thin to allow significant current flow across the interface layer. Contact resistances of less than or equal to approximately $2500 \text{ } \Omega\text{-}\mu\text{m}^2$, $1000 \text{ } \Omega\text{-}\mu\text{m}^2$, $100 \text{ } \Omega\text{-}\mu\text{m}^2$, $50 \text{ } \Omega\text{-}\mu\text{m}^2$, $10 \text{ } \Omega\text{-}\mu\text{m}^2$ or even less than or equal to $1 \text{ } \Omega\text{-}\mu\text{m}^2$ may be achieved.

[0071] Characteristics that may be adjusted to provide a desired barrier height thus include the passivation material used (e.g., selection based on bandgap), the interface layer thickness (e.g., especially where the interface layer is a compound layer formed of a passivation layer and a separation layer), the method of forming the interface layer (e.g., control of parameters such as temperature), the interface layer thickness that is substantially similar to a penetration depth of MIGS formed at a metal interface, the metal used for the source and/or drain, and other characteristics.

[0072] One advantage of the ability to adjust the Schottky barrier height with the introduction of interface layer 620 is the ability to form a substantially high barrier height. For example, an interface layer may be used to create a Schottky barrier having a barrier height that is greater than can be achieved through the use of metal silicides, greater than about 2.0 eV, or greater than about 2.5 eV (using a semiconductor with a bandgap at least this large), or nearly 1.0 V using silicon. Such high barrier heights imply the ability to withstand high voltages before breakdown occurs. Thus, Schottky barriers having such high barrier heights may be particularly useful in high-voltage Schottky diodes.

[0073] Another advantage achieved through the use of the interface layer 620 is greater flexibility afforded in selecting a conductor 630. Typically, metals chosen for application in classic Schottky diodes are those that can form a silicide with a silicon semiconductor. The formation of the silicide helps to reduce surface states (resulting from dangling bonds), but not the effects of MIGS. Thus, the Fermi level at the semiconductor surface is still pinned. Using metals that form silicides upon contact with silicon may thus help to make the devices more

reproducible in a manufacturing environment, but such devices still suffer from the drawback of having a barrier height that is fixed.

[0074] According to one embodiment of the present invention, however, one may select a conductor that is not able (or not readily able) to form a silicide with the semiconductor. The metal silicide is not needed because the interface layer provided in accordance with the present invention passivates the semiconductor surface and also reduces or eliminates the effect of MIGS. This may allow for selection of a metal that has properties such as a desirable work function or Fermi level energy, even though that metal may not form a metal silicide.

[0075] For example, to make large-barrier diodes, for an *n*-type doped silicon semiconductor, a metal may be selected that has a work function that is either substantially equal to the valence band energy of the semiconductor or that is within about 0.1 eV to about 0.3 eV of the valence band energy of the semiconductor. Similarly, for a *p*-type doped silicon semiconductor, a metal may be selected that has a work function substantially equal to the conduction band energy of the semiconductor. For Schottky diodes configured in accordance with the present invention, the Fermi level of the metal may lie anywhere in the bandgap of the semiconductor when an interface layer is disposed within the junction, resulting in diodes of various barrier heights. The Fermi level of the metal may also lie in the conduction or valence band of the semiconductor.

[0076] The use of interface layer 620 thus provides a way to tune, adjust, or control the height of the barrier between the conductor and the semiconductor. Without the interface layer 620, the barrier height would be substantially un-tunable, un-adjustable, and fixed (as discussed above).

[0077] The role played by interface layer 620 in tuning, adjusting, or controlling the height of the barrier between the conductor 630 and the semiconductor 610 may be understood as a depinning of the Fermi level of the semiconductor. That is, the interface layer may reduce surface states by bonding to the semiconductor material to consume dangling bonds. Additionally, the interface layer may reduce the formation of MIGS in the semiconductor by

providing a thickness and bandgap that prevent the electron wave function (of the metal) from penetrating into the semiconductor. The electron wave function may instead penetrate into the interface layer and form MIGS within the interface layer at an energy related to the states of the interface layer material. As desired, the density of the MIGS and the depth of MIGS penetration into the interface layer may be reduced by choosing an interface layer material or materials having a larger bandgap or higher effective mass than the semiconductor.

[0078] According to one embodiment of the present invention then, the interface layer 620 is incorporated into a device operable to pass current through the semiconductor surface and the interface layer during device operation. In such an embodiment, it may be desirable to use an interface layer having a thickness of a monolayer, or, for example between about 0.1 nm and about 0.3 nm, and also having a wide bandgap (as compared to that of the semiconductor) so that the interface layer both de-pins the Fermi level (so that the barrier height depends predominantly on bulk properties of the junction materials) and allows sufficient current transfer across it. Advantageously, such interface layers may be sufficiently thin to provide low impedance to current flow (due to the exponential dependence of direct tunneling on barrier thickness), which is desirable for many semiconductor devices, while also providing sufficient semiconductor surface passivation to allow an adjustable barrier height. That is, the interface layer may allow passivation of surface states and reduction (or elimination) of MIGS in the semiconductor to allow for an adjustable barrier height with a substantially thin layer that allows sufficient current to be transferred across the interface layer.

[0079] There are several methods by which the barrier height can be made adjustable. For example, adjustment may be made by tuning the degree of Fermi level pinning. In other words, some embodiments may allow for a sufficiently thin interface layer so that not all of the effects of MIGS in the Si are eliminated. Further, the pinning may be varied by combinations of thickness of the interface layer and the choice of interface material. The metal in contact with the interface layer may be pinned by MIGS at different levels in different materials. Conversely, or in addition, the passivation may be left incomplete to allow for an

effective level of unpassivated states. Complete depinning of the Fermi level (that is removal of all surface states in Si including MIGS) is another option, in which case one could tune the barrier height simply by choosing a pure metal or an alloy that possesses the desired workfunction. In that case, the barrier height is determined by Equation (1), which until now has been an unrealizable idealization. Note that the type of tuning being discussed here is adjustment of the barrier height by altering the structure of the junction at the time of manufacture, not by varying an externally applied condition during junction operation.

[0080] **Figure 7a – 7d** show relationships between Fermi energy, conduction band energy, and valence band energy for various Schottky barriers containing a metal in contact with (or in close proximity to) a semiconductor, where the bandgap (E_g) of the semiconductor exists between the conduction band (E_c) and the valence band (E_v). In this example, the work function of the metal Φ_M is chosen to be approximately equal to the electron affinity χ_s of the semiconductor. In **Figure 7a**, an unpassivated Schottky barrier 700 is shown. In this example, the Fermi level (E_F) of the metal 730 is pinned in the bandgap of the semiconductor 710. This results in a discontinuity in the vacuum level caused by a charged dipole at the interface.

[0081] In **Figure 7b**, the interface layer 720b is thick enough to passivate dangling bonds at the surface of the semiconductor 710, but not thick enough to eliminate or sufficiently reduce the effect of MIGS. As a result, the band structure is largely unaltered from that seen in the previous illustration. Similarly, in **Figure 7c**, when the interface layer 720c is sufficiently thick to eliminate or reduce the effect of MIGS but not to passivate the semiconductor surface, little change in the energy band structure is observed. However, as shown in **Figure 7d**, when the interface layer 720d is sufficient to both eliminate or reduce the effect of MIGS and to passivate the semiconductor surface, we see the Fermi level of the metal aligning with the conduction band of the semiconductor (i.e., the Fermi level of the semiconductor has been depinned and no longer lines up with the Fermi level of the metal). The vacuum level is now continuous as there is no charged dipole at the interface. Thus, the band structure of a device

constructed in this fashion is a result of only bulk material properties, not properties of the surface. By way of example, the materials in such cases may be Al and Si, with a work function for Al of approximately $\Phi_M = 4.1$ eV and the electron affinity for Si of approximately $\chi_S = 4.05$ eV.

V. Transistors Containing Passivated Semiconductor Surfaces

[0082] The interface layers described herein may be used in connection with a semiconductor surface of a channel in a field effect transistor. That is, an interface layer may be disposed between a source and a channel, a channel and a drain, or both of an insulated gate field effect transistor. Such use of an interface layer is described in detail in co-pending U.S. Patent Application No.: _____ entitled “INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL”, filed _____, 2002 by the present inventors, and assigned to the assignee of the present invention.

[0083] The source and drain contacts at the channel of a field effect transistor are examples of a broader category of metal-interface layer-semiconductor contacts that make up the present invention. In the past, such contacts generally comprised a silicide-n⁺-Si junction, which formed a somewhat “leaky” Schottky diode, with a Fermi level of the semiconductor pinned at the midgap. In contrast, the present invention provides a contact wherein the Fermi level of the metal is aligned with the conduction band of the semiconductor (e.g., as shown in Figure 7d). Note that in other cases, depending on the type of semiconductor material and conductors used, the Fermi level of the metal may align with the valence band of the semiconductor.

[0084] Although both types of junctions (i.e., the new passivated Schottky barrier junction and the conventional silicide-semiconductor junction) permit tunneling currents, the present junction can be fabricated with a much thinner interface layer as compared to the thickness of the silicide layer used previously. Indeed, thickness of an order of magnitude less than the silicide thickness can be expected. In a conventional silicide – semiconductor junction a

Schottky barrier is formed which is comprised of a depletion layer. The tunnel barrier presented by such a depletion layer may be an order of magnitude thicker than the dielectric tunnel barrier in the present invention. The thinner interface layers provided by the present invention permit higher current across the junction (i.e., lower junction specific contact resistance).

[0085] Two other properties of the dielectric deserve mention. First is the property of the height of the barrier compared to the semiconductor conduction band (for electrons). In making the barrier thinner than a silicide barrier, the tradeoff may be a higher tunnel barrier (e.g., 2 eV for nitride, compared with about half the gap of 0.6 eV for silicide). Spacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV). Nevertheless, even with the higher barrier to electrons, the present inventors have determined that the resistance can still be one hundred times lower than a contact to silicon with a silicide barrier.

[0086] The second property is the effective mass of electrons in the dielectric. Larger mass electrons will not penetrate as far (i.e., because of their shorter wavelength) from the metal into the semiconductor. The less the electrons penetrate into the dielectric, the less the effect of MIGS in the dielectric. Thus, MIGS in the dielectric are reduced with larger bandgap and larger effective mass.

[0087] In addition the junction of the present invention can be used in making contacts to source or drain implanted wells and will have the advantage of reducing the need for high doping levels (which are now reaching their limits of solid solubility). The high doping profiles were required in the past in order to keep the junction depletion layer relatively thin, so as to increase the tunneling current, thus reducing the junction resistance. However, it is becoming increasingly difficult to increase doping profiles in order to provide low resistance junctions. It may be possible to reach the same level of resistance with a lower doping concentration using the present invention. It may further be possible to achieve much lower resistance even with lower doping concentration. When the present invention is used with high doping levels, the resistance will be further reduced.

[0088] Thus, methods and applications for semiconductor-interface layer-metal junctions have been described. Although described with reference to specific embodiments it should be remembered that various modifications and changes may be made to the techniques described herein without departing from the broader spirit and scope of the invention. The specification and drawings are accordingly to be regarded in an illustrative rather than a restrictive sense and the invention measured only in terms of the claims, which follow.

CLAIMS

What is claimed is:

1. An electrical device, comprising:
 - a metal;
 - a silicon-based semiconductor having a Fermi level; and
 - an interface layer disposed between and in contact with both the metal and the semiconductor and configured to depin the Fermi level of the semiconductor,
 wherein the electrical device has a specific contact resistance of less than or equal to approximately $1000 \Omega - \mu m^2$.
2. The electrical device of claim 1 wherein the interface layer includes a passivating material.
3. The electrical device of claim 2 wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of silicon.
4. The electrical device of claim 3 wherein the interface layer consists essentially of a monolayer configured to depin the Fermi level of the semiconductor.
5. The electrical device of claim 2 wherein the interface layer further includes a separation layer.
6. The electrical device of claim 1 wherein the specific contact resistance is less than or equal to approximately $100 \Omega - \mu m^2$.

7. The electrical device of claim 1 wherein the specific contact resistance is less than or equal to approximately $50 \Omega\text{-}\mu\text{m}^2$.
8. The electrical device of claim 1 wherein the specific contact resistance is less than or equal to approximately $10 \Omega\text{-}\mu\text{m}^2$.
9. The electrical device of claim 1 wherein the specific contact resistance is less than or equal to approximately $1 \Omega\text{-}\mu\text{m}^2$.
10. The electrical device of claim 1 wherein the interface layer comprises a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material.
11. The electrical device of claim 10 wherein the nitrogenous material comprises at least one of ammonia (NH_3), nitrogen (N_2) or unbound nitrogen (N).
12. An electrical device, comprising a metal – interface layer – Si-based semiconductor junction in which the interface layer includes a passivating material and the electrical device has a specific contact resistance of less than approximately $1000 \Omega\text{-}\mu\text{m}^2$.
13. The electrical device of claim 12 wherein the specific contact resistance is less than or equal to approximately $100 \Omega\text{-}\mu\text{m}^2$.
14. The electrical device of claim 12 wherein the specific contact resistance is less than or equal to approximately $50 \Omega\text{-}\mu\text{m}^2$.
15. The electrical device of claim 12 wherein the specific contact resistance is less than or equal to approximately $10 \Omega\text{-}\mu\text{m}^2$.

16. The electrical device of claim 1 wherein the specific contact resistance is less than or equal to approximately $1 \Omega\text{-}\mu\text{m}^2$.

17. The electrical device of claim 12, wherein the passivating material comprises one or more of a nitride, an oxide, an oxynitride a hydride, a fluoride and/or an arsenide of silicon.

18. The electrical device of claim 17, wherein the interface layer comprises a passivation layer and a separation layer.

19. A method, comprising depinning a Fermi level of a silicon-based semiconductor in an electrical junction through the use of an interface layer disposed between a surface of the semiconductor and a conductor, wherein the interface layer (i) has a thickness sufficient to reduce effects of metal-induced gap states in the semiconductor while providing the junction with a specific contact resistance of less than approximately $1000 \text{ } \Omega - \mu\text{m}^2$, and (ii) passivates the surface of the semiconductor.

20. The method of claim 19 wherein the specific contact resistance is less than or equal to approximately $100\ \Omega\text{-}\mu\text{m}^2$.

21. The method of claim 19 wherein the specific contact resistance is less than or equal to approximately 50 $\Omega\text{-}\mu\text{m}^2$.

22. The method of claim 19 wherein the specific contact resistance is less than or equal to approximately $10 \Omega\text{-}\mu\text{m}^2$.

23. The method of claim 19 wherein the specific contact resistance is less than or equal to approximately $1 \Omega\text{-}\mu\text{m}^2$.

24. The method of claim 19 wherein the interface layer has a thickness sufficient to provide a specific contact resistance of the electrical junction of less than or equal to approximately $1 \Omega\text{-}\mu\text{m}^2$.
25. The method of claim 19 wherein the interface layer includes a passivating material selected from the list comprising: an arsenide, a hydride, a fluoride, an oxide, an oxynitride and a nitride of silicon.
26. The method of claim 25 wherein the interface layer consists essentially of a monolayer.
27. The method of claim 19 wherein the interface layer is grown on the semiconductor surface at temperatures above approximately 300°C .
28. The method of claim 27 wherein the interface layer is grown in the presence of a nitrogenous material.
29. The method of claim 28 wherein the nitrogenous material comprises one of ammonia (NH_3), nitrogen (N_2), or unbound nitrogen (N).
30. The method of claim 19 wherein the interface layer includes a passivation layer grown by immersion of the semiconductor in a liquid containing hydrogen and fluorine ions.
31. An electrical device, comprising a junction between a Si-based semiconductor and a conductor separated from the semiconductor by an interface layer having a thickness that allows a Fermi level of the conductor to align with a conduction band of the semiconductor,

wherein the electrical device has a specific contact resistance less than approximately $1000 \Omega\text{-}\mu\text{m}^2$.

32. The electrical device of claim 31 wherein the specific contact resistance is less than or equal to approximately $100 \Omega\text{-}\mu\text{m}^2$.

33. The electrical device of claim 31 wherein the specific contact resistance is less than or equal to approximately $50 \Omega\text{-}\mu\text{m}^2$.

34. The electrical device of claim 31 wherein the specific contact resistance is less than or equal to approximately $10 \Omega\text{-}\mu\text{m}^2$.

35. The electrical device of claim 31 wherein the specific contact resistance is less than or equal to approximately $1 \Omega\text{-}\mu\text{m}^2$.

36. An electrical device, comprising a junction between a Si-based semiconductor and a conductor separated from the semiconductor by an interface layer having a thickness that allows a Fermi level of the conductor to align with a valence band of the semiconductor, wherein the electrical device has a specific contact resistance less than approximately $1000 \Omega\text{-}\mu\text{m}^2$.

37. The electrical device of claim 36 wherein the specific contact resistance is less than or equal to approximately $100 \Omega\text{-}\mu\text{m}^2$.

38. The electrical device of claim 36 wherein the specific contact resistance is less than or equal to approximately $50 \Omega\text{-}\mu\text{m}^2$.

39. The electrical device of claim 36 wherein the specific contact resistance is less than or equal to approximately $10\ \Omega\text{-}\mu\text{m}^2$.

40. The electrical device of claim 36 wherein the specific contact resistance is less than or equal to approximately $1\ \Omega\text{-}\mu\text{m}^2$.

41. An electrical device, comprising a junction between a Si-based semiconductor and a conductor separated from the semiconductor by an interface layer having a thickness that allows a Fermi level of the semiconductor to be independent of a Fermi level of the conductor, wherein the electrical device has a specific contact resistance less than approximately $1000\ \Omega\text{-}\mu\text{m}^2$.

42. The electrical device of claim 41 wherein the specific contact resistance is less than or equal to approximately $100\ \Omega\text{-}\mu\text{m}^2$.

43. The electrical device of claim 41 wherein the specific contact resistance is less than or equal to approximately $50\ \Omega\text{-}\mu\text{m}^2$.

44. The electrical device of claim 41 wherein the specific contact resistance is less than or equal to approximately $10\ \Omega\text{-}\mu\text{m}^2$.

45. The electrical device of claim 41 wherein the specific contact resistance is less than or equal to approximately $1\ \Omega\text{-}\mu\text{m}^2$.

46. An electrical device, comprising:

a silicon-based semiconductor of either *n*-type or *p*-type semiconductor material;

a metal having a workfunction approximately equal to a conduction band of the semiconductor if the semiconductor is of *n*-type semiconductor material or having a workfunction approximately equal to a valence band of the semiconductor if the semiconductor is of *p*-type semiconductor material; and

an interface layer disposed between and in contact with both the semiconductor and the metal, wherein the electrical device has a specific contact resistance of less than or approximately equal to $1000 \Omega\text{-}\mu\text{m}^2$.

47. The electrical device of claim 46 wherein the interface layer includes a passivating material.

48. The electrical device of claim 47 wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of silicon.

49. The electrical device of claim 48 wherein the interface layer consists essentially of a monolayer configured to depin a Fermi level of the semiconductor.

50. The electrical device of claim 47 wherein the interface layer further includes a separation layer.

51. The electrical device of claim 46 wherein the specific contact resistance is less than or equal to approximately $100 \Omega\text{-}\mu\text{m}^2$.

52. The electrical device of claim 46 wherein the specific contact resistance is less than or equal to approximately $50 \Omega\text{-}\mu\text{m}^2$.

53. The electrical device of claim 46 wherein the specific contact resistance is less than or equal to approximately $10 \Omega\text{-}\mu\text{m}^2$.

54. The electrical device of claim 46 wherein the specific contact resistance is less than or equal to approximately $1 \Omega\text{-}\mu\text{m}^2$.

55. The electrical device of claim 46 wherein the interface layer comprises a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material.

56. The electrical device of claim 55 wherein the nitrogenous material comprises at least one of ammonia (NH_3), nitrogen (N_2) or unbound nitrogen (N).

57. An electrical device, comprising:
 a silicon-based semiconductor of either *n*-type or *p*-type semiconductor material;
 a metal having a workfunction near or substantially equal to a conduction band edge of the semiconductor if the semiconductor is of *p*-type semiconductor material, or having a workfunction near or substantially equal to a valence band edge of the semiconductor if the semiconductor is of *n*-type semiconductor material; and
 an interface layer disposed between and in contact with both the semiconductor and the metal and configured to depin a Fermi level of the semiconductor.

58. The electrical device of claim 57 wherein the interface layer includes a passivating material.

59. The electrical device of claim 58 wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of silicon.

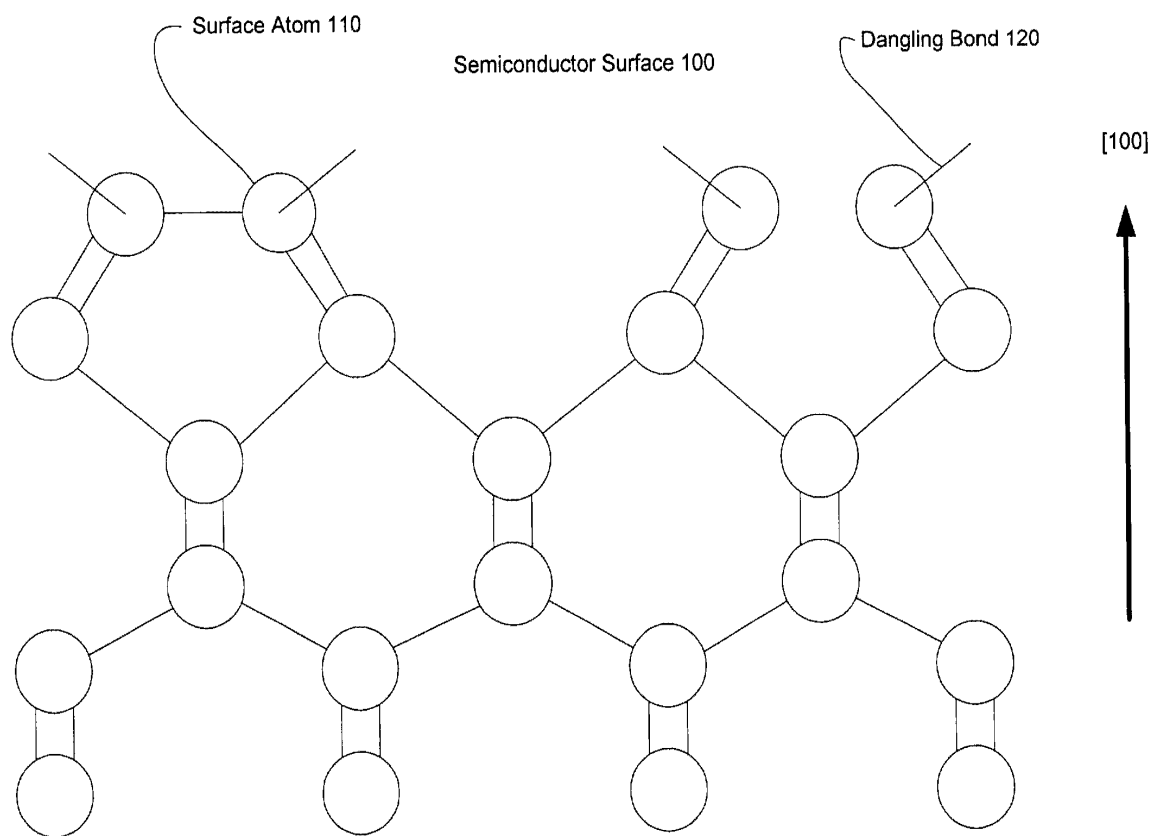
60. The electrical device of claim 57 wherein the interface layer consists essentially of a monolayer configured to depin a Fermi level of the semiconductor.

61. The electrical device of claim 57 wherein the interface layer further includes a separation layer.

ABSTRACT

[0089] An electrical device in which an interface layer is disposed between and in contact with a metal and a Si-based semiconductor, the interface layer being of a thickness effective to depin of the Fermi level of the semiconductor while still permitting current to flow between the metal and the semiconductor. The interface layer may include a layer of a passivating material (e.g., made from nitrogen, oxygen, oxynitride, arsenic, hydrogen and/or fluorine) and sometimes also includes a separation layer. In some cases, the interface layer may be a monolayer of a semiconductor passivating material. The interface layer thickness corresponds to a minimum specific contact resistance of less than or equal to $10 \Omega\text{-}\mu\text{m}^2$ or even less than or equal to $1 \Omega\text{-}\mu\text{m}^2$ for the electrical device.

Fig. 1



1002-47/273

Energy Scales for Metal - Semiconductor Junctions

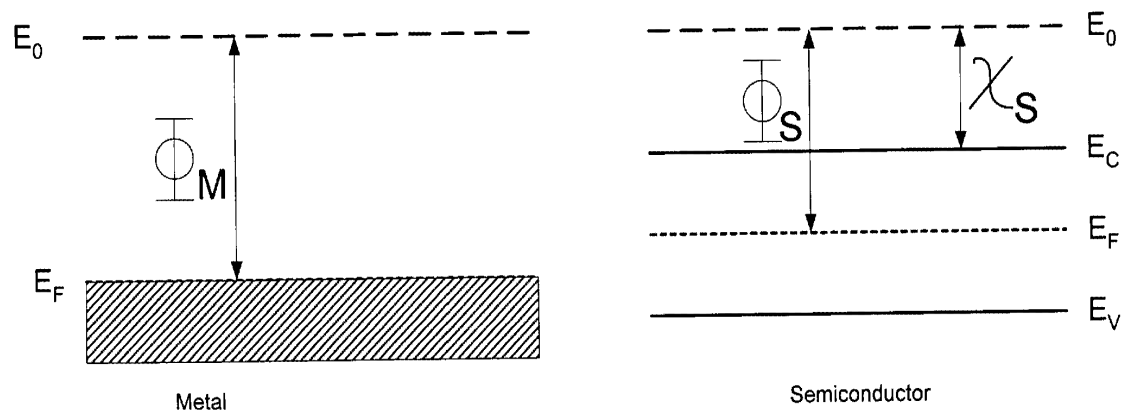


Fig. 2

10047553.001202

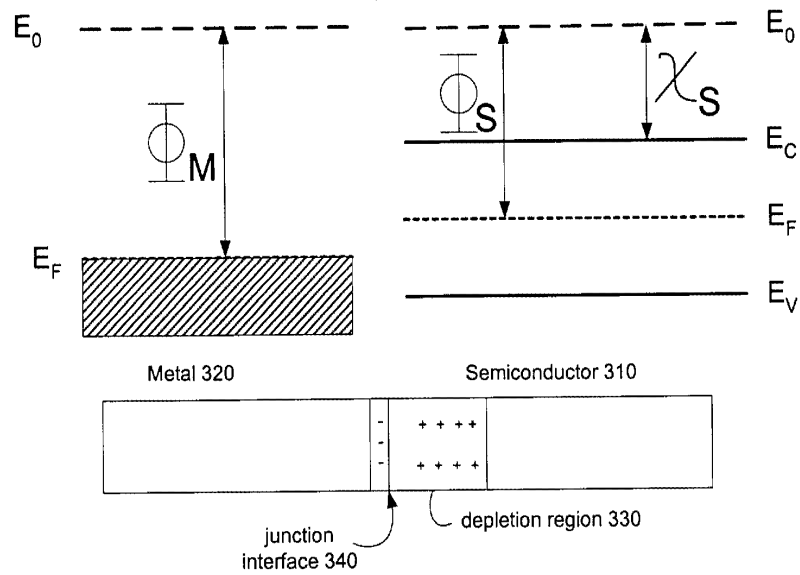


Fig. 3

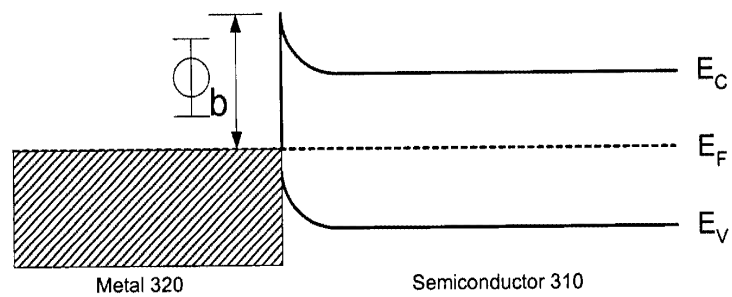


Fig. 4

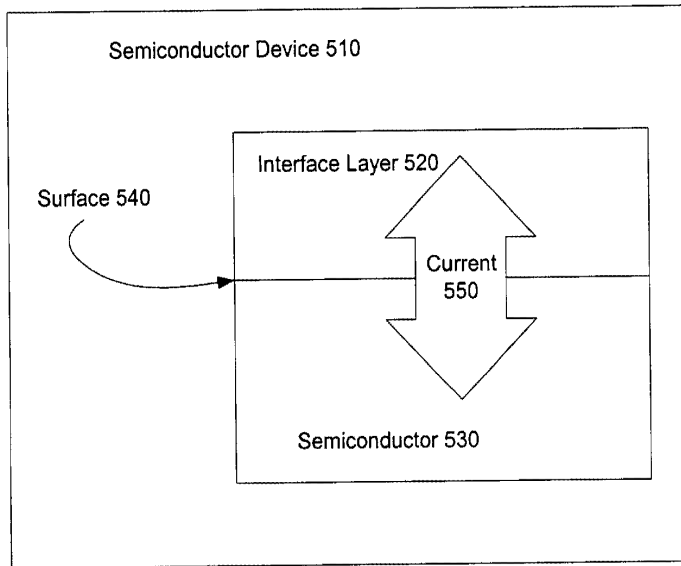


Fig. 5

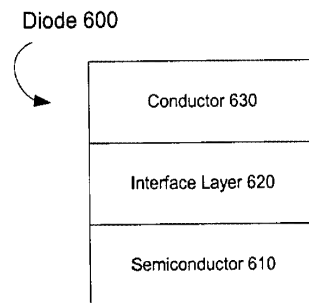
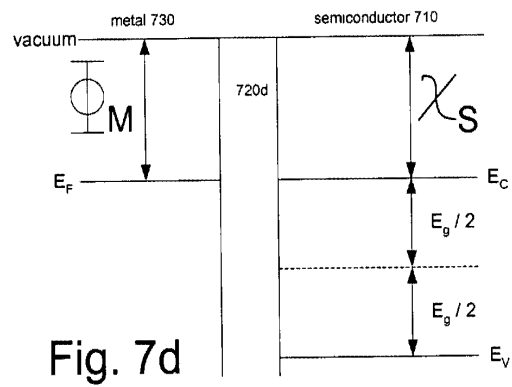
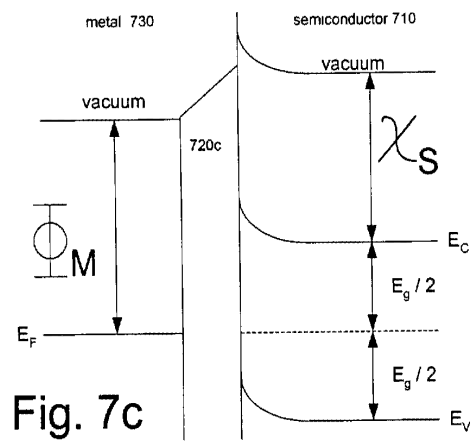
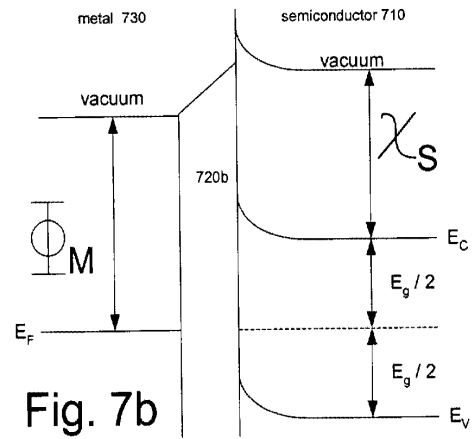
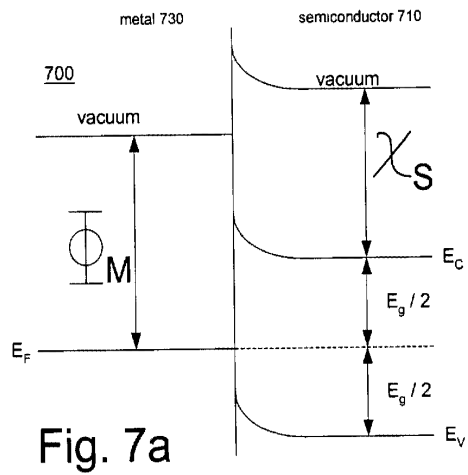


Fig. 6

2025 RELEASE UNDER E.O. 14176



2025 RELEASE UNDER E.O. 14176

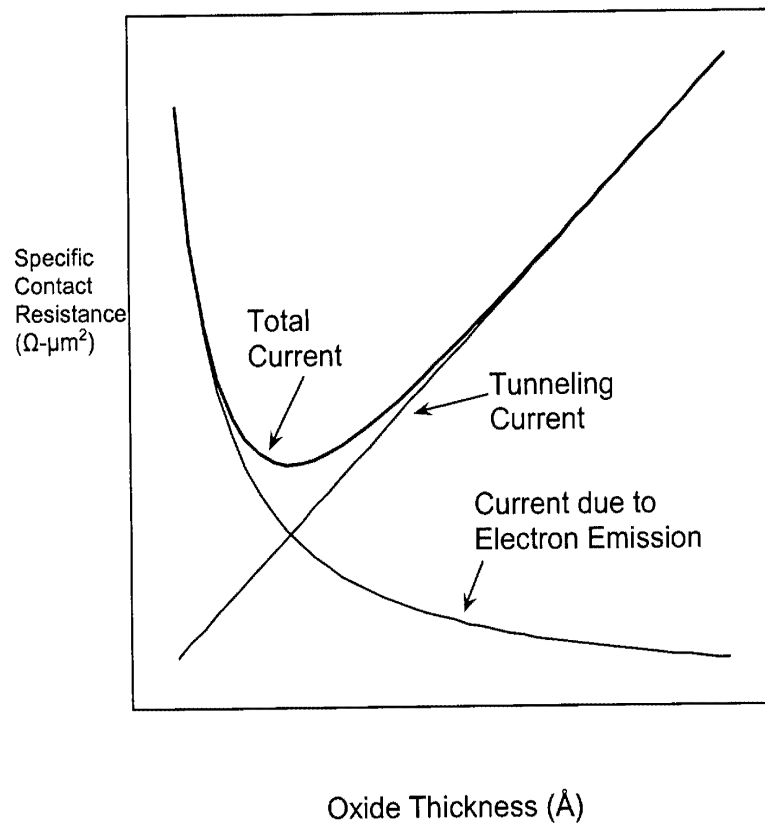


Fig. 8

10647438 UNCLASSIFIED

Attorney's Docket No.: 3771P003PatentDECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

the specification of which

 X

is attached hereto.

was filed on (MM/DD/YYYY)

as

United States Application Number

or PCT International Application Number

and was amended on (MM/DD/YYYY)

(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application. I do not know and do not believe that the claimed invention was in public use or on sale in the United States of America more than one year prior to this application, nor do I know or believe that the invention has been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

<u>Prior Foreign Application(s)</u>			<u>Priority Claimed</u>	
(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No
(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No
(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

(Application Number)	(Filing Date – MM/DD/YYYY)
(Application Number)	(Filing Date – MM/DD/YYYY)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	(Filing Date – MM/DD/YYYY)	(Status -- patented, pending, abandoned)
(Application Number)	(Filing Date – MM/DD/YYYY)	(Status -- patented, pending, abandoned)

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence Tarek N. Fahmi, Reg. No. 41,402 , BLAKELY, SOKOLOFF, TAYLOR &

(Name of Attorney or Agent)

ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to Tarek N. Fahmi, (408) 720-8300.

(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor DANIEL E. GRUPP

Inventor's Signature *DE Grupp* Date 8/7/02

Residence PALO ALTO, CA Citizenship USA
(City, State) (Country)

Post Office Address 334 LELAND AVE.

Full Name of Second/Joint Inventor DANIEL J. CONNELLY

Inventor's Signature *Daniel Connelly* Date 8 Aug 2002

Residence REDWOOD CITY CA Citizenship USA
(City, State) (Country)

Post Office Address 525 RUTHERFORD AVE

APPENDIX A

Ramin Aghevli, Reg. No. 43,462; William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. 42,261; W. Thomas Babbitt, Reg. No. 39,591; Jordan M. Becker, Reg. No. 39,602; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; R. Alan Burnett, Reg. No. 46,149; Daniel J. Burns, Reg. No. 50,222; Gregory D. Caldwell, Reg. No. 39,926; Thomas M. Coester, Reg. No. 39,637; Robert P. Cogan, Reg. No. 25,049; Donna Jo Coningsby, Reg. No. 41,684; Florin A. Corie, Reg. No. 46,244; Mimi D. Dao, Reg. No. 45,628; Stephen M. De Klerk, Reg. No. 46,503; Daniel M. De Vos, Reg. No. 37,813; Justin M. Dillon, Reg. No. 42,486; Sanjeet Dutta, Reg. No. 46,145; Tarek N. Fahmi, Reg. No. 41,402; Mark C. Farrell, Reg. No. 45,988; Thomas S. Ferrill, Reg. No. 42,532; Kyle H. Flindt, Reg. No. 42,539; George L. Fountain, Reg. No. 37,374; Andre M. Gibbs, Reg. No. 47,593; James Y. Go, Reg. No. 40,621; Mark A. Goldstein, Reg. No. 50,759; Alan E. Heimlich, Reg. No. 48,808; James A. Henry, Reg. No. 41,064; Willmore F. Holbrow III, Reg. No. 41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W. Hoover II, Reg. No. 32,992; Libby H. Hope, Reg. No. 46,774; Eric S. Hyman, Reg. No. 30,139; William W. Kidd, Reg. No. 31,772; Walter T. Kim, Reg. No. 42,731; Eric T. King, Reg. No. 44,188; Steve Laut, Reg. No. 47,736; Suk S. Lee, Reg. No. 47,745; Gordon R. Lindeen III, Reg. No. 33,192; Jan C. Little, Reg. No. 41,181; Julio Loza, Reg. No. 47,758; Joseph Lutz, Reg. No. 43,765; Lawrence Lycke, Reg. No. 38,540; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, Reg. No. 48,095; Raul D. Martinez, Reg. No. 46,904; Paul A. Mendonsa, Reg. No. 42,879; Clive D. Menezes, Reg. No. 45,493; Jonathan S. Miller, Reg. No. 48,534; Richard A. Nakashima, Reg. No. 42,023; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Robert B. O'Rourke, Reg. No. 46,972; Daniel E. Ovanezian, Reg. No. 41,236; Gregg A. Peacock, Reg. No. 45,001; Marina Portnova, Reg. No. 45,750; Michael A. Proksch, Reg. No. 43,021; William F. Ryann, Reg. No. 44,313; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Jeffrey S. Schubert, Reg. No. 43,098; Saina S. Shamilov, Reg. No. 48,266; Kevin G. Shao, Reg. No. 45,095; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Ronald S. Tamura, Reg. No. 43,179; Edwin H. Taylor, Reg. No. 25,129; Lance A. Termes, Reg. No. 43,184; John F. Travis, Reg. No. 43,203; Thomas J. Treutler, Reg. No. 51,126; Kerry D. Tweet, Reg. No. 45,959; Mark C. Van Ness, Reg. No. 39,865; Thomas A. Van Zandt, Reg. No. 43,219; Lester J. Vincent, Reg. No. 31,460; Archana B. Vittal, Reg. No. 45,182; Glenn E. Von Tersch, Reg. No. 41,364; John P. Ward, Reg. No. 40,216; Mark L. Watson, Reg. No. 46,322; Thomas C. Webster, Reg. No. 46,154; Linda S. Zachariah, Reg. No. 48,057; and Norman Zafman, Reg. No. 26,250; my patent attorneys, and William E. Hickman, Reg. No. 46,771, Brent E. Vecchia, Reg. No. 48,011, and Lehua Wang, Reg. No. 48,023; my patent agents, of BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and James R. Thein, Reg. No. 31,710, my patent attorney with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56 Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

- (1) Prior art cited in search reports of a foreign patent office in a counterpart application, and
- (2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

- (1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or
- (2) It refutes, or is inconsistent with, a position the applicant takes in:
 - (i) Opposing an argument of unpatentability relied on by the Office, or
 - (ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

- (1) Each inventor named in the application;
 - (2) Each attorney or agent who prepares or prosecutes the application; and
 - (3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.
- (d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.
- (e) In any continuation-in-part application, the duty under this section includes the duty to disclose to the Office all information known to the person to be material to patentability, as defined in paragraph (b) of this section, which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

08/12/02



U.S. PTO

Please type a plus sign (+) inside this box



Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PTO/SB/05 (03-01)

Approved for use through 10/31/2002. OMB 0651-0032

U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

**UTILITY
PATENT APPLICATION
TRANSMITTAL**

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 3771P003

First Inventor Daniel E. Grupp, et al.

Title Method For Depinning The Fermi Level of a Semiconductor at an Electrical

Express Mail Label No. EV060610698US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☐ Applicant claims small entity status.
See 37 CFR 1.27.
3. ☒ Specification [Total Pages 42]
(preferred arrangement set forth below)
- Descriptive title of the invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to sequence listing, a table,
or a computer program listing appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure
4. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 6]
5. Oath or Declaration (signed) [Total Pages 5]
a. ☐ Newly executed (original or copy)
b. ☐ Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 18 completed)
i. ☐ **DELETION OF INVENTOR(S)**
Signed statement attached deleting inventor(s)
named in the prior application, see 37 CFR
1.63(d)(2) and 1.33(b).
6. ☐ Application Data Sheet. See 37 CFR 1.76
7. ☐ CD-ROM or CD-R in duplicate, large table or
Computer Program (Appendix)
8. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all of the following are necessary)
a. ☐ Computer Readable Form (CRF)
b. Specification Sequence Listing on:
i. ☐ CD-ROM or CD-R (2 copies); or
ii. ☐ paper
c. ☐ Statements verifying identity of above copies
9. ☒ Assignment Papers (cover sheet & document(s))
10. ☐ 37 C.F.R. § 3.73(b) Statement ☒ Power of Attorney
(when there is an assignee)
11. ☐ English Translation Document (if applicable)
12. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
13. ☐ Preliminary Amendment
14. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
15. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16. ☒ Nonpublication Request under 35 U.S.C. 122 (b)(2)(B)(i).
Applicant must attach form PTO/SB/35 or its equivalent.
17. ☐ Other: _____

18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP)

of prior application No: _____

Prior application Information: Examiner _____

Group/Art Unit: _____

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

18. CORRESPONDENCE ADDRESS☒ Customer Number or Bar Code Label

08791

or ☒ Correspondence address below

Name	Tarek N. Fahmi					
	Blakely, Sokoloff, Taylor & Zafman LLP					
Address	12400 Wilshire Boulevard, Seventh Floor					
City	Los Angeles	State	California	Zip Code	90025-1030	
Country	USA	Telephone	(408) 947-8200	Fax	(408) 947-8280	

Name (Print/Type)	Tarek N. Fahmi	Registration No. (Attorney/Agent)	41,402
Signature		Date	08/12/02

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

PTO/SB/17(09/00)

Approved for use through 10/31/2002. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL FOR FY 2002**TOTAL AMOUNT OF PAYMENT (\$)** \$1,938.00**Complete if Known:**

Application No. Not Yet Assigned
Filing Date Herewith
First Named Inventor Daneil E. Grupp
Group Art Unit Not Yet Assigned
Examiner Name Not Yet Assigned
Attorney Docket No. 3771P003

METHOD OF PAYMENT (check one)

1. ☒ **The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:**

Deposit Account Number 02-2666
Deposit Account Name _____

- ☒ **Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17**

- ☐ **Applicant claims small entity status. See 37 CFR 1.27**

2. ☒ **Payment Enclosed:** ☒ **Check**
☐ **Money Order**
☐ **Other**

FEE CALCULATION**1. BASIC FILING FEE**

Large Entity		Small Entity		Fee Description	Fee Paid
Code	Fee (\$)	Code	Fee (\$)		
101	740	201	370	Utility application filing fee	\$740.00
106	330	206	165	Design application filing fee	_____
107	510	207	255	Plant filing fee	_____
108	740	208	370	Reissue filing fee	_____
114	160	214	80	Provisional application filing fee	_____
SUBTOTAL (1)					\$ 740.00

2. EXTRA CLAIM FEES

			Extra Claims	Fee from below	Fee Paid
Total Claims	<u>61</u>	- 20** =	<u>41</u>	X \$18	= \$738
Independent Claims	<u>8</u>	- 3** =	<u>5</u>	X \$84	= \$420
Multiple Dependent					= _____

**Or number previously paid, if greater; For Reissues, see below.

Large Entity		Small Entity		Fee Description
Code	Fee (\$)	Code	Fee (\$)	
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) \$ 1,158.00

FEE CALCULATION (continued)**3. ADDITIONAL FEES**

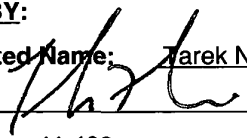
<u>Large Entity</u>		<u>Small Entity</u>		<u>Fee Description</u>	<u>Fee Paid</u>
<u>Fee Code</u>	<u>Fee (\$)</u>	<u>Fee Code</u>	<u>Fee (\$)</u>		
105	130	205	65	Surcharge - late filing fee or oath	_____
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	_____
139	130	139	130	Non-English specification	_____
147	2,520	147	2,520	For filing a request for ex parte reexamination	_____
099	8,800	099	8,800	Request for inter parties reexamination	_____
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	_____
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	_____
115	110	215	55	Extension for reply within first month	_____
116	400	216	200	Extension for reply within second month	_____
117	920	217	460	Extension for reply within third month	_____
118	1,440	218	720	Extension for reply within fourth month	_____
128	1,960	228	980	Extension for reply within fifth month	_____
119	320	219	160	Notice of Appeal	_____
120	320	220	160	Filing a brief in support of an appeal	_____
121	280	221	140	Request for oral hearing	_____
138	1,510	138	1,510	Petition to institute a public use proceeding	_____
140	110	240	55	Petition to revive - unavoidable	_____
141	1,280	241	640	Petition to revive - unintentional	_____
142	1,280	242	640	Utility issue fee (or reissue)	_____
143	460	243	230	Design issue fee	_____
144	620	244	310	Plant issue fee	_____
122	130	122	130	Petitions to the Commissioner	_____
123	50	123	50	Processing fee under 37 CFR 1.17(q)	_____
126	180	126	180	Submission of Information Disclosure Stmt	_____
581	40	581	40	Recording each patent assignment per property (times number of properties)	\$40
146	740	246	370	For filing a submission after final rejection (see 37 CFR 1.129(a))	_____
148	110	248	55	Statutory Disclaimer	_____
149	740	249	370	For each additional invention to be examined (see 37 CFR 1.129(b))	_____
179	740	279	370	Request for Continued Examination (RCE)	_____
169	900	169	900	Request for expedited examination of a design application	_____
195	300	195	300	Publication fee for early, voluntary, or normal pub.	_____
196	300	196	300	Publication fee for republication	_____
194	130	194	130	Request for voluntary publication or republication	_____
098	130	098	130	Processing fee under 37 CFR 1.17(i) (except provisionals)	_____
091	1,280	091	1,280	Acceptance of unintentionally delayed claim for priority	_____

Other fee (specify) _____

Other fee (specify) _____

SUBTOTAL (3) \$ 40.00

*Reduced by Basic Filing Fee Paid

SUBMITTED BY:Typed or Printed Name: Tarek N. FahmiSignature:  Date: August 12, 2002Reg. Number: 41,402 Telephone Number: 408.947.8200

**NONPUBLICATION REQUEST
UNDER
35 U.S.C. 122(b)(2)(B)(i)**

First Named Inventor	Daniel E. Grupp
Title	Method For Depinning The Fermi Level of a Semiconductor at an Electrical Junction and
Attorney Docket Number	3771P003

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing.

I hereby request that the attached application not be published under 35 U.S.C. 122(b).

08/12/02

Date


Signature

Tarek N. Fahmi, Reg. No. 41,402

Typed or printed name

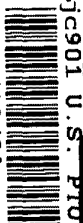
This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing**.

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 112(b)(2)(B)(iii)).**

Burden Hour Statement: This collection of information is required by 37 CFR 1.213(a). This information is used by the public to request that an application not be published under 35 U.S.C. 122(b) (and the PTO to process that request). Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This form is estimated to take 6 minutes to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

08/12/02



U.S. PTO

Please type a plus sign (+) inside this box



Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PTO/SB/05 (03-01)

Approved for use through 10/31/2002. OMB 0651-0032

U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

**UTILITY
PATENT APPLICATION
TRANSMITTAL**

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 3771P003

First Inventor Daniel E. Grupp, et al.

Title Method For Depinning The Fermi Level of a Semiconductor at an Electrical

Express Mail Label No. EV060610698US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☐ Applicant claims small entity status.
See 37 CFR 1.27.
3. ☒ Specification [Total Pages 42]
(preferred arrangement set forth below)
- Descriptive title of the invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to sequence listing, a table,
or a computer program listing appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure
4. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 6]
5. Oath or Declaration (signed) [Total Pages 5]
a. ☐ Newly executed (original or copy)
b. ☐ Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 18 completed)
i. ☐ **DELETION OF INVENTOR(S)**
Signed statement attached deleting inventor(s)
named in the prior application, see 37 CFR
1.63(d)(2) and 1.33(b).
6. ☐ Application Data Sheet. See 37 CFR 1.76
7. ☐ CD-ROM or CD-R in duplicate, large table or
Computer Program (Appendix)
8. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all of the following are necessary)
a. ☐ Computer Readable Form (CRF)
b. Specification Sequence Listing on:
i. ☐ CD-ROM or CD-R (2 copies); or
ii. ☐ paper
c. ☐ Statements verifying identity of above copies
9. ☒ Assignment Papers (cover sheet & document(s))
10. ☐ 37 C.F.R. § 3.73(b) Statement ☒ Power of Attorney
(when there is an assignee)
11. ☐ English Translation Document (if applicable)
12. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
13. ☐ Preliminary Amendment
14. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
15. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16. ☒ Nonpublication Request under 35 U.S.C. 122 (b)(2)(B)(i).
Applicant must attach form PTO/SB/35 or its equivalent.
17. ☐ Other: _____

18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP)

of prior application No: _____

Prior application Information: Examiner _____

Group/Art Unit: _____

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

18. CORRESPONDENCE ADDRESS☒ Customer Number or Bar Code Label

08791

or ☒ Correspondence address below

Name	Tarek N. Fahmi					
	Blakely, Sokoloff, Taylor & Zafman LLP					
Address	12400 Wilshire Boulevard, Seventh Floor					
City	Los Angeles	State	California	Zip Code	90025-1030	
Country	USA	Telephone	(408) 947-8200	Fax	(408) 947-8280	

Name (Print/Type)	Tarek N. Fahmi	Registration No. (Attorney/Agent)	41,402
Signature		Date	08/12/02

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

PTO/SB/17(09/00)

Approved for use through 10/31/2002. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL FOR FY 2002**TOTAL AMOUNT OF PAYMENT (\$)** \$1,938.00**Complete if Known:**

Application No. Not Yet Assigned
Filing Date Herewith
First Named Inventor Daneil E. Grupp
Group Art Unit Not Yet Assigned
Examiner Name Not Yet Assigned
Attorney Docket No. 3771P003

METHOD OF PAYMENT (check one)

1. ☒ **The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:**

Deposit Account Number 02-2666
Deposit Account Name _____

- ☒ **Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17**

- ☐ **Applicant claims small entity status. See 37 CFR 1.27**

2. ☒ **Payment Enclosed:** ☒ **Check**
☐ **Money Order**
☐ **Other**

FEE CALCULATION**1. BASIC FILING FEE**

Large Entity		Small Entity		Fee Description	Fee Paid
Code	Fee (\$)	Code	Fee (\$)		
101	740	201	370	Utility application filing fee	\$740.00
106	330	206	165	Design application filing fee	_____
107	510	207	255	Plant filing fee	_____
108	740	208	370	Reissue filing fee	_____
114	160	214	80	Provisional application filing fee	_____
SUBTOTAL (1)					\$ 740.00

2. EXTRA CLAIM FEES

			Extra Claims	Fee from below	Fee Paid
Total Claims	<u>61</u>	- 20** =	<u>41</u>	X \$18	= \$738
Independent Claims	<u>8</u>	- 3** =	<u>5</u>	X \$84	= \$420
Multiple Dependent					= _____

**Or number previously paid, if greater; For Reissues, see below.

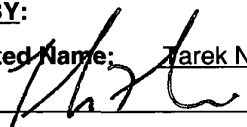
Large Entity		Small Entity		Fee Description
Code	Fee (\$)	Code	Fee (\$)	
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) \$ 1,158.00

FEE CALCULATION (continued)**3. ADDITIONAL FEES**

<u>Large Entity</u>		<u>Small Entity</u>		<u>Fee Description</u>	<u>Fee Paid</u>
<u>Fee Code</u>	<u>Fee (\$)</u>	<u>Fee Code</u>	<u>Fee (\$)</u>		
105	130	205	65	Surcharge - late filing fee or oath	_____
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	_____
139	130	139	130	Non-English specification	_____
147	2,520	147	2,520	For filing a request for ex parte reexamination	_____
099	8,800	099	8,800	Request for inter parties reexamination	_____
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	_____
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	_____
115	110	215	55	Extension for reply within first month	_____
116	400	216	200	Extension for reply within second month	_____
117	920	217	460	Extension for reply within third month	_____
118	1,440	218	720	Extension for reply within fourth month	_____
128	1,960	228	980	Extension for reply within fifth month	_____
119	320	219	160	Notice of Appeal	_____
120	320	220	160	Filing a brief in support of an appeal	_____
121	280	221	140	Request for oral hearing	_____
138	1,510	138	1,510	Petition to institute a public use proceeding	_____
140	110	240	55	Petition to revive - unavoidable	_____
141	1,280	241	640	Petition to revive - unintentional	_____
142	1,280	242	640	Utility issue fee (or reissue)	_____
143	460	243	230	Design issue fee	_____
144	620	244	310	Plant issue fee	_____
122	130	122	130	Petitions to the Commissioner	_____
123	50	123	50	Processing fee under 37 CFR 1.17(q)	_____
126	180	126	180	Submission of Information Disclosure Stmt	_____
581	40	581	40	Recording each patent assignment per property (times number of properties)	\$40
146	740	246	370	For filing a submission after final rejection (see 37 CFR 1.129(a))	_____
148	110	248	55	Statutory Disclaimer	_____
149	740	249	370	For each additional invention to be examined (see 37 CFR 1.129(b))	_____
179	740	279	370	Request for Continued Examination (RCE)	_____
169	900	169	900	Request for expedited examination of a design application	_____
195	300	195	300	Publication fee for early, voluntary, or normal pub.	_____
196	300	196	300	Publication fee for republication	_____
194	130	194	130	Request for voluntary publication or republication	_____
098	130	098	130	Processing fee under 37 CFR 1.17(i) (except provisionals)	_____
091	1,280	091	1,280	Acceptance of unintentionally delayed claim for priority	_____
Other fee (specify) _____					_____
Other fee (specify) _____					_____
SUBTOTAL (3)					\$ 40.00

*Reduced by Basic Filing Fee Paid

SUBMITTED BY:Typed or Printed Name: Tarek N. FahmiSignature:  Date: August 12, 2002Reg. Number: 41,402 Telephone Number: 408.947.8200

**NONPUBLICATION REQUEST
UNDER
35 U.S.C. 122(b)(2)(B)(i)**

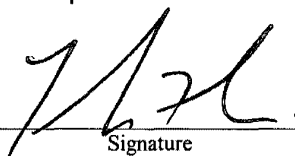
First Named Inventor	Daniel E. Grupp
Title	Method For Depinning The Fermi Level of a Semiconductor at an Electrical Junction and
Attorney Docket Number	3771P003

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing.

I hereby request that the attached application not be published under 35 U.S.C. 122(b).

08/12/02

Date


Signature

Tarek N. Fahmi, Reg. No. 41,402

Typed or printed name

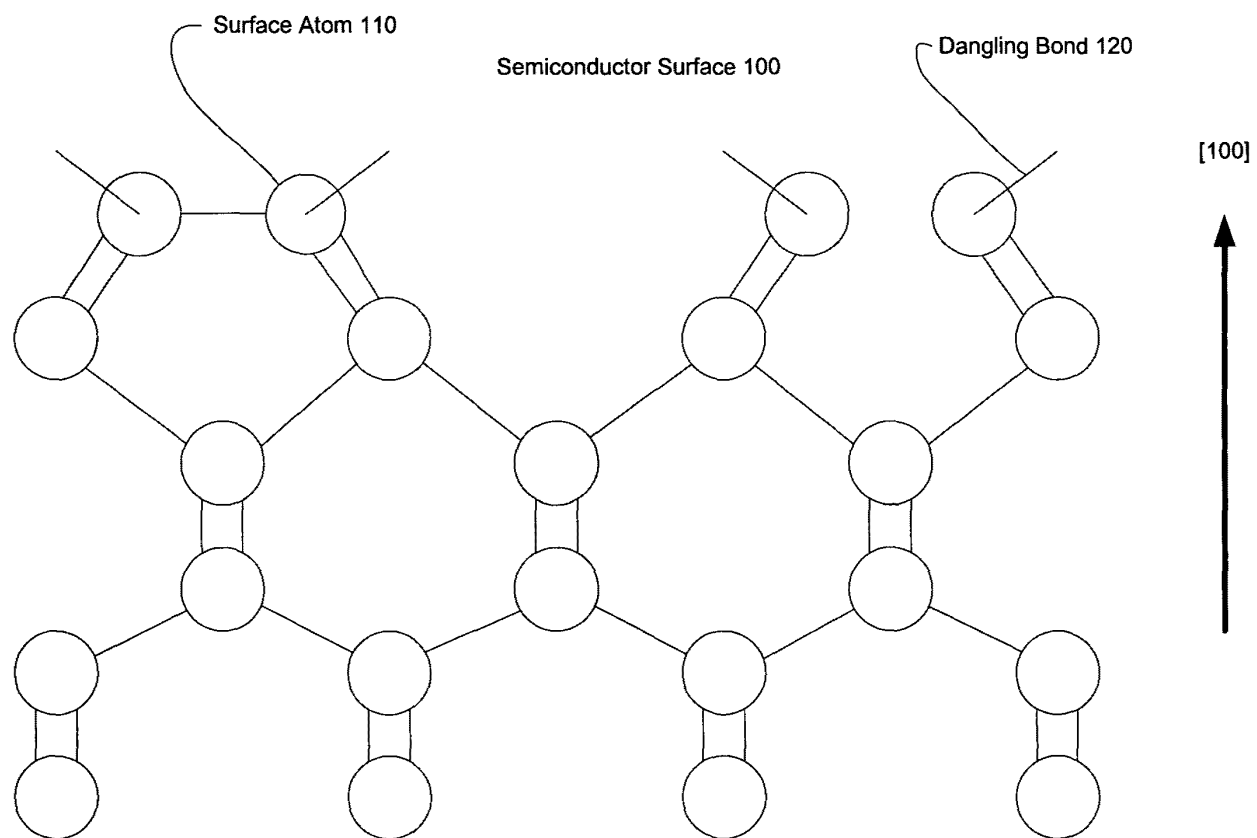
This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing**.

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 112(b)(2)(B)(iii)).**

Burden Hour Statement: This collection of information is required by 37 CFR 1.213(a). This information is used by the public to request that an application not be published under 35 U.S.C. 122(b) (and the PTO to process that request). Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This form is estimated to take 6 minutes to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Fig. 1



Energy Scales for Metal - Semiconductor Junctions

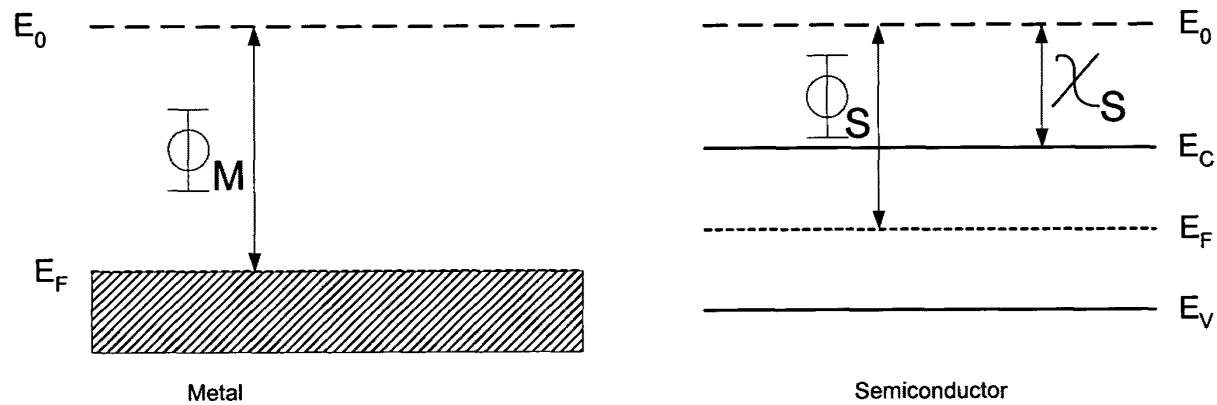


Fig. 2

1024750-024202

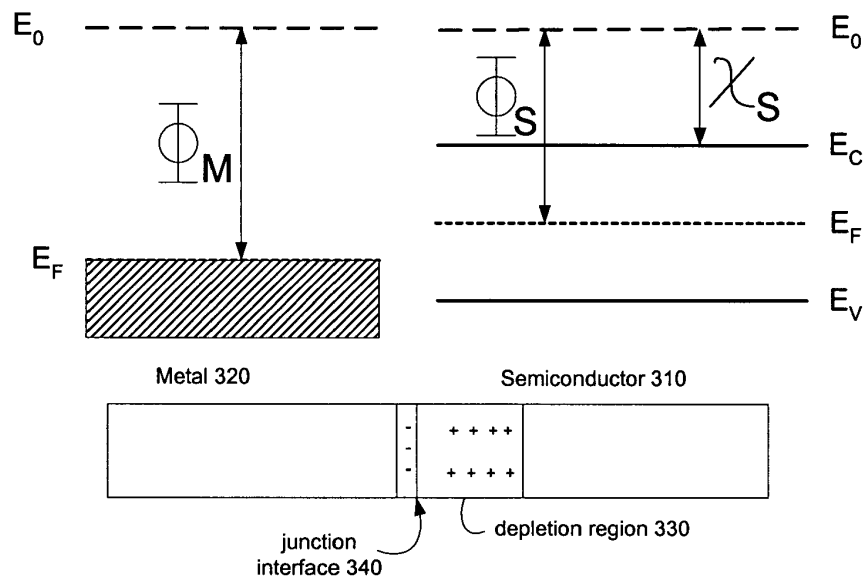


Fig. 3

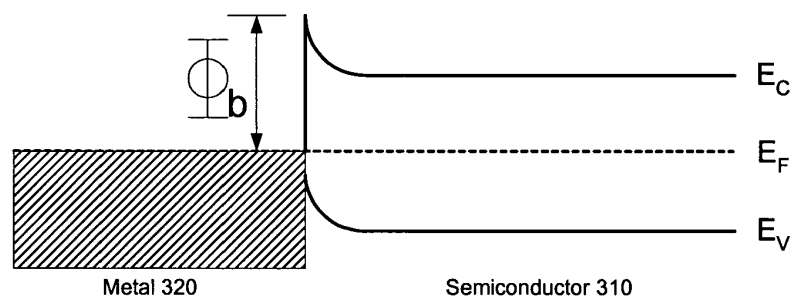


Fig. 4

10247753.064202
20210929 09:27:01

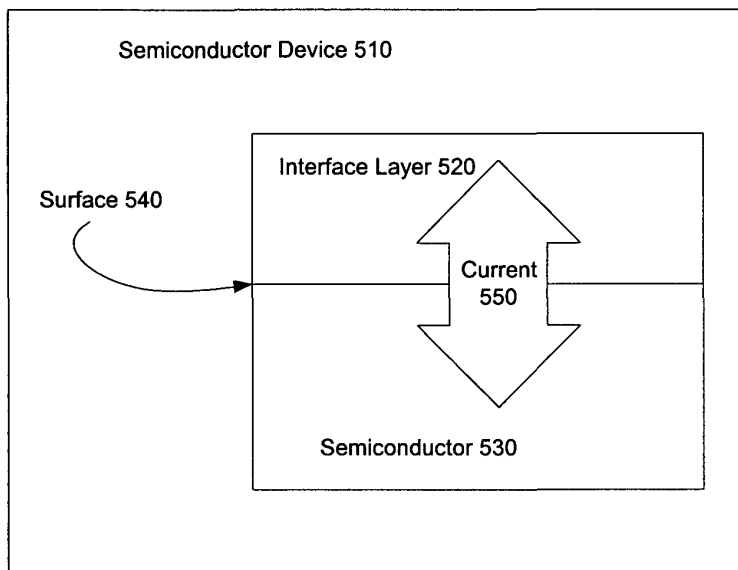


Fig. 5

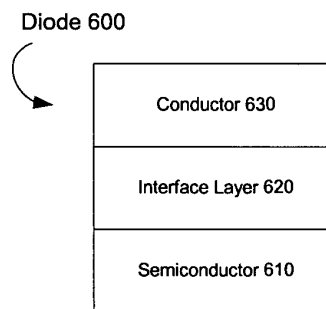
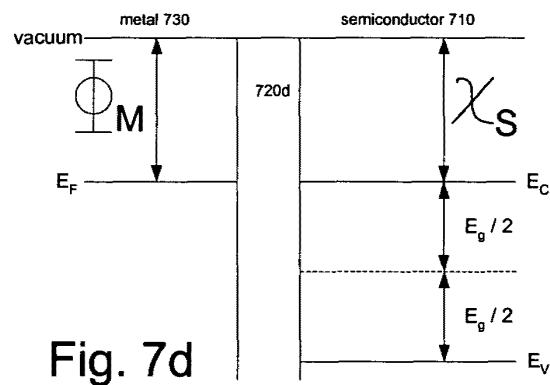
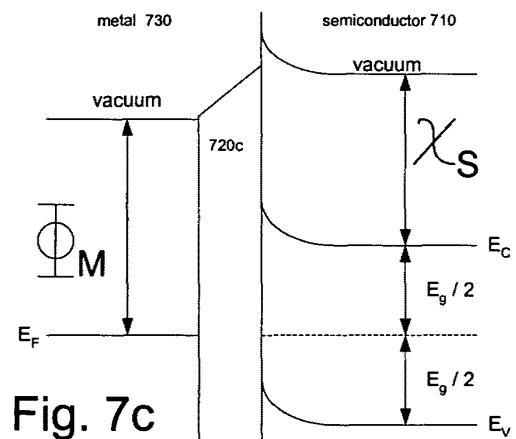
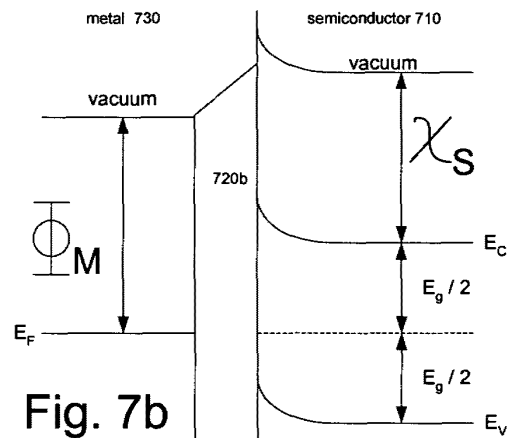
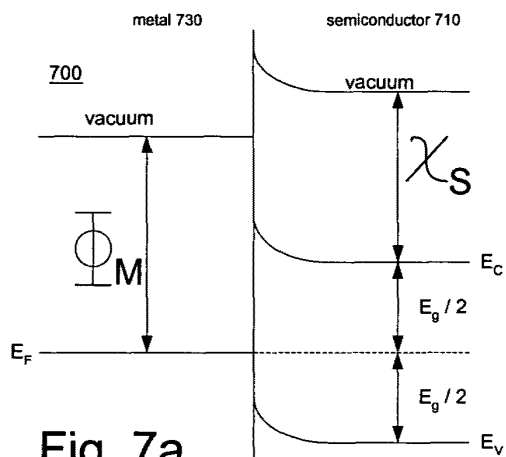


Fig. 6



1021758-021202

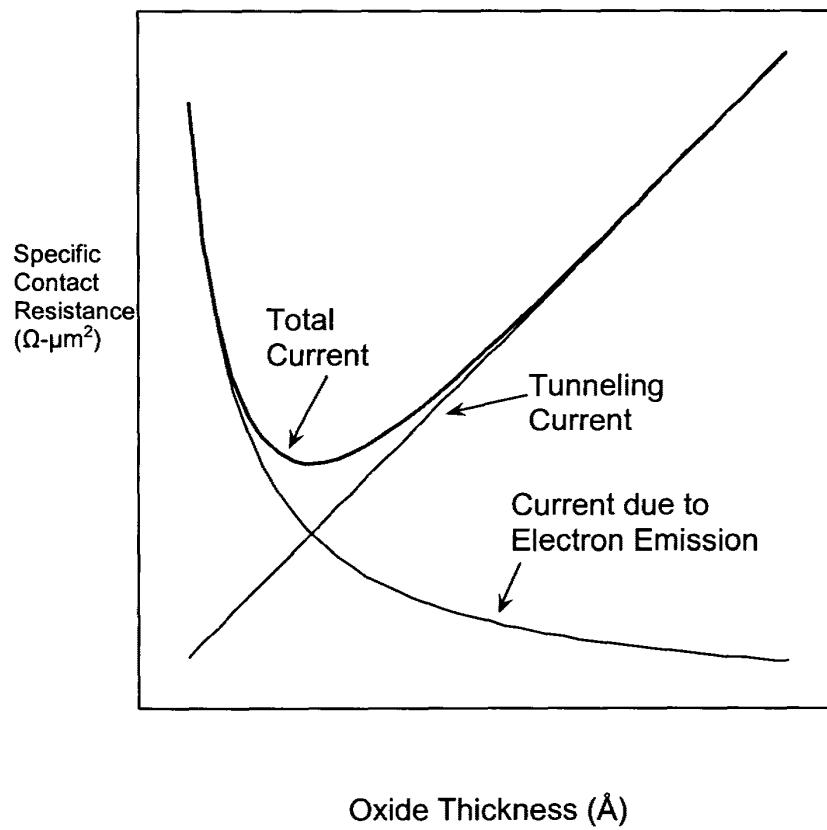


Fig. 8

1064758-034202

Attorney Docket No.: 03771P003

Patent Application

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL
JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS**

INVENTORS

**DANIEL E. GRUPP
DANIEL J. CONNELLY**

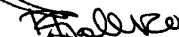
Prepared by

**BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1026
408-947-8200****EXPRESS MAIL CERTIFICATE OF MAILING**"Express Mail" mailing label number: EV060610698USDate of Deposit: August 12, 2002

I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Commissioner of Patents and Trademarks, Washington, D. C. 20231

Patricia A. Balero

(Typed or printed name of person mailing paper or fee)



(Signature of person mailing paper or fee)

**METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL
JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS**

RELATED APPLICATIONS

[0001] The present application is related to co-pending U.S. Patent Application No.____
_____, entitled "INSULATED GATE FIELD EFFECT TRANSISTOR HAVING
PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL", filed on_____,
2002, by the present inventors and assigned to the same assignee as the present application.
This related patent application is hereby incorporated by reference in its entirety.

FIELD OF THE INVENTION

[0002] The invention relates generally to semiconductor processing and semiconductor
devices. More particularly, the invention relates to a process for depinning the Fermi level of
a semiconductor at a metal-interface layer-semiconductor junction and to devices that employ
such a junction.

BACKGROUND

[0003] One of the most basic electrical junctions used in modern devices is the metal-
semiconductor junction. In these junctions, a metal (such as aluminum) is brought in contact
with a semiconductor (such as silicon). This forms a device (a diode) which can be inherently
rectifying; that is, the junction will tend to conduct current in one direction more favorably
than in the other direction. In other cases, depending on the materials used, the junction may
be ohmic in nature (i.e., the contact may have negligible resistance regardless of the direction
of current flow). Grondahl and Geiger first studied the rectifying form of these junctions in

1926, and by 1938 Schottky had developed a theoretical explanation for the rectification that was observed.

[0004] Schottky's theory explained the rectifying behavior of a metal-semiconductor contact as depending on a barrier at the surface of contact between the metal and the semiconductor. In this model, the height of the barrier (as measured by the potential necessary for an electron to pass from the metal to the semiconductor) was postulated as the difference between the work function of the metal (the work function is the energy required to free an electron at the Fermi level of the metal, the Fermi level being the highest occupied energy state of the metal at $T = 0$) and the electron affinity of the semiconductor (the electron affinity is the difference between the energy of a free electron and the conduction band edge of the semiconductor). Expressed mathematically:

$$\phi_B = \phi_M - \chi_s \quad [1]$$

where Φ_B is the barrier height, Φ_M is the work function of the metal and χ_s is the electron affinity of the semiconductor.

[0005] Not surprisingly, many attempts were made to verify this theory experimentally. If the theory is correct, one should be able to observe direct variations in barrier heights for metals of different work functions when put in contact with a common semiconductor. What is observed, however, is not direct scaling, but instead only a much weaker variation of barrier height with work function than implied by the model.

[0006] Bardeen sought to explain this difference between theoretical prediction and experimental observation by introducing the concept that surface states of the semiconductor play a role in determining the barrier height. Surface states are energy states (within the bandgap between the valence and conduction bands) at the edge of the semiconductor crystal that arise from incomplete covalent bonds, impurities, and other effects of crystal termination. **Figure 1** shows a cross-section of an un-passivated silicon surface labeled 100. The particular silicon surface shown is an Si(100) 2x1 surface. As shown, the silicon atoms at the surface, such as atom 110, are not fully coordinated and contain un-satisfied dangling bonds, such as

dangling bond 120. These dangling bonds may be responsible for surface states that trap electrical charges.

[0007] Bardeen's model assumes that surface states are sufficient to pin the Fermi level in the semiconductor at a point between the valence and conduction bands. If true, the barrier height at a metal-semiconductor junction should be independent of the metal's work function. This condition is rarely observed experimentally, however, and so Bardeen's model (like Schottky's) is best considered as a limiting case.

[0008] For many years, the cause underlying the Fermi level pinning of the semiconductor at a metal-semiconductor junction remained unexplained. Indeed, to this day no one explanation satisfies all experimental observations regarding such junctions. Nevertheless, in 1984, Tersoff proposed a model that goes a long way towards explaining the physics of such junctions. See J. Tersoff, "Schottky Barrier Heights and the Continuum of Gap States," Phys. Rev. Lett. 52 (6), Feb. 6, 1984.

[0009] Tersoff's model (which is built on work by Heine and Flores & Tejedor, and see also Louie, Chelikowsky, and Cohen, "Ionicity and the theory of Schottky barriers," Phys. Rev. B 15, 2154 (1977)) proposes that the Fermi level of a semiconductor at a metal-semiconductor interface is pinned near an effective "gap center", which is related to the bulk semiconductor energy band structure. The pinning is due to so-called metal induced gap states (MIGS), which are energy states in the bandgap of the semiconductor that become populated due to the proximity of the metal. That is, the wave functions of the electrons in the metal do not terminate abruptly at the surface of the metal, but rather decay in proportion to the distance from that surface (i.e., extending inside the semiconductor). To maintain the sum rule on the density of states in the semiconductor, electrons near the surface occupy energy states in the gap derived from the valence band such that the density of states in the valence band is reduced. To maintain charge neutrality, the highest occupied state (which defines the Fermi level of the semiconductor) will then lie at the crossover point from states derived from the valence band to those derived from the conduction band. This crossover occurs at the branch

point of the band structure. Although calculations of barrier heights based on Tersoff's model do not satisfy all experimentally observed barrier heights for all metal-semiconductor junctions, there is generally good agreement for a number of such junctions.

[0010] One final source of surface effects on diode characteristics is inhomogeneity. That is, if factors affecting the barrier height (e.g., density of surface states) vary across the plane of the junction, the resulting properties of the junction are found not to be a linear combination of the properties of the different regions. In summary then, a classic metal-semiconductor junction is characterized by a Schottky barrier, the properties of which (e.g., barrier height) depend on surface states, MIGS and inhomogeneities.

[0011] The importance of the barrier height at a metal-semiconductor interface is that it determines the electrical properties of the junction. Thus, if one were able to control or adjust the barrier height of a metal-semiconductor junction, one could produce electrical devices of desired characteristics. Such barrier height tuning may become even more important as device sizes shrink even further. Before one can tune the barrier height, however, one must depin the Fermi level of the semiconductor. As discussed in detail below, the present inventors have achieved this goal in a device that still permits substantial current flow between the metal and the semiconductor.

SUMMARY OF THE INVENTION

[0012] The present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal – interface layer – semiconductor junction, there exist corresponding minimum specific contact resistances. The interface layer thickness corresponding to this minimum specific contact resistance will vary depending upon the materials used, however, it is a thickness that allows for depinning the Fermi level of the semiconductor while still permitting current to flow between the metal and the semiconductor when the junction is biased (e.g., forward or reverse biased). By depinning the Fermi level, the present inventors mean a condition wherein all, or substantially all, dangling bonds that may otherwise be present at the semiconductor surface have been terminated, and the effect of MIGS has been overcome, or at least reduced, by displacing the semiconductor a sufficient distance from the metal. Minimum specific contact resistances of less than or equal to approximately $10 \Omega - \mu m^2$ or even less than or equal to approximately $1 \Omega - \mu m^2$ may be achieved for such junctions in accordance with the present invention.

[0013] Thus, in one embodiment, the present invention provides an electrical device in which an interface layer is disposed between and in contact with a metal and a silicon-based semiconductor and is configured to depin the Fermi level of the semiconductor while still permitting current flow between the metal and the semiconductor when the electrical device is biased. The specific contact resistance of the electrical device is less than approximately $10 \Omega - \mu m^2$. The interface layer may include a passivating material (e.g., a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride) and sometimes also includes a separation layer. In some cases, the interface layer may be essentially a monolayer (or several monolayers) of a semiconductor passivating material.

[0014] In another embodiment, the interface layer is made up of a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material, for example ammonia

(NH₃), nitrogen (N₂) or unbound gaseous nitrogen (N) generated from a plasma process. In such cases, the interface layer may be fabricated by heating the semiconductor while in a vacuum chamber and exposing the semiconductor to the nitrogenous material.

[0015] A further embodiment of the present invention provides for depinning the Fermi level of a semiconductor in an electrical junction through the use of an interface layer disposed between a surface of the semiconductor and a conductor. The interface layer preferably (i) is of a thickness sufficient to reduce effects of MIGS in the semiconductor, and (ii) passivates the surface of the semiconductor. Despite the presence of the interface layer, significant current may flow between the conductor and the semiconductor because the thickness of the interface layer may be chosen to provide a minimum (or near minimum) specific contact resistance for the junction. As indicated above, the interface layer may include a passivating material such as a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride.

[0016] Further embodiments of the present invention provide a junction between a semiconductor and a conductor separated from the semiconductor by an interface layer configured to allow a Fermi level of the conductor to (i) align with a conduction band of the semiconductor, (ii) align with a valence band of the semiconductor, or (iii) to be independent of the Fermi level of the semiconductor. In some or all of these cases, current may flow between the conductor and the semiconductor when the junction is biased because the interface layer has a thickness corresponding to a minimum or near minimum specific contact resistance for the junction. For example, specific contact resistances of less than or equal to approximately $2500 \Omega - \mu m^2$, $1000 \Omega - \mu m^2$, $100 \Omega - \mu m^2$, $50 \Omega - \mu m^2$, $10 \Omega - \mu m^2$ or even less than or equal to $1 \Omega - \mu m^2$ may be achieved.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0017] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0018] **Figure 1** shows a cross-section of an un-passivated silicon surface containing surface silicon atoms with dangling bonds.

[0019] **Figure 2** illustrates various energy levels for metals and semiconductors and is labeled to show the work function of a metal and the electron affinity of a semiconductor.

[0020] **Figure 3** shows an energy band diagram for a conventional metal – *n*-type semiconductor junction and also illustrates the concept of a depletion region formed in the semiconductor when the materials are brought into contact with one another.

[0021] **Figure 4** illustrates band bending at a conventional metal – *n*-type semiconductor junction.

[0022] **Figure 5** shows a semiconductor device containing a semiconductor material having a surface across which electrical current flows during operation of the semiconductor device, and containing an interface layer formed on the surface according to one embodiment of the present invention.

[0023] **Figure 6** shows an electrical junction containing an interface layer that is disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

[0024] **Figures 7a, 7b, 7c and 7d** show relationships between Fermi energy, conduction-band energy, and valence-band energy for an unpassivated Schottky diode, a passivated Schottky diode in which MIGS are not removed, an unpassivated Schottky diode in which

MIGS are removed and a passivated Schottky diode in which MIGS are removed according to one embodiment of the present invention, respectively.

[0025] **Figure 8** shows a curve of interface layer resistance versus interface layer thickness for an electrical junction containing an interface layer disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

[0026] Described herein are processes for depinning the Fermi level of a silicon-based semiconductor (e.g., Si, SiC or SiGe) at a metal-semiconductor junction as well as devices that use such a junction. As more fully discussed below, an interface layer is introduced between the semiconductor and the metal. The interface layer functions to passivate the semiconductor surface (that is, terminate dangling bonds that may otherwise be present at the semiconductor surface so as to assure chemical stability of the surface) and to displace the semiconductor from the metal so as to reduce the effect of MIGS.

[0027] As discussed more fully below, the present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal – interface layer – semiconductor junction, there exist corresponding minimum specific contact resistances. Indeed, minimum specific contact resistances of less than or equal to approximately $10 \Omega - \mu m^2$ or even less than or equal to approximately $1 \Omega - \mu m^2$ may be achieved for such junctions in accordance with the present invention. To achieve such low contact resistances, a metal that has a work function near the conduction band of the semiconductor for n-type semiconductors, or a work function that is near the valence band for p-type semiconductors, is selected.

[0028] The Schottky barrier in such junctions is already minimized, meaning that it is much less than the Schottky barrier presented by a junction in which the Fermi level is pinned, generally near the middle of the semiconductor's bandgap. The current versus voltage (IV) characteristic of these junctions is non-linear, generally having a slope that increases as the voltage increases, such that the derivative of current with respect to voltage is increasing with voltage. This results in a decreasing differential resistance (dV/dI) and a decreasing resistance (V/I). Thus, a junction that has high resistance or high differential resistance near the origin of the IV characteristic (zero volts) may have significantly lower resistance or lower differential resistance at higher voltages.

[0029] The present invention achieves low resistance and low differential resistance near the origin of the current-voltage characteristic for a metal – interface layer – semiconductor junction. Generally, the voltage around the origin should be less than about 100 mV, or more preferably less than about 10 mV for purposes of measuring, determining, or utilizing such junctions of low resistance. At higher voltages, the junction resistance will be even lower. It is thus a feature of the present invention to set an upper bound on the resistance of a contact, where the upper bound occurs at low voltages.

[0030] It is further noted that in junctions where the Schottky barrier is minimized as described above, such that the Fermi level at the junction interface at zero volts lies at or near the conduction band edge or valence band edge (for *n*- and *p*-type semiconductors, respectively), the *IV* characteristic will be nearly symmetric, especially at low voltage. In this case, the term “forward bias” is not defined in the usual sense of a diode wherein forward bias corresponds to the direction of bias for which greater current flows. Thus, in determining or utilizing low resistance junctions of the present invention, the voltage may be either positive or negative.

[0031] It is also possible (in accordance with a further embodiment of the present invention) to make junctions where the Schottky barrier is higher than it would be if the Fermi level at the junction interface were pinned, usually around mid-gap of the semiconductor. Such junctions are formed in the present invention between a metal with a workfunction near or substantially equal to the conduction band edge of a *p*-type semiconductor, or between a metal with a workfunction near or substantially equal to the valence band edge of an *n*-type semiconductor. These junctions are diodes, in that little current will flow if the *n*-type (*p*-type) semiconductor is biased positive (negative) with respect to the metal, and large currents will flow if the voltage is reversed. The low-current flow state is referred to as reverse bias, and the high-current flow state is referred to as positive bias.

[0032] Low resistance in the case of a diode is only relevant in forward bias conditions. In junctions created in accordance with the present invention the resistance contribution of the

interface layer is smaller than the resistance due to the Schottky barrier. That is, in forward bias conditions for junctions created in accordance with the present invention, the transport of charge is limited mainly by the thermal emission of carriers from the semiconductor over the barrier at the interface, and not by the tunneling through the interface dielectric. Thus, low resistance in the case of a diode refers to a resistance lower than the resistance presented by the Schottky barrier.

[0033] In certain applications of diodes, the ability to withstand high reverse biases may be more desirable than high current flow in forward bias. These applications would be considered high voltage/low power applications. In such cases, a low resistance is not essential, and junctions created in accordance with still another embodiment of the present invention provide high-voltage diodes capable of withstanding voltages higher than could otherwise be achieved if the Fermi level of the semiconductor in the junction were pinned.

[0034] The present invention is discussed below in terms of presently preferred embodiments thereof, however, this discussion is not meant to limit the scope of the invention. By studying the present disclosure, others of ordinary skill in the art may recognize equivalent procedures, materials or structures that can be substituted for those described herein to achieve the same effect. The reader is advised and reminded that the use of such equivalents is deemed to be within the scope of the present invention. For example, where the discussion refers to well-known structures and devices, block diagrams are used, in part to demonstrate the broad applicability of the present invention to a wide range of such structures and devices.

I. Introduction and Definitions

[0035] The present discussion makes use of terms that, although well known in the art, may not be familiar to all readers. Therefore, before beginning a detailed discussion of the present invention, it is helpful to define certain terms and concepts. To understand the properties of metal-semiconductor junctions and the impact of the present invention, one must refer to some important energy scales, which are shown graphically in **Figure 2**. The so-called vacuum

level (E_0) represents the minimum energy that an electron needs to possess in order to completely free itself from a metal or semiconductor. For a metal, the Fermi level (E_F) represents the highest occupied energy level for the material. That is, nearly all energy states below the Fermi level are filled, while nearly all states above the Fermi level are empty. The work function of the metal (Φ_M) is then defined as the energy required to free an electron at the Fermi level and mathematically it is the difference between the vacuum level and the Fermi level. The work function is an invariant bulk property of the metal.

[0036] As illustrated in the diagram, semiconductors also have a Fermi level (E_F) and a work function (Φ_S), however, the work function is not an invariant property of the semiconductor. Because the Fermi level varies depending on the doping level in the semiconductor (i.e., the relative amounts of impurities introduced into the semiconductor crystal which change the electron and hole carrier concentrations), a separate parameter, the electron affinity (χ_S), is defined. The electron affinity is an invariant property of the semiconductor and is the difference between the vacuum level and the conduction band edge of the semiconductor. In a semiconductor, almost all energy states are filled in the valence band (E_V) while the conduction band (E_C) is almost empty.

[0037] Now consider a conventional junction between a metal and an n -type semiconductor that has a work function smaller than the work function of the metal (i.e., $\Phi_S < \Phi_M$). An n -type semiconductor is one in which electrons are the majority charge carriers (in p -type semiconductors, holes are the majority charge carrier). As shown in **Figure 3**, because the Fermi level in the semiconductor is higher than the Fermi level in the metal, electrons transfer from the semiconductor 310 to the metal 320 when the materials are brought into contact. Thus, a depletion region (i.e., a region in which there are no free charge carriers) 330 forms near the junction interface 340.

[0038] The formation of the depletion region gives rise to an electric field and so-called "band bending", as one approaches the junction interface from the semiconductor side (see **Figure 4**). The band bending creates an energy barrier (discussed above) that blocks further

transfer of electrons into or out of the semiconductor. Similar barriers are formed for a junction between a metal and a *p*-type semiconductor when the work function of the metal is less than the work function of the semiconductor. However, in the case of a metal-*n*-type semiconductor junction in which the work function of the semiconductor is greater than that of the metal or a metal-*p*-type semiconductor junction in which the work function of the semiconductor is less than that of the metal, no such energy barriers are created and the contact is said to be ohmic in nature.

[0039] As discussed above, although Schottky first postulated that the height of the energy barrier (Φ_b) formed at a metal-semiconductor junction was simply the difference between the work function of the metal and the electron affinity of the semiconductor, experiments have not verified this relationship. Instead a more complex explanation that takes into account the effects of surface defect states, inhomogeneities and MIGS appears to provide more accurate estimates of barrier heights by explaining the pinning of the Fermi level in the semiconductor. The present inventors have created a technique which is believed to depin the Fermi level of a Si-based semiconductor at a junction with a metal (and thus allow for control or tuning of the barrier height) by both passivating the semiconductor surface (to eliminate or at least reduce the effects of surface states and possibly inhomogeneities) and displacing the metal from the semiconductor (to eliminate or at least reduce the effects of MIGS). This depinning is achieved by introducing an interface layer between the semiconductor and the metal to create a semiconductor -- interface layer -- metal junction, which still permits significant current to flow between the metal and the semiconductor when the junction is forward biased.

[0040] This latter point is important. As discussed further below, for contacts where the energy bands of the semiconductor and the conductor align (i.e., where the Fermi level of the conductor aligns with the conduction or valence band of the semiconductor depending on semiconductor type and/or contact application), if the interface layer is too thin, the specific contact resistance of the junction increases because of the presence of MIGS, resulting in an increased barrier height; thus, current flow is hampered. Conversely, if the interface layer is

too thick, the specific contact resistance is again increased and one gets low current across the junction because of tunneling limitations. The present invention achieves an interface layer that is thick enough to reduce or eliminate the effect of MIGS, while still thin enough to permit significant current flow.

II. Passivation of Semiconductor Surfaces

[0041] A common processing operation performed during semiconductor device fabrication is silicon surface passivation. Surface passivation (whether by an oxide or another material) chemically neutralizes and physically protects the underlying silicon. For example, exposing a silicon surface to oxygen (under the appropriate conditions to grow a protective film of silicon dioxide) will allow the oxygen to react with the dangling bonds of the silicon surface to form covalent bonds that satisfy the surface silicon atoms' valency and render the surface fully coordinated. These covalent bonds provide chemical stability to the silicon surface. The covalent bonds also tie up unbound charges that exist on the silicon surface as a result of the discontinuation of the semiconductor crystal at the surface.

[0042] However, passivation with silicon dioxide has several significant disadvantages. For example, silicon dioxide is a dielectric insulator that poses a significant barrier to the flow of current. Accordingly, a layer of silicon dioxide deposited or grown on a silicon surface may significantly reduce the ability for electrical current to flow through that surface. As a result, the use of silicon dioxide has been limited in practicality to surfaces external to the active region of semiconductor devices through which current passes during device operation (e.g., as a gate oxide layer). This disadvantage is compounded by the fact that the silicon dioxide grows very rapidly and readily on the silicon surface so that it is difficult to limit the growth to a thin layer. Silicon dioxide is also a poor diffusion barrier to semiconductor dopants such as boron.

[0043] Instead of making use of silicon dioxide then, in one embodiment the present inventors utilize a nitrided semiconductor surface to provide chemical passivation. That is, a

nitride layer is introduced to passivate the semiconductor surface by eliminating or at least reducing the effects of surface states and possibly inhomogeneities. The nitride layer also displaces the metal from the semiconductor and eliminates or at least reduces the effects of MIGS. The result of introducing the nitride layer as an interface between the semiconductor and the metal is a depinning of the Fermi level of the semiconductor. When the Fermi level of the semiconductor is depinned, the Fermi level of the metal at the interface will be that of the bulk metal, and will not be dependent upon the interface. In addition to the above, the present inventors propose techniques for providing non-insulating, passivated semiconductor surfaces using materials other than nitrogen; for example, oxides, hydrides, arsenides and/or fluorides.

[0044] These developments have wide applicability in connection with the fabrication of Schottky diodes, Schottky-barrier transistors and other electrical components. For example, in Schottky diodes, the ability to control the energy barrier height at the diode junction is important if the device is to be tailored to specific applications. Use of the present techniques allows for tuning of the barrier height. Further, for other three-terminal devices with Schottky-barrier-isolated channels, control of device characteristics is made possible through the present invention by allowing *n*- and *p*-type devices to be fabricated without dopants, relying instead on the use of metals with different work functions.

[0045] **Figure 5** shows a semiconductor device 510 that contains a semiconductor 530 and an interface layer 520 formed on a surface 540 of the semiconductor in accordance with the present invention. The terms semiconductor device, microelectronic device, monolithic device, chip, and integrated circuit are often used interchangeably in this field. Any or all such devices may each contain an interface layer formed on a semiconductor surface in accordance with the present invention.

[0046] The semiconductor 530 contains a semiconductor material. The term semiconductor material refers to a material having a bandgap that is greater than about 0.1 eV and less than about 4 eV. The term bandgap refers to an energy gap of forbidden energy levels separating the conduction band, which is an upper energy band that is mostly devoid of electrons and

wherein electrons can conduct, and the valence band, which is an energy band that is mostly filled with electrons and wherein electrons cannot conduct. The semiconductor material may have a wide range of doping levels including no doping at all.

[0047] The semiconductor 530 has a surface 540 that is passivated by the interface layer 520. In this context (and as used elsewhere herein) the term passivation means the elimination or at least the reduction of the effects of surface states due to defects or dangling bonds of the semiconductor surface 540. Note that passivation does not, as a practical matter, require that all surface states be eliminated. Rather, it is the effect of surface states on the device properties that is limited or eliminated in passivation. Note further that the presence of MIGS may be regarded as a surface state, however, as used herein the term passivation is not meant to infer the elimination of MIGS (though in some cases, a passivation layer may have sufficient thickness to provide a separation layer between the semiconductor and the metal sufficient to reduce or eliminate MIGS). The semiconductor 530 is operable to be electrically coupled with a first voltage associated with the semiconductor device 510 and to conduct electrical current 550 across the passivated surface 540.

[0048] The interface layer 520 is formed on the semiconductor 530 and may contain a passivation material that bonds to the semiconductor material by way of a covalent (or other) bond formed between the passivation material and the semiconductor material. For example, an atom of passivation material may covalently bond with a dangling bond of a surface silicon atom to fully coordinate the silicon atom and thereby help passivate the silicon atom. In some cases, the passivation material may be the sole component of the interface layer 520, while in other cases the interface layer 520 may be a compound layer that includes both a passivation layer and a separation layer. That is, the interface layer serves to (i) chemically passivate the semiconductor surface 540, and (ii) displace the semiconductor from the metal sufficiently to eliminate or at least reduce the effect of MIGS. As explained below, this may necessitate including a separation layer in addition to a passivation layer within the interface layer, depending on the passivation material selected. Of course, the combination of the passivation

layer and the separation layer must be sufficiently thin to permit the low specific contact resistances described herein.

[0049] Different passivation materials are contemplated. According to one embodiment, the interface layer 520 is formed using a material that is preferably selected from the group consisting of hydrogen (H), oxygen (O), nitrogen (N), arsenic (As), and fluorine (F) (that is, the interface layer 520 may include a nitride, an oxide, a hydride, an arsenide and/or a fluoride). Other materials having chemical characteristics or valences similar to these materials may also be used. Note that distinct separation layers (i.e., in addition to the passivation layer(s)) may be needed where H, As, or F passivation layers are used, as these tend to form monolayer coverage, rather than a layer of a compound with Si of process-dependent thickness. In contrast, passivation layers made using N and/or O may not require distinct separation layers, as these elements may form a layer of a compound of Si with a thickness that can be varied depending on processing.

[0050] Different amounts of passivation material are contemplated to be useful for different embodiments of the present invention. Often, the interface layer 520 includes or is made up of a passivation layer with a thickness of between approximately 0.1 nm and about 5 nm. For example, depending upon the particular implementation, the thickness may be less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, may be the thickness corresponding to a single layer or monolayer of passivation material that is bonded to the semiconductor surface, or may even be the number of atoms of passivation material required to passivate substantially all the dangling bonds associated with the semiconductor surface 540.

[0051] In some cases, passivation of the semiconductor surface 540 will include removing (or terminating) dangling bonds located proximate to the surface of the semiconductor material, including those at the surface as well as those within a few molecular dimensions from the surface. This process may stabilize the surface of the semiconductor material and may improve the controllability of subsequent fabrication operations. Passivation may also reduce the density of surface states that may exist at the semiconductor surface as a result of the

discontinuation of the semiconductor crystal at the surface. This may improve consistency and performance of the semiconductor device, inasmuch as such states are known to interfere with proper device operation. For example, they may provide surface charge states that result in a pinning of the Fermi level.

III. Forming Interface Layers

[0052] Exemplary methods for forming interface layers to provide (i) passivation of semiconductor surfaces, and (ii) displacement of the semiconductor from the metal to eliminate or at least reduce of the effects of MIGS within the semiconductor when in the presence of the metal (collectively referred to herein as depinning the Fermi level of the semiconductor) with hydrogen, fluorine or nitrogen are presented below to further illustrate the concepts of the present invention. Other passivation materials may include arsenic, oxygen or an oxynitride, and in some cases such passivation layers are combined with separation layers (e.g., made of an oxide) to complete the interface layer.

A. Hydrogen And Fluorine

[0053] An interface layer may contain hydrogen, fluorine, or both hydrogen and fluorine (e.g., in the form of a hydride and/or a fluoride). One method for forming an interface layer on a semiconductor surface with hydrogen and fluorine includes cleaning the semiconductor substrate with a cleaning solution, immersing the cleaned substrate in a hydrogen fluoride solution (or other liquid containing hydrogen and fluorine ions) having an effective concentration typically between about 1%-50% by weight, waiting an effective period of time, typically between about several seconds and about 5 minutes, removing the substrate from the hydrogen fluoride solution, optionally rinsing the substrate in deionized water, and blow-drying the substrate with nitrogen. Such a method may form an interface layer containing hydrogen and fluorine that are bonded (e.g., covalently) to the semiconductor surface.

[0054] It should be noted that long rinses in deionized water, generally longer than about 30 seconds, might remove the hydrogen passivation. Thus, deionized water rinses might advantageously be kept to less than about 30 seconds to maintain the hydrogen passivation of the surface. Also, the higher the concentration of the hydrogen fluoride during the immersion, the greater the concentration of fluorine passivation. Finally, methods are also contemplated where the ratio of hydrogen to fluorine passivation is altered by removing either the hydrogen or the fluorine.

[0055] An interface layer formed in this fashion may be best suited for applications where a subsequent metal layer is deposited over the interface layer in a generally non-invasive fashion, for example using a thermally evaporated source. Experiments by the present inventors to date suggest that using other approaches (e.g., plasma deposition) may cause damage to the thin (e.g., monolayer thick) interface layer contemplated as part of the present invention.

B. Nitrogen

[0056] In a further embodiment, an interface layer may contain nitrogen (e.g., in the form of silicon nitride). One method for forming an interface over a semiconductor surface with nitrogen includes heating a substrate containing the semiconductor surface in the presence of a nitrogenous material (that is, a gas or other material containing nitrogen). For example, a substrate containing an exposed silicon surface may be annealed at a temperature between about 300°C and about 750°C, which is lower than temperatures conventionally used for Rapid Thermal Nitridation (RTN), under a gaseous ambient having, for example, ammonia (NH₃) at some effective partial pressure. By exposed, we mean a clean surface, free of everything except silicon. Such a method may form an interface layer containing nitrogen, often in the form of a nitride, bonded to the semiconductor surface. Note that the present inventors have observed indications suggesting that in these low temperature conditions interface layer growth is self-limiting, depending only on temperature.

[0057] According to another embodiment, an interface layer that includes nitrogen may be formed on an exposed surface of a semiconductor material by a method that includes heating a semiconductor material to a substantially high temperature under vacuum and exposing the semiconductor material to a substantially small amount of a nitrogenous material, such as ammonia. The method may include placing a semiconductor having an exposed semiconductor surface in a heating chamber, pulling a vacuum of less than about one millionth of a Torr, or more favorably an ultra high vacuum of less than 10^{-9} Torr, and then heating the semiconductor in the heating chamber to a substantially high temperature. The higher the vacuum, the longer the substrate may be heated without growth of an oxide from residual oxygen or water in the chamber. Thus, the process may include heating the semiconductor to a temperature that is between about 900°C and about 1000°C, or higher, in an inert ambient. As desired, the semiconductor may be exposed to hydrogen gas, or an equivalent, to reduce any native oxide on the semiconductor. These high temperatures may provide for greater passivation of the semiconductor surface as compared with results that may be achieved at lower temperatures.

[0058] Then, the heated semiconductor may be exposed to a substantially small amount of a nitrogenous material, such as ammonia. This may include exposing the semiconductor surface to ammonia for a substantially short period of time. For example, the surface may be subjected to a burst or pulse of ammonia lasting for a time period between about 0.5 seconds and about 5 seconds. Alternatively, the surface may be exposed to a controlled, small amount of ammonia over an arbitrarily longer period of time. In this way, the substantially small amount of ammonia will react with the surface to form a nitrogenous interface layer, such as a nitride layer, thereon and then further growth of the interface layer will cease. Then the semiconductor may be cooled from the substantially high temperature to ambient temperature and removed from the heating chamber. Further annealing of the substrate and the grown nitride layer may also be performed in the vacuum chamber before removal, at a substantially elevated temperature between about 700°C and 1000°C, or higher.

[0059] Advantageously, it has been unexpectedly observed that a process such as that described above and incorporating substantially high temperature exposure for substantially short periods may be used to controllably form thin yet effective interface layers. That is, the present inventors have observed that in the creation of thin interface layers that include nitrogenous materials, temperature appears to be a dominant factor in controlling thickness. For example, by such methods effective interface layers may be formed having a thickness that is less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, or having a thickness that corresponds to essentially a single monolayer sufficient to passivate essentially all dangling bonds proximate the semiconductor surface.

[0060] Further, thin interface layers may be advantageously grown on a semiconductor in the presence of nitrogen gas, or other inert nitrogen-containing gas. The reaction rate of a semiconductor such as silicon with nitrogen gas is significantly lower than that of a reactive nitrogen-containing gas such as ammonia. The slow growth rate may be desirable for better control of the growth of films of nitrogen on a semiconductor of a thickness of less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, or having a thickness that corresponds to essentially a single monolayer sufficient to passivate essentially all dangling bonds proximate the silicon surface.

IV. Diodes Containing Passivated Semiconductor Surfaces

[0061] Diodes made from Schottky barriers (i.e., asymmetric electrical potentials formed at a junction between a metal and a semiconductor) are widely used in rectifiers in power supply and control applications. As used herein, the terms Schottky diode, metal-semiconductor junction diode, diode, and rectifier are all related and appear in order from more specific at the left to more general at the right. Likewise, the terms Schottky barrier, metal-semiconductor barrier, conductor-semiconductor junction, and multi-material junction are all related and

appear in order from more specific at the left to more general at the right. The term Schottky diode will be used to refer to a diode containing a Schottky barrier.

[0062] As mentioned above, the present inventors have devised a scheme to control or adjust a Schottky barrier height by forming an interface layer (which includes or sometimes consists of a passivation layer that includes an oxide, oxynitride, nitride, arsenide, hydride, fluoride, or an equivalent) between a metal and a semiconductor. This scheme differs from past attempts by others to control barrier height, which attempts generally involved either using a silicide as a contact metal (and thus limiting the choices of available contact metals to those that can form silicides), or using esoteric substrates that exhibit wide bandgaps. Further, in previous devices the Fermi level of the semiconductor remains pinned, with the barrier height being virtually independent of the metal used. Finally, doping of substrates has also been attempted, however, it has not been shown to truly affect the barrier height of the substrate material. For example, PtSi contacts have reduced resistance due to high silicon doping such that the current across the junction is dominated by tunneling through the barrier. Doping may thus lead to cases where the top of the barrier may be so thin as to be essentially transparent to electrons, however, doping does not appear to allow actual tuning of the barrier height.

[0063] **Figure 6** shows an example of a diode 600 containing, according to one embodiment of the present invention, an interface layer 620 disposed between and attached to both a semiconductor 610 and a conductor 630. The conductor and the semiconductor are operable to be electrically coupled with different voltages associated with the operation of the diode 600 and to pass electrical current through a passivated semiconductor surface formed at the junction between the semiconductor 610 and the interface layer 620.

[0064] The conductor 630 contains a conductive material such as a metal or an alloy of a metal. The terms metal, conductive material, and conductor are all related and appear in order from specific at the left to general at the right. In general, the terms refer to a highly electrically conductive substance that has a Fermi energy level that sits in a partially filled band. Unless otherwise specified, conductors include metals (e.g., pure metals and alloys),

and other conductors such as doped polysilicon (a nonporous silicon containing randomly oriented crystallites), doped single crystal silicon, and metal silicides. Note that alloys may have workfunctions different than their constituents and may be designed to have specific workfunctions though selective use of ratios of the constituent metals.

[0065] Often, the conductor is a metal since metals may offer advantages over conductive semiconductors including lower resistance, higher carrier mobilities that provide superior high frequency performance and switching, favorable low power characteristics, and ease of manufacturing control. Use of metals may also avoid the need to perform semiconductor doping, which may simplify manufacturing and improve quality control.

[0066] Metals that are contemplated include pure metals, alloys, refractory metals, metals that do not form silicides, metals physically deposited by substantially non-invasive processes such as by condensation of a thermally evaporated metal vapor, and metals having a predetermined work function. The use of non-invasively deposited metals may allow for forming the metal on a thin interface layer without disrupting the passivation properties of the layer.

[0067] A metal having a predetermined work function may be a metal having a work function smaller or greater than that of the semiconductor, depending on the desired application. Often, the semiconductor will be silicon. In this case by the work function of a semiconductor or silicon we mean the energy in the middle of the semiconductor bandgap. Exemplary metals that have a work function smaller than silicon include Group 3A elements, aluminum (Al), indium (In), titanium (Ti), chromium (Cr), tantalum (Ta), cesium (Cs), magnesium (Mg), erbium (Er), ytterbium (Yb), manganese (Mn), lead (Pb), silver (Ag), yttrium (Y), and zinc (Zn). Exemplary metals that have a work function greater than silicon include platinum (Pt), gold (Au), tungsten (W), nickel (Ni), molybdenum (Mo), copper (Cu), cobalt (Co), and palladium (Pd).

[0068] The semiconductor-interface layer-conductor configuration illustrated in **Figure 6** defines what the present inventors have chosen to call a "passivated Schottky barrier". The

passivated Schottky barrier is a naturally formed electrical potential barrier to an electron or hole at the Fermi energy (the electrochemical potential) in the conductor due to a depletion region formed in the semiconductor adjacent the conductor. The passivated Schottky barrier may deviate in barrier height from a standard un-passivated Schottky barrier that would form naturally at a contact junction between the semiconductor and the conductor without the interface layer disposed therebetween. That is, the passivated Schottky barrier may have a barrier height that depends predominantly upon the bulk characteristics of the semiconductor and the conductor, rather than on surface properties, and may depend in part on the characteristics of the interface layer.

[0069] Indeed, the present inventors have determined that changes in barrier height are approximately monotonic and continuous for variations in surface passivation thickness by nitridation of the semiconductor substrate. More specifically, experiments by the present inventors in a regime where the nitride layer is sufficiently thick to remove MIGS show that temperature of interface layer formation has the strongest effect on barrier height. In other regimes, thickness may be critical. Ideally, if all surface states are removed, barrier height should be controllable simply by the choice of metal used.

[0070] To understand why thickness of the interface layer is important, refer briefly to **Figure 8** where a graph of interface-specific contact resistance versus interface thickness is shown. The graph is for a structure where the workfunction of the metal is the same as the electron affinity in the semiconductor, such that the Fermi level of the metal lines up with the conduction band of the semiconductor. At large thicknesses, the interface layer poses significant resistance to current. As thickness decreases, resistance falls due to increased tunneling current. However, there comes a point where even as the interface layer continues to get thinner, resistance increases. This is due to the effect of MIGS, which increasingly pull the Fermi level of the metal down towards mid-gap of the semiconductor, creating a Schottky barrier. The present inventors have discovered that this competition results in an optimum thickness, as shown in the illustration, where the resistance is a minimum. At this thickness

the effect of MIGS has been sufficiently reduced to depin the metal and lower the Schottky barrier, and the layer is still sufficiently thin to allow significant current flow across the interface layer. Contact resistances of less than or equal to approximately $2500 \text{ } \Omega\text{-}\mu\text{m}^2$, $1000 \text{ } \Omega\text{-}\mu\text{m}^2$, $100 \text{ } \Omega\text{-}\mu\text{m}^2$, $50 \text{ } \Omega\text{-}\mu\text{m}^2$, $10 \text{ } \Omega\text{-}\mu\text{m}^2$ or even less than or equal to $1 \text{ } \Omega\text{-}\mu\text{m}^2$ may be achieved.

[0071] Characteristics that may be adjusted to provide a desired barrier height thus include the passivation material used (e.g., selection based on bandgap), the interface layer thickness (e.g., especially where the interface layer is a compound layer formed of a passivation layer and a separation layer), the method of forming the interface layer (e.g., control of parameters such as temperature), the interface layer thickness that is substantially similar to a penetration depth of MIGS formed at a metal interface, the metal used for the source and/or drain, and other characteristics.

[0072] One advantage of the ability to adjust the Schottky barrier height with the introduction of interface layer 620 is the ability to form a substantially high barrier height. For example, an interface layer may be used to create a Schottky barrier having a barrier height that is greater than can be achieved through the use of metal silicides, greater than about 2.0 eV, or greater than about 2.5 eV (using a semiconductor with a bandgap at least this large), or nearly 1.0 V using silicon. Such high barrier heights imply the ability to withstand high voltages before breakdown occurs. Thus, Schottky barriers having such high barrier heights may be particularly useful in high-voltage Schottky diodes.

[0073] Another advantage achieved through the use of the interface layer 620 is greater flexibility afforded in selecting a conductor 630. Typically, metals chosen for application in classic Schottky diodes are those that can form a silicide with a silicon semiconductor. The formation of the silicide helps to reduce surface states (resulting from dangling bonds), but not the effects of MIGS. Thus, the Fermi level at the semiconductor surface is still pinned. Using metals that form silicides upon contact with silicon may thus help to make the devices more

reproducible in a manufacturing environment, but such devices still suffer from the drawback of having a barrier height that is fixed.

[0074] According to one embodiment of the present invention, however, one may select a conductor that is not able (or not readily able) to form a silicide with the semiconductor. The metal silicide is not needed because the interface layer provided in accordance with the present invention passivates the semiconductor surface and also reduces or eliminates the effect of MIGS. This may allow for selection of a metal that has properties such as a desirable work function or Fermi level energy, even though that metal may not form a metal silicide.

[0075] For example, to make large-barrier diodes, for an *n*-type doped silicon semiconductor, a metal may be selected that has a work function that is either substantially equal to the valence band energy of the semiconductor or that is within about 0.1 eV to about 0.3 eV of the valence band energy of the semiconductor. Similarly, for a *p*-type doped silicon semiconductor, a metal may be selected that has a work function substantially equal to the conduction band energy of the semiconductor. For Schottky diodes configured in accordance with the present invention, the Fermi level of the metal may lie anywhere in the bandgap of the semiconductor when an interface layer is disposed within the junction, resulting in diodes of various barrier heights. The Fermi level of the metal may also lie in the conduction or valence band of the semiconductor.

[0076] The use of interface layer 620 thus provides a way to tune, adjust, or control the height of the barrier between the conductor and the semiconductor. Without the interface layer 620, the barrier height would be substantially un-tunable, un-adjustable, and fixed (as discussed above).

[0077] The role played by interface layer 620 in tuning, adjusting, or controlling the height of the barrier between the conductor 630 and the semiconductor 610 may be understood as a depinning of the Fermi level of the semiconductor. That is, the interface layer may reduce surface states by bonding to the semiconductor material to consume dangling bonds. Additionally, the interface layer may reduce the formation of MIGS in the semiconductor by

providing a thickness and bandgap that prevent the electron wave function (of the metal) from penetrating into the semiconductor. The electron wave function may instead penetrate into the interface layer and form MIGS within the interface layer at an energy related to the states of the interface layer material. As desired, the density of the MIGS and the depth of MIGS penetration into the interface layer may be reduced by choosing an interface layer material or materials having a larger bandgap or higher effective mass than the semiconductor.

[0078] According to one embodiment of the present invention then, the interface layer 620 is incorporated into a device operable to pass current through the semiconductor surface and the interface layer during device operation. In such an embodiment, it may be desirable to use an interface layer having a thickness of a monolayer, or, for example between about 0.1 nm and about 0.3 nm, and also having a wide bandgap (as compared to that of the semiconductor) so that the interface layer both de-pins the Fermi level (so that the barrier height depends predominantly on bulk properties of the junction materials) and allows sufficient current transfer across it. Advantageously, such interface layers may be sufficiently thin to provide low impedance to current flow (due to the exponential dependence of direct tunneling on barrier thickness), which is desirable for many semiconductor devices, while also providing sufficient semiconductor surface passivation to allow an adjustable barrier height. That is, the interface layer may allow passivation of surface states and reduction (or elimination) of MIGS in the semiconductor to allow for an adjustable barrier height with a substantially thin layer that allows sufficient current to be transferred across the interface layer.

[0079] There are several methods by which the barrier height can be made adjustable. For example, adjustment may be made by tuning the degree of Fermi level pinning. In other words, some embodiments may allow for a sufficiently thin interface layer so that not all of the effects of MIGS in the Si are eliminated. Further, the pinning may be varied by combinations of thickness of the interface layer and the choice of interface material. The metal in contact with the interface layer may be pinned by MIGS at different levels in different materials. Conversely, or in addition, the passivation may be left incomplete to allow for an

effective level of unpassivated states. Complete depinning of the Fermi level (that is removal of all surface states in Si including MIGS) is another option, in which case one could tune the barrier height simply by choosing a pure metal or an alloy that possesses the desired workfunction. In that case, the barrier height is determined by Equation (1), which until now has been an unrealizable idealization. Note that the type of tuning being discussed here is adjustment of the barrier height by altering the structure of the junction at the time of manufacture, not by varying an externally applied condition during junction operation.

[0080] **Figure 7a – 7d** show relationships between Fermi energy, conduction band energy, and valence band energy for various Schottky barriers containing a metal in contact with (or in close proximity to) a semiconductor, where the bandgap (E_g) of the semiconductor exists between the conduction band (E_c) and the valence band (E_v). In this example, the work function of the metal Φ_M is chosen to be approximately equal to the electron affinity χ_s of the semiconductor. In **Figure 7a**, an unpassivated Schottky barrier 700 is shown. In this example, the Fermi level (E_F) of the metal 730 is pinned in the bandgap of the semiconductor 710. This results in a discontinuity in the vacuum level caused by a charged dipole at the interface.

[0081] In **Figure 7b**, the interface layer 720b is thick enough to passivate dangling bonds at the surface of the semiconductor 710, but not thick enough to eliminate or sufficiently reduce the effect of MIGS. As a result, the band structure is largely unaltered from that seen in the previous illustration. Similarly, in **Figure 7c**, when the interface layer 720c is sufficiently thick to eliminate or reduce the effect of MIGS but not to passivate the semiconductor surface, little change in the energy band structure is observed. However, as shown in **Figure 7d**, when the interface layer 720d is sufficient to both eliminate or reduce the effect of MIGS and to passivate the semiconductor surface, we see the Fermi level of the metal aligning with the conduction band of the semiconductor (i.e., the Fermi level of the semiconductor has been depinned and no longer lines up with the Fermi level of the metal). The vacuum level is now continuous as there is no charged dipole at the interface. Thus, the band structure of a device

constructed in this fashion is a result of only bulk material properties, not properties of the surface. By way of example, the materials in such cases may be Al and Si, with a work function for Al of approximately $\Phi_M = 4.1$ eV and the electron affinity for Si of approximately $\chi_S = 4.05$ eV.

V. Transistors Containing Passivated Semiconductor Surfaces

[0082] The interface layers described herein may be used in connection with a semiconductor surface of a channel in a field effect transistor. That is, an interface layer may be disposed between a source and a channel, a channel and a drain, or both of an insulated gate field effect transistor. Such use of an interface layer is described in detail in co-pending U.S. Patent Application No.: _____ entitled "INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL", filed _____, 2002 by the present inventors, and assigned to the assignee of the present invention.

[0083] The source and drain contacts at the channel of a field effect transistor are examples of a broader category of metal-interface layer-semiconductor contacts that make up the present invention. In the past, such contacts generally comprised a silicide- n^+ -Si junction, which formed a somewhat "leaky" Schottky diode, with a Fermi level of the semiconductor pinned at the midgap. In contrast, the present invention provides a contact wherein the Fermi level of the metal is aligned with the conduction band of the semiconductor (e.g., as shown in Figure 7d). Note that in other cases, depending on the type of semiconductor material and conductors used, the Fermi level of the metal may align with the valence band of the semiconductor.

[0084] Although both types of junctions (i.e., the new passivated Schottky barrier junction and the conventional silicide-semiconductor junction) permit tunneling currents, the present junction can be fabricated with a much thinner interface layer as compared to the thickness of the silicide layer used previously. Indeed, thickness of an order of magnitude less than the silicide thickness can be expected. In a conventional silicide – semiconductor junction a

Schottky barrier is formed which is comprised of a depletion layer. The tunnel barrier presented by such a depletion layer may be an order of magnitude thicker than the dielectric tunnel barrier in the present invention. The thinner interface layers provided by the present invention permit higher current across the junction (i.e., lower junction specific contact resistance).

[0085] Two other properties of the dielectric deserve mention. First is the property of the height of the barrier compared to the semiconductor conduction band (for electrons). In making the barrier thinner than a silicide barrier, the tradeoff may be a higher tunnel barrier (e.g., 2 eV for nitride, compared with about half the gap of 0.6 eV for silicide). Spacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV). Nevertheless, even with the higher barrier to electrons, the present inventors have determined that the resistance can still be one hundred times lower than a contact to silicon with a silicide barrier.

[0086] The second property is the effective mass of electrons in the dielectric. Larger mass electrons will not penetrate as far (i.e., because of their shorter wavelength) from the metal into the semiconductor. The less the electrons penetrate into the dielectric, the less the effect of MIGS in the dielectric. Thus, MIGS in the dielectric are reduced with larger bandgap and larger effective mass.

[0087] In addition the junction of the present invention can be used in making contacts to source or drain implanted wells and will have the advantage of reducing the need for high doping levels (which are now reaching their limits of solid solubility). The high doping profiles were required in the past in order to keep the junction depletion layer relatively thin, so as to increase the tunneling current, thus reducing the junction resistance. However, it is becoming increasingly difficult to increase doping profiles in order to provide low resistance junctions. It may be possible to reach the same level of resistance with a lower doping concentration using the present invention. It may further be possible to achieve much lower resistance even with lower doping concentration. When the present invention is used with high doping levels, the resistance will be further reduced.

[0088] Thus, methods and applications for semiconductor-interface layer-metal junctions have been described. Although described with reference to specific embodiments it should be remembered that various modifications and changes may be made to the techniques described herein without departing from the broader spirit and scope of the invention. The specification and drawings are accordingly to be regarded in an illustrative rather than a restrictive sense and the invention measured only in terms of the claims, which follow.

CLAIMS

What is claimed is:

1. An electrical device, comprising:
 - a metal;
 - a silicon-based semiconductor having a Fermi level; and
 - an interface layer disposed between and in contact with both the metal and the semiconductor and configured to depin the Fermi level of the semiconductor,wherein the electrical device has a specific contact resistance of less than or equal to approximately $1000 \text{ } \Omega - \mu\text{m}^2$.
2. The electrical device of claim 1 wherein the interface layer includes a passivating material.
3. The electrical device of claim 2 wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of silicon.
4. The electrical device of claim 3 wherein the interface layer consists essentially of a monolayer configured to depin the Fermi level of the semiconductor.
5. The electrical device of claim 2 wherein the interface layer further includes a separation layer.
6. The electrical device of claim 1 wherein the specific contact resistance is less than or equal to approximately $100 \text{ } \Omega - \mu\text{m}^2$.

7. The electrical device of claim 1 wherein the specific contact resistance is less than or equal to approximately $50 \Omega\text{-}\mu\text{m}^2$.
8. The electrical device of claim 1 wherein the specific contact resistance is less than or equal to approximately $10 \Omega\text{-}\mu\text{m}^2$.
9. The electrical device of claim 1 wherein the specific contact resistance is less than or equal to approximately $1 \Omega\text{-}\mu\text{m}^2$.
10. The electrical device of claim 1 wherein the interface layer comprises a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material.
11. The electrical device of claim 10 wherein the nitrogenous material comprises at least one of ammonia (NH_3), nitrogen (N_2) or unbound nitrogen (N).
12. An electrical device, comprising a metal – interface layer – Si-based semiconductor junction in which the interface layer includes a passivating material and the electrical device has a specific contact resistance of less than approximately $1000 \Omega\text{-}\mu\text{m}^2$.
13. The electrical device of claim 12 wherein the specific contact resistance is less than or equal to approximately $100 \Omega\text{-}\mu\text{m}^2$.
14. The electrical device of claim 12 wherein the specific contact resistance is less than or equal to approximately $50 \Omega\text{-}\mu\text{m}^2$.
15. The electrical device of claim 12 wherein the specific contact resistance is less than or equal to approximately $10 \Omega\text{-}\mu\text{m}^2$.

16. The electrical device of claim 1 wherein the specific contact resistance is less than or equal to approximately $1 \Omega\text{-}\mu\text{m}^2$.

17. The electrical device of claim 12, wherein the passivating material comprises one or more of a nitride, an oxide, an oxynitride a hydride, a fluoride and/or an arsenide of silicon.

18. The electrical device of claim 17, wherein the interface layer comprises a passivation layer and a separation layer.

19. A method, comprising depinning a Fermi level of a silicon-based semiconductor in an electrical junction through the use of an interface layer disposed between a surface of the semiconductor and a conductor, wherein the interface layer (i) has a thickness sufficient to reduce effects of metal-induced gap states in the semiconductor while providing the junction with a specific contact resistance of less than approximately $1000 \Omega\text{-}\mu\text{m}^2$, and (ii) passivates the surface of the semiconductor.

20. The method of claim 19 wherein the specific contact resistance is less than or equal to approximately $100 \Omega\text{-}\mu\text{m}^2$.

21. The method of claim 19 wherein the specific contact resistance is less than or equal to approximately $50 \Omega\text{-}\mu\text{m}^2$.

22. The method of claim 19 wherein the specific contact resistance is less than or equal to approximately $10 \Omega\text{-}\mu\text{m}^2$.

23. The method of claim 19 wherein the specific contact resistance is less than or equal to approximately $1 \Omega\text{-}\mu\text{m}^2$.

24. The method of claim 19 wherein the interface layer has a thickness sufficient to provide a specific contact resistance of the electrical junction of less than or equal to approximately $1 \Omega\text{-}\mu\text{m}^2$.
25. The method of claim 19 wherein the interface layer includes a passivating material selected from the list comprising: an arsenide, a hydride, a fluoride, an oxide, an oxynitride and a nitride of silicon.
26. The method of claim 25 wherein the interface layer consists essentially of a monolayer.
27. The method of claim 19 wherein the interface layer is grown on the semiconductor surface at temperatures above approximately 300°C .
28. The method of claim 27 wherein the interface layer is grown in the presence of a nitrogenous material.
29. The method of claim 28 wherein the nitrogenous material comprises one of ammonia (NH_3), nitrogen (N_2), or unbound nitrogen (N).
30. The method of claim 19 wherein the interface layer includes a passivation layer grown by immersion of the semiconductor in a liquid containing hydrogen and fluorine ions.
31. An electrical device, comprising a junction between a Si-based semiconductor and a conductor separated from the semiconductor by an interface layer having a thickness that allows a Fermi level of the conductor to align with a conduction band of the semiconductor,

wherein the electrical device has a specific contact resistance less than approximately $1000 \Omega\text{-}\mu\text{m}^2$.

32. The electrical device of claim 31 wherein the specific contact resistance is less than or equal to approximately $100 \Omega\text{-}\mu\text{m}^2$.

33. The electrical device of claim 31 wherein the specific contact resistance is less than or equal to approximately $50 \Omega\text{-}\mu\text{m}^2$.

34. The electrical device of claim 31 wherein the specific contact resistance is less than or equal to approximately $10 \Omega\text{-}\mu\text{m}^2$.

35. The electrical device of claim 31 wherein the specific contact resistance is less than or equal to approximately $1 \Omega\text{-}\mu\text{m}^2$.

36. An electrical device, comprising a junction between a Si-based semiconductor and a conductor separated from the semiconductor by an interface layer having a thickness that allows a Fermi level of the conductor to align with a valence band of the semiconductor, wherein the electrical device has a specific contact resistance less than approximately $1000 \Omega\text{-}\mu\text{m}^2$.

37. The electrical device of claim 36 wherein the specific contact resistance is less than or equal to approximately $100 \Omega\text{-}\mu\text{m}^2$.

38. The electrical device of claim 36 wherein the specific contact resistance is less than or equal to approximately $50 \Omega\text{-}\mu\text{m}^2$.

39. The electrical device of claim 36 wherein the specific contact resistance is less than or equal to approximately $10 \Omega\text{-}\mu\text{m}^2$.
40. The electrical device of claim 36 wherein the specific contact resistance is less than or equal to approximately $1 \Omega\text{-}\mu\text{m}^2$.
41. An electrical device, comprising a junction between a Si-based semiconductor and a conductor separated from the semiconductor by an interface layer having a thickness that allows a Fermi level of the semiconductor to be independent of a Fermi level of the conductor, wherein the electrical device has a specific contact resistance less than approximately $1000 \Omega\text{-}\mu\text{m}^2$.
42. The electrical device of claim 41 wherein the specific contact resistance is less than or equal to approximately $100 \Omega\text{-}\mu\text{m}^2$.
43. The electrical device of claim 41 wherein the specific contact resistance is less than or equal to approximately $50 \Omega\text{-}\mu\text{m}^2$.
44. The electrical device of claim 41 wherein the specific contact resistance is less than or equal to approximately $10 \Omega\text{-}\mu\text{m}^2$.
45. The electrical device of claim 41 wherein the specific contact resistance is less than or equal to approximately $1 \Omega\text{-}\mu\text{m}^2$.
46. An electrical device, comprising:
a silicon-based semiconductor of either *n*-type or *p*-type semiconductor material;

a metal having a workfunction approximately equal to a conduction band of the semiconductor if the semiconductor is of *n*-type semiconductor material or having a workfunction approximately equal to a valence band of the semiconductor if the semiconductor is of *p*-type semiconductor material; and

an interface layer disposed between and in contact with both the semiconductor and the metal, wherein the electrical device has a specific contact resistance of less than or approximately equal to $1000 \Omega\text{-}\mu\text{m}^2$.

47. The electrical device of claim 46 wherein the interface layer includes a passivating material.
48. The electrical device of claim 47 wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of silicon.
49. The electrical device of claim 48 wherein the interface layer consists essentially of a monolayer configured to depin a Fermi level of the semiconductor.
50. The electrical device of claim 47 wherein the interface layer further includes a separation layer.
51. The electrical device of claim 46 wherein the specific contact resistance is less than or equal to approximately $100 \Omega\text{-}\mu\text{m}^2$.
52. The electrical device of claim 46 wherein the specific contact resistance is less than or equal to approximately $50 \Omega\text{-}\mu\text{m}^2$.

53. The electrical device of claim 46 wherein the specific contact resistance is less than or equal to approximately $10 \Omega\text{-}\mu\text{m}^2$.
54. The electrical device of claim 46 wherein the specific contact resistance is less than or equal to approximately $1 \Omega\text{-}\mu\text{m}^2$.
55. The electrical device of claim 46 wherein the interface layer comprises a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material.
56. The electrical device of claim 55 wherein the nitrogenous material comprises at least one of ammonia (NH_3), nitrogen (N_2) or unbound nitrogen (N).
57. An electrical device, comprising:
- a silicon-based semiconductor of either *n*-type or *p*-type semiconductor material;
 - a metal having a workfunction near or substantially equal to a conduction band edge of the semiconductor if the semiconductor is of *p*-type semiconductor material, or having a workfunction near or substantially equal to a valence band edge of the semiconductor if the semiconductor is of *n*-type semiconductor material; and
 - an interface layer disposed between and in contact with both the semiconductor and the metal and configured to depin a Fermi level of the semiconductor.
58. The electrical device of claim 57 wherein the interface layer includes a passivating material.

59. The electrical device of claim 58 wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of silicon.

60. The electrical device of claim 57 wherein the interface layer consists essentially of a monolayer configured to depin a Fermi level of the semiconductor.

61. The electrical device of claim 57 wherein the interface layer further includes a separation layer.

Attorney's Docket No.: 3771P003

Patent

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

the specification of which

 X

is attached hereto.

was filed on (MM/DD/YYYY) _

as

United States Application Number _____

or PCT International Application Number _____

and was amended on (MM/DD/YYYY) _____.

(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application. I do not know and do not believe that the claimed invention was in public use or on sale in the United States of America more than one year prior to this application, nor do I know or believe that the invention has been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)Priority
Claimed

<u>(Number)</u>	<u>(Country)</u>	<u>(Foreign Filing Date - MM/DD/YYYY)</u>	<u>Yes</u>	<u>No</u>
<u>(Number)</u>	<u>(Country)</u>	<u>(Foreign Filing Date - MM/DD/YYYY)</u>	<u>Yes</u>	<u>No</u>
<u>(Number)</u>	<u>(Country)</u>	<u>(Foreign Filing Date - MM/DD/YYYY)</u>	<u>Yes</u>	<u>No</u>

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

(Application Number) (Filing Date – MM/DD/YYYY)

(Application Number) (Filing Date – MM/DD/YYYY)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number) (Filing Date – MM/DD/YYYY) (Status -- patented,
pending, abandoned)

(Application Number) (Filing Date – MM/DD/YYYY) (Status -- patented,
pending, abandoned)

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

**Send correspondence Tarek N. Fahmi, Reg. No. 41,402, BLAKELY,
SOKOLOFF, TAYLOR &**

(Name of Attorney or Agent)

**ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California
90025 and direct telephone calls to Tarek N. Fahmi, (408) 720-
8300.**

(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor **DANIEL E. GRUPP**

Inventor's Signature *DE Grupp* Date 8/7/02

Residence PALO ALTO, CA Citizenship USA
(City, State) (Country)

Post Office Address 334 LELAND AVE.

Full Name of Second/Joint Inventor **DANIEL J. CONNELLY**

Inventor's Signature *Daniel Connelly* Date 8 Aug 2002

Residence REDWOOD CITY CA Citizenship USA
(City, State) (Country)

Post Office Address 525 RUTHERFORD AVE

APPENDIX A

Ramin Aghevli, Reg. No. 43,462; William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. 42,261; W. Thomas Babbitt, Reg. No. 39,591; Jordan M. Becker, Reg. No. 39,602; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; R. Alan Burnett, Reg. No. 46,149; Daniel J. Burns, Reg. No. 50,222; Gregory D. Caldwell, Reg. No. 39,926; Thomas M. Coester, Reg. No. 39,637; Robert P. Cogan, Reg. No. 25,049; Donna Jo Coningsby, Reg. No. 41,684; Florin A. Corie, Reg. No. 46,244; Mimi D. Dao, Reg. No. 45,628; Stephen M. De Klerk, Reg. No. 46,503; Daniel M. De Vos, Reg. No. 37,813; Justin M. Dillon, Reg. No. 42,486; Sanjeet Dutta, Reg. No. 46,145; Tarek N. Fahmi, Reg. No. 41,402; Mark C. Farrell, Reg. No. 45,988; Thomas S. Ferrill, Reg. No. 42,532; Kyle H. Flindt, Reg. No. 42,539; George L. Fountain, Reg. No. 37,374; Andre M. Gibbs, Reg. No. 47,593; James Y. Go, Reg. No. 40,621; Mark A. Goldstein, Reg. No. 50,759; Alan E. Heimlich, Reg. No. 48,808; James A. Henry, Reg. No. 41,064; Willmore F. Holbrow III, Reg. No. 41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W. Hoover II, Reg. No. 32,992; Libby H. Hope, Reg. No. 46,774; Eric S. Hyman, Reg. No. 30,139; William W. Kidd, Reg. No. 31,772; Walter T. Kim, Reg. No. 42,731; Eric T. King, Reg. No. 44,188; Steve Laut, Reg. No. 47,736; Suk S. Lee, Reg. No. 47,745; Gordon R. Lindeen III, Reg. No. 33,192; Jan C. Little, Reg. No. 41,181; Julio Loza, Reg. No. 47,758; Joseph Lutz, Reg. No. 43,765; Lawrence Lycke, Reg. No. 38,540; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, Reg. No. 48,095; Raul D. Martinez, Reg. No. 46,904; Paul A. Mendonsa, Reg. No. 42,879; Clive D. Menezes, Reg. No. 45,493; Jonathan S. Miller, Reg. No. 48,534; Richard A. Nakashima, Reg. No. 42,023; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Robert B. O'Rourke, Reg. No. 46,972; Daniel E. Ovanezian, Reg. No. 41,236; Gregg A. Peacock, Reg. No. 45,001; Marina Portnova, Reg. No. 45,750; Michael A. Proksch, Reg. No. 43,021; William F. Ryann, Reg. No. 44,313; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Jeffrey S. Schubert, Reg. No. 43,098; Saina S. Shamilov, Reg. No. 48,266; Kevin G. Shao, Reg. No. 45,095; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Ronald S. Tamura, Reg. No. 43,179; Edwin H. Taylor, Reg. No. 25,129; Lance A. Termes, Reg. No. 43,184; John F. Travis, Reg. No. 43,203; Thomas J. Treutler, Reg. No. 51,126; Kerry D. Tweet, Reg. No. 45,959; Mark C. Van Ness, Reg. No. 39,865; Thomas A. Van Zandt, Reg. No. 43,219; Lester J. Vincent, Reg. No. 31,460; Archana B. Vittal, Reg. No. 45,182; Glenn E. Von Tersch, Reg. No. 41,364; John P. Ward, Reg. No. 40,216; Mark L. Watson, Reg. No. 46,322; Thomas C. Webster, Reg. No. 46,154; Linda S. Zachariah, Reg. No. 48,057; and Norman Zafman, Reg. No. 26,250; my patent attorneys, and William E. Hickman, Reg. No. 46,771, Brent E. Vecchia, Reg. No. 48,011, and Lehua Wang, Reg. No. 48,023; my patent agents, of BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and James R. Thein, Reg. No. 31,710, my patent attorney with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56 Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

(e) In any continuation-in-part application, the duty under this section includes the duty to disclose to the Office all information known to the person to be material to patentability, as defined in paragraph (b) of this section, which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 2001

Application or Docket Number

3771p003

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	61	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	61 - minus 20 =	* 41
INDEPENDENT CLAIMS	8 - minus 3 =	* 5
MULTIPLE DEPENDENT CLAIM PRESENT ☐		

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**
Independent	*	Minus	***
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**
Independent	*	Minus	***
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**
Independent	*	Minus	***
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SMALL ENTITY

TYPE ☐

OR

OTHER THAN

SMALL ENTITY

RATE	FEE
BASIC FEE	370.00
X\$ 9=	
X42=	
+140=	
TOTAL	

RATE	FEE
BASIC FEE	740.00
X\$18=	738.00
X84=	120.00
+280=	
TOTAL	1158.00

SMALL ENTITY

OR

OTHER THAN

SMALL ENTITY

RATE	ADDITIONAL FEE
X\$ 9=	
X42=	
+140=	
TOTAL	

RATE	ADDITIONAL FEE
X\$18=	
X84=	
+280=	
TOTAL	

RATE	ADDITIONAL FEE
X\$ 9=	
X42=	
+140=	
TOTAL	

RATE	ADDITIONAL FEE
X\$18=	
X84=	
+280=	
TOTAL	

RATE	ADDITIONAL FEE
X\$ 9=	
X42=	
+140=	
TOTAL	

RATE	ADDITIONAL FEE
X\$18=	
X84=	
+280=	
TOTAL	

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

08/15/2002 WABRHAM1 00000045 10217758

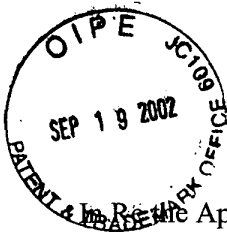
01 FC:101	740.00	OP
02 FC:103	738.00	OP
03 FC:102	420.00	OP

PTO-1556
(5/87)

*U.S. Government Printing Office: 2001 — 481-697/59173

3280

Docket No.: 3771P003



72

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Reply, Please Refer to the Application of:

DANIEL E. GRUPP, ET AL.

Application No.: 10/217,758

Filed: August 12, 2002

For: **Method For Depinning The Fermi Level of
a Semiconductor at an Electrical Junction
and Devices Incorporation Such Junctions**

Art Group:

Examiner:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

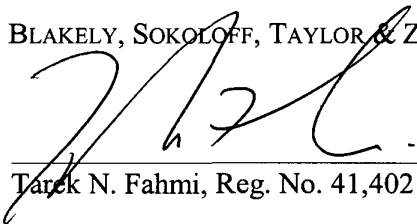
In accordance with the duty of disclosure, enclosed is a copy of Information Disclosure Statement by Applicant (form PTO/SB/08), which is being submitted within three (3) months of filing of the application. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s). Copies of the references cited on PTO/SB/08 are enclosed herewith.

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP



Tarek N. Fahmi, Reg. No. 41,402

Date: September 16, 2002

12400 Wilshire Blvd., 7th Floor
Los Angeles, California 90025
(408) 947-8200

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class mail with sufficient postage in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on:



Monique M. Pearson

9/16/02
Date

Substitute for Form 1449A/PTO (Modified)

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

SEP 19 2002

Sheet

of

6

Complete if Known

Application Number	10/217,758
Filing Date	August 12, 2002
First Named Inventor:	Daniel E. Grupp
Group Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	3771P003

U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Code ²	Kind (If known)			
		3,590,471		Lepselter et al.	7/6/71	
		3,708,360		Wakefield, Jr., et al.	1/2/73	
		4,300,152		Lepselter	11/10/81	
		4,485,550		Koeneke et al.	12/4/84	
		5,399,206		de Lyon	3/21/95	
		5,612,567		Baliga	3/18/97	
		5,663,584		Welch	9/2/97	
		5,801,398		Hebiguchi	9/1/98	
		5,888,891		Gould	3/30/99	
		5,939,763		Hao, et al.	8/17/99	
		6,037,605		Yoshimura	3/14/00	
		6,096,590		Chan et al.	8/1/00	
		6,150,286		Sun, et al.	11/21/00	
		6,198,113	B1	Grupp	3/6/01	
		6,207,976	B1	Takahashi et al.	3/27/01	
		6,261,932	B1	Hulfachor	7/17/01	
		6,291,866		Wallace, et al.	9/18/01	
		6,291,867		Wallace, et al.	9/18/01	
		6,303,479	B1	Snyder	10/16/01	
		5,596,218	B1	Soleimani, et al.	01-21-1997	
		5,578,848		Kwong, et al.	11-26-1996	

FOREIGN PATENT DOCUMENTS

Exam. Initial*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (If known)				

Examiner
Signature

Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Unique citation designation number. ²See attached Kinds of U.S. Patent Documents. ³Enter Office that issued the document, by the two-letter code (WIPO Standard S.3). ⁴For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Substitute for Form 1449A/PTO (Modified)

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

SEP 19 2002

Sheet

2

off#

6

Complete if Known

Application Number	10/217,758
Filing Date	August 12, 2002
First Named Inventor:	Daniel E. Grupp
Group Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	3771P003

OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
	f	M.C. Gilmer et al., "Process and Manufacturing Challenges for High-K Gate Stack Systems", Mat. Res. Soc. Symp. Proc. Vol. 567, (1999), pp. 323-341	
	b	John P. Snyder et al., "Experimental Investigation of a PtSi Source and Drain Field Emission Transistor", American Institute of Physics", pp. 1-3	
	q	Chung-Kuang Huang, Wei E. Zhang and C. H. Yang, "Two-Dimensional Numerical Simulation of Schottky Barrier MOSFET with Channel Length to 10 nm", IEEE, pp. 842-848	
	o	S. Hara et al., "Control of Schottky and Ohmic Interfaces by Unpinning Fermi Level", Elsevier Science B.V., pp. 394-399	
	o	S. Hara et al., "Pinning-Controlled Ohmic Contacts: Application to SiC(0001), Elsevier Science B.V., pp. 218-221	
	1	S. Hara, et al., "Pinning-Controlled Metal/Semiconductor Interfaces", Electrotechnical Laboratory, pp. 802-807	
	#	http://www.rciqu.hokudai.ac.jp/RCIQEold/ResearchAchievements.html , downloaded on 4/12/02	
	f	I. Shalish et al., "Yellow Luminescence and Fermi Level Pinning in GaN Layers", American Institute of Physics", Vol., 77, No. 7, (8/14/00) pp. 987-989	
	e	Andreas Mandelis and R. Arief Budiman, "Evidence of a Surface Acceptor State in Undoped Semi-Insulating GaAs by Photothermal Radiometric Deep Level Transient Spectroscopy", Sociedad Mexicana de Ciencias de Superficies y de Vacio, (1999) pp. 13-17	
	t	TAKHEE LEE, JAI LIU, NIEN-PO CHEN, R.P. ANDRES, D.B. JANES, AND R. REIFENBERGER; "Electronic Property of Metallic Nanoclusters on Semiconductor Surfaces: Implications for Nanoelectronic Device Applications"; Journal of Nanoparticle Research 2; pp 345-362; 2000.	
	t	Y.K. KIM AND SEHUN KIM; "Metal-Dependent Fermi-Level Movement in the Metal/Sulfur-Passivated InGaP Contact"; J. Vac Sci. Technol. A 15(3); pp. 1124-1128; May/June 1997.	

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Substitute for Form 1449A/PTO (Modified) INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary) SEP 19 2002		Complete if Known <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Application Number</td> <td>10/217,758</td> </tr> <tr> <td>Filing Date</td> <td>August 12, 2002</td> </tr> <tr> <td>First Named Inventor:</td> <td>Daniel E. Grupp</td> </tr> <tr> <td>Group Art Unit</td> <td>Not Yet Assigned</td> </tr> <tr> <td>Examiner Name</td> <td>Not Yet Assigned</td> </tr> <tr> <td>Attorney Docket Number</td> <td>3771P003</td> </tr> </table>		Application Number	10/217,758	Filing Date	August 12, 2002	First Named Inventor:	Daniel E. Grupp	Group Art Unit	Not Yet Assigned	Examiner Name	Not Yet Assigned	Attorney Docket Number	3771P003
Application Number	10/217,758														
Filing Date	August 12, 2002														
First Named Inventor:	Daniel E. Grupp														
Group Art Unit	Not Yet Assigned														
Examiner Name	Not Yet Assigned														
Attorney Docket Number	3771P003														
Sheet	off#	6													
OTHER ART - NO PATENT LITERATURE DOCUMENTS															
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²												
	b	HIDEKI HASEGAWA, TAKETOMO SATE, SEIYA KASAI; "Unpinning of Fermi Level in Nanometer-Sized Schottky Contacts on GaAs and InP"; Research Center for Interface Quantum Electronics and Graduate School of Electronics and Info. Eng, Hokkaido Univ., Japan; pp. 92-96; 2000;													
	b	P. BAUERNSCHMITT ET AL; "Yb-SiO ₂ -Si Tunneling Junctions"; Elsevier Publishers B.V.; pp. 105-108; 1993.													
		NAOYA OKAMOTO, TSUYOSHI TAKAHSHI, TANAKA & MASAHICO TAKIKAWA; "Near-Ohmic Contact of n-GaAs with Ga/GaAs Quasi-Metal-Insulator-Semiconductor Structure"; Jpn. J. Appl. Phys., Vol. 37 (1998) pp. 32483251.													
		J. TERSOFF; "Schottky Barrier Heights and the Continuum of Gap States" Physical Review Letters, vol. 52, No. 6; February 6, 1984; AT & T Bell Lab., Murphy Jill, New Jersey 07974.													
		VOLKER HEINE; "Theory of Surface States"; Physical Review Letters, vol. 138 No. 6A, June 4, 1965; Tell Telephone Lab., Murphy Jill, New Jersey.													
		STEVEN G. LOUIE, JAMES R. CHELOKOWSKY, MARVIN L. COHEN; "Ionicity and the Theory of Schottky Barriers"; Physical Review Letters, vol. 15 No. 4, February 15, 1977; Dept. of Phys. Univ. of California, and Materials and Molecular Research Div., Lawrence Berkley Lab., Berkley, CA 94720.													
		W.E. SPICER, I. LINDAU, P. SKEATH, C.Y. SU, PATRICK CHYE; "Unified Mechanism for Schottky-Barrier Formation and III-V Oxide Interface States"; Physical Review Letters, Vol. 44, No. 6, Stanford Electronics Lab., Stanford Univ., Stanford, CA 94305; February 11, 1980, pp. 420-423.													
		D.J. CHADI, P.H. CITRIN, C.H. PARK, D.L. ADLER, M.A. MARCUS, H.J. GOSSMAN; "Fermi-Level-Pinning Defects in Highly n-Doped Silicon"; Physical Review Letters, Vol. 79, No. 24, December 1997; NEC Research Institute, Princeton, New Jersey 08540-6634; pp. 4834-4837.													
		R.A. MCKEE, F.J. WALKER, M.F. CHISHOLM; "Physical Structure and Inversion Charge at a Semiconductor Interface with a Crystalline Oxide"; www.sciencemag.org , Vol. 293; July 20, 2001; pp. 468-469.													
		F.A. PADOVANI; "Forward Voltage-Current Characteristics of Metal-Silicon Schottky Barriers"; Texas Instruments, Inc., Dallas Texas; September 15, 1966; pp. 892-892.													
		R.T. TUNG; "Electron Transport of Inhomogeneous Schottky Barriers; AT & T Bell Lab., Murray hill, New Jersey 07974; March 21, 1991; 3832-3834.													

Examiner Signature	Date Considered
--------------------	-----------------

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Substitute for Form 1449A/PTO (Modified) INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Complete if Known		
			Application Number	10/217,758	
			Filing Date	August 12, 2002	
			First Named Inventor:	Daniel E. Grupp	
			Group Art Unit	Not Yet Assigned	
			Examiner Name	Not Yet Assigned	
Sheet	4	off#	6	Attorney Docket Number	3771P003

OTHER ART – NO PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
		M. MIYAWAK, I S. YOSHITAKE, TADAHIRO OHMI; "Improvement of Aluminum-Si Contact Performance in Native-Oxide-Free Processing"; IEEE Electron Device Letters, vol. 11, No. 10, October 1990; pp. 448-450.	
		MITSUTERU KINURA; TADASHI MATUSADATE; "A New Type of Schottky Tunnel Transistor"; IEEE Electron Device Letters, vol. 15, no. 10; October 1994; pp. 412-414.	
		FENG-JUNG HUANG, K.K.O.; "Metal-Oxide Semiconductor field-Effect Transistors Using Schottky Barrier Drains"; Electronics Letters, vol. 33, no. 15; July 17, 1997; pp. 1341-1342.	
		LIE WANG AND M.I. NATHAN; "High BARRIER GaN Schottky Diodes: Pt/GaN and Pd/GaN"; Dept. of Electrical Eng., Univ. of Minnesota, Minneapolis, Minnesota 55455; Appl. Phys. Letters, Vol. 68 (9); February 26, 1996, pp/ 1267-1270.	
		B.J. ZHANG, T. EGAWA, G. Y. ZHAO, H. ISHIKAWA, M. UMENO; "Schottky Diodes of Ni/Au on n-GaN Grown on Sapphire and SiC Substrates"; Applied Physics Letters, Vol. 79, No. 16; October 15, 2001; pp. 2567-2569.	
		SATOSHI KAMIYAMA, PIERR-Yves LESAICHERRE, HIROSHI SUZIKI, AKIRA SAKAI, IWAO NISHIYAMA, AKIJIKO ISHITANI; "Ultrathin Tantalum Oxide Capacitor DIELECTRIC Layers Fabricated Using Rapid Thermal Nitridation Prior to Low Pressure Chemical Vapor Deposition"; J. Electrochem. Soc., vol. 140, no. 6; June 1993; The Electrochemical society, inc.; p. 1617.	
		C. CHANELOERE, J.L. AUTRAN, R.A.B. DEVINE, B. BALLAND; "Tantalum Pentoxide (Ta ₂ O ₅) Thin Films for Advanced Dielectric Applications"; Reports: a Review Journal; Materials Science and Engineering, R22 (1998) 269-322.	
		G.B. AKERS, L.A. STURLING, R.B. VANDOVER, J.P. CHANG, D.J. WERDER, R.URDDAHL, R.RAJOPALAN; "Effects of Thermal Stability and Roughness on Electrical Properties of Tantalus Oxide Gates"; Mat. Res., Soc. Symp. Proc, vol. 567 1999 Materials Research Society; pp. 391-395.	
		HANYANG YANG, HIRO NIIMI, JEFF W. KEISTER, GERALD LUCOVSKY, JACKIE. ROWE; "The Effects of Interfacial Sub-Oxide Transition Regions and Monolayer Level Nitridation on Tunneling Currents in Silicon Devices"; IEEE Electron Device Letters, vol. 21, no. 2; February 2000; pp. 76-78.	
		R.D. BRINGANSS; "Arsenic Passivation of Si and Ge Surfaces"; Critical Reviews in Solid State and Materials Sciences, 17(4): 353-395 (1992); pp. 353-395	

Examiner Signature	Date Considered
--------------------	-----------------

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Substitute for Form 1449A/PTO (Modified)

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

SEP 19 2002

Sheet

5

off#

6

Complete if Known

Application Number	10/217,758
Filing Date	August 12, 2002
First Named Inventor:	Daniel E. Grupp
Group Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	3771P003

OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
	9	J.R. PATEL, J.A. GOLOVCHENKO, P.E. FREELAND, H.J. GOSSMANN; "Arsenic Atom Location on Passive Silicon (111) Surfaces"; Physical Review B. Vol., 36, No. 14; November 15, 1987; pp. 7715-7717.	
	0	U.J.R. BAUMVOL; "Atomic Transport During Growth of Ultrathin Dielectrics on Silicon"; Surface Science Reports 36 (1999) 1-166.	
	0	S. VERHACERBEKE, J. ALAY, P. MERTENS, M. MEURIS, M. HEYNS, W. VANDERVOUES, M. MURREL, S. SOFIELD; "Surface Characterization of Si After HF Treatments and its Influence in the Dielectric Breakdown of Thermal Oxides"; Research Aspirant of the Belgium National Fund for Scientific Research; Mat. Res. Soc. Symp. Proc., Vol. 259; 1992 Material Research Society; pp. 391-399.	
	0	T.I. KAMINS, K. NAUKA; "Effect of Hydrogen on p-Type Epitaxial Silicon Sheet-Resistance Measurements"; Electrochemical and Solid-State Letters 1(2) 100-101 (1998); pp. 100-101.	
	0	PETER J. WRIGHT, NAIKI KASAI; "Hot-Electron Immunity of SiO ₂ Dielectrics with Fluorine Incorporation"; IEEE Electron Device Letters, vol. 10, No. 8; August 8, 1989; pp. 347-348.	
	0	YASUSHIRO NOSHIOKA, YUZURU OHJI, KIICHIRO MUKAI; "Dielectric Characteristics of Forinated Ultradry SiO ₂ "; Appl. Phys. Letters 54(12); March 20, 1989; pp. 1127-1129.	
	0	C.L. CHEN, T.S. CHAO, C.S. LAI, T.Y. HUANG; "High Quality Native-Oxide-Free Untrathin Oxide Grown by In-Situ HF-Vapor Treatment"; Electronic Letters, vol. 36, no. 11; pp. 981-983; May 25, 2000.	
	0	J. HILSENBECK, E. NEBAUER, J. WÜRFL, TRÄNKLE, H. OBLOH; "Aging Behavior of Algan HFETs with Advanced Ohmic and Schottky Contacts"; Electronic letters, vol. 36, NO. 11; pp. 980-981; May 25, 2000.	
	0	HIROTO IZUMI, STELLA CHEMIFA; "43. Hydrogen Termination: The Ideally Finished Silicon Surface"; Ultraclean Surface Processing of Silicon Wafers: Secrets of Vlsi Manufacturing http://halloftechnology.com/electrical_optical/986.shtml ; November, 1998	
	0	K. NAUKA, T.I. KAMINS; "Surface Photovoltage Measurement of Hydrogen-Treated Si Surfaces"; Journal of Electrochemical Society, 146 (1) 292-295 (1999).	
	0	E. YABLONOVITCH, D.L. ALLARA, C.C. CHANG, T. GMITTER, T.B. BRIGHT; "Unusually low Surface-Recombination Velocity on Silicon and Germanium Surfaces"; Physical Review Letters, vol. 57, no. 2, pp. 249-252; July 14, 1986.	

Examiner
SignatureDate
Considered

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Substitute for Form 1449A/PTO (Modified) INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	10/217,758
				Filing Date	August 12, 2002
				First Named Inventor:	Daniel E. Grupp
				Group Art Unit	Not Yet Assigned
				Examiner Name	Not Yet Assigned
				Attorney Docket Number	3771P003
Sheet	6	off#	6		
OTHER ART - NO PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			
		B.R. WEINBERGER, G.G. PETERSON, T.C. ESCRICH, H.A. KRASINSKI; "Surface Chemistry of HF Passivation Silicon: X-Ray Photoelectron and Ion Scattering Spectroscopy Results"; J. Appl. Phys. 60(9), pp. 3232-3234; November 1, 1986.			
		LAHIR SHAIK ADAM, MARK E. LAW; "Experimental Identification of Nitrogen-Vacancy Complexes in Nitrogen Implanted Silicon"; Applied Physics Letters, vol. 79, No. 5, pp. 623-625; July 30, 2001.			
		R.M.C. DE ALMEIDA, I.R.J. BAUMVOL; "Reaction-Diffusion Model for Thermal Growth of Silicon Nitride Films on Si"; Physical Review B, vol. 62, No. 24, pp. R16 255- R16 258; December 15, 2000.			
		YUNIARTO WIDJAJA, MICHAEL M. MYSINGER, CHARLES B. MUSGRAVE; "Ab Initio Study and Decomposition of NH ₃ on Si(100)-(2x1); J. Phy. Chem B 2000; pp. 2527-2533.			
		ARMIN G. ABERLE, THOMAS LAUINGER, JAN SCHMIDT, RUDOLF HEZEL; "Injection-Level Dependent Surface Recombination Velocities at the Silicon-Plasma Silicon Nitride Interface"; Institut für Solarenergieforschung, ISFH, D-3 1860 Emmerthal, Germany; pp. 2828-2830; March 9, 1995.			
		L. CAI, A. ROHATGI, G. MAY; "Investigation of the Properties of Plasma-Enhanced Chemical Vapor Deposition Silicon Nitride and its effect on Silicon Surface Passivation"; Journal of Applied Physics, vol. 83, no. 11, pp. 5885-5889; June 1, 1998.			
		JAN SCHMIDT, ARMIN G. ABELE; "Carrier Recombination at Silicon-Silicon Nitride Interfaces Fabricated by Plasma-Enhanced Chemical Vapor Deposition"; Journal of Applied Physics, vol. 85, no. 7, pp. 3626-3633; April 1, 1999.			
		Y. HAYAFUJI, K. KAJIWARA; "Nitridation of Silicon and Oxidized-Silicon"; Sony Corp. Research Center, 174 Fujitsuka-Cho, Hodogaya-Ku, Yokohama, 240 Japan; J. Electrochem. Soc.: Solid State Science and Technology; September 1982.			
		S.A. WOLF, D.D. AWSCHALOM, R.A. BUHRMAN, J.M. DAUGHTON, S. VON MOLNAR, M.L. ROUKES, A.Y. CHTCHELKANOVA, D.M. TREGER; "Spintronics: A Spin-Based Vision for the Future"; www.sciencemag.org , vol. 294, pp. 1488; November 16, 2001.			

Examiner Signature	Date Considered
--------------------	-----------------

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

L Number	Hits	Search Text	DB	Time stamp
1	322715	((("257") or ("438"))).CLAS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/27 20:06
2	2661	((("257") or ("438"))).CLAS.) and fermi	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/27 20:08
3	1599	((((("257") or ("438"))).CLAS.) and fermi) and interface	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/27 20:09
4	1018	(((((("257") or ("438"))).CLAS.) and fermi) and interface) and resistance	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/27 20:10

Search History



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

08791 7590 10/07/2003

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD, SEVENTH FLOOR
LOS ANGELES, CA 90025

EXAMINER

NGO, NGAN V

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 10/07/2003

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/217,758	08/12/2002	Daniel E. Grupp	3771P003	1710

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$0	\$1330	01/07/2004

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. **PROSECUTION ON THE MERITS IS CLOSED.** THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN **THREE MONTHS** FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. **THIS STATUTORY PERIOD CANNOT BE EXTENDED.** SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status is changed, pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above and notify the United States Patent and Trademark Office of the change in status, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check the box below and enclose the PUBLICATION FEE and 1/2 the ISSUE FEE shown above.

☐ Applicant claims SMALL ENTITY status.
See 37 CFR 1.27.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail

**Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
(703) 746-4000**

or Fax

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

08791 7590 10/07/2003

**BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD, SEVENTH FLOOR
LOS ANGELES, CA 90025**

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/217,758	08/12/2002	Daniel E. Grupp	3771P003	1710

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPL.N. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$0	\$1330	01/07/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGO, NGAN V	2814	257-030000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1	_____
2	_____
3	_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY AND STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent); ☐ individual ☐ corporation or other private group entity ☐ government

4a. The following fee(s) are enclosed:

- ☐ Issue Fee
- ☐ Publication Fee
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

- ☐ A check in the amount of the fee(s) is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

Director for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature)

(Date)

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Alexandria, Virginia 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.** SEND TO: Commissioner for Patents, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMIT THIS FORM WITH FEE(S)



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/217,758	08/12/2002	Daniel E. Grupp	3771P003	1710
08791	7590	10/07/2003	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD, SEVENTH FLOOR LOS ANGELES, CA 90025			NGO, NGAN V	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 10/07/2003

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) system (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (703) 305-1383. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/217,758	08/12/2002	Daniel E. Grupp	3771P003	1710
08791	7590	10/07/2003	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD, SEVENTH FLOOR LOS ANGELES, CA 90025			NGO, NGAN V	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 10/07/2003

Notice of Fee Increase on October 1, 2003

If a reply to a "Notice of Allowance and Fee(s) Due" is filed in the Office on or after October 1, 2003, then the amount due will be higher than that set forth in the "Notice of Allowance and Fee(s) Due" since there will be an increase in fees effective on October 1, 2003. See Revision of Patent Fees for Fiscal Year 2004; Final Rule, 68 Fed. Reg. 41532, 41533, 41534 (July 14, 2003).

The current fee schedule is accessible from (<http://www.uspto.gov/main/howtofees.htm>).

If the fee paid is the amount shown on the "Notice of Allowance and Fee(s) Due" but not the correct amount in view of the fee increase, a "Notice of Pay Balance of Issue Fee" will be mailed to applicant. In order to avoid processing delays associated with mailing of a "Notice of Pay Balance of Issue Fee," if the response to the Notice of Allowance is to be filed on or after October 1, 2003 (or mailed with a certificate of mailing on or after October 1, 2003), the issue fee paid should be the fee that is required at the time the fee is paid. If the issue fee was previously paid, and the response to the "Notice of Allowance and Fee(s) Due" includes a request to apply a previously-paid issue fee to the issue fee now due, then the difference between the issue fee amount at the time the response is filed and the previously-paid issue fee should be paid. See Manual of Patent Examining Procedure, Section 1308.01 (Eighth Edition, August 2001).

Effective October 1, 2003, 37 CFR 1.18 is amended by revising paragraphs (a) through (c) to read as set forth below.

Section 1.18 Patent post allowance (including issue) fees.

- (a) Issue fee for issuing each original or reissue patent, except a design or plant patent:
- By a small entity (Sec. 1.27(a))..... \$665.00
 - By other than a small entity..... \$1,330.00
- (b) Issue fee for issuing a design patent:
- By a small entity (Sec. 1.27(a))..... \$240.00
 - By other than a small entity..... \$480.00
- (c) Issue fee for issuing a plant patent:
- By a small entity (Sec. 1.27(a))..... \$320.00
 - By other than a small entity..... \$640.00

Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

Notice of Allowability

Application No.

10/217,758

Applicant(s)

GRUPP ET AL.

Examiner

Ngan Ngo

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.
2. ☒ The allowed claim(s) is/are 1-61.
3. ☐ The drawings filed on _____ are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
- * Certified copies not received: _____.
5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 - (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
8. ☒ CORRECTED DRAWINGS must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No. _____.
 - (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
 - (c) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. 0803.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet.

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|---|
| 1 ☒ Notice of References Cited (PTO-892) | 2 ☐ Notice of Informal Patent Application (PTO-152) |
| 3 ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | 4 ☐ Interview Summary (PTO-413), Paper No. _____ |
| 5 ☒ Information Disclosure Statements (PTO-1449), Paper No. <u>0902</u> . | 6 ☒ Examiner's Amendment/Comment |
| 7 ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material | 8 ☒ Examiner's Statement of Reasons for Allowance |
| | 9 ☐ Other |


Ngan Van Ngo
Primary Examiner

Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

In the specification:

Page 1, line 4, after "Application No.", insert -- 10/342,576 --;

Line 6, after "filed on", insert -- January 14, 2003 --;

Line 7, delete "2002".

Page 30, line 10, after "Application No.", insert -- 10/342,576 --;

Line 12, after "filed", insert -- January 14, 2003 --;

Line 12, delete "2002".

In the drawings:

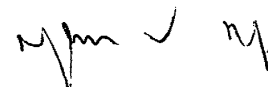
Figures 3 and 4 are labeled "PRIOR ART". See MPEP 608.02(g).

Any inquiry concerning this communication should be directed to Examiner Ngan Ngo at telephone number (703) 308-4938. The fax number for the Art unit is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Ngan Ngo

8/27/03

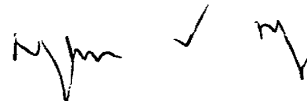

Ngan Van Ngo
Primary Examiner

Reasons for Allowance

The following is an examiner's statement of reasons for allowance:

The prior arts of record do not teach the electrical device comprising a metal, a silicon-based semiconductor having a Fermi level, an interface layer configured to depin the Fermi level of the semiconductor in which the electrical device has a specific contact resistance of less than or equal to $1000 \text{ Ohms-}\mu\text{m}^2$.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

A handwritten signature in black ink, appearing to read 'Ngan Van Ngo', with a checkmark and a small mark to its right.

Ngan Van Ngo
Primary Examiner

Notice of References Cited	Application/Control No. 10/217,758	Applicant(s)/Patent Under Reexamination GRUPP ET AL.	
	Examiner Ngan Ngo	Art Unit 2814	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2003/0127700 A1	07-2003	Moddel et al.	257/425
*	B	US-5,098,859	03-1992	Jackson et al.	438/509
*	C	US-4,583,110	04-1986	Jackson et al.	257/734
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Substitute for Form 1449A/PTO (Modified)

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet

6 of 6

Complete if Known

Application Number	10/217,758
Filing Date	August 12, 2002
First Named Inventor:	Daniel E. Grupp
Group Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	3771P003

U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Code ²	Kind (If known)			
		3,590,471		Lepselter et al.	7/6/71	
		3,708,360		Wakefield, Jr., et al.	1/2/73	
		4,300,152		Lepselter	11/10/81	
		4,485,550		Koeneke et al.	12/4/84	
		5,399,206		de Lyon	3/21/95	
		5,612,567		Baliga	3/18/97	
		5,663,584		Welch	9/2/97	
		5,801,398		Hebiguchi	9/1/98	
		5,888,891		Gould	3/30/99	
		5,939,763		Hao, et al.	8/17/99	
		6,037,605		Yoshimura	3/14/00	
		6,096,590		Chan et al.	8/1/00	
		6,150,286		Sun, et al.	11/21/00	
		6,198,113	B1	Grupp	3/6/01	
		6,207,976	B1	Takahashi et al.	3/27/01	
		6,261,932	B1	Hulfachor	7/17/01	
		6,291,866		Wallace, et al.	9/18/01	
		6,291,867		Wallace, et al.	9/18/01	
		6,303,479	B1	Snyder	10/16/01	
		5,596,218	B1	Soleimani, et al.	01-21-1997	
		5,578,848		Kwong, et al.	11-26-1996	

FOREIGN PATENT DOCUMENTS

Exam. Initial*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (If known)				

Examiner
Signature

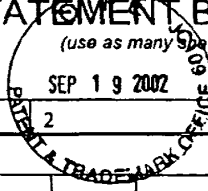
[Signature]

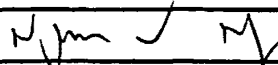
Date Considered
8-27-03

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Unique citation designation number. ²See attached Kinds of U.S. Patent Documents. ³Enter Office that issued the document, by the two-letter code (WIPO Standard S.3). ⁴For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Substituted for Form 1449A/PTO (Modified) INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary) 		Complete if Known <table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td>Application Number</td><td>10/217,758</td></tr> <tr><td>Filing Date</td><td>August 12, 2002</td></tr> <tr><td>First Named Inventor:</td><td>Daniel E. Grupp</td></tr> <tr><td>Group Art Unit</td><td>Not Yet Assigned</td></tr> <tr><td>Examiner Name</td><td>Not Yet Assigned</td></tr> <tr><td>Attorney Docket Number</td><td>3771P003</td></tr> </table>		Application Number	10/217,758	Filing Date	August 12, 2002	First Named Inventor:	Daniel E. Grupp	Group Art Unit	Not Yet Assigned	Examiner Name	Not Yet Assigned	Attorney Docket Number	3771P003
Application Number	10/217,758														
Filing Date	August 12, 2002														
First Named Inventor:	Daniel E. Grupp														
Group Art Unit	Not Yet Assigned														
Examiner Name	Not Yet Assigned														
Attorney Docket Number	3771P003														
Sheet	2	of #	6												
OTHER ART - NO PATENT LITERATURE DOCUMENTS															
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²												
N	1	M.C. Gilmer et al., "Process and Manufacturing Challenges for High-K Gate Stack Systems", Mat. Res. Soc. Symp. Proc. Vol. 567, (1999), pp. 323-341													
	2	John P. Snyder et al., "Experimental Investigation of a PtSi Source and Drain Field Emission Transistor", American Institute of Physics", pp. 1-3													
	3	Chung-Kuang Huang, Wei E. Zhang and C. H. Yang, "Two-Dimensional Numerical Simulation of Schottky Barrier MOSFET with Channel Length to 10 nm", IEEE, pp. 842-848													
	4	S. Hara et al., "Control of Schottky and Ohmic Interfaces by Unpinning Fermi Level", Elsevier Science B.V., pp. 394-399													
	5	S. Hara et al., "Pinning-Controlled Ohmic Contacts: Application to SiC(0001), Elsevier Science B.V., pp. 218-221													
	6	S. Hara, et al., "Pinning-Controlled Metal/Semiconductor Interfaces", Electrotechnical Laboratory, pp. 802-807													
	7	http://www.rciq.hokudai.ac.jp/RCIQEold/ResearchAchievements.html , downloaded on 4/12/02													
	8	I. Shalish et al., "Yellow Luminescence and Fermi Level Pinning in GaN Layers", American Institute of Physics", Vol. 77, No. 7, (8/14/00) pp. 987-989													
	9	Andreas Mandelis and R. Arief Budiman, "Evidence of a Surface Acceptor State in Undoped Semi-Insulating GaAs by Photothermal Radiometric Deep Level Transient Spectroscopy", Sociedad Mexicana de Ciencias de Superficies y de Vacio, (1999) pp. 13-17													
	10	TAKHEE LEE, JAI LIU, NIEN-PO CHEN, R.P. ANDRES, D.B. JAMES, AND R. REIFENBERGER; "Electronic Property of Metallic Nanoclusters on Semiconductor Surfaces: Implications for Nanoelectronic Device Applications"; Journal of Nanoparticle Research 2; pp 345-362; 2000.													
N	11	Y.K. KIM AND SEHUN KIM; "Metal-Dependent Fermi-Level Movement in the Metal/Sulfur-Passivated InGaP Contact"; J. Vac. Sci. Technol. A 15(3); pp. 1124-1128; May/June 1997.													

Examiner Signature: 	Date Considered: 8-27-03
---	--------------------------

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Substitute for Form 1449A/PTO (Modified)		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	10/217,758
		Filing Date	August 12, 2002
		First Named Inventor:	Daniel E. Grupp
		Group Art Unit	Not Yet Assigned
		Examiner Name	Not Yet Assigned
		Attorney Docket Number	3771P003
Sheet	6 of 6		
OTHER ART - NO PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
W	8	HIDEKI HASEGAWA, TAKETOMO SATE, SEIYA KASAI; "Unpinning of Fermi Level in Nanometer-Sized Schottky Contacts on GaAs and InP"; Research Center for Interface Quantum Electronics and Graduate School of Electronics and Info. Eng, Hokkaido Univ., Japan; pp. 92-96; 2000;	
	9	P. BAUERNSCHMITT ET AL; "Yb-SiO ₂ -Si Tunneling Junctions"; Elsevier Publishers B.V.; pp. 105-108; 1993.	
		NAOYA OKAMOTO, TSUYOSHI TAKAHSHI, TANAKA & MASAHICO TAKIKAWA; "Near-Ohmic Contact of n-GaAs with Ga/GaAs Quasi-Metal-Insulator-Semiconductor Structure"; Jpn. J. Appl. Phys., Vol. 37 (1998) pp. 32483251.	
		J. TERSOFF; "Schottky Barrier Heights and the Continuum of Gap States" Physical Review Letters, vol. 52, No. 6; February 6, 1984; AT & T Bell Lab., Murphy Jill, New Jersey 07974.	
		VOLKER HEINE; "Theory of Surface States"; Physical Review Letters, vol. 138 No. 6A, June 4, 1965; Tell Telephone Lab., Murphy Jill, New Jersey.	
		STEVEN G. LOUIE, JAMES R. CHELOKOWSKY, MARVIN L. COHEN; "Ionicity and the Theory of Schottky Barriers"; Physical Review Letters, vol. 15 No. 4, February 15, 1977; Dept. of Phys. Univ. of California, and Materials and Molecular Research Div., Lawrence Berkley Lab., Berkley, CA 94720.	
		W.E. SPICER, I. LINDAU, P. SKEATH, C.Y. SU, PATRICK CHYE; "Unified Mechanism for Schottky-Barrier Formation and III-V Oxide Interface States"; Physical Review Letters, Vol. 44, No. 6, Stanford Electronics Lab., Stanford Univ., Stanford, CA 94305; February 11, 1980, pp. 420-423.	
		D.J. CHADI, P.H. CITRIN, C.H. PARK, D.L. ADLER, M.A. MARCUS, H.J. GOSSMAN; "Fermi-Level-Pinning Defects in Highly n-Doped Silicon"; Physical Review Letters, Vol. 79, No. 24, December 1997; NEC Research Institute, Princeton, New Jersey 08540-6634; pp. 4834-4837.	
		R.A. MCKEE, F.J. WALKER, M.F. CHISHOLM; "Physical Structure and Inversion Charge at a Semiconductor Interface with a Crystalline Oxide"; www.sciencemag.org , Vol. 293; July 20, 2001; pp. 468-469.	
		F.A. PADOVANI; "Forward Voltage-Current Characteristics of Metal-Silicon Schottky Barriers"; Texas Instruments, Inc., Dallas Texas; September 15, 1966; pp. 892-892.	
W		R.T. TUNG; "Electron Transport of Inhomogeneous Schottky Barriers; AT & T Bell Lab., Murray hill, New Jersey 07974; March 21, 1991; 3832-3834.	

Examiner Signature	<i>[Signature]</i>	Date Considered	8-27-03
--------------------	--------------------	-----------------	---------

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Substitute for Form 1449A/PTO (Modified)

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

SEP 19 2002

Sheet

4

off#

6

Complete if Known

Application Number	10/217,758
Filing Date	August 12, 2002
First Named Inventor:	Daniel E. Grupp
Group Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	3771P003

OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
fw		M. MIYAWAK, I.S. YOSHITAKE, TADAHIRO OHMI; "Improvement of Aluminum-Si Contact Performance in Native-Oxide-Free Processing"; IEEE Electron Device Letters, vol. 11, No. 10, October 1990; pp. 448-450.	
		MITUTERU KINURA; TADASHI MATSUDATE; "A New Type of Schottky Tunnel Transistor"; IEEE Electron Device Letters, vol. 15, no. 10; October 1994; pp. 412-414.	
		FENG-JUNG HUANG, K.K.O.; "Metal-Oxide Semiconductor field-Effect Transistors Using Schottky Barrier Drains"; Electronics Letters, vol. 33, no. 15; July 17, 1997; pp. 1341-1342.	
		LIE WANG AND M.I. NATHAN; "High BARRIER GaN Schottky Diodes: Pt/GaN and Pd/GaN"; Dept. of Electrical Eng., Univ. of Minnesota, Minneapolis, Minnesota 55455; Appl. Phys. Letters, Vol. 68 (9); February 26, 1996, pp/ 1267-1270.	
		B.J. ZHANG, T. EGAWA, G. Y. ZHAO, H. ISHIKAWA, M. UMENO; "Schottky Diodes of Ni/Au on n-GaN Grown on Sapphire and SiC Substrates"; Applied Physics Letters, Vol. 79, No. 16; October 15, 2001; pp. 2567-2569.	
		SATOSHI KAMIYAMA, PIERR-Yves LESAICHERRE, HIROSHI SUZIKI, AKIRA SAKAI, IWAO NISHIYAMA, AKIHIKO ISHITANI; "Ultrathin Tantalum Oxide Capacitor DIELECTRIC Layers Fabricated Using Rapid Thermal Nitridation Prior to Low Pressure Chemical Vapor Deposition"; J. Electrochem. Soc., vol. 140, no. 6; June 1993; The Electrochemical society, inc.; p. 1617.	
		C. CHANELOERE, J.L. AUTRAN, R.A.B. DEVINE, B. BALLAND; "Tantalum Pentoxide (Ta ₂ O ₅) Thin Films for Advanced Dielectric Applications"; Reports: a Review Journal; Materials Science and Engineering, R22 (1998) 269-322.	
		G.B. AKERS, L.A. STURLING, R.B. VANDOVER, J.P. CHANG, D.J. WERDER, R. URDDAHL, R. RAJOPALAN; "Effects of Thermal Stability and Roughness on Electrical Properties of Tantalum Oxide Gates"; Mat. Res., Soc. Symp. Proc, vol. 567 1999 Materials Research Society; pp. 391-395.	
		HANYANG YANG, HIRO NIIMI, JEFF W. KEISTER, GERALD LUCOVSKY, JACKIE ROWE; "The Effects of Interfacial Sub-Oxide Transition Regions and Monolayer Level Nitridation on Tunneling Currents in Silicon Devices"; IEEE Electron Device Letters, vol. 21, no. 2; February 2000; pp. 76-78.	
fw	1	R.D. BRINGANSS; "Arsenic Passivation of Si and Ge Surfaces"; Critical Reviews in Solid State and Materials Sciences, 17(4): 353-395 (1992); pp. 353-395	

Examiner Signature

fw

Date

Considered

8-27-03

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Substitute for Form 1449A/PTO (Modified) INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
SEP 19 2002 TRADEMARK OFFICE				Application Number	10/217,758
				Filing Date	August 12, 2002
				First Named Inventor:	Daniel E. Grupp
				Group Art Unit	Not Yet Assigned
				Examiner Name	Not Yet Assigned
Sheet	5	off#	6	Attorney Docket Number	3771P003
OTHER ART - NO PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			T ²
m	1	J.R. PATEL, J.A. GOLOVCHENKO, P.E. FREELAND, H.J. GOSSMANN; "Arsenic Atom Location on Passive Silicon (111) Surfaces"; Physical Review B. Vol., 36, No. 14; November 15, 1987; pp. 7715-7717.			
	2	U.J.R. BAUMVOL; "Atomic Transport During Growth of Ultrathin Dielectrics on Silicon"; Surface Science Reports 36 (1999) 1-166.			
	3	S. VERHACERBEKE, J. ALAY, P. MERTENS, M. MEURIS, M. HEYNS, W. VANDERVOUES, M. MURREL, S. SOFIELD; "Surface Characterization of Si After HF Treatments and its Influence in the Dielectric Breakdown of Thermal Oxides"; Research Aspirant of the Belgium National Fund for Scientific Research; Mat. Res. Soc. Symp. Proc., Vol. 259; 1992 Material Research Society; pp. 391-399.			
	4	T.I. KAMINS, K. NAUKA; "Effect of Hydrogen on p-Type Epitaxial Silicon Sheet-Resistance Measurements"; Electrochemical and Solid-State Letters 1(2) 100-101 (1998); pp. 100-101.			
	5	PETER J. WRIGHT, NAIKI KASAI; "Hot-Electron Immunity of SiO ₂ Dielectrics with Fluorin Incorporation"; IEEE Electron Device Letters, vol. 10, No. 8; August 8, 1989; pp. 347-348.			
	6	YASUSHIRO NOSHIOKA, YUZURU OHJI, KIICHIRO MUKAI; "Dielectric Characteristics of Forinated Ultradry SiO ₂ "; Appl. Phys. Letters 54(12); March 20, 1989; pp. 1127-1129.			
	7	C.L. CHEN, T.S. CHAO, C.S. LAI, T.Y. HUANG; "High Quality Native-Oxide-Free Ultrathin Oxide Grown by In-Situ HF-Vapor Treatment"; Electronic Letters, vol. 36, no. 11; pp. 981-983; May 25, 2000.			
	8	J. HILSENBECK, E. NEBAUER, J. WÜRFEL, TRÄNKLE, H. OBLOH; "Aging Behavior of Algan HFETs with Advanced Ohmic and Schottky Contacts"; Electronic letters, vol. 36, NO. 11; pp. 980-981; May 25, 2000.			
	9	HIROTO IZUMI, STELLA CHEMIFA; "43. Hydrogen Termination: The Ideally Finished Silicon Surface"; Ultraclean Surface Processing of Silicon Wafers: Secrets of Visi Manufacturing http://halloftechnology.com/electrical_optical/986.shtml ; November, 1998			
	10	K. NAUKA, T.I. KAMINS; "Surface Photovoltage Measurement of Hydrogen-Treated Si Surfaces"; Journal of Electrochemical Society, 146 (1) 292-295 (1999).			
m	11	E. YABLONOVITCH, D.L. ALLARA, C.C. CHANG, T. GMITTER, T.B. BRIGHT; "Unusually low Surface-Recombination Velocity on Silicon and Germanium Surfaces"; Physical Review Letters, vol. 57, no. 2, pp. 249-252; July 14, 1986.			
Examiner Signature				Date Considered	8-27-03

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Substitute for Form 1449A/PTO (Modified)				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary) SEP 19 2002 PATE TRADEMARK OFFICE				Application Number	10/217,758
				Filing Date	August 12, 2002
				First Named Inventor:	Daniel E. Grupp
				Group Art Unit	Not Yet Assigned
				Examiner Name	Not Yet Assigned
Sheet	6	off#	6	Attorney Docket Number	3771P003
OTHER ART - NO PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			T ²
W		B.R. WEINBERGER, G.G. PETERSON, T.C. ESCRICH, H.A. KRASINSKI; "Surface Chemistry of HF Passivation Silicon: X-Ray Photoelectron and Ion Scattering Spectroscopy Results"; J. Appl. Phys. 60(9), pp. 3232-3234; November 1, 1986.			
		LAHIR SHAIK ADAM, MARK E. LAW; "Experimental Identification of Nitrogen-Vacancy Complexes in Nitrogen Implanted Silicon"; Applied Physics Letters, vol. 79, No. 5, pp. 623-625; July 30, 2001.			
		R.M.C. DE ALMEIDA, I.R.J. BAUMVOL; "Reaction-Diffusion Model for Thermal Growth of Silicon Nitride Films on Si"; Physical Review B, vol. 62, No. 24, pp. R16 255- R16 258; December 15, 2000.			
		YUNIARTO WIDJAJA, MICHAEL M. MYSINGER, CHARLES B. MUSGRAVE; "Ab Initio Study and Decomposition of NH ₃ on Si(100)-(2x1); J. Phy. Chem B 2000; pp. 2527-2533.			
		ARMIN G. ABERLE, THOMAS LAUINGER, JAN SCHMIDT, RUDOLF HEZEL; "Injection-Level Dependent Surface Recombination Velocities at the Silicon-Plasma Silicon Nitride Interface"; Institut für Solarenergieforschung, ISFH, D-3 1860 Emmerthal, Germany; pp. 2828-2830; March 9, 1995.			
		L. CAI, A. ROHATGI, G. MAY; "Investigation of the Properties of Plasma-Enhanced Chemical Vapor Deposition Silicon Nitride and its effect on Silicon Surface Passivation"; Journal of Applied Physics, vol. 83, no. 11, pp. 5885-5889; June 1, 1998.			
		JAN SCHMIDT, ARMIN G. ABELE; "Carrier Recombination at Silicon-Silicon Nitride Interfaces Fabricated by Plasma-Enhanced Chemical Vapor Deposition"; Journal of Applied Physics, vol. 85, no. 7, pp. 3626-3633; April 1, 1999..			
		Y. HAYAFUJI, K. KAJIWARA; "Nitridation of Silicon and Oxidized-Silicon"; Sony Corp. Research Center, 174 Fujitsuka-Cho, Hodogaya-Ku, Yokohama, 240 Japan; J. Electrochem. Soc.: Solid State Science and Technology; September 1982.			
W		S.A. WOLF, D.D. AWSCHALOM, R.A. BUHRMAN, J.M. DAUGHTON, S. VON MOLNAR, M.L. ROUKES, A.Y. CHTCHELKANOVA, D.M. TREGER; "Spintronics: A Spin-Based Vision for the Future"; www.sciencemag.org, vol. 294, pp. 1488; November 16, 2001.			

Examiner Signature	<i>M/m</i> ✓ <i>M</i>	Date Considered	8-27-03
--------------------	-----------------------	-----------------	---------

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Issue Classification 	Application No.	Applicant(s)	
	10/217,758	GRUPP ET AL.	
	Examiner	Art Unit	
	Ngan Ngo	2814	

ISSUE CLASSIFICATION										
ORIGINAL				CROSS REFERENCE(S)						
CLASS	SUBCLASS			CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
257	30			257	485					
INTERNATIONAL CLASSIFICATION										
H0	I	L	39/00							
H0	I	L	31/108							
			/							
			/							
			/							
				NGÂN V. NGÔ PRIMARY EXAMINER GRUPP 2300				Total Claims Allowed: 61		
(Assistant Examiner) (Date) <i>M. Brunson</i> 9/5/03 (Legal Instruments Examiner) (Date)				(Primary Examiner) (Date) <i>Ngan Ngo</i> 8-27-03 (Date)				O.G. Print Claim(s) 12		O.G. Print Fig. 7D

☒ Claims renumbered in the same order as presented by applicant										☐ CPA		☐ T.D.		☐ R.1.47	
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	31	31	61	61		91		121		151		181		211
	2		32		62		92		122		152		182		212
	3		33		63		93		123		153		183		213
	4		34		64		94		124		154		184		214
	5		35		65		95		125		155		185		215
	6		36		66		96		126		156		186		216
	7		37		67		97		127		157		187		217
	8		38		68		98		128		158		188		218
	9		39		69		99		129		159		189		219
	10		40		70		100		130		160		190		220
	11		41		71		101		131		161		191		221
	12		42		72		102		132		162		192		222
	13		43		73		103		133		163		193		223
	14		44		74		104		134		164		194		224
	15		45		75		105		135		165		195		225
	16		46		76		106		136		166		196		226
	17		47		77		107		137		167		197		227
	18		48		78		108		138		168		198		228
	19		49		79		109		139		169		199		229
	20		50		80		110		140		170		200		230
	21		51		81		111		141		171		201		231
	22		52		82		112		142		172		202		232
	23		53		83		113		143		173		203		233
	24		54		84		114		144		174		204		234
	25		55		85		115		145		175		205		235
	26		56		86		116		146		176		206		236
	27		57		87		117		147		177		207		237
	28		58		88		118		148		178		208		238
	29		59		89		119		149		179		209		239
30	30	60	60		90		120		150		180		210		240

Index of Claims 	Application No.		Applicant(s)
	10/217,758		GRUPP ET AL.
	Examiner		Art Unit
	Ngan Ngo		2814

✓	Rejected
=	Allowed

-	(Through numeral) Cancelled
+	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claim		Date	
Final	Original		
1	1		
2	2		
3	3		
4	4		
5	5		
6	6		
7	7		
8	8		
9	9		
10	10		
11	11		
12	12		
13	13		
14	14		
15	15		
16	16		
17	17		
18	18		
19	19		
20	20		
21	21		
22	22		
23	23		
24	24		
25	25		
26	26		
27	27		
28	28		
29	29		
30	30		
31	31		
32	32		
33	33		
34	34		
35	35		
36	36		
37	37		
38	38		
39	39		
40	40		
41	41		
42	42		
43	43		
44	44		
45	45		
46	46		
47	47		
48	48		
49	49		
50	50		

Claim		Date	
Final	Original		
51	51		
52	52		
53	53		
54	54		
55	55		
56	56		
57	57		
58	58		
59	59		
60	60		
61	61		
62	62		
63	63		
64	64		
65	65		
66	66		
67	67		
68	68		
69	69		
70	70		
71	71		
72	72		
73	73		
74	74		
75	75		
76	76		
77	77		
78	78		
79	79		
80	80		
81	81		
82	82		
83	83		
84	84		
85	85		
86	86		
87	87		
88	88		
89	89		
90	90		
91	91		
92	92		
93	93		
94	94		
95	95		
96	96		
97	97		
98	98		
99	99		
100	100		

Claim		Date	
Final	Original		
101	101		
102	102		
103	103		
104	104		
105	105		
106	106		
107	107		
108	108		
109	109		
110	110		
111	111		
112	112		
113	113		
114	114		
115	115		
116	116		
117	117		
118	118		
119	119		
120	120		
121	121		
122	122		
123	123		
124	124		
125	125		
126	126		
127	127		
128	128		
129	129		
130	130		
131	131		
132	132		
133	133		
134	134		
135	135		
136	136		
137	137		
138	138		
139	139		
140	140		
141	141		
142	142		
143	143		
144	144		
145	145		
146	146		
147	147		
148	148		
149	149		
150	150		

Search Notes 	Application No.		Applicant(s)	
	10/217,758		GRUPP ET AL.	
	Examiner		Art Unit	
	Ngan Ngo		2814	

SEARCHED			
Class	Subclass	Date	Examiner
257	30,31 32,35	8-27-03	NW
	56,62		
	65,471		
	472		
	473		
	475		
	485		

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
257	all of subclass above	8-27-03	NW

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
BRS Search using EAST	8-27-03	NW

constructed in this fashion is a result of only bulk material properties, not properties of the surface. By way of example, the materials in such cases may be Al and Si, with a work function for Al of approximately $\Phi_M = 4.1$ eV and the electron affinity for Si of approximately $\chi_S = 4.05$ eV.

V. Transistors Containing Passivated Semiconductor Surfaces

[0082] The interface layers described herein may be used in connection with a semiconductor surface of a channel in a field effect transistor. That is, an interface layer may be disposed between a source and a channel, a channel and a drain, or both of an insulated gate field effect transistor. Such use of an interface layer is described in detail in co-pending U.S. Patent Application No.: 10/342,574 entitled "INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL", filed 1/14/02, 2002 by the present inventors, and assigned to the assignee of the present invention.

[0083] The source and drain contacts at the channel of a field effect transistor are examples of a broader category of metal-interface layer-semiconductor contacts that make up the present invention. In the past, such contacts generally comprised a silicide- n^+ -Si junction, which formed a somewhat "leaky" Schottky diode, with a Fermi level of the semiconductor pinned at the midgap. In contrast, the present invention provides a contact wherein the Fermi level of the metal is aligned with the conduction band of the semiconductor (e.g., as shown in Figure 7d). Note that in other cases, depending on the type of semiconductor material and conductors used, the Fermi level of the metal may align with the valence band of the semiconductor.

[0084] Although both types of junctions (i.e., the new passivated Schottky barrier junction and the conventional silicide-semiconductor junction) permit tunneling currents, the present junction can be fabricated with a much thinner interface layer as compared to the thickness of the silicide layer used previously. Indeed, thickness of an order of magnitude less than the silicide thickness can be expected. In a conventional silicide – semiconductor junction a



01/17/2003
01/17/2003
01/17/2003

**PETITION FOR REVIVAL OF AN APPLICATION FOR PATENT
ABANDONED FOR FAILURE TO NOTIFY THE OFFICE OF A FOREIGN OR
INTERNATIONAL FILING (37 CFR 1.137(f))**

Docket Number (Optional)

3771P003

First Named Inventor: Daniel E. Grupp

Application No.: 10/217,758

Art Unit: 2811

Filed: August 12, 2002

Examiner:

Title: Method For Depinning The Fermi Level of a Semiconductor at an Electrical Junction and
Devices Incorporating Such Junctions

Attention: Office of Petitions

Mail Stop Petition

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

FAX: (703) 308-6916

NOTE: If information or assistance is needed in completing this form, please contact Petitions Information at
(703) 305-9283

The above-identified application became abandoned pursuant to 35 U.S.C. 122(b)(2)(B)(iii) for failure to timely notify
the Office of the filing of an application in a foreign country or under a multinational international treaty that requires
publication of applications eighteen months after filing. The date of abandonment is the day after the expiration date
of the forty-five (45) day period set in 35 U.S.C. 122(b)(2)(B)(iii).

PURSUANT TO 37 CFR 1.137(f), APPLICANT HEREBY PETITIONS FOR REVIVAL OF THIS APPLICATION
UNDER 37 CFR 1.137(b)

1. Petition fee

☒ Small entity-fee \$665.00 (37 CFR 1.17(m)). Applicant claims small entity status. See 37 CFR 1.27.

☐ Other than small entity - fee \$_____ (37 CFR 1.17(m)).

2. Notice of Foreign or International Filing (35 U.S.C. 122(b)(2)(B)(iii) and 37 CFR 1.213(c))

Subsequent to the filing of the above-identified application, an application was filed in another country, or under a
multinational international treaty (e.g., filed under the Patent Cooperation Treaty), that requires publication of applications
eighteen months after filing. The filing date of the subsequently filed foreign or international application is August 8,
2003.

SEND TO: Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
Based on Form PTO/SB/64a (05-03) as modified by BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP on 5/13/03.

[Page 1 of 2]

STATEMENT: The entire delay in filing the required notice of a foreign or international filing from the due date for the required notice until the filing of a grantable petition under 37 CFR 1.137(b) was unintentional.

[NOTE: The United States Patent and Trademark Office may require additional information if there is a question as to whether either the abandonment or the delay in filing a petition under 37 CFR 1.137(b) was unintentional (MPEP 711.03(c), subsections (III)(C) and (D))].

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2039.

October 14, 2003

Date

Telephone

Number: (408) 947-8200



Signature

Tarek N. Fahmi, Reg. No. 41,402

Typed or printed name & Registration No.

Blakely, Sokoloff, Taylor & Zafman LLP
12400 Wilshire Boulevard, 7th Floor
Los Angeles, CA 90025

Enclosures: ☒ Fee Payment

☐ Additional sheets containing statements establishing unintentional delay

☐ Other:

CERTIFICATE OF MAILING OR TRANSMISSION [37 CFR 1.8(a)]

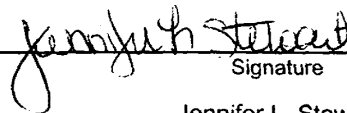
I hereby certify that this correspondence is being:

☒ deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313.1450.

☐ transmitted by facsimile on the date shown below to the United States Patent and Trademark Office at (703) 308-6916.

October 14, 2003

Date



Signature

Jennifer L. Stewart

Typed or printed name of person signing certificate



FEE TRANSMITTAL for FY 2003 Effective 01/01/2003. Patent fees are subject to annual revision.		Complete if Known	
☒ Applicant claims small entity status. See 37 CFR 1.27.		Application Number	10/217,758
TOTAL AMOUNT OF PAYMENT (\$)		Filing Date	August 12, 2002
665.00		First Named Inventor	Daniel E. Grupp
		Examiner Name	
		Group/Art Unit	2811
		Attorney Docket No.	3771P003

METHOD OF PAYMENT (check all that apply)		FEE CALCULATION (continued)																																																																																																																																																																																															
☒ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None ☒ Deposit Account		3. ADDITIONAL FEES																																																																																																																																																																																															
Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP																																																																																																																																																																																																	
The Commissioner is authorized to: (check all that apply) ☒ Charge fee(s) indicated below ☒ Credit any overpayments ☒ Charge any additional fee(s) required under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20 ☐ Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account																																																																																																																																																																																																	
1. BASIC FILING FEE																																																																																																																																																																																																	
<table border="1"><thead><tr><th colspan="2">Large Entity</th><th colspan="2">Small Entity</th><th rowspan="2">Fee Description</th><th rowspan="2">Fee Paid</th></tr><tr><th>Fee Code</th><th>Fee (\$)</th><th>Fee Code</th><th>Fee (\$)</th></tr></thead><tbody><tr><td>1001</td><td>770</td><td>2001</td><td>385</td><td>Utility filing fee</td><td></td></tr><tr><td>1002</td><td>340</td><td>2002</td><td>170</td><td>Design filing fee</td><td></td></tr><tr><td>1003</td><td>530</td><td>2003</td><td>265</td><td>Plant filing fee</td><td></td></tr><tr><td>1004</td><td>770</td><td>2004</td><td>385</td><td>Reissue filing fee</td><td></td></tr><tr><td>1005</td><td>160</td><td>2005</td><td>80</td><td>Provisional filing fee</td><td></td></tr><tr><td colspan="4">SUBTOTAL (1)</td><td></td><td></td></tr></tbody></table>		Large Entity		Small Entity		Fee Description	Fee Paid	Fee Code	Fee (\$)	Fee Code	Fee (\$)	1001	770	2001	385	Utility filing fee		1002	340	2002	170	Design filing fee		1003	530	2003	265	Plant filing fee		1004	770	2004	385	Reissue filing fee		1005	160	2005	80	Provisional filing fee		SUBTOTAL (1)																																																																																																																																																							
Large Entity		Small Entity		Fee Description	Fee Paid																																																																																																																																																																																												
Fee Code	Fee (\$)	Fee Code	Fee (\$)																																																																																																																																																																																														
1001	770	2001	385	Utility filing fee																																																																																																																																																																																													
1002	340	2002	170	Design filing fee																																																																																																																																																																																													
1003	530	2003	265	Plant filing fee																																																																																																																																																																																													
1004	770	2004	385	Reissue filing fee																																																																																																																																																																																													
1005	160	2005	80	Provisional filing fee																																																																																																																																																																																													
SUBTOTAL (1)																																																																																																																																																																																																	
2. EXTRA CLAIM FEES																																																																																																																																																																																																	
Total Claims: 20* Independent Claims: 3 Multiple Dependent:																																																																																																																																																																																																	
<table border="1"><thead><tr><th colspan="2">Large Entity</th><th colspan="2">Small Entity</th><th rowspan="2">Fee Description</th><th rowspan="2">Fee Paid</th></tr><tr><th>Fee Code</th><th>Fee (\$)</th><th>Fee Code</th><th>Fee (\$)</th></tr></thead><tbody><tr><td>1202</td><td>18</td><td>2202</td><td>9</td><td>Claims in excess of 20</td><td></td></tr><tr><td>1201</td><td>86</td><td>2201</td><td>43</td><td>Independent claims in excess of 3</td><td></td></tr><tr><td>1203</td><td>290</td><td>2203</td><td>145</td><td>Multiple Dependent claim, if not paid</td><td></td></tr><tr><td>1204</td><td>86</td><td>2204</td><td>43</td><td>**Reissue independent claims over original patent</td><td></td></tr><tr><td>1205</td><td>18</td><td>2205</td><td>9</td><td>**Reissue claims in excess of 20 and over original patent</td><td></td></tr><tr><td colspan="4">SUBTOTAL (2)</td><td></td><td></td></tr></tbody></table>		Large Entity		Small Entity		Fee Description	Fee Paid	Fee Code	Fee (\$)	Fee Code	Fee (\$)	1202	18	2202	9	Claims in excess of 20		1201	86	2201	43	Independent claims in excess of 3		1203	290	2203	145	Multiple Dependent claim, if not paid		1204	86	2204	43	**Reissue independent claims over original patent		1205	18	2205	9	**Reissue claims in excess of 20 and over original patent		SUBTOTAL (2)																																																																																																																																																							
Large Entity		Small Entity		Fee Description	Fee Paid																																																																																																																																																																																												
Fee Code	Fee (\$)	Fee Code	Fee (\$)																																																																																																																																																																																														
1202	18	2202	9	Claims in excess of 20																																																																																																																																																																																													
1201	86	2201	43	Independent claims in excess of 3																																																																																																																																																																																													
1203	290	2203	145	Multiple Dependent claim, if not paid																																																																																																																																																																																													
1204	86	2204	43	**Reissue independent claims over original patent																																																																																																																																																																																													
1205	18	2205	9	**Reissue claims in excess of 20 and over original patent																																																																																																																																																																																													
SUBTOTAL (2)																																																																																																																																																																																																	
*or number previously paid, if greater, For Reissues, see below																																																																																																																																																																																																	
		3. ADDITIONAL FEES																																																																																																																																																																																															
		<table border="1"><thead><tr><th colspan="2">Large Entity</th><th colspan="2">Small Entity</th><th rowspan="2">Fee Description</th><th rowspan="2">Fee Paid</th></tr><tr><th>Fee Code</th><th>Fee (\$)</th><th>Fee Code</th><th>Fee (\$)</th></tr></thead><tbody><tr><td>1051</td><td>130</td><td>2051</td><td>65</td><td>Surcharge - late filing fee or oath</td><td></td></tr><tr><td>1052</td><td>50</td><td>2052</td><td>25</td><td>Surcharge - late provisional filing fee or cover sheet</td><td></td></tr><tr><td>2053</td><td>130</td><td>2053</td><td>130</td><td>Non-English specification</td><td></td></tr><tr><td>1812</td><td>2,520</td><td>1812</td><td>2,520</td><td>For filing a request for <i>ex parte</i> reexamination</td><td></td></tr><tr><td>1804</td><td>920*</td><td>1804</td><td>920*</td><td>Requesting publication of SIR prior to Examiner action</td><td></td></tr><tr><td>1805</td><td>1,840*</td><td>1805</td><td>1,840*</td><td>Requesting publication of SIR after Examiner action</td><td></td></tr><tr><td>1251</td><td>110</td><td>2251</td><td>55</td><td>Extension for reply within first month</td><td></td></tr><tr><td>1252</td><td>420</td><td>2252</td><td>210</td><td>Extension for reply within second month</td><td></td></tr><tr><td>1253</td><td>950</td><td>2253</td><td>475</td><td>Extension for reply within third month</td><td></td></tr><tr><td>1254</td><td>1,480</td><td>2254</td><td>740</td><td>Extension for reply within fourth month</td><td></td></tr><tr><td>1255</td><td>1,210</td><td>2255</td><td>605</td><td>Extension for reply within fifth month</td><td></td></tr><tr><td>1404</td><td>330</td><td>2401</td><td>165</td><td>Notice of Appeal</td><td></td></tr><tr><td>1402</td><td>330</td><td>2402</td><td>165</td><td>Filing a brief in support of an appeal</td><td></td></tr><tr><td>1403</td><td>290</td><td>2403</td><td>145</td><td>Request for oral hearing</td><td></td></tr><tr><td>1451</td><td>1,510</td><td>2451</td><td>1,510</td><td>Petition to institute a public use proceeding</td><td></td></tr><tr><td>1452</td><td>110</td><td>2452</td><td>55</td><td>Petition to revive - unavoidable</td><td></td></tr><tr><td>1453</td><td>1,330</td><td>2453</td><td>665</td><td>Petition to revive - unintentional</td><td>665.00</td></tr><tr><td>1501</td><td>1,330</td><td>2501</td><td>665</td><td>Utility issue fee (or reissue)</td><td></td></tr><tr><td>1502</td><td>480</td><td>2502</td><td>240</td><td>Design issue fee</td><td></td></tr><tr><td>1503</td><td>640</td><td>2503</td><td>320</td><td>Plant issue fee</td><td></td></tr><tr><td>1460</td><td>130</td><td>2460</td><td>130</td><td>Petitions to the Commissioner</td><td></td></tr><tr><td>1807</td><td>50</td><td>1807</td><td>50</td><td>Processing fee under 37 CFR 1.17(q)</td><td></td></tr><tr><td>1806</td><td>180</td><td>1806</td><td>180</td><td>Submission of Information Disclosure Stmt</td><td></td></tr><tr><td>8021</td><td>40</td><td>8021</td><td>40</td><td>Recording each patent assignment per property (times number of properties)</td><td></td></tr><tr><td>1809</td><td>770</td><td>1809</td><td>385</td><td>Filing a submission after final rejection (37 CFR § 1.129(a))</td><td></td></tr><tr><td>1810</td><td>770</td><td>2810</td><td>385</td><td>For each additional invention to be examined (37 CFR § 1.129(b))</td><td></td></tr><tr><td>1801</td><td>770</td><td>2801</td><td>385</td><td>Request for Continued Examination (RCE)</td><td></td></tr><tr><td>1802</td><td>900</td><td>1802</td><td>900</td><td>Request for expedited examination of a design application</td><td></td></tr><tr><td colspan="4">Other fee (specify)</td><td></td><td></td></tr><tr><td colspan="4"></td><td>SUBTOTAL (3)</td><td>665.00</td></tr></tbody></table>		Large Entity		Small Entity		Fee Description	Fee Paid	Fee Code	Fee (\$)	Fee Code	Fee (\$)	1051	130	2051	65	Surcharge - late filing fee or oath		1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet		2053	130	2053	130	Non-English specification		1812	2,520	1812	2,520	For filing a request for <i>ex parte</i> reexamination		1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action		1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action		1251	110	2251	55	Extension for reply within first month		1252	420	2252	210	Extension for reply within second month		1253	950	2253	475	Extension for reply within third month		1254	1,480	2254	740	Extension for reply within fourth month		1255	1,210	2255	605	Extension for reply within fifth month		1404	330	2401	165	Notice of Appeal		1402	330	2402	165	Filing a brief in support of an appeal		1403	290	2403	145	Request for oral hearing		1451	1,510	2451	1,510	Petition to institute a public use proceeding		1452	110	2452	55	Petition to revive - unavoidable		1453	1,330	2453	665	Petition to revive - unintentional	665.00	1501	1,330	2501	665	Utility issue fee (or reissue)		1502	480	2502	240	Design issue fee		1503	640	2503	320	Plant issue fee		1460	130	2460	130	Petitions to the Commissioner		1807	50	1807	50	Processing fee under 37 CFR 1.17(q)		1806	180	1806	180	Submission of Information Disclosure Stmt		8021	40	8021	40	Recording each patent assignment per property (times number of properties)		1809	770	1809	385	Filing a submission after final rejection (37 CFR § 1.129(a))		1810	770	2810	385	For each additional invention to be examined (37 CFR § 1.129(b))		1801	770	2801	385	Request for Continued Examination (RCE)		1802	900	1802	900	Request for expedited examination of a design application		Other fee (specify)										SUBTOTAL (3)	665.00
Large Entity		Small Entity		Fee Description	Fee Paid																																																																																																																																																																																												
Fee Code	Fee (\$)	Fee Code	Fee (\$)																																																																																																																																																																																														
1051	130	2051	65	Surcharge - late filing fee or oath																																																																																																																																																																																													
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet																																																																																																																																																																																													
2053	130	2053	130	Non-English specification																																																																																																																																																																																													
1812	2,520	1812	2,520	For filing a request for <i>ex parte</i> reexamination																																																																																																																																																																																													
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action																																																																																																																																																																																													
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action																																																																																																																																																																																													
1251	110	2251	55	Extension for reply within first month																																																																																																																																																																																													
1252	420	2252	210	Extension for reply within second month																																																																																																																																																																																													
1253	950	2253	475	Extension for reply within third month																																																																																																																																																																																													
1254	1,480	2254	740	Extension for reply within fourth month																																																																																																																																																																																													
1255	1,210	2255	605	Extension for reply within fifth month																																																																																																																																																																																													
1404	330	2401	165	Notice of Appeal																																																																																																																																																																																													
1402	330	2402	165	Filing a brief in support of an appeal																																																																																																																																																																																													
1403	290	2403	145	Request for oral hearing																																																																																																																																																																																													
1451	1,510	2451	1,510	Petition to institute a public use proceeding																																																																																																																																																																																													
1452	110	2452	55	Petition to revive - unavoidable																																																																																																																																																																																													
1453	1,330	2453	665	Petition to revive - unintentional	665.00																																																																																																																																																																																												
1501	1,330	2501	665	Utility issue fee (or reissue)																																																																																																																																																																																													
1502	480	2502	240	Design issue fee																																																																																																																																																																																													
1503	640	2503	320	Plant issue fee																																																																																																																																																																																													
1460	130	2460	130	Petitions to the Commissioner																																																																																																																																																																																													
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)																																																																																																																																																																																													
1806	180	1806	180	Submission of Information Disclosure Stmt																																																																																																																																																																																													
8021	40	8021	40	Recording each patent assignment per property (times number of properties)																																																																																																																																																																																													
1809	770	1809	385	Filing a submission after final rejection (37 CFR § 1.129(a))																																																																																																																																																																																													
1810	770	2810	385	For each additional invention to be examined (37 CFR § 1.129(b))																																																																																																																																																																																													
1801	770	2801	385	Request for Continued Examination (RCE)																																																																																																																																																																																													
1802	900	1802	900	Request for expedited examination of a design application																																																																																																																																																																																													
Other fee (specify)																																																																																																																																																																																																	
				SUBTOTAL (3)	665.00																																																																																																																																																																																												

SUBMITTED BY		Complete (if applicable)	
Name (Print/Type)	Tarek N. Fahim	Registration No. (Attorney/Agent)	41,402
Signature		Telephone	(408) 947-8200
		Date	10/14/03

Based on PTO/SB/17 (08-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 08/11/2003.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450



OCT 24 2003

OCT 24 2003

D ACKS

TRANSMITTAL FORM (to be used for all correspondence after initial filing)		Application No.	10/217,758
		Filing Date	August 12, 2002
		First Named Inventor	Daniel E. Grupp
		Art Unit	2811
		Examiner Name	
Total Number of Pages in This Submission	3	Attorney Docket Number	3771P003

ENCLOSURES (check all that apply)		
☒ Fee Transmittal Form ☒ Fee Attached ☐ Amendment / Response ☐ After Final ☐ Affidavits/declaration(s) ☐ Extension of Time Request ☐ Express Abandonment Request ☐ Information Disclosure Statement ☐ PTO/SB/08 ☐ Certified Copy of Priority Document(s) ☐ Response to Missing Parts/Incomplete Application ☐ Basic Filing Fee ☐ Declaration/POA ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53	☐ Drawing(s) ☐ Licensing-related Papers ☒ Petition ☐ Petition to Convert a Provisional Application ☐ Power of Attorney, Revocation Change of Correspondence Address ☐ Terminal Disclaimer ☐ Request for Refund ☐ CD, Number of CD(s)	☐ After Allowance Communication to Group ☐ Appeal Communication to Board of Appeals and Interferences ☐ Appeal Communication to Group (Appeal Notice, Brief, Reply Brief) ☐ Proprietary Information ☐ Status Letter ☐ Other Enclosure(s) (please identify below):
Remarks		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual name	Tarek N. Fahmi, Reg. No. 41,402 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	October 14, 2003

CERTIFICATE OF MAILING/TRANSMISSION			
I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.			
Typed or printed name	Jennifer L. Stewart		
Signature		Date	October 14, 2003

Based on PTO/SB/21 (08-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wir) 09/11/2003.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P. O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD, SEVENTH FLOOR
LOS ANGELES, CA 90025

COPY MAILED

NOV 03 2003

OFFICE OF PETITIONS

In re Application of	:
Daniel E. Grupp et al	: DECISION GRANTING PETITION
Application No. 10/217,758	: UNDER 37 CFR 1.137(b)
Filed: August 12, 2002	:
Attorney Docket No. 3771P003	:

This is a decision on the petition, filed October 17, 2003, which is being treated as a petition under 37 CFR 1.137(b) to revive the instant nonprovisional application for failure to timely notify the U.S. Patent and Trademark Office (USPTO) of the filing of an application in a foreign country, or under a multinational treaty that requires publication of applications eighteen months after filing. See 37 CFR 1.137(f).

The petition under 37 CFR 1.137(f) is GRANTED.

Petitioner states that the instant nonprovisional application is the subject of an application filed in an eighteen month publication country on August 8, 2003. However, the USPTO was unintentionally not notified of this filing within 45 days subsequent to the filing of the subject application in an eighteen month publication country.

In view of the above, this application became abandoned pursuant to 35 U.S.C. § 122(b)(2)(B)(iii) and 37 CFR 1.213(c) for failure to timely notify the USPTO of the filing of an application in a foreign country, or under a multilateral international agreement, that requires publication of applications 18 months after filing.

A petition to revive an application abandoned pursuant to 35 U.S.C. 122(b)(2)(B)(iii) for failure to notify the USPTO of a foreign filing must be accompanied by:

- (1) the required reply which is met by the notification of such filing in a foreign country or under a multinational treaty;
- (2) the petition fee as set forth in 37 CFR 1.17(m);
- and
- (3) a statement that the entire delay in filing the

required reply from the due date of the reply until the filing of a grantable petition was unintentional.

The instant petition has been found to be in compliance with 37 CFR 1.137(b). Accordingly, the failure to timely notify the USPTO of a foreign or international filing within 45 days after the date of filing of such foreign or international application as provided by 35 U.S.C. § 122(b)(2)(B)(iii) and 37 CFR 1.213(c) is accepted as having been unintentionally delayed.

The previous Request and Certification under 35 U.S.C. § 122(b)(2)(B)(i) has been rescinded. A Notice Regarding Rescission of Nonpublication Request which sets forth the projected publication date of February 12, 2004 accompanies this decision on petition.

A Notice of Allowability and a Notice of Allowance and Fee(s) Due were mailed in this case on October 7, 2003. However, in view of the nonpublication request filed with the application, the Notice of Allowance and Fee(s) Due mailed in this case did not require the submission of a publication fee. Therefore, in view of the rescinding of the nonpublication request, the \$300 publication fee will be charged to petitioner's deposit account. If publication of the application does not occur, applicant may file a request for refund after the patent issues. See 37 CFR 1.211(e). Questions relating to a refund of the publication fee should be directed to the patent publication hotline at (703) 605-4283 or by e-mail to pppub@uspto.gov.

This application is being forwarded to Publishing Division to await a reply to the Notice of Allowance and Fee(s) Due mailed October 7, 2003.

Any inquiries concerning this decision may be directed to the undersigned at (703) 305-8680.



Frances Hicks
Petitions Examiner
Office of Petitions
Office of the Deputy Commissioner
for Patent Examination Policy

ATTACHMENT: Notice Regarding Rescission of Nonpublication Request



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
10/217,758	08/12/2002	Daniel E. Grupp	3771P003

CONFIRMATION NO. 1710

08791
 BLAKELY SOKOLOFF TAYLOR & ZAFMAN
 12400 WILSHIRE BOULEVARD, SEVENTH FLOOR
 LOS ANGELES, CA 90025

OC000000011159811

Date Mailed: 11/03/2003

Communication Regarding Rescission Of Nonpublication Request and/or Notice of Foreign Filing

Applicant's rescission of the previously-filed nonpublication request and/or notice of foreign filing is acknowledged. The paper has been reflected in the Patent and Trademark Office's (USPTO's) computer records so that the earliest possible projected publication date can be assigned.

The projected publication date is 02/12/2004.

If applicant rescinded the nonpublication request before or on the date of "foreign filing,"¹ then no notice of foreign filing is required.

If applicant foreign filed the application after filing the above application and before filing the rescission, and the rescission did not also include a notice of foreign filing, then a notice of foreign filing (not merely a rescission) is required to be filed within 45 days of the date of foreign filing. See 35 U.S.C. § 122(b)(2)(B)(iii), and Clarification of the United States Patent and Trademark Office's Interpretation of the Provisions of 35 U.S.C. § 122(b)(2)(B)(ii)-(iv), 1272 Off. Gaz. Pat. Office 22 (July 1, 2003).

If a notice of foreign filing is required and is not filed within 45 days of the date of foreign filing, then the application becomes abandoned pursuant to 35 U.S.C. § 122(b)(2)(B)(iii). In this situation, applicant should either file a petition to revive or notify the Office that the application is abandoned. See 37 CFR 1.137(f). Any such petition to revive will be forwarded to the Office of Petitions for a decision. Note that the filing of the petition will not operate to stay any period of reply that may be running against the application.

Questions regarding petitions to revive should be directed to the Office of Petitions at (703) 305-9282. Questions regarding publications of patent applications should be directed to the patent application publication hotline at (703) 605-4283 or by e-mail pgpub@uspto.gov.

¹ Note, for purpose of this notice, that "foreign filing" means "filing an application directed to the same invention in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing".

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (703) 746-4000

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

08791 7590 10/07/2003

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD, SEVENTH FLOOR
LOS ANGELES, CA 90025

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO, on the date indicated below.

Patricia A. Balero (Depositor's name)
(Signature)
January 7, 2004 (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/217,758	08/12/2002	Daniel E. Grupp	3771P003	1710

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$0	\$1330	01/07/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGO, NGAN V	2814	257-030000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

BLAKELY SOKOLOFF
TAYLOR & ZAFMAN LLP

2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

ACORN TECHNOLOGIES, INC.

(B) RESIDENCE: (CITY AND STATE OR COUNTRY)

PACIFIC PALISADES, CA

Please check the appropriate assignee category or categories (will not be printed on the patent); ☐ individual ☒ corporation or other private group entity ☐ government

4a. The following fee(s) are enclosed:

- ☒ Issue Fee
☐ Publication Fee
☒ Advance Order - # of Copies 10

4b. Payment of Fee(s):

- ☒ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 02-2666 (enclose an extra copy of this form).

Director for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature)

(Date)

Tarek N. Fahmi - Reg. No.: 41,402 January 7, 2004

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

01/14/2004 JADD02 00000002 10217758

01 FC:1501
02 FC:80011330.00 OP
30.00 OP

TRANSMIT THIS FORM WITH FEE(S)



DOCKET NO.: 3771P003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

DANIEL E. GRUPP, ET AL.

Application No.: 10/217,758

Filed: August 12, 2002

For: **Method For Depinning The Fermi Level of a Semiconductor at an Electrical Junction and Devices Incorporating Such Junctions**

Art Group: 2814

Examiner: Ngo, Ngan V.

Date of mailing of PTOL 85 entitled
"Notice of Allowance and Base Issue Fee
Due" October 07, 2003

Confirmation No. 1710

Mail Stop ISSUE FEE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF FORMAL DRAWINGS

Sir:

Enclosed herewith for filing in the above-identified U.S. Patent Application are the formal drawings, 6 sheets including 11 Figures. The three month period of response set in the Notice of Allowability (PTOL 37) expires on January 7, 2004. This submission is on or before this expiration date. Please charge any additional extension or petition fees under 37 C.F.R. §1.17 or credit for any overpayment to our Deposit Account No. 02-2666. A duplicate copy of the Fee Transmittal sheet is enclosed.

Respectfully submitted,

Blakely, Sokoloff, Taylor & Zafman LLP

Dated: January 7, 2004

Tarek N. Fahmi, Reg. No. 41,402

12400 Wilshire Boulevard, 7th Floor
Los Angeles, CA 90025
Telephone: (408) 947-8200

CERTIFICATE OF MAILING/TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Patricia A. Balero

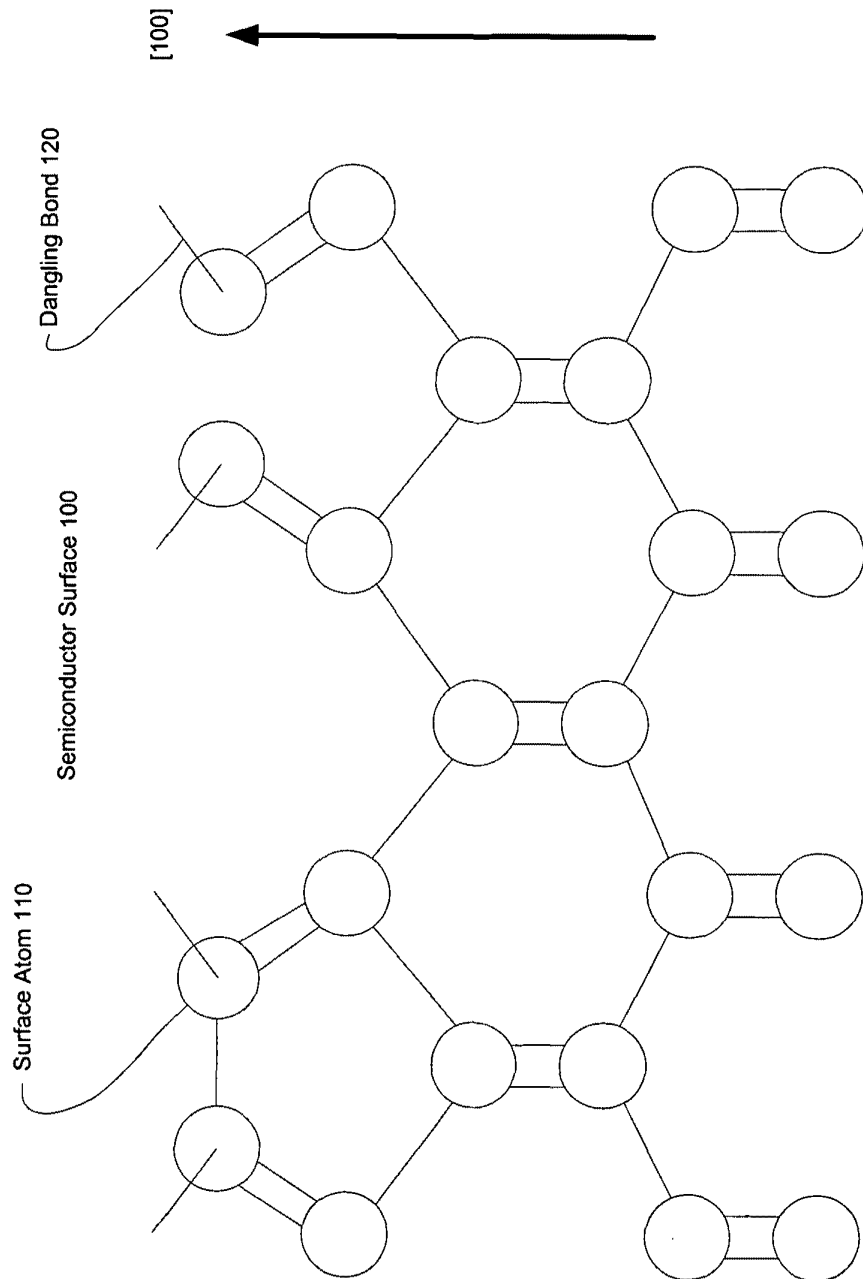
01/07/04

Date



Blakely, Sokoloff, Taylor & Zafman LLP (408) 947-8200
Title: Method For Depinning The Fermi Level of a Semiconductor at an
Electrical Junction and Devices Incorporating Such Junctions
1st Named Inventor: Daniel E. Grupp
Application No.: 10/217,758 Docket No.: 3771P003
Sheet: 1 of 6

Fig. 1





Energy Scales for Metal - Semiconductor Junctions

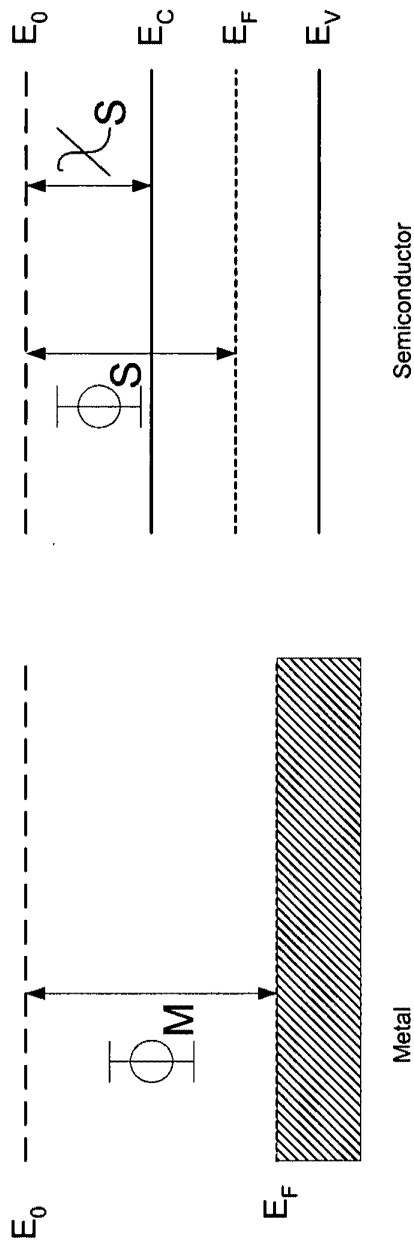


Fig. 2



Fig. 3
(Prior Art)

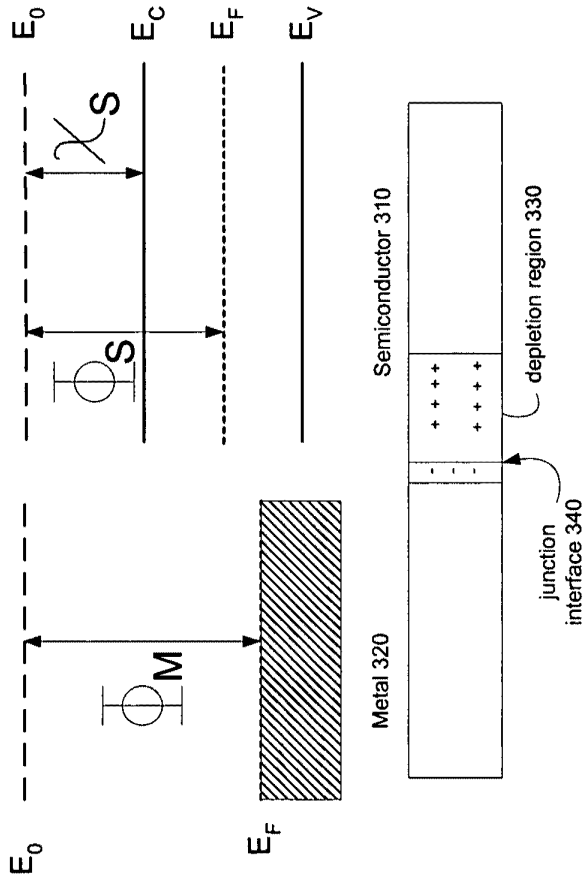
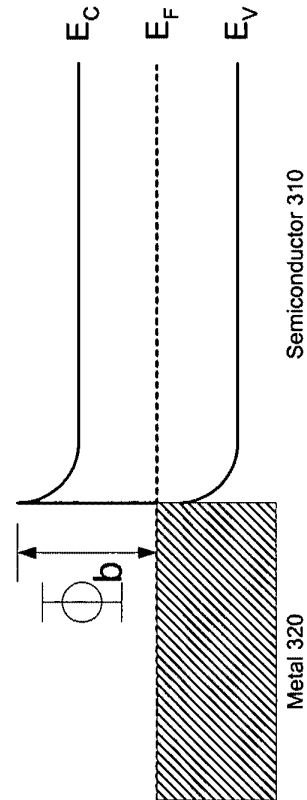


Fig. 4
(Prior Art)





Blakely, Sokoloff, Taylor & Zafman LLP (408) 947-8200
Title: Method For Depinning The Fermi Level of a Semiconductor at
an Electrical Junction and Devices Incorporating Such Junctions
1st Named Inventor: Daniel E. Grupp
Application No.: 10/217,758 Docket No.: 3771P003
Sheet: 4 of 6

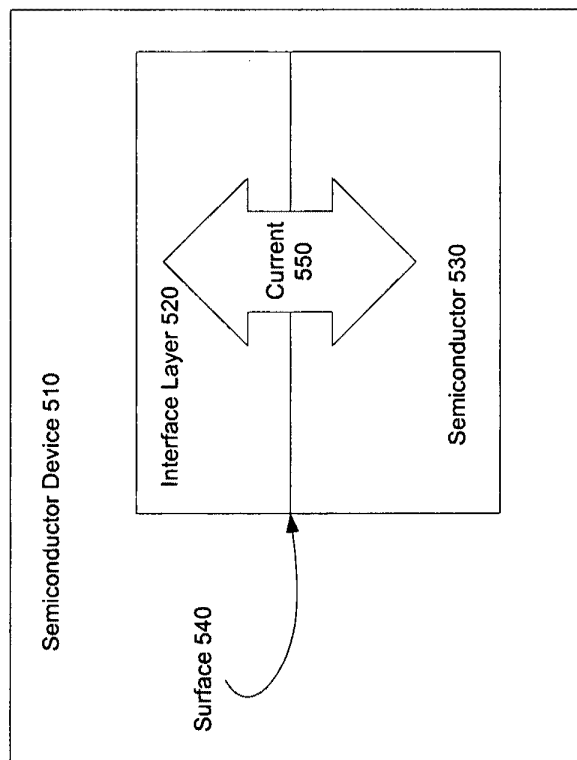


Fig. 5

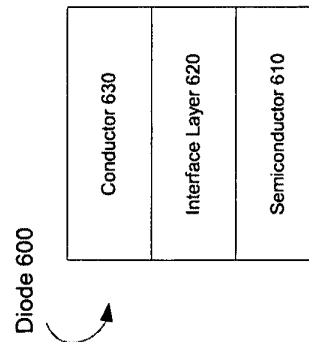
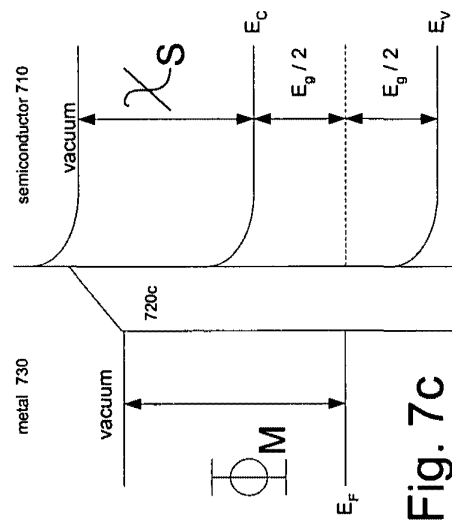
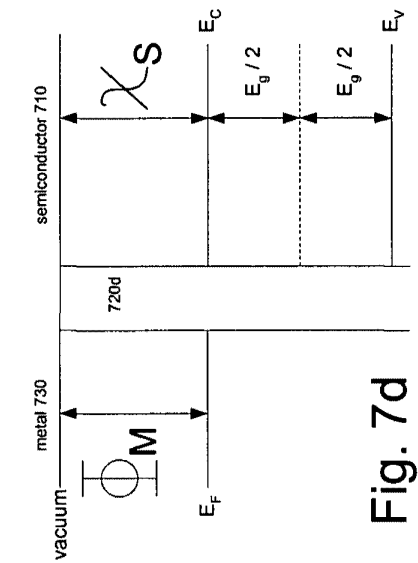
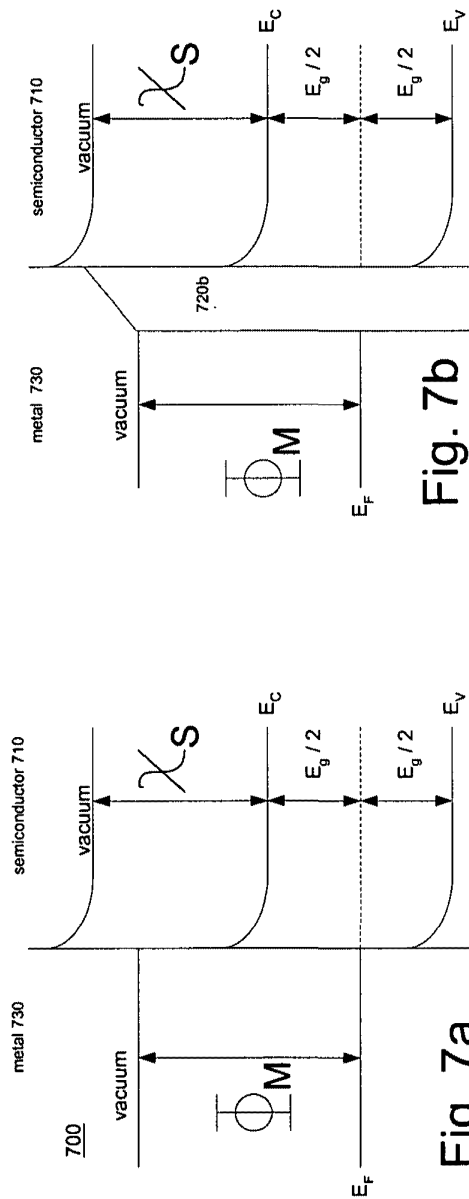


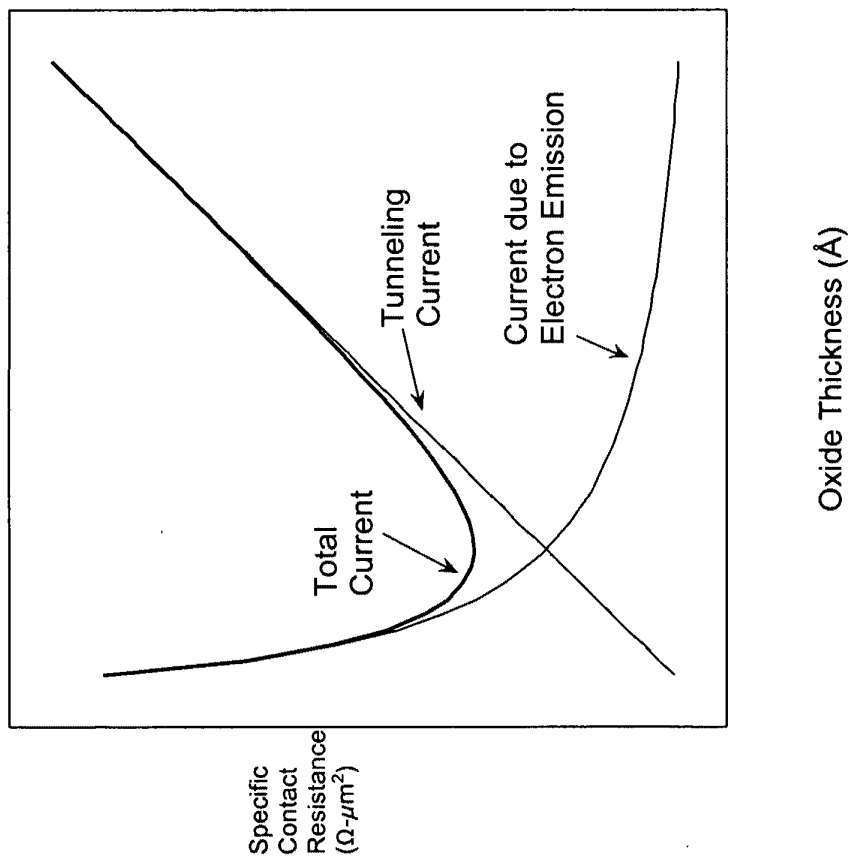
Fig. 6





Blakely, Sokoloff, Taylor & Zafman LLP (408) 947-8200
Title: Method For Depinning The Fermi Level of a Semiconductor at
an Electrical Junction and Devices Incorporating Such Junctions
1st Named Inventor: Daniel E. Grupp
Application No.: 10/217,758 Docket No.: 3771P003
Sheet: 6 of 6

Fig. 8





image

Office petition
DAC

**REQUEST
FOR
CONTINUED EXAMINATION (RCE)
TRANSMITTAL**

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. 1450
Alexandria, VA 22313-1450

Application No.	10/217,758
Filing Date	August 12, 2002
First Named Inventor	Daniel E. Grupp
Art Unit	2814
Examiner Name	Ngo, Ngan V.
Attorney Docket Number	3771P003

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR § 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. **Submission required under 37 C.F.R. § 1.114**

- a. ☐ Previously submitted
- i. ☐ Consider the amendment(s)/reply under 37 C.F.R. § 1.116 previously filed on
(Any unentered amendment(s) referred to above will be entered).
- ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on
- iii. ☐ Other _____
- b. ☒ Enclosed
- i. ☐ Amendment/Reply
- ii. ☐ Affidavit(s)/Declaration(s)
- iii. ☒ Information Disclosure Statement (IDS)
- iv. ☒ Other Petition to Withdrawal from Issue

2. **Miscellaneous**

- a. ☐ Suspension of action on the above-identified application is requested under 37 C.F.R. § 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 C.F.R. § 1.17(i) required)
- b. ☐ Other _____

3. **Fees** The RCE fee under 37 C.F.R. § 1.17(e) is required by 37 C.F.R. § 1.114 when the RCE is filed.

- a. ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 02-2666.
- i. ☒ RCE fee required under 37 C.F.R. § 1.17(e) and any additional claims fee(s)
- ii. ☐ Extension of time fee (37 C.F.R. § 1.136 and 1.17)
- iii. ☒ Other: Petition For Withdrawal from Issue (\$130.00)
- b. ☒ Check in the amount of \$515.00 enclosed
- c. ☐ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print/Type)	Tarek N. Fahmi	Registration No. (Attorney/Agent)	41,402
Signature		Date	January 21, 2004

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

January 21, 2004

Name (Print/Type)	Patricia A. Balero	Date	January 21, 2004
Signature			

Based on PTO/SB/30 (08-03) as modified by Blakely, Solokoff, Taylor & Zafman (wlr) 09/11/2003.
SEND TO: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

01/28/2004 CNGUYEN 00000077 10217758

01 FC:2801

385.00 OP



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No. : 10/217,758 Confirmation No. 1710
Applicant : Daniel E. Grupp
Filed : August 12, 2002
TC/A.U. : 2814
Examiner : Ngo, Ngan V.

Docket No. : 3771P003
Customer No. : 08791

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450.

PETITION FOR WITHDRAWAL FROM ISSUE - ISSUE FEE PAID (37 C.F.R. 1.313(c))

Sir:

PETITION

1. Applicant hereby petitions for the withdrawal of this application from issue.

PATENT ISSUE FEE

2. The issue fee for this case was paid on January 7, 2004

REASON(S) FOR WITHDRAWAL REQUEST

3. The reason for the request for withdrawal from issue is:
☒ Consideration of a request for continued examination in compliance with 1.114.

INFORMATION DISCLOSURE STATEMENT

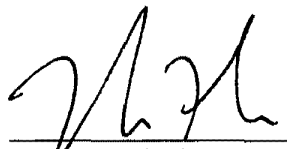
4. ☒ Accompanying this petition is an information disclosure statement.

PETITION FEES

5. The petition fee is paid as follows:
☒ Enclosed is a check in the sum of \$130.00
☒ Please charge any fees due to Deposit Account 02-2666. A duplicate of this petition is attached.

Date: Jan 21, 2004

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 947.8200



Tarek N. Fahmi
Reg. No. 41,402

01/20/2004 CNGUYEN 00000077 10217758

02 FC:1460

130.00 OP

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 on: January 21, 2004
Date of Deposit

Patricia A. Balero
Name of Person Mailing Correspondence

Signature

1/21/04

Date



Docket No.: 3771P003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

DANIEL E. GRUPP, ET AL.

Application No.: 10/217,758

Filed: August 12, 2002

For: **Method For Depinning The Fermi Level of
a Semiconductor at an Electrical Junction
and Devices Incorporating Such Junctions**

Art Group: 2814

Examiner: Ngo, Ngan V.

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure, enclosed is a copy of Information Disclosure Statement by Applicant (form PTO/SB/08), which is being submitted concurrently with the Request for Continued Examination. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s). Copies of the references cited on PTO/SB/08 are enclosed herewith.

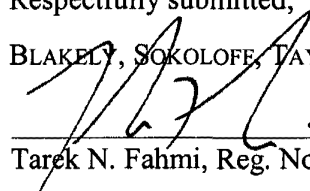
The references were cited in a Search Report dated December 3, 2003 (copy enclosed herewith) in a counterpart PCT application.

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP



Tarek N. Fahmi, Reg. No. 41,402

Date: January 21, 2004

12400 Wilshire Boulevard, 7th Floor
Los Angeles, CA 90025
Telephone: (408) 947-8200



Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	10/217,758
				Filing Date	August 12, 2002
				First Named Inventor	Daniel E. Grupp
				Art Unit	2814
				Examiner Name	Ngo, Ngan V.
Sheet	2	of	2	Attorney Docket Number	3771P003

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.†	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
		International Search Report, (Decemeber 3, 2003), pp. 8	
		M. A. SOBOLEWSKI, et al., "Properties of Ultrathin Thermal Nitrides In Silicon Schottky Barrier Structures", Applied Physics Letters, American Institute of Physics, Vol. 54, No. 7, (2/13/89), pp. 638-640	
		T. TERAJI, et al., "Ohmic Contacts To N. Type 6H.SIC Without Post-Annealing", Materials Research Society Symposium Proceeding, (4/8/96), pp. 149-154	
		S. M. SZE, "Metal-Semiconductor Contacts", Physics of Semiconductor Devices, John Wiley & Sons, 1981, pp. 245-311	
		L. M. PORTER, "A Critical Review of Ohmic and Rectifying Contacts For Silicon Carbide", Materials Science and Engineering, Vol. 34, No. 2 (11/1/95), pp. 83-105	

Examiner Signature		Date Considered	
-----------------------	--	--------------------	--

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

†Applicant's unique citation designation number. ‡Applicant is to place a check mark here if English language Translation is attached.

Based on PTO/SB/08B (08-03) as modified by Blakely, Solokoff, Taylor & Zafman (wlr) 08/11/2003.
Send To: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

(19)



Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number:

**0 295 490
A1**

(12)

EUROPEAN PATENT APPLICATION

(21) Application number: 88108684.7

(51) Int. Cl. 4: **H01L 21/314 , H01L 29/40 ,
H01L 21/285**

(22) Date of filing: 31.05.88

(30) Priority: 18.06.87 US 64414

(43) Date of publication of application:
21.12.88 Bulletin 88/51

(84) Designated Contracting States:
DE FR GB

(71) Applicant: **International Business Machines
Corporation**
Old Orchard Road
Armonk, N.Y. 10504(US)

(72) Inventor: **Fowler, Alan B.**
3511 Kamhi Drive
Yorktown Heights New York 10598(US)
Inventor: **Freeouf, John L.**
East Mountain, Lake Katonah, Route 3
Katonah New York 10536(US)
Inventor: **Kirchner, Peter D.**
RR1, Box 156A
Putnam Valley New York 10579(US)
Inventor: **Warren, Alan C.**
150 Overlook Avenue, Apt. 7A
Peekskill New York 10566(US)
Inventor: **Woodall, Jerry M.**
336 Cherry Street
Katonah New York 10507(US)

(74) Representative: **Kreidler, Eva-Maria, Dr. rer.
nat.**
IBM Deutschland GmbH Patentwesen und
Urheberrecht Schönaicher Strasse 220
D-7030 Böblingen(DE)

(54) Compound semiconductor surface termination.

EP 0 295 490 A1

(57) A surface termination of a compound semiconductor is provided wherein conditions are provided for a pristine surface to be retained in an unpinned condition and a surface layer of a non-metallic material is provided. A GaAs substrate is heated in an oxygen-free atmosphere at high temperature with hydrogen sulfide, producing a pristine surface with a coating of gallium sulfide covered with a 1,000 nanometer covering of low temperature plasma enhanced chemical vapor deposited silicon dioxide.

COMPOUND SEMICONDUCTOR SURFACE TERMINATION

The invention relates to semiconductor devices fabricated of compound semiconductor materials and to the surfaces of those semiconductor materials that influence the fabrication of devices.

The design and operation of compound semiconductor devices are influenced by a number of factors, a principal one being the properties of the exposed semiconductor surface and of interfaces between the semiconductor crystal and metals or insulators.

In such compound semiconductor devices, on the surface of the semiconductor crystal, the Fermi level is pinned at some characteristic energy and this produces the undesirable effect of both carrier recombination at the surface and an inherent barrier. The development of a number of otherwise possible and useful devices and device structures have been prevented by these conditions and a more nearly ideal interface, that is one whose Fermi level may be moved freely and has low recombination velocity is required.

There has been effort directed to the problem. The effort usually is called passivation and the result is the providing of a covering member over the compound semiconductor crystal surface.

The work in the art indicates responsiveness to the presence of the element sulfur.

In U.S. Patent 4,354,198, it is taught that on a Group III-V compound semiconductor, such as GaAs, a Group II-VI semiconductor operates to passivate the surface, with the preferred Group II-VI compound being ZnS.

Further work indicates a need for care in the field. In an article in the Journal of Vacuum Science & Technology, Volume 17, No. 5, p.1134, Sept/Oct. 1980, there is described the fact that exposure of GaAs to H₂S in vacuum unpins the Fermi level and that this effect persists after the adding of Al. In another article in the Journal of Vacuum Science & Technology, Vol. B3, No. 4, July/Aug. 1985, p.1197, studies and data indicate the fact that for GaAs, arsenic must be removed or the results become unpredictable. In yet another article, in the Journal of Vacuum Science and Technology, Vol. 19, 1981, p.794, it is shown that native oxides of Ga and As which form in the presence of O are associated with Fermi level pinning. Thus, O behaves in a detrimental way.

The use of sulfur compounds to passivate Group III-V compound semiconductors has been reported Applied Physics Letters, July 1987, wherein data is advanced that lithium sulfide, ammonium sulfide and sodium sulfide provide improvement in the GaAs surface recombination property.

The sulfur compound type further passivation work is reported in Applied Physics Letters, July 1987, describing the use of sodium sulfide in an aqueous solution applied at surface electrode locations to provide passivation.

FIG. 1 is a schematic view of a compound semiconductor crystal illustrating a surface with the elements of the invention.

FIG. 2 is an illustration of a band diagram of a tunneling type contact achievable with the invention.

FIG. 3 is an illustration of a variable barrier height contact achievable with the invention.

FIG. 4 is an illustration of passivation in a planar structure where a p-n junction is at the surface.

FIG. 5 is a schematic illustration of the application of the invention to a metal oxide semiconductor field effect transistor.

FIG. 6 is a schematic illustration of the application of the invention to the passivation of a bipolar transistor.

FIG. 7 is a schematic illustration of the application of the invention to the passivation of a light emitting device.

FIG. 8 is a schematic illustration of the application of the invention to the passivation of a semiconductor structure employing a small dimension, quantum wire type feature.

The invention provides a surface termination capability for a variety of compound semiconductor device structures in which there is recognized that there are several interdependent factors that are responsible and that useful termination properties include compatibility with the device being fabricated.

The invention structurally employs a very thin Fermi level pinning control layer of a material that unpins the Fermi level of the compound semiconductor material at the surface. This layer should be on the order of a monolayer in thickness. A monolayer layer of a material may be defined as one surface atom for each surface atom of the material on which it is positioned. The quantity needed for coverage is sensitive to crystallographic orientation. For compatibility with device fabricating the pinning control layer would preferably be thin enough not to attenuate light and permit tunneling for ohmic contact performance. A quantum mechanical tunneling thickness of the order of 2 nm would be satisfactory. The term pristine crystal surface refers to a damage-free uncontaminated crystal surface. The layer of unpinning material is covered with a second layer of a non-metallic material. The non-metallic material is selected for dielectric, ambient

reaction inertness and translucence properties.

The resulting compound semiconductor crystal with the surface termination structure of the invention can serve as an intermediate manufacturing product in the fabrication of compound semiconductor devices.

The factors influencing the surface problem may be viewed in the light of the following principles. In order to facilitate communication, the III-V compound GaAs has been selected for illustration although in the light of the principles involved, translation to other semiconductor materials will be readily apparent.

The first factor is that there exists at a compound semiconductor surface an agent responsible for moving the Fermi level away from the normal which is the position in the absence of any surface charge and producing the phenomenon in the art known as Fermi level pinning. In the case of GaAs, this agent appears to be an excess of one or more of the components of the compound semiconductor crystal. In view of this, surface termination for practical device purposes will require the removal of any such agent at that surface. The semiconductor surface is to be pristine.

A second factor is that the compound semiconductor surface will react with the ambient and become contaminated unless steps are taken by protecting with a coating of material that insures that the Fermi level remain in an unpinned condition both on the shelf and in conditions of use, such as in the presence of the materials at the device interface.

The third factor is that generally materials that will control the pinning condition must be able to be compatible with other functional purposes in device fabrication and there may be conditions of material properties and layer thickness incompatibility. In accordance with the invention where such conditions are encountered, a layer is applied to provide the required properties.

The resulting multilayer termination structure of the invention is capable of being employed in a variety of compound semiconductor device structures because the elimination of the Fermi level pinning condition enables the formation of ideal interfaces where barrier height to conduction is no longer constant but depends on the relative work functions of the materials. This in turn provides the ability to selectively form such interfaces as ohmic contacts, selectable barrier height rectifying contacts, and selectable threshold inversion channel carrier control in devices.

Referring to FIG. 1, on a compound semiconductor substrate 1, at a pristine surface 2, that is at a surface 2 where there is essentially no damage and essentially no extraneous material, there will be no pinning agent species, a layer of material

that retains the Fermi level in the normal position is applied. The layer for device fabrication and performance compatibility is a very thin, of the order of a monolayer in thickness layer of a material 3 for coverage and is preferably for tunneling purposes of less than tunneling thickness.

Over the layer 3, a layer 4 is provided. The layer 4 is selected to provide dielectric, ambient reaction inertness and translucence properties. It is non-metallic and may be a semiconductor or an insulator.

In accordance with the invention, the compound semiconductor may be a compound of Ga, Al or In with As or Sb or ternary and quaternary alloys thereof.

The layer 3 is a compound of a cation ingredient with respect to the compound semiconductor together with one of S, Se and Te. In a compound semiconductor, the element of the lower group of the periodic table is the cationic ingredient. For one example, a compound of Ga with S. For another example, the layer 3 can be a cation oxide such as Ga_2O_3 for a GaAs crystal, if the anion oxide which for GaAs would be As_2O_3 plus any excess anion such as As are removed before or during formation of the unpinning layer.

The layer 4 is non-metallic and may be such materials as low temperature plasma enhanced SiO_2 , CaF_2 , NaS, ZnS, GaP, GaSe and polyimides.

In the fabrication of the invention, the substrate 1 may be rendered pristine and free of the pinning producing species in, as examples, the following ways, using GaAs as the example:

- by heating the crystal with an arsenic coating at about 400 °C for about 10 seconds in vacuum. This procedure produces a surface reconstruction such that the surface unit cell is equivalent to the bulk unit cell and removes the cause of the Fermi level pinning;
- by treatment with zinc selenide in a beam that tends to strip the arsenic from the surface;
- by exposure to an ambient of hydrogen sulfide at high temperatures;
- by the etching of the surface with acids and bases; and
- by photo-washing under conditions where the crystal surface is subjected to water in the presence of light.

All of these operations provide a compound semiconductor crystal with pristine surface that does not have any of the pinning causing species thereon. Such a surface requires protection so that in accordance with the invention a very thin material that will retain the Fermi level in the free

position is applied. This material is a compound of the cation of the compound semiconductor crystal and is a member taken from the group of S, Se and Te, which for GaAs is gallium sulfide, gallium selenide and gallium telluride.

The application of the layer 4 may employ such techniques as exposing the crystal 1 in FIG. 1 with the layer 3 in place to an ambient of H_2S , to an evaporation of sodium sulfide, gallium sulfide or gallium selenide, and by the technique of photo-washing.

The technique of photo-washing is described in European patent application Serial No. 87 107 476.1. The surface produced by that technique may be used as the structure of Fig. 1 on which the layer 4 is to be applied.

The layer 4 is then applied in a thickness of up to approximately 1,000 nanometers.

The surface termination of the invention is useful in a variety of device structures.

Referring next to FIG. 2, there is shown a band energy diagram illustrating an interface suitable for ohmic contact performance where the layer 3 at the pristine surface 2 results in the Fermi level E_f being unpinned at the surface 2 and the dielectric layer 4 is made sufficiently thin to permit quantum mechanical tunneling so that a contact through a low work function metal, such as In for the metal 5 will demonstrate on a GaAs crystal essentially ohmic conduction performance. The layer 3 being of a monolayer order is thin enough not to interfere with the tunneling mechanism and the layer 4 is of the proper thickness which for most applications is of the order of 2 nm generally achieved in connection with the positioning of the metal contact 5.

In the fabricating of different types of device structures, it is desirable to have a barrier to electrical conduction that is selectable. The selectability provides controllable performance rectifying contacts and the ability to control carrier flow in an inversion channel in a device.

Referring next to FIG. 3, a band energy diagram is shown where the layer 4 is sufficiently thin to permit quantum mechanical tunneling so that when a higher work function metal, such as Au is used for the metal 5, the performance is that of a selectable Schottky barrier height. This is useful in threshold control of field effect transistors.

In FIGS. 4 through 8, the application of the invention to various types of semiconductor structures is illustrated.

Referring next to FIG. 4, there is illustrated a device wherein there is a p-n junction 6 that terminates at the surface. Where such a structural condition occurs, the carrier recombination is aggravated by the presence of very high fields illustrated at one intersection as element 7. In accordance with the invention, the layers 3 and 4 under these

conditions operate to prevent both carrier recombination and the effects of the field.

In FIG. 5, a field effect transistor semiconductor device known as a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is illustrated wherein the semiconductor substrate 1 has positioned thereon source and drain ohmic contacts 8 and 9 that go through the layer 3 on the surface 2 and dielectric layer 4 is in a shape modified to accommodate the other requirements of the device. The thin essentially monolayer thickness of the layer 3 permits the ohmic contacts 8 and 9 to be merely positioned on the layer 3 which in turn doesn't interfere with their electrical performance. The layer 4 serves as the insulator of gate 10 with the layer 4 being provided with appropriate thickness and dielectric strength to have the threshold properties for the inversion of a channel between contacts 8 and 9 at the interface of the crystal 1.

With the structural principles of the invention, it will be readily apparent that the type of selectability of the barrier shown in FIG. 3 provides flexibility in imparting characteristics to a device being fabricated.

Referring next to FIG. 6, a bipolar transistor type structure is illustrated vertically oriented with respect to the substrate wherein the substrate 1, appropriately doped, serves as the collector, with an opposite conductivity type appropriately doped base region 11 positioned adjacent the interface 2. On the layer 3 at interface 2, a circular ohmic electrode 12 is positioned separated from and surrounding a mesa semiconductor region 13 epitaxially joined at the interface 2 serving as the emitter which in turn has a contact facilitating semiconductor region 14 serving as the interface to the metal emitter contact 15.

The features of the invention are employed in this type of structure to facilitate prevention of leakage problems that occur with respect to closely positioned contacts, interfaces terminating at the surface, and ohmic performance. The two layer termination structure on pristine surface of the invention is applied around the emitter 13 shown as element 16. The layer 4 is removed in the positioning of ohmic contact 12 and the layer 3 due to the thin dimension thereof does not affect the ohmic performance of contact 12.

The principles of the invention are further applicable to facilitate construction of electro-optical conversion devices.

Referring next to FIG. 7, one of the serious problems in the electro-optical conversion field has been the translucent passivation of pn junctions that radiate light.

Referring to FIG. 7, a light emitting diode type device is shown wherein on a substrate 1, there is a high conductivity extrinsic n+ layer 18, an n-type

layer 19 and a p-type layer 20 in a mesa type configuration, with the pn junction between elements 19 and 20 serving as the light emitting source in a mesa type configuration. The light emitting junction at the surface is indicated as having a field with the circle at 21. The termination structure of the invention is shown as element 22 applied over the mesa. The ohmic contacts 23 to the n+ region 18 and 24 to the p region 20 are made by removing the layer 4, the ohmic performance being unaffected by the thin layer 3.

In this type of structure, the layers 3 and 4 in the termination of the invention are sufficiently thin not to attenuate the emitted light, yet they serve in passivation and facilitate contacting.

Referring to FIG. 8, a typical, very small, of the order of 5 to 10nm dimension active region device is shown. Such a device has come to be known in the art as a quantum wire structure. In FIG. 8, on the substrate 25 of a first band gap semiconductor material, such as GaAs, a region 26 of an atomically compatible different band gap high mobility semiconductor, such as InGaAs, is sandwiched between another layer 27 of a different band gap lower mobility semiconductor material such as GaAs in a mesa configuration. In accordance with the invention, the surface at both sides of the mesa and the substrate is coated with the termination structure comprising layer 3 on a pristine surface covered by layer 4.

The termination operates to passivate the surfaces including the hetero-interfaces between different semiconductor materials. Ohmic contacts 28 and 29 are illustrated showing the presence of the layer 3 which due to thickness does not affect ohmic contact performance. The structure of FIG. 8 would have a contact to the quantum wire region 26, not shown.

The preferred embodiment for fabrication of the structure of FIG. 1 would employ a GaAs crystal 1 which is heated with surface 2 exposed in an oxygen-free atmosphere in H₂S at 700°C for 30 seconds to render the surface 2 pristine and forms a thin, of the order of a monolayer, coating 3 of gallium sulfide. The GaS coated structure is then provided with a 1-1,000 nanometer dielectric coating 4 of low temperature plasma enhanced chemical vapor deposited silicon dioxide.

What has been described is the fact that surface termination of compound semiconductor material for device use involves insuring the absence of an agent that causes the pinning, the presence of a material that prevents the pinning, and the protection of that material with a non-metallic layer that provides capability for dielectric, ambient reaction inertness and translucence properties.

Claims

1. Compound semiconductor crystal intermediate manufacturing product comprising in combination on a pristine crystal interface of a monocrystalline compound semiconductor material taken from the group of Ga or Al or In and As or Sb and monocrystalline ternary and quaternary alloys thereof,
2. a Fermi level pinning control layer of a compound of a cation ingredient of said compound semiconductor and a member taken from the group of S, Se and Te in a thickness compatible with electrical current conduction through said layer, and
3. a surface layer of a non-metallic material.
2. Intermediate manufacturing product of claim 1 wherein said compound semiconductor crystal is GaAs and said Fermi level pinning control layer is a Ga compound.
3. Intermediate manufacturing product of claim 1 wherein said non-metallic material is taken from the group of SiO₂, CaF₂, NaS, ZnS, GaP, GaSe and polyimides.
4. Intermediate manufacturing product of claim 1 wherein said Fermi level pinning layer thickness is in a range of one monolayer to approximately 2 nm.
5. Intermediate manufacturing product of claim 1 where the surface layer is in the range of 1 to 1000 nanometers thick.
6. In the fabrication of compound semiconductor device structures, the improvement in providing a compound semiconductor crystal with a device fabrication compatible surface termination, the intermediate manufacturing product comprising on a pristine crystal interface of a monocrystalline compound semiconductor material taken from the group of Ga or Al or In and As or Sb and monocrystalline ternary and quaternary alloys thereof,
7. a Fermi level pinning control layer of a compound of a cation ingredient of said compound semiconductor and a member taken from the group of S, Se and Te in a thickness compatible with electrical current conduction through said layer, and
8. a surface layer of a non-metallic material.
7. Intermediate manufacturing product of claim 6 wherein said compound semiconductor crystal is GaAs and said Fermi level pinning control layer is a Ga compound.
8. Intermediate manufacturing product of claim 6 wherein said non-metallic material is taken from the group of SiO₂, CaF₂, NaS, ZnS, GaP, GaSe and polyimides.
9. Intermediate manufacturing product of claim 6 wherein said Fermi level pinning layer thickness is in a range of the order of one monolayer to approximately 2 nm.

10. Intermediate manufacturing product of claim 6 where the surface layer is in the range of 1 to 1000 nanometers thick.

5

10

15

20

25

30

35

40

45

50

55

6

FIG. 1

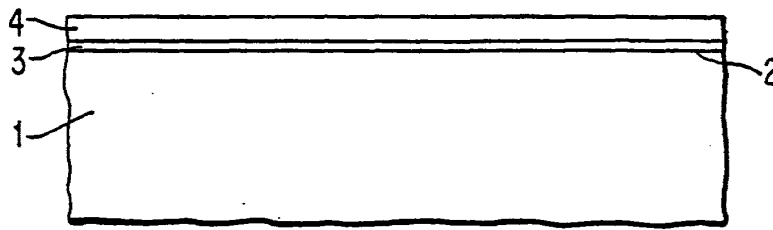


FIG. 2

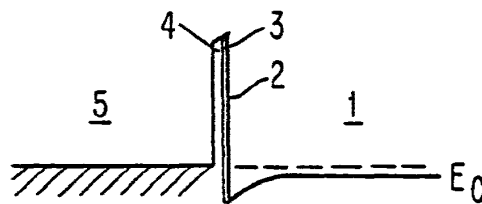


FIG. 3

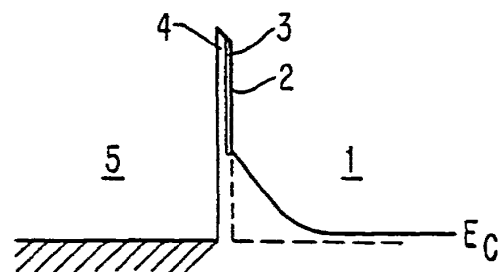


FIG. 4

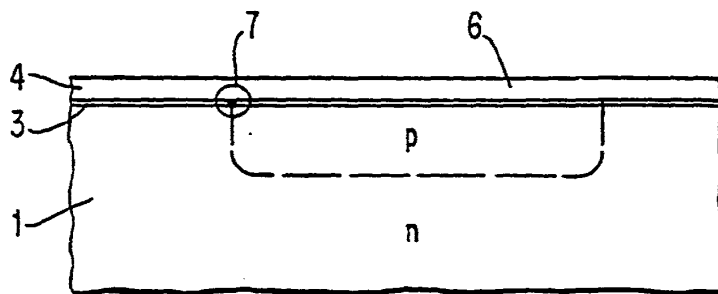


FIG. 5

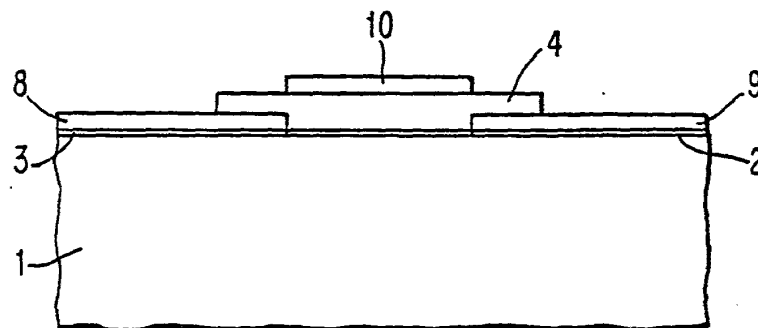


FIG. 6

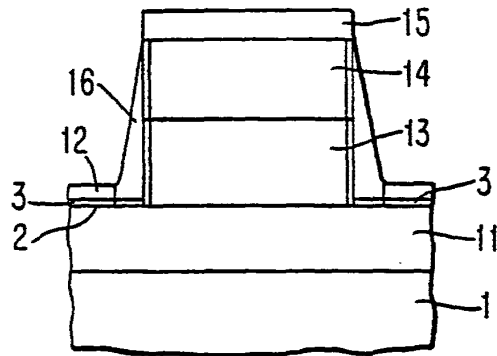


FIG. 7

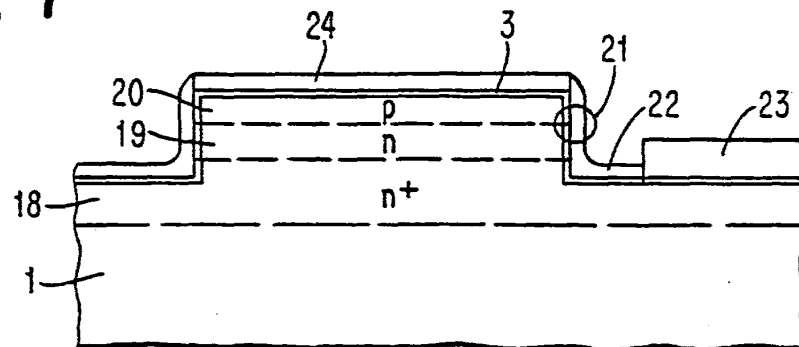
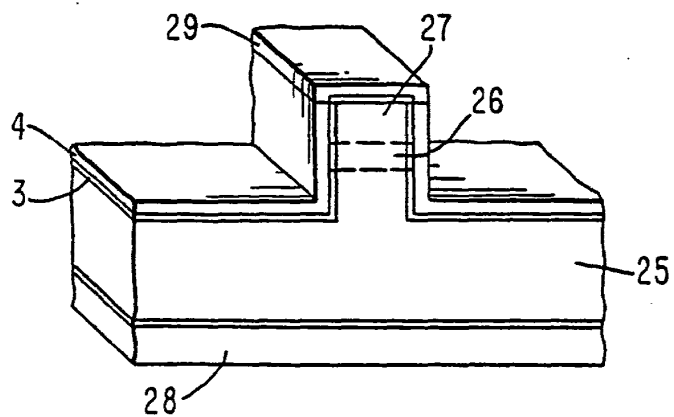


FIG. 8





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number

EP 88 10 8684

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 4)
P,X	EP-A-0 265 314 (CNET/CNRS) * Page 2, line 37 - page 3, line 36 *	1-3	H 01 L 21/314 H 01 L 29/40 H 01 L 21/285
Y	APPLIED PHYSICS LETTERS, vol. 38, no. 9, 1st May 1981, pages 693-695, American Institute of Physics, New York, US; J. MASSIES et al.: "Monocrystalline aluminium ohmic contact to n-GaAs by H ₂ S adsorption" * Abstract; page 695 *	6,7,9	
A	IDEM ---	1,2,4	
X	WO-A-8 304 420 (HUGHES AIRCRAFT CO.) * Page 12, line 24; page 15, lines 26-34; page 24, line 4 - page 26, line 30; page 27, line 1 - page 28, line 1 *	1,2,4	
Y	---	6,7,9	
A	US-A-3 983 264 (TEXAS INSTRUMENTS INC.) * Page 3, lines 1-39 *	1,2,4,6 7,9	TECHNICAL FIELDS SEARCHED (Int. Cl.4)
A	GB-A-2 046 994 (D. CHEMLA et al.) * Abstract *	1,2,6,7	H 01 L
D,A	JOURNAL OF VACUUM SCIENCE & TECHNOLOGY, vol. B3, no. 4, July/August 1985, pages 1197-1201, American Vacuum Society, New York, US; J.R. WALDROP: "Influence of S and Se on the schottky-barrier height and interface chemistry of Au contacts to GaAs" * Abstract; page 1197, right-hand column - page 1198, left-hand column * --- -/-	1,6	
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 30-09-1988	Examiner GELEBART J.F.M.
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ----- & : member of the same patent family, corresponding document			

EPO FORM 1503 03.82 (P0401)



DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. CL.4)
A	JOURNAL OF THE ELECTROCHEMICAL SOCIETY, vol. 134, no. 2, February 1987, pages 437-439, Manchester, NH, US; T. NARUSAWA et al.: "Structural study of GaAs-dielectric film (CaF ₂ ,Al ₂ O ₃) interfaces by high-energy ion scattering" * Abstract *	3,8	
D,A	JOURNAL OF VACUUM SCIENCE & TECHNOLOGY, vol. 17, no. 5, September/October 1980, pages 1134-1140, American Vacuum Society; J. MASSIES et al.: "Effects of H ₂ S adsorption on surface properties of GaAs (100) grown in situ by MBE"		
			TECHNICAL FIELDS SEARCHED (Int. CL4)
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 30-09-1988	Examiner GELEBART J.F.M.
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ----- & : member of the same patent family, corresponding document	

EPO FORM 1503 01.82 (P0401)

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

(19)



Europäisches Patentamt

European Patent Office

Office européen des brevets



(11)

EP 0 789 388 A2

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:

13.08.1997 Bulletin 1997/33

(51) Int Cl.⁶: H01L 21/285

(21) Application number: 96306139.5

(22) Date of filing: 22.08.1996

(84) Designated Contracting States:

DE FR GB

(30) Priority: 25.08.1995 JP 216935/95

25.03.1996 JP 68018/96

(71) Applicant: AGENCY OF INDUSTRIAL SCIENCE
AND TECHNOLOGY
Chiyoda-ku Tokyo (JP)

(72) Inventors:

- Hara, Shiro
Tsukuba-shi, Ibaraki (JP)

- Kajimura, Koji
Tsukuba-shi, Ibaraki (JP)
- Okushi, Hideyo
Tsukuba-shi, Ibaraki (JP)
- Teraji, Tokuyuki
Tsukuba-shi, Ibaraki (JP)

(74) Representative: Beresford, Keith Denis Lewis
BERESFORD & Co.
2-5 Warwick Court
High Holborn
London WC1R 5DJ (GB)

(54) Structure and fabrication method for schottky and ohmic electrodes onto semiconductor devices

(57) A novel electrode structure for Schottky electrodes and Ohmic electrodes and novel methods of fabricating electrodes by freely controlling electric characteristics of electrodes on semiconductors. Interface states density of a semiconductor (11) after deposition of an electrode metal (13, 14) is decreased by flattening the surface of the semiconductor on an atomic level to freely control the Schottky barrier height. The method can realize an ideal Ohmic electrode having a Schottky barrier height of substantially zero. The Schottky barrier height is varied freely by decreasing the interface level density and selecting work function of the electrode metal. The method can provide stable Schottky and Ohmic electrodes (13, 14) without need of heat treatment. Further, the method can provide Ohmic electrodes without high concentration doping.

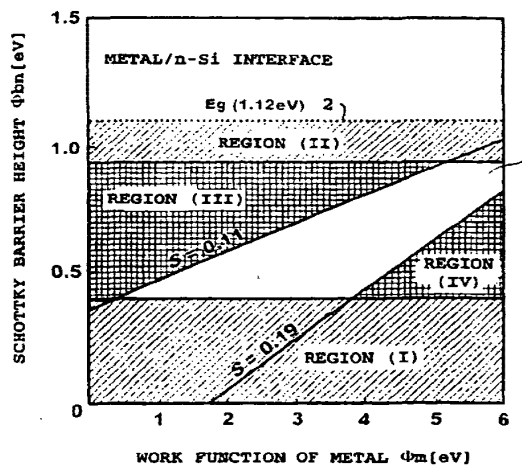


FIG. 2

EP 0 789 388 A2

Description

The present invention relates to an electrode provided on a semiconductor and a method for fabricating an electrode on a semiconductor. The present invention is applicable to various fields of industry which involve fabrication of electrodes on semiconductors. For example, the present invention can be applied to various semiconductor devices such as microprocessors, memories, power devices and the like.

In conventional fabrication methods of electrodes on semiconductors, rectifying potential barriers, i.e., Schottky barriers, which will appear on the interfaces between electrode metals and semiconductors, have been impossible to control their magnitude. Hence, it has been impossible to artificially control the rectifying properties and conductivities of all the electrodes including not only those semiconductor devices whose performance depends directly on the heights of Schottky barriers, such as Schottky diodes as typical examples, but also those electrodes in the semiconductor devices thus far fabricated. The Schottky barrier height and leakage current, which is an indicator of important performance of interface on the device, inconveniently vary to a greater extent depending on combination of metals and semiconductors as well as on the process in which the interface is formed. Conventionally, this problem has been solved empirically. That is, when a new semiconductor has been developed, a method for fabricating an electrode on the semiconductor has been investigated and developed for each metal one after another until a suitable one is obtained. In other words, going into detail, there have conventionally been developed unique fabrication methods for fabricating electrodes adapted for respective combinations of semiconductors and electrode metal materials. Because of having had to resort to empirical rule, methods for fabricating electrodes differ from institution to institution or from manufacturer to manufacturer. There has been established no fabrication method for fabricating electrodes which method can be uniformly applied to any or most of electrode metal/semiconductor combinations. Under the circumstances, development of electrodes has needed much human and monetary resources for investigation. In all the semiconductor device fabrication technology inclusive of technologies for fabricating integrated semiconductor devices such as VLSIs and the like, only the technology for forming electrodes has remained as a unit technology that is out of reach of successful efforts for free designing.

More specific explanation will be made as to how to fabricate electrodes for Schottky electrodes and Ohmic electrodes, respectively.

First, in the case of Schottky electrodes, it was almost impossible to control their Schottky barrier height and, hence there was no other way than accept such non-controlled values as they are. For example, silicon Schottky diodes have almost fixed barrier heights on the order of about 0.5 to about 0.7 eV. While use of different metals or application of heat to cause interface reaction will vary barrier height to some extent, the width of change in barrier height is at most about 0.2 eV. Thus, in Schottky devices, the Schottky barrier height, which is the most important indicator for the device characteristics, cannot be controlled freely.

In the case of Ohmic electrodes, a severer problem arises. That is, electrode fabrication inevitably results in the formation of a Schottky barrier whose interface usually shows rectifying resistance. As a result, formation of a conductive Ohmic electrode, which is contrary to the fabrication of an electrode having a rectifying resistance, requires in principle a very difficult technique. Practically, in fabrication of almost all of the Ohmic electrodes fabricators have presupposed presence of a Schottky barrier in the interface between the electrode metal and semiconductor and then taken a measure to allow a leakage current to flow in the barrier.

There have been known several methods for increasing a leakage current. For example, a method for fabricating a device in which impurity ions are doped to extremely increase the concentration of electrons or holes which contribute to conductivity in the vicinity of the surface of the semiconductor (cf., e.g., E.H. Rhoderick and R.H. Williams: "Metal-Semiconductor Contacts, 2nd Ed.," Oxford Science Publications, 1988, M. Murakami: Materials Science Reports, 5, 273 (1990), P.A. Barnes and A.Y. Cho, Appl. Phys. Lett., 33, 651 (1978), and T. Uemoto: Jpn. J. Appl. Phys., 34, L7 (1995)). This reduces the width of the Schottky barrier, i.e., decreases the thickness of the depletion layer and, hence, a leakage current in the form of tunneling current, can be flown in the thin depletion layer. However, in the case of SiC, GaN and the like new semiconductor materials that are under development are usually difficult to dope with impurities at high concentrations so that electrodes having sufficiently low resistance cannot be obtained in most cases. The above-described method is not simple nor convenient in some cases since it requires an ion implanting apparatus or an electric oven for diffusing impurities in gaseous phases. Furthermore, the concentration of impurities has an upper limit at about 10^{20}cm^{-3} . This automatically determines the minimum width of the depletion layer and, hence, sets technical limits to the interface resistance of an Ohmic electrode to be realized. Theoretically, this approach is unsuccessful in making the interface resistance of the Ohmic electrode to be zero. In addition, there may occur reflection of electrons or holes between the high concentration doped region and the low concentration doped substrate. This reflection of carriers increases the resistance of the electrode. From these, the interface resistance of an Ohmic electrode fabricated on a silicon substrate is limited to about $10^{-8}\ \Omega\text{cm}^2$ based on the technical restrictions as described above.

Another method for fabricating an Ohmic electrode is to heat the electrode to decrease its resistance (cf., e.g., E. H. Rhoderick and R.H. Williams: "Metal-Semiconductor Contacts, 2nd Ed.," Oxford Science Publications, 1988, M.

Murakami: Materials Science Reports, 5, 273 (1990), H.C. Card: IEEE Trans. Electron Devices, ED-23, 538 (1976), T.C. Shen, G.B. Gao, and H. Morkoç: J. Vac. Sci. Technol., B10, 2113 (1992), N. Braslau, J.B. Gunn, and J.L. Staples: Solid-State Electronics, 10, 381 (1967), J. Appl. Phys., 77, 1317 (1967), and J. Crofton, P.G. McMullin, J.R. Williams, and M.J. Bozack: J. Appl. Phys., 77, 1317 (1995)). In this method, after the electrode metal is deposited, heat treatment is carried out so that there occurs interface chemical reaction between the metal and the semiconductor and metallization of the semiconductor proceeds in the vicinity of the interface. This induces impurity level or defect level in the depletion layer of the Schottky barrier. These levels generate leakage current. This method is simple and can be used in combination with high concentration doping. Because of the advantages, the method is used without fail in the conventional process of fabricating electrodes. However, interface reaction is complicated since it differs from a metal/semiconductor system to another and the mode of reaction varies widely depending on temperature and time of heat treatment. In some reaction systems, it is often the case that heating results in the formation of good Schottky barrier, which means heating does not always enhance Ohmicity (cf., e.g., S. Zaima, T. Yamauchi, Y. Koide, and Y. Yasuda: Appl. Surf. Sci., 70, 624 (1993)). This is a decisive defect of the above-described heating method.

Still another approach is to grow on a first semiconductor a crystal of a second semiconductor having a bandgap smaller than that of the first semiconductor so that the highest possible Schottky barrier height can be decreased to facilitate the formation of Ohmic contact (cf., e.g., E.H. Rhoderick and R.H. Williams: "Metal-Semiconductor Contacts, 2nd Ed.," Oxford Science Publications, 1988, M. Murakami: Materials Science Reports, 5, 273 (1990), and T.C. Shen, G.B. Gao, and H. Morkoç: J. Vac. Sci. Technol., B10, 2113 (1992)). This method involves heteroepitaxy of a semiconductor and, hence, its application is limited to semiconductor systems which allow heteroepitaxy.

Further, heteroepitaxy itself is a high technology which requires a complicated manufacturing process, which increases production costs. Therefore, the method is suited to a very limited range of semiconductor materials, more particularly, new semiconductor materials having wide bandgaps, such as GaN and the like, which are difficult to dope impurities with high concentration doping of impurities.

The above-described three methods use large process apparatus suitable for fabricating devices and thus are not simple. Accordingly, in early stages of research and development for evaluating electric properties of materials or developing various devices, simpler means such as scratching of semiconductor or the like is used (here, by the term "scratching" is meant to hurt the surface of a semiconductor with a diamond needle or the like to coarsen it (cf., e.g., E.H. Rhoderick and R.H. Williams: "Metal-Semiconductor Contacts, 2nd Ed.," Oxford Science Publications, 1988). On a coarse surface, a lot of structural defects are induced which increase leakage current. This method is quite inconvenient for making fine structures in the fabrication of semiconductor devices. In most cases, no good interface resistance can be obtained.

As described above, electrodes have been fabricated based on empirical rules. The primary reason for this is a lack of common or uniform understanding of the mechanism in forming a metal/semiconductor interface potential barrier. Uncontrollability of Schottky barriers and complexity of the mechanism of Ohmic contact formation which is attributable thereto would be due to the fact that Schottky barrier height is by nature fixed to a certain level. Fixation of Schottky barrier height of a semiconductor is equivalent to the fact that the Fermi level is fixed in the bandgap of the semiconductor on the metal/semiconductor interface. The fixation of Fermi level is usually referred to pinning of the Fermi level. The pinning of the Fermi level occurs as a result of generation of electron level in the bandgap of a semiconductor on the interface between the metal and the semiconductor. Carriers flow from bulk to the interface, i.e., electrons in the case of n-type semiconductor or holes in the case of p-type semiconductor flow from the bulk semiconductor to the interface and the carriers are trapped therein to create an electric double layer of the semiconductor bulk and the interface, i.e., a potential barrier or Schottky barrier.

Reviewing the development of Schottky barrier, in 1947, J. Bardeen stated that the interface level is caused by electronic level due to dangling bonds and the like existing on the surface of the semiconductor (cf. J. Bardeen: Phys. Rev., 71, 717 (1947)). Thereafter, however, in view of the impossibility of controlling the surface level density accurately by the technology available at that time, the leading view was that surface level density was uncontrollable and intrinsic to the material concerned, and interface electron level embedded in a solid should be an essential electron level that was more difficult to control than the surface level. The belief that pinning was intrinsic to materials and cannot be controlled artificially has led to a theory of MIGS (Metal-induced Gap States) which explains a cause of generation of interface levels (cf. V. Heine: Phys. Rev., 138, A1689 (1965)). According to this theory, interface levels are induced when a metal approaches toward the semiconductor. Since 1965 when V. Heine proposed it, the MIGS theory has been leading to date. The MIGS theory has inhibited research of a technology which controls the height of Schottky barrier. In fact, regardless of theories, there have been unavailable high technologies that can control interface level density in actual semiconductor devices.

Concerning numerical consideration of pinning, the work which referred to Schottky barrier for the first time was by W. Schottky (cf. W. Schottky: Naturwissenschaften, 26, 843 (1938) and N.F. Mott: Proc. Camb. Philos. Soc., 34, 568 (1938)). According to Schottky, the Schottky barrier height, ϕ_{bn} , of a n-type semiconductor is given by the following equation (1):

EP 0 789 388 A2

$$\phi_{bn} = \phi_m - \chi S + C \quad (1)$$

wherein ϕ_m is a work function of the metal, χS is electron affinity of the semiconductor, C is a constant no greater than several meV. On the other hand, the Schottky barrier height of a p-type semiconductor in a pinning-free state is given by the following equation (2):

$$\phi_{bp} = E_g - (\phi_m - \chi S + C) \quad (2)$$

wherein E_g is a bandgap.

The equations (1) and (2) are called Schottky models. However, no interface has been realized that meets these equations. The actual interface is expressed by the following equation (3):

$$\phi_{bn} = S (\phi_m - \chi S) + C \quad (3)$$

wherein S is a coefficient which indicates a dependence of ϕ_{bn} on ϕ_m and $0 \leq S \leq 1$.

When $S=0$, ϕ_{bn} is constant and the interface is pinned strongly. This state is called a Bardeen barrier. On the contrary, when $S=1$, the equation (3) is the same as the equation (1) and represents a pinning-free interface according to the Schottky-Mott model. Actual interfaces fall between the both states. Heretofore, the S factor has been believed to be a physical property specific to the material concerned and, hence, beyond control.

Table 1 below summarizes values of S factor and maximum and minimum values of Schottky barrier height of representative semiconductors.

Table 1

PINNING RATIOS S OF VARIOUS KNOWN SEMICONDUCTORS AND RANGE OF SCHOTTKY BARRIER HEIGHT

SEMI- CONDUCTOR	S FACTOR	INTERCEPT PARAMETER	MINIMUM SCHOTTKY BARRIER HEIGHT [eV]	MAXIMUM SCHOTTKY BARRIER HEIGHT [eV]
Ge	$0.18 \geq S \geq 0.05^1$	$-0.23 \leq C_2 \leq 0.11^1$		
Si (001)	$0.19 \geq S \geq 0.11^1$	$-0.34 \leq C_2 \leq 0.35^1$	$0.37 (\text{GdSi}_2/\text{HoSi}_2)^2$	$0.94 (\text{IrSi}_3)^3$
GaAs (001)	$0.22 \geq S \geq 0.06^1$	$-0.40 \leq C_2 \leq 0.075^1$	$0.62 (\text{Mg})^4$	$0.96 (\text{Cu})^4$
GaP	$0.21 \geq S \geq 0.07^1$	$0.45 \leq C_2 \leq 0.80^1$		
InP	$0.37 \geq S \geq 0.24^1$	$-1.00 \leq C_2 \leq 0.81^1$		
ZnS	$0.66 \geq S \geq 0.21^1$	$-1.63 \leq C_2 \leq 0.91^1$		
ZnSe	$0.24 \geq S \geq 0.17^1$	$-0.25 \leq C_2 \leq 0.57^1$		
6H-SiC (0001)	$0.25 \geq S \geq 0.23^{5-10}$	$-3.5 \leq C_2 \leq 0.15^{5-10}$	$0.73 (\text{Ti})^6$	$1.37 (\text{Au})^5$

1. B.L. Sharma and S.C. Gupta, Solid State Technology, **23**(6), 90 (1980).
2. K.N. Tu, R.D. Thompson, and B.Y. Tsaur, Appl. Phys. Lett. **38**, 626 (1981).
3. C.S. Petersson, et al., J. Appl. Phys., **50**, 3357 (1979).
4. J.R. Waldrop, J. Vac. Sci. Technol., **B2**, 445 (1984).
5. J.R. Waldrop, et al., J. Appl. Phys., **72**, 4757 (1992).
6. J.R. Waldrop, et al., Appl. Phys. Lett., **62**, 2685 (1993).
7. L.M. Porter, et al., Mat. Res. Soc. Symp. Proc., **287**, 471 (1993).
8. L.M. Porter, et al., J. Mat. Res., **10**, 26 (1995).
9. L.M. Porter, et al., J. Mat. Res., **10**, 668 (1995).
10. L.M. Porter, et al., M. Mat. Res. **10**, 2336 (1995).

Fig. 1 is a graphical presentation of the data in Table 1, plotting Schottky barrier height (ϕ_{bn} [eV]) against work function of a metal (ϕ_m [eV]) taking as an example of an n-type Si(001) semiconductor substrate. Fig. 1 shows that the Schottky barrier height was limited within a certain range for various metals. In Fig. 1, reference numeral 1 denotes an area representing the range in which the Schottky barrier heights of conventionally fabricated metal-Si interfaces fall and 2 denotes a line which represents an absolute upper limit of the Schottky barrier height of metal-In-Si interfaces corresponding to the bandgap $E_g = 1.12$ eV. With different metals, there are always upper and lower limits of the Schottky

barrier heights.

Consequently, it has heretofore been impossible to freely control the Schottky height of metal/semiconductor interfaces.

The present invention is directed to overcoming the problem of uncontrollability of the Schottky barrier height between an electrode metal and a semiconductor, which problem has been an important subject since a transistor was invented.

Also, the present invention is aimed at solving the scientific and technological problem of uncontrollability of Ohmic electrodes, which has heretofore been considered a different problem from the uncontrollability of Schottky barrier height.

Further, the present invention is intended to provide a systematic technology which can control both Schottky electrodes and Ohmic electrodes, that have been treated separately one from another, based on a single principle that allows understanding them consistently. More specifically, the present invention is directed to overcoming the problem of uncontrollability of pinning of Fermi level of the interface of metal/semiconductor that has been impossible to control conventionally.

Therefore, an object of the present invention is to provide a method for fabricating Schottky electrode or Ohmic electrode formed at the interface between an electrode metal/semiconductor, which enables freely controlling electric properties of the electrode formed on the semiconductor.

Another object of the present invention is to provide an electrode structure comprising an electrode having a controlled Schottky barrier height of the interface between the electrode metal and the semiconductor.

According to a first aspect of the present invention, there is provided a method of fabricating a layer of an electrode metal on a surface of a semiconductor, comprising the step of:

decreasing a surface states density of the surface of the semiconductor.

According to a second aspect of the present invention, there is provided a method of fabricating a layer of an electrode metal on a surface of a semiconductor, comprising the step of:

controlling a Schottky barrier height of a rectifying Schottky electrode formed on the surface of the semiconductor.

Here, the control of the Schottky barrier height of the Schottky electrode may be carried out by controlling flatness of an electrode metal/semiconductor interface.

The control of the Schottky barrier height of the Schottky electrode may be carried out by controlling a step density on an atomic level of an electrode metal/semiconductor interface.

The control of the Schottky barrier height of the Schottky electrode may be carried out by controlling selecting a work function of the metal.

The control of the Schottky barrier height of the Schottky electrode may be carried out by controlling the Schottky barrier height of the Schottky electrode under conditions without giving thermal hysteresis.

According to a third aspect of the present invention, there is provided a method of fabricating a layer of an electrode metal on a surface of a semiconductor, comprising the step of:

fabricating a Schottky electrode from a metal having a high work function, and fabricating an Ohmic electrode from a metal having a low work function, for an n-type semiconductor, or
fabricating a Schottky electrode from a metal having a low work function and an Ohmic electrode from a metal having a high work function, for a p-type semiconductor.

Here, the method may further comprise the step of heating.

According to a fourth aspect of the present invention, there is provided a method of fabricating an Ohmic electrode, comprising the step of: forming flat electrode metal/semiconductor interface on an atomic level.

According to a fifth aspect of the present invention, there is provided a method of fabricating an Ohmic electrode, comprising the step of: forming an electrode metal/semiconductor interface having a low step density on an atomic level.

According to a sixth aspect of the present invention, there is provided a method of fabricating an electrode, comprising the step of:

fabricating an Ohmic electrode as described above in a highly integrated electronic device.

Here, the semiconductor may be made of a semiconductor selected from the group consisting of Si and SiC.

The electrode metal may be selected from the group consisting of Al, Au, Mo and Ti.

According to a seventh aspect of the present invention, there is provided a Schottky electrode structure provided on a semiconductor having an interface portion which is flat on an atomic level.

According to an eighth aspect of the present invention, there is provided a Schottky electrode structure provided on a semiconductor having a Schottky barrier height which is impossible to realize by conventional method.

According to a ninth aspect of the present invention, there is provided a Schottky electrode structure provided on a semiconductor containing no high concentration impurity.

According to a tenth aspect of the present invention, there is provided an Ohmic electrode structure having a Schottky barrier height which is substantially zero.

Here, the semiconductor may be made of a semiconductor selected from the group consisting of Si and SiC.

The electrode metal may be selected from the group consisting of Al, Au, Mo and Ti.

According to an eleventh aspect of the present invention, there is provided a method of fabricating an electrode, comprising the step of:

oxidizing a surface layer of silicon or silicon carbide on a surface of a semiconductor and removing the resulting oxide film.

Here, the oxidizing of the silicon or silicon carbide may be carried out by heating the silicon or silicon carbide in an oxidative gaseous atmosphere.

Removing the oxide film may be carried out by reacting the oxide film with a reducing liquid or gas.

The silicon or silicon carbide may be n-type silicon or n-type silicon carbide, and wherein the electrode metal is a metal having a work function lower than that of noble metals.

The silicon carbide may be p-type silicon carbide, and wherein the electrode material is a noble metal or a metal having a work function of a level substantially equal to that of noble metals.

The electrode material may be titanium (Ti).

The electrode material may be aluminum (Al).

The above and other objects, effects, features and advantages of the present invention will become more apparent from the following description of the embodiment thereof taken in conjunction with the accompanying drawings.

Fig. 1 is a graph plotting Schottky barrier height of a Schottky electrode fabricated on an n-type Si(001) substrate by a conventional method against the work function of the electrode metal;

Fig. 2 is a graph illustrating regions representing Schottky barrier heights realized by the fabrication method of the present invention;

Fig. 3 is a graph illustrating current-voltage characteristics of Ti electrodes on SiC according to examples of the present invention;

Fig. 4 is a graph illustrating current-voltage characteristics of a Ti electrode on SiC which has been subjected to a conventional treatment with 5% hydrofluoric acid;

Fig. 5 is a graph illustrating current-voltage characteristics of an Al electrode on SiC according to the present invention;

Fig. 6 is a graph illustrating current-voltage characteristics of Al electrodes on SiC according to the present invention;

Fig. 7 is a graph illustrating current-voltage characteristics of an Al electrode on Si(111) which has been subjected to a conventional treatment with 5% hydrofluoric acid;

Fig. 8A is a sketch prepared based on an optical micrograph of the surface of a Ti electrode fabricated by the fabrication method according to EXAMPLE 4 of the present invention;

Fig. 8B is a schematic cross sectional view showing the Ti electrode illustrated in Fig. 8A;

Fig. 9A is a sketch prepared based on an optical micrograph of the surface of an Ni electrode fabricated by a conventional fabrication method;

Fig. 9B is a schematic cross sectional view showing the Ti electrode illustrated in Fig. 9A;

Fig. 10 is a graph illustrating logarithmic current-voltage characteristics of Au electrodes on 6H-SiC(0001) substrates according to EXAMPLE 7 of the present invention;

Fig. 11 is a graph plotting Schottky barrier height of electrode metals fabricated on 6H-SiC(0001) substrates against the work function of the electrode metals; and

Fig. 12 is a graph illustrating new areas for Schottky barrier heights of electrode metals fabricated on 6H-SiC(0001) substrates using the techniques of the present invention.

In order to solve the problem of uncontrollability of Schottky barrier height, it is only necessary to decrease the interface states density of the interface between an electrode metal and a semiconductor on which the electrode metal layer is formed. According to the present invention, a decrease in the interface states density is realized by decreasing the surface states density of the semiconductor before deposition of a metal thereon. The decrease in the surface states density can be realized primarily by flattening the surface of a semiconductor on an atomic level.

Flattening of the surface of a semiconductor results in a decrease in an atomic step density which generates dangling bond density which is a cause of surface states and in an amount of unstable atoms adsorbed on the surface of the semiconductor. According to the present invention, it has been found for the first time that flattening of the surface of a semiconductor on an atomic level decreases the surface states density of the semiconductor and that a decrease in the surface states density is effective for decreasing the interface states density of the electrode metal/semiconductor structure.

Recently, the technology of flattening the surface of semiconductors on an atomic level has developed rapidly and a variety of methods have been proposed. The present invention uses the newest known atomic level surface flattening

technologies to demonstrate the above effect. However, the present invention should not be construed as being limited to specific atomic level surface flattening techniques. There have been known several important techniques for flattening surfaces of semiconductors on an atomic level, all of which have been proved useful in decreasing interface level density according to the present invention.

5 The present invention is based on a principle contrary to the conventional method in which particularly in the case of Ohmic contact, the desired Ohmic contact has been realized by intentionally decreasing ideality of interface, i.e., abruptness of structural connection.

Description will be made on how to flatten the surface of a semiconductor on an atomic level. An example of such a method is to set up conditions of oxidation appropriately so that oxidation can proceed flat on an atomic level, thus making the surface of the semiconductor after etching more flattened than the original surface.

10 Another method is a treatment with dilute hydrofluoric acid adjusted to have an appropriate pH. The pH of the solution can be rendered alkaline with ammonia water. Such a solution has an activity of flattening the surface of a semiconductor on an atomic level by means of a weak etching action of a lot of OH groups contained in the solution. Similarly, a semiconductor may be immersed in boiling water. This method can flatten the surface of a semiconductor on an atomic level by means of a weak etching action of deionized water.

15 High temperature heat treatment in hydrogen gas is also effective for flattening the surface of a semiconductor. Homoepitaxial growth can accelerate surface migration of atoms at relatively low growth rates to flatten the surface of crystal growth. As the last example, a method utilizing electromigration can also be used for flattening the surface of a semiconductor on an atomic level. Electromigration is a phenomenon in which upon application of electric current to a sample, surface atoms will migrate in a direction the same as or opposite to the direction in which electric current flows. Use of this method semiconductor surfaces can be flattened depending on the conditions. The present invention is not limited to the above-described specific methods. Instead, any method that can flatten semiconductor surfaces on an atomic level may be used similarly and will be effective for decreasing interface levels.

25 Hereinbelow, the idea of flattening semiconductor surfaces on an atomic level will be described in more detail. To be flat on an atomic level means existence of wide flat terraces when viewed on an atomic level. This directly indicates that an atomic step density is low in the surface concerned. Atoms at a step generally have more dangling bonds than atoms on a terrace. While the dangling bonds on a terrace will disappear after the formation of an interface with a metal due to bonding with the metal, the dangling bonds at a step will not disappear completely because of the step or difference in height as high as the thickness of one atomic layer. Therefore, after the formation of an interface, a main cause of generation of interface states is dangling bonds at steps. In other words, a decrease in a step density will result in a decrease in an interface level density. Hence, in order to decrease an interface states density, it is sufficient to flatten the surface of a semiconductor so that its step density can be decreased. Thus, even if the surface is not flattened when viewed on a scale on the order of micrometers, existence of wide terraces in more minute regions will suffice for decreasing interface states. Therefore, electrode structures with an interface having wide terraces on an atomic level, even though they have uneven or rough surfaces when viewed in a broader region, will cause a decrease in surface states density and, hence, fall within the scope of the present invention as defined below in appended claims.

30 If the interface states density is reduced enough by one of the above-described methods, the pinning of Fermi level will disappear. On such a pinning-free interface, what determines its potential barrier is merely a difference between respective Fermi levels, i.e., a difference between respective work functions, of the metal and the semiconductor. In this case, Schottky-Mott model expressed by equations (1) and (2) above is followed. Therefore, in the case of an n-type semiconductor, use of a metal having a high work function results in the formation of a Schottky barrier while use of a metal having a low work function gives rise to an Ohmic contact. To control the Schottky barrier height, it is only necessary to select an appropriate metal with regard to work function. For p-type semiconductors, the same idea as that for n-type semiconductors can be applied except that relationship of the magnitudes of the work functions should be reversed.

35 According to the present invention, the Schottky barrier height of a semiconductor can be expanded to a minimum value of 0 eV (cf. Fig. 2, region (I)) and a maximum value equivalent to the bandgap (cf. Fig. 2, region (II)).

Also, controlling the degree of pinning will in effect vary the Schottky height and, hence, controlling interface level density will enable the Schottky barrier height even when the same metal is used. That pinning can be controlled means that the Schottky barrier height can be controlled at will for each metal. As a result, the region where the Schottky barrier height can be controlled is expanded to regions (III) and (IV) in Fig. 2.

40 As described above, the present invention has made it possible to expand the region where the Schottky barrier height can appear from region (1) to regions (I) to (IV) in Fig. 2. Therefore, for a given metal, electrodes having the Schottky barrier heights within one of the regions (I) to (IV) also fall within the scope of the present invention. The present invention is generally applicable and operable regardless of the kind of metal and for all n-type and p-type semiconductor substrates, can be set up the regions (I) to (IV) as illustrated in Fig. 2 according to the present invention. Table 1 above indicates the Schottky barrier height regions of the present invention for representative semiconductor materials.

Another important feature of the present invention is that control of Schottky/Ohmic property can be performed without heat treatment. However, if heat treatment is carried out after the deposition of electrode metals, still a flat interface can be obtained since originally a flat surface on an atomic level is provided, an interface reaction between the metal and the semiconductor occurs uniformly in the interface therebetween. Therefore, the present invention is also effective to electrodes which are subjected to heat treatment.

While not intended to be bound thereto, the present invention can be applied suitably to fabrication of electrodes on silicon carbide (SiC). While SiC is a material with which p- and n-type semiconductors can be used with ease, they have various excellent physical properties such as large a large bandgap. The present invention will be explained further taking SiC as an example. Since in the present invention, processes are used that do not involve heat treatment, no appreciable interface chemical reaction does occur between the metal and the semiconductor. Therefore, the resulting interface receives the conditions of the surface of the semiconductor without any change, and the interface has electrical characteristics which depend on structural and chemical properties of the surface of SiC before the deposition of the electrode metal. In other words, control of the conditions of the surface of SiC makes it possible to control electric properties freely.

When no treatment is performed on the surface of SiC, a natural oxide film is formed thereon. Also, a lot of water and/or impurity atoms are adsorbed on the SiC surface. Further, in the case of as ground surfaces, there are near the surface a lot of impurity atoms contaminating or defects induced upon grinding. Such conditions depend strongly on the process by which the SiC surface is fabricated so that the resulting surface does not always have the same surface atomic conditions and surface electronic state and then unstable.

In the present invention, a method is used which depends strongly on the conditions of surface atoms as described above. Therefore, such an unstable surface layer must be removed. For this purpose, SiC is oxidized and then the resulting oxide film is removed. The oxidation and removal of the oxide film may be performed simultaneously.

As a specific example of oxidation method for oxidizing silicon carbide (SiC), there can be used a method in which SiC is heated in an oxidizing gas atmosphere. The oxidation can be carried out at a heating temperature within the range of usually 800 to 1,250°C, preferably 950 to 1,150°C.

Concerning the selection of metals for use as an electrode material, a lot of metal materials with which Ohmic electrodes have not been realized by the conventional high temperature heat treatment can be used for forming Ohmic electrodes according to surface condition controlling technique in the fabrication method for fabricating electrodes on SiC according to the present invention. Properly speaking, a theoretical approach for realizing an Ohmic contact for n-type semiconductors is to use metal materials having a low work function. However, conventionally, Ohmic contacts were obtained by coarsening or roughening the interface by means of high temperature heat treatment to provide the interface with a non-ideal (non-uniform) structure and metal materials having a high work function which are difficult to oxidize were used in order to prevent the high temperature oxidation. On the contrary, in the present invention, heat treatment does not have to be done so that the interface is abrupt enough to be ideal one and then it is possible to realize an Ohmic contact for those metal materials which do not have high work function naturally. Here, metals which do not have high work functions are those metal materials composed mainly of elements other than noble metals (Ni, Pd, Pt, Cu, Ag, and Au) having high work functions, such as Ni which has been used conventionally. More specifically, a wide variety of metals can be used, including, for example, Mg, Ca, Sr, Ba, Sc, Y, La, Ti, Zr, Hf, V, Nb, Ta, Cr, Mn, Re, Fe, Al, Ga, In, Tl and the like. Among these, those metals having not so high an oxidizing capability, e.g., Ti and Al are preferred.

In order to realize Ohmic contacts with p-type semiconductors, theoretically, metal materials having high work functions should be used. Conventionally, however, Ohmic contacts were formed by addition of impurities in high concentrations and hence, aluminum (Al) has been used as an electrode metal because it can serve as a p-type impurity. However, Al has a low work function and is not suited as a metal for p-type metals. In the present invention, metals having high work functions are used. More specifically, metals which can be used for p-type semiconductors for forming Ohmic contacts include noble metals such as Ni, Pd, Pt, Cu, Ag, and Au and metals having approximately the same work function as the noble metals, such as Co, Rh, Ir, Ru, Os, and Re.

In the case of n-type SiC, if heat treatment is required after the formation of electrodes, a metal which is resistant to oxidation and has a high work function can be deposited on the above-described electrode metals having low work functions to prevent oxidation of the electrode portions. Similar effects can be obtained by depositing two or more metals having low work functions on a metal forming a metal semiconductor interface. Therefore, if heating is needed or desired, the above-described effect of the present invention cannot be deteriorated. What is important in the present invention is to use a metal having a low work function for an n-type SiC and a metal having a high work function for a p-type SiC. Practically, metals are divided into low and high work function metals when they have work functions up to 4.5 eV or higher than 4.5 V. However, 4.5 V is not a strict threshold value. This is because when a metal is deposited on SiC at ambient (room) temperature, e.g., about 20°C, mutual diffusion of the atoms constituting the metal and the atoms constituting the SiC semiconductor may occur on the metal/semiconductor interface and effective work function alters if the metal used is highly reactive. So, 4.5 eV is to be understood to be a practical standard for classifying

metals.

More specifically, the present invention comprises an oxidation process using an oxidative gas. Usually, a sample is placed in an oxidative atmosphere in an apparatus which enables heating of the sample, such as electric oven, and the sample is heated at a temperature within the range of 800 to 1,250°C. With this treatment, the surface of the sample becomes insulating due to formation of an oxide film thereon and a sufficient electric contact is not achieved. Then, the oxide film is removed with a reducing liquid or gas. It is often the case that the atoms on the surface of SiC are arranged or accumulate in a manner different from that the atoms in the bulk of the SiC. The oxidation process in an oxidative gaseous atmosphere is meant to oxidize such a denatured surface layer and make the surface layer ready to be removed by a liquid process including dissolving the surface oxide layer with a reducing liquid to remove it, or gaseous process involving reducing the surface oxide layer with a reducing gas to convert the oxide layer to a semiconductor of non-oxidized state.

In conventional processes for fabricating electrodes, immersion or dipping of a semiconductor in a dilute hydrofluoric acid has been conducted to remove spontaneous oxide film on the surface of SiC. However, no intentional or artificial oxidation of SiC has been performed so that the unstable surface layer has not been removed completely, thus failing to provide stable Ohmic contacts.

According to the present invention, development of Schottky and Ohmic electrodes, which has heretofore been made relying on experience or empirical rules, can be made in a shorter time than before since the present invention is based on a systematized knowledge. Thus, efforts for the development of electrodes can be minimized. The method for fabricating electrodes according to the present invention does not need heat treatment, which makes a great increase in stability of the electrode structure as compared with the conventional method in which heat treatment is essential. Further, in the case of fabricating Ohmic electrodes, conventional methods use doping semiconductors with impurities in high concentrations. In the present invention, however, high concentration doping is unnecessary so that Ohmic electrodes can be fabricated simply and conveniently. In contrast to the conventional methods in which leakage current in the Schottky barrier is used, the method for fabricating electrodes according to the present invention can reduce the Schottky barrier height to zero so that high performance Ohmic electrodes having theoretically no interface resistance that has not been achieved conventionally.

According to the present invention, Schottky barrier heights, that have been almost impossible to control by conventional methods, can be controlled freely by controlling interface level density and selecting work function of metals.

In practicing the present invention, it is only necessary to make the surface of a semiconductor as flat as possible on an atomic level. There are various kinds of known techniques for flattening the surface of a semiconductor on an atomic level and all such techniques can be used in the present invention. Therefore, there is no technical difficulty in practicing the present invention and the present invention can be applied to various metals and semiconductors simply and conveniently.

Hereinafter, the present invention will be described in greater detail by examples with reference to the attached drawings. However, the present invention should not be construed as being limited thereto.

EXAMPLE 1 Confirmation of Ohmic Property (SiC-Ti Structure)

In the instant example, vacuum sublimated n-type 6H-SiC was used as a semiconductor substrate immediately after it was ground. The substrate had a carrier density of about $1 \times 10^{17} \text{ cm}^{-3}$. At this carrier density, usually, the semiconductor was not metallic and it was difficult to produce an Ohmic contact. The substrate was cleaned using methanol and trichloroethylene, and then placed in an electric oven filled with an oxygen gas atmosphere and oxidized at 300 °C for 30 minutes, followed by 800°C for 10 minutes. Thus an oxide film of about 5 nm thick was formed. The substrate was dipped in 5% hydrofluoric acid to remove the oxide film.

On the thus-obtained SiC substrate was deposited titanium (Ti), which is a representative high melting metal and has a low work function. The work function of Ti was 4.4 eV, which is by 0.9 eV lower than Ni, which has conventionally been used as an Ohmic electrode and has a work function of 5.3 eV. The SiC substrate used was not heated previously. The thickness of deposited film was about 500 nm. Deposition was not carried out on the entire surface of the semiconductor but through a metal mask formed with a round hole of 0.30 mm in diameter for subsequent electrical measurements.

Fig. 3 is a graph illustrating current-voltage (I-V) characteristics of the sample taken out of the vacuum apparatus (cf. line 3a). As apparent from Fig. 3, the line 3a is a straight line. Lack of nonlinearity as shown by the straight line 3a in Fig. 3 clearly indicates that the electrode obtained is Ohmic, that is, current is proportional to voltage. The interface resistance of the resulting electrode was $6.7 \times 10^{-2} \Omega \text{ cm}^2$. The electrode made of a SiC material having a low carrier density as low as $2 \times 10^{17} \text{ cm}^{-3}$ had an Ohmic contact which had theoretically the lowest resistance.

An electrode structure was fabricated in the same manner as in EXAMPLE 1 except that no oxidative etching was conducted but only dipping in 5% hydrofluoric acid was performed (COMPARATIVE EXAMPLE 1). The comparative electrode structure showed no Ohmic property but exhibited Schottky property (Fig. 4). In Fig. 4, curves 4a and 4b

show normal and reverse direction leakage currents, respectively.

EXAMPLE 2 Confirmation of Ohmic Property (SiC-Al structure)

Next, an electrode structure was fabricated in the same manner as in EXAMPLE 1 except that instead of Ti was used aluminum (Al), which is a non-transient, low melting metal and belonging to the group (III) of the periodic table. In this case, too, was obtained an Ohmic contact similar to that fabricated in EXAMPLE 1. The work function of Al is 4.3 eV. Fig. 5 shows current-voltage characteristics of the aluminum electrode fabricated under the same conditions as the Ti electrode. Similarly to EXAMPLE 1, a line 5 representing the current-voltage characteristics of the Al electrode showed linearity and the interface resistance was about $1.4 \times 10^{-2} \Omega \text{cm}^2$. The electrode made of a SiC material having a low carrier density as low as $2 \times 10^{17} \text{ cm}^{-3}$ had an Ohmic contact which had theoretically the lowest resistance.

What is common between EXAMPLE 1 and EXAMPLE 2 is that the both metals used have work functions by about 1 eV lower than those of noble metals used as electrode metal for SiC in the conventional methods. The both metals tested here exhibited effects which attain the objects of the present invention.

EXAMPLE 3 Confirmation of Ohmic Property (Si-Al structure)

The instant example is to show that the present invention is applicable to Si substrates and also realize Ohmic contacts. As a semiconductor substrate was used an n-type Si substrate having a carrier density of $7 \times 10^{16} \text{ cm}^{-3}$. The substrate was cleaned using methanol and trichloroethylene, and then placed in an electric oven filled with an oxygen gas atmosphere and oxidized at 300°C for 30 minutes, followed by 800°C for 10 minutes. Thus an oxide film of about 50 nm thick was formed. The substrate was dipped in 5% hydrofluoric acid to remove the oxide film. The substrate thus obtained was dipped in hot water to make the surface of the semiconductor substrate flat on an atomic level. Thereafter, aluminum was deposited on the surface as an electrode metal. Fig. 6 illustrates current-voltage characteristics of the resulting electrode structure. A line 6a, which is a straight line, represents the sample with 5% hydrofluoric acid treatment. A line 6b, which is also a straight line, represents the sample with hot water treatment after 5% hydrofluoric acid treatment. A line 6c, which is also a straight line, represents the sample with 5% hydrofluoric acid treatment followed by hot water treatment. Here, by the term "hot water treatment" is meant a treatment with heated deionized water at a temperature below 100°C. From Fig. 6, it is apparent that the electrode fabricated according to the present invention has an Ohmic contact having a good linearity of current-voltage characteristics (the line 6c). Herebefore, as illustrated in Fig. 1, no metal could provide an Ohmic contact for Si substrates without high concentration doping. In fact, a comparative sample having an Si(111) substrate which did not subjected to high concentration doping and having a carrier density of $7 \times 10^{16} \text{ cm}^{-3}$ (COMPARATIVE EXAMPLE 2) gave a Schottky barrier whose ϕ_{bn} was 0.69 eV after receiving the same 5% hydrofluoric acid treatment as in the instant example (Fig. 7). In Fig. 7, curves 7a and 7b denote current flows in normal and reverse directions, respectively. Comparing the lines 6a to 6c in Fig. 6, it is observed that according as flattening processes are added or flatness increases, current increases and contact resistance decreases. In the instant example (the line 6c in Fig. 6), the doping concentration was $7 \times 10^{16} \text{ cm}^{-3}$, at which the width of the depletion layer is sufficiently thick and no tunneling will occur theoretically. Therefore, the Ohmic property observed in the sample of the instant example is considered to be attributable to a sufficiently decreased Schottky barrier.

EXAMPLE 4 Structural Uniformity of Electrode Structure

A Ti electrode was fabricated in the same manner as in EXAMPLE 1. Fig. 8A is an illustrative view prepared based on an optical micrograph of the surface of the Ti electrode. Fig. 8B is an expanded schematic cross sectional view showing the Ti electrode shown in Fig. 8A. As COMPARATIVE EXAMPLE 3, was prepared an Ni electrode by a conventional heat treatment method. The Ni electrode fabricated by cleaning using methanol and trichloroethylene, the same n-type SiC substrate as used in EXAMPLE 1, depositing Ni thereon by vapor deposition and then heating the substrate at 1,000°C for 60 minutes. Fig. 9A is an illustrative view prepared based on an optical micrograph of the surface of the Ni electrode. Fig. 9B is an expanded schematic cross sectional view showing the Ni electrode shown in Fig. 8A. In Figs. 8A and 9A, reference numeral 11 denotes an SiC substrate, 12 is an outline contour line of the electrode, 13 is an Ni electrode, and 14 is a Ti electrode. The both Ni and Ti electrodes were in the form of a disk of 0.3 mm in diameter. From Figs. 8A, 8B, 9A and 9B, it is apparent that the Ti electrode fabricated on SiC fabricated without heat treatment in accordance with the present invention has a high flatness in surface. The Ni electrode 13 shown in Fig. 9A has a rough surface, clearly lacking structural uniformity. In contrast, in the Ti electrode 14 of the present invention, no region is observed where surface conditions are different, and the area inside a contour line 12 of the electrode 14 is uniform in appearance and highly flat, thus presenting excellent structure for Ohmic structure. The electrode fabricated according to the method of the present invention (Fig. 8B) had a surface with an unevenness (X1) of 5 nm or

less. On the contrary, the electrode fabricated by the conventional method (Fig. 9B) had a surface with an unevenness (X2) of about 200 nm. This clearly indicates that the electrode fabricated by the method of the present invention had a surface flatness much superior to the electrode fabricated by the conventional method.

EXAMPLE 5 Dependence on Atomic Level Flattening Treatment - Epitaxial Growth

The same SiC substrate immediately after grinding as used in EXAMPLE 1 was dipped in boiling water (100°C) for 10 minutes. On the other hand, a sample was prepared by homoepitaxially growing SiC on the same SiC substrate after grinding as used in EXAMPLE 1. The sample was dipped in boiling water (100°C) for 10 minutes. Then, difference in current-voltage characteristics between the epitaxial SiC substrate and the SiC substrate immediately after grinding were examined. In the case of the epitaxial SiC substrate, an expectation will be made that flattening in surface proceeds sufficiently so that the interface level density decreases and as a result, the Schottky barrier height decreased and Ohmic property increases. In fact, the SiC substrate immediately after grinding had an interface resistance of $1.2 \times 10^{-2} \Omega \text{cm}^2$ (the line 3c in Fig. 3) while the epitaxial SiC substrate had an improved interface resistance of $6 \times 10^{-3} \Omega \text{cm}^2$ (the line 3d in Fig. 3). From this it follows that epitaxial growth is effective for flattening on an atomic level the surface of a semiconductor and for decreasing interface level density of the semiconductor.

EXAMPLE 6 Dependence on Atomic Level Flattening Treatment - pH Adjusted Dilute Hydrofluoric Acid Treatment

An oxidized etched substrate having a current-voltage characteristics represented by the line 3a in Fig. 3 as used in EXAMPLE 1 was dipped in a pH adjusted dilute hydrofluoric acid for 10 minutes. Then, a metal was deposited on the surface of the thus obtained substrate. In Fig. 3, the line 3b represents the current-voltage characteristics of the electrode sample. In this case, the dilute hydrofluoric acid was adjusted to pH 10. Comparison of the line 3b with the line 3a shows that the interface resistance is improved to $1.5 \times 10^{-2} \Omega \text{cm}^2$. As demonstrated in the instant example, pH adjusted dilute hydrofluoric acid treatment is also effective in decreasing interface level density.

EXAMPLE 7 Fabrication of a Schottky Electrode Showing Less Leakage

Fig. 10 illustrates current-voltage characteristics of gold (Au) electrode on 6H-SiC(0001) face. Lines 10a, 10b and 10c show normal direction leakage currents and 10a', 10b' and 10c' show reverse direction leakage currents. In the case of SiC surface with usual 5% hydrofluoric acid treatment, the reverse direction leakage current was on the order of 10^{-7} A/cm^2 (line 10a'). When oxidation/etching treatment was conducted, the reverse direction leakage current was decreased to 10^{-19} A/cm^2 or less (line 10b'), thus showing a drastically improvement in leakage characteristics by 12 digits. Furthermore, with additional boiling water treatment, the reverse direction leakage current was further improved by 2 digits to 10^{-21} A/cm^2 (line 10c'). This indicates that oxidation/etching treatment and boiling water treatment which accelerate flattening of the surface of the semiconductor weaken the pinning of the Schottky barrier. To note, in the instant example, the electrode itself was subjected to no heat treatment. Therefore, the instant example clearly shows that high quality Schottky electrode can be fabricated without heat treatment of the electrode.

EXAMPLE 8 Control of Pinning and Schottky Barrier Height

Fig. 11 illustrate Schottky barrier height for various metals deposited on 6H-SiC(0001) face. The horizontal axis indicates work function of the metal. In the case of usual pretreatment with 5% hydrofluoric acid, the Schottky barrier height does not substantially depend on the work function of the metal and S factor which indicates an inclination of the line is about 0.2 (line 11a). Then, atomic level flattening of SiC was conducted by oxidation/etching treatment, $S=0.8$ was obtained which indicates almost pinning free state (line 11b). Further, boiling water treatment gives rise to $S=1.0$, which indicates no pinning is observed (line 11c). Thus, the present invention realized pinning free state for those semiconductors which inherently show pinning. As a result, the Schottky barrier height can be freely changed merely by changing the work function of the metal as illustrated in Fig. 11 clearly. When the same metal is used, change in the process of atomic level flattening of the surface of the semiconductor results in varied Schottky barrier height. Note that for Ti electrodes, Schottky barrier heights were theoretically estimated from contact resistance values.

Fig. 12 illustrates Schottky barrier heights of Schottky electrodes fabricated on 6H-SiC(0001) substrates by the conventional method and by the methods of the examples of the present invention. For strict comparison, conventional electrodes were fabricated on clean surfaces and I-V characteristics values measured at room temperature were used. The data of the conventional electrodes exist in the region (0). Ti, Mo and Au electrodes subjected to oxidation/etching treatment and boiling water treatment according to the present invention are plotted in regions (I), (IV) and (II), respectively. The data show that the present invention made it possible to realize Schottky barrier heights beyond the lower limit (region (I)) and beyond the upper limit (region (II)) that were impossible to achieve by the conventional method.

EP 0 789 388 A2

The Mo electrode plotted in region (IV) gives the same Schottky barrier height as that of the conventional Ti electrode having lower work function. This means that to give a certain Schottky barrier height, those materials that were considered inappropriate in view of pinning action can be used in the method of the present invention.

As described above, Schottky barrier height of semiconductors can be freely controlled according to the present invention.

Table 2 summarizes the results of examples and Comparative examples above.

10

15

20

25

30

35

40

45

50

55

Table 2

	Substrate	Electrode Metal	Treatment	Figure	Interface Resistance ($10^{-2}\Omega\text{cm}^2$)	Reverse Direction Leakage Current (A/cm ²)	Surface Unevenness (nm)
Ex. 1	SiC	Ti	A+B	Fig. 3 Line (a)	6.7		
C.Ex.1	SiC	Ti	B	Fig. 4			
Ex. 2	SiC	Al	A+B	Fig. 5	1.4		
Ex. 3	Si	Al	A+B	Fig. 6 Line (a)			
	Si	Al	B+C	Fig. 6 Line (b)			
	Si	Al	A+B+C	Fig. 6 Line (c)			
C.Ex.2	Si	Al	B	Fig. 7			
Ex. 4	SiC	Ti	A+B	Fig. 8A, Fig. 8B			52
C.Ex.3	SiC	Ni	Cleaning* Heating 1,000°C	Fig. 9A, Fig. 9B			200

EP 0 789 388 A2

The present invention has been described in detail with respect to an embodiment, and it will now be apparent

Table 2 (Continued)

	Electrode			Interface	Reverse	Surface
	Substrate	Metal	Treatment	Resistance	Direction	Unevenness
				($10^{-2}\Omega\text{cm}^2$)	Leakage	(nm)
					Current	
					(A/cm^2)	
Ex. 5	SiC	Ti	A+B+C	Fig. 3	1.2	
	(Bulk)			Line (c)		
	SiC-SiC		A+B+C	Fig. 3	0.6	
	(Epitaxial)	Ti		Line (d)		
Ex. 6	SiC	Ti	A+B'	Fig. 3	1.5	
				Line (b)		
Ex. 7	6H-SiC	Au	A+B	Fig. 10	10^{-19}	
	(0001)					
	6H-SiC	Au	A+B+C	Fig. 10	10^{-21}	
	(0001)					
C.Ex. 4	6H-SiC	Au	B	Fig. 10	10^{-7}	
	(0001)					
Ex. 8	6H-SiC	Ti,	A+B+C	Fig. 11		
	(0001)	Mo,				
		Ni				

*: with methanol and trichloroethylene

EP 0 789 388 A2

from the foregoing to those skilled in the art that changes and modifications may be made without departing from the invention in its broader aspects, and it is the intention, therefore, in the appended claims to cover all such changes and modifications as fall within the true spirit of the invention.

Claims

1. A method of fabricating a layer of an electrode metal on a surface of a semiconductor, characterized by comprising the step of:
decreasing a surface states density of said surface of said semiconductor.
2. A method of fabricating a layer of an electrode metal on a surface of a semiconductor, characterized by comprising the step of:
controlling a Schottky barrier height of a rectifying Schottky electrode formed on said surface of said semiconductor.
3. The method as claimed in claim 2, characterized in that said control of the Schottky barrier height of said Schottky electrode is carried out by controlling flatness of an electrode metal/semiconductor interface.
4. The method as claimed in claim 2, characterized in that said control of the Schottky barrier height of said Schottky electrode is carried out by controlling a step density on an atomic level of an electrode metal/semiconductor interface.
5. The method as claimed in claim 2, characterized in that said control of the Schottky barrier height of said Schottky electrode is carried out by controlling selecting a work function of the metal.
6. The method as claimed in claim 2, characterized in that said control of the Schottky barrier height of said Schottky electrode is carried out by controlling the Schottky barrier height of the Schottky electrode under conditions without giving thermal hysteresis.
7. A method of fabricating a layer of an electrode metal on a surface of a semiconductor, characterized by comprising the step of:
fabricating a Schottky electrode from a metal having a high work function, and fabricating an Ohmic electrode from a metal having a low work function, for an n-type semiconductor, or
fabricating a Schottky electrode from a metal having a low work function and an Ohmic electrode from a metal having a high work function, for a p-type semiconductor.
8. The method as claimed in any one of claims 2 to 7, characterized by further comprising the step of heating.
9. A method of fabricating an Ohmic electrode, characterized by comprising the step of: forming flat electrode metal/semiconductor interface on an atomic level.
10. A method of fabricating an Ohmic electrode, characterized by comprising the step of: forming an electrode metal/semiconductor interface having a low step density on an atomic level.
11. A method of fabricating an electrode, characterized by comprising the step of:
fabricating an Ohmic electrode as claimed in any one of claim 1 to 10 in a highly integrated electronic device.
12. The method as claimed in any one of claims 1 to 11, characterized in that said semiconductor is made of a semiconductor selected from the group consisting of Si and SiC.
13. The method as claimed in any one of claims 1 to 12, characterized in that said electrode metal is selected from the group consisting of Al, Au, Mo and Ti.
14. A Schottky electrode structure provided on a semiconductor characterized by having an interface portion which is flat on an atomic level.

15. A Schottky electrode structure provided on a semiconductor characterized by having a Schottky barrier height which is impossible to realize by conventional method.
- 5 16. An Ohmic electrode structure provided on a semiconductor characterized by containing no high concentration impurity.
17. An Ohmic electrode structure characterized by having a Schottky barrier height which is substantially zero.
- 10 18. The electrode structure as claimed in any one of claims 14 to 17, characterized in that said semiconductor is made of a semiconductor selected from the group consisting of Si and SiC.
19. The electrode structure as claimed in any one of claims 14 to 17, characterized in that said electrode metal is selected from the group consisting of Al, Au, Mo and Ti.
- 15 20. A method of fabricating an electrode, characterized by comprising the step of:
oxidizing a surface layer of silicon or silicon carbide and removing the resulting oxide film.
- 20 21. The method as claimed in claim 20, characterized in that said oxidizing of the silicon or silicon carbide is carried out by heating the silicon or silicon carbide in an oxidative gaseous atmosphere.
22. The method as claimed in claim 20, characterized in that said removing the oxide film is carried out by reacting the oxide film with a reducing liquid or gas.
- 25 23. The method as claimed in any one of claims 20 to 22, characterized in that said silicon or silicon carbide is n-type silicon or n-type silicon carbide, and wherein said electrode metal is a metal having a work function lower than that of noble metals.
- 30 24. The method as claimed in any one of claims 20 to 22, characterized in that said silicon carbide is p-type silicon carbide, and wherein said electrode material is a noble metal or a metal having a work function of a level substantially equal to that of noble metals.
25. The method as claimed in claim 23, characterized in that said electrode material is titanium (Ti).
- 35 26. The method as claimed in claim 23, characterized in that said electrode material is aluminum (Al).
27. A method of producing a Schottky diode or other semiconductor device having electrodes which includes fabricating electrodes by any method or combination of methods as claimed in any of claims 9 to 13 or 20 to 26 or which includes fabricating electrodes by patterning or fabricating in a pattern a layer of electrode metal produced by any method claimed in claims 1 to 8.
- 40 28. A semiconductor device having at least two metal electrodes formed on a semiconductor surface and wherein the flatness of the semiconductor surface is different at each interface with said two respective metal electrodes.
- 45 29. A device according to claim 28 wherein the electrodes are ohmic and Schottky electrodes respectively, and the interfaces therewith are atomically flat and other than atomically flat respectively.

50

55

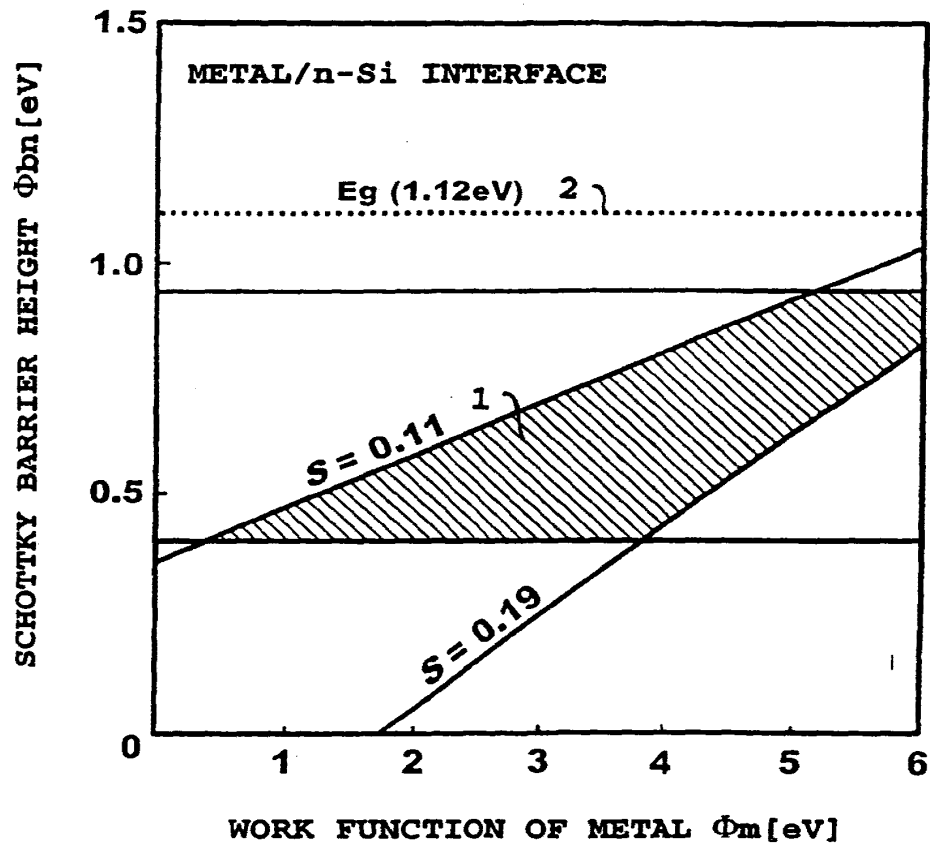


FIG. 1
(PRIOR ART)

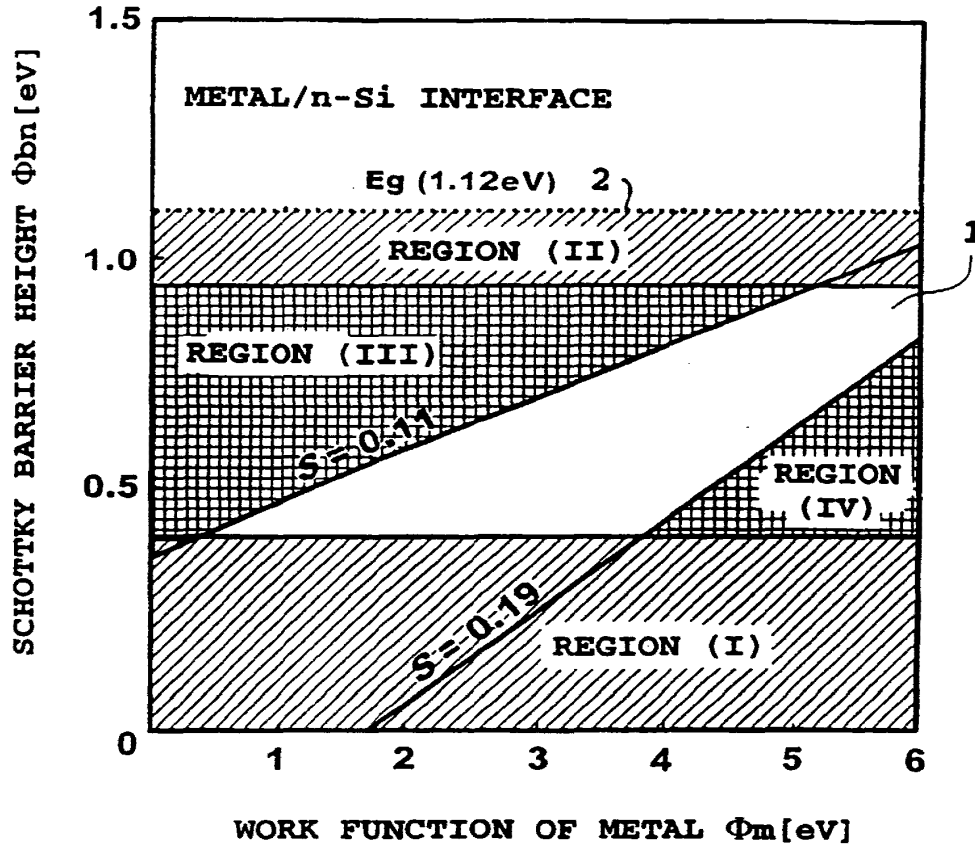


FIG. 2

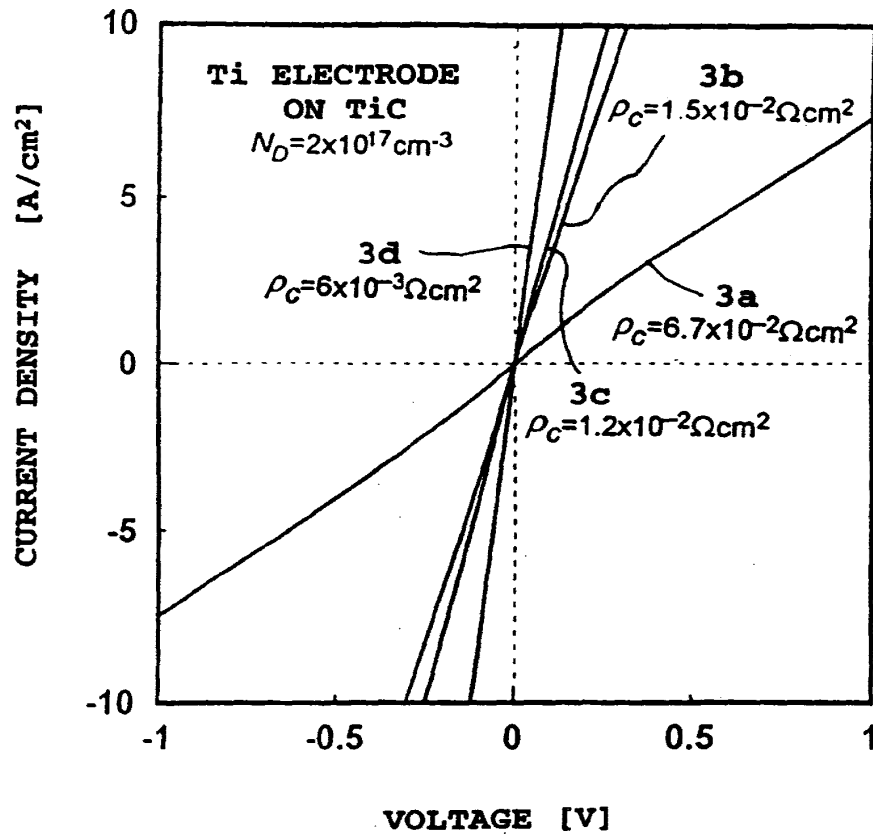


FIG. 3

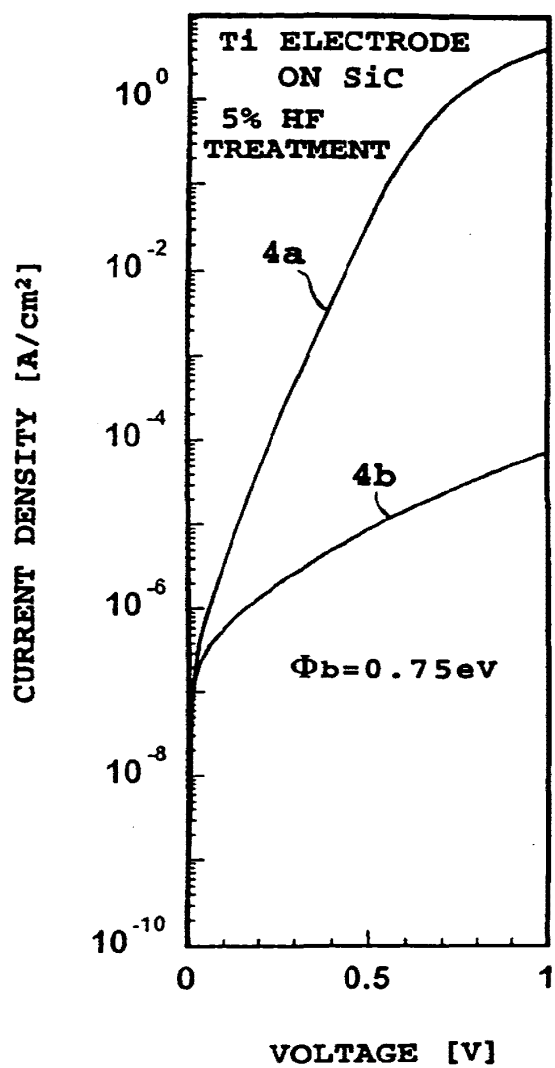


FIG. 4

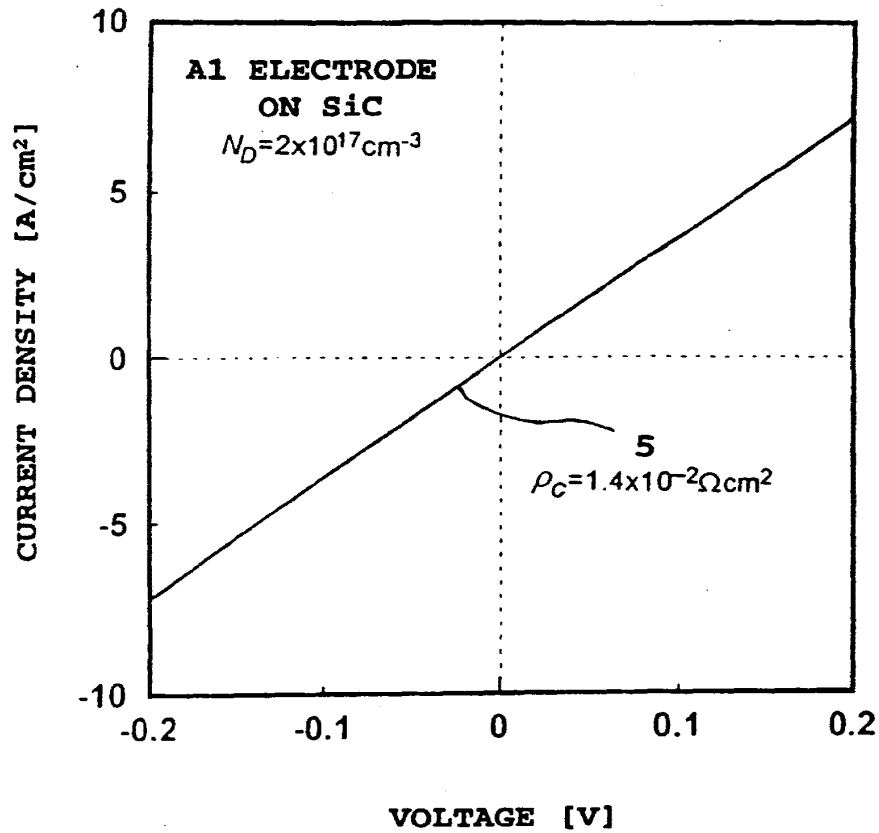
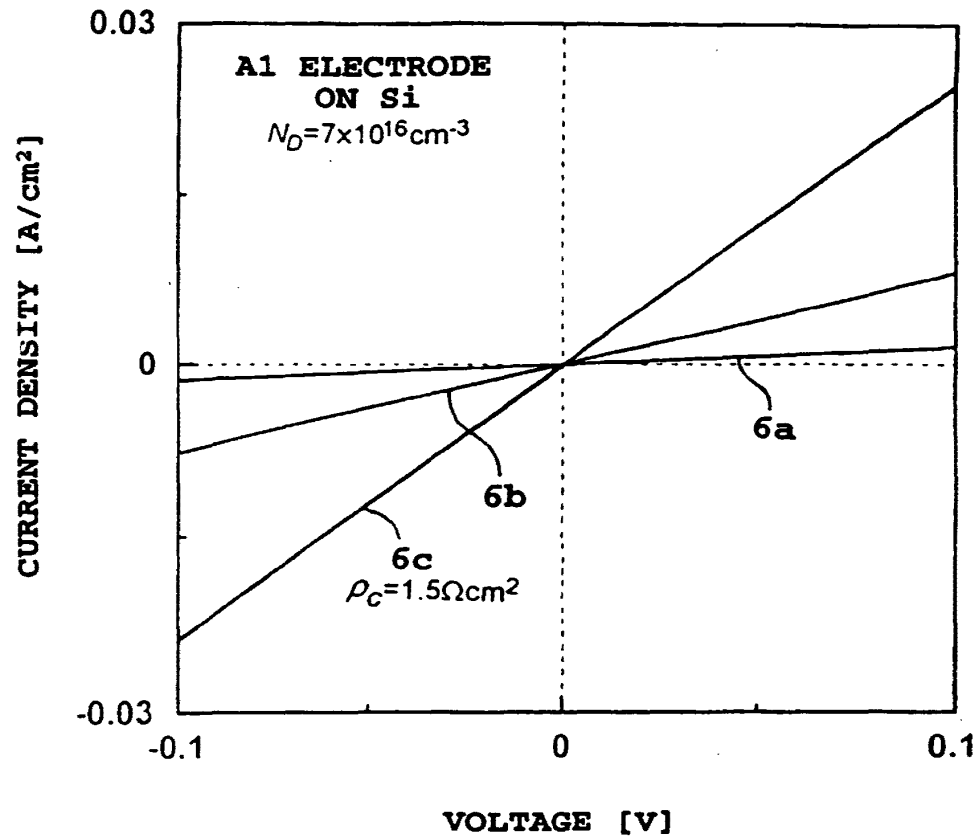


FIG. 5

**FIG. 6**

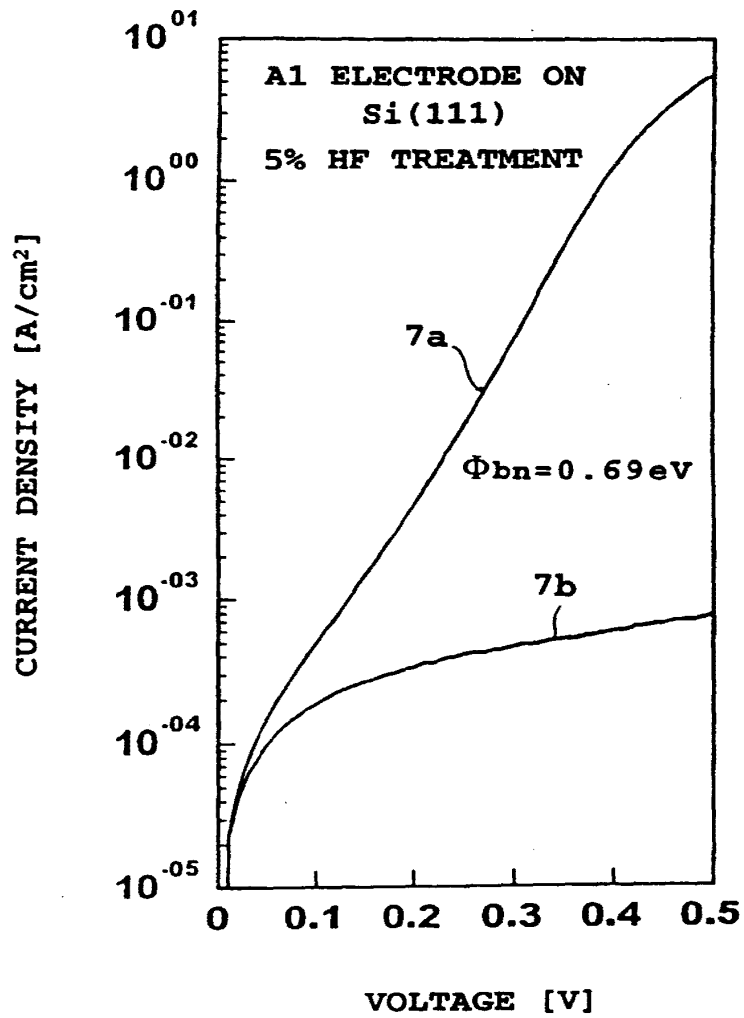


FIG. 7

FIG. 8A

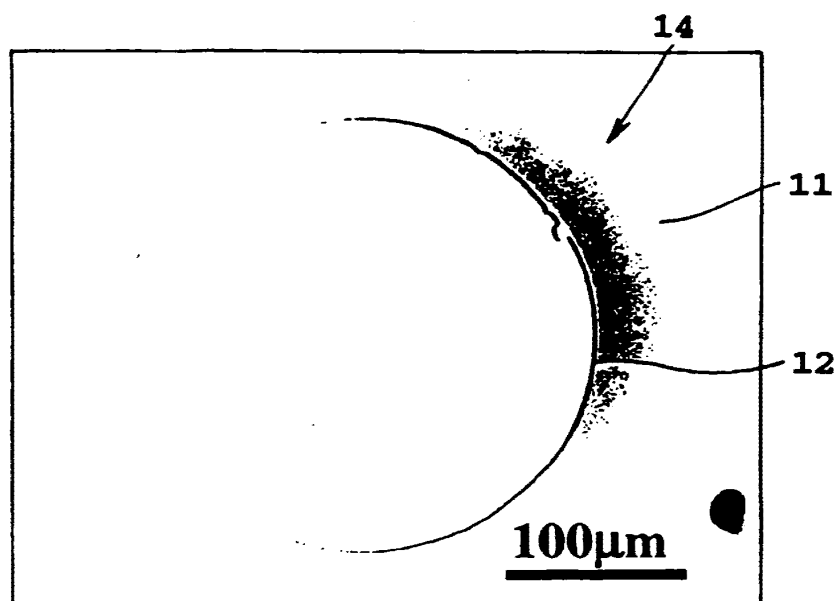


FIG. 8B

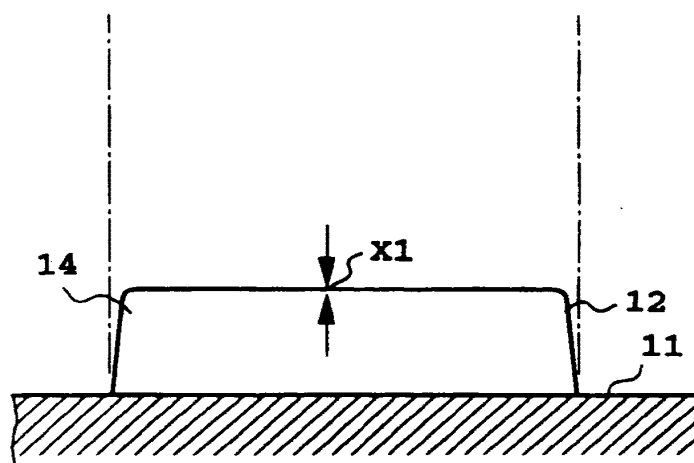


FIG. 9A

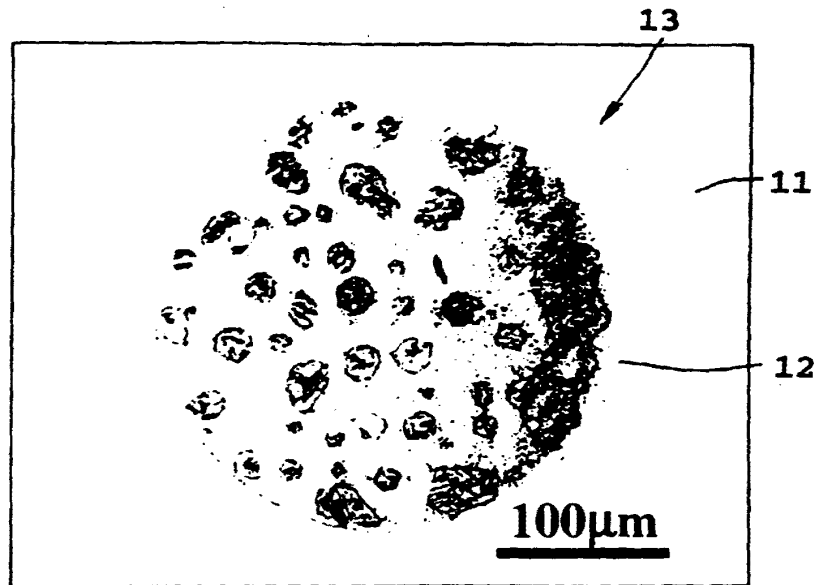
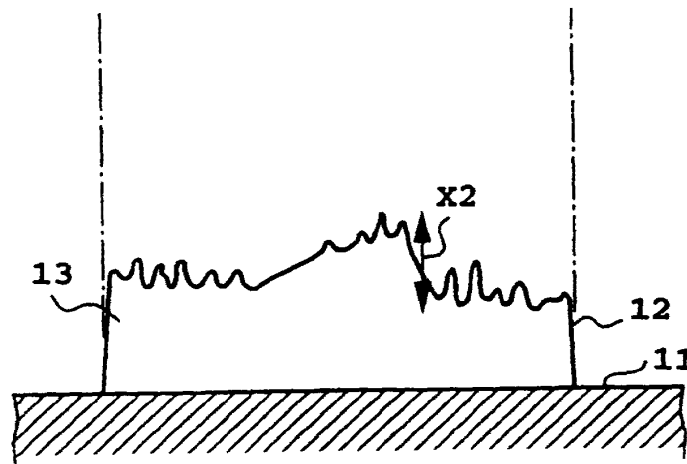
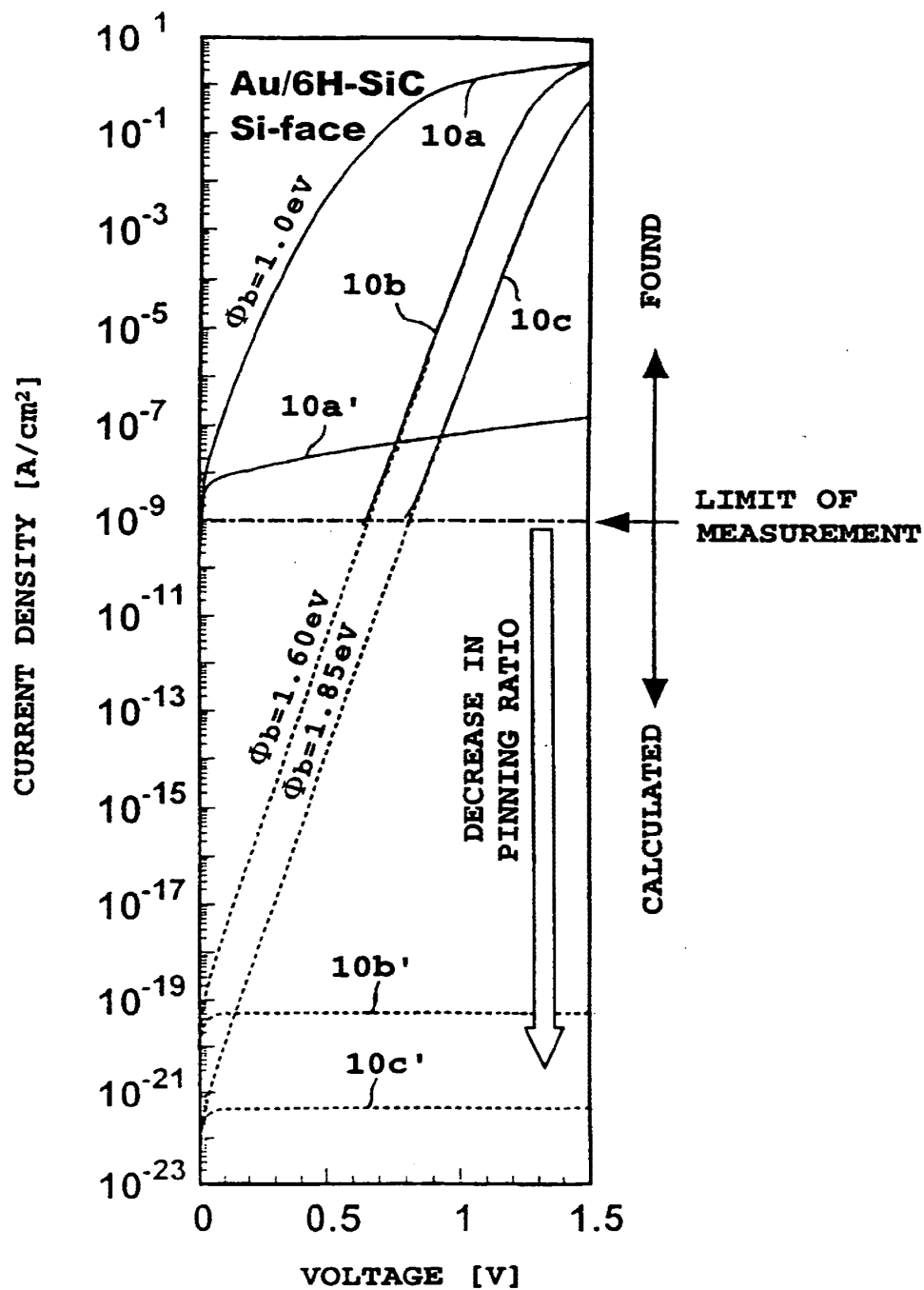


FIG. 9B



**FIG. 10**

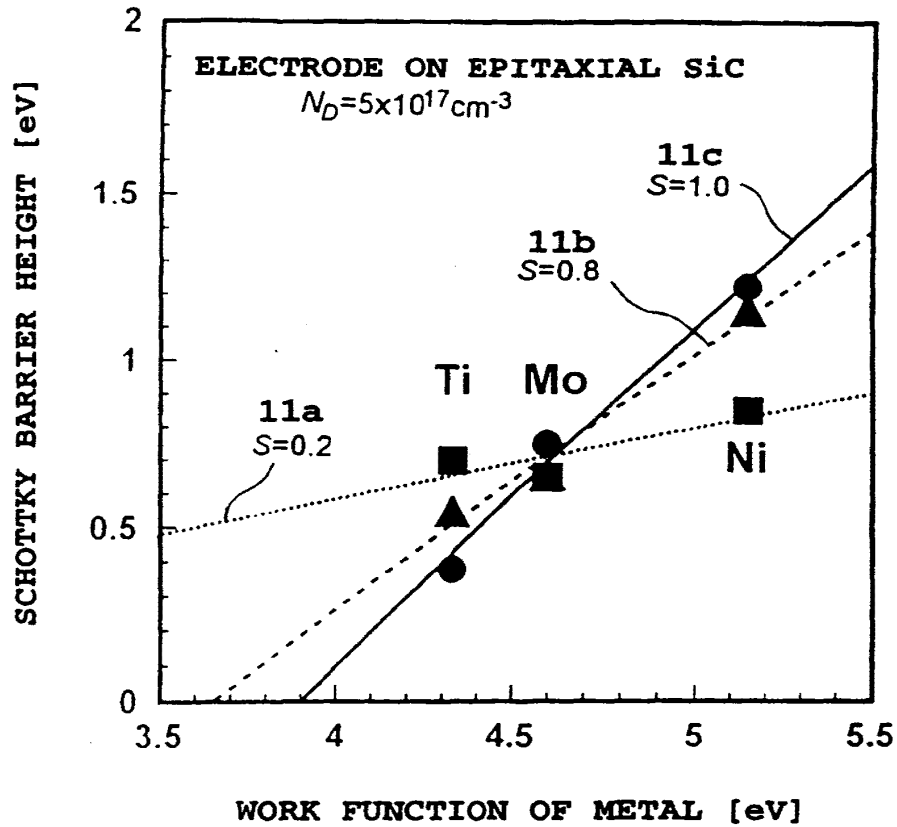


FIG. 11

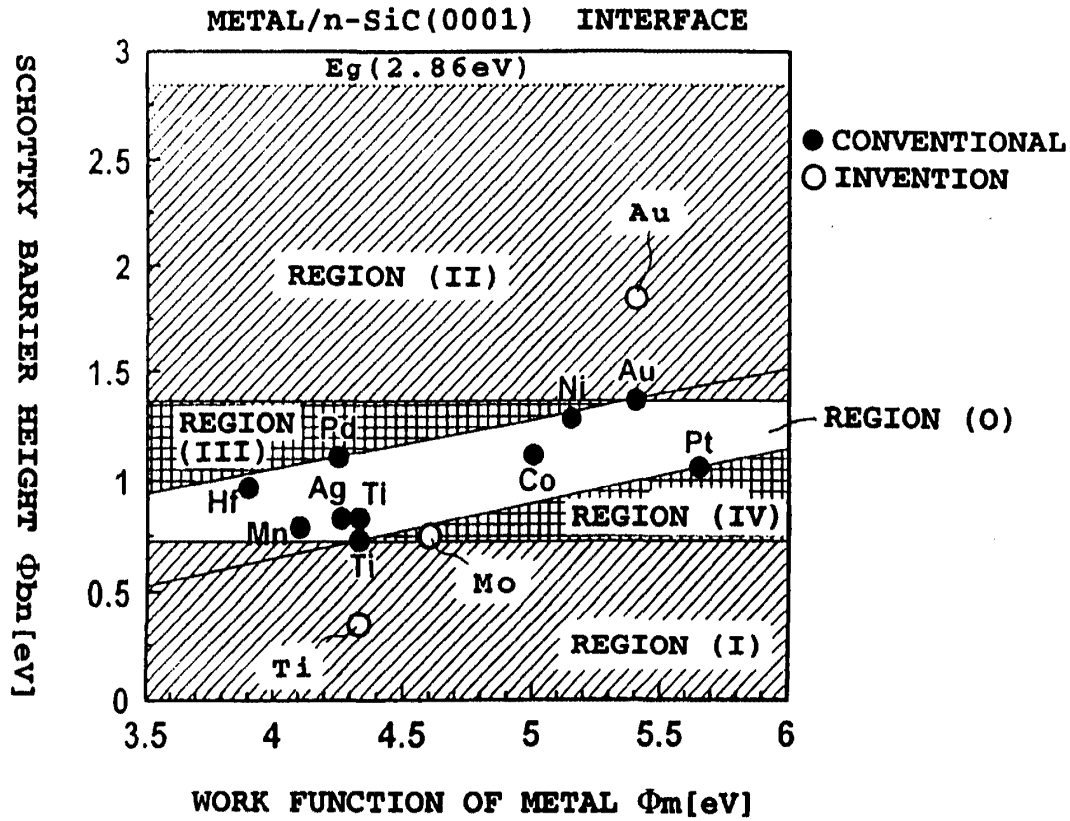
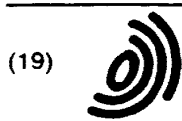


FIG.12

EP 0 789 388 A2



Eur päisch Pat ntamt
European Patent Office
Offic eur péén d s brevets



(11) EP 0 789 388 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
16.09.1998 Bulletin 1998/38

(51) Int Cl.⁶: H01L 21/285, H01L 21/04

(43) Date of publication A2:
13.08.1997 Bulletin 1997/33

(21) Application number: 96306139.5

(22) Date of filing: 22.08.1996

(84) Designated Contracting States:
DE FR GB

(30) Priority: 25.08.1995 JP 216935/95
25.03.1996 JP 68018/96

(71) Applicant: AGENCY OF INDUSTRIAL SCIENCE
AND TECHNOLOGY
Chiyoda-ku Tokyo (JP)

(72) Inventors:
• Hara, Shiro
Tsukuba-shi, Ibaraki (JP)

• Kajimura, Koji
Tsukuba-shi, Ibaraki (JP)
• Okushi, Hideyo
Tsukuba-shi, Ibaraki (JP)
• Teraji, Tokuyuki
Tsukuba-shi, Ibaraki (JP)

(74) Representative: Beresford, Keith Denis Lewis
BERESFORD & Co.
2-5 Warwick Court
High Holborn
London WC1R 5DJ (GB)

(54) Structure and fabrication method for schottky and ohmic electrodes onto semiconductor devices

(57) A novel electrode structure for Schottky electrodes and Ohmic electrodes and novel methods of fabricating electrodes by freely controlling electric characteristics of electrodes on semiconductors. Interface states density of a semiconductor (11) after deposition of an electrode metal (13, 14) is decreased by flattening the surface of the semiconductor on an atomic level to freely control the Schottky barrier height. The method can realize an ideal Ohmic electrode having a Schottky barrier height of substantially zero. The Schottky barrier height is varied freely by decreasing the interface level density and selecting work function of the electrode metal. The method can provide stable Schottky and Ohmic electrodes (13, 14) without need of heat treatment. Further, the method can provide Ohmic electrodes without high concentration doping.

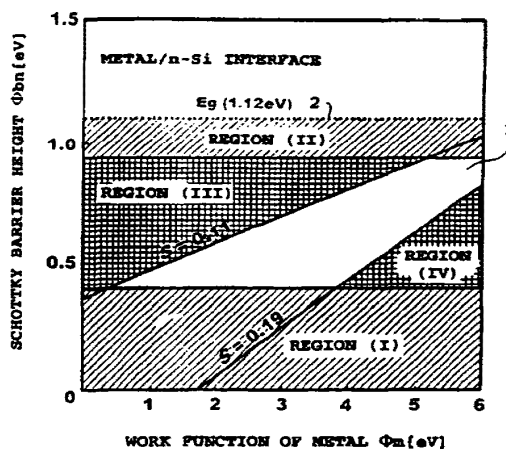


FIG. 2

EP 0 789 388 A3



European Patent
Office

PARTIAL EUROPEAN SEARCH REPORT

Application Number

which under Rule 45 of the European Patent Convention EP 96 30 6139 shall be considered, for the purposes of subsequent proceedings, as the European search report

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	S. M. SZE: "Physics or Semiconductor Devices" 1981, JOHN WILEY & SONS, NEW YORK XP002068071 * page 245 - page 311 *	2,5,7,8,17	H01L21/285 H01L21/04
X	US 4 301 592 A (LIN HUNG CHANG) 24 November 1981 * column 2, line 63 - column 3, line 32; figures 2,3 *	1	
X	EP 0 111 364 A (PHILIPS NV) 20 June 1984 * abstract; figure 2 *	2,7	
X	ADEGBOYEGA G A ET AL: "SCHOTTKY CONTACT BARRIER HEIGHT ENHANCEMENT ON P-TYPE SILICON BY WET CHEMICAL ETCHING" APPLIED PHYSICS A. SOLIDS AND SURFACES, vol. A48, no. 4, 1 April 1989, pages 391-395. XP000112320 * the whole document *	20,22	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H01L
INCOMPLETE SEARCH The Search Division considers that the present application, or one or more of its claims, does/do not comply with the EPC to such an extent that a meaningful search into the state of the art cannot be carried out, or can only be carried out partially, for these claims. Claims searched completely: Claims searched incompletely: Claims not searched: Reason for the limitation of the search: see sheet C			
Place of search THE HAGUE		Date of completion of the search 15 June 1998	Examiner Königstein, C
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

EPO FORM 1500a & 1500b (Part 1)



European Patent
Office

INCOMPLETE SEARCH
SHEET C

Application Number
EP 96 30 6139

Claim(s) searched completely:
1-5,7-14,16-29

Claim(s) searched incompletely:
6,15

Reason for the limitation of the search:

The subclaim 6 describes the fabrication of a Schottky electrode characterized in that the Schottky barrier height is controlled 'under conditions without giving thermal hysteresis'.

The claim 15 describes a Schottky electrode characterised by having a Schottky barrier height 'which is impossible to realize by conventional method'.

The wording used in these two claims is not clear (Art. 84 EPC).

In claim 6, it is not clear what (effect) gives the thermal hysteresis and how this can be achieved.

In claim 15, it is not clear what is meant with 'conventional method'.



European Patent
Office

PARTIAL EUROPEAN SEARCH REPORT

Application Number
EP 96 30 6139

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
X	CHANDRIKA NARAYAN: "TUNING OF THE SCHOTTKY BARRIER HEIGHT USING BI-METALLIC LAYERED STRUCTURES" APPLIED PHYSICS LETTERS, vol. 59, no. 20, 11 November 1991, pages 2541-2542, XP000330120 * the whole document *	2,5	
X	PATENT ABSTRACTS OF JAPAN vol. 095, no. 003, 28 April 1995 & JP 06 333892 A (FUJI ELECTRIC CORP RES & DEV LTD), 2 December 1994, * abstract *	3	
A	US 5 087 322 A (LILLIENFELD DAVID ET AL) 11 February 1992 * the whole document *	29	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
A	EP 0 452 661 A (IBM) 23 October 1991 * the whole document *		
A	US 4 060 820 A (PUCEL ROBERT A ET AL) 29 November 1977 * the whole document *		
P.X	TERAJI T ET AL: "Ohmic contacts to n-type 6H-SiC without post-annealing" III-NITRIDE, SiC AND DIAMOND MATERIALS FOR ELECTRONIC DEVICES. SYMPOSIUM, III-NITRIDE, SiC AND DIAMOND MATERIALS FOR ELECTRONIC DEVICES. SYMPOSIUM, SAN FRANCISCO, CA, USA, 8-12 APRIL 1996, 1996, PITTSBURGH, PA, USA, MATER. RES. SOC., USA, pages 149-154, XP002068069 * the whole document *	1-4, 9-14, 16-20, 22,23, 25,27,29	

	-/--		

EPO FORM 1503 03-02 (P04C10)



European Patent
Office

PARTIAL EUROPEAN SEARCH REPORT

Application Number

EP 96 30 6139

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
P.X	HARA S ET AL: "Pinning-controlled metal/semiconductor interfaces" THIRD INTERNATIONAL CONFERENCE ON INTELLIGENT MATERIALS. THIRD EUROPEAN CONFERENCE ON SMART STRUCTURES AND MATERIALS, LYON, FRANCE. 3-5 JUNE 1996, vol. 2779, ISSN 0277-786X, PROCEEDINGS OF THE SPIE - THE INTERNATIONAL SOCIETY FOR OPTICAL ENGINEERING, 1996, SPIE-INT. SOC. OPT. ENG, USA, pages 802-806, XP002068070 • the whole document *	1,2,7	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)

EPO FORM 1803 (3.92) (P01:10)



UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450
www.uspto.gov

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD SEVENTH FLOOR
LOS ANGELES, CA 90025

COPY MAILED

FEB 06 2004

OFFICE OF PETITIONS

ON PETITION

In re Application of
Daniel E. Grupp
Application No. 10/217,758
Filed: August 12, 2002
Attorney Docket No. 3771P003

This is a decision on the petition, filed January 26, 2004, under 37 CFR 1.313(c)(2) to withdraw the above-identified application from issue after payment of the issue fee.

The petition is **GRANTED**.

The above-identified application is withdrawn from issue for consideration of a submission under 37 CFR 1.114 (request for continued examination). See 37 CFR 1.313(c)(2).

Petitioner is advised that the issue fee paid on January 12, 2004 in the above-identified application cannot be refunded. If, however, the above-identified application is again allowed, petitioner may request that it be applied towards the issue fee required by the new Notice of Allowance.¹

Telephone inquiries should be directed to Irvin Dingle at (703) 306-5684.

After receipt of the file in the Office of Petitions, the file will be forwarded to Technology Center AU 2814 for processing of the request for continued examination under 37 CFR 1.114 and for consideration of the concurrently filed Information Disclosure Statement.

Irvin Dingle
Petitions Examiner
Office of Petitions
Office of the Deputy Commissioner
for Patent Examination Policy

¹ The request to apply the issue fee to the new Notice may be satisfied by completing and returning the new Issue Fee Transmittal Form PTOL-85(b), which includes the following language thereon: "Commissioner for Patents is requested to apply the Issue Fee and Publication Fee (if any) or re-apply any previously paid issue fee to the application identified above." Petitioner is advised that, whether a fee is indicated as being due or not, the Issue Fee Transmittal Form **must** be completed and timely submitted to avoid abandonment. Note the language in bold text on the first page of the Notice of Allowance and Fee(s) Due (PTOL-85).



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/217,758	08/12/2002	Daniel E. Grupp	3771P003	1710
8791	7590	02/11/2005	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD SEVENTH FLOOR LOS ANGELES, CA 90025-1030			NGO, NGAN V	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 02/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

Office Action Summary	Application No.	Applicant(s)	
	10/217,758	GRUPP ET AL.	
	Examiner	Art Unit	
	Ngan Ngo	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-61 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-26 and 31-61 is/are rejected.
- 7) ☒ Claim(s) 27-30 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☐ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) ☐ Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>0104</u> . | 6) ☐ Other: _____ |

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-26 and 31- 61 rejected under 35 U.S.C. 102(b) as being anticipated by Schroen et al.

Schroen et al discloses an electrical device comprising a metal (16), a silicon based semiconductor (11) having a Fermi level, and an interface layer (15) configured to depin the Fermi level of the semiconductor in which the electrical device has a specific contact resistance of less than $1000 \text{ ohm-}\mu\text{m}^2$. Note lines 21-25 of column 2, lines 55-59 of column 2, and lines 60-63 of column 5 of Schroen et al.

In re claims 2 and 3, the interface layer in Schroen is made of an oxide.

In re claim 5, Schroen shows a separation layer (12) in figure 2.

In re claims 10 and 11, no patentable weight is given to "fabricated by heating...".

A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17(footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a

product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear.

In re claim 19, the step of passivation of the surface of the semiconductor is shown by oxide layer 12 in Schroen.

In re claim 46, the device in Schroen inherently has a workfunction approximately equal to a conduction band of the semiconductor if the semiconductor is of n-type semiconductor material or a workfunction approximately equal to a valence band of the semiconductor if the semiconductor is of p-type semiconductor material.

Claims 27-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication should be directed to Examiner Ngan Ngo at telephone number (571) 272-1711. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Application/Control Number: 10/217,758
Art Unit: 2818

Page 4

Handwritten signature of Ngan Van Ngo, consisting of a stylized 'N' followed by a checkmark and another stylized 'N'.

Ngan Van Ngo
Primary Examiner

Ngan Ngo

February 4, 2005



Substitute for form 1449A/PTO		Complete if Known			
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	10/217,758		
		Filing Date	August 12, 2002		
		First Named Inventor	Daniel E. Grupp		
		Art Unit	2814		
		Examiner Name	Ngo, Ngan V.		
Sheet	1	of	2	Attorney Docket Number	3771P003

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.†	Document Number Number - Kind Code* (if known)	Publication Date or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
MF		US-3,983,264	09-28-2076	Schroen et al.	
MF		US-4,056,642	11-01-2077	Saxena et al.	
MF		US-5,021,365	06-04-1991	Kirchner et al.	
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No.†	Foreign Patent Document Country Code* - Number* - Kind Code* (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
MF		EP 0 295 490	05-31-2088	Alan B. Fowler, et al.	
MF		EP 0 789 388	08-22-1996	Shiro Hara, et al.	

Examiner Signature		Date Considered	2-4-05
--------------------	--	-----------------	--------

*Examiner. Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

†Applicant's unique citation designation number (optional). *See Kind Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. †Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). *For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. *Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. *Applicant is to place a check mark here if English language Translation is attached.

Based on PTO/SB/08A (08-03) as modified by Blakely, Solokoff, Taylor & Zafman (w/r) 08/11/2003.

Send To: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Complete if Known

Application Number	10/217,758
Filing Date	August 12, 2002
First Named Inventor	Daniel E. Grupp
Art Unit	2814
Examiner Name	Ngo, Ngan V.
Attorney Docket Number	3771P003

Sheet 2 of 2

NON PATENT LITERATURE DOCUMENTS

[illegible]

**Examiner
Signature**

Date _____

Considered

2-4-55

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

*Applicant's unique citation designation number. *Applicant is to place a check mark here if English language Translation is attached.

Based on PTO/SB/08B (08-03) as modified by Blakely, Solokoff, Taylor & Zafman (wtr) 08/11/2003.
Send To: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Ngan Ngo

2814

[illegible]

Class	Subclass	Date	Examiner
257	cell y	8-27-03	nm
	subclass		
	above		

[illegible]

Index of Claims 	Application/Control No.		Applicant(s)/Patent under Reexamination	
	10/217,758		GRUPP ET AL.	
	Examiner		Art Unit	
	Ngan Ngo		2818	

√	Rejected
=	Allowed

—	(Through numeral) Cancelled
÷	Restricted

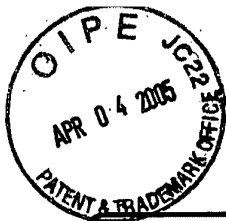
N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claim		Date											
Final	Original												
	2												
	4												
	5												
	8												
	1	✓											
	2												
	3												
	4												
	5												
	6												
	7												
	8												
	9												
	10												
	11												
	12												
	13												
	14												
	15												
	16												
	17												
	18												
	19												
	20												
	21												
	22												
	23												
	24												
	25												
	26	✓											
	27	0											
	28	0											
	29	0											
	30	0											
	31	✓											
	32												
	33												
	34												
	35												
	36												
	37												
	38												
	39												
	40												
	41												
	42												
	43												
	44												
	45												
	46												
	47												
	48												
	49												
	50	✓											

Claim		Date											
Final	Original												
	2												
	4												
	5												
	51	✓											
	52												
	53												
	54												
	55												
	56												
	57												
	58												
	59												
	60												
	61	✓											
	62												
	63												
	64												
	65												
	66												
	67												
	68												
	69												
	70												
	71												
	72												
	73												
	74												
	75												
	76												
	77												
	78												
	79												
	80												
	81												
	82												
	83												
	84												
	85												
	86												
	87												
	88												
	89												
	90												
	91												
	92												
	93												
	94												
	95												
	96												
	97												
	98												
	99												
	100												

Claim		Date											
Final	Original												
	101												
	102												
	103												
	104												
	105												
	106												
	107												
	108												
	109												
	110												
	111												
	112												
	113												
	114												
	115												
	116												
	117												
	118												
	119												
	120												
	121												
	122												
	123												
	124												
	125												
	126												
	127												
	128												
	129												
	130												
	131												
	132												
	133												
	134												
	135												
	136												
	137												
	138												
	139												
	140												
	141												
	142												
	143												
	144												
	145												
	146												
	147												
	148												
	149												
	150												



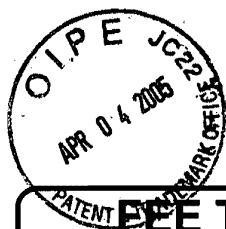
TRANSMITTAL FORM (to be used for all correspondence after initial filing)		Application No.	10/217,758
		Filing Date	August 12, 2002
		First Named Inventor	Daniel E. Grupp
		Art Unit	2814
		Examiner Name	Ngo, Ngan V.
Total Number of Pages in This Submission	15	Attorney Docket Number	3771P003

ENCLOSURES (check all that apply)		
☒ Fee Transmittal Form ☒ Fee Attached ☒ Amendment / Response ☐ After Final ☐ Affidavits/declaration(s) ☐ Extension of Time Request ☐ Express Abandonment Request ☐ Information Disclosure Statement ☐ PTO/SB/08 ☐ Certified Copy of Priority Document(s) ☐ Response to Missing Parts/Incomplete Application ☐ Basic Filing Fee ☐ Declaration/POA ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53	☐ Drawing(s) ☐ Licensing-related Papers ☐ Petition ☐ Petition to Convert a Provisional Application ☐ Power of Attorney, Revocation Change of Correspondence Address ☐ Terminal Disclaimer ☐ Request for Refund ☐ CD, Number of CD(s)	☐ After Allowance Communication to Group ☐ Appeal Communication to Board of Appeals and Interferences ☐ Appeal Communication to Group (Appeal Notice, Brief, Reply Brief) ☐ Proprietary Information ☐ Status Letter ☐ Other Enclosure(s) (please identify below):
Remarks		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual name	Tarek N. Fahmi, Reg. No. 41,402 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	March 23, 2005

CERTIFICATE OF MAILING/TRANSMISSION			
I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.			
Typed or printed name	Patricia A. Balero		
Signature		Date	March 23, 2005

Based on PTO/SB/21 (04-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wtr) 06/04/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450



FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☒ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT (\$)

300.00

Complete if Known

Application Number 10/217,758
Filing Date August 12, 2002
First Named Inventor Daniel E. Grupp
Examiner Name Ngo, Ngan V.
Art Unit 2814
Attorney Docket No. 3771P003

METHOD OF PAYMENT (check all that apply)

☒ Check ☐ Credit card ☐ Money Order ☐ None ☐ Other (please identify):
☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, except for the filing fee
☒ Charge any additional fee(s) or underpayment of fee(s) ☒ Credit any overpayments
under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20.

FEE CALCULATION

1. EXTRA CLAIM FEES

	Extra Claims	Fee from below	Fee Paid
Total Claims	69	61*	8
Independent Claims	9	8*	1
Multiple Dependent			

Large Entity	Small Entity	Fee Description
Fee Code	Fee Code	Fee (\$)
1202 50	2202 25	Claims in excess of 20
1201 200	2201 100	Independent claims in excess of 3
1203 360	2203 180	Multiple Dependent claim, if not paid
1204 300	2204 150	**Reissue independent claims over original patent
1205 300	2205 150	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (1) (\$)

300.00

*or number previously paid, if greater. For Reissues, see below

2. ADDITIONAL FEES

Large Entity	Small Entity	Fee Description
Fee Code	Fee Code	Fee (\$)
1051 130	2051 65	Surcharge - late filing fee or oath
1052 50	2052 25	Surcharge - late provisional filing fee or cover sheet.
2053 130	2053 130	Non-English specification
1251 120	2251 60	Extension for reply within first month
1252 450	2252 225	Extension for reply within second month
1253 1,020	2253 510	Extension for reply within third month
1254 1,590	2254 795	Extension for reply within fourth month
1255 2,160	2255 1,080	Extension for reply within fifth month
1401 500	2401 250	Notice of Appeal
1402 500	2402 250	Filing a brief in support of an appeal
1403 1,000	2403 500	Request for oral hearing
1451 1,510	2451 1,510	Petition to institute a public use proceeding
1460 130	2460 130	Petitions to the Commissioner
1807 50	1807 50	Processing fee under 37 CFR 1.17(q)
1806 180	1806 180	Submission of Information Disclosure Stmt
1809 790	1809 395	Filing a submission after final rejection (37 CFR § 1.129(a))
1810 790	2810 395	For each additional invention to be examined (37 CFR § 1.129(b))

Other fee (specify)

SUBTOTAL (2)

(\$)

Fee Paid

SUBMITTED BY

Name (Print/Type)

Tarek N. Fahmy

Registration No.
(Attorney/Agent)

41,402

Complete (if applicable)

Telephone

(408) 947-8200

Signature

Date

03/23/05

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (w/r) 12/15/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450



2818
/CW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/217,758

Applicant: Grupp, Daniel E. et al.

Filed: 08/12/2002

Art unit: 2818

Examiner: Ngo, Ngan V.

Docket No.: 3771P003

Customer No.: 08791

Confirmation No.: 1710

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

on March 23, 2005
Date of Deposit

Patricia A. Balero
Name of Person Mailing Correspondence

[Signature] 3/23/05
Signature Date

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450.

AMENDMENT

Sir:

In response to the Office action of February 11, 2005, please amend the above-identified application as follow:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 12 of this paper.

04/05/2005 GWORDF1 00000012 10217758

01 FC:2201 100.00 OP
02 FC:2202 200.00 OP

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of Claims:

1. (Amended) An electrical device, comprising:
 - a metal;
 - a silicon-based semiconductor ~~having a Fermi level~~; and
 - an interface layer of less than 1 nm thickness in a vicinity disposed between and in contact with both the metal and the semiconductor and configured to ~~depin the~~ a Fermi level of the semiconductor metal,wherein the electrical device has a specific contact resistance of less than or equal to approximately $1000\ \Omega - \mu m^2$.
2. (Original) The electrical device of claim 1 wherein the interface layer includes a passivating material.
3. (Original) The electrical device of claim 2 wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of silicon.
4. (Amended) The electrical device of claim 3 wherein the interface layer consists essentially of a monolayer ~~configured to depin the Fermi level of the semiconductor~~.

5. (Original) The electrical device of claim 2 wherein the interface layer further includes a separation layer.
6. (Original) The electrical device of claim 1 wherein the specific contact resistance is less than or equal to approximately $100 \Omega - \mu m^2$.
7. (Original) The electrical device of claim 1 wherein the specific contact resistance is less than or equal to approximately $50 \Omega - \mu m^2$.
8. (Original) The electrical device of claim 1 wherein the specific contact resistance is less than or equal to approximately $10 \Omega - \mu m^2$.
9. (Original) The electrical device of claim 1 wherein the specific contact resistance is less than or equal to approximately $1 \Omega - \mu m^2$.
10. (Original) The electrical device of claim 1 wherein the interface layer comprises a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material.
11. (Original) The electrical device of claim 10 wherein the nitrogenous material comprises at least one of ammonia (NH₃), nitrogen (N₂) or unbound nitrogen (N).
12. (Amended) An electrical device, comprising a metal – interface layer – Si-based semiconductor junction in which the interface layer is less than 1 nm thick in a vicinity of the junction and includes a passivating material and the electrical device has a specific contact resistance of less than approximately $1000 \Omega - \mu m^2$.

13. (Original) The electrical device of claim 12 wherein the specific contact resistance is less than or equal to approximately $100 \Omega - \mu m^2$.

14. (Original) The electrical device of claim 12 wherein the specific contact resistance is less than or equal to approximately $50 \Omega - \mu m^2$.

15. (Original) The electrical device of claim 12 wherein the specific contact resistance is less than or equal to approximately $10 \Omega - \mu m^2$.

16. (Original) The electrical device of claim 1 wherein the specific contact resistance is less than or equal to approximately $1 \Omega - \mu m^2$.

17. (Original) The electrical device of claim 12, wherein the passivating material comprises one or more of a nitride, an oxide, an oxynitride a hydride, a fluoride and/or an arsenide of silicon.

18. (Original) The electrical device of claim 17, wherein the interface layer comprises a passivation layer and a separation layer.

19. (Amended) A method, comprising depinning a Fermi level of a ~~silicon-based semiconductor~~ semiconductor in an electrical junction with a silicon-based semiconductor through the use of an interface layer disposed between a surface of the semiconductor and ~~the~~ a conductor, wherein the interface layer (i) has a thickness of less than 1 nm in a vicinity of the junction yet sufficient to reduce effects of metal-induced gap states in the semiconductor while providing the junction with a specific contact resistance of less than approximately $1000 \Omega - \mu m^2$, and (ii) passivates the surface of the semiconductor.

20. (Original) The method of claim 19 wherein the specific contact resistance is less than or equal to approximately $100 \Omega - \mu m^2$.

21. (Original) The method of claim 19 wherein the specific contact resistance is less than or equal to approximately $50 \Omega - \mu m^2$.

22. (Original) The method of claim 19 wherein the specific contact resistance is less than or equal to approximately $10 \Omega - \mu m^2$.

23. (Original) The method of claim 19 wherein the specific contact resistance is less than or equal to approximately $1 \Omega - \mu m^2$.

24. (Original) The method of claim 19 wherein the interface layer has a thickness sufficient to provide a specific contact resistance of the electrical junction of less than or equal to approximately $1 \Omega - \mu m^2$.

25. (Original) The method of claim 19 wherein the interface layer includes a passivating material selected from the list comprising: an arsenide, a hydride, a fluoride, an oxide, an oxynitride and a nitride of silicon.

26. (Original) The method of claim 25 wherein the interface layer consists essentially of a monolayer.

27. (Original) The method of claim 19 wherein the interface layer is grown on the semiconductor surface at temperatures above approximately 300 °C.

28. (Original) The method of claim 27 wherein the interface layer is grown in the presence of a nitrogenous material.

29. (Original) The method of claim 28 wherein the nitrogenous material comprises one of ammonia (NH₃), nitrogen (N₂), or unbound nitrogen (N).

30. (Original) The method of claim 19 wherein the interface layer includes a passivation layer grown by immersion of the semiconductor in a liquid containing hydrogen and fluorine ions.

31. (Amended) An electrical device, comprising a junction between a Si-based semiconductor and a conductor separated from the semiconductor by an interface layer having a thickness of less than 1 nm in a vicinity of the junction yet that allows a Fermi level of the conductor to align with a conduction band of the semiconductor, wherein the electrical device has a specific contact resistance less than approximately $1000 \Omega - \mu m^2$.

32. (Original) The electrical device of claim 31 wherein the specific contact resistance is less than or equal to approximately $100 \Omega - \mu m^2$.

33. (Original) The electrical device of claim 31 wherein the specific contact resistance is less than or equal to approximately $50 \Omega - \mu m^2$.

34. (Original) The electrical device of claim 31 wherein the specific contact resistance is less than or equal to approximately $10 \Omega - \mu m^2$.

35. (Original) The electrical device of claim 31 wherein the specific contact resistance is less than or equal to approximately $1 \Omega - \mu m^2$.

36. (Amended) An electrical device, comprising a junction between a Si-based semiconductor and a conductor separated from the semiconductor by an interface layer having a thickness of less than 1 nm in a vicinity of the junction yet that allows a Fermi level of the conductor to

align with a valence band of the semiconductor, wherein the electrical device has a specific contact resistance less than approximately $1000 \Omega - \mu m^2$.

37. (Original) The electrical device of claim 36 wherein the specific contact resistance is less than or equal to approximately $100 \Omega - \mu m^2$.

38. (Original) The electrical device of claim 36 wherein the specific contact resistance is less than or equal to approximately $50 \Omega - \mu m^2$.

39. (Original) The electrical device of claim 36 wherein the specific contact resistance is less than or equal to approximately $10 \Omega - \mu m^2$.

40. (Original) The electrical device of claim 36 wherein the specific contact resistance is less than or equal to approximately $1 \Omega - \mu m^2$.

41. (Amended) An electrical device, comprising a junction between a Si-based semiconductor and a conductor separated from the semiconductor by an interface layer having a thickness of less than 1 nm in a vicinity of the junction yet that allows a Fermi level of the semiconductor to be independent of a Fermi level of the conductor, wherein the electrical device has a specific contact resistance less than approximately $1000 \Omega - \mu m^2$.

42. (Original) The electrical device of claim 41 wherein the specific contact resistance is less than or equal to approximately $100 \Omega - \mu m^2$.

43. (Original) The electrical device of claim 41 wherein the specific contact resistance is less than or equal to approximately $50 \Omega - \mu m^2$.

44. (Original) The electrical device of claim 41 wherein the specific contact resistance is less than or equal to approximately $10 \Omega - \mu m^2$.

45. (Original) The electrical device of claim 41 wherein the specific contact resistance is less than or equal to approximately $1 \Omega - \mu m^2$.

46. (Amended) An electrical device, comprising:

a silicon-based semiconductor of either *n*-type or *p*-type semiconductor material;

a metal having a workfunction approximately equal to a conduction band of the semiconductor if the semiconductor is of *n*-type semiconductor material or having a workfunction approximately equal to a valence band of the semiconductor if the semiconductor is of *p*-type semiconductor material; and

an interface layer of less than 1 nm thickness in a vicinity disposed between and in contact with both the semiconductor and the metal, wherein the electrical device has a specific contact resistance of less than or approximately equal to $1000 \Omega - \mu m^2$.

47. (Original) The electrical device of claim 46 wherein the interface layer includes a passivating material.

48. (Original) The electrical device of claim 47 wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of silicon.

49. (Amended) The electrical device of claim 48 wherein the interface layer consists essentially of a monolayer ~~configured to depin a Fermi level of the semiconductor.~~

50. (Original) The electrical device of claim 47 wherein the interface layer further includes a separation layer.

51. (Original) The electrical device of claim 46 wherein the specific contact resistance is less than or equal to approximately $100 \Omega - \mu m^2$.

52. (Original) The electrical device of claim 46 wherein the specific contact resistance is less than or equal to approximately $50 \Omega - \mu m^2$.

53. (Original) The electrical device of claim 46 wherein the specific contact resistance is less than or equal to approximately $10 \Omega - \mu m^2$.

54. (Original) The electrical device of claim 46 wherein the specific contact resistance is less than or equal to approximately $1 \Omega - \mu m^2$.

55. (Original) The electrical device of claim 46 wherein the interface layer comprises a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material.

56. (Original) The electrical device of claim 55 wherein the nitrogenous material comprises at least one of ammonia (NH₃), nitrogen (N₂) or unbound nitrogen (N).

57. (Amended) An electrical device, comprising:

a silicon-based semiconductor of either *n*-type or *p*-type semiconductor material;

a metal having a workfunction near or substantially equal to a conduction band edge of the semiconductor if the semiconductor is of *p*-type semiconductor material, or having a workfunction near or substantially equal to a valence band edge of the semiconductor if the semiconductor is of *n*-type semiconductor material; and

an interface layer of less than 1 nm thickness in a vicinity disposed between and in contact with both the semiconductor and the metal and configured to depin a Fermi level of the ~~semiconductor~~ metal.

58. (Original) The electrical device of claim 57 wherein the interface layer includes a passivating material.

59. (Original) The electrical device of claim 58 wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of silicon.

60. (Amended) The electrical device of claim 57 wherein the interface layer consists essentially of a monolayer ~~configured to depin a Fermi level of the semiconductor~~.

61. (Original) The electrical device of claim 57 wherein the interface layer further includes a separation layer.

62. (New) An electrical device, comprising a junction between a Si-based semiconductor and a conductor separated from the semiconductor by an interface layer having a thickness sufficient to depin a Fermi level of the conductor in a vicinity of the junction yet thin enough to provide the junction with a specific contact resistance that is generally dependent on the workfunction of the conductor.

63. (New) The electrical device of claim 62 wherein the interface layer includes a passivating material.

64. (New) The electrical device of claim 63 wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of silicon.

65. (New) The electrical device of claim 63 wherein the interface layer consists essentially of a monolayer.

66. (New) The electrical device of claim 63 wherein the interface layer further includes a separation layer.

67. (New) The electrical device of claim 62 wherein the interface layer comprises a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material.

68. (New) The electrical device of claim 67 wherein the nitrogenous material comprises one of: ammonia (NH₃), nitrogen (N₂), or unbound nitrogen (N).

69. (New) The electrical device of claim 62 wherein the interface layer includes a passivation layer grown by immersion of the semiconductor in a liquid containing hydrogen and fluorine ions.

REMARKS

Reconsideration of this application, as amended, is respectfully requested. The claims have been amended to clarify that the interface layer has a thickness of less than 1 nm in the region of the junction. Support for these amendments may be found in the specification as originally filed, for example at paragraph 59. In addition, the phrase “Fermi level of the semiconductor” has been revised to read “Fermi level of the metal/conductor” in claims 1, 19 and 57 to clarify the nature of the physics as explained at paragraph 70 of the specification as originally filed. No new matter is added by these amendments.

The present claims are patentable over Schroen, US 3,983,264, which fails to teach or suggest the use of such an interface layer. In fact, Schroen specifically indicates that the use of such an interface layer is undesirable:

The adherent film of nonconductive material must have a thickness in the range of about 10 – 100 Angstroms. A film of less than 10 Å thick is unsatisfactory due to lack of uniformity or operating stability, i.e., the likelihood of discontinuities and lifetest failures.

Schroen at col. 3, ll. 1 – 5.

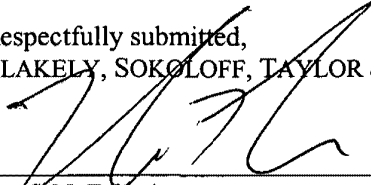
To anticipate a claim, the reference must teach every element of the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Schroen fails to meet this test because the reference fails to describe the use of an interface layer less than 1 nm thick as claimed.

New claim 62 recites an electrical device in which the interface layer has a thickness sufficient to depin a Fermi level of the conductor yet thin enough to provide the junction with a specific contact resistance that is *generally dependent on the workfunction of the conductor*. Support for this claim may be found, for example at paragraph 70 et seq. of the specification as originally filed. This claim is patentable over Schroen, which specifically indicates that the junction has a thickness sufficiently thick so that resistance is *independent of the metal workfunction*. See, e.g., Schroen at col. 5, ll. 19 – 24 (‘the metallurgical compatibility constraint is removed.’). Because these junctions are thus substantially different, the new claim is patentably distinct from the structure disclosed by Schroen.

New claims 63 – 69 depend from claim 62 and include subject matter previously recited in other claims. Hence, these claims are supported by the specification as originally filed and are patentable over Schroen for at least the same reasons as claim 62.

For at least the foregoing reasons, all of the presently pending claims are patentable over Schroen. If there are any additional fees associated with this communication, please charge Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP



Dated: March 23, 2005

Tarek N. Fahmi
Reg. No. 41,402

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025-1026
(408) 947-8200

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2001

Application or Docket Number

10/217758

3771p003

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	61	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	61 - minus 20 =	* 41
INDEPENDENT CLAIMS	8 - minus 3 =	* 5
MULTIPLE DEPENDENT CLAIM PRESENT ☐		

* If the difference in column 1 is less than zero, enter "0" in column 2

4-4-05 **CLAIMS AS AMENDED - PART II**

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	* 69	Minus ** 61	= 8
Independent	* 9	Minus *** 8	= 1
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SMALL ENTITY TYPE ☐

OR OTHER THAN SMALL ENTITY

RATE	FEE
BASIC FEE	370.00
X\$ 9=	
X42=	
+140=	
TOTAL	

RATE	FEE
BASIC FEE	740.00
X\$18=	738.00
X84=	420.00
+280=	
TOTAL	1158.00

SMALL ENTITY

OR OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE
~~25.~~	200.
~~50.~~	
~~100.~~	100.
~~150.~~	
~~180.~~	
+140=	
TOTAL	300.

RATE	ADDITIONAL FEE
~~30.~~	400.
~~50.~~	
~~100.~~	200.
~~150.~~	
~~180.~~	
+280=	
TOTAL	

RATE	ADDITIONAL FEE
X\$ 9=	
X42=	
+140=	
TOTAL	

RATE	ADDITIONAL FEE
X\$18=	
X84=	
+280=	
TOTAL	

RATE	ADDITIONAL FEE
X\$ 9=	
X42=	
+140=	
TOTAL	

RATE	ADDITIONAL FEE
X\$18=	
X84=	
+280=	
TOTAL	

Index of Claims



Application/Control No.

10/217,758

Examiner

Ngan Ngo

Applicant(s)/Patent under Reexamination

GRUPP ET AL.

Art Unit

2818

✓	Rejected
=	Allowed

-	(Through numeral) Cancelled
+	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claim		Date	
Final	Original		
	2		
	4		
	05		
	1	✓	
	2		
	3		
	4		
	5		
	6		
	7		
	8		
	9		
	10		
	11		
	12		
	13		
	14		
	15		
	16		
	17		
	18		
	19		
	20		
	21		
	22		
	23		
	24		
	25		
	26	✓	
	27	0	
	28	0	
	29	0	
	30	0	
	31	0	
	32		
	33		
	34		
	35		
	36		
	37		
	38		
	39		
	40		
	41		
	42		
	43		
	44		
	45		
	46		
	47		
	48		
	49		
	50	✓	

Claim		Date	
Final	Original		
	2		
	4		
	05		
	51	✓	
	52		
	53		
	54		
	55		
	56		
	57		
	58		
	59		
	60		
	61	✓	
	62		
	63		
	64		
	65		
	66		
	67		
	68		
	69		
	70		
	71		
	72		
	73		
	74		
	75		
	76		
	77		
	78		
	79		
	80		
	81		
	82		
	83		
	84		
	85		
	86		
	87		
	88		
	89		
	90		
	91		
	92		
	93		
	94		
	95		
	96		
	97		
	98		
	99		
	100		

Claim		Date	
Final	Original		
	101		
	102		
	103		
	104		
	105		
	106		
	107		
	108		
	109		
	110		
	111		
	112		
	113		
	114		
	115		
	116		
	117		
	118		
	119		
	120		
	121		
	122		
	123		
	124		
	125		
	126		
	127		
	128		
	129		
	130		
	131		
	132		
	133		
	134		
	135		
	136		
	137		
	138		
	139		
	140		
	141		
	142		
	143		
	144		
	145		
	146		
	147		
	148		
	149		
	150		

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	("3983264").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/26 16:40
L3	0	l1 and depin	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/26 16:40
L4	6	depin and fermi and workfunction	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/26 16:50
L5	5	depin and fermi and work adj function	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/26 16:50



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

08791 7590 06/02/2005

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER

NGO, NGAN V

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 06/02/2005

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/217,758	08/12/2002	Daniel E. Grupp	3771P003	1710

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$70	\$0	\$70	09/02/2005

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. **PROSECUTION ON THE MERITS IS CLOSED.** THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Complete and send this form, together with applicable fee(s), to: **Mail**

**Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (703) 746-4000**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

08791 7590 06/02/2005

**BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030**

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (703) 746-4000, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/217,758	08/12/2002	Daniel E. Grupp	3771P003	1710

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$70	\$0	\$70	09/02/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGO, NGAN V	2818	257-030000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

- ☐ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above. NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____
 Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/217,758	08/12/2002	Daniel E. Grupp	3771P003	1710
08791	7590	06/02/2005	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD SEVENTH FLOOR LOS ANGELES, CA 90025-1030			NGO, NGAN V	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 06/02/2005

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 242 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 242 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571) 272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

Notice of Allowability	Application No.	Applicant(s)	
	10/217,758	GRUPP ET AL.	
	Examiner	Art Unit	
	Ngan Ngo	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed 4-4-05.
2. ☒ The allowed claim(s) is/are 1-69.
3. ☒ The drawings filed on 12 August 2002 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|---|
| <ol style="list-style-type: none"> 1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date _____ 4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | <ol style="list-style-type: none"> 5. ☐ Notice of Informal Patent Application (PTO-152) 6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____ 7. ☐ Examiner's Amendment/Comment 8. ☐ Examiner's Statement of Reasons for Allowance 9. ☐ Other _____ |
|---|---|



**Ngan Van Ngo
Primary Examiner**

Substitute for Form 1449A/PTO (Modified)

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet

6

Complete if Known

Application Number 10/217,758
 Filing Date August 12, 2002
 First Named Inventor: Daniel E. Grupp
 Group Art Unit Not Yet Assigned
 Examiner Name Not Yet Assigned
 Attorney Docket Number 3771P003

U.S. PATENT DOCUMENTS

Exam. Initial ¹	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Code ²	Kind (If known)			
		3,590,471		Lepselter et al.	7/6/71	
		3,708,360		Wakefield, Jr., et al.	1/2/73	
		4,300,152		Lepselter	11/10/81	
		4,485,550		Koenekke et al.	12/4/84	
		5,399,206		de Lyon	3/21/95	
		5,612,567		Baliga	3/18/97	
		5,663,584		Welch	9/2/97	
		5,801,398		Hebiguchi	9/1/98	
		5,888,891		Gould	3/30/99	
		5,939,763		Hao, et al.	8/17/99	
		6,037,605		Yoshimura	3/14/00	
		6,096,590		Chan et al.	8/1/00	
		6,150,286		Sun, et al.	11/21/00	
		6,198,113	B1	Grupp	3/6/01	
		6,207,976	B1	Takahashi et al.	3/27/01	
		6,261,932	B1	Hulfachor	7/17/01	
		6,291,866		Wallace, et al.	9/18/01	
		6,291,867		Wallace, et al.	9/18/01	
		6,303,479	B1	Snyder	10/16/01	
		5,596,218	B1	Soleimani, et al.	01-21-1997	
		5,578,848		Kwong, et al.	11-26-1996	

FOREIGN PATENT DOCUMENTS

Exam. Initial ¹	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ³
		Office ⁴	Number ⁴	Kind Code ⁵ (If known)				

Examiner Signature

Mjm ✓ Mj

Date Considered

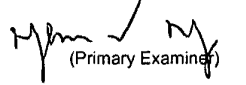
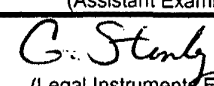
8-27-03

¹EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

²Unique citation designation number. ³See attached Kinds of U.S. Patent Documents. ⁴Enter Office that issued the document, by the two-letter code (WIPO Standard S.3). ⁵For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. ⁶Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.18 if possible. ⁷Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Issue Classification 	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/217,758	GRUPP ET AL.	
	Examiner	Art Unit	
	Ngan Ngo	2818	

ISSUE CLASSIFICATION									
ORIGINAL		CLASS	CROSS REFERENCE(S)						
CLASS	SUBCLASS		SUBCLASS (ONE SUBCLASS PER BLOCK)						
257	30	257	485						
INTERNATIONAL CLASSIFICATION									
H01L	39/00								
H01L	31/108								
	/								
	/								
	/								
(Assistant Examiner) (Date)		NGÂN V. NGÔ PRIMARY EXAMINER GROUP 2800 			Total Claims Allowed: 69				
 5-27-05 (Legal Instruments Examiner) (Date)					O.G. Print Claim(s) 62		O.G. Print Fig. 7D		
					5-26-05				
					(Primary Examiner) (Date)				

☒ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47	
Final	Original	Final	Original	Final	Original	Final	Original
	1		31		61		121
	2		32		62		122
	3		33		63		123
	4		34		64		124
	5		35		65		125
	6		36		66		126
	7		37		67		127
	8		38		68		128
	9		39		69		129
	10		40		70		130
	11		41		71		131
	12		42		72		132
	13		43		73		133
	14		44		74		134
	15		45		75		135
	16		46		76		136
	17		47		77		137
	18		48		78		138
	19		49		79		139
	20		50		80		140
	21		51		81		141
	22		52		82		142
	23		53		83		143
	24		54		84		144
	25		55		85		145
	26		56		86		146
	27		57		87		147
	28		58		88		148
	29		59		89		149
	30		60		90		150
							151
							152
							153
							154
							155
							156
							157
							158
							159
							160
							161
							162
							163
							164
							165
							166
							167
							168
							169
							170
							171
							172
							173
							174
							175
							176
							177
							178
							179
							180
							181
							182
							183
							184
							185
							186
							187
							188
							189
							190
							191
							192
							193
							194
							195
							196
							197
							198
							199
							200
							201
							202
							203
							204
							205
							206
							207
							208
							209
							210

Search Notes



Application No.

10/217,758

Examiner

Ngan Ngo

Applicant(s)

GRUPP ET AL.

Art Unit

2814

SEARCHED

Class	Subclass	Date	Examiner
257	30,31 32,35	8-27-03	WW
	56,62		
	65,471		
	472		
	473		
	475		
	485		
update all	above	2-4-05	WW
update all	above	5-26-05	WW

INTERFERENCE SEARCHED

Class	Subclass	Date	Examiner
257	all of subclass	8-27-03	WW
	above		
update all	above	5-26-05	WW

SEARCH NOTES (INCLUDING SEARCH STRATEGY)

	DATE	EXMR
BRS Search using EAST	8-27-03	WW
BRS Search using EAST	5-26-05	WW



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov



Bib Data Sheet

CONFIRMATION NO. 1710

SERIAL NUMBER 10/217,758	FILING DATE 08/12/2002 RULE	CLASS 257	GROUP ART UNIT 2818	ATTORNEY DOCKET NO. 3771P003
-----------------------------	---------------------------------------	--------------	------------------------	------------------------------------

APPLICANTS

Daniel E. Grupp, Palo Alto, CA;
 Daniel J. Connelly, Redwood City, CA;

** CONTINUING DATA *****

** FOREIGN APPLICATIONS *****

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
 ** 10/21/2002

Foreign Priority claimed 35 USC 119 (a-d) conditions met	☐ yes ☐ yes ☒ no ☒ no ☐ Met after Allowance	STATE OR COUNTRY CA	SHEETS DRAWING 6	TOTAL CLAIMS 61	INDEPENDENT CLAIMS 8
---	--	---------------------------	------------------------	-----------------------	----------------------------

Verified and Acknowledged

Examiner's Signature *[Signature]* Initials *[Initials]*

ADDRESS
 08791
 BLAKELY SOKOLOFF TAYLOR & ZAFMAN
 12400 WILSHIRE BOULEVARD
 SEVENTH FLOOR
 LOS ANGELES , CA
 90025-1030

TITLE
 METHOD FOR DEPINNING THE FERMIL LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION
 AND DEVICES INCORPORATING SUCH JUNCTIONS

FILING FEE RECEIVED	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees
		☐ 1.16 Fees (Filing)
		☐ 1.17 Fees (Processing Ext. of time)

2498	☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit _____
------	--

Complete and send this form, together with applicable fee(s), to: **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (703) 746-4000

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

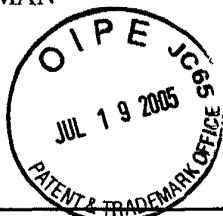
CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

08791 7590 06/02/2005

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

07/20/2005 HDEMESS2 00000081 022666 10217758

01 FC:1501 70.00 DA 1330.00 OP



Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (703) 746-4000, on the date indicated below.

Geneva Walls (Depositor's name)
Geneva Walls (Signature)
 July 14, 2005 (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/217,758	08/12/2002	Daniel E. Grupp	3771P003	1710

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$70	\$0	\$70	09/02/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGO, NGAN V	2818	257-030000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
 BEAKELY SOKOLOFF TAYLOR & ZAFMAN LLP.
 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR FOREIGN COUNTRY)
 Pacific Palisades, CA

Adjustment date: 07/20/2005 HDEMESS2
 01 FC:1501 022666 10217758
 -1330.00 OP

ACORN TECHNOLOGIES, INC.

Pacific Palisades, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

☐ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 02-2666 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above. NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date July 14, 2005

Typed or printed name Tarek N. Fahmi

Registration No. 41,402

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	4	Application No.	10/217,758
		Filing Date	August 12, 2002
		First Named Inventor	Daniel E. Grupp
		Art Unit	2814
		Examiner Name	Ngo, Ngan V.
		Attorney Docket Number	3771P003

ENCLOSURES (check all that apply)

☐ Fee Transmittal Form ☐ Fee Attached ☐ Amendment / Response ☐ After Final ☐ Affidavits/declaration(s) ☐ Extension of Time Request ☐ Express Abandonment Request ☐ Information Disclosure Statement ☐ PTO/SB/08 ☐ Certified Copy of Priority Document(s) ☐ Response to Missing Parts/Incomplete Application ☐ Basic Filing Fee ☐ Declaration/POA ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53	☐ Drawing(s) ☐ Licensing-related Papers ☐ Petition ☐ Petition to Convert a Provisional Application ☐ Power of Attorney, Revocation Change of Correspondence Address ☐ Terminal Disclaimer ☐ Request for Refund ☐ CD, Number of CD(s)	☒ After Allowance Communication to Group ☐ Appeal Communication to Board of Appeals and Interferences ☐ Appeal Communication to Group (Appeal Notice, Brief, Reply Brief) ☐ Proprietary Information ☐ Status Letter ☒ Other Enclosure(s) (please identify below): Request That The Issue Fee Paid On January 12, 2004 Be Applied Towards The New Notice Of Allowance; Postcard.
Remarks		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Tarek N. Fahmy, Reg. No. 41,402 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	July 14, 2005

CERTIFICATE OF MAILING/TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Typed or printed name	Geneva Walls		Date	July 14, 2005
Signature				

Based on PTO/SB/21 (04-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 05/04/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/217,758

Applicant: Grupp, Daniel E. et al.

Filed: 08/12/2002

Art unit: 2818

Examiner: Ngo, Ngan V.

Docket No.: 3771P003

Customer No.: 08791



Confirmation No.: 1710

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

on July 14, 2005
Date of Deposit

Geneva Walls
Name of Person Mailing Correspondence

Geneva Walls July 14, 2005
Signature Date

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450.

**REQUEST THAT THE ISSUE FEE PAID ON JANUARY 12, 2004 BE APPLIED TOWARDS
THE NEW NOTICE OF ALLOWANCE**

Sir:

In response to the New Notice of Allowance, we request that the Issue Fee paid on January 12, 2004 be applied towards the new Notice of Allowance of the above-identified application.

If there are any additional fees associated with this communication, please charge Deposit

Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Tarek N. Fahmi
Reg. No. 41,402

Dated: July 14, 2005

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025-1026
(408) 947-8200

Tarek N. Fahmi
650.798.0320
tfahmi@sonnenschein.com

1530 Page Mill Road
Suite 200
Palo Alto, CA 94304-1125
650.798.0300
650.798.0310 fax
www.sonnenschein.com

February 1, 2010

Mail Stop M Correspondence
Director of the US Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

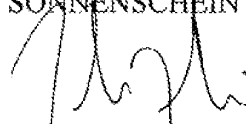
Re: U.S. Patent No. 7,084,423
US Application No. 10/217,758
Our Docket No.: 40003771-0003-002

Issue Date: 08/01/2006
Filing Date: 08/12/2002

Dear Sir/Madam:

This letter is to notify the United States Patent and Trademark Office that the entity status for the above-referenced patent has changed from large entity status to small entity status.

Very truly yours,
SONNENSCHN NATH & ROSENTHAL LLP



Tarek N. Fahmi
Reg. No. 41,402

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INSTRUCTIONS: Only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be specified when the patentee would like correspondence related to maintenance fees to be mailed to a different address than the correspondence address for the application.

When to check the first box below: If the fee address for the patent and/or application number(s) you indicate is to be established with, or changed to, an existing Customer Number.

When to check the second box below: If a Customer Number representing the fee address has to be established so it can then be associated with the patent and/or application number(s) you indicate. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

Please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:



Customer Number:

26263

OR



Request for Customer Number (PTO/SB/125) attached hereto
in the following listed application(s) for which the Issue Fee has been paid for patent(s).

PATENT NUMBER (if known)	APPLICATION NUMBER
7,084,423	10/217,758

Completed by (check one):



Applicant/Inventor

/Tarek N. Fahmi/
Signature



Attorney or Agent of record 41,402
(Reg. No.)

Tarek N. Fahmi
Typed or printed name



Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

650.798.0320
Requester's telephone number



Assignee recorded at Reel _____ Frame _____

February 1, 2010
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.



* Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	6923647
Application Number:	10217758
International Application Number:	
Confirmation Number:	1710
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	08791
Filer:	Tarek N. Fahmi
Filer Authorized By:	
Attorney Docket Number:	3771P003
Receipt Date:	01-FEB-2010
Filing Date:	12-AUG-2002
Time Stamp:	16:50:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	40003771-0003-002_Entity_Stat us_change_02_01_2010.pdf	373114 73d58a1456c0fd4d7d9cbd5864645b558f7 1a303	no	1

Warnings:

Information:

2	Change of Address	40003771-0003-002_Fee_Address_Indication_02_01_2010.pdf	269702 6287d308a2f90bb40c073179f539e870c8827c53	no	1
Warnings:					
Information:					
Total Files Size (in bytes):			642816		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

**REVOCATION OF PREVIOUS POWERS OF ATTORNEY WITH NEW
GENERAL POWER OF ATTORNEY TO PROSECUTE APPLICATIONS AND REEXAMINATION
PROCEEDINGS BEFORE THE UNITED STATES PATENT AND TRADEMARK OFFICE**

I hereby revoke all previous powers of attorney given in the application(s), reexamination proceeding(s) and/or patent(s) listed below and appoint:

Practitioners associated with the Customer Number

27571

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications and reexamination proceedings assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application(s), reexamination proceeding(s) and/or patent(s) listed below to the address associated with Customer Number 27571.

Assignee Name and Address:

Acom Technologies, Inc.
1200 Prospect Street, Suite 475
La Jolla, California 92037

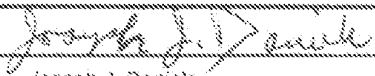
A statement under 37 CFR 3.73(b) is attached.

List of application(s), reexamination proceeding(s) and/or patent(s):

See Attached List.

SIGNATURE OF ASSIGNEE OF RECORD

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	3/14/2012
Name	Joseph J. Daniele	Telephone	858-551-1552
Title	Chief Operating Officer		

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Acorn Technologies, Inc.

States that it is:

1. ☒ The assignee of the entire right, title, and interest, or
2. ☐ an assignee of less than the entire right, title and interest
(The extent (by percentage) of its ownership interest is: _____%)

in the patent applicants/patents identified in the attached spreadsheet by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent applications/patents identified in the attached spreadsheet. The assignment was recorded in the United States Patent and Trademark Office at the Reel and Frame listed thereon.

OR

B. ☐ A chain of title from the inventor(s) of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____
The document was recorded in the United States Patent and Trademark office at
Reel _____, Frame _____, or for which a copy thereof is attached.
2. From: _____ To: _____
The document was recorded in the United States Patent and Trademark office at
Reel _____, Frame _____, or for which a copy thereof is attached.
3. From: _____ To: _____
The document was recorded in the United States Patent and Trademark office at
Reel _____, Frame _____, or for which a copy thereof is attached.

Additional documents in the chain of title are listed on a supplemental sheet.

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Tarek N. Fahmi/
Signature

March 26, 2013
Date

Tarek N. Fahmi
Printed or Typed Name

866-877-4883
Telephone Number

Attorney of Record
Title

AppNumber	FileDate	AssignmentTo	Reel	Frame	Ref No.
10/217758	12-Aug-02	Acom Technologies, Inc.	013195	0068	40003771-0003-002
11/181217	13-Jul-05	Acom Technologies, Inc.	13195	0068	40003771-0003-003
10/753504	07-Jan-04	Acom Technologies, Inc.	015453	0248	40003771-0003-005
10/753504	07-Jan-04	Acom Technologies, Inc.	016115	0318	40003771-0003-005
10/753504	07-Jan-04	Acom Technologies, Inc.	018401	0333	40003771-0003-005
12/197996	25-Aug-08	Acom Technologies, Inc.	022077	0447	40003771-0003-403
13/022522	07-Feb-11	Acom Technologies, Inc.	022077	0447	40003771-0003-453
10/342576	14-Jan-03	Acom Technologies, Inc.	016771	0810	40003771-0004-002
11/403185	11-Apr-06	Acom Technologies, Inc.	018181	0437	40003771-0004-403
10/754966	09-Jan-04	Acom Technologies, Inc.	18181	437	40003771-0004-004
13/022559	07-Feb-11	Acom Technologies, Inc.	018181	0437	40003771-0004-453
10/832576	26-Apr-04	Acom Technologies, Inc.	015846	0802	40003771-0005-002
11/010048	09-Dec-04	Acom Technologies, Inc.	016081	0879	40003771-0007-002
11/166286	23-Jun-05	Acom Technologies, Inc.	016729	0283	40003771-0008-002
13/019789	02-Feb-11	Acom Technologies, Inc.	016729	0283	40003771-0008-004
11/678397	23-Feb-07	Acom Technologies, Inc.	019424	0808	40003771-0009-002
12/878930	09-Sep-10	Acom Technologies, Inc.	019424	0808	40003771-0009-004
12/253769	17-Oct-08	Acom Technologies, Inc.	022058	0069	40003771-0010-002
12/253835	17-Oct-08	Acom Technologies, Inc.	022063	0521	40003771-0011-002
12/549227	27-Aug-09	Acom Technologies, Inc.	023159	0144	40003771-0014-002
61/537433	21-Sep-11	Acom Technologies, Inc.	027228	0055	40003771-0015-051

Electronic Acknowledgement Receipt

EFS ID:	12396190
Application Number:	10217758
International Application Number:	
Confirmation Number:	1710
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	8791
Filer:	Tarek N. Fahmi/Jennifer Stewart
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771P003
Receipt Date:	26-MAR-2012
Filing Date:	12-AUG-2002
Time Stamp:	18:55:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Acorn_executed_POA.pdf	325167 80c6d19a8e22bf29e157c34ec08b5aba90fe056d	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Power of Attorney	1	1
	Assignee showing of ownership per 37 CFR 3.73(b).	2	3
Warnings:			
Information:			
Total Files Size (in bytes):		325167	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/217,758	08/12/2002	Daniel E. Grupp	40003771-0003

27571
TAREK N. FAHMI, APC
84 W. Santa Clara St.
Suite 550
San Jose, CA 95113

CONFIRMATION NO. 1710
POA ACCEPTANCE LETTER



Date Mailed: 04/04/2012

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/26/2012.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/ttkim/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/217,758	08/12/2002	Daniel E. Grupp	40003771-0003

8791
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

CONFIRMATION NO. 1710
POWER OF ATTORNEY NOTICE



Date Mailed: 04/04/2012

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/26/2012.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/ttkim/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101