

¹ Discovery in this case is ongoing. Accordingly, Plaintiff expects that these contentions may be subject to supplementation and/or amendment after further discovery and disclosure of Defendants' non-infringement positions in order to focus the issues in this case. For example, Plaintiff may supplement these contentions in response to information learned during discovery to rebut allegations of non-infringement either literally or under the doctrine of equivalents. Additionally, Plaintiff expects that these contentions may be subject to amendment or supplementation to identify and accuse additional devices released, developed, or made available after the date on which these contentions are served.

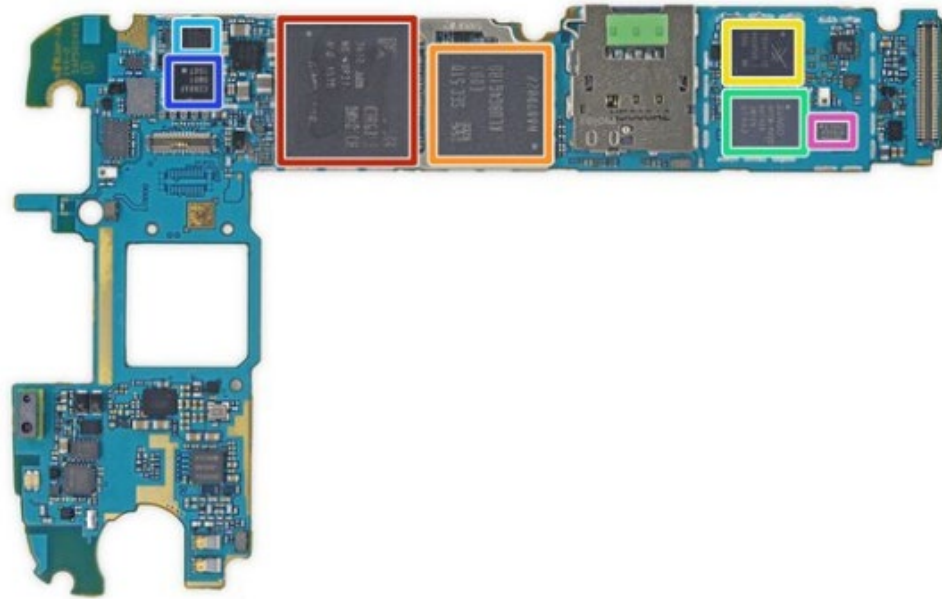
² As described in more detail herein, the limitations recited in this chart are all met by processors (and the transistors thereon) that Samsung manufactures according to Samsung's 14 nm FinFET process technology, including Samsung's 14LPE and 14LPP processes. Samsung makes, uses, sells, offers for sale, imports, advertises, and/or markets these infringing processors. The infringing processors include Samsung Exynos processors (and the transistors thereon) manufactured by Samsung according to Samsung's 14 nm FinFET process technology, including the Samsung Exynos 7420, Samsung Exynos 7570, Samsung Exynos 7870, Samsung Exynos 7880, Samsung Exynos 7872, Samsung Exynos 7874, Samsung Exynos 7885, Samsung Exynos 8890, Samsung Exynos 7904, and Samsung Exynos 7270 processors. The infringing processors also include third-party processors (and the transistors thereon) manufactured by Samsung according to Samsung's 14 nm FinFET process technology, including A9 processors. The infringing processors, in turn, are incorporated into a wide range of Samsung and third party devices, including the Samsung Galaxy A40, Samsung Galaxy A30, Samsung Galaxy M30, Samsung Galaxy M20, Samsung Galaxy M10, Samsung Galaxy J2 Core, Samsung Galaxy On6, Samsung Galaxy J6, Samsung Galaxy J4, Samsung Galaxy A6, Samsung Galaxy On7 Prime, Samsung Galaxy A8, Samsung Galaxy A8+, Samsung Galaxy J7, Samsung Galaxy J5, Samsung Galaxy J3, Samsung Galaxy Xcover 4, Samsung Galaxy A7, Samsung Galaxy A5, Samsung Galaxy A3, Samsung Galaxy A8, Samsung Galaxy J7, Samsung Galaxy S7 Edge, Samsung Galaxy S7, Samsung Galaxy Note5, Samsung Galaxy S6 Edge+, Samsung Galaxy S6 Edge, Samsung Galaxy S6, Samsung Galaxy S6 Active, Samsung Galaxy Tab A10.1, Samsung Galaxy Tab Active 2, Samsung Galaxy J7 Duo, Samsung Galaxy Gear Sport, Samsung Galaxy Gear S3 Frontier, Samsung Galaxy Gear S3 Classic, Apple iPhone 6s, Apple iPhone 6s Plus, Xiaomi Mi 5, Alcatel Idol 4S Windows 10 mobile(6071W), ASUS ZenFone 3 Deluxe, Blackberry DTEK60, Gree Phone 2, Gree Phone 2 mini, HP Elite X3, HTC 10, Light L 16, LeEco (leTv) Le Max 2 X820, LeEco (LeTv) LeMax Pro X910, LeEco (LeTv) Le Pro 3 Elite, LeEco (LeTv) Max 3 X920, Lenovo ZUK Z2, Lenovo ZUK Z2 Pro, LG G5, LG Q8, LG V20, Moto Z, Moto Z Force, OnePlus 3, Qiku 360 Q5 Plus, Samsung Galaxy S7 Active, Samsung Galaxy Note 7, Samsung Galaxy Tab S3, Sharp Aquos Zeta SH-04H, Sharp Aquos XX3, Sony Xperia X Performance, Sony Xperia XZ, Sony Xperia XZS, TCL 950, Vertu Constellation, Vivo Xplay 5 Elite, Vivo Xplay 6, 8848 M4, Xiaomi Mi 5 Prime/Pro, ZTE Axon 7, ZTE Nubia Z11, Google Pixel, Google Pixel XL, Xiaomi Mi 5s, HTC U Ultra, ASUS ZenFone 3 Deluxe, Asus Zenfone AR, Asus Zenfone Ares, Xiaomi Mi 5s Plus, Xiaomi Mi Note 2, Xiaomi Mi Mix, LeEco Le Pro 3, LeEco Cool Changer S1, Smartisan M1, Smartisan M1L, OnePlus 3T, Lenovo ZUK Edge, LG G6, LG G6+, LG G7 Fit, ZTE Axon 7s, ZTE Axon M, and Samsung Galaxy Note FE. The foregoing processors and devices incorporating those processors are the "Samsung Accused Devices."

1[a] An electrical junction comprising

To the extent the preamble is limiting, the Samsung Accused Devices include electrical junctions. Broadly speaking, the Samsung Accused Devices are processors, such as the Exynos 7420, the Snapdragon 820, and the Apple A9, which are devices that use electrical energy to operate, and electronic devices incorporating those processors, such as the Galaxy S6, the LG G5, and the iPhone 6s. The below pictures depict, as an example, a teardown of a Galaxy S6 to reveal the Exynos 7420 processor therein, outlined in red.

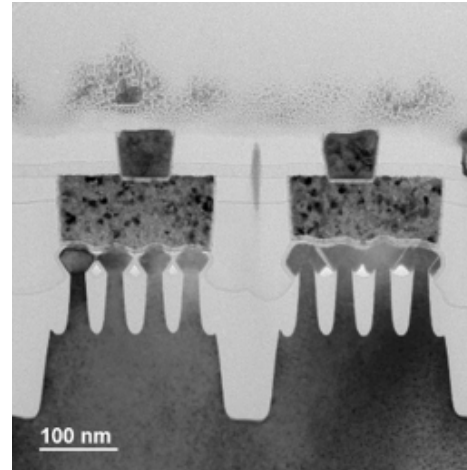






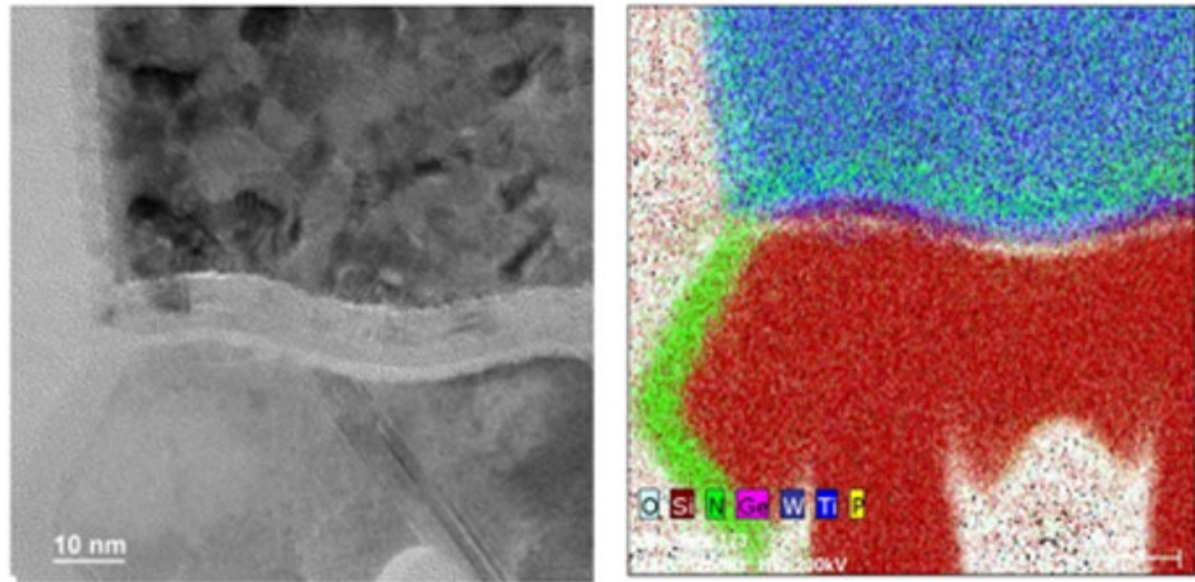
See <https://www.ifixit.com/Teardown/Samsung+Galaxy+S6+Teardown/39174> (last visited February 28, 2020).

The Samsung Accused Devices include billions of FinFET transistors packed closely together and corresponding contacts, with junctions between the semiconductor of the transistors and the contacts that constitute junctions between a silicon-based semiconductor (at the source/drain area of the FinFET transistor) and a conductor (the corresponding metal electrical contact). Taking a random cross section from one Samsung accused processor reveals the following transmission electron microscope (TEM) image, which depicts the source/drain semiconductor region of two FinFET transistors (each of the transistors having four fins), their corresponding metal electrical contacts, and the junctions between them.

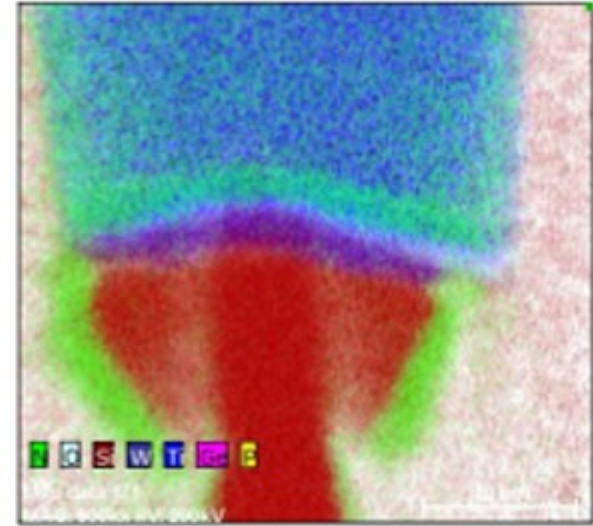
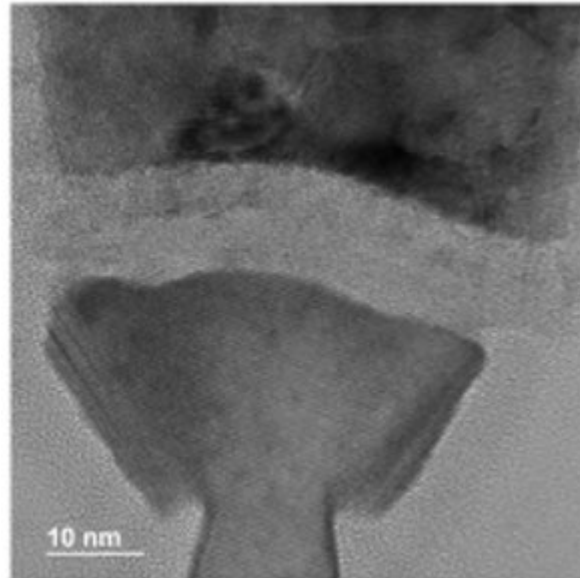


Samsung 14nm LPE - Exynos 7420 (Galaxy S6)

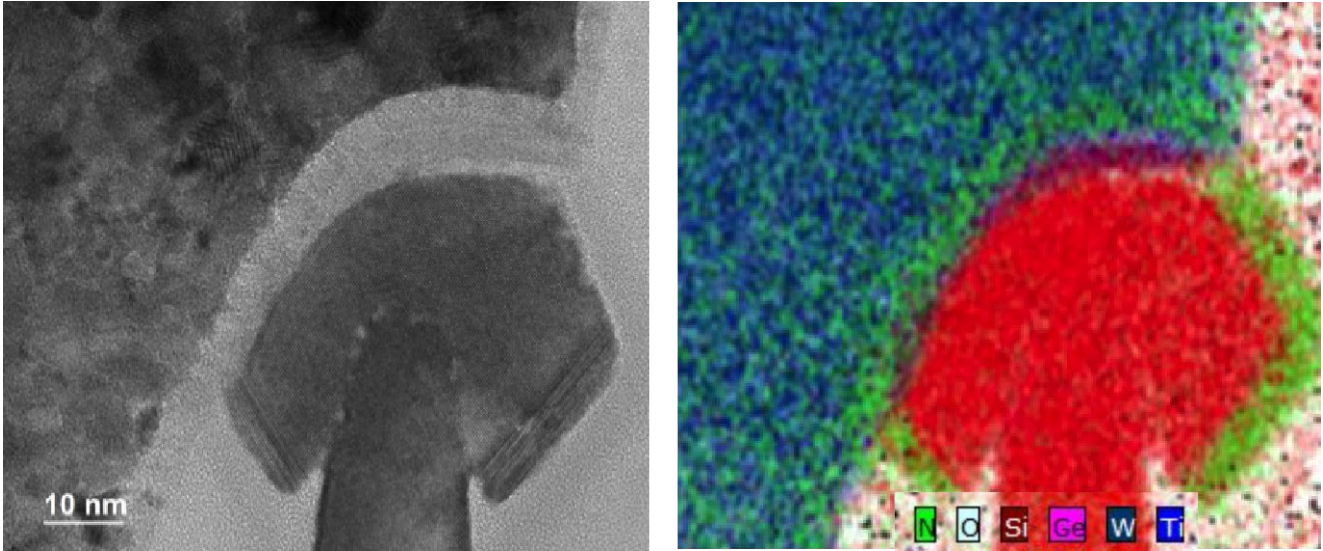
The images below are similar TEM images, zoomed in more closely. The images on the left below are close-up TEM images of the electrical junction between a FinFET source/drain region and the corresponding contact in various exemplary Samsung Accused Devices. The color images on the right are EDX elemental intensity maps showing that the source/drain is made of a silicon-based semiconductor and the contact area includes two conductors, tungsten (W) and titanium nitride (TiN).



Samsung 14nm LPE – Exynos 7420 (Galaxy S6)



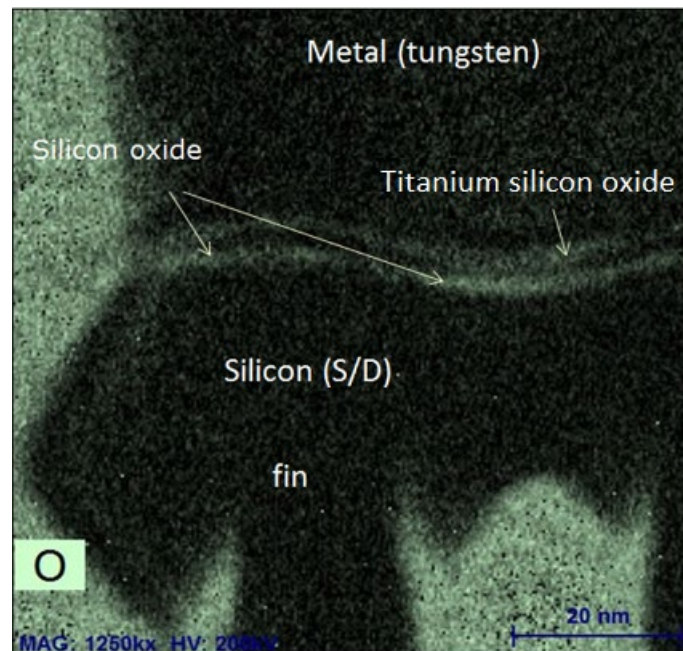
Samsung 14 nm LPP - Qualcomm Snapdragon 820 (LG G5)

	 Samsung 14 nm LPE - Apple A9 (iPhone 6s)
1[b] a region in a semiconductor substrate, a metal electrical contact to said region, and an interface layer between said region and said metal electrical contact,	As described and shown above with respect to claim limitation 1[a], the accused electrical junctions include: (1) a region in a semiconductor substrate, which is the silicon-based source/drain region of the FinFET transistor; (2) a metal electrical contact to said region, which includes tungsten and titanium nitride, and an interface layer disposed therebetween.
1[c] said region being electrically connected to said metal electrical contact through said interface layer	As shown and described above with respect to claim limitation 1[a], the accused semiconductor region is electrically connected to the accused metal electrical contact through the accused interface layer. During operation of the Accused Samsung Devices, when the FinFET is turned on, an electrical current passes from the source contact through the interface layer to the semiconductor region and from the semiconductor region through the interface layer to the drain contact.
1[d] and said interface layer comprising a metal	The interface layer shown and described above with respect to claim limitations 1[a] and 1[b] includes a metal oxide and a semiconductor oxide.

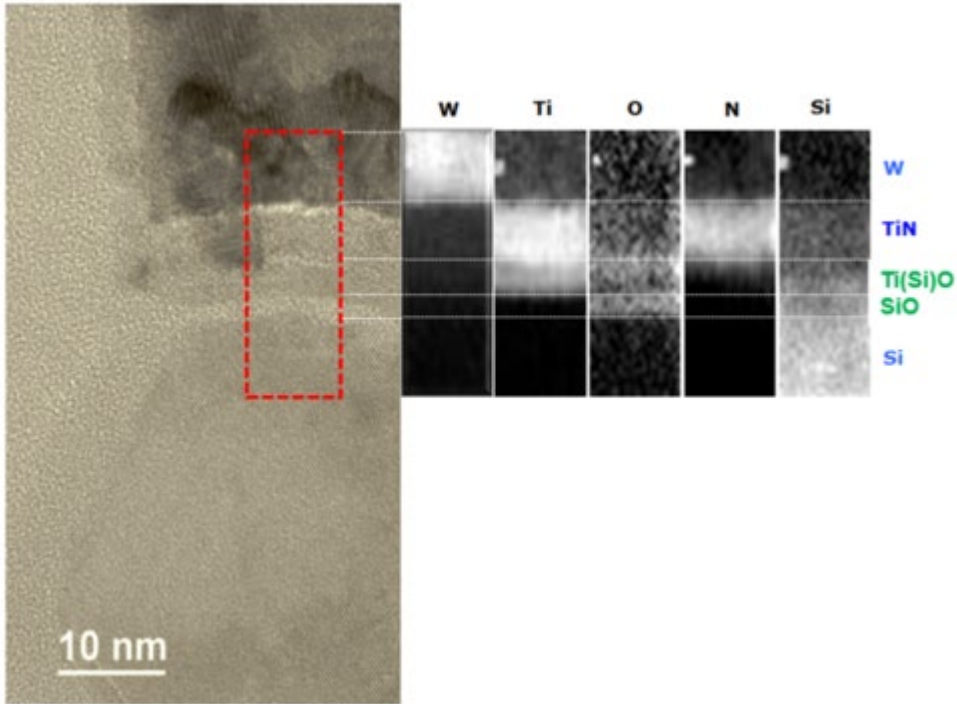
oxide and a semiconductor oxide,

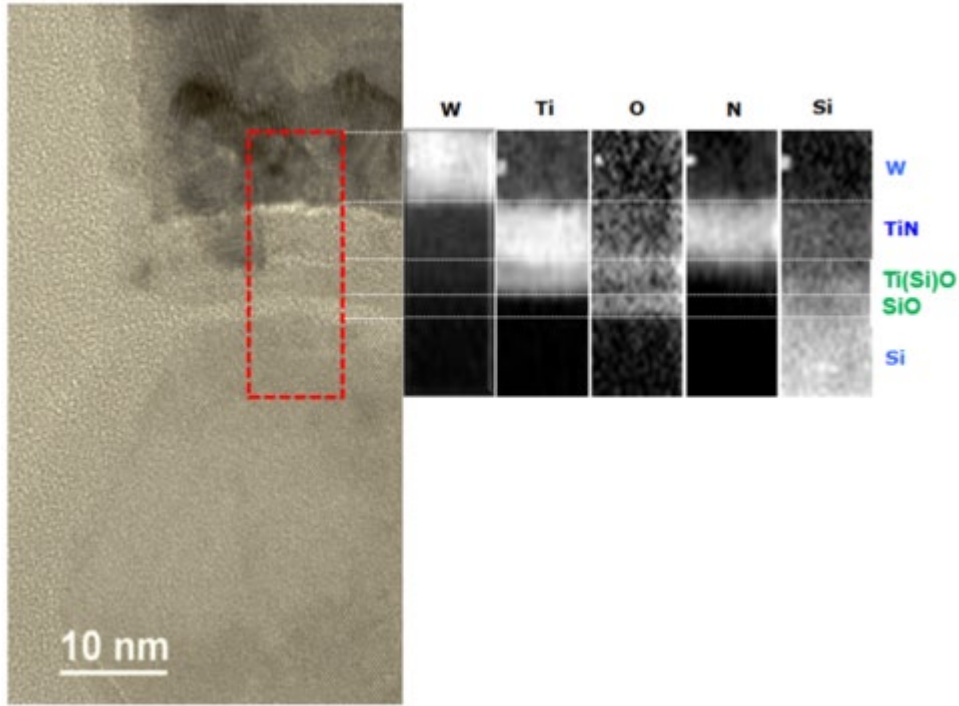
For example, the top image below shows an EDX oxygen elemental intensity map (oxygen indicated by green in top image below) of the interface layer, showing that it includes two sublayers, one of silicon oxide (a semiconductor oxide) and one of titanium silicon oxide (a metal oxide).

The next image below shows a TEM image and the corresponding EELS elemental intensity map of the same area again, showing the interface layer including silicon oxide and titanium silicon oxide sublayers.

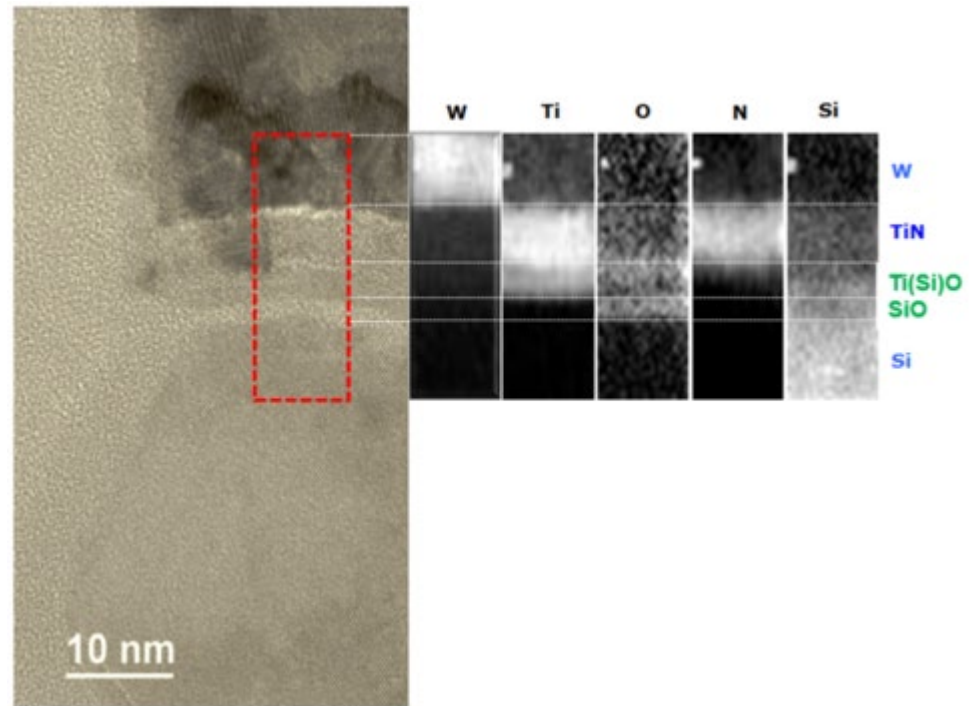


Samsung 14nm LPE - Exynos 7420 (Galaxy S6)

	 Samsung 14nm LPE - Exynos 7420 (Galaxy S6)
1[e] and being in contact with said region in the semiconductor substrate and said metal electrical contact.	As shown and described above with respect to claim limitations 1[a] and 1[d], the accused interface layer comprising silicon oxide and titanium silicon oxide sublayers is between and in contact with both the semiconductor substrate region (the silicon-based source/drain region of the FinFET transistors) and the metal electrical contact (including tungsten and titanium nitride).
2 The electrical junction of claim 1, wherein the semiconductor oxide comprises an oxide of the region in the	Acorn incorporates by reference all exemplary evidence related to claim 1 above. As shown and described above with respect to claim limitation 1[d], the semiconductor oxide sublayer is made of silicon oxide, which is an oxide of the semiconductor substrate region, which comprises silicon.

semiconductor substrate.	
3 The electrical junction of claim 2, wherein the semiconductor oxide has a thickness of approximately 0.1 nm to 5 nm.	Acorn incorporates by reference all exemplary evidence related to claim 2 above, as well as claim limitation 1[d] above. The exemplary TEM image and corresponding EELS elemental intensity map reproduced below show that the semiconductor oxide (made of silicon oxide) has a thickness of approximately 2 nm, which is between 0.1 nm and 5 nm.  Samsung 14nm LPE - Exynos 7420 (Galaxy S6)
4 The electrical junction of claim 1, wherein said region in the semiconductor substrate	Acorn incorporates by reference all exemplary evidence related to claim 1 above. As described and shown above with respect to claim limitation 1[a], the region in the accused semiconductor substrate comprises a source or drain of a FinFET transistor.

comprises a source or drain of a transistor.	
5 The electrical junction of claim 1, wherein said interface layer has a thickness sufficient to depin a Fermi level of the metal electrical contact in a vicinity of the junction yet thin enough to provide the junction with a specific contact resistivity that is generally dependent on: a workfunction of the metal electrical contact, a Fermi energy of the semiconductor in the region, or both the workfunction of the metal electrical contact and the Fermi energy of the semiconductor in the region.	Acorn incorporates by reference all exemplary evidence related to claim 1 above. The Samsung Accused Devices include FinFET transistors (with source/drain areas made up of a silicon-based semiconductor) and corresponding contacts (comprising tungsten and titanium nitride), that are separated by an interface layer having a thickness sufficient to depin a Fermi level of the metal electrical contact in a vicinity of the junction yet thin enough to provide the junction with a specific contact resistivity that is generally dependent on: a workfunction of the metal electrical contact, a Fermi energy of the semiconductor in the region, or both the workfunction of the metal electrical contact and the Fermi energy of the semiconductor in the region. For example, the TEM image and corresponding EELS elemental intensity map below show that the interface layer (comprising silicon oxide and titanium silicon oxide sublayers) measures approximately 5 nm thick.

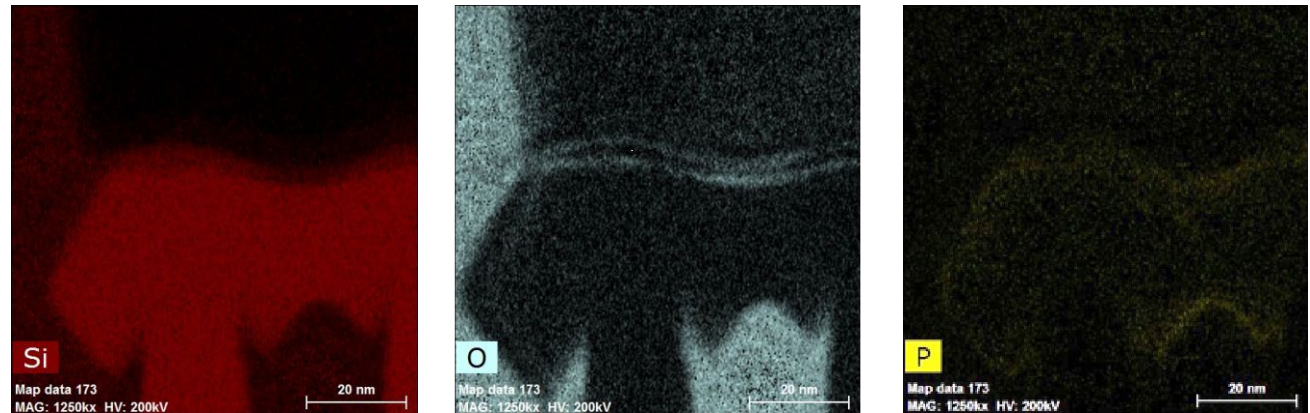


Samsung 14nm LPE - Exynos 7420 (Galaxy S6)

As described in the Complaint and the '395 Patent, at a typical metal-semiconductor junction, there exists a Schottky barrier (the energy needed to move an electron between the metal Fermi level and the semiconductor conduction band) that, for a low work function metal, is higher than simple theoretical models based on the work function of the metal would predict. This heightened Schottky barrier is due to the Fermi level of the metal being “pinned” between the valence and conduction bands of the semiconductor. As described in the '395 Patent, an interface layer of the correct materials and of sufficient thickness can “depin” the Fermi level of the metal, so as to reduce the Schottky barrier. Such an interface layer cannot be so thick, however, that it increases contact resistance at the junction significantly beyond that provided by the work function of the conductor. The approximately 5 nm interface layer depicted herein between the source/drain region of a FinFET transistor and its corresponding contact is of a thickness sufficient to depin a Fermi level of the conductor in a vicinity of

	the junction yet thin enough to provide the junction with a specific contact resistivity that is generally dependent on: a workfunction of the metal electrical contact, a Fermi energy of the semiconductor in the region, or both the workfunction of the metal electrical contact and the Fermi energy of the semiconductor in the region. <i>See, e.g.</i>, '395 Patent, 10:27-29 ("Often, the interface layer 520 includes or is made up of a passivation layer with a thickness of between approximately (0.1 nm and about 5 nm."). For example, the interface layer is sufficiently thick to terminate substantially all the silicon semiconductor surface dangling bonds. <i>See, e.g.</i>, '395 Patent, 15:63-16:2 ("The role played by interface layer 620 in tuning, adjusting, or controlling the height of the barrier between the conductor 630 and the semiconductor 610 may be understood as a depinning of the Fermi level of the semiconductor. That is, the interface layer may reduce surface states by bonding to the semiconductor material to consume dangling bonds."). It is also sufficiently thick to reduce the formation of MIGS—metal induced gap states—in the semiconductor. <i>See id.</i> at 16:2-5 ("Additionally, the interface layer may reduce the formation of MIGS in the semiconductor by providing a thickness and bandgap that prevent the electron wave function (of the metal) from penetrating into the semiconductor."). The conductor electron wave function penetration distance is 1-3 nm, or less, and thus does not substantially penetrate the silicon semiconductor. <i>See, e.g.</i>, Kobayashi et al., <i>Fermi-Level Depinning in Metal/Ge Schottky Junction and Its Application to Metal Source/Drain Ge NMOSFET</i>, 2008 Symposium on VLSI Technology Digest of Technical Papers, IEEE, pp. 54-55; Connelly et al., <i>A New Route to Zero-Barrier Metal Source/Drain MOSFETs</i>, IEEE Transactions on Nanotechnology, Vol. 3, No. 1, March 2004, pp. 98-10; Hu et al., <i>Fermi Level Depinning For the Design of III-V FET Source/Drain Contacts</i>, 2009 Symposium on VLSI Technology, IEEE, pp. 123-124; Mönch, <i>On the alleviation of Fermi-level pinning by ultrathin insulator layers in Schottky contacts</i>, Journal of Applied Physics, Vol. 111, pp. 073706-1 – 073706-7 (2012).
6 The electrical junction of claim 1, wherein said interface layer is configured to provide a specific contact resistivity between the metal electrical contact and the region in the	Acorn incorporates by reference all exemplary evidence related to claim 1 above. The interface layer of the accused electrical junctions is configured to provide a specific contact resistivity between the metal electrical contact and the source/drain region of the FinFET transistors of less than 10 $\Omega \cdot \mu\text{m}^2$. This is shown by the 2013 International Technology Roadmap for Semiconductors, which makes clear that doping process technology requirements for these devices have required specific contact resistances of less than 10 $\Omega \cdot \mu\text{m}^2$ for years.

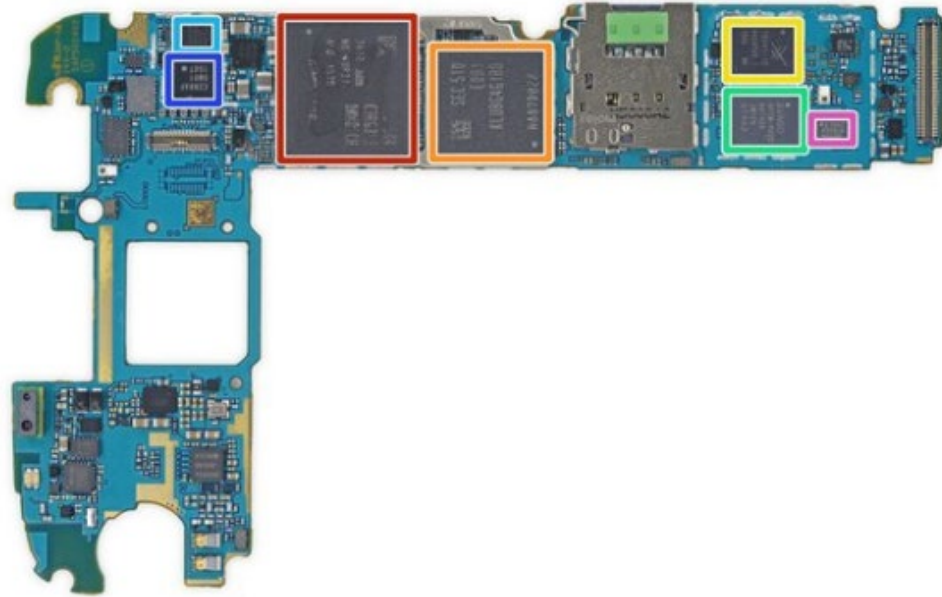
semiconductor of less than 10 Ω-μm ² .	<table><tr><th colspan="3">Table FEP11 Thermal, Thin Film, Doping Process Technology Requirements</th><th colspan="3">Rc expressed here as Ω · μm²</th></tr><tr><th>Year of Production</th><th>2013</th><th>2014</th><th>2015</th><th>2016</th><th>2017</th></tr><tr><td>Contact maximum resistivity for multi-gate MPU/ASI(Ω · μm²)</td><td>1.5</td><td>1.3</td><td>1.0</td><td>0.9</td><td>0.8</td></tr></table> See also, e.g., Agrawal <i>et al.</i>, Fermi level depinning and contact resistivity reduction using a reduced titania interlayer in n-silicon metal-insulator-semiconductor ohmic contacts, abstract (Applied Physics Letters 104, 112101 2014) (“Experimental evidence” showing “Ultra-low contact resistivity of 9.1 x 10⁻⁹ Ω-cm² [= 0.91 Ω·μm²] was obtained using Ti/10 Å TiO_{2-x}/n⁺ Si, which is a dramatic 13X reduction”).	Table FEP11 Thermal, Thin Film, Doping Process Technology Requirements			Rc expressed here as Ω · μm ²			Year of Production	2013	2014	2015	2016	2017	Contact maximum resistivity for multi-gate MPU/ASI(Ω · μm ²)	1.5	1.3	1.0	0.9	0.8
Table FEP11 Thermal, Thin Film, Doping Process Technology Requirements			Rc expressed here as Ω · μm ²																
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8 The electrical junction of claim 1, wherein said metal oxide comprises an oxide of said metal electrical contact.	Acorn incorporates by reference all exemplary evidence related to claim 1 above. As shown and described above with respect to claim limitations 1[a] and 1[d], the metal electrical contact comprises tungsten and titanium nitride, and thus comprises titanium, and the metal oxide layer comprises titanium silicon oxide, which comprises an oxide of titanium.																		
9 The electrical junction of claim 8, wherein said semiconductor oxide comprises an oxide of the region in the semiconductor substrate.	Acorn incorporates by reference all exemplary evidence related to claim 8 above. As shown and described above with respect to claim limitations 1[a] and 1[d], the semiconductor region comprises silicon, and the semiconductor oxide comprises silicon oxide, an oxide of silicon.																		
11 The electrical junction of claim 1, wherein said metal oxide comprises an oxide of titanium.	Acorn incorporates by reference all exemplary evidence related to claim 1 above. As shown and described above with respect to claim limitations 1[a] and 1[d], the accused metal oxide layer comprises titanium silicon oxide, which comprises an oxide of titanium.																		
12 The electrical junction of claim 11, wherein said semiconductor oxide comprises an oxide of silicon.	Acorn incorporates by reference all exemplary evidence related to claim 11 above. Acorn incorporates herein its arguments made with respect to claim 2 above.																		

14 The electrical junction of claim 12, wherein said region in the semiconductor substrate comprises an n-type doped source or drain of a transistor.	Acorn incorporates by reference all exemplary evidence related to claim 12 above. The silicon in the source/drain area of the accused FinFET transistors is n-type doped. Phosphorus is a common n-type dopant, and it is visible in the source/drain regions. Below are EELS elemental intensity maps of the Samsung 14nm LPE - Exynos 7420 (Galaxy S6) sample, highlighting silicon (red in left image), oxygen (light blue in middle image), and phosphorus (yellow in right image). The phosphorus color is very faint, even with image enhancement, because the density of phosphorus atoms is approximately 1% of the density of silicon atoms. 
15 The electrical junction of claim 1, wherein said metal electrical contact comprises titanium.	Acorn incorporates by reference all exemplary evidence related to claim 1 above. As shown and described above with respect to claim limitations 1[a] and 1[d], the metal electrical contact includes tungsten and titanium nitride, which comprises titanium.
16 The electrical junction of claim 1, wherein said metal electrical contact comprises tungsten.	Acorn incorporates by reference all exemplary evidence related to claim 1 above. As shown and described above with respect to claim limitations 1[a] and 1[d], the metal electric contact includes tungsten and titanium nitride, and thus comprises tungsten.
17[a] An electrical junction comprising:	To the extent the preamble is limiting, the Samsung Accused Devices include electrical junctions. Broadly speaking, the Samsung Accused Devices are processors, such as the Exynos 7420, the Snapdragon 820, and the Apple A9, which are devices that use electrical energy to operate, and electronic devices incorporating those processors, such as the Galaxy S6, the LG G5, and the iPhone

6s. The below pictures depict, as an example, a teardown of a Galaxy S6 to reveal the Exynos 7420 processor therein, outlined in red.

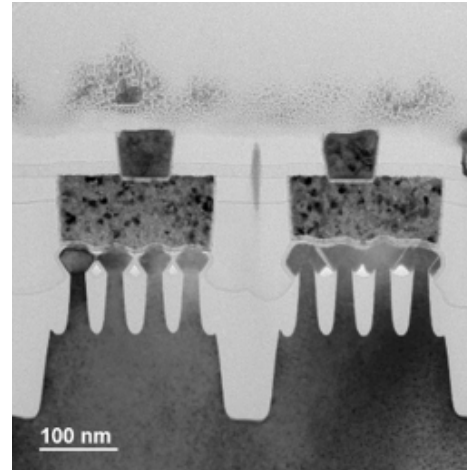






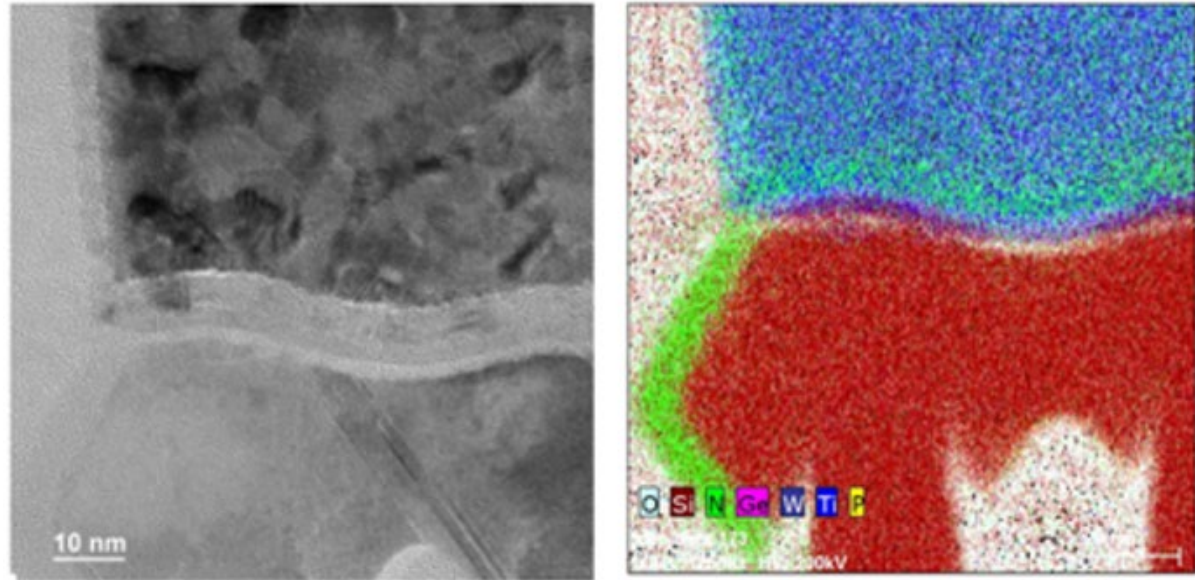
See <https://www.ifixit.com/Teardown/Samsung+Galaxy+S6+Teardown/39174> (last visited February 28, 2020).

The Samsung Accused Devices include billions of FinFET transistors packed closely together and corresponding contacts, with electrical junctions between the semiconductor of the transistors and the contacts. Taking a random cross section from one Samsung accused processor reveals the following transmission electron microscope (TEM) image, which depicts the source/drain semiconductor region of two FinFET transistors (each of the transistors having four fins), their corresponding metal electrical contacts, and the electrical junctions between them.

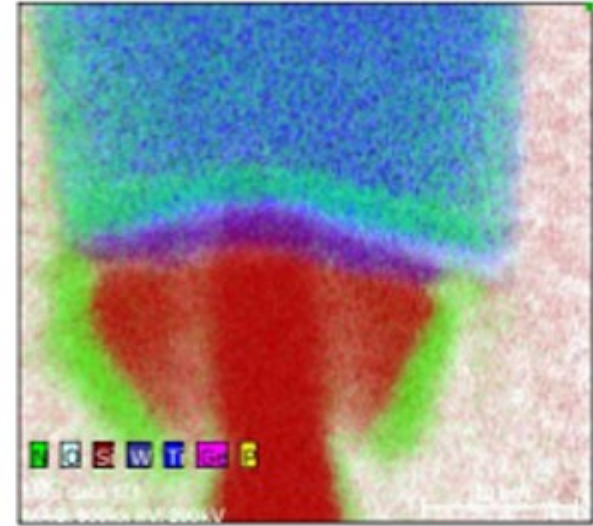
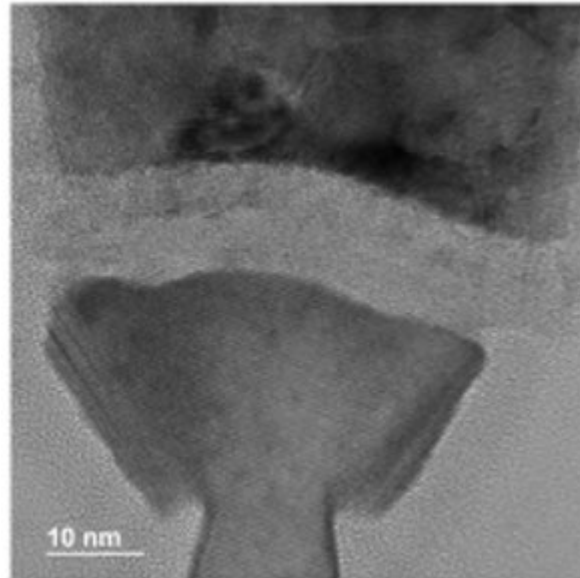


Samsung 14nm LPE - Exynos 7420 (Galaxy S6)

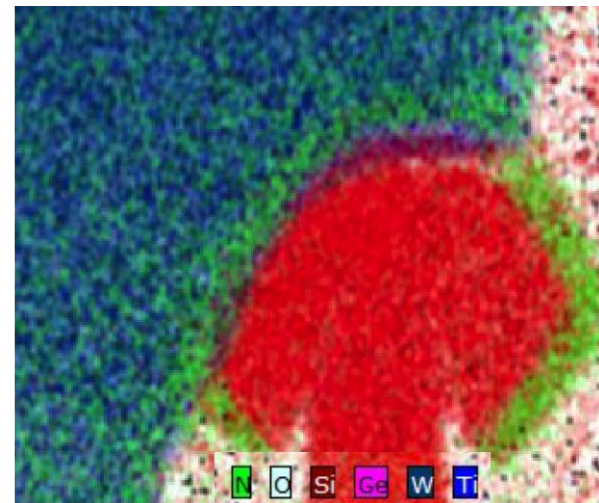
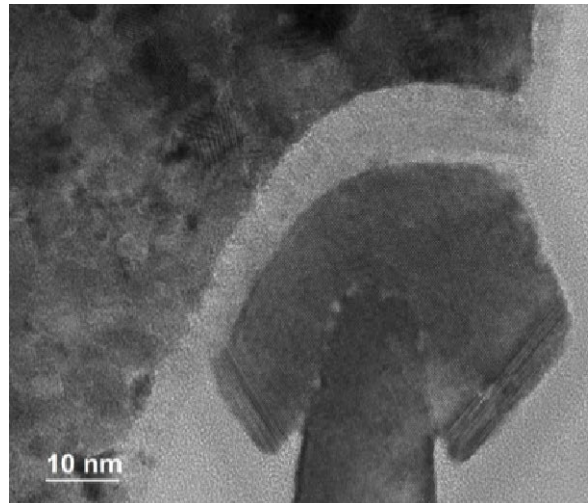
The images below are similar TEM images, zoomed in more closely. The images on the left below are close-up TEM images of the junction between a FinFET source/drain area and the corresponding contact in various exemplary Samsung Accused Devices. The color images on the right are EDX elemental intensity maps showing that the source/drain is made of a silicon-based semiconductor and the contact area includes two conductors, tungsten (W) and titanium nitride (TiN).



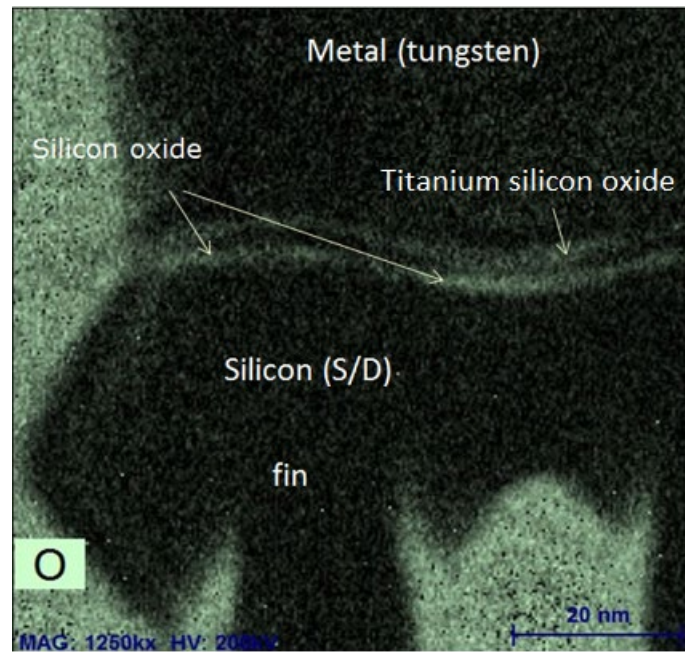
Samsung 14nm LPE - Exynos 7420 (Galaxy S6)



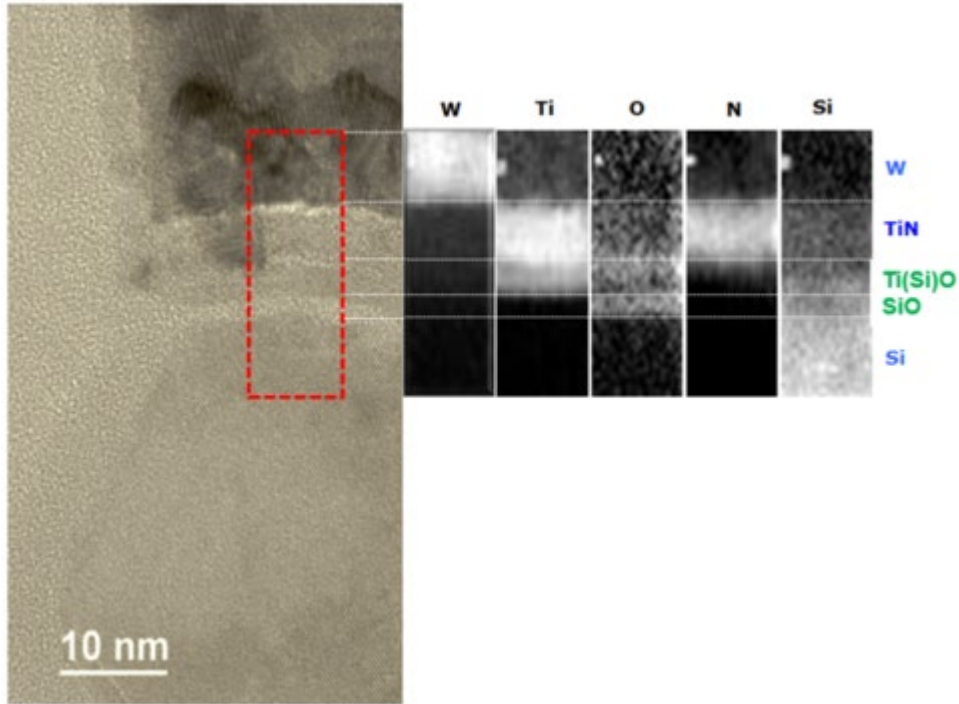
Samsung 14 nm LPP - Qualcomm Snapdragon 820 (LG G5)



	Samsung 14 nm LPE - Apple A9 (iPhone 6s)
17[b] a source or drain of a transistor, said source or drain comprising a semiconductor,	As described and shown above with respect to claim limitation 17[a], the semiconductor of the accused electrical junctions comprises a source or drain of a transistor.
17[c] a metal electrical contact to said source or drain, and	As described and shown above with respect to claim limitation 17[a], the contact to the source/drain region of the FinFET transistors comprises tungsten and titanium nitride, and thus comprises a metal electrical contact.
17[d] an interface layer disposed between and in contact with said source or drain and said metal electrical contact,	The Samsung Accused Devices include FinFET transistors (with source/drain regions made up of a silicon-based semiconductor) and corresponding contacts (which include tungsten and titanium nitride), that are separated by an interface layer disposed between them and in contact with both. For example, the top image below shows an EDS oxygen elemental intensity map (oxygen indicated by green in top image below) showing an interface layer between the semiconductor source/drain region of a FinFET transistor and a corresponding contact metal (tungsten) in an exemplary Samsung Accused Product. The next image below shows a TEM image and the corresponding EELS elemental intensity map of the same interface layer, including sublayers of silicon oxide and titanium silicon oxide, located between and in contact with the titanium nitride portion of the metal electrical contact and the silicon-based source/drain region of the FinFET transistor.



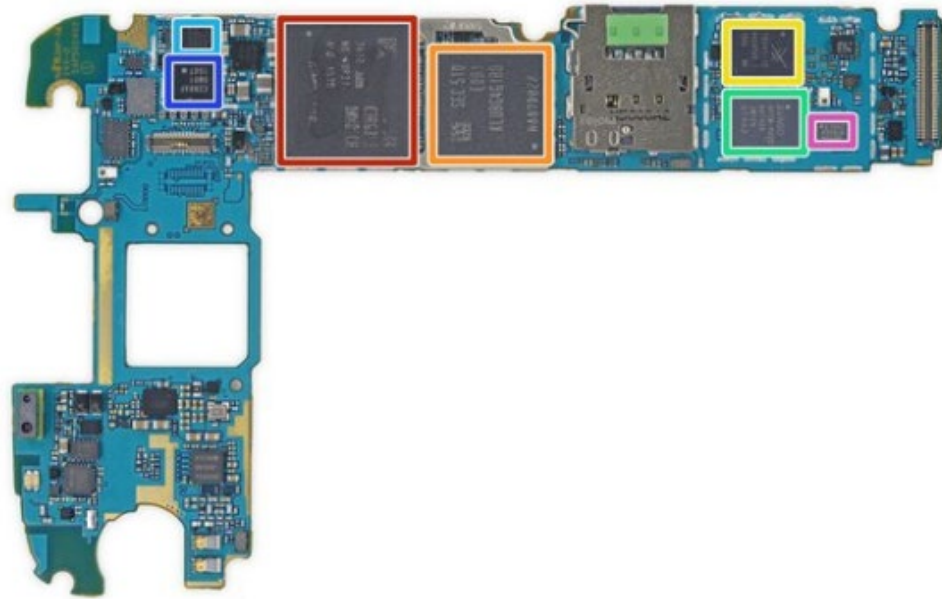
Samsung 14nm LPE - Exynos 7420 (Galaxy S6)

	 Samsung 14nm LPE - Exynos 7420 (Galaxy S6)
17[e] said source or drain being electrically connected to said metal electrical contact through said interface layer and	As shown and described above with respect to claim limitations 17[a] and 17[d], the accused semiconductor region (the source/drain region of the FinFET transistors) is electrically connected to the accused metal electrical contact through the interface layer that comprises silicon oxide and titanium silicon oxide sublayers. During operation of the Accused Samsung Devices, when the FinFET is turned on, an electrical current passes from the source contact through the layers to the semiconductor region and from the semiconductor region through the layers to the drain contact.
17[f] said interface layer comprising an oxide of titanium and an oxide of the semiconductor.	As shown and described above with respect to claim limitation 17[d], the accused interface layer includes sublayers of titanium silicon oxide, which comprises an oxide of titanium, and silicon oxide, which is an oxide of silicon. As shown and described above with respect to claim limitation 17[a], the source/drain regions of the accused FinFET transistors comprise silicon.

18 The electrical junction of claim 17, wherein said metal electrical contact includes titanium.	Acorn incorporates by reference all exemplary evidence related to claim 17 above. As shown and described above with respect to claim limitations 1[a] and 1[d], the metal electrical contact includes tungsten and titanium nitride, which includes titanium.
19 The electrical junction of claim 18, wherein said semiconductor comprises silicon.	Acorn incorporates by reference all exemplary evidence related to claim 18 above. Acorn incorporates herein its arguments made with respect to claim 17[f] above.
20 The electrical junction of claim 17, wherein said metal electrical contact includes tungsten.	Acorn incorporates by reference all exemplary evidence related to claim 17 above. As shown and described above with respect to claim limitations 17[a] and 17[d], the metal electric contact includes tungsten and titanium nitride, and thus comprises tungsten.
21 The electrical junction of claim 20, wherein said semiconductor comprises silicon.	Acorn incorporates by reference all exemplary evidence related to claim 20 above. Acorn incorporates herein its arguments made with respect to claim 17[f] above.
22 The electrical junction of claim 17, wherein said semiconductor comprises silicon.	Acorn incorporates by reference all exemplary evidence related to claim 17 above. Acorn incorporates herein its arguments made with respect to claim 17[f] above.
23[a] A semiconductor device, comprising:	To the extent the preamble is limiting, the Samsung Accused Devices comprise semiconductor devices. Broadly speaking, the Samsung Accused Devices are processors, such as the Exynos 7420, the Snapdragon 820, and the Apple A9, which are devices that use electrical energy to operate, and electronic devices incorporating those processors, such as the Galaxy S6, the LG G5, and the iPhone 6s. The below pictures depict, as an example, a teardown of a Galaxy S6 to reveal the Exynos 7420 processor therein, outlined in red.

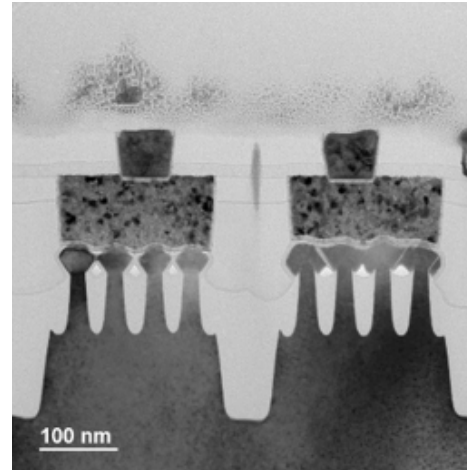






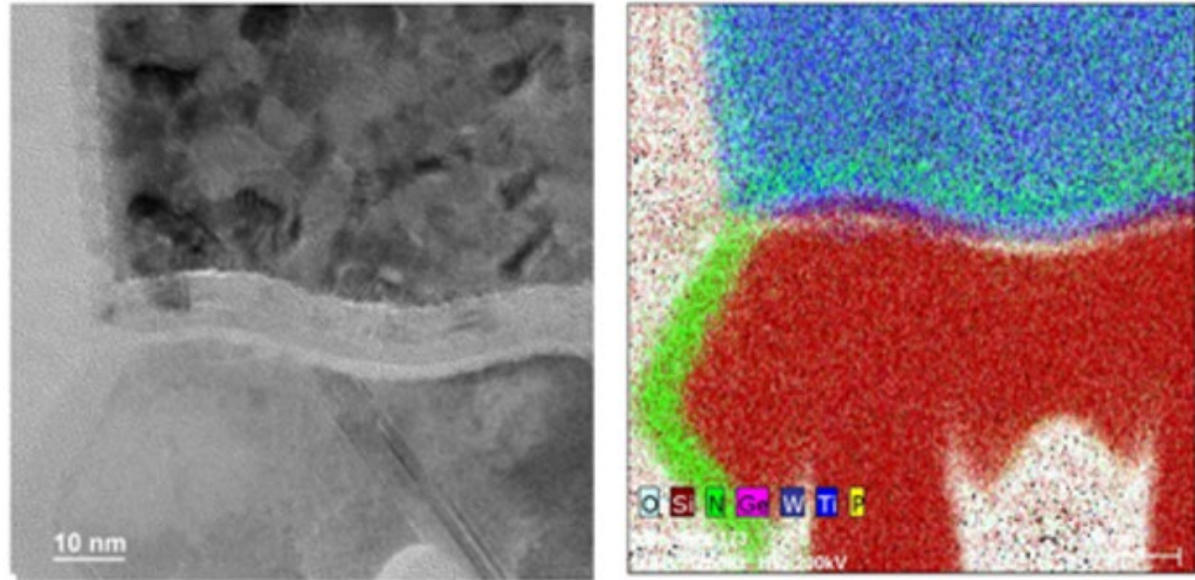
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The Samsung Accused Devices include billions of FinFET transistors packed closely together and corresponding contacts, with junctions between the semiconductor of the transistors and the contacts that constitute junctions between a silicon-based semiconductor (at the source/drain area of the FinFET transistor) and a conductor (the corresponding metal electrical contact). Taking a random cross section from one Samsung accused processor reveals the following transmission electron microscope (TEM) image, which depicts the source/drain semiconductor region of two FinFET transistors (each of the transistors having four fins), their corresponding metal electrical contacts, and the junctions between them. The FinFET transistors, with the metal contacts and the junctions between the semiconductor of the transistors and those contacts, comprise semiconductor devices.

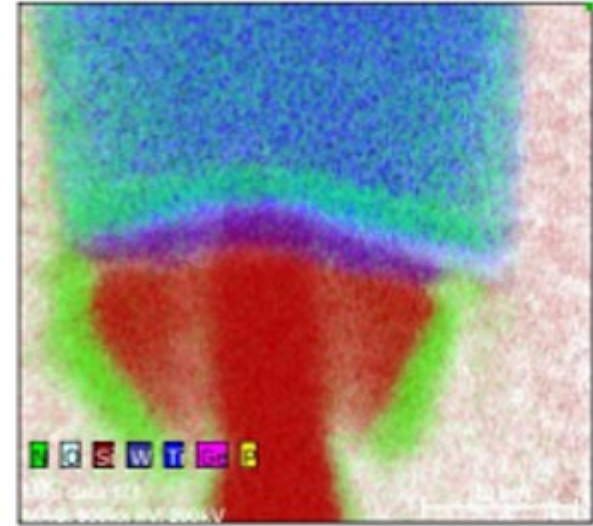
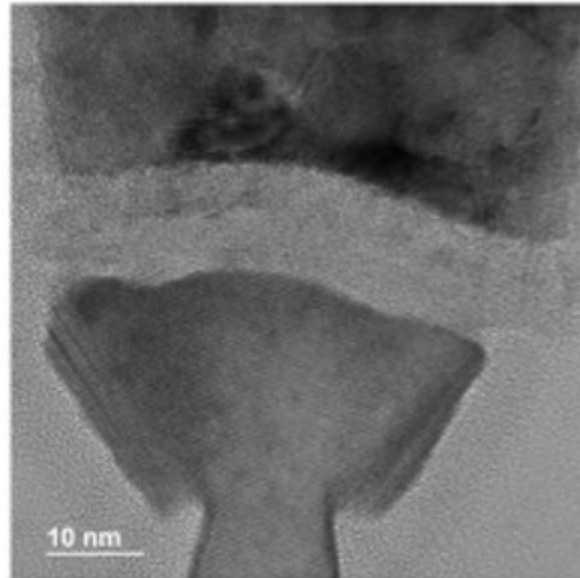


Samsung 14nm LPE - Exynos 7420 (Galaxy S6)

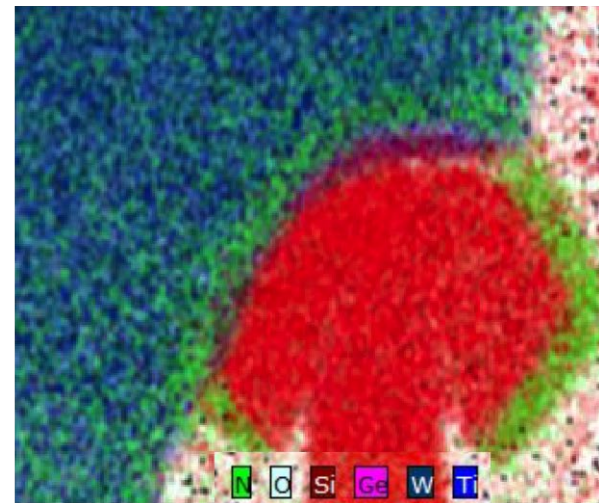
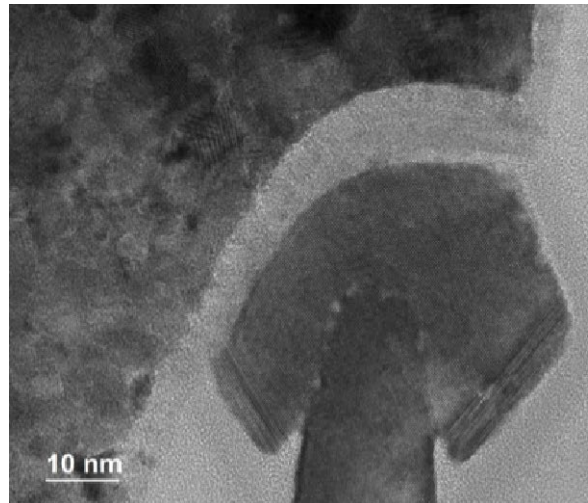
The images below are zoomed-in TEM images of the junction between a FinFET source/drain area and the corresponding contact in various exemplary Samsung Accused Devices. The images on the left are close-up TEM images. The color images on the right are EDX elemental intensity maps showing that the source/drain is made of a silicon-based semiconductor and the contact area includes two conductors, tungsten (W) and titanium nitride (TiN).



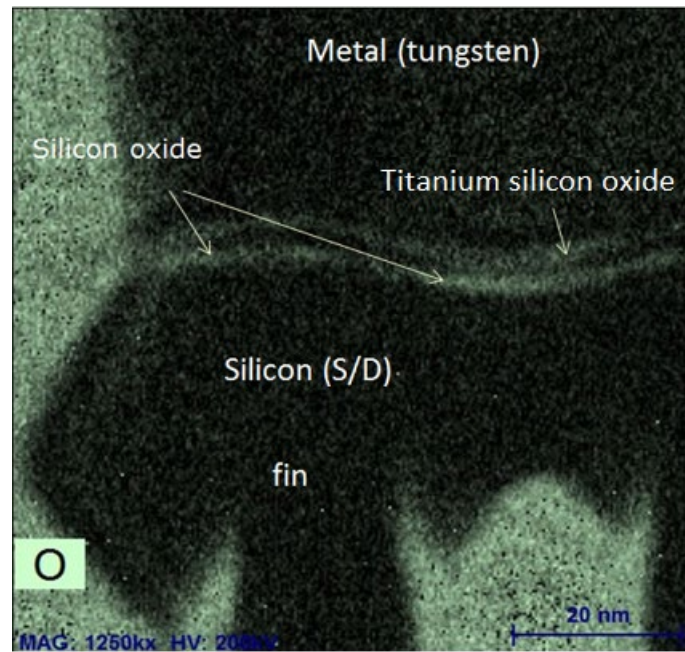
Samsung 14nm LPE - Exynos 7420 (Galaxy S6)



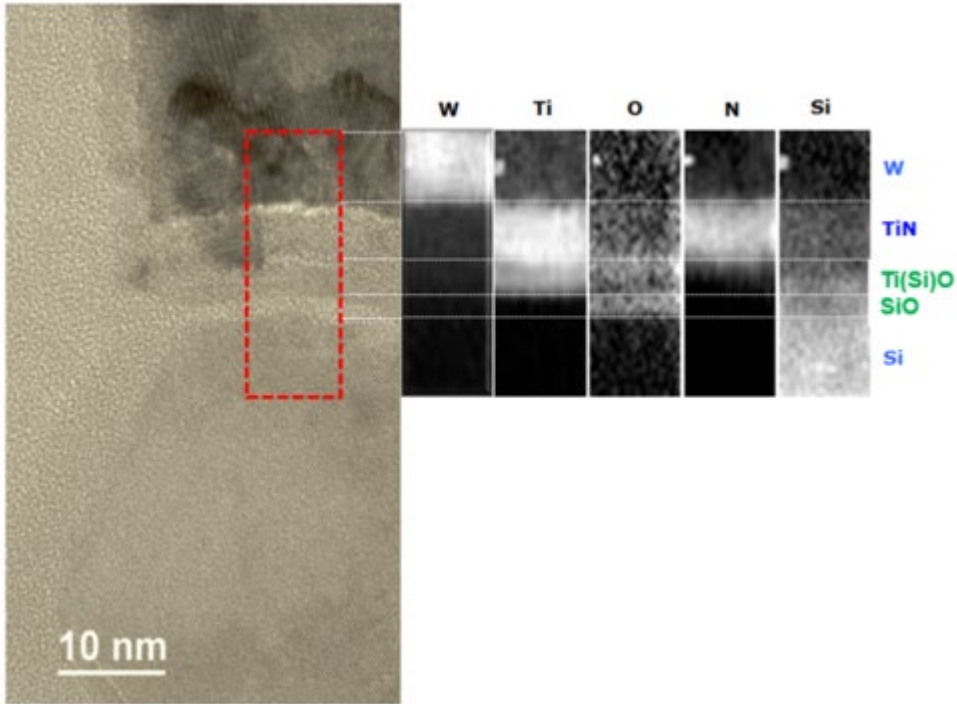
Samsung 14 nm LPP - Qualcomm Snapdragon 820 (LG G5)



	Samsung 14 nm LPE - Apple A9 (iPhone 6s)
23[b] a semiconductor region, a metal electrical contact to said semiconductor region, and an interface layer disposed between and in contact with said semiconductor region and said metal electrical contact,	As described and shown above with respect to claim limitation 23[a], the accused semiconductor devices include: (1) a semiconductor region, which is the silicon-based source/drain region of the FinFET transistor; (2) a metal electrical contact to said semiconductor region, which includes tungsten and titanium nitride, and an interface layer disposed therebetween and in contact with both.
23[c] said semiconductor region being electrically connected to said metal electrical contact through said interface layer and	As shown and described above with respect to claim limitation 23[a], the accused semiconductor region is electrically connected to the accused metal electrical contact through the interface layer. During operation of the Accused Samsung Devices, when the FinFET is turned on, an electrical current passes from the source contact through the interface layer to the semiconductor region and from the semiconductor region through the interface layer to the drain contact.
23[d] said interface layer comprising an oxide of titanium and an oxide of the semiconductor region.	The Samsung Accused Devices include FinFET transistors (with source/drain areas made up of a silicon-based semiconductor) and corresponding contacts (which include tungsten and titanium nitride), that are separated by an interface layer disposed between them and in contact with both. That interface layer comprises a layer of titanium silicon oxide, which comprises an oxide of titanium. That interface layer also comprises a layer of silicon oxide, which is an oxide of silicon, which is a component of the semiconductor region. For example, the top image below shows an EDS oxygen elemental intensity map (oxygen indicated by green in top image below) showing an interface layer between the silicon-based source/drain area of a FinFET transistor and a corresponding contact metal (tungsten) in an exemplary Samsung Accused Product. That interface layer includes two sublayers, one of titanium silicon oxide and another of silicon oxide. The next image below shows a TEM image and the corresponding EELS elemental intensity map of the same interface layer, including sublayers of silicon oxide and titanium silicon oxide, located between and in contact with the titanium nitride portion of the metal electrical contact and the silicon-based source/drain region of the FinFET transistor.



Samsung 14nm LPE - Exynos 7420 (Galaxy S6)

	 Samsung 14nm LPE - Exynos 7420 (Galaxy S6)
24 The semiconductor device of claim 23, wherein said metal electrical contact includes titanium.	Acorn incorporates by reference all exemplary evidence related to claim 23 above. As shown and described above with respect to claim limitations 23[a] and 23[d], the metal electric contact includes tungsten and titanium nitride, which comprises titanium.
25 The semiconductor device of claim 24, wherein said semiconductor region comprises silicon.	Acorn incorporates by reference all exemplary evidence related to claim 24 above. As shown as described above with respect to claim limitations 23[a] and 23[d], the semiconductor region (the silicon-based source/drain region of the FinFET transistor) comprises silicon.

26 The semiconductor device of claim 23, wherein said metal electrical contact includes tungsten.	Acorn incorporates by reference all exemplary evidence related to claim 23 above. As shown and described above with respect to claim limitations 23[a] and 23[d], the metal electric contact includes tungsten and titanium nitride, and thus comprises tungsten.
27 The semiconductor device of claim 26, wherein said semiconductor region comprises silicon.	Acorn incorporates by reference all exemplary evidence related to claim 26 above. As shown as described above with respect to claim limitations 23[a] and 23[d], the semiconductor region (the silicon-based source/drain region of the FinFET transistor) comprises silicon.
28 The semiconductor device of claim 23, wherein said semiconductor region comprises silicon.	Acorn incorporates by reference all exemplary evidence related to claim 23 above. As shown as described above with respect to claim limitations 23[a] and 23[d], the semiconductor region (the silicon-based source/drain region of the FinFET transistor) comprises silicon.