

EXHIBIT B-1

FILED UNDER SEAL

Acorn
v.
Samsung

DR. EDWIN PINER

Acorn Technical Expert – Dr. Edwin Piner



EDUCATION:

NC STATE
UNIVERSITY

1993: B.S. Material Science
& Engineering

1998: Ph.D. Material
Science & Engineering

Acorn Technical Expert – Dr. Edwin Piner



EXPERIENCE:

ATMI Corporation/Epitronics: Research Engineer

.....

Nitronex Corporation: Director of Advanced Technology

.....



Professor:

Semiconductor device microfabrication,
Semiconductor device physics,
Electrical characterization of materials, etc.

.....



Senior Member

Acorn Technical Expert – Dr. Edwin Piner



Inventor: Dr. Edwin Piner



30+ Patents
relating to semiconductor materials

Overview

Technology Background

Infringement

Value of the Invention

Samsung's Knowledge of the Invention

Technical Comparability of License Agreements

Smallest Salable Patent Practicing Unit = Wafer

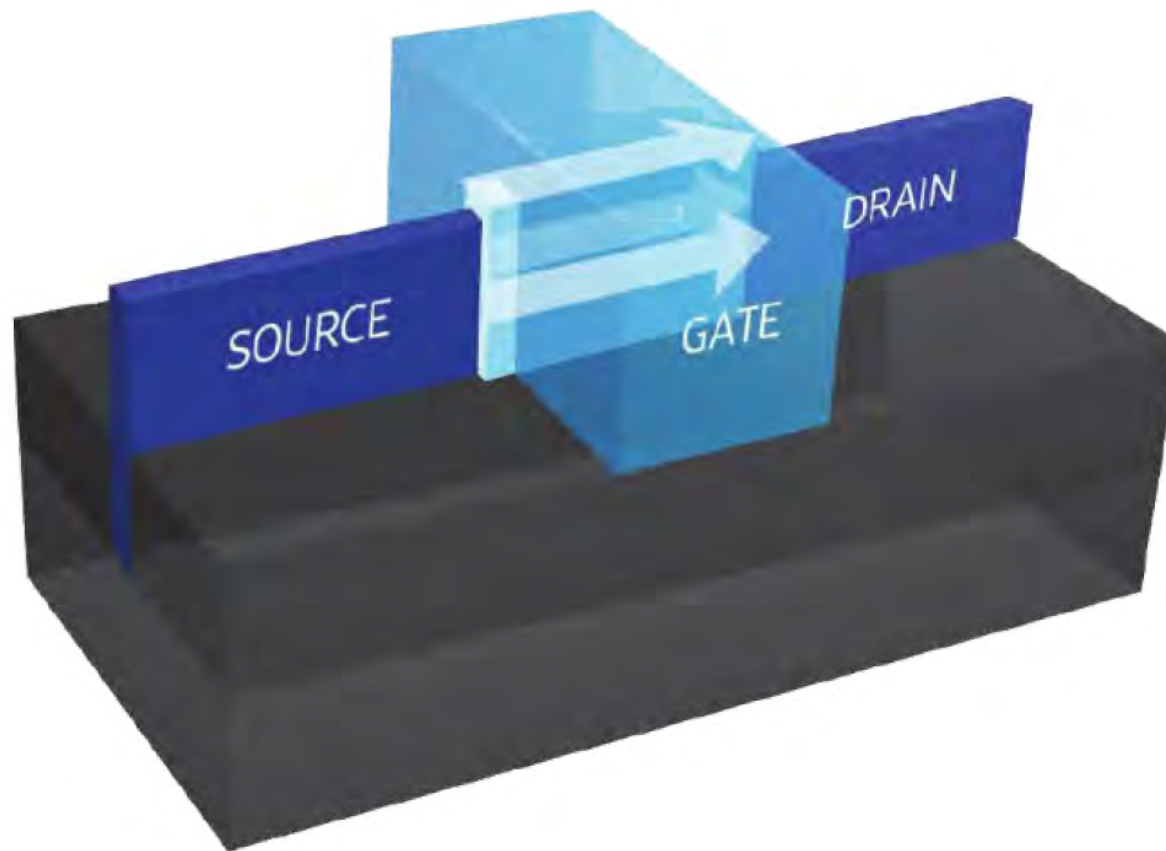
Materials Considered

- The '336, '167, '691, and '395 Patents
- 10 sample Samsung devices
- Samsung documentation regarding its 14nm FinFET process and devices
- Samsung witness testimony
- Patents and technical publications re semiconductor materials

**HIGHLY
CONFIDENTIAL**

**HIGHLY
CONFIDENTIAL**

Transistor



PTX00433

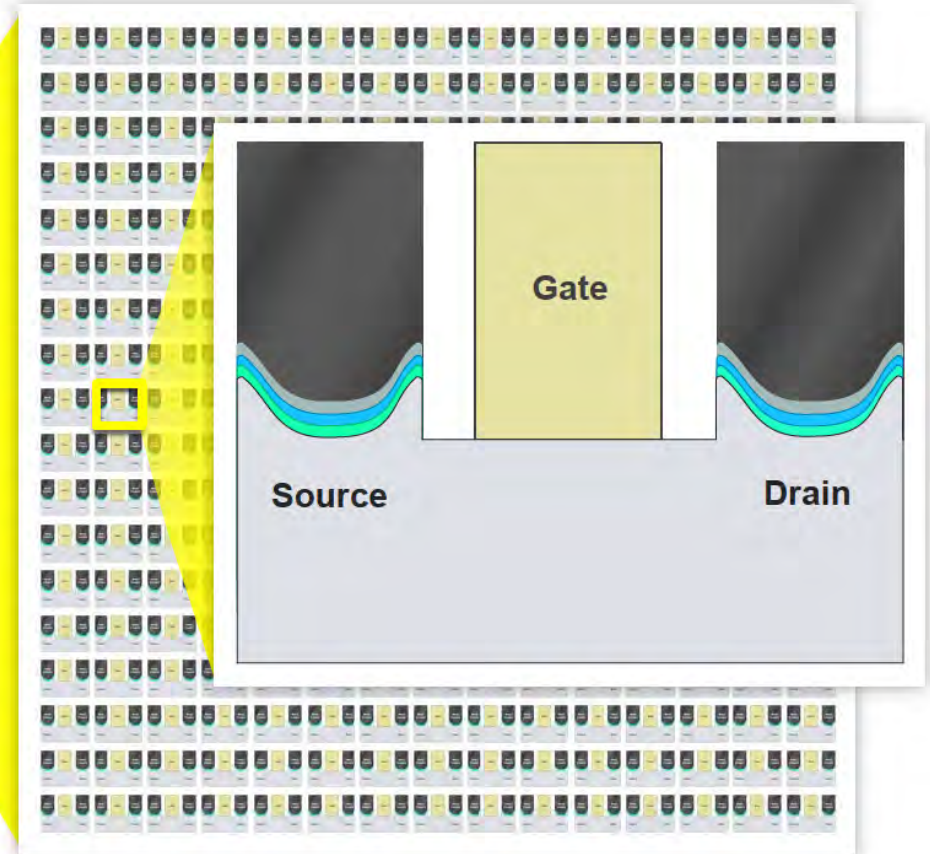
Accused Transistor Devices: 14 nm FinFET



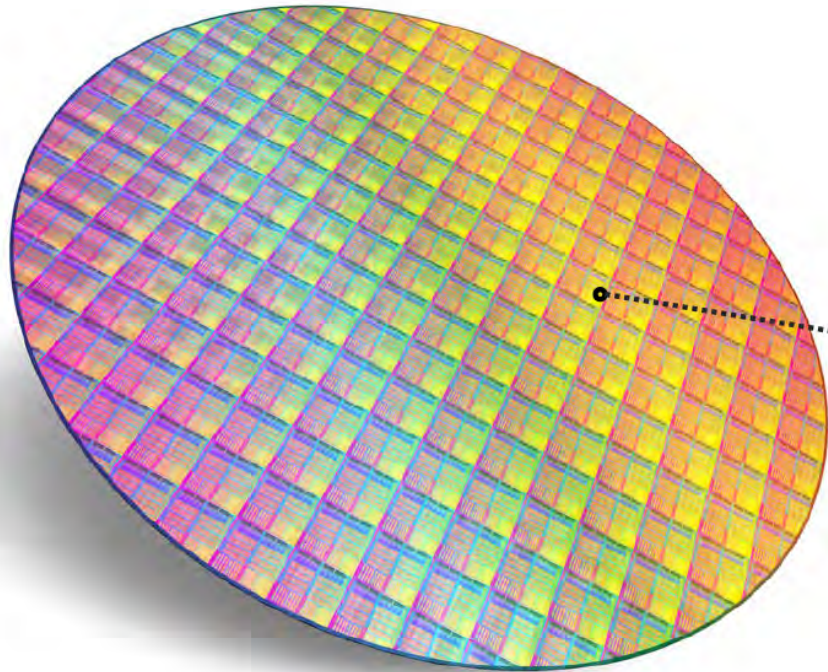
SAMSUNG Galaxy S6



SAMSUNG
Exynos
Processor



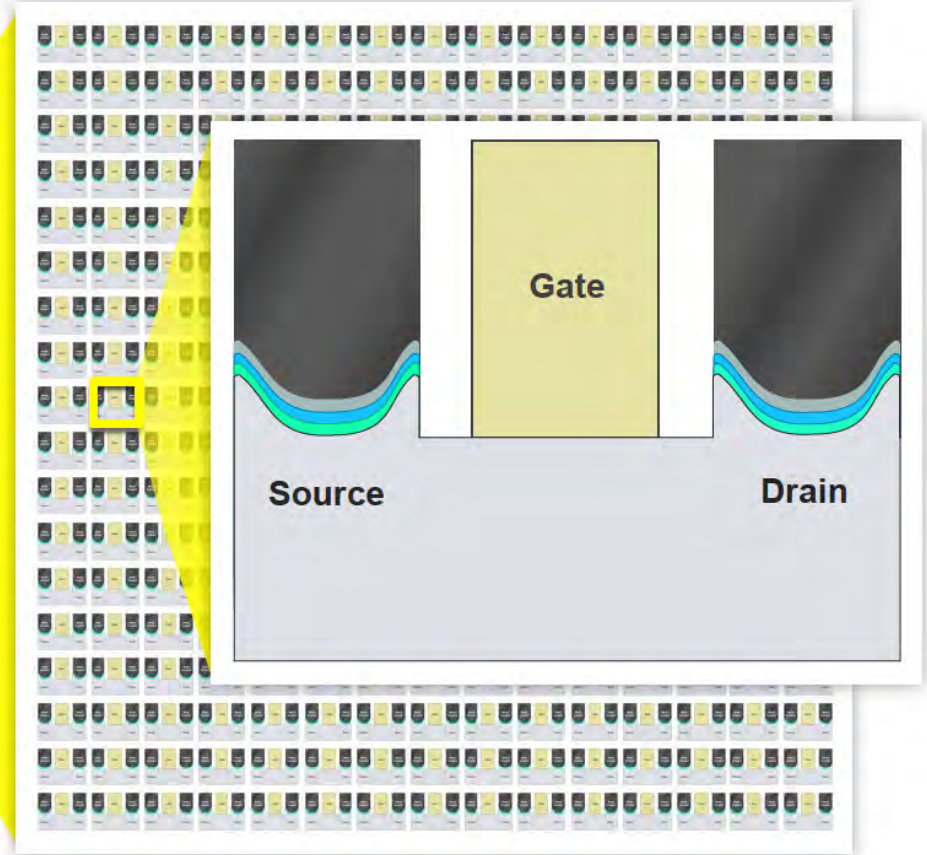
Accused Transistor Devices: 14 nm FinFET



Semiconductor Wafer

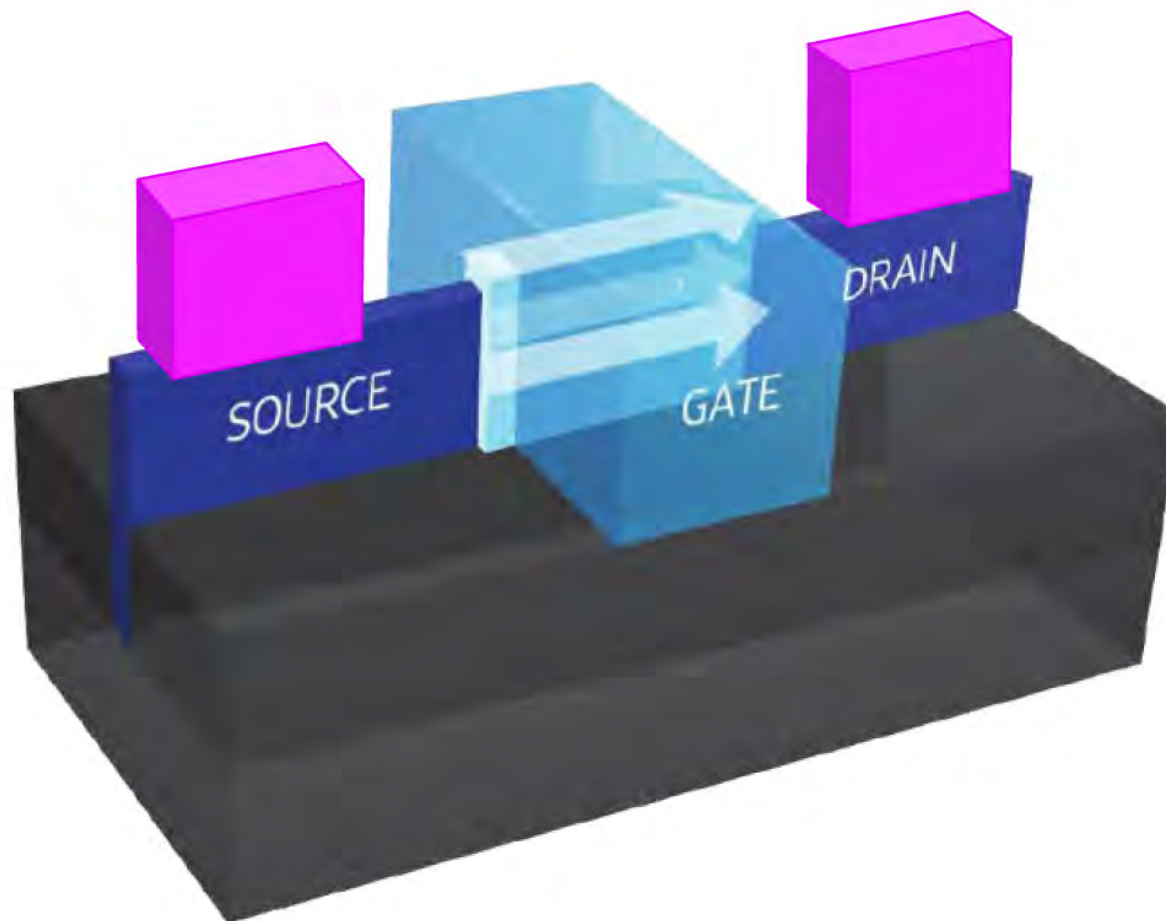


SAMSUNG
Exynos
Processor



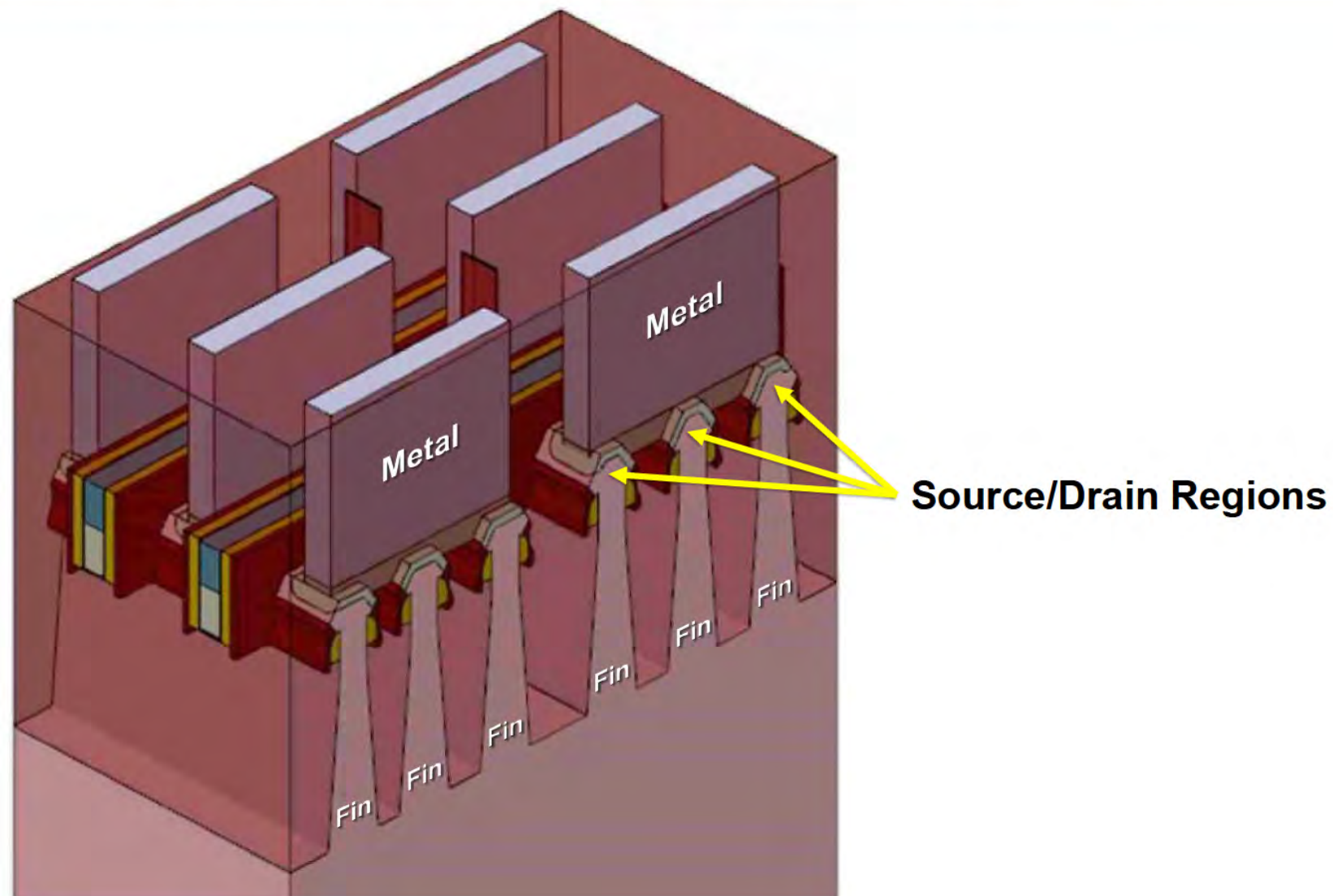
Case 2:19-cv-00347-JRG Document 401-3 Filed 09/02/21 Page 11 of 115 PageID #: 22714

Accused Transistor Devices: 14 nm FinFET



Case 2:19-cv-00347-JRG Document 401-3 Filed 09/02/21 Page 12 of 115 PageID #: 22715

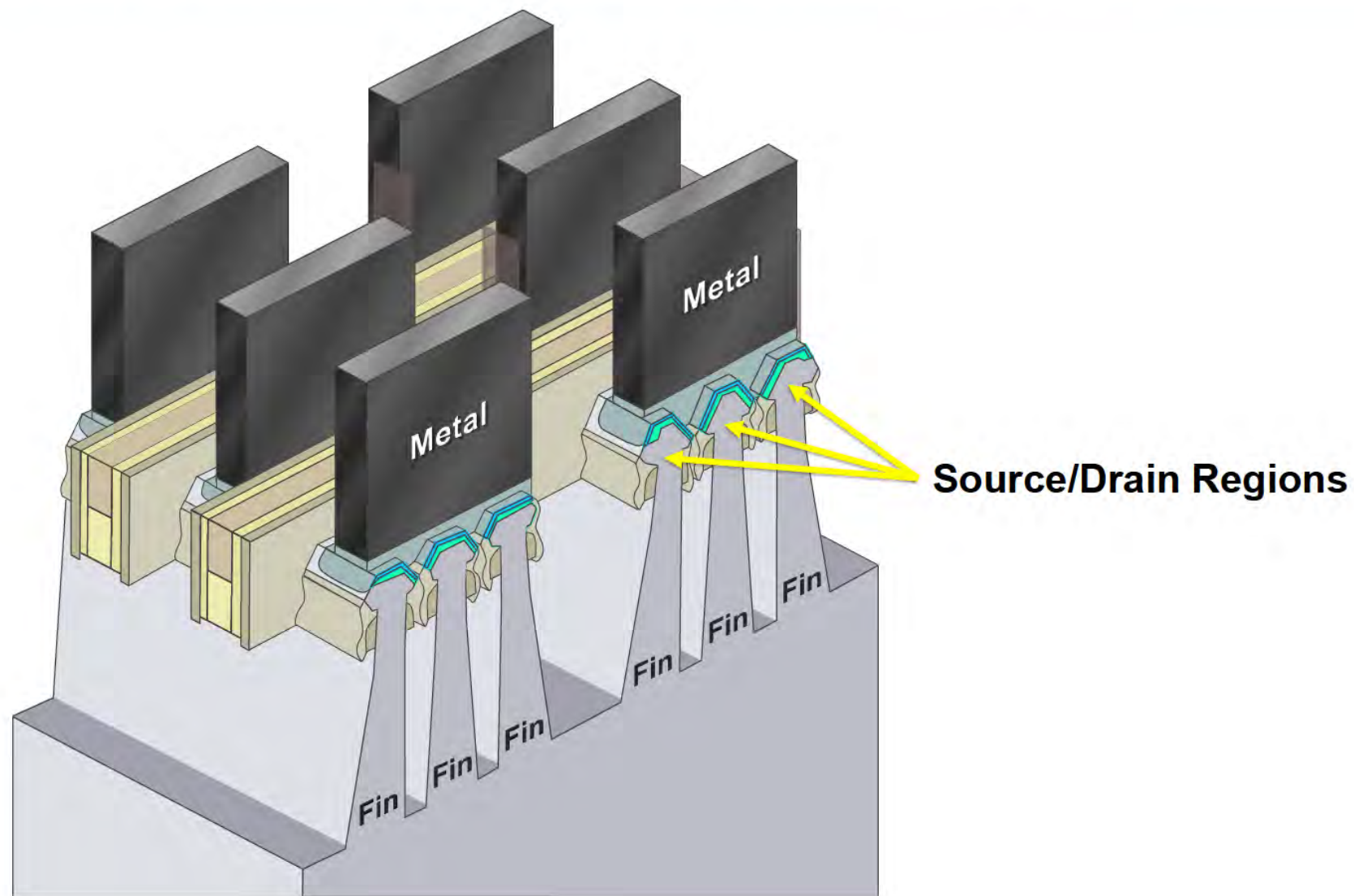
Accused Transistor Devices: 14 nm FinFET



PTX00650

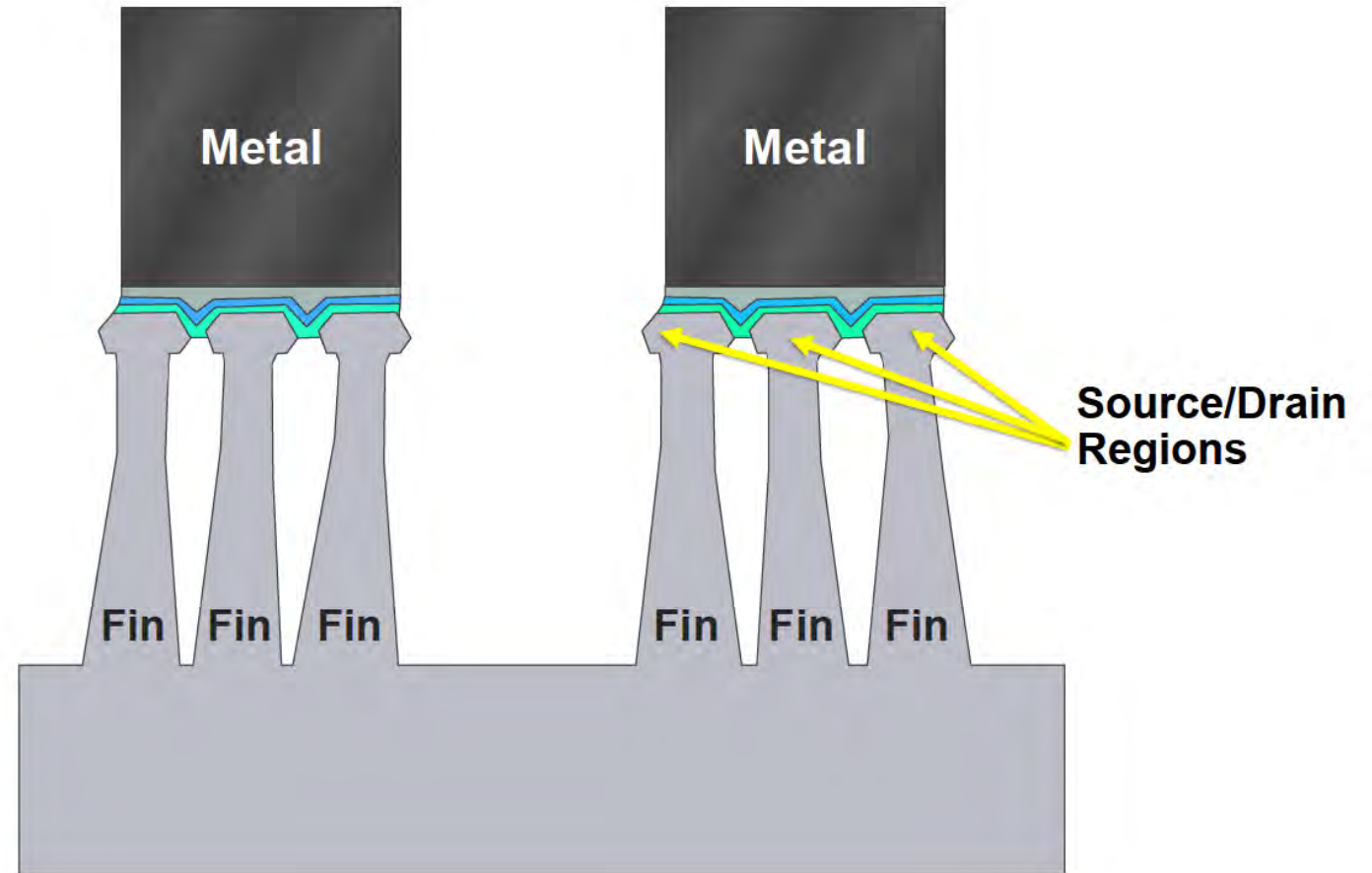
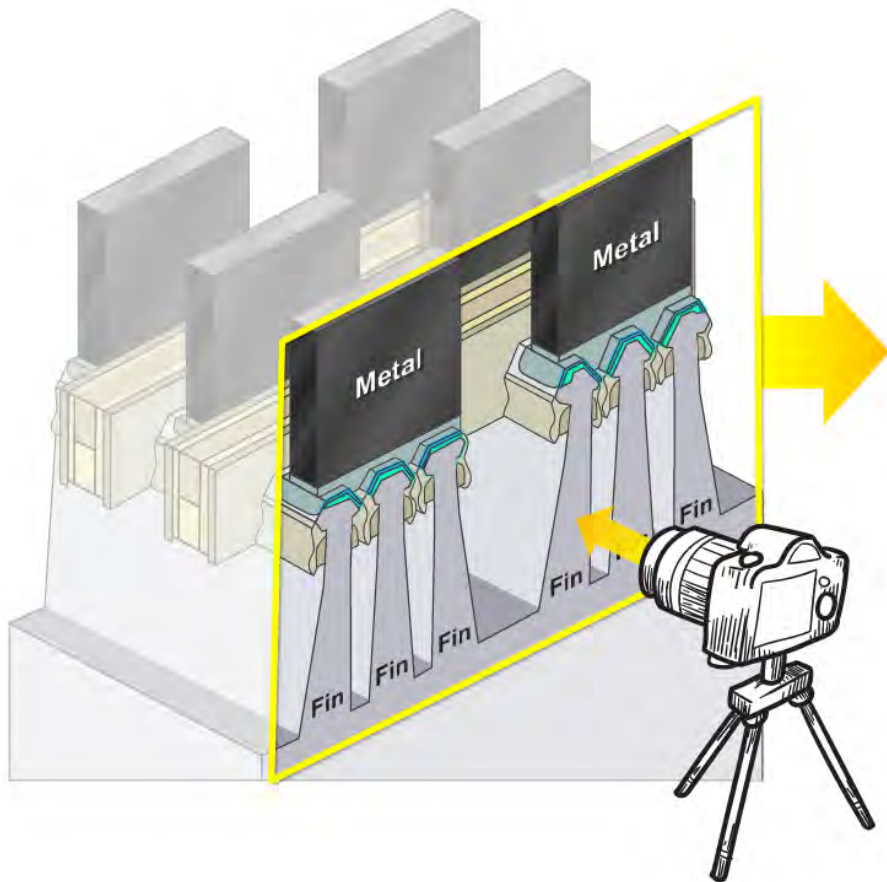
Case 2:19-cv-00347-JRG Document 401-3 Filed 09/02/21 Page 13 of 115 PageID #: 22716

Accused Transistor Devices: 14 nm FinFET



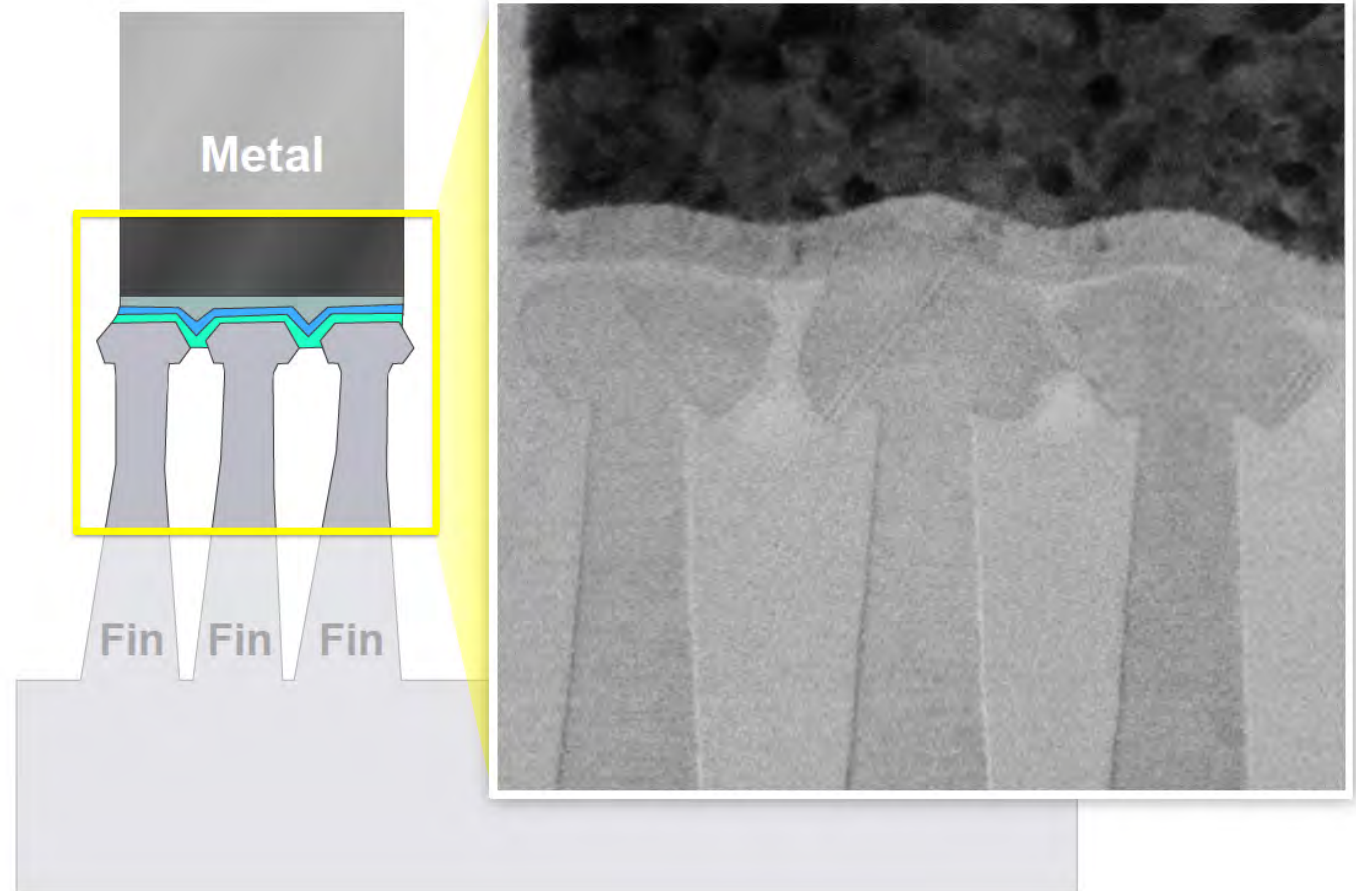
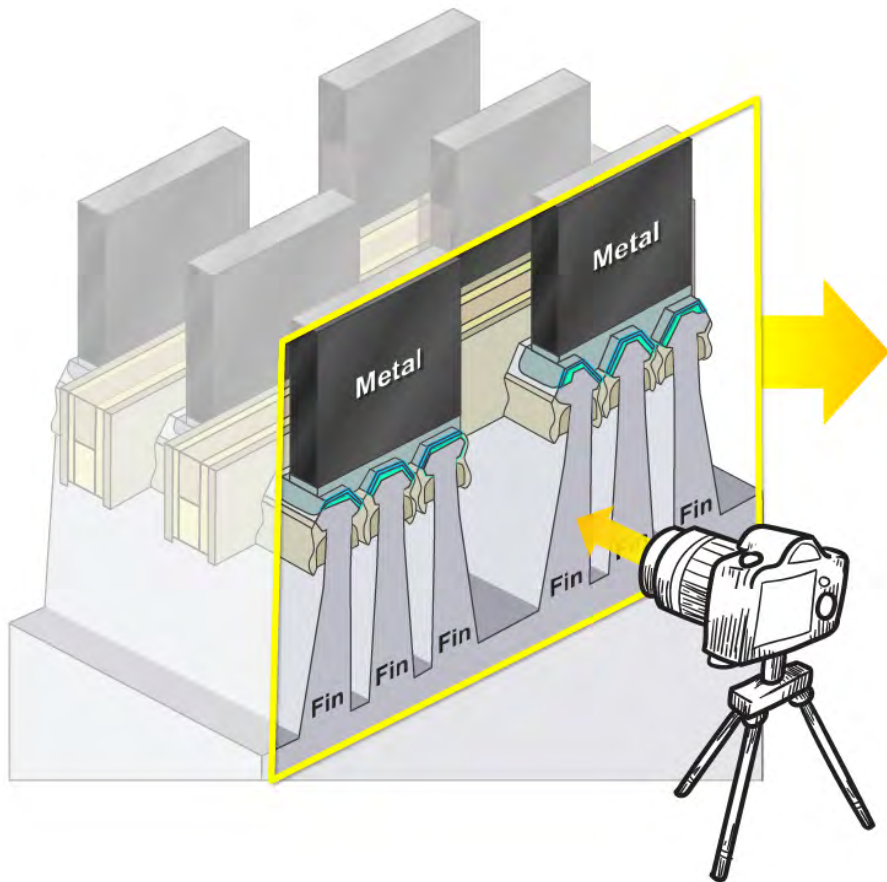
Accused Transistor Devices: 14 nm FinFET

Front View (Y-Cut)



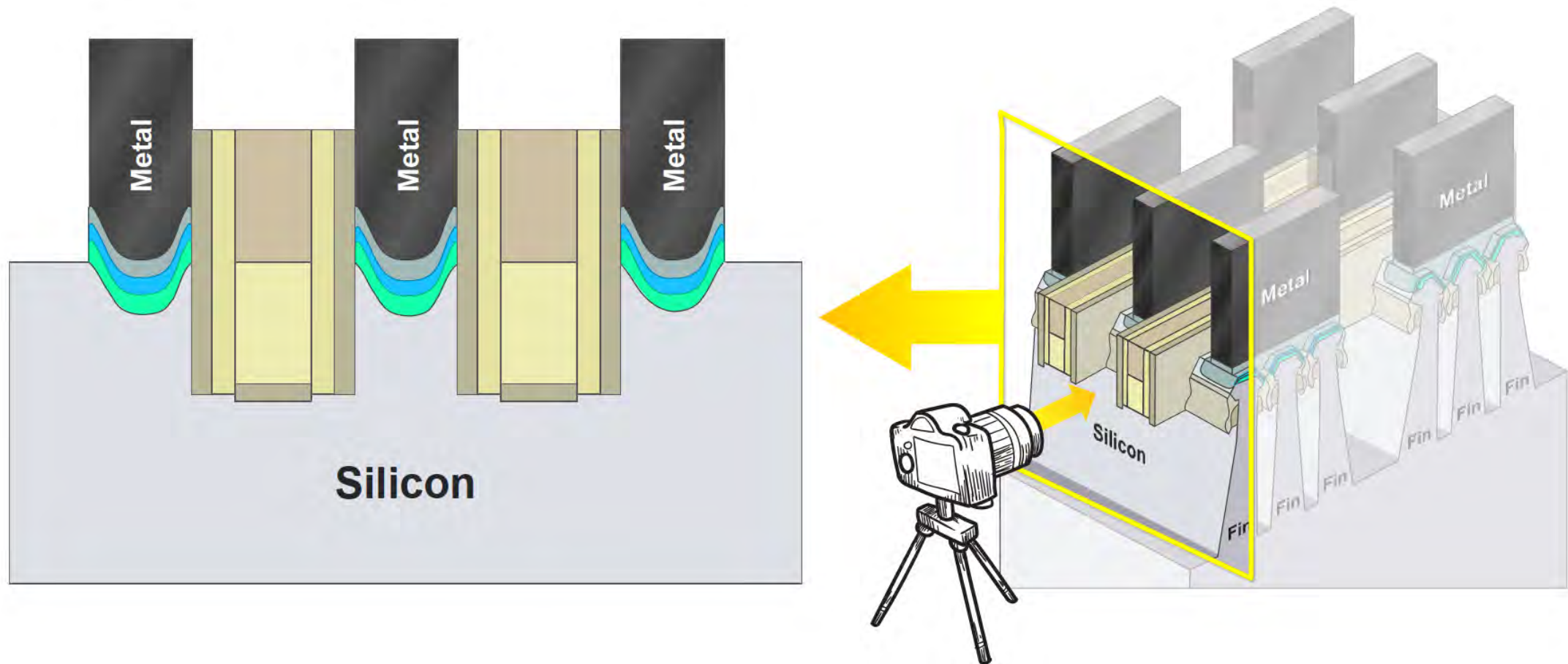
Accused Transistor Devices: 14 nm FinFET

Front View (Y-Cut)



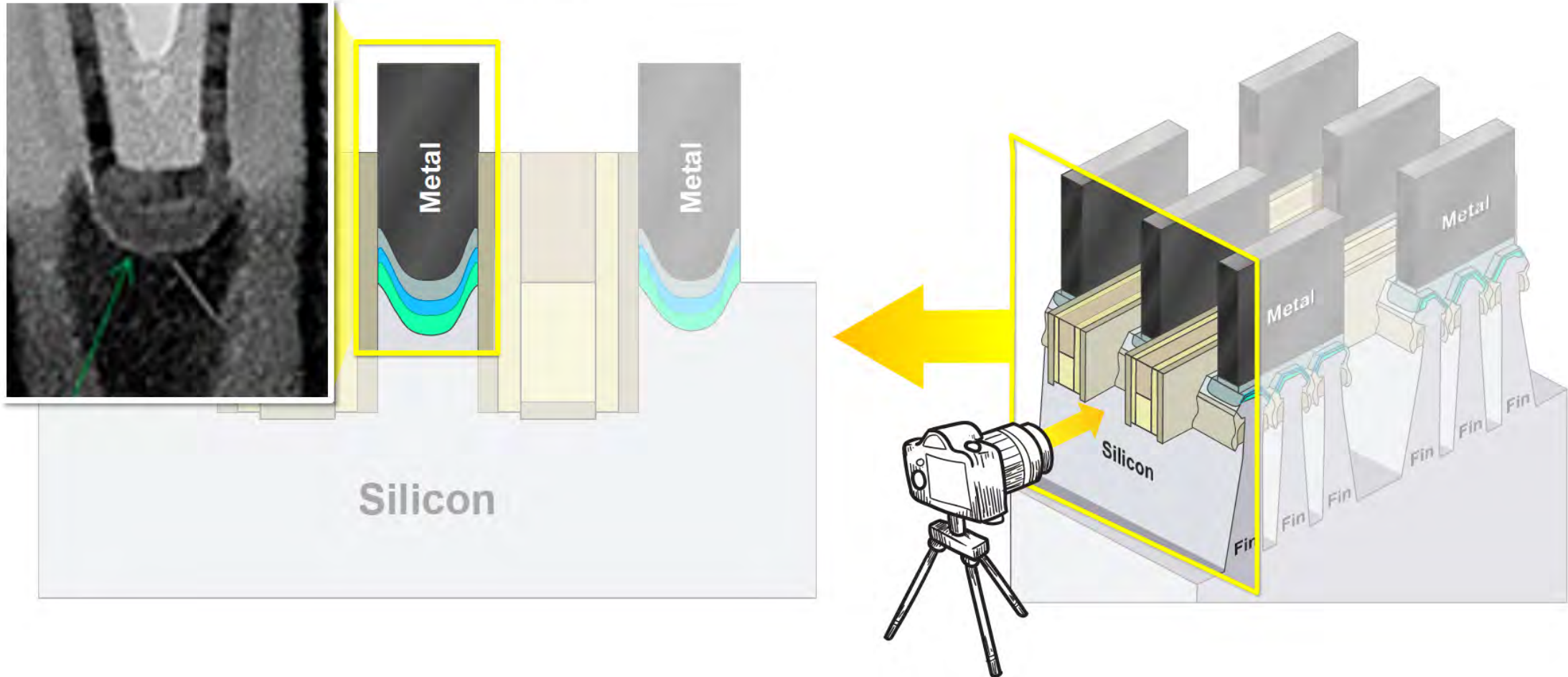
Accused Transistor Devices: 14 nm FinFET

Side View (X-Cut)

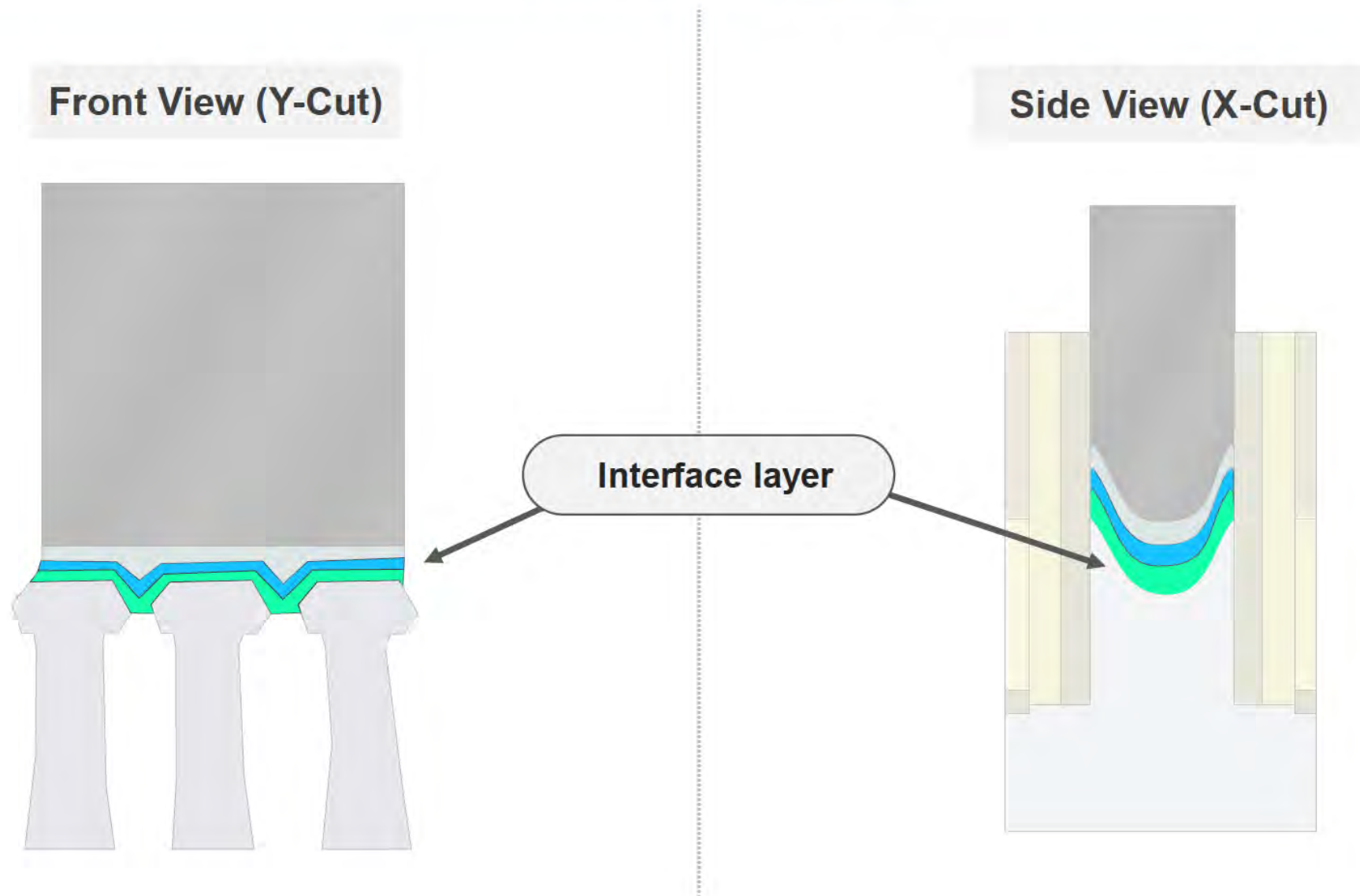


Accused Transistor Devices: 14 nm FinFET

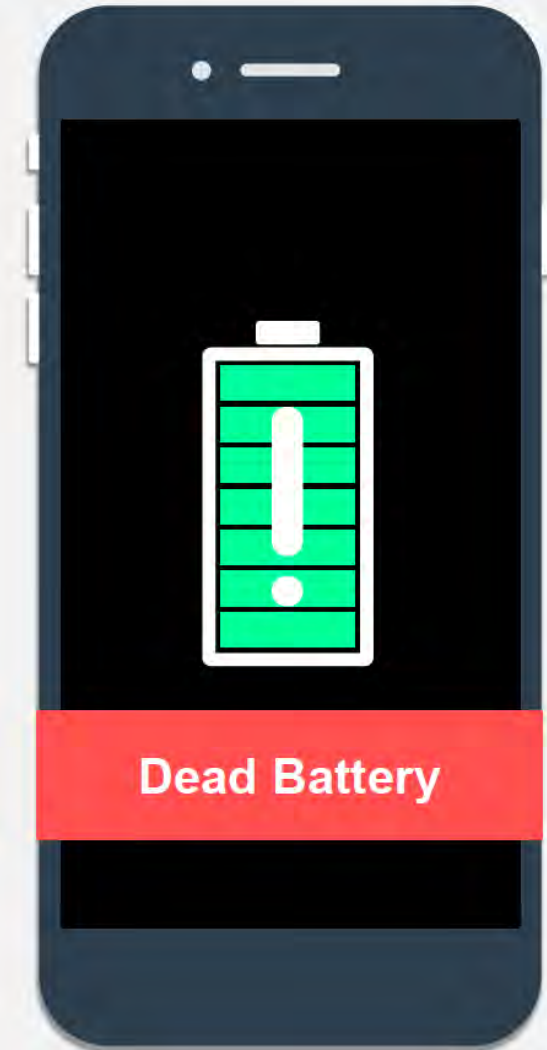
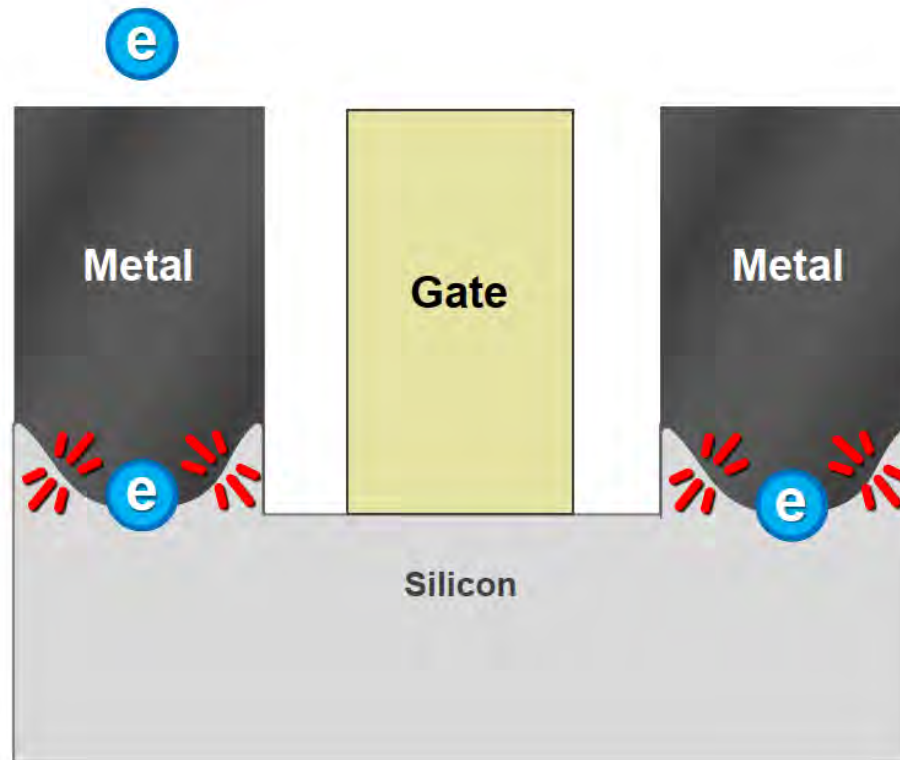
Side View (X-Cut)



Interface Layer



Contact Resistance



14 nm FinFET Process Families

- LPU

- LPP

- LPPM

- LPPS

- LPEM

- LPCM

- LPRF

- LPSM

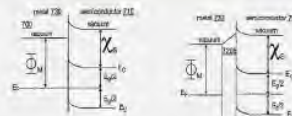
Acorn Patents-in-Suit

'336 Patent

Issued: **July 1, 2014**

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Inventors: **Daniel E. Grupp**, San Francisco, CA (US); **Daniel J. Connelly**, San Francisco, CA (US)



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PTX-01298-2

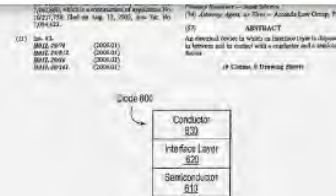
ACORN-SAMSUNG_029101

'167 Patent

Issued: **Oct. 4, 2016**

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Inventors: **Daniel E. Grupp**, San Francisco, CA (US); **Daniel J. Connelly**, San Francisco, CA (US)



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PTX-01164-2

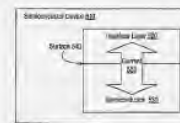
ACORN-SAMSUNG_029102

'691 Patent

Issued: **Feb. 27, 2018**

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Inventors: **Daniel E. Grupp**, San Francisco, CA (US); **Daniel J. Connelly**, San Francisco, CA (US)



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PTX-01306-2

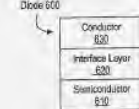
ACORN-SAMSUNG_029103

'395 Patent

Issued: **Oct. 2, 2018**

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Inventors: **Daniel E. Grupp**, San Francisco, CA (US); **Daniel J. Connelly**, San Francisco, CA (US)



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PTX-01368-2

ACORN-SAMSUNG_029104

PTX01298, PTX01304, PTX01308, PTX01306

Claim: 13

ACORN-SAMSUNG 02470

Claims: 1, 6

[illegible]

ACORN-SAMSUNG_025820

Claims: 6, 8, 19

ACORN-SAMSUNG-20802

Claims: 17, 20

Diode 600

Conductor 830
Interface Layer 620
Semiconductor 610

ACORN-SAMSUNG 0205283

Claim Constructions

CLAIM TERM	COURT'S CONTRUCTION
“having a thickness sufficient to depin a Fermi level of the conductor” (’336 Patent, Claim 13)	“displacing the semiconductor from the conductor by a sufficient distance to eliminate or at least reduce the effects of metal-induced gap states in the semiconductor and terminating all or substantially all dangling bonds that may be present at the surface of the semiconductor without the layer present”
“the interface layer comprising a metal oxide and an oxide of the semiconductor” (’167 Patent, Claim 1)	“the interface layer comprising a layer of a metal oxide and a distinct layer of an oxide of the semiconductor”
“said interface layer comprising an oxide of titanium and an oxide of the semiconductor” (’395 Patent, Claim 17)	“said interface layer comprising a layer of an oxide of titanium and a distinct layer of an oxide of the semiconductor”
“a metal oxide layer, and a passivating dielectric tunnel barrier layer” (’691 Patent, Claim 1)	“a metal oxide layer, and a distinct dielectric tunnel barrier layer that terminates all or substantially all dangling bonds that may be present at the surface of the semiconductor region without the layer present”

Devices Analyzed

Processor Name	Device	Date Manufactured	14nm Process Family	RF Etch Step
A9	iPhone 6s Plus	2015	LPE	Yes
Exynos 7420	Samsung Galaxy S6	2015	LPEM	Yes
Exynos 7880	Samsung Galaxy A7	2017	LPPM	Yes
Exynos 8890	Samsung Galaxy S7	2016	LPPM	Yes
Exynos 7885	Samsung Galaxy A8	2018	LPSM	No
Exynos 7570	Samsung Galaxy J2 Core	2018	LPCM	Yes
Exynos 7904	Samsung Galaxy A30	2019	LPCM	No
Exynos 7884	Samsung Galaxy M10	2019	LPCM	No
Nvidia GP108	PNY Nvidia GEFORCE GT 1030 Graphics Card	2020	LPPS	No
Nvidia P1000	Dell Precision 7530 Nvidia Quadro P1000 - 4GD86	2018	LPP	No

Acorn Patents-in-Suit

'336 Patent

Claims: 13



'167 Patent

Claims: 1, 6



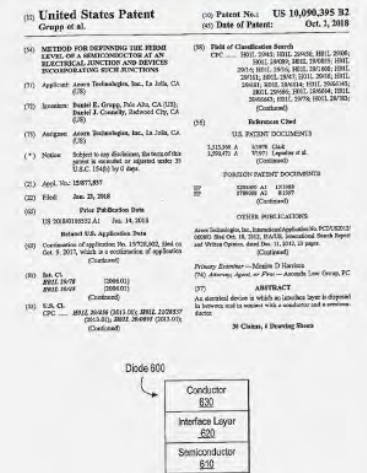
'691 Patent

Claims: 6, 8, 19



'395 Patent

Claims: 17, 20



PTX01298, PTX01304, PTX01308, PTX01306

395 Patent: Claims 17 and 20

- ☐ **[17a]** An electrical junction comprising:
-
- a source or drain of a transistor, said source or drain comprising a semiconductor,
-
- a metal electrical contact to said source or drain, and
-
- an interface layer disposed between and in contact with said source or drain and said metal electrical contact,

- ☐ **[17b]** said source or drain being electrically connected to said metal electrical contact through said interface layer and

- ☐ **[17c]** said interface layer comprising an oxide of titanium and an oxide of the semiconductor.

-
- ☐ **[20]** The electrical junction of claim 17, wherein said metal electrical contact includes tungsten.

395 Patent: Claims 17 and 20

☐

[17a] An electrical junction comprising:

a source or drain of a transistor, said source or drain comprising a semiconductor,

a metal electrical contact to said source or drain, and

an interface layer disposed between and in contact with said source or drain and said metal electrical contact,

☐

[17b] said source or drain being electrically connected to said metal electrical contact through said interface layer and

☐

[17c] said interface layer comprising an oxide of titanium and an oxide of the semiconductor.

☐

[20] The electrical junction of claim 17, wherein said metal electrical contact includes tungsten.

Teardown of Samsung Galaxy A7



Front (glass)

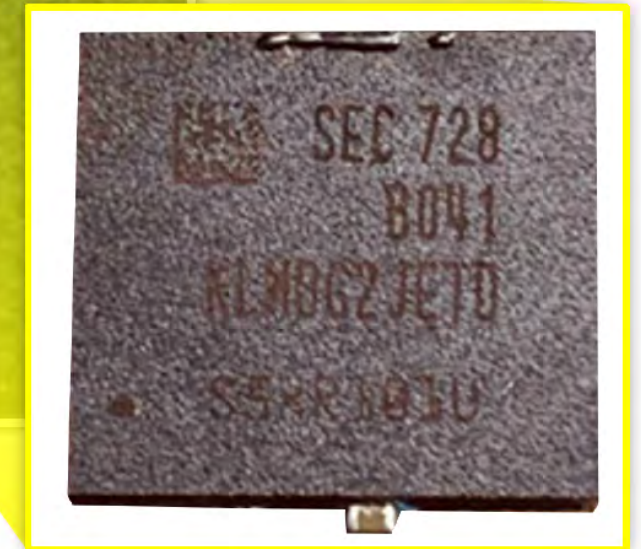
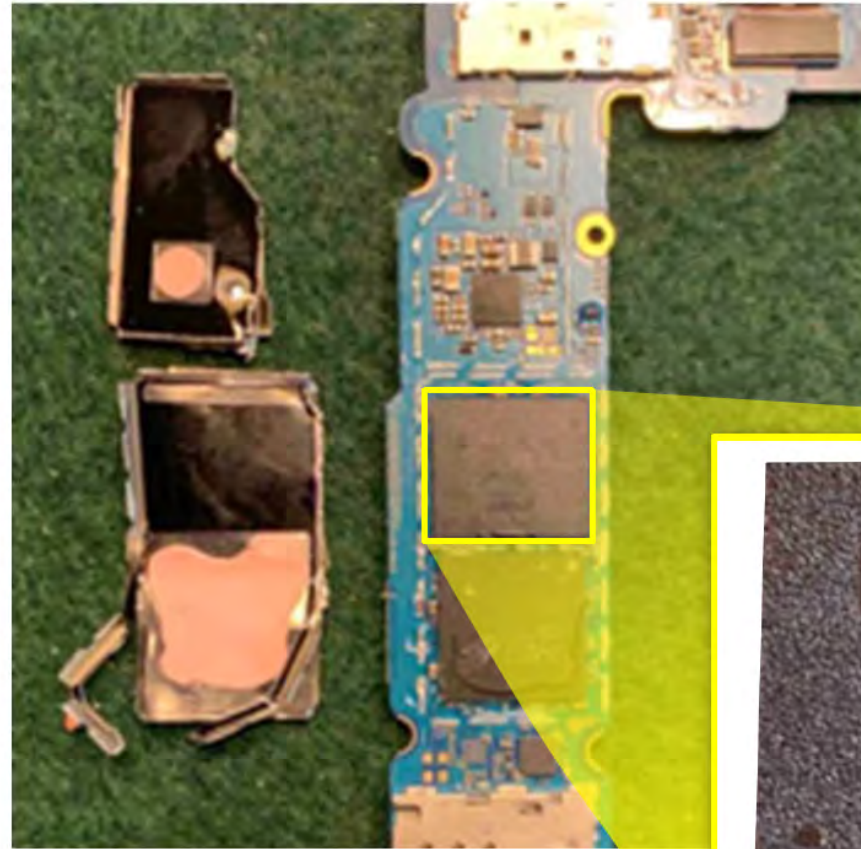


Back (glass)

Tear-down of Samsung Galaxy A7



Midframe separated



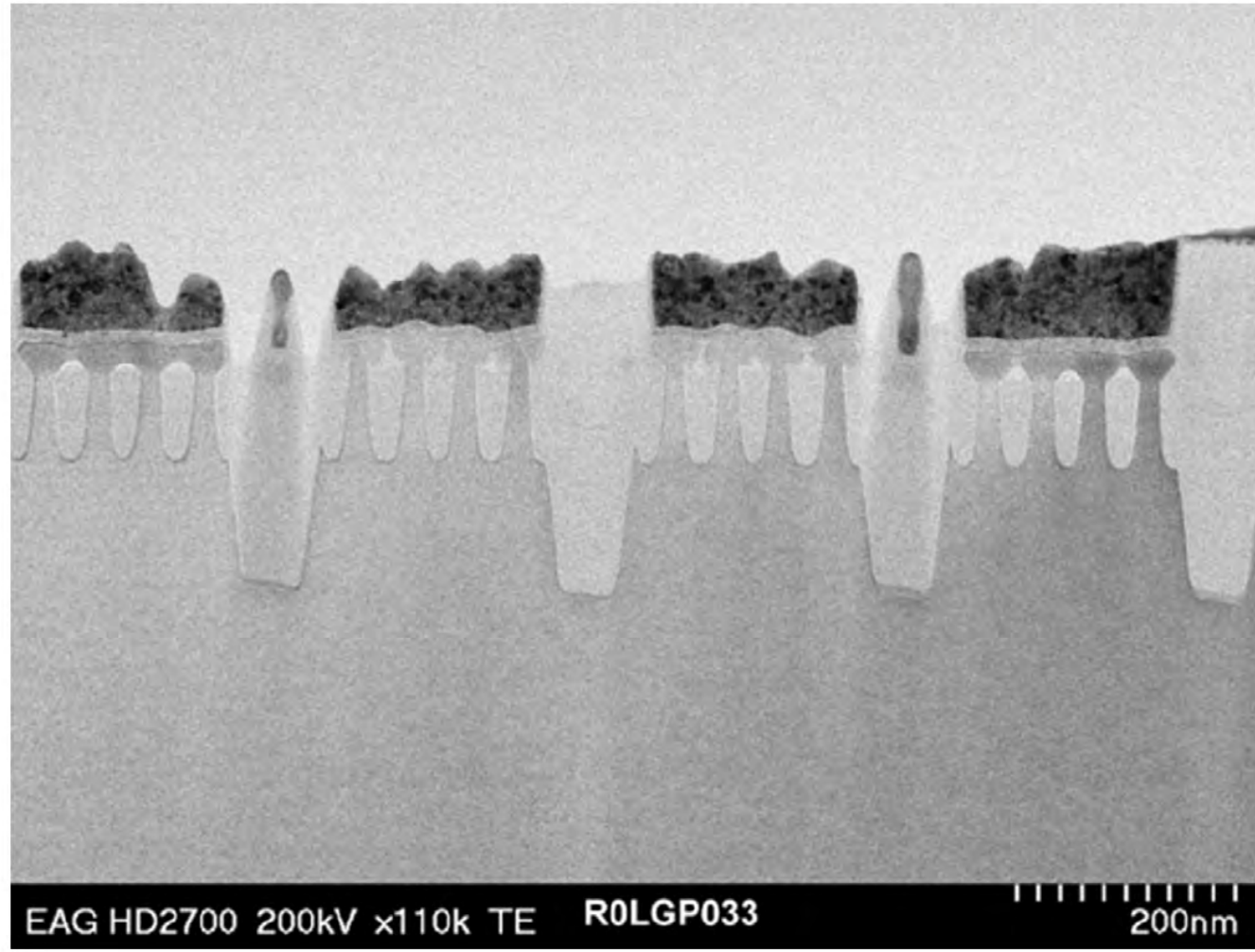
Chip removed

Analysis Machines



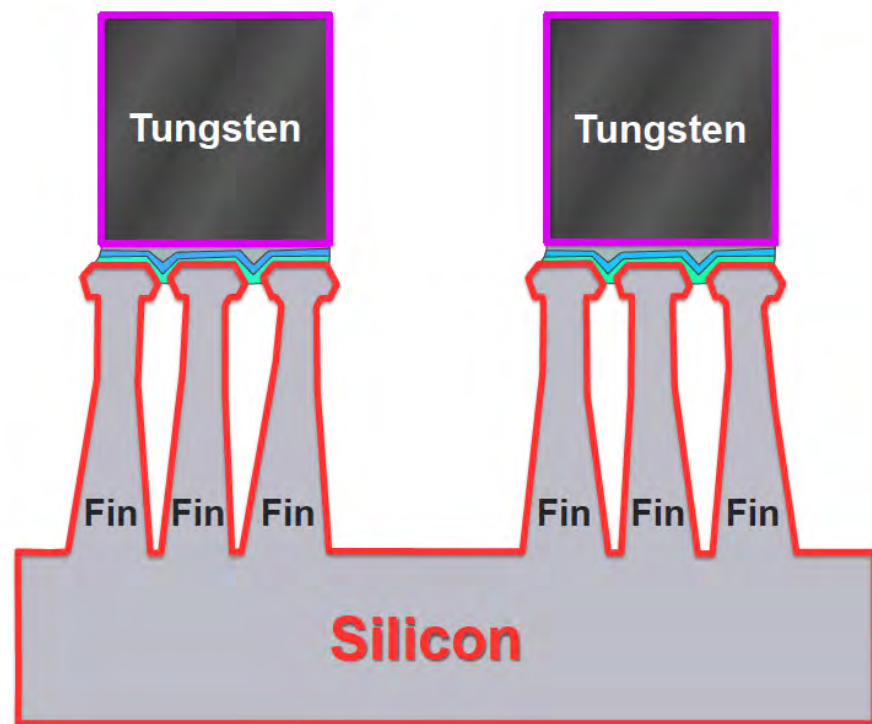
TEM Imaging of Exynos 7880

Actual Samsung Transistor

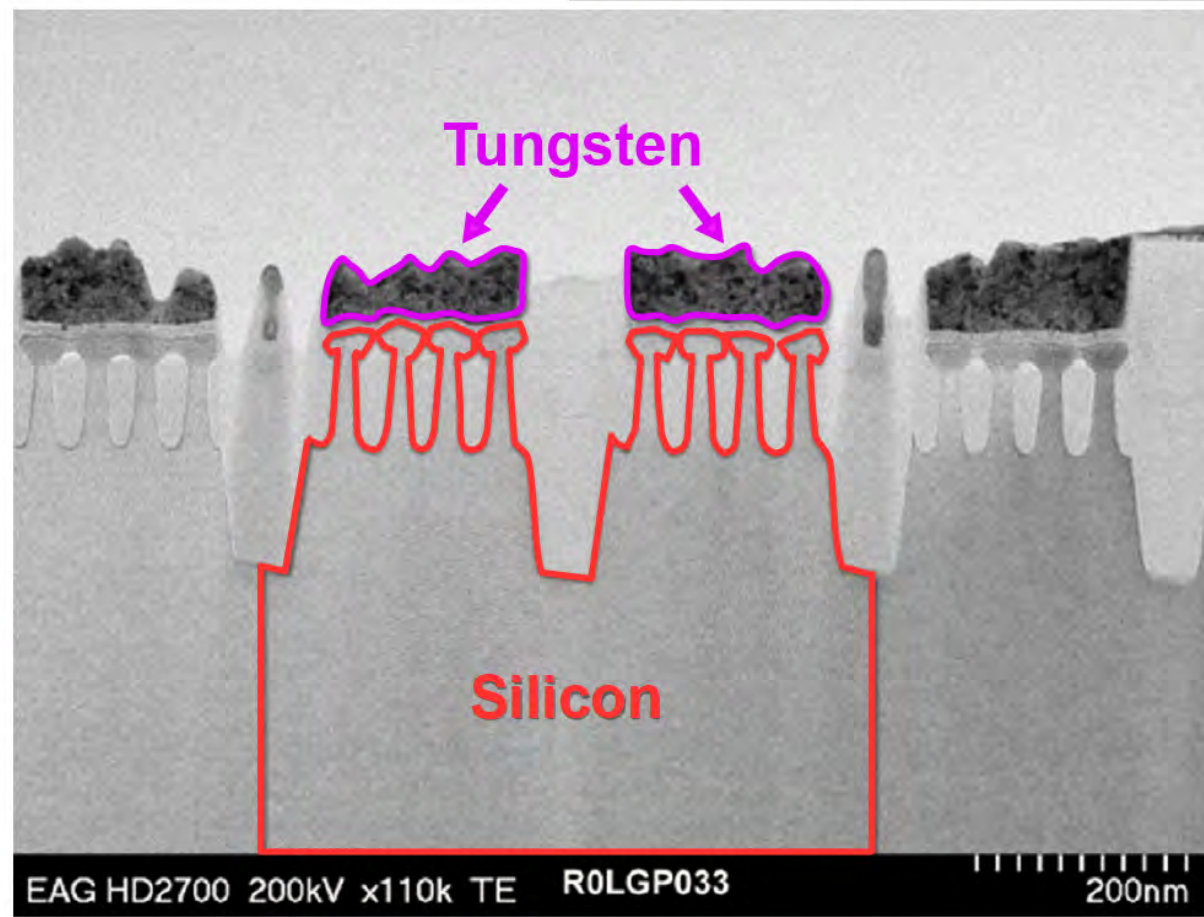


PTX00373-68

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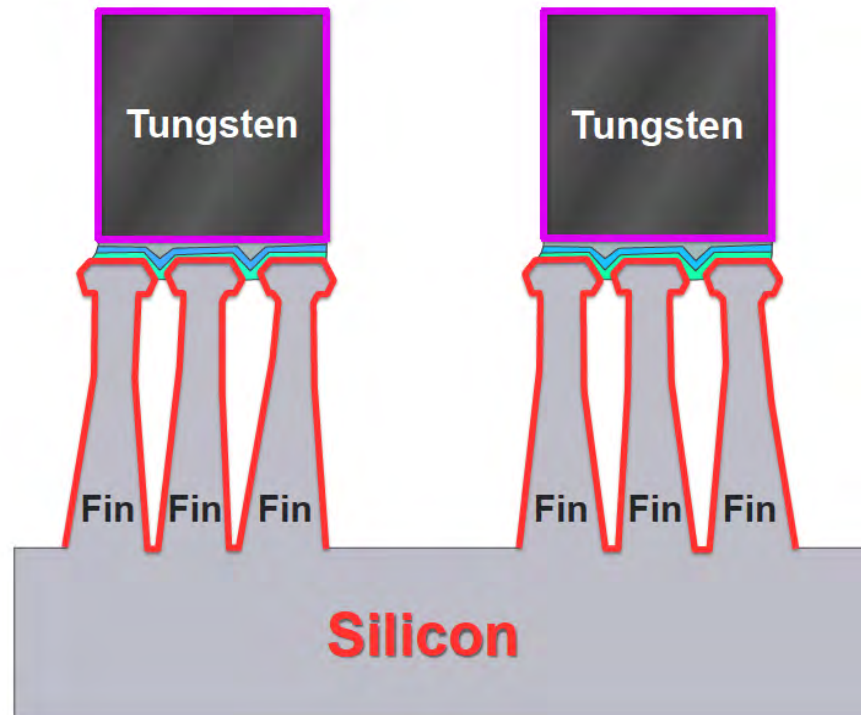


Actual Samsung Transistor

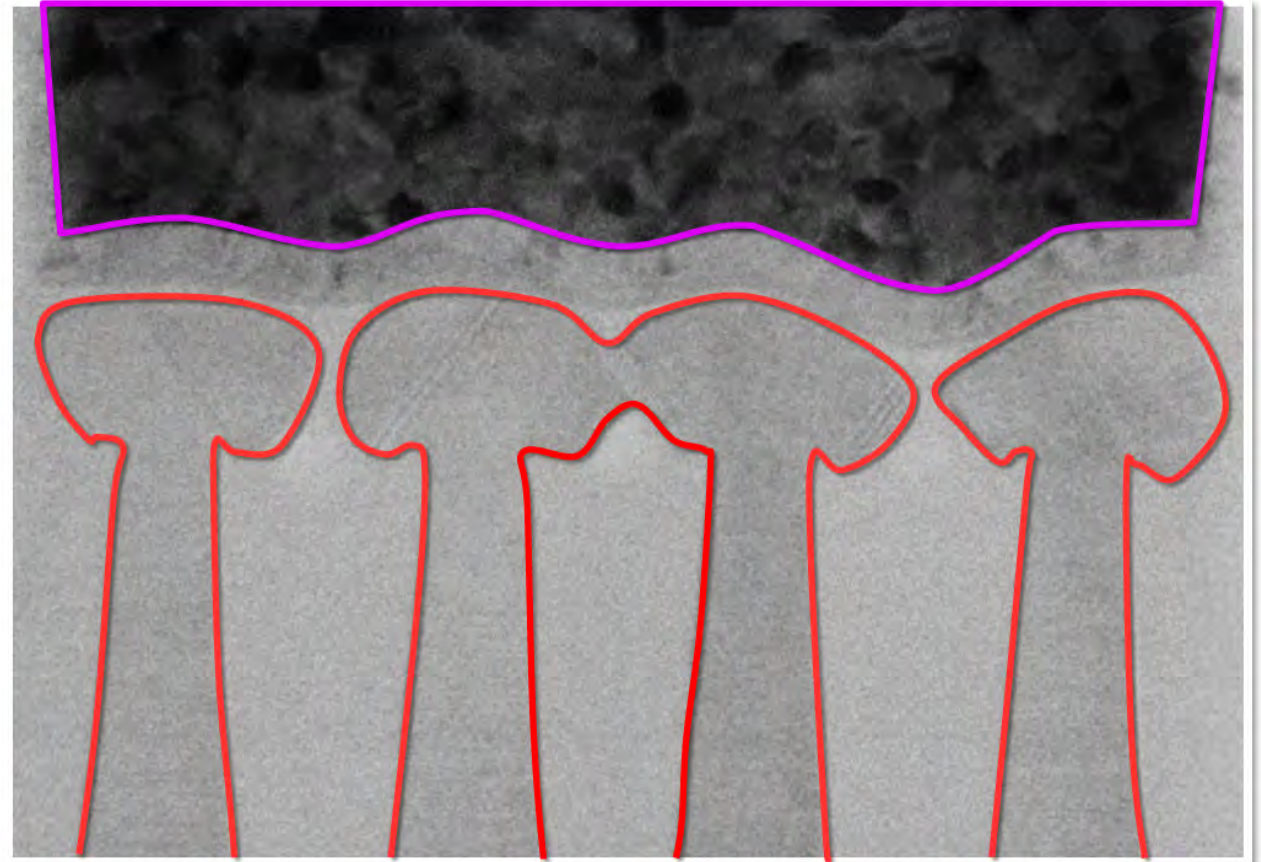


PTX00373-68

TEM Imaging of Accused Device

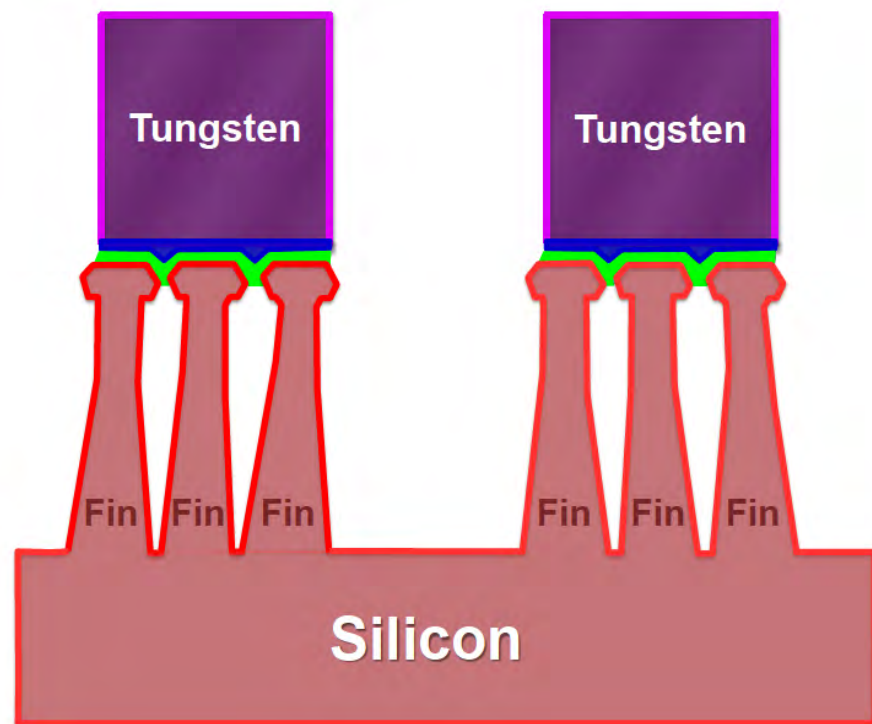


Actual Samsung Transistor

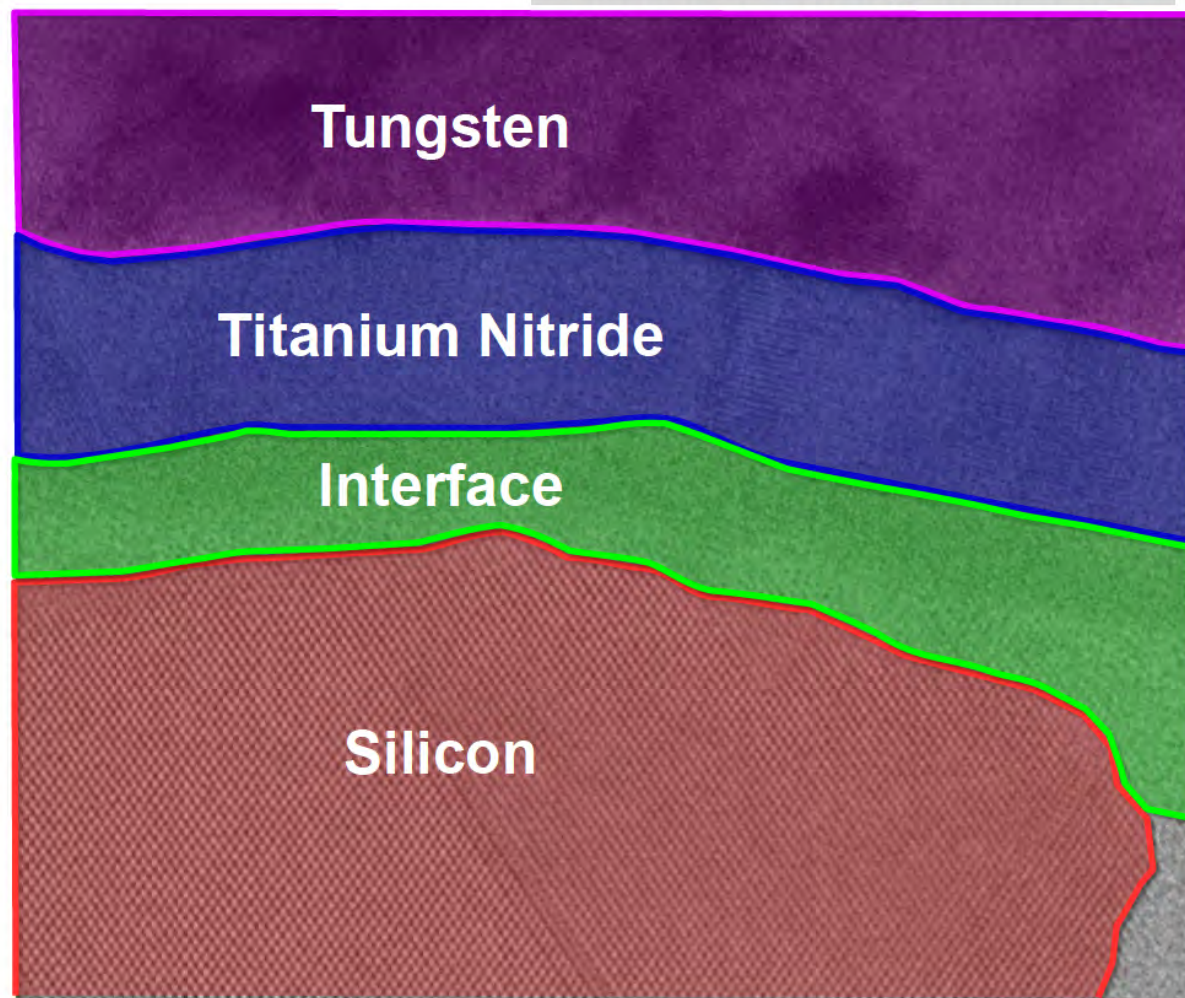


PTX00373-69

TEM Imaging of Accused Device



Actual Samsung Transistor



PTX00373-70

33

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Claim 17[a]: Interface Layer Between Metal and Semiconductor

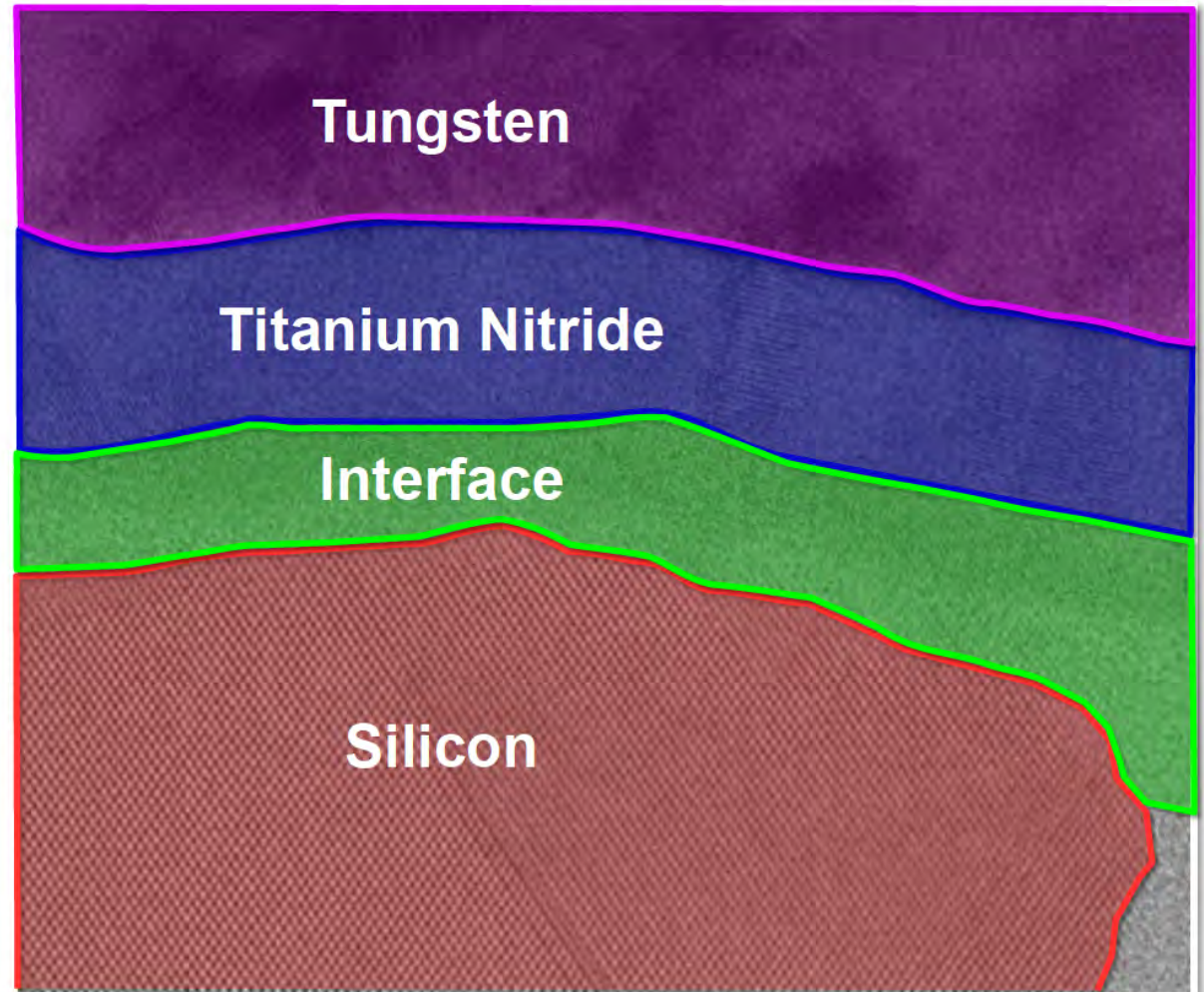
[17a] An electrical junction comprising:

a source or drain of a transistor, said source or drain comprising a semiconductor,

a metal electrical contact to said source or drain, and

an interface layer disposed between and in contact with said source or drain and said metal electrical contact,

Actual Samsung Transistor



PTX00373-70

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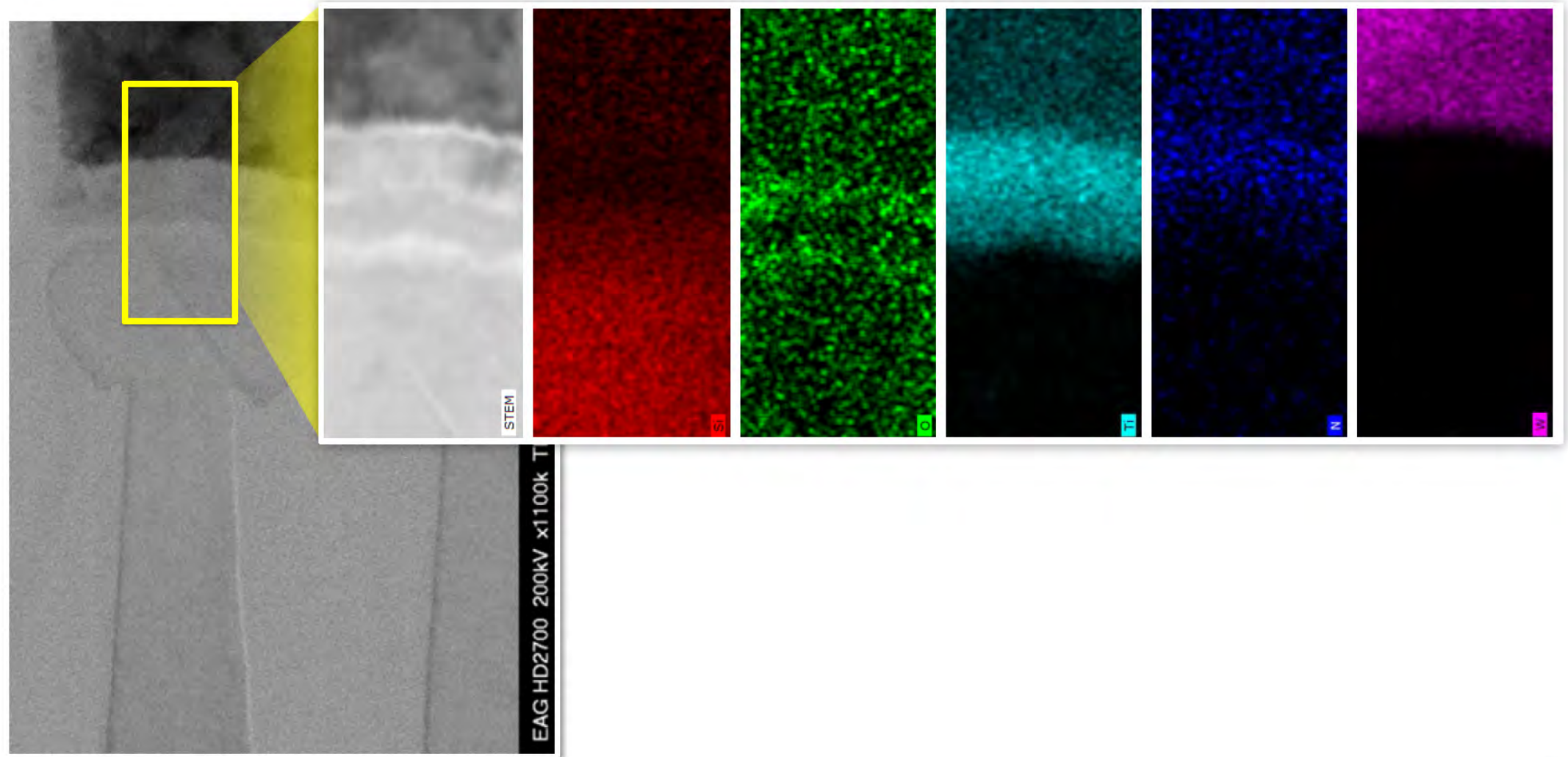
Elemental Analysis of Exynos 7880



PTX00373

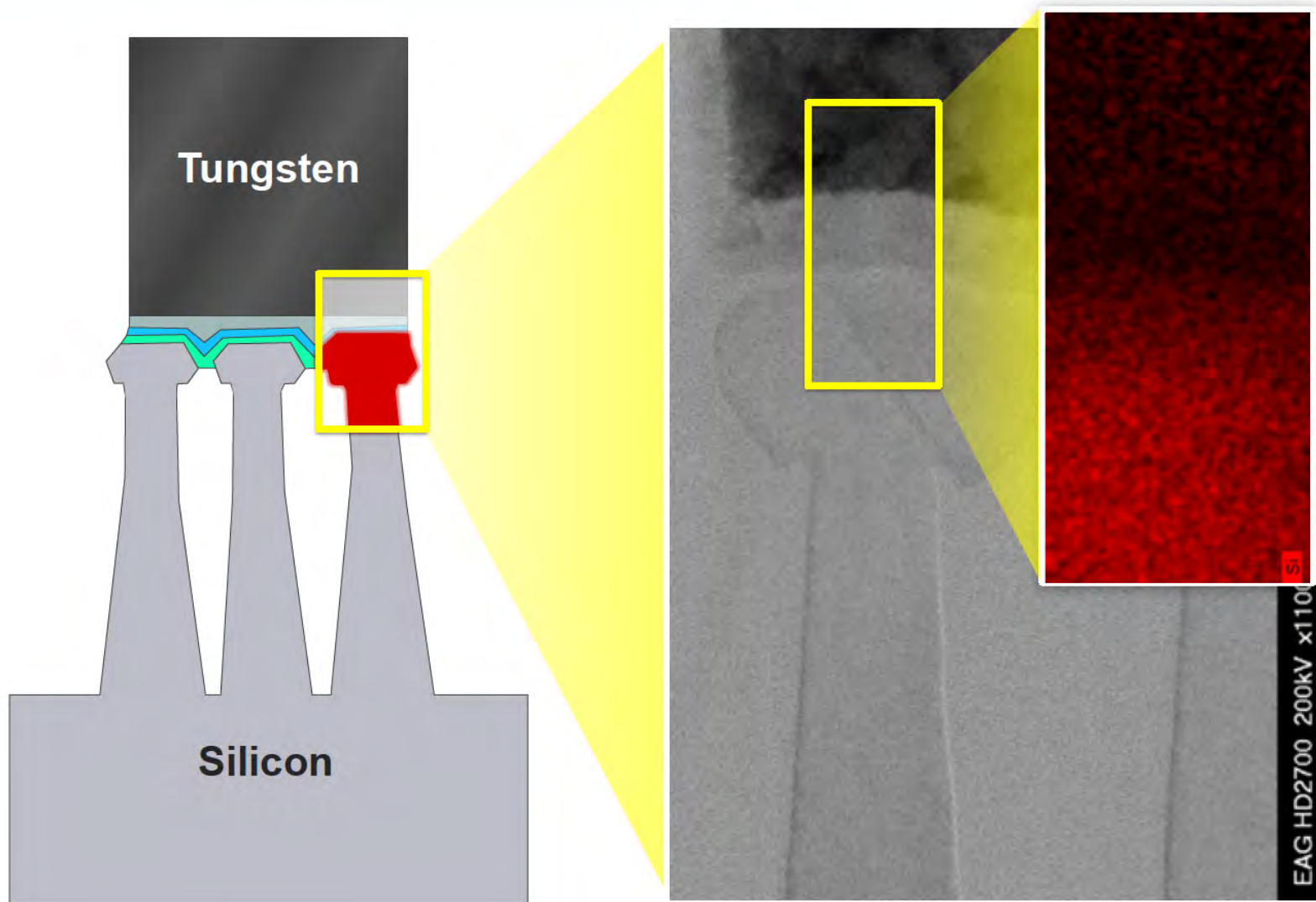
Case 2:19-cv-00347-JRG Document 401-3 Filed 09/02/21 Page 37 of 115 PageID #: 22740

Elemental Analysis of Exynos 7880



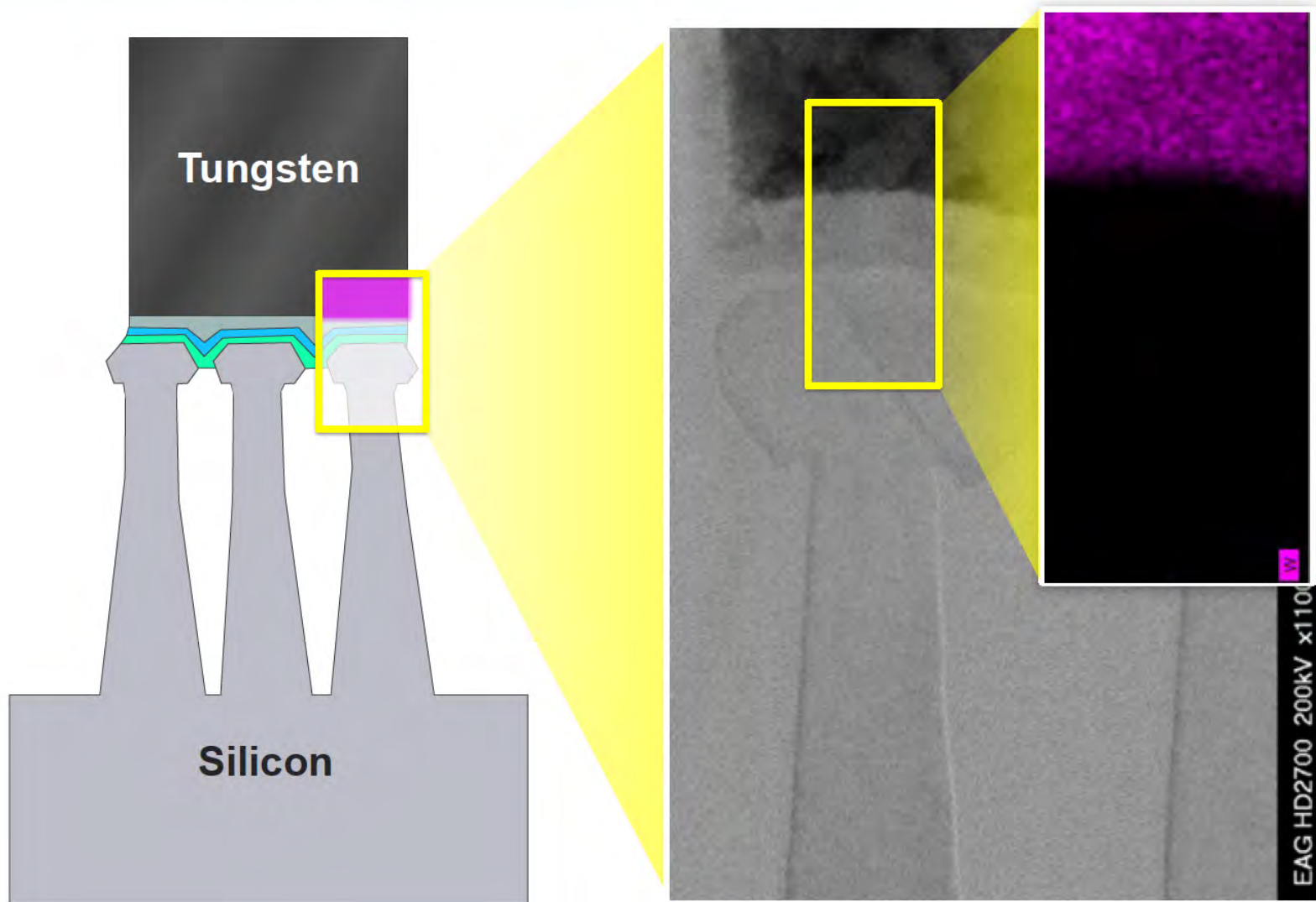
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Elemental Analysis: Silicon



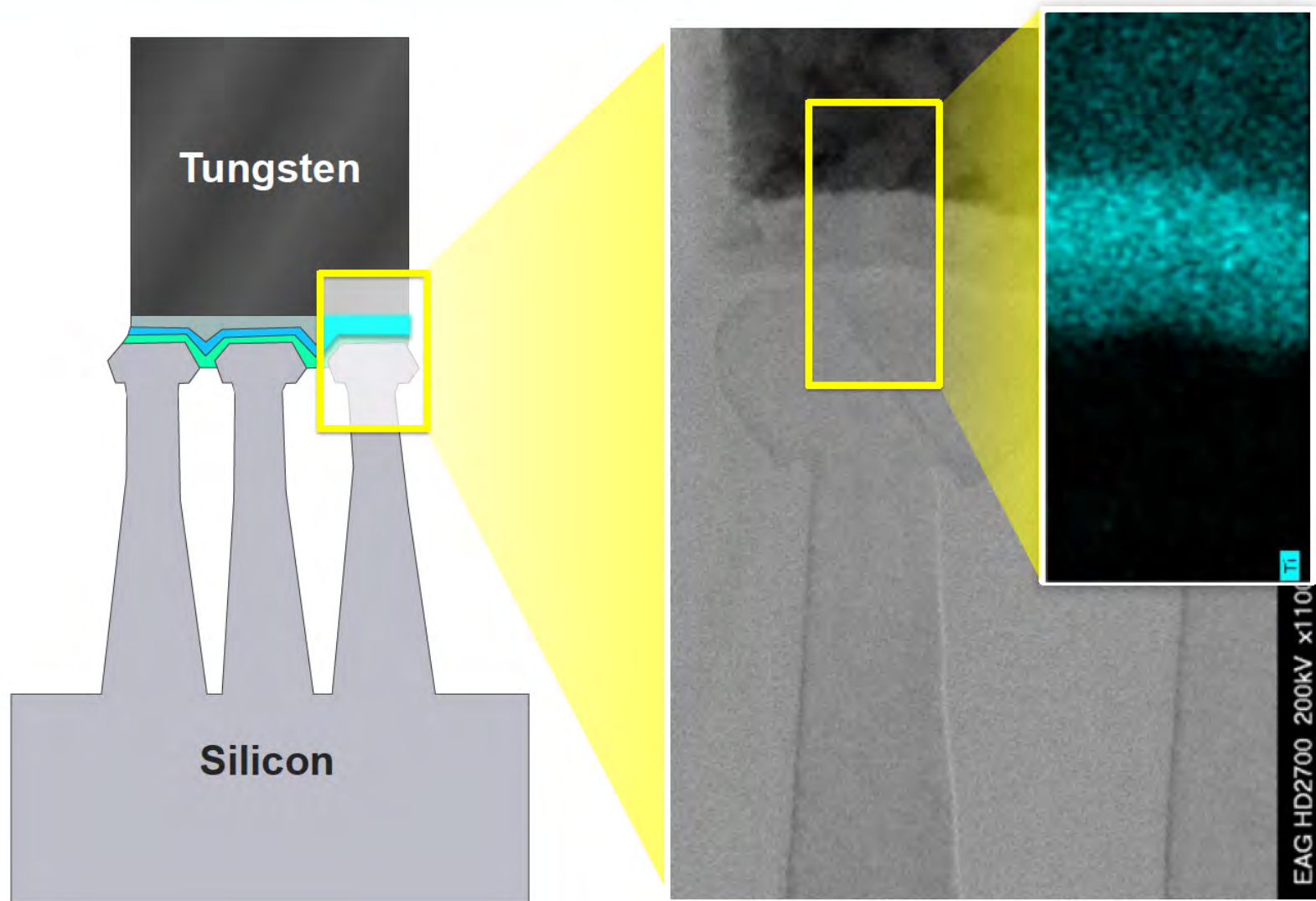
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Elemental Analysis: Tungsten



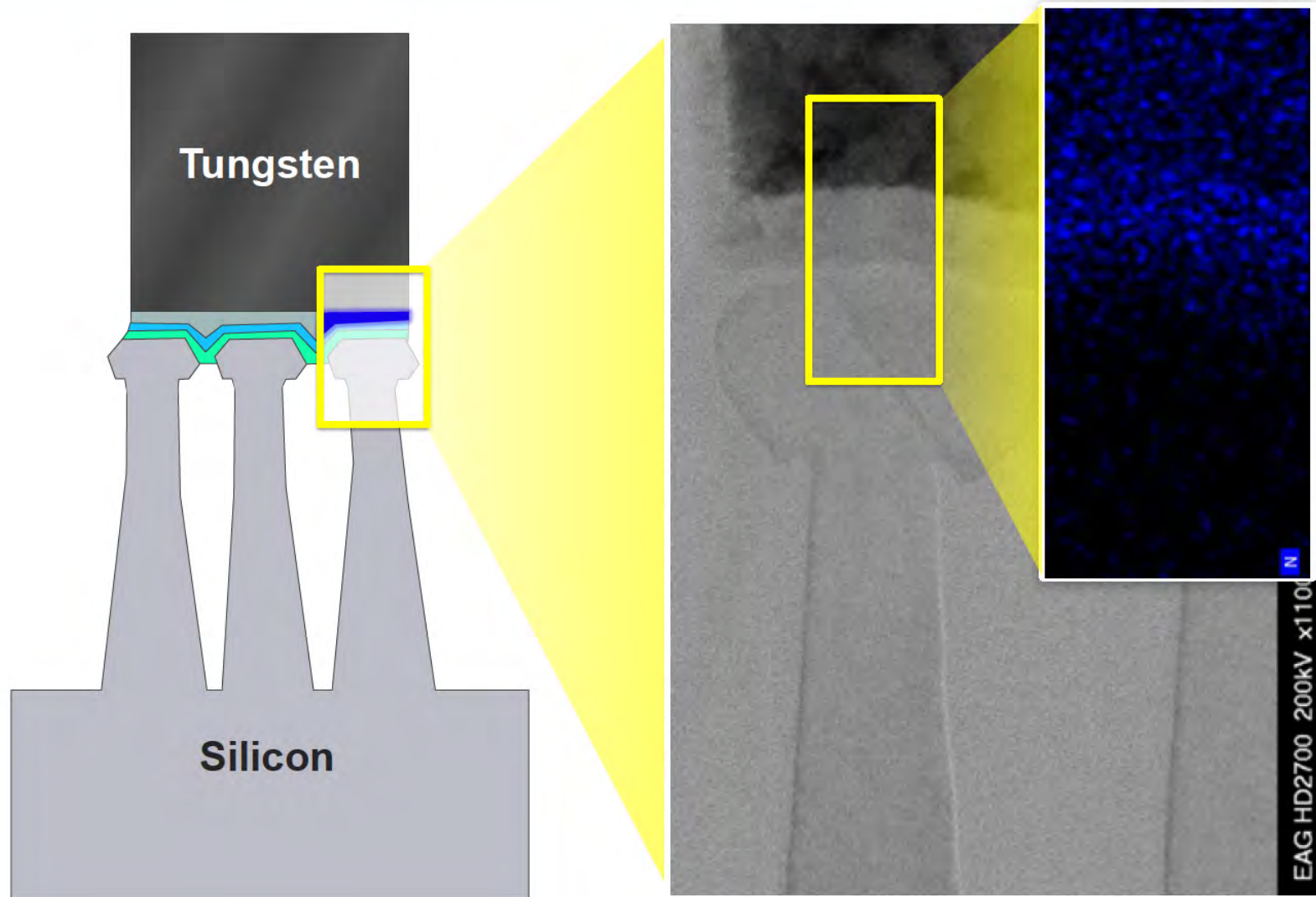
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Elemental Analysis: Titanium



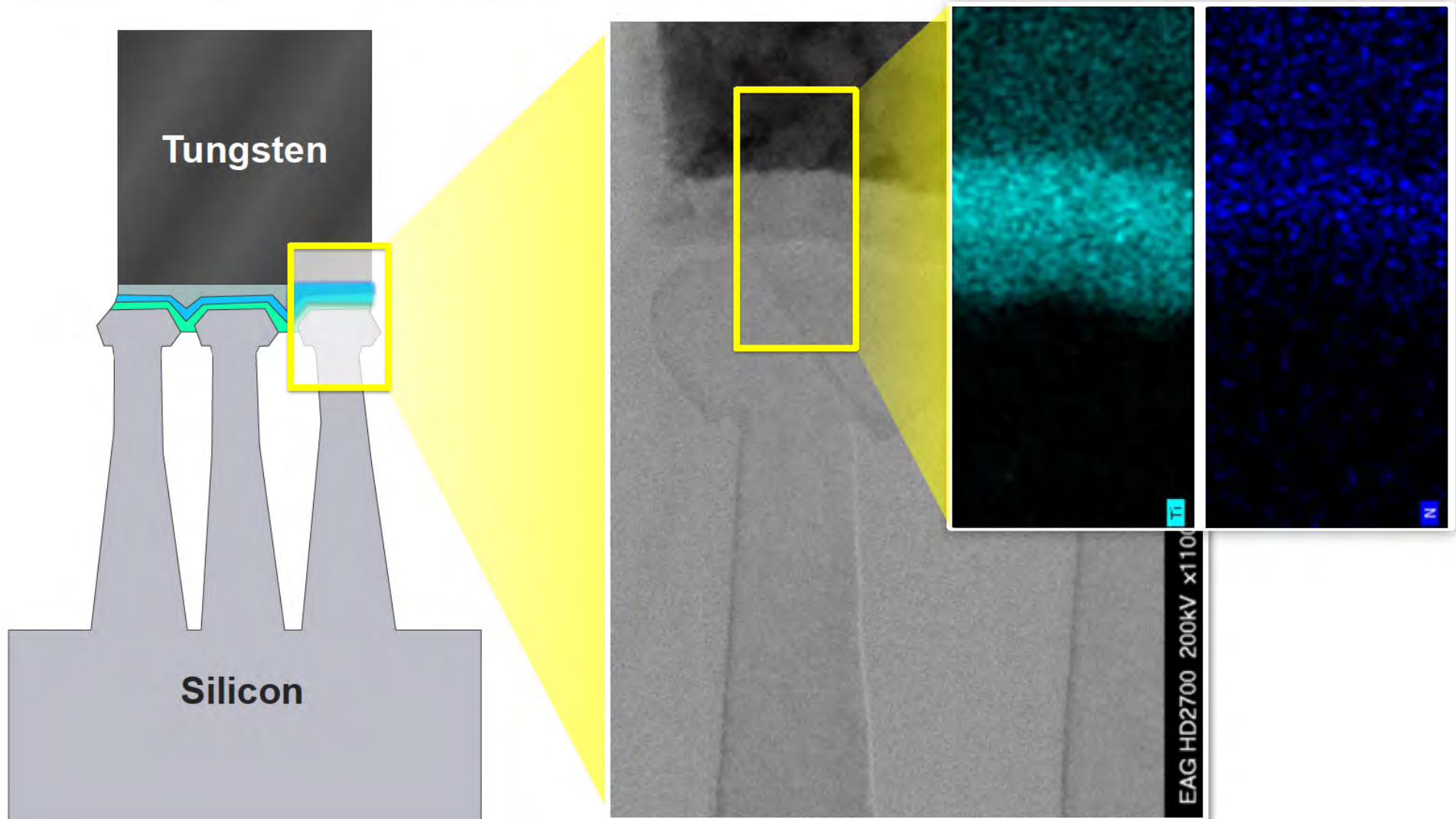
PTX00373-72

Elemental Analysis: Nitrogen



PTX00373-72

Elemental Analysis: Layer of Titanium Nitride



PTX00373-72

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Claim 17[a]: Interface Layer Between Metal and Semiconductor

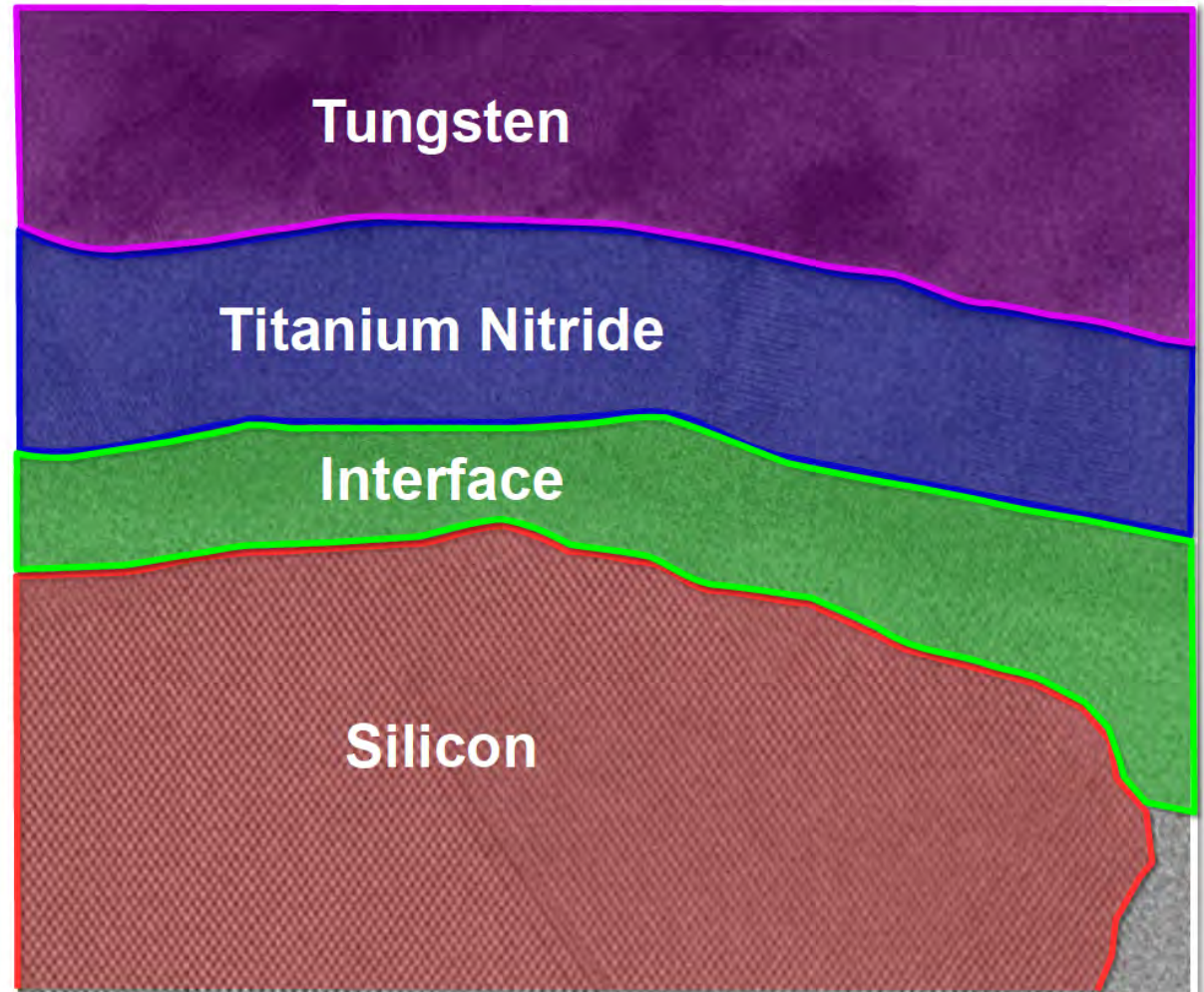
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an interface layer disposed between and in contact with said source or drain and said metal electrical contact,

Actual Samsung Transistor



PTX00373-70

395 Patent: Claims 17 and 20



[17a] An electrical junction comprising:

a source or drain of a transistor, said source or drain comprising a semiconductor,

a metal electrical contact to said source or drain, and

an interface layer disposed between and in contact with said source or drain and said metal electrical contact,



[17b] said source or drain being electrically connected to said metal electrical contact through said interface layer and



[17c] said interface layer comprising an oxide of titanium and an oxide of the semiconductor.



[20] The electrical junction of claim 17, wherein said metal electrical contact includes tungsten.

395 Patent: Claims 17 and 20



[17a] An electrical junction comprising:

a source or drain of a transistor, said source or drain comprising a semiconductor,

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an interface layer disposed between and in contact with said source or drain and said metal electrical contact,



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395 Patent: Claims 17 and 20



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395 Patent: Claims 17 and 20



[17a] An electrical junction comprising:

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[17b] said source or drain being electrically connected to said metal electrical contact through said interface layer and



[17c] said interface layer comprising an oxide of titanium and an oxide of the semiconductor.



[20] The electrical junction of claim 17, wherein said metal electrical contact includes tungsten.

Claim Constructions

CLAIM TERM	COURT'S CONTRUCTION
“having a thickness sufficient to depin a Fermi level of the conductor” ('336 Patent, Claims 13)	“displacing the semiconductor from the conductor by a sufficient distance to eliminate or at least reduce the effects of metal-induced gap states in the semiconductor and terminating all or substantially all dangling bonds that may be present at the surface of the semiconductor without the layer present”
“the interface layer comprising a metal oxide and an oxide of the semiconductor” ('167 Patent, Claim 1)	“the interface layer comprising a layer of a metal oxide and a distinct layer of an oxide of the semiconductor”
“said interface layer comprising an oxide of titanium and an oxide of the semiconductor” ('395 Patent, Claim 17)	“said interface layer comprising a layer of an oxide of titanium and a distinct layer of an oxide of the semiconductor”
“a metal oxide layer, and a passivating dielectric tunnel barrier layer” ('691 Patent, Claim 1)	“a metal oxide layer, and a distinct dielectric tunnel barrier layer that terminates all or substantially all dangling bonds that may be present at the surface of the semiconductor region without the layer present”

395 Patent: Claims 17 and 20



[17a] An electrical junction comprising:

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[17b] said source or drain being electrically connected to said metal electrical contact through said interface layer and

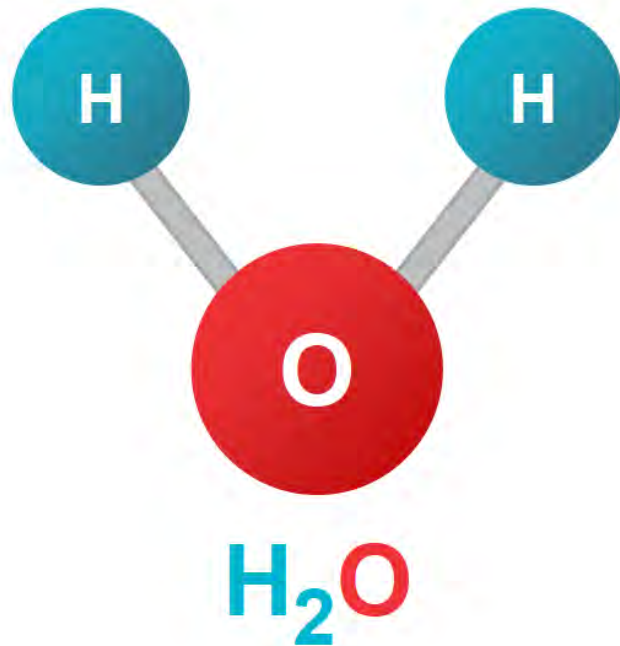


[17c] said interface layer comprising **a layer of** an oxide of titanium and **a distinct layer of** an oxide of the semiconductor.

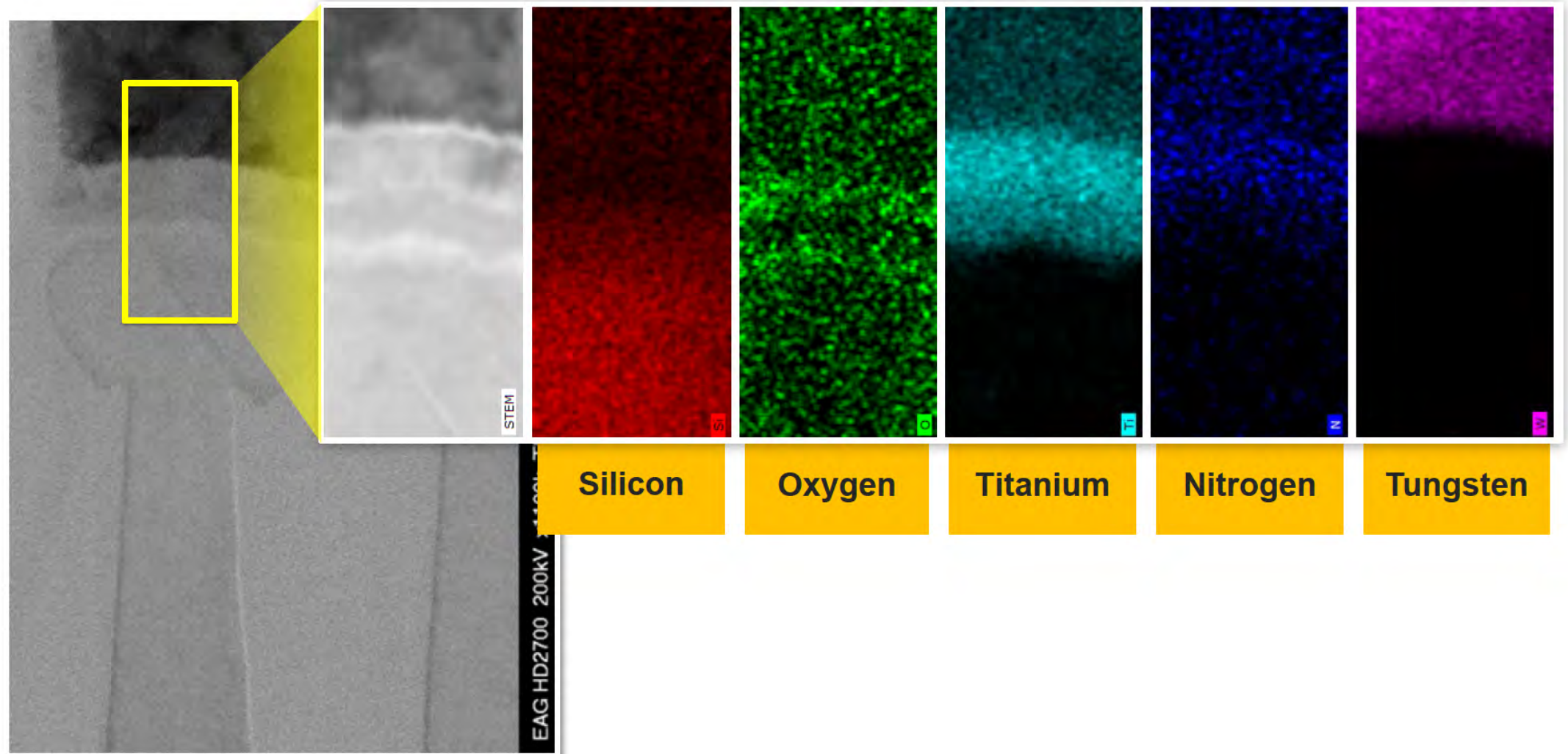


[20] The electrical junction of claim 17, wherein said metal electrical contact includes tungsten.

Oxides

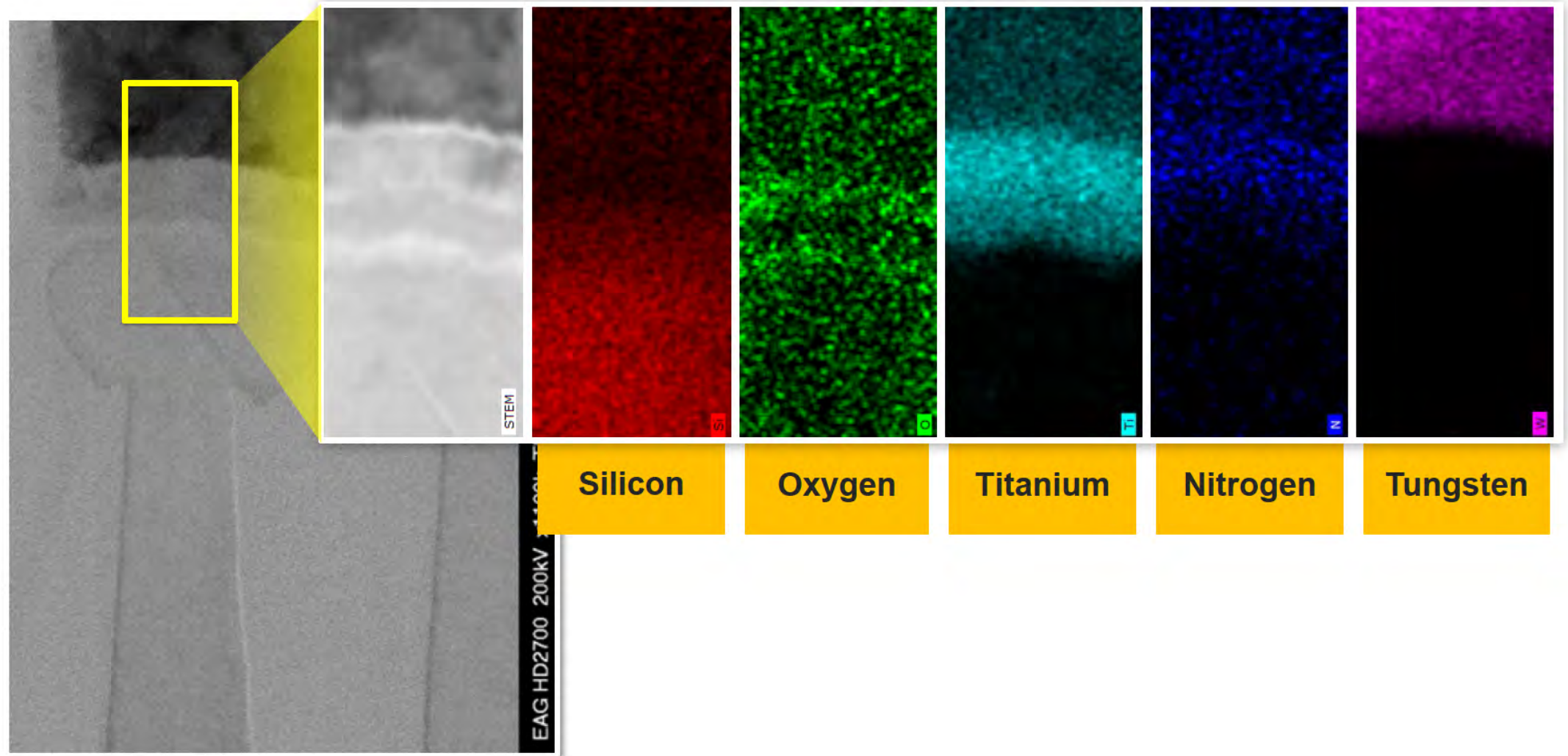


Layer of Silicon Oxide



PTX00373-72

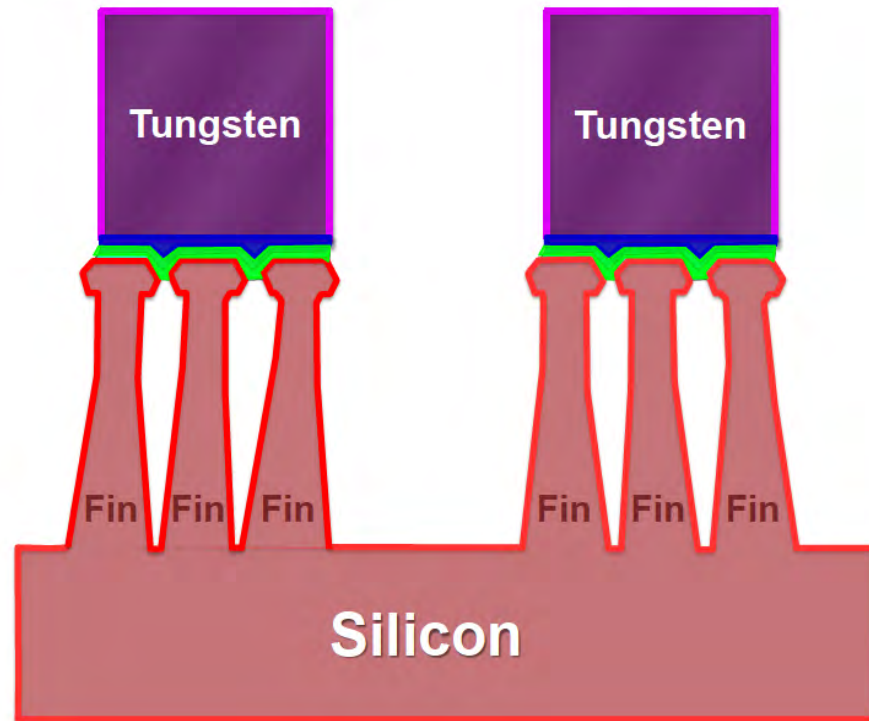
Layer of Titanium Silicon Oxide



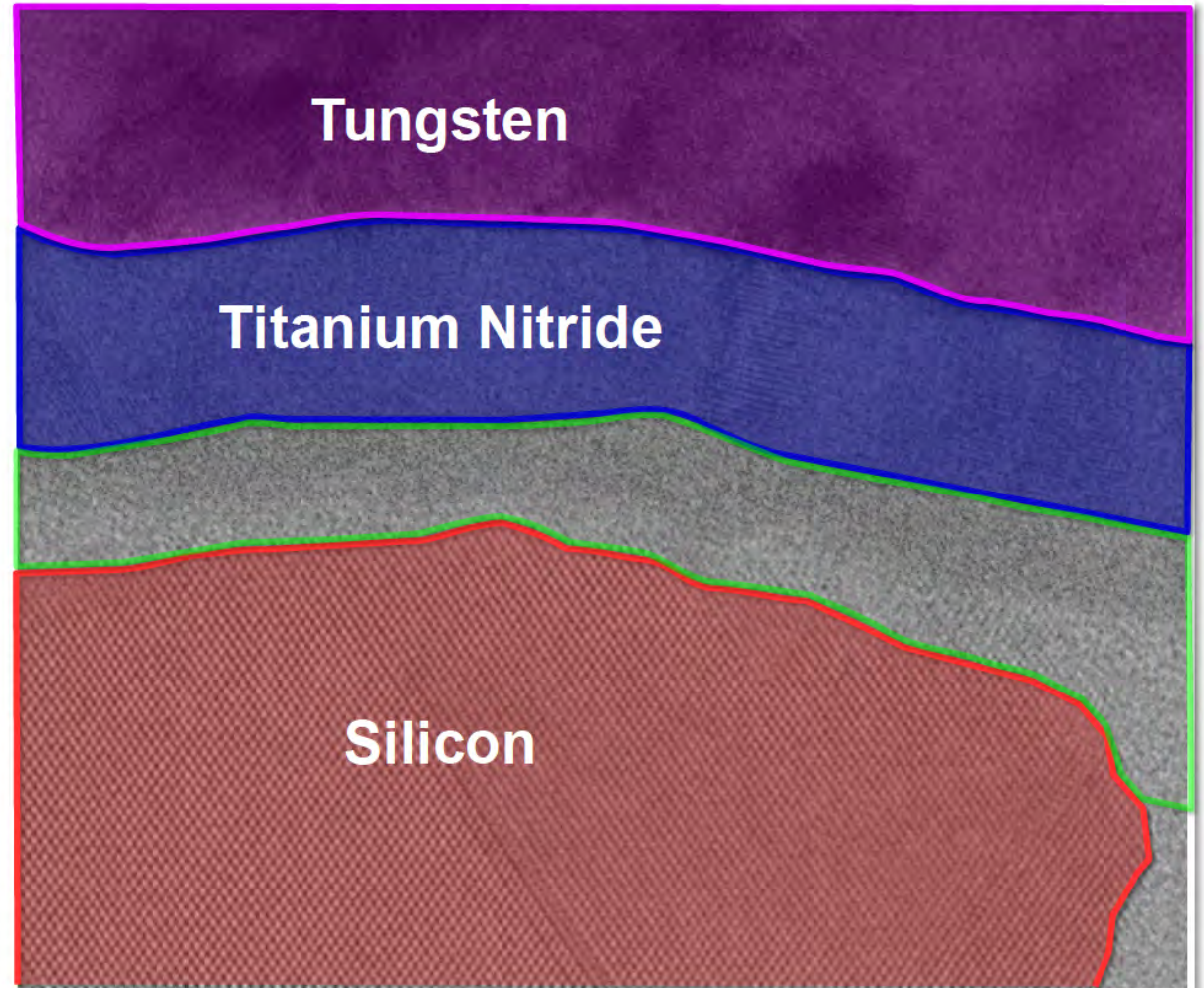
PTX00373-72

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Claim 17[c]: Distinct Layers of Oxide



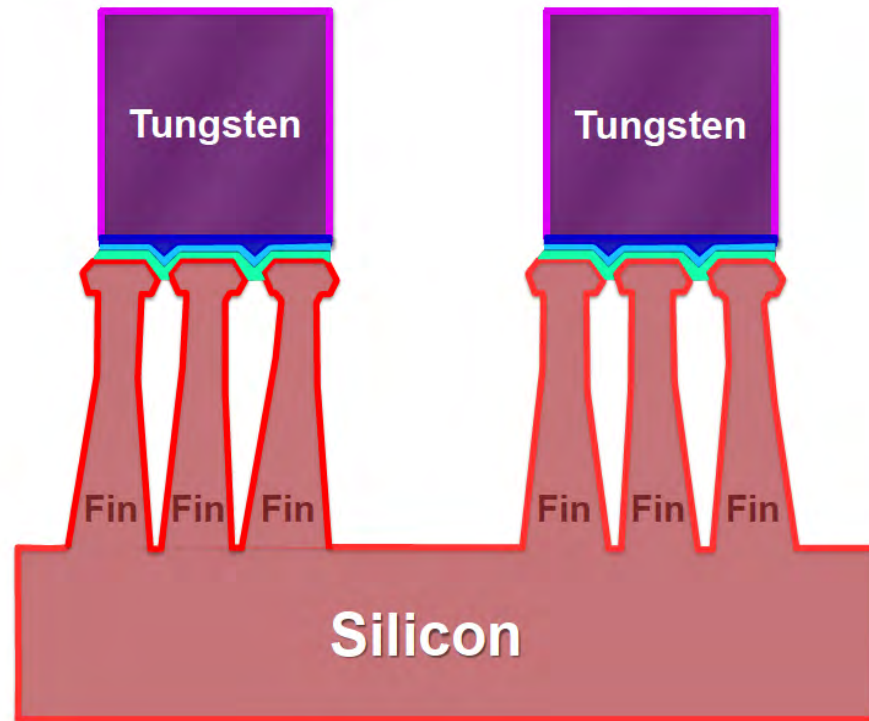
Actual Samsung Transistor



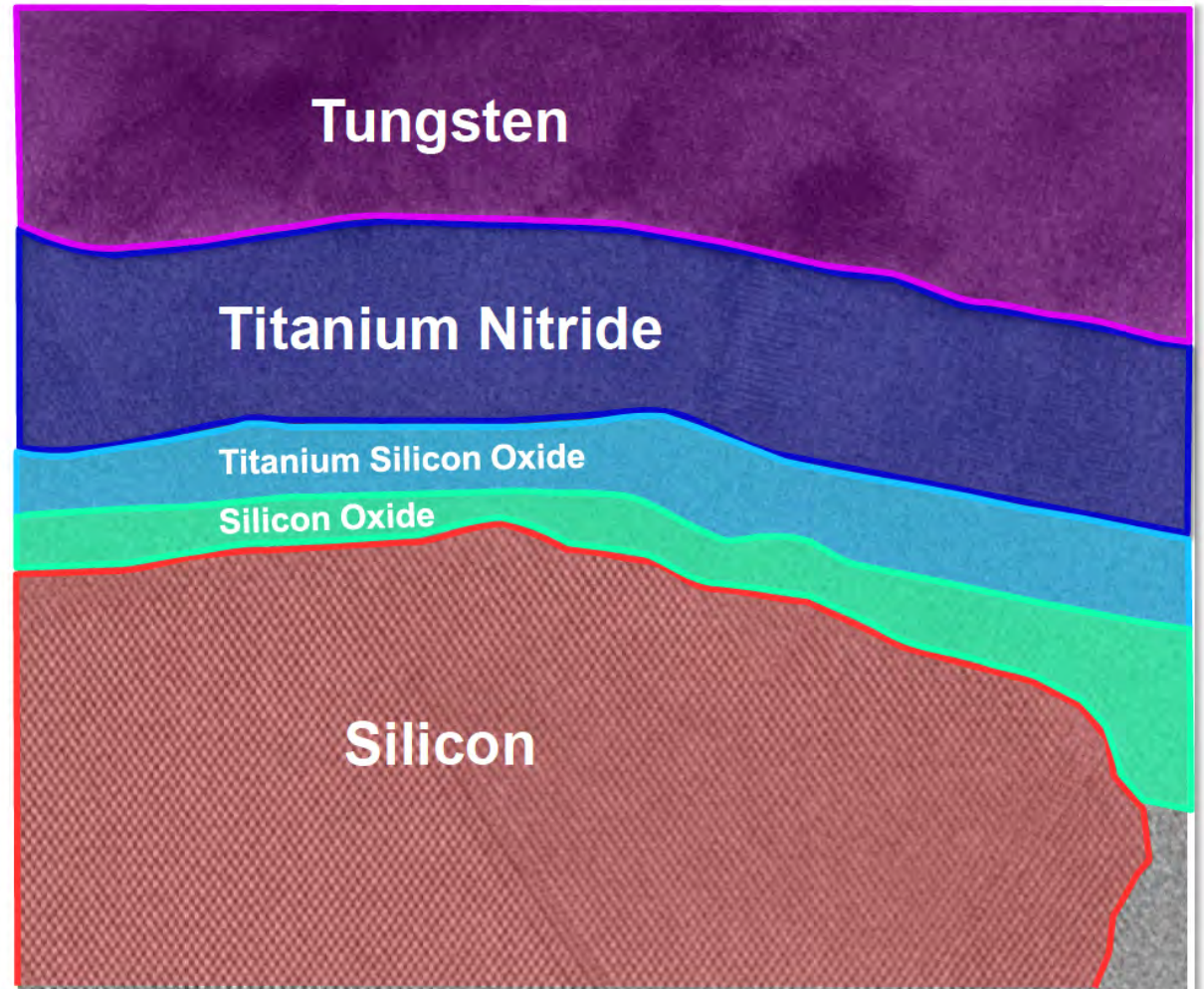
PTX00373-70

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Claim 17[c]: Distinct Layers of Oxide



Actual Samsung Transistor

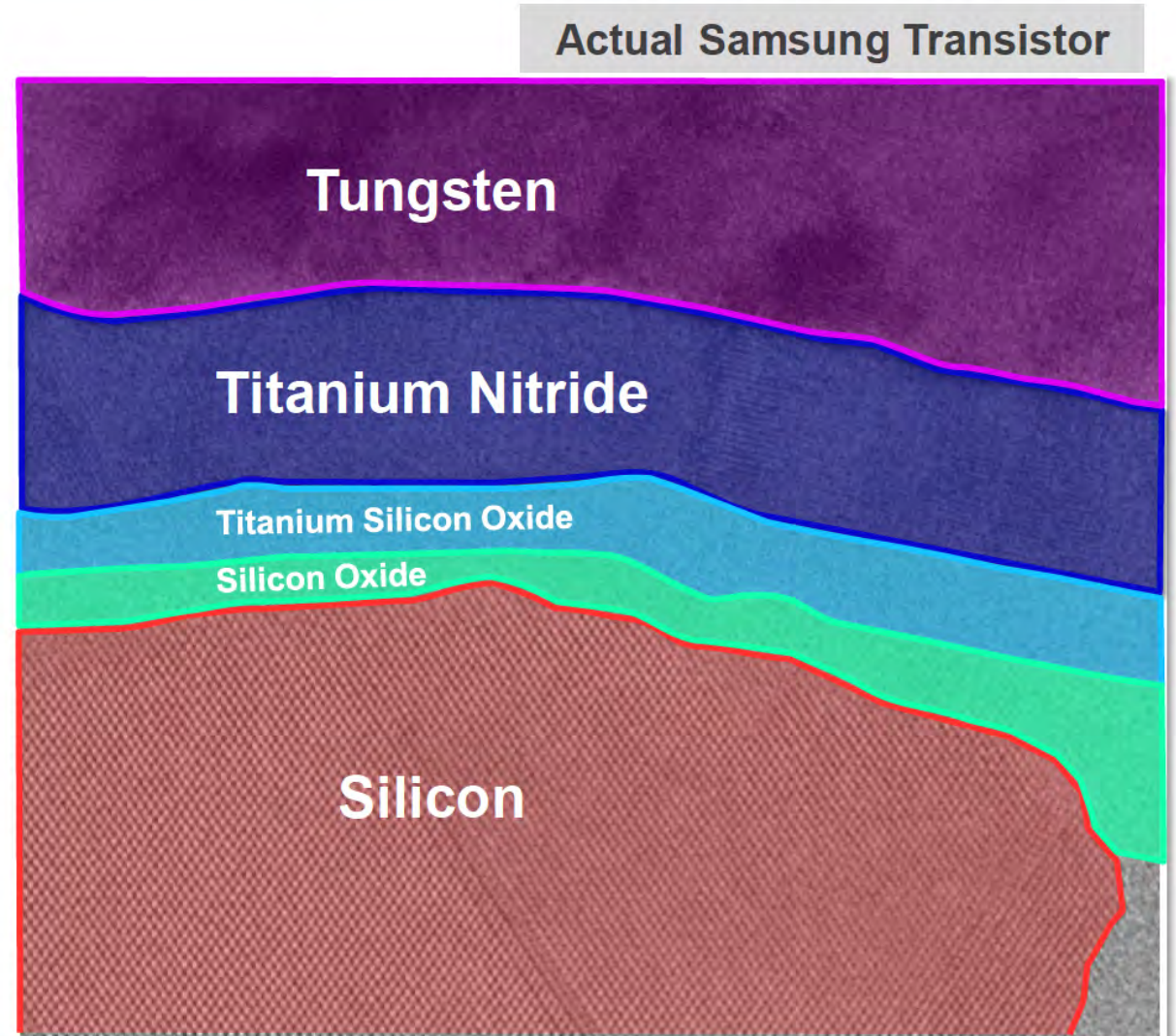


PTX00373-70

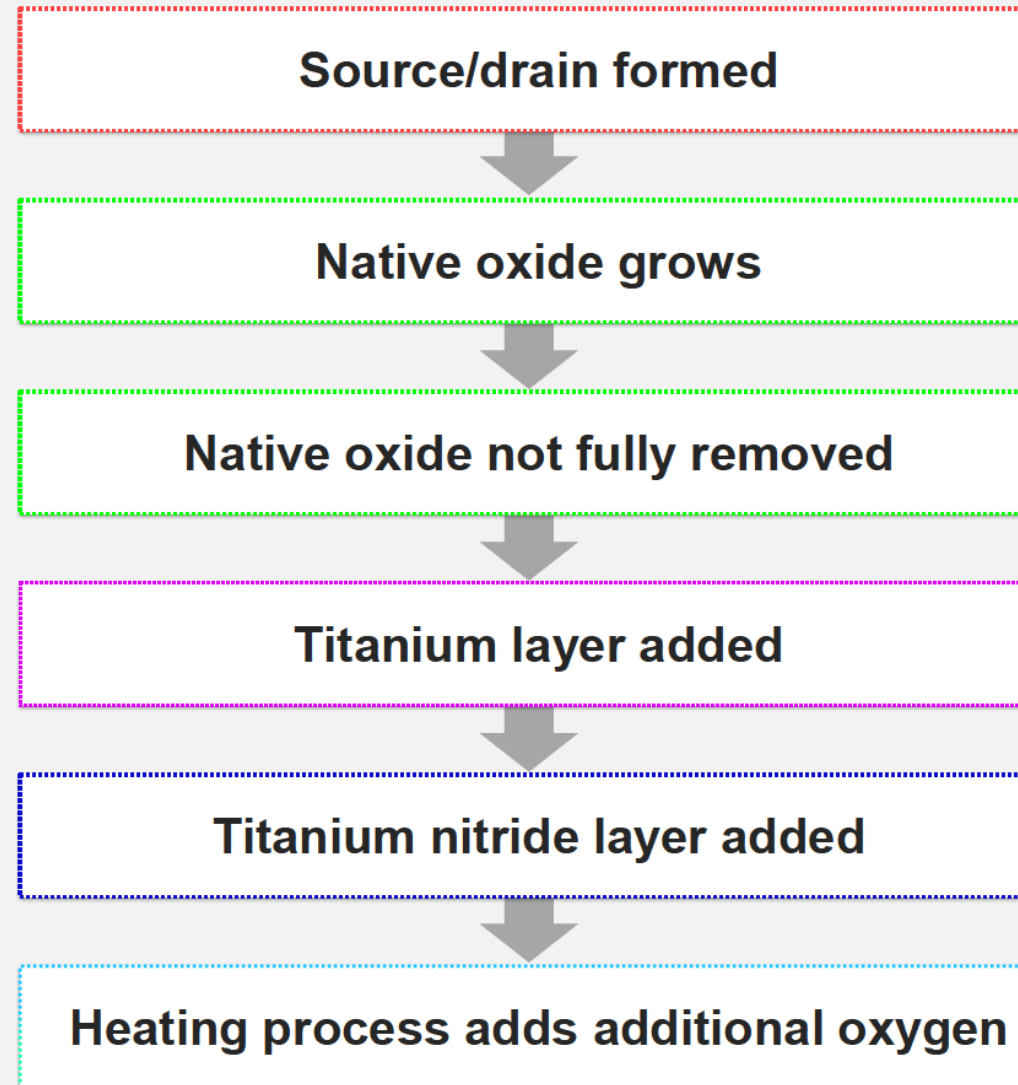
Case 2:19-cv-00347-JRG Document 401-3 Filed 09/02/21 Page 55 of 115 PageID #: 22758

Claim 17[c]: Distinct Layers of Oxide

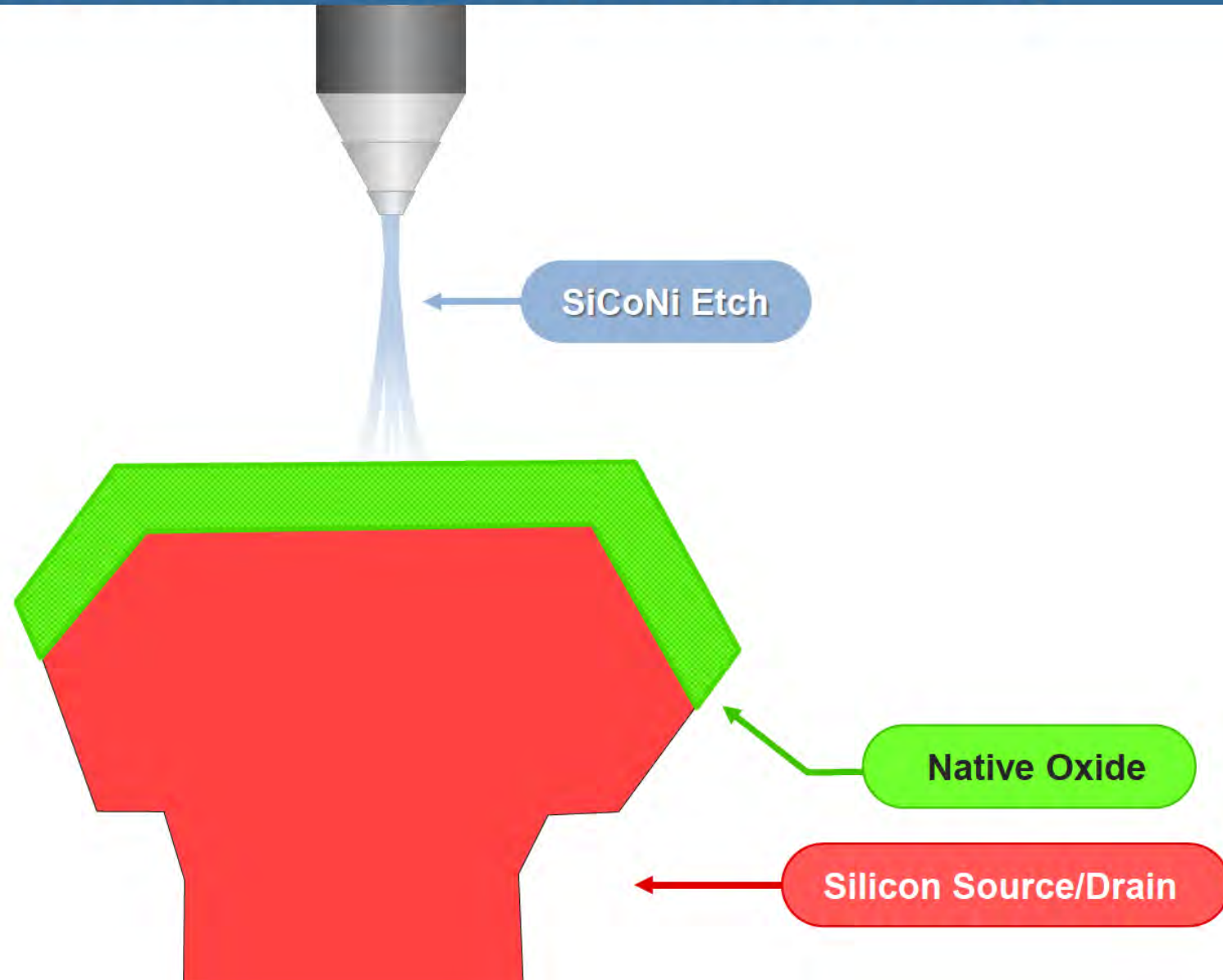
[17c] said interface layer comprising a layer of an oxide of titanium and a distinct layer of an oxide of the semiconductor.



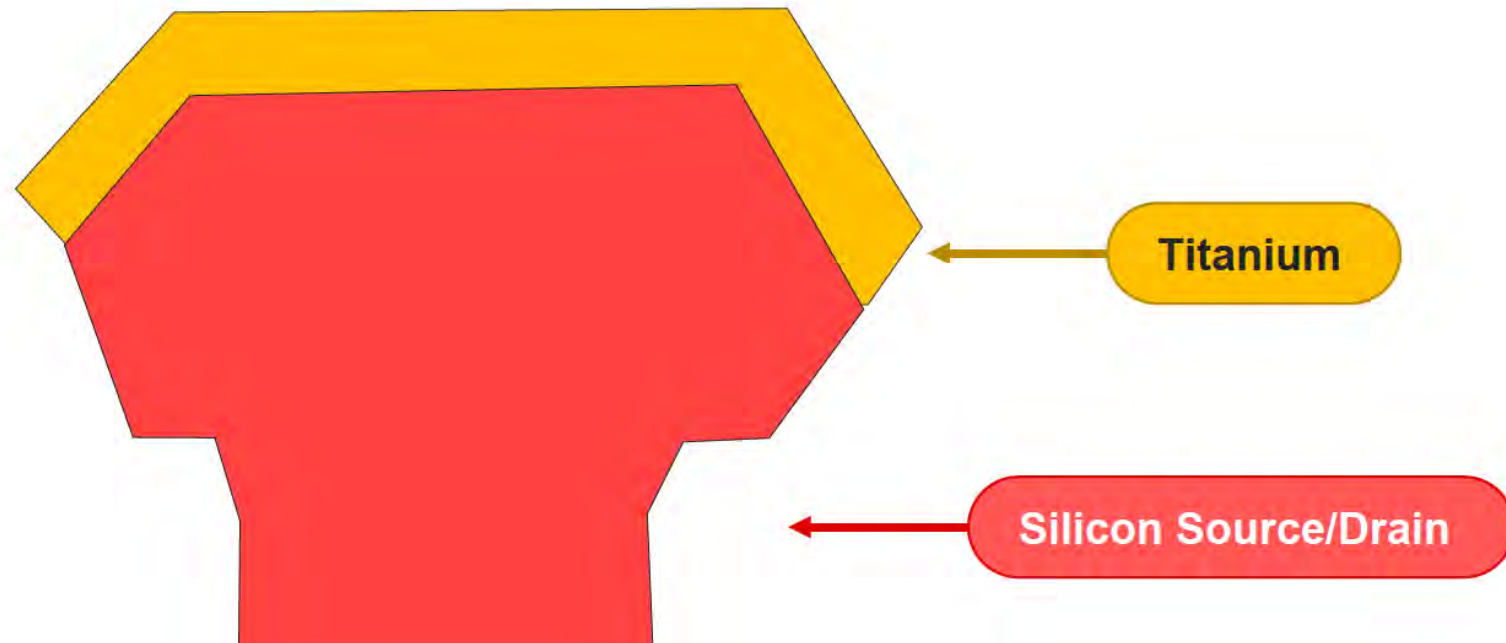
Samsung's Process Results in Oxide Layers



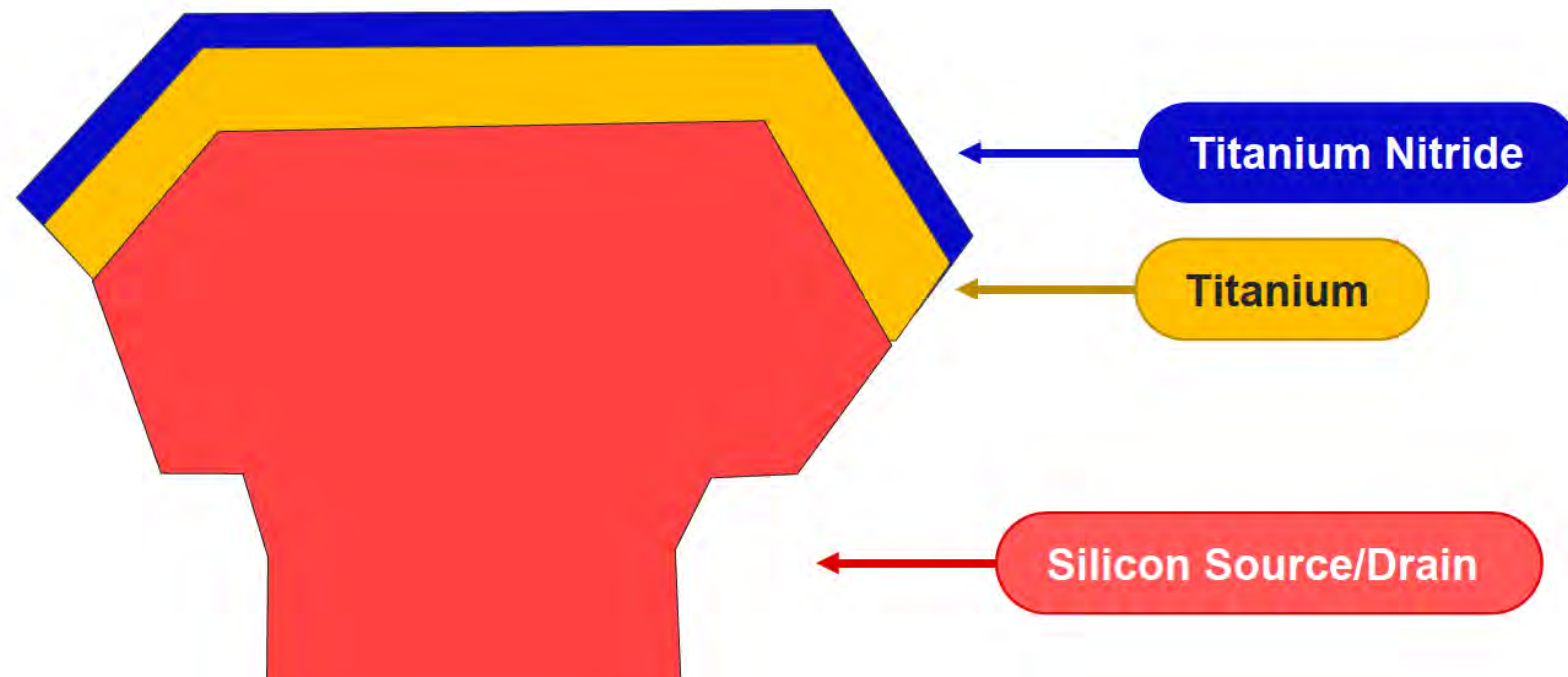
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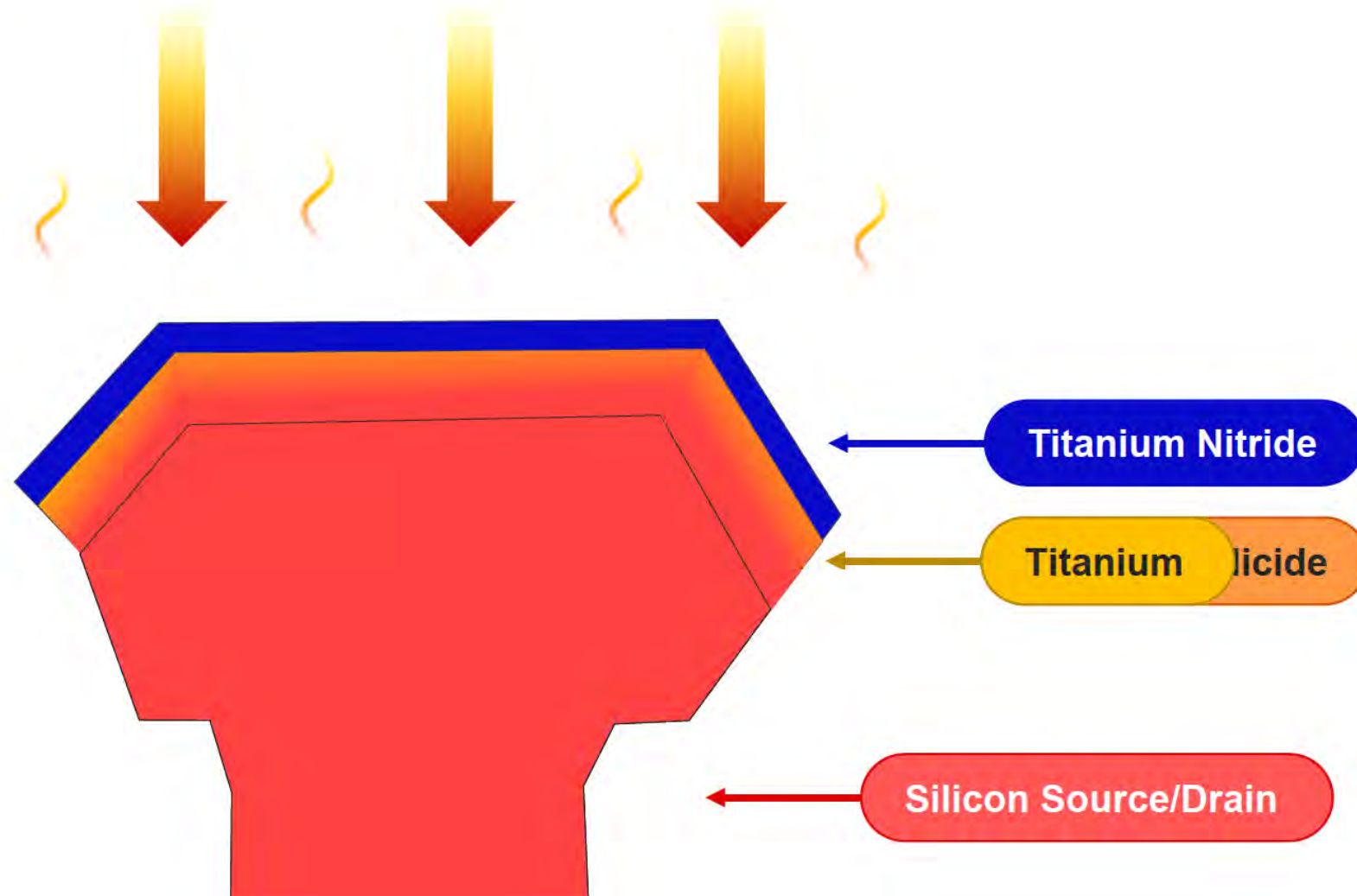
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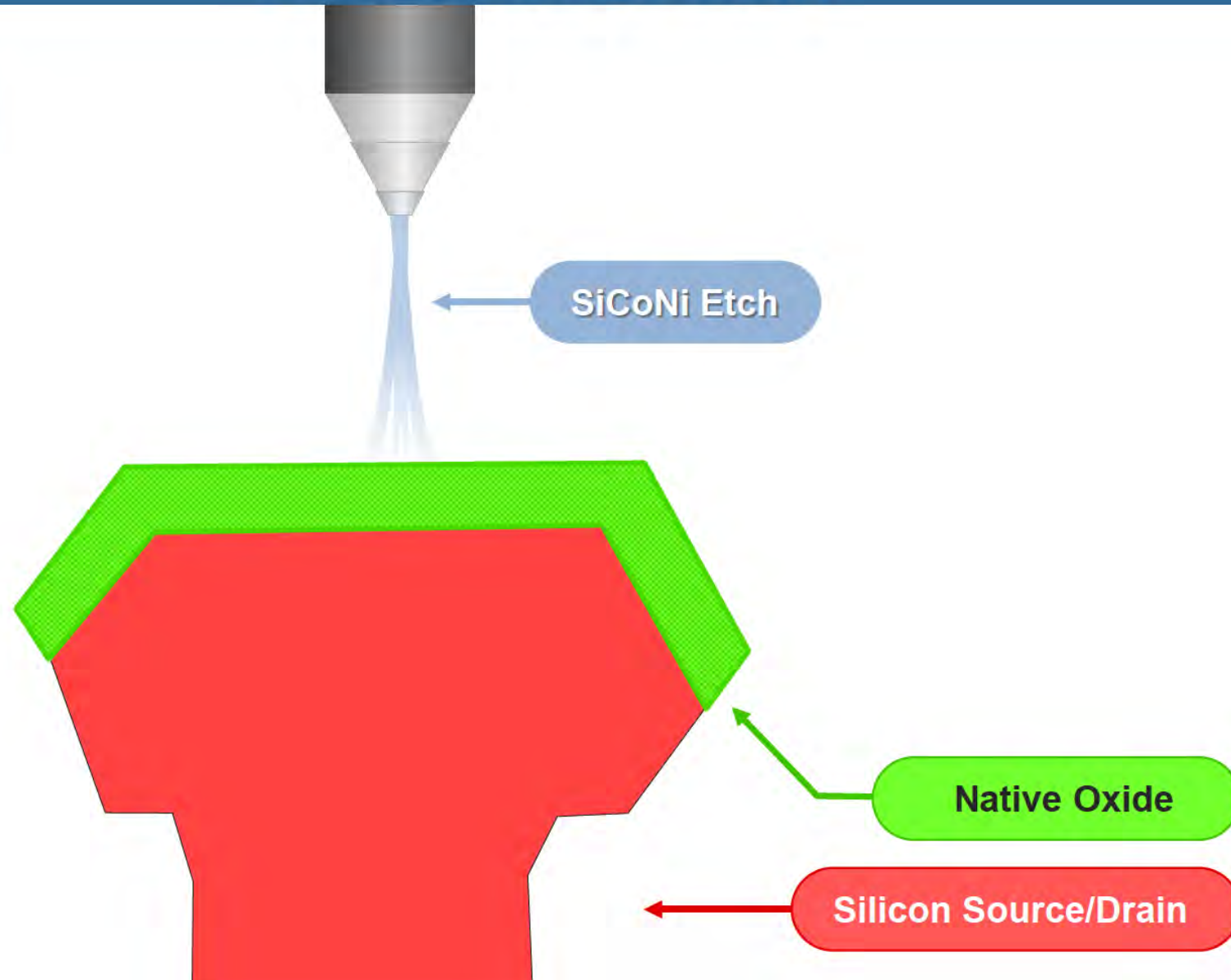
What Samsung Says Is Happening

SAMSUNG



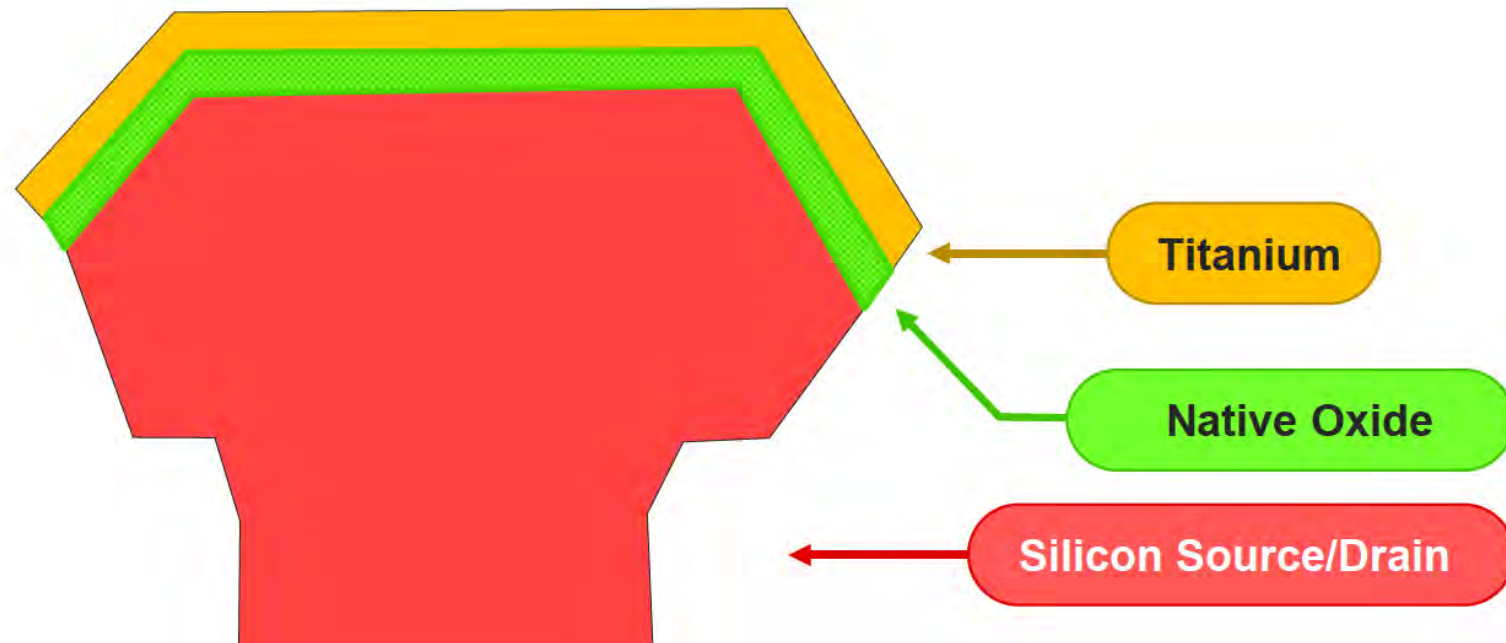
What Is Happening

ACORN
TECHNOLOGIES



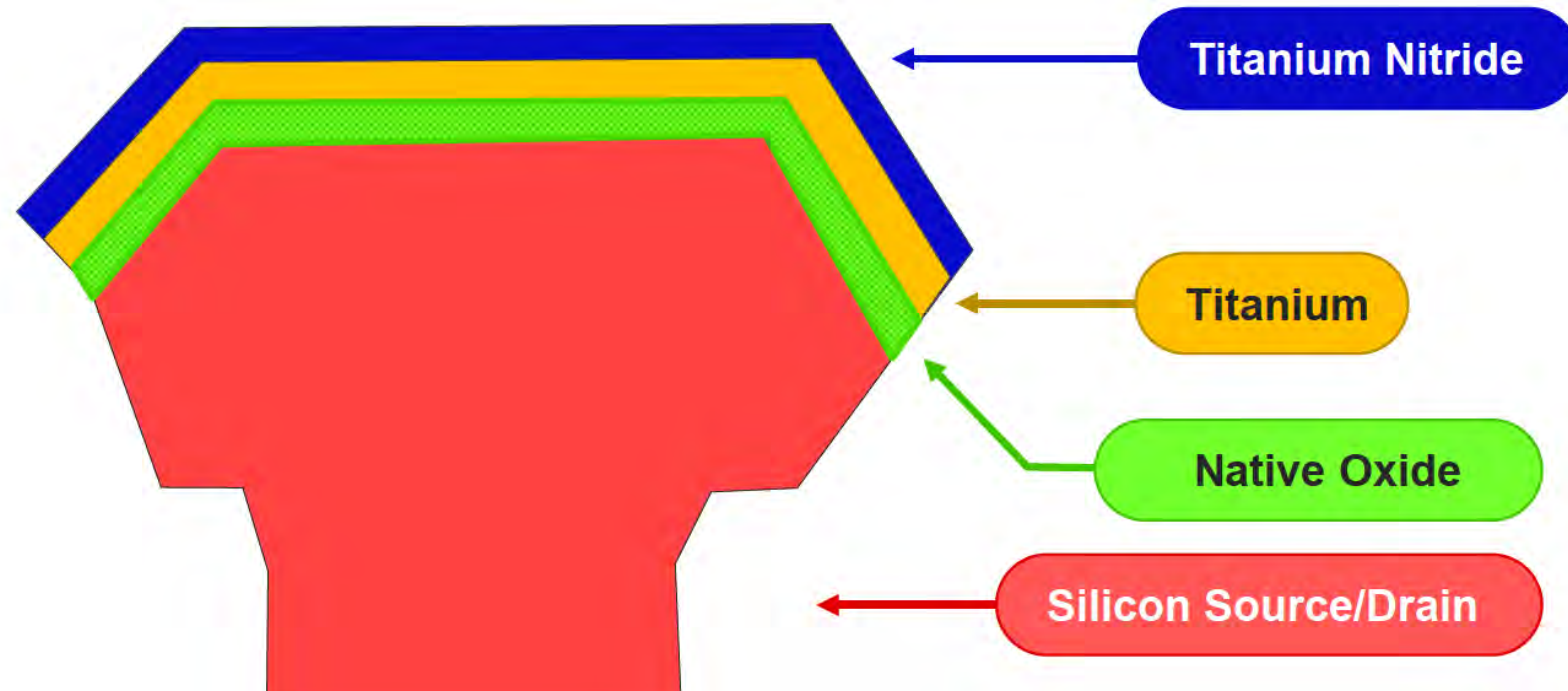
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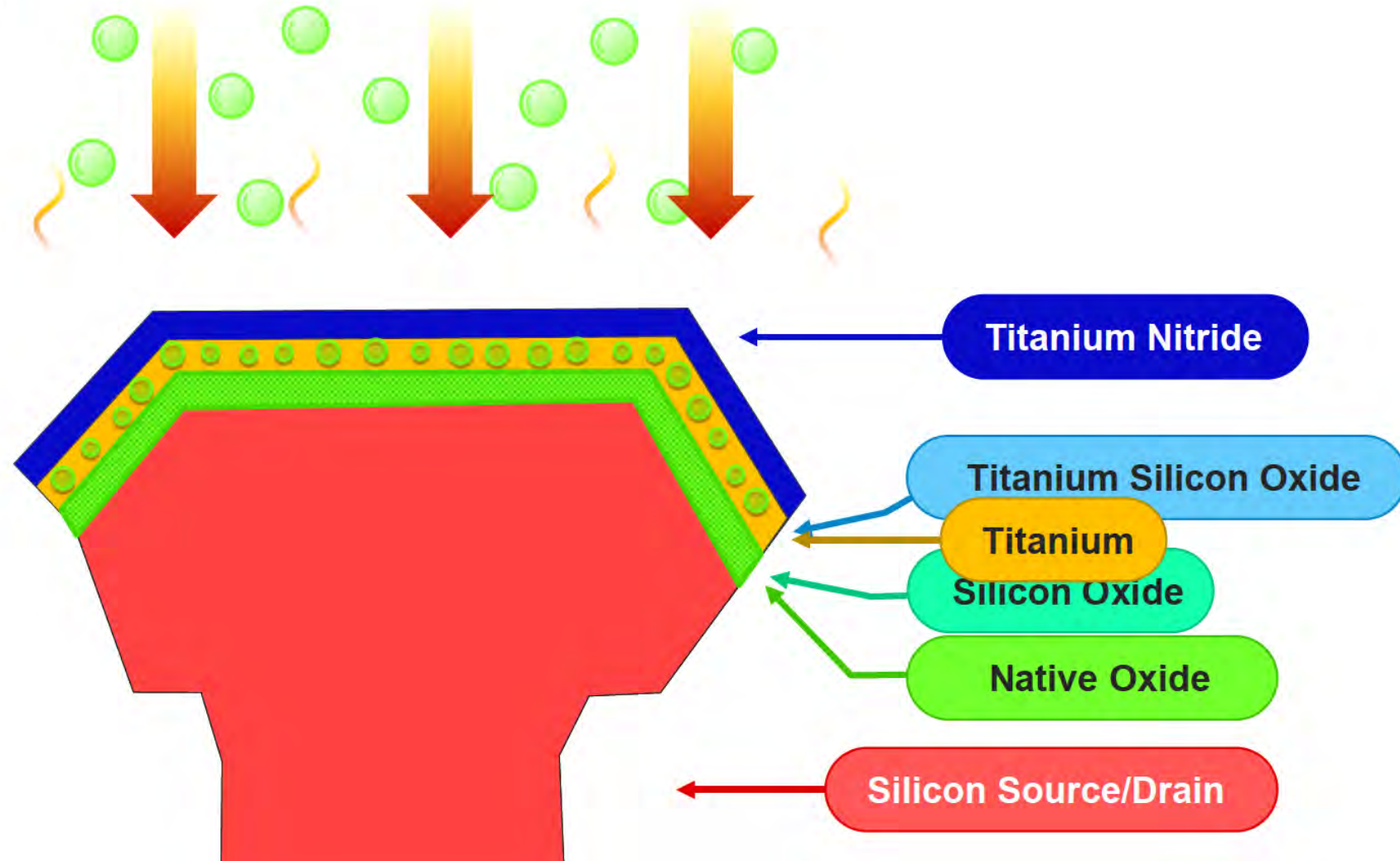
What Is Happening

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What Is Happening

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Samsung's Patent Re Metal Oxide Silicides

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US08110499B2

(12) United States Patent
Kang et al.

(10) Patent No.: US 8,110,499 B2
(45) Date of Patent: Feb. 7, 2012

(54) METHOD OF FORMING A CONTACT STRUCTURE

(75) Inventors: Dae-Hyun Kang, Gyeonggi-do (KR);
Young-Ho Kim, Gyeonggi-do (KR);
Chang-Ki Hong, Gyeonggi-do (KR);
Kun-Tack Lee, Gyeonggi-do (KR);
Jae-Dong Lee, Gyeonggi-do (KR);
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Jong-Nam Han, Seoul (KR)

(73) Assignee: Samsung Electronics Co., Ltd.,
Gyeonggi-do (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 68 days.

(21) Appl. No.: 12/437,390

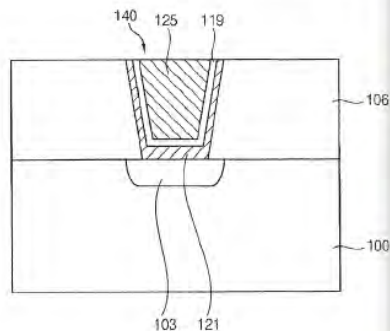
(22) Filed: May 7, 2009

(65) Prior Publication Data
US 2009/0286641 A1 Nov. 12, 2009

(30) Foreign Application Priority Data
May 7, 2008 (KR) 10-2008-0042251

(51) Int. Cl. H01L 21/44 (2006.01)

(52) U.S. Cl. 438/664 15 Claims, 15 Drawing Sheet



PTX-00106-1

Patent No.: US,811,499 B2
Date of Patent: Feb. 7, 2012

Assignee: Samsung Electronics Co., Ltd.,
Gyeonggi-do (KR)

(57)

ABSTRACT

An insulation layer may be formed on an object having a contact region. The insulation layer may be partially etched to form an opening exposing the contact region. A material layer including silicon and oxygen may be formed on the exposed contact region. A metal layer may be formed on the material layer including silicon and oxygen. The material layer including silicon and oxygen may be reacted with the metal layer to form a metal oxide silicide layer at least on the contact region. A conductive layer may be formed on the metal oxide silicide layer to fill up the opening.

PTX00106 at Abstract

Samsung's Patent Re Metal Oxide Silicides

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US008110499B2

(12) **United States Patent**
Kang et al.

(10) **Patent No.:** **US 8,110,499 B2**
(45) **Date of Patent:** **Feb. 7, 2012**

(54) **METHOD OF FORMING A CONTACT STRUCTURE**

(75) **Inventors:** **Dae-Hyuk Kang, Gyeonggi-do (KR);**
Yung-Ho Kim, Gyeonggi-do (KR);
Chang-Ki Hong, Gyeonggi-do (KR);
Kan-Tack Lee, Gyeonggi-do (KR);
Jae-Dong Lee, Gyeonggi-do (KR);
Dae-Hong Lim, Gyeonggi-do (KR);
Jeong-Nam Han, Seoul (KR)

(73) **Assignee:** **Samsung Electronics Co., Ltd.,**
Gyeonggi-do (KR)

(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 68 days.

(21) **Appl. No.:** **12/437,390**

(22) **Filed:** **May 7, 2009**

(65) **Prior Publication Data**
US 2009/0290641 A1 Nov. 12, 2009

(30) **Foreign Application Priority Data**
May 7, 2008 (KR) 10-2008-0042251

(51) **Int. Cl.**
H01L 21/44 (2006.01)

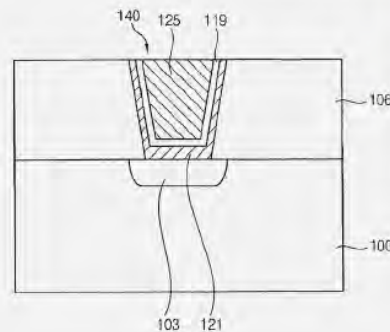
(52) **U.S. Cl.** 438/664

(58) **Field of Classification Search** 438/653, 438/664
See application file for complete search history.

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* cited by examiner
Primary Examiner—Bradley K. Smith
(74) **Attorney, Agent, or Firm**—Myers Bigel Saxe LLP, P.A.

(57) **ABSTRACT**
An insulative layer may be formed on an object contact region. The insulative layer may be partially form an opening exposing the contact region. A material including silicon and oxygen may be formed on the contact region. A metal layer may be formed on the layer including silicon and oxygen. The material including silicon and oxygen may be reacted with the metal layer to form a metal oxide silicide layer at least on the contact region. A conductive layer may be formed on the metal oxide silicide layer to fill up the opening.

15 Claims, 15 Drawing Sheets



PTX-00106-1

PLAINTIFF'S
TRIAL EXHIBIT
PTX-00106
Case No. 19-cv-00347-JRG

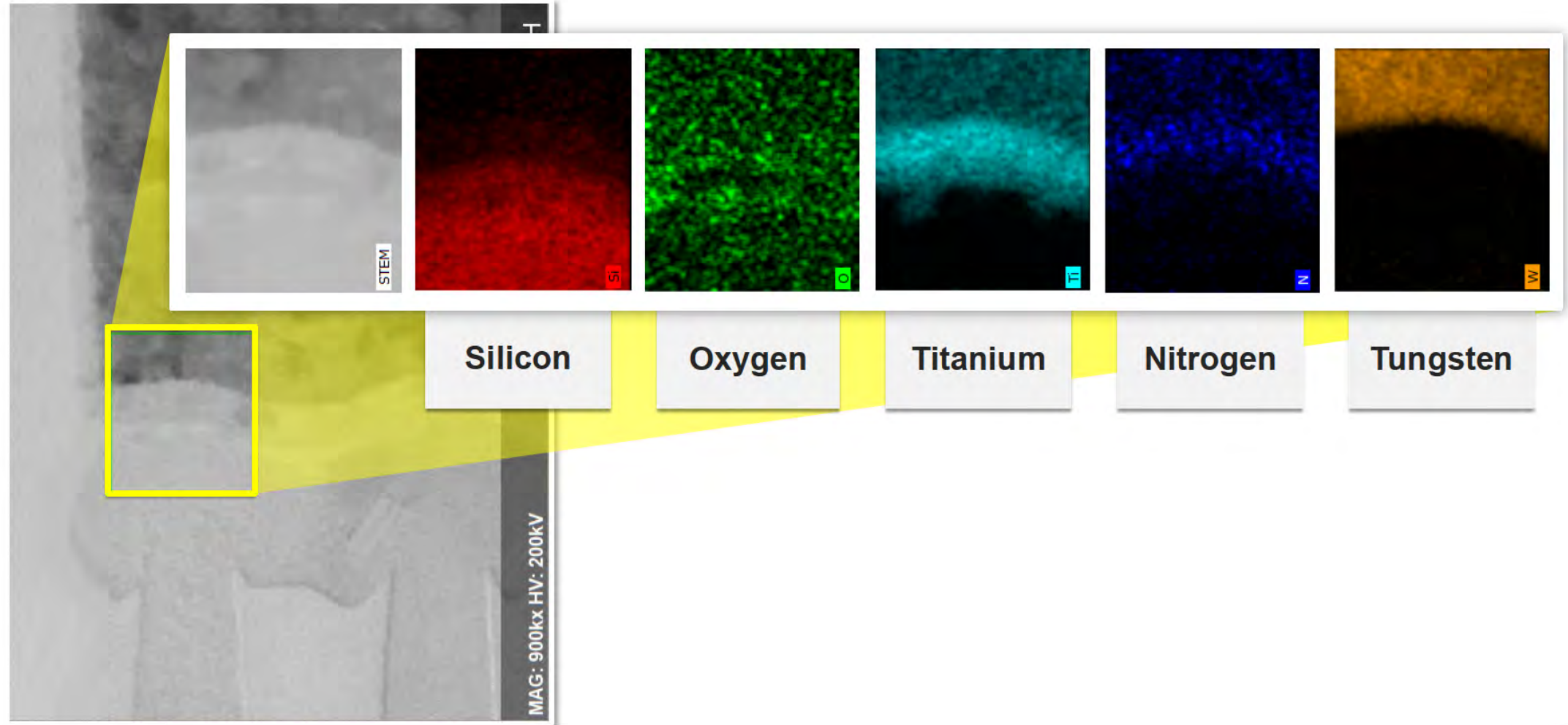
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According to example embodiments, a material layer including silicon and oxygen is formed on a contact region of an object, and then a silicidation process is carried out. Hence, a metal oxide silicide layer having a ternary composition of oxygen-silicon-metal may be uniformly formed with a desired thickness between the contact region and a contact or a plug.

PTX00106 at 10:18-29

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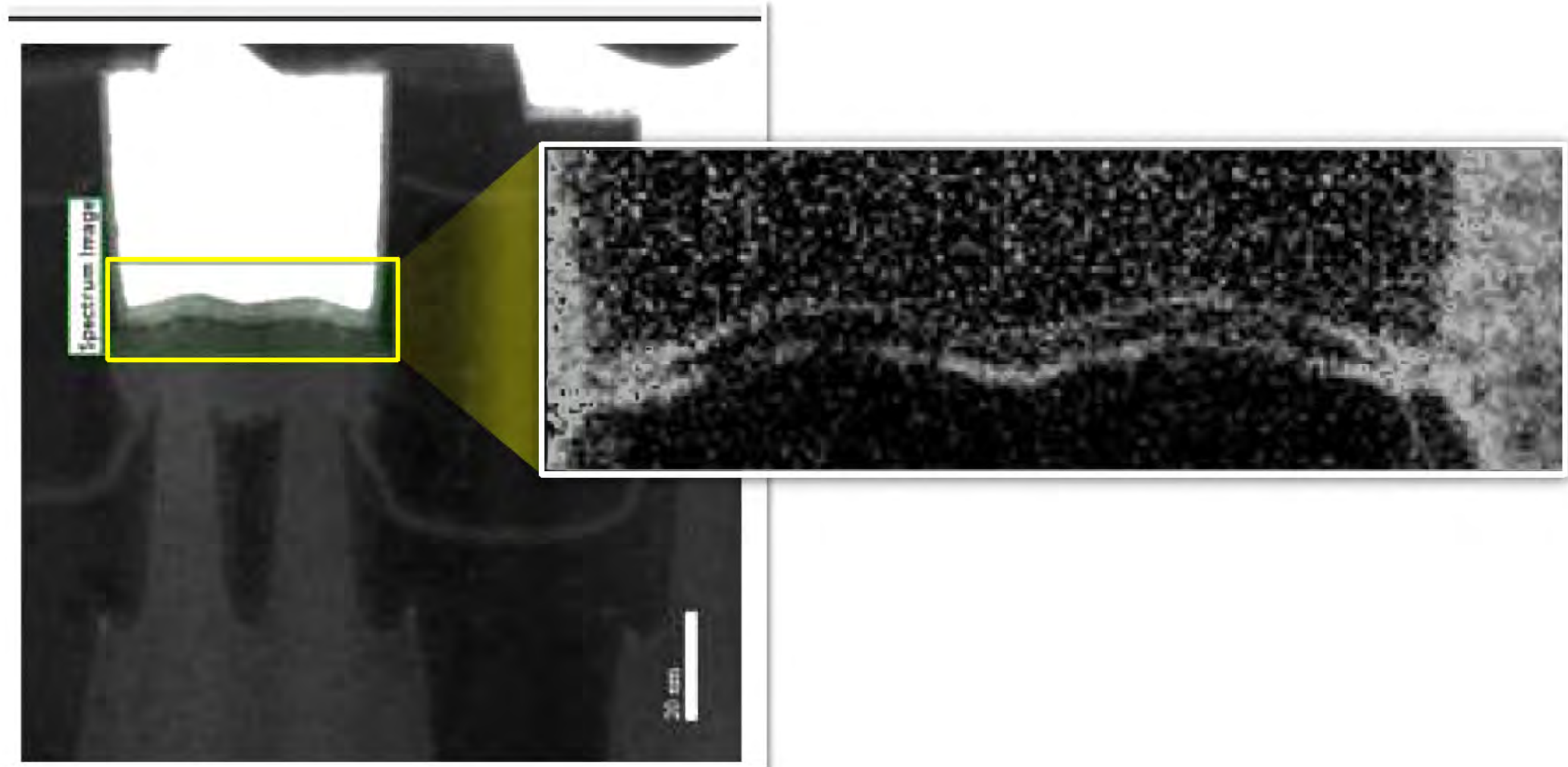
Elemental Analysis of Exynos 7420



PTX00373-8

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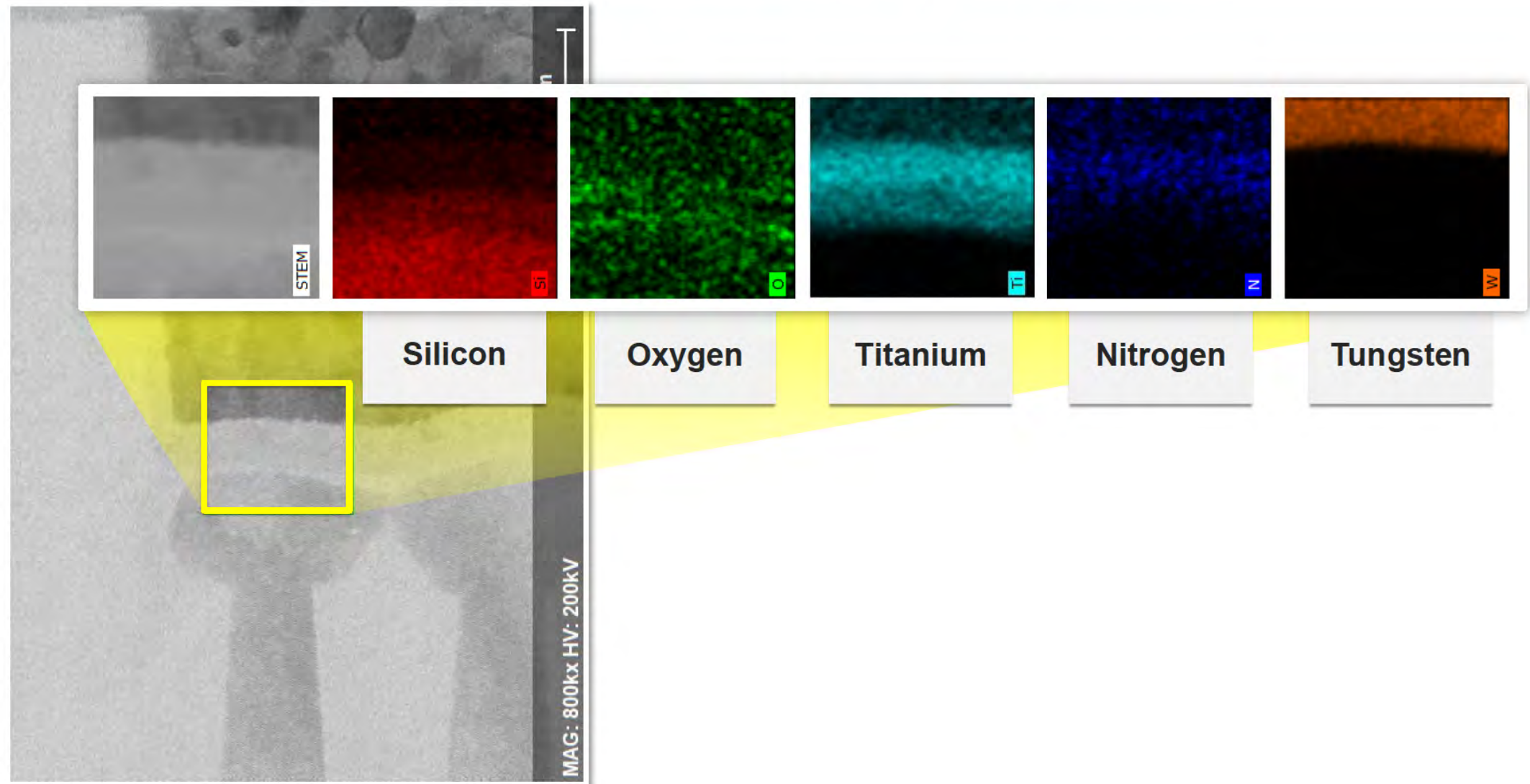
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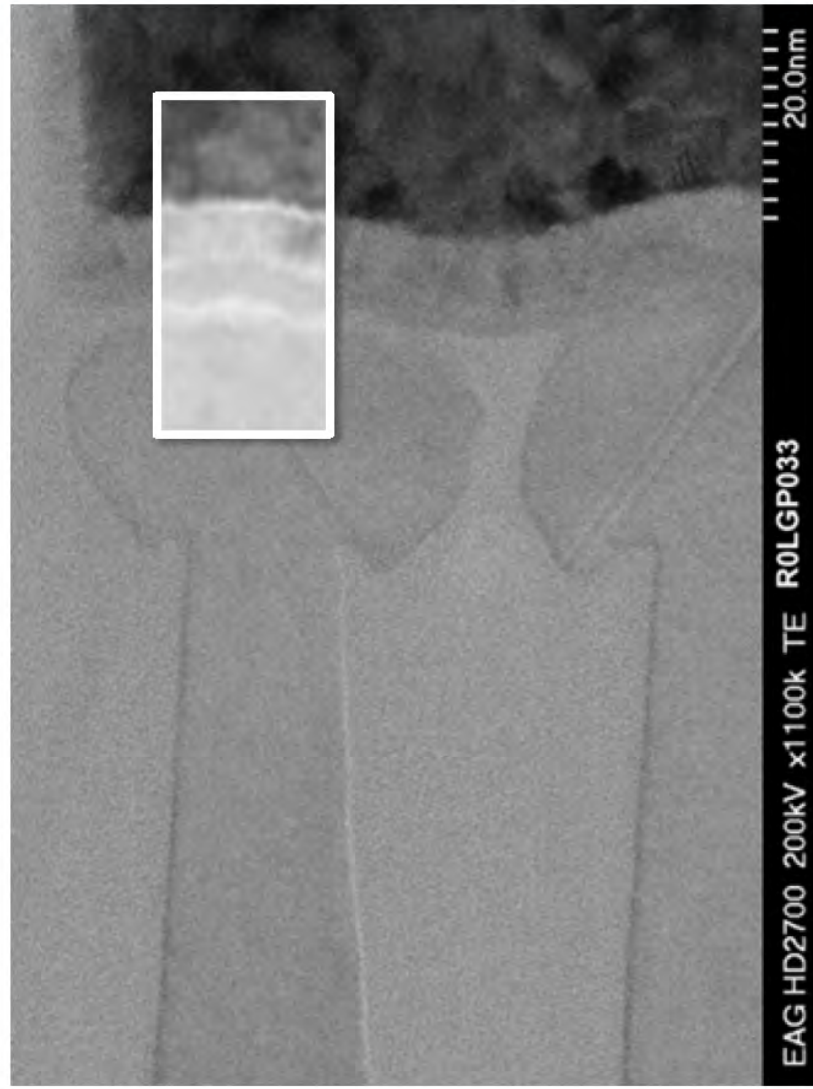
Case 2:19-cv-00347-JRG Document 401-3 Filed 09/02/21 Page 69 of 115 PageID #: 22772

Elemental Analysis of Exynos 8890



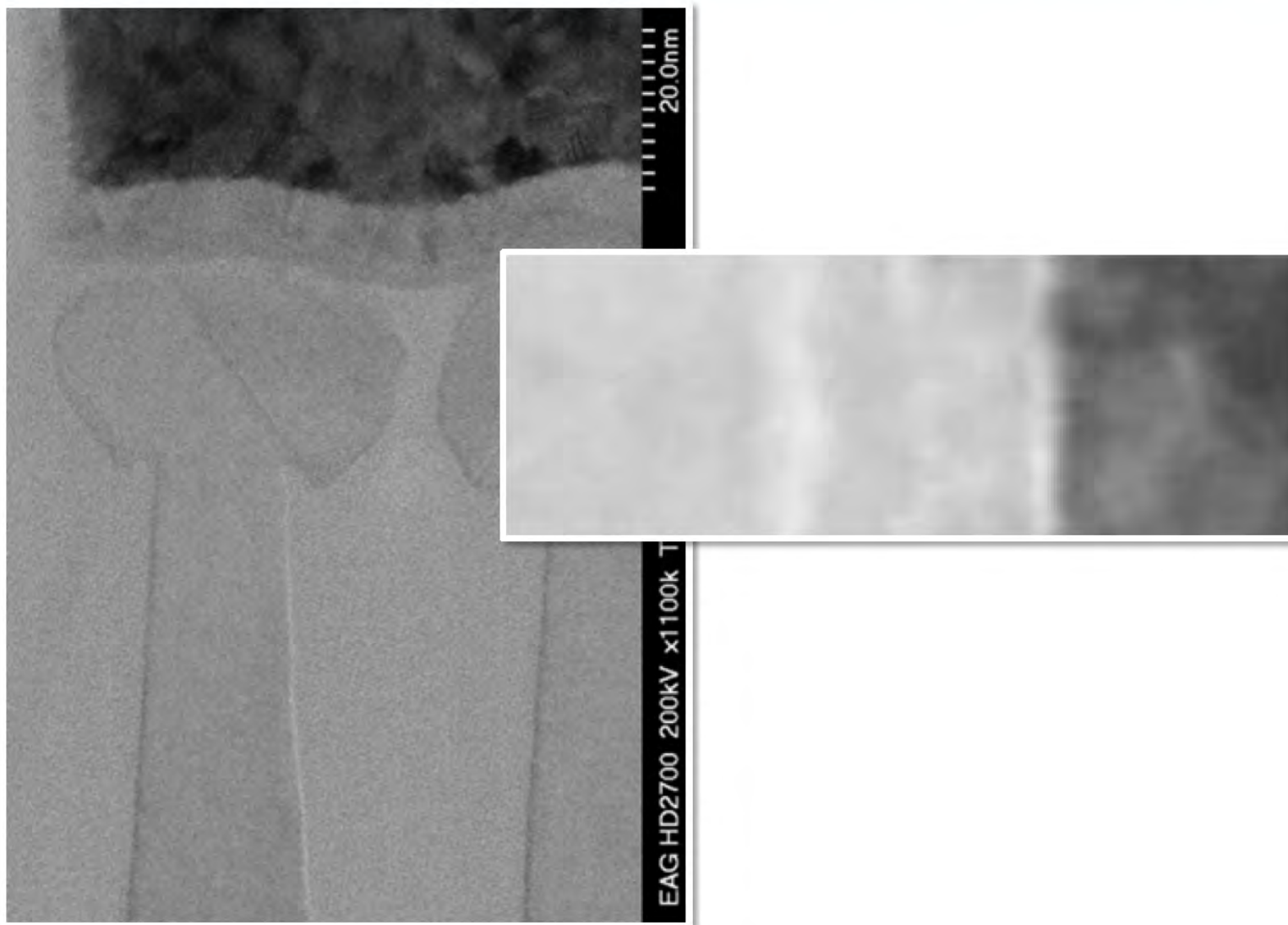
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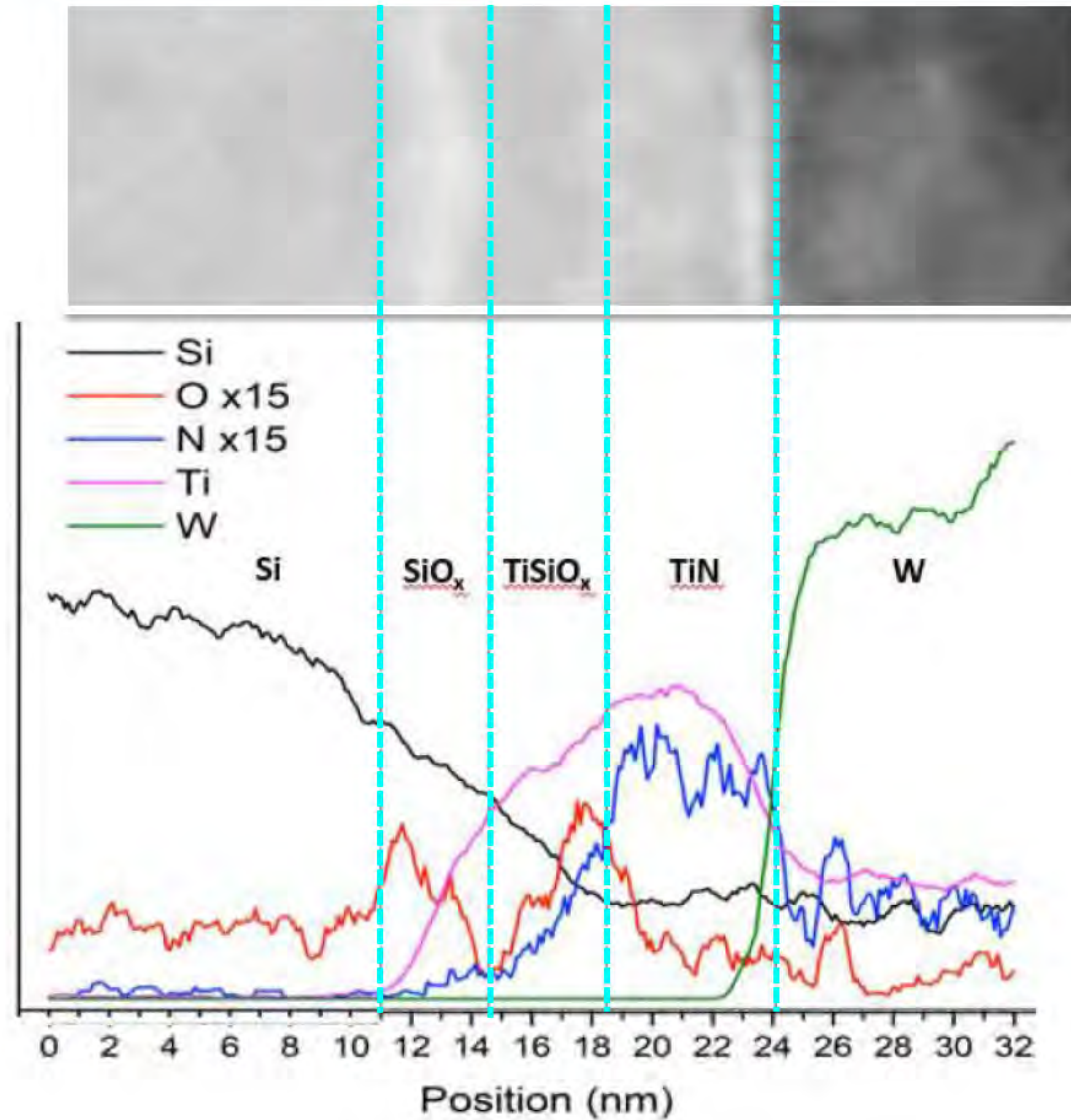
PTX00373

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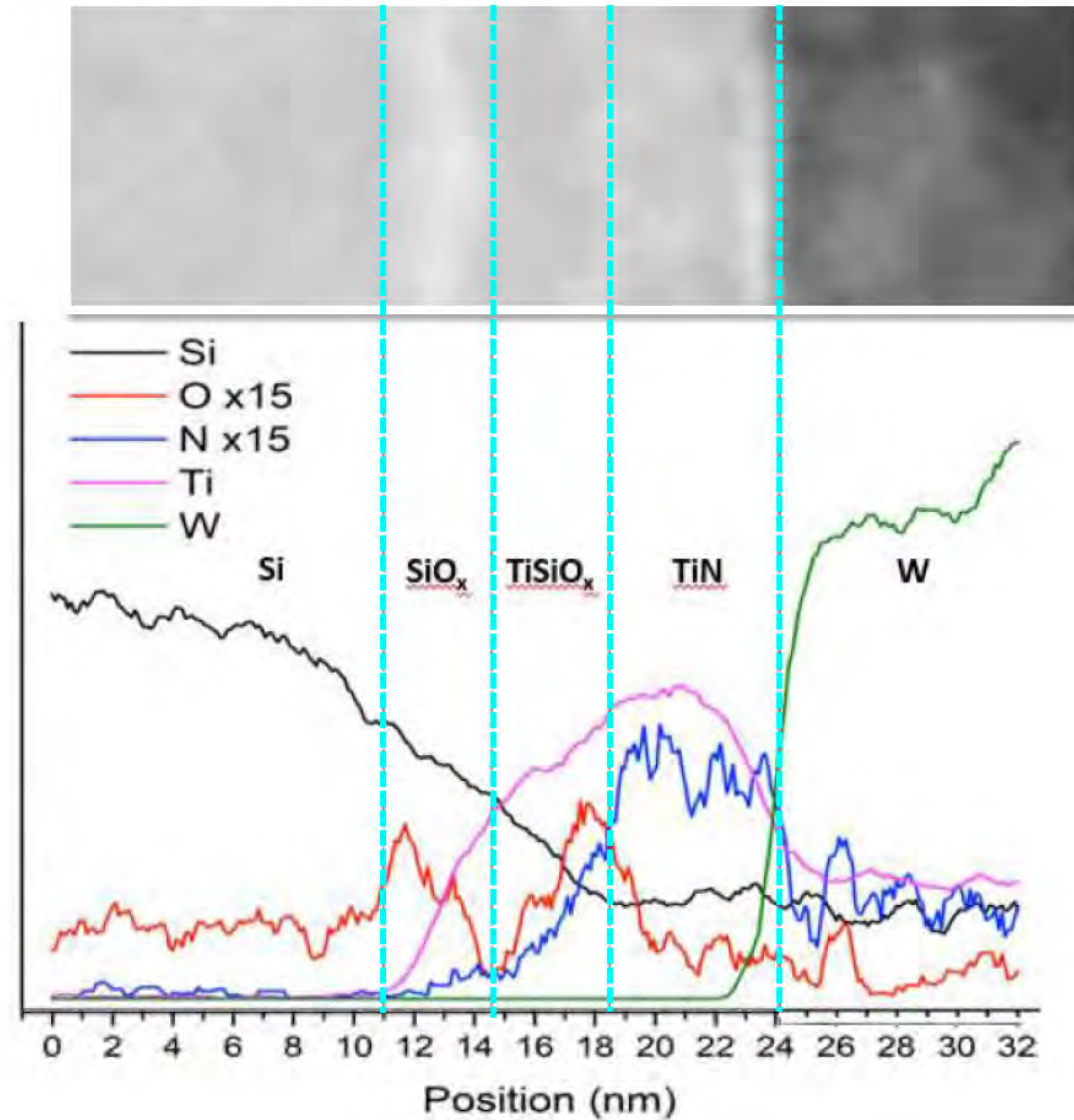


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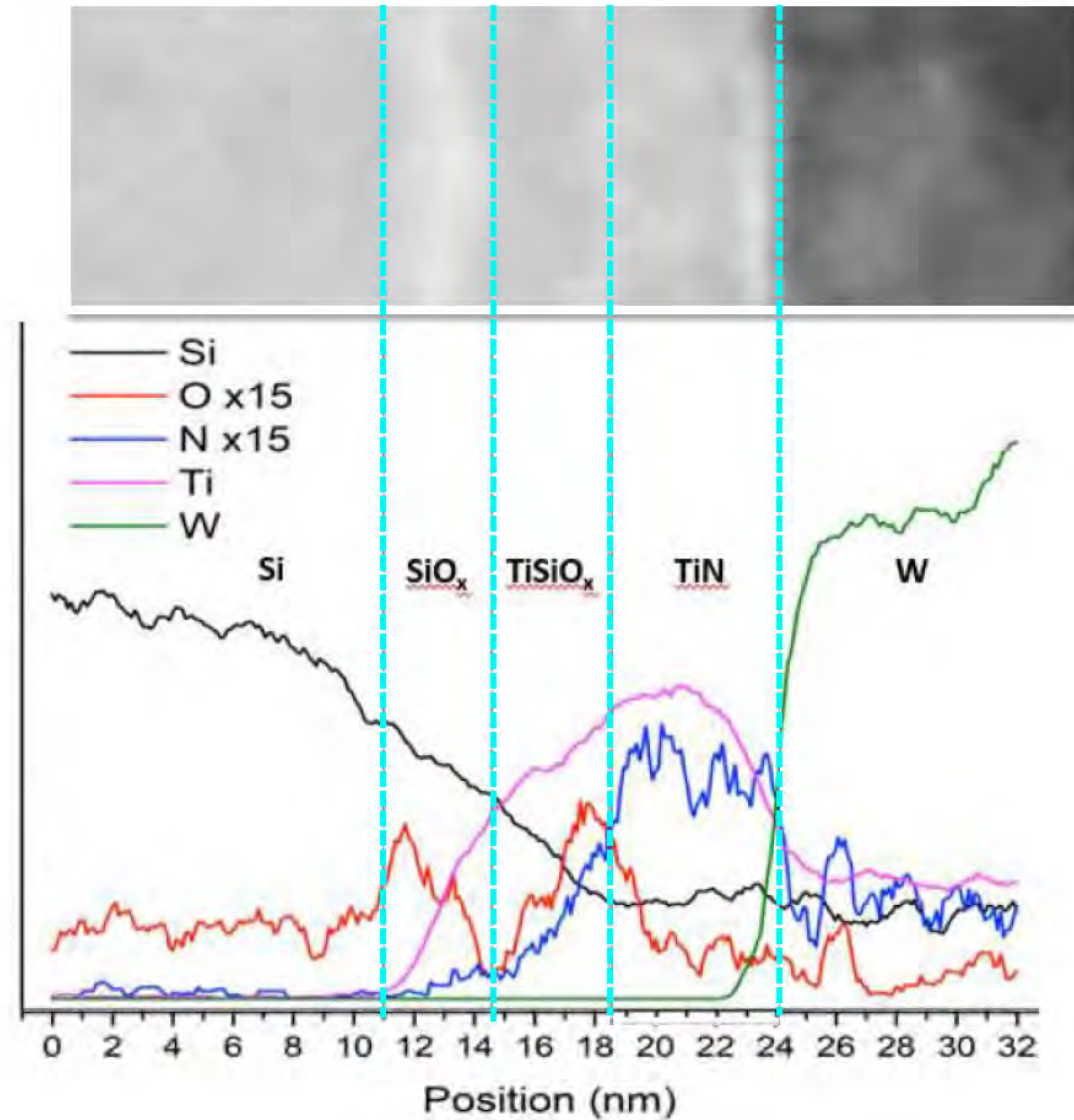
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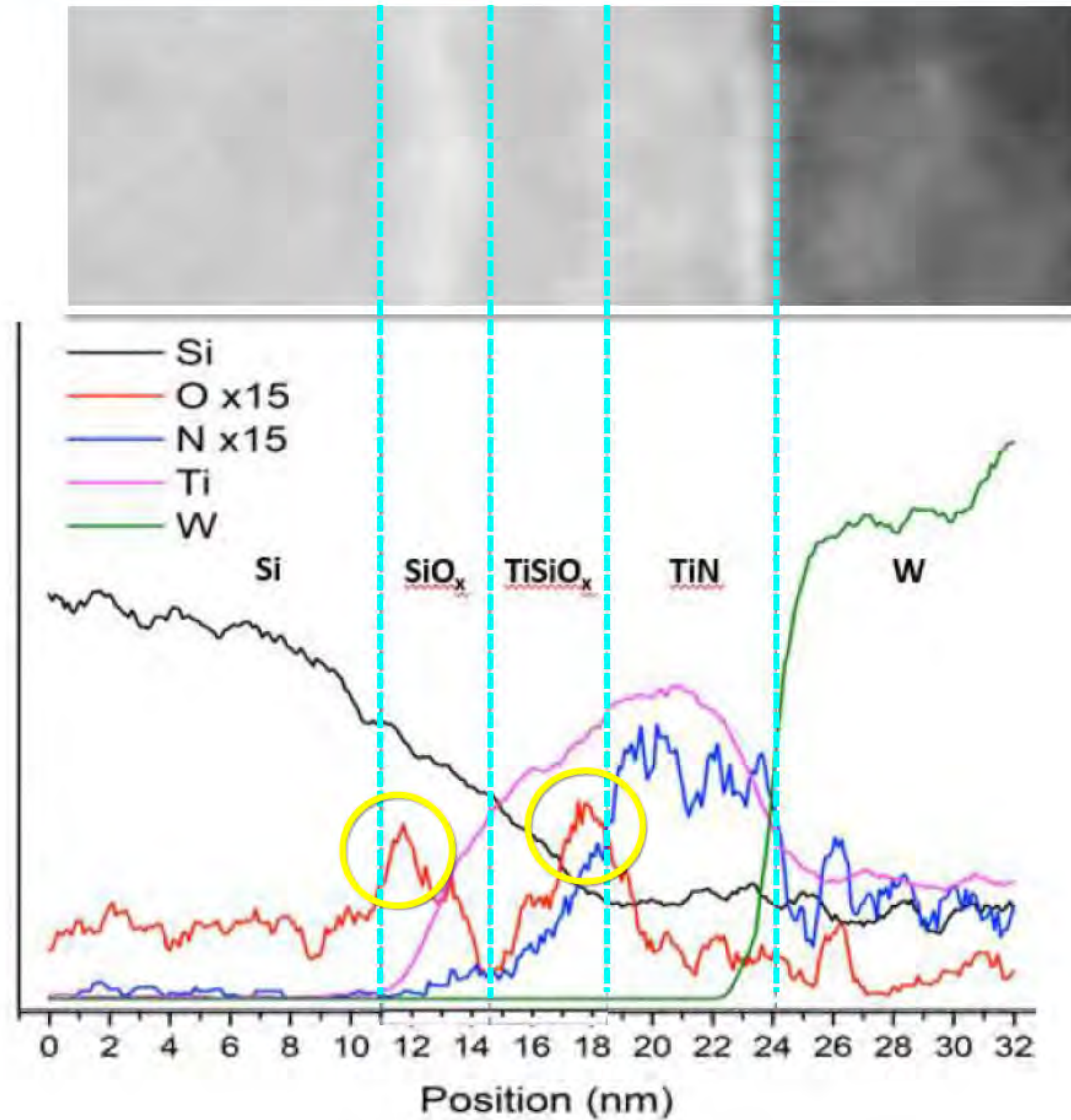
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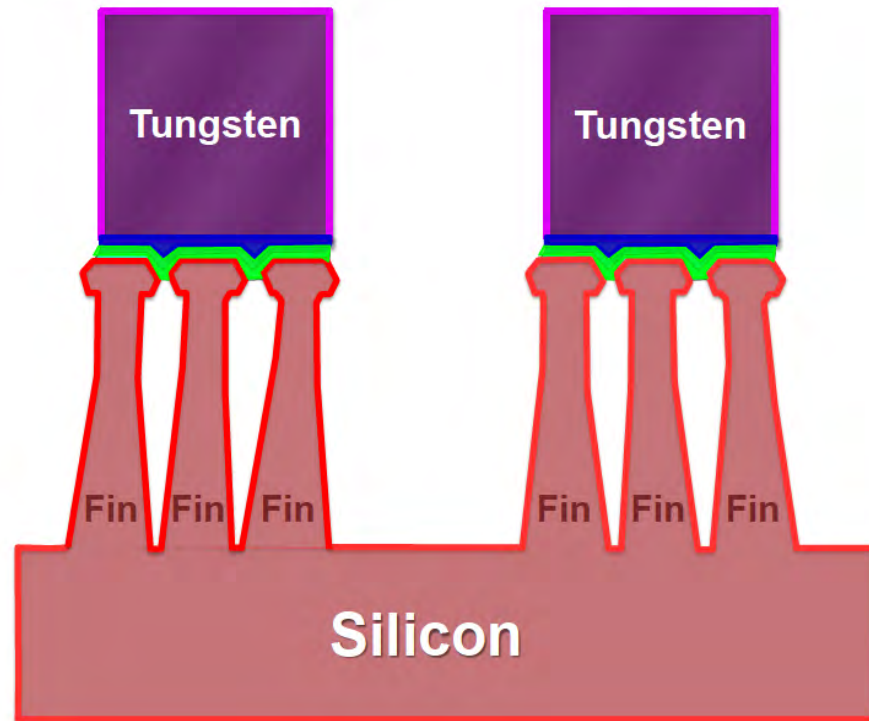


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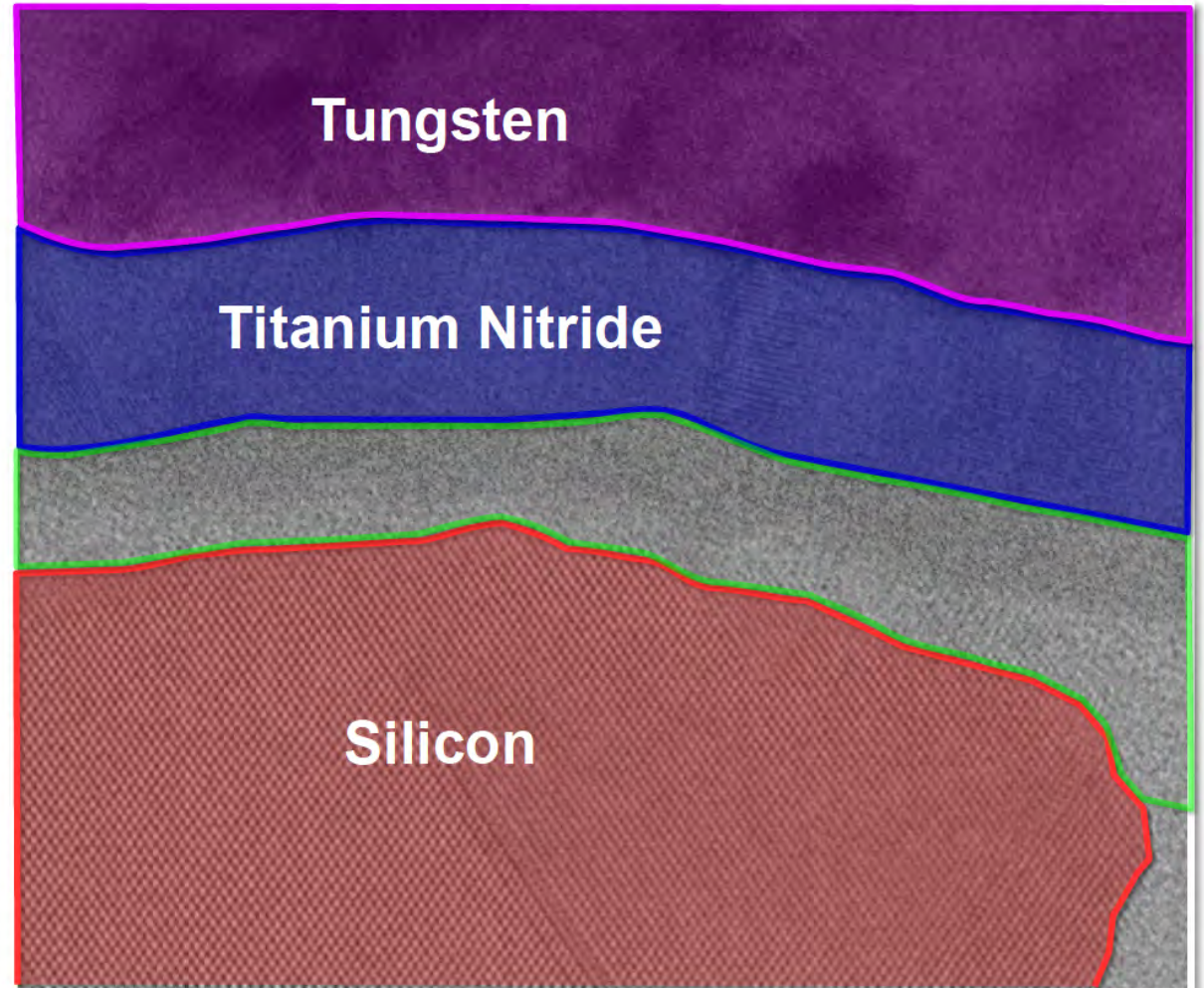


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Claim 17[c]: Distinct Layers of Oxide



Actual Samsung Transistor

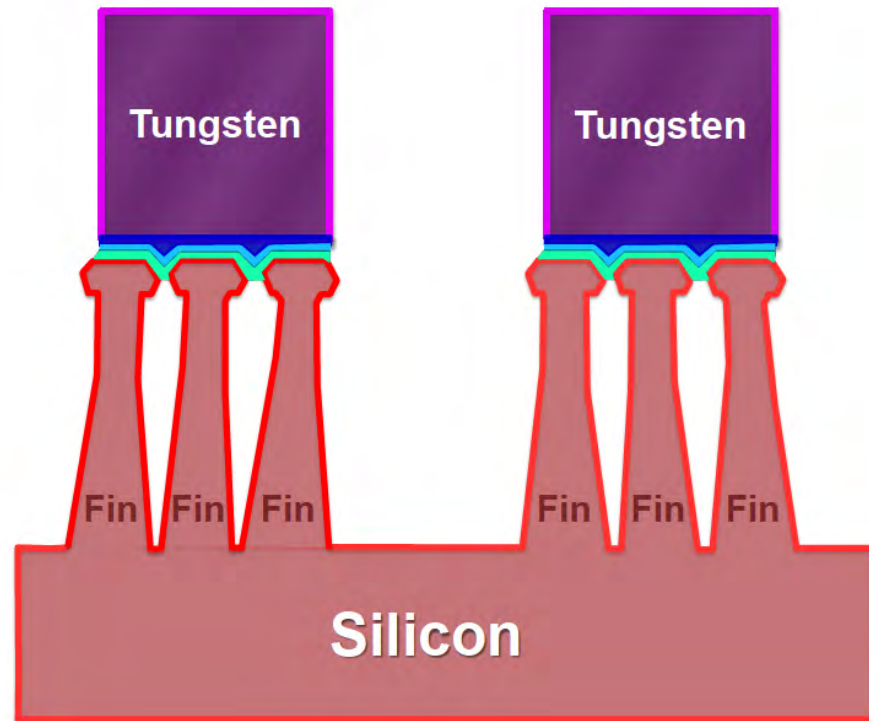


PTX00373-70

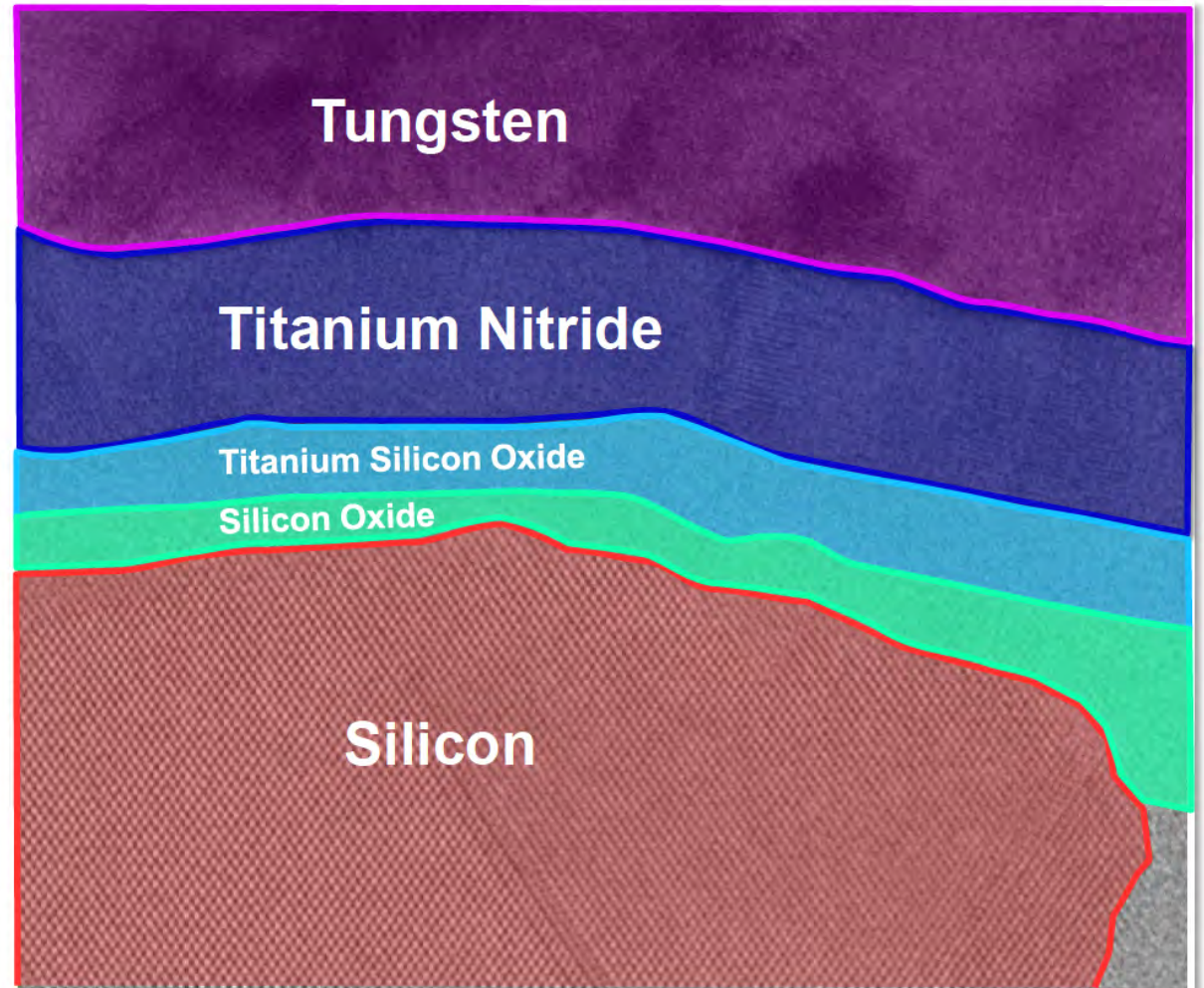
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Claim 17[c]: Distinct Layers of Oxide



Actual Samsung Transistor



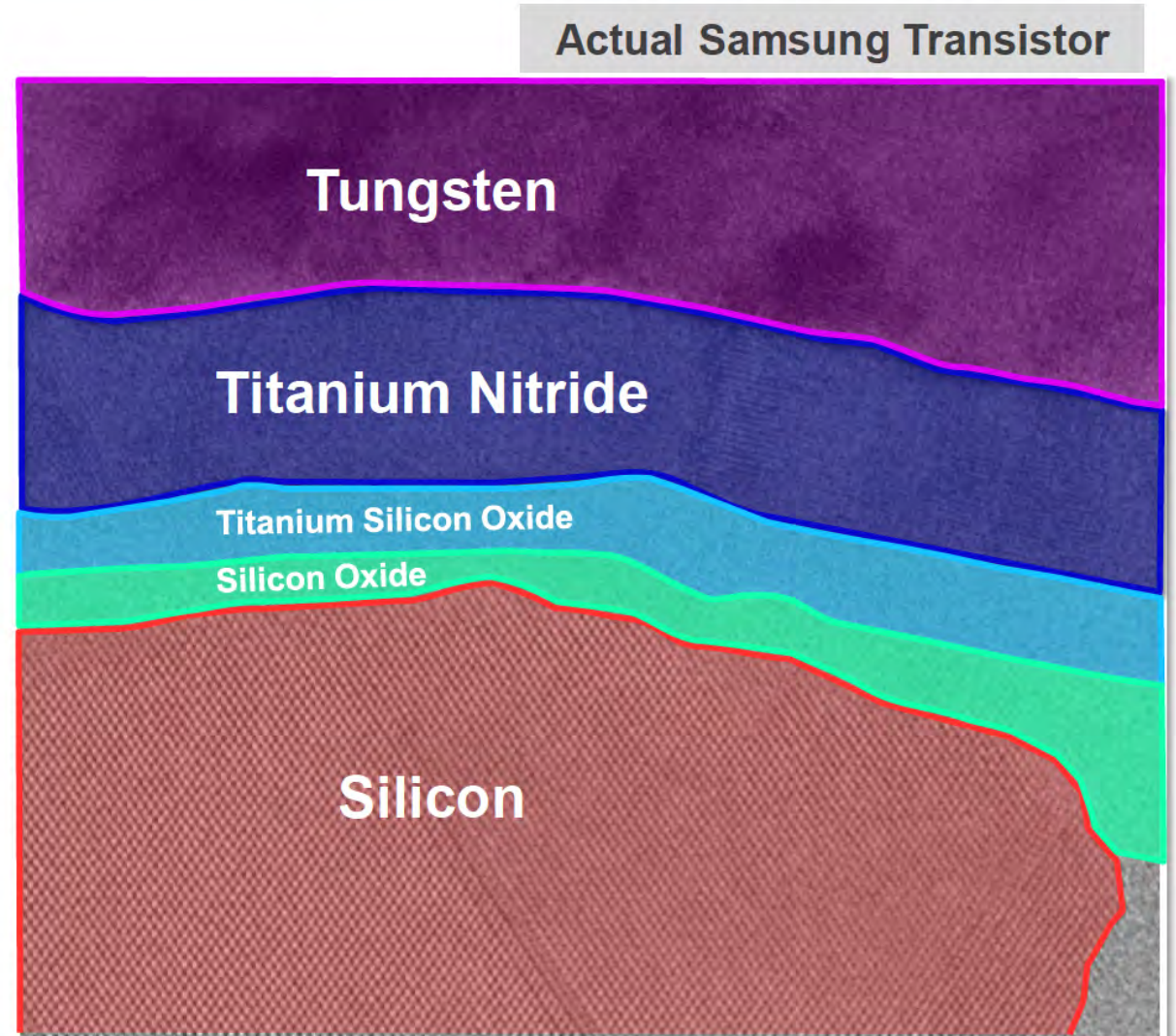
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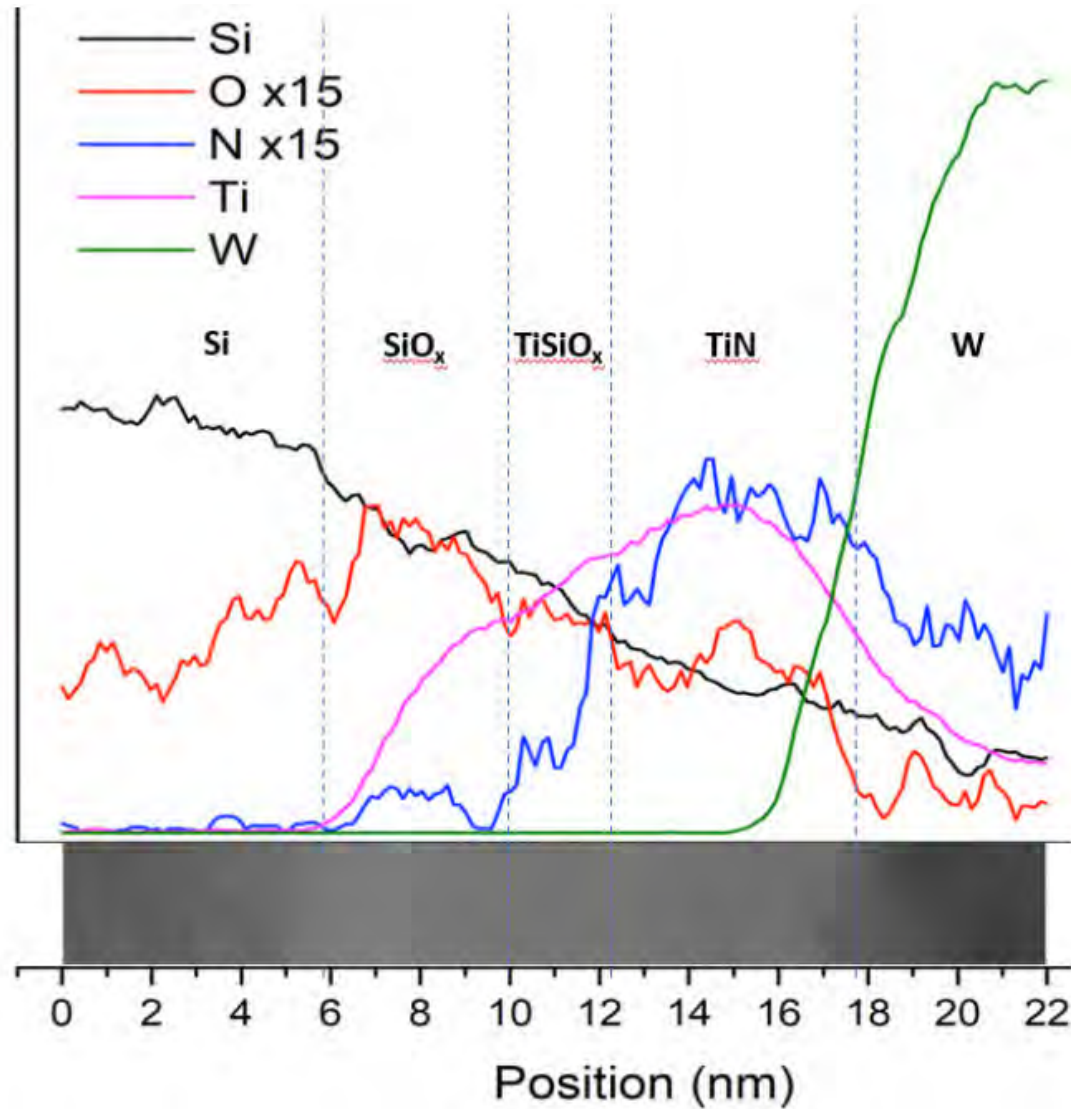
Claim 17[c]: Distinct Layers of Oxide

[17c] said interface layer comprising a layer of an oxide of titanium and a distinct layer of an oxide of the semiconductor.



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Elemental Analysis of Exynos 7885



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Elemental Analysis of Exynos 7884

