

Si dangling-bond-type defects at the interface of (100)Si with ultrathin layers of SiO_x , Al_2O_3 , and ZrO_2

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Electron spin resonance on (100)Si/ SiO_x / ZrO_2 and (100)Si/ Al_2O_3 / ZrO_2 stacks with nm-thin dielectric layers reveals the Si dangling-bond-type centers P_{b0} , P_{b1} as prominent defects at the (100)Si/dielectric interface. This P_{b0} , P_{b1} fingerprint indicates that, while gratifying for the Si/ SiO_x / ZrO_2 case, the as-deposited (100)Si/ Al_2O_3 interface is basically Si/ SiO_2 -like. The interfaces are in an enhanced (unrelaxed) stress state, characteristic of low-temperature Si/ SiO_2 growth. Based on the P_{b0} , P_{b1} criterion, standard thermal Si/ SiO_2 interface properties may be approached by appropriate annealing ($\geq 650^\circ\text{C}$) in vacuum in the case of Si/ SiO_x / ZrO_2 . Yet, O_2 ambient is required for Si/ Al_2O_3 , indicating that the initial abruptness of the interface prevents thermal adaptation to occur until an additional SiO_x interlayer grows. A minimal SiO_x interlayer thickness (≥ 0.5 nm) appears requisite. © 2002 American Institute of Physics.

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The relentless scaling of metal–oxide–silicon (MOS) based devices projects shrinking of the SiO_2 thickness (d_{SiO_2}) to the sub-2-nm range in the near future.¹ Yet, obstacles such as excessive leakage (tunneling) current, reduced drive current, and reliability issues, pose severe limitations² to such extreme reduction of d_{SiO_2} . One remedy is to use insulators of dielectric permittivity ϵ higher than SiO_2 ($\epsilon_{\text{SiO}_2} = \kappa_{\text{SiO}_2} \epsilon_0 = 3.9\epsilon_0$, where ϵ_0 is the vacuum permittivity), which should enable usage of thicker layers of equivalent SiO_2 capacitance thickness $d_{\text{EOT}} \equiv d_{\text{high } \kappa} \epsilon_{\text{SiO}_2} / \epsilon_{\text{high } \kappa}$. Though addressed before³ in connection with integrated circuit technology, this has recently propelled research^{4–6} in appropriate alternative high- κ materials for replacing SiO_2 gates in future deep sub- μm MOS generations.

Intensively studied alternative dielectrics include ZrO_2 ($\kappa \sim 20$), HfO_2 ($\kappa \sim 20$), and Al_2O_3 ($\kappa \sim 8.5$). Multiple high-sensitivity analytical techniques are combined to explore microstructural, compositional, and bonding chemistry aspects^{7–9} of ultrathin high- κ layers on Si. Electrical performance (transport, charge trapping) has been probed by capacitance–voltage (CV) and current–voltage (IV) measurements.¹⁰ Yet, as to the atomic nature of crucial point defects, which, as is well known, were demonstrated or hinted to be the origin of almost all electric imperfections in the case of c-Si/ SiO_2 , information on atomic scale has predominantly come from electron spin resonance (ESR) analysis (see, e.g., Ref. 11), often in conjunction with Si/ SiO_2 electrical probing. Particularly regarding the Si/ SiO_2 interface, this has revealed the atomic nature^{11–13} of a dominant class of interface traps, i.e., P_b -type (Si dangling-bond) defects: P_b ($\text{Si}_3 \equiv \text{Si}^\cdot$) in (111)Si/ SiO_2 , and P_{b0} and P_{b1} ($a\langle 211 \rangle$ oriented $\text{Si}_3 \equiv \text{Si}^\cdot$) in (100)Si/ SiO_2 . P_b and P_{b0} , evidenced as chemically identical, were both conclusively established as adverse electrical interface traps.^{14,15} This provided a landmark in structural modeling. So, in a complementary approach, ESR investigation is extended

here to stacks of ultrathin SiO_x and Al_2O_3 films sandwiched between (100)Si and thin ZrO_2 layers, with the aim of providing atomic identification and quantification of occurring defects and to analyze the influence of postdeposition thermal treatment. The known characteristics of the amply studied Si/ SiO_2 structure are used as a backdrop.

The samples studied were Si/ SiO_x / ZrO_2 and Si/ Al_2O_3 / ZrO_2 stacks, prepared on low-doped one-side-polished (100)Si wafers (p type; $n_a \sim 10^{15} \text{ cm}^{-2}$; $0.8 \mu\text{m}$ thick), last cleaned in aqueous HF (5% by weight). Uniform stoichiometric ultrathin layers of Al_2O_3 (~ 0.5 – 3 nm) and ZrO_2 (5 – 20 nm), as well as ultrathin SiO_x layers, were deposited at 300°C in an atomic-layer chemical-vapor deposition (ALCVD) reactor¹⁶ using $\text{Al}(\text{CH}_3)_3$ and H_2O , and ZrCl_4 and H_2O as precursors, respectively, at a pressure of ~ 1 Torr. The SiO_x layers (~ 5 Å) were grown in H_2O at 300°C for 20 min. Details can be found elsewhere.¹¹ From these wafers, 2×9 -mm²-area ESR samples were cut with their 9 mm edge along a $[011]$ direction. To analyze the thermal stability of deposited layers and interfaces, after initial ESR tests, some samples were subjected to additional annealings at ~ 650 and 800°C in vacuum ($< 4 \times 10^{-6}$ Torr) or dry O_2 (99.9995%; ~ 1.1 atm). A fresh sample was used for each additional thermal step.

cw K-band ESR measurements were performed at 4.3 K under conditions of adiabatic slow passage.¹⁷ Prior to some ESR observations, samples were submitted to VUV irradiation (8.48 eV; ~ 5 min) at room temperature (RT) in air to photodissociate H from (possibly) passivated defects (ESR-defect activation).¹² Concomitantly, it might reveal some nonideal (strained, weak) bonding.

As anticipated (cf. H-rich ambient used in ALCVD), only weak ESR signals could be observed in the as-deposited state [cf. Fig. 1(a)]. However, as illustrated in Fig. 1 for Si/ $\text{Al}_2\text{O}_3(0.5)/\text{ZrO}_2(5 \text{ nm})$, distinct signals do appear upon VUV irradiation. For the applied magnetic field $\mathbf{B} \parallel [100]$ interface normal $\mathbf{n}$ (i.e., magnet angle $\varphi_B = 0^\circ$), two clear signals are observed: a prominent one at $g = 2.0059 \pm 0.0001$,

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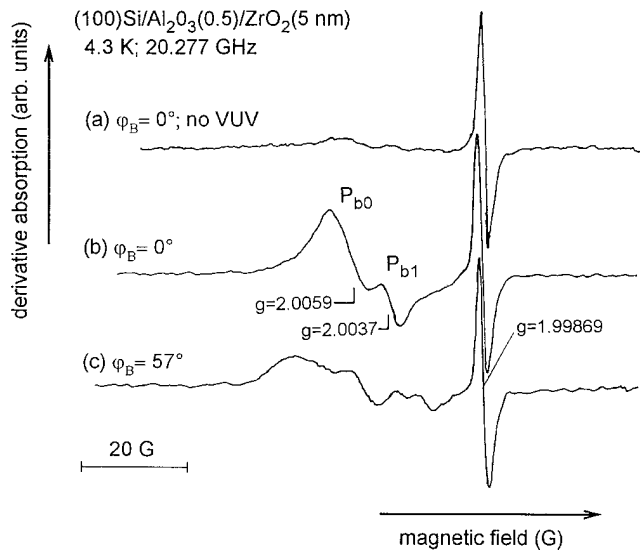


FIG. 1. ESR spectra observed at 4.3 K for two directions of $\mathbf{B}$ in the (011) plane on (100)Si/Al₂O₃(0.5)/ZrO₂(5 nm): (a) as grown; (b) and (c) after RT VUV irradiation (8.48 eV; ~5 min) revealing P_{b0} , P_{b1} defects at the Si/Al₂O₃ interface. The signal at $g=1.99869$ stems from a comounted Si:P marker. Applied modulation field amplitude was 0.4 G, and incident microwave power $P_\mu \sim 2$ nW.

with peak-to-peak width $\Delta B_{pp} = 9.7 \pm 0.4$ G, and a weaker one characterized by $g = 2.00375 \pm 0.0001$ and $\Delta B_{pp} = 3.75 \pm 0.2$ G, with spin ($S=1/2$) densities determined as 5.9 ± 0.3 and $(1.5 \pm 0.2) \times 10^{12} \text{ cm}^{-2}$ (intensity ratio $R \sim 3.9$), respectively.

The signals also exhibit distinct anisotropy, as evidenced by spectrum (c) in Fig. 1. They were decisively identified as originating from P_{b0} , P_{b1} —the well-known centers at the thermal Si/SiO₂ interface—by g mapping. The inferred principal g matrix values for P_{b0} ($g_{\parallel} = 2.00185$, $g_{\perp} = 2.0081$) and P_{b1} ($g_1 = 2.00577$, $g_2 = 2.00735$, $g_3 = 2.0022$) match those of previous work¹⁸ on conventional (100)Si/SiO₂. This strict crystallographic correlation with the Si substrate implies that the defects pertain to the nominal (100)Si/Al₂O₃ interface. This conclusion is confirmed by the study of simple (100)Si/Al₂O₃(3 nm) ALCVD structures.

Similar observations were made on the (100)Si/SiO_x(0.5)/ZrO₂(5 nm) structure, yet with two noticeable differences: First, as compared to the Si/Al₂O₃(0.5)/ZrO₂(5 nm) case, the signals are narrower, i.e., for $\mathbf{B} \parallel \mathbf{n}$, $\Delta B_{pp} = 6.8 \pm 0.4$ and 3.5 ± 0.2 G, for P_{b0} and P_{b1} , respectively. Second, relative to the P_{b0} signal (density = $4.3 \times 10^{12} \text{ cm}^{-2}$), the P_{b1} signal is weaker ($R \geq 9$). The observed linewidths may be compared with those observed in thermal Si/SiO₂ grown at $T > 900^\circ\text{C}$, given as $\Delta B_{pp} = 6.0 \pm 0.2$ and 3.3 ± 0.2 G, for P_{b0} and P_{b1} , respectively.¹⁸ It thus appears that as compared to standard Si/SiO₂, the linewidths observed in the structures here are broadened, the more so for the Si/Al₂O₃(0.5)/ZrO₂(5 nm) stack. There are two noteworthy results: (1) P_{b0} , P_{b1} are demonstrated as prominent defects at the Si/dielectric interface in both types of ALCVD-grown stacks studied. (2) As the P_{b0} , P_{b1} fingerprint is generally unique for the thermal (100)Si/SiO₂ interface, the results reveal that, while gratifying for the latter stack, the initial nominal (100)Si/Al₂O₃ interface is basically also (100)Si/SiO₂ type.

Besides excessive broadening, the P_{b0} , P_{b1} linewidths also exhibit field-angle dependence (see Fig. 1), a well-

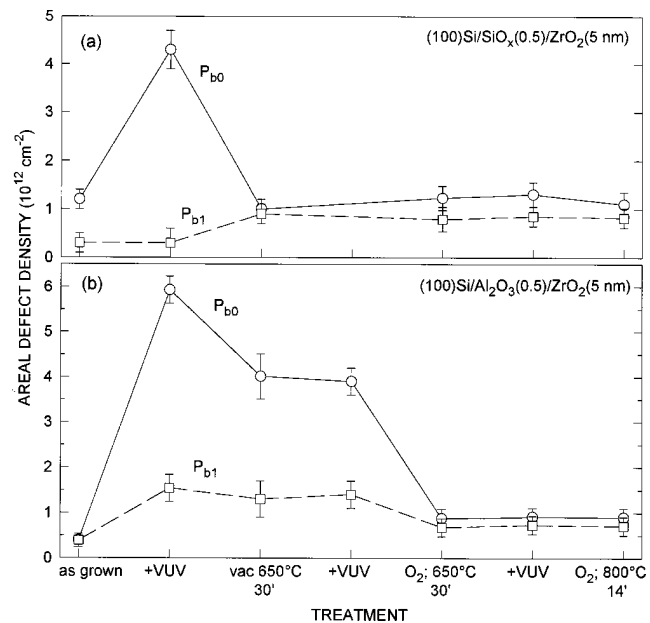


FIG. 2. Evolution of P_{b0} , P_{b1} defect densities at the Si/SiO_x interface in (100)Si/SiO_x(0.5)/ZrO₂(5 nm) (a) and (100)Si/Al₂O₃(0.5)/ZrO₂(5 nm) (panel b) stacks under various postdeposition treatments.

known characteristic first clearly quantified¹⁹ for P_b in (111)Si/SiO₂, and later also for P_{b0} , P_{b1} .¹⁸ It originates from mismatch (stress) induced local variations in the defect morphology over the various P_b sites, resulting in a (supposedly Gaussian) spread σ_g in g , predominantly in $g_{\perp}$. Analyzing along the lines outlined elsewhere,¹⁸ gives the values $\sigma_{g\perp}$ (P_{b0}) = 0.0011 ± 0.0001 and 0.00175 ± 0.00015 for (100)Si/SiO_x(0.5)/ZrO₂(5 nm) and Si/Al₂O₃/ZrO₂, respectively. As compared to the value $\sigma_{g\perp} = 0.00095 \pm 0.00005$ for thermal (100)Si/SiO₂, we thus find enhanced stress, in particular for the Si/Al₂O₃ interface.

Here, it is interesting to note that, in agreement with previous reports (see, e.g., Ref. 20), the observed P_{b0} , P_{b1} signature, i.e., the large P_{b0} system, strongly reduced P_{b1} signal—the large P_{b0} /feeble P_{b1} attribute—and broadened lines as compared to standard thermal Si/SiO₂, is the one characteristic of thermal Si/SiO₂ interfaces grown at reduced temperature.

More interesting information emerges after postdeposition annealing (PDA), as diagramed in Fig. 2 in terms of P_{b0} , P_{b1} densities—chosen as representative mark. As to Si/SiO_x(0.5)/ZrO₂(5 nm) [Fig. 2(a)], a first noteworthy observation is that upon annealing in vacuum at 650°C , the P_{b0} , P_{b1} densities attain values typical for standard (relaxed) Si/SiO₂: [P_{b0}] decreases drastically to $\sim 1 \times 10^{12} \text{ cm}^{-2}$, while [P_{b1}] grows to $\sim 1 \times 10^{12} \text{ cm}^{-2}$. This is observed to be attendant with narrowing of the linewidth to standard values— 6.0 ± 0.2 and 3.3 ± 0.2 for P_{b0} and P_{b1} , respectively, for $\mathbf{B} \parallel \mathbf{n}$ —bearing out reduced strain broadening. Pertinently, in line with the findings for the as-deposited state, these characteristics also comply with those of thermal Si/SiO₂ structures grown at low T . Here, it was also observed that upon simple PDA in vacuum ($\sim 750^\circ\text{C}$), more standard-like narrowed P_b and P_{b1} signals [with increased [P_{b1}] of $\sim (1.5-3) \times 10^{12} \text{ cm}^{-2}$] are retrieved.²⁰

Subsequently, the Si/SiO_x/ZrO₂ structures were subjected to PDA in oxygen at 650 and 800°C . However, this did not result in any noticeable further change in the ESR

spectrum, $[P_{b0}]$, $[P_{b1}]$ remaining unchanged within error, [cf. Fig. 2(a)]. This may not be surprising, as once a (close to) standard Si/SiO₂ interface realized, this is retained when regrowing at high(er) T .

Interestingly, PDA affects (100)Si/Al₂O₃(0.5)/ZrO₂ (5 nm) differently. As shown in Fig. 2(b), there is now only a modest impact of PDA in vacuum at 650 °C (30 min): $[P_{b0}]$ decreases (only) about 30%, while $[P_{b1}]$ remains unchanged at a density of $(1.45 \pm 0.3) \times 10^{12} \text{ cm}^{-2}$. This contrasts with the (100)Si/SiO_x/ZrO₂ case, where the P_{b0} , P_{b1} densities evolve to those of standard thermal Si/SiO₂. In broad terms, this finding for (100)Si/Al₂O₃/ZrO₂ is corroborated by results from previous microstructural and compositional analysis⁸ using nuclear reaction analysis and x-ray photoelectron spectroscopy, reporting all species to remain immobile under PDA in vacuum (~ 30 s) for T up to 800 °C. Yet, importantly, while broadly in agreement, the present ESR data reveal a limited change does occur in vacuum. Likely then, it only concerns a spatially very limited (perhaps on the scale of one atomic layer) modification (e.g., structural rearrangement/relaxation, some additional interfacial SiO_x growth), which has inherently escaped detection in previous probing. However, as shown in Fig. 2(b), a drastic difference is observed when changing to O₂ ambient: standard Si/SiO₂ $[P_{b0}]$, $[P_{b1}]$ values are attained after PDA at 650 °C in O₂ (30 min), with no further change for T increasing to 800 °C.

It is thus found that the Si/dielectric interface in Si/SiO_x/ZrO₂ may be upgraded (close) to that of standard thermal Si/SiO₂ by moderate annealing at $T \geq 650$ °C in vacuum, i.e., no additional O₂ supply needed—an interesting result when put in broader context. Indeed, previous work reported the ZrO₂ layer, under annealing at T up to ~ 900 °C (in vacuum or O₂) to be very stable against silicate formation and intermixing,^{6,9} hinting that, likely, no O is extracted from the ZrO₂ network to grow an additional SiO₂ interlayer. The present ESR results would thus indicate that with an initial SiO_x interlayer ~ 0.5 nm thick, annealing at $T \geq 650$ °C suffices to transform the Si/SiO_x interface in Si/SiO_x(0.5)/ZrO₂(nm) to standard like without (or marginal) additional SiO_x interlayer growth.

For the Si/Al₂O₃/ZrO₂ stack, by contrast, an additional supply of O₂ is required to upgrade the interface, i.e., likely, there is need for additional growth of the SiO_x interlayer. This may indicate that, in the as-grown state, the Si/Al₂O₃ interface—although clearly Si/SiO₂ type—is very abrupt, indeed, in agreement with previous work,⁷ and that essentially no thermal reshaping can occur without attendant growth of additional SiO_x layer(s). It suggests that to enable thermally induced upgrading of the interface, a minimal SiO_x thickness $d_{\text{SiO}_x}^{\text{min}}$ is required: The Si/SiO_x/ZrO₂ data suggest $d_{\text{SiO}_x}^{\text{min}} \geq 0.5$ nm. This may be compared with the value (~ 0.6 nm) inferred for the Si/Si₃N₄ case on the basis of electrical (CV, IV) data.⁴ Interestingly, $d_{\text{SiO}_x} \sim 0.7$ nm was also concluded to be the minimum layer thickness to obtain bulk (e.g., regarding band gap) SiO₂ properties.²¹ Pertinently, it may also be added that model calculations based on constraint theory bear out the necessity for interposing an ultrathin SiO₂ layer between the Si substrate and high- κ oxides (Al₂O₃, Ta₂O₅, TiO₂) to attain device grade interfaces.⁴

Finally, one may notice that the very specific ESR signature of the P_b -type interface defects is invoked here as criterion for technological interface quality. As amply evidenced before,^{11,15,17} technological interface quality is inextricably connected with a standard P_{b0} , P_{b1} fingerprint, both regarding inherent defect densities and salient ESR features—whatever the manufacturing facility. This criterion finds support from other disciplines. From the theory, the existence of an inherent interface defect density (dangling bonds) in standard thermal Si/SiO₂, is corroborated by the extension of constraint theory to Si/dielectric interfaces.²² On the experimental side, it falls in line with previous notions that with oxide layers deposited at reduced T on Si, low-interface trap density can only be obtained by deposition on thin oxides pregrown by standard high- T processing²³—effectively stating that only thermally grown Si/SiO₂ meets microelectronics requirements—or by providing a sufficient (higher- T) thermal budget.

In summary, the observed P_{b0}/P_{b1} signature, reassuring for the (100)Si/SiO_x/ZrO₂ case, reveals the initial Si/Al₂O₃ interface also to be basically Si/SiO₂ type. This apparently natural fact may contribute to successful application of high- κ metal oxides in future Si-based devices. Yet, the pertinent interfaces are found to be under enhanced stress, inherent to low- T fabrication. Upgrading (close) to that of standard thermal (100)Si/SiO₂ may be realized through providing appropriate thermal budget. A minimum SiO_x interlayer thickness (≥ 0.5 nm) appears necessary. It heralds the potential to carry over the unexcelled properties of (100)Si/SiO₂ towards the Si/metal–oxide entities. But, obviously, the presence of an SiO_x interlayer will impair ultimate d_{EOT} optimization.

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