Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

CLAIMS JPH07263375

1.
A method of making an ohmic contact on an n-type semiconductor layer of a III-V compound semiconductor, comprising first forming a metal contact layer on the n-type semiconductor layer, then forming a gold layer on the metal contact layer, and then forming a gold layer on the metal contact layer. A method of heat-treating the obtained array in a heat treatment step, wherein the metal contact layer is made of AuGeNi, and the germanium content and nickel content of each do not exceed 1% by weight.

2.
The method according to claim 1, characterized in that the layer arrangement is heat-treated at 360-390 ° C. for 40-180 minutes.

3.
Method according to claim 1, characterized in that the layer arrangement is heat-treated at 430-480 ° C for 5-20 seconds.

4.
4. The method according to claim 1, wherein the nickel content in the AuGeNi layer is 0.5% by weight.

5.

GF Exhibit 1124 - 1454/2704

Method according to one of the claims 1 to 4, characterized in that the germanium content in the AuGeNi layer is 0.4% by weight.

6.
Method according to one of the claims 1 to 5, characterized in that the thickness of the AuGeNi layer is in the range 50-200 nm.

7.
Method according to one of the claims 1 to 6, characterized in that the thickness of the gold layer is in the range 250 to 1000 nm.

8.
Method according to one of claims 1 to 7, characterized in that, prior to the heat treatment step, first a TiWN layer and then an aluminum layer is deposited on the metal covering the AuGeNi layer.

9.
The method according to claim 8, wherein the thickness of the TiWN film layer is in the range of 100 to 500 nm.

10.
A method according to claim 8 or 9, characterized in that the thickness of the aluminum layer is in the range of 1 to 3 µm.

11.
10. The method according to claim 1, wherein the contact arrangement is structured before the heat treatment step.

GF Exhibit 1124 - 1455/2704

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号

特開平8－167693

(43)公開日　平成８年(1996)６月25日

(51)Int.Cl.[6]	識別記号	庁内整理番号	ＦＩ		技術表示箇所
Ｈ０１Ｌ 27/04					
21/822					
29/861					
			Ｈ０１Ｌ 27/ 04	Ｃ	
			29/ 91	Ｆ	

審査請求　未請求　請求項の数10　ＯＬ　（全 ９ 頁）

(21)出願番号　特願平6－311823

(22)出願日　平成６年(1994)12月15日

(71)出願人　000005049
シャープ株式会社
大阪府大阪市阿倍野区長池町22番22号

(72)発明者　松本　信之
大阪府大阪市阿倍野区長池町22番22号　シャープ株式会社内

(72)発明者　宮宇地　真人
大阪府大阪市阿倍野区長池町22番22号　シャープ株式会社内

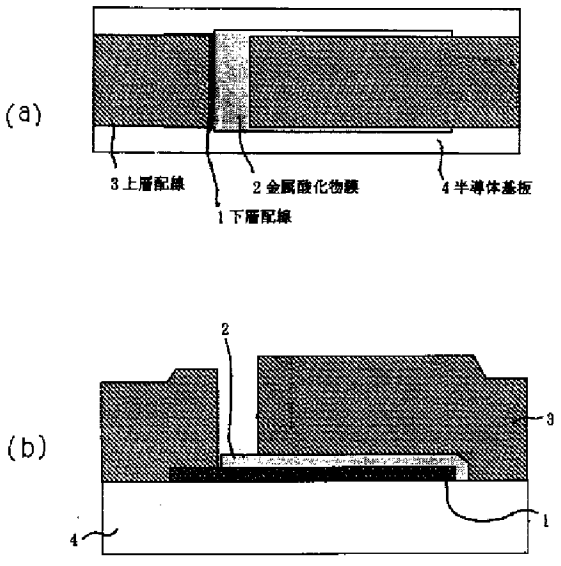
(74)代理人　弁理士　野河　信太郎

(54)【発明の名称】　半導体装置及びその製造方法

(57)【要約】

【目的】　充分な酸素欠陥を形成して実用的な電流（～ｍＡ）が流せる金属酸化物を利用した、ダイオード並びにキャパシタとして動作する半導体装置を提供することを目的とする。

【構成】　この発明の半導体装置は、半導体基板上に、金属酸化物とショットキィ接触を形成する金属により構成された任意の形状の下層配線と、酸素欠陥を有する金属酸化物膜を挟んで、酸素との親和力が該金属酸化物膜に含まれる金属より大きい金属より構成される任意の形状の上層配線をもつ縦型構造を特徴とする。



GF Exhibit 1124 - 1456/2704

【特許請求の範囲】
【請求項１】　半導体基板上に、金属酸化物とショットキィ接触を形成する金属により構成された任意の形状の下層配線と、酸素欠陥を有する金属酸化物膜を挟んで、酸素との親和力が該金属酸化物膜に含まれる金属より大きい金属より構成される任意の形状の上層配線をもつ縦型構造を特徴とする半導体装置。
【請求項２】　下層配線が、金属酸化物膜と接する上部表面に白金層を有し、上層配線が、金属酸化物膜と接する下部表面にチタン層を有してなる請求項１記載の半導体装置。
【請求項３】　下層配線が、チタン／白金の積層体からなり、上層配線が、チタン／金又はチタン／白金／金の積層体からなる請求項１又は２記載の半導体装置。
【請求項４】　金属酸化物膜が、バリウムチタン酸ストロンチウム（$Ba_xSr_{1-x}TiO_3$ ；$0 \leqq x \leqq 0.7$）である請求項１～３いずれか１つに記載の半導体装置。
【請求項５】　半導体基板と下層配線の間に、窒化シリコン膜又は酸化シリコン膜が挟まれてなる請求項１～４いずれか１つに記載の半導体装置。
【請求項６】　半導体装置が、ダイオードとして使用される請求項１～５いずれか１つに記載の半導体装置。
【請求項７】　下層配線が、上層配線と相対的に一定のＤＣ負バイアスを絶縁を破壊しない範囲で印加してキャパシタとして使用される請求項１～５いずれか１つに記載の半導体装置。
【請求項８】　一定のＤＣ負バイアスが、－０．５Ｖ～－１０Ｖである請求項７記載の半導体装置。
【請求項９】　回路内に、同じ工程で作製した請求項６と請求項７又は８の半導体装置が構成素子として含まれてなることを特徴とする集積回路半導体装置。
【請求項１０】　請求項１～９の金属酸化物膜が、金属酸化物膜を構成する金属のアルコキシドからなる前駆体溶液を下層配線上へ塗布し、次いで焼成を空気中３００℃～５００℃の範囲で行なうことからなる加水分解を利用したゾルゲル法により形成されてなることを特徴とする半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】この発明は、半導体装置及びその製造方法に関する。更に詳しくは、この発明は、金属酸化物を用いた半導体装置及びその製造方法に関する。
【０００２】
【従来の技術】純粋な金属酸化物の場合、３から４ｅＶと大きいバンドギャップを有するので絶縁体としての性質を示す。しかし、酸素欠陥が存在すると、ドナー準位が生じ、ｎ型の半導体導電性を示す。金属酸化物は、上記のように大きいバンドギャップを有するので、電流を流すための適当なキャリアを酸素欠陥によって生じさせれば、高耐圧特性を示すダイオードとしての利用が期待される。
【０００３】金属酸化物をチャネルとして利用する半導体装置として、第１１回強誘電体応用会議講演予稿集ｐ２７－ｐ２８に示されているもの（文献１）が挙げられる。即ち、この文献１では酸化マグネシウム（ＭｇＯ）上にレーザーアブレーション法によって形成したチタン酸ストロンチウム（$SrTiO_3$）をチャネルに用いた薄膜トランジスタにおいて、ニオブ（Ｎｂ）をオーミックメタルとして用い、オーミック形成領域にアルゴン（Ａｒ）イオンの注入を行なって酸素欠陥を作りキャリアを形成している。得られた半導体装置の特性は、ゲート幅２０μｍに対し、１００ｎＡの電流が得られている程度である。
【０００４】また、金属酸化物を用いた半導体装置のうち、金属酸化物の絶縁特性と高誘電率特性を用いた半導体装置としての利用は、例えば、日経マイクロデバイス、ｐ１１１～ｐ１１６、１９９２年１月号（文献２）及び特開平５－２６７５６５号公報（文献３）にも示されている。即ち、文献２では、Ｓｉ基板上にマグネトロンスパッタで形成した$Ba_{0.5}Sr_{0.5}TiO_3$を用い、金属酸化物の高温の熱工程を受ける下側の電極に熱工程による劣化の少ないＰｔ／Ｔａを用い、上側の電極にＴｉＮを用いたＤＲＡＭ用のキャパシタが記載されている。一方、文献３では、誘電体にゾルゲル法で形成した$Ba_{0.7}Sr_{0.3}TiO_3$を用い、その下側の電極にＰｔ／Ｔｉ、上側の電極にＰｔを用いたキャパシタが記載されている。
【０００５】また文献２では、５００℃以上で熱処理を施すと、Ｐｔ／Ｔｉ電極に反応が生じ、信頼性の低下を生じることも報告されている。
【０００６】
【発明が解決しようとする課題】金属酸化物をチャネルとした薄膜トランジスタとして使用している文献１では、電極とコンタクトする部分にＡｒイオン注入を行なって酸素欠陥を形成することによりn^+層を形成しているが、チャネルの$SrTiO_3$には、充分な酸素欠陥、すなわちキャリアが形成されていないので、実用的な電流が流れないと考えられる。
【０００７】また、この文献１のデバイスは、金属電極が金属酸化物膜の両端にある横型構造であり、電流が流れる方向の金属酸化物の距離が長く、電流が流れ難い構造である。実際、この例での金属酸化物膜の通過電流は、ゲート幅２０μｍに対して、１００ｎＡ程度であり、デバイスとして実用的な電流（～ｍＡ）は、得られていない。
【０００８】金属酸化物を高誘電体として用いた半導体装置の従来例、即ち文献２及び３では、キャパシタとして用いる場合、金属酸化物の高誘電率特性を利用するので、リーク電流の存在によって、例えば、ＤＲＡＭのメ

GF Exhibit 1124 - 1457/2704

モリーに蓄積されている電荷が消失し、キャパシタとしての特性を劣化させる。このために、文献２のように、ペロブスカイト型の結晶化を促進するため６５０℃でのスパッタ成膜や、文献３のように７００℃以上の高温の酸素処理等によって結晶化を促進し、金属酸化物のリーク電流を現象させる工夫を行なっている。

【０００９】しかしながら、高温でのスパッタ成膜や、高温の酸素中焼成が必要なために、低温での処理が必要なＳｉやＧａＡｓ等の半導体素子とのプロセス温度の整合が取れない。このために、文献２のように、Ｐｔ／Ｔａを電極に採用したり、ＦＥＴを先に作り込む従来の工程では、ＩＣの多層配線がキャパシタの上下電極として使用できるのにもかかわらず、文献３では、ＦＥＴ作製工程より以前にキャパシタをつくりこむため、キャパシタ用の電極を別工程でつくる必要が生じている。このような電極や工程の大幅な変化は、電極材料への悪影響（信頼性の低下）や、製造コストの大幅な増加をもたらす。

【００１０】このように、従来の技術では、金属酸化物を半導体材料として利用する場合、金属酸化物に充分な酸素欠陥が簡単には形成されず、電流を制御通過できる半導体層としての特性を利用することが困難であり、そのオーミック接触電極の形成においても、あえてＡｒイオンの注入を行ないｎ$^{+}$ 層を形成するなど、工程が複雑になる問題があった。

【００１１】また、金属酸化物を高誘電率の絶縁体として利用する場合、高温処理が必要なため、ＳｉやＧａＡｓ等の半導体基板上に形成する場合、電極や、製造工程の変更が必要になり、信頼性の低下や、製造コストの増加をもたらす問題があった。従って、この発明は、充分な酸素欠陥を形成して実用的な電流（～ｍＡ）が流せる金属酸化物を利用した、ダイオード並びにキャパシタとして動作する半導体装置を提供することを目的とする。

【００１２】

【課題を解決するための手段】かくしてこの発明によれば、半導体基板上に、金属酸化物とショットキィ接触を形成する金属により構成された任意の形状の下層配線と、酸素欠陥を有する金属酸化物膜を挟んで、酸素との親和力が該金属酸化物膜に含まれる金属より大きい金属より構成される任意の形状の上層配線をもつ縦型構造を特徴とする半導体装置が提供される。

【００１３】更に、この発明によれば、上記金属酸化物膜が、金属酸化物膜を構成する金属のアルコキシドからなる前駆体溶液を下層配線上へ塗布し、次いで焼成を空気中３００℃～５００℃の範囲で行なうことからなる加水分解を利用したゾルゲル法により形成されてなることを特徴とする半導体装置の製造方法も提供される。この発明に使用できる半導体基板としては、特に限定されず、シリコン、ＧａＡｓ等が挙げられる。この半導体基板上には下層配線が配設されるが、その前に窒化シリコン、酸化シリコン等の絶縁膜を形成しておいてもよい。絶縁膜を半導体基板上に形成することにより、基板上に形成された他の半導体装置との製造工程の整合性を良好にすることができる。絶縁膜の厚さは、３００～５０００Åである。

【００１４】次に、この発明に使用できる下層配線は、後に説明する金属酸化物膜を構成する金属とショットキィ接触を形成する金属からなる。下層配線に使用できる金属としては、例えば、白金、チタン、タングステン等が挙げられ、このうち、白金が好ましい。下層配線の厚さは５００～２００００Åであり、更に６０００～１００００Åであることが好ましい。ここで、５００Åより小さいと配線が高抵抗化して好ましくなく、２００００Åより大きいと電極エッジの段差が大きくなりすぎるので好ましくない。また、下層配線は必ずしも１層からなる必要はなく、２層以上であってもよい。例えば、２層からなる場合は、チタン／白金、アルミニウム／白金等の積層体が挙げられる。このうち、チタン／白金からなる積層体が半導体基板及び金属酸化物膜との密着力を考慮すると好ましく、厚さはチタン層が５００～１０００Åであり、白金層が５００～２０００Åである。なお、下層配線は金属酸化物膜と接する上部表面に白金層が形成されていることが好ましい。これは、白金層が酸化されにくく、金属酸化物膜とある程度の密着力があるためである。下層配線の形成方法は、特に限定されず、スパッタ法、真空蒸着法等が挙げられ、所望の形状にするためにフォトリソグラフ法により成形してもよい。

【００１５】次に、上記上層配線の上には、酸素欠陥を有する金属酸化物膜が形成される。この発明に使用できる金属酸化物としては、例えば、$Ba_x Sr_{1-x} TiO_3$（$0 \leqq x \leqq 0.7$）、$SrTiO_3$、$BaMgF_4$、$LiNbO_3$、$LiTaO_3$、$CaBi_4 Ti_4 O_{15}$、$KNbO_3$、$NaNbO_3$ 等の高誘電率材料が挙げられる。このうち、$Ba_x Sr_{1-x} TiO_3$（$0 < x \leqq 0.7$、特に$0.5 < x \leqq 0.7$）が好ましい。また、金属酸化物層の厚さは１０００～３０００Åであり、更に２０００～２５００Åであることが好ましい。ここで、１０００Åより小さいと破壊耐圧が著しく小さくなるので好ましくなく、３０００Åより大きいと形成時にストレスによりクラックが生じるので好ましくない。金属酸化物膜の形成方法は、ゾルゲル法が好ましい。この方法は、金属酸化物を構成する金属のアルコキシドからなる前駆体溶液を、例えばスピンコート等により塗布し、３００～５００℃の低温で焼成することにより金属酸化物膜を形成する方法である。焼成温度が３００℃より低い場合、金属酸化物膜の結晶化が十分ではなく、５００℃より高い場合、半導体装置の製造工程自体を変更する必要があり、また新たな配線材料の選択が必要となり、信頼性の低下及び製造コストを増加させるので好ましくない。このような形成条件では完全な結晶状態（ペロブス

GF Exhibit 1124 - 1458/2704

カイト構造）とならないが、比誘電率が２０～３０のものを得ることができる。この値は、ＳｉＮに比べて４～６倍の比誘電率であり、絶縁体を金属で挟んだ構造のＭＩＭ（メタル／絶縁体／メタル）キャパシタ材料として使用することができる。また、金属酸化物膜は、所望の形状にするためにフォトリソグラフ法により成形してもよい。

【００１６】次に、金属酸化物膜の上には上層配線が形成される。この発明に使用できる上層配線は、上記で説明した金属酸化物膜を構成する金属より酸素に対する親和力の大きい金属からなる。上層配線に使用できる金属としては、例えば、チタン、白金、金、アルミニウム等が挙げられ、このうち、チタンが好ましい。上層配線の厚さは５００Å～１０μｍであり、更に２～１０μｍであることが好ましい。ここで、５００Åより小さいと高抵抗化し好ましくなく、１０μｍより大きいと製作が困難なので好ましくない。また、上層配線は必ずしも１層からなる必要はなく、２層以上であってもよい。例えば、２層からなる場合は、チタン／金、白金／金等の積層体が挙げられ、３層からなる場合は、チタン／白金／金、タングステン／白金／金等の積層体が挙げられる。このうち、チタン／金、チタン／白金／金からなる積層体が半導体基板及び金属酸化物膜との密着力を考慮すると好ましく、厚さは２層の場合、チタン層が５００～１０００Åであり、金層が２～１０μｍであり、一方３層の場合、チタン層が５００～１０００Åであり、白金層が１０００～２０００Åであり、金層が２～１０μｍである。なお、上層配線は金属酸化物膜と接する下部表面にチタン層が形成されていることが好ましい。これは、チタン層が金属酸化物膜の表面から酸素を奪うことにより酸化チタンを形成し、金属酸化物膜表面に高濃度の酸素欠乏層を形成し、オーミック接触を形成することができるからである。上層配線の形成方法は、特に限定されず、スパッタ法、真空蒸着法等が挙げられ、所望の形状にするためにフォトリソグラフ法により成形してもよい。

【００１７】この発明の縦型構造を有する半導体装置は、キャパシタ、ダイオード、バイパスコンデンサ等に使用することができる。例えば、下層配線が、上層配線と相対的に一定のＤＣ負バイアスを絶縁を破壊しない範囲で印加することによりキャパシタとして使用することができる。一定のＤＣ負バイアスに固定して、金属酸化物膜を流れる電流を抑制すると、金属酸化物膜は絶縁体としての特性を示し、ロスの小さいキャパシタとして動作する。なお、一定のＤＣ負バイアスは、－０．５～－１０Ｖが好ましい。－１０Ｖより大きいと絶縁が破壊される恐れがあるので好ましくなく、－０．５Ｖより小さいと回路に制約が多いので好ましくない。

【００１８】また、上記では、簡単のため、１つの半導体装置のみを例として説明したが、２つ以上の半導体装置を同時に形成してもよく、他の半導体装置と組み合わせてもよい。

【００１９】

【作用】この発明の半導体装置は、半導体基板上に、金属酸化物とショットキィ接触を形成する金属により構成された任意の形状の下層配線と、酸素欠陥を有する金属酸化物膜を挟んで、酸素との親和力が該金属酸化物膜に含まれる金属より大きい金属より構成される任意の形状の上層配線をもつ縦型構造を特徴とするので、半導体基板上に高耐圧の素子を形成することができ、基板上に形成されたその他の能動素子とともに動作させることができ集積回路の高性能化が図られる。

【００２０】また、下層配線が、金属酸化物膜と接する上部表面に白金層を有し、上層配線が、金属酸化物膜と接する下部表面にチタン層を有してなるので、下部配線と金属酸化物膜間ではショットキィ接触が、上部配線と金属酸化物膜間ではオーミック接触が形成される。また、金属酸化物膜の上下配線の金属を変えることで、縦方向に実用的な電流密度１～１０Ａ／ｃｍ^2 の電流を流すことができる半導体装置が提供される。

【００２１】更に、下層配線が、チタン／白金の積層体からなり、上層配線が、チタン／金又はチタン／白金／金の積層体からなるので、更に特性の良好な半導体装置が得られる。また、金属酸化物が、バリウムチタン酸ストロンチウム（$Ba_x\ Sr_{1-x}\ TiO_3$ ；０≦ｘ≦０．７）であるので、従来のＳｉＮ等の絶縁物を使用したものと比べて比誘電率が向上した半導体装置が得られる。

【００２２】更に、半導体基板と下層配線の間に、窒化シリコン又は酸化シリコンが挟まれてなることにより、半導体基板上の他の半導体装置とのプロセス整合が良好となる。また、半導体装置が、ダイオードとして使用されるので、高耐圧のダイオードが得られる。

【００２３】更に、下層配線が、上層配線と相対的に一定のＤＣ負バイアスを絶縁を破壊しない範囲で印加してキャパシタとして使用するので、金属酸化物膜の絶縁体としての特性が示され、ロスの少ないキャパシタが得られる。また、一定のＤＣ負バイアスが、－０．５Ｖ～－１０Ｖであるので、更にロスの少ないキャパシタが得られる。

【００２４】更に、回路内に、同じ工程で作製したダイオードとキャパシタが構成素子として含まれてなるので、キャパシタとダイオードが同一の工程で形成される。また、金属酸化物膜が、金属酸化物膜を構成する金属のアルコキシドからなる前駆体溶液を下層配線上へ塗布し、次いで焼成を空気中３００℃～５００℃の範囲で行なうことからなる加水分解を利用したゾルゲル法により形成されてなるので、十分な通過電流（１～１０Ａ／ｃｍ^2 ）を奏する酸素欠陥状態が維持される。

【００２５】

【実施例】以下、この発明を実施例をもとに説明する

GF Exhibit 1124 - 1459/2704

が、この発明は実施例に限定されるものではない。

実施例１

図１に示す半導体装置を形成した。なお、図１（ａ）は平面図、（ｂ）は断面図を表す。図１中１は白金からなる下層配線、２はバリウムチタン酸ストロンチウム（$Ba_x Sr_{1-x} TiO_3$，ｘ＝０．５又は０．７）からなる金属酸化物膜、３はチタンからなる上層配線、４はＧａＡｓからなる絶縁性半導体基板を示している。

【００２６】まず、絶縁性半導体基板４上にレジストをスピンコート法により塗布し、フォトリソグラフィ法によりレジストに１１０μｍ×１５０μｍの矩形のスペースパターンを形成した。この基板４上にチタンをスパッタ法により厚さ２５００Åで堆積し、リフトオフにより１１０μｍ×１５０μｍの矩形の下層配線１のパターンを形成した。

【００２７】次に、この基板４上に後にバリウムチタン酸ストロンチウム（$Ba_x Sr_{1-x}TiO_3$ ｘ＝０．５又は０．７）となる金属アルコキシドからなる前駆体溶液を、スピンコート法により厚さ２０００Åに塗布した。この後、空気中で１５０℃、１５分間乾燥させ、続いて空気中で５００℃、１時間の焼成を行い金属酸化物膜２を形成した。次いで、金属酸化物膜２上にレジストをスピンコート法により塗布し、エッチングにより下層配線１を一部露出させ、コンタクト用のホールを形成すると共に、不要な部分の金属酸化物膜を取り去った。なお、エッチャントは５％バッファーフッ酸：塩酸：純水（１：１：２）溶液とし、この溶液に１５秒浸すことによりエッチングを行った。

【００２８】次に、上記基板４上にレジストをスピンコート法により塗布し、フォトリソグラフィ法によりレジストにスペースパターンを形成した。この基板４上に白金をスパッタ法により厚さ２μｍで堆積し、リフトオフにより上層配線３のパターンを形成することにより図１に示す如き半導体装置を形成した。なお、下層配線１と上層配線３が金属酸化物膜２を介して接している面積は１００μｍ×１００μｍであった。

【００２９】実施例２

図５に示す半導体装置を図２～４に基づいて形成した。なお、図２～５において（ａ）は平面図、図２（ｂ）は断面図を示している。図２～５中１～４は図１と同じであり、５はチタン層、６は白金層、７は金層、８はＳｉＮからなる絶縁膜を示している。

【００３０】まず、絶縁性半導体基板４上にＳｉＮからなる絶縁膜８を厚さ２０００ÅでＰＣＶＤ法により形成した。次に、実施例１と同様にして、１１０μｍ×１５０μｍのレジストからなる矩形のスペースパターンを形成し、スパッタ法によりチタン層５を５００Å、白金層６を２０００Åこの順で堆積し、リフトオフにより１１０μｍ×１５０μｍの矩形の下層配線１のパターンを形成した（図２（ａ）及び（ｂ）参照）。

【００３１】次に、実施例１と同様にして、金属酸化物膜２を下層配線１上に形成した。なお、ｘは０．７とした（図３（ａ）及び（ｂ）参照）。次に、実施例１と同様にして、レジストからなるパターンを形成し、スパッタ法によりチタン層５を５００Å、金層７を２μｍこの順で堆積し、リフトオフにより上層配線３のパターンを形成した（図４（ａ）及び（ｂ）参照）。

【００３２】この後レジストを取り除くことにより、図５に示す如き半導体装置を得た。なお、下層配線１と上層配線３が金属酸化物膜２を介して接している面積は１００μｍ×１００μｍであった。図６は、図５の構成において、焼成を５００℃で１時間行なった厚み２０００Åの$Ba_{0.7} Sr_{0.3} TiO_3$を金属酸化物膜２に用いた半導体装置の下層配線１に与える電圧と、下層配線から上層配線３に半導体装置を流れる電流の関係を示すグラフである。

【００３３】図６から明らかなように、下層配線に－１０Ｖ印加しても、電流はほとんど流れず、良好なダイオード特性を示している。また、下層配線に、－１０Ｖ以下の範囲で長時間電圧を印加した場合、高誘電体に流れる電流が増加し、絶縁破壊に到った。

実施例３

図７に示す半導体装置を、上層配線３の形成において、チタン層５と金層７の間に厚さ１００Åの白金層６を形成すること、絶縁膜８をSiO_2にすること以外は、実施例２と同様の工程を繰り返すことにより形成した。

【００３４】図８は、図７の構成において、焼成を３００℃で１時間行なった厚み２０００Åの$Ba_{0.5} Sr_{0.5} TiO_3$を金属酸化物膜２に用いた半導体装置の、下層配線１に与える電圧と、下層配線１から上層配線３に半導体装置を流れる規格化電流の関係を示す。図８では、上層配線３の寸法を、２０μｍ×１０μｍ～２００μｍ×２００μｍまで、変化させている。

【００３５】図８から明らかなように、順方向電流は、上層配線３の面積に依存していることが判る。また、－８～－１０Ｖまで下層電極にＤＣバイアスを印加しても、ほとんど逆方向電流は流れず、＋２～３ＶのＤＣバイアスを印加すると、実用レベルの順方向電流（約１Ａ／cm^2）が流れる。このことは、この発明によって得られる半導体装置が、逆耐圧の高いダイオードとして動作することを示している。更に、下層電極に印加されるＤＣバイアスを－２Ｖに固定すると、電流が10^{-6}～10^{-4}Ａ／cm^2に抑制され、良好なリーク特性を示す。

【００３６】実施例４

図９は、この発明の半導体装置を、キャパシタとして用いる際の回路構成の一例を示す。なお、図９中Ａは、下層配線１、金属酸化物膜２及び上層配線３からなるこの発明の半導体装置である。下層配線１に、－５Ｖ印加した際の１～１５ＧＨｚの比誘電率は、$Ba_{0.7} Sr_{0.3} TiO_3$の場合が３０、$Ba_{0.5} Sr_{0.5} TiO_3$の場

GF Exhibit 1124 - 1460/2704

合が２５、$SrTiO_3$ の場合が２０であった。これら高誘電体金属酸化物で本来得られる比誘電率（１００～３００）は得られていないが、ＳｉＮが５．６，SiO_2 が４であることに比べると、これらの金属酸化物で作ったキャパシタは、４～７倍の容量を示すことが判った。従って、同じ厚みのＳｉＮやSiO_2 を使う場合、キャパシタ面積を１／４～１／７に縮小することが可能である。

【００３７】実施例５

図１０は、この発明の半導体装置を同一基板上でダイオード及びキャパシタとして使用する場合の回路構成の一例を示している。同じデバイス構造でも、キャパシタとダイオードを一度に作りこむことが可能で、プロセスの簡略化が可能になる。

【００３８】

【発明の効果】この発明の半導体装置は、半導体基板上に、金属酸化物とショットキィ接触を形成する金属により構成された任意の形状の下層配線と、酸素欠陥を有する金属酸化物膜を挟んで、酸素との親和力が該金属酸化物膜に含まれる金属より大きい金属より構成される任意の形状の上層配線をもつ縦型構造を特徴とするので、半導体基板上に高耐圧の素子を形成することができ、基板上に形成されたその他の能動素子とともに動作させることができ集積回路の高性能化を図ることができる。

【００３９】また、下層配線が、金属酸化物膜と接する上部表面に白金層を有し、上層配線が、金属酸化物膜と接する下部表面にチタン層を有してなるので、下部配線と金属酸化物膜間ではショットキィ接触を、上部配線と金属酸化物膜間ではオーミック接触を形成することができる。また、金属酸化物膜の上下配線の金属を変えることで、縦方向に実用的な電流密度１～１０Ａ／cm^2 の電流を流すことができる半導体装置を提供できる。

【００４０】更に、下層配線が、チタン／白金の積層体からなり、上層配線が、チタン／金又はチタン／白金／金の積層体からなるので、更に特性の良好な半導体装置を得ることができる。また、金属酸化物が、バリウムチタン酸ストロンチウム（$Ba_x\ Sr_{1-x}\ TiO_3$ ；$0 \leqq x \leqq 0.7$）であるので、従来のＳｉＮ等の絶縁物を使用したものと比べて比誘電率が向上した半導体装置を得ることができる。

【００４１】更に、半導体基板と下層配線の間に、窒化シリコン又は酸化シリコンが挟まれてなることにより、半導体基板上の他の半導体装置とのプロセス整合が良好となる。また、半導体装置が、ダイオードとして使用されるので、高耐圧のダイオードが得られる。

【００４２】更に、下層配線が、上層配線と相対的に一定のＤＣ負バイアスを絶縁を破壊しない範囲で印加してキャパシタとして使用するので、金属酸化物膜の絶縁体としての特性が示され、ロスの少ないキャパシタを得ることができる。また、一定のＤＣ負バイアスが、－０．５Ｖ～－１０Ｖであるので、更にロスの少ないキャパシタを得ることができる。

【００４３】更に、回路内に、同じ工程で作製したダイオードとキャパシタが構成素子として含まれてなるので、キャパシタとダイオードが同一の工程で形成することができる。また、金属酸化物膜が、金属酸化物膜を構成する金属のアルコキシドからなる前駆体溶液を下層配線上へ塗布し、次いで焼成を空気中３００℃～５００℃の範囲で行なうことからなる加水分解を利用したゾルゲル法により形成されてなるので、十分な通過電流（１～１０Ａ／cm^2 ）を奏する酸素欠陥状態を維持することができる。また、焼成を低温で行うことができるので、半導体基板上に形成される他の半導体装置の製造工程を大幅に変更することはなく、信頼性の低下を生じさせる電極材料の選択も不要である。従って、信頼性の低下の問題や、製造コストは増加しない。

【図面の簡単な説明】

【図１】この発明の半導体装置の概略平面図及び断面図である。

【図２】この発明の半導体装置の製造工程の概略平面図及び断面図である。

【図３】この発明の半導体装置の製造工程の概略平面図及び断面図である。

【図４】この発明の半導体装置の製造工程の概略平面図及び断面図である。

【図５】この発明の半導体装置の概略平面図及び断面図である。

【図６】この発明の半導体装置の電流と下層配線への印加電圧との関係を示すグラフである。

【図７】この発明の半導体装置の概略平面図及び断面図である。

【図８】この発明の半導体装置の電流と下層配線への印加電圧との関係を示すグラフである。

【図９】この発明の半導体装置をキャパシタとして使用した場合の回路構成図である。

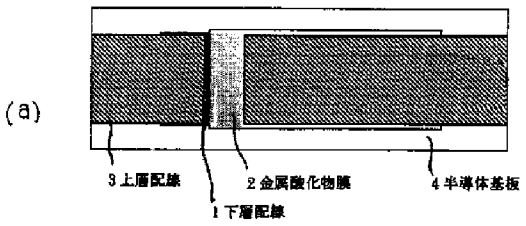
【図１０】この発明の半導体装置を同一基板上でダイオード及びキャパシタとして使用した場合の回路構成図である。

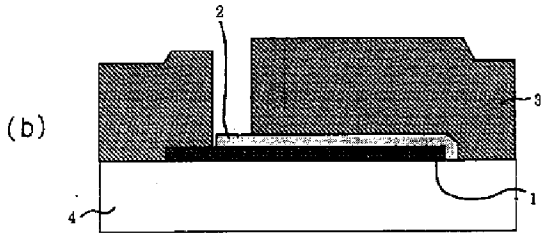
【符号の説明】

１　下層配線
２　金属酸化物膜
３　上層配線
４　半導体基板
５　チタン層
６　白金層
７　金層
８　絶縁膜
Ａ　半導体装置

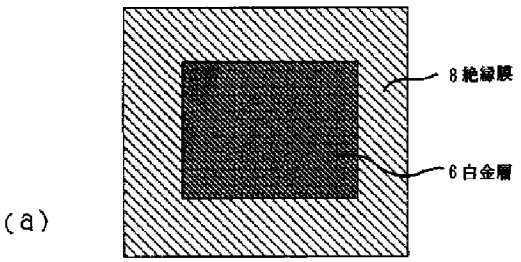
GF Exhibit 1124 - 1461/2704

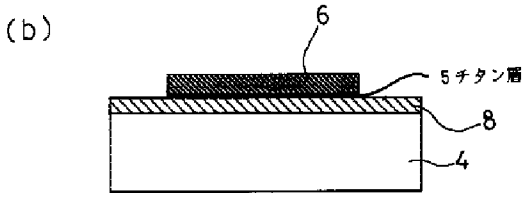
【図1】



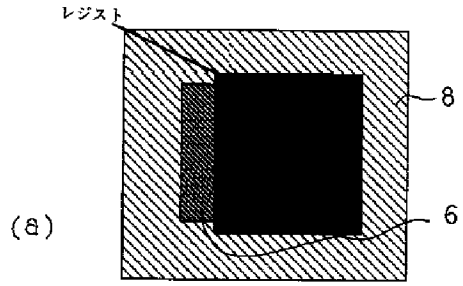


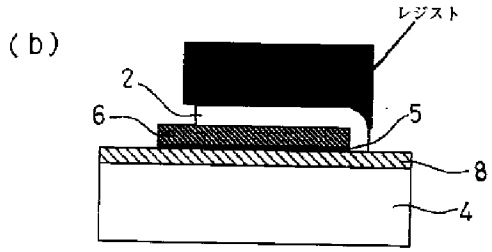
【図2】



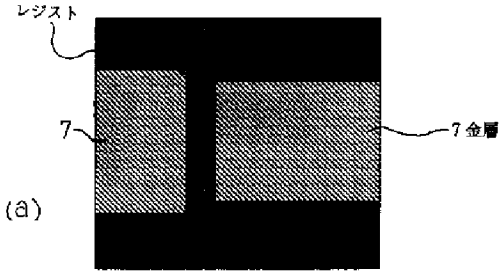


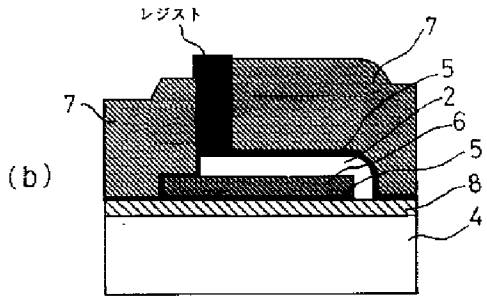
【図3】





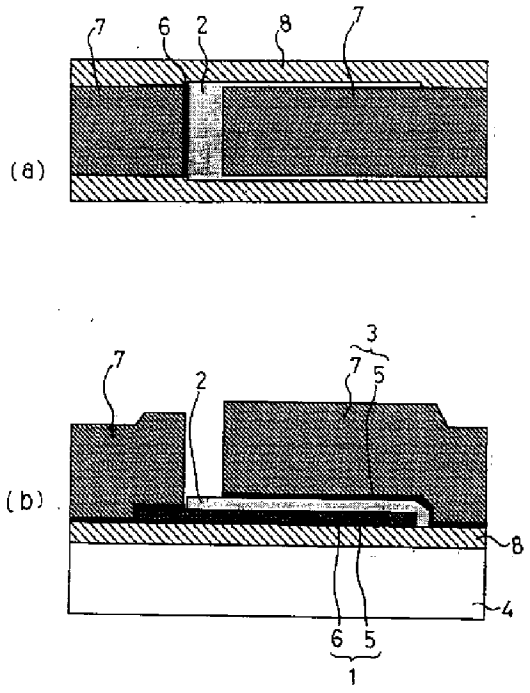
【図4】



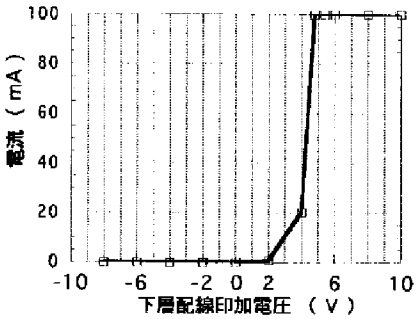


GF Exhibit 1124 - 1462/2704

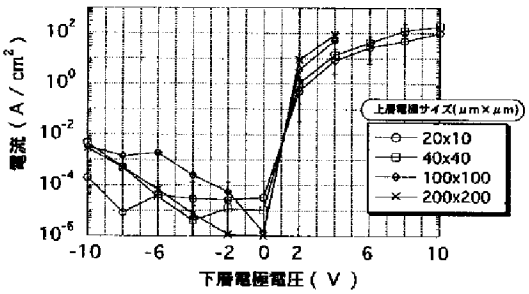
【図5】



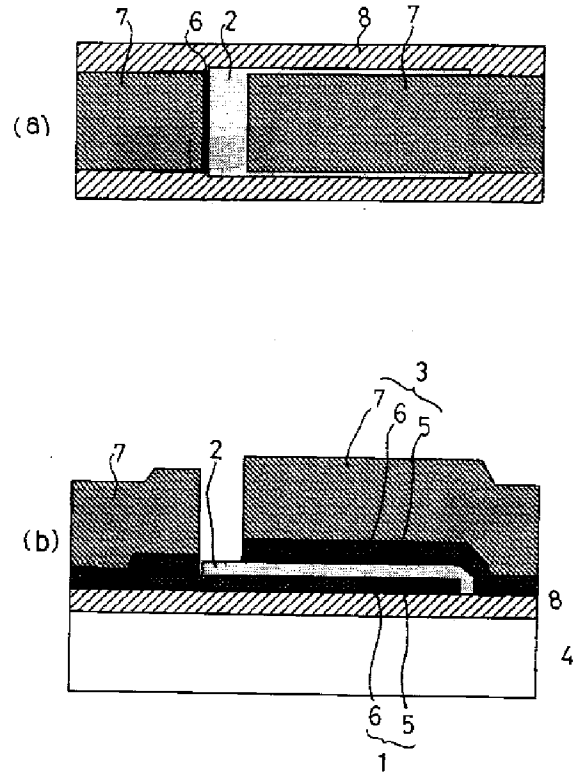
【図6】



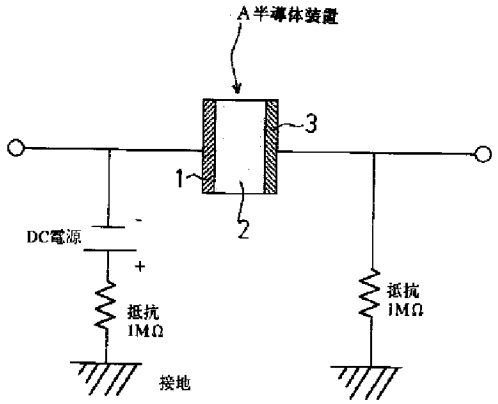
【図8】



【図7】

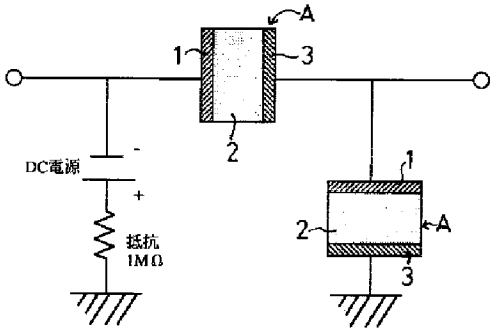


【図9】



GF Exhibit 1124 - 1463/2704

【図１０】



Europäisches Patentamt
European Patent Office
Office européen des brevets

Espacenet

JPH08167693A SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

Applicants: SHARP KK

Inventors: MATSUMOTO NOBUYUKI,MIYAUCHI MASATO

Classifications:
IPC ***H01L21/822; H01L27/04; H01L29/861;*** (IPC1-7): H01L21/822; H01L27/04; H01L29/861;

Priorities: JP31182394A 1994-12-15

Application: JPH08167693A·1994-12-15

Publication: JPH08167693A·1996-06-25

Published as: JPH08167693A;**JP3198453B2**

SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

Abstract

PURPOSE: To raise the performance of an integrated circuit by forming a vertical structure which has lower-layer wiring and upper-layer wiring in an optional shape consisting of each specified metal, on a semiconductor substrate. CONSTITUTION: A vertical structure, which has lower-layer wiring 1 in an optional shape consisting of metal to form Schottky contact with a metallic oxide and upper-layer wiring 3 in optional shape consisting of metal whose affinity with oxygen is larger than that of the metal contained in a metallic oxide film 2, with a metallic oxide film 2 having oxygen defect between, is made on a semiconductor substrate 4. The metallic oxide film 2 is made by sol gel method making use of the hydrolysis by applying precursor solution consisting of alkoxide of metal constituting the metallic oxide film 2 on the lower-layer wiring 1, and baking it in the range of 300 deg.C-500 deg.C in air. Hereby, a high breakdown strength element can be made on the semiconductor substrate 4, and it can be operated together with other active elements made on the substrate 4, so that an integrated circuit can enhance performance.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION JPH08167693

[0001]
BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor device and its manufacturing method. More specifically, the present invention relates to a semiconductor device using a metal oxide and a method for manufacturing the same.

[0002]

2. Description of the Related Art In the case of a pure metal oxide, it has a large band gap of 3 to 4 eV and thus exhibits a property as an insulator. However, in the presence of oxygen defects, a donor level is generated, and n-type semiconductor conductivity is exhibited. Since the metal oxide has a large band gap as described above, it is expected to be used as a diode exhibiting a high withstand voltage characteristic if oxygen carriers generate suitable carriers for passing a current.

[0003]

As a semiconductor device using a metal oxide as a channel, the one shown in Proceedings of the 11th Ferroelectric Application Conference p27-p28 (Reference 1) can be mentioned. That is, in Document 1, in a thin film transistor using strontium titanate (SrTiO3) formed on a magnesium oxide (MgO) by a laser ablation method as a channel, niobium (Nb) is used as an ohmic metal and argon (Ar) is formed in an ohmic formation region.) Ions are implanted to create oxygen defects

GF Exhibit 1124 - 1466/2704

and form carriers. The characteristics of the obtained semiconductor device are such that a current of 100 nA is obtained for a gate width of 20 μm.

[0004]

Further, among semiconductor devices using metal oxides, the use as a semiconductor device using the insulating properties and high dielectric constant properties of metal oxides is described in, for example, Nikkei Microdevice, p111 to p116, January 1992 issue (Reference 2) and Japanese Patent Laid-Open No. 267565/1993 (Reference 3). That is, in Reference 2, Ba0.5 Sr0.5 TiO3 formed by magnetron sputtering on a Si substrate is used, and Pt / Ta, which is less deteriorated by the thermal process, is used for the lower electrode which is subjected to the high temperature thermal process of the metal oxide. A capacitor for DRAM using TiN for the upper electrode is described. On the other hand, Document 3 describes a capacitor in which Ba0.7Sr0.3TiO3 formed by a sol-gel method is used as a dielectric, Pt / Ti is used as the lower electrode and Pt is used as the upper electrode.

[0005]
Further, in Document 2, it is also reported that when heat treatment is performed at 500 ° C. or higher, a reaction occurs in the Pt / Ti electrode and reliability is lowered.

[0006]
In Reference 1, which is used as a thin film transistor using a metal oxide as a channel, Ar ion implantation is performed in a portion in contact with an electrode to form an oxygen defect, thereby forming an n + layer. However, since sufficient oxygen defects, that is, carriers are not formed in the SrTiO3 of the channel, it is considered that a practical current does not flow.

[0007]

Further, the device of Document 1 has a horizontal structure in which metal electrodes are provided at both ends of the metal oxide film, and the distance of the metal oxide in the direction in which the current flows is long, so that the current hardly flows.

In fact, the current passing through the metal oxide film in this example is about 100 nA for a gate width of 20 μm, and a practical current (mA) as a device has not been obtained.

GF Exhibit 1124 - 1467/2704

[0008]

In a conventional example of a semiconductor device using a metal oxide as a high dielectric, that is, in Documents 2 and 3, the high dielectric constant characteristic of the metal oxide is used when used as a capacitor. The electric charge accumulated in the memory disappears, and the characteristics as a capacitor are deteriorated.

For this reason, as in Reference 2, the crystallization is promoted by sputter film formation at 650 ° C. in order to promote crystallization of the perovskite type or by oxygen treatment at a temperature of 700 ° C. or higher as in Reference 3. , We are making efforts to make the leakage current of metal oxides a phenomenon.

[0009]

However, since the sputtering film formation at a high temperature and the baking in oxygen at a high temperature are required, the process temperature cannot be matched with that of a semiconductor element such as Si or GaAs that needs a low temperature treatment. Therefore, as in Reference 2, in the conventional process of adopting Pt / Ta for the electrode or forming the FET first, the multilayer wiring of the IC can be used as the upper and lower electrodes of the capacitor. In No. 3, since the capacitor is formed before the FET manufacturing process, it is necessary to form the capacitor electrode in another process. Such a drastic change in the electrode and the process causes an adverse effect on the electrode material (reduction in reliability) and a drastic increase in manufacturing cost.

[0010]

As described above, in the conventional technique, when a metal oxide is used as a semiconductor material, sufficient oxygen defects are not easily formed in the metal oxide, and the characteristics of the semiconductor layer that can control and pass an electric current are used. However, in forming the ohmic contact electrode, there is a problem that the process is complicated, such as intentionally implanting Ar ions to form an n + layer.

[0011]

GF Exhibit 1124 - 1468/2704

Further, when using a metal oxide as an insulator having a high dielectric constant, high temperature treatment is required. Therefore, when it is formed on a semiconductor substrate such as Si or GaAs, it is necessary to change an electrode or a manufacturing process. However, there is a problem that the productivity is lowered and the manufacturing cost is increased.

Therefore, an object of the present invention is to provide a semiconductor device that operates as a diode and a capacitor, which uses a metal oxide capable of forming a sufficient oxygen defect and allowing a practical current (-mA) to flow.

[0012]
Thus, according to the present invention, an underlayer wiring of any shape made of a metal forming a Schottky contact with a metal oxide and a metal oxide having an oxygen defect are formed on a semiconductor substrate. Provided is a semiconductor device characterized by a vertical structure having an upper layer wiring of any shape made of a metal having an affinity for oxygen higher than that of a metal contained in the metal oxide film with a physical film sandwiched therebetween.

[0013]

Further, according to the present invention, the metal oxide film is formed by applying a precursor solution composed of an alkoxide of a metal forming the metal oxide film onto the lower layer wiring, and then baking the same in air at 300 ° C to 500 ° C. Also provided is a method for manufacturing a semiconductor device, which is formed by a sol-gel method utilizing hydrolysis, which is performed in the range of

The semiconductor substrate that can be used in the present invention is not particularly limited, and examples thereof include silicon and GaAs. The lower layer wiring is provided on this semiconductor substrate, but an insulating film of silicon nitride, silicon oxide or the like may be formed before that. By forming the insulating film on the semiconductor substrate, it is possible to improve the compatibility of the manufacturing process with other semiconductor devices formed on the substrate. The thickness of the insulating film is 300 to 5000 Å.

[0014]

GF Exhibit 1124 - 1469/2704

Next, the lower layer wiring that can be used in the present invention is made of a metal forming a metal oxide film, which will be described later, and a metal forming a Schottky contact. Examples of the metal that can be used for the lower layer wiring include platinum, titanium, and tungsten. Of these, platinum is preferable. The thickness of the lower layer wiring is 500 to 20000 Å, preferably 6000 to 10000 Å. Here, if it is less than 500 Å, the wiring becomes high in resistance, which is not preferable, and if it is more than 20000 Å, the step difference of the electrode edge becomes too large, which is not preferable. Further, the lower layer wiring does not necessarily have to be composed of one layer and may be composed of two or more layers. For example, when it is composed of two layers, a laminate of titanium / platinum, aluminum / platinum, etc. may be mentioned. Of these, a laminate of titanium / platinum is preferable in consideration of the adhesion to the semiconductor substrate and the metal oxide film, and the titanium layer has a thickness of 500 to 1000 Å and the platinum layer has a thickness of 500 to 2000 Å. The lower wiring preferably has a platinum layer formed on the upper surface in contact with the metal oxide film. This is because the platinum layer is not easily oxidized and has a certain degree of adhesion to the metal oxide film. The method for forming the lower layer wiring is not particularly limited, and examples thereof include a sputtering method and a vacuum vapor deposition method, and the lower layer wiring may be formed by a photolithographic method in order to obtain a desired shape.

[0015]

Next, a metal oxide film having oxygen defects is formed on the upper wiring. Examples of the metal oxide usable in the present invention include high dielectric constant materials such as Bax Sr1-x TiO3 (0 x 0.7), SrTiO3, BaMgF4, LiNbO3, LiTaO3, CaBi4 Ti4 O15, KNbO3, and NaNbO3. Can be mentioned. Of these, Bax Sr1-x TiO3 (0 <x 0.7, particularly 0.5 <x 0.7) is preferable. Further, the thickness of the metal oxide layer is 1000 to 3000 Å, and preferably 2000 to 2500 Å. Here, if it is less than 1000 Å, the breakdown voltage is remarkably reduced, and if it is more than 3000 Å, cracks are generated due to stress during formation, which is not preferable. The method of forming the metal oxide film is preferably the sol-gel method. This method is a method of forming a metal oxide film by applying a precursor solution composed of a metal alkoxide constituting a metal oxide by, for example, spin coating and baking at a low temperature of 300 to 500 ° C. . If the firing temperature is lower than 300 ° C, the crystallization of the metal oxide film is not sufficient, and if it is higher than 500 ° C, the manufacturing process of the semiconductor device itself needs to be changed, and a new wiring material needs to be selected. It is not preferable because it becomes necessary and the reliability is lowered and the manufacturing cost is increased. Under such forming conditions, a perfect crystalline state (perovskite structure) is not obtained, but a dielectric constant of 20 to 30 can be obtained. This value is 4 to 6 times as high as that of SiN and can be used as an MIM (metal / insulator / metal)

GF Exhibit 1124 - 1470/2704

capacitor material having a structure in which an insulator is sandwiched between metals. Further, the metal oxide film may be formed by a photolithography method so as to have a desired shape.

[0016]

Next, an upper wiring is formed on the metal oxide film. The upper layer wiring that can be used in the present invention is made of a metal having a greater affinity for oxygen than the metal forming the metal oxide film described above. Examples of the metal that can be used for the upper layer wiring include titanium, platinum, gold, aluminum and the like, and among these, titanium is preferable. The upper wiring has a thickness of 500 Å to 10 μm, and preferably 2 to 10 μm. Here, if it is less than 500 Å, the resistance becomes high, which is not preferable, and if it is more than 10 μm, it is difficult to manufacture. Further, the upper layer wiring does not necessarily have to be composed of one layer and may be composed of two or more layers. For example, in the case of two layers, a laminate of titanium / gold, platinum / gold, etc. may be mentioned, and in the case of three layers, a laminate of titanium / platinum / gold, tungsten / platinum / gold, etc. may be mentioned. Of these, a laminate of titanium / gold and titanium / platinum / gold is preferable in consideration of the adhesiveness to the semiconductor substrate and the metal oxide film, and when the thickness is two layers, the titanium layer has a thickness of 500 to 1000 Å, The gold layer is 2-10 μm, while in the case of three layers the titanium layer is 500-1000 Å, the platinum layer is 1000-2000 Å and the gold layer is 2-10 μm. The upper wiring preferably has a titanium layer formed on the lower surface in contact with the metal oxide film. This is because the titanium layer can form titanium oxide by depriving the surface of the metal oxide film of oxygen, form a high-concentration oxygen-deficient layer on the surface of the metal oxide film, and form ohmic contact. is there. The method for forming the upper layer wiring is not particularly limited, and examples thereof include a sputtering method, a vacuum vapor deposition method, and the like, and the upper layer wiring may be formed by a photolithography method in order to obtain a desired shape.

[0017]

The semiconductor device having the vertical structure of the present invention can be used for capacitors, diodes, bypass capacitors, and the like. For example, the lower layer wiring can be used as a capacitor by applying a constant DC negative bias relative to the upper layer wiring within a range that does not destroy the insulation. When the current flowing through the metal oxide film is suppressed by fixing it to a constant DC negative bias, the metal oxide film exhibits characteristics as an insulator and operates as a capacitor with low loss. The constant DC

GF Exhibit 1124 - 1471/2704

negative bias is preferably -0.5 to -10V. If it is higher than -10V, the insulation may be broken, which is not preferable, and if it is lower than -0.5V, there are many restrictions on the circuit, which is not preferable.

[0018]

Further, in the above description, only one semiconductor device is described as an example for simplicity, but two or more semiconductor devices may be formed at the same time or may be combined with another semiconductor device.

[0019]

According to the semiconductor device of the present invention, a lower layer wiring of any shape made of a metal forming a Schottky contact with a metal oxide and a metal oxide film having an oxygen defect are sandwiched on a semiconductor substrate. Since a vertical structure having an upper wiring of arbitrary shape made of a metal having an affinity for oxygen higher than that of the metal contained in the metal oxide film is formed, a high breakdown voltage element can be formed on a semiconductor substrate. Therefore, it can be operated together with other active elements formed on the substrate, and high performance of the integrated circuit can be achieved.

[0020]

In addition, since the lower wiring has a platinum layer on the upper surface in contact with the metal oxide film and the upper wiring has a titanium layer on the lower surface in contact with the metal oxide film, the lower wiring and the metal oxide film are Schottky contact is formed between the upper wiring and the metal oxide film, and ohmic contact is formed between the upper wiring and the metal oxide film.

Further, by changing the metal of the upper and lower wirings of the metal oxide film, a semiconductor device capable of passing a current having a practical current density of 1 to 10 A / cm @ 2 in the vertical direction is provided.

[0021]

Furthermore, since the lower layer wiring is made of a titanium / platinum laminated body and

GF Exhibit 1124 - 1472/2704

the upper layer wiring is made of a titanium / gold or titanium / platinum / gold laminated body, a semiconductor device having further excellent characteristics can be obtained.

Further, since the metal oxide is barium strontium titanate (Bax Sr1-x TiO3; $0 \leqq x \leqq 0.7$), the relative dielectric constant is improved as compared with the conventional one using an insulator such as SiN. A semiconductor device can be obtained.

[0022]

Further, since silicon nitride or silicon oxide is sandwiched between the semiconductor substrate and the lower layer wiring, the process matching with other semiconductor devices on the semiconductor substrate becomes good. Further, since the semiconductor device is used as a diode, a high breakdown voltage diode can be obtained.

[0023]

Further, since the lower layer wiring applies a DC negative bias, which is relatively constant to the upper layer wiring, within a range where the insulation is not destroyed, and is used as a capacitor, the characteristics of the metal oxide film as an insulator are exhibited and the loss is small. A capacitor is obtained. Further, since the constant DC negative bias is -0.5V to -10V, a capacitor with less loss can be obtained.

[0024]

Furthermore, since the diode and the capacitor manufactured in the same process are included in the circuit as constituent elements, the capacitor and the diode are formed in the same process. In addition, the metal oxide film is formed by applying a precursor solution composed of a metal alkoxide constituting the metal oxide film onto the lower layer wiring, and then performing firing in air in the range of 300 ° C to 500 ° C. Since it is formed by a sol-gel method utilizing hydrolysis, an oxygen deficiency state that provides a sufficient passing current (1 to 10 A / cm2) is maintained.

[0025]

GF Exhibit 1124 - 1473/2704

EXAMPLES The present invention will be described below based on examples, but the present invention is not limited to the examples. The semiconductor device shown in FIG. 1 was formed. 1A is a plan view and FIG. 1B is a sectional view. In FIG. 1, 1 is a lower layer wiring made of platinum, 2 is a metal oxide film made of barium strontium titanate (Bax Sr1-x TiO3, x = 0.5 or 0.7), 3 is an upper layer wiring made of titanium, 4 Indicates an insulating semiconductor substrate made of GaAs.

[0026]

First, a resist was applied on the insulating semiconductor substrate 4 by spin coating, and a 110 μm × 150 μm rectangular space pattern was formed on the resist by photolithography. Titanium was deposited to a thickness of 2500 Å on the substrate 4 by a sputtering method, and a pattern of a rectangular lower layer wiring 1 of 110 μm × 150 μm was formed by lift-off.

[0027]

Next, a precursor solution of a metal alkoxide which later becomes barium strontium titanate (Bax Sr1-x TiO3 x = 0.5 or 0.7) was applied on the substrate 4 by a spin coating method to a thickness of 2000 Å. Then, it was dried in air at 150 ° C. for 15 minutes, and subsequently baked in air at 500 ° C. for 1 hour to form a metal oxide film 2. Next, a resist was applied onto the metal oxide film 2 by a spin coating method, a part of the lower wiring 1 was exposed by etching, a hole for contact was formed, and an unnecessary portion of the metal oxide film was removed. The etchant was a 5% buffer hydrofluoric acid: hydrochloric acid: pure water (1: 1: 2) solution, and etching was performed by immersing the solution in this solution for 15 seconds.

[0028]

Next, a resist was applied on the substrate 4 by spin coating, and a space pattern was formed on the resist by photolithography. Platinum was deposited on the substrate 4 to a thickness of 2 μm by a sputtering method, and a pattern of the upper wiring 3 was formed by lift-off to form a semiconductor device as shown in FIG. The area where the lower layer wiring 1 and the upper layer wiring 3 were in contact with each other through the metal oxide film 2 was 100 μm × 100 μm.

GF Exhibit 1124 - 1474/2704

[0029]

Example 2 The semiconductor device shown in FIG. 5 was formed based on FIGS. 2 to 5, (a) is a plan view and FIG. 2 (b) is a sectional view. 2 to 5, 1 to 4 are the same as those in FIG. 1, 5 is a titanium layer, 6 is a platinum layer, 7 is a gold layer, and 8 is an insulating film made of SiN.

[0030]

First, the insulating film 8 made of SiN was formed on the insulating semiconductor substrate 4 to a thickness of 2000 Å by the PCVD method. Next, in the same manner as in Example 1, a rectangular space pattern made of a resist having a size of 110 μm × 150 μm was formed, a titanium layer 5 was deposited in a thickness of 500 Å and a platinum layer 6 was deposited in a thickness of 2000 Å in this order, and 110 μm × was lifted off. A 150 μm rectangular lower layer wiring 1 pattern was formed (see FIGS. 2A and 2B).

[0031]

Next, in the same manner as in Example 1, the metal oxide film 2 was formed on the lower layer wiring 1. Note that x was 0.7 (see FIGS. 3A and 3B). Then, in the same manner as in Example 1, a resist pattern was formed, a titanium layer 5 of 500 Å and a gold layer 7 of 2 μm were deposited in this order by a sputtering method, and a pattern of the upper wiring 3 was formed by lift-off (See FIGS. 4 (a) and 4 (b)).

[0032]

After that, the resist was removed to obtain a semiconductor device as shown in FIG. The area where the lower layer wiring 1 and the upper layer wiring 3 were in contact with each other through the metal oxide film 2 was 100 μm × 100 μm. FIG. 6 shows a voltage applied to the lower wiring 1 of the semiconductor device using Ba0.7Sr0.3TiO3 having a thickness of 2000 Å which is obtained by firing at 500 ° C. for 1 hour in the structure of FIG. 6 is a graph showing the relationship between the current flowing through the semiconductor device from the lower layer wiring to the upper layer wiring 3.

GF Exhibit 1124 - 1475/2704

[0033]

As is clear from FIG. 6, even if −10 V is applied to the lower layer wiring, almost no current flows and good diode characteristics are shown. Further, when a voltage was applied to the lower layer wiring for a long time within the range of −10 V or less, the current flowing through the high dielectric material increased, resulting in dielectric breakdown. The semiconductor device shown in FIG. 7 is the same as the semiconductor device shown in FIG. 7 except that the platinum layer 6 having a thickness of 100 Å is formed between the titanium layer 5 and the gold layer 7 and the insulating film 8 is SiO 2 in the formation of the upper wiring 3. It was formed by repeating the same process as in 2.

[0034]

FIG. 8 shows the voltage applied to the lower layer wiring 1 of the semiconductor device in which Ba 0.5 Sr 0.5 TiO 3 having a thickness of 2000 Å, which was fired at 300 ° C. for 1 hour in the structure of FIG. 7, was used for the metal oxide film 2. , The relationship of the standardized current flowing through the semiconductor device from the lower layer wiring 1 to the upper layer wiring 3 is shown. In FIG. 8, the size of the upper layer wiring 3 is changed from 20 μm × 10 μm to 200 μm × 200 μm.

[0035]

As is clear from FIG. 8, the forward current depends on the area of the upper layer wiring 3. Further, even if a DC bias is applied to the lower layer electrode from -8 to -10V, almost no reverse current flows. When a DC bias of +2 to 3V is applied, a practical level forward current (about 1A / cm2) is obtained. Flowing. This indicates that the semiconductor device obtained by the present invention operates as a diode having a high reverse breakdown voltage. Further, when the DC bias applied to the lower layer electrode is fixed at -2 V, the current is suppressed to 10 -6 to 10 -4 A / cm 2 and good leak characteristics are exhibited.

[0036]

GF Exhibit 1124 - 1476/2704

Fourth Embodiment FIG. 9 shows an example of a circuit configuration when the semiconductor device of the present invention is used as a capacitor. In addition, A in FIG. 9 is a semiconductor device of the present invention including a lower layer wiring 1, a metal oxide film 2, and an upper layer wiring 3. The relative dielectric constant of 1 to 15 GHz when -5 V is applied to the lower layer wiring 1 is 30 in the case of Ba0.7 Sr0.3 TiO3, 25 in the case of Ba0.5 Sr0.5 TiO3, and 20 in the case of SrTiO3. there were. Although the relative permittivity (100 to 300) originally obtained by these high dielectric metal oxides has not been obtained, compared with the fact that SiN is 5.6 and SiO2 is 4, it is made of these metal oxides. It has been found that the capacitor exhibits a capacity of 4 to 7 times. Therefore, when SiN or SiO2 having the same thickness is used, the capacitor area can be reduced to 1/4 to 1/7.

[0037]

Fifth Embodiment FIG. 10 shows an example of a circuit configuration when the semiconductor device of the present invention is used as a diode and a capacitor on the same substrate. Even with the same device structure, it is possible to build capacitors and diodes at the same time, which simplifies the process.

[0038]

According to the semiconductor device of the present invention, a lower layer wiring of any shape made of a metal forming a Schottky contact with a metal oxide and a metal oxide film having an oxygen defect are sandwiched on a semiconductor substrate. In addition, since the vertical structure having an upper wiring of arbitrary shape made of a metal having an affinity with oxygen larger than that of the metal contained in the metal oxide film is formed, a high breakdown voltage element is formed on the semiconductor substrate. Therefore, the integrated circuit can be operated together with other active elements formed on the substrate, and high performance of the integrated circuit can be achieved.

[0039]

In addition, since the lower wiring has a platinum layer on the upper surface in contact with the metal oxide film and the upper wiring has a titanium layer on the lower surface in contact with the metal oxide film, the lower wiring and the metal oxide film are Can form a Schottky contact between the upper wiring and the ohmic contact between the upper wiring and the metal oxide film.

GF Exhibit 1124 - 1477/2704

Further, by changing the metal of the upper and lower wirings of the metal oxide film, it is possible to provide a semiconductor device capable of flowing a current having a practical current density of 1 to 10 A / cm @ 2 in the vertical direction.

[0040]

Further, since the lower layer wiring is made of a titanium / platinum laminated body and the upper layer wiring is made of a titanium / gold or titanium / platinum / gold laminated body, a semiconductor device having further excellent characteristics can be obtained. Further, since the metal oxide is barium strontium titanate (Bax Sr1-x TiO3; $0 \leqq x \leqq 0.7$), the relative dielectric constant is improved as compared with the conventional one using an insulator such as SiN. A semiconductor device can be obtained.

[0041]

Further, since silicon nitride or silicon oxide is sandwiched between the semiconductor substrate and the lower layer wiring, the process matching with other semiconductor devices on the semiconductor substrate becomes good. Further, since the semiconductor device is used as a diode, a high breakdown voltage diode can be obtained.

[0042]

Further, since the lower layer wiring applies a DC negative bias, which is relatively constant to the upper layer wiring, within a range where the insulation is not destroyed, and is used as a capacitor, the characteristics of the metal oxide film as an insulator are exhibited and the loss is small. A capacitor can be obtained. Further, since the constant DC negative bias is -0.5 V to -10 V, it is possible to obtain a capacitor with less loss.

[0043]

Furthermore, since the diode and the capacitor manufactured in the same process are included in the circuit as constituent elements, the capacitor and the diode can be formed in the same

GF Exhibit 1124 - 1478/2704

process. In addition, the metal oxide film is formed by applying a precursor solution composed of a metal alkoxide constituting the metal oxide film onto the lower layer wiring, and then performing firing in air in the range of 300 ° C to 500 ° C. Since it is formed by the sol-gel method utilizing hydrolysis, it is possible to maintain an oxygen deficiency state that provides a sufficient passing current (1 to 10 A / cm 2). Further, since the firing can be performed at a low temperature, the manufacturing process of other semiconductor devices formed on the semiconductor substrate is not significantly changed, and it is not necessary to select an electrode material that causes a decrease in reliability. .. Therefore, the problem of deterioration of reliability and the manufacturing cost do not increase.

[0044]
Brief description of the drawings

[0045]
1 is a schematic plan view and a sectional view of a semiconductor device of the present invention.

[0046]
2 is a schematic plan view and a sectional view of the manufacturing process of the semiconductor device of the present invention.

[0047]
3 is a schematic plan view and a sectional view of the manufacturing process of the semiconductor device of the present invention.

[0048]
4 is a schematic plan view and a sectional view of the manufacturing process of the semiconductor device of the present invention.

[0049]
5 is a schematic plan view and a sectional view of the semiconductor device of the present invention.

[0050]

GF Exhibit 1124 - 1479/2704

6 is a graph showing the relationship between the current and the voltage applied to the lower layer wiring of the semiconductor device of the present invention.

[0051]
7 is a schematic plan view and a sectional view of the semiconductor device of the present invention.

[0052]
8 is a graph showing the relationship between the current of the semiconductor device of the present invention and the voltage applied to the lower layer wiring.

[0053]
9 is a circuit configuration diagram when the semiconductor device of the present invention is used as a capacitor.

[0054]
10 is a circuit configuration diagram when the semiconductor device of the present invention is used as a diode and a capacitor on the same substrate.

[0055]
Explanation of symbols

[0056]
1 Lower Layer Wiring 2 Metal Oxide Film 3 Upper Layer Wiring 4 Semiconductor Substrate 5 Titanium Layer 6 Platinum Layer 7 Gold Layer 8 Insulating Film A Semiconductor Device

GF Exhibit 1124 - 1480/2704

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

CLAIMS JPH08167693

1.
A metal oxide film having an oxygen defect is sandwiched between a lower wiring of an arbitrary shape formed of a metal that forms a Schottky contact with a metal oxide on a semiconductor substrate, and the affinity with oxygen is high. A semiconductor device characterized by a vertical structure having an upper layer wiring of an arbitrary shape composed of a metal larger than the metal contained in.

2.
2. The semiconductor device according to claim 1, wherein the lower wiring has a platinum layer on the upper surface in contact with the metal oxide film, and the upper wiring has a titanium layer on the lower surface in contact with the metal oxide film.

3.
3. The semiconductor device according to claim 1, wherein the lower layer wiring is made of a titanium / platinum laminated body, and the upper layer wiring is made of a titanium / gold or titanium / platinum / gold laminated body.

4.
4. The semiconductor device according to claim 1, wherein the metal oxide film is barium strontium titanate (BaxSr1-x TiO3; 0 x 0.7).

GF Exhibit 1124 - 1481/2704

5.
The semiconductor device according to claim 1, wherein a silicon nitride film or a silicon oxide film is sandwiched between the semiconductor substrate and the lower layer wiring.

6.
The semiconductor device according to claim 1, wherein the semiconductor device is used as a diode.

7.
The semiconductor device according to claim 1, wherein the lower layer wiring is used as a capacitor by applying a constant DC negative bias relative to the upper layer wiring within a range that does not destroy the insulation.

8.
8. The semiconductor device according to claim 7, wherein the constant DC negative bias is −0.5V to −10V.

9.
An integrated circuit semiconductor device, comprising the semiconductor device according to claim 6 and claim 7 or 8 manufactured in the same step as a constituent element in a circuit.

10.
The metal oxide film according to any one of claims 1 to 9 is obtained by applying a precursor solution consisting of a metal alkoxide constituting the metal oxide film onto the lower layer wiring, and then firing in air in the range of 300 ° C to 500 ° C. The method for manufacturing a semiconductor device is characterized in that the semiconductor device is formed by a sol-gel method utilizing hydrolysis, which is performed in 1.

GF Exhibit 1124 - 1482/2704

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号

特開平9－289178

(43)公開日　平成９年(1997)11月４日

(51)Int.Cl.[6]		識別記号	庁内整理番号	ＦＩ			技術表示箇所
Ｈ０１Ｌ	21/28	３０１		Ｈ０１Ｌ	21/28	３０１Ｒ	
	21/265				21/265	Ｗ	
	21/3205				21/88	Ｎ	
	21/768				21/90	Ｃ	
	29/78				29/78	３０１Ｐ	

審査請求　未請求　請求項の数23　ＦＤ　（全 18 頁）　最終頁に続く

(21)出願番号　特願平9－47053

(22)出願日　平成９年(1997)２月14日

(31)優先権主張番号　特願平8－34512

(32)優先日　平８(1996)２月22日

(33)優先権主張国　日本（ＪＰ）

(71)出願人　000005821
松下電器産業株式会社
大阪府門真市大字門真1006番地

(72)発明者　関口　満
大阪府門真市大字門真1006番地　松下電器産業株式会社内

(72)発明者　山中　通成
大阪府門真市大字門真1006番地　松下電器産業株式会社内

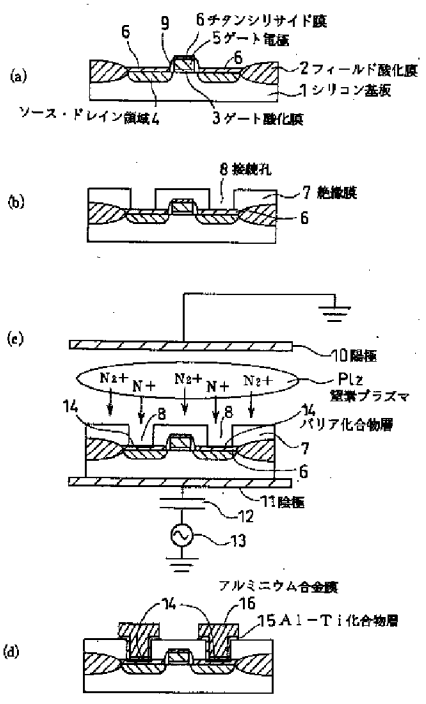
(74)代理人　弁理士　前田　弘　（外２名）

(54)【発明の名称】　半導体装置及びその製造方法

(57)【要約】

【課題】　半導体装置において、熱処理時に金属シリサイドとその上の金属層との間の反応に起因する接合リーク等の発生を防止する。

【解決手段】　接続孔８の開口後ないしは絶縁膜７の堆積前に、半導体装置をプラズマ発生装置の陰極１１に固定し、例えばチタンシリサイド膜６等の金属シリサイド膜の表面を５５０℃以下で窒素を含むガスのプラズマにさらす。この処理により、チタンシリサイド膜６等の金属シリサイド膜の表面付近の領域に窒素－酸素－金属－シリコン間化合物からなるバリア化合物層１４を形成する。その後、接続孔８に窒化チタン・窒化膜等のバリアメタルを堆積しなくても、Ａｌ－Ｔｉ化合物層１５，アルミニウム合金膜１６等の段差被覆性のよい材料で埋込層を形成しながら、後の熱処理時における金属シリサイドと埋込層との反応を阻止できる。したがって、コンタクト抵抗やシート抵抗及び接合リークを低減し、信頼性を向上させることができる。



GF Exhibit 1124 - 1483/2704

【特許請求の範囲】
【請求項１】　半導体基板と、
上記半導体基板の一部に形成され第１の金属がシリサイド化されてなる金属シリサイド膜と、
上記金属シリサイド膜の上に形成された第２の金属からなる金属膜と、
上記金属シリサイド膜の表面付近の領域に形成され、窒素－酸素－第１の金属－シリコン間化合物からなるバリア化合物層とを備えていることを特徴とする半導体装置。
【請求項２】　請求項１記載の半導体装置において、
上記金属シリサイド膜全体の表面付近の領域に上記バリア化合物層が形成されていることを特徴とする半導体装置。
【請求項３】　請求項１又は２記載の半導体装置において、
上記バリア化合物層の厚みは、上記第２の金属の上記バリア化合物層への拡散を阻止するのに十分な厚み以上で上記金属シリサイド膜の厚みの３０％以下であることを特徴とする半導体装置。
【請求項４】　請求項１又は２記載の半導体装置において、
上記バリア化合物層の厚みは、２～２０ｎｍの範囲であることを特徴とする半導体装置。
【請求項５】　請求項１，２又は３記載の半導体装置において、
上記バリア化合物層内における上記窒素の濃度が最大となる位置は、上記酸素の濃度が最大となる位置よりも奥方であることを特徴とする半導体装置。
【請求項６】　請求項１記載の半導体装置において、
上記金属シリサイド膜の上に形成された絶縁膜と、
上記絶縁膜の一部に形成され上記金属シリサイド膜に到達する接続孔とをさらに備え、
上記金属膜は、上記接続孔内に堆積された第２の金属からなる埋込層であることを特徴とする半導体装置。
【請求項７】　請求項１記載の半導体装置において、
上記金属シリサイド膜の上に形成された絶縁膜と、
上記絶縁膜の一部に形成され上記金属シリサイド膜に到達する接続孔と、
上記接続孔内に堆積された第３の金属からなる埋込層とをさらに備えていることを特徴とする半導体装置。
【請求項８】　請求項１，２，３，４，５，６又は７記載の半導体装置において、
上記第１の金属は、チタン，コバルト，ニッケル，タンタル，タングステン，ニオブ，パラジウム，白金及びモリブデンのうちいずれか１つであることを特徴とする半導体装置。
【請求項９】　請求項１，２，３，４，５，６又は７記載の半導体装置において、
上記第２の金属は、アルミニウムを含む金属，銅を含む金属及びタングステンを含む金属のうちいずれか１つであることを特徴とする半導体装置。
【請求項１０】　半導体基板上に、第１の金属とシリコンとの化合物からなる金属シリサイド膜を形成する第１の工程と、
中性ないし酸化雰囲気下で、上記金属シリサイド膜の表面に窒素を含むイオンを照射して、上記金属シリサイド膜の表面付近の領域に窒素－酸素－第１の金属－シリコン間化合物からなるバリア化合物層を形成する第２の工程と、
上記金属シリサイド膜の上記バリア化合物層の上に第２の金属を堆積して金属膜を形成する第３の工程とを備えていることを特徴とする半導体装置の製造方法。
【請求項１１】　請求項１０記載の半導体装置の製造方法において、
上記第１の工程の後かつ上記第２の工程の前に、上記金属シリサイド膜の上に絶縁膜を形成する工程と、上記絶縁膜の一部を選択的に除去して上記金属シリサイド膜に到達する接続孔を形成する工程とをさらに備え、
上記第２の工程では、上記金属シリサイド膜の表面付近の領域のうち上記接続孔の底部に露出した領域に上記バリア化合物層を形成し、
上記第３の工程では、上記接続孔内を上記第２の金属で埋め込むことを特徴とする半導体装置の製造方法。
【請求項１２】　請求項１０記載の半導体装置の製造方法において、
上記第２の工程の後に、上記金属シリサイド膜の上記バリア化合物層の上に絶縁膜を形成する工程と、上記絶縁膜の一部を選択的に除去して上記バリア化合物層に到達する接続孔を形成する工程とをさらに備え、
上記第３の工程では、上記接続孔内に上記第２の金属を堆積することを特徴とする半導体装置の製造方法。
【請求項１３】　請求項１２記載の半導体装置の製造方法において、
上記第３の工程の後に、
上記金属シリサイド膜の上記バリア化合物層の上に絶縁膜を形成する工程と、
上記絶縁膜の一部を選択的に除去して上記バリア化合物層に到達する接続孔を形成する工程と、
上記接続孔内に第３の金属を堆積して埋込層を形成する工程とをさらに備えていることを特徴とする半導体装置の製造方法。
【請求項１４】　請求項１０，１１，１２又は１３記載の半導体装置の製造方法において、
上記第２の工程では、チャンバ内に陰極である下部電極と陽極である上部電極とを配置したプラズマ発生装置を用い、上記チャンバ内において、上記半導体基板を上記下部電極上に載置した状態で上記金属シリサイド膜を窒素を含むガスのプラズマにさらすことにより上記バリア化合物層を形成することを特徴とする半導体装置の製造

GF Exhibit 1124 - 1484/2704

方法。
【請求項１５】　請求項１０，１１，１２又は１３記載の半導体装置の製造方法において、
上記第２の工程では、上記金属シリサイド膜の表面を窒素を含むガスにさらしながら紫外線及び電離放射線のうちいずれか一方を照射することにより、上記バリア化合物層を形成することを特徴とする半導体装置の製造方法。
【請求項１６】　請求項１０，１１，１２又は１３記載の半導体装置の製造方法において、
上記第２の工程では、上記金属シリサイド膜の表面を窒素を含むイオンビームにさらすことにより、上記バリア化合物層を形成することを特徴とする半導体装置の製造方法。
【請求項１７】　請求項１０，１１，１２，１３，１４，１５又は１６記載の半導体装置の製造方法において、
上記第２の工程を、５５０℃以下で行なうことを特徴とする半導体装置の製造方法。
【請求項１８】　請求項１０，１１，１２，１３，１４，１５又は１６記載の半導体装置の製造方法において、
上記第２の工程では、上記窒素を含むガスとしてN2 ガスを用いることを特徴とする半導体装置の製造方法。
【請求項１９】　請求項１０，１１，１２，１３，１４，１５，１６，１７又は１８記載の半導体装置の製造方法において、
上記第２の工程の前に、水素を含むガスを流すことにより、上記金属シリサイド膜上の自然酸化膜を除去する工程をさらに備え、
上記第２の工程では、酸素を含むガスを添加することを特徴とする半導体装置の製造方法。
【請求項２０】　請求項１０，１１，１２，１３，１４，１５又は１６記載の半導体装置の製造方法において、
上記第２の工程では、窒素を含むイオンを３ｋｅＶ以下のイオンエネルギーで上記金属シリサイド膜内に導入することを特徴とする半導体装置の製造方法。
【請求項２１】　請求項１０，１１，１２，１３，１４，１５，１６，１７，１８，１９又は２０記載の半導体装置の製造方法において、
上記第１の工程では、金属シリサイド膜として、チタン，コバルト，ニッケル，タンタル，タングステン，パラジウム，白金及びモリブデンのうちいずれか１つのシリサイド膜を形成することを特徴とする半導体装置の製造方法。
【請求項２２】　請求項１０，１１，１２，１３，１４，１５，１６，１７，１８，１９又は２０記載の半導体装置の製造方法において、
上記第３の工程では、ＣＶＤ法を用いてアルミニウムを含む金属，銅を含む金属及びタングステンを含む金属のうちいずれか１つを堆積することを特徴とする半導体装置の製造方法。
【請求項２３】　請求項１０，１１，１２，１３，１４，１５，１６，１７，１８，１９又は２０記載の半導体装置の製造方法において、
上記第３の工程では、チタン及びアルミニウム合金を連続的にスパッタすることにより、上記金属膜をＡｌ－Ｔｉ化合物層及びアルミニウム合金膜により構成することを特徴とする半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、シリサイド層を有する半導体装置及びその製造方法に係り、特にシリサイド層の上層配線や上部低抵抗金属膜との間におけるコンタクト部の構造の改良に関するものである。
【０００２】
【従来の技術】近年、超ＬＳＩの高集積化、高密度化にともない、超ＬＳＩに搭載されるＭＯＳ型トランジスタのゲート電極、ソース・ドレイン領域の表面に自己整合的に金属シリサイド層を形成し、ゲート電極、ソース・ドレイン領域のシート抵抗を小さくすると共にコンタクト抵抗や拡散抵抗等の寄生抵抗を低減し、半導体素子の動作速度を向上させる技術（サリサイド技術）が用いられている。
【０００３】ところで、上記金属シリサイド層の上にアルミニウム，タングステン，銅からなる埋込層を形成する方法として、例えば高温におけるアルミニウム合金の流動性を利用した高温スパッタ法、あるいは、被覆性に優れる化学気相堆積（以下ＣＶＤと記す）法により選択的に接続孔内にアルミニウムやタングステン、銅等の金属を堆積して、信頼性の高い埋込層を形成する方法が知られている。その場合、埋込層を構成するこれらの金属と金属シリサイド層とが接する部分において、両者間で反応が生じ問題となることがある。すなわち、高温スパッタや選択ＣＶＤあるいは上層の配線を形成するＣＶＤにおいて４５０～６００℃程度の熱履歴が生じるので、金属シリサイドと埋込層を構成する金属とが反応し、この反応生成物によってシリコン基板が浸食されて、接合リークを発生する虞れがある。そのため、両者間における反応を抑制すべく、埋込層と金属シリサイド層との間に窒化チタン等のバリアメタルを形成することが一般的に行なわれている。
【０００４】以下、図１５（ａ）～（ｄ）を参照しながら、高温スパッタ法を用いて金属シリサイド層上の埋込層を形成する従来の方法について説明する。
【０００５】まず、図１５（ａ）に示すように、シリコン基板１上のフィールド酸化膜２により取り囲まれる活性領域の上に、シリコン酸化膜からなるゲート酸化膜３と、ポリシリコン膜からなるゲート電極５と、シリコン

GF Exhibit 1124 - 1485/2704

酸化膜からなるサイドウォール９と、シリコン基板１内に不純物を導入してなるソース・ドレイン領域４とを備えたＭＯＳトランジスタを形成する。そして、ＭＯＳトランジスタのソース・ドレイン領域４とゲート電極５との上に、スパッタ法により例えばチタン膜を堆積し、６００～９００℃で熱処理した後、H2 SO4 －H2 O2 混合液で未反応チタン膜を除去することにより、ソース・ドレイン領域４とゲート電極５との上にのみチタンシリサイド膜６を選択的に形成する。

【０００６】次に，図１５（ｂ）に示すように、基板の全面上に絶縁膜７を形成し、絶縁膜７にソース・ドレイン領域４のチタンシリサイド膜６に到達する接続孔８を開口する。

【０００７】次に、図１５（ｃ）に示すように、接続孔８内及び絶縁膜７の上にソース・ドレイン領域４上のチタンシリサイド膜６との接触特性を良好にするためのチタン膜、バリアメタルとしての窒化チタン膜をスパッタ法により堆積し、窒化チタン・チタン膜１９を形成する。

【０００８】次に、図１５（ｄ）に示すように、チタンをスパッタした後その上にアルミニウム合金を５００℃でスパッタすることにより、アルミニウム合金とチタンとが化合してなるＡｌ－Ｔｉ化合物層１５と、その上のアルミニウム合金膜１６とを形成する。その際、Ａｌ－Ｔｉ間の反応熱を利用することにより、接続孔８内をアルミニウム合金で埋め込む。そして、フォトリソグラフィ法により、窒化チタン・チタン膜１９、Ａｌ－Ｔｉ化合物層１５、アルミニウム合金１６をパターニングして、金属配線を形成する。

【０００９】

【発明が解決しようとする課題】しかしながら、半導体装置の微細化に応じて接続孔の径が微細化が進行すると、上記従来の方法において、図１５（ｃ）に示す工程で、窒化チタン・チタン膜１９をスパッタ法により堆積することは、以下の理由により好ましくない。

【００１０】　一般的に、スパッタ法で成膜した窒化チタン膜は段差被覆性がよくないので、接続孔上部の角でオーバーハング形状が形成されやすい。そのため、高温スパッタ時の接続孔内へのアルミニウム合金の流動を妨げ、接続孔が埋め込みにくくなる（例えばY.Takegawa他 Ext. Abst. SSDM,p.558, 1993）。

【００１１】　そこで、窒化チタン膜を形成する際に、N2 ガスを流しながらハニカム状のフィルタ（コリメータ）を通してチタンをスパッタすることによりオーバーハング形状の形成を抑制する方法もあるが、コリメータを使用するとパーティクルを発生しやすい。

【００１２】　また、図１５（ｂ）に示す工程で、接続孔８以外の部分（絶縁膜７上の部分　）も窒化チタン・チタン膜１９で覆われてしまうため、下地の違いを利用した選択ＣＶＤ法により接続孔８内にのみ選択的にアルミニウムやタングステン、銅等の金属を堆積するという方法を用いることができない。

【００１３】一方、上述のような問題を回避するために、絶縁膜に接続孔を形成した後、窒化チタン・チタン膜１９を堆積せずに、８５０℃程度のＮH3 雰囲気中で熱処理を行うことにより、チタンシリサイド膜の表面に窒化チタン膜を形成した後、選択ＣＶＤ法により接続孔内にのみ、選択的にアルミニウムを堆積する技術が提案されている（例えばH.Shinriki他 Ext. Abst. SSDM,p.968, 1994）。

【００１４】しかし、８００℃以上の熱処理をチタンシリサイド膜に加えると、ソース・ドレイン領域中のボロンがチタンシリサイド膜中に吸い上げられ、Ｐチャネルトランジスタの飽和電流値が低下するという虞れがある。また、金属シリサイドの種類によっては、高温で熱処理を行なうとシリサイドの凝集がおこり、ソース・ドレインのシート抵抗が増大する。そのため、上記従来の方法を適用し得るシリサイドの種類が限定される。

【００１５】また、以上のような不具合は、接続孔内の埋込層とシリサイド膜との間だけでなく、シリサイド膜の上に低抵抗の金属膜を形成しようとするときにも同じように生じるので、シリサイド膜と金属膜との積層構造における信頼性を悪化させる原因となっている。

【００１６】本発明は、金属シリサイド層とその上の金属膜との境界付近に窒素－酸素－金属－シリコン間化合物からなる化合物層が形成されると、半導体基板中に接合リークの原因となるような化合物の侵入が生じないという事実の発見に基づきなされたものであり、その目的は、このようなバリアとなる化合物層を形成することにより、バリアメタルを不要として埋込層やシリサイド膜と金属膜の積層構造における信頼性の向上を図りつつ、金属シリサイド膜全体のシート抵抗値を低く保ち、かつ接合リークの発生を防止し得る半導体装置およびその製造方法を提供することにある。

【００１７】

【課題を解決するための手段】上記目的を達成するために、本発明では、請求項１～９に記載されている半導体装置に関する手段と、請求項１２～２３に記載されている半導体装置の製造方法に関する手段とを講じている。

【００１８】本発明の半導体装置は、請求項１に記載されているように、半導体基板と、上記半導体基板の一部に形成され第１の金属がシリサイド化されてなる金属シリサイド膜と、上記金属シリサイド膜の上に形成された第２の金属からなる金属膜と、上記金属シリサイド膜の表面付近の領域に形成され、窒素－酸素－第１の金属－シリコン間化合物からなるバリア化合物層とを備えている。

【００１９】これにより、金属シリサイド膜の表面に窒素－酸素－金属－シリコン間化合物からなるバリア化合物層が形成されているので、金属膜を堆積する際などの

GF Exhibit 1124 - 1486/2704

製造工程中における高温履歴があっても、金属シリサイド膜を構成する第１の金属と金属膜を構成する第２の金属との反応が抑制されている。すなわち、窒化チタン・窒化膜等のバリアメタルを介在させなくても、接合リークの発生やゲート酸化膜の特性の劣化が抑制される。したがって、バリアメタルの段差被覆性や抵抗特性がよくないことに起因する不具合、例えば信頼性の低下やシート抵抗の増大を回避できる。

【００２０】請求項２に記載されているように、請求項１において、上記金属シリサイド膜全体の表面付近の領域に上記バリア化合物層が形成されていることが好ましい。

【００２１】これにより、半導体装置の製造工程が簡略化され、かつ金属シリサイド層の耐薬品性が向上するので、その結果製造コストも低減できることになる。

【００２２】請求項３，４に記載されているように、請求項１又は２において、上記バリア化合物層の厚みは、上記第２の金属の上記バリア化合物層への拡散を阻止するのに十分な厚み以上で上記金属シリサイド膜の厚みの３０％以下であることが好ましく、或いは別の観点からすると、２～２０ｎｍの範囲であることが好ましい。

【００２３】これにより、あまりに厚いバリア化合物層が形成されることによるコンタクト抵抗やシート抵抗の増大が可及的に抑制されることになる。

【００２４】請求項５に記載されているように、請求項１，２又は３において、上記バリア化合物層内における上記窒素の濃度が最大となる位置を上記酸素の濃度が最大となる位置よりも奥方に位置させることが好ましい。

【００２５】これにより、窒素濃度が高くなる位置では相対的に酸素濃度が低くなっていくので、特にコンタクト抵抗やシート抵抗の増大を招く酸化物層の濃度の高い領域をごく表面近傍に抑制することができる。したがって、金属膜とシリサイド膜との接触部におけるシート抵抗等の増大が可及的に抑制されることになる。

【００２６】請求項６に記載されているように、請求項１において、上記金属シリサイド膜の上に形成された絶縁膜と、上記絶縁膜の一部に形成され上記金属シリサイド膜に到達する接続孔とをさらに備え、上記金属膜を上記接続孔内に堆積された第２の金属からなる埋込層とすることができる。

【００２７】これにより、金属膜の表面付近の領域に第１の金属と第２の金属との反応を抑制するバリア化合物が存在しているので、接続孔にバリアメタルを形成する必要がなくなる。したがって、特に段差被覆性が要求される接続孔内の埋込層を構成する第２の金属としてカバレージの良好なものを選択することができ、半導体装置の信頼性が向上する。

【００２８】請求項７に記載されているように、請求項１において、上記金属シリサイド膜の上に形成された絶縁膜と、上記絶縁膜の一部に形成され上記金属シリサイド膜に到達する接続孔と、上記接続孔内に堆積された第３の金属からなる埋込層とをさらに備えることができる。

【００２９】これにより、第２の金属で構成される金属膜として電気抵抗の小さい材料を選択して埋込層と金属シリサイド膜との間に低抵抗層を介在させることができるので、コンタクト抵抗の小さい微細化に適した半導体装置が得られることになる。

【００３０】請求項８に記載されているように、請求項１，２，３，４，５，６又は７において、上記第１の金属を、チタン，コバルト，ニッケル，タンタル，タングステン，ニオブ，パラジウム，白金及びモリブデンのうち少なくともいずれか１つで構成することが好ましい。

【００３１】請求項９に記載されているように、請求項１，２，３，４，５，６又は７において、上記第２の金属を、アルミニウムを含む金属，銅を含む金属及びタングステンを含む金属のうち少なくともいずれか１つで構成することが好ましい。

【００３２】本発明の半導体装置の製造方法は、請求項１０に記載されているように、半導体基板上に、第１の金属とシリコンとの化合物からなる金属シリサイド膜を形成する第１の工程と、中性ないし酸化雰囲気下で、上記金属シリサイド膜の表面に窒素を含むイオンを照射して、上記金属シリサイド膜の表面付近の領域に窒素－酸素－第１の金属－シリコン間化合物からなるバリア化合物層を形成する第２の工程と、上記金属シリサイド膜の上記バリア化合物層の上に第２の金属を堆積して金属膜を形成する第３の工程とを備えている。

【００３３】この方法により、第２の工程において金属シリサイド膜の表面にバリア化合物層が形成されるので、第３の工程において、バリアメタルを形成することなく金属膜を形成することが可能となる。したがって、第２の金属として段差被覆性のよい材料を適宜選択して用いることにより、金属膜の下地に対する段差被覆性が向上し、信頼性の高い半導体装置を形成することができる。

【００３４】請求項１１に記載されているように、請求項１０において、上記第１の工程の後かつ上記第２の工程の前に、上記金属シリサイド膜の上に絶縁膜を形成する工程と、上記絶縁膜の一部を選択的に除去して上記金属シリサイド膜に到達する接続孔を形成する工程とをさらに備え、上記第２の工程では、上記金属シリサイド膜の表面付近の領域のうち上記接続孔の底部に露出した領域に上記バリア化合物層を形成し、上記第３の工程では、上記接続孔内を上記第２の金属で埋め込むことができる。

【００３５】この方法により、バリア化合物層の形成領域が特に必要な領域に限定されるので、金属シリサイド膜のシート抵抗の増大が抑制される。

【００３６】請求項１２に記載されているように、請求

GF Exhibit 1124 - 1487/2704

項１０において、上記第２の工程の後に、上記金属シリサイド膜の上記バリア化合物層の上に絶縁膜を形成する工程と、上記絶縁膜の一部を選択的に除去して上記バリア化合物層に到達する接続孔を形成する工程とをさらに備え、上記第３の工程では、上記接続孔内に上記第２の金属を堆積することができる。

【００３７】この方法により、金属シリサイド膜の任意の場所に各配線層からコンタクトを形成する際に、どの部位においてもバリア化合物層が形成されていることから、接続孔を形成するごとにバリア化合物層を形成する必要がないので、工程が簡略化される。また、金属シリサイド膜のＨＦ等の薬品に対する耐性も向上するので、後の工程上の制限が緩和されることになる。

【００３８】請求項１３に記載されているように、請求項１２において、上記第３の工程の後に、上記金属シリサイド膜の上記バリア化合物層の上に絶縁膜を形成する工程と、上記絶縁膜の一部を選択的に除去して上記バリア化合物層に到達する接続孔を形成する工程と、上記接続孔内に第３の金属を堆積して埋込層を形成する工程とをさらに備えることができる。

【００３９】この方法により、第２の金属として電気抵抗の小さい材料を選択すれば、金属シリサイド膜の上に低抵抗層が形成され、その上に埋込層が形成されるので、コンタクト抵抗の小さい特性の良好な半導体装置が得られることになる。

【００４０】請求項１４に記載されているように、請求項１０，１１，１２又は１３において、上記第２の工程では、チャンバ内に陰極である下部電極と陽極である上部電極とを配置したプラズマ発生装置を用い、上記チャンバ内において、上記半導体基板を上記下部電極上に載置した状態で上記金属シリサイド膜を窒素を含むガスのプラズマにさらすことにより上記バリア化合物層を形成することができる。

【００４１】この方法により、陰極上に半導体基板を設置することで窒素プラズマ中でプラスイオンとなっている窒素が効率的に金属シリサイド中に取り込まれる。

【００４２】請求項１５に記載されているように、請求項１０，１１，１２又は１３において、上記第２の工程では、上記金属シリサイド膜の表面を窒素を含むガスにさらしながら紫外線及び電離放射線のうちいずれか一方を照射することにより、上記バリア化合物層を形成することができる。

【００４３】請求項１６に記載されているように、請求項１０，１１，１２又は１３において、上記第２の工程では、上記金属シリサイド膜の表面を窒素を含むイオンビームにさらすことにより、上記バリア化合物層を形成することができる。

【００４４】請求項１７に記載されているように、請求項１０，１１，１２，１３，１４，１５又は１６において、上記第２の工程を５５０℃以下で行なうことが好ましい。

【００４５】この方法により、５５０℃以下の低温条件でプラズマ処理等が行なわれるので、チタンシリサイドなどを用いた場合でも金属シリサイドの凝集を招くことがなく、金属シリサイドの種類の選択幅が拡大される。

【００４６】請求項１８に記載されているように、請求項１０，１１，１２，１３，１４，１５又は１６において、上記第２の工程では、上記窒素を含むガスとしてＮ２ガスを用いることができる。

【００４７】この方法により、バリア化合物層を形成する際に、金属シリサイド膜の表面に存在する自然酸化膜を利用して、窒素－酸素－金属－シリコン間化合物からなるバリア化合物層が容易に形成される。

【００４８】請求項１９に記載されているように、請求項１０，１１，１２，１３，１４，１５，１６，１７又は１８において、上記第２の工程の前に、水素を含むガスを流すことにより、上記金属シリサイド膜上の自然酸化膜を除去する工程をさらに備え、上記第２の工程では、酸素を含むガスを添加することができる。

【００４９】この方法により、バリア化合物層内における酸素濃度が制御されるので、各元素の分布状態をより好ましい状態に調整することが可能となる。

【００５０】請求項２０に記載されているように、請求項１０，１１，１２，１３，１４，１５又は１６において、上記第２の工程では、窒素を含むイオンを３ｋｅＶ以下のイオンエネルギーで上記金属シリサイド膜内に導入することが好ましい。

【００５１】この方法により、バリア化合物層が形成される領域が金属シリサイド膜の表面から２０ｎｍ程度の深さまでに限定されるので、形成される半導体装置のコンタクト抵抗やシート抵抗の増大が抑制されることになる。

【００５２】請求項２１に記載されているように、請求項１０，１１，１２，１３，１４，１５，１６，１７，１８，１９又は２０において、上記第１の工程では、金属シリサイド膜として、チタン，コバルト，ニッケル，タンタル，タングステン，パラジウム，白金及びモリブデンのうちいずれか１つのシリサイド膜を形成することが好ましい。

【００５３】請求項２２に記載されているように、請求項１０，１１，１２，１３，１４，１５，１６，１７，１８，１９又は２０において、上記第３の工程では、ＣＶＤ法を用いてアルミニウムを含む金属，銅を含む金属及びタングステンを含む金属のうちいずれか１つを堆積することが好ましい。

【００５４】請求項２３に記載されているように、請求項１０，１１，１２，１３，１４，１５，１６，１７，１８，１９又は２０において、上記第３の工程では、チタン及びアルミニウム合金を連続的にスパッタすることにより、上記金属膜をＡｌ－Ｔｉ化合物層及びアルミニ

GF Exhibit 1124 - 1488/2704

ウム合金膜により構成することができる。
【００５５】これらの方法により、半導体装置の種類や金属シリサイド膜の上に形成される配線層の相違に応じた金属膜及び配線の形成方法の選択が可能となる。
【００５６】
【発明の実施の形態】
（第１の実施形態）図１（ａ）～（ｄ）は、第１の実施形態に係る半導体装置の製造工程を示す断面図である。
【００５７】まず、図１（ａ）に示すように、シリコン基板１上のフィールド酸化膜２により取り囲まれる活性領域の上に、シリコン酸化膜からなるゲート酸化膜３と、ポリシリコン膜からなるゲート電極５と、シリコン酸化膜からなるサイドウォール９と、シリコン基板１内に不純物を導入してなるソース・ドレイン領域４とを備えたＭＯＳトランジスタを形成する。そして、スパッタ法により、基板上に例えばチタン膜を堆積し、６５０℃で熱処理した後、H2 SO4 －H2 O2 混合液で未反応チタン膜を除去することにより、ソース・ドレイン領域４とゲート電極５との上にのみ、厚みが７０ｎｍ程度のチタンシリサイド膜６を選択的に形成する。その後、８５０℃で熱処理を行いチタンシリサイド膜を低抵抗化する。
【００５８】次に，図１（ｂ）に示すように、上記基板の全面上に厚みが８００ｎｍ程度の絶縁膜７を形成し、絶縁膜７にソース・ドレイン領域４のチタンシリサイド膜６に到達する接続孔８を開口する。
【００５９】次に、図１（ｃ）に示すように、平行平板電極を構成する陽極１０及び陰極１１と、ブロッキングコンデンサー１２と、高周波電源１３とを有するプラズマ発生装置を用い、プラズマ発生装置の反応室（図示せず）内に配置される陰極１１上に、図１（ｂ）までの工程を経た半導体装置を載置し、チタンシリサイド膜６の表面を窒素含有ガスのプラズマにさらす。例えば、温度５０℃にて、圧力８０ｍTorr の下で、１００％のN2 ガスを導入し、平行平板型電極１０，１１間に電力３００W程度の高周波電力を３００sec の間印加する。このとき、反応室内に窒素プラズマPlzが発生する。この窒素プラズマPlz中の窒素はN+ ，N2+等の陽イオンになっており、陰極１１方向にプラズマ電位約６０Vと自己バイアス電圧約２４０Vとを加算した合計３００Vの電位が発生する。そして、窒素イオンがこの電位で半導体装置の表面に引かれる。つまり、平行平板型電極１０，１１のうち陰極１１の上に半導体装置を設置することで、チタンシリサイド膜６表面への窒素の導入が促進されることとなる。この時、チタンシリサイド膜６の表面に形成されている自然酸化層中の酸素もチタンシリサイド層６内に取り込まれ、窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層１４がチタンシリサイド膜６の表面付近に形成される。
【００６０】次に、図１（ｄ）に示すように、チタンを７５ｎｍ程度の厚み分だけスパッタした後、シリコン１％と銅０．５％を含むアルミニウム合金を５００℃で９００ｎｍ程度の厚み分だけスパッタすることにより、アルミニウム合金とチタンとが化合してなるＡｌ－Ｔｉ化合物層１５と、その上のアルミニウム合金膜１６とを形成する。その際、Ａｌ－Ｔｉ間の反応熱を利用することにより、接続孔８内をアルミニウム合金で埋め込んで埋込層を形成する。そして、フォトリソグラフィ法により、Ａｌ－Ｔｉ化合物層１５、アルミニウム合金膜１６をパターニングして、金属配線を形成する。
【００６１】なお、ゲート電極５上にも同時に接続孔を形成し（図１（ａ）～（ｄ）に示す断面とは別の断面で）、ゲート電極５上のチタンシリサイド膜６の表面付近にバリア化合物層１４を形成した後、Ａｌ－Ｔｉ化合物層１５、アルミニウム合金膜１６を堆積して埋込層及び金属配線を形成するようにしてもよい。
【００６２】図2は、上述の製造方法によって形成された半導体装置の断面構造を示すものである。すなわち、シリコン基板１上に、ゲート酸化膜３と、ポリシリコン膜からなるゲート電極５と、ソース・ドレイン領域４と、ソース・ドレイン領域４及びゲート電極５上に形成されたチタンシリサイド膜６と、サイドウォール９とを備えたＭＯＳトランジスタが形成されている。そして、基板上に形成された絶縁膜７にはソース・ドレイン領域４上のチタンシリサイド膜６に到達する接続孔８が形成されており、この接続孔８内及び絶縁膜７の上に埋込層及び金属配線を構成するＡｌ－Ｔｉ化合物層１５とアルミニウム合金膜１６とが形成されている。そして、本実施形態に係る半導体装置の特徴として、アルミニウム合金膜１６の下に窒化チタン・窒化膜等のバリアメタルは形成されておらず、代わりに、ソース・ドレイン領域４上のチタンシリサイド膜６のうち接続孔８の底面となる領域の表面のみに、窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層１４が形成されている。
【００６３】次に、本実施形態で得られる半導体装置のバリア化合物層１４の構造の詳細と本実施形態の半導体装置におけるコンタクト抵抗等等の詳細とについて説明する。
【００６４】図9は、本実施形態における図１（ｃ）に示す工程を経た後のチタンシリサイド膜６の表面付近の領域をオージェ電子分光法によって分析した結果得られた各元素の濃度プロファイルを示す図である。ただし、オージェ電子分光法による分析の際各元素に対する感度が異なっているので、図９は各元素の組成比を正確に示すものではなく、各元素個々の濃度分布を示しているに過ぎない。図９に示されるように、表面から２～３ｎｍまではシリコンと酸素が特に多く存在しており、これは分析する過程でチタンシリサイド膜の表面に自然酸化膜としてＳｉO2膜が形成されたことによるものと考えられる。そして，ＳｉO2 膜の下方に８ｎｍ程度の範囲で

GF Exhibit 1124 - 1489/2704

窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層が形成されている。そして、表面付近のＳｉＯ２膜を除外してみると、表面のごく近傍に酸素濃度のピークが見られ、さらにＳｉO2 膜の下方４～５ｎｍ程度の深さ位置に窒素濃度のピークが見られる。

【００６５】このバリア化合物層１４内における各元素間の結合状態については、反応層が薄いため分析することはできなかったが、ＴｉＮ，ＴｉO２，Ｓi３Ｎ４，ＳｉO2 の標準生成熱は、順に、－７３．０ｋｃａｌ／ｍｏｌ、－２１８．０ｋｃａｌ／ｍｏｌ、－１７９．３、－２０２．５ｋｃａｌ／ｍｏｌであるところから、本実施形態のようにチタンシリサイド膜を用いた場合は、酸素はチタン、シリコンと結合しており、窒素は主としてシリコンと結合していると考えられる。

【００６６】このバリア化合物層１４を形成した結果、シート抵抗は２．６Ω／□から２．９Ω／□に増加したが、増加の割合は１０％程度であり、トランジスタ動作等には特に問題のない十分低い値である。本実施形態では、接続孔８内のチタンシリサイド膜表面のみに、窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層１４が形成されているだけなので、チタンシリサイド６の上記窒素プラズマ処理によるシート抵抗の上昇率はさらに小さくなる。

【００６７】図１０は、図１（ｃ）に示す窒素プラズマ処理を行なわない試料、本実施形態の処理を行なった試料、及び図１５に示す従来の方法で製造されたリファレンスの試料（ＴｉＮ・Ｔｉ膜からなるバリアメタルを有し高温スパッタを行なっていない試料）についての接合リーク特性を比較する図である。ただし、面積が８０００μm2 のN+ Ｐ接合部に５．５Ｖの逆方向電圧を印加したときの接合リーク特性を示す。同図に示されるように、窒素プラズマ処理を行わなかった試料では接合リークが大きい。これは、図１（ｄ）に示す工程で、５００℃でアルミニウム合金をスパッタする際に、アルミニウム合金膜１６ないしはＡｌ－Ｔｉ化合物層１５がチタンシリサイド膜６と反応して，シリコン基板１中にアルミニウムが侵入し、接合リークが発生しているものと考えられる。これに対し、本実施形態による窒素プラズマ処理を行った試料の接合リークは、バリアメタルを有しないにも拘らず、バリアメタルを有し高温スパッタを行わなかったリファレンスの試料の接合リークと同等であることがわかる。これは、アルミニウム合金を５００℃でスパッタする際に、アルミニウム合金膜１６ないしはＡｌ－Ｔｉ化合物層１５がチタンシリサイド膜６と反応するのをバリア化合物層１４が阻止しているためと考えられる。

【００６８】また、本実施形態におけるN+ 拡散領域に対するコンタクト抵抗は、１．０μｍ角のコンタクト形状を有し窒素プラズマ処理を行なった試料で１５Ωであり、リファレンスの試料のコンタクト抵抗は５Ωである。本実施形態に係る試料のコンタクト抵抗はやや高いが、トランジスタの動作等には特に不具合は生ぜず、シリコン基板との電気的接続も十分とれていることがわかる。

【００６９】図１１は、窒素プラズマ処理を行なった後Ａｌ合金を堆積してアニール処理を行なった各種試料のシート抵抗のアニール温度依存性を示す図である。処理条件は、厚みが７０ｎｍのチタンシリサイド膜上に、図１（ｃ）に示す窒素プラズマ処理を行ない、さらにＡｌ－１％Ｓｉ－０．５％Ｃｕ合金を２００ｎｍの厚み分だけ堆積した後、３０分間アニールしている。試料には、窒素プラズマ処理を行なわなかったものと、２０sec の間窒素プラズマ処理を行なったものと、６０sec の間窒素プラズマ処理を行なったものと、３００sec の間窒素プラズマ処理を行なったものとがある。同図に示されるように、窒素プラズマ処理を６０sec 間行ったものと窒素プラズマ処理を３００sec 間行ったものでは、５３０℃でアニールした時のシート抵抗の上昇が抑制されていることがわかる。この図からも、チタンシリサイド膜表面に形成した窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層が、アルミニウム合金とチタンシリサイド膜との反応を抑制する効果があることがわかる。

【００７０】以上のように、本実施形態によれば、金属シリサイドの表面に窒素プラズマ処理を行なって、金属シリサイド膜の表面に窒素－酸素－金属－シリコン間化合物からなるバリア化合物層を形成するようにしたので、その後の工程の熱処理により金属シリサイド膜とアルミニウム合金との反応により生じた金属のシリコン基板中への侵入を有効に阻止できる。つまり、従来の方法のごとくアルミニウム合金膜等からなる埋込層と金属シリサイドとの間に窒化チタン・窒化膜等のバリアメタルを介在させることなく、接合リークの発生を抑制できる。したがって、バリアメタルを設けた場合のような埋込層の信頼性の悪化を回避できる。しかも、コンタクト抵抗は実用的に十分低く抑制することができ、金属シリサイド膜自体のシート抵抗も十分低く保つことができる。

【００７１】また、ゲート電極５上の金属シリサイド膜の表面付近に領域にバリア化合物層を形成した場合にも、ゲート電極中に金属が侵入するのを阻止できるので、ゲート酸化膜の特性の劣化等を有効に阻止することができる。

【００７２】特に、本実施形態では、５５０℃以下の低い温度で窒素プラズマ処理を行なっているので、多種類の金属シリサイドについて金属シリサイド膜の凝集を生じることがない、つまり、金属シリサイドを構成する金属材料の選択の幅の拡大を図ることができる利点がある。

【００７３】（第２の実施形態）次に、第２の実施形態

GF Exhibit 1124 - 1490/2704

について説明する。本実施形態では、製造工程の図示は省略するが、上述の第１の実施形態における図１（ａ）～（ｃ）と同じ処理を行なった後、選択的ＣＶＤ法により、接続孔８内に埋込層となるタングステン膜１７を堆積する。そして、タングステン膜１７及び絶縁膜７の上にアルミニウム合金膜１６を堆積した後、これをパターニングして金属配線を形成する。

【００７４】図３は、本実施形態により形成された半導体装置の構造を示す断面図である。上記第１の実施形態では、Ａｌ－Ｔｉ化合物層１５とアルミニウム合金膜１６とによって埋込層及び金属配線が一体的に構成されていたが、本実施形態では、タングステン膜１７により埋込層が構成され、アルミニウム合金膜１６により金属配線が構成されている。そして、ソース・ドレイン領域４上のチタンシリサイド膜６のうち接続孔８の底面の部分のみに窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層１４が形成されていて、タングステン膜１７とチタンシリサイド膜６とがこのバリア化合物層１４を介して接触している。つまり、本実施形態の半導体装置は、埋込層と金属配線とが異なる材料で構成されている点のみが第１の実施形態の半導体装置と異なり、他の部分は第１の実施形態の半導体装置と同じ構造を有する。したがって、上記第１の実施形態と基本的には同様の効果を発揮することができる。

【００７５】加えて、本実施形態の半導体装置においては、埋込層がタングステン膜１７で構成されているので、半導体装置の接合リークをもたらす反応の生じる温度がアルミニウム合金膜等の場合よりも高くなる。本実施形態では、バリア化合物層１４により、その後の６００℃以上の熱処理でチタンシリサイドとタングステンとが反応してシリコン基板中に金属が侵入し、接合リークが発生するのを防止することができる。

【００７６】（第３の実施形態）次に、第３の実施形態について説明する。図４（ａ）～（ｄ）は、本実施形態の半導体装置の製造工程を示す断面図である。

【００７７】まず、図４（ａ）に示すように、シリコン基板１上のフィールド酸化膜２により取り囲まれる活性領域の上に、シリコン酸化膜からなるゲート酸化膜３と、ポリシリコン膜からなるゲート電極５と、シリコン酸化膜からなるサイドウォール９と、シリコン基板１内に不純物を導入してなるソース・ドレイン領域４とを備えたＭＯＳトランジスタを形成する。そして、スパッタ法により、基板上に例えばチタン膜を堆積し、６５０℃で熱処理した後、H2 SO4 －H2 O2 混合液で未反応チタン膜を除去することにより、ソース・ドレイン領域４とゲート電極５との上にのみ、厚みが７０ｎｍ程度のチタンシリサイド膜６を選択的に形成する。その後、８５０℃で熱処理を行いチタンシリサイド膜を低抵抗化する。

【００７８】次に、図４（ｂ）に示すように、平行平板電極を構成する陽極１０及び陰極１１と、直流電源１８とを有するプラズマ発生装置を用い、プラズマ発生装置の反応室（図示せず）内に配置される陰極１１上に半導体装置を載置し、チタンシリサイド膜６の表面を窒素ガス等の窒素含有ガスのプラズマにさらす。すると、上記第１の実施形態と同様に、チタンシリサイド膜６の表面に形成されている自然酸化膜中の酸素もチタンシリサイド膜６内に取り込まれ、N2 ガスのプラズマによってチタンシリサイド膜６全体の表面付近に窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層１４が形成される。

【００７９】次に，図４（ｃ）に示すように、上記基板の全面上に厚みが８００ｎｍ程度の絶縁膜７を形成し、絶縁膜７にソース・ドレイン領域４のチタンシリサイド膜６に到達する接続孔８を開口する。

【００８０】次に、図４（ｄ）に示すように、スパッタ装置にて、チタンを７５ｎｍ程度の厚み分だけスパッタした後、シリコン１％と銅０．５％を含むアルミニウム合金を５００℃で９００ｎｍ程度の厚み分だけスパッタすることにより、アルミニウム合金とチタンとが化合してなるＡｌ－Ｔｉ化合物層１５と、その上のアルミニウム合金膜１６とを形成する。その際、Ａｌ－Ｔｉ間の反応熱を利用することにより、接続孔８内をアルミニウム合金で埋め込んで埋込層を形成する。そして、フォトリソグラフィ法により、Ａｌ－Ｔｉ化合物層１５、アルミニウム合金膜１６をパターニングして、金属配線を形成する。

【００８１】図５は、上述の製造方法によって形成された半導体装置の断面構造を示すものである。すなわち、シリコン基板１上に、ゲート酸化膜３と、ポリシリコン膜からなるゲート電極５と、ソース・ドレイン領域４と、ソース・ドレイン領域４とゲート電極５との上に形成されたチタンシリサイド膜６と、サイドウォール９とを備えたＭＯＳトランジスタが形成されている。そして、チタンシリサイド膜６の全面上に窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層１４が形成されている。そして、基板上に形成された絶縁膜７にはソース・ドレイン領域４上のチタンシリサイド膜６に到達する接続孔８が形成されており、この接続孔８内及び絶縁膜７の上に埋込層及び金属配線を構成するＡｌ－Ｔｉ化合物層１５とアルミニウム合金膜１６とが形成されている。つまり、上記第１の実施形態の半導体装置においては、ソース・ドレイン領域４上のチタンシリサイド膜６のうち接続孔８の底面となる領域の表面のみに、窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層１４が形成されていたが、本実施形態の半導体装置においては、ソース・ドレイン領域４及びゲート電極５の上のチタンシリサイド膜６の全面上にバリア化合物層１４が形成されている点に特徴がある。

【００８２】本実施形態においても、チタンシリサイド

GF Exhibit 1124 - 1491/2704

膜６の表面付近の領域に窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層１４が形成されているので、上記第１の実施形態と同様の効果が得られる。特に、本実施形態の方法では、ソース・ドレイン領域４だけでなくゲート電極５上のチタンシリサイド膜６の表面付近の領域にもバリア化合物層１４が形成されているので、図４（ｄ）に示すＡｌ－Ｔｉ化合物層１５及びアルミニウム合金膜１６とは別の配線層からゲート電極５にコンタクト部を形成する際にも、再度窒素プラズマ処理を行なわなくても、バリア化合物層１４を介してコンタクトすることができる利点がある。

【００８３】また、図４（ｄ）に示す工程の前つまり半導体装置をスパッタ装置内に入れる前に、接続孔８内をＨＦ溶液でウエットエッチングし、金属シリサイドの表面酸化層を除去する必要があるが、チタンシリサイド膜６はＨＦ溶液でエッチングされやすい。その点、本実施形態では、窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層１４はシリコンと窒素の結合を含んでいるためＳｉＮに近い組成を有しているものと思われ、ＨＦ溶液でエッチングされにくいと考えられる。そのため、本実施形態ではチタンシリサイド膜の対薬品性が向上し、プロセスの余裕度が増すという利点もある。

【００８４】ただし、本実施形態の半導体装置においては、チタンシリサイド膜６の表面全面にバリア化合物層１４が形成されるため、第１の実施形態の半導体装置よりは、チタンシリサイド膜６のシート抵抗上昇は大きくなる。しかし、第１の実施形態で述べたようにその場合でもシート抵抗の増加割合は１０％程度であり、トランジスタ動作等には特に問題のない十分低い値である。

【００８５】（第４の実施形態）次に、第４の実施形態について説明する。本実施形態では、製造工程の図示は省略するが、上述の第３の実施形態における図３（ａ）～（ｃ）と同じ処理を行なった後、選択的ＣＶＤ法により、接続孔８内に埋込層となるタングステン膜１７を堆積する。そして、タングステン膜１７及び絶縁膜７の上にアルミニウム合金膜１６を堆積した後、これをパターニングして金属配線を形成する。

【００８６】図６は、本実施形態により形成された半導体装置の構造を示す断面図である。上記第３の実施形態では、Ａｌ－Ｔｉ化合物層１５とアルミニウム合金膜１６とによって埋込層及び金属配線が一体的に構成されていたが、本実施形態では、タングステン膜１７により埋込層が構成され、アルミニウム合金膜１６により金属配線が構成されている。そして、ソース・ドレイン領域４及びゲート電極５の上のチタンシリサイド膜６の全面上に窒素－酸素－金属－シリコン間化合物からなるバリア化合物層１４が形成されていて、タングステン膜１７とチタンシリサイド膜６とがこのバリア化合物層１４を介して接触している。つまり、本実施形態の半導体装置は、埋込層と金属配線とが異なる材料で構成されている点のみが第３の実施形態の半導体装置と異なり、他の部分は第３の実施形態の半導体装置と同じ構造を有する。したがって、上記第３の実施形態と基本的には同様の効果を発揮することができる。

【００８７】加えて、本実施形態の半導体装置においては、埋込層がタングステン膜１７で構成されているので、バリア化合物層１７により、タングステンとチタンシリサイドとの反応を防止すればよい。したがって、その後の６００℃以上の熱処理でチタンシリサイドとタングステンとが反応してシリコン基板中に金属が侵入し、接合リークが発生するのを防止することができる。

【００８８】（第５の実施形態）次に、第５の実施形態について説明する。図７（ａ）～（ｄ）は、本実施形態の半導体装置の製造工程を示す断面図である。

【００８９】まず、図７（ａ）に示すように、シリコン基板１上のフィールド酸化膜２により取り囲まれる活性領域の上に、シリコン酸化膜からなるゲート酸化膜３と、ポリシリコン膜からなるゲート電極５と、シリコン酸化膜からなるサイドウォール９と、シリコン基板１内に不純物を導入してなるソース・ドレイン領域４とを備えたＭＯＳトランジスタを形成する。そして、スパッタ法により、基板上に例えばコバルト膜を堆積し、窒素雰囲気中５００℃で熱処理した後、H2 SO4 －H2 O2 混合液で未反応コバルト膜を除去することにより、ソース・ドレイン領域４とゲート電極５との上にのみ、厚みが５０ｎｍ程度のコバルトシリサイド膜２４を選択的に形成する。その後、８５０℃で熱処理を行いコバルトシリサイド膜２４を低抵抗化する。

【００９０】次に、図７（ｂ）に示すように、平行平板電極を構成する上部電極２９及び下部電極２６と、ハイパスフィルター２７と、ローパスフィルター２８と、１３．５６ＭＨｚの高周波電源２９と、４００ＫＨｚの高周波電源３０とを有するプラズマ発生装置を用い、プラズマ発生装置の反応室（図示せず）内に配置される下部電極２６の上に半導体装置を載置し、コバルトシリサイド膜２４の表面を窒素ガス等の窒素含有ガスのプラズマにさらす。例えば温度４００℃，圧力２Torrの下で、１００％のN2 ガスを導入し、上部電極２５に高周波電源２９により８０Wの高周波電力を、下部電極２６に高周波電源３０により１００Wの高周波電力を９００secの間印加する。このとき、反応室内に窒素プラズマＰlzが発生する。この窒素プラズマＰlz中の窒素はN+ ，Ｎ2+等の陽イオンになっており、下部電極２６の方が周波数が低いため、下部電極２５の方向に窒素イオンが引かれる。つまり、２周波数電力加式のプラズマ発生装置を使用しても、低周波数側の電力が印加される電極の上に半導体装置を設置することで、コバルトシリサイド膜２４表面への窒素の導入が促進されることとなる。この時、コバルトシリサイド膜２４の表面に形成されている自然酸化層中の酸素ないしチャンバに残存していた酸素

GF Exhibit 1124 - 1492/2704

もコバルトシリサイド層２４内に取り込まれ、窒素－酸素－コバルト－シリコン間化合物からなるバリア化合物層１４がコバルトシリサイド膜２４の表面付近に形成される。

【００９１】次に、図7（ｃ）に示すように、ＤＭＡＨ（ジメチルアルミニウムハイドライド）を用いた選択ＣＶＤ法により、バリア化合物層１４の上のみに第１のアルミニウム膜２２を形成する。ＤＭＡＨを用いた選択ＣＶＤ法は導電層の上のみに選択的にアルミニウム膜を堆積できる方法である。

【００９２】次に，図7（ｄ）に示すように、第１のアルミニウム膜２２の上に厚みが８００ｎｍ程度の絶縁膜７を形成し、絶縁膜7にソース・ドレイン領域４上の第１のアルミニウム膜２２に到達する接続孔８を開口する。

【００９３】次に、図7（ｅ）に示すように、ＤＭＡＨを用いた選択ＣＶＤ法により、接続孔８内に第２のアルミニウム膜２３を形成する。さらに、スパッタ法により、第２のアルミニウム膜２３及び絶縁膜7の上にアルミニウム合金膜１６を堆積し、フォトリソグラフィ法により、アルミニウム合金膜１６をパターニングして、金属配線を形成する。

【００９４】図8は、上述の製造方法によって形成された半導体装置の断面構造を示すものである。すなわち、シリコン基板１上に、ゲート酸化膜３と、ポリシリコン膜からなるゲート電極５と、ソース・ドレイン領域４と、ソース・ドレイン領域４及びゲート電極５上に形成されたコバルトシリサイド膜２４と、サイドウォール９とを備えたＭＯＳトランジスタが形成されている。そして、コバルトシリサイド膜２４の全面上に窒素－酸素－コバルト－シリコン間化合物からなるバリア化合物層１４が形成され、さらにコバルトシリサイド膜２４のバリア化合物層１４の上に第１のアルミニウム膜２２が形成されている。そして、基板上に形成された絶縁膜７にはソース・ドレイン領域４上の第１のアルミニウム膜２２に到達する接続孔８が形成されており、この接続孔８内に埋込層としての第２のアルミニウム膜２３が形成されている。また、第２のアルミニウム膜２３及び絶縁膜７の上に金属配線を構成するアルミニウム合金膜１６が形成されている。つまり、本実施形態の半導体装置においては、ソース・ドレイン領域４及びゲート電極５の上のコバルトシリサイド膜２４の全面上にバリア化合物層１４が形成されているとともに、コバルトシリサイド膜２４の上に電気抵抗の低いアルミニウム膜（低抵抗層）が形成されている点に特徴がある。

【００９５】次に、本実施形態で得られる半導体装置のバリア化合物層１４の構造の詳細と、本実施形態の半導体装置における第１のアルミニウム膜２２の反応防止効果の詳細とについて説明する。

【００９６】図１２（ａ）～（ｃ）は、プラズマ処理されていないコバルトシリサイド膜，N2 ガス中でプラズマ処理されたコバルトシリサイド膜及びNH3 ガス中でプラズマ処理されたコバルトシリサイド膜について、それぞれの表面付近の領域をＸＰＳ法によって分析した結果得られた各元素の濃度プロファイルを示す図である。ただし、図１２（ａ）～（ｃ）において、横軸は表面からの深さを、縦軸は各元素の組成比を示している。プラズマ処理されていないコバルトシリサイド膜でも、シリサイド形成時に窒素雰囲気中で７５０℃の熱処理が行われるので、その表面付近に窒素が導入されているが、窒素濃度のピークは表面位置にあり、その後窒素濃度が減少して約２ｎｍの深さ位置において窒素がなくなっている。また、酸素濃度も約２ｎｍの深さ位置でほとんど無視できるぐらいまで小さくなっている。それに対し、Ｎ２ ガス中或いはNH3 ガス中でプラズマ処理されたコバルトシリサイド膜においては、その表面から２ｎｍ程度奥方に入った深さ位置に窒素濃度のピークがみられる。また、酸素濃度の濃い領域も、その表面から約６ｎｍの深さ位置にまで及んでいる。すなわち、窒素雰囲気中でプラズマ処理が行われたコバルトシリサイド膜においては、その表面から約６ｎｍの深さ位置に亘って窒素－酸素－コバルト－シリコン間化合物からなるバリア化合物層が形成されていることがわかる。

【００９７】本実施形態では、コバルトシリサイド膜２４の表面付近にバリア化合物層１４を形成した結果、コバルトシリサイド膜２４の電気抵抗が３．５Ω／□から３．６Ω／□に増大したが、その増加割合は１０％以下であり、トランジスタの動作等には特に問題のない十分低い値である。

【００９８】図１３は、コバルトシリサイド膜の上に第１のアルミニウム膜２２としてＡｌ－０．５％Ｃｕ膜を堆積してアニール処理を行った結果得られた各種試料のシート抵抗のアニール温度依存性を示す図であり、コバルトシリサイド膜には、９００sec の間N2 ガス中でプラズマ処理されたものと、９００sec の間NH3 ガス中でプラズマ処理されたものと、プラズマ処理されなかったものとがある。プラズマ処理は、厚みが５０ｎｍのコバルトシリサイド膜に、９００sec の間、N2ガス又はNH3 ガス中で窒素プラズマを照射することにより行われた。そして、いずれの試料についても、コバルトシリサイド膜の上にＡｌ－０．５％Ｃｕ合金膜が約２００ｎｍの厚みで堆積されており、その後、約３０分間アニールされている。

【００９９】同図を参照するとわかるように、プラズマ処理されていない試料では、４００℃でアニールされたときのシート抵抗値の増大はそれほどでないものの４３０℃でアニールされたときのシート抵抗値は著しく増大している。それに対し、プラズマ処理された試料は、いずれも４００℃，４３０℃でアニールされても抵抗値の増大が抑制されている。すなわち、コバルトシリサイド

GF Exhibit 1124 - 1493/2704

膜の表面に形成されたバリア化合物層により、アルミニウム膜とコバルトシリサイド膜との反応が抑制されていることがわかる。一般に、シンターは４００～４５０℃程度で行われるので、このようなシート抵抗値の抑制効果は、実用上重要な意義がある。

【０１００】また、４３０℃でアニールされた試料をＸＰＳ分析した結果、窒素プラズマ処理されていないものは、Ｃｏ2 Ａｌ19又はＣｏ4 Ａ13 合金が形成されていたのに対し、窒素プラズマ処理された試料では、ＡｌとＣｏＳｉ2 のピークしか見られなかった。つまり、X線分析からも窒素プラズマ処理によりＡｌとＣｏＳｉ2との反応が４３０℃まで抑制されていることがわかった。

【０１０１】以上のように、本実施形態によれば、金属シリサイドの表面に窒素プラズマ処理を行って、金属シリサイド膜の表面に窒素－酸素－金属－シリコン間化合物からなるバリア化合物層を形成するようにしたので、その後の工程の熱処理により金属シリサイド膜とアルミニウム合金との反応により生じた金属のシリコン基板中への進入を有効に阻止できる。つまり、従来の方法のごとく８００℃以上の熱処理をシリサイド膜に加えてバリア化合物層を形成する必要がないので、ソース・ドレイン領域中のボロンが金属シリサイド膜中に吸い上げられ、Ｐチャネルトランジスタの飽和電流値が低下するという問題がない。また、５５０℃以下の低い温度で窒素プラズマ処理を行っているので、多種類の金属シリサイドについても金属シリサイド膜の凝集を生じることがないという効果をることができる。つまり、金属シリサイドを構成する金属材料の選択の幅の拡大を図ることができるのである。

【０１０２】（他の実施形態）上記第１又は第３の実施形態において、アルミニウム合金膜１６とＡｌ－Ｔｉ化合物層１５から接続孔８上の金属配線を形成しているが、Ａｌ－Ｔｉ化合物層１５は別の金属膜ないしはその化合物でもよく、あるいは設けなくてもよい。さらに、他の金属膜をアルミニウム合金膜１６上に積層してもよい。また、アルミニウム合金膜１６として、シリコンと銅を含むアルミニウム合金を用いたが、シリコンのみやスカンジウムなど他の金属を含む他のアルミニウム合金や純アルミニウムを用いてもよい。また、アルミニウム合金の代わりに銅または銅合金を用いてもよい。

【０１０３】上記各実施形態では、窒素を含むガスとしてN2 ガスを用いたが、まず、NH3 ガスやH2 ガスを流して金属シリサイド膜の表面の自然酸化膜を除去し、その後、N2 ガスに微量のO2 ガスを加えた雰囲気の中でプラズマを発生させて、窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層を形成してもよい。その場合、酸素量をコントロールできるので、バリア化合物層内の各元素の分布をできるだけ最適状態に近付けることができ、自然酸化膜を利用するよりもさらにコンタクト抵抗の低いかつ接合リーク防止効果の高いバリア化合物層を有する半導体装置を形成することができる。

【０１０４】また、NH3 ガスを用いてプラズマ処理を行なう場合でも、５５０℃以下でプラズマ処理を行なうことにより、上記従来の８００℃程度の条件下でプラズマ処理を行なって窒化チタンを形成する場合のような不具合は生じない。さらに、NH3 ガスを用いてプラズマ処理を行なう場合でも、自然酸化膜を利用して窒素－酸素－チタン等の金属－シリコン間化合物からなるバリア化合物層を形成することができる条件下であれば、本発明の効果を発揮することは可能である。

【０１０５】図１４は、NH3 ガスを用いてコバルトシリサイド表面をプラズマ処理した場合にシリサイド表面に形成されるバリア化合物層を示すＴＥＭ写真図である。プラズマ発生条件は第５の実施形態で述べたN2 ガスのプラズマ発生条件と同じである。約４－６ｎｍ厚みの窒素－酸素－コバルト－シリコン間化合物層（アモルファス層）が形成されていることがわかる。また、すでに述べた図１３のデータに示されるように、熱処理の際のアルミニウムとコバルトシリサイドとの反応によるシート抵抗の上昇が４３０℃まで抑制されており、N2 ガスを用いた場合と同じ程度の反応抑制効果があることがわかる。その理由は、すでに説明した図１２に示されるように、NH3 ガスを用いると、窒素－酸素－コバルト－シリコン間化合物層中の酸素の組成比が低減され、窒素の組成比が高くなっており、両者の組成比が適度に調整されることによるものと推定される。

【０１０６】なお、プラズマ形成の条件としては、上記各実施形態における条件以外の他の条件を用いることができることはいうまでもない。

【０１０７】上記各実施形態において、チタンシリサイド膜又はコバルトシリサイド膜の表面を窒素プラズマ処理して窒素－酸素－シリコン間化合物層を形成する工程は、スパッタ装置ないしは選択ＣＶＤ装置内で、接続孔内に銅、アルミニウム、タングステンないしはその合金を堆積させる直前に同一装置内でおこなってもよいし、あるいは、バリア化合物層の上のみに銅，アルミニウム，タングステンないしはその合金を選択ＣＶＤ法で形成する直前に同一装置内で行ってもよい。

【０１０８】また、上記各実施形態において、金属シリサイド膜としてチタンシリサイドを用いたが、コバルトシリサイド，ニッケルシリサイド，タンタルシリサイド，タングステンシリサイド，ニオブシリサイド，パラジウムシリサイド，白金シリサイド及びモリブデンシリサイド等を用いてもよい。

【０１０９】また、上記各実施形態において、窒素－酸素－金属－シリコン間化合物からなるバリア化合物層を形成する工程において、金属シリサイド膜の表面を窒素を含むガスのプラズマにさらす代わりに、金属シリサイド膜の表面を窒素を含むガスにさらすと同時に紫外線や電離放射線を照射することにより、紫外線等のエネルギ

GF Exhibit 1124 - 1494/2704

ーを利用して、温度５５０℃以下の低温で、金属シリサイド膜の表面に窒素－酸素－金属－シリコン間化合物からなるバリア化合物層を形成してもよい。あるいは、プラズマを使用する代わりに、金属シリサイド膜の表面を窒素を含むイオンビームにさらすことにより、イオンのエネルギーを利用して、温度５５０℃以下の低温で、金属シリサイド膜の表面に窒素－酸素－金属－シリコン間化合物からなるバリア化合物層を形成してもよい。

【０１１０】なお、第１～第４の実施形態において、窒素－酸素－金属－シリコン間化合物からなるバリア化合物層を形成する工程において、プラズマ処理、紫外線線等の照射、イオンビームの照射などのいずれを選択する場合にも、窒素イオンを金属シリサイド側に引き寄せるための電位は、３ｋｅＶ程度以下であることが好ましい。その理由について説明する。一般的に、シリコン中における窒素イオンの飛程から類推すると、電位が１ｋｅＶの場合には、シリコン中の窒素濃度は深さ３．８ｎｍの部位でピークとなり、深さ９．８ｎｍの部位で１０％まで減小する。そして、電位が３ｋｅＶの場合には、シリコン中の窒素濃度は深さ８．５ｎｍの部位でピークとなり、深さ２０．３ｎｍの部位で１０％まで減小する。したがって、通常７０ｎｍ程度の厚みのシリサイド膜のうち３０％に相当する２０ｎｍ程度の深さまでにバリア化合物層の形成を抑えておくことで、シート抵抗やコンタクト抵抗の増大を回避できる。

【０１１１】また、本発明のバリア化合物層が形成される金属シリサイド膜は上記各実施形態に示すゲート電極やソース・ドレイン領域上に限定されるものではない。例えば、ポリシリコン膜を抵抗やコンデンサの構成要素（特に電極）として利用する際にも、ポリシリコン膜上のシリサイド膜が形成されることがあり、その場合にも、上層配線とコンタクトする金属シリサイド膜の表面に本発明の窒素－酸素－金属－シリコン間化合物からなるバリア化合物層を形成することにより、接続孔内にバリアメタルを堆積しなくても、埋込層と金属シリサイド層との反応で生じた金属等が電極中あるいは電極を介して他の部材中に侵入するのを有効に防止することができる利点がある。

【０１１２】また、第５の実施形態では、ソース・ドレイン領域４及びゲート電極５の上のコバルトシリサイド膜２４の全面上に窒素－酸素－金属－シリコン間化合物からなるバリア化合物層１４が形成されていて、第１のアルミニウム膜２２とチタンシリサイド膜６とがこのバリア化合物層１４を介して接触しているが、第１のアルミニウム膜２２の代わりに、アルミニウムを含む金属，銅を含む金属及びタングステンを含む金属からなる膜が堆積された場合にも同じ効果が得られる。例えば第１のアルミニウム膜２２の代わりにタングステン膜が用いられた場合でも、バリア化合物層１４の存在によって、その後の６００℃以上の熱処理でコバルトシリサイドとタングステンとが反応してシリコン基板中に金属が進入し、接合リークが生じるのを有効に防止することができる。

【０１１３】

【発明の効果】以上説明したように、本発明によれば、金属シリサイド上の絶縁膜に形成される接続孔内の埋込層を介して金属シリサイド膜と上層の配線とが電気的に接続される半導体装置において、少なくとも接続孔の底面となる金属シリサイド膜の表面付近の領域に窒素－酸素－金属－シリコン間化合物からなるバリア化合物層を形成するようにしたので、接続孔内にバリアメタルを堆積することによる信頼性の低下を招くことなく、半導体基板等への化合物の侵入を阻止することができ、よって、金属シリサイド膜全体のシート抵抗値を低く保ち、かつ接合リークを抑制し得ると共に接続孔内への埋込層の信頼性の高い半導体装置およびその製造方法を提供することができる。

【図面の簡単な説明】

）

【図１】第１の実施形態における半導体装置の製造工程を示す断面図である。

【図２】第１の実施形態における半導体装置の断面図である。

【図３】第２の実施形態における半導体装置の断面図である。

【図４】第３の実施形態における半導体装置の製造工程を示す断面図である。

【図５】第３の実施形態における半導体装置の断面図である。

【図６】第４の実施形態における半導体装置の断面図である。

【図７】第５の実施形態における半導体装置の製造工程を示す断面図である。

【図８】第５の実施形態における半導体装置の断面図である。

【図９】第１の実施形態における半導体装置のチタンシリサイド膜表面の深さ方向の元素分析結果を示す図である。

【図１０】窒素プラズマ処理を行なわない試料、第１の実施形態の処理を行なった試料、及びリファレンスの試料についての接合リーク特性を比較する図である。

【図１１】窒素プラズマ処理を行なった後Ａｌ合金を堆積してアニール処理を行なった各種試料のシート抵抗のアニール温度依存性を示す図である。

【図１２】プラズマ窒化処理を行わない場合、N2 ガス雰囲気でプラズマ窒化処理を行った場合、ＮH3 ガス雰囲気でプラズマ窒化処理を行った場合におけるＣｏＳｉ2膜の表面付近をＸＰＳ分析した結果得られた各元素の組成比をそれぞれ示す図である。

【図１３】プラズマ窒化処理を行わない場合、N2 ガス

GF Exhibit 1124 - 1495/2704

雰囲気でプラズマ窒化処理を行った場合、NH3 ガス雰囲気でプラズマ窒化処理を行った場合におけるＡｌＣｕ／ＣｏＳｉ2 構造のシート抵抗の温度依存性を示す図である。

【図１４】NH3 ガス雰囲気でプラズマ窒化処理を行った場合におけるＡｌＣｕ／ＣｏＳｉ2 構造の境界付近におけるＴＥＭ写真図である。

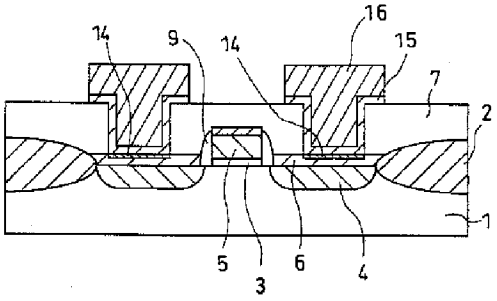
【図１５】従来の半導体装置の製造工程を示す断面図である。

【符号の説明】

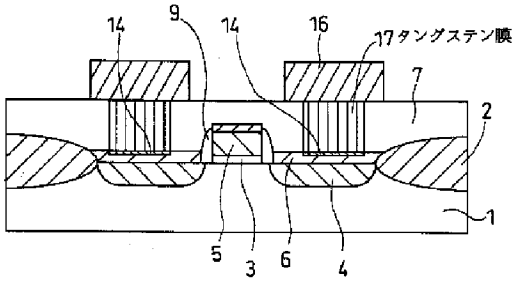
１	シリコン基板
２	フィールド酸化膜
３	ゲート酸化膜
４	ソース・ドレイン領域
５	ゲート電極
６	チタンシリサイド膜
７	絶縁膜
８	接続孔
９	サイドウォール
１０	陽極
１１	陰極
１２	ブロッキングコンデンサー
１３	高周波電源
１４	バリア化合物層
１５	Ａｌ－Ｔｉ化合物層
１６	アルミニウム合金膜
１７	タングステン膜
１８	直流電源
Ｐｌｚ	窒素プラズマ
２２	第１のアルミニウム膜
２３	第２のアルミニウム膜
２４	コバルトシリサイド膜
２５	上部電極
２６	下部電極
２７	ハイパスフィルター
２８	ローパスフィルター
２９	高周波電源
３０	高周波電源

【図１】

【図２】

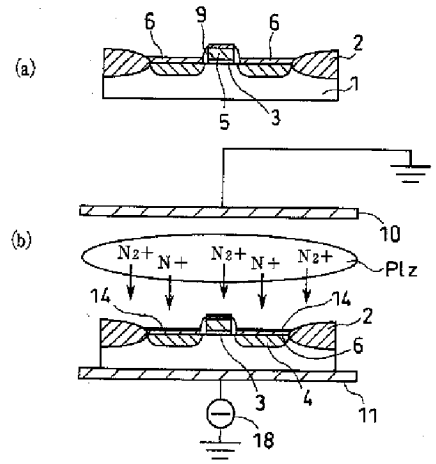


【図３】

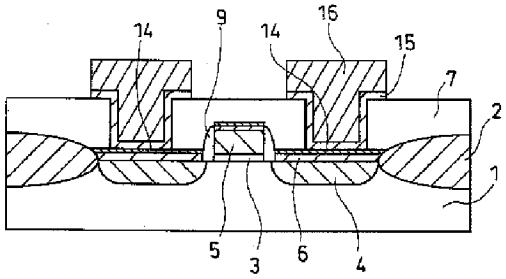


GF Exhibit 1124 - 1496/2704

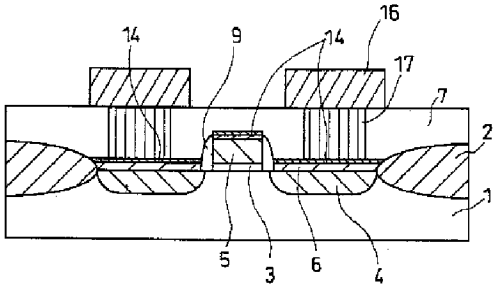
【図4】



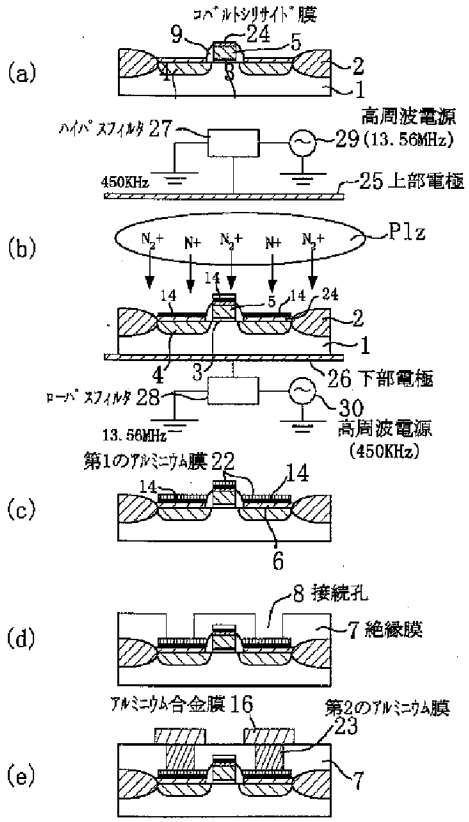
【図5】



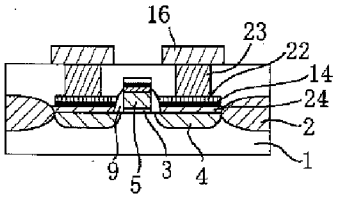
【図6】



【図7】

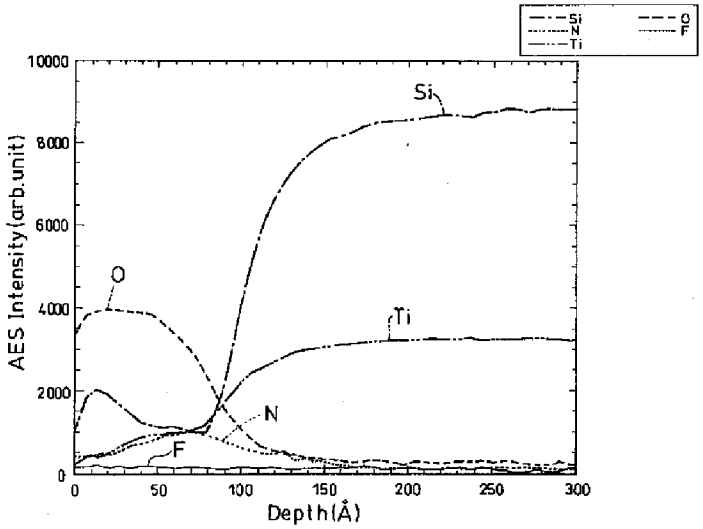


【図8】

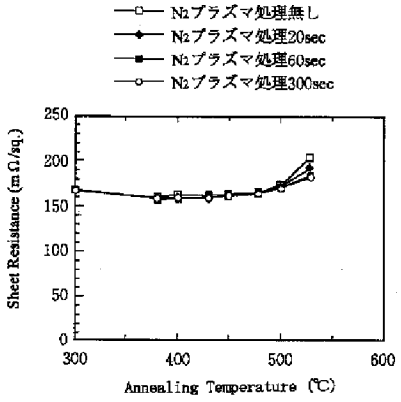


GF Exhibit 1124 - 1497/2704

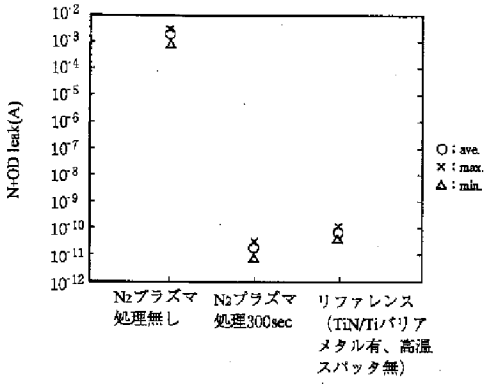
【図9】



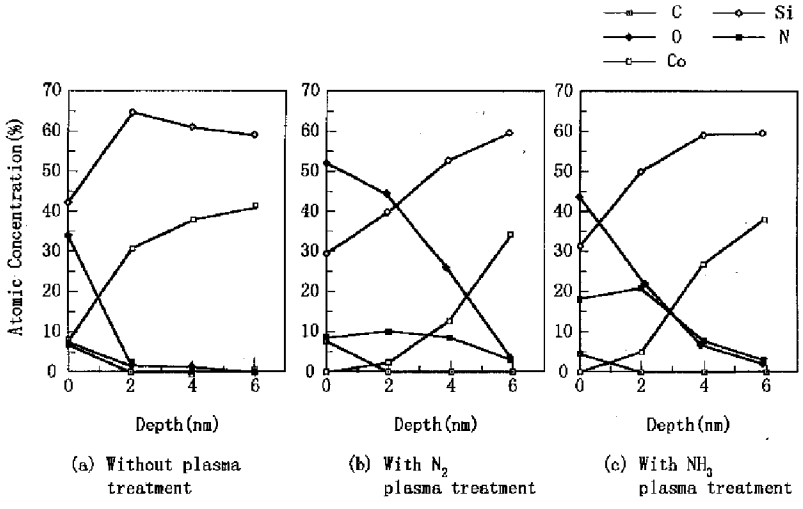
【図11】



【図10】

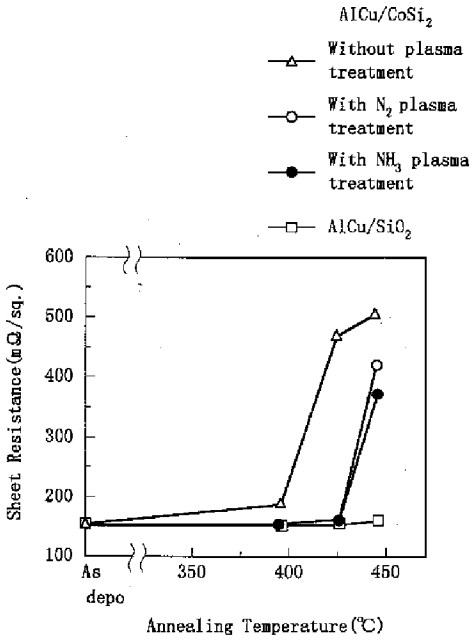


【図12】

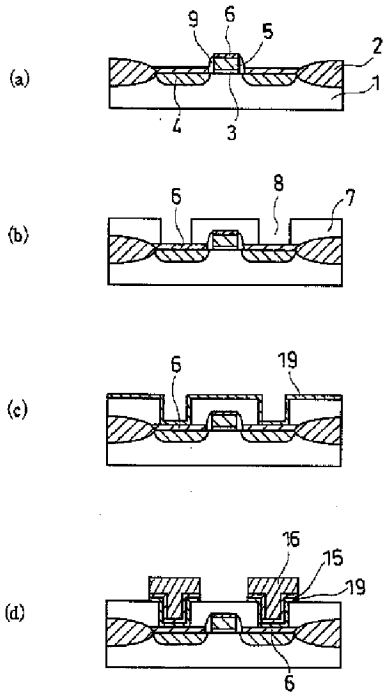


GF Exhibit 1124 - 1498/2704

【図13】



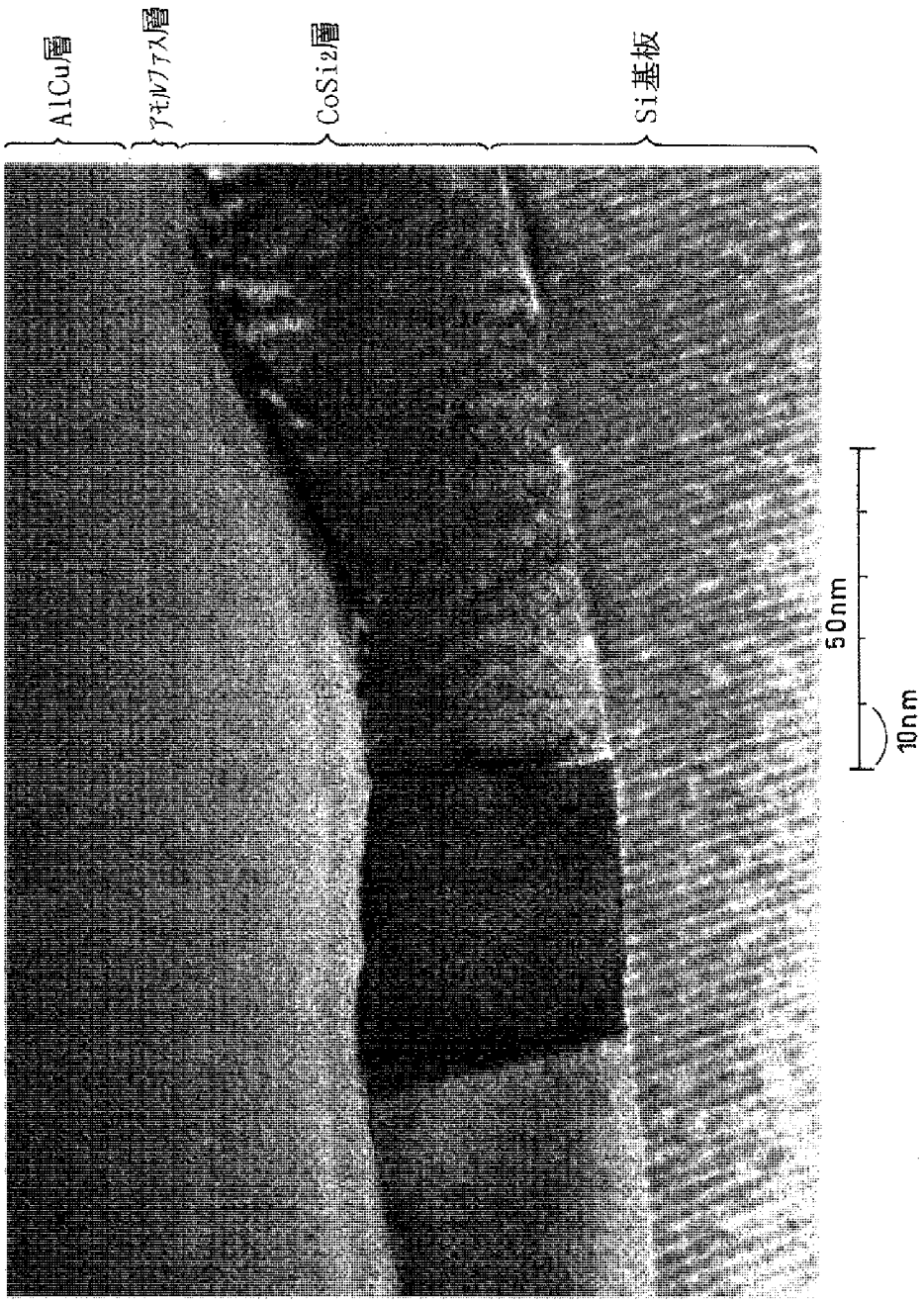
【図15】



GF Exhibit 1124 - 1499/2704

【図14】

図面代用写真



フロントページの続き

(51)Int.Cl.[6]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０１Ｌ　21/336				

GF Exhibit 1124 - 1500/2704

Europäisches Patentamt
European Patent Office
Office européen des brevets

Espacenet

JPH09289178A SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

Applicants: MATSUSHITA ELECTRIC IND CO LTD

Inventors: SEKIGUCHI MITSURU,YAMANAKA MICHINARI

Classifications:

IPC ***H01L21/265; H01L21/28; H01L21/3205; H01L21/336; H01L21/768; H01L23/52; H01L29/78;***
(IPC1-7): H01L21/265; H01L21/28; H01L21/3205; H01L21/336; H01L21/768; H01L29/78;

Priorities: JP3451296A 1996-02-22; JP4705397A 1997-02-14

Application: JPH09289178A·1997-02-14

Publication: JPH09289178A·1997-11-04

Published as: JPH09289178A

SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

Abstract

PROBLEM TO BE SOLVED: To prevent generation of junction leak or the like which are to be caused by reaction between a metal silicide and a metal layer thereon at the time of thermal treatment, in a semiconductor device. SOLUTION: After connection holes 8 is formed or before an insulating film 7 is deposited, a semiconductor device is fixed on a cathode 11 of a plasma generating equipment. For example, the surface of a metal silicide layer such as a titanium silicide film 6 is exposed to plasma of gas containing nitrogen at a temperature lower than or equal to 550 deg.C. By this treatment, a barrier compound layer 14 composed of nitrogen-oxygen-metal-intersilicon compound is formed in a region in the vicinity of the surface of the metal silicide film such as the titanium silicide film 6. Reaction between the metal silicide layer and a buried layer in the later thermal treatment can be obstructed, while the buried layer is formed by using material having excellent step-difference coverage, e.g. an Al-Ti compound layer 15 and an aluminum alloy film 16, without depositing barrier metal such as titanium nitride . a nitride film on the connection holes 8. Thereby contact resistance, sheet resistance, and junction leak are reduced, and reliability can be improved.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION JPH09289178

[0001]
BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor device having a silicide layer and a method of manufacturing the same, and more particularly to improvement of a structure of a contact portion between an upper wiring of the silicide layer and an upper low resistance metal film. ..

[0002]
2. Description of the Related Art In recent years, with higher integration and higher density of VLSI, metal silicide layers are formed on the surfaces of gate electrodes and source / drain regions of MOS transistors mounted on VLSI in a self-aligned manner. A technique (salicide technique) is used to reduce the sheet resistance of the gate electrode and the source / drain regions and reduce the parasitic resistance such as contact resistance and diffusion resistance to improve the operation speed of the semiconductor element.

[0003]

By the way, as a method of forming a buried layer made of aluminum, tungsten, and copper on the metal silicide layer, for example, a high temperature sputtering method utilizing the fluidity of an aluminum alloy at a high temperature, or a chemical vapor deposition excellent in coating property. There is known a method of forming a highly reliable buried layer by selectively depositing a metal such as aluminum, tungsten, or copper in the connection hole by a (hereinafter referred to as CVD) method.

GF Exhibit 1124 - 1502/2704

In that case, a reaction may occur between the metal composing the buried layer and the metal silicide layer, which may cause a problem. That is, since a thermal history of about 450 to 600 ° C. is generated in high temperature sputtering, selective CVD, or CVD for forming an upper layer wiring, the metal silicide reacts with the metal forming the buried layer, and the reaction product produces silicon. The substrate may be eroded and a junction leak may occur. Therefore, in order to suppress the reaction between the two, a barrier metal such as titanium nitride is generally formed between the buried layer and the metal silicide layer.

[0004]
Hereinafter, a conventional method of forming a buried layer on a metal silicide layer by using a high temperature sputtering method will be described with reference to FIGS.

[0005]

First, as shown in FIG. 15A, a gate oxide film 3 made of a silicon oxide film and a gate electrode 5 made of a polysilicon film are formed on an active region surrounded by a field oxide film 2 on a silicon substrate 1. Then, a MOS transistor having sidewalls 9 made of a silicon oxide film and source / drain regions 4 made by introducing impurities into the silicon substrate 1 is formed.

Then, for example, a titanium film is deposited on the source / drain region 4 and the gate electrode 5 of the MOS transistor by a sputtering method, heat-treated at 600 to 900 ° C., and then unreacted titanium is mixed with a H 2 SO 4 -H 2 O 2 mixed solution. By removing the film, the titanium silicide film 6 is selectively formed only on the source / drain regions 4 and the gate electrode 5.

[0006]
Next, as shown in FIG. 15B, an insulating film 7 is formed on the entire surface of the substrate, and a contact hole 8 reaching the titanium silicide film 6 in the source / drain region 4 is opened in the insulating film 7.

[0007]
Next, as shown in FIG. 15C, a titanium film and a barrier metal for improving the contact characteristics with the titanium silicide film 6 on the source / drain regions 4 in the connection

GF Exhibit 1124 - 1503/2704

hole 8 and on the insulating film 7. A titanium nitride film is deposited by the sputtering method to form a titanium nitride / titanium film 19.

[0008]

Next, as shown in FIG. 15 (d), titanium is sputtered and then an aluminum alloy is sputtered thereon at 500 ° C. to form an Al—Ti compound layer 15 formed by combining the aluminum alloy and titanium. , And the aluminum alloy film 16 thereon is formed.

At this time, the reaction heat between Al and Ti is used to fill the inside of the connection hole 8 with an aluminum alloy.

Then, the titanium nitride / titanium film 19, the Al—Ti compound layer 15, and the aluminum alloy 16 are patterned by photolithography to form metal wiring.

[0009]
However, when the diameter of the connection hole is further miniaturized in accordance with the miniaturization of the semiconductor device, in the above-mentioned conventional method, titanium nitride / titanium nitride is used in the step shown in FIG. 15 (c). It is not preferable to deposit the film 19 by the sputtering method for the following reasons.

[0010]

In general, since the titanium nitride film formed by the sputtering method does not have good step coverage, an overhang shape is likely to be formed at the corner of the connection hole.

Therefore, the flow of the aluminum alloy into the connection hole during high-temperature sputtering is hindered and the connection hole becomes difficult to fill (for example, Y. Takegawa et al. Abst. SSDM, p.558, 1993).

[0011]
Therefore, when forming a titanium nitride film, there is also a method of suppressing the

GF Exhibit 1124 - 1504/2704

formation of an overhang shape by sputtering titanium through a honeycomb filter (collimator) while flowing N2 gas, but when a collimator is used, particles are generated. It's easy to do.

[0012]
Further, in the step shown in FIG. 15B, the part other than the connection hole 8 (the part on the insulating film 7) is also covered with the titanium nitride / titanium film 19, so that the selective CVD method utilizing the difference in the underlying layer is used. It is not possible to use a method of selectively depositing a metal such as aluminum, tungsten, or copper only in the connection hole 8.

[0013]

On the other hand, in order to avoid the above-mentioned problems, after forming the contact hole in the insulating film, the titanium nitride / titanium film 19 is not deposited and heat treatment is performed in an NH3 atmosphere at about 850 ° C. A technique has been proposed in which a titanium nitride film is formed on the surface of a titanium silicide film, and then aluminum is selectively deposited only in the contact holes by a selective CVD method (for example, H. Shinriki et al. Ext.

Abst.

SSDM, p.968, 1994).

[0014]

However, if a heat treatment at 800 ° C. or higher is applied to the titanium silicide film, boron in the source / drain regions may be absorbed into the titanium silicide film, and the saturation current value of the P-channel transistor may decrease. Further, depending on the type of metal silicide, when heat treatment is performed at a high temperature, the silicide agglomerates to increase the sheet resistance of the source / drain. Therefore, the types of silicide to which the above conventional method can be applied are limited.

[0015]

GF Exhibit 1124 - 1505/2704

In addition, the above-mentioned problems occur not only between the buried layer in the connection hole and the silicide film, but also when a low resistance metal film is formed on the silicide film. This is a cause of deteriorating the reliability of the laminated structure of the silicide film and the metal film.

[0016]
The present invention relates to a compound that causes a junction leak in a semiconductor substrate when a compound layer made of a nitrogen-oxygen-metal-silicon compound is formed in the vicinity of a boundary between a metal silicide layer and a metal film thereon. It was made based on the discovery of the fact that the invasion of the barrier does not occur, and the purpose is to form a compound layer that serves as such a barrier, thereby eliminating the need for a barrier metal and forming a buried layer or a silicide film and a metal film. It is an object of the present invention to provide a semiconductor device capable of keeping the sheet resistance value of the entire metal silicide film low and preventing the occurrence of a junction leak while improving the reliability of the laminated structure, and a manufacturing method thereof.

[0017]
In order to achieve the above object, the present invention provides means for a semiconductor device according to claims 1 to 9 and a semiconductor device according to claims 12 to 23. Measures related to the manufacturing method are taken.

[0018]
As described in claim 1, a semiconductor device of the present invention includes a semiconductor substrate, a metal silicide film formed on a part of the semiconductor substrate and having a first metal silicided, and the metal silicide film. And a barrier compound layer formed of a nitrogen-oxygen-first metal-silicon compound and formed in a region near the surface of the metal silicide film. There is.

[0019]

As a result, since the barrier compound layer made of the nitrogen-oxygen-metal-silicon compound is formed on the surface of the metal silicide film, even if there is a high temperature history during the manufacturing process such as when depositing the metal film, the metal The reaction between the first metal forming the silicide film and the second metal forming the metal film is suppressed.

GF Exhibit 1124 - 1506/2704

That is, the occurrence of junction leakage and the deterioration of the characteristics of the gate oxide film are suppressed without interposing a barrier metal such as titanium nitride / nitride film.

Therefore, it is possible to avoid problems due to poor step coverage and resistance characteristics of the barrier metal, such as a decrease in reliability and an increase in sheet resistance.

[0020]
As described in claim 2, in claim 1, it is preferable that the barrier compound layer is formed in a region near the surface of the entire metal silicide film.

[0021]
This simplifies the manufacturing process of the semiconductor device and improves the chemical resistance of the metal silicide layer, and as a result, the manufacturing cost can be reduced.

[0022]
As described in claims 3 and 4, in claim 1 or 2, the thickness of the barrier compound layer is not less than a thickness sufficient to prevent diffusion of the second metal into the barrier compound layer. Then, it is preferably 30% or less of the thickness of the metal silicide film, or from another viewpoint, it is preferably in the range of 2 to 20 nm.

[0023]
As a result, an increase in contact resistance and sheet resistance due to the formation of a too thick barrier compound layer is suppressed as much as possible.

[0024]
As described in claim 5, in claim 1, 2 or 3, the position where the concentration of the nitrogen in the barrier compound layer is maximum is located deeper than the position where the concentration of the oxygen is maximum. Preferably.

[0025]

GF Exhibit 1124 - 1507/2704

As a result, the oxygen concentration becomes relatively low at the position where the nitrogen concentration becomes high, so that the region where the concentration of the oxide layer is high, which causes the increase in contact resistance and sheet resistance, can be suppressed near the surface. ..

Therefore, an increase in sheet resistance or the like at the contact portion between the metal film and the silicide film can be suppressed as much as possible.

[0026]
According to a sixth aspect of the present invention, in the first aspect, the insulating film formed on the metal silicide film and the connection hole formed in a part of the insulating film and reaching the metal silicide film are provided. Further, the metal film may be a buried layer made of the second metal deposited in the connection hole.

[0027]

Accordingly, since the barrier compound that suppresses the reaction between the first metal and the second metal exists in the region near the surface of the metal film, it is not necessary to form the barrier metal in the connection hole.

Therefore, it is possible to select a second metal having a good coverage as the second metal forming the burying layer in the connection hole which is required to have the step coverage, and the reliability of the semiconductor device is improved.

[0028]
As described in claim 7, in claim 1, an insulating film formed on the metal silicide film, a connection hole formed in a part of the insulating film and reaching the metal silicide film, A buried layer made of a third metal deposited in the connection hole may further be provided.

[0029]
This makes it possible to select a material having a low electric resistance as the metal film composed of the second metal and to interpose the low resistance layer between the buried layer

GF Exhibit 1124 - 1508/2704

and the metal silicide film. It is possible to obtain a semiconductor device that is suitable for the realization.

[0030]
As described in claim 8, in claim 1, 2, 3, 4, 5, 6 or 7, the first metal is titanium, cobalt, nickel, tantalum, tungsten, niobium, palladium, platinum. And at least one of molybdenum.

[0031]
As described in claim 9, in claim 1, 2, 3, 4, 5, 6 or 7, the second metal is a metal containing aluminum, a metal containing copper or a metal containing tungsten. It is preferable to configure at least one of them.

[0032]
According to a tenth aspect of the present invention, there is provided a method of manufacturing a semiconductor device, comprising: forming a metal silicide film made of a compound of a first metal and silicon on a semiconductor substrate; Of a nitrogen-oxygen-first metal-silicon compound in the region near the surface of the metal silicide film by irradiating the surface of the metal silicide film with ions containing nitrogen under a neutral or oxidizing atmosphere. And a third step of depositing a second metal on the barrier compound layer of the metal silicide film to form a metal film.

[0033]

By this method, since the barrier compound layer is formed on the surface of the metal silicide film in the second step, it is possible to form the metal film in the third step without forming the barrier metal.

Therefore, by appropriately selecting and using a material having a good step coverage as the second metal, the step coverage with respect to the base of the metal film is improved, and a highly reliable semiconductor device can be formed.

[0034]
As described in claim 11, in claim 10, after the first step and before the second step, a step of forming an insulating film on the metal silicide film; And a step of selectively removing a part of

GF Exhibit 1124 - 1509/2704

the film to form a contact hole reaching the metal silicide film. In the second step, the contact hole in the region near the surface of the metal silicide film is formed. The barrier compound layer may be formed in a region exposed at the bottom of the substrate, and in the third step, the inside of the connection hole may be filled with the second metal.

[0035]
By this method, the formation region of the barrier compound layer is limited to a particularly required region, so that the increase of the sheet resistance of the metal silicide film is suppressed.

[0036]
As described in claim 12, in claim 10, the step of forming an insulating film on the barrier compound layer of the metal silicide film after the second step, and a part of the insulating film. Is further removed to form a connection hole reaching the barrier compound layer. In the third step, the second metal can be deposited in the connection hole.

[0037]

By this method, when the contact is formed from each wiring layer at an arbitrary position of the metal silicide film, the barrier compound layer is formed at any position. Therefore, the barrier compound layer is formed every time the connection hole is formed. Therefore, the process is simplified.

Further, since the resistance of the metal silicide film to chemicals such as HF is also improved, restrictions on subsequent steps are alleviated.

[0038]
As described in claim 13, in claim 12, the step of forming an insulating film on the barrier compound layer of the metal silicide film after the third step, and a part of the insulating film. The method may further include a step of selectively removing the metal to form a connection hole reaching the barrier compound layer, and a step of depositing a third metal in the connection hole to form a buried layer.

[0039]

GF Exhibit 1124 - 1510/2704

By this method, when a material having a low electric resistance is selected as the second metal, a low resistance layer is formed on the metal silicide film and a buried layer is formed on the metal silicide film. A good semiconductor device can be obtained.

[0040]
As described in claim 14, in claim 10, 11, 12 or 13, in the second step, a plasma generating device in which a lower electrode which is a cathode and an upper electrode which is an anode are arranged in a chamber. The barrier compound layer can be formed by exposing the metal silicide film to plasma of a gas containing nitrogen in a state where the semiconductor substrate is placed on the lower electrode in the chamber.

[0041]
By this method, by placing a semiconductor substrate on the cathode, nitrogen, which is a positive ion in nitrogen plasma, is efficiently taken into the metal silicide.

[0042]
As described in claim 15, in claim 10, 11, 12 or 13, in the second step, one of ultraviolet rays and ionizing radiation is performed while exposing the surface of the metal silicide film to a gas containing nitrogen. The barrier compound layer can be formed by irradiating either one.

[0043]
As described in claim 16, in claim 10, 11, 12 or 13, in the second step, the barrier compound layer is formed by exposing the surface of the metal silicide film to an ion beam containing nitrogen. Can be formed.

[0044]
As described in claim 17, in claim 10, 11, 12, 13, 14, 15 or 16, the second step is preferably performed at 550 ° C or lower.

[0045]
By this method, plasma treatment or the like is performed under a low temperature condition of 550 ° C. or less, so that even when titanium silicide or the like is used, the metal silicide is not aggregated and the selection range of the type of metal silicide is expanded.

GF Exhibit 1124 - 1511/2704

[0046]
As described in claim 18, in claim 10, 11, 12, 13, 14, 15 or 16, N 2 gas can be used as the nitrogen-containing gas in the second step.

[0047]
According to this method, when forming the barrier compound layer, the barrier compound layer made of the nitrogen-oxygen-metal-silicon compound is easily formed by utilizing the natural oxide film existing on the surface of the metal silicide film.

[0048]
As described in claim 19, in claim 10, 11, 12, 13, 14, 15, 16, 17 or 18, by flowing a gas containing hydrogen before the second step, The method further comprises a step of removing the natural oxide film on the metal silicide film, and a gas containing oxygen can be added in the second step.

[0049]
By this method, the oxygen concentration in the barrier compound layer is controlled, so that the distribution state of each element can be adjusted to a more preferable state.

[0050]
As described in claim 20, in claim 10, 11, 12, 13, 14, 15 or 16, in the second step, the nitrogen-containing ion is ion-energy of 3 keV or less, the metal silicide film. It is preferable to introduce it inside.

[0051]
By this method, the region where the barrier compound layer is formed is limited to a depth of about 20 nm from the surface of the metal silicide film, so that the increase in contact resistance and sheet resistance of the formed semiconductor device is suppressed. ..

[0052]
As described in claim 21, in claim 10, 11, 12, 13, 14, 15, 16, 17, 18, 19 or 20, in the first step, titanium is used as the metal silicide film. It is preferable to form a silicide film of any one of cobalt, nickel, tantalum, tungsten, palladium, platinum and molybdenum.

GF Exhibit 1124 - 1512/2704

[0053]
As described in claim 22, in claim 10, 11, 12, 13, 14, 15, 16, 17, 18, 19 or 20, in the third step, the CVD method is used to remove aluminum. It is preferable to deposit any one of a metal containing metal, a metal containing copper, and a metal containing tungsten.

[0054]
As described in claim 23, in claim 10, 11, 12, 13, 14, 15, 16, 17, 18, 19 or 20, titanium and aluminum alloy are continuously added in the third step. The metal film can be composed of an Al—Ti compound layer and an aluminum alloy film by sputtering.

[0055]
By these methods, it is possible to select the method of forming the metal film and the wiring according to the type of the semiconductor device and the difference in the wiring layer formed on the metal silicide film.

[0056]
DESCRIPTION OF THE PREFERRED EMBODIMENTS (First Embodiment) FIGS. 1A to 1D are cross-sectional views showing a manufacturing process of a semiconductor device according to a first embodiment.

[0057]

First, as shown in FIG. 1A, a gate oxide film 3 made of a silicon oxide film and a gate electrode 5 made of a polysilicon film are formed on an active region surrounded by a field oxide film 2 on a silicon substrate 1. Then, a MOS transistor having sidewalls 9 made of a silicon oxide film and source / drain regions 4 made by introducing impurities into the silicon substrate 1 is formed.

Then, for example, a titanium film is deposited on the substrate by a sputtering method, heat-treated at 650 ° C., and then the unreacted titanium film is removed with a mixed solution of H 2 SO 4 -H 2 O 2 to form the source / drain region 4 and the gate electrode. A titanium silicide film 6 having a thickness of about 70 nm is selectively formed only on the film 5.

Then, heat treatment is performed at 850 ° C. to reduce the resistance of the titanium silicide film.

GF Exhibit 1124 - 1513/2704

[0058]
Next, as shown in FIG. 1B, an insulating film 7 having a thickness of about 800 nm is formed on the entire surface of the substrate, and a contact hole reaching the titanium silicide film 6 in the source / drain region 4 is formed in the insulating film 7. Open 8

[0059]

Next, as shown in FIG. 1C, a plasma generator having an anode 10 and a cathode 11 forming a parallel plate electrode, a blocking capacitor 12, and a high frequency power source 13 is used, and a reaction chamber of the plasma generator (A semiconductor device which has undergone the steps up to FIG. 1B is mounted on a cathode 11 arranged inside (not shown), and the surface of the titanium silicide film 6 is exposed to plasma of a nitrogen-containing gas.

For example, at a temperature of 50 ° C. and under a pressure of 80 mTorr, 100% N 2 gas is introduced, and high frequency power of about 300 W is applied between the parallel plate electrodes 10 and 11 for 300 seconds.

At this time, nitrogen plasma Plz is generated in the reaction chamber.

Nitrogen in the nitrogen plasma Plz is positive ions such as N + and N2 +, and a total potential of 300V is generated in the direction of the cathode 11 by adding the plasma potential of about 60V and the self-bias voltage of about 240V.

Then, nitrogen ions are attracted to the surface of the semiconductor device at this potential.

That is, by installing the semiconductor device on the cathode 11 of the parallel plate electrodes 10 and 11, the introduction of nitrogen to the surface of the titanium silicide film 6 is promoted.

At this time, oxygen in the natural oxide layer formed on the surface of the titanium silicide film 6 is also taken into the titanium silicide layer 6, and the barrier compound layer 14 made of the nitrogen-oxygen-titanium-silicon compound is formed into the titanium silicide film 6. Formed

GF Exhibit 1124 - 1514/2704

near the surface of the.

[0060]

Next, as shown in FIG. 1D, titanium is sputtered to a thickness of about 75 nm, and then an aluminum alloy containing 1% of silicon and 0.5% of copper is sputtered to a thickness of about 900 nm at 500 ° C. By doing so, the Al—Ti compound layer 15 formed by combining the aluminum alloy and titanium and the aluminum alloy film 16 thereon are formed.

At this time, the reaction heat between Al and Ti is used to fill the inside of the connection hole 8 with an aluminum alloy to form a buried layer.

Then, the Al—Ti compound layer 15 and the aluminum alloy film 16 are patterned by photolithography to form metal wiring.

[0061]

In addition, a connection hole is also formed on the gate electrode 5 at the same time (in a cross section different from the cross section shown in FIGS. 1A to 1D), and a barrier compound is formed near the surface of the titanium silicide film 6 on the gate electrode 5. After forming the layer 14, the Al—Ti compound layer 15 and the aluminum alloy film 16 may be deposited to form the buried layer and the metal wiring.

[0062]

FIG. 2 shows a cross-sectional structure of a semiconductor device formed by the above manufacturing method.

That is, a gate oxide film 3, a gate electrode 5 made of a polysilicon film, a source / drain region 4, and a titanium silicide film 6 formed on the source / drain region 4 and the gate electrode 5 are formed on a silicon substrate 1. , Sidewalls 9 are formed.

A connection hole 8 reaching the titanium silicide film 6 on the source / drain region 4 is formed

GF Exhibit 1124 - 1515/2704

in the insulation film 7 formed on the substrate. The connection hole 8 is buried in the connection hole 8 and on the insulation film 7. An Al—Ti compound layer 15 and an aluminum alloy film 16 that form a layer and a metal wiring are formed.

As a feature of the semiconductor device according to the present embodiment, a barrier metal such as titanium nitride / nitride film is not formed under the aluminum alloy film 16, and instead, the titanium silicide film 6 on the source / drain region 4 is used. A barrier compound layer 14 made of a nitrogen-oxygen-titanium-silicon compound is formed only on the surface of a region which will be the bottom surface of the connection hole 8.

[0063]
Next, details of the structure of the barrier compound layer 14 of the semiconductor device obtained in the present embodiment and details of the contact resistance and the like in the semiconductor device of the present embodiment will be described.

[0064]

FIG. 9 is a diagram showing the concentration profile of each element obtained as a result of analyzing the region near the surface of the titanium silicide film 6 after the step shown in FIG. 1C according to the present embodiment by Auger electron spectroscopy. is there.

However, since the sensitivities of the respective elements are different during the analysis by Auger electron spectroscopy, FIG. 9 does not accurately show the composition ratio of each element, but merely shows the concentration distribution of each element.

As shown in FIG. 9, silicon and oxygen are particularly abundant up to 2 to 3 nm from the surface. This is because the SiO2 film was formed as a natural oxide film on the surface of the titanium silicide film in the analysis process. Thought to be a thing.

A barrier compound layer made of a nitrogen-oxygen-titanium-silicon compound is formed below the SiO2 film in the range of about 8 nm.

When the SiO2 film near the surface is excluded, a peak of oxygen concentration is found in the

GF Exhibit 1124 - 1516/2704

vicinity of the surface, and a peak of nitrogen concentration is found at a depth of about 4-5 nm below the SiO2 film.

[0065]
The bonding state between the elements in the barrier compound layer 14 could not be analyzed because the reaction layer was thin, but the standard heats of formation of TiN, TiO2, Si3 N4 and SiO2 were -73.0 kcal in order. / Mol, -218.0 kcal / mol, -179.3, and -202.5 kcal / mol, oxygen is bonded to titanium and silicon when the titanium silicide film is used as in the present embodiment. It is considered that nitrogen is mainly bonded to silicon.

[0066]

As a result of forming the barrier compound layer 14, the sheet resistance increased from 2.6Ω / □ to 2.9Ω / □, but the increase rate was about 10%, which is sufficiently low that there is no particular problem in transistor operation or the like. It is a value.

In the present embodiment, since the barrier compound layer 14 made of the nitrogen-oxygen-titanium-silicon compound is formed only on the surface of the titanium silicide film in the connection hole 8, the sheet of titanium silicide 6 obtained by the above-mentioned nitrogen plasma treatment is used. The rate of resistance increase is even smaller.

[0067]

FIG. 10 shows a sample shown in FIG. 1C that is not subjected to the nitrogen plasma treatment, a sample that has been subjected to the treatment of the present embodiment, and a reference sample that is manufactured by the conventional method shown in FIG. 15 (from a TiN / Ti film). FIG. 3 is a diagram comparing the junction leak characteristics of samples having a barrier metal that does not perform high temperature sputtering.

However, the junction leakage characteristics are shown when a reverse voltage of 5.5 V is applied to the N + P junction having an area of 8000 μm 2.

As shown in the figure, the junction leak is large in the sample which is not subjected to the

GF Exhibit 1124 - 1517/2704

nitrogen plasma treatment.

In the process shown in FIG. 1D, the aluminum alloy film 16 or the Al—Ti compound layer 15 reacts with the titanium silicide film 6 when the aluminum alloy is sputtered at 500 ° C. It is probable that aluminum invaded into the structure and caused a junction leak.

On the other hand, the junction leak of the sample subjected to the nitrogen plasma treatment according to the present embodiment is equivalent to the junction leak of the reference sample which has the barrier metal and does not perform high-temperature sputtering despite having no barrier metal. I know there is.

It is considered that this is because the barrier compound layer 14 prevents the aluminum alloy film 16 or the Al—Ti compound layer 15 from reacting with the titanium silicide film 6 when the aluminum alloy is sputtered at 500 ° C.

[0068]

Further, the contact resistance to the N + diffusion region in this embodiment is 15Ω for the sample having a contact shape of 1.0 μm square and subjected to the nitrogen plasma treatment, and the contact resistance of the reference sample is 5Ω.

Although the contact resistance of the sample according to this embodiment is slightly high, it is understood that no particular trouble occurs in the operation of the transistor and the electrical connection with the silicon substrate is sufficient.

[0069]

FIG. 11 is a diagram showing the annealing temperature dependence of the sheet resistance of various samples that have been subjected to a nitrogen plasma treatment and then deposited with an Al alloy and annealed.

The processing conditions are as follows. After performing the nitrogen plasma treatment shown

GF Exhibit 1124 - 1518/2704

in FIG. 1C on the titanium silicide film having a thickness of 70 nm and further depositing an Al-1% Si-0.5% Cu alloy by a thickness of 200 nm, Annealed for 30 minutes.

The samples were those that were not subjected to nitrogen plasma treatment, those that were subjected to nitrogen plasma treatment for 20 seconds, those that were subjected to nitrogen plasma treatment for 60 seconds, and those that were subjected to nitrogen plasma treatment for 300 seconds. is there.

As shown in the figure, it can be seen that the increase in the sheet resistance when annealed at 530 ° C. is suppressed between the nitrogen plasma treatment for 60 seconds and the nitrogen plasma treatment for 300 seconds.

This figure also shows that the barrier compound layer formed of the nitrogen-oxygen-titanium-silicon compound formed on the surface of the titanium silicide film has an effect of suppressing the reaction between the aluminum alloy and the titanium silicide film.

[0070]

As described above, according to the present embodiment, the surface of the metal silicide is subjected to the nitrogen plasma treatment to form the barrier compound layer including the nitrogen-oxygen-metal-silicon compound on the surface of the metal silicide film. Therefore, it is possible to effectively prevent the metal generated by the reaction between the metal silicide film and the aluminum alloy from entering the silicon substrate by the heat treatment in the subsequent process.

That is, it is possible to suppress the occurrence of a junction leak without interposing a barrier metal such as a titanium nitride / nitride film between the buried layer made of an aluminum alloy film and the metal silicide as in the conventional method.

Therefore, it is possible to prevent the reliability of the buried layer from being deteriorated as in the case where the barrier metal is provided.

Moreover, the contact resistance can be suppressed to a sufficiently low level for practical use,

GF Exhibit 1124 - 1519/2704

and the sheet resistance of the metal silicide film itself can be kept to a sufficiently low level.

[0071]
Further, even when the barrier compound layer is formed in the region near the surface of the metal silicide film on the gate electrode 5, it is possible to prevent the metal from entering the gate electrode, which effectively prevents the deterioration of the characteristics of the gate oxide film. Can be blocked.

[0072]
In particular, in this embodiment, since the nitrogen plasma treatment is performed at a low temperature of 550 ° C. or less, aggregation of the metal silicide film does not occur for many kinds of metal silicide, that is, the metal material forming the metal silicide. There is an advantage that the range of selection can be expanded.

[0073]

(Second Embodiment) Next, the second embodiment will be described.

In the present embodiment, although illustration of the manufacturing process is omitted, after performing the same processing as in FIGS. 1A to 1C in the above-described first embodiment, the inside of the connection hole 8 is formed by the selective CVD method. A tungsten film 17 to be a buried layer is deposited.

Then, after depositing the aluminum alloy film 16 on the tungsten film 17 and the insulating film 7, the aluminum alloy film 16 is patterned to form a metal wiring.

[0074]

FIG. 3 is a cross-sectional view showing the structure of the semiconductor device formed according to this embodiment.

In the first embodiment, the embedded layer and the metal wiring are integrally formed by the

GF Exhibit 1124 - 1520/2704

Al—Ti compound layer 15 and the aluminum alloy film 16, but in the present embodiment, the embedded layer is formed by the tungsten film 17. The aluminum alloy film 16 constitutes a metal wiring.

The barrier compound layer 14 made of a nitrogen-oxygen-titanium-silicon compound is formed only on the bottom surface of the connection hole 8 in the titanium silicide film 6 on the source / drain region 4, and the tungsten film 17 and the titanium film are formed. The silicide film 6 is in contact with the barrier compound layer 14.

That is, the semiconductor device of this embodiment is different from the semiconductor device of the first embodiment only in that the buried layer and the metal wiring are made of different materials, and the other parts are the semiconductor of the first embodiment. It has the same structure as the device.

Therefore, basically the same effect as the first embodiment can be exhibited.

[0075]

In addition, in the semiconductor device of this embodiment, since the buried layer is formed of the tungsten film 17, the temperature at which the reaction causing the junction leak of the semiconductor device occurs is higher than that of the aluminum alloy film or the like. In the present embodiment, the barrier compound layer 14 can prevent a junction leak from occurring due to the reaction of titanium silicide and tungsten by the subsequent heat treatment at 600 ° C. or more to cause the metal to enter the silicon substrate. ..

[0076]

(Third Embodiment) Next, a third embodiment will be described. 4A to 4D are cross-sectional views showing the manufacturing process of the semiconductor device of this embodiment.

[0077]

GF Exhibit 1124 - 1521/2704

First, as shown in FIG. 4A, a gate oxide film 3 made of a silicon oxide film and a gate electrode 5 made of a polysilicon film are formed on an active region surrounded by a field oxide film 2 on a silicon substrate 1. Then, a MOS transistor having sidewalls 9 made of a silicon oxide film and source / drain regions 4 made by introducing impurities into the silicon substrate 1 is formed. Then, for example, a titanium film is deposited on the substrate by a sputtering method, heat-treated at 650 ° C., and then the unreacted titanium film is removed with a mixed solution of H 2 SO 4 -H 2 O 2 to remove the source / drain region 4 and the gate electrode. A titanium silicide film 6 having a thickness of about 70 nm is selectively formed only on the film 5. Then, heat treatment is performed at 850 ° C. to reduce the resistance of the titanium silicide film.

[0078]

Next, as shown in FIG. 4B, in a reaction chamber (not shown) of the plasma generator, a plasma generator having an anode 10 and a cathode 11 forming parallel plate electrodes and a DC power supply 18 is used. The semiconductor device is placed on the cathode 11 arranged in the above, and the surface of the titanium silicide film 6 is exposed to plasma of nitrogen-containing gas such as nitrogen gas. Then, as in the first embodiment, oxygen in the natural oxide film formed on the surface of the titanium silicide film 6 is also taken into the titanium silicide film 6, and the entire titanium silicide film 6 is exposed by the plasma of N2 gas. A barrier compound layer 14 made of a nitrogen-oxygen-titanium-silicon compound is formed near the surface.

[0079]

Next, as shown in FIG. 4C, an insulating film 7 having a thickness of about 800 nm is formed on the entire surface of the substrate, and a contact hole reaching the titanium silicide film 6 in the source / drain region 4 is formed in the insulating film 7. Open 8

[0080]

Next, as shown in FIG. 4 (d), after sputtering titanium by a thickness of about 75 nm with a sputtering apparatus, an aluminum alloy containing 1% of silicon and 0.5% of copper is about 900 nm at 500 ° C. The Al—Ti compound layer 15 formed by combining the aluminum alloy and titanium and the aluminum alloy film 16 thereon are formed by sputtering by the thickness of the above.

At this time, the reaction heat between Al and Ti is used to fill the inside of the connection hole 8

GF Exhibit 1124 - 1522/2704

with an aluminum alloy to form a buried layer. Then, the Al—Ti compound layer 15 and the aluminum alloy film 16 are patterned by photolithography to form metal wiring.

[0081]

FIG. 5 shows a sectional structure of a semiconductor device formed by the above-described manufacturing method. That is, a gate oxide film 3, a gate electrode 5 made of a polysilicon film, a source / drain region 4, and a titanium silicide film formed on the source / drain region 4 and the gate electrode 5 on the silicon substrate 1. A MOS transistor including 6 and the sidewall 9 is formed. Then, the barrier compound layer 14 made of a nitrogen-oxygen-titanium-silicon compound is formed on the entire surface of the titanium silicide film 6. A connection hole 8 reaching the titanium silicide film 6 on the source / drain region 4 is formed in the insulation film 7 formed on the substrate. The connection hole 8 is buried in the connection hole 8 and on the insulation film 7. An Al—Ti compound layer 15 and an aluminum alloy film 16 that form a layer and a metal wiring are formed. That is, in the semiconductor device of the first embodiment, the nitrogen-oxygen-titanium-silicon compound is formed only on the surface of the region of the titanium silicide film 6 on the source / drain region 4 which will be the bottom of the contact hole 8. However, in the semiconductor device of this embodiment, the barrier compound layer 14 is formed on the entire surface of the titanium silicide film 6 on the source / drain regions 4 and the gate electrode 5. The point is characteristic.

[0082]

Also in this embodiment, since the barrier compound layer 14 made of the nitrogen-oxygen-titanium-silicon compound is formed in the region near the surface of the titanium silicide film 6, the same effect as that of the first embodiment can be obtained. Be done. In particular, according to the method of the present embodiment, the barrier compound layer 14 is formed not only in the source / drain regions 4 but also in the region near the surface of the titanium silicide film 6 on the gate electrode 5, so that FIG. Even when a contact portion is formed on the gate electrode 5 from a wiring layer different from the Al—Ti compound layer 15 and the aluminum alloy film 16 shown, the contact is made via the barrier compound layer 14 without performing the nitrogen plasma treatment again. There is an advantage that can be done.

[0083]

GF Exhibit 1124 - 1523/2704

Further, before the step shown in FIG. 4D, that is, before the semiconductor device is put into the sputtering apparatus, it is necessary to wet etch the inside of the connection hole 8 with an HF solution to remove the surface oxide layer of the metal silicide. The titanium silicide film 6 is easily etched by the HF solution. In this respect, in the present embodiment, the barrier compound layer 14 made of the nitrogen-oxygen-titanium-silicon compound is considered to have a composition close to SiN because it contains a bond between silicon and nitrogen, and therefore the HF solution is used. It is thought that it is difficult to etch. Therefore, this embodiment also has an advantage that the chemical resistance of the titanium silicide film is improved and the process margin is increased.

[0084]

However, in the semiconductor device of this embodiment, since the barrier compound layer 14 is formed on the entire surface of the titanium silicide film 6, the increase in sheet resistance of the titanium silicide film 6 is larger than that of the semiconductor device of the first embodiment. Become. However, as described in the first embodiment, even in that case, the increase rate of the sheet resistance is about 10%, which is a sufficiently low value that causes no particular problem in the transistor operation and the like.

[0085]

(Fourth Embodiment) Next, a fourth embodiment will be described. In the present embodiment, although illustration of the manufacturing process is omitted, after performing the same processing as in FIGS. 3A to 3C in the above-described third embodiment, the inside of the connection hole 8 is formed by the selective CVD method. A tungsten film 17 to be a buried layer is deposited. Then, after depositing the aluminum alloy film 16 on the tungsten film 17 and the insulating film 7, the aluminum alloy film 16 is patterned to form a metal wiring.

[0086]

FIG. 6 is a cross-sectional view showing the structure of the semiconductor device formed according to this embodiment. In the third embodiment, the embedded layer and the metal wiring are integrally formed by the Al—Ti compound layer 15 and the aluminum alloy film 16, but in the present embodiment, the embedded layer is formed by the tungsten film 17. The aluminum alloy film 16 constitutes a metal wiring. A barrier compound layer 14 made of a

GF Exhibit 1124 - 1524/2704

nitrogen-oxygen-metal-silicon compound is formed on the entire surface of the titanium silicide film 6 on the source / drain regions 4 and the gate electrode 5, and the tungsten film 17 and the titanium silicide film are formed. 6 are in contact with each other via the barrier compound layer 14. That is, the semiconductor device of this embodiment is different from the semiconductor device of the third embodiment only in that the buried layer and the metal wiring are made of different materials, and the other parts are the semiconductor of the third embodiment. It has the same structure as the device. Therefore, basically the same effect as the third embodiment can be obtained.

[0087]

In addition, in the semiconductor device of this embodiment, since the buried layer is composed of the tungsten film 17, the barrier compound layer 17 may prevent the reaction between tungsten and titanium silicide. Therefore, it is possible to prevent a junction leak from occurring due to the reaction of titanium silicide and tungsten with the subsequent heat treatment at 600 ° C. or more to cause the metal to enter the silicon substrate.

[0088]

(Fifth Embodiment) Next, a fifth embodiment will be described. 7A to 7D are cross-sectional views showing the manufacturing process of the semiconductor device of this embodiment.

[0089]

First, as shown in FIG. 7A, a gate oxide film 3 made of a silicon oxide film and a gate electrode 5 made of a polysilicon film are formed on an active region surrounded by a field oxide film 2 on a silicon substrate 1. Then, a MOS transistor having sidewalls 9 made of a silicon oxide film and source / drain regions 4 made by introducing impurities into the silicon substrate 1 is formed. Then, for example, a cobalt film is deposited on the substrate by a sputtering method, heat-treated at 500 ° C. in a nitrogen atmosphere, and then the unreacted cobalt film is removed with a H 2 SO 4 -H 2 O 2 mixed solution to form the source / drain region 4. A cobalt silicide film 24 having a thickness of about 50 nm is selectively formed only on the gate electrode 5 and the gate electrode 5. Then, heat treatment is performed at 850 ° C. to reduce the resistance of the cobalt silicide film 24.

GF Exhibit 1124 - 1525/2704

[0090]

Next, as shown in FIG. 7B, an upper electrode 29 and a lower electrode 26 which form a parallel plate electrode, a high pass filter 27, a low pass filter 28, a 13.56 MHz high frequency power supply 29, and a 400 KHz high frequency. A semiconductor device is placed on a lower electrode 26 arranged in a reaction chamber (not shown) of the plasma generator using a plasma generator having a power supply 30, and the surface of the cobalt silicide film 24 is replaced with nitrogen gas or the like. Exposed to plasma of nitrogen-containing gas. For example, under a temperature of 400 ° C. and a pressure of 2 Torr, 100% N2 gas is introduced, and a high frequency power of 29 W is applied to the upper electrode 25 by a high frequency power supply 29, and a high frequency power of 100 W is applied to the lower electrode 26 of a high frequency power supply of 900 W for 900 sec. Apply for a period of time. At this time, nitrogen plasma Plz is generated in the reaction chamber. Nitrogen in the nitrogen plasma Plz is positive ions such as N + and N2 +, and the lower electrode 26 has a lower frequency. Therefore, nitrogen ions are attracted toward the lower electrode 25. That is, even if a plasma generator of dual frequency power addition type is used, the introduction of nitrogen to the surface of the cobalt silicide film 24 is promoted by installing the semiconductor device on the electrode to which the low frequency power is applied. Will be done. At this time, oxygen in the natural oxide layer formed on the surface of the cobalt silicide film 24 or oxygen remaining in the chamber is also taken into the cobalt silicide layer 24, and is a barrier composed of a nitrogen-oxygen-cobalt-silicon compound. The compound layer 14 is formed near the surface of the cobalt silicide film 24.

[0091]

Next, as shown in FIG. 7C, the first aluminum film 22 is formed only on the barrier compound layer 14 by the selective CVD method using DMAH (dimethyl aluminum hydride). The selective CVD method using DMAH is a method capable of selectively depositing an aluminum film only on a conductive layer.

[0092]

Next, as shown in FIG. 7D, an insulating film 7 having a thickness of about 800 nm is formed on the first aluminum film 22, and the first aluminum film on the source / drain region 4 is formed on the insulating film 7. The connection hole 8 reaching 22 is opened.

GF Exhibit 1124 - 1526/2704

[0093]

Next, as shown in FIG. 7E, the second aluminum film 23 is formed in the connection hole 8 by the selective CVD method using DMAH.

Further, the aluminum alloy film 16 is deposited on the second aluminum film 23 and the insulating film 7 by the sputtering method, and the aluminum alloy film 16 is patterned by the photolithography method to form the metal wiring.

[0094]

FIG. 8 shows a cross-sectional structure of a semiconductor device formed by the above manufacturing method. That is, a gate oxide film 3, a gate electrode 5 made of a polysilicon film, a source / drain region 4, and a cobalt silicide film 24 formed on the source / drain region 4 and the gate electrode 5 on the silicon substrate 1. , Sidewalls 9 are formed. Then, the barrier compound layer 14 made of a nitrogen-oxygen-cobalt-silicon compound is formed on the entire surface of the cobalt silicide film 24, and the first aluminum film 22 is further formed on the barrier compound layer 14 of the cobalt silicide film 24. Has been done. A connection hole 8 reaching the first aluminum film 22 on the source / drain region 4 is formed in the insulating film 7 formed on the substrate, and the connection hole 8 has a first hole as a buried layer. 2 aluminum film 23 is formed. Further, the aluminum alloy film 16 forming the metal wiring is formed on the second aluminum film 23 and the insulating film 7. That is, in the semiconductor device of this embodiment, the barrier compound layer 14 is formed on the entire surface of the cobalt silicide film 24 on the source / drain regions 4 and the gate electrode 5, and the cobalt silicide film 24 is electrically connected to the barrier compound layer 14. The feature is that an aluminum film (low resistance layer) having a low resistance is formed.

[0095]
Next, details of the structure of the barrier compound layer 14 of the semiconductor device obtained in the present embodiment and details of the reaction prevention effect of the first aluminum film 22 in the semiconductor device of the present embodiment will be described.

[0096]

GF Exhibit 1124 - 1527/2704

FIGS. 12A to 12C show a cobalt silicide film which is not plasma-treated, a cobalt silicide film which is plasma-treated in N2 gas, and a cobalt silicide film which is plasma-treated in NH3 gas. It is a figure which shows the concentration profile of each element obtained as a result of having analyzed the area ¦ region by the XPS method.

However, in FIGS. 12A to 12C, the horizontal axis represents the depth from the surface, and the vertical axis represents the composition ratio of each element. Even in the cobalt silicide film which is not plasma-treated, since the heat treatment is performed at 750 ° C. in the nitrogen atmosphere during the formation of the silicide, nitrogen is introduced near the surface, but the peak of the nitrogen concentration is at the surface position, The nitrogen concentration decreased and nitrogen was lost at a depth of about 2 nm. Also, the oxygen concentration is so small that it can be almost ignored at a depth of about 2 nm. On the other hand, in the cobalt silicide film plasma-processed in N2 gas or NH3 gas, a peak of nitrogen concentration is found at a depth of about 2 nm from the surface. In addition, the region where the oxygen concentration is high extends to a depth position of about 6 nm from the surface. That is, in the cobalt silicide film subjected to the plasma treatment in the nitrogen atmosphere, the barrier compound layer made of the nitrogen-oxygen-cobalt-silicon compound is formed from the surface to a depth position of about 6 nm. I understand.

[0097]
In the present embodiment, as a result of forming the barrier compound layer 14 near the surface of the cobalt silicide film 24, the electric resistance of the cobalt silicide film 24 increased from 3.5Ω / □ to 3.6Ω / □, but the increase rate is It is 10% or less, which is a sufficiently low value that does not cause any particular problem in the operation of the transistor.

[0098]

FIG. 13 shows the annealing temperature dependence of the sheet resistance of various samples obtained by depositing an Al-0.5% Cu film as the first aluminum film 22 on the cobalt silicide film and performing annealing treatment. It is a diagram, and there are two types of cobalt silicide films that have been plasma-treated in N2 gas for 900 seconds, those that have been plasma-treated in NH3 gas for 900 seconds, and those that have not been plasma-treated.

The plasma treatment was performed by irradiating a cobalt silicide film having a thickness of 50 nm with nitrogen plasma in N2 gas or NH3 gas for 900 seconds. Then, in each of the samples, an Al-0.5% Cu alloy film was deposited to a thickness of about 200 nm on the cobalt silicide film,

GF Exhibit 1124 - 1528/2704

and then annealed for about 30 minutes.

[0099]

As can be seen from the figure, in the sample not subjected to the plasma treatment, the sheet resistance value when annealed at 400 ° C does not increase so much, but the sheet resistance value when annealed at 430 ° C significantly increases. is doing. On the other hand, in each of the plasma-treated samples, the increase in resistance value is suppressed even if they are annealed at 400 ° C and 430 ° C. That is, it is understood that the barrier compound layer formed on the surface of the cobalt silicide film suppresses the reaction between the aluminum film and the cobalt silicide film. Generally, since sintering is performed at about 400 to 450 ° C., such an effect of suppressing the sheet resistance value is of significant significance in practical use.

[0100]

Further, as a result of XPS analysis of the sample annealed at 430 ° C., those not treated with nitrogen plasma showed that Co2 Al1 9 or Co4 Al3 alloy was formed, whereas the sample treated with nitrogen plasma showed Al. Only the CoSi2 peak was seen. That is, it was found from the X-ray analysis that the reaction between Al and CoSi2 was suppressed up to 430 ° C by the nitrogen plasma treatment.

[0101]

As described above, according to this embodiment, the surface of the metal silicide is subjected to the nitrogen plasma treatment to form the barrier compound layer made of the nitrogen-oxygen-metal-silicon compound on the surface of the metal silicide film. Therefore, the heat treatment in the subsequent steps can effectively prevent the metal generated by the reaction between the metal silicide film and the aluminum alloy from entering the silicon substrate. In other words, unlike the conventional method, it is not necessary to apply a heat treatment at 800 ° C. or higher to the silicide film to form the barrier compound layer, so that boron in the source / drain regions is absorbed in the metal silicide film and the P-channel transistor There is no problem that the saturation current value decreases. Further, since the nitrogen plasma treatment is performed at a low temperature of 550 ° C. or lower, it is possible to obtain an effect that the metal silicide film does not aggregate even for many kinds of metal silicide. That is, it is possible

GF Exhibit 1124 - 1529/2704

to increase the range of selection of the metal material forming the metal silicide.

[0102]

(Other Embodiments) In the first or third embodiment, the metal wiring on the connection hole 8 is formed from the aluminum alloy film 16 and the Al—Ti compound layer 15, but the Al—Ti compound layer 15 is It may be another metal film or its compound, or may not be provided. Further, another metal film may be laminated on the aluminum alloy film 16. Further, although the aluminum alloy containing silicon and copper is used as the aluminum alloy film 16, other aluminum alloy containing only metal such as silicon or scandium, or pure aluminum may be used. Further, copper or a copper alloy may be used instead of the aluminum alloy.

[0103]

In each of the above embodiments, N2 gas was used as the gas containing nitrogen. First, NH3 gas or H2 gas was flowed to remove the natural oxide film on the surface of the metal silicide film, and then a small amount of O2 gas was added to the N2 gas. Plasma may be generated in an atmosphere to which is added to form a barrier compound layer composed of a nitrogen-oxygen-titanium-silicon compound. In that case, since the amount of oxygen can be controlled, the distribution of each element in the barrier compound layer can be made as close as possible to the optimum state, and the barrier having a lower contact resistance and a higher junction leak prevention effect than using a natural oxide film A semiconductor device having a compound layer can be formed.

[0104]

Even when the plasma treatment is performed using NH3 gas, by performing the plasma treatment at 550 ° C or lower, it is possible to perform the plasma treatment under the conventional conditions of about 800 ° C to form titanium nitride. No trouble will occur. Further, even when performing plasma treatment using NH3 gas, under the condition that a barrier compound layer made of a metal-silicon compound such as nitrogen-oxygen-titanium can be formed by utilizing a natural oxide film. It is possible to exert the effect of the present invention.

GF Exhibit 1124 - 1530/2704

[0105]

FIG. 14 is a TEM photograph showing the barrier compound layer formed on the surface of the silicide when the surface of the cobalt silicide is plasma-treated using NH3 gas. The plasma generation conditions are the same as the N2 gas plasma generation conditions described in the fifth embodiment. It can be seen that a nitrogen-oxygen-cobalt-silicon compound layer (amorphous layer) having a thickness of about 4-6 nm is formed. Further, as shown in the data of FIG. 13 already described, the increase of the sheet resistance due to the reaction between aluminum and cobalt silicide during the heat treatment is suppressed up to 430 ° C., which is about the same as when using N 2 gas. It can be seen that there is an effect of suppressing the reaction. The reason is that, as shown in FIG. 12 already described, when NH3 gas is used, the composition ratio of oxygen in the nitrogen-oxygen-cobalt-silicon compound layer is reduced and the composition ratio of nitrogen is increased. It is presumed that the composition ratio of the two is adjusted appropriately.

[0106]

Needless to say, as the conditions for plasma formation, conditions other than the conditions in the above embodiments can be used.

[0107]

In each of the above-described embodiments, the step of forming the nitrogen-oxygen-silicon compound layer by subjecting the surface of the titanium silicide film or the cobalt silicide film to nitrogen plasma treatment is performed in a sputtering device or a selective CVD device by using copper in the connection hole, It may be performed in the same apparatus immediately before depositing aluminum, tungsten or an alloy thereof, or in the same apparatus immediately before forming copper, aluminum, tungsten or an alloy thereof only on the barrier compound layer by the selective CVD method. You may go in.

[0108]

Although titanium silicide is used as the metal silicide film in each of the above embodiments, cobalt silicide, nickel silicide, tantalum silicide, tungsten silicide, niobium silicide, palladium silicide, platinum silicide, molybdenum silicide, or the like may be used.

[0109]

GF Exhibit 1124 - 1531/2704

Further, in each of the above-described embodiments, in the step of forming the barrier compound layer composed of the nitrogen-oxygen-metal-silicon compound, instead of exposing the surface of the metal silicide film to plasma of a gas containing nitrogen, the surface of the metal silicide film is Of the nitrogen-oxygen-metal-silicon on the surface of the metal silicide film at a low temperature of 550 ° C. or lower by exposing the material to a gas containing nitrogen and irradiating it with ultraviolet rays or ionizing radiation at the same time by using energy such as ultraviolet rays. You may form the barrier compound layer which consists of an intermetallic compound.

Alternatively, instead of using plasma, by exposing the surface of the metal silicide film to an ion beam containing nitrogen, the energy of the ions is used to remove nitrogen-on the surface of the metal silicide film at a low temperature of 550 ° C. or lower. A barrier compound layer made of an oxygen-metal-silicon compound may be formed.

[0110]

In the first to fourth embodiments, in the step of forming the barrier compound layer made of the nitrogen-oxygen-metal-silicon compound, any one of plasma treatment, irradiation with ultraviolet rays, irradiation with ion beam, etc. is selected. Also in this case, the potential for attracting nitrogen ions to the metal silicide side is preferably about 3 keV or less.

The reason will be described.

By analogy with the range of nitrogen ions in silicon, when the potential is 1 keV, the nitrogen concentration in silicon peaks at a depth of 3.8 nm and reaches 10 at a depth of 9.8 nm. Reduce to%. When the potential is 3 keV, the nitrogen concentration in silicon reaches a peak at a depth of 8.5 nm and decreases to 10% at a depth of 20.3 nm. Therefore, by suppressing the formation of the barrier compound layer to a depth of about 20 nm, which corresponds to 30% of the silicide film having a thickness of about 70 nm, it is possible to avoid an increase in sheet resistance and contact resistance.

[0111]

Further, the metal silicide film on which the barrier compound layer of the present invention is

GF Exhibit 1124 - 1532/2704

formed is not limited to the gate electrode and the source / drain regions shown in the above embodiments. For example, when the polysilicon film is used as a component (particularly an electrode) of a resistor or a capacitor, a silicide film on the polysilicon film may be formed, and even in that case, a metal silicide that contacts the upper wiring By forming the barrier compound layer of the nitrogen-oxygen-metal-silicon compound of the present invention on the surface of the film, the reaction between the buried layer and the metal silicide layer is achieved without depositing the barrier metal in the connection hole. There is an advantage that it is possible to effectively prevent the metal or the like generated in step 2 from entering the electrode or other members through the electrode.

[0112]

In the fifth embodiment, the barrier compound layer 14 made of a nitrogen-oxygen-metal-silicon compound is formed on the entire surface of the cobalt silicide film 24 on the source / drain regions 4 and the gate electrode 5. The first aluminum film 22 and the titanium silicide film 6 are in contact with each other via the barrier compound layer 14, but instead of the first aluminum film 22, a metal containing aluminum, a metal containing copper and tungsten are contained. The same effect is obtained when a metal film is deposited. For example, even when a tungsten film is used instead of the first aluminum film 22, the presence of the barrier compound layer 14 causes the cobalt silicide and tungsten to react with each other in the subsequent heat treatment at 600 ° C. or higher, so that the metal in the silicon substrate is reacted. Can be effectively prevented from entering and causing a junction leak.

[0113]

As described above, according to the present invention, the metal silicide film and the upper wiring are electrically connected via the buried layer in the connection hole formed in the insulating film on the metal silicide. In the semiconductor device described above, since the barrier compound layer made of the nitrogen-oxygen-metal-silicon compound is formed at least in the region near the surface of the metal silicide film that becomes the bottom surface of the connection hole, the barrier metal layer is formed in the connection hole. The compound can be prevented from entering the semiconductor substrate or the like without lowering the reliability due to the deposition of the metal, and thus the sheet resistance value of the entire metal silicide film can be kept low and the junction leakage can be suppressed. At the same time, it is possible to provide a semiconductor device having a highly reliable buried layer in the connection hole and a method for manufacturing the same.

[0114]

GF Exhibit 1124 - 1533/2704

Brief description of the drawings

[0115]
1 is a cross-sectional view showing a manufacturing process of the semiconductor device in the first embodiment.

[0116]
2 is a cross-sectional view of the semiconductor device in the first embodiment.

[0117]
3 is a cross-sectional view of the semiconductor device in the second embodiment.

[0118]
4 is a cross-sectional view showing a manufacturing process of the semiconductor device in the third embodiment.

[0119]
5 is a cross-sectional view of a semiconductor device in the third embodiment.

[0120]
6 is a cross-sectional view of a semiconductor device according to the fourth embodiment.

[0121]
7 is a cross-sectional view showing the manufacturing process of the semiconductor device in the fifth embodiment.

[0122]
8 is a cross-sectional view of a semiconductor device according to the fifth embodiment.

[0123]
<Figure 9> It is the figure which shows the elemental analysis result of the depth direction of the titanium silicide film surface of the semiconductor device in 1st execution form.

GF Exhibit 1124 - 1534/2704

[0124]
10 is a diagram comparing the junction leakage characteristics of the sample not subjected to the nitrogen plasma treatment, the sample subjected to the treatment of the first embodiment, and the reference sample.

[0125]
11 is a diagram showing the annealing temperature dependence of the sheet resistance of various samples annealed by depositing an Al alloy after performing the nitrogen plasma treatment.

[0126]
Fig. 12 XPS analysis of the vicinity of the surface of the CoSi2 film when plasma nitriding was not performed, plasma nitriding was performed in an N2 gas atmosphere, and plasma nitriding was performed in an NH3 gas atmosphere. It is a figure which shows each composition ratio.

[0127]
FIG. 13 is a diagram showing the temperature dependence of the sheet resistance of the AlCu / CoSi2 structure when plasma nitriding is not performed, when plasma nitriding is performed in an N2 gas atmosphere, and when plasma nitriding is performed in an NH3 gas atmosphere. ..

[0128]
14 is a TEM photograph near the boundary of the AlCu / CoSi2 structure when plasma nitriding is performed in an NH3 gas atmosphere.

[0129]
15 is a cross-sectional view showing a manufacturing process of a conventional semiconductor device.

[0130]
Explanation of symbols

[0131]

GF Exhibit 1124 - 1535/2704

1 Silicon Substrate 2 Field Oxide Film 3 Gate Oxide Film 4 Source / Drain Region 5 Gate Electrode 6 Titanium Silicide Film 7 Insulating Film 8 Connection Hole 9 Sidewall 10 Anode 11 Cathode 12 Blocking Capacitor 13 High Frequency Power Supply 14 Barrier Compound Layer 15 Al-Ti Compound layer 16 Aluminum alloy film 17 Tungsten film 18 DC power supply Plz Nitrogen plasma 22 First aluminum film 23 Second aluminum film 24 Cobalt silicide film 25 Upper electrode 26 Lower electrode 27 High-pass filter 28 Low-pass filter 29 High-frequency power supply 30 High-frequency power supply 30

GF Exhibit 1124 - 1536/2704

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

CLAIMS JPH09289178

1.
A semiconductor substrate, a metal silicide film formed on a part of the semiconductor substrate by siliciding the first metal, a metal film formed of a second metal on the metal silicide film, and the metal A semiconductor device, comprising: a barrier compound layer formed in a region near the surface of a silicide film and made of a nitrogen-oxygen-first metal-silicon compound.

2.
The semiconductor device according to claim 1, wherein the barrier compound layer is formed in a region near the surface of the entire metal silicide film.

3.
3. The semiconductor device according to claim 1, wherein the thickness of the barrier compound layer is at least a thickness sufficient to prevent the diffusion of the second metal into the barrier compound layer, and is 30 times the thickness of the metal silicide film. % Or less, a semiconductor device.

4.
The semiconductor device according to claim 1, wherein the barrier compound layer has a thickness in the range of 2 to 20 nm.

5.

GF Exhibit 1124 - 1537/2704

The semiconductor device according to claim 1, 2, or 3, wherein the position where the concentration of nitrogen is maximum in the barrier compound layer is deeper than the position where the concentration of oxygen is maximum. apparatus.

6.

The semiconductor device according to claim 1, further comprising: an insulating film formed on the metal silicide film; and a connection hole formed in a part of the insulating film and reaching the metal silicide film, wherein the metal film is A buried layer made of the second metal deposited in the connection hole.

7.

2. The semiconductor device according to claim 1, wherein an insulating film formed on the metal silicide film, a connection hole formed in a part of the insulating film and reaching the metal silicide film, and deposited in the connection hole. And a buried layer made of a third metal.

8.

The semiconductor device according to claim 1, 2, 3, 4, 5, 6 or 7, wherein the first metal is any one of titanium, cobalt, nickel, tantalum, tungsten, niobium, palladium, platinum and molybdenum. A semiconductor device characterized in that

9.

The semiconductor device according to claim 1, 2, 3, 4, 5, 6 or 7, wherein the second metal is any one of a metal containing aluminum, a metal containing copper and a metal containing tungsten. A semiconductor device characterized by the above.

10.

A first step of forming a metal silicide film made of a compound of a first metal and silicon on a semiconductor substrate, and irradiating the surface of the metal silicide film with ions containing nitrogen in a neutral or oxidizing atmosphere. Then, a second step of forming a barrier compound layer made of a nitrogen-oxygen-first metal-silicon compound in a region near the surface of the metal silicide film, and a step of forming a barrier compound layer of the metal silicide film on the barrier compound layer. And a third step of depositing a second metal to form a metal film.

GF Exhibit 1124 - 1538/2704

11.

11. The method for manufacturing a semiconductor device according to claim 10, wherein an insulating film is formed on the metal silicide film after the first step and before the second step, A step of selectively removing a portion to form a connection hole reaching the metal silicide film, and in the second step, a bottom portion of the connection hole in a region near the surface of the metal silicide film is formed. A method of manufacturing a semiconductor device, comprising forming the barrier compound layer in an exposed region, and filling the inside of the connection hole with the second metal in the third step.

12.

11. The method of manufacturing a semiconductor device according to claim 10, wherein after the second step, a step of forming an insulating film on the barrier compound layer of the metal silicide film, and a part of the insulating film are selectively formed. And a step of forming a connection hole that reaches the barrier compound layer by removing the second metal in the connection hole in the third step. Production method.

13.

13. The method of manufacturing a semiconductor device according to claim 12, wherein after the third step, a step of forming an insulating film on the barrier compound layer of the metal silicide film, and a part of the insulating film are selectively formed. And a step of forming a contact hole that reaches the barrier compound layer by removing the second metal, and a step of depositing a third metal in the contact hole to form a buried layer. Method of manufacturing semiconductor device.

14.

14. The method of manufacturing a semiconductor device according to claim 10, 11, 12 or 13, wherein in the second step, a plasma generating device in which a lower electrode as a cathode and an upper electrode as an anode are arranged in a chamber, In the chamber, the barrier compound layer is formed by exposing the metal silicide film to plasma of a gas containing nitrogen while the semiconductor substrate is placed on the lower electrode. Method.

15.

14. The method of manufacturing a semiconductor device according to claim 10, 11, 12, or 13, wherein in the second step, one of ultraviolet rays and ionizing radiation is exposed while exposing the surface of the metal silicide film to a gas containing nitrogen. A method for manufacturing a semiconductor device, which comprises forming the barrier compound layer by irradiation.

GF Exhibit 1124 - 1539/2704

16.

14. The method of manufacturing a semiconductor device according to claim 10, 11, 12 or 13, wherein in the second step, the barrier compound layer is formed by exposing the surface of the metal silicide film to an ion beam containing nitrogen. A method of manufacturing a semiconductor device, comprising:

17.

A method of manufacturing a semiconductor device according to claim 10, 11, 12, 13, 14, 15 or 16, wherein the second step is performed at 550 ° C or lower.

18.

A method of manufacturing a semiconductor device according to claim 10, 11, 12, 13, 14, 15 or 16, wherein in the second step, N2 gas is used as the gas containing nitrogen. Production method.

19.

A method of manufacturing a semiconductor device according to claim 10, 11, 12, 13, 14, 15, 16, 17 or 18, wherein the metal silicide is obtained by flowing a gas containing hydrogen before the second step. A method of manufacturing a semiconductor device, further comprising a step of removing a natural oxide film on the film, wherein a gas containing oxygen is added in the second step.

20.

17. The method for manufacturing a semiconductor device according to claim 10, 11, 12, 13, 14, 15 or 16, wherein in the second step, ions containing nitrogen are introduced into the metal silicide film at an ion energy of 3 keV or less. A method of manufacturing a semiconductor device, comprising:

21.

21. A method of manufacturing a semiconductor device according to claim 10, 11, 12, 13, 14, 15, 16, 17, 18, 19 or 20, wherein titanium, cobalt, nickel is used as the metal silicide film in the first step. And tantalum, tungsten, palladium, platinum, and molybdenum, a silicide film is formed.

GF Exhibit 1124 - 1540/2704

22.

A method of manufacturing a semiconductor device according to claim 10, 11, 12, 13, 14, 15, 16, 17, 18, 19 or 20, wherein in the third step, a metal containing aluminum using a CVD method, A method of manufacturing a semiconductor device, comprising depositing one of a metal containing copper and a metal containing tungsten.

23.

A method of manufacturing a semiconductor device according to claim 10, 11, 12, 13, 14, 15, 15, 16, 17, 18, 19 or 20, wherein in the third step, titanium and aluminum alloys are continuously sputtered. Thus, the method for manufacturing a semiconductor device is characterized in that the metal film is composed of an Al—Ti compound layer and an aluminum alloy film.

GF Exhibit 1124 - 1541/2704

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報**（Ａ）　(11)特許出願公開番号

特開平10－135452

(43)公開日　平成10年(1998)５月22日

(51)Int.Cl.[6]	識別記号	ＦＩ	
Ｈ０１Ｌ　29/78		Ｈ０１Ｌ　29/78	３０１Ｃ

審査請求　未請求　請求項の数26　ＯＬ　（全　９　頁）

(21)出願番号　特願平9－293730

(22)出願日　平成９年(1997)10月27日

(31)優先権主張番号　０８／７３９７６５

(32)優先日　1996年10月30日

(33)優先権主張国　米国（ＵＳ）

(71)出願人　390009531
インターナショナル・ビジネス・マシーンズ・コーポレイション
ＩＮＴＥＲＮＡＴＩＯＮＡＬ　ＢＵＳＩＮＥＳＳ　ＭＡＳＣＨＩＮＥＳ　ＣＯＲＰＯＲＡＴＩＯＮ
アメリカ合衆国10504、ニューヨーク州　アーモンク　（番地なし）

(72)発明者　ダグラス・アンドリュー・ブカナン
アメリカ合衆国10566　ニューヨーク州　コートランド　マナ　イースト　コーズウェイ　10

(74)代理人　弁理士　坂口　博　（外１名）

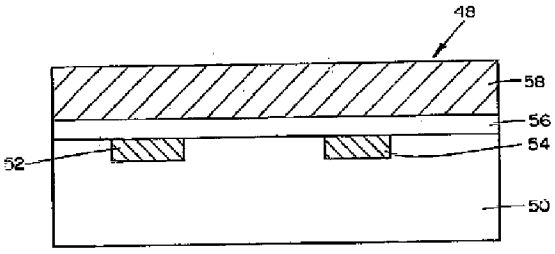
最終頁に続く

(54)【発明の名称】　中間ギャップ作業関数タングステン・ゲートの製造方法

(57)【要約】

【課題】高速・高密度アドバンスト酸化金属半導体（ＭＯＳ）および相補形金属酸化膜半導体（ＣＭＯＳ）デバイスに使用される超薄ゲート誘電体等のゲート誘電体上に対して直接に中間ギャップ仕事関数タングステン（Ｗ）ゲートおよびＷ電極を製造する方法と、該方法によって製造された少なくとも一つのCVDによるＷゲートまたはＷ電極を持つMOSおよびCMOSデバイスを提供する。本発明の方法を量子デバイスに使用可能なＷ電極の製造にも適用可能とする。

【解決手段】中間ギャップ作業関数タングステン・ゲートの製造方法は、（ａ）原料物質として$W(CO)_6$を使用した化学蒸着（CVD）によって、半導体基板上に配置されているゲート誘電体上にタングステン（Ｗ）の層を蒸着する工程と、（ｂ）ゲート誘電体上に中央ギャップ作業関数Ｗゲートを含むMOSデバイスを形成するために、（ａ）の工程で形成された構造をリソグラフィ技術を用いてパターニングする工程とを有する。



GF Exhibit 1124 - 1542/2704

【特許請求の範囲】
【請求項１】金属酸化物半導体（MOS）の応用に使用される中間ギャップ作業関数タングステン・ゲートの製造方法であって、
（ａ）原料物質として$W(CO)_6$を使用した化学蒸着（CVD）によって、半導体基板上に配置されているゲート誘電体上にタングステン（Ｗ）の層を蒸着する工程と、
（ｂ）前記ゲート誘電体上に前記中間ギャップ作業関数Ｗゲートを含むMOSデバイスを形成するために、前記（ａ）の工程で形成された構造をリソグラフィ技術を用いてパターニングする工程とを有する中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項２】前記ゲート誘電体は、厚さが4.0nm未満である超薄ゲート誘電体であることを特徴とする請求項１に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項３】前記超薄ゲート誘電体は、厚さが３nm未満であることを特徴とする請求項２に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項４】前記超薄ゲート誘電体は、SiO_2 窒化SiO_2 Si_3N_4、金属酸化物、およびこれらの混合物からなる群から選択されることを特徴とする請求項３に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項５】前記超薄ゲート誘電体は、SiO_2であることを特徴とする請求項４に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項６】前記半導体基板は、少なくとも一つのソース領域と少なくとも一つのドレイン領域とを備えることを特徴とする請求項１に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項７】前記半導体基板は、ｐ型の半導体基板またはｎ型の半導体基板であることを特徴とする請求項１に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項８】前記半導体基板は、シリコン、SiGe、またはGaAsからなることを特徴とする請求項１に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項９】前記半導体基板は、シリコンからなることを特徴とする請求項１に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項１０】前記化学蒸着（CVD）を行う工程は、250℃から500℃までの温度範囲で実施されることを特徴とする請求項１に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項１１】前記化学蒸着（CVD）を行う工程は、275℃から500℃までの温度範囲で実施されることを特徴とする請求項１０に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項１２】前記化学蒸着（CVD）を行う工程は、$1x10^{-6}$Torrから$3x10^{-4}$Torrまでの圧力範囲で実施されることを特徴とする請求項１に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項１３】前記化学蒸着（CVD）を行う工程は、$1x10^{-4}$Torrから$2x10^{-4}$Torrまでの圧力範囲で実施されることを特徴とする請求項１２に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項１４】前記化学蒸着（CVD）を行う工程によって得られる前記タングステンの層は、厚さが3.5nmから200nmまでの範囲にあることを特徴とする請求項１に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項１５】前記タングステンの層は、厚さが50nmから100nmまでの範囲にあることを特徴とする請求項１４に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項１６】前記パターニングを行う工程は、
前記タングステンの層の所定の領域上に少なくとも一つのフォトレジストを配置する工程と、
前記フォトレジストを現像する工程と、
前記フォトレジストが含まれない前記タングステンの層の領域をエッチングする工程とからなることを特徴とする請求項１に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項１７】前記エッチングの工程は、ウエット・エッチングまたはドライ・エッチングからなることを特徴とする請求項１６に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項１８】前記ウエット・エッチングは、H_2O_2、リン酸、クロム酸、硝酸、およびこれらの混合物からなる群から選択される化学エッチング剤を用いて行われることを特徴とする請求項１７に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項１９】前記化学エッチング剤は、H_2O_2であることを特徴とする請求項１８に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項２０】前記ドライ・エッチングとして、反応性イオン・エッチング（RIE）、イオン・ビーム・エッチング（IBE）、およびレーザ切除によるエッチングが挙げられることを特徴とする請求項１７に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項２１】MOSウエハを設ける工程をさらに含み、また前記MOSウエハは、少なくとも一つのソース領域と少なくとも一つのドレイン領域とを有するｐ型半導体基板またはｎ型半導体基板であり、さらに該ｐ型半導体基板またはｎ型半導体基板上に誘電体が配置されていることを特徴とする請求項１に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項２２】タングステン電極を製造する方法であって、
（ａ）原料材料として$W(CO)_6$を用いる化学蒸着（CV

GF Exhibit 1124 - 1543/2704

D）によって、誘電体をタングステンの層に蒸着する工程と、
（ｂ）前記誘電体上にタングステン電極を形成するために、前記タングステンの層をパターニングする工程とを有することを特徴とするタングステン電極の製造方法。
【請求項２３】ゲート誘電体上に少なくとも一つの中間ギャップ作業関数タングステン・ゲートを有するMOSデバイスであって、
前記中間ギャップ作業関数タングステン・ゲートは、請求項１に記載の方法によって形成されることを特徴とするMOSデバイス。
【請求項２４】前記ゲート誘電体は、厚さが4.0nm未満である超薄ゲート誘電体であることを特徴とする請求項２３に記載のMOSデバイス。
【請求項２５】ゲート誘電体上に少なくとも一つの中間ギャップ作業関数タングステン・ゲートを有する電界効果トランジスタ（FET）であって、
前記中間ギャップ作業関数タングステン・ゲートは、請求項１に記載の方法によって形成されることを特徴とする電界効果トランジスタ。
【請求項２６】前記ゲート誘電体は、厚さが4.0nm未満である超薄ゲート誘電体であることを特徴とする請求項２５に記載の電界効果トランジスタ。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、高速・高密度アドバンスト酸化金属半導体（MOS）および相補形金属酸化膜半導体（CMOS）デバイスに使用される超薄ゲート誘電体等のゲート誘電体上に直接に中間ギャップ仕事関数（mid-gap workfuncition）タングステン（W）ゲートを製造する方法に関する。特に、本発明の中間ギャップ仕事関数Wゲートは、六塩化タングステン（以下、$W(CO)_6$とする）を原料物質として用いる低温・低圧化学蒸着法によって直接にゲート誘電体上に製造する。本発明の方法を量子デバイスに使用可能なW電極の製造にも適用することができる。
【０００２】本発明は、電界効果トランジスタ（FET）やゲート誘電体上に、本発明の方法によって製造される少なくとも一つの中間ギャップ仕事関数Wゲートを含む単純なキャパシタ等の高速・高密度アドバンストMOSおよびCMOSデバイスに関する。
【０００３】
【従来の技術】アドバンスト半導体製造の分野では、高速・高密度MOSデバイスは一般に0.1μm未満のたいへん短いチャンネル長を必要とする。既存のMOSデバイス構造を直線的にそのような短いチャンネル長に合わせることは実用的ではなく、また実行可能なものでもない。
【０００４】したがって、従来のMOSデバイスの上記問題点を克服するために、ポリシリコン・ゲートを持つMOSデバイスのいくつかの新しい型、例えばシリコン・オン・インシュレータ（SOI）やダブル・ゲートMOSデバイスが開発されてきた。しかし、このような従来のデバイスのすべてに共通することは、一般に厚さが約4.0nm未満のたいへん薄い誘電体を必要とする。そのような薄いゲート誘電体を持つデバイスは、可能な限り低いバイアス電圧でもって作動させなければならない。
【０００５】現在のところ、閾値電圧VTの制御は２つのパラメータを調整することによって行われる。第１に、ポリシリコン・ゲートの仕事関数を、p-FETおよびn-FETそれぞれについて、ゲートにp^+またはn^+をドープすることで調整する。第２に、チャンネルの仕事関数を、該チャンネルとゲートとの間に許容可能な仕事関数差を設けるために、基板へ相応にドーピングすることで調節する。この仕事関数差によって内部拡散電位が与えられる。この内部拡散電位は、外部に印加されたバイアス電圧とともに作用して、デバイスのオンおよびオフを行う。
【０００６】ゲート長が0.1μmよりもかなり下回るMOSデバイスでは、一つのデバイスから他のデバイスまでの局所的ドーパント濃度の変動は、容認できないほどのVTの分散をもたらす。したがって、アドバンストCMOSの設計は、本質的に固有のチャンネルで作られなければならない。このことは、VTを設定するために今まで使用された上記パラメータの一つを取り除くので、ゲート仕事関数だけが残る。
【０００７】もっとも低い実現可能な外部から印加されたバイアス電圧を得るために、ゲートのフェルミ準位は、シリコンの価電子帯と伝導帯との間の中間、すなわち中間ギャップに位置すべきである。その結果、ポリシリコン・ゲートを使用する既存の技術ではこのような要求に応えることができない。したがって、精巧な超薄誘電体の加工ができるほど良好な導電率、中間ギャップ仕事関数を持つ新規ゲート材料の開発が求められている。このことには、限定されるものではないけれども、高エネルギー荷電粒子、イオン照射、超薄ゲート誘電体を腐食すると思われる腐食性薬品、および任意の好ましくないゲート材料と誘電体との間の熱力学的に固有の相互作用、例えば相互拡散、粗面化、または相互的な科学的不安定性が無いことが含まれる。ここで注目すべきことは、後に掲げられた固有の要件は、超薄誘電体にとってたいへん厳しいものである。なぜなら、許容できないほど大きな漏れ電流が誘電体の有効厚さにおけるたいへん小さな変化によって誘導されるかもしれないからである。
【０００８】これらの目的および他の目的は、タングステン・ヘキサカルボニル、$W(CO)_6$を原料物質とする低温・低圧CVDプロセスを用いて超薄誘電体等の誘電体層に直接蒸着される中間ギャップ仕事関数Wゲートまたは電極を提供する本発明の方法に合致する。
【０００９】ここで、強調しておくべきことは、CVD技

GF Exhibit 1124 - 1544/2704

術を用いたWの蒸着は当該技術分野において熟知されたものであり、一般に実装の際に配線手段として適用されるということである。そのような用途では、$W(CO)_6$ではなくタングステン・ヘキサフルオリド、WF6が原料物質として一般に用いられる。配線の応用にタングステン・カルボニルを使用することについてはほとんど注目されてこなかった。なぜなら、適度に純粋なW膜を作る上で相対的に高温が必要とされるからである。

【００１０】WF_6を用いたCVDの化学的性質を用いた中間ギャップ仕事関数Wゲートについては、従来技術にすでに開示されている。しかし、このプロセスは、基本的に本発明のものとは異なる。WF_6は超薄ゲート誘電体上に直接Wを蒸着させることに使用することはできない。その代わり、化学的活性段階においてゲート誘電体上にシリコンの薄層を最初に蒸着させ、つぎに（SiF_4を形成するために）シリコンを反応させて除去し、そのかわりにWを残す。さらに、均一にかなり厚い酸化物膜（250nm）の露光はいかなる例外もなしに、大規模なゲート誘電体漏れ電流が認められる完全なデバイス破損を引き起こす。CVDに加えて他の技術が用いられてきたが、従来のプロセスのいずれも超薄ゲート誘電体上に直接Wを蒸着することはできない。

【００１１】配線の用途にタングステン・カルボニルがかなり使用されているにもかかわらず、超薄ゲート誘電体等の誘電体上に中間ギャップ仕事関数Wゲートを設けるために$W(CO)_6$をCDV原料物質として使用することは開示されていない。

【００１２】

【発明が解決しようとする課題】本発明の第１の目的は、ほとんどの従来のプロセスによって一般に必要とされるような任意の化学的活性化準備段階の必要性なしにMOSおよびCMOS用途に使用するために超薄ゲート誘電体等のゲート誘電体に直接中間ギャップ作業関数Wゲートを製造するための方法を提供することである。

【００１３】本発明の第２の目的は、高純度（99.99%以上）で、かつ一般に約５ないし６μohm－cmである理想的なバルク値に近似する抵抗値を持つ超薄ゲート誘電体等のゲート誘電体と合致する中間ギャップ作業関数Wゲートの製造方法を提供することである。

【００１４】本発明の第３の目的は、原料物質として$W(CO)_6$を用いた低温度・低圧力CVDプロセスを含む誘電体上に直接W電極を製造する方法を影響することである。

【００１５】本発明の第４の目的は、原料物質として$W(CO)_6$を用いたCVDによってゲート誘電体上に直接蒸着された本発明の少なくとも一つのWゲートを含むFET等のMOSおよびCMOSデバイスに関する。

【００１６】

【課題を解決するための手段】これらの目的は他の目的と同様に、原料物質として$W(CO)_6$を使用した低温・低圧CVD技術を用いることで本発明によって達成される。特に、本発明の方法は、（ａ）薄膜ゲート誘電体のような誘電体上にWの均一層を直接蒸着する工程と、（ｂ）前記誘電体上に前記中間ギャップ作業関数Wゲートを含むMOSデバイスを形成するために、標準的なリソグラフィック技術を用いて、工程（ａ）で形成された構造をパターニングする工程とを有する。ここで強調すべきことは、本発明では誘電体上にW層を蒸着する上で化学的活性化段階を必要としない。

【００１７】本発明はまた、本発明の方法にもとづいて調製された少なくとも一つの中間ギャップ作業関数Wゲートを含むFET等のMOSデバイスを提供する。本発明にもとづくこのデバイスは、既存の技術にもとづいて調製された従来のデバイスに匹敵するゲート漏れ電流を示し、さらに金属ゲート作業関数に対する理論的値を示す。

【００１８】さらに、本発明は量子デバイスで使用するためのW電極を製造する方法を提供する。本発明のこの実施形態例によれば、W電極は（ａ）誘電体上にWからなる層を蒸着する工程と、前記誘電体上に前記W電極を形成するために前記W層をパターニングする工程とを有し、さらに前記蒸着は$W(CO)_6$を原料物質として用いる化学蒸着法によって行われる方法によって製造される。

【００１９】

【発明の実施の形態】上記したように、本発明は中間ギャップ作業関数WゲートまたはW電極を、いっさいの化学的活性化工程を必要とすることなし、MOSデバイス上に存在する誘電体上に直接設ける方法を提供する。本発明にもとづいて作られる中間ギャップ作業関数WゲートまたはW電極は、高純度であり、MOSデバイス上に見いだされる町薄ゲート誘電体との適合性を有し、さらに理想的なバルク値に近似した固有抵抗値をを持つ。

【００２０】本発明の方法によれば、誘電体上にW層を形成するのに十分な条件下で原料材料として$W(CO)_6$を用いたCDVを採用することによって、Wからなる層を半導体基板の表面にある誘電体の表面に直接蒸着する。当業者が熟知している従来の技術を用いて、W層を含むそのような構造をパターニングする。

【００２１】図１は、W層を蒸着するために本発明に適用される典型的なCVD装置10を示す。特に、装置10は、試験MOSウエハが置かれるグラファイト試料ホルダ・カートリッジ（不図示）を有するロード－ロック・ステンレス合金製反応室12が備わっている。この反応室12は、さらに蒸着中に試料を加熱するためのヒータ・アセンブリ18と蒸着中の圧力を制御する２つの超高真空管16および20とを備える。

【００２２】原料物質14、タングステン・ヘキサカルボニル、$W(CO)_6$は、ステンレス合金製バルブ22を介して反応室12に導入され、かつ管24によって反応室12内に入れられた試験MOSウエハに向けられる。

GF Exhibit 1124 - 1545/2704

【００２３】本発明では任意の等級の$W(CO)_6$を使用することができよう。もし低純度の等級の$W(CO)_6$を用いるとするならば、当業者に既知の精製技術を用いて反応室12への導入に先だって精製することができる。

【００２４】約250℃から約600℃の温度でもって$W(CO)_6$のCVDが起こる。より好ましくは、WのCVD蒸着は約275℃から約500℃の温度でもって起こる。CVD中の反応室の圧力は、$1x10^{-6}$Torrないし約$3x10^{-4}$Torrである。より好ましくは、$W(CO)_6$のCVDは、約$1x10^{-4}$Torrないし約$2x10^{-4}$Torrである。

【００２５】CVDプロセスの実行に要する時間は、一般に約３分から約４時間までの範囲である。この範囲よりも長い時間あるいは短い時間もここで考察する。

【００２６】上記条件下で、厚さが約3.5ないし約200、より好ましくは約50ないし100nmであるWからなる層を、誘電体上に直接蒸着させる。

【００２７】本発明に用いられる典型的なMOSウエハを図３に示す。特に、本発明に適用されうるMOSウエハ48は、少なくとも１つのドレイン領域52と少なくとも一つのソース領域54とを有し、かつこれらの領域が組み入れられた半導体基板50から構成される。また、ドレイン領域52およびソース領域54を半導体基板50の表面に配置してもよい。半導体基板50の表面には、誘電体56からなる層が配置されている。W58からなる層は、既に述べたCVD技術によってゲート誘電体層56の上面に形成される。

【００２８】本発明で使用してもよい半導体基板50は、限定されるものではないが、シリコン、SiGe、またはGaAsである。半導体基板としては、シリコンがもっとも好ましい。

【００２９】製造されている所望のMOSデバイスに応じて、本発明で用いる半導体基板をｐ－型またはｎ－型とすることができる。基板は、当業者に既知の技術を用い製造することができる。半導体基板の厚さは、本発明の方法にとっては重要なことではない。製造されている所望のデバイスに応じて厚さを変えてもよい。

【００３０】本発明で用いる超薄誘電体としては、SiO_2、窒化SiO_2、Si_3N_4、金属酸化物、およびこれらの混合物または化合物が挙げられる。本発明で用いる誘電体を、当業者に既知の方法でもって成長、蒸着、または反応させてもよい。ここで言及したゲート誘電体のため、SiO_2または軽く窒化SiO_2（全窒素含有量５％以下）が現時点ではかなり好ましいものとなっている。

【００３１】本発明の別のかなり好ましい実施形態例では、超薄ゲート誘電体を用いる。「超薄」という用語は、上記に定義したようなゲート誘電体を意味する。この材料の全体の厚さは、デバイスに組み込まれ、かつ通常の状態で作動させた場合に、ゲート漏れ電流の大部分が直接的なトンネル形成の結果によるものとなるような厚さである。特にSiO_2では、このことは約4.0nm未満の厚さに一致する。よりいっそう明確には、「超薄」という用語は、約3.0nm未満の厚さを持つゲート誘電体を意味する。

【００３２】W層58を蒸着させた後、図２に示すMOSウエハを当業者に既知の標準的なリソグラフィ技術を用いてパターニングする。この工程には、限定されるものではないが、化学蒸着（CVD）したW層の表面にフォトレジストを位置決めする段階と、フォトレジストを現像する段階と、フォトレジストがない領域をエッチング技術によって除去する段階とを含む。パターニング後の最終構造60を図３に示す。

【００３３】エッチングは、当業者に既知のウエット・エッチングあるいはドライ・エッチングの技術を用いて行うことができる。ウエット・エッチングを採用する場合、化学エッチング剤はH_2O_2、クロム酸、リン酸、酢酸硝酸等からなる群から選択される。本発明において好ましい化学エッチング剤は、H_2O_2である。化学エッチング剤からなる混合物単独で、あるいは該混合物に水を加えたものもここで検討される。

【００３４】本発明においてドライ・エッチングが採用される場合、反応性イオン・エッチング（RIE）、イオン・ビーム・エッチング（IBE）、またはレーザ切除によってエッチングを行ってもよい。これらのドライ・エッチング技術の各々は、当業者によく知られたものである。

【００３５】本発明はまた、発明の方法によって作製された超薄ゲート誘電体上に少なくとも一つの中間ギャップ作業関数Wゲートをデバイス構造内に含むMOSデバイスに関する。本発明にもとづいて調製された一つの中間ギャップ作業関数Wゲートを含む単純化されたMOSデバイスを図３に示す。デュアル・ゲートMOSデバイスのような２つ以上のMOSゲートを有するデバイスもここで検討される。

【００３６】他のMOSデバイス、例えば電解効果トランジスタ（FET）、単純キャパシタ構造、電解放出デバイス、および量子デバイスもまたここで検討される。これらの構造全体に共通なことは、本発明の方法にもとづいて製造される少なくとも一つの中間ギャップ作業関数Wゲートまたは W電極が誘電体上に直接設けられていることである。

【００３７】以下の実施例は、本発明の範囲を説明するためのものである。この実施例はただ単に説明を目的したものであることから、本発明の実施形態例はそれに限定されてはならない。

【００３８】実施例１

厚さが2.8～7.0nmの範囲内にある熱成長二酸化珪素薄膜を用いて試験構造を製造した。個々のキャパシタを100nm熱成長フィールド酸化物を用いて絶縁した。約0.1ないし0.2ohm－cmの抵抗率を持つｐ型ウエハおよびｎ型ウエハの両方に膜を成長させた。

【００３９】タングステン膜を一括して試験ウエハ上に

GF Exhibit 1124 - 1546/2704

蒸着した。特にW蒸着は約10^{-9}torrのベース圧力を持ち、荷重がロックされたステンレス合金製反応室内で行われた。タングステン・ヘキサカルボニル、$W(CO)_6$を原料気体として用いた。また、この$W(CO)_6$をステンレンス合金バルブ経由で反応室に放出するとともに、銅管を介して試料上に向けた。試料をグラファイト製試料ホルダ・カートリッジに導入し、次に反応室チャンバ内に位置したヒータ・アセンブリに導入した。約500℃で蒸着を行った。この系における成長速度は、概して約１．５nm／分であり、大ざっぱにいって温度に依存したものではなく、輸送が限定された成長の仕方を示す。

【００４０】W膜の蒸着後、標準的なリソグラフィ技術を用いてデバイスをパターニングした。各デバイスのタングステン膜に対して、H_2O_2を用いたウエット・エッチングを施した。これによって約10^{-6}から約$10^{-2}cm^2$までの範囲の面積を持つキャパシタ構造が形成された。

【００４１】上記のようにして形成されたキャパシタを高周波数および準静的キャパシタンス－電圧（Ｃ－Ｖ）および電流－電圧技術を用いて試験した。図４および図５は、約3.0ないし7.0nmキャパシタの厚さを持つWゲート酸化膜により形成されたWゲート・キャパシタ構造に関する典型的なＣ－Ｖデータを示す。データは、ｐ型およびｎ型シリコン・ウエハの両方とも含まれるデバイスに関するものである。破線および実線は、約30分間にわたって450℃で10％H_2含有窒素中で実行される標準的な後金属ゲート蒸着成形ガス・アニーリング（FGA）段階の前および後のＣ－Ｖデータを示すものである。図６および図７は、それぞれ処理通りの構造およびFGA構造のＣ－Ｖ特性を示す。

【００４２】Ｃ－Ｖデータを分析すると、FGA処理された試料について低$10^{11}cm^{-2}ev^{-1}$の境界状態密度が示される。平坦なバンド電圧は、ｎ型シリコン・ウエハでは約0.3ボルトであり、ｐ型シリコン・ウエハでは約－0.3ボルトである。このことは、それ自身のなかで、金属ゲートの準位はシリコン中間ギャップにたいへん近いところに位置していることを示している。このことはまた、図４および図５のｙ軸でのＣ－Ｖ曲線の対称性を示している。基板はｎ型およびｐ型の基板の両方ともにドーピング濃度がほぼ同一であることから、電圧の軸について完全な対称性を中間ギャップ金属作業関数ゲートが示すであろうことが予想できよう。

【００４３】上記キャパシタ構造からの電流－電圧データは、図６および図７に示すように、タングステン・ゲートおよびシリコン基板の相対的フェルミ準位と一致している漏れ電流を示している。

【００４４】これらのデータによって、タングステン・ゲート・キャパシタが図６に示すような標準的なポリシリコンをベースとしたキャパシタによって示される漏れ電流と同等の低さの漏れ電流を持つことが示される（妥当な比較を行うために、漏れ電流は真のゲート誘電体電圧降下、$V_{ox} = V_{gate} - V_{FB}$の関数として比較した）。この結果は、厚さ、7.0nmゲート誘電体についてのみ得たものではなく、超薄3.0nm誘電体膜についても求めた。タングステン・ゲートを作る（他の技術によって）ために他の研究者による以前の試みは、厚さが7.0nmの膜であってもこの要求を達成することはできない。

【００４５】本発明を詳細に示し、かつ好ましい実施形態例によって記載してきた一方で、形態および記載において上述および他の変更は本発明の精神および範囲から離れることなく実施することは当業者によって容易に理解されよう。

【００４６】まとめとして、本発明の構成に関して以下の事項を開示する。

（１）金属酸化物半導体（MOS）の応用に使用される中間ギャップ作業関数タングステン・ゲートの製造方法であって、（ａ）原料物質として$W(CO)_6$を使用した化学蒸着（CVD）によって、半導体基板上に配置されているゲート誘電体上にタングステン（Ｗ）の層を蒸着する工程と、（ｂ）前記ゲート誘電体上に前記中間ギャップ作業関数Wゲートを含むMOSデバイスを形成するために、前記（ａ）の工程で形成された構造をリソグラフィ技術を用いてパターニングする工程とを有する中間ギャップ作業関数タングステン・ゲートの製造方法。

（２）前記ゲート誘電体は、厚さが4.0nm未満である超薄ゲート誘電体であることを特徴とする上記（１）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。

（３）前記超薄ゲート誘電体は、厚さが３nm未満であることを特徴とする上記（２）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。

（４）前記超薄ゲート誘電体は、SiO_2 窒化SiO_2 Si_3N_4、金属酸化物、およびこれらの混合物からなる群から選択されることを特徴とする上記（３）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。

（５）前記超薄ゲート誘電体は、SiO_2であることを特徴とする上記（４）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。

（６）前記半導体基板は、少なくとも一つのソース領域と少なくとも一つのドレイン領域とを備えることを特徴とする上記（１）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。

（７）前記半導体基板は、ｐ型の半導体基板またはｎ型の半導体基板であることを特徴とする上記（１）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。

（８）前記半導体基板は、シリコン、SiGe、またはGaAsからなることを特徴とする上記（１）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。

（９）前記半導体基板は、シリコンからなることを特徴とする上記（１）に記載の中間ギャップ作業関数タング

GF Exhibit 1124 - 1547/2704

ステン・ゲートの製造方法。
（１０）前記化学蒸着（CVD）を行う工程は、250℃から500℃までの温度範囲で実施されることを特徴とする上記（１）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（１１）前記化学蒸着（CVD）を行う工程は、275℃から500℃までの温度範囲で実施されることを特徴とする上記（１０）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（１２）前記化学蒸着（CVD）を行う工程は、$1x10^{-6}$Torrから$3x10^{-4}$Torrまでの圧力範囲で実施されることを特徴とする上記（１）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（１３）前記化学蒸着（CVD）を行う工程は、$1x10^{-4}$Torrから$2x10^{-4}$Torrまでの圧力範囲で実施されることを特徴とする上記（１２）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（１４）前記化学蒸着（CVD）を行う工程によって得られる前記タングステンの層は、厚さが3.5nmから200nmまでの範囲にあることを特徴とする上記（１）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（１５）前記タングステンの層は、厚さが50nmから100nmまでの範囲にあることを特徴とする上記（１４）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（１６）前記パターニングを行う工程は、前記タングステンの層の所定の領域上に少なくとも一つのフォトレジストを配置する工程と、前記フォトレジストを現像する工程と、前記フォトレジストが含まれない前記タングステンの層の領域をエッチングする工程とからなることを特徴とする上記（１）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（１７）前記エッチングの工程は、ウエット・エッチングまたはドライ・エッチングからなることを特徴とする上記（１６）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（１８）前記ウエット・エッチングは、H_2O_2、リン酸、クロム酸、硝酸、およびこれらの混合物からなる群から選択される化学エッチング剤を用いて行われることを特徴とする上記（１７）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（１９）前記化学エッチング剤は、H_2O_2であることを特徴とする上記（１８）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（２０）前記ドライ・エッチングとして、反応性イオン・エッチング（RIE）、イオン・ビーム・エッチング（IBE）、およびレーザ切除によるエッチングが挙げられることを特徴とする上記（１７）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（２１）MOSウエハを設ける工程をさらに含み、また前記MOSウエハは、少なくとも一つのソース領域と少なくとも一つのドレイン領域とを有するｐ型半導体基板またはｎ型半導体基板であり、さらに該ｐ型半導体基板またはｎ型半導体基板上に誘電体が配置されていることを特徴とする上記（１）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（２２）タングステン電極を製造する方法であって、（ａ）原料材料として$W(CO)_6$を用いる化学蒸着（CVD）によって、誘電体をタングステンの層に蒸着する工程と、（ｂ）前記誘電体上にタングステン電極を形成するために、前記タングステンの層をパターニングする工程とを有することを特徴とするタングステン電極の製造方法。
（２３）ゲート誘電体上に少なくとも一つの中間ギャップ作業関数タングステン・ゲートを有するMOSデバイスであって、前記中間ギャップ作業関数タングステン・ゲートは、上記（１）に記載の方法によって形成されることを特徴とするMOSデバイス。
（２４）前記ゲート誘電体は、厚さが4.0nm未満である超薄ゲート誘電体であることを特徴とする上記（２３）に記載のMOSデバイス。
（２５）ゲート誘電体上に少なくとも一つの中間ギャップ作業関数タングステン・ゲートを有する電界効果トランジスタ（FET）であって、前記中間ギャップ作業関数タングステン・ゲートは、上記（１）に記載の方法によって形成されることを特徴とする電界効果トランジスタ。
（２６）前記ゲート誘電体は、厚さが4.0nm未満である超薄ゲート誘電体であることを特徴とする上記（２５）に記載の電界効果トランジスタ。

【図面の簡単な説明】

【図１】超薄ゲート誘電体上にWを直接蒸着するために、本発明に適用される典型的なCVD装置の構成を説明するための模式的平面図である。
【図２】本発明にもとづく方法にもとづいて調製された典型的なMOSデバイスの構成を示すもので、Wを蒸着した後の断面図である。
【図３】本発明にもとづく方法にもとづいて調製された典型的なMOSデバイスの構成を示すもので、パターニングを施した後の断面図である。
【図４】本発明にもとづいて形成された厚さ3.0nmのWゲート・キャパシタ構造のキャパシタンスと電圧との関係を示すキャパシタンス－電圧曲線図であり、図中、破線は成長した際の関係を示し、実線は成形ガス・アニーリング（FGA）を行った後の関係を示す。
【図５】本発明にもとづいて形成された厚さ7.0nmのWゲート・キャパシタ構造のキャパシタンスと電圧との関係を示すキャパシタンス－電圧曲線図であり、図中、破線は成長した際の関係を示し、実線は成形ガス・アニーリング（FGA）を行った後の関係を示す。

GF Exhibit 1124 - 1548/2704

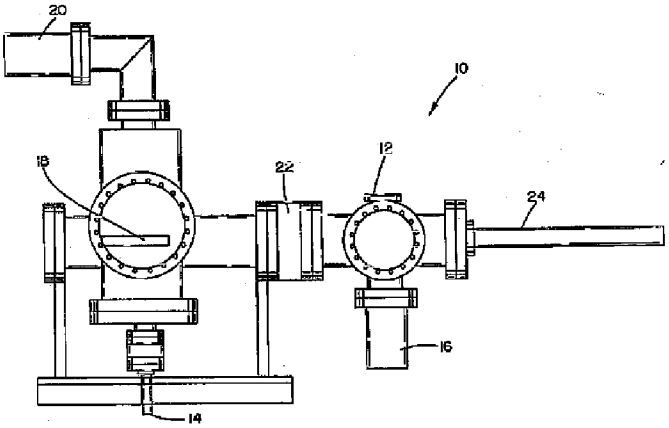
【図６】本発明にもとづいて形成された厚さ3.0nmのWゲート・キャパシタ構造の電流と電圧との関係を示す電流－電圧曲線図であり、図中、破線は成長した際の関係を示し、実線は成形ガス・アニーリング（FGA）を行った後の関係を示す。

【図７】本発明にもとづいて形成された厚さ7.0nmのWゲート・キャパシタ構造の電流と電圧との関係を示す電流－電圧曲線図であり、図中、破線は成長した際の関係を示し、実線は成形ガス・アニーリング（FGA）を行った後の関係を示す。

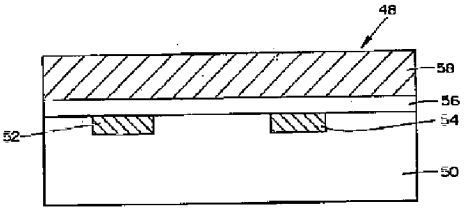
【符号の説明】

１０	CVD装置
１２	ロード－ロック・ステンレス合金製反応室
１４	原料物質
１６	超高真空管
１８	ヒータ・アセンブリ
２０	超高真空管
２２	ステンレス合金製バルブ
２４	管
４８	MOSウエハ
５０	半導体基板
５２	ドレイン領域
５４	ソース領域
５６	誘電体からなる層（ゲート誘電体層）
５８	タングステン（W）からなる層
６０	最終構造

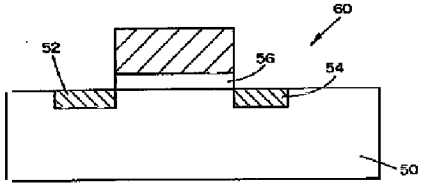
【図１】



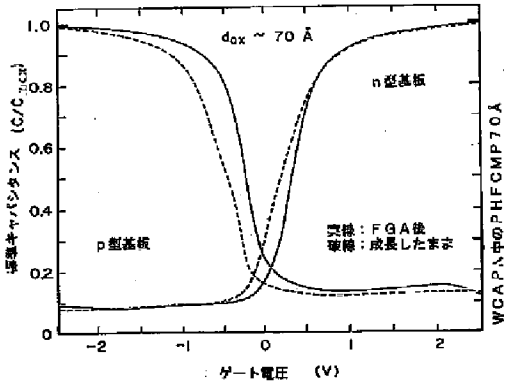
【図２】



【図３】

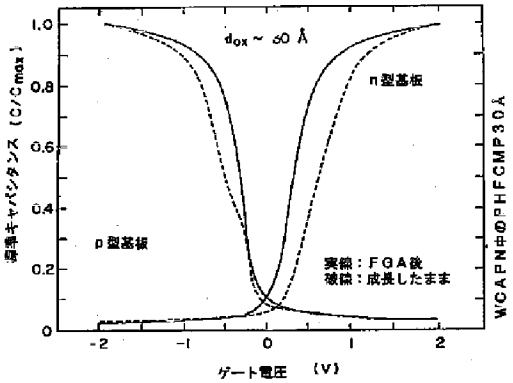


【図４】

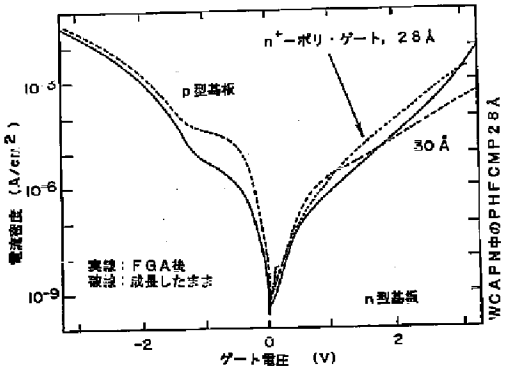


GF Exhibit 1124 - 1549/2704

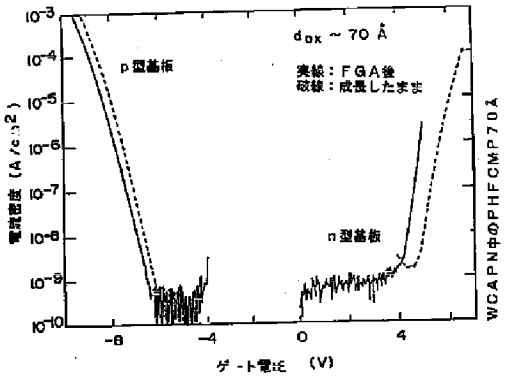
【図５】



【図６】



【図７】



フロントページの続き

(72)発明者　フェントン・リード・マクフェリィー
アメリカ合衆国10562　ニューヨーク州
オッシニング　ドナルド　レーン　25

(72)発明者　ジョン・ヤコブ・ユーカス
アメリカ合衆国06905　コネティカット州
スタンフォード　ハイ　アヴェニュー
94

GF Exhibit 1124 - 1550/2704

Espacenet

JPH10135452A MANUFACTURE OF INTERMEDIATE GAP WORK FUNCTION TUNGSTEN GATE

Applicants: IBM

Inventors: BUCHANAN DOUGLAS ANDREW,MCFEELY FENTON READ,YURKAS JOHN JACOB

Classifications:

IPC ***C23C16/16; H01L21/28; H01L21/3205; H01L29/78;*** (IPC1-7): H01L29/78;

CPC **C23C16/16 (EP); H01L21/28079 (EP); H01L21/32051 (EP);**

Priorities: US73976596A 1996-10-30

Application: JPH10135452A·1997-10-27

Publication: JPH10135452A·1998-05-22

Published as: **EP0840362A1;** JPH10135452A;**JP3251889B2; KR19980032402A; SG53082A1; TW353201B; US6091122A; US5789312A**

MANUFACTURE OF INTERMEDIATE GAP WORK FUNCTION TUNGSTEN GATE

Abstract

PROBLEM TO BE SOLVED: To provide a method of forming an intermediate gap work function tungsten (W) gate and a W electrode directly on a gate dielectric such as an ultra-thin gate dielectric for use in a high speed and high density advanced metal-oxide semiconductor(MOS) and a complementary metal oxide film semiconductor(CMOS) device, and an MOS device and a CMOS device each having at least one W gate or W electrode formed by the above method by chemical vapor deposition(CVD), and to enable the method to be applied to the manufacture of a W electrode which can be used in a quantum device. SOLUTION: This method comprises the steps of (a) vapor depositing a tungsten (W) layer 58 on a gate dielectric 56 arranged on a semiconductor substrate 50 by CVD using W(CO)6 as a material substance, and (b) patterning the structure formed by the step (a) by using a lithography technique in order to form a MOS device including an intermediate gap work function W gate on the gate dielectric 56.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION JPH10135452

[0001]
FIELD OF THE INVENTION This invention relates directly to gate dielectrics such as ultra-thin gate dielectrics used in high speed, high density advanced metal oxide semiconductor (MOS) and complementary metal oxide semiconductor (CMOS) devices. To a method for manufacturing a mid-gap workfunction tungsten (W) gate. In particular, the intermediate gap work function W gate of the present invention is fabricated directly on the gate dielectric by low temperature low pressure chemical vapor deposition using tungsten hexachloride (hereinafter W (CO) 6) as the source material. The method of the present invention can also be applied to the manufacture of W electrodes that can be used in quantum devices.

[0002]
The present invention is directed to high speed, high density advanced MOS and CMOS devices such as simple capacitors containing at least one intermediate gap work function W gate fabricated by the method of the present invention on field effect transistors (FETs) and gate dielectrics. Regarding

[0003]

BACKGROUND OF THE INVENTION In the field of advanced semiconductor manufacturing, high speed, high density MOS devices typically require very short channel lengths of less than 0.1 μm.

GF Exhibit 1124 - 1552/2704

Linearly matching existing MOS device structures to such short channel lengths is neither practical nor feasible.

[0004]

Therefore, in order to overcome the above problems of conventional MOS devices, several new types of MOS devices with polysilicon gates have been developed, such as silicon-on-insulator (SOI) and double-gate MOS devices. It was However, common to all such conventional devices requires a very thin dielectric, typically less than about 4.0 nm thick. Devices with such thin gate dielectrics must operate with the lowest possible bias voltage.

[0005]

At present, the control of the threshold voltage VT is done by adjusting two parameters. First, the work function of the polysilicon gate is tuned for p-FET and n-FET, respectively, by doping the gate with p + or n +. Second, the work function of the channel is adjusted by correspondingly doping the substrate to provide an acceptable work function difference between the channel and the gate. An internal diffusion potential is given by this work function difference. This internal diffusion potential acts with the externally applied bias voltage to turn the device on and off.

[0006]

For MOS devices with gate lengths well below 0.1 μm, variations in local dopant concentration from one device to another result in unacceptable VT dispersion. Therefore, advanced CMOS designs must be made with essentially unique channels. This removes one of the above parameters previously used to set VT, so that only the gate work function remains.

[0007]

In order to obtain the lowest feasible externally applied bias voltage, the Fermi level of the gate should be located at the middle, or middle gap, between the valence band and the conduction band of silicon. As a result, existing technology using polysilicon gates cannot meet such

GF Exhibit 1124 - 1553/2704

demands. Therefore, there is a demand for the development of a new gate material having a good conductivity and an intermediate gap work function, which are capable of processing delicate ultrathin dielectrics. This includes, but is not limited to, energetic charged particles, ion bombardment, corrosive chemicals that are believed to corrode ultra-thin gate dielectrics, and any unwanted heat between the gate material and the dielectric. It includes the absence of mechanically intrinsic interactions such as interdiffusion, roughening, or mutual scientific instability. It is worth noting here that the unique requirements listed below are very strict for ultra-thin dielectrics. This is because unacceptably high leakage currents may be induced by very small changes in the effective thickness of the dielectric.

[0008]
These and other objectives are the intermediate gap work function that is directly deposited on the dielectric layer such as ultra-thin dielectric by using low temperature / low pressure CVD process using tungsten / hexacarbonyl and W (CO) 6 as raw materials. Consistent with the method of the present invention to provide a W gate or electrode.

[0009]

Here, it should be emphasized that the vapor deposition of W using the CVD technique is well known in the technical field and is generally applied as a wiring means at the time of mounting.

For such applications, tungsten hexafluoride, WF6, rather than W (CO) 6, is commonly used as the source material. Little attention has been given to using tungsten carbonyl for wiring applications. This is because a relatively high temperature is required in order to make a moderately pure W film.

[0010]

Intermediate gap work function W gates using the CVD chemistry of WF6 have already been disclosed in the prior art. However, this process is fundamentally different from that of the present invention. WF6 cannot be used to deposit W directly on ultra-thin gate dielectrics. Instead, a thin layer of silicon is first deposited on the gate dielectric in a chemically active step, then the silicon is reacted away (to form SiF4) and removed, leaving W in its place. Furthermore, the exposure of a uniformly thick oxide film (250 nm), without any exception, causes complete device damage with large gate dielectric leakage currents observed. Although other techniques

GF Exhibit 1124 - 1554/2704

have been used in addition to CVD, none of the conventional processes are capable of depositing W directly on the ultrathin gate dielectric.

[0011]
Uses W (CO) 6 as a CDV source material to provide intermediate gap work function W gates on dielectrics such as ultra-thin gate dielectrics, despite the considerable use of tungsten carbonyl for wiring applications It is not disclosed.

[0012]
The first object of the present invention is to use it in MOS and CMOS applications without the need for any chemical activation preparatory steps as is generally required by most conventional processes. To provide a method for fabricating an intermediate gap work function W gate directly on a gate dielectric, such as an ultra thin gate dielectric.

[0013]
A second object of the invention is a gate dielectric, such as an ultra-thin gate dielectric, which is highly pure (99.99% or higher) and which has a resistance value that approximates the ideal bulk value, which is generally about 5 to 6 μ ohm-cm. Is to provide a method of manufacturing an intermediate gap work function W gate that conforms to

[0014]
A third object of the present invention is to influence the method of producing W electrodes directly on a dielectric including a low temperature, low pressure CVD process using W (CO) 6 as the source material.

[0015]
A fourth object of the invention relates to MOS and CMOS devices such as FETs comprising at least one W gate of the invention deposited directly on the gate dielectric by CVD using W (CO) 6 as the source material.

[0016]

These objects, as well as other objects, are achieved by the present invention by using a low temperature, low pressure CVD technique using W (CO) 6 as a starting material.

GF Exhibit 1124 - 1555/2704

In particular, the method of the present invention includes (a) depositing a uniform layer of W directly on a dielectric, such as a thin film gate dielectric, and (b) including the intermediate gap work function W gate on the dielectric. Patterning the structure formed in step (a) using standard lithographic techniques to form a MOS device.

It should be emphasized that the present invention does not require a chemical activation step to deposit the W layer on the dielectric.

[0017]

The invention also provides a MOS device, such as a FET, comprising at least one intermediate gap work function W gate prepared according to the method of the invention.

This device according to the invention exhibits a gate leakage current comparable to conventional devices prepared according to the existing technology, and also a theoretical value for the metal gate work function.

[0018]

Furthermore, the present invention provides a method of making a W electrode for use in a quantum device.

According to this exemplary embodiment of the present invention, the W electrode comprises (a) depositing a layer of W on the dielectric and patterning the W layer to form the W electrode on the dielectric. And the vapor deposition is performed by a chemical vapor deposition method using W (CO) 6 as a raw material.

[0019]

DETAILED DESCRIPTION OF THE INVENTION As indicated above, the present invention provides

GF Exhibit 1124 - 1556/2704

an intermediate gap work function W-gate or W-electrode on a dielectric present on a MOS device without the need for any chemical activation step. Provide a method of providing directly.

The mid-gap work function W-gates or W-electrodes made in accordance with the present invention are of high purity, compatible with the thin gate dielectrics found on MOS devices, and even closer to the ideal bulk value. It has a specific resistance value.

[0020]

According to the method of the present invention, by adopting CDV using W (CO) 6 as a raw material under conditions sufficient to form a W layer on a dielectric, a layer made of W is formed on a semiconductor substrate. Evaporate directly on the surface of the dielectric on the surface. Patterning such structures, including W layers, using conventional techniques familiar to those skilled in the art.

[0021]

FIG. 1 shows a typical CVD apparatus 10 applied to the present invention to deposit a W layer. In particular, the apparatus 10 includes a load-lock stainless steel alloy reaction chamber 12 having a graphite sample holder cartridge (not shown) on which a test MOS wafer is placed. The reaction chamber 12 further comprises a heater assembly 18 for heating the sample during deposition and two ultra high vacuum tubes 16 and 20 for controlling the pressure during deposition.

[0022]
The source material 14, tungsten hexacarbonyl, W (CO) 6 is introduced into the reaction chamber 12 via a stainless alloy valve 22 and directed by a tube 24 to a test MOS wafer contained in the reaction chamber 12.

[0023]

Any grade of W (CO) 6 could be used in the present invention.

GF Exhibit 1124 - 1557/2704

If a low purity grade W (CO) 6 is used, it can be purified prior to introduction into reaction chamber 12 using purification techniques known to those skilled in the art.

[0024]

CVD of W (CO) 6 occurs at temperatures of about 250 ° C to about 600 ° C. More preferably, the CVD deposition of W occurs at a temperature of about 275 ° C to about 500 ° C. The pressure of the reaction chamber during CVD is 1x10-6 Torr to about 3x10-4 Torr. More preferably, the W (CO) 6 CVD is from about 1×10^{-4} Torr to about 2×10^{-4} Torr.

[0025]

The time required to perform the CVD process generally ranges from about 3 minutes to about 4 hours. Times longer or shorter than this range are also considered here.

[0026]
Under the above conditions, a layer of W having a thickness of about 3.5 to about 200, more preferably about 50 to 100 nm is deposited directly on the dielectric.

[0027]

A typical MOS wafer used in the present invention is shown in FIG.

In particular, the MOS wafer 48 applicable to the present invention comprises a semiconductor substrate 50 having at least one drain region 52 and at least one source region 54 and incorporating these regions. Further, the drain region 52 and the source region 54 may be arranged on the surface of the semiconductor substrate 50. On the surface of the semiconductor substrate 50, a layer made of a dielectric material 56 is arranged. A layer of W58 is formed on top of the gate dielectric layer 56 by the CVD technique previously described.

[0028]

GF Exhibit 1124 - 1558/2704

The semiconductor substrate 50 that may be used in the present invention is, but not limited to, silicon, SiGe, or GaAs. Silicon is the most preferable semiconductor substrate.

[0029]

The semiconductor substrate used in the present invention can be p-type or n-type depending on the desired MOS device being manufactured. The substrate can be manufactured using techniques known to those skilled in the art. The thickness of the semiconductor substrate is not critical to the method of the present invention. The thickness may vary depending on the desired device being manufactured.

[0030]

Ultrathin dielectrics used in the present invention include SiO2, SiO2 nitride, Si3N4, metal oxides, and mixtures or compounds thereof. The dielectric used in the present invention may be grown, deposited, or reacted by methods known to those skilled in the art. Due to the gate dielectrics mentioned here, SiO2 or lightly nitrided SiO2 (total nitrogen content <5%) is currently quite preferred.

[0031]

Another fairly preferred embodiment of the present invention uses an ultra-thin gate dielectric. The term "ultra thin" means a gate dielectric as defined above. The total thickness of this material is such that when incorporated into a device and operated under normal conditions most of the gate leakage current is the result of direct tunneling. Especially for SiO2, this corresponds to a thickness of less than about 4.0 nm. Even more specifically, the term "ultra-thin" means a gate dielectric having a thickness of less than about 3.0 nm.

[0032]

After the W layer 58 is deposited, the MOS wafer shown in FIG. 2 is patterned using standard

GF Exhibit 1124 - 1559/2704

lithographic techniques known to those skilled in the art. The process is not limited to, but includes the steps of positioning the photoresist on the surface of the chemical vapor deposition (CVD) W layer, developing the photoresist, and removing the photoresist-free area by an etching technique. And the step of doing. The final structure 60 after patterning is shown in FIG.

[0033]

Etching can be performed using wet etching or dry etching techniques known to those skilled in the art. If wet etching is employed, the chemical etchant is selected from the group consisting of H2O2, chromic acid, phosphoric acid, acetic acid nitric acid and the like. The preferred chemical etchant in the present invention is H2O2. Mixtures of chemical etchants either alone or with water added are also contemplated herein.

[0034]

When dry etching is employed in the present invention, the etching may be done by reactive ion etching (RIE), ion beam etching (IBE), or laser ablation. Each of these dry etching techniques are well known to those skilled in the art.

[0035]

The present invention also relates to a MOS device including at least one intermediate gap work function W gate in a device structure on an ultrathin gate dielectric made by the method of the invention. A simplified MOS device containing one mid-gap work function W gate prepared according to the present invention is shown in FIG. Devices having more than one MOS gate, such as dual gate MOS devices, are also contemplated herein.

[0036]

Other MOS devices, such as field effect transistors (FETs), simple capacitor structures, field emission devices, and quantum devices are also discussed herein. Common to all of these structures is that at least one intermediate gap work function W gate or W electrode manufactured according to the method of the present invention is provided directly on the

GF Exhibit 1124 - 1560/2704

dielectric.

[0037]

The following examples serve to illustrate the scope of the invention. The example embodiments of the present invention should not be limited thereto, as this example is for illustrative purposes only.

[0038]

Example 1 A test structure was manufactured using a thermally grown silicon dioxide thin film having a thickness in the range of 2.8 to 7.0 nm. Individual capacitors were insulated with 100 nm thermally grown field oxide. Films were grown on both p-type and n-type wafers with a resistivity of about 0.1 to 0.2 ohm-cm.

[0039]

A tungsten film was collectively deposited on the test wafer. In particular, W deposition was performed in a stainless steel reaction chamber with a base pressure of about 10-9 torr and a load locked. Tungsten hexacarbonyl and W (CO) 6 were used as source gases. In addition, this W (CO) 6 was discharged into the reaction chamber via a stainless steel alloy valve and was directed onto the sample via a copper tube. The sample was introduced into a graphite sample holder cartridge and then into a heater assembly located in the reaction chamber chamber. Deposition was performed at about 500 ° C. The growth rate in this system is generally about 1.5 nm / min and is roughly temperature independent and shows a mode of transport limited growth.

[0040]

After deposition of the W film, the device was patterned using standard lithographic techniques. Wet etching using H2O2 was performed on the tungsten film of each device. This formed a capacitor structure with an area in the range of about 10-6 to about 10-2 cm2.

GF Exhibit 1124 - 1561/2704

[0041]

The capacitors formed as described above were tested using high frequency and quasi-static capacitance-voltage (CV) and current-voltage techniques. 4 and 5 show typical CV data for a W gate capacitor structure formed by a W gate oxide having a thickness of about 3.0 to 7.0 nm capacitor. The data is for devices that include both p-type and n-type silicon wafers. Dashed and solid lines show C-V data before and after a standard post metal gate deposition forming gas annealing (FGA) step performed in nitrogen containing 10% H2 at 450 ° C for about 30 minutes. Is. 6 and 7 show the CV characteristics of the as-processed structure and the FGA structure, respectively.

[0042]

Analysis of the CV data shows a low 1011 cm-2ev-1 boundary state density for the FGA treated sample. The flat band voltage is about 0.3 volts for n-type silicon wafers and about -0.3 volts for p-type silicon wafers. This indicates that in itself the metal gate level is located very close to the silicon intergap. This also shows the symmetry of the CV curve on the y-axis of FIGS. 4 and 5. Since the substrates are nearly identical in doping concentration for both n-type and p-type substrates, one would expect that the mid-gap metal work function gate would exhibit perfect symmetry about the voltage axis.

[0043]
The current-voltage data from the above capacitor structure shows leakage currents consistent with the relative Fermi levels of the tungsten gate and silicon substrate, as shown in FIGS.

[0044]

These data show that tungsten gate capacitors have leakage currents comparable to those exhibited by standard polysilicon-based capacitors as shown in Figure 6 (a reasonable comparison). The leakage current is compared as a function of the true gate dielectric voltage drop, Vox = Vgate-VFB).

The results were not only obtained for 7.0 nm thick gate dielectrics, but also for ultrathin 3.0 nm dielectric films. Earlier attempts by other researchers to make tungsten gates (by other

GF Exhibit 1124 - 1562/2704

techniques) cannot meet this requirement even with 7.0 nm thick films.

[0045]
While the present invention has been shown in detail and described by way of preferred example embodiments, it will be readily understood by those skilled in the art that the above and other changes in form and description may be made without departing from the spirit and scope of the invention. See.

[0046]

As a summary, the following matters are disclosed regarding the configuration of the present invention.

(1) A method of manufacturing an intermediate gap work function tungsten gate used in metal oxide semiconductor (MOS) applications, which is (a) by chemical vapor deposition (CVD) using W (CO) 6 as a source material. Depositing a layer of tungsten (W) on a gate dielectric disposed on a semiconductor substrate, and (b) forming a MOS device including the intermediate gap work function W gate on the gate dielectric. And a step of patterning the structure formed in the step (a) by using a lithographic technique. (2) The method of manufacturing an intermediate gap work function tungsten gate according to (1) above, wherein the gate dielectric is an ultra-thin gate dielectric having a thickness of less than 4.0 nm. (3) The method for manufacturing an intermediate gap work function tungsten gate according to (2) above, wherein the ultrathin gate dielectric has a thickness of less than 3 nm. (4) The intermediate gap work function tungsten of (3) above, wherein the ultra-thin gate dielectric is selected from the group consisting of SiO2, SiO2 nitride, Si3N4, metal oxides, and mixtures thereof. -Method of manufacturing gate. (5) The method of manufacturing the intermediate gap work function tungsten gate according to the above (4), wherein the ultra-thin gate dielectric is SiO2. (6) The method of manufacturing the intermediate gap work function tungsten gate according to the above (1), wherein the semiconductor substrate has at least one source region and at least one drain region. (7) The method for manufacturing an intermediate gap work function tungsten gate according to (1) above, wherein the semiconductor substrate is a p-type semiconductor substrate or an n-type semiconductor substrate. (8) The method for manufacturing an intermediate gap work function tungsten gate according to the above (1), wherein the semiconductor substrate is made of silicon, SiGe, or GaAs. (9) The method of manufacturing the intermediate gap work function tungsten gate according to the above (1), wherein the semiconductor substrate is made of silicon. (10) Manufacturing of the intermediate gap work function tungsten gate according to the above (1), wherein the step of performing the chemical vapor deposition (CVD) is performed in a

GF Exhibit 1124 - 1563/2704

temperature range of 250 ° C to 500 ° C. Method. (11) Manufacturing of the intermediate gap work function tungsten gate according to the above (10), wherein the step of performing the chemical vapor deposition (CVD) is performed in a temperature range of 275 ° C to 500 ° C. Method.

(12) Manufacturing of the intermediate gap work function tungsten gate according to the above (1), wherein the step of performing the chemical vapor deposition (CVD) is performed in a pressure range of 1x10-6 Torr to 3x10-4 Torr. Method. (13) Manufacturing of the intermediate gap work function tungsten gate according to the above (12), wherein the step of performing the chemical vapor deposition (CVD) is performed in a pressure range of 1x10-4 Torr to 2x10-4 Torr. Method. (14) The intermediate gap work function tungsten according to the above (1), wherein the tungsten layer obtained by the step of performing the chemical vapor deposition (CVD) has a thickness in a range of 3.5 nm to 200 nm. -Method of manufacturing gate. (15) The method of manufacturing the intermediate gap work function tungsten gate according to the above (14), wherein the tungsten layer has a thickness in a range of 50 nm to 100 nm. (16) The patterning step includes the steps of disposing at least one photoresist on a predetermined region of the tungsten layer, developing the photoresist, and removing the tungsten not containing the photoresist. The method of manufacturing an intermediate gap work function tungsten gate according to (1) above, comprising the step of etching a region of the layer. (17) The method for manufacturing an intermediate gap work function tungsten gate according to the above (16), wherein the etching step comprises wet etching or dry etching. (18) The wet etching according to (17) above, wherein the wet etching is performed using a chemical etching agent selected from the group consisting of H2O2, phosphoric acid, chromic acid, nitric acid, and a mixture thereof. Method of manufacturing intermediate gap work function tungsten gate. (19) The method for manufacturing an intermediate gap work function tungsten gate according to the above (18), wherein the chemical etching agent is H2O2. (20) The intermediate gap work according to (17) above, wherein the dry etching includes reactive ion etching (RIE), ion beam etching (IBE), and laser ablation etching. Method of manufacturing a function tungsten gate. (21) The method further includes the step of providing a MOS wafer, and the MOS wafer is a p-type semiconductor substrate or an n-type semiconductor substrate having at least one source region and at least one drain region, and the p-type semiconductor substrate is further included. Alternatively, the method for manufacturing the intermediate gap work function tungsten gate according to the above (1), wherein the dielectric is disposed on the n-type semiconductor substrate.

(22) A method of manufacturing a tungsten electrode, comprising: (a) depositing a dielectric material on a tungsten layer by chemical vapor deposition (CVD) using W (CO) 6 as a raw material; A step of patterning the tungsten layer in order to form a tungsten electrode on the body. (23) A MOS device having at least one intermediate gap work function tungsten gate on a

GF Exhibit 1124 - 1564/2704

gate dielectric, wherein the intermediate gap work function tungsten gate is formed by the method according to (1) above. Characteristic MOS device. (24) The MOS device according to (23) above, wherein the gate dielectric is an ultrathin gate dielectric having a thickness of less than 4.0 nm. (25) A field effect transistor (FET) having at least one intermediate gap work function tungsten gate on a gate dielectric, said intermediate gap work function tungsten gate formed by the method according to (1) above. A field effect transistor characterized by being formed. (26) The field effect transistor according to the above (25), wherein the gate dielectric is an ultrathin gate dielectric having a thickness of less than 4.0 nm.

[0047]
Brief description of the drawings

[0048]
1 is a schematic plan view for explaining the configuration of a typical CVD apparatus applied to the present invention to deposit W directly on the ultra-thin gate dielectric.

[0049]
2 is a cross-sectional view showing the structure of a typical MOS device prepared by the method according to the present invention, after W is deposited.

[0050]
3 is a cross-sectional view after patterning, showing the structure of a typical MOS device prepared according to the method according to the present invention.

[0051]
4 is a capacitance-voltage curve diagram showing the relationship between the capacitance and voltage of the W gate capacitor structure having a thickness of 3.0 nm formed according to the present invention, in which the broken line shows the relationship when grown, The solid line shows the relationship after performing forming gas annealing (FGA).

[0052]
5 is a capacitance-voltage curve diagram showing the relationship between the capacitance and the voltage of the W gate capacitor structure having a thickness of 7.0 nm formed according to the present invention, in which the broken line shows the relationship when grown, The solid line shows the relationship after performing forming gas annealing (FGA).

GF Exhibit 1124 - 1565/2704

[0053]
6 is a current-voltage curve diagram showing the relationship between the current and voltage of the W gate capacitor structure having a thickness of 3.0 nm formed according to the present invention, in which the broken line shows the relationship when grown, The solid line shows the relationship after performing forming gas annealing (FGA).

[0054]
7 is a current-voltage curve diagram showing the relationship between the current and voltage of the W gate capacitor structure having a thickness of 7.0 nm formed according to the present invention, in which the broken line shows the relationship when grown, The solid line shows the relationship after performing forming gas annealing (FGA).

[0055]
Explanation of symbols

[0056]
10 CVD Device 12 Load-Lock Stainless Steel Reaction Chamber 14 Raw Material 16 Ultra High Vacuum Tube 18 Heater Assembly 20 Ultra High Vacuum Tube 22 Stainless Alloy Valve 24 Tube 48 MOS Wafer 50 Semiconductor Substrate 52 Drain Region 54 Source Region 56 Dielectric Material Layer made of (gate dielectric layer) 58 Layer made of tungsten (W) 60 Final structure

GF Exhibit 1124 - 1566/2704

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

CLAIMS JPH10135452

1.
A method of manufacturing an intermediate gap work function tungsten gate used in metal oxide semiconductor (MOS) applications, comprising: (a) a chemical vapor deposition (CVD) using W (CO) 6 as a source material to form a semiconductor substrate. Depositing a layer of tungsten (W) on an overlying gate dielectric, and (b) forming a MOS device including the intermediate gap work function W gate on the gate dielectric. Patterning the structure formed in step (a) using a lithographic technique.

2.
The method of claim 1, wherein the gate dielectric is an ultra-thin gate dielectric having a thickness of less than 4.0 nm.

3.
The method of claim 2, wherein the ultra-thin gate dielectric has a thickness of less than 3 nm.

4.
The fabrication of intermediate gap work function tungsten gates according to claim 3, wherein the ultra-thin gate dielectric is selected from the group consisting of SiO2, SiO2 nitride, Si3N4, metal oxides, and mixtures thereof. Method.

5.

GF Exhibit 1124 - 1567/2704

The method of claim 4, wherein the ultra-thin gate dielectric is SiO2.

6.
The method of claim 1, wherein the semiconductor substrate comprises at least one source region and at least one drain region.

7.
The method of claim 1, wherein the semiconductor substrate is a p-type semiconductor substrate or an n-type semiconductor substrate.

8.
The method of claim 1, wherein the semiconductor substrate comprises silicon, SiGe, or GaAs.

9.
The method of claim 1, wherein the semiconductor substrate is made of silicon.

10.
The method of claim 1, wherein the step of performing chemical vapor deposition (CVD) is performed in a temperature range of 250 ° C to 500 ° C.

11.
The method of claim 10, wherein the step of performing chemical vapor deposition (CVD) is performed in a temperature range of 275 ° C to 500 ° C.

12.
The method of claim 1, wherein the step of performing chemical vapor deposition (CVD) is performed in a pressure range of 1x10-6 Torr to 3x10-4 Torr.

13.
13. The method of claim 12, wherein the step of performing chemical vapor deposition (CVD) is performed in a pressure range of 1x10-4 Torr to 2x10-4 Torr.

GF Exhibit 1124 - 1568/2704

14.

10. The intermediate gap work function tungsten gate of claim 1, wherein the layer of tungsten obtained by the step of performing chemical vapor deposition (CVD) has a thickness in the range of 3.5 nm to 200 nm. Production method.

15.

15. The method of manufacturing a mid-gap work function tungsten gate of claim 14, wherein the layer of tungsten has a thickness in the range of 50 nm to 100 nm.

16.

The step of patterning comprises the steps of disposing at least one photoresist over a predetermined region of the tungsten layer, developing the photoresist, and removing the tungsten layer not containing the photoresist. The method of claim 1, further comprising the step of etching the region.

17.

17. The method of claim 16, wherein the etching step comprises wet etching or dry etching.

18.

18. The intermediate gap work of claim 17, wherein the wet etching is performed with a chemical etchant selected from the group consisting of H2O2, phosphoric acid, chromic acid, nitric acid, and mixtures thereof. Method of manufacturing a function tungsten gate.

19.

19. The method of claim 18, wherein the chemical etchant is H2O2.

20.

18. The intermediate gap work function tungsten of claim 17, wherein the dry etching includes reactive ion etching (RIE), ion beam etching (IBE), and laser ablation etching. Gate manufacturing method.

21.

The method further includes the step of providing a MOS wafer, and the MOS wafer is a p-type semiconductor substrate or an n-type semiconductor substrate having at least one source region

GF Exhibit 1124 - 1569/2704

and at least one drain region, and the p-type semiconductor substrate or n-type semiconductor substrate. The method of claim 1, wherein the dielectric is disposed on the semiconductor substrate of the mold.

22.

A method of manufacturing a tungsten electrode, the method comprising: (a) depositing a dielectric material on a tungsten layer by chemical vapor deposition (CVD) using W (CO) 6 as a raw material; and (b) on the dielectric material. A step of patterning the tungsten layer to form a tungsten electrode on the substrate.

23.

A MOS device having at least one intermediate gap work function tungsten gate on a gate dielectric, said intermediate gap work function tungsten gate being formed by the method of claim 1. MOS device.

24.

The MOS device of claim 23, wherein the gate dielectric is an ultra-thin gate dielectric having a thickness of less than 4.0 nm.

25.

A field effect transistor (FET) having at least one intermediate gap work function tungsten gate on a gate dielectric, said intermediate gap work function tungsten gate being formed by the method of claim 1. Field-effect transistor characterized by.

26.

The field effect transistor of claim 25, wherein the gate dielectric is an ultra-thin gate dielectric having a thickness of less than 4.0 nm.

GF Exhibit 1124 - 1570/2704

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号

特開平10－209445

(43)公開日　平成10年(1998)８月７日

(51)Int.Cl.[6]	識別記号	ＦＩ	
Ｈ０１Ｌ　29/78		Ｈ０１Ｌ　29/78	３０１Ｇ
21/336			３０１Ｐ

審査請求　有　　請求項の数10　ＯＬ　（全 10 頁）

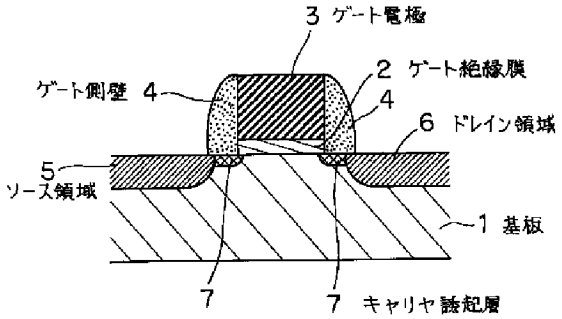
(21)出願番号　特願平9－8653

(22)出願日　平成９年(1997)１月21日

(71)出願人　000004237
日本電気株式会社
東京都港区芝五丁目７番１号
(72)発明者　古川　昭雄
東京都港区芝五丁目７番１号　日本電気株式会社内
(74)代理人　弁理士　若林　忠

(54)【発明の名称】　ＭＯＳＦＥＴおよびその製造方法

(57)【要約】
【課題】　短チャネル効果を抑制するのに充分な拡散層の接合深さを、寄生容量増加によるスイッチング速度の低下、製造工程の複雑化などの問題を引き起こさず実現する。
【解決手段】　ゲート側壁４にシリコンよりバンドギャップの大きな半導体を用いているので、ゲート側壁４にドープされた不純物のエネルギーと基板１の伝導帯のエネルギー差のため、ゲート側壁４からその下の基板１上にキャリヤが移動するが、キャリヤにはゲート側壁４の方向に押し付けられるような力が働くため、キャリヤは基板１上でシート状に薄く蓄積され、厚さ５ｎｍ以下の極めて薄いソース領域５・ドレイン領域６端を形成することができ短チャネル効果を抑制することができる。



GF Exhibit 1124 - 1571/2704

【特許請求の範囲】
【請求項１】　シリコン基板の上にゲート絶縁膜を介して設けられたゲート電極と、
前記ゲート電極の側壁部に設けられたゲート側壁と、
前記シリコン基板上に設けられたソース領域とドレイン領域とを有するＭＯＳＦＥＴにおいて、
前記ゲート側壁が、シリコンよりバンドギャップが大きく非導電性の半導体層により形成されるとともに不純物が導入されていることを特徴とするＭＯＳＦＥＴ。
【請求項２】　前記ゲート側壁が空乏化することにより非導電性となっている請求項１記載のＭＯＳＦＥＴ。
【請求項３】　前記ゲート側壁と前記ゲート電極の間、または前記ゲート側壁と前記シリコン基板の間、または前記ゲート側壁と前記ゲート電極および前記ゲート側壁と前記シリコン基板との間に絶縁膜が設けられている請求項１または２記載のＭＯＳＦＥＴ。
【請求項４】　シリコン基板の上にゲート絶縁膜を介して設けられたゲート電極と、
前記ゲート電極の側壁部に設けられ、シリコンよりバンドギャップが大きく非導電性の半導体層により形成されるとともに不純物が導入されているゲート側壁と、
前記シリコン基板上に設けられたソース領域とドレイン領域とを有するＭＯＳＦＥＴの製造方法において、
前記ゲート側壁への不純物の導入を、前記ソース領域および前記ドレイン領域への不純物イオン注入または前記ゲート電極への不純物イオン注入と同時に行うことを特徴とするＭＯＳＦＥＴの製造方法。
【請求項５】　シリコン基板の上にゲート絶縁膜を介して設けられたゲート電極と、
前記ゲート電極の側壁部に設けられたゲート側壁と、
前記シリコン基板上に設けられたソース領域とドレイン領域とを有するＭＯＳＦＥＴにおいて、
前記ゲート側壁が強誘電体材料により形成され、前記シリコン基板がｐ形の場合には前記ゲート電極から前記シリコン基板の方向に分極され、前記シリコン基板がｎ形の場合は前記シリコン基板からゲート電極の方向に分極されていることを特徴とするＭＯＳＦＥＴ。
【請求項６】　前記ゲート側壁と前記ゲート電極の間、または前記ゲート側壁と前記シリコン基板の間、または前記ゲート側壁と前記ゲート電極および前記ゲート側壁と前記シリコン基板との間に絶縁膜が設けられている請求項５記載のＭＯＳＦＥＴ。
【請求項７】　シリコン基板の上にゲート絶縁膜を介して設けられたゲート電極と、
前記ゲート電極の側壁部に設けられ強誘電体材料により形成されたゲート側壁と、
前記シリコン基板上に設けられたソース領域とドレイン領域とを有するＭＯＳＦＥＴの製造方法において、
層間絶縁膜を前記シリコン基板の上に形成し、前記層間絶縁膜に前記シリコン基板へ通ずるコンタクト穴を形成し、前記コンタクト穴を金属で埋め込みコンタクト埋め込みとする工程と、
前記ゲート側壁上部に前記層間絶縁膜を介して第１の電極を形成し、前記コンタクト埋め込みの上部に第２の電極を形成する工程と、
前記第１の電極と前記第２の電極との間に電圧を印加し、前記ゲート側壁を分極する工程とを有することを特徴とするＭＯＳＦＥＴの製造成方法。
【請求項８】　シリコン基板の上に複数のウェルが設けられ、前記各ウェル上に複数のゲート絶縁膜を介して設けられた複数のゲート電極と、
前記各ゲート電極の側壁部に設けられ強誘電体材料により形成された複数のゲート側壁と、
前記各ウェル上に設けられた複数のソース領域と複数のドレイン領域とを有するＭＯＳＦＥＴの製造方法において、
層間絶縁膜を前記シリコン基板の上に形成し、前記層間絶縁膜に前記各ウェルへ通ずる複数のコンタクト穴を形成し、前記各コンタクト穴を金属で埋め込みコンタクト埋め込みとする工程と、
前記各ゲート側壁上部に前記層間絶縁膜を介して複数の第１の電極を形成し、前記各コンタクト埋め込みの上部に複数の第２の電極を形成する工程と、
前記各第１の電極どうしと前記各第２の電極どうしをそれぞれ配線により接続し、接続された前記各配線の間に電圧を印加し、前記各ゲート側壁を分極する工程とを有することを特徴とするＭＯＳＦＥＴの製造成方法。
【請求項９】前記第１と第２の電極を除去する工程をさらに有する請求項７または８記載のＭＯＳＦＥＴの製造方法。
【請求項１０】　前記ゲート側壁より外側のソース領域およびドレイン領域部が金属材料により形成されていることを特徴とする請求項１、２、３、５、６のいずれか１項記載のＭＯＳＦＥＴ。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、ＭＯＳＦＥＴおよびその製造方法に関し、特にソース領域およびドレイン領域が浅く形成された構造のＭＯＳＦＥＴおよびその製造方法に関する。
【０００２】
【従来の技術】ＭＯＳＦＥＴのゲート長を０．１μｍ以下に微細化する上で問題となる現象として、しきい値がゲート長の微細化とともに減少する短チャネル効果がある。この短チャネル効果を抑制するためには、ソース領域およびドレイン領域構造において、その拡散層の接合深さ、特にゲート端付近の拡散層を浅くする方法が有効である。
【０００３】拡散層の接合深さを浅く形成する従来の方法として、図１０に示すような低エネルギーイオン注入

GF Exhibit 1124 - 1572/2704

法がある。この方法は、基板１０１表面のゲート電極１０３脇のソース領域１０５およびドレイン領域１０６に、例えば１０ｋｅＶ程度のできるだけ小さい値の注入エネルギーで不純物イオンを注入する方法であり、不純物イオン注入層１０４の深さを数十ｎｍ程度に浅くすることができる。

【０００４】拡散層の接合深さをさらに浅くする従来の方法として、図１１に示すような固層拡散法が例えば特開平７－３１２４２２号公報において提案されている。この方法は、ゲート電極１０３の横に例えばリンシリケイトガラス（ＰＳＧ）またはボロンシリケイトガラス（ＢＳＧ）からなる不純物を含んだ絶縁膜として側壁１０７をまず形成し、次いで熱処理により側壁１０７中の不純物を基板１０１中に拡散する。これにより、拡散層の深さを１０ｎｍから４０ｎｍ程度にでき、イオン注入法に比べてより浅い拡散層を得ることができる。

【０００５】また、ソース領域・ドレイン領域の接合深さをさらに浅くする方法として、図１２に示すような方法が例えば特開平１－１２５９７７号公報において提案されている。この方法は、ゲート電極１０３の横に絶縁膜１０８を介してポリシリコンからなる導電性のあるサブゲート１０９を設け、それに電圧を印加するものであり、この方法によれば、サブゲート１０９下の基板１０１上にキャリヤが誘起され反転層となったキャリヤ誘起層１１１が形成されきわめて浅い導伝層が形成される。

【０００６】また、反転層を形成した浅い接合をもったＭＯＳＦＥＴの他の構造として、例えば特開平１－２３２７６５号公報には、第１ゲート電極の横に第２ゲート電極として仕事関数の異なる材料、例えば第１ゲート電極がｐ型シリコンにより形成されている場合には第２ゲート電極にｎ型シリコンを用いたり、第１ゲート電極がｎ型シリコンにより形成されている場合には第２ゲート電極に白金を用いるなどして、第２ゲート電極の下に反転層を形成したものが提案されている。

【０００７】

【発明が解決しようとする課題】上述した従来のＭＯＳＦＥＴでは、下記のような問題点があった。

（１）低エネルギーイオン注入法や固相拡散法においては、拡散層の接合深さを１０ｎｍ以下とすることができず、ゲート長０．１μｍ以下のＭＯＳＦＥＴにおいて十分短チャネル効果を抑制することができない。

（２）サブゲートを設けて電圧を印加して反転層を形成した構造においては、接合深さは浅いものの、動作時にサブゲートに電圧を印加しつづけなければならないことと、サブゲートとゲート電極およびサブゲートとドレイン領域の間に寄生容量が形成されるために、スイッチング速度の低下を招く。

（３）仕事関数の異なる第２ゲート電極を設けた構造においては、第２ゲート電極がゲート電極と接続しており、しかも導電性を持つことから、ゲート電圧印加時に第２ゲート電極にも電圧がかかるため、第２ゲート電極とチャネル間の寄生容量が存在してスイッチング速度の低下をまねく。さらに、ゲート電極および第２ゲート電極の導電性の型が異なるときは、それぞれに異なる不純物を導入する必要があるためＭＯＳＦＥＴの形成工程が複雑となる。

【０００８】本発明の目的は、短チャネル効果を抑制するのに充分な拡散層の接合深さを、寄生容量増加によるスイッチング速度の低下、製造工程の複雑化などの問題を引き起こさず実現したＭＯＳＦＥＴを提供することである。

【０００９】

【課題を解決するための手段】上記目的を達成するために、本発明のＭＯＳＦＥＴは、シリコン基板の上にゲート絶縁膜を介して設けられたゲート電極と、前記ゲート電極の側壁部に設けられたゲート側壁と、前記シリコン基板上に設けられたソース領域とドレイン領域とを有するＭＯＳＦＥＴにおいて、前記ゲート側壁が、シリコンよりバンドギャップが大きく非導電性の半導体層により形成されるとともに不純物が導入されていることを特徴とする。

【００１０】本発明は、ゲート側壁にシリコンよりバンドギャップの大きな半導体を用いているので、ゲート側壁にドープされた不純物がドナーの場合はその電子のエネルギーはシリコン基板の伝導帯のエネルギー準位より高くなり、アクセプタの場合はシリコン基板の価電子帯のエネルギー準位より低くなる。そのため、ゲート側壁にドナーがドープされていれば、そのエネルギーとシリコン基板の伝導帯のエネルギー差のため、ゲート側壁からその下のシリコン基板上に電子が移動・蓄積される。他方、アクセプタがドープされていれば、正孔が移動・蓄積される。この電子や正孔にはゲート側壁の方向に押し付けられるように力が働くため、これらの蓄積層はシート状に薄く形成され、その厚さは５ｎｍ以下となる。このため、この部分をソース領域やドレイン領域のゲート端として用いれば、５ｎｍ以下の極めて薄いソース領域・ドレイン領域端を形成することができ短チャネル効果を抑制することができる。

【００１１】本発明の実施態様によれば、前記ゲート側壁が空乏化することにより非導電性となっている。

【００１２】また、本発明の実施態様によれば、前記ゲート側壁と前記ゲート電極の間、または前記ゲート側壁と前記シリコン基板の間、または前記ゲート側壁と前記ゲート電極および前記ゲート側壁と前記シリコン基板との間に絶縁膜が設けられている。

【００１３】本発明は、絶縁膜をゲート側壁とゲート電極またはゲート側壁とシリコン基板の間に設けるようにしたものである。したがって、ゲート側壁とゲート電極またはゲート側壁とシリコン基板との間の絶縁性を向上することができる。

GF Exhibit 1124 - 1573/2704

【００１４】また、本発明のＭＯＳＦＥＴの製造方法は、シリコン基板の上にゲート絶縁膜を介して設けられたゲート電極と、前記ゲート電極の側壁部に設けられ、シリコンよりバンドギャップが大きく非導電性の半導体層により形成されるとともに不純物が導入されているゲート側壁と、前記シリコン基板上に設けられたソース領域とドレイン領域とを有するＭＯＳＦＥＴの製造方法において、前記ゲート側壁への不純物の導入を、前記ソース領域および前記ドレイン領域への不純物イオン注入または前記ゲート電極への不純物イオン注入と同時に行うことを特徴とする。

【００１５】本発明は、ゲート側壁への不純物導入を、ソース領域およびドレイン領域への不純物イオン注入またはゲート電極への不純物イオン注入と同時に行うようにしたものである。

【００１６】したがって、ゲート側壁へイオン注入する独自の工程を必要としないので、製造工程数を減らすことができる。

【００１７】また、本発明のＭＯＳＦＥＴは、シリコン基板の上にゲート絶縁膜を介して設けられたゲート電極と、前記ゲート電極の側壁部に設けられたゲート側壁と、前記シリコン基板上に設けられたソース領域とドレイン領域とを有するＭＯＳＦＥＴにおいて、前記ゲート側壁が強誘電体材料により形成され、前記シリコン基板がｐ形の場合には前記ゲート電極から前記シリコン基板の方向に分極され、前記シリコン基板がｎ形の場合は前記シリコン基板からゲート電極の方向に分極されていることを特徴とする。

【００１８】本発明は、ゲート側壁に分極された強誘電体を用いているので、その分極方向により電子または正孔がゲート側壁とシリコン基板の界面のシリコン基板側に誘起され、その単位面積当たりの濃度は$1\times10^{14}cm^{-2}$程度となる。そして、この電子や正孔にはゲート側壁の方向に押し付けられるように力が働くため、これらの層はシート状に薄く形成され、その厚さは５ｎｍ以下となる。このため、この部分をソース領域領域やドレイン領域のゲート端として用いれば、５ｎｍ以下の極めて薄いソース領域・ドレイン領域端を形成することができ短チャネル効果を抑制することができる。

【００１９】また、本発明の実施態様によれば、前記ゲート側壁と前記ゲート電極の間、または前記ゲート側壁と前記シリコン基板の間、または前記ゲート側壁と前記ゲート電極および前記ゲート側壁と前記シリコン基板との間に絶縁膜が設けられている。

【００２０】本発明は、絶縁膜をゲート側壁とゲート電極またはゲート側壁とシリコン基板の間に設けるようにしたものである。したがって、ゲート側壁とゲート電極またはゲート側壁とシリコン基板との間の絶縁性を向上することができる。

【００２１】また、本発明のＭＯＳＦＥＴは、シリコン基板の上にゲート絶縁膜を介して設けられたゲート電極と、前記ゲート電極の側壁部に設けられ強誘電体材料により形成されたゲート側壁と、前記シリコン基板上に設けられたソース領域とドレイン領域とを有するＭＯＳＦＥＴの製造方法において、層間絶縁膜を前記シリコン基板の上に形成し、前記層間絶縁膜に前記シリコン基板へ通ずるコンタクト穴を形成し、前記コンタクト穴を金属で埋め込みコンタクト埋め込みとする工程と、前記ゲート側壁上部に前記層間絶縁膜を介して第１の電極を形成し、前記コンタクト埋め込みの上部に第２の電極を形成する工程と、前記第１の電極と前記第２の電極との間に電圧を印加し、前記ゲート側壁を分極する工程とを有することを特徴とする。

【００２２】本発明は、シリコン基板上に層間絶縁膜を形成し、その層間絶縁膜にシリコン基板と電気的に接続するためのコンタクト埋め込みを設けるとともに層間絶縁膜を介したゲート電極上部とコンタクト埋め込み上にそれぞれ電極を設けるようにしたものである。

【００２３】したがって、その設けられた２つの電極間に電圧を印加することにより、ゲート側壁を分極することができる。

【００２４】また、本発明のＭＯＳＦＥＴは、シリコン基板の上に複数のウェルが設けられ、前記各ウェル上に複数のゲート絶縁膜を介して設けられた複数のゲート電極と、前記各ゲート電極の側壁部に設けられ強誘電体材料により形成された複数のゲート側壁と、前記各ウェル上に設けられた複数のソース領域と複数のドレイン領域とを有するＭＯＳＦＥＴの製造方法において、層間絶縁膜を前記シリコン基板の上に形成し、前記層間絶縁膜に前記各ウェルへ通ずる複数のコンタクト穴を形成し、前記各コンタクト穴を金属で埋め込みコンタクト埋め込みとする工程と、前記各ゲート側壁上部に前記層間絶縁膜を介して複数の第１の電極を形成し、前記各コンタクト埋め込みの上部に複数の第２の電極を形成する工程と、前記各第１の電極どうしと前記各第２の電極どうしをそれぞれ配線により接続し、接続された前記各配線の間に電圧を印加し、前記各ゲート側壁を分極する工程とを有することを特徴とする。

【００２５】本発明は、１つのシリコン基板の複数のウェル上に設けられた複数のＭＯＳＦＥＴに対して、シリコン基板上に層間絶縁膜を形成し、その層間絶縁膜に各ウェルと電気的に接続するためのコンタクト埋め込みを設けるとともに層間絶縁膜を介したゲート電極上部とコンタクト埋め込み上にそれぞれ第１と第２の電極を設け、第１の電極どうしと第２の電極どうしを配線により接続したものである。

【００２６】したがって、その接続された２つの電極間に電圧を印加することにより、複数のＭＯＳＦＥＴの強誘電体側壁を同時に分極することができる。

【００２７】また、本発明の実施態様によれば、第１と

GF Exhibit 1124 - 1574/2704

第２の電極を除去する工程をさらに有する。
【００２８】本発明は、ゲート側壁の分極を行った後に第１と第２の電極を除去するようにして、以後のプロセスを進める上で障害とならないようにしたものである。したがて、ＭＯＳＦＥＴの製作が容易になる。
【００２９】また、本発明の実施態様によれば、前記ゲート側壁より外側のソース領域およびドレイン領域部が金属材料により形成されていることを特徴とする。
【００３０】本発明は、ソース領域およびドレイン領域を金属材料により形成するようにしたものである。したがって、イオン注入の工程が不要となりＭＯＳＦＥＴを製造するための工程数を減らすことができる。
【００３１】
【発明の実施の形態】次に、本発明の実施形態について図面を参照して詳細に説明する。
（第１の実施形態）図１は本発明の第１の実施形態のＭＯＳＦＥＴの製造方法を示す断面摸式図、図２は図１のＭＯＳＦＥＴの構造を示す断面摸式図である。
【００３２】本実施形態のＭＯＳＦＥＴの製造方法を図１を用いて説明する。
【００３３】本実施形態は、不純物濃度が1×10^{14}ｃｍ$^{-3}$程度のｐ型シリコンの基板１上に酸化シリコンでできた５ｎｍ厚のゲート絶縁膜２を形成し、絶縁膜２の上にｎ型ポリシリコン膜を２００ｎｍ形成した後、レジスト塗布、露光、現像工程をへてエッチングによりゲート電極３を形成する（図１（ａ））。
【００３４】次に、基板１上にノンドープのシリコンカーバイドを５０ｎｍ形成した後、異方性エッチングによりゲート側壁４を形成する（図１（ｂ））。
【００３５】この後、ＭＯＳＦＥＴ全面に砒素または燐をイオン注入することにより、ゲート電極３、ゲート側壁４への不純物導入と、基板１表面上にソース領域５およびドレイン領域６の形成を同時に行う（図１（ｃ））。この後、１０００℃、３０秒間の熱処理を行い不純物を活性化させる。
【００３６】上記の方法によれば、ゲート側壁４への不純物導入をソース領域５・ドレイン領域６へのイオン注入と同時に行うことができるので、工程数の増加を回避することができる。
【００３７】本実施形態のＭＯＳＦＥＴの構造を図２を用いて説明する。
【００３８】本実施形態のＭＯＳＦＥＴは、ゲート側壁４がシリコンよりバンドギャップの大きなシリコンカーバイドであるため、その中の電子はエネルギーの低いシリコンにより形成された基板１の表面に移動し、キャリヤ誘起層７が形成される。このキャリヤ誘起層７は電子の波動関数程度の広がりしか持たないために、その厚さは５ｎｍ以下と薄くなり短チャネル効果を抑制することができる。
【００３９】また、ゲート側壁４は半導体で形成されているため、伝導性をもつ可能性があり、その場合にはゲート側壁４はゲート電極３の一部となって実質上ゲート長が大きくなったり、ドレイン領域６との容量増加の原因となるため、ゲート側壁４は導電性をもたなくする必要がある。そのためには、ドナーやアクセプタが空乏化する程度にゲート側壁４の厚さを薄くする必要がある。
【００４０】しかし本実施形態では、ゲート側壁４の膜厚は５０ｎｍと薄いため、電子はすべて基板１に移動し、ゲート側壁４は空乏化し伝導性を持たなくなる。そのため、寄生容量の増加などによりＭＯＳＦＥＴの特性を劣化させることはない。
【００４１】本実施形態では、不純物をｎ型ＭＯＳＦＥＴの場合の導伝型として記述したが、ｐ型ＭＯＳＦＥＴの場合には、導伝型を逆にした不純物を用いればよい。
【００４２】また、ここではゲート側壁４の材料として、シリコンカーバイドを用いたが、ダイヤモンドやガリウムヒソ、インジウムリンなどシリコンよりバンドギャップの大きい材料を用いれば同様な効果が得られる。ただし、そのなかの元素がシリコン中に拡散しないようなプロセスや材料にする必要がある。
（第２の実施形態）図３は本発明の第２の実施形態のＭＯＳＦＥＴの構造を示す断面摸式図である。図２中と同番号は同じ構成要素を示す。
【００４３】本実施形態は、図２の第１の実施形態に対して、ゲート電極３の形成後にキャリヤが通過できない厚さ５ｎｍ程度の酸化シリコン膜を絶縁膜８として、ゲート側壁４とゲート電極３およびゲート側壁４と基板１との間に形成したものである。
【００４４】本実施形態は、絶縁膜８、ゲート側壁４を形成した後、ＭＯＳＦＥＴ全面に不純物をイオン注入することにより、第１の実施形態と同様にゲート側壁４に不純物を導入することができる。
【００４５】本実施形態のＭＯＳＦＥＴは、第１の実施形態と同様に短チャネル効果を抑制することができ、さらに絶縁膜８が存在するために、ゲート側壁４とゲート電極３およびゲート側壁４と基板１間の絶縁性を向上することができる。
【００４６】本実施形態ではゲート側壁４とゲート電極３およびゲート側壁４と基板１との間に絶縁膜８が設けられていたが、ゲート側壁４とゲート電極３の間またはゲート側壁４と基板１の間のみに絶縁膜８が設けられていてもよい。
（第３の実施形態）図４は本発明の第３の実施形態のＭＯＳＦＥＴの製造方法を示す断面摸式図、図５は図４のＭＯＳＦＥＴの強誘電体側壁４４の分極方法を示す断面模式図、図６は図４のＭＯＳＦＥＴの強誘電体側壁４４の分極方向を示す断面模式図、図７は図４のＭＯＳＦＥＴの構造を示す断面模式図である。
【００４７】本実施形態のＭＯＳＦＥＴの製造方法を図４を用いて説明する。

GF Exhibit 1124 - 1575/2704

【００４８】本実施形態は、不純物濃度が1×10^{14} cm^{-3}程度のｐ型シリコンの基板４１上に酸化シリコンでできた５ｎｍ厚のゲート絶縁膜４２、ｎ型ポリシリコン膜を２００ｎｍ形成した後、レジスト塗布、露光、現像工程をへてエッチングによりゲート電極４３を形成する（図4（ａ））。

【００４９】次に、ＰＺＴなどの強誘電体膜４０をゲート電極４３と基板４１の上に厚さ５０ｎｍで形成し（図４（ｂ））、異方性エッチングにより強誘電体側壁４４を形成する（図4（ｃ））。

【００５０】この後、基板４１の表面上に不純物をイオン注入することにより、ソース領域４５およびドレイン領域４６を形成することができる。このあと、１０００℃、３０秒間の熱処理を行い不純物を活性化させる。

【００５１】次に本実施形態のＭＯＳＦＥＴの強誘電体側壁４４の分極方法を図５を用いて説明する。図４中と同番号は同じ構成要素を示す。

【００５２】ＭＯＳＦＥＴを素子分離９３およびコンタクト層９４とともに基板４１に形成したあと、層間絶縁膜９９を形成し、基板４１へ通ずるコンタクト穴を形成し、それをタングステンなどで埋め込み、コンタクト埋め込み１００を形成する。

【００５３】素子分離９３は、SiO_2等により形成され、１つのチップ上に複数のＭＯＳＦＥＴを形成する場合等に、それぞれのＭＯＳＦＥＴどうしを電気的に分離するためのものである。

【００５４】コンタクト層９４は、コンタクト埋め込み１００と基板４１との間を電気的に低抵抗で接続するために、基板４１と同じ不純物を高濃度で導入した層である。

【００５５】その後、コンタクト埋め込み１００の上に電極１１３を形成し、層間絶縁膜９９を挟んだゲート電極９５上に電極１１２を形成する。

【００５６】そして、電極１１２と電極１１３の間に電圧を印加し、強誘電体側壁４４を分極する。電圧の印加の仕方は、ｎ型ＭＯＳＦＥＴでは基板４１に対して電極１１２を正にし、ｐ型ＭＯＳＦＥＴでは基板４１に対して電極１１２を負にすればよい。

【００５７】強誘電体側壁４４の分極は、図５の状態で行うか、または、さらにプロセスを進めた状態で行う。図５の状態で行う場合は、分極後に層間絶縁膜９９上に形成された電極１１２、１１３をエッチングにより除去しても、残しておいてもよい。しかし、電極１１２、１１３は除去したほうが以後のプロセスを進める上で障害とならずＭＯＳＦＥＴの製作が容易になる。

【００５８】本実施形態では、１つのＭＯＳＦＥＴに対する分極方法を示したが、１つの半導体の基板上に複数のＭＯＳＦＥＴが形成されている場合は、複数のＭＯＳＦＥＴの強誘電体側壁を同時に分極することが可能である。この場合、基板上に複数のウェルを形成し、そのそれぞれのウェル上に図５のようなＭＯＳＦＥＴを形成し、複数のＭＯＳＦＥＴのゲート電極の上に形成された電極どうしを配線で接続し、コンタクト埋め込みの上に形成された電極どうしを配線で接続し、それぞれの配線の間に電圧を印加すれば複数のＭＯＳＦＥＴの強誘電体側壁を同時に分極することができる。

【００５９】次に、本実施形態のＭＯＳＦＥＴにおける強誘電体側壁４４の分極の方向を図６を用いて説明する。図６において、強誘電体４４の中の矢印は分極方向を示している。図４中と同番号は同じ構成要素を示す。

【００６０】図６（ａ）はｎ型ＭＯＳＦＥＴにおける分極方向を示した図であり、強誘電体側壁４４の分極方向は下向きである。この場合、強誘電体側壁４４中の下側は正に帯電するため、それを打ち消すように基板に負の電荷（電子）が蓄積され、電子誘起層４９が形成される。

【００６１】図６（ｂ）はｐ型ＭＯＳＦＥＴにおける分極方向を示した図であり、強誘電体側壁４４の分極方向は上向きである。この場合、強誘電体側壁４４中の下側は負に帯電するため、それを打ち消すように基板に正の電荷（正孔）が蓄積され、正孔誘起層５０が形成される。

【００６２】また、上記の分極方向は基板４１に対し垂直な方向を向いているが、必ずしもその必要はなく、垂直から６０度程度傾いてもキャリヤは誘起することができるため問題はない。

【００６３】本実施形態のＭＯＳＦＥＴの構造を図７を用いて説明する。図４中と同番号は同じ構成要素を示す。

【００６４】本実施形態は、強誘電体側壁４４をゲート電極４３の側面に形成しているため、それをゲート電極４３から基板４１方向に平行に分極することにより基板４１の表面に電子が誘起され、キャリヤ誘起層４７が形成される。このキャリヤ誘起層４７は電子の波動関数程度の広がりしか持たないために、その厚さは５ｎｍ以下と薄く、短チャネル効果を抑制することができる。強誘電体側壁４４は伝導性をもたない絶縁体であるため、その形成による寄生容量の増加などのＭＯＳＦＥＴ特性を劣化することはない。

【００６５】ここでは、不純物はｎ型ＭＯＳＦＥＴを仮定して導伝型を記述したが、ｐ型ＭＯＳＦＥＴにおいては、導伝性が逆のものを用いればよい。

（第４の実施形態）図８は本発明の第４の実施形態のＭＯＳＦＥＴの構造を示す断面摸式図である。図７中と同番号は同じ構成要素を示す。

【００６６】本実施形態は、図７の第３の実施形態の構造に追加して、ゲート電極４３の形成後にキャリヤが通過できない５ｎｍ程度の厚さの酸化シリコン膜を絶縁膜４８として、強誘電体側壁４４とゲート電極４３および強誘電体側壁４４と基板４１の間に形成したものであ

GF Exhibit 1124 - 1576/2704

る。本実施形態のＭＯＳＦＥＴは、第４の実施形態のように短チャネル効果を抑制し、さらに絶縁膜４８が存在するために、強誘電体側壁４４とゲート電極４３や強誘電体側壁４４と基板４１間の絶縁性を向上することができる。

【００６７】本実施形態ではゲート側壁４４とゲート電極４３およびゲート側壁４４と基板４１との間に絶縁膜４８が設けられていたが、ゲート側壁４４とゲート電極４３の間またはゲート側壁４４と基板４１の間のみに絶縁膜４８が設けられていてもよい。

（第５の実施形態）図９は本発明の第５の実施形態のＭＯＳＦＥＴの構造を示す断面摸式図である。　本実施形態は、不純物濃度が$1\times10^{14}cm^{-3}$程度のｐ型シリコンの基板７１上に酸化シリコンでできた５ｎｍ厚のゲート絶縁膜７２、ｎ型ポリシリコン膜を２００ｎｍ形成した後、それをレジスト塗布、露光、現像工程をへてエッチングによりゲート電極７３を形成し、強誘電体のＰＺＴ膜１００ｎｍを形成したあと異方性エッチングにより強誘電体側壁７４を形成、その後チタンを全面に形成し、８００℃の熱処理により基板７１とチタンを反応させ、その後強誘電体側壁７４上のチタンの反応物およびチタンをフッ酸系のエッチング液により剥離し、チタンシリサイドでできた金属層のソース領域７５と金属層のドレイン領域７６を形成する。

【００６８】また、強誘電体側壁７４の下の基板７１の表面にはキャリヤ誘起層７７が形成され、その濃度は$1\times10^{14}cm^{-2}$程度である。

【００６９】本実施形態の構造では、キャリヤ誘起層７７の外側に金属層でできたソース領域７５とドレイン領域７６が形成されている。通常は金属とシリコンが接触している場合には、その間にショットキーバリヤというポテンシャル障壁が存在し、接触抵抗が生ずる。そして、この接触抵抗によりＭＯＳＦＥＴの特性が劣化する。但し、半導体側の不純物濃度が高い場合には、このポテンシャル障壁厚が薄くなるため、小さな接触抵抗になる。

【００７０】本実施形態の場合には、キャリヤ誘起層７７の濃度は非常に高く、単位体積当たりの濃度に換算すると$1\times10^{20}cm^{-3}$程度のため、接触抵抗はＭＯＳＦＥＴのチャネル抵抗に比べるとほとんどゼロに近く、ＭＯＳＦＥＴの特性には問題とならない。そして、短チャネル効果については、第４の実施形態と同じく抑制することができる。そのため、ソース領域７５、ドレイン領域７６を金属層により形成すると、短チャネル効果を抑制できるとともに、イオン注入の工程を不要とすることができＭＯＳＦＥＴを製造するための工程数を減らすことができる。

【００７１】本実施形態では、ゲート側壁として強誘電体を用いた場合について述べたが、第１の実施形態のようにシリコンよりバンドギャップが大きく、不純物をドープした半導体を用いた場合でも同様な効果がある。

【００７２】

【発明の効果】以上説明したように、本発明は、ゲート端の基板上部に浅いソース領域、ドレイン領域の一部を形成することができ、０．１μｍ以下のゲート長をもつＭＯＳＦＥＴにおいて、寄生抵抗を増加することなく短チャネル効果を抑制することができるという効果を有する。

【図面の簡単な説明】

【図１】本発明の第１の実施形態のＭＯＳＦＥＴの製造方法を示す断面模式図である。

【図２】図１のＭＯＳＦＥＴの構造を示す断面模式図である。

【図３】本発明の第２の実施形態のＭＯＳＦＥＴの構造を示す断面模式図である。

【図４】本発明の第３の実施形態のＭＯＳＦＥＴの製造方法を示す断面模式図である。

【図５】図４のＭＯＳＦＥＴの強誘電体側壁４４の分極方法を示す断面模式図である。

【図６】図４のＭＯＳＦＥＴの強誘電体側壁４４の分極方向を示す断面模式図である。

【図７】図４のＭＯＳＦＥＴの構造を示す断面模式図である。

【図８】本発明の第４の実施形態のＭＯＳＦＥＴの構造を示す断面模式図である。

【図９】本発明の第５の実施形態のＭＯＳＦＥＴの構造を示す断面模式図である。

【図１０】従来のＭＯＳＦＥＴの構造を示す断面模式図である。

【図１１】従来のＭＯＳＦＥＴの構造を示す断面模式図である。

【図１２】従来のＭＯＳＦＥＴの構造を示す断面模式図である。

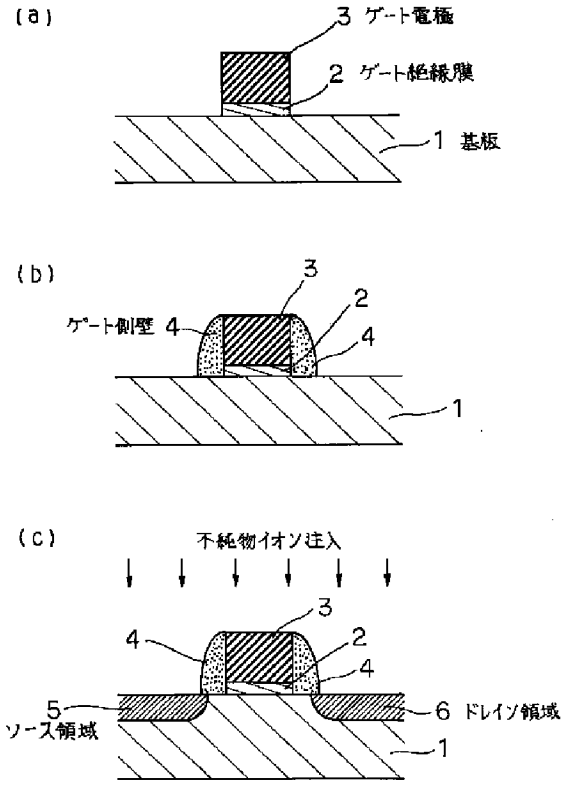
【符号の説明】

１　基板
２　ゲート絶縁膜
３　ゲート電極
４　ゲート側壁
５　ソース領域
６　ドレイン領域
７　キャリヤ誘起層
８　絶縁膜
４０　強誘電体膜
４１　基板
４２　ゲート絶縁膜
４３　ゲート電極
４４　強誘電体側壁
４５　ソース領域
４６　ドレイン領域
４７　キャリヤ誘起層

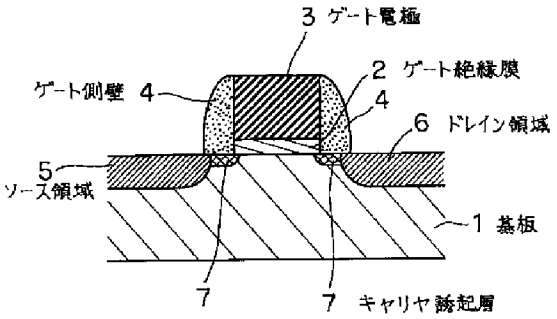
GF Exhibit 1124 - 1577/2704

４８　絶縁膜
４９　電子誘起層
５０　正孔誘起層
７１　基板
７２　ゲート絶縁膜
７３　ゲート電極
７４　強誘電体側壁
７５　ソース領域
７６　ドレイン領域
７７　キャリヤ誘起層
９３　素子分離
９４　コンタクト層
９９　層間絶縁膜
１００　コンタクト埋め込み
１０１　基板
１０２　ゲート絶縁膜
１０３　ゲート電極
１０４　不純物イオン注入層
１０５　ソース領域
１０６　ドレイン領域
１０７　側壁
１０８　絶縁膜
１０９　サブゲート
１１０　不純物拡散層
１１１　キャリア誘起層
１１２、１１３　電極

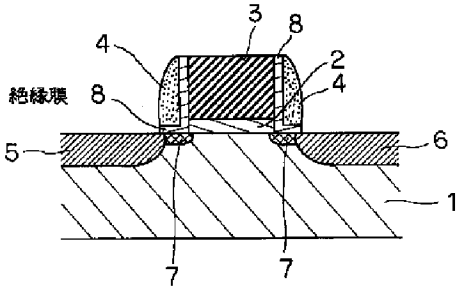
【図１】



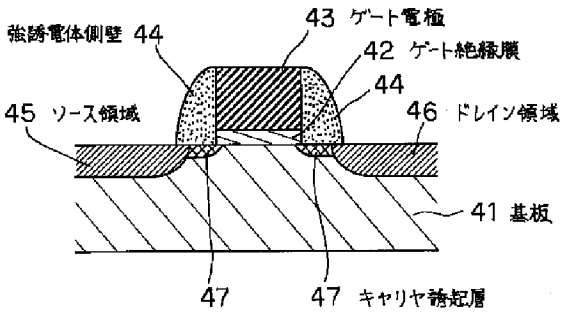
【図２】



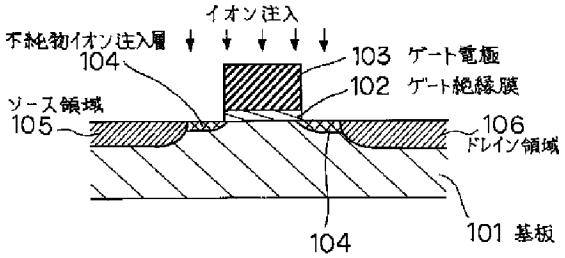
【図３】



【図７】

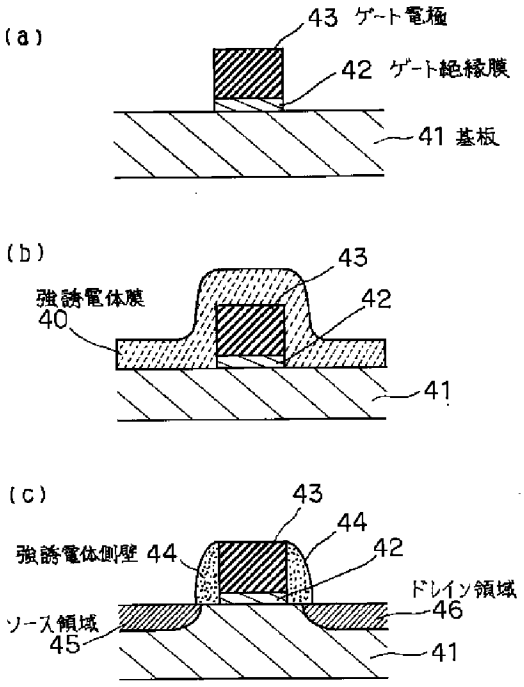


【図１０】

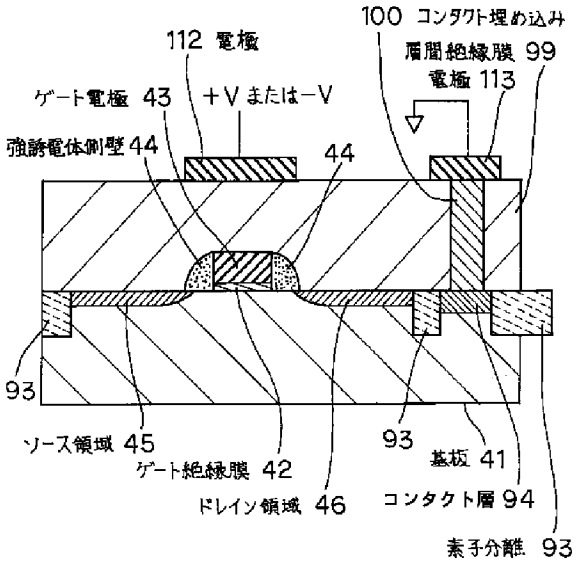


GF Exhibit 1124 - 1578/2704

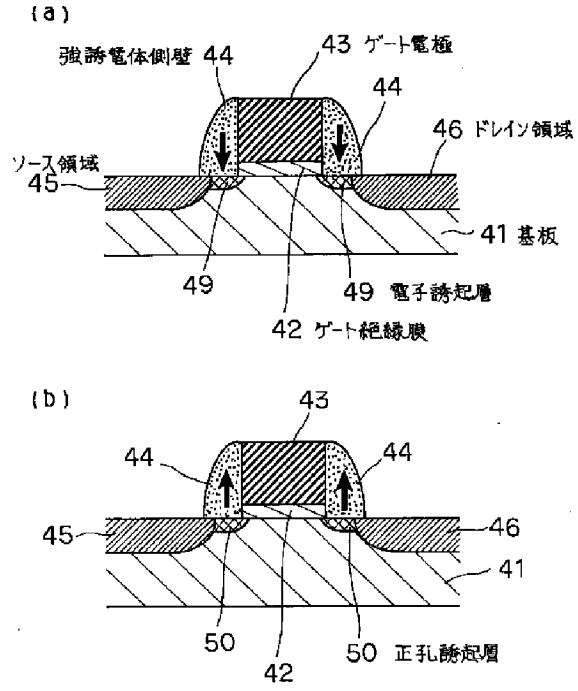
【図4】



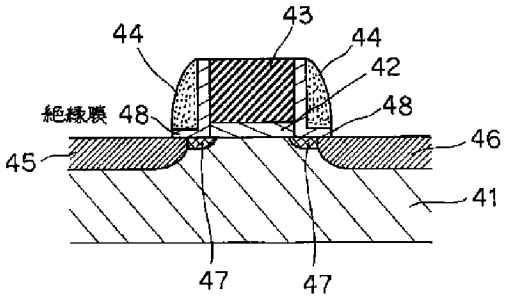
【図5】



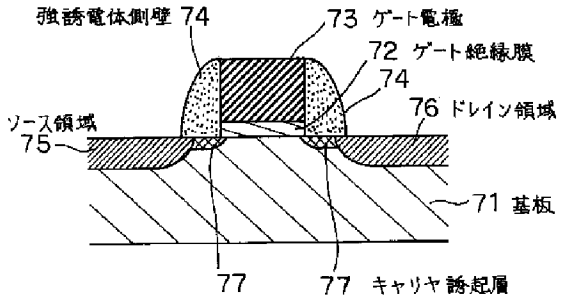
【図6】



【図8】

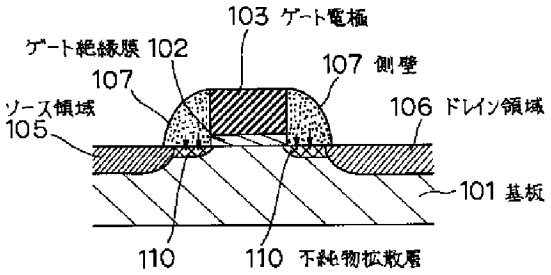


【図9】

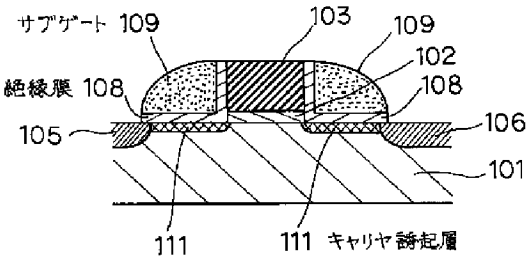


GF Exhibit 1124 - 1579/2704

【図１１】



【図１２】



GF Exhibit 1124 - 1580/2704

Europäisches Patentamt
European Patent Office
Office européen des brevets

Espacenet

JPH10209445A MOSFET AND MANUFACTURE THEREOF

Applicants: NEC CORP

Inventors: FURUKAWA AKIO

Classifications:
IPC ***H01L21/336; H01L29/78;*** (IPC1-7): H01L21/336; H01L29/78;

Priorities: JP865397A 1997-01-21

Application: JPH10209445A·1997-01-21

Publication: JPH10209445A·1998-08-07

Published as: JPH10209445A;**JP3060976B2**

MOSFET AND MANUFACTURE THEREOF

Abstract

PROBLEM TO BE SOLVED: To reailize the junction depth of a diffused layer, which is enough for inhibiting the short tunnel effect of a MOSFET, without causing problems, such as a reduction in the switching rate of the MOSFET due to an increase in a parasitic capacitance and the complication of the manufacturing process of the MOSFET. SOLUTION: In a MOSFET, which has a gate electrode 3 on a silicon substrate 1 via a gate insulating film 3, gate sidewalls on the substrate 1 and source and drain regions 5 and 6 in the substrate 1, the sidewalls 4 are formed of a non-conductive semiconductor layer having a band gap larger than that of a silicon layer and at the same time, impurities are introduced in the substrate 1. As the semiconductor layer having a band gap larger than of the silicon layer is used for the gate sidewalls 4, carriers are moved from the sidewalls 4 to the interiors of the upper parts, which are located under the sidewalls 4, of the substrate 1 due to a difference between the energy of impurities doped to the sidewalls 4 and the energy of the conduction band of the substrate 1, but as such a force that the carriers are pressed in the directions of the sidewalls 4 works on the carriers, the carriers 4 are thinly stored in the substrate 1 in a sheet type, the ends, which have a very thin thickness of 5nm or thinner, of the regions 5 and 6 can be formed and the short channel effect of the MOSFET can be inhibited.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION JPH10209445

[0001]
BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a MOSFET and a manufacturing method thereof, and more particularly to a MOSFET having a structure in which a source region and a drain region are shallowly formed and a manufacturing method thereof.

[0002]

2. Description of the Related Art A phenomenon which becomes a problem in miniaturizing a gate length of a MOSFET to 0.1 .mu.m or less is a short channel effect in which a threshold value is reduced as the gate length is miniaturized. In order to suppress this short channel effect, it is effective to make the junction depth of the diffusion layer, especially the diffusion layer near the gate end, shallow in the source region and drain region structure.

[0003]

As a conventional method for forming the junction depth of the diffusion layer shallow, there is a low energy ion implantation method as shown in FIG. This method is a method of implanting impurity ions into the source region 105 and the drain region 106 beside the gate electrode 103 on the surface of the substrate 101 with implantation energy as small as possible, for example, about 10 keV, and the depth of the impurity ion implantation layer 104. Can be made as shallow

GF Exhibit 1124 - 1582/2704

as several tens of nm.

[0004]

As a conventional method for further reducing the junction depth of the diffusion layer, a solid layer diffusion method as shown in FIG. 11 is proposed in, for example, Japanese Unexamined Patent Publication No. 7-312422. According to this method, a side wall 107 is first formed as an insulating film containing impurities such as phosphorus silicate glass (PSG) or boron silicate glass (BSG) next to the gate electrode 103, and then the impurities in the side wall 107 are treated by heat treatment to the substrate. Diffuses into 101. Thereby, the depth of the diffusion layer can be set to about 10 nm to 40 nm, and a shallower diffusion layer can be obtained as compared with the ion implantation method.

[0005]

Further, as a method for further reducing the junction depth between the source region and the drain region, a method as shown in FIG. 12 is proposed in, for example, Japanese Patent Laid-Open No. 1-125977. In this method, a conductive sub-gate 109 made of polysilicon is provided beside the gate electrode 103 via an insulating film 108, and a voltage is applied to the conductive sub-gate 109. According to this method, the substrate 101 under the sub-gate 109 is provided. A carrier inducing layer 111, which is an inversion layer in which carriers are induced and which is an inversion layer, is formed to form an extremely shallow conductive layer.

[0006]

Further, as another structure of a MOSFET having a shallow junction in which an inversion layer is formed, for example, in JP-A-1-232765, a material having a different work function, for example, a second gate electrode beside the first gate electrode is used. When the first gate electrode is formed of p-type silicon, n-type silicon is used for the second gate electrode, and when the first gate electrode is formed of n-type silicon, platinum is used for the second gate electrode. It is proposed that an inversion layer is formed under the second gate electrode by using it.

[0007]

GF Exhibit 1124 - 1583/2704

The above-mentioned conventional MOSFET has the following problems.

(1) In the low energy ion implantation method or the solid phase diffusion method, the junction depth of the diffusion layer cannot be 10 nm or less, and the sufficiently short channel effect can be suppressed in the MOSFET having a gate length of 0.1 μm or less. Can not. (2) In the structure in which the subgate is provided and the voltage is applied to form the inversion layer, the junction depth is shallow, but the voltage must be continuously applied to the subgate during operation, and the subgate, the gate electrode, and the subgate Since the parasitic capacitance is formed between the drain regions, the switching speed is reduced. (3) In the structure in which the second gate electrode having a different work function is provided, since the second gate electrode is connected to the gate electrode and has conductivity, the voltage is applied to the second gate electrode when the gate voltage is applied. Therefore, there is a parasitic capacitance between the second gate electrode and the channel, which causes a decrease in switching speed. Further, when the conductivity types of the gate electrode and the second gate electrode are different, it is necessary to introduce different impurities into the respective gate electrodes, which complicates the MOSFET forming process.

[0008]

An object of the present invention is to provide a MOSFET in which a junction depth of a diffusion layer sufficient to suppress a short channel effect is realized without causing problems such as a decrease in switching speed due to an increase in parasitic capacitance and a complicated manufacturing process. That is.

[0009]

To achieve the above object, a MOSFET of the present invention is provided with a gate electrode provided on a silicon substrate via a gate insulating film and a sidewall portion of the gate electrode. In a MOSFET having a gate side wall and a source region and a drain region provided on the silicon substrate, the gate side wall is formed of a non-conductive semiconductor layer having a band gap larger than that of silicon and impurities are introduced. It is characterized by

[0010]

Since the present invention uses a semiconductor having a bandgap larger than that of silicon on the gate side wall, when the impurity doped on the gate side wall is a donor, the energy of the electron is higher than the energy level of the conduction band of the silicon substrate. In the case of an acceptor, it is lower than the energy level of the valence band of the silicon substrate.

GF Exhibit 1124 - 1584/2704

Therefore, if the side wall of the gate is doped with a donor, electrons move and accumulate from the side wall of the gate to the silicon substrate therebelow due to the energy difference between the energy and the conduction band of the silicon substrate.

On the other hand, if the acceptor is doped, holes move and accumulate. Since a force acts on these electrons and holes so that they are pressed toward the side wall of the gate, these accumulation layers are thinly formed in a sheet shape, and the thickness thereof is 5 nm or less. Therefore, if this portion is used as the gate end of the source region or the drain region, an extremely thin source / drain region end of 5 nm or less can be formed, and the short channel effect can be suppressed.

[0011]
According to an embodiment of the present invention, the gate sidewalls are depleted to render them non-conductive.

[0012]
According to an embodiment of the present invention, between the gate sidewall and the gate electrode, or between the gate sidewall and the silicon substrate, or between the gate sidewall and the gate electrode and the gate sidewall and the silicon substrate. An insulating film is provided between them.

[0013]

In the present invention, an insulating film is provided between the gate side wall and the gate electrode or between the gate side wall and the silicon substrate.

Therefore, the insulation between the gate sidewall and the gate electrode or between the gate sidewall and the silicon substrate can be improved.

[0014]
Further, a method for manufacturing a MOSFET according to the present invention includes a gate electrode provided on a silicon substrate via a gate insulating film, and a semiconductor

GF Exhibit 1124 - 1585/2704

provided on a sidewall portion of the gate electrode and having a band gap larger than that of silicon and being non-conductive. In a method of manufacturing a MOSFET having a gate side wall formed of a layer and having impurities introduced therein, and a source region and a drain region provided on the silicon substrate, the impurity is introduced into the gate side wall by the source. The impurity ion implantation into the region and the drain region or the impurity ion implantation into the gate electrode is performed simultaneously.

[0015]
According to the present invention, the impurity is introduced into the side wall of the gate simultaneously with the impurity ion implantation into the source region and the drain region or the impurity ion implantation into the gate electrode.

[0016]
Therefore, it is possible to reduce the number of manufacturing steps, because a unique step of implanting ions into the gate sidewall is not required.

[0017]
Further, the MOSFET of the present invention includes a gate electrode provided on a silicon substrate via a gate insulating film, a gate sidewall provided on a sidewall portion of the gate electrode, and a source region provided on the silicon substrate. And a drain region, the gate sidewall is formed of a ferroelectric material, and when the silicon substrate is p-type, it is polarized in the direction from the gate electrode to the silicon substrate, and the silicon substrate is n-type. In this case, the polarization is performed in the direction from the silicon substrate to the gate electrode.

[0018]

Since the present invention uses the polarized ferroelectric on the gate sidewall, electrons or holes are induced on the silicon substrate side of the interface between the gate sidewall and the silicon substrate depending on the polarization direction, and the concentration per unit area is It will be about 1 x 1014 cm-2.

Then, a force acts on the electrons and holes so that they are pressed toward the side wall of the gate, so that these layers are thinly formed in a sheet shape, and the thickness thereof is 5 nm or less.

GF Exhibit 1124 - 1586/2704

Therefore, if this portion is used as the gate end of the source region or drain region, an extremely thin source / drain region end of 5 nm or less can be formed, and the short channel effect can be suppressed.

[0019]
According to an embodiment of the present invention, between the gate sidewall and the gate electrode, or between the gate sidewall and the silicon substrate, or between the gate sidewall and the gate electrode and the gate sidewall and the silicon substrate. An insulating film is provided between them.

[0020]

In the present invention, an insulating film is provided between the gate side wall and the gate electrode or between the gate side wall and the silicon substrate.

Therefore, the insulation between the gate sidewall and the gate electrode or between the gate sidewall and the silicon substrate can be improved.

[0021]
Further, the MOSFET of the present invention includes a gate electrode provided on a silicon substrate via a gate insulating film, a gate sidewall formed on a sidewall portion of the gate electrode and made of a ferroelectric material, and the silicon substrate. In a method of manufacturing a MOSFET having a source region and a drain region provided above, an interlayer insulating film is formed on the silicon substrate, a contact hole communicating with the silicon substrate is formed in the interlayer insulating film, and the contact is formed. Filling the hole with a metal to fill the contact; forming a first electrode on the upper portion of the gate sidewall through the interlayer insulating film; forming a second electrode on the upper portion of the contact filling; A voltage is applied between the first electrode and the second electrode to polarize the side wall of the gate.

[0022]
According to the present invention, an interlayer insulating film is formed on a silicon substrate, a contact buried for electrically connecting to the silicon substrate is provided in the interlayer

GF Exhibit 1124 - 1587/2704

insulating film, and a gate electrode upper part and a contact buried via the interlayer insulating film are provided respectively. An electrode is provided.

[0023]
Therefore, the gate sidewall can be polarized by applying a voltage between the two electrodes provided.

[0024]
Further, in the MOSFET of the present invention, a plurality of wells are provided on a silicon substrate, a plurality of gate electrodes provided on each of the wells via a plurality of gate insulating films, and a sidewall portion of each of the gate electrodes. In a method of manufacturing a MOSFET having a plurality of gate sidewalls formed of a ferroelectric material and a plurality of source regions and a plurality of drain regions provided on each well, an interlayer insulating film is formed on the silicon substrate. Forming a plurality of contact holes in the interlayer insulating film leading to the respective wells, filling the contact holes with a metal to form a contact buried, and forming the contact insulating film on the upper side wall of each gate via the interlayer insulating film. Forming a plurality of first electrodes and forming a plurality of second electrodes on top of the respective contact embeddings, and connecting the first electrodes to the second electrodes by wiring. And applying a voltage between the connected wirings to polarize the sidewalls of the gates.

[0025]
The present invention forms an interlayer insulating film on a silicon substrate for a plurality of MOSFETs provided on a plurality of wells of one silicon substrate, and electrically connects each well to the interlayer insulating film. In this structure, contact embedding is provided, and first and second electrodes are respectively provided on the upper part of the gate electrode and the contact embedding via the interlayer insulating film, and the first electrode and the second electrode are connected by wiring.

[0026]
Therefore, by applying a voltage between the two connected electrodes, it is possible to polarize the ferroelectric sidewalls of the plurality of MOSFETs at the same time.

[0027]
In addition, according to the embodiment of the present invention, the method further includes the step of removing the first and second electrodes.

GF Exhibit 1124 - 1588/2704

[0028]

According to the present invention, the first and second electrodes are removed after the polarization of the gate sidewall so as not to hinder the subsequent process.

Therefore, the manufacture of the MOSFET becomes easy.

[0029]
According to an embodiment of the present invention, the source region and the drain region outside the gate sidewall are formed of a metal material.

[0030]

In the present invention, the source region and the drain region are made of a metal material.

Therefore, the step of ion implantation becomes unnecessary and the number of steps for manufacturing MOSFET can be reduced.

[0031]

DESCRIPTION OF THE PREFERRED EMBODIMENTS Next, embodiments of the present invention will be described in detail with reference to the drawings.

(First Embodiment) FIG. 1 is a schematic sectional view showing a method for manufacturing a MOSFET according to a first embodiment of the present invention, and FIG. 2 is a schematic sectional view showing the structure of the MOSFET shown in FIG.

[0032]
A method of manufacturing the MOSFET of this embodiment will be described with reference to

GF Exhibit 1124 - 1589/2704

FIG.

[0033]
In this embodiment, a 5 nm-thick gate insulating film 2 made of silicon oxide is formed on a p-type silicon substrate 1 having an impurity concentration of about 1 × 10 14 cm −3, and an n-type polysilicon film is formed on the insulating film 2. After 200 nm is formed, the gate electrode 3 is formed by etching through resist coating, exposure, and development steps (FIG. 1A).

[0034]
Next, after forming 50 nm of non-doped silicon carbide on the substrate 1, the gate sidewall 4 is formed by anisotropic etching (FIG. 1B).

[0035]

After that, arsenic or phosphorus is ion-implanted into the entire surface of the MOSFET to simultaneously introduce impurities into the gate electrode 3 and the gate sidewall 4 and simultaneously form the source region 5 and the drain region 6 on the surface of the substrate 1 (see FIG. c)).

After that, heat treatment is performed at 1000 ° C. for 30 seconds to activate the impurities.

[0036]
According to the above method, the impurity can be introduced into the gate sidewall 4 at the same time as the ion implantation into the source region 5 and the drain region 6, so that an increase in the number of steps can be avoided.

[0037]
The structure of the MOSFET of this embodiment will be described with reference to FIG.

[0038]

GF Exhibit 1124 - 1590/2704

In the MOSFET of the present embodiment, since the gate sidewall 4 is silicon carbide having a bandgap larger than that of silicon, electrons therein move to the surface of the substrate 1 formed of silicon having low energy, and the carrier inducing layer 7 is formed. To be done.

Since the carrier inducing layer 7 has a spread of only about a wave function of electrons, its thickness is as thin as 5 nm or less, and the short channel effect can be suppressed.

[0039]

Further, since the gate side wall 4 is formed of a semiconductor, it may have conductivity, and in that case, the gate side wall 4 becomes a part of the gate electrode 3 to substantially increase the gate length and the drain length. The gate sidewall 4 needs to have no conductivity because it causes an increase in capacitance with the region 6.

For that purpose, it is necessary to reduce the thickness of the gate side wall 4 to the extent that the donor and the acceptor are depleted.

[0040]

However, in this embodiment, since the thickness of the gate side wall 4 is as thin as 50 nm, all the electrons move to the substrate 1 and the gate side wall 4 is depleted and has no conductivity.

Therefore, the characteristics of the MOSFET are not deteriorated due to an increase in parasitic capacitance.

[0041]
In this embodiment, the impurity is described as the conductivity type in the case of the n-type MOSFET, but in the case of the p-type MOSFET, the impurity having the opposite conductivity type may be used.

[0042]

GF Exhibit 1124 - 1591/2704

Further, although silicon carbide is used as the material of the gate side wall 4 here, the same effect can be obtained by using a material having a band gap larger than that of silicon such as diamond, gallium arsenide, and indium phosphide.

However, it is necessary to use a process or material that does not allow the elements in it to diffuse into silicon.

(Second Embodiment) FIG. 3 is a schematic sectional view showing the structure of a MOSFET according to a second embodiment of the present invention.

The same numbers as in FIG. 2 indicate the same components.

[0043]
This embodiment is different from the first embodiment in FIG. 2 in that the insulating film 8 is a silicon oxide film having a thickness of about 5 nm through which carriers cannot pass after the gate electrode 3 is formed, and the gate sidewall 4 and the gate electrode 3 and the gate are formed. It is formed between the side wall 4 and the substrate 1.

[0044]
In the present embodiment, after forming the insulating film 8 and the gate side wall 4, the impurities can be ion-implanted into the entire surface of the MOSFET to introduce the impurity into the gate side wall 4 as in the first embodiment.

[0045]
The MOSFET of the present embodiment can suppress the short channel effect as in the first embodiment, and since the insulating film 8 is present, the gate side wall 4 and the gate electrode 3 and the gate side wall 4 and the substrate 1 are separated from each other. The insulating property of can be improved.

[0046]

GF Exhibit 1124 - 1592/2704

In this embodiment, the insulating film 8 is provided between the gate sidewall 4 and the gate electrode 3 and between the gate sidewall 4 and the substrate 1. However, between the gate sidewall 4 and the gate electrode 3 or between the gate sidewall 4 and the substrate 1. The insulating film 8 may be provided only on the above.

(Third Embodiment) FIG. 4 is a schematic sectional view showing a method for manufacturing a MOSFET according to a third embodiment of the present invention, and FIG. 5 is a schematic sectional view showing a polarization method for a ferroelectric sidewall 44 of the MOSFET shown in FIG. 6 is a schematic sectional view showing the polarization direction of the ferroelectric sidewall 44 of the MOSFET of FIG. 4, and FIG. 7 is a schematic sectional view showing the structure of the MOSFET of FIG.

[0047]
A method of manufacturing the MOSFET of this embodiment will be described with reference to FIG.

[0048]
In this embodiment, a 5 nm-thick gate insulating film 42 made of silicon oxide and an n-type polysilicon film are formed to a thickness of 200 nm on a p-type silicon substrate 41 having an impurity concentration of about 1 × 10 14 cm −3, and then resist coating is performed. The gate electrode 43 is formed by etching through the exposure and development processes (FIG. 4A).

[0049]
Next, a ferroelectric film 40 such as PZT is formed on the gate electrode 43 and the substrate 41 with a thickness of 50 nm (FIG. 4B), and the ferroelectric sidewall 44 is formed by anisotropic etching (FIG. 4B). 4 (c)).

[0050]

After that, the source region 45 and the drain region 46 can be formed by ion-implanting impurities on the surface of the substrate 41.

Then, heat treatment is performed at 1000 ° C. for 30 seconds to activate the impurities.

GF Exhibit 1124 - 1593/2704

[0051]

Next, a polarization method of the ferroelectric sidewall 44 of the MOSFET of this embodiment will be described with reference to FIG.

The same numbers as in FIG. 4 indicate the same components.

[0052]

After the MOSFET is formed on the substrate 41 together with the element isolation 93 and the contact layer 94, an interlayer insulating film 99 is formed, a contact hole leading to the substrate 41 is formed, and it is filled with tungsten or the like to form a contact embedding 100.

[0053]

The element isolation 93 is formed of SiO2 or the like and is for electrically isolating each MOSFET when a plurality of MOSFETs are formed on one chip.

[0054]

The contact layer 94 is a layer in which the same impurity as that of the substrate 41 is introduced at a high concentration in order to electrically connect the contact embedding 100 and the substrate 41 with low resistance.

[0055]

After that, the electrode 113 is formed on the contact embedding 100, and the electrode 112 is formed on the gate electrode 95 with the interlayer insulating film 99 sandwiched therebetween.

[0056]

Then, a voltage is applied between the electrode 112 and the electrode 113 to polarize the ferroelectric side wall 44.

GF Exhibit 1124 - 1594/2704

The voltage may be applied by making the electrode 112 positive with respect to the substrate 41 in the n-type MOSFET and making the electrode 112 negative with respect to the substrate 41 in the p-type MOSFET.

[0057]

The polarization of the ferroelectric side wall 44 is performed in the state of FIG. 5 or in the state where the process is further advanced.

When performing in the state of FIG. 5, the electrodes 112 and 113 formed on the interlayer insulating film 99 after polarization may be removed by etching or may be left.

However, removal of the electrodes 112 and 113 does not hinder the subsequent process and facilitates the manufacture of the MOSFET.

[0058]

In the present embodiment, the polarization method for one MOSFET is shown, but when a plurality of MOSFETs are formed on one semiconductor substrate, it is possible to simultaneously polarize the ferroelectric sidewalls of the plurality of MOSFETs. is there.

In this case, a plurality of wells are formed on the substrate, MOSFETs as shown in FIG. 5 are formed on the respective wells, electrodes formed on the gate electrodes of the plurality of MOSFETs are connected by wiring, and contacts are formed. If the electrodes formed on the buried layers are connected by wirings and a voltage is applied between the wirings, the ferroelectric sidewalls of a plurality of MOSFETs can be polarized at the same time.

[0059]

Next, the polarization direction of the ferroelectric sidewall 44 in the MOSFET of this embodiment will be described with reference to FIG.

GF Exhibit 1124 - 1595/2704

In FIG. 6, the arrow in the ferroelectric substance 44 indicates the polarization direction.

The same numbers as in FIG. 4 indicate the same components.

[0060]

FIG. 6A is a diagram showing the polarization direction in the n-type MOSFET, and the polarization direction of the ferroelectric side wall 44 is downward.

In this case, since the lower side of the ferroelectric side wall 44 is positively charged, negative charges (electrons) are accumulated in the substrate so as to cancel it and the electron inducing layer 49 is formed.

[0061]

FIG. 6B is a diagram showing the polarization direction in the p-type MOSFET, and the polarization direction of the ferroelectric side wall 44 is upward.

In this case, since the lower side of the ferroelectric side wall 44 is negatively charged, positive charges (holes) are accumulated in the substrate so as to cancel it and the hole inducing layer 50 is formed.

[0062]

Further, although the above polarization direction is perpendicular to the substrate 41, this is not always necessary, and there is no problem because carriers can be induced even if they are inclined by about 60 degrees from the vertical.

[0063]

GF Exhibit 1124 - 1596/2704

The structure of the MOSFET of this embodiment will be described with reference to FIG.

The same numbers as in FIG. 4 indicate the same components.

[0064]

In this embodiment, since the ferroelectric side wall 44 is formed on the side surface of the gate electrode 43, electrons are induced on the surface of the substrate 41 by polarization of the ferroelectric side wall 44 parallel to the direction of the substrate 41 from the gate electrode 43, and carrier The induction layer 47 is formed.

Since the carrier inducing layer 47 has a spread of only about the wave function of electrons, its thickness is as thin as 5 nm or less, and the short channel effect can be suppressed.

Since the ferroelectric side wall 44 is an insulator having no conductivity, it does not deteriorate MOSFET characteristics such as an increase in parasitic capacitance due to its formation.

[0065]

Here, the conductivity is described assuming that the impurity is an n-type MOSFET, but in the p-type MOSFET, an impurity having an opposite conductivity may be used.

(Fourth Embodiment) FIG. 8 is a schematic sectional view showing the structure of a MOSFET according to a fourth embodiment of the present invention.

The same numbers as in FIG. 7 indicate the same components.

[0066]

In this embodiment, in addition to the structure of the third embodiment of FIG. 7, the

GF Exhibit 1124 - 1597/2704

ferroelectric side wall 44 is formed by using a silicon oxide film having a thickness of about 5 nm through which the carriers cannot pass after forming the gate electrode 43 as the insulating film 48. And the gate electrode 43 and the ferroelectric side wall 44 and the substrate 41.

The MOSFET according to the present embodiment suppresses the short channel effect as in the fourth embodiment, and further has the insulating film 48. Therefore, the ferroelectric side wall 44 and the gate electrode 43 or the ferroelectric side wall 44 and the substrate 41. The insulation between them can be improved.

[0067]

In this embodiment, the insulating film 48 is provided between the gate sidewall 44 and the gate electrode 43 and between the gate sidewall 44 and the substrate 41. However, between the gate sidewall 44 and the gate electrode 43 or between the gate sidewall 44 and the substrate 41. The insulating film 48 may be provided only on the above.

(Fifth Embodiment) FIG. 9 is a schematic sectional view showing the structure of a MOSFET according to a fifth embodiment of the present invention. In this embodiment, a 5 nm-thick gate insulating film 72 made of silicon oxide and an n-type polysilicon film are formed to a thickness of 200 nm on a p-type silicon substrate 71 having an impurity concentration of about 1 × 10 14 cm −3, and then the resist is used as a resist. The gate electrode 73 is formed by etching through the steps of coating, exposing, and developing, the ferroelectric PZT film 100 nm is formed, and then the ferroelectric side wall 74 is formed by anisotropic etching, and then titanium is formed on the entire surface. The substrate 71 and titanium are reacted by a heat treatment at 800 ° C., and then the titanium reactant and titanium on the ferroelectric side wall 74 are stripped off by a hydrofluoric acid-based etching solution to form a source region 75 of a metal layer made of titanium silicide. And a drain region 76 of the metal layer is formed.

[0068]
A carrier inducing layer 77 is formed on the surface of the substrate 71 below the ferroelectric side wall 74, and its concentration is about 1 × 10 14 cm −2.

[0069]

GF Exhibit 1124 - 1598/2704

In the structure of this embodiment, the source region 75 and the drain region 76 made of a metal layer are formed outside the carrier inducing layer 77.

Usually, when metal and silicon are in contact with each other, a potential barrier called a Schottky barrier exists between them, and contact resistance occurs. The contact resistance deteriorates the characteristics of the MOSFET. However, when the impurity concentration on the semiconductor side is high, this potential barrier thickness becomes thin, resulting in a small contact resistance.

[0070]

In the case of the present embodiment, the concentration of the carrier inducing layer 77 is very high, and when converted into the concentration per unit volume, it is about $1 \times 10\ 20\ \mathrm{cm}\ -3$, so the contact resistance is almost zero compared to the channel resistance of the MOSFET. , MOSFET characteristics do not matter. Then, the short channel effect can be suppressed similarly to the fourth embodiment. Therefore, when the source region 75 and the drain region 76 are formed of a metal layer, the short channel effect can be suppressed, the step of ion implantation can be omitted, and the number of steps for manufacturing the MOSFET can be reduced.

[0071]

In the present embodiment, the case where the ferroelectric is used as the gate sidewall has been described. However, similar to the first embodiment, the band gap is larger than that of silicon, and the same effect can be obtained when a semiconductor doped with impurities is used. ..

[0072]

As described above, according to the present invention, it is possible to form a part of the shallow source region and the drain region on the upper part of the substrate at the gate end, and in the MOSFET having the gate length of 0.1 μm or less, the parasitic It has an effect that the short channel effect can be suppressed without increasing the resistance.

GF Exhibit 1124 - 1599/2704

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

CLAIMS JPH10209445

1.
In a MOSFET having a gate electrode provided on a silicon substrate via a gate insulating film, a gate sidewall provided on a sidewall of the gate electrode, and a source region and a drain region provided on the silicon substrate. A MOSFET characterized in that the gate side wall is formed of a non-conductive semiconductor layer having a band gap larger than that of silicon and impurities are introduced.

2.
The MOSFET according to claim 1, wherein the gate sidewall is depleted to be non-conductive.

3.
An insulating film is provided between the gate sidewall and the gate electrode, between the gate sidewall and the silicon substrate, or between the gate sidewall and the gate electrode and between the gate sidewall and the silicon substrate. 1. The MOSFET according to 1 or 2.

4.
A gate electrode provided on a silicon substrate via a gate insulating film and a sidewall portion of the gate electrode, formed of a non-conductive semiconductor layer having a bandgap larger than that of silicon and impurities introduced thereinto. In a method of manufacturing a MOSFET having a gate side wall and a source region and a drain region provided on the silicon substrate, introducing an impurity into the gate side wall is performed by implanting impurity ions into the source region and the drain region. A method for manufacturing a MOSFET, which is performed

GF Exhibit 1124 - 1600/2704

simultaneously with the impurity ion implantation into the gate electrode.

5.

In a MOSFET having a gate electrode provided on a silicon substrate via a gate insulating film, a gate sidewall provided on a sidewall of the gate electrode, and a source region and a drain region provided on the silicon substrate. , The gate sidewall is formed of a ferroelectric material, and is polarized in the direction from the gate electrode to the silicon substrate when the silicon substrate is p-type, and is gated from the silicon substrate when the silicon substrate is n-type. A MOSFET characterized by being polarized in the direction of the electrodes.

6.

An insulating film is provided between the gate sidewall and the gate electrode, between the gate sidewall and the silicon substrate, or between the gate sidewall and the gate electrode and between the gate sidewall and the silicon substrate. 5. The MOSFET according to item 5.

7.

A gate electrode provided on a silicon substrate via a gate insulating film; a gate sidewall provided on a sidewall portion of the gate electrode and made of a ferroelectric material; and a source region provided on the silicon substrate. In a method of manufacturing a MOSFET having a drain region, an interlayer insulating film is formed on the silicon substrate, a contact hole communicating with the silicon substrate is formed in the interlayer insulating film, and the contact hole is filled with metal to fill the contact. And a step of forming a first electrode on the upper side wall of the gate via the interlayer insulating film, and forming a second electrode on the upper side of the contact embedding, the first electrode and the second electrode. A voltage is applied between the gate electrode and the electrode to polarize the side wall of the gate.

8.

A plurality of wells are provided on a silicon substrate, a plurality of gate electrodes are provided on each of the wells via a plurality of gate insulating films, and a ferroelectric material is provided on sidewalls of the gate electrodes. In a method of manufacturing a MOSFET having a plurality of gate sidewalls, a plurality of source regions and a plurality of drain regions provided on each well, an interlayer insulating film is formed on the silicon substrate, and the interlayer insulating film is formed. A step of forming a plurality of contact holes communicating with the respective wells in the film, burying the contact holes with a metal for contact filling, and forming a plurality of first electrodes on the upper portions of the respective gate sidewalls through the interlayer insulating film. Forming and forming a plurality of second electrodes on top of the respective contact embeddings; connecting the respective first electrodes to the respective

GF Exhibit 1124 - 1601/2704

second electrodes by wiring, and connecting the respective wirings And a voltage is applied between the gates to polarize the sidewalls of the gates.

9.

9. The method of manufacturing a MOSFET according to claim 7, further comprising a step of removing the first and second electrodes.

10.

10. The MOSFET according to claim 1, wherein the source region and the drain region outside the gate sidewall are formed of a metal material.

GF Exhibit 1124 - 1602/2704

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報**（Ａ）　(11)特許出願公開番号

特開平10－335265

(43)公開日　平成10年(1998)12月18日

(51)Int.Cl.[6]		識別記号	FI		
Ｈ０１Ｌ	21/285	３０１	Ｈ０１Ｌ	21/285	３０１Ｔ
	29/78			29/78	３０１Ｙ
	21/336				

審査請求　未請求　請求項の数６　ＯＬ　（全 13 頁）

(21)出願番号　特願平9－137063

(22)出願日　平成９年(1997)５月27日

(71)出願人　000002185
ソニー株式会社
東京都品川区北品川６丁目７番35号

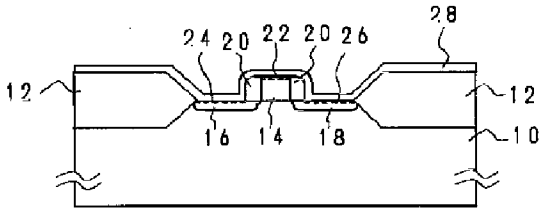
(72)発明者　千葉　安浩
東京都品川区北品川６丁目７番35号　ソニー株式会社内

(54)【発明の名称】　半導体装置の製造方法

(57)【要約】

【課題】　本発明は、シリサイド膜を形成する際に、リーク電流の発生原因となるシリサイドのスパイクが形成されることを防止し、信頼性が高く、高速な半導体装置の製造方法を提供することを目的とする。

【解決手段】　ＲＴＡ法を用いたNH_3雰囲気ガス中における熱処理により、多結晶シリコン層からなるゲート電極１４並びにシリコン基板１０表層部のソース領域１６及びドレイン領域１８上にスパイク防止用のＳｉＮ薄膜２２、２４、２６を形成した後、基体全面にＣｏ膜２８を成膜し、第１回目のＲＴＡ法を用いたアニール処理によりＣｏ膜２８を下地のＳｉと反応させてＣｏＳｉ膜３０、３２、３４を形成する。このとき、ゲート電極１４並びにソース領域１６及びドレイン領域１８とＣｏ膜２８と間にＳｉＮ薄膜２２、２４、２６が介在し、局所的なＣｏ原子の異常拡散を抑制し、Ｃｏシリサイドのスパイクの形成を防止する。



10・・・Si基板　18・・・ドレイン領域
12・・・LOCOS膜　20・・・サイドウオール
14・・・ゲート電極　22、24、26・・・SiN薄膜
16・・・ソース領域　28・・・Co膜

GF Exhibit 1124 - 1603/2704

【特許請求の範囲】
【請求項１】　シリコン領域を含む基体全面に金属膜を形成した後、熱処理により前記金属膜と前記シリコン領域のＳｉとを反応させ、前記シリコン領域上にシリサイド膜を自己整合的に形成する半導体装置の製造方法であって、
前記シリコン領域を含む基体全面に前記金属膜を形成する前に、前記シリコン領域上にスパイク防止用の薄膜を形成する工程が含まれることを特徴とする半導体装置の製造方法。
【請求項２】　請求項１記載の半導体装置の製造方法において、
前記金属膜が、Ｃｏ膜であることを特徴とする半導体装置の製造方法。
【請求項３】　請求項１記載の半導体装置の製造方法において、
前記スパイク防止用の薄膜が、ＳｉＮ膜からなることを特徴とする半導体装置の製造方法。
【請求項４】　請求項３記載の半導体装置の製造方法において、
前記ＳｉＮ膜からなるスパイク防止用の薄膜を形成する工程が、短時間熱処理法を用いて、前記シリコン領域を含む基体全面に対してNH_3雰囲気中におけるアニール処理を行い、前記シリコン領域表面に前記ＳｉＮ膜を形成する工程であることを特徴とする半導体装置の製造方法。
【請求項５】　請求項２記載の半導体装置の製造方法において、
前記シリコン領域を含む基体全面に前記Ｃｏ膜を形成した後に、前記Ｃｏ膜上に酸化防止用の薄膜を形成する工程が含まれることを特徴とする半導体装置の製造方法。
【請求項６】　請求項５記載の半導体装置の製造方法において、
前記酸化防止用の薄膜が、ＴｉＮ膜からなることを特徴とする半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、半導体装置の製造方法に係り、特にシリコン領域を含む基体全面に金属膜を形成し、熱処理により金属とＳｉ（シリコン）とを反応させてシリコン領域上にシリサイド膜を自己整合的に形成する、いわゆるサリサイド（ＳＡＬＩＣＩＤＥ；Self-Alinged Slicide）プロセスに関するものである。
【０００２】
【従来の技術】昨今の半導体デバイスの低抵抗化、高速化の要求から、ゲート（Gate）及びソース／ドレイン（Ｓ／Ｄ）領域上に低抵抗シリサイド膜を自己整合的に形成するサイサイド技術が注目されている。このような場合のシリサイド材料としては、Ｔｉ（チタン）シリサイドやＣｏ（コバルト）シリサイド等が活発に検討されている。
【０００３】しかし、Ｔｉシリサイドの場合、図１５のグラフに示されるように、n^+型拡散層上にＴｉシリサイド膜を形成すると、初期Ｔｉ膜の膜厚が厚くなるほどＴｉシリサイド膜のシート抵抗Ｒｓは減少するが、n^+型拡散層の幅Ｗが狭くなるほどＴｉシリサイド膜のシート抵抗Ｒｓは増大する傾向になる。そして、このＴｉシリサイド膜のシート抵抗Ｒｓの線幅依存性は、初期Ｔｉ膜の膜厚が厚くなるほど大きい。
【０００４】また、図１６のグラフに示されるように、p^+型拡散層上にＴｉシリサイド膜を形成する際にも、n^+型拡散層上に形成する場合と同様に、Ｔｉシリサイド膜のシート抵抗Ｒｓの線幅依存性が現れる。こうして、微細なライン上にＴｉシリサイド膜を形成する場合においては、そのシート抵抗Ｒｓが上昇する、いわゆる細線効果を生じることになる。
【０００５】これに対して、Ｃｏシリサイドの場合は、図１７のグラフに示されるように、n^+型拡散層上にＣｏシリサイド膜を形成すると、初期Ｃｏ膜の膜厚が厚くなるほどＣｏシリサイド膜のシート抵抗Ｒｓは減少するが、n^+型拡散層の幅Ｗが狭くなってもＣｏシリサイド膜のシート抵抗Ｒｓは殆ど変動しない。そして、このようにＣｏシリサイド膜のシート抵抗Ｒｓが線幅依存性を有していないことは、図１８のグラフに示されるように、p^+型拡散層上にＣｏシリサイド膜を形成する際も同様である。
【０００６】なお、上記図１７及び図１８のグラフにおいては、Ｃｏシリサイド膜を形成する際にＣｏ膜上にＴｉＮ膜を被せた、いわゆるＴｉＮキャップ（ｃａｐ）構造の場合のデータを示しているが、ＴｉＮ膜のないＣｏ膜だけを用いてＣｏシリサイド膜を形成する場合においても、基本的には同様の特性を示す。従って、微細なライン上にＣｏシリサイド膜を形成する場合にも、そのシート抵抗Ｒｓが上昇する細線効果を生じることはない。
【０００７】このように、微細なライン上に形成しても細線効果が生じないことから、最近においてはＣｏシリサイド膜についてより活発に検討されるようになっている。以下、従来のＣｏシリサイド・プロセスを図１９～図２２を用いて説明する。
【０００８】先ず、例えばＬＯＣＯＳ（Local Oxidation of Slicon ；選択酸化）法を用いて、シリコン基板５０上にＬＯＣＯＳ膜５２を選択的に形成して素子分離を行った後、素子領域のシリコン基板５０上に、ゲート酸化膜（図示せず）を介して、多結晶シリコン層からなるゲート電極５４を形成する。続いて、例えばイオン注入法を用いて、ＬＯＣＯＳ膜５２及びゲート電極５４をマスクに素子領域のシリコン基板５０表層部に不純物を選択的に添加して、ソース領域５６及びドレイン領域５８を形成する。続いて、基体全面にSiO_2膜（シリコン酸化膜）を堆積した後、ドライエッチング法により、こ

GF Exhibit 1124 - 1604/2704

のＳｉO_2膜をエッチング除去すると共に、ゲート電極５４側面にＳｉO_2膜を残存させ、ゲート電極５４側面にＳｉO_2膜からなるサイドウォール６０を形成する（図１９参照）。

【０００９】次いで、例えばスパッタ法を用いて、基体全面にＣｏ膜６２を一様に成膜する（図２０参照）。次いで、ＲＴＡ（Rapid Thermal Annealing ；短時間熱処理）法を用い、処理温度５５０℃程度の条件において、第１回目のアニール処理を行い、ゲート電極５４並びにソース領域５６及びドレイン領域５８上のＣｏ膜６２を下地のＳｉと反応させ、高抵抗のＣｏシリサイドであるＣｏＳｉ膜６４、６６、６８をそれぞれ形成する。このとき、ＬＯＣＯＳ膜５２及びサイドウォール６０上には、Ｃｏ膜６２が未反応なままの状態で残存する（図２１参照）。

【００１０】次いで、ウェット（ｗｅｔ）エッチング法を用いて、ＬＯＣＯＳ膜５２及びサイドウォール２０上に未反応のまま残っているＣｏ膜６２を選択的にエッチング除去する（図２２参照）。次いで、ＲＴＡ法を用い、処理温度７００℃程度の条件において、第２回目のアニール処理を行い、高抵抗のＣｏシリサイドであるＣｏＳｉ膜６４、６６、６８をＣｏシリサイドの中で最も低抵抗な相である$CoSi_2$膜７０、７２、７４に相転移する（図２３参照）。

【００１１】即ち、この従来のＣｏシリサイド・プロセスは、ＬＯＣＯＳ法、イオン注入法、ドライエッチング法等を用いて、ＬＯＣＯＳ膜５２によって分離された素子領域のシリコン基板５０上にゲート酸化膜を介して多結晶シリコン層からなるゲート電極５４を形成し、シリコン基板５０表層部にソース領域５６及びドレイン領域５８を形成し、ゲート電極５４側面にサイドウォール６０を形成する工程と、スパッタ法を用いて、基体全面にＣｏ膜６２を成膜する工程と、ＲＴＡ法を用いた第１回目のアニール処理により、ゲート電極５４並びにソース領域５６及びドレイン領域５８上のＣｏ膜６２を下地のＳｉと反応させ、高抵抗のＣｏシリサイドであるＣｏＳｉ膜６４、６６、６８をそれぞれ形成する工程と、ウェットエッチング法を用いて、ＬＯＣＯＳ膜５２及びサイドウォール６０上の未反応Ｃｏ膜６２を除去した後、ＲＴＡ法を用いた第２回目のアニール処理により、ＣｏＳｉ膜６４、６６、６８をＣｏシリサイドの中で最も低抵抗な相である$CoSi_2$膜７０、７２、７４にそれぞれ相転移する工程との４つの主要な工程からなる。

【００１２】このように、従来のＣｏシリサイド・プロセスにおいては、$CoSi_2$膜７０、７２、７４を形成するためのＲＴＡ法によるアニール処理を行う際に、Ｃｏ膜６２を下地のＳｉと反応させてＣｏＳｉ膜６４、６６、６８をそれぞれ形成する処理温度５５０℃程度の第１回目のアニール処理と、これらのＣｏＳｉ膜６４、６６、６８を$CoSi_2$膜７０、７２、７４に相転移する処理温度７００℃程度の第２回目のアニール処理との２段階に分けていることにより、ゲート電極５４並びにソース領域５６及びドレイン領域５８上にＣｏＳｉ膜６４、６６、６８が形成されるだけでなく、隣接するサイドウォール６０上にまでＣｏＳｉ膜が形成される、いわゆる這い上がり現象の発生が防止される。このため、サイドウォール２０上に形成されたＣｏＳｉ膜を介してゲート電極１４上のＣｏＳｉ膜３０とソース領域１６及びドレイン領域１８上のＣｏＳｉ膜３２、３４とが短絡する、即ちゲート電極１４とソース領域１６及びドレイン領域１８とが短絡する、いわゆるブリッジング現象が発生することもなく、ゲート電極５４並びにソース領域５６及びドレイン領域５８上に低抵抗の$CoSi_2$膜７０、７２、７４が自己整合的に形成される。

【００１３】

【発明が解決しようとする課題】しかしながら、上記従来のＣｏシリサイド・プロセスにおいては、図２４及び図２５のグラフに示されるように、n^+型拡散層及びp^+型拡散層上にそれぞれＣｏシリサイド膜を形成すると、これらのn^+型拡散層及びp^+型拡散層においてばらつきの大きなリーク電流が発生する。特に、n^+型拡散層上にＣｏシリサイド膜を形成する場合には、n^+型拡散層上に形成したＣｏ膜をシリサイド化する際のアニール処理温度によりリーク電流の発生に大きな差異が生じる。即ち、アニール処理温度が４００℃から４５０℃に上昇すると、リーク電流は急激に増大する。そして、アニール処理温度が４５０℃から更に７００℃に上昇するにつれて、リーク電流は僅かながら減少する傾向を示す。

【００１４】このようなことから、図２６に示されるように、例えばn^+型拡散層７６上にＣｏシリサイド膜７８を形成する際に発生するリーク電流は、４５０℃近傍の比較的低温のアニール処理温度においてn^+型拡散層７６中に形成されるＣｏシリサイドのスパイク８０に起因すると考えられている（K.Goto,et al.,“LeakageMechanism and Optimized Conditions of Co Process for Deep-Submicron CMOSDevices” IEDM (1995) p.449 参照）。そして、このＣｏシリサイドのスパイク８０の形成は、Ｃｏ原子がn^+型拡散層７６中に異常拡散して、その部分だけにＣｏシリサイドが形成されるためであると考えられている。従って、Ｃｏシリサイドは、上述のように細線効果がないことから今後更に微細化する半導体デバイスへの適用を考えた場合に極めて有利である反面、シリサイド化反応の初期において発生するＣｏシリサイドのスパイクに起因するリーク電流の発生が実デバイスへの適用の大きな障害となっている。

【００１５】そこで本発明は、上記事情を鑑みてなされたものであり、シリサイド膜を形成する際に、リーク電流の発生原因となるシリサイドのスパイクが形成されることを防止し、信頼性が高く、高速な半導体装置の製造

GF Exhibit 1124 - 1605/2704

方法を提供することを目的とする。
【００１６】
【課題を解決するための手段】上記課題は、以下の本発明に係る半導体装置の製造方法により達成される。即ち、請求項１に係る半導体装置の製造方法は、シリコン領域を含む基体全面に金属膜を形成した後、熱処理により金属膜とシリコン領域のＳｉとを反応させ、シリコン領域上にシリサイド膜を自己整合的に形成する半導体装置の製造方法であって、シリコン領域を含む基体全面に金属膜を形成する前に、シリコン領域上にスパイク防止用の薄膜を形成する工程が含まれることを特徴とする。
【００１７】このように請求項１に係る半導体装置の製造方法においては、シリコン領域を含む基体全面に金属膜を形成する前に、このシリコン領域上にスパイク防止用の薄膜を形成することにより、熱処理によりシリコン領域のＳｉと金属とを反応させる際に、シリコン領域と金属膜との間にスパイク防止用の薄膜が介在することになるため、シリサイド化反応の初期において発生する局所的な金属原子の異常拡散が抑制され、金属原子が均一に拡散して、シリサイドのスパイクの形成が防止される。従って、このシリサイドのスパイクに起因するリーク電流の発生が防止される。
【００１８】なお、ここで、シリコン領域とは、多結晶シリコン領域及び単結晶シリコン領域の両方を含むものとする。また、シリコン領域と金属膜と間に介在するスパイク防止用の薄膜はその膜厚が極めて薄くなっているため、Ｓｉと金属とのシリサイド化反応を阻止するものではない。
【００１９】また、請求項２に係る半導体装置の製造方法は、上記請求項１に係る半導体装置の製造方法において、金属膜がＣｏ膜である構成とすることにより、Ｓｉとの反応によりシリサイド膜が形成される際、特にシリサイドのスパイクが形成され易いＣｏ膜の場合であっても、シリコン領域とＣｏ膜と間にスパイク防止用の薄膜が介在しているため、シリサイド化反応の初期において発生する局所的なＣｏ原子の異常拡散が抑制され、Ｃｏ原子が均一に拡散して、ＣｏシリサイドのスパイクのＳ形成が防止される。従って、このＣｏシリサイドのスパイクに起因するリーク電流の発生が防止される。
【００２０】また、請求項３に係る半導体装置の製造方法は、上記請求項１に係る半導体装置の製造方法において、スパイク防止用の薄膜がＳｉＮ膜（シリコン窒化膜）からなる構成とすることにより、例えばシリコン領域と金属膜と間に自然酸化膜が介在する場合のようにシリサイド化反応を妨害することがないため、シリコン領域と金属膜との間に介在するＳｉＮ膜は、局所的な金属原子の異常拡散を抑制するというシリサイド膜を形成する際のスパイク防止用薄膜としての機能を良好に発揮する。
【００２１】また、請求項４に係る半導体装置の製造方法は、上記請求項３に係る半導体装置の製造方法において、ＳｉＮ膜からなるスパイク防止用の薄膜を形成する工程が、ＲＴＡ法を用いて、シリコン領域を含む基体全面に対してNH_3（アンモニア）雰囲気中におけるアニール処理を行い、シリコン領域表面にＳｉＮ膜を形成する工程である構成とすることにより、Ｓｉと金属とのシリサイド化反応を阻止することなく、且つシリサイド膜を形成する際のスパイク防止用薄膜として機能するのに必要十分な膜厚をもつ緻密なＳｉＮ膜が容易に形成される。
【００２２】また、請求項５に係る半導体装置の製造方法は、上記請求項２に係る半導体装置の製造方法において、シリコン領域を含む基体全面にＣｏ膜を形成した後に、このＣｏ膜上に酸化防止用の薄膜を形成する工程が含まれる構成とすることにより、本来Ｃｏは非常に酸化され易い金属膜であるが酸化防止用の薄膜によって覆われるため、Ｃｏ膜が大気暴露によって表面酸化されることから保護される。なお、このＣｏ膜の酸化防止用の薄膜としては、ＴｉＮ膜が好適である。
【００２３】
【発明の実施の形態】以下、添付図面を参照しながら、本発明の実施の形態を説明する。
（第１の実施形態）図１～図６は、それぞれ本発明の第１の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図である。先ず、例えばＬＯＣＯＳ法を用いて、シリコン基板１０上にＬＯＣＯＳ膜１２を選択的に形成し、素子分離を行う。その後、ＬＯＣＯＳ膜１２によって分離された素子領域のシリコン基板１０上に、ゲート酸化膜（図示せず）を介して多結晶シリコン層からなるゲート電極１４を形成する。
【００２４】続いて、例えばイオン注入法を用いて、ＬＯＣＯＳ膜１２及びゲート電極１４をマスクに素子領域のシリコン基板１０表層部に不純物を選択的に添加して、ソース領域１６及びドレイン領域１８を形成する。続いて、基体全面にSiO_2膜を堆積した後、ドライエッチング法により、このSiO_2膜をエッチング除去すると共に、ゲート電極１４側面にこのSiO_2膜を残存させる。こうして、ゲート電極１４側面にSiO_2膜からなるサイドウォール２０を形成する（図１参照）。
【００２５】次いで、ＲＴＡ法を用いて、ゲート電極１４上面並びにソース領域１６及びドレイン領域１８表面が露出している基体全体をNH_3雰囲気中において熱処理する。こうして、ゲート電極１４上面並びにソース領域１６及びドレイン領域１８表面を窒化して、膜厚１．５ｎｍの緻密なＳｉＮ薄膜２２、２４、２６をそれぞれ形成する（図２参照）。なお、これらの膜厚１．５ｎｍのＳｉＮ薄膜２２、２４、２６を形成する際のＲＴＡ法を用いた熱処理条件は、
NH_3雰囲気ガス流量：５ｓｃｃｍ
処理温度：９００℃

GF Exhibit 1124 - 1606/2704

処理時間：３０秒
である。
【００２６】次いで、例えばスパッタ法を用いて、基体全面に膜厚１０ｎｍのＣｏ膜２８を一様に成膜する（図３参照）。なお、この膜厚１０ｎｍのＣｏ膜２８を形成する際の成膜条件は、
ＤＣパワー：０．８ｋＷ
圧力：０．４Ｐａ
ヒータ用のＡｒ（アルゴン）ガス流量：３０ｓｃｃｍ
プロセス用のＡｒガス流量：６０ｓｃｃｍ
基板加熱温度：１５０℃
である。
【００２７】次いで、ＲＴＡ法を用いて、全面にＣｏ膜２８が成膜された基体に対してN_2（窒素）雰囲気中における第１回目のアニール処理を行い、ゲート電極１４並びにソース領域１６及びドレイン領域１８上のＣｏ膜２８を下地のＳｉと反応させて、高抵抗のＣｏシリサイドであるＣｏＳｉ膜３０、３２、３４をそれぞれ形成する。このとき、ＬＯＣＯＳ膜１２及びサイドウォール２０上には、Ｃｏ膜２８が未反応なままの状態で残存している（図４参照）。なお、これらのＣｏＳｉ膜３０、３２、３４を形成する際の第１回目のＲＴＡ法を用いたアニール処理条件は、
N_2 雰囲気ガス流量：１０ｓｃｃｍ
処理温度：５５０℃
処理時間：３０秒
である。
【００２８】このとき、ゲート電極１４の多結晶シリコン面並びにソース領域１６及びドレイン領域１８の単結晶シリコン面（以下、多結晶シリコン面及び単結晶シリコン面の両方を併せて単に「シリコン面」という）とＣｏ膜２８との間にはそれぞれＳｉＮ薄膜２２、２４、２６が介在しているものの、これらのＳｉＮ薄膜２２、２４、２６はその膜厚が１．５ｎｍと極めて薄いため、Ｃｏ膜２８がゲート電極１４並びにソース領域１６及びドレイン領域１８のシリコン面と反応することを阻止することはない。
【００２９】また、上記の条件において第１回目のアニール処理を行うと、従来の場合は、上記図２６に示されるように、ＣｏＳｉのスパイクが形成されるのが通常であったが、本実施形態においては、Ｃｏ膜２８とその下地のシリコン面との間にそれぞれＳｉＮ薄膜２２、２４、２６が介在していることにより、局所的なＣｏ原子の異常拡散が抑制され、Ｃｏ原子が均一に拡散するため、ＣｏＳｉのスパイクが形成されることはなくなる。即ち、ＳｉＮ薄膜２２、２４、２６は、ＣｏＳｉ膜３０、３２、３４を形成する際のスパイク防止用薄膜として機能する。
【００３０】また、本実施形態においては、処理温度５５０℃、処理時間３０秒という条件においてアニール処理を行っているため、サイドウォール２０上にもＣｏＳｉ膜が形成されてゲート電極１４上のＣｏＳｉ膜３０とソース領域１６及びドレイン領域１８上のＣｏＳｉ膜３２、３４とが短絡する、即ちゲート電極１４とソース領域１６及びドレイン領域１８とが短絡する、いわゆるＣｏＳｉ膜の這い上がりによるブリッジング現象が起きることもない。
【００３１】次いで、ウェットエッチング法を用いて、ＬＯＣＯＳ膜１２及びサイドウォール２０上に未反応のままの状態で残存しているＣｏ膜２８を選択的にエッチング除去する（図５参照）。なお、この未反応Ｃｏ膜２８のウェットエッチング条件は、
薬液：硫酸過水（H_2SO_4：H_2O_2＝４：１）
薬液温度：７０℃
処理時間：３分
である。
【００３２】次いで、ＲＴＡ法を用いて、ゲート電極１４並びにソース領域１６及びドレイン領域１８上にそれぞれＣｏＳｉ膜３０、３２、３４が形成された基体に対してN_2 雰囲気中における第２回目のアニール処理を行い、これらのＣｏＳｉ膜３０、３２、３４をＣｏシリサイドの中で最も低抵抗な相である$CoSi_2$ 膜３６、３８、４０に相転移する（図６参照）。
【００３３】なお、これらのＣｏＳｉ膜３０、３２、３４を$CoSi_2$ 膜３６、３８、４０に相転移する際の第２回目のアニール処理条件は、
N_2 雰囲気ガス流量：１０ｓｃｃｍ
処理温度：７００℃
処理時間：３０秒
である。
【００３４】以上のように本実施形態によれば、ＲＴＡ法を用いたNH_3 雰囲気中における熱処理により、多結晶シリコン層からなるゲート電極１４並びにシリコン基板１０表層部のソース領域１６及びドレイン領域１８上に膜厚１．５ｎｍのＳｉＮ薄膜２２、２４、２６を形成した後、基体全面に膜厚１０ｎｍのＣｏ膜２８を成膜し、第１回目のＲＴＡ法を用いたアニール処理によりＣｏ膜２８を下地のＳｉと反応させて、高抵抗のＣｏシリサイドであるＣｏＳｉ膜３０、３２、３４を形成し、第２回目のＲＴＡ法を用いたアニール処理によりＣｏシリサイドの中で最も低抵抗な相である$CoSi_2$ 膜３６、３８、４０に相転移しているが、第１回目のＲＴＡ法を用いたアニール処理によりＣｏ膜２８と下地のＳｉとを反応させる際に、ゲート電極１４並びにソース領域１６及びドレイン領域１８とＣｏ膜２８と間にスパイク防止用のＳｉＮ薄膜２２、２４、２６が介在していることにより、局所的なＣｏ原子の異常拡散が抑制され、Ｃｏ原子が均一に拡散して、Ｃｏシリサイドのスパイクの形成を防止することができるため、このＣｏシリサイドのスパイクに起因するリーク電流の発生を防止することがで

GF Exhibit 1124 - 1607/2704

き、半導体デバイスの信頼性を向上させることが可能になる。

【００３５】また、このようにリーク電流の発生を防止することができることから、低抵抗の$CoSi_2$膜３６、３８、４０の膜厚を更に十分に厚くすることが可能になるため、これらの$CoSi_2$膜３６、３８、４０を形成したゲート電極１４並びにソース領域１６及びドレイン領域１８の抵抗を更に低減することができ、半導体デバイスの動作速度を更に高速化することが可能になる。

【００３６】（第２の実施形態）図７～図１４は、それぞれ本発明の第２の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図である。なお、上記図１～図６に示す構成要素と同一の要素には同一の符号を付して説明を省略する。先ず、ＬＯＣＯＳ法を用いて、シリコン基板１０上にＬＯＣＯＳ膜１２を選択的に形成し、素子分離を行った後、ＬＯＣＯＳ膜１２によって分離された素子領域のシリコン基板１０上に、ゲート酸化膜（図示せず）を介して多結晶シリコン膜からなるゲート電極１４を形成する。

【００３７】続いて、イオン注入法を用い、素子領域のシリコン基板１０表層部に不純物を選択的に添加し、ソース領域１６及びドレイン領域１８を形成した後、SiO_2膜の堆積及びそのドライエッチングにより、ゲート電極１４側面にSiO_2膜からなるサイドウォール２０を形成する（図７参照）。

【００３８】次いで、ＲＴＡ法を用いて、基体全体をNH_3雰囲気中において熱処理して、ゲート電極１４上面並びにソース領域１６及びドレイン領域１８表面を窒化し、膜厚１．５ｎｍの緻密なＳｉＮ薄膜２２、２４、２６をそれぞれ形成する（図８参照）。なお、これら膜厚１．５ｎｍのＳｉＮ薄膜２２、２４、２６を形成する際のＲＴＡ処理条件は、上記第１の実施形態の場合と同様である。

【００３９】次いで、スパッタ法を用いて、基体全面に膜厚１０ｎｍのＣｏ膜２８を一様に成膜する（図９参照）。なお、この膜厚１０ｎｍのＣｏ膜２８を形成する際の成膜条件は、上記第１の実施形態の場合と同様である。

【００４０】次いで、例えばスパッタ法を用いて、Ｃｏ膜２８を一様に成膜した基体を大気開放することなく、このＣｏ膜２８上に膜厚２０ｎｍのＴｉＮキャップ膜４２を成膜する（図１０参照）。なお、このＴｉＮキャップ膜４２を形成する際の成膜条件は、

ＤＣパワー：６．５ｋＷ
圧力：０．４Ｐａ
ヒータ用のＡｒガス流量：１５ｓｃｃｍ
プロセス用のN_2ガス流量：１３５ｓｃｃｍ
基板加熱温度：１５０℃
である。

【００４１】このとき、前の工程におけるスパッタチャンバ内において基体全面に成膜されたＣｏ膜２８は、大気開放されることなく、その全面がＴｉＮキャップ膜４２によって覆われるため、本来は非常に酸化され易い金属膜であるＣｏ膜２８が大気暴露されてその表面が酸化されることから保護される。即ち、ＴｉＮキャップ膜４２は、Ｃｏ膜２８の酸化防止用膜として機能する。

【００４２】次いで、ＲＴＡ法を用いて、全面にＣｏ膜２８及びＴｉＮキャップ膜４２が順に積層された基体に対してN_2雰囲気中における第１回目のアニール処理を行い、ゲート電極１４並びにソース領域１６及びドレイン領域１８上のＣｏ膜２８を下地のＳｉと反応させて、高抵抗のＣｏシリサイドであるＣｏＳｉ膜３０、３２、３４をそれぞれ形成すると共に、ＬＯＣＯＳ膜１２及びサイドウォール２０上には、未反応Ｃｏ膜２８を残存する（図１１参照）。なお、これらのＣｏＳｉ膜３０、３２、３４を形成する際の第１回目のアニール処理条件は、上記第１の実施形態の場合と同様である。

【００４３】このとき、上記第１の実施形態の場合と同様にして、ゲート電極１４並びにソース領域１６及びドレイン領域１８のシリコン面とＣｏ膜２８との間にはスパイク防止用薄膜として機能する膜厚１．５ｎｍのＳｉＮ薄膜２２、２４、２６がそれぞれ介在していることにより、ゲート電極１４並びにソース領域１６及びドレイン領域１８のシリコン面とＣｏ膜２８との反応を阻止することなく、局所的なＣｏ原子の異常拡散を抑制してＣｏ原子を均一に拡散させるため、ＣｏＳｉ膜３０、３２、３４が形成されると共に、ＣｏＳｉのスパイクの形成が防止される。また、本実施形態においても、上記第１の実施形態の場合と同様に、処理温度５５０℃、処理時間３０秒という条件においてアニール処理を行っているため、ＣｏＳｉ膜の這い上がりによるブリッジング現象が起きることもない。

【００４４】次いで、例えばウェットエッチング法を用いて、Ｃｏ膜２８の酸化防止用膜としてＣｏ膜２８上に成膜したＴｉＮキャップ膜４２をエッチング除去する（図１２参照）。なお、このＴｉＮキャップ膜４２のウェットエッチング条件は、

薬液：アンモニア過水（$NH_4OH:H_2O_2:H_2O$＝１：２：６）
薬液温度：６５℃
処理時間：３分
である。

【００４５】次いで、ウェットエッチング法を用いて、ＬＯＣＯＳ膜１２及びサイドウォール２０上の未反応Ｃｏ膜２８を選択的にエッチング除去する（図１３参照）。なお、この未反応Ｃｏ膜２８のウェットエッチング条件は、上記第１の実施形態の場合と同様である。

【００４６】次いで、ＲＴＡ法を用いて、ゲート電極１４並びにソース領域１６及びドレイン領域１８上にそれ

GF Exhibit 1124 - 1608/2704

ぞれＣｏＳｉ膜３０、３２、３４が形成された基体に対してN_2雰囲気中における第２回目のアニール処理を行い、これらのＣｏＳｉ膜３０、３２、３４をＣｏシリサイドの中で最も低抵抗な相である$CoSi_2$膜３６、３８、４０に相転移する（図１４参照）。なお、これらのＣｏＳｉ膜３０、３２、３４を$CoSi_2$膜３６、３８、４０に相転移する際の第２回目のアニール処理条件は、上記第１の実施形態の場合と同様である。

【００４７】以上のように本実施形態によれば、上記第１の実施形態にいわゆるＴｉＮキャップ・プロセスを組み合わせることにより、即ちＲＴＡ法を用いたNH_3雰囲気中における熱処理によりゲート電極１４並びにソース領域１６及びドレイン領域１８上にＳｉＮ薄膜２２、２４、２６をそれぞれ形成し、基体全面にＣｏ膜２８を成膜した後、このＣｏ膜２８上に酸化防止用膜としてＴｉＮキャップ膜４２を成膜し、続いて第１回目のＲＴＡ法を用いたアニール処理によりＣｏＳｉ膜３０、３２、３４をそれぞれ形成し、第２回目のＲＴＡ法を用いたアニール処理により$CoSi_2$膜３６、３８、４０に相転移することにより、成膜後のＣｏ膜２８全面がＴｉＮキャップ膜４２によって覆われ、大気暴露による表面酸化から保護されるため、その後の第１回目のアニール処理によるＣｏＳｉ膜３０、３２、３４の形成、更に第２回目のアニール処理による$CoSi_2$膜３６、３８、４０への相転移を安定して行うことができる。従って、上記第１の実施形態の場合と同様の効果を奏することに加え、低抵抗の$CoSi_2$膜３６、３８、４０をより安定に形成することができるため、更に信頼性の高い、より高速な半導体デバイスを作製することが可能になる。

【００４８】

【発明の効果】以上、詳細に説明した通り、本発明に係る半導体装置の製造方法によれば、次のような効果を奏することができる。即ち、請求項１に係る半導体装置の製造方法によれば、シリコン領域を含む基体全面に金属膜を形成する前に、このシリコン領域上にスパイク防止用の薄膜を形成することにより、シリコン領域と金属膜との間にスパイク防止用の薄膜が介在することになるため、熱処理によりシリコン領域のＳｉと金属とを反応させる際に、シリサイド化反応の初期において発生する局所的な金属原子の異常拡散が抑制され、金属原子が均一に拡散して、シリサイドのスパイクが形成されることを防止することが可能になり、このシリサイドのスパイクに起因するリーク電流の発生を防止することができる。また、こうしたリーク電流の発生を防止することができることから、低抵抗のシリサイド膜の膜厚を更に十分に厚くすることが可能になるため、このシリサイド膜を形成したシリコン領域の抵抗を更に低減することができる。従って、高信頼性、高性能の半導体デバイスを作製することが可能になる。

【００４９】また、請求項２に係る半導体装置の製造方法によれば、上記請求項１に係る半導体装置の製造方法において、金属膜がＣｏ膜であることにより、特にシリサイドのスパイクが形成され易いＣｏ膜の場合であっても、シリコン領域のＳｉとの反応によってシリサイド膜が形成される際に、シリコン領域とＣｏ膜と間にスパイク防止用の薄膜が介在しているため、局所的なＣｏ原子の異常拡散が抑制され、Ｃｏ原子が均一に拡散して、Ｃｏシリサイドのスパイクの形成を防止することが可能になる。このため、Ｃｏシリサイドのスパイクに起因するリーク電流の発生を防止することができると共に、こうしたリーク電流の発生を防止することができることから、最も低抵抗な相のＣｏシリサイド膜、即ち$CoSi_2$膜の膜厚を更に十分に厚くすることが可能になり、この$CoSi_2$膜を形成したシリコン領域、例えばゲート電極やソース領域及びドレイン領域の抵抗を更に低減することができるため、信頼性の高い、より高速な半導体デバイスを作製することが可能になる。

【００５０】また、請求項３に係る半導体装置の製造方法によれば、上記請求項１に係る半導体装置の製造方法において、スパイク防止用の薄膜がＳｉＮ膜からなることにより、シリコン領域と金属膜との間にＳｉＮ膜が介在するため、局所的な金属原子の異常拡散を抑制して均一に拡散させ、シリサイド膜を形成する際のスパイク防止用薄膜として機能することができる。

【００５１】また、請求項４に係る半導体装置の製造方法によれば、上記請求項３に係る半導体装置の製造方法において、ＳｉＮ膜からなるスパイク防止用の薄膜を形成する工程が、ＲＴＡ法を用いて、シリコン領域を含む基体全面に対してNH_3雰囲気中におけるアニール処理を行い、シリコン領域表面にＳｉＮ膜を形成する工程であることにより、Ｓｉと金属との反応を阻止することなく、且つシリサイド膜を形成する際のスパイク防止用薄膜として機能するのに必要十分な膜厚をもつ緻密なＳｉＮ膜を容易に形成することが可能になる。

【００５２】また、請求項５に係る半導体装置の製造方法によれば、上記請求項２に係る半導体装置の製造方法において、シリコン領域を含む基体全面にＣｏ膜を形成した後に、このＣｏ膜上に例えばＴｉＮ膜からなる酸化防止用の薄膜を形成する工程が含まれることにより、Ｃｏ膜が大気暴露によって表面酸化されることから保護されるため、上記請求項２に係る半導体装置の製造方法の場合よりも更に安定してＣｏシリサイド膜の形成を行うことができる。

【図面の簡単な説明】

【図１】本発明の第１の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その１）である。

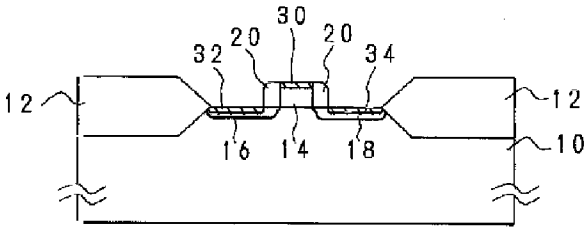
【図２】本発明の第１の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その２）である。

GF Exhibit 1124 - 1609/2704

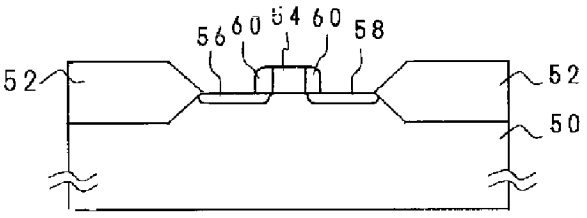
【図３】本発明の第１の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その３）である。
【図４】本発明の第１の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その４）である。
【図５】本発明の第１の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その５）である。
【図６】本発明の第１の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その６）である。
【図７】本発明の第２の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その１）である。
【図８】本発明の第２の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その２）である。
【図９】本発明の第２の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その３）である。
【図１０】本発明の第２の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その４）である。
【図１１】本発明の第２の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その５）である。
【図１２】本発明の第２の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その６）である。
【図１３】本発明の第２の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その７）である。
【図１４】本発明の第２の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その８）である。
【図１５】n^+ 型拡散層上に形成されたＴｉシリサイド膜のシート抵抗Ｒｓの線幅依存性を示すのグラフである。
【図１６】p^+ 型拡散層上に形成されたＴｉシリサイド膜のシート抵抗Ｒｓの線幅依存性を示すのグラフである。
【図１７】n^+ 型拡散層上に形成されたＣｏシリサイド膜のシート抵抗Ｒｓの線幅依存性を示すのグラフである。
【図１８】p^+ 型拡散層上に形成されたＣｏシリサイド膜のシート抵抗Ｒｓの線幅依存性を示すのグラフである。
【図１９】従来のＣｏシリサイド・プロセスを説明するための工程断面図（その１）である。
【図２０】従来のＣｏシリサイド・プロセスを説明するための工程断面図（その２）である。
【図２１】従来のＣｏシリサイド・プロセスを説明するための工程断面図（その３）である。
【図２２】従来のＣｏシリサイド・プロセスを説明するための工程断面図（その４）である。
【図２３】従来のＣｏシリサイド・プロセスを説明するための工程断面図（その５）である。
【図２４】n^+ 型拡散層上にＣｏシリサイド膜を形成する際のシリサイド温度によるリーク電流の累積度数分布を示すのグラフである。
【図２５】p^+ 型拡散層上にＣｏシリサイド膜を形成する際のシリサイド温度によるリーク電流の累積度数分布を示すのグラフである。
【図２６】従来のＣｏシリサイド・プロセスにおいて形成されるＣｏシリサイドのスパイクを示す模式図である。

【符号の説明】
１０…シリコン基板、１２…ＬＯＣＯＳ膜、１４…ゲート電極、１６…ソース領域、１８…ドレイン領域、２０…サイドウォール、２２、２４、２６…ＳｉＮ薄膜、２８…Ｃｏ膜、３０、３２、３４…ＣｏＳｉ膜、３６、３８、４０…$CoSi_2$ 膜、４２…ＴｉＮキャップ膜、５０…シリコン基板、５２…ＬＯＣＯＳ膜、５４…ゲート電極、５６…ソース領域、５８…ドレイン領域、６０…サイドウォール、６２…Ｃｏ膜、６４、６６、６８…ＣｏＳｉ膜、７０、７２、７４…$CoSi_2$ 膜、７６…n^+ 型拡散層、７８…Ｃｏシリサイド膜、８０…Ｃｏシリサイドのスパイク。

【図5】

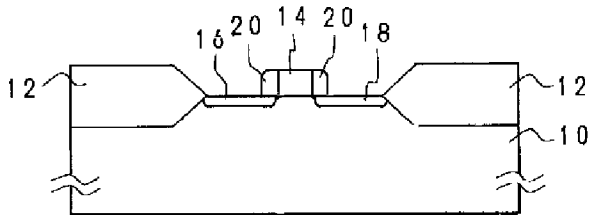


【図１９】



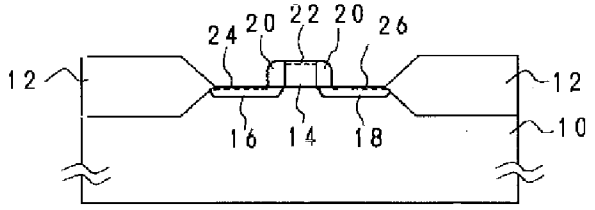
GF Exhibit 1124 - 1610/2704

【図1】



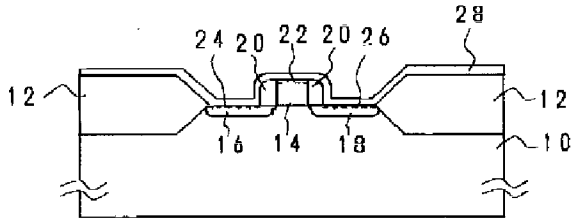
10・・・Si基板
12・・・LOCOS膜
14・・・ゲート電極
16・・・ソース領域
18・・・ドレイン領域
20・・・サイドウオール

【図2】

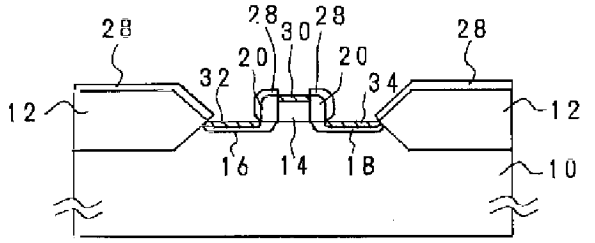


22、24、26・・・SiN薄膜

【図3】



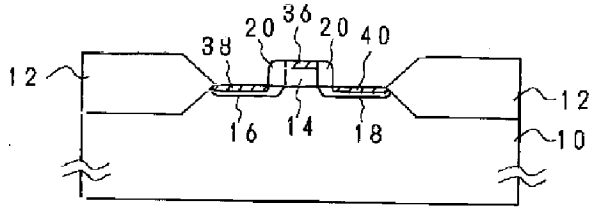
【図4】



30、32、34・・・CoSi膜

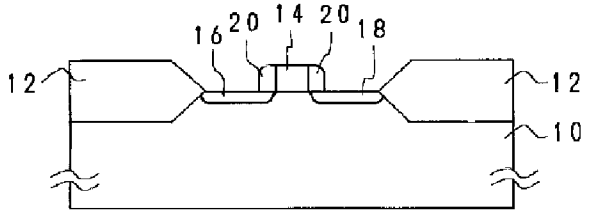
10・・・Si基板
12・・・LOCOS膜
14・・・ゲート電極
16・・・ソース領域
18・・・ドレイン領域
20・・・サイドウオール
22、24、26・・・SiN薄膜
28・・・Co膜

【図6】



36、38、40・・・$CoSi_2$膜

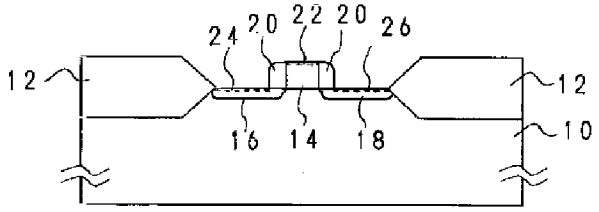
【図7】



10・・・Si基板
12・・・LOCOS膜
14・・・ゲート電極
16・・・ソース領域
18・・・ドレイン領域
20・・・サイドウオール

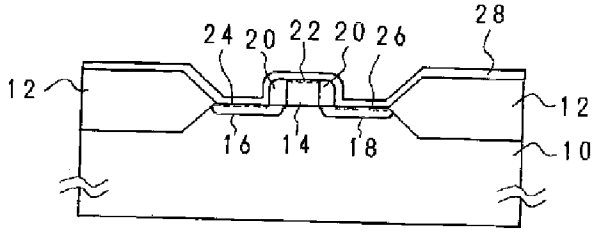
GF Exhibit 1124 - 1611/2704

【図8】



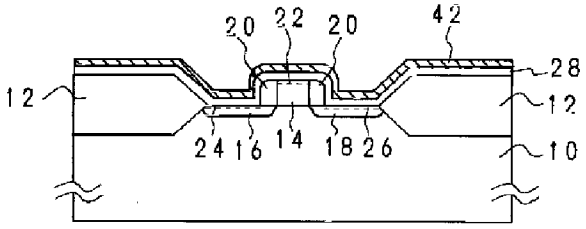
22、24、26・・・SiN膜

【図9】



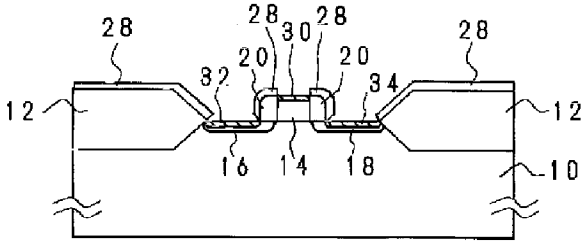
28・・・Co膜

【図10】

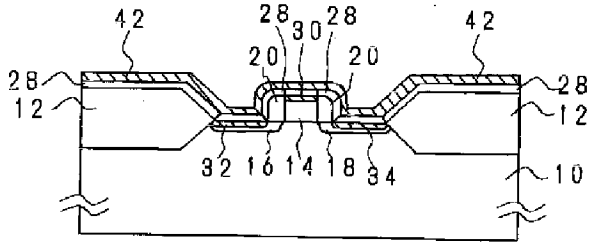


42・・・TiNキャップ膜

【図12】

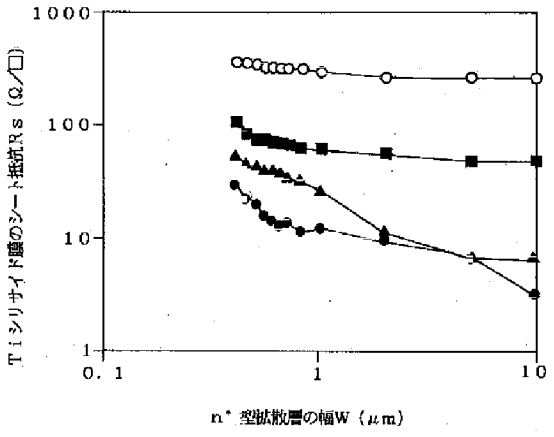


【図11】

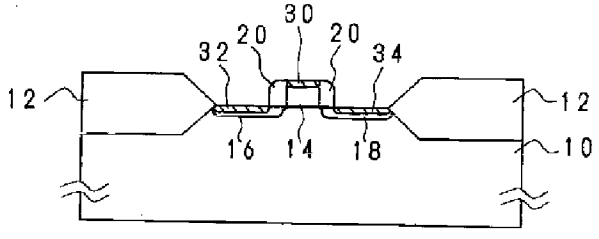


30、32、34・・・CoSi膜

【図15】

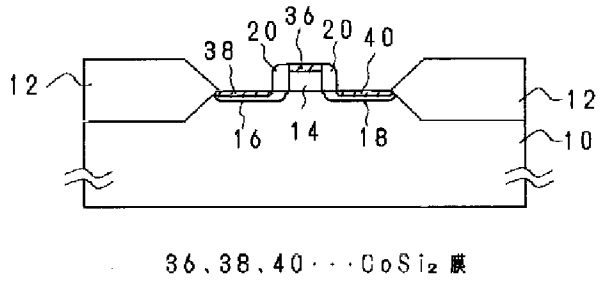


【図13】



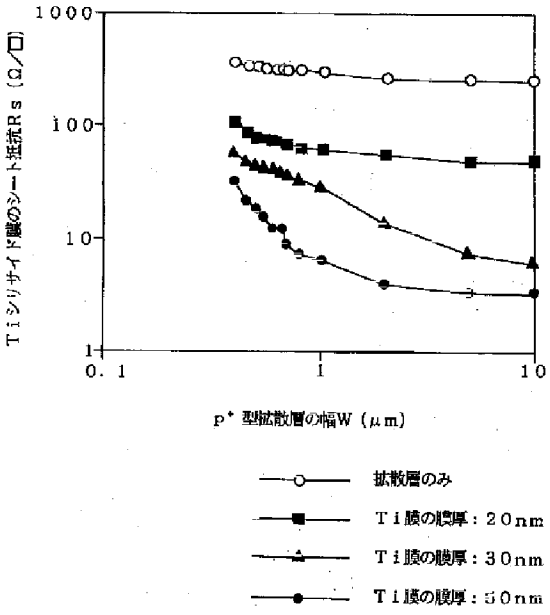
GF Exhibit 1124 - 1612/2704

【図14】

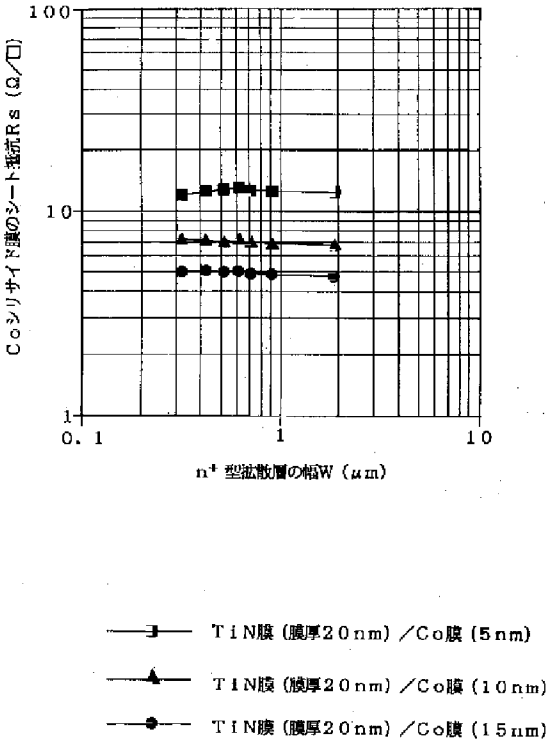


36、38、40・・・$CoSi_2$ 膜

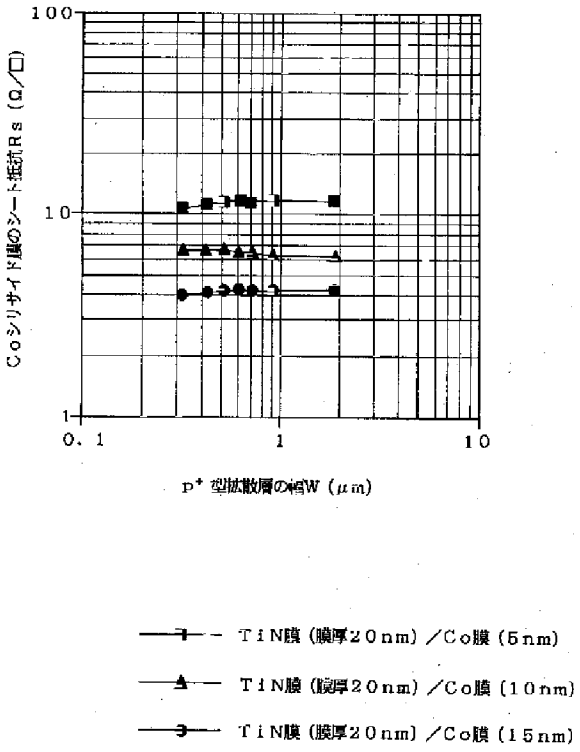
【図16】



【図17】

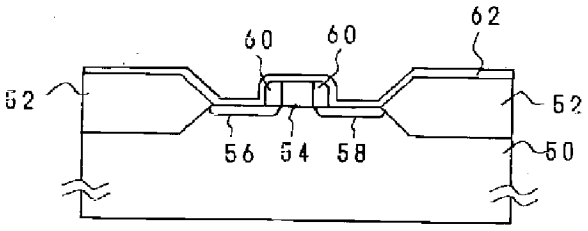


【図18】

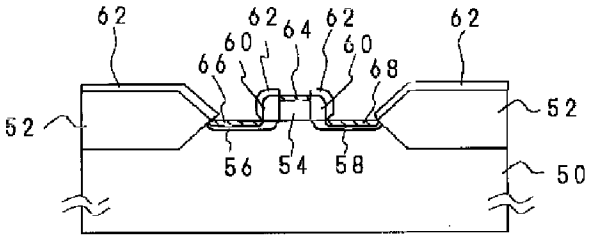


GF Exhibit 1124 - 1613/2704

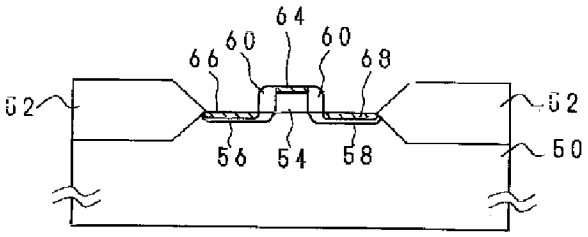
【図20】



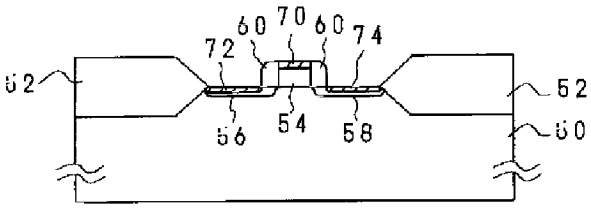
【図21】



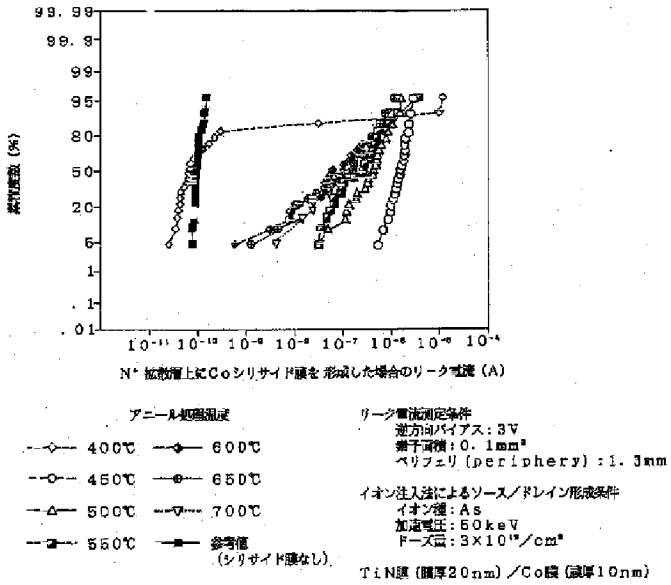
【図22】



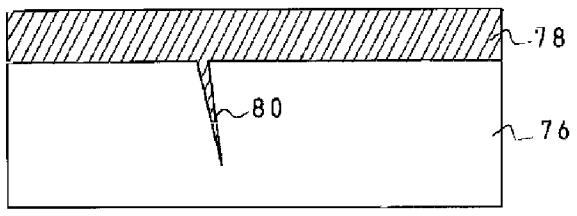
【図23】



【図24】

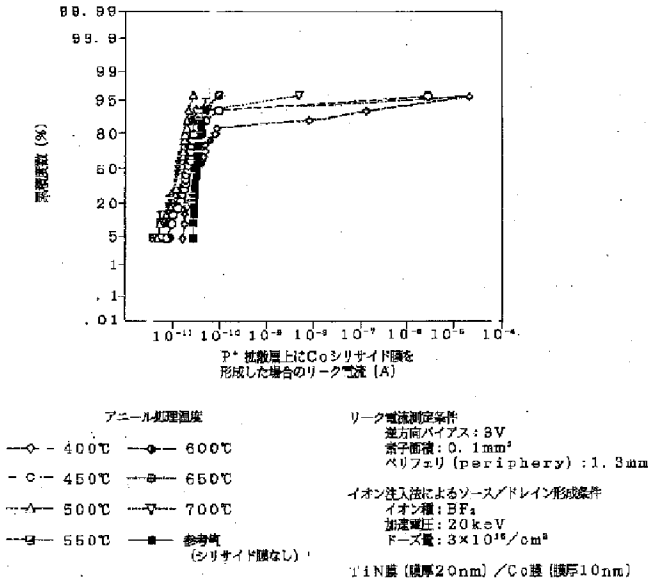


【図26】



GF Exhibit 1124 - 1614/2704

【図25】



GF Exhibit 1124 - 1615/2704

Europäisches Patentamt
European Patent Office
Office européen des brevets

Espacenet

JPH10335265A MANUFACTURE OF SEMICONDUCTOR DEVICE

Applicants: SONY CORP

Inventors: CHIBA YASUHIRO

Classifications:

IPC ***H01L21/28; H01L21/285; H01L21/336; H01L29/78;*** (IPC1-7): H01L21/285; H01L21/336; H01L29/78;

Priorities: JP13706397A 1997-05-27

Application: JPH10335265A·1997-05-27

Publication: JPH10335265A·1998-12-18

Published as: JPH10335265A

MANUFACTURE OF SEMICONDUCTOR DEVICE

Abstract

PROBLEM TO BE SOLVED: To provide a manufacturing method for a highly reliable, high-speed semiconductor device by preventing the generation of spikes of Co silicide, which causes a leakage current when a silicide film is formed. SOLUTION: This SiN films 22, 24, 26 for preventing spikes are formed on a gate electrode 14 comprising a polycrystalline silicon layer and a source region 16 and a drain region 18 that are formed on the surface layer of a silicon substrate 10, by a heat treatment in NH3 atmospheric gas using a RTA(rapid thermal annealing) method, and then a Co film 28 is formed on the whole surface of the substrate and is reacted with Si in a base by first annealing treatment, using the RTA method to form CoSi films 30, 32, 34. At this time, the thin SiN films 22, 24, 26 are interposed between the Co film and the gate electrode 14 and the source region 16 and the drain region 18 and prevent the abnormal diffusion of local Co atoms, which prevents the formation of spikes of Co silicide.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION JPH10335265

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a method of manufacturing a semiconductor device, and more particularly, to forming a metal film on the entire surface of a substrate including a silicon region and heat treating the metal to react with Si (silicon) to form a silicon film on the silicon region. The present invention relates to a so-called salicide (SALIDE: Self-Alinged Slicide) process for forming a silicide film in a self-aligned manner.

[0002]

2. Description of the Related Art Due to recent demands for lower resistance and higher speed of semiconductor devices, there is a side technology for forming a low resistance silicide film on a gate and source / drain (S / D) regions in a self-aligned manner. Attention has been paid. As a silicide material in such a case, Ti (titanium) silicide, Co (cobalt) silicide, or the like has been actively studied.

[0003]

However, in the case of Ti silicide, as shown in the graph of FIG. 15, when a Ti silicide film is formed on the n + type diffusion layer, the sheet resistance Rs of the Ti silicide film decreases as the initial Ti film becomes thicker. However, the sheet resistance Rs of the Ti silicide film tends to

GF Exhibit 1124 - 1617/2704

increase as the width W of the n + type diffusion layer decreases. The line width dependence of the sheet resistance Rs of the Ti silicide film increases as the film thickness of the initial Ti film increases.

[0004]

In addition, as shown in the graph of FIG. 16, when the Ti silicide film is formed on the p + type diffusion layer, the sheet resistance Rs of the Ti silicide film is similar to the case where the Ti silicide film is formed on the n + type diffusion layer. The line width dependency of appears. Thus, when a Ti silicide film is formed on a fine line, the sheet resistance Rs of the film is increased, which is a so-called thin line effect.

[0005]

On the other hand, in the case of Co silicide, as shown in the graph of FIG. 17, when the Co silicide film is formed on the n + type diffusion layer, the sheet resistance of the Co silicide film increases as the initial Co film becomes thicker. Although Rs is reduced, the sheet resistance Rs of the Co silicide film hardly changes even if the width W of the n + type diffusion layer is narrowed. The fact that the sheet resistance Rs of the Co silicide film does not depend on the line width as described above also means that the Co silicide film is formed on the p + -type diffusion layer as shown in the graph of FIG. It is the same.

[0006]

The graphs of FIGS. 17 and 18 show data in the case of a so-called TiN cap structure in which a CoN film is covered with a TiN film when the Co silicide film is formed. In the case where the Co silicide film is formed using only the Co film that does not have the same characteristics, basically the same characteristics are exhibited. Therefore, even when a Co silicide film is formed on a fine line, the thin line effect of increasing the sheet resistance Rs does not occur.

[0007]

As described above, since the thin line effect does not occur even when formed on a fine line, the

GF Exhibit 1124 - 1618/2704

Co silicide film has recently been studied more actively. The conventional Co silicide process will be described below with reference to FIGS.

[0008]

First, for example, by using a LOCOS (Local Oxidation of Slicon; selective oxidation) method, a LOCOS film 52 is selectively formed on a silicon substrate 50 to perform element isolation, and then a gate is formed on the silicon substrate 50 in the element region. A gate electrode 54 made of a polycrystalline silicon layer is formed through an oxide film (not shown). Then, by using, for example, an ion implantation method, impurities are selectively added to the surface layer portion of the silicon substrate 50 in the element region using the LOCOS film 52 and the gate electrode 54 as a mask to form the source region 56 and the drain region 58. Subsequently, after depositing an SiO2 film (silicon oxide film) on the entire surface of the substrate, the SiO2 film is removed by etching by a dry etching method, the SiO2 film is left on the side surface of the gate electrode 54, and the SiO2 film is left on the side surface of the gate electrode 54. A sidewall 60 made of is formed (see FIG. 19).

[0009]

Then, the Co film 62 is uniformly formed on the entire surface of the substrate by using, for example, the sputtering method (see FIG. 20). Then, using RTA (Rapid Thermal Annealing) method, a first annealing process is performed at a processing temperature of about 550 ° C. to perform a Co film on the gate electrode 54 and the source region 56 and the drain region 58. 62 is reacted with the underlying Si to form CoSi films 64, 66 and 68 which are high resistance Co silicides, respectively. At this time, the Co film 62 remains unreacted on the LOCOS film 52 and the sidewall 60 (see FIG. 21).

[0010]

Then, the Co film 62 remaining unreacted on the LOCOS film 52 and the sidewall 20 is selectively removed by etching using a wet etching method (see FIG. 22). Then, using the RTA method, a second annealing process is performed under the condition of a processing temperature of about 700 ° C., and the CoSi films 64, 66 and 68 which are high resistance Co silicides have the lowest resistance among Co silicides. The phase changes to the CoSi2 films 70, 72 and 74 which are the phases (see FIG. 23).

GF Exhibit 1124 - 1619/2704

[0011]

That is, this conventional Co silicide process uses polycrystalline silicon through the gate oxide film on the silicon substrate 50 in the element region separated by the LOCOS film 52 by using the LOCOS method, the ion implantation method, the dry etching method, or the like. Forming a gate electrode 54 made of a layer, forming a source region 56 and a drain region 58 on the surface layer of the silicon substrate 50, and forming a sidewall 60 on the side surface of the gate electrode 54; By the step of forming the Co film 62 and the first annealing process using the RTA method, the Co film 62 on the gate electrode 54 and the source region 56 and the drain region 58 reacts with the underlying Si to obtain a high resistance. After removing the unreacted Co film 62 on the LOCOS film 52 and the sidewalls 60 by using the step of forming the CoSi films 64, 66, and 68 that are Co silicide and the wet etching method, respectively, the RTA method is used. By the second annealing, the CoSi films 64, 66 and 68 are transformed into the CoSi2 films 70, 72 and 74, which have the lowest resistance among Co silicides, respectively.

[0012]

As described above, in the conventional Co silicide process, when the annealing treatment by the RTA method for forming the CoSi2 films 70, 72 and 74 is performed, the Co film 62 reacts with the underlying Si to form the CoSi film 64, The first annealing treatment at a treatment temperature of about 550 ° C. to form 66 and 68, and the treatment temperature at a treatment temperature of about 700 ° C. at which these CoSi films 64, 66 and 68 undergo phase transition to the CoSi 2 films 70, 72 and 74. By being divided into two stages including the second annealing process, not only the CoSi films 64, 66 and 68 are formed on the gate electrode 54 and the source region 56 and the drain region 58, but also the adjacent sidewalls 60. It is possible to prevent a so-called creeping phenomenon that a CoSi film is formed up to the top.

Therefore, the CoSi film 30 on the gate electrode 14 and the CoSi films 32 and 34 on the source region 16 and the drain region 18 are short-circuited via the CoSi film formed on the sidewall 20, that is, the gate electrode 14 and the source. The low resistance CoSi2 films 70, 72 and 74 are self-aligned on the gate electrode 54 and the source region 56 and the drain region 58 without causing a so-called bridging phenomenon in which the region 16 and the drain region 18 are short-circuited. It is formed.

[0013]

GF Exhibit 1124 - 1620/2704

However, in the above conventional Co silicide process, as shown in the graphs of FIGS. 24 and 25, Co silicide is formed on the n + type diffusion layer and the p + type diffusion layer, respectively. When the film is formed, a leak current with large variations occurs in these n + type diffusion layer and p + type diffusion layer. In particular, when a Co silicide film is formed on the n + type diffusion layer, there is a large difference in the generation of leak current depending on the annealing treatment temperature for siliciding the Co film formed on the n + type diffusion layer. That is, when the annealing temperature rises from 400 ° C to 450 ° C, the leak current increases sharply. Then, as the annealing temperature rises from 450 ° C to 700 ° C, the leakage current tends to decrease slightly.

[0014]

For this reason, as shown in FIG. 26, for example, the leakage current generated when the Co silicide film 78 is formed on the n + type diffusion layer 76 is a relatively low annealing temperature near 450 ° C. (K. Goto, et al., "Leakage Mechanism and Optimized Conditions of Co Process for Deep-Submicron CMOSDevices" IEDM (1995). (See p.449). It is considered that the formation of the Co silicide spike 80 is because Co atoms are abnormally diffused into the n + type diffusion layer 76 and Co silicide is formed only in that portion. Therefore, since Co silicide has no thin line effect as described above, it is extremely advantageous when it is applied to a semiconductor device that will be further miniaturized in the future, while Co silicide has a spike in Co silicide that occurs in the initial stage of the silicidation reaction. The generation of leak current caused by this is a major obstacle to application to actual devices.

[0015]
Therefore, the present invention has been made in view of the above circumstances, and when forming a silicide film, it is possible to prevent formation of a spike of silicide that causes a leak current, and to achieve high reliability and high speed. It is an object to provide a method for manufacturing a semiconductor device.

[0016]

The above object can be achieved by the following method for manufacturing a semiconductor device according to the present invention.

GF Exhibit 1124 - 1621/2704

That is, in the method of manufacturing a semiconductor device according to the first aspect, after the metal film is formed on the entire surface of the base body including the silicon region, the metal film is reacted with Si in the silicon region by heat treatment to form the silicide film on the silicon region. A method of manufacturing a semiconductor device, which is formed in a consistent manner, characterized by including a step of forming a thin film for spike prevention on a silicon region before forming a metal film on the entire surface of a substrate including a silicon region. .

[0017]

As described above, in the method of manufacturing a semiconductor device according to the first aspect, before forming the metal film on the entire surface of the substrate including the silicon region, the spike preventing thin film is formed on the silicon region, so that the silicon is heat-treated. When reacting Si in the region with the metal, a thin film for preventing spikes is interposed between the silicon region and the metal film, so that local abnormal diffusion of metal atoms occurs at the initial stage of the silicidation reaction. Are suppressed and the metal atoms are uniformly diffused to prevent the formation of silicide spikes. Therefore, generation of a leak current due to the spike of the silicide is prevented.

[0018]

Note that here, the silicon region includes both a polycrystalline silicon region and a single crystal silicon region. Further, since the spike preventing thin film interposed between the silicon region and the metal film is extremely thin, it does not prevent the silicidation reaction between Si and the metal.

[0019]

A method of manufacturing a semiconductor device according to a second aspect is the method of manufacturing a semiconductor device according to the first aspect, wherein the metal film is a Co film, and a silicide film is formed by a reaction with Si. In particular, even in the case of a Co film in which a silicide spike is easily formed, since a thin film for preventing spikes is interposed between the silicon region and the Co film, the local occurrence of the silicide reaction occurs at the initial stage. Such abnormal diffusion of Co atoms is suppressed, Co atoms are uniformly diffused, and formation of spikes of Co silicide is prevented. Therefore, generation of a leak

GF Exhibit 1124 - 1622/2704

current due to the spike of Co silicide is prevented.

[0020]
Further, a method for manufacturing a semiconductor device according to a third aspect is the method for manufacturing a semiconductor device according to the first aspect, wherein the spike prevention thin film is made of a SiN film (silicon nitride film). Since the silicidation reaction is not disturbed as in the case where the natural oxide film is interposed between the region and the metal film, the SiN film interposed between the silicon region and the metal film has a local abnormality of metal atoms. The function as a spike prevention thin film at the time of forming a silicide film of suppressing diffusion is well exhibited.

[0021]
The method of manufacturing a semiconductor device according to claim 4 is the method of manufacturing a semiconductor device according to claim 3, wherein the step of forming the spike-preventing thin film made of a SiN film uses a RTA method to form a silicon region. Since the entire surface of the substrate including is subjected to an annealing treatment in an NH3 (ammonia) atmosphere to form a SiN film on the surface of the silicon region, the silicidation reaction between Si and metal can be prevented. In addition, a dense SiN film having a film thickness necessary and sufficient to function as a spike preventing thin film when forming a silicide film is easily formed.

[0022]

A method of manufacturing a semiconductor device according to a fifth aspect is the method of manufacturing a semiconductor device according to the second aspect, wherein a Co film is formed on the entire surface of the base body including a silicon region, and then a Co film for preventing oxidation is formed on the Co film. By adopting a configuration including a step of forming a thin film, Co is originally a metal film that is very easily oxidized, but it is covered with a thin film for oxidation protection, so the Co film is protected from surface oxidation by exposure to the atmosphere. To be done.

A TiN film is suitable as a thin film for preventing the oxidation of the Co film.

[0023]

GF Exhibit 1124 - 1623/2704

BEST MODE FOR CARRYING OUT THE INVENTION Embodiments of the present invention will be described below with reference to the accompanying drawings.

(First Embodiment) FIGS. 1 to 6 are process sectional views for explaining a Co silicide process according to a first embodiment of the present invention. First, the LOCOS film 12 is selectively formed on the silicon substrate 10 by using, for example, the LOCOS method, and element isolation is performed. After that, a gate electrode 14 made of a polycrystalline silicon layer is formed on the silicon substrate 10 in the element region separated by the LOCOS film 12 with a gate oxide film (not shown) interposed therebetween.

[0024]

Subsequently, by using, for example, an ion implantation method, impurities are selectively added to the surface layer portion of the silicon substrate 10 in the element region using the LOCOS film 12 and the gate electrode 14 as a mask to form the source region 16 and the drain region 18. Then, after depositing an SiO2 film on the entire surface of the substrate, the SiO2 film is removed by etching by a dry etching method, and the SiO2 film is left on the side surface of the gate electrode 14. Thus, the side wall 20 made of the SiO2 film is formed on the side surface of the gate electrode 14 (see FIG. 1).

[0025]

Then, by RTA method, the entire substrate with the upper surface of the gate electrode 14 and the surfaces of the source region 16 and the drain region 18 exposed is heat-treated in an NH3 atmosphere. In this way, the upper surface of the gate electrode 14 and the surfaces of the source region 16 and the drain region 18 are nitrided to form dense SiN thin films 22, 24 and 26 having a film thickness of 1.5 nm, respectively (see FIG. 2). The heat treatment conditions using the RTA method when forming these SiN thin films 22, 24, and 26 with a film thickness of 1.5 nm are as follows: NH3 atmosphere gas flow rate: 5 sccm Treatment temperature: 900 ° C. Treatment time: 30 seconds

[0026]

GF Exhibit 1124 - 1624/2704

Next, a 10 nm-thickness Co film 28 is uniformly formed on the entire surface of the substrate by using, for example, a sputtering method (see FIG. 3). The film forming conditions for forming the Co film 28 having a film thickness of 10 nm are as follows: DC power: 0.8 kW Pressure: 0.4 Pa Ar (argon) gas flow rate for heater: 30 sccm Ar gas flow rate for process: 60 sccm Substrate heating temperature: 150 ° C

[0027]

Next, the RTA method is used to perform the first annealing treatment in a N 2 (nitrogen) atmosphere on the substrate on which the Co film 28 is formed on the entire surface thereof, to thereby form the gate electrode 14, the source region 16 and the drain. The Co film 28 on the region 18 is reacted with the underlying Si to form CoSi films 30, 32, and 34 that are high-resistance Co silicide. At this time, the Co film 28 remains unreacted on the LOCOS film 12 and the sidewall 20 (see FIG. 4). The annealing treatment conditions using the first RTA method when forming these CoSi films 30, 32 and 34 are as follows: N2 atmosphere gas flow rate: 10 sccm Treatment temperature: 550 ° C. Treatment time: 30 seconds

[0028]
At this time, the polycrystalline silicon surface of the gate electrode 14 and the single crystal silicon surfaces of the source region 16 and the drain region 18 (hereinafter, both the polycrystalline silicon surface and the single crystal silicon surface are collectively referred to as "silicon surface").) And the Co film 28, the SiN thin films 22, 24, and 26 are interposed respectively, but since the SiN thin films 22, 24, and 26 have a very thin film thickness of 1.5 nm, the Co film 28 Does not block the reaction with the silicon surface of the gate electrode 14 and the source and drain regions 16 and 18.

[0029]

Further, when the first annealing treatment is performed under the above conditions, in the conventional case, CoSi spikes were usually formed as shown in FIG. 26, but in the present embodiment, Since the SiN thin films 22, 24, and 26 are interposed between the Co film 28 and the Co film 28 and the underlying silicon surface, the local abnormal diffusion of Co atoms is suppressed, and the Co atoms are uniformly diffused. , CoSi spikes are no longer formed.

That is, the SiN thin films 22, 24 and 26 function as spike preventing thin films when the CoSi

GF Exhibit 1124 - 1625/2704

films 30, 32 and 34 are formed.

[0030]
Further, in the present embodiment, since the annealing treatment is performed under the condition of the treatment temperature of 550 ° C. and the treatment time of 30 seconds, the CoSi film is formed also on the sidewall 20 and the CoSi film 30 on the gate electrode 14. A short circuit between the CoSi films 32 and 34 on the source region 16 and the drain region 18, that is, a short circuit between the gate electrode 14 and the source region 16 and the drain region 18, that is, a bridging phenomenon due to so-called CoSi film climbing may occur. Absent.

[0031]

Then, the Co film 28 remaining in the unreacted state on the LOCOS film 12 and the sidewalls 20 is selectively removed by etching using a wet etching method (see FIG. 5).

The wet etching conditions for the unreacted Co film 28 are as follows: chemical solution: sulfuric acid / hydrogen peroxide (H2 SO4: H2 O2 = 4: 1) chemical solution temperature: 70 ° C. Treatment time: 3 minutes

[0032]
Next, the RTA method is used to perform a second annealing treatment in a N 2 atmosphere on the substrate on which the CoSi films 30, 32, and 34 are formed on the gate electrode 14 and the source region 16 and the drain region 18, respectively. Then, the CoSi films 30, 32, and 34 undergo phase transition to the CoSi2 films 36, 38, and 40, which have the lowest resistance among the Co silicides (see FIG. 6).

[0033]
The second annealing treatment condition for the phase transition of the CoSi films 30, 32, 34 into the CoSi2 films 36, 38, 40 is as follows: N2 atmosphere gas flow rate: 10 sccm Processing temperature: 700 ° C Processing time: 30 Second

[0034]
As described above, according to this embodiment, the gate electrode 14 made of the polycrystalline silicon layer and the source region 16 and the drain region 18 at the surface layer

GF Exhibit 1124 - 1626/2704

of the silicon substrate 10 are heat-treated in the NH 3 atmosphere using the RTA method. After forming the SiN thin films 22, 24 and 26 having a film thickness of 1.5 nm on the substrate, a Co film 28 having a film thickness of 10 nm is formed on the entire surface of the substrate, and the Co film 28 is formed by the first annealing treatment using the RTA method. By reacting with the underlying Si, CoSi films 30, 32, and 34 that are high-resistance Co silicide are formed, and have the lowest resistance phase among the Co silicides by the second annealing treatment using the RTA method. Although the phase transition has occurred in the CoSi2 films 36, 38 and 40, when the Co film 28 and the underlying Si are reacted by the first annealing treatment using the RTA method, the gate electrode 14, the source region 16 and the drain are formed. Since the spike-preventing SiN thin films 22, 24, and 26 are interposed between the region 18 and the Co film 28, local abnormal diffusion of Co atoms is suppressed, and the Co atoms are uniformly diffused. Since the formation of the spike of silicide can be prevented, it is possible to prevent the generation of the leak current due to the spike of Co silicide, and it is possible to improve the reliability of the semiconductor device.

[0035]
Further, since the generation of the leak current can be prevented in this way, the film thickness of the low resistance CoSi2 films 36, 38 and 40 can be further increased sufficiently, and thus the CoSi2 films 36 and 38 can be made thicker. , 40, the resistance of the gate electrode 14 and the source region 16 and the drain region 18 can be further reduced, and the operation speed of the semiconductor device can be further increased.

[0036]

(Second Embodiment) FIGS. 7 to 14 are process cross-sectional views for explaining a Co silicide process according to a second embodiment of the present invention.

The same elements as those shown in FIGS. 1 to 6 are designated by the same reference numerals and the description thereof will be omitted.

First, by using the LOCOS method, the LOCOS film 12 is selectively formed on the silicon substrate 10 to perform element isolation, and then the gate oxide film (on the silicon substrate 10 in the element region isolated by the LOCOS film 12). A gate electrode 14 made of a polycrystalline silicon film is formed through (not shown).

GF Exhibit 1124 - 1627/2704

[0037]
Subsequently, by using the ion implantation method, impurities are selectively added to the surface layer portion of the silicon substrate 10 in the element region to form the source region 16 and the drain region 18, and then a gate electrode is formed by depositing a SiO2 film and dry etching the same. A sidewall 20 made of a SiO2 film is formed on the side surface 14 (see FIG. 7).

[0038]

Then, using RTA, the entire substrate is heat-treated in an NH3 atmosphere to nitride the upper surface of the gate electrode 14 and the surfaces of the source region 16 and the drain region 18, and the dense SiN thin films 22 and 24 having a thickness of 1.5 nm. 26 are formed respectively (see FIG. 8).

The RTA processing conditions for forming the SiN thin films 22, 24 and 26 having a film thickness of 1.5 nm are the same as in the case of the first embodiment.

[0039]

Then, a 10 nm-thickness Co film 28 is uniformly formed on the entire surface of the substrate by using the sputtering method (see FIG. 9).

The film forming conditions for forming the Co film 28 having the film thickness of 10 nm are the same as in the case of the first embodiment.

[0040]

Next, a TiN cap film 42 having a film thickness of 20 nm is formed on the Co film 28 by using, for example, a sputtering method without exposing the substrate on which the Co film 28 is uniformly formed to the atmosphere (see FIG. 10). ..

The film forming conditions for forming the TiN cap film 42 are: DC power: 6.5 kW Pressure: 0.4

GF Exhibit 1124 - 1628/2704

Pa Ar gas flow rate for heater: 15 sccm N2 gas flow rate for process: 135 sccm Substrate heating temperature: 150 ° C

[0041]

At this time, since the Co film 28 formed on the entire surface of the substrate in the sputtering chamber in the previous step is covered with the TiN cap film 42 without being exposed to the atmosphere, it is originally very oxidized. The Co film 28, which is a susceptible metal film, is protected from being exposed to the atmosphere and oxidizing its surface. That is, the TiN cap film 42 functions as an oxidation preventing film for the Co film 28.

[0042]

Next, the RTA method is used to perform a first annealing treatment in an N2 atmosphere on the base body on which the Co film 28 and the TiN cap film 42 are sequentially laminated on the entire surface, thereby performing the gate electrode 14, the source region 16 and the drain region. The Co film 28 on 18 is reacted with the underlying Si to form CoSi films 30, 32, and 34 that are high-resistance Co silicide, and the unreacted Co film is formed on the LOCOS film 12 and the sidewalls 20. 28 remains (see FIG. 11). The conditions of the first annealing treatment for forming these CoSi films 30, 32, 34 are the same as in the case of the first embodiment.

[0043]

At this time, similar to the case of the first embodiment, the film thickness 1. functioning as a spike preventing thin film is provided between the Co film 28 and the silicon surface of the gate electrode 14, the source region 16 and the drain region 18. Since the 5 nm SiN thin films 22, 24, and 26 are respectively interposed, the local Co atoms can be prevented without blocking the reaction between the silicon film of the gate electrode 14 and the source region 16 and the drain region 18 and the Co film 28. Since the abnormal diffusion of Co is suppressed and Co atoms are uniformly diffused, the CoSi films 30, 32, and 34 are formed, and the formation of CoSi spikes is prevented. Also in this embodiment, as in the case of the first embodiment, since the annealing treatment is performed under the conditions of the treatment temperature of 550 ° C. and the treatment time of 30 seconds, the bridging phenomenon due to the creeping-up of the CoSi film. Will never happen.

GF Exhibit 1124 - 1629/2704

[0044]

Next, by using, for example, a wet etching method, the TiN cap film 42 formed on the Co film 28 as an oxidation preventing film of the Co film 28 is removed by etching (see FIG. 12). The wet etching conditions for the TiN cap film 42 are as follows: chemical solution: ammonia hydrogen peroxide (NH4 OH: H2 O2: H2 O = 1: 2: 6) chemical solution temperature: 65 ° C. processing time: 3 minutes

[0045]

Next, the unreacted Co film 28 on the LOCOS film 12 and the sidewalls 20 is selectively removed by etching using a wet etching method (see FIG. 13). The wet etching conditions for the unreacted Co film 28 are the same as in the case of the first embodiment.

[0046]

Then, the RTA method is used to perform a second annealing treatment in an N 2 atmosphere on the substrate on which the CoSi films 30, 32, and 34 are formed on the gate electrode 14 and the source region 16 and the drain region 18, respectively. These CoSi films 30, 32 and 34 undergo phase transition to the CoSi2 films 36, 38 and 40 which have the lowest resistance among Co silicides (see FIG. 14). The conditions of the second annealing treatment when the CoSi films 30, 32 and 34 are phase-transitioned to the CoSi2 films 36, 38 and 40 are the same as those in the first embodiment.

[0047]

As described above, according to the present embodiment, the gate electrode 14, the source region 16 and the drain region are formed by combining the first embodiment with the so-called TiN cap process, that is, by the heat treatment in the NH 3 atmosphere using the RTA method. After forming SiN thin films 22, 24, and 26 on 18 respectively and forming a Co film 28 on the entire surface of the substrate, a TiN cap film 42 is formed on this Co film 28 as an oxidation preventing film, and then The CoSi films 30, 32, and 34 are formed by the first annealing process using the RTA method, and the phase transition to the CoSi2 films 36, 38, and 40 is performed

GF Exhibit 1124 - 1630/2704

by the second annealing process using the RTA method. Since the entire surface of the Co film 28 after the film is covered with the TiN cap film 42 and protected from surface oxidation due to exposure to the atmosphere, the CoSi films 30, 32, and 34 are formed by the subsequent first annealing treatment, and further the second time. It is possible to stably perform the phase transition to the CoSi2 films 36, 38 and 40 by the annealing treatment of. Therefore, in addition to achieving the same effect as in the case of the first embodiment, the CoSi2 films 36, 38, 40 having low resistance can be formed more stably, so that the reliability is higher and the speed is higher. It becomes possible to manufacture a semiconductor device.

[0048]

As described in detail above, according to the method of manufacturing a semiconductor device of the present invention, the following effects can be obtained. That is, according to the method of manufacturing a semiconductor device according to claim 1, before forming the metal film on the entire surface of the base body including the silicon region, a thin film for preventing spikes is formed on the silicon region to form the silicon region. Since a thin film for preventing spikes is interposed between the metal film and the metal film, when the Si in the silicon region is reacted with the metal by heat treatment, the local abnormal diffusion of metal atoms occurs at the initial stage of the silicidation reaction. It is possible to prevent the formation of a silicide spike by uniformly diffusing the metal atoms, and it is possible to prevent a leak current from being generated due to the silicide spike. Further, since it is possible to prevent the occurrence of such a leak current, it is possible to further increase the thickness of the low-resistance silicide film, thereby further reducing the resistance of the silicon region in which the silicide film is formed. be able to. Therefore, it becomes possible to manufacture a highly reliable and high performance semiconductor device.

[0049]

Further, according to the method of manufacturing a semiconductor device according to claim 2, in the method of manufacturing a semiconductor device according to claim 1, since the metal film is a Co film, a Co film that is particularly apt to form a spike of silicide is formed. Even in this case, when the silicide film is formed by the reaction with Si in the silicon region, a spike prevention thin film is interposed between the silicon region and the Co film, so that a local Co atom abnormality occurs. The diffusion is suppressed, Co atoms are uniformly diffused, and it becomes possible to prevent the formation of spikes of Co silicide. Therefore, it is possible to prevent the generation of a leak current due to the spike of Co silicide, and to prevent the generation of such a leak current. Therefore, the Co silicide film having the lowest resistance,

GF Exhibit 1124 - 1631/2704

that is, the film of the CoSi2 film. It is possible to further increase the thickness and further reduce the resistance of the silicon region in which the CoSi2 film is formed, for example, the gate electrode, the source region and the drain region, resulting in higher reliability and higher speed. It becomes possible to manufacture a semiconductor device.

[0050]
Further, according to the method of manufacturing a semiconductor device according to claim 3, in the method of manufacturing a semiconductor device according to claim 1, since the thin film for preventing spikes is made of a SiN film, a gap between the silicon region and the metal film is formed. Since the SiN film is interposed between the SiN film and the SiN film, it is possible to suppress the local abnormal diffusion of metal atoms and uniformly diffuse the metal atoms to function as a spike preventing thin film when forming a silicide film.

[0051]
According to the method of manufacturing a semiconductor device according to claim 4, in the method of manufacturing a semiconductor device according to claim 3, the step of forming the spike-preventing thin film made of a SiN film uses an RTA method. Since the entire surface of the substrate including the silicon region is annealed in an NH3 atmosphere to form a SiN film on the surface of the silicon region, a silicide film is formed without blocking the reaction between Si and a metal. It becomes possible to easily form a dense SiN film having a necessary and sufficient film thickness to function as a spike prevention thin film at the time of etching.

[0052]
Further, according to the method of manufacturing a semiconductor device according to claim 5, in the method of manufacturing a semiconductor device according to claim 2, after a Co film is formed on the entire surface of the substrate including a silicon region, for example, TiN is formed on the Co film. Since the Co film is protected from being surface-oxidized by exposure to the atmosphere by including the step of forming the oxidation-preventing thin film made of a film, the Co film is more protected than the semiconductor device manufacturing method according to claim 2. The Co silicide film can be formed more stably.

[0053]
Brief description of the drawings

[0054]
1 is a process sectional view (1) for explaining the Co silicide process according to the first

GF Exhibit 1124 - 1632/2704

embodiment of the present invention.

[0055]
2 is a process cross-sectional view (No. 2) for explaining the Co silicide process according to the first embodiment of the present invention.

[0056]
3 is a process sectional view (3) for explaining the Co silicide process according to the first embodiment of the present invention.

[0057]
4 is a process sectional view (4) for explaining the Co silicide process according to the first embodiment of the present invention.

[0058]
5 is a process sectional view (5) for explaining the Co silicide process according to the first embodiment of the present invention. FIG.

[0059]
6 is a process sectional view (6) for explaining the Co silicide process according to the first embodiment of the present invention.

[0060]
7 is a process sectional view (1) for explaining the Co silicide process according to the second embodiment of the present invention.

[0061]
8 is a process cross-sectional view (No. 2) for explaining the Co silicide process according to the second embodiment of the present invention.

[0062]
9 is a process sectional view (3) for explaining the Co silicide process according to the second embodiment of the present invention.

GF Exhibit 1124 - 1633/2704

[0063]
10 is a process sectional view (4) for explaining the Co silicide process according to the second embodiment of the present invention.

[0064]
FIG. 11 is a process sectional view (5) for explaining the Co silicide process according to the second embodiment of the present invention.

[0065]
FIG. 12 is a process sectional view (6) for explaining the Co silicide process according to the second embodiment of the present invention.

[0066]
13 is a process cross-sectional view (No. 7) for explaining the Co silicide process according to the second embodiment of the present invention.

[0067]
14 is a process sectional view (8) for explaining the Co silicide process according to the second embodiment of the present invention.

[0068]
15 is a graph showing the line width dependence of the sheet resistance Rs of the Ti silicide film formed on the n + type diffusion layer.

[0069]
16 is a graph showing the line width dependence of the sheet resistance Rs of the Ti silicide film formed on the p + type diffusion layer.

[0070]
17 is a graph showing the line width dependence of the sheet resistance Rs of the Co silicide film formed on the n + type diffusion layer.

GF Exhibit 1124 - 1634/2704

[0071]
18 is a graph showing the line width dependence of the sheet resistance Rs of the Co silicide film formed on the p + type diffusion layer.

[0072]
19 is a process sectional view (1) for explaining the conventional Co silicide process.

[0073]
20 is a process sectional view (2) for explaining the conventional Co silicide process.

[0074]
21 is a process sectional view (3) for explaining the conventional Co silicide process.

[0075]
22 is a process sectional view (4) for explaining the conventional Co silicide process.

[0076]
23 is a process sectional view (5) for explaining the conventional Co silicide process.

[0077]
FIG. 24 is a graph showing a cumulative frequency distribution of leak current depending on a silicide temperature when forming a Co silicide film on the n + type diffusion layer.

[0078]
FIG. 25 is a graph showing a cumulative frequency distribution of leak current depending on a silicide temperature when forming a Co silicide film on a p + type diffusion layer.

[0079]
26 is a schematic view showing a spike of Co silicide formed in the conventional Co silicide process.

GF Exhibit 1124 - 1635/2704

[0080]
Explanation of symbols

[0081]
10 ... Silicon substrate, 12 ... LOCOS film, 14 ... Gate electrode, 16 ... Source region, 18 ... Drain region, 20 ... Side wall, 22, 24, 26 ... SiN thin film, 28 ... Co film, 30, 32, 34 ... CoSi film, 36, 38, 40 ... CoSi2 film, 42 ... TiN cap film, 50 ... Silicon substrate, 52 ... LOCOS film, 54 ... Gate electrode, 56 ... Source region, 58 ... Drain region, 60 ... Sidewall, 62 ... Co film, 64, 66, 68 ... CoSi film, 70, 72, 74 ... CoSi2 film, 76 ... N + type diffusion layer, 78 ... Co silicide film, 80 ... Co silicide spike.

GF Exhibit 1124 - 1636/2704

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

CLAIMS JPH10335265

1.
A method of manufacturing a semiconductor device, comprising forming a metal film on the entire surface of a substrate including a silicon region, and then heat treating the metal film to react with Si in the silicon region to form a silicide film on the silicon region in a self-aligned manner. A method for manufacturing a semiconductor device, further comprising the step of forming a spike prevention thin film on the silicon region before forming the metal film on the entire surface of the substrate including the silicon region.

2.
The method of manufacturing a semiconductor device according to claim 1, wherein the metal film is a Co film.

3.
The method of manufacturing a semiconductor device according to claim 1, wherein the spike prevention thin film is a SiN film.

4.
4. The method of manufacturing a semiconductor device according to claim 3, wherein the step of forming the spike-preventing thin film made of the SiN film is performed in a NH3 atmosphere on the entire surface of the substrate including the silicon region by using a short time heat treatment method. A method of manufacturing a semiconductor device, comprising a step of performing an annealing treatment to form the SiN film on the surface of the silicon region.

GF Exhibit 1124 - 1637/2704

5.

The method of manufacturing a semiconductor device according to claim 2, further comprising the step of forming the oxidation preventive thin film on the Co film after forming the Co film on the entire surface of the substrate including the silicon region. Method of manufacturing semiconductor device.

6.

The method for manufacturing a semiconductor device according to claim 5, wherein the oxidation preventing thin film is a TiN film.

GF Exhibit 1124 - 1638/2704

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報**（Ａ）　(11)特許出願公開番号

特開平11－162874

(43)公開日　平成11年(1999)６月18日

(51)Int.Cl.[6]	識別記号	ＦＩ	
Ｈ０１Ｌ　21/283		Ｈ０１Ｌ　21/283	Ｃ

審査請求　未請求　請求項の数３　ＦＤ　（全　５　頁）

(21)出願番号　特願平9－347162

(22)出願日　平成９年(1997)12月１日

(71)出願人　000002037
新電元工業株式会社
東京都千代田区大手町２丁目２番１号

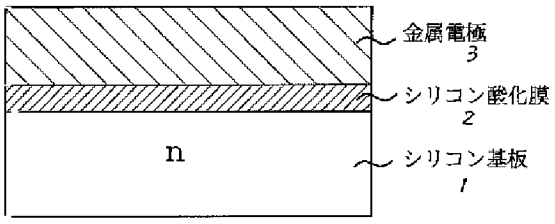
(72)発明者　岩黒　弘明
埼玉県飯能市南町10番13号新電元工業株式会社工場内

(54)【発明の名称】　オーム性接合電極およびこれを用いた半導体装置

(57)【要約】　（修正有）

【課題】　シリコン基板上に金属膜を形成してオーミック電極を形成するとき、そのシリコン基板の不純物の数は理論上１ｃｍ^{3}当たり１０^{20}個以上必要であるが、この不純物濃度よ売りも低いシリコン基板に対しても良好な低接触抵抗を示すオーム性接合電極を提供する。

【解決手段】　シリコン基板１とオーム接合用金属３との間にシリコンサブ酸化膜［ＳｉＯｘ（ｘ＝０．５，１．０，１．５）］２を介在せしめ且つ前記酸化膜の厚さを０．３ｎｍ～２．２５ｎｍとしたことを特徴とする。



GF Exhibit 1124 - 1639/2704

【特許請求の範囲】
【請求項１】　シリコン基板とオーム接合用金属との間にシリコンサブ酸化膜［ＳｉＯｘ（ｘ＝０．５，１．０，１．５）］を介在せしめ且つ前記酸化膜の厚さを０．３ｎｍ～２．２５ｎｍとしたことを特徴とするオーム性接合電極。
【請求項２】　ｎ型シリコン基板を用い且つ前記基板の不純物濃度を10^{16}ｃｍ$^{-3}$乃至10^{20}ｃｍ$^{-3}$としたことを特徴とする請求項１のオーム性接合電極。
【請求項３】　シリコン基板に能動領域を形成し、前記シリコン基板の表面もしくは裏面にシリコンサブ酸化膜［ＳｉＯｘ（ｘ＝０．５，１．０，１．５）］を介して電極金属を接合したことを特徴とする半導体装置。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明はオーム性接合電極及びこれを用いた半導体装置に関するものである。
【０００２】
【従来の技術】シリコン電子デバイスを作る上で金属半導体接合は重要な要素である。この接合には、整流性を示すショットキー接合、他は整流性のないオーム性接合の２つがある。ｎ型シリコン基板と金属を接触させて良好な低接触抵抗を示すオーム性接合電極を形成するには、理論上、シリコン基板の不純物濃度を10^{20}ｃｍ$^{-3}$以上にする必要がある。実用的には、シリコン基板の不純物濃度が10^{19}から10^{20}ｃｍ$^{-3}$でオーム性接合を作っている。シリコンに不純物を多量に導入するために、イオン注入・熱処理法や不純物デポジション・熱拡散法などの方法が使われてきた。
【０００３】最近のシリコンウェーハの大口径化に伴い、ウェーハの厚さは厚くなっている。縦型構造のパワーデバイスにおいては、ウェーハの厚さが厚くなることは、オ
（２）
ン抵抗の上昇を引き起こすことになるので、このオン抵抗の上昇を抑えるためにウェーハ表側のデバイスを作製した後、組み立て前にウェーハを裏側から削って薄くする。この裏側を薄くした後、裏側にオーム性接合電極を作製する。しかしながら、このときシリコン基板の不純物濃度は、10^{20}ｃｍ$^{-3}$よりも低いことが多い。表側にデバイスがすでにできており、Ａ１などの金属配線がなされているため、高温熱処理が困難であり、イオン注入・熱処理法や不純物デポジション・熱拡散法を使って意識的に不純物をシリコン基板に導入することはできない。又、特開平７－３０７３０６号に示すように半導体基板表面に電荷を内存する薄膜を設けてオーム性電極を形成することも提案されている。
【０００４】
【発明が解決しようとする課題】本発明はこのような問題に対して、たとえシリコン基板の不純物濃度が10^{20}ｃｍ$^{-3}$よりも低くても良好な低接触抵抗を示すオーム性接合を提供するものである。通常、シリコン基板の不純物濃度が低いとき、その上に金属膜を堆積させると、金属とシリコン基板の間でショットキー接触となる。このような場合でも、金属とシリコン基板の間にシリコン酸化膜を介することで、良好な低接触抵抗を示すオーム性接合を得る。
【０００５】
【課題を解決するための手段】本発明は、シリコン基板とオーム接合用金属との間にシリコンサブ酸化膜［ＳｉＯｘ（ｘ＝０．５，１．０，１．５）］を介在せしめ且つ前記酸化膜の厚さを０．３ｎｍ～２．２５ｎｍとしたことを特徴とする。
【０００６】シリコン基板を熱酸化法やプラズマ酸化法で酸化させると、２酸化シリコン（ＳｉＯ2）がシリコン基板上には生成される。この２酸化シリコンとシリコン基板の界面には、２酸化シリコン（ＳｉＯ2）ではなく、サブシリコン酸化膜［ＳｉＯｘ（ｘ＝０．５，１．０，１．５）］が形成される。このサブシリコン酸化膜の厚さは界面から２ｎｍ程度である。本発明の電極構造のシリコン酸化膜とは
（３）
このサブ酸化膜［ＳｉＯｘ（ｘ＝０．５，１．０，１．５）］のことである。金属膜とサブシリコン酸化膜とを接触させることによって、良好で低接触抵抗を示すオーム性接合が得られる。サブシリコン酸化膜の化学的な活性さによって、本発明の効果が得られるものと思われるが、詳細な理由は明確ではない。２酸化シリコン層と金属膜を接触させると、効果はまったくなくなる。
【０００７】
【実施例】図１は本発明の一実施例を示す断面図で図中１はシリコン基板、２はシリコンサブ酸化膜、３は電極金属である。図２は本発明の酸化膜の厚さの有効性を調べるためのデバイス構造を示す。使用したシリコン基板は、抵抗率が２ｍΩｃｍ（不純物濃度：8×10^{19}ｃｍ$^{-3}$）のｎ+シリコン基板６に、抵抗率が０．５Ωｃｍ（不純物濃度：10^{16}ｃｍ$^{-3}$）のシリコンエピタクシャル層５を５μｍ成長させたものを使用した。このエピタクシャル面はミラーポリッシュ加工されており、表面のひずみは小さい。
【０００８】図２の構造を作製するための製造プロセスは、まず、シリコン基板を希沸酸で１分間洗浄した後、ドライ酸化法を用いて８００℃、３０分間酸化させた。酸化膜厚は約３ｎｍである。次に、その酸化膜の厚さを変えるために希沸酸（ＨＦ：H_2O＝１：１００）液中に一定の時間だけ浸漬させた。この希沸酸で上記３ｎｍの酸化膜を完全にエッチングするには、１００秒の時間がかかった。さらに、上部電極４を形成するために、シリコンエピタクシャル層５の上にチタン膜をスパッタ法で５００ｎｍの厚さに堆積した後、ホトリソグラフィ技

GF Exhibit 1124 - 1640/2704

術を使って図２に示すように０．９ｍｍ角にパターン化した。チタンの化学エッチングには希沸酸を使用した。エッチング時間は２．５分間である。ホトレジストは、沸騰硝酸を用いて除去した。最後に、シリコン基板の裏側にチタンを１００ｎｍ、ニッケルを５００ｎｍ、銀を１００ｎｍ真空蒸着し、下部電極７を形成した。下部電極７はオーム性接合電極である。

【０００９】（４）

図３は各ＨＦ浸漬時間に対する評価デバイス（図２）の電流－電圧特性を示すもので、図２において電極４をプラス（＋）、電極７をマイナス（－）にした時を第一象限に示し（順方向特性）、又極性を逆にした時を第３象限に示した（逆方向特性）ものである。ＨＦ浸漬しない時（酸化膜の厚さ３ｎｍ）図中特性Ａに示すように順方向、逆方向共、電流は全く流れない。ＨＦ浸漬時間を増加するのに伴って電流は両方向共流れ始め酸化膜が厚さ１．５ｎｍで（浸漬時間５０秒）で特性Ｂに示すオーミック特性が得られている。更に浸漬時間を増し約１００秒で酸化膜はなくなり特性Ｃに示す整流特性（ショットキー特性）になった。

【００１０】図４は図３の電流－電圧特性から抵触抵抗の変化を示す値（ΔＲ）のＨＦ浸漬時間依存性を示す特性図で横軸は浸漬時間Ｓ（秒）、縦軸に変化値ΔＲ（ｍΩｃｍ^2）を示す。なお、ΔＲは酸化膜を介さない従来デバイスの抵抗値（図３Ｃ）を基準に算出した。又、この時の抵抗値は第１象限の特性から求めた。この方法により接触抵抗以外の抵抗成分は相殺され、接触抵抗の変化分のみ得られる。ΔＲの値がマイナス（負）であることは従来デバイスより接触抵抗が減少していることを意味する。このマイナス領域は図４から明らかなように浸漬時間で２５秒～９０秒の範囲即ち残余の酸化膜の厚さ２．２５ｎｍ～０．３ｎｍに相当する。

【００１１】図５は酸化法をO_2プラズマ照射法および基板を２ｍΩｃｍにしたとき、接触抵抗が改善されるかどうかを調べるためのデバイス構造を示す。使用したシリコン基板は、抵抗率が２ｍΩｃｍ（不純物濃度：８×10^{19}ｃｍ$^{-3}$）のn^+シリコン基板６を使用した。この構造を作製するため、まず、シリコン基板を希沸酸で１分間洗浄した後、マイクロ波プラズマ照射装置で酸素プラズマをシリコンに照射させた。すなわち、シリコン基板の表側のみに酸素プラズマを照射させ、酸化させた。プラズマパワーを１０００Ｗ、酸素圧を０．５Ｔｏｒｒ、照射時間を２分とした。このときの酸化膜の厚さは２．５ｎｍであった。次に、その酸化膜の厚さを変えるために希沸酸（ＨＦ：H_2O＝１：１００）液中に一定時間だけ浸漬させ、さらに、上部電極４を形成するために、シリコンの上にチタン膜をスパ

（５）

ッタ法で５００ｎｍの厚さに堆積した後、ホトリソグラフィ技術を使って０．９ｍｍ角にパターン化した。チタンの化学エッチングには希沸酸を使用した。エッチング時間は２．５分間である。ホトレジストは、沸騰硝酸を用いて除去した。最後にシリコン基板の裏側にチタンを１００ｎｍ、ニッケルを５００ｎｍ、銀を１００ｎｍ真空蒸着し、下部電極７を形成した。下部電極７はオーム性接合電極である。

【００１２】図６は酸化膜厚に対するデバイスの（図５）電流－電圧特性を示したものである。この特性は、図５において上部電極４をプラス、下部電極７をマイナスにしたときと第１象限に描き、逆の場合を第３象限に描いている。ＨＦ浸漬をしないとき（酸化膜厚：２．５ｎｍ）、電流は順、逆の両方向とも流れていない（Ａ）。ＨＦ浸漬を３０秒行って、酸化膜の厚さを、１．６ｎｍとしたとき、電流－電圧特性Ｂが得られた。さらに、浸漬時間を９０秒行って酸化膜を完全にエッチングすると電流－電圧特性はＣになった。図６から明らかなように、酸化膜を１．６ｎｍ残したときに得られた特性Ｂは酸化膜のないときの特性Ｃよりも抵抗は低減している。特性Ｃにおいてもオーミック特性が得られているのは抵抗率が２ｍΩｃｍの基板を使用したためである。結果として、酸化膜を介した電極構造とすることでより低い接触抵抗を持ったオーミック特性が得られることがわかった。この実施例では、上部電極４の金属膜をチタンとしたが、チタン以外の金属膜たとえばクロムに対しても同様に本発明の効果を確認した。

【００１３】図７は本発明の電極構造にパワーＭＯＳＦＥＴ（６０Ｖ、４０Ａ級）のドレイン電極に適用したＭＯＳＦＥＴの出力特性図で図中特性Ｂは従来例（酸化膜なし）特性Ａは実施例を示す。従来例のドレイン電極構造の出力特性Ｂのオン抵抗は、１９．０４ｍΩであるのに対して、酸化膜を介したドレイン電極構造の出力特性Ａのオン抵抗は、１６．３１ｍΩとなり、酸化膜を介さない電極構造の出力特性のオン抵抗よりも約１４．３％低下した。なお、ＭＯＳＦＥＴはアンチモン添加した抵抗率が１７ｍΩｃｍ（不純物濃度約10^{18}ｃｍ$^{-3}$）シリコン基板にソー

（６）

ス領域、ドレイン領域、ゲート等の能動領域を形成した後、ウェーハの裏側を削って薄くし、その表面に厚さ１．２ｎｍのシリコン酸化膜をシリコン基板の裏側に形成した。その後、チタンを１００ｎｍの厚さだけ真空蒸着し、さらに引き続きニッケルを５００ｎｍ、銀を１００ｎｍの厚さだけ真空蒸着しドレイン電極とした。

【００１４】

【発明の効果】本発明によれば、０．３～２．２５ｎｍのシリコンサブ酸化膜を金属膜とシリコン基板の間にはさむことにより、良好なオーミック接触電極が得られ、高性能デバイスの開発に極めて有効である。

【図面の簡単な説明】

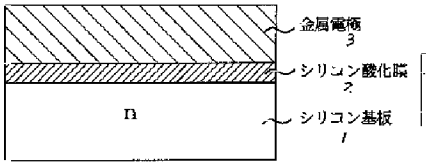
【図１】本発明の実施例を示す断面図

GF Exhibit 1124 - 1641/2704

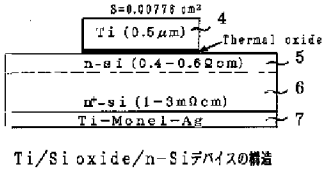
【図２】本発明の有効性を評価するデバイスの構造図
【図３】評価デバイスの電圧－電流特性図
【図４】ＨＦ浸漬時間依存性を示す特性図
【図５】他の評価デバイスの電流－電圧特性図
【図６】評価デバイスの電流－電圧特性図
【図７】本発明をＭＯＳＦＥＴに適用した出力特性図
【符号の説明】

１，６　シリコン基板
２　　シリコンサブ酸化膜
（７）
３　　電極金属
４，７　電極
５　　エピタキシアル層

【図１】

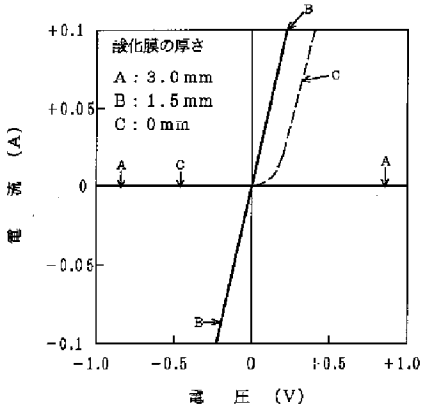


【図２】

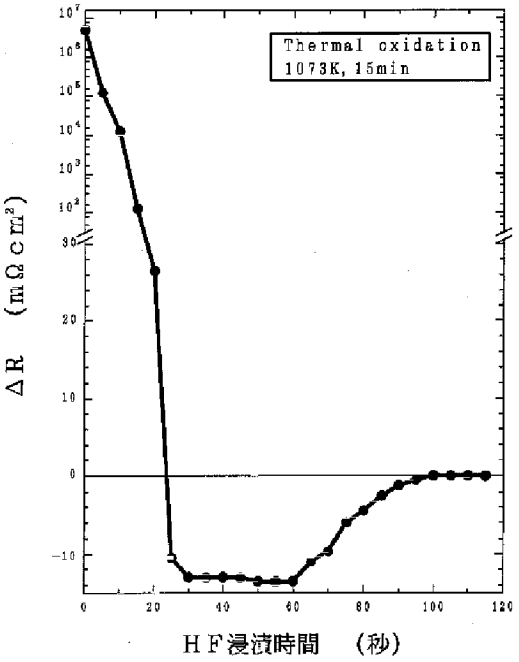


Ti/Si oxide/n-Siデバイスの構造

【図３】

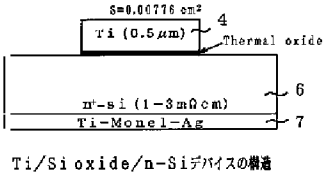


【図４】



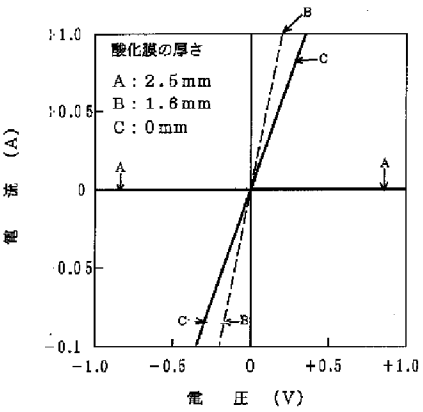
金属／熱酸化膜／ｎ－Ｓｉ構造における
ΔＲの浸漬時間依存性

【図５】



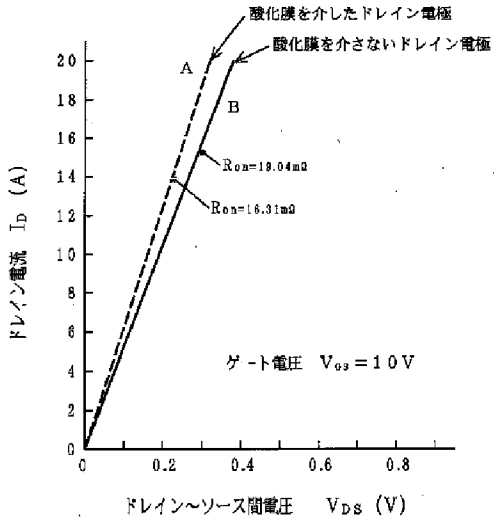
Ti/Si oxide/n-Siデバイスの構造

【図６】



GF Exhibit 1124 - 1642/2704

【図７】



GF Exhibit 1124 - 1643/2704

Europäisches Patentamt
European Patent Office
Office européen des brevets

Espacenet

JPH11162874A OHMIC JOINT ELECTRODE AND SEMICONDUCTOR DEVICE USING THE SAME

Applicants: SHINDENGEN ELECTRIC MFG

Inventors: IWAGURO HIROAKI

Classifications:
IPC ***H01L21/283;*** (IPC1-7): H01L21/283;

Priorities: JP34716297A 1997-12-01

Application: JPH11162874A·1997-12-01

Publication: JPH11162874A·1999-06-18

Published as: JPH11162874A;**JP4067159B2**

OHMIC JOINT ELECTRODE AND SEMICONDUCTOR DEVICE USING THE SAME

Abstract

PROBLEM TO BE SOLVED: To allow ohmic joint which represents a good low contact resistance even when impurity concentration of a silicon substrate is low, by inserting a silicon sub-oxide film of specific film thickness between the silicon substrate and an ohmic joint metal. SOLUTION: A silicon substrate 1 is oxidized by thermal oxidation method or plasma oxidation method to generate a silicon dioxide (SiO2) 2 on the silicon substrate 1. At true interface between the silicon dioxide 1 and the silicon substrate, a sub-silicon oxide film [SiOx (x=0.5, 1.0, 1.5)] is formed instead of the silicon dioxide (SiO2). The thickness of the sub-silicon oxide film is 0.3-2.25 nm from the interface. In short, the silicon oxide film 2 of electrode structure is a sub oxide film [SiOx (x=0.5, 1.0, 1.5)]. So, a metal film and a sub-silicon oxide film are made to contact each other to obtain ohmic joint representing good and low contact resistance.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION JPH11162874

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to an ohmic junction electrode and a semiconductor device using the same.

[0002]

Metal-semiconductor junctions are an important factor in making silicon electronic devices. There are two types of this junction, a Schottky junction that exhibits a rectifying property and an ohmic junction that has no other rectifying property. In order to bring an n-type silicon substrate into contact with a metal to form an ohmic contact electrode exhibiting a good low contact resistance, theoretically, the impurity concentration of the silicon substrate must be 1020 cm-3 or more. Practically, the ohmic junction is made with the impurity concentration of the silicon substrate of 1019 to 1020 cm-3. In order to introduce a large amount of impurities into silicon, methods such as ion implantation, heat treatment, impurity deposition, and thermal diffusion have been used.

[0003]

With the recent increase in the diameter of silicon wafers, the thickness of wafers has increased. In a vertical structure power device, an increase in wafer thickness causes an increase in on-resistance, so in order to suppress this increase in on-resistance, the device on the front surface

GF Exhibit 1124 - 1645/2704

of the wafer is manufactured and then assembled. Then thin the wafer from the back side. After thinning this back side, an ohmic bonding electrode is produced on the back side. However, at this time, the impurity concentration of the silicon substrate is often lower than 10 20 cm −3. Since the device has already been made on the front side and metal wiring such as A1 has been made, high temperature heat treatment is difficult, and impurities are intentionally added to the silicon substrate by ion implantation / heat treatment method or impurity deposition / thermal diffusion method. Cannot be introduced to. It has also been proposed to form an ohmic electrode by providing a thin film containing electric charges on the surface of a semiconductor substrate as shown in JP-A-7-307306.

[0004]

SUMMARY OF THE INVENTION In order to solve the above problems, the present invention provides an ohmic junction exhibiting a good low contact resistance even if the impurity concentration of the silicon substrate is lower than 10 20 cm -3. is there. Usually, when the impurity concentration of the silicon substrate is low, depositing a metal film on the silicon substrate results in Schottky contact between the metal and the silicon substrate. Even in such a case, by interposing the silicon oxide film between the metal and the silicon substrate, an ohmic junction exhibiting a good low contact resistance can be obtained.

[0005]
According to the present invention, a silicon sub oxide film [SiOx (x = 0.5, 1.0, 1.5)] is interposed between a silicon substrate and an ohmic bonding metal. The oxide film has a thickness of 0.3 nm to 2.25 nm.

[0006]

When a silicon substrate is oxidized by a thermal oxidation method or a plasma oxidation method, silicon dioxide (SiO2) is generated on the silicon substrate.

At the interface between the silicon dioxide and the silicon substrate, not the silicon dioxide (SiO2) but the sub-silicon oxide film [SiOx (x = 0.5, 1.0, 1.5)] is formed. The thickness of this sub-silicon oxide film is about 2 nm from the interface. The silicon oxide film of the electrode structure of the present invention is this sub oxide film [SiOx (x = 0.5, 1.0, 1.5)]. By bringing the metal film and the sub-silicon oxide film into contact with each other, an ohmic bond exhibiting

GF Exhibit 1124 - 1646/2704

good and low contact resistance can be obtained. The effect of the present invention is considered to be obtained by the chemical activity of the sub-silicon oxide film, but the detailed reason is not clear. When the silicon dioxide layer and the metal film are brought into contact with each other, the effect is completely lost.

[0007]

FIG. 1 is a sectional view showing an embodiment of the present invention, in which 1 is a silicon substrate, 2 is a silicon sub-oxide film, and 3 is an electrode metal. FIG. 2 shows a device structure for investigating the effectiveness of the oxide film thickness of the present invention. The silicon substrate used is an n + silicon substrate 6 having a resistivity of 2 mΩcm (impurity concentration: 8 × 10 19 cm -3) and a silicon epitaxial layer 5 having a resistivity of 0.5 Ωcm (impurity concentration: 10 16 cm -3) of 5 μm. The grown one was used. This epitaxial surface is mirror-polished, and the surface strain is small.

[0008]

In the manufacturing process for manufacturing the structure of FIG. 2, first, the silicon substrate was washed with dilute hydrofluoric acid for 1 minute and then oxidized at 800 ° C. for 30 minutes using the dry oxidation method. The oxide film thickness is about 3 nm. Next, in order to change the thickness of the oxide film, it was immersed in a dilute hydrofluoric acid (HF: H2O = 1: 100) solution for a certain period of time. It took 100 seconds to completely etch the oxide film having a thickness of 3 nm with this dilute hydrofluoric acid. Further, in order to form the upper electrode 4, a titanium film having a thickness of 500 nm is deposited on the silicon epitaxial layer 5 by a sputtering method, and then a 0.9 mm square is formed by photolithography as shown in FIG. Patterned. Dilute hydrofluoric acid was used for the chemical etching of titanium. The etching time is 2.5 minutes. The photoresist was removed using boiling nitric acid. Finally, 100 nm of titanium, 500 nm of nickel, and 100 nm of silver were vacuum-deposited on the back side of the silicon substrate to form the lower electrode 7. The lower electrode 7 is an ohmic junction electrode.

[0009]

(4) FIG. 3 shows the current-voltage characteristics of the evaluation device (FIG. 2) with respect to each HF immersion time, and shows the results when the electrode 4 is positive (+) and the

GF Exhibit 1124 - 1647/2704

electrode 7 is negative (−) in FIG. It is shown in one quadrant (forward characteristic), and when the polarity is reversed is shown in the third quadrant (reverse characteristic). When not immersed in HF (thickness of oxide film: 3 nm), no current flows in both forward and reverse directions as indicated by characteristic A in the figure. As the HF immersion time is increased, the current starts to flow in both directions, and the ohmic characteristics shown in the characteristic B are obtained when the oxide film has a thickness of 1.5 nm (immersion time is 50 seconds). When the immersion time was further increased and the oxide film disappeared after about 100 seconds, the rectifying characteristic (Schottky characteristic) shown in characteristic C was obtained.

[0010]

FIG. 4 is a characteristic diagram showing the HF immersion time dependency of the value (ΔR) indicating the change in contact resistance from the current-voltage characteristics of FIG. 3, in which the horizontal axis represents the immersion time S (seconds) and the vertical axis represents the change value ΔR (mΩcm 2) Is shown. Note that ΔR was calculated based on the resistance value (FIG. 3C) of the conventional device without the oxide film. The resistance value at this time was obtained from the characteristics of the first quadrant. By this method, the resistance components other than the contact resistance are canceled out, and only the change in the contact resistance is obtained. The minus (negative) value of ΔR means that the contact resistance is smaller than that of the conventional device. As is apparent from FIG. 4, this minus region corresponds to a range of 25 seconds to 90 seconds in the immersion time, that is, a remaining oxide film thickness of 2.25 nm to 0.3 nm.

[0011]

FIG. 5 shows a device structure for investigating whether the contact resistance is improved when the oxidation method is O2 plasma irradiation method and the substrate is 2 mΩcm. As the silicon substrate used, an n + silicon substrate 6 having a resistivity of 2 mΩcm (impurity concentration: 8×10^{19} cm $^{-3}$) was used. In order to manufacture this structure, first, the silicon substrate was washed with dilute hydrofluoric acid for 1 minute, and then oxygen plasma was applied to the silicon with a microwave plasma irradiation device. That is, only the front side of the silicon substrate was irradiated with oxygen plasma for oxidation. The plasma power was 1000 W, the oxygen pressure was 0.5 Torr, and the irradiation time was 2 minutes. At this time, the thickness of the oxide film was 2.5 nm. Next, in order to change the thickness of the oxide film, it is dipped in a dilute hydrofluoric acid (HF: H2O = 1: 100) solution for a certain period of time, and titanium is deposited on silicon to form the upper electrode 4. The film was deposited

GF Exhibit 1124 - 1648/2704

by sputtering to a thickness of 500 nm and then patterned into 0.9 mm square using photolithography technology. Dilute hydrofluoric acid was used for the chemical etching of titanium. The etching time is 2.5 minutes. The photoresist was removed using boiling nitric acid. Finally, 100 nm of titanium, 500 nm of nickel and 100 nm of silver were vacuum-deposited on the back side of the silicon substrate to form the lower electrode 7. The lower electrode 7 is an ohmic junction electrode.

[0012]

FIG. 6 shows the current-voltage characteristics of the device (FIG. 5) with respect to the oxide film thickness. This characteristic is drawn in the first quadrant as compared with the case where the upper electrode 4 is made positive and the lower electrode 7 is made negative in FIG. 5, and the opposite case is drawn in the third quadrant. When not immersed in HF (oxide film thickness: 2.5 nm), current does not flow in both forward and reverse directions (A). When the HF immersion was performed for 30 seconds and the thickness of the oxide film was set to 1.6 nm, the current-voltage characteristic B was obtained. Further, when the immersion time was 90 seconds to completely etch the oxide film, the current-voltage characteristic became C. As is clear from FIG. 6, the characteristic B obtained when the oxide film is left to have a thickness of 1.6 nm is lower in resistance than the characteristic C when the oxide film is not present. In the characteristic C, the ohmic characteristic is obtained because the substrate having the resistivity of 2 mΩcm is used. As a result, it was found that the ohmic characteristics with lower contact resistance can be obtained by using the electrode structure with the oxide film interposed. In this example, the metal film of the upper electrode 4 was titanium, but the effect of the present invention was similarly confirmed for metal films other than titanium, such as chromium.

[0013]

FIG. 7 is an output characteristic diagram of a MOSFET applied to the drain electrode of a power MOSFET (60 V, 40 A class) in the electrode structure of the present invention. In the figure, characteristic B shows a conventional example (no oxide film) and characteristic A shows an example. The on-resistance of the output characteristic B of the drain electrode structure of the conventional example is 19.04 mΩ, while the on-resistance of the output characteristic A of the drain electrode structure through the oxide film is 16.31 mΩ, and the oxide film It was about 14.3% lower than the on resistance of the output characteristics of the electrode structure without the interposition. The MOSFET has an antimony-added resistivity of 17 mΩcm (impurity concentration of about 10 18 cm -3) After forming active regions such as a source region, a drain region, and a gate on a silicon substrate, the back side of the wafer is ground and thinned, A

GF Exhibit 1124 - 1649/2704

silicon oxide film having a thickness of 1.2 nm was formed on the back side of the silicon substrate. Then, titanium was vacuum-deposited to a thickness of 100 nm, and then nickel was vacuum-deposited to a thickness of 500 nm and silver to a thickness of 100 nm to form a drain electrode.

[0014]
According to the present invention, by sandwiching a silicon sub-oxide film of 0.3 to 2.25 nm between a metal film and a silicon substrate, a good ohmic contact electrode can be obtained and a high performance device can be developed. It is extremely effective for

[0015]
Brief description of the drawings

[0016]
1 is a sectional view showing an embodiment of the present invention

[0017]
Fig. 2 Structural diagram of device for evaluating effectiveness of the present invention

[0018]
Figure 3 Voltage-current characteristic diagram of the evaluation device

[0019]
Figure 4 Characteristic diagram showing HF immersion time dependence

[0020]
Figure 5 Current-voltage characteristics of other evaluation devices

[0021]
Figure 6 Current-voltage characteristic diagram of the evaluation device

[0022]

GF Exhibit 1124 - 1650/2704

Fig. 7 Output characteristic diagram in which the present invention is applied to a MOSFET

[0023]

Explanation of symbols

[0024]

1,6 Silicon substrate 2 Silicon sub oxide film (7) 3 Electrode metal 4,7 Electrode 5 Evitaxial layer

GF Exhibit 1124 - 1651/2704

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

CLAIMS JPH11162874

1.
A silicon sub oxide film [SiOx (x = 0.5, 1.0, 1.5)] is interposed between the silicon substrate and the ohmic bonding metal, and the thickness of the oxide film is 0.3 nm to 2. An ohmic contact electrode having a thickness of 25 nm.

2.
The ohmic contact electrode according to claim 1, wherein an n-type silicon substrate is used and the impurity concentration of the substrate is set to 10 16 cm -3 to 10 20 cm -3.

3.
An active region is formed on a silicon substrate, and an electrode metal is bonded to the front surface or the back surface of the silicon substrate through a silicon sub oxide film [SiOx (x = 0.5, 1.0, 1.5)]. Semiconductor device.

GF Exhibit 1124 - 1652/2704

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報**（Ａ）　(11)特許出願公開番号

特開平11－233760

(43)公開日　平成11年(1999)８月27日

(51)Int.Cl.[6]	識別記号	ＦＩ	
Ｈ０１Ｌ　29/78		Ｈ０１Ｌ　29/78	３０１Ｂ
29/16		29/16	
		29/78	３０１Ｃ

審査請求　未請求　請求項の数５　ＯＬ　（全　４　頁）

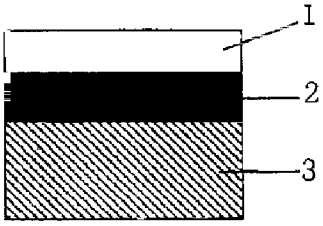
(21)出願番号　特願平10－27979

(22)出願日　平成10年(1998)２月10日

(71)出願人　000004097
日本原子力研究所
東京都千代田区内幸町２丁目２番２号
(72)発明者　吉川　正人
群馬県高崎市綿貫町1233番地　日本原子力研究所高崎研究所内
(72)発明者　梨山　勇
群馬県高崎市綿貫町1233番地　日本原子力研究所高崎研究所内
(74)代理人　弁理士　社本　一夫　（外５名）

(54)【発明の名称】　金属、酸化膜及び炭化珪素半導体からなる積層構造体

(57)【要約】
【課題】　炭化珪素単結晶表面を熱酸化して作製したＭＯＳ構造を持つ素子の熱酸化膜内部に発生する正及び負電荷を低減させてＭＯＳ構造のＣ－Ｖ特性及びＩ－Ｖ特性の横方向シフトを低減させることに関するものである。
【構成】　金属、熱酸化膜及び炭化珪素半導体から構成される積層構造体において、その熱酸化膜を５ｎｍ以下の熱酸化膜で形成したことからなる積層構造体であり、又、その熱酸化膜の上に、更に熱酸化以外の方法で酸化膜を作製することにより２層以上の酸化膜を堆積させた積層構造体であり、更に又、その熱酸化以外の方法で作製した酸化膜が窒化膜である積層構造体である。



GF Exhibit 1124 - 1653/2704

【特許請求の範囲】
【請求項１】　金属、酸化膜及び炭化珪素（ＳｉＣ）半導体からなるＭＯＳ構造を有する積層構造体において、この酸化膜が５ｎｍ以下の熱酸化膜で形成されたことを特徴とする積層構造体。
【請求項２】　熱酸化膜の上に熱酸化以外の方法で酸化膜を堆積させて作製した２層以上の酸化膜を持つ請求項１記載の積層構造体。
【請求項３】　熱酸化膜の上に窒化膜を堆積させて作製した請求項２記載の積層構造体。
【請求項４】　金属、酸化膜及び炭化珪素（ＳｉＣ）半導体からなるＭＯＳ構造を有する積層構造体において、金属が導電性の物質で置き換えられた請求項１に記載の積層構造体。
【請求項５】　導電性の物質が多結晶シリコンである請求項４に記載の積層構造体。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、炭化珪素（ＳｉＣ）単結晶表面を熱酸化して作製したＭＯＳ構造を持つ積層構造体の熱酸化膜内部に発生する正電荷及び負電荷を低減させてＭＯＳ構造におけるＣ－Ｖ（容量－電圧）特性及びＩ－Ｖ（電流－電圧）特性の横方向シフトを低減させることに関するものである。
【０００２】
【従来の技術】従来の炭化珪素におけるＭＯＳ構造は、単に炭化珪素単結晶表面に熱酸化膜を作製し、その表面にＭＯＳ構造を形成しただけのものであるので、これらＭＯＳ構造の酸化膜中には、炭化珪素単結晶と熱酸化膜との界面近傍に負の電荷が存在し、又その界面から４０ｎｍ程度離れた酸化膜中には正の多量の電荷が存在していた。
【０００３】このＭＯＳ構造とは、半導体トランジスタを作製する上で基本となる、金属（Ｍｅｔａｌ）ー酸化膜（Ｏｘｉｄｅ）－半導体（Ｓｅｍｉｃｏｎｄｕｃｔｏｒ）の積層構造を意味している。この積層構造の酸化膜は、正確にはSiO_2から構成されるが、電気的には絶縁体である。即ち、半導体表面の酸化を行うだけで、半導体表面に酸化膜からなる絶縁体が形成されるが、これは工業的利用価値が極めて高いので、現在トランジスタ等を作製するための基本的な技術となっている。そこで、現在、シリコン（Ｓｉ）半導体が使用されるのは、この表面を酸化すると酸化膜の絶縁体が形成されるためである。
【０００４】炭化珪素（ＳｉＣ）半導体も、シリコン（Ｓｉ）半導体と同様に、その表面を酸化するとSiO_2酸化膜が形成される。この炭化珪素（ＳｉＣ）半導体は、シリコン（Ｓｉ）半導体の作製技術と同様な方法によりＭＯＳ構造が作製できるので、半導体素子の集積化等の可能性が他の半導体に比べて高く、現在注目されている。
【０００５】
【発明が解決しようとする課題】炭化珪素単結晶表面を熱酸化し、その表面に熱酸化膜を作製した炭化珪素ＭＯＳ構造を持つ積層構造体は、その作製条件により、ＭＯＳ構造のＣ－Ｖ特性及びＩ－Ｖ特性の横方向シフトの量が異なったり、放射線照射時のＣ－Ｖ特性及びＩ－Ｖ特性の横方向シフトが酸化膜の吸収線量により増減するなどの複雑で不安定な挙動を示した。
【０００６】即ち、ＳｉＣのＭＯＳ構造を作製するためにＳｉＣ表面を酸化すると、その時の酸化法によって、酸化膜の中に電子や正孔（電子の抜けた穴）が形成される。トランジスタを、炭化珪素単結晶のＭＯＳ構造を利用して作製する場合には、この電子や正孔がトランジスタ特性を劣化させるので、大きな問題となっていた。
【０００７】又、Ｃ－Ｖ特性とは、ＭＯＳ構造を形成する酸化膜に電圧（Ｖｏｌｔａｇｅ）を印加したときの、酸化膜内部、又は酸化膜と炭化珪素との界面近傍に蓄積する電子や正孔の量を反映する電気容量（Ｃａｐａｃｉｔａｎｃｅ）の変化を調べる測定のことで、ＭＯＳ構造のＣ－Ｖ特性を調べることにより、トランジスタ特性の劣化の主原因となる電子や正孔の量を評価することができる。したがって、種々の酸化方法で半導体表面を酸化してＭＯＳ構造を形成し、そのＣ－Ｖ特性を測定することにより酸化方法の最適化を行うことが可能になる。
【０００８】更に又、Ｉ－Ｖ特性とは、ＭＯＳ構造を有する半導体素子を図４のように作製したときに、ＭＯＳ構造電極に印加する電圧（Ｖ）に対し、ＭＯＳ構造を挟むようにして配置した電極間に流れる電流（Ｉ）の強さを表す特性のことであり、これは、ＭＯＳ構造の電極に電圧を印加すると、電極直下の酸化膜と炭化珪素半導体界面、あるいは炭化珪素半導体中の抵抗を大きく変化することを利用している。
【０００９】したがって、酸化膜中に図３に示されるような電荷が蓄積しているときには、酸化膜を介して電圧を炭化珪素半導体に印加すると、酸化膜内の電荷の影響により印加電圧（Ｖ）の強さが変化する。これにより、ＭＯＳ構造電極に電圧（Ｖ）を印加したときには、ＭＯＳ構造を挟むようにして配置した電極間に流れる電流（Ｉ）の流れ具合が変化してしまい、本来のＩ－Ｖ特性が得られなくなる。そこで、本発明による５ｎｍ以下の酸化膜を有するＭＯＳ構造を作製すると、酸化膜中の電荷が大きく低減されるので、Ｉ－Ｖ特性の大きな改善がなされることになる。
【００１０】
【課題を解決するための手段】本発明は、炭化珪素単結晶表面に形成された熱酸化膜の厚さを５ｎｍ以下に保つことにより、熱酸化によって酸化膜内部に発生する、炭化珪素と酸化膜との界面から５ｎｍ以上離れ且つ約２０ｎｍ以内までの範囲に分布する負電荷、及び界面から４

GF Exhibit 1124 - 1654/2704

０ｎｍの位置近傍に生ずる正電荷を除去できるので、酸化膜中の電荷量が減少してＭＯＳ構造のＣ－Ｖ特性の挙動を安定させることができるものである。

【００１１】即ち、本発明は、金属、酸化膜及び炭化珪素半導体からなるＭＯＳ構造を有する積層構造体において、この酸化膜が５ｎｍ以下の熱酸化膜で形成された積層構造体であり、又この熱酸化膜の上に熱酸化以外の方法で酸化膜を堆積させて２層以上の酸化膜を持つことができ、更に又熱酸化膜の上に窒化膜を堆積させることもできるものである。

【００１２】本発明において、炭化珪素単結晶半導体表面に酸化膜を形成してＭＯＳ構造を作製した場合には、図１に示されるように、炭化珪素半導体３の上に熱酸化膜２が作製され、その上に金属１が形成される。又図２に示されるように、炭化珪素半導体３の上に熱酸化膜２が作製され、更にその上に熱酸化以外の方法で作製された酸化膜４又は窒化膜４が形成され、更にその上に金属１が形成される。

【００１３】又、炭化珪素単結晶半導体表面に酸化膜を形成してＭＯＳ構造を有する半導体素子を作製した場合には、図４に示されるように、ＭＯＳ構造を挟むような形で半導体に直接触れる金属電極を配置した構造となり、そのＭＯＳ構造部分に電圧を印加すると、挟み込むように配置した電極間の抵抗が減少して電流が流れるようになるので、この素子構造の動作をつかさどる中心部はＭＯＳ構造である。

【００１４】

【発明の実施の形態】本発明のＭＯＳ構造の作製においては、熱酸化膜の厚さが５ｎｍ以下になるように熱酸化する。また、耐電圧が必要なＭＯＳ構造の半導体素子を作製するには、熱酸化により５ｎｍ以下の熱酸化膜を作製後、ＣＶＤ法等の熱酸化以外の方法により、その熱酸化膜の上に酸化膜又は窒化膜などの絶縁膜を堆積成長させて増加した膜厚を得る。

【００１５】本発明の金属、酸化膜及び炭化珪素半導体からなるＭＯＳ構造を有する積層構造体における金属としては、アルミニウム、金、白金、モロブデン等の導電性金属が使用されるが、この金属のに代えて導電性が金属に匹敵する燐を多量に含むポリシリコン（多結晶シリコン）等の導電性物質も使用され得る。

【００１６】熱酸化方法には、１０００－１２００℃の乾燥酸素中でＳｉＣを酸化する方法と同程度の温度の水蒸気中でＳｉＣを酸化する方法とが知られているが、水蒸気による酸化法が電気的に良い酸化膜を得ることができるので、本発明においてもこの方法を使用する。

【００１７】なお、熱酸化方法以外の酸化方法としては、ＳｉＣに対して室温でオゾンを用いてＳｉＣ表面を酸化して酸化膜を作製する方法、Ｓｉ原子を含むガスと酸素を含むガスとを１０００℃程度に加熱したＳｉＣに吹き付けて、その表面にSiO_2膜を化学的に堆積させる化学気相堆積法（Ｃｈｅｍｉｃａｌ　Ｖａｐｏｒ　Ｄｅｐｏｓｉｔｉｏｎ法）等の方法が使用される。

【００１８】図３に、炭化珪素単結晶表面に１００ｎｍの熱酸化膜を作製してＭＯＳ構造を形成したときの熱酸化膜内部の電荷分布を示している。負電荷は、結晶界面から５ｎｍまでの範囲と、５ｎｍから２０ｎｍまでの範囲とに分布する２種類の負電荷からなり、前者が極めて応答時間の長いイオン化した界面準位を示し、後者が熱酸化膜中に捕らえられた負電荷である。また正電荷は４０ｎｍ近傍の位置に局在している。したがって、熱酸化膜を５ｎｍ以下にすることにより、上述の負電荷の一部と正電荷の全て（５ｎｍから２０ｎｍまでの負電荷、及び４０ｎｍ近傍の位置の正電荷）を除去する事ができる。

【００１９】ＳｉＣの酸化膜中には、図３に示すように、通常の酸化方法で酸化膜を作製すると深さ方向に向かって負電荷や正電荷が局在することが知られているが、界面準位とは、酸化膜と炭化珪素（ＳｉＣ）半導体の界面近傍に発生する酸化膜の欠陥のことであり、ＭＯＳ構造に印加される電圧の強さによって酸化膜中の電子や正孔を捕獲したり放出したりするので、この捕獲や放出のタイミングがトランジスタ特性に悪影響を与えるために、通常はこれを無くすことが技術的に重要である。しかし、ＳｉＣの界面準位（ＳｉＣ半導体の界面から５ｎｍの範囲の酸化膜）の場合は、この捕獲又は放出のタイミングが、室温では極めて遅い性質があり、電圧を加えても捕らえた電子をなかなか放出しないので、あたかも捕獲や放出を行わない酸化膜内部に蓄積した負電荷のように行動する。

【００２０】

【実施例】ＳｉＣ半導体の表面処理を行い、その清浄表面を露出させた。次に、酸化炉を立ち上げて酸化炉内を１０００－１２００℃の高温の水蒸気雰囲気（水素燃焼酸化が行われる雰囲気）に保持した。この炉内に表面浄化された半導体を挿入し、その浄化表面に酸化膜を作製した。酸化が終了した段階で得られた半導体を炉外に引き出して室温まで急速に冷却した。その結果、酸化時間を調整することにより５ｎｍの酸化膜を半導体表面に作製できた。

【００２１】次に、必要に応じて、この半導体をＣＶＤ装置の炉内に入れ、その表面に酸化膜又は窒化膜を堆積させた。

【００２２】なお、酸化時間は、ＳｉＣ半導体の面方位と呼ばれている結晶軸の方向や結晶の形態により異なり、比較的よく使用されている６Ｈ－ＳｉＣ（六方晶ＳｉＣ）と呼ばれる単結晶のシリコン面（０００１面）では、１１００℃の温度で、その表面を酸化すると一分間に０．４ｎｍ酸化されるので、５ｎｍの酸化膜を作製するためには、約１３分の酸化時間を要した。

【００２３】

GF Exhibit 1124 - 1655/2704

【発明の効果】本発明の方法によれば、ＳｉＣのＭＯＳ構造体の熱酸化膜中に発生する電荷量を低く押さえることができるため、炭化珪素ＭＯＳ構造のＣ－Ｖ特性及びＩ－Ｖ特性、あるいは炭化珪素ＭＯＳ構造を有する炭化珪素半導体素子などの電気特性を安定させる事ができる。

【図面の簡単な説明】

【図１】　ＭＯＳ構造の基本断面図である。

【図２】　酸化膜とＣＶＤ法で堆積させた２層の酸化膜又は窒化膜を持つＭＯＳ構造の基本断面図である。

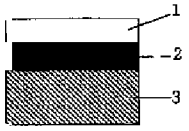
【図３】　炭化珪素単結晶表面に１００ｎｍの熱酸化膜を作製し、その表面にＭＯＳ構造を形成したときの、熱酸化膜内部の電荷分布を示す図である。

【図４】　ＭＯＳ構造及びＭＯＳ構造を有する炭化珪素半導体素子構造を示す図である。

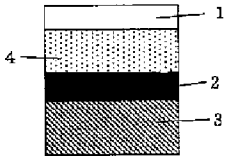
【符号の説明】

１：電極、２：熱酸化膜、３：炭化珪素半導体、４：ＣＶＤ法で堆積させた酸化膜又は窒化膜、５：電極。

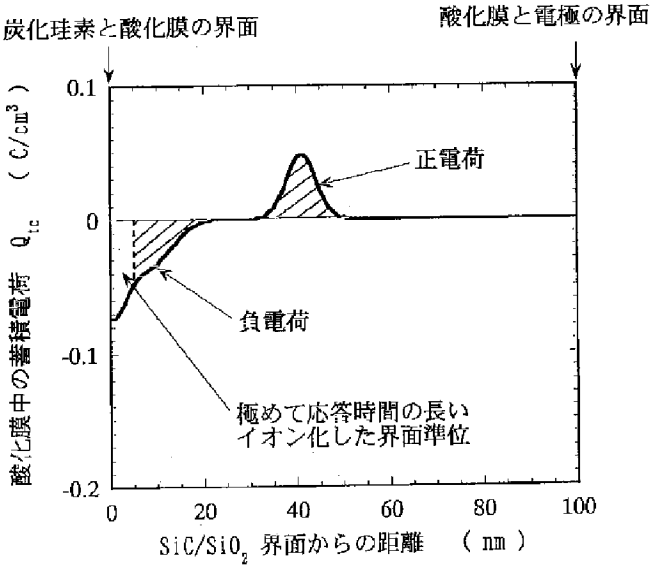
【図１】



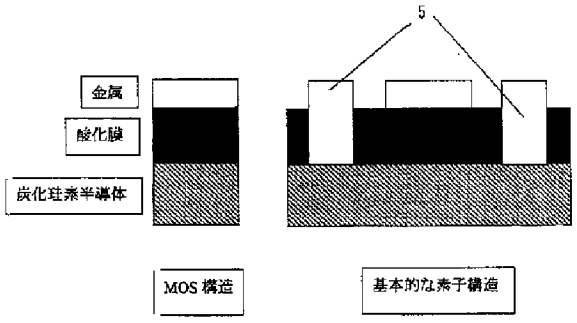
【図２】



【図３】



【図４】



GF Exhibit 1124 - 1656/2704

Europäisches Patentamt
European Patent Office
Office européen des brevets

Espacenet

JPH11233760A LAMINATED STRUCTURE MEMBER COMPOSED OF METAL, OXIDE FILM AND SILICON CARBIDE SEMICONDUCTOR

Applicants: JAPAN ATOMIC ENERGY RES INST

Inventors: NASHIYAMA ISAMU,YOSHIKAWA MASATO

Classifications:
IPC ***H01L29/16; H01L29/78;*** (IPC1-7): H01L29/16; H01L29/78;

Priorities: JP2797998A 1998-02-10

Application: JPH11233760A·1998-02-10

Publication: JPH11233760A·1999-08-27

Published as: JPH11233760A;**JP3855019B2**

LAMINATED STRUCTURE MEMBER COMPOSED OF METAL, OXIDE FILM AND SILICON CARBIDE SEMICONDUCTOR

Abstract

PROBLEM TO BE SOLVED: To reduce lateral direction shift of C-V characteristics and I-V characteristics of an MOS structure, by reducing positive and negative charges generated in a thermal oxidation film of an element having an MOS structure which is formed by thermally oxidizing silicon carbide single crystal surface. SOLUTION: This laminated structure member is constituted of metal 1, a thermal oxidation film 2 and silicon carbide semiconductor 3. The thermal oxidation film 2 is formed of a thermal oxidation film of at most 5 nm in thickness. By forming an oxide film on the thermal oxidation film by using a method except thermal oxidation, a laminated structure member in which at least two layers of oxide films are deposited is obtained. The oxide film formed by a method except the thermal oxidation is a nitride film.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION JPH11233760

[0001]
BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention reduces the positive and negative charges generated inside a thermal oxide film of a laminated structure having a MOS structure, which is produced by thermally oxidizing the surface of a silicon carbide (SiC) single crystal. The present invention relates to reducing a lateral shift of a CV (capacitance-voltage) characteristic and an IV (current-voltage) characteristic in a MOS structure.

[0002]
2. Description of the Related Art In the conventional MOS structure in silicon carbide, a thermal oxide film is simply formed on the surface of a silicon carbide single crystal, and the MOS structure is formed on the surface. , There was a negative charge near the interface between the silicon carbide single crystal and the thermal oxide film, and a large amount of positive charges were present in the oxide film about 40 nm away from the interface.

[0003]

The MOS structure means a laminated structure of metal (Metal) -oxide film (Oxide) -semiconductor (Semiconductor) which is a basis for manufacturing a semiconductor transistor.

To be precise, the oxide film of this laminated structure is composed of SiO2, but is electrically an insulator. That is, an insulator made of an oxide film is formed on the semiconductor surface only

GF Exhibit 1124 - 1658/2704

by oxidizing the semiconductor surface. However, since this has an extremely high industrial utility value, it is currently used as a basic technique for manufacturing a transistor or the like. Has become. Therefore, a silicon (Si) semiconductor is currently used because an oxide film insulator is formed when the surface is oxidized.

[0004]

Similar to a silicon (Si) semiconductor, a silicon carbide (SiC) semiconductor forms a SiO2 oxide film when its surface is oxidized. Since this silicon carbide (SiC) semiconductor has a MOS structure that can be manufactured by a method similar to that of a silicon (Si) semiconductor, the possibility of integration of semiconductor elements is higher than that of other semiconductors, and it is currently receiving attention. ing.

[0005]
A laminated structure having a silicon carbide MOS structure, in which a surface of a silicon carbide single crystal is thermally oxidized and a thermal oxide film is formed on the surface, has a C-V structure of a MOS structure depending on the manufacturing conditions. The amount of lateral shift of the characteristics and IV characteristics is different, and the lateral shift of the CV characteristics and IV characteristics during irradiation increases or decreases depending on the absorbed dose of the oxide film. showed that.

[0006]

That is, when the SiC surface is oxidized to form a SiC MOS structure, electrons and holes (holes from which electrons have been removed) are formed in the oxide film by the oxidation method at that time.

In the case of manufacturing a transistor using a silicon carbide single crystal MOS structure, the electrons and holes deteriorate the transistor characteristics, which is a serious problem.

[0007]

The C-V characteristic is the amount of electrons and holes accumulated inside the oxide film or

GF Exhibit 1124 - 1659/2704

near the interface between the oxide film and silicon carbide when a voltage (Voltage) is applied to the oxide film forming the MOS structure. It is possible to evaluate the amount of electrons and holes, which are the main causes of deterioration of transistor characteristics, by examining the CV characteristic of the MOS structure by measuring the change in the capacitance that reflects the change. .. Therefore, it becomes possible to optimize the oxidation method by oxidizing the semiconductor surface by various oxidation methods to form a MOS structure and measuring the CV characteristics thereof.

[0008]

Furthermore, the IV characteristic means that when a semiconductor device having a MOS structure is manufactured as shown in FIG. 4, a voltage (V) applied to the MOS structure electrodes is applied between electrodes arranged so as to sandwich the MOS structure. This is a characteristic that expresses the strength of a current (I) that flows, and when a voltage is applied to an electrode with a MOS structure, the resistance in the oxide film and silicon carbide semiconductor interface directly under the electrode or in the silicon carbide semiconductor changes greatly. You are taking advantage of what you do.

[0009]

Therefore, when the voltage as shown in FIG. 3 is accumulated in the oxide film and the voltage is applied to the silicon carbide semiconductor through the oxide film, the applied voltage (V) is increased due to the influence of the charges in the oxide film. Changes.

As a result, when a voltage (V) is applied to the MOS structure electrodes, the flow condition of the current (I) flowing between the electrodes arranged so as to sandwich the MOS structure changes, and the original IV characteristic cannot be obtained. .. Therefore, when a MOS structure having an oxide film of 5 nm or less according to the present invention is manufactured, the charge in the oxide film is greatly reduced, and thus the IV characteristic is greatly improved.

[0010]

According to the present invention, by keeping the thickness of a thermal oxide film formed on the surface of a silicon carbide single crystal to be 5 nm or less, silicon carbide and oxides generated inside the oxide film by thermal oxidation can be obtained. Since the negative charges distributed in the range of 5 nm or more from the interface with the film and within about 20 nm and the positive charges generated in the vicinity of the position of 40 nm from the interface can

GF Exhibit 1124 - 1660/2704

be removed, the amount of charges in the oxide film is reduced and The behavior of the C-V characteristic can be stabilized.

[0011]
That is, the present invention is a laminated structure having a MOS structure composed of a metal, an oxide film and a silicon carbide semiconductor, wherein the oxide film is a thermal oxide film of 5 nm or less, and the thermal oxide film is It is possible to deposit an oxide film by a method other than thermal oxidation to have two or more oxide films, and it is also possible to deposit a nitride film on the thermal oxide film.

[0012]

In the present invention, when an oxide film is formed on the surface of a silicon carbide single crystal semiconductor to produce a MOS structure, a thermal oxide film 2 is produced on a silicon carbide semiconductor 3 as shown in FIG. Metal 1 is formed on top.

Further, as shown in FIG. 2, thermal oxide film 2 is formed on silicon carbide semiconductor 3, and further, oxide film 4 or nitride film 4 formed by a method other than thermal oxidation is formed thereon. Metal 1 is formed on top.

[0013]
When an oxide film is formed on the surface of a silicon carbide single crystal semiconductor to manufacture a semiconductor device having a MOS structure, as shown in FIG. 4, a metal electrode that directly contacts the semiconductor with the MOS structure sandwiched therebetween. When a voltage is applied to the MOS structure part, the resistance between the electrodes arranged so as to sandwich it is reduced and a current flows. Therefore, the central part that controls the operation of this element structure is the MOS structure. is there.

[0014]

BEST MODE FOR CARRYING OUT THE INVENTION In manufacturing the MOS structure of the present invention, thermal oxidation is performed so that the thickness of the thermal oxide film is 5 nm or less.

GF Exhibit 1124 - 1661/2704

Further, in order to manufacture a semiconductor device having a MOS structure that requires a withstand voltage, a thermal oxide film having a thickness of 5 nm or less is formed by thermal oxidation, and then oxidation is performed on the thermal oxide film by a method other than thermal oxidation such as a CVD method. An insulating film such as a film or a nitride film is deposited and grown to obtain an increased film thickness.

[0015]

A conductive metal such as aluminum, gold, platinum, or molobden is used as the metal in the laminated structure having the MOS structure including the metal, the oxide film, and the silicon carbide semiconductor according to the present invention. Conductive materials such as polysilicon (polycrystalline silicon) containing a large amount of phosphorus whose properties are comparable to those of metals can also be used.

[0016]

As a thermal oxidation method, a method of oxidizing SiC in dry oxygen at 1000 to 1200 ° C. and a method of oxidizing SiC in steam at a temperature similar to that of steam are known. This method is also used in the present invention because an excellent oxide film can be obtained.

[0017]

As an oxidation method other than the thermal oxidation method, a method of oxidizing the SiC surface by using ozone at room temperature for SiC to form an oxide film, and a gas containing Si atoms and a gas containing oxygen at 1000 ° C. A method such as a chemical vapor deposition method (Chemical Vapor Deposition method) for spraying moderately heated SiC to chemically deposit an SiO2 film on the surface is used.

[0018]

FIG. 3 shows the charge distribution inside the thermal oxide film when a 100 nm thermal oxide film was formed on the surface of a silicon carbide single crystal to form a MOS structure.

Negative charges consist of two types of negative charges distributed in the range from the crystal interface to 5 nm and in the range from 5 nm to 20 nm. The former shows an ionized interface state with a very long response time, and the latter shows thermal oxidation. It is the negative charge trapped in the film.

GF Exhibit 1124 - 1662/2704

The positive charge is localized at a position near 40 nm.

Therefore, by setting the thermal oxide film to 5 nm or less, it is possible to remove a part of the above-mentioned negative charges and all of the positive charges (negative charges from 5 nm to 20 nm, and positive charges in the vicinity of 40 nm).

[0019]

As shown in FIG. 3, it is known that, when an oxide film is formed by an ordinary oxidation method, negative charges and positive charges are localized in the depth direction in the oxide film of SiC. The term "position" refers to a defect in the oxide film that occurs near the interface between the oxide film and the silicon carbide (SiC) semiconductor, and traps electrons and holes in the oxide film depending on the strength of the voltage applied to the MOS structure. It is technically important to eliminate this because the timing of this capture or release adversely affects the transistor characteristics.

However, in the case of the SiC interface state (oxide film in the range of 5 nm from the interface of the SiC semiconductor), the timing of this capture or release is extremely slow at room temperature, and it is difficult to capture the captured electrons even if a voltage is applied. Since it does not release, it behaves as if it were a negative charge accumulated inside the oxide film that does not capture or release.

[0020]

EXAMPLE A surface treatment of a SiC semiconductor was performed to expose its clean surface. Next, the oxidation furnace was started up and the inside of the oxidation furnace was maintained in a high temperature steam atmosphere of 1000 to 1200 ° C (an atmosphere in which hydrogen combustion oxidation is performed). A semiconductor whose surface was purified was inserted into this furnace, and an oxide film was formed on the purified surface. The semiconductor obtained at the stage when the oxidation was completed was taken out of the furnace and rapidly cooled to room temperature. As a result, a 5 nm oxide film could be formed on the semiconductor surface by adjusting the oxidation time.

GF Exhibit 1124 - 1663/2704

[0021]
Next, if necessary, this semiconductor was put in a furnace of a CVD apparatus, and an oxide film or a nitride film was deposited on the surface thereof.

[0022]
Note that the oxidation time varies depending on the direction of the crystal axis, which is called the plane orientation of the SiC semiconductor, and the form of the crystal, and is a relatively frequently used single-crystal silicon surface called 6H—SiC (hexagonal SiC) (0001 plane), when the surface is oxidized at a temperature of 1100 ° C., 0.4 nm is oxidized in 1 minute, so that it takes about 13 minutes to form a 5 nm oxide film.

[0023]
According to the method of the present invention, the amount of charges generated in the thermal oxide film of the SiC MOS structure can be kept low, so that the C-V characteristic and the I-V characteristic of the silicon carbide MOS structure can be suppressed. Alternatively, the electrical characteristics of a silicon carbide semiconductor device having a silicon carbide MOS structure or the like can be stabilized.

GF Exhibit 1124 - 1664/2704

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

CLAIMS JPH11233760

1.
A laminated structure having a MOS structure composed of a metal, an oxide film, and a silicon carbide (SiC) semiconductor, wherein the oxide film is formed of a thermal oxide film of 5 nm or less.

2.
The laminated structure according to claim 1, which has two or more oxide films formed by depositing an oxide film on the thermal oxide film by a method other than thermal oxidation.

3.
The laminated structure according to claim 2, which is manufactured by depositing a nitride film on the thermal oxide film.

4.
The laminated structure according to claim 1, wherein the metal is replaced with a conductive substance in the laminated structure having a MOS structure composed of a metal, an oxide film, and a silicon carbide (SiC) semiconductor.

5.
The laminated structure according to claim 4, wherein the conductive substance is polycrystalline silicon.

GF Exhibit 1124 - 1665/2704

GF Exhibit 1124 - 1666/2704

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号

特開平11－330482

(43)公開日　平成11年(1999)11月30日

(51)Int.Cl.[6]	識別記号	ＦＩ	
Ｈ０１Ｌ　29/786		Ｈ０１Ｌ　29/78	６１７Ｎ
			６１３Ａ

審査請求　未請求　請求項の数６　ＯＬ　（全 26 頁）

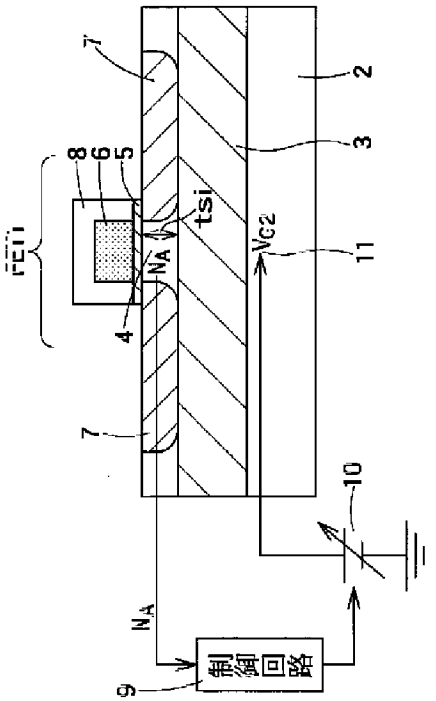
(21)出願番号　特願平10－137236

(22)出願日　平成10年(1998) 5月19日

(71)出願人　000003078
株式会社東芝
神奈川県川崎市幸区堀川町72番地
(72)発明者　沼　田　敏　典
神奈川県川崎市幸区小向東芝町１　株式会社東芝研究開発センター内
(72)発明者　野　口　充　宏
神奈川県横浜市磯子区新杉田町８番地　株式会社東芝横浜事業所内
(74)代理人　弁理士　佐藤　一雄　（外３名）

(54)【発明の名称】　半導体装置

(57)【要約】
【課題】　ＳＯＩ層を用いた完全空乏化ＭＩＳＦＥＴトランジスタを形成してなる半導体装置において、ＭＩＳＥＴのチャネル不純物濃度に依存して、バックゲート電圧を変化させることによって、不純物濃度が変動しても、ＳＯＩ膜厚バラツキに対するしきい値感度をほぼ極小に保ったままで、しきい値を規定する値にできるようにする半導体装置を提供することを目的とする。
【解決手段】　ＳＯＩ層の膜厚を、しきい値変動が小さくなる膜厚に設定する。さらに、ダミー素子を用いてチャネル領域の不純物濃度を測定し、その測定値に基づいてバックゲート電圧を調節することにより所望のしきい値を維持することができる。



GF Exhibit 1124 - 1667/2704

【特許請求の範囲】
【請求項１】バックゲートが形成されてなる支持基板と、
前記支持基板上に設けられた絶縁膜と、
前記絶縁膜上に設けられた第１の半導体層と、
前記支持基板の前記バックゲートに対向して前記第１の半導体層の一部をチャネル領域としたＭＩＳＦＥＴトランジスタと、
前記第１の半導体層の不純物濃度またはキャリア濃度に応じて変化する測定信号を出力するダミー素子と、
前記ダミー素子から出力される前記測定信号に応じて前記バックゲートに電圧を印加する電圧印加手段と、
を備えたことを特徴とする半導体装置。
【請求項２】第１及び第２のバックゲートが形成されてなる支持基板と、
前記支持基板上に設けられた絶縁膜と、
前記絶縁膜上に設けられ第１の膜厚を有する第１の半導体層と、
前記支持基板の前記第１のバックゲートに対向して前記第１の半導体層の一部をチャネル領域とした第１のＭＩＳＦＥＴトランジスタと、
前記絶縁膜上に設けられ前記第１の膜厚とは異なる第２の膜厚を有する第２の半導体層と、
前記支持基板の前記第２のバックゲートに対向して前記第２の半導体層の一部をチャネル領域とした第２のＭＩＳＦＥＴトランジスタと、
前記第１のバックゲートに、前記第２のバックゲートの電圧とは独立に電圧を印加する電圧印加手段と、
を備えたことを特徴とする半導体装置。
【請求項３】バックゲートが形成されてなる支持基板と、
前記支持基板上に設けられた絶縁膜と、
前記絶縁膜上に設けられた第１の半導体層と、
前記支持基板の前記バックゲートに対向して前記第１の半導体層の一部をチャネル領域としたＭＩＳＦＥＴトランジスタと、
前記バックゲートに印加する電圧に対応する情報を記憶する記憶素子と、
前記記憶素子に記憶された前記情報に基づいて前記バックゲートに電圧を印加する電圧印加手段と、
を備えたことを特徴とする半導体装置。
【請求項４】第１及び第２のバックゲートが形成されてなる支持基板と、
前記支持基板上に設けられた絶縁膜と、
前記絶縁膜上に設けられ第１の膜厚を有する第１の半導体層と、
前記支持基板の前記第１のバックゲートに対向して前記第１の半導体層の一部をチャネル領域とした第１のＭＩＳＦＥＴトランジスタと、
前記第１のバックゲートに印加する電圧に対応する情報を記憶する第１の記憶素子と、
前記絶縁膜上に設けられ前記第１の膜厚とは異なる第２の膜厚を有する第２の半導体層と、
前記支持基板の前記第２のバックゲートに対向して前記第２の半導体層の一部をチャネル領域とした第２のＭＩＳＦＥＴトランジスタと、
前記第２のバックゲートの電圧とは独立に、前記第１の記憶素子に記憶された前記情報に基づいて前記第１のバックゲートに電圧を印加する電圧印加手段と、
を備えたことを特徴とする半導体装置。
【請求項５】前記記憶素子は、前記第１の半導体層の不純物濃度またはキャリア濃度に応じた情報を記憶することを特徴とする請求項３または４に記載の半導体装置。
【請求項６】前記ＭＩＳＦＥＴトランジスタは、前記チャネル領域が完全に空乏化した完全空乏型トランジスタであることを特徴とする請求項１～５のいずれか１つに記載の半導体装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、半導体装置に関する。より具体的には、本発明は、支持基板上に絶縁膜を介して設けられた半導体層上に完全空乏化ＭＩＳＦＥＴ（Metal Insulator Semiconductor Field Effect Transistor）を形成してなる半導体装置に関する。
【０００２】
【従来の技術】ＳＯＩ（Silicon on Insulator）すなわち絶縁性の基板上に形成された半導体層を用いて形成されたＦＥＴ型トランジスタは、ソース・ドレイン間の寄生容量を、バルク（bulk）の半導体基板上に形成したＦＥＴより小さくすることができることから、低消費電力デバイスあるいは高速ＣＰＵなどの高速動作回路への応用が期待されている。特に、半導体層であるＳＯＩ膜の厚さをチャネル領域の空乏層の厚さ以下にすると、チャネル領域を完全に空乏化することができる。その結果として、空乏層より厚い半導体層を用いて形成されたＳＯＩトランジスタで問題となるキンク特性や電流オーバーシュート効果などの好ましくない現象を、解消または抑制することができる。
【０００３】このようにチャネル領域を全て空乏化することができるトランジスタ（以下、これを「完全空乏化トランジスタ」と呼ぶ）は、さらに、短チャネル効果の抑制、パンチスルー耐性の向上、サブスレッショルド係数の改善、チャネル移動度の増大などの多岐にわたる利点が得られる。
【０００４】
【発明が解決しようとする課題】しかし、完全空乏化トランジスタには、例えば、プロセス条件のバラツキによって、チャネル領域の半導体層の不純物濃度やＳＯＩ膜厚が変化すると、しきい値が変化してしまうという問題があった。

GF Exhibit 1124 - 1668/2704

【０００５】このようなプロセス条件のバラツキに起因する問題に対処する方法として、従来、例えば、特開平９－３１２４０１号公報において開示されているように、ＳＯＩ層の下の絶縁層の下の支持基板にバックゲートを設け、そのバックゲートに印加する電圧を動作時と待機時とで変化させて、しきい値を制御する例が知られている。

【０００６】しかし、この方法においては、バックゲートの電圧は、ＳＯＩ膜厚のバラツキや基板濃度のバラツキに無関係に決定される。そして、例えばＳＯＩ膜厚バラツキに対するしきい値感度を極小にするバックゲート電圧印加手段やその具体的な構成については何ら開示されていなかった。

【０００７】つまり、従来の完全空乏化トランジスタにおける、しきい値感度を低減する手法および構造では、ＳＯＩ膜厚バラツキに対するしきい値感度を低減するためのバックゲート電圧制御について検討されてきたが、ＳＯＩ膜厚の最適値や、不純物濃度との関係については考慮されていなかった。そのため、しきい値を規定の値に設定し、かつＳＯＩ層の膜厚や不純物濃度のバラツキに対するしきい値感度を小さくすることは困難であった。

【０００８】本発明は、かかる課題の認識に基づいてなされたものである。すなわち、その目的とするところは、ＳＯＩ層を用いた完全空乏化ＭＩＳＦＥＴトランジスタを形成してなる半導体装置において、ＭＩＦＳＥＴのチャネル不純物濃度に依存して、バックゲート電圧を変化させることによって、不純物濃度が変動しても、ＳＯＩ膜厚バラツキに対するしきい値感度をほぼ極小に保ったままで、しきい値を規定する値にできるようにする半導体装置を提供することにある。

【０００９】

【課題を解決するための手段】本発明の骨子は、絶縁膜を介してバックゲートと対向した半導体層に、完全空乏化トランジスタを形成してなる半導体装置において、前記トランジスタのチャネル不純物濃度に応じてバックゲート電圧を制御できる制御回路を設け、不純物濃度に応じたバックゲート電圧をバックゲートに印加することを特徴とする半導体装置を提供することにある。

【００１０】なお、完全空乏化ＳＯＩトランジスタを形成する半導体層は、規定のしきい値で、しきい値変動が小さくなるＳＯＩ膜厚に設定し、さらに、不純物濃度に関しては、半導体層の絶縁膜に接した表面がaccumulationとinversion とで決まる範囲内に、例えば中間に、設定する。ここで、規定のしきい値が異なると、それぞれしきい値変動が抑えられる膜厚が異なる。

【００１１】すなわち、本発明の半導体装置は、バックゲートが形成されてなる支持基板と、前記支持基板上に設けられた絶縁膜と、前記絶縁膜上に設けられた第１の半導体層と、前記支持基板の前記バックゲートに対向して前記第１の半導体層の一部をチャネル領域としたＭＩＳＦＥＴトランジスタと、前記第１の半導体層の不純物濃度またはキャリア濃度に応じて変化する測定信号を出力するダミー素子と、前記ダミー素子から出力される前記測定信号に応じて前記バックゲートに電圧を印加する電圧印加手段と、を備えたことを特徴とする。

【００１２】または、本発明の半導体装置は、第１及び第２のバックゲートが形成されてなる支持基板と、前記支持基板上に設けられた絶縁膜と、前記絶縁膜上に設けられ第１の膜厚を有する第１の半導体層と、前記支持基板の前記第１のバックゲートに対向して前記第１の半導体層の一部をチャネル領域とした第１のＭＩＳＦＥＴトランジスタと、前記絶縁膜上に設けられ前記第１の膜厚とは異なる第２の膜厚を有する第２の半導体層と、前記支持基板の前記第２のバックゲートに対向して前記第２の半導体層の一部をチャネル領域とした第２のＭＩＳＦＥＴトランジスタと、前記第１のバックゲートに、前記第２のバックゲートの電圧とは独立に電圧を印加する電圧印加手段と、を備えたことを特徴とする。

【００１３】または、本発明の半導体装置は、バックゲートが形成されてなる支持基板と、前記支持基板上に設けられた絶縁膜と、前記絶縁膜上に設けられた第１の半導体層と、前記支持基板の前記バックゲートに対向して前記第１の半導体層の一部をチャネル領域としたＭＩＳＦＥＴトランジスタと、前記バックゲートに印加する電圧に対応する情報を記憶する記憶素子と、前記記憶素子に記憶された前記情報に基づいて前記バックゲートに電圧を印加する電圧印加手段と、を備えたことを特徴とする。

【００１４】または、本発明の半導体装置は、第１及び第２のバックゲートが形成されてなる支持基板と、前記支持基板上に設けられた絶縁膜と、前記絶縁膜上に設けられ第１の膜厚を有する第１の半導体層と、前記支持基板の前記第１のバックゲートに対向して前記第１の半導体層の一部をチャネル領域とした第１のＭＩＳＦＥＴトランジスタと、前記第１のバックゲートに印加する電圧に対応する情報を記憶する第１の記憶素子と、前記絶縁膜上に設けられ前記第１の膜厚とは異なる第２の膜厚を有する第２の半導体層と、前記支持基板の前記第２のバックゲートに対向して前記第２の半導体層の一部をチャネル領域とした第２のＭＩＳＦＥＴトランジスタと、前記第２のバックゲートの電圧とは独立に、前記第１の記憶素子に記憶された前記情報に基づいて前記第１のバックゲートに電圧を印加する電圧印加手段と、を備えたことを特徴とする。

【００１５】ここで、前記記憶素子は、前記第１の半導体層の不純物濃度またはキャリア濃度に応じた情報を記憶することを特徴とする。

【００１６】また、前記ＭＩＳＦＥＴトランジスタは、前記チャネル領域が完全に空乏化した完全空乏型トラン

GF Exhibit 1124 - 1669/2704

ジスタであることを特徴とする。

【００１７】また、前記ダミー素子は、前記第１または第２の半導体層の不純物濃度またはキャリア濃度に応じてその抵抗値、容量値、またはインダクタンスの少なくともいずれかが変化するインピーダンス素子であることを特徴とする。

【００１８】また、前記ＭＩＳＦＥＴトランジスタのチャネル領域が形成された前記第１または第２の半導体層の厚さは、４０ｎｍ乃至１００ｎｍの範囲にあり、不純物濃度は3×10^{16}ｃｍ$^{-3}$乃至3×10^{17}ｃｍ$^{-3}$の範囲にあることを特徴とする。

【００１９】また、前記支持基板は、半導体基板で形成され、前記バックゲートの不純物濃度は1×10^{17}ｃｍ$^{-3}$乃至1×10^{20}ｃｍ$^{-3}$の範囲にあることを特徴とする。

【００２０】また、前記ダミー素子により前記不純物濃度または前記キャリア濃度を測定する回路がＭＩＳＦＥＴトランジスタと同一の半導体層上に設けられていることを特徴とする。

【００２１】また、前記第１の半導体層は前記第２の半導体層よりも膜厚が厚く、且つ、前記第１の半導体層は、前記第２の半導体層よりも不純物濃度が低いことを特徴とする。

【００２２】また、前記第１のＭＩＳＦＥＴトランジスタのしきい値は、前記第２のＭＩＳＦＥＴトランジスタのしきい値より小さいことを特徴とする。

【００２３】

【発明の実施の形態】本発明によれば、ＳＯＩ層の膜厚を、しきい値変動が小さくなる膜厚に設定する。さらに、ダミー素子を用いてチャネル領域の不純物濃度を測定し、その測定値に基づいてバックゲート電圧を調節することにより所望のしきい値を維持することができる。よって、完全空乏化トランジスタで問題となるＳＯＩ膜厚や不純物濃度のバラツキに対するしきい値感度をほぼ最小に保ったままで、かつしきい値を所望の値にすることが可能である。

【００２４】以下に図面を参照しつつ本発明の実施の形態について説明する。なお、以下の説明では、ｎ型ＭＯＳＦＥＴを例に挙げて説明する。また、ＳＯＩ層の素子分離のパターン形状については、本発明においては本質的ではないので特に触れない。

【００２５】図１は、本発明の第１の具体例に係わる半導体装置を表す要部断面図である。すなわち、同図において、６はゲート電極、７はソース・ドレイン領域、２は支持基板、３は絶縁膜、４はチャネル領域、５はゲート絶縁膜、８は絶縁膜、９は制御回路、１０は可変電源（例えば出力電流または電圧を制御入力の電圧または電流によって制御する電源）、そして１１はバックゲートを表す。

【００２６】その具体的な構成例について説明すれば、以下の如くである。すなわち、シリコンからなる支持基板２の主面上に、例えば厚さ１０ｎｍ～１μｍのシリコン酸化膜やシリコン窒化膜からなる絶縁膜３が形成され、この絶縁膜３上に膜厚t_{si}、ボロンまたはインジウムなどのｐ型不純物濃度N_Aを有するシリコンなどからなるチャネル領域４が形成されている。膜厚t_{si}は、例えば１ｎｍ～５００ｎｍとし、不純物濃度N_Aは、例えば10^{16}～10^{19}ｃｍ$^{-3}$とすることができる。

【００２７】このチャネル領域４の上に、ゲート絶縁膜５を介して、ゲート電極６が形成されている。ゲート絶縁膜５の材料としては、例えば、シリコン酸化膜、シリコン窒化膜、タンタル酸化膜、チタン酸化膜などを用いることができ、その厚さは１ｎｍ～２００ｎｍとすることができる。ゲート電極６の材料としては、例えば、多結晶シリコン、アルミニウム（Ａｌ）、タングステン（Ｗ）、チタンナイトライド（ＴｉＮ）などを用いることができ、その厚さは１０ｎｍ～１μｍとすることができる。

【００２８】そして、このゲート電極６は、その側壁を例えばシリコン酸化膜、シリコン窒化膜からなる絶縁膜８で覆われて絶縁されている。チャネル領域４の両側には、ｎ型不純物となる砒素（Ａｓ）、リン（Ｐ）、アンチモン（Ｓｂ）などを、例えば10^{18}～10^{21}ｃｍ$^{-3}$添加したソース・ドレイン領域７が形成されている。ここでチャネル領域４は、チャネル領域４と絶縁膜５との界面に反転層が形成された状態で完全に空乏化しており、完全空乏化トランジスタＦＥＴ１を形成している。

【００２９】一方、制御回路９は、後に詳述するように、半導体層、特にチャネル領域４における不純物濃度N_Aを測定する図示しないダミー素子からの電圧、電流、容量または抵抗値の情報を入力して最適なバックゲート電圧値を算出し、それに対応する制御信号を出力する。可変電源１０は、制御回路９から出力された制御信号に基づいて所定のバックゲート電圧をバックゲート１１に印加する。

【００３０】次に、図１に示した半導体装置の製造工程を説明する。ここでは、支持基板２としてシリコン基板、絶縁膜３としてシリコン酸化膜、そしてチャネル領域４やソース・ドレイン領域７としてシリコンからなるＳＯＩ層をそれぞれ用いることとする。このようなＳＯＩ基板の作成方法としては、片面を酸化した２枚のシリコン基板を酸化膜面を密着させ１０００～１２００℃で熱処理して張り合わせる方法を用いることができる。または、シリコン基板に酸素イオンを、加速電圧１６０ｋｅＶドーズ量$1.5\sim3.0\times10^{18}$ａｔｏｍ／ｃｍ^{2}程度の条件でイオン注入し、１３００～１３５０℃で熱処理することにより、埋め込み酸化膜３を形成する方法でもよい。

【００３１】絶縁膜３上の半導体層は、ポリッシングやイオンエッチング、あるいはウェットエッチングにより

GF Exhibit 1124 - 1670/2704

薄膜化し、４０ｎｍ～１μｍの厚さの均一なＳＯＩ膜を形成する。

【００３２】次に、バックゲート１１として、リソグラフィとイオン注入により支持基板２に不純物添加領域を形成する。すなわち、リソグラフィによりＭＩＳＦＥＴトランジスタを形成する領域の絶縁膜３を介して支持基板２へ例えば、燐（Ｐ）またはヒ素（Ａｓ）を、加速電圧５０～７００ｋｅＶ、ドーズ量1×10^{13}～1×10^{16}ａｔｏｍ／ｃｍ^2 程度の条件で注入することにより、バックゲート１１を形成することができる。但し、このようなバックゲート１１の形成工程は、絶縁膜３やＳＯＩ層４の形成よりも前に行うようにしても良い。

【００３３】次に、チャネル領域４の不純物濃度が1×10^{16}ｃｍ$^{-3}$～1×10^{19}ｃｍ$^{-3}$の範囲になるようにイオン注入する。

【００３４】この後、ゲート酸化膜５を形成し、さらにゲート電極６や絶縁膜８を形成することにより、ＭＩＳＦＥＴ１の要部が完成する。

【００３５】以上説明した製造工程においては、特に、完全空乏化ＳＯＩトランジスタでしきい値を－０．１～０．４Ｖの範囲に設定するために、チャネル層４のＳＯＩ膜厚、不純物濃度をそれぞれ４０ｎｍ～１μｍ、3×10^{16}ｃｍ$^{-3}$～3×10^{17}ｃｍ$^{-3}$の範囲とすることが望ましい。

【００３６】次に、本発明の半導体装置におけるチャネル領域４のＳＯＩ膜厚t_{si}、不純物濃度N_A、そしてバックゲート電圧V_{G2}の最適範囲について説明する。

【００３７】図２は、本発明者の計算により得られた完全空乏化ＦＥＴのＳＯＩ層としきい値との関係を表すグラフ図である。ここでは、絶縁体基板３として膜厚８０ｎｍのシリコン酸化膜、バックゲート１１に1×10^{20}ｃｍ$^{-3}$のｐ型Ｓｉ基板、ゲート電極６として1×10^{20}ｃｍ$^{-3}$のｎ型ポリシリコン（多結晶シリコン）、そしてゲート酸化膜５としてシリコン酸化膜３ｎｍからなるｎ型ＭＯＳＦＥＴをモデルとした。そして、バックゲート電圧を０Ｖ、チャネル領域４の不純物濃度1×10^{17}ｃｍ$^{-3}$とした時の、チャネル領域４の膜厚すなわちＳＯＩ膜厚t_{si}としきい値Ｖthの関係を図２において実線で示した。

【００３８】このグラフ図に示した関係の算出にあたっては、完全空乏化トランジスタのしきい値を表す式として文献（“Electrical characterization of Silicon-on-Insulator Materials and Devices ”Sorin Cristlovеanu and Sheng S.Li 著、Kluwer Academic Publishers,（1995））に記載されているものと同様の式を用い、さらに表面量子効果として文献（M.J.van Dort, P.H.Woerlee, A.J.Walker, C.A.H.Juffermans and H.Lifka: IEDM91 p495,（1991））、（J.W.Slotboom and H.C.de Graaff, IEEE trans. Electron Devices, vol.ED-24, No.8,pp.1123-1125,(1977)）、（「デバイス物理のための量子力学」David K.Ferry 著、長岡洋介他訳、丸善、（１９９６））に記載されているものを考慮した。

【００３９】図２からわかるように、トランジスタのしきい値は、チャネル領域４の膜厚t_{si}に対して、極小値（図２中の矢印）を有する。この極小値の付近においては、膜厚t_{si}の変化に対して、しきい値の変化量が最小となる。つまり、ＳＯＩ層の膜厚のバラツキに対する、しきい値感度は極めて小さくなる。

【００４０】また、バックゲート電圧を印加することにより、チャネル領域４のうちの絶縁膜３に接した表面の電子状態が蓄積（図２中の破線$V_{th1,ac2}$）、または反転（図２中の破線$V_{th1,inv2}$）となる範囲内で、しきい値を変えることができる。従って、所定のバックゲート電圧を印加することにより、しきい値を制御して、設定したいしきい値が図２での極小値と一致するようにチャネル領域４の膜厚を形成した完全空乏化トランジスタは、設定した値でＳＯＩ膜厚バラツキに対するしきい値感度をほぼ最小とすることができる。

【００４１】次に、図２に示したようなＳＯＩのしきい値の計算方法について詳細に説明する。以下の説明では、まず、古典論モデルに基づく計算方法について説明し、次にチャネル反転層の表面量子化の効果の補正を加えた計算方法について説明する。

【００４２】まず、バックゲート電圧を印加できる完全空乏化トランジスタにおいては、しきい値は、チャネル領域４の絶縁膜３に接した表面における電子状態に依存する。そして、絶縁膜３に接したチャネル領域４の表面の状態はバックゲート電圧により、蓄積状態から反転状態まで変化させることが可能である。

【００４３】この時のゲート電圧V_{G1}と表面ポテンシャルとの関係は次式で表される。

【００４４】

【数１】

$$V_{G1}=\Phi_{MS1}-\frac{Q_{OX1}}{C_{OX1}}+\left(1+\frac{C_{Si}}{C_{OX1}}\right)\Phi_{S1}-\frac{C_{Si}}{C_{OX1}}\Phi_{S2}-\frac{\frac{1}{2}Q_{depl}+Q_{invl}}{C_{OX1}} \qquad (1)$$

ここで、Φ_{s1}、Φ_{s2}はそれぞれチャネル領域４のゲート絶縁膜５に接した表面、絶縁膜３に接した表面でのフェルミポテンシャル、Φ_{Ms1} はゲート絶縁膜５側のゲート電極６との仕事関数の差、Q_{OX1} はゲート絶縁膜５中の固定電荷密度、C_{OX1} はゲート絶縁膜５のキャパシタンス、Q_{invl}はチャネル領域４におけるチャネルの反転層電荷を表す。また、Q_{depl}はチャネル領域４での空乏層電荷を表し、電子の電荷量ｑ、チャネル領域４の不純物

GF Exhibit 1124 - 1671/2704

濃度N_A、チャネル領域４の膜厚t_{si}を用いて$-qN_At_{si}$で表される。また、フェルミポテンシャルΦpは、シリコンの真性キャリア密度n_i、ボルツマン定数k、温度T、電子の電荷量qを用いて、$\Phi p = (kT/q)\ln(N_A/n_i)$と表され、また、$C_{si}=\varepsilon_{si}/t_{si}$である（$\varepsilon_{si}$はシリコンの誘電率）。

【００４５】完全空乏化トランジスタのしきい値V_{th}は、絶縁膜３に接した側のチャネル領域４の表面の電子状態によって以下のように場合分けして表すことができる。なお、$V_{G1}=V_{th}$となる時の表面ポテンシャルΦ_{si}とチャネルの反転層電荷Q_{inv1}は、ゲート電圧がしきい値である条件からそれぞれ$\Phi_{si}=2\Phi_F$、$Q_{inv1}=0$となる。

【００４６】①back surfaceが蓄積（accumulation）した時は、$\Phi_{s2}=0$より

【００４７】

【数２】

$$V_{th1,acc2}=\Phi_{MS1}-\frac{Q_{OX1}}{C_{OX1}}+\left(1+\frac{C_{Si}}{C_{OX1}}\right)2\Phi_F-\frac{Q_{depl}}{2C_{OX1}} \qquad (2)$$

ここで$V_{th1,acc2}$の添字である「１」と「２」は、チャネル領域４のゲート絶縁膜５と接する表面、絶縁膜３と接する表面での状態をそれぞれ表す。式（２）の場合は、絶縁膜３に接したチャネル領域４の表面が蓄積状態である場合を示している。

【００４８】②back surfaceが反転（inversion）した時は、$\Phi_{s2}=2\Phi_F$より

【００４９】

【数３】

$$V_{th1,inv2}=\Phi_{MS1}-\frac{Q_{OX1}}{C_{OX1}}+2\Phi_F-\frac{Q_{depl}}{2C_{OX1}} \qquad (3)$$

③back surfaceが空乏（depletion）した時は、そのポテンシャルは蓄積時と反転時の中間となり、Φ_{s2}はバックゲート電圧V_{G2}に依存する。この時、絶縁膜３と接したチャネル領域４の表面が蓄積、反転した時のバックゲート電圧V_{G2}をそれぞれ$V_{G2,acc}$、$V_{G2,inv}$とすると、$V_{G2,acc}<V_{G2}<V_{G2,inv}$の条件を満たす。さらに、チャネル領域４の容量$C_{si}$、および絶縁膜３の容量$C_{OX2}$が直列に接続されているから、Φs2は、

【００５０】

【数４】

$$\Phi_{S2}=\frac{C_{OX2}}{(C_{si}+C_{OX2})}(V_{G2}-V_{G2,acc})$$

と表される。よってしきい値は次式で表される。

【００５１】

【数５】

$$V_{th1,depl2}=V_{th1,acc2}-\frac{C_{Si}C_{OX2}}{C_{OX1}(C_{Si}+C_{OX2})}(V_{G2}-V_{G2,acc}) \qquad (4)$$

ここで$V_{G2,acc}$は絶縁膜３について表面と対称であると考えて、$\Phi_{s1}=2\Phi_F$、$\Phi_{s2}=0$の条件から以下のようになる。

【００５２】

【数６】

$$V_{G2,acc}=\Phi_{MS2}-\frac{Q_{OX2}}{C_{OX2}}-\frac{C_{Si}}{C_{OX2}}2\Phi_F-\frac{Q_{depl}}{2C_{OX2}} \qquad (5)$$

図３は、式（２）～（５）により、チャネル領域４の不純物濃度$N_A=1\times10^{17}cm^{-3}$、ＳＯＩ膜厚$t_{si}=60nm$、$\Phi_{Ms1}=-1V$、$Q_{OX1}=Q_{OX2}=0$の場合について計算したバックゲート電圧に対するしきい値の関係を表したグラフである。完全空乏化トランジスタにおいて、チャネル領域４の絶縁膜３に接する表面での電子状態が、反転または蓄積になると、その表面でのポテンシャルΦ_{s2}は一定となる。このため、それ以上のバックゲート電圧を印加してもしきい値はバックゲート電圧に依存せず一定値となる。つまり、完全空乏化トランジスタのしきい値は、チャネル領域４の絶縁膜３に接した表面の電子状態が、蓄積した時のしきい値と反転した時のしきい値の範囲内に限定される。

【００５３】図４は、チャネル領域４の不純物濃度を$1\times10^{17}cm^{-3}$としたときの、式（２）～（５）の古典論モデルを用いて計算したしきい値のチャネル領域４のＳＯＩ膜厚の依存性を示したグラフである。同図においては、$V_{th1,acc2}$を破線、$V_{th1,inv2}$を点線で、そして$V_{G2}=0V$におけるＳＯＩ膜厚に対するしきい値を実線で示している。$V_{th1,acc2}$、$V_{th1,inv2}$はV_{G2}に依存せずチャネル領域４の膜厚により決まる。一方$V_{th1,depl2}$はバックゲート電圧V_{G2}によりしきい値が変化する。図４からわかるように、古典論モデルでの$V_{th1,depl2}$はＳＯＩ膜厚が薄くなるとＳＯＩ空乏層に含まれる空乏層電荷（$-Q_{depl}$）が減少するため線形に減少する。

GF Exhibit 1124 - 1672/2704

【００５４】次に、以上説明した古典論モデルにチャネル反転層の表面量子化補正を加えた場合について説明する。このような表面量子化補正によるしきい値変化は解析的に求めることができる。ここで、表面量子化補正は、表面ポテンシャルの表面バンド曲がりの増加量$\Delta\Psi$

$$\Delta\Psi_S=(E_0-E_C-\Delta E_g)/q+E_S\Delta z \qquad (6)$$

で表される。この式に$2\Phi_F$を加えたものをゲート電圧がしきい値である時の表面ポテンシャルΦ_{s1}とした。

【００５７】図５は、表面量子化補正を説明するためのバンド図である。

【００５８】式（６）は、図５に示したように伝導帯Ｅｃから最低エネルギー準位Ｅｏへのシフト$Eo-Ec$、高濃度のチャネル不純物添加によるバンドギャップの縮小（bandgap narrowing）効果ΔEg、そして量子論に

$$E_0-E_C=\frac{h^2}{2m}\left(\frac{9\pi m q E_S}{4h^2}\right)^{2/3} \qquad (7)$$

ここでＥｓは表面電界を表し、

【００６１】

$$E_S=\left(\frac{\Phi_{S1}-\Phi_{S2}}{t_{Si}}+\frac{qN_A t_{Si}}{2\varepsilon_{Si}}\right) \qquad (8)$$

と表される。

【００６２】また、高濃度のチャネル不純物添加によるbandgap narrowing効果ΔEgは、

$$\Delta E_g/q=\Delta V_{g0}(N_A)=9\left\{\ln\left(\frac{N_A}{10^{17}}\right)+\sqrt{\left[\ln\left(\frac{N_A}{10^{17}}\right)\right]^2+0.5}\right\}\ [mV] \qquad (9)$$

$Es\Delta z$の近似式は、

【００６４】

$$E_S\Delta z\approx max\left((1-(1/3)^{2/3})(E_0-E_C)-\frac{kT}{q},0\right) \qquad (10)$$

と表される。

【００６５】また、有効界面量子効果により、反転層電荷の中心がＳｉ膜とＳｉＯ2膜との界面からΔzだけ離れているから、ゲート酸化膜容量C_{OX1}は、$C_{OX1}=\varepsilon_{OX}/(t_{OX1}+\varepsilon_{Si}/\varepsilon_{OX}\Delta z)$と表される。

【００６６】以上説明したように量子補正を考慮して得られた、チャネル領域４のＳＯＩ膜厚に対するしきい値の依存性が図２である。図２からわかるように、バックゲート電圧を一定とし、チャネル領域４の膜厚を変化させた場合には、しきい値が極小値（図２中の矢印）を取る。そしてさらにチャネル領域４の膜厚が薄くなるとしきい値は増加する。これは、バックゲート電圧が一定の条件でチャネル領域４の膜厚が薄くなるとSiとSiO_2との界面の電界Ｅｓが大きくなるために、量子準位のエネルギーが大きくなり、表面が反転するのにより大きなゲート電圧が必要となるからである。

【００６７】このように、量子補正を考慮した計算を用いることによって、チャネル領域４の膜厚バラツキに対し、しきい値感度が極小となるチャネル領域４の膜厚が存在することが説明される。

【００６８】図６は、図２と同一のＦＥＴのモデルにおいて、図２でしきい値が極小となるチャネル領域４のＳＯＩ膜厚t_{Si}と印加するバックゲート電圧V_{G2}とを、チャネル領域４の不純物濃度N_Aに対して示したグラフである。ここでは、しきい値の設定値がそれぞれ０．１Ｖ、０．２Ｖ、０．３Ｖの場合について示した。

【００６９】図６からわかるように、しきい値が設定した値となり、かつ膜厚バラツキに対するしきい値感度が最小となるＳＯＩ膜厚t_{Si}は、チャネル領域４の不純物濃度N_Aに対する依存性が低いことが、本発明者の詳細な検討により新たに明らかとなった。つまり、ＳＯＩ膜厚t_{Si}の最適値は、不純物濃度N_Aに対してあまり変化せず、ほぼ一定の値をとる。

【００７０】また、設定するしきい値が異なると、ＳＯ

GF Exhibit 1124 - 1673/2704

Ｉ膜厚のバラツキに対するしきい値感度がほぼ最小となるＳＯＩ膜厚t_{Si}は異なることがわかった。ここで、t_{Si}の最適値としきい値V_{th}との関係は、$t_{Si}=250V_{th}^2-275V_{th}+105$（ｎｍ）で、$V_{th}$が０ボルト以上０．５ボルト以下は近似できる。よって、V_{th}が任意の値でも、t_{Si}の最適値を求めることができる。また、しきい値が設定した値となるために必要なバックゲート電圧V_{G2}は、チャネル領域４の不純物濃度N_Aに対して、ほぼ線形に増加することが新たに明らかになった。

【００７１】従って、設定したいしきい値に応じて図６にもとづいて決定したＳＯＩ膜厚t_{Si}、不純物濃度N_Aで作成した場合には、不純物濃度N_Aが例えばプロセスのバラツキ等で所望の値からずれたとしても、チャネル領域４の不純物濃度を測定し、それに応じて、しきい値が設定した大きさとなるのに必要なバックゲート電圧を印加することにより、ＳＯＩ膜厚に対するしきい値感度が最小で、且つ設定したしきい値を有する半導体装置を実現することができる。

【００７２】ここで、膜厚バラツキに対するしきい値感度がほぼ最小となるＳＯＩ膜厚が、チャネル領域４の不純物濃度N_Aに対してほぼ一定となるのは、式（６）の量子力学補正項がt_{Si}に強く依存し、N_Aにはあまり依存しないこと、および、式（５）の空乏層電荷のQ_{depl}が、N_Aが変化してもV_{G2}を変化させることによりほぼ補償することができることによる。

【００７３】この特徴により、もちろん、チャネル領域４の濃度分布が均一でなく所定の不純物プロファイルを有するような場合でも、式（２）で$Q_{depl}/2C_{OX1}$が$2\Phi_F$よりも小さい場合には、上記の不純物濃度N_Aに対してしきい値感度がほぼ一定となる特徴は維持される。

【００７４】また、図７に示したような、ＬＯＣＯＳ犠牲酸化などの方法により形成されたリセス（Recess）ゲート構造を有するＭＩＳＦＥＴの場合には、ＬＯＣＯＳ端部のバーズビークにより、チャネル領域４の膜厚が一定でない場合が多い。すなわち、チャネル領域の膜厚は、ソース・ドレイン寄りで厚く、中央付近で薄くなる。図８は、ＬＯＣＯＳ犠牲酸化法によるリセス型ゲート構造の製造工程を表す概略工程断面図である。例えば、厚さ２０ｎｍ～１μｍのシリコンなどのＳＯＩ層４の上に、厚さが５～１００ｎｍ程度のシリコン酸化膜１４を形成し、その上に例えば膜厚が５０～２００ｎｍのシリコン窒化膜からなる酸化防止膜２０を堆積する。次に、図８（ａ）に示したように、熱酸化法により、ＬＯＣＯＳを形成する。さらに、図８（ｂ）に示したように、酸化防止膜２０をマスクとしてＬＯＣＯＳ酸化膜をイオンエッチングし、ゲート形成領域を形成する。この方法によると、ゲート電極をセルフアラインに形成できるが、ＬＯＣＯＳのバーズビークがゲート形成領域に残るために、チャネル領域のＳＯＩ膜厚が図示したように不均一になりやすい。このようにチャネル領域の膜厚が不均一になると、しきい値の安定性が劣化して問題となる。

【００７５】これに対して、本発明によれば、チャネルの膜厚が均一でない場合にも、例えばチャネルの中央部のＳＯＩ膜厚で、所定のしきい値に対して膜厚ばらつきに対するしきい値感度が最小となるようなＳＯＩ膜厚を設定すれば、所望のしきい値を安定して得ることができる。従って、チャネル領域のＳＯＩ膜厚が、図２または図６に示したような最適膜厚となるように、チャネル中央付近と端部でのＳＯＩ膜厚の不均一性が例えば２０％以内に収まるように、ＬＯＣＯＳ酸化を行うと、所望のしきい値を得ることができる。

【００７６】ここで、チャネル領域４の不純物濃度N_Aの測定箇所は、必ずしもＭＩＳＦＥＴのチャネル領域４そのものである必要はなく、ＭＩＳＦＥＴのチャネル領域と同一の不純物濃度を有する領域であればよい。例えば、複数のＭＩＳＦＥＴを集積した集積素子を製造する際には、その集積素子のいずれかの箇所で測定しても良い。また、ウェーハ上に複数の集積素子を作成する場合に、ウェーハ内での不純物濃度の均一性が良好であれば、ウェーハのいずれかの箇所で測定しても良い。さらに、このようなウェーハを複数枚同時にプロセスする、いわゆる「バッチ処理」の製造プロセスにおいて、バッチ内のウェーハ毎の不純物濃度の変動が小さい場合には、バッチ毎にいずれかのウェーハで測定を行えば良い。

【００７７】このようにして、チャネル領域４の不純物濃度を測定し、設定するしきい値にするためのバックゲート電圧を決定すれば、このしきい値でトランジスタを用いる限りバックゲート電圧を変更する必要はない。つまり、バックゲート電圧が決まった後は、制御回路は必ずしも必要としない。そのため、チャネル領域４の不純物濃度測定を行い、本発明に必要なバックゲート電圧を求めれば、バックゲートに印加する可変電源を必要な電圧を出力するよう設定するだけでよい。

【００７８】ここで、チャネル領域４の不純物濃度の測定には、例えば、文献（“Materials Processing Theory and Practice volume.2-impurity doping processes in silicon”：F.F.Y.Wang著, North Holland Publishing Company(1981)）に紹介されているような測定手法を用いればよい。以下に、不純物濃度測定を含めた構成例を示す。

【００７９】図９は、本発明の半導体装置の第２の具体例を表す概略断面図である。なお、同図においては、図１と同一の部分には、同一符号を付し、その詳しい説明は省略する。

【００８０】図９において、４ａはダミー領域、１２は素子分離領域、１３は高濃度半導体領域、１８は電極領域、そして１９はメタルプラグを示している。ダミー領

GF Exhibit 1124 - 1674/2704

域４ａは、チャネル領域と同一の条件で作成された半導体領域である。高濃度半導体領域１３は、例えば、ｐ型のドーパントが固溶限界までドーピングされた半導体領域である。

【００８１】また、バックゲート１１は、支持基板２内に形成された導電性領域であり、例えば支持基板２をｐ型Ｓｉとし、バックゲート１１をｎ型Ｓｉとすることによって、それぞれ別の電圧が加えられるようにすることが望ましい。また、バックゲート１１は、しきい値を制御するＦＥＴの直下に形成し、不純物濃度を測定するダミー領域４ａの下には形成しない。これは、バックゲート１１に印加する電圧によってダミー領域４ａの空乏層厚さが変化するのを防ぐためである。

【００８２】以下に、チャネル領域４の不純物濃度と膜厚を測定する方法について説明する。図９において、回路９、９ａは制御回路で、回路９ａでは固溶限界で形成された高濃度半導体領域１３の抵抗を測定して、ＳＯＩ膜厚を求め、回路９へ出力する。回路９ではダミー領域４ａの両端の抵抗１８－４ａ－１８を測定し、回路９ａより入力されたＳＯＩ膜厚データを用いてチャネル領域４の不純物濃度を求める。このようにして求めた不純物濃度より、所望のしきい値を得るために必要なバックゲート電圧の値を求め、電源１０へ出力する。

【００８３】図９の構成例では、トランジスタＦＥＴ１のチャネル部分と同じ不純物添加を行ったダミー領域４ａに接するように半導体層と同じ導電性をもつ例えばp^+型の電極領域１８を形成している。そして制御回路９では、電極領域１８と１８との間の抵抗を測定する。ここで、抵抗率ρは、抵抗をＲ、電極領域１８の間隔をＬ、幅をＷ、そしてＳＯＩ膜厚をt_{Si}とすると、$\rho = W t_{Si} R / L$と表される。このようにして、抵抗率ρが得られれば、チャネル領域４の不純物濃度N_Aは、例えば、アービン曲線より求めることができる。

【００８４】一方、ＳＯＩ膜厚t_{Si}については、高濃度半導体領域１３から求めることができる。すなわち、図９に示したように、シリコン中にホウ素（Ｂ）などが固溶限界の濃度までドープされたp^+型の高濃度半導体領域１３において、この半導体領域１３の抵抗を求める。この高濃度半導体領域１３の抵抗から、抵抗率ρを求めることができ、さらに、不純物濃度は固溶度で定まる値となっているので、t_{Si}とN_Aとを分解することができる。よって、高濃度半導体領域１３における抵抗を測定することで半導体層の膜厚を求めることができる。

【００８５】以上の手法により得られたＳＯＩ膜厚t_{Si}を前述の式に代入することでチャネル領域４における不純物濃度N_Aを求めることができる。本構成例では、ＭＩＳＦＥＴ１を形成するのと同じプロセスでN_A測定領域を形成できる。

【００８６】ここで、回路９、回路１０の具体例としては、例えば、ｈａｌｆ－V_{dd}回路や基板バイアス回路などを挙げることができる。図１０は、ｈａｌｆ－V_{dd}回路を用いた実施例を表す概略回路図である。V_{B2}は例えば、０Ｖとなる電圧であり、V_{B1}は例えばV_{DD}となる電圧であり、$V_{B1} > V_{B2}$となっている。図１０の１８－４－１８の抵抗器は図９のダミー領域４ａにおいて形成された抵抗測定装置１８－４－１８であり、Ｒ１はダミー領域４ａが設定した不純物濃度で形成されたときの抵抗値と同じ抵抗値を有する抵抗器である。またトランジスタＱ３、Ｑ４はＱ１、Ｑ２よりも幅広く形成され、電流バッファとなっている。さらにＲ１および１８－４－１８のコンダクタンスはＱ１またはＱ２のトランスコンダクタンスよりも十分小さいとする。不純物濃度が変動したとき、１８－４－１８の抵抗が変化するため、抵抗分割によって、それにより出力される電圧も変化し、１８－４－１８抵抗が大きくなると出力は小さく、また１８－４－１８抵抗が小さくなるとノードＶｏの電圧は大きくなる。この出力ノードＶｏ は電圧と等しくなるように、バックゲート１１に接続されるノードの電圧Ｖ1 が定まる。よって抵抗測定装置の抵抗の変化によりバックゲート電圧を変化することができる。ここで、ＳＯＩ膜厚t_{Si}の変化の影響は、V_{B1}を変化させることによって取り除くことができる。

【００８７】また、図１１（ａ）（ｂ）は、基板バイアス回路による実施例を表す概略回路図である。すなわち、リング・オシレータ中に１８－４－１８抵抗器を設け、ダミー領域４ａの不純物濃度が変化すると、抵抗が変わるためにリング・オシレータの周波数が変化する。この周波数変化によって、チャージポンプ回路の励起回数が変化し、バックゲートへ供給される電流が変化し、バックゲート電圧を変化させることができる。

【００８８】次に、図９の半導体装置の製造工程について説明する。図１２～図１４は、図９の半導体装置の要部製造工程を表す工程断面図である。まず、図１２に示したように、バックゲート１１を形成する。具体的には、ＳＯＩウェーハ上にレジストマスク１５を形成し、チャネル領域４と絶縁膜３を介してシリコンなどの支持基板２にホウ素などの不純物をイオン注入する。このようにして、例えば$1 \times 10^{17} cm^{-3}$から$1 \times 10^{20} cm^{-3}$の不純物濃度からなるｐ型のバックゲート１１を形成することができる。

【００８９】ここで、チャネル領域４、ダミー領域４ａは、図１に関して前述したような方法により形成することができる。なお、ダミー領域４ａチャネル領域４における不純物濃度を測定するための領域である。従って、製造工程においてはチャネル領域４と同時に同じ条件で作成することが望ましい。

【００９０】次に、図１３に示したように素子分離領域１２を形成し、リソグラフィによりゲート長Ｌからなるゲート電極を６、６ａを形成する。さらに、ゲート電極の上に絶縁膜８、８ａを形成する。

GF Exhibit 1124 - 1675/2704

【００９１】次に、図１４に示したように、電極領域を形成する。具体的には、ＭＩＳＦＥＴを形成する領域をレジストマスク１５でマスキングし、例えばホウ素をゲート電極６の両脇にドーズ量10^{13}～10^{16}ｃｍ$^{-2}$でイオン注入することにより、ｐ型の電極領域１８を形成する。

【００９２】この電極領域１８を形成する工程は、ｐ型ＭＩＳＦＥＴのソース・ドレインを形成する時に同時に行うこともできる。つまり、ゲート電極の形成工程の後、例えばホウ素をイオン注入することによりゲート電極がマスクとなりｐ型の電極領域１８とソース・ドレイン領域７とを同時に形成することができる。

【００９３】さらに、電極領域１８を形成した領域とは異なる領域に、例えばホウ素を半導体層の固溶限までイオン注入した高濃度半導体領域１３を形成する（図１４）。この高濃度半導体領域１３は、先の電極領域１８やソース・ドレイン領域７を形成するイオン注入により同時に形成することができる。つまり、ゲートを形成しない領域を設け、ｐ型ＭＩＳＦＥＴのソース・ドレイン領域の形成ためのイオン注入を実施する時、例えばホウ素をシリコンの固溶限の不純物濃度まで注入することにより高濃度半導体領域１３も形成することができる。

【００９４】次に、図９に示したようにバックゲート１１へのコンタクト１９を形成する。具体的には、素子分離領域１２の上から、例えばイオンエッチングによりコンタクトホールを形成し、さらに例えばタングステン（Ｗ）などの電極材料を堆積することにより、メタルコンタクト１９を形成することができる。このメタルコンタクト１９を形成する工程は、図９に示した抵抗測定領域のメタルコンタクトや、ゲート・ソース・ドレイン電極への図示しないコンタクト形成と同時に行うこともできる。これらのコンタクトホール形成する際に、シリコン酸化膜とシリコンのエッチングの選択比の大きいガスを用いてイオンエッチングすることにより、コンタクトホールの深さの異なる領域も同時にエッチングすることができる。次に、ＳＯＩ膜厚t_{Si}を求めるための別の構成例について説明する。

【００９５】図１５は、本発明の半導体装置の第３の具体例を表す概略断面図である。同図の構成においては、ＭＩＳＦＥＴトランジスタ１とは別に、ダミー領域４ｂが形成され、そのダミー領域４ｂの上下にゲート電極６ｂとバックゲート１１ａとが設けられている。そして、これらの電極間のキャパシタンスの容量を測定する。ここでバックゲート１１ａは、バックゲートの表面半導体層に表面空乏化が生じないように充分、例えば10^{18}ｃｍ$^{-3}$以上に不純物添加することが望ましい。また、電極６ｂおよび電極１１ａは、ダミー領域４ｂが完全に空乏化し、その表面に反転層が生じないようにすることが望ましい。

【００９６】このような条件で測定したキャパシタンスC_{total}は、ゲート絶縁膜５、ダミー領域４ｂ、および絶縁膜３のキャパシタンスを直列したものと等しい。従って、ゲート絶縁膜５およびダミー領域４ｂ（すなわちチャネル領域４）の誘電率をそれぞれε_{OX}、ε_{Si}、ゲート絶縁膜５、ダミー領域４ｂ、絶縁膜３の膜厚をそれぞれ、t_{OX}、t_{Si}、t_{box}とすると、キャパシタンスは

【００９７】

【数１２】

$$C_{total}=\frac{1}{\frac{1}{\frac{\varepsilon_{Si}}{t_{Si}}}+\frac{1}{\frac{\varepsilon_{OX}}{t_{OX}}}+\frac{1}{\frac{\varepsilon_{OX}}{t_{box}}}}$$

であらわされる。よって、ゲート絶縁膜５の膜厚t_{OX}と絶縁膜３の膜厚t_{box}が求められ、ゲート絶縁膜５、および絶縁膜３のキャパシタンスが既知であればダミー領域４ｂ（すなわちチャネル領域４）の膜厚$t_{Si}=\varepsilon_{Si}/C_{total}-\varepsilon_{Si}(t_{OX}+t_{box})/\varepsilon_{OX}$を算出することができる。

【００９８】また、後に詳述する図１８に表した半導体装置の図中の左側に形成したダミー素子を用いてt_{Si}を求めることもできる。すなわち、図１８において、ｎ＋層１６とバックゲート１１ｂとの間の容量C_{total}を測定する。ここで、１０ｂの電圧源は、ゲート絶縁膜５ｂとＳＯＩ層４ａとの界面とに反転層が形成されるだけ十分に電圧が印加されているとする。また、バックゲートに十分な電圧を印加することにより、ダミー領域４ａのバックゲート側が空乏化するようにした条件では、測定容量C_{total}は、

【００９９】

【数１３】

$$C_{total}=\frac{\frac{\varepsilon_{Si}}{t_{Si}}\frac{\varepsilon_{OX}}{t_{box}}}{\frac{\varepsilon_{Si}}{t_{Si}}+\frac{\varepsilon_{OX}}{t_{box}}}$$

で表される。よって、t_{box}が既知であればt_{Si}を算出できる。この方法によれば、t_{ox}がばらついても正確にt_{Si}を算出することができる。

【０１００】また、抵抗率を求める方法としては、電圧電流端子を分離した４端子法を用いても良い。この方法の場合には、電極のコンタクト抵抗による誤差を低減できるという利点がある。

【０１０１】次に、図１５に示した半導体装置の製造方法について説明する。図１６、図１７は、図１５の半導体装置の要部製造工程を表す概略工程断面図である。ＭＩＳＦＥＴ、およびキャパシタンス容量を測定する領域の絶縁膜３を介して対抗する例えばシリコンからなる支持基板２の領域に、リソグラフィーと例えばホウ素をイオン注入することにより、例えば1×10^{18}ｃｍ$^{-3}$から1×10^{20}ｃｍ$^{-3}$の不純物濃度からなるｐ型バックゲート１１、１１ａを形成する（図１６）。ここで、チャネ

GF Exhibit 1124 - 1676/2704

ル領域４、ダミー領域４ｂは、図１に関して前述したような製造工程により形成することができる。

【０１０２】次に、図１７に示したように、素子分離領域１２を形成し、さらにゲート絶縁膜５とゲート電極６を形成する。引き続き、図１５に示したように電極領域１８と、ソース・ドレイン領域７を形成する。これらの製造方法は、図９に関して前述したものと同様とすることができる。ここで、図１５の具体例の場合は、ダミー領域４ｂの容量を測定するためにはゲート電極６ｂ下の半導体層が十分空乏化すればよい。従って、電極領域１８およびソース・ドレイン領域７を形成するイオン注入においても、ゲート電極６ｂがマスクの役割を果たすので、この領域をレジストなどでマスキングしなくとも良い。

【０１０３】次に、本発明の半導体装置の第４の具体例について説明する。図１８は、本発明の半導体装置の第４の具体例を表す概略断面図である。すなわち、同図に表した半導体装置においては、ＭＩＳＦＥＴ１とは別に設けられたＭＩＳキャパシタのダミー素子を用いてＣ－Ｖ測定法により不純物濃度を求めることができる。ＦＥＴ１と素子分離領域１２を介して隣接するダミー領域４ａの上に絶縁膜を５ｂが積層され、さらにＭＩＳキャパシタ電極として例えばp^+型ポリシリコン（多結晶シリコン）６ｂが積層されている。

【０１０４】また、このＭＩＳキャパシタの下部に作成したバックゲート１１にＭＩＳＦＥＴトランジスタに使う電圧源とは別の電圧源V_{G2}ｂを設ける。この電圧源V_{G2}ｂはダミー領域４ａの絶縁膜３に接する表面の電子状態が蓄積するだけの電圧が印加される固定電源でよい。

【０１０５】このようなＭＩＳキャパシタを用いてＣ－Ｖ法により半導体の不純物濃度を求め、本発明を実現するのに必要なバックゲート電圧を決定することができる。キャパシタンス測定は、ダミー領域４ａが完全に空乏化しない程度で固定のゲート電圧を印加し、そして、ゲート近傍に設けたn^+型、p^+型の半導体領域の電極を用いてキャパシタンス測定を行う。

【０１０６】この時の容量は、不純物濃度をN_Aとすると$(N_A)^{1/2}$に比例するため、容量からN_Aを求めることができる。

【０１０７】図１９は、回路９ｃ、１０ｂの具体例を表す概略回路図である。同図に表した回路は、例えば、図１１の回路と似ており、リング・オシレータにダミー素子のＭＩＳキャパシタによるキャパシタンスＣが組み込まれている。ダミー領域４ａの不純物濃度が変動するとキャパシタンスＣが変化し、リング・オシレータの周波数が変化する。この周波数の変化によって、バックゲート電圧を変化することができる。

【０１０８】次に、図１８の半導体装置の製造方法について説明する。図２０、図２１は、図１８の半導体装置の要部製造工程を表す概略工程断面図である。まず、図２０に示したように、ＭＩＳＦＥＴトランジスタを形成する領域に、例えば隣接する領域に、ＭＩＳＦＥＴトランジスタとは別のバックゲート１１ｂを形成する。次に、ゲート工程と同じ工程で、例えば、シリコン酸化膜からなるゲート絶縁膜５ｂおよび、ｎ型ポリシリコンからなるゲート電極６ｂを作成し、これがＭＩＳキャパシタを形成する。これは、ＭＩＳＦＥＴ１のゲート形成工程と同時に形成しても良い（図２０）。

【０１０９】次に、ＭＩＳキャパシタのゲート電極近傍にn^+型とp^+型の半導体領域を形成する。具体的には、ｎ型ＭＩＳＦＥＴ、ｐ型ＭＩＳＦＥＴのソース・ドレイン領域７の形成のためのイオン注入に際して、ＭＩＳキャパシタ領域にはそれぞれ片側ずつイオン注入すればよい（図２１）。

【０１１０】Ｃ－Ｖ法を用いた不純物濃度測定としては、ｐｎ接合により求める手法もある。図２２は、ｐｎ接合により不純物濃度を測定するためのダミー素子を設けた半導体装置を例示する概略断面図である。すなわち、ＦＥＴ１と素子分離領域１２を介して隣接するダミー領域４ａの表面層に、n^+型シリコン領域１４を形成する。このようにして形成したｐｎ接合を用いて、Ｃ－Ｖ法により不純物濃度を測定し、本発明を実現するのに必要なバックゲート電圧を決定することができる。ここで、ダミー領域４ａに絶縁膜３を介して対向するバックゲート１１ｃには、十分大きな負の電圧V_{G2a}を印加して、絶縁膜３に接した表面の電子状態を蓄積状態にする。

【０１１１】図２３は、図２２のダミー素子を含めた回路９ｄ、１０ｂの具体例を表す概略回路図である。図２３の回路における容量Ｃは図２２の電極６ｂで測定される容量である。図２２に示したようなダミー領域のｐｎ接合ダイオードのダイオードキャパシタンスは不純物濃度の変動によって変化する。このように容量Ｃが変化するとリング・オシレータの周波数が変化し、バックゲート電圧V_{G2}にフィードバックすることができる。ここで、容量Ｃが小さい場合にはポンプ周波数が上昇してV_{G2}が上昇する。もちろん、ｐｎ接合ではなく、例えばショットキー接合を用いていもよい。

【０１１２】次に、本発明の第５の具体例について説明する。図２４は、本発明の第５の具体例に係わる半導体装置の概略断面図である。本実施形態においては、同一基板上に、２つ以上の異なるしきい値を有する完全空乏化トランジスタを設け、それぞれのトランジスタのしきい値が、膜厚バラツキに対してしきい値感度が最小で、かつ設定したしきい値となるようにする。

【０１１３】なお、図２４に示した具体例では、説明の便宜上、チャネル領域４の膜厚や不純物濃度が異なる２つの完全空乏化トランジスタが並列している場合を示したが、絶縁体基板３上に形成されていればよく、必ずしも、同図に示した方向に隣接する必要はない。また、図

GF Exhibit 1124 - 1677/2704

２４において、図１と同一部分には、同一符号を付して、その詳しい説明は省略する。

【０１１４】本実施例は、同一基板上に少なくとも２つの異なるしきい値を有する完全空乏化トランジスタ１Ａ、１Ｂを備えている。具体的に説明すると、例えばシリコンからなる支持基板２上のシリコン酸化膜などの絶縁膜３の上に、２０ｎｍ～０．１μｍ程度の膜厚のＳＯＩ層、例えば、膜厚が８０ｎｍのチャネル領域４Ａと、６０ｎｍのチャネル領域４Ｂとが形成されている。それぞれの不純物濃度は、$1\times10^{16}cm^{-3}$～$1\times10^{19}cm^{-3}$程度の範囲にあり、例えば、それぞれ$1\times10^{17}cm^{-3}$と、$1.6\times10^{17}cm^{-3}$という異なる不純物濃度N_{AA}、N_{AB}を有する。ＭＩＳＦＥＴ１Ａ、１Ｂを形成するＳＯＩ層と絶縁膜３を介して対向する支持基板２には、それぞれのＭＩＳＦＥＴに異なる電位を与えられるバックゲート１１Ａ、１１Ｂが形成されている。また、チャネル領域４Ａ、４Ｂのそれぞれの不純物濃度に応じたバックゲート電圧を設定する制御回路９Ａ、９Ｂが設けられ、電極１１Ａ、１１Ｂに印加する可変電源１０Ａ、１０Ｂが設けられている。

【０１１５】ここで、図２に関して前述したモデルを用いて説明すると、図６に例示したように、ＳＯＩ膜厚のバラツキに対するしきい値感度がほぼ最小で、かつしきい値が設定した値になるチャネル領域４の最適領域すなわち設計値は、しきい値により一義的に決まる。つまり、設定するしきい値が異なると、しきい値のＳＯＩ膜厚バラツキ感度を最小とするための半導体層の最適膜厚は異なる。

【０１１６】図６に示した計算結果を用いると、同一基板上にしきい値が０．１Ｖと０．２Ｖの２つのしきい値変動が極小となる完全空乏化トランジスタを形成する時、チャネル領域４は例えば、それぞれ膜厚８０ｎｍ、６０ｎｍ、不純物濃度$1.0\times10^{17}cm^{-3}$、$1.6\times10^{17}cm^{-3}$で形成する必要があり、膜厚および不純物濃度を２つトランジスタで同じ値にすることはできない。すなわち、それぞれのトランジスタのＳＯＩ膜厚や不純物濃度を別々の値に設定することによって、ＳＯＩ膜厚のばらつきなどに対してしきい値が変動しにくいトランジスタを実現することができる。従来のようにＳＯＩ膜厚が同一では、それぞれのトランジスタのしきい値感度を低減することは困難である。

【０１１７】ＦＥＴ１Ａの設定しきい値がＦＥＴ１Ｂの設定しきい値よりも小さい場合には、それぞれのしきい値感度を極小にするために、同一基板上において、ＦＥＴ１ＡのＳＯＩ膜厚（t_{siA}）が厚く不純物濃度（N_{AA}）が低くチャネル領域４Ａと、ＳＯＩ膜厚（t_{siB}）が薄く不純物濃度（N_{AB}）が大きいチャネル領域４Ｂとを形成することが望ましい。

【０１１８】また、このようにチャネル領域の厚さや不純物濃度が異なる複数の領域に対応して、それぞれの領域に独立に電位を設定することができるバックゲート電極および図示しないダミー素子を設けることが望ましい。すなわち、これらのダミー素子を用いてそれぞれのチャネル領域の不純物濃度や層厚を測定し、その測定結果をフィードバックして、それぞれのＦＥＴに所定のバックゲート電圧を印加することにより、それぞれのＦＥＴのしきい値を所望の値に調節することができる。このためのダミー素子は、例えば、図９、図１５、図１８、或いは図２２などに例示したものを用いることができる。さらに、測定のための回路やバックゲート電圧の印加回路も、本願明細書において例示した種々のものを用いることができる。

【０１１９】さらに、ｎ型ＭＩＳＦＥＴとｐ型ＭＩＳＦＥＴを同一基板上に形成する場合にも、本実施例を用いることができる。つまり、図２４に示したＦＥＴ１Ａとして、例えば、ｎ型ＭＩＳＦＥＴを用い、ＦＥＴ１Ｂとして、例えばｐ型ＭＩＳＦＥＴを用いればよい。通常、ゲート電極と基板との仕事関数の差やゲート絶縁膜界面の電荷は、ｎ型ＭＩＳＦＥＴとｐ型ＭＩＳＦＥＴで異なるため、そのフラットバンド電圧の絶対値$|V_{FB}|$も異なる。このため、たとえ同じしきい値を設定しても、ｎ型ＭＩＳＦＥＴとｐ型ＭＩＳＦＥＴのそれぞれに対し、ＳＯＩ膜厚変動に対するしきい値感度を最小にするためのＳＯＩ膜厚も異なる。すなわち、図２４に例示したように、それぞれのトランジスタＦＥＴ１ＡおよびＦＥＴ１Ｂで最適なＳＯＩ膜厚を用いることで、しきい値感度を小さく保つことができる。

【０１２０】次に、図２４の半導体装置の製造方法について説明する。図２５は、図２４の半導体装置の要部製造工程を表す概略工程断面図である。本構造の形成に際しては、図２５（ａ）に示したように、ＳＯＩ基板に対して、リソグラフィとイオン注入によって、バックゲート１１Ａ、１１Ｂを、それぞれのＭＩＳＦＥＴに対し別の電位を与えられるように形成する。絶縁膜３の上のＳＯＩ層をポリッシングやドライエッチング、あるいはウエットエッチングにより薄膜化し、例えば８０ｎｍの膜厚で、またホウ素（Ｂ）などをイオン注入することにより、例えば$1\times10^{17}cm^{-3}$の不純物濃度のＳＯＩ層４を形成する。次に、レジストマスク１５を形成して、エッチングすることにより、例えば、６０ｎｍの膜厚からなるチャネル領域４Ｂを形成する。引き続き、チャネル領域４Ｂに、例えばホウ素（Ｂ）をイオン注入して、この領域の不純物濃度N_{AB}を例えば、$1.6\times10^{17}cm^{-3}$とする。

【０１２１】そして、図示しないゲート工程以降の工程を行うことにより、同一の基板上に完全空乏化トランジスタＦＥＴ１Ａ、ＦＥＴ１Ｂを形成することができる。また、それぞれのチャネル領域に対応して、図示しないダミー素子を適宜形成する。さらに、ＭＩＳＦＥＴを形成するＳＯＩ層の不純物濃度に応じてバックゲート電圧

GF Exhibit 1124 - 1678/2704

を制御する回路９Ａ、９Ｂを設け、各々バックゲート１１Ａ、１１Ｂに印加する可変電源１０Ａ、１０Ｂなどを設置して半導体装置が完成する。

【０１２２】次に、本発明の第６の具体例について説明する。

【０１２３】図２６は、本発明の第６の具体例に係わる半導体装置の概略断面図である。本具体例においては、薄いＳＯＩ層にＦＥＴ１を形成し、厚いＳＯＩ層に不純物濃度を測定するためのダミー素子を形成することを特徴とする。

【０１２４】このダミー素子はｐｎ接合を有し、Ｃ－Ｖ法を用いて不純物濃度を測定できるものであり、その構造及び測定の方法の詳細は、図２２に関して前述したものと同様とすることができる。膜厚の薄いＳＯＩ層にｐｎ接合を形成する際には、その接合位置の制御は容易でなく、イオン注入するりん（Ｐ）や砒素（Ａｓ）の突き抜けなどによってｐ型層が失われるおそれがあり、また、ｐ型層の空乏層がバックゲート領域まで延びN_Aを測定できなくなるおそれがある。これに対して、本具体例によれば、ＳＯＩ層の膜厚を厚くした領域でｐｎ接合を形成することができるので、その形成がはるかに容易となり、ｐ型層の領域が確保できるなどの利点がある。

【０１２５】その製造工程について概説すると以下の如くである。まず、例えば膜厚が８０ｎｍで不純物濃度が$1\times10^{17}cm^{-3}$のｐ型シリコン層からなるＳＯＩ層を形成する。次に、パターニングとエッチングにより、トランジスタを形成する部分のＳＯＩ層の膜厚を例えば６０ｎｍとする。次に、これらのＳＯＩ層の不純物濃度が例えば、$1.6\times10^{17}cm^{-3}$となるようにホウ素（Ｂ）などをイオン注入する。さらに、ＭＩＳＦＥＴを形成する領域に、ゲート工程以降の工程を行う。

【０１２６】次に、図２７に示したように、ダミー素子を形成する領域に例えばリン（Ｐ）をイオン注入することによりｐｎ接合を形成する。このイオン注入工程は、ｎ型ＭＩＳＦＥＴのソース・ドレイン領域７の形成工程と兼ねることも可能である。ここで、図２４や図２６に例示したように膜厚が異なるＳＯＩ領域を方法としは、ＬＯＣＯＳ（Local Oxidation of Silicon）犠牲酸化によることもできる。図２８は、ＬＯＣＯＳ犠牲酸化によるリセス（Recess）構造を用いることにより膜厚の薄いＳＯＩ領域を形成する技術を説明する工程断面図である。この方法においては、まず、ＳＯＩ層４ａの上にシリコン酸化膜１４を形成し、その全面に例えば、シリコン窒化膜からなる膜２０を堆積する。そして、図２８（ａ）に示したように、薄膜化したいチャネル領域においてシリコン窒化膜２０を開口する。そして、開口した領域のＳＯＩ層にイオン注入し、熱処理を施すことにより所定の不純物濃度とする。

【０１２７】次に、図２８（ｂ）に示したように、開口した領域のＳＯＩ層の膜厚が所定の厚さに低下するまで、表面層を熱酸化する。そして、シリコン窒化膜２０、シリコン酸化膜１４を剥離することにより、膜厚が薄く、所定の不純物濃度を有するＳＯＩ領域を形成することができる。この後は、図示しないゲート形成工程以降の工程を実施することにより、半導体装置を完成することができる。

【０１２８】ここでは、ＳＯＩ層のチャネル部の薄膜化についてＬＯＣＯＳ犠牲酸化によるリセス構造について説明した。しかし、この他にも、図２９に示すように、チャネル領域のＳＯＩ層をリソグラフィとエッチングにより薄膜化するコーンケーブ（concave）構造により形成してもよい。

【０１２９】次に、本発明の第７の具体例について説明する。前述した各具体例では、所望のしきい値を有し且つプロセスのばらつきによるしきい値の変動を低減するために、完全空乏化トランジスタを形成する基板と同一基板上に、不純物濃度またはキャリア濃度を測定する測定用ダミー素子と、測定用ダミー素子により測定した不純物濃度またはキャリア濃度に応じてバックゲート電圧を設定する制御回路を設ける技術について説明した。これに対して、本具体例では、あらかじめ測定用ダミー素子で不純物濃度またはキャリア濃度を測定し、その値を記憶させた記憶素子を設けた半導体装置を実現する。

【０１３０】図３０は、本具体例に係わる半導体装置の要部断面図である。また、図３１は、本具体例における各構成要素の関連を説明する機能ブロック図である。同図においては、前述した各具体例と同一部分には同一記号を付して、その詳細な説明は省略する。本具体例においても、所望のしきい値に対し、しきい値感度が低減されるように設定されたＳＯＩ膜厚と、不純物濃度またはキャリア濃度（例えば、図６）を有するチャネル領域４とバックゲート１１からなる完全空乏化トランジスタＦＥＴ１が設けられている。さらに、本具体例においては、バックゲート１１に印加するバックゲート電圧を設定するための、不純物濃度またはキャリア濃度の情報を記憶する記憶素子を有する。この記憶素子は、例えば、ポリシリコンやアモルファスシリコンやアルミニウム（Ａｌ）や銅（Ｃｕ）、あるいは白金シリサイド（ＰｔＳｉ）やチタンシリサイド（ＴｉＳｉ）などからなる配線層で形成されたヒューズＦ１、Ｆ２、Ｆ３を有することを特徴とする。

【０１３１】図３２～３４は、図３０の半導体装置の製造工程を説明するための断面図である。すなわち、本具体例においても、図３２に示したように、製造工程の途中では測定用ダミー素子を設ける。このダミー素子は、図９に示したように、ＳＯＩ層の抵抗率ρから不純物濃度またはキャリア濃度を測定するものである。

【０１３２】次に、図３３に示したように、測定用ダミー素子を用いて、チャネル領域４の不純物濃度またはキャリア濃度を測定する。そして、この測定値に基づい

GF Exhibit 1124 - 1679/2704

て、所望のしきい値に要するバックゲート電圧を決定し、記憶素子に記憶する。すなわち、ヒューズを切断して、必要なバックゲート電圧を作成する。ここで、測定用ダミー素子はＦＥＴ１のそれぞれについて形成されている必要は必ずしもない。例えば、共通するしきい値を有する複数のＦＥＴについて１つの測定用ダミー素子を形成することにより、素子面積を減らすことができる。さらに具体的には、複数のＦＥＴが形成された集積回路を有する半導体装置について１つの測定用ダミー素子を設けても良く、または、このような半導体装置が複数個形成されるウェーハについて１つの測定用ダミー素子を設けても良い。さらに、これらのウェーハが複数枚バッチ処理される場合に、ウェーハ間のばらつきが小さければ、いずれかのウェーハのみに測定用ダミー素子を設けても良い。

【０１３３】一旦、チャネル領域４の不純物濃度またはキャリア濃度が測定され、図６に示したような関係に基づいて必要なバックゲート電圧が決定されると、測定用ダミー素子は不要となる。そこで、図３４に示すように、チップ化するための例えば、ダイシング工程において、ＦＥＴ１と測定用ダミー素子とを分離することができる。

【０１３４】本具体例によれば、不純物濃度またはキャリア濃度を測定するための回路を最終的に得られるチップ上に形成する必要がなく、はるかに小さなサイズの記憶素子に記憶させればよい。よって、高集積化およびチップ面積の縮小を図ることができる。また、不純物濃度またはキャリア濃度測定回路が不要となるために、より低消費電力化を図ることもできる。

【０１３５】ここで、チャネル領域の不純物濃度またはキャリア濃度の測定は、図３２に示した測定用ダミー素子に限らず、前述した各具体例にて説明したいずれの手法も同様に用いることができる。

【０１３６】また、本具体例は、図２４に例示したような複数の異なるＦＥＴが形成されてなる半導体装置についても適用することができる。すなわち、チャネル領域の層厚や不純物濃度などが異なる複数の種類のＭＩＳＦＥＴが形成されている場合に、それぞれの種類のＦＥＴ毎に記憶素子を設けることにより、ダミー素子の測定結果をフィードバックして最適なバックゲート電圧を印加することができる。

【０１３７】次に、本具体例で使用するバイアス回路の具体的な構成を例示する。

【０１３８】図３５～図４０は、本具体例で用いることができる記憶素子を含んだバイアス回路の構成例を表す。

【０１３９】図３５は、チャネル領域４の不純物濃度またはキャリア濃度のばらつく範囲をあらかじめ予測し、それぞれの予測値に対応した最適なバックゲート電圧を、例えばV_{G1}、V_{G2}、V_{G3}、と設けておいて、必要に応じて記憶素子のヒューズを切断する例である。

【０１４０】図６のＳＯＩ膜厚と不純物濃度との関係のグラフを用いて具体的に説明する。まず、所望のしきい値を０．２Ｖとし、不純物濃度が例えば、１．２×10^{17}ｃｍ$^{-3}$～１．８×10^{17}ｃｍ$^{-3}$までの範囲内でばらつくとする。この時、バックゲート電圧の供給電源として例えば、V_{G1}、V_{G2}、V_{G3}として－１、０、１Ｖを設けておく。次に、ダミー素子を用いてチャネル領域４の不純物濃度の測定を行い、その測定値が１．２×10^{17}ｃｍ$^{-3}$～１．４×10^{17}ｃｍ$^{-3}$の時は、記憶素子のＦ１を非切断とし、Ｆ２とＦ３を切断することによりバックゲート電圧としてV_{G1}＝－１Ｖを印加する。また、測定値が１．４×10^{17}ｃｍ$^{-3}$～１．６×10^{17}ｃｍ$^{-3}$の時は、Ｆ２を非切断とし、Ｆ１とＦ３を切断することによりバックゲート電圧としてV_{G2}＝０Ｖを印加する。さらに、測定値が１．６×10^{17}ｃｍ$^{-3}$～１．８×10^{17}ｃｍ$^{-3}$の時は、Ｆ３を非切断とし、Ｆ１とＦ２を切断することによりバックゲート電圧としてV_{G3}＝１Ｖを印加するようにヒューズを各々切断する。このようにすれば、測定値に基づいて、所望の範囲内のバックゲート電圧を印加することが可能となり、所望のしきい値に近いしきい値を得ることができる。

【０１４１】図３６は、図３５の電源V_{G1}～V_{G3}を、昇降圧回路に置き換えた例である。このようにすれば、従来から用いられている電源電圧を基にして適宜、所定のバックゲート電圧に昇圧または降圧することができる点で便利である。

【０１４２】図３７は、例えば、電源電圧であるＶcc＝３ＶからＶss＝０Ｖまでの、Ｖcc～Ｖssの電圧範囲内で適宜分圧して、バックゲート電圧として用いる例である。例えば抵抗Ｒからなる抵抗器を直列に接続し、それぞれの端子にて電圧が抽出できるようにヒューズを配線する。そして、バックゲート電圧印加の際には、例えばヒューズＦ２を非切断、Ｆ１、Ｆ３を切断することで２／３Ｖcc、またＦ３を非切断、Ｆ１、Ｆ２を切断することで１／３Ｖcc、そして例えば全てのヒューズを非切断することでＶccの電圧をバックゲートに印加することができる。図３７では抵抗器を３つ設けたが、複数個であればよく、より多くの抵抗器を設ければ、より細かく分圧されることになり、所望のしきい値に近い値を得ることができる。また電圧の範囲は、Ｖcc～Ｖssの範囲に限らず、昇降圧回路を用いることで範囲を変えることも可能である。

【０１４３】図３８は、図３７の変形例であり、２つの抵抗器と１つのヒューズとからなるセルをｎ個用いることで、例えばＶcc～Ｖssまでの電圧の範囲を分割することができる回路例である。

【０１４４】また、図３７のように、抵抗器の出力を直接基板バイアスノードに加える他に、図３９に示したように、制御入力によって出力電圧が変化する可変電源に

GF Exhibit 1124 - 1680/2704

抵抗器出力を接続してもよい。このようにすることにより、抵抗器に流す電流を小さくしても大きな基板バイアス出力電流が得られるという利点がある。

【０１４５】さらに図４０のように、複数のチャージポンプ回路を縦続接続し、基板バイアス電圧を記憶素子のヒューズＦ１～Ｆ３の状態によって切り替えるようにしても良い。ここでトランジスタのしきい値をV_tとすると、Ｆ１、Ｆ２、Ｆ３が非切断の時、基板バイアス電源出力の開放電圧は$-3Vcc+4V_t$、Ｆ１、Ｆ２非切断、Ｆ３切断の時、$-2Vcc+4V_t$、Ｆ１非切断、Ｆ２、Ｆ３切断の時$-Vcc+4V_t$の出力を得ることができる。

【０１４６】本具体例において用いる記憶素子としては、上述したようなヒューズを切断する方法の他にも、例えば、浮遊ゲート電極に電荷を蓄積する方法や、強誘電体を分極させて記憶させる方法、さらには、金属またはシリサイドにはさまれた薄い半導体または絶縁体の絶縁破壊によって記憶させる方法、いわゆるアンチヒューズを用いてもよい。

【０１４７】以上、具体例を例示しつつ本発明の実施の形態について説明した。しかし、本発明は、上述した各具体例に限定されるものではない。

【０１４８】例えば、絶縁膜の形成法としては、熱酸化による酸化膜形成法や、３０ｋｅＶ程度の低加速エネルギーで酸素を注入した酸化膜を形成する方法としてもよいし、シリコン酸化膜を堆積する方法や、シリコン窒化膜を堆積する方法、またはこれらを組み合わせた方法でもよい。また、シリコンをシリコン酸化膜やシリコン窒化膜に変換するこれら以外の方法、例えば酸素イオンを堆積したシリコンに注入する方法や、堆積したシリコンを酸化する方法を用いてもかまわない。また、これらの絶縁膜に、シリコン窒化膜その他タンタル酸化膜、チタン酸化膜、チタン酸ストロンチウムやチタン酸バリウム、チタン酸ジルコニウム鉛などの強誘電体膜、常誘電体膜の単層膜またはそれらの複合膜を用いることもできる。

【０１４９】また、上述した具体例においては特に言及していないが、素子分離としては、トレンチ分離の素子分離や、ＬＯＣＯＳ素子分離膜や、リセス型（Recessed）ＬＯＣＯＳや改良ＬＯＣＯＳ法やフィールドシールド分離を用いても良いし、これらを組み合わせてもよい。

【０１５０】さらに、上述した各具体例では、ＳＯＩ層としてｐ型Ｓｉを用いたが、代わりにｎ型ＳｉやＧａＡｓ、ＩｎＰを用いても良い。また、ｎ型ＭＩＳＦＥＴではなくｐ型ＭＩＳＦＥＴに適用してもよく、その場合、上述の実施例のｎ型をｐ型、ｐ型をｎ型と読み替え、さらに、ドーピング不純物種のＡｓ、Ｐ、Ｓｂなどを Ｉｎ、Ｂなどのいずれかと読み替え、イオン注入の場合にもＡｓ、Ｐ、ＳｂをＩｎ、Ｂ、ＢＦ2 のいずれかと読み替えればよい。

【０１５１】さらに、ゲート電極は、多結晶シリコン以外の単結晶シリコン、ポーラス（多孔質）シリコン、アモルファスシリコン、ＳｉＧｅ混晶、ＳｉＣ混晶、ＧａＡｓ、Ｗ、Ｔａ、Ｔｉ、Ｈｆ、Ｃｏ、Ｐｔ、Ｐｄの金属あるいはシリサイドを用いることもできる。さらに、これらの積層構造としても良い。

【０１５２】その他、本発明の趣旨を逸脱しない範囲で種々に変形して実施することができる。

【０１５３】

【発明の効果】本発明は、以上説明した形態で実施され、以下に説明する効果を奏する。

【０１５４】まず、本発明によれば、完全空乏化トランジスタで問題となるＳＯＩ膜厚や不純物濃度のバラツキに対するしきい値感度をほぼ最小に保ったままで、かつしきい値を所望の値にすることが可能である。

【０１５５】また、本発明によれば、例えば集積回路を形成した場合に、不純物濃度のばらつきを補正し、従来例よりもＳＯＩ膜厚ばらつきに対するしきい値感度が小さいので、より、特性が均一な素子を集積できる。

【０１５６】一方、ＭＯＳ論理回路では、トランジスタのしきい値が高くなると、電流駆動能力が落ち遅延時間が長くなる一方、しきい値が低くなると、ｏｆｆ時のサブスレッショルドリーク電流が大きくなる。よって、本発明によれば、より遅延時間や消費電力のばらつきを小さく保つことができる。

【０１５７】また、遅延時間はしきい値V_{th}に対し、電源電圧をV_{DD}として（$V_{DD}-V_{th}$）$-\alpha$（αは１以上の正の数）に比例する。よって、遅延時間をV_{th}のばらつき分だけ低下させることができ、より遅延時間が同じでも低電圧動作させることができる。よって、低電圧動作させることによって、より例えばゲート絶縁膜の電源電圧に対する信頼性を向上させ、ゲート充放電の消費電力を小さくすることができる。

【０１５８】また、本発明によれば、ＬＯＣＯＳ犠牲酸化によるリセスゲート構造を形成した場合においても、所望のしきい値でＳＯＩ膜厚のばらつきに対してしきい値感度が最小となるようなＳＯＩ膜厚を設定することにより、このＳＯＩ膜厚付近でのしきい値の変動が最小化されるため、所望のしきい値を得ることができる。

【０１５９】また、ペアトランジスタ間のしきい値のばらつきをより抑えられるので、例えばカレントミラー回路や交差結合型センスアンプをより精度よく対称に実現することができ、より電流源の精度やセンスアンプの感度を増大することができる。さらに、本発明によれば、２つ以上のしきい値を持つＭＩＳＦＥＴを集積した半導体回路に対し、ＳＯＩ膜厚ばらつきに対するしきい値感度をそれぞれの素子に対して極小とすることができる。これはＣＭＯＳ回路においても、ｎ型ＭＩＳＦＥＴ、ｐ型ＭＩＳＦＥＴの所望のしきい値に応じたＳＯＩ膜厚で

GF Exhibit 1124 - 1681/2704

形成された完全空乏化ＭＩＳＦＥＴでは、それぞれのＭＩＳＦＥＴにおいて、ＳＯＩ膜厚バラツキに起因するしきい値感度は最小になる。これは従来の単一なＳＯＩ膜厚を有するＦＤ－ＳＯＩＭＩＳＦＥＴでは困難である。よって、複数のしきい値を有するトランジスタやＣＭＯＳ回路を用いた論理回路において、ＳＯＩ膜厚がばらついても、各々所望のしきい値で、しきい値感度をほぼ最小に保つことができる。また、本発明によれば、不純物濃度に応じたバックゲート電圧制御回路はｈａｌｆ－V_{dd}回路や、基板バイアス回路を応用することにより、同一基板上に形成することも可能である。

【０１６０】また、本発明においてＭＩＳＦＥＴを形成する半導体層の不純物濃度を抵抗を測定することから求める手法は、キャパシタンスの容量を測定する手法により低電圧で行うことができ、そしてゲート酸化膜耐圧による印加電圧の限界に問題はないという利点を有する。一方、キャパシタンスの容量測定より不純物濃度を求める手法では、抵抗測定による手法より感度が高く、消費電力を小さくすることが可能であるという利点を有する。

【０１６１】さらに、本発明のダミー素子の製造に際しては、ＭＩＳＦＥＴに用いるゲートをそのまま用いることもできるため、従来の半導体装置の工程数で同一基板上に不純物濃度測定のためのダミー素子を形成することができる。

【０１６２】また、本発明によれば、薄いＳＯＩ膜厚からなる半導体層の不純物濃度測定のためのダミー素子を、厚いＳＯＩ膜厚からなる半導体層領域に形成することにより、ダミー素子のｐｎ接合形成のための膜厚マージンを確保することができる。そして、例えば、ｐ型半導体層にイオン注入によりｎ型層を形成しｐｎ接合領域を形成するとき、ｎ型ＭＩＳＦＥＴにおけるソース・ドレイン電極領域形成のイオン注入と同時に行うことで、リソグラフィー工程を現状のままで、ｐｎ接合領域を形成することが可能である。

【０１６３】以上説明したように、本発明によれば、完全空乏化トランジスタを有する半導体装置において、ＳＯＩ膜厚や不純物濃度のばらつきに対するしきい値感度をほぼ最小に保ったままで、しきい値を所望する値にすることができ、産業上のメリットは多大である。

【図面の簡単な説明】

【図１】本発明の第１の具体例に係わる半導体装置を表す要部断面図である。

【図２】本発明者の計算により得られた完全空乏化ＦＥＴのＳＯＩ層としきい値との関係を表すグラフ図である。

【図３】式（２）～（５）により、チャネル領域４の不純物濃度N_A＝１×10^{17}ｃｍ$^{-3}$、ＳＯＩ膜厚t_{si}＝６０ｎｍ、Φ_{Ms1}＝－１Ｖ、Q_{0X1}＝Q_{0X2}＝０の場合について計算したバックゲート電圧に対するしきい値の関係を表したグラフである。

【図４】チャネル領域４の不純物濃度を１×10^{17}ｃｍ$^{-3}$としたときの、式（２）～（５）の古典論モデルを用いて計算したしきい値のチャネル領域４のＳＯＩ膜厚の依存性を示したグラフである。

【図５】表面量子化補正を説明するためのバンド図である。

【図６】図２と同一のＦＥＴのモデルにおいて、図２でしきい値が極小となるチャネル領域４のＳＯＩ膜厚t_{Si}と印加するバックゲート電圧V_{G2}とを、チャネル領域４の不純物濃度N_Aに対して示したグラフである。

【図７】ＬＯＣＯＳ犠牲酸化などの方法により形成されたリセス（Recess）ゲート構造を有するＭＩＳＦＥＴを表す断面図である。

【図８】ＬＯＣＯＳ犠牲酸化法によるリセス型ゲート構造の製造工程を表す概略工程断面図である。

【図９】本発明の半導体装置の第２の具体例を表す概略断面図である。

【図１０】ｈａｌｆ－V_{dd}回路を用いた実施例を表す概略回路図である。

【図１１】基板バイアス回路による実施例を表す概略回路図である。

【図１２】図９の半導体装置の要部製造工程を表す工程断面図である。

【図１３】図９の半導体装置の要部製造工程を表す工程断面図である。

【図１４】図９の半導体装置の要部製造工程を表す工程断面図である。

【図１５】本発明の半導体装置の第３の具体例を表す概略断面図である。

【図１６】図１５の半導体装置の要部製造工程を表す概略工程断面図である。

【図１７】図１５の半導体装置の要部製造工程を表す概略工程断面図である。

【図１８】本発明の半導体装置の第４の具体例を表す概略断面図である。

【図１９】回路９ｃ、１０ｂの具体例を表す概略回路図である。

【図２０】図１８の半導体装置の要部製造工程を表す概略工程断面図である。

【図２１】図１８の半導体装置の要部製造工程を表す概略工程断面図である。

【図２２】ｐｎ接合により不純物濃度を測定するためのダミー素子を設けた半導体装置を例示する概略断面図である。

【図２３】図２２のダミー素子を含めた回路９ｄ、１０ｂの具体例を表す概略回路図である。

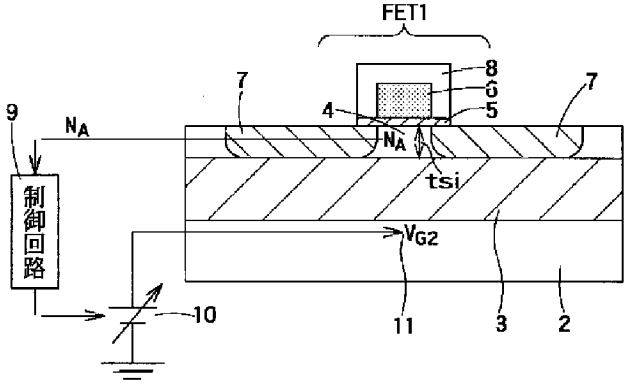
【図２４】本発明の第５の具体例に係わる半導体装置の概略断面図である。

【図２５】図２４の半導体装置の要部製造工程を表す概

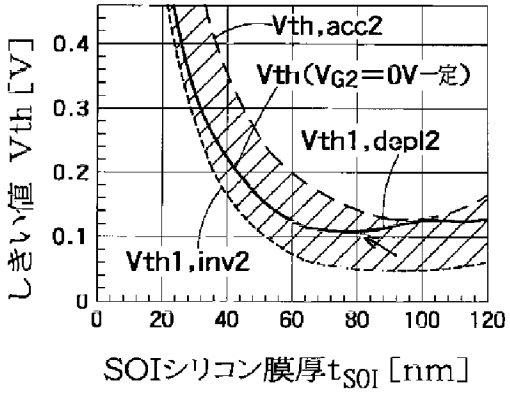
GF Exhibit 1124 - 1682/2704

略工程断面図である。
【図２６】本発明の第６の具体例に係わる半導体装置の概略断面図である。
【図２７】リン（Ｐ）をイオン注入する工程を表す概略断面図である。
【図２８】ＬＯＣＯＳ犠牲酸化によるリセス（Recess）構造を用いることにより膜厚の薄いＳＯＩ領域を形成する技術を説明する工程断面図である。
【図２９】コーンケーブ（concave）構造を表す概略断面図である。
【図３０】第７具体例に係わる半導体装置の要部断面図である。
【図３１】第７具体例における各構成要素の関連を説明する機能ブロック図である。
【図３２】図３０の半導体装置の製造工程を説明するための断面図である。
【図３３】図３０の半導体装置の製造工程を説明するための断面図である。
【図３４】図３０の半導体装置の製造工程を説明するための断面図である。
【図３５】第７具体例で用いることができる記憶素子を含んだバイアス回路の構成例を表す。
【図３６】第７具体例で用いることができる記憶素子を含んだバイアス回路の構成例を表す。
【図３７】第７具体例で用いることができる記憶素子を含んだバイアス回路の構成例を表す。
【図３８】第７具体例で用いることができる記憶素子を含んだバイアス回路の構成例を表す。
【図３９】第７具体例で用いることができる記憶素子を含んだバイアス回路の構成例を表す。
【図４０】第７具体例で用いることができる記憶素子を含んだバイアス回路の構成例を表す。
【符号の説明】
１　完全空乏化トランジスタ
２　導電性支持基板
３　絶縁膜
４　チャネル領域
５　ゲート絶縁膜
６　ゲート電極
７　ソース・ドレイン電極
８，１４　絶縁膜
９　制御回路
１０　可変電源（電圧制御電圧源）
１１　バックゲート
１２　素子分離領域
１３　半導体層領域
１５　レジスト
１８　電極
１９　メタルプラグ
Ｆ１～Ｆ３　ヒューズ

【図１】

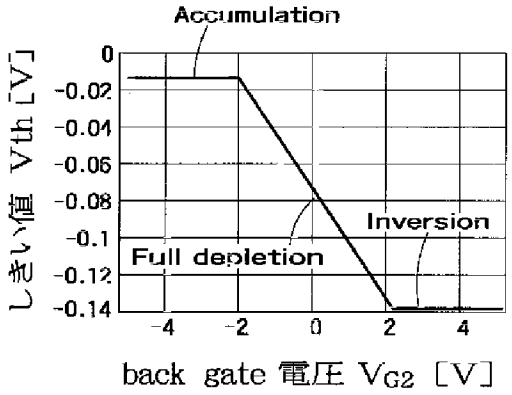


【図２】

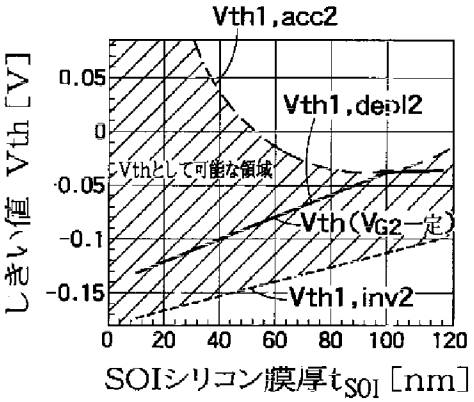


GF Exhibit 1124 - 1683/2704

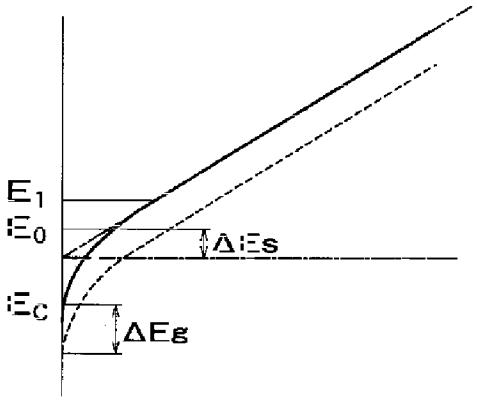
【図3】



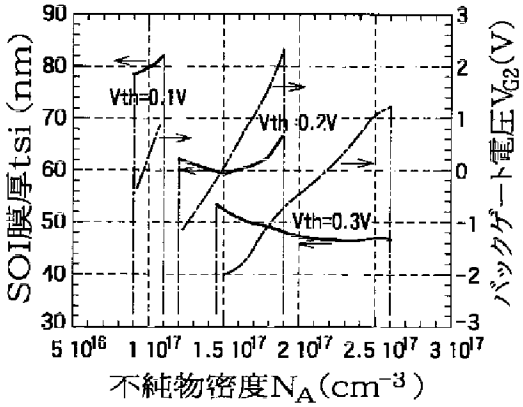
【図4】



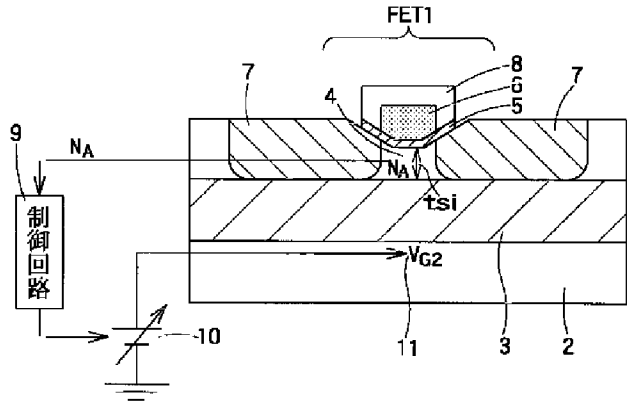
【図5】



【図6】

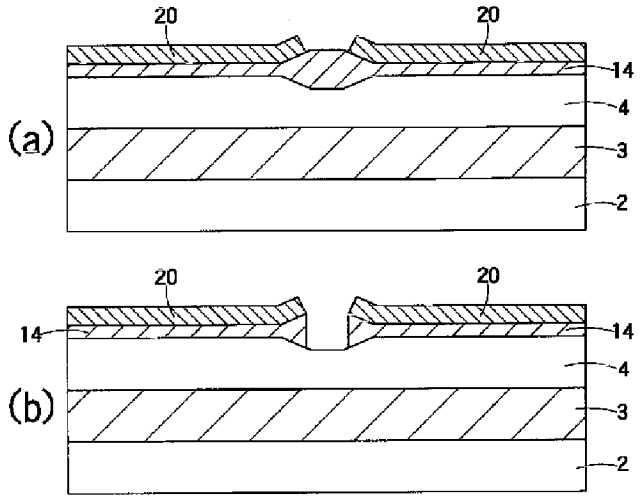


【図7】

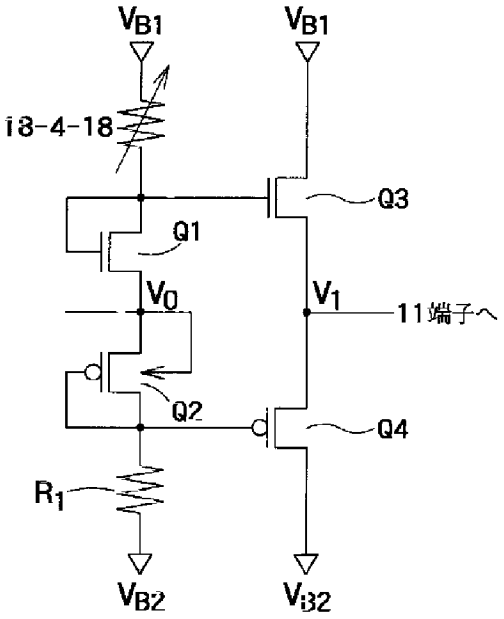


GF Exhibit 1124 - 1684/2704

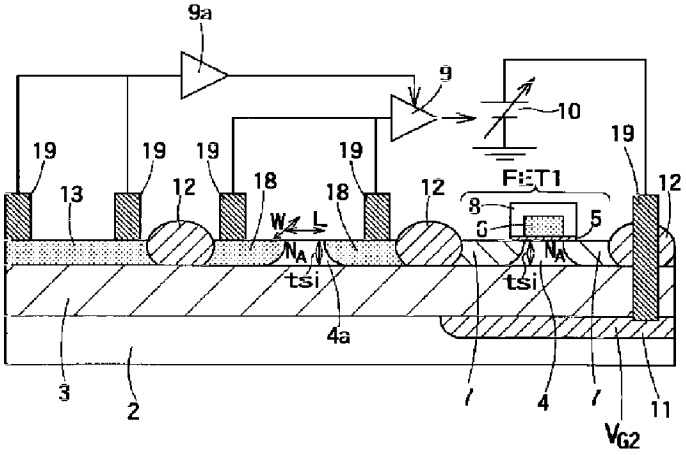
【図8】



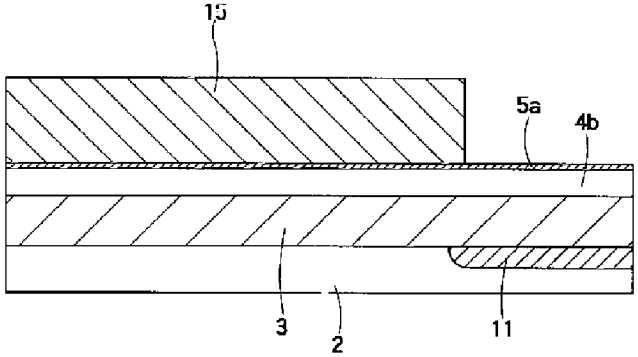
【図10】



【図9】

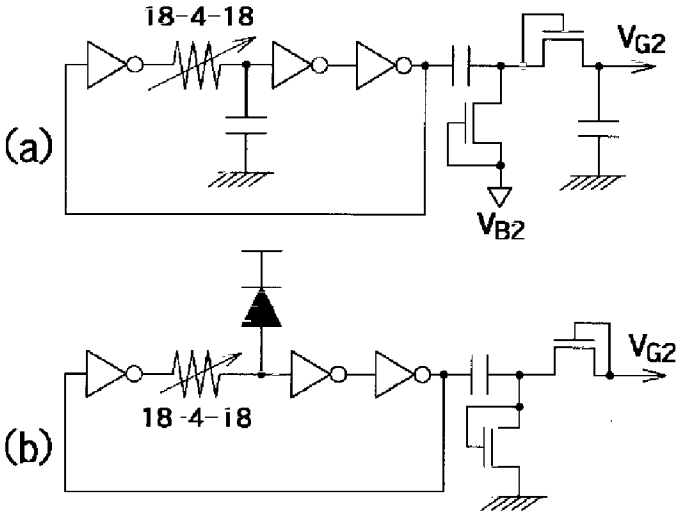


【図12】

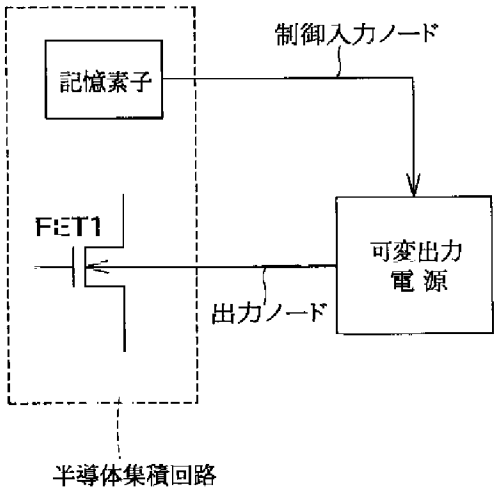


GF Exhibit 1124 - 1685/2704

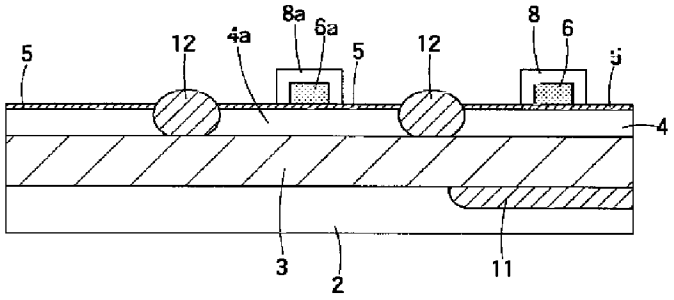
【図１１】



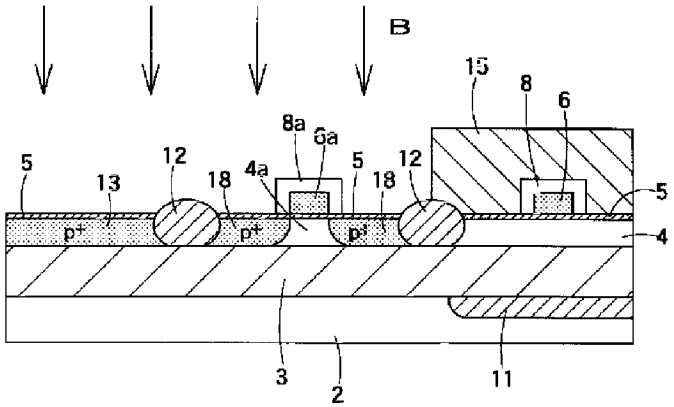
【図３１】



【図１３】

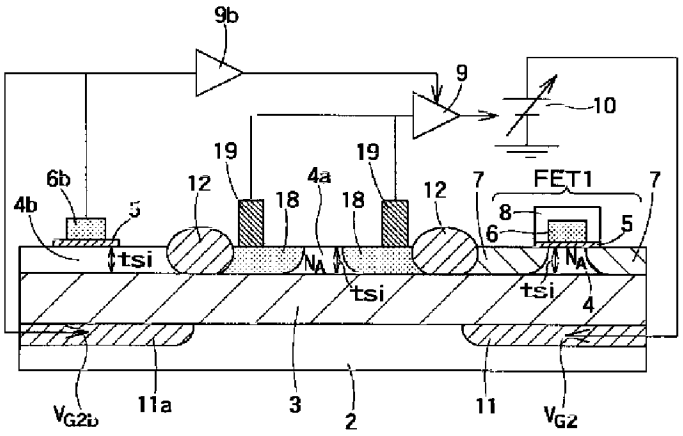


【図１４】

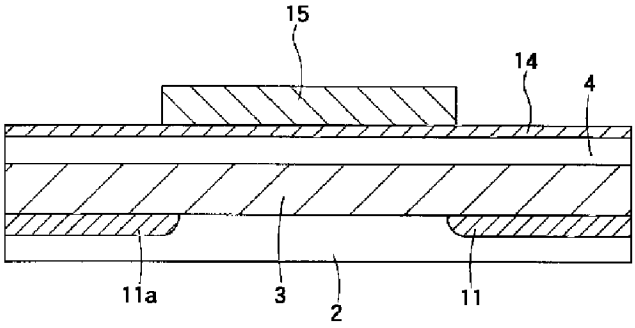


GF Exhibit 1124 - 1686/2704

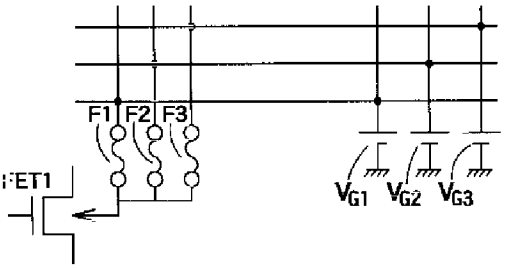
【図１５】



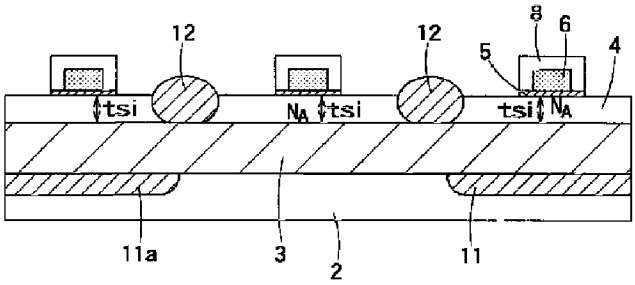
【図１６】



【図３５】

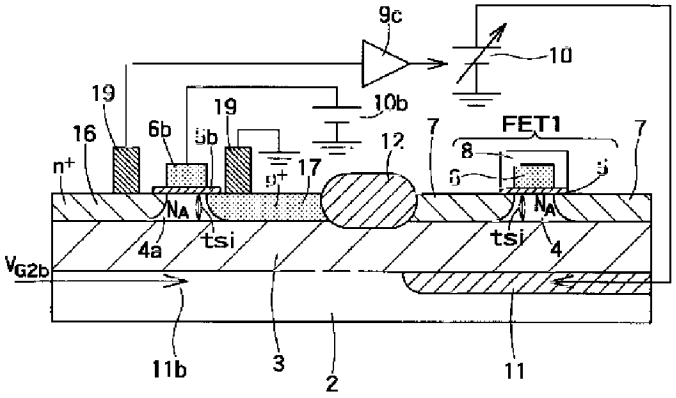


【図１７】

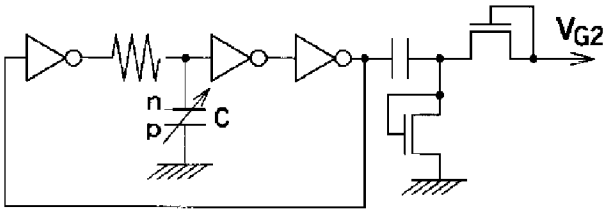


GF Exhibit 1124 - 1687/2704

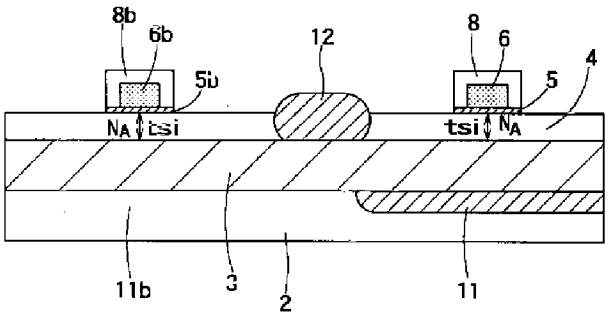
【図１８】



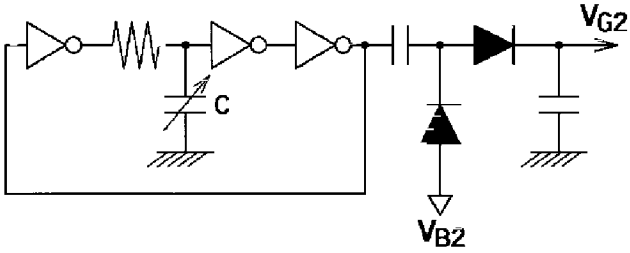
【図１９】



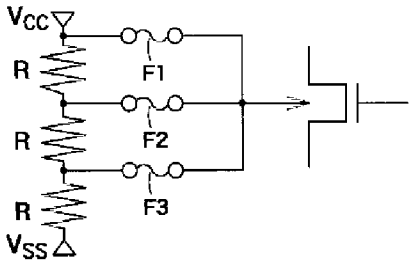
【図２０】



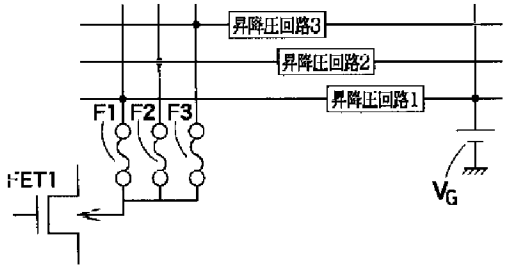
【図２３】



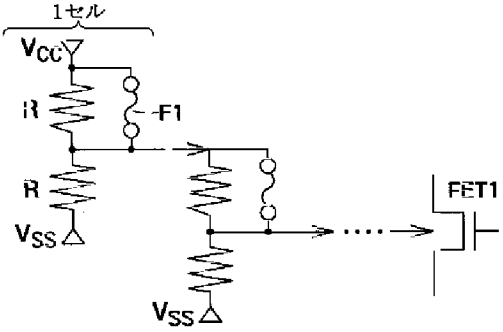
【図３７】



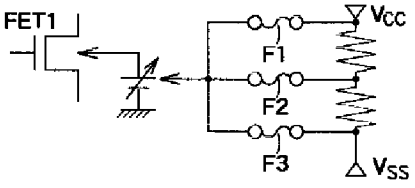
【図３６】



【図３８】

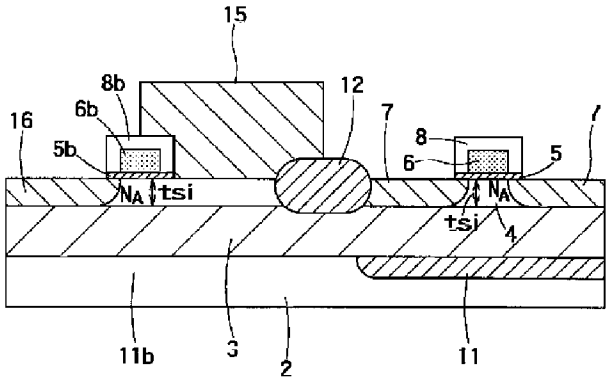


【図３９】

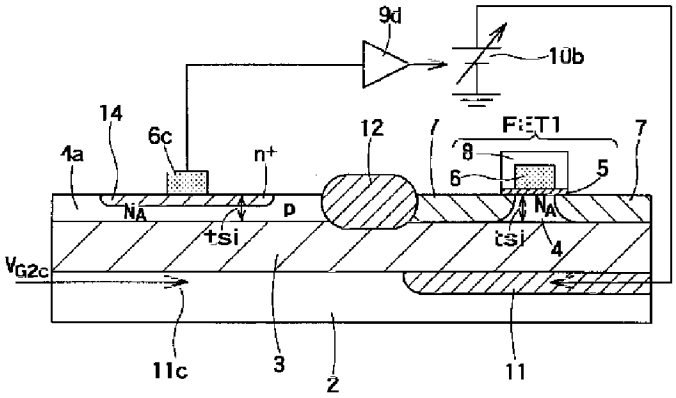


GF Exhibit 1124 - 1688/2704

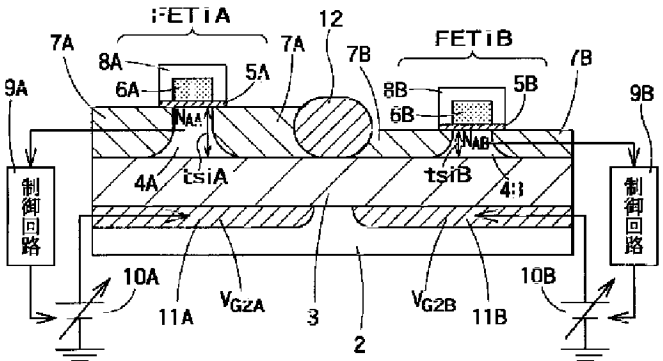
【図２１】



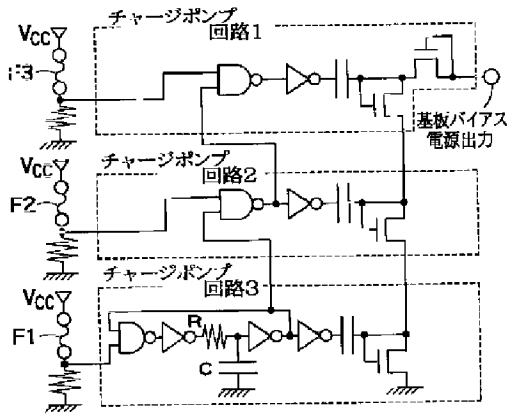
【図２２】



【図２４】

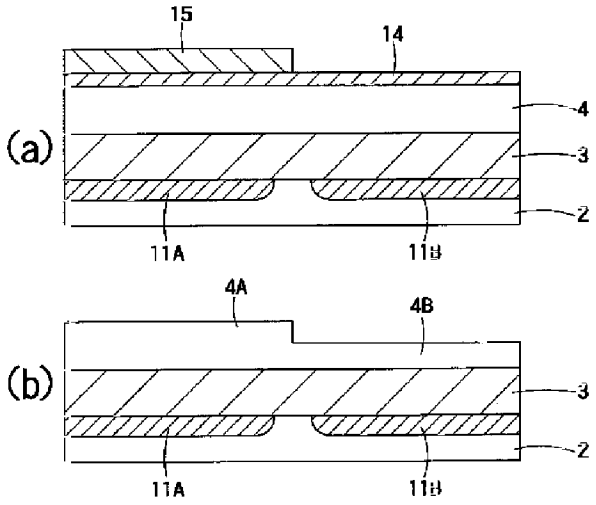


【図４０】

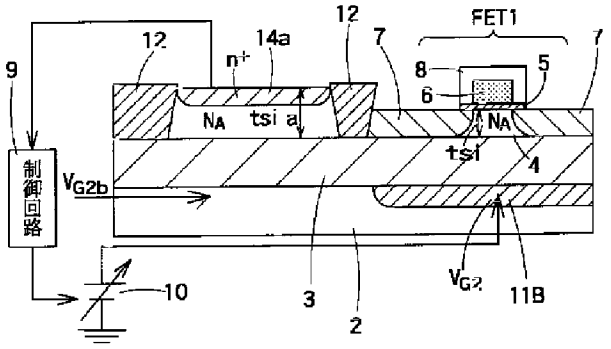


GF Exhibit 1124 - 1689/2704

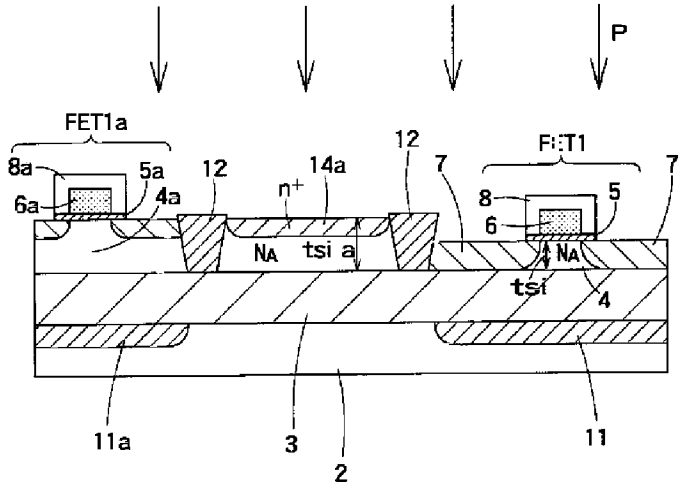
【図25】



【図26】

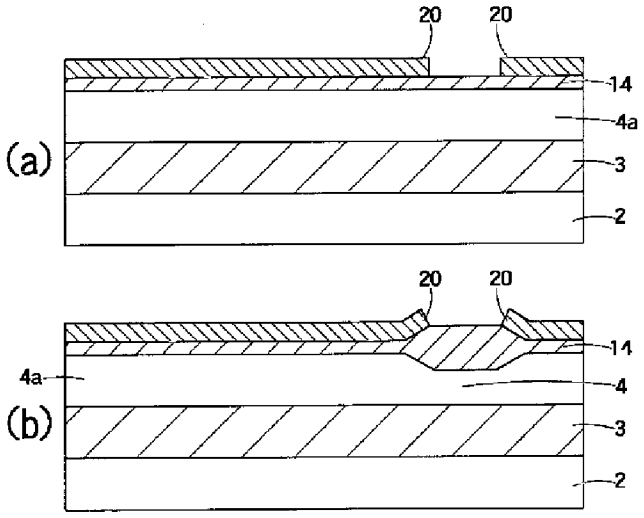


【図27】

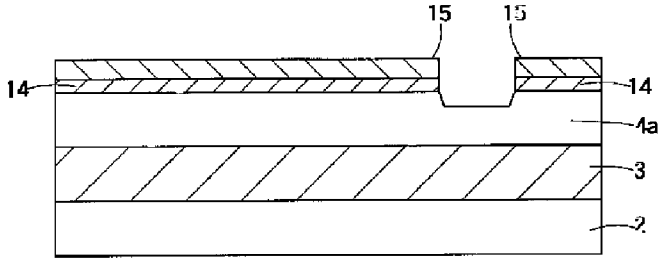


GF Exhibit 1124 - 1690/2704

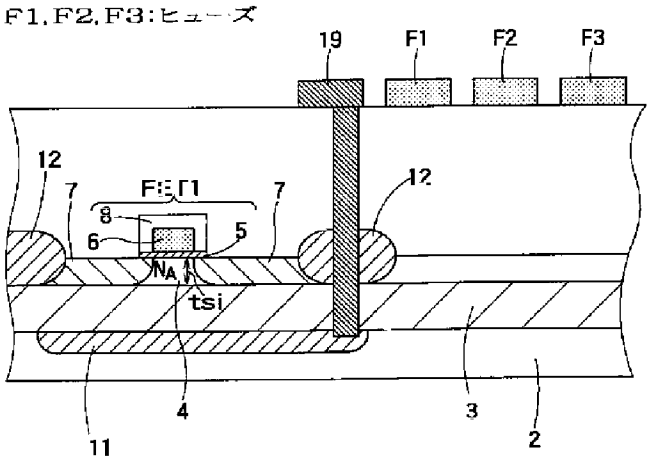
【図２８】



【図２９】

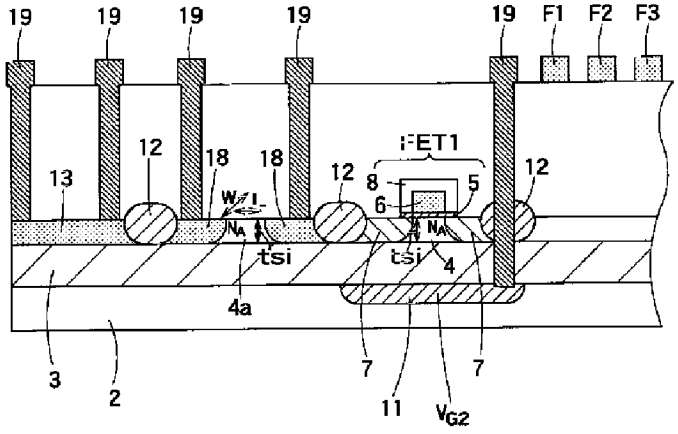


【図３０】

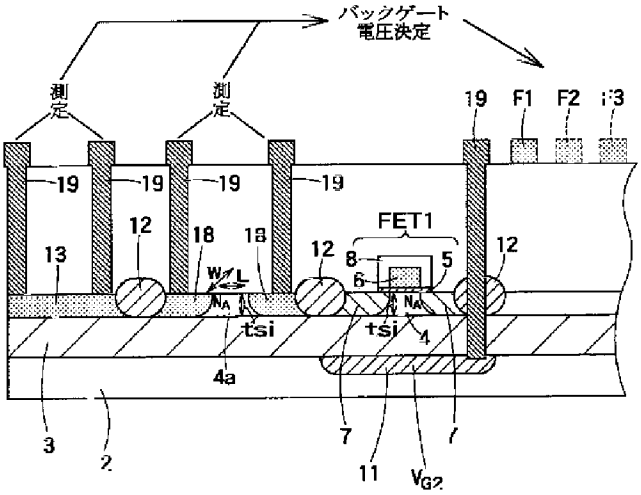


GF Exhibit 1124 - 1691/2704

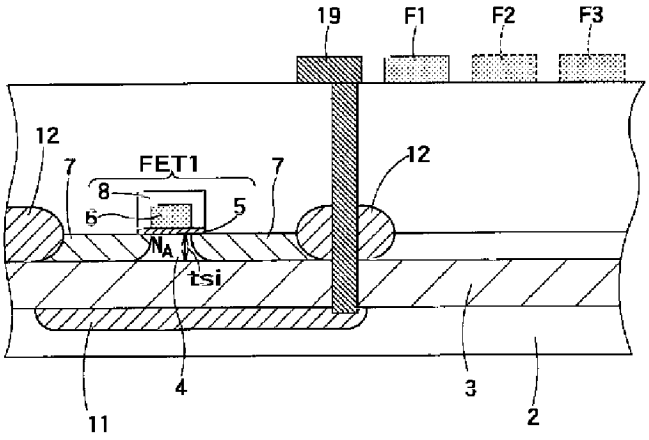
【図３２】



【図３３】



【図３４】



GF Exhibit 1124 - 1692/2704

Espacenet

JPH11330482A SEMICONDUCTOR DEVICE

Applicants: TOSHIBA CORP

Inventors: NOGUCHI MITSUHIRO,NUMATA TOSHINORI

Classifications:

IPC ***B82B1/00; H01L21/336; H01L21/84; H01L27/12; H01L29/786;*** (IPC1-7): H01L29/786;

CPC **H01L21/84 (EP); H01L27/1203 (EP); H01L29/66772 (EP); H01L29/78648 (EP); H01L29/78696 (EP);**

Priorities: JP13723698A 1998-05-19

Application: JPH11330482A·1998-05-19

Publication: JPH11330482A·1999-11-30

Published as: JPH11330482A;**JP3699823B2; US6043536A**

SEMICONDUCTOR DEVICE

Abstract

PROBLEM TO BE SOLVED: To hold threshold sensitivity for variations of a SOI film thickness substantially at a minimum to set to a value prescribing a threshold by a method, wherein a back gate voltage is applied from a control circuit, in response to channel impurity concentration of transistors. SOLUTION: An insulating film 3, such as a silicon oxide film or the like, is formed on the main face of a silicon substrate 2, and a channel region 4 of silicon having a p-type impurity concentration NA, such as boron is formed on this insulating film. A gate electrode 6 is formed via the gate insulating film 5 on the channel region 4, and a source/drain region 7 is formed on both sides of the channel region 4, to form completely depleted transistors FET1. A control circuit 9 inputs the information measuring the impurity concentration NA and calculates an optimum back gate voltage value and outputs a corresponding control signal to a variable power source 10, so that a specified voltage is applied on a back gate 11. This application substantially minimizes the threshold sensitivity for variations of a SOI film thickness by controlling the threshold.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION JPH11330482

[0001]
TECHNICAL FIELD The present invention relates to a semiconductor device. More specifically, the present invention relates to a semiconductor device in which a fully depleted MISFET (Metal Insulator Semiconductor Field Effect Transistor) is formed on a semiconductor layer provided on a supporting substrate via an insulating film.

[0002]

2. Description of the Related Art A FET type transistor formed by using an SOI (Silicon on Insulator), that is, a semiconductor layer formed on an insulating substrate, has a parasitic capacitance between a source and a drain, which is a bulk semiconductor substrate. Since it can be made smaller than the FET formed above, it is expected to be applied to a low power consumption device or a high speed operation circuit such as a high speed CPU. In particular, when the thickness of the SOI film which is the semiconductor layer is set to be equal to or less than the thickness of the depletion layer in the channel region, the channel region can be completely depleted. As a result, it is possible to eliminate or suppress an unfavorable phenomenon such as a kink characteristic or a current overshoot effect, which is a problem in an SOI transistor formed using a semiconductor layer thicker than a depletion layer.

[0003]
In this way, a transistor capable of depleting the entire channel region (hereinafter, referred to as “completely depleted transistor”) further suppresses the short channel effect, improves punch-

GF Exhibit 1124 - 1694/2704

through resistance, improves the subthreshold coefficient, It offers a number of benefits, including increased channel mobility.

[0004]
However, in the fully depleted transistor, if the impurity concentration of the semiconductor layer in the channel region or the SOI film thickness changes due to variations in process conditions, the threshold value changes. There was a problem.

[0005]
As a method of coping with the problem caused by such variation in process conditions, conventionally, as disclosed in, for example, Japanese Patent Laid-Open No. 9-321401, a back surface of a support substrate below an insulating layer below an SOI layer is backed up. An example is known in which a gate is provided and the threshold voltage is controlled by changing the voltage applied to the back gate during operation and during standby.

[0006]

However, in this method, the back gate voltage is determined regardless of variations in the SOI film thickness and variations in the substrate concentration.

Further, for example, there is no disclosure about a back gate voltage applying means for minimizing the threshold sensitivity to variations in the SOI film thickness and its specific configuration.

[0007]

That is, in the conventional method and structure for reducing the threshold sensitivity in the fully depleted transistor, the back gate voltage control for reducing the threshold sensitivity with respect to the variation in the SOI film thickness has been studied. The optimum value of, and the relationship with the impurity concentration were not considered.

Therefore, it is difficult to set the threshold value to a prescribed value and reduce the threshold sensitivity to variations in the film thickness of the SOI layer and the impurity concentration.

GF Exhibit 1124 - 1695/2704

[0008]

The present invention has been made based on the recognition of such problems.

That is, the purpose is to change the back gate voltage depending on the channel impurity concentration of MIFSET in a semiconductor device formed by forming a fully depleted MISFET transistor using an SOI layer so that the impurity concentration is It is an object of the present invention to provide a semiconductor device in which the threshold value can be set to a value that regulates the threshold value while keeping the threshold sensitivity to the SOI film thickness variation to a minimum even if it fluctuates.

[0009]
The gist of the present invention is to provide a semiconductor device in which a fully depleted transistor is formed in a semiconductor layer opposed to a back gate with an insulating film interposed therebetween, depending on the channel impurity concentration of the transistor. A semiconductor device characterized in that a control circuit capable of controlling a back gate voltage is provided to apply a back gate voltage according to an impurity concentration to the back gate.

[0010]

The semiconductor layer forming the fully-depleted SOI transistor is set to an SOI film thickness at which the threshold fluctuation is reduced at a specified threshold, and the impurity concentration is in contact with the insulating film of the semiconductor layer. The surface is set within a range determined by accumulation and inversion, for example, in the middle.

Here, if the specified threshold values are different, the film thickness for suppressing the threshold variation is different.

[0011]
That is, the semiconductor device of the present invention includes a support substrate having a back gate formed thereon, an insulating film provided on the support substrate, a first

GF Exhibit 1124 - 1696/2704

semiconductor layer provided on the insulating film, and the support substrate. Of a MISFET transistor facing the back gate and having a part of the first semiconductor layer as a channel region, and a dummy element for outputting a measurement signal that changes according to an impurity concentration or a carrier concentration of the first semiconductor layer. And voltage applying means for applying a voltage to the back gate according to the measurement signal output from the dummy element.

[0012]
Alternatively, in the semiconductor device of the present invention, a supporting substrate on which the first and second back gates are formed, an insulating film provided on the supporting substrate, and a first film thickness provided on the insulating film. Provided on the insulating film, a first semiconductor layer having a first semiconductor layer, a first MISFET transistor facing the first back gate of the support substrate and having a part of the first semiconductor layer as a channel region, A second semiconductor layer having a second film thickness different from the first film thickness, and a part of the second semiconductor layer facing the second back gate of the support substrate to form a channel region. And a voltage applying means for applying a voltage to the first back gate independently of the voltage of the second back gate.

[0013]
Alternatively, in the semiconductor device of the present invention, a supporting substrate having a back gate formed thereon, an insulating film provided on the supporting substrate, a first semiconductor layer provided on the insulating film, and the supporting substrate. Of a MISFET transistor having a channel region of a part of the first semiconductor layer facing the back gate, a storage element for storing information corresponding to a voltage applied to the back gate, and a storage element stored in the storage element. And a voltage applying unit that applies a voltage to the back gate based on the information.

[0014]
Alternatively, in the semiconductor device of the present invention, a supporting substrate on which the first and second back gates are formed, an insulating film provided on the supporting substrate, and a first film thickness provided on the insulating film. A first semiconductor layer having: a first MISFET transistor facing the first back gate of the supporting substrate and having a part of the first semiconductor layer as a channel region; and the first back gate. A first memory element that stores information corresponding to a voltage applied to the second semiconductor layer; a second semiconductor layer that is provided on the insulating film and has a second film thickness different from the first film thickness; A second MISFET transistor in which a part of the second semiconductor layer is used as a channel region facing the second back gate of the substrate, and the voltage of the second back gate is independent of the first

GF Exhibit 1124 - 1697/2704

MISFET transistor. Voltage applying means for applying a voltage to the first back gate based on the information stored in the storage element.

[0015]
Here, the storage element stores information according to an impurity concentration or a carrier concentration of the first semiconductor layer.

[0016]
Further, the MISFET transistor is a fully depleted transistor in which the channel region is completely depleted.

[0017]
In addition, the dummy element is an impedance element in which at least one of a resistance value, a capacitance value, and an inductance changes according to an impurity concentration or a carrier concentration of the first or second semiconductor layer. .

[0018]
The thickness of the first or second semiconductor layer in which the channel region of the MISFET transistor is formed is in the range of 40 nm to 100 nm, and the impurity concentration is in the range of 3×10 16 cm -3 to 3×10 17 cm -3. It is characterized by being in.

[0019]
Further, the support substrate is formed of a semiconductor substrate, and the impurity concentration of the back gate is in the range of 1×10 17 cm -3 to 1×10 20 cm -3.

[0020]
Further, a circuit for measuring the impurity concentration or the carrier concentration by the dummy element is provided on the same semiconductor layer as the MISFET transistor.

[0021]
Further, the first semiconductor layer is thicker than the second semiconductor layer, and the first semiconductor layer is lower in impurity concentration than the second semiconductor layer.

GF Exhibit 1124 - 1698/2704

[0022]
Further, the threshold value of the first MISFET transistor is smaller than the threshold value of the second MISFET transistor.

[0023]

According to the present invention, the film thickness of the SOI layer is set to a film thickness with which the threshold variation is reduced.

Furthermore, a desired threshold value can be maintained by measuring the impurity concentration of the channel region using the dummy element and adjusting the back gate voltage based on the measured value.

Therefore, the threshold value can be set to a desired value while keeping the threshold sensitivity to the variation of the SOI film thickness and the impurity concentration, which is a problem in the fully depleted transistor, at a minimum.

[0024]

Embodiments of the present invention will be described below with reference to the drawings.

In the following description, an n-type MOSFET will be described as an example.

Further, the pattern shape of the element isolation of the SOI layer is not essential in the present invention, and is not particularly mentioned.

[0025]

FIG. 1 is a cross-sectional view of essential parts showing a semiconductor device according to a first example of the present invention.

GF Exhibit 1124 - 1699/2704

That is, in the figure, 6 is a gate electrode, 7 is a source / drain region, 2 is a support substrate, 3 is an insulating film, 4 is a channel region, 5 is a gate insulating film, 8 is an insulating film, 9 is a control circuit, and 10 is a control circuit. Is a variable power supply (for example, a power supply whose output current or voltage is controlled by the voltage or current of the control input), and 11 represents a back gate.

[0026]

The specific configuration example is as follows.

That is, the insulating film 3 made of, for example, a silicon oxide film or a silicon nitride film having a thickness of 10 nm to 1 μm is formed on the main surface of the support substrate 2 made of silicon, and the film thickness tsi, boron or indium is formed on the insulating film 3. A channel region 4 made of silicon or the like having a p-type impurity concentration NA is formed.

The film thickness tsi may be, for example, 1 nm to 500 nm, and the impurity concentration NA may be, for example, 1016 to 1019 cm-3.

[0027]

A gate electrode 6 is formed on the channel region 4 with a gate insulating film 5 interposed therebetween.

As a material of the gate insulating film 5, for example, a silicon oxide film, a silicon nitride film, a tantalum oxide film, a titanium oxide film, or the like can be used, and the thickness thereof can be set to 1 nm to 200 nm.

As a material of the gate electrode 6, for example, polycrystalline silicon, aluminum (Al), tungsten (W), titanium nitride (TiN), or the like can be used, and the thickness thereof can be set to 10 nm to 1 μm.

GF Exhibit 1124 - 1700/2704

[0028]

The gate electrode 6 is insulated by covering its sidewall with an insulating film 8 made of, for example, a silicon oxide film or a silicon nitride film.

On both sides of the channel region 4, there are formed source / drain regions 7 to which arsenic (As), phosphorus (P), antimony (Sb), etc., which are n-type impurities, are added, for example, 10 18 to 10 21 cm −3.

Here, the channel region 4 is completely depleted in the state where the inversion layer is formed at the interface between the channel region 4 and the insulating film 5, and forms the fully depleted transistor FET1.

[0029]

On the other hand, as will be described later in detail, the control circuit 9 inputs the information on the voltage, current, capacitance or resistance value from a dummy element (not shown) for measuring the impurity concentration NA in the semiconductor layer, particularly in the channel region 4, to obtain the optimum value. The back gate voltage value is calculated and a control signal corresponding to it is output.

The variable power supply 10 applies a predetermined back gate voltage to the back gate 11 based on the control signal output from the control circuit 9.

[0030]

Next, a manufacturing process of the semiconductor device shown in FIG. 1 will be described. Here, a silicon substrate is used as the support substrate 2, a silicon oxide film is used as the insulating film 3, and an SOI layer made of silicon is used as the channel region 4 and the source / drain regions 7. As a method of producing such an SOI substrate, a method of bonding two silicon substrates whose one surface is oxidized with their oxide film surfaces in close contact

GF Exhibit 1124 - 1701/2704

with each other by heat treatment at 1000 to 1200 ° C. can be used. Alternatively, a buried oxide film 3 is formed by implanting oxygen ions into a silicon substrate under conditions of an acceleration voltage of 160 keV and a dose amount of about 1.5 to 3.0 × 10 18 atoms / cm 2 and heat treating at 1300 to 1350 ° C. You can also do

[0031]
The semiconductor layer on the insulating film 3 is thinned by polishing, ion etching, or wet etching to form a uniform SOI film having a thickness of 40 nm to 1 μm.

[0032]

Next, as the back gate 11, an impurity added region is formed in the supporting substrate 2 by lithography and ion implantation.

That is, for example, phosphorus (P) or arsenic (As) is applied to the supporting substrate 2 through the insulating film 3 in a region where a MISFET transistor is formed by lithography, an accelerating voltage of 50 to 700 keV, a dose amount of 1 × 10 13 to 1 × 10 16 atom / The back gate 11 can be formed by implanting under the condition of about cm 2. However, the step of forming the back gate 11 may be performed before the formation of the insulating film 3 and the SOI layer 4.

[0033]
Next, ion implantation is performed so that the impurity concentration of the channel region 4 is in the range of 1.times.10@16 cm @ -3 to 1.times.10@19 cm @ -3.

[0034]
After that, the gate oxide film 5 is formed, and further the gate electrode 6 and the insulating film 8 are formed, whereby the main part of the MISFET 1 is completed.

[0035]
In the manufacturing process described above, in particular, in order to set the threshold value in the range of −0.1 to 0.4 V in the fully depleted SOI transistor, the SOI film thickness and impurity concentration of the channel layer 4 are 40 nm to 40 nm, respectively. It is desirable that the thickness is in the range of 1 μm, 3 × 10 16 cm −3 to 3 × 10 17 cm −3.

GF Exhibit 1124 - 1702/2704

[0036]
Next, the optimum range of the SOI film thickness tsi of the channel region 4, the impurity concentration NA, and the back gate voltage VG2 in the semiconductor device of the present invention will be described.

[0037]

FIG. 2 is a graph showing the relationship between the SOI layer and the threshold value of the fully depleted FET obtained by the calculation of the present inventor.

Here, a silicon oxide film having a film thickness of 80 nm is used as the insulating substrate 3, a 1×10 20 cm -3 p-type Si substrate is used as the back gate 11, and 1×10 20 cm -3 n-type polysilicon (polycrystalline silicon) is used as the gate electrode 6. As the gate oxide film 5, an n-type MOSFET having a silicon oxide film of 3 nm was used as a model.

The solid line in FIG. 2 shows the relationship between the film thickness of the channel region 4, that is, the SOI film thickness tsi and the threshold value Vth, when the back gate voltage is 0 V and the impurity concentration of the channel region 4 is 1×10 17 cm -3.

[0038]

In the calculation of the relationship shown in this graph, an equation expressing the threshold value of the fully depleted transistor was used as a reference (“Electrical characterization of Silicon-on-Insulator Materials and Devices” Sorin Cristloveanu and Sheng S.Li, Kluwer Academic. Publishers, (1995)) and the surface quantum effect as a reference (MJvan Dort, PHWoerlee, AJWalker, CAHJuffermans and H.Lifka: IEDM91 p495, (1991)). , (JWSlotboom and HCde Graaff, IEEE trans.

Electron Devices, vol.

ED-24, No.8, pp.1123-1125, (1977)), ("Quantum Mechanics for Device Physics" by David K.

GF Exhibit 1124 - 1703/2704

Ferry, Yosuke Nagaoka et al., Maruzen, (1996)). Considering what is present.

[0039]

As can be seen from FIG. 2, the threshold value of the transistor has a minimum value (arrow in FIG. 2) with respect to the film thickness tsi of the channel region 4. In the vicinity of this minimum value, the amount of change in the threshold value becomes minimum with respect to the change in the film thickness tsi. That is, the threshold sensitivity to the variation in the film thickness of the SOI layer becomes extremely small.

[0040]

Further, by applying the back gate voltage, the electronic state of the surface of the channel region 4 in contact with the insulating film 3 is accumulated (broken line Vth1, ac2 in FIG. 2) or inverted (broken line Vth1, in FIG. 2). The threshold can be changed within the range of inv2). Therefore, the threshold voltage is controlled by applying a predetermined back gate voltage, and the film thickness of the channel region 4 is formed so that the desired threshold value matches the minimum value in FIG. The transistor can set the threshold value sensitivity to the SOI film thickness variation to a minimum at a set value.

[0041]

Next, a method of calculating the SOI threshold value as shown in FIG. 2 will be described in detail. In the following description, the calculation method based on the classical theory model will be described first, and then the calculation method in which the effect of the surface quantization of the channel inversion layer is corrected will be described.

[0042]

First, in a fully depleted transistor to which a back gate voltage can be applied, the threshold value depends on the electronic state on the surface of the channel region 4 in contact with the insulating film 3. The state of the surface of the channel region 4 in contact with the insulating film 3 can be changed from the accumulated state to the inverted state by the back gate voltage.

GF Exhibit 1124 - 1704/2704

[0043]
The relationship between the gate voltage VG1 and the surface potential at this time is expressed by the following equation.

[0044]

Here, Φs1 and Φs2 are the Fermi potentials on the surface in contact with the gate insulating film 5 and the surface in contact with the insulating film 3, respectively, of the channel region 4, and ΦMs1 is the difference in work function from the gate electrode 6 on the gate insulating film 5 side. , QOX1 represents the fixed charge density in the gate insulating film 5, COX1 represents the capacitance of the gate insulating film 5, and Qinv1 represents the inversion layer charge of the channel in the channel region 4.

Qdep1 represents the charge of the depletion layer in the channel region 4, and is represented by −qNAtsi using the electron charge amount q, the impurity concentration NA of the channel region 4, and the film thickness tsi of the channel region 4. The Fermi potential Φp is expressed as Φp = (kT / q) ln (NA / ni) using the intrinsic carrier density ni of silicon, the Boltzmann constant k, the temperature T, and the amount of charge q of electrons, and Csi = E si / tsi (ε si is the dielectric constant of silicon).

[0045]

The threshold value Vth of the fully depleted transistor can be expressed in the following cases depending on the electronic state of the surface of the channel region 4 in contact with the insulating film 3. The surface potential Φsi and the channel inversion layer charge Qinv1 when VG1 = Vth are Φsi = 2ΦF and Qinv1 = 0, respectively, because the gate voltage is the threshold value.

[0046]
When back surface is accumulated, Φs2 = 0

[0047]

GF Exhibit 1124 - 1705/2704

Here, the subscripts "1" and "2" of Vth1 and acc2 represent the states of the surface of the channel region 4 in contact with the gate insulating film 5 and the surface in contact with the insulating film 3, respectively.

In the case of the formula (2), the case where the surface of the channel region 4 in contact with the insulating film 3 is in an accumulated state is shown.

[0048]
When the back surface is inversion, $\Phi s2 = 2\Phi F$

[0049]

When the back surface is depleted, its potential is intermediate between accumulation and inversion, and $\Phi s2$ depends on the back gate voltage VG2.

At this time, if the back gate voltage VG2 when the surface of the channel region 4 in contact with the insulating film 3 is accumulated and inverted is VG2, acc and VG2, inv, respectively, the condition of VG2, acc <VG2 <VG2, inv is satisfied. .. Furthermore, since the capacitance Csi of the channel region 4 and the capacitance COX2 of the insulating film 3 are connected in series, $\Phi s2$ is

[0050]

Is expressed as Therefore, the threshold value is expressed by the following equation.

[0051]
Here, VG2, acc is considered to be symmetrical with respect to the surface of the insulating film 3, and the following is obtained from the condition of $\Phi s1 = 2\Phi F$ and $\Phi s2 = 0$.

[0052]

GF Exhibit 1124 - 1706/2704

FIG. 3 is calculated by the equations (2) to (5) for the case where the impurity concentration NA of the channel region 4 is NA = 1 × 10 17 cm −3, the SOI film thickness tsi = 60 nm, ΦMs1 = −1V, and QOX1 = QOX2 = 0. 6 is a graph showing a relationship between a back gate voltage and a threshold.

In the fully depleted transistor, when the electronic state on the surface of the channel region 4 in contact with the insulating film 3 is inverted or accumulated, the potential Φs2 on the surface becomes constant. Therefore, even if a back gate voltage higher than that is applied, the threshold value becomes a constant value without depending on the back gate voltage. That is, the threshold value of the fully depleted transistor is limited within the range of the threshold value when the electronic state of the surface of the channel region 4 in contact with the insulating film 3 and the threshold value when the electronic state is inverted. ..

[0053]

FIG. 4 shows the SOI film thickness of the channel region 4 of the threshold value calculated using the classical theory model of the equations (2) to (5) when the impurity concentration of the channel region 4 is 1 × 10 17 cm −3. It is the graph which showed the dependency. In the figure, Vth1 and acc2 are shown by broken lines, Vth1 and inv2 are shown by dotted lines, and the threshold for the SOI film thickness at VG2 = 0V is shown by solid lines. Vth1, acc2, Vth1, inv2 are determined by the film thickness of the channel region 4 without depending on VG2. On the other hand, the threshold values of Vth1 and dep12 change depending on the back gate voltage VG2. As can be seen from FIG. 4, Vth1, dep12 in the classical theory model linearly decreases as the SOI film thickness decreases, because the depletion layer charge (−Qdep1) contained in the SOI depletion layer decreases.

[0054]

Next, a case where the surface quantization correction of the channel inversion layer is added to the classical model described above will be described. The threshold change due to such surface quantization correction can be analytically obtained. Here, in the surface quantization correction, the increase amount ΔΨs of the surface band bending of the surface potential and the decrease of the gate capacitance due to the inversion layer capacitance were considered.

GF Exhibit 1124 - 1707/2704

[0055]
The amount of increase in surface band bending due to surface quantization correction of the surface potential is

[0056]

It is represented by.

The surface potential Φs1 when the gate voltage is the threshold value is obtained by adding 2ΦF to this equation.

[0057]
FIG. 5 is a band diagram for explaining the surface quantization correction.

[0058]
As shown in FIG. 5, the equation (6) is a shift Eo-Ec from the conduction band Ec to the lowest energy level Eo, a bandgap narrowing effect ΔEg due to the addition of a high concentration channel impurity, and quantum theory. Of Es Δz of the surface potential due to the shift Δz of the position where the surface charge density is maximum due to the above, and each term is expressed as follows.

[0059]
The shift Eo-Ec to the lowest energy level Eo is

[0060]
Where Es is the surface electric field,

[0062]
The bandgap narrowing effect ΔEg due to the addition of high-concentration channel impurities is

GF Exhibit 1124 - 1708/2704

[0063]
The approximate expression of Es Δz is

[0065]
Further, due to the effective interface quantum effect, the center of the inversion layer charge is separated from the interface between the Si film and the SiO2 film by Δz, so that the gate oxide film capacitance COX1 is COX1 = ε OX / (tOX1 + ε Si / ε OX Δz). expressed.

[0066]

FIG. 2 shows the dependence of the threshold value on the SOI film thickness of the channel region 4 obtained in consideration of the quantum correction as described above.

As can be seen from FIG. 2, when the back gate voltage is kept constant and the film thickness of the channel region 4 is changed, the threshold takes a minimum value (arrow in FIG. 2).

Then, as the thickness of the channel region 4 becomes thinner, the threshold value increases.

This is because the electric field Es at the interface between Si and SiO2 increases when the film thickness of the channel region 4 decreases under the condition that the back gate voltage is constant, so that the energy of the quantum level increases and the surface is inverted. This is because a large gate voltage is required.

[0067]
As described above, it is explained that there is a film thickness of the channel region 4 having the minimum threshold sensitivity with respect to the film thickness variation of the channel region 4 by using the calculation considering the quantum correction.

[0068]

FIG. 6 shows the same FET model as in FIG. 2, in which the SOI film thickness tSi of the channel region 4 and the back gate voltage VG2 to be applied, which has the minimum threshold value in

GF Exhibit 1124 - 1709/2704

FIG. It is the graph shown to the contrary.

Here, the case where the set values of the threshold values are 0.1 V, 0.2 V, and 0.3 V are shown.

[0069]

As can be seen from FIG. 6, the SOI film thickness tSi at which the threshold value is set and the threshold sensitivity to the film thickness variation is minimum has a low dependence on the impurity concentration NA of the channel region 4. It was newly clarified by the detailed study by the present inventor.

That is, the optimum value of the SOI film thickness tSi does not change much with respect to the impurity concentration NA, and takes an almost constant value.

[0070]

Further, it has been found that when the thresholds to be set are different, the SOI film thickness tSi at which the threshold sensitivity to the variation of the SOI film thickness is almost minimum is different.

Here, the relationship between the optimum value of tSi and the threshold value Vth is tSi = 250Vth2−275Vth + 105 (nm), and it can be approximated that Vth is 0 volt or more and 0.5 volt or less.

Therefore, even if Vth is an arbitrary value, the optimum value of tSi can be obtained.

Further, it is newly revealed that the back gate voltage VG2 required for the threshold value to reach the set value increases almost linearly with respect to the impurity concentration NA of the channel region 4.

GF Exhibit 1124 - 1710/2704

[0071]
Therefore, when the SOI film thickness tSi and the impurity concentration NA are determined based on FIG. 6 according to the desired threshold value, even if the impurity concentration NA deviates from a desired value due to, for example, process variations. By measuring the impurity concentration of the channel region 4 and applying the back gate voltage required for the threshold value to have a set value accordingly, the threshold sensitivity to the SOI film thickness is minimized, and A semiconductor device having a set threshold value can be realized.

[0072]
Here, the SOI film thickness at which the threshold sensitivity to film thickness variation is almost the same is almost constant with respect to the impurity concentration NA of the channel region 4 because the quantum mechanical correction term of the equation (6) is tSi. It is strongly dependent and not so dependent on NA, and that Qdep1 of the depletion layer charge in the equation (5) can be almost compensated by changing VG2 even when NA is changed.

[0073]
Due to this feature, of course, even when the concentration distribution of the channel region 4 is not uniform and has a predetermined impurity profile, when Qdep1 / 2COX1 is smaller than 2ΦF in the formula (2), the impurity concentration NA becomes On the other hand, the characteristic that the threshold sensitivity is almost constant is maintained.

[0074]

In the case of a MISFET having a recess gate structure formed by a method such as LOCOS sacrificial oxidation as shown in FIG. 7, the thickness of the channel region 4 is not constant due to the bird's beak at the LOCOS end. In many cases.

That is, the thickness of the channel region is thicker near the source / drain and thinner near the center.

FIG. 8 is a schematic process cross-sectional view showing a manufacturing process of a recess type gate structure by the LOCOS sacrificial oxidation method.

For example, a silicon oxide film 14 having a thickness of about 5 to 100 nm is formed on an SOI

GF Exhibit 1124 - 1711/2704

layer 4 such as silicon having a thickness of 20 nm to 1 μm, and a silicon nitride film having a thickness of, for example, 50 to 200 nm is formed thereon. The antioxidant film 20 is deposited. Next, as shown in FIG. 8A, LOCOS is formed by a thermal oxidation method. Further, as shown in FIG. 8B, the LOCOS oxide film is ion-etched using the antioxidant film 20 as a mask to form a gate formation region. According to this method, the gate electrode can be formed in a self-aligned manner, but since the bird's beak of LOCOS remains in the gate formation region, the SOI film thickness in the channel region tends to be nonuniform as shown in the figure. When the film thickness of the channel region becomes nonuniform in this way, the stability of the threshold value deteriorates, which becomes a problem.

[0075]

On the other hand, according to the present invention, even when the film thickness of the channel is not uniform, for example, in the SOI film thickness of the central portion of the channel, the threshold sensitivity with respect to the film thickness variation with respect to a predetermined threshold value is obtained. A desired threshold value can be stably obtained by setting the SOI film thickness so as to be the minimum. Therefore, the non-uniformity of the SOI film thickness in the vicinity of the center of the channel and the end part thereof falls within, for example, 20% so that the SOI film thickness of the channel region becomes the optimum film thickness as shown in FIG. 2 or 6. Thus, the desired threshold value can be obtained by performing the LOCOS oxidation.

[0076]

Here, the measurement location of the impurity concentration NA of the channel region 4 does not necessarily have to be the channel region 4 of the MISFET itself, and may be a region having the same impurity concentration as the channel region of the MISFET. For example, when manufacturing an integrated device in which a plurality of MISFETs are integrated, the measurement may be performed at any place of the integrated device. Further, when a plurality of integrated devices are formed on a wafer, if the uniformity of the impurity concentration within the wafer is good, the measurement may be performed at any place on the wafer. Furthermore, in a so-called “batch processing” manufacturing process in which multiple such wafers are processed at the same time, if the fluctuation of the impurity concentration for each wafer in the batch is small, measurement is performed on either wafer for each batch. I'm fine.

[0077]

GF Exhibit 1124 - 1712/2704

In this way, by measuring the impurity concentration of the channel region 4 and determining the back gate voltage for setting the threshold value, it is not necessary to change the back gate voltage as long as the transistor is used at this threshold value. .. That is, the control circuit is not necessarily required after the back gate voltage is determined. Therefore, if the impurity concentration of the channel region 4 is measured and the back gate voltage required for the present invention is obtained, it is only necessary to set the variable power supply applied to the back gate so as to output the required voltage.

[0078]

Here, the measurement of the impurity concentration of the channel region 4 is introduced, for example, in a document (“Materials Processing Theory and Practice volume.2-impurity doping processes in silicon” : FFYWang, North Holland Publishing Company (1981)). The measurement method described above may be used. An example of the configuration including the measurement of the impurity concentration is shown below.

[0079]

FIG. 9 is a schematic sectional view showing a second specific example of the semiconductor device of the present invention. In the figure, the same parts as those in FIG. 1 are designated by the same reference numerals, and detailed description thereof will be omitted.

[0080]

In FIG. 9, 4a is a dummy region, 12 is an element isolation region, 13 is a high-concentration semiconductor region, 18 is an electrode region, and 19 is a metal plug. The dummy region 4a is a semiconductor region created under the same conditions as the channel region. The high-concentration semiconductor region 13 is, for example, a semiconductor region doped with a p-type dopant to the solid solution limit.

[0081]

GF Exhibit 1124 - 1713/2704

The back gate 11 is a conductive region formed in the support substrate 2. For example, when the support substrate 2 is p-type Si and the back gate 11 is n-type Si, different voltages are applied to the back gate 11 and the back gate 11. It is desirable to do so. The back gate 11 is formed immediately below the FET for controlling the threshold value, and is not formed below the dummy region 4a for measuring the impurity concentration. This is to prevent the thickness of the depletion layer in the dummy region 4a from changing due to the voltage applied to the back gate 11.

[0082]

Hereinafter, a method for measuring the impurity concentration and the film thickness of the channel region 4 will be described. In FIG. 9, circuits 9 and 9a are control circuits, and the resistance of the high concentration semiconductor region 13 formed at the solid solution limit in the circuit 9a is measured to obtain the SOI film thickness and output to the circuit 9. In the circuit 9, the resistances 18-4a-18 at both ends of the dummy region 4a are measured, and the impurity concentration of the channel region 4 is obtained using the SOI film thickness data input from the circuit 9a. The value of the back gate voltage required to obtain a desired threshold value is obtained from the impurity concentration thus obtained, and is output to the power supply 10.

[0083]

In the configuration example of FIG. 9, a p + type electrode region 18 having the same conductivity as the semiconductor layer is formed so as to contact the dummy region 4a to which the same impurity is added as the channel portion of the transistor FET1. Then, the control circuit 9 measures the resistance between the electrode regions 18 and 18. Here, the resistivity ρ is expressed as $\rho = WtSiR / L$, where R is the resistance, L is the distance between the electrode regions 18, W is the width, and tSi is the SOI film thickness. If the resistivity ρ is obtained in this way, the impurity concentration NA of the channel region 4 can be obtained from, for example, an Irvin curve.

[0084]

On the other hand, the SOI film thickness tSi can be obtained from the high concentration

GF Exhibit 1124 - 1714/2704

semiconductor region 13. That is, as shown in FIG. 9, in the p + type high-concentration semiconductor region 13 in which silicon (B) or the like is doped to a concentration of the solid solution limit, the resistance of the semiconductor region 13 is obtained. The resistivity ρ can be obtained from the resistance of the high-concentration semiconductor region 13, and since the impurity concentration has a value determined by the solid solubility, tSi and NA can be decomposed. Therefore, the film thickness of the semiconductor layer can be obtained by measuring the resistance in the high-concentration semiconductor region 13.

[0085]

The impurity concentration NA in the channel region 4 can be obtained by substituting the SOI film thickness tSi obtained by the above method into the above equation. In this configuration example, the NA measurement area can be formed by the same process as that for forming the MISFET 1.

[0086]

Here, as specific examples of the circuit 9 and the circuit 10, for example, a half-Vdd circuit and a substrate bias circuit can be cited. FIG. 10 is a schematic circuit diagram showing an embodiment using the half-Vdd circuit. VB2 is, for example, a voltage of 0 V, VB1 is, for example, a voltage of VDD, and VB1> VB2. The resistor 18-4-18 in FIG. 10 is the resistance measuring device 18-4-18 formed in the dummy region 4a in FIG. 9, and R1 is the resistance when the dummy region 4a is formed at the set impurity concentration. A resistor having the same resistance value as the value. Further, the transistors Q3 and Q4 are formed wider than Q1 and Q2 to form a current buffer. Furthermore, it is assumed that the conductance of R1 and 18-4-18 is sufficiently smaller than the transconductance of Q1 or Q2. When the impurity concentration fluctuates, the resistance of 18-4-18 changes, so the voltage output by the resistance division also changes, and when the 18-4-18 resistance increases, the output decreases, and 18-4 As the −18 resistance decreases, the voltage at the node Vo increases. The voltage V1 of the node connected to the back gate 11 is determined so that the output node Vo becomes equal to the voltage. Therefore, the back gate voltage can be changed by changing the resistance of the resistance measuring device. Here, the influence of the change in the SOI film thickness tSi can be removed by changing VB1.

[0087]

GF Exhibit 1124 - 1715/2704

11 (a) and 11 (b) are schematic circuit diagrams showing an embodiment of the substrate bias circuit. That is, when the 18-4-18 resistor is provided in the ring oscillator and the impurity concentration of the dummy region 4a changes, the resistance changes, so that the frequency of the ring oscillator changes. Due to this frequency change, the number of excitations of the charge pump circuit changes, the current supplied to the back gate changes, and the back gate voltage can be changed.

[0088]

Next, a manufacturing process of the semiconductor device of FIG. 9 will be described. 12 to 14 are process cross-sectional views showing the main part manufacturing process of the semiconductor device of FIG. First, as shown in FIG. 12, the back gate 11 is formed. Specifically, a resist mask 15 is formed on the SOI wafer, and impurities such as boron are ion-implanted into the supporting substrate 2 such as silicon via the channel region 4 and the insulating film 3. In this way, the p-type back gate 11 having an impurity concentration of, for example, 1×10 17 cm -3 to 1×10 20 cm -3 can be formed.

[0089]

Here, the channel region 4 and the dummy region 4a can be formed by the method described above with reference to FIG. The dummy region 4a is a region for measuring the impurity concentration in the channel region 4. Therefore, it is desirable that the channel region 4 and the channel region 4 are formed under the same conditions in the manufacturing process.

[0090]

Next, the element isolation region 12 is formed as shown in FIG. 13, and gate electrodes 6 and 6a having a gate length L are formed by lithography. Further, insulating films 8 and 8a are formed on the gate electrode.

[0091]

GF Exhibit 1124 - 1716/2704

Next, as shown in FIG. 14, an electrode region is formed. Specifically, the region where the MISFET is formed is masked with a resist mask 15, and, for example, boron is ion-implanted on both sides of the gate electrode 6 at a dose amount of 1013 to 1016 cm-2 to form a p-type electrode region 18. To do.

[0092]

The step of forming the electrode region 18 can be performed simultaneously with the formation of the source / drain of the p-type MISFET. That is, after the step of forming the gate electrode, the p-type electrode region 18 and the source / drain region 7 can be simultaneously formed by using the gate electrode as a mask by ion-implanting boron, for example.

[0093]

Further, a high-concentration semiconductor region 13 in which, for example, boron is ion-implanted to the solid solution limit of the semiconductor layer is formed in a region different from the region where the electrode region 18 is formed (FIG. 14). The high-concentration semiconductor region 13 can be formed at the same time by ion implantation for forming the electrode region 18 and the source / drain region 7 described above. That is, when the region where the gate is not formed is provided and the ion implantation for forming the source / drain regions of the p-type MISFET is performed, for example, by implanting boron to the impurity concentration of the solid solution limit of silicon, the high concentration semiconductor region 13 is formed. Can also be formed.

[0094]

Next, as shown in FIG. 9, the contact 19 to the back gate 11 is formed. Specifically, the metal contact 19 can be formed by forming a contact hole from above the element isolation region 12 by, for example, ion etching, and further depositing an electrode material such as tungsten (W). The step of forming the metal contact 19 can be performed simultaneously with the formation of the metal contact in the resistance measuring region shown in FIG. 9 and the contact (not shown) to the gate / source / drain electrodes. When these contact holes are formed, ion etching is performed using a gas having a large etching selection ratio between the silicon oxide film and silicon, so that regions having different depths of the contact holes can be simultaneously etched. Next, another configuration example for obtaining the SOI film thickness tSi will be described.

GF Exhibit 1124 - 1717/2704

[0095]

FIG. 15 is a schematic cross-sectional view showing a third specific example of the semiconductor device of the present invention. In the configuration shown in the figure, a dummy region 4b is formed separately from the MISFET transistor 1, and a gate electrode 6b and a back gate 11a are provided above and below the dummy region 4b. Then, the capacitance of the capacitance between these electrodes is measured. Here, it is desirable that the back gate 11a be sufficiently doped with impurities, for example, 1018 cm-3 or more, so that surface depletion does not occur in the surface semiconductor layer of the back gate. Further, it is desirable that the dummy region 4b of the electrode 6b and the electrode 11a be completely depleted so that an inversion layer does not occur on the surface thereof.

[0096]

The capacitance Ctotal measured under such conditions is equal to the capacitance of the gate insulating film 5, the dummy region 4b, and the insulating film 3 in series. Therefore, assuming that the dielectric constants of the gate insulating film 5 and the dummy region 4b (that is, the channel region 4) are ε OX and ε Si, and the film thicknesses of the gate insulating film 5, the dummy region 4b, and the insulating film 3 are tOX, tSi, and tbox, respectively. , The capacitance is

[0097]

であらわされる。 Therefore, the film thickness tOX of the gate insulating film 5 and the film thickness tbox of the insulating film 3 are obtained, and if the capacitances of the gate insulating film 5 and the insulating film 3 are known, the film thickness of the dummy region 4b (that is, the channel region 4). It is possible to calculate tSi = ε Si / Ctotal− ε Si (tOX + tbox) / ε OX.

[0098]

Further, tSi can be obtained by using a dummy element formed on the left side of the semiconductor device shown in FIG. 18, which will be described later in detail. That is, in FIG. 18,

GF Exhibit 1124 - 1718/2704

the capacitance Ctotal between the n + layer 16 and the back gate 11b is measured. Here, it is assumed that the voltage source of 10b is applied with a voltage sufficient to form an inversion layer at the interface between the gate insulating film 5b and the SOI layer 4a. Further, under the condition that the back gate side of the dummy region 4a is depleted by applying a sufficient voltage to the back gate, the measured capacitance Ctotal is

[0099]

It is represented by. Therefore, if tbox is known, tSi can be calculated. According to this method, tSi can be accurately calculated even if tox varies.

[0100]

Further, as a method for obtaining the resistivity, a 4-terminal method in which the voltage / current terminals are separated may be used. This method has an advantage that errors due to the contact resistance of the electrodes can be reduced.

[0101]

Next, a method of manufacturing the semiconductor device shown in FIG. 15 will be described. 16 and 17 are schematic process cross-sectional views showing the main part manufacturing process of the semiconductor device of FIG. For example, 1 × 10 18 cm −3 to 1 × 10 20 cm is formed by lithography and ion implantation of boron, for example, into the MISFET and the region of the support substrate 2 made of, for example, silicon that opposes through the insulating film 3 in the region for measuring capacitance. The p-type back gates 11 and 11a having an impurity concentration of −3 are formed (FIG. 16). Here, the channel region 4 and the dummy region 4b can be formed by the manufacturing process as described above with reference to FIG.

[0102]

Next, as shown in FIG. 17, the element isolation region 12 is formed, and the gate insulating film 5 and the gate electrode 6 are further formed. Subsequently, as shown in FIG. 15, the electrode

GF Exhibit 1124 - 1719/2704

region 18 and the source / drain region 7 are formed. These manufacturing methods can be similar to those described above with reference to FIG. Here, in the case of the specific example of FIG. 15, in order to measure the capacitance of the dummy region 4b, the semiconductor layer under the gate electrode 6b may be sufficiently depleted. Therefore, even in the ion implantation for forming the electrode region 18 and the source / drain region 7, the gate electrode 6b plays a role of a mask, and it is not necessary to mask this region with a resist or the like.

[0103]

Next, a fourth specific example of the semiconductor device of the present invention will be described. FIG. 18 is a schematic cross-sectional view showing a fourth specific example of the semiconductor device of the present invention. That is, in the semiconductor device shown in the figure, the impurity concentration can be obtained by the CV measurement method using the dummy element of the MIS capacitor provided separately from the MISFET 1. An insulating film 5b is laminated on the dummy region 4a adjacent to the FET 1 via the element isolation region 12, and, for example, p + type polysilicon (polycrystalline silicon) 6b is further laminated as a MIS capacitor electrode.

[0104]

Further, a voltage source VG2b different from the voltage source used for the MISFET transistor is provided in the back gate 11 formed under the MIS capacitor. The voltage source VG2b may be a fixed power supply to which a voltage is applied so that the electronic state of the surface of the dummy region 4a in contact with the insulating film 3 is accumulated.

[0105]

By using such a MIS capacitor, the impurity concentration of the semiconductor can be obtained by the CV method, and the back gate voltage required to realize the present invention can be determined. The capacitance is measured by applying a fixed gate voltage to the extent that the dummy region 4a is not completely depleted, and using the electrodes of the n + type and p + type semiconductor regions provided near the gate.

[0106]

GF Exhibit 1124 - 1720/2704

Since the capacity at this time is proportional to (NA) 1/2 when the impurity concentration is NA, NA can be obtained from the capacity.

[0107]

FIG. 19 is a schematic circuit diagram showing a specific example of the circuits 9c and 10b.

The circuit shown in the figure is similar to the circuit shown in FIG. 11, for example, and the capacitance C by the MIS capacitor of the dummy element is incorporated in the ring oscillator. When the impurity concentration of the dummy region 4a changes, the capacitance C changes and the frequency of the ring oscillator changes. The back gate voltage can be changed by changing the frequency.

[0108]

Next, a method of manufacturing the semiconductor device of FIG. 18 will be described. 20 and 21 are schematic process cross-sectional views showing the main part manufacturing process of the semiconductor device of FIG. First, as shown in FIG. 20, a back gate 11b different from the MISFET transistor is formed in a region where the MISFET transistor is formed, for example, in an adjacent region. Next, in the same step as the gate step, for example, a gate insulating film 5b made of a silicon oxide film and a gate electrode 6b made of n-type polysilicon are formed, and this forms a MIS capacitor. This may be formed simultaneously with the step of forming the gate of the MISFET 1 (FIG. 20).

[0109]

Next, n + type and p + type semiconductor regions are formed near the gate electrode of the MIS capacitor. Specifically, in the ion implantation for forming the source / drain regions 7 of the n-type MISFET and the p-type MISFET, one side may be implanted into each MIS capacitor region (FIG. 21).

[0110]

GF Exhibit 1124 - 1721/2704

As the impurity concentration measurement using the CV method, there is also a method of obtaining it by a pn junction. FIG. 22 is a schematic cross-sectional view illustrating a semiconductor device provided with a dummy element for measuring an impurity concentration by a pn junction. That is, the n + type silicon region 14 is formed in the surface layer of the dummy region 4a which is adjacent to the FET 1 via the element isolation region 12. Using the pn junction formed in this way, the impurity concentration can be measured by the CV method to determine the back gate voltage required to realize the present invention. Here, a sufficiently large negative voltage VG2a is applied to the back gate 11c that faces the dummy region 4a via the insulating film 3 to bring the electronic state of the surface in contact with the insulating film 3 into an accumulated state.

[0111]

FIG. 23 is a schematic circuit diagram showing a specific example of the circuits 9d and 10b including the dummy element of FIG. The capacitance C in the circuit of FIG. 23 is the capacitance measured at the electrode 6b of FIG. The diode capacitance of the pn junction diode in the dummy region as shown in FIG. 22 changes depending on the fluctuation of the impurity concentration. When the capacitance C changes in this way, the frequency of the ring oscillator changes and can be fed back to the back gate voltage VG2. Here, when the capacity C is small, the pump frequency rises and VG2 rises. Of course, for example, a Schottky junction may be used instead of the pn junction.

[0112]

Next, a fifth specific example of the present invention will be described. FIG. 24 is a schematic sectional view of a semiconductor device according to the fifth example of the present invention. In the present embodiment, fully depleted transistors having two or more different threshold values are provided on the same substrate, and the threshold values of the respective transistors have the minimum threshold sensitivity to the film thickness variation. , And the threshold is set.

[0113]

Note that, in the specific example shown in FIG. 24, for convenience of description, a case where two fully depleted transistors having different film thicknesses and impurity concentrations of

GF Exhibit 1124 - 1722/2704

the channel region 4 are arranged in parallel is shown. However, they are formed on the insulator substrate 3. It does not necessarily have to be adjacent in the direction shown in FIG. 24, the same parts as those in FIG. 1 are designated by the same reference numerals, and detailed description thereof will be omitted.

[0114]

This embodiment includes fully depleted transistors 1A and 1B having at least two different threshold values on the same substrate. More specifically, for example, an SOI layer having a film thickness of about 20 nm to 0.1 μm, for example, a channel region 4A having a film thickness of 80 nm is formed on an insulating film 3 such as a silicon oxide film on a support substrate 2 made of silicon. And a channel region 4B of 60 nm are formed. The respective impurity concentrations are in the range of about $1 \times 10\ 16\ \mathrm{cm}^{-3}$ to $1 \times 10\ 19\ \mathrm{cm}^{-3}$, and for example, they have different impurity concentrations NAA and NAB of $1 \times 10\ 17\ \mathrm{cm}^{-3}$ and $1.6 \times 10\ 17\ \mathrm{cm}^{-3}$, respectively. Back gates 11A and 11B for applying different potentials to the respective MISFETs are formed on the support substrate 2 facing the SOI layer forming the MISFETs 1A and 1B with the insulating film 3 interposed therebetween. Further, control circuits 9A and 9B that set back gate voltages according to the impurity concentrations of the channel regions 4A and 4B are provided, and variable power sources 10A and 10B that are applied to the electrodes 11A and 11B are provided.

[0115]

Now, using the model described above with reference to FIG. 2, as illustrated in FIG. 6, the channel region in which the threshold sensitivity to variations in the SOI film thickness is almost the minimum and the threshold value is the set value. The optimum region of 4, that is, the design value is uniquely determined by the threshold value. That is, when the set threshold value is different, the optimum film thickness of the semiconductor layer for minimizing the sensitivity of the SOI film thickness variation of the threshold value is different.

[0116]

Using the calculation results shown in FIG. 6, when forming a fully depleted transistor in which two threshold voltage variations of 0.1 V and 0.2 V are minimal on the same substrate, the channel region 4 is The film thickness and the impurity concentration cannot be the same in two

GF Exhibit 1124 - 1723/2704

transistors, since it is necessary to form them with the film thicknesses of 80 nm and 60 nm and the impurity concentrations of 1.0 × 10 17 cm −3 and 1.6 × 10 17 cm −3, respectively. That is, by setting the SOI film thickness and the impurity concentration of each transistor to different values, it is possible to realize a transistor in which the threshold value is less likely to vary with variations in the SOI film thickness and the like. If the SOI film thickness is the same as in the conventional case, it is difficult to reduce the threshold sensitivity of each transistor.

[0117]

When the set threshold value of the FET 1A is smaller than the set threshold value of the FET 1B, the SOI film thickness (tsiA) of the FET 1A is large and the impurity concentration is high on the same substrate in order to minimize the threshold sensitivity of each. It is desirable to form the channel region 4A having a low (NAA) and the channel region 4B having a small SOI film thickness (tsiB) and a large impurity concentration (NAB).

[0118]

Further, it is desirable to provide a back gate electrode and a dummy element (not shown) capable of independently setting a potential in each of the plurality of regions having different thicknesses or impurity concentrations of the channel region as described above.

That is, the impurity concentration and the layer thickness of each channel region are measured using these dummy elements, the measurement result is fed back, and a predetermined back gate voltage is applied to each FET, thereby The threshold can be adjusted to the desired value. As the dummy element for this purpose, for example, the one illustrated in FIG. 9, FIG. 15, FIG. 18, or FIG. 22 can be used. Further, as the circuit for measurement and the circuit for applying the back gate voltage, various circuits exemplified in the present specification can be used.

[0119]

Further, this embodiment can be used also when the n-type MISFET and the p-type MISFET are formed on the same substrate. That is, for example, an n-type MISFET may be used as the FET 1A shown in FIG. 24, and a p-type MISFET may be used as the FET 1B. Normally, the work function difference between the gate electrode and the substrate and the charge at the interface of the gate insulating film are different between the n-type MISFET and the p-type MISFET, and therefore the absolute value ¦ VFB ¦ of the flat band voltage is also different. Therefore, even if

GF Exhibit 1124 - 1724/2704

the same threshold value is set, the n-type MISFET and the p-type MISFET also have different SOI film thicknesses for minimizing the threshold sensitivity with respect to variations in the SOI film thickness. That is, as illustrated in FIG. 24, the threshold sensitivity can be kept small by using the optimum SOI film thickness for each of the transistors FET1A and FET1B.

[0120]

Next, a method of manufacturing the semiconductor device of FIG. 24 will be described. FIG. 25 is a schematic process cross-sectional view showing a main part manufacturing process of the semiconductor device of FIG. In forming this structure, as shown in FIG. 25A, the back gates 11A and 11B can be applied to the SOI substrate by lithography and ion implantation, and different potentials can be applied to the respective MISFETs. Form. The SOI layer on the insulating film 3 is thinned by polishing, dry etching, or wet etching, and has a film thickness of, for example, 80 nm and boron (B) ions are implanted to obtain an impurity concentration of, for example, 1×10 17 cm -3. The SOI layer 4 is formed. Next, a resist mask 15 is formed and etching is performed to form a channel region 4B having a film thickness of 60 nm, for example. Subsequently, for example, boron (B) is ion-implanted into the channel region 4B so that the impurity concentration NAB in this region is set to, for example, 1.6×10 17 cm -3.

[0121]

Then, by performing steps after the gate step (not shown), the fully depleted transistors FET1A and FET1B can be formed on the same substrate. Further, a dummy element (not shown) is appropriately formed corresponding to each channel region. Further, circuits 9A and 9B that control the back gate voltage according to the impurity concentration of the SOI layer forming the MISFET are provided, and variable power supplies 10A and 10B that are applied to the back gates 11A and 11B, respectively, are installed to complete the semiconductor device. To do.

[0122]

Next, a sixth specific example of the present invention will be described.

[0123]

FIG. 26 is a schematic sectional view of a semiconductor device according to the sixth example of

GF Exhibit 1124 - 1725/2704

the present invention.

This specific example is characterized in that the FET 1 is formed in the thin SOI layer and the dummy element for measuring the impurity concentration is formed in the thick SOI layer.

[0124]

This dummy element has a pn junction and can measure the impurity concentration using the CV method. The structure and the details of the measuring method can be the same as those described above with reference to FIG. When forming a pn junction in a thin SOI layer, it is not easy to control the junction position, and the p-type layer may be lost due to penetration of phosphorus (P) or arsenic (As) that is ion-implanted. In addition, the depletion layer of the p-type layer may extend to the back gate region and NA may not be measured. On the other hand, according to this example, since the pn junction can be formed in the region where the film thickness of the SOI layer is thick, the formation is much easier and the region of the p-type layer can be secured. There are advantages.

[0125]

The outline of the manufacturing process is as follows. First, for example, an SOI layer made of a p-type silicon layer having a film thickness of 80 nm and an impurity concentration of 1 × 10 17 cm −3 is formed. Next, by patterning and etching, the film thickness of the SOI layer in the portion where the transistor is formed is set to 60 nm, for example. Next, boron (B) or the like is ion-implanted so that the impurity concentration of these SOI layers becomes, for example, 1.6 × 10 17 cm −3. Further, steps after the gate step are performed in the region where the MISFET is formed.

[0126]

Next, as shown in FIG. 27, a pn junction is formed by ion-implanting phosphorus (P), for example, into a region where a dummy element is to be formed. This ion implantation step can also serve as the step of forming the source / drain regions 7 of the n-type MISFET. Here, as a method using the SOI regions having different film thicknesses as illustrated in FIGS. 24 and 26, LOCOS (Local Oxidation of Silicon) sacrificial oxidation may be used. FIG. 28 is a process cross-sectional view

GF Exhibit 1124 - 1726/2704

illustrating a technique of forming an SOI region having a small film thickness by using a recess structure by LOCOS sacrificial oxidation. In this method, first, a silicon oxide film 14 is formed on the SOI layer 4a, and a film 20 made of, for example, a silicon nitride film is deposited on the entire surface thereof. Then, as shown in FIG. 28A, the silicon nitride film 20 is opened in the channel region to be thinned. Then, the SOI layer in the opened region is ion-implanted and heat-treated to obtain a predetermined impurity concentration.

[0127]

Next, as shown in FIG. 28B, the surface layer is thermally oxidized until the film thickness of the SOI layer in the opened region is reduced to a predetermined value. Then, by peeling off the silicon nitride film 20 and the silicon oxide film 14, an SOI region having a small film thickness and a predetermined impurity concentration can be formed. After that, the semiconductor device can be completed by carrying out steps after the gate forming step (not shown).

[0128]

Here, the recess structure by LOCOS sacrificial oxidation has been described for thinning the channel portion of the SOI layer. However, in addition to this, as shown in FIG. 29, the SOI layer in the channel region may be formed by a concave structure in which it is thinned by lithography and etching.

[0129]

Next, a seventh specific example of the present invention will be described. In each of the specific examples described above, in order to have a desired threshold value and reduce the fluctuation of the threshold value due to the process variation, the impurity concentration or the carrier concentration is formed on the same substrate on which the fully depleted transistor is formed. The technique has been described in which the measurement dummy element for measuring the voltage and the control circuit for setting the back gate voltage according to the impurity concentration or the carrier concentration measured by the measurement dummy element are provided. On the other hand, in this example, a semiconductor device provided with a storage element in which the impurity concentration or the carrier concentration is measured in advance by a measurement dummy element and the value is stored is realized.

GF Exhibit 1124 - 1727/2704

[0130]

FIG. 30 is a cross-sectional view of essential parts of a semiconductor device according to this example. In addition, FIG. 31 is a functional block diagram illustrating the relationship between the components in the present specific example. In the figure, the same parts as those in the above-described specific examples are designated by the same reference numerals, and detailed description thereof will be omitted. Also in this specific example, the SOI film thickness and the channel region 4 having the impurity concentration or the carrier concentration (for example, FIG. 6) set so that the threshold sensitivity is reduced with respect to a desired threshold value and the back surface. A fully depleted transistor FET1 consisting of a gate 11 is provided. Further, this specific example has a storage element for storing the information of the impurity concentration or the carrier concentration for setting the back gate voltage applied to the back gate 11. This memory element includes, for example, fuses F1, F2, and F3 formed of wiring layers made of polysilicon, amorphous silicon, aluminum (Al), copper (Cu), platinum silicide (PtSi), titanium silicide (TiSi), or the like. It is characterized by having.

[0131]

32 to 34 are cross-sectional views for explaining the manufacturing process of the semiconductor device of FIG. That is, also in the present specific example, as shown in FIG. 32, the measurement dummy element is provided during the manufacturing process. As shown in FIG. 9, this dummy element measures the impurity concentration or carrier concentration from the resistivity ρ of the SOI layer.

[0132]

Next, as shown in FIG. 33, the impurity concentration or the carrier concentration of the channel region 4 is measured using the measurement dummy element. Then, based on this measured value, the back gate voltage required for a desired threshold value is determined and stored in the storage element. That is, the fuse is blown to create the required back gate voltage. Here, the measurement dummy element does not necessarily have to be formed for each FET 1. For example, the element area can be reduced by forming one measurement dummy element for a plurality of FETs having a common threshold value. More specifically, one measurement dummy element may be provided for a semiconductor device having an integrated circuit in which a plurality of FETs are formed, or one measurement dummy element for a wafer on which a

GF Exhibit 1124 - 1728/2704

plurality of such semiconductor devices are formed. Dummy elements may be provided. Further, when a plurality of these wafers are batch processed, if the variation between the wafers is small, the measurement dummy element may be provided only on any one of the wafers.

[0133]

Once the impurity concentration or the carrier concentration of the channel region 4 is measured and the required back gate voltage is determined based on the relationship shown in FIG. 6, the measurement dummy element becomes unnecessary. Therefore, as shown in FIG. 34, the FET 1 and the measurement dummy element can be separated in a dicing process for chip formation, for example.

[0134]

According to this example, it is not necessary to form a circuit for measuring the impurity concentration or the carrier concentration on the finally obtained chip, and it suffices to store the circuit in a memory element having a much smaller size. Therefore, high integration and reduction in chip area can be achieved. Further, since the impurity concentration or carrier concentration measuring circuit is unnecessary, it is possible to further reduce power consumption.

[0135]

Here, the measurement of the impurity concentration or the carrier concentration in the channel region is not limited to the measurement dummy element shown in FIG. 32, and any method described in each of the above-described specific examples can be used as well.

[0136]

In addition, this specific example can be applied to a semiconductor device in which a plurality of different FETs as illustrated in FIG. 24 are formed.

That is, when a plurality of types of MISFETs having different layer thicknesses and impurity concentrations of the channel region are formed, a storage element is provided for each type of

GF Exhibit 1124 - 1729/2704

FET, and the measurement result of the dummy element is fed back and optimized. It is possible to apply various back gate voltages.

[0137]
Next, a specific configuration of the bias circuit used in this example is illustrated.

[0138]
35 to 40 show a configuration example of a bias circuit including a memory element that can be used in this example.

[0139]
In FIG. 35, the range in which the impurity concentration or the carrier concentration varies in the channel region 4 is predicted in advance, and the optimum back gate voltage corresponding to each predicted value is set as, for example, VG1, VG2, VG3, This is an example in which the fuse of the memory element is blown accordingly.

[0140]

This will be specifically described with reference to the graph of the relationship between the SOI film thickness and the impurity concentration in FIG.

First, the desired threshold value is set to 0.2 V, and the impurity concentration varies within the range of 1.2 × 10 17 cm −3 to 1.8 × 10 17 cm −3, for example.

At this time, for example, -1, 0, 1V are provided as VG1, VG2, and VG3 as the power supply for the back gate voltage.

Next, the impurity concentration of the channel region 4 is measured using a dummy element, and when the measured value is 1.2 × 10 17 cm −3 to 1.4 × 10 17 cm −3, the memory element F1 is not cut., F2 and F3 are cut off to apply VG1 = -1V as a back gate voltage. When the measured value is 1.4.times.10@17 cm @ -3 to 1.6.times.10@17 cm @ -3, F2 is not cut and F1 and F3 are cut to apply VG2 = 0V as the back gate voltage. Further, when the measured value is 1.6 × 10 17 cm −3 to 1.8 × 10 17 cm −3, F3 is not cut and F1 and F2 are cut so that VG3 =

GF Exhibit 1124 - 1730/2704

1V is applied as the back gate voltage. Cut each fuse. By doing so, it is possible to apply a back gate voltage within a desired range based on the measured value, and a threshold value close to the desired threshold value can be obtained.

[0141]

FIG. 36 shows an example in which the power supplies VG1 to VG3 in FIG. 35 are replaced with a step-up / down circuit. This is convenient in that it can appropriately step up or step down to a predetermined back gate voltage based on the conventionally used power supply voltage.

[0142]

FIG. 37 shows an example in which the voltage is appropriately divided within the voltage range of Vcc to Vss from Vcc = 3V which is the power supply voltage to Vss = 0V and used as the back gate voltage. For example, a resistor composed of a resistor R is connected in series, and a fuse is wired so that a voltage can be extracted at each terminal. When the back gate voltage is applied, for example, the fuse F2 is not cut, F1 and F3 are cut to 2/3 Vcc, and F3 is not cut and F1 and F2 are cut to 1/3 Vcc. By disconnecting all fuses, the voltage of Vcc can be applied to the back gate. Although three resistors are provided in FIG. 37, a plurality of resistors may be provided, and if more resistors are provided, the voltage is divided more finely and a value close to a desired threshold value is obtained. You can The range of voltage is not limited to the range of Vcc to Vss, and it is possible to change the range by using a step-up / down circuit.

[0143]
FIG. 38 is a modification of FIG. 37, and is a circuit example in which the voltage range from Vcc to Vss can be divided by using n cells each including two resistors and one fuse. ..

[0144]

Further, as shown in FIG. 37, in addition to directly applying the output of the resistor to the substrate bias node, as shown in FIG. 39, the resistor output may be connected to a variable power source whose output voltage changes according to the control input. ..

GF Exhibit 1124 - 1731/2704

By doing so, there is an advantage that a large substrate bias output current can be obtained even if the current flowing through the resistor is reduced.

[0145]

Further, as shown in FIG. 40, a plurality of charge pump circuits may be connected in series and the substrate bias voltage may be switched depending on the states of the fuses F1 to F3 of the memory element. Assuming that the threshold value of the transistor is Vt, the open circuit voltage of the substrate bias power supply output is -3Vcc + 4Vt when F1, F2 and F3 are not disconnected, and -2Vcc + 4Vt and F1 are not connected when F1 and F2 are disconnected. An output of -Vcc + 4Vt can be obtained at the time of disconnection, F2 and F3 disconnection.

[0146]

As the memory element used in this example, in addition to the method of cutting the fuse as described above, for example, a method of accumulating charges in the floating gate electrode, a method of polarizing and storing a ferroelectric substance, and Alternatively, a so-called antifuse may be used, which is a method of storing data by dielectric breakdown of a thin semiconductor or an insulator sandwiched between a metal or a silicide.

[0147]

The embodiments of the present invention have been described above by exemplifying specific examples.

However, the present invention is not limited to the above specific examples.

[0148]

For example, as an insulating film forming method, an oxide film forming method by thermal oxidation, a method of forming an oxide film into which oxygen is injected with low acceleration energy of about 30 keV, a method of depositing a silicon oxide film, A method of depositing a silicon nitride film or a method of combining these may be used. Further, a method other than these methods for converting silicon into a silicon oxide film or a silicon nitride film, for example,

GF Exhibit 1124 - 1732/2704

a method of implanting oxygen ions into deposited silicon or a method of oxidizing deposited silicon may be used. In addition, a silicon nitride film or other tantalum oxide film, a titanium oxide film, a ferroelectric film such as strontium titanate or barium titanate, or lead zirconium titanate, a single-layer film of a paraelectric film, or a film thereof Composite membranes can also be used.

[0149]
Further, although not particularly mentioned in the above-mentioned specific examples, as the element isolation, element isolation of trench isolation, LOCOS element isolation film, recessed type (Recessed) LOCOS, improved LOCOS method, or field shield isolation is used. Or a combination of these.

[0150]

Furthermore, although p-type Si is used for the SOI layer in each of the above-described specific examples, n-type Si, GaAs, or InP may be used instead.

Further, it may be applied to a p-type MISFET instead of the n-type MISFET. In that case, the n-type in the above-described embodiment is read as p-type and the p-type is read as n-type, and the doping impurity species As, P and Sb are used. Etc. may be read as either In, B or the like, and As, P, Sb may be read as any of In, B, BF2 in the case of ion implantation.

[0151]

Further, the gate electrode is made of single crystal silicon other than polycrystalline silicon, porous silicon, amorphous silicon, SiGe mixed crystal, SiC mixed crystal, GaAs, W, Ta, Ti, Hf, Co, Pt, Pd metal. Alternatively, silicide can be used. Further, a laminated structure of these may be used.

[0152]
In addition, various modifications can be made without departing from the spirit of the present invention.

GF Exhibit 1124 - 1733/2704

[0153]
The present invention is carried out in the form described above, and has the following effects.

[0154]
First, according to the present invention, the threshold value can be set to a desired value while keeping the threshold sensitivity to the variation of the SOI film thickness and the impurity concentration, which is a problem in the fully depleted transistor, at a minimum. Is.

[0155]
Further, according to the present invention, for example, when an integrated circuit is formed, the variation of the impurity concentration is corrected, and the threshold sensitivity to the variation of the SOI film thickness is smaller than that of the conventional example. Can be accumulated.

[0156]

On the other hand, in the MOS logic circuit, when the threshold value of the transistor is high, the current driving capability is low and the delay time is long, while when the threshold value is low, the subthreshold leak current when off is large.

Therefore, according to the present invention, variations in delay time and power consumption can be kept small.

[0157]

Further, the delay time is proportional to (VDD-Vth) - α (α is a positive number of 1 or more), where VDD is the power supply voltage, with respect to the threshold value Vth.

Therefore, the delay time can be reduced by the variation of Vth, and the low voltage operation can be performed even if the delay time is the same.

Therefore, by operating at a low voltage, the reliability of the gate insulating film with respect to

GF Exhibit 1124 - 1734/2704

the power supply voltage can be further improved, and the power consumption for gate charge / discharge can be reduced.

[0158]
Further, according to the present invention, even when the recess gate structure is formed by LOCOS sacrificial oxidation, the SOI film thickness is set so that the threshold sensitivity becomes minimum with respect to the variation of the SOI film thickness at a desired threshold value. By doing so, the fluctuation of the threshold value near the SOI film thickness is minimized, so that a desired threshold value can be obtained.

[0159]

Further, since the variation in the threshold value between the pair transistors can be further suppressed, for example, a current mirror circuit or a cross-coupled sense amplifier can be realized more accurately and symmetrically, and the accuracy of the current source and the sensitivity of the sense amplifier can be improved. Can be increased.

Further, according to the present invention, in a semiconductor circuit in which MISFETs having two or more threshold values are integrated, the threshold sensitivity to variations in SOI film thickness can be minimized for each element.

This is because even in the CMOS circuit, in the fully depleted MISFET formed with the SOI film thickness corresponding to the desired threshold value of the n-type MISFET and the p-type MISFET, the threshold caused by the SOI film thickness variation in each MISFET. Value sensitivity is minimal. This is difficult for the conventional FD-SOIMISFET having a single SOI film thickness. Therefore, in a logic circuit using a transistor having a plurality of threshold values or a CMOS circuit, even if the SOI film thickness varies, the threshold sensitivity can be kept to a minimum at each desired threshold value. Further, according to the present invention, the back gate voltage control circuit according to the impurity concentration can be formed on the same substrate by applying a half-Vdd circuit or a substrate bias circuit.

[0160]

Further, in the present invention, the method of obtaining the impurity concentration of the

GF Exhibit 1124 - 1735/2704

semiconductor layer forming the MISFET by measuring the resistance can be performed at a low voltage by the method of measuring the capacitance of the capacitance, and the applied voltage due to the breakdown voltage of the gate oxide film can be changed. It has the advantage that there are no limits. On the other hand, the method of obtaining the impurity concentration by measuring the capacitance of the capacitance has the advantages that the sensitivity is higher than the method of measuring the resistance and the power consumption can be reduced.

[0161]
Further, when manufacturing the dummy element of the present invention, the gate used for the MISFET can be used as it is, so that the dummy element for measuring the impurity concentration can be formed on the same substrate by the number of steps of the conventional semiconductor device. ..

[0162]

Further, according to the present invention, a dummy element for measuring the impurity concentration of a semiconductor layer having a thin SOI film thickness is formed in a semiconductor layer region having a large SOI film thickness to form a pn junction of the dummy element. The film thickness margin can be secured.

Then, for example, when the n-type layer is formed in the p-type semiconductor layer by ion implantation to form the pn junction region, the lithography process is performed at the same time as the ion implantation for forming the source / drain electrode region in the n-type MISFET. Up to this, it is possible to form a pn junction region.

[0163]
As described above, according to the present invention, in a semiconductor device having a fully depleted transistor, a desired threshold value is maintained while the threshold sensitivity to variations in SOI film thickness and impurity concentration is kept at a minimum. The industrial advantages are enormous.

GF Exhibit 1124 - 1736/2704

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

CLAIMS JPH11330482

1.
A support substrate having a back gate formed thereon, an insulating film provided on the support substrate, a first semiconductor layer provided on the insulating film, and the support substrate facing the back gate. A MISFET transistor using a part of the first semiconductor layer as a channel region, a dummy element that outputs a measurement signal that changes according to the impurity concentration or the carrier concentration of the first semiconductor layer, and the dummy element that outputs the measurement signal. A semiconductor device comprising: a voltage applying unit that applies a voltage to the back gate according to the measurement signal.

2.
A supporting substrate formed with first and second back gates, an insulating film provided on the supporting substrate, and a first semiconductor layer having a first film thickness provided on the insulating film, The first MISFET transistor having a part of the first semiconductor layer as a channel region facing the first back gate of the supporting substrate and the first film thickness provided on the insulating film are A second semiconductor layer having a different second film thickness; a second MISFET transistor facing the second back gate of the support substrate and having a part of the second semiconductor layer as a channel region; A semiconductor device comprising: a voltage applying unit that applies a voltage to the first back gate independently of a voltage of the second back gate.

3.
A support substrate having a back gate formed thereon, an insulating film provided on the

GF Exhibit 1124 - 1737/2704

support substrate, a first semiconductor layer provided on the insulating film, and the support substrate facing the back gate of the support substrate. A MISFET transistor using a part of the first semiconductor layer as a channel region, a storage element that stores information corresponding to a voltage applied to the back gate, and the back gate based on the information stored in the storage element A semiconductor device comprising: a voltage applying unit that applies a voltage to the.

4.

A supporting substrate having first and second back gates formed thereon, an insulating film provided on the supporting substrate, and a first semiconductor layer having a first film thickness provided on the insulating film, Information corresponding to a first MISFET transistor in which a part of the first semiconductor layer is a channel region facing the first back gate of the support substrate and information corresponding to a voltage applied to the first back gate is provided. A first memory element for storing, a second semiconductor layer provided on the insulating film and having a second film thickness different from the first film thickness, and a second back gate of the support substrate. A second MISFET transistor, which opposes and uses a part of the second semiconductor layer as a channel region, and a voltage of the second back gate are independent of the information stored in the first storage element. And a voltage applying unit that applies a voltage to the first back gate based on the semiconductor device.

5.

The semiconductor device according to claim 3, wherein the storage element stores information according to an impurity concentration or a carrier concentration of the first semiconductor layer.

6.

The semiconductor device according to claim 1, wherein the MISFET transistor is a fully depleted transistor in which the channel region is completely depleted.

GF Exhibit 1124 - 1738/2704

⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　昭62－61363

⑤1Int.Cl.⁴	識別記号	庁内整理番号	⑬公開　昭和62年(1987)3月18日
H 01 L 29/78 29/20 29/62		8422－5F	

審査請求　未請求　発明の数 1　（全12頁）

⑤4発明の名称　半導体装置

⑳特　願　昭60－199406

㉒出　願　昭60(1985)9月11日

⑦2発明者　梅本　康成　国分寺市東恋ケ窪1丁目280番地　株式会社日立製作所中央研究所内

⑦2発明者　松岡　直之　国分寺市東恋ケ窪1丁目280番地　株式会社日立製作所中央研究所内

⑦2発明者　高谷　信一郎　国分寺市東恋ケ窪1丁目280番地　株式会社日立製作所中央研究所内

⑦2発明者　重田　淳二　国分寺市東恋ケ窪1丁目280番地　株式会社日立製作所中央研究所内

⑦1出願人　株式会社日立製作所　東京都千代田区神田駿河台4丁目6番地

⑦4代理人　弁理士　小川　勝男　外1名

最終頁に続く

明　細　書

発明の名称　半導体装置

特許請求の範囲

1．第1の導電性を有するIII－V族の第1の半導体領域上に界面準位層とこの界面準位層上に単結晶又は多結晶Siよりなる第2の半導体層とを少なくとも有する制御手段と、該制御手段をはさんで設けられたキヤリアの送受手段とを少なくとも有し、前記界面準位層は前記第2の半導体層が有するフエルミ・レベルを当該界面準位層のフエルミ・レベルにピンニングせしめて成ることを特徴とする半導体装置。

2．前記界面準位層は前記第1の半導体層のエネルギー・ギヤツプに当たる位置に10^{12}／cm／eV以上の界面準位を持つことを特徴とする特許請求の範囲第1項記載の半導体装置。

3．前記界面準位層の厚さは30Å以下になることを特徴とする特許請求の範囲第1項又は第2項記載の半導体装置。

4．前記第2の半導体層は縮退した半導体より成ることを特徴とする特許請求の範囲第1項～第3項のいずれかに記載の半導体装置。

5．エネルギー・バンド・ギヤツプの大きさが前記第1の半導体層の少数キヤリアの存在する界面におけるエネルギー・バンドの端と前記第2の半導体層の多数キヤリアの存在するエネルギー・バンドの端との差よりも大きく、且前記第1の半導体層と同一の導電性を有し、前記制御手段と前記キヤリアの送受手段との間の半導体層の導電性は前記第1の半導体層の導電性とは逆なることを特徴とする特許請求の範囲第1項～第4項のいずれかに記載の半導体装置。

6．エネルギー・バンド・ギヤツプの大きさが前記第1の半導体層の多数キヤリアの存在する界面におけるエネルギー・バンドの端と前記第2の半導体層の多数キヤリアの存在するエネルギー・バンドの端との差よりも大きく、且前記第1の半導体層と逆の導電性を有し、前記制御手段と前記キヤリアの送受手段との間の半導体層の導電性は前記第5項と同一であることを特徴

GF Exhibit 1124 - 1739/2704

とする特許請求の範囲第１項～第４項のいずれかに記載の半導体装置。

発明の詳細な説明

〔発明の利用分野〕

本発明は、高速の電界効果トランジスタに関するものである。

〔発明の背景〕

GaAsやＩｎＰ等の化合物半導体基板を用いたMISFET（Metal Insulator Field Effect Transistor）の断面図を第１図（ａ）に示す。ここで、１はｐ－GaAs基板、２はｎ－GaAs層、３は絶縁膜、４は界面準位層、５はゲート電極、６はソース電極、７はドレイン電極である。絶縁膜３の厚さは、1000～3000Åの間にとるのが通例である。このようなMISFETは、反転型の動作をさせることができるデバイスである。すなわち、ゲート電極５に正の電圧を印加すると、絶縁膜３とｐ－GaAs基板１の界面に電子の反転層８が形成される。反転転層をチヤンネルに用いるため、MISFETは大電流がとれ高速デバイスとしての可能性をもつている。しかし、実際には第１図（ｂ）のバンド構造図に示すように絶縁膜３とｐ－GaAs基板１の界面には、半導体のエネルギー・ギヤップ中央付近に10^{12}～10^{13}／㎠／ｅＶ台の極めて高密度の界面準位の存在する層４（以降、この層を界面準位層４と呼ぶ）が１０～３０Åの厚さで存在することが知られている。特に、化合物半導体では、これを10^{14}㎝$^{-2}$／ｅＶ以下に抑えることは、極めて困難である（例えば、GaAsにおいては、空気中にさらしたり、不純物汚染することにより、酸素原子や金属原子が表面に一層付着したのみで界面準位層が10^{12}㎝$^{-2}$／ｅＶ以上生ずることが知られている。）。このため、従来のMISFETは界面準位のフエルミレベルϕ_{ss}が半導体のフエルミレベルϕ_sに固定される傾向が強く、ゲート電極に正電圧を印加しても表面電位ϕ_sが変動せず反転層が形成され難いという欠点をもつていた。

このように、従来からあるMISFETでは反転層をチヤンネルとして用いることは困難であり、電流を多くとれない。これは高密度の界面準位層が存在し、その界面準位のフエルミレベルが半導体のフエルミレベルに固定される傾向が強いためである。以上説明した如きＭＩＳトランジスターの例はたとえばソリツドーステート　エレクトロニクス〔Solid－State Electronics〕vol．１７，pp７５１～７５９（1974）にみられる。

〔発明の目的〕

本発明の目的は大電流を流すことのできる高速の電界効果トランジスタを提供することにある。

〔発明の概要〕

前述のように、従来からあるMISFETでは界面準位のフエルミレベルが半導体のフエルミレベルに固定される傾向が強い。これは、物理的には、界面準位への半導体側からの電子の充放電時間が、他の領域（例えば、ゲート金属）からの充放電時間よりも短いために、準熱平衡状態が界面準位と半導体との間に成立するからである。

より定量的に記せば、界面準位への半導体側からの電子の充放電時間t_eは、例えば半導体がｎ－GaAsの場合に、１０nsec～１０msecの範囲にあり、より一般に、Ⅲ－Ⅴ族の化合物半導体においても、上記充放電時間は、１０nsec～１０msecの間におさまることが知られている。

一方、ゲート金属からの界面準位への電子の充放電時間t_eは、

$$t_e=\frac{D_{it}\cdot\Delta\phi_{ss}}{v_{th}\cdot N\cdot T_t} \quad \cdots(1)$$

$$T_t=\exp\left[-a\cdot\phi^{1/2}\cdot\left(\frac{m}{m_0}\right)^{1/2}\right] \quad \cdots(2)$$

となる。

但し、

D_{it}：界面準位層４の界面準位密度（㎝$^{-2}$／ｅＶ）

$\Delta\phi_{ss}$：電子の充放電に伴う界面準位のフエルミレベルϕ_{ss}の移動量（ｅＶ）

v_{th}：ゲート金属５中の自由電子の速度（㎝／sec）

Ｎ　：ゲート金属５中の自由電子濃度（㎝$^{-3}$）

T_t：絶縁膜３をトンネルする確率（但し、簡単のためここでは矩形のポテンシヤ

GF Exhibit 1124 - 1740/2704

ル障壁をトンネルすると仮定した。）

d　：絶縁膜3の厚さ（Å）

φ　：電子がトンネルする絶縁膜3による障壁の高さ（eV）

m　：絶縁膜3中の電子の有効質量（g）

m_0：真空中の電子の質量（g）

である。$D_s \cdot \Delta\phi_s \fallingdotseq 10^{12}\,cm^{-2}$，$v_{th} \fallingdotseq 10^7$ cm／sec，$N \fallingdotseq 10^{22}\,cm^{-3}$，$\phi \fallingdotseq 4$ eV，$m/m_0 \fallingdotseq 0.2$，$d \fallingdotseq 1000$Å（上に列挙した値は、通常のMIS構造の典型値である。）とすれば、

$$\tau_s \fallingdotseq 10^{365}\,sec$$

となり、$\tau_i \ll \tau_s$となることがわかる。このため、準熱平衡状態は、界面準位と半導体の間に成立することとなり、界面準位のフエルミレベルは、半導体のフエルミレベルに固定されることになる。

したがつて、上述のことからわかるように、界面準位のフエルミレベルをゲート金属のフエルミレベルに固定させるには、$\tau_i \gg \tau_s$となるように、ゲート構造を構成すればよい。

本発明は、上記のゲート構造を実現するために、基本的に次の如き構成を有する。

第1の導電性を有するIII－V族半導体領域上に界面準位層とこの界面準位層上に単結晶あるいは多結晶Si層（以下、Si層と記す）とを少なくとも有する制御手段と、該制御手段をはさんで設けられたキヤリアの送受手段とを少なくとも有し、前記界面準位層は前記Si層が有するフエルミ・レベルを当該界面準位層のフエルミ・レベルにピンニングせしめて成る。

前記界面準位層は前記III－V族の半導体層のエネルギー・ギヤツプに当たる位置に10^{13}／cm／eV以上の界面準位を持つのが良い。又その厚さは30Å以下であることが好ましい。

このような界面準位層は、III－V族の半導体とSiの格子定数の不整合、Siの成長時、あるいは被着時の高温プロセスによるストイキオメトリのずれ、空気や水にさらすこと、あるいはSiの成長，被着時に成長，被着容器中残存する酸素により形成されるIII－V族の半導体とSiの界面に生ずるIII－V族の半導体あるいはSiの酸化物（自然酸化膜）等の絶縁物、界面に残存する微量な金属による汚染等により容易に導入することができる。また、このような界面準位層はより積極的には、プラズマ酸化法や陽極酸化法等の手段で形成することも出来る。

Si層としては縮退したものを用いるのが通例であるが、その条件はたとえばダブリユ・ショツクレー〔W. Shockley〕“エレクトロン・アンド・ホールズ・イン・セミコンダクター〔Electrons and Holes in Semiconductors〕” ディー・フアン・ノストランド・プリンストン・エヌ・ジエー〔D. Fan Nostrand. Princeton. N. J.〕，1950等に知られているものを用いれば良い。半導体の縮退条件は現実には不純物濃度によつて制御する。その条件を例示すれば第1表の如きである。

第　1　表

	Si
n導電型	4.2以上
p導電型	1.5以上

（単位×$10^{20}\,cm^{-3}$，室温）

（前記文献により、縮退条件をn導電型に対しては、$E_f - E_c \geqq kT$，p導電型に対しては$E_v - E_f \geqq kT$として計算した。但し、E_fは半導体のフエルミレベル、E_cは伝導帯端のエネルギー、E_vは価電子帯端のエネルギー、kはボルツマン定数、Tは絶対温度である。）

Si層の厚さは、少なくとも50Å以上であればよく、必要に応じて、50～5000Åの範囲を選択する。

更に具体的半導体装置の構成として次の2つの型が考えられる。

(1) Si層は、そのエネルギー・バンドギヤツプの大きさがIII－V族の半導体層の少数キヤリアの存在する界面におけるエネルギーバンドの端とSi層の多数キヤリアの存在するエネルギーバンドの端との差よりも大きく、III－V族の半導体層と同一の導電性を有し、ゲートとソースあるいはドレインの間の半導体層の導電性はIII－V族の半導体層の導電性とは逆となす。この構成によれば、反転層の形成が容易で、大電

GF Exhibit 1124 - 1741/2704

流を流すことを可能とする。

(2)Si層は、そのエネルギー・バンドギャップの大きさがIII－V族の半導体層の多数キャリアの存在する界面におけるエネルギーバンドの端とSi層の多数キャリアの存在するエネルギーバンドの端との差よりも大きく、III－V族の半導体層と逆の導電性を有し、ゲートとソースあるいはドレインとの間の半導体層の導電性はIII－V族の半導体層の導電性と同一となす。この構成によれば、薄積層の形成が容易で、大電流を流すことを可能とする。

以下、各々について説明する。

(1) 第1の型

本発明による縮退したSi層／界面準位層／III－V族半導体の三層構造を持つ電界効果トランジスタの第1の型のものの断面を第2図(a)に示す。この三層構造のバンド構造を第2図(b)に示す。9は、半絶縁性半導体基板、10はn型半導体層、11はIII－V族のp型半導体層、12は界面準位層、13は縮退したp型Si層（ゲート）、14はソース電極、15はドレイン電極である。9は、必ずしも半絶縁性半導体基板に限らず、11と同じp型導電性を有する半導体基板であってもよい。縮退したSi13がゲートをなしており、界面準位層12の厚さは30Å以下、界面準位の密度は10^{12}／cm／eV以上である。また、縮退したSi層13とIII－V族の半導体11との間には、$E_g \geqq V_{t1}$ の関係がある。ここで、E_g は縮退したSi層13のエネルギーバンドギャップであり、V_{t1}は、縮退したSi層13の価電子帯端E_{v0}とIII－V族の半導体11の伝導帯端E_nとのエネルギー差である。

Siのエネルギーギャップは、室温で1.1eVであることが知られており、また、III－V族半導体の場合、その半導体のエネルギーギャップE_g'のおよそ2／3だけ、伝導帯端から離れた位置に界面のフェルミレベルがあることは周知の事実である。すなわち、$V_{t1}=\frac{2}{3}E_g'$ である。したがって、

$$E_g \geqq \frac{2}{3}E_g'$$

なる関係を満たすIII－V族半導体は、上記III－V族半導体11に適用できる。例えば、GaAsのエネルギーギャップはE_g'＝1.4eVであり、上式を満足する。

縮退したSi層13は第2図(b)に示すように直接界面準位層12と接触しており、かつ、正孔濃度が$10^{20}cm^{-3}$以上と高いので、界面準位への正孔の充放電時間は縮退したSiからのものが最も短い。その理由は、以下に述べる通りである。

縮退したSi層からの界面準位への電子の充放電時間τ_nは、式(1)，(2)と類似の形式に表現できて、

$$\tau_n=\frac{D_t\cdot\Delta\phi_{nn}}{v_{t1}\cdot N\cdot T_t} \quad \cdots(3)$$

$$T_t=\exp\left[-d_1\cdot\phi_1^{1/2}\left(\frac{m_1}{m_0}\right)^{1/2}-d_2\cdot\phi_2^{1/2}\left(\frac{m_2}{m_0}\right)^{1/2}\right] \quad \cdots(4)$$

$$d_1=\sqrt{2\varepsilon_1\left(\phi_1+\frac{kT}{q}\ell_n(N/N_{v1})\right)/qN\times10^8} \quad \cdots(5)$$

となる。但し、

D_t ：界面準位層12の界面準位密度（cm^{-2}／eV）

$\Delta\phi_{nn}$：電子の充放電に伴う界面準位のフェルミレベルϕ_{nn}の移動量（eV）

V_{t1}：縮退したSi層13中の自由正孔の速度（cm／sec）

N ：縮退したSi層13中の自由正孔の濃度（cm^{-3}）

T_t ：縮退したSi層13中に生ずる空乏層17及び、界面準位層12をトンネルする確率。（但し、ここでも簡単のため矩形のポテンシャル障壁をトンネルすると仮定した。）

d_1 ：空乏層17の厚さ（Å）

ϕ_1 ：正孔がトンネルする空乏層17による障壁の高さ（eV）

m_1 ：縮退したSi層13中の正孔の有効質量（g）

m_0 ：真空中の電子の質量（g）

GF Exhibit 1124 - 1742/2704

d_2 ：界面準化層１２の厚さ（Å）

ϕ_2 ：正孔がトンネルする界面準位層１２による障壁の高さ（ｅＶ）

m_2 ：界面準位層１２中の正孔の有効質量（ｇ）

ε_1 ：縮退したＳｉ層１３の誘電率（Ｆ／ｃｍ）

ｋ　：ボルツマン定数（ｅｎｇ／Ｋ）

ｑ　：電子の電荷（ｃ）

Ｔ　：絶対温度（Ｋ）

N_{v1}：縮退したＳｉ層１３の価電子帯の有効状態密度（cm^{-3}）

である。

Ｄ．$\Delta\phi_{s1} \fallingdotseq 10^{12}cm^{-2}$，$v_{th} \fallingdotseq 10^{7}$ｃｍ／ｓｅｃ，$\phi_1 \fallingdotseq 0.45$ｅＶ，$m_1 \fallingdotseq 0.2m_0$，$d_2 \fallingdotseq 10$Å，$\phi_2 \fallingdotseq 1$ｅＶ，$m_2 \fallingdotseq 0.2m_0$，$\varepsilon_1 = 11.9\varepsilon_0$（$\varepsilon_0$ は真空の誘電率：0.885×10^{-13}Ｆ／ｃｍ），Ｔ＝３００Ｋ，$N_{v1} \fallingdotseq 10^{19}cm^{-3}$と仮定すれば、縮退したＳｉ層１３の正孔濃度を$N = 10^{20}cm^{-3}$とおくと、

$d_1 = 26$Å

$\tau_n = 200$ｐｓ

となる。したがつて、半導体層１１からの充放電時間τ_r（＝１０ｎｓｃｅ～１０ｍｓｃｅ）に比べ、τ_nは、十分短い。

したがつて、縮退したＳｉ層１３と界面準位とは準熱平衡状態を達成し、界面準位のフエルミレベルϕ_{fs}は、縮退したＳｉ層のフエルミレベルϕ_nに固定される。このため、ゲートに正電圧を印加すると、表面電位ϕ_sがそれに伴い変動する。

一方、縮退したＳｉ層１３とⅢ－Ⅴ族の半導体１１との間には、$E_g \geqq V_{bi}$の関係があるので、Ⅲ－Ⅴ族の半導体１１の伝導帯の電子にとつてゲート側にバリアが存在することになる。

以上述べたように、本発明によるＦＥＴのゲート構造は、表面電位ϕ_sをゲート電圧とともに変動させることができ、しかも伝導帯の電子にとつてゲート側の界面にバリアが存在する。そのため、容易に電子の反転層１６を界面に形成することができ、このようなＦＥＴは大電流を流せて高速である。

以上の説明では、Ⅲ－Ⅴ族の半導体及び縮退したＳｉ層としてｐ型のものを一例として挙げたが、ｎ型の半導体のものでも全く同じように界面に正孔の反転層を形成することができる。

（２）第２の型

本発明による縮退したＳｉ層／界面準位層／Ⅲ－Ⅴ族半導体の三層構造をもつ電界効果トランジスタの第２の型のものの断面を第３図（ａ）に示す。この三層構造のバンド構造を第３図（ｂ）に示す。４０は、半絶縁性半導体基板、４１は高濃度ｎ型半導体層、４２はⅢ－Ⅴ族のｎ型半導体層、４３は界面準位層、４４は縮退したｐ型Ｓｉ層（ゲート）、４５はソース電極、４６はドレイン電極である。４０は、必ずしも半絶縁性半導体基板に限らず、４２と反対のｐ型導電性を有する半導体基板であつてもよい。縮退したＳｉ層４４がゲートをなしており、界面準位層４３の厚さは３０Å以下、界面準位の密度は10^{12}／ｃｍ／ｅＶ以上である。また、縮退したＳｉ層４４とⅢ－Ⅴ族半導体４２との間には、$E_g \geqq V_{bi}$の関係がある。ここで、E_gは縮退したＳｉ層４４のエネルギー・バンドギヤツプであり、V_{bi}は縮退したＳｉ層４４の価電子帯端E_{v1}とⅢ－Ⅴ族の半導体４２の伝導帯端E_cとのエネルギー差である。

ここで、前述の第１の型の構成で説明したように、$E_g \geqq \frac{2}{3}E_g'$なるエネルギーギヤツプ$E_g'$を有するⅢ－Ⅴ族半導体は、上記Ⅲ－Ⅴ族半導体４２に適用できることは言うまでもない。

縮退したＳｉ層４４は、第３図（ｂ）に示すように直接界面準位層４３と接触しており、かつ正孔濃度が$10^{20}cm^{-3}$以上と高いので界面準位への正孔の充放電時間は縮退したＳｉ層からのものが最も短い。その理由は、第１の型の構成で説明したのでここでは省略する。

したがつて、縮退したＳｉ層４４と界面準位とは準熱平衡状態を達成し、界面準位のフエルミレベルϕ_{fs}は、縮退したＳｉ層のフエルミレベルϕ_nに固定される。このため、ゲートに正電圧V_gを印加すると、表面電位ϕ_sがそれに伴い変

GF Exhibit 1124 - 1743/2704

動する。

一方、縮退したＳｉ層４４とⅢ－Ⅴ族半導体４２との間には、$E_{s} \geqq V_{s}$の関係があるので、Ⅲ－Ⅴ族半導体４２の伝導帯の電子にとつてゲート側にバリアが存在することになる。

以上述べてきたように、本発明によるＦＥＴのゲート構造では、表面電位ϕ_{s}をゲート電圧V_{g}とともに変動させることができ、しかも伝導帯の電子にとつてゲート側の界面にバリアが存在する。そのため、容易に電子の蓄積層４７を界面に形成することができ、このようなＦＥＴは大電流を流せて高速である。

以上の説明では、Ⅲ－Ⅴ族半導体４２としてｎ型のものを、縮退したＳｉ層４４としてｐ型のものを一例として挙げたが、Ⅲ－Ⅴ族半導体４２としてｐ型，縮退したＳｉ層４４としてｎ型のものでも全く同じように界面に正孔の蓄積層を形成することができる。

以上、述べてきたゲート構成は、$\tau_{s} \gg \tau_{r}$となるように、Ⅲ－Ⅴ族半導体と単結晶あるいは多結晶Ｓｉの組み合わせで説明してきた。しかし、本発明のゲート構造は、より一般的に、構成の説明で述べてきた一定の条件を満足できるあらゆる半導体の組み合わせで構成できる一般的なゲート構造であることを付言しておく（但し、ゲート電極となる半導体は、多結晶であつても単結晶であつてもよい）。

〔発明の実施例〕

実施例１

第４図（ａ）～（ｄ）に主要工程を示す。

第４図（ａ）：半絶縁性GaAs基板５０上に、$^{28}Si^{+}$の選択イオン打込み法によつてｎ層５１とｎ$^{+}$層５２を形成し、その後SiO_{2}膜５３を表面に被着した状態で高温熱処理を行い活性化した。$^{28}Si^{+}$の打込み条件は、ｎ層５１については打込みエネルギ７５ｋｅＶ，ドーズ量３×$10^{12}cm^{-2}$であり、ｎ$^{+}$層５２については打込みエネルギ１５０ｋｅＶ，ドーズ量１×$10^{13}cm^{-2}$である。通常ｎ層５１の不純物濃度は、所望する素子特性に応じて10^{16}～$10^{18}cm^{-3}$の範囲で選ぶ。SiO_{2}膜５３の厚さは2000Åであり、CVD（Chemical Vapor Deposition）法で被着した。高温熱処理は、８００℃，２０分間、H_{2}雰囲気中で行つた。

第４図（ｂ）：SiO_{2}膜５３を除去後、プラズマＣＶＤ法により、ホウ素と不純物としてドーピングしたＳｉ膜５５を被着し、続いてスパツタ法によりＷ膜５６を被着した。その後、ホトレジストによるパターンニング後、Ｗ膜５６及びＳｉ膜５５をCF_{4}とO_{2}の混合ガスによるドライエツチングで加工し、ゲート電極を形成した。ここで、Ｓｉ膜５５の膜厚は3000Å、Ｗ膜５６の膜厚は1000Åである。Ｗ膜５６を被着し、Ｓｉ膜５５の膜厚を3000Åとしたのは、ゲート抵抗の低減を目的とするものであり、必ずしも必要でなく、Ｓｉ膜５５の膜厚はゲート電極としての役割を果たすために最低５０Åあればよい。

また、SiO_{2}膜５３除去からＳｉ膜５５被着までの間に通常の工程では、ｎ型５１の表面を空気中あるいは水中の酸素にさらすことが普通である。このためｎ層５１表面に自然酸化膜が１０Å程度形成される。このため、ｎ層５１とＳｉ膜５５との界面には、界面準位層５４が形成される。また、Ｓｉ膜５５とGaAsとの格子定数の不整合によつて、より一層界面準位は導入されやすくなる。

本実施例によるＳｉ膜５５は、基板温度200℃，$B_{2}H_{6}$とSiH_{4}の流量比４対１００，高周波電力１００Ｗ、圧力1Torrで形成した。この基板温度によれば、形成されたＳｉ膜５５はアモルファス状態である。また、この$B_{2}H_{6}$とSiH_{4}の流量比によれば、後の高温熱処理工程で、活性化するホウ素は$10^{20}cm^{-3}$以上となる。

第４図（ｃ）：SiO_{2}膜５７を2000Å被着した後、再び、８００℃，２０分間の熱処理をH_{2}雰囲気中で行つた。この高温熱処理により、Ｓｉ膜５５は多結晶へ転換し、膜中に含有されたホウ素は電気的に活性化する。この結果、Ｓｉ膜５５はｐ型の導電性を有する多結晶膜となり、電気的に活性なホウ素濃度は$10^{20}cm^{-3}$となつた。

ｐ型の導電性を実現するために、本実施例では

GF Exhibit 1124 - 1744/2704

ホウ素を添加したが、ガリウムやアルミニウムを添加してもp型導電性を実現できることは言うまでもない。ホウ素は、p－CVD法で、ガリウムやアルミニウムはMBE法で添加するのが容易である。

第4図（d）：ホトレジストにより電極パターンを形成した後、パターン部のSiO_2膜を除去し、AuGe／Ni／Auを全面に被着し、不要な金属をホトレジストとともに取り除き（リフトオフ法）、ソース・ドレイン電極58，59を形成した。金属の被着膜厚は、AuGe600Å，Ni100Å，Au800Åである。その後400℃，3分間，H_2雰囲気中で熱処理を行つた。この時、n⁺層52へのオーミツク接触が実現する。

本実施例によれば、多結晶p－Si層とn－GaAs層の界面に電子の蓄積層がゲート電圧0.8V以上で容易に形成され、従来のMISFETに比べ、同じゲート電圧で3倍以上の電流を流すことができ、相互コンダクタンスgm＝400mS／mmが得られた。また、界面準位の充放電時間が短く、相互コンダクタンスや容量の周波数依存性が小さくなるという改善効果も同時に確認された。

本実施例では、縮退したSi層がp型，Ⅲ－Ⅴ族半導体がn型，ゲートとソースあるいはドレインの間の半導体もn型であつたが、これらの導電性が逆の場合、すなわち縮退したSi層がn型であり、Ⅲ－Ⅴ族半導体及びゲートとソースあるいはドレインの間の半導体が共にp型である場合にも、同様に正孔の蓄積層が形成されて、大電流を流すことができた。

また、本実施例では、ゲート電極として縮退したSi層を用いたが、この他に以下に列挙する半導体を用いることもできる。すなわち、
BP，AlP，AlAs，AlSb，GaN，GaP，GaAs，GaSb，InN，InP，$Al_xIn_{1-x}P$（$0<x<1$），$Al_xGa_{1-x}As$（$0<x<1$），$Al_xIn_{1-x}As$（$0.2\leqq x<1$），$Al_xGa_{1-x}Sb$（$0<x<1$），$Al_xIn_{1-x}Sb$（$0.4\leqq x<1$），$Ga_xIn_{1-x}P$（$0<x<1$），$Ga_xIn_{1-x}As$（$0.4\leqq x<1$），GaP_xAs_{1-x}（$0<x<1$），$GaAs_xSb_{1-x}$（$0.8\leqq x<1$），InP_xAs_{1-x}（$0.4\leqq x<1$），$Al_xGa_{1-x}P_yAs_{1-y}$（$0<x<1$，$0<y<1$），$Al_xGa_{1-x}As_ySb_{1-y}$（$0<x<1$，$0<y<1$），$Ga_xIn_{1-x}P_yAs_{1-y}$（$0.4\leqq x<1$，$0.4\leqq y<1$），$Ga_xIn_{1-x}As_ySb_{1-y}$（$0.7\leqq x<1$，$0.7\leqq y<1$），$(Al_xGa_{1-x})_yIn_{1-y}P$（$0<x<1$，$0<y<1$），$(Al_xGa_{1-x})_yIn_{1-y}As$（$0<x<1$，$0.5<y<1$），$(Al_xGa_{1-x})_yIn_{1-y}Sb$

（$0.5\leqq x<1$かつ$0.5\leqq y<1$あるいは、
$0.4\leqq x<0.5$かつ$0.6\leqq y<1$あるいは、
$0.3\leqq x<0.4$かつ$0.7\leqq y<1$あるいは、
$0.2\leqq x<0.3$かつ$0.8\leqq y<1$）

$In(P_xAs_{1-x})_ySb_{1-y}$（$0.6\leqq x<1$）

からひとつを選ぶことができる。これらの半導体のエネルギーギヤツプE_gは、GaAs（エネルギーギヤツプ$E_g'=1.4eV$）に対して、前述の関係式$E_g\geqq\frac{2}{3}E_g'$を満足する。

また、本実施例ではⅢ－Ⅴ族半導体としてGaAsを用いたが、この他に、InP，AlGaAs，InGaAs，InGaAsP 等のⅢ－Ⅴ族半導体を用いることもできる。特に、InPに対しては、このエネルギーギヤツプが1.3eV のため、前に列挙した半導体をゲート電極にすべて適用できる。また、Ⅲ－Ⅴ族半導体に限らず、Si，Geを用いても良いことは言うまでもない。

実施例2

第5図（a）～（d）に主要工程を示す。本実施例では、ゲート電極として用いるSi膜をマスクとして、自己整合的にn⁺層を形成する工程に特徴がある。

第5図（a）：半絶縁性GaAs基板50に、$^{28}Si^+$の選択イオン打込み法によつてn層51を形成し、その後SiO_2膜53を表面に被着した状態で、高温熱処理を行い活性化した。$^{28}Si^+$の打込み条件は、打込みエネルギー75keV，ドーズ量$3\times10^{13}cm^{-2}$である。SiO_2膜53の厚さは2000Åであり、CVD法で被着した。高温熱処理は、800℃，20分間，H_2雰囲気中で行つた。

第4図（b）：SiO_2膜53を除去後、プラ

GF Exhibit 1124 - 1745/2704

ズマCVD法により、ホウ素を不純物としてドーピングしたSi膜55を被着し、続いてスパッタ法によりW膜56を被着した。その後、ホトレジストによるパターンニング後、W膜56及びSi膜55をCF$_4$とO$_2$の混合ガスによるドライエッチングで加工し、ゲート電極を形成した。ここで、Si膜55の膜厚は3000Å，W膜56の膜厚は1000Åとしたが、この二層膜を合わせた膜厚は、後のn$^+$層形成に用いる$^{29}Si^+$のイオン打込みエネルギーに応じて決定される。また、Si膜55の膜厚はゲート電極としての役割を果たすために最低50Åあればよい。

実施例1で説明したように、n層51の表面には自然酸化膜が10Å程度形成される。このため、n層51とSi膜55との界面には、界面準位層54が形成される。また、Si膜55の製造条件は、実施例1と同様である。

第5図（c）：Si膜55とW膜56の二層膜をマスクとし、$^{29}Si^+$を選択的にイオン打込みし、ゲートに隣接する領域をn$^+$－GaAs層52とソース・ドレインのn$^+$層52へのオーミック接触がとれる。

本実施例のゲート構造は実施例1と同一であるが、特に本実施例によれば、ゲートとソース及びドレインの間のn$^+$層を$1\times10^{13}cm^{-2}$の高ドーズで形成したために、寄生抵抗が低下し、従来のMISFETに比べ4倍以上の電流を流すことができた。また、相互コンダクタンス540mS／mmが得られた。

本実施例においても、実施例1に列挙した如き、半導体をゲート電極として用いることは可能である。

ゲート電極にIII－V族半導体を用いる場合、実施例1の如く、n$^+$層52をゲートに自己整合して設けることをしない素子では、第4図（c）の高温熱処理工程は省略できる。なぜなら、たとえばAlGaAsをゲート電極として用いる場合には、通常MOCVD法やMBE法によつて成長することが可能であり、これらの方法によれば膜はすでに成長時に、多結晶あるいは単結晶となるからである。

した。この時、二層膜の直下のGaAsには$^{29}Si^+$は打込まれない。その後、再び2000ÅのSiO$_2$膜57を被着した状態で高温熱処理を行いn$^+$層52を活性化した。$^{29}Si^+$の打込み条件は、打込みエネルギー150keV，ドーズ量$1\times10^{13}cm^{-2}$であり、高温の熱処理は800℃，20分間，H$_2$雰囲気中で行つた。この高温熱処理により、Si膜55は多結晶へ転換し、膜中に含有されたホウ素は電気的に活性化する。この結果、Si膜55は、p型の導電性を有する多結晶膜となり、電気的に活性なホウ素濃度は$10^{20}cm^{-3}$となつた。

第5図（d）：ホトレジストにより、電極パターンを形成した後、パターン部のSiO$_2$膜57を除去し、AuGe／Ni／Auを全面に被着し、不要な金属をホトレジストとともに取り除き（リフトオフ法）、ソース・ドレイン電極58，59を形成した。金属の被着膜厚はAuGe600Å，Ni100Å，Au800Åである。その後、400℃，3分間H$_2$雰囲中で熱処理を行つた。このとき、

しかし、本実施例の如く、n$^+$層52をゲートに自己整合して設ける素子においては、その高温熱処理工程を省略できない（第5図（c））。すなわち、ゲート電極にAlGaAs等のIII－V族半導体を用いた場合、ゲート電極をp型の導電性を持たせるためにドーピングする不純物は、GaAsに対してアクセプタとなりうる。そのため、第5図（c）の工程に含まれるn$^+$層を活性化する高温熱処理により、ゲート電極中の不純物がGaAs側に拡散し、n－GaAs層51のキャリア濃度を変動させる要因となる。このような、変動は、一般にキャリア濃度制御を精密に実現することが重要な高集積回路の製作には致命的である。

ところが、本実施例の如く、Si膜をゲート電極に用いた場合、Si膜にドーピングされる不純物はホウ素やガリウム等のIII族の元素であり、GaAs中においては、アクセプタあるいはドナーとならない。このため、高温熱処理を施してもキャリア濃度の変動要因とならない。したがつて、本実施例の如くIII－V族の半導体基板を用い、高温

GF Exhibit 1124 - 1746/2704

熱処理工程を終る素子においては、特にＳｉ膜が有用である。

実施例３

第６図（ａ）～（ｄ）に主要工程を示す。

第６図（ａ）：半絶縁性GaAs基板２０上に、$^{28}Si^{+}$の選択イオン打込み法によつてｎ層２１とｎ$^{+}$層２２を形成し、その後SiO_2膜２３を表面に被着した状態で高温熱処理（８００℃，２０分）を行い活性化した。$^{28}Si^{+}$の打込み条件は、ｎ層２１については打込みエネルギー７５ｋｅＶ，ドーズ量$3\times10^{12}cm^{-2}$であり、ｎ$^{+}$層２２については打込みエネルギー１５０ｋｅＶ，ドーズ量$1\times10^{13}cm^{-2}$である。SiO_2膜２３の厚さは2000Åであり、ＣＶＤ（Chemical Vapor Deposition）法で被着した。高温熱処理は、800℃，２０分間，H_2雰囲気中で行つた。

第６図（ｂ）：高温熱処理に用いたSiO_2膜２３のゲート部をエツチングにより除去した。その後空気中に長時間さらし、GaAsの自然酸化膜による界面準位層２４を１０Åの厚さでつくつた後、除去した領域だけにMOCVD（Metal Organic Chemical Vapor Deposition）法により縮退したｐ－$Ga_{0.7}Al_{0.3}As$層２５を選択エピタキシヤル成長した。ｐ－$Ga_{0.7}Al_{0.3}As$層２５の不純物濃度は縮退の条件を満足させるために10^{20}~$10^{21}cm^{-3}$台とした。この時用いた不純物はＺｎであり、MOCVD法による成長温度を、６８０℃としたのでｐ－$Ga_{0.7}Al_{0.3}As$層２５直下のｎ層はＺｎによる拡散で完全に補償されてｐ－GaAs層２６となる。また、ゲート部のSiO_2膜を除去したのち、空気中に長時間さらしてGaAs基板表面に、GaAs中のバンドギヤツプ中に準位を高密度に持つGaAsの自然酸化膜を１０Å程度つくり、その上にｐ－$Ga_{0.7}Al_{0.3}As$層を成長させたのでｐ－$Ga_{0.7}Al_{0.3}As$層２５とｐ－GaAs層２６の界面には高密度の界面準位層２４が形成されている。

第６図（ｃ）：AuGe／Ｎｉ／Ａｕをこの順に６００Å，１００Å，８００Åと被着し、イオンミリング法によりゲート部以外の領域の金属を除去し、ゲート電極２７を形成した。

第６図（ｄ）：ホトレジストにより電極パターンを形成した後、パターン部のSiO_2膜を除去しAuGe／Ｎｉ／Ａｕを全面に被着し、不要な金属をホトレジストとともに取り除き（リフトオフ法）ソース・ドレイン電極２８，２９を形成した。金属の被着膜厚は、AuGe６００Å，Ｎｉ１００Å，Ａｕ８００Åである。その後４００℃，３分間，H_2雰囲気中で熱処理を行つた。この時、ｎ$^{+}$層２２へのオーミツク接触とともに、ｐ－$Ga_{0.7}Al_{0.3}As$層２５へのオーミツク接触が実現する。

本実施例によれば、ｐ－$Ga_{0.7}Al_{0.3}As$層とｐ－GaAs層の界面に電子の反転層がゲート電圧が０．８Ｖ以上で容易に形成され、従来のMISFETに比べ、同じゲート電圧で３倍以上の電流を流すことができ相互コンダクタンスg_m＝４００ｍＳ／㎜が得られた。また、界面準位の充放電時間が短く、相互コンダクタンスや容量の周波数依存が小さくなるという改善効果も同時に確認された。

本実施例では、ゲート電極となる$Ga_{0.7}Al_{0.3}As$層もGaAs層も共にｐ型であり、ゲートとソースあるいはドレインの間の半導体はｎ型であつたが、これらの導電性が逆の場合、すなわちゲート電極となる$Ga_{0.7}Al_{0.3}As$層もGaAs層も共にｎ型であり、ゲートとソースあるいはドレインの間の半導体はｐ型である場合にも同様に正孔の反転層が形成されて、大電流を流すことができた。

また、本実施例では、ゲート電極として縮退した$Ga_{0.7}Al_{0.3}As$層を用いたが、この他にＳｉ層、あるいは、実施例１で列挙した半導体を用いることも可能である。また、基板に用いたGaAsの代りに、ＩｎＰ，ＡｌGaAs，InGaAs，InGaAsP等のⅢ－Ⅴ族半導体あるいはＳｉ，Ｇｅを用いることができることは言うまでもない。

〔発明の効果〕

以上述べたように、本発明によれば縮退した半導体と半導体の界面に反転層あるいは蓄積層が容易に形成され、従来のMISFETに比べ、同じゲート電圧で３倍以上の電流を流すことができ、ＦＥＴを高速化できる効果がある。

図面の簡単な説明

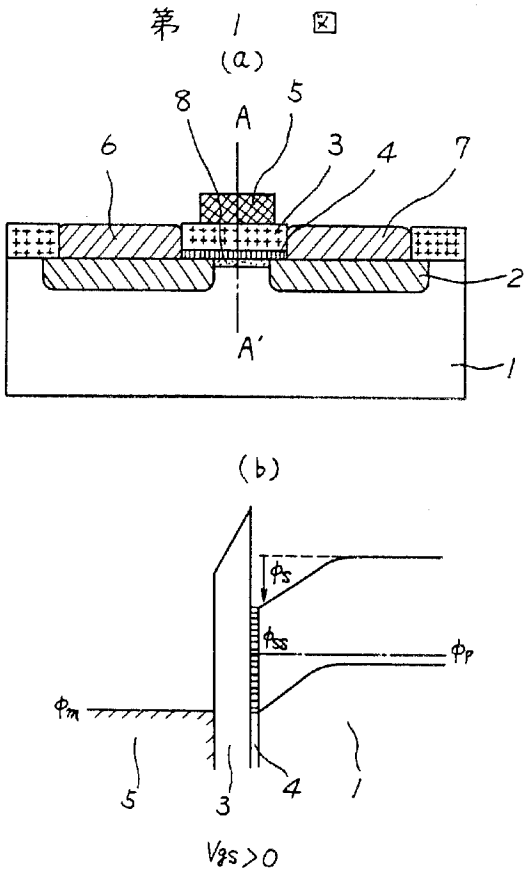
GF Exhibit 1124 - 1747/2704

第１図（ａ）はMISFETの構造断面図、同図（ｂ）はＡ－Ａ′線断面のバンド構造図である。第２図（ａ）は本発明によるＦＥＴの構造断面図、同図（ｂ）はＢ－Ｂ′線断面のバンド構造図である。第３図（ａ）は本発明によるＦＥＴの構造断面図、同図（ｂ）はＢ－Ｂ′線断面のバンド構造図である。第４図～第６図は、本発明によるＦＥＴの一実施例としての製造プロセスに従う装置断面図である。

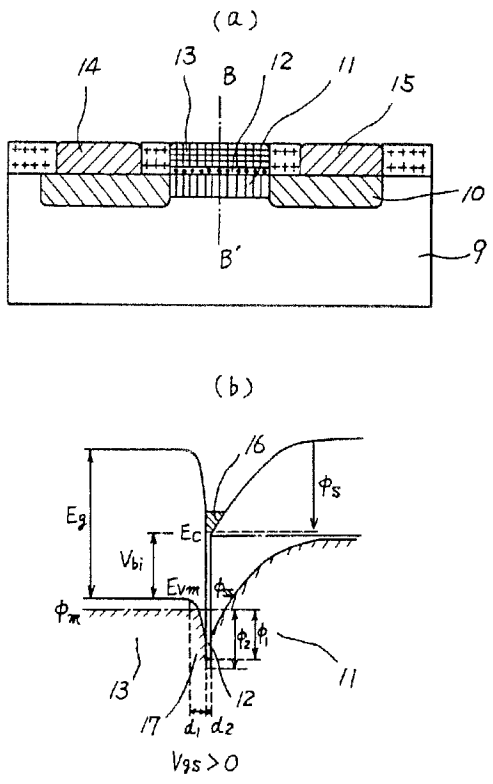
９…半絶縁性半導体基板、１０…ｎ型半導体層、１１…ｐ型Ⅲ－Ⅴ族半導体層、１２…界面準位層、１３…細退したｐ型Ｓｉ層（ゲート）、１４…ソース電極、１５…ドレイン電極、４０…半絶縁性半導体基板、４１…高濃度ｎ型半導体層、４２…ｎ型Ⅲ－Ⅴ族半導体層、４３…界面準位層、４４…細退したｐ型Ｓｉ層（ゲート）、４５…ソース電極、４６…ドレイン電極。

代理人　弁理士　小川勝男

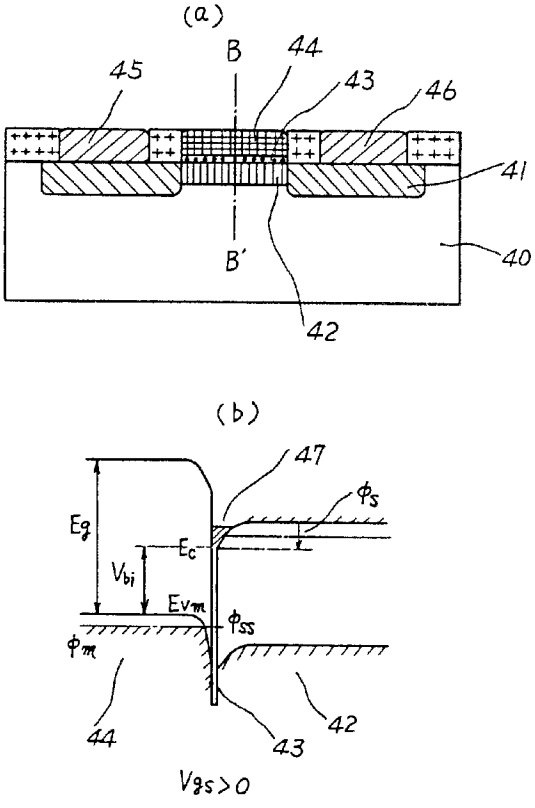
第１図



第２図

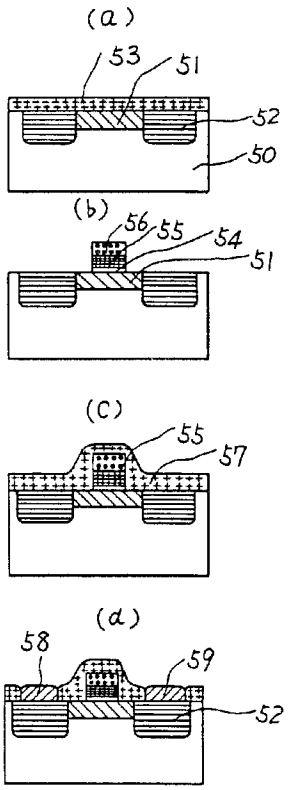


第３図

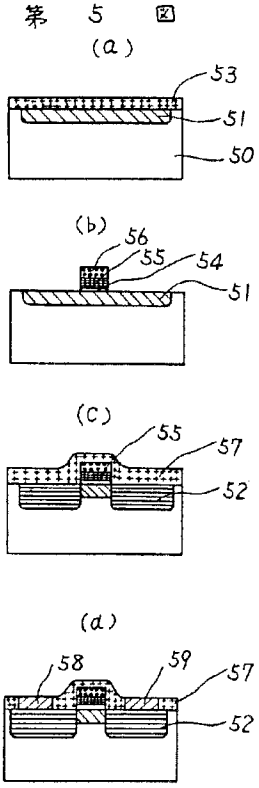


GF Exhibit 1124 - 1748/2704

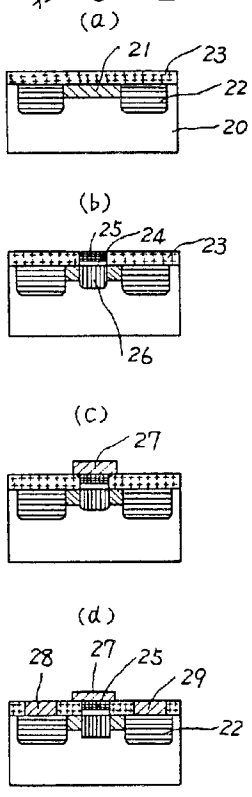
第 4 図



第 5 図



第 6 図



GF Exhibit 1124 - 1749/2704

第1頁の続き

⑫発明者　橋本　哲一　国分寺市東恋ケ窪1丁目280番地　株式会社日立製作所中央研究所内

⑫発明者　松原　宏和　国分寺市東恋ケ窪1丁目280番地　株式会社日立製作所中央研究所内

⑫発明者　小野　佑一　国分寺市東恋ケ窪1丁目280番地　株式会社日立製作所中央研究所内

⑫発明者　中塚　慎一　国分寺市東恋ケ窪1丁目280番地　株式会社日立製作所中央研究所内

⑫発明者　石岡　祥男　国分寺市東恋ケ窪1丁目280番地　株式会社日立製作所中央研究所内

⑫発明者　高橋　進　国分寺市東恋ケ窪1丁目280番地　株式会社日立製作所中央研究所内

GF Exhibit 1124 - 1750/2704

Espacenet

JPS6261363A SEMICONDUCTOR DEVICE

Applicants: HITACHI LTD

Inventors: HASHIMOTO TETSUKAZU,ISHIOKA YOSHIO,MATSUBARA HIROKAZU,MATSUOKA NAOYUKI,NAKATSUKA SHINICHI,ONO YUICHI,SHIGETA JUNJI,TAKAHASHI SUSUMU,TAKATANI SHINICHIRO,UMEMOTO YASUNARI

Classifications:
IPC ***H01L29/20; H01L29/78;*** (IPC1-7): H01L29/20; H01L29/62; H01L29/78;

Priorities: JP19940685A 1985-09-11

Application: JPS6261363A·1985-09-11

Publication: JPS6261363A·1987-03-18

Published as: JPS6261363A

SEMICONDUCTOR DEVICE

Abstract

PURPOSE:To obtain a high speed field effect transistor which can feed a large current by forming a 3-layer structure of a degenerate Si layer/boundary level layer/group III-V semiconductor, and pinning the Fermi level of the Si layer to that of the boundary level layer. CONSTITUTION:An N-type semiconductor layer 10, group III-V P-type semiconductor layer 11, a boundary level layer 12, a degenerate P-type Si layer (gate) 13, a source electrode 14, and a drain electrode 15 are formed on a semi- insulating semiconductor substrate 9. The thickness of the layer 12 is 30Angstrom or less, the density of the boundary level is 10<12>/cm<2>/eV or higher, and there is a relation of Eg>=Vbi between the layer 13 and the semiconductor 11. Eg is the energy band gap of the layer 13, and Vbi is the energy difference between the valence band end of the layer 13 and the conduction band end of the semiconductor 11. The layer 13 and the boundary level perform a quasi-thermal equilibrium state, and the Fermi level of the boundary level is secured to the Fermi level of the layer 13.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION JPS6261363

[0001]

[Field of Use of the Invention] The present invention relates to a high-speed electrodeposition effect transistor. [Background of the Invention] A cross-sectional view of a MISFET (Metal fi, nsu) ator Field E, ffcct Transistor) using a compound semiconductor substrate such as GaAs or InP is shown in Fig. 1 ('l). Here, 1 is a p-GaAs substrate, 2 is an n GaAs layer, 3 is an insulating film, 4 is an interface state layer, 5 is a gate electrode, 6 is a source electrode, and 7 is a drain electrode. The thickness of the insulating film 3 is usually between 1000 and 3000. Such an MJSFET is a device capable of performing an inversion type operation. That is, when the stopping voltage is applied to the gate electrode 5, the electron inversion layer 8 is formed at the interface between the insulating film 3 and the P-GaAs substrate 1. Since the inversion layer is used for the channel, the MISFET has a potential as a high speed device because it can draw a large current. However, in reality, as shown in the band structure diagram of FIG. 1 (b), at the interface between the insulating film 3 and the P GaAs substrate 1, the 10 ″ -1011 / cd / eV level is near the center of the semiconductor energy gap. It is known that there is a layer 4 with extremely high density of interface 1 (4) (hereinafter referred to as interface level layer 4) with a thickness of 10 to 30 people. Especially in compound semiconductors. It is extremely difficult to keep this value below LO "cx-'/ eV (for example, in GaA + s, oxygen atoms and metal atoms are exposed on the surface due to exposure to air or contamination with impurities. It is known that an interface state layer of 10 "aa-" / eV or more is generated only by attaching one layer.) Therefore, the conventional MIsFhi has the Fermi level ϕ 6. Has a strong tendency to be fixed to the Fermi level ϕ of the semiconductor, and even if a positive voltage is applied to the gate electrode, the surface potential ϕ 6 does not fluctuate and it is difficult to form the inversion layer. As described above, in the conventional MiSFET, it is difficult to use the inversion layer as a channel, and a large amount of current cannot be obtained. This is because there is a high-density interface state layer, and the Fermi level of the interface state tends to be fixed to the Fermi level of the

GF Exhibit 1124 - 1752/2704

semiconductor. Examples of MIS transistors as explained below can be found in, for example, solid-state electronics [5olid-8tate Electronics] vol, 17r pp751-759 (1974).

[Object of the Invention] An object of the present invention is to provide a high-speed field effect transistor capable of passing a large current. [Outline of the Invention] As described above, in the conventional MISFET, the Fermi level of the interface state tends to be fixed to the Fermi level of the semiconductor. This is physically the charge / discharge time of electrons from the semiconductor side to the interface state. This is because the quasi-thermal equilibrium state is established between the interface state and the semiconductor because it is shorter than the charging / discharging time from another region (for example, the gate metal). To describe more quantitatively, the charge / discharge time t of electrons from the semiconductor side to the interface state is, for example, in the range of 10n5ec-10m5ec when the semiconductor is n-GaAs, and more generally nl-V It is known that the charge / discharge time of the group compound semiconductors falls within the range of 10 n5ac to 10 m5ec. On the other hand, the charge / discharge time t of the charge P from the gate metal to the interface state is. となる。 However, D, the interface state density (cn-2 / eV) Aϕ1. = Is the Fermi level ϕ1. Movement of 1 t (eV) V @ k: velocity of free electrons in gate metal 5 (am / 5ee) N: concentration of free electrons in gate metal 5 (aII-J) T1: probability of tunneling through insulating film 3 (however, , For the sake of simplicity, it is assumed here that the rectangular potential barrier is 1-channel.) D: Insulation 1 (thickness of the island 3) ϕ: Height of the barrier due to the insulating film 3 through which electrons tunnel eV) m: Effective mass of electrons in the insulation 1 void 3 (g) mo: Electrons in vacuum Is the mass (g) of D, -Aϕs 6:10 ” ” ” (2m- “ gVtb in] 07cn / see, N * 10 ” ao-3, ϕ in 4eVrm / rr +. -: 0.2, d = I-1000A <up to 1 enumeration 1. 4 Ut, which is a typical value of a normal MIS structure.), T becomes 10 ″ 'sac, and τ becomes (τ). Therefore, the equilibrium state is established between the interface level and the conductor, and the Fermi level of the interface level is fixed to the Fermi level of the semiconductor. Therefore, as described above, in order to fix the Fermi level of the interface state to the Fermi level of the gate metal, the gate structure may be configured so that τ1 is controlled. The present invention realizes the above gate structure. Basically, it has the following configuration.

At least an interface level layer in the mv group semiconductor region having the first conductivity and a single crystal or polycrystalline Si layer (hereinafter referred to as Si layer) in the interface level layer-1. The interface level layer has at least a control unit and a carrier transmission / reception unit sandwiching the control unit, and the interface level layer pin the Fermi level of the Si layer to the Fermi level of the interface level layer. I will make it at least. It is preferable that the interface level layer has an interface level of 10 ″ / cd / eV or more at a position corresponding to the energy gap of the semiconductor layer of the group (1)-(4). The thickness is preferably 30 Å or less. Such an interface state layer has a mismatch in lattice constant between the semiconductor of the --- group and Si, deviation of stoichiometry due to a

GF Exhibit 1124 - 1753/2704

high temperature process during Si growth or deposition, exposure to air or water, Alternatively, the growth of Si, the growth during deposition, and the formation of oxygen in the deposition container by the oxygen remaining in the group ■-■ group ■-■ semiconductor or Si oxide (natural oxide film), etc. It can be easily introduced due to contamination by the insulating material and trace amount of metal remaining on the interface. Further, such an interface level layer can be more positively formed by means such as a plasma oxidation method or an anodic oxidation method. It is customary to use a degenerated Si layer, but the conditions are, for example, W Shockley [W, 5 hockley] "I Reftron and Holes in Semiconductor (Electron! 1 and Ho1es in Sem1conductors) ” , Dee 9 Juan Nostrand Princeton NJ (D, Fan No5trand, Pr1nceton, N, J,) +1950, etc. should be used. The degeneration condition of the semiconductor is actually controlled by the impurity concentration. An example of the condition is shown in Table 1. Table 1 Sinf! , Electric type 4.2 or higher P conductive type], 5 or higher (unit x t o) ■ -3. Room temperature) (According to the above-mentioned literature, the degeneracy condition was calculated as E, −EC ≧ kT for n conductivity type, and Ev−E, ≧ kT for p conductivity type. However, E is the Fermi level of the semiconductor, and Ec is the energy at the conduction band edge. Ev is the valence band edge energy, k is the Boltzmann constant, and T is the absolute temperature.) The thickness of the Si layer may be at least 50 Å or more, and the range of 50 to 5000 is selected as necessary.

The following two types are conceivable as more specific semiconductor device configurations. (1) The Si layer has an energy bandgap whose size is between the edge of the energy band at the interface where minority carriers are present in the semiconductor layer of the group and the edge of the energy band where majority carriers are present in the Si layer. It is larger than the difference, and has the same conductivity as that of the ■ -v semiconductor layer, and the conductivity of the semiconductor layer between the gate and the source or the drain is opposite to that of the ■-■ semiconductor layer. Eggplant According to this structure, the inversion layer can be easily formed and a large current can be passed. (2) In the Si layer, the size of the energy band gap is between the band of the energy band at the interface where majority carriers exist in the semiconductor layer of the group --- and the edge of the energy band where majority carriers exist in the Si layer. The conductivity is larger than the difference, and has the opposite conductivity to that of the group V semiconductor layer, and the conductivity of the semiconductor layer between the gate and the source or the drain is the same as that of the group S semiconductor layer. . According to the configuration of 1 :, the formation of the storage layer is easy and a large current can be passed. Each will be described below. (1) First type FIG. 2 (a) shows a cross section of a first type of field effect transistor having a three-layer structure of degenerated Si layer / metaphysical layer / m = v semiconductor according to the present invention. The band structure of this two-layer structure shown in FIG. 2 is shown in FIG. 9 is a semi-insulating semiconductor substrate, 10 is an n-type semiconductor layer, 11 is an m-v group p-type semiconductor layer, 12 is an interface state layer, 13 is a degenerate p-type Si layer (gate), and 14 is a source. Electrodes and 15 are drain bars. 9 is not necessarily a semi-

GF Exhibit 1124 - 1754/2704

insulating semiconductor substrate, but may be a semiconductor substrate having the same P-type thick electrical property as 1]. The degenerated Si 13 serves as a gate, and the thickness of the interface state layer 12 is 30 Å or less and the density of 5 interface states is], and O″ / ad / AV or less-hi. Further, there is a relationship of E, ≧ Vbl between the degenerated Si layer 13 and the semiconductor 11 of the group ■-■. Here, El is the energy bandgap of the degenerate S iMl 3, and ■, l are the valence band edge Ev of the degenerated Si layer 13 and the conduction band edge E of the mv semiconductor J1. It is the energy difference. The energy gap of Si is known to be 1.1 cV at room temperature, and in the case of In-V group semiconductors, about 2/3 of the energy gap E9 'of the semiconductor is separated from the conduction band edge. It is a well-known fact that there is a Fermi 1 novel on the interface at a different position, that is, Vbc = Eg '.

Therefore, the In-v group semiconductor satisfying the relationship of E and ≧ −E1 ′ can be applied to the above-mentioned 1-— group semiconductor 1.1. For example, the energy gap of GaAs is E, '= 1.4 eV, which satisfies the above equation. The degenerated Si layer] -3 is directly in contact with the interface level layer 12 as shown in FIG. 2 (b), and the hole concentration is as high as 10 "+ a ++-'or -L. At the time of charging / discharging holes to the level, IIn is the shortest from degenerate Si. The reason is that the charge / discharge time τ of electrons from the Si layer degenerate to 5 to the interface state can be expressed in a form similar to the equations (1) and (2), as described below. .. However, D ,: Interface state density of the interface state layer 12 (dll-"/ eV) A ϕ 8. Fermi level of interface level ϕ 8 due to charge / discharge of two electrons. + T (eV) V z k: Velocity of free holes in degenerated Si layer 13 (cs / 5ee) N: Concentration of free holes in degenerated Si layer 13 („ “3) Tt: Degeneracy Probability of tunneling the depletion layer 17 generated in the Si layer 13 and the interface state layer 12. (However, for the sake of simplicity, it is assumed here that a rectangular potential barrier is tunneled.) Dl: thickness of depletion layer 17) ϕ 1: height of barrier due to depletion layer 17 in which holes tunnel eV) ml: effective mass of holes in degenerated Si layer 13 (g) mo: in vacuum Mass of electron (g) d2 = thickness of interface enhancement layer 12) ϕ 2: height of barrier eV) m due to interface level layer 12 through which holes tunnel, m: of holes in interface coating layer 12 Effective mass (FC) ε : Dielectric constant (F / m) k of degenerated S i Ml 3 k: Boltzmann constant (eng / K) q: Electric charge (c) T: Absolute temperature (K) Nyl: Degenerated It is the effective state density (1-3) of the valence band of the Si layer 13. D, Δ ϕ as "F 10" (! 1-"+ Vtb" "10" 1 / 5ec) ϕ 1 * 0.45eV + m 0.2m in hand, 10 people in d2. ϕ 2-: 1 eV, m ,: 0.2 mo, E, = 11.9 f. (Fo is the dielectric constant of vacuum: 0,885X IQ- "F / m). Assuming T "300 K-Nvx f'10" low ", the hole concentration of the degenerated Si layer 13 is set as N = l 02oam- '. d, = 26 people τ , = 200 ps. Therefore, τ 1 is sufficiently shorter than the charge / discharge time v of the semiconductor layer 11 (= 10 n5ca to 10 m5ce).

Therefore, the degenerated S1 layers 1; 3 and the interface state achieve a montothermal

GF Exhibit 1124 - 1755/2704

equilibrium state, and the Fermi level ϕ9. Is fixed to the Fermi level ϕ of the degenerated Si layer. Therefore, when a positive voltage is applied to the gate, the surface potential ϕ changes accordingly. On the other hand, the degenerate Si layer 13 and the semiconductor 11 of the group 1 to 4 have a relation of E, ≧ 3. A barrier exists on the gate side for electrons in the conduction band of the semiconductor group 11-. As described above, in the gate structure of the FET according to the present invention, the surface potential ϕ can be varied with the goo voltage to the voltage, and further, a barrier exists at the interface on the gate side for electrons in the conduction band. Therefore, the electron inversion layer 16 can be easily formed at the interface, and such an FET can flow a large current at a high speed. In the above description, the group III-V semiconductor and the degenerate Si layer are used as P layers. I took the type as an example. A hole inversion layer can be formed at the interface in the same manner even with an n-type semiconductor. (2) Second type FIG. 3 (a) shows a cross section of a second type of field effect transistor having a three-layer structure of a degenerated Si layer / physical plane layer / group III-group semiconductor according to the present invention. The band structure of the three-layer structure shown in FIG. 3 is shown in FIG. 3B, 40 is a semi-insulating semiconductor substrate, 41 is a high-concentration n-type semiconductor layer, 42 is a ■ -V group n-type semiconductor layer, 43 is an interface state layer, 44 is a degenerated p-type Si layer (gate), 45 is a source electrode, and 4G is a drain electrode. 40 is not necessarily a semi-insulating semiconductor substrate, and may be a semiconductor substrate having a P-type trench property opposite to 42. The degenerated 31 layer 44 forms a gate, the thickness of the interface state layer 43 is 30 Å or less, and the density of the interface state is 10 ″ / ffl / eV or more. In addition, the degenerate 31 layer 44 and the {circle around (1)}-■ group semiconductor 42 have a relationship of E, ≧ 1. Here, E is the energy bandgap of the degenerate 31 layer 44, and ■ □ is the valence 1 of the degenerate 31 layer 44, and the conduction band edge E of the − and III-V semiconductor 42 4: F. This is the energy difference from the end E1. Here, as described in the configuration of the first type described above, the −V group semiconductor having the energy gaps E and J such that E and ≧ −E1 ′ is applicable to the III-V group semiconductor 42 described above. Needless to say. Since the degenerated 31 layer 44 is in direct contact with the interface level layer 43 as shown in FIG. 3 (b) and the hole concentration is as high as 10 ″ cs ° 1 or more, holes to the interface level are increased. The shortest charging / discharging time is from the degenerated Si layer. The reason for this is omitted here because it has been described in the first type configuration.

Therefore, the degenerated S1 layer 44 and the interface state achieve a heat-increasing equilibrium state, and the Fermi level ϕ1. Is fixed to the Fermi level ϕ of the degenerated Si layer. Therefore, a positive voltage is applied to the gate. Is applied, the surface potential ϕ fluctuates with the passing. On the other hand, since the degenerate Si layer 44 and the In-V group semiconductor 42 have a relationship of E and ≧ Vkl, a barrier exists on the gate side for electrons in the conduction band of the III-V group semiconductor 42. Will be done. As described above, in the gate structure of the FET according to the present invention, the surface potential

GF Exhibit 1124 - 1756/2704

ϕ can be changed along with the gate voltage v1 ° , and a barrier exists for the electrons in the conduction band at the interface on the gate side. Therefore, the FET can be easily formed on the interface of the electron storage layer 47, and such an FET can flow a large current and is high speed. In the following description, the n-type semiconductor is used as the 1 --- group semiconductor 42 and the n-type one is used as the degenerated Si layer 44 as an example. Even if an n-type layer 44 is used, a 9M layer for holes can be formed at the interface in the same manner. The gate structure described above has been described by combining {circle over ()} and [tau], and the combination of (1) -V group semiconductor and single crystal or polycrystalline Si. However, it should be added that the gate structure of the present invention is more generally a general gate structure that can be composed of any combination of semiconductors that can satisfy the certain conditions described in the description of the structure (however, Gate t !! The polar semiconductor may be polycrystalline or single crystal). [Embodiment of the Invention] Embodiment 1 Main steps are shown in FIGS. 4 (a) to 4 (d). Fig. 4 (a) A state in which the 1st layer 51 and the n0 layer 52 are formed on the semi-insulating GaAs substrate 5o by the selective ion implantation method of Z @ Si +, and then the S x Ox I grain 53 is deposited on the surface. Implantation conditions of e "S x" activated by high-temperature heat treatment are: implantation energy 75 θ V for 1 layer 51, dose 13X10 "as- ', implantation energy 150 keV, dose I for n0 layer 52. The impurity concentration of the 0 normal n-layer 51, which is X 1013aW- ', is selected in the range of 10 "to lO" cx- "according to the desired device characteristics, and the thickness of the 5iO7 film 53 is 2000 persons. (Chemical Vapor Deposition) method. The high temperature heat treatment was performed at 800 ° C. for 20 minutes in an H 2 atmosphere.

FIG. 4 (b): After removing the S x O 2 film 53, a Si film 55 doped with boron and impurities as a plasma CVD method is deposited, and then a W film 56 is deposited by a sputtering method 6 After that, After patterning with a photoresist, the W film 56 and the S1 film 55 were processed by dry etching with a mixed gas of CF4 and 0 □ to form a gate electrode. Here, the film thickness of the Si film 55 is 3000 and the film thickness of the W film 56 is 1000. The reason why the W film 56 is deposited and the film thickness of the Si film 55 is set to 3000 is for the purpose of reducing the gate resistance and is not always necessary. You need at least 50 people to play a role. In addition, in the usual process from the removal of the Sin / film 53 to the deposition of the Si film 55, the surface of the n-type 51 is usually exposed to oxygen in the air or water. Therefore, a natural oxide film is formed on the surface of the 9th layer 51 to the extent of [O]. Therefore, the interface level layer 54 is formed at the interface between the first layer 51 and the Si film 55. Further, due to the mismatch of lattice constants between the Si film 55 and GaAs, the interface state is more easily introduced. The Si film 55 according to the present embodiment has a substrate temperature of 200 ° C. B, H, and Sin flow rate ratio 4 to 100. The high frequency power was 100 W and the pressure was L Torr. According to this substrate temperature, the formed Si film 55 is in an amorphous state. Further, according to the flow rate ratio of B2H and Sin, the boron to be activated becomes lQ "an-" or more in the subsequent high temperature heat treatment step. FIG. 4 (c): After depositing 2000 people of SiO and film 57, heat

GF Exhibit 1124 - 1757/2704

treatment at 800 ° C. for 20 minutes is performed again for H. I went in the atmosphere. By this high temperature heat treatment, the Si film 55 is converted into polycrystal, and the boron contained in the film is electrically activated. As a result, the Si film 55 became a polycrystalline film having P-type conductivity, and the concentration of electrically active boron was 1020 -3. Although boron was added in this embodiment to achieve n-type conductivity, it goes without saying that p-type trench conductivity can also be achieved by adding gallium or aluminum. It is easy to add boron by the p-CVD method and gallium or aluminum by the MBE method. Fig. 4 (d): After forming a 7-pole pattern with photo-diss 1-, the SiO □ film of the pattern part is removed, AuGe / Ni / Au is deposited on the entire surface, and unnecessary metal is removed. It was removed together with the photoresist (lift-off method) to form source / drain electrodes 58.59.

The metal deposition thickness is 600 for AuGe, 100 for Ni, and 800 for Au. Then 400 ° C. Heat treatment was performed in (2) atmosphere for 3 minutes. At this time, ohmic contact with the n0 layer 52 appears. According to this embodiment, an electron accumulation layer is easily formed at the interface between the polycrystalline p-S i layer and the n-GaAs layer at a Goo 1-voltage of 0.8 V or more, and has the same gate voltage as that of the conventional MISFET. Then; a current of 3 times or more can be passed, and mutual conductance g m = 400 m S / m is nine, and interface 1 v! It was also confirmed at the same time that the charging / discharging time at 18:11) 1 was short and the frequency dependence of the mutual conductance and the capacity became small. In this example, the degenerated S1 layer was n-type, the mv group semiconductor was n-type, and the semiconductor between the gate and the source or the drain was also n-type. Even when the formed Si layer is of the rl type and the m-v group semiconductor and the semiconductor between the gate and the source or the drain are both of the n type, an alternate stack of holes is similarly formed to flow a large current. I was able to do it. Further, in this example, the degenerated Si layer is used as the gate electrode, but other semiconductors listed below may be used. すなわち。 ＢＰ、ＡＱＰ、ＡＲＡｓ、ＡＱＳｂ、ＧａＮ、ＧａＰ。
ＧａＡｓ、ＧａＳｂ、ＩｎＮｖＩｎＰ＋へＱ、Ｉｎ、－、Ｐ（０＜Ｘ＜１）、ＡＱ、Ｇａｌ－、
Ａｓ（０＜ｘ＜１）。ＡＱ、Ｉｎ、－、
Ａｓ（０，２≦ｘ＜１）＊ＡＱ－Ｇａｌ－．５ｂ（０＜ｘ＜１）、
ＡＱ－Ｉｎｔ－５ｂ（０，４≦ｘ＜１）。Ｇａ、Ｉｎ、－、Ｐ（０＜Ｘ＜１）ｒＧａＪｎ、－、
Ａｓ（０，４≦ｘ＜１）、ＧａＰ、Ａｓ、－、（０＜ｘ＜１）、ＧａＡｓ、Ｓｂ、－。
（０，８≦ｘ＜１）＝ＩｎＰ－Ａｓｌ－＋＋（０－４≦ｘ＜１）。ＡＱ、Ｇａ、－、
ＰｙＡｓｔ－ｙ（０＜ｘ＜１．Ｏ＜ｙ＜１）ＩＡＱ、Ｇａｔ－、
＋ＡｓｙＳｂｔ－ｙ（０＜ｘ＜１．Ｏ＜ｙ＜１）。Ｇａ、
Ｉｎｔ－ｗＰｙＡｓｔ－ｙ（０－４≦ｘ＜１、０、４≦ｙ＜１）。Ｇａ、Ｉｎ、－、Ａｓ、
Ｓｂ、－、（０、７≦ｘ＜１、０、７≦ｙ＜ｉ）ｖ（ＡＱ、Ｇａｌ－、
）ｙＩｎｘ－ｙＰ（０＜ｘ＜１、Ｏ＜ｙ＜１）。(A QmGal-, +) yIJ-yAS (0 <x <1, 0, 5 <y <IL (AQ, Ga,-)), In5-ysb (0,5 x <1 or-) 0 5 ≦ y <1 or 0.4 ≦ x <0, 5 and 0.6 ≦ y <1 or 0.3 ≦ x <0, 4 and 0.7 ≦ y <1 or 0.2 ≦ x <0, 3 and 0.8 ≦ y 1) In (P, As,), 5b1-, (0, 6 ≦ x 1), one can be selected.

GF Exhibit 1124 - 1758/2704

The energy gap EII of these semiconductors satisfies the above-mentioned relational expression E1 ≧ −E, l with respect to GaAs (energy gap E, '= 1.4 eV). Further, in the present embodiment, GaAs was used as the ■-■ group semiconductor, but in addition to this, it is also possible to use a ■ -V group semi-specialized body such as InP, AQ GaAs, InGaAsw ■ mouth GaAsP. In particular, for InP, this energy gap is 1.3 eV, so that all the semiconductors listed above are suitable for the gate electrode. Moreover, it is not limited to the ■-■ group semiconductors, and it is possible to use Sly (ro). Example 2 Main steps are shown in FIGS. 5 (a) to 5 (d). This embodiment is characterized by the step of forming the n3 layer in a self-aligned manner by using the Si film used as the gate 1'a electrode as a mask. 6 Fig. 5 (a) Two-hand insulating GaAst treatment 50, 21 SL The 0 layer 51 is formed by the selective ion implantation method of b. Then, with the SiO 2 film 5; 3 deposited on the surface, high temperature heat treatment was performed to activate it. The implantation conditions for 211 Sili are an implantation energy of 75 keV and a dose amount of 3 X 10 "am-". The thickness of S i O2 [53 was 2000 people and was deposited by the CVD method. The high temperature heat treatment was performed at 800 ° C. for 20 minutes in an H 2 atmosphere. FIG. 4 (b): After the SiO □ film 53 is removed, Sx pancreas 55 doped with boron as an impurity by plasma (, ▪ D method) is deposited, and then by a sputtering method, a W film 56 '! Lid deposited. Then, after patterning with Photolith 1-, the W film 56 and the Si film 55 were processed by dry etching with a mixed gas of CF4 and 02 to form a Goo 1-electrode. Here, the film thickness of the Sl film 55 was set to 3000 and the film thickness of the W film 56 was set to 1000, but the combined film thickness of these two layers is the ion of the Si film to be used later in n “layer formation”. It is determined according to the driving energy. Further, the film thickness of the Si film 55 may be at least 50 in order to function as a gate electrode. As described in the first embodiment, a natural oxide film is formed on the surface of the 0 layer 51- at a 1-0 boundary level. Therefore, the interface level layer 54 is formed at the interface between the 0 layer 51 and the Si film 55. The manufacturing conditions for 5il1955 are the same as in Example 1. FIG. 5 (c): Using the two-layer film of the Si film 55 and the W film 56 as a mask, "the Si film was selectively ion-implanted, and the region adjacent to the gate 1 was set to n" '-GiAsM52.

At this time, two layers! Under the itt of I9 is rrh, and for 24S 3. + Is not driven in. After that, the n ″ layer 52 was activated again by high-temperature treatment with 200 (one person's S10 film 57-coated spasticity). 2 ″ 'S ;, under the conditions of “implantation”, the implantation energy is 150 keV, the dose is tlX1013clQ-2, and the high temperature heat treatment is 800 ° C. It was carried out in an H1 atmosphere for 20 minutes. By this high temperature heat treatment, the Si film 55 is converted into polycrystal and the boron contained in the pancreas is electrically activated. As a result, the Si film 55 became a polycrystalline film having p-type conductivity, and the concentration of electrically active boron was 10 ″ l ″ ″. FIG. 5 (d): An electrical contact pattern by a photoresist. After forming the pattern, the S10 i film 57 of the pattern part is removed, and AuGe / N i / A 1. J was deposited on the entire surface and

GF Exhibit 1124 - 1759/2704

unnecessary metal was removed together with the photoresist (riff] -off method) to form source / drain electrodes 58.59. If the metal deposition v is thick, it is AuGc600A, Ni 100 people, Au 800 people. After that, 400 ° C. Heat treatment was performed in an H □ atmosphere for 3 minutes. このとき。 An ohmic contact is made to the n0 layer 52 of the source / drain. Although the gate structure of this embodiment is the same as that of the first embodiment, in particular, according to this embodiment, the n ″ ″ layer between the gate, the source and the train is formed with a high dose of IX 1013am− ″ , The parasitic resistance was reduced, and a current that was four times or more that of the conventional MISFET could flow. Also, mutual conductance of 540 ms / rm was obtained. Also in this embodiment, it is possible to use a semiconductor as the gate electrode as listed in the first embodiment. In the case where the group 1- to 6 group semiconductor is used for the gate electrode, the high temperature heat treatment step of FIG. 4 (e) can be omitted in the device in which the n "layer 52 is not provided in self alignment with the gate as in the first embodiment. Because, for example, when the person αGa ^ 3 is used as the gate fa pole. This is because it is usually possible to grow by the MOCVD method or the MBE method, and according to these methods, the film is already polycrystal or single crystal at the time of growth. However, in the device in which the n0 layer 52 is self-aligned with the gate as in the present embodiment, the high temperature heat treatment step cannot be omitted (FIG. 5 (c)), that is, AQ'GaAs or the like is used for the gate electrode. When using a group (1)-(6) group semiconductor, the impurities that are doped to make the gate electrode have P-type conductivity can serve as acceptors for GaAs.

Therefore, due to the high temperature heat treatment for activating the n0 layer included in the step of FIG. 5C, the impurities in the gate tI & the electrode diffuse to the GaAs side, which causes the carrier concentration of the n-GaAs layer 51 to change. .. Such a variation is fatal to the manufacture of a highly integrated circuit in which it is generally important to realize the gear rear concentration control at M '/ l. However, when the Si film is used for the gate (-electrode) as in this example, the impurities doped to 5 illi are group III elements such as boron and gallium, and do not serve as acceptors or donors in GaAs. Therefore, even if the high temperature heat treatment is performed, it does not cause a change in the key X7 rear concentration. Therefore, in the element using the <tO-V group semiconductor substrate as in the present embodiment and finishing the high temperature heat treatment step, the Si film is particularly It is useful. Example 3 Main steps are shown in FIGS. 6 (a) to 6 (d). FIG. 6 (a): A state in which n) fl 21 and n ” 122 are formed on the semi-absolute GaAs substrate 20 by the selective ion implantation method of “ Si ”, and then SiOz lli 23 is adhered to the surface. High temperature heat treatment (800 ° C. The activation conditions of 2 # Si + activated by performing 20 minutes) are as follows: n layer 21 has an implant energy of 75 ksV, dose amount 3 X i O "am-2, and n0 layer 22 has an implant energy of 150 keV. The dose filter 'XIQia,-, the thickness of the 5 in 2 film 23 is 2000 persons, and it was deposited by the CVD (Che + m1ca-i VaporDeposition) method. High temperature heat treatment is 800 ° C. It was carried out in a H2 atmosphere for 20 minutes. FIG. 6B: Sin used for the high temperature heat treatment, and the gate portion of the film 23 was removed by

GF Exhibit 1124 - 1760/2704

etching. After that, it was exposed to the air for a long time, and after forming the interface level layer 24 of a natural oxide film of GaAs with a thickness of 10 people, only the removed region was degenerated by MOCVD (Metal Organicqhs +++ 1cal cal Vapor Deposition) method. The impurity concentration of m-p-Ga5.tAQo and 3AF4 layer 25 obtained by selective epitaxial growth of the -1AQ6 and 3As layer 25 was set to three 1.0 "to 1021Qll" in order to satisfy the degeneracy condition. The impurity used at this time is Zn. Since the growth temperature by the MOCVD method was set to 680 ° C., P Gas, tA n 6 and the n layer directly under the As layer 25 were completely compensated by diffusion by Zn to become the p-GAAs layer 26. After removing the SiO film, it was exposed to the air for a long time and a natural oxide film of GaAs with a high density level in the band gap of GaAs was formed on the surface of the GaAs substrate for about 10 people. Since p-Ga, ..., AQll, and 3As layers were grown, PGa ++, iAQ, 0.

A high-density interface state layer 24 is formed at the interface between the As layer 25 and the p-GaAs7fl2F3. FIG. 6 (c): AuGa / Nj / Au was deposited in this order on 600 people, 100 people, and 800 people, and the metal in the region other than the gate portion was removed by the ion milling method to form the gate electrode 27. No. 614 (d): After forming the electrode pattern with the photoresist, the SiO □ film of the pattern part is removed, AuGe / Ni / Au is deposited on the entire surface, and unnecessary metal is removed together with the photoresist (Riff 1 to off Method) The deposited film thickness of the metal on which the source / drain electrodes 28.29 are formed is 600 AuGa and 100 Ni. There are 800 Au. After that, 400 ° C for 3 minutes. The heat treatment was performed with IL2 '+' lJ # width. At this time, along with ohmic contact to the fourth layer 22, P Ga11. .. AQ „ Ohmic contact to the As layer 25 is realized. According to this example, p Ga. , 7 A Q l, 3 An electron inversion layer is easily formed at the interface between the As layer and the P-GaAs layer with a gate voltage of 0.8 v or more, and is three times or more the same gate voltage as the conventional MISFET. An electric current could be passed, and a transconductance g- =400 m510n was obtained. At the same time, the improvement effect that the charge / discharge time of the interface state is short and the frequency dependence of the mutual conductance and the capacity is reduced was also confirmed. In this embodiment, both the Ga, tAQO,) As layer and the GaAs layer, which are gate electrodes, are D-type, and the semiconductor between the gate and the source or drain is D-type. In the opposite case, that is, when the Ga, 1, A, AQ, 3As layers and GaAs layers that are gate electrodes are both D-type and the semiconductor between the gate and the source or train is P-type, A hole inversion layer was formed and a large current could be passed. Also, in this example, the degenerate Gag, 7AQg, and 3 layers of 9 layers were used as the gate electrode, but in addition to this, it is also possible to use the Si layer or the semiconductors enumerated in Example J-. .. It goes without saying that, instead of GaAs used for the substrate, III-V group semiconductors such as InP, AQ GaAs, InGaAsP InGaAsP or Si, Ge can be used. As described above, according to the present invention, the inversion layer or the storage layer is easily formed at the interface between the degenerated semiconductor and the semiconductor i ´ : It is possible to flow a current more than twice as much, and there is an effect that the FE "I" can be

GF Exhibit 1124 - 1761/2704

speeded up.

[0002]
Brief description of the drawings

[0003]

FIG. 1 (a) is a structural cross-sectional view of a MISFET, and FIG. 1 (b) is a band cross-sectional structural view along the line A-A '.

FIG. 2 (a) is a structural sectional view of the FET according to the present invention, and FIG. 2 (b) is a band structure diagram of a B-B ″ sectional view. FIG. 3 (a) is a structural sectional view of the FET according to the present invention. FIG. 3B is a band structure diagram of a B-B ″ cross section. 4 to 6 are sectional views of the device according to the manufacturing process as one embodiment of the FET according to the present invention. 9 ... Semi-insulating semiconductor substrate, 1o ... n-type semiconductor layer, 11 ... p-type group ■-■ group semiconductor layer, 12 ... interface level layer. 13 ... Degenerate P-type Si layer (gate), 14 ... Source electrode, 15 ... Drain electrode, 40 ... Semi-insulating semiconductor substrate, 41 ... High-concentration n-type semiconductor layer, 42 ... n-type m-v group semiconductor layer, 43 ... interface level layer, 44 ... degenerate p-type Si layer (gate), 45 ... source number / ll (shi] vys>. Early 2 mouths (a-) (b) and 9s> O 3rd country (α) (b) V O> 0 4th mouth 4th! 5 mouth (d)

GF Exhibit 1124 - 1762/2704

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

CLAIMS JPS6261363

1.
A control means having at least an interface level layer on the electrically conductive III-V group first semiconductor region and a second semiconductor layer made of single crystal or polycrystalline Si on the interface level layer; At least a carrier transmission / reception means sandwiching a control means is provided, and the interface level layer causes the Fermi level of the second semiconductor layer to be pinned to the Fermi level of the interface level layer. A semiconductor device characterized by being formed. 2. The interface level layer has an interface level of 10 ^ 1 ^ 2 / cm ^ 2 / eV or more at a position corresponding to an energy gap of the first semiconductor layer. The semiconductor device according to the paragraph. 3. The semiconductor device according to claim 1 or 2, wherein the interface level layer has a thickness of 30 Å or less. 4. The semiconductor device according to any one of claims 1 to 3, wherein the second semiconductor layer is made of a degenerate semiconductor. 5. The size of the energy band gap between the edge of the energy band at the interface where minority carriers exist in the first semiconductor layer and the edge of the energy band where majority carriers exist in the second semiconductor layer The conductivity of the semiconductor layer is larger than that of the first semiconductor layer, and has the same conductivity as that of the first semiconductor layer. The semiconductor device according to any one of claims 1 to 4, characterized in that: 6. The size of the energy band gap between the edge of the energy band at the interface where majority carriers exist in the first semiconductor layer and the edge of the energy band where majority carriers exist in the second semiconductor layer The conductivity of the semiconductor layer between the control means and the carrier transfer means is the same as that of the fifth term. The semiconductor device according to any one of claims 1 to 4, which is characterized.

GF Exhibit 1124 - 1763/2704

⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　昭61－133646

⑤1Int.Cl.⁴	識別記号	庁内整理番号	⑬公開　昭和61年(1986)6月20日
H 01 L 21/88		6708－5F	
21/28		7638－5F	

審査請求　有　発明の数 1　（全4頁）

⑤4発明の名称　半導体装置の製造方法

⑳特　願　昭59－255500

㉒出　願　昭59(1984)12月3日

⑦2発明者　嶋　昇平　川崎市幸区小向東芝町1　株式会社東芝総合研究所内

⑦2発明者　守屋　孝彦　川崎市幸区小向東芝町1　株式会社東芝総合研究所内

⑦1出願人　株式会社東芝　川崎市幸区堀川町72番地

⑦4代理人　弁理士　木村　高久

明　細　書

1. 発明の名称

半導体装置の製造方法

2. 特許請求の範囲

(1) 半導体層を有する基板上に形成された絶縁膜上に、障壁金属層を介して該半導体層に電気的に接続される電極配線層を形成する方法であって、

前記絶縁膜に対し、前記半導体層へのコンタクト用窓明けを行なう穿孔工程の後、前記障壁金属層および電極配線層の形成工程に先立ち、形成された前記コンタクト用窓内に気相成長法により高融点金属を選択的に被着する工程とを備えたことを特徴とする半導体装置の製造方法。

(2) 障壁金属層は、半導体層と電極配線層の界面反応を防ぐものであることを特徴とする特許請求の範囲第(1)項に記載した半導体装置の製造方法。

3. 発明の詳細な説明

〔発明の技術分野〕

本発明は、半導体装置の製造方法に係り、特に、半導体基板上に形成された拡散層領域と配線層との間に高い信頼性をもつ微細面積のコンタクト電極を形成する方法に関する。

〔発明の技術的背景とその問題点〕

半導体装置の分野では、１９７０年代以降、特に、高集積化への傾向は強まる一方となり、超大規模集積回路（超ＬＳＩ）へと進歩し、１つの半導体チップ上にコンピュータ等のシステムが構成されるまでになってきている。

ところで集積回路の高速化と高集積化は素子の微細化によって実現される。例えばＭＯＳ集積回路では、素子の微細化に伴い、多結晶シリコンゲート電極や、ソース拡散層、ドレイン拡散層等と金属配線層との間で電気的接続を行うためのコンタクト部の面積は縮小されると共にＰＮ接合の深さについても浅くなるように形成されることが必要となってくる。

しかしながら、コンタクト面積の縮小化あるい

GF Exhibit 1124 - 1764/2704

はＰＮ接合が浅く形成されるのに伴い、配線材料としてアルミニウムーシリコン合金を用いた場合においても、アルミニウム中に含まれる過剰シリコンの析出によるコンタクト抵抗の増加や浅いＰＮ接合の破壊等の問題が顕在化してくる。特に超ＬＳＩの場合、数ミリ角のシリコンチップ１個当たり、百万個以上のコンタクトが存在するため、このような接続特性の劣化は素子の信頼性の低下につながり、集積回路の高速化、高集積化への大きな障害となっている。

例えば、第５図に示す如くＰ型のシリコン（Ｓｉ）基板21内に砒素（Ａｓ）イオンをイオン注入して形成されたＰＮ接合の深さ $X=0.1\ \mu m$ となるような N^+ 型のシリコン拡散層22に対し、絶縁膜23内に穿孔されたコンタクト窓24を介してアルミニウム（Ａℓ）電極25を形成した場合、該 N^+ 型のシリコン拡散層22とアルミニウム電極25の間でシリコンとアルミニウムの相互作用に基づく界面反応によって前記ＰＮ接合部がショートすることがある。

（３）

なる。このように、バリヤーメタルを形成したにもかかわらずバリヤー効果がなくなり、アルミニウム層25と N^+ 型のシリコン拡散層22とが反応して第７図に示す如く、N^+ 型シリコンがアルミニウム層中へ溶け出し、シリコン原子の放出路にアルミニウムがくさび状に浸入することがあった。これは、拡散層の突き抜け27と呼ばれ、接合破壊の原因となっていた。

また、スパッタリング法によってバリヤーメタルを形成する場合、拡散層表面に、シリコンの自然酸化膜が生成され、接触抵抗が高くなるという問題があった。この問題を解決するため、バリヤーメタルの形成に先立ち、アルゴンイオン等を用いたスパッタエッチングによるシリコン自然酸化膜のクリーニング工程を付加するというような技術も提案されてはいるが、スパッタリングによるダメージあるいは装置内におけるデバイスの汚染等の問題を依然として残している。

このように、スパッタリング法によってバリヤーメタルを形成する方法では、接触抵抗が充分に

（５）

このような問題を解決する技術として、前記 N^+ 型のシリコン拡散層22とアルミニウム電極25との間に前述の如き界面反応が発生するのを防止するため、障壁金属（バリヤーメタル）を形成する方法が注目されている。

この方法は、例えば第６図に示す如く、Ｐ型のシリコン基板21内に形成された N^+ 型のシリコン拡散層22に対応する位置にコンタクト窓24を有するような絶縁層23を形成した後、コンタクト電極25としてのアルミニウム層の形成に先立ち、スパッタリング法により、全面にバリヤーメタルとして窒化チタン膜26を形成しようというものであるが、この方法は、また以下に述べるような欠点を有している。

すなわち、通常のスパッタリング法により、バリヤーメタルを形成した場合、コンタクト窓24の周囲におけるバリヤーメタルの膜厚は、平坦部では 500～1000 Åであるのに対し、その $\frac{1}{10}\sim\frac{1}{2}$ と薄くなる上、この部分でバリヤーメタルの膜応力による歪が集中して膜にクラックが発生し易く

（４）

低く、素子としての信頼性の高いコンタクト電極を実現するには、多くの問題があり、実用化は困難な状態であった。

〔発明の目的〕

本発明は、前記実情に鑑みてなされたもので、微細でかつ浅い半導体層（拡散層）をもつ基板に対しても、接合特性を劣化させることなく、配線層と半導体層（拡散層）との間に、低抵抗でかつ信頼性の高いオーミックコンタクトを形成することを目的とする。

〔発明の概要〕

そこで、本発明の方法では、拡散層等の半導体層を有する基板の表面に形成された絶縁膜上にコンタクト窓を形成した後、まず、気相成長法により該コンタクト窓内に露呈する基板の表面に選択的に高融点金属を形成し、この後、バリヤーメタル、配線層を順次形成するようにしている。

〔発明の効果〕

すなわち、拡散層（半導体層）に対するコンタクト窓を穿孔した後、スパッタリング法によりバ

（６）

GF Exhibit 1124 - 1765/2704

リヤーメタルを形成するに先立ち、金属化合物ガスを用いた高融点金属の気相成長工程を導入することにより、基板表面を覆う絶縁膜に形成されたコンタクト窓内にのみ選択的に高融点金属膜が析出せしめられ、コンタクト窓の存在による段差が緩和されるため、バリヤーメタルの膜厚が薄くなる部分がほとんどなくなり、ほぼ均一な膜厚のバリヤーメタルが形成され、拡散層（半導体層）の突き抜けによる接合破壊はほとんど皆無となる。

また、気相成長法によって高融点金属膜が形成される際に、半導体層（拡散層）と反応し、高融点金属が成長せしめられるという過程をとるため、基板表面上の自然酸化膜は完全に除去され、極めて低抵抗のオーミックコンタクトが実現可能となる。

このように、本発明の方法によれば、微細でかつ浅い拡散層をもつ基板に対し、低抵抗でかつ極めて信頼性の高い、拡散層へのオーミックコンタクトの形成が可能となる。

〔発明の実施例〕

（7）

ン（WF_6）とアルゴン（Ar）との混合ガスを用いた気相成長法により、高融点金属被膜としてタングステン（W）膜5を前記コンタクト窓3内に露呈するN^+型のシリコン拡散層2上にのみ選択的に形成する。形成条件としては、基板温度は250～450℃、反応炉内の圧力は1×10^{-2}～760Torr、六弗化タングステンガスの分圧は1×10^{-4}～5×10^{-2}の範囲にとるのが望ましい。また、膜厚は200～1000Åとするのが望ましい。

この後、スパッタリング法により、バリヤーメタルとして窒化チタン膜（TiN）6を通常の形成条件で、膜厚500～1000Åとなるように形成する。（第4図）

そして最後に、コンタクト用電極および電極配線層としてのアルミニウム膜7を形成し、第1図に示したような半導体装置が完成する。

このようにして形成されたコンタクト用電極は、N^+型シリコン拡散層上に自然酸化膜が残留していない状態で被着せしめられたタングステン膜上に、バリヤーメタルとしての窒化チタン膜を介し

（9）

以下、本発明の実施例を、図面を参照しつつ詳細に説明する。第1図に示すのは、本発明の一実施例の方法によって形成された半導体装置の構造を示すもので、P型のシリコン基板1内のN^+型のシリコン拡散層2に対応する部分にコンタクト窓3を有する絶縁膜4が形成されており、このコンタクト窓3内に高融点金属層としてタングステン膜5が形成され、この上膜にバリヤーメタルとしての窒化チタン膜6、そして電極配線層としてのアルミニウム膜7が順次形成されている。

次に、かかる構造の半導体装置の形成方法を説明する。まず、第2図に示す如く、P型のシリコン基板1上に砒素（As）をイオン注入することによって形成されたPN接合深さ$X=0.1\,\mu m$のN^+型のシリコン拡散層2の表面全体に絶縁膜として酸化シリコン膜4を堆積し、これにフォトリソエッチング法等により、コンタクト窓3を穿孔する。（このときのエッチングは、反応性イオンエッチングを用いて行なう。）

次いで、第3図に示す如く、六弗化タングステ

（8）

て形成されているため、コンタクト抵抗が低く抑えられる。すなわち、タングステン膜の成長は、N^+型のシリコン拡散層表面におけるシリコンとの反応によって進むため、前記自然酸化膜は完全に除去された状態でタングステン膜が被着せしめられており、コンタクト電極部が$1.0\,\mu m$口以下の微細なものについても、コンタクト抵抗を数十Ω程度におさえることができる。

また、バリヤーメタルとしての窒化チタン膜をスパッタリング法によって形成するに際しても、その下層のタングステン膜が均一な膜厚でコンタクト窓内に充填されているため、コンタクト窓による段差が緩和され、ほぼ均一な膜厚の窒化チタン膜が形成し得ることになり、充分なバリヤー効果を有するため、コンタクト電極としてのアルミニウム膜と拡散層との間に相互作用が生じることもなく、デバイスとしての信頼性は極めて高いものとなる。

なお、実施例においては、コンタクト窓内に形成する高融点被膜として、六弗化タングステンを

（10）

GF Exhibit 1124 - 1766/2704

反応ガスとして用いた気相成長法によって形成されるタングステン膜を用いたが、反応ガスとして、塩化タングステンWCl_6等の他のタングステン化合物を用いて形成されるタングステン膜を用いたり、更には、モリブデン（Mo）、ニオブ（Nb）、タンタル（Ta）、チタン（Ti）の弗化物、塩化物等による気相成長膜等から選択したものを使用してもよい。

また、実施例においては、バリヤーメタルとして窒化チタン膜を用いたが、その他窒化タンタル、窒化ハフニウムを用いてもよいことはいうまでもない。

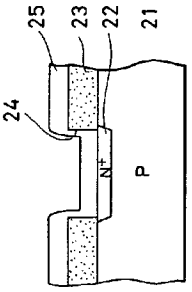
4. 図面の簡単な説明

第1図は、本発明実施例の方法によって形成された半導体装置のコンタクト部を示す図、第2図乃至第4図は、同装置の製造工程を示す図、第5図乃至第7図は、従来例を示す図である。

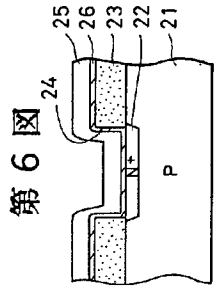
1…シリコン基板、2…シリコン拡散層、3…コンタクト窓、4…酸化シリコン膜、5…タングステン膜、6…窒化チタン膜、7…アルミニウム膜、21…シリコン基板、22…シリコン拡散層、23…絶縁膜、24…コンタクト窓、25…アルミニウム電極、26…窒化チタン膜。

出願人代理人　木　村　高　久

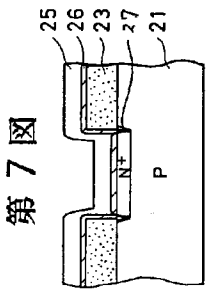
第5図



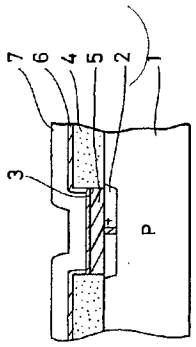
第6図



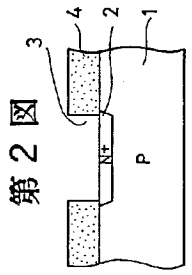
第7図



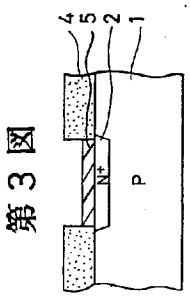
第1図



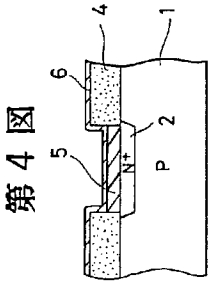
第2図



第3図



第4図



GF Exhibit 1124 - 1767/2704

Europäisches Patentamt
European Patent Office
Office européen des brevets

Espacenet

JPS61133646A MANUFACTURE OF SEMICONDUCTOR DEVICE

Applicants: TOSHIBA CORP

Inventors: MORIYA TAKAHIKO,SHIMA SHOHEI

Classifications:
IPC ***H01L21/28; H01L21/768;*** (IPC1-7): H01L21/28;

Priorities: JP25550084A 1984-12-03

Application: JPS61133646A·1984-12-03

Publication: JPS61133646A·1986-06-20

Published as: JPS61133646A

MANUFACTURE OF SEMICONDUCTOR DEVICE

Abstract

PURPOSE:To obtain highly reliable ohmic contact, by forming a high-melting- point metal on the surface of a substrate, which is exposed in a contact window, and forming a barrier metal and a wiring layer.
CONSTITUTION:As ions are implanted in a P type silicon substrate, and an N<+> type silicon diffused layer 2 is formed. Then, a silicon oxide film 4 is deposited on the surface. Thereafter, a contact window 3 is formed. Then, a tungsten film 5 as a high-melting-point metal film is formed on the layer 2. Thereafter a titanium nitride film 6 as a barrier metal is formed. Then, an aluminum film 7 as a contact electrode and a wiring layer is formed.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION JPS61133646

[0001]

TECHNICAL FIELD OF THE INVENTION The present invention relates to a method for manufacturing a semiconductor device, and more particularly, to forming a highly reliable contact electrode having a fine area between a diffusion layer region formed on a semiconductor substrate and a wiring layer. Regarding the method. [Technical Background of the Invention and Problems Thereof] In the field of semiconductor devices, the tendency toward high integration has been increasing especially since the 1970's, and the progress toward ultra-large-scale integrated circuits (ultra-LSI) has made it one semiconductor. A system such as a computer is being constructed on a chip. By the way, high speed and high integration of an integrated circuit are realized by miniaturization of elements. For example, in an MO8 integrated circuit, the area of a contact portion for making electrical connection between a polycrystalline silicon gate electrode, a source diffusion layer, a drain diffusion layer, and the like and a metal wiring layer is reduced with the miniaturization of elements. In addition, the PN junction needs to be formed so as to have a shallow depth. However, when the contact surface line is reduced or the PN junction is formed shallow, even when an aluminum-silicon alloy is used as the wiring material, the contact resistance increases or the depth is shallow due to the precipitation of excess silicon contained in aluminum. Problems such as destruction of the PN junction become apparent. In particular, in the case of an ultra-LSI, there are more than 1 million contacts per 211 mm square sili- lantich, so such deterioration of the connection characteristics leads to a decrease in the reliability of the element, which results in higher speed and It is a major obstacle to integration. For example, as shown in FIG. 5, a P + type silicon (8i) substrate 21 is formed of an N + type such that the depth X of a PN junction formed by implanting arsenic (As) ions is 0.1 μ. When the aluminum (A1) electrode 5 is formed on the silicon diffusion layer η through the contact window holes perforated in the insulating film n, silicon and aluminum are formed between the N + type silicon diffusion layer n and the aluminum electrode 5. The PN junction may be short-

GF Exhibit 1124 - 1769/2704

circuited due to an interfacial reaction based on the interaction of the above. As a technique for solving such a problem, a method of forming a barrier metal (barrier metal) in order to prevent the above-mentioned interfacial reaction between the N + type silicon diffusion layer n and the aluminum electrode 5 from occurring. Is getting attention. This method is, for example, as shown in FIG. 6, after forming an insulating layer portion having a contact window U at a position corresponding to the N + type silicon diffusion layer B formed in the P type silicon substrate 21, Prior to forming the aluminum layer as the contact electrode 5, a titanium nitride film is formed as a barrier metal on the entire surface by a sputtering method, but this method also has the following drawbacks. .

That is, when the barrier metal is formed by the normal sputtering method, the film thickness of the barrier metal around the contact window row becomes thinner at the flat portion, and the strain due to the film stress of the barrier metal concentrates at this portion. The film is likely to be cracked. In this way, despite the formation of the barrier metal, the barrier effect disappears and the aluminum layer reacts with the N + type silicon diffusion layer to dissolve the N + type silicon into the aluminum layer as shown in FIG. In some cases, aluminum was wedged out into the discharge path of silicon atoms. This was called the punch-out of the diffusion layer and was the cause of junction failure. Further, when the barrier metal is formed by the sputtering method, there is a problem that a natural oxide film of silicon is formed on the surface of the diffusion layer and the contact resistance increases. In order to solve this problem, a technique of adding a cleaning process of the silicon natural oxide film by sputter etching using argon ions or the like before forming the barrier metal has been proposed, but damage or damage caused by sputtering However, there still remain problems such as device contamination within the company. As described above, in the method of forming a barrier metal by the sputtering method, contact resistance is sufficiently low, and there are many problems in realizing a highly reliable contact electrode as an element. there were. [Object of the Invention] The present invention has been made in view of the above-mentioned circumstances, and even for a substrate having a fine and shallow semiconductor layer (diffusion layer), a wiring layer and a semiconductor layer can be formed without deteriorating the bonding characteristics. The purpose is to form a highly reliable ohmic contact with the (diffusion layer). SUMMARY OF THE INVENTION Therefore, in the method of the present invention, after forming a contact window on an insulating film formed on the surface of a substrate having a semiconductor layer such as a diffusion layer, first, the inside of the contact window is formed by vapor phase epitaxy. The refractory metal is selectively formed on the surface of the substrate exposed to the outside, and then the barrier metal and the wiring layer are sequentially formed. [Advantages of the Invention] That is, after the contact window for the diffusion layer (semiconductor layer) is punched, a vapor phase growth step of a refractory metal using a metal compound gas is introduced before forming a barrier metal by a sputtering method. By this, the refractory metal film is selectively deposited only in the contact window formed in the insulating film covering the substrate surface, and the step due to the existence of the contact window is mitigated, so that the barrier metal film thickness is reduced.

GF Exhibit 1124 - 1770/2704

Is almost eliminated, and a barrier metal having a substantially uniform film thickness is formed, and there is almost no junction breakdown due to penetration of the diffusion layer (semiconductor layer).

Also, when the refractory metal film is formed by the vapor phase growth method, the refractory metal reacts with the semiconductor layer (diffusion layer) to grow the refractory metal, so that the natural oxide film on the substrate surface is completely removed. It is possible to realize an ohmic contact with extremely low resistance. As described above, according to the method of the present invention, it is possible to form an ohmic contact with a diffusion layer having low resistance and extremely high reliability on a substrate having a fine and shallow diffusion layer. Embodiments of the Invention Embodiments of the present invention will be described in detail below with reference to the drawings. FIG. 1 shows the structure of a semiconductor device formed by the method of one embodiment of the present invention, in which a portion corresponding to an N + type silicon diffusion layer 2 in a P type silicon substrate 1 is contacted. An insulating film 4 having a window 3 is formed, a tungsten film 5 is formed in the contact window 3 as a refractory metal layer, and a titanium nitride film 6 as a barrier metal and an electrode wiring layer as a barrier metal are formed on the tungsten film 5. The aluminum film 7 is sequentially formed. Next, a method of forming a semiconductor device having such a structure will be described. First, as shown in FIG. 2, a surface metal body of an N + type silicon diffusion layer 20 having a PN junction depth X = 0.1 μm formed by ion-implanting arsenic (AS) on a P type silicon substrate 1. Then, a silicon oxide film 4 is deposited as an insulating film, and a contact window 3 is perforated by a photolithography method or the like. (At this time, etching is performed using reactive ion etching.) Then, as shown in FIG. 3, the tungsten (W) film 5 as a refractory metal film is formed on the contact window by a vapor phase growth method using a mixed gas of tungsten hexafluoride (WF6) and argon (Ar). It is selectively formed only on the N + type silicon diffusion layer 2 exposed in the inside 3. As the formation conditions, the substrate temperature is 250 to 450 ″ O, and the pressure in the reaction furnace is 1 × 10 −2 to 760 ° rr. The partial pressure of the tungsten hexafluoride gas is preferably in the range of IX 10- 'to 5 × 10-2. The film thickness is preferably 200 to 1000; Thereafter, a titanium nitride film (TiN) 6 is formed as a barrier metal by a sputtering method under normal forming conditions so as to have a film thickness of 500 to 1000 A. (FIG. 4) And finally, the aluminum film 7 as a contact electrode and an electrode wiring layer is formed, and the semiconductor device as shown in FIG. 1 is completed. The contact electrode thus formed has a tungsten film deposited on the N + type silicon diffusion layer in a state where no natural oxide film remains, and a titanium nitride film as a barrier metal is interposed therebetween.), The contact resistance can be kept low.

That is, since the growth of the tungsten film proceeds by the reaction with silicon on the surface of the N + type silicon diffusion layer, the tungsten film is deposited with the natural oxide film completely removed, and the contact electrode portion is The contact resistance can be

GF Exhibit 1124 - 1771/2704

suppressed to about several tens of Ω even for a fine one having a diameter of 1.0 μm or less. Further, even when the titanium nitride film as the barrier metal is formed by the sputtering method, the tungsten film as the lower layer is filled in the contact window with a uniform thickness, so that the step due to the contact window is relaxed, and the unevenness is almost uniform. Since a titanium nitride film having a large thickness can be formed and has a sufficient barrier effect, no interaction occurs between the aluminum film as the contact electrode and the diffusion layer, and the reliability as a device is high. It will be extremely expensive. In the examples, a tungsten film formed by a vapor phase growth method using tungsten hexafluoride as a reaction gas was used as the high melting point film formed in the contact window. A tungsten film formed by using another tungsten compound such as No. 6 is used. You may use what was selected from the phase growth film etc. Further, in the embodiment, the titanium nitride film is used as the barrier metal, but it is needless to say that tantalum carbide and hafnium nitride may be used.

[0002]
Brief description of the drawings

[0003]

FIG. 1 is a diagram showing a contact portion of a semiconductor device formed by the method of an embodiment of the present invention, FIGS. 2 to 4 are diagrams showing a manufacturing process of the device, and FIGS. FIG. 7 is a diagram showing a conventional example.

1 ... Silicon substrate, 2 ... Silicon diffusion layer, 3 ... Contact window, 4 ... Silicon oxide film, 5 ... Tungsten film, 6 ... Titanium nitride film, 7 ... Aluminum A film, 21 ... Silicon substrate, n ... Silicon diffusion layer, n ... Insulating film, U ... Contact window, 5 ... Aluminum electrode, 26 ... Titanium nitride film.

GF Exhibit 1124 - 1772/2704

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

CLAIMS JPS61133646

1.

A method of forming an electrode wiring layer electrically connected to the semiconductor layer via a barrier metal layer on an insulating film formed on a substrate having a layer, the method comprising: After the perforation step of opening a contact window to the above, prior to the step of forming the barrier metal layer and the electrode wiring layer, a refractory metal is selectively deposited in the formed contact window by vapor phase epitaxy. A method of manufacturing a semiconductor device, comprising: (2) The method for manufacturing a semiconductor device according to claim (1), wherein the barrier metal layer prevents an interface reaction between the semiconductor layer and the electrode wiring layer.

GF Exhibit 1124 - 1773/2704

⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　昭63－157466

⑤Int.Cl.⁴　識別記号　庁内整理番号　⑬公開　昭和63年(1988)6月30日

H 01 L 29/48
// H 01 L 29/91　B－7638－5F

審査請求　未請求　発明の数 1　（全5頁）

⑭発明の名称　ショットキーバリアダイオード

⑳特　願　昭61－304462
㉒出　願　昭61(1986)12月20日

⑫発明者　藤田　一朗　神奈川県川崎市中原区上小田中1015番地　富士通株式会社内
⑫発明者　角田　一夫　神奈川県川崎市中原区上小田中1015番地　富士通株式会社内
⑫発明者　上嶋　才史　神奈川県川崎市中原区上小田中1015番地　富士通株式会社内
⑪出願人　富士通株式会社　神奈川県川崎市中原区上小田中1015番地
⑭代理人　弁理士　井桁　貞一

明細書

1.発明の名称

ショットキーバリアダイオード

2.特許請求の範囲

(1)半導体基板（2）上のエピタキシャル層（3）と金属層（5）との間の界面層（21a）を、窒化チタン（22）及び／又は酸化チタン（23）を所定量含有した組成としてなることを特徴とするショットキーバリアダイオード。

(2)上記界面層（21a）は、アルゴンガスに所望量の窒素及び／又は酸素を混合してなる混合ガスを使用してチタンをスパッタリングすることにより形成されてなることを特徴とする特許請求の範囲第1項記載のショットキーバリアダイオード。

3.発明の詳細な説明

（概要）

本発明はショットキーバリアダイオードおいて、アルミニウムとシリコンとの界面に窒化チタン及び／又は酸化チタンを一部介在させ、製造工程の種々の要因により影響されずに、所望の順方向電流－電圧特性を再現性良く得ることが出来るようにしたものである。

（産業上の利用分野）

本発明はショットキーバリアダイオードに係り、特に金属層とエピタキシャル層との界面に関する。

（従来の技術）

ショットキーバリアダイオードにおいて、順方向電流（I_F）－電圧（V_F）特性は重要であり、ばらつきの少ないことが要求される。

このダイオードをTTL回路に組み込んで使用する場合には動作速度が速いことが必要である。

動作速度はV_Fが低い程速いため、上記のダイオードでは、バリアハイトΦ_bが小さいTiをバリアメタルとして使用している。

第7図はこの種の従来のショットキーバリアダイオード1の一部を概略的に示す。同図中、2はシリコン基板、3はエピタキシャル成長層、4は絶縁層、5は導電メタルとしてのAℓ層、6はバ

GF Exhibit 1124 - 1774/2704

リアメタルである。バリアメタル6のうち符号6aで示す部分がエピタキシャル成長層3とAℓ層5との間の界面層を形成する。

界面層6a（バリアメタル6）は、×で示す$Ti_xAℓ_y$7と□で示すTi_xSi_y8とよりなる組成である。この界面層6aのバイリアハイトは$Φ_{b1}$であり、ダイオード1は第8図中線Ⅰで示すI_F-V_F特性を有する。

〔発明が解決しようとする問題点〕

ところで、このダイオード1は、第9図に示すように、絶縁層4に窓をあけ、厚さが約 100Åの Ti 膜9をスパッタリングで形成し、この上にAℓ層5を形成し、この後、図示はしないが、絶縁層とAℓ層とを交互に形成することにより製造される。

絶縁層及びAℓ層の形成過程で全体が加熱される。例えば絶縁層をPSGで形成したときには、420～ 450℃の熱が30分～1時間かゝる。

このTi 膜9形成後における製造工程における熱により、Ti 膜7のTiは、Aℓ及びSiと反応して前記の$Ti_xAℓ_y$7，Ti_xSi_y8となる。

各製造設備の間でのTi 膜7が受ける熱量のバラツキは避けられない。またTi膜7自体の質についても、スパッタリング装置間である程度ばらついてしまう。

熱がかゝり過ぎたときには、第10図に示すように$Ti_xAℓ_y$7の一部及びTi_xSi_y8の一部がAℓ層5及びエピタキシャル成長層3内に拡散し、界面層6aは薄くなる。これによりバリアハイトが増して$Φ_{b2}$となり、V_Fが高くなって、I_F-V_F特性は例えば線Ⅱで示すようになってしまい、所定のI_{F1}においてV_Fは所望の値より比較的大なる値$ΔV_F$違ってしまう。$ΔV_F$が大きいと、ダイオードは動作速度が遅くなりTTL回路に組み込むのに不適となり、不良品となってしまう。

上記のように従来のダイオードは、そのI_F-V_F特性が、製造過程で影響を受け易いという問題点があった。

〔問題点を解決するための手段〕

本発明は、半導体基板上のエピタキシャル層と金属層との間の界面層を、窒化チタン及び／又は酸化チタンを所望量含有した組成としてなるものである。

〔作用〕

上記の組成は、製造工程がばらついても、バリアハイトが影響されにくゝ、製造設備の違いによりI_F-V_F特性の違いを制限する。

〔実施例〕

第1図は本発明になるショットキーバリアダイオード20を示す。同図中、第7図に示す構成部分と対応する部分には同一符号を付しその説明を省略する。

21はバリアメタルであり、エピタキシャル成長層3とAℓ層5との間に介在している。このうち符号21aで示す部分が、エピタキシャル成長層3とAℓ層5との間の界面層を形成する。界面層21a（バリアメタル21）は、×で示す$Ti_xAℓ_y$7，□で示すTi_xSi_y8との他に○で示すTi_xN_y（窒化チタン）22及び△で示すTi_xO_y（酸化チタン）23を含んだ組成である。Ti_xN_y22及びTi_xO_y23の合計の含有量の全体に対する割合は20％以下であり、以下に述べるように制御されている。

第2図はTi 膜24をスパッタリングで形成した後の状態を示す。スパッタリングは、第3図に示すように、ArにN_2及びO_2を所定の微少量混入させた混合ガスのボンベ25を使用して行なう。例えばArにN_2が200ppM及びO_2が20ppM混入された混合ガスのボンベを使用する。第3図中、26は真空チャンバである。

この混合ガスを使用してスパッタリングを行なうことによりN_2，O_2がTiと反応し、

GF Exhibit 1124 - 1775/2704

Ti_xN_y，Ti_xO_yが生成し、Ti中にTi_xN_y22及びTi_xO_y23を含有する組成のTi膜24が形成される。

Ti膜形成後に、Al層5が形成され更に絶縁層とAl層とを交互に形成される。このときに全体が加熱され、Ti膜24中のTiはAl及びSiと反応して、Ti_xAl_y7，Ti_xSi_y8となる。Ti_xN_y22及びTi_xO_y23は安定でありAl，Siとは極めて反応しにくいため、そのまゝの形で、残る。

これにより、第1図に示すように、バリアメタル21は、Ti_xAl_y7，Ti_xSi_y8，Ti_xN_y22，Ti_xO_y23の組成となり、これらが協働してバリアハイトΦ_{B3}を形成し、ダイオード20は第4図中線IIIで示すI_F-V_F特性を有する。

上記のAl層，絶縁層の形成工程で予定より余分に加熱されたときには、従来の場合と同じく第5図に示すように、Ti_xAl_y7の一部及びTi_xSi_y8の一部がAl層5及びエピタキシャル成長層3内に拡散する。しかし、Ti_xN_y22及びTi_xO_y23は反応しにくいため、Al，Siとは反応せず、界面に残留し続ける。

このため、界面層21aのバリアハイトは前記の場合より多少上昇するも殆んど変わらず、I_F-V_F特性も例えば第4図中線IVで示す如くになり、所定のI_{F1}におけるV_Fの変化量ΔV_Fは僅かの値に留まり、ダイオードのI_F-V_F特性は許容誤差範囲に収まる。

従って、上記のダイオード20は、製造工程での種々のばらつきによりI_F-V_F特性が影響されにくいものとなる。

こゝで、バリアメタル21中のTi_xN_y22及びTi_xO_y23の量は、前記の混合ガス中のN_2，O_2の量により定まる。一方、混合ガス中のN_2，O_2の量を正確に定めることは容易である。従って、N_2，O_2の量を違えた混合ガスを使用することにより、バリアメタル21中のTi_xN_y22及びTi_xO_y23の量を制御することが可能となり、バリアメタル21中に所定量のTi_xN_y22及びTi_xO_y23量を形成させることが出来、終極的に所望のバリアハイトを有する界面層21aを形成することが出来る。

第6図はダイオードのI_F-V_F特性をスパッタリング工程で使用した混合ガスの成分と対応させて示す。同図中、線Vは$Ar+150ppM N_2+20ppM O_2$の混合ガスを使用した場合、線VIは$Ar+100ppM N_2+20ppM O_2$の混合ガスを使用した場合、線VIIは$Ar+50ppM N_2+20ppM O_2$の混合ガスを使用した場合、線VIIIは$Ar+150ppM N_2+40ppM O_2$の混合ガスを使用した場合のI_F-V_F特性を示す。同図よりN_2，O_2の混入量を増やす程V_Fが小さくなっていること及び所望の混合ガスを使用することにより希望するI_F-V_F特性を有するダイオードを製造できることが分かる。

なお、第6図は、100AのTi膜及び1μのAl層を形成し、アニール450℃，30分を3回繰り返した場合であって、界面層の面積が$256\mu^2$のときの特性である。

なお、バリアメタル21中に、Ti_xN_y22及びTi_xO_y23のうちいずれか一方のみが混入した構成であってもよく、上記と同様な効果を有する。

〔発明の効果〕

本発明によれば、界面層が所定量の窒化チタン及び／又は酸化チタンを含有した組成であるため、製造過程の違いによるバリアハイトへの影響が少なく、然して製造装置が相違しても、速い動作速度を有する所望の順方向電流－電圧特性を有するものを再現性良く得ることが出来、歩留りの向上を図ることが出来る。

4.図面の簡単な説明

第1図は本発明になるショットキーバリアダイオードの一実施例の要部の拡大断面図、

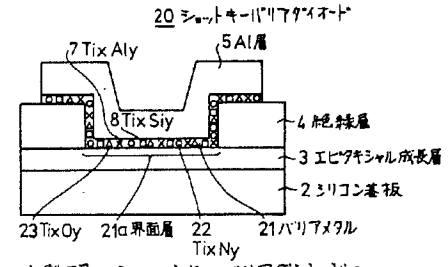
第2図はTi膜形成後の状態を示す図、

第3図はTi膜形成用のスパッタリング装置の

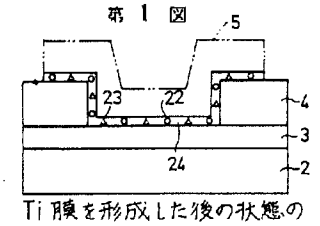
GF Exhibit 1124 - 1776/2704

概略図、
第４図は第１図のダイオードのI_F-V_F特性のばらつきを説明する図、
第５図は熱がかゝり過ぎた場合の界面層の状態を説明する図、
第６図は混合ガスの成分の違いに対応するダイオードのI_F-V_F特性の違いを説明する図、
第７図は従来のショットキーバリアダイオードの１例の要部の拡大断面図、
第８図は第７図のダイオードのI_F-V_F特性のばらつきを説明する図、
第９図はＴｉ膜形成後の状態を示す図、
第１０図は熱がかゝり過ぎた場合の界面層の状態を説明する図である。
図において、
２はシリコン基板、
３はエピタキシャル成長層、
４は絶縁層
５はＡｌ層、
７はTi_xAl_y、
８はTi_xSi_y、
２０はショットキーバリアダイオード、
２１はバリアメタル、
２１ａは界面層、
２２はTi_xN_y、
２３はTi_xO_y、
２４はＴｉ膜、
２５は混合ガスボンベである。

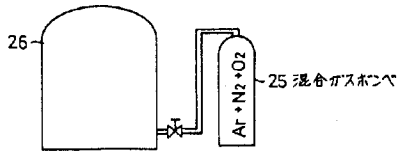
代理人　弁理士　井　桁　貞



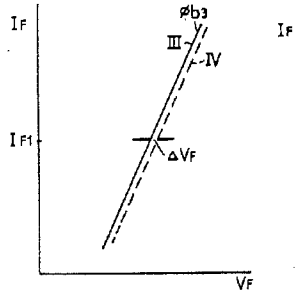
本発明のショットキーバリアダイオードの要部の断面図
第 1 図



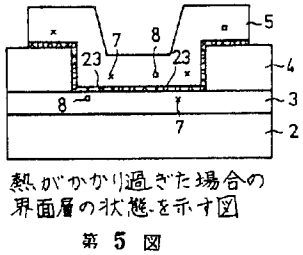
Ti膜を形成した後の状態の断面図
第 2 図



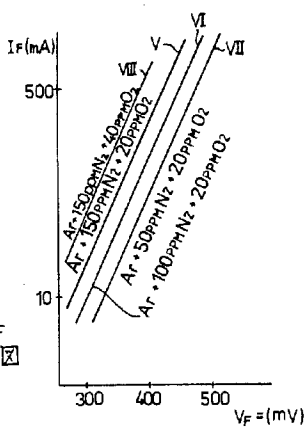
Ti膜形成用スパッタリング装置の概略図
第 3 図



第1図のダイオードのI_F-V_F特性のばらつきを説明する図
第 4 図

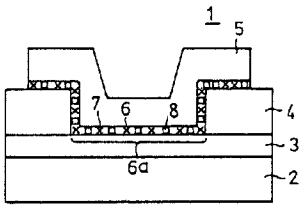


熱がかかり過ぎた場合の界面層の状態を示す図
第 5 図



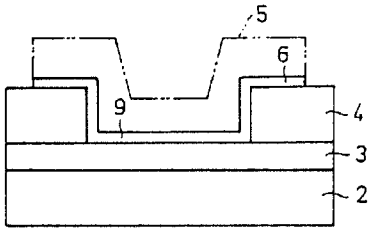
混合ガスの違いに対応するダイオードのI_F-V_F特性を示す図
第 6 図

GF Exhibit 1124 - 1777/2704



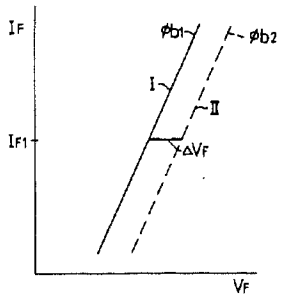
従来のショットキーバリア
ダイオードの要部の断面図

第 7 図



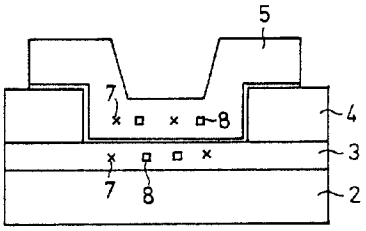
Ti膜形成後の状態を示す図

第 9 図



第7図のダイオードのIF-VF
特性のばらつきを説明する図

第 8 図



熱がかかり過ぎた場合の
界面層の状態を示す図

第 10 図

GF Exhibit 1124 - 1778/2704

Europäisches Patentamt
European Patent Office
Office européen des brevets

Espacenet

JPS63157466A SCHOTTKY BARRIER DIODE

Applicants: FUJITSU LTD

Inventors: FUJITA ICHIRO,TSUNODA KAZUO,UESHIMA SAISHI

Classifications:
IPC ***H01L29/45; H01L29/47; H01L29/872;*** (IPC1-7): H01L29/48; H01L29/91;

CPC **H01L29/456 (EP);**

Priorities: JP30446286A 1986-12-20

Application: JPS63157466A·1986-12-20

Publication: JPS63157466A·1988-06-30

Published as: JPS63157466A

SCHOTTKY BARRIER DIODE

Abstract

PURPOSE:To assure specified forward current-voltage characteristics with high reproducibility not to be affected by various factors of manufacturing processes by a method wherein TiN and/or TiO is partly laid on the interface between Al and Si. CONSTITUTION:An interface layer 21a by a barrier metal 21 is formed between an epitaxial layer 3 and an Al layer 5. The barrier metal 21 contains a TixAly 7, a Tix Siy 8, a TixNy 22 and a TixOy 23 while the total content TixNy 22 and TixOy 23 shall not exceed 20% out of the whole content. In order to form the barrier metal 21, firstly Ti films are formed by sputtering process using Al gas containing specified amount of N2 and O2 gas to form Ti films containing TixNy 22 and TixOy 23 and then TixNy 7 and TixSiy 8 are produced by repeatedly heating the Al layer 5. Through these procedures, the TixNy 22 and TixOy 23 are stabilized to be so hardly reactive to Al, Si that the barrier height is hardly changeable to assure IF-VF characteristics of diode with high reproducibility.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION JPS63157466

[0001]
(Outline) In the Schottky barrier diode of the present invention, titanium nitride and / or titanium oxide is partially interposed at the interface between aluminum and silicon, and a desired forward current is obtained without being affected by various factors in the manufacturing process. -The voltage characteristics can be obtained with good reproducibility. [Field of Industrial Application] The present invention relates to a Schottky barrier diode, and more particularly to an interface between a gold layer and an epitaxial layer. [Prior Art] In a Schottky barrier diode, the forward current (IF) -voltage (VF) characteristic is important, and it is required that the variation be small. When this diode is used by incorporating it in a TTL circuit, it is necessary to have a high operation speed. Since the operating speed is longer as vF is lower, in the above diode, Ti having a small barrier hide Φb is used as the barrier metal. FIG. 7 schematically shows a part of a conventional Schottky barrier diode 1 of this type. In the figure, 2 is a silicon substrate, 3 is an epitaxial growth layer, 4 is an insulating layer, 5 is an A2 layer as a conductive metal, and 6 is a barrier metal. A portion of the barrier metal 6 indicated by reference numeral 6a forms an interface layer between the epitaxial growth WJ3 and Ae115. The interface H6a (barrier metal 6) is composed of Ti A2 7 indicated by X and T indicated by the mouth; x s i y 8 and y. The vialiahide of this interface m6a is Φ, 1 and the diode 1 has the IF-V characteristic shown by degeneracy in FIG. [Problems to be Solved by the Invention] In the diode 1, as shown in FIG. 9, a window is formed in the insulating layer 4 and a Ti film 9 having a thickness of about 100 is formed by sputtering. It is manufactured by forming an A2 layer 5 on the upper surface and then forming insulating layers and A2 layers alternately, though not shown. Insulation layer and AJ! The whole is heated in the process of forming l. For example, when the insulating layer is formed of PSG, heat of 420 to 450 ° C. is 30 minutes to 1 hour). このＴｉ！！ The Ti in the T1 film 7 reacts with A2 and 3i due to the heat in the manufacturing process after the formation of J9, and the Ti XAly7. Ｔｉｘ Ｓ＋ｙ ８となる。 A variation in the heat m received by the T1 film 7

GF Exhibit 1124 - 1780/2704

between the manufacturing facilities is inevitable. The quality of the Ti film itself also varies to some extent between sputtering devices. When the heat is too much, a part of TiXA2,7 and a part of Tr xs t ys diffuse into the AIL layer 5 and the epitaxial growth layer 3 as shown in FIG. 10, and the interface 116a becomes thin.

As a result, the barrier hide is increased to Φb2, vF is increased, and rF-V, the characteristic is shown by, for example, a line {circle around (2)}, and vF is relatively larger than a desired value ΔVF at a predetermined IFl. Will end up. If ΔvF is large, the operating speed of the diode becomes slow, making it unsuitable for incorporation in a TTL circuit, resulting in a defective product. As described above, the conventional diode has a problem that its IF- ■ F characteristic is easily affected in the manufacturing process. [Means for Solving the Problems] In the present invention, the interface layer between the epitaxial layer and the metal layer on the semiconductor substrate has a composition containing titanium nitride and / or titanium oxide in a desired solid content. [Operation] The above composition limits the difference in IF-V and characteristics due to the difference in manufacturing equipment even if the manufacturing process varies. (Embodiment) FIG. 1 shows a Schottky barrier diode 20 according to the present invention. In the figure, those parts corresponding to the parts shown in FIG. 7 are designated by the same reference numerals, and a description thereof will be omitted. Reference numeral 21 is a barrier metal, which is interposed between the epitaxial growth layer 3 and the / 1 layer 5. Of these, the portion indicated by reference numeral 21a is the epitaxial growth layer 3 and / M! The interface layer between 1ii5 is formed. The interface 1121a (barrier metal 21) is Ti xAIly7. The composition includes TixNy (titanium nitride) 22 indicated by O and TixOy (titanium oxide) 23 indicated by Δ in addition to T i x S i y 8 indicated by mouth. The ratio of the total y content of Ti N 22 and T + xo, 23 to the total content is 20% or less, which is controlled as described below. FIG. 2 shows a state after the Ti film 24 is formed by sputtering. As shown in FIG. 3, the sputtering is performed using a gas cylinder 25 of a mixed gas in which A "is mixed with a predetermined minute amount of N2 and o2. For example, a cylinder of a mixed gas in which N2 is 2001) l) H and 02 is mixed with 20pp) l in Ar is used. In FIG. 3, 26 is a vacuum chamber. By performing sputtering using this mixed gas, N2.02 reacts with Ti to produce Ti N TiX0y, and a Ti film with a composition y containing X y'Ti N 22 and T i X0y23 in Ji. 24 is formed. (2) After forming the i film, the A2 layer 5 is formed, and the insulating layer and the A2 layer are alternately formed. At this time, the whole is heated, Ti in the T1 film 24 reacts with A2 and Si, and Ti Ae 7.

Ｔ ｌ Ｘ５ ｉ ｙ ｙ ８となる。 Since Ti N 22 and TixOy 23 are y stable and extremely difficult to react with Ae and st, they remain in that form. As a result, as shown in FIG. 1, the barrier metal 21 has T i A'l 7 and T i x S i y 8. The composition is yT i N 22 and T t x Oy 23, and these y cooperate to form the barrier hide Φb3, and the diode 20 has I, −V and characteristics shown by the solid line in FIG. Above An! f. When excessively heated in the insulating layer forming

GF Exhibit 1124 - 1781/2704

process, the T1xA-deficient y7 part and the TiX5iy8 part are in the A2 layer 5 and the epitaxial growth layer 3 as shown in FIG. Spread to. しかし、Ｔｉ Ｘ Ｎ。 Since 22 and Tr x o y 23 do not easily react, they do not react with Ae and Si and remain at the interface. Therefore, the barrier bite of the interface layer 21a is slightly higher than that in the above case, but is almost the same. -V, the characteristic also becomes as shown by the line IV in FIG. 4, for example, the change in V at a given IFI, ΔV [, remains at a slight value, and the diode 1. The -VF characteristic falls within the allowable error range. Therefore, the above-mentioned diode 20 is less susceptible to I-V and characteristics due to various variations in manufacturing: Here, the defects of T1xNy22 and TixOy23 in the barrier metal 21 are determined by the threshold of N2,02 in the mixed gas. On the other hand, it is easy to accurately determine the values of N and 02 in the mixed gas. Therefore, it is possible to control the mouths of Ti N 22 and T ixo, 23 in the barrier metal 21 by using a mixed gas having different N2, 02, and the predetermined amount in the barrier metal 21. ff1 (7) Ti N 22 and T + xo, 23 ffi can be formed and y, and finally the interface FIJ21a having a desired barrier hide can be formed. FIG. 6 shows the IF-V characteristics of the diode in correspondence with the components of the mixed gas used in the subbattering process. In the figure, line V shows the case where the mixed gas of Ar + 150p1) HN 2 +201) l) 802 is used, and line ■ shows the case where the mixed gas of Ar +1001) pHN 2 +20 DI) H02 is used. ■ indicates the IF-VF characteristics when using a mixed gas of Al + 50p11M N2 + 20p1) HO2, and line ■ indicates using a mixed gas of Δr + 150p1) HN2 + 40 DDHO2.

From the figure, it can be seen that as the mixing amount of N2 02 increases, F decreases and that a diode having a desired I-VF characteristic can be manufactured by using a desired mixed gas. Incidentally, FIG. 6 shows the characteristics when a Ti film of 100 persons and an A2 layer of 1 μm were formed and annealing at 450 ° C. for 230 minutes was repeated three times, and the area of the interface layer was 256 μ2. The barrier metal 21 may have a configuration in which only one of Ti XNy22 and T1xoy23 is mixed, and the same as above! Have a significant effect. [Effect of the Invention] According to the present invention, since the interface layer has a composition containing titanium nitride and / or titanium oxide a predetermined number of times, the influence on the barrier hide due to the difference in the manufacturing process is small, and the manufacturing apparatus is different. Even in this case, it is possible to obtain with high reproducibility a desired forward current-voltage characteristic having a high operation speed, and it is possible to improve the yield.

[0002]
Brief description of the drawings

[0003]

GF Exhibit 1124 - 1782/2704

FIG. 1 is an enlarged sectional view of an essential part of an embodiment of a Schottky barrier diode according to the present invention, FIG. 2 is a view showing a state after forming a 7i film, and FIG. 3 is a sputtering device for forming a Ti film. Fig. 4 is a schematic diagram, Fig. 4 is a diagram for explaining the variation in the IF-vF characteristics of the diode of Fig. 1, Fig. 5 is a diagram for explaining the state of the interface when too much heat is applied, and Fig. 6 is 1. The diode corresponding to the difference in the components of the mixed gas.

FIG. 7 is a diagram for explaining a difference in −VF characteristic, FIG. 7 is an enlarged cross-sectional view of a main part of an example of a conventional Schottky barrier diode, and FIG. 8 is a description of IF-V of the diode in FIG. 7 and characteristic variation. FIG. 9 is a diagram showing the state after the Ti film is formed, and FIG. 10 is a diagram explaining the state of the interface layer when the heat is excessive. In the figure, 2 is a silicon substrate, 3 is an epitaxial growth layer, 4 is an insulating layer 5 is an A2 layer, 7 is TixA, 8 is TjxSjys20 is a Schottky barrier diode, 21 is a barrier metal, and 21a is An interface layer, 22 is TjxNy123, TixOyl24 is a Ti film, and 25 is a mixed gas cylinder. Cross section of the zero portion of the 9th,-, Toki-It "IT lead wire. Fig. 1 Fig. 75 Fig. 3 Fig. 3 Fig. 3 Fig. 5 Fig. 5 Fig. 5 IF-VF 7 Confectionery 8 Fig. 1 T-pod type hair support 1 No, 1 small figure 9 Fig. 9 Fever and s"j 4 +-, interface counterfeiting, 1 Dimensions Figure 1O

GF Exhibit 1124 - 1783/2704

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

CLAIMS JPS63157466

1.
The interface layer (21a) between the epitaxial layer (3) and the metal layer (5) on the substrate (2) has a composition containing a predetermined amount of titanium nitride (22) and / or titanium oxide (23). Is a Schottky barrier diode. (2) The interface layer (21a) is formed by sputtering titanium using a mixed gas obtained by mixing a desired amount of nitrogen and / or oxygen with argon gas. A Schottky barrier diode according to item 1 above.

GF Exhibit 1124 - 1784/2704

⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　昭63－175471

⑤1Int.Cl.⁴　識別記号　庁内整理番号　⑬公開　昭和63年(1988)7月19日
H 01 L 29/46　B－7638－5F

審査請求　未請求　発明の数 1　（全5頁）

⑤4発明の名称　半導体装置

⑳特　願　昭62－6078
㉒出　願　昭62(1987)1月16日

⑦2発明者　牧本　俊樹　東京都武蔵野市緑町3丁目9番11号　日本電信電話株式会社基礎研究所内
⑦2発明者　堀越　佳治　東京都武蔵野市緑町3丁目9番11号　日本電信電話株式会社基礎研究所内
⑦2発明者　小林　直樹　東京都武蔵野市緑町3丁目9番11号　日本電信電話株式会社基礎研究所内
⑦1出願人　日本電信電話株式会社　東京都千代田区内幸町1丁目1番6号
⑦4代理人　弁理士　谷　義一

明　細　書

1．発明の名称

半導体装置

2．特許請求の範囲

1)　半導体層の表面近傍に該表面と平行に第1の不純物ドープ単原子層が形成されており、該第1の不純物ドープ単原子層により内部に該第1の層と平行に第2の不純物ドープ単原子層が形成されていることを特徴とする半導体装置。

2)　前記第1の不純物ドープ単原子層の前記表面からの距離が100Å以内であり、かつ前記第2の不純物ドープ単原子層の前記表面からの距離が500 Å以内であることを特徴とする特許請求の範囲第1項記載の半導体装置。

3)　前記第1の不純物層のドーピング量は、金属と前記半導体を接触させた際に形成されるショットキバリアの高さに相当する電圧よりも小さな電圧降下を引き起こす量であることを特徴とする特許請求の範囲第1項または第2項に記載の半導体装置。

4)　前記第1および第2の不純物層によって引き起こされる電圧降下の量が前記ショットキバリアの高さに相当する電圧より大きいことを特徴とする特許請求の範囲第1項記載の半導体装置。

（以　下　余　白）

GF Exhibit 1124 - 1785/2704

3.発明の詳細な説明

[産業上の利用分野]

本発明は半導体装置に関し、特に合金化プロセスを経ずに、半導体上へオーミック電極の形成を可能とする不純物ドーピング層を有する半導体装置に関するものである。

[従来の技術]

原子層ドーピングを用いて、トンネル電流を流すことにより、低抵抗のオーミックコンタクトを形成する方法として、金属と半導体の界面近傍の半導体中に一層の原子層ドーピングを行う方法がある。この方法におけるエネルギバンド図を第3図に示す。この方法においては以下に示すような2つの欠点がある。

① まず、原子層ドープ層とショットキバリアにより形成される三角ポテンシャル（第3図参照）を通過するトンネル電流を増やさねばならない。このためには原子層ドープ層中の不純物が高濃度であり、かつ活性化していなければならない。しかし、高濃度に原子層ドーピングを行うと、不純物準位が深くなり、不純物が十分活性化されず。ショットキバリアの高さに相当する電圧よりも大きな電圧降下は得ることができず、ノンアロイオーミックコンタクトの実現は困難であった。

② 次に、一層の原子層ドーピングによって、ショットキバリアの高さに相当する電圧よりも大きな電圧降下を引き起こすためには、ドーピング層をある程度、金属と半導体の界面から離さねばならない。(Appl. Phys. Lett. ; 49 (5),1986, 292)。しかし、この時には三角ポテンシャルは厚くなり電子のトンネル確率は低いものとなるため、ノンアロイオーミックコンタクトの実現は困難なものとなる。

金属と半導体との界面から距離dの位置に、シートキャリア濃度がNcの原子層ドーピングを行った場合の電圧降下ΔVは

$$\Delta V = q \times d \times N_c / \epsilon \qquad (1)$$

（qは電子電荷、εは誘電率）

で与えられる。

ここでは、GaAs中にSiを原子層ドープした例について述べる。

原子層ドープ層にSi不純物を面密度で5×10^{13}個/cm²だけ入れた場合には、そのうちの20%だけがドナとなり活性化することが報告されている（Jpn. J. Appl. Phys. ; 25, (1986),L748)。これはSi不純物の準位が深くなっているため、不純物が十分に活性化されていないためである。

第4図に従来の方法で作成した一層のドープ層を有する半導体装置の例を示す。この従来例はn-type GaAs 基板1上にノンドープGaAs層2を200[Å] 形成した後、Si不純物を面密度で5×10^{13}個／cm² 入れた単原子層ドーピング層3を形成した後、再びノンドープGaAs層2をd [Å] 形成し、裏面にAuGeNiオーミックコンタクト4を蒸着し、表面には、Au電極5を蒸着した構造となっている。

接触抵抗ρ_cは第4図に示すように、膜厚方向に電圧をかけ、電流を測定することによって測定するができる。dによる接触抵抗ρ_cの変化を第5図に示す。dの小さいときには、一層の原子層ドープ層による電圧降下がショットキバリアに相当する電圧よりも小さなためρ_cは高い。また、dを大きくすると、三角ポテンシャルが厚いためρ_cは高い。接触抵抗ρ_cが最小となるのは式(1) においてΔVがショットキバリアの高さに相当するd＝60 [Å] である。しかし、この場合にも、三角ポテンシャルが厚いために十分なトンネル電流が流れないため、ρ_cは高い。

[発明が解決しようとする問題点]

本発明は、上述した従来の欠点、すなわちドーピング層の活性化率が低下し、トンネル電流が少なかった点を解決し、良好なノンアロイオーミック電極層を有する半導体装置を提供することを目的とする。

[問題点を解決するための手段]

このような目的を達成するために、本発明の半導体装置は、半導体層の表面近傍に表面と平行に

GF Exhibit 1124 - 1786/2704

第１の不純物ドープ単原子層が形成されており、第１の不純物ドープ単原子層により内部に第１の層と平行に第２の不純物ドープ単原子層が形成されていることを特徴とする。

［作　用］

本発明においては単原子層ドープ層によって形成されるポテンシャルを薄くすることによって、十分なトンネル電流を流すために、単原子層ドープ層を金属と半導体界面に十分に近くして不純物原子の活性化率を極めて高くし、さらに次の単原子層ドーピング層と供にショットキバリアの高さに相当する電圧よりも大きな電圧降下を引き起こさせる。金属と半導体との界面に近い高濃度のドーピング層の不純物準位は深いのにもかかわらず、フェルミレベルよりも上にあるために、すべて活性化されることになる。

このために十分なトンネル電流を流すことができるので、ノンアロイオーミックコンタクトの実現が可能である。

［実施例］

以下に図面を参照して本発明の実施例を説明する。

第１図に本発明の実施例を示す。

第１の不純物ドープ層としてｄ＝10［Å］の位置に５×10^{13}個／cm^2 だけSiを単原子層ドープした第１の層3Aを形成し、さらにｄ＝ 60[Å] の位置に、第２の不純物ドープ層3Bとして活性化率が100 %である５×10^{12}個／cm^2 のSi単原子層ドーピングを行った構造を作製した。他の構造は第４図に示した従来例と同じである。

第１および第２の不純物ドープ層はそれぞれ複数の原子層からなると、原子層間での不純物の相互作用によって電子の放出が抑制される。従って両不純物ドープ層はそれぞれ単原子層であることが必要である。高濃度の不純物をドープした単原子層を形成するには、MOCVD 法を改良した流量変調MOCVD 法が有効である。

このとき、第１の不純物ドープ層の活性化率を従来例と同様に20%とすると、第１層による電圧降下は$\Delta V_1 = 0.14$[V] となり、第２の不純物ドープ層による電圧降下は、$\Delta V_2 = 0.42$[V] であるから、$\Delta V_1 + \Delta V_2 < \phi_B$ (0.9V)となり、低い接触抵抗ρ_cは得られない。しかし、実際に測定を行なうと$\rho_c = 1 \times 10^{-6}$[Ω・$cm^2$]程度の極めて低い接触抵抗が得られた。

第２図に本発明における２層の単原子層ドープを行った構造のエネルギーバンドを示す。

本発明においてはフェルミレベルよりも上の不純物準位から電子が放出されることにより、第１層の活性化率が実質上高くなったために低い接触抵抗が得られる。このように第１層の位置における伝導帯とフェルミレベルとの差を比較的大きくとることにより、不純物の活性化率を上げることができる。第２図と第３図とを比較すれば明らかなように金属と半導体との界面付近の電子に対するポテンシャルは、従来の三角ポテンシャルに比べ薄くなり、十分なトンネル電流を流すことができるために、ノンアロイオーミックコンタクトの実現が可能である。

さらに、第１層および第２層のドーピング量をそれぞれ５×10^{13}個／cm^2 ，５×10^{12}個／cm^2 とし、第１層および第２層の半導体表面からの位置を変え、抵抗率の変化を調べた。その結果を第１表に示す。第１層の位置が界面から 100Åをこえて離れている場合および第２層の位置が 500Åをこえて離れている場合には10^{-6}Ω・cm^2 台の低い抵抗率を得ることはできなかった。従って10^{-6}Ω・cm^2 台の低い抵抗率を得るためには、第１層および第２層の位置は、半導体の表面から、それぞれ100 Å，500 Å以内が望ましい。

表　1

第１層の位置［Å］	第２層の位置［Å］	抵抗率［Ω・cm^2］
１０	１００	２×10^{-6}
１０	２００	４×10^{-6}
１０	５００	６×10^{-6}
５０	１５０	３×10^{-6}
１００	１５０	５×10^{-6}

GF Exhibit 1124 - 1787/2704

［効　果］

以上説明したように、本発明によれば金属と半導体との界面付近に存在する単原子層ドーピング層内の不純物原子のエネルギ準位が、フェルミレベルよりも上であり、高濃度にドーピングを行なっても不純物原子は十分活性化できる。このため、界面付近に存在するポテンシャルは、非常に薄くなり、十分なトンネル電流を流すことができるため、ノンアロイオーミックコンタクトの実現が可能となった。

4．図面の簡単な説明

第1図は本発明の実施例を示す断面図、

第2図は本発明におけるエネルギーバンド図、

第3図は従来の単一のドープ層を有する半導体装置におけるエネルギーバンド図、

第4図は従来の半導体装置の一例の断面図、

第5図は従来の装置における接触抵抗を示す図である。

1…n－GaAs基板、

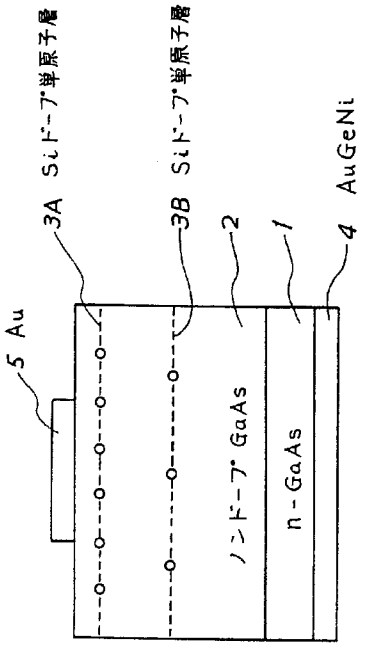
2…ノンドープGaAs層、

3A…第1の不純物ドープ単原子層、

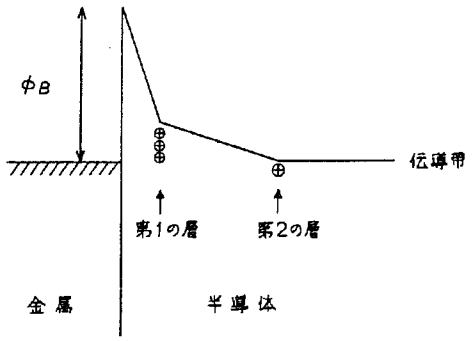
3B…第2の不純物ドープ単原子層。

特許出願人　　日本電信電話株式会社

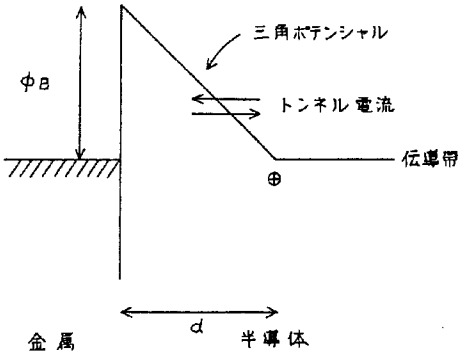
代　理　人　　弁理士　谷　　義　一



第1図

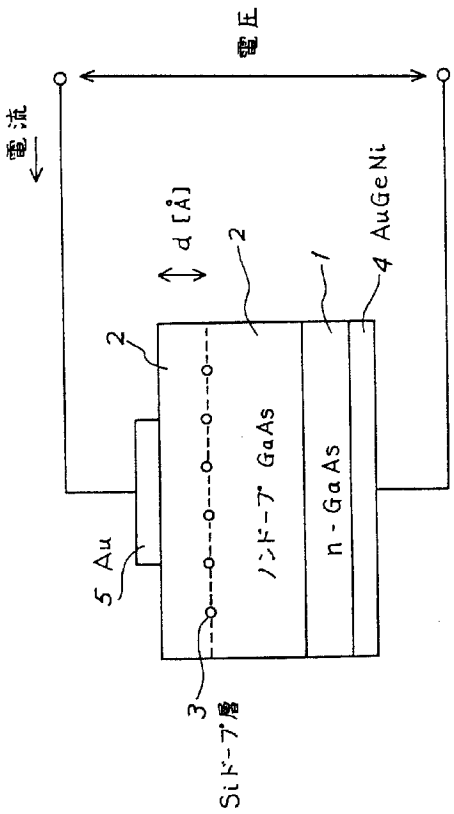


第2図

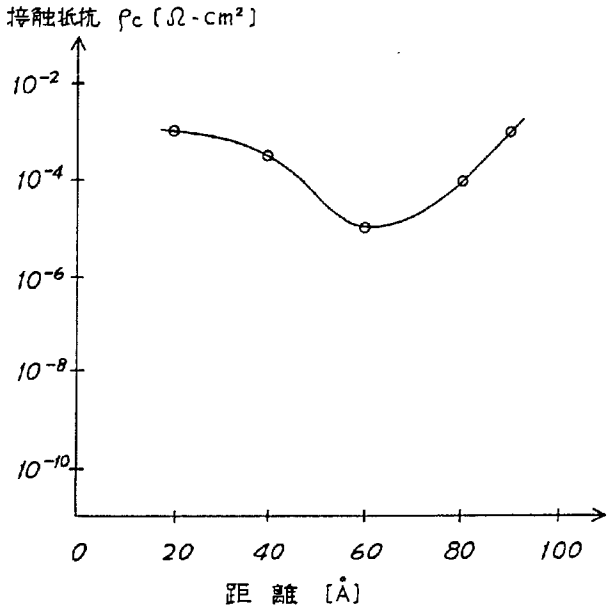


第3図

GF Exhibit 1124 - 1788/2704



第 4 図



第 5 図

GF Exhibit 1124 - 1789/2704

Europäisches Patentamt
European Patent Office
Office européen des brevets

Espacenet

JPS63175471A SEMICONDUCTOR DEVICE

Applicants: NIPPON TELEGRAPH & TELEPHONE

Inventors: HORIKOSHI YOSHIHARU,KOBAYASHI NAOKI,MAKIMOTO TOSHIKI

Classifications:
IPC ***H01L21/28; H01L21/338; H01L29/43; H01L29/812;*** (IPC1-7): H01L29/46;

Priorities: JP607887A 1987-01-16

Application: JPS63175471A·1987-01-16

Publication: JPS63175471A·1988-07-19

Published as: JPS63175471A;**JPH0728025B2**

SEMICONDUCTOR DEVICE

Abstract

PURPOSE:To make non-alloy ohmic contact by supplying sufficient tunnel current by a method wherein a single atomic doped layer is formed close to an interface between a metal and a semiconductor to augment the rate of activation of impurity atom. CONSTITUTION:The first impurity doped single atomic layer 3A is formed on the part near the surface of a semiconductor layer 2 while the second impurity doped single atomic layer 3B is formed in parallel with and inside the first impurity doped layer 3A. Resultantly, the energy level of impurity atom in a single atomic doped layer existing in the part near an interface between a metal and a semiconductor exceeds the Fermi level so that the impurity atom may be sufficiently activated even in high concentration doping process to lower the potential existing close to the interface for supplying a sufficient tunnel current. Through these procedures, non-alloy ohmic contact can be made.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION JPS63175471

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor device, and more particularly to a semiconductor device having an impurity doping layer which enables formation of an ohmic electrode on a semiconductor without undergoing an alloying process. [Prior Art] As a method of forming a low-resistance ohmic contact by passing a tunnel current using atomic layer doping, there is a method of performing one atomic layer doping in a semiconductor in the vicinity of an interface between a metal and a semiconductor. . The energy band diagram in this method is shown in FIG. This method has the following two drawbacks. ■ First, the tunnel current that passes through the triangular potential (see Fig. 3) formed by the atomic layer dope layer and the Schottky barrier must be increased. For this purpose, the impurities in the atomic layer dope layer must be highly concentrated and activated. However, when the atomic layer doping is performed at a high concentration, the impurity level becomes deep and the impurities are not sufficiently activated. A voltage drop larger than the voltage corresponding to the height of the Schottky barrier could not be obtained, and it was difficult to realize a non-alloy ohmic contact. ■ Next, in order for one atomic layer doping to cause a voltage drop greater than the voltage corresponding to the height of the Schottky barrier, the doping layer must be separated from the metal-semiconductor interface to some extent. (Appl, Phys, Lett ,; 49 (5), 1986.292), L, streak. At this time, the triangular potential becomes thick and the electron tunneling probability becomes low, so it is difficult to realize a non-alloy ohmink contact. Will be things. The voltage drop ΔV is $\Delta V = qxdxNc / 6$ (1) (q is the electronic charge, ε is the read The electric rate) is given. Here, an example will be described in which GaAs is atomically layered with St. It has been reported that when 5 X 10 "pieces / cm" of Si impurity is added to the atomic layer dope layer in an area density, only 20% of it becomes a donor and is activated (Jpn, J, Appl, Phys ,; 25 ° (1986), L748), because the level of the Si impurity is deep and the impurity is not sufficiently activated. FIG. 4 shows an example of a

GF Exhibit 1124 - 1791/2704

semiconductor device having a single doped layer formed by a conventional method. In this conventional example, after forming the undoped GaAs layer 2 for 200 [persons] on the n-type GaAs substrate 1, after forming the monoatomic layer doping layer 3 containing 5 × 10″ Si / impurity / cm 2 in area density , The non-doped GaAs layer 2 is formed again [person], the AuGeNi ohmic contact 4 is vapor-deposited on the back surface, and the Au electrode 5 is vapor-deposited on the front surface.

Contact resistance ρ . Can be measured by applying a voltage in the film thickness direction and measuring the current as shown in FIG. The change in contact resistance ρ C due to d is shown in FIG. When d is small, pc is high because the voltage drop due to one atomic layer doped layer is smaller than the voltage corresponding to the Schottky barrier. Further, when d is increased, the triangular potential is thicker, so that pc is higher. The minimum contact resistance pc is d = 60 [ON], which corresponds to the height of the Schottky barrier in the formula (1). However, in this case as well, since the triangular potential is thick and a sufficient tunnel current does not flow, ρ 0 is high. [Problems to be Solved by the Invention] The present invention solves the above-mentioned conventional drawbacks, that is, the activation rate of the doping layer is lowered and the tunnel current is small, and has a good non-alloy ohmic electrode layer. An object is to provide a semiconductor device. [Means for Solving the Problems] In order to achieve such an object, in the semiconductor device of the present invention, a first impurity-doped monoatomic layer is formed in the vicinity of the surface of the semiconductor layer in parallel with the surface. A second impurity-doped monoatomic layer is formed inside the first impurity-doped monoatomic layer in parallel with the first layer. [Operation] In the present invention, by thinning the potential formed by the monoatomic layer-doped layer, the monoatomic layer-doped layer is sufficiently close to the metal-semiconductor interface in order to pass a sufficient tunnel current. The activation rate of atoms is made extremely high, and further, together with the subsequent monoatomic layer doping layer, a voltage drop larger than the voltage corresponding to the height of the Schottky barrier is caused. Although the impurity level of the high-concentration doping layer close to the interface between the metal and the semiconductor is deep, it is above the Fermi level, so that the impurity levels are all activated. For this reason, a sufficient tunnel current can be passed, so that non-alloy ohmic contact can be realized. [Embodiment] The present invention will be described below in detail with reference to the drawings. 1C shows an embodiment of the present invention. As the first impurity-doped layer, the first layer 3A was formed at the position of d = 10 [persons] by 5 × 10″ pieces / crn2 of mono atomic layer doped with St, and roughly at the position of d = 60 CAl. As the impurity-doped layer 3B of No. 2, a structure having 5 × 10″ pieces / cI 112 of Si monoatomic layer doping having an activation rate of 100% was prepared. The other structure is the same as the conventional example shown in FIG.

When each of the first and second impurity-doped layers is composed of a plurality of atomic

GF Exhibit 1124 - 1792/2704

layers, the interaction of impurities between the atomic layers suppresses electron emission. Therefore, it is necessary that both the impurity-doped layers are monoatomic layers. The flow rate modulation MOGVD method, which is an improved MOCVD method, is effective for forming a monoatomic layer doped with a high concentration of impurities. At this time, assuming that the activation rate of the first impurity-doped layer is 20% as in the conventional example, the voltage drop due to the first layer is $\Delta V, = O, 14$ [V], and the voltage due to the second impurity-doped layer is Since the drop is $\Delta V2 = 0{,}42$ [V], $\Delta v, -1 - AV2 < \phi B$ (0,9V), and a low contact resistance ρ. Can't get However, when actually measured, $\rho . = A$ very low contact resistance of about IX 10-'[$\Omega \cdot$ cm2] was obtained. FIG. 2 shows an energy band of a structure in which two layers of monoatomic layers are doped in the present invention. In the present invention, electrons are emitted from the impurity levels above the Fermi level, so that the activation rate of the first layer is substantially higher (a low contact resistance is obtained). Thus, by making the difference between the conduction band and the Fermi level at the position of the first layer relatively large, the activation rate of impurities can be increased. As is apparent from a comparison between FIG. 2 and FIG. 3, the potential for electrons near the interface between the metal and the semiconductor is thinner than the conventional triangular potential, and a sufficient tunnel current can flow. It is possible to realize non-alloy ohmic contact. Rokukyu Mu Flute 1 Maki) γ has a 7th layer doping layer of 5 x 1G "pieces / cod", 5 x 10'2 pieces / cm 2, and semiconductors of the first and second layers The position from the surface was changed and the change in resistivity was examined. The results are shown in Table 1. When the position of the first layer is more than 100 people away from the interface and the position of the second layer is more than 500 people, it is possible to obtain a low resistivity of $10^{-6}\ \Omega \cdot$ cm 2. There wasn't. Therefore, in order to obtain a resistivity as low as $10^{-8}\ \Omega \cdot$ cm 2, it is desirable that the positions of the first layer and the second layer are within 100 and 500 persons from the surface of the semiconductor, respectively. Table 1 [Effect] As described above, according to the present invention, the energy level of the impurity atom in the monoatomic layer doping layer existing near the interface between the metal and the semiconductor is higher than the Fermi level, Impurity atoms can be sufficiently activated even if doping is performed at a high concentration.

For this reason, the potential existing near the interface becomes extremely thin, and a sufficient tunnel current can flow, so that non-alloy ohmic contact can be realized.

[0002]
Brief description of the drawings

[0003]

GF Exhibit 1124 - 1793/2704

FIG. 1 is a sectional view showing an embodiment of the present invention, FIG. 2 is an energy band diagram in the present invention, FIG. 3 is an energy band diagram in a conventional semiconductor device having a single doped layer, and FIG. FIG. 5 is a sectional view of an example of the semiconductor device of FIG. 5, and FIG. 5 is a view showing the contact resistance in the conventional device.

1 --- n-GaAs substrate, 2 ... non-doped GaAs layer, 3A ... first impurity-doped monoatomic layer, 3B ... second impurity-doped monoatomic layer.

GF Exhibit 1124 - 1794/2704

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

CLAIMS JPS63175471

1.

A first impurity-doped monoatomic layer is formed in the vicinity of the surface in parallel with the surface, and a second impurity-doped monoatomic layer is provided inside the first impurity-doped monoatomic layer in parallel with the first layer by the first impurity-doped monoatomic layer. A semiconductor device in which a layer is formed. 2) The distance from the surface of the first impurity-doped monoatomic layer is within 100 Å, and the distance of the second impurity-doped monoatomic layer from the surface is within 500 Å The semiconductor device according to claim 1. 3) The doping amount of the first impurity layer is an amount that causes a voltage drop smaller than a voltage corresponding to the height of the Schottky barrier formed when the metal and the semiconductor are brought into contact with each other. The semiconductor device according to claim 1 or 2. 4) The semiconductor device according to claim 1, wherein the amount of voltage drop caused by the first and second impurity layers is larger than the voltage corresponding to the height of the Schottky barrier.

GF Exhibit 1124 - 1795/2704

(19) 대한민국특허청(KR)
(12) 특허공보(B1)

(51) Int. Cl.[5]
H01L 29/78

(45) 공고일자 1992년03월21일
(11) 공고번호 92-002350

(21) 출원번호	특1988-0005839	(65) 공개번호	특1988-0014685
(22) 출원일자	1988년05월19일	(43) 공개일자	1988년12월24일

(30) 우선권주장
62-124221 1987년05월21일 일본(JP)
62-155822 1987년06월23일 일본(JP)
62-155824 1987년06월23일 일본(JP)
62-176176 1987년07월15일 일본(JP)
62-176177 1987년07월15일 일본(JP)
62-176178 1987년07월15일 일본(JP)

(71) 출원인
마쯔시다덴기산교 가부시기가이샤 다니이 아끼오
일본국 오오사까후 가도마시 오오아자가도마 1006반지

(72) 발명자
고부시 가즈히로
일본국 오오사까후 오오사까시 미야고지마구 미야고지마미나미 도오리 1죠오메 2반 5고
가메야마 슈우이찌
일본국 효오고껭 이다미시 히가시아리오까 1죠오메 22
오가다 쇼오죠오
일본국 효오고껭 고오베시 히가시나다구 후가에흔마찌 2죠오메 4반 20고 쯔지 가즈히고
일본국 나라껭 이고마시 가미마찌 4800-256

(74) 대리인
신중훈

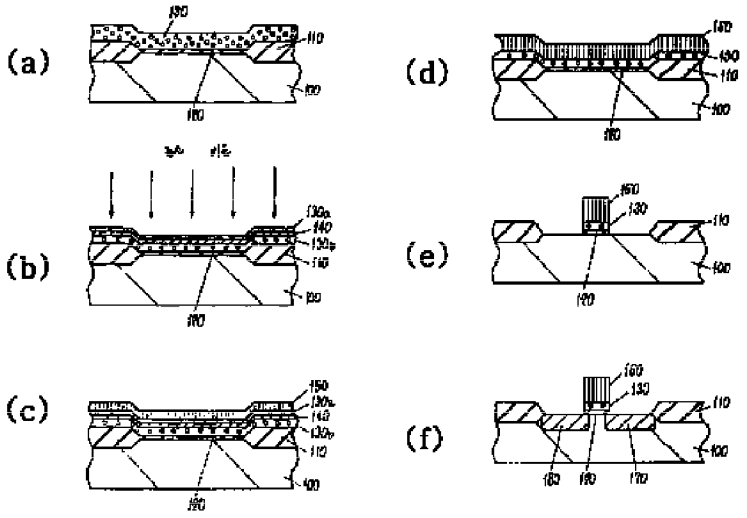
심사관 : 김경국 (책자공보 제2704호)

(54) 반도체장치의 제조방법

요약

내용 없음.

대표도



명세서

[발명의 명칭]

GF Exhibit 1124 - 1796/2704

반도체장치의 제조방법

[도면의 간단한 설명]

제1도는 본 발명의 제1실시예의 공정순서를 도시한 단면도.

제2도는 본 발명의 제2실시예의 공정순서를 도시한 단면도.

제3도는 본 발명의 제3실시예의 공정순서를 도시한 단면도.

제4도는 본 발명의 제4실시예의 공정순서를 도시한 단면도.

* 도면의 주요부분에 대한 부호의 설명

100,200,300,400 : 실리콘기판 110,210,310,410 : 산화막

120,220,320,420 : 게이트 산화막 130,230,330,430 : 다결정 실리콘막

140,440 : 원자도입층 150 : 얇은 티탄막

160,260,360,460 : 합금화층 170,270,370,470 : 소오스영역

180,280,380,480 : 드레인영역 240,340 : 제1원자도입층

250,350,450 : 얇은 텅스텐막 290,390 : 제2원자도입층

[발명의 상세한 설명]

본 발명은 반도체장치의 제조방법에 관한 것으로, 특히 MOS형 집적회로등의 비(非)단결정도전체막과 저(低)저항도전체막으로 구성된 저저항화된 게이트전극의 전기적 특성을 개량하고, 또 게이트절연막의 절약파괴를 방지할 수 있는 제조방법에 관한 것이다.

전계효과형 반도체집적회로에서 미세하고 고성능의 트랜지스터를 얻기 위하여, 비단결정도전체막으로 구성된 게이트전극상에 저저항도전체막을 형성하고 열처리하여 게이전극의 저저항화를 일반적으로 실행한다.

예를 들면, 저저항전도체로서, 고융점 금속 또는 실리콘과의 합금, 즉, 실리사이드는 다결정체실리콘상에 퇴적되어 게이트전극으로 사용되고, 약 500℃로 열처리 하면 고융점금속 또는 실리사이드는 쉽게 다결정체실리콘과 반응하여 전부 실리사이드속으로 변형됨으로써 저저항화가 된다.

이렇게 형성된 도전체막의 시이트저항은 대략 1-10Ω/스퀘어로 낮아, 반도체집적회로의 고속작동이 예기된다.

반면, 금속종류에 의존하여, 다결정체실리콘과는 다른 물질과 반응하고, 특히 티탄은 게이트 전극물질로서 사용되는 실리콘산화막과 반응하므로, 비록 이것이 매우 저저항이지만 게이트전극물질로 사용되기는 어렵다.

따라서, 티탄보다는 약간 고저항이지만 실리콘산화막과는 거의 반응하지 않는, 텅스텐과 몰리브덴이 일반적으로 사용된다.

이런 고융점금속 또는 실리사이드와 실리콘질화막 또는 실리콘산화막과의 반응성 및 반응물의 생성에너지는 N.G.Einsprach 편(Academic Press 출판)의 VLSI 전자공학 : 미세구조, 제9권, 제2장에 기재되어 있다.

한편, 반응의 용이성은 활성화에너지의 크기에 의해 판단될 수 있으며, 활성화에너지가 작을수록 반응이 쉬워지는 것은 알려져 있다.

비단결정도전체막으로 구성된 게이트전극상에 저저항도전체막을 형성한 후 열처리하면, 비단결정도전체막과 저저항도전체막사이의 계면에서 상호의 구성원자가 이동하여, 계면부근이 합금화되어, 저저항화된다.

그러나, 비단결정도전체의 결정입자사이의 계면, 즉, 입자 경계에서, 비단결정도전체의 구성원자의 결합력이 약하므로, 저저항도전체막의 구성원자와의 원자의 치환이 결정입자내에서 보다 빠르게 진행되어, 저저항도전체는 입자경계를 따라서 국부적으로 확산되는 경향이 있다.

저저항도전체가 국부적으로 확산되어 게이트전극 아래의 절연막을 찢게되면, 게이트전극이 다른 전극과 단락되어, 트랜지스터의 신뢰성 또는 제품의 수율을 저하시킨다.

이것을 방지하기 위해, 비단결정도전체와 저저항도전체 사이에 CVD(화학적 증착)에 의해 초박형의 실리콘질화막을 퇴적시켜 저저항도전체의 국부적인 확산을 억제하고 신뢰성을 증가시키는 방법이 IEEE Transactions of Electron Devices, Vol., ED-33, No.4, April 1986, pp. 464~467에 언급되어 있다.

그러나 이것은 막두께의 고재현성에서, CVD에 의한 초박편실리콘 질화막의 퇴적은 어렵고, 더욱이 비교적 낮은 온도에서의 퇴적과 불순물확산층내의 불순물의 재확산에 기인한 전기적 특성에의 변화를 방지하는 것이 필요하므로, 저저항도전체의 국부적 확산을 충분히 억제하는 조밀막성질을 얻기가 곤란하여, 신뢰성과 수율의 향상 또는 충분하지가 않았다.

상기 문제점을 해결하기 위해 본 발명의 일차적 목적은 저저항도전막의 구성원자와 비단결정도전체

GF Exhibit 1124 - 1797/2704

막의 구성원자사이의 양막의 계면부근에서의 치환을 제한하여, 입자경계를 따른 저저항도전체의 국부적인 확산을 억제하고 게이트전극의 전기저항을 균일하게 감소시켜 신뢰성을 향상시킨 반도체장치의 제조방법을 제공하는데 있다.

본 발명의 다른 목적은 절연막상에 비단결정도전체막을 형성하는 공정과, 상기 비단결정도전체막속에 최소한 한 종류의 원자를 도입하여 원자도입층을 형성하는 공정과, 상기 비단결정도전체막상에 저저항도전체막을 형성하는 공정과, 상기 비단결정도전체막상에 형성된 저저항도전체막을 열처리하는 공정을 포함하여, 비단결정도전체막표면으로부터 침입한 저저항도전체막의 원자가 원자도입층내에서 편재되거나 정지되는 특징을 지닌 반도체장치의 제조방법을 제공하는데 있다.

본 발명의 제조방법에 따라서, 비단결정도전체막으로 구성된 게이트전극상에 저저항도전체막을 형성하고 열처리하여 게이트전극을 저저항화하므로써, 비단결정도전체의 구성원자와 저저항도전체막의 구성원자와의 상호원자치환은 두막의 계면의 제한된 영역에서만 균일하게 일어날 수 있다.

더욱이, 게이트전극의 전기저항이 일정하게 저감됨과 동시에, 입자경계를 따른 저저항도전체의 국부적인 확신이 억제될 수 있어, 결국, 신뢰성이 향상된 반도체장치를 제공하는 것이 가능하다.

본 발명의 신규한 특징은 특히, 첨부한 청구범위에 나타내었고, 본 발명의 구성과 내용에 대해서는 기타 다른 목적들과 특징에 따라, 도면과 함께 상세한 설명으로 충분히 이해될 수 있을 것이다.

[제1실시예]

본 발명의 제1실시예는 제1도(a)-제1도(f)를 참조하여, 게이트전극에 다결정실리콘과, 티탄을 조합시킨 전계효과형 금속-산화물-반도체(MOS)와 관련하여 상세히 설명한다.

(I) 실리콘기판(100)의 능동영역 형성 예정부를 제외한 표면에 대략 700nm의 산화막(110)을 피일드 산화막으로서 선택적으로 형성하고, 능동영역 형성 예정부의 표면에 대략 10nm의 게이트산화막(120)을 형성하고, 상기 산화막(110)과 (120)상에 대략 200nm의 다결정 실리콘막(130)을 퇴적시키고, $POCl_3$를 사용해 인을 확산시켜 다결정실리콘막(130)을 저저항화하였다(제1도(a)).

(II) 다음 단계로, 다결정실리콘막(130)에 질소이온을 가속에너지 150KeV로 $1\times10^{15}\sim1\times10^{18}cm^{-2}$ 주입하고, 다결정실리콘막(130)의 중간부분에 원자도입층(140)을 형성하였다(제1도(b)).

(III) 물리증착법에 의해서, 대략 100nm의 얇은 티탄막(150)을 퇴적하였다(제1도(c)).

(IV) 500-1000℃에서 10초간 신속하에 열어니일링하거나 500-1000℃에서 30분동안 용광로어니일링에 의한 열처리에 의해서, 질화티탄 및 티탄 실리사이드가 생성되어, 합금화층(160)이 형성되었다(제1도(d)).

(V) 다음 단계로, 포토마스크공정으로 저항패턴을 생성하고, 게이트전극 형성 예정부 및 그의 주변부부 이외의 다른 부분을 건식 에칭하여, 게이트전극을 형성하였다(제1도(e)).

(VI) 마지막으로, 가속에너지 80KeV로 As 이온을 $4\times10^{15}cm^{-2}$ 주입하여, 소오스영역(170) 및 드레인영역(180)을 형성하였다(제1도(f)).

이상의 일련의 공정에 의해서, 소망하는 전계효과형 트랜지스터가 형성되었다.

질소원자도입층(140)은 다결정실리콘 보다는 티탄과 반응하기 훨씬 쉽고, 원자도입층(140) 및 그의 윗부분에서 대부분의 합금화가 일어났다.

따라서, 합금화층의 두께가 균일하게 되므로, 게이트전극의 전기저항이 균일해지고 또한, 저저항도전체의 국부적인 확산도 거의 발생하지 않게 되어, 게이트산화막의 파괴를 방지할 수 있었다.

한편, 제1실시예의 공정(II)에서, 게이트산화막과 그 주변에 걸쳐서 상기 다결정층내에 원자도입층을 선택적으로 형성하고, 원자가 도입되지 않은 부분을 다음 공정의 저저항배선영역으로 사용하면, 이 부분에서는 저저항도전체막과 합금화층이 다결정실리콘막의 거의 전역에 퍼져서, 다결정실리콘과 저저항도전체막 사이의 접속저항을 낮출 수 있다.

그러므로, 게이트산화막에 대한 인가전계의 도전성은 개량된다.

배선영역아래의 산화막은 두꺼우므로, 저저항도전체가 산화막내에 국부적으로 확산되는 것은 문제가 되지 않는다.

이때에, 게이트산화막의 단부에서부터 저저항배선영역까지의 거리는 다음과 같이 규정되는 것이 바람직하다.

즉, 저저항도전체막의 구성원자가 저저항배선영역으로부터 원자도입영역의 하부를 통하여 확산되어 게이트 산화막의 단부까지 침입하고 있으므로, 이런 확산길이보다도 긴 길이로 설정하는 것이 바람직하다.

본 발명의 제1실시예에 있어서는, 저저항도전체로서 티탄을 사용하고, 원자도입층의 구성원자로서 질소를 사용하였으나, 저저항도전체로서 다른 고융점금속 또는 이것의 실리사이드를 사용해도 되며, 원자도입층의 구성원자로서 산소 또는 실리콘 또는 불활성 원자를 사용해도 게이트절연막의 파괴를 방지할 수 있다.

그러나, 저저항도전체막의 구성원자와 전자도입층의 구성원자의 조합에 의해, 게이트절연막의 파괴를 방지하는 메타니즘은 다양하다.

본 발명의 제1실시예인 티탄과 조합의 경우, 즉, 원자도입층의 구성원자가 비단결정도전체의 구성원자보다 저저항전체의 구성원자와 더욱 쉽게 반응할때, 원자도입층의 구성원자와 저저항도전체의 구

GF Exhibit 1124 - 1798/2704

성원자는 서로 반응하여 균일한 합금화층을 형성하고, 저저항도전체의 국부적인 확산이 억제됨으로써 게이트절연막의 파괴를 방지한다.

또, 비단결정도전체막과 저저항도전체막사이의 접속저항이 느려, 인가된 전계에 대한 게이트산화막의 내구력은 우수하다.

또한, 텅스텐과 산소를 조합하는 경우, 즉, 원자도입층의 구성원자가 저저항도전체막의 구성원자보다 비단결정도전체막의 구성원자와 더욱 쉽게 반응하면, 저저항도전체막의 구성원자의 확산은 원자도입층내에서 저지되고, 저저항도전체의 극부적인 확산은 억제되어 게이트절연막의 전기적 파괴를 방지한다.

그러므로 저저항화시 저저항도전체막의 막두께가 증가되면, 게이트절연막의 파괴는 효과적으로 방지될 수 있다.

또한, 원자도입층을 형성하기 위하여 도입되는 원자는, 1종류 또는 복수종류이어도 된다.

[제2실시예]

본 발명의 제조방법은 게이트전극에 다결정실리콘 및 텅스텐을 조합시킨 전계효과형 트랜지스터에 관한 것으로 제2도(a)-제2도(g)를 참조하여 상세히 설명한다.

(I) 실리콘기판(200)의 능동영역 형성예정부를 제외한 표면상에, 대략 700nm의 산화막(210)을 피일드 산화막으로서 선택적으로 형성하고, 대략 10nm의 게이트산화막(220)을 능동영역 형성예정부의 표면상에 형성하고, 상기 산화막(210)과 (220)상에 대략 200nm의 다결정실리콘막(230)을 퇴적한 후, $POCl_3$를 사용해 인을 확산시켜서 다결정실리콘막(230)을 저저항화하였다(제2도(a)).

(II) 다음에, 다결정실리콘막(230)속으로 산소이온을 가소에너지 40keV로 $1\times10^{15}$$1\times10^{18}cm^{-2}$ 주입하고 열처리하여, 다결정실리콘막(230)의 중간 부분에 실리콘산화물의 제1원자도입층(240)을 형성하였다(제2도(b)).

(III) 다음단계로, 다결정실리콘막(230)의 표면상에 실리콘이온을 가속에너지 2keV로 1×10^{15}-$1\times10^{18}cm^{-2}$ 주입하고 열처리하여, 다결정실리콘막(230)의 표면상에 무정형실리콘으로 구성된 제2원자도입층(290)을 형성하였다(제2도(c)).

(IV) 물리증착법에 의해서 대략 100nm의 얇은 텅스텐막(250)을 퇴적하였다(제2도(d)).

(V) 500-1000℃에서 10초간 신속하게 열어니일링하거나 500-1000℃에서 30분간 전기오븐에서 열처리하면, 텅스텐 실리사이드에 의한 합금화층(260)이 다결정실리콘막(230)의 표면근처에 형성되었다(제2도(e)).

(VI) 포토마스크공정으로 저항패턴을 형성하여, 게이트전극 형성예정부 및 그의 주변부 이외의 부분을 건식 에칭하여 게이트전극을 형성하였다(제2도(f)).

(VII) As 이온을 가속에너지 80keV로 $4\times10^{15}cm^{-2}$ 주입하여, 소오스영역(270)과 드레인영역(280)을 최종적으로 형성하였다(제2도(g)).

상기 일련의 공정에서, 소망하는 전계효과형 트랜지스터가 형성되었다.

제2원자도입층(290)내의 무정형 실리콘은 다결정실리콘보다 텅스텐과 훨씬 쉽게 반응하여 원자도입층과 그 윗부분에서 대부분의 합금화가 일어났다.

그러므로, 두께가 균일한 우수한 합금화층이 얻어졌다.

텅스텐원자의 이동영역은 제2원자도입층(290)의 근처에서 정지되는 것이 가능하였으나, 약간의 텅스텐 원자가 제2원자도입층(290)을 통하여 침투하였다.

그러나, 제1원자도입층(240)내의 실리콘산화물은 효과적으로 텅스텐을 저지하여 대부분의 합금화는 원자도입층(240)의 윗부분으로 제한되었다.

합금화층(260)의 두께가 매우 균일하였으므로, 게이트전극의 전기저항이 균일해지고, 저저항도전체의 국부적인 확산도 덜 발생하여, 게이트산화막의 파괴를 방지할 수 있었다.

본 발명에서는, 제1원자도입층을 형성하는 방법으로서, 이온주입방법을 사용하였으나, 다음의 방법을 사용해도 된다.

즉, 게이트산화막상에 제1층으로서 대략 100nm의 다결정실리콘을 퇴적하고, 이 다결정실리콘막의 게이트전극 형성예정부 및 그의 주변부의 표면상에, 수 nm의 얇은 실리콘막을 선택적으로 형성하여, 대략 100nm의 제2의 다결정실리콘층을 퇴적하고, 이와 같이 선택적으로 형성된 수 nm의 실리콘산화막을 제1원자도입층으로 사용해도 된다.

반면, 제2원자도입층(290)은 선택적으로 형성해도 되나, 적어도 게이트전극 형성예정부와 그의 주변부상에 형성되어야 한다.

[제3실시예]

본 발명의 제조방법은 게이트전극에 다결정실리콘 및 텅스텐을 조합시킨 전계효과형 트랜지스터에 관한 것으로 제3도(a)-제3도(g)를 참조하여 이하 상세히 설명한다.

(I) 실리콘기판(300)의 능동영역 형성예정부를 제외한 표면에 대략 700nm의 산화막(310)을 피일드산화막으로서 선택적으로 형성하고, 능동영역 형성예정부의 표면에 대략 10nm의 게이트산화막(320)을

GF Exhibit 1124 - 1799/2704

형성한 후, 상기 산화막(310)과 (320)상에 대략 100㎚의 다결정 실리콘막(330)을 퇴적시키고, $POCl_3$를 사용해 인을 확산시켜 다결정실리콘막(330)을 저저항화 하였다(제3도(a)).

(II) 다음 단계로 다결정실리콘막(330)에 산소이온을 가속에너지 10keV로 1×10^{15}-$1\times10^{18}cm^{-2}$ 주입하고 열처리하여, 다결정실리콘막(330)의 표면에 실리콘산화물의 제1원자도입층(340)을 형성하였다(제3도(b)).

(III) 물리증착법에 의해서, 대략 100㎚의 얇은 텅스텐막(350)을 퇴적하였다(제3도(c)).

(IV) 얇은 텅스텐막(350)의 표면상에, 실리콘이온을 가속에너지 20keV로 1×10^{15}-$1\times10^{18}cm^{-2}$ 주입하고, 얇은 텅스텐막(350)내부에 실리콘으로 구성된 제2원자도입층(390)을 형성하였다(제3도(d)).

(V) 500-1000℃에서 10초간 신속하게 열어니일링하거나 500-1000℃에서 30분동안 용광로 어니일링을 통한 열처리에 의해서 얇은 텅스텐막(350)의 내부에 텅스텐 실리사이드의 합금화층(360)을 형성하였다(제3도(e)).

(VI) 다음 단계로, 포토마스크공정으로 저항패턴을 형성하고, 게이트전극 형성 예정부와 그의 인접부분 이외의 다른 부분을 건식 에칭하여, 게이트전극을 형성하였다(제3도(f)).

(VII) 마지막으로, 가속에너지 80keV로 As이온을 $4\times10^{15}cm^{-2}$ 주입하여, 소오스영역(370)과 드레인영역(380)을 형성하였다(제3도(g)).

이상의 일련의 공정에서, 소망하는 전계효과형 트랜지스터가 형성되었다.

제2원자도입층(390)내의 실리콘은 결정형이 아니고, 다결정실리콘 보다는 텅스텐과 훨씬 쉽게 반응하여 제2원자도입층(390)의 근접부에서 대부분의 합금화가 일어났다.

그러므로, 두께가 균일한 우수한 합금화층이 얻어졌다.

텅스텐원자의 이동영역은 제2원자도입층(390)내에 거의 국한되고, 약간의 텅스텐원자는 제2원자도입층(390)에 의해 국한되지 않았으나, 제2원자도입층(390)내에 실리콘산화물은 효과적으로 텅스텐을 방해하여, 대부분의 합금화가 제1원자도입층(340)의 윗부분으로 제한되었다.

합금화층(360)의 두께가 매우 균일하였으므로, 게이트전극의 전기저항이 균일해지고, 또 저저항도전체의 국부적인 확산은 거의 발생되지 않아 게이트산화막의 파괴를 방지할 수 있었다.

[제4실시예]

본 발명의 제조방법은 게이트전극에 다결정실리콘 및 텅스텐을 조합시킨 전계효과형 트랜지스터의 제4실시예에 관한 것으로 제4도(a)-제4도(f)를 참조하여 이하 설명한다.

(I) 실리콘기판(400)의 능동영역 형성예정부를 제외한 표면에 대략 700㎚의 산화막(410)을 피일드산화막으로 선택적으로 형성하고, 능동영역 형성예정부의 표면에 대략 10㎚의 게이트산화막(420)을 형성하여, 상기 산화막(410)과 (420)상에 대략 200㎚의 다결정실리콘막(430)을 퇴적시킨 후, $POCl_3$를 사용해 인을 확산시켜 다결정실리콘막(430)을 저저항화 하였다(제4도(a)).

(II) 물리증착법에 의해서, 대략 100㎚의 얇은 텅스텐막(450)을 퇴적하였다(제4도(b)).

(III) 이런 얇은 텅스텐막(450) 상에 산소이온을 가속에너지 60keV로 $1\times10^{15}\sim1\times10^{18}cm^{-2}$ 주입하여, 얇은 텅스텐막(450)과 다결정실리콘막(430) 사이의 계면부근에 실리콘산화물의 원자도입층(440)을 형성하였다(제4도(c)).

(IV) 다음에, 500-1000℃에서 10초간 신속하게 열어니일링하여, 다결정실리콘막(430)과 얇은 텅스텐막(450)사이의 계면부근에 텅스텐실리사이드의 합금화층(460)를 형성하였다(제4도(d)).

(V) 포토마스크공정에서 저항패턴을 형성하고 게이트전극 형성예정부와 그의 주변부이외의 부분을 건식 에칭하여 게이트전극을 형성하였다(제4도(e)).

(VI) 마지막으로, 가속에너지 80keV로 As 이온을 $4\times10^{15}cm^{-2}$ 주입하여, 소오스영역(470)과 드레인영역(480)을 형성하였다(제4도(f)).

이상의 일련의 공정에서, 소망하는 전계효과형 트랜지스터가 형성되었다.

원자도입층(440)의 실리콘산화물은 효과적으로 텅스텐을 방해하여, 대부분의 합금화는 원자도입층의 위부분으로 한정되었다.

합금화층(460)의 두께가 매우 균일하였으므로, 게이트전극의 전기저항이 균일해지고, 저저항도전체의 국부적인 확산도 덜 발생되어 게이트산화막의 파괴를 방지할 수 있었다.

본 발명의 제4실시예에서는, 이온주입에 의해 원자도입층을 형성한 후에도 저저항도전체막을 그대로 사용하였으나, 원자도입층형성후에 이 저저항도전체층의 일부 또는 전부를 제거해도 되며, 동일 또는 다른 저저항도전체막을 다시 퇴적해도 된다.

예를 들면, 이온주입을 위하여 사용된 제1저저항도전체층의 두께를 감축할 수 있으므로, 이온주입의 가속에너지를 저감할 수 있다.

또한, 저저항도전체막을 제거하지 않고, 동일 또는 다른 저저항도전체막을 퇴적하여 복수층의 막을 형성해도 된다.

GF Exhibit 1124 - 1800/2704

예를 들면, 텅스텐막상에 티틴막을 퇴적시키므로서, 보다 좋은 저저항화를 기대할 수 있다.

본 발명의 제4실시예에서는, 저저항도전체로서 텅스텐을 사용하고, 원자도입층의 구성원자로서 산소를 사용하였으나, 제1실시예에서와 같이, 저저항도전체로서 다른 고융점금속 또는 이것의 실리사이드를 사용해도 되며, 원자도입층의 구성원자로서 질소, 실리콘 또는 불활성원자를 사용하면, 게이트절연막의 파괴를 방지하는 동일효과를 얻을 수 있다.

마찬가지로, 원자도입층의 구성원자가 비단결정도전체의 구성원자보다 저저항도전체의 구성원자와 훨씬 쉽게 반응하는 조합의 경우, 저저항도전체의 구성원자와 원자도입층의 구성원자의 상호반응에 의해 균일한 합금화층이 형성되고, 저저항도전체의 국부적인 확산을 억제하여서 게이트절연막의 파괴를 방지하게 된다.

또한, 원자도입층의 구성원자가 저저항도전체의 구성원자보다 비단결정도전체의 구성원자와 훨씬 쉽게 반응하는 조합의 경우, 원자도입층내에서의 저저항도전체내의 구성원자의 확산을 억제하고, 저저항도전체의 국부적인 확산을 억제하여서 게이트절연막의 파괴를 또한 방지한다.

본 발명의 방법에 따라서, 전계효과형 트랜지스터가 게이트전극물질로서 열처리에 의한 다결정실리콘의 합금화를 이용하여 형성되면, 이때, 합금화층의 두께는 상기 설명한 바와 같이 균일해지고, 저저항도전체의 국부적인 확산에 기인한 게이트절연막의 파괴를 방지할 수 있다.

본 발명의 바람질한 실시예로서, 원자도입층을 고조사된 이온주입방법에 의해 형성하는 경우, 이온주입시 발생하는 표면상의 전기전하는 저저항도전체막을 통하여 효과적으로 제거될 수 있으므로, 게이트절연막의 전기적파괴도 방지할 수 있다.

이상, 본 발명의 특정실시예를 기술하였지만, 다른 변형과 변화도 당업자에 의해 실현될 수 있다.

그러므로 본 발명의 정신과 범위를 벗어나지 않는한 이런 모든 변형과 변화를 첨부한 청구범위내에 포함시키고자 한다.

(57) 청구의 범위

청구항 1

기판(100)위에 비단결정도전체막(130)을 형성하는 공정과, 상기 비단결정도전체막내부에 원자를 도입하므로써 원자도입층(140)을 형성하는 공정과, 상기 원자도입층이 형성된 비단결정도전체막상에 저저항도전체막(150)을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

청구항 2

제1항에 있어서, 기판(100)의 표면위에 절연막(120)을 형성하고, 상기 절연막을 게이트절연막(120)으로서 사용하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 3

제2항에있어서, 반도체장치의 능동영역 형성예정부 상부와 그 근방의 비단결정도전체막내부에만 선택적으로 원자도입층(140)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 4

제3항에 있어서, 저저항도전체층(150)을 구성하고 있는 원자가, 원자도입층(140)아래의 하부층을 통해서 확산되어 반도체장치의 능동영역 형성예정부의 단부로 침입하는 것을 방지하도록 충분한 거리로 설계된 것을 특징으로 하는 반도체장치의 제조방법.

청구항 5

제4항에 있어서, 이온주입에 의해 원자를 도입하므로서 비단결정도전체막(130)내부에 원자도입층(140)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 6

기판(400)위에 비단결정도전체막(430)을 형성하는 공정과, 상기 비단결정 도전체막상에 저저항도전체막(450)을 형성하는 공정과, 상기 비단결정도전체막과 상기 저저항도전체막내부중 적어도 한쪽에 원자를 도입하므로서 원자도입층(440)을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

청구항 7

제6항에 있어서, 비단결정도전체막(430)상에 형성된 저저항도전체막(450)을, 원자도입층(440)을 형성한 후 제거하고, 비단결정도전체막상에 다시 저저항도전체막(450)을 형성하는 것을 특징으로 하는 반도체 장치의 제조방법.

청구항 8

제7항에 있어서, 저저항도전체막(450)은 다층막을 형성하도록 비단결정도전체막(430)상에 복수회 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 9

제8항에 있어서, 이온주입에 의해 원자를 도입하므로서 비단결정도전체막(430) 내부에 원자도입층

GF Exhibit 1124 - 1801/2704

(440)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 10

기판(200)위에 비단결정도전체막(230)을 형성하는 공정과, 상기 비단결정도전체막내부에 제1원자를 도입하므로서 제1원자도입층(240)을 형성하는 공정과, 상기 비단결정도전체막내부에 제2원자를 도입하므로서 상기 제1원자도입층을 깊이보다도 얕게 제2원자도입층(290)을 형성하는 공정과, 상기 두 개의 원자도입층(240),(290)이 형성된 비단결정도전체막상에 저저항도전체막(250)을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

청구항 11

제10항에 있어서, 반도체장치의 능동영역 형성예정부상부와 그 근방의 비단결정도전체막내부에만 선택적으로 제1원자도입층(240)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 12

제11항에 있어서, 저저항도전체막(250)을 구성하고 있는 원자가, 제1원자도입층(240)아래의 하부층을 통해서 확산되어 반도체장치의 능동영역 형성예정부의 단부로 침입하는 것을 방지하도록 충분한 거리로 설계된 것을 특징으로 하는 반도체장치의 제조방법.

청구항 13

제12항에 있어서, 비단결정도전체막(230)을 적어도 두 번 퇴적하여 형성하고, 첫 번째 퇴적후 비단결정도전체의 표면근방에 제1원자로 구성된 제1원자도입층(240)을 형성한 후에만, 비단결정도전체막의 다음 퇴적을 시행하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 14

제13항에 있어서, 이온주입에 의해 원자를 도입하므로서 비단결정도전체막(230)내부에 원자도입층(240)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 15

기판(300)위에 비단결정도전체막(330)을 형성하는 공정과, 상기 비단결정도전체막내부에 제1원자를 도입하므로서 제1원자도입층(340)을 형성하는 공정과, 상기 제1원자도입층이 형성된 비단결정도전체막상에 저저항도전체막(350)을 형성하는 공정과, 상기 비단결정도전체막상에 형성된 저저항도전체막 내부에 제2원자를 도입하므로서 제2원자도입층(390)을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

청구항 16

제15항에 있어서, 반도체장치의 능동영역 형성예정부 상부와 그 근방의 비단결정도전체막내부에만 선택적으로 제1원자도입층(340)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 17

제16항에 있어서, 저저항도전체막(350)을 구성하고 있는 원자가, 제1원자도입층 아래의 하부층을 통해서 확산되어 반도체장치의 능동영역 형성예정부 단부로 침입하는 것을 방지하도록 충분한 거리로 설계된 것을 특징으로 하는 반도체장치의 제조방법.

청구항 18

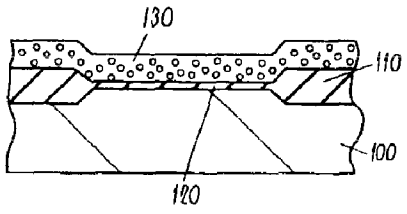
제17항에 있어서, 비단결정도전체막(330)을 적어도 두번 퇴적하여 형성하고, 첫번째 퇴적후 비단결정도전체의 표면근방에 제1원자로 구성된 제1원자도입층(340)을 형성한 후에만, 비단결정도전체막의 다음 퇴적을 시행하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 19

제18항에 있어서, 이온주입에 의해 원자를 도입하므로서 비단결정도전체막(330)내부에 원자도입층(340)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

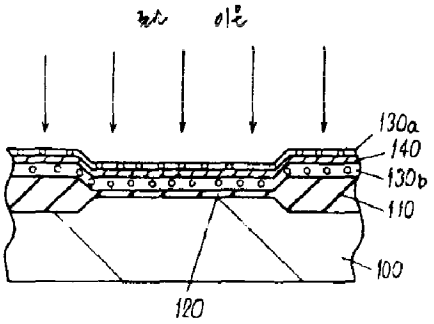
도면

도면1A

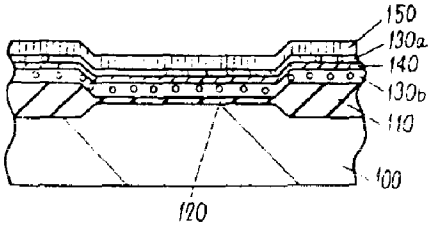


GF Exhibit 1124 - 1802/2704

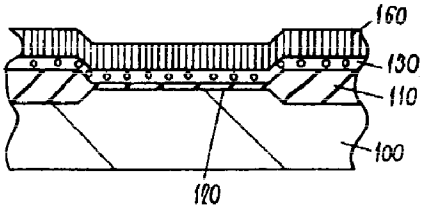
도면1-B



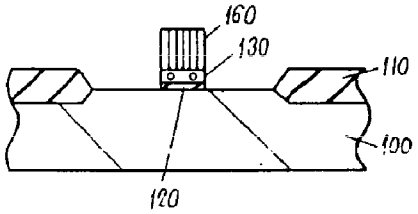
도면1-C



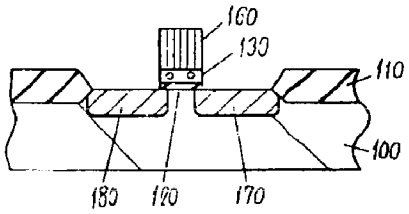
도면1-D



도면1-E

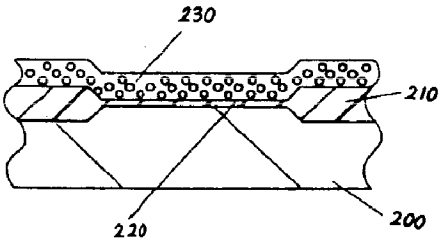


도면1-F

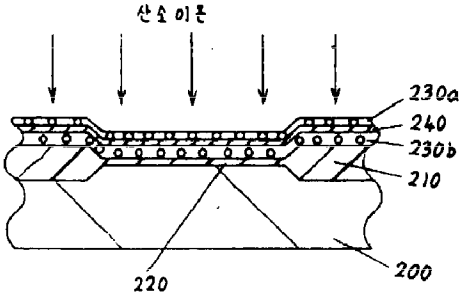


GF Exhibit 1124 - 1803/2704

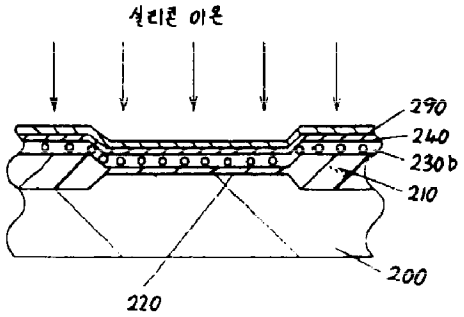
도면2-A



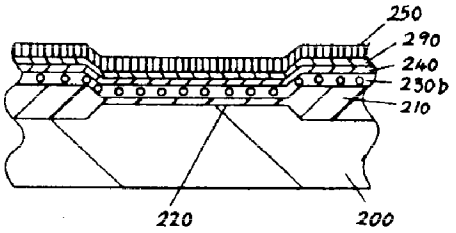
도면2-B



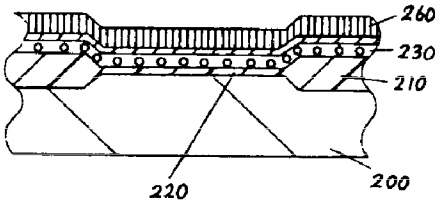
도면2-C



도면2-D

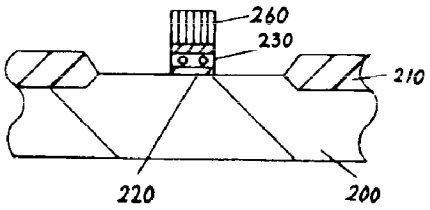


도면2-E

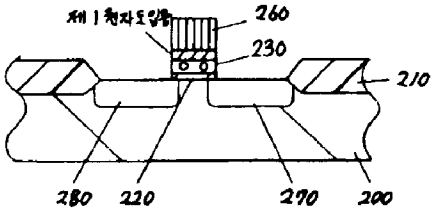


GF Exhibit 1124 - 1804/2704

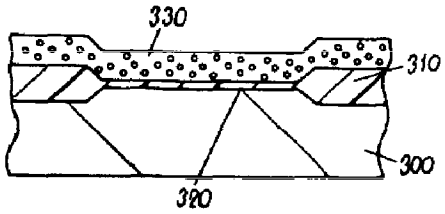
도면2-f



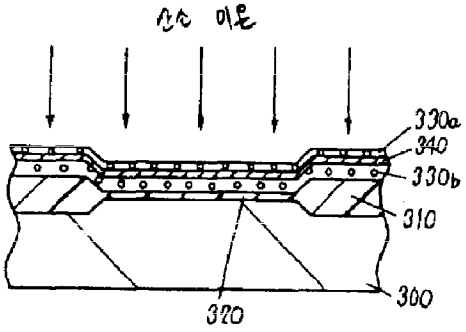
도면2-g



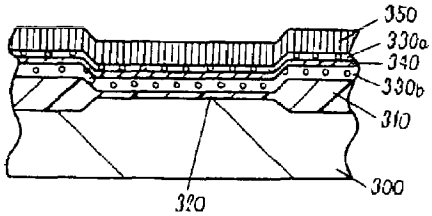
도면3-a



도면3-b

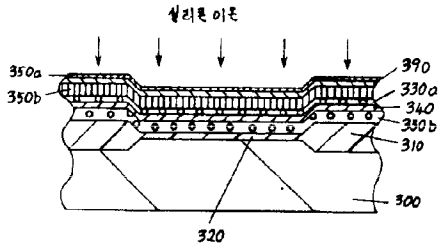


도면3-c

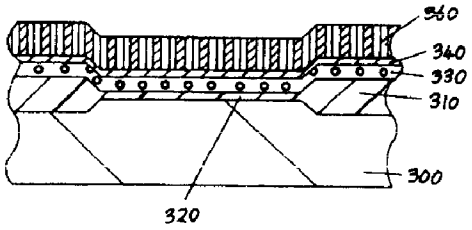


GF Exhibit 1124 - 1805/2704

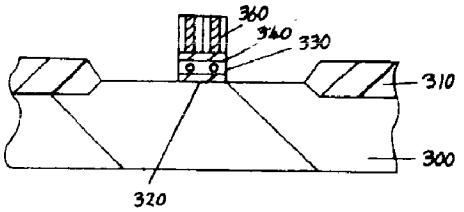
도면3-D



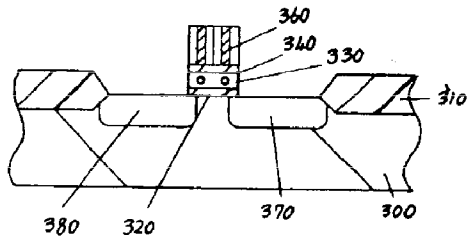
도면3-E



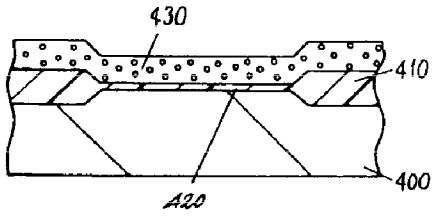
도면3-F



도면3-G

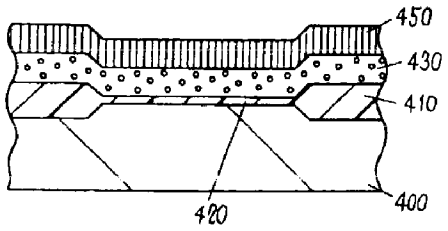


도면4-A

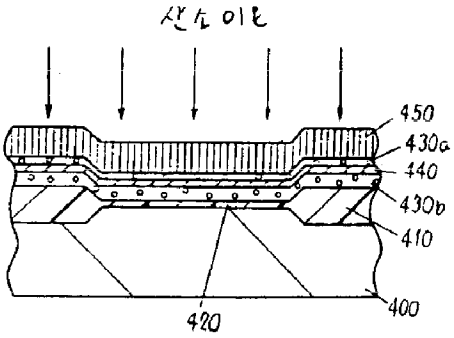


GF Exhibit 1124 - 1806/2704

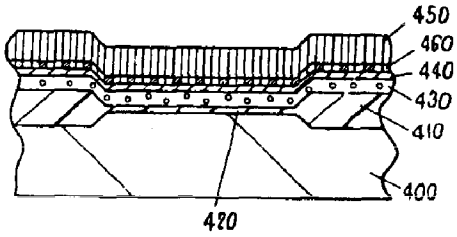
도면4-B



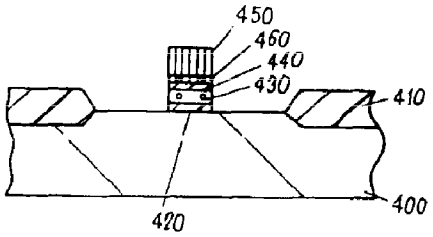
도면4-C



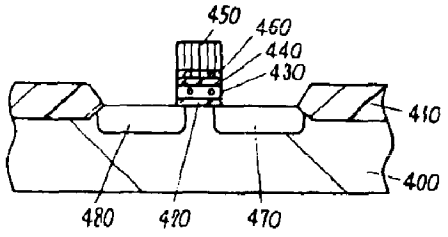
도면4-D



도면4-E



도면4-F



GF Exhibit 1124 - 1807/2704

Examined Patent Publication(B1)

Bibliographic Data

Int.Cl.	H01L 21/28 | H01L 21/02 | H01L 21/265 | H01L 21/768
Published Date	19920321
Registration No.	1000528040000
Registration Date	19920706
Application No.	1019880005839
Application Date	19880519
Unexamined Publication No.	1019880014685
Unexamined Publication Date	19881224
Priority Claims	62-124221 | 19870521 | JP
Requested Date of Examination	19880519
Agent.	SHIN, Joong Hoon
Inventor	GoBuSiGaJeuHiRo | GaMeYaMaSyuUIJji | OGaDaSyoOJyoO | JjeuJiGaJeuHiGo
Applicant	PANASONIC CORPORATION
Rightholder	-Maysushita electric ind.

발명의 명칭

반도체장치의제조방법

Title of Invention

Method for fabricating semiconductor device.

요약

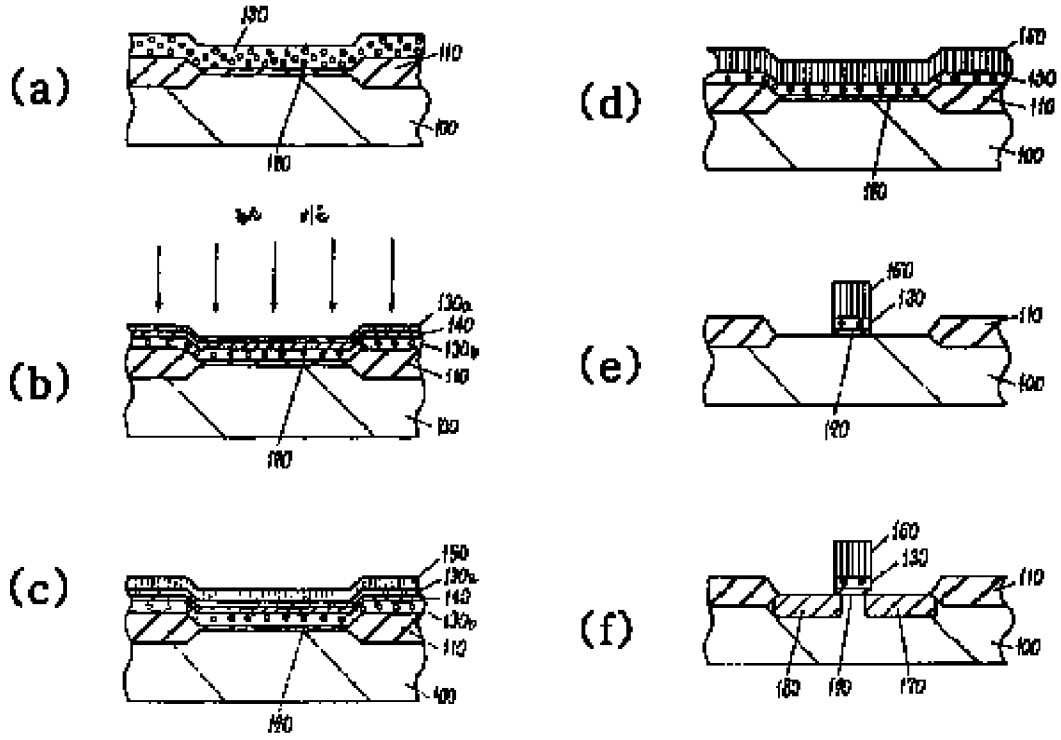
내용 없음.

Abstract

Content none.

대표도면(Representative drawing)

GF Exhibit 1124 - 1808/2704



청구의 범위

청구 1항:

기판(100)위에 비단결정도전체막(130)을 형성하는 공정과, 상기 비단결정도전체막내부에 원자를 도입하므로써 원자도입층(140)을 형성하는 공정과, 상기 원자도입층이 형성된 비단결정도전체막상에 저저항도전체막(150)을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

청구 2항:

제1항에 있어서, 기판(100)의 표면위에 절연막(120)을 형성하고, 상기 절연막을 게이트절연막(120)으로서 사용하는 것을 특징으로 하는 반도체장치의 제조방법.

청구 3항:

제2항에있어서, 반도체장치의 능동영역 형성예정부 상부와 그 근방의 비단결정도전체막내부에만 선택적으로 원자도입층(140)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구 4항:

제3항에 있어서, 저저항도전체층(150)을 구성하고 있는 원자가, 원자도입층(140)아래의 하부층을 통해서 확산되어 반도체장치의 능동영역 형성예정부의 단부로 침입하는 것을 방지하도록 충분한 거리로 설계된 것을 특징으로 하는 반도체장치의 제조방법.

Scope of Claims

Claim 1:

The method for fabricating semiconductor device consisting of the process of forming the non-single crystal conductor film (130) on the substrate (100), the process of forming the atom introduction layer (140) by introducing the atom inside the non-single crystal conductor film, and the process of forming the low resistance conductor film (150) on the non-single crystal conductor film, and as to the process of, the atom introduction layer is formed.

Claim 2:

As for claim 1, the method for fabricating semiconductor device which forms the insulating layer (120) on the surface of the substrate (100) ; and uses the insulating layer as the gate insulating layer (120).

Claim 3:

As for claim 2, the method for fabricating semiconductor device which selectively forms the atom introduction layer (140) inside the active region formation presumptive region upper portion of the semiconductor device and non-single crystal conductor film of the neighborhood.

Claim 4:

As for claim 3, the method for fabricating semiconductor device which is designed to enough distance in order to prevent being diffused through the valence comprising the low resistance conductive filler layer (150), and the sub-layer under the atom introductio

GF Exhibit 1124 - 1809/2704

n layer (140) and entering into the end of the active re gion formation presumptive region of the semiconductor device forcibly.

청구 5항:

제4항에 있어서, 이온주입에 의해 원자를 도입하므로서 비단결정도전체막(130)내부에 원자도입층(140)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 5:

As for claim 4, the method for fabricating semiconductor device which forms the atom introductio n layer (140) inside the non-single crystal conductor fil m (130) since it introduces the atom with the ion impla ntation.

청구 6항:

기판(400)위에 비단결정도전체막(430)을 형성하는 공정과, 상기 비단결정 도전체막상에 저저항도전체막(450)을 형성하는 공정과, 상기 비단결정도전체막과 상기 저저항도전체막내부중 적어도 한쪽에 원자를 도입하므로서 원자도입층(440)을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

Claim 6:

The method for fabricating semiconductor device consisting of the process of forming the non-single cry stal conductor film (430) on the substrate (400), the p rocess of forming the low resistance conductor film (45 0) on the non-single crystal conductor film, and the no n-single crystal conductor film and the process of formi ng the atom introduction layer (440) among the low res istance conductor film inside since it introduces the ato m to at least one side.

청구 7항:

제6항에 있어서, 비단결정도전체막(430)상에 형성된 저저항도전체막(450)을, 원자도입층(440)을 형성한 후 제거하고, 비단결정도전체막상에 다시 저저항도전체막(450)을 형성하는 것을 특징으로 하는 반도체 장치의 제조방법.

Claim 7:

As for claim 6, the method for fabricating semiconductor device which removes the atom introdu ction layer (440) the formed low resistance conductor f ilm (450) on the non-single crystal conductor film (430) after doing the formation ; and again forms the low resi stance conductor film (450) on the non-single crystal c onductor film.

청구 8항:

제7항에 있어서, 저저항도전체막(450)은 다층막을 형성하도록 비단결정도전체막(430)상에 복수회 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 8:

As for claim 7, the method for fabricating semiconductor device which it forms on the non-single crystal conductor film (430) so that the low resistance conductor film (450) forms the multilayer.

청구 9항:

제8항에 있어서, 이온주입에 의해 원자를 도입하므로서 비단결정도전체막(430) 내부에 원자도입층(440)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 9:

As for claim 8, the method for fabricating semiconductor device which forms the atom introductio n layer (440) inside the non-single crystal conductor fil m (430) since it introduces the atom with the ion impla ntation.

청구 10항:

기판(200)위에 비단결정도전체막(230)을 형성하는 공정과, 상기 비단결정도전체막내부에 제1원자를 도입하므로서 제1원자도입층(240)을 형성하는 공정과, 상기 비단결정도전체막내부에 제2원자를 도입하므로서 상기 제1원자도입층을 깊이보다도 얕게 제2원자도입층(290)을 형성하는 공정과, 상기 두 개의 원자도입층(240),(290)이 형성된 비단결정도전체막상에 저저항도전체막(250)을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

Claim 10:

The method for fabricating semiconductor device consisting of the process of forming the non-single cry stal conductor film (230) on the substrate (200), the p rocess of forming the first circle toll dialing mouth layer (240) since it introduces the first circle person inside t he non-single crystal conductor film, the process it is s hallow than the depth of forming the second circle toll dialing mouth layer (290) said first circle toll dialing the mouth layer since it introduces the second circle perso n inside the non-single crystal conductor film, and the process of forming the low resistance conductor film (2 50) on the non-single crystal conductor film, and as to the process of, two atom introduction layers (240), an d (290) are formed.

GF Exhibit 1124 - 1810/2704

청구 11항:

제10항에 있어서, 반도체장치의 능동영역 형성예정부상부와 그 근방의 비단결정도전체막내부에만 선택적으로 제1원자도입층(240)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 11:

As for claim 10, the method for fabricating semiconductor device which selectively forms the first circle toll dialing mouth layer (240) inside the active re gion formation predetermine flotation part of the semic onductor device and non-single crystal conductor film of the neighborhood.

청구 12항:

제11항에 있어서, 저저항도전체막(250)을 구성하고 있는 원자가, 제1원자도입층(240)아래의 하부층을 통해서 확산되어 반도체장치의 능동영역 형성예정부의 단부로 침입하는 것을 방지하도록 충분한 거리로 설계된 것을 특징으로 하는 반도체장치의 제조방법.

Claim 12:

As for claim 11, the method for fabricating semiconductor device which is designed to enough dist ance in order to prevent being diffused through the val ence comprising the low resistance conductor film (25 0), and the sub-layer under the first circle toll dialing m outh layer (240) and entering into the end of the activ e region formation presumptive region of the semicondu ctor device forcibly.

청구 13항:

제12항에 있어서, 비단결정도전체막(230)을 적어도 두 번 퇴적하여 형성하고, 첫 번째 퇴적후 비단결정도전체의 표면근방에 제1원자로 구성된 제1원자도입층(240)을 형성한 후에만, 비단결정도전체막의 다음 퇴적을 시행하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 13:

As for claim 12, the method for fabricating semiconductor device which accumulates the non-singl e crystal conductor film (230) with at least twice and i t forms ; and implements the next deposition of the no n-single crystal conductor film the first circle toll dialing mouth layer (240) made up of the first circle person in the near surface of the non-single crystal conductor af ter the first deposition in the formation.

청구 14항:

제13항에 있어서, 이온주입에 의해 원자를 도입하므로서 비단결정도전체막(230)내부에 원자도입층(240)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 14:

As for claim 13, the method for fabricating semiconductor device which forms the atom introductio n layer (240) inside the non-single crystal conductor fil m (230) since it introduces the atom with the ion impla ntation.

청구 15항:

기판(300)위에 비단결정도전체막(330)을 형성하는 공정과, 상기 비단결정도전체막내부에 제1원자를 도입하므로서 제1원자도입층(340)을 형성하는 공정과, 상기 제1원자도입층이 형성된 비단결정도전체막상에 저저항도전체막(350)을 형성하는 공정과, 상기 비단결정도전체막상에 형성된 저저항도전체막내부에 제2원자를 도입하므로서 제2원자도입층(390)을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

Claim 15:

The method for fabricating semiconductor device consisting of the process of forming the non-single cry stal conductor film (330) on the substrate (300), the p rocess of forming the first circle toll dialing mouth layer (340) since it introduces the first circle person inside t he non-single crystal conductor film, the process of for ming the low resistance conductor film (350) on the no n-single crystal conductor film, and the process of form ing the second circle toll dialing mouth layer (390) sinc e it introduces the second circle person on the non-sin gle crystal conductor film inside the formed low resista nce conductor film, and as to the process of, said first circle toll dialing the mouth layer is formed.

청구 16항:

제15항에 있어서, 반도체장치의 능동영역 형성예정부 상부와 그 근방의 비단결정도전체막내부에만 선택적으로 제1원자도입층(340)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 16:

As for claim 15, the method for fabricating semiconductor device which selectively forms the first circle toll dialing mouth layer (340) inside the active re gion formation presumptive region upper portion of the semiconductor device and non-single crystal conductor film of the neighborhood.

GF Exhibit 1124 - 1811/2704

청구 17항:

제16항에 있어서, 저저항도전체막(350)을 구성하고 있는 원자가, 제1원자도입층 아래의 하부층을 통해서 확산되어 반도체장치의 능동영역 형성예정부 단부로 침입하는 것을 방지하도록 충분한 거리로 설계된 것을 특징으로 하는 반도체장치의 제조방법.

Claim 17:

As for claim 16, the method for fabricating semiconductor device which is designed to enough distance in order to prevent being diffused through the valence comprising the low resistance conductor film (350), and the sub-layer under the first circle toll dialing mouth layer and entering into the active region formation presumptive region end of the semiconductor device forcibly.

청구 18항:

제17항에 있어서, 비단결정도전체막(330)을 적어도 두번 퇴적하여 형성하고, 첫번째 퇴적후 비단결정도전체의 표면근방에 제1원자로 구성된 제1원자도입층(340)을 형성한 후에만, 비단결정도전체막의 다음 퇴적을 시행하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 18:

As for claim 17, the method for fabricating semiconductor device which accumulates the non-single crystal conductor film (330) with at least twice and it forms ; and implements the next deposition of the non-single crystal conductor film the first circle toll dialing mouth layer (340) made up of the first circle person in the near surface of the non-single crystal conductor after the first deposition in the formation.

청구 19항:

제18항에 있어서, 이온주입에 의해 원자를 도입하므로서 비단결정도전체막(330)내부에 원자도입층(340)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 19:

As for claim 18, the method for fabricating semiconductor device which forms the atom introduction layer (340) inside the non-single crystal conductor film (330) since it introduces the atom with the ion implantation.

상세설명

Detailed Description

[발명의 명칭]

[Title of invention]

반도체장치의 제조방법

Method for fabricating semiconductor device.

[도면의 간단한 설명]

[Brief description of drawings]

제1도는 본 발명의 제1실시예의 공정순서를 도시한 단면도.

Figure 1 is a cross-sectional view showing the processing procedure of the first preferred embodiment of the invention.

제2도는 본 발명의 제2실시예의 공정순서를 도시한 단면도.

Figure 2 is a cross-sectional view showing the processing procedure according to the second preferred embodiment of the present invention.

제3도는 본 발명의 제3실시예의 공정순서를 도시한 단면도.

Figure 3 is a cross-sectional view showing the processing procedure according to the third preferred embodiment of the present invention.

제4도는 본 발명의 제4실시예의 공정순서를 도시한 단면도.

Figure 4 is a cross-sectional view showing the processing procedure according to the fourth preferred embodiment of the present invention.

* 도면의 주요부분에 대한 부호의 설명

* The description of reference numerals showing the main elements in drawings.

100,200,300,400 : 실리콘기판 110,210,310,410 : 산화막

100,200,300,400: silicon substrate 110,210,310,410: oxide film.

120,220,320,420 : 게이트 산화막 130,230,330,430 : 다

120,220,320,420: gate oxidation film 130,230,330,430:

GF Exhibit 1124 - 1812/2704

결정 실리콘막

polysilicon layer.

140,440 : 원자도입층 150 : 얇은 티탄막

140,440: atom introduction layer 150: the thin titan film.

160,260,360,460 : 함금화층 170,270,370,470 : 소오스영역

160,260,360,460: box gold 300coin layer 170,270,370,470: source area.

180,280,380,480 : 드레인영역 240,340 : 제1원자도입층

180,280,380,480: drain region 240,340: first circle toll dialing mouth layer.

250,350,450 : 얇은 텅스텐막 290,390 : 제2원자도입층

250,350,450: the thin tungsten film 290,390: second circle toll dialing mouth layer.

[발명의 상세한 설명]

[Detailed description of the invention]

본 발명은 반도체장치의 제조방법에 관한 것으로, 특히 MOS형 집적회로등의 비(非)단결정도전체막과 저(低)저항도전체막으로 구성된 저저항화된 게이트전극의 전기적 특성을 개량하고, 또 게이트절연막의 절약파괴를 방지할 수 있는 제조방법에 관한 것이다.

The invention relates to the method for fabricating semiconductor device, and particularly, to the manufacturing method which improves the electrical characteristic of the gate electrode which becomes to have low-resistance consisting of the low resistance conductor film and non-single crystal conductor film including the MOS type integrated circuit etc. and can prevent and, the saving break down of the gate insulating layer.

전계효과형 반도체집적회로에서 미세하고 고성능의 트랜지스터를 얻기 위하여, 비단결정도전체막으로 구성된 게이트전극상에 저저항도전체막을 형성하고 열처리하여 게이전극의 저저항화를 일반적으로 실행한다.

In order that it is minute in the field effect type semiconductor IC(integrated circuit) and the transistor of the high effectiveness is obtained the low resistance conductor film is formed on the gate electrode consisting of the non-single crystal conductor film and it heat-treats and the low resistance of the gay electrode the generally is executed.

예를 들면, 저저항전도체로서, 고융점 금속 또는 실리콘과의 합금, 즉, 실리사이드는 다결정체실리콘상에 퇴적되어 게이트전극으로 사용되고, 약 500℃로 열처리 하면 고융점금속 또는 실리사이드는 쉽게 다결정체실리콘과 반응하여 전부 실리사이드속으로 변형됨으로써 저저항화가 된다.

For example, as the low resistance conductive material, it is accumulated in the polycrystal silicone phase and the alloy with the high melting point metal or the silicone, in other words, the silicide is used as the gate electrode and by if it heat-treats at about 500℃, the high melting point metal or the silicide reacting easily with the polycrystal silicone and being all transformed into inside the silicide it becomes to have low-resistance.

이렇게 형성된 도전체막의 시이트저항은 대략 1-10Ω/스퀘어로 낮아, 반도체집적회로의 고속작동이 예기된다.

The sheet resistance of the conductor film formed in this way is lower than approximately, 1-10Ω / specifying queries as relational expressions and the high-speed of the semiconductor IC(integrated circuit) is expected.

반면, 금속종류에 의존하여, 다결정체실리콘과는 다른 물질과 반응하고, 특히 티탄은 게이트 전극물질로서 사용되는 실리콘산화막과 반응하므로, 비록 이것이 매우 저저항이지만 게이트전극물질로 사용되기는 어렵다.

On the other hand, it depends on steel and it reacts with the material different from the polycrystal silicone and the material reacts to the silicon oxide film in which especially, titanium is used as the gate electrode material. Therefore this is difficult that it is the low resistance but this is very used as the gate electrode material.

따라서, 티탄보다는 약간 고저항이지만 실리콘산화막과는 거의 반응하지 않는, 텅스텐과 몰리브덴이 일반적으로 사용된다.

Therefore, a little bit is the high value resistor than titanium but tungsten and the molybdenum which nearly does not react are generally used with the silicon oxide film.

GF Exhibit 1124 - 1813/2704

이런 고융점금속 또는 실리사이드와 실리콘질화막 또는 실리콘산화막과의 반응성 및 반응물의 생성에너지는 N.G.Einsprach 편(Academic Press 출판)의 VLSI 전자공학 : 미세구조, 제9권, 제2장에 기재되어 있다.

The formation energy of the reactive reactant with such high melting point metal or the silicide and silicon nitride film or the silicon oxide film is the VLSI electronics of the No Good. Einsprach. piece (academic Press publication): it is written in the fine structure, the vol. 9, and the second field.

한편, 반응의 용이성은 활성화에너지의 크기에 의해 판단될 수 있으며, 활성화에너지가 작을수록 반응이 쉬워지는 것은 알려져 있다.

In the meantime, the simplicity of reaction can be determined by the size of the activation energy and the size is known that reaction becomes easy as the activation energy is small.

비단결정도전체막으로 구성된 게이트전극상에 저저항도전체막을 형성한 후 열처리하면, 비단결정도전체막과 저저항도전체막사이의 계면에서 상호의 구성원자가 이동하여, 계면부근이 합금화되어, 저저항화된다.

If the low resistance conductor film is heat-treated on the gate electrode consisting of the non-single crystal conductor film after doing the formation , the constitutional atom of reciprocity moves in the interface between the low resistance conductor film and the non-single crystal conductor film and the interface department radical is alloyed and it becomes to have low-resistance.

그러나, 비단결정도전체의 결정입자사이의 계면, 즉, 입자 경계에서, 비단결정도전체의 구성원자의 결합력이 약하므로, 저저항도전체막의 구성원자와의 원자의 치환이 결정입자내에서보다 빠르게 진행되어, 저저항도전체는 입자경계를 따라서 국부적으로 확산되는 경향이 있다.

But in the interface between the crystal particle of the non-single crystal conductor, in other words, the grain boundary, the connectivity of the constitutional atom of the non-single crystal conductor is weak. Therefore the substitution of the atom with the constitutional atom of the low resistance conductor film is rapidly launched than inside of the crystal particle and the low resistance conductor tends to be diffused according to the grain boundary.

저저항도전체가 국부적으로 확산되어 게이트전극 아래의 절연막을 찢게되면, 게이트전극이 다른 전극과 단락되어, 트랜지스터의 신뢰성 또는 제품의 수율을 저하시킨다.

If the low resistance conductor is locally diffused and the insulating layer under the gate electrode is torn , it is circuit-shorted with the electrode in which the gate electrode is different and the yield of the reliability of the transistor or the product is lowered.

이것을 방지하기 위해, 비단결정도전체와 저저항도전체 사이에 CVD(화학적 증착)에 의해 초박형의 실리콘질화막을 퇴적시켜 저저항도전체의 국부적인 확산을 억제하고 신뢰성을 증가시키는 방법이 IEEE Transactions of Electron Devices, Vol., ED-33, No.4, April 1986, pp. 464~467에 언급되어 있다.

In order that this is prevented the non-single crystal conductor and the method for sedimenting the silicon nitride film of the ultra thin between the low resistance conductor with the CVD (chemical vapor deposition) and suppressing the local diffusion of the low resistance conductor and increasing the reliability are mentioned in the IEEE Transactions of Electron Devices, vol, ED-33, no.4, april 1986, pp. 464~467.

그러나 이것은 막두께의 고재현성에서, CVD에 의한 초박편실리콘 질화막의 퇴적은 어렵고, 더욱이 비교적 낮은 온도에서의 퇴적과 불순물확산층내의 불순물의 재확산에 기인한 전기적 특성에의 변화를 방지하는 것이 필요하므로, 저저항도전체의 국부적 확산을 충분히 억제하는 조밀막성질을 얻기가 곤란하여, 신뢰성과 수율의 향상 또는 충분하지가 않았다.

But in this is the high reproducibility of the film thickness, the deposition of the ultra-thin section silicon nitride film by CVD was difficult and the change was necessary to prevent the change of the electrical characteristic of being caused by the respread of the impurity within the deposition at the relatively low temperature and impurity spreading layer. Therefore it was difficult to get the density coating property which enough suppressed the local diffusion of the low resistance conductor and it improved of the reliability and yield or it was not sufficient.

상기 문제점을 해결하기 위해 본 발명의 일차적 목적은 저저항도전막의 구성원자와 비단결정도전체막의 구성원자사이의 양막의 계면부근에서의 치환을 제한하여, 입자경계를 따른 저저항도전체의 국부적인 확산을 억제하고 게이트전극의 전기저항을 균일하게 감소시켜 신뢰성을 향상시킨 반도체장치의 제조방법을 제공하는데 있다.

To solve the problem, the primary object of the invention limits the substitution at the interface department radical of the amnion between the constitutional atom of the constitutional atom of the low resistance conductive film and the non-single crystal conductor film and the local diffusion of the low resistance conductor following the grain boundary is to be suppressed and th

GF Exhibit 1124 - 1814/2704

e electric resistance of the gate electrode is uniformly reduced and the method for fabricating semiconductor device improving the reliability is to be provided.

본 발명의 다른 목적은 절연막상에 비단결정도전체막을 형성하는 공정과, 상기 비단결정도전체막속에 최소한 한 종류의 원자를 도입하여 원자도입층을 형성하는 공정과, 상기 비단결정도전체막상에 저저항도전체막을 형성하는 공정과, 상기 비단결정도전체막상에 형성된 저저항도전체막을 열처리하는 공정을 포함하여, 비단결정도전체막표면으로부터 침입한 저저항도전체막의 원자가 원자도입층내에서 편재되거나 정지되는 특징을 지닌 반도체장치의 제조방법을 제공하는데 있다.

Another object of the invention is to provide the method for fabricating semiconductor device carrying t he characteristic in which the atom of the low resistan ce conductor film breaking from the non-single crystal conductor film surface is maldistributed including the pr ocess, of forming the non-single crystal conductor film on the insulating layer and the process, of introducing the atom of at least one kind in the non-single crystal conductor film and forming the atom introduction layer and the process, of forming the low resistance conduct or film on the non-single crystal conductor film and the process of heat-treating the formed low resistance con ductor film on the non-single crystal conductor film in t he atom introduction layer or which is stopped.

본 발명의 제조방법에 따라서, 비단결정도전체막으로 구성된 게이트전극상에 저저항도전체막을 형성하고 열처리하여 게이트전극을 저저항화하므로써, 비단결정도전체의 구성원자와 저저항도전체막의 구성원자와의 상호원자치환은 두막의 계면의 제한된 영역에서만 균일하게 일어날 수 있다.

According to the manufacturing method of the invention, the low resistance conductor film is formed o n the gate electrode consisting of the non-single cryst al conductor film and it heat-treats and the gate electr ode is made lower resistance. In that way the reciproci ty atom substitution with the constitutional atom of th e constitutional atom of the non-single crystal conduct or and low resistance conductor film uniformly can occ ur in the limited domain of the interface of two films.

더욱이, 게이트전극의 전기저항이 일정하게 저감됨과 동시에, 입자경계를 따른 저저항도전체의 국부적인 확신이 억제될 수 있어, 결국, 신뢰성이 향상된 반도체장치를 제공하는 것이 가능하다.

Furthermore, the electric resistance of the gate electrode is regularly reduced. Simultaneously the local assurance of the low resistance conductor following th e grain boundary can be suppressed and it is possible t o provide the semiconductor device in which in conclusi on, the reliability is improved.

본 발명의 신규한 특징은 특히, 첨부한 청구범위에 나타내었고, 본 발명의 구성과 내용에 대해서는 기타 다른 목적들과 특징에 따라, 도면과 함께 상세한 설명으로 충분히 이해될 수 있을 것이다.

It showed in the claims which the characteristic which is novel of the invention especially attached and it will be able to be enough understood as the detailed expla nation about configuration and content of the present i nvention according to the purposes and the characteri stic which the other is different with drawing.

[제1실시예]

[First preferred embodiment]

본 발명의 제1실시예는 제1도(a)-제1도(f)를 참조하여, 게이트전극에 다결정실리콘과, 티탄을 조합시킨 전계효과형 금속-산화물-반도체(MOS)와 관련하여 상세히 설명한다.

The first preferred embodiment of the invention the first (a) particularly illustrates with reference to the firs t (f) in the gate electrode in connection with the poly-crystal silicon, and the field effect type metal-oxide-se miconductor (MOS) combining titanium.

(I) 실리콘기파(100)의 농동영역 형성 예정부를 제외한 표면에 대략 700nm의 산화막(110)을 피일드 산화막으로서 선택적으로 형성하고, 능동영역 형성 예정부의 표면에 대략 10nm의 게이트산화막(120)을 형성하고, 상기 산화막(110)과 (120)상에 대략 200nm의 다결정 실리콘막(130)을 퇴적시키고, POCl3를 사용해 인을 확산시켜 다결정실리콘막(130)을 저저항화하였다(제1도(a)).

(I)Approximately, the oxide film (110) of 700nm was selectively formed on the surface except for the same field formation presumptive region of the silicon group wave (100) as the field oxide film and approximately, th e gate oxidation film (120) of 10nm was formed on the surface of the active region formation presumptive regi on and approximately, the polysilicon layer (130) of 200 nm was sedimented on the oxide film (110) and (120) a nd the phosphorus was diffused by using the POCl 3 an d the polysilicon layer (130) was made lower resistance (first (a)).

(II) 다음 단계로, 다결정실리콘막(130)에 질소이온을 가속에

(II)The nitrogen ion was injected into the polysilicon

GF Exhibit 1124 - 1815/2704

너지 150KeV로 1#215#1015~1#215#1018cm-2 주입하고, 다결정실리콘막(130)의 중간부분에 원자도입층(140)을 형성하였다(제1도(b)).

layer (130) to the following step to the acceleration energy 150KeV with 1× 10 15 ~1× 10 18 cm - 2 and the atom introduction layer (140) was formed on the middle part of the polysilicon layer (130)(first (b)).

(III) 물리증착법에 의해서, 대략 100nm의 얇은 티탄막(150)을 퇴적하였다(제1도(c)).

(III)Using the physical vapour deposition, the thin titan film (150) of 100nm was approximately accumulated(first (c)).

(IV) 500-1000℃에서 10초간 신속하에 열어니일링하거나 500-1000℃에서 30분동안 용광로어니일링에 의한 열처리에 의해서, 질화티탄 및 티탄 실리사이드가 생성되어, 합금화층(160)이 형성되었다(제1도(d)).

(IV)In 500-1000℃, annealed thermally under for 10 seconds rapid or the titane nitride and titanium silicide were generated in 500-1000℃ for 30 minutes with the thermal process by the blast furnace annealing and the alloy layer (160) was formed(first (d)).

(V) 다음 단계로, 포토마스크공정으로 저항패턴을 생성하고, 게이트전극 형성 예정부 및 그의 주변부부 이외의 다른 부분을 건식 에칭하여, 게이트전극을 형성하였다(제1도(e)).

(V)The resistance pattern was produced to the following step to the photo mask process and the dissimilar part except the gate electrode forming presumptive region and its peripheral unit part dry were etched and the gate electrode was formed(first (e)).

(VI) 마지막으로, 가속에너지 80KeV로 As 이온을 4#215#1015cm-2 주입하여, 소오스영역(170) 및 드레인영역(180)을 형성하였다(제1도(f)).

(VI)Finally, the As ion was injected to the acceleration energy 80KeV with 4× 10 15 cm - 2 and the source area (170) and drain region (180) were formed(first (f)).

이상의 일련의 공정에 의해서, 소망하는 전계효과형 트랜지스터가 형성되었다.

Using the series of process described in the above, the desired field effect transistor was formed.

질소원자도입층(140)은 다결정실리콘 보다는 티탄과 반응하기 훨씬 쉽고, 원자도입층(140) 및 그의 윗부분에서 대부분의 합금화가 일어났다.

The nitrogen atom introduction layer (140) was more easy than the poly-crystal silicon to react with titanium and most of alloyings occurred in the atom introduction layer (140) and its top.

따라서, 합금화층의 두께가 균일하게 되므로, 게이트전극의 전기저항이 균일해지고 또한, 저저항도 전체의 국부적인 확산도 거의 발생하지 않게 되어, 게이트산화막의 파괴를 방지할 수 있었다.

Therefore, it became uniformly the thickness of the alloy layer. Therefore the electric resistance of the gate electrode was uniform and moreover, the low resistance the local diffusion of whole was not generated and the break down of the gate oxidation film could be prevented.

한편, 제1실시예의 공정(II)에서, 게이트산화막과 그 주변에 걸쳐서 상기 다결정층내에 원자도입층을 선택적으로 형성하고, 원자가 도입되지 않은 부분을 다음 공정의 저저항배선영역으로 사용하면, 이 부분에서는 저저항도전체막과 합금화층이 다결정실리콘막의 거의 전역에 퍼져서, 다결정실리콘과 저저항도전체막 사이의 접속저항을 낮출 수 있다.

In the meantime, in the process (II) of the first preferred embodiment, the atom introduction layer is selectively formed through the gate oxidation film and around within the polycrystalline layer and if the part in which the atom is not introduced is used as the low resistance wiring domain of the next process , the low resistance conductor film and alloy layer nearly spread to all the area from the teeth of the polysilicon layer and the contact resistance between the low resistance conductor film and the poly-crystal silicon can be lowered.

그러므로, 게이트산화막에 대한 인가전계의 도전성은 개량된다.

Therefore, the conductivity of the applied field about the gate oxidation film is improved.

배선영역아래의 산화막은 두꺼우므로, 저저항도전체가 산화막내에 국부적으로 확산되는 것은 문제가 되지 않는다.

The oxide film under the wiring area is thick. Therefore it does not become a problem that the low resistance conductor is locally diffused within the oxide film.

이때에, 게이트산화막의 단부에서부터 저저항배선영역까지의 거리는 다음과 같이 규정되는 것이 바람직하다.

Even in this case, in the end of the gate oxidation film, it is the be desirable that the distance to the low resistance wiring domain is prescribed like the next.

즉, 저저항도전체막의 구성원자가 저저항배선영역으로부터 원

That is, the constitutional atom of the low resistance

GF Exhibit 1124 - 1816/2704

자도입영역의 하부를 통하여 확산되어 게이트 산화막의 단부까지 침입하고 있으므로, 이런 확산길이보다도 긴 길이로 설정하는 것이 바람직하다.

conductor film is diffused through the lower part of the atom lead-in area from the low resistance wiring domain and it breaks to the end of the gate oxidation film. Therefore it is the be desirable to set up as the length longer than such diffusion length.

본 발명의 제1실시예에 있어서는, 저저항도전체로서 티탄을 사용하고, 원자도입층의 구성원자로서 질소를 사용하였으나, 저저항도전체로서 다른 고융점금속 또는 이것의 실리사이드를 사용해도 되며, 원자도입층의 구성원자로서 산소 또는 실리콘 또는 불활성 원자를 사용해도 게이트절연막의 파괴를 방지할 수 있다.

It was in the first preferred embodiment of the invention and titanium was used as the low resistance conductor and nitrogen was used as the constitutional atom of the atom introduction layer. But the silicide of the dissimilar high melting point metal or this is used as the low resistance conductor and the break down of the gate insulating layer can be prevented even if oxygen, the silicone, or the inactive atom is used as the constitutional atom of the atom introduction layer.

그러나, 저저항도전체막의 구성원자와 전자도입층의 구성원자의 조합에 의해, 게이트절연막의 파괴를 방지하는 메타니즘은 다양하다.

But using the combination of the constitutional atom of the constitutional atom of the low resistance conductor film and electron introduction layer, the mechanism preventing the break down of the gate insulating layer is various.

본 발명의 제1실시예인 티탄과 조합의 경우, 즉, 원자도입층의 구성원자가 비단결정도전체의 구성원자보다 저저항전체의 구성원자와 더욱 쉽게 반응할때, 원자도입층의 구성원자와 저저항도전체의 구성원자는 서로 반응하여 균일한 합금화층을 형성하고, 저저항도전체의 국부적인 확산이 억제됨으로써 게이트절연막의 파괴를 방지한다.

In case of titanium and the combination which is the first preferred embodiment of the invention, when it is more easy in other words, the constitutional atom of the atom introduction layer reacts with the constitutional atom of the low resistance whole than the constitutional atom of the non-single crystal conductor , the constitutional atom of the atom introduction layer and constitutional atom of the low resistance conductor react and the uniform alloy layer is formed and the break down of the gate insulating layer is prevented since the local diffusion of the low resistance conductor is suppressed.

또, 비단결정도전체막과 저저항도전체막사이의 접속저항이 느려, 인가된 전계에 대한 게이트산화막의 내구력은 우수하다.

And the contact resistance between the low resistance conductor film and the non-single crystal conductor film are slow and the applied endurance of the gate oxidation film about the electric field is excellent.

또한, 텅스텐과 산소를 조합하는 경우, 즉, 원자도입층의 구성원자가 저저항도전체막의 구성원자보다 비단결정도전체막의 구성원자와 더욱 쉽게 반응하면, 저저항도전체막의 구성원자의 확산은 원자도입층내에서 저지되고, 저저항도전체의 국부적인 확산은 억제되어 게이트절연막의 전기적 파괴를 방지한다.

Moreover, in other words, the constitutional atom of the atom introduction layer is more easy than the constitutional atom of the low resistance conductor film with the constitutional atom of the non-single crystal conductor film the reaction lower-side , and the diffusion of the constitutional atom of the low resistance conductor film are tungsten and oxygen interrupted in case the combination in the atom introduction layer and the local diffusion of the low resistance conductor is suppressed and the electrical breakdown of the gate insulating layer is prevented.

그러므로 저저항화시 저저항도전체막의 막두께가 증가되면, 게이트절연막의 파괴는 효과적으로 방지될 수 있다.

Therefore, if the film thickness of the low resistance conductor film is increased in the low resistance , the break down of the gate insulating layer can be effectively prevented.

또한, 원자도입층을 형성하기 위하여 도입되는 원자는, 1종류 또는 복수종류이어도 된다.

Moreover, the atom which is introduced in order to form the atom introduction layer is 1 kind or the plural species.

[제2실시예]

[The second preferred embodiment]

본 발명의 제조방법은 게이트전극에 다결정실리콘 및 텅스텐을

The second (a) particularly illustrates as the field

GF Exhibit 1124 - 1817/2704

조합시킨 전계효과형 트랜지스터에 관한 것으로 제2도(a)-제2도(g)를 참조하여 상세히 설명한다.

effect transistor in which the manufacturing method of the invention combines the poly-crystal silicon and tungsten in the gate electrode with reference to the second (g).

(I) 실리콘기판(200)의 능동영역 형성예정부를 제외한 표면상에, 대략 700nm의 산화막(210)을 피일드 산화막으로서 선택적으로 형성하고, 대략 10nm의 게이트산화막(220)을 능동영역 형성예정부의 표면상에 형성하고, 상기 산화막(210)과 (220)상에 대략 200nm의 다결정실리콘막(230)을 퇴적한 후, POCl3를 사용해 인을 확산시켜서 다결정실리콘막(230)을 저저항화하였다(제2도(a)).

(I)Approximately, the oxide film (210) of 700nm was selectively formed on the surface except for the active region formation presumptive region of the silicon substrate (200) as the field oxide film and approximately, the gate oxidation film (220) of 10nm was formed on the surface of the active region formation presumptive region and the phosphorus was diffused by using the POCl 3 approximately, the polysilicon layer (230) of 200nm on the oxide film (210) and (220) after doing the deposition and the polysilicon layer (230) was made lower resistance(second (a)).

(II) 다음에, 다결정실리콘막(230)속으로 산소이온을 가소에너지 40keV로 1#215#10151#215#1018cm-2 주입하고 열처리하여, 다결정실리콘막(230)의 중간 부분에 실리콘산화물의 제1원자도입층(240)을 형성하였다(제2도(b)).

(II)Next, the oxygen ion was injected inside the polysilicon layer (230) to the calcination energy 40keV with 1× 10 15 1× 10 18 cm -2 and it heat-treated and the first circle toll dialing mouth layer (240) of the silicon oxide was formed on the middle part of the polysilicon layer (230)(second (b)).

(III) 다음단계로, 다결정실리콘막(230)의 표면상에 실리콘이온을 가속에너지 2keV로 1#215#1015-1#215#1018cm-2 주입하고 열처리하여, 다결정실리콘막(230)의 표면상에 무정형실리콘으로 구성된 제2원자도입층(290)을 형성하였다(제2도(c)).

(III)The silicon ion was injected on the surface of the polysilicon layer (230) to the acceleration energy 2keV with 1× 10 15 -1× 10 18 cm - 2 and it heat-treated at the following step and the second circle toll dialing mouth layer (290) consisting of the amorphous silicon was formed on the surface of the polysilicon layer (230)(second (c)).

(IV) 물리증착법에 의해서 대략 100nm의 얇은 텅스텐막(250)을 퇴적하였다(제2도(d)).

(IV)Approximately, the thin tungsten film (250) of 100nm was accumulated with the physical vapour deposition(second (d)).

(V) 500-1000℃에서 10초간 신속하게 열어니일링하거나 500-1000℃에서 30분간 전기오븐에서 열처리하면, 텅스텐 실리사이드에 의한 합금화층(260)이 다결정실리콘막(230)의 표면근처에 형성되었다(제2도(e)).

(V)In 500-1000℃, if it rapidly annealed thermally for 10 seconds or it heat-treated in 30 min. electric oven in 500-1000℃ , the alloy layer (260) by the tungsten silicide was formed in the near surface of the polysilicon layer (230)(second (e)).

(VI) 포토마스크공정으로 저항패턴을 형성하여, 게이트전극 형성예정부 및 그의 주변부 이외의 부분을 건식 에칭하여 게이트전극을 형성하였다(제2도(f)).

(VI)The resistance pattern was formed into the photo mask process and the part except the gate electrode forming presumptive region and its peripheral unit dry were etched and the gate electrode was formed(second (f)).

(VII) As 이온을 가속에너지 80keV로 4#215#1015cm-2 주입하여, 소오스영역(270)과 드레인영역(280)을 최종적으로 형성하였다(제2도(g)).

(VII)The As ion was injected to the acceleration energy 80keV with 4× 10 15 cm - 2 and finally the source area (270) and drain region (280) were formed(second (g)).

상기 일련의 공정에서, 소망하는 전계효과형 트랜지스터가 형성되었다.

In said series of process, the desired field effect transistor was formed.

제2원자도입층(290)내의 무정형 실리콘은 다결정실리콘보다 텅스텐과 훨씬 쉽게 반응하여 원자도입층과 그 윗부분에서 대부분의 합금화가 일어났다.

The amorphous silicon within the second circle toll dialing mouth layer (290) more easily reacted with tungsten than the poly-crystal silicon and most of alloyings occurred in the atom introduction layer and top.

그러므로, 두께가 균일한 우수한 합금화층이 얻어졌다.

Therefore, the excellent alloy layer in which the thickness was uniform was obtained.

GF Exhibit 1124 - 1818/2704

텅스텐원자의 이동영역은 제2원자도입층(290)의 근처에서 정지되는 것이 가능하였으나, 약간의 텅스텐 원자가 제2원자도입층(290)을 통하여 침투하였다.

It was possible that the movement area of the tungsten atom was nearby stopped of the second circl e toll dialing mouth layer (290). But the some tungsten atom penetrated through the second circle toll dialing mouth layer (290).

그러나, 제1원자도입층(240)내의 실리콘산화물은 효과적으로 텅스텐을 저지하여 대부분의 합금화는 원자도입층(240)의 윗부분으로 제한되었다.

But the silicon oxide within the first circle toll dialing mouth layer (240) effectively interrupted tungsten and most of alloyings were limited within the top of the ato m introduction layer (240).

합금화층(260)의 두께가 매우 균일하였으므로, 게이트전극의 전기저항이 균일해지고, 저저항도전체의 국부적인 확산도 덜 발생하여, 게이트산화막의 파괴를 방지할 수 있었다.

The thickness of the alloy layer (260) was very uniform. Therefore the electric resistance of the gate e lectrode was uniform and the local diffusion of the low resistance conductor was generated and the break do wn of the gate oxidation film could be prevented.

본 발명에서는, 제1원자도입층을 형성하는 방법으로서, 이온주입방법을 사용하였으나, 다음의 방법을 사용해도 된다.

In the present invention, as the method for forming the first circle toll dialing mouth layer, the ion implantation method was used. But the following method is used.

즉, 게이트산화막상에 제1층으로서 대략 100nm의 다결정실리콘을 퇴적하고, 이 다결정실리콘막의 게이트전극 형성예정부 및 그의 주변부의 표만상에, 수 nm의 얇은 실리콘막을 선택적으로 형성하여, 대략 100nm의 제2의 다결정실리콘층을 퇴적하고, 이와 같이 선택적으로 형성된 수 nm의 실리콘산화막을 제1원자도입층으로 사용해도 된다.

That is, the first layer on the gate oxidation film, approximately, the poly-crystal silicon of 100nm can be used as the first circle toll dialing mouth layer the silico n oxide film of several nm which accumulates and it sel ectively forms the thin silicon film of several nm on the gate electrode forming presumptive region of this polysi licon layer and table all things in the universe of its peri pheral unit and it accumulates approximately, the seco nd polycrystalline silicon layer of 100nm and is selectiv ely formed in this way.

반면, 제2원자도입층(290)은 선택적으로 형성해도 되나, 적어도 게이트전극 형성예정부와 그의 주변부상에 형성되어야 한다.

On the other hand, the second circle toll dialing mouth layer (290) selectively forms. But it has to be formed o n at least gate electrode forming presumptive region an d its peripheral unit.

[제3실시예]

[The third preferred embodiment]

본 발명의 제조방법은 게이트전극에 다결정실리콘 및 텅스텐을 조합시킨 전계효과형 트랜지스터에 관한 것으로 제3도(a)-제3도(g)를 참조하여 이하 상세히 설명한다.

The third (a) hereinafter particularly illustrates as the field effect transistor in which the manufacturing meth od of the invention combines the poly-crystal silicon an d tungsten in the gate electrode with reference to the third (g).

(I) 실리콘기판(300)의 능동영역 형성예정부를 제외한 표면에 대략 700nm의 산화막(310)을 피일드산화막으로서 선택적으로 형성하고, 능동영역 형성예정부의 표면에 대략 10nm의 게이트산화막(320)을 형성한 후, 상기 산화막(310)과 (320)상에 대략 100nm의 다결정 실리콘막(330)을 퇴적시키고, POCl 3를 사용해 인을 확산시켜 다결정실리콘막(330)을 저저항화하였다(제3도(a)).

(I)Approximately, the oxide film (310) of 700nm was selectively formed on the surface except for the active region formation presumptive region of the silicon subst rate (300) as the field oxide film and approximately, the polysilicon layer (330) of 100nm approximately, the gat e oxidation film (320) of 10nm was sedimented on the s urface of the active region formation presumptive regio n after doing the formation on the oxide film (310) and (320) and the phosphorus was diffused by using the PO Cl 3 and the polysilicon layer (330) was made lower resi stance(third (a)).

(II) 다음 단계로 다결정실리콘막(330)에 산소이온을 가속에너지 10keV로 1#215#1015-1#215#1018cm-2 주입하고 열처리하여, 다결정실리콘막(330)의 표면에 실리콘산화물의 제1원자도입층(340)을 형성하였다(제3도(b)).

(II)The oxygen ion was injected into the polysilicon layer (330) to the acceleration energy 10keV with 1× 1 0 15 -1× 10 18 cm - 2 and it heat-treated at the follo wing step and the first circle toll dialing mouth layer (3 40) of the silicon oxide was formed on the surface of t he polysilicon layer (330)(third (b)).

GF Exhibit 1124 - 1819/2704

(III) 물리증착법에 의해서, 대략 100nm의 얇은 텅스텐막(350)을 퇴적하였다(제3도(c)).

(III)Using the physical vapour deposition, the thin tungsten film (350) of 100nm was approximately accum ulated(third (c)).

(IV) 얇은 텅스텐막(350)의 표면상에, 실리콘이온을 가속에너지 20keV로 1#215#1015-1#215#1018cm-2 주입하고, 얇은 텅스텐막(350)내부에 실리콘으로 구성된 제2원자도입층(390)을 형성하였다(제3도(d)).

(IV)The silicon ion was injected on the surface of the thin tungsten film (350) to the acceleration energy 20k eV with 1× 10 15 -1× 10 18 cm - 2 and the second cir cle toll dialing mouth layer (390) consisting of the silico ne was formed inside the thin tungsten film (350)(third (d)).

(V) 500-1000℃에서 10초간 신속하게 열어니일링하거나 500-1000℃에서 30분동안 용광로 어니일링을 통한 열처리에 의해서 얇은 텅스텐막(350)의 내부에 텅스텐 실리사이드의 합금화층(360)을 형성하였다(제3도(e)).

(V)In 500-1000℃, rapidly annealed thermally for 10 seconds or the alloy layer (360) of the tungsten silicide was formed at 500-1000℃ for 30 minutes with the ther mal process through the blast furnace annealing inside the thin tungsten film (350)(third (e)).

(VI) 다음 단계로, 포토마스크공정으로 저항패턴을 형성하고, 게이트전극 형성 예정부와 그의 인접부분 이외의 다른 부분을 건식 에칭하여, 게이트전극을 형성하였다(제3도(f)).

(VI)The resistance pattern was formed into the following step into the photo mask process and the dis similar part except the gate electrode forming presumpt ive region and its adjacent part dry were etched and t he gate electrode was formed(third (f)).

(VII) 마지막으로, 가속에너지 80keV로 As이온을 4#215#1015cm-2 주입하여, 소오스영역(370)과 드레인영역(380)을 형성하였다(제3도(g)).

(VII)Finally, the As ion was injected to the acceleration energy 80keV with 4× 10 15 cm - 2 and the source are a (370) and drain region (380) were formed(third (g)).

이상의 일련의 공정에서, 소망하는 전계효과형 트랜지스터가 형성되었다.

In the series of process described in the above, the desired field effect transistor was formed.

제2원자도입층(390)내의 실리콘은 결정형이 아니고, 다결정실리콘 보다는 텅스텐과 훨씬 쉽게 반응하여 제2원자도입층(390)의 근접부에서 대부분의 합금화가 일어났다.

The silicone within the second circle toll dialing mouth layer (390) was not crystalline form and it more easily r eacted with tungsten than the poly-crystal silicon and most of alloyings occurred in the neighborhood portion of the second circle toll dialing mouth layer (390).

그러므로, 두께가 균일한 우수한 합금화층이 얻어졌다.

Therefore, the excellent alloy layer in which the thickness was uniform was obtained.

텅스텐원자의 이동영역은 제2원자도입층(390)내에 거의 국한되고, 약간의 텅스텐원자는 제2원자도입층(390)에 의해 국한되지 않았으나, 제2원자도입층(390)내에 실리콘산화물은 효과적으로 텅스텐을 방해하여, 대부분의 합금화가 제1원자도입층(340)의 윗부분으로 제한되었다.

The movement area of the tungsten atom was nearly limited within the second circle toll dialing mouth layer (390) and the some tungsten atom was not limited by t he second circle toll dialing mouth layer (390). But the silicon oxide effectively obstructed tungsten within the second circle toll dialing mouth layer (390) and most of alloyings were limited within the top of the first circle t oll dialing mouth layer (340).

합금화층(360)의 두께가 매우 균일하였으므로, 게이트전극의 전기저항이 균일해지고, 또 저저항도전체의 국부적인 확산은 거의 발생되지 않아 게이트산화막의 파괴를 방지할 수 있었다.

The thickness of the alloy layer (360) was very uniform. Therefore the electric resistance of the gate e lectrode was uniform and and, the local diffusion of the low resistance conductor was not nearly generated an d the break down of the gate oxidation film could be pr evented.

[제4실시예]

[The fourth preferred embodiment]

본 발명의 제조방법은 게이트전극에 다결정실리콘 및 텅스텐을 조합시킨 전계효과형 트랜지스터의 제4실시예에 관한 것으로 제4도(a)-제4도(f)를 참조하여 이하 설명한다.

The fourth (a) explains underneath as the fourth preferred embodiment of the field effect transistor in w hich the manufacturing method of the invention combin es the poly-crystal silicon and tungsten in the gate ele ctrode with reference to the fourth (f).

GF Exhibit 1124 - 1820/2704

(I) 실리콘기판(400)의 능동영역 형성예정부를 제외한 표면에 대략 700nm의 산화막(410)을 피일드산화막으로 선택적으로 형성하고, 능동영역 형성예정부의 표면에 대략 10nm의 게이트산화막(420)을 형성하여, 상기 산화막(410)과 (420)상에 대략 200nm의 다결정실리콘막(430)을 퇴적시킨 후, POCl3를 사용해 인을 확산시켜 다결정실리콘막(430)을 저저항화 하였다(제4도(a)).

(I)Approximately, the oxide film (410) of 700nm was selectively formed on the surface except for the active region formation presumptive region of the silicon substrate (400) into the field oxide film and approximately, the gate oxidation film (420) of 10nm was formed on the surface of the active region formation presumptive region and after approximately, the polysilicon layer (430) of 200nm was sedimented on the oxide film (410) and (420) the phosphorus was diffused by using the POCl 3 and the polysilicon layer (430) was made lower resistance(fourth (a)).

(II) 물리증착법에 의해서, 대략 100nm의 얇은 텅스텐막(450)을 퇴적하였다(제4도(b)).

(II)Using the physical vapour deposition, the thin tungsten film (450) of 100nm was approximately accumulated(fourth (b)).

(III) 이런 얇은 텅스텐막(450) 상에 산소이온을 가속에너지 60keV로 1#215#1015~1#215#1018cm-2 주입하여, 얇은 텅스텐막(450)과 다결정실리콘막(430) 사이의 계면부근에 실리콘산화물의 원자도입층(440)을 형성하였다(제4도(c)).

(III)The oxygen ion was injected on the thin tungsten film (450) to the acceleration energy 60keV with 1× 10 15 ~1× 10 18 cm - 2 and the atom introduction layer (440) of the silicon oxide was formed on the interface department radical between the thin polysilicon layer (430) and the tungsten film (450)(fourth (c)).

(IV) 다음에, 500-1000℃에서 10초간 신속하게 열어니일링하여, 다결정실리콘막(430)과 얇은 텅스텐막(450)사이의 계면부근에 텅스텐실리사이드의 합금화층(460)를 형성하였다(제4도(d)).

(IV)Next, in 500-1000℃, rapidly annealed thermally for 10 seconds and the alloy layer (460) of the tungsten silicide was formed on the interface department radical between the thin tungsten film (450) and the polysilicon layer (430)(fourth (d)).

(V) 포토마스크공정에서 저항패턴을 형성하고 게이트전극 형성예정부와 그의 주변부이외의 부분을 건식 에칭하여 게이트전극을 형성하였다(제4도(e)).

(V)In the photo mask process, the resistance pattern was formed and the part except the gate electrode forming presumptive region and its peripheral unit dry were etched and the gate electrode was formed(fourth (e)).

(VI) 마지막으로, 가속에너지 80keV로 As 이온을 4#215#1015cm-2 주입하여, 소오스영역(470)과 드레인영역(480)을 형성하였다(제4도(f)).

(VI)Finally, the As ion was injected to the acceleration energy 80keV with 4× 10 15 cm - 2 and the source area (470) and drain region (480) were formed(fourth (f)).

이상의 일련의 공정에서, 소망하는 전계효과형 트랜지스터가 형성되었다.

In the series of process described in the above, the desired field effect transistor was formed.

원자도입층(440)의 실리콘산화물은 효과적으로 텅스텐을 방해하여, 대부분의 합금화는 원자도입층의 위부분으로 한정되었다.

The silicon oxide of the atom introduction layer (440) effectively obstructed tungsten and most of alloyings were restricted to the top area of the atom introduction layer.

합금화층(460)의 두께가 매우 균일하였으므로, 게이트전극의 전기저항이 균일해지고, 저저항도전체의 국부적인 확산도 덜 발생되어 게이트산화막의 파괴를 방지할 수 있었다.

The thickness of the alloy layer (460) was very uniform. Therefore the electric resistance of the gate electrode was uniform and the local diffusion of the low resistance conductor was less generated and the break down of the gate oxidation film could be prevented.

본 발명의 제4실시예에서는, 이온주입에 의해 원자도입층을 형성한 후에도 저저항도전체막을 그대로 사용하였으나, 원자도입층형성후에 이 저저항도전체층의 일부 또는 전부를 제거해도 되며, 동일 또는 다른 저저항도전체막을 다시 퇴적해도 된다.

In the fourth preferred embodiment of the invention, the low resistance conductor film was like that used even after forming the atom introduction layer with the ion implantation. But a portion or the whole of this low resistance conductive filler layer is removed after the atom introduction layer formation and the identity or the dissimilar low resistance conductor film is again accumulated.

GF Exhibit 1124 - 1821/2704

예를 들면, 이온주입을 위하여 사용된 제1저저항도전체층의 두께를 감축할 수 있으므로, 이온주입의 가속에너지를 저감할 수 있다.

For example, the thickness of the first low resistance conductive filler layer used for the ion implantation can be reduced. Therefore the acceleration energy of the i on implantation can be reduced.

또한, 저저항도전체막을 제거하지 않고, 동일 또는 다른 저저항도전체막을 퇴적하여 복수층의 막을 형성해도 된다.

Moreover, the low resistance conductor film is not removed and the identity or the dissimilar low resistanc e conductor film is accumulated and the film of the mul ti-layer is formed.

예를 들면, 텅스텐막상에 티틴막을 퇴적시키므로서, 보다 좋은 저저항화를 기대할 수 있다.

For example, the titin film is sedimented on the tungsten film. Therefore the low resistance which is be tter can be expected.

본 발명의 제4실시예에서는, 저저항도전체로서 텅스텐을 사용하고, 원자도입층의 구성원자로서 산소를 사용하였으나, 제1실시예에서와 같이, 저저항도전체로서 다른 고융점금속 또는 이것의 실리사이드를 사용해도 되며, 원자도입층의 구성원자로서 질소, 실리콘 또는 불활성원자를 사용하면, 게이트절연막의 파괴를 방지하는 동일효과를 얻을 수 있다.

In the fourth preferred embodiment of the invention, tungsten was used as the low resistance conductor an d oxygen was used as the constitutional atom of the a tom introduction layer. But the silicide of the dissimilar high melting point metal or this is used the first preferr ed embodiment as the low resistance conductor and if nitrogen, and the silicone or the inactive atom are used as the constitutional atom of the atom introduction lay er , the same effect preventing the break down of the gate insulating layer can be obtained.

마찬가지로, 원자도입층의 구성원자가 비단결정도전체의 구성원자보다 저저항도전체의 구성원자와 훨씬 쉽게 반응하는 조합의 경우, 저저항도전체의 구성원자와 원자도입층의 구성원자의 상호반응에 의해 균일한 합금화층이 형성되고, 저저항도전체의 국부적인 확산을 억제하여서 게이트절연막의 파괴를 방지하게 된다.

Similarly, in case of the combination in which it is more easy the constitutional atom of the atom introduction l ayer reacts with the constitutional atom of the low resi stance conductor than the constitutional atom of the n on-single crystal conductor, the uniform alloy layer is f ormed by the mutual reversal of the constitutional ato m of the constitutional atom of the low resistance con ductor and atom introduction layer and the local diffusi on of the low resistance conductor is suppressed and t he break down of the gate insulating layer is prevente d.

또한, 원자도입층의 구성원자가 저저항도전체의 구성원자보다 비단결정도전체의 구성원자와 훨씬 쉽게 반응하는 조합의 경우, 원자도입층내에서의 저저항도전체내의 구성원자의 확산을 억제하고, 저저항도전체의 국부적인 확산을 억제하여서 게이트절연막의 파괴를 또한 방지한다.

Moreover, in case of the combination in which it is more easy the constitutional atom of the atom introduc tion layer reacts with the constitutional atom of the no n-single crystal conductor than the constitutional atom of the low resistance conductor, the diffusion of the co nstitutional atom within the low resistance conductor within the atom introduction layer is held back and the local diffusion of the low resistance conductor is suppr essed and the break down of the gate insulating layer i s moreover prevented.

본 발명의 방법에 따라서, 전계효과형 트랜지스터가 게이트전극물질로서 열처리에 의한 다결정실리콘의 합금화를 이용하여 형성되면, 이때, 합금화층의 두께는 상기 설명한 바와 같이 균일해지고, 저저항도전체의 국부적인 확산에 기인한 게이트절연막의 파괴를 방지할 수 있다.

According to the method of the invention, if the total crab effect type transistor is formed as the gate electr ode material using the alloying of the poly-crystal silico n by the thermal process , as described above, the thi ckness of the alloy layer is then uniform and the break down of the gate insulating layer caused by the local di ffusion of the low resistance conductor can be prevent ed.

본 발명의 바람질한 실시예로서, 원자도입층을 고조사된 이온주입방법에 의해 형성하는 경우, 이온주입시 발생하는 표면상의 전기전하는 저저항도전체막을 통하여 효과적으로 제거될 수 있으므로, 게이트절연막의 전기적파괴도 방지할 수 있다.

As *** embodiment of the invention, the effectively the case , and the electric charge on the surface gene rated in the ion implantation can be removed using the ion implantation method which becomes the atom intro duction layer with the high irradiance through the low r esistance conductor film. Therefore of forming the elec trical breakdown of the gate insulating layer can preve

GF Exhibit 1124 - 1822/2704

nt.

이상, 본 발명의 특정실시예를 기술하였지만, 다른 변형과 변화도 당업자에 의해 실현될 수 있다.

Over, and the certain embodiment of the invention were described. However over can be materialized by deformation and the dissimilar gradient person skilled in the art.

그러므로 본 발명의 정신과 범위를 벗어나지 않는한 이런 모든 변형과 변화를 첨부한 청구범위내에 포함시키고자 한다.

Therefore, it tries to include within the claims which attaches such all deformations and change as long as it does not deviate from spirit and range of the present invention.

Disclaimer

본 문서는 특허 및 과학기술문헌 전용의 첨단 자동번역 시스템을 이용해 생성되었습니다. 따라서 부분적으로 오역의 가능성이 있으며, 본 문서를 자격을 갖춘 전문 번역가에 의한 번역물을 대신하는 것으로 이용되어서는 안 됩니다. 시스템 및 네트워크의 특성때문에 발생한 오역과 부분 누락, 데이터의 불일치등에 대하여 본원은 법적인 책임을 지지 않습니다. 본 문서는 당사의 사전 동의 없이 권한이 없는 일반 대중을 위해 DB 및 시스템에 저장되어 재생, 복사, 배포될 수 없음을 알려드립니다.
(The document produced by using the high-tech machine translation system for the patent and science & technology literature. Therefore, the document can include the mistranslation, and it should not be used as a translation by a professional translator. We hold no legal liability for inconsistency of mistranslation, partial omission, and data generated by feature of system and network. We would like to inform you that the document cannot be regenerated, copied, and distributed by being stored in DB and system for unauthorized general public without our consent.)

GF Exhibit 1124 - 1823/2704

(19) 대한민국특허청(KR)
(12) 등록특허공보(B1)

(45) 공고일자 1999년06월15일
(11) 등록번호 10-0197653
(24) 등록일자 1999년02월25일

(51) 국제분류코드
H01L 21/28 (2006.01)

(21) 출원번호 10-1995-0050467

(22) 출원일자 1995년12월15일
심사청구일자 1999년02월25일

(65) 공개번호 특1997-0052237

(43) 공개일자 1997년07월29일

(72) 발명자
황성보
서울특별시 영등포구 신길동 4656 우성아파트 303-701, 대한민국

(73) 특허권자
김영환
현대전자산업주식회사
경기도 이천시 부발읍 아미리 산 136-1, 대한민국

(74) 대리인
이정훈
이권희

(77) 심사관
권인회

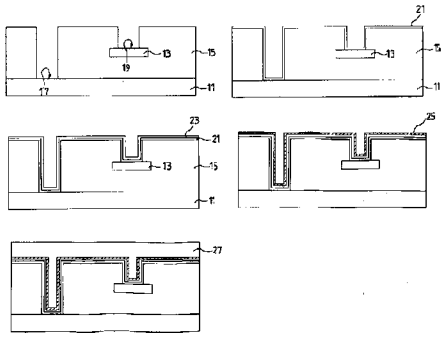
전체 청구항 수 : 총 13 항

(54)반도체 소자의 콘택 형성방법

(57)요 약

본 발명은 반도체소자의 콘택형성방법에 관한 것으로, 반도체기판 상부에 전도체가 형성된 절연층을 형성하고 상기 반도체기판과 전도체를 노출시키는 콘택홀을 형성한 다음, 전체표면상부에 티타늄막, 티타늄질화막, 티타늄산화막 적층구조나 티타늄막, 티타늄산화막, 티타늄질화막 적층구조 또는 이들 중 티타늄막이나 티타늄질화막이 제거된 적층구조를 갖는 콘택접합층을 형성하고 텅스텐으로 콘택플러그를 형성함으로써 티타늄막의 침식이나 절연체 형성을 억제하여 소자의 동작특성을 향상시켜 반도체소자의 특성 및 신뢰성을 향상시키고 그에 따른 반도체소자의 고집적화를 가능하게 하는 기술이다.

대 표 도 - 도 1



This Facsimile Page has been artificially created from KIPO data.

청구의 범위

청구항 1

반도체기판 상부에 전도체가 구비된 절연층을 형성하는 공정과, 상기 반도체기판과 전도체를 노출시키는 제1, 2콘택홀을 각각 형성하는 공정과, 전체표면상부에 티타늄막과 티타늄질화막을 각각 일정두께 형성하는 공정과, 전체표면상부에 티타늄산화막을 일정두께 형성하여 티타늄막, 티타늄질화막, 티타늄산화막 적층구조의 콘택접합층을 형성하는 공정과, 전체표면상부에 텅스텐막을 형성하는 공정을 포함하는 반도체소자의 콘택 형성방법.

청구항 2

제1항에 있어서, 상기 티타늄막은 PVD방법으로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

청구항 3

제1항에 있어서, 상기 티타늄막은 CVD방법으로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

청구항 4

제1항 내지 제3항중 어느 한 항에 있어서, 상기 티타늄막은 100내지 500Å 두께로 형성되는 것을 특징으로 하는 반도체 소자의 콘택 형성방법.

청구항 5

제1항에 있어서, 상기 티타늄질화막은 PVD또는 CVD방법으로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

청구항 6

제5항에 있어서, 상기 티타늄질화막은 300내지 1000Å두께로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

청구항 7

제1항에 있어서, 상기 티타늄산화막은 티타늄 아이소-프로포옥사이드와 산소(O_2)를 반응물로 하여 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

청구항 8

제1항에 있어서, 상기 티타늄산화막은 150내지 250℃의 온도, 0.5내지 2torr의 압력에서 CVD방법으로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

청구항 9

제1항에 있어서, 상기 티타늄산화막은 10내지 30Å 두께로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

청구항 10

제1항에 있어서, 상기 콘택접합층은 티타늄막, 티타늄산화막 적층구조로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

청구항 11

제1항에 있어서, 상기 콘택접합층은 티타늄질화막, 티타늄산화막 적층구조로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

청구항 12

제1항에 있어서, 상기 콘택접합층은 티타늄막, 티타늄산화막, 티타늄질화막 적층구조로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

청구항 13

제1항, 제10항 내지 제12항 중 어느 한 항에 있어서, 상기 콘택접합층은 하나의 챔버내에서 연속적으로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

명세서

[발명의 명칭]

반도체 소자의 콘택 형성방법

[도면의 간단한 설명]

제1a도 내지 제1e도는 본 발명의 제1실시예에 따른 반도체소자의 콘택 형성 공정을 도시한 단면도.

제2a도 내지 제2c도는 본 발명의 제2실시예에 따른 반도체소자의 콘택 형성 공정을 도시한 단면도.

* 도면의 주요부분에 대한 부호의 설명

11, 31 : 반도체 기판　　13, 33 : 전도체

15, 35 : 절연층　　17, 37 : 제1콘택홀

19, 39 : 제2콘택홀　　21 : 티타늄막

23, 45 : 티타늄 질화막　　25, 43 : 티타늄 산화막

27, 47 : 텅스텐막

[발명의 상세한 설명]

본 발명은 반도체소자의 콘택 형성방법에 관한 것으로, 특히 화학기상 증착법에 의한 텅스텐 증착시 티타늄질화막(TiN)/티타늄의 접합층 위에 또는 티타늄질화막(TiN)과 티타늄(Ti)사이에 TiO_2(티타늄 산화물)박막을 형성 또는 증착하여 CVD(화학기상증착법) 텅스텐의 반응물인 텅스텐 헥사플루오라이드(WF_6)의 티타늄(Ti)침식에 의한 절연체 티타늄플루오라이트(TiF_3)형성을 억제시켜 신뢰성 있는 콘택을 형성하는 기술에 관한 것이다.

일반적으로, CVD텅스텐막의 접합층으로 티타늄(Ti)위에 티타늄질화막(TiN)를 적층한 구조를 사용하는데, 이 접합층 형성방법으로 스퍼터링을 사용하는 경우 박막의 밀도를 높이고 박막표면에 '산소(O)'가 거의 없는 상태로 만들어도 CVD텅스텐의 반응물인 WF_6가 티타늄질화막을 통과하여 티타늄과 반응하여 티타늄플루오라이트를 형성시키면서 콘택의 신뢰성을 떨어뜨린다.

그로 인하여, 반도체소자의 특성 및 신뢰성을 저하시키고 그에 따른 반도체소자의 고집적화를 어렵게 하는 문제점이 있다.

따라서, 본 발명은 티타늄질화막/티타늄의 접합층 위에 또는 티타늄 질화막과 티타늄 사이에 티타늄 산화물(TiO_2)을 얇게 증착하거나 형성시켜 CVD텅스텐 반응물인 WF_6과 티타늄의 반응을 억제시켜서 절연체인 TiF_3형성을 억제하고 신뢰성 있는 콘택을 형성함으로써 반도체소자의 특성 및 신뢰성을 향상시키고 그에 따른 반도체소자의 고집적화를 가능하게 하는 반도체소자의 콘택 형성방법을 제공하는데 그 목적이 있다.

이상의 목적을 달성하기 위하여 본 발명에 따른 반도체소자의 콘택 형성방법의 특징은, 반도체기판 상부에 전도체가 구비된 절연층을 형성하는 공정과, 상기 반도체기판과 전도체를 노출시키는 제1,2콘택홀을 각각 형성하는 공정과, 전체표면상부에 티타늄막과 티타늄질화막을 각각 일정두께 형성하는 공정

과, 전체표면상부에 티타늄산화막을 일정두께 형성하여 티타늄막, 티타늄질화막, 티타늄산화막 적층구조의 콘택접합층을 형성하는 공정과, 전체표면상부에 텅스텐막을 형성하는 공정을 포함하는데 있다.

여기서, 상기 티타늄막은 물리증착방법(PVD : Physical Vapor Deposition, 이하에서 PVD라 함)방법으로 형성되는 것과, 상기 티타늄막은 화학기상증착(CVD : Chemical Vapor Deposition, 이하에서 CVD라 함)방법으로 형성되는 것과, 상기 티타늄막은 100내지 500Å 두께로 형성되는 것과, 상기 티타늄질화막은 PVD 또는 CVD방법으로 형성되는 것과, 상기 티타늄질화막은 300내지 1000Å 두께로 형성되는 것과, 상기 티타늄산화막은 티타늄 아이소-프로포옥사이드와 산소(O_2)를 반응물로 하여 형성되는 것과, 상기 티타늄산화막은 150내지 250℃의 온도, 0.5 내지 2torr의 압력에서 CVD방법으로 형성되는 것과, 상기 티타늄산화막은 10내지 30Å 두께로 형성되는 것과, 상기 콘택접합층은 티타늄막, 티타늄산화막 적층구조로 형성되는 것과, 상기콘택접합층은 티타늄질화막, 티타늄산화막 적층구조로 형성되는 것과, 상기콘택접합층은 티타늄막, 티타늄산화막, 티타늄질화막 적층구조로 형성되는 것과, 상기 콘택접합층은 하나의 챔버내에서 연속적으로 형성되는 것이다.

본 발명의 원리는, 결합 에너지(binding energy)로 설명할 수 있는데 두 원자의 분자구조를 기본으로 실온에서의 결합에너지가 Ti-Ti 경우 141.4±21 $KJmol^{-1}$, F-Ti 경우 569.±33 $KJmol^{-1}$, O-Ti 경우 672.4±9.2 $KJmol^{-1}$이므로, 이를 비교하면 Ti-Ti F-Ti O-Ti과 같아 Ti-Ti는 플루오라이트(Ti-F_3)를 형성할 수 있지만 O-Ti 구조는 쉽게 플루오라이트를 형성할 수 없어 O-Ti 구조를 갖는 티타늄산화막으로 Ti-F_3 형성을 억제하는 것이다.

이하, 첨부된 도면을 참고로 하여 본 발명을 상세히 설명하기로 한다.

제1a도 내지 제1e도는 본 발명의 제1실시예에 따른 반도체소자의 콘택 형성공정을 도시한 단면도이다.

제1a도를 참조하면, 반도체기판(11)상부에 전도체(13)가 형성된 절연층(15)을 형성한다. 그리고, 콘택마스크(도시안됨)를 이용한 식각공정으로 상기 반도체기판(11)과 전도체(13)를 노출시키는 제1콘택홀(17)과 제2콘택홀(19)을 각각 형성한다.

제1b도를 참조하면, 전체표면상부에 PVD또는 CVD방법으로 티타늄막(21)을 100내지 500Å두께 형성한다.

제1c도를 참조하면, 전체표면상부에 PVD또는 CVD방법으로 티타늄질화막(23)을 300내지 1000Å 두께 형성한다.

제1d도를 참조하면, 전체표면상부에 티타늄(IV) 아이소-프로포옥사이드{$Ti[OCH(CH_3)_2]_4$}와 산소(O_2)를 반응물로 150내지 250℃온도, 0.5내지 2torr 압력의 증착조건에서 CVD방법에 의한 티바늄산화막(25)을 10내지 30Å두께 형성한다.

제1e도를 참조하면, 전체표면상부에 WF_6와 H_2를 반응물로 하여 300내지 500℃온도, 10내지 100torr압력의 증착조건에서 텅스텐막(27)을 형성함으로써 콘택을 형성한다.

제2a도 내지 제2c도는 본 발명의 제2실시예에 따른 반도체소자의 콘택형성공정을 도시한 단면도이다.

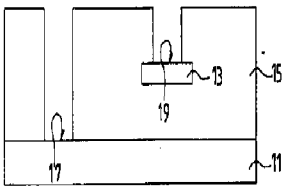
제2a도를 참조하면, 반도체기판(11)상부에 전도체(13)가 형성된 절연층(15)을 형성한다. 그리고, 콘택마스크(도시안됨)를 이용한 식각공정으로 상기 반도체기판(11)과 전도체(13)를 노출시키는 제1콘택홀(17)과 제2콘택홀(19)을 각각 형성한다. 그리고, 전체표면상부에 PVD또는 CVD방법으로 티타늄막(21)을 100내지 500Å두께 형성한다. 그리고, 전체표면상부에 티타늄(IV) 아이소-프로옥사이드

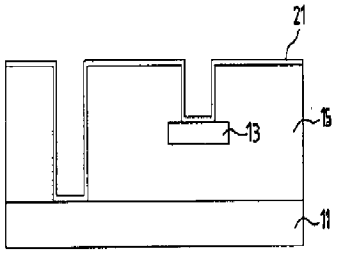
{Ti[OCH(CH3)2]4}와 산소를 반응물로 150내지 250℃온도, 0.5내지 2torr압력의 증착조건에서 CVD방법에 따라 티바늄산화막(43)을 10내지 30Å두께 형성한다.

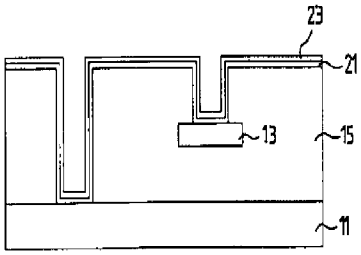
제2b도를 참조하면, 전체표면상부에 PVD 또는 CVD방법으로 티타늄질화막(45)을 300~1000Å 두께 형성한다.

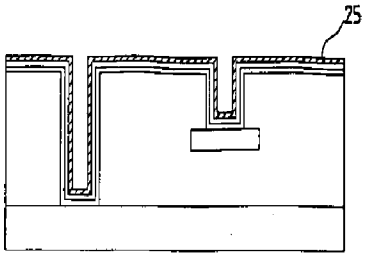
제2c도를 참조하면, 전체표면상부에 WF_6와 H_2를 반응물로 하여 300내지 500℃온도, 10내지 100torr압력의 증착조건에서 텅스텐막(47)을 형성함으로써 콘택을 형성한다.

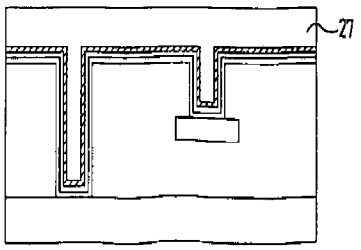
이상에서 설명한 바와 같이 본발명에 따른 반도체소자의 콘택 형성방법은, 콘택공정시 WF_6에 의한 티타늄막의 침식을 억제하고 절연체의 발생을 억제하여 콘택특성을 향상시킴으로써 반도체소자의 특성 및 신뢰성을 향상시키고 그에 따른 반도체소자의 고집적화를 가능하게 하는 잇점이 있다.

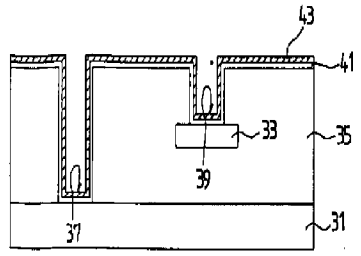

13
15
19
17
11

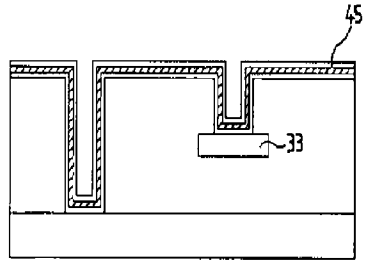

21
13
15
11

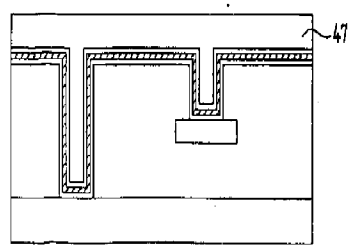

23
21
13
15
11


25


27


43
41
33
35
39
37
31


45
33


47

Examined Patent Publication(B1)

Bibliographic Data

Int.Cl.	H01L 21/768
Published Date	19990615
Registration No.	1001976530000
Registration Date	19990225
Application No.	1019950050467
Application Date	19951215
Unexamined Publication No.	1019970052237
Unexamined Publication Date	19970729
Requested Date of Examination	19960527
Agent.	LEE, Jung Hoon | HANYANG PATENT FIRM
Inventor	Hwang,Seong-Bo
Applicant	SK hynix Inc.
Rightholder	Hyundai Electronics industry CO., LTD

발명의 명칭

반도체 소자의 콘택 형성방법

Title of Invention

Manufacturing method of contact in semiconductor device

요약

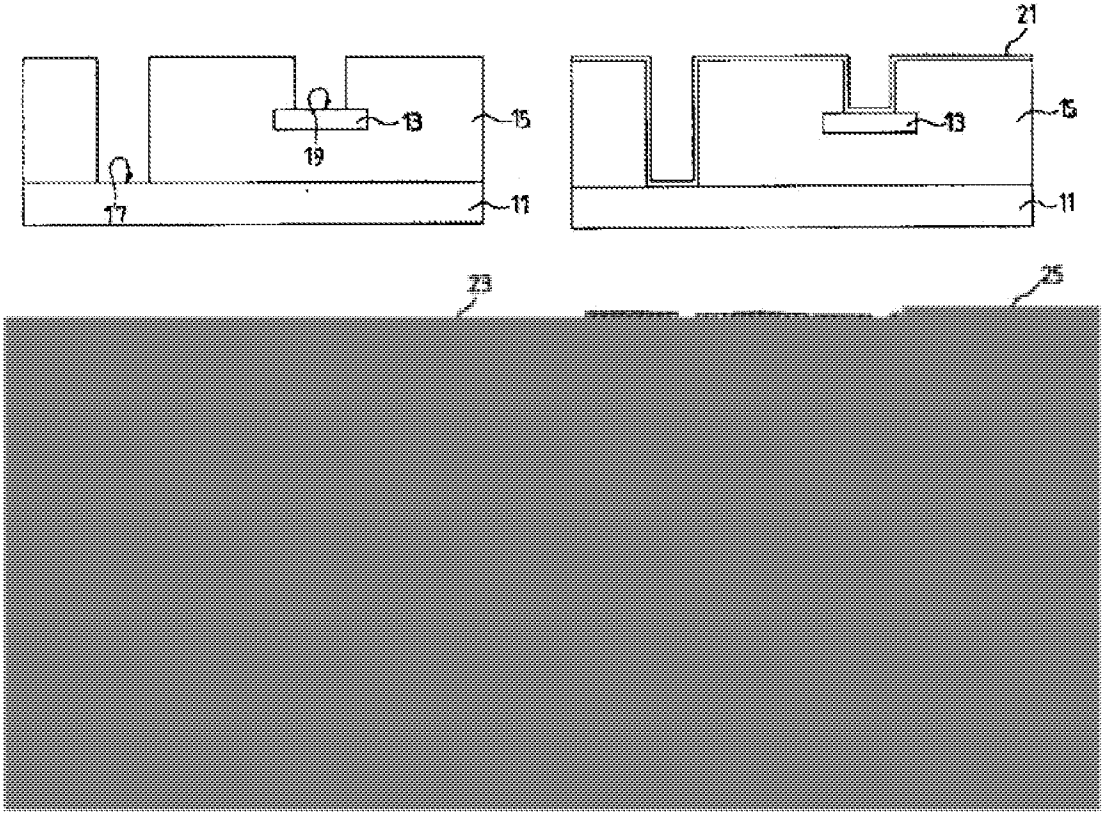
본 발명은 반도체소자의 콘택형성방법에 관한 것으로, 반도체 기판 상부에 전도체가 형성된 절연층을 형성하고 상기 반도체 기판과 전도체를 노출시키는 콘택홀을 형성한 다음, 전체표면 상부에 티타늄막, 티타늄질화막, 티타늄산화막 척층구조나 티타늄막, 티타늄산화막, 티타늄질화막 적층구조 또는 이들 중 티타늄막이나 티타늄질화막이 제거된 적층구조를 갖는 콘택접합층을 형성하고 텅스텐으로 콘택플러그를 형성함으로써 티타늄막의 침식이나 절연체 형성을 억제하여 소자의 동작특성을 향상시켜 반도체소자의 특성 및 신뢰성을 향상시키고 그에 따른 반도체소자의 고집적화를 가능하게 하는 기술이다.

Abstract

According to the invention, the insulating layer in which the conductive material is formed is formed in the semiconductor substrate upper as the contact forming method of a semiconductor device. And after the contact hole exposing the semiconductor substrate and conductive material is formed it is the technology suppressing the erosion or the insulator formation of the titanium film by forming the borderless junction layer having the titanium film, the TiN film, the titanium oxide film laminate structure or the titanium film, the titanium oxide film, and the structure of layer built titanium nitride or the laminating structure in which the titanium film or the TiN film is removed among these

at the upper part of the whole surface and formin g the contact plug into tungsten and improves the performance characteristic of the device and prop erty and reliability of the semiconductor device an d makes the high integration of the semiconducto r device according to the same possible.

대표도면(Representative drawing)



청구의 범위

청구 1항:

반도체기판 상부에 전도체가 구비된 절연층을 형성하는 공정과 , 상기 반도체기판과 전도체를 노출시키는 제1, 2콘택홀을 각 각 형성하는 공정과, 전체표면상부에 티타늄막과 티타늄질화막 을 각각 일정두께 형성하는 공정과, 전체표면상부에 티타늄산 화막을 일정두께 형성하여 티타늄막, 티타늄질화막, 티타늄산 화막 적층구조의 콘택접합층을 형성하는 공정과, 전체표면상부 에 텅스텐막을 형성하는 공정을 포함하는 반도체소자의 콘택 형성방법.

Scope of Claims

Claim 1:

The contact forming method of a semiconductor d evice which comprises the process of forming the insulating layer in which the conductive material i s equipped in the semiconductor substrate upper, the semiconductor substrate, and the process, of forming first and second contact hole exposing th e conductive material and the process, of respecti vely forming certain thickness the titanium film a nd TiN film at the upper part of the whole surface and the process, of forming the titanium film, the TiN film, and the borderless junction layer of the t itanium oxide film laminating structure the titaniu m oxide film is certain thickness formed at the up per part of the whole surface and the process of f orming the tungsten film at the upper part of the whole surface.

청구 2항:

제1항에 있어서, 상기 티타늄막은 PVD방법으로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 2:

As for claim 1, the contact forming method of a semiconductor device in which the titanium film is formed with the PVD method.

청구 3항:

제1항에 있어서, 상기 티타늄막은 CVD방법으로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 3:

As for claim 1, the contact forming method of a semiconductor device in which the titanium film is formed with the CVD method.

청구 4항:

제1항 내지 제3항중 어느 한 항에 있어서, 상기 티타늄막은 100내지 500Å 두께로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 4:

As for any one of claim 1 through 3, the contact forming method of a semiconductor device in which the titanium film is formed with 100 through 500Å thickness.

청구 5항:

제1항에 있어서, 상기 티타늄질화막은 PVD또는 CVD방법으로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 5:

As for claim 1, the contact forming method of a semiconductor device in which the TiN film is formed with PVD or the CVD method.

청구 6항:

제5항에 있어서, 상기 티타늄질화막은 300내지 1000Å두께로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 6:

As for claim 5, the contact forming method of a semiconductor device in which the TiN film is formed with 300 through 1000Å thickness.

청구 7항:

제1항에 있어서, 상기 티타늄산화막은 티타늄 아이소-프로포옥사이드와 산소(O2)를 반응물로 하여 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 7:

As for claim 1, the contact forming method of a semiconductor device in which the titanium oxide film decides on the titanium iso - pro cannonade oxide and oxygen (O(SB)2(/SB)) to the reactant and which is formed.

청구 8항:

제1항에 있어서, 상기 티타늄산화막은 150내지 250℃의 온도, 0.5내지 2torr의 압력에서 CVD방법으로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 8:

As for claim 1, the contact forming method of a semiconductor device in which the titanium oxide film is formed at the temperature of 150 through 250℃, and the pressure of 0.5 through 2torr into the CVD method.

청구 9항:

제1항에 있어서, 상기 티타늄산화막은 10내지 30Å 두께로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 9:

As for claim 1, the contact forming method of a semiconductor device in which the titanium oxide film is formed with 10 through 30Å thickness.

청구 10항:

제1항에 있어서, 상기 콘택접합층은 티타늄막, 티타늄산화막 적층구조로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 10:

As for claim 1, the contact forming method of a semiconductor device in which the borderless junction layer is formed with the titanium film, and the titanium oxide film laminating structure.

청구 11항:

제1항에 있어서, 상기 콘택접합층은 티타늄질화막, 티타늄산화막 적층구조로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 11:

As for claim 1, the contact forming method of a semiconductor device in which the borderless junction layer is formed with the TiN film, and the titanium oxide film laminating structure.

청구 12항:

제1항에 있어서, 상기 콘택접합층은 티타늄막, 티타늄산화막, 티타늄질화막 적층구조로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 12:

As for claim 1, the contact forming method of a semiconductor device in which the borderless junction layer is formed with the titanium film, the titanium oxide film, and the structure of layer built titanium nitride.

청구 13항:

제1항, 제10항 내지 제12항 중 어느 한 항에 있어서, 상기 콘택접합층은 하나의 챔버내에서 연속적으로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 13:

Claim 1, and the contact forming method of a semiconductor device in which as for any one of claim 10 through 12, the borderless junction layer is consecutively formed in one chamber.

상세설명

[발명의 명칭]

반도체 소자의 콘택 형성방법

[도면의 간단한 설명]

제1a도 내지 제1e도는 본 발명의 제1실시예에 따른 반도체소자의 콘택 형성 공정을 도시한 단면도.

제2a도 내지 제2c도는 본 발명의 제2실시예에 따른 반도체소자의 콘택 형성 공정을 도시한 단면도.

* 도면의 주요부분에 대한 부호의 설명

11, 31 : 반도체 기관 13, 33 : 전도체

15, 35 : 절연층 17, 37 : 제1콘택홀

19, 39 : 제2콘택홀 21 : 티타늄막

23, 45 : 티타늄 질화막 25, 43 : 티타늄 산화막

27, 47 : 텅스텐막

[발명의 상세한 설명]

본 발명은 반도체소자의 콘택 형성방법에 관한 것으로, 특히 화학기상 증착법에 의한 텅스텐 증착시 티타늄질화막(TiN)/티타늄의 접합층 위에 또는 티타늄질화막(TiN)과 티타늄(Ti)사이

Detailed Description

[Title of invention]

Contact forming method of a semiconductor device.

[Brief description of drawings]

To Figure 1a. And figure 1e is a cross-sectional view showing the contact forming process of the semiconductor device according to the first preferred embodiment of the invention.

To Figure 2a. And figure 2c is a cross-sectional view showing the contact forming process of the semiconductor device according to the second preferred embodiment of the present invention.

* The description of reference numerals showing the main elements in drawings.

11, 31: the semiconductor engine 13, 33: conductive material.

15, 35: insulating layer 17, 37: first contact hole.

19, 39: second contact hole 21: titanium film.

23, 45: tiN film 25, 43: titanium oxide film.

27, 47: tungsten film.

[Detailed description of the invention]

The invention relates to the contact forming method of a semiconductor device, and particularly, to the junction layer of the TiN film (TiN) / titanium i

에 TiO2(티타늄 산화물)박막을 형성 또는 증착하여 CVD(화학기상증착법) 텅스텐의 반응물인 텅스텐 헥사플루오라이드(WF6)의 티타늄(Ti)침식에 의한 절연체 티타늄플루오라이트(TiF3)형성을 억제시켜 신뢰성 있는 콘택을 형성하는 기술에 관한 것이다.

n the tungsten deposition by the chemistry gaseity deposition method, or, the TiN film (TiN) and the technology forming the TiO 2 (titanium oxide) thin film between the titanium (Ti) or deposits and suppresses the insulator titanium fluorite (TiF(SB)3(/SB)) formation by the titanium (Ti) erosion of the tungsten hexafluoride (WF(SB)6(/SB)) which is the reactant of the CVD (chemistry gaseity deposition method) tungsten and forms the contact having reliability.

일반적으로, CVD텅스텐막의 접합층으로 티타늄(Ti)위에 티타늄질화막(TiN)를 적층한 구조를 사용하는데, 이 접합층 형성 방법으로 스퍼터링을 사용하는 경우 박막의 밀도를 높이고 박막표면에 #39#산소(O)#39#가 거의 없는 상태로 만들어도 CVD텅스텐의 반응물인 WF6가 티타늄질화막을 통과하여 티타늄과 반응하여 티타늄플루오라이트를 형성시키면서 콘택의 신뢰성을 떨어뜨린다.

Generally, the structure of laminating the TiN film (TiN) in the junction layer of the CVD tungsten film on the titanium (Ti) is used. Even if while the density of the thin film is enhanced in case the use and the sputtering is made into the state where there is nearly no ' oxygen (O) ' with this manufacturing method of junction in the thin film surface the WF 6 which is the reactant of the CVD tungsten passes the TiN film and the thin film reacts to titanium and the titanium fluorite is formed the reliability of the contact is dropped down.

그로 인하여, 반도체소자의 특성 및 신뢰성을 저하시키고 그에 따른 반도체소자의 고집적화를 어렵게 하는 문제점이 있다.

There is a problem that property and reliability of the semiconductor device are lowered due to that and the high integration of the semiconductor device according to the same is made difficult.

따라서, 본 발명은 티타늄질화막/티타늄의 접합층 위에 또는 티타늄 질화막과 티타늄 사이에 티타늄 산화물(TiO2)을 얇게 증착하거나 형성시켜 CVD텅스텐 반응물인 WF6과 티타늄의 반응을 억제시켜서 절연체인 TiF3형성을 억제하고 신뢰성 있는 콘택을 형성함으로써 반도체소자의 특성 및 신뢰성을 향상시키고 그에 따른 반도체소자의 고집적화를 가능하게 하는 반도체소자의 콘택 형성방법을 제공하는데 그 목적이 있다.

Therefore, an object of the present invention are to provide the junction layer of the TiN film / titanium, or, the TiN film and the contact forming method of a semiconductor device which improves property and reliability of the semiconductor device by the thinly depositing the titanium oxide (TiO(SB)2(/SB)) between titanium or forming and suppressing the WF 6 which is the CVD tungsten reactant and the TiF 3 formation suppressing the reaction of titanium and is the insulator and forming the contact having reliability and makes the high integration of the semiconductor device according to the same possible.

이상의 목적을 달성하기 위하여 본 발명에 따른 반도체소자의 콘택 형성방법의 특징은, 반도체기판 상부에 전도체가 구비된 절연층을 형성하는 공정과, 상기 반도체기판과 전도체를 노출시키는 제1,2콘택홀을 각각 형성하는 공정과, 전체표면상부에 티타늄막과 티타늄질화막을 각각 일정두께 형성하는 공정과, 전체표면상부에 티타늄산화막을 일정두께 형성하여 티타늄막, 티타늄질화막, 티타늄산화막 적층구조의 콘택접합층을 형성하는 공정과, 전체표면상부에 텅스텐막을 형성하는 공정을 포함하는데 있다.

To achieve the above goals, the characteristic of the contact forming method of a semiconductor device according to the present invention comprises the process, of forming the insulating layer in which the conductive material is equipped in the semiconductor substrate upper and semiconductor substrate and the process, of forming first and second contact hole exposing the conductive material and the process, of respectively forming certain thickness the titanium film and TiN film at the upper part of the whole surface and the process, of forming the titanium film, the TiN film, and the borderless junction layer of the titanium oxide film laminating structure the titanium oxide film is certain thickness formed at the upper part of the whole surface and the process of forming the tungsten fi

lm at the upper part of the whole surface.

여기서, 상기 티타늄막은 물리증착방법(PVD : Physical Vapor Deposition, 이하에서 PVD라 함)방법으로 형성되는 것과, 상기 티타늄막은 화학기상증착(CVD : Chemical Vapor Deposition, 이하에서 CVD라 함)방법으로 형성되는 것과, 상기 티타늄막은 100내지 500Å 두께로 형성되는 것과, 상기 티타늄질화막은 PVD 또는 CVD방법으로 형성되는 것과, 상기 티타늄질화막은 300내지 1000Å 두께로 형성되는 것과, 상기 티타늄산화막은 티타늄 아이소-프로포옥사이드와 산소(O2)를 반응물로 하여 형성되는 것과, 상기 티타늄산화막은 150내지 250℃의 온도, 0.5 내지 2torr의 압력에서 CVD방법으로 형성되는 것과, 상기 티타늄산화막은 10내지 30Å 두께로 형성되는 것과, 상기 콘택접합층은 티타늄막, 티타늄산화막 적층구조로 형성되는 것과, 상기콘택접합층은 티타늄질화막, 티타늄산화막 적층구조로 형성되는 것과, 상기콘택접합층은 티타늄막, 티타늄산화막, 티타늄질화막 적층구조로 형성되는 것과, 상기 콘택접합층은 하나의 챔버내에서 연속적으로 형성되는 것이다.

Here, the borderless junction layer is consecutively formed in one chamber the titanium film is formed with the physical vapor deposition (hereinafter the PVD : Physical Vapor Deposition says to be PVD) method the reactant is formed.

본 발명의 원리는, 결합 에너지(binding energy)로 설명할 수 있는데 두 원자의 분자구조를 기본으로 실온에서의 결합에너지가 Ti-Ti 경우 141.4#177#21 KJmol-1, F-Ti 경우 569.#177#33 KJmol-1, O-Ti 경우 672.4#177#9.2 KJmol-1이므로, 이를 비교하면 Ti-Ti F-Ti O-Ti과 같아 Ti-Ti는 플루오라이트(Ti-F3)를 형성할 수 있지만 O-Ti 구조는 쉽게 플루오라이트를 형성할 수 없어 O-Ti 구조를 갖는 티타늄산화막으로 Ti-F3 형성을 억제하는 것이다.

The principles of the invention can illustrate as the binding energy but the binding energy at the room temperature is the molecular structure of two atoms the Ti-Ti case 141.4±21 KJmol - 1 , the F-Ti case 569.±33 KJmol - 1 , and the O-Ti case 672.4±9.2 KJmol - 1 to the basis. Therefore it suppresses the Ti- F 3 formation with the titanium oxide film is the same as that of the Ti-Ti F-Ti O-Ti and in which the Ti-Ti can form the fluorite (Ti-F(SB)3(/SB)) but if it compares this the O-Ti structure is easy it cannot form the fluorite and having the O-Ti structure.

이하, 첨부된 도면을 참고로 하여 본 발명을 상세히 설명하기로 한다.

The attached invention decides to be hereinafter particularly illustrated.

제1a도 내지 제1e도는 본 발명의 제1실시예에 따른 반도체소자의 콘택 형성공정을 도시한 단면도이다.

To Figure 1a. And figure 1e is a cross-sectional view showing the contact forming process of the semiconductor device according to the first preferred embodiment of the invention.

제1a도를 참조하면, 반도체기판(11)상부에 전도체(13)가 형성된 절연층(15)을 형성한다. 그리고, 콘택마스크(도시안됨)를 이용한 식각공정으로 상기 반도체기판(11)과 전도체(13)를 노출시키는 제1콘택홀(17)과 제2콘택홀(19)을 각각 형성한다.

Referring to figure 1a, the insulating layer (15) in which the conductive material (13) is formed at the upper part of the semiconductor substrate (11) is formed. And the first contact hole (17) and the second contact hole (19) exposing the semiconductor substrate (11) and conductive material (13) are formed into the etching process using the contact mask (is not shown).

제1b도를 참조하면, 전체표면상부에 PVD또는 CVD방법으로 티타늄막(21)을 100내지 500Å두께 형성한다.

Referring to figure 1b, the titanium film (21) is formed into PVD or the CVD method at the upper part of the whole surface with 100 through 500Å thickness.

제1c도를 참조하면, 전체표면상부에 PVD또는 CVD방법으로 티타늄질화막(23)을 300내지 1000Å두께 형성한다.

Referring to figure 1c, the TiN film (23) is formed into PVD or the CVD method at the upper part of the whole surface with 300 through 1000Å thickne

ss.

제1d도를 참조하면, 전체표면상부에 티타늄(IV) 아이소-프로포옥사이드{Ti[OCH(CH3)2]4}와 산소(O2)를 반응물로 150내지 250℃온도, 0.5내지 2torr 압력의 증착조건에서 CVD방법에 의한 티바늄산화막(25)을 10내지 30Å두께 형성한다.

Referring to figure 1d, in the reactant 150 through 250℃ temperature the titanium (IV) iso - pro cannonade oxide [Ti(OCH(CH(SB)3(/SB))(SB)2(/SB))(SB)4(/SB)] at the upper part of the whole surface and oxygen (O(SB)2(/SB)), and the deposition condition of 0.5 through 2torr pressure, *** oxide film (25) by the CVD method is formed with 10 through 30Å thickness.

제1e도를 참조하면, 전체표면상부에 WF6와 H2를 반응물로 하여 300내지 500℃온도, 10내지 100torr압력의 증착조건에서 텅스텐막(27)을 형성함으로써 콘택을 형성한다.

Referring to figure 1e, by having the WF 6 and H 2 as the reactant at the upper part of the whole surface and forming the tungsten film (27) at 300 through 500℃ temperature, and the deposition condition of 10 through 100torr pressure the contact is formed.

제2a도 내지 제2c도는 본 발명의 제2실시예에 따른 반도체소자의 콘택형성공정을 도시한 단면도이다.

To Figure 2a. And figure 2c is a cross-sectional view showing the contact of a semiconductor device formation process according to the second preferred embodiment of the present invention.

제2a도를 참조하면, 반도체기판(11)상부에 전도체(13)가 형성된 절연층(15)을 형성한다. 그리고, 콘택마스크(도시안됨)를 이용한 식각공정으로 상기 반도체기판(11)과 전도체(13)를 노출시키는 제1콘택홀(17)과 제2콘택홀(19)을 각각 형성한다. 그리고, 전체표면상부에 PVD또는 CVD방법으로 티타늄막(21)을 100내지 500Å두께 형성한다. 그리고, 전체표면상부에 티타늄(IV) 아이소-프로옥사이드{Ti[OCH(CH3)2]4}와 산소를 반응물로 150내지 250℃온도, 0.5내지 2torr압력의 증착조건에서 CVD방법에 따라 티바늄산화막(43)을 10내지 30Å두께 형성한다.

Referring to figure 2a, the insulating layer (15) in which the conductive material (13) is formed at the upper part of the semiconductor substrate (11) is formed. And the first contact hole (17) and the second contact hole (19) exposing the semiconductor substrate (11) and conductive material (13) are formed into the etching process using the contact mask (is not shown). And the titanium film (21) is formed into PVD or the CVD method at the upper part of the whole surface with 100 through 500Å thickness. And in the reactant 150 through 250℃ temperature the titanium (IV) iso - pro oxide [Ti(OCH(CH(SB)3(/SB))(SB)2(/SB))(SB)4(/SB)] at the upper part of the whole surface and oxygen, and the deposition condition of 0.5 through 2torr pressure, *** oxide film (43) is formed according to the CVD method with 10 through 30Å thickness.

제2b도를 참조하면, 전체표면상부에 PVD 또는 CVD방법으로 티타늄질화막(45)을 300~1000Å 두께 형성한다.

Referring to figure 2b, the TiN film (45) is formed into PVD or the CVD method at the upper part of the whole surface with 300~1000Å thickness.

제2c도를 참조하면, 전체표면상부에 WF6와 H2를 반응물로 하여 300내지 500℃온도, 10내지 100torr압력의 증착조건에서 텅스텐막(47)을 형성함으로써 콘택을 형성한다.

Referring to figure 2c, by having the WF 6 and H 2 as the reactant at the upper part of the whole surface and forming the tungsten film (47) at 300 through 500℃ temperature, and the deposition condition of 10 through 100torr pressure the contact is formed.

이상에서 설명한 바와 같이 본발명에 따른 반도체소자의 콘택형성방법은, 콘택공정시 WF6에 의한 티타늄막의 침식을 억제하고 절연체의 발생을 억제하여 콘택특성을 향상시킴으로써 반도체소자의 특성 및 신뢰성을 향상시키고 그에 따른 반도체소자의 고집적화를 가능하게 하는 잇점이 있다.

As illustrated in the above, the contact forming method of a semiconductor device according to the present invention has the advantage that property and reliability of the semiconductor device are improved by the erosion of the titanium film by the WF 6 being suppressed in the contact process a

nd the generation of the insulator being suppress ed and improving the contact quality and it makes the high integration of the semiconductor device according to the same possible.

Disclaimer

본 문서는 특허 및 과학기술문헌 전용의 첨단 자동번역 시스템을 이용해 생성되었습니다. 따라서 부분적으로 오역의 가능성이 있으며, 본 문서를 자격을 갖춘 전문 번역가에 의한 번역물을 대신하는 것으로 이용되어서는 안 됩니다. 시스템 및 네트워크의 특성때문에 발생한 오역과 부분 누락, 데이터의 불일치등에 대하여 본원은 법적인 책임을 지지 않습니다. 본 문서는 당사의 사전 동의 없이 권한이 없는 일반 대중을 위해 DB 및 시스템에 저장되어 재생, 복사, 배포될 수 없음을 알려드립니다.

(The document produced by using the high-tech machine translation system for t he patent and science & technology literature. Therefore, the document can inclu de the mistranslation, and it should not be used as a translation by a professional translator. We hold no legal liability for inconsistency of mistranslation, partial om ission, and data generated by feature of system and network. We would like to in form you that the document cannot be regenerated, copied, and distributed by b eing stored in DB and system for unauthorized general public without our consen t.)

(19) 대한민국특허청(KR)
(12) 등록특허공보(B1)

(51) 。Int. Cl. [6]
H01L 21/28

(45) 공고일자 2001년08월07일
(11) 등록번호 10-0290467
(24) 등록일자 2001년03월02일

(21) 출원번호 10-1997-0081150
(22) 출원일자 1997년12월31일

(65) 공개번호 특1999-0060904
(43) 공개일자 1999년07월26일

(73) 특허권자 현대전자산업주식회사
박종섭
경기 이천시 부발읍 아미리 산136-1

(72) 발명자 홍상기
경기도 성남시 분당구 구미동 엘지아파트 210동 1504호
김우현
서울특별시 용산구 용산동3가 1-70

(74) 대리인 신영무
최승민

심사관 : 김동원

(54) 반도체소자의확산방지막형성방법

요약

본 발명은 반도체 소자의 확산 방지막 형성 방법에 관한 것으로, 실리콘 기판 상부에 형성된 층간 절연막의 소정 영역을 식각하여 상기 실리콘 기판의 소정 영역을 노출시키는 콘택홀을 형성하고, 상기 콘택홀을 포함한 전체 구조 상부에 스퍼터링 방법으로 제 1 티타늄 나이트라이드(TiN)층과 티타늄(Ti)층을 형성한 후 질소가 함유된 가스 분위기에서 급속 열질화 처리(RTN)를 실시함으로써 티타늄층은 미세 결정 구조의 제 2 티타늄 나이트라이드층으로 되고, 제 1 티타늄 나이트라이드층은 콘택홀 기저부에서 균일한 두께의 티타늄 실리사이드층으로 되며, 제 2 티타늄 나이트라이드층과 제 1 티타늄 나이트라이드층 및 티타늄 실리사이드층 사이에 티타늄 옥사이드(TiO)층이 형성되어 확산 방지 효과를 극대화시킨다.

대표도
도 3

색인어
층간 절연막, 콘택홀, 티타늄 옥사이드층, 티타늄 실리사이드층, 확산 방지막

GF Exhibit 1124 - 1840/2704

명세서

도면의 간단한 설명

도 1(a) 내지 1(c)는 종래의 반도체 소자의 확산 방지막 형성 방법을 설명하기 위한 소자의 단면도.

도 2는 도 1(c)의 콘택홀 기저부를 확대한 도면.

도 3(a) 내지 3(c)는 본 발명에 따른 반도체 소자의 확산 방지막 형성 방법을 설명하기 위한 소자의 단면도.

도 4는 도 3(c)의 콘택홀 기저부를 확대한 도면.

도 5(a) 및 도 5(b)는 종래의 방법으로 형성된 반도체 소자의 확산 방지막의 SEM 사진.

도 6(a) 및 도 6(b)는 본 발명에 따른 방법으로 형성된 반도체 소자의 확산 방지막의 SEM 사진.

< 도면의 주요 부분에 대한 부호 설명>

11 및 21 : 실리콘 기판12 및 22 : 층간 절연막

13 및 24 : 티타늄(Ti)층

14, 23 및 24A : 티타늄 나이트라이드(TiN)층

15 및 25 : 티타늄 실리사이드($TiSi_2$)층

26 : 티타늄 옥사이드(TiO)층17 및 27 : 텅스텐층

19 및 29 : 콘택홀

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 반도체 소자의 확산 방지막(metal barrier film) 형성 방법에 관한 것으로, 특히 콘택 저항을 감소시키며 확산 방지 효과를 증대시킬 수 있는 반도체 소자의 확산 방지막 형성 방법에 관한 것이다.

일반적으로, 반도체 소자가 고집적화 됨에 따라 콘택홀의 크기는 줄어들고 있다. 이에 따라 금속 콘택 공정시 콘택홀을 양호하게 매립하기 어렵고, 또한 콘택 저항이 증가되어 소자의 전기적 특성을 저하시키게 된다. 이를 해결하기 위하여, 티타늄(Ti)과 티타늄 나이트라이드(TiN)를 증착한 후 열처리하여 콘택홀 기저부에 티타늄 실리사이드($TiSi_2$)를 갖는 확산 방지막을 형성한다.

종래의 반도체 소자의 확산 방지막 형성 방법을 도 1(a) 내지 1(c)를 참조하여 설명하면 다음과 같다.

도 1(a)를 참조하면, 실리콘 기판(11) 상부에 형성된 층간 절연막(12)의 선택된 영역이 식각되어 실리콘 기판(11)의 소정 영역을 노출시키는 콘택홀(19)이 형성된다. 콘택홀(19)을 포함한 전체 구조 상부에 스퍼터링(sputtering) 방식으로 티타늄층(13) 및 티타늄 나이트라이드층(14)이 순차적으로 형성된다.

GF Exhibit 1124 - 1841/2704

도 1(b)를 참조하면, 질소(N_2) 또는 암모늄(NH_3) 가스 분위기에서 급속 열처리(Rapid Thermal Process; RTP) 공정을 실시하여 콘택홀(19) 기저부의 티타늄층(13)이 티타늄 실리사이드층(15)으로 변형되게 한다. 티타늄 실리사이드층(15)은 급속 열처리 공정 동안에 실리콘 기판(11)의 실리콘 원자(Si)와 티타늄층(13)의 티타늄 원자(Ti)가 상호 반응하여 형성된다.

이와 같이 티타늄층(13) 및 티타늄 나이트라이드층(14)을 순차적으로 형성한 후 급속 열처리 공정을 실시하여 확산 방지막이 형성되고, 이후 도 1(c)에 도시된 바와 같이, 텅스텐층(17)을 화학 기상 증착(Chemical Vapor Deposition ; CVD) 방식으로 형성한 후 패터닝하여 금속 배선이 형성된다.

도 1(c)의 콘택홀 기저부를 확대한 도 2에 도시된 바와 같이, 티타늄 나이트라이드층(14)은 원주형(columnar) 구조로 형성된다. 티타늄층(13)은 그 두께가 두꺼울 경우 급속 열처리에 의해 균일한 티타늄 실리사이드층을 형성할 수 있으나, 반도체 소자가 고집적화 되어감에 따라 콘택홀 크기가 줄어들어 종횡비(aspect ratio)가 크게되기 때문에 스퍼터링 방식으로 형성되는 티타늄층(13)의 층덮힘(step coverage)이 나쁘게 되므로 티타늄층(13)을 두껍게 형성하는데 한계가 있다. 티타늄층(13)을 두껍게 형성하기 위하여, 층덮힘이 우수한 CVD 방식을 적용하고 있으나, CVD 방식을 적용할 경우 박막에 불순물 함유량이 높아지는 등 많은 공정상의 문제점이 존재하므로 현재로서는 실질 공정에 적용하기 어려운 실정이다. 따라서, 텅스텐층(13)은 스퍼터링 방식으로 형성되며, 텅스텐층(13)의 두께가 임계 두께 이하일 경우 급속 열처리로 형성되는 티타늄 실리사이드층(15)은, 도 2에 도시된 바와 같이, 균일한 두께로 형성되지 못한다. 이와 같이 티타늄 나이트라이드층(14)이 원주형 구조를 갖고, 티타늄 실리사이드층(15)이 불균일하게 형성된 상태에서 WF_6가스를 이용하여 텅스텐층(17)을 형성할 경우, 형성 공정중에 원주형 구조의 티타늄 나이트라이드층(14)의 그레인 바운더리와 티타늄 실리사이드층(15)의 얇은 부분을 통해 텅스텐 원자(W)/플루오린 원자(F)와 실리콘 원자(Si)가 상호 확산되어 접합 파괴, 누설 전류 및 콘택 저항을 증가시켜 소자의 신뢰성을 저하시키는 문제점이 발생된다.

발명이 이루고자 하는 기술적 과제

따라서, 본 발명은 콘택 저항을 감소시키면서 확산 방지 효과를 증대시킬 수 있는 반도체 소자의 확산 방지막 및 그 형성 방법을 제공하는데 그 목적이 있다.

상술한 목적을 달성하기 위한 본 발명의 확산 방지막 형성 방법은 반도체 소자를 제조하기 위한 소정의 구조가 형성된 실리콘 기판 상부에 형성된 층간 절연막의 소정 영역을 식각하여 상기 실리콘 기판의 소정 영역을 노출시키는 콘택홀을 형성하는 단계와, 상기 콘택홀을 포함한 전체 구조 상부에 제 1 티타늄 나이트라이드층 및 티타늄층을 순차적으로 형성하는 단계와, 질소가 함유된 가스 분위기에서 열처리 공정을 실시함으로써 상기 티타늄층은 제 2 티타늄 나이트라이드층이 되고, 상기 제 1 티타늄 나이트라이드층과 상기 제 2 티타늄 나이트라이드층 사이에는 티타늄 옥사이드층이 생성되며, 상기 콘택홀 기저부의 제 1 티타늄 나이트라이드층은 티타늄 실리사이드층으로 되는 단계를 포함하여 이루어진 것을 특징으로 한다.

발명의 구성 및 작용

첨부된 도면을 참조하여 본 발명을 상세히 설명하기로 한다.

도 3(a) 내지 3(c)는 본 발명에 따른 반도체 소자의 확산 방지막 형성 방법을 설명하기 위한 소자의 단면도이고, 도 4는 도 3(c)의 콘택홀 기저부를 확대한 도면이다.

도 3(a)를 참조하면, 반도체 소자를 제조하기 위한 소정의 구조가 형성된 실리콘 기판(21) 상부에 형성된 층간 절연막(22)의 선택된 영역을 식각하여 실리콘 기판(21)의 소정 영역을 노출시키는 콘택홀(29)이 형성된다. 콘택홀(29)을 포함한 전체 구조 상부에 스퍼터링 방식으로 제 1 티타늄 나이트라이드층(23) 및 티타늄층(24)이 순차적으로 형성된다. 제 1 티타늄 나이트라이드층(23)은 약 50Å 의 두께로 형성되며, 티타늄층(24)은 약 400~600Å 의 두께로 형성된다.

GF Exhibit 1124 - 1842/2704

도 3(b)는 열처리 공정을 실시한 상태의 단면도로서, 열처리 공정은 저압용 반응로(low pressure furnace)에서 실시하거나 급속 열질화 처리(Rapid Thermal Nitridation; RTN)로 하며, 이때 분위기는 질소(N_2) 가스, 암모늄(NH_3) 가스 및 질소(N_2)와 암모늄(NH_3)의 혼합 가스 분위기중 어느 하나의 분위기로 한다. 열처리 결과, 티타늄층(24)은 제 2 티타늄 나이트라이드층(24A)으로 되고, 제 1 티타늄 나이트라이드층(23)과 제 2 티타늄 나이트라이드층(24A) 사이에는 티타늄 옥사이드층(TiO; 26)이 생성되며, 콘택홀(29) 기저부의 제 1 티타늄 나이트라이드층(23)은 티타늄 실리사이드층(25)으로 된다. 티타늄 실리사이드층(25)은 열처리 동안에 실리콘 기판(21)의 실리콘 원자(Si)와 제 1 티타늄 나이트라이드층(23)의 티타늄 원자(Ti)가 상호 반응함으로써 형성된다.

이와 같이 제 1 티타늄 나이트라이드층(23) 및 티타늄층(24)을 순차적으로 형성한 후 질소 분위기에서 열처리를 실시하여 확산 방지막이 완성되고, 이후 도 3(c)에 도시된 바와 같이, 텅스텐층(27)을 화학 기상 증착(Chemical Vapor Deposition; CVD) 방식으로 형성한 후 패터닝하여 금속 배선이 형성한다.

도 3(c)의 콘택홀 기저부를 확대한 도 4에 도시된 바와 같이, 제 2 티타늄 나이트라이드층(24A)은 미세 결정(microcrystalline) 구조로 형성된다. 티타늄 실리사이드층(25) 형성을 위한 열처리 공정 동안에 제 1 티타늄 나이트라이드층(23)에 함유된 질소 원자가 티타늄 원자와 실리콘 원자의 반응 속도 및 양을 일정하게 제어해 주기 때문에 제 1 티타늄 나이트라이드층(23)이 약 50Å 두께로 얇게 형성되더라도, 도 4에 도시된 바와 같이, 티타늄 실리사이드층(25)은 균일하게 형성된다. 따라서, 제 2 티타늄 나이트라이드층(24A)이 미세 결정 구조를 갖고, 티타늄 실리사이드층(25)이 균일하게 형성된 상태에서 WF_6가스를 이용하여 텅스텐층(27)을 형성할 경우, 형성 공정중에 텅스텐 원자(W)/플루오린 원자(F)와 실리콘 원자(Si)가 상호 확산되는 것이 방지된다. 한편, 열처리 동안에 극히 적은 산소(O_2) 가스에 의해 형성된 티타늄 옥사이드층(26)이 제 2 티타늄 나이트라이드층(24A)과 티타늄 실리사이드층(25) 사이에 존재하므로써, 확산 방지 효과는 더욱 극대화된다.

본 발명의 다른 실시 예로서 실리콘을 함유한 막 상부에 티타늄을 증착한 후 상술한 방법과 동일한 조건에서 급속 열질화 공정을 실시한 후 티타늄 나이트라이드층을 형성해도 동일한 효과를 얻을 수 있다.

도 5(a) 및 도 5(b)는 종래의 방법으로 형성된 반도체 소자의 확산 방지막의 SEM 사진이고, 도 6(a) 및 도 6(b)는 본 발명에 따른 방법으로 형성된 반도체 소자의 확산 방지막의 SEM 사진이다.

도 5(a)를 참조하면, 100Å 의 티타늄층을 형성하고 200Å 의 티타늄 나이트라이드층을 형성한 후 급속 열처리 공정을 실시하면 그레인 바운더리에서 티타늄 실리사이드의 덩어리가 형성된다. 이러한 상태에서 도 5(b)에서와 같이 890℃의 온도에서 1시간동안 열처리 공정을 실시하면 텅스텐 실리사이드층 하부에서 실리콘의 손실이 발생된다.

도 6(a)를 참조하면, 100Å 의 티타늄층을 형성하고 급속 열질화 공정을 실시한 후 200Å 의 티타늄 나이트라이드층을 형성하고 급속 열질화 공정을 실시한다. 이러한 공정에 의해 티타늄층과 티타늄 나이트라이드층 사이에 티타늄 실리사이드층과 티타늄 옥사이드층이 형성된다. 이러한 상태에서 도 6(b)에서와 같이 890℃의 온도에서 1시간동안 열공정을 실시하더라도 균일한 막질을 얻을 수 있다.

발명의 효과

상술한 바와 같이, 본 발명은 확산 방지막으로 스퍼터링 방식에 의해 제 1 티타늄 나이트라이드(TiN)층과 티타늄(Ti)층을 형성한 후 질소가 함유된 가스 분위기에서 급속 열질화 처리(RTN)를 실시하여 티타늄층을 미세 결정 구조의 제 2 티타늄 나이트라이드층으로 변형시키고, 콘택홀 기저부의 제 1 티타늄 나이트라이드층을 균일한 두께의 티타늄 실리사이드층으로 변형시키며, 제 1 티타늄 나이트라이드층과 티타늄 실리사이드층 사이에 티타늄 옥사이드(TiO)층이 형성되어 확산 방지 효과를 극대화시킬 수 있다.

(57) 청구의 범위

청구항 1.

GF Exhibit 1124 - 1843/2704

소정의 구조가 형성된 실리콘 기판 상부에 층간 절연막을 형성한 후 상기 층간 절연막의 소정 영역을 식각하여 상기 실리콘 기판의 소정 영역을 노출시키는 콘택홀을 형성하는 단계와,

상기 콘택홀을 포함한 전체 구조 상부에 제 1 티타늄 나이트라이드층 및 티타늄층을 순차적으로 형성하는 단계와,

질소가 함유된 가스 분위기에서 열처리 공정을 실시하고, 이에 의해 상기 티타늄층은 제 2 티타늄 나이트라이드층으로 변화되고, 상기 제 1 티타늄 나이트라이드층과 상기 제 2 티타늄 나이트라이드층 사이에는 티타늄 옥사이드층이 생성되며, 상기 콘택홀 기저부의 제 1 티타늄 나이트라이드층은 티타늄 실리사이드층으로 변화되는 단계를 포함하여 이루어진 것을 특징으로 하는 반도체 소자의 확산 방지막 형성 방법.

청구항 2.

제 1 항에 있어서, 상기 열처리 공정은 질소(N_2) 가스, 암모늄(NH_3) 가스 및 질소(N_2)와 암모늄(NH_3)의 혼합 가스 분위기중 어느 하나의 분위기에서 실시하는 급속 열질화 공정인 것을 특징으로 하는 반도체 소자의 확산 방지막 형성 방법.

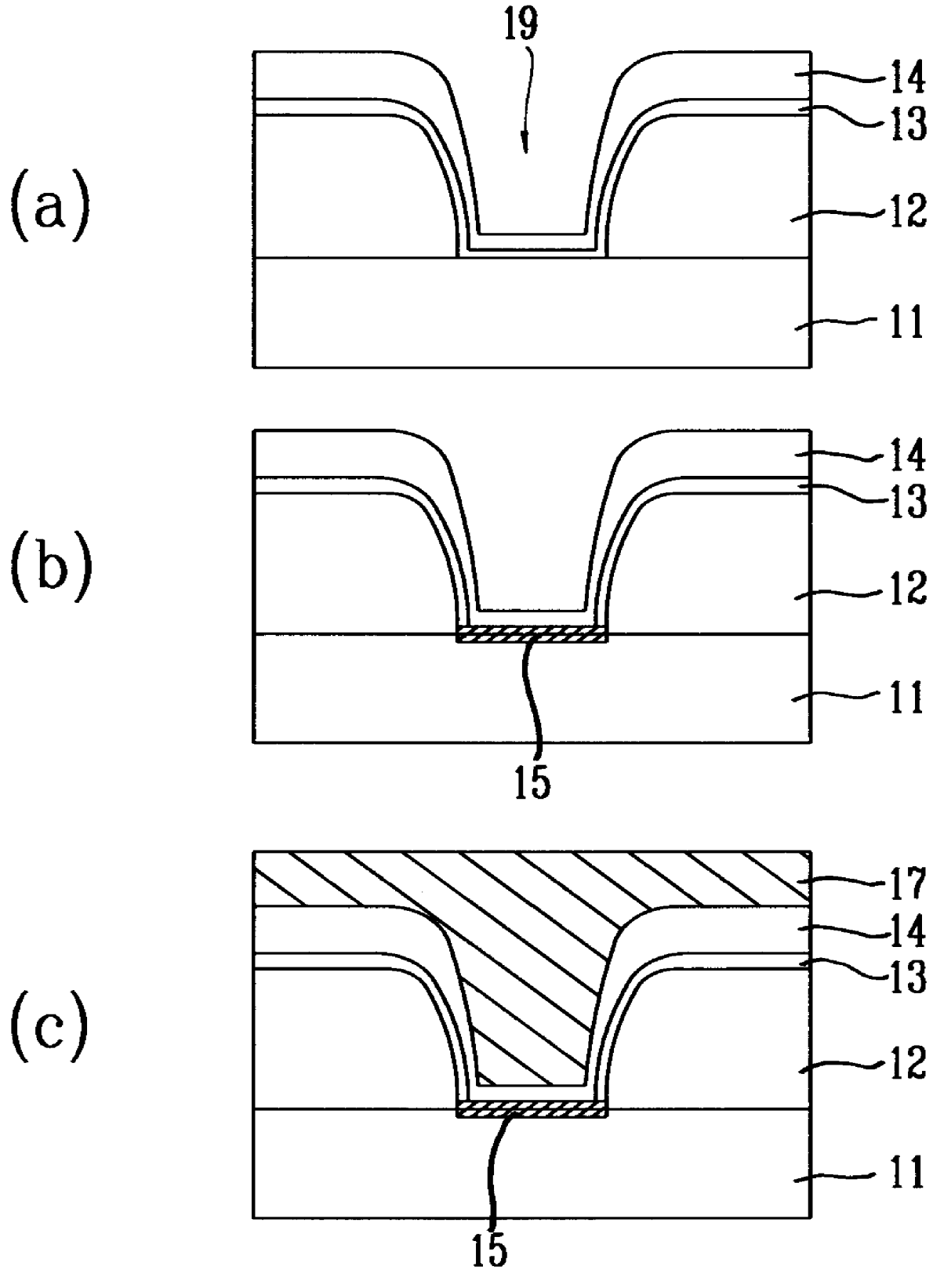
청구항 3.

제 1 항에 있어서, 상기 티타늄층은 400 내지 600Å 의 두께로 형성되는 것을 특징으로 하는 반도체 소자의 확산 방지막 형성 방법.

도면

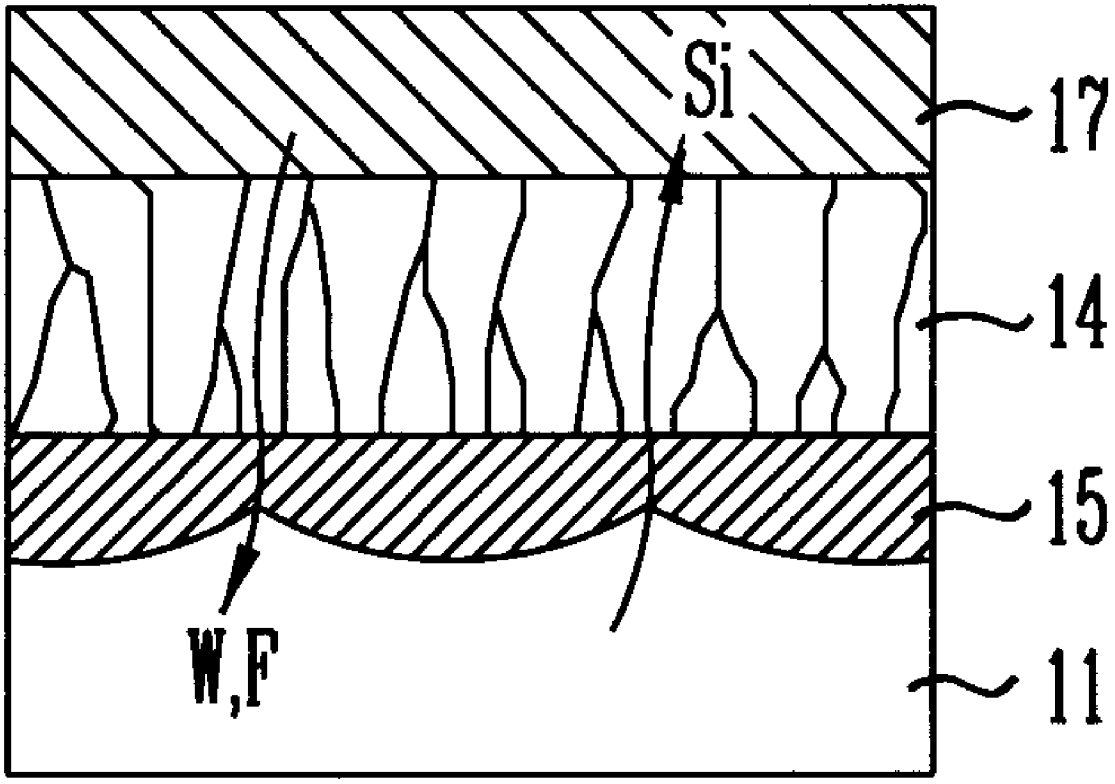
GF Exhibit 1124 - 1844/2704

도면 1



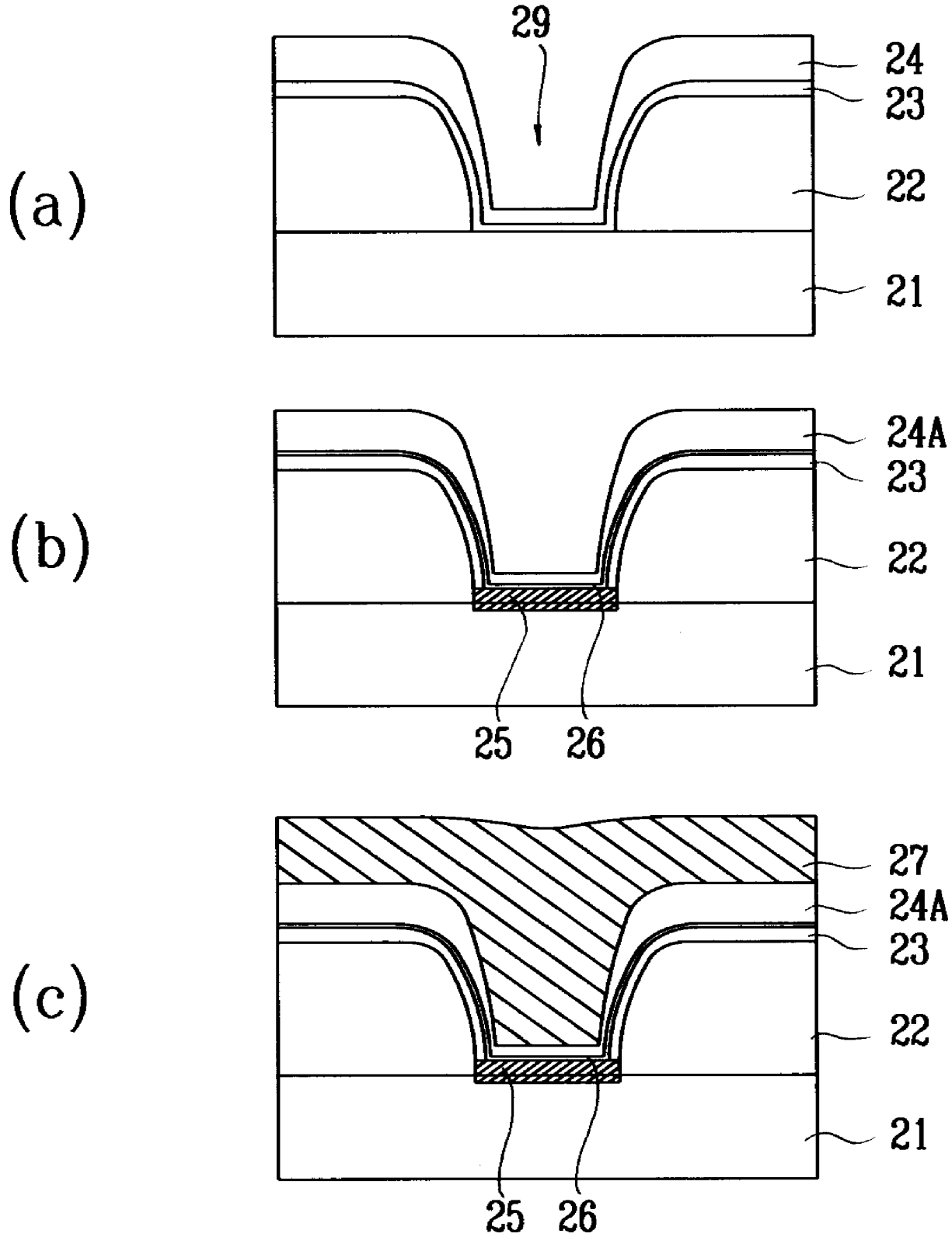
GF Exhibit 1124 - 1845/2704

도면 2



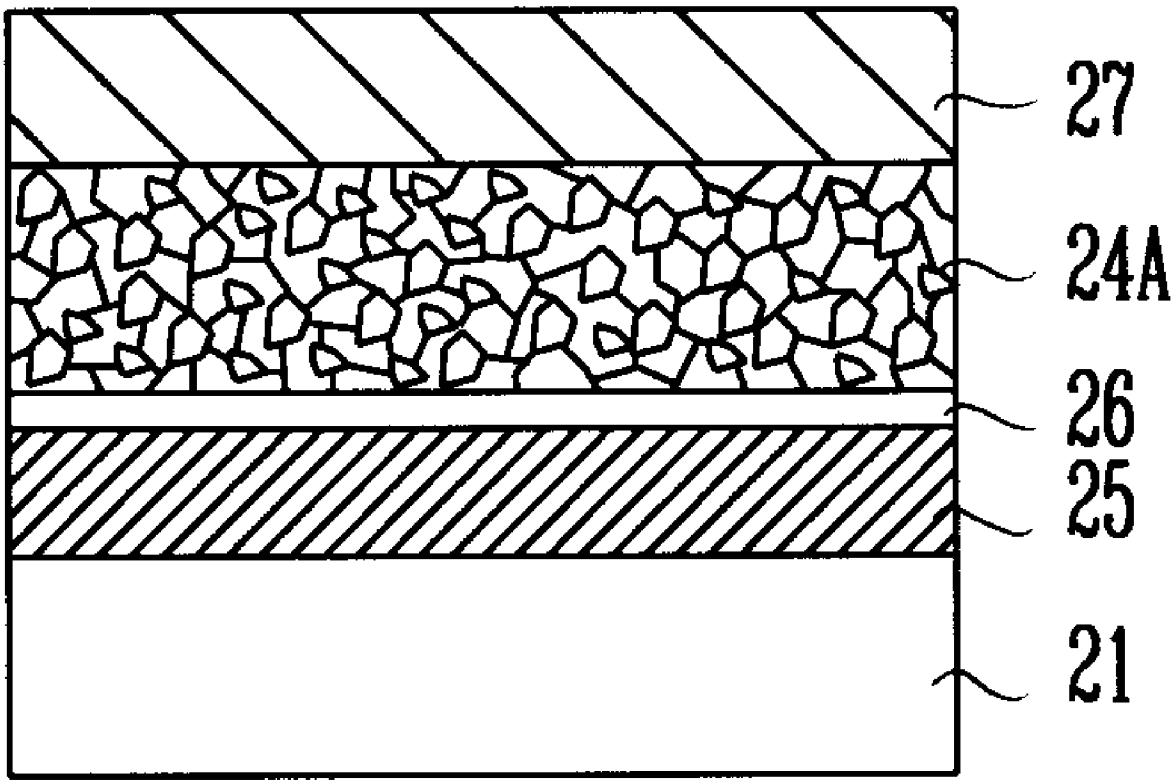
GF Exhibit 1124 - 1846/2704

도면 3

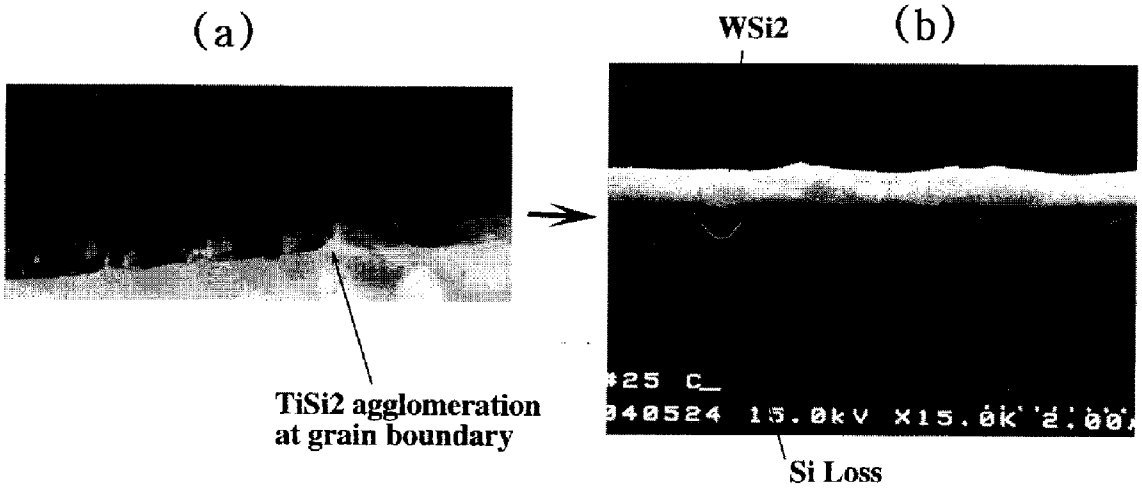


GF Exhibit 1124 - 1847/2704

도면 4

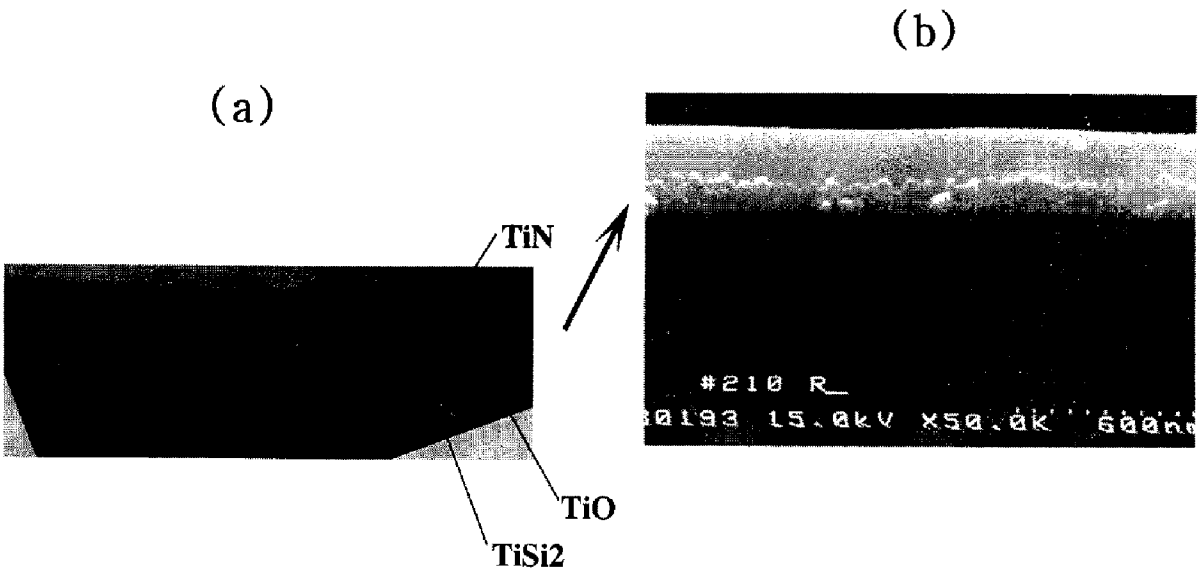


도면 5



GF Exhibit 1124 - 1848/2704

도면 6



GF Exhibit 1124 - 1849/2704

Examined Patent Publication(B1)

Bibliographic Data

Int.Cl.	H01L 21/768
Published Date	20010807
Registration No.	1002904670000
Registration Date	20010302
Application No.	1019970081150
Application Date	19971231
Unexamined Publication No.	1019990060904
Unexamined Publication Date	19990726
Requested Date of Examination	19971231
Agent.	SHIN, Young Moo | CHOI, Sung Min
Inventor	Sang-Gi Hong | U-Hyeon Kim
Applicant	SK hynix Inc.
Rightholder	Hyundai Electronics industry CO., LTD

발명의 명칭

반도체소자의확산방지막형성방법

Title of Invention

METHOD FOR FORMING DIFFUSION BARRIER LAYER OF SEMICONDUCTOR DEVICE

요약

본 발명은 반도체 소자의 확산 방지막 형성 방법에 관한 것으로, 실리콘 기판 상부에 형성된 층간 절연막의 소정 영역을 식각하여 상기 실리콘 기판의 소정 영역을 노출시키는 콘택홀을 형성하고, 상기 콘택홀을 포함한 전체 구조 상부에 스퍼터링 방법으로 제 1 티타늄 나이트라이드(TiN)층과 티타늄(Ti)층을 형성한 후 질소가 함유된 가스 분위기에서 급속 열질화 처리(RTN)를 실시함으로써 티타늄층은 미세 결정 구조의 제 2 티타늄 나이트라이드층으로 되고, 제 1 티타늄 나이트라이드층은 콘택홀 기저부에서 균일한 두께의 티타늄 실리사이드층으로 되며, 제 2 티타늄 나이트라이드층과 제 1 티타늄 나이트라이드층 및 티타늄 실리사이드층 사이에 티타늄 옥사이드(TiO)층이 형성되어 확산 방지 효과를 극대화시킨다.

Abstract

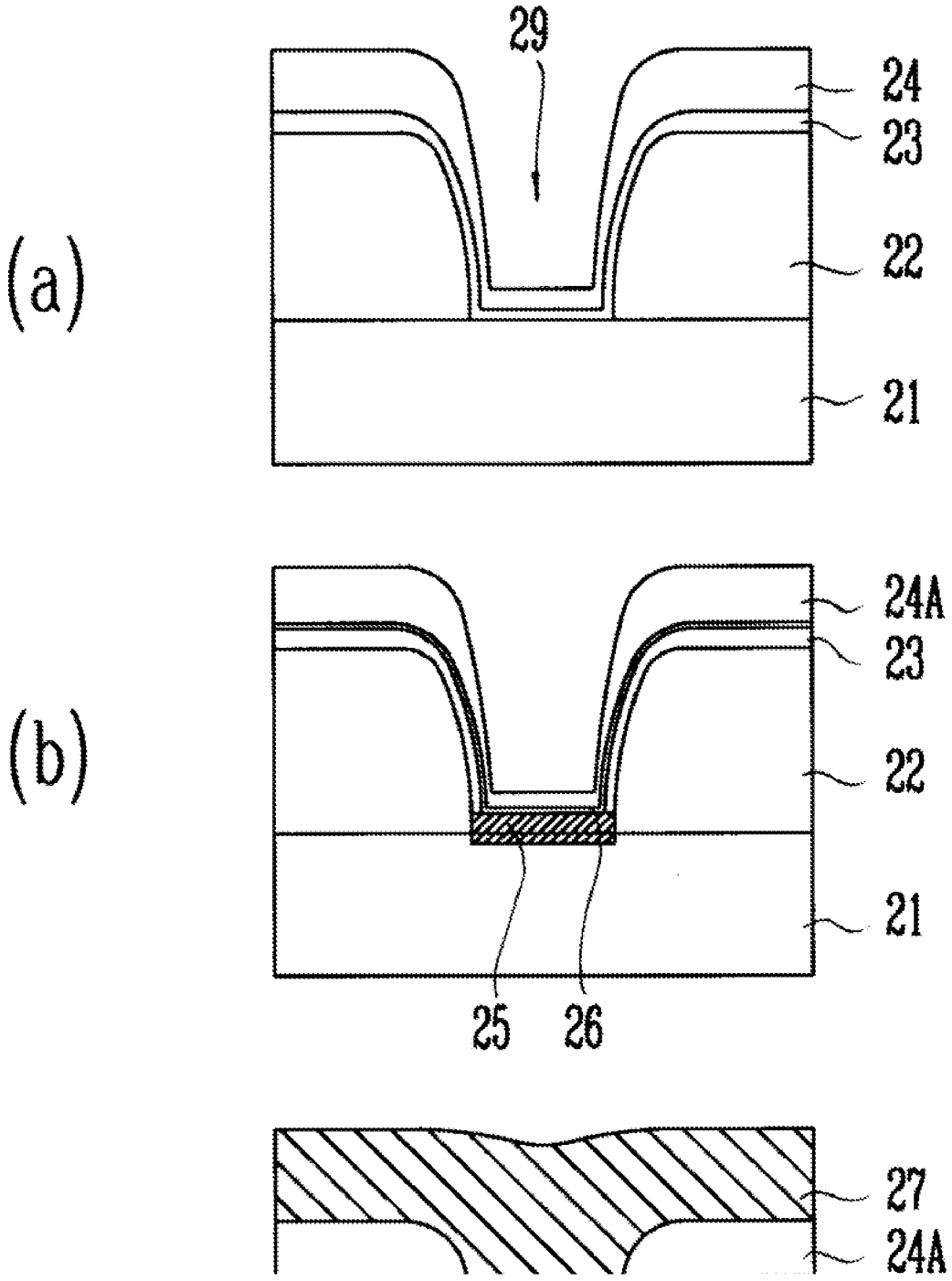
According to the invention, the contact hole etching the fixed region of the formed inter-layer insulating film and exposes the fixed region of the silicon substrate are formed in the upper silicon substrate as the method for forming diffusing barrier layer, of the semiconductor device. And by performing the rapid thermal nitridation (RTN) in the first titanium nitride (TiN) layer and the gas atmosphere in which nitrogen is the titanium (Ti) layer contained after doing the formation to the sputtering method including the contact hole the titanium layer is to the second titanium nitride layer of the nanocryatalline structure and the first titanium nitri

층간 절연막, 콘택홀, 티타늄 옥사이드층, 티타늄 실리사이드층, 확산 방지막

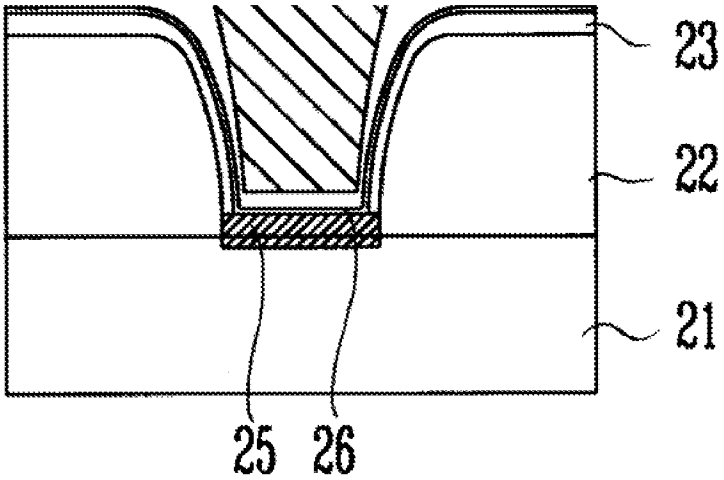
de layer is in the contact hole fundament to the titanium silicide layer of the uniform thickness and the titanium oxide (TiO) layer is formed between the second titanium nitride layer, the first titanium nitride layer and titanium silicide layer and the scattering prevention effect is maximized.

The inter-layer insulating film, the contact hole, the titanium oxide layer, the titanium silicide layer, the diffusion barrier .

대표도면(Representative drawing)



(c)



청구의 범위

청구 3항:

제 1 항에 있어서, 상기 티타늄층은 400 내지 600Å의 두께로 형성되는 것을 특징으로 하는 반도체 소자의 확산 방지막 형성 방법.

Scope of Claims

Claim 3:

As for claim 1, the method for forming diffusing barrier layer of the semiconductor device in which the titanium layer is formed into the thickness of 400 through 600Å.

배경기술

본 발명은 반도체 소자의 확산 방지막(metal barrier film) 형성 방법에 관한 것으로, 특히 콘택 저항을 감소시키며 확산 방지 효과를 증대시킬 수 있는 반도체 소자의 확산 방지막 형성 방법에 관한 것이다.

일반적으로, 반도체 소자가 고집적화 됨에 따라 콘택홀의 크기는 줄어들고 있다. 이에 따라 금속 콘택 공정시 콘택홀을 양호하게 매립하기 어렵고, 또한 콘택 저항이 증가되어 소자의 전기적 특성을 저하시키게 된다. 이를 해결하기 위하여, 티타늄(Ti)과 티타늄 나이트라이드(TiN)를 증착한 후 열처리하여 콘택홀 기저부에 티타늄 실리사이드(TiSi2)를 갖는 확산 방지막을 형성한다.

종래의 반도체 소자의 확산 방지막 형성 방법을 도 1(a) 내지 1(c)를 참조하여 설명하면 다음과 같다.

도 1(a)를 참조하면, 실리콘 기판(11) 상부에 형성된 층간 절연막(12)의 선택된 영역이 식각되어 실리콘 기판(11)의 소정 영역을 노출시키는 콘택홀(19)이 형성된다. 콘택홀(19)을 포함한 전체 구조 상부에 스퍼터링(sputtering) 방식으로 티타늄층(13) 및 티타늄 나이트라이드층(14)이 순차적으로 형성

Background Art

The invention relates to the diffusion barrier (metal barrier film) formation method of the semiconductor device, and particularly, to the method for forming diffusing barrier layer of the semiconductor device which can increase the scattering prevention effect while reducing the contact resistance.

Generally, the size of the contact hole is decreased as the semiconductor device is highly integrated. Accordingly, it is difficult in the metal contact process to be good reclaim the contact hole and moreover, the contact resistance is increased and the electrical characteristic of the device is lowered. To solve this, the titanium (Ti) and the diffusion barrier heat-treating the titanium nitride (TiN) after doing the deposition and has the titanium silicide (TiSi(SB)2(/SB)) on the contact hole fundament are formed.

The method for forming diffusing barrier layer of the conventional semiconductor device is made to be equal to the next it illustrates with reference to Figure 1(a) to 1 (c).

The contact hole (19) in which the selected domain of the inter-layer insulating film (12) formed in upper part the silicon substrate (11) is etched with reference to Figure 1(a) and exposing the fixed region of the silicon substrate (11) is formed. The

된다.

도 1(b)를 참조하면, 질소(N2) 또는 암모늄(NH3) 가스 분위기에서 급속 열처리(Rapid Thermal Process; RTP) 공정을 실시하여 콘택홀(19) 기저부의 티타늄층(13)이 티타늄 실리사이드층(15)으로 변형되게 한다. 티타늄 실리사이드층(15)은 급속 열처리 공정 동안에 실리콘 기판(11)의 실리콘 원자(Si)와 티타늄층(13)의 티타늄 원자(Ti)가 상호 반응하여 형성된다.

이와 같이 티타늄층(13) 및 티타늄 나이트라이드층(14)을 순차적으로 형성한 후 급속 열처리 공정을 실시하여 확산 방지막이 형성되고, 이후 도 1(c)에 도시된 바와 같이, 텅스텐층(17)을 화학 기상 증착(Chemical Vapor Deposition; CVD) 방식으로 형성한 후 패터닝하여 금속 배선이 형성된다.

도 1(c)의 콘택홀 기저부를 확대한 도 2에 도시된 바와 같이, 티타늄 나이트라이드층(14)은 원주형(columnar) 구조로 형성된다. 티타늄층(13)은 그 두께가 두꺼울 경우 급속 열처리에 의해 균일한 티타늄 실리사이드층을 형성할 수 있으나, 반도체 소자가 고집적화 되어감에 따라 콘택홀 크기가 줄어들어 종횡비(aspect ratio)가 크게되기 때문에 스퍼터링 방식으로 형성되는 티타늄층(13)의 층덮힘(step coverage)이 나쁘게 되므로 티타늄층(13)을 두껍게 형성하는데 한계가 있다. 티타늄층(13)을 두껍게 형성하기 위하여, 층덮힘이 우수한 CVD 방식을 적용하고 있으나, CVD 방식을 적용할 경우 박막에 불순물 함유량이 높아지는 등 많은 공정상의 문제점이 존재하므로 현재로서는 실질 공정에 적용하기 어려운 실정이다. 따라서, 텅스텐층(13)은 스퍼터링 방식으로 형성되며, 텅스텐층(13)의 두께가 임계 두께 이하일 경우 급속 열처리로 형성되는 티타늄 실리사이드층(15)은, 도 2에 도시된 바와 같이, 균일한 두께로 형성되지 못한다. 이와 같이 티타늄 나이트라이드층(14)이 원주형 구조를 갖고, 티타늄 실리사이드층(15)이 불균일하게 형성된 상태에서 WF6 가스를 이용하여 텅스텐층(17)을 형성할 경우, 형성 공정중에 원주형 구조의 티타늄 나이트라이드층(14)의 그레인 바운더리와 티타늄 실리사이드층(15)의 얇은 부분을 통해 텅스텐 원자(W)/플루오린 원자(F)와 실리콘 원자(Si)가 상호 확산되어 접합 파괴, 누설 전류 및 콘택 저항을 증가시켜 소자의 신뢰성을 저하시키는 문제점이 발생된다.

titanium layer (13) and titanium nitride layer (14) are successively formed with the sputtering mode including the contact hole (19).

In the nitrogen (N(SB)2(/SB)) with reference to Figure 1(b) or the ammonium (NH(SB)3(/SB)) gas atmosphere, the rapid thermal processing (Rapid Thermal Process: RTP) process is performed and the titanium layer (13) of the contact hole (19) base part is transformed into into the titanium silicide layer (15). The silicon atom (Si) of the silicon substrate (11) and titanium atom (Ti) of the titanium layer (13) cross-react and the titanium silicide layer (15) is formed for the rapid thermal processing.

In this way, the rapid thermal processing is successively performed after doing the formation and the diffusion barrier is formed with the titanium layer (13) and titanium nitride layer (14) as the and the tungsten layer (17) is patterned in the chemical vapor deposition (Chemical Vapor Deposition: CVD) mode after doing the formation and after the metal wiring is formed as shown in 1 (c).

The titanium nitride layer (14) enlarging the contact hole fundament of Figure 1(c) is formed with the columnar structure. In case the titanium layer (13) the thickness is thick the uniform titanium silicide layer can be formed with the rapid thermal processing. But as the semiconductor device is highly integrated the contact hole size is decreased and because the aspect ratio is large since the step coverage of the titanium layer (13) formed with the sputtering method is bad the titanium layer (13) is thickly formed but it has the limit. In order that the titanium layer (13) is thickly formed the CVD manner in which the step coverage is excellent is applied. But it is the difficult actual condition that it applies to the parenchyma process since the problem of many eutectic phase exists the impurity content is enhanced in the thin film in case of applying the CVD manner. Therefore, the titanium silicide layer (15) which the tungsten layer (13) is formed with the sputtering method and is formed into the rapid thermal processing in case the thickness of the tungsten layer (13) is the critical thickness or less as shown in FIG. 2 is unable to be formed with the uniform thickness. In this way, the titanium nitride layer (14) has the columnar structure and when the tungsten layer (17) is formed at the state is uneven where the titanium silicide layer (15) is formed using the WF 6 gas the problem of the tungsten atom (W) / fluorine atom (F) and silicon atom (Si) being mutually diffused among the formation process through the thin part of the grain boundary of the titanium nitride layer (14) of the columnar structure and titanium silicide l

ayer (15) and increasing the junction breakdown, and the leakage current and contact resistance an d decreasing the reliability of the device is genera ted.

발명의 내용

발명의 효과

상술한 바와 같이, 본 발명은 확산 방지막으로 스퍼터링 방식에 의해 제 1 티타늄 나이트라이드(TiN)층과 티타늄(Ti)층을 형성한 후 질소가 함유된 가스 분위기에서 급속 열질화 처리(RTN)를 실시하여 티타늄층을 미세 결정 구조의 제 2 티타늄 나이트라이드층으로 변형시키고, 콘택홀 기저부의 제 1 티타늄 나이트라이드층을 균일한 두께의 티타늄 실리사이드층으로 변형시키며, 제 1 티타늄 나이트라이드층과 티타늄 실리사이드층 사이에 티타늄 옥사이드(TiO)층이 형성되어 확산 방지 효과를 극대화시킬 수 있다.

Summary of Invention

Effects of the Invention

As described above, in the invention is the first titanium nitride (TiN) layer by the diffusion barrier the sputtering method and the gas atmosphere in which nitrogen is the titanium (Ti) layer contained after doing the formation, the rapid thermal nitridation (RTN) is performed and the titanium layer is transformed to the second titanium nitride layer of the nanocryatalline structure and the first titanium nitride layer of the contact hole fundament is transformed to the titanium silicide layer of the uniform thickness and the titanium oxide (TiO) layer is formed between the first titanium nitride layer and titanium silicide layer and the scattering prevention effect can be maximized.

기술적 과제

따라서, 본 발명은 콘택 저항을 감소시키면서 확산 방지 효과를 증대시킬 수 있는 반도체 소자의 확산 방지막 및 그 형성 방법을 제공하는데 그 목적이 있다.

상술한 목적을 달성하기 위한 본 발명의 확산 방지막 형성 방법은 반도체 소자를 제조하기 위한 소정의 구조가 형성된 실리콘 기판 상부에 형성된 층간 절연막의 소정 영역을 식각하여 상기 실리콘 기판의 소정 영역을 노출시키는 콘택홀을 형성하는 단계와, 상기 콘택홀을 포함한 전체 구조 상부에 제 1 티타늄 나이트라이드층 및 티타늄층을 순차적으로 형성하는 단계와, 질소가 함유된 가스 분위기에서 열처리 공정을 실시함으로써 상기 티타늄층은 제 2 티타늄 나이트라이드층이 되고, 상기 제 1 티타늄 나이트라이드층과 상기 제 2 티타늄 나이트라이드층 사이에는 티타늄 옥사이드층이 생성되며, 상기 콘택홀 기저부의 제 1 티타늄 나이트라이드층은 티타늄 실리사이드층으로 되는 단계를 포함하여 이루어진 것을 특징으로 한다.

Technical Task

Therefore, an object of the present invention is to provide the diffusion barrier of the semiconductor device which can increase the scattering preventi on effect while it reduces the contact resistance a nd method for forming the same.

The method for forming diffusing barrier layer of t he invention for achieving the above-described pu rpose comprises the step on the upper part of the entire structure, of successively forming the first t itanium nitride layer and titanium layer, and the s tep in the titanium layer, the second titanium nitri de layer is by performing the thermal process in t he gas atmosphere etching the fixed region of the inter-layer insulating film formed in the upper silic on substrate in which the predetermined structure for manufacturing the semiconductor device is for med and include the step of forming the contact h ole exposing the fixed region of the silicon substra te, and the contact hole. As to the step in the tita nium layer, the second titanium nitride layer is by, nitrogen occurs plentifully and the titanium oxide layer is generated between the first titanium nitri de layer and the second titanium nitride layer and that the first titanium nitride layer of the contact hole fundament consists of the titanium silicide la yer.

발명의 구성 및 작용

첨부된 도면을 참조하여 본 발명을 상세히 설명하기로 한다.

도 3(a) 내지 3(c)는 본 발명에 따른 반도체 소자의 확산 방지막 형성 방법을 설명하기 위한 소자의 단면도이고, 도 4는 도 3(c)의 콘택홀 기저부를 확대한 도면이다.

도 3(a)를 참조하면, 반도체 소자를 제조하기 위한 소정의 구조가 형성된 실리콘 기판(21) 상부에 형성된 층간 절연막(22)의 선택된 영역을 식각하여 실리콘 기판(21)의 소정 영역을 노출시키는 콘택홀(29)이 형성된다. 콘택홀(29)을 포함한 전체 구조 상부에 스퍼터링 방식으로 제 1 티타늄 나이트라이드층(23) 및 티타늄층(24)이 순차적으로 형성된다. 제 1 티타늄 나이트라이드층(23)은 약 50Å의 두께로 형성되며, 티타늄층(24)은 약 400~600Å의 두께로 형성된다.

도 3(b)는 열처리 공정을 실시한 상태의 단면도로서, 열처리 공정은 저압용 반응로(low pressure furnace)에서 실시하거나 급속 열질화 처리(Rapid Thermal Nitridation; RTN)로 하며, 이때 분위기는 질소(N2) 가스, 암모늄(NH3) 가스 및 질소(N2)와 암모늄(NH3)의 혼합 가스 분위기중 어느 하나의 분위기로 한다. 열처리 결과, 티타늄층(24)은 제 2 티타늄 나이트라이드층(24A)으로 되고, 제 1 티타늄 나이트라이드층(23)과 제 2 티타늄 나이트라이드층(24A) 사이에는 티타늄 옥사이드층(TiO; 26)이 생성되며, 콘택홀(29) 기저부의 제 1 티타늄 나이트라이드층(23)은 티타늄 실리사이드층(25)으로 된다. 티타늄 실리사이드층(25)은 열처리 동안에 실리콘 기판(21)의 실리콘 원자(Si)와 제 1 티타늄 나이트라이드층(23)의 티타늄 원자(Ti)가 상호 반응함으로써 형성된다.

이와 같이 제 1 티타늄 나이트라이드층(23) 및 티타늄층(24)을 순차적으로 형성한 후 질소 분위기에서 열처리를 실시하여 확산 방지막이 완성되고, 이후 도 3(c)에 도시된 바와 같이, 텅스텐층(27)을 화학 기상 증착(Chemical Vapor Deposition; CVD) 방식으로 형성한 후 패터닝하여 금속 배선이 형성한다.

Structure & Operation of the Invention

The attached invention decides to be particularly illustrated.

It is the cross-sectional view in which Figure 3(a) to 3 (c) illustrates the method for forming diffusing barrier layer of the semiconductor device according to the present invention of the device. And figure 4 is a magnificated drawing the contact hole fundament of Figure 3(c).

The contact hole (29) etching the selected domain of the inter-layer insulating film (22) formed in upper part the silicon substrate (21) in which the predetermined structure for manufacturing the semiconductor device is formed with reference to Figure 3(a) and exposes the fixed region of the silicon substrate (21) is formed. The first titanium nitride layer (23) and titanium layer (24) are successively formed with the sputtering method including the contact hole (29). The first titanium nitride layer (23) is formed with the thickness of about 50 Å and the titanium layer (24) is formed into the thickness of about 400~600Å.

Figure 3(b) is the cross-sectional view of the state performing the thermal process. The thermal process performs in for low voltage furnace (low pressure furnace) or it does to the rapid thermal nitridation (Rapid Thermal Nitridation: RTN) and the environment does among the nitrogen (N(SB)2(/SB)) gas, and the ammonium (NH(SB)3(/SB)) gas, the nitrogen (N(SB)2(/SB)) and mixed gas atmosphere of the ammonium (NH(SB)3(/SB)) to one mood. The heat treatment result , and the titanium layer (24) consist of the second titanium nitride layer (24A) and the titanium oxide layer (TiO: 26) is generated between the first titanium nitride layer (23) and the second titanium nitride layer (24A) and the first titanium nitride layer (23) of the contact hole (29) base part consists of the titanium silicide layer (25). The titanium silicide layer (25) is formed for the thermal process since the silicon atom (Si) of the silicon substrate (21) and titanium atom (Ti) of the first titanium nitride layer (23) cross-react.

In this way, the first titanium nitride layer (23) and titanium layer (24) the thermal process are successively performed after doing the formation in the nitrogen atmosphere and the diffusion barrier is completed and the tungsten layer (27) is patterned in the chemical vapor deposition (Chemical Vapor Deposition: CVD) mode after doing the formation and after the metal wiring forms as shown in 3 (c).

도 3(c)의 콘택홀 기저부를 확대한 도 4에 도시된 바와 같이, 제 2 티타늄 나이트라이드층(24A)은 미세 결정(microcrystalline) 구조로 형성된다. 티타늄 실리사이드층(25) 형성을 위한 열처리 공정 동안에 제 1 티타늄 나이트라이드층(23)에 함유된 질소 원자가 티타늄 원자와 실리콘 원자의 반응 속도 및 양을 일정하게 제어해 주기 때문에 제 1 티타늄 나이트라이드층(23)이 약 50Å 두께로 얇게 형성되더라도, 도 4에 도시된 바와 같이, 티타늄 실리사이드층(25)은 균일하게 형성된다. 따라서, 제 2 티타늄 나이트라이드층(24A)이 미세 결정 구조를 갖고, 티타늄 실리사이드층(25)이 균일하게 형성된 상태에서 WF6 가스를 이용하여 텅스텐층(27)을 형성할 경우, 형성 공정중에 텅스텐 원자(W)/플루오린 원자(F)와 실리콘 원자(Si)가 상호 확산되는 것이 방지된다. 한편, 열처리 동안에 극히 적은 산소(O2) 가스에 의해 형성된 티타늄 옥사이드층(26)이 제 2 티타늄 나이트라이드층(24A)과 티타늄 실리사이드층(25) 사이에 존재하므로써, 확산 방지 효과는 더욱 극대화된다.

The second titanium nitride layer (24A) enlarging the contact hole fundament of Figure 3(c) is formed with the microcrystal (microcrystalline) structure. Because the nitrogen atom contained in the first titanium nitride layer (23) for the thermal process for the titanium silicide layer (25) formation regularly controls the reaction speed of the titanium atom and silicon atom and amount the first titanium nitride layer (23) is formed into about 50Å thickness. And yet the titanium silicide layer (25) is uniformly formed. Therefore, the second titanium nitride layer (24A) has the nanocryatalline structure and when the tungsten layer (27) is formed at the state where the titanium silicide layer (25) is uniformly formed using the WF 6 gas the state is prevented among the formation process that the tungsten atom (W) / fluorine atom (F) and silicon atom (Si) are mutually diffused. In the meantime, the titanium oxide layer (26) formed by the oxygen (O(SB)2(/SB)) gas which is exceedingly less for the thermal process exists between the second titanium nitride layer (24A) and titanium silicide layer (25). In that way the scattering prevention effect becomes more maximized.

본 발명의 다른 실시 예로서 실리콘을 함유한 막 상부에 티타늄을 증착한 후 상술한 방법과 동일한 조건에서 급속 열질화 공정을 실시한 후 티타늄 나이트라이드층을 형성해도 동일한 효과를 얻을 수 있다.

In the method and the same condition describing in detail at the upper part of the film containing the silicone as the dissimilar embodiment of the invention after depositing titanium, even if the titanium nitride layer is formed after the rapid thermal nitridation is performed the same effect can be obtained.

도 5(a) 및 도 5(b)는 종래의 방법으로 형성된 반도체 소자의 확산 방지막의 SEM 사진이고, 도 6(a) 및 도 6(b)는 본 발명에 따른 방법으로 형성된 반도체 소자의 확산 방지막의 SEM 사진이다.

Figure 5(a) and Figure 5(b) are the SEM picture of the diffusion barrier of the semiconductor device formed into the conventional method and Figure 6(a) and Figure 6(b) are the SEM picture of the diffusion barrier of the semiconductor device formed into the method according to the present invention.

도 5(a)를 참조하면, 100Å의 티타늄층을 형성하고 200Å의 티타늄 나이트라이드층을 형성한 후 급속 열처리 공정을 실시하면 그레인 바운더리에서 티타늄 실리사이드의 덩어리가 형성된다. 이러한 상태에서 도 5(b)에서와 같이 890℃의 온도에서 1시간동안 열처리 공정을 실시하면 텅스텐 실리사이드층 하부에서 실리콘의 손실이 발생된다.

The titanium layer of 100Å is formed and if the rapid thermal processing is performed after doing the formation, the lump of the titanium silicide is formed with the titanium nitride layer of 200Å as the with reference to Figure 5(a) at the grain boundary. In this state, the loss of the silicone comes in the tungsten silicide layer lower part if the thermal process is performed Figure 5(b) at a temperature of 890℃ for 1 hour.

도 6(a)를 참조하면, 100Å의 티타늄층을 형성하고 급속 열질화 공정을 실시한 후 200Å의 티타늄 나이트라이드층을 형성하고 급속 열질화 공정을 실시한다. 이러한 공정에 의해 티타늄층과 티타늄 나이트라이드층 사이에 티타늄 실리사이드층과 티타늄 옥사이드층이 형성된다. 이러한 상태에서 도 6(b)에서와 같이 890℃의 온도에서 1시간동안 열공정을 실시하더라도

After the titanium layer of 100Å is formed and the rapid thermal nitridation is performed with reference to Figure 6(a) the titanium nitride layer of 200Å is formed and the rapid thermal nitridation is performed. By this process, the titanium silicide layer and titanium oxide layer are formed between the titanium layer and titanium nitride layer. In thi

균일한 막질을 얻을 수 있다.

s state, although the thermal process is performe d Figure 6(b) at a temperature of 890℃ for 1 hou r the uniform thin film can be obtained.

도면에 대한 간단한 설명

도 1(a) 내지 1(c)는 종래의 반도체 소자의 확산 방지막 형성 방법을 설명하기 위한 소자의 단면도.

도 2는 도 1(c)의 콘택홀 기저부를 확대한 도면.

도 3(a) 내지 3(c)는 본 발명에 따른 반도체 소자의 확산 방지막 형성 방법을 설명하기 위한 소자의 단면도.

도 4는 도 3(c)의 콘택홀 기저부를 확대한 도면.

도 5(a) 및 도 5(b)는 종래의 방법으로 형성된 반도체 소자의 확산 방지막의 SEM 사진.

도 6(a) 및 도 6(b)는 본 발명에 따른 방법으로 형성된 반도체 소자의 확산 방지막의 SEM 사진.

#60#도면의 주요 부분에 대한 부호 설명>

11 및 21 : 실리콘 기판 12 및 22 : 층간 절연막

13 및 24 : 티타늄(Ti)층
14, 23 및 24A : 티타늄 나이트라이드(TiN)층
15 및 25 : 티타늄 실리사이드(TiSi2)층

26 : 티타늄 옥사이드(TiO)층 17 및 27 : 텅스텐층

19 및 29 : 콘택홀

Brief explanation of the drawing

The cross-sectional view in which Figure 1(a) to 1 (c) illustrates the method for forming diffusing ba rrier layer of the conventional semiconductor devi ce of the device.

Fig. 2 is the magnificated drawing the contact hol e fundament of Figure 1(c).

The cross-sectional view in which Figure 3(a) to 3 (c) illustrates the method for forming diffusing ba rrier layer of the semiconductor device according to the present invention of the device.

Fig. 4 is the magnificated drawing the contact hol e fundament of Figure 3(c).

The SEM picture of the diffusion barrier of the se miconductor device in which Figure 5(a) and Figur e 5(b) are formed into the conventional method.

The SEM picture of the diffusion barrier of the se miconductor device in which Figure 6(a) and Figur e 6(b) are formed into the method according to th e present invention.

The code description > toward the main part of th e < drawing.

With 11 21: with the silicon substrate 12 22: inter -layer insulating film.

With 13 24: titanium (Ti) layer.
With 14, 23 24A: titanium nitride (TiN) layer.
With 15 25: titanium silicide (TiSi(SB)2(/SB)) laye r.

26: with the titanium oxide (TiO) layer 17 27: tun gsten layer.

With 19 29: contact hole.

Disclaimer

본 문서는 특허 및 과학기술문헌 전용의 첨단 자동번역 시스템을 이용해 생성되었습니다. 따라서 부분적으로 오역의 가능성이 있으며, 본 문서를 자격을 갖춘 전문 번역가에 의한 번역물을 대신하는 것으로 이용되어서는 안 됩니다. 시스템 및 네트워크의 특성때문에 발생한 오역과 부분 누락, 데이터의 불일치등에 대하여 본원은 법적인 책임을 지지 않습니다. 본 문서는 당사의 사전 동의 없이 권한이 없는 일반 대중을 위해 DB 및 시스템에 저장되어 재생, 복사, 배포될 수 없음을 알려드립니다.

(The document produced by using the high-tech machine translation system for t he patent and science & technology literature. Therefore, the document can inclu de the mistranslation, and it should not be used as a translation by a professional translator. We hold no legal liability for inconsistency of mistranslation, partial om ission, and data generated by feature of system and network. We would like to in form you that the document cannot be regenerated, copied, and distributed by b eing stored in DB and system for unauthorized general public without our consen t.)

Electronic Acknowledgement Receipt

EFS ID:	39743891
Application Number:	16506022
International Application Number:	
Confirmation Number:	3561
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC12
Receipt Date:	17-JUN-2020
Filing Date:	09-JUL-2019
Time Stamp:	13:29:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	DEFIVES.pdf	671506 25a9106674aaa31e12dfbcf59f86f9ec6ac58166	no	6

Warnings:

Information:					
2	Non Patent Literature	GOODNICK.pdf	1573492 46d1870face99d1e58eb86bcd2e3390072900df6	no	7
Warnings:					
Information:					
3	Non Patent Literature	SCHMIDT.pdf	1425624 0565b0f61ad0cd34186c81f31117a83741cc9e74	no	5
Warnings:					
Information:					
4	Non Patent Literature	WALDROP_1993.pdf	968557 005d5fa1dd1f3c0d8f5250d239b1833af59fb01f	no	4
Warnings:					
Information:					
5	Foreign Reference	EP0042066A2.pdf	558527 43f703cda929b2f2f64e72ec8ede9f10f8998fde	no	16
Warnings:					
Information:					
6	Foreign Reference	EP0068897A2.pdf	416249 17b9c4c2b3e4e39394020036bbb90b0835a61d58	no	14
Warnings:					
Information:					
7	Foreign Reference	EP0111364A2.pdf	1983067 cd380ec7c167183aeacb15297a7241758526a21a	no	40
Warnings:					
Information:					
8	Foreign Reference	EP0168125A1.pdf	569606 3e5eff2fcbde0fea998bbb881395f9ef37596970	no	19
Warnings:					
Information:					

9	Foreign Reference	EP0458353A2.pdf	904431 37db897ca4524a65c6f679b89d4de790076f14a6	no	18
Warnings:					
Information:					
10	Foreign Reference	EP0789388A2.pdf	1282294 65606bdba6cface1ceb160727591c428e9ab1af9	no	29
Warnings:					
Information:					
11	Foreign Reference	FR2814856A1.pdf	379015 50d7a637461b88daaf2839c97e08ad3795f5517c	no	15
Warnings:					
Information:					
12	Foreign Reference	GB1222594A.pdf	358782 6aae4389ae128febe8bc7926d3790945ff2d4971	no	4
Warnings:					
Information:					
13	Foreign Reference	JP2630279B2_wTransl.pdf	531353 9b41fb559e100ce6be1d85bde9d783ca45d83653	no	13
Warnings:					
Information:					
14	Foreign Reference	JP3191728B2_wTransl.pdf	616420 44ea4f2a041f708f95d04e72ed15e28cdb1f1c27	no	15
Warnings:					
Information:					
15	Foreign Reference	JP3208599B2_wTransl.pdf	858998 68f29ef54e29f680d72e4b6bd84ec271f13489a2	no	20
Warnings:					
Information:					

16	Foreign Reference	JP2000101064A_wTransl.pdf	834855 939efd0ff2b88e49345fce2ff20c6303a015aad1	no	27
Warnings:					
Information:					
17	Foreign Reference	JP2000101100A_wTransl.pdf	574167 9274b3a99da663877e09caa0e77aabb1c4a8da4b	no	12
Warnings:					
Information:					
18	Foreign Reference	JP2000174261A_wTransl.pdf	1261088 8d7143b2894362b0e897bb2ae74f57b6ad5ce4a1	no	39
Warnings:					
Information:					
19	Foreign Reference	JP2000195954A_wTransl.pdf	1081480 756cf6238b77fcc9723abefe961c456ddc4c23d8	no	23
Warnings:					
Information:					
20	Foreign Reference	JP2000216241A_wTransl.pdf	491553 adc0c3f6c84eb80d1a7ba0e72a4f8da52e85304e	no	16
Warnings:					
Information:					
21	Foreign Reference	JP2000228523A_wTransl.pdf	2305964 9095612453d723655371aca9e804489e105e6ee9	no	63
Warnings:					
Information:					
22	Foreign Reference	JP2000236086A_wTransl.pdf	1196865 4d5e6a4f35051e0aef3ed00c4df61e8f7916f096	no	38
Warnings:					
Information:					

23	Foreign Reference	JP2000299479A_wTransl.pdf	383714 3c559c0044bc007c36a6a294b3a03c110df35e8d	no	14
Warnings:					
Information:					
24	Foreign Reference	JP2001223180A_wTransl.pdf	1218680 d6a9ba97a4ae4854374046438589 26c9046496e4	no	26
Warnings:					
Information:					
25	Foreign Reference	JP2002075909A_wTransl.pdf	3167557 0eb95492823d76fd9e925d9d34513c2a2b4aa3c9	no	97
Warnings:					
Information:					
26	Foreign Reference	JP2002093742A_wTransl.pdf	3555722 21cd60891d680b4d4b322572748decd5ce292f67	no	104
Warnings:					
Information:					
27	Foreign Reference	JP2002151428A_wTransl.pdf	1430789 4445a832954313692019a5f0369dc66f6d0dbcb2	no	37
Warnings:					
Information:					
28	Foreign Reference	JP2002184978A_wTransl.pdf	816763 319b6300cf57389003f4d5c12e816d58b8282251	no	16
Warnings:					
Information:					
29	Foreign Reference	JP2002217425A_wTransl.pdf	2109496 d7549891cd2d4777c442ce9a032363e645170783	no	57
Warnings:					
Information:					

30	Foreign Reference	JPH065737B2_wTransl.pdf	275215 eba0fcc258446e69bc6f0722bfcafba580daa577	no	8
Warnings:					
Information:					
31	Foreign Reference	JPH0226073A_wTransl.pdf	1151045 1b7d5a7144a40cbdf19cc7fbe2616d05ee766d60	no	16
Warnings:					
Information:					
32	Foreign Reference	JPH0329355A_wTransl.pdf	486138 088d003523ac5d11a82a9ea1e1c693176d033bb4	no	8
Warnings:					
Information:					
33	Foreign Reference	JPH0653165A_wTransl.pdf	577246 adc3488994abd71a027033a8d978f3404ab4427a	no	18
Warnings:					
Information:					
34	Foreign Reference	JPH0661177A_wTransl.pdf	1298317 b007c17930a08495ffcc85774d5f0e8f3f76e54d	no	46
Warnings:					
Information:					
35	Foreign Reference	JPH0864800A_wTransl.pdf	586253 e8b93ae617aad375fba5921e90866fd8c454f347	no	21
Warnings:					
Information:					
36	Foreign Reference	JPH1027847A_wTransl.pdf	821422 c33f3bfa301a02380b8f065fc81fe4312574eb45	no	27
Warnings:					
Information:					

37	Foreign Reference	JPH1074707A_wTransl.pdf	1972077 8c920eca21dd844fef65623166aef7057e6309d4	no	53
Warnings:					
Information:					
38	Foreign Reference	JPH1126713A_wTransl.pdf	3325042 725f485590df56c25e40197f33d77bdd70a2b599	no	109
Warnings:					
Information:					
39	Foreign Reference	JPH01186672A_wTransl.pdf	523558 3c3cb696802f7b247ff138fd4c1fa6f8723b3927	no	9
Warnings:					
Information:					
40	Foreign Reference	JPH03191518A_wTransl.pdf	759112 10b02feff74b80fccb0dd7325a60023db3d478e2	no	11
Warnings:					
Information:					
41	Foreign Reference	JPH03274735A_wTransl.pdf	917832 60a6aab4d574a50fcf24270de2d923ccad178916	no	14
Warnings:					
Information:					
42	Foreign Reference	JPH04199628A_wTransl.pdf	548244 ffbfcb636ae88ff898d0cba30c98974fe3d57cb9	no	9
Warnings:					
Information:					
43	Foreign Reference	JPH04284668A_wTransl.pdf	715930 ae9326df46de3f7b5cf0662def15ad6f7a89f2f7	no	15
Warnings:					
Information:					

44	Foreign Reference	JPH07122519A_wTransl.pdf	1584073 6f9d94f8f2cd22ba78601a6780893ceda724bb28	no	49
Warnings:					
Information:					
45	Foreign Reference	JPH07263375A_wTransl.pdf	440891 f650391138c31a4eb7c8a2ac0994d9dd9c307d13	no	13
Warnings:					
Information:					
46	Foreign Reference	JPH08167693A_wTransl.pdf	873909 24a60362788f118b3f974ef819efb009146fca1f	no	27
Warnings:					
Information:					
47	Foreign Reference	JPH09289178A_wTransl.pdf	1918351 b27225f5a69b8031084fe8fb545cdce1cd54217d	no	59
Warnings:					
Information:					
48	Foreign Reference	JPH10135452A_wTransl.pdf	945024 d71ae689c3dfb21c506789a0bc5c31288d3cf367	no	29
Warnings:					
Information:					
49	Foreign Reference	JPH10209445A_wTransl.pdf	994893 b9b58d0ac1ae756f0f33f20735cccf4ff0fb8dce	no	32
Warnings:					
Information:					
50	Foreign Reference	JPH10335265A_wTransl.pdf	1080720 36f5d5a6425f639e882a46ad1c4c4face9fb0d1b	no	36
Warnings:					
Information:					

51	Foreign Reference	JPH11162874A_wTransl.pdf	426881 5d090ffef0b2b67b70219892e9dda60bb024139c	no	14
Warnings:					
Information:					
52	Foreign Reference	JPH11233760A_wTransl.pdf	432689 4ec06b57cdd056d7bf2f43d4eed38fd54207e5bf	no	14
Warnings:					
Information:					
53	Foreign Reference	JPH11330482A_wTransl.pdf	2260519 5969ef36898d301bd4d9f6dd898189c5b57f06ea	no	72
Warnings:					
Information:					
54	Foreign Reference	JPS6261363A_wTransl.pdf	1783040 48d5f14edc9b0dfa78cfd5353de89d3dab65e3a1	no	25
Warnings:					
Information:					
55	Foreign Reference	JPS61133646A_wTransl.pdf	686379 0df13241df08b3dce5252ff39b07d49895e6d85c	no	10
Warnings:					
Information:					
56	Foreign Reference	JPS63157466A_wTransl.pdf	704863 be15d6558dc853b2b65d416a0236b7647fbe23e8	no	11
Warnings:					
Information:					
57	Foreign Reference	JPS63175471A_wTransl.pdf	654824 e6b8d3def10ef49531938c0936c9a3606eda8a48	no	11
Warnings:					
Information:					

58	Foreign Reference	KR92002350B1_wTransl.pdf	1171826 31927ff947210fc31da6e647cf8da784408b0af6	no	28
Warnings:					
Information:					
59	Foreign Reference	KR100197653B1_wTransl.pdf	686822 6a23b90897979331a2ab3061d300f52c55939116	no	16
Warnings:					
Information:					
60	Foreign Reference	KR100290467B1_wTransl.pdf	406366 83a3f684f8e8dce22f08361216cd6442a485b4a8	no	19
Warnings:					
Information:					
			Total Files Size (in bytes):	64536115	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt

EFS ID:	39744509
Application Number:	16506022
International Application Number:	
Confirmation Number:	3561
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC12
Receipt Date:	17-JUN-2020
Filing Date:	09-JUL-2019
Time Stamp:	13:31:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	GROVE.pdf	1460828 f349a9dc49bc7b6c0d80c2d917b5e74b5e05fba0	no	19

Warnings:

Information:					
2	Non Patent Literature	GUO_IEEE.pdf	468473 46ed25d0b1435ee8aeb8dc3c3be562643d90fb0b	no	4
Warnings:					
Information:					
3	Non Patent Literature	GUO_Solid-State.pdf	439333 8d1ef66bedd71ccd5748f56615637ea5e2b7e493	no	5
Warnings:					
Information:					
4	Non Patent Literature	HARA_Applied_Surface_Sci.pdf	816686 1f79ca1ae84cf100cbe6beb13245fe7edccf767c	no	6
Warnings:					
Information:					
5	Non Patent Literature	HARA_Materials_Res.pdf	395249 96e47a99780a8f57a7b42c4a89b16c7cd626e352	no	6
Warnings:					
Information:					
6	Non Patent Literature	HARTSTEIN.pdf	739575 fe5b9e058c71b0b7b59b761789a1137b96defd57	no	6
Warnings:					
Information:					
7	Non Patent Literature	HASEGAWA_1993.pdf	352248 db81d91014c6f12be410b50e45da464e8a7dc034	no	4
Warnings:					
Information:					
8	Non Patent Literature	HASEGAWA_Intl_J.pdf	5419552 7c95ed157ec5d5e70c3fcfd59c851e06cd538a93	no	60
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					

Information:					
9	Non Patent Literature	HASEGAWA_JPN.pdf	1091463 2476a32708a707cb537ec8f9ed8c4d5383865cc2	no	6
Warnings:					
Information:					
10	Non Patent Literature	HASEGAWA_JVSTB.pdf	1940103 2f7231eae42072d9ef1b73018b72b8dbcd37ff4b	no	10
Warnings:					
Information:					
11	Non Patent Literature	HO.pdf	1012202 09aebbbdd902d4f257e98a8edfceb4e2c88e04ef	no	7
Warnings:					
Information:					
12	Non Patent Literature	HOFMANN.pdf	689936 88cb3aedebb10c660b4cfbc5b6d7322b0c9b7869	no	6
Warnings:					
Information:					
13	Non Patent Literature	HORIGUCHI.pdf	2411585 2e7d18f367cc188d27eb9c45a8669b0ddd84e647	no	5
Warnings:					
Information:					
14	Non Patent Literature	HORVATH.pdf	401147 d6617757e6c36a9cb8375ec2b9f54b3220d3543a	no	3
Warnings:					
Information:					
15	Non Patent Literature	HUDAIT.pdf	665875 85428b4cba2ae5852f9d24a1f14ef750a84105db	no	7
Warnings:					
Information:					

16	Non Patent Literature	HUI.pdf	355356 cb171d930d75127a6e81b22e88f2d63667b2f342	no	3
Warnings:					
Information:					
17	Non Patent Literature	ILDEREM.pdf	1155724 4bc853688d625a49479db4c3c5f7e11c27d4aed9	no	6
Warnings:					
Information:					
18	Non Patent Literature	INGERLY.pdf	484267 83016bc2f82e279d1334cbf40507b5973a1ac799	no	3
Warnings:					
Information:					
19	Non Patent Literature	ITOH.pdf	1278227 70f6dae3297a4e4f629651c1067696c160b44464	no	20
Warnings:					
Information:					
20	Non Patent Literature	ITRS.pdf	4869303 b346ec5e8c26ee1eef9ff2ea9393ab9deef1154c	no	51
Warnings:					
Information:					
21	Non Patent Literature	IVANCO_J_Appl_Phys.pdf	1483484 b4e3ed96d6b52cecea901de95da4385f9e808cde	no	7
Warnings:					
Information:					
22	Non Patent Literature	IVANCO_Solid-State.pdf	881703 0c03f47658fda077324cd072f381afdde53ec2ec	no	6
Warnings:					
Information:					

23	Non Patent Literature	IVANCO_Vacuum.pdf	818357 91794da6cd09c39a42850957fd8dc2409592675a	no	6
Warnings:					
Information:					
24	Non Patent Literature	IVY.pdf	1454770 a7e7310067faa0180d2a327c72ac28ad6edd6f65	no	11
Warnings:					
Information:					
25	Non Patent Literature	JACOBS.pdf	337671 c10d6fd7cea4658824f673eb9c0216d8d281f059	no	4
Warnings:					
Information:					
26	Non Patent Literature	KAR.pdf	1390478 f231217d84ebd4db2212678cffbe86015ee4d501	no	17
Warnings:					
Information:					
27	Non Patent Literature	KASAI.pdf	18742622 e99e198faa9b0db4e6e79c8cc47f037625315a50	no	309
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
28	Non Patent Literature	KEDZIERSKI.pdf	10738182 29fa0cf30f053ec022c9f85291e0acb5cca3a14f	no	134
Warnings:					
Information:					
29	Non Patent Literature	KIM.pdf	509015 899918145222e7a183d8bd6120878d47611708f7	no	4
Warnings:					
Information:					

30	Non Patent Literature	KIPPERMAN.pdf	754190 98193ed11a5869dcf6fda9134ad6a9041fcee01f	no	3
Warnings:					
Information:					
31	Non Patent Literature	KOBAYASHI.pdf	800048 64722eb61a9731f0d58ac101de31fbe620df0309	no	6
Warnings:					
Information:					
32	Non Patent Literature	KOLODZEY.pdf	1095359 0a226d24a6a2e88c1156f5796635cc6724457ef2	no	8
Warnings:					
Information:					
33	Non Patent Literature	LEBRASCA.pdf	1792763 4dad2e2454097a96fe103545a1e5b462acac95a8	no	7
Warnings:					
Information:					
34	Non Patent Literature	LEE_Applied_Phys_2289.pdf	1428042 96b3cf9fd7992ebd747e66dd8df8f55a49700680	no	5
Warnings:					
Information:					
35	Non Patent Literature	LEE_Applied_Phys_3143.pdf	899144 515008ce713f0b7e508cffe3843d877590510cd7	no	4
Warnings:					
Information:					
36	Non Patent Literature	LEE_Dissertation.pdf	4547287 13e44d4242d8fb7fa6c8ba9e66779491d2ba0479	no	106
Warnings:					
Information:					

37	Non Patent Literature	LEPRINCE-WANG.pdf	1278436 e19f40d09dc372c3c2871fec46842893ce4cc681	no	7
Warnings:					
Information:					
38	Non Patent Literature	LEVY.pdf	10211652 eceb7da0443b9b5990b27a2600fb1c965d017a8e	no	8
Warnings:					
Information:					
39	Non Patent Literature	LIAUH.pdf	2057297 e8ef4259288d2f33f1d20b82094d0ab9e0eee70d	no	9
Warnings:					
Information:					
40	Non Patent Literature	LILLINGTON.pdf	763314 cafa44bfa8431158138532b8903af8edb0f58cfd	no	3
Warnings:					
Information:					
41	Non Patent Literature	LIN_APPLIED.pdf	403970 9826a9e84188d262c2460c6549a3157dd1d7c64c	no	3
Warnings:					
Information:					
42	Non Patent Literature	LIN_SEMICON.pdf	4560623 bc2518bd8ee881ba89221e7353dfc4245eff5301	no	6
Warnings:					
Information:					
43	Non Patent Literature	LOOK.pdf	977356 357a4152c48c6b7857971bb6670d9c995373e670	no	4
Warnings:					
Information:					

44	Non Patent Literature	LUCOVSKY.pdf	1380308 1b0c49c702c29f51838b881f1124c9e51090827f	no	12
Warnings:					
Information:					
45	Non Patent Literature	LUE.pdf	1884131 68d420b67b4afd0a517dd3d70d1e16c5b371c8e7	no	9
Warnings:					
Information:					
46	Non Patent Literature	LUTHER.pdf	1289788 10ae0407dbaa2515f21bc9e58764c24012860739	no	4
Warnings:					
Information:					
47	Non Patent Literature	MAEDA.pdf	1819533 97dfb4377a76a83461cc39aa6bafb5daacfe525e	no	8
Warnings:					
Information:					
48	Non Patent Literature	MAHALINGAM.pdf	16283636 8b94f1fd27fc8df6d6707a60ef681fbf84175b52	no	295
Warnings:					
Information:					
49	Non Patent Literature	MAMOR.pdf	1269031 40e37b5dbb630517f26faa85fd44ab27849a6f29	no	10
Warnings:					
Information:					
50	Non Patent Literature	MARINOVA.pdf	500257 85f5123ab8c367b83a69324489cc59faf41e9f9b	no	4
Warnings:					
Information:					

51	Non Patent Literature	MATSUZAWA.pdf	666996 dbde3fbb152700f558e6776674fc681ccdb1d37a	no	6
Warnings:					
Information:					
52	Non Patent Literature	MILLER.pdf	914204 29e7795beecd8ca45a10718f89b99ed1791ff0eb	no	6
Warnings:					
Information:					
53	Non Patent Literature	MONCH.pdf	1131925 28a2debc45ce0420da1c31a244c1930139cc70d4	no	9
Warnings:					
Information:					
54	Non Patent Literature	MORITA.pdf	2179316 46a09f5b75aec8445adff6c5f7861716a15cfb5d	no	11
Warnings:					
Information:					
55	Non Patent Literature	MURET.pdf	1187245 8c23c42d36924d5e7c0c0d13dc11458a3b9a67b5	no	5
Warnings:					
Information:					
56	Non Patent Literature	NAKASAKI.pdf	1801962 92a0ed6e3b13fcc66a2500d3e4a71043f6031b5f	no	7
Warnings:					
Information:					
57	Non Patent Literature	NIELSEN_127.pdf	783637 0e68bf4267578e08e1cb684b2cfa11d8543c4a1f	no	7
Warnings:					
Information:					

58	Non Patent Literature	NIELSEN_129.pdf	390911 3cebd91d659bdc6c16999cf944c41fcf330910a3	no	4
Warnings:					
Information:					
59	Non Patent Literature	ODONNELL.pdf	357983 247fd1e624772241e010ce16feb1e323a34623a01	no	3
Warnings:					
Information:					
60	Non Patent Literature	OKADA.pdf	707872 7d0373e5f1e5de5279a1fa8cb880b41ebc158dbf	no	4
Warnings:					
Information:					
			Total Files Size (in bytes):	128921630	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

(19) 대한민국특허청(KR)
(12) 특허공보(B1)

(51) Int. Cl.[5]
H01L 29/78

(45) 공고일자 1991년08월17일
(11) 공고번호 특1991-0006249

(21) 출원번호	특1984-0001637	(65) 공개번호	특1984-0008537
(22) 출원일자	1984년03월29일	(43) 공개일자	1984년12월15일

(30) 우선권주장 58-55075 1983년04월01일 일본(JP)
58-121185 1983년07월04일 일본(JP)

(71) 출원인 가부시기가이샤 히다찌세이사꾸쇼 미쓰다 가쓰시게
일본국 도오교도 지요다구 간다 스루가다이 4-6

(72) 발명자 호리우지 마사다타
일본국 도오교도 고가네이시 스구이미나미쵸 5-13-7
야마구지 겐
일본국 도오교도 히가시구루메시 마에자와 2-5-12

(74) 대리인 백낭기

심사관 : 김원국 (현자공보 제2677호)

(54) 반도체 장치

요약

내용 없음.

대표도

도1

명세서

[발명의 명칭]

반도체 장치

[도면의 간단한 설명]

제1도는 종래의 CMOS를 도시한 단면도.

제2도는 A는 종래의 이중 드레인 구조를 갖는 MISFET의 단면도.

제3도는 BSMS 제2도의 A의 MISFET의 반도체 표면의 불순물농도 분포와 그에 있어서의 전계를 해석한 것은 도시한 도면.

제3도~제6도는 본 발명의 제1의 실시에의 제조 공정을 순으로 도시한 단면도.

제7도는 본 발명의 제2의 실시에의 단면도.

제8도는 본 발명의 제3의 실시에의 단면도.

제9도는 본발명의 제1의 실시에의 특성을 도시한 도면.

제10도는 본 발명의 제4의 실시예의 단면도.

제11도는 본 발명의 제5의 실시예의 단면도.

제12도는 본 발명의 제6의 실시예의 단면도.

제13도, 제14도는 본 발명의 제7~제9의 실시에의 특성을 표시한 도면.

제15도~제17도는 본 발명의 제7의 실시에를 제조 공정 순서로 도시한 단면도.

제18도~제19도는 본 발명의 제8의 실시에를 제조 공정 순서로 도시한 단면도.

제20도는 본 발명의 제9의 실시예의 단면도.

제21도는 본 발명의 제9의 실시예의 드레인의 깊이 방향의 불순물 농도 분포를 도시한 도면.

GF Exhibit 1124 - 1879/2704

[발명의 상세한 설명]

본 발명은 MISFET에 관하여, 특히 초미세 MISFET의 고내압화에 가장 적합하고, 내 핫 캐리어 효과가 우수한 MISFET에 관한 것이다.

또한, 본 발명은 CMOSFET에 관하여, 특히 0.5㎛ 이하의 게이트 길이에 있어서도 5V 전원으로 동작가능한 고내압초미세 CMOSFET에 관한 것이다.

현재, MIS 전계 효과 트랜지스터(이하MISFET라 한다)는 미세화를 위해 게이트 절연막을 얇게 하여, 소오스와 드레인의 간격을 좁게하고, 또한 소오스와 드레인의 접합을 얇게 하려고 하고 있다.

상기의 경향의 결과, 현재의 MISFET에 있어서의 최대의 문제는 소오스와 드레인 사이의 내압의 저하이다. 드레인 측에서 신장해온 공핍층이 소오스 영역에 도달하기 때문에 생긴 소위, 펀치 스루 내압의 저하는 기판 농도를 증가하는 것에 의해 피할 수가 있으나, 그와 같이 하는 것에 의해서 역으로 전자사태 항복내압(avalanche effect break down)이 감소하게 된다. 특히, 게이트, 소오스 및 기판 전압을 영으로 하였을때의 전자사태 항복전압(이하, BV_{DS}라 한다)은 게이트 전압에 의해서 기판표면 전위의 증가가 억제되기 때문에 젖합 내압에비해서 극단으로 저하해 버린다. 그 결과, 찬넬 길이 1㎛, 게이트 산화막의 두께20nm, 소오스 드레인 접합 깊이 0.35㎛인 미세 MISFET의 소오스와 드레인 사이의 내압은 약6V로 통상의 전원 전압5V에 거의 일치할때까지 저하한다. 상기와 같이 미세 트랜지스터에 있어서는 전원 전압의 변동에 의해 간단히 파괴된다.

따라서, 종래의 미세 MISFET에 있어서는 상기의 결점을 극복하기 위해 드레인 구조에 관하여 0.2㎛ 정도의 얇은 접합 깊이를 갖는 고농도 불순물 확산층과 0.35㎛ 정도의 보다 깊은 접합깊이를 갖는 저농도 불순물확산층을 조합시키는 소위, 이중 드레인 구조를 채용하고 있다. 상기 구조에의 BV_{DS}값을 약 1.5내지 2V 향상시킬 수가 있다. 그러나, 상기의 개량된 미세 MISFET에 있어서는 전원 전압의 변동에 의한 파괴로부터 통상 피할 수가 있다. 그러나, 상기의 개량된 미세MISFET에 있어서도 신뢰성의 관점에서는 아직까지 만족할 수가 없었다.

즉, 통상 조건의 장기간 동작에 있어서는 드레인 근방에 있어서의 강한 전계 효과에 의해 핫 케리어(hot carrier)가 게이트 절연막중에 주입되어 임계 전압 값의 변동, 또 표면준의 밀도의 증대 및 전달 콘덕턴스의 저항 등의 열화가 생긴다.

또, 이상은 MISFET의 단일체에 관한 것이지만, 2개 이상의 트랜지스터를 조합해서 구성한 CMOS(Complementary Metal Oxide Semiconductor) 구조에 있어서도 대략 마찬가지로 적용된다. 또, CMOS에서는 다음의 문제도 갖고 있다.

여기서, CMOS는 P 찬넬 MOS(이하 PMOS라 한다)와 N 찬넬 MOS(이하 NMOS라 한다)를 쌍으로 해서 동일칩위에 형성하고 있는 구조이다.

제1도는 2㎛ 이상의 게이트 길이를 갖는 종래의 CMOS의 단면 구조도이다.

제1도에 있어서 (21)은 N 도전형의 반도체 기판, (22)는 반도체 기판(21)내에 형성된 P 도전형의 확산층 영역으로 웰이라 한다. (23)은 필드 산화막, (24) 및 (25)는 웰(22)내에 형성된 NMOS의 소오스 및 드레인 확산층 영역으로 n 도전형을 가지며, 그 최대 불순물 농도는 $10^{20}cm^{-3}$이상으로 구성된다. (26) 및 (27)은 PMOS의 소오스 및 드레인 확산층 영역으로 P 도전형을 가지며, 그 최대 불순물 농도는 $10^{19}cm^{-3}$이상으로 구성된다. (28) 및 (29)는 각각 게이트 절연막 및 게이트 전극이다. (210) 및 (211)은 각각 보호절연막 및 소오스 또는 드레인 전극이다.

이와 같은 드레인 확산층의 불순물농도 구성을 갖는 종래 구조의 CMOS에 있어서는 소자의 미소화에 따라서 여러 가지의 결점이 발생한다.

(i) 소오스와 드레인 사이의 내압 저하, 즉 소자가 미소화 되는데 따라 찬넬 길이가 감소하기 때문에 펀치 스루 내압이 저하한다. 펀치 스루 내압의 향상은 기판 농도를 증가하는 것에 의해 달성할 수 있으나, 기판 농도의 증가는 역으로 전자사태 항복 내압이 저하하여 버린다. 찬넬 길이가 0.3㎛ 이하의 매우 미소한 NMOS에 있어서는 소오스와 드레인 사이의 내압이 2V이하로 현저하게 저하하기 때문에 통상의 전원 전압의 5V로서는 동작이 불가능하다.

그리고, 펀치 수루 내압의 향상을 위해서 기판 농도를 증가하면, 찬넬 콘덕턴스 gm의 감소를 수반하기 때문에 MISFET이 미세화에 의해 얻어지는 고속 동작 특성은 저해된다.

(ii) 래치 업에 의한 MISFET의 파괴, 즉 종래 구조를 갖는 CMOSFET의 최대의 결점은 래치업이라고 부르는 사이리스터(thyristor) 동작에 기인하는 MISFET의 파괴이다. 이 래치 업 현상은 특히 CMOSFET의 미세화에 따라서 현저하게 된다. 즉, NMOS와 PMOS사이의 거리가 근접된 CMOSFET에 있어서는 NMOS의 드레인(25), 웰(22),반도체 기판(21) 및 PMOS의 소오스(26) 또는 드레인 (27)사이에 NPNP 구조를 갖는 기생 사이리스터가 형성된다. 상기의 사이리스터는 과전압의 인가, 통상 스위치 동작중의 내부과도적 과전압의 발생, 또는 광이나 방사선의 조사에 기인하는 소수 캐리어의 유기 등에 의해 유발되어 동작을 개시하고 전원을 정지할때까지 사이리스터 동작을 억제하는 것은 불가능하게 된다. 이 사이리스터 동작에 기인하여 과대 전류가 CMOSFET에 흐르기 때문에 CMOSFET는 파괴된다.

상기의 사이리스터 동작은 CMOSFET의 미세화에 따라서 웰(22)와 PMOS의 간격이 축소되어 기생 PNP 바이폴라 트랜지스터 및 기생 NPN 바이폴라 트랜지스터의 각각의 전류 이득률의 곱이 1보다 크게 되기 때문에 발생한다는 것이 알려져 있다.

상기의 각 기생 바이폴라 트랜지스터에 있어서의 전류 이득률의 곱을 갖게 하는 것에 의해 사이리스터 동작을 저지하는 방법이 제안되고 있다. 즉, P+N 접합으로 형성된 제1도에 도시한 종래 구조 PMS0의 소

GF Exhibit 1124 - 1880/2704

오스(26) 및 드레인(27)을 쇼트기 접합로 치환한 CMOSFET 구조가 1982년도 국제 전자 장치 학회(International Electron Devices Meeting) 에고집 462페이지에 기재되어 있다. 상기의 "쇼트키 장벽 PMOS에 의한 CMOS 래치 업 현상의 해결(CMOS latch-up elimination using schottky barrier PMOS)"라고 하는 보고서에서는 쇼트키 접합에 있어서의 소수 캐리어 주입 효율이 P+N접합의 것과 비교해서 대단히 작은 사실을 이용해서 기생 PNP 바이폴라 트랜지스터의 전류 이득률을 P+N 접합에 의한 종래 구조의 것과 비교해서 1/100 이하로 까지 저하시키는 것에 의해 래치 업 현상을 해결하고 있다.

P+N 접합대신에 쇼트키 접합으로 소오스 접합 및 드레인 접합을 형성하는 상기의 CMOSFET에 있어서 래치 업 현상은 방지되지만, 쇼트키 접합 특유의 결점이 존재한다. 즉, 쇼트키 접합을 사용한 CMOSFET에 있어서는 드레인 접합누설 전류가 큰 것, 비선형 출력으로 되어 옴접촉 특성을 얻을 수 없는 것 및 전달 콘덕턴스가 낮기 때문에 충분한 전류가 확보되지 않아 고속 동작을할 수 없는 것 등의여러 가지의 결점이 있다.

쇼트키 접합에 따른 상기의 결점은 그후 제한된 "저농도 불순물 확산을행한 쇼트키 트랜지스터(blightly doped schottky MOSFET)"에 의해 해결할 수가 있다. (1982년도 국제 전자 장치 학회 에고집, 466페이지 참조). 즉, 상기 쇼트키 트랜지스터에 있어서는 낮은 불순물 분포의 드레인 영역 위에 쇼트키 접합을 형성하면, 드레인 접합의 누설 전류가 작게할 수가 있고, 또한 전달 콘덕턴스도 통상 구조의 PMOS의 그것에 가깝게 할 수가 있다.

그러나, 낮은 불순물 농도 드레인 확산층과 쇼트키 접합을 조합시킨 구조에 의해 CMOSFET를 구성하는 방법에도 다음과 같은 결점이 존재한다. 즉, 상기의 문헌 "CMOS latch-up elimination using schottky barrier PMOS"에도 기재되어 있는 바와 같이 NMOS의 소오스 접합 및 드레인 접합을 쇼트키 접합으로 형성한 경우에 있어서의 기생 NPN 바이폴라 트랜지스터의 전류 이득률은 N+P 접합에 의해 드레인 접합을 형성한 종래 구조에 있어서의 기생 NPN 바이폴라 트랜지스터의 전류 이득률에 비해서 최대 10배나 크게 되는 것이다. 이에 따르면, 낮은 불순물 농도를 갖는 드레인 확산층의 유무에 관계없이 쇼트키 접합으로 PMOS 및 NMOS를 형성한 CMOS 트랜지스터는 PMOS의 소오스 접합 및 드레인 접합을 쇼트키접합으로 형성하고, NMOS의 각 접합은 통상의 N+P접합으로 형성한 CMOS트랜지스터보다 래치 업 현상이 생기기 쉽다는 결점이 있다.

쇼트키 접합에 의한 래치 방지에 관한 상기 2건의 문헌에 의하면, 낮은 불순물 농도 분포를 갖는 소오스 영역 및 드레인 영역의 각 표면에 쇼트키 장벽을 형성한 PMOS와 옹상의 높은 불순물 농도를 갖는 소오스 확산층 및 드레인 확산층이 형성된 NMSO의 조합에 의해 CMOS 트랜지스터를 구성하는 것이 래치업방지의 관점에서 가장 바람직한 것이된다.

그러나 , 상기 2건의 문헌 및 그들의 조합에 의해 얻어지는 결론은 CMOS 트랜지스터의 래치 업 방지의 관점에서만 성립하는 것으로서 CMOS 트랜지스터의 미세화에 따른 NMOS 및 PMOS의 내압 저하에 관한 상술한 결점에 대해서는 아무런 해결 방법도 제안되어 있지 않았다.

특히 , 찬넬길이가 0.5㎛이하의 초미세 CMOS 트랜지스터에 관해서는 상기 2건의 문헌에는 아무런 기재도 없고, 상술의 결점에 대해서는 전혀 해결 방법이 없다.

본 발명의 목적은 소오스와 드레인 사이의 내압이 통상의 전원 전압에 비해 충분히 높고, 핫 케리어 주입에 따라 특성 열화가 생기지 않는 초미세 MISFET를 제공하는데 있다.

본 발명의 다른 목적은 상기와 같은 종래의 결점을 해소하고, 극히 짧은 찬넬 길이로도 통상의 전원 전압으로 동작하고, 또한 래치 업 현상도 방지할 수 있는 CMOSFET를 제공하는데 있다.

본 발명은 종래의 이중드레인 구조의 가장 적합한 조건의 검토에 있어서, 특히 얕은 접합깊이를 갖는 고농도 불순물분포 영역이 완수하는 역할에 착안하여 해석한 결과에 기인한다. 제2도 A는 종래하여금 이중 드레인 구조를 갖는 MISFET의 단면도이다. 제2도 A에 있어서 (1)은 P형 반도체 기판, (2)는 필드 산화막, (2)은 게이트 산화막, (5)~(8)은 게이트 전극(4)를 확산 마스크로서 형성한 n형 불순물 영역으로 (5) 및 (7)은 드레인 확산층 (6) 및 (8)은 소오스 확산층이다. 여기서 (5) 및 (6)은 낮은 불순물 농도 확산층이며, 표면 불순물 농도를 Cs_2, 접합 깊이를 Xj_2로 정의한다. (7) 및 (8)은 높은 불순물 농도 확산층이며, 표면 불순물 농도를 Cs_1, 접합 깊이를 Xj_1로 정의한다. (9) 및 (10)은 각각 드레인 전극, 소오스 전극이다. 제2도 B는 제2도 A의 MISFET의 반도체 표면에 있어서 드레인 확산층 끝에서 소오스 확산층 측으로의 거리의 함수로서의 불순물 농도 분포가 거기에 있어서의 전계를 해석한 대표적인 결과다. 제2도 B는 실효 찬넬 길이가 1.1㎛, 게이트 산화막(3)의 막의 두께가 20nm, Xj_1이 0.25㎛, Xj_2가 0.3㎛, Cs_1이 $1\times10^{21}cm^{-3}$, $Cs_2\times10^{19}cm^{-3}$의 경우이고, 게이트 전극(4) 및 드레인 전극(9)에 인가한 전압은 각각 0V 및 10V이다.

제2도 B에서 명확한 바와 같이 드레인 전압의 인가에 의해 반도체 표면에 있어서, 최대 전계는 불순물농도가 $10^{18}cm^{-3}$부근에 있어서의 드레인 확산층 내부에서 형성되고, 불순물 농도가 보다 높은 드레인 확산층(7)내에서는 전계가 보다 작게 되어 가는 것을 알 수 있다. 본 발명은 이러한 해석 결과, 높은 불순물 농도 확산층(7) 내에 있어서하여금 전계가 보다 작게 되어 가는 것을 알 수 있다. 본 발명은 이러한 해석 결과, 높은 불순물농도 확산층(7)내에 있어서의 전계의 급격한 저하 경향에 착안한 것에 기안한다.

즉, 상기의 결과는 종래의 이중 드레인 구조의 MISFET에 있어서 상기 영역(7)이고, 내압화에 관해 거의 기여하고 있지 않다고 생각할 수 있다. 상기 개념에 따르면, 미세 MISFET의 고내압화의 관점에서 높은 불순물 농도 확산층의 존재는 도리어 장해로 되고 있으며, 드레인 확산층을 낮은 불순물 농도 확산층으로 구성하는 것이 바람직하다고 생각된다.

그러나 , 상기의 개념은 종래에 실시되어 있지 않는다. 이것은 종래의 드레인 확산층이 높은 불순물 농도 확산층으로 구성되는 것이라는 고정 개념에서 벗어나지 못했기 때문이고, 따라서 이중 드레인 구조에

GF Exhibit 1124 - 1881/2704

있어서도 높은 불순물 농도 확산층의 존재는 불가피하다라고 생각하였기 때문이다.

상기의 관점에 따라서 이중 드레인 구조에 있어서의 높은 불순물 농도 확산층(7) 및 (8)의 역할을 보면, 상기 영역(7) 및 (8)은 단지 전극(9) 및 (10)과의 옴접촉의 확보 및 소오스 및 드레인 영역의 확산층 저항의 저감화 이외는 아무런 역할에서도 하고 있지 않는 것은 명확하다. 한편, 소오스 및 드레인 영역의 확산층저항에 관해서는 백금 등의 실리사이드를 확산층 위에 형성하는 종래 기술에 의해 통상의 높은 불순물 농도확산층에 의한 시이트 저항값 50Ω/cm^3를 3!&/cm^2이하의 1/10 이하로 까지 저감화 할 수 있는 것이 알려져 있다. 그러나, 상기의 실리사이드 드레인 구조에 있어서는 시이트 저항의 저감 효과에만 착안하고, 소오스와 드레인 사이의 내압의 향상의 관점에서의 검토는 종래에 있어서 행하여지지 않아 드레인 확산층에는 고정 개념에 따라서 $10^{20}cm^{-3}$이상의 표면 농도를 갖는 높은 불순물 확산층이 사용되어 왔다.

본발명은 상기의 고정 개념이 무의미한 것이며, 드레인 확산층, 불순물 분포의 최적화에 의해 소오스 및 드레인 내압의 고내압화와 드레인 전극, 드레인 확산층사이의 양호한 옴접촉, 더 나아가서는 낮은 시이트저항화가 가능하게 된다고 생각하고, 검토한 결과에 따른 즉, 본 발명은 실리사이드 층을 형성하여야 할 드레인 확산층의 표면농도가 $10^{18}cm^{-3}$이상이면, 실리사이드 층 바로 아래에 표면농도가 $10^{19}cm^{-3}$정도의 석출층이 10nm 정도 형성되어 실리사이드와 드레인 확산층 사이에 MISFET의 통상동작에 충분한 옴접촉이 확보되는 사실을 발견한 것에 따른다. 또 본 발명은 상기 드레인 확산층의 표면 농도가 $10^{20}cm^{-3}$이하이면, 소오스와 드레인 사이의 내압을 실효 찬넬 길이 1μm 이하의 MISFET에 있어서도 최대 5V 이상 종래의 MISFET에 비해서 고내압화 할 수 있는 것을 발견한 사실에 따른다.

본 발명에 의한 CMOSFET는 불순물 확산 영역의 최대 불순물 농도가 10^{18}~$10^{20}cm^{-3}$정도의 N형드레인 영역과 최대 불순물 농도가 10^{17}~$10^{19}cm^{-3}$정도의 P형 드레인 영역을 가지며, 또한 상기 각 드레인 영역의 적어도 일부가 고용점 금속 또는 상기 금속의 실리사이드 층과 접합되어 구성되어 있는 것에 특징이 있다.

다음에 본 발명을 실시예에 따라서 더욱 상세하게 설명한다. 설명의 편의상, 도면을 가지고 설명하지만 주요부를 확대하여 도시하고 있으므로 주의를 한다.

[실시예 1]

제3도~제6도는 본 발명에 의한 MISFET하여금 1실시예의 제조 공정을 공정 순서로 도시한 도면으로서, (1)은 P도전형 비저항 1Ω/cm의 실리콘 기판이다. 반도체 기판(1)표면에 종래의 소자 분리 기술을 이용해서 0.8μm의 두꺼운 필드 산화막(2)를 선택적으로 형성한 후, 활성 영역의 반도체 표면을 노출하고, 20nm의 깨끗한 게이트 산화막(3)을 형성한다. 그후, 약 0.3μm하여금 실리콘 박막을 게이트 산화막(3) 위에 형성하고, $POCl_3$을 소오스로 하는 열 확산에 의해 실리콘박막에 인(p)의 고농도 확산을 행한다.

그 후에, 리도그래피에 의해 게이트 전극(4)를 형성한다. 리도그래피후의 찬넬 길이는 1μm이다. 다음에 테트라에록시실란 ($Si(OC_2H_5)_4$)을 사용한 화학 기상반응에 의해 0.5μm의 막의 두께를 갖는 실리콘 산화막(11)을 전면으로 퇴적시킨다. 상기의 퇴적막(11)을 반응성 스퍼터 에칭에 의해 최대기판 표면과 수직 방향으로 에칭을 행하여 평탄부에 퇴적된 실리콘 산화막을 제거하면, 제4도에 도시한 바와 같이 게이트 전극(4)의 측벽에만 실리콘 산화막(11)이 남게된다. 이 상태에서 산화막(3)을거쳐서 비소를 가속에너지70 KeV의 조건에서 이온 주입에 의해 반도체 기판(1) 표면에 주입한다. 상기의 조건은 최대 기판 표면에서 최대 불순물 농도로 되는 조건이다. 본 실시예에 있어서는 주입량을 변수로 하고, 표면 불순물 농도가 1×10^{17}~$10^{19}cm^{-3}$의 범위에서 여러 가지의 값을취할 수 있도록 다수개의 MISFET를 작성하였다. 상기의 이온주입 공정후 주입 이온의 활성화의 열처리를 행하였다.

상기의 열처리는 1000℃에서 행하였지만, 여러가지의 주입량을 갖는 각각의 MISFET에 대해 접합깊이 Xj가 0.25μm로 되도록 각각 열처리 시간을 설정하였다. 그후, 드레인 확산층(5) 및 소오스 확산층(6) 위의 게이트 산화막(3)을 제거하고, 50nm의 막의 두께의 백금(Pt)를 전면에 스퍼터링법에 의해 증착한다. 다음에 450℃의 열처리를 하고, 드레인(5), 소오스 확산층(6) 표면 및 게이트 전극(4)표면에 백금 실리사이드(PtSi)(12)를 형성한다.

상기의 열처리에 있어서 산화막(11) 및 (2) 위에서는 실리콘과의 반응은 일어나지 않아 실리사이드는 형성되지 않는다. 따라서 상기 열처리 공정후, 왕수로 에칭하면 PtSi는 왕수로 에칭되지 않기 때문에 산화막 및 반응하지 않는 Pt만이 제거되고, 게이트 전극(4), 드레인 확산층 (5) 침소오스 확산층(6)의 각 표면에 위에만 PtSi가 자기 정합적으로 남게 된다. 여기에 있어서 PtSi 층(12) 바로 아래에는 PtSi 층 형성전의 표면 불순물 농도 보다도 1자리수 높은 불순물 농도를 갖는 약 10nm두께의 석출층(13)이 PtSi 층(12)와 자기 정합적으로 형성되었다. 상기 석출층(13)내에 있어서의 깊이 방향의 불순물 분포는 깊이에 대해 아래로 볼록한 형상을 갖는다. PtSi 층 (12)의 형성 후, 공지의 기술을 사용해서 보호 절연막(15), 또 드레인 전극(9) 및 소오스 전극(10)을포함하는 배선전극을 바라는 회로 방식에 따라서 형성한다. 상기의 전극(9)(10)에는 알루미늄(Al)의 증착만을 사용하지만, Al이 PtSi 층 (12)와 반응하는 것을 방지하기 위하여 A1배선 공정전에 Ti와 Ta의 동시 스퍼터링에 의해 TiTa 막(14)를 PtSi 막(12)위의 접촉구멍 부분에 사전에 형성한다.

상기의 제조 과정을 거쳐서 제조된 각종의 표면 불순물 농도 Cs_2를 갖는 드레인 확산층(5)로 구성된 각각의 MISFET의 게이트 전압이 영에서 소오스와 드레인 사이의 내압 BV_{DS}를 측정하였을 때, 제9도의 결과가 얻어졌다. 제9도의 측정에 사용한 각 MISFET는 본 실시예의 제조 과정에서도 명확한 바와 같이 실효찬넬 길이가 1μm 게이트 산화막(3)의 막의 두께가 20nm, 드레인 접합 깊이 0.25μm의 동일 조건의 것이고, 드레인 확산층(5)의 표면 불순물 농도만이 달라지고 있다. 본 실시예의 각 MISFET에 있어서는 드레인 접합끝이 게이트 전극(4)의 끝과 일치하도록 게이트 측벽 산화막(11)의 막하여금 두께를 제어하고 있

GF Exhibit 1124 - 1882/2704

다. 제9도의 결과로 주목되는 것은 드레인 확산층(5)의 표면 불순물 농도가 $5\times10^{18}cm^{-3}$부근에서 BV_{DS}값이 최대로 되어 11.5V에 까지 도달하는 것이다.

상기의 값은 표면 불순물 농도가 $10^{20}cm^{-3}$이상의 드레인으로 구성되는 동일 접합 깊이를 갖는 종래 MISFET의 BV_{DS}값보다 4.5V 이상이나 높은 내압화가 실현되어 있는 것을 나타내고 있다. 또, 제9도에 있어서 점선으로 표시한 종래의 이중 드레인 구조 MISFET에 있어서 BV_{DS}값의 최대값보다도 본 발명에 의한 MISFET의 쪽이 3.5V 이상이나 높은 내압화가 실현되어 있는 것을 나타내고 있다.

그리고, 제9도에 도시한 이중 드레인 구조의 특성은 낮은 불순물 농도 분포(5)의 접합 깊이 Xj_2가 0.25 μm, 표면 불순물 농도 Cs_2는 도시한 각각의 값이고, 높은 불순물농도 분포 (7)의 접합 깊이 Xj_1이 0.15 μm, 표면 불순물 농도 Cs_1은 $1\times10^{21}cm^{-3}$의 구성으로 되는 드레인 확산층을 갖는 MISFET에 관한 것이다. 여기에서 게이트 산화막(3)의 막 두께는 20nm, 실효 찬넬 길이는 1μm이다.

본 실시예에 따라서 제조한 MISFET에 있어서의 전류 전압 특성을 상세하게 검토하였으나, 드레인(5) 및 소오스 확산층(6)의 표면 불순물 농도가 $1\times10^{18}cm^{-3}$ 이상으로 구성된 MISFET에 있어서는 전류의 상승 특성에 쇼트키 성분이나 큰 직렬 저항 등이 발견되지 않고, 양호한 옴접촉이 드레인(5) 및 소오스 확산층(6)과 백금 실리사이드(12) 사이가 얻어지고 있는 것이 명확하게 되었다. 본실시예에 따라서 제조된 MISFET에 관한 상기 측정결과에서 드레인 확산층(5)의 표면 불순물 농도로 $10^{18}cm^{-3}$이상$10^{20}cm^{-3}$ 미만인 것이 소오스 드레인 내압의 고내압화의 관점 및 양호한 음접촉의 관점에서 바람직하고, 특히 $5\times10^{18}cm^{-3}$ 정도인 것이 바람직하다. 상기의 조건에서 드레인 확산층이 구성된 본 발명에 의한 MISFET에 있어서는 종래의 동일치수의 미세 MISFET에 비해서 BV_{DS} 값에서 3.5V 이상의 고내압비가 실현되고, 또한 양호한 옴접촉도 확보할 수가 있었다. 상기의 양호한 옴접촉은 낮은 불순물 농도 표면으로서 실리사이드 형성시에 실리사이드층 (12) 바로 아래에 매우 얇은 높은 불순물 농도 석출층(13)이 동시에 형성되기 때문이라고 생각된다.

본발명에 따라서 구성된 MISFET에 있어서는 종래의 실리사이드 드레인 구조를 갖는 MISFET와 마찬가지로 $3\Omega/cm^2$ 의 낮은 시이트 저항을 확보할 수가 있었다.

[실시예 2]

제7도는 본발명의 다른 실시예를 도시한 도면이며, 상기 제1의 실시예에 있어서 게이트 측벽 산화막(11)의 막의 두께를 얇게 하고, 드레인 접합 끝이 게이트 전극(4)아래에 존재하도록 구성하여 MISFET를 작성하였다.

상기 구성에 있어서는 드레인 확산층(5)의 낮은 불순물 농도 영역의 대부분 이 게이트 인가 전압에 의해 제어되는 것이 가능하게 된다. 실효 찬넬 길이 1μm, 소오스와 드레인의 각 적합 깊이 0.25μm 및 게이트 산화막의 두께 20nm등 MISFET의 구조 파라미터를 동일하게 하고, 상기 제1의 실시예 및 본 실시예에 따라서 구성된 MISF ET, 또 종래의 높은 불순물농도 분포만으로 소오스 및 드레인이 구성된 MISFET에 대해서 각각 그 전달 콘덕턴스를 측정하였다. 그 결과, 상기 종래 구조 MISFET의 전달 콘덕턴스를 1로 하였을 때, 제1 및 본 실시예에 따라서 구성된 각 MISFET의 전달 콘덕턴스는 각각 0.95 및 0.98로 되었다.

본 실시예에 따른 상기 MISFET의 전달콘덕턴스의 값은 드레인 접합 깊이의 약절반이 게이트 전극(4)로 덮여지도록 구성된 MISFET에 관한 것이다. 상기 측정 결과에서 명확한 바와 같이, 드레인 접합이 게이트 전극(4)로 덮여지는 것과 같이 구성한 MISFET에 있어서는 종래 구조 MISFET와 거의 동일한 전달콘덕턴스를 확보하고, 또한 종래 구조 MISFET의 약2배의 소오스와 드레인 사이의 내압을 실현할 수가 있었다. 본 실시예에 있어서, 전달 콘덕턴스 향상의 관점에서는 게이트 전극(4)로 덮여지는 드레인 저농도 영역의 비율을 크게 하는 것이 바람직하지만, 게이트 용량의 저하의 관점에서는 상기 비율을 적게하는 쪽이 바람직하다. 따라서, 상기의 비율은 집적회로 설계에 관한 종합적 판단에 의해 결정하면 좋다.

[실시예 3]

제8도는 본 발명의 다른 실시예를 도시한 도면으로서, 상기 제1의 실시예에 있어서 낮은 불순물 농도 드레인 확산층의 형성을 위한 비소 이온 주입 공정을 2회로 나누어 각각 70KeV 및 300KeV의 에너지로 이온주입하고, 다음에 상기 제1의 실시예에 따라서 MISFET를 제조하였다.

상기 제1의 이온 주입에 의해 $5\times10^{18}cm^{-3}$ 인 최대 불순물 농도가 반도체 표면에 형성되고, 제2의 이온 주입에 의해서는 $5\times10^{17}cm^{-3}$ 인 최대 불순물 농도가 반도체 기판 표면에서 약 0.16μm 내부에 구성되는 드레인 확산층 구조로 하였다. 상기 MISFET에 있어서 소오스와 드레인 사이에 5V의 전압을 인가하고, 게이트 인가 전압의 함수로서 기판(1)에 흐르는 전류를 측정하였을 때, 그 최대 전류값은 $1.7\times10^{-7}A$이었다.

본 실시예에 의한 MISFET와 동일한 구조 파라미터를 갖는 상기 제1의 실시예에 따른 트렌지스터 및 공지의 이중 드레인 구조로 구성된 MISFET에 대해서 상기와 동일한 조건에 의해 기판 전류를 측정한 결과는 그 최대 전류가 각각 $9.6\times10^{-7}A$ 및 $1.2\times10^{-5}A$이었다.

본 실시예에 따른 MISFET의 기판전류가 종래의 구조의 MISFET에 있어서의 기판전류 보다도 약 2리 수만큼이나 작은 것은 MISFET의 신뢰성의 향상에 본 발명에 의한 MISFET가 매우 유효하다는 것을 나타내고 있다. 즉, 기판 전류의 저감은 게이트 산화막 속의로의 핫 캐리어 주입량의 저감화의 작용을 갖는 것으로 알려져 있고, 임계 전압값의 변동이나 표면 준위 밀도의 증가등의 트랜지스터 특성이 저하하지 않도

GF Exhibit 1124 - 1883/2704

록 한다.

본 실시예에 있어서는 이온 주입의 가속 에너지를 변경한 2회의 이온 주입 공정에 의해 다른 분포를 갖는 낮은 불순물 농도 분포의 합성에 의해 드레인 확산층 (5)를 구성한 일 예를 나타냈지만, 상기의 드레인 확산층은 3종류 이상의 낮은 불순물 농도 분포의 합성에 의해서도 좋고, 제조 공정도 이온 주입 법에 한정되는 것이 아니라 예를들면, 공지의 열 확산법에 의해서도 좋다. 또, 드레인 확산층을 형성하는 불순물은 동일의 것일 필요는 없고, 동일한 도전형의 원자이면 그 조합은 아무래도 좋다. 즉, 본 실시예의 기본 개념은 드레인 확산층(5)내의 최대 전계인가 영역이 한점에 집중하는 일 없이 인가 전계를 가능한 한 분산시킬 수 있는 드레인 불순물 분포를 실현하는데 있다. 상기 개념에 따르면, 최대 전계가 인가되는 불순물 농도가 약 $1\times10^{18}cm^{-3}$로 드레인 확산층(5) 전체가 구성되는 것이 이상적이고, 상기의 이상에 의해 합당한 불순물 농도 분포를 합성하여 드레인 확산층(5)를 구성하는 것이바람직하다.

[실시예 4]

제10도는 본 발명의 다른 실시예를 도시한 도면으로, 상기 제1의 실시예에 있어서의 실리콘 박막에 의해 구성된 게이트 전극(4) 대신에 Mo 박막에 의한 금속 게이트 전극(4)를 사용하고 있다. 상기의 Mo 전극의 표면 위에는 실리콘 질화막으로 되는 전국 보호막(18)을 게이트 전극(4)와 자기 정합적으로 구성하였다. 이것은 동일의 포토레지스트를 사용해서 에칭하는 것에 의해 행한 상기의 게이트 구조는 금속 게이트 구조로서 공지이며, 그 상세한 설명은 생략한다. 상기 제1의 실시예 및 상기 공지의 금속 게이트 구조 트랜지스터의 제조 방법에 따라서 낮은 불순물 농도 드레인 확산층(5) 및 소오스 확산층(6)위에 PtSi층 (12)를 형성한다.

그후, 상기 실리사이드 층(12) 바로 아래에 실리사이드층과 자기 정합의 관계로 As 이온을 주입하였다. 상기 As 이온 주입에 의한 최대 불순물 농도는$1\times10^{21}cm^{-3}$이고, 반도체 표면에서 최대값을 갖는 구성으로 되어 있다. 상기 As 이온 주입에 의한 접합 깊이는 50nm 이하로 되는 것과 같이 이온 주입기에 가속 에너지를 여러 가지로 변화시켜서 실시하였다. 그후 램프가열을 사용한 순간가열법에 의해 상기의 높은 불순물농도 영역(16)만을 활성화 하였다.

그후, 상기 제1의 실시예에 따라서 보호 절연막(15) 및 드레인 전극(9)와 소오스 전극(10)을 구성하였다. 상기 전극(9) 및 (10)과 실리사이드 층(12) 사이에는 A1과 실리사이드의 반응을 방지하기 위한 Ti,Ta혼합막(14)가 상기 실시예 1에 따라서 구성되어 있다. 상기 구성에 따라서 제조된 접합 깊이 10nm에서 50nm인 높은 불순물 농도 영역(16)을갖는 각종 MISFET에 있어서 그 BV_{DS} 값을 측정하였을 때 모든 MISFET에 있어서도 BV_{DS}값은 상기 제1의 실시예에 따른 MISFET의 BV_{DS} 값보다 약0.5V낮을 뿐 이었다.

상기의 결과는 실리사이드 층(12) 바로 아래의 높은 불순물 농도 영역(16)이 50nm 이하로 얇으면, 종래 구조 MISFET에 비해서 소오스 및 드레인 내압이 한층 개선되는 것을 나타내고 있다. 본 실시예의 기본적 개념은 드레인 확산층(5) 표면에 구성하는 높은 불순물 농도 영역(16)이 접합 깊기로 50nm 이하로 매우 얇으면 BV_{DS}값의 고내압화에 실효적으로 지장이 없고, 또한 양호한 음접촉도 확보할 수 있는 것이다. 본 실시예에 있어서는 실리사이드 층(12)를 드레인 확산층(5) 위에 구성한 에에 대해서 나타내었지만, 상기 개념에 따르면 실리사이드 층은 백금 실리사이드에 한정되는 것이 아니고, Mo,W,Pt,Pd,Ni,Ti,Ta,Nb,Cr,Pr등의 고융점 금속 및 그들의 실리사이드 막으로 치환하여 구성하여도 지장이 없다.

[발명의 다른 실시예]

이상의 각 길기예에서는 모두 소오스, 드레인 영역으로 되는 확산층은 낮은 불순물 농도의 얇은 확산층이고, 화산층 저항을 저감하는 길리사이드 층은 게이트 전국에서 분리(오프 셋)되어 형성되어 있다. 따라서, 이와 같은 오프 셋 구조의 트랜지스터에서는 소오스와 드레인을 고농도, 확산층으로 형성한 것보다도 실효찬넬 콘덕턴스가 저하한다.

그래서, 게이트 측벽 절연막(제6도, 제7도, 제8도, 제19도의 부호(11)을 실리콘 산화막이 아니고, 비유전율이 보다 높은 재료로 형성하면 게이트에서의 프린지(fringe) 용량(면이 대향하는 용향보다 광의의 의미로서, 도전체의 언저리나 끝에 생기는 용량을 말한다.)에 의해 소오스 및 드레인의 낮은 불순물 농도 확산층의 표면으로의 게이트 전압의 영향을 높일 수가 있어 실효 전달 콘덕턴스가 높은 디바이스를 얻을 수가 있다. 이것은 제1도에 도시한 바와 같은 이중 확산 구조의 소오스와 드레인을 갖는 MIS FET에 대해서도 적용된다.

[실시예 5]

제11도는 본 발명에 의한 MISFET의 1실시예를 도시한 도면으로, (1)은 P 도전형 비저항 1Ω/cm의 실리콘 기판이고, (2)는 공지의 선택 산화법에 의해 형성된 필드 산화막으로 인접하는 MISFET사이를 분리하는 두꺼운 실리콘 산화막이다. (3)은 20 nm의 실리콘 열 산화막, (4)는 인을 첨가시켜 저 조항화된 실리콘 박막으로 구성된 게이트 전극이다. 공지의 실리콘 게이트 기술에 의해 게이트 전극(4)을 형성한 후, 실리콘 열 산화막(3)을 거쳐 게이트 전극을 마스크로 해서 비소(As) 이온을 이온 주입법에 의해 실리콘 기판 표면에 주입하고, 이어서 주입 이온의 활성화를 위한 열처리를 행하여 드레인 확산층(5) 및 소오스 확산층(6)을 형성하였다. 상기의 이온 주입에 있어서는 반도체 표면에서 불순물 농도가 최대로 되고, 그 최대값이$5\times10^{18}Cm^{-3}$으로 되는 조건에서 행하였다.

그후, 암모니아(NH_3)와 모노실란(SiH_4)의 화학 기상 반응에 의해 주표면 전면에 비유전율 6.0인 실리콘질화(Si_3N_4)막을 막두께 0.25㎛의 조건으로 퇴적한다.

그후, 평행 평판형 반응성 스피터 에칭 장치에 의해 상기의 Si_3N_4 막을 0.25㎛두께만큼 에칭하였다.

GF Exhibit 1124 - 1884/2704

상기의 에칭은 소위 이방성 에칭이라고 하는 것으로서 반도체 기판 표면과 수직 방향에만 에칭을 진행시킬 수가 있다. 따라서, 상기의 에칭후에는 게이트 전극(4)의 측벽부에만 Si_3N_4막(19)가 남게 된다. Si_3N_4막으로 구성되는 측벽 절연막(19)의 형성 후, 게이트 전극(4)와 측벽절연 막(19)를 마스크로 하여 소오스 및 드레인 확산층 표면에서 최대 불순물 농도로 되는 조건으로 재차 As 이온 주입을 행한 후, 그 활성화를 위한 열처리를 실시하였다.

살기 제2의 이온 주입에 의해서 고오스 및 드에인 확산층의 최대 불순물 농도는 1×10^{-3} 이상의 높은 불순물 농도로 되었다. 그후, 통상의 반도체 제조 공정 순서에 따라, 게이트 보호 산화막(20) 및 드네인 전극(21)과 소오스 전극(22)를 형성하고 MISFET로 되는 반도체 장치를 제조하였다.

본 실시에에 따라서 제조한 MISFET는 실효 찬넬 길이가 0,9㎛, 드레인 확산층에 있어서의 낮은 불순물 농도 영역(5)의 접합 깊이가 0.35㎛, 높은 불순물 농도 영역(7)의 접합 깊이가 0.15㎛이었다.

상기 MISFET에 있어서 측벽 절연막(19)는 소오스 및 드레인 확산층 위에서 10^{20} cm^{-3} 이하의 불순물 농도 영역 표면을 덮고 있는 구성으로 되어 있다. 본 실시에에 따른 상기 MISFET의 전달 콘덕턴스는 측벽 절연막이 증래의 실리콘 산화막으로 구성되는 동일 치수의 MISFET에 있어서 전달 콘덕턴스의 약1.1배 크다는 것을 알게 되었다.

상기의 전달 콘덕턴스의 차이는 게이트 전극(4)의 측벽에 있어서 절연막(19)의 비유전율의 차이에 차이에 따른 전속 밀도의 차이에 의한 것이라고 생각된다. 즉, 본 실시에와 같아 측벽 절연박(19)의 비유전율이 게이트 산화막의 비유전율 보다 1.6배 큰 경우에는 측벽 절연막의 비유전율이 게이트 산화막의 비유전율과 동등한 종래 구성의 MISFET의 경우보다 게이트 전계가 소오스 및 드레인 확산층의 낮은 불순물 농도 영역 표면으로 돌아 들어가는 전속 밀도가 크고, 낮은 불순물 농도 영역 표면을 보다 n형화하여 전도도를 높이기 위함이라고 생각된다.

[실시에 6]

제12도는 본 발명의 다른 실시에를 설명하기 위한 도면이다. 상기 제1의 실시에에 있어서 낮은 불순물농도의 드레인 확산층(5)및 소오스 확산층(6)을 형성한 후, 실리콘 게이트 전극(4)의 표면을 열산화하여 10㎚의 실리콘 산화막(23)으로 게이트 전극(4)을 덮는다. 그후, 비유전율로 되는 실리콘 박막을 SiH_4가스의 화학 기상 반응을 사용해서 전면에 퇴적하였다. 퇴적막의 두께는 약0,5㎛이었다.

그후, 평행 평판형 반응성 스피터 장치에 의해 반도체 표면과 수직 방향으로 상기 실리콘 박막을 0.5㎛ 에칭하였다.

상기 공정에 의해 게이트 전극(4)의 측벽에 얇은 실리콘 박막(23)을 거쳐서 실리콘 퇴적막(19)가 외부로부터 격리되어 0.5㎛의 으로 남게 되었다. 상기 에칭 후는 상기 제1의 실시에에 따라서 MISFET를 제조하였다. 본 실시에에 따라서 제조한 MISFET의 전달 콘덕턴스를 측정하였을 때 실리콘 산화막으로 게이트 전극의측벽 절연막을 구성한 동일 치수의 증래 MISFET의 전달 콘덕턴스의 약 1.2배에 달하였다. 더욱 주목 되는 것은 본 실시에에 따른 MISFET의 정특성 측정후에 재차 전달 콘덕턴스를 측정하였을 때 전달 콘덕턴스는 더욱 증가하여 통상 이중 드레인 구조 MISFET의 전달 콘덕턴스의 약 1.25배까지 달한다.

상기는 소오스 및 드레인 확산층이 높은 불순물 증도 분포만으로 구성되는 통상MISFET의 전달 콘덕턴스와 거의 같은 것이다. 본 실시에의 MISFET에 있어서 실효적인 전달 콘덕턴스가 향상한 제1의 이유는 측벽 퇴적막(19)의 비유전율이 실리사이드(12)와 실리콘 산화막의 값에 비해서 충분히 크기 때문이라고 생각된다. 또, 제2의 이유는 정특성의 측정으로 5V 이상의 게이트 전압을 인가하였을 때, 게이트 전극보다 정의 전하가 얇은 산화막(23)을 거쳐서 실리콘 퇴적막(19)에 천이되어 축적되고, 이 정의 축적 전하에 의해 소오스 및 드레인 확산층의 낮은 불순물 농도 영역표면이 더욱 n형화하여 전도도가 상승하였기 때문이라고 생각된다.

즉, 실리콘 퇴적막(19)는 전기적으로 프로그램 가능한 불휘발성 메모리에 있어서의 부유 게이트의 작용을 갖는 것이라고 생각된다. 실리콘 퇴적막(19)를 정의 전하를 축적하는 부유 게이트로서 작용시키는 것은 MISFET 제조후의 좋은 품질 선택 테스트시에 특성 점검을 행할 때에 실시할 수 있으므로 제품 출하전에 전하를 주입하여 축적, 유지시키는 본 실시례의 트랜지스터에 있었어는 드레인 전계에 의한 드레인의 낮은 불순물 농도 영역의 표면 전계를 약하게 하는 적용도 갖고 있으며, 드레인 강전계에 의한 핫 캐리어의 게이트 산화막으로 주입에 따른 MISFET의 열화현상도 방지하는 다른 작용도 갖고 있다.

이상과 같이 하면 ,게이트 측벽에 있어서 프린지 용량을 개재한 게이트 전계의 영향을 소오스 및 드레인의 낮은 불순물 농도 영역 표면에 강하게 영향을 줄 수가 있고, 실효적인 전달 콘턴스를 종래 구조에 비해서 1.1~1.2배 이상 크헤 할 수 있다.

본 발명의 기본적인 개념에 따르면, 측벽 퇴적막은 실리콘 질화막에 한정되는 것은 아니고, 알루미나(Al_2O_3)탄달 산화막(Ta_2O_5), 티타늄(TiO_2), 지르코늄 산화막(Zr_2O_3), 하프늄 산화막(Hf_2O3)등 실리콘 산화막의 비유전율 보다 충분히 큰 비유전율을 갖는 유전체이면 좋다.

또, 본 발명에 의한 전달 콘덕턴스의 향상 효과는 게이트 측벽에 반도체 등으로 구성되고, 외부에서 격리된 부유 게이트 또는 외부에서 격리되 전하 축적 기구를 갖는 절연막 또는 절연막 사이의 경계면에서 형성되어도 좋으며, 외부에서 격리된 측벽 퇴적막은 실리콘에 한정되는 것은 아니고, 다른 반도체 예를 들면, 실리콘 카바이드(SiC)나 게르마늄(Ge)등이라도 좋고, 또 실리콘 질화막이나 알루미나막 등의 절연막이라도 좋다.

[발명의 또 다른 실시에]

본 발명은 드레인 확산층에 있어서의 높은 불순물 농도 영역에 관해서 증래의 상식에 구애받지 않고 그

GF Exhibit 1124 - 1885/2704

물리적 근간에 까지 되돌아가 해석한 결과에 기인한다. 즉, 여러가지의 드레인 확산층 농도를 갖는 MISFET에 있어서 드레인 확산층 표면에 고융점 금속의 실리 사이드 층을 형성 하였을 때, 인(P) 및 비소(As)등의 도전형의 불순물로 상기 드레인 확산층이 형성되어 있는 경우에 한하여 드레인 확산층 표면에 불순물 농도가 약 10nm의 깊이로 고농도화 되는 현상이 있다. 즉, NMOS에 있어서는 드레인 확산층 표면 불순물 농도가 $1\times10^{18}cm^{-3}$이상이면 상기 실리사이드 층과 반도체 표면 사이에 양호한 옴특성이 얻어져 NMOS로서의 특성에 아무런 문제도 생기지 않는다는 사실이 발견되었다.

통상의 MISFET에 있어서의 드레인 확산층은 반도체 기판 표면 부근에서 $10^{20}cm^{-3}$이상의 높은 불순물농도 영역을 가지며, 기판 내부를 향해서 가우스 분포, 또는 오차함수 분포로 감쇠하는 불순물 농도 분포를 갖는다.

상기의 통상 드레인 확산층에 전압을 인가하고, 이 즉, 불순물 농도의 함수로서 인가 전계를 해석하면, $10^{20}cm^{-3}$이상의 높은 불순물 농도 영역에 있어서는 매우 약한 전계밖에 인가되지 않는다는 사실이 판명되었다. 이 사실은, 초미세MISFET의 고내압화의 관점에서 보면, 높은 불순물 농도의 존재는 도리어 유해하고, 드레인 확산층의 최대 불순물 농도는 $10^{19}cm^{-3}$이하로 구성되는 것이 바람직하다는 것이 판명되었다. 상기의 $10^{20}cm^{-3}$이상의 높은 불순물 농도 영역의 MISFET에 있어서의 역할은 확산층 정항의 저감화와 배선 금속의 양호한 옴접촉의 확보에 있지만, 상기 후자의 역활 즉, 배선 금속과의 양호한 옴 접촉은 $1\times10^{18}cm^{-3}$이상의 표면 불순물 농도를 갖는 드레인 확산층 위의 실리사이드 층의 구조에 의해서 치환이 가능하다. 상기 전자의 역할, 즉 소오스 확산저항 및 드레인 확산 저항의 저감화에 관해서는 소오스 및 드레인 확산층 표면의 실리사이드화에 의해 실현되는 것이 알려져 있고 , 특히 초미세 트랜지스터에 있어서의 매우 얕은 접합 형성에서는 실리사이드화에 의한 저항 저감의 효과는 현저한 것이 있다.

그리하여, 본 발명의 CMOSFET는 상기의 해석 결과에 따른 개념을 발전시켜 드레인 확산층의 높은 불순물 농도 영역을 드레인 확산층과 옴 접촉으로 결합된 얇은 실리사이드 층으로 치환하고 , 또한 드레인 확산층의 불순물 농도에 관한 최적 조건을 해석적으로 구한 결과를 이용하는 것이다.

상기 최적조건은 특히 0.5㎛이하의 게이트 길이를 갖는 초미세 MISFET의 고내압화 및 래치 업 방지에 관한 최적 조건이다.

제13도 및 제14도는 각각 본 발명에 의한 해석 결과를 도시한 도면으로서, 드레인 확산층 표면 불순물 농도의 함수로써 구한 소오스 및 드레인 내압 및 최대 기판 전류의 곡선을 표시하고 있다.

제13도에 있어서는 소오스와 드레인 사이의 내압으로서 전자사태 항복전압을 점선으로 표시하고, 펀치 스루 내압을 실선으로 표시하고 있다. 각 내압 모두 찬넬 길이의 함수로서 각각 구하고 있다.

제13도에 있어서 전자사태 항복전압은 PMOS에 관한 것이고 , NMOS의 값의 전체적으로 표시된 곡선보다 0.1~1(V) 저하하는 경향에 있다. 펀치 스루 내압에 대해서는 PMOS와 MNOS의 값 사이에 다른 것은 발견되지 않는다.

제13도에서 새로이 명확하게 된 사실은 찬넬 길이가 0.5㎛ 이상의 트랜지스터에 있어서는 드레인 확산층의 표면 불순물 농도를 $3\times10^{18}cm^{-3}$으로 설정하면, 통상 구조의 동일 치수의 트랜지스터에 있어서 소오스 및 드레인 내압에 비해서 약 2배에 해당하는 10V 이상의 내압을 실현할 있는 것이다. 또, 찬넬 길이가 0.4㎛ 이하의 트랜지스터에 있어서는 찬넬 길이에 의존해서 각각 최적의 드레인 확산층 표면 불순물 농도를 약 $1\times10^{18}cm^{-3}$으로 설정하면, 소오스 및 드레인 내압을 약 7V로 까지 향상할 수가 있다. 찬넬 길이가 0.2㎛의 PMOS 트랜지스터에 있어서는 5×10^{17}의 드레인 표면 불순물 농도로 설정하면, 약 5V의 내압이 얻어지게 된다.

다음에, 제14도에 있어서는 드레인 전류에 의해 유기되는 소수 캐리어가 기판측으로 흐르는 기판 전류를 게이트 전압의 함수로써 구하고, 그 최대로 되는 값, 즉 최대 기판 전류를 드레인 확산층 표면 불순물 농도의 함수로서 해석한 것이다.

제14도에서는 찬넬 길이 1.0㎛, 찬넬 폭 10㎛의 MISFET에 관해서 소오스 및 드레인 확산층의 접합 깊이를 파라미터로 하고 , 드레인 전압은 5V이다.

제14도에서 새로이 명확하게 된 사실은 드레인 접합 깊이에 다소 의존하지만 , 드레인 확산층 표면 농도를 10^{17}내지 $10^{18}cm^{-3}$으로 설정하면, 기판전류를 통상구조의 것에 비해서 현저하게 개선할 수가 있어 래치 업 현상을 방지할 수도 있다.

내 래치 업 현상에 대한 최적 표면 불순물 농도의 드레인 확산층 위에 실리사이드층을 형성하면, 음접촉은 얻을 수 없고, 쇼트키 장벽이 형성된다.

본 발명에 있어서는 제13도 및 제14도에서 얻어진 새로운 해석 결과와 상술한 2건의 참고문헌에 따라서 지금까지 없었던 고내압에서 내 래치 업의 초미세 CMOS FET를 실현하였다. 즉, 발명의 CMOSFET에 있어서는 PMOS를 간디 2건의 문헌에 따른 쇼트키 장벽의 드레인 접합으로 형성하고, 한편 NMOS에 대해서는 제13도에서 얻어진 새로운 해석 결과에 따라서 $10^{18}cm^{-3}$이상의 표면 불순물 농도를 갖는 확산층과 음접촉을 갖는 실리사이드등의 조합으로 드레인 접합을 형성하고 있다. 이것에 의하여 내 래치 업 특성 향상 이외의 PMOS 및 NMOS의 각 소오스 드레인 확산층의 표면 불순물 농도를 0.5㎛이하의 초미세 COMSFET의 고내압화의 관점에서 더욱 최적화 하는 것이 가능하게 된다.

[실시예 7]

제15도, 제16도 및 제17도는 각각 본 발병의 제7의 실시예를 도시한 CMOSF ET의 제조공정의 단면 구조도

GF Exhibit 1124 - 1886/2704

이다.

제15도~제17도에 있어서 (221)은 n도전형으로 비저항 0.4Ω.㎝의 실리콘 기판이며, 이 기판(221)의 소정의 위치에 붕소를 접합깊이 2㎛, 표면 불순물 농도 $1\times10^{16}㎝^{-3}$으로 확산하고, P오전형 웰(222)를 형성한다. 다음에 공지의 소자 분리 기술을 이용해서 0.5㎛의 두꺼운 필드 산화막(223)을 선택적으로 형성한 후 활성 영역의 반도체 표면을 노출하고 20㎚의 막의 두께를 갖는 깨끗한 게이트 산화막(28)을 형성한다. 그후, 약 0.4㎛두께의 실리콘 박막을 게이트 산화막(28)위에 형성하고, POC_3을 확산원으로 하는 열확산에 의해 상기 실리콘 각막에 인(P)의 고능도 확산을 행한다. 다음에 상기 실리콘 박막 표면을 열산화 하고 0.2㎛두께의 실리콘 산화막을 상기 실리콘 박막위에 형성한다. 그후, 리도그래피에 의해 상기 실리콘 산화막 및 실리콘 박막을 바라는 회로구성에 따라서 동시에 제거하고, 게이트 보호 절연막(212) 및 게이트 전극(29)를 각각 남겨 놓는다. 그리고, 상기 리도그래피 후의 게이트 전극(29)의 폭 즉, 찬넬폭으로서는 1.0, 0.5, 0.3, 0.2 및 0.1㎛의 5개 조건에 대해서 실시하였다.

상기 리도그래피 후, 테트라 에록시실란($Si(OC_2H_5)_4$)를 사용한 화학 기상 반응에 의해 0.3㎛의 막의 두께를 갖는 실리콘 산화막을 전면적으로 퇴적시킨다. 상기 퇴적막을 반응성 스피터 에칭에 의해 반도체 기판 표면과 수직방향으로 에칭하고, 평탄부에 퇴적된 실리콘 산화 퇴적막을 제거하면 게이트 전극(29) 및 필드 산화막(223)의 각 측벽부분에만 실리콘 산화 퇴적막(213)이 남게 된다. 다음에 0.8㎛두께의 포트 레지스트막을 웰(222)를 제외한 영역의 게이트 산화막(28)위에 남겨 놓고, 가속 에너지 70KeV의 조건에서 비소(As)의 이온주입을 행한다. 상기의 이온주입은 웰 영역(222)에 대해서는 게이트 산화막(28)을 거쳐서 행하여지고, 반도체 기판 표면에서 최대 불순물 농도로 되는 조건이다. 한편, 웰 영역(222)이외에 대해서는 상기 포트 레지스트막에 의해 주입 이온이 저지되어 반도체 기판(221)내에는 주입되지 않는다. 상기의 이온 주입후, 남겨진 포트 레지스트막을 제거하고 나서 주입 이온의 활성화, 열처리를 실시하고, N도 전형의 소오스(24) 및 드레인(25)를 형성한다(이상 제15도).

그리고, 상기의 소오스 및 드레인 확산층(24), (25)의 각각의 표면 불순물 농도는 찬넬 길이가 0.5㎛이상 일때에는 3×10^{18}, 0.3㎛이하 일때에는 $1\times10^{18}㎝^{-3}$으로 최종적으로 형성되도록 비소(As) 이온 양을 설정한다. 도, 상기의 소오스(24), 드레인(25)의 확산층의 접합 깊이가 최종적으로 0.25㎛가 되도록 상기의 열처리 조건을 제어한다. 상기 열처리후, 웰 영역(222)위에만 0.8㎛두께의 포트 레지스트막으로 덮고, 붕소를 가속 에너지 70KeV의 조건으로 이온 주입을 행한다. 상기의 이온 주입에 의해 웰 영역(222) 이외의 영역에 있어서 게이트 산화막(28)을 거쳐서 붕소가 반도체 기판(221)에 주입되고, 그 최대 불순물 농도는 반도체 기판(221)의 표면이었다. 웰 영역(222)에 있어서는 상기 포토 레지스트막에 의해 이온주입이 저지되어 반도체 기판(221)내에 주입되지 않는다. 상기의 이온주입 후, 남겨진 포트 레지스트막을 제거하고 나서 주입 붕소 이온의 활성화 열처리를 실시하고, P도전형의 소오스(26)및 드레인(27)을 형성한다(이상 제16도 참조).

상기 소오스(26) 및 드레인(27)의 확산층의 각각의 표면 불순물 농도는 최종적으로 3종류의 조건 $3\times10^{17}㎝^{-3}$, $1\times10^{18}㎝^{-3}$로 되도록 주입 붕소량을 설정한다. 또, 소오스(26)및 드레인(27)의 확산층의 접합 깊이가 최종적으로 0.25㎛로 되도록 상기의 열처리 조건을 제어한다. 상기 열처리 후, 반도체 기판(221)위에 노출되어 있는 게이트 산화막을 제거하고 나서 50㎚의 막의 두께를 갖는 백금(Pt)을 스피터링 법에 의해 전면에 증착하고, 계속하여 450℃의 열처리를 실시한다. 상기의 저온 열처리에 의해 반도체 기판(221)의 표면에 노출하고 있는 소오스 확산층 영역(24) 및 (26), 드레인 확산층 영역(25) 및 (27)의 각 표면 부분에 백금 실리사이드(PtSi)층(214)가 자기 정합적으로 형성된다. 상기의 열처리에 있어서 필드 산화막(223), 측벽 퇴적 산화막(213) 및 보호 산화막(212)위에서 백금(Pt)은 반응하지 않으므로 실리사이드층(214)는 형성되지 않는다. 상기의 저온 열처리 후, 왕수로 전면적에 백금(Pt)을 에칭한다. 백금 실리사이드(PtSi)는 왕수로 제거되지 않아 소오스 확산층(24) 및 (26)과 드레인 확산층(25) 및 (27)위에만 자기 정합적으로 남게 된다. 이 시점에서는 N도전형의 소오스(24) 및 드레인(25)영역에 있어서의 백금 실리사이드(PtSi)층(214)의 바로 아래에는 백금 실리사이드층 형성전의 표면 불순물 농도보다도 1자리수 높은 불순물 농도를 갖는 약 10㎚두께의 석출층의 백금 실리사이드(PtSi)층(214)에 대해 자기 정합적으로 형성된다.

백금 실리사이드층(214)형성후, 모노실란(SiH_4)과 산소(0_2)의 화학 기상 반응에 의해 약 500㎚두께의 실리콘 산화막(210)을 전면에 퇴적하고, 소오스(24) 및 (26), 드레인(25) 및 (27)위, 또 게이트 전극(29)위의 접촉구멍을 구성시키는 부분의 상기 실리콘 산화막(210)를 리도그래피에 의해 선택적으로 제거한다. 상기의 실리콘 산화막(210)의 선택적 제거를 한 후, 상기 공정에 사용한 포트 레지스트막을 남겨둔 채, 티타늄(Ti)와 텅스텐(W)의 동시 스퍼터에 의해 TiW 막(215)를 전면에 피착시킨다. 그후, 상기 포토 레지스트막을 제거하지만, 이 공정에 의해 포트 레지스트막 위의 TiW막도 동시에 제거되기 때문에 실리콘 산화막(210)이 제거된 영역에만 선택적으로 TiW막(215)가 남게 된다. 최후로 바라는 회로구성에 따라서 알루미늄(Al)에 의한 배선(211)을 형성한다(이상 제17도 참조).

그리고, TiW막(215)는 알루미늄 배선(211)과 실리사이드층(214)의 반응을 방지하기 위해서 필요하게 된다.

다음에, 상기 제조 공정에 의해서 제조된 CMOSFET에 관하여 우선, 소오스와 드레인 사이의 내압을 측정하였을때, 다음의 결과를 얻었다. 즉, P도전형의 소오스(26) 및 드레인(27)의 각 확산층에 있어서의 표면 불순물 농도를 $3\times10^{37}㎝^{-3}$으로 설정한 PMOS에 있어서는 쇼트키 특성을 나타내지만, 찬넬 길이가 0.2㎛이상의 MOSFET의 내압은 약 5V의 값을 얻을수가 있었다. 이 값은 P전형 드레인 표면 불순물 농도가 $10^{18}㎝^{-3}$이상에서 구성되는 종래 구조의 MOSFET에 있어서의 내압의 2배 이상의 값이다. P도전형 드레인 표면 불순물 농도를 $1\times10^{18}㎝^{-3}$으로 설정한 PMOS에 있어서는 P+N접점에 따른 트랜지스터 특성을 표시하지만, 그 소오스와 드레인 사이의 내압은 찬넬 길이가 0.3㎛이상의 MOSFET에 있어서 6.5 내지 7V로 되었다. 이

GF Exhibit 1124 - 1887/2704

값은 종래의 값에 비해서 1.6 내지 1.7배 이며, 고내압화가 실현된 것을 나타내고 있다. 또, P도전형 드레인 표면 불순물 농도를 $3\times10^{18}cm^{-3}$로 설정한 PMOS있어서도 P+N접합에 따르는 특성을 나타내지만, 그 소오스와 드레인 사이의 내압은 찬넬 길이가 0.5㎛이상의 MOSFET에 있어서는 약 12V로 되었다. 이 값을 종래의 값에 비해서 2V이상 높고, 고내압이 실현되게 된다.

N도전형의 소오스(4) 및 드레인(5)의 각 확산층에 있어서의 표면 불순물 농도를 $3\times10^{18}cm^{-3}$으로 설정한 NMOS에 있어서 찬넬 길이가 0.5㎛이상의 MOSFET에 있어서는 그 소오스와 드레인 사이의 내압은 약 10V이었다. 이 값 은 종래의 값에 비해서 약 2배의 값이며, 고내압화가 되게 된다. 드레인 표면 불순물 농도를 $1\times10^{18}cm^{-3}$으로 설정한 NMOS에 있어서도 소오스(24) 및 드레인(25)와 실리사이드층(214)의 사이에는 양호한 음특성이 확보되어 P+N 접합에 따흐는 트랜지스터 특성이 얻어졌다. 그 소오스와 드레인 사이의 내압은 찬넬 길이에 의존하고, 찬넬 길이가 0.3㎛MOSFET에서는 약 3V로 되었다. 이들의 값은 종래 구조의 NMOS에 있어서의 소오스와 드레인 사이의 내압에 비해서 2배 이상의 고내압화로 된다.

본 실시예에 따른 CMOSFET에 있어서의 NMOS 및 PMOS의 소오스와 드레인 사이의 내압은 제13도에 도시한 해석결과의 매우 잘 일치하고 있으며, 상기 해석의 타당성이 증명되게 된다. 즉, 본 실시예에 의하면 0.5㎛이하의 찬넬 길이를 갖는 초미세 CMOSFET의 소오스와 드레인 사이의 내압을 종래에 비해서 2배이상 향상시킬 수가 있다. 구체적으로는 찬넬 길이가 0.5㎛이상의 CMOSFET에 있어서는 NMOS 및 PMOS의 각 소오스 및 드레인 확산층 표면 불순물 농도를 $3\times10^{18}cm^{-3}$으로, 찬넬 길이가 0.3㎛일때에는 상기 불순물 농도를 $1\times10^{18}cm^{-3}$로 설정해서 본 실시예에 따라 MOSFET를 완성시키면, 각각 10V 및 6V의 고내압 초미세 COMSFET를 얻을 수가 있다. 또, 찬넬길이가 0.2㎛일때에는, PMOS의 소오스 및 드레인 확산층이 표면 불순물 농도를 $3\times10^{17}cm^{-3}$으로, NMON의 상기 표면 불순물 농도를 $1\times10^{18}cm^{-3}$에 각각 설움직여써하고, 본 실시에에 따라서 MOSFET를 완성시키면, 소오스와 드레인 사이의 내압 3V의 초미세 CMOSFET를 얻을 수가 있다. 상기의 MOSFET에 있어서 POMS의 소오스(26) 및 드레인 (27)과 실리사이드층(214)의 사이에는 쇼트키 장벽이 형성되지만, 특성상 문제로 되지 않는다. 이 쇼트키 장벽은 오히려 내 래치 업 특성을 향상시키는 기능을 갖추고 있다.

다음에, 본 실시에에 표시한 제조 공정에 의해 제조된 CMOSFET에 대해서 내 래치 업 특성을 평가한다. 내 래치 업 특성으로서는 다음의 것을 측정한다. 즉, NMOS의 드레인(25)를 에미터, 웰(22)를 베이스, 반도체 기판(21)를 콜렉터로 하는 기생 NPN트랜지스터의 전류 이득률 βN과 PMOS의 소오스(26)을 에미터, 반도체 기판(21)을 베이스, 웰(22)를 콜렉터로 하는 기생 PNP트랜지스터의 전류 이득률 βP와의 곱 βN · βP를 측정하였다. 이 측정에서는 베이스와 콜렉터 사이에 5V의 전압을 인가하고, 10^{-6}내지 10^{-2}A의 범위의 에미터 전류의 함수로서 βN · βP를 구하였다. 그 결과, PMOS 및 NMOS의 각 드레인 표면 불순물 농도가 $3\times10^{18}cm^{-3}$ 찬넬 길이가 0.5㎛의 CMOSFET상기 각 드레인 표면 불순물 농도가 $1\times10^{18}cm^{-3}$ 찬넬 길이가 0.3㎛의 CMOSFET 및 PMOS의 드레인 표면 불순물 농도가 $3\times10^{17}cm^{-3}$, NMOS의 상기 표면 불순물 농도가 $1\times10^{18}cm^{-3}$ 찬넬 길이가 0.2㎛의 CMOSFET에 있어서의 각 βN · βP의 곱의 최고 값은 모두 10^{-2} 내지 10^{-4}이었다. 상기의 값은 래치 업이 발생할 수 있는 조건 βN · βP> 1을 만족시킬수 있는 것은 아니며, 또 ,PMOS의 드레인을 쇼트키 접합으로, NMOS의 드레인을 통상의 높은 불순물 농도 N+P접합으로 구성한 CMOSFET에 있어서의 βN · βP 곰의 값 10^{-2}와 거의 같던가 그 이하의 값이다. 상기의 결과에서 PMOS의 드레인 확산층을 낮은 불순물 농도로 설정한 COMSFET에 있어서는 내 래치 업의 관점에서 오히려 소오스와 드레인 사이의 내압의 향상의 관정에 있어서 NMOS의 드레인 표면 불순물 농도의 최적조건을 바라는 찬넬 길이에 따라서 설정하면 좋은 것으로 된다.

다음에 본 실시에에 의한 CMOSFET에 있어서 NMOS 및 PMOS의 각 드레인 표면 불순물 농도를 5×10^{18}내지 $10^{20}cm^{-3}$으로 설정한 찬넬 길이 0.2 내지 1.0㎛의 COMSFET도 동시에 제조하고, 그 소오스와 드레인 사이의 내압 및 내 래치 업 특성을 측정하였다. 상기 COMSFET의 소오스 드레인 사이의 내압은 종래의 값보다 최대 수 V로 개선되고, 또 βN · βP곱도 1이하이었지만, 상술의 결과에 비하면 약간 뒤떨어지는 특성이었다.

[실시에 8]

제18도 및 제19도는 본 발명의 제8의 실시예를 도시한 CMOSFET의 제조 공정의 단면 구조도이다.

제15도에 도시한 상술한 제7의 실시에에 있어서 실리콘 산화 퇴적막(213)를 게이트 전극(29)및 필드 산화막(23)의 측벽부에만 자기 정합적으로 남겨둔 후, 노출되어 있는 게이트 산화막을 완전히 제거한다. 다음에, 지클로루실탄(SiH_2Cl)과 염산(HCL)의 화학기상반응을 775℃의 온도로 행하고, 0.3㎛의 두께의 다결정질 또는 비정질의 실리콘 박막(216)을 웰(222)표면위 및 N도전형을 유지하고 있는 반도체 기판(21) 표면 위에 선택적으로 퇴적시킨다(이상 제18도 참조). 상기 실리콘 퇴적막의 형성조건은, 지클로루실란200cc, 염산 60cc의 조건으로 퇴적속도는 10㎚/분이다. 이 조건에 있어서는 피퇴적 표면에 실리콘 질화막(Si_3N_4)이 존재하지 않는 한 실리콘 기판 위에만 선택적으로 퇴적하고, 또 측벽 절연막(213)과의 경계부에 있어서도 소위 파셋(facet)이라 하는 오목 볼록이 없는 평탄한 현상을 얻을 수가 있다.

실리콘 박막(216)의 퇴적후, 웰 영역(222)위의 실리콘 박막 부분에만 이온 주입이 행하여지도록 포토 레지스트막을 선택적으로 형성하고, 붕소 이온 주입을 실시한다. 붕소 주입량은 상기 실리콘 박막(216)내의 불순물 농도가 웰 (222)표면의 불순물 농도와 일치하도록 설정한다. 주입 에너지는 25KeV이다. 그후, 이온 주입의 마스크에 사용한 포토 레지스트막을 제거하고 나서 1150℃, 15초의 조건으로 고온 단시간 열처리를 실시하고, 주입 이온의 활성화와 실리콘 박막(216)의 단결정화를 행한다. 사전에 다결정질, 또는 비정질로 형성된 실리콘 박막(216)내에 있어서 불순물의 확산 계수는 단결정 실리콘 내에 있어서의 확장 계수에 비해서 10 내지 20배나 크다. 따라서, 상기의 단시간 열처리에 의해 웰(222)위의 실리콘 박

GF Exhibit 1124 - 1888/2704

막(216)에 주입된 붕소는 실리콘 박막(216)내에서 깊이 방향에 대해 대략 균일하게 분포한다. 상기 열처리를 한 후, 상술의 제7의 실시예에 따라서 N도전형의 소오스(24) 및 드레인(25)와 P도전형의 소오스(26) 및 드레인(27)을 형성한다. 상기의 단시간 고온 열처리에 의해 실리콘 박막(216)은 이미 단결정화 되어 있다. 따라서, 상기의 각 소오스 및 드레인의 형성 조건은 상기 제7의 실시예의 경우와 같은 조건으로 실시된다. 그후의 공정도 상술한 제7의 실시예에 따라서 CMOSFET를 제조한다(이상 제19도 참조).

제19도에 표시한 제8실시에 따른 CMOSFET는 상술한 제7의 실시예에 따른 CMOSFET와 동일 치수를 갖고 있으며, 양자의 소오스와 드레인 사이의 내압을 비교하였을때, 찬넬 길이 0.3㎛, 소오스 및 드레인 표면 불순물 농도 $1\times10^{18}cm^{-3}$의 조건에 있어서의 제8실시에의 CMOSFET의 쪽이 약 1V만큼 높고, 7V의 내압이 얻어졌다. 또, 찬넬 길이 0.2㎛, NMOS 및PMOS의 드레인 표면 불순물 농도가 각각 $1\times10^{18}cm^{-3}$ 및 $3\times10^{17}cm^{-3}$의 조건으로 구성된 제8실시에의 CMOSFET의 내압을 측정하고, 상술한 제7실시에의 CMOSFET의 내압과 비교하였을때, 전자의 쪽이 약 2V높은 5V의 값을 얻었다. 상기의 값은 종래 구조에 따른 CMOSFET의 소오스, 드레인 사이의 내압과 비교해서 3배 이상의 고내압화를 실현한 것으로 된다. 제8의 실시에에 따르는 CMOS FET에 있어서 기생 바이폴라 트랜지스터에 관한 전류 이득률의 곱 βN · βP를 여러가지의 찬넬 길이, 소오스 및 드레인 표면 불순물 농도를 갖는 경우에 대해서 측정하였으나, 모두 상술의 제7실시에에 따른 CMOSFET의 측정값에 비해서 2/3 내지 1/2로 저감화 되어 있었다. 이와 같이, 제8실시에에 따른 CMOSFET는 제7실시에에 따른 CMOSFET보다 소오스와 드레인 사이의 내압 및 내 래치 업 특성에 있어서 향상하고 있지만, 그 이유는 소오스 및 드레인의 각 접합이 반도체 박막(216)내에 설치된 것에 의해 접합 면적이 저하하고, 또한 실효 찬넬 길이가 증가하였기 때문이라고 생각된다.

[실시에 9]

제20도 및 제21도는 본 발명의 제9의 실시예를 표시한 CMOSFET의 단면구조도와 N도전형의 드레인 확산영역에서의 깊이 방향에 관한 불순물 농도 분포도이다.

제18도에 도시한 제8실시에에 있어서 다결정질, 또는 비정질의 실리콘 박막(216)을 반도체 기판(221)위에 자기 정합적으로 퇴적시킨 후, 웰 영역(222)위의 실리콘 박막 부분에만 이온 주입이 행하여지도록 다른 영역 표면위에 포토 레지스트막을 남겨 놓는다. 그후, 웰 영역9222)위의 실리콘 박막 부분에 비소의 이온 주입을 행하고 나서 상기의 남겨진 포트 레지스트막을 제거한다.

다음에, 웰 영역(222)를 포토 레지스트막으로 덮고, 웰 영역(222)이외의 N도전형을 갖는 반도체 기판(221)위의 실리콘 박막 부분에만 이온 주입이 행하여지도록 재차 포트 레지스트막을 남겨 놓는다. 그후, 붕소를 이온 주입하고, 재차 포토 레지스트막을 완전히 제거해서 실리콘 박막(216)의 표면을 노출시킨다. 이상태에서 1100℃, 30초의 조건의 단시간 고온 열처리를 실시한다. 상기 조건의 열처리을 행하여도 실리콘박막(216)은 단결정화 되지 않고, 다경정질 또는 비정질의 상태를 유지하고 있다. 다결정질, 또는 비정질의 실리콘 박막(216)내에 있어서의 불순물의 확산 계수는 상술과 같이 매우 큰 값이기 때문에 상기 조건에 의한 단시간 열처리에 의해서 실리콘 박막(216)내에서 비소 및 붕소는 고속으로 거의 균일한 농도 분포로 된다. 그러나, 반도체 기판(21)내에 있어서의 각 불순물의 확산 계수는 상대적으로 작고, 상기 단시간의 열처리에 의해서는 반도체 기판(21)내에 약 20㎚정도밖에 확산되지 않았다.

이와 같이 비소 및 붕소의 이온 주입과 그에 따르는 단시간 열처리에 의해 실리콘 박막(216)과 웰(222) 및 N도전형 반도체 기판(221)내에 각각 N도전형의 소오스(24)와 드레인(25) 및 P도전형의 소오스(26)과 드레인(27)을 형성한다. 그후, 상기 각 소오스(24) 및 (26)과 드레인(25) 및 (27)위에 백금 실리사이드(PiSi)층(214)를 상술의 제7의 실시에에 따라서 자기 정합적으로 형성하고, 그후의 공정도 제7의 실시에에 따라서 실시하는 것에 의해 제20도에 도시한 CMOSFET를 제조할 수가 있다.

제9실시에에 의한 CMOSFET의 N도전형 소오스(24) 및 드레인(25)의 불순물 농도 분포는 제21도에 도시한 바와 같이 3개의 영역 A, B, C로 분리된다. 즉, 실리사이드층(214)바로 아래에 있어서의 약 10㎚두께의 불순물 석출 영역A, 실리콘 박막(216) 내부의 균일 분포 영역 B 및 웰9222)내에 있어서의 접합 깊이 약 20㎚를 갖는 급격한 농도 분포 영역 C이다. P도전형 소오스(26) 및 드레인(27)내에 있어서는 상기 불순물 석출 영역 A의 존재는 인정되지 않았다.

제9실시에에 따른 CMOSFET에 있어서는 상기 실리콘 박막(216)내의 균일 분포 농도로서, NMOS에 관해서는 $1\times10^{18}cm^{-3}$, $3\times10^{18}cm^{-3}$, $10^{19}cm^{-3}$, $5\times10^{19}cm^{-3}$의 각 값이, 또 PMOS에 관해서는 $1\times10^{17}cm^{-3}$, $3\times10^{17}cm^{-3}$, $1\times10^{18}cm^{-3}$, $3\times10^{18}cm^{-3}$ 및 $5\times10^{18}cm^{-3}$의 값이 최종적으로 되도록 비소 또는 붕소 이온 주입량을 설정하는 것에 의해서 MOSFET를 제조하였다. 또, 찬넬 길이에 관해서도, 0.1, 0.2, 0.3, 0.5 및 1.0㎛의 값 일 때에 대해서 MOSFET를 제조하였다. 상기 각종의 CMOSFET에 대해서 소오스와 드레인 사이의 내압 및 기생 바이폴라 트랜지스터의 각 전류 이득률의 곱 βN · βP를 측정하였다. NMOS의 드레인(27)내의 균일 분포 불순물 농도가 $10^{18}cm^{-3}$이상 일 때, 상기 특성 향상은 그다지 확인되지 않았다. 그러나, 상기 균인 분포 불순물 농도가 10^{17} 내지 $10^{19}cm^{-3}$의 낮은 불순물 농도로 설정되어 있을 때에는 특히 소오스와 드레인 사이의 내압의 향상이 현저하였다. 드레인 내의 균일 분포 불순물 농도가 $1\times10^{18}cm^{-3}$일 때 찬넬 길이가 0.1 및 0.2㎛의 각 CMOSFET에 있어서의 소오스와 드레인 사이의 내압은 각각 4.5 및 8 V에 달하였다. 이들이 값은 제8의 실시에에 따른 CMOSFET일 때에 비해서도 많이 개선되어 있으나, 이 효과는 찬넬 길이가 짧은 경우의 쪽이 상대적으로 현저하였다. PMOS에 있어서의 드레인(25) 내의 균일 분포 불순물 농도가 10^{17} 내지 $10^{18}cm^{-3}$미만으로 설정되고, 또한 게이트 길이가 0.1㎛일때에도 소오스와 드레인 사이의 내압은 제8의 실시에 일 때와 비교해서 수 V 향상되고 있으며, 그 값은 5V 이상에 달하였다.

제9의 실시에와 제8의 실시에에 있어서의 이 효과의 차이는 드레인 최대 전계가 인가되는 낮은 불순물 농도 영역이 제9실시에일 때에는 실리콘 박막(216)내에서 제21에 도시한 바와 같이 대략 균일하게 형성

GF Exhibit 1124 - 1889/2704

되기 때문이고, 그에 의한 전계분산 효과가 된다고 생각된다.

또, 제9실시예에 따른 초미세 CMOSFET의 기생 바이폴라 트랜지스터의 곱 βN · βP에 관해서는 제8실시예의 경우와 거의 변함이 없고, 래치 업 현상은 무시할 수 있는 정도이었다.

본 발명의 제1내지 제6의 실시예에 의하면, 최대 전계인가 영역이 드레인 확산층내에서 넓게 분산할 수 있으므로, 동일 구조 파라미터를 갖는 종래 구조의 트랜지스터 보다 5V이상이나 소오스와 드레인 사이의 내압을 향상할 수 있다. 따라서, 본 발명에 의하면 전원 정압을 종래의 5V에서 3V이하로 내리는 것과 같은 변경도 없이 실효 찬넬 길이가 0.5㎛이하의 미세 트랜지스터를 동작시킬수가 있다.

본 발명의 제1 내지 제3의 실시예에 있어서는 PtSi층의 형성시에 있어서의 PtSi층 바로 밑의 불순물의 석출 효과를 이용해서 음 접촉에 필요한 불순물 농도 영역을 PtSi층과 자기 정합의 관계로 구성하였으나, 상기의 PtSi층은 Mo, W, Pb, Ni, Ti, Ta, Nb, Cr, Pr등의 다른 고융점 금속 또는 그들의 실리사이드막으로 치환해서 구성하여도 지장이 없다. 또, 본 발명의 각 실시예에 있어서는 소오스 및 드레인 확산층을 P이온에 의해 형성한 이를 도시하였으나, 상기 확산층은 P이온에 의해서 형성하여도 좋다. 또, 그 형성 방법도 이온 주입에 한정되는 일없이 열 확산법 등 다른 공지의 수단에 의해서도 본 발명의 요지를 이탈하지 않는다. 또, 본 발명은 상기와 같은 단일체 트랜지스터에 한정되는 일이 없이 반도체 집적회로 장치에 대해서도 적용된다.

또, 제7 내지 제9도의 실시예에 의한 효과는 종래 구조에 있어서의 소오스와 드레인에 대응하는 영역을 개선하는 것에 의해 얻어지는 것으로, 결코 반도체 기판(221)의 농도를 증대시켜서 고내압화를 도모하는 것은 아니다. 따라서, 반도체 기판 농도의 증대에 따르는 이동도의 저하를 조래하는 일도 없고 고속 동작을 손상하는 일도 없다.

본 발명의 제7 내기 제9의 실시예에 의하면, 소오스 및 드레인 위에 고융점 금속 또는 그 실리사이드층이 형성되어있기 때문에 초미세 CMOSFET에 있어서도 그 시이트 저항는 수Ω/㎠으로 낮은 저항성을 유지할 수 있어 고속 동작을 보장할 수가 있다.

제7~제9의 각 실시예에 있어서는 소오스 및 드레인 확산층의 최대 불순물 농도에 관하여 $1\times10^{17}cm^{-3}$이상일 때에 대해서 기술하였으나, 이것은 제13도의 해석 결과 즉, 0.1㎛의 게이트 길이에 대하여서의 해석 결과에 따르고 있다. 0.1㎛의 값은 실현할 수 있는 최소의 게이트 길이이다. 또, 상기의 불순물 농도($1\times10^{17}cm^{-3}$)이하에서 본 발명을 적용할 때에 제14도에서 추측할 수 있는 바와 같이 기판 전류의 증대 및 드레인 누설 전류의 증대를 초래하게 되는 것이다.

또, 제7~제9의 각 실시예에 있어서는 소오스 및 드레인 확산층 위에 백금 실리사이드(PtSi)층을 자기 정합적으로 형성하였으나, 이것은 일예로서 이 PtSi층 대신에 Mo, W, Pb, N, Ti, Ta, Nb, Cr, Pr등의 고융점 금속 또는 그 실리사이드 막을 사용할 수가 있다. 또, 각 실시예에 있어서는 단시간 열처리로서 고온 전기로를 사용하는 방법에 대해서 설명하였으나, 이 공정은 램프가열법, 레이저 또는 전자선 조사법 등의 다른 방법에 의해서도 가능하다. 또, 각 실시예에 있어서는 P도전형 웰을 사용한 경우에 대해서 설명하였으나, 역으로 P도전형 반도체 기판내에 N도전형의 웰을 형성한 구조의 CMOSFET에 대해서도 본 발명을 적용할 수가 있다.

이상 설명한 바와 같이 본 발명에 의하면, 0.2㎛의 극히 짧은 찬넬 길이라도 5V의 통상 전원으로 동작시킬수가 있고, 또 래치 업 현상을 방지할 수 있기 때문에 고속 동작을 손상시키는 일없이 초미세 CMOSFET를 실현하는 것이 가능하다.

(57) 청구의 범위

청구항 1

전계 효과 트랜지스터에 있어서, 반도체 기판(1)과 반대 도전형의 드레인(5) 또는 소오스(6) 영역에 있어서 최대 불순물 농도가 $10^{18}cm^{-3}$이상 $10^{20}cm^{-3}$미만으로 구성되고, 상기 드레인 또는 소오스 영역표면의 적어도 일부는 고융점 금속층 또는 그 실리사이드층(12)와 50㎚을 초과하지 않는 두께를 갖는 높은 불순물 농도 영역(16)으로 되는 높은 도전층과 접하고 있는 것을 특징으로 하는 반도체 장치.

청구항 2

특허청구의 범위 제1항은 기재의 전계 효과 트랜지스터에 있어서, 상기 높은 도전층이 고융점 금속층 또는 그 실리사이드층(12)만으로 구성되어 있는 것을 특징으로 하는 반도체 장치.

청구항 3

특허청구의 범위 제1항은 기재의 전계 효과 트랜지스터에 있어서, 상기 드레인(5) 또는 소오스(6)영역의 적어도 일부가 게이트 전극(4)아래에 존재하는 것을 특징으로 하는 반도체 장치.

청구항 4

특허청구의 범위 제1항은 기재의 전계 효과 트랜지스터에 있어서, 상기 드레인(5) 또는 소오스(6)영역의 적어도 한쪽이 적어도 2회의 이온 주입에 의해서 형성되는 것을 특징으로 하는 반도체 장치.

청구항 5

특허청구의 범위 제3항 기재의 전계 효과 트랜지스터에 있어서, 상기 게이트 전극(4)가 Mo 박막 또는 실리콘 박막으로 구성되는 것을 특징으로 하는 반도체 장치.

GF Exhibit 1124 - 1890/2704

청구항 6

특허청구의 범위 제3항 기재의 전계 효과 트랜지스터에 있어서, 상기 게이트 전극(4)의 측벽부에 비유전율이 실리콘 산화막 보다 높은 게이트 측벽 절연막(19)를 형성하여 되는 것을 특징으로 하는 반도체 장치.

청구항 7

특허청구의 범위 제6항 기재의 전계 효과 트랜지스터에 있어서, 상기 측벽 절연막(19)를 실리콘 질화막으로 구성한 것을 특징으로 하는 반도체 장치.

청구항 8

불순물 확산 영역의 최대 불순물 농도가 10^{18} 내지 $10^{20}cm^{-3}$정도의 N형 드레인(24) 또는 소오스 영역(25)와 최대 불순물 농도가 10_1^7 내지 $10^{19}cm^{-3}$정도의 P형 드레인(26) 또는 소오스 (27)영역을 가지며, 또 상기 각 드레인 또는 소오스 영역의 적어도 일부가 고융점 금속 또는 금속의 실리사이드층(214)와 접합되어 구성되고 있는 것을 특징으로 하는 반도체 장치.

청구항 9

특허청구의 범위 제8항에 있어서, 상기 각 드레인(24, 26) 또는 소오스 (25, 27)영역의 일부는 반도체 기판 표면 위에 절연막(28)을 거쳐서 구성된 게이트 전극(29)와 상기 게이트 전극의 측벽에 형성된 절연막(213)을 거쳐서 인접해서 형성되는 반도체 장치.

청구항 10

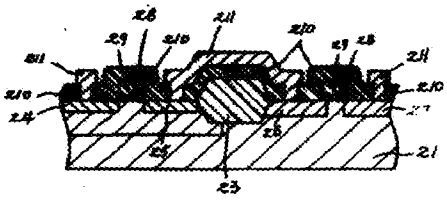
특허청구의 범위 제 8항에 있어서, 상기 N형 드레인(24) 또는 소오스(25)영역은 고융점 금속 또는 그 실리사이드층(214) 바로 아래의 불순물 석출영역(A), 실리콘박막(216)내부의 균일한 분포의 영역(B), 급격한 농도 분포 영역(C)의 3개의 불순물 농도 분포 영역을 수직 방향으로 갖고 있는 반도체 장치.

청구항 11

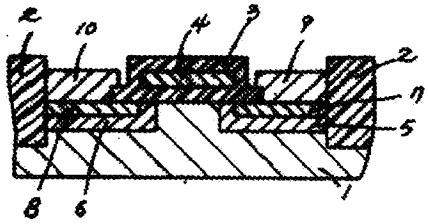
특허청구의 범위 제9항에 있어서, 상기 각 드레인(24, 26) 또는 소오스(25, 27)영역의 일보는 다결정 박막 또는 비정질 박막(216)으로 형성되는 반도체 장치.

도면

도면1

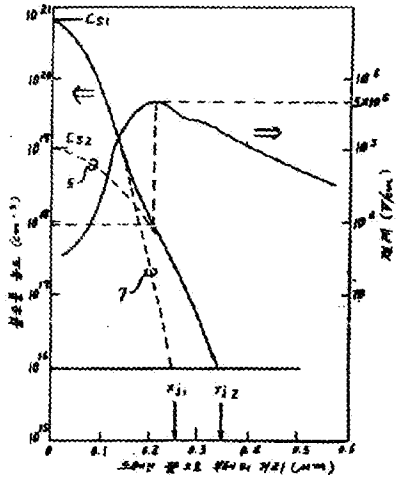


도면2a

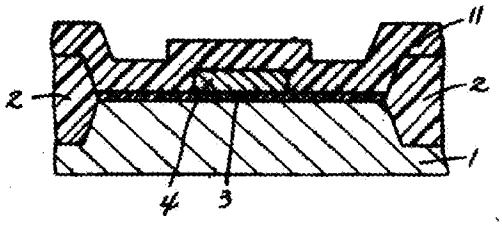


GF Exhibit 1124 - 1891/2704

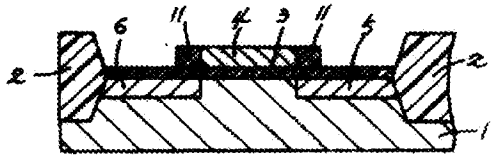
도면2b



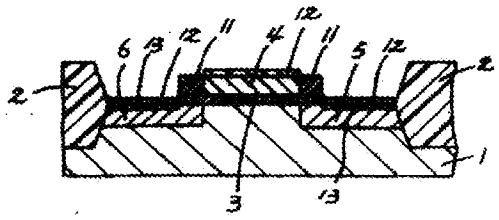
도면3



도면4

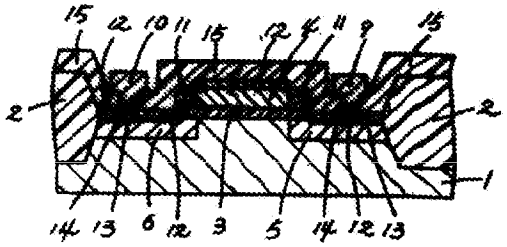


도면5

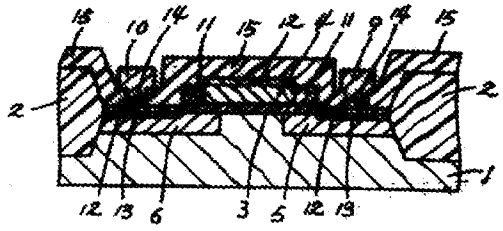


GF Exhibit 1124 - 1892/2704

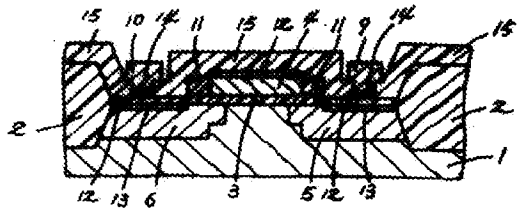
도면6



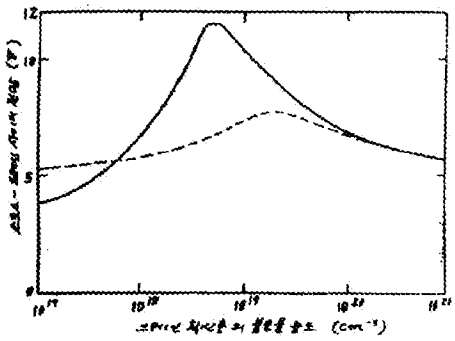
도면7



도면8

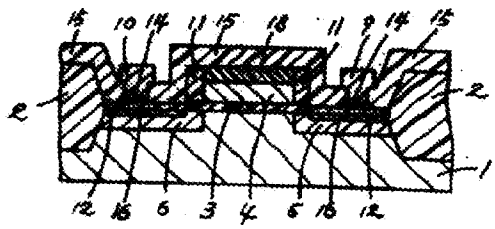


도면9

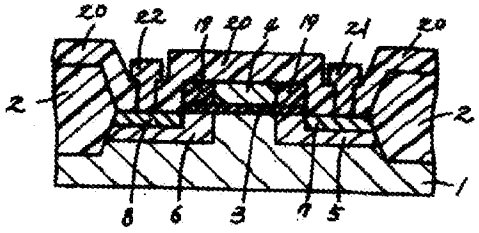


GF Exhibit 1124 - 1893/2704

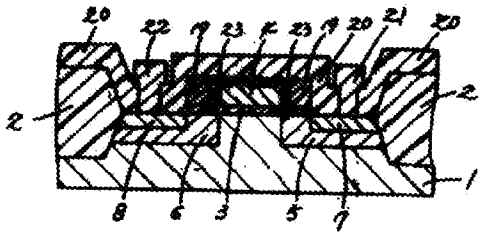
도면10



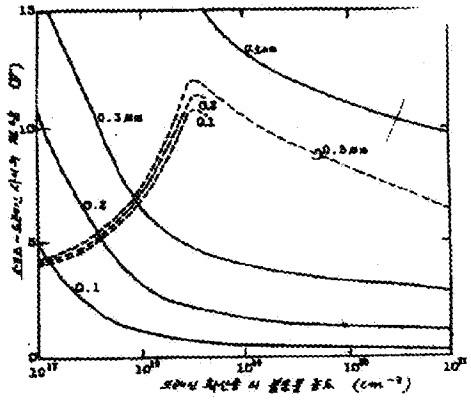
도면11



도면12

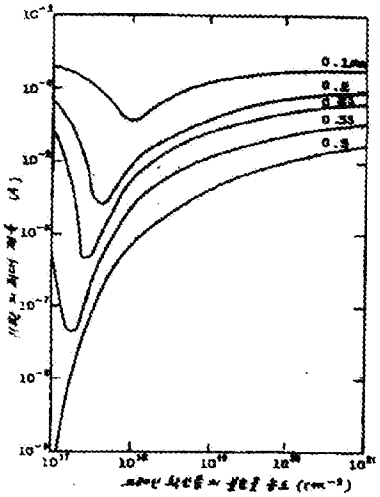


도면13

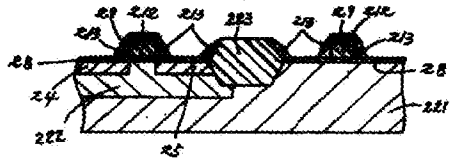


GF Exhibit 1124 - 1894/2704

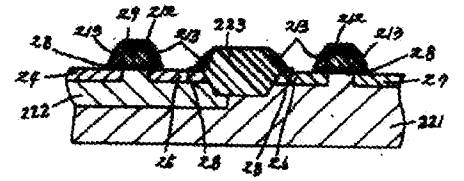
도면14



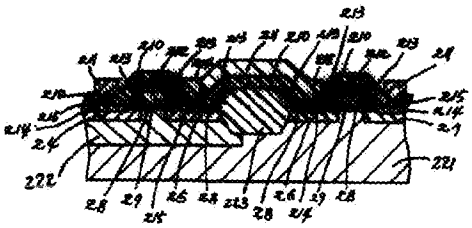
도면15



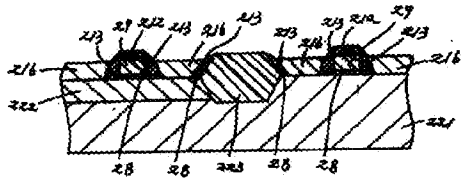
도면16



도면17

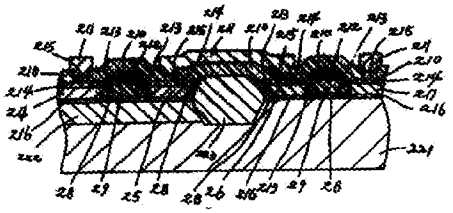


도면18

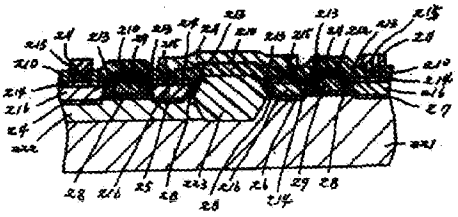


GF Exhibit 1124 - 1895/2704

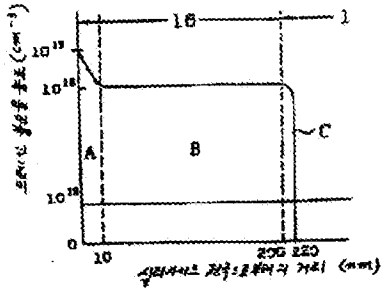
도면19



도면20



도면21



GF Exhibit 1124 - 1896/2704

Bibliographic Data

Int.Cl.	H01L 29/78
Published Date	19910817
Registration No.	1000465640000
Registration Date	19911202
Application No.	1019840001637
Application Date	19840329
Unexamined Publication No.	1019840008537
Unexamined Publication Date	19841215
Priority Claims	58-55075 | 19830401 | JP 58-121185 | 19830704 | JP
Requested Date of Examination	19880629
Agent.	PAIK, Nam Ki
Inventor	HoRiUJiMaSaDaTa | YaMaGuJiGen
Applicant	HITACHI, LTD.
Rightholder	HITACHILTD CO., LTD

발명의 명칭

반도체장치

Title of Invention

Semiconductor device.

요약

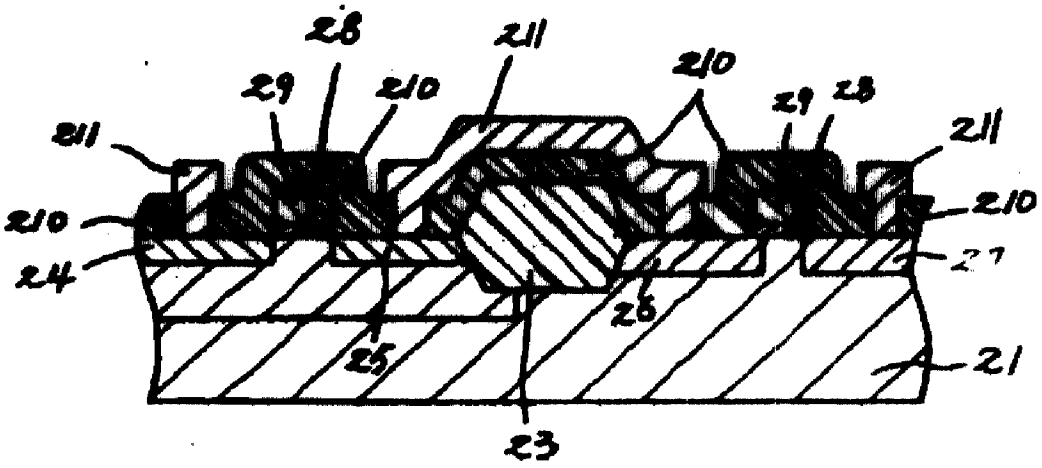
내용 없음.

Abstract

Content none.

대표도면(Representative drawing)

GF Exhibit 1124 - 1897/2704



청구의 범위

청구 1항:

전계 효과 트랜지스터에 있어서, 반도체 기판(1)과 반대 도전형의 드레인(5) 또는 소오스(6) 영역에 있어서 최대 불순물 농도가 1018㎝-3이상 1020㎝-3미만으로 구성되고, 상기 드레인 또는 소오스 영역표면의 적어도 일부는 고융점 금속층 또는 그 실리사이드층(12)와 50㎚을 초과하지 않는 두께를 갖는 높은 불순물 농도 영역(16)으로 되는 높은 도전층과 접하고 있는 것을 특징으로 하는 반도체 장치.

청구 2항:

특허청구의 범위 제1항은 기재의 전계 효과 트랜지스터에 있어서, 상기 높은 도전층이 고융점 금속층 또는 그 실리사이드층(12)만으로 구성되어 있는 것을 특징으로 하는 반도체 장치.

청구 3항:

특허청구의 범위 제1항은 기재의 전계 효과 트랜지스터에 있어서, 상기 드레인(5) 또는 소오스(6)영역의 적어도 일부가 게이트 전극(4)아래에 존재하는 것을 특징으로 하는 반도체 장치.

청구 4항:

특허청구의 범위 제1항은 기재의 전계 효과 트랜지스터에 있어서, 상기 드레인(5) 또는 소오스(6)영역의 적어도 한쪽이 적어도 2회의 이온 주입에 의해서 형성되는 것을 특징으로 하는 반도체 장치.

청구 5항:

특허청구의 범위 제3항 기재의 전계 효과 트랜지스터에 있어서, 상기 게이트 전극(4)가 Mo 박막 또는 실리콘 박막으로 구성되는 것을 특징으로 하는 반도체 장치.

청구 6항:

Scope of Claims

Claim 1:

The semiconductor device the maximum impurity concentration consists of 10 20 ㎝ - 3 under as to the field effect transistor as to the drain (5) of the semiconductor substrate (1) and opposite conductive or the source (6) domain over 10 18 ㎝ - 3 ; and for contacting with the high conductive layer consisting of the high concentration domain of impurities (16) having the thickness in which at least a part of the drain or the source area surface does not exceed the metal layer or the silicide layer (12) and 50㎚.

Claim 2:

The semiconductor device in which the above-mentioned high conductive layer the scope of claims claim 1 consists of the metal layer or the silicide layer (12) as to the field effect transistor of the material.

Claim 3:

The semiconductor device in which the scope of claims claim 1 at least a part of the drain (5) or the source (6) domain exists as to the field effect transistor of the material under the gate electrode (4).

Claim 4:

The semiconductor device in which the scope of claims claim 1 at least one side of the drain (5) or the source (6) domain is formed by the ion implantation of at least two times as to the field effect transistor of the material.

Claim 5:

The gate electrode (4) as to the field effect transistor of the scope of claims claim 3 material is the Mo thin film or the semiconductor device for consisting of the silicon thin film.

Claim 6:

GF Exhibit 1124 - 1898/2704

특허청구의 범위 제3항 기재의 전계 효과 트랜지스터에 있어서, 상기 게이트 전극(4)의 측벽부에 비유전율이 실리콘 산화막 보다 높은 게이트 측벽 절연막(19)를 형성하여 되는 것을 특징으로 하는 반도체 장치.

The semiconductor device for the relative permittivity forming the gate sidewall insulation film (19) higher tha n the silicon oxide film on the sidewall part of the gate electrode (4) as to the field effect transistor of the sc ope of claims claim 3 material and becoming.

청구 7항:

Claim 7:

특허청구의 범위 제6항 기재의 전계 효과 트랜지스터에 있어서, 상기 측벽 절연막(19)를 실리콘 질화막으로 구성한 것을 특징으로 하는 반도체 장치.

The semiconductor device for organizing the side wall insulating film (19) on the silicon nitride film as to the fi eld effect transistor of the scope of claims sixth claim materials.

청구 8항:

Claim 8:

불순물 확산 영역의 최대 불순물 농도가 1018 내지 1020㎝-3 정도의 N형 드레인(24) 또는 소오스 영역(25)와 최대 불순물 농도가 1017 내지 1019㎝-3정도의 P형 드레인(26) 또는 소오스 (27)영역을 가지며, 또 상기 각 드레인 또는 소오스 영역의 적어도 일부가 고융점 금속 또는 금속의 실리사이드층(214)와 접합되어 구성되고 있는 것을 특징으로 하는 반도체 장치.

The semiconductor device N type drain (24) of 10 18 to about 10 20 ㎝ - 3 or the source area (25) and maxi mum impurity concentration of the maximum impurity c oncentration of the impurity diffusion region has the P- type drain (26) of 10 1 7 to about 10 19 ㎝ - 3 or the s ource (27) domain ; and for and, at least a part of eac h drain or the source area being welded to the silicide l ayer (214) of the high melting point metal or the metal and being formed.

청구 9항:

Claim 9:

특허청구의 범위 제8항에 있어서, 상기 각 드레인(24, 26) 또는 소오스 (25, 27)영역의 일부는 반도체 기판 표면 위에 절연막(28)을 거쳐서 구성된 게이트 전극(29)와 상기 게이트 전극의 측벽에 형성된 절연막(213)을 거쳐서 인접해서 형성되는 반도체 장치.

The semiconductor device for the part of each drain (24, 26) or the source (25, 27) domain being adjacent as to the scope of claims eighth claim after the insulati ng layer (213) formed on the surface of semiconductor substrate after the insulating layer (28) in the sidewall of the gate electrode and the formed gate electrode (2 9) and being formed.

청구 10항:

Claim 10:

특허청구의 범위 제 8항에 있어서, 상기 N형 드레인(24) 또는 소오스(25)영역은 고융점 금속 또는 그 실리사이드층(214) 바로 아래의 불순물 석출영역(A), 실리콘박막(216)내부의 균일한 분포의 영역(B), 급격한 농도 분포 영역(C)의 3개의 불순물 농도 분포 영역을 수직 방향으로 갖고 있는 반도체 장치.

The semiconductor device in which N type drain (24) or the source (25) domain has the high melting point meta l or the silicide layer (214), immediately, the following i mpurity precipitation domain (A), the domain (B) of the uniform distribution of the silicon thin film (216) inside, and the impurity concentration distribution domain of 3 of the sudden concentration distribution domain (C) to that as to the scope of claims eighth claim in the verti cal direction.

청구 11항:

Claim 11:

특허청구의 범위 제9항에 있어서, 상기 각 드레인(24, 26) 또는 소오스(25, 27)영역의 일보는 다결정 박막 또는 비정질 박막(216)으로 형성되는 반도체 장치.

The semiconductor device in which the step of each drain (24, 26) or the source (25, 27) domain is formed as to the scope of claims ninth claim into the polycryst alline thin film or the amorphous thin film (216).

상세설명

Detailed Description

[발명의 명칭]

[Title of invention]

반도체 장치

Semiconductor device.

[도면의 간단한 설명]

[Brief description of drawings]

GF Exhibit 1124 - 1899/2704

제1도는 종래의 CMOS를 도시한 단면도.

Figure 1 is a cross-sectional view showing the conventional CMOS.

제2도는 A는 종래의 이중 드레인 구조를 갖는 MISFET의 단면도.

The cross-sectional view of MISFET in which figure the second A has the drain structure among the conventio nal this.

제3도는 BSMS 제2도의 A의 MISFET의 반도체 표면의 불순물 농도 분포와 그에 있어서의 전계를 해석한 것은 도시한 도면.

Drawing illustrated figure the third interprets the electric field in the impurity concentration distribution o f the semiconductive surface of MISFET of A of the BS MS second drawing and that.

제3도~제6도는 본 발명의 제1의 실시예의 제조 공정을 순으로 도시한 단면도.

The cross-sectional view in which the third figure the sixth shows the manufacturing process of the first emb odiment of the invention to the net.

제7도는 본 발명의 제2의 실시예의 단면도.

Figure the seventh is the cross-sectional view of the embodiment of the second of the invention.

제8도는 본 발명의 제3의 실시예의 단면도.

Figure the eighth is the cross-sectional view of the embodiment of the third of the invention.

제9도는 본발명의 제1의 실시예의 특성을 도시한 도면.

Figure 9 is a drawing showing the property of the first embodiment of the invention.

제10도는 본 발명의 제4의 실시예의 단면도.

Figure the tenth is the cross-sectional view of the embodiment of the fourth of the invention.

제11도는 본 발명의 제5의 실시예의 단면도.

Figure the eleventh is the cross-sectional view of the embodiment of the fifth of the invention.

제12도는 본 발명의 제6의 실시예의 단면도.

Figure the twelfth is the cross-sectional view of the embodiment of the sixth of the invention.

제13도, 제14도는 본 발명의 제7~제9의 실시예의 특성을 표시한 도면.

Drawing in which the thirteenth figure the fourteenth indicates the property of the embodiment of 7~ ninth o f the invention.

제15도~제17도는 본 발명의 제7의 실시예를 제조 공정 순서로 도시한 단면도.

The cross-sectional view in which the 15 figure the seventeenth shows the embodiment of the seventh of the invention to the fabrication sequence.

제18도~제19도는 본 발명의 제8의 실시예를 제조 공정 순서로 도시한 단면도.

The cross-sectional view in which the eighteenth figure the nineteenth shows the embodiment of the eighth of the invention to the fabrication sequence.

제20도는 본 발명의 제9의 실시예의 단면도.

Figure the twentieth is the cross-sectional view of the embodiment of the ninth of the invention.

제21도는 본 발명의 제9의 실시예의 드레인의 깊이 방향의 불순물 농도 분포를 도시한 도면.

Figure 21 is a drawing showing the impurity concentration distribution of the longitudinal direction o f the drain of the embodiment of the ninth of the inven tion.

[발명의 상세한 설명]

[Detailed description of the invention]

본 발명은 MISFET에 관하여, 특히 초미세 MISFET의 고내압화에 가장 적합하고, 내 핫 캐리어 효과가 우수한 MISFET에 관한 것이다.

The present invention relates to MISFET in which it is most suitable for especially, the high voltage-resistant of the ultra-fine MISFET about MISFET and my hot carr ier effect is excellent.

GF Exhibit 1124 - 1900/2704

또한, 본 발명은 CMOSFET에 관하여, 특히 0.5#956#m 이하의 게이트 길이에 있어서도 5V 전원으로 동작가능한 고내압초미세 CMOSFET에 관한 것이다.

Moreover, the present invention relates to the high voltage-resistant ultra-fine CMOSFET which is operable in the drawing 5V power source about CMOSFET as to especially, the gate length less than 0.5μm.

현재, MIS 전계 효과 트랜지스터(이하MISFET라 한다)는 미세화를 위해 게이트 절연막을 얇게 하여, 소오스와 드레인의 간격을 좁게하고, 또한 소오스와 드레인의 접합을 얕게 하려고 하고 있다.

It makes the gate insulating layer the present , and the metal-insulation-semiconductor field effect transistor (it says to be less than MISFET) thin for the miniaturization and it makes the gap of the drain and source narrow and it makes moreover, the junction of the drain and source shallow.

상기의 경황의 결과, 현재의 MISFET에 있어서의 최대의 문제는 소오스와 드레인 사이의 내압의 저하이다. 드레인 측에서 신장해온 공핍층이 소오스 영역에 도달하기 때문에 생긴 소위, 편치 스루 내압의 저하는 기판 농도를 증가하는 것에 의해 피할 수가 있으나, 그와 같이 하는 것에 의해서 역으로 전자사태 항복내압(avalanche effect break down)이 감소하게 된다. 특히, 게이트, 소오스 및 기판 전압을 영으로 하였을때의 전자사태 항복전압(이하, BVDS라 한다)은 게이트 전압에 의해서 기판표면 전위의 증가가 억제되기 때문에 젖합 내압에비해서 극단으로 저하해 버린다. 그 결과, 찬넬 길이 1#956#m, 게이트 산화막의 두께20nm, 소오스 드레인 접합 깊이 0.35#956#m인 미세 MISFET의 소오스와 드레인 사이의 내압은 약6V로 통상의 전원 전압5V에 거의 일치할때까지 저하한다. 상기와 같이 미세 트랜지스터에 있어서는 전원 전압의 변동에 의해 간단히 파괴된다.

The result of the state of things described in the above , and the problem of the maximum in the current MISFET are the degradation of the internal pressure between the source and the drain. By the result of that the degradation of the so-called piece value slew internal pressure which is generated because the depletion layer has been extend in the drain section reaches the source area increases the substrate concentration it can avoid. But the electron avalanche breakdown internal pressure (avalanche effect break down) reduces by doing like that. Especially, because the increase of the substrate surface electric potential is suppressed by the gate voltage the electron avalanche breakdown voltage (it the hereinafter says to be the BV DS) when having gate, and the source and substrate voltage as zero is degraded in comparison with the breast sum total internal pressure to extreme. Consequently, the channel length 1μm, the thickness 20nm of the gate oxidation film , and the internal pressure between the source of the minute MISFET and the drain which is the source drain conjugation depth 0.35μm are degraded until it nearly coincides with the normal power supply voltage 5V to about 6V. As described above, it is in the minute transistor and it is simply destroyed by the change of the power supply voltage.

따라서, 종래의 미세 MISFET에 있어서는 상기의 결점을 극복하기 위해 드레인 구조에 관하여 0.2#956#m 정도의 얕은 접합 깊이를 갖는 고농도 불순물 확산층과 0.35#956#m 정도의 보다 깊은 접합깊이를 갖는 저농도 불순물확산층을 조합시키는 소위, 이중 드레인 구조를 채용하고 있다. 상기 구조에의 BVDS 값을 약 1.5내지 2V 향상시킬 수가 있다. 그러나, 상기의 개량된 미세 MISFET에 있어서는 전원 전압의 변동에 의한 파괴로부터 통상 피할 수가 있다. 그러나, 상기의 개량된 미세MISFET에 있어서도 신뢰성의 관점에서는 아직까지 만족할 수가 없었다.

Therefore, the drain structure is employed among the so-called this combining the highly doped impurity diffusion layer which has the shallow junction depth of about 0.2μm about the drain structure in order to be in the conventional minute MISFET and overcome the defect described in the above, and the lightly doped drain implant diffusion layer having the junction depth which is more deep of about 0.35μm. The BV DS value of the structure can be improved with about 1.5 through 2V. But it is in the improved minute MISFET described in the above and generally it can avoid from the break down by the change of the power supply voltage. But in the viewpoint of the reliability as to the improved minute MISFET described in the above, it could not be so far satisfied.

즉, 통상 조건의 장기간 동작에 있어서는 드레인 근방에 있어서의 강한 전계 효과에 의해 핫 케리어(hot carrier)가 게이트 절연막중에 주입되어 임계 전압 값의 변동, 또 표면준의 밀도의 증대 및 전달 콘덕턴스의 저항 등의 열화가 생긴다.

That is, generally, the deterioration including the resistance of the transfer conductance and increase in the change of the threshold voltage value, and, the density of the Pyo MyeonJun it is in the long period operation of the condition and the hot carrier is injected with the strong field effect in the drain neighborhood among the gate insulating layer etc. comes up.

또, 이상은 MISFET의 단일체에 관한 것이지만, 2개 이상의 트랜지스터를 조합해서 구성한 CMOS(Complementary Metal Oxide Semiconductor) 구조에 있어서도 대략 마찬가지로 적

And over relates to the monolith of MISFET, but it is applied as to the CMOS (Complementary Metal Oxide Semiconductor) structure of assembling at least 2 transi

GF Exhibit 1124 - 1901/2704

용된다. 또, CMOS에서는 다음의 문제도 갖고 있다.

stors and configuring to approximately, the likeness. And in CMOS, the following problem has.

여기서, CMOS는 P 찬넬 MOS(이하 PMOS라 한다)와 N 찬넬 MOS(이하 NMOS라 한다)를 쌍으로 해서 동일칩 위에 형성하고 있는 구조이다.

Here, CMOS is P channel MOS (it the hereinafter says to be PMOS) and the structure of N channel MOS (it the hereinafter says to be NMOS) being to pair and forming on the same chip.

제1도는 2#956#m 이상의 게이트 길이를 갖는 종래의 CMOS의 단면 구조도이다.

Figure 1 is a sectional configuration of the conventional CMOS having the gate length more than 2μm.

제1도에 있어서 (21)은 N 도전형의 반도체 기판, (22)는 반도체 기판(21)내에 형성된 P 도전형의 확산층 영역으로 웰이라 한다. (23)은 필드 산화막, (24) 및 (25)는 웰(22)내에 형성된 NMOS의 소오스 및 드레인 확산층 영역으로 n 도전형을 가지며, 그 최대 불순물 농도는 1020cm-3이상으로 구성된다. (26) 및 (27)은 PMOS의 소오스 및 드레인 확산층 영역으로 P 도전형을 가지며, 그 최대 불순물 농도는 1019cm-3이상으로 구성된다. (28) 및 (29)는 각각 게이트 절연막 및 게이트 전극이다. (210) 및 (211)은 각각 보호절연막 및 소오스 또는 드레인 전극이다.

(21) is done by the diffusion layer area of P conductivity type in which the semiconductor substrate of N conductivity type , and (22) is formed within the semiconductor substrate (21) as to Figure 1 because of being the well. (23) has the n conductivity type to the source and drain diffusion layer domain of NMOS in which the field oxide film , and (24) and (25) are formed within the well (22) and the maximum impurity concentration is formed over 10 20 cm - 3 . (26) (27) has P conductivity type to the source and drain diffusion layer domain of PMOS and the maximum impurity concentration is formed over 10 19 cm - 3 . (28) The respectively (29) is the gate insulating layer and gate electrode. (210) The respectively (211) is the protective insulator film and source or the drain electrode.

이와 같은 드레인 확산층의 불순물농도 구성을 갖는 종래 구조의 CMOS에 있어서는 소자의 미소화에 따라서 여러 가지의 결점이 발생한다.

It is in CMOS having the impurity concentration configuration of this kind of drain diffusion layer of the conventional structure and the defect of the various is generated according to the submicron of the device.

(i) 소오스와 드레인 사이의 내압 저하, 즉 소자가 미소화 되는데 따라 찬넬 길이가 감소하기 때문에 펀치 스루 내압이 저하한다. 펀치 스루 내압의 향상은 기판 농도를 증가하는 것에 의해 달성할 수 있으나, 기판 농도의 증가는 역으로 전자사태 항복 내압이 저하하여 버린다. 찬넬 길이가 0.3#956#m 이하의 매우 미소한 NMOS에 있어서는 소오스와 드레인 사이의 내압이 2V이하로 현저하게 저하하기 때문에 통상의 전원 전압의 5V로서는 동작이 불가능하다.

(i) Because the channel length decreases as the internal pressure degradation between the drain and the source, in other words, the device become microscopic the punch-through breakdown voltage is degraded. It can achieve by the result of that the improvement of the punch-through breakdown voltage increases the substrate concentration. But the increase of the substrate concentration the electron avalanche breakdown internal pressure is reversely degraded. Because it is in NMOS which is very minute less than 0.3μm and the internal pressure between the drain and the source of the channel length is remarkably degraded less than 2V the operation is impossible as 5V of the normal power supply voltage.

그리고, 편치 수루 내압의 향상을 위해서 기판 농도를 증가하면, 찬넬 콘덕턴스 gm의 감소를 수반하기 때문에 MISFET이 미세화에 의해 얻어지는 고속 동작 특성은 저해된다.

And if the substrate concentration is increased for the improvement of the piece value *** internal pressure , because the reduction of the channel conductance gm is accompanied the high speed operation characteristic that MISFET is obtained with the miniaturization is hindered.

(ii) 래치 업에 의한 MISFET의 파괴, 즉 종래 구조를 갖는 CMOSFET의 최대의 결점은 래치업이라고 부르는 사이리스터(thyristor) 동작에 기인하는 MISFET의 파괴이다. 이 래치 업 현상은 특히 CMOSFET의 미세화에 따라서 현저하게 된다. 즉,

(ii) It is the break down of MISFET by the latch up, and the break down of MISFET in which the defect of the maximum of CMOSFET having in other words, the conventional structure is caused by the thyristor operatio

GF Exhibit 1124 - 1902/2704

NMOS와 PMOS사이의 거리가 근접된 CMOSFET에 있어서는 NMOS의 드레인(25), 웰(22),반도체 기판(21) 및 PMOS의 소오스(26) 또는 드레인 (27)사이에 NPNP 구조를 갖는 기생 사이리스터가 형성된다. 상기의 사이리스터는 과전압의 인가, 통상 스위치 동작중의 내부과도적 과전압의 발생, 또는 광이나 방사선의 조사에 기인하는 소수 캐리어의 유기 등에 의해 유발되어 동작을 개시하고 전원을 정지할때까지 사이리스터 동작을 억제하는 것은 불가능하게 된다. 이 사이리스터 동작에 기인하여 과대 전류가 CMOSFET에 흐르기 때문에 CMOSFET는 파괴된다.

n of calling as the latch up. This latch-up is significant according to especially, the miniaturization of CMOSFE T. That is, in CMOSFET in which the distance between PMOS and NMOS are near and the parasitic Thyristor h aving the NPNP structure is formed between the drain (25) of NMOS, the well (22), and the source (26) of th e semiconductor substrate (21) and PMOS or the drain (27). Generally the thyristor described in the above is i mpossible with the approval of the overvoltage to supp ress the thyristor operation until it is caused by the org anic of the minority carrier caused by the investigation of the generation of the inside transient overvoltage a mong the switch operation or the light or radiation etc. and the operation is disclosed and the power source is readjusted. CMOSFET is destroyed because the overcu rrent flows due to this thyristor operation in CMOSFET.

상기의 사이리스터 동작은 CMOSFET의 미세화에 따라서 웰(22)와 PMOS의 간격이 축소되어 기생 PNP 바이폴라 트랜지스터 및 기생 NPN 바이폴라 트랜지스터의 각각의 전류 이득률의 곱이 1보다 크게 되기 때문에 발생한다는 것이 알려져 있다.

According to the thyristor operation described in the above is the miniaturization of CMOSFET, it is known th at the gap is generated because the gap of PMOS and well (22) is reduced and it becomes the double of each current gain modulus of the parasitism PNP bipolar tran sistor and parasitism NPN bipolar transistor than 1.

상기의 각 기생 바이폴라 트랜지스터에 있어서의 전류 이득률의 곱을 갖게 하는 것에 의해 사이리스터 동작을 저지하는 방법이 제안되고 있다. 즉, P+N 접합으로 형성된 제1도에 도시한 종래 구조 PMSO의 소오스(26) 및 드레인(27)을 쇼트기 접합로 치환한 CMOSFET 구조가 1982년도 국제 전자 장치 학회(International Electron Devices Meeting) 예고집 462페이지에 기재되어 있다. 상기의 #8220#쇼트키 장벽 PMOS에 의한 CMOS 래치 업 현상의 해결(CMOS latch-up elimination using schottky barrier PMOS)#8221#라고 하는 보고서에서는 쇼트키 접합에 있어서의 소수 캐리어 주입 효율이 P+N접합의 것과 비교해서 대단히 작은 사실을 이용해서 기생 PNP 바이폴라 트랜지스터의 전류 이득률을 P+N 접합에 의한 종래 구조의 것과 비교해서 1/100 이하로 까지 저하시키는 것에 의해 래치 업 현상을 해결하고 있다.

The method for interrupting the thyristor operation by making have the double of the current gain modulus in each parasitic bipolar transistor described in the above is proposed. That is, the CMOSFET structure of substit uting for the source (26) and drain (27) of the convent ional structure PMSO shown with the P+N junction in f ormed Figure 1 with the shot machine bonding furnace 1982 year is written in the international electronic devi ce learned society (International Electron Devices Meet ing) preview collection 462 page. In the report done as the resolution (CMOS latch-up elimination using schott ky barrier PMOS) " of the CMOS latch-up by the " Scho ttky barrier PMOS described in the above, by comparin g with of the P+N junction and the minority carrier inje ction efficiency in the Schottky barrier using the fact t hat is very small and the current gain modulus of the p arasitism PNP bipolar transistor being compared with of the conventional structure by the P+N junction and lo wering to 1/100 less than furnace the latch-up is solve d.

P+N 접합대신에 쇼트키 접합으로 소오스 접합 및 드레인 접합을 형성하는 상기의 CMOSFET에 있어서 래치 업 현상은 방지되지만, 쇼트키 접합 특유의 결점이 존재한다. 즉, 쇼트키 접합을 사용한 CMOSFET에 있어서는 드레인 접합누설 전류가 큰 것, 비선형 출력으로 되어 옴접촉 특성을 얻을 수 없는 것 및 전달 콘덕턴스가 낮기 때문에 충분한 전류가 확보되지 않아 고속 동작을할 수 없는 것 등의여러 가지의 결점이 있다.

The latch-up is prevented as to the CMOSFET described in the above forming the source junction and drain junction on the P+N splicer into the Schottky bar rier. However the defect of the Schottky barrier charac teristic exists. That is, in CMOSFET using the Schottky barrier and, and the current enough because it consist s of the non-linear output and it cannot obtain the oh mic contact property the transfer conductance is low a re not secured and the drain junction leakage current i s large it there is no with the high speed operation num ber it has the defect of the tergal various.

쇼트키 접합에 따른 상기의 결점은 그후 제한된 #8220#저농도 불순물 확산을행한 쇼트키 트랜지스터 (blightly doped schottky MOSFET)#8221#에 의해 해결할 수가 있다. (1982년도 국제 전자 장치 학회 예고집, 466페이지 참조). 즉, 상기 쇼트키 트랜지스터에 있어서는 낮은 불순물 분포의 드레인 영역 위에 쇼트키 접합을 형성하면, 드레인 접합의 누설 전류가

It can solve with the schottky transistor (blightly doped schottky MOSFET) " done with the " lightly dope d drain implant diffusion row thereafter the defect desc ribed in the above according to the Schottky barrier is l imited. (1982 year is the international electronic device learned society preview collection, 466 page reference)

GF Exhibit 1124 - 1903/2704

작게할 수가 있고, 또한 전달 콘덕턴스도 통상 구조의 PMOS의 그것에 가깝게 할 수가 있다.

If it is in other words, the schottky transistor and the Schottky barrier is formed on the drain region of the lo w impurity distribution , it makes small and it makes ne ar to that of PMOS of the trading structure.

그러나, 낮은 불순물 농도 드레인 확산층과 쇼트키 접합을 조합시킨 구조에 의해 CMOSFET를 구성하는 방법에도 다음과 같은 결점이 존재한다. 즉, 상기의 문헌#8220#CMOS latch-up elimination using schottky barrier PMOS#8221#에도 기재되어 있는 바와 같이 NMOS의 소오스 접합 및 드레인 접합을 쇼트키 접합으로 형성한 경우에 있어서의 기생 NPN 바이폴라 트랜지스터의 전류 이득률은 N+P 접합에 의해 드레인 접합을 형성한 종래 구조에 있어서의 기생 NPN 바이폴라 트랜지스터의 전류 이득률에 비해서 최대 10배나 크게 되는 것이다. 이에 따르면, 낮은 불순물 농도를 갖는 드레인 확산층의 유무에 관계없이 쇼트키 접합으로 PMOS 및 NMOS를 형성한 CMOS 트랜지스터는 PMOS의 소오스 접합 및 드레인 접합을 쇼트키 접합으로 형성하고, NMOS의 각 접합은 통상의 N+P접합으로 형성한 CMOS트랜지스터보다 래치 업 현상이 생기기 쉽다는 결점이 있다.

But the defect as follows exists in the method for configuring CMOSFET with the low impurity concentrati on drain diffusion layer and the structure of combining the Schottky barrier. That is, it as described in the liter ature "CMOS latch-up elimination using schottky barrie r PMOS" described in the above is large in comparison with the current gain modulus in which the current gain modulus of the parasitism NPN bipolar transistor forms t he drain junction with the N+P junction it has in case o f forming the source junction and drain junction of NMO S into the Schottky barrier of the parasitism NPN bipola r transistor in the conventional structure as the maxim um factor of ten. According to this, the CMOS transist or forming PMOS and NMOS into the Schottky barrier re gardless of the occurrence of the drain diffusion layer h aving the low impurity concentration forms the source j unction and drain junction of PMOS into the Schottky b arrier and it has the defect that it is easy than the CM OS transistor which each junction of NMOS forms into t he normal N+P junction that the latch-up is generated.

쇼트키 접합에 의한 래치 방지에 관한 상기 2건의 문헌에 의하면, 낮은 불순물 농도 분포를 갖는 소오스 영역 및 드레인 영역의 각 표면에 쇼트키 장벽을 형성한 PMOS와 옹상의 높은 불순물 농도를 갖는 소오스 확산층 및 드레인 확산층이 형성된 NMSO의 조합에 의해 CMOS 트랜지스터를 구성하는 것이 래치업 방지의 관점에서 가장 바람직한 것이된다.

According to the literature of 2 cases about the latch prevention by the Schottky barrier, it do in the viewpoi nt of the latch-up protection with desirable to arrange the CMOS transistor by the combination of NMSO in wh ich the drain diffusion layer is formed and the source di ffusion layer having the high impurity concentration on PMOS forming the Schottky barrier on each surface of the drain region and the source area having the low im purity concentration distribution and NULL.

그러나 , 상기 2건의 문헌 및 그들의 조합에 의해 얻어지는 결론은 CMOS 트랜지스터의 래치 업 방지의 관점에서만 성립하는 것으로서 CMOS 트랜지스터의 미세화에 따른 NMOS 및 PMOS의 내압 저하에 관한 상술한 결점에 대해서는 아무런 해결 방법도 제안되어 있지 않았다.

But the outcome obtained with literature and their combinations of the , 2 cases was established in the vi ewpoint of the latch-up protection of the CMOS transis tor and any solution was not proposed about the abov e-described defect about the internal pressure degrada tion of NMOS according to the miniaturization of the C MOS transistor and PMOS.

특히 , 찬넬길이가 0.5#956#m이하의 초미세 CMOS 트랜지스터에 관해서는 상기 2건의 문헌에는 아무런 기재도 없고, 상술의 결점에 대해서는 전혀 해결 방법이 없다.

Especially, in the , channel length is the literature of 2 cases about the ultra-fine CMOS transistor less than 0.5μm, any material does not have and there is no solu tion about the defect of the detailed description at all.

본 발명의 목적은 소오스와 드레인 사이의 내압이 통상의 전원 전압에 비해 충분히 높고, 핫 케리어 주입에 따라 특성 열화가 생기지 않는 초미세 MISFET를 제공하는데 있다.

As to the object of the present invention, the internal pressure between the drain and the source are enough high in comparison with the normal power supply voltag e and the ultra-fine MISFET in which the characteristic deterioration is not generated according to the hot car rier injection is to be provided.

본 발명의 다른 목적은 상기와 같은 종래의 결점을 해소하고, 극히 짧은 찬넬 길이로도 통상의 전원 전압으로 동작하고, 또한 래치 업 현상도 방지할 수 있는 CMOSFET를 제공하는데 있다.

Another object of the invention is to provide CMOSFET which it cancels the above-mentioned conventional def ect and it operates to the channel length which is exce edingly short to the normal power supply voltage and m oreover, the latch-up can prevent.

본 발명은 종래의 이중드레인 구조의 가장 적합한 조건의 검토에 있어서, 특히 얕은 접합깊이를 갖는 고농도 불순물분포 영역

As for the review of the condition that is most suitable of the conventional duplication drain structure of the in

GF Exhibit 1124 - 1904/2704

이 완수하는 역할에 착안하여 해석한 결과에 기인한다. 제2도 A는 종래하여금 이중드레인 구조를 갖는 MISFET의 단면도이다. 제2도 A에 있어서 (1)은 P형 반도체 기판, (2)는 필드 산화막, (2)은 게이트 산화막, (5)~(8)은 게이트 전극(4)를 확산 마스크로서 형성한 n형 불순물 영역으로 (5) 및 (7)은 드레인 확산층 (6) 및 (8)은 소오스 확산층이다. 여기서 (5) 및 (6)은 낮은 불순물 농도 확산층이며, 표면 불순물 농도를 Cs2, 접합 깊이를 Xj2로 정의한다. (7) 및 (8)은 높은 불순물 농도 확산층이며, 표면 불순물 농도를 Cs1, 접합 깊이를 Xj1로 정의한다. (9) 및 (10)은 각각 드레인 전극, 소오스 전극이다. 제2도 B는 제2도 A의 MISFET의 반도체 표면에 있어서 드레인 확산층 끝에서 소오스 확산층 측으로의 거리의 함수로서의 불순물 농도 분포가 거기에 있어서의 전계를 해석한 대표적인 결과다. 제2도 B는 실효 찬넬 길이가 1.1#956#m, 게이트 산화막(3)의 막의 두께가 20nm, Xj1이 0.25#956#m, Xj2가 0.3#956#m, Cs1이 1#215#1021cm-3, Cs2#215#1019cm-3의 경우이고, 게이트 전극(4) 및 드레인 전극(9)에 인가한 전압은 각각0V 및 10V이다.

vention, caused by the result which takes notice of the role that the highly doped impurity distribution area having especially, the shallow junction depth accomplishes and interpreted. The second is the cross-sectional view of MISFET in which A has the conventional women gold duplication drain structure. The second is (1) as to A is the P-type semiconductor substrate, and (2) are the n-impurity area in which the field oxide film , and (2) the gate oxidation film , and (5) ~ (8) form the gate electrode (4) as the diffusion mask (5) and (7) the drain diffusion layer (6) and (8) is the source diffusion layer. Here, it is the impurity concentration diffusion layer in which (5) and (6) are low and the surface impurity concentration the Cs 2 , and the junction depth is defined as the Xj 2 . (7) It is the impurity concentration diffusion layer in which (8) is high and the surface impurity concentration the Cs 1 , and the junction depth is defined as the Xj 1 . (9) The respectively (10) is the drain electrode, and the source electrode. In the second B the second is the drain diffusion layer end as to the semiconductive surface of MISFET of A, it is the typical result in which the impurity concentration distribution as the function of the distance to the source diffusion layer interprets the electric field in the there. The second is B is the effectiveness channel length is 1.1μm, and the voltage which 0.3μm, and the Cs 1 of 0.25μm, and the Xj 2 of 20nm, and the Xj 1 of the thickness of the film of the gate oxidation film (3) is in case of 1× 10 21 cm − 3 , and the Cs 2 × 10 19 cm − 3 and it applies in the gate electrode (4) and drain electrode (9) are 0V and 10V.

제2도 B에서 명확한 바와 같이 드레인 전압의 인가에 의해 반도체 표면에 있어서, 최대 전계는 불순물농도가 1018cm-3부근에 있어서의 드레인 확산층 내부에서 형성되고, 불순물 농도가 보다 높은 드레인 확산층(7)내에서는 전계가 보다 작게 되어 가는 것을 알 수 있다. 본 발명은 이러한 해석 결과, 높은 불순물농도 확산층(7) 내에 있어서하여금 전계가 보다 작게 되어 가는 것을 알 수 있다. 본 발명은 이러한 해석 결과, 높은 불순물농도 확산층(7)내에 있어서의 전계의 급격한 저하 경향에 착안한 것에 기안한다.

As to the maximum electric field, the impurity concentration is formed by the approval of the drain voltage as to the semiconductive surface within the drain diffusion layer in 10 18 cm − 3 vicinity as the second been clear and accurate in B than and the impurity concentration can know in the higher drain diffusion layer (7) that the electric field is smaller. The invention can know within such interpretation result , and the high impurity concentration diffusion layer (7) Ha YeoGeum, that at the electric field is smaller with ***. The invention takes notice of such interpretation result , and the degradation tendency to be rapid of the electric field in the high impurity concentration diffusion layer (7) in it drafts.

즉, 상기의 결과는 종래의 이중 드레인 구조의 MISFET에 있어서 상기 영역(7)이고, 내압화에 관해 거의 기여하고 있지 않다고 생각할 수 있다. 상기 개념에 따르면, 미세 MISFET의 고내압화의 관점에서 높은 불순물 농도 확산층의 존재는 도리어 장해로 되고 있으며, 드레인 확산층을 낮은 불순물 농도 확산층으로 구성하는 것이 바람직하다고 생각된다.

That is, the result described in the above is the domain (7) among the conventional this as to MISFET of the drain structure and it can think that it nearly does not contribute about the resisting voltage. According to the concept, the high presence of the impurity concentration diffusion layer rather consists of the failure in the viewpoint of the high voltage-resistant of the minute MISFET and it is sweet with be desirable and it is the drain diffusion layer regarded as the low impurity concentration diffusion layer to configure.

그러나 , 상기의 개념은 종래에 실시되어 있지 않는다. 이것은 종래의 드레인 확산층이 높은 불순물 농도 확산층으로 구성되는 것이라는 고정 개념에서 벗어나지 못했기 때문이고, 따라서 이중 드레인 구조에 있어서도 높은 불순물 농도 확산층의 존재는 불가피하다라고 생각하였기 때문이다.

But it was not contrary to the fixing concept the concept of the , the above was not performed on the convention that this consisted of the impurity concentration diffusion layer in which the conventional drain diffusion layer was high and it was due to think among this as to the drain structure that the high presence of the impurity concentration diffusion layer was inevitable.

GF Exhibit 1124 - 1905/2704

상기의 관점에 따라서 이중 드레인 구조에 있어서의 높은 불순물 농도 확산층(7) 및 (8)의 역할을 보면, 상기 영역(7) 및 (8)은 단지 전극(9) 및 (10)과의 옴접촉의 확보 및 소오스 및 드레인 영역의 확산층 저항의 저감화 이외는 아무런 역할에서도 하고 있지 않는 것은 명확하다. 한편, 소오스 및 드레인 영역의 확산층저항에 관해서는 백금 등의 실리사이드를 확산층 위에 형성하는 종래 기술에 의해 통상의 높은 불순물 농도확산층에 의한 시이트 저항값 50Ω/cm3를 3!&/cm2이하의 1/10 이하로 까지 저감화 할 수 있는 것이 알려져 있다. 그러나, 상기의 실리사이드 드레인 구조에 있어서는 시이트 저항의 저감 효과에만 착안하고, 소오스와 드레인 사이의 내압의 향상의 관점에서의 검토는 종래에 있어서 행하여지지 않아 드레인 확산층에는 고정 개념에 따라서 1020cm-3이상의 표면 농도를 갖는 높은 불순물 확산층이 사용되어 왔다.

According to the viewpoint described in the above, if the role of the impurity concentration diffusion layer (7) in the drain structure and high (8) are looked at among this , it is clear that the domain (7) and (8) the reduction except of the diffusion layer resistance of the security of the ohmic contact with the electrode (9) and (10) and source and drain region only does not play in any role. In the meantime, what can reduce is the sheet resistance value 50Ω / cm 3 by the high impurity concentration diffusion layer known with the prior art forming the silicide including platinum etc. about the diffusion layer resistance of the drain region and source on the diffusion layer until 1/10 less than furnace less than 3!& / cm 2 . But in the drain diffusion layer the review at the viewpoint of the improvement of the internal pressure between the source and the drain are not performed as to the convention it is in the silicide drain structure described in the above and it takes notice of the reduction effect of the sheet resistance, the high impurity spreading layer having the surface concentration more than 10 20 cm - 3 according to the fixing concept should be used.

본발명은 상기의 고정 개념이 무의미한 것이며, 드레인 확산층, 불순물 분포의 최적화에 의해 소오스 및 드레인 내압의 고내압화와 드레인 전극, 드레인 확산층사이의 양호한 옴접촉, 더 나아가서는 낮은 시이트저항화가 가능하게 된다고 생각하고, 검토한 결과에 따른 즉, 본 발명은 실리사이드 층을 형성하여야 할 드레인 확산층의 표면농도가 1018cm-3이상이면, 실리사이드 층 바로 아래에 표면농도가 1019cm-3정도의 석출층이 10nm 정도 형성되어 실리사이드와 드레인 확산층 사이에 MISFET의 통상동작에 충분한 옴접촉이 확보되는 사실을 발견한 것에 따른다. 또 본 발명은 상기 드레인 확산층의 표면 농도가 1020cm-3이하이면, 소오스와 드레인 사이의 내압을 실효 찬넬 길이 1#956#m 이하의 MISFET에 있어서도 최대 5V 이상 종래의 MISFET에 비해서 고내압화 할 수 있는 것을 발견한 사실에 따른다.

As to the invention, the fixing concept described in the above is meaningless and it thinks that the high voltage-resistant of the source and drain internal pressure and drain electrode, the good ohmic contact between the drain diffusion layer, and the sheet resistance are possible with the drain diffusion layer, and the optimization of the impurity distribution and is morefurther more low if the surface concentration of the drain diffusion layer in which the result, in other words, the invention examined has to form the silicide layer is 10 18 cm - 3 or greater , 10nm gad is formed and the precipitation layer of about 10 19 cm - 3 of the surface concentration discovers the fact that the ohmic contact sufficient in the typical operation of MISFET is secured between the silicide and drain diffusion layer the fact immediately beneath follows. And if the surface concentration of the drain diffusion layer as to the invention, is 10 20 cm - 3 or less , it follows the fact that discovers making the internal pressure between the drain and the source endure high voltage as to MISFET less than the effectiveness channel length 1μm over the maximum 5V in comparison with the conventional MISFET.

본 발명에 의한 CMOSFET는 불순물 확산 영역의 최대 불순물 농도가 1018~1020cm-3정도의 N형드레인 영역과 최대 불순물 농도가 1017~1019cm-3정도의 P형 드레인 영역을 가지며, 또한 상기 각 드레인 영역의 적어도 일부가 고융점 금속 또는 상기 금속의 실리사이드 층과 접합되어 구성되어 있는 것에 특징이 있다.

N type drain domain maximum impurity concentration of about 10 18 ~ 10 20 cm - 3 as to the CMOSFET according to the invention, of the maximum impurity concentration of the impurity diffusion region has the P-type drain region of about 10 17 ~ 10 19 cm - 3 and moreover, at least a part of each drain region is welded to the silicide layer of the refractory or the metal and it is formed it has the characteristic.

다음에 본 발명을 실시예에 따라서 더욱 상세하게 설명한다. 설명의 편의상, 도면을 가지고 설명하지만 주요부를 확대하여 도시하고 있으므로 주의를 한다.

Next, according to the embodiment the invention, more specifically, it illustrates. Since it illustrates having for convenience of the description, and drawing but the main part is augmented and it shows it notes.

[실시예 1]

[Embodiment 1]

제3도~제6도는 본 발명에 의한 MISFET하여금 1실시예의 제

The third is drawing in which Ha YeoGeum, figure the

GF Exhibit 1124 - 1906/2704

조 공정을 공정 순서로 도시한 도면으로서, (1)은 P도전형 비저항 1Ω/cm의 실리콘 기판이다. 반도체 기판(1)표면에 종래의 소자 분리 기술을 이용해서 0.8#956#m의 두꺼운 필드 산화막(2)를 선택적으로 형성한 후, 활성 영역의 반도체 표면을 노출하고, 20nm의 깨끗한 게이트 산화막(3)을 형성한다. 그 후, 약 0.3#956#m하여금 실리콘 박막을 게이트 산화막(3)위에 형성하고, PDC/3을 소오스로 하는 열 확산에 의해 실리콘박막에 인(p)의 고농도 확산을 행한다.

sixth shows the manufacturing process of 1 embodimen t to the processing procedure with MISFET according t o the invention. (1) It is the silicon substrate of the sil ver P conductivity type resistivity 1Ω / cm. The thick fi eld oxide film (2) of 0.8μm the semiconductive surface of the active area is selectively exposed after doing th e formation by using the conventional isolation technol ogy for the semiconductor substrate (1) surface and th e gate oxidation film (3) which is clean of 20nm is form ed. Thereafter, ha YeoGeum, the silicon thin film is for med on the gate oxidation film (3) with about 0.3μm an d the high concentration diffusion of the phosphorus (p) is performed with the thermal diffusion the PDC / 3 t o the source in the silicon thin film.

그 후에, 리도그래피에 의해 게이트 전극(4)를 형성한다. 리도그래피후의 찬넬 길이는 1#956#m이다. 다음에 테트라에톡시실란(Si(OC2H5)4)을 사용한 화학 기상반응에 의해 0.5#956#m의 막의 두께를 갖는 실리콘 산화막(11)을 전면으로 퇴적시킨다. 상기의 퇴적막(11)을 반응성 스퍼터 에칭에 의해 최대기판 표면과 수직 방향으로 에칭을 행하여 평탄부에 퇴적된 실리콘 산화막을 제거하면, 제4도에 도시한 바와 같이 게이트 전극(4)의 측벽에만 실리콘 산화막(11)이 남게된다. 이 상태에서 산화막(3)을거쳐서 비소를 가속 에너지70KeV의 조건에서 이온 주입에 의해 반도체 기판(1) 표면에 주입한다. 상기의 조건은 최대 기판 표면에서 최대 불순물 농도로 되는 조건이다. 본 실시예에 있어서는 주입량을 변수로 하고, 표면 불순물농도가 1#215#1017~1019cm-3의 범위에서 여러 가지의 값을취할 수 있도록 다수개의 MISFET를 작성하였다. 상기의 이온주입 공정후 주입 이온의 활성화의 열처리를 행하였다.

Thereafter, the gate electrode (4) is formed with lithography. The channel length after lithography is 1μ m. Next, the silicon oxide film (11) having the thickness of the film of 0.5μm with the chemical vapor deposition using the tetraethoxysilane (Si(OC(SB)2(/SB)H(SB)5(/S B))(SB)4(/SB)) is sedimented with the front side. As sh own in Figure 4 the heap film (11) described in the abo ve the etching is performed with the reactive sputter e tching into the maximum substrate surface and vertical direction, the silicon oxide film (11) remains in the side wall of the gate electrode (4). In this state, in the con dition of the acceleration energy 70 KeV the arsenic th rough the oxide film (3), it injects into the semiconduct or substrate (1) surface with the ion implantation. In t he condition described in the above is the maximum su bstrate surface, it is the condition consisting of the ma ximum impurity concentration. It was in this embodimen t and the injection amount was to the variable and the surface impurity concentration prepared multiple MISFE Ts in order to have in the range of 1× 10 17 ~ 10 19 c m - 3 with the value number of the various. The therm al process of the activation of the implant ion was perf ormed after the ion implantation process described in t he above.

상기의 열처리는 1000℃에서 행하였지만, 여러가지의 주입량을 갖는 각각의 MISFET에 대해 접합깊이 Xj가 0.25#956#m로 되도록 각각 열처리 시간을 설정하였다. 그후, 드레인 확산층(5) 및 소오스 확산층(6) 위의 게이트 산화막(3)을 제거하고, 50nm의 막의 두께의 백금(Pt)를 전면에 스퍼터링법에 의해 증착한다. 다음에 450℃의 열처리를 하고, 드레인(5), 소오스 확산층(6) 표면 및 게이트 전극(4)표면에 백금 실리사이드(PtSi)(12)를 형성한다.

The thermal process described in the above is for the establishment of the junction depth Xj about each MIS FET which has the injection amount of the various perf ormed in 1000℃ is 0.25μm, as as possible, the thermal processing annealing time. Thereafter, the gate oxidati on film (3) above the drain diffusion layer (5) and sourc e diffusion layer (6) is removed and the platinum (Pt) o f the thickness of the film of 50nm is deposited on fron t with the sputtering method. Next, it heat-treats of 4 50℃ and the platinum-silicide (PtSi) (12) is formed on t he drain (5), and the source diffusion layer (6) surface and gate electrode (4) surface.

상기의 열처리에 있어서 산화막(11) 및 (2) 위에서는 실리콘과의 반응은 일어나지 않아 실리사이드는 형성되지 않는다. 따라서 상기 열처리 공정후, 왕수로 에칭하면 PtSi는 왕수로 에칭되지 않기 때문에 산화막 및 반응하지 않는 Pt만이 제거되고,

Reaction with the silicone on the oxide film (11) as to the thermal process described in the above and (2) ha ve the oxide film it does not occur and the silicide is no t formed if it etches to the aqua regia after the therma

GF Exhibit 1124 - 1907/2704

게이트 전극(4), 드레인 확산층 (5) 침소오스 확산층(6)의 각 표면에 위에만 PtSi가 자기 정합적으로 남게 된다. 여기에 있어서 PtSi 층(12) 바로 아래에는 PtSi 층 형성전의 표면 불순물 농도 보다도 1자리수 높은 불순물 농도를 갖는 약 10nm두께의 석출층(13)이 PtSi 층 (12)와 자기 정합적으로 형성되었다. 상기 석출층(13)내에 있어서의 깊이 방향의 불순물 분포는 깊이에 대해 아래로 볼록한 형상을 갖는다. PtSi 층 (12)의 형성 후, 공지의 기술을 사용해서 보호 절연막(15), 또 드레인 전극(9) 및 소오스 전극(10)을포함하는 배선전극을 바라는 회로 방식에 따라서 형성한다. 상기의 전극(9)(10)에는 알루미늄(Al)의 증착만을 사용하지만, Al이 PtSi 층 (12)와 반응하는 것을 방지하기 위하여 A1배선 공정전에 Ti와 Ta의 동시 스퍼터링에 의해 TiTa 막(14)를 PtSi 막(12)위의 접촉구멍 부분에 사전에 형성한다.

l process, the therefore the PtSi is not etched at the a qua regia and the PtSi layer (12) as to the excitation, i mmediately, the impurity distribution of the longitudinal direction in the precipitation layer (13) is the convex s hape down the depth the precipitation layer (13) of ab out 10nm thickness having the impurity concentration which the single digit was beneath higher than the surf ace impurity concentration of the PtSi layer formation t otal was formed with the PtSi layer (12) and self-align ment manner the PtSi remains in the upper part in the gate electrode (4), and each surface of the drain diffus ion layer (5) sleeping place OSS diffusion layer (6) as t he self-alignment manner it is removed only the Pt whic h does not react. And and it forms according to the cir cuit method wanting the interconnection electrode whi ch the drain electrode (9) and source electrode (10) in clusion is named by using the publicly known technolog y after the formation of the PtSi layer (12). In the elec trode (9) (10) described in the above, it uses only the deposition of the aluminum (Al). However in order to pr event the Al from reacting to the PtSi layer (12), the T iTa film (14) is formed on the contact hole part above t he PtSi film (12) before the A1 interconnection process with the co-sputtering of the Ta and Ti in advance.

상기의 제조 과정을 거쳐서 제조된 각종의 표면 불순물 농도 Cs2를 갖는 드레인 확산층(5)로 구성된 각각의 MISFET의 게이트 전압이 영에서 소오스와 드레인 사이의 내압 BVDS를 측정하였을 때, 제9도의 결과가 얻어졌다. 제9도의 측정에 사용한 각 MISFET는 본 실시예의 제조 과정에서도 명확한 바와 같이 실효찬넬 길이가 1#956#m 게이트 산화막(3)의 막의 두께가 20nm, 드레인 접합 깊이 0.25#956#m의 동일 조건의 것이고, 드레인 확산층(5)의 표면 불순물 농도만이 달라지고 있다. 본 실시예의 각 MISFET에 있어서는 드레인 접합끝이 게이트 전극(4)의 끝과 일치하도록 게이트 측벽 산화막(11)의 막하 여금 두께를 제어하고 있다. 제9도의 결과로 주목되는 것은 드레인 확산층(5)의 표면 불순물 농도가 5#215#1018cm-3부근에서 BVDS값이 최대로 되어 11.5V에 까지 도달하는 것이다.

When the gate voltage of each MISFET consisting of the drain diffusion layer (5) having the various surface i mpurity concentration Cs 2 manufactured after the ma nufacturing process described in the above measured t he internal pressure BV DS between the drain and the s ource in zero , the result of Figure 9 was obtained. As each MISFET used in the measurement of Figure 9 bee n clear and accurate in the manufacturing process of t his embodiment than the thickness of the film of 1μm g ate oxidation film (3) of the effectiveness channel leng th is 20nm, and of the same condition of the drain conj ugation depth 0.25μm and the thickness is changed onl y the surface impurity concentration of the drain diffusi on layer (5). It is in each MISFET of this embodiment a nd the staff-officer women gold thickness of the gate s idewall oxide (11) is controlled so that the drain junctio n end coincides with the end of the gate electrode (4). The BV DS value is maximized in 5× 10 18 cm − 3 vicini ty and the surface impurity concentration of the drain diffusion layer (5) reaches 11.5V to be watched to the result of Figure 9.

상기의 값은 표면 불순물 농도가 1020cm-3이상의 드레인으로 구성되는 동일 접합 깊이를 갖는 종래 MISFET의 BVDS값보다 4.5V 이상이나 높은 내압화가 실현되어 있는 것을 나타내고 있다. 또, 제9도에 있어서 점선으로 표시한 종래의 이중 드레인 구조 MISFET에 있어서 BVDS값의 최대값보다도 본 발명에 의한 MISFET의 쪽이 3.5V 이상이나 높은 내압화가 실현되어 있는 것을 나타내고 있다.

It shows that the resisting voltage which is higher than the BV DS value of the conventional MISFET in which t he value described in the above has the identical juncti on depth in which the surface impurity concentration c onsists of the drain more than 10 20 cm − 3 over 4.5V is realized. And it shows among the conventional this in dicated by the dotted line as to Figure 9 that the resis ting voltage in which the side of the MISFET according to the invention is higher than the maximum value of th e BV DS value over 3.5V is realized as to the drain stru cture MISFET.

그리고, 제9도에 도시한 이중 드레인 구조의 특성은 낮은 불순물 농도 분포(5)의 접합 깊이 Xj2가 0.25#956#m, 표면 불순물 농도 Cs2는 도시한 각각의 값이고, 높은 불순물농도 분포(7)의 접합 깊이 Xj1이 0.15#956#m, 표면 불순물 농도 Cs1

And the property of the drain structure among this shown in Figure 9 relates to MISFET which the junction depth Xj 2 of the low impurity concentration distributio n (5) is each value which 0.25μm , and the surface imp

GF Exhibit 1124 - 1908/2704

은 1#215#1021cm-3의 구성으로 되는 드레인 확산층을 갖는 MISFET에 관한 것이다. 여기에서 게이트 산화막(3)의 막두께는 20nm, 실효 찬넬 길이는 1#956#m이다.

urity concentration Cs 2 show and has the drain diffusion layer in which the junction depth Xj 1 of the high impurity concentration distribution (7) 0.15μm , and the surface impurity concentration Cs 1 consists of the configuration of 1× 10 21 cm − 3 . Here, the film thickness of the gate oxidation film (3) is 20nm, and the effectiveness channel length are 1μm.

본 실시예에 따라서 제조한 MISFET에 있어서의 전류 전압 특성을 상세하게 검토하였으나, 드레인(5) 및 소오스 확산층(6)의 표면 불순물 농도가 1#215#1018cm-3 이상으로 구성된 MISFET에 있어서는 전류의 상승 특성에 쇼트키 성분이나 큰 직렬 저항 등이 발견되지 않고, 양호한 옴접촉이 드레인(5) 및 소오스 확산층(6)과 백금 실리사이드(12) 사이가 얻어지고 있는 것이 명확하게 되었다. 본실시예에 따라서 제조된 MISFET에 관한 상기 측정결과에서 드레인 확산층(5)의 표면 불순물 농도로 1018cm-3이상1020cm-3 미만인 것이 소오스 드레인 내압의 고내압화의 관점 및 양호한 음접촉의 관점에서 바람직하고, 특히 5#215#1018cm-3 정도인 것이 바람직하다. 상기의 조건에서 드레인 확산층이 구성된 본 발명에 의한 MISFET에 있어서는 종래의 동일치수의 미세 MISFET에 비해서 BVDS 값에서 3.5V 이상의 고내압비가 실현되고, 또한 양호한 옴접촉도 확보할 수가 있었다. 상기의 양호한 옴접촉은 낮은 불순물 농도 표면으로서 실리사이드 형성시에 실리사이드층 (12) 바로 아래에 매우 얇은 높은 불순물 농도 석출층(13)이 동시에 형성되기 때문이라고 생각된다.

According to the present preferred embodiment, specifically the current voltage property in MISFET manufactured was examined. But it was in formed MISFET and the short key component or the serial resistance etc. of the surface impurity concentration of the source diffusion layer (6) and drain (5) was not discovered over 1× 10 18 cm −3 in the rising characterisitics of the current and big it was clear that the drain (5), the source diffusion layer (6) and platinum-silicide (12) interval of the good ohmic contact was obtained. According to the present preferred embodiment, in the measurement result about manufactured MISFET, it is the be desirable to the surface impurity concentration of the drain diffusion layer (5) 10 18 cm − 3 over 10 20 cm −3 under in the viewpoint of the viewpoint of the high voltage-resistant of source and drain internal pressure and the good negative principle in nature contact and what is about especially, 5× 10 18 cm −3 is the be desirable. In the condition described in the above, it was in the MISFET according to the invention in which the drain diffusion layer was formed and the high voltage-resistant ratio more than 3.5V in the BV DS value was realized in comparison with the minute MISFET of the conventional same size and the ohmic contact which was moreover good could secure. It is regarded that very thin high impurity concentration precipitation layer (13) is due to be immediately simultaneously beneath formed as the impurity concentration surface in which the good ohmic contact described in the above is low in the silicide formation with the silicide layer (12).

본발명에 따라서 구성된 MISFET에 있어서는 종래의 실리사이드 드레인 구조를 갖는 MISFET와 마찬가지로 3Ω/cm2 의 낮은 시이트 저항을 확보할 수가 있었다.

The low sheet resistance of 3Ω / cm 2 could be secured like MISFET which was in MISFET formed according to the invention and had the conventional silicide drain structure.

[실시예 2]

[Embodiment 2]

제7도는 본발명의 다른 실시예를 도시한 도면이며, 상기 제1의 실시예에 있어서 게이트 측벽 산화막(11)의 막의 두께를 얇게 하고, 드레인 접합 끝이 게이트 전극(4)아래에 존재하도록 구성하여 MISFET를 작성하였다.

It is drawing in which figure the seventh shows the other embodiment of the invention. It made the thickness of the film of the gate sidewall oxide (11) thin as to the first embodiment and it configured so that the drain junction end existed under the gate electrode (4) and MISFET was prepared.

상기 구성에 있어서는 드레인 확산층(5)의 낮은 불순물 농도 영역의 대부분 이 게이트 인가 전압에 의해 제어되는 것이 가능하게 된다. 실효 찬넬 길이 1#956#m, 소오스와 드레인의 각 적합 깊이 0.25#956#m 및 게이트 산화막의 두께 20nm등 MISFET의 구조 파라미터를 동일하게 하고, 상기 제1의 실시예 및 본 실시예에 따라서 구성된 MISFET, 또 종래의 높은 불순물농도 분포만으로 소오스 및 드레인이 구성된 MISFET에 대해서 각각 그 전달 콘덕턴스를 측정하였다. 그 결과, 상기 종래 구조 MISFET의 전달 콘덕턴스를 1로 하였을 때, 제1 및 본 실시예에 따라서 구성된 각 MISFET의 전달 콘덕턴스는 각각 0.95 및 0.98로 되었다.

It is possible that it is in the configuration and the mostly is controlled of the low concentration domain of impurities of the drain diffusion layer (5) with this gate impressed voltage. It made the structure parameter of MISFET including the thickness 20nm of the gate oxidation film and 0.25μm etc. the deeply identical with the effectiveness channel length 1μm, and each conformity of the drain and source and the transfer conductance was measured about MISFET in which the source and drain consisted of the high impurity concentration distribution with the MISFET. According to the present preferred embodiment. was formed with the first embodimen

GF Exhibit 1124 - 1909/2704

t. Consequently, when the transfer conductance of the conventional structure MISFET was done to 1 , it beca me the transfer conductance of each MISFET which ac cording to the present preferred embodiment, was form ed with the first with 0.95 to 0.98.

본 실시예에 따른 상기 MISFET의 전달콘덕턴스의 값은 드레인 접합 깊이의 약절반이 게이트 전극(4)로 덮여지도록 구성된 MISFET에 관한 것이다. 상기 측정 결과에서 명확한 바와 같이, 드레인 접합이 게이트 전극(4)로 덮여지는 것과 같이 구성한 MISFET에 있어서는 종래 구조 MISFET와 거의 동일한 전달콘덕턴스를 확보하고, 또한 종래 구조 MISFET의 약2배의 소오스와 드레인 사이의 내압을 실현할 수가 있었다. 본 실시예에 있어서, 전달 콘덕턴스 향상의 관점에서는 게이트 전극(4)로 덮여지는 드레인 저농도 영역의 비율을 크게 하는 것이 바람직하지만, 게이트 용량의 저하의 관점에서는 상기 비율을 적게 하는 쪽이 바람직하다. 따라서, 상기의 비율은 집적회로 설계에 관한 종합적 판단에 의해 결정하면 좋다.

The value of the transfer conductance of MISFET according to this embodiment relates to MISFET in whi ch about half of the drain conjugation depth is covered with the gate electrode (4). As shown in it was clear a nd accurate in the measurement result than it was in M ISFET which it configured as the drain junction been co vered with the gate electrode (4) and the same transf er conductance as the conventional structure MISFET was secured and moreover, the internal pressure betw een the source of about two times of the conventional structure MISFET and the drain could be realized. As to this embodiment, it is the be desirable to play the rate of the drain low density area covered with the gate ele ctrode (4) in the viewpoint of the transfer conductanc e improvement. However the side writing the rate is th e be desirable in the viewpoint of the degradation of th e gate capacitance. Therefore, it is better that the rat e described in the above determines with the synthetic determination about the integrated circuit design.

[실시예 3]

[Embodiment 3]

제8도는 본 발명의 다른 실시예를 도시한 도면으로서, 상기 제1의 실시예에 있어서 낮은 불순물 농도 드레인 확산층의 형성을 위한 비소 이온 주입 공정을 2회로 나누어 각각 70KeV 및 300KeV의 에너지로 이온 주입하고, 다음에 상기 제1의 실시예에 따라서 MISFET를 제조하였다.

Figure 8 is drawing showing the other embodiment of the invention. The arsenide ion injection process for th e formation of the low impurity concentration drain diff usion layer was divided into two times as to the first e mbodiment and it ion-implanted the respectively at the energy of 300KeV and 70KeV and next MISFET was ma nufactured according to the first embodiment.

상기 제1의 이온 주입에 의해 5#215#1018cm-3 인 최대 불순물 농도가 반도체 표면에 형성되고, 제2의 이온주입에 의해서는 5#215#1017cm-3 인 최대 불순물 농도가 반도체 기판 표면에서 약 0.16#956#m 내부에 구성되는 드레인 확산층 구조로 하였다. 상기 MISFET에 있어서 소오스와 드레인 사이에 5V의 전압을 인가하고, 게이트 인가 전압의 함수로서 기판(1)에 흐르는 전류를 측정하였을 때, 그 최대 전류값은 1.7#215#10-7A이었다.

The maximum impurity concentration which was 5× 10 18 cm - 3 was formed in the semiconductive surface w ith the first ion implantation and it was according to du e to the second ion implantation and the maximum impu rity concentration which was 5× 10 17 cm -3 was don e by the drain diffusion layer structure of being formed in the surface of semiconductor substrate inside about 0.16μm. The voltage of 5V was applied as to MISFET b etween the source and drain and when the current flo wing in the substrate (1) was measured as the functio n of the gate impressed voltage , the peak current valu e was 1.7× 10 - 7 A.

본 실시예에 의한 MISFET와 동일한 구조 파라미터를 갖는 상기 제1의 실시예에 따른 트렌지스터 및 공지의 이중 드레인 구조로 구성된 MISFET에 대해서 상기와 동일한 조건에 의해 기판 전류를 측정한 결과는 그 최대 전류가 각각 9.6#215#10-7A 및 1.2#215#10-5A이었다.

As to the measured result, the maximum current was the substrate current 9.6× 10 - 7 A and 1.2× 10 - 5 A about MISFET consisting of the drain structure amon g the transistor according to the first embodiment havi ng the same structure parameter as MISFET by this em bodiment and publicly known this with the above and s ame condition.

본 실시예에 따른 MISFET의 기판전류가 종래의 구조의 MISFET에 있어서의 기판전류 보다도 약 2리 수만큼이나 작은 것은 MISFET의 신뢰성의 향상에 본 발명에 의한 MISFET가 매우 유효하다는 것을 나타내고 있다. 즉, 기판 전류의 저감은 게이트 산화막 속의로의 핫 캐리어 주입량의 저감화의 작용을 갖는 것으로 알려져 있고, 임계 전압값의 변동이나 표면 준위

The that the MISFET according to the invention is very effective thing is shown in the improvement of the relia bility of MISFET that the substrate current of MISFET according to this embodiment is smaller than the substr ate current in MISFET of the conventional structure as about 2 Lee number. That is, the action is known that

GF Exhibit 1124 - 1910/2704

밀도의 증가등의 트랜지스터 특성이 저하하지 않도록 한다.

the reduction of the substrate current has the action o f the reduction of the hot carrier injection amount to t he gate oxidation film *** and the transistor characteri stic including the increase of the change of the thresh old voltage value or the surface level density etc. is no t degraded.

본 실시예에 있어서는 이온 주입의 가속 에너지를 변경한 2회의 이온 주입 공정에 의해 다른 분포를 갖는 낮은 불순물 농도 분포의 합성에 의해 드레인 확산층 (5)를 구성한 일 예를 나타냈지만, 상기의 드레인 확산층은 3종류 이상의 낮은 불순물 농도 분포의 합성에 의해서도 좋고, 제조 공정도 이온 주입 법에 한정되는 것이 아니라 예를들면, 공지의 열 확산법에 의해서도 좋다. 또, 드레인 확산층을 형성하는 불순물은 동일의 것일 필요는 없고, 동일한 도전형의 원자이면 그 조합은 아무래도 좋다. 즉, 본 실시예의 기본 개념은 드레인 확산층(5)내의 최대 전계인가 영역이 한점에 집중하는 일 없이 인가 전계를 가능한 한 분산시킬 수 있는 드레인 불순물 분포를 실현하는데 있다. 상기 개념에 따르면, 최대 전계가 인가되는 불순물 농도가 약 1 #215#1018cm-3로 드레인 확산층(5) 전체가 구성되는 것이 이상적이고, 상기의 이상에 의해 합당한 불순물 농도 분포를 합성하여 드레인 확산층(5)를 구성하는 것이바람직하다.

One example configuring the drain diffusion layer (5) with the composition of the low impurity concentration distribution having the dissimilar distribution with the io n implantation process of being in this embodiment and changing the acceleration energy of the ion implantatio n of two times was shown. However the drain diffusion layer described in the above is good with the compositi on of the low impurity concentration distribution more t han 3 kind and the manufacturing process is not restric ted to the ion implantation method but it is good with f or example, the publicly known thermal diffusion metho d. And the need that the impurity forming the drain diff usion layer is of the identity does not have and the co mbination is by no means good if it is the atom of the s ame conductivity type. That is, the basic concepts of this embodiment is to realize the drain impurity distribut ion which can disperse the applied field as long as the maximum electric field approved area within the drain di ffusion layer (5) converges on one point task is possibl e without the task in which. According to the concept, it is ideal that the drain diffusion layer (5) whole of the impurity concentration in which the maximum electric fi eld is applied is formed of about 1× 10 18 cm - 3 and t he impurity concentration distribution merging is synthe sized with over described in the above and the drain dif fusion layer (5) is configured it is the lice be desirable.

[실시예 4]

[Embodiment 4]

제10도는 본 발명의 다른 실시예를 도시한 도면으로, 상기 제1의 실시예에 있어서의 실리콘 박막에 의해 구성된 게이트 전극(4) 대신에 Mo 박막에 의한 금속 게이트 전극(4)를 사용하고 있다. 상기의 Mo 전극의 표면 위에는 실리콘 질화막으로 되는 전국 보호막(18)을 게이트 전극(4)와 자기 정합적으로 구성하였다. 이것은 동일의 포토레지스트를 사용해서 에칭하는 것에 의해 행한 상기의 게이트 구조는 금속 게이트 구조로서 공지이며, 그 상세한 설명은 생략한다. 상기 제1의 실시예 및 상기 공지의 금속 게이트 구조 트랜지스터의 제조 방법에 따라서 낮은 불순물 농도 드레인 확산층(5) 및 소오스 확산층(6)위에 PtSi층 (12)를 형성한다.

Figure 10 is a drawing of the other embodiment of the invention, the metal gate electrode (4) by the Mo thin film instead of the gate electrode (4) which the silicon thin film in the first embodiment is organized is used. T he whole country protective film (18) consisting of the silicon nitride film was organized on the gate electrode (4) and self-alignment manner on the surface of the M o electrode described in the above. The gate structure described in the above of performing by this using the photoresist of the identity and etching is the bulletin a s the metal gate structure and the detailed explanation omits. The PtSi layer (12) is formed according to the m anufacturing method of the publicly known metal gate structure transistor and the first embodiment on the im purity concentration drain diffusion layer (5) and the lo w source diffusion layer (6).

그후, 상기 실리사이드 층(12) 바로 아래에 실리사이드층과 자기 정합의 관계로 As 이온을 주입하였다. 상기 As 이온 주입에 의한 최대 불순물 농도는1#215#1021cm-3이고, 반도체 표면에서 최대값을 갖는 구성으로 되어 있다. 상기 As 이온 주입에 의한 접합 깊이는 50nm 이하로 되는 것과 같이 이온 주입기에 가속 에너지를 여러 가지로 변화시켜서 실시하였다. 그후 램프가열을 사용한 순간가열법에 의해 상기의 높은 불순물농도 영역(16)만을 활성화 하였다.

Thereafter, the As ion was immediately beneath injected to the relation of the self alignment and silicid e layer with the silicide layer (12). It is the maximum im purity *** × 10 21 cm - 3 by the As ion implantation and it consists of the configuration of having the maxi mum value in the semiconductive surface. As the juncti on depth by the As ion implantation become less than 50nm the acceleration energy was variously diversified and it performed to the ion-implanter. Thereafter, it ac tivated with the flash heating method using the Lamp h eating only the high concentration domain of impurities (16) described in the above.

GF Exhibit 1124 - 1911/2704

그후, 상기 제1의 실시예에 따라서 보호 절연막(15) 및 드레인 전극(9)와 소오스 전극(10)을 구성하였다. 상기 전극(9) 및 (10)과 실리사이드 층(12) 사이에는 A1과 실리사이드의 반응을 방지하기 위한 Ti,Ta혼합막(14)가 상기 실시예 1에 따라서 구성되어 있다. 상기 구성에 따라서 제조된 접합 깊이 10nm에서 50nm인 높은 불순물 농도 영역(16)을갖는 각종 MISFET에 있어서 그 BVDS 값을 측정하였을 때 모든 MISFET에 있어서도 BVDS값은 상기 제1의 실시예에 따른 MISFET의 BVDS 값보다 약0.5V낮을 뿐 이었다.

Thereafter, according to the first embodiment, the protective insulator film (15), the drain electrode (9) a nd source electrode (10) were configured. The Ti,Ta mi xing film (14) for preventing the reaction of the silicide and A1 is formed between the electrode (9), (10) and silicide layer (12) according to the embodiment 1. In th e junction depth 10nm manufactured according to the configuration, when measuring the BV DS value as to t he high concentration domain of impurities (16) *** all kinds of MISFET that was 50nm, the BV DS value conti nued about 0.5V day as to all MISFETs than the BV DS value of MISFET according to the first embodiment wit h only.

상기의 결과는 실리사이드 층(12) 바로 아래의 높은 불순물 농도 영역(16)이 50nm 이하로 얇으면, 종래구조 MISFET에 비해서 소오스 및 드레인 내압이 한층 개선되는 것을 나타내고 있다. 본 실시예의 기본적 개념은 드레인 확산층(5) 표면에 구성하는 높은 불순물 농도 영역(16)이 접합 깊기로 50nm 이하로 매우 얇으면 BVDS값의 고내압화에 실효적으로 지장이 없고, 또한 양호한 옴접촉도 확보할 수 있는 것이다. 본실시예에 있어서는 실리사이드 층(12)를 드레인 확산층(5) 위에 구성한 예에 대해서 나타내었지만, 상기 개념에 따르면 실리사이드 층은 백금 실리사이드에 한정되는 것이 아니고, Mo,W,Pt,Pd,Ni,Ti,Ta,Nb,Cr,Pr등의 고융점 금속 및 그들의 실리사이드 막으로 치환하여 구성하여도 지장이 없다.

If as to the result described in the above, the silicide layer (12), immediately, the following high concentratio n domain of impurities (16) is thin less than 50nm , it s hows that the source and drain internal pressure are m ore and more improved in comparison with the conventi onal structure MISFET. If it is very thin, the impedimen t is effectively not in the high voltage-resistant of the BV DS value less than 50nm that the basic concept of this embodiment the high concentration domain of impu rities (16) configured is deep in the drain diffusion layer (5) surface with junction and the ohmic contact which is moreover good can secure. It showed about the exa mple which was in this embodiment and configured the silicide layer (12) on the drain diffusion layer (5). Howe ver the silicide layer is not restricted according to the concept to the platinum-silicide but even if it substitut es with the high melting point metal and their silicide fil ms including Mo,W,Pt,Pd,Ni,Ti,Ta,Nb,Cr,Pr etc. and it c onfigures there is no impediment.

[발명의 다른 실시예]

[The other embodiment of the invention]

이상의 각 길기예에서는 모두 소오스, 드레인 영역으로 되는 확산층은 낮은 불순물 농도의 얇은 확산층이고, 화산층 저항을 저감하는 길리사이드 층은 게이트 전국에서 분리(오프 셋)되어 형성되어 있다. 따라서, 이와 같은 오프 셋 구조의 트랜지스터에서는 소오스와 드레인을 고농도, 확산층으로 형성한 것보다도 실효찬넬 콘덕턴스가 저하한다.

In each road arts described in the above, it is the thin diffusion layer of the impurity concentration in which th e diffusion layer which altogether consists of the sourc e, and the drain region is low and it becomes in the gat e whole country with the separation (offset) and the gi lly side layer reducing the volcano layer resistance is fo rmed. Therefore, in the transistor of this kind of the off set structure, the effectiveness channel conductance i s degraded than forms the source and drain into the hi gh concentration, and the diffusion layer.

그래서, 게이트 측벽 절연막(제6도, 제7도, 제8도, 제19도의 부호(11)을 실리콘 산화막이 아니고, 비유전율이 보다 높은 재료로 형성하면 게이트에서의 프린지(fringe) 용량(면이 대향하는 용향보다 광의의 의미로서, 도전체의 언저리나 끝에 생기는 용량을 말한다.)에 의해 소오스 및 드레인의 낮은 불순물 농도 확산층의 표면으로의 게이트 전압의 영향을 높일 수가 있어 실효 전달 콘덕턴스가 높은 디바이스를 얻을 수가 있다. 이것은 제1도에 도시한 바와 같은 이중 확산 구조의 소오스와 드레인을 갖는 MIS FET에 대해서도 적용된다.

So, the seventh the eighth is the denotation (11) of Figure 19 not gate sidewall insulation film (sixth the sili con oxide film and if the relative permittivity forms into the higher material, the influence of the gate voltage t o the surface of the low impurity concentration diffusio n layer of the source and drain can be enhanced with t he fringe (fringe) capacity (as the meaning of the broa d sense than the capacity in which side is faced, the g enerated capacity is referred to the brim or the end of the conductor.) at gate and the device in which the ef fectiveness transfer conductance is high can be obtain ed. This is applied to Figure 1 to the MIS FET having th e source and drain of the spread structure among this l ike showing.

[실시예 5]

[Embodiment 5]

GF Exhibit 1124 - 1912/2704

제11도는 본 발명에 의한 MISFET의 1실시예를 도시한 도면으로, (1)은 P 도전형 비저항 1Ω/㎝의 실리콘 기판이고, (2)는 공지의 선택 산화법에 의해 형성된 필드 산화막으로 인접하는 MISFET사이를 분리 하는 두꺼운 실리콘 산화막이다. (3)은 20 nm의 실리콘 열 산화막, (4)는 인을 첨가시켜 저 조항화된 실리콤 박막으로 구성된 게이트 전극이다. 공지의 실리콘 게이트 기술에 의해 게이트 전극(4)을 형성한 후, 실리콘 열 산화막(3)을 거쳐 게이트 전극을 마스크로 해서 비소(As) 이온을 이온 주입법에 의해 실리콘 기판 표면에 주입하고, 이어서 주입 이온의 활성화를 위한 열처리를 행하여 드레인 확산층(5) 및 소오스 확산층(6)을 형성하였다. 상기의 이온 주입에 있어서는 반도체 표면에서 불순물 농도가 최대로 되고, 그 최대값이5#215#1018Cm-3으로 되는 조건에서 행하였다.

Figure 11 is a drawing of 1 embodiment of the MISFET according to the invention, (1) is the silicon substrate of P conductivity type resistivity 1Ω / ㎝. (2) It is the thick silicon oxide film separating according to the field oxide film formed with the increased publicly known local oxidation of silicon between adjacent MISFET. (3) is the silicon thermal oxide film of 20 nm, and (4) are the gate electrode consisting of the silicon thin film adding the phosphorus and becomes with the base clause. The gate electrode was after the silicon thermal oxide film (3) to the mask and the gate electrode (4) the arsenic (As) ion was injected with the publicly known silicon gate technology after doing the formation with the ion implantation method into the silicon substrate surface and subsequently the thermal process for the activation of the implant ion was performed and the drain diffusion layer (5) and source diffusion layer (6) were formed. It was in the ion implantation described in the above and the impurity concentration was maximized in the semiconductive surface and it performed in the condition consisting of the maximum value lice 5× 10 18 Cm - 3 .

그후, 암모니아(NH3)와 모노실란(SiH4)의 화학 기상 반응에 의해 주표면 전면에 비유전율 6.0인 실리콘질화(Si3N4)막을 막두께 0.25㎛의 조건으로 퇴적한다.

Thereafter, the silicon nitride (Si(SB)3(/SB)N(SB)4 (/SB)) film which is the relative permittivity 6.0 is accumulated with the chemical vapor deposition of the monosilane (SiH(SB)4(/SB)) and ammonia (NH(SB)3(/SB)) in the major surface front side to the condition of the film thickness 0.25㎛.

그후, 평행 평판형 반응성 스피터 에칭 장치에 의해 상기의 Si3N4 막을 0.25㎛두께만큼 에칭하였다.

Thereafter, the si 3 N 4 film described in the above was etched with the parallel plate type reactive Peter etching device as 0.25㎛ thickness.

상기의 에칭은 소위 이방성 에칭이라고 하는 것으로서 반도체 기판 표면과 수직 방향에만 에칭을 진행시킬 수가 있다. 따라서, 상기의 에칭후에는 게이트 전극(4)의 측벽부에만 Si3N4막(19)가 남게 된다. Si3N4막으로 구성되는 측벽 절연막(19)의 형성 후, 게이트 전극(4)와 측벽절연 막(19)를 마스크로 하여 소오스 및 드레인 확산층 표면에서 최대 불순물 농도로 되는 조건으로 재차 As 이온 주입을 행한 후, 그 활성화를 위한 열처리를 실시하였다.

The etching described in the above is called the so-called anisotropic etching and the etching can be proceeded in the surface of semiconductor substrate and vertical direction. Therefore, in the post-etching described in the above, the Si 3 N 4 film (19) remains in the sidewall part of the gate electrode (4). It had the gate electrode (4) and side wall insulating film (19) as the mask and the As ion implantation the thermal process for the activation was again performed after the formation of the side wall insulating film (19) consisting of the Si 3 N 4 film in the source and drain diffusion layer surface to the condition consisting of the maximum impurity concentration after doing the row.

살기 제2의 이온 주입에 의해서 고오스 및 드에인 확산층의 최대 불순물 농도는 1#215#10㎝-3 이상의 높은 불순물 농도로 되었다. 그후, 통상의 반도체 제조 공정 순서에 따라, 게이트 보호 산화막(20) 및 드네인 전극(21)과 소오스 전극(22)를 형성하고 MISFET로 되는 반도체 장치를 제조하였다.

The maximum impurity concentration of the diffusion layer which was in the high OSS and consisted of the high impurity concentration more than 1×10 ㎝ - 3 with the ion implantation of the violent temper second. Thereafter, according to the normal process of manufacturing semiconductor order, the electrode (21) which was the protecting gate oxide film (20) and the semiconductor device for forming the source electrode (22) and consisting of MISFET were manufactured.

본 실시예에 따라서 제조한 MISFET는 실효 찬넬 길이가 0,9㎛, 드레인 확산층에 있어서의 낮은 불순물 농도 영역(5)의 접합 깊이가 0.35㎛, 높은 불순물 농도 영역(7)의 접합 깊이가 0.15㎛이었다.

According to the present preferred embodiment, 0.35㎛, and the junction depth of the high concentration domain of impurities (7) of 0,9㎛, and the junction depth of the low concentration domain of impurities (5) in the drain diffusion layer as to the MISFET, manufactured of the effectiveness channel length was 0.15㎛.

GF Exhibit 1124 - 1913/2704

상기 MISFET에 있어서 측벽 절연막(19)는 소오스 및 드레인 확산층 위에서 1020㎝-3 이하의 불순물 농도 영역 표면을 덮고 있는 구성으로 되어 있다. 본 실시예에 따른 상기 MISFET의 전달 콘덕턴스는 측벽 절연막이 종래의 실리콘 산화막으로 구성되는 동일 치수의 MISFET에 있어서 전달 콘덕턴스의 약 1.1배 크다는 것을 알게 되었다.

It consists of the configuration where the side wall insulating film (19) covers the concentration domain of impurities surface less than 10 20 ㎝ -3 as to MISFET in the source and drain diffusion layer. The transfer cond uctance of MISFET according to this embodiment knew as to MISFET of the same size in which the side wall in sulating film consisted of the conventional silicon oxide film being large with about 1.1 times of the transfer co nductance.

상기의 전달 콘덕턴스의 차이는 게이트 전극(4)의 측벽에 있어서 절연막(19)의 비유전율의 차이에 차이에 따른 전속 밀도의 차이에 의한 것이라고 생각된다. 즉, 본 실시예와 같아 측벽 절연박(19)의 비유전율이 게이트 산화막의 비유전율 보다 1.6배 큰 경우에는 측벽 절연막의 비유전율이 게이트 산화막의 비유전율과 동등한 종래 구성의 MISFET의 경우보다 게이트 전계가 소오스 및 드레인 확산층의 낮은 불순물 농도 영역 표면으로 돌아 들어가는 전속 밀도가 크고, 낮은 불순물 농도 영역 표면을 보다 n형화하여 전도도를 높이기 위함이라고 생각된다.

It is regarded in the difference of the difference is the relative permittivity of the insulating layer (19) as to th e sidewall of the gate electrode (4) of the transfer con ductance described in the above as by the difference o f the electric flux density according to the difference. That is, in case it is the same as that of this embodime nt and the relative permittivity of the sidewall insulatio n tape (19) is greater than the relative permittivity of t he gate oxidation film with 1.6 times the electric flux d ensity in which the gate electric field rotates into the l ow concentration domain of impurities surface of the dr ain diffusion layer and source than the relative permitti vity of the gate oxidation film and MISFET of the equiv alent conventional composition and the relative permitti vity of the side wall insulating film enters is large and it is for the low concentration domain of impurities surfac e to the n-type more look fine and raise conductivity it is regarded.

[실시예 6]

[Embodiment 6]

제12도는 본 발명의 다른 실시예를 설명하기 위한 도면이다. 상기 제1의 실시예에 있어서 낮은 불순물농도의 드레인 확산층(5)및 소오스 확산층(6)을 형성한 후, 실리콘 게이트 전극(4)의 표면을 열산화하여 10nm의 실리콘 산화막(23)으로 게이트 전극(4)을 덮는다. 그후, 비유전율로 되는 실리콘 박막을 SiH4 가스의 화학 기상 반응을 사용해서 전면에 퇴적하였다. 퇴적막의 두께는 약0,5㎛이었다.

Figure 12 is a drawing illustrating the other embodiment of the invention. The surface of the silicon gate electro de (4) thermally is oxidated and the drain diffusion laye r (5) and source diffusion layer (6) of the low impurity concentration the gate electrode (4) are covered as to the first embodiment after doing the formation with the silicon oxide film (23) of 10nm. Thereafter, the silicon t hin film consisting of the relative permittivity was accu mulated in the front side by using the chemical vapor d eposition of the SiH 4 gas. The thickness of the heap fi lm was about 0,5㎛.

그후, 평행 평판형 반응성 스피터 장치에 의해 반도체 표면과 수직 방향으로 상기 실리콘 박막을 0.5㎛ 에칭하였다.

Thereafter, the silicon thin film 0.5㎛ was etched to the semiconductive surface and vertical direction with the parallel plate type reactive Peter apparatus.

상기 공정에 의해 게이트 전극(4)의 측벽에 얇은 실리콘 박막(23)을 거쳐서 실리콘 퇴적막(19)가 외부로 부터 격리되어 0.5㎛의 으로 남게 되었다. 상기 에칭 후는 상기 제1의 실시에에 따라서 MISFET를 제조하였다. 본 실시예에 따라서 제조한 MISFET의 전달 콘덕턴스를 측정하였을 때 실리콘 산화막으로 게이트 전극의측벽 절연막을 구성한 동일 치수의 종래 MISFET의 전달 콘덕턴스의 약 1.2배에 달하였다. 더욱 주목 되는 것은 본 실시예에 따른 MISFET의 정특성 측정후에 재차 전달 콘덕턴스를 측정하였을 때 전달 콘덕턴스는 더욱 증가하여 통상 이중 드레인 구조 MISFET의 전달 콘덕턴스의 약 1.25배까지 달한다.

Silicone heap film (19) was isolated from the outside and it remained in the sidewall of the gate electrode (4) with the process after the thin silicon thin film (23) as 0.5㎛. According to the first operation after the etc hing, MISFET was manufactured. According to the pres ent preferred embodiment, number reached about 1.2 ti mes of the transfer conductance of the conventional M ISFET of the same size organizing the gate electrode si de wall insulating film on silicon oxide film when measuri ng the transfer conductance of MISFET manufactured. More, when again measuring the transfer conductance after the static characteristics measurement of MISFE T according to this embodiment, the transfer conducta nce more increases and generally the number reaches among this to about 1.25 times of the transfer conduct ance of the drain structure MISFET to be watched.

GF Exhibit 1124 - 1914/2704

상기는 소오스 및 드레인 확산층이 높은 불순물 종도 분포만으로 구성되는 통상MISFET의 전달 콘덕턴스와 거의 같은 것이다. 본 실시예의 MISFET에 있어서 실효적인 전달 콘덕턴스가 향상한 제1의 이유는 측벽 퇴적막(19)의 비유전율이 실리사이드(12)와 실리콘 산화막의 값에 비해서 충분히 크기 때문이라고 생각된다. 또, 제2의 이유는 정특성의 측정으로 5V 이상의 게이트 전압을 인가하였을 때, 게이트 전극보다 정의 전하가 얇은 산화막(23)을 거쳐서 실리콘 퇴적막(19)에 천이되어 축적되고, 이 정의 축적 전하에 의해 소오스 및 드레인 확산층의 낮은 불순물 농도 영역표면이 더욱 n형화하여 전도도가 상승하였기 때문이라고 생각된다.

The impurity type in which as to the above, the source and drain diffusion layer are high is is nearly the same a s that of the transfer conductance of the formed ordin arily MISFET to the distribution. Reason for the first th e relative permittivity of the sidewall heap film (19) is e nough regarded in comparison with the value of the sili con oxide film and silicide (12) as the because why the effective transfer conductance improves as to MISFET of this embodiment to be large. And when the second r eason applied the gate voltage more than 5V to the me asurement of the static characteristics , it is transmitt ed after the oxide film (23) in which the definition elect ric charge is thin than the gate electrode in silicone he ap film (19) and it is accumulated and it is regarded th at the n-type the low concentration domain of impuriti es surface of the drain diffusion layer and source more looked fine and conductivity was due to rise with the bi modal stored charge.

즉, 실리콘 퇴적막(19)는 전기적으로 프로그램 가능한 불휘발성 메모리에 있어서의 부유 게이트의 작용을 갖는 것이라고 생각된다. 실리콘 퇴적막(19)를 정의 전하를 축적하는 부유 게이트로서 작용시키는 것은 MISFET 제조후의 좋은 품질 선택 테스트시에 특성 점검을 행할 때에 실시할 수 있으므로 제품 출하전에 전하를 주입하여 축적, 유지시키는 본 실시례의 트랜지스터에 있었어는 드레인 전계에 의한 드레인의 낮은 불순물 농도 영역의 표면 전계를 약하게 하는 적용도 갖고 있으며, 드레인 강전계에 의한 핫 캐리어의 게이트 산화막으로 주입에 따른 MISFET의 열화현상도 방지하는 다른 작용도 갖고 있다.

That is, regarded that silicone heap film (19) electrically has the action of the floating gate in the pr ogrammable nonvolatile memory. The application which injects the electric charge before the product shipment and makes the reduced surface field of the low concen tration domain of impurities of the drain by the drain el ectric field which was in accumulation, and the transist or of this operation example which maintained weak sin ce it can perform to operate silicone heap film (19) as t he floating gate accumulating the definition electric ch arge when performing the characteristic test in the goo d quality selection test after the MISFET manufacture has and the dissimilar action of the degradation of MIS FET according to injection preventing to the gate oxida tion film of the hot carrier by the drain strong electric fi eld has.

이상과 같이 하면 ,게이트 측벽에 있어서 프린지 용량을 개재한 게이트 전계의 영향을 소오스 및 드레인의 낮은 불순물 농도 영역 표면에 강하게 영향을 줄 수가 있고, 실효적인 전달 콘턴스를 종래 구조에 비해서 1.1~1.2배 이상 크헤 할 수 있다.

As described above, the influence is strong against the low concentration domain of impurities surface of the d rain and source the influence the influence of the gate electric field which interposes the fringe capacitance a s to the , gate sidewall if it does can be given and the effective transmission cone turns can be done in comp arison with the conventional structure over 1.1~1.2 ti mes with ***.

본 발명의 기본적인 개념에 따르면, 측벽 퇴적막은 실리콘 질화막에 한정되는 것은 아니고, 알루미나(Al2O3)탄달 산화막(Ta2O5), 티타늄(TiO2), 지르코늄 산화막(Zr2O3), 하프늄 산화막(Hf2O3)등 실리콘 산화막의 비유전율 보다 충분히 큰 비유전율을 갖는 유전체이면 좋다.

According to the cardinal concept of the invention, it is better that the sidewall heap film is not restricted to th e silicon nitride film and it is the dielectric which enoug h has the big relative permittivity as compared with the relative permittivity of the oxide film (Ta(SB)2(/SB)O(S B)5(/SB)), the titanium (TiO(SB)2(/SB)), the zirconium oxide layer (Zr(SB)2(/SB)O(SB)3(/SB)), the silicon oxid e film including the hafnium dioxide layer (Hf(SB)2(/SB) O3) etc which is sweet with the alumina (Al(SB)2(/SB) O(SB)3(/SB)) coal.

또, 본 발명에 의한 전달 콘덕턴스의 향상 효과는 게이트 측벽에 반도체 등으로 구성되고, 외부에서 격리된 부유 게이트 또는 외부에서 격리되 전하 축적 기구를 갖는 절연막 또는 절연막 사이의 경계면에서 형성되어도 좋으며, 외부에서 격리된 측벽 퇴적막은 실리콘에 한정되는 것은 아니고, 다른 반도체 예를 들면, 실리콘 카바이드(SiC)나 게르마늄(Ge)등이라도 좋고, 또 실리콘 질화막이나 알루미나막 등의 절연막이라도 좋다.

And the enhancement effect of the transfer conductance according to the invention comprises the semiconductor in the gate sidewall etc. And in the float ing gate or the outside isolated in the outside, it is goo d even if it is formed at the boundary face between th e insulating layer having the isolation measure charge a ccumulation tool or the insulating layer and the sidewall heap film isolated in the outside is not restricted to the silicone and it is good although it is the dissimilar semic

GF Exhibit 1124 - 1915/2704

onductor, for example, the silicon carbide (SiC) or the germanium (Ge) etc. and it is good although it is and, t he insulating layer lice including the silicon nitride film o r the alumina film etc.

[발명의 또 다른 실시예]

[Another preferred embodiment of the invention]

본 발명은 드레인 확산층에 있어서의 높은 불순물 농도 영역에 관해서 종래의 상식에 구애받지 않고 그 물리적 근간에 까지 되돌아가 해석한 결과에 기인한다. 즉, 여러가지의 드레인 확산층 농도를 갖는 MISFET에 있어서 드레인 확산층 표면에 고융점 금속의 실리 사이드 층을 형성 하였을 때, 인(P) 및 비소(As)등의 도전형의 불순물로 상기 드레인 확산층이 형성되어 있는 경우에 한하여 드레인 확산층 표면에 불순물 농도가 약 10nm의 깊이로 고농도화 되는 현상이 있다. 즉, NMOS에 있어서는 드레인 확산층 표면 불순물 농도가 1#215#1018㎝-3이상이면 상기 실리사이드 층과 반도체 표면 사이에 양호한 옴특성이 얻어져 NMOS로서의 특성에 아무런 문제도 생기지 않는다는 사실이 발견되었다.

It is caused by the result in which the invention is not restricted by the conventional common sense about th e high concentration domain of impurities in the drain di ffusion layer and returning in the physical basis and int erpreted. That is, in case the drain diffusion layer is for med with the impurity of the conductivity type includin g the phosphorus (P) and arsenic (As) etc. it is limited and when the silicide layer of the high melting point me tal in the drain diffusion layer surface as to MISFET ha ving the drain diffusion layer concentration of the vario us is formed, the phenomenon that is highly enriched h as the impurity concentration in the drain diffusion laye r surface to the depth of about 10nm. That is, the fact that the good ohmic property was obtained between th e silicide layer and semiconductive surface if it was in NMOS and the drain diffusion layer surface impurity con centration was 1× 10 18 ㎝ - 3 or greater and any prob lem was not generated in property as NMOS was disco vered.

통상의 MISFET에 있어서의 드레인 확산층은 반도체 기판 표면 부근에서 1020㎝-3이상의 높은 불순물농도 영역을 가지며, 기판 내부를 향해서 가우스 분포, 또는 오차함수 분포로 감쇠하는 불순물 농도 분포를 갖는다.

The drain diffusion layer in the normal MISFET includes the high concentration domain of impurities more than 10 20 ㎝ - 3 in the surface of semiconductor substrate vicinity, and the Gaussian distribution towards the insid e substrate or the impurity concentration distribution d amping to the error-function distribution.

상기의 통상 드레인 확산층에 전압을 인가하고, 이 즉, 불순물 농도의 함수로서 인가 전계를 해석하면, 1020㎝-3이상의 높은 불순물 농도 영역에 있어서는 매우 약한 전계밖에 인가되지 않는다는 사실이 판명되었다. 이 사실은, 초미세MISFET의 고내압화의 관점에서 보면, 높은 불순물 농도의 존재는 도리어 유해하고, 드레인 확산층의 최대 불순물 농도는 1019㎝-3이하로 구성되는 것이 바람직하다는 것이 판명되었다. 상기의 1020㎝-3이상의 높은 불순물 농도 영역의 MISFET에 있어서의 역할은 확산층 정항의 저감화와 배선 금속의 양호한 옴접촉의 확보에 있지만, 상기 후자의 역활 즉, 배선 금속과의 양호한 옴접촉은 1#215#1018 ㎝-3이상의 표면 불순물 농도를 갖는 드레인 확산층 위의 실리사이드 층의 구조에 의해서 치환이 가능하다. 상기 전자의 역할, 즉 소오스 확산저항 및 드레인 확산저항의 저감화에 관해서는 소오스 및 드레인 확산층 표면의 실리사이드화에 의해 실현되는 것이 알려져 있고 , 특히 초미세 트랜지스터에 있어서의 매우 얕은 접합 형성에서는 실리사이드화에 의한 저항 저감의 효과는 현저한 것이 있다.

The voltage the generally was applied of the above in the drain diffusion layer and if the applied field was inte rpreted as the , in other words, the function of the imp urity concentration , the fact that was in the high con centration domain of impurities more than 10 20 ㎝ - 3 and was not applied to the outside electric field which was very weak was confirmed. If this fact looked aroun d the viewpoint of the high voltage-resistant of the ult ra-fine MISFET , the high presence of the impurity con centration was rather harmful and this fact was proven that this fact was sweet that the maximum impurity co ncentration of the drain diffusion layer was formed less than 10 19 ㎝ - 3 . The high role in MISFET of the conc entration domain of impurities more than 10 20 ㎝ - 3 d escribed in the above is in the security of the good oh mic contact of the reduction of the diffusion layer cons tant resistance and wiring metal. However the substitu tion is possible with the structure of the silicide layer a bove the drain diffusion layer in which good said later r ole the , in other words, the ohmic contact of the wirin g metal has the surface impurity concentration more th an 1× 10 18 ㎝ - 3 . It is known about the role of the e lectron, in other words, the reduction of the drain diffu sion resistance and source diffusion resistance to be re alized by the salicidation of the drain diffusion layer sur face and source and it has that the effect of the resist ance reduction by the salicidation is very significant es pecially, the ultra-fine transistor in the shallow junction formation.

GF Exhibit 1124 - 1916/2704

그리하여, 본 발명의 CMOSFET는 상기의 해석 결과에 따른 개념을 발전시켜 드레인 확산층의 높은 불순물 농도 영역을 드레인 확산층과 옴 접촉으로 결합된 얇은 실리사이드 층으로 치환하고 , 또한 드레인 확산층의 불순물 농도에 관한 최적 조건을 해석적으로 구한 결과를 이용하는 것이다.

And the result in which the CMOSFET of the invention develops the concept according to the interpretation r esult described in the above and which substitutes for the high concentration domain of impurities of the drain diffusion layer with the thin silicide layer which is combi ned to the drain diffusion layer and ohmic contact and which analytically saves moreover, the optimal conditio n about the impurity concentration of the drain diffusio n layer is used.

상기 최적조건은 특히 0.5㎛이하의 게이트 길이를 갖는 초미세 MISFET의 고내압화 및 래치 업 방지에 관한 최적 조건이다.

It is the optimal condition about the high voltage-resistant of the ultra-fine MISFET in which the optimal condition has especially, the gate length less than 0.5 ㎛ and latch-up protection.

제13도 및 제14도는 각각 본 발명에 의한 해석 결과를 도시한 도면으로서, 드레인 확산층 표면 불순물 농도의 함수로써 구한 소오스 및 드레인 내압 및 최대 기판 전류의 곡선을 표시하고 있다.

As Figure 13 and drawing in which figure the fourteenth shows the interpretation result according to the inventi on, the source, saved the drain internal pressure and c urve of the maximum substrate current are indicated as the function of the drain diffusion layer surface impurit y concentration.

제13도에 있어서는 소오스와 드레인 사이의 내압으로서 전자사태 항복전압을 점선으로 표시하고, 펀치 스루 내압을 실선으로 표시하고 있다. 각 내압 모두 찬넬 길이의 함수로서 각각 구하고 있다.

It is in Figure 13 and the electron avalanche breakdown voltage is indicated by the dotted line as th e internal pressure between the drain and the source a nd the punch-through breakdown voltage is indicated b y the solid line. It altogether saves as the function of t he channel length with each internal pressure.

제13도에 있어서 전자사태 항복전압은 PMOS에 관한 것이고 , NMOS의 값의 전체적으로 표시된 곡선보다 0.1~1(V) 저하하는 경향에 있다. 펀치 스루 내압에 대해서는 PMOS와 MNOS의 값 사이에 다른 것은 발견되지 않는다.

It is in the tendency to the electron avalanche breakdown voltage be as to Figure 13 about PMOS and be degraded than the curve which on the whole, is indi cated of the value of the , NMOS with 0.1~ 1 (V). The other is not discovered about the punch-through break down voltage between the value of MNOS and PMOS.

제13도에서 새로이 명확하게 된 사실은 찬넬 길이가 0.5㎛ 이상의 트랜지스터에 있어서는 드레인 확산층의 표면 불순물 농도를 3#215#1018㎝-3으로 설정하면, 통상 구조의 동일 치수의 트랜지스터에 있어서 소오스 및 드레인 내압에 비해서 약 2배에 해당하는 10V 이상의 내압을 실현할 있는 것이다. 또, 찬넬 길이가 0.4㎛ 이하의 트랜지스터에 있어서는 찬넬 길이에 의존해서 각각 최적의 드레인 확산층 표면 불순물 농도를 약 1#215#1018㎝-3으로 설정하면, 소오스 및 드레인 내압을 약 7V로 까지 향상할 수가 있다. 찬넬 길이가 0.2㎛의 PMOS 트랜지스터에 있어서는 5#215#1017의 드레인 표면 불순물 농도로 설정하면, 약 5V의 내압이 얻어지게 된다.

In Figure 13, if it is in the transistor more than 0.5㎛ and as to the fact, that is afresh clear the channel len gth sets up the surface impurity concentration of the d rain diffusion layer as 3× 10 18 ㎝ - 3 , the fact, has. I t realizes the internal pressure more than 10V correspo nding to about two times as to the transistor of the sa me size of the trading structure in comparison with the source and drain internal pressure. And if it is in the tra nsistor less than 0.4㎛ and the channel length depends on the channel length and the optimal drain diffusion la yer surface impurity concentration is set up as about 1 × 10 18 ㎝ - 3 , the source and drain internal pressure can be improved to about 7V. If it is in the PMOS transi stor of 0.2㎛ and the channel length sets up as the drai n surface impurity concentration of 5× 10 17 , the inte rnal pressure of about 5V is obtained.

다음에, 제14도에 있어서는 드레인 전류에 의해 유기되는 소수캐리어가 기판측으로 흐르는 기판 전류를 게이트 전압의 함수로써 구하고, 그 최대로 되는 값, 즉 최대 기판 전류를 드레인 확산층 표면 불순물 농도의 함수로서 해석한 것이다.

Next, it is in Figure 14 and the substrate current in which the minority carrier induced with the drain curren t flows toward the substrate side is saved as the funct ion of the gate voltage and the maximized value, in oth er words, the maximum substrate current is interpreted as the function of the drain diffusion layer surface impu rity concentration.

제14도에서는 찬넬 길이 1.0㎛, 찬넬 폭 10㎛의 MISFET에 관해서 소오스 및 드레인 확산층의 접합 깊이를 파라미터로 하고 , 드레인 전압은 5V이다.

In Figure 14, it has the junction depth of the drain diffusion layer and source as the parameter about the channel length 1.0㎛, and MISFET of the channel width

GF Exhibit 1124 - 1917/2704

10㎛ and the , drain voltage is 5V.

제14도에서 새로이 명확하게 된 사실은 드레인 접합 깊이에 다소 의존하지만 , 드레인 확산층 표면 농도를 1017내지 1018㎝-3으로 설정하면, 기판전류를 통상구조의 것에 비해서 현저하게 개선할 수가 있어 래치 업 현상을 방지할 수도 있다.

In Figure 14, if the fact that is afresh clear a bit depends on the drain conjugation depth but the , drain diffusion layer surface concentration is set up as 10 17 to 10 18 ㎝ - 3 , the substrate current can be remarka bly improved in comparison with of the trading structur e and the latch-up can be prevented.

내 래치 업 현상에 대한 최적 표면 불순물 농도의 드레인 확산층 위에 실리사이드층을 형성하면, 음접촉은 얻을 수 없고, 쇼트키 장벽이 형성된다.

If the silicide layer is formed on the drain diffusion layer of the optimal surface impurity concentration about my latch-up , the negative principle in nature contact can not obtain and the Schottky barrier is formed.

본 발명에 있어서는 제13도 및 제14도에서 얻어진 새로운 해석결과와 상술한 2건의 참고문헌에 따라서 지금까지 없었던 고내압에서 내 래치 업의 초미세 CMOS FET를 실현하였다. 즉, 발명의 CMOSFET에 있어서는 PMOS를 간디 2건의 문헌에 따른 쇼트키 장벽의 드레인 접합으로 형성하고, 한편 NMOS에 대해서는 제13도에서 얻어진 새로운 해석 결과에 따라서 1018㎝-3이상의 표면 불순물 농도를 갖는 확산층과 음접촉을 갖는 실리사이드등의 조합으로 드레인 접합을 형성하고 있다. 이것에 의하여 내 래치 업 특성 향상 이외의 PMOS 및 NMOS의 각 소오스 드레인 확산층의 표면 불순물 농도를 0.5㎛이하의 초미세 COMSFET의 고내압화의 관점에서 더욱 최적화 하는 것이 가능하게 된다.

It was in the invention and the ultra-fine CMOS FET of my latch up was realized with the new interpretation re sult which was obtained in Figure 13 and Figure 14 in t he high voltage-resistant which there was so far no ac cording to the above-described reference of 2 cases. T hat is, in CMOSFET of the invention and PMOS is forme d into the drain junction of the Schottky barrier accordi ng to the literature of the Gandie 2 cases and the drain junction is formed into the combination including the dif fusion layer having the surface impurity concentration more than 10 18 ㎝ - 3 according to the new interpreta tion result which is obtained about NMOS in Figure 13 a nd silicide etc. in the meantime. Having the negative pr inciple in nature contact. According to this, in the view point of the high voltage-resistant of the ultra-fine CO MSFET less than 0.5㎛ the surface impurity concentrati on of each source drain diffusion layer of PMOS except my latch up property improvement and NMOS, it is poss ible to more optimize.

[실시예 7]

[Embodiment 7]

제15도, 제16도 및 제17도는 각각 본 발병의 제7의 실시예를 도시한 CMOSF ET의 제조공정의 단면 구조도이다.

With the 15, is Figure 16. And figure 17 is a sectional configuration of the manufacturing process of the CMO SF ET showing the seventh embodiment of the onset lo oked.

제15도~제17도에 있어서 (221)은 n도전형으로 비저항 0.4Ω.㎝의 실리콘 기판이며, 이 기판(221)의 소정의 위치에 붕소를 접합깊이 2㎛, 표면 불순물 농도 1#215#1016㎝-3으로 확산하고, P오전형 웰(222)를 형성한다. 다음에 공지의 소자 분리 기술을 이용해서 0.5㎛의 두꺼운 필드 산화막(223)을 선택적으로 형성한 후 활성 영역의 반도체 표면을 노출하고 20㎚의 막의 두께를 갖는 깨끗한 게이트 산화막(28)을 형성한다. 그후, 약 0.4㎛두께의 실리콘 박막을 게이트 산화막(28)위에 형성하고, POC3을 확산원으로 하는 열 확산에 의해 상기 실리콘 각막에 인(P)의 고농도 확산을 행한다. 다음에 상기 실리콘 박막 표면을 열산화 하고 0.2㎛두께의 실리콘 산화막을 상기 실리콘 박막위에 형성한다. 그후, 리도그래피에 의해 상기 실리콘 산화막 및 실리콘 박막을 바라는 회로구성에 따라서 동시에 제거하고, 게이트 보호 절연막(212) 및 게이트 전극(29)를 각각 남겨 놓는다. 그리고, 상기 리도그래피 후의 게이트 전극(29)의 폭 즉, 찬넬폭으로서는 1.0, 0.5, 0.3, 0.2 및 0.1㎛의 5개 조건에 대해서 실시하였다.

The 15 (221) is the silicon substrate of the resistivity 0.4Ω ㎝. as to figure the seventeenth to the n conduct ivity type and boron is diffused to the predetermined p osition of this substrate (221) to the junction depth 2 ㎛, and the surface impurity concentration 1× 10 16 ㎝ - 3 and the gate oxidation film (28) which selectively e xposes the semiconductive surface of the active area t he thick field oxide film (223) of 0.5㎛ after doing the fo rmation by it forms P forenoon type well (222) next usi ng the publicly known isolation technology and has the thickness of the film of 20㎚ and is clean is formed ther eafter the silicon thin film of about 0.4㎛ thickness is fo rmed on the gate oxidation film (28) and the high conc entration diffusion of the phosphorus (P) is performed with the thermal diffusion the POC 3 to the diffusion so urce in silicone cornea the silicon thin film surface ther mally is oxidated to the next and the silicon oxide film o f 0.2㎛ thickness is formed on the silicon thin film it sim ultaneously removes with lithography according to the circuit configuration wanting the silicon oxide film and s ilicon thin film and the gate protective insulator film (21 2) and gate electrode (29) are left respectively. And it performed about 5 the condition of 0.1㎛ and 1.0, 0.5,

GF Exhibit 1124 - 1918/2704

0.3, 0.2 as the width of the gate electrode (29) after t he lithography, in other words, the channel width.

상기 리도그래피 후, 테트라 에톡시실란(Si(OC2HS)4)를 사용한 화학 기상 반응에 의해 0.3㎛의 막의 두께를 갖는 실리콘 산화막을 전면적으로 퇴적시킨다. 상기 퇴적막을 반응성 스피터 에칭에 의해 반도체 기판 표면과 수직방향으로 에칭하고, 평탄부에 퇴적된 실리콘 산화 퇴적막을 제거하면 게이트 전극(29) 및 필드 산화막(223)의 각 측벽부분에만 실리콘 산화 퇴적막(213)이 남게 된다. 다음에 0.8㎛두께의 포트 레지스트막을 웰(222)를 제외한 영역의 게이트 산화막(28)위에 남겨 놓고, 가속 에너지 70KeV의 조건에서 비소(As)의 이온주입을 행한다. 상기의 이온주입은 웰 영역(222)에 대해서는 게이트 산화막(28)을 거쳐서 행하여지고, 반도체 기판 표면에서 최대 불순물 농도로 되는 조건이다. 한편, 웰 영역(222)이외에 대해서는 상기 포트 레지스트막에 의해 주입 이온이 저지되어 반도체 기판(221)내에는 주입되지 않는다. 상기의 이온 주입후, 남겨진 포트 레지스트막을 제거하고 나서 주입 이온의 활성화, 열처리를 실시하고, N도 전형의 소오스(24) 및 드레인(25)를 형성한다(이상 제15도).

The silicon oxide film having the thickness of the film of 0.3㎛ with the chemical vapor deposition using the tetr aethoxysilane (Si(OC(SB)2(/SB)H(SB)S(/SB))(SB)4(/S B)) the extensively is sedimented after lithography. Th e heap film is etched to the surface of semiconductor s ubstrate and vertical direction with the reactive Peter etching and if the silicon oxidation heap film accumulat ed in the plateau is removed, the silicon oxidation heap film (213) remains in each sidewall portion of the field o xide film (223) and gate electrode (29). Next, the phot oresist film of 0.8㎛ thickness is left on the gate oxidati on film (28) of the domain except for the well (222) an d the ion implantation of the arsenic (As) is performed i n the condition of the acceleration energy 70KeV. The i on implantation described in the above is performed ab out the well region (222) after the gate oxidation film (28) and it is the condition consisting of the maximum i mpurity concentration in the surface of semiconductor substrate. In the meantime, the photoresist film hinder s the implant ion and it is not injected about the well r egion (222) except within the semiconductor substrate (221). After the photoresist film remaining is removed t he activation of the implant ion, and the thermal proce ss is performed after the ion implantation described in t he above and N forms the source (24) and drain (25) o f the model (over the 15).

그리고, 상기의 소오스 및 드레인 확산층(24), (25)의 각각의 표면 불순물 농도는 찬넬 길이가 0.5㎛이상 일때에는 3#215#1018, 0.3㎛이하 일때에는 1#215#1018㎝-3으로 최종적으로 형성되도록 비소(As) 이온 양을 설정한다. 도, 상기의 소오스(24), 드레인(25)의 확산층의 접합 깊이가 최종적으로 0.25㎛가 되도록 상기의 열처리 조건을 제어한다. 상기 열처리후, 웰 영역(222)위에만 0.8㎛두께의 포트 레지스트막으로 덮고, 붕소를 가속 에너지 70KeV의 조건으로 이온 주입을 행한다. 상기의 이온 주입에 의해 웰 영역(222)이외의 영역에 있어서 게이트 산화막(28)을 거쳐서 붕소가 반도체 기판(221)에 주입되고, 그 최대 불순물 농도는 반도체 기판(221)의 표면이었다. 웰 영역(222)에 있어서는 상기 포토 레지스트막에 의해 이온 주입이 저지되어 반도체 기판(221)내에 주입되지 않는다. 상기의 이온주입 후, 남겨진 포트 레지스트막을 제거하고 나서 주입 붕소 이온의 활성화 열처리를 실시하고, P도전형의 소오스(26)및 드레인(27)을 형성한다(이상 제16도 참조).

And the source described in the above and drain diffusion layer (24), and each surface impurity concent ration of (25) are for the establishment of the arsenic (As) ion dose when it is less than 3× 10 18 , 0.3㎛ whe n the channel length is 0.5㎛, the finally is formed with 1× 10 18 ㎝ - 3 . Drawing, the source (24) described in the above, and the junction depth of the diffusion laye r of the drain (25) control the heat treatment condition described in the above so that 0.25㎛ finally. It covers up with the photoresist film of 0.8㎛ thickness on the p ost-baking, and the well region (222) and boron the ion implantation is performed into the condition of the acce leration energy 70KeV. Boron was injected with the ion implantation described in the above as to the domain e xcept the well region (222) after the gate oxidation film (28) in the semiconductor substrate (221) and the max imum impurity concentration was the surface of the se miconductor substrate (221). It is in the well region (2 22) and the photoresist film hinders the ion implantatio n and it is not injected within the semiconductor substr ate (221). After the photoresist film remaining is remov ed the activation annealing of the injection boron ion is performed after the ion implantation described in the a bove and the source (26) and drain (27) of P conductiv ity type are formed (over the 16 is the reference).

상기 소오스(26) 및 드레인(27)의 확산층의 각각의 표면 불순물 농도는 최종적으로 3종류의 조건 3#215#1017㎝-3, 1#215#1018㎝-3로 되도록 주입 붕소량을 설정한다. 또, 소오스(26)및 드레인(27)의 확산층의 접합 깊이가 최종적으로 0.25㎛로 되도록 상기의 열처리 조건을 제어한다. 상기 열처리 후, 반도체 기판(221)위에 노출되어 있는 게이트 산화막을 제거하

Each surface impurity concentration of the diffusion layer of the source (26) and drain (27) are for the esta blishment of finally, the condition 3× 10 17 ㎝ - 3 of 3 kind, and 1× 10 18 ㎝ - 3 , as as possible, the injection boron amount. And finally the junction depth of the diff usion layer of the source (26) and drain (27) control th

GF Exhibit 1124 - 1919/2704

고 나서 50㎚의 막의 두께를 갖는 백금(Pt)을 스피터링 법에 의해 전면에 증착하고, 계속하여 450℃의 열처리를 실시한다. 상기의 저온 열처리에 의해 반도체 기판(221)의 표면에 노출하고 있는 소오스 확산층 영역(24) 및 (26), 드레인 확산층 영역(25) 및 (27)의 각 표면 부분에 백금 실리사이드(PtSi)층(214)가 자기 정합적으로 형성된다. 상기의 열처리에 있어서 필드 산화막(223), 측벽 퇴적 산화막(213) 및 보호 산화막(212)위에서 백금(Pt)은 반응하지 않으므로 실리사이드층(214)는 형성되지 않는다. 상기의 저온 열처리 후, 왕수로 전면적에 백금(Pt)을 에칭한다. 백금 실리사이드(PtSi)는 왕수로 제거되지 않아 소오스 확산층(24) 및 (26)과 드레인 확산층(25) 및 (27)위에만 자기 정합적으로 남게 된다. 이 시점에서는 N도전형의 소오스(24) 및 드레인(25)영역에 있어서의 백금 실리사이드(PtSi)층(214)의 바로 아래에는 백금 실리사이드층 형성전의 표면 불순물 농도보다도 1자리수 높은 불순물 농도를 갖는 약 10㎚두께의 석출층의 백금 실리사이드(PtSi)층(214)에 대해 자기 정합적으로 형성된다.

e heat treatment condition described in the above to 0.25㎛ as as possible. The platinum (Pt) which has the thickness of the film of 50㎚ after it removes the gate oxidation film exposed on the post-baking, and the sem iconductor substrate (221) is deposited on front with t he spirofluorene method and then, the thermal process of 450℃ is performed. The platinum-silicide (PtSi) layer (214) is formed in the source diffusion layer domain (2 4) and (26) exposing on the surface of the semiconduc tor substrate (221), and each surface part of (27) and drain diffusion layer domain (25) with the anneal descri bed in the above into the self-alignment manner. The si licide layer (214) is not formed since the platinum (Pt) does not react as to the thermal process described in t he above in the field oxide film (223), and the sidewall deposition oxide layer (213) and passivation (212). The platinum (Pt) is etched to the aqua regia after the ann eal described in the above. The platinum-silicide (PtSi) is not removed to the aqua regia and it remains as the self-alignment manner on the source diffusion layer (2 4), (26), the drain diffusion layer (25) and (27). At this moment, it is formed with the self-alignment manner ab out the platinum-silicide (PtSi) layer (214) of the precip itation layer of about 10㎚ thickness having the impurit y concentration which the single digit is beneath higher than the surface impurity concentration of the platinum silicide layer formation total of the platinum-silicide (Pt Si) layer (214) in the source (24) of N conductivity typ e and drain (25) domain.

백금 실리사이드층(214)형성후, 모노실란(SiH4)과 산소(O2)의 화학 기상 반응에 의해 약 500㎚두께의 실리콘 산화막(210)을 전면에 퇴적하고, 소오스(24) 및 (26), 드레인(25) 및 (27)위, 또 게이트 전극(29)위의 접촉구멍을 구성시키는 부분의 상기 실리콘 산화막(210)를 리도그래피에 의해 선택적으로 제거한다. 상기의 실리콘 산화막(210)의 선택적 제거를 한 후, 상기 공정에 사용한 포트 레지스트막을 남겨둔 채, 티타늄(Ti)와 텅스텐(W)의 동시 스퍼터에 의해 TiW 막(215)를 전면에 피착시킨다. 그후, 상기 포토 레지스트막을 제거하지만, 이 공정에 의해 포트 레지스트막 위의 TiW막도 동시에 제거되기 때문에 실리콘 산화막(210)이 제거된 영역에만 선택적으로 TiW막(215)가 남게 된다. 최후로 바라는 회로구성에 따라서 알루미늄(Al)에 의한 배선(211)을 형성한다(이상 제17도 참조).

The silicon oxide film (210) of about 500㎚ thickness is accumulated after the platinum silicide layer (214) form ation with the chemical vapor deposition of the oxygen (O(SB)2(/SB)) and monosilane (SiH(SB)4(/SB)) in the fr ont side and after the silicon oxide film (210) of the par t organizing the contact hole above the gate electrode (29) is selectively removed with lithography and the sel ective removal of the silicon oxide film (210) described i n the above is done with the source (24) and (26), and the drain (25) and (27) the upper part the photoresist film used in the process is left. The TiW film (215) is at tached in the front side with the same time sputtering of the tungsten (W) and titanium (Ti) thereafter the ph otoresist film is removed. However because the simulta neously the TiW film above the photoresist film is remo ved using this process the TiW film (215) selectively re mains in the domain from which the silicon oxide film (2 10) is removed the wiring (211) by the aluminum (Al) is formed according to the circuit configuration which it la stly hopes in their heart (over seventeenth is the refer ence).

그리고, TiW막(215)는 알루미늄 배선(211)과 실리사이드층(214)의 반응을 방지하기 위해서 필요하게 된다.

And the reaction is necessary so that the TiW film (215) prevent the reaction of the silicide layer (214) an d aluminium wiring (211).

다음에, 상기 제조 공정에 의해서 제조된 CMOSFET에 관하여 우선, 소오스와 드레인 사이의 내압을 측정하였을때, 다음의 결과를 얻었다. 즉, P도전형의 소오스(26) 및 드레인(27)의 각 확산층에 있어서의 표면 불순물 농도를 3#215#1037㎝-3

Next, first when the internal pressure between the drain and the source were measured about CMOSFET m anufactured by the manufacturing process , the followi ng result was obtained. That is, it was in PMOS setting

GF Exhibit 1124 - 1920/2704

으로 설정한 PMOS에 있어서는 쇼트키 특성을 나타내지만, 찬넬 길이가 0.2㎛이상의 MOSFET의 내압은 약 5V의 값을 얻을 수가 있었다. 이 값은 P전형 드레인 표면 불순물 농도가 1018㎝-3이상에서 구성되는 종래 구조의 MOSFET에 있어서의 내압의 2배 이상의 값이다. P도전형 드레인 표면 불순물 농도를 1#215#1018㎝-3으로 설정한 PMOS에 있어서는 P+N접점에 따른 트랜지스터 특성을 표시하지만, 그 소오스와 드레인 사이의 내압은 찬넬 길이가 0.3㎛이상의 MOSFET에 있어서 6.5 내지 7V로 되었다. 이 값은 종래의 값에 비해서 1.6 내지 1.7 배 이며, 고내압화가 실현된 것을 나타내고 있다. 또, P도전형 드레인 표면 불순물 농도를 3#215#1018㎝-3로 설정한 PMOS있어서도 P+N접합에 따르는 특성을 나타내지만, 그 소오스와 드레인 사이의 내압은 찬넬 길이가 0.5㎛이상의 MOSFET에 있어서는 약 12V로 되었다. 이 값을 종래의 값에 비해서 2V 이상 높고, 고내압이 실현되게 된다.

up the surface impurity concentration in each diffusion layer of the source (26) of P conductivity type and drai n (27) as 3× 10 37 ㎝ - 3 and the schottky property w as shown. However the channel length the internal pre ssure of MOSFET more than 0.2㎛ could obtain the valu e of about 5V. This value is the value in which P model drain surface impurity concentration is formed in 10 18 ㎝ - 3 or greater more than two times of the internal pr essure in MOSFET of the conventional structure. It wa s in PMOS setting up P conductivity type drain surface impurity concentration as 1× 10 18 ㎝ - 3 and the tran sistor characteristic according to the P+N contact poin t was indicated. However in the internal pressure betw een the drain and the source, the channel length were as to MOSFET more than 0.3㎛ to 6.5 through 7V. This value is 1.6 through 1.7 times in comparison with the c onventional value and it shows that the high voltage-r esistant is realized. And even by being PMOS setting u p P conductivity type drain surface impurity concentrat ion as 3× 10 18 ㎝ - 3 the property of following the P+ N junction was shown. However it was in MOSFET more than 0.5㎛ and in the internal pressure between the dra in and the source, the channel length were to about 12 V. It is this value high in comparison with the conventi onal value over 2V and the high voltage-resistant is re alized.

N도전형의 소오스(4) 및 드레인(5)의 각 확산층에 있어서의 표면 불순물 농도를 3#215#1018㎝-3으로 설정한 NMOS에 있어서 찬넬 길이가 0.5㎛이상의 MOSFET에 있어서는 그 소오스와 드레인 사이의 내압은 약 10V이었다. 이 값은 종래의 값에 비해서 약 2배의 값이며, 고내압화가 되게 된다. 드레인 표면 불순물 농도를 1#215#1018㎝-3으로 설정한 NMOS에 있어서도 소오스(24) 및 드레인(25)와 실리사이드층(214)의 사이에는 양호한 음특성이 확보되어 P+N 접합에 따흐는 트랜지스터 특성이 얻어졌다. 그 소오스와 드레인 사이의 내압은 찬넬 길이에 의존하고, 찬넬 길이가 0.3㎛MOSFET에서는 약 3V로 되었다. 이들의 값은 종래 구조의 NMOS에 있어서의 소오스와 드레인 사이의 내압에 비해서 2배 이상의 고내압화로 된다.

It was in MOSFET more than 0.5㎛ and the channel length the internal pressure between the drain and the source was about 10V as to NMOS setting up the surfa ce impurity concentration in each diffusion layer of the source (4) of N conductivity type and drain (5) as 3× 10 18 ㎝ - 3 . This value is the value of about two time s in comparison with the conventional value and it bec omes the high voltage-resistant. In the interval of the source (24) as to NMOS setting up the drain surface im purity concentration as 1× 10 18 ㎝ - 3 and drain (25) and silicide layer (214), the good negative characteristi c was secured and as to ***, the transistor characteri stic was obtained in the P+N junction. The internal pre ssure between the drain and the source depended on t he channel length and the channel length was in 0.3㎛ MOSFET to about 3V. Their value is in comparison with the internal pressure between the source in NMOS of t he conventional structure and the drain to the high vol tage-resistant more than two times.

본 실시예에 따른 CMOSFET에 있어서의 NMOS 및 PMOS의 소오스와 드레인 사이의 내압은 제13도에 도시한 해석결과의 매우 잘 일치하고 있으며, 상기 해석의 타당성이 증명되게 된다. 즉, 본 실시예에 의하면 0.5㎛이하의 찬넬 길이를 갖는 초미세 CMOSFET의 소오스와 드레인 사이의 내압을 종래에 비해서 2배이상 향상시킬 수가 있다. 구체적으로는 찬넬 길이가 0.5㎛이상의 CMOSFET에 있어서는 NMOS 및 PMOS의 각 소오스 및 드레인 확산층 표면 불순물 농도를 3#215#1018㎝-3으로, 찬넬 길이가 0.3㎛일때에는 상기 불순물 농도를 1#215#1018㎝-3로 설정해서 본 실시예에 따라 MOSFET를 완성시키면, 각각 10V 및 6V의 고내압 초미세 COMSFET를 얻을 수가 있다. 또, 찬넬길이가 0.2㎛일때에는, PMOS의 소오스 및 드레인 확산층이 표면 불순물 농도를 3#215#1017㎝-3으로, NMON의 상기 표면 불순물 농도를 1#215#1018㎝-3에 각각 설움직여써하고, 본 실시예에 따라서 MOSFET를 완성시키면, 소오스와 드레인 사이의 내압 3V의 초미세 CMOSFET를 얻을 수가 있다. 상기의 MOSFET에 있어서 POMS의 소오스(26)

The internal pressure between the source of NMOS in CMOSFET according to this embodiment and PMOS and drain very well coincide with Figure 13 and it shows the feasibility of the interpretation is proved. That is, accor ding to this embodiment, in comparison with the conve ntional invention, the internal pressure between the so urce of the ultra-fine CMOSFET having the channel len gth less than 0.5㎛ and the drain can be improved over two times. Specifically, if it is in CMOSFET more than 0.5㎛ and when the channel length is 0.3㎛, the impurit y concentration is set up as 1× 10 18 ㎝ - 3 and accor ding to the present preferred embodiment, the channel length completes MOSFET each source of NMOS and P MOS and drain diffusion layer surface impurity concentr ation to 3× 10 18 ㎝ - 3 , the high voltage-resistant ult ra-fine COMSFET of 6V and 10V can be obtained. And when the channel length was 0.2㎛ , the source and dr ain diffusion layer of PMOS were the surface impurity c

GF Exhibit 1124 - 1921/2704

및 드레인 (27)과 실리사이드층(214)의 사이에는 쇼트키 장벽이 형성되지만, 특성상 문제로 되지 않는다. 이 쇼트키 장벽은 오히려 내 래치 업 특성을 향상시키는 기능을 갖추고 있다.

oncentration of NMON the surface impurity concentrati on the sorrow work to 3× 10 17 ㎝ - 3 in 1× 10 18 ㎝ - 3 and according to the present preferred embodiment, i f MOSFET is completed , the ultra-fine CMOSFET of the internal pressure 3V between the source and the drain can be obtained. In the interval of the source (26) of P OMS as to the MOSFET described in the above and drai n (27) and silicide layer (214), the Schottky barrier is f ormed. However it does not consist of the property pro blem. This Schottky barrier has the function rather of i mproving my latch up property.

다음에, 본 실시예에 표시한 제조 공정에 의해 제조된 CMOSFET에 대해서 내 래치 업 특성을 평가한다. 내 래치 업 특성으로서는 다음의 것을 측정한다. 즉, NMOS의 드레인(25)를 에미터, 웰(22)를 베이스, 반도체 기판(21)를 콜렉터로 하는 기생 NPN트랜지스터의 전류 이득률 #946#N과 PMOS의 소오스(26)을 에미터, 반도체 기판(21)을 베이스, 웰(22)를 콜렉터로 하는 기생 PNP트랜지스터의 전류 이득률 #946#P와의 곱 #946#N#183##946#P를 측정하였다. 이 측정에서는 베이스와 콜렉터 사이에 5V의 전압을 인가하고, 10-6내지 10-2A의 범위의 에미터 전류의 함수로서 #946#N#183##946#P를 구하였다. 그 결과, PMOS 및 NMOS의 각 드레인 표면 불순물 농도가 3#215#1018㎝-3 찬넬 길이가 0.5㎛의 CMOSFET상기 각 드레인 표면 불순물 농도가 1#215#1018㎝-3 찬넬 길이가 0.3㎛의 CMOSFET 및 PMOS의 드레인 표면 불순물 농도가 3#215#1017㎝-3, NMOS의 상기 표면 불순물 농도가 1#215#1018㎝-3 찬넬 길이가 0.2㎛의 CMOSFET에 있어서의 각 #946#N#183##946#P의 곱의 최고 값은 모두 10-2 내지 10-4이었다. 상기의 값은 래치 업이 발생할 수 있는 조건 #946#N#183##946#P〉 1을 만족시킬수 있는 것은 아니며, 또 ,PMOS의 드레인을 쇼트키 접합으로, NMOS의 드레인을 통상의 높은 불순물 농도 N+P접합으로 구성한 CMOSFET에 있어서의 #946#N#183##946#P 곰의 값 10-2와 거의 같던가 그 이하의 값이다. 상기의 결과에서 PMOS의 드레인 확산층을 낮은 불순물 농도로 설정한 COMSFET에 있어서는 내 래치 업의 관점에서 오히려 소오스와 드레인 사이의 내압의 향상의 관점에 있어서 NMOS의 드레인 표면 불순물 농도의 최적조건을 바라는 찬넬 길이에 따라서 설정하면 좋은 것으로 된다.

Next, my latch up property is evaluated about CMOSFET manufactured by the manufacturing process of indicating in this embodiment the following is measur ed as my latch up property in other words, the drain (2 5) of NMOS is emitted and the current gain modulus βN of the parasitism NPN transistor doing the base, and th e semiconductor substrate (21) about the well (22) to the collector and source (26) of PMOS are emitted and the double βN·βP with the current gain modulus βP of t he parasitism PNP transistor doing the base, and the w ell (22) about the semiconductor substrate (21) to the collector was measured the voltage of 5V is applied in t his measurement between the base and collector The β N·βP was saved as the function of the emitter current of the range of 10 - 6 to 10 - 2 A 1× 10 18 ㎝ - 3 chan nel length of 3× 10 17 ㎝ - 3 , and the surface impurity concentration of NMOS of CMOSFET of 0.3㎛ and drain surface impurity concentration of PMOS of 1× 10 18 ㎝ - 3 channel length of the CMOSFET each drain surface impurity concentration of 0.5㎛ of 3× 10 18 ㎝ -3 chan nel length of each drain surface impurity concentration of NMOS and PMOS the highest value of the double of each βN·βP in CMOSFET of 0.2㎛ was altogether 10 - 2 to 10 - 4 it is not consequently the value described in the above satisfies the condition βN·βP>1 in which the latch up can be generated. And it is better that the dr ain of the ,PMOS is set up according to the channel len gth which is in COMSFET which is nearly the same as t hat of the value 10 - 2 of the βN·βP bear in CMOSFET organizing the drain of NMOS on the high impurity conc entration N+P junction to the Schottky barrier it is the value of less sets up the drain diffusion layer of PMOS as the low impurity concentration in the result describe d in the above and rather hopes the optimal condition of the drain surface impurity concentration of NMOS in the viewpoint of my latch up as to the viewpoint of the improvement of the internal pressure between the sour ce and the drain.

다음에 본 실시예에 의한 CMOSFET에 있어서 NMOS 및 PMOS의 각 드레인 표면 불순물 농도를 5#215#1018내지 1020㎝-3으로 설정한 찬넬 길이 0.2 내지 1.0㎛의 COMSFET도 동시에 제조하고, 그 소오스와 드레인 사이의 내압 및 내 래치 업 특성을 측정하였다. 상기 COMSFET의 소오스 드레인 사이의 내압은 종래의 값보다 최대 수 V로 개선되고, 또 #946#N#183##946#P곱도 1이하이었지만, 상술의 결과에 비하면 약간 뒤떨어지는 특성이었다.

Next, COMSFET of the channel length 0.2 through 1.0 ㎛ setting up each drain surface impurity concentration of PMOS and NMOS as 5× 10 18 to 10 20 ㎝ - 3 as to CMOSFET by this embodiment simultaneously manufact ured and the internal pressure between the source and the drain and my latch up property were measured. Th e internal pressure between source and drain of COMSF ET were improved with the maximum number V than th e conventional value and and, the βN·βP double was 1 or less. However it was the property of being a little bit inferior if the property compared to the result of the de tailed description.

GF Exhibit 1124 - 1922/2704

[실시예 8]

제18도 및 제19도는 본 발명의 제8의 실시예를 도시한 CMOSFET의 제조 공정의 단면 구조도이다.

제15도에 도시한 상술한 제7의 실시예에 있어서 실리콘 산화 퇴적막(213)를 게이트 전극(29)및 필드 산화막(23)의 측벽부에만 자기 정합적으로 남겨둔 후, 노출되어 있는 게이트 산화막을 완전히 제거한다. 다음에, 지클로루실탄(SiH2Cl)과 염산(HCL)의 화학기상반응을 775℃의 온도로 행하고, 0.3㎛의 두께의 다결정질 또는 비정질의 실리콘 박막(216)을 웰(222)표면 위 및 N도전형을 유지하고 있는 반도체 기판(21)표면 위에 선택적으로 퇴적시킨다(이상 제18도 참조). 상기 실리콘 퇴적막의 형성조건은, 지클로루실란200cc, 염산 60cc의 조건으로 퇴적속도는 10㎚/분이다. 이 조건에 있어서는 피퇴적 표면에 실리콘 질화막(SiN4)이 존재하지 않는 한 실리콘 기판 위에만 선택적으로 퇴적하고, 또 측벽 절연막(213)과의 경계부에 있어서도 소위 파셋(facet)이라 하는 오목 볼록이 없는 평탄한 현상을 얻을 수가 있다.

실리콘 박막(216)의 퇴적후, 웰 영역(222)위의 실리콘 박막 부분에만 이온 주입이 행하여지도록 포토 레지스트막을 선택적으로 형성하고, 붕소 이온 주입을 실시한다. 붕소 주입량은 상기 실리콘 박막(216)내의 불순물 농도가 웰 (222)표면의 불순물 농도와 일치하도록 설정한다. 주입 에너지는 25KeV이다. 그후, 이온 주입의 마스크에 사용한 포토 레지스트막을 제거하고 나서 1150℃, 15초의 조건으로 고온 단시간 열처리를 실시하고, 주입 이온의 활성화와 실리콘 박막(216)의 단결정화를 행한다. 사전에 다결정질, 또는 비정질로 형성된 실리콘 박막(216)내에 있어서 불순물의 확산 계수는 단결정 실리콘 내에 있어서의 확장 계수에 비해서 10 내지 20배나 크다. 따라서, 상기의 단시간 열처리에 의해 웰(222)위의 실리콘 박막(216)에 주입된 붕소는 실리콘 박막(216)내에서 깊이 방향에 대해 대략 균일하게 분포한다. 상기 열처리를 한 후, 상술의 제7의 실시예에 따라서 N도전형의 소오스(24) 및 드레인(25)와 P도전형의 소오스(26) 및 드레인(27)을 형성한다. 상기의 단시간 고온 열처리에 의해 실리콘 박막(216)은 이미 단결정화 되어 있다. 따라서, 상기의 각 소오스 및 드레인의 형성 조건은 상기 제7의 실시예의 경우와 같은 조건으로 실시된다. 그후의 공정도 상술한 제7의 실시예에 따라서 CMOSFET를 제조한다(이상 제19도 참조).

제19도에 표시한 제8실시에 따른 CMOSFET는 상술한 제7의

[Embodiment 8]

With Figure 18. And figure 19 is a sectional configuration of the manufacturing process of CMOSFET showing the embodiment of the eighth of the invention.

In a preferred embodiment, after the silicon oxidation heap film (213) is left in the sidewall part of the field oxide film (23) and gate electrode (29) of the above-described seventh shown in Figure 15 through the self-alignment manner the exposed gate oxidation film is completely removed. Next, the chemical vapor deposition of the hydrochloric acid (HCL) and paper chloro bullet (SiH(SB)2(/SB)Cl) is performed into the temperature of 775℃ and the polycrystalline of the thickness of 0.3㎛ or the amorphous silicon thin film (216) the selectively is sedimented on the semiconductor substrate (21) surface maintaining the well (222) surface the upper part and N conductivity type (over eighteenth is the reference). The formation condition of silicone heap film is the paper chloro silane 200cc, and the condition of the hydrochloric acid 60cc the deposition rate are 10㎚/. It is in this condition and as long as the silicon nitride film (SiN(SB)4(/SB)) is nonexistent in the blood deposition surface it selectively accumulates in on silicon substrate and the even phenomenon without the concave-convex that it is the so-called facet as to and, the border of the side wall insulating film (213) can be obtained.

The photoresist film is selectively formed so that the ion implantation is performed after the deposition of the silicon thin film (216) in the silicon thin film part above the well region (222) and the boron ion implantation is performed. The boron injection level sets up so that the impurity concentration within the silicon thin film (216) coincides with the impurity concentration of the well (222) surface. The implant energy is 25KeV. Thereafter, after the photoresist film used in the mask of the ion implantation is removed the rapid thermal annealing is performed to 1150℃, and the condition of 15 second and the activation of the implant ion and monocrystallization of the silicon thin film (216) are performed. In advance, it is in the silicon thin film (216) formed with the polycrystalline or the amorphous and the diffusion coefficient of the impurity is large in comparison with the coefficient of expansion in inside of the single-crystal silicon as 10 through 20 times. Therefore, the boron injected with the RTA described in the above in the silicon thin film (216) above the well (222) is distributed to uniform approximately in the silicon thin film (216) about the longitudinal direction. After it heat-treats at the above the source (26) of the source (24) of N conductivity type and drain (25) and P conductivity type and drain (27) are formed according to the seventh embodiment of the detailed description. The already the silicon thin film (216) is single crystallized with the RCA described in the above. Therefore, the formation condition of the drain and each source described in the above is performed to the condition like the case of the seventh embodiment. According to the seventh embodiment in which the process of the after describes in detail, CMOSFET is manufactured (over nineteenth is the reference).

CMOSFET according to the eighth operation indicated

GF Exhibit 1124 - 1923/2704

실시예에 따른 CMOSFET와 동일 치수를 갖고 있으며, 양자의 소오스와 드레인 사이의 내압을 비교하였을때, 찬넬 길이 0.3㎛, 소오스 및 드레인 표면 불순물 농도 1#215#1018㎝-3의 조건에 있어서의 제8실시예의 CMOSFET의 쪽이 약 1V만큼 높고, 7V의 내압이 얻어졌다. 또, 찬넬 길이 0.2㎛, NMOS 및 PMOS의 드레인 표면 불순물 농도가 각각 1#215#1018㎝-3 및 3#215#1017㎝-3의 조건으로 구성된 제8실시예의 CMOSFET의 내압을 측정하고, 상술한 제7실시예의 CMOSFET의 내압과 비교하였을때, 전자의 쪽이 약 2V높은 5V의 값을 얻었다. 상기의 값은 종래 구조에 따른 CMOSFET의 소오스, 드레인 사이의 내압과 비교해서 3배 이상의 고내압화를 실현한 것으로 된다. 제8의 실시예에 따르는 CMOS FET에 있어서 기생 바이폴라 트랜지스터에 관한 전류 이득률의 금 #946#N#183##946#P를 여러가지의 찬넬 길이, 소오스 및 드레인 표면 불순물 농도를 갖는 경우에 대해서 측정하였으나, 모두 상술의 제7실시예에 따른 CMOSFET의 측정값에 비해서 2/3 내지 1/2로 저감화 되어 있었다. 이와 같이, 제8실시예에 따른 CMOSFET는 제7실시예에 따른 CMOSFET보다 소오스와 드레인 사이의 내압 및 내 래치 업 특성에 있어서 향상하고 있지만, 그 이유는 소오스 및 드레인의 각 접합이 반도체 박막(216)내에 설치된 것에 의해 접합 면적이 저하하고, 또한 실효 찬넬 길이가 증가하였기 때문이라고 생각된다.

in Figure 19 had the same dimension as CMOSFET according to the above-described the seventh embodiment and when the internal pressure between the source of both sides and the drain was compared , the channel length 0.3㎛, and the side of CMOSFET of the eighth preferred embodiment in the condition of the source and drain surface impurity concentration 1× 10 18 ㎝ - 3 were high as about 1V and the internal pressure of 7V was obtained. And the internal pressure of CMOSFET of the eighth preferred embodiment consisting of channel length 0.2㎛, and the drain surface impurity concentration of NMOS and PMOS is the condition of 1× 10 18 ㎝ - 3 and 3× 10 17 ㎝ - 3 was measured and when it compared with the internal pressure of CMOSFET of the above-described the seventh preferred embodiment , the side of the electron about 2V obtained the value of 5V. It compares with the source of CMOSFET according to the conventional structure, and the internal pressure between the drain and the value described in the above realizes the high voltage-resistant more than the treble. In case of having the channel length of the various, and the source and drain surface impurity concentration the gold βN·βP of the current gain modulus about the parasitic bipolar transistor was confronted as to the CMOS FET followed the eighth embodiment and it measured. But the altogether became decreasing in comparison with the measured value of CMOSFET according to the seventh preferred embodiment of the detailed description to 2/3 through 1/2. In this way, CMOSFET according to the eighth preferred embodiment improves than CMOSFET according to the seventh preferred embodiment as to the internal pressure between the source and the drain and my latch up property. However the junction area is degraded by the result of that reason for the each junction of the drain and source is installed within the semiconductor film (216) and it is regarded that moreover, the effectiveness channel length was due to increase.

[실시예 9]

[Embodiment 9]

제20도 및 제21도는 본 발명의 제9의 실시예를 표시한 CMOSFET의 단면구조도와 N도전형의 드레인 확산영역에서의 깊이 방향에 관한 불순물 농도 분포도이다.

With Figure 20. And figure 21 is an impurity concentration distribution drawing about the longitudinal direction at the drain diffusion region of the sectional configuration of CMOSFET indicating the ninth embodiment and N conductivity type of the invention.

제18도에 도시한 제8실시예에 있어서 다결정질, 또는 비정질의 실리콘 박막(216)을 반도체 기판(221)위에 자기 정합적으로 퇴적시킨 후, 웰 영역(222)위의 실리콘 박막 부분에만 이온 주입이 행하여지도록 다른 영역 표면위에 포토 레지스트막을 남겨 놓는다. 그후, 웰 영역9222)위의 실리콘 박막 부분에 비소의 이온 주입을 행하고 나서 상기의 남겨진 포트 레지스트막을 제거한다.

After the polycrystalline or the amorphous silicon thin film (216) is sedimented with the self-alignment manner in Figure 18 as to the eighth preferred embodiment shown on the semiconductor substrate (221) the photoresist film is left on the dissimilar domain surface so that the ion implantation is performed in the silicon thin film part above the well region (222). Thereafter, the photoresist film remaining described in the above is removed after the ion implantation of arsenic is performed in the silicon thin film part above the well region 9222).

다음에, 웰 영역(222)를 포토 레지스트막으로 덮고, 웰 영역(222)이외의 N도전형을 갖는 반도체 기판(221)위의 실리콘 박막 부분에만 이온 주입이 행하여지도록 재차 포트 레지스트막을 남겨 놓는다. 그후, 붕소를 이온 주입하고, 재차 포토 레지스트막을 완전히 제거해서 실리콘 박막(216)의 표면을 노출시킨다. 이상태에서 1100℃, 30초의 조건의 단시간 고온 열처

Next, the well region (222) is covered up with the photoresist film and the photoresist film is left again so that the ion implantation is performed in the silicon thin film part above the semiconductor substrate (221) having N conductivity type except the well region (222). Thereafter, boron is ion-implanted and the photoresist fil

GF Exhibit 1124 - 1924/2704

리를 실시한다. 상기 조건의 열처리을 행하여도 실리콘박막(216)은 단결정화 되지 않고, 다경정질 또는 비정질의 상태를 유지하고 있다. 다결정질, 또는 비정질의 실리콘 박막(216)내에 있어서의 불순물의 확산 계수는 상술과 같이 매우 큰 값이기 때문에 상기 조건에 의한 단시간 열처리에 의해서 실리콘 박막(216)내에서 비소 및 붕소는 고속으로 거의 균일한 농도 분포로 된다. 그러나, 반도체 기판(21)내에 있어서의 각 불순물의 확산 계수는 상대적으로 작고, 상기 단시간의 열처리에 의해서는 반도체 기판(21)내에 약 20㎚정도밖에 확산되지 않았다.

m is again completely removed and the surface of the silicon thin film (216) is exposed. In this state, 1100℃, and RCA of the condition of 30 second are performed. The silicon thin film (216) is not single crystallized even if the thermal process of the condition is performed and the multi-stem chiseling or the amorphous state is maintained. Because it is the big value the diffusion coefficient of the impurity in the polycrystalline or the amorphous silicon thin film (216) in very consists of the concentration distribution in which arsenic and boron are nearly uniform at high speed like the detailed description with RTA by the condition in the silicon thin film (216). But relatively the diffusion coefficient of each impurity in the semiconductor substrate (21) in was small and it was according to due to the thermal process of the short time and it was not diffused within the semiconductor substrate (21) about 20㎚.

이와 같이 비소 및 붕소의 이온 주입과 그에 따르는 단시간 열처리에 의해 실리콘 박막(216)과 웰(222) 및 N도전형 반도체 기판(221)내에 각각 N도전형의 소오스(24)와 드레인(25) 및 P도전형의 소오스(26)과 드레인(27)을 형성한다. 그후, 상기 각 소오스(24) 및 (26)과 드레인(25) 및 (27)위에 백금 실리사이드(PiSi)층(214)를 상술의 제7의 실시예에 따라서 자기 정합적으로 형성하고, 그후의 공정도 제7의 실시예에 따라서 실시하는 것에 의해 제20도에 도시한 CMOSFET를 제조할 수가 있다.

In this way, the source (26) of the source (24) of N conductivity type and drain (25) and P conductivity type and drain (27) are formed with the ion implantation of arsenic and boron and RTA followed that within the silicon thin film (216), the well (222) and N conductive semiconductor board (221). Thereafter, according to the seventh embodiment of the detailed description the platinum-silicide (PiSi) layer (214) on each source (24) and (26) and drain (25) and (27), it forms into the self-alignment manner and by the result of that the process of the after performs by the seventh embodiment CMOSFET shown can be manufactured at a rate per Figure 20.

제9실시예에 의한 CMOSFET의 N도전형 소오스(24) 및 드레인(25)의 불순물 농도 분포는 제21도에 도시한 바와 같이 3개의 영역 A, B, C로 분리된다. 즉, 실리사이드층(214)바로 아래에 있어서의 약 10㎚두께의 불순물 석출 영역A, 실리콘 박막(216) 내부의 균일 분포 영역 B 및 웰9222)내에 있어서의 접합 깊이 약 20㎚를 갖는 급격한 농도 분포 영역 C이다. P도전형 소오스(26) 및 드레인(27)내에 있어서는 상기 불순물 석출 영역 A의 존재는 인정되지 않았다.

It as shown in the impurity concentration distribution of N conductivity type source (24) of CMOSFET by the ninth preferred embodiment and drain (25) is Figure 21 is separated into the domain A of 3, B, and C. That is, the sudden concentration distribution domain C having the impurity precipitation domain A of about 10㎚ thickness in the lower part, and the junction depth about 20 ㎚ in the uniform distribution domain B of the silicon thin film (216) inside and well 9222) in the silicide layer (214). It was in P conductivity type source (26) and drain (27) and the presence of the impurity precipitation domain A was not recognized.

제9실시예에 따른 CMOSFET에 있어서는 상기 실리콘 박막(216)내의 균일 분포 농도로서, NMOS에 관해서는 1#215#1018㎝-3, 3#215#1018㎝-3, 1019㎝-3, 5#215#1019㎝-3의 각 값이, 또 PMOS에 관해서는 1#215#1017㎝-3, 3#215#1017㎝-3, 1#215#1018㎝-3, 3#215#1018㎝-3 및 5#215#1018㎝-3의 값이 최종적으로 되도록 비소 또는 붕소 이온 주입량을 설정하는 것에 의해서 MOSFET를 제조하였다. 또, 찬넬 길이에 관해서도, 0.1, 0.2, 0.3, 0.5 및 1.0㎛의 값일때에 대해서 MOSFET를 제조하였다. 상기 각종의 CMOSFET에 대해서 소오스와 드레인 사이의 내압 및 기생 바이폴라 트랜지스터의 각 전류 이득률의 곱 #946#N#183##946#P를 측정하였다. NMOS의 드레인(27)내의 균일 분포 불순물 농도가 1018㎝-3이상 일 때, 상기 특성 향상은 그다지 확인되지 않았다. 그러나, 상기 균인 분포 불순물 농도가 1017 내지 1019㎝-3의 낮은 불순물 농도로 설정되어 있을 때에는 특히 소오스와 드레인 사이의 내압의 향상이 현저하였다. 드레인 내의 균일 분포 불순물 농도가 1#215#1018㎝-3일 때 찬넬 길이가 0.1 및 0.2㎛의 각 CMOSFET에 있어서의 소오스와 드레인 사이의 내압은 각각 4.5 및 8 V에 달하였다. 이들이 값은 제8의 실시

It was in CMOSFET according to the ninth preferred embodiment and it was the uniform distribution concentration within the silicon thin film (216) and MOSFET was manufactured finally by the result of that the value of 5× 10 18 ㎝ - 3 and 1× 10 17 ㎝ - 3 , 3× 10 17 ㎝ - 3 , 1× 10 18 ㎝ - 3 , 3× 10 18 ㎝ - 3 of each value of 1 × 10 18 ㎝ - 3 , 3× 10 18 ㎝ - 3 , 10 19 ㎝ - 3 , 5× 10 19 ㎝ - 3 set up arsenic or the boron ion dosage about NMOS about and, PMOS as as possible. And MOSFET was manufactured about the value task time of 1.0㎛ and drawing about the channel length, 0.1, 0.2, 0.3, 0.5. The double βN·βP of each current gain modulus of the internal pressure between the source and the drain and parasitic bipolar transistor were measured about the various CMOSFET. The uniform distribution impurity concentration within the drain (27) of NMOS the characteristic improvement was not particularly confirmed over 10 18 ㎝ - 3 in the task. But when the distribution impurity concentration which was the bacteria was set up as the low impurity concentration of 10 17 to 10 19 ㎝ - 3 ,

GF Exhibit 1124 - 1925/2704

예에 따른 CMOSFET일 때에 비해서도 많이 개선되어 있으나, 이 효과는 찬넬 길이가 짧은 경우의 쪽이 상대적으로 현저하였다. PMOS에 있어서의 드레인(25) 내의 균일 분포 불순물 농도가 1017 내지 1018㎝-3미만으로 설정되고, 또한 게이트 길이가 0.1㎛일때에도 소오스와 드레인 사이의 내압은 제8의 실시예 일 때와 비교해서 수 V 향상되고 있으며, 그 값은 5V 이상에 달하였다.

especially, the improvement of the internal pressure between the source and the drain was remarkable. The channel length the internal pressure between the source in each CMOSFET of 0.1 and 0.2㎛ and drain reached 4.5 and 8 V when the uniform distribution impurity concentration within the drain was 1× 10 18 ㎝ - 3 . Even though the value compared when being CMOSFET according to the eighth embodiment these were improved. But relatively the side of the case where this effect the channel length was short was significant. The uniform distribution impurity concentration within the drain (25) in PMOS was set up as 10 17 to 10 18 ㎝ - 3 under and even when moreover, the gate length was 0.1㎛ it compared with the eighth embodiment task time and the internal pressure between the drain and the source were improved with the number V and the number of the value reached 5V or greater.

제9의 실시예와 제8의 실시예에 있어서의 이 효과의 차이는 드레인 최대 전계가 인가되는 낮은 불순물 농도 영역이 제9실시예일 때에는 실리콘 박막(216)내에서 제21에 도시한 바와 같이 대략 균일하게 형성되기 때문이고, 그에 의한 전계분산 효과가 된다고 생각된다.

As shown in the twenty first within the silicon thin film (216) the low concentration domain of impurities in which the drain maximum electric field the difference of this effect in the ninth embodiment and the eighth embodiment is applied is the ninth preferred embodiment, it is due to be formed to uniform approximately and it is regarded to become with electric field dispersion effect thereby.

또, 제9실시예에 따른 초미세 CMOSFET의 기생 바이폴라 트랜지스터의 곱 #946#N#183##946#P에 관해서는 제8실시예의 경우와 거의 변함이 없고, 래치 업 현상은 무시할 수 있는 정도이었다.

And the case there was no to nearly change about the double βN·βP of the parasitic bipolar transistor of the ultra-fine CMOSFET according to the ninth preferred embodiment with the case of the eighth preferred embodiment and it was the extent which the latch-up could ignore.

본 발명의 제1내지 제6의 실시예에 의하면, 최대 전계인가 영역이 드레인 확산층내에서 넓게 분산할 수 있으므로, 동일 구조 파라미터를 갖는 종래 구조의 트랜지스터 보다 5V이상이나 소오스와 드레인 사이의 내압을 향상할 수 있다. 따라서, 본 발명에 의하면 전원 정압을 종래의 5V에서 3V이하로 내리는 것과 같은 변경도 없이 실효 찬넬 길이가 0.5㎛이하의 미세 트랜지스터를 동작시킬수가 있다.

According to the first through the sixth embodiment of the present invention., it wides the maximum electric field approved area can be scattered in the drain diffusion layer. Therefore the internal pressure between the drain and the source can be improved than the transistor having the identical structure parameter of the conventional structure over 5V. Therefore, the effectiveness channel length can operate the minute transistor less than 0.5㎛ without the varying degree which according to the invention seems to drop the power source hydrostatic from the conventional 5V less than 3V.

본 발명의 제1 내지 제3의 실시예에 있어서는 PtSi층의 형성시에 있어서의 PtSi층 바로 밑의 불순물의 석출 효과를 이용해서 음 접촉에 필요한 불순물 농도 영역을 PtSi층과 자기 정합의 관계로 구성하였으나, 상기의 PtSi층은 Mo, W, Pb, Ni, Ti, Ta, Nb, Cr, Pr등의 다른 고융점 금속 또는 그들의 실리사이드 막으로 치환해서 구성하여도 지장이 없다. 또, 본 발명의 각 실시예에 있어서는 소오스 및 드레인 확산층을 P이온에 의해 형성한 이를 도시하였으나, 상기 확산층은 P이온에 의해서 형성하여도 좋다. 또, 그 형성 방법도 이온 주입에 한정되는 일없이 열 확산법 등 다른 공지의 수단에 의해서도 본 발명의 요지를 이탈하지 않는다. 또, 본 발명은 상기와 같은 단일체 트랜지스터에 한정되는 일이 없이 반도체 집적회로 장치에 대해서도 적용된다.

The concentration domain of impurities required for the negative principle in nature contact was gotten the relation of the self alignment and PtSi layer comprise by being in the first of the invention to the third embodiment and using the precipitation effect of the PtSi layer impurity immediately below in the formation time of the PtSi layer. But even if the ptSi layer described in the above substitutes with the high melting point metal or dissimilar their silicide films of the mo, W, pb, ni, ti, ta, nb, cr, the Pr etc and it configures there is no impediment. And it may be acceptable that this which was in each embodiment of the invention and formed the source and drain diffusion layer with P ion was shown. But the diffusion layer forms with P ion. And the gist of the invention is not broken away from without the task in which the formation method is restricted to the ion implantation with the different publicly known means. And it is applied to without the task in which the invention is restricted to the above-mentioned monolith transistor semico

GF Exhibit 1124 - 1926/2704

nductor integrated circuit device.

또, 제7 내지 제9도의 실시예에 의한 효과는 종래 구조에 있어서의 소오스와 드레인에 대응하는 영역을 개선하는 것에 의해 얻어지는 것으로, 결코 반도체 기판(221)의 농도를 증대시켜서 고냉압화를 도모하는 것은 아니다. 따라서, 반도체 기판 농도의 증대에 따르는 이동도의 저하를 조래하는 일도 없고 고속 동작을 손상하는 일도 없다.

And by improving the domain in which the effect by the embodiment of the seventh through Figure 9 correspon ds to the source in the conventional structure and drai n the domain is obtained. The concentration of the se miconductor substrate (221) is ever increased and the high cold press is not planned. Therefore, *** the task does the degradation of the mobility following the incre ase in semiconductor substrate concentration not have and there is no task injuring the high speed operation.

본 발명의 제7 내기 제9의 실시예에 의하면, 소오스 및 드레인 위에 고융점 금속 또는 그 실리사이드층이 형성되어있기 때문에 초미세 CMOSFET에 있어서도 그 시이트 저항는 수Ω/㎠으로 낮은 저항성을 유지할 수 있어 고속 동작을 보장할 수가 있다.

According to the embodiment of the seventh betting ninth of the present invention., because the high melti ng point metal or the silicide layer is formed on the sou rce and drain the low resistivity can be maintained with the number Ω / ㎠ which the sheet resistance is increa sed as to the ultra-fine CMOSFET and the high speed o peration can be guaranteed.

제7~제9의 각 실시예에 있어서는 소오스 및 드레인 확산층의 최대 불순물 농도에 관하여 1#215#1017㎝-3이상일 때에 대해서 기술하였으나, 이것은 제13도의 해석 결과 즉, 0.1㎛의 게이트 길이에 대하여서의 해석 결과에 따르고 있다. 0.1㎛의 값은 실현할 수 있는 최소의 게이트 길이이다. 또, 상기의 불순물 농도(1#215#1017㎝-3)이하에서 본 발명을 적용할 때에 제14도에서 추측할 수 있는 바와 같이 기판 전류의 증대 및 드레인 누설 전류의 증대를 초래하게 되는 것이다.

It was in each embodiment of the 7~ ninth and when being 1× 10 17 ㎝ - 3 or greater, it confronted and it d escribed about the maximum impurity concentration of the drain diffusion layer and source. But this follows th e interpretation result of Figure 13, in other words, the gate length of 0.1㎛ into the interpretation result at ** *. It is the minimum gate length which the value of 0.1 ㎛ can realize. And in the impurity concentration (1×10 (SP)17(/SP)㎝(SP)-3(/SP)) or less described in the abo ve, the increase in the substrate current it can guess and increase in drain leak electric current are caused in Figure 14 when applying the invention.

또, 제7~제9의 각 실시예에 있어서는 소오스 및 드레인 확산층 위에 백금 실리사이드(PtSi)층을 자기 정합적으로 형성하였으나, 이것은 일예로서 이 PtSi층 대신에 Mo, W, Pb, N, Ti, Ta, Nb, Cr, Pr등의 고융점 금속 또는 그 실리사이드 막을 사용할 수가 있다. 또, 각 실시예에 있어서는 단시간 열처리로서 고온 전기로를 사용하는 방법에 대해서 설명하였으나, 이 공정은 램프가열법, 레이저 또는 전자선 조사법등의 다른 방법에 의해서도 가능하다. 또, 각 실시예에 있어서는 P도전형 웰을 사용한 경우에 대해서 설명하였으나, 역으로 P도전형 반도체 기판내에 N도전형의 웰을 형성한 구조의 CMOSFET에 대해서도 본 발명을 적용할 수가 있다.

And it was in each embodiment of the 7~ ninth and the platinum-silicide (PtSi) layer was formed into the self-al ignment manner on the source and drain diffusion layer. But as an example, this instead of can use the high mel ting point metal or the silicide film of the mo, W, pb, N, ti, ta, nb, cr, the Pr etc with this PtSi layer. And it expl ained the method for being in each embodiment and usi ng the high temperature electric furnace as RTA. But t his process is possible with the dissimilar method includi ng the lamp heating method, the laser or the electronic beam irradiation method etc. And in case of being in ea ch embodiment and using P conductive well it confront ed and it illustrated. But the invention can be applied t o CMOSFET which reversely forms the well of N conduc tivity type within P conductive semiconductor board of the structure.

이상 설명한 바와 같이 본 발명에 의하면, 0.2㎛의 극히 짧은 찬넬 길이라도 5V의 통상 전원으로 동작 시킬수가 있고, 또 래치 업 현상을 방지할 수 있기 때문에 고속 동작을 손상시키는 일없이 초미세 CMOSFET를 실현하는 것이 가능하다.

As described above, although it is the channel length which is exceedingly short of 0.2㎛ the generally can a ctivate from the according to the invention to the pow er source of 5V and the injures the high speed operatio n because it can prevent and, the latch-up task is pos sible to realize the ultra-fine CMOSFET without the tas k which.

Disclaimer

본 문서는 특허 및 과학기술문헌 전용의 첨단 자동번역 시스템을 이용해 생성되었습니다. 따라서 부분적으로 오역의 가능성이 있으며, 본 문서를 자격을 갖춘 전문 번역가에 의한 번역물을 대신하는 것으로 이

GF Exhibit 1124 - 1927/2704

용되어서는 안 됩니다. 시스템 및 네트워크의 특성때문에 발생한 오역과 부분 누락, 데이터의 불일치등에 대하여 본원은 법적인 책임을 지지 않습니다. 본 문서는 당사의 사전 동의 없이 권한이 없는 일반 대중을 위해 DB 및 시스템에 저장되어 재생, 복사, 배포될 수 없음을 알려드립니다.
(The document produced by using the high-tech machine translation system for the patent and science & technology literature. Therefore, the document can include the mistranslation, and it should not be used as a translation by a professional translator. We hold no legal liability for inconsistency of mistranslation, partial omission, and data generated by feature of system and network. We would like to inform you that the document cannot be regenerated, copied, and distributed by being stored in DB and system for unauthorized general public without our consent.)

GF Exhibit 1124 - 1928/2704

(19) 대한민국특허청(KR)
(12) 특허공보(B1)

(51) Int. Cl.[5]
H01L 21/336

(45) 공고일자 1992년11월16일
(11) 공고번호 특1992-0010131

(21) 출원번호	특1988-0016051	(65) 공개번호	특1989-0011074
(22) 출원일자	1988년12월02일	(43) 공개일자	1989년08월12일

(30) 우선권주장 128,742 1987년12월04일 미국(US)

(71) 출원인 아메리칸 텔리폰 앤드 텔레그라프 캄파니 엘리 와이스
미합중국, 뉴욕 10022, 뉴욕, 메디슨 애비뉴 550

(72) 발명자 루이첸 리우
미합중국, 뉴져지 07060, 워렌, 노스릿지 웨이 4
윌리암 토마스 린츠
미합중국, 뉴져지 07901, 써미트, 패싸익 애비뉴 72
데이비드 솔레이트 윌리암스
미합중국, 텍사스 78746, 오스틴, 레이크쇼어 드라이브 2009

(74) 대리인 이병호, 최달용

심사관 : 박형식 (책자공보 제3065호)

(54) 반도체 소자 및 그 제조 방법

요약

내용 없음.

대표도

도1

명세서

[발명의 명칭]

반도체 소자 및 그 제조 방법

[도면의 간단한 설명]

제1도 내지 제8도는 본 발명의 반도체 소자 제조 방법의 실시예 1에 수반된 단계를 도시하는 도면.

제9도 내지 제17도는 본 발명의 반도체 소자 제조 방법의 실시예 2에 수반된 단계를 도시하는 도면.

* 도면의 주요부분에 대한 부호의 설명

10 : P형 실리콘 기판 20 : FOX

30 : GASAD영역 50 : 다결정 실리콘층

100 : 소스 110 : 드레인

230 : 실리콘 이산화물층

[발명의 상세한 설명]

본 발명은 일반적으로 반도체 소자, 즉 반도체 집적 회로 IC)소자 뿐만 아니라 그 결과로된 소자를 제조하는 방법에 관한 것이다.

반도체 집적 회로(IC)는 반도체 기판에 형성된 다수의 전기적으로 상호 접속된 별개의 소자를 포함하는 소자와, 이들 IC중에는 MOS(metal-oxide semiconductor) 및 MES(metal-semiconductor) IC등에 포함한다. MOS IC는 통상적으로 다수의 MOSFET(CMOS 전계효과 트랜지스터)를 포함하는데 이 MOSFET 각각은 반도체 물질, 즉 실리콘의 활성 표면층을 포함한다. 각각의 MOSFET는 또는 활성층의 표면에 형성된 비교적 얇은 게이트 산화물(GOX)과, 예를들어, GOX의 표면상에 형성된 다결정 실리콘(폴리실리콘)의 게이트 전극 및, 상기 게이트 전극의 반대측에 MOSFET의 소스 및 드레인을 구성하는 활성층의 2개의 비교적 두껍게 도핑된 부분을 포함한다. 비교적 두꺼운(GOX와 비교하여) 필드 산화물(FO

GF Exhibit 1124 - 1929/2704

X)이 서로로 부터 MOSFET를 분리하고 전기적으로 절연하도록 작용한다. 유사하게, MES IC도 통상적으로 다수의 MESFET(MES전계효과 트랜지스터)를 포함하는데 MESFET는 MESFET의 게이트 전극이 금속이나 금속함유 혼합물, 즉 금속 실리사이드로 이루어지고 반도체 물질과 직접 접촉하고 있다는 점에서만 MOSFET와 다르다.

현재 상업적으로 유용한 IC에 있어서, 게이트 전극의 길이, 즉 전류 채널의 길이는 통상적으로 약 2마이크로미터(㎛)이며, 소스 및 드레인의 두께는 약 0.5㎛이다. 그러나 증가된 패킹 밀도(별개 소자의)를 가진 IC를 실현하기 위해, 게이트 전극 길이(즉 전류 채널 길이)가 약 1㎛보다 작거나 같게 축소될 것으로 기대된다. 동시에, 통상 짧은 채널 영향으로 불리는 어떤 바람직하지 않은 영향을 피하기 위해, 소스 및 드레인의 두께가 약 0.2㎛보다 작거나 같은 값으로 축소될 것이다(여기서 언급된 바람직하지 않은 짧은 채널 영향은 바람직하지 않은 임계 전압 시프와 소스-드레인 부임계 결핍 전류인데, 이것은 소스/드레인 두께에 대한 채널 길이의 비율이 비교적 작을때 즉, 약 2.5이하일때 발생한다. 짧은-채널 영향에 대해서는 제이.알.브로우스 등의 "MOSFET 소형화에 대한 일반 안내"란 논문을 참조하라).

비교적 얇은 소스 및 드레인, 즉 0.2㎛이하인 두께를 가진 소스 및 드레인은 바람직하지 못하게 큰 저항을 가지는데, 이것은 소자의 성능에 역으로 영향을 미친다. 비교적 얇은 소스 및 드레인을 사용하여 비교적 낮은 소스/드레인 저항을 실현하기 위해, 몰리브데늄 실리사이드($MoSi_2$), 텅스텐 실리사이드(WSi_2)나 티타늄 실리사이드($TiSi_2$)와 같은 금속 실리사이드의 위에 놓인 영역을 포함하도록 각각의 비교적 얇은 소스 및 드레인이 형성되는 것이 제안되었는데 그 목적은 저-저항 전류 분류기로서 작용하도록 한 것이다. 이에 관해 금속 실리사이드 커버된 소스 및 드레인의 효과적인(전기적)두께, 즉 소스-드레인-게이트 상호 작용에 포함되는 두께는 활성층의 표면 아래로 뻗어있으며 그 표면에 비교하여 아래에 놓인(두껍게 도핑된) 소스 및 드레인과 금속 실리사이드 영역의 결합된 두께이다.

금속 실리사이드 커버된 소스 및 드레인을 포함하는 IC를 제조하기 위한 이전의 시도는 소스 및 드레인을 형성하기 위한 통상적인 절차의 이용을 포함하고 있는데, 즉 소스 및 드레인이 필요한 실리콘 기판의 영역으로 소스 및 드레인 도펀트를 주입 및 확산하는 단계와 다음에 밑에 있는 소스 및 드레인의 표면에 Mo, W, Ti와 같은 금속을 증착시키는 단계를 포함하고 있다. 이때 증착된 금속은 대응하는 금속 실리사이드를 형성하도록 소스 및 드레인의 아래에 놓인 실리콘과 반응한다. 이 기술은 소스 및 드레인이 초기에(금속 실리사이드의 형성에 앞서) 실리콘내로 비교적 깊게 연장된 경우, 즉 실리콘내로 약 0.25㎛ 이상 연장된 경우에 효과적인 것으로 입증되었다. 그러나 이 기술은 소스 및 드레인이 초기에 실리콘내로 비교적 작은 거리만을 연장되어 있는 경우, 즉 약 0.25㎛보다 작거나 같은 거리만큼 연장되어 있는 경우에는 바람직하지 못한 것으로 입증되었는데, 이것은 바람직하지 못하게 큰 양의 소스/드레인 실리콘이 금속 실리사이드를 형성하는데 소비되어 결과적으로 소스/드레인 p-n 접합을 통해 연장된 즉 단락 회로시키는 금속 실리사이드 스파이크를 초래하기 때문이다.

금속 실리사이드 커버된 소스 및 드레인을 형성하기 위한 다른 기술이 1983년 IEDM 기술 다이제스트 670 내지 673페이지에 "실리사이드를 통한 측면 확산을 이용한 새로운 저 저항의 얇은 접합 형성 방법"이란 제목으로 에이취.오가바야시 등에 의해 기술되어 있다. 이 기술에 따라, 이와 같은 소스 및 드레인은 초기에 실리콘 기판의 표면상에 예를들어 0.1㎛의 두께를 가진 몰리브데늄 실리사이드($MoSi_2$) 영역을 제조함으로써 형성되는데, 이것은 실리콘 기판상에 몰리브데늄을 증착시키고 아래에 놓인 실리콘과 몰리브에늄을 반응시킴으로써 실현된다. 이때 소스/드레인 도펀트를 몰리브데늄 실리사이드로 확산되어 그곳으로 부터 소스/드레인 p-n 접합을 형성하도록 아래에 놓인 실리콘으로 확산된다. 즉 몰리브데늄 실리사이드 커버된 실리콘 기판이 개스 또는 고체의 도펀트 소스에 접촉되어져 한 단계로 몰리브데늄 실리사이드와 아래에 놓인 실리콘내로 도펀트를 효과적으로 확산시키기 위해 충분히 높은 온도와 충분히 긴 시간 주기동안, 즉 1000℃에서 20분동안 가열된다. 이와 달리 도펀트는 2단계 공정으로 실리콘내로 확산되는데, 제1단계는 초기에 몰리브데늄 실리사이드 커버된 실리콘 기판을 비교적 낮은 온도, 즉 800℃로 가열하여 가스 또는 고체의 도펀트 소스로 부터 몰리브데늄 실리사이드내로(실리콘내로는 확산되지 않음)도펀트를 확산시키는 것이다. 계속해서 도펀트는 실질적으로 보아 높은 온도, 즉 950℃나 1000℃로 기판을 가열함으로써 몰리브데늄 실리사이드로 부터 실리콘내로 확산된다. 1단계 확산 공정을 비교적 깊은 소스 및 드레인을 만드는데, 즉 만일 몰리브데늄 실리사이드가 0.1㎛ 두께이면, 소스 및 드레인은 실리사이드의 상부 표면 아래로 약 1.5㎛ 연장된다. 2단계 확산 공정은 보다 얕은 소스 및 드레인을 만드는데, 이것은 비교적 깊은 것으로서, 만일 몰리브데늄 실리사이드가 0.1㎛ 두께라면, 소스 및 드레인은 실리사이드의 상부 표면아래로 약 0.36㎛ 연장된다.

금속 실리사이드 커버된 소스 및 드레인을 형성하기 위해 이전에 사용된 또다른 기술에 있어서, 텅스텐 실리사이드(WSi_2) 영역이 초기에 실리콘 기판상에 형성되고 텅스텐 실리사이드내로 도펀트가 주입된다(확산이 아님)(1985년 IEDM 기술 다이제스트 407 내지 410페이지에 있는 에프.씨.숀 등의 "도핑된 실리사이드 기술에 의한 0.1㎛ N^+/P와 P^+/N 접합의 형성"을 참조) 이때 주입된 도펀트는 통상적인 용광로 어닐링 기술이나 금속 열 어닐링(RTA)기술을 이용하여 기판을 가열함으로써 텅스텐 실리사이드로 부터 실리콘 기판내로 확산된다(RTA에 대해서는 1983년 전자화학회의 저널 130권의 484페이지에 있는 티.오.세리웍크의 "단시간 어닐링"을 참조) 중요하게도(에프.씨.숀 등에 의해 알려진 바와 같이), 텅스텐 실리사이드 영역의 두께는 0.2㎛이며, 대응하는 주입량과 가열 온도 및 가열 시간은 텅스텐 실리사이드의 특정 두께에 대해 모두(추정적으로)특수하게 맞추어진다. 결과적으로, 상기 특정 기술은 단지 0.3㎛보다 크거나 같은 깊이(텅스텐 실리사이드의 상부 표면으로 부터 측정될때)를 가진 소스 및 드레인만을 만들게된다.

1986년 산 디에고의 VLSI에 관한 1986 심포지엄에서 논문 다이제스트의 "서브-미크론 CMOS에 대한 $TiSi_2$ 및 WSi_2 실리사이드된 낮은 접합의 비교"란 제목으로 엔.고바야시 등에 의해 상기 기술의 변

GF Exhibit 1124 - 1930/2704

형이 기술되어 있다. 여기에서는 텅스텐 실리사이드 또는 티타늄 실리사이드의 0.1㎛ 두께 영역이 초기에 실리콘 기판상에 형성되고, 소스/드레인 도펀트가 실리사이드 내로 주입되어 실리사이드로부터 실리콘내로 확산된다. 그러나 텅스텐 실리사이드의 경우에 엔.고바야시 등의 저널 논문의 제1도에 도시된 바와같이, 이 논문의 저자는 0.2㎛보다 훨씬 큰 깊이(텅스텐 실리사이드의 상부 표면으로 부터 측정할때), 즉 0.26㎛ 및 0.28㎛의 깊이를 가진 소스 및 드레인을 만드는 주입량과 가열 온도 및 가열 시간을 가르쳐주고 있다. 이에 대비하여, 티타늄 실리사이드의 경우에는 제1도에 도시된 바와같이 저자가 0.2㎛보다 작은 깊이(티타늄 실리사이드의 표면으로 부터 측정할때), 즉 0.16㎛의 깊이를 가진 소스나 드레인을 만드는 비소 주입량과 가열 온도 및 가열 시간을 가르쳐 주고 있지 않다. 그러나 제1도로 부터 명백한 바와같이, 티타늄 실리사이드/실리콘 인터페이스에서의 비소의 농도는 비교적 낮다. 이것은(저널 논문의 저자의 주장과는 반대로) 상기 비교적 낮은 인터페이스 농도가 바람직하지 못하게 높은 특정 저항(Rc)을 유도하기 때문에 매우 중요한데, 여기서 Rc는 $10^{-6}\Omega$-Cm^2 보다도 크다. 사실 상기 저널 논문에서 저자는 인터페이스 비소 농도를 증가시키기 위해(추정상 Rc를 낮추기 위한 목적으로) 추가의 비소를 실리콘(티타늄 실리사이드가 아님)대로 주입하는 바람직성을 나타내고 있다. 그러나 불행하게도 알려진 바와같이, 이와 같은 절차는 실리콘 기판이 추가의 도펀트 확산, 결과적으로 비교적 깊은 소스 및 드레인을 만드는 실리콘내로의 생성 주입 손상을 어닐링하기 위해 비교적 높은 온도로 가열되어야만 하기 때문에 바람직하지 못하다.

그러므로 IC제조 방법의 개발에 종사하는 사람들은 약 $10^{-6}\Omega$-cm^2 이하의 Rc를 나타내는 금속 실리사이드를 포함하는 비교적 얕은 소스 및 드레인을 가진 IC를 제조하기 위한 방법을 추구해왔다.

본 발명은 금속 함유 물질 영역, 즉 기초 금속이나 금속 실리사이드와 같은 금속 함유 혼합물을 함유하는 영역으로 커버된 소스나 드레인을 형성하기 위한 새로운 기술을 포함한다. 중요하게도 이 새로운 기술은 약 0.2㎛이하의 깊이(물질 영역의 상부 표면과 비교하여)를 갖고 약 $10^{-6}\Omega$-cm^2 이하의 Rc를 나타내는 물질 영역 커버된 소스나 드레인을 만든다.

본 발명의 기술에 따라, 0.2㎛이하의 평균 두께 t를 가진 금속 함유 물질 영역이 초기에 반도체 기판의 표면상에 형성된다. 그 다음에, 하나 혹은 그 이상의 도펀트가 상기 영역에 주입되고, 반도체 기판이 가열되어 상기 도펀트가 상기 영역으로 부터 기판내로 확산되게 된다. 약 $10^{-6}\Omega$-cm^2 이하의 Rc를 발생하기 위해, 가열 절차는 상기 물질 영역/기판 인터페이스에 인접한 기판에서 최소한 하나의 도펀트를 집중시켜야 하는데, 이것은 기판 가열전의 인터페이스에서의 쇼트키 전위 장벽의 높이에 의해 결정되는 최소 값보다 크거나 같다. 상기 최소값을 실현하기 위해 다음 3조건이 만족되어야 한다고 알려져 있다. 제1조건은 가열 절차 동안에 사용된 온도에서 기판내의 최소한 하나의 도펀트의 고체 용해도가 상기 최소값보다 크거나 같아야 한다는 것이다. 제2조건은 상기 동일한 도펀트에 있어서, 상기 물질 영역의 평균 두께에 대한 대응하는 주입량의 비율이 상기 가열 온도에서 상기 물질 영역내의 상기 도펀트의 고체 용해도의 약 1/2보다 크거나 같아야 된다는 것이다.(이것에 대해서, 예를들어, 엔.고바야시 등에 의해 사용된 비소 주입량이 상기 제2임계 요구조건을 만족하지 못한다고 결정되었다). 원하는 인터페이스 농도를 실현하고 유용한 소스/드레인 접합을 실현하기 위해 만족되어야할 제3조건은, 상기 동일한 도펀트에 대해 상기 물질 영역내로 주입되는 도펀트 이온의 총수효가 아래에 놓인 확산된 소스 및 드레인을 형성하는데 필요한 수보다 실질적으로 커야된다는 것이다. 만일 상기 물질 영역/기판 인터페이스에 가까이 인접한 기판에서의 도펀트의 농도의 필요한 최소값이 Co로 표시되고 상기 물질 영역의 바닥과 비교하여 소스/드레인 접합의 원하는 깊이가 X로 표시되면 제3조건은 자동적으로 $1 \geq g5Co \cdot X/2$가 만족된다. 실예로 제2조건을 만족하는 주입량은 또한 제3조건도 만족한다. 그러나 주입량의 제2조건을 만족하지만 5Co·X/2 보다 작은 경우에 제3조건은 Co·X/2보다 크거나 같은 양만큼 상기 주입량을 증가시킴으로써 확실하게 만족되게 된다.

본 발명의 기술은 또한 원하는 깊이를 가진 소스 및 드레인을 만드는데 필요한 가열 온도-시간 프로필을 선택하기 위한 절차(후술됨)를 포함한다.

본 발명은 MOS나 MES 반도체 IC와 같은 반도체 소자뿐 아니라 그 합성 소자를 제조하기 위한 방법을 모두 포함하고 있다. 본 발명의 방법에 따라 제조된 소자는 금속 함유 물질 영역, 즉 텅스텐(W)과 같은 기초 금속을 함유하는 영역으로 커버된 최소한 하나의 소스나 드레인을 포함하고 있다. 이와 달리 금속 함유 물질 영역은 금속 실리사이드, 즉 코발트 실리사이드($CoSi_2$), 티타늄 실리사이드($TiSi_2$), 텅스텐 실리사이드(WSi_2), 몰리브데늄 실리사이드($MoSi_2$), 탄탈륨 실리사이드($TaSi_2$)나 플라티늄 실리사이드(ptSi)와 같은 금속 함유 혼합물을 포함한다. 또한 상기 물질 영역의 상부 표면에 비교하여 상기 물질 영역으로 커버된 소스나 드레인의 깊이는 약 0.2㎛ 보다 작거나 같다. (본 발명의 목적을 위해 상기 물질 영역 커버된 소스나 드레인의 깊이는 상기 물질 영역의 상부 표면에 대한 최소 면적 평면 근사부로 부터 소스나 드레인이 형성되는 반도체 기판과 소스나 드레인 사이의 인터페이스의 최저점까지 직각으로 연장된 길이다. 만일 예를들어 소스나 드레인이 n형 전도성이면 인터페이스는 소스나 드레인에서의 n형 도펀트의 농도가 기판에서의 p형 도펀트의 농도가 같은 (그 역도 마찬가지임) 점들이 궤적이다. 이와 같은 인터페이스는 2차 이온 질량 분광학(secondary ion mass spectroscopg : SIMS)과 같은 종래의 기술을 이용하여 쉽게 위치된다.) 또한 아래에 놓인(확산된) 소스나 드레인에 대한 상기 물질 영역의 특정 접촉 저항, Rc는 약 $10^{-6}\Omega \cdot cm^2$ 보다 작거나 같다.(Rc는 IEEE전자 소자란 책의 544페이지에 있는 케이.케이.에지, "MOSFET의 접촉 저항을 측정하기 위한 새로운 기술" 에 기술된 종래의 절차를 이용하여 쉽게 측정된다.)

본 발명의 방법에 따라, 상기 물질 영역 커버된 소스나 드레인이 초기에 실리콘이나 갈륨 비소와 같은 반도체 물질을 포함하는 기판상에 상기 물질 영역을 형성함으로써 형성된다. 이와 같은 물질 영역은 예를들어, 종래 기술, 즉 종래의 스퍼터링(sputtering)기술을 이용하여, 기판상에 상기 영역을 구성하는 물질을 침착시킴으로써 형성된다. 이와 달리, 만일 상기 물질 영역이 예를들어 금속 실리사이드를 포함하고 기판이 실리콘으로 되어 있으면, 상기 물질 영역은 대응하는 기초 금속을 실리콘 기판상에 침착시키고 금속 실리사이드를 형성하기 위해 침착된 금속을 아래에 있는 실리콘과 반응시

GF Exhibit 1124 - 1931/2704

킴으로써 최소한 부분적으로 쉽게 형성된다. 약 0.2㎛보다 작거나 같은 깊이를 가진 상기 물질 영역 커버된 소스나 드레인을 실형하기 위해서는 상기 물질 영역의 최대 두께, 즉 결과적으로 평균 두께 (일반적으로 균일하지 않은 두께임)가 0.2㎛보다 작아야 된다. 또한 (균일하지 않은 두께의) 상기 물질 영역의 최소 두께는 약 0.1㎛보다 크거나 같은 것이 양호하다. 약 0.1㎛보다 작은 최소 두께는 바람직하지 못한데 이것은 다른 이유중에서, 상기 물질 영역의 대응하는 부분이 종종, 주입 단계동안에 매우 많은 양의 도펀트를 상기 물질 영역이 아닌 기판내로 주입되도록 허용하는 매우 많은 수의 핀구멍을 포함하게 되기 때문이다.

상기 물질 영역을 형성한 후에, 하나 혹은 그 이상의 도펀트가 상기 물질 영역내로 주입되고, 계속해서 원하는 소스나 드레인을 형성하기 위해 상기 물질 영역으로 부터 상기 기판내로 주입된 도펀트가 확산되도록 기판이 가열된다. 만일 기판 반도체 물질이 p형 전도성이면, 주입된 도펀트는 기판에서 전자도우너를 형성해야 하며, 만일 기판 반도체 물질이 n형 전도성이면 상기 도펀트는 전자 액셉터를 형성해야 한다. 예를들어 실리콘의 경우에, 유용한 도오너 이온은 인(p)과 비소(As)이온을 포함하며, 동시에 유용한 액셉터 이온은 붕소(B)이온을 포함한다.

전술한 바와같이, 약 $10^{-6}\Omega \cdot cm^2$보다 작거나 같은 Rc를 실현하기 위해, 기판 가열 절차는 상기 물질 영역/기판 인터페이스에 인접한 기판에서의 최소한 하나의 도펀트의 농도를 산출해야 되는데 이것은 기판 가열 이전의 상기 물질 영역/기판 인터페이스에서의 쇼트키 전위 장벽의 높이에 의해 결정되는 최소값보다 크거나 같다. 즉, 상기 전위 장벽 높이를 아는 것은 대응하는 최소값을 의미하고 있다. 이점에 있어서, 금속 함유 물질과 반도체 물질 사이의 인터페이스에서의 쇼트키 전위 장벽 높이는 원하는 Rc를 발생시키기 위해 인터페이스 도펀트 농도의 대응하는 최소값이 필요한 바와같이 문헌상 쉽게 이용할 수 있다. 예를들어, n형이나 p형 실리콘과 다양한 기초 금속 사이의 인터페이스에서의 쇼트키 전위 장벽 높이는 에스.엠.스제의 "반도체 소자의 물리학" 제2판(1981) 292페이지에서 찾아볼 수 있다. 비슷하게 예를들어 n형 또는 p형 실리콘과 다양한 기초 금속 사이의 인터페이스 사이의 쇼트키 전위 장벽 높이는 에스.피.유라카의 "VLSI 응용을 실라이드"(1983) 15페이지에서 찾아볼 수 있다.

또한 거의 모든 쇼트키 전위 장벽 높이에 대응하는 약 $10^{-6}\Omega \cdot cm^2$보다 작거나 같은 Rc를 발생시키는데 필요한 최소 인터페이스 도펀트 농도는 에스.엠.스제의 상기 참조 논문의 304 내지 305페이지에서 찾아볼 수 있다. 예를들어 만일 상기 물질 영역이 코발트 실리사이드($CoSi_2$)를 포함하고 기판이 p형 실리콘을 포함하며 주입된 n형 도펀트중 하나가 비소(As)라면, 에스.피.유라카의 상기 참조 온도에 따라, 대응하는 쇼트키 전위 장벽 높이는 0.64볼트이며, 에스.엠.스제의 상기 참조는 논문에 따라 비소의 대응하는 최소 인터페이스 농도는 약 $1\times10^{20}cm^{-3}$이다. 비슷하게, 만일 상기 물질 영역이 티타늄 실리사이드($TiSi_2$)를 포함하고 기판이 n형 실리콘을 포함하며 주입된 p형 도펀트중 하나가 붕소(B)라면, 에스.피.유라카의 상기 논문에 따라 대응하는 쇼트키 전위 장벽 높이는 0.5볼트이고 에스.엠.스제의 상기 논문에 따라 붕소의 대응하는 최소 인터페이스 농도는 약 $3\times10^{19}cm^{-3}$이다.

또한 전술한 바와같이, 약 $10^{-6}\Omega \cdot cm^2$보다 작거나 같은 Rc를 발생시키기 위해 필요한 상기 물질 영역/기판 인터페이스에 인접한 기판에서의 도펀트 농도를 실현하기 위해서는 3가지 조건이 만족되어야 한다고 알려져 있다. 제1조건은 기판 가열 절차동안에 사용된 온도에서 최소한 하나의 도펀트의 기판에서의 고체 용해도가 전술한 최소 인터페이스 농도보다 크거나 같아야 된다는 것이다. 중요하게도, 반도체에서 도펀트의 고체 용해도는 일반적으로 매우 민감하며 온도에 따라 증가한다. 결과적으로 제1조건은 사실 기판 가열 절차동안에 사용될 수도 있는 온도에 대한 최소값 Tmin을 강요한다. 즉, 최소한 하나의 도펀트의 기판에서의 고체 용해도가 원하는 Rc를 실현하는데 필요한, 상기 물질 영역/기판 인터페이스에 인접한 기판에서의 최소 도펀트 농도의 최소한 같게 되는 것을 보장하기 위해 가열 온도는 Tmin보다 크거나 같아야 된다. 이점에 있어서, 온도 함수로서의 다양한 반도체 물질에서의 다양한 도펀트의 고체 용해도는 문헌에서 이용 가능하다.(즉 에서 엠.스제에 의해 출판된 "VLSI 기술에서의 제이.씨.씨.츠아이" 198 내지 199페이지를 참조하라).

결과적으로 제1조건을 만족하는데 필요한 Tmin은 쉽게 결정된다. 예를들어, 740℃, 800℃ 및 900℃에서, 실리콘에서의 비소의 고체 용해도는 각각 $1\times10^{20}cm^{-3}$, $1.5\times10^{20}cm^{-3}$, $2\times10^{20}cm^{-2}$이다. (상기 논문 제이.씨.씨.츠아이를 참조). 만일 비소가 n형 실리콘에서 n형 도펀트로서 사용되고 상기 물질 영역이 $CoSi_2$로 이루어져 있으면, 전술한 바와같이 원하는 Rc를 실현하는데 필요한 최소 인터페이스 농도는 $1\times10^{20}cm^{-3}$이며, 결과적으로 Tmin은 740℃이다. 유사하게, 800℃ 및 900℃에서 실리콘에서의 붕소의 고체 용해도는 각각 $3\times10^{19}cm^{-3}$ 및 $6\times10^{19}cm^{-3}$이다. 만일 붕소가 n형 실리콘에서 p형 도펀트로서 사용되고 상기 물질 영역이 $TiSi_2$라면, 전술한 바와 같이 원하는 Rc를 실현하는데 필요한 최소 인터페이스 농도는 $3\times10^{19}cm^{-3}$이며, 결과적으로 Tmin은 800℃이다.

만족되어야 할 제2조건은 위에서 언급된 최소한 하나의 도펀트에 대해 상기 물질 영역의 두께 t에 대한 대응하는 주입량의 비율, 즉 I/t가 기판 가열동안에 사용된 온도(필수적으로 대응하는 보다 크거나 같은)에서 상기 물질 영역에서의 상기 도펀트의 고체 용해도의 1/2보다 크거나 같아야 되며, 바람직하게는 더 커야된다는 것이다. 여기서 논의되는 고체 용해도는 기판 가열 절차 동안에 사용된 온도에서, 상기 물질 영역과 기판 사이의 인터페이스를 포함하여 상기 물질 영역에서의 최소한 하나의 도펀트의 포화 레벨을 말한다. 중요하게도, 이 포화 레벨은 온도에 민감하며, 일반적으로 온도에 따라 증가한다. 또한 이 포화 레벨은 상기 물질 영역의 합성 성분과 상기 물질 영역의 결정성의 정도에 의존한다(즉, 예를들어 다결정 물질의 경우에, 도펀트는 종종 그레인(grain) 및 그레인 경계내에 분배된다). 또한 상기 포화 레벨은 상기 물질 영역/기판 인터페이스의 특성에 의존하는데, 즉 도펀트가 상기 인터페이스에서 비교적 높게 농축되는지의 여부에 의존한다.

일반적으로, 기판 가열 절차동안에 사용된 온도에서, (상기 물질 영역/기판 인터페이스를 포함하여)

GF Exhibit 1124 - 1932/2704

상기 물질 영역내의 도펀트의 고체 용해도는 실험적으로 결정된다. 즉, 본 발명에 따라, 소자에 사용된 상기 물질 영역과 동일한 평균 두께를 가진 상기 물질 영역의 제어 샘플이(소자에 사용된 기판과 동일한 합성 성분 및 구조를 가진)반도체 기판상에(소자의 제조에 사용된 바와 동일한 기술을 이용하여)형성된다. (중요하게도, 이하에서 더욱 자세히 설명되는 바와같이, 제어 샘플의 상부 표면의 영역 A는 상기 물질 영역의 그것과 동일하게 되는 것을 필요로 하지 않는다. 제어 샘플을 지탱하는 기판은 비워진 용광로, 즉 주위 압력이 예를들어 10^{-6} 토르(torr)의 값으로 낮아지는 용광로에 배치된다. 이때 관심있는 도펀트를 포함하는 가스가 용광로내로 흘러들어간다. 예를들어, 만일 인이라면 유용한 인 함유 가스는 PH_3이다. 유사하게, 만일 도펀트가 비소라면, 유용한 비소 함유 가스는 AsH_3이며, 만일 도펀트가 붕소라면 유용한 붕소 함유 가스는 B_2H_6이다(PH_3, AsH_3 및 B_2H_6는 매우 유독성 가스이므로 적당한 안전 예방책이 사용되어야 한다는 것을 주목하자). 이점에 있어서, 도펀트 함유 가스의 유동률은 상기 가스의 부분 압력이 주위 압력의 최소한 백배가 되도록 충분히 높아야 되는데, 만일 주의 가스 압력이 10^{-6} 토르이면 도펀트 함유 가스의 부분 압력은 최소한 10^{-4} 토르가 되어야 한다. 이 필요성은 제어 샘플이 필수적으로 주위의 오염물질이 아닌 도펀트에 의해서만 (다음 단계 동안에)포화되는 것을 보장하기 위한 것이다. 도펀트 함유 가스가 용광로내로 흐르는 동안, 용광로는 관련있는 온도, 즉 기판 가열동안에 사용될 온도로 가열되게 된다. 제어 샘플내에서 도펀트 포화를 실현하기 위해서는 이 온도가 최소한 1분동안 유지되어야 하는데, 최소한 30분동안 유지되는 것이 바람직하다.

도펀트 함유 가스에 영향을 받은 후에 제어 샘플은 용광로로 부터 이동되며 제어 샘플/기판 인터페이스를 포함하며 제어 샘플내의 도펀트 원자의 총 수 N이 예를들어 종래의 SIMS 기술을 이용하여 측정된다. 상기 물질 영역에서 도펀트의 고체 용해도는 바로 N/At이다. (원자의 총 수 N는 표면 영역 A에 선형적으로 비례한다는 것을 주목하자.) 결과적으로, 표면 영역은 다르지만, 동일한 평균 두께를 가진 제어 샘플은 동일한 값의 고체 용해도를 산출하게 된다). 결과적으로 제2조건을 만족하기 위해서는 $I/t \geq g0.5N/At$가 되도록 I가 선택되어야 한다.

전술한 실험적 절차를 이용하여, 예를들어 만일 상기 물질 영역이 코발트 실리사이드로 이루어지고, 0.07㎛의 평균 두께를 가지며, 실리콘 기판위에 놓여 있고, 도펀트가 비소라면, $5\times10^{15}cm^{-2}$ 이상의 주입량이 800℃의 온도에서 제2조건을 만족한다. 비슷하게, 상기 물질 영역이 티타늄 실리사이드로 이루어져 있고 0.08㎛의 평균 두께를 가지며 실리콘 기판위에 놓여있고, 도펀트가 붕소라면, $1\times10^{16}cm^{-2}$ 이상의 주입량의 800℃의 온도에서 제2조건을 만족한다.

원하는 Rc를 실현하고 유용한 소스/드레인 접합(즉 예를들어 0.5볼트의 전압과 25℃의 온도에서 반전 전류에 대한 진행 전류의 비율이 10^6보다 크거나 같아지는 접합)을 실현하기 위해 만족되어져야 하는 제3조건은, 최소한 하나의 도펀트에 대해, 상기 물질 영역내로 주입된 도펀트 이온의 총수가 아래에 놓인, 확산된 소스나 드레인을 형성하는데 필요한 수보다 실질적으로 커야된다는 것이다. 만일 상기 물질 영역/기판 인터페이스에 인접한 상기 기판에의 도펀트 농도의 최소값이 Co로 표시되고 상기 물질 영역의 바닥과 비교하여 소스/드레인 P-N접합의 원하는 깊이가 X로 표시되면, 제3조건은 자동적으로 $1 \geq 5Co \cdot X/2$이 만족되도록 제공된다. 그러나 만일 주입량이 제2조건을 만족하지만 $5Co \cdot X/2$보다 작다면, 제3조건은 보다 크거나 같은 양만큼 상기 주입량을 증가시킴으로써 확실하게 만족되게 된다. 이점에 있어서, 위에서 주어진 두 주입량은 또한 제3조건도 만족한다.

상기 금속 함유 물질 영역내로 주입된 이온의 에너지는 근본적으로 모든 이온, 즉, 이온의 최소한 90퍼센트가 상기 영역내로 주입되는 기초적인 반도체 기판내로는 주입되지 않도록 선택된다는 것을 주목하자. 이점에 있어서, 또한 실리콘의 본 발명에 사용된 금속 함유 물질 영역보다 밀도가 높지 않고, 그러므로 동일한 에너지를 가진 동일한 이온이 상기 물질 영역보다 더 큰 깊이로 실리콘내로 관통된다는 것을 주목하자. 결과적으로, 거의 모든 이온이 상기 물질 영역내로 주입되는 것을 보장하기 위해, 이온 에너지는 상기 물질 영역의 두께이하의 실리콘내로의 대응하는 관통 깊이를 산출하도록 선택된다.(이온 에너지의 함수로서의 실리콘내로의 이온 관통 깊이는 알.에이.콜콜레이저의 "마이크로 전자공학처리 및 소자 설계" 150 내지 153페이지에서 찾아볼 수 있다.)

예를 들어, 60keV 이하의 주입 에너지(0.07㎛보다 작거나 같은 깊이로 실리콘을 관통하는 비스 이온의 90퍼센트가 되는 비소 이온 에너지)를 이용하여 0.07㎛의 평균 두께를 가진 코발트 실리사이드의 영역내로의 비소 이온의 주입은 거의 모든 비소 이온이 코발트 실리사이드내로 주입되는 것을 보장한다. 유사하게, 10keV 이하의 주입 에너지(0.08㎛ 이하의 깊이로 실리콘을 관통하는 붕소 이온의 90퍼센트가 되는 붕소 이온 에너지)를 이용하여, 0.08㎛의 평균 둑께를 가진 티타늄 실리사이드의 영역내로 붕소 이온을 주입하면 거의 모든 붕소 이온의 티타늄 실리사이드로 주입되는 것을 보장한다.

본 발명은 또한 원하는 소스/드레인 깊이를 실현하기 위해 기판 가열 동안에 이용될 온도-시간 프로필을 선택하기 위한 반복적(iterative) 기술을 포함하고 있다. 여기서, 상기 물질 영역이 두게는 기판의 도핑 레벨, NA 일대 공지되거나 지정된 것을 가정 한다. 또한 상기 세가지 조건이
만족되었고, 기판 가열의 결과로서 상기 물질 영역/기판 인터페이스에 인접한 기판내의 도펀트 농도가 원하는 Rc를 실현하는데 필요한 (공지된) 최소값인 Co보다 크거나 같은 것으로 가정한다.
처음에, 또한 간편성을 위해, 필수적으로 Tmin보다 크거나 같은 온도 T만이 가열 절차 동안에 사용된다고 가정한다. 만일 변수 X′가 상기 물질 영역의 바닥에 대한(확산된) 소스나 드레인내의 점의 수직 위치를 표시하고, T가 시간을 나타내고, D(=D(T))가 기판에서의 도펀트의 확산 계수를 표시하고, Co′가 약 $10^{-6}\Omega-cm^2$ 이하의 Rc를 산출하는 상기 물질 영역/기판 인터페이스에 인접한 원하는 도펀트 농도를 나타낸다면, C가 공식

GF Exhibit 1124 - 1933/2704

$$C(X', \gamma) = Co' \cdot erfc(X'/2\sqrt{D\Gamma}) \quad \cdots\cdots (1)$$

에 의해 잘 근사된다는 것이 결정되었다. 여기서 erfc는 상보 에러 함수이다. X′가 X(상기 물질 영역의 바닥에 비교한 소스나 드레인의 원하는 깊이)와 같아지는 소스나 드레인의 바닥에서, C(X, Γ)는 필수적으로 NA와 동일하며, 그러므로 공식(1)로 부터,

$$erfc(X/2\sqrt{D\Gamma}) = NA/Co' \quad \cdots\cdots (2)$$

이다.

공식(2)의 오른쪽이 공지된 양이기 때문에, 공식(2)에서 상보 에러 함수의 독립변수(argument)가 알려지며, 즉 예를 들어 erfc 함수의 테이블로 부터 쉽게 결정된다(엠.아브라모위쯔와 아이.에디.세건에 의해 출판된 "수학적 함수의 핸드북"에서 윌터 고쯔찌를 참조하라). 그러나 X는 알려져 있다. 또한 D는 필수적으로 온도의 함수이며, 단일 온도만이 가열 절차동안에 사용되기 때문에 D도 또한 낮게되며, 단일 온도T에 대응하는 D의 값은 예를 들어, 테이블(제이.씨.씨.쯔아이의 상기 참조 논문을 참조)로 부터 쉽게 결정된다. 그러므로, erfc 함수의 독립 변수의 값이 알려지고, X와 D의 값이 알려졌기 때문에 Γ(가열시간)의 값은 쉽게 추론할 수 있다. 만일(제어 샘플의 바닥과 비교하여) 소스나 드레인의 생성 깊이가(예를 들어 SIMS 기술을 통해 결정될때) 원하는 깊이가 아니면 가열시간 및 가열온도가 변경된다.

만일 대응하는 다수의 시간 간격 Γ_1, $\Gamma_2 \cdots \Gamma_n$에 대해 다수의 가열온도 T_1, $T_2 \cdots T_n$을 사용하는 것이 필요하다면, C는

$$C(X', T_1, T_2 \cdots T_n) = Co' erfc(X'/2\sqrt{D_1(T_1)T_1 + D_2(T_2)T_2 + \cdots D_n(T_n)T_n}) \quad \cdots\cdots (3)$$

의해 잘 근사된다. 여기서 D_1, D_2, $\cdots D_n$는 온도 T_1, T_2, $\cdots T_n$에서 기판내의 도펀트의 확산 계수를 표시한다. 그러므로, C가 NA와 동일한, 즉 X′=X인 소스나 드레인의 바닥에서,

$$erfc(X/2\sqrt{D_1T_1 + D_2T_2 + \cdots (D_nT_n)} = NA/Co' \quad \cdots\cdots (4)$$

이된다. 전술한 바와 같이, 공식(4)의 오른쪽은 알려져 있고, 그러므로 공식(4)에서 erfc 함수의 독립변수는 쉽게 결정된다. 또한 X는 알려져 있고, T_1, T_2, $\cdots T_n$가 지정된 것으로 가정하면 D_1, D_2, $\cdots D_n$도 또한 쉽게 결정된다. 그러므로 공식(4)를 만족하는 Γ_1, Γ_2, $\cdots \Gamma_n$의 값이 쉽게 선택된다. 만일 Γ가 원하는 소스/드레인 깊이를 산출하지 못하면, 반복적 절차에 따라, Γ 및 T가 변경된다.

상기 반복적 기술을 이용하여, $1 \times 10^{16} cm^{-3}$의 도핑레벨을 가진 P형 실리콘 기판을 가열하는 단계와 800℃의 온도로 130분 동안 상기 비소가 주입된 코발트 실리사이드 영역을 지탱하는 단계는 0.15㎛와 동일한 깊이(코발트 실리사이드의 상부 표면에 대하여)를 가진 소스나 드레인을 산출한다는 것이 알려졌다. 유사하게, $1 \times 10^{17} cm^{-3}$의 도핑 레벨을 가진 n형 실리콘 기판을 가열하는 단계와 124분 동안 800℃의 온도로 상기 붕소가 주입된 티타늄 실리사이드 영역을 지탱하는 단계는 0.2㎛와 동일한 깊이(티타늄 실리사이드의 상부 표면에 대하여)를 가진 소스나 드레인을 산출한다는 것도 알려져 있다.

본 발명의 보다 완전한 이해를 위한 교육학적 도움으로서 n채널 MOS IC 및 CMOS(상보 금속 산화물 반도체) IC의 제조를 위한 본 발명의 소자 제조 방법의 용융이 이하에서 기술되게 된다(간략하게 하기 위해 완전히 통상적인 몇몇 단계는 생략된다).

제1도 내지 제8도를 참조하면, 예를 들어 종래의 산화 기술을 이용하여, P형 실리콘 기판(10)상에 FOX(20)(비교적 두꺼운 SiO_2층)을 형성함으로써 본 발명의 한 실시예에 따라 n채널 MOS IC가 제조된다. 기판(10)에서 P형 도펀트의 도핑 레벨은 예를 들어 $1 \times 10^{15} cm^{-3}$이다. 또한 FOX(20)의 두께는 예를 들어 0.35㎛이다.

이제 FOX(20)는 MOSFET가 형성될, 여기서는 GASAD(gate-and-source-and-drain)으로 불리는 기판 표면의 영역(30)을 노출시키기 위해 예를 들어, 석판 인쇄술 및 반응 이온 에칭(RIE)기술을 이용하여 선택적으로 에칭된다. 예를 들어, 0.15㎛의 두께를 가진 GOX(40)(비교적 얇은 SiO_2층)는 예를 들어 종래의 산화 기술을 이용하여 GASAD 영역(30)의 표면상에 형성된다.

MOSFET의 게이트 전극은 GASAD 영역(30) 뿐만 아니라 FOX(20)상에도 다결정 실리콘(이후 폴리실리콘)의 층(50)을 초기에 침착시킴으로써 형성된다. 침착은 예를 들어 종래의 저압 화학적 증기 침착(LPCVD) 기술을 이용하여 실행되며, 침착된 폴리실리콘의 두께는 예를 들어 0.3㎛가 된다.

GF Exhibit 1124 - 1934/2704

침착후에, 폴리실리콘은 예를 들어 $1\times10^{15}cm^{-2}$의 주입량(implant dose)과 80kev의 이온 에너지를 이용하여, 폴리실리콘에 비소와 같은 n형 도펀트를 주입함으로써 전기적 전도성으로 만들어진다.

침착된 전기적 전도성의 폴리실리콘(50)은 이제 제4도에 도시된 바와 같이, 간각이 GASAD 영역(30) 위에 있는 폴리실리콘 구조를 형성하기 위해 종래의 RIE 기술을 이용하여 패턴된다. 상기 구조의 측벽은 대응하는 GASAD 영역이 표면에 직각인 면에 비하여 각도 α(제4도 참조)를 형성하는데, 이것은 +15° 보다 작거나 같으며, 0도가 되는것이 바람직하다(제4도에 도시한 폴리실리콘 구조의 좌측벽에 대해, 각도 X는 수직으로 부터 시계 방향으로 측정될때 포지티브가 된다. 한편 우측벽에 대해서는 이 각도가 반시계 방향으로 측정될때 포지티브다 된다). 측벽 각도에 관한 관계는 이하에서 논의되는 바와 같이 실리콘 이산화물 측벽 스페이서(55)의 형성과 관련하여 매우 중요하다.

이하에서 논의되는 소자 제조 절차는 결과적으로 금속 실리사이드 영역을 각각의 MOSFET의 소스, 드레인 및 게이트 전극으로 병합시킨다. 게이트 전극에서의 금속실리사이드 영역과 소스 및 드레인에서의 금속 실리사이드 영역 사이의 전기적 접촉을 배제하기 위해, 각 게이트 전극의 폴리실리콘 부분은 각 폴리실리콘 측벽을 커버링하는 실리콘 이산화물 측벽 스페이서(55)(제4도 참조)를 포함하도록 형성된다. 이것은 예를 들어 FOX의 상부 및 측벽 표면과 GASAD 영역의 노출된 표면상에 뿐만 아니라 폴리실리콘 구조의 상부 및 측벽 표면상에 테트라에틸오소실리케이트(TEOS)와 같은 실리콘과 산소 함유 물질의 층을 침착 시킴으로써 실현된다. TEOS의 침착은 예를 들어 종래의 LPCVD 기술을 이용하여 쉽게 실행되며, TEOS의 두께는 예를 들어 0.1㎛이다. 침착이 이루어진 후에, TEOS는 TEOS를 농후하게 하고 효과적으로 실리콘 이산화물과 같은 물질로 변환시키기 위해 스팀 대기에서 20분 동안 900℃로 가열되는 것이 바람직하다. 이때 TEOS는 폴리실리콘 구조의 상부 표면 뿐만 아니라 FOX 및 GASAD 표면으로 부터 TEOS를 제거하기 위해 예를 들어 CHF_3 및 O_2의 에천트(etchant) 환경에서 예를 들어 RIE를 이용하여 이동방향으로 에칭된다. 이 에칭 절차 이후에, 예를 들어 0.06㎛의 두께를 가진 농후하게 된 TEOS의 층이 측벽 각도가 전술한 요구를 만족하도록 제공되어 폴리실리콘 구조의 측벽상에 남아 있게 된다.

측벽 스페이서(55)의 형성 이후에, 티타늄과 같은 금속 실리사이드를 형성하기 위해 실리콘과 반응할 수 있는 금속층이 각 폴리실리콘 구조의 상부 표면과, 측벽 스페이서(55)의 표면과, GASAD 영역의 노출된 표면(소스와 드레인 형성될 곳) 및 FOX(20)의 상부 및 측벽 표면상에 침착된다. 이 침착은 예를 들어, 종래의 스퍼터링 기술을 이용하여 실현되며, 침착된 티타늄의 두께는 예를 들어, 0.1㎛이다. 침착 이후에, 티타늄으로 커버된 실리콘 기판은 종래의 RTA 기술을 이용하여 약 1분동안 약 600℃의 온도로 질소(N_2) 환경에서 가열된다. 티타늄 층이 실리콘과 접촉하는 곳, 즉 GASAD 영역의 표면 뿐만 아니라 폴리실리콘 구조의 상부 표면상에서, 이 가열 절차는 TiN, Ti 및 Tisiy의 연속한 층의 형성을 초래하게 되는데, 여기서 y≤2이다. 대조적으로, 침착된 티타늄 층이 실리콘 이산화물과 접촉하는 곳, 즉 FOX 및 측벽 스페이서의 표면에서, 상기 가열절차는 TiN 및 Ti의 연속한 층의 형성을 야기하게 된다.

TiSiy(y≤2)가 아닌 TiN 및 Ti층은 90℃의 온도로 가열된 H_2SO_4 : H_2O_2(1 : 1)의 용액과 같은 선택적 습식 에천트를 사용하여 에칭된다. 폴리실리콘 구조의 상부 표면과 GASAD 영역의 노출된 표면을 커버링하는 남아있는 TiSiy(y≤2)는 이제 종래의 RTA 기술을 이용하여 예를 들어 20초동안 800℃의 온도로 질소 환경에서 TiSiy로 커버된 실리콘 기판을 가열함으로써(폴리실리콘 구조 및 실리콘 기판에서) 아래에 있는 실리콘과 반응하게 된다. 그 결과 $TiSi_2$ 함유 영역(60, 70)(제5도 참조)이 폴리실리콘 주조의 반대측에 형성되어 수직으로 정렬되고 $TiSi_2$ 함유 영역(80)은 폴리실리콘 구조의 정상부에 형성되는데, 이와 같은 영역은 약 0.08㎛의 동일한 $TiSi_2$의 두께를 갖는다(각각의 이와 같은 영역은 또한 통상적으로 약 0.01㎛의 두께를 갖고 $TiSi_2$ 위에 있는 TiN층(양호한 전기적 전도체)을 포함한다).

n^+형 소스 및 드레인을 형성하기 위해, 하나 혹은 그 이상의 도펀트, 즉 비소 이온이나 인 이온이 $TiSi_2$ 함유 영역(60, 70)내로 주입된다. 주입량은 물론 전술한 세가지 조건을 만족하도록 선택된다. 또한 이온 에너지도 거의 모든 이온이 영역(60, 70)내로 주입되고 아래에 놓인 실리콘내로는 주입되지 않도록 선택된다.

이온 주입 이후에, 인터레벨 유전체(90)(제6도 참조)가 기판상에 침착된다. 이와 같은 유용한 인터레벨 유전체는 예를 들어, 0.2㎛의 두께를 가진 도핑되지 않은 TEOS와 약 0.8㎛의 두께를 가진 인으로 도핑된 TEOS의 잇따른 층을 포함한다.

침착된 인터레벨 유전체(9)의 상부 표면은 통상적으로 비평면이다(일반적으로 후속 처리동안 바람직하지 못하다). 인터레벨 유전체(90)를 흐르도록 유도하고 그래서 표면 평면성을 실현하고 또한 티타늄 실리사이드로 커버된 소스 및 드레인(100, 110)(제7도 참조)을 형성하도록 $TiSi_2$ 함유 영역(60, 70)으로 부터 아래에 놓인 실리콘내로 주입 도펀트를 확산시키기 위해, 기판이 가열된다. 전술한 바와 같이, 가열 절차의 온도-시간 프로필은 약 0.2㎛ 이하의 깊이를 가진 소스 및 드레인을 산출하도록 선택된다.

소스 및 드레인 형성 이후에, 인터레벨 유전체는 소스와 드레인 및 게이트 전극으로 경유 구멍을 개방하도록(종래 기술을 이용하여) 패턴된다. 이제 물질층(120, 130, 140)(제8도 참조)이 기판상에 침착되는데 그래서, 알루미늄과 실리콘의(바람직하지 못한) 상호 확산에 대한 장벽으로서 작동하도록 소스와 드레인 및 게이트 전극으로 각각 뻗은 경유 구멍내로 침착되게 된다. 이들 층은 예를 들어, 10퍼센트(중량으로)의 티타늄과 90퍼센트의 텅스텐 합성물을 포함하며 예를 들어 0.1㎛의 두께를 갖는다.

이제, 예를 들어 1㎛의 두께를 가진 알루미늄 층이 경유 구멍내의 장벽층(120, 130, 140) 뿐만 아니라 인터레벨 유전체(90)상에도 침착된다. 침착후 계속해서, 금속 접촉 패드에서 중단되는 상호 접속

GF Exhibit 1124 - 1935/2704

알루미늄 런너(runner)(150, 160, 170)를 형성하기 위해 종래의 기술을 이용하여 알루미늄층이 패턴된다.

n채널 MOS IC는 통상적인 일련의 단계를 통해 완성되는데, 통상적으로 습기 및 기계적 손상에 대비한 장벽을 형성하기 위해 IC상에 실리콘 질화물 층을 침착하는 단계를 포함한다.

이제 제9도 내지 제17도를 참조하면, 종래기술을 이용하여 P+형 실리콘 기판(200)상에 P형 실리콘층(210)(제9도 참조)을 에피택셜 성장시킴으로써 본 발명의 제2실시예에 따라 CMOS IC가 제조된다. 기판(200)의 도핑 레벨은 예를 들어 $10^{18}cm^{-3}$ 이며, 에피택셜 성장된 층(210)의 도핑 레벨은 예를 들어 $10^{15}cm^{-2}$이다. 또한, 에피택셜 성장된 층(210)의 두께는 예를 들어 5㎛이다.

1984년 3월 13일 엘.씨.파릴로와 알.에스.페인에게 특허된 미합중국 제 4,435,896호에 기술된 바와 같은 소위 2중 튜브 공정을 이용하여 에피택셜 성장층(210)에 인접한 n튜브 및 P튜브(240, 250)가 형성된다. 즉 예를 들어 0.1㎛의 두께를 가진 실리콘 질화물층(220)(제10도 참조)이 통상적인 침착 기술을 이용하여 상기 층(210)의 상부 표면에 처음에 침착된다. 종래의 석판 인쇄술 및 RIE 기술이 실리콘 질화물층(220)의 일부분을 제거하고, 그러므로 n튜브(240)가 될 실리콘 표면을 노출시키는데 이용된다. 이제 도우너 이온, 즉 인 이온과 비소 이온이 상기 층(210)(층(210)의 노출되지 않는 실리콘을 주입으로 부터 차폐하도록 작용하는 잔여 실리콘 질화물층)의 노출된 실리콘 표면내로 주입되는데, 인과 비소 이온 모두에 대한 주입량 및 에너지는 예를 들어 각각 $2\times10^{12}cm^{-2}$와 100keV이다. 다음에, n튜브의 표면상에 약 0.4㎛의 두께를 가진 실리콘 이산화물의 층(230)(제10도 참조)을 형성하기 위해, 예를 들어 950℃의 온도로 140분의 대응하는 가열 시간동안 스팀 함유 환경에서 실리콘 기판이 가열된다.

이제 실리콘 질화물의 층(220)이 뜨거운 H_3Po_4와 같은 습식 에천트로 에칭되고, 액셉터 이온 즉 붕소 이온이 P튜브(250)가 될 노출된 실리콘 표면으로 주입된다(실리콘 이산화물층(230)은 n튜브(240)을 주입으로 부터 차폐한다). 만일 붕소 이온이 사용되면, 주입량 및 대응하는 주입 에너지는 예를 들어 각각 $2\times10^{12}cm^{-2}$ 및 50keV이다. 다음에, 실리콘 기판은 붕소 이온 및 인 이온을 약 2㎛의 깊이까지 상기 층(210)내로 확산시켜 n튜브(240) 및 p튜브(250)(제11도 참조) 모두를 형성시키기 위해, 예를 들어 1150℃의 온도로 120분의 대응하는 시간 주기동안 질소(N_2) 환경에서 가열된다.

n튜브(240)를 커버링하는 실리콘 이산화물층(230)은 H_2O : HF(7 : 1)와 같은 습식 에천트로 에칭된다. 이제 CMOS IC에서 FOX로서 작용하는 예를 들어 0.4㎛의 두께를 가진 실리콘 이산화물의 비교적 두꺼운 층(260)(제12도 참조)이 에피택셜 성장층(210)의 (이제 완전히 노출된) 상부 표면상에 형성된다. 이것을 예를 들어 850℃의 온도로 25분의 대응하는 가열 시간동은 고압스팀 함유 대기, 즉 25기압의 압력을 나타내는 스팀 함유 대기에서 실리콘 기판을 가열함으로써 실현된다.

실리콘 이산화물의 비교적 두꺼운 층(260)은, n채널 MOSFET가 형성된 P튜브(250)과 표면상의 GASAD 영역(270)을 노출시키고, P채널 MOSFET가 형성될 n튜브(240)의 표면상의 GASAD 영역(400)을 노출시키기 위해 종래의 기술을 이용하여 패턴된다. 다음에, 실리콘 기판은 GASAD 영역(270)의 표면상에 실리콘 이산화물의 층(280)을 형성하고 GASAD 영역(400)의 표면상에 실리콘 이산화물의 층(410)을 형성하기 위해 900℃의 온도로 27분의 대응하는 시간 주기동안 가열되게 되는데, 이들 층(280, 410)은 약 0.0125㎛의 두께를 가지며, n채널 및 P채널 MOSFET의 GOX로서 작용한다.

n채널 및 P채널 MOSFET의 게이트 전극은 처음에, FOX(260) 뿐만 아니라 GASAD 영역(270, 400)상에 예를 들어 0.3㎛의 두께를 가진 폴리실리콘 층을 침착시킴으로써 형성되며, 포토레지스트가 기판상에 침착되어 n튜브(240)에 대응하는 기판 표면을 노출시키기 위해 패턴된다. 이제 액셉터 이온, 즉 붕소 이온이 n튜브 위에 놓인 폴리실리콘내로 주입되는데 레지스트는 P튜브 위에 놓인 폴리실리콘을 주입으로 부터 차폐한다. 주입량 및 주입 에너지는 예를 들어, 각각 $1\times10^{15}cm^{-2}$와 30keV이다. 이 레지스트는 벗겨지고, 제2레지스트가 기판상에 침착되어 P튜브(250)에 대응하는 기판 표면을 노출시키기 위해 패턴된다. 이제 도우너 이온, 즉 비소 이온이 P튜브(250)위에 놓인 폴리실리콘내로 주입되는데, 제2레지스트는 n튜브(240) 위에 놓인 폴리실리콘을 제2주입으로 부터 차폐한다. 도우너 이온에 대응하는 주입량 및 주입 에너지는 예를 들어, 각각 $1\times10^{15}cm^{-2}$와 30keV이다. 이제 제2레지스트는 벗겨지고, 기판은, 예를 들어 900℃의 온도로 30분의 대응하는 시간 주기동안 질소(N_2) 디기에서 가열된다. 결과적으로, 주입된 도펀트가 폴리실리콘내로 확산되어, n튜브(240)위에 놓인 폴리실리콘은 P형 전도성이 되고, P튜브(250)위에 놓인 폴리실리콘은 n형 전도성이 된다.

이제, 침착되고 주입된 폴리실리콘(도한 아래에 놓인 비교적 얇은 실리콘 이산화물층(280, 410)로 마찬가지)이 각각 GASAD 영역(270, 400)위에 놓인 폴리실리콘 구조(290, 420)(제13도 참조)를 형성하기 위해 전술한 바와 같이 패턴된다. 이 폴리실리콘 구조의 측벽은 위에서 논의된 요구에 부합해야 한다. 또한 전술한 바와 같이 실리콘 이산화물 측벽 스페이서(295, 425)가 각각 폴리실리콘 구조(290, 420)상에 형성된다.

이제 코발트와 같이 금속 실리사이드를 형성 하기 위해 실리콘과 반응할 수 있는 금속층이 폴리실리콘구조(290, 410)의 상부 표면과, 측벽 스페이서(295, 425)의 표면과, GASAD 영역의 노출된 표면(소스와 드레인의 형성될 곳)과, FOX(260)의 상부 및 측벽 표면상에 침착된다. 침착된 코발트의 두께는 예를 들어 0.02㎛이다. 침착 이후에, 코발드로 커버된 기판은 450℃의 온도로 90분의 대응하는 시간 주기동안, 감소대기, 즉 대기에서 가열된다. 코발트가 실리콘과 접촉하는 곳, 즉 GASAD 영역과 노출된 표면뿐만 아니라 폴리실리콘 구조의 상부 표면상에서, 이 가열 절차는 코발트 모노실리사이드(CoSi)를 형성하게 된다. 모든 다른 영역에 있어서, 코발트는 반응하지 않은채로 남아 있다. 반응하지 않은 코발트(CoSi가 아님)는 이제 H_3Po_4 : CH_2COOH : HNO_3 : H_2O(16 : 2 : 1 : 1)과 같은 선택적 습식 에천트를 사용하여 벗겨진다. 다음에, 기판은 예를 들어 700℃의 온도로 30분의 대응하는 시간 주기동안 불활성 대기, 즉 아르곤(Ar) 대기에서 두번째 가열된다. 이 제2가열은 약 0.07㎛의 두께를

GF Exhibit 1124 - 1936/2704

가진 코발트 다이실리사이드($CoSi_2$)를 형성하기 위해 CoSi를 아래에 놓인 실리콘과 반응하도록 한다. 그러므로, $CoSi_2$ 함유 영역(300, 310)(제14도 참조)이 각각의 폴리실리콘구조(290)와 수직으로 정렬하여 반대측에 형성되고, 함유 영역(320)이 각각의 폴리실리콘구조(290)의 정상부에 형성된다. 유사하게, $CoSi_2$ 함유 영역(430, 440)이 각각의 폴리실리콘 구조(420)와 수직으로 정렬하여 반대측에 형성되고, $CoSi_2$ 함유 영역(450)이 각각의 폴리실리콘 구조(420)의 정상부에 형성된다.

n튜브(240)에서 P채널 MOSFET에 대한 P^+형 소스 및 드레인을 형성하기 위해, 예를 들어 1㎛의 두께를 가진 포토레지스트가 기판상에 침착되어, n튜브의 표면을 노출시키도록 패턴된다. 이제 액셉터 이온이 $CoSi_2$ 함유 영역(430, 440)내로 주입된다(이 레지스트는 P튜브(250)를 주입으로 부터 차폐한다). 전술한 바와 같이, 주입량은 3가지 조건을 만족하도록 선택되며, 이온 에너지는 거의 모든 이온이 상기 영역(430, 440)내로 주입되도록 선택된다. 이점에 있어서, 액셉터 이온은 예를 들어 붕소 이온이며, 유용한 주입량은 $8\times10^{15}cm^{-2}$ 이고 유용한 대응하는 주입 에너지는 10keV인 것으로 결정되었다.

침착되어 패턴된 포토레지스트는 벗겨지고, 약 1㎛의 두께를 가진 다른 포토레지스트가 기판상에 침착되고, 이번에는 P튜브(250)의 표면을 노출시키기 위해 패턴된다. 이제, 도우너 이온이 $CoSi_2$ 함유 영역(300, 310)내로 주입된다(세로 침착된 레지스트는 n튜브(240)를 제2주입으로 부터 차폐한다). 다시, 주입량 및 이온 에너지는 상기 조건과 요구를 만족하도록 선택된다. 이점에 있어서, 만일 도우너 이온이 예를 들어 비소 이온이면, 유용한 주이량은 $5\times10^{15}cm^{-2}$ 이고 유용한 대응하는 이온 에너지는 60keV 보다 작거나 같다. 한편, 만일 도우너 이온이 인 이온이면, 유용한 주입량은 $5\times10^{25}cm^{-2}$이고, 유용한, 대응하는 주입 에너지는 30keV 이하의 에너지이다.

이온 주입 이후에, 예를 들어, 0.2㎛ 두께의 도핑 되지 않은 TEOS층과 0.2㎛두께의 인 도핑된 TEOS층의 연속한 층을 포함하는 인터레벨 유전체(600)(제15도 참조)가 기판상에 침착된다. 인터레벨 유전체(600)는 흐르도록 유도되고, 주입된 도펀트는 $CoSi_2$로 커버된 n^+형 소스 및 드레인(330, 340)(제16도 참조)과, $CoSi_2$로 커버된 P^+형 소스 및 드레인(460, 470)을 기판 가열에 의해 형성하기 위해 $CoSi_2$ 함유 영역으로 부터 아래에 놓인 실리콘으로 확산된다. 이점에 있어서, 약 0.2㎛보다 작거나 같은 깊이를 가진 소스 및 드레인을 실현하기 위해, 유용한 가열 절차가 800℃의 온도로 120분동안 기판을 가열하는 것이라는 것이 결정되었다.

COMOS IC의 제조와 관련하여, 금속 실리사이드 영역으로 부터 기판내로 주입된 도펀트를 확산하는데 사용되는 가열 온도를 선택할때 만족되어야 할 추가의 요구 조건이 있다는 것을 주목하자. 즉 예를 들어 종래의 용광로 가열을 이용할때, 약 900℃를 초과하는 온도에서, n형 폴리실리콘 구조(420)내의 n형 도펀트가 P형 폴리실리콘구조(290)(통상적으로 n형 폴리실리콘 주조(420)와 접속 되어 있음)로 확산되어 그것을 카운터 도핑하려는 경향이 있는 것으로 알려져 있다. 이와 같은 카운터 도핑은 그것이 P채널 MOSFET에서 바람직하지 못한 임계 전압 시프트를 유도하기 때문에 바람직하지 못하다. 결과적으로, 본 발명의 실시예 2에 따라, CMOS IC를 제조하기 위해 용광로 가열을 이용할때 사용된 가열 온도는 900℃보다 낮으며, 850℃ 이하의 것이 바람직하다.

소스와 드레인을 형성한 후에, 인터레벨 유전체(600)가 소스와 드레인 및 게이트 전극으로 경유 구멍을 개방하기 위해 패턴된다. 알루미늄과 실리콘, 즉 층(350, 360과 370(제17도 참조), 480, 490과 500)의 상호 확산에 대한 장벽이 경유 구멍으로 침착된다. 소스와 드레인 및 게이트 전극으로 부터 금속 접촉 패드로 연장된 상호 접속 알루미늄 런너(375, 385, 395와 505, 515, 525)(제17도 참조)가 전술한 바와 같이 형성된다.

CMOS IC는 습기 및 기계적 손상에 대비한 장벽을 형성하기 위해 IC상에 실리콘 질화물층을 침착시키는 단계를 포함하는 통상적인 일련의 단계를 통해 완성된다.

(57) 청구의 범위

청구항 1

기초적인 반도체 물질을 포함하는 기판상(10)에 금속 함유 물질 영역(60)을 형성하는 단계와, 상기 금속 함유 물질 영역내에 도펀트를 주입시키는데, 상기 도펀트는 상기 기초적인 반도체 물질이 P-형 전도성으로 되어 있으면 상기 기초적인 반도체 물질내에서 도우너가 되나 상기 기초적인 반도체 물질이 n-형 전도성으로 되어 있으면 액셉터가 되는 최소한 하나의 도펀트를 상기 금속 함유 물질 영역내에 주입시키는 단계와, 상기 금속 함유 물질 영역에서 상기 기판내로 상기 도펀트를 확산시키도록 상기 기판을 가열하며, 그로써 상기 기판내에 도펀트 함유 영역(100)을 형성하는 단계와, 반도체 소자 제조를 완료시키는 단계를 포함하는 반도체 소자 제조 방법에 있어서, 상기 금속 함유 물질 영역은 0.2㎛ 이하의 평균 두께 t를 가지며, 상기 가열 온도 및 시간은 상기 도펀트 함유 영역의 깊이가 상기 금속 함유 물질 영역의 정상부로부터 측정할때 약 0.2㎛ 이하가 되도록 선정되며, 상기 금속 함유 물질 영역 I내로 주입된 단위면적당 도펀트의 양은 t에 대한 I의 비율이 상기 가열동안에 사용된 온도에서 상기 금속 함유 물질 영역내의 상기 도펀트의 고체 용해도의 약 1/2 이상이 되도록 선정되는 것을 특징으로 하는 반도체 소자 제조 방법.

청구항 2

제1항에 있어서, 상기 금속 함유 혼합물은 금속 실리사이드인 것을 특징으로 하는 반도체 소자 제조 방법.

GF Exhibit 1124 - 1937/2704

청구항 3

제2항에 있어서, 상기 금속 실리사이드는 코발트 실리사이드인 것을 특징으로 하는 반도체 소자 제조 방법.

청구항 4

제1항에 있어서, 상기 반도체 물질은 실리콘을 포함하는 것을 특징으로 하는 반도체 소자 제조 방법.

청구항 5

표면, 반도체 물질 및 상기 표면으로 부터 기판내로 연장되고 상기 표면보다 작은 측면 넓이를 가지며, 주위 반도체 물질의 전도성과 반대인 전도성을 가진 기판 영역을 포함하는 기판(10)과, 상기 표면과 접촉하고 상기 기판 영역 위에 놓인 금속 함유 물질 영역(60)을 구비하는 반도체 소자에 있어서, 상기 기판 영역의 깊이는 상기 금속 함유 물질 영역의 정상부로 부터 측정할때 약 0.2㎛ 이하이고, 상기 기판에 대한 상기 금속 함유 물질 영역의 특정 접촉 저항은 약 $10^{-6}\Omega \cdot cm^2$ 이하인 것을 특징으로 하는 반도체 소자.

청구항 6

제5항에 있어서, 상기 반도체 소자는 MOSFET를 포함하고, 상기 금속 함유 물질 영역과 상기 기판 영역은 상기 MOSFET의 소스나 드레인을 형성하는 것을 특징으로 하는 반도체 소자.

청구항 7

제5항에 있어서, 상기 반도체 소자는 MESFET를 포함하고, 상기 금속 함유 물질 영역과 상기 기판 영역은 상기 MESFET의 소스나 드레인을 형성하는 것을 특징으로 하는 반도체 소자.

청구항 8

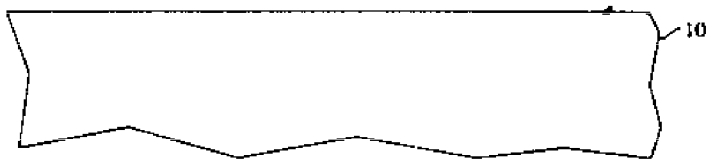
제5항에 있어서, 상기 금속 함유 혼합물은 금속 실리사이드인 것을 특징으로 하는 반도체 소자.

청구항 9

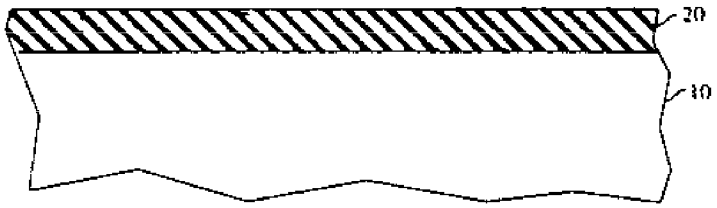
제8항에 있어서, 상기 금속 실리사이드는 코발트 실리사이드인 것을 특징으로 하는 반도체 소자.

도면

도면1

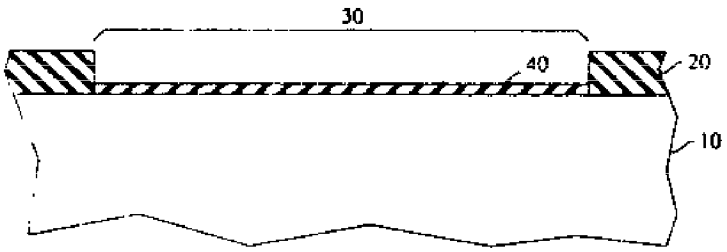


도면2

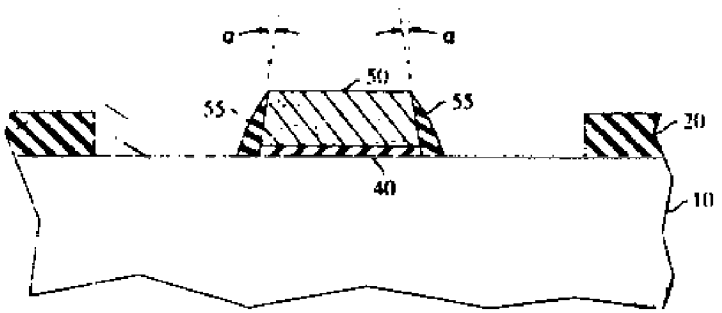


GF Exhibit 1124 - 1938/2704

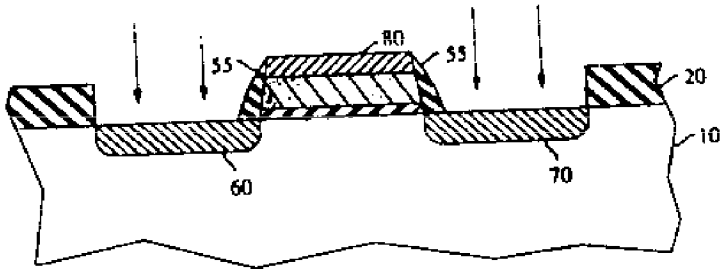
도면3



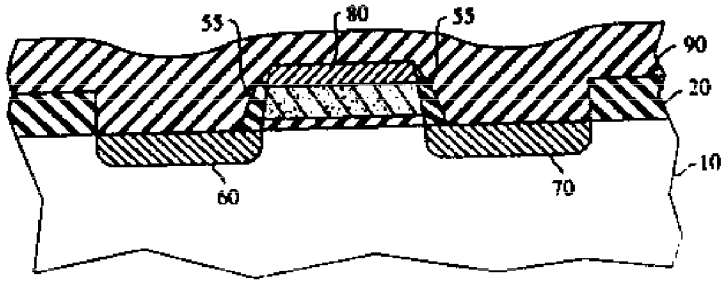
도면4



도면5

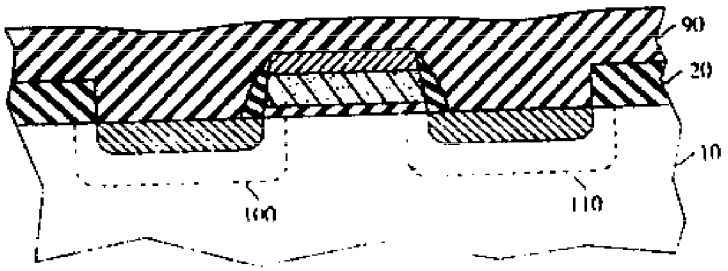


도면6

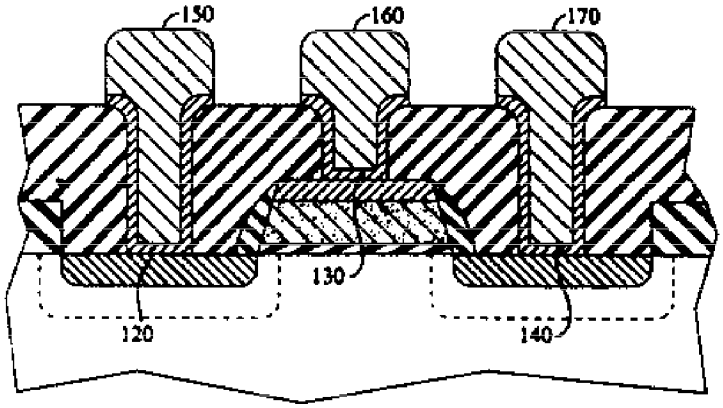


GF Exhibit 1124 - 1939/2704

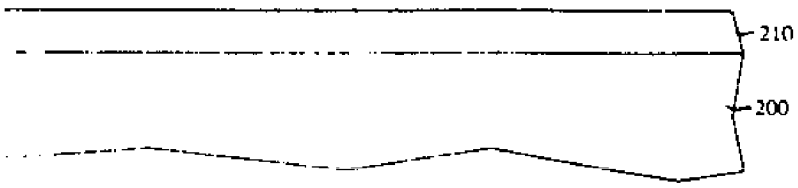
도면7



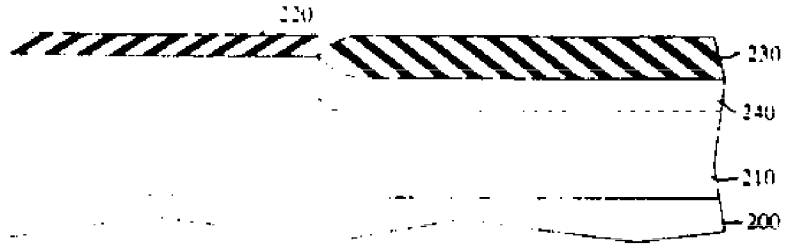
도면8



도면9

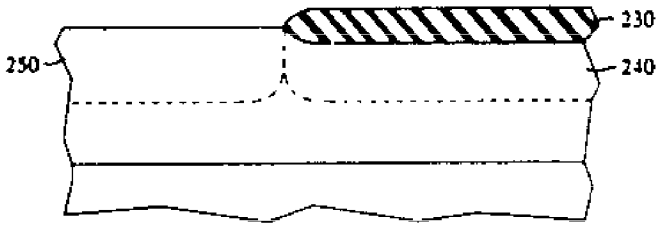


도면10

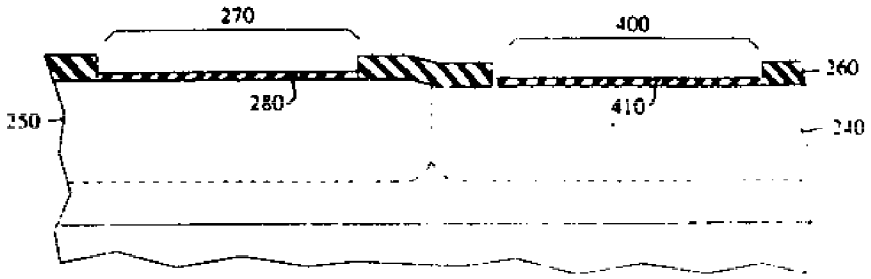


GF Exhibit 1124 - 1940/2704

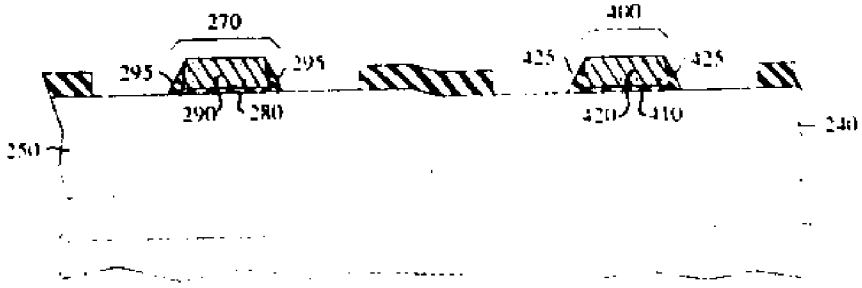
도면11



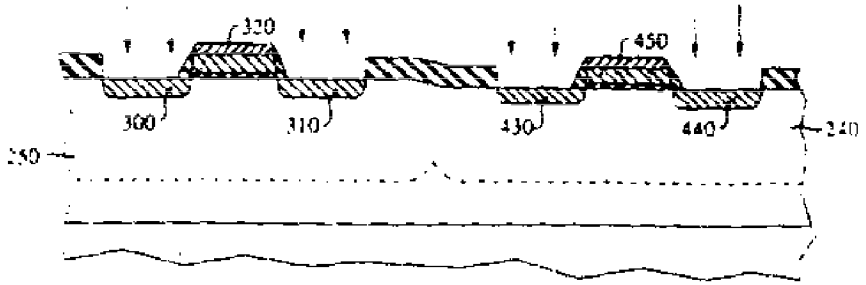
도면12



도면13

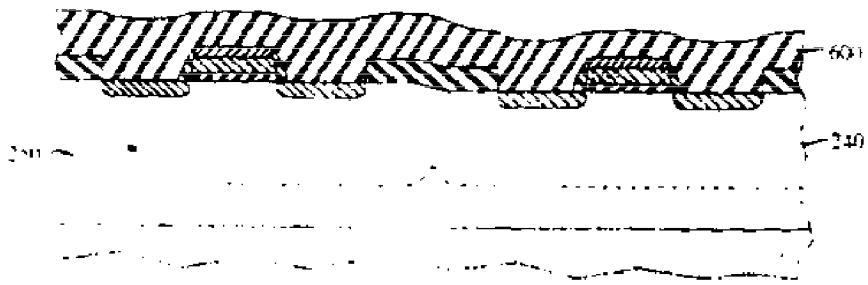


도면14

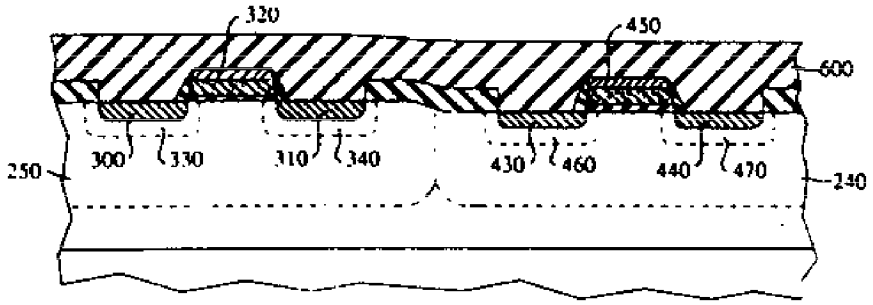


GF Exhibit 1124 - 1941/2704

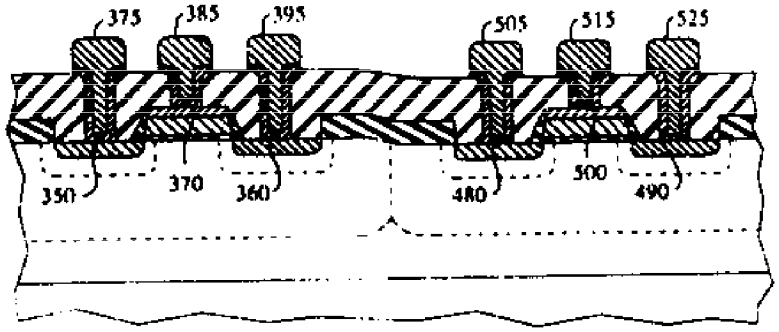
도면15



도면16



도면17



GF Exhibit 1124 - 1942/2704

Bibliographic Data

Int.Cl.	H01L 21/8238 | H01L 21/225 | H01L 27/092 | H01L 29/66
Published Date	19921116
Registration No.	1000607090000
Registration Date	19930323
Application No.	1019880016051
Application Date	19881202
Unexamined Publication No.	1019890011074
Unexamined Publication Date	19890812
Priority Claims	128,742 | 19871204 | US
Requested Date of Examination	19890202
Agent.	LEE, Byong Ho | CHOI, Dall Ryong
Inventor	RuUChenRiU | WilRiAmToMaSeuRinCheu | DeIBiDeuSeulReITeuWilRiAmSeu
Applicant	AT&T Corp.
Rightholder	AMeRiKanTelRiPonAenDeuTelReGeuRaPeuKamPaNi

발명의 명칭

반도체소자및그제조방법

Title of Invention

MANUFACTURING METHOD AND THERE DEVICES OF SEMICONDUCTOR ELEMENTS

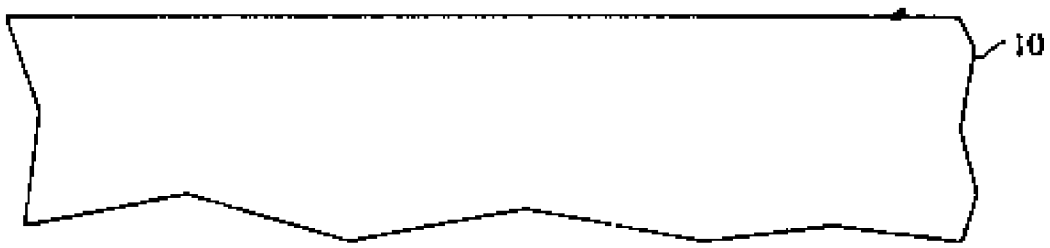
요약

내용 없음.

Abstract

Content none.

대표도면(Representative drawing)



청구의 범위

Scope of Claims

GF Exhibit 1124 - 1943/2704

청구 1항:

기초적인 반도체 물질을 포함하는 기판상(10)에 금속 함유 물질 영역(60)을 형성하는 단계와, 상기 금속 함유 물질 영역내에 도펀트를 주입시키는데, 상기 도펀트는 상기 기초적인 반도체 물질이 P-형 전도성으로 되어 있으면 상기 기초적인 반도체 물질내에서 도우너가 되나 상기 기초적인 반도체 물질이 n-형 전도성으로 되어 있으면 액셉터가 되는 최소한 하나의 도펀트를 상기 금속 함유 물질 영역내에 주입시키는 단계와, 상기 금속 함유 물질 영역에서 상기 기판내로 상기 도펀트를 확산시키도록 상기 기판을 가열하며, 그로써 상기 기판내에 도펀트 함유 영역(100)을 형성하는 단계와, 반도체 소자 제조를 완료시키는 단계를 포함하는 반도체 소자 제조 방법에 있어서, 상기 금속 함유 물질 영역은 0.2㎛ 이하의 평균 두께 t를 가지며, 상기 가열 온도 및 시간은 상기 도펀트 함유 영역의 깊이가 상기 금속 함유 물질 영역의 정상부로부터 측정할때 약 0.2㎛ 이하가 되도록 선정되며, 상기 금속 함유 물질 영역 I내로 주입된 단위 면적당 도펀트의 양은 t에 대한 I의 비율이 상기 가열동안에 사용된 온도에서 상기 금속 함유 물질 영역내의 상기 도펀트의 고체 용해도의 약 1/2 이상이 되도록 선정되는 것을 특징으로 하는 반도체 소자 제조 방법.

Claim 1:

The dopant is injected within the step of forming the metal containing material domain (60) on the substrate phase (10) including the fundamental semiconductor material, and the metal containing material domain ; the substrate is heated up in order to diffuse the dopant in the step of injecting the dopant of at least one in which the acceptor is within the metal containing material domain if the donor is in the above-mentioned fundamental semiconductor material if in the dopant, the above-mentioned fundamental semiconductor material is to the P- type conductivity but the above-mentioned fundamental semiconductor material is to the n-type conductivity, and the metal containing material domain within the substrate ; the metal containing material domain has the average thickness t less than 0.2㎛ as to the semiconductor device fabricating method including the step of forming the dopant containing domain (100) as that within the substrate, and the step of completing the semiconductor device fabrication ; and it is chosen so that in the heating temperature and time, about 0.2㎛ this are when the depth of the dopant containing domain measures from the top of the metal containing material domain. The semiconductor device fabricating method in which amount of the dopant per the unit area injected within the metal containing material domain I is chosen in the temperature in which the rate of I about the t is used for for heating in order to become over about 1/2 of the solid solubility of the dopant within the metal containing material domain.

청구 2항:

제1항에 있어서, 상기 금속 함유 혼합물은 금속 실리사이드인 것을 특징으로 하는 반도체 소자 제조 방법.

Claim 2:

As for claim 1, the semiconductor device fabricating method in which the metal containing mixture is the metal silicide.

청구 3항:

제2항에 있어서, 상기 금속 실리사이드는 코발트 실리사이드인 것을 특징으로 하는 반도체 소자 제조 방법.

Claim 3:

As for claim 2, the semiconductor device fabricating method in which the metal silicide is the cobalt silicide.

청구 4항:

제1항에 있어서, 상기 반도체 물질은 실리콘을 포함하는 것을 특징으로 하는 반도체 소자 제조 방법.

Claim 4:

The semiconductor device fabricating method of claim 1, wherein the above semiconductor material comprises the silicone.

청구 5항:

표면, 반도체 물질 및 상기 표면으로 부터 기판내로 연장되고 상기 표면보다 작은 측면 넓이를 가지며, 주위 반도체 물질의 전도성과 반대인 전도성을 가진 기판 영역을 포함하는 기판(10)과, 상기 표면과 접촉하고 상기 기판 영역 위에 놓인 금속 함유 물질 영역(60)을 구비하는 반도체 소자에 있어서, 상기 기판 영역의 깊이는 상기 금속 함유 물질 영역의 정상부로 부터 측정할때 약 0.2㎛ 이하이고, 상기 기판에 대한 상기 금속 함유 물질 영역의 특정 접촉 저항은 약 10-6Ω#183#cm2 이하인 것을 특징으로 하는 반도체 소자.

Claim 5:

The semiconductor device in which it is about 0.2㎛ or less as to the semiconductor device equipped with the metal containing material domain (60) contacting with the substrate (10) and contacts with the surface and is puts on the substrate region when the depth of the substrate region measures from the top of the metal containing material domain ; and the specific constant resistance of the metal containing material domain about the substrate is about 10 - 6 Ω· cm 2 or less which comprise the surface, the semiconductor material, and the substrate region which is extended from the surface within the substrate and it has the side width smaller than the surface ; and has the conductivity which is conduc

GF Exhibit 1124 - 1944/2704

tivity and opposite of the surrounding semiconductor material.

청구 6항:

제5항에 있어서, 상기 반도체 소자는 MOSFET를 포함하고, 상기 금속 함유 물질 영역과 상기 기판 영역은 상기 MOSFET의 소스나 드레인을 형성하는 것을 특징으로 하는 반도체 소자.

Claim 6:

The semiconductor device of claim 5, wherein the semiconductor device comprises MOSFET, and the metal containing material domain and substrate region forms the source or the drain of MOSFET.

청구 7항:

제5항에 있어서, 상기 반도체 소자는 MESFET를 포함하고, 상기 금속 함유 물질 영역과 상기 기판 영역은 상기 MESFET의 소스나 드레인을 형성하는 것을 특징으로 하는 반도체 소자.

Claim 7:

The semiconductor device of claim 5, wherein the semiconductor device comprises MESFET, and the metal containing material domain and substrate region forms the source or the drain of MESFET.

청구 8항:

제5항에 있어서, 상기 금속 함유 혼합물은 금속 실리사이드인 것을 특징으로 하는 반도체 소자.

Claim 8:

As for claim 5, the semiconductor device in which the metal containing mixture is the metal silicide.

청구 9항:

제8항에 있어서, 상기 금속 실리사이드는 코발트 실리사이드인 것을 특징으로 하는 반도체 소자.

Claim 9:

As for claim 8, the semiconductor device in which the metal silicide is the cobalt silicide.

상세설명

Detailed Description

[발명의 명칭]

반도체 소자 및 그 제조 방법

[Title of invention]

Semiconductor device and method for manufacturing the same.

[도면의 간단한 설명]

제1도 내지 제8도는 본 발명의 반도체 소자 제조 방법의 실시예 1에 수반된 단계를 도시하는 도면.

제9도 내지 제17도는 본 발명의 반도체 소자 제조 방법의 실시예 2에 수반된 단계를 도시하는 도면.

[Brief description of drawings]

Drawing in which the first the inland eighth drawing shows the step accompanied with the embodiment 1 of the semiconductor device fabricating method of the invention.

Drawing in which the ninth the inland seventeenth drawing shows the step accompanied with the embodiment 2 of the semiconductor device fabricating method of the invention.

* 도면의 주요부분에 대한 부호의 설명

10 : P형 실리콘 기판 20 : FOX

30 : GASAD영역 50 : 다결정 실리콘층

100 : 소스 110 : 드레인

230 : 실리콘 이산화물층

* The description of reference numerals showing the main elements in drawings.

10: p-sub 20: FOX.

30: GASAD domain 50: polycrystalline silicon layer.

100: source 110: drain.

230: silicon dioxide layer.

[발명의 상세한 설명]

본 발명은 일반적으로 반도체 소자, 즉 반도체 집적 회로 IC)소

[Detailed description of the invention]

The invention generally relates to the method for

GF Exhibit 1124 - 1945/2704

자 뿐만 아니라 그 결과로된 소자를 제조하는 방법에 관한 것이다.

manufacturing the device which becomes with the semiconductor device, in other words, not only the semiconductor IC(integrated circuit) IC) device but also the result furnace.

반도체 집적 회로(IC)는 반도체 기판에 형성된 다수의 전기적으로 상호 접속된 별개의 소자를 포함하는 소자와, 이들 IC중에는 MOS(metal-oxide semiconductor) 및 MES(metal-semiconductor) IC등에 포함한다. MOS IC는 통상적으로 다수의 MOSFET(CMOS 전계효과 트랜지스터)를 포함하는데 이 MOSFET 각각은 반도체 물질, 즉 실리콘의 활성 표면층을 포함한다. 각각의 MOSFET는 또는 활성층의 표면에 형성된 비교적 얇은 게이트 산화물(GOX)과, 예를들어, GOX의 표면상에 형성된 다결정 실리콘(폴리실리콘)의 게이트 전극 및, 상기 게이트 전극의 반대측에 MOSFET의 소스 및 드레인을 구성하는 활성층의 2개의 비교적 두껍게 도핑된 부분을 포함한다. 비교적 두꺼운(GOX와 비교하여) 필드 산화물(FOX)이 서로로 부터 MOSFET를 분리하고 전기적으로 절연하도록 작용한다. 유사하게, MES IC도 통상적으로 다수의 MESFET(MES전계효과 트랜지스터)를 포함하는데 MESFET는 MESFET의 게이트 전극이 금속이나 금속함유 혼합물, 즉 금속 실리사이드로 이루어지고 반도체 물질과 직접 접촉하고 있다는 접에서만 MOSFET와 다르다.

It includes the MOS (metal-oxide semiconductor) and MES (metal-semiconductor) IC etc. among the device, in which the semiconductor IC(integrated circuit) (IC) includes lots of the separate device which is formed in the semiconductor substrate and the electrically is interconnected and these ICs. The generally the MOS IC includes multiple MOSFETs (CMOS field effect transistor) but this MOSFET includes semiconductor material, and in other words, the active surface layer of the silicone. Each MOSFET comprises the gate oxide (GOX) which or is formed on the surface of the active layer and is relatively thin, the source of MOSFET in the opposite side of the gate electrode of the poly-crystal silicon (poly-silicon) formed on for example, the surface of GOX and gate electrode, and the part thickly doped in the relatively of 2 of the active layer comprising the drain. It acts in order to the relative thick (it compares with GOX) field oxide (FOX) separate MOSFET and electrically insulate. Similarly, MESFET the generally the MES IC includes multiple MESFETs (the MES field effect transistor) is composed of the gate electrode of MESFET is the metal or the metal-containing mixture, in other words, the metal silicide. And in the semiconductor material and direct contact that it contacts, it is different from MOSFET.

현재 상업적으로 유용한 IC에 있어서, 게이트 전극의 길이, 즉 전류 채널의 길이는 통상적으로 약 2마이크로미터(㎛)이며, 소스 및 드레인의 두께는 약 0.5㎛이다. 그러나 증가된 패킹 밀도(별개 소자의)를 가진 IC를 실현하기 위해, 게이트 전극 길이(즉 전류 채널 길이)가 약 1㎛보다 작거나 같게 축소될 것으로 기대된다. 동시에, 통상 짧은 채널 영향으로 불리는 어떤 바람직하지 않은 영향을 피하기 위해, 소스 및 드레인의 두께가 약 0.2㎛보다 작거나 같은 값으로 축소될 것이다(여기서 언급된 바람직하지 않은 짧은 채널 영향은 바람직하지 않은 임계 전압 시프와 소스-드레인 부임계 결핍 전류인데, 이것은 소스/드레인 두께에 대한 채널 길이의 비율이 비교적 작을때 즉, 약 2.5 이하일때 발생한다. 짧은-채널 영향에 대해서는 제이.알.브로우스 등의 #8220#MOSFET 소형화에 대한 일반 안내#8221#란 논문을 참조하라).

Presently, as to the commercially useful IC, the length of the gate electrode, in other words, the length of the current channel, generally, the thickness of about 2 micrometer (㎛), the source and drain are about 0.5㎛. But in order that IC having the increased packing density (of the discrete device) is realized it is smaller than about 1㎛ or it is the same the gate electrode length (in other words, the current channel length) be reduced. Simultaneously, generally, it in order to avoid the influence noting any kind of be desirable paper called the short channel effect is the critical voltage thief and the source-drain subthreshold lack current in which the short channel effect noting the be desirable paper which the thickness of the drain and source will be reduced to the value which is smaller than about 0.2㎛ or thes same is mentioned nots the be desirable paper. Relatively when the rate of the channel length about the source/drain thickness is little, when being in other words, about 2.5 or less, this is generated. J about short - channel effect. The general guideline " about the "MOSFET miniaturization including the egg Brouse. etc. refers to paper.

비교적 얇은 소스 및 드레인, 즉 0.2㎛이하인 두께를 가진 소스 및 드레인은 바람직하지 못하게 큰 저항을 가지는데, 이것은 소자의 성능에 역으로 영향을 미친다. 비교적 얇은 소스 및 드레인을 사용하여 비교적 낮은 소스/드레인 저항을 실현하기 위해, 몰리브데늄 실리사이드(MoSi2), 텅스텐 실리사이드(WSi2)나 티타늄 실리사이드(TiSi2)와 같은 금속 실리사이드의 위에 놓인 영역을 포함하도록 각각의 비교적 얇은 소스 및 드레인

Relatively, the source and the drain having the thickness which is the thin source and drain, in other words, 0.2㎛ or less have the big resistance to cannot with the be desirable paper. This reversely affects the element performance. Relatively, it was proposed that the source and the drain which was thin with each relative were formed but the purpose acts as the low-ohmic

GF Exhibit 1124 - 1946/2704

이 형성되는 것이 제안되었는데 그 목적은 저-저항 전류 분류기로서 작용하도록 한 것이다. 이에 관해 금속 실리사이드 커버된 소스 및 드레인의 효과적인(전기적)두께, 즉 소스-드레인-게이트 상호 작용에 포함되는 두께는 활성층의 표면 아래로 뻗어있으며 그 표면에 비교하여 아래에 놓인(두껍게 도핑된) 소스 및 드레인과 금속 실리사이드 영역의 결합된 두께이다.

electric current division device in order to include the molybdenum silicide (MoSi(SB)2(/SB)) the relatively low source/drain resistance is realized using the source and the thin drain, and the domain put on the upper part of the metal silicide like the tungsten silicide (WSi(SB)2(/SB)) or the titanium silicide (TiSi(SB)2(/SB)). It is the source, which the effective thickness of the drain and the source , and the thickness included in other words, the source-drain - gate interaction compare in the surface the metal silicide is covered about this while spreading under the surface of the active layer and is put (it the thickly is doped)s the drain and the combined thickness of the metal silicide domain.

금속 실리사이드 커버된 소스 및 드레인을 포함하는 IC를 제조하기 위한 이전의 시도는 소스 및 드레인을 형성하기 위한 통상적인 절차의 이용을 포함하고 있는데, 즉 소스 및 드레인이 필요한 실리콘 기판의 영역으로 소스 및 드레인 도펀트를 주입 및 확산하는 단계와 다음에 밑에 있는 소스 및 드레인의 표면에 Mo, W, Ti와 같은 금속을 증착시키는 단계를 포함하고 있다. 이때 증착된 금속은 대응하는 금속 실리사이드를 형성하도록 소스 및 드레인의 아래에 놓인 실리콘과 반응한다. 이 기술은 소스 및 드레인이 초기에(금속 실리사이드의 형성에 앞서) 실리콘내로 비교적 깊게 연장된 경우, 즉 실리콘내로 약 0.25㎛ 이상 연장된 경우에 효과적인 것으로 입증되었다. 그러나 이 기술은 소스 및 드레인이 초기에 실리콘내로 비교적 작은 거리만을 연장되어 있는 경우, 즉 약 0.25㎛보다 작거나 같은 거리만큼 연장되어 있는 경우에는 바람직하지 못한 것으로 입증되었는데, 이것은 바람직하지 못하게 큰 양의 소스/드레인 실리콘이 금속 실리사이드를 형성하는데 소비되어 결과적으로 소스/드레인 p-n 접합을 통해 연장된 즉 단락 회로시키는 금속 실리사이드 스파이크를 초래하기 때문이다.

The previous attempt for manufacturing the source which the metal silicide is covered and IC including the drain comprise the step of evaporating the Mo on the surface of the step of being expanded over the domain of the silicon substrate in which in other words, the source and drain are necessary it injects the source and drain dopant it includes the usage of the normal procedure for forming the source and drain and the source which is in the beneath in the next and drain, W, and the metal like the Ti. It then reacts with the silicone which is beneath puts of the drain and source in order to form the metal silicide in which the deposited metal corresponds. Relatively in case this technology the source and drain were deeply extended due to the initial (before the formation of the metal silicide) within the silicone with it was effective in case of being extended within in other words, the silicone over about 0.25㎛ it was proved. But it was proved that it could not with the be desirable paper in case this technology the source and drain were extended due to the initial within the silicone only the distance which was relatively small as the distance which was smaller than the case, of being extended in other words, about 0.25㎛ or thed same. When the metal silicide is formed but the source/drain silicone of the large amount is consumed and so that this cannot with the be desirable paper this is extended through the source/drain p-n junction the key in the short circuit is due to cause the metal silicide spike.

금속 실리사이드 커버된 소스 및 드레인을 형성하기 위한 다른 기술이 1983년 IEDM 기술 다이제스트 670 내지 673페이지에 #8220#실리사이드를 통한 측면 확산을 이용한 새로운 저저항의 얇은 접합 형성 방법#8221#이란 제목으로 에이취.오가바야시 등에 의해 기술되어 있다. 이 기술에 따라, 이와 같은 소스 및 드레인은 초기에 실리콘 기판의 표면상에 예를들어 0.1㎛의 두께를 가진 몰리브데늄 실리사이드(MoSi2) 영역을 제조함으로써 형성되는데, 이것은 실리콘 기판상에 몰리브데늄을 증착시키고 아래에 놓인 실리콘과 몰리브에늄을 반응시킴으로써 실현된다. 이때 소스/드레인 도펀트를 몰리브데늄 실리사이드로 확산되어 그곳으로 부터 소스/드레인 p-n 접합을 형성하도록 아래에 놓인 실리콘으로 확산된다. 즉 몰리브데늄 실리사이드 커버된 실리콘 기판이 개스 또는 고체의 도펀트 소스에 접촉되어져 한 단계로 몰리브데늄 실리사이드와 아래에 놓인 실리콘내로 도펀트를 효과적으로 확산시키기 위해 충분히 높은 온도와 충분히 긴 시간 주기동안, 즉 1000℃에서 20분동안 가열된다. 이와 달리 도펀트는 2단계 공정으로 실리콘내로

The thin joining formation process " of the new low resistance in which the source which the metal silicide is covered and the dissimilar technology for forming the drain use the side spreading through the " silicide for 1983 year IEDM technology digest 670 through 673 page is the title H. It is described by the auger drill night market etc. According to this technology, by manufacturing the molybdenum silicide (MoSi(SB)2(/SB)) domain having for example, the thickness of 0.1㎛ on the surface of the silicon substrate at a rate per the initial this kind of source and drain are formed. By reacting the silicone and the mole rib enium in which this evaporates molybdenum on the silicon substrate and which is beneath puts it is realized. Then, it is diffused to the silicone which is beneath puts in order to be the source / drain dopant diffused including to the molybdenum silicide and form the source/drain p-n junction from that place. That is,

GF Exhibit 1124 - 1947/2704

확산되는데, 제1단계는 초기에 몰리브데늄 실리사이드 커버된 실리콘 기판을 비교적 낮은 온도, 즉 800℃로 가열하여 가스 또는 고체의 도펀트 소스로 부터 몰리브데늄 실리사이드내로(실리콘내로는 확산되지 않음)도펀트를 확산시키는 것이다. 계속해서 도펀트는 실질적으로 보아 높은 온도, 즉 950℃나 1000℃로 기판을 가열함으로써 몰리브데늄 실리사이드로 부터 실리콘내로 확산된다. 1단계 확산 공정을 비교적 깊은 소스 및 드레인을 만드는데, 즉 만일 몰리브데늄 실리사이드가 0.1㎛ 두께이면, 소스 및 드레인은 실리사이드의 상부 표면 아래로 약 1.5㎛ 연장된다. 2단계 확산 공정은 보다 얕은 소스 및 드레인을 만드는데, 이것은 비교적 깊은 것으로서, 만일 몰리브데늄 실리사이드가 0.1㎛ 두께라면, 소스 및 드레인은 실리사이드의 상부 표면아래로 약 0.36㎛ 연장된다.

enough enough heated with the high temperature for the long time period in other words, 1000℃ for 20 minutes the dopant is effectively diffused to the step that the silicon substrate which the molybdenum silicide is covered is contacted with the dopant source of the gas or solid within the silicone which is beneath puts with the molybdenum silicide. On the other hand, the dopant is diffused to 2 stage processing within the silicone. The first step heats the silicon substrate which the molybdenum silicide is covered with the relatively low temperature, in other words, 800℃ in the initial and the dopant is diffused from the dopant source of the gas or solid in the molybdenum silicide (it is not diffused within the silicone). And then, by the dopant substantially looking and heating the substrate with the high temperature, in other words, 950℃ or 1000℃ the dopant is diffused from the molybdenum silicide within the silicone. 1 step diffusion process the source and the drain which is relatively deep is made. If the molybdenum silicide is 0.1㎛ thickness , the source and drain are extended under the top surface of the silicide with about 1.5㎛. The source and the drain which is shallow than 2 step diffusion process are made. Relatively this is deep. The molybdenum silicide is 0.1㎛ thickness. If it is the case the source and drain are extended under the top surface of the silicide.

금속 실리사이드 커버된 소스 및 드레인을 형성하기 위해 이전에 사용된 또다른 기술에 있어서, 텅스텐 실리사이드(WSi2) 영역이 초기에 실리콘 기판상에 형성되고 텅스텐 실리사이드내로 도펀트가 주입된다(확산이 아님)(1985년 IEDM 기술 다이제스트 407 내지 410페이지에 있는 에프.씨.숀 등의 #8220#도핑된 실리사이드 기술에 의한 0.1㎛ N+/P와 P+/N 접합의 형성#8221#을 참조) 이때 주입된 도펀트는 통상적인 용광로 어닐링 기술이나 금속 열 어닐링(RTA)기술을 이용하여 기판을 가열함으로써 텅스텐 실리사이드로 부터 실리콘 기판내로 확산된다(RTA에 대해서는 1983년 전자화학회의 저널 130권의 484페이지에 있는 티.오.세리윅크의 #8220#단시간 어닐링#8221#을 참조) 중요하게도(에프.씨.숀 등에 의해 알려진 바와 같이), 텅스텐 실리사이드 영역의 두께는 0.2㎛이며, 대응하는 주입량과 가열 온도 및 가열 시간은 텅스텐 실리사이드의 특정 두께에 대해 모두(추정적으로)특수하게 맞추어진다. 결과적으로, 상기 특정 기술은 단지 0.3㎛보다 크거나 같은 깊이(텅스텐 실리사이드의 상부 표면으로 부터 측정될때)를 가진 소스 및 드레인만을 만들게된다.

F which the tungsten silicide (WSi(SB)2(/SB)) domain is formed in the initial on the silicon substrate and the dopant is injected as to the source which the metal silicide is covered and another technology which is used in order to form the drain, within the tungsten silicide (it is not diffusion) is in 1985(year IEDM technology digest 407 through 410 page. The furnace annealing technology, in which the dopant which is then the formation " of 0.1㎛ N + / P by the A -doped silicide technology the " including seed etc. and P + / N union injected with the reference) is normal importantly, the drawing F it is diff used from the tungsten silicide within the silicon substr ate (the reference the " short time annealing " of the t hio. ***. which is in 484 page of the journal 130 Keow n of 1983 year electronization learned society about RT A) the substrate is heated up using the metal thermal annealing (RTA) technology. As is well known, seed the thickness of the tungsten silicide area is 0.2㎛ with the etc. and the everyone (putatively) is unusual the injec tion amount, the heating temperature and heating time corresponding to are adjusted about the specific thickn ess of the tungsten silicide. Consequently, it produces only the source and the drain in which the specific tec hnique has the depth (it is measured from the top surfa ce of the tungsten silicide) which is only greater than 0.3㎛ or thes same.

1986년 산 디에고의 VLSI에 관한 1986 심포지엄에서 논문 다이제스트의 #8220#서브-미크론 CMOS에 대한 TiSi2 및 WSi2 실리사이드된 낮은 접합의 비교#8221#란 제목으로 엔.고바야시 등에 의해 상기 기술의 변형이 기술되어 있다. 여기에서는 텅스텐 실리사이드 또는 티타늄 실리사이드의 0.1㎛ 두께 영역이 초기에 실리콘 기판상에 형성되고, 소스/드레인 도펀트가 실리사이드 내로 주입되어 실리사이드로 부터 실리콘내로 확산

In 1986 symposium about VLSI of 1986 year San Diego, disclosed is the deformation of technology including the comparison " of the low junction which is silicidated the TiSi 2 about the " sub-micron CMOS of the paper digest and WSi 2 is the title N Kobayashi. etc. Here, 0.1㎛ thickness domain of the tungsten silicide or the titanium silicide is formed in the initial on the silicon substrate a

GF Exhibit 1124 - 1948/2704

된다. 그러나 텅스텐 실리사이드의 경우에 엔.고바야시 등의 저널 논문의 제1도에 도시된 바와같이, 이 논문의 저자는 0.2㎛보다 훨씬 큰 깊이(텅스텐 실리사이드의 상부 표면으로 부터 측정할때), 즉 0.26㎛ 및 0.28㎛의 깊이를 가진 소스 및 드레인을 만드는 주입량과 가열 온도 및 가열 시간을 가르쳐주고 있다. 이에 대비하여, 티타늄 실리사이드의 경우에는 제1도에 도시된 바와같이 저자가 0.2㎛보다 작은 깊이(티타늄 실리사이드의 표면으로 부터 측정할때), 즉 0.16㎛의 깊이를 가진 소스나 드레인을 만드는 비소 주입량과 가열 온도 및 가열 시간을 가르쳐 주고 있지 않다. 그러나 제1도로 부터 명백한 바와같이, 티타늄 실리사이드/실리콘 인터페이스에서의 비소의 농도는 비교적 낮다. 이것은(저널 논문의 저자의 주장과는 반대로) 상기 비교적 낮은 인터페이스 농도가 바람직하지 못하게 높은 특정 저항(Rc)을 유도하기 때문에 매우 중요한데, 여기서 Rc는 10-6Ω-Cm2보다도 크다. 사실 상기 저널 논문에서 저자는 인터페이스 비소 농도를 증가시키기 위해(추정상 Rc를 낮추기 위한 목적으로) 추가의 비소를 실리콘(티타늄 실리사이드가 아닝) 대로 주입하는 바람직성을 나타내고 있다. 그러나 불행하게도 알려진 바와같이, 이와 같은 절차는 실리콘 기판이 추가의 도펀트 확산, 결과적으로 비교적 깊은 소스 및 드레인을 만드는 실리콘내로의 생성 주입 손상을 어닐링하기 위해 비교적 높은 온도로 가열되어야만 하기 때문에 바람직하지 못하다.

nd the source / drain dopant is injected within the silici de and it is diffused from the silicide within the silicone. But in case of the tungsten silicide, the source, in whic h the author of this paper has the depth (it measures f rom the top surface of the tungsten silicide), which is more greater than 0.2㎛ in other words, the depth of 0.28㎛ and 0.26㎛ the injection amount, making the drai n the heating temperature and heating time are taught as shown in Figure 1 of the journal paper including N Ko bayashi. etc. Thus, it compares and the source in whic h the author has the depth (it measures from the surfa ce of the titanium silicide), smaller than 0.2㎛ in other words, the depth of 0.16㎛ in the titanium silicide as sh own in Figure 1 or the arsenic implant amount making t he drain and heating temperature and heating time are not taught. But as shown in it is clear from Figure 1 rel atively the concentration of the arsenic at the titanium silicide / silicon interface is low. Because the high speci fic resistance (Rc) is induced so that the interface con centration which is low with this (contrary to the insist ence of the author of the journal paper) relative canno t with the be desirable paper it is very important. Here the Rc is greater than 10 - 6 Ω- Cm 2 . Fact, in the jo urnal paper, so that the author increase the interface arsenic concentration (to the purpose of lowering the e stimation phase Rc), the additional arsenic the overall quality injected is shown according to silicone (it is not titanium silicide). But because the relatively high tempe rature has to be heated by this kind of the procedure s o that the silicon substrate anneal the additional dopan t diffusion, and the production injection damage into th e source which is consequentlyrelatively deep and the silicone making the drain as is well known, it unfortunat ely cannot with the be desirable paper.

그러므로 IC제조 방법의 개발에 종사하는 사람들은 약 10-6Ω-cm2 이하의 Rc를 나타내는 금속 실리사이드를 포함하는 비교적 얕은 소스 및 드레인을 가진 IC를 제조하기 위한 방법을 추구해왔다.

Therefore, the process for manufacturing the source which was relatively shallow including the metal silicide in which the people engaged in the development of the method of fabricating IC showed the Rc less than abou t 10 - 6 Ω- cm 2 and IC having the drain had been bein g investigated.

본 발명은 금속 함유 물질 영역, 즉 기초 금속이나 금속 실리사이드와 같은 금속 함유 혼합물을 함유하는 영역으로 커버된 소스나 드레인을 형성하기 위한 새로운 기술을 포함한다. 중요하게도 이 새로운 기술은 약 0.2㎛이하의 깊이(물질 영역의 상부 표면과 비교하여)를 갖고 약 10-6Ω-cm2이하의 Rc를 나타내는 물질 영역 커버된 소스나 드레인을 만든다.

The invention includes the source covered with the domain containing the metal containing mixture or the new technology for forming the drain, such as the met al containing material domain, in other words, the base metal or the metal silicide. Importantly, the source or t he drain which the territory of material in which this ne w technology has the depth (it compares with the top surface of the territory of material) less than about 0.2 ㎛ and showing the Rc less than about 10 - 6 Ω- cm 2 i s covered is made.

본 발명의 기술에 따라, 0.2㎛이하의 평균 두께 t를 가진 금속 함유 물질 영역이 초기에 반도체 기판의 표면상에 형성된다. 그 다음에, 하나 혹은 그 이상의 도펀트가 상기 영역에 주입되고, 반도체 기판이 가열되어 상기 도펀트가 상기 영역으로 부터 기판내로 확산되게 된다. 약 10-6Ω-cm2이하의 Rc를 발생하기 위해, 가열 절차는 상기 물질 영역/기판 인터페이스에 인접한 기판에서 최소한 하나의 도펀트를 집중시켜야 하는데, 이것은 기판 가열전의 인터페이스에서의 쇼트키 전위 장벽의 높이에 의해 결정되는 최소 값보다 크거나 같다. 상기 최소값을 실현하기 위해 다음 3조건이 만족되어야 한다고 알려져 있다. 제1조건은 가열 절차 동안에 사용된 온도에서 기판내의 최소한 하나의 도펀트의 고체 용해도가 상기 최소값보다 크거나 같아야 한

According to the technology of the invention, the metal containing material domain having the average th ickness t less than 0.2㎛ is formed in the initial on the s urface of the semiconductor substrate. And then, one or the dopant described in the above is injected in the domain and the semiconductor substrate is heated and the dopant is diffused from the domain within the subst rate. In order that it is generated the Rc less than abo ut 10 - 6 Ω- cm 2 the dopant of at least one has to be focused in the substrate in which the heating process i s adjacent to the territory of material / plate interface. It is greater than the minimum value in which this is de

GF Exhibit 1124 - 1949/2704

다는 것이다. 제2조건은 상기 동일한 도펀트에 있어서, 상기 물질 영역의 평균 두께에 대한 대응하는 주입량의 비율이 상기 가열 온도에서 상기 물질 영역내의 상기 도펀트의 고체 용해도의 약 1/2보다 크거나 같아야 된다는 것이다.(이것에 대해서, 예를들어, 엔.고바야시 등에 의해 사용된 비소 주입량이 상기 제2임계 요구조건을 만족하지 못한다고 결정되었다). 원하는 인터페이스 농도를 실현하고 유용한 소스/드레인 접합을 실현하기 위해 만족되어야할 제3조건은, 상기 동일한 도펀트에 대해 상기 물질 영역내로 주입되는 도펀트 이온의 총수효가 아래에 놓인 확산된 소스 및 드레인을 형성하는데 필요한 수보다 실질적으로 커야된다는 것이다. 만일 상기 물질 영역/기판 인터페이스에 가까이 인접한 기판에서의 도펀트의 농도의 필요한 최소값이 Co로 표시되고 상기 물질 영역의 바닥과 비교하여 소스/드레인 접합의 원하는 깊이가 X로 표시되면 제3조건은 자동적으로 1g5Co#183#X/2가 만족된다. 실예로 제2조건을 만족하는 주입량은 또한 제3조건도 만족한다. 그러나 주입량의 제2조건을 만족하지만 5Co#183#X/2 보다 작은 경우에 제3조건은 Co#183#X/2보다 크거나 같은 양만큼 상기 주입량을 증가시킴으로써 확실하게 만족되게 된다.

termined with the height of the schottky potential barrier at the interface of the substrate heating total or it is the same. It is known the minimum value is realized that the next 3 condition has to be satisfied. In the temperature in which the first condition is used for the heating process, it is greater than the minimum value or the solid solubility of the dopant of at least one within the substrate has to be the same. As to the article 2 gun is the above-mentioned same dopant, the rate is large than about 1/2 of the solid solubility of the dopant within the territory of material or the rate of the injection amount corresponding to about the average thickness of the territory of material be the same in the heating temperature. (This was determined that the arsenic implant amount used with the etc. was unable to be satisfied the second critical requirement specification about this) The article 3 gun to be satisfied it realizes the source/drain junction realizing the desired interface concentration and is useful forms the source and the diffused drain in which the total amount of the dopant ion injected within the territory of material is beneath puts about the above-mentioned same dopant but the substantially is *** than the necessary number. If the necessary minimum value of the concentration of the dopant at the substrate adjacent to the territory of material / plate interface is indicated as the Co and it compares with the bottom surface of the territory of material and the desired depth of the source/drain junction is indicated as X, the article 3 gun 1 g5Co·X / 2 is automatically satisfied. For example, the injection amount satisfied the article 2 gun moreover, the article 3 gun is satisfied. But it is satisfied the article 2 gun of the injection amount but in case of being smaller than 5Co·X / 2 since the article 3 gun increases the injection amount as the amount which is large than the Co·X / 2 or thes same it is authentically satisfied.

본 발명의 기술은 또한 원하는 깊이를 가진 소스 및 드레인을 만드는데 필요한 가열 온도-시간 프로필을 선택하기 위한 절차(후술됨)를 포함한다.

The technology of the invention includes the source having the desired depth and the procedure (it is mentioned later) which it is to make the drain but select the necessary heating temperature - time profile.

본 발명은 MOS나 MES 반도체 IC와 같은 반도체 소자뿐 아니라 그 합성 소자를 제조하기 위한 방법을 모두 포함하고 있다. 본 발명의 방법에 따라 제조된 소자는 금속 함유 물질 영역, 즉 텅스텐(W)과 같은 기초 금속을 함유하는 영역으로 커버된 최소한 하나의 소스나 드레인을 포함하고 있다. 이와 달리 금속 함유 물질 영역은 금속 실리사이드, 즉 코발트 실리사이드(CoSi2), 티타늄 실리사이드(TiSi2), 텅스텐 실리사이드(WSi2), 몰리브데늄 실리사이드(MoSi2), 탄탈륨 실리사이드(TaSi2)나 플라티늄 실리사이드(ptSi)와 같은 금속 함유 혼합물을 포함한다. 또한 상기 물질 영역의 상부 표면에 비교하여 상기 물질 영역으로 커버된 소스나 드레인의 깊이는 약 0.2㎛ 보다 작거나 같다. (본 발명의 목적을 위해 상기 물질 영역 커버된 소스나 드레인의 깊이는 상기 물질 영역의 상부 표면에 대한 최소 면적 평면 근사부로 부터 소스나 드레인이 형성되는 반도체 기판과 소스나 드레인 사이의 인터페이스의 최저점까지 직각으로 연장된 길이다. 만일 예를들어 소스나 드레인이 n형 전도성이면 인터페이스는 소스나 드레인에서의 n형 도펀트의 농도가 기판에서의 p형 도펀트의 농도가 같은 (그 역도 마찬가지임) 점들이 궤적이다. 이와 같은 인터페이스는 2차 이온 질량 분광학(secondary ion mass spectroscopg : SIMS)과 같은 종래의 기술을 이용하여 쉽게 위치된다.) 또한 아래에 놓인(확산된) 소스나 드레인에 대한 상기 물질 영역의 특정 접촉 저항, Rc는 약 10-6Ω#183#cm2보다 작거나 같다.(Rc는 IEEE전자

The method in which the invention manufactures not only the semiconductor device like MOS or the MES semiconductor IC but also the synthesis element the altogether is included. The device manufactured according to the method of the invention includes the source or the drain of at least one covered with the domain containing the base metal, such as the metal containing material domain, in other words, the tungsten (W). On the other hand, the metal containing material domain comprises the metal silicide, in other words, the cobalt silicide (CoSi(SB)2(/SB)), the titanium silicide (TiSi(SB)2(/SB)), the tungsten silicide (WSi(SB)2(/SB)), the molybdenum silicide (MoSi(SB)2(/SB)), the tantalum silicide (TaSi(SB)2(/SB)), or the metal containing mixture like the platinum silicide (ptSi). Moreover, it is smaller than about 0.2㎛ or the depth of the source or the drain which compares in the top surface of the territory of material and which is covered with the territory of material is the same. (It is the way in which the depth of the source or the drain which the territory of material is covered for the object of the present invention is abeam extended to the peak base of the interface between the semiconductor substrate in which the source or the drain is formed from the minimum area plane approximation part

GF Exhibit 1124 - 1950/2704

소자란 책의 544페이지에 있는 케이.케이.에지, #8220#MOSFET의 접촉 저항을 측정하기 위한 새로운 기술#8221#에 기술된 종래의 절차를 이용하여 쉽게 측정된다.)

toward the top surface of the territory of material and the source or the drain. For example, if the source or the drain is the n-type conductivity, it is the trajectory the concentration of the P-dopant at the substrate as to the interface, of the concentration of the n-type dopant at the source or the drain is the same (it applies equally to the reverse) that. It is smaller than about 10 - 6 Ω· cm 2 or the specific constant resistance of the territory of material about the source or the drain , and the Rc which this kind of the interface is easily located using the conventional technology like the secondary ion mass spectrometry (secondary ion mass spectroscopg : SIMS) is moreover beneath put (it is diffused)s are the same. K in which (Rc the IEEE electric component is in 544 page of book. K. It is easily measured using the conventional procedure described in the new technology " for measuring the edge, and the constant resistance of the "MOSFET.

본 발명의 방법에 따라, 상기 물질 영역 커버된 소스나 드레인이 초기에 실리콘이나 갈륨 비소와 같은 반도체 물질을 포함하는 기판상에 상기 물질 영역을 형성함으로써 형성된다. 이와 같은 물질 영역은 예를들어, 종래 기술, 즉 종래의 스퍼터링(sputtering)기술을 이용하여, 기판상에 상기 영역을 구성하는 물질을 침착시킴으로써 형성된다. 이와 달리, 만일 상기 물질 영역이 예를들어 금속 실리사이드를 포함하고 기판이 실리콘으로 되어 있으면, 상기 물질 영역은 대응하는 기초 금속을 실리콘 기판상에 침착시키고 금속 실리사이드를 형성하기 위해 침착된 금속을 아래에 있는 실리콘과 반응시킴으로써 최소한 부분적으로 쉽게 형성된다. 약 0.2㎛보다 작거나 같은 깊이를 가진 상기 물질 영역 커버된 소스나 드레인을 실형하기 위해서는 상기 물질 영역의 최대 두께, 즉 결과적으로 평균 두께(일반적으로 균일하지 않은 두께임)가 0.2㎛보다 작아야 된다. 또한 (균일하지 않은 두께의) 상기 물질 영역의 최소 두께는 약 0.1㎛보다 크거나 같은 것이 양호하다. 약 0.1㎛보다 작은 최소 두께는 바람직하지 못한데 이것은 다른 이유중에서, 상기 물질 영역의 대응하는 부분이 종종, 주입 단계동안에 매우 많은 양의 도펀트를 상기 물질 영역이 아닌 기판내로 주입되도록 허용하는 매우 많은 수의 핀구멍을 포함하게 되기 때문이다.

According to the method of the invention, since the source or the drain which the territory of material is covered forms the territory of material on the substrate including the semiconductor material such as the silicone and GaAs in the initial the drain is formed. By sinking the material comprising the domain on the substrate this kind of the territory of material is formed using for example, the prior art, in other words, the conventional sputtering technology. On the other hand, if the territory of material includes for example, the metal silicide and the substrate if to the silicone , by the base metal in which the territory of material corresponds being sunk on the silicon substrate and reacting the metal which is deposited in order to form the metal silicide, with the silicone which is beneath have the metal is partly easily formed. It is for the source or the drain which the territory of material having the depth which is smaller than about 0.2㎛ or thes same is covered with the prison sentence and consequently the average thickness (it the generally is the thickness which is not uniform) be smaller than 0.2㎛ with the maximum thickness of the territory of material. Moreover, is good what the minimum thickness of (of the thickness which is not uniform) territory of material is greater than about 0.1㎛ or thes same. The minimum thickness smaller than about 0.1㎛ cannot with the be desirable paper but the part corresponding to of the territory of material includes the pin hole which often allows very many dopant of the amount for the impregnation step in order to be injected within the substrate which is not territory of material, and is very many of the number among the reason why this is different.

상기 물질 영역을 형성한 후에, 하나 혹은 그 이상의 도펀트가 상기 물질 영역내로 주입되고, 계속해서 원하는 소스나 드레인을 형성하기 위해 상기 물질 영역으로 부터 상기 기판내로 주입된 도펀트가 확산되도록 기판이 가열된다. 만일 기판 반도체 물질이 p형 전도성이면, 주입된 도펀트는 기판에서 전자도우너를 형성해야 하며, 만일 기판 반도체 물질이 n형 전도성이면 상기 도펀트는 전자 액셉터를 형성해야 한다. 예를들어 실리콘의 경우에, 유용한 도오너 이온은 인(p)과 비소(As)이온을 포함하며, 동시에 유용한 액셉터 이온은 붕소(B)이온을 포함한다.

After the territory of material is formed one or the dopant described in the above is injected within the territory of material and the substrate is heated so that the dopant injected from the territory of material within the substrate is diffused in order to form the source or the desired drain. If the substrate semiconductor material is the p-type conductivity , the injected dopant has to form the electron donor at the substrate and the dopant has to form the electron acceptor if the substrate semiconductor material is the n-type conductivity. For example, the drawing owner ion which is useful in case of the silicone includes the phosphorus (p) and the acceptor ion which includes the arsenic (As) ion and is sim

GF Exhibit 1124 - 1951/2704

ultaneously useful. Is the boron (B) ion.

전술한 바와같이, 약 10-6Ω#183#cm2보다 작거나 같은 Rc를 실현하기 위해, 기판 가열 절차는 상기 물질 영역/기판 인터페이스에 인접한 기판에서의 최소한 하나의 도펀트의 농도를 산출해야 되는데 이것은 기판 가열 이전의 상기 물질 영역/기판 인터페이스에서의 쇼트키 전위 장벽의 높이에 의해 결정되는 최소값보다 크거나 같다. 즉, 상기 전위 장벽 높이를 아는 것은 대응하는 최소값을 의미하고 있다. 이점에 있어서, 금속 함유 물질과 반도체 물질 사이의 인터페이스에서의 쇼트키 전위 장벽 높이는 원하는 Rc를 발생시키기 위해 인터페이스 도펀트 농도의 대응하는 최소값이 필요한 바와같이 문헌상 쉽게 이용할 수 있다. 예를들어, n형이나 p형 실리콘과 다양한 기초 금속 사이의 인터페이스에서의 쇼트키 전위 장벽 높이는 에스.엠.스제의 #8220#반도체 소자의 물리학#8221# 제2판(1981) 292 페이지에서 찾아볼 수 있다. 비슷하게 예를들어 n형 또는 p형 실리콘과 다양한 기초 금속 사이의 인터페이스 사이의 쇼트키 전위 장벽 높이는 에스.피.뮤라카의 #8220#VLSI 응용을 실라이드#8221#(1983) 15페이지에서 찾아볼 수 있다.

As described above, in order that the Rc which is smaller than about 10 - 6 Ω· cm 2 or thes same is reali zed it is greater than the minimum value which produce the concentration of the dopant of at least one at the substrate in which the substrate heating process is adj acent to the territory of material / plate interface but i n which this is determined with the height of the schot tky potential barrier at the territory of material / plate i nterface of the substrate heating previous or it is the s ame. That is, the minimum value in which it correspond s to know the potential barrier height is meant. As to t he advantage, in order to generate the Rc in which the schottky potential barrier height at the interface betwe en the metal containing material and the semiconducto r material desires, as the minimum value corresponding to of the interface dopant concentration been necessa ry it easily can use. For example, the schottky potentia l barrier height at the interface between the n-type or the p-type silicone and the various base metal is S. It can look out in the physics " second board (1981) 292 page of the " semiconductor device of M S. M. Sze. An alogously, for example, the schottky potential barrier h eight between the interface between the n-type or the p-type silicone and the various base metal is S. The "V LSI application of the blood Mura. car can be looked ou t in the ride #8221 U # (1983) 15 page.

또한 거의 모든 쇼트키 전위 장벽 높이에 대응하는 약 10-6Ω#183#cm2보다 작거나 같은 Rc를 발생시키는데 필요한 최소 인터페이스 도펀트 농도는 에스.엠.스제의 상기 참조 논문의 304 내지 305페이지에서 찾아볼 수 있다. 예를들어 만일 상기 물질 영역이 코발트 실리사이드(CoSi2)를 포함하고 기판이 p형 실리콘을 포함하며 주입된 n형 도펀트중 하나가 비소(As)라면, 에스.피.뮤라카의 상기 참조 온도에 따라, 대응하는 쇼트키 전위 장벽 높이는 0.64볼트이며, 에스.엠.스제의 상기 참조는 논문에 따라 비소의 대응하는 최소 인터페이스 농도는 약 1#215#1020cm-3이다. 비슷하게, 만일 상기 물질 영역이 티타늄 실리사이드(TiSi2)를 포함하고 기판이 n형 실리콘을 포함하며 주입된 p형 도펀트중 하나가 붕소(B)라면, 에스.피.뮤라카의 상기 논문에 따라 대응하는 쇼트키 전위 장벽 높이는 0.5 볼트이고 에스.엠.스제의 상기 논문에 따라 붕소의 대응하는 최소 인터페이스 농도는 약 3#215#1019cm-3이다.

Moreover, the minimum interface dopant concentration necessary to generate the Rc which is smaller than abo ut 10 - 6 Ω· cm 2 corresponding to all schottky potenti al barrier heights or thes same is S. It can look out in 3 04 of the reference paper of M S. M. Sze. through 305 page. For example, one among the n-type dopant whic h is injected while the territory of material includes the cobalt silicide (CoSi(SB)2(/SB)) and the substrate inclu des the p-type silicone is the arsenic (As), S. S the sc hottky potential barrier height corresponding according to the reference temperature of the blood Mura. car is 0.64 bolt. According to the see above of M S. M. Sze. i s paper, the minimum interface concentration of arseni c corresponding to is about 1× 10 20 cm - 3 . Analogo usly, one among the P-dopant which is injected while t he territory of material includes the titanium silicide (Ti Si(SB)2(/SB)) and the substrate includes N type silicon is the boron (B), S. S the schottky potential barrier hei ght corresponding according to the paper of the blood Mura. car is 0.5 bolt. According to the paper of M S. M. Sze, the minimum interface concentration of boron corresponding to is about 3× 10 19 cm - 3 .

또한 전술한 바와같이, 약 10-6Ω#183#cm2보다 작거나 같은 Rc를 발생시키기 위해 필요한 상기 물질 영역/기판 인터페이스에 인접한 기판에서의 도펀트 농도를 실현하기 위해서는 3가지 조건이 만족되어야 한다고 알려져 있다. 제1조건은 기판 가열 절차동안에 사용된 온도에서 최소한 하나의 도펀트의 기판에서의 고체 용해도가 전술한 최소 인터페이스 농도보다 크거나 같아야 된다는 것이다. 중요하게도, 반도체에서 도펀트의 고체 용해도는 일반적으로 매우 민감하며 온도에 따라 증가한다. 결과적으로 제1조건은 사실 기판 가열 절차동안에 사용될 수도 있는 온도에 대한 최소값 Tmin을 강요한다. 즉, 최소한

Moreover, as described above, in order to realize the dopant concentration at the substrate adjacent to the necessary territory of material / plate interface in order to generate the Rc which is smaller than about 10 - 6 Ω· cm 2 or thes same, , the substrate is known that th ree condition has to be satisfied. In the temperature in which the first condition is used for the substrate heati ng process, it is greater than the minimum interface co ncentration in which the solid solubility at the substrat e of the dopant of at least one describes in the above

GF Exhibit 1124 - 1952/2704

하나의 도펀트의 기판에서의 고체 용해도가 원하는 Rc를 실현하는데 필요한, 상기 물질 영역/기판 인터페이스에 인접한 기판에서의 최소 도펀트 농도의 최소한 같게 되는 것을 보장하기 위해 가열 온도는 Tmin보다 크거나 같아야 된다. 이점에 있어서, 온도 함수로서의 다양한 반도체 물질에서의 다양한 도펀트의 고체 용해도는 문헌에서 이용 가능하다.(즉 에서 엠.스제에 의해 출판된 #8220#VLSI 기술에서의 제이.씨.씨.츠아이#8221#198 내지 199페이지를 참조하라).

or it be the same. Importantly, in the semiconductor, generally the solid solubility of the dopant is very sensitive and it increases according to the temperature. Consequently, the first condition extorts the minimum value Tmin which can be used about the temperature for the substrate heating process in fact. That is, in order to realize the Rc in which the solid solubility at the substrate of the dopant of at least one desires but guarantee being the same of the minimum dopant concentration at the necessary substrate adjacent to the territory of material / plate interface at least, it is greater than the Tmin or the heating temperature be the same. As to the advantage, the various various dopant at the semiconductor materials of solid solubilities as the temperature function plays in literature with available. (J in the "VLSI technology published by M S. M. Sze in other words. 198 through 199 page is referred to the CC. Tsai.

결과적으로 제1조건을 만족하는데 필요한 Tmin은 쉽게 결정된다. 예를들어, 740℃, 800℃ 및 900℃에서, 실리콘에서의 비소의 고체 용해도는 각각 1#215#1020cm-3, 1.5#215#1020cm-3, 2#215#1020cm-2이다. (상기 논문 제이.씨.씨.츠아이를 참조). 만일 비소가 n형 실리콘에서 n형 도펀트로서 사용되고 상기 물질 영역이 CoSi2로 이루어져 있으면, 전술한 바와 같이 원하는 Rc를 실현하는데 필요한 최소 인터페이스 농도는 1#215#1020cm-3이며, 결과적으로 Tmin은 740℃이다. 유사하게, 800℃ 및 900℃에서 실리콘에서의 붕소의 고체 용해도는 각각 3#215#1019cm-3 및 6#215#1019cm-3이다. 만일 붕소가 n형 실리콘에서 p형 도펀트로서 사용되고 상기 물질 영역이 TiSi2라면, 전술한 바와 같이 원하는 Rc를 실현하는데 필요한 최소 인터페이스 농도는 3#215#1019cm-3이며, 결과적으로 Tmin은 800℃이다.

Consequently, it is satisfied the first condition but the necessary Tmin is easily determined. For example, in 740℃, 800℃ and 900℃, the respectively the solid solubility of the arsenic at the silicone is 1× 10 20 cm - 3 , 1.5× 10 20 cm - 3 , 2× 10 20 cm - 2 . (The paper J. If arsenic is used in N type silicon as the n-type dopant and the territory of material is the CC. Tsai made of the CoSi 2 with the reference) , the consequently the Tmin is 740℃ the minimum interface concentration necessary is 1× 10 20 cm - 3 . Similarly, in 800℃ and 900℃, the respectively the solid solubility of the boron at the silicone is 3× 10 19 cm - 3 and 6× 10 19 cm - 3 . Boron is used in N type silicon as the P-dopant and consequently the if the Tmin is 800℃ the minimum interface concentration necessary to realize the territory of material is the TiSi 2 , the desired Rc as described above, is 3× 10 19 cm - 3 .

만족되어야 할 제2조건은 위에서 언급된 최소한 하나의 도펀트에 대해 상기 물질 영역의 두께 t에 대한 대응하는 주입량의 비율, 즉 I/t가 기판 가열동안에 사용된 온도(필수적으로 대응하는 보다 크거나 같은)에서 상기 물질 영역에서의 상기 도펀트의 고체 용해도의 1/2보다 크거나 같아야 되며, 바람직하게는 더 커야된다는 것이다. 여기서 논의되는 고체 용해도는 기판 가열 절차 동안에 사용된 온도에서, 상기 물질 영역과 기판 사이의 인터페이스를 포함하여 상기 물질 영역에서의 최소한 하나의 도펀트의 포화 레벨을 말한다. 중요하게도, 이 포화 레벨은 온도에 민감하며, 일반적으로 온도에 따라 증가한다. 또한 이 포화 레벨은 상기 물질 영역의 합성 성분과 상기 물질 영역의 결정성의 정도에 의존한다(즉, 예를들어 다결정 물질의 경우에, 도펀트는 종종 그레인(grain) 및 그레인 경계내에 분배된다). 또한 상기 포화 레벨은 상기 물질 영역/기판 인터페이스의 특성에 의존하는데, 즉 도펀트가 상기 인터페이스에서 비교적 높게 농축되는지의 여부에 의존한다.

The article 2 gun to be satisfied is the rate of the injection amount corresponding to about the thickness t of the territory of material about the dopant of at least one mentioned by the upper part, and *** it is large than 1/2 of the solid solubility of the dopant at the territory of material are. Here, the interface between the substrate and the territory of material are included and the saturation level of the dopant of at least one at the territory of material is referred to the temperature in which the discussed solid solubility is used for the substrate heating process. Importantly, this saturation level is sensitive to the temperature and the temperature increases according to the temperature. Moreover, this saturation level depends on the extent of the crystallization of the compound ingredient of the territory of material and territory of material moreover, the saturation level depends on the property of the territory of material / plate interface. The property depends on acceptance and rejection of the paper (in case of in other words, for example, the polycrystalline material, the dopant is often distributed within the grain and grain boundary) in which it is relatively high in other words, the dopant is concentrated in the interface.

일반적으로, 기판 가열 절차동안에 사용된 온도에서, (상기 물질 영역/기판 인터페이스를 포함하여) 상기 물질 영역내의 도펀트의 고체 용해도는 실험적으로 결정된다. 즉, 본 발명에 따라, 소자에 사용된 상기 물질 영역과 동일한 평균 두께를 가진

Generally, in the temperature used for the substrate heating process, the solid solubility of the dopant within (the territory of material / plate interface is included) territory of material is experimentally determined. That i

GF Exhibit 1124 - 1953/2704

상기 물질 영역의 제어 샘플이(소자에 사용된 기판과 동일한 합성 성분 및 구조를 가진)반도체 기판상에(소자의 제조에 사용된 바와 동일한 기술을 이용하여)형성된다. (중요하게도, 이하에서 더욱 자세히 설명되는 바와같이, 제어 샘플의 상부 표면의 영역 A는 상기 물질 영역의 그것과 동일하게 되는 것을 필요로 하지 않는다. 제어 샘플을 지탱하는 기판은 비워진 용광로, 즉 주위 압력이 예를들어 10-6 토르(torr)의 값으로 낮아지는 용광로에 배치된다. 이때 관심있는 도펀트를 포함하는 가스가 용광로내로 흘러들어간다. 예를들어, 만일 인이라면 유용한 인 함유 가스는 pH3이다. 유사하게, 만일 도펀트가 비소라면, 유용한 비소 함유 가스는 AsH3이며, 만일 도펀트가 붕소라면 유용한 붕소 함유 가스는 B2H6이다(pH3, AsH3 및 B2H6는 매우 유독성 가스이므로 적당한 안전 예방책이 사용되어야 한다는 것을 주목하자). 이점에 있어서, 도펀트 함유 가스의 유동률은 상기 가스의 부분 압력이 주위 압력의 최소한 백배가 되도록 충분히 높아야 되는데, 만일 주의 가스 압력이 10-6토르이면 도펀트 함유 가스의 부분 압력은 최소한 10-4토르가 되어야 한다. 이 필요성은 제어 샘플이 필수적으로 주위의 오염물질이 아닌 도펀트에 의해서만 (다음 단계동안에)포화되는 것을 보장하기 위한 것이다. 도펀트 함유 가스가 용광로내로 흐르는 동안, 용광로는 관련있는 온도, 즉 기판 가열동안에 사용될 온도로 가열되게 된다. 제어 샘플내에서 도펀트 포화를 실현하기 위해서는 이 온도가 최소한 1분동안 유지되어야 하는데, 최소한 30분동안 유지되는 것이 바람직하다.

s, according to the invention, control sample (it has the compound ingredient which is identical with the used substrate in the device and the structure thereof) of the territory of material having the same average thickness as the territory of material used for the device are formed in the semiconductor substrate phase (using the used for the manufacture of the device same technology). (Importantly, hereinafter, as shown in it is more explained in detail the domain A of the top surface of the control sample does not require being identical with that of the territory of material. It is arranged in the blast furnace in which the substrate supporting the control sample is vacated, and the blast furnace in which in other words, the ambient pressure is decreased to for example, the value of 10 - 6 Torr. Then, the gas including the dopant having finds the gas way within the blast furnace. For example, the phosphorus containing gas which is useful if the if is the phosphorus is the pH 3 . Similarly, the arsenic containing gas is the AsH 3 , the boron contain gas which is useful if the dopant is boron is B 2 H 6 . The dopant is arsenic. If it is the case (it pays attention that the safety precaution in which the pH 3 , and the AsH 3 and B 2 H 6 are very appropriate since it is the toxic gas has to be used). As to the advantage, the flow rate of the dopant containing gas the partial pressure of the gas be enough high so that it becomes at least white times of the ambient pressure. In the partial pressure of the dopant containing gas, at least 10 - 4 Torr has to be if the attention gas pressure is 10 - 6 Torr. This necessity is to guarantee that the control sample is saturated with the dopant which the obligatorily is not neighbouring contaminant with (for the following step). While the dopant containing gas flows within the blast furnace the relevant temperature, and the temperature used for in other words, the substrate heating are heated by the blast furnace. The ionic degree has to be maintained for at least 1 minutes in order to realize the dopant saturation in the control sample. It is the be desirable to be maintained for at least 30 minutes.

도펀트 함유 가스에 영향을 받은 후에 제어 샘플은 용광로로 부터 이동되며 제어 샘플/기판 인터페이스를 포함하며 제어 샘플내의 도펀트 원자의 총 수 N이 예를들어 종래의 SIMS 기술을 이용하여 측정된다. 상기 물질 영역에서 도펀트의 고체 용해도는 바로 N/At이다. (원자의 총 수 N는 표면 영역 A에 선형적으로 비례한다는 것을 주목하자.) 결과적으로, 표면 영역은 다른지만, 동일한 평균 두께를 가진 제어 샘플은 동일한 값의 고체 용해도를 산출하게 된다). 결과적으로 제2조건을 만족하기 위해서는 I/tg0.5N/At가 되도록 I가 선택되어야 한다.

While including the control sample / plate interface after it is affected by the dopant containing gas while the control sample is moved from the blast furnace the total count N of the dopant atom within the control sample is measured using for example, the conventional SIMS technology. In the territory of material, the solid solubility of the dopant is immediately, N / At. (It pays attention that the total count N of the atom is linearly in proportion to the surface region A) Consequently, the surface region is different only whether I have to be selected so that I / t g0.5N / At is in order to the control sample having the same average thickness produce the solid solubility of the same value consequently be satisfied the article 2 gun.

전술한 실험적 절차를 이용하여, 예를들어 만일 상기 물질 영역이 코발트 실리사이드로 이루어지고, 0.07㎛의 평균 두께를 가지며, 실리콘 기판위에 놓여 있고, 도펀트가 비소라면, 5#215 #1015cm-2 이상의 주입량이 800℃의 온도에서 제2조건을 만족한다. 비슷하게, 상기 물질 영역이 티타늄 실리사이드로 이루어져 있고 0.08㎛의 평균 두께를 가지며 실리콘 기판위에 놓여있고, 도펀트가 붕소라면, 1#215#1016cm-2 이상의 주입량의 800℃의 온도에서 제2조건을 만족한다.

The territory of material is made of the cobalt silicide using the above-described empirical procedure for example and it has the average thickness of 0.07㎛ and it is puts on on silicon substrate and the dopant is arsenic. If it is the case the injection amount more than 5× 10 15 cm - 2 is satisfied the article 2 gun at a temperature of 800℃. Analogously, while the territory of material is made of the titanium silicide and it has the average thickness of 0.08㎛ it is puts on on silicon substrate a

GF Exhibit 1124 - 1954/2704

nd the dopant is boron. If it is the case it is satisfied t he article 2 gun at a temperature of 800℃ of the injecti on amount more than 1× 10 16 cm - 2 .

원하는 Rc를 실현하고 유용한 소스/드레인 접합(즉 예를들어 0.5볼트의 전압과 25℃의 온도에서 반전 전류에 대한 진행 전류의 비율이 106보다 크거나 같아지는 접합)을 실현하기 위해 만족되어져야 하는 제3조건은, 최소한 하나의 도펀트에 대해, 상기 물질 영역내로 주입된 도펀트 이온의 총수가 아래에 놓인, 확산된 소스나 드레인을 형성하는데 필요한 수보다 실질적으로 커야된다는 것이다. 만일 상기 물질 영역/기판 인터페이스에 인접한 상기 기판에의 도펀트 농도의 최소값이 Co로 표시되고 상기 물질 영역의 바닥과 비교하여 소스/드레인 P-N접합의 원하는 깊이가 X로 표시되면, 제3조건은 자동적으로 1#8805#5 Co#183#X/2이 만족되도록 제공된다. 그러나 만일 주입량이 제2조건을 만족하지만 5Co#183#X/2보다 작다면, 제3조건은 보다 크거나 같은 양만큼 상기 주입량을 증가시킴으로써 확실하게 만족되게 된다. 이점에 있어서, 위에서 주어진 두 주입량은 또한 제3조건도 만족한다.

The article 3 gun which is satisfied it realizes source/drain junction (the junction which is large than 10 6 or in which the rate of the progressing current ab out the reverse current becomes same at a temperatur e of in other words, for example, the voltage and 25℃ of 0.5 bolt) realizing the desired Rc and are useful form s the source or the diffused drain in which the total co unt of the dopant ion injected within the territory of m aterial is beneath puts about the dopant of at least on e but the substantially is *** than the necessary num ber. If the minimum value of the dopant concentration of the substrate adjacent to the territory of material / plate interface is indicated as the Co and it compares with the bottom surface of the territory of material and the desired depth of the source/drain P-N junction is in dicated as X , the article 3 gun is provided so that 1≥5 Co·X / 2 is automatically satisfied. But if the injection a mount is satisfied the article 2 gun but it is smaller tha n 5Co·X / 2 , by increasing the injection amount as the amount which is large than the article 3 gun or thes sa me it is authentically satisfied. As to the advantage, t wo injection amounts given in the upper part moreover, the article 3 gun is satisfied.

상기 금속 함유 물질 영역내로 주입된 이온의 에너지는 근본적으로 모든 이온, 즉, 이온의 최소한 90퍼센트가 상기 영역내로 주입되는 기초적인 반도체 기판내로는 주입되지 않도록 선택된다는 것을 주목하자. 이점에 있어서, 또한 실리콘의 본 발명에 사용된 금속 함유 물질 영역보다 밀도가 높지 않고, 그러므로 동일한 에너지를 가진 동일한 이온이 상기 물질 영역보다 더 큰 깊이로 실리콘내로 관통된다는 것을 주목하자. 결과적으로, 거의 모든 이온이 상기 물질 영역내로 주입되는 것을 보장하기 위해, 이온 에너지는 상기 물질 영역의 두께이하의 실리콘내로의 대응하는 관통 깊이를 산출하도록 선택된다.(이온 에너지의 함수로서의 실리콘내로의 이온 관통 깊이는 알.에이.콜롤레이저의 #8220#마이크로 전자공학처리 및 소자 설계#8221# 150 내지 153페이지에서 찾아볼 수 있다.)

The energy of the ion injected within the metal containing material domain fundamentally pays attentio n being selected in order not to be injected within the f undamental semiconductor substrate in which all ions in other words at least 90 percent of ion are injected wit hin the domain. As to the advantage, the density is no t moreover higher than the metal containing material d omain used for the invention of the silicone and it there fore pays attention that the same ion having the same energy is penetrated toward the depth which is greater than the territory of material within the silicone. Conse quently, in order that it guarantees that all ions are ne arly injected within the territory of material the thickne ss is selected so that the ion energy produces the nee dle depth corresponding to into the silicone less than t he thickness of the territory of material. (The ion need le depth into the silicone as the function of the ion ene rgy is the ra. It can look out in the " microelectronics p rocessing of the call call laser and device design " 150 through 153 page.

예를 들어, 60keV 이하의 주입 에너지(0.07㎛보다 작거나 같은 깊이로 실리콘을 관통하는 비스 이온의 90퍼센트가 되는 비소 이온 에너지)를 이용하여 0.07㎛의 평균 두께를 가진 코발트 실리사이드의 여역내로의 비소 이온의 주입은 거의 모든 비소 이온이 코발트 실리사이드내로 주입되는 것을 보장한다. 유사하게, 10keV 이하의 주입 에너지(0.08㎛ 이하의 깊이로 실리콘을 관통하는 붕소 이온의 90퍼센트가 되는 붕소 이온 에너지)를 이용하여, 0.08㎛의 평균 둑께를 가진 티타늄 실리사이드의 영역내로 붕소 이온을 주입하면 거의 모든 붕소 이온의 티타늄 실리사이드로 주입되는 것을 보장한다.

For example, the injection of the arsenic ion into the women reverse of the cobalt silicide having the averag e thickness of 0.07㎛ using the implant energy (the ars enic ion energy in which it becomes 90 percent of the bis ion passing through the silicone through the depth which is smaller than 0.07㎛ or thes same) less than 60 keV guarantees that all arsenic ions are injected within the cobalt silicide. Similarly, it guarantees that the dom ain is injected to the titanium silicide of all boron ions if the boron ion is injected using the implant energy (the boron ion energy in which it becomes 90 percent of the boron ion passing through the silicone through the dept h less than 0.08㎛) less than 10keV within the domain of the titanium silicide having the average bank of 0.08 ㎛.

GF Exhibit 1124 - 1955/2704

본 발명은 또한 원하는 소스/드레인 깊이를 실현하기 위해 기판 가열 동안에 이용될 온도-시간 프로필을 선택하기 위한 반복적(iterative) 기술을 포함하고 있다. 여기서, 상기 물질 영역이 두게는 기판의 도핑 레벨, NA 일대 공지되거나 지정된 것을 가정 한다. 또한 상기 세가지 조건이 만족되었고, 기판 가열의 결과로서 상기 물질 영역/기판 인터페이스에 인접한 기판내의 도펀트 농도가 원하는 Rc를 실현하는데 필요한 (공지된) 최소값인 Co보다 크거나 같은 것으로 가정한다. 처음에, 또한 간편성을 위해, 필수적으로 Tmin보다 크거나 같은 온도 T만이 가열 절차 동안에 사용된다고 가정한다. 만일 변수 X#180#가 상기 물질 영역의 바닥에 대한(확산된) 소스나 드레인내의 점의 수직 위치를 표시하고, T가 시간을 나타내고, D(=D(T))가 기판에서의 도펀트의 확산 계수를 표시하고, Co#180#가 약 10-6 Ω-cm2 이하의 Rc를 산출하는 상기 물질 영역/기판 인터페이스에 인접한 원하는 도펀트 농도를 나타낸다면, C가 공식

The repetitive (iterative) technology which it is to select the temperature-time profile used for the substrate heating in order to realize the source/drain depth in which the invention moreover desires, is contained. Here, it assumes that the thickness is known as the doping level of the substrate, and the NA area or the territory of material is designated. Moreover, three conditions was satisfied and with it is greater than the Co realizing the Rc in which the dopant concentration within the substrate adjacent to the territory of material / plate interface desires as the result of the substrate heating but is the necessary (it is known) minimum value or it is the same it assumes. First, moreover, it assumes that it is used for simplicity only the temperature T which is obligatorily greater than the Tmin or thes same for the heating process. C is the equation the desired dopant concentration in which the Co´ is adjacent to the territory of material / plate interface producing the Rc less than about 10 - 6 Ω- cm 2 is shown the variable X´ indicates the perpendicular position of the point within the source about the bottom surface (it is diffused) of the territory of material or the drain and T shows time and D (=D(T)) indicates the diffusion coefficient of the dopant at the substrate.

에 의해 잘 근사된다는 것이 결정되었다. 여기서 erfc는 상보에러 함수이다. X#180#가 X(상기 물질 영역의 바닥에 비교한 소스나 드레인의 원하는 깊이)와 같아지는 소스나 드레인의 바닥에서, C(X, Γ)는 필수적으로 NA와 동일하며, 그러므로 공식(1)로 부터,

It was determined that it was due to and the well was approximated. Here, the erfc is the complementary error function. From the equation (1) the obligatorily C (X, Γ) is identical with NA in the bottom surface of the source in which the X´ becomes same with X (the desired depth of the source compared in the bottom surface of the territory of material or the drain) or the drain.

이다.

It is.

공식(2)의 오른쪽이 공지된 양이기 때문에, 공식(2)에서 상보에러 함수의 독립변수(argument)가 알려지며, 즉 예를 들어 erfc 함수의 테이블로 부터 쉽게 결정된다(엠.아브라모위쯔와 아이.에디.세건에 의해 출판된 #8220#수학적 함수의 핸드북 #8221#에서 왈터 고쯔찌를 참조하라). 그러나 X는 알려져 있다. 또한 D는 필수적으로 온도의 함수이며, 단일 온도만이 가열 절차동안에 사용되기 때문에 D도 또한 낮게되며, 단일 온도 T에 대응하는 D의 값은 예를 들어, 테이블(제이.씨.씨.쯔아이의 상기 참조 논문을 참조)로 부터 쉽게 결정된다. 그러므로, erfc 함수의 독립 변수의 값이 알려지고, X와 D의 값이 알려졌기 때문에 Γ(가열시간)의 값은 쉽게 추론할 수 있다. 만일(제어 샘플의 바닥과 비교하여) 소스나 드레인의 생성 깊이가(예를 들어 SIMS 기술을 통해 결정될때) 원하는 깊이가 아니면 가열 시간 및 가열온도가 변경된다.

The M(***. Larmor and I the right of the equation (2) is known amount is determined from in other words, for example, the table of the erfc function it is the amount in which and therefore the independent variable (argument) of the complementary error function is known in the equation (2). Eddy. In the handbook " published by the force gun of the " mathematical function, but X is known because of referring to the Walter Gozdz fishing float. Moreover, the value of the D, which corresponds to the monothermal T the obligatorily D is the function of the temperature and D is low because it is used only the monothermal for the heating process. For example, the table (J. It is easily the reference paper of the CC. I determined from the reference). Therefore, the value of the independent variable of the erfc function becomes known and the value of Γ (the heating time) easily can reason because the value of D and X became known. If it is not depth in which the production depth (it is determined through the SIMS technology for example) of the if (it compares with the bottom surface of the control sample) source or the drain desires, the heating time and heating temperature are changed.

만일 대응하는 다수의 시간 간격 Γ1, Γ2…Γn에 대해 다수의 가열온도 T1, T2…Tn을 사용하는 것이 필요하다면, C는

C it is requisite about the multiple time interval Γ 1 s which the if corresponds, and Γ 2 … Γ n to use the multiple heating temperature T 1 s, and T 2 … T n .

의해 잘 근사된다. 여기서 D1, D2, …Dn는 온도 T1, T2, …Tn

It is according to and it is approximated to the well.

GF Exhibit 1124 - 1956/2704

에서 기판내의 도펀트의 확산 계수를 표시한다. 그러므로, C가 NA와 동일한, 즉 X#180#=X인 소스나 드레인의 바닥에서,

Here, in D 1 , D 2 , … D n is the temperature T 1 , T 2 , and … T n , the diffusion coefficient of the dopant with in the substrate is indicated. Therefore, in the bottom surface of the source in which C is identical with NA an d which is in other words, the X′=X or the drain

이된다. 전술한 바와 같이, 공식(4)의 오른쪽은 알려져 있고, 그러므로 공식(4)에서 erfc 함수의 독립변수는 쉽게 결정된다. 또한 X는 알려져 있고, T1, T2, …Tn가 지정된 것으로 가정하면 D1, D2, …Dn도 또한 쉽게 결정된다. 그러므로 공식(4)를 만족하는 Γ1, Γ2, …Γn의 값이 쉽게 선택된다. 만일 Γ가 원하는 소스/드레인 깊이를 산출하지 못하면, 반복적 절차에 따라, Γ 및 T가 변경된다.

It is ***. As described above, the right of the equation (4) is known and the independent variable of the erfc function is therefore easily determined on the equation (4). Moreover, X is known and if it assumes th at T 1 , T 2 , and … T n are designated, D 1 , D 2 , an d … D n are moreover easily determined. Therefore, Γ 1 , satisfied the equation (4) Γ 2 , and the value of … Γ n are easily selected. If the source/drain depth in whic h Γ desires is unable to be produced , Γ and T are acco rding to procedure changed.

상기 반복적 기술을 이용하여, 1#215#1016cm-3의 도핑레벨을 가진 P형 실리콘 기판을 가열하는 단계와 800℃의 온도로 130분 동안 상기 비소가 주입된 코발트 실리사이드 영역을 지탱하는 단계는 0.15㎛와 동일한 깊이(코발트 실리사이드의 상부 표면에 대하여)를 가진 소스나 드레인을 산출한다는 것이 알려졌다. 유사하게, 1#215#1017cm-3의 도핑 레벨을 가진 n형 실리콘 기판을 가열하는 단계와 124분 동안 800℃의 온도로 상기 붕소가 주입된 티타늄 실리사이드 영역을 지탱하는 단계는 0.2㎛와 동일한 깊이(티타늄 실리사이드의 상부 표면에 대하여)를 가진 소스나 드레인을 산출한다는 것도 알려져 있다.

The source having the depth (about the top surface of the cobalt silicide) in which the step and the step of su pporting the cobalt silicide domain in which arsenic was injected as the temperature of 800℃ for 130 minutes w ere identical with 0.15㎛ of heating up the P-sub havin g the doping level of 1× 10 16 cm - 3 or the to produc e the drain thing was known using the iterative techniq ue. Similarly, it is known that the step and the step of supporting the titanium silicide region in which boron is injected to the temperature of 800℃ for 124 minutes pr oduce the source or the drain having the same depth (about the top surface of the titanium silicide) as 0.2㎛ of heating up the n-type silicon substrate having the d oping level of 1× 10 17 cm - 3 .

본 발명의 보다 완전한 이해를 위한 교육학적 도움으로서 n채널 MOS IC 및 CMOS(상보 금속 산화물 반도체) IC의 제조를 위한 본 발명의 소자 제조 방법의 용융이 이하에서 기술되게 된다(간략하게 하기 위해 완전히 통상적인 몇몇 단계는 생략된다).

Hereinafter the melting of the element manufacture method of the invention for the manufacture of the N-channel Metal Oxide Semiconductor IC and CMOS (com plementary metal oxide semiconductor) IC are describe d as the pedagogy help for the complete understanding of the invention (brevis breviterLat, it is to do and the normal some step is completely omitted).

제1도 내지 제8도를 참조하면, 예를 들어 종래의 산화 기술을 이용하여, P형 실리콘 기판(10)상에 FOX(20)(비교적 두꺼운 SiO2층)을 형성함으로써 본 발명의 한 실시예에 따라 n채널 MOS IC가 제조된다. 기판(10)에서 P형 도펀트의 도핑 레벨은 예를 들어 1#215#1015cm-3이다. 또한 FOX(20)의 두께는 예를 들어 0.35㎛이다.

The first the N-channel Metal Oxide Semiconductor IC is manufactured with reference to the inland eighth dra wing using for example, the conventional oxidation tech nology according to one embodiment of the invention b y forming the FOX (20) (the SiO 2 layer which is relativ ely thick) on the P-sub (10). In the substrate (10), the doping level of the p-dopant is for example, 1× 10 15 c m - 3 . Moreover, the thickness of the FOX (20) is for example, 0.35㎛.

이제 FOX(20)는 MOSFET가 형성될, 여기서는 GASAD (gate-and-source-and-drain)으로 불리는 기판 표면의 영역(30)을 노출시키기 위해 예를 들어, 석판 인쇄술 및 반응 이온 에칭(RIE)기술을 이용하여 선택적으로 에칭된다. 예를 들어, 0.15㎛의 두께를 가진 GOX(40)(비교적 얇은 SiO2층)는 예를 들어 종래의 산화 기술을 이용하여 GASAD 영역(30)의 표면상에 형성된다.

Now, it is etched at the selectively using for example, lithography and reactive ion etching (RIE) technology t he domain (30) of the substrate surface called here, th e GASAD (gate-and-source-and-drain) in which the FO X (20) MOSFET is formed is exposed. For example, the GOX (40) (the SiO 2 layer which is relatively thin) havin g the thickness of 0.15㎛ is formed on the surface of th e GASAD domain (30) using for example, the conventio nal oxidation technology.

MOSFET의 게이트 전극은 GASAD 영역(30) 뿐만 아니라 FOX(20)상에도 다결정 실리콘(이후 폴리실리콘)의 층(50)을 초기에 침착시킴으로써 형성된다. 침착은 예를 들어 종래의 저

The gate electrode of MOSFET is formed by sinking the layer (50) of the poly-crystal silicon (then, the poly-sili con) into the initial on not only the GASAD domain (30)

GF Exhibit 1124 - 1957/2704

압 화학적 증기 침착(LPCVD) 기술을 이용하여 실행되며, 침착된 폴리실리콘의 두께는 예를 들어 0.3㎛가 된다. 침착후에, 폴리실리콘은 예를 들어 1#215#1015cm-2의 주입량(implant dose)과 80kev의 이온 에너지를 이용하여, 폴리실리콘에 비소와 같은 n형 도펀트를 주입함으로써 전기적 전도성으로 만들어진다.

but also the FOX (20). The deposition is performed using for example, the conventional low pressure chemical vapour deposition (LPCVD) technology and for example, 0.3㎛ becomes the deposited thickness of the poly-silicon. The poly-silicon is made as the electrical conductivity after the deposition using for example, the injection amount (implant dose) of 1× 10 15 cm - 2 and ion energy of 80kev by injecting the n-type dopant like arsenic into the poly-silicon.

침착된 전기적 전도성의 폴리실리콘(50)은 이제 제4도에 도시된 바와 같이, 간각이 GASAD 영역(30)위에 있는 폴리실리콘 구조를 형성하기 위해 종래의 RIE 기술을 이용하여 패턴된다. 상기 구조의 측벽은 대응하는 GASAD 영역이 표면에 직각인 면에 비하여 각도 #945#(제4도 참조)를 형성하는데, 이것은 +15#176# 보다 작거나 같으며, 0도가 되는것이 바람직하다(제4도에 도시한 폴리실리콘 구조의 좌측벽에 대해, 각도 X는 수직으로 부터 시계 방향으로 측정될때 포지티브가 된다. 한편 우측벽에 대해서는 이 각도가 반시계 방향으로 측정될때 포지티브다 된다). 측벽 각도에 관한 관계는 이하에서 논의되는 바와 같이 실리콘 이산화물 측벽 스페이서(55)의 형성과 관련하여 매우 중요하다.

So that the liver angle form the polysilicon structure of having on the GASAD domain (30), the deposited poly-silicon (50) of the electrical conductivity is patterned on the now as shown in Figure 4 using the conventional RIE technology. The GASAD domain in which the sidewall of the structure corresponds forms the angle α (the fourth is the reference) on the surface in comparison with the side which is the right angle. This is smaller than the +15° or it is the same and when the angle X is clockwise measured from the perpendicularity, it is positive about the left side wall of the polysilicon structure of showing in the be desirable or figure the fourth that figure 0 is. In the meantime, as when this angle is counterclockwise measured about the right side wall, it becomes as positive hereinafter the relation about the side wall angle been discussed it is important in connection with the formation of the silicon dioxide side wall spacer (55).

이하에서 논의되는 소자 제조 절차는 결과적으로 금속 실리사이드 영역을 각각의 MOSFET의 소스, 드레인 및 게이트 전극으로 병합시킨다. 게이트 전극에서의 금속실리사이드 영역과 소스 및 드레인에서의 금속 실리사이드 영역 사이의 전기적 접촉을 배제하기 위해, 각 게이트 전극의 폴리실리콘 부분은 각 폴리실리콘 측벽을 커버링하는 실리콘 이산화물 측벽 스페이서(55)(제4도 참조)를 포함하도록 형성된다. 이것은 예를 들어 FOX의 상부 및 측벽 표면과 GASAD 영역의 노출된 표면상에 뿐만 아니라 폴리실리콘 구조의 상부 및 측벽 표면상에 테트라에틸오소실리케이트(TEOS)와 같은 실리콘과 산소 함유 물질의 층을 침착 시킴으로써 실현된다. TEOS의 침착은 예를 들어 종래의 LPCVD 기술을 이용하여 쉽게 실행되며, TEOS의 두께는 예를 들어 0.1㎛이다. 침착이 이루어진 후에, TEOS는 TEOS를 농후하게 하고 효과적으로 실리콘 이산화물과 같은 물질로 변환시키기 위해 스팀 대기에서 20분동안 900℃로 가열되는 것이 바람직하다. 이때 TEOS는 폴리실리콘 구조의 상부 표면뿐만 아니라 FOX 및 GASAD 표면으로 부터 TEOS를 제거하기 위해 예를 들어 CHF3 및 O2의 에천트(etchant) 환경에서 예를 들어 RIE를 이용하여 이동방향으로 에칭된다. 이 에칭 절차 이후에, 예를 들어 0.06㎛의 두께를 가진 농후하게 된 TEOS의 층이 측벽 각도가 전술한 요구를 만족하도록 제공되어 폴리실리콘 구조의 측벽상에 남아 있게 된다.

Hereinafter, the consequently the device manufacture procedure of being discussed incorporates the metal silicide domain to the source of each MOSFET, and the drain and gate electrode. In order that the electrical contact of the metal silicide between area at the metal silicide domain at the gate electrode and source and drain are excluded drain are formed in order to include the silicon dioxide side wall spacer (55) (the fourth is the reference) in which the polysilicon part of each gate electrode covers each polysilicon side wall. By sinking the layer of the silicone like the taraethylothosilicate (TEOS) and oxygen containing material on the upper portion and side wall surface of the polysilicon structure besides this is realized on for example, the exposed surface of the upper portion of FOX and side wall surface and GASAD domain. The deposition of TEOS is easily performed using for example, the conventional LPCVD technology and the thickness of TEOS is for example, 0.1㎛. After the deposition is made it is the be desirable that the material is heated in the steam atmosphere for 20 minutes by 900℃ so that it make TEOS strong and TEOS effectively change to the material like the silicon dioxide. Then, it is etched at the moving direction in for example, the etchant environment of O 2 and CHF 3 using for example, RIE so that TEOS remove TEOS from not only the top surface of the polysilicon structure but also FOX and GASAD surface. The layer of thick TEOS having for example, the thickness of 0.06㎛ is provided in order to be satisfied the demand in which the side wall angle describes in the above and , the layer remains after this etching procedure on the sidewall of the polysilicon structure.

측벽 스페이서(55)의 형성 이후에, 티타늄과 같은 금속 실리사이드를 형성하기 위해 실리콘과 반응할 수 있는 금속층이 각 폴리실리콘 구조의 상부 표면과, 측벽 스페이서(55)의 표면과, G

In order to form the metal silicide like titanium, the metallic layer reacting to the silicone is deposited after the formation of the side wall spacer (55) on the upper

GF Exhibit 1124 - 1958/2704

ASAD 영역의 노출된 표면(소스와 드레인 형성될 곳) 및 FOX (20)의 상부 및 측벽 표면상에 침착된다. 이 침착은 예를 들어, 종래의 스퍼터링 기술을 이용하여 실현되며, 침착된 티타늄의 두께는 예를 들어, 0.1㎛이다. 침착 이후에, 티타늄으로 커버된 실리콘 기판은 종래의 RTA 기술을 이용하여 약 1분동안 약 600℃의 온도로 질소(N2) 환경에서 가열된다. 티타늄 층이 실리콘과 접촉하는 곳, 즉 GASAD 영역의 표면 뿐만 아니라 폴리실리콘 구조의 상부 표면상에서, 이 가열 절차는 TiN, Ti 및 Ti siy의 연속한 층의 형성을 초래하게 되는데, 여기서 y#8804# 2이다. 대조적으로, 침착된 티타늄 층이 실리콘 이산화물과 접촉하는 곳, 즉 FOX 및 측벽 스페이서의 표면에서, 상기 가열절차는 TiN 및 Ti의 연속한 층의 형성을 야기하게 된다.

portion of exposed surface (the place formed with sour ce and drain) of the surface of the top surface of each polysilicon structure and side wall spacer (55) and GAS AD domain and FOX (20) and side wall surface. This de position is realized using for example, the conventional sputtering technique and the deposited thickness of th e titanium is for example, 0.1㎛. The temperature of ab out 600℃ is heated by the silicon substrate covered wi th titanium after the deposition using the conventional RTA technology for about 1 minute in the nitrogen (N(S B)2(/SB)) environment. This heating process causes th e TiN, and the formation of the consecutive layer of th e Ti and Tisiy on the place, where the titanium layer co ntacts with the silicone in other words, the top surface of not only the surface of the GASAD domain but also t he polysilicon structure. It the here is the y≤2. Contras tively, the heating process causes the formation of the consecutive layer of the TiN and Ti on the surface of t he place, where the deposited titanium layer contacts the silicon dioxide in other words, FOX and side wall sp acer.

TiSiy(y#8804#2)가 아닌 TiN 및 Ti층은 90℃의 온도로 가열된 H2SO4 : H2O2(1 : 1)의 용액과 같은 선택적 습식 에천트를 사용하여 에칭된다. 폴리실리콘 구조의 상부 표면과 GASA D 영역의 노출된 표면을 커버링하는 남아있는 TiSiy(y#8804 #2)는 이제 종래의 RTA 기술을 이용하여 예를 들어 20초동안 800℃의 온도로 질소 환경에서 TiSiy로 커버된 실리콘 기판을 가열함으로써(폴리실리콘 구조 및 실리콘 기판에서) 아래에 있는 실리콘과 반응하게 된다. 그 결과 TiSi2 함유 영역(60, 70)(제5도 참조)이 폴리실리콘 주조의 반대측에 형성되어 수직으로 정렬되고 TiSi2 함유 영역(80)은 폴리실리콘 구조의 정상부에 형성되는데, 이와 같은 영역은 약 0.08㎛의 동일한 TiSi2의 두께를 갖는다(각각의 이와 같은 영역은 또한 통상적으로 약 0.01㎛의 두께를 갖고 TiSi2위에 있는 TiN층(양호한 전기적 전도체)을 포함한다).

The TiN and the Ti layer which is not TiSiy (y≤2) are etched using the optional wet etchant like the service of H 2 SO 4 : H 2 O 2 (1 : 1) which the temperature of 90℃ is heated. By the nitrogen ambient heating the sili con substrate covered with the TiSiy using the conven tional RTA technology for for example, 20 second with the temperature of 800℃ (in the polysilicon structure a nd silicon substrate) the TiSiy (y≤2) which covers the top surface of the polysilicon structure and the expose d surface of the GASAD domain remaining now reacts w ith the silicone which is beneath have. Consequently, t he TiSi 2 containing domain (60, 70) (the fifth is the re ference) is formed in the opposite side of the poly-silic on casting and it is arranged in the perpendicularly and the TiSi 2 containing domain (80) is formed in the top o f the polysilicon structure. This kind of domain has the thickness of the same TiSi 2 of about 0.08㎛ (generally the domain like each this moreover has the thickness o f about 0.01㎛ and the TiN layer (the good electrically conducting body) having on the TiSi 2 is included).

n+형 소스 및 드레인을 형성하기 위해, 하나 혹은 그 이상의 도펀트, 즉 비소 이온이나 인 이온이 TiSi2 함유 영역(60, 70)내로 주입된다. 주입량은 물론 전술한 세가지 조건을 만족하도록 선택된다. 또한 이온 에너지도 거의 모든 이온이 영역(60, 70)내로 주입되고 아래에 놓인 실리콘내로는 주입되지 않도록 선택된다.

In order that the n + type source and drain are formed one or the dopant described in the above, in other wor ds, the arsenic ion or the phosphor ion is injected withi n TiSi 2 containing domains (60, 70). It is selected in o rder to be satisfied above-described three conditions a s well as the injection amount. Moreover, the all ions ar e injected within domains (60, 70) and the ion energy i s beneath puts silicone is selected in order not to be in jected within the silicone in which.

이온 주입 이후에, 인터레벨 유전체(90)(제6도 참조)가 기판상에 침착된다. 이와 같은 유용한 인터레벨 유전체는 예를 들어, 0.2㎛의 두께를 가진 도핑되지 않은 TEOS와 약 0.8㎛의 두께를 가진 인으로 도핑된 TEOS의 잇따른 층을 포함한다.

The interlevel dielectric (90) (the sixth is the reference) is deposited after the ion implantation on th e substrate. This kind of the interlevel dielectric which i s useful includes undoped TEOS having for example, th e thickness of 0.2㎛ and the layer following of TEOS do ped to the phosphorus having the thickness of about 0.8㎛.

침착된 인터레벨 유전체(9)의 상부 표면은 통상적으로 비평면이다(일반적으로 후속 처리동안 바람직하지 못하다). 인터레벨 유전체(90)를 흐르도록 유도하고 그래서 표면 평면성을 실현하고 또한 티타늄 실리사이드로 커버된 소스 및 드레인(100, 1

The generally the deposited top surface of the interlevel dielectric (9) is the non-planar (generally, it c annot for the next treatment with the be desirable pap er). In order that it induces in order to flow the interlev

GF Exhibit 1124 - 1959/2704

10)(제7도 참조)을 형성하도록 TiSi2 함유 영역(60, 70)으로부터 아래에 놓인 실리콘내로 주입 도펀트를 확산시키기 위해, 기판이 가열된다. 전술한 바와 같이, 가열 절차의 온도-시간 프로필은 약 0.2㎛ 이하의 깊이를 가진 소스 및 드레인을 산출하도록 선택된다.

el dielectric (90) and , so the injection dopant is diffused within the silicone which is beneath puts from TiSi 2 containing domains (60, 70) in order to realize the surface planarity and form the source and the covered drain (100, 110) (the seventh is the reference) into moreover, the titanium silicide the substrate is heated. As described above, the source are selected in order to produce the source and the drain in which the temperature-time profile of the heating process has the depth less than about 0.2㎛.

소스 및 드레인 형성 이후에, 인터레벨 유전체는 소스와 드레인 및 게이트 전극으로 경유 구멍을 개방하도록(종래 기술을 이용하여) 패턴된다. 이제 물질층(120, 130, 140)(제8도 참조)이 기판상에 침착되는데 그래서, 알루미늄과 실리콘의(바람직하지 못한) 상호 확산에 대한 장벽으로서 작동하도록 소스와 드레인 및 게이트 전극으로 각각 뻗은 경유 구멍내로 침착되게 된다. 이들 층은 예를 들어, 10퍼센트(중량으로)의 티타늄과 90퍼센트의 텅스텐 합성물을 포함하며 예를 들어 0.1㎛의 두께를 갖는다.

It is patterned after the source and drain formation so that the interlevel dielectric opens the via hole to source and drain and gate electrode (using the prior art). Now, the material layer (120, 130, 140) (the eighth is the reference) is deposited on the substrate but it is deposited to the so within the via hole spreading toward source and drain and gate electrode in order to operate as the obstacle about the interdiffusion of aluminum and silicone (it cannot with the be desirable paper). These layers has for example, the titanium of 10 percent (to the weight) and for example, the thickness of 0.1㎛ the tungsten synthesized material of 90 percent is included.

이제, 예를 들어 1㎛의 두께를 가진 알루미늄 층이 경유 구멍내의 장벽층(120, 130, 140) 뿐만 아니라 인터레벨 유전체(90) 상에도 참착된다. 침착후 계속해서, 금속 접촉 패드에서 중단되는 상호 접속 알루미늄 런너(runner)(150, 160, 170)를 형성하기 위해 종래의 기술을 이용하여 알루미늄층이 패턴된다.

Now, for example, the aluminum layer having the thickness of 1㎛ is settled down on not only barriers (120, 130, 140) within the via hole but also the interlevel dielectric (90). In order to form interconnection aluminum runner (runner) (150, 160, 170) and then interrupted in the metal contact pad after the deposition, the aluminum layer is patterned using the conventional technology.

n채널 MOS IC는 통상적인 일련의 단계를 통해 완성되는데, 통상적으로 습기 및 기계적 손상에 대비한 장벽을 형성하기 위해 IC상에 실리콘 질화물 층을 침착하는 단계를 포함한다.

The N-channel Metal Oxide Semiconductor IC comprises the step of being compose the silicon nitride layer on IC the obstacle which generally compares for moisture and mechanical damage is formed it is completed through normal a series of step.

이제 제9도 내지 제17도를 참조하면, 종래기술을 이용하여 P+형 실리콘 기판(200)상에 P형 실리콘층(210)(제9도 참조)을 에피택셜 성장시킴으로써 본 발명의 제2실시예에 따라 CMOS IC가 제조된다. 기판(200)의 도핑 레벨은 예를 들어 1018cm-3이며, 에피택셜 성장된 층(210)의 도핑 레벨은 예를 들어 1015cm-2이다. 또한, 에피택셜 성장된 층(210)의 두께는 예를 들어 5㎛이다.

Referring now to the ninth is the inland seventeenth drawing, according to the second preferred embodiment of the present invention, the CMOS IC is manufactured by making the P-type silicon layer (210) (the ninth is the reference) using the prior art on the P+ type silicon substrate (200) with epitaxial growth. The doping level of the substrate (200), for example, the doping level of 10 18 cm - 3 , the layer (210) which epitaxially grows is for example, 10 15 cm - 2 . Moreover, the thickness of the layer (210) which epitaxially grows is for example, 5㎛.

1984년 3월 13일 엘.씨.파릴로와 알.에스.페인에게 특허된 미합중국 제 4,435,896호에 기술된 바와 같은 소위 2중 튜브 공정을 이용하여 에피택셜 성장층(210)에 인접한 n튜브 및 P튜브(240, 250)가 형성된다. 즉 예를 들어 0.1㎛의 두께를 가진

1984 year March 13 LC. Parrillo. and RS. The n tube and P tubes (240, 250) adjacent to the Epitaxial growth layer (210) among the patented so-called 2 like being described in US4,435,896 A using the tube processing

GF Exhibit 1124 - 1960/2704

실리콘 질화물층(220)(제10도 참조)이 통상적인 침착 기술을 이용하여 상기 층(210)의 상부 표면에 처음에 침착된다. 종래의 석판 인쇄술 및 RIE 기술이 실리콘 질화물층(220)의 일부분을 제거하고, 그러므로 n튜브(240)가 될 실리콘 표면을 노출시키는데 이용된다. 이제 도우너 이온, 즉 인 이온과 비소 이온이 상기 층(210)(층(210)의 노출되지 않는 실리콘을 주입으로부터 차폐하도록 작용하는 잔여 실리콘 질화물층)의 노출된 실리콘 표면내로 주입되는데, 인과 비소 이온 모두에 대한 주입량 및 에너지는 예를 들어 각각 2#215#1012cm-2와 100keV이다. 다음에, n튜브의 표면상에 약 0.4㎛의 두께를 가진 실리콘 이산화물의 층(230)(제10도 참조)을 형성하기 위해, 예를 들어 950℃의 온도로 140분의 대응하는 가열 시간동안 스팀 함유 환경에서 실리콘 기판이 가열된다.

are formed to the pain. That is, for example, it at first time is sunk in the top surface of the layer (210) using the deposition technology in which the silicon nitride layer (220) (the tenth is the reference) having the thickness of 0.1㎛ is normal. The conventional lithography and RIE technology remove one part of the silicon nitride layer (220) and it is therefore used to expose the surface of silicon in which the n tube (240) is. Now, the donor ion, in other words, the phosphor ion and arsenic ion are injected within the exposed surface of silicon of the layer (210) (the residual silicon nitride layer which acts in order to shield the silicone which is not exposed of the layer (210) from injection). For example the injection amount about the phosphorus and arsenic ion every one and energy is 2× 10 12 cm - 2 and 100keV. Next, in order that the layer (230) (the tenth is the reference) of the silicon dioxide having the thickness of about 0.4㎛ is formed on the surface of the n tube the silicon substrate is heated by for example, the temperature of 950℃ for the heating time to correspond to of 140 minutes in the steam containing environment.

이제 실리콘 질화물의 층(220)이 뜨거운 H3Po4와 같은 습식 에천트로 에칭되고, 액셉터 이온 즉 붕소 이온이 P튜브(250)가 될 노출된 실리콘 표면으로 주입된다(실리콘 이산화물층(230)은 n튜브(240)을 주입으로 부터 차폐한다). 만일 붕소 이온이 사용되면, 주입량 및 대응하는 주입 에너지는 예를 들어 각각 2#215#1012cm-2 및 50keV이다. 다음에, 실리콘 기판은 붕소 이온 및 인 이온을 약 2㎛의 깊이까지 상기 층(210) 내로 확산시켜 n튜브(240) 및 p튜브(250)(제11도 참조) 모두를 형성시키기 위해, 예를 들어 1150℃의 온도로 120분의 대응하는 시간 주기동안 질소(N2) 환경에서 가열된다.

Now, it is etched at the wet etchant like H 3 Po 4 in which the layer (220) of the silicon nitride is hot and if it is injected to the exposed surface of silicon (the silicon dioxide layer (230) shields the n tube (240) from injection) in which for the acceptor ion, in other words, the boron ion, P tube (250) is the boron ion is used , for example the implant energy corresponding with the injection amount is 2× 10 12 cm - 2 and 50keV. Next, in order that the boron ion and phosphor ion are diffused to the depth of about 2㎛ within the layer (210) and the silicon substrate forms both the n tube (240) and p tube (250) (the eleventh is the reference) for example, the temperature of 1150℃ is heated for the time period corresponding to of 120 minutes in the nitrogen (N(SB)2(/SB)) environment.

n튜브(240)를 커버링하는 실리콘 이산화물층(230)은 H2D : HF(7 : 1)와 같은 습식 에천트로 에칭된다. 이제 CMOS IC에서 FOX로서 작용하는 예를 들어 0.4㎛의 두께를 가진 실리콘 이산화물의 비교적 두꺼운 층(260)(제12도 참조)이 에피택셜 성장층(210)의 (이제 완전히 노출된) 상부 표면상에 형성된다. 이것을 예를 들어 850℃의 온도로 25분의 대응하는 가열 시간동은 고압스팀 함유 대기, 즉 25기압의 압력을 나타내는 스팀 함유 대기에서 실리콘 기판을 가열함으로써 실현된다.

The silicon dioxide layer (230) covering the n tube (240) is etched at the wet etchant like H 2 D : HF (7 : 1). Now, in the CMOS IC, the layer (260) (the twelfth is the reference) which is relatively thick of the silicon dioxide having the thickness of 0.4㎛ acting as FOX is formed on (it is now completely exposed) top surface of the Epitaxial growth layer (210). Since the steam containing atmosphere showing the high pressure steam containing atmosphere, in other words, the pressure of 25 atmospheric pressure the heating time copper of 25 minutes corresponding to heats the silicon substrate with for example, the temperature of 850℃ it is this realized.

실리콘 이산화물의 비교적 두꺼운 층(260)은, n채널 MOSFET가 형성된 P튜브(250)과 표면상의 GASAD 영역(270)을 노출시키고, P채널 MOSFET가 형성될 n튜브(240)의 표면상의 GASAD 영역(400)을 노출시키기 위해 종래의 기술을 이용하여 패턴된다. 다음에, 실리콘 기판은 GASAD 영역(270)의 표면상에 실리콘 이산화물의 층(280)을 형성하고 GASAD 영역(400)의 표면상에 실리콘 이산화물의 층(410)을 형성하기 위해 900℃의 온도로 27분의 대응하는 시간 주기동안 가열되게 되는데, 이들 층(280, 410)은 약 0.0125㎛의 두께를 가지며, n채널 및 P채널 MOSFET의 GOX로서 작용한다.

The layer (260) which is relatively thick of the silicon dioxide exposes the GASAD domain (270) on P tube (250) and the surface in which the n channel type MOSFET is formed and it is patterned using the conventional technology it exposes the GASAD domain (400) on the surface of the n tube (240) in which the P-ch MOSFET is formed. Next, in order to the silicon substrate form the layer (280) of the silicon dioxide on the surface of the GASAD domain (270) and form the layer (410) of the silicon dioxide on the surface of the GASAD domain (400), the surface is heated by the temperature of 900℃ for the time period corresponding to of 27 minutes. These layers (280, 410) have the thickness of about 0.012

GF Exhibit 1124 - 1961/2704

5㎛ and the temperature acts as GOX of the P-ch MOS FET and n channel.

n채널 및 P채널 MOSFET의 게이트 전극은 처음에, FOX(260) 뿐만 아니라 GASAD 영역(270, 400)상에 예를 들어 0.3㎛의 두께를 가진 폴리실리콘 층을 침착시킴으로써 형성되며, 포토레지스트가 기판상에 침착되어 n튜브(240)에 대응하는 기판 표면을 노출시키기 위해 패턴된다. 이제 액셉터 이온, 즉 붕소 이온이 n튜브 위에 놓인 폴리실리콘내로 주입되는데 레지스트는 P튜브 위에 놓인 폴리실리콘을 주입으로 부터 차폐한다. 주입량 및 주입 에너지는 예를 들어, 각각 1#215#1015cm-2와 30keV이다. 이 레지스트는 벗겨지고, 제2레지스트가 기판상에 침착되어 P튜브(250)에 대응하는 기판 표면을 노출시키기 위해 패턴된다. 이제 도우너 이온, 즉 비소 이온이 P튜브(250) 위에 놓인 폴리실리콘내로 주입되는데, 제2레지스트는 n튜브(240) 위에 놓인 폴리실리콘을 제2주입으로 부터 차폐한다. 도우너 이온에 대응하는 주입량 및 주입 에너지는 예를 들어, 각각 1#215#1015cm-2와 30keV이다. 이제 제2레지스트는 벗겨지고, 기판은, 예를 들어 900℃의 온도로 30분의 대응하는 시간 주기동안 질소(N2) 디기에서 가열된다. 결과적으로, 주입된 도펀트가 폴리실리콘내로 확산되어, n튜브(240)위에 놓인 폴리실리콘은 P형 전도성이 되고, P튜브(250)위에 놓인 폴리실리콘은 n형 전도성이 된다.

By sinking the polysilicon layer having for example, the thickness of 0.3㎛ on not only the FOX (260) but also G ASAD domains (270, 400) at first time the gate electro de of the P-ch MOSFET and n channel is formed and so that the photoresist is deposited on the substrate and the substrate surface corresponding to the n tube (24 0) be exposed, it is patterned. Now, it is injected withi n the poly-silicon in which the acceptor ion, in other w ords, the boron ion is puts on the n tube but the poly- silicon in which the resist is puts on P tube is shielded f rom injection. For example the injection amount and im plant energy are 1× 10 15 cm - 2 and 30keV. This resis t comes off and so that the second resist is deposited on the substrate and the substrate surface correspondi ng to P tube (250) be exposed, it is patterned. Now, th e donor ion, in other words, the arsenic ion is injected within the poly-silicon which is puts on P tube (250). T he poly-silicon in which the second resist is puts on th e n tube (240) is shielded from the second injection. Fo r example the injection amount and the implant energy corresponding to the donor ion are 1× 10 15 cm - 2 an d 30keV. Now, the second resist comes off and the sub strate is heated by for example, the temperature of 90 0℃ for the time period corresponding to of 30 minutes i n the nitrogen (N(SB)2(/SB)) di. Consequently, the inje cted dopant is diffused within the poly-silicon and in th e poly-silicon which is puts on the n tube (240), the p- type conductivity is and in the poly-silicon which is put s on P tube (250), the n-type conductivity is.

이제, 침착되고 주입된 폴리실리콘(도한 아래에 놓인 비교적 얇은 실리콘 이산화물층(280, 410)로 마찬가지)이 각각 GAS AD 영역(270, 400)위에 놓인 폴리실리콘 구조(290, 420)(제13도 참조)를 형성하기 위해 전술한 바와 같이 패턴된다. 이 폴리실리콘 구조의 측벽은 위에서 논의된 요구에 부합해야 한다. 또한 전술한 바와 같이 실리콘 이산화물 측벽 스페이서(295, 425)가 각각 폴리실리콘 구조(290, 420)상에 형성된다.

Now, it is patterned on as described above the polysilicon structure (290, 420) (the thirteenth is the r eference) in which poly-silicons (silicon dioxide layers (280, 410) which *** are beneath put and are relativel y thin the likeness) that deposited are injected are put on GASAD domains (270, 400) is formed. It has to coin cide with the demand in which the sidewall of this poly silicon structure is discussed before the upper part. Mo reover, as described above, silicon dioxide side wall spa cers (295, 425) are formed on polysilicon structures (2 90, 420).

이제 코발트와 같이 금속 실리사이드를 형성 하기 위해 실리콘과 반응할 수 있는 금속층이 폴리실리콘구조(290, 410)의 상부 표면과, 측벽 스페이서(295, 425)의 표면과, GASAD 영역의 노출된 표면(소스와 드레인의 형성될 곳)과, FOX(260)의 상부 및 측벽 표면상에 침착된다. 침착된 코발트의 두께는 예를 들어 0.02㎛이다. 침착 이후에, 코발트로 커버된 기판은 450℃의 온도로 90분의 대응하는 시간 주기동안, 감소대기, 즉 대기에서 가열된다. 코발트가 실리콘과 접촉하는 곳, 즉 GASAD 영역과 노출된 표면뿐만 아니라 폴리실리콘 구조의 상부 표면상에서, 이 가열 절차는 코발트 모노실리사이드(CoSi)를 형성하게 된다. 모든 다른 영역에 있어서, 코발트는 반응하지 않은채로 남아 있다. 반응하지 않은 코발트(CoSi가 아님)는 이제 H3Po4 : CH2COOH : HNO3 : H2O(16 : 2 : 1 : 1)과 같은 선택적 습식 에천트를 사용하여 벗겨진다. 다음에, 기판은 예를 들어 700℃의 온도로 30분의 대응하는 시간 주기동안 불활성 대기, 즉 아르곤(Ar) 대기에서 두번째 가열된다. 이 제2가열은 약 0.07㎛의 두께를 가진 코발트 다이실리사이드(CoSi2)를 형성하기 위해 CoSi를 아래에 놓인 실리콘과 반응하도록 한다. 그러므로, CoSi2 함유 영역(300, 310)(제14도 참조)이 각각

Now, the metal silicide is respected like cobalt to do with formation and the metallic layer reacting to the sili cone is deposited on the upper portion of exposed surf ace (the place to be formed of source and drain), of th e surface of the top surface of polysilicon structures (2 90, 410) and side wall spacers (295, 425) and GASAD d omain and FOX (260) and side wall surface. The deposi ted thickness of the cobalt is for example, 0.02㎛. The temperature of 450℃ is heated by the substrate covere d with cobalt after the deposition for the time period c orresponding to of 90 minutes in the reducing atmosph ere, in other words, the atmosphere. This heating proc ess forms the cobalt monosilicide (CoSi) on the place w here cobalt contacts with the silicone, and the top surf ace of not only the surface exposed with other words, the GASAD domain but also the polysilicon structure. A s to dissimilar domains, it remains while cobalt does not react. The cobalt (it is not CoSi) which does not react now comes off using the optional wet etchant like H 3 Po 4 : CH 2 COOH : HNO 3 : H 2 O (16 : 2 : 1 : 1). Nex

GF Exhibit 1124 - 1962/2704

의 폴리실리콘구조(290)와 수직으로 정렬하여 반대측에 형성되고, 함유 영역(320)이 각각의 폴리실리콘구조(290)의 정상부에 형성된다. 유사하게, CoSi2 함유 영역(430, 440)이 각각의 폴리실리콘 구조(420)와 수직으로 정렬하여 반대측에 형성되고, CoSi2 함유 영역(450)이 각각의 폴리실리콘 구조(420)의 정상부에 형성된다.

t, secondly for example, the temperature of 700℃ is he ated by the substrate for the time period correspondin g to of 30 minutes in the inert atmosphere, in other wo rds, the argon (Ar) atmosphere. It reacts with the silic one which is beneath the CoSi puts in order to form th e cobalt disilicide (CoSi(SB)2(/SB)) in which this secon d heating has the thickness of about 0.07㎛. Therefor e, the CoSi 2 containing domain (300, 310) (the fourte enth is the reference) perpendicularly arranges with ea ch polysilicon structure (290) and it is formed in the op posite side and the containing domain (320) is formed i n the top of each polysilicon structure (290). Similarly, it perpendicularly arranges with each polysilicon structu re (420) and CoSi 2 containing domains (430, 440) are formed in the opposite side and the CoSi 2 containing d omain (450) is formed in the top of each polysilicon str ucture (420).

n튜브(240)에서 P채널 MOSFET에 대한 P+형 소스 및 드레인을 형성하기 위해, 예를 들어 1㎛의 두께를 가진 포토레지스트가 기판상에 침착되어, n튜브의 표면을 노출시키도록 패턴된다. 이제 액셉터 이온이 CoSi2 함유 영역(430, 440)내로 주입된다(이 레지스트는 P튜브(250)를 주입으로 부터 차폐한다). 전술한 바와 같이, 주입량은 3가지 조건을 만족하도록 선택되며, 이온 에너지는 거의 모든 이온이 상기 영역(430, 440)내로 주입되도록 선택된다. 이점에 있어서, 액셉터 이온은 얘를 들어 붕소 이온이며, 유용한 주입량은 8#215#1015cm-2이고 유용한 대응하는 주입 에너지는 10keV인 것으로 결정되었다.

In the n tube (240), in order that P + type source and drain about the P-ch MOSFET are formed the photoresi st having for example, the thickness of 1㎛ is deposited on the substrate and it is patterned in order to expose the surface of the n tube. Now, the acceptor ion is inje cted within CoSi 2 containing domains (430, 440) as de scribed above, the injection amount is selected in order to be satisfied three condition and the ion energy is sel ected so that all ions are nearly injected within domain s (430, 440) (A resist shields P tube (250) from injectio n). As to the advantage, it lifted and the acceptor ion was the boron ion and the injection amount which was useful was 8× 10 15 cm - 2 and the implant energy whi ch was useful corresponding to was 10keV and the inje ction amount was determined.

침작되어 패턴된 포토레지스트는 벗겨지고, 약 1㎛의 두께를 가진 다른 포토레지스트가 기판상에 침착되고, 이번에는 P튜브(250)의 표면을 노출시키기 위해 패턴된다. 이제, 도우너 이온이 CoSi2 함유 영역(300, 310)내로 주입된다(세로 침착된 레지스트는 n튜브(240)를 제2주입으로 부터 차폐한다). 다시, 주입량 및 이온 에너지는 상기 조건과 요구를 만족하도록 선택된다. 이점에 있어서, 만일 도오너 이온이 예를 들어 비소 이온이면, 유용한 주이량은 5#215#1015cm-2이고 유용한 대응하는 이온 에너지는 60keV 보다 작거나 같다. 한편, 만일 도우너 이온이 인 이온이면, 유용한 주입량은 5#215#1025cm-2이고, 유용한, 대응하는 주입 에너지는 30keV 이하의 에너지이다.

The photoresist which deposited is patterned comes off and the dissimilar photoresist having the thickness of about 1㎛ is deposited on the substrate and it is pat terned this time, in order to expose the surface of P tu be (250). Now, demand are selected so that the donor ion is injected within CoSi 2 containing domains (300, 3 10) (the resist deposited to the force shields the n tub e (240) from the second injection) the injection amoun t and ion energy are again satisfied the condition and d emand. As to the advantage, if the drawing owner ion i s for example, the arsenic ion , the heed amount which is useful is 5× 10 15 cm - 2 and it is smaller than 60ke V or the ion energy which is useful corresponding to is the same. In the meantime, if the donor ion is the phos phor ion , the injection amount which is useful is 5× 10 25 cm - 2 and the implant energy which is useful corre sponding to is energy less than 30keV.

이온 주입 이후에, 예를 들어, 0.2㎛ 두께의 도핑 되지 않은 TEOS층과 0.2㎛두께의 인 도핑된 TEOS층의 연속한 층을 포함하는 인터레벨 유전체(600)(제15도 참조)가 기판상에 침착된다. 인터레벨 유전체(600)는 흐르도록 유도되고, 주입된 도펀트는 CoSi2로 커버된 n+형 소스 및 드레인(330, 340)(제16도 참조)과, CoSi2로 커버된 P+형 소스 및 드레인(460, 470)을 기판 가열에 의해 형성하기 위해 CoSi2 함유 영역으로 부터 아래에 놓인 실리콘으로 확산된다. 이점에 있어서, 약 0.2㎛보다 작거나 같은 깊이를 가진 소스 및 드레인을 실현하기 위해, 유용한 가열 절차가 800℃의 온도로 120분동안 기판을 가열하는 것이라는 것이 결정되었다.

It was induced so that the interlevel dielectric (600) (the 15 is the reference) including for example, the und oped TEOS layer of 0.2㎛ thickness and the consecutiv e layer of the A -doped TEOS layer the phosphorus of 0.2㎛ thickness after the ion implantation was deposite d on the substrate the interlevel dielectric (600) flowed and in order that form the n + type source and the drai n (330, 340) (the 16 is the reference), covered with th e CoSi 2 and P + type source and drains (460, 470) co vered with the CoSi 2 with the substrate heating, the i njected dopant was diffused to the silicone which was beneath puts from the CoSi 2 containing domain the so urce and the drain having the depth which was smaller

GF Exhibit 1124 - 1963/2704

than about 0.2㎛ or thed same were realized as to the advantage the source were determined that the heatin g process which was useful heated the substrate with the temperature of 800℃ for 120 minutes.

COMOS IC의 제조와 관련하여, 금속 실리사이드 영역으로 부터 기판내로 주입된 도펀트를 확산하는데 사용되는 가열 온도를 선택할때 만족되어야 할 추가의 요구 조건이 있다는 것을 주목하자. 즉 예를 들어 종래의 용광로 가열을 이용할때, 약 900℃를 초과하는 온도에서, n형 폴리실리콘 구조(420)내의 n형 도펀트가 P형 폴리실리콘구조(290)(통상적으로 n형 폴리실리콘 주조(420)와 접속 되어 있음)로 확산되어 그것을 카운터 도핑하려는 경향이 있는 것으로 알려져 있다. 이와 같은 카운터 도핑은 그것이 P채널 MOSFET에서 바람직하지 못한 임계 전압 시프트를 유도하기 때문에 바람직하지 못하다. 결과적으로, 본 발명의 실시예 2에 따라, CMOS IC를 제조하기 위해 용광로 가열을 이용할때 사용된 가열 온도는 900℃보다 낮으며, 850℃ 이하의 것이 바람직하다.

It pays attention that it has the additional requirement specification to be satisfied when choosing the heating temperature which is used to diffuse the dopant inject ed from the metal silicide domain within the substrate i n connection with the manufacture of the COMOS IC. That is, for example, when the conventional blast furna ce heating is used , it has the tendency to the n-type dopant within the n-type polysilicon structure (420) be diffused to the P-type polysilicon structure (290) (gene rally it is connected to the n-type poly-silicon casting (420)) and decide on that in the temperature exceedin g about 900℃ with counter doping and it is known. In t his kind of counter doping, that the P-ch MOSFET, bec ause the threshold voltage shift could not with the be desirable paper is induced it cannot with the be desirab le paper. Consequently, to produce the CMOS IC accor ding to the embodiment 2 of the invention, the heating temperature which is used when using the blast furnac e heating is lower than that of 900℃ and less than 85 0℃ is the be desirable.

소스와 드레인을 형성한 후에, 인터레벨 유전체(600)가 소스와 드레인 및 게이트 전극으로 경유 구멍을 개방하기 위해 패턴된다. 알루미늄과 실리콘, 즉 층(350, 360과 370(제17도 참조), 480, 490과 500)의 상호 확산에 대한 장벽이 경유 구멍으로 침착된다. 소스와 드레인 및 게이트 전극으로 부터 금속 접촉 패드로 연장된 상호 접속 알루미늄 런너(375, 385, 395와 505, 515, 525)(제17도 참조)가 전술한 바와 같이 형성된다.

After source and drain are formed it is patterned so that the interlevel dielectric (600) open the via hole to source and drain and gate electrode. Aluminum and silic one, in other words, the obstacle toward the interdiffu sion of layers (350, 360 and 370 (the seventeenth is th e reference), 480, 490 and 500) are deposited to the v ia hole. As described above, interconnection aluminum r unner (375, 385, 395 and 505, 515, 525) (the sevente enth is the reference) extended to the metal contact p ad from source and drain and gate electrode are forme d.

CMOS IC는 습기 및 기계적 손상에 대비한 장벽을 형성하기 위해 IC상에 실리콘 질화물층을 침착시키는 단계를 포함하는 통상적인 일련의 단계를 통해 완성된다.

It is completed through normal a series of step that the CMOS IC includes the step of sinking the silicon nitr ide layer on IC in order to form the obstacle comparing for moisture and mechanical damage.

Disclaimer

본 문서는 특허 및 과학기술문헌 전용의 첨단 자동번역 시스템을 이용해 생성되었습니다. 따라서 부분적으로 오역의 가능성이 있으며, 본 문서를 자격을 갖춘 전문 번역가에 의한 번역물을 대신하는 것으로 이용되어서는 안 됩니다. 시스템 및 네트워크의 특성때문에 발생한 오역과 부분 누락, 데이터의 불일치등에 대하여 본원은 법적인 책임을 지지 않습니다. 본 문서는 당사의 사전 동의 없이 권한이 없는 일반 대중을 위해 DB 및 시스템에 저장되어 재생, 복사, 배포될 수 없음을 알려드립니다.
(The document produced by using the high-tech machine translation system for the pate nt and science & technology literature. Therefore, the document can include the mistrans lation, and it should not be used as a translation by a professional translator. We hold n o legal liability for inconsistency of mistranslation, partial omission, and data generated by feature of system and network. We would like to inform you that the document canno t be regenerated, copied, and distributed by being stored in DB and system for unauthori zed general public without our consent.)

GF Exhibit 1124 - 1964/2704

GF Exhibit 1124 - 1965/2704

(19) 대한민국특허청(KR)
(12) 공개특허공보(A)

(51) Int. Cl.[5]
H01L 27/04

(11) 공개번호 특1994-0020550
(43) 공개일자 1994년09월16일

(21) 출원번호 특1993-0003018
(22) 출원일자 1993년02월27일

(71) 출원인 삼성전자 주식회사 김광호
경기도 수원시 팔달구 매탄동 416번지
(72) 발명자 김진우
경기도 용인군 기흥읍 농서리 산 24번지
(74) 대리인 이영필, 박영우, 이윤민

심사청구 : 없음

(54) 반도체장치의 제조방법

요약

본 발명은 프로그램가능한 접속소자(programmable interconnect devices;PID)용 안티퓨즈 제조방법에 관한 것이다.

본 발명에 의한 PID용 안티퓨즈 제조방법은 PID용 안티퓨즈콘택과 금속콘택을 동시에 형성하는 공정과 안티퓨즈 막질로서 금속산화막을 형성하는 공정으로 이루어지는 것을 특징으로 한다.

본 발명에 의하면, 최소한의 포토리소그래픽공정에 의해 ID용 안티퓨즈를 형성할 수 있으며, 금속산화막을 안티퓨즈막으로 사용함으로써 막질의 두께를 조절할 수 있고 누설전류를 감소시킬 수 있어 안정된 소자동작을 얻을 수 있다.

대표도

도7

명세서

[발명의 명칭]

반도체장치의 제조방법

[도면의 간단한 설명]

제7도 내지 제11도는 본 발명에 의한 PID용 안티퓨즈 제조방법을 도시한 공정순서도.

본 내용은 요부공개 건이므로 전문 내용을 수록하지 않았음.

(57) 청구의 범위

청구항 1

반도체기판상에 하부도전층을 형성하는 공정; 상기 하부도전층상에 절연층을 형성하는 공정; 상기 하부도전층의 소정부분을 노출시키기 위해 상기 절연층에 안티퓨즈 콘택개구부 및 금속 콘택개구부를 동시에 형성하는 공정; 상기 결과물 전면에 금속산화막을 형성하는 공정; 상기 안티퓨즈 콘택영역에만 상기 금속산화막을 남기는 공정; 상기 결과물 전면에 금속을 증착한 후 이를 소정패턴으로 패터닝하여 상기 안티퓨즈 콘택영역의 상기 남아있는 금속산화막의 상부 및 상기 금속 콘택영역상에 상부도전층을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

청구항 2

제1항에 있어서, 상기 금속산화막은 금속을 증착한 후 산화공정에 의해 상기 금속을 산화시켜 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 3

제2항에 있어서, 상기 금속은 Ti, Al, Ba, Ge, Sn, Be, Nb 및 Ta 중에서 선택한 어느 하나임을 특징으로 하는 반도체장치의 제조방법.

청구항 4

GF Exhibit 1124 - 1966/2704

제2항에 있어서, 상기 산화공정은 400℃~800℃의 온도 범위에서 행하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 5

제1항에 있어서, 상기 금속산화막은 금속가스를 산소플라즈마에 통과시켜 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

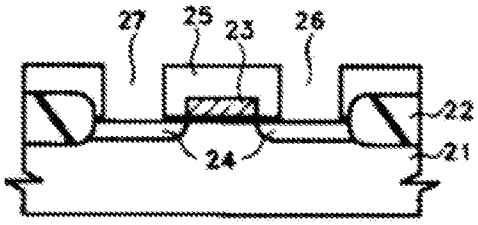
청구항 6

제1항에 있어서, 상기 상부도전층은 반도에기판에 형성된 불순물확산영역, 불순물이 도우프된 폴리실리콘층, 폴리사이드층 또는 반도체기판의 도전영역임을 특징으로 하는 프로그램가능한 접속소자의 제조방법.

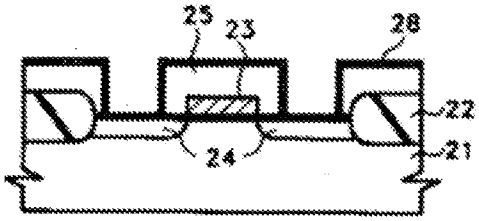
※ 참고사항 : 최초출원 내용에 의하여 공개하는 것임

도면

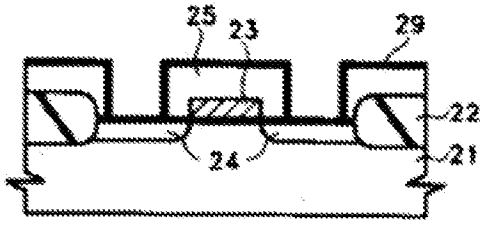
도면7



도면8

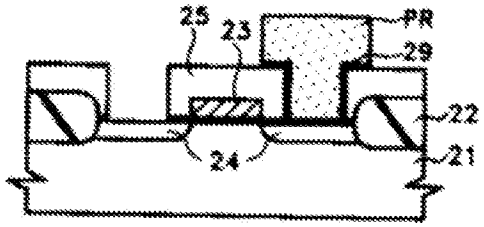


도면9

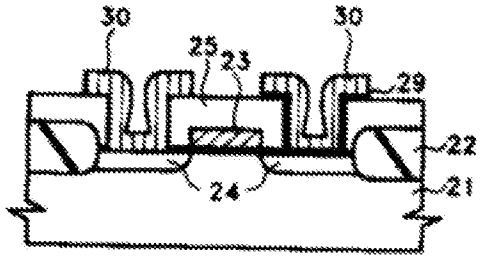


GF Exhibit 1124 - 1967/2704

도면10



도면11



GF Exhibit 1124 - 1968/2704

Unexamined Patent Publication(A)

Bibliographic Data

Int.Cl.	H01L 23/525
Published Date	19950925
Registration No.	1000941860000
Registration Date	19960116
Application No.	1019930003018
Application Date	19930227
Unexamined Publication No.	1019940020550
Unexamined Publication Date	19940916
Requested Date of Examination	19930227
Agent.	PARK, Young Woo | Lee Young Pil | Lee Yoon Min
Inventor	Jin-U Kim
Applicant	SAMSUNG ELECTRONICS CO., LTD.
Rightholder	SAMSUNG ELECTRONICS CO., LTD.

발명의 명칭

반도체장치의제조방법

Title of Invention

SEMICONDUCTOR DEVICE

요약

본 발명은 프로그램가능한 접속소자(programmable interconnect devices;PID)용 안티퓨즈 제조방법에 관한 것이다.

본 발명에 의한 PID용 안티퓨즈 제조방법은 PID용 안티퓨즈콘택과 금속콘택을 동시에 형성하는 공정과 안티퓨즈 막질로서 금속산화막을 형성하는 공정으로 이루어지는 것을 특징으로 한다.

본 발명에 의하면, 최소한의 포토리소그래픽공정에 의해 ID용 안티퓨즈를 형성할 수 있으며, 금속산화막을 안티퓨즈막으로 사용함으로써 막질의 두께를 조절할 수 있고 누설전류를 감소시킬 수 있어 안정된 소자동작을 얻을 수 있다.

Abstract

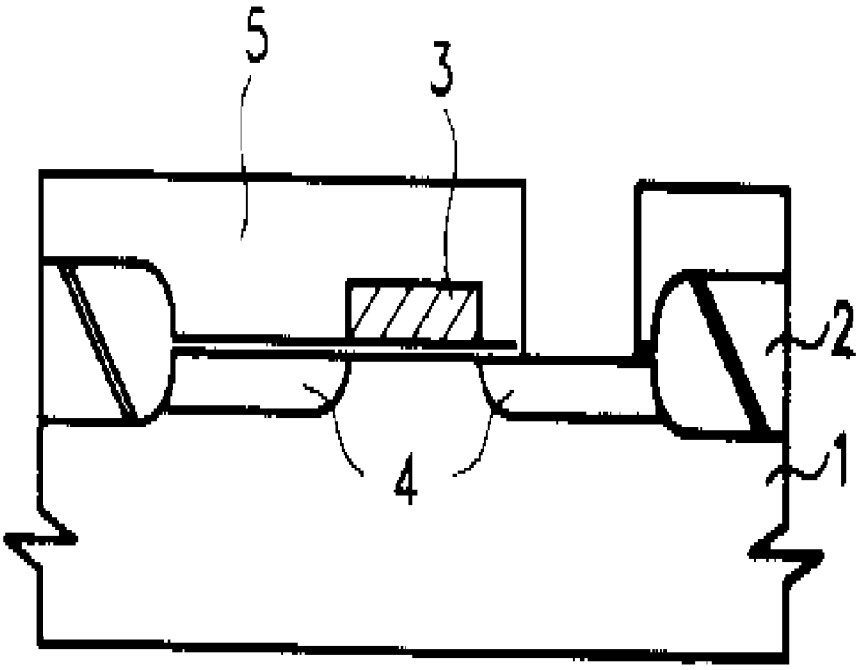
The present invention relates to the programmable method for manufacturing anti-fuse for the connection element (programmable interconnect devices:PID).

The method for manufacturing anti-fuse for PID according to the invention comprises the anti-fuse contact for PID and the process of simultaneously forming the metal contact and the process of forming the metal oxide layer as the anti-fuse thin film.

According to the invention, the anti-fuse for ID by the minimum photolithographic process is used as the anti-fuse film the metal oxide layer it can form. And the component performance controlling the thickness of the thin film and reduce the leakage current and is stabilized can be obtained.

대표도면(Representative drawing)

GF Exhibit 1124 - 1969/2704



청구의 범위

청구 1항:

반도체기판상에 하부도전층을 형성하는 공정; 상기 하부도전층상에 절연층을 형성하는 공정; 상기 하부도전층의 소정부분을 노출시키기 위해 상기 절연층에 안티퓨즈 콘택개구부 및 금속 콘택개구부를 동시에 형성하는 공정; 상기 결과물 전면에 금속산화막을 형성하는 공정; 상기 안티퓨즈 콘택영역에만 상기 금속산화막을 남기는 공정; 상기 결과물 전면에 금속을 증착한 후 이를 소정패턴으로 패터닝하여 상기 안티퓨즈 콘택영역의 상기 남아있는 금속산화막의 상부 및 상기 금속 콘택영역상에 상부도전층을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

청구 2항:

제1항에 있어서, 상기 금속산화막은 금속을 증착한 후 산화공정에 의해 상기 금속을 산화시켜 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구 3항:

제2항에 있어서, 상기 금속은 Ti, Al, Ba, Ge, Sn, Be, Nb 및 Ta 중에서 선택한 어느 하나임을 특징으로 하는 반도체장치의 제조방법.

Scope of Claims

Claim 1:

The method for fabricating semiconductor device consisting of the process of forming the bottom conductive layer on the semiconductor substrate, the process of forming the insulating layer on the bottom conductive layer, the anti-fuse contact opening in the insulating layer and the process of simultaneously forming the metal contact opening part the prescribed part of the bottom conductive layer is exposed, the process of forming the metal oxide layer on the outcome front side, the process of leaving the metal oxide layer in the anti-fuse contact area, and the process of patterning this in the desired pattern after depositing the metal and forming the top conductive layer on the outcome front side on the upper portion of the above-mentioned metal oxide layer remaining of the anti-fuse contact area and metal contact area.

Claim 2:

As for claim 1, the method for fabricating semiconductor device which oxidizes the metal after depositing the metal with the oxidation process and which the metal oxide layer forms.

Claim 3:

As for claim 2, the method for fabricating semiconductor device which is characterized that the metal is any one that selects between the ti, al, ba, ge, sn, be, nb and Ta.

GF Exhibit 1124 - 1970/2704

청구 4항:

제2항에 있어서, 상기 산화공정은 400℃~800℃의 온도 범위에서 행하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 4:

As for claim 2, the method for fabricating semiconductor device which the oxidation process perf orms in the temperature range of 400℃~800℃.

청구 5항:

제1항에 있어서, 상기 금속산화막은 금속가스를 산소플라즈마에 통과시켜 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 5:

As for claim 1, the method for fabricating semiconductor device which passes the metal gas thro ugh in the oxygen plasma and which the metal oxide la yer forms.

청구 6항:

제1항에 있어서, 상기 상부도전층은 반도에기판에 형성된 불순물확산영역, 불순물이 도우프된 폴리실리콘층, 폴리사이드층 또는 반도체기판의 도전영역임을 특징으로 하는 프로그램가능한 접속소자의 제조방법.※ 참고사항 : 최초출원 내용에 의하여 공개하는 것임.

Claim 6:

As for claim 1, the manufacturing method of the programmable connection element which is characteriz ed being the impurity diffusion region, in which the top conductive layer is formed in the Ban DoE substrate th e polysilicon layer in which the impurity is doped, and t he conductive region of the polycide layer or the semic onductor substrate. ※ list of reference: it discloses wit h the initial application contents.

상세설명

[발명의 명칭]

반도체장치의 제조방법

[도면의 간단한 설명]

제7도 내지 제11도는 본 발명에 의한 PID용 안티퓨즈 제조방법을 도시한 공정순서도.

본 내용은 요부공개 건이므로 전문 내용을 수록하지 않았음.

Detailed Description

[Title of invention]

Method for fabricating semiconductor device.

[Brief description of drawings]

The process flowchart in which the seventh the inland eleventh drawing shows the method for manufacturing anti-fuse for PID according to the invention.

The technical content was not given mention of since this content was the main part disclosure gun.

Disclaimer

본 문서는 특허 및 과학기술문헌 전용의 첨단 자동번역 시스템을 이용해 생성되었습니다. 따라서 부분적으로 오역의 가능성이 있으며, 본 문서를 자격을 갖춘 전문 번역가에 의한 번역물을 대신하는 것으로 이용되어서는 안 됩니다. 시스템 및 네트워크의 특성때문에 발생한 오역과 부분 누락, 데이터의 불일치등에 대하여 본원은 법적인 책임을 지지 않습니다. 본 문서는 당사의 사전 동의 없이 권한이 없는 일반 대중을 위해 DB 및 시스템에 저장되어 재생, 복사, 배포될 수 없음을 알려드립니다.
(The document produced by using the high-tech machine translation system for the pate nt and science & technology literature. Therefore, the document can include the mistrans lation, and it should not be used as a translation by a professional translator. We hold n o legal liability for inconsistency of mistranslation, partial omission, and data generated by feature of system and network. We would like to inform you that the document canno t be regenerated, copied, and distributed by being stored in DB and system for unauthori zed general public without our consent.)

GF Exhibit 1124 - 1971/2704

(19) 대한민국특허청(KR)
(12) 특허공보(B1)

(51) Int. Cl.[6]
H01L 27/04(105)

(45) 공고일자 1995년09월25일
(11) 공고번호 특1995-0010873
(24) 등록일자 1995년09월25일

(21) 출원번호 특1993-0003018
(22) 출원일자 1993년02월27일
(65) 공개번호 특1994-0020550
(43) 공개일자 1994년09월16일

(71) 출원인 삼성전자주식회사 김광호
경기도 수원시 팔달구 매탄동 416번지

(72) 발명자 김진우
경기도 용인군 기흥읍 농서리 산 25번지

(74) 대리인 이영필, 박영우, 이윤민

심사관 : 김형욱 (특허공보 제1993호)

(54) 반도체장치의 제조방법

요약

내용 없음.

대표도

도1

명세서

[발명의 명칭]

반도체장치의 제조방법

[도면의 간단한 설명]

제1도 내지 제6도는 종래의 PID용 안티퓨즈 형성방법을 도시한 공정순서도.

제7도 내지 제11도는 본 발명에 의한 PID용 안티퓨즈 제조방법을 도시한 공정순서도.

[발명의 상세한 설명]

본 발명은 집적회로 반도체장치의 제조방법에 관한 것으로, 특히 프로그램가능한 접속소자(Programmable interconnect devices: PID)의 제조방법에 관한 것이다.

프로그램가능한 반도체장치에는 PROM(Programmable Read only Memory), PLD(Programmable Logic Device) 및 프로그램 가능한 게이트어레이(Programmable Gate Array) 등이 있으며, 이러한 종류의 반도체장치들에 적합한 프로그램가능한 소자에는 퓨즈(fuse) 방식과 안티퓨즈(antifuse)방식이 적용된다.

PID는 안티퓨즈(Antifuse) 구조의 한 유형으로서, 안티퓨즈구조란 이름 그대로 퓨즈와 반대되는 동작을 하는 소자를 말한다. 안티퓨즈는 프로그램되지 않았을 때, 즉, 프로그래밍전압을 인가하기 전에는 고저항을 형성하거나 저기적 통로를 개방시키고, 임계전압을 인가함에 따라 프로그램되면 저저항을 형성하거나 두도전선간에 폐쇄된 전기적 통로를 형성한다.

집적회로에 있어서, 접속되는 도전선(coducting line)들이 다층으로 서로 적층되는데 이러한 다층접속구조는 도전선들 사이에 절연층을 개재하여 형성한다. 특히, 가장 최하부의 제1도전선들과 그 윗층의 제2도전선들 사이에 안티퓨즈 구조를 형성하기 위해서는 제1도전선상에 두거운 절연층을 형성한다. 이 제1 도전선은 집적회로기판의 불순물이 도우프된 영역, 기판상에 형성된 에피택셜층의 불순물이 도우프된 영역 또는 기판상의 불순물이 도우프된 폴리실리콘층일 수도 있다. 그리고 나서 상기 두꺼운 절연막을 통하여 원하는 접속부위에 콘택개구부(contact opening)를 형성한 다음 상기 두꺼운 절연층과 콘택개구부상에 안티퓨즈 유전층을 증착한다. 안티퓨즈구조의 중요한 변수는이 유전층에 사용되는 물질에 크게 의존한다. 이어서 상기 안티퓨즈 유전층상에 제2 도전층을 증착한 후, 통상의 반도체 공정기술에 의해 상기 제2 도전층을 마스킹, 식각 및 한정하여 도전성을 형성한다.

종래의 필드 프로그램가능한 소자(Field programmable devices; FPD) 또는 안티퓨즈구조는 통상 기준 프로그래밍 전압이 15V~30V 인가되면 프로그램되는 동안 약 1msec의 프로그램시간 동안에 약 1mA의 프로그래밍전류를 흐르게 한다. 또한, 이들 종래의 소자는 통상 프로그램되지 않은 상태에서 10MΩ~10GΩ의 오프(off) 저항을 가지며, 10Ω~1000Ω의 온(on) 저항을 갖는다.

여러가지 다양한 안티퓨즈구조가 미합중국 특허 제4,882,611호 및 유럽특허 416,903A2에 개시되어 있다.

미합중국 특허 제4,882,611호에 개시된 안티퓨즈구조는 이온주입기술을 이용하여 도핑된 반도체기판 부분

GF Exhibit 1124 - 1972/2704

의 표면을 비정질환(Amorphous)하여 저항값을 증가시켜 개방(open)효과를 얻고, 고전압을 인가하면 비정질조직이 다시 결정화되어 단락(Short)되는 효과를 얻는 것이다.

유럽특허 416,903A2에 개시된 안티퓨즈구조는 안티퓨즈층으로서 비정질실리콘으로 사용하거나, 또는 비정질실리콘층/박막의 유전체막/비정질실리콘층의 적층된 구조를 사용하고 있다.

제1도 내지 제6도를 참조하여 종래의 PID용 안티퓨즈 형성방법을 설명하면 다음과 같다.

먼저, 제1도를 참조하면, 실리콘기판(1)상에 통상의 MOS공정에 의해 필드산화막(2), 게이트전극(3) 및 소오스/드레인영역(4)을 형성하고 전면에 절연층(5)을 형성한 후 포토리소그래피공정에 의해 상기 절연층(5)에 안티퓨즈 콘택을 형성한다.

이어서 제2도에 도시된 바와 같이 상기 안티퓨즈 콘택에 산화막(6)을 형성한다.

다음에 제3도에 도시된 바와 같이 상기 결과물 전면에 불순물에 도핑되지 않은 폴리실리콘(Undoped polysilicon)(7)을 증착한다.

이어서 제4도에 도시된 바와 같이 포토레지스트(PR)를 도포하고 포토리소그래피공정을 통해 안티퓨즈가 형성될 부분에만 상기 폴리실리콘층(7)이 남도록 패터닝하여 소정 패턴의 폴리실리콘층(8)을 형성한다.

다음에 제5도에 도시된 바와 같이 포토레지스트(PR)를 도포하고 포토리소그래피공정을 통해 금속콘택을 형성한다.

이어서 제6도에 도시된 바와 같이 포토레지스트를 제거한 후, 상기 결과물 전면에 금속을 증착한 후, 포토리소그래피공정에 의해 금속배선(10)을 형성한다.

상기한 종래의 안티퓨즈 형성방법들에 있어서는, 일반적인 MOS공정에 PID형성공정을 적용할 경우 안티퓨즈콘택 형성을 위한 포토리소그래피공정 및 상기 불순물이 도핑되지 않은 폴리실리콘층(Undoped polysilicon) 패터닝을 위한 포토리소그래피공정등으로 제조공정이 복잡하며, 안티퓨즈층이 산화막/불순물이 도핑되지 않은 폴리실리콘층(Undoped polysilicon)의 구조로 구성되므로 안티퓨즈층 두께의 조절이 불리하며, 불순물이 도핑되지 않은 폴리실리콘층의 추가에 따른 안티퓨즈의 캐패시턴스 변화가 크고 누설전류가 문제가 된다.

본 발명은 상술한 문제를 해결하기 위한 것으로, PID 제조공정을 최소한의 포토리소그래피공정에 의해 MOS 공정에 적용할 수 있으며, 금속산화막을 안티퓨즈막질로 사용함으로써 막질의 두께조절 및 누설전류의 감소가 가능한 PID제조방법을 제공하는 것을 그 목적으로 한다.

상기 목적을 달성하기 위해 본 발명은 반도체기판상에 하부도전층을 형성하는 공정; 상기 하부도전층상에 절연층을 형성하는 공정; 상기 하부도전층의 소정부분을 노출시키기 위해 상기 절연층에 안티퓨즈 콘택개구부 및 금속 콘택개구부를 동시에 형성하는 공정; 상기 결과물 전면에 금속산화막을 형성하는 공정; 상기 안티퓨즈 콘택영역에만 상기 금속산화막을 남기는 공정; 및 상기 결과물 전면에 금속을 증착한 후 이를 소정패턴으로 패터닝하여 상기 안티퓨즈 콘택영역의 상기 남아 있는 금속산화막의 상부 및 상기 금속콘택영역상에 상부 도전층을 형성하는 공정으로 이루어진 것을 특징으로 하는 프로그램가능한 접속소자의 제조방법을 제공한다.

본 발명의 일실시예에 의하면, 상기 금속산화막은 금속을 증착한 후 산화공정에 의해 상기 금속을 산화시켜 형성한다.

상기 금속으로는 Ti, Al, Ba, Ge, Sn, Be, Nb 및 Ta중에서 선택한 어느 하나를 사용하여 금속산화막을 형성한다.

본 발명의 다른 실시예에 의하면, 상기 금속산화막은 금속가스를 산소플라즈마에 통과시켜 형성한다.

상기 상부전층은 반도체기판에 형성된 불순물확산영역, 불순물이 도우프된 폴리실리콘층, 폴리사이드층 또는 반도체기판의 도전영역일 수 있다.

본 발명에 의한 PID용 안티퓨즈 제조방법은 PID용 안티퓨즈 콘택과 금속콘택을 동시에 형성하는 공정과 안티퓨즈 막질로서 금속산화막을 형성하는 공정으로 이루어지는 것을 특징으로 한다.

제7도 내지 제11도를 참조하여 본 발명에 의한 PID용 안티퓨즈 제조방법을 설명하면 다음과 같다.

먼저, 제7도를 참조하면, 실리콘기판(21)상에 통상의 MOS 공정에 의해 필드산화막(22), 게이트전극(23) 및 소오스/드레인영역(24)을 형성하고 전면에 절연층(25)을 형성한 후 포토리소그래피공정에 의해 상기 절연층(5)에 안티퓨즈 콘택개구부(26)와 금속콘택개구부(27)를 동시에 형성한다.

이어서 제8도를 참조하면, 상기 결과물상에 금속층(28)을 얇게 증착한다.

다음에 제9도를 참조하면, 산화공정을 진행하여 상기 형성된 금속층을 산화시켜 금속산화막(29)을 형성한다.

이어서 제10도를 참조하면, 포토리소그래피공정을 통해 상기 안티퓨즈 콘택부분에만 상기 금속산화막(29)을 남기고 나머지 부분에 형성된 금속산화막은 제거한다.

다음에 제11도를 참조하면, 상기 결과물 전면에 금속을 증착한 후 이를 포토리소그래피공정에 의해 소정패턴으로 패터닝하여 금속배선(30)을 형성한다.

상기한 바와 같이 본 발명은 안티퓨즈콘택과 금속패턴을 동시에 형성함으로써 제조공정을 단순화시킬 수 있다. 또한, 안티퓨즈 산화막/불순물이 도핑되지 않은 폴리실리콘으로 된 안티퓨즈구조를 금속산화막으로 된 안티퓨즈구조로 바꿈으로써 안티퓨즈막두께의 조절이 용이하게 되며, 누설전류를 감소시키는 효과가 생긴다.

GF Exhibit 1124 - 1973/2704

이하, 본 발명의 일실시예를 도면에 참조하여 설명하면 다음과 같다.

제7도 내지 제11도에 본 발명에 의한 PID용 안티퓨즈 제조방법을 도시하였다.

먼저, 제7도에 도시한 바와 같이 실리콘기판(21)상에 통상의 MOS공정에 의해 필드산화막(22), 게이트 전극(23) 및 소오스/드레인영역(24)을 형성하고 전면에 절연층(25)으로서, 예컨대 산화막을 형성한 후, 포토리소그래피공정에 의해 상기 산화막(5)에 안티퓨즈 콘택개구부(26)와 금속콘택개구부(27)를 동시에 형성한다.

이어서 제8도에 도시한 바와 같이 상기 결과물상에 금속층(28)으로서, 예컨대 Ti, Al, Sn, Ta, Ba, Ge, Be, Nb 중에서 선택한 어느 하나를 100Å~500Å 정도의 두께로 얇게 증착한다.

다음에 제9도에 도시한 바와 같이 450℃~800℃의 온도범위에서 산화공정을 진행하여 상기 형성된 금속층을 산화시켜 금속산화막(29)을 형성한다.

이때, 상기 금속산화막을 형성하는 공정을 제8도 및 제9도에 도시한 바와 같이 금속층을 먼저 형성한 후 이를 산화시키는 공정을 이용하지 않고, 금속가스를 산소플라즈마에 통과시켜 금속산화물을 형성할 수도 있다.

이어서 제10도에 도시한 바와 같이 포토리소그래피공정을 통해 상기 안티퓨즈 콘택부분에만 상기 금속산화막(29)을 남기고 나머지 부분에 형성된 금속산화막은 제거한다.

다음에 제11도에 도시된 바와 같이 상기 결과물을 전면에 금속을 증착한 후 이를 포토리소그래피공정에 의해 소정패턴으로 패터닝하여 금속배선(30)을 형성한다.

상기 금속산화막을 Al을 이용하여 형성할 경우, 상술한 바와 하나의 챔버(Chamber)내에서 산소플라즈마에 Al가스를 흘려주어 Al_2O_3의 금속산화막을 형성한 후, 동일한 챔버내에서 타겟(Target)만 변경하여(인시이튜(in-situ)로 Al(1% Si+0.5% Cu를 함유하는)을 증착함으로써 금속배선을 형성할 수 있으므로 현재의 스퍼터(Sputter)장비에서 쉽게 적용시킬 수 있으며, 금속산화막 형성후에 행해지는 후속공정인 금속배선의 형성을 하나의 장비내에서 용이하게 형성할 수 있다.

상술한 본 발명에 의하면, 안티퓨즈 콘택과 금속콘택을 동시에 형성함으로써 이를 각각 형성하던 종래방법 보다 공정을 단순화시킬 수 있으며, 종래의 산화막/불순물이 도핑되지 않은 폴리실리콘구조로 이루어진 안티퓨즈구조를 금속산화막으로 대체함으로써 안티퓨즈막의 두께조절이 용이하게 되며 누설전류가 감소하게 된다. 특히, Al_2O_3와 같은 금속산화막은 Na^+이온의 확산에 강한 배리어(barrier)로 작용하여 소자를 신뢰성을 향상시킨다.

이상, 상술한 바와 같이 본 발명에 의하면, 최소한의 포토리소그래피공정에 의해 PID용 안티퓨즈를 형성할 수 있으며, 금속산화막을 안티퓨즈막으로 사용함으로써 막질의 두께를 조절할 수 있고 누설전류를 감소시킬 수 있어 안정된 소자동작을 얻을 수 있다.

(57) 청구의 범위

청구항 1

반도체기판상에 하부도전층을 형성하는 공정; 상기 하부도전층상에 절연층을 형성하는 공정; 상기 하부도전층의 소정부분을 노출시키기 위해 상기 절연층에 안티퓨즈 콘택개구부 및 금속 콘택개구부를 동시에 형성하는 공정; 상기 결과를 전면에 금속산화막을 형성하는 공정; 사기 안티퓨즈 콘택영역에만 상기 금속산화막을 남기는 공정; 및 상기 결과물 전면에 금속을 증착한 후 이를 소정패턴으로 패터닝하여 상기 안티퓨즈 콘택영역의 상기 남아 있는 금속산화막의 상부 및 상기 금속 콘택영역상에 상부도전층을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

청구항 2

제1항에 있어서, 상기 금속산화막은 금속을 증착한 후 산화공정에 의해 상기 금속을 산화시켜 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 3

제2항에 있어서, 상기 금속은 Ti, Al, Ba, Ge, Sn, Be, Nb 및 Ta 중에서 선택한 어느 하나임을 특징으로 하는 반도체장치의 제조방법.

청구항 4

제2항에 있어서, 상기 산화공정은 400℃~800℃의 온도범위내에서 행하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 5

제1항에 있어서, 상기 금속산화막은 금속가스를 산소플라즈마에 통과시켜 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

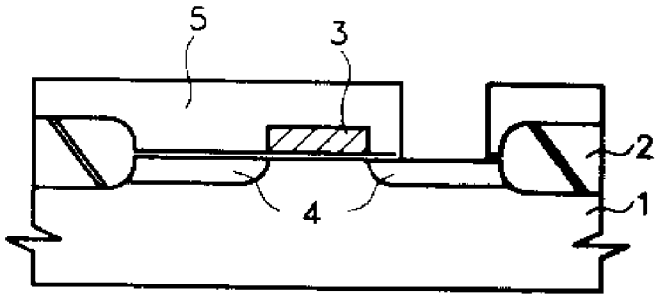
청구항 6

제1항에 있어서, 상기 상부도전층은 반도체기판에 형성된 불순물확산영역, 불순물이 도우프된 폴리실리콘층, 폴리사이드층 또는 반도체기판의 도전영역임을 특징으로 하는 프로그램 가능한 접속소자의 제조방법.

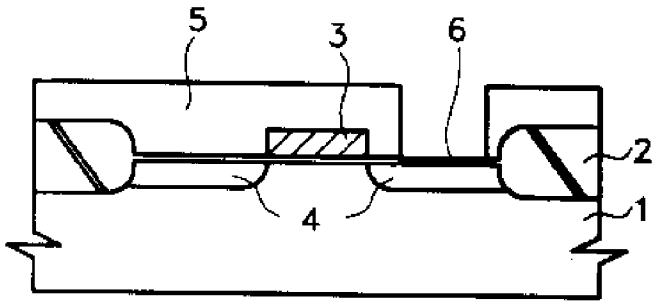
GF Exhibit 1124 - 1974/2704

도면

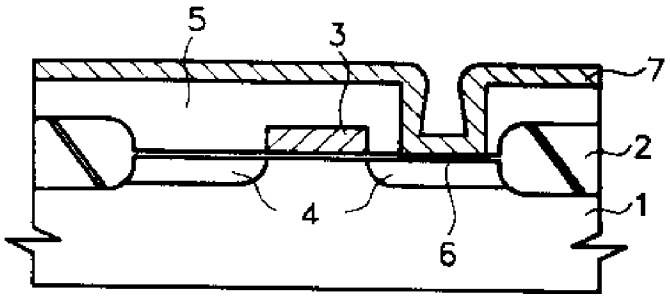
도면1



도면2

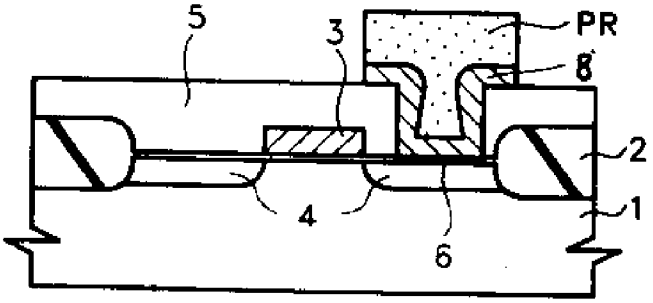


도면3

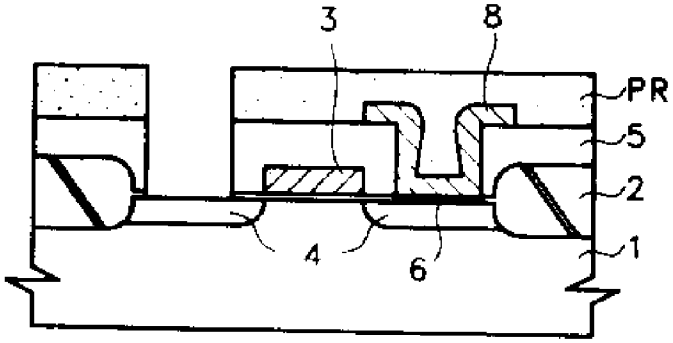


GF Exhibit 1124 - 1975/2704

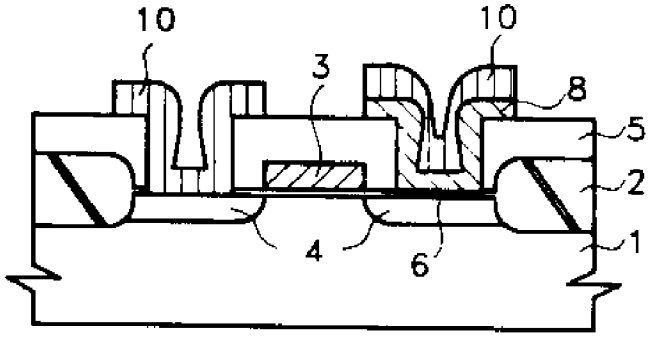
도면4



도면5

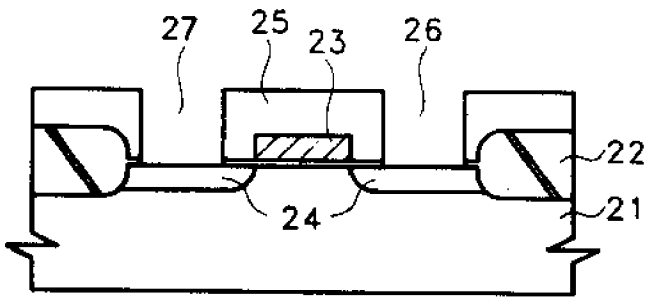


도면6

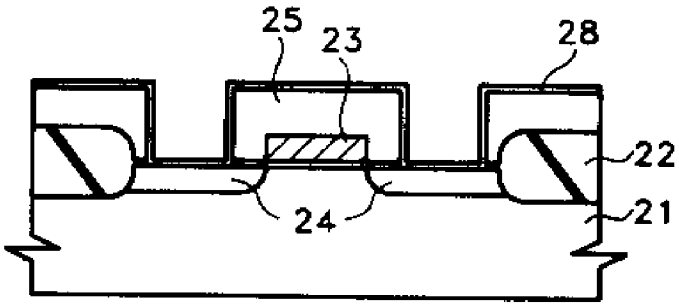


GF Exhibit 1124 - 1976/2704

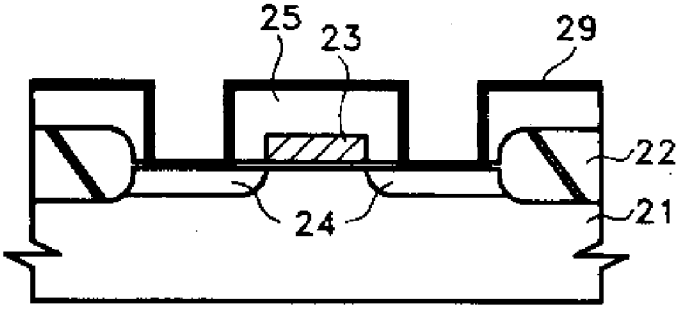
도면7



도면8

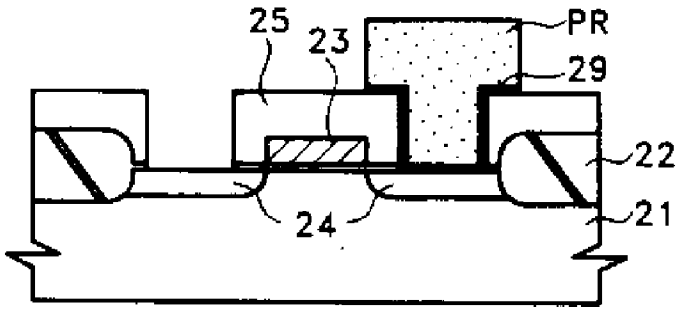


도면9

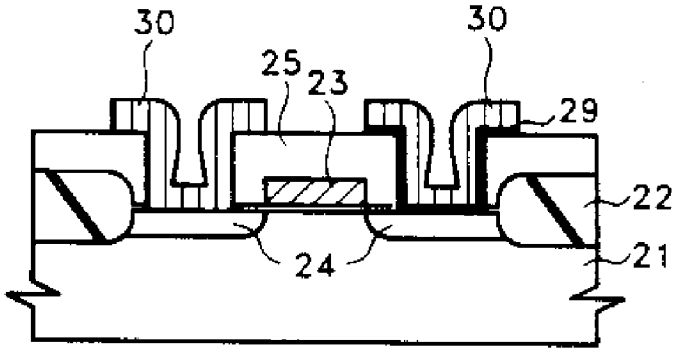


GF Exhibit 1124 - 1977/2704

SB10



SB11



GF Exhibit 1124 - 1978/2704

Examined Patent Publication(B1)

Bibliographic Data

Int.Cl.	H01L 23/525
Published Date	19950925
Registration No.	1000941860000
Registration Date	19960116
Application No.	1019930003018
Application Date	19930227
Unexamined Publication No.	1019940020550
Unexamined Publication Date	19940916
Requested Date of Examination	19930227
Agent.	PARK, Young Woo | Lee Young Pil | Lee Yoon Min
Inventor	Jin-U Kim
Applicant	SAMSUNG ELECTRONICS CO., LTD.
Rightholder	SAMSUNG ELECTRONICS CO., LTD.

발명의 명칭

반도체장치의제조방법

Title of Invention

SEMICONDUCTOR DEVICE

요약

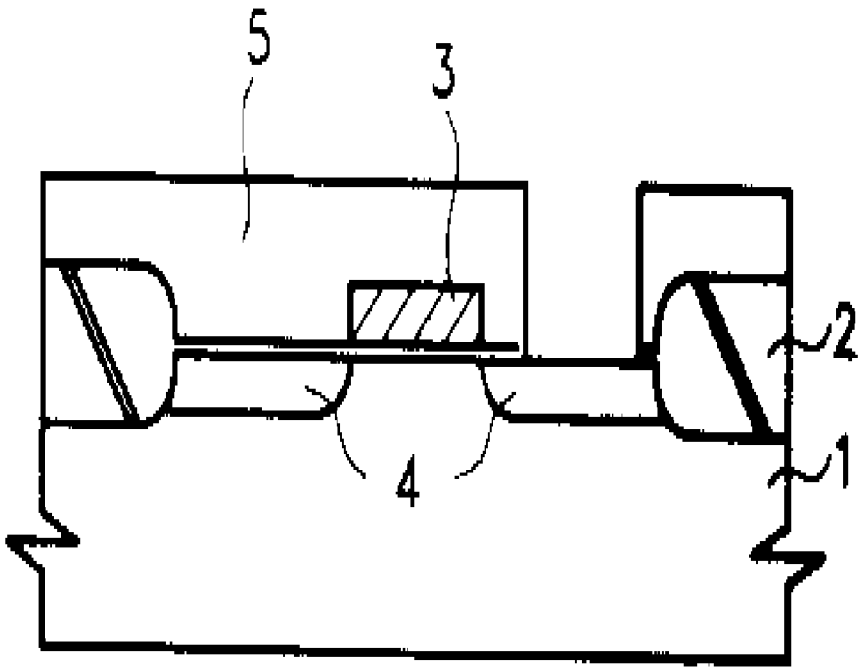
내용 없음.

Abstract

Content none.

대표도면(Representative drawing)

GF Exhibit 1124 - 1979/2704



청구의 범위

청구 1항:

반도체기판상에 하부도전층을 형성하는 공정; 상기 하부도전층상에 절연층을 형성하는 공정; 상기 하부도전층의 소정부분을 노출시키기 위해 상기 절연층에 안티퓨즈 콘택개구부 및 금속 콘택개구부를 동시에 형성하는 공정; 상기 결과를 전면에 금속산화막을 형성하는 공정; 사기 안티퓨즈 콘택영역에만 상기 금속산화막을 남기는 공정; 및 상기 결과물 전면에 금속을 증착한 후 이를 소정패턴으로 패터닝하여 상기 안티퓨즈 콘택영역의 상기 남아 있는 금속산화막의 상부 및 상기 금속 콘택영역상에 상부도전층을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

청구 2항:

제1항에 있어서, 상기 금속산화막은 금속을 증착한 후 산화공정에 의해 상기 금속을 산화시켜 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구 3항:

제2항에 있어서, 상기 금속은 Ti, Al, Ba, Ge, Sn, Be, Nb 및 Ta 중에서 선택한 어느 하나임을 특징으로 하는 반도체장치의 제조방법.

Scope of Claims

Claim 1:

The method for fabricating semiconductor device consisting of the process of forming the bottom conductive layer on the semiconductor substrate, the process of forming the insulating layer on the bottom conductive layer, the anti-fuse contact opening in the insulating layer and the process of simultaneously forming the metal contact opening part the prescribed part of the bottom conductive layer is exposed, the process of forming the metal oxide layer the result on front, the process of leaving the metal oxide layer in the cheating anti-fuse contact area, and the process of patterning this in the desired pattern after depositing the metal and forming the top conductive layer on the outcome front side on the upper portion of the above-mentioned metal oxide layer remaining of the anti-fuse contact area and metal contact area.

Claim 2:

As for claim 1, the method for fabricating semiconductor device which oxidizes the metal after depositing the metal with the oxidation process and which the metal oxide layer forms.

Claim 3:

As for claim 2, the method for fabricating semiconductor device which is characterized that the metal is any one that selects between the ti, al, ba, ge, sn, be, nb and Ta.

GF Exhibit 1124 - 1980/2704

청구 4항:

제2항에 있어서, 상기 산화공정은 400℃~800℃의 온도범위내에서 행하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 4:

As for claim 2, the method for fabricating semiconductor device which the oxidation process performs in the temperature range of 400℃~800℃.

청구 5항:

제1항에 있어서, 상기 금속산화막은 금속가스를 산소플라즈마에 통과시켜 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 5:

As for claim 1, the method for fabricating semiconductor device which passes the metal gas through in the oxygen plasma and which the metal oxide layer forms.

청구 6항:

제1항에 있어서, 상기 상부도전층은 반도체기판에 형성된 불순물확산영역, 불순물이 도우프된 폴리실리콘층, 폴리사이드층 또는 반도체기판의 도전영역임을 특징으로 하는 프로그램 가능한 접속소자의 제조방법.

Claim 6:

As for claim 1, the manufacturing method of the programmable connection element which is characterized being the impurity diffusion region, in which the top conductive layer is formed in the semiconductor substrate the polysilicon layer in which the impurity is doped, and the conductive region of the polycide layer or the semiconductor substrate.

상세설명

Detailed Description

[발명의 명칭]

반도체장치의 제조방법

[Title of invention]

Method for fabricating semiconductor device.

[도면의 간단한 설명]

제1도 내지 제6도는 종래의 PID용 안티퓨즈 형성방법을 도시한 공정순서도.

제7도 내지 제11도는 본 발명에 의한 PID용 안티퓨즈 제조방법을 도시한 공정순서도.

[Brief description of drawings]

The process flowchart in which the first the inland sixth drawing shows the method for forming the anti-fuse for the conventional PID.

The process flowchart in which the seventh the inland eleventh drawing shows the method for manufacturing anti-fuse for PID according to the invention.

[발명의 상세한 설명]

[Detailed description of the invention]

본 발명은 집적회로 반도체장치의 제조방법에 관한 것으로, 특히 프로그램가능한 접속소자(Programmable interconnect devices: PID)의 제조방법에 관한 것이다.

The invention relates to the integrated circuit method for fabricating semiconductor device, and particularly, to the manufacturing method of the programmable connection element (Programmable interconnect devices: PID).

프로그램가능한 반도체장치에는 PROM(Programmable Read only Memory), PLD(Programmable Logic Device) 및 프로그램 가능한 게이트어레이(Programmable Gate Array) 등이 있으며, 이러한 종류의 반도체장치들에 적합한 프로그램가능한 소자에는 퓨즈(fuse) 방식과 안티퓨즈(antifuse)방식이 적용된다.

In the programmable semiconductor device, it has the PROM (Programmable Read only Memory), and the PLD (Programmable Logic Device) and programmable gate array etc and the fuse mode and anti-fuse (antifuse) mode are applied in the programmable device which is suitable for the semiconductor devices of such kind.

PID는 안티퓨즈(Antifuse) 구조의 한 유형으로서, 안티퓨즈구조란 이름 그대로 퓨즈와 반대되는 동작을 하는 소자를 말한다. 안티퓨즈는 프로그램되지 않았을 때, 즉, 프로그래밍전압을 인가하기 전에는 고저항을 형성하거나 저기적 통로를 개방시키고, 임계전압을 인가함에 따라 프로그램되면 저저항을 형성하거나 두도전선간에 폐쇄된 전기적 통로를 형성한다.

As PID is one type of the anti-fuse (Antifuse) structure, the anti-fuse structure refers to the device doing the operation of being like that opposed to the fuse with name. When the anti-fuse was not programmed , the high value resistor is formed in total to apply in other words, the programming voltage or the base wonder path is opened and if it is programmed according to apply the critical voltage, the low resistance is formed

GF Exhibit 1124 - 1981/2704

or the electrical gateway closed at two conductive line livers is formed.

집적회로에 있어서, 접속되는 도전선(coducting line)들이 다층으로 서로 적층되는데 이러한 다층접속구조는 도전선들 사이에 절연층을 개재하여 형성한다. 특히, 가장 최하부의 제1도전선들과 그 윗층의 제2도전선들 사이에 안티퓨즈 구조를 형성하기 위해서는 제1도전선상에 두거운 절연층을 형성한다. 이 제1도전선은 집적회로기판의 불순물이 도우프된 영역, 기판상에 형성된 에피택셜층의 불순물이 도우프된 영역 또는 기판상의 불순물이 도우프된 풀리실리콘층일 수도 있다. 그리고 나서 상기 두꺼운 절연막을 통하여 원하는 접속부위에 콘택개구부(contact opening)를 형성한 다음 상기 두꺼운 절연층과 콘택개구부상에 안티퓨즈 유전층을 증착한다. 안티퓨즈구조의 중요한 변수는이 유전층에 사용되는 물질에 크게 의존한다. 이어서 상기 안티퓨즈 유전층상에 제2 도전층을 증착한 후, 통상의 반도체 공정기술에 의해 상기 제2 도전층을 마스킹, 식각 및 한정하여 도전성을 형성한다.

As to the integrated circuit, connected conductive line (coducting line) are laminated to the multi layer but such multi-layer connection structure interposes the insulating layer in the interval like the electric conduction and the interval forms. Especially, *** luck insulating layer is formed on the first conductive line in order to most form the anti-fuse structure on the interval like first conductive lines of the bottom and the second electric conduction of the upper phase. This first conductive line can be the pulley chamber recon layer in which the domain in which the impurity of the integrated circuit board is doped, and the impurity on the domain in which the impurity of the epitaxial layer formed on the substrate is doped or the substrate are doped. And after the contact opening is formed on the connecting area desiring through the above-mentioned thick insulating layer the anti-fuse dielectric layer is deposited on the above-mentioned thick insulating layer and contact opening. The important variable of the anti-fuse structure depends on the material used for this dielectric layer. Subsequently, the second conductive layer is masked on the anti-fuse dielectric layer after depositing the second conductive layer with the normal semiconductor process technology and it etches and it limits and conductivity is formed.

종래의 필드 프로그램가능한 소자(Field programmable devices; FPD) 또는 안티퓨즈구조는 통상 기준 프로그래밍 전압이 15V~30V 인가되면 프로그램되는 동안 약 1msec의 프로그램시간 동안에 약 1mA의 프로그래밍전류를 흐르게 한다. 또한, 이들 종래의 소자는 통상 프로그램되지 않은 상태에서 10MΩ~10GΩ의 오프(off) 저항을 가지며, 10Ω~1000Ω의 온(on) 저항을 갖는다.

While the device (Field programmable devices: FPD) or the anti-fuse structure which is possible with the conventional field program is programmed if the standard programming voltage is applied from the generally with 15V~30V the programmed current of about 1mA is flowed for the program time of about 1msec. Moreover, these conventional devices includes the off resistance of 10MΩ ~10G Ω in the state that is not generally programmed, and the resistance come (on)ing of 10Ω~1000Ω.

여러가지 다양한 안티퓨즈구조가 미합중국 특허 제4,882,611호 및 유럽특허 416,903A2에 개시되어 있다.

The anti-fuse structure which is differently various is disclosed in US4,882,611 A and EP416,903A2.

미합중국 특허 제4,882,611호에 개시된 안티퓨즈구조는 이온주입기술을 이용하여 도핑된 반도체기판 부분의 표면을 비정질환(Amorphous)하여 저항값을 증가시켜 개방(open)효과를 얻고, 고전압을 인가하면 비정질조직이 다시 결정화되어 단락(Short)되는 효과를 얻는 것이다.

The surface of the semiconductor substrate region in which the disclosed anti-fuse structure is doped in US 4,882,611 A using the ion implantation technique is decided on with the amorphous ring (Amorphous) and the resistance value is increased and the opening (open) effect is obtained and if the high voltage is applied, the amorphous structure is crystallized from the again and the effect that becomes with the short circuit (Short) is obtained.

유럽틀허 416,903A2에 개시된 안티퓨즈구조는 안티퓨즈층으로서 비정질실리콘으로 사용하거나, 또는 비정질실리콘층/박막의 유전체막/비정질실리콘층의 적층된 구조를 사용하고 있다.

The disclosed anti-fuse structure uses in the Europe frame emptiness 416,903A2 as the antifuse layer as the amorphous silicon or or the structure of being laminated of the amorphous silicon layer / thin film heredity body film / amorphous silicon layer is used.

제1도 내지 제6도를 참조하여 종래의 PID용 안티퓨즈 형성방법을 설명하면 다음과 같다.

The first is the method for forming the anti-fuse for the conventional PID with reference to the inland sixth drawing, is as follows.

먼저, 제1도를 참조하면, 실리콘기판(1)상에 통상의 MOS공정에 의해 필드산화막(2), 게이트전극(3) 및 소오스/드레인영역

In advance, referring to figure 1, the field oxide film (2), and the gate electrode (3) and source/drain region

GF Exhibit 1124 - 1982/2704

(4)을 형성하고 전면에 절연층(5)을 형성한 후 포토리소그래피 공정에 의해 상기 절연층(5)에 안티퓨즈 콘택을 형성한다.

(4) are formed on the silicon substrate (1) with the normal MOS process and the insulating layer (5) the anti-fuse contact is formed on front after doing the formation with the photolithography process on the insulating layer (5).

이어서 제2도에 도시된 바와 같이 상기 안티퓨즈 콘택에 산화막(6)을 형성한다.

Subsequently, the oxide film (6) is formed on the anti-fuse contact as shown in Figure 2.

다음에 제3도에 도시된 바와 같이 상기 결과물 전면에 불순물에 도핑되지 않은 폴리실리콘(Undoped polysilicon)(7)을 증착한다.

Next, the undoped poly-silicon (Undoped polysilicon) (7) is deposited on the impurity as shown in Figure 3 in the outcome front side.

이어서 제4도에 도시된 바와 같이 포토레지스트(PR)를 도포하고 포토리소그래피공정을 통해 안티퓨즈가 형성될 부분에만 상기 폴리실리콘층(7)이 남도록 패터닝하여 소정 패턴의 폴리실리콘층(8)을 형성한다.

Subsequently, the photoresist (PR) is coated with as shown in Figure 4 and it patterns so that the polysilicon layer (7) remains in the part in which the anti-fuse is formed through the photolithography process and the polysilicon layer (8) of the desired pattern is formed.

다음에 제5도에 도시된 바와 같이 포토레지스트(PR)를 도포하고 포토리소그래피공정을 통해 금속콘택을 형성한다.

Next, the photoresist (PR) is coated with as shown in Figure 5 and the metal contact is formed through the photolithography process.

이어서 제6도에 도시된 바와 같이 포토레지스트를 제거한 후, 상기 결과물 전면에 금속을 증착한 후, 포토리소그래피공정에 의해 금속배선(10)을 형성한다.

Subsequently, after the photoresist is removed as shown in Figure 6 the metal wiring (10) is formed on the outcome front side after depositing the metal with the photolithography process.

상기한 종래의 안티퓨즈 형성방법들에 있어서는, 일반적인 MOS공정에 PID형성공정을 적용할 경우 안티퓨즈콘택 형성을 위한 포토리소그래피공정 및 상기 불순물이 도핑되지 않은 폴리실리콘층(Undoped polysilicon) 패터닝을 위한 포토리소그래피공정등으로 제조공정이 복잡하며, 안티퓨즈층이 산화막/불순물이 도핑되지 않은 폴리실리콘층(Undoped polysilicon)의 구조로 구성되므로 안티퓨즈층 두께의 조절이 불리하며, 불순물이 도핑되지 않은 폴리실리콘층의 추가에 따른 안티퓨즈의 캐패시턴스 변화가 크고 누설전류가 문제가 된다.

It is in the above-described conventional anti-fuse formation methods and the manufacturing process is crowded with the photolithography process for the polysilicon layer (Undoped polysilicon) patterning in which the photolithography process for the anti-fuse contact forming and impurity is not doped in case of applying the PID formation process to the general MOS process etc. and the modulation of the antifuse layer thickness is disadvantageous since the antifuse layer consists of the structure of the polysilicon layer (Undoped polysilicon) in which the oxide film / impurity is not doped and the capacitance variation of the anti-fuse according to the addition of the polysilicon layer in which the impurity is not doped is large and the leakage current becomes a problem.

본 발명은 상술한 문제를 해결하기 위한 것으로, PID 제조공정을 최소한의 포토리소그래피공정에 의해 MOS 공정에 적용할 수 있으며, 금속산화막을 안티퓨즈막질로 사용함으로써 막질의 두께조절 및 누설전류의 감소가 가능한 PID제조방법을 제공하는 것을 그 목적으로 한다.

The object of the invention is to provide the PID manufacturing method in which it can apply the PID manufacturing process to the MOS process to the minimum photolithography process and for resolving the above-described problem the thickness adjustment of the thin film and reduction of the leakage current are possible by using the metal oxide layer as the anti-fuse thin film.

상기 목적을 달성하기 위해 본 발명은 반도체기판상에 하부도전층을 형성하는 공정; 상기 하부도전층상에 절연층을 형성하는 공정; 상기 하부도전층의 소정부분을 노출시키기 위해 상기 절연층에 안티퓨즈 콘택개구부 및 금속 콘택개구부를 동시에 형성하는 공정; 상기 결과물 전면에 금속산화막을 형성하는 공정; 상기 안티퓨즈 콘택영역에만 상기 금속산화막을 남기는 공정; 및 상기 결과물 전면에 금속을 증착한 후 이를 소정패턴으로 패터닝하여 상기 안티퓨즈 콘택영역의 상기 남아 있는 금속산화막의 상부 및 상기 금속 콘택영역상에 상부 도전층을 형성하는 공정으로 이루어진 것을 특징으로 하는 프로그램가능한 접속소자의 제조방법을 제공한다.

To accomplish the above objects, the present invention is to provide the manufacturing method of the programmable connection element consisting of the process of forming the bottom conductive layer on the semiconductor substrate, the process of forming the insulating layer on the bottom conductive layer, the anti-fuse contact opening in the insulating layer and the process of simultaneously forming the metal contact opening part the prescribed part of the bottom conductive layer is exposed, the process of forming the metal oxide layer on the outcome front side, the process of leaving

GF Exhibit 1124 - 1983/2704

the metal oxide layer in the anti-fuse contact area, an d the process of patterning this in the desired pattern after depositing the metal and forming the top conducti ve layer on the outcome front side on the upper portio n of the above-mentioned metal oxide layer remaining o f the anti-fuse contact area and metal contact area.

본 발명의 일실시예에 의하면, 상기 금속산화막은 금속을 증착한 후 산화공정에 의해 상기 금속을 산화시켜 형성한다.

According to a preferred embodiment of the present invention, the metal is oxidized after depositing the me tal with the oxidation process and the metal oxide layer forms.

상기 금속으로는 Ti, Al, Ba, Ge, Sn, Be, Nb 및 Ta중에서 선택한 어느 하나를 사용하여 금속산화막을 형성한다.

The metal oxide layer is formed into the metal among the ti, al, ba, ge, sn, be, nb and Ta using any one chos en.

본 발명의 다른 실시예에 의하면, 상기 금속산화막은 금속가스를 산소플라즈마에 통과시켜 형성한다.

According to the other embodiment of the present invention., the metal gas is passed through in the oxyg en plasma and the metal oxide layer forms.

상기 상부전층은 반도체기판에 형성된 불순물확산영역, 불순물이 도우프된 폴리실리콘층, 폴리사이드층 또는 반도체기판의 도전영역일 수 있다.

The upper portion front layer can be the impurity diffusion region, formed in the semiconductor substrate the polysilicon layer in which the impurity is doped, and the conductive region of the polycide layer or the semi conductor substrate.

본 발명에 의한 PID용 안티퓨즈 제조방법은 PID용 안티퓨즈 콘택과 금속콘택을 동시에 형성하는 공정과 안티퓨즈 막질로서 금속산화막을 형성하는 공정으로 이루어지는 것을 특징으로 한다.

The method for manufacturing anti-fuse for PID according to the invention comprises the anti-fuse con tact for PID and the process of simultaneously forming the metal contact and the process of forming the meta l oxide layer as the anti-fuse thin film.

제7도 내지 제11도를 참조하여 본 발명에 의한 PID용 안티퓨즈 제조방법을 설명하면 다음과 같다.

The seventh is the method for manufacturing anti-fuse for PID according to the invention with reference to th e inland eleventh drawing, is as follows.

먼저, 제7도를 참조하면, 실리콘기판(21)상에 통상의 MOS 공정에 의해 필드산화막(22), 게이트전극(23) 및 소오스/드레인 영역(24)을 형성하고 전면에 절연층(25)을 형성한 후 포토리소그래피공정에 의해 상기 절연층(5)에 안티퓨즈 콘택개구부(26)와 금속콘택개구부(27)를 동시에 형성한다.

In advance, referring to figure 7, the field oxide film (22), and the gate electrode (23) and source/drain regi on (24) are formed on the silicon substrate (21) with t he normal MOS process and the insulating layer (25) th e anti-fuse contact opening (26) and metal contact op ening part (27) is simultaneously formed on front after doing the formation with the photolithography process on the insulating layer (5).

이어서 제8도를 참조하면, 상기 결과물상에 금속층(28)을 얇게 증착한다.

Subsequently, referring to figure 8, the metallic layer (28) the thinly is deposited on the outcome.

다음에 제9도를 참조하면, 산화공정을 진행하여 상기 형성된 금속층을 산화시켜 금속산화막(29)을 형성한다.

Next, referring to figure 9, the oxidation process is progressed and the above-mentioned formed metallic la yer is oxidized and the metal oxide layer (29) is formed.

이어서 제10도를 참조하면, 포토리소그래피공정을 통해 상기 안티퓨즈 콘택부분에만 상기 금속산화막(29)을 남기고 나머지 부분에 형성된 금속산화막은 제거한다.

Subsequently, referring to figure 10, the metal oxide layer leaving the metal oxide layer (29) in the anti-fuse contact portion through the photolithography process and is formed in the remaining part removes.

다음에 제11도를 참조하면, 상기 결과물 전면에 금속을 증착한 후 이를 포토리소그래피공정에 의해 소정패턴으로 패터닝하여 금속배선(30)을 형성한다.

Next, referring to figure 11, this is patterned in the desired pattern after depositing the metal with the pho tolithography process and the metal wiring (30) is form ed on the outcome front side.

상기한 바와 같이 본 발명은 안티퓨즈콘택과 금속패턴을 동시

As described above, the manufacturing process can be

GF Exhibit 1124 - 1984/2704

에 형성함으로써 제조공정을 단순화시킬 수 있다. 또한, 안티퓨즈 산화막/불순물이 도핑되지 않은 폴리실리콘으로 된 안티퓨즈구조를 금속산화막으로 된 안티퓨즈구조로 바꿈으로써 안티퓨즈막두께의 조절이 용이하게 되며, 누설전류를 감소시키는 효과가 생긴다.

simplified since the invention simultaneously forms the anti-fuse contact and metal pattern. Moreover, by cha nging the anti-fuse structure consisting of the poly-sili con in which the anti-fuse oxide film / impurity is not d oped into the anti-fuse structure consisting of the met al oxide layer the modulation of the anti-fuse film thick ness is facilitated and the effect reducing the leakage current is generated.

이하, 본 발명의 일실시예를 도면에 참조하여 설명하면 다음과 같다.

Hereinafter, a preferred embodiment of the present invention is made to be equal to the next it refers in dr awing and it illustrates.

제7도 내지 제11도에 본 발명에 의한 PID용 안티퓨즈 제조방법을 도시하였다.

The seventh showed the method for manufacturing anti-fuse for PID according to the invention in the inlan d eleventh drawing.

먼저, 제7도에 도시한 바와 같이 실리콘기판(21)상에 통상의 MOS공정에 의해 필드산화막(22), 게이트 전극(23) 및 소오스/드레인영역(24)을 형성하고 전면에 절연층(25)으로서, 예컨대 산화막을 형성한 후, 포토리소그래피공정에 의해 상기 산화막(5)에 안티퓨즈 콘택개구부(26)와 금속콘택개구부(27)를 동시에 형성한다.

In advance, the field oxide film (22), and the gate electrode (23) and source/drain region (24) are formed on the silicon substrate (21) with the normal MOS proc ess and it as shown in Figure 7 is the insulating layer (25) in the front side and for example, the oxide film th e anti-fuse contact opening (26) and metal contact op ening part (27) is simultaneously formed after doing the formation with the photolithography process on the oxi de film (5).

이어서 제8도에 도시한 바와 같이 상기 결과물상에 금속층(28)으로서, 예컨대 Ti, Al, Sn, Ta, Ba, Ge, Be, Nb 중에서 선택한 어느 하나를 100Å~500Å 정도의 두께로 얇게 증착한다.

Subsequently, as as shown in Figure 8, the metallic layer (28) on the outcome, any one chosen the thinly i s deposited on for example by the thickness of about 1 00Å~500Å among the ti, al, sn, ta, ba, ge, be, nb.

다음에 제9도에 도시한 바와 같이 450℃~800℃의 온도범위에서 산화공정을 진행하여 상기 형성된 금속층을 산화시켜 금속산화막(29)을 형성한다.

Next, the oxidation process is progressed in the temperature range of 450℃~800℃ and the above-menti oned formed metallic layer is oxidized and as shown in Figure 9, the metal oxide layer (29) is formed.

이때, 상기 금속산화막을 형성하는 공정을 제8도 및 제9도에 도시한 바와 같이 금속층을 먼저 형성한 후 이를 산화시키는 공정을 이용하지 않고, 금속가스를 산소플라즈마에 통과시켜 금속산화물을 형성할 수도 있다.

Then, as shown in Figure 8 and Figure 9 the process of forming the metal oxide layer, the impartiality of oxidizi ng this the metallic layer after doing the formation in a dvance is not used and the metal gas is passed throug h in the oxygen plasma and the metal oxide can be for med.

이어서 제10도에 도시한 바와 같이 포토리소그래피공정을 통해 상기 안티퓨즈 콘택부분에만 상기 금속산화막(29)을 남기고 나머지 부분에 형성된 금속산화막은 제거한다.

Subsequently, as shown in Figure 10, the metal oxide layer leaving the metal oxide layer (29) in the anti-fuse contact portion through the photolithography process and is formed in the remaining part removes.

다음에 제11도에 도시된 바와 같이 상기 결과물을 전면에 금속을 증착한 후 이를 포토리소그래피공정에 의해 소정패턴으로 패터닝하여 금속배선(30)을 형성한다.

Next, this is patterned in the desired pattern after depositing the metal with the photolithography process and the outcome the metal wiring (30) is formed as sho wn in Figure 11 on front.

상기 금속산화막을 Al을 이용하여 형성할 경우, 상술한 바와 하나의 챔버(Chamber)내에서 산소플라즈마에 Al가스를 흘려주어 Al2O3의 금속산화막을 형성한 후, 동일한 챔버내에서 타갯(Target)만 변경하여(인시이튜(in-situ)로 Al(1% Si+0.5% Cu를 함유하는)을 증착함으로써 금속배선을 형성할 수 있으므로 현재의 스퍼터(Sputter)장비에서 쉽게 적용시킬 수 있으며, 금속산화막 형성후에 행해지는 후속공정인 금속배선의 형성을 하나의 장비내에서 용이하게 형성할 수 있다.

When the metal oxide layer is formed using the Al since the metal wiring can be formed by the Al gas being spil t on the oxygen plasma in and above-described one ch amber and the rudder get (Target) changing the metal oxide layer of the Al 2 O 3 after doing the formation in the same chamber and depositing the Al (1% Si+0.5% Cu is contained) by situ (in-situ) it easily can apply in t he current sputtering equipment and the formation of t he metal wiring which is the subsequent processes perf ormed after the metal oxide layer formation can be easi

GF Exhibit 1124 - 1985/2704

ly formed in one equipment.

상술한 본 발명에 의하면, 안티퓨즈 콘택과 금속콘택을 동시에 형성함으로써 이를 각각 형성하던 종래방법 보다 공정을 단순화시킬 수 있으며, 종래의 산화막/불순물이 도핑되지 않은 폴리실리콘구조로 이루어진 안티퓨즈구조를 금속산화막으로 대체함으로써 안티퓨즈막의 두께조절이 용이하게 되며 누설전류가 감소하게 된다. 특히, Al2O3와 같은 금속산화막은 Na+이온의 확산에 강한 배리어(barrier)로 작용하여 소자를 신뢰성을 향상시킨다.

According to the present invention described in the above, the process can be simplified than the anti-fuse contact and the conventional method which forms this by simultaneously forming the metal contact and by replacing the anti-fuse structure consisting of the polysilicon structure in which the conventional oxide film / impurity is not doped with the metal oxide layer the thickness adjustment of the anti-fuse film is facilitated and the leakage current reduces. Especially, the metal oxide layer like the Al 2 O 3 acts on the diffusion of the Na + ion on the strong barrier and the device the reliability is improved.

이상, 상술한 바와 같이 본 발명에 의하면, 최소한의 포토리소그래피공정에 의해 PID용 안티퓨즈를 형성할 수 있으며, 금속산화막을 안티퓨즈막으로 사용함으로써 막질의 두께를 조절할 수 있고 누절전류를 감소시킬 수 있어 안정된 소자동작을 얻을 수 있다.

The over, as described above, the anti-fuse for PID by the minimum photolithography process is used as the anti-fuse film the metal oxide layer it can form. And the component performance controlling the thickness of the thin film and reduce the leakage current and is stabilized can be obtained.

Disclaimer

본 문서는 특허 및 과학기술문헌 전용의 첨단 자동번역 시스템을 이용해 생성되었습니다. 따라서 부분적으로 오역의 가능성이 있으며, 본 문서를 자격을 갖춘 전문 번역가에 의한 번역물을 대신하는 것으로 이용되어서는 안 됩니다. 시스템 및 네트워크의 특성때문에 발생한 오역과 부분 누락, 데이터의 불일치등에 대하여 본원은 법적인 책임을 지지 않습니다. 본 문서는 당사의 사전 동의 없이 권한이 없는 일반 대중을 위해 DB 및 시스템에 저장되어 재생, 복사, 배포될 수 없음을 알려드립니다.
(The document produced by using the high-tech machine translation system for the patent and science & technology literature. Therefore, the document can include the mistranslation, and it should not be used as a translation by a professional translator. We hold no legal liability for inconsistency of mistranslation, partial omission, and data generated by feature of system and network. We would like to inform you that the document cannot be regenerated, copied, and distributed by being stored in DB and system for unauthorized general public without our consent.)

GF Exhibit 1124 - 1986/2704

(19) 대한민국특허청(KR)
(12) 공개특허공보(A)

(51) Int. Cl.[6]
H01L 21/28

(11) 공개번호 특1997-0030333
(43) 공개일자 1997년06월26일

(21) 출원번호 특1995-0039691
(22) 출원일자 1995년11월03일

(71) 출원인 현대전자산업 주식회사 김주용
경기도 이천군 부발읍 아미리 산 136-1
(72) 발명자 김헌도
경기도 고양시 고열1동 50번지 강선 한양아파트 603동 201호
(74) 대리인 이권희, 이정훈

심사청구 : 없음

(54) 반도체소자의 도전 배선 콘택 제조방법

요약

본 발명은 반도체소자의 도전배선 콘택 제조방법에 관한 것으로서, 소정의 기판상에 형성되어있는 하측 도전배선을 노출시키는 콘택홀을 구비하는 층간절연막을 형성하고, 전처리 공정 없이 장벽금속층인 Ti층을 형성하며 소정의 온도에서 열처리하여 하측 금속층과 Ti층의 사이에 타이타늄 산화막을 형성한 후, 상기 콘택홀을 통하여 하측 도전배선과 연결되는 상측 도전배선을 형성하였으므로, 타이타늄 산화막이 확산방지막의 일부가 되어 확산 방지 효과가 증가되고, 콘택 저항이 감소되며, 하측 도전배선 표면에 형성되는 산화막이 타이타늄 산화막의 일부로 전환되므로 전처리 공정이 불필요하여 공정수율을 향상시킬 수 있다.

대표도

도1c

명세서

[발명의 명칭]

반도체소자의 도저 배선 콘택 제조방법

[도면의 간단한 설명]

제1c도 내지 제1d도는 본 발명의 제1실시예에 따른 반도체소자의 도전배선 콘택 제조공정도.

"본 내용은 요부공개 건이므로 전문내용을 수록하지 않았음"

(57) 청구의 범위

청구항 1

소정의 기판상에 하측 도전배선을 형성하는 공정과, 상기 하측 도전배선에서 콘택으로 예정되어있는 부분을 노출시키는 콘택홀을 구비하는 층간절연막을 형성하는 공정과, 상기 구조의 전표면에 Ti 층을 포함하는 장벽금속층을 형성하는 공정과, 상기 구조의 기판을 열처리하여 상기 노출된 하측 도전배선과 Ti층의 사이에 타이타늄 산화막을 형성하는 공정과, 상기 장벽금속층상에 주금속층을 형성하는 공정과, 상기 주금속층과 장벽금속층을 패턴닝하여 상측 도전배선을 형성하는 공정을 구비하는 반도체소자의 도전배선 콘택 제조방법.

청구항 2

제1항에 있어서, 상기 하측 도전배선이 반도체기판이나 하측 금속배선인 것을 특징으로 하는 반도체소자의 도전배선 콘택 제조방법.

청구항 3

제2항에 있어서, 상기 하측 도전배선이 반도체기판인 경우 열처리 공정시 콘택홀 부분에 형성된 자연산화막이 타이타늄 산화막의 일부로 변환하는 것을 특징으로 하는 반도체소자의 도전배선 콘택 제조방법.

청구항 4

제1항 또는 제3항에 있어서, 상기 하측 도전배선이 반도체기판인 경우 장벽 금속층을 Ti층/TiN층의 적층

GF Exhibit 1124 - 1987/2704

구조로 형성하는 것을 특징으로 하는 반도체소자의 도전배선 콘택 제조방법.

청구항 5

제2항에 있어서,상기 하측 도전배선이 하측 금속배선으로서 Al 계열 합금층인 경우 열처리 공정시 콘택홀 부분에 형성된 Al 산화막이 타이타늄 산화막의 일부로 변환되는 것을 특징으로 하는 반도체소자의 도전배선 콘택 제조방법.

청구항 6

제1항 또는 제2항에 있어서, 상기 하측 도전배선이 하측 도전배선으로서 Al 계열 합금층인 경우 장벽 금속층을 Ti층의 단층으로 형성하는 것을 특징으로 하는 반도체소자의 도전배선 콘택 제조방법.

청구항 7

제1항에 있어서, 상기 열처리 공정을 튜브나 급속열처리기에서 400~700℃ 온도에서 실시하는 것을 특징으로 하는 반도체소자의 도전배선 콘택 제조방법.

청구항 8

제1항에 있어서, 상기 타이타늄 산화막을 20~100Å 두께로 형성하는 것을 특징으로 하는 반도체소자의 도전배선 콘택 제조방법.

청구항 9

제1항에 있어서, 상기 콘택홀내에 장벽금속층 상에 콘택 플러그를 형성하고 상측 도전배선을 형성하는 것을 특징으로 하는 반도체소자의 도전배선 콘택 제조방법.

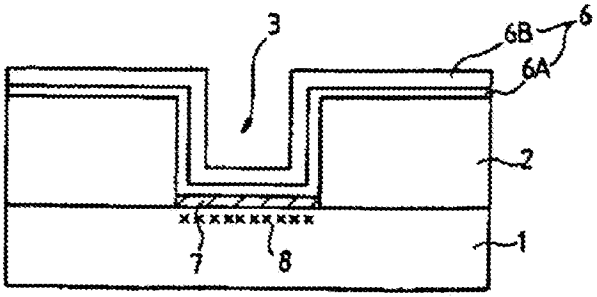
청구항 10

제9항에 있어서, 상기 콘택 플러그를 선택적 WOI나 W-플러그로 형성하는 것을 특징으로 하는 반도체소자의 도전배선 콘택 제조방법.

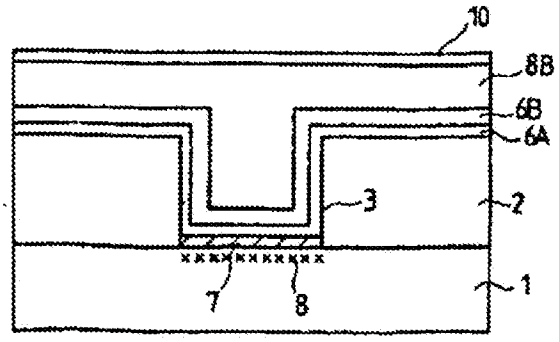
※ 참고사항 : 최초출원 내용에 의하여 공개하는 것임.

도면

도면1c



도면1d



GF Exhibit 1124 - 1988/2704

Unexamined Patent Publication(A)

Bibliographic Data

Int.Cl.	H01L 21/768
Application No.	1019950039691
Application Date	19951103
Unexamined Publication No.	1019970030333
Unexamined Publication Date	19970626
Requested Date of Examination	19951103
Agent.	LEE, Jung Hoon | HANYANG PATENT FIRM
Inventor	Heon-Do Kim
Applicant	SK hynix Inc.

발명의 명칭

반도체소자의도전배선콘택제조방법

Title of Invention

Semiconductor device intention total wiring contact manufacturing method.

요약

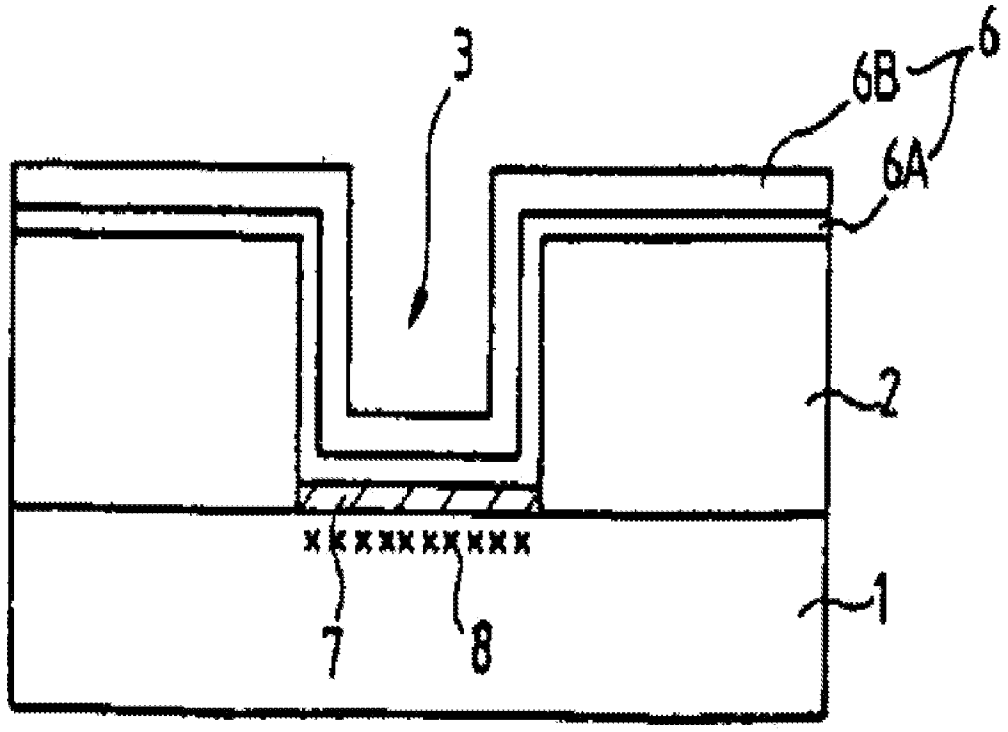
본 발명은 반도체소자의 도전배선 콘택 제조방법에 관한 것으로서, 소정의 기판상에 형성되어있는 하측 도전배선을 노출시키는 콘택홀을 구비하는 층간절연막을 형성하고, 전처리 공정없이 장벽금속층인 Ti층을 형성하며 소정의 온도에서 열처리하여 하측 금속층과 Ti층의 사이에 타이타늄 산화막을 형성한 후, 상기 콘택홀을 통하여 하측 도전배선과 연결되는 상측 도전배선을 형성하였으므로, 타이타늄 산화막이 확산방지막의 일부가 되어 확산 방지 효과가 증가되고, 콘택 저항이 감소되며, 하측 도전배선 표면에 형성되는 산화막이 타이타늄 산화막의 일부로 전환되므로 전처리 공정이 불필요하여 공정수율을 향상시킬 수 있다.

Abstract

The invention relates to the conductor wiring making method of contact hole of the semiconductor device. And the inter-layer insulating film equipped with the contact hole exposing the lower side conductor wiring formed on the predetermined substrate was formed and while forming the Ti layer which was the barrier metal layer without the fabrication process it heat-treated at a temperature of the predetermined and the titanium oxide film the upper side conductor wiring connected to the lower side conductor wiring through the contact hole was formed between the lower side metallic layer and Ti layer after doing the formation. Therefore the part of the diffusion barrier becomes the titanium oxide film and the scattering prevention effect is increased and the contact resistance is reduced and since the oxide film formed in the lower side conductor wiring surface is converted to the part of the titanium oxide film the fabrication process is unnecessary and the processing yield can be improved.

대표도면(Representative drawing)

GF Exhibit 1124 - 1989/2704



청구의 범위

청구 1항:

소정의 기판상에 하측 도전배선을 형성하는 공정과, 상기 하측 도전배선에서 콘택으로 예정되어있는 부분을 노출시키는 콘택홀을 구비하는 층간절연막을 형성하는 공정과, 상기 구조의 전표면에 Ti 층을 포함하는 장벽금속층을 형성하는 공정과, 상기 구조의 기판을 열처리하여 상기 노출된 하측 도전배선과 Ti층의 사이에 타이타늄 산화막을 형성하는 공정과, 상기 장벽금속층상에 주금속층을 형성하는 공정과, 상기 주금속층과 장벽금속층을 패턴닝하여 상측 도전배선을 형성하는 공정을 구비하는 반도체소자의 도전배선 콘택 제조방법.

청구 2항:

제1항에 있어서, 상기 하측 도전배선이 반도체기판이나 하측 금속배선인 것을 특징으로 하는 반도체소자의 도전배선 콘택 제조방법.

청구 3항:

제2항에 있어서, 상기 하측 도전배선이 반도체기판인 경우 열처리 공정시 콘택홀 부분에 형성된 자연산화막이 타이타늄 산화막의 일부로 변환하는 것을 특징으로 하는 반도체소자의 도전배선 콘택 제조방법.

Scope of Claims

Claim 1:

The conductor wiring making method of contact hole of the semiconductor device which comprises the process of forming the lower side conductor wiring on the predetermined substrate, the above-mentioned exposed lower side conductor wiring the substrate of the process, of forming the inter-layer insulating film equipped with the contact hole exposing the part scheduled for the contact in the lower side conductor wiring and the process, of forming the barrier metal layer including the Ti layer on the blanket of the structure and structure is heat-treated, and the process, of forming the titanium oxide film between the Ti layer and the process, of forming the main metal layer on the barrier metal layer and the process of patterning the main metal layer and barrier metal layer and forming the upper side conductor wiring.

Claim 2:

As for claim 1, the conductor wiring making method of contact hole of the semiconductor device in which the lower side conductor wiring is the semiconductor substrate or the lower side metal wiring.

Claim 3:

As for claim 2, the conductor wiring making method of contact hole of the semiconductor device which the native oxide film formed in the thermal process in the contact hole portion converts into the part of the titanium oxide film in case the lower side conductor wiring is the

GF Exhibit 1124 - 1990/2704

semiconductor substrate.

청구 4항:

제1항 또는 제3항에 있어서, 상기 하측 도전배선이 반도체기판인 경우 장벽 금속층을 Ti층/TiN층의 적층구조로 형성하는 것을 특징으로 하는 반도체소자의 도전배선 콘택 제조방법.

Claim 4:

As for claim 1 or 3, the conductor wiring making method of contact hole of the semiconductor device which forms the barrier metal layer into the laminating structure of the Ti layer / TiN layer in case the lower side conductor wiring is the semiconductor substrate.

청구 5항:

제2항에 있어서,상기 하측 도전배선이 하측 금속배선으로서 Al 계열 합금층인 경우 열처리 공정시 콘택홀 부분에 형성된 Al 산화막이 타이타늄 산화막의 일부로 변환되는 것을 특징으로 하는 반도체소자의 도전배선 콘택 제조방법.

Claim 5:

As for claim 2, the conductor wiring making method of contact hole of the semiconductor device in which the Al oxide film formed in the thermal process in the contact hole portion is transformed to the part of the titanium oxide film in case the lower side conductor wiring is the Al series alloy layer as the lower side metal wiring.

청구 6항:

제1항 또는 제2항에 있어서, 상기 하측 도전배선이 하측 도전배선으로서 Al 계열 합금층인 경우 장벽 금속층을 Ti층의 단층으로 형성하는 것을 특징으로 하는 반도체소자의 도전배선 콘택 제조방법.

Claim 6:

As for claim 1 or 2, the conductor wiring making method of contact hole of the semiconductor device in which the lower side conductor wiring forms the barrier metal layer into the single story of the Ti layer as the lower side conductor wiring in case of being the Al series alloy layer.

청구 7항:

제1항에 있어서, 상기 열처리 공정을 튜브나 급속열처리기에서 400~700℃ 온도에서 실시하는 것을 특징으로 하는 반도체소자의 도전배선 콘택 제조방법.

Claim 7:

As for claim 1, the conductor wiring making method of contact hole of the semiconductor device performing the thermal process in the tube or the rapid thermal processor in 400~700℃ temperature.

청구 8항:

제1항에 있어서, 상기 타이타늄 산화막을 20~100Å 두께로 형성하는 것을 특징으로 하는 반도체소자의 도전배선 콘택 제조방법.

Claim 8:

As for claim 1, the conductor wiring making method of contact hole of the semiconductor device forming the titanium oxide film into 20~100Å thickness.

청구 9항:

제1항에 있어서, 상기 콘택홀내에 장벽금속층 상에 콘택 플러그를 형성하고 상측 도전배선을 형성하는 것을 특징으로 하는 반도체소자의 도전배선 콘택 제조방법.

Claim 9:

As for claim 1, the conductor wiring making method of contact hole of the semiconductor device forming the contact plug within the contact hole on the barrier metal layer and forms the upper side conductor wiring.

청구 10항:

제9항에 있어서, 상기 콘택 플러그를 선택적 W이나 W-플러그로 형성하는 것을 특징으로 하는 반도체소자의 도전배선 콘택 제조방법.

Claim 10:

As for claim 9, the conductor wiring making method of contact hole of the optional W or the semiconductor device formed into the W- plug the contact plug.

상세설명

Detailed Description

[발명의 명칭]

반도체소자의 도저 배선 콘택 제조방법

[Title of invention]

The dozer wiring making method of contact hole of the semiconductor device.

[도면의 간단한 설명]

[Brief description of drawings]

GF Exhibit 1124 - 1991/2704

제1c도 내지 제1d도는 본 발명의 제1실시예에 따른 반도체소자의 도전배선 콘택 제조공정도.	To Figure 1c. And figure 1d is a conductor wiring process of producing contact of the semiconductor device according to the first preferred embodiment of the invention.
#34#본 내용은 요부공개 건이므로 전문내용을 수록하지 않았음#34#	The " the technical content was not given mention of since the " this content was the main part disclosure gun.

Disclaimer

본 문서는 특허 및 과학기술문헌 전용의 첨단 자동번역 시스템을 이용해 생성되었습니다. 따라서 부분적으로 오역의 가능성이 있으며, 본 문서를 자격을 갖춘 전문 번역가에 의한 번역물을 대신하는 것으로 이용되어서는 안 됩니다. 시스템 및 네트워크의 특성때문에 발생한 오역과 부분 누락, 데이터의 불일치등에 대하여 본원은 법적인 책임을 지지 않습니다. 본 문서는 당사의 사전 동의 없이 권한이 없는 일반 대중을 위해 DB 및 시스템에 저장되어 재생, 복사, 배포될 수 없음을 알려드립니다.
(The document produced by using the high-tech machine translation system for the patent and science & technology literature. Therefore, the document can include the mistranslation, and it should not be used as a translation by a professional translator. We hold no legal liability for inconsistency of mistranslation, partial omission, and data generated by feature of system and network. We would like to inform you that the document cannot be regenerated, copied, and distributed by being stored in DB and system for unauthorized general public without our consent.)

GF Exhibit 1124 - 1992/2704

(19) 대한민국특허청(KR)
(12) 공개특허공보(A)

(11) 공개번호 특1998-024649
(43) 공개일자 1998년07월06일

(51) 국제분류코드
H01L 29/78 (2006.01)

(21) 출원번호 특1997-047286

(22) 출원일자 1997년09월13일

(30) 우선권주장 96-244395
96-314551
1996년09월17일
1996년11월26일
일본(JP) 일본(JP)

(71) 출원인
모리시다 요이치
마쯔시다 덴키 산교 가부시키가이샤
일본국 오사카후 가도마시 오아자가도마 1006반지, 일본

(72) 발명자
구보 미노루
일본국 미에켄 나바리시 기료가오카 니시이치반쵸 125반지, 일본
노자와 가쓰야
일본국 오사카후 오사카시 히라노쿠 히라노히가시 1-9-19, 일본
스즈키 마사카쓰
일본국 오사카후 가타노시 묘켄자카 6-21-203, 일본
우에노야마 다케시
일본국 교토후 쓰즈키군 다나베쵸 오아자쿠사와치 고아자한쇼와리 42-1, 일본
구마부치 야스히토
일본국 오사카후 도요나카시 히가시토요나카쵸 3-23-에이-304, 일본

(74) 대리인
김영철

(77) 심사관
없음

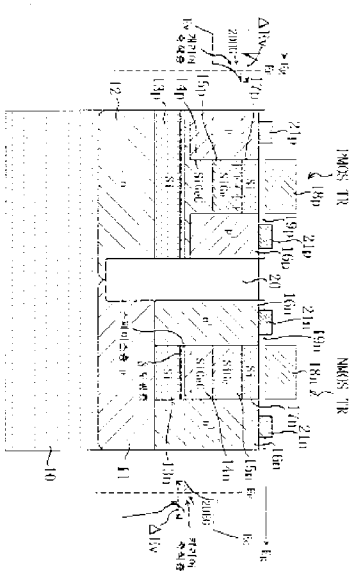
전체 청구항 수 : 총 37 항

(54) 반도체 장치 및 그 제조방법

(57) 요 약

캐리어의 이동도가 높고, 결정 결함이 적은 채널을 갖는 전계 효과 트랜지스터를 구비한 반도체 장치를 제공하기 위하여, Si 기판(10) 상의 NMOS 트랜지스터에 있어서, Si 층(13n), SiGeC 층(14n)이 형성되어 있다. 이 SiGeC 층(14n)과 Si 층(13n)의 헤테로 경계면에 존재하는 전도대의 불연속부를 이용한 캐리어 축적층이 형성되어 있고, 이 캐리어 축적층을 채널로서 전자가 주행하며, SiGeC 층(14n)은 실리콘에 비교해서 전자의 이동도가 크고, NMOS 트랜지스터의 동작속도도 커지며, PM0S 트랜지스터의 정공이 주행하는 채널은, SiGe 층(15p)과 Si 층(17p)의 경계면에 생기는 가전자대의 불연속부를 이용하여 형성되어 있으므로, SiGe 층도 Si 층에 비교해서 정공의 이동도가 크고, 상기 PMOS 트랜지스터의 동작속도도 커지게 된다.

대 표 도 - 도 1



This Facsimile Page has been artificially created from KIPO data.

GF Exhibit 1124 - 1993/2704

청구의 범위

청구항 1

반도체 기판의 일부에 형성되어 게이트 전극과 소스□드레인 영역 및 해당 소스□드레인 영역 사이의 채널 영역을 갖는 전계 효과 트랜지스터를 구비하고 있는 반도체 장치에 있어서,

상기 채널영역에는

Si 층과,

상기 Si 층에 근접하여 형성되고 C의 조성비 y가 0.01□0.03인 $Si_{1-x-y}Ge_xC_y$ 층 ($0 \leq x \leq 1$, $0 y \leq 1$)이 설치되고,

$Si_{1-x-y}Ge_x$ C_y층 내에서의 상기 Si 층에 근접한 영역에는 캐리어 축적층이 형성되어 있는 것을 특징으로 하는 반도체 장치.

청구항 2

제 1 항에 있어서,

상기 $Si_{1-x-y}Ge_xC_y$ 층의 각 원소의 조성비는, 상기 $Si_{1-x-y}Ge_xC_y$ 층과 상기 Si 층 이 격자 정합하는 조성비로 조정되는 것을 특징으로 하는 반도체 장치.

청구항 3

제 1 항에 있어서,

상기 $Si_{1-x-y}Ge_xC_y$ 층은 상기 Si 층보다도 작은 격자 정수를 갖고, 또한 격자 완화를 발생하지 않는 막 두께를 갖는 것을 특징으로 하는 반도체 장치.

청구항 4

제 1 항 내지 제 3 항에 있어서,

상기 반도체 기판상에 형성되어 단일 조성의 반도체층을 채널 영역으로 하는 M0S 트랜지스터를 추가로 구비하는 것을 특징으로 하는 반도체 장치.

청구항 5

제 1 항 내지 제 3 항 중 어느 한 항에 있어서,

상기 캐리어 축적층에 축적되는 캐리어는 부의 캐리어인 것을 특징으로 하는 반도체 장치.

GF Exhibit 1124 - 1994/2704

청구항 6

제 4 항에 있어서,

상기 캐리어 축적층에 축적되는 캐리어는 부의 캐리어인 것을 특징으로 하는 반도체 장치.

청구항 7

제 1 항 내지 제 3 항 및 제 6 항 중 어느 한 항에 있어서,

상기 Si 층 내의 상기 $Si_{1-x-y}Ge_xC_y$ 층에 근접한 영역에는 상기 캐리어 축적층에 캐리어를 공급하기 위한 캐리어 공급층을 추가로 설치하는 것을 특징으로 하는 반도체 장치.

청구항 8

제 4 항에 있어서,

상기 Si 층 내의 상기 $Si_{1-x-y}Ge_xC_y$ 층에 근접한 영역에는 상기 캐리어 축적층에 캐리어를 공급하기 위한 캐리어 공급층을 추가로 설치하는 것을 특징으로 하는 반도체 장치.

청구항 9

제 5 항에 있어서,

상기 Si 층 내의 상기 $Si_{1-x-y}Ge_xC_y$ 층에 근접한 영역에는 상기 캐리어 축적층에 캐리어를 공급하기 위한 캐리어 공급층을 추가로 설치하는 것을 특징으로 하는 반도체 장치.

청구항 10

제 1 항에 있어서,

상기 캐리어 축적층에 축적되는 캐리어는 부의 캐리어이고,

상기 반도체 기판의 다른 부분에 형성되어 게이트 전극과, 소스□드레인 영역과 이 소스□드레인 영역 사이의 채널영역을 갖는 또 하나의 전계 효과 트랜지스터를 구비하며,

상기 또 하나의 전계 효과 트랜지스터의 채널영역은,

제 2 Si 층과,

상기 제 2 Si 층에 근접하여 형성된 SiGe 층을 구비하고,

상기 SiGe 내에서의 상기 제 2 Si 층에 근접한 영역에는, 정의 캐리어를 축적하기 위하여 제 2 캐리어 축적층이 형성되는 것을 특징으로 하는 반도체 장치.

청구항 11

제 1 항에 있어서,

상기 $Si_{1-x-y}Ge_xC_y$층은 양자 우물 영역으로 되어있는 것을 특징으로 하는 반도체 장치.

청구항 12

제 10 항에 있어서,

상기 SiGe 층은 양자 우물 영역으로 되어있는 것을 특징으로 하는 반도체 장치.

청구항 13

제 1 항 내지 제 3 항, 제 6 항 및 제 8 항 내지 제 12 한 중 어느 한 항에 있어서,

상기 소스□드레인 영역은 제 1 반도체층과, 이 1 반도체층보다 큰 밴드 갭을 갖는 제 2 반도체층을 갖고,

상기 제 1 반도체층의 바로 위에 형성된 저저항의 도체막으로 된 소스□드레인 콘택트층을 추가로 구비하는 것을 특징으로 하는 반도체 장치.

청구항 14

제 4 항에 있어서,

상기 소스□드레인 영역은 제 1 반도체층과, 이 1 반도체층보다 큰 밴드 갭을 갖는 제 2 반도체층을 갖고,

상기 제 1 반도체층의 바로 위에 형성된 저저항의 도체막으로 된 소스□드레인 콘택트층을 추가로 구비하는 것을 특징으로 하는 반도체 장치.

청구항 15

제 5 항에 있어서,

상기 소스□드레인 영역은 제 1 반도체층과, 이 1 반도체층보다 큰 밴드 갭을 갖는 제 2 반도체층을 갖고,

상기 제 1 반도체층의 바로 위에 형성된 저저항의 도체막으로 된 소스□드레인 콘택트층을 추가로 구비하는 것을 특징으로 하는 반도체 장치.

청구항 16

제 7 항에 있어서,

상기 소스□드레인 영역은 제 1 반도체층과, 이 1 반도체층보다 큰 밴드 갭을 갖는 제 2 반도체층을 갖고,

상기 제 1 반도체층의 바로 위에 형성된 저저항의 도체막으로 된 소스□드레인 콘택트층을 추가로 구비하는 것을 특징으로 하는 반도체 장치.

청구항 17

반도체 기판의 일부에 형성되어 게이트 전극과, 소스□드레인 영역과 이 소스□드레인 영역 사이의 채널영역을 갖는 전계 효과 트랜지스터를 구비하고,

상기 채널영역에는,

제 1 의 Si 층과,

상기 Si 층에 인접하여 형성된 제 1 의 $Si_{1-x-y}Ge_xC_y$층(0≤x≤1, Oy≤1)과,

제 2 의 Si 층과,

상기 제 2 의 Si 층에 인접하여 형성되고 상기 제 1 의 $Si_{1-x-y}Ge_xC_y$층과는 다른 밴드 갭을 갖는 제 2 의 $Si_{1-x-y}Ge_xC_y$층(0≤x≤1,0≤y≤1)이 설치되며,

상기 제 1 $Si_{1-x-y}Ge_xC_y$층 내에서의 상기 제 1 의 Si 층에 근접한 영역과, 상기 제 2 의 $Si_{1-x-y}Ge_xC_y$층 안에서의 상기 제 2 의 Si 층에 근접한 영역과는 서로 다른 도전형의 캐리어를 폐쇄하기 위한 제 1 및 제 2 캐리어 축적층이 각각 형성되는 것을 특징으로 하는 반도체 장치.

청구항 18

제 17 항에 있어서,

상기 제 2 $Si_{1-x-y}Ge_xC_y$층에 있어서의 C의 조성비 y는 0인 것을 특징으로 하는 반도체 장치.

청구항 19

제 17 항에 있어서,

상기 반도체 기판상에 형성되어 단일조성의 반도체층을 채널영역으로 하는 M0S 트랜지스터를 추가로 구비하는 것을 특징으로 하는 반도체 장치.

청구항 20

제 17 항에 있어서,

상기 제 1 의 $Si_{1-x-y}Ge_xC_y$층에 있어서의 C의 조성비 y는, 0.01□0.03인 것을 특징으로 하는 반도체 장치.

GF Exhibit 1124 - 1997/2704

청구항 21

제 17 항에 있어서,

상기 제 1 의 $Si_{1-x-y}Ge_xC_y$층의 각 원소의 조성비는, 상기 제 1 의 $Si_{1-x-y}Ge_xC_y$층과 상기 제 1 Si 층이 격자 정합하는 조성비로 조정되어 있는 것을 특징으로 하는 반도체 장치.

청구항 22

제 17 항에 있어서,

상기 제 1 의 $Si_{1-x-y}Ge_xC_y$층은 상기 제 1 의 Si 층의 격자정수보다 작은 격자정수를 갖고, 또한 격자완화를 일으키지 않는 막 두께를 갖는 것을 특징으로 하는 반도체 장치.

청구항 23

제 17 항 내지 제 22 항 중 어느 한 항에 있어서,

상기 제 1 캐리어 축적층에 축적되는 캐리어는 부의 캐리어이고,

상기 제 2 캐리어 축적층에 축적되는 캐리어는 정의 캐리어인 것을 특징으로 하는 반도체 장치.

청구항 24

제 17 항 내지 제 22 항 중 어느 한 항에 있어서,

상기 제 1 의 Si 층 내에서의 상기 제 1 의 $Si_{1-x-y}Ge_xC_y$층에 근접한 영역에는, 상기 제 1 캐리어 축적층에 캐리어를 공급하기 위한 캐리어 공급층이 추가로 형성되는 것을 특징으로 하는 반도체 장치.

청구항 25

제 23 항에 있어서,

상기 제 1 의 Si 층 내에서의 상기 제 1 의 $Si_{1-x-y}Ge_xC_y$층에 근접한 영역에는, 상기 제 1 캐리어 축적층에 캐리어를 공급하기 위한 캐리어 공급층이 추가로 형성되는 것을 특징으로 하는 반도체 장치.

청구항 26

제 17 항에 있어서,

상기 제 1 및 제 2 의 $Si_{1-x-y}Ge_xC_y$층 중 적어도 어느 한쪽의 $Si_{1-x-y}Ge_xC_y$층은 양자 우물 영역으로 되어있는 것을 특징으로 하는 반도체 장치.

GF Exhibit 1124 - 1998/2704

청구항 27

제 17 항 내지 제 22 항, 제 25 항 및 제 26 항 중 어느 한 항에 있어서,

상기 제 1 및 제 2 의 $Si_{1-x-y}Ge_xC_y$층 중 위쪽에 형성된 $Si_{1-x-y}Ge_xC_y$층의 바로 위에 형성된 저저항의 도체막으로 된 소스□드레인 콘택트층을 추가로 구비하는 것을 특징으로 하는 반도체 장치.

청구항 28

제 23 항에 있어서,

상기 제 1 및 제 2 의 $Si_{1-x-y}Ge_xC_y$층 중 위쪽에 형성된 $Si_{1-x-y}Ge_xC_y$층의 바로 위에 형성된 저저항의 도체막으로 된 소스□드레인 콘택트층을 추가로 구비하는 것을 특징으로 하는 반도체 장치.

청구항 29

제 24 항에 있어서,

상기 제 1 및 제 2 의 $Si_{1-x-y}Ge_xC_y$층 중 위쪽에 형성된 $Si_{1-x-y}Ge_xC_y$층의 바로 위에 형성된 저저항의 도체막으로 된 소스□드레인 콘택트층을 추가로 구비하는 것을 특징으로 하는 반도체 장치.

청구항 30

반도체 기판상에 형성된 적어도 1개의 전계 효과 트랜지스터를 구비한 반도체 장치에 있어서,

상기 전계 효과 트랜지스터는,

$Si_{1-x-y}Ge_xC_y$층$(0\leq x\leq 1,\ 0\leq y\leq 1)$을 포함하는 제 1 반도체층, 상기 제 l 반도체층과는 밴드 갭이 다른 반도체에 의해 구성되는 제 2 반도체층 및 상기 제 1,제 2 반도체층 사이의 경계면 부근의 영역에 형성된 캐리어 축적층을 갖는 채널영역과,

제 3 반도체층 및 이 제 3 반도체층보다 밴드 갭이 큰 반도체로 구성되는 제 4 반도체층을 갖는 소스□드레인 영역과,

상기 제 3 반도체층의 바로 위에 형성된 저저항의 도체막으로 이루어지는 소스□드레인 콘택트층을 구비하는 것을 특징으로 하는 반도체 장치.

청구항 31

제 30 항에 있어서,

상기 제 1 반도체층과 상기 제 3 반도체층은 공통의 제 1 반도체막에 의해 구성되고,

상기 제 2 반도체층과 상기 제 4 반도체는 공통의 제 2 반도체막에 의해 구성되며,

상기 제 2 반도체막은 상기 제 1 반도체막의 위에 형성되는 것을 특징으로 하는 반도체 장치.

청구항 32

제 30 항에 있어서,

상기 제 1 반도체층과 상기 제 3 반도체층은 서로 다른 반도체막에 의해 구성되고,

상기 제 3 반도체층은 상기 제 1 반도체층의 위쪽에 형성되고,

상기 제 4 반도체층은 상기 제 3 반도체층의 위에 형성되는 것을 특징으로 하는 반도체 장치.

청구항 33

n-채널 전계 효과형 트랜지스터와, p-채널 전계 효과형 트랜지스터를 갖는 반도체 장치의 제조방법에 있어서,

반도체 기판상에, 제 1 Si 층과, 상기 Si 층에 근접함과 동시에 상기 제 1 Si 층에 근접한 영역에 상기 n-채널 전계 효과형 트랜지스터의 채널로 되는 제 1 캐리어 축적층을 갖도록 제 1 의 $Si_{1-x-y}Ge_xC_y$층 $(0\leq x\leq l, Oy\leq 1)$을 형성하는 제 1 공정과,

반도체 기판상에, 제 2 Si 층과, 상기 제 2 Si 층에 근접함과 동시에, 상기 제 1 의 $Si_{1-x-y}Ge_xC_y$층과는 다른 밴드 갭을 갖고, 상기 제 2 의 Si 층에 근접한 영역에 상기 p-채널 전계 효과형 트랜지스터의 채널로 되는 제 2 캐리어 축적층을 갖는 제 2 $Si_{1-x-y}Ge_xC_y$층$(0\leq x\leq 1,0\leq y\leq 1)$을 형성하는 제 2 공정과,

상기 제 1 및 제 2 의 $Si_{1-x-y}Ge_xC_y$층 중 위쪽에 위치하는 $Si_{1-x-y}Ge_xC_y$층위에 도체막을 퇴적한 후, 이 도체막을 패터닝하여 상기 n-채널 전계 효과형 트랜지스터 및 p-채널 전계 효과형 트랜지스터의 게이트 전극을 각각 형성하는 제 3 공정과,

상기 각 트랜지스터의 게이트 전극을 마스크로서, 상기 n-채널 전계 효과형 트랜지스터 형성 영역에는 적어도 상기 제 1 캐리어 축적층에 도달하는 깊이까지 n 형 불순물을, 상기 p-채널 전계 효과형 트랜지스터 형성 영역에는 적어도 상기 제 2 캐리어 축적층에 도달하는 깊이까지 p형 불순물을 각각 도입하고, 상기 n-채널 전계 효과형 트랜지스터 및 p-채널 전계 효과형 트랜지스터의 소스□드레인 영역을 각각 형성하는 제 4 공정을 구비하는 것을 특징으로 하는 반도체 장치의 제조방법.

청구항 34

$Si_{1-x-y}Ge_xC_y$층$(0\leq x\leq 1,0\leq y\leq 1)$을 포함하는 제 1 반도체층과, 상기 제 1 반도체층과는 다른 밴드 갭을 갖는 제 2 반도체층과, 상기 제 1,제 2 반도체층 사이의 경계면 부근의 영역에 형성된 채널로 되는 캐리어 축적층 갖고, 전계 효과 트랜지스터로서 기능하는 반도체 장치의 제조방법에 있어서,

반도체 기판의 전계 효과 트랜지스터 형성 영역에, 제 3 반도체층과, 이 제 3 반도체층보다 큰 밴드 갭을 갖는 제 4 반도체층을 차례로 형성하는 제 l의 공정과,

상기 제 4 반도체층의 위쪽에 도체막을 퇴적한 후, 이 도체막을 패터닝하여 게이트막을 형성하는 제 2 공정과,

GF Exhibit 1124 - 2000/2704

상기 게이트 전극 양측에 위치하는 상기 전계 효과형 트랜지스터 형성 영역에 적어도 상기 캐리어 축적층에 도달하는 깊이까지 불순물을 도입하여, 소스□드레인 영역을 형성하는 제 3 공정과,

상기 소스□드레인 영역에서의 상기 제 4 반도체층을 적어도 상기 제 3 반도체층이 노출될 때까지 에칭에 의해 제거하는 제 4 공정과,

상기 제 3 반도체층이 노출된 면 위에 저저항의 도체막으로 이루어지는 소스□드레인 콘택트층을 형성하는 제 5 공정을 구비하는 것을 특징으로 하는 반도체 장치의 제조방법.

청구항 35

제 34 항에 있어서,

상기 제 1 공정은, 상기 제 1 및 제 3 반도체층을 공통의 제 1 반도체막으로 구성하고, 상기 제 2 및 제 4 반도체층을 공통의 제 2 반도체막으로 구성하는 것을 특징으로 하는 반도체 장치의 제조방법.

청구항 36

제 34 항에 있어서,

상기 제 1 공정의 앞에 상기 제 1 및 제 2 반도체층을 형성하는 공정을 추가로 구비하고,

상기 제 1 공정은 상기 제 1 반도체층의 위쪽에 제 3 반도체층을 형성하도록 행하는 것을 특징으로 하는 반도체 장치의 제조방법.

청구항 37

제 34 항 내지 제 36 항 중 어느 한 항에 있어서,

상기 제 4 공정은 상기 제 3 반도체층과 상기 제 4 반도체층과 대한 에칭 선택비가 높은 에칭조건으로 하는 것을 특징으로 하는 반도체 장치의 제조방법.

명세서

발명의 명칭

반도체 장치 및 그 제조방법

도면의 간단한 설명

도 1은 본 발명의 제 1 실시예에 의한 SiGeC 계 HCMOS 장치의 구조를 나타내는 단면도.

도 2는 HCMOS 장치 내의 SiGeC 층의 격자 왜곡의 Ge 조성율 및 C 조성율에 대한 의존성을 도시한 도면.

도 3은 SiGeC 계 HCMOS 장치의 SiCeC 층과 Si 층 사이에 있어 격자정합 또는 인장 왜곡을 발생하는 Si, Ge, C의 조성율과의 관계를 도시한 도면.

도 4는 SiGeC 층의 C 조성비와 에너지 갭 값의 관계를 도시한 도면.

도 5는 본 발명의 제 l의 실시예에 의한 반도체 장치의 제조 공정을 나타내는 단면도.

도 6은 본 발명의 제 2 실시예에 있어서의 SiGeC 층의 조성과 격자 부정합에 의한 왜곡의 관계를 도시한 도면.

도 7은 본 발명의 제 2 실시예에 의한 격자 정합계 SiGeC-HCMOS 장치의 밴드-라인업을 도시한 도면.

도 8은 본 발명의 제 3 실시예에 의한 양자 우물 구조의 채널을 갖는 HCMOS 장치의 구조를 나타내는 단면도.

도 9는 본 발명의 제 3 실시예에 의한 반도체 장치의 제조공정을 나타내는 단면도.

도 10은 본 발명의 제 4 실시예에 의한 HCMOS 장치의 구조를 나타내는 단면도.

도 11은 본 발명의 제 4 실시예에 의한 HCMOS 장치의 제조공정 중의 전반 부분을 나타내는 단면도.

도 12는 본 발명의 제 4 실시예에 의한 HCMOS 장치의 제조공정 중의 후반 부분을 나타내는 단면도.

도 13은 본 발명의 제 5 실시예에 의한 HCMOS 장치의 구조를 나타내는 단면도.

도 14는 본 발명의 제 6 실시예에 의한 HCMOS 장치의 구조를 나타내는 단면도.

도 15는 종래의 HCMOS 장치의 구조를 나타내는 단면도

도 16은 종래의 HCMOS 장치의 헤테로 경계면에 도입되는 격자 부정합에 의한 전위 등의 결함을 도시한 도면.

도면의 주요한 부위를 나타내는 부호의 설명

1O, 30, 50 : Si 기판　　11, 31, 51n : p 홀

12, 32, 51p : n 홀　　13 : Si 층

GF Exhibit 1124 - 2002/2704

14, 34 : SiGeC 층　　15, 36 : SiGe 층

16 소스□드레인 영역　　17 Si 층

18, 38, 65 : 게이트 전극　　19, 39, 58 : 게이트 절연막

21, 41 : 소스□드레인 전극　　25, 45, 61 : 소스□드레인 콘택트W 층

33 : 제 1 Si 층　　35 : 제 2 Si 층

37 : 제 3 Si 층　　42, 49 : 소스□드레인 영역

52 : SiGe 버퍼층　　53 : δ 도핑층

54 : 스페이스 층　　55, 57 : i-Si 층

56 : i-$Si_{1-x}Ge_x$ 층　　63 : Al 소스□드레인 전극

66 : 제 1 층 절연막　　67 : n-채널

68 : p-채널

발명의 상세한 설명

본 발명은, 반도체 장치에 관하여, 특히, SiGeC 층 또는 SiGe 층을 이용하는 헤테로 접합의 전계 효과형 트랜지스터를 구비한 반도체 장치 및 그 제조방법에 관한 것이다.

최근, 반도체 장치의 고집적화가 진행되고 있지만, M0S 형 트랜지스터의 미세화도 게이트 길이가 O.1μm를 하회하는 초미세화 영역에서는, 단채널 효과의 영향이나 저항성분의 증대 등에 의해, 전류 구동 능력이 포화하는 등, 지금까지와 같은 성능 향상을 기대할 수 없는 것이 예상되고 있다. 특히, 미세 M0S 트랜지스터의 고 구동력화를 위해서는, 채널의 캐리어 이동도의 향상이나, 소스□드레인 전극의 콘택트의 저 저항화가 중요하다.

그래서, 실리콘 기판 상에 형성되는 단일 조성의 Si를 이용한 상보형 반도체 장치(CMOS 장치)에 대신하여, Si/SiGe 계(IV 족 혼합 결정)에 의한 헤테로 구조 CMOS 장치(Heterostructure CMOS : 이하, HCMOS 장치라 한다)가 제안되어 있다. 이것은, 채널로서 Si/SiO2 경계면이 아니라 밴드 갭이 상이한 두 종류의 반도체에 의한 헤테로 접합체의 경계면을 이용하는 것이다. 이러한 Si보다도 높은 캐리어 이동도를 부여하는 Si/SiGe 계를 이용함으로써, 더욱 더 고속인 소자를 실현할 수 있다고 기대되고 있다. 이 Si/SiGe 계에서는, 조성의 제어에 의해 Si 기판 상에 원하는 왜곡 양과 밴드 값을 갖는 에피텍셜 성장층을 형성하는 것이 가능하다. IBM 사의 Ismail은, Si/SiGe 계의 HCMOS 장치에 의한 특성 향상에 관해서의 기초 실험을 한다 (K.Ismail, Si/SiGe High Speed Field-Effect Transistors , IEDM Tech. Dig. 1995. p509. 및 M.A. Armstrong et al, Design of Si/SiGe Hetrojunction Complementary Metal-Oxide-Semiconductor TransistorsIEDM Tech. Dig. 1995,p701을 참조).

도 15는, 이 HCMOS 장치의 일례를 나타내는 단면도이다. 도 15에 도시한 바와 같이, Si 기판(101)의 일부에는, 소스□드레인 영역(109)과, 게이트 절연막(107) 및 그 위에 게이트 전극(110)으로 구성되는 전계 효과형 트랜지스터가 설치된다. 그리고, 게이트 전극(110)의 아래쪽에 의한 소스 영역-드레인 영역 사이의 소위 채널영역에는, SiGe 버퍼층(102)과, δ 도핑층(115)과, 스페이스층(103)과, i-Si층(104)과, i-SiGe 층(105) 및 i-Si층(106)이 형성되어 있다. 이들의 영역에서, SiGe 버퍼층(102)은,

GF Exhibit 1124 - 2003/2704

i-Si층(104)과 i-SiGe층(105)의 사이에 n-채널층(112)을 형성하기 위해서, i-Si 층(104)에 인장 왜곡을 주는 것이다. 이 SiGe 버퍼층(102)에 있어서, Si 기판(101)의 바로 위에서는 Ge 조성비가 0%로 되고, 최상에서는 Ge 조성비가 30%로 되도록 단계적으로 조성비가 변경되어 있다.

여기서, 부 바이어스가 인가되면, i-Si 층(104)에 있어서 아래쪽의 SiGe 버퍼층(102)과의 헤테로 경계면에 n-채널층(112)이 형성된다. δ 도핑층(115)은 위쪽에 형성되는 n-채널층(112)에 캐리어인 전자를 공급한 것이다. 또한, 스페이스층(103)은, 아래쪽으로 형성된 δ 도핑층(115)의 이온과 위쪽의 n-채널층(112)을 공간적으로 분리하여, 캐리어의 이온 산란에 의한 이동도의 저하를 방지한 것이다.

또한, 정 바이어스가 인가되면, i-SiGe 층(105)에 있어서, 위쪽의 i-Si층(106)과의 헤테로 경계면에는 p-채널층(111)이 형성된다. 게이트 절연막(107)은, 게이트 전극(110)과 p-채널층(111)을 절연하기 위한 것이다.

상술한 바와 같이, 헤테로 전계 효과 트랜지스터에서는, 밴드 갭이 다른 두 종류의 반도체층 간의 헤테로 경계면에 채널을 형성하는 것이 특징이다. 따라서, 채널 형성을 위해 필연적으로 밴드 갭이 다른 적어도 두 가지의 반도체층이 존재한다. 덧붙여, 반도체층 중에 전자 또는 정공이 고속으로 이동하기 위한 채널을 형성하기 위해서는, 헤테로 경계면에 전도대 또는 가전자대의 불연속부를 갖는 것이 필요하게 된다. 상술한 Si/SiGe 계에서는, 정공에 대해서는 SiGe 층(105)이 i-Si 층(106)에 대하여 가전자대에 있어서의 불연속부를 갖기 때문에, 정공용의 채널이 형성된다 (도 15의 왼쪽 부분 참조). 그러나, 전도대에는 불연속부가 거의 없기 때문에, 전자용의 채널을 형성하기 위하여 i-Si 층(104)에 인장 왜곡을 인가함으로써, i-SiGe 층(105)과의 헤테로 경계면에 전도대의 불연속부를 형성하고 있다 (도 15의 오른쪽 부분참조).

이러한 구조를 갖는 HCMOS 장치는, Si/Si02에 의한 채널을 사용하는 종래의 CMOS 장치에 비교하여, 같은 가공 치수로 2배의 고속도 동작을 1/2의 소비 전력으로 실현할 수 있는 것이 시뮬레이션의 결과로부터 예상되고 있다. 즉, Si 반도체와 SiGe 혼합 결정을 조합함으로써 헤테로 경계면을 형성하여, 고이동도 채널을 형성한 반도체 소자로서, 헤테로 접합을 이용하는 소자의 고속 동작과, M0S 장치의 대규모 집적성을 모두 실현하는 소자로서 매우 주목을 끌고 있다.

그렇지만, 상술한 바와 같은 SiGe 등의 Ⅳ족 혼합 결정을 이용하는 헤테로 장치는 종래의 CM0S 장치의 성능 한계를 극복하는 방법으로서 크게 기대되고 있지만, SiGe로 대표되는 Ⅳ족 혼합 결정을 이용하는 헤테로 전계 효과 트랜지스터는, 그 제조가 곤란하기 때문에 같은 SiGe 혼합 결정을 이용한 헤테로 장치인 헤테로 바이폴라 트랜지스터에 비교하여 연구 개발이 늦게 되고, 아직 그 기대되는 성능을 충분히 발휘하도록 구조 및 제조 방법의 검토가 충분히 행하여지고 있다고는 할 수 없다. 또한, 헤테로 전계 효과 트랜지스터 중에서도, 상술한 바와 같은 게이트 전극과 반도체층 사이에 절연막을 갖는 소위 헤테로 MOS 구조의 경우, SiGe 층 내에는 안정에서 양호한 절연막을 형성할 수 없기 때문에, 게이트 절연막으로서 SiO2로 이루어지는 산화막을 사용한다. 따라서, 게이트 절연막의 바로 아래는 반드시 Si층 일 필요가 있지만, Si는 SiGe에 비교하여 반드시 밴드 갭이 커진다고 하는 특징을 갖고 있다.

그 때문에, 상기 종래의 HCMOS 장치의 구조에 있어서는, 이하와 같은 문제가 있었다.

첫번째로, 상술한 바와 같이 Si 기판(101)상에 전자의 채널을 형성하기 위하여, i-Si 층(104)에 인장 왜곡을 인가하여, Si/SiGe 헤테로 경계면에 밴드 불연속을 형성하고 있다. 그러나, 격자정수를 변화시킴으로써, 격자 완화에 의한 전위의 도입을 수반한다.

도 16은, SiGe 버퍼층(102)과 그 위의 i-Si 층(104)을 발췌하여 나타내는 단면도이다. i-Si 층(104)은, SiGe 버퍼층(102)보다도 격자정수가 작기 때문에, 결정 성장된 단계에서 인장왜곡이 축적된다. 이 왜곡의 축적이 커지면, 도 16에 도시하는 바와 같이, i-Si 층(104)에 전위가 입력된다. 이와 같이, i-Si 층(104)과 SiGe 버퍼층(102)의 사이에 걸친 격자 부정합 왜곡에 의한 전위나 결함의 도입은 피

GF Exhibit 1124 - 2004/2704

할 수 없다. 따라서, 이 결정을 이용한 소자의 초기 특성은 어쨌든, 신뢰성이나 수명의 관점에서는 전위의 증식 등에 의한 특성 열화의 영향이 생겨난다고 여겨진다.

또한, Si 기판 (l01)상에 Si보다 격자 정수의 큰 SiGe로 이루어지는 SiGe 버퍼층(102)을 적층하여, 그 위에 성장하는 i-Si 층(104)에 인장 왜곡을 적층시키고 있지만, SiGe 버퍼층(102)의 막 두께를 크게 하면, 그 사이에 SiGe 버퍼층(102)의 격자 정수가 Si의 격자정수로부터 원래의 SiGe의 격자 정수로 변화하는 임계막 두께를 초월하기 때문에, 격자완화가 생겨 SiGe 버퍼층(102)에도 전위 등의 결함이 도입된다.

이것들의 결함은, 소자의 초기 특성으로의 영향은 적은 경우도 있지만, 장기적인 신뢰성이나 수명이라는 관점에서는 중대한 문제를 야기할 우려가 있다. 즉, 전류에 의한 결함의 증식이나 금속이나 불순물의 결함을 개재한 확산에 의한 열화가 생겨 신뢰성의 저하를 초래하는 우려가 있다.

본 발명의 제 1 목적은, HCMOS 장치의 게이트 아래쪽의 채널 영역에 길친 구조로서 캐리어 축적층을 형성할 수 있는 밴드 불연속부를 갖으면서 격자 정합 또는 거의 격자 정합된 헤테로 접합체를 이용함으로써, 캐리어의 이동도가 높고 또한 신뢰성이 높은 반도체 장치를 제공하는 것에 있다.

두번째로, SiGe로 대표되는 Ⅳ족 혼합 결정을 이용한 헤테로 진계 효과 장치는 종래의 미세 CM0S 장치의 성능 한계를 극복하는 소자 구조로서 유효한 기술이지만, 현시점에서는 채널 이동도의 향상의 연구에 비하여 소스□드레인 전극의 콘택트의 최적화의 검토는 더욱 불충분하고, 그 고이동도를 충분히 활용하는 구조로 되는 것은 아니다. 상술한 IBM 사에 의한 헤테로 CMOS 장치의 기술도 채널 영역의 이동도 향상에 있어서는 상세한 검토가 이루어지고 있지만, 미세 트랜지스터의 성능 향상에 중요한 또 하나의 요소인 소스□드레인 전극의 콘택트의 저저항화에 있어서는 거의 검토가 이루어지지 않고 있다.

즉, Si 단결정을 이용한 CM0S 장치 구조에 있어서는, 소스□드레인 전극에 접속되는 기판측의 콘택트 영역의 구조에 있어서는 여러 가지의 검토가 이루어지고 있지만, 일반적인 CM0S 장치에 있어서의 최적의 콘택트 영역의 구조 및 형성방법이, 소자 구조가 다른 헤테로 전계 효과 장치에 있어서도 최선인지 어떤지는 검토가 필요하다.

본 발명의 제 2 목적은, 헤테로 전계 효과 장치가 뛰어난 특성을 손상시키는 일없이 작은 콘택트 저항을 발휘할 수 있는 콘택트 영역을 갖는 반도체 장치 및 그 제조방법을 제공하는 것에 있다.

상기 제 1 목적을 달성하기 위해서, 본 발명에서는, 청구항 1□16에 기재되어 있는 제 1 반도체 장치에 관한 수단과, 청구항 17□29에 기재되어 있는 제 2 반도체 장치에 관한 수단과, 청구항 33에 기재되어 있는 제 1 반도체 장치의 제조방법에 관한 수단을 강구하고 있다.

상기 제 2 목적을 달성하기 위해서, 본 발명에서는, 청구항 30□32에 기재되어 있는 제 3 반도체 장치에 관한 수단과, 청구항 34□37에 기재되어 있는 제 2 반도체 장치의 제조방법에 관한 수단을 강구하고 있다.

본 발명의 제 1 반도체 장치는, 청구항 1에 기재되어 있는 바와 같이, 반도체 기판의 일부에 형성되어 게이트 전극과 소스□드레인 영역 및 해당 소스□드레인 영역사이의 채널 영역을 갖는 전계 효과 트랜지스터를 구비하고 있는 반도체 장치로서, 상기 채널영역에는 Si 층과, 상기 Si 층에 접하여 형성되고 C의 조성비 y가 0.01□0.03인 $Si_{1-x-y}Ge_xC_y$ 층 ($0 \leq x \leq 1$, $0 y \leq 1$)이 설치되고, $Si_{1-x-y}Ge_xC_y$층 내에서의 상기 Si 층에 근접한 영역에는 캐리어 축적층이 형성되어 있다.

이에 따라, C의 조성비 y가 0□01□0.03인 $Si_{1-x-y}Ge_xC_y$ 층과 Si 층의 경계면에는 캐리어를 2차원적으로 가두는 캐리어 축적층을 형성하는 데 필요한 밴드 불연속부를 형성하는 것이 가능하다. 그리고, 이 캐리어 축적층이 채널로서 기능하기 때문에, Si 층보다도 큰 캐리어 이동도를 부여하는 Si_{1-x-}

GF Exhibit 1124 - 2005/2704

$_yGe_xC_y$ 층을 채널로 하는 동작 속도가 큰 전계 효과형 트랜지스터를 얻을 수 있다. 더구나, $Si_{1-x-y}Ge_xC_y$ 층과 Si 층 사이에서는 격자 부정합이 없게되거나 혹은 매우 작게 되도록 제어할 수 있기 때문에, 격자 왜곡을 0 혹은 거의 없도록 조정할 수 있고, $Si_{1-x-y}Ge_xC_y$ 층에 결정 결함이 도입되지 않도록 구성하는 것이 가능하다. 따라서, 높은 신뢰성을 갖는 반도체 장치를 얻을 수 있다.

청구항 2에 기재된 바와 같이, 상기 $Si_{1-x-y}Ge_xC_y$ 층의 각 원소의 조성비를, 상기 $Si_{1-x-y}Ge_xC_y$ 층과 상기 Si 층 이 격자 정합하는 조성비로 조정해 놓을 수 있다.

이에 따라, 격자 부정합에 기인하는 왜곡이 없는 $Si_{1-x-y}Ge_xC_y$ 층 내에 채널이 형성되기 때문에, 매우 높은 신뢰성을 갖는 반도체 장치를 얻을 수 있게 된다.

청구항 3에 기재된 바와 같이, 상기 $Si_{1-x-y}Ge_xC_y$ 층을 상기 Si 층보다 작은 격자 정수를 갖고 또한 격자 완화를 발생하지 않는 막 두께를 갖는 것으로 할 수가 있다.

이에 따라, $Si_{1-x-y}Ge_xC_y$ 층에는 인장 왜곡이 가해지기 위해서, Si 층과의 밴드의 불연속량을 크게 할 수 있어 캐리어의 폐쇄 효율이 향상된다.

청구항 4에 기재된 바와 같이, 상기 반도체 기판 상에 형성되어 단일 조성의 반도체층을 채널 영역으로 하는 M0S 트랜지스터를 추가로 구비할 수 있다.

청구항 5 및 6에 기재된 바와 같이, 상기 캐리어 축적층에 축적되는 캐리어를 부의 캐리어로 할 수 있다.

청구항 7□9에 기재된 바와 같이, 상기 Si 층내의 상기 $Si_{1-x-y}Ge_xC_y$ 층에 근접한 영역에 상기 캐리어 축적층에 캐리어를 공급하기 위한 캐리어 공급층을 설치하여 두는 것이 바람직하다.

청구항 10에 기재된 바와 같이, 상기 캐리어 축적층에 축적되는 캐리어를 부의 캐리어로 하고, 상기 반도체 기판의 타부에 형성되어 게이트 전극과 소스□드레인 영역과 해당 소스□드레인 영역사이의 채널 영역을 갖는 또 1개의 전계 효과 트랜지스터를 추가로 설치하여, 상기 또 1개의 전계 효과 트랜지스터의 채널 영역에 제 2 Si 층과 ,상기 제 2 Si 층에 근접하여 형성된 SiGe 층을 설치하여, 상기 SiGe 내에서의 상기 제 2 Si 층에 근접한 영역에 정의 캐리어를 축적하기 위한 제 2 캐리어 축적층을 형성해 두는 것이 바람직하다.

이에 따라, n-채널측 및 p-채널측 중 어느 하나에서도 높은 캐리어 이동을 갖는 HCMOS 장치로서 기능하는 반도체 장치를 얻을 수 있다.

청구항 11에 기재된 바와 같이, 상기 $Si_{1-x-y}Ge_xC_y$ 층을 양자 우물 영역으로 할 수 있다.

청구항 12에 기재된 바와 같이, 상기 SiGe 층을 양자 우물 영역으로 할 수 있다.

청구항 11 또는 12에 의해, 캐리어의 폐쇄 효율이 높은 채널을 갖는 전계 효과형 트랜지스터를 얻을 수 있다.

청구항 13□16에 기재된 바와 같이, 상기 소스□드레인 영역에 제 1 반도체층과, 이 제 1 반도체층보다도 큰 밴드 갭을 갖는 제 2 반도체층을 설치하여, 상기 제 1 반도체층의 바로 위에 형성된 저저항의 도체막으로 이루어지는 소스□드레인 콘택트층을 구비할 수 있다.

이에 따라, 각 청구항의 작용 효과에 덧붙여 헤테로 접합을 이용하면서 콘택트 저항이 작은 반도체 장치를 얻을 수 있다.

GF Exhibit 1124 - 2006/2704

본 발명의 제 2 반도체 장치는, 청구항 17에 기재된 바와 같이, 반도체 기판의 일부에 형성되어, 게이트 전극과 소스□드레인 영역과 이 소스□드레인 영역사이의 채널 영역을 갖는 전계 효과 트랜지스터를 구비하고, 상기 채널 영역에는, 제 1 Si 층과, 상기 Si 층에 접하여 형성된 제 1 $Si_{1-x-y}Ge_xC_y$ 층 $(0\leq x\leq 1, 0y\leq 1)$과, 제 2 Si 층 및 상기 제 2 Si 층 것에 접하여 형성되고 상기 제 1 $Si_{1-x-y}Ge_xC_y$ 층과는 다른 밴드 갭을 갖는 제 2 $Si_{1-x-y}Ge_xC_y$ 층$(0\leq x\leq 1, 0\leq y\leq 1)$이 설치되어, 상기 제 1 $Si_{1-x-y}Ge_xC_y$ 층 안에서의 상기 제 1 Si 층에 근접한 영역과, 상기 제 2 $Si_{1-x-y}Ge_xC_y$ 층 안에서의 상기 제 2 Si 층에 근접한 영역과는 서로 다른 도전형의 캐리어를 폐쇄하기 위한 제 1 및 제 2 캐리어 축적층이 각각 형성되어 있다.

이에 따라, 각각 캐리어의 폐쇄 효율이 높은 채널을 갖고 또한 동작 속도가 큰 n-채널 전계 효과 트랜지스터 및 p-채널 전계 효과 트랜지스터를 구비한 HCMOS 장치로서 기능하는 반도체 장치를 얻을 수 있다. 더구나, 제 1 $Si_{1-x-y}Ge_xC_y$ 층과 제 1 Si 층의 사이에서는 격자 부정합이 없게 되거나 또는 매우 적게 되도록 제어할 수 있기 때문에, 제 1 $Si_{1-x-y}Ge_xC_y$ 층에 결정 결함이 도입되지 않도록 구성하는 것이 가능하다. 따라서, 높은 신뢰성을 갖는 반도체 장치를 얻을 수 있다.

청구항 18에 기재된 바와 같이, 상기 제 2 $Si_{1-x-y}Ge_xC_y$ 층에 있어서의 C의 조성비 y를 0으로 할 수 있다.

청구항 l9에 기재된 바와 같이, 상기 반도체 기판 상에 형성되어, 단일 조성의 반도체층을 채널 영역으로 하는 M0S 트랜지스터를 추가로 설치하여도 된다.

이에 따라, 동작 속도가 요구되는 부분에는 상기 제 1 $Si_{1-x-y}Ge_xC_y$ 층을 채널 영역으로 갖는 트랜지스터를 배치하고, 그 이외의 부분에서는 통상의 M0S 트랜지스터를 배치하여 반도체 장치의 응용 범위를 확대시킬 수 있다.

청구항 20에 기재된 바와 같이, 상기 제 1 $Si_{1-x-y}Ge_xC_y$ 층에 있어서의 C의 조성비 y를, 0.01□0.03으로 하는 것이 바람직하다.

청구항 21에 기재된 바와 같이, 상기 제 1 $Si_{1-x-y}Ge_xC_y$ 층의 각 원소의 조성비를 상기 제 1 $Si_{1-x-y}Ge_xC_y$ 층과 상기 제 1 Si 층이 격자 정합 하는 조성비로 조정해 두는 것이 바람직하다.

이에 따라, 격자 왜곡이 없는 신뢰성이 높은 전계 효과형 트랜지스터를 갖는 반도체 장치를 얻을 수 있다.

청구항 22에 기재된 바와 같이, 상기 제 1 $Si_{1-x-y}Ge_xC_y$ 층을 상기 제 1 Si 층의 격자 정수보다 작은 격자정수를 갖고 또한 격자 완화를 일으키지 않는 막 두께를 갖는 것으로 할 수가 있다.

이에 따라, 제 1 $Si_{1-x-y}Ge_xC_y$ 층에는 인장 왜곡이 가해지기 때문에 제 1 Si 층과의 사이의 밴드 불연속량을 크게 할 수 있어 캐리어의 폐쇄 효율이 향상된다.

청구항 23에 기재된 바와 같이, 상기 제 1 캐리어 축적층에 축적되는 캐리어를 부의 캐리어로 하고, 상기 제 2 캐리어 축적층에 축적되는 캐리어를 정의 캐리어로 하는 것이 바람직하다.

청구항 24 및 25에 기재된 바와 같이, 상기 제 1 Si 층 내에서의 상기 제 1 $Si_{1-x-y}Ge_xC_y$ 층에 근접한 영역에 상기 제 1 캐리어 축적층에 캐리어를 공급하기 위한 캐리어 공급층을 추가로 형성하는 것이 바람직하다.

GF Exhibit 1124 - 2007/2704

청구항 26에 기재된 바와 같이, 상기 제 1 및 제 2 $Si_{1-x-y}Ge_xC_y$ 층 내 적어도 어느 한쪽의 $Si_{1-x-y}Ge_xC_y$ 층은 양자 우물 영역으로 되는 것이 바람직하다.

청구항 27□29에 기재된 바와 같이, 상기 제 1 및 제 2 $Si_{1-x-y}Ge_xC_y$ 층 중 위쪽에 형성된 $Si_{1-x-y}Ge_xC_y$ 층의 바로 위에 형성된 저저항의 도체막으로 이루어지는 소스□드레인 콘택트층을 추가로 구비하는 것이 바람직하다.

본 발명의 제 3 반도체 장치는, 청구항 30에 기재된 바와 같이, 반도체 기판 상에 형성된 적어도 1개의 전계 효과 트랜지스터를 구비한 반도체 장치에 있어서, 상기 전계 효과 트랜지스터는 $Si_{1-x-y}Ge_xC_y$ 층($0\leq X\leq 1, 0\leq y\leq 1$)을 포함하는 제 1 반도체층, 상기 제 1 반도체층과는 밴드 갭이 다른 반도체에 의해 구성되는 제 2 반도체층 및 상기 제1, 제 2 반도체층 사이의 경계면 부근의 영역에 형성된 캐리어 축적층을 갖는 채널 영역과, 제 3 반도체층 및 이 제 3 반도체층보다도 밴드 갭이 큰 반도체층으로 구성되는 제 4 반도체층을 갖는 소스□드레인 영역과, 상기 제 3 반도체층의 바로 위에 형성된 저저항의 도체막으로 이루어지는 소스□드레인 콘택트층을 구비하고 있다.

이에 따라, 헤테로 접합을 이용한 캐리어 이동이 높은 요컨대 동작 속도가 높은 전계 효과 트랜지스터에 있어서의 소스□드레인 영역에의 콘택트 저항을 저감하는 것이 가능하게 된다.

청구항 31에 기재된 바와 같이, 상기 제 1 반도체층과 상기 제 3 반도체층을 공통의 제 1 반도체막에 의해 형성하고, 상기 제 2 반도체층과 상기 제 4 반도체층을 공통의 제 2 반도체막에 의해 형성하여, 상기 제 2 반도체막을 상기 제 1 반도체막의 위에 형성해 놓을 수 있다.

청구항 32에 기재된 바와 같이, 상기 제 1 반도체층과 상기 제 3 반도체층을 서로 다른 반도체막에 의해 형성하고, 상기 제 3 반도체층을 상기 제 1 반도체층의 위쪽에 형성하고, 상기 제 4 반도체층을 상기 제 3 반도체층의 위에 형성해 놓을 수 있다.

본 발명의 제 1 반도체 장치의 제조방법은, 청구항 33에 기재된 바와 같이, n-채널 전계 효과형 트랜지스터와, p-채널 전계 효과형 트랜지스터를 갖는 반도체 장치의 제조방법으로서, 반도체 기판 상에 제 1 Si 층과, 상기 Si 층에 접함과 동시에 상기 제 1 Si 층에 근접한 영역에 상기 n-채널 전계 효과형 트랜지스터의 채널로 되는 제 1 캐리어 층을 갖도록 제 1 $Si_{1-x-y}Ge_xC_y$ 층($0\leq x\leq 1, 0y\leq 1$)을 형성하는 제 1 공정과, 반도체 기판 상에 제 2 Si 층과, 상기 제 2 Si 층에 접함과 동시에 상기 제 1 $Si_{1-x-y}Ge_xC_y$ 층과는 다른 밴드 갭을 갖고, 상기 제 2 Si 층에 근접한 영역에 상기 p-채널 전계 효과형 트랜지스터의 채널로 되는 제 2 캐리어 축적층을 갖는 제 2 $Si_{1-x-y}Ge_xC_y$ 층($0\leq x\leq 1, 0\leq y\leq 1$)을 형성하는 제 2 공정과, 상기 제 1 및 제 2 $Si_{1-x-y}Ge_xC_y$ 층 중 위쪽에 위치하는 $Si_{1-x-y}Ge_xC_y$ 층의 위에 도체막을 퇴적한 후, 이 반도체막을 패터닝하여 상기 n-채널 전계 효과형 트랜지스터 및 p-채널 전계 효과형 트랜지스터의 게이트 전극을 각각 형성하는 제 3 공정과, 상기 각 트랜지스터의 게이트 전극을 마스크로서 상기 n-채널 전계 효과형 트랜지스터 형성 영역에는 적어도 상기 제 1 캐리어 층에 도달하는 깊이까지 n 형 불순물을, 상기 p-채널 전계 효과형 트랜지스터 형성 영역에는 적어도 상기 제 2 캐리어 축적층에 도달하는 깊이까지 p 형 불순물을 각각 도입하고, 상기 n-채널 전계 효과형 트랜지스터 및 p-채널 전계 효과형 트랜지스터의 소스□드레인 영역을 각각 형성하는 제 4 공정을 구비하고 있다.

이 방법에 의해, 청구항 17의 구조를 갖는 반도체 장치가 용이하게 형성되게 된다.

본 발명의 제 2 반도체 장치의 제조방법은, 청구항 34에 기재된 바와 같이, $Si_{1-x-y}Ge_xC_y$ 층($0\leq x\leq 1, 0\leq y\leq 1$)을 포함하는 제 1 반도체층과, 상기 제 1 반도체층과는 다른 밴드 갭을 갖는 제 2 반도체층 및 상기 제 1, 제 2 반도체층의 사이의 경계면 부근의 영역에 형성된 채널로 되는 캐리어 축적층을 갖고, 전계 효과 트랜지스터로서 기능하는 반도체 장치의 제조방법으로서, 반도체 기판의 전계 효과 트랜지스터 형성 영역에 제 3 반도체층과, 이 제 3 반도체층보다 큰 밴드 갭을 갖는 제 4 반도체층을

GF Exhibit 1124 - 2008/2704

차례로 형성하는 제 1 공정과, 상기 제 4 반도체층의 위쪽에 반도체막을 퇴적한 후, 이 도체막을 패터닝하여 게이트 전극을 형성하는 제 2 공정과, 상기 게이트 전극 양쪽에 위치하는 상기 전계 효과형 트랜지스터 형성 영역에 적어도 상기 캐리어 축적층에 도달하는 깊이까지 불순물을 도입하여 소스□드레인 영역을 형성하는 제 3 공정과, 상기 소스□드레인 영역에서의 상기 제 4 반도체층을 적어도 상기 제 3 반도체층이 노출될 때까지 에칭에 의해 제거하는 제 4 공정과, 상기 제 3 반도체층이 노출된 면 위에 저저항의 도체막으로 이루어지는 소스□드레인 콘택트층을 형성하는 제 5 공정을 구비하고 있다.

이 방법에 의해, 청구항 30의 구조를 갖는 반도체 장치가 용이하게 형성되게 된다.

청구항 35에 기재된 바와 같이, 상기 제 1 공정은 상기 제 1 및 제 3 반도체층을 공통의 제 1 반도체막으로 형성하고, 상기 제 2 및 제 4 반도체층을 공통의 제 2 반도체막으로 형성할 수 있다.

청구항 36에 기재된 바와 같이, 상기 제 1 공정의 앞에 상기 제 1 및 제 2 반도체층을 형성하는 공정을 추가로 구비하고, 상기 제 1 공정은, 상기 제 1 반도체층의 위쪽에 제 3 반도체층을 형성하도록 할 수 있다.

청구항 37에 기재된 바와 같이, 상기 제 4 공정은, 상기 제 3 반도체층과 상기 제 4 반도체층에 대한 에칭 선택비가 높은 에칭 조건으로 하는 것이 바람직하다.

상술한 목적 및 기타의 목적과 본 발명의 특징 및 이점은 첨부도면과 관련한 다음의 상세한 설명을 통해 보다 분명해질 것이다.

(실시예)

(제 1 실시예)

제 1 실시예에 의한 HCMOS 장치는,SiGe/Si 계에 C를 첨가하여 되는 SiGeC의 3원 혼합 결정계를 이용하여, 이 SiGeC 층과 Si 층을 거의 격자정합시켜, 밴드 갭 에너지의 차이로부터 헤테로 경계면에 밴드 불연속부를 형성하는 전계 효과 트랜지스터이다.

도 1은, 제 1 실시예에 의한 HCMOS 장치의 구조를 나타내는 단면도이다. 도 1에 도시한 바와 같이, 실리콘 기판(10)상에는,NMOS 트랜지스터와 PMOS 트랜지스터가 형성되어 있지만, 우선, NMOS 트랜지스터의 구조부터 설명한다.

NMOS 트랜지스터에 있어서, Si 기판(10)상에는 p홀(11)(고농도 p형 실리콘층)이 형성되어 있고, 또 그 위에 V족 원소가 고농도로 도핑된 δ 도핑층 및 스페이스층을 갖는 Si 층 (13n)과, SiGeC 층(14n)(C의 조성율은 1%, Ge의 조성율은 8.2%)이 차례로 형성되어 있다. 후술하는 바와 같이, 이 SiGeC 층 (14n)에서의 각 원소의 조성비는, SiGeC 층(14n)과 그 바로 아래의 Si 층(13n)이 격자정합하는 값으로 되어있다.

이 SiGeC 층(14n)과 Si 층(13n)의 헤테로 경계면에는 도 1의 오른쪽 부분에 도시한 바와 같이, 밴드 오프셋 값 ΔEc를 갖는 전도대 Ec의 밴드 불연속부가 존재하고, 이 밴드 불연속부에 부의 캐리어인 전자를 2차원 전자가스(2 DEG)로서 폐쇄하기 위한 캐리어 축적층이 형성된다. 그리고, 이 SiGeC 층(14n) 측의 경계면 부근에 형성된 캐리어 축적층이 전자가 고속으로 주행하는 채널로 된다. SiGeC 층(14n) 내에서는, Si 층 내에 비교해서 전자의 이동도가 크고 이 NMOS 트랜지스터의 동작속도도 크게 할 수 있다.

또, 이 SiGeC 층(14n) 위에, SiGe 층(15n)(Ge의 조성율은 30%, Si의 조성율은 70%)과, Si 층(17n)이 차례로 형성되고, 또 표면에는 실리콘 산화막으로 이루어지는 게이트 절연막(19n)이 형성되어 있다. 이 게이트 절연막(19n)의 아래로는 Si 층(17n)이 존재하고 있기 때문에 Si 층 (17n)의 표면을 산화하는 것만으로 결정성이 높은 게이트절연막(19n)을 용이하게 형성할 수가 있다. 게이트 절연막(19n)

GF Exhibit 1124 - 2009/2704

위에는 게이트 전극(18n)이 형성되고, 이 게이트 전극(18n)의 양측에 위치하는 기판 내에는 소스□드레인층(16n)이 형성되어 있다. SiGeC 층(14n) 내에서의 전자의 주행은 게이트 전극(18n)에 인가되는 전압에 의해서 제어된다. 또, 소스□드레인층(16n)은, p홀(11)에 도달하는 깊이까지 형성되어 있지만, 적어도, SiGeC 층(14n)에 형성되는 채널로 되는 부분의 깊이까지 형성되면 된다.

한편, PMOS 트랜지스터는, 이상에서 설명한 NMOS 트랜지스터와 거의 같은 구조를 갖고 있다. Si 기판(10)상에는 n홀(12)(고강도 n형 Si 층)이 형성되어 있고, 또 그 위에, V 족 원소가 고농도로 도핑된 δ 도핑층을 갖는 Si 층(13p)과, SiGeC 층 (14p)(Ge의 조성율은 8.2%, C의 조성율은 1%)이 차례로 형성되어 있다. 또, 이 SiGeC 층 (14p) 위에, SiGe 층(15p)(Ge의 조성율은 30%, Si의 조성율은 70%), Si 층(17p)이 차례로 형성되어 있다. PMOS 트랜지스터의 경우는, 캐리어가 정공으로 되지만 이 정공이 흐르는 채널은 SiGe 층(15p)과 Si 층(17p)의 경계면의 SiGe 층(15p) 측에 형성된다. 이 SiGe 층(15p)과 Si 층(17p)의 헤테로 경계면에 밴드 오프셋 값ΔEv를 갖는 가전자대의 밴드 불연속부가 존재하고, 이 불연속부에 캐리어 층이 형성된다. 따라서, SiGe 층(15p) 측의 경계면에 형성된 캐리어 축적층 채널을 정공이 주행하지만, SiGe 층(15p) 내에서도 Si 층내에 비교해서 정공의 이동도가 크기 때문에 이 PM0S 트랜지스터의 동작속도도 커진다.

PMOS 트랜지스터에 있어서, Si 층(17p)의 위에는, 실리콘 산화막으로 이루어지는 게이트 절연막(19p)이 형성되어 있다. 게이트 전극(18p)의 양측에는 소스□드레인층(16p)이 형성되고, SiGe 층(15p)에서의 정공의 주행은 게이트 전극(18p)에 인가되는 전압에 의해 제어되고 있다.

또한, NMOS 트랜지스터와 PMOS 트랜지스터와의 사이는 기판에 형성된 홈을 실리콘 산화막에 의해서 매립하여 되는 트랜치(trench)분리(20)가 설정되고, 이 트랜치분리(20)에 의해서, NMOS 트랜지스터와 PMOS 트랜지스터와가, 서로 전기적으로 분리되어 있다.

또, 각 Si 층(13n, 13p),각 SiGeC 층(14p, 14n), 각 SiGe 층(15n, 15p), 각 Si 층(17n, 17p)은, 결정 성장에 의해 각각 동시에 형성되어 있다. 그리고, 각 층의 치수는, 예컨대 이하 같은 치수로 할 수 있다. 단지, 반드시 이하의 치수로 한정되는 것은 아니다.

각 Si 층(13n, 13p)의 두께는 예를 들면 0.6μm 정도이고, 0□1μm의 범위에 있는 것이 바람직하다. 스페이스층의 두께는 예를 들면 30 nm 정도이고, 0□50nm의 범위에 있는 것이 바람직하다. 각 SiGeC 층(14p, 14n)의 두께는 3□50nm 인 것이 바람직하다. 각 SiGe 층(15n, 15p)의 두께는 5nm 정도이고, 3□5nm의 범위에 있는 것이 바람직하다. 각 Si 층 (17n, 17p)의 두께는 1nm 정도이고, 0.5□5nm의 범위에 있는 것이 바람직하다. 게이트 절연막(19n, 19p)의 두께는, 예컨대 5nm 정도이다.

또한, 게이트 전극 (18n, 18p)의 게이트 길이는 0.25μm, 게이트 폭은 2.5μm, 소스□드레인 영역의 폭은 1.2μm 정도이고, 소스□드레인 전극(21n, 21p)의 콘택트 면적은, 0.5μm× 0.6μm 정도이다. 각 홀(13n, 13p)의 도핑 농도는 1×10^{17}□1×10^{18} cm^{-3}정도이고, δ 도핑층의 도핑농도는, 1×10^{18}□1×10^{20} cm^{-3}정도이다.

본 실시예에 있어서의 HCMOS 장치(HeterostructureCMOS 장치)의 특징은, SiGeC 층을 이용하는 점이다. 이 SiGeC 층은, Si, Ge, C의 각각의 조성비의 조정에 의해 밴드 갭 층 및 실리콘에 대한 격자 부정합율을 바꿀 수 있다. 여기서, 본 실시예에 있어서의 Si, Ge, C의 조성비와, 각 층의 왜곡 및 밴드 오프셋 량과의 관계에 관해서 상세히 설명하기로 한다.

도 2는, 가로축에 C(탄소)의 조성비(%), 세로축에 Ge의 조성비(%)를 잡을 때에, SiGeC 층과 Si 층은 격자 부정합율(%)(Miss fit)이 변화하는 모양을 보이고 있다. 부정합율이 0인 선은, SiGeC 층과, Si 층의 격자 정수가 같은 것을 나타낸다. Ge(게르마늄)단결정의 격자정수는 Si 단결정의 격자정수보다도 크고, C(탄소)단결정의 격자정수는 Si 단결정의 격자정수보다도 작기 때문에, Ge와 C의 조성비를 조정함으로써 SiGeC 층(14n)의 격자정수와 Si 층 (13n)의 격자정수를 일치시킬 수 있는 것이다.

GF Exhibit 1124 - 2010/2704

도 3은, Si, Ge, C의 3원소의 조성비에 대한 격자정합의 관계를 나타내는 특성도이다. 도 3의 3개의 꼭지점은, 각각 Si, Ge, C의 조성율이 100%(조성비가 1)인 점이고, SiGeC 층의 3원 혼합 결정계의 조성비의 조정에 의해서 Si와의 격자 부정합율이 변화하는 형태를 보이고 있다. 도 3 중 해칭 영역은 SiGeC 층에 인장 왜곡을 주는 조성비의 영역을 나타내고, 도 3 중의 실선은 SiGeC 층과 Si 층의 격자 부정합이 0 요컨대 양자가 격자 정합하기 위한 각 원소의 조성비의 조건을 나타낸다. Ge의 격자정수는 Si의 격자정수보다도 4.2% 크고, C의 격자정수는 Si의 격자정수보다도 34.3% 작기 때문에, Ge의 조성비를 C의 조성비보다도 8.2배 크게 함으로써 SiGeC 층의 격자정수를 Si 층의 격자정수에 일치시킬 수 있다.

본 실시예에 있어서의 SiGeC 층(14n)에서는, Ge의 조성율이 8.2%(x= 0.082)이고, C의 조성율이 1%(y= 0.01)인 것으로부터, 도 3보다 Si 기판과의 격자 부정합이 0이고, SiGeC 층(14n)과 아래쪽의 Si 층(13n)은 같은 격자정수를 갖고 있는 것을 알수 있다.

다음에, 도 4는 가로축에 C의 조성비를 잡고, 세로축에 에너지 레벨을 잡은 경우에, SiGeC 층과 Si 층의 경계면에 있어서의 전도대의 밴드 오프셋 값 ΔEc 및 가전자대의 밴드 오프셋 값ΔEv가 변화하는 형태를 보이고 있다. 단지, 검은 고리형은 가전자대의 밴드 오프셋 값ΔEv이고, 흰 고리형은 전도대의 밴드 오프셋 값ΔEc를 나타내고 있다. 또한, 에너지의 원점은 전도대에 대해서는 Si의 전도대 하단의 에너지 값으로 잡고, 가전자대에 대해서는 Si의 가전자대의 상단의 에너지 값으로 잡고 있다. 또한, 도 4의 실선은 무왜곡계에 대응하며 도 4의 점선은 인장 왜곡계에 대응하고 있다.

도 4에 도시하는 바와 같이, 본 실시예의 SiGeC 층 (C의 조성비가 0.0l) 및 Si 층간의 경계면에 있어서의 전도대 및 가전자대의 밴드 오프셋 값은, 각각 300 meV, 0 meV이고, SiGeC 층과 Si 층의 경계면으로서는 가전자대에는 밴드 불연속부가 없고, 전도대에만 밴드 불연속부가 형성되는 것을 알수 있다. 또한, 본 실시예의 SiGeC 층(14n)에서의 C의 조성비는 0.01이기 때문에, SiGeC 층(14n)과 Si 층(13n)은 격자정합하고 있다. 따라서, 2차원 전자 가스가 주행하는 채널이 형성되는 SiGeC 층(14n) 내에서, 아래쪽의 Si 층(13n)과의 격자 부정합에 기인하는 전위 등의 결함의 발생을 방지할 수 있다.

한편, 본 실시예에 있어서의 SiGeC 층(14n)과 Si 층(13n) 사이의 경계면에 있어서의 가전자대에는 밴드 불연속부가 없기 때문에, SiGeC 층(14n) 내에 정공을 폐쇄할 수 없다. 따라서, 정공을 캐리어로 하는 PM0S 트랜지스터의 경우는 SiGe 층(15p)과 Si 층(17p)의 헤테로 접합을 이용하고 있다. SiGe 단결정의 격자정수는 Si 단결정의 격자정수보다 크고, 더구나, SiGe 층(15p)은 Si 층(13p)과 격자정합하고 있는 SiGeC 층(14p) 위에 위치하고 있기 때문에, 압축왜곡에 의한 밴드 구조의 변화에 의해 가전자대에서의 밴드 오프셋 값이 커지고 있다. 이 경우도 게이트로부터의 전계 인가시에 밴드 경사에 의해 정공이 2차원적으로 폐쇄되어(2DHG) 캐리어 축적층으로 된다. 따라서, SiGe 층(15p) 내의 캐리어 축적층이 정공이 고속으로 주행하기 위한 채널로 된다.

이상과 같이, 본 실시예의 구조에 의하면, NMOS 트랜지스터에 있어서는, SiGeC 층(14n) 에서의 각 원소 Si, Ge, C의 조성비의 조정에 의해 전도대의 밴드 오프셋 값을 2차원 전자 가스를 축적하는데 충분한 값으로 유지하면서, SiGeC 층과 Si 층의 사이의 격자정합을 도모할 수 있다. 따라서, SiGeC 층 안에서의 2차원 전자 가스가 높은 캐리어 이동도를 이용한 동작 속도의 고속화를 실현하면서 결함밀도의 저감에 의한 높은 신뢰성을 발휘할 수가 있다. 또한, SiGeC 층(14n)과 Si 층(13n) 사이의 경계면에 있어서의 가전자대에는 밴드 불연속부가 없기 때문에, SiCeC 층(14n) 내에 정공을 폐쇄할 수 없지만, SiGe 층(15p)과 Si 층(17p)의 헤테로 접합을 이용함으로써 정공을 캐리어로서 이용하는 PM0S 트랜지스터의 채널을 형성할 수가 있어 고속동작을 실현할 수가 있다.

그리고, 속도가 큰 NMOS 트랜지스터와 SiGe를 이용하여 가전자대의 밴드 불연속부를 형성하여 속도가 큰 PM0S 트랜지스터를 집적함으로써, 고성능인 HCMOS 장치를 실현할 수가 있다.

또, 본 실시예로서는, Ge의 조성율을 8.2%, C의 조성율을 1%로 하였지만, 도 4로부터 격자 정합계에서 밴드 불연속부 요컨대 밴드 오프셋 값 ΔEv가 가장 커지도록 하기 위해서는, C의 조성비를 크게

GF Exhibit 1124 - 2011/2704

하면 되는 것을 알 수 있다. 이와 같이 큰 밴드 오프셋 값 ΔEv를 설정함으로써, 헤테로 경계면에 폐쇄된 2차원 전자 가스(2DEG)는, 전자의 농도가 높게 되더라도 헤테로 경계면을 넘는 일이 없고 안정되게 주행할 수가 있다. 특히, C의 조성비를 0.01□0.03의 범위로 조정하는 것이 바람직하다. 이 범위 내에서는, 무왜곡계 및 인장 왜곡계 중 어디에서도 2차원 전자 가스를 폐쇄하기 위한 캐리어 축적층을 형성하는 데 적정한 밴드 오프셋 값 ΔEv(=-0.2□-0.6eV)를 얻을 수 있다.

또, 본 실시예로서는, SiGe 층(15p) 에서의 Ge의 조성율을 30%로 하였지만, 밴드 오프셋 값이 가장 커지도록 Ge의 조성율을 크게 하고 압축왜곡을 크게 하여도 된다.

또한,HCMOS 장치는 Si 기판 상에 형성하기 때문에, 소자의 스피드가 요구되는 곳에는 이 HCMOS 장치를 이용하고, 그 이외에는 통상의 Si 단일 조성을 갖는 활성 영역 상에 형성한 CM0S 장치를 제작하여도 된다. 이와 같이 구성함으로써 Si 기판에 직접 제작하는 M0S 형 전계 효과 트랜지스터의 집적화도 가능하게 된다. 또, SiGeC를 이용한 장치로서는, 동일 기판 상에 p, n 형의 트랜지스터를 형성할 필요는 없다. 예컨대, 이동 통신기기에 이용하는 집적 회로의 경우, 고속동작이 요구되는 고주파 영역에서 사용되는 증폭기, 믹서 등은 상보형 회로를 구성할 필요는 없기 때문에, p, n 형 중의 한 편만(예컨대 n 형)의 SiGeC를 이용한 MOS 트랜지스터로 구성하여, 상보형 회로를 구성할 필요가 있는 디지털 신호처리를 하는 부분을 Si 단일 조성을 이용한 CM0S 장치로 구성하는 것 등이 고려된다.

다음에, 제 1 실시예의 HCMOS 장치의 제조방법에 관해서, 도 5의 (a)□(f)를 참조하면서 설명한다. 도 5의 (a)□(f)는 도 1에 나타내는 HCMOS 장치의 구조를 실현하기 위한 제조공정의 일례를 나타내는 단면도이다.

우선, 도의 5(a)에 나타내는 공정에서, Si 기판(10)에 p 홀(11), n 홀(12)을 이온 주입에 의해 형성한다.

다음에, 도 5의 (b)에 나타내는 공정에서 각 홀(11,12)상에, UHV-CVD 법에 의해 δ 도핑층을 포함하는 Si 층(13)과, SiGeC 층(14)(Ge:8.2%, C:1%)과, SiGe 층(15)과, Si 층(17)을 각각 성장시킨다. 또, δ 도핑층 및 스페이스층도 형성되어 있지만, 보기 쉽게 하기 위해서 이것들의 층의 도시는 생략되어 있다.

다음에, 도 5의 (c)에 나타내는 공정에서, PMOS 트랜지스터, NMOS 트랜지스터를 전기적으로 분리하기 위해서, 트랜치 분리용의 홈을 형성한 후, 이 홈을 실리콘 산화막으로 매립하여 트랜치 분리(20)를 형성한다. 이 처리에 의해, Si 층 (13), SiCeC 층(14), SiGe 층(15), Si 층(17)이 각각 NMOS 트랜지스터 측의 Si 층(13n), SiGeC 층(14n), SiGe 층(15n), Si 층(17n)과, PMOS 트랜지스터 측의 Si 층(13p), SiGeC 층(14p), SiGe 층(15p), Si 층(17p)과 분리된다. 또, Si 층(17n, 17p)의 표면을 산화하여 게이트 절연막(19n, 19p)을 각각 형성한다.

다음에, 도 5의 (d)에 나타내는 공정에서 기판의 전면 상에 폴리실리콘막을 퇴적한 후, 이것을 패터닝하여 NMOS 트랜지스터 및 PMOS 트랜지스터의 각 게이트 절연막(19n, 19p) 위에 게이트 전극(l8n, 18p)을 각각 형성한다. 그 후, 각 게이트 전극(18n, 18p)을 마스크로서 NMOS 트랜지스터 측에는 인 이온(P+)의 주입에 의해 소스□드레인 영역(16n)을 형성하고, PM0S 트랜지스터 측에는, 붕소 이온(B+)의 주입에 의해 소스□드레인 영역(16p)을 각각 형성한다. NMOS 트랜지스터의 소스□드레인 영역(16n)의 깊이는 적어도 SiCeC 층(14n) 내의 캐리어 축적층보다도 깊으면 되고, PMOS 트랜지스터의 소스□드레인 영역(l6p)의 깊이는, 적어도 SiGe 층(15p) 내의 캐리어 축적층보다 깊으면 된다. 이것은, SiGeC 층(14n), SiGe 층 (15p) 내의 각 캐리어 축적층에 채널이 형성되기 때문이다.

다음에, 도 5의 (e)에 나타내는 공정에서, 게이트 절연막(19n, 19p) 중 소스□드레인 영역(16n, 16p)의 위쪽의 부분에 개구를 형성하여, 도 5의 (f)에 나타내는 공정에서, 게이트 절연막(19n, 19p)의 개구에 소스□드레인 전극(21n, 21p)을 각각 형성한다.

GF Exhibit 1124 - 2012/2704

이에 따라, S i 기판(10) 위에 NMOS 트랜지스터, PMOS 트랜지스터로 이루어지는 HCMOS 장치가 형성된다.

이와 같이, 본 실시예의 제조방법에 의하면, NMOS 트랜지스터, PMOS 트랜지스터에서 다른 채널을 형성해야 하지만, 결정 성장은 NM0S 트랜지스터, PM0S 트랜지스터에 공통으로 할 수 있어 간단히 제조할 수가 있다.

(제 2 실시예)

상술한 제 1 실시예로서는, SiGeC 층을 실리콘에 격자 정합시킨 것을 이용하여 전계 효과형 트랜지스터를 형성하였지만, 본 실시예에서는 결정성의 열화가 없는 범위에서 SiGeC 층에 적극적으로 왜곡을 도입하고, 이 왜곡에 의한 밴드 구조의 변화를 이용한 트랜지스터로 하는 것이다. 본 실시예에 의한 HCMOS 장치의 구조는 기본적으로는, 도 1에 나타내는 제 1 실시예에 의한 PM0S 트랜지스터, NMOS 트랜지스터를 1개의 트랜지스터 내에 실현한 구조로 되어 있다.

도 6의 (a)□(c)는, 각각 SiGeC 층에 압축왜곡을 발생시킨 경우, SiGeC 층을 Si 층에 격자 정합시킨 경우(왜곡 없슴) 및 SiGeC 층에 인장왜곡을 발생시킨 경우에 있어서의 결정 구조의 상태를 도시한 도면이다. 도 6의 (a)에 도시한 바와 같이, SiGeC 층의 격자정수를 Si 층의 격자정수보다 크게 하면 SiGeC 층에는 압축왜곡이 생겨 SiGeC 층에 있어서의 전도대의 하단과 가전자대의 상단 사이의 밴드 갭 값이 확대된다. 한편, 도 6의 (c) 에 도시한 바와 같이 SiGeC 층의 격자정수를 Si 층의 격자정수보다 작게 하면 SiGeC 층에는 인장왜곡이 생겨 SiGeC 층에 있어서의 전도대의 하단과 가전자대의 상단 사이의 밴드 갭이 축소된다. 즉, SiGeC 층의 왜곡에 의해 밴드 구조가 변화하기 때문에 이 효과를 적극적으로 이용함으로써 SiGeC 층에 근접하는 Si 층 등의 층의 밴드 오프셋 값을 변경할 수가 있다.

여기서, SiGeC 층의 격자정수를 Si 층의 격자정수로부터 벗어나게 한 경우에도 SiGeC 층의 두께를 격자 완화가 일어나지 않고 왜곡이 축적되는 정도로 함으로써 전위 등의 결정 결함의 발생에 기인하는 소자의 신뢰성의 저하를 효율적으로 방지할 수가 있다.

도 7의 (a), (b)는, 본 실시예에 의한 전계 효과 트랜지스터의 채널영역에서의 밴드 구조도 및 단면도이다. Si 기판의 위에 Si 층(13n)을 성장시킨 후, C의 조성비를 크게 한 SiGeC 층(14n)(Ge를 10%, C를 4%)을 성장시킴으로써, SiGeC 층(14n) 에서의 밴드 갭 값은 크고, 격자정수는 작아지도록 설정할 수가 있다. 그리고, SiGeC 층(14n)의 두께를 격자완화가 일어나지 않고 왜곡이 축적되는 정도로 작게 함으로써, SiGeC 층(14n)은 인장왜곡을 받는다. 따라서, C의 조성비를 크게 하는 것에 의한 밴드 갭 값의 증대 효과에 덧붙여, SiGeC 층(14n)의 인장왜곡에 의해, SiGeC 층(14n)에서 Si 층(13n)의 경계면에 있어서의 전도대의 밴드 오프셋 값이 커져 2차원 전자 가스(2 DEG)의 폐쇄 효율이 향상한다.

또, SiGeC 층(14n)은 격자 완화되지 않기 때문에 표면의 격자정수는 Si 층 (13n)의 격자정수에 일치하고 있다. 따라서, SiGeC 층(14n)의 위에 SiGe 층(15p)을 성장시키면 SiGe 층(15p)의 격자정수가 Si 층(13n)의 격자정수보다 커지기 때문에 SiGe 층(15p)은 압축왜곡을 받는다.

따라서, 본 실시예에 의한 반도체 장치에 의하면, SiGeC 층(14n)에 인장왜곡, SiGe 층(15p)에 압축왜곡이 도입됨으로써, SiGeC 층(14n)과 Si 층(13n)의 경계면에 있어서의 전도대에서의 밴드 오프셋 값을 크고 또한 SiGe 층(15p)과 Si 층(17p)의 경계면에 있어서의 가전자대에서의 밴드 오프셋 값을 크게 하고, 이 트랜지스터를 NMOS 트랜지스터로서 사용하는 경우에는 SiGeC 층(14n)에 형성되는 채널을 이용하는 한편,PMOS 트랜지스터로서 사용하는 경우에는 SiGe 층(15p)에 형성되는 채널을 이용함으로써 공통의 게이트 전극이나 소스□드레인 영역을 갖으면서 채널 위치가 다른 HCMOS 장치를 형성할 수가 있다.

더구나, 각 층의 두께를 적정히 설정함으로써, 격자 부정합에 의한 전위나 결함의 도입이 없고, 양호한 결정성에 의한 신뢰성이 높은 전계 효과형 트랜지스터를 갖는 HCMOS 장치를 얻을 수 있다.

GF Exhibit 1124 - 2013/2704

또, 상술한 도 4의 점선은, 본 실시예에 있어서의 SiGeC 층(14n)에 0.25%의 인장 왜곡이 가해지도록 조성을 나타내고 있다. 일반적으로, SiGeC 층에 있어서의 Ge의 조성비가 C의 조성비의 8.2배인 때에 Si 층에 격자정합하게 되므로, Ge의 조성비를 C의 조성비의 8.2배보다 작게 함으로써 SiGeC 층(14n)에 인장왜곡을 도입할 수가 있다. 또한, C의 조성비를 y로 하였을 때 Ge의 조성을 8.2y-0.12로 한 경우, SiGeC 층(14n)의 격자정수를 Si 층(13n)의 격자정수보다 0.25% 작게 할 수가 있다.

도 4에 도시한 바와 같이, 무왜곡계의 경우와 같이 SiGeC 층(14n)과 Si 층(13n)의 경계면에서는 가전자대에는 밴드 불연속부가 없고 전도대에만 밴드 불연속이 형성되는 것을 알 수 있다. C의 조성율이 2% 이하의 경우는 전도대의 밴드 오프셋 값은 무왜곡의 경우와 거의 동일하며, C의 조성율과 Ge의 조성율의 비가 격자 정합의 조건을 만족하는 값으로부터 벗어나더라도 격자정합계와 거의 같은 소자특성을 얻을 수 있다. 이 것은, SiGeC 층(14n)을 결정 성장하는 때의 C의 조성율과

Ge의 조성율의 제어의 면에서 본 조건에 폭을 유지시키는 것을 의미하고, SiGeC층의 결정성장을 용이하게 한다. 또, C의 조성율이 2% 이상일 경우 무왜곡의 경우와 비교하여 같은 C의 조성율에서도 밴드 오프셋 값을 크게 할 수 있다. 이것에 의해 밴드 오프셋 값을 더욱 더 크게 할 경우에도 대응할 수 있다.

여기에서는, SiGeC의 격자정수를 Si보다 작게 하여 사용하고 있지만, 층의 두께는 격자 완화가 일어나지 않는 왜곡이 축적되는 정도이기 때문에 전위 등의 결정 결함에 의해 소자의 신뢰성이 저하되지는 않는다.

(제 3 실시예)

상술한 제 1 실시예에서는, 전계 효과 트랜지스터의 채널영역에 SiGeC 층을 Si 층에 격자정합시킨 헤테로 구조를 형성하여 헤테로 경계면에 있어서의 밴드 불연속부에 전자 또는 정공을 폐쇄하여 캐리어로서 이용하였다.

본 실시예에서는, 캐리어를 폐쇄하는 영역을 헤테로 경계면이 아니라 Si/SiGeC/Si 또는, Si/SiGe/Si의 구조로 양자 우물 구조를 형성하고 장벽층으로는 끼일 수 있는 양자 우물(SiGeC, SiGe)를 채널로서 동작하는 트랜지스터를 설치한다.

도 8은, 본 실시예에 의한 HCMOS 장치의 단면도이다. Si 기판(30)상에, NMOS 트랜지스터와 PMOS 트랜지스터가 형성된 CMOS 장치구조이다. 이 구조에서는, 실리콘 기판(30)상에 p홀(31) 및 n홀(32)을 설치하고 있는 점과, 그 위에 V 족 원소가 고농도로 도핑된 δ 도핑층을 갖는 제 1 Si 층(33n, 33p)을 마련하고 있는 점은, 제 1 실시예에 있어서의 도 1에 나타내는 HCMOS 장치의 구조와 동일하다. 단지, 이 제 1 Si 층(33n, 33 p) 상의 PMOS 트랜지스터, NMOS 트랜지스터의 구조는 상기 제 1 실시예의 구조와 다르다.

NMOS 트랜지스터에 있어서는, 제 1 Si 층(33n) 위에, 제 1 Si 층(33n)에 격자정합하는 조성을 갖는 SiGeC 층(34n)이 형성되어 있고, 또 SiGeC 층(34n) 위에 제 2 Si 층(35n)이 적층되어 있다. 본 실시예에서는, 제 1 Si 층(33n)-SiGeC 층(34n)과 제 2 Si 층(35n)에 걸치는 전도대에서, 2개의 밴드 불연속부에 의해서 좁아지는 양자 우물 영역(SiGeC 층(34n))이 존재하기 때문에, 이 양자 우물 영역인 SiGeC 층(34n)에 캐리어인 2차원 전자가스(2 DEG)를 폐쇄하기 위한 캐리어 축적층이 형성된다(도 8의 오른쪽의 밴드 도 참조). 즉, NMOS 트랜지스터의 동작시에는 SiGeC 층(34n)에 채널이 형성된다. 또, 제 2 Si 층(35n) 위에, 막 두께가 작은 SiGe 층(36n)과, 제 3 Si 층(37n)이 차례로 형성되어 있다.

이 구조에 의해, 상기 제 1 실시예와 같이, Si 층에 비교해서 전자의 이동도가 큰 SiGeC 층(34n)에 캐리어의 이동을 위한 채널이 형성되기 때문에, 동작 속도가 큰 NMOS 트랜지스터를 얻을 수 있다. 덧붙여, 양자 우물로 되는 SiGeC 층(34n)의 막 두께가 작기 때문에 캐리어의 폐쇄 효율이 상기 제 1 실시예에 있어서의 구조보다 향상되어 혼합 결정비가 작은 계로 실현될 수 있다. 그 때문에, 혼합

GF Exhibit 1124 - 2014/2704

결정화에 따르는 결정구조의 규칙성 악화에 기인하는 캐리어의 산란 등의 캐리어로 되는 전자의 이동도를 열화시키는 요인을 억제할 수 있다.

PMOS 트랜지스터에 있어서도, 제 1 Si 층(33p) 위에 제 1 Si 층(33p)에 격자정합하는 조성을 갖는 SiGeC 층(34p)과, 제 2 Si 층(35p)과, 막 두께가 작은 SiGe 층(36p)과, 제 3 Si 층(37p)이 차례로 형성되어 있는 점은 상기 NMOS 트랜지스터의 구조와 동일하다. 단지, PMOS 트랜지스터의 경우는, 제 2 Si 층(35p)과 SiGe 층(36p) 및 제 3 Si 층(37p)에 걸치는 가전자대에 있어서, 2개의 밴드 불연속부에서 좁아지는 양자 우물 영역(SiGe 층(36p))이 존재하고, 이 양자 우물 영역에 캐리어인 정공을 2차원적으로 폐쇄하기 위한 캐리어 축적층이 형성된다. 즉, PM0S 트랜지스터의 동작시에는, SiGe 층(36p)에 채널이 형성된다. SiGe 층(36p)도 Si 층에 비교해서 정공의 이동도가 크기 때문에, 이 PM0S 트랜지스터의 동작속도도 커진다.

또, NMOS 트랜지스터, PMOS 트랜지스터에 있어서 기판 위에는 실리콘 산화막으로 이루어지는 게이트 절연막(39n, 39p)이 형성되고, 게이트 절연막(39n, 39p) 위에는 게이트 전극(38n, 38p)이 형성되어 있다. 게이트 전극(38n, 38p)의 양측에는 소스□드레인 영역(42n, 42p)이 형성되고 소스□드레인 영역(42n, 42p) 위에는 소스□드레인 전극(41n, 41p)이 콘택트하고 있다. 또, 말할 필요도 없지만, NMOS 트랜지스터, PMOS 트랜지스터에 있어서, 양자 우물 영역인 SiGeC 층(34n), SiGe 층(36p)에서의 전자, 정공의 주행은 게이트 전극(38n, 38p)에 인가되는 전압에 의해 각각 제어되고 있다.

또한, NMOS 트랜지스터와 PMOS 트랜지스터의 사이는 분리용 홈에 실리콘 산화막을 매립하여 되는 트랜치분리(40)가 형성되어 있고, 이 트랜치분리(40)에 의하여 NMOS 트랜지스터, PMOS 트랜지스터는 서로 전기적으로 분리되어 있다.

본 실시예의 HCMOS 장치에 의하면, 제 1 실시예와 같이, NMOS 트랜지스터에 있어서는, Si 층에 격자정합함과 동시에 양자 우물 영역으로 되는 SiGeC 층(34n)이 형성되어 있고, 이 SiGeC 층(34n)에 전자가 주행하기 위한 채널이 형성된다. 또한, PM0S 트랜지스터에 있어서도, 양자 우물 영역으로 되는 SiGe 층(36p)이 형성되어 있고, 이 SiGe 층(36p)에 정공이 주행하기 위한 채널이 형성된다. 따라서, 캐리어 폐쇄 효율이 높은 양자 우물 구조를 이용한 스위칭 속도가 큰 NMOS 트랜지스터와 PMOS 트랜지스터를 집적함으로써 고성능인 HCMOS를 실현할 수가 있다.

단지, 본 실시예에 있어서, 소자의 속도가 요구되는 회로에 이 HCM0S 장치를 이용하고, 그 이외의 회로에는 통상의 Si 기판 상에 형성한 CM0S 장치를 제작하여도 되고, Si 기판 상에 직접 형성한 M0S형 전계 효과 트랜지스터의 집적도 가능하다.

또, 반드시 NMOS 트랜지스터 및 PMOS 트랜지스터의 채널의 쌍방이 양자 우물 영역으로 되어있지 않더라도 된다.

다음에, 제 3 실시예에 의한 HCMOS 장치의 제조방법에 관해서, 도 9의 (a)□(f)를 참조하면서 설명하기로 한다. 도 9의 (a)□(f)는, 도 8에 나타내는 HCM0S 장치의 구조를 실현하기 위한 제조공정의 일례를 나타내는 단면도이다.

우선, 제조공정의 개략을 설명하면, SiGeC 층(34), 제 2 Si 층(35) 및 SiGe 층(36)을 성장시킬 때, SiGeC 층(34)및 SiGe 층(36)의 막 두께를 양자 우물 구조가 되도록 10nm이하, 예컨대 3nm로 하고 있다. 그 밖의 부분은, 도 5(a)□(f)에 나타내는 공정과 거의 같은 공정으로 형성된다.

우선, 도 9의 (a)에 나타내는 공정에서, Si 기판(30)에 p홀(31), n홀(32)을 이온 주입에 의해 형성한다.

그리고, 도 9의 (b) 에 나타내는 공정에서 p홀(31), n홀(32)상에, UHV-CVD 법에 의해 δ 도핑층을 포함하는 제 1 Si 층(33)과, SiGeC 층 (34)(Ge:36%, C:4%)과, 제 2 Si 층(35)과, SiGe 층(36) 및 제 3 Si 층(37)을 차례로 성장시켜 간다.

GF Exhibit 1124 - 2015/2704

다음에, 도 9의 (c)에 나타내는 공정에서, PMOS 트랜지스터, NMOS 트랜지스터를 전기적으로 분리하기 위하여 트랜치분리용 홈을 형성한 후, 이 홈을 실리콘 산화막으로 매립하여 트랜치분리(40)를 형성한다. 이 처리에 의해 제 1 Si 층(33), SiGeC 층(34),제 2 Si 층(35), SiGe 층(36),제 3 Si 층(37) 및 게이트 절연막(39)이, 각각 NMOS 트랜지스터 측의 제 1 Si 층(33n), SiGeC 층(34n), 제 2 Si 층(35n), SiGe 층(36n), 제 3 Si 층(37n) 및 PMOS 트랜지스터 측의 제 1 Si 층(33p), SiGeC 층(34p), 제 2 Si 층(35p), SiGe 층(36p), 제 3 Si 층(37p)으로 분리된다. 그 후, 제 3 Si 층(37n, 37p)의 표면을 산화하여, 게이트 절연막(39n, 39p)을 형성한다.

다음에, 도 9의 (d)에 나타내는 공정에서, 게이트 전극(38n, 38p)을 형성한 후, NMOS 트랜지스터 측에는 인 이온(P+)의 주입에 의해, 소스□드레인 영역(42n)을 형성하고, PMOS 트랜지스터 측에는 붕소 이온(B+)의 주입에 의해, 소스□드레인 영역(42p)을 형성한다. NMOS 트랜지스터의 소스□드레인 영역(42n)의 깊이는 적어도 SiGeC 층(34n)보다 깊으면 되고, PMOS 트랜지스터의 소스□드레인 영역(42p)의 깊이는 적어도 SiGe 층(36p)보다 깊으면 된다. 이것은, SiGeC 층(34)n, SiGe 층(36p) 내에 채널이 형성되기 때문이다.

그 다음, 도 9의 (e)에 나타내는 공정에서, 소스□드레인 영역(42n, 42p)의 위쪽 부분의 게이트 절연막(39n, 39p)에 개구를 형성하여, 도 9의 (f)에 나타내는 공정에서 그 개구에 소스□드레인 전극(41n, 41p)을 각각 형성한다.

이상의 공정에 의해, 제 3 실시예에 의한 NMOS 트랜지스터, PMOS 트랜지스터로 이루어지는 HCMOS 장치의 구조가 실현된다.

본 실시예의 제조방법에 의하면, NMOS 트랜지스터의 채널을 헤테로 접합을 이용한 양자 우물 구조의 SiGeC 층(34n)으로 하고, PMOS 트랜지스터의 채널을 헤테로 접합을 이용한 양자 우물 구조의 SiGe 층(36p)으로 하는 HCMOS 장치가 용이하게 형성된다. 더구나, 본 실시예의 제조방법에 의하면, NM0S 트랜지스터, PM0S 트랜지스터에 다른 채널을 형성해야 하지만, 결정성장은 NMOS 트랜지스터, PMOS 트랜지스터에 공통으로 할 수 있어 간단히 제조할 수가 있다.

(제 4 실시예)

도 10은, 제 4 실시예에 의한 전계 효과 트랜지스터의 구조를 나타내는 단면도이다. 본 실시예는, 헤테로 전계 효과 트랜지스터에 적합한 소스□드레인 콘택트를 제공하는 구조에 관한 것이다.

도 10에 도시된 바와 같이, Si 층으로 이루어지는 홀(51) 위에는, SiGe 버퍼층(52)과, δ 도핑층(53)과, 스페이스층(54)과, n-채널층(67)과, i-Si 층(55)과, i-$Si_{1-x}Ge_x$ 층(56)과, i-Si 층(57)과, 게이트 절연막(58)이 형성되어 있다. 그리고, 게이트 절연막(58) 위에 게이트 전극(65)이 형성되어, i-$Si_{1-x}Ge_x$ 층(56) 중 게이트 전극(65)의 양쪽에 위치하는 영역 위에, 소스□드레인 콘택트 W 층(61)과 Al 소스□드레인 전극(63)이 차례로 형성되어 있다. 또한, 게이트 전극(65)의 양측에서 SiGe 버퍼층(52)의 일부, δ 도핑층(53), 스페이스층(54), n-채널층(67), i-Si 층(55), i-$Si_{1-x}Ge_x$ 층(56) 및 i-Si 층(57)에 걸치는 영역에, 소스□드레인 영역(59)이 형성되어 있다. 또, 게이트 전극(65)과 Al 소스□드레인전극(63)의 사이는, 제 1층의 절연막(66)에 의하여 매립되고 있다.

여기서, 상기 전계 효과 트랜지스터의 각음의 구조에 관해서 설명하기로 한다.

우선, SiGe 버퍼층(52) 내에서의 Ge의 조성율은, 위쪽으로 가면서 커지고 있다. 이 SiGe 버퍼층(52)은, SiGe 혼합결정을 격자 완화시키는 데 충분한 막 두께로 형성함으로써, Si보다 큰 격자정수를 갖고, 그 위에 왜곡 효과를 이용한 n-채널의 형성이 가능가게 된다. 또, 이러한 격자 완화시킨 SiGe 버퍼층을 이용하지 않고, Si 기판에 격자 정합시킨 상태로 Si 층과 SiGe 층의 헤테로 접합을 형성한 경우,

GF Exhibit 1124 - 2016/2704

가전자대에는 단차가 큰 불연속부가 나타나지만, 전도대에는 불연속부는 거의 나타나지 않기 때문에, 2차원 전자 가스를 폐쇄하여 n-채널을 형성하는 것은 곤란하다.

여기서, SiGe 버퍼층 (52)중에서의 Ge의 조성율은, 예컨대 0%□30%까지 연속적으로 또는 얇은 층마다 단계적으로 변화하고 있다. 이 때, 각 층에서 격자완화를 발생시켜 버퍼층의 최상면에서 기판면내의 격자정수가 체적이 $Si_{0.7}Ge_{0.3}$과 동일하도록 한다. 조성율을 세로방향으로 변화시키는 것은, 격자완화에 따르는 전위 등의 결정 결함이 그 위의 채널에 주는 영향을 작게 하기 때문이다. 또, SiGe 버퍼층 (52) 전체의 막 두께는 대략 1μm 정도 필요하다.

이 SiGe 버퍼층(52)상에 불순물을 가하지 않은 $Si_{0.7}Ge_{0.3}$으로 이루어지는 스페이스층(54)을 배치한다. 이 스페이스층(54)과 그 위의 Si 층(55)의 헤테로 경계면에 존재하는 전도대의 불연속부에 캐리어 구조를 형성하여, 이 캐리어 축적층을 2차원적으로 전자를 폐쇄하는 n-채널(67)로 한다.

δ 도핑층(53)은 n-채널(67)에 캐리어인 전자를 공급하기 위하여 P나 As 라고 하는 V 족의 원소를 고농도로 도핑한 층이다. δ 도핑층 (53)상의 스페이스층(54)은 불순물을 도핑하지 않은 $Si_{0.7}Ge_{0.3}$으로 구성되고, n-채널(67)의 캐리어 전자와 δ 도핑층(53)의 이온을 공간적으로 분리함으로써, 캐리어 전자의 이온에 의한 산란을 저감하여 이동도를 향상시키는 역할을 갖는다. 이 스페이스층(54)의 막 두께는 두꺼울수록 이온화된 불순물에 의한 캐리어의 산란 효과를 저감할 수가 있지만, 반대로 캐리어 밀도가 감소하기 때문에 3 nm 정도의 두께로 하는 것이 바람직하다.

$i\text{-}Si_{1-x}Ge_x$ 층(56)과 i-Si 층(57)은, 헤테로 경계면에 가전자대에 단차를 형성하여 p-채널(68)을 형성하기 위해서 사용된다. X는 0.7전후로 설정하는 것이 바람직하다.

게이트 절연막(58)은 게이트 전극(65)과 그 아래의 반도체층 사이를 절연함으로써, 게이트 누설전류를 저감시켜 소자의 저소비 전력 동작을 가능하게 한다. 또, SiGe 층(56)을 산화하여 형성되는 산화막은 수용성으로 불안정한 막으로 되기 때문에, SiGe 계 전계 효과 트랜지스터에 있어서도 게이트 절열막으로서 실리콘 산화막을 이용하는 것이 바람직하다. 따라서, Si 계 헤테로 M0S 장치에 있어서는 게이트 절연막 바로 아래의 반도체층은 Si 층 인 것이 바람직하다.

즉, 본 실시예에 의한 전계 효과 트랜지스터는 상기의 적층막으로 이루어지는 채널영역과, 도 10의 점선으로 표시되는 소스□드레인 영역(59)과, 트랜지스터의 동작을 위한 전류의 도입□취득을 위한 Al 소스□드레인 전극(63)과, 전류를 제어하기 위한 전압을 인가하기 위한 게이트 전극(65)에 의해 구성되고 있다. 그리고, 이 전계 효과 트랜지스터를 n-채널 전계 효과형 트랜지스터로서 사용하는 경우에는 n-채널(67)을 형성시키도록 게이트 전극(65)에 전압을 인가하고, p-채널 전계 효과형 트랜지스터로서 사용하는 경우에는 p-채널(68)을 형성시키도록 게이트 전극(65)에 전압을 인가한다.

본 실시예에 의한 발명의 특징은, $i\text{-}Si_{1-x-y}Ge_xC_y$ 층($0\le x\le 1, 0\le y\le 1$)을 포함하는 제 1 반도체층과, 상기 제 1 반도체층과는 다른 밴드 갭을 갖는 제 2 반도체층과, 상기 제 1, 제 2 반도체층 사이의 경계면 부근의 영역에 형성된 캐리어 축적층을 갖는 채널 영역과, 제 3 반도체층과, 이 제 3 반도체층보다 큰 밴드 갭을 갖는 제 4 반도체층을 갖는 소스□드레인 영역과, 상기 제 3 반도체층의 바로 위에 형성된 저저항의 도체막으로 이루어지는 소스□드레인 콘택트층을 구비하고 있는 점이다.

그리고, 본 실시예의 전계 효과 트랜지스터를 n-채널 전계 효과형 트랜지스터로서 사용하는 경우에는, i-Si 층(55)은 $i\text{-}Si_{1-x-y}Ge_xC_y$ 층($0\le x\le 1, 0\le y\le 1$)을 포함하는 제 1 반도체층이고($x = y = 0$), SiGe 버퍼층(52)은 제 2 반도체층이고, $i\text{-}Si_{1-x}Ge_x$층(56)은 제 3 반도체층이며 i-Si 층(57)은 $i\text{-}Si_{1-x}Ge_x$층(56)보다 밴드 갭이 큰 제 4 반도체층으로서, 제 3 반도체층인 $i\text{-}Si_{1-x}Ge_x$층(56)의 바로 위에 소스□드레인 콘택트 W 층(61)이 형성되어 있다.

GF Exhibit 1124 - 2017/2704

한편, 본 실시예의 전계 효과 트랜지스터를 p-채널 전계 효과형 트랜지스터로서 사용하는 경우에는, $i\text{-}Si_{1-x}Ge_x$층(56)은 $i\text{-}Si_{1-x-y}Ge_xC_y$ 층($0\leq x\leq 1, 0\leq y\leq 1$)을 포함하는 제 1 반도체층인 (y= 0) 동시에 제 3 반도체층이며, i-Si 층(57)은 제 2 반도체층인 동시에 제 3 반도체층보다 밴드 갭이 큰 제 4 반도체층으로서, 제 3 반도체층인 $i\text{-}Si_{1-x}Ge_x$층(56)의 바로 위에 소스□드레인 콘택트 W 층(61)이 형성되어 있다.

이상과 같이, 본 실시예에서는, A1소스□드레인 전극(63)의 콘택트를 하는 기판측의 영역을, 채널 형성을 위한 각 반도체층 내 밴드 갭이 작은 층에 설치되어 있다. 이 실시예의 경우, p-채널 형성용의 Si 층(57)과 $i\text{-}Si_{1-x}Ge_x$층(56)의 헤테로 경계면 중, 밴드 갭이 작은 $i\text{-}Si_{1-x}Ge_x$층(56)의 바로 위에 소스□드레인 콘택트 W 층 (61)을 설치하고 있다. 이에 따라, 최상층의 반도체층인 i-Si 층(57)의 바로 위에 콘택트를 설치하는 것보다 콘택트 저항이 작아지고, 소자의 저소비 전력과 고속동작이 가능하게 된다.

또, Si 층상의 $Si_{0.7}Ge_{0.3}$층의 위에 W를 성장시킨 후, 금속(이 경우 Al)을 퇴적시키면, 대단히 저항이 낮은 콘택트를 얻을 수 있다. 이 SiGe 막을 이용한 콘택트는 종래의 CMOS 장치로 일반적으로 저저항 콘택트로서 이용되고 있는 실리사이드 기술을 이용한 저저항 콘택트보다 1자리수 저항값이 낮은 콘택트를 얻을 수 있다 (IEEE Electron Device Letters 지 vol. l7. No.7, l996 pp360).

이 논문에서는 SiGe 층은 소스□드레인 전극 콘택트 형성을 위해서만 성장시켜지고 있지만, 본 실시예와 같이, 채널 형성용의 SiGe 층에 콘택트를 잡는 구조를 잡으면, 후술하는 트랜지스터 제조방법으로 분명해지는 바와 같이, 새롭게 SiGe 결정을 성장시킬 필요가 없어져 생산성이 향상된다.

다만, 본 실시예에 있어서, 장치의 속도가 요구되는 곳에 이 HCMOS 장치를 이용하고, 그 이외에는, 통상의 Si 기판상에 형성한 CMOS 장치를 제작하여도 되고, Si 기판상에 직접 형성한 M0S 형 전계 효과 트랜지스터의 집적이 가능하다.

다음에, 본 실시예에 의한 전계 효과 트랜지스터의 제조방법에 관해서 설명하기로 한다. 도 11의 (a)□(e) 및 도 12의 (a)□(e)는, 도 10에 도시된 전계 효과 트랜지스터의 구조를 실현하기 위한 제조공정의 예를 나타내는 단면도이다.

우선, 도 11의 (a)에 나타내는 공정에서, 채널형성의 에피텍셜 성장에 앞서서, Si 기판(50)에 이온을 주입하고, NMOS 트랜지스터, PMOS 트랜지스터의 기초가 되는 p홀(51n), 및 n홀(51p)을 형성한다.

다음에, 도 11의 (b)에 나타내는 공정에서, 기판상에 에피텍셜 성장을 하기 전에, 기판에 RCA 세정법 등을 이용한 세정을 하여 표면의 불순물을 제거한다. 그 후, 표면의 산화막을 제거하고, 기판을 에피텍셜 성장장치에 삽입하여 진공상태로 가열을 하여 청정한 표면을 얻는다. 그리고, 이 청정한 표면상에 채널영역을 형성하기 위한 반도체층의 에피텍셜 성장을 한다. 이 반도체층에는, SiGe 버퍼층(52), δ 도핑층(53), 스페이스층(54), n-채널층(67),i-Si 층(55), $i\text{-}Si_{1-x}Ge_x$층(56), p-채널층(68), i-Si 층(57) 등이 포함된다. 단지, 보기 쉽게 하기 위하여 δ 도핑층 (53), 스페이스층(54), n-채널층(67) 및 p-채널층(68)의 도시는 생략한다. 이하, 이 반도체층 내의 각 층의 형성순서를 설명한다.

반도체층의 성장방법에 있어서는, 고체 소스를 이용하는 MBE 법이나 기체 소스를 이용하는 UHV-CVD 법 등이 이용될 수 있다. UHV-CVD 법의 경우 장치 내의 분위기를 우선 초고진공($1O^{-10}$ Torr 정도)으로 하여 결정성장에 필요한 소스를 진공용 기내에 도입하고 나서, $1O^{-5}$□$1O^{-6}$ Torr 정도의 진공도에 도달한 상태로 결정성장을 한다.

따라서, 본 실시예에 있어서도, 상술한 처리에 의해 기판에 청정한 표면을 생성한 후, 진공 용기 내의 진공도가 충분히 높게 된 시점에서 기판 온도를 500□700℃ 정도로 설정하여 각 반도체 결정층의 성장을 한다. 또, 기판 온도를 변화시키면, 단일의 반도체 결정층 내에서 조성비가 변화하는 등 결정의

GF Exhibit 1124 - 2018/2704

질에 영향을 주기 위하여, 기본적으로는 단일층을 성장시키고 있는 사이는 기판 온도를 변화시키지 않는다. 또한, 800℃ 이상이라고 하는 고온에서는 Ge와 Si가 상호 확산하여 헤테로 경계면의 급준성이 손상되거나, 왜곡 완화가 행하여져 채널특성이 악화하는 등 바람직하지 못한 일이 일어나기 때문에 성장온도는 상기 한 바와 같이 700℃ 이하를 선택한다.

결정성장은, 초고진공 상태로 한 진공용기 내에, 결정성장에 필요한 소스가스를 도입하는 것으로 한다. 결정성장에 사용하는 소스 가스로서는 Si 층의 성장용에는 지시랜을 사용하고 있다. SiGe 층의 성장에는 지시랜등의 Si 층을 성장시키기 위한 소스 가스에 가하여, 게르마늄을 Ge의 소스가스로서 사용한다. 이 때, 각 소스가스의 분압비의 조정에 의해 SiGe 층 내의 Si와 Ge의 조성비를 제어할 수가 있다. 가스유량은 진공도가 $1O^{-5}$□$1O^{-6}$Torr 정도가 되도록 조정한다.

우선, 조성비를 단계적으로 변화시키고 또한 격자 완화된 다수의 SiGe 층을 적층하여 SiGe 버퍼층(52)을 형성한다. 이 때, 조성비를 단계적으로 변화시키기 위하여, 상술한 바와 같이 Si의 소스가스의 분압과 Ge의 소스가스의 분압의 비를 단계적으로 변화시킨다.

다음에, δ 도핑층(53)의 형성에는 아루신 또는 포스핀이라고 하는 도우펀트 가스를, 지시랜 및 게르마늄과 동시에 진공용기 내에 도입한다.

여기서, δ 도핑층(53)에 도입한 불순물이 스페이스층(54)에 혼합되면, 트랜지스터 특성이 열화하기 때문에, 도우펀트 가스를 진공용기 내에 도입한 후는 일단 소스가스의 공급을 멈추고, 진공도가 충분히 향상된 후에 스페이스층(54)을 성장시키기 위한 가스를 도입하여 스페이스층 (54)을 성장시킨다. 스페이스층 (54)의 조성은 균일하게 $Si_{0.7}$ $Ge_{0.3}$으로 하여, 지시랜과 게르마늄의 유량을 고정하여 성장시킨다.

스페이스층(54)의 성장 후, 소스가스의 공급을 일단 정지하고 진공도가 향상되고 나서 지시랜만을 성장실에 도입하여, 불순물을 도핑하지 않은 i-Si 층(55)을 성장시킨다.

i-Si 층(55)의 성장 후, 다시 지시랜과 게르마늄을 성장실에 도입하여, i-$Si_{1-x}Ge_x$층(56)을 성장시킨다. Ge의 조성비는 70%으로 한다. i-$Si_{1-x}Ge_x$층(56)의 성장 후, 소스가스의 공급을 일단 정지한 후, 진공도가 향상되고 나서 지시랜만을 성장실에 도입하여 i-Si 층(57)을 성장시킨다.

이상의 처리에 의해, 채널영역을 구성하는 반도체층의 에피텍셜 성장공정은 종료한다.

다음에, 도 11의 (c)에 나타내는 공정에서는, 기판을 UHV-CVD 장치로부터 인출하여 열산화 화로 내에 도입하여, 최상층의 i-Si 층(57)의 표면을 산화하여 실리콘 산화막으로 이루어지는 게이트 절연막(58)을 형성한다.

다음에, 도 11의 (d)에 나타내는 공정에서, 게이트 절연막(58) 상에 게이트 전극(65)을 형성한다. 이 게이트 전극의 형성법은 종래의 CM0S 장치 공정과 마찬가지다. 즉, 폴리실리콘막을 퇴적하고, 불순물을 이온 주입한 후 드라이 에칭에 의해 폴리실리콘막을 패터닝하여 게이트 전극(65n, 65p)을 형성한다. 불순물 이온으로서는 불화 붕소이온(BF2+)을 사용할 수 있다. 이 게이트 전극용의 폴리실리콘막이 퇴적된 단계에서는 소스□드레인 영역은 형성되지 않는다.

다음에, 도 11의 (e)에 나타내는 공정에서, 게이트 전극(65n, 65p)을 마스크로서, 도우펀트가 되는 불순물 이온을 기판 내에 주입하여 소스□드레인 영역(59n, 59p)을 형성한 후, 콘택트를 취하기 위하여 기판상에 노출되는 산화막을 제거하기 위한 에칭을 한다. 또, 이온주입인 때는, 이온의 가속전압을 불순물 분포의 피크가 소스□드레인 전극의 콘택트를 설치하는 것과 같이 선택한다. 주입하는 불순물이온으로서는 NMOS 트랜지스터영역에는 n 형 불순물인 비소 이온(As+) 또는 인 이온(p+)을, PMOS 트랜지스터영역에는 p형 불순물인 붕소 이온(B+)을 사용한다. 따라서, NMOS 트랜지스터의 소스□

GF Exhibit 1124 - 2019/2704

드레인 영역(59n)을 형성하기 위한 이온 주입과, PMOS 트랜지스터의 소스□드레인 영역(59p)을 형성하기 위한 이온 주입은 각각 별개의 마스크를 이용할 필요가 있다.

또, 이온주입 직후는, 불순물의 활성화를 위한 아닐을 행한다. 단지, 아닐 열처리에 의해 헤테로 경계면에서의 Si와 Ge의 상호 확산이나, Si/SiGe 계에 존재하는 왜곡의 완화과정에서의 결정 결함의 발생이 없도록 1OOO℃ 정도로 단시간(30초)의 RTA (Rapid thermal anylling)을 하는 것이 바람직하다.

다음에, 도 12의 (a)에 나타내는 공정에서, 기판상에 다시 한번 포토 레지스터 마스크(도시 생략)를 형성하고, 드라이 에칭에 의해 NMOS 트랜지스터 형성 영역과 PMOS 트랜지스터 형성 영역 사이의 영역을 적어도 채널영역보다 깊게 들어가 소자분리용 홈(71)을 형성한다.

다음에, 도 12의 (b)에 나타내는 공정에서, 홈(71)을 포함하는 기판의 전면 상에 제 1 층 절연막(72)을 퇴적한다. 절연막을 구성하는 재료로서는 고온 처리를 피하기 위하여, 500℃ 이하로 성막되는 플라즈마 CVD 법에 의한 TEOS 막 등을 사용하는 것이 바람직하다. 이 때, 홈(71)에 매립된 절연막에 의해 트랜치분리(73)가 구성된다.

다음에, 본 실시예의 특징인 소스□드레인 콘택트 이하의 순서에 의해 형성한다. 단지, 도 10에 나타내는 구조를 실현하기 위한 공정은, 이하의 순서에 한정되는 것은 아니다.

본 실시예의 효과를 최대한 발휘하기 위해서는 최종적으로 콘택트의 기초가 되는 매우 얇은 특정한 반도체층이 존재할 필요가 있다. 그 때문에, 본 실시예에서는, 기초가 되는 특정한 반도체층으로서 i-Si_1-xGe_x층(56n, 56p)을 선택하여, i-Si_1-xGe_x층(56n, 56p)이 노출될 때까지 에칭을 한다. i-Si_1-xGe_x층(56n, 56p)을 노출시킬 때는 습식 에칭에 의한 선택성이 높은 에칭을 이용하는 것이 바람직하다. 단지, 습식 에칭은 다른 방향성이 결핍되고 미세 가공에 적합하지 않기 때문에 ,우선, 드라이 에칭에 의해 제 1 층의 절연막(72) 중 소스□드레인 전극을 형성하고자 하는 영역을 선택적으로 제거하여 컨택트 홀을 형성하고, 게이트 절연막(58n, 58p)을 노출시킨 후, 습식 에칭을 하는 것이 바람직하다. 이러한 처리의 예 로서는 예컨대 이하의 처리가 있다.

우선, 최상층의 산화막(게이트 절연막(58n, 58p))의 제거에는 잘 알려진 바와 같이 불산계의 용액을 사용한다. 그리고, i-Si 층(57n, 57p)이 노출되면, 불산은 실리콘을 거의) 제거하지 못하기 때문에, 에칭액을 i-Si 층(57)을 제거할 수 있는 에칭액으로 변경한다. 여기서, 본 실시예에서는, i-Si 층(57n, 57p)의 아래의 i-$Si_{1-x}Ge_x$층(56n, 56p)에 콘택트를 형성하기 때문에, i-$Si_{1-x}Ge_x$층(56n, 56p)을 그다지 에칭하지 않고, i-Si 층(57n, 57p)을 선택적으로 에칭할 수 있는 에칭액(엣첸트)을 선택한다. 그리고, 이 엣첸트를 사용하여, i-Si 층(57n, 57p)을 제거하여 i-$Si_{1-x}Ge_x$층(56n, 56p)을 노출시킨다. 이 때, i-$Si_{1-x}Ge_x$층(56n, 56p)의 일부가 오버 에칭에 의해 제거되어도 된다. 상술한 바와 같이, 이 i-$Si_{1-x}Ge_x$층(56n, 56p)은, NMOS 트랜지스터의 채널영역에 n-채널을 형성시키기 위하여 에피텍셜 성장시킨 것이다. 따라서, 본 실시예를 이용하면, SiGe 층을 이용한 저저항 콘택트를 형성하기 위하여 새롭게 i-$Si_{1-x}Ge_x$층(56n, 56p)을 성장시키기 위한 공정이 불필요하게 된다.

다음에, 콘택트를 형성하기 위하여, 이 노출된 i-$Si_{1-x}Ge_x$층(56n, 56p) 위에 저저항의 금속막을 퇴적시킨다. 이 금속막을 구성하는 금속 재료로서는, 상술한 바와 같이 텅스텐(W)을 사용하면 매우 저항값이 낮은 콘택트를 형성할 수가 있다. 그래서, 본 실시예에서는, LPCVD 법에 의해, WF6을 수소로 희석한 가스를 소스가스로서 이용하여, 온도조건을 400℃ 로서, i-$Si_{1-x}Ge_x$층(56n, 56p) 위에 소스□드레인콘택트 W 층(61n, 61p)을 선택 성장시키고 있다.

다음에, 도 12의 (e)에 나타내는 공정에서, 스퍼터링을 하여 기판의 전면 상에 A1합금막을 퇴적한 후 패터닝하여, A1 소스□드레인 전극(63n, 63p)을 형성한다. 이상의 공정에서, 소스□드레인 영역 상에 저저항의 콘택트를 형성할 수가 있다.

GF Exhibit 1124 - 2020/2704

상술한 바와 같이, Si 계 헤테로 M0S 장치에 있어서는, 게이트 절연막으로서 실리콘 산화막을 사용하는 관계상, 반도체 최상층은 밴드 갭이 큰 Si 층인 것이 바람직하기 때문에, 본 실시예와 같은 반도체층을 제거한 후 콘택트 금속층을 형성하는 기술은, Si 계 헤테로 M0S 장치의 형성에 특히 알맞은 기술이다.

(제 5 실시예)

상기 실시예에서는 Si와 SiGe로 이루어지는 헤테로 접합체를 이용한 채널구조를 대표로 들었지만, HCMOS 장치의 소스□드레인 영역에 저저항의 콘택트를 형성하는 발명은, 이러한 실시예에 한정되는 것이 아니라, Si와 이 실시예의 SiGe의 적층 구조 이외의 구성을 갖는 헤테로 에피텍셜 적층막에 의한 채널, 예컨대 Si와 i-$Si_{1-x-y}Ge_xC_y$층($0\leq x\leq 1, 0\leq y\leq 1$) 혼합 결정 반도체의 사이에 채널 형성한 것이라도 된다. 헤테로 경계면에 의한 채널형성에는, 반드시 밴드 갭이 다른 두 가지의 반도체의 접합이 필요하기 때문에 이러한 저저항의 콘택트 층의 형성이 유효하게 된다.

도 13은, 도 1에 나타내는 구조에 저저항의 콘택트 금속층을 형성한 제 5 실시예에 의한 HCMOS 장치의 단면도이다.

도 13에 도시하는 바와 같이, 본 실시예에 의한 HCMOS 장치에 있어서는, S iGe 층(15n, 15p)의 위에 소스□드레인 콘택트 W 층(25n, 25p)이 형성되어 있다.

본 실시예에 의한 발명의 특징은, 상기 제 1 실시예의 특징에 덧붙여 상기 제 4 실시예와 같이, $Si_{1-x-y}Ge_xC_y$층($0\leq x\leq 1, 0\leq y\leq 1$)을 포함하는 제 1 반도체층과, 상기 제 1 반도체층과는 다른 밴드 갭을 갖는 제 2 반도체층과, 상기 제 1, 제 2 반도체층 사이의 경계면 부근의 영역에 형성된 캐리어 축적층을 갖는 채널영역과, 제 3 반도체층과, 이 제 3 반도체층보다 큰 밴드 갭을 갖는 제 4 반도체층을 갖는 소스□드레인 영역과, 상기 제 3 반도체층의 바로 위에 형성된 저저항의 도체막으로 이루어지는 소스□드레인 콘택트층을 구비하고 있는 점이다.

그리고, 본 실시예의 NMOS 트랜지스터에 있어서는, SiGeC 층(14n)은 $Si_{1-x-y}Ge_xC_y$층($0\leq x\leq 1, 0\leq y\leq 1$)을 포함하는 제 1 반도체층으로, Si 층(13n)은 제 2 반도체층이고, SiGe 층(15n)은 제 3 반도체층이며, Si 층(17n)은 SiGe 층(15n)보다 밴드 갭이 큰 제 4 반도체층으로서, 제 3 반도체층인 SiGe 층(15n)의 바로 위에 소스□드레인 콘택트 W 층(25n)이 형성되어 있다.

한편, 본 실시예의 PMOS 트랜지스터에 있어서는, SiGe 층(15p)은 $Si_{1-x-y}Ge_xC_y$층($0\leq x\leq 1, 0\leq y\leq 1$)을 포함하는 제 1 반도체층(y= 0)인 동시에 제 3 반도체층이고, Si 층(17p)은 제 2 반도체층임과 동시에 제 3 반도체층보다 밴드 갭이 큰 제 4 반도체층으로서, 제 3 반도체층인 SiGe 층(15p)의 바로 위에 소스□드레인 콘택트 W 층(25p)이 형성되어 있다.

이상과 같이, 본 실시예로서는, A1소스□드레인 전극(21n, 21p)의 콘택트를 하는 기판측의 영역(소스□드레인 콘택트 W 층 (25n, 25p))을, 채널 형성을 위한 각 반도체층 중 밴드 갭이 작은 층의 바로 위에 설치하고 있기 때문에, 최상층의 반도체층인 Si 층(17n, 17p)의 바로 위에 콘택트를 설치하는 것보다 콘택트 저항이 작아지게 되어, 소자의 저소비 전력과 고속동작이 가능하게 된다.

특히, SiGe 층(15n, 15p)에 접촉하도록 텅스텐(W)으로 되는 소스□드레인 콘택트 W 층(25n, 25p)을 설치하고 있기 때문에, 매우 낮은 콘택트 저항을 얻을 수 있다.

즉, 본 실시예에서는 상기 제 1 실시예의 효과를 발휘하면서 콘택트 저항의 저감을 도모할 수 있다.

(제 6 실시예)

GF Exhibit 1124 - 2021/2704

도 14는, 도 8에 나타내는 구조에 저저항의 콘택트 금속층을 형성한 제 6 실시예에 의한 HCMOS 장치의 단면도이다.

도 14에 도시하는 바와 같이, 본 실시예에 의한 HCMOS 장치에 있어서는, 양자 우물 영역으로 되는 SiGe 층(36n, 36p) 위에, 소스□드레인 콘택트 W 층(45n, 45p)이 형성되어 있다.

본 실시예에 의한 발명의 특징은, 상기 제 3 실시예의 특징에 덧붙여, 상기 제 4 실시예와 같이, $Si_{1-x-y}Ge_xC_y$층$(0\leq x\leq 1, 0\leq y\leq 1)$을 포함하는 제 1 반도체층과, 상기 제 1 반도체층과는 다른 밴드 갭을 갖는 제 2 반도체층과, 상기 제 1, 제 2 반도체층 사이의 경계면 부근의 영역에 형성된 캐리어 축적층을 갖는 채널영역과, 제 3 반도체층과, 이 제 3 반도체층보다 큰 밴드 갭을 갖는 제 4 반도체층을 갖는 소스□드레인 영역과, 상기 제 3 반도체층의 바로 위에 형성된 저저항의 도체막으로 이루어지는 소스□드레인 콘택트층을 구비하고 있는 점이다.

그리고, 본 실시예의 NMOS 트랜지스터에 있어서는, 양자 우물 영역인 SiGeC 층(34n)은 $Si_{1-x-y}Ge_xC_y$층$(0\leq x\leq 1, 0\leq y\leq 1)$을 포함하는 제 1 반도체층으로, 제 1 Si 층(33n)은 제 2 반도체층이고, 양자 우물 영역인 SiGe 층(36n)은 제 3 반도체층이며, 제 3 Si 층(37n)은 SiGe 층(36n)보다 밴드 갭이 큰 제 4 반도체층으로서, 제 3 반도체층인 SiGe 층(36n)의 바로 위에 소스□드레인 콘택트 W 층(45n)이 형성되어 있다.

한편, 본 실시예의 PMOS 트랜지스터에 있어서는, SiGe 층(36p)은 $Si_{1-x-y}Ge_xC_y$층$(0\leq x\leq 1, 0\leq y\leq 1)$을 포함하는 제 1 반도체층(y= 0)인 동시에 제 3 반도체층이고, 제 3 Si 층(37p)은 제 2 반도체층인 동시에 제 3 반도체층보다 밴드 갭이 큰 제 4 반도체층으로서, 제 3 반도체층인 SiGe 층(36p)의 바로 위에 소스□드레인 콘택트 W 층(45p)이 형성되어 있다.

이상과 같이, 본 실시예에서는 Al 소스□드레인 전극(41n, 41p)의 콘택트를 하는 기판측의 영역(소스□드레인 콘택트 W 층(45n, 45p)을 채널 형성을 위한 각 반도체층 중 밴드 갭이 작은 층의 바로 위에 설치하고 있기 때문에, 최상층의 반도체층인 Si 층(37n, 37p)의 바로 위에 콘택트를 설치하는 것보다 콘택트 저항이 작아지게 되어 장치의 저소비 전력과 고속동작이 가능하게 된다.

특히, SiGe 층(36n, 36p)에 접촉하도록 텅스텐(W)으로 되는 소스□드레인 콘택트 W 층(45n, 45p)을 설치하고 있기 때문에 매우 낮은 콘택트 저항을 얻을 수 있다.

즉, 본 실시예로서는, 상기 제 3 실시예의 효과를 발휘하면서 콘택트 저항의 저감을 도모할 수 있다.

(그 밖의 변형 실시예)

상기 제 1□제 6 실시예로서는, 게이트 전극의 밑으로 게이트 절연막을 설치한 MOS 형 전계 효과 트랜지스터에 대하여 설명하였지만, 본 발명은 이러한 실시예에 한정되는 것은 아니다. 특히, 최상층에 절연막이 있는 헤테로 M0S 구조가 아니라 헤테로 경계면을 이용하는 전계 효과 트랜지스터이면, 절연막을 이용하지 않는 쇼트키 접합을 이용하는 장치라도 실시 가능하고, 저항의 저감효과를 얻는 것이 가능하여, 장치의 저소비전력 및 고속동작에 유리하게 된다.

상기 제 1□제 6 실시예에서는, δ 도핑층을 형성하였지만, 본 발명은 이러한 실시예에 한정되는 것이 아니고, δ 도핑층을 설치하지 않더라도 본 발명의 효과를 발휘하는 것은 가능하다. 또한, δ 도핑층을 형성하는 경우에도 스페이스층은 반드시 필요한 것은 아니다.

상기 제 1, 제 2, 제 3, 제 5, 제 6 실시예에 있어서 SiGe 층에 대신하여 C층을 미량 첨가한 SiGeC 층을 설치하여도 된다.

GF Exhibit 1124 - 2022/2704

또, 상기 제 1, 제 2, 제 3, 제 5, 제 6 실시예에 있어서는, SiGeC 층과, SiGe 층의 상하관계를 반대로 하여도 되는 것으로 한다. 그 경우, 제 5,제 6 실시예에서는 소스□드레인 영역에서의 SiGeC 층 바로 위에 소스□드레인 콘택트 W 층을 형성하면 된다.

청구항 1□16에 의하면, 전계 효과 트랜지스터를 갖는 반도체 장치에 있어서, Si 층과 C의 조성비 y가 0.01□0.03인 $Si_{1-x-y}Ge_xC_y$층을 설치하고, $Si_{1-x-y}Ge_xC_y$층 내에 형성되는 캐리어 축적층을 채널로서 이용하도록 하였기 때문에, 동작속도가 크고 또한 신뢰성이 높은 전계 효과형 트랜지스터를 갖는 반도체 장치의 제공을 도모할 수 있다.

청구항 17□29에 의하면, 전계 효과형 트랜지스터를 갖는 반도체 장치에 있어서, 제 1 의 Si 층과 제 1 의 $Si_{1-x-y}Ge_xC_y$층 사이, 제 2 의 Si 층과 제 2 의 $Si_{1-x-y}Ge_xC_y$층 사이의 경계면에 생기는 밴드 불연속부를 이용하여 전자와 정공을 2차원적으로 폐쇄하는 축적층을 형성하고, 이 축적층을 채널로 하는 전계 효과 트랜지스터를 설치하였기 때문에, 캐리어의 폐쇄 효율이 높은 채널을 갖고 또한 동작 속도가 크고 또한 신뢰성이 높은 n-채널 및 p-채널 전계 효과 트랜지스터를 구비한 HCMOS 장치로서 기능하는 반도체 장치의 제공을 도모할 수 있다.

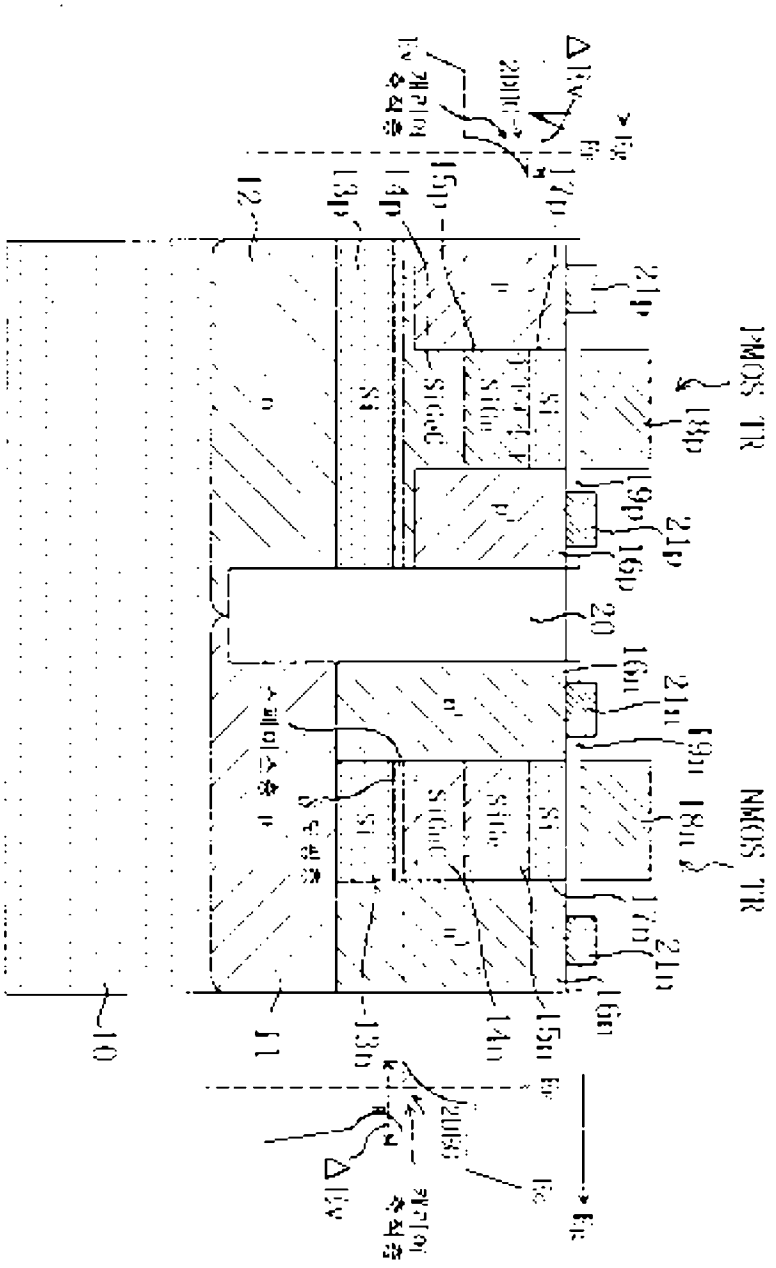
이 반도체 장치의 구조는, 청구항 33의 반도체 장치의 제조방법에 의해 용이하게 실현할 수가 있다.

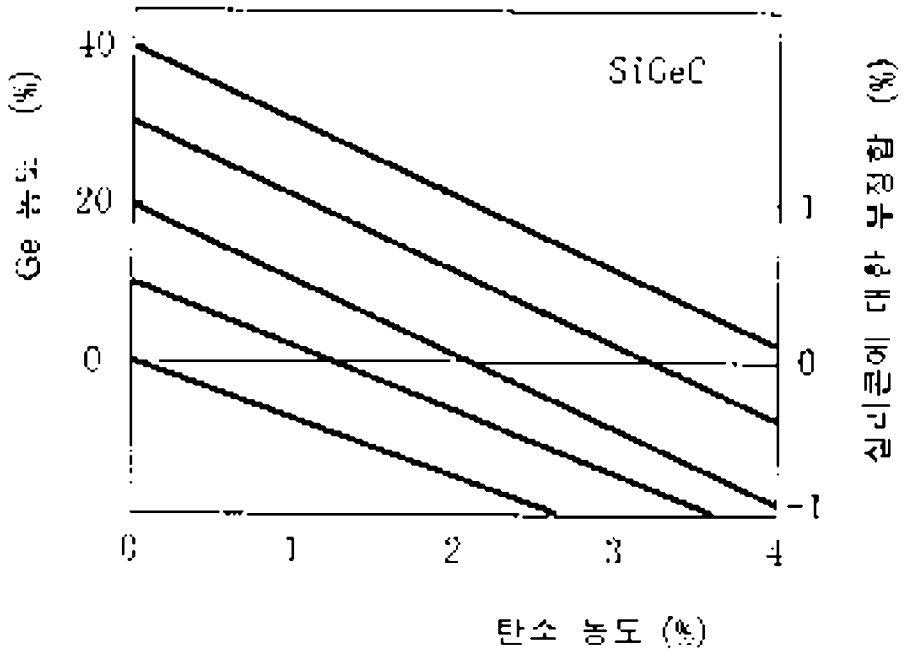
청구항 30□32에 의하면, $Si_{1-x-y}Ge_xC_y$층을 포함하는 제 1 반도체층과 제 2 반도체층 사이에 채널로 되는 밴드 불연속부를 형성시킨 전계 효과 트랜지스터를 갖는 반도체 장치에 있어서, 소스□드레인 영역을 제 3 반도체층 및 제 3 반도체층보다 밴드 갭이 큰 제 4 반도체층에 의해 구성되고, 이 제 3 반도체층의 바로 위에 저저항의 도체막으로 이루어지는 소스□드레인 콘택트층을 설치하였기 때문에, 헤테로 접합을 이용한 동작 속도가 높으며 또한 소스□드레인 콘택트 저항이 작은 반도체 장치의 제공을 도모할 수 있다.

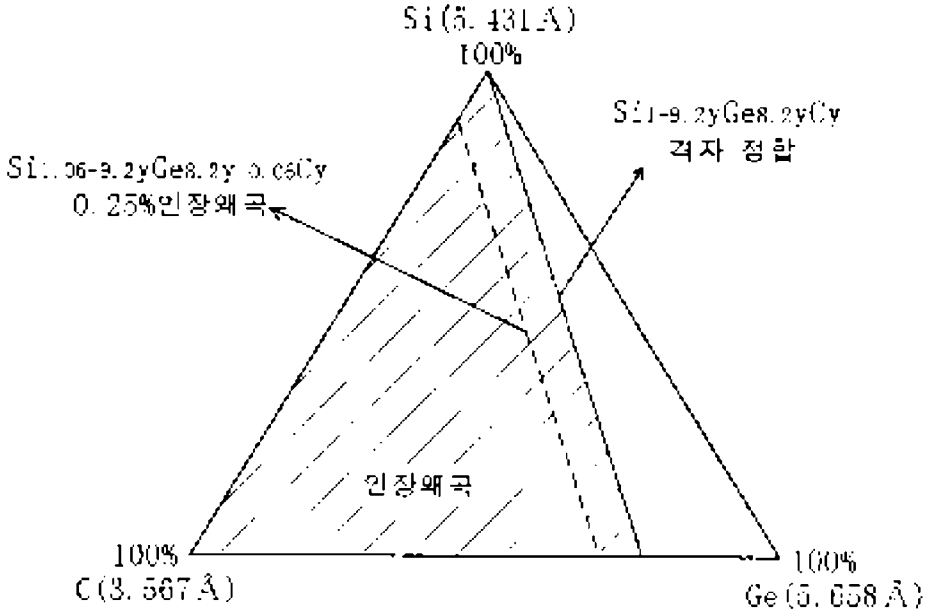
이 반도체 장치의 구조는, 청구항 34□37의 반도체 장치의 제조방법에 의해 용이하게 실현할 수가 있다.

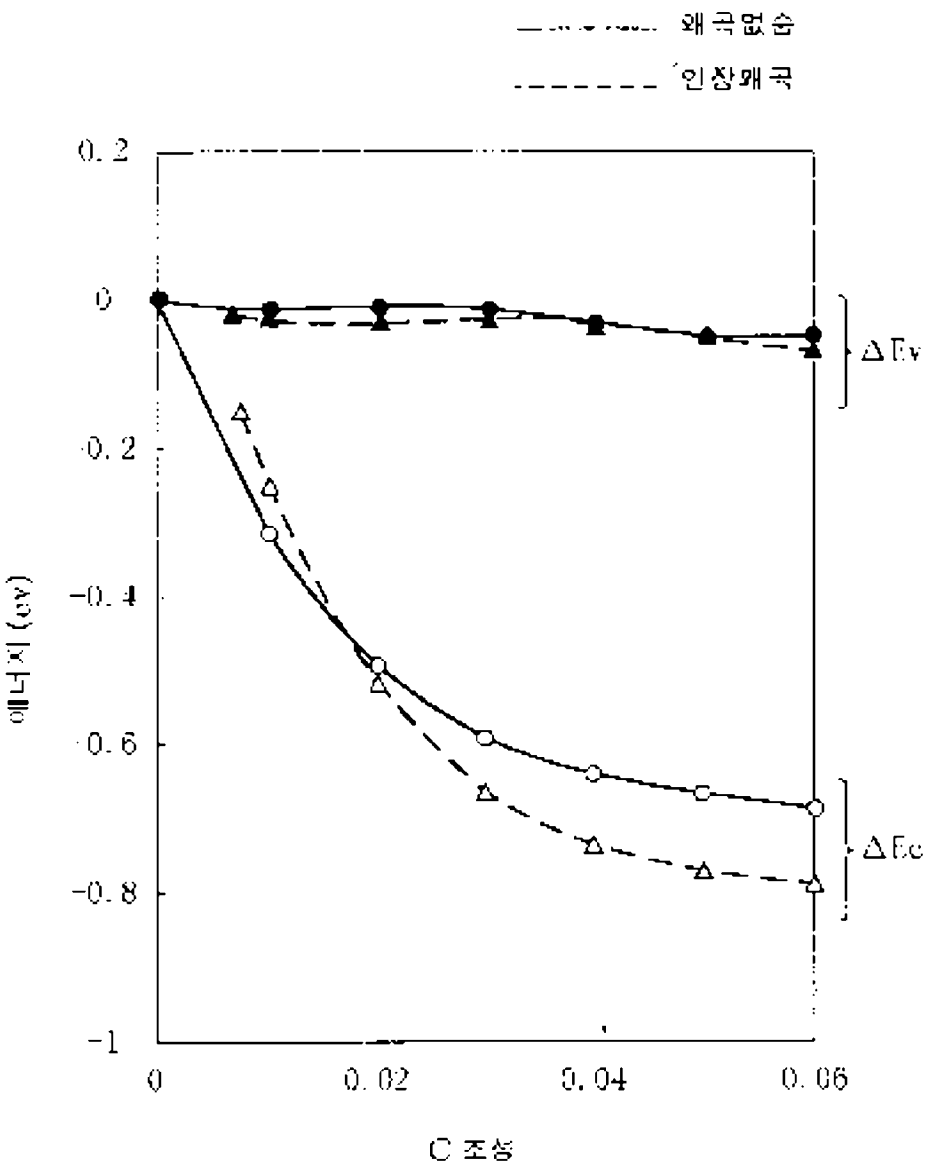
본 발명의 바람직한 실시예들은 예시의 목적을 위해 개시된 것이며, 당업자라면 첨부된 특허청구범위에 개시된 본 발명의 사상과 범위를 통해 각종 수정, 변경, 대체 및 부가가 가능할 것이다.

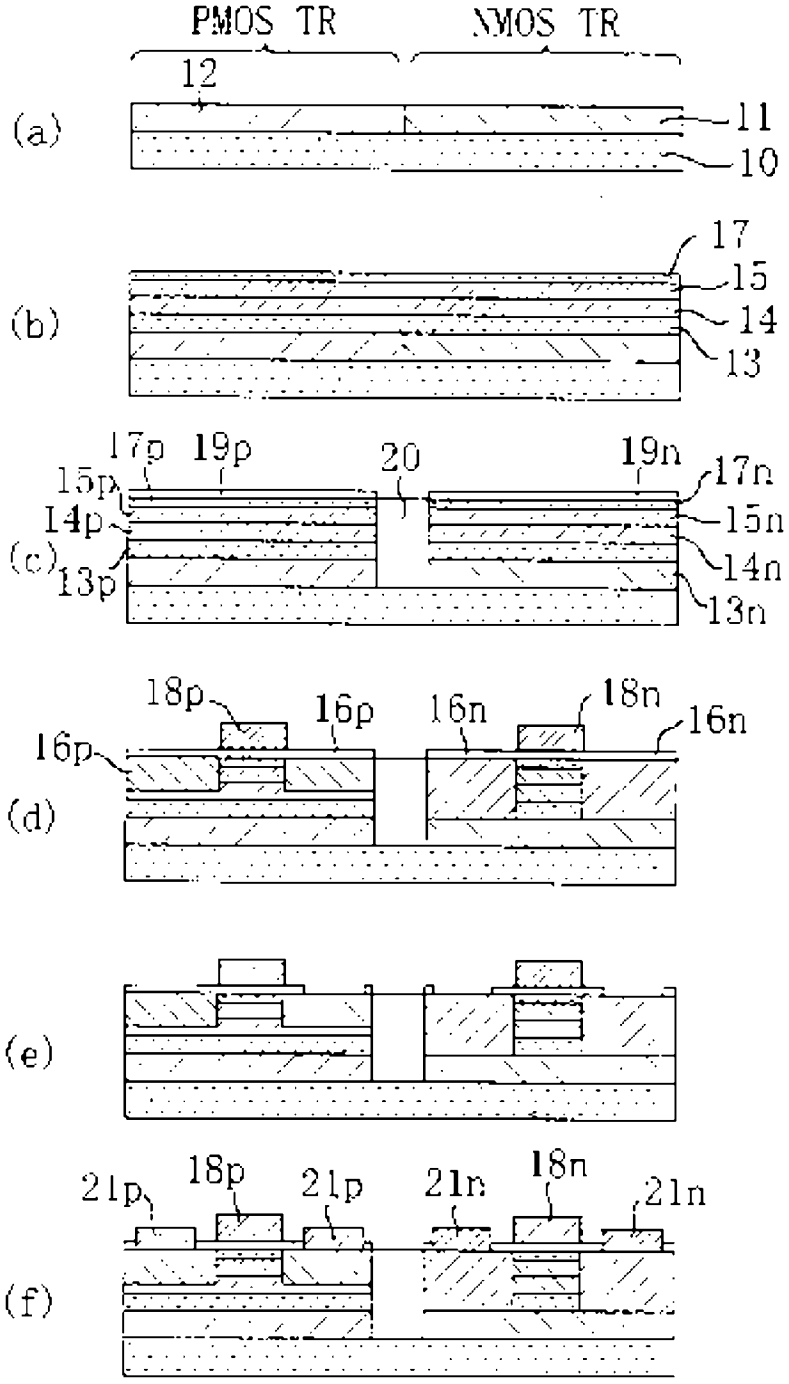
GF Exhibit 1124 - 2023/2704

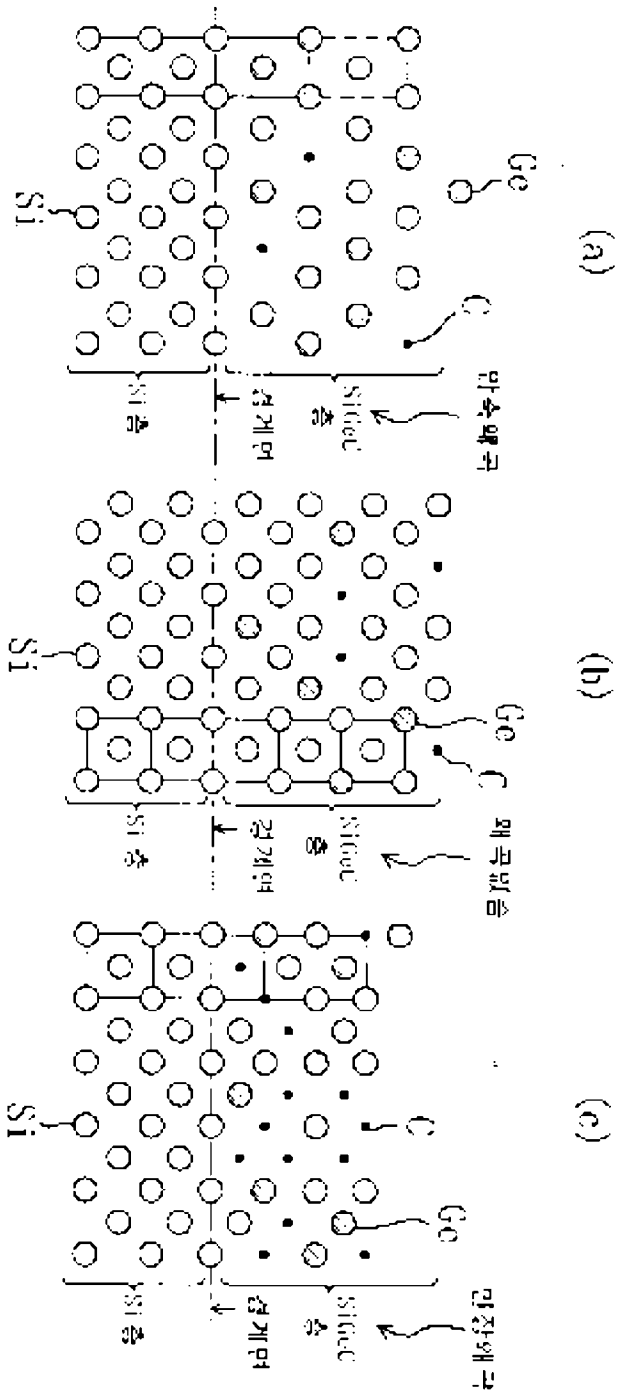

PMOS TR
NMOS TR
Si
SiGeC
n+
p+
n
p
10
11
12
20
캐리어 주입층
캐리어 추출층

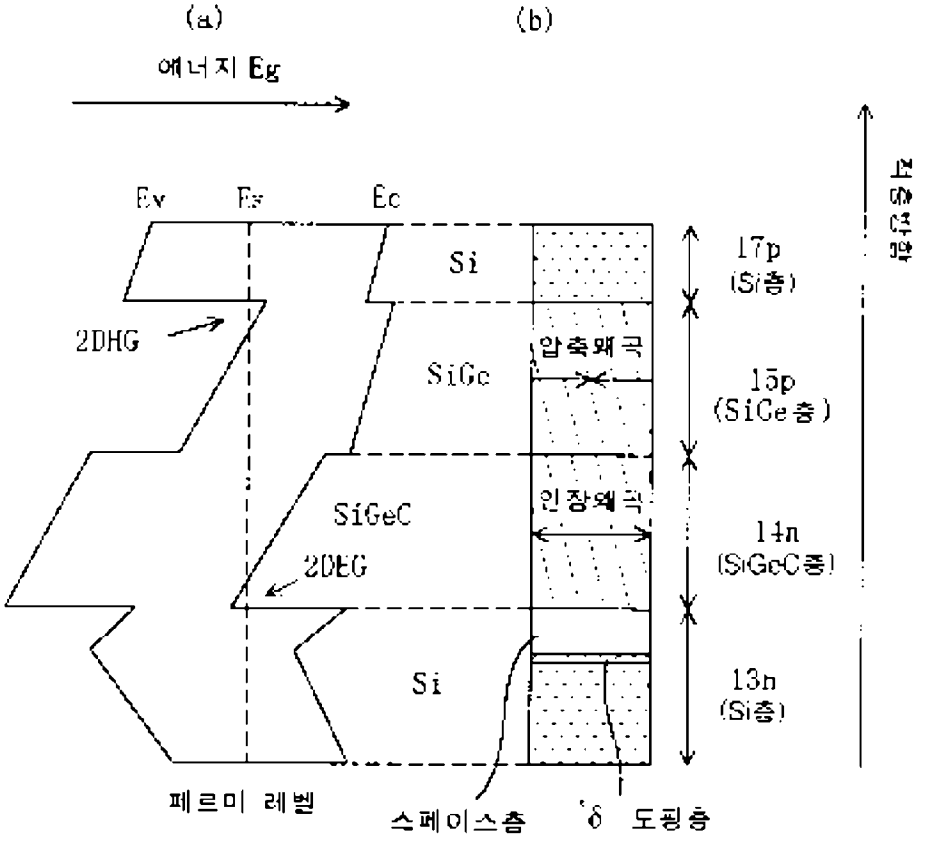

SiGeC
Ge 농도 (%)
40
20
0
1
0
-1
0
1
2
3
4
탄소 농도 (%)
실리콘에 대한 부정합 (%)

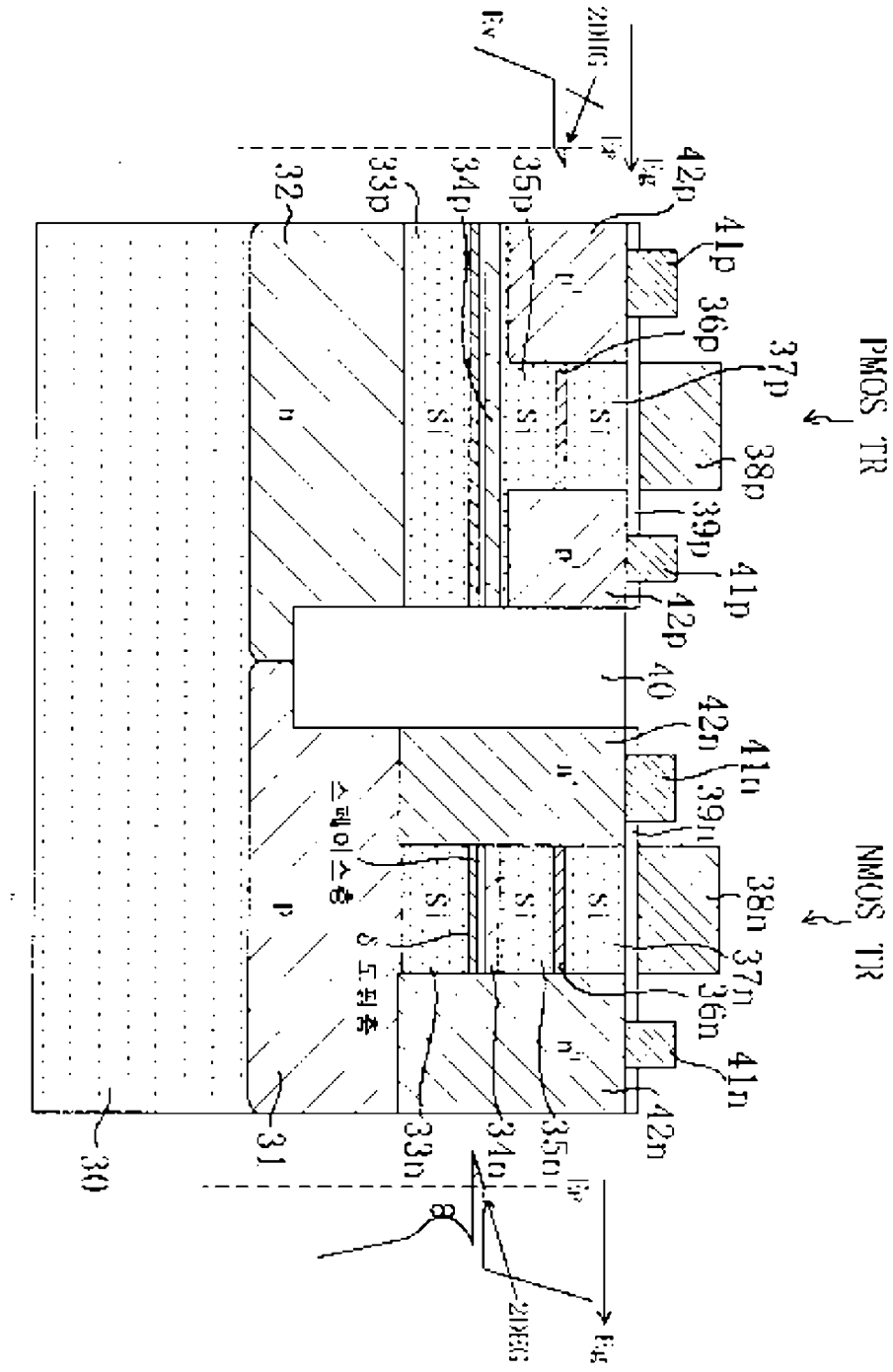

Si(5.431Å)
100%
Si1-a-2yGeaCy
격자 정합
Si1-a-2yGeaCy
0.25%인장왜곡
인장왜곡
100%
C(3.567Å)
100%
Ge(5.658Å)

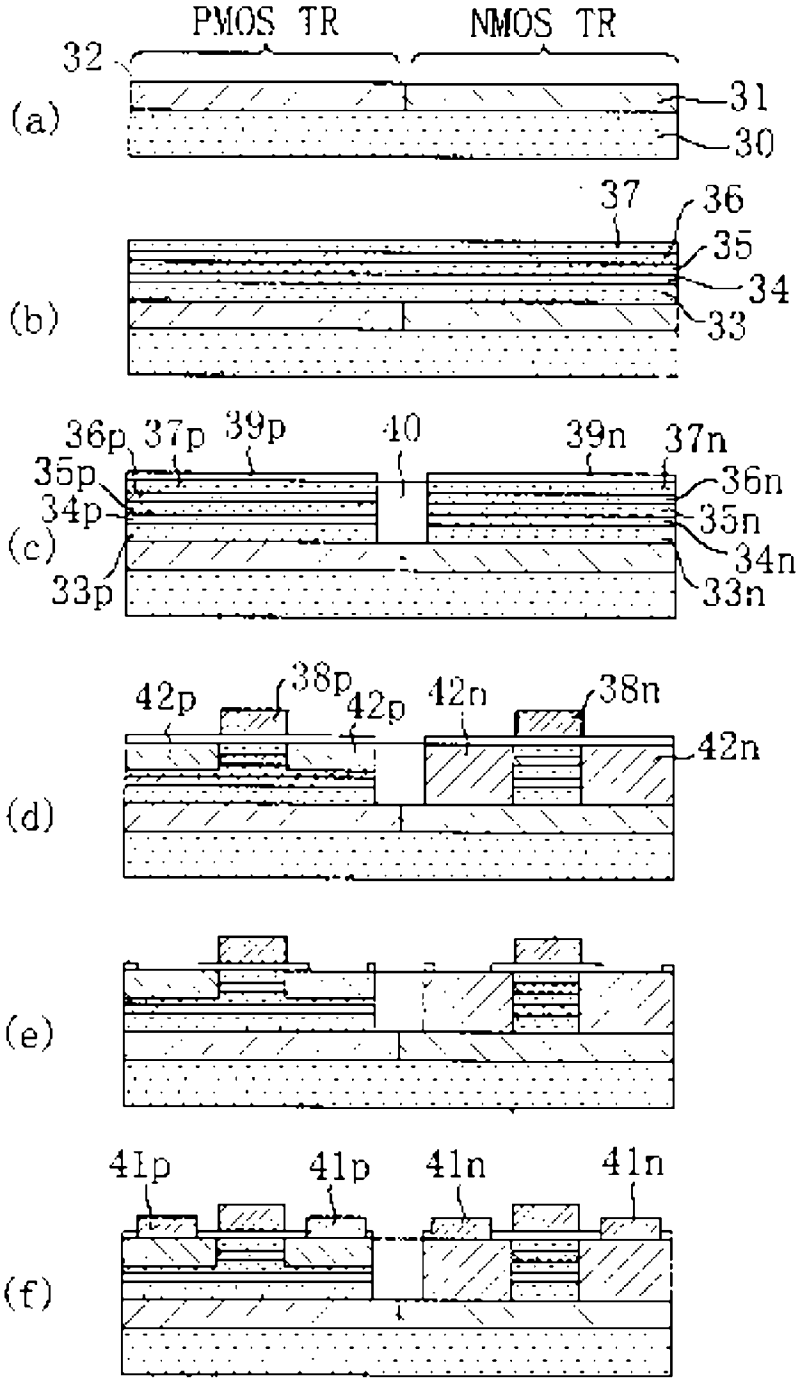

왜곡없음
인장왜곡
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
에너지 (eV)
ΔEv
ΔEc
0
0.02
0.04
0.06
C 조성

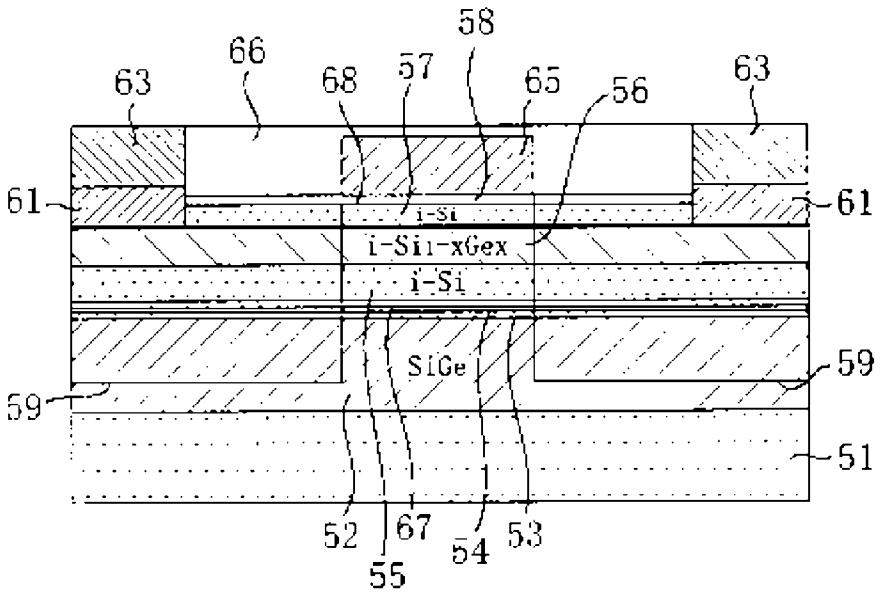

PMOS TR
NMOS TR
12
(a)
11
10
(b)
17
15
14
13
17p
19p
20
19n
17n
15p
15n
14p
(c)
14n
13p
13n
18p
16p
16n
18n
16n
16p
(d)
(e)
21p
18p
21p
21n
18n
21n
(f)

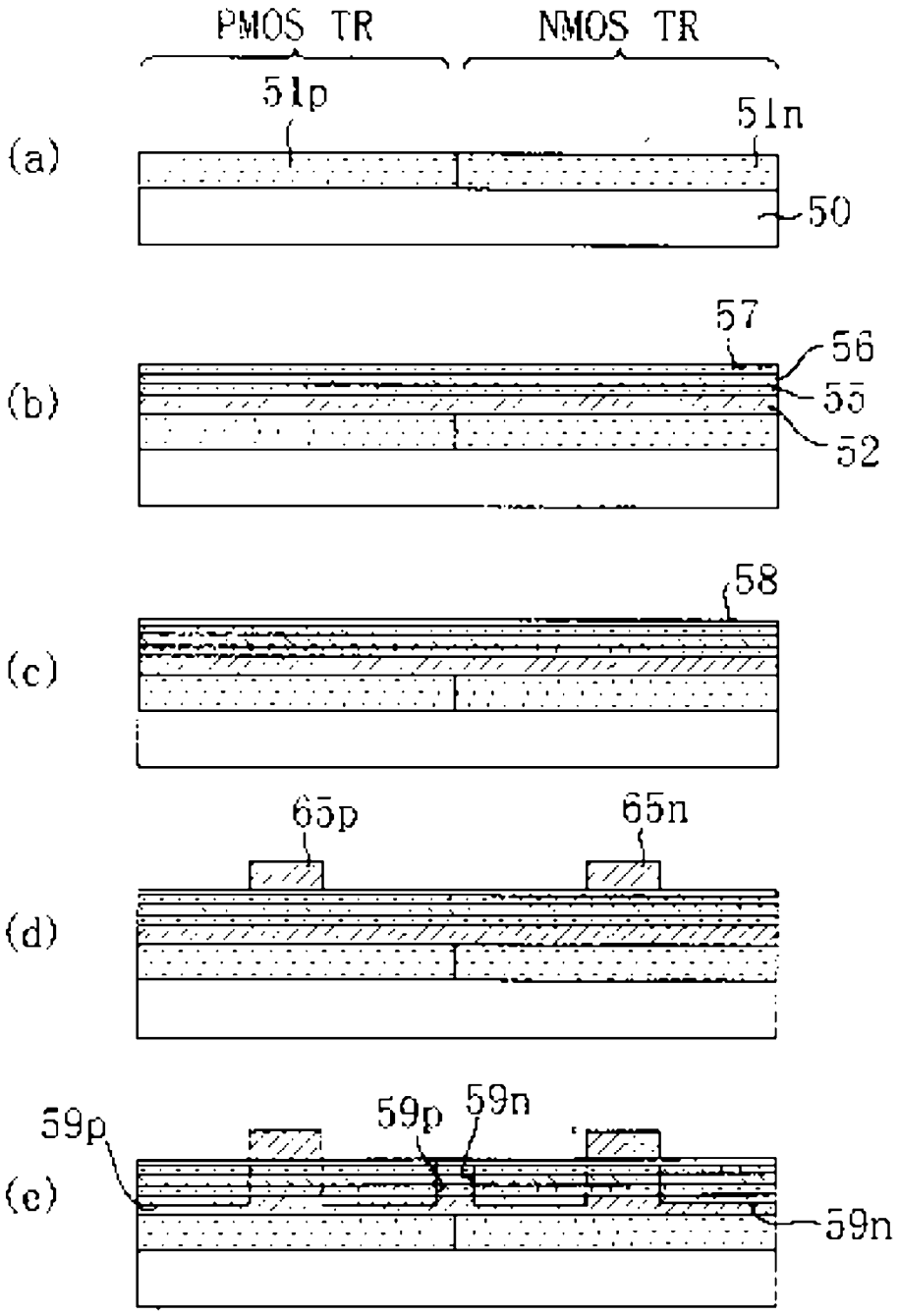

(a)
Ge
Si
C
Si층
SiGeC층
격자면
마스크층
(b)
Si
Ge
C
Si층
격자면
SiGeC층
매몰층
(c)
Si
C
Ge
Si층
격자면
SiGeC층
단결정층

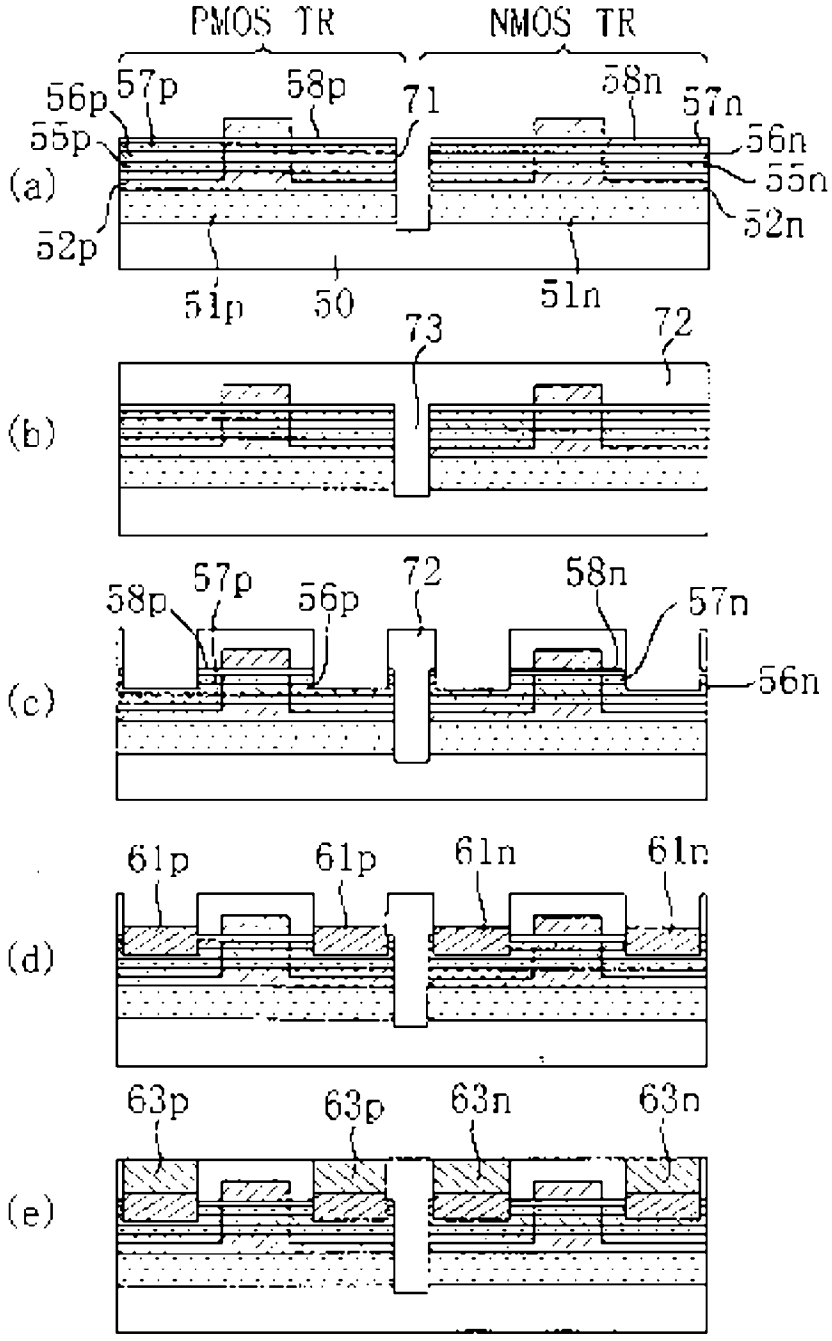

(a)
(b)
에너지 Eg
Ev
Ef
Ec
Si
SiGe
SiGeC
Si
2DHG
2DEG
압축왜곡
인장왜곡
17p
(Si층)
15p
(SiGe층)
14n
(SiGeC층)
13n
(Si층)
성장방향
페르미 레벨
스페이스층
δ 도핑층

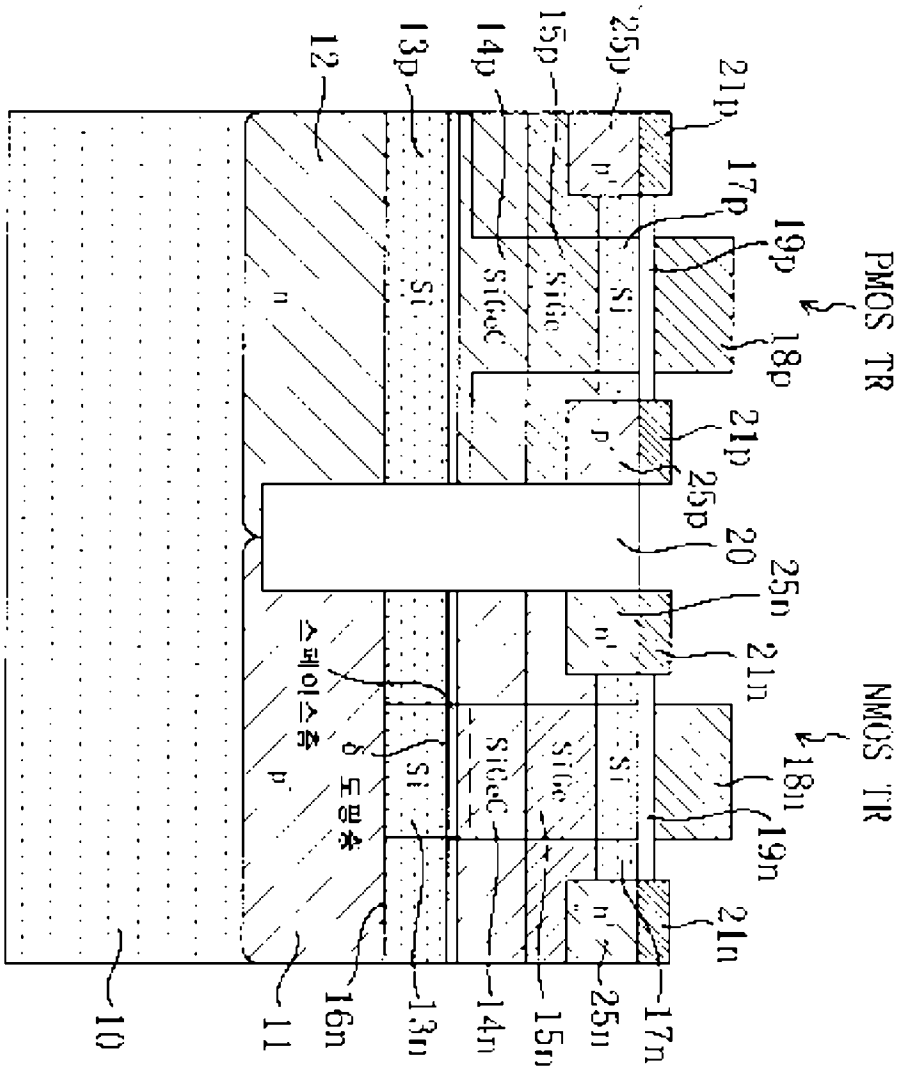

PMOS TR
NMOS TR
스페이스층
δ 도핑층
Si
n
p
n+
p+
30
31
32
33p
34p
35p
36p
37p
38p
39p
40
41p
42p
33n
34n
35n
36n
37n
38n
39n
41n
42n

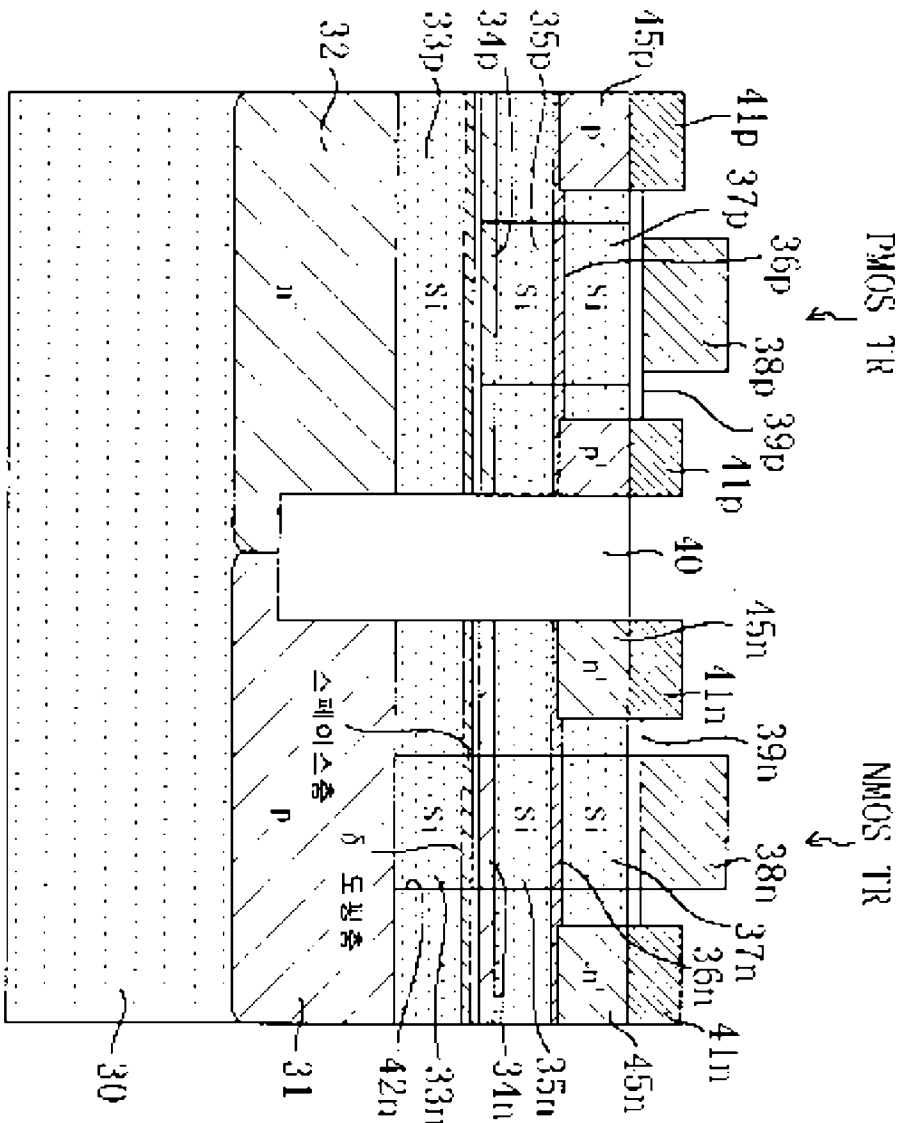

PMOS TR
NMOS TR
32
(a)
31
30
37
36
35
34
(b)
33
36p
37p
39p
40
39n
37n
35p
34p
(c)
33p
36n
35n
34n
33n
42p
38p
42p
42n
38n
42n
(d)
(e)
41p
41p
41n
41n
(f)

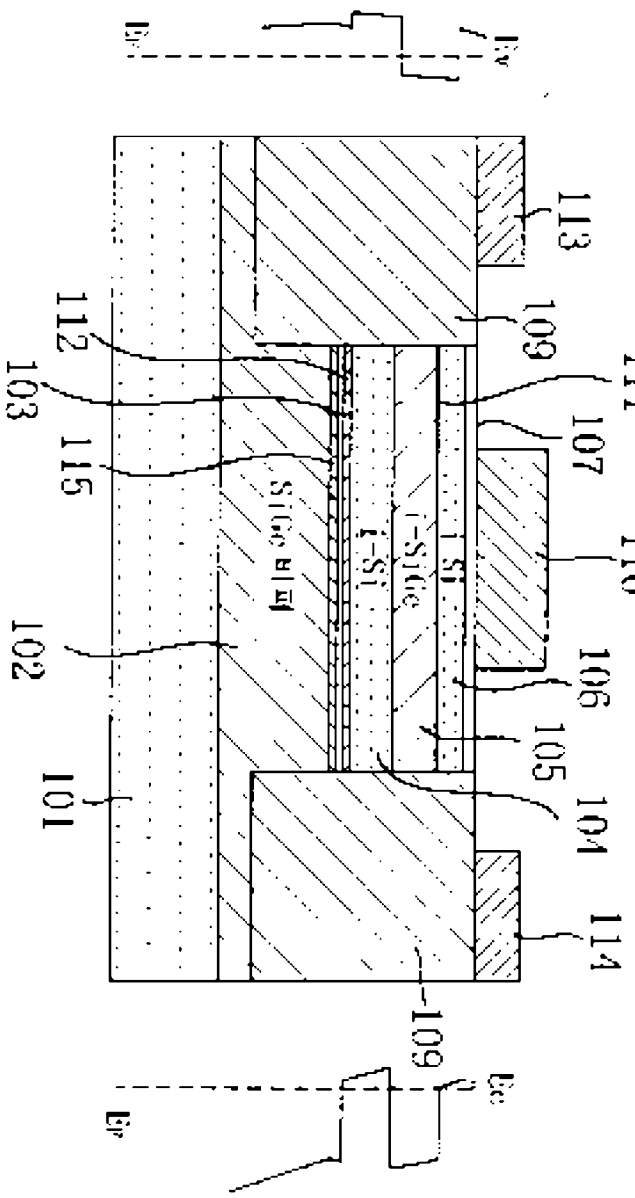

58
66
63
68
57
65
56
63
61
61
i-Si
i-Si1-xGex
i-Si
SiGe
59
59
51
52
67
54
53
55

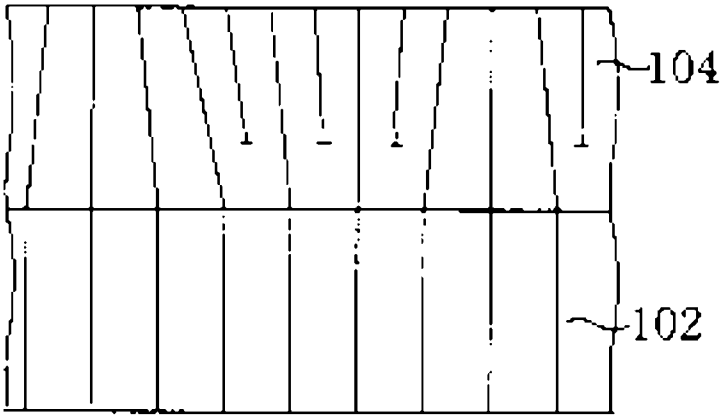

PMOS TR
NMOS TR
51p
51n
(a)
50
57
56
(b)
55
52
58
(c)
65p
65n
(d)
59p
59p
59n
(e)
59n


PMOS TR
NMOS TR
56p
57p
58p
71
58n
57n
55p
56n
(a)
55n
52p
52n
51p
50
51n
73
72
(b)
58p
57p
56p
72
58n
57n
(c)
56n
61p
61p
61n
61n
(d)
63p
63p
63n
63n
(e)


PMOS TR
NMOS TR
21p
17p
19p
18p
25p
15p
14p
13p
12
21p
25p
20
25n
21n
18n
19n
21n
17n
25n
15n
14n
13n
16n
11
10
Si
SiGe
SiGeC
p
n
스페이스층
δ 도핑층


PMOS TR
NMOS TR
45p
41p
37p
36p
38p
39p
41p
35p
34p
33p
32
40
45n
41n
39n
38n
37n
36n
41n
45n
35n
34n
33n
42n
31
30
스페이스층
δ 도핑층
Si
n
p
n'
p'


113
112
109
111
103
107
115
110
106
102
105
101
104
114
109


104
102

Unexamined Patent Publication(A)

Bibliographic Data

Int.Cl.	H01L 29/778 | H01L 29/10 | H01L 29/161 | H01L 29/66
Published Date	20050908
Registration No.	1004955430000
Registration Date	20050607
Application No.	1019970047286
Application Date	19970913
Unexamined Publication No.	1019980024649
Unexamined Publication Date	19980706
Priority Claims	특원평8-244395 | 19960917 | JP 특원평8-269578 | 19961011 | JP 특원평8-314551 | 19961126 | JP
Requested Date of Examination	20020425
Agent.	Kim Young Chul
Inventor	NoJaWaGaSseuYa | GuMaBuChiYaSeuHiTo | KUBO,Minoru | SeuJeuKiMaSaKaSseu | UENOYAMA,Takeshi
Applicant	PANASONIC CORPORATION
Rightholder	MATSUSHITA ELECTRIC INDUSTRIAL CO.. LTD.

발명의 명칭

반도체장치및그제조방법

Title of Invention

Semiconductor device and method for producing the same.

요약

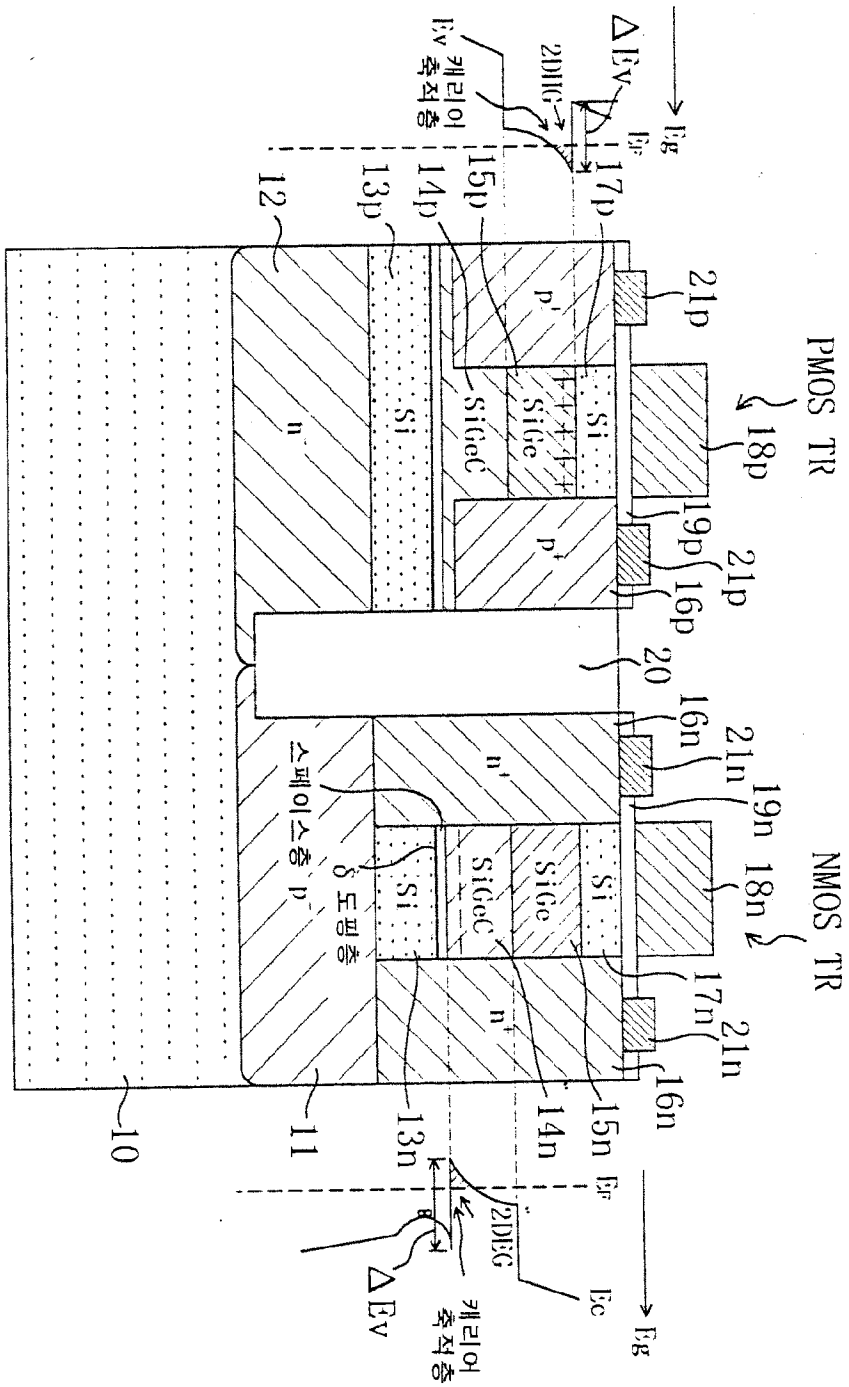
캐리어의 이동도가 높고, 결정 결함이 적은 채널을 갖는 전계 효과 트랜지스터를 구비한 반도체 장치를 제공하기 위하여, Si 기판(10)상의 NMOS 트랜지스터에 있어서, Si 층(13n), SiGeC 층(14n)이 형성되어 있다. 이 SiGeC 층(14n)과 Si 층(13n)의 헤테로 경계면에 존재하는 전도대의 불연속부를 이용한 캐리어 축적층이 형성되어 있고, 이 캐리어 축적층을 채널로서 전자가 주행하며, SiGeC 층(14n)은 실리콘에 비교해서 전자의 이동도가 크고, NMOS 트랜지스터의 동작속도도 커지며, PM0S 트랜지스터의 정공이 주행하는 채널은, SiGe 층(15p)과 Si 층(17p)의 경계면에 생기는 가전자대의 불연속부를 이용하여 형성되어 있으므로, SiGe 층도 Si 층에 비교해서 정공의 이동도가 크고, 상기 PMOS 트랜지스터의 동작속도도 커지게 된다.

Abstract

The mobility of the carrier is high and in order that the semiconductor device equipped with the field effect transistor having the channel in which the crystal defect is less is provided the Si layer (13n), and the SiGeC layer (14n) are formed as to the NMOS transistor on the Si substrate (10). The carrier accumulation layer using the discontinuity of the condition band existing in the hetero boundary face of the Si layer (13n) and this SiGeC layer (14n) is formed and the electron travels this carrier accumulation layer as the channel and the SiGeC layer (14n) compares in the silicone and the mobility of the electron is large and the working speed of the NMOS transistor is enlarged and the hole of the PM0S transistor as to the driving channel, is formed using the discontinuity of the valence band generated in the boundary face of the Si layer (17p) and SiGe layer (15p). Therefore the SiGe layer compares in the Si layer and the mobility of the hole is large and the working speed of the PMOS transistor is enlarged.

GF Exhibit 1124 - 2039/2704

대표도면(Representative drawing)



청구의 범위

청구 1항:

반도체 기판의 일부에 형성되어 게이트 전극과 소스#183#드레인 영역 및 해당 소스#183#드레인 영역 사이의 채널 영역을 갖는 전계 효과 트랜지스터를 구비하고 있는 반도체 장치에 있어서,상기 채널영역에는Si 층과, 상기 Si 층에 근접하여 형성되고 C의 조성비 y가 0.01~0.03인 Si1-x-yGexCy 층 (0#88

Scope of Claims

Claim 1:

The semiconductor device in which *** Si layer, and Si 1-x- y Ge x C y layers (0≤x≤1, 0y≤1) which come close to the Si layer and which are formed and in which the composition ratio y of C is 0.01~0.03 are installed as t o the semiconductor device including the field effect tr

GF Exhibit 1124 - 2040/2704

04#x#8804#1, 0y#8804#1)이 설치되고, Si1-x-yGex Cy 층 내에서의 상기 Si 층에 근접한 영역에는 캐리어 축적층이 형성되어 있는 것을 특징으로 하는 반도체 장치.

ansistor which is formed in the part of the semiconduct or substrate and has the channel region between the g ate electrode and the source · drain region and corresp onding source · drain region ; and the carrier accumula tion layer is formed in the domain near to the Si layer within the Si 1-x- y Ge x C y layer.

청구 2항:

Claim 2:

제 1 항에 있어서, 상기 Si1-x-yGexCy 층의 각 원소의 조성비는, 상기 Si1-x-yGexCy 층과 상기 Si 층 이 격자 정합하는 조성비로 조정되는 것을 특징으로 하는 반도체 장치.

As for claim 1, the semiconductor device in which the composition ratio of each element of the Si 1-x- y Ge x C y layer is adjusted to the Si 1-x- y Ge x C y layer an d the composition ratio which the Si layer this lattice-matches.

청구 3항:

Claim 3:

제 1 항에 있어서, 상기 Si1-x-yGexCy 층은 상기 Si 층보다도 작은 격자 정수를 갖고, 또한 격자 완화를 발생하지 않는 막 두께를 갖는 것을 특징으로 하는 반도체 장치.

As for claim 1, the semiconductor device wherein the Si 1-x- y Ge x C y layer has the film thickness that is n ot generated the lattice mismatch distortion it has the lattice constant smaller than the Si layer.

청구 4항:

Claim 4:

제 1 항 내지 제 3 항에 있어서, 상기 반도체 기판상에 형성되어 단일 조성의 반도체층을 채널 영역으로 하는 M0S 트랜지스터를 추가로 구비하는 것을 특징으로 하는 반도체 장치.

As for claim 1 through 3, the semiconductor device for additionally including the MOS transistor which is forme d in the substrate and has the semiconductor layer of t he single composition as the channel region.

청구 5항:

Claim 5:

제 1 항 내지 제 3 항 중 어느 한 항에 있어서,상기 캐리어 축적층에 축적되는 캐리어는 부의 캐리어인 것을 특징으로 하는 반도체 장치.

As for any one of claim 1 through 3, the semiconductor device in which the carrier accumulated in the carrier a ccumulation layer is the carrier of the part.

청구 6항:

Claim 6:

제 4 항에 있어서,상기 캐리어 축적층에 축적되는 캐리어는 부의 캐리어인 것을 특징으로 하는 반도체 장치.

As for claim 4, the semiconductor device in which the carrier accumulated in the carrier accumulation layer is the carrier of the part.

청구 7항:

Claim 7:

제 1 항 내지 제 3 항 및 제 6 항 중 어느 한 항에 있어서, 상기 Si 층 내의 상기 Si1-x-yGexCy 층에 근접한 영역에는 상기 캐리어 축적층에 캐리어를 공급하기 위한 캐리어 공급층을 추가로 설치하는 것을 특징으로 하는 반도체 장치.

As for any one of claim 1 to claim 3 and claim 6, the semiconductor device for additionally setting up the ca rrier supply layer for supplying the carrier to the carrier accumulation layer in the domain near to the Si 1-x- y Ge x C y layer within the Si layer.

청구 8항:

Claim 8:

제 4 항에 있어서, 상기 Si 층 내의 상기 Si1-x-yGexCy 층에 근접한 영역에는 상기 캐리어 축적층에 캐리어를 공급하기 위한 캐리어 공급층을 추가로 설치하는 것을 특징으로 하는 반도체 장치.

As for claim 4, the semiconductor device for additionally setting up the carrier supply layer for suppl ying the carrier to the carrier accumulation layer in the domain near to the Si 1-x- y Ge x C y layer within the Si layer.

청구 9항:

Claim 9:

제 5 항에 있어서, 상기 Si 층 내의 상기 Si1-x-yGexCy 층에 근접한 영역에는 상기 캐리어 축적층에 캐리어를 공급하기 위한 캐리어 공급층을 추가로 설치하는 것을 특징으로 하는 반도체 장치.

As for claim 5, the semiconductor device for additionally setting up the carrier supply layer for suppl ying the carrier to the carrier accumulation layer in the domain near to the Si 1-x- y Ge x C y layer within the Si layer.

GF Exhibit 1124 - 2041/2704

청구 10항:

제 1 항에 있어서,상기 캐리어 축적층에 축적되는 캐리어는 부의 캐리어이고,상기 반도체 기판의 다른 부분에 형성되어 게이트 전극과, 소스#183#드레인 영역과 이 소스#183#드레인 영역 사이의 채널영역을 갖는 또 하나의 전계 효과 트랜지스터를 구비하며,상기 또 하나의 전계 효과 트랜지스터의 채널영역은, 제 2 Si 층과,상기 제 2 Si 층에 근접하여 형성된 SiGe 층을 구비하고,상기 SiGe 내에서의 상기 제 2 Si 층에 근접한 영역에는, 정의 캐리어를 축적하기 위하여 제 2 캐리어 축적층이 형성되는 것을 특징으로 하는 반도체 장치.

Claim 10:

As for claim 1, the semiconductor device wherein the carrier accumulated in the carrier accumulation layer th e second carrier the accumulation layer is formed in ord er to accumulate the definition carrier in the domain th at includes ; and comes close to the second Si layer wi thin the SiGe the formed SiGe layer it includes ; and th e channel region of one field effect transistor comes cl ose to the second Si layer, and the second Si layer wit h the above one field effect transistor which is the carr ier of the part ; and it is formed in the dissimilar part of the semiconductor substrate and has the gate electrod e, and the channel region between this source · drain r egion and the source · drain region.

청구 11항:

제 1 항에 있어서,상기 Si1-x-yGexCy층은 양자 우물 영역으로 되어있는 것을 특징으로 하는 반도체 장치.

Claim 11:

As for claim 1, the semiconductor device in which the Si 1-x- y Ge x C y layer is to the quantum-well gain reg ion.

청구 12항:

제 10 항에 있어서,상기 SiGe 층은 양자 우물 영역으로 되어있는 것을 특징으로 하는 반도체 장치.

Claim 12:

As for claim 10, the semiconductor device in which the SiGe layer is to the quantum-well gain region.

청구 13항:

제 1 항 내지 제 3 항, 제 6 항 및 제 8 항 내지 제 12 한 중 어느 한 항에 있어서,상기 소스#183#드레인 영역은 제 1 반도체층과, 이 1 반도체층보다 큰 밴드 갭을 갖는 제 2 반도체층을 갖고,상기 제 1 반도체층의 바로 위에 형성된 저저항의 도체막으로 된 소스#183#드레인 콘택트층을 추가로 구비하는 것을 특징으로 하는 반도체 장치.

Claim 13:

The semiconductor device it has the second semiconductor layer in which the source · drain region has the first semiconductor layer, and the band gap wh ich is greater than this 1 semiconductor layer to that a s to claim 1 to claim 3, and claim 6 and claim 8 to the t welfth one middle any one claim ; and for additionally in cluding the source · drain contact layer consisting of t he conductor film of the low resistance formed in the fi rst semiconductor layer, immediately, the upper part.

청구 14항:

제 4 항에 있어서,상기 소스#183#드레인 영역은 제 1 반도체층과, 이 1 반도체층보다 큰 밴드 갭을 갖는 제 2 반도체층을 갖고,상기 제 1 반도체층의 바로 위에 형성된 저저항의 도체막으로 된 소스#183#드레인 콘택트층을 추가로 구비하는 것을 특징으로 하는 반도체 장치.

Claim 14:

As for claim 4, the semiconductor device wherein the source · drain region includes the additionally the sourc e · drain contact layer which has the second semicond uctor layer ; and consists of the conductor film of the l ow resistance formed in the first semiconductor layer, i mmediately, the upper part that has the first semicond uctor layer, and the band gap which is greater than thi s 1 semiconductor layer.

청구 15항:

제 5 항에 있어서,상기 소스#183#드레인 영역은 제 1 반도체층과, 이 1 반도체층보다 큰 밴드 갭을 갖는 제 2 반도체층을 갖고,상기 제 1 반도체층의 바로 위에 형성된 저저항의 도체막으로 된 소스#183#드레인 콘택트층을 추가로 구비하는 것을 특징으로 하는 반도체 장치.

Claim 15:

As for claim 5, the semiconductor device wherein the source · drain region includes the additionally the sourc e · drain contact layer which has the second semicond uctor layer ; and consists of the conductor film of the l ow resistance formed in the first semiconductor layer, i mmediately, the upper part that has the first semicond uctor layer, and the band gap which is greater than thi s 1 semiconductor layer.

청구 16항:

Claim 16:

GF Exhibit 1124 - 2042/2704

제 7 항에 있어서,상기 소스#183#드레인 영역은 제 1 반도체층과, 이 1 반도체층보다 큰 밴드 갭을 갖는 제 2 반도체층을 갖고,상기 제 1 반도체층의 바로 위에 형성된 저저항의 도체막으로 된 소스#183#드레인 콘택트층을 추가로 구비하는 것을 특징으로 하는 반도체 장치.

As for claim 7, the semiconductor device wherein the source · drain region includes the additionally the source · drain contact layer which has the second semiconductor layer ; and consists of the conductor film of the low resistance formed in the first semiconductor layer, immediately, the upper part that has the first semiconductor layer, and the band gap which is greater than this 1 semiconductor layer.

청구 17항:

Claim 17:

반도체 기판의 일부에 형성되어 게이트 전극과, 소스#183#드레인 영역과 이 소스#183#드레인 영역 사이의 채널영역을 갖는 전계 효과 트랜지스터를 구비하고,상기 채널영역에는, 제 1 의 Si 층과,상기 Si 층에 인접하여 형성된 제 1 의 Si1-x-yGexCy층(0#8804#x#8804#1, Oy#8804#1)과,제 2 의 Si 층과,상기 제 2 의 Si 층에 인접하여 형성되고 상기 제 1 의 Si1-x-yGexCy층과는 다른 밴드 갭을 갖는 제 2 의 Si1-x-yGexCy층(0#8804#x#8804#1,0#8804#y#8804#1)이 설치되며, 상기 제 1 Si1-x-yGexCy층 내에서의 상기 제 1 의 Si 층에 근접한 영역과, 상기 제 2 의 Si1-x-yGexCy층 안에서의 상기 제 2 의 Si 층에 근접한 영역과는 서로 다른 도전형의 캐리어를 폐쇄하기 위한 제 1 및 제 2 캐리어 축적층이 각각 형성되는 것을 특징으로 하는 반도체 장치.

The semiconductor device in which it is formed in the part of the semiconductor substrate and it includes gate electrode, and the field effect transistor having the channel region between this source · drain region and the source · drain region ; the first si layer, and the first Si 1-x- y Ge x C y layer (0≤x≤1, Oy≤1), formed adjacently in the Si layer and the second si layer, and the second si 1-x- y Ge x C y layers (0≤x≤1,0≤y≤1) which is formed adjacently in the second si layer and has the band gap different from the first si 1-x- y Ge x C y layer to that are installed in the channel region ; and first and second carrier accumulation layer for closing the carrier of the different conductivity type with the domain, near to the first si layer within the first Si 1-x- y Ge x C y layer and the domain near to the second si layer at the second si 1-x- y Ge x C y inside layer are formed respectively.

청구 18항:

Claim 18:

제 17 항에 있어서,상기 제 2 Si1-x-yGexCy층에 있어서의 C 의 조성비 y는 0인 것을 특징으로 하는 반도체 장치.

As for claim 17, the semiconductor device in which the composition ratio y of C in the second Si 1-x- y Ge x C y layer is 0.

청구 19항:

Claim 19:

제 17 항에 있어서,상기 반도체 기판상에 형성되어 단일조성의 반도체층을 채널영역으로 하는 M0S 트랜지스터를 추가로 구비하는 것을 특징으로 하는 반도체 장치.

As for claim 17, the semiconductor device for additionally including the MOS transistor which is formed in the substrate and has the semiconductor layer of the single-bath nature as the channel region.

청구 20항:

Claim 20:

제 17 항에 있어서,상기 제 1 의 Si1-x-yGexCy층에 있어서의 C의 조성비 y는, 0.01~0.03인 것을 특징으로 하는 반도체 장치.

As for claim 17, the semiconductor device in which the composition ratio y of C in the first si 1-x- y Ge x C y layer is 0.01~0.03.

청구 21항:

Claim 21:

제 17 항에 있어서,상기 제 1 의 Si1-x-yGexCy층의 각 원소의 조성비는, 상기 제 1 의 Si1-x-yGexCy층과 상기 제 1 Si 층이 격자 정합하는 조성비로 조정되어 있는 것을 특징으로 하는 반도체 장치.

As for claim 17, the semiconductor device in which the composition ratio of each element of the first si 1-x- y Ge x C y layer is adjusted to the first si 1-x- y Ge x C y layer and the composition ratio in which the first Si layer lattice-matches.

청구 22항:

Claim 22:

제 17 항에 있어서,상기 제 1 의 Si1-x-yGexCy층은 상기 제 1 의 Si 층의 격자정수보다 작은 격자정수를 갖고, 또한 격자완화를 일으키지 않는 막 두께를 갖는 것을 특징으로 하는 반도체 장치.

As for claim 17, the semiconductor device wherein the first Si 1-x- y Ge x C y layer has the film thickness that does not cause the lattice mismatch distortion it has the lattice constant smaller than the lattice constant of the first Si layer.

GF Exhibit 1124 - 2043/2704

청구 23항:

제 17 항 내지 제 22 항 중 어느 한 항에 있어서,상기 제 1 캐리어 축적층에 축적되는 캐리어는 부의 캐리어이고,상기 제 2 캐리어 축적층에 축적되는 캐리어는 정의 캐리어인 것을 특징으로 하는 반도체 장치.

Claim 23:

As for any one of claim 17 through 22, the semiconductor device in which the carrier accumulated in the first carrier accumulation layer is the carrier of t he part ; and the carrier accumulated in the second ca rrier the accumulation layer is the definition carrier.

청구 24항:

제 17 항 내지 제 22 항 중 어느 한 항에 있어서,상기 제 1 의 Si 층 내에서의 상기 제 1 의 Si1-x-yGexCy층에 근접한 영역에는, 상기 제 1 캐리어 축적층에 캐리어를 공급하기 위한 캐리어 공급층이 추가로 형성되는 것을 특징으로 하는 반도체 장치.

Claim 24:

As for any one of claim 17 through 22, the semiconductor device in which the carrier supply layer for supplying the carrier to the first carrier accumulatio n layer is additionally formed in the domain near to the first si 1-x- y Ge x C y layer within the first si layer.

청구 25항:

제 23 항에 있어서,상기 제 1 의 Si 층 내에서의 상기 제 1 의 Si1-x-yGexCy층에 근접한 영역에는, 상기 제 1 캐리어 축적층에 캐리어를 공급하기 위한 캐리어 공급층이 추가로 형성되는 것을 특징으로 하는 반도체 장치.

Claim 25:

As for claim 23, the semiconductor device in which the carrier supply layer for supplying the carrier to the first carrier accumulation layer is additionally formed in the domain near to the first si 1-x- y Ge x C y layer within the first si layer.

청구 26항:

제 17 항에 있어서,상기 제 1 및 제 2 의 Si1-x-yGexCy층 중 적어도 어느 한쪽의 Si1-x-yGexCy층은 양자 우물 영역으로 되어있는 것을 특징으로 하는 반도체 장치.

Claim 26:

As for claim 17, the semiconductor device in which the Si 1-x- y Ge x C y layer of at least one side consists of the quantum-well gain region among the Si 1-x- y Ge x C y layer of first and second.

청구 27항:

제 17 항 내지 제 22 항, 제 25 항 및 제 26 항 중 어느 한 항에 있어서,상기 제 1 및 제 2 의 Si1-x-yGexCy층 중 위쪽에 형성된 Si1-x-yGexCy층의 바로 위에 형성된 저저항의 도체막으로 된 소스#183#드레인 콘택트층을 추가로 구비하는 것을 특징으로 하는 반도체 장치.

Claim 27:

The semiconductor device for additionally including the source · drain contact layer consisting of the conducto r film of the low resistance formed in claim 17 to claim 22, and the Si 1-x- y Ge x C y layer, which as for any one of claim 25 and 26, is formed in the upside among t he Si 1-x- y Ge x C y layer of first and second immedia tely, the upper part.

청구 28항:

제 23 항에 있어서,상기 제 1 및 제 2 의 Si1-x-yGexCy층 중 위쪽에 형성된 Si1-x-yGexCy층의 바로 위에 형성된 저저항의 도체막으로 된 소스#183#드레인 콘택트층을 추가로 구비하는 것을 특징으로 하는 반도체 장치.

Claim 28:

As for claim 23, the semiconductor device for additionally including the source · drain contact layer c onsisting of the conductor film of the low resistance for med in the Si 1-x- y Ge x C y layer, formed in the upsid e among the Si 1-x- y Ge x C y layer of first and secon d immediately, the upper part.

청구 29항:

제 24 항에 있어서,상기 제 1 및 제 2 의 Si1-x-yGexCy층 중 위쪽에 형성된 Si1-x-yGexCy층의 바로 위에 형성된 저저항의 도체막으로 된 소스#183#드레인 콘택트층을 추가로 구비하는 것을 특징으로 하는 반도체 장치.

Claim 29:

As for claim 24, the semiconductor device for additionally including the source · drain contact layer c onsisting of the conductor film of the low resistance for med in the Si 1-x- y Ge x C y layer, formed in the upsid e among the Si 1-x- y Ge x C y layer of first and secon d immediately, the upper part.

청구 30항:

반도체 기판상에 형성된 적어도 1개의 전계 효과 트랜지스터를 구비한 반도체 장치에 있어서,상기 전계 효과 트랜지스터는,Si 1-x-yGexCy층(0#8804#x#8804#1, 0#8804#y#8804#

Claim 30:

The semiconductor device which comprises the first semiconductor layer in which the field effect transistor includes y Ge x C y layers (0≤x≤1, 0≤y≤1) as to the se

GF Exhibit 1124 - 2044/2704

1)을 포함하는 제 1 반도체층, 상기 제 l 반도체층과는 밴드 갭이 다른 반도체에 의해 구성되는 제 2 반도체층 및 상기 제 1, 제 2 반도체층 사이의 경계면 부근의 영역에 형성된 캐리어 축적층을 갖는 채널영역과,제 3 반도체층 및 이 제 3 반도체층보다 밴드 갭이 큰 반도체로 구성되는 제 4 반도체층을 갖는 소스#183#드레인 영역과,상기 제 3 반도체층의 바로 위에 형성된 저저항의 도체막으로 이루어지는 소스#183#드레인 콘택트층을 구비하는 것을 특징으로 하는 반도체 장치.

miconductor device equipped with at least one field effect transistor formed on the semiconductor substrate with the Si , and 1, the l semiconductor layer, and the source · drain contact layer consisting of the conductor film of the low resistance formed in the channel region, having the carrier accumulation layer formed in the second semiconductor layer and the first which the semiconductor in which the band gap is different is organized, and the domain of the boundary area neighborhood between the second semiconductor layer and the source · drain domain having the fourth semiconductor layer consisting of the semiconductor in which the band gap is greater than the third semiconductor layer and this third semiconductor layer, and the third semiconductor layer, immediately, the upper part.

청구 31항:

제 30 항에 있어서,상기 제 1 반도체층과 상기 제 3 반도체층은 공통의 제 1 반도체막에 의해 구성되고,상기 제 2 반도체층과 상기 제 4 반도체는 공통의 제 2 반도체막에 의해 구성되며, 상기 제 2 반도체막은 상기 제 1 반도체막의 위에 형성되는 것을 특징으로 하는 반도체 장치.

Claim 31:

As for claim 30, the semiconductor device in which the first semiconductor film of common is organized by the first semiconductor layer and the third semiconductor layer ; the second semiconductor film of common is organized by the second semiconductor layer and fourth semiconductor ; and the second semiconductor film is formed in the upper part of the first semiconductor film.

청구 32항:

제 30 항에 있어서,상기 제 1 반도체층과 상기 제 3 반도체층은 서로 다른 반도체막에 의해 구성되고,상기 제 3 반도체층은 상기 제 1 반도체층의 위쪽에 형성되고,상기 제 4 반도체층은 상기 제 3 반도체층의 위에 형성되는 것을 특징으로 하는 반도체 장치.

Claim 32:

As for claim 30, the semiconductor device in which the different semiconductor film is organized by the first semiconductor layer and the third semiconductor layer ; the third semiconductor layer is formed in the upside of the first semiconductor layer ; and the fourth semiconductor layer is formed in the upper part of the third semiconductor layer.

청구 33항:

n-채널 전계 효과형 트랜지스터와, p-채널 전계 효과형 트랜지스터를 갖는 반도체 장치의 제조방법에 있어서,반도체 기판상에, 제 1 Si 층과, 상기 Si 층에 근접함과 동시에 상기 제 1 Si 층에 근접한 영역에 상기 n-채널 전계 효과형 트랜지스터의 채널로 되는 제 1 캐리어 축적층을 갖도록 제 1 의 Si1-x-yGexCy층(0#8804#x#8804#l, Oy#8804# 1)을 형성하는 제 1 공정과,반도체 기판상에, 제 2 Si 층과, 상기 제 2 Si 층에 근접함과 동시에, 상기 제 1 의 Si1-x-yGexCy층과는 다른 밴드 갭을 갖고, 상기 제 2 의 Si 층에 근접한 영역에 상기 p-채널 전계 효과형 트랜지스터의 채널로 되는 제 2 캐리어 축적층을 갖는 제 2 Si1-x-yGexCy층(0#8804#x#8804#1,0#8804#y#8804#1)을 형성하는 제 2 공정과,상기 제 1 및 제 2 의 Si 1-x-yGexCy층 중 위쪽에 위치하는 Si1-x-yGexCy층위에 도체막을 퇴적한 후, 이 도체막을 패터닝하여 상기 n-채널 전계 효과형 트랜지스터 및 p-채널 전계 효과형 트랜지스터의 게이트 전극을 각각 형성하는 제 3 공정과,상기 각 트랜지스터의 게이트 전극을 마스크로서, 상기 n-채널 전계 효과형 트랜지스터 형성 영역에는 적어도 상기 제 1 캐리어 축적층에 도달하는 깊이까지 n 형 불순물을, 상기 p-채널 전계 효과형 트랜지스터 형성 영역에는 적어도 상기 제 2 캐리어 축적층에 도달하는 깊이까지 p형 불순물을 각각 도입하고, 상기 n-채널 전계 효과형 트랜지스터 및 p-채널 전계 효과형 트랜지스터의 소스#183#드레인 영역을 각각 형성하는 제 4 공정을 구비하는 것을 특징으로 하는 반도체 장치의 제조방법.

Claim 33:

After doing the deposition the first Si layer, on the semiconductor substrate, as to the n-channel field effect transistor, and the method for fabricating semiconductor device, having the p-channel field effect transistor and the first Si 1-x- y Ge x C y layer (0≤x≤l, Oy≤ 1) the conductor film in the second Si layer, on the first process of forming, and semiconductor substrate, and the second process, of forming second Si 1-x- y Ge x C y layers (0≤x≤1,0≤y≤1) having the second carrier the accumulation layer consisting of the channel of the p-channel field effect transistor on the domain near to the second si layer it has the band gap different from the first si 1-x- y Ge x C y layer to that it comes close to the second Si layer and the Si 1-x- y Ge x C y layer positioned in the upper direction among the Si 1-x- y Ge x C y layer of first and second it has the first carrier accumulation layer consisting of the channel of the n-channel field effect transistor on the domain near to the first Si layer it comes close to the Si layer. The method for fabricating semiconductor device which comprises the third process of patterning this conductor film and forming the gate electrode of the p-channel field effect transistor and n-channel field effect transistor, the n-channel field effect transistor the n type impurity the p-type impurity is introduced to the depth reaching at least first carrier accumulation layer in the n-channel field effect transistor formation area in the p-channel field effect t

GF Exhibit 1124 - 2045/2704

ransistor formation area to the depth reaching at least second carrier the accumulation layer it is the gate ele ctrode of each transistor the features, and the fourth process of forming the source · drain region of the p-c hannel field effect transistor.

청구 34항:

Si1-x-yGexCy층 (0#8804#x#8804#1,0#8804#y#8804#1)을 포함하는 제 1 반도체층과, 상기 제 1 반도체층과는 다른 밴드 갭을 갖는 제 2 반도체층과, 상기 제 1,제 2 반도체층 사이의 경계면 부근의 영역에 형성된 채널로 되는 캐리어 축적층 갖고, 전계 효과 트랜지스터로서 기능하는 반도체 장치의 제조방법에 있어서,반도체 기판의 전계 효과 트랜지스터 형성 영역에, 제 3 반도체층과, 이 제 3 반도체층보다 큰 밴드 갭을 갖는 제 4 반도체층을 차례로 형성하는 제 I의 공정과,상기 제 4 반도체층의 위쪽에 도체막을 퇴적한 후, 이 도체막을 패터닝하여 게이트막을 형성하는 제 2 공정과,상기 게이트 전극 양측에 위치하는 상기 전계 효과형 트랜지스터 형성 영역에 적어도 상기 캐리어 축적층에 도달하는 깊이까지 불순물을 도입하여, 소스#183#드레인 영역을 형성하는 제 3 공정과,상기 소스#183#드레인 영역에서의 상기 제 4 반도체층을 적어도 상기 제 3 반도체층이 노출될 때까지 에칭에 의해 제거하는 제 4 공정과,상기 제 3 반도체층이 노출된 면 위에 저저항의 도체막으로 이루어지는 소스#183#드레인 콘택트층을 형성하는 제 5 공정을 구비하는 것을 특징으로 하는 반도체 장치의 제조방법.

Claim 34:

After doing the deposition the conductor film in the upside of the process of the I which has with the carrie r accumulation layer ; and consists of the channel form ed in the second semiconductor layer, having of the fir st semiconductor layer including Si 1-x- y Ge x C y laye rs (0#8804#x#8804#1,0#8804#y#8804#1) and has th e band gap different from the first semiconductor layer to that and the first, and the domain of the boundary a rea neighborhood between the second semiconductor l ayer successively forms the fourth semiconductor layer having the third semiconductor layer, in the field effect transistor formation area, of the semiconductor substra te as to the method for fabricating semiconductor devi ce, functioning as the field effect transistor and the ba nd gap which is greater than this third semiconductor l ayer. And fourth semiconductor layer. The method for f abricating semiconductor device patterning this conduc tor film and includes the second process of forming the gate film, the third process of introduces the impurity t o the depth, at least third semiconductor layer is the f ourth process of removing with the etching until is exp osed the fourth semiconductor layer at the source #18 3# drain region, and the third process of forming the so urce #183# drain contact layer which is made of the c onductor film of the low resistance in over face, and th e third process of introduces the impurity to the depth reaches ; and forming the source #183# drain region in at least carrier accumulation layer in the field effect tr ansistor formation area positioned at the gate electrod e both sides; and as to the third process of, the third s emiconductor layer is exposed.

청구 35항:

제 34 항에 있어서,상기 제 1 공정은, 상기 제 1 및 제 3 반도체층을 공통의 제 1 반도체막으로 구성하고, 상기 제 2 및 제 4 반도체층을 공통의 제 2 반도체막으로 구성하는 것을 특징으로 하는 반도체 장치의 제조방법.

Claim 35:

As for claim 34, the method for fabricating semiconductor device which the first process organizes the first and the third semiconductor layer on the first semiconductor film of common ; and comprises the sec ond and fourth semiconductor layer to the second semi conductor film of common.

청구 36항:

제 34 항에 있어서,상기 제 1 공정의 앞에 상기 제 1 및 제 2 반도체층을 형성하는 공정을 추가로 구비하고,상기 제 1 공정은 상기 제 1 반도체층의 위쪽에 제 3 반도체층을 형성하도록 행하는 것을 특징으로 하는 반도체 장치의 제조방법.

Claim 36:

As for claim 34, the method for fabricating semiconductor device which it additionally includes the process of forming first and second semiconductor laye r in the front of the first process ; and it performs so t hat the first process forms the third semiconductor lay er on the upside of the first semiconductor layer.

청구 37항:

제 34 항 내지 제 36 항 중 어느 한 항에 있어서,상기 제 4 공정은 상기 제 3 반도체층과 상기 제 4 반도체층과 대한 에칭 선택비가 높은 에칭조건으로 하는 것을 특징으로 하는 반도체 장치의 제조방법.

Claim 37:

As for any one of claim 34 through 36, the method for fabricating semiconductor device which the fourth proc ess is done by the etching condition in which the etchi ng selectivity treated the third semiconductor layer an d fourth semiconductor layer is high.

GF Exhibit 1124 - 2046/2704

배경기술

본 발명은, 반도체 장치에 관하여, 특히, SiGeC 층 또는 SiGe 층을 이용하는 헤테로 접합의 전계 효과형 트랜지스터를 구비한 반도체 장치 및 그 제조방법에 관한 것이다.

최근, 반도체 장치의 고집적화가 진행되고 있지만, M0S 형 트랜지스터의 미세화도 게이트 길이가 O.1#956#m를 하회하는 초미세화 영역에서는, 단채널 효과의 영향이나 저항성분의 증대 등에 의해, 전류 구동 능력이 포화하는 등, 지금까지와 같은 성능 향상을 기대할 수 없는 것이 예상되고 있다. 특히, 미세 M0S 트랜지스터의 고 구동력화를 위해서는, 채널의 캐리어 이동도의 향상이나, 소스#183#드레인 전극의 콘택트의 저 저항화가 중요하다.

그래서, 실리콘 기판 상에 형성되는 단일 조성의 Si를 이용한 상보형 반도체 장치(CMOS 장치)에 대신하여, Si/SiGe 계(IV 족 혼합 결정)에 의한 헤테로 구조 CMOS 장치(Heterostructure CMOS : 이하, HCMOS 장치라 한다)가 제안되어 있다. 이것은, 채널로서 Si/SiO2 경계면이 아니라 밴드 갭이 상이한 두 종류의 반도체에 의한 헤테로 접합체의 경계면을 이용하는 것이다. 이러한 Si보다도 높은 캐리어 이동도를 부여하는 Si/SiGe 계를 이용함으로써, 더욱 더 고속인 소자를 실현할 수 있다고 기대되고 있다. 이 Si/SiGe 계에서는, 조성의 제어에 의해 Si 기판 상에 원하는 왜곡 양과 밴드 값을 갖는 에피텍셜 성장층을 형성하는 것이 가능하다. IBM 사의 Ismail은, Si/SiGe 계의 HCMOS 장치에 의한 특성 향상에 관해서의 기초 실험을 한다 (K.Ismail, Si/SiGe High Speed Field-Effect Transistors , IEDM Tech. Dig. 1995. p509. 및 M.A. Armstrong et al, Design of Si/SiGe Hetrojunction Complementary Metal-Oxide-Semiconductor TransistorsIEDM Tech. Dig. 1995,p701을 참조).

도 15는, 이 HCMOS 장치의 일례를 나타내는 단면도이다. 도 15에 도시한 바와 같이, Si 기판(101)의 일부에는, 소스#183#드레인 영역(109)과, 게이트 절연막(107) 및 그 위에 게이트 전극(110)으로 구성되는 전계 효과형 트랜지스터가 설치된다. 그리고, 게이트 전극(110)의 아래쪽에 의한 소스 영역-드레인 영역 사이의 소위 채널영역에는, SiGe 버퍼층(102)과, #948# 도핑층(115)과, 스페이스층(103)과, i-Si층(104)과, i-SiGe 층(105) 및 i-Si층(106)이 형성되어 있다. 이들의 영역에서, SiGe 버퍼층(102)은, i-Si층(104)과 i-SiGe층(105)의 사이에 n-채널층(112)을 형성하기 위해서, i-Si 층(104)에 인장 왜곡을 주는 것이다. 이 SiGe 버퍼층(102)에 있어서, Si 기판(101)의 바로 위에서는 Ge 조성비가 0%로 되고, 최상에서는 Ge 조성비가 30%로 되도록 단계적으로 조성비가 변경되어 있다.

Background Art

The present invention relates to semiconductor device and method for manufacturing same including especially, the field effect transistor of the SiGeC layer or the heterojunction using the SiGe layer about the semiconductor device.

Recently, the high integration of the semiconductor device is progressed. However IDRIVE is saturated in the hyperfine domain in which the miniaturization of the M0S type transistor the gate length is the O.1μm with the enlargement of the influence of the short channel effect or the parasitic resistance etc. The influence are expected to cannot expect the same performance improvement to the now. Especially, it is for the high driving force of the minute MOS transistor and the low resistance of the contact of the improvement of the carrier mobility of the channel or the source · drain electrode is important.

So, it replaces in the complementary semiconductor device (the CMOS apparatus) using the Si of the single composition formed on the silicon substrate and the hetero structure CMOS apparatus (it says to be the HCMOS apparatus less than Heterostructure CMOS :) by the Si / SiGe group (IV group mixed crystal) is proposed. This is not Si / SiO2 boundary face but this uses the boundary face of the heterozygote by the semiconductor of two types in which the band gap is different as the channel. The Si / SiGe precept giving the carrier mobility higher than such Si is used. In that way that the device which is the high speed can be more and more realized it is expected. In this Si / SiGe group, the control is possible to form the desired distortion amount and the epitaxial growth layer having the band value with the control of the composition on the Si substrate. The Ismail of the IBM Corporation experiments with the basis of the characteristic enhancement by the HCMOS apparatus of the Si / SiGe group (k. The Ismail, the Si / SiGe High Speed Field-Effect Transistors , IEDM Tech. Dig. 1995. p509. and M A. Armstrong et al, and the reference the Design of Si / SiGe Hetrojunction Complementary Metal-Oxide-Semiconductor TransistorsIEDM Tech. Dig. 1995,p701).

Figure 15 is a cross-sectional view an example of this HCMOS apparatus is shown. As shown in Figure 15, the field effect transistor consisting of the source · drain region (109), and the gate electrode (110) in the gate insulating layer (107) and the upper part may be installed in the part of the Si substrate (101). And the so-called channel region between the area-source - drain region by the downside of the gate electrode (110) may be provided with the SiGe buffer layer (102), with the δ doped layer (115), with the space layer (103), with the i-Si layer (104), the i-SiGe layer (105) and i-Si layer (106). In their domain, in order that the SiGe buffer layer (102) forms the n- channel layer (112) between the i-Si layer (104) and i-SiGe layer (105) the tensile distortion is given to the i-Si layer (104). As to this SiGe buffer layer (102), the Ge composition ratio is in the Si substrate (101), immediately, the upper part to 0% and the composition ratio of the Ge composition ratio is graduall

GF Exhibit 1124 - 2047/2704

y changed in the best to 30% as as possible.

여기서, 부 바이어스가 인가되면, i-Si 층(104)에 있어서 아래쪽의 SiGe 버퍼층(102)과의 헤테로 경계면에 n-채널층(112)이 형성된다. #948# 도핑층(115)은 위쪽에 형성되는 n-채널층(112)에 캐리어인 전자를 공급한 것이다. 또한, 스페이스층(103)은, 아래쪽으로 형성된 #948# 도핑층(115)의 이온과 위쪽의 n-채널층(112)을 공간적으로 분리하여, 캐리어의 이온 산란에 의한 이동도의 저하를 방지한 것이다.

Here, if the negative bias is applied , the n- channel layer (112) is formed in the hetero boundary face with the SiGe buffer layer (102) of the downside as to the i-Si layer (104). The electron which is the carrier is supplied to the n- channel layer (112) in which the δ doped layer (115) is formed in the upside. Moreover, the space layer (103) downwards spatially separates the ion of the formed δ doped layer (115) and n- channel layer (112) of the upside and it prevents the degradation of mobility by the ion scattering of the carrier.

또한, 정 바이어스가 인가되면, i-SiGe 층(105)에 있어서, 위쪽의 i-Si층(106)과의 헤테로 경계면에는 p-채널층(111)이 형성된다. 게이트 절연막(107)은, 게이트 전극(110)과 p-채널층(111)을 절연하기 위한 것이다.

Moreover, the hetero boundary face with the i-Si layer (106) of the upside as to the i-SiGe layer (105), the positive bias is applied may be provided with the p- channel layer (111). The gate insulating layer (107) is to insulate the gate electrode (110) and p- channel layer (111).

상술한 바와 같이, 헤테로 전계 효과 트랜지스터에서는, 밴드 갭이 다른 두 종류의 반도체층 간의 헤테로 경계면에 채널을 형성하는 것이 특징이다. 따라서, 채널 형성을 위해 필연적으로 밴드 갭이 다른 적어도 두 가지의 반도체층이 존재한다. 덧붙여, 반도체층 중에 전자 또는 정공이 고속으로 이동하기 위한 채널을 형성하기 위해서는, 헤테로 경계면에 전도대 또는 가전자대의 불연속부를 갖는 것이 필요하게 된다. 상술한 Si/SiGe 계에서는, 정공에 대해서는 SiGe 층(105)이 i-Si 층(106)에 대하여 가전자대에 있어서의 불연속부를 갖기 때문에, 정공용의 채널이 형성된다 (도 15의 왼쪽 부분 참조). 그러나, 전도대에는 불연속부가 거의 없기 때문에, 전자용의 채널을 형성하기 위하여 i-Si 층(104)에 인장 왜곡을 인가함으로써, i-SiGe 층(105)과의 헤테로 경계면에 전도대의 불연속부를 형성하고 있다 (도 15의 오른쪽 부분참조).

As described above, in the hetero field effect transistor, it is characterized to form the channel on the hetero boundary face between the semiconductor layer of two types in which the band gap is different. Therefore, the semiconductor layer of at least two kinds of in which the band gap is inevitably different exists for the channel-forming. Moreover, in order that the channel in which the electron or the hole moves at high speed is formed among the semiconductor layer the channel is necessary to have the discontinuity of the condition band or the valence band on the hetero boundary face. In the above-described Si / SiGe group, the SiGe layer (105) has the discontinuity in the valence band about the hole about the i-Si layer (106). Therefore the channel for the hole is formed (the left reference modification of fig. 15). But in the condition band, there is nearly no discontinuity. Therefore the tensile distortion is applied in the i-Si layer (104) in order to build up the channel for the electron. In that way the discontinuity of the condition band is formed on the hetero boundary face with the i-SiGe layer (105) (the right reference modification of fig. 15).

이러한 구조를 갖는 HCMOS 장치는, Si/Si02에 의한 채널을 사용하는 종래의 CMOS 장치에 비교하여, 같은 가공 치수로 2배의 고속도 동작을 1/2의 소비 전력으로 실현할 수 있는 것이 시뮬레이션의 결과로부터 예상되고 있다. 즉, Si 반도체와 SiGe 혼합 결정을 조합함으로써 헤테로 경계면을 형성하여, 고이동도 채널을 형성한 반도체 소자로서, 헤테로 접합을 이용하는 소자의 고속 동작과, M0S 장치의 대규모 집적성을 모두 실현하는 소자로서 매우 주목을 끌고 있다.

It compares in the conventional CMOS apparatus in which the HCMOS apparatus for having such structure uses the channel by the Si / Si02 and it is expected as the same processing measure from the result of the simulation that the high speed of two times can realize the operation with the power consumption of 1/2. That is, the hetero boundary face is formed by assembling the Si semiconductor and SiGe mixed crystal and it is the semiconductor device in which the high mobility forms the channel and attention is very pulled as the high speed operation of using the heterojunction of the device and the device which altogether realizes the highly integraded anger of the M0S apparatus.

발명의 내용

Summary of Invention

발명의 효과

Effects of the Invention

청구항 1~16에 의하면, 전계 효과 트랜지스터를 갖는 반도체 장치에 있어서, Si 층과 C의 조성비 y가 0.01~0.03인 Si1-x-yGexCy층을 설치하고, Si1-x-yGexCy층 내에 형성되는 캐리

According to claim 1~16, the Si 1-x- y Ge x C y layer in which the composition ratio y of C and Si layer was 0.01~0.03 was set up as to the semiconductor device

GF Exhibit 1124 - 2048/2704

어 축적층을 채널로서 이용하도록 하였기 때문에, 동작속도가 크고 또한 신뢰성이 높은 전계 효과형 트랜지스터를 갖는 반도체 장치의 제공을 도모할 수 있다.

for having the field effect transistor and the carrier accumulation layer formed within the Si 1-x- y Ge x C y layer was used as the channel. Therefore the provision of the semiconductor device for the working speed being large and having the field effect transistor in which moreover, the reliability is high can be planned.

청구항 17~29에 의하면, 전계 효과형 트랜지스터를 갖는 반도체 장치에 있어서, 제 1 의 Si 층과 제 1 의 Si1-x-yGexCy층 사이, 제 2 의 Si 층과 제 2 의 Si1-x-yGexCy층 사이의 경계면에 생기는 밴드 불연속부를 이용하여 전자와 정공을 2차원적으로 폐쇄하는 축적층을 형성하고, 이 축적층을 채널로 하는 전계 효과 트랜지스터를 설치하였기 때문에, 캐리어의 폐쇄 효율이 높은 채널을 갖고 또한 동작 속도가 크고 또한 신뢰성이 높은 n-채널 및 p-채널 전계 효과 트랜지스터를 구비한 HCMOS 장치로서 기능하는 반도체 장치의 제공을 도모할 수 있다.

According to claim 17~29, the accumulation layer closing the electron and hole due to two dimensional using the band discontinuity part generated in the boundary face between the second si 1-x- y Ge x C y layer and the second si layer was formed as to the semiconductor device for having the field effect transistor for the first si layer and the first si 1-x- y Ge x C y layer and the field effect transistor this accumulation layer to the channel was set up. Therefore the provision of the semiconductor device for functioning as the HCMOS apparatus which has the channel in which the closure efficiency of the carrier is high and in which moreover, the working speed is large and including the n-channel and the p-channel electric field effect transistor in which moreover, the reliability is high can be planned.

이 반도체 장치의 구조는, 청구항 33의 반도체 장치의 제조방법에 의해 용이하게 실현할 수가 있다.

The structure of this semiconductor device can realize with the method for fabricating semiconductor device of claim 33.

청구항 30~32에 의하면, Si1-x-yGexCy층을 포함하는 제 1 반도체층과 제 2 반도체층 사이에 채널로 되는 밴드 불연속부를 형성시킨 전계 효과 트랜지스터를 갖는 반도체 장치에 있어서, 소스#183#드레인 영역을 제 3 반도체층 및 제 3 반도체층보다 밴드 갭이 큰 제 4 반도체층에 의해 구성되고, 이 제 3 반도체층의 바로 위에 저저항의 도체막으로 이루어지는 소스#183#드레인 콘택트층을 설치하였기 때문에, 헤테로 접합을 이용한 동작 속도가 높으며 또한 소스#183#드레인 콘택트 저항이 작은 반도체 장치의 제공을 도모할 수 있다.

According to claim 30~32, it was the source · drain region composed by the fourth semiconductor layer in which the band gap was greater than the third semiconductor layer and the third semiconductor layer as to the semiconductor device for having the field effect transistor forming the band discontinuity part consisting to the channel between the first semiconductor layer and the second semiconductor layer including the Si 1-x- y Ge x C y layer and the source · drain contact layer consisting of the conductor film of the low resistance was set up in this third semiconductor layer, immediately, the upper part. Therefore the working speed using the heterojunction is high and the provision of the semiconductor device in which moreover, the source · drain contact resistance is small can be planned.

이 반도체 장치의 구조는, 청구항 34~37의 반도체 장치의 제조방법에 의해 용이하게 실현할 수가 있다.

The structure of this semiconductor device can realize with the method for fabricating semiconductor device of claim 34~37.

본 발명의 바람직한 실시예들은 예시의 목적을 위해 개시된 것이며, 당업자라면 첨부된 특허청구범위에 개시된 본 발명의 사상과 범위를 통해 각종 수정, 변경, 대체 및 부가가 가능할 것이다.

The preferred embodiments of the invention is disclosed for the exemplary purpose and the various kinds modification, the change, and the substitution and addition will be possible in the patent claim which is attached if it is the person skilled in the art through thought and range of the disclosed invention.

기술적 과제

Technical Task

그렇지만, 상술한 바와 같은 SiGe 등의 IV족 혼합 결정을 이용하는 헤테로 장치는 종래의 CM0S 장치의 성능 한계를 극복하는 방법으로서 크게 기대되고 있지만, SiGe로 대표되는 IV족 혼합 결정을 이용하는 헤테로 전계 효과 트랜지스터는, 그 제조가 곤란하기 때문에 같은 SiGe 혼합 결정을 이용한 헤테로 장치인 헤테로 바이폴라 트랜지스터에 비교하여 연구 개발이 늦

However, the review of the structure the expected performance is yet enough exhibited the hetero appara tus for using the IV group mixed crystal is expected as the method for overcoming the performance limitation o f the conventional CM0S apparatus and however it com pares in the hetero bipolar transistor which is the heter

GF Exhibit 1124 - 2049/2704

게 되고, 아직 그 기대되는 성능을 충분히 발휘하도록 구조 및 제조 방법의 검토가 충분히 행하여지고 있다고는 할 수 없다. 또한, 헤테로 전계 효과 트랜지스터 중에서도, 상술한 바와 같은 게이트 전극과 반도체층 사이에 절연막을 갖는 소위 헤테로 MOS 구조의 경우, SiGe 층 내에는 안정에서 양호한 절연막을 형성할 수 없기 때문에, 게이트 절연막으로서 SiO2로 이루어지는 산화막을 사용한다. 따라서, 게이트 절연막의 바로 아래는 반드시 Si층 일 필요가 있지만, Si는 SiGe에 비교하여 반드시 밴드 갭이 커진다고 하는 특징을 갖고 있다.

o apparatus using the SiGe mixed crystal which thes same because the manufacture the hetero field effect transistor using the IV group mixed crystal represented as the SiGe is too much and research and development are late and a manufacturing method thereof of the SiGe etc as described above is enough performed. Moreover, among the hetero field effect transistor, the good insulating layer cannot be formed at the stability between the gate electrode as described above and semiconductor layer in case of the so-called hetero metal oxide semiconductor structure of having the insulating layer within the SiGe layer. Therefore the oxide film consisting of the SiO2 is used as the gate insulating layer. Therefore, the certainly the gate insulating layer, immediately, the lower part need to be the Si layer. However the Si compares in the SiGe and it has the characteristic in which the band gap is certainly enlarged.

그 때문에, 상기 종래의 HCMOS 장치의 구조에 있어서는, 이하와 같은 문제가 있었다.

Consequently, it was in the structure of the conventional HCMOS apparatus and the structure had the problem like this.

첫번째로, 상술한 바와 같이 Si 기판(101)상에 전자의 채널을 형성하기 위하여, i-Si 층(104)에 인장 왜곡을 인가하여, Si/SiGe 헤테로 경계면에 밴드 불연속을 형성하고 있다. 그러나, 격자정수를 변화시킴으로써, 격자 완화에 의한 전위의 도입을 수반한다.

First, as described above, in order that the channel of the electron is formed on the Si substrate (101) the tensile distortion is applied in the i-Si layer (104) and the band discontinuity is formed on the Si / SiGe hetero boundary face. But the lattice constant is diversified. In that way the introduction of the electric potential by the lattice mismatch distortion is accompanied.

도 16은, SiGe 버퍼층(102)과 그 위의 i-Si 층(104)을 발췌하여 나타내는 단면도이다. i-Si 층(104)은, SiGe 버퍼층(102)보다도 격자정수가 작기 때문에, 결정 성장된 단계에서 인장왜곡이 축적된다. 이 왜곡의 축적이 커지면, 도 16에 도시하는 바와 같이, i-Si 층(104)에 전위가 입력된다. 이와 같이, i-Si 층(104)과 SiGe 버퍼층(102)의 사이에 걸친 격자 부정합 왜곡에 의한 전위나 결함의 도입은 피할 수 없다. 따라서, 이 결정을 이용한 소자의 초기 특성은 어쨌든, 신뢰성이나 수명의 관점에서는 전위의 증식 등에 의한 특성 열화의 영향이 생겨난다고 여겨진다.

Figure 16 is a cross-sectional view the SiGe buffer layer (102) and i-Si layer (104) are extracted and it shows. As to the i-Si layer (104), the lattice constant is smaller than the SiGe buffer layer (102). Therefore the tensile distortion is accumulated in the step undergoing crystal growth. If the accumulation of this distortion is enlarged , as shown in Figure 16, the electric potential is inputted to the i-Si layer (104). In this way, the introduction of the electric potential by the i-Si layer (104) and the lattice mismatch distortion or the deformity of spanning between the SiGe buffer layer (102) cannot avoid. Therefore, the initial attribute of the device of using this Decision is anyhow regarded that the influence of the characteristic deterioration including the proliferation of the electric potential etc. appears in the viewpoint of the reliability or the lifetime.

또한, Si 기판 (l01)상에 Si보다 격자 정수의 큰 SiGe로 이루어지는 SiGe 버퍼층(102)을 적층하여, 그 위에 성장하는 i-Si 층(104)에 인장 왜곡을 적층시키고 있지만, SiGe 버퍼층(102)의 막 두께를 크게 하면, 그 사이에 SiGe 버퍼층(102)의 격자정수가 Si의 격자정수로부터 원래의 SiGe의 격자정수로 변화하는 임계막 두께를 초월하기 때문에, 격자완화가 생겨 SiGe 버퍼층(102)에도 전위 등의 결함이 도입된다.

Moreover, the SiGe buffer layer (102) made of the big SiGe of the lattice constant than the Si is laminated on the Si substrate (l01) and the tensile distortion is laminated in the i-Si layer (104) growing in the upper part. However if it makes the film thickness of the SiGe buffer layer (102) large , the critical membrane thickness in which the lattice constant of the SiGe buffer layer (102) changes into the lattice constant of the original SiGe in the interval from the lattice constant of the Si is transcended. Therefore the lattice mismatch distortion is generated and the deformity including the electric potential etc. is introduced to the SiGe buffer layer (102).

이것들의 결함은, 소자의 초기 특성으로의 영향은 적은 경우도 있지만, 장기적인 신뢰성이나 수명이라는 관점에서는 중대한 문제를 야기할 우려가 있다. 즉, 전류에 의한 결함의 증식이나 금속이나 불순물의 결함을 개재한 확산에 의한 열화가 생겨 신뢰성의 저하를 초래하는 우려가 있다.

From the viewpoint of the reliability or the lifetime it has the deformity of these even in case the influence to the initial attribute of the device is less and however long-term, it has the concern causing the important problem. That is, it has the concern arousing the deterior

GF Exhibit 1124 - 2050/2704

ation by the diffusion interposing the deformity of the p roliferation of the deformity by the current or the metal or the impurity and causes the degradation of the relia bility.

본 발명의 제 1 목적은, HCMOS 장치의 게이트 아래쪽의 채널 영역에 걸친 구조로서 캐리어 축적층을 형성할 수 있는 밴드 불연속부를 갖으면서 격자 정합 또는 거의 격자 정합된 헤테로 접합체를 이용함으로써, 캐리어의 이동도가 높고 또한 신뢰성이 높은 반도체 장치를 제공하는 것에 있다.

While the first object of the present invention has the band discontinuity part forming the carrier accumulatio n layer as the structure of spanning the channel region of the gate downside of the HCMOS apparatus it uses t he lattice matching or the heterozygote which the near ly is lattice-matched. In that way the mobility of the c arrier is high and it provides the semiconductor device i n which moreover, the reliability is high the carrier has.

두번째로, SiGe로 대표되는 IV족 혼합 결정을 이용한 헤테로 전계 효과 장치는 종래의 미세 CM0S 장치의 성능 한계를 극복하는 소자 구조로서 유효한 기술이지만, 현시점에서는 채널 이동도의 향상의 연구에 비하여 소스#183#드레인 전극의 콘택트의 최적화의 검토는 더욱 불충분하고, 그 고이동도를 충분히 활용하는 구조로 되는 것은 아니다. 상술한 IBM 사에 의한 헤테로 CMOS 장치의 기술도 채널 영역의 이동도 향상에 있어서는 상세한 검토가 이루어지고 있지만, 미세 트랜지스터의 성능 향상에 중요한 또 하나의 요소인 소스#183#드레인 전극의 콘택트의 저저항화에 있어서는 거의 검토가 이루어지지 않고 있다.

Secondly, it is the technology which is effective as the device structure where the hetero field effect device u sing the IV group mixed crystal represented as the SiG e overcomes the performance limitation of the conventi onal minute CM0S apparatus. However the review of th e optimization of the contact of the source · drain elec trode is insufficient in the present point in comparison with the research of the improvement of the channel s hift drawing and it does not consist of the structure of enough utilizing the high mobility. It is in the improveme nt and the detail review the above-described technolo gy of the hetero CMOS apparatus by the IBM Corporati on the movement of the channel region is achieved. Ho wever it is in the low resistance of the contact of the source · drain electrode which is one element important in the performance improvement of the minute transist or and the review is not nearly achieved.

즉, Si 단결정을 이용한 CM0S 장치 구조에 있어서는, 소스#183#드레인 전극에 접속되는 기판측의 콘택트 영역의 구조에 있어서는 여러 가지의 검토가 이루어지고 있지만, 일반적인 CM0S 장치에 있어서의 최적의 콘택트 영역의 구조 및 형성방법이, 소자 구조가 다른 헤테로 전계 효과 장치에 있어서도 최선인지 어떤지는 검토가 필요하다.

That is, in the CM0S device structure of using the Si monocrystal and it is in the structure of the contact ar ea of the substrate side connected to the source · drai n electrode and the review of the various is achieved. However the review any kind of paper is requisite whet her it is the best as to the hetero field effect device in which the device structure of structure and method for forming the same of the optimal contact area in the ge neral CM0S apparatus are different.

본 발명의 제 2 목적은, 헤테로 전계 효과 장치가 뛰어난 특성을 손상시키는 일없이 작은 콘택트 저항을 발휘할 수 있는 콘택트 영역을 갖는 반도체 장치 및 그 제조방법을 제공하는 것에 있다.

The second object of the present invention has to provide semiconductor device and method for manufact uring same having the contact area exhibiting the small contact resistance without the task injuring the proper ty that the hetero field effect device is excellent.

발명의 구성 및 작용

Structure & Operation of the Invention

상기 제 1 목적을 달성하기 위해서, 본 발명에서는, 청구항 1~16에 기재되어 있는 제 1 반도체 장치에 관한 수단과, 청구항 17~29에 기재되어 있는 제 2 반도체 장치에 관한 수단과, 청구항 33에 기재되어 있는 제 1 반도체 장치의 제조방법에 관한 수단을 강구하고 있다.

To accomplish the first object, in the present invention, the means about the means about the mean s about the first semiconductor device for being writte n in claim 1~16 and the second semiconductor device f or being written in claim 17~29 and the first method fo r fabricating semiconductor device written in claim 33 a re taken.

상기 제 2 목적을 달성하기 위해서, 본 발명에서는, 청구항 30~32에 기재되어 있는 제 3 반도체 장치에 관한 수단과, 청구항 34~37에 기재되어 있는 제 2 반도체 장치의 제조방법에 관한 수단을 강구하고 있다.

To accomplish the second object, in the present invention, the means about the means about the third semiconductor device for being written in claim 30~32 and the second method for fabricating semiconductor d evice written in claim 34~37 are taken.

GF Exhibit 1124 - 2051/2704

본 발명의 제 1 반도체 장치는, 청구항 1에 기재되어 있는 바와 같이, 반도체 기판의 일부에 형성되어 게이트 전극과 소스#183#드레인 영역 및 해당 소스#183#드레인 영역사이의 채널 영역을 갖는 전계 효과 트랜지스터를 구비하고 있는 반도체 장치로서, 상기 채널영역에는 Si 층과, 상기 Si 층에 접하여 형성되고 C의 조성비 y가 0.01~0.03인 Si1-x-yGexCy 층 (0#8804# x #8804#1, 0y#8804# 1)이 설치되고, Si1-x-yGexCy 층 내에서의 상기 Si 층에 근접한 영역에는 캐리어 축적층이 형성되어 있다.

The channel region the first semiconductor device of the invention is written in claim 1 may be provided with the carrier accumulation layer in the domain which the Si layer, and Si 1-x- y Ge x C y layers (0≤ x ≤1, 0y≤ 1) which contact to the Si layer and which are formed an d in which the composition ratio y of C is 0.01~0.03 ar e installed and comes close to the Si layer within the Si 1-x- y Ge x C y layer.

이에 따라, C의 조성비 y가 0#183#01~0.03인 Si1-x-yGexCy 층과 Si 층의 경계면에는 캐리어를 2차원적으로 가두는 캐리어 축적층을 형성하는 데 필요한 밴드 불연속부를 형성하는 것이 가능하다. 그리고, 이 캐리어 축적층이 채널로서 기능하기 때문에, Si 층보다도 큰 캐리어 이동도를 부여하는 Si 1-x-yGexCy 층을 채널로 하는 동작 속도가 큰 전계 효과형 트랜지스터를 얻을 수 있다. 더구나, Si1-x-yGexCy 층과 Si 층 사이에서는 격자 부정합이 없게되거나 혹은 매우 작게 되도록 제어할 수 있기 때문에, 격자 왜곡을 0 혹은 거의 없도록 조정할 수 있고, Si1-x-yGexCy 층에 결정 결함이 도입되지 않도록 구성하는 것이 가능하다. 따라서, 높은 신뢰성을 갖는 반도체 장치를 얻을 수 있다.

Accordingly, in the boundary face of the Si layer and the Si 1-x- y Ge x C y layer in which the composition r atio y of C is 0·01~0.03, it is possible to form the carri er accumulation layer confining the carrier to two dime nsional but form the necessary band discontinuity part. And this carrier accumulation layer functions as the ch annel. Therefore the field effect transistor in which the working speed of having the Si 1-x- y Ge x C y layer gi ving the carrier mobility which is greater than the Si lay er as the channel is large can be obtained. Moreover, t here is no lattice mismatch or it can control between t he Si 1-x- y Ge x C y layer and Si layer or in order to b e very small. Therefore the lattice distortion can be co ntrolled in order to there be nearly no as 0 and it is pos sible to configure so that the crystal defect is not intro duced to the Si 1-x- y Ge x C y layer. Therefore, the s emiconductor device for having the elevated reliability can be obtained.

청구항 2에 기재된 바와 같이, 상기 Si1-x-yGexCy 층의 각 원소의 조성비를, 상기 Si1-x-yGexCy 층과 상기 Si 층 이 격자 정합하는 조성비로 조정해 놓을 수 있다.

As shown in it is written in claim 2 the composition ratio of each element of the Si 1-x- y Ge x C y layer is controlled as the Si 1-x- y Ge x C y layer and the comp osition ratio which the Si layer this lattice-matches.

이에 따라, 격자 부정합에 기인하는 왜곡이 없는 Si1-x-yGexCy 층 내에 채널이 형성되기 때문에, 매우 높은 신뢰성을 갖는 반도체 장치를 얻을 수 있게 된다.

Accordingly, the channel is formed within the Si 1-x- y Ge x C y layer without the distortion caused by the latt ice mismatch. Therefore the semiconductor device for very having the elevated reliability can be obtained.

청구항 3에 기재된 바와 같이, 상기 Si1-x-yGexCy 층을 상기 Si 층보다 작은 격자 정수를 갖고 또한 격자 완화를 발생하지 않는 막 두께를 갖는 것으로 할 수가 있다.

As shown in it is written in claim 3 with it has the lattice constant smaller than the Si layer the Si 1-x- y Ge x C y layer and it has the film thickness which is not generated moreover, the lattice mismatch distortion it can do.

이에 따라, Si1-x-yGexCy 층에는 인장 왜곡이 가해지기 위해서, Si 층과의 밴드의 불연속량을 크게 할 수 있어 캐리어의 폐쇄 효율이 향상된다.

Accordingly, in the Si 1-x- y Ge x C y layer, in order that the tensile distortion is applied the discontinuous quantity of the band with the Si layer can be done and the closure efficiency of the carrier is improved.

청구항 4에 기재된 바와 같이, 상기 반도체 기판 상에 형성되어 단일 조성의 반도체층을 채널 영역으로 하는 M0S 트랜지스터를 추가로 구비할 수 있다.

As shown in it is written in claim 4 the MOS transistor which is formed on the semiconductor substrate and ha s the semiconductor layer of the single composition as the channel region can be additionally included.

청구항 5 및 6에 기재된 바와 같이, 상기 캐리어 축적층에 축적되는 캐리어를 부의 캐리어로 할 수 있다.

As described in claim 5 and 6, the carrier accumulated in the carrier accumulation layer can be appointed as t he carrier of the part.

청구항 7~9에 기재된 바와 같이, 상기 Si 층내의 상기 Si1-x-yGexCy 층에 근접한 영역에 상기 캐리어 축적층에 캐리어를 공급하기 위한 캐리어 공급층을 설치하여 두는 것이 바람직하다.

As described in claim 7~9, it is the be desirable to set up the carrier supply layer for supplying the carrier to t he carrier accumulation layer in the domain near to the Si 1-x- y Ge x C y layer within the Si layer.

GF Exhibit 1124 - 2052/2704

청구항 10에 기재된 바와 같이, 상기 캐리어 축적층에 축적되는 캐리어를 부의 캐리어로 하고, 상기 반도체 기판의 타부에 형성되어 게이트 전극과 소스#183#드레인 영역과 해당 소스#183#드레인 영역사이의 채널 영역을 갖는 또 1개의 전계 효과 트랜지스터를 추가로 설치하여, 상기 또 1개의 전계 효과 트랜지스터의 채널 영역에 제 2 Si 층과 ,상기 제 2 Si 층에 근접하여 형성된 SiGe 층을 설치하여, 상기 SiGe 내에서의 상기 제 2 Si 층에 근접한 영역에 정의 캐리어를 축적하기 위한 제 2 캐리어 축적층을 형성해 두는 것이 바람직하다.

As shown in it is written in claim 10 the carrier accumulated in the carrier accumulation layer is appoin ted as the carrier of the part and one field effect transi stor which is formed in the other part of the semicondu ctor substrate and has the channel region between the gate electrode and the source · drain region and corres ponding source · drain region is additionally set up and the SiGe layer coming close to the second Si layer and, second Si layer and is formed in the channel region of o ne field effect transistor is set up with the above and i t is the be desirable to form the second carrier the acc umulation layer for accumulating the definition carrier in the domain near to the second Si layer within the SiGe.

이에 따라, n-채널측 및 p-채널측 중 어느 하나에서도 높은 캐리어 이동을 갖는 HCMOS 장치로서 기능하는 반도체 장치를 얻을 수 있다.

Accordingly, the semiconductor device for functioning as the HCMOS apparatus for having the high carrier mo vement at any one of n-channel and p-channel can be obtained.

청구항 11에 기재된 바와 같이, 상기 Si1-x-yGexCy 층을 양자 우물 영역으로 할 수 있다.

As shown in it is written in claim 11 the Si 1-x- y Ge x C y layer can be to the quantum-well gain region.

청구항 12에 기재된 바와 같이, 상기 SiGe 층을 양자 우물 영역으로 할 수 있다.

As shown in it is written in claim 12 the SiGe layer can be to the quantum-well gain region.

청구항 11 또는 12에 의해, 캐리어의 폐쇄 효율이 높은 채널을 갖는 전계 효과형 트랜지스터를 얻을 수 있다.

Using claim 11 or 12, the field effect transistor having the channel in which the closure efficiency of the carri er is high can be obtained.

청구항 13~16에 기재된 바와 같이, 상기 소스#183#드레인 영역에 제 1 반도체층과, 이 제 1 반도체층보다도 큰 밴드 갭을 갖는 제 2 반도체층을 설치하여, 상기 제 1 반도체층의 바로 위에 형성된 저저항의 도체막으로 이루어지는 소스#183#드레인 콘택트층을 구비할 수 있다.

As described in claim 13~16, the source · drain contact layer consisting of the first semiconductor laye r in the source · drain region, and the conductor film of the low resistance can be included. The conductor film of the low resistance sets up the second semiconducto r layer having the band gap which is greater than this f irst semiconductor layer and is formed in the first semic onductor layer, immediately, the upper part.

이에 따라, 각 청구항의 작용 효과에 덧붙여 헤테로 접합을 이용하면서 콘택트 저항이 작은 반도체 장치를 얻을 수 있다.

Accordingly, moreover while the heterojunction is used for the functional effect of each claim the semiconduct or device in which the contact resistance is small can be obtained.

본 발명의 제 2 반도체 장치는, 청구항 17에 기재된 바와 같이, 반도체 기판의 일부에 형성되어, 게이트 전극과 소스#183#드레인 영역과 이 소스#183#드레인 영역사이의 채널 영역을 갖는 전계 효과 트랜지스터를 구비하고, 상기 채널 영역에는, 제 1 Si 층과, 상기 Si 층에 접하여 형성된 제 1 Si1-x-yGexCy 층 (0#8804#x#8804#1,0y#8804#1)과, 제 2 Si 층 및 상기 제 2 Si 층 것에 접하여 형성되고 상기 제 1 Si1-x-yGexCy 층과는 다른 밴드 갭을 갖는 제 2 Si1-x-yGexCy 층(0#8804#x#8804#1, 0#8804#y#8804#1)이 설치되어, 상기 제 1 Si1-x-yGexCy 층 안에서의 상기 제 1 Si 층에 근접한 영역과, 상기 제 2 Si1-x-yGexCy 층 안에서의 상기 제 2 Si 층에 근접한 영역과는 서로 다른 도전형의 캐리어를 폐쇄하기 위한 제 1 및 제 2 캐리어 축적층이 각각 형성되어 있다.

The second semiconductor device of the invention first and second carrier accumulation layer for closing is for med respectively the carrier of the domain, which come s close to the first Si layer at the first Si 1-x- y Ge x C y inside layer second Si 1-x- y Ge x C y layers (0≤x≤1, 0≤y≤1) are installed and the domain near to the secon d Si layer at the second Si 1-x- y Ge x C y inside layer and different conductivity type having the band gap w hich includes the field effect transistor and it contacts to the first Si layer, and first Si 1-x- y Ge x C y layers (0≤x≤1,0y≤1),s contacting to the Si layer and are form ed and the second Si layer and the second Si layer and it is formed in the channel region and is different from t he first Si 1-x- y Ge x C y layer that has the channel r egion between the gate electrode and the source · drai n region and this source · drain region it is formed to th e part of the semiconductor substrate it is written in cl aim 17.

이에 따라, 각각 캐리어의 폐쇄 효율이 높은 채널을 갖고 또한

Accordingly, the semiconductor device for functioning

GF Exhibit 1124 - 2053/2704

동작 속도가 큰 n-채널 전계 효과 트랜지스터 및 p-채널 전계 효과 트랜지스터를 구비한 HCMOS 장치로서 기능하는 반도체 장치를 얻을 수 있다. 더구나, 제 1 Si1-x-yGexCy 층과 제 1 Si 층의 사이에서는 격자 부정합이 없게 되거나 또는 매우 적게 되도록 제어할 수 있기 때문에, 제 1 Si1-x-yGexCy 층에 결정 결함이 도입되지 않도록 구성하는 것이 가능하다. 따라서, 높은 신뢰성을 갖는 반도체 장치를 얻을 수 있다.

as the HCMOS apparatus having the channel in which t he closure efficiency of the carrier is high and includes the n-channel field effect transistor and the p-channel electric field effect transistor in which moreover, the w orking speed is large can be obtained. Moreover, in the interval of the first Si layer and the first Si 1-x- y Ge x C y layer, there is no lattice mismatch or it can control in order to be very less. Therefore it is possible to confi gure so that the crystal defect is not introduced to the first Si 1-x- y Ge x C y layer. Therefore, the semicondu ctor device for having the elevated reliability can be ob tained.

청구항 18에 기재된 바와 같이, 상기 제 2 Si1-x-yGexCy 층에 있어서의 C의 조성비 y를 0으로 할 수 있다.

As shown in it is written in claim 18 the composition ratio y of C in the second Si 1-x- y Ge x C y layer can be done to 0.

청구항 l9에 기재된 바와 같이, 상기 반도체 기판 상에 형성되어, 단일 조성의 반도체층을 채널 영역으로 하는 M0S 트랜지스터를 추가로 설치하여도 된다.

As shown in it is written in claim l9 it is formed on the semiconductor substrate and the MOS transistor havin g the semiconductor layer of the single composition as the channel region is additionally set up.

이에 따라, 동작 속도가 요구되는 부분에는 상기 제 1 Si1-x-yGexCy 층을 채널 영역으로 갖는 트랜지스터를 배치하고, 그 이외의 부분에서는 통상의 M0S 트랜지스터를 배치하여 반도체 장치의 응용범위를 확대시킬 수 있다.

Accordingly, in the part in which the working speed is required, the first Si 1-x- y Ge x C y layer the transisto r having is arranged to the channel region and the nor mal MOS transistor is arranged and the scope of applic ation of the semiconductor device can be enlarged in t he part of the except.

청구항 20에 기재된 바와 같이, 상기 제 1 Si1-x-yGexCy 층에 있어서의 C의 조성비 y를, 0.01~0.03으로 하는 것이 바람직하다.

As shown in it is written in claim 20 it is the be desirable to have the composition ratio y of C in the fir st Si 1-x- y Ge x C y layer as 0.01~0.03.

청구항 21에 기재된 바와 같이, 상기 제 1 Si1-x-yGexCy 층의 각 원소의 조성비를 상기 제 1 Si1-x-yGexCy 층과 상기 제 1 Si 층이 격자 정합 하는 조성비로 조정해 두는 것이 바람직하다.

As shown in it is written in claim 21 it is the be desirable to control the composition ratio of each elem ent of the first Si 1-x- y Ge x C y layer as the composi tion ratio in which the first Si 1-x- y Ge x C y layer and the first Si layer lattice-match.

이에 따라, 격자 왜곡이 없는 신뢰성이 높은 전계 효과형 트랜지스터를 갖는 반도체 장치를 얻을 수 있다.

Accordingly, the semiconductor device for having the field effect transistor in which the reliability without th e lattice distortion is high can be obtained.

청구항 22에 기재된 바와 같이, 상기 제 1 Si1-x-yGexCy 층을 상기 제 1 Si 층의 격자 정수보다 작은 격자정수를 갖고 또한 격자 완화를 일으키지 않는 막 두께를 갖는 것으로 할 수가 있다.

As shown in it is written in claim 22 with it has the lattice constant smaller than the lattice constant of th e first Si layer the first Si 1-x- y Ge x C y layer and it h as the film thickness which does not cause moreover, t he lattice mismatch distortion it can do.

이에 따라, 제 1 Si1-x-yGexCy 층에는 인장 왜곡이 가해지기 때문에 제 1 Si 층과의 사이의 밴드 불연속량을 크게 할 수 있어 캐리어의 폐쇄 효율이 향상된다.

Accordingly, in the first Si 1-x- y Ge x C y layer, because the tensile distortion is applied the band disco ntinuity amount between the first Si layer can be done and the closure efficiency of the carrier is improved.

청구항 23에 기재된 바와 같이, 상기 제 1 캐리어 축적층에 축적되는 캐리어를 부의 캐리어로 하고, 상기 제 2 캐리어 축적층에 축적되는 캐리어를 정의 캐리어로 하는 것이 바람직하다.

As shown in it is written in claim 23 the carrier accumulated in the first carrier accumulation layer is ap pointed as the carrier of the part and it is the be desira ble to appoint the carrier accumulated in the second c arrier the accumulation layer as the definition carrier.

청구항 24 및 25에 기재된 바와 같이, 상기 제 1 Si 층 내에서의 상기 제 1 Si1-x-yGexCy 층에 근접한 영역에 상기 제 1 캐리어 축적층에 캐리어를 공급하기 위한 캐리어 공급층을 추가

It as described in claim 24 and 25 is the be desirable to additionally form the carrier supply layer for supplying t he carrier to the first carrier accumulation layer on the

GF Exhibit 1124 - 2054/2704

로 형성하는 것이 바람직하다.

domain near to the first Si 1-x- y Ge x C y layer within the first Si layer.

청구항 26에 기재된 바와 같이, 상기 제 1 및 제 2 Si1-x-yGexCy 층 내 적어도 어느 한쪽의 Si1-x-yGexCy 층은 양자 우물 영역으로 되는 것이 바람직하다.

As shown in it is written in claim 26 it is the be desirable that the Si 1-x- y Ge x C y layer of first and second Si 1-x- y Ge x C y layer my at least Chinese race consists of the quantum-well gain region.

청구항 27~29에 기재된 바와 같이, 상기 제 1 및 제 2 Si1-x-yGexCy 층 중 위쪽에 형성된 Si1-x-yGexCy 층의 바로 위에 형성된 저저항의 도체막으로 이루어지는 소스#183#드레인 콘택트층을 추가로 구비하는 것이 바람직하다.

As described in claim 27~29, it is the be desirable to additionally include the source · drain contact layer consisting of the conductor film of the low resistance formed in the Si 1-x- y Ge x C y layer, formed in the upside among first and second Si 1-x- y Ge x C y layer immediately, the upper part.

본 발명의 제 3 반도체 장치는, 청구항 30에 기재된 바와 같이, 반도체 기판 상에 형성된 적어도 1개의 전계 효과 트랜지스터를 구비한 반도체 장치에 있어서, 상기 전계 효과 트랜지스터는 Si1-x-yGexCy 층(0#8804#X#8804#1,0#8804#y#8804#1)을 포함하는 제 1 반도체층, 상기 제 1 반도체층과는 밴드 갭이 다른 반도체에 의해 구성되는 제 2 반도체층 및 상기 제1, 제 2 반도체층 사이의 경계면 부근의 영역에 형성된 캐리어 축적층을 갖는 채널 영역과, 제 3 반도체층 및 이 제 3 반도체층보다도 밴드 갭이 큰 반도체층으로 구성되는 제 4 반도체층을 갖는 소스#183#드레인 영역과, 상기 제 3 반도체층의 바로 위에 형성된 저저항의 도체막으로 이루어지는 소스#183#드레인 콘택트층을 구비하고 있다.

The third semiconductor device of the present invention comprises the first semiconductor layer in which as shown in it is written in claim 30 the field effect transistor includes Si 1-x- y Ge x C y layers (0≤X≤1,0≤y≤1) as to the semiconductor device equipped with at least one field effect transistor formed on the semiconductor substrate, the first semiconductor layer and the source · drain contact layer consisting of the conductor film of the low resistance formed in the channel region, having the carrier accumulation layer formed in the second semiconductor layer and the first which the semiconductor in which the band gap is different is organized, and the domain of the boundary area neighborhood between the second semiconductor layer and the source · drain domain having the fourth semiconductor layer consisting of the semiconductor layer in which the band gap is greater than the third semiconductor layer and this third semiconductor layer, and the third semiconductor layer, immediately, the upper part.

이에 따라, 헤테로 접합을 이용한 캐리어 이동이 높은 요컨대 동작 속도가 높은 전계 효과 트랜지스터에 있어서의 소스#183#드레인 영역에의 콘택트 저항을 저감하는 것이 가능하게 된다.

Accordingly, it is possible to reduce the contact resistance of the source · drain region in the field effect transistor in which the working speed in which the carrier movement using the heterojunction is high is high.

청구항 31에 기재된 바와 같이, 상기 제 1 반도체층과 상기 제 3 반도체층을 공통의 제 1 반도체막에 의해 형성하고, 상기 제 2 반도체층과 상기 제 4 반도체층을 공통의 제 2 반도체막에 의해 형성하여, 상기 제 2 반도체막을 상기 제 1 반도체막의 위에 형성해 놓을 수 있다.

As shown in it is written in claim 31 the first semiconductor layer and the third semiconductor layer are formed with the first semiconductor film of common and the second semiconductor layer and fourth semiconductor layer are formed with the second semiconductor film of common and the second semiconductor film is formed on the upper part of the first semiconductor film.

청구항 32에 기재된 바와 같이, 상기 제 1 반도체층과 상기 제 3 반도체층을 서로 다른 반도체막에 의해 형성하고, 상기 제 3 반도체층을 상기 제 1 반도체층의 위쪽에 형성하고, 상기 제 4 반도체층을 상기 제 3 반도체층의 위에 형성해 놓을 수 있다.

As shown in it is written in claim 32 the first semiconductor layer and the third semiconductor layer are formed with the different semiconductor film and the third semiconductor layer is formed on the upside of the first semiconductor layer and the fourth semiconductor layer is formed on the upper part of the third semiconductor layer.

본 발명의 제 1 반도체 장치의 제조방법은, 청구항 33에 기재된 바와 같이, n-채널 전계 효과형 트랜지스터와, p-채널 전계 효과형 트랜지스터를 갖는 반도체 장치의 제조방법으로서, 반도체 기판 상에 제 1 Si 층과, 상기 Si 층에 접함과 동시에 상기

After doing the first method for fabricating semiconductor device of the invention, is the deposition the conductor film in the upper part of the second Si layer, on claim the 33th process of as shown is written

GF Exhibit 1124 - 2055/2704

제 1 Si 층에 근접한 영역에 상기 n-채널 전계 효과형 트랜지스터의 채널로 되는 제 1 캐리어 층을 갖도록 제 1 Si1-x-yGexCy 층(0#8804#x#8804#1,0y#8804# 1)을 형성하는 제 1 공정과, 반도체 기판 상에 제 2 Si 층과, 상기 제 2 Si 층에 접함과 동시에 상기 제 1 Si1-x-yGexCy 층과는 다른 밴드 갭을 갖고, 상기 제 2 Si 층에 근접한 영역에 상기 p-채널 전계 효과형 트랜지스터의 채널로 되는 제 2 캐리어 축적층을 갖는 제 2 Si1-x-yGexCy 층(0#8804#x#8804#1,0#8804#y#8804#1)을 형성하는 제 2 공정과, 상기 제 1 및 제 2 Si1-x-yGexCy 층 중 위쪽에 위치하는 Si1-x-yGexCy 층의 위에 도체막을 퇴적한 후, 이 반도체막을 패터닝하여 상기 n-채널 전계 효과형 트랜지스터 및 p-채널 전계 효과형 트랜지스터의 게이트 전극을 각각 형성하는 제 3 공정과, 상기 각 트랜지스터의 게이트 전극을 마스크로서 상기 n-채널 전계 효과형 트랜지스터 형성 영역에는 적어도 상기 제 1 캐리어 층에 도달하는 깊이까지 n 형 불순물을, 상기 p-채널 전계 효과형 트랜지스터 형성 영역에는 적어도 상기 제 2 캐리어 축적층에 도달하는 깊이까지 p 형 불순물을 각각 도입하고, 상기 n-채널 전계 효과형 트랜지스터 및 p-채널 전계 효과형 트랜지스터의 소스#183#드레인 영역을 각각 형성하는 제 4 공정을 구비하고 있다.

in claim 33 is the n-channel field effect transistor, and the method for fabricating semiconductor device having the p-channel field effect transistor and forming first Si 1-x- y Ge x C y layers (0≤x≤1,0y≤ 1) on the domain near to the first Si layer with contacting to the first Si layer, and Si layer on the semiconductor substrate in order to have the first carrier layer which consists of the channel of the n-channel field effect transistor, and semiconductor substrate and the second process, of forming second Si 1-x- y Ge x C y layers (0≤x≤1,0≤y≤1) having the second carrier the accumulation layer consisting of the channel of the p-channel field effect transistor on the domain near to the second Si layer it has the band gap different from the first Si 1-x- y Ge x C y layer to that it contacts to the second Si layer and the Si 1-x- y Ge x C y layer positioned in the upper direction among first and second Si 1-x- y Ge x C y layer. The third process of patterning this semiconductor film and forming the gate electrode of the p-channel field effect transistor and n-channel field effect transistor, and the fourth process of introduces the p type impurity to the depth are included. The fourth process of introduces the p type impurity to the depth reaches and forming the source · drain region of the p-channel field effect transistor and n-channel field effect transistor in at least second carrier the accumulation layer in the p-channel field effect transistor formation area the n type impurity, till the depth reaching the gate electrode of each transistor at least first carrier layer as the mask in the n-channel field effect transistor formation area.

이 방법에 의해, 청구항 17의 구조를 갖는 반도체 장치가 용이하게 형성되게 된다.

Using this method, the semiconductor device for having the structure of claim 17 is easily formed.

본 발명의 제 2 반도체 장치의 제조방법은, 청구항 34에 기재된 바와 같이, Si1-x-yGexCy 층(0#8804#x#8804#1,0#8804#y#8804#1)을 포함하는 제 1 반도체층과, 상기 제 1 반도체층과는 다른 밴드 갭을 갖는 제 2 반도체층 및 상기 제 1, 제 2 반도체층의 사이의 경계면 부근의 영역에 형성된 채널로 되는 캐리어 축적층을 갖고, 전계 효과 트랜지스터로서 기능하는 반도체 장치의 제조방법으로서, 반도체 기판의 전계 효과 트랜지스터 형성 영역에 제 3 반도체층과, 이 제 3 반도체층보다 큰 밴드 갭을 갖는 제 4 반도체층을 차례로 형성하는 제 1 공정과, 상기 제 4 반도체층의 위쪽에 반도체막을 퇴적한 후, 이 도체막을 패터닝하여 게이트 전극을 형성하는 제 2 공정과, 상기 게이트 전극 양쪽에 위치하는 상기 전계 효과형 트랜지스터 형성 영역에 적어도 상기 캐리어 축적층에 도달하는 깊이까지 불순물을 도입하여 소스#183#드레인 영역을 형성하는 제 3 공정과, 상기 소스#183#드레인 영역에서의 상기 제 4 반도체층을 적어도 상기 제 3 반도체층이 노출될 때까지 에칭에 의해 제거하는 제 4 공정과, 상기 제 3 반도체층이 노출된 면 위에 저저항의 도체막으로 이루어지는 소스#183#드레인 콘택트층을 형성하는 제 5 공정을 구비하고 있다.

After doing the deposition the semiconductor film in the upside of the third process of as the method for fabricating semiconductor device which functioning, the fourth semiconductor layer having the third semiconductor layer, and the band gap which is greater than this third semiconductor layer is successively formed on the field effect transistor formation area of the semiconductor substrate, as the field effect transistor and fourth semiconductor layer the second method for fabricating semiconductor device of the invention is written in claim 34. This conductor film is patterned and the second process of forming the gate electrode, the third process of introducing the impurity and forming the source · drain region reaches in at least carrier accumulation layer in the field effect transistor formation area positioned in the gate electrode both sides, at least third semiconductor layer is the fourth process of removing with the etching until is exposed the fourth semiconductor layer at the source · drain region, and the third process of forming the source · drain contact layer which is made of the conductor film of the low resistance in over face are included. As to the third process of, the third semiconductor layer is exposed.

이 방법에 의해, 청구항 30의 구조를 갖는 반도체 장치가 용이하게 형성되게 된다.

Using this method, the semiconductor device for having the structure of claim 30 is easily formed.

청구항 35에 기재된 바와 같이, 상기 제 1 공정은 상기 제 1 및 제 3 반도체층을 공통의 제 1 반도체막으로 형성하고, 상기 제 2 및 제 4 반도체층을 공통의 제 2 반도체막으로 형성할 수 있다.

As shown in it is written in claim 35 the first process forms the first and the third semiconductor layer into the first semiconductor film of common and the second and fourth semiconductor layer can be formed into the

GF Exhibit 1124 - 2056/2704

second semiconductor film of common.

청구항 36에 기재된 바와 같이, 상기 제 1 공정의 앞에 상기 제 1 및 제 2 반도체층을 형성하는 공정을 추가로 구비하고, 상기 제 1 공정은, 상기 제 1 반도체층의 위쪽에 제 3 반도체층을 형성하도록 할 수 있다.

As shown in it is written in claim 36 the process of forming first and second semiconductor layer is addition ally included in the front of the first process and the fir st process forms the third semiconductor layer on the upside of the first semiconductor layer.

청구항 37에 기재된 바와 같이, 상기 제 4 공정은, 상기 제 3 반도체층과 상기 제 4 반도체층에 대한 에칭 선택비가 높은 에칭 조건으로 하는 것이 바람직하다.

As shown in it is written in claim 37 the fourth process is the be desirable to be done by the etching condition that the etching selectivity for the fourth semiconduct or layer and the third semiconductor layer is high.

상술한 목적 및 기타의 목적과 본 발명의 특징 및 이점은 첨부 도면과 관련한 다음의 상세한 설명을 통해 보다 분명해질 것이다.

It is evident than the following detailed explanation that the above-described purpose, the miscellaneous p urpose and characteristic and advantage of the presen t invention relate with the attached view.

(실시예)

(Embodiment)

(제 1 실시예)

(First preferred embodiment)

제 1 실시예에 의한 HCMOS 장치는,SiGe/Si 계에 C를 첨가하여 되는 SiGeC의 3원 혼합 결정계를 이용하여, 이 SiGeC 층과 Si 층을 거의 격자정합시켜, 밴드 갭 에너지의 차이로부터 헤테로 경계면에 밴드 불연속부를 형성하는 전계 효과 트랜지스터이다.

It is the field effect transistor forming the band discontinuity part on the hetero boundary face from dif ference of the HCMOS apparatus by the first preferred embodiment is the SiGe, and this SiGeC layer using the three-membered mixed crystal system, of the SiGeC ad ding C in the Si group and becomes and band gap ener gy the Si layer the nearly is grid-matched.

도 1은, 제 1 실시예에 의한 HCMOS 장치의 구조를 나타내는 단면도이다. 도 1에 도시한 바와 같이, 실리콘 기판(10)상에는,NMOS 트랜지스터와 PMOS 트랜지스터가 형성되어 있지만, 우선, NMOS 트랜지스터의 구조부터 설명한다.

Figure 1 is a cross-sectional view showing the structure of the HCMOS apparatus by the first preferre d embodiment. As shown in Figure 1, in the silicon subs trate (10) phase, the transistor and PMOS transistor ar e formed. However it illustrates from the structure of t he NMOS transistor.

NMOS 트랜지스터에 있어서, Si 기판(10)상에는 p홀(11)(고농도 p형 실리콘층)이 형성되어 있고, 또 그 위에 V족 원소가 고농도로 도핑된 #948# 도핑층 및 스페이스층을 갖는 Si 층(13n)과, SiGeC 층(14n)(C의 조성율은 1%, Ge의 조성율은 8.2%)이 차례로 형성되어 있다. 후술하는 바와 같이, 이 SiGeC 층 (14n)에서의 각 원소의 조성비는, SiGeC 층(14n)과 그 바로 아래의 Si 층(13n)이 격자정합하는 값으로 되어있다.

As to the NMOS transistor, the p hole (11) (high concentration p-type silicon layer) is formed on the Si substrate (10) and the δ doped layer in which Ⅴgroup element is doped to the high concentration and the Si l ayer (13n), having the space layer and SiGeC layer (14 n) (the composition rate of C is 1%, and the compositi on rate of the Ge is 8.2%) are successively formed in a nd, the upper part. As shown in it describes later the c omposition ratio of each element at this SiGeC layer (1 4n) consists of the value in which the SiGeC layer (14 n) and, immediately, the following Si layer (13n) lattic e-match.

이 SiGeC 층(14n)과 Si 층(13n)의 헤테로 경계면에는 도 1의 오른쪽 부분에 도시한 바와 같이, 밴드 오프셋 값 ΔEc를 갖는 전도대 Ec의 밴드 불연속부가 존재하고, 이 밴드 불연속부에 부의 캐리어인 전자를 2차원 전자가스(2 DEG)로서 폐쇄하기 위한 캐리어 축적층이 형성된다. 그리고, 이 SiGeC 층(14n) 측의 경계면 부근에 형성된 캐리어 축적층이 전자가 고속으로 주행하는 채널로 된다. SiGeC 층(14n) 내에서는, Si 층 내에 비교해서 전자의 이동도가 크고 이 NMOS 트랜지스터의 동작 속도도 크게 할 수 있다.

The hetero boundary face of the Si layer (13n) and this SiGeC layer (14n) may be provided with the carrier accumulation layer as shown in the right of fig. 1, the band discontinuity part of the condition band Ec having the band offset value ΔEc exists and for closing the ele ctron who is the carrier of the part at this band discon tinuity part as two dimensional electron gas (2 DEG). A nd for the carrier accumulation layer formed in the bou ndary area neighborhood of this SiGeC layer (14n), the electron at high speed to the driving channel. In the Si GeC layer (14n) in, it compares within the Si layer and the mobility of the electron can be large and the worki ng speed of this NMOS transistor can do.

GF Exhibit 1124 - 2057/2704

또, 이 SiGeC 층(14n) 위에, SiGe 층(15n)(Ge의 조성율은 30%, Si의 조성율은 70%)과, Si 층(17n)이 차례로 형성되고, 또 표면에는 실리콘 산화막으로 이루어지는 게이트 절연막(19n)이 형성되어 있다. 이 게이트 절연막(19n)의 아래로는 Si 층(17n)이 존재하고 있기 때문에 Si 층 (17n)의 표면을 산화하는 것만으로 결정성이 높은 게이트절연막(19n)을 용이하게 형성할 수가 있다. 게이트 절연막(19n) 위에는 게이트 전극(18n)이 형성되고, 이 게이트 전극(18n)의 양측에 위치하는 기판 내에는 소스#183#드레인층(16n)이 형성되어 있다. SiGeC 층(14n) 내에서의 전자의 주행은 게이트 전극(18n)에 인가되는 전압에 의해서 제어된다. 또, 소스#183#드레인층(16n)은, p홀(11)에 도달하는 깊이까지 형성되어 있지만, 적어도, SiGeC 층(14n)에 형성되는 채널로 되는 부분의 깊이까지 형성되면 된다.

And the surface SiGe layer (15n) (the composition rate of the Ge is 30%, and the composition rate of the Si is 70%), and Si layer (17n) are successively formed on this SiGeC layer (14n) may be provided with the gate insulating layer (19n) consisting of silicon oxide film. The gate insulating layer (19n) in which the crystallization is high can be easily formed only by oxidizing the surface of the Si layer (17n) because the Si layer (17n) down exists of this gate insulating layer (19n). The source · drain layer (16n) is formed within the substrate positioned in both sides of this gate electrode (18n) the gate electrode (18n) is formed on the gate insulating layer (19n). The driving of the electron within the SiGeC layer (14n) is controlled with the voltage applied in the gate electrode (18n). And it is formed to the depth reaching the p hole (11). However the depth is formed to the depth of the part consisting to the channel formed in at least SiGeC layer (14n).

한편, PMOS 트랜지스터는, 이상에서 설명한 NMOS 트랜지스터와 거의 같은 구조를 갖고 있다. Si 기판(10)상에는 n홀(12)(고강도 n형 Si 층)이 형성되어 있고, 또 그 위에, V 족 원소가 고농도로 도핑된 #948# 도핑층을 갖는 Si 층(13p)과, SiGeC 층 (14p)(Ge의 조성율은 8.2%, C의 조성율은 1%)이 차례로 형성되어 있다. 또, 이 SiGeC 층 (14p) 위에, SiGe 층(15p)(Ge의 조성율은 30%, Si의 조성율은 70%), Si 층(17p)이 차례로 형성되어 있다. PMOS 트랜지스터의 경우는, 캐리어가 정공으로 되지만 이 정공이 흐르는 채널은 SiGe 층(15p)과 Si 층(17p)의 경계면의 SiGe 층(15p) 측에 형성된다. 이 SiGe 층(15p)과 Si 층(17p)의 헤테로 경계면에 밴드 오프셋 값ΔEv를 갖는 가전자대의 밴드 불연속부가 존재하고, 이 불연속부에 캐리어 층이 형성된다. 따라서, SiGe 층(15p) 측의 경계면에 형성된 캐리어 축적층 채널을 정공이 주행하지만, SiGe 층(15p) 내에서도 Si 층내에 비교해서 정공의 이동도가 크기 때문에 이 PM0S 트랜지스터의 동작속도도 커진다.

In the meantime, the PMOS transistor has the NMOS transistor which in the above, it illustrates and the structure of being nearly the same. The n hall (12) (the high intensity n-type Si layer) is formed on the Si substrate (10) and the Si layer (13p), having the δ doped layer in which Ⅴgroup element is doped to the high concentration and SiGeC layer (14p) (the composition rate of the Ge is 8.2%, and the composition rate of C is 1%) are successively formed in and, the upper part. And siGe layer (15p) (the composition rate of the Ge is 30%, and the composition rate of the Si is 70%), and the Si layer (17p) are successively formed on this SiGeC layer (14p). In case of the PMOS transistor, it becomes the carrier to the hole but the channel in which this hole flows is formed to side the SiGe layer (15p) of the boundary face of the SiGe layer (15p) and Si layer (17p). The band discontinuity part of the valence band having the band offset value ΔEv exists in the hetero boundary face of the Si layer (17p) and this SiGe layer (15p) and the carrier layer is formed in this discontinuity. Therefore, the hole travels the carrier accumulation layer channel formed in the boundary face of the SiGe layer (15p). However it compares in the SiGe layer (15p) within the Si layer and the working speed of this PM0S transistor is enlarged that the mobility of the hole is large.

PMOS 트랜지스터에 있어서, Si 층(17p)의 위에는, 실리콘 산화막으로 이루어지는 게이트 절연막(19p)이 형성되어 있다. 게이트 전극(18p)의 양측에는 소스#183#드레인층(16p)이 형성되고, SiGe 층(15p)에서의 정공의 주행은 게이트 전극(18p)에 인가되는 전압에 의해 제어되고 있다.

The upper part of the Si layer (17p) as to the PMOS transistor may be provided with the gate insulating layer (19p) consisting of the silicon oxide film. In both sides of the gate electrode (18p), the source · drain layer (16p) is formed and the driving of the hole at the SiGe layer (15p) is controlled with the voltage applied in the gate electrode (18p).

또한, NMOS 트랜지스터와 PMOS 트랜지스터와의 사이는 기판에 형성된 홈을 실리콘 산화막에 의해서 매립하여 되는 트랜치(trench)분리(20)가 설정되고, 이 트랜치분리(20)에 의해서, NMOS 트랜지스터와 PMOS 트랜지스터와가, 서로 전기적으로 분리되어 있다.

Moreover, the trench (trench) separation (20) in which the interval between the NMOS transistor and the PMOS transistor reclaim the groove formed in the substrate with the silicon oxide film and which becomes is set up and the NMOS transistor and PMOS transistor tile-roofed house is electrically classified with this trench isolation (20).

또, 각 Si 층(13n, 13p),각 SiGeC 층(14p, 14n), 각 SiGe 층(15n, 15p), 각 Si 층(17n, 17p)은, 결정 성장에 의해 각각 동시에 형성되어 있다. 그리고, 각 층의 치수는, 예컨대 이하

And each Si layer (13n, 13p), each SiGeC layer (14p, 14n), each SiGe layer (15n, 15p), each Si layer (17n, 17p) is simultaneously formed by the crystal growth. An

GF Exhibit 1124 - 2058/2704

같은 치수로 할 수 있다. 단지, 반드시 이하의 치수로 한정되는 것은 아니다.

d the dimension of each layer hereinafter can do to the same dimension. Area, it is not certainly restricted to t he dimension of less than.

각 Si 층(13n, 13p)의 두께는 예를 들면 0.6#956#m 정도이고, 0~1#956#m의 범위에 있는 것이 바람직하다. 스페이스층의 두께는 예를 들면 30 nm 정도이고, 0~50nm의 범위에 있는 것이 바람직하다. 각 SiGeC 층(14p, 14n)의 두께는 3~50nm 인 것이 바람직하다. 각 SiGe 층(15n, 15p)의 두께는 5nm 정도이고, 3~5nm의 범위에 있는 것이 바람직하다. 각 Si 층 (17n, 17p)의 두께는 1nm 정도이고, 0.5~5nm의 범위에 있는 것이 바람직하다. 게이트 절연막(19n, 19p)의 두께는, 예컨대 5nm 정도이다.

The thickness of each Si layer (13n, 13p) is about for example, 0.6μm and what is in the range of 0~1μm is t he be desirable. The thickness of the space layer is ab out for example, 30 nm and what is in the range of 0~5 0nm is the be desirable. It is the be desirable that the thickness of each SiGeC layer (14p, 14n) is 3~50nm. T he thickness of each SiGe layer (15n, 15p) is about 5n m and what is in the range of 3~5nm is the be desirabl e. The thickness of each Si layer (17n, 17p) is about 1 nm and what is in the range of 0.5~5nm is the be desir able. The thickness of gate insulating layers (19n, 19p) for example are about 5nm.

또한, 게이트 전극 (18n, 18p)의 게이트 길이는 0.25#956#m, 게이트 폭은 2.5#956#m, 소스#183#드레인 영역의 폭은 1.2#956#m 정도이고, 소스#183#드레인 전극 (21n, 21p)의 콘택트 면적은, 0.5#956#m#215# 0.6#956#m 정도이다. 각 홀(13n, 13p)의 도핑 농도는 1 #215# 1O 17~1 #215# 1O18cm-3정도이고, #948# 도핑층의 도핑농도는, 1 #215# 1O18~1 #215# 1O20 cm-3정도이다.

Moreover, the gate length of gate electrodes (18n, 18p) is 0.25μm, and the gate width are the contact siz e of source · drain electrodes (21n, 21p) is about 0.5μ m× 0.6μm 2.5μm , and the width of the source · drain r egion are about 1.2μm. The doping concentration of th ruholes (13n, 13p) is about 1 × 1 O 17 ~1 × 1 O 18 c m - 3 and the doping concentration of the δ doped lay er is about 1 × 1 O 18 ~1 × 1 O 20 cm - 3 .

본 실시예에 있어서의 HCMOS 장치(HeterostructureCMOS 장치)의 특징은, SiGeC 층을 이용하는 점이다. 이 SiGeC 층은, Si, Ge, C의 각각의 조성비의 조정에 의해 밴드 갭 층 및 실리콘에 대한 격자 부정합율을 바꿀 수 있다. 여기서, 본 실시예에 있어서의 Si, Ge, C의 조성비와, 각 층의 왜곡 및 밴드 오프셋 량과의 관계에 관해서 상세히 설명하기로 한다.

The characteristic of the HCMOS apparatus (the HeterostructureCMOS apparatus) in this embodiment is the point using the SiGeC layer. This SiGeC layer can c hange the lattice unconformity rate for the silicone and band cap layer with the Si, the Ge, and the control of each composition ratio of C. Here, it particularly decide s to illustrate about the Si in this embodiment, the Ge, and the relation of the distortion of the composition rat io of C and each layer and quantity of band offset.

도 2는, 가로축에 C(탄소)의 조성비(%), 세로축에 Ge의 조성비(%)를 잡을 때에, SiGeC 층과 Si 층은 격자 부정합율(%) (Miss fit)이 변화하는 모양을 보이고 있다. 부정합율이 0인 선은, SiGeC 층과, Si 층의 격자 정수가 같은 것을 나타낸다. Ge (게르마늄)단결정의 격자정수는 Si 단결정의 격자정수보다도 크고, C(탄소)단결정의 격자정수는 Si 단결정의 격자정수보다도 작기 때문에, Ge와 C의 조성비를 조정함으로써 SiGeC 층 (14n)의 격자정수와 Si 층 (13n)의 격자정수를 일치시킬 수 있는 것이다.

Figure 2 show the SiGeC layer and the shape that the Si layer the lattice unconformity rate (%) (Miss fit) cha nges the composition ratio (%) of the Ge is caught in t he horizontal axis in the composition ratio (%) of C (car bon), and the longitudinal axis. The line in which it is th e discordance rate 0 shows that the lattice constant o f the SiGeC layer, and Si layer is the same. The lattice constant of the Ge (germanium) monocrystal is greater than the lattice constant of the Si monocrystal and th e lattice constant of C (carbon) monocrystal is smaller than the lattice constant of the Si monocrystal. Theref ore it can be conformed the lattice constant of the SiG eC layer (14n) and lattice constant of the Si layer (13 n) by controlling the composition ratio of C and Ge.

도 3은, Si, Ge, C의 3원소의 조성비에 대한 격자정합의 관계를 나타내는 특성도이다. 도 3의 3개의 꼭지점은, 각각 Si, Ge, C의 조성율이 100%(조성비가 1)인 점이고, SiGeC 층의 3원 혼합 결정계의 조성비의 조정에 의해서 Si와의 격자 부정합율이 변화하는 형태를 보이고 있다. 도 3 중 해칭 영역은 SiGeC 층에 인장 왜곡을 주는 조성비의 영역을 나타내고, 도 3 중의 실선은 SiGeC 층과 Si 층의 격자 부정합이 0 요컨대 양자가 격자 정합하기 위한 각 원소의 조성비의 조건을 나타낸다. Ge의 격자정수는 Si의 격자정수보다도 4.2% 크고, C의 격자정수는 Si의 격자정수보다도 34.3% 작기 때문에, Ge의 조성비를 C의 조성비보다도 8.2배 크게 함으로써 SiGeC 층의 격자정수를 Si 층의 격자정수에 일치시킬 수 있다.

Figure 3 is a characteristic view showing the Si, the Ge, and the relation of the lattice matching about the composition ratio of 3 element of C. The vertex of 3 of fig. 3 is the point in which the Si, the Ge, and the com position rate of C are 100 % (the composition ratio is 1) and it shows the form in which the lattice unconfor mity rate with the Si changes with the control of the c omposition ratio of the three-membered mixed crystal s ystem of the SiGeC layer. The domain of the compositi on ratio in which the hatching area gives the tensile dis tortion to the SiGeC layer is shown among fig. 3 and th e solid line among fig. 3 the lattice mismatch of the Si l ayer and SiGeC layer shows the condition of the compo sition ratio of each element in which both sides lattice-

GF Exhibit 1124 - 2059/2704

match in short. The lattice constant of the Ge is greater than the lattice constant of the Si with 4.2% and 34.3% the lattice constant of C is smaller than the lattice constant of the Si. Therefore it can be conformed the lattice constant of the SiGeC layer in the lattice constant of the Si layer by being the composition ratio of the Ge than the composition ratio of C with 8.2 times.

본 실시예에 있어서의 SiGeC 층(14n)에서는, Ge의 조성율이 8.2%(x= 0.082)이고, C의 조성율이 1%(y= 0.01)인 것으로부터, 도 3보다 Si 기판과의 격자 부정합이 0이고, SiGeC 층(14n)과 아래쪽의 Si 층(13n)은 같은 격자정수를 갖고 있는 것을 알수 있다.

In the SiGeC layer (14n) in this embodiment, the composition rate of the Ge is 8.2 % (x= 0.082) and it is the lattice mismatch with the Si substrate from than fig. 3 0 and the composition rate of C is 1 % (y= 0.01) it can know having the lattice constant in which the Si layer (13n) of the downside and SiGeC layer (14n) is the same.

다음에, 도 4는 가로축에 C의 조성비를 잡고, 세로축에 에너지 레벨을 잡은 경우에, SiGeC 층과 Si 층의 경계면에 있어서의 전도대의 밴드 오프셋 값 ΔEc 및 가전자대의 밴드 오프셋 값ΔEv가 변화하는 형태를 보이고 있다. 단지, 검은 고리형은 가전자대의 밴드 오프셋 값ΔEv이고, 흰 고리형은 전도대의 밴드 오프셋 값ΔEc를 나타내고 있다. 또한, 에너지의 원점은 전도대에 대해서는 Si의 전도대 하단의 에너지 값으로 잡고, 가전자대에 대해서는 Si의 가전자대의 상단의 에너지 값으로 잡고 있다. 또한, 도 4의 실선은 무왜곡계에 대응하며 도 4의 점선은 인장 왜곡계에 대응하고 있다.

Next, figure 4 shows the form in which it catches the composition ratio of C in the horizontal axis and in case it catches the energy level in the longitudinal axis the band offset value ΔEv of the band offset value ΔEc of the condition band in the boundary face of the SiGeC layer and Si layer and valence band change. Area, the black cyclic type is the band offset value ΔEv of the valence band and the white cyclic type shows the band offset value ΔEc of the condition band. Moreover, the origin of energy catches as the energy value of the condition band lower part of the Si about the condition band and it catches about the valence band as the energy value of the upper end of the valence band of the Si. Moreover, the dotted line of fig. 4 corresponds with the tensile distortion mutual-aid society while the solid line of fig. 4 corresponds with the distortionless mutual-aid society.

도 4에 도시하는 바와 같이, 본 실시예의 SiGeC 층 (C의 조성비가 0.0l) 및 Si 층간의 경계면에 있어서의 전도대 및 가전자대의 밴드 오프셋 값은, 각각 300 meV, 0 meV이고, SiGeC 층과 Si 층의 경계면으로서는 가전자대에는 밴드 불연속부가 없고, 전도대에만 밴드 불연속부가 형성되는 것을 알수 있다. 또한, 본 실시예의 SiGeC 층(14n)에서의 C의 조성비는 0.01이기 때문에, SiGeC 층(14n)과 Si 층(13n)은 격자정합하고 있다. 따라서, 2차원 전자 가스가 주행하는 채널이 형성되는 SiGeC 층(14n) 내에서, 아래쪽의 Si 층(13n)과의 격자 부정합에 기인하는 전위 등의 결함의 발생을 방지할 수 있다.

As shown in Figure 4, the band offset value of the condition band in the boundary face of the SiGeC layer (the composition ratio of C is 0.0l) of this embodiment and Si inter-layer and valence band the respectively are 300 meV, 0 meV and there is no band discontinuity part as the boundary face of the Si layer and SiGeC layer in the valence band and it can know that the band discontinuity part is formed in the condition band. Moreover, the composition ratio of C at the SiGeC layer (14n) of this embodiment is 0.01. Therefore the SiGeC layer (14n) and Si layer (13n) lattice-match. Therefore, two dimensional electron gas can prevent the generation of the defect including the electric potential etc. in the SiGeC layer (14n) in which the driving channel is formed caused by the lattice mismatch with the Si layer (13n) of the downside.

한편, 본 실시예에 있어서의 SiGeC 층(14n)과 Si 층(13n) 사이의 경계면에 있어서의 가전자대에는 밴드 불연속부가 없기 때문에, SiGeC 층(14n) 내에 정공을 폐쇄할 수 없다. 따라서, 정공을 캐리어로 하는 PM0S 트랜지스터의 경우는 SiGe 층(15p)과 Si 층(17p)의 헤테로 접합을 이용하고 있다. SiGe 단결정의 격자정수는 Si 단결정의 격자정수보다 크고, 더구나, SiGe 층(15p)은 Si 층(13p)과 격자정합하고 있는 SiGeC 층(14p) 위에 위치하고 있기 때문에, 압축왜곡에 의한 밴드 구조의 변화에 의해 가전자대에서의 밴드 오프셋 값이 커지고 있다. 이 경우도 게이트로부터의 전계 인가시에 밴드 경사에 의해 정공이 2차원적으로 폐쇄되어(2DHG) 캐리어 축적층으로 된다. 따라서, SiGe 층(15p) 내의 캐리어 축적층이 정공이 고속으로 주행하기 위한 채널로 된다.

In the meantime, in the valence band in the boundary face between the SiGeC layer (14n) in this embodiment and the Si layer (13n), there is no band discontinuity part. Therefore the hole cannot be closed within the SiGeC layer (14n). Therefore, in case of the PM0S transistor appointing the hole as the carrier, the heterojunction of the Si layer (17p) and SiGe layer (15p) is used. The lattice constant of the SiGe monocrystal is greater than the lattice constant of the Si monocrystal and moreover the SiGe layer (15p) is positioned on the Si layer (13p) and the SiGeC layer (14p) lattice-matching. Therefore the band offset value at the valence band is enlarged with the change of the band structure by the compressive strain. In this case, it is closed at two dimensi

GF Exhibit 1124 - 2060/2704

onal (2DHG) and the hole is in the application of electri c field from gate to the carrier accumulation layer by t he band slope. Therefore, the carrier accumulation laye r within the SiGe layer (15p) consists of the channel in which the hole goes by boat at high speed.

이상과 같이, 본 실시예의 구조에 의하면, NMOS 트랜지스터에 있어서는, SiGeC 층(14n) 에서의 각 원소 Si, Ge, C의 조성비의 조정에 의해 전도대의 밴드 오프셋 값을 2차원 전자 가스를 축적하는데 충분한 값으로 유지하면서, SiGeC 층과 Si 층의 사이의 격자정합을 도모할 수 있다. 따라서, SiGeC 층 안에서의 2차원 전자 가스가 높은 캐리어 이동도를 이용한 동작 속도의 고속화를 실현하면서 결함밀도의 저감에 의한 높은 신뢰성을 발휘할 수가 있다. 또한, SiGeC 층(14n)과 Si 층(13n) 사이의 경계면에 있어서의 가전자대에는 밴드 불연속부가 없기 때문에, SiCeC 층(14n) 내에 정공을 폐쇄할 수 없지만, SiGe 층(15p)과 Si 층(17p)의 헤테로 접합을 이용함으로써 정공을 캐리어로서 이용하는 PM0S 트랜지스터의 채널을 형성할 수가 있어 고속동작을 실현할 수가 있다.

As described above, according to the structure of this embodiment, it is in the NMOS transistor and while two dimensional electron gas is accumulated but the band o ffset value of the condition band is maintained with en ough value with each element Si at the SiGeC layer (14 n), the Ge, and the control of the composition ratio of C the lattice matching of the interval of the SiGeC laye r and Si layer can be planned. Therefore, while the high speed of the working speed using the carrier mobility in which two dimensional electron gas at the SiGeC inside layer is high is made come true the elevated reliability by the reduction of the defect density can be exhibite d. Moreover, in the valence band in the boundary face between the SiGeC layer (14n) and the Si layer (13n), there is no band discontinuity part. Therefore the hole cannot be closed within the SiCeC layer (14n). Howeve r the channel of the PM0S transistor which uses the ho le as the carrier by using the heterojunction of the Si l ayer (17p) and SiGe layer (15p) can be built up and th e high speed operation can be realized.

그리고, 속도가 큰 NMOS 트랜지스터와 SiGe를 이용하여 가전자대의 밴드 불연속부를 형성하여 속도가 큰 PM0S 트랜지스터를 집적함으로써, 고성능인 HCMOS 장치를 실현할 수가 있다.

And the NMOS transistor in which the speed is large and the PM0S transistor which forms the band disconti nuity part of the valence band using the SiGe and in w hich the speed is large are accumulated. In that way t he HCMOS apparatus which is the high effectiveness c an be realized.

또, 본 실시예로서는, Ge의 조성율을 8.2%, C의 조성율을 1%로 하였지만, 도 4로부터 격자 정합계에서 밴드 불연속부 요컨대 밴드 오프셋 값 ΔEv가 가장 커지도록 하기 위해서는, C의 조성비를 크게 하면 되는 것을 알 수 있다. 이와 같이 큰 밴드 오프셋 값 ΔEv를 설정함으로써, 헤테로 경계면에 폐쇄된 2차원 전자 가스(2DEG)는, 전자의 농도가 높게 되더라도 헤테로 경계면을 넘는 일이 없고 안정되게 주행할 수가 있다. 특히, C의 조성비를 0.01~0.03의 범위로 조정하는 것이 바람직하다. 이 범위 내에서는, 무왜곡계 및 인장 왜곡계 중 어디에서도 2차원 전자 가스를 폐쇄하기 위한 캐리어 축적층을 형성하는데 적정한 밴드 오프셋 값 ΔEv(=-0.2~-0.6eV)를 얻을 수 있다.

And as this embodiment, the composition rate of the Ge 8.2%, and the composition rate of C was done abou t to 1%. However in order that the band offset value Δ Ev is most enlarged from fig. 4 in the lattice-match sys tem in short it can know being the composition ratio of C. In this way, the big band offset value ΔEv is set up. In that way it can go by boat to there be no work in w hich two dimensional electron gas (2DEG) closed at the hetero boundary face exceeds the hetero boundary fac e although the concentration of the electron is high an d be stabilized. Especially, it is the be desirable to cont rol the composition ratio of C as the range of 0.01~0.0 3. In this in range, the carrier accumulation layer for cl osing two dimensional electron gas in the where is form ed among the distortionless group and tensile distortion group but the proper band offset value Δ Ev (=-0.2~-0.6eV) can be obtained.

또, 본 실시예로서는, SiGe 층(15p) 에서의 Ge의 조성율을 30%로 하였지만, 밴드 오프셋 값이 가장 커지도록 Ge의 조성율을 크게 하고 압축왜곡을 크게 하여도 된다.

And as this embodiment, it had the composition rate of the Ge at the SiGe layer (15p) as 30%. However it mak es the composition rate of the Ge large so that the ban d offset value is most enlarged and the compressive str ain is a lot.

또한,HCMOS 장치는 Si 기판 상에 형성하기 때문에, 소자의 스피드가 요구되는 곳에는 이 HCMOS 장치를 이용하고, 그 이외에는 통상의 Si 단일 조성을 갖는 활성 영역 상에 형성한 CM0S 장치를 제작하여도 된다. 이와 같이 구성함으로써 Si 기판

Moreover, the apparatus forms on the Si substrate. Therefore this HCMOS apparatus is used in the place w here the speed of the device is required and the CM0S apparatus formed on the active area having the normal

GF Exhibit 1124 - 2061/2704

에 직접 제작하는 M0S 형 전계 효과 트랜지스터의 집적화도 가능하게 된다. 또, SiGeC를 이용한 장치로서는, 동일 기판 상에 p, n 형의 트랜지스터를 형성할 필요는 없다. 예컨대, 이동통신기기에 이용하는 집적 회로의 경우, 고속동작이 요구되는 고주파 영역에서 사용되는 증폭기, 믹서 등은 상보형 회로를 구성할 필요는 없기 때문에, p, n 형 중의 한 편만(예컨대 n 형)의 SiGeC를 이용한 MOS 트랜지스터로 구성하여, 상보형 회로를 구성할 필요가 있는 디지털 신호처리를 하는 부분을 Si 단일 조성을 이용한 CM0S 장치로 구성하는 것 등이 고려된다.

Si single composition in the except is made. In this way, the integration of the direct M0S type field effect transistor made is possible in the Si substrate by configuring. And as the apparatus using the SiGeC, the need to form the p, and the transistor of the n-type on the same board does not have. For example, in case of the integrated circuit used for the mobile communication unit, the need that the amplifier, the mixer etc. used in the high frequency band in which the high speed operation is required configure the complementary circuit does not have. Therefore it makes up with the MOS transistor using the p, and the SiGeC of on the other hand (for example, the n-type) among the n-type and the does the digital signal processing comprising the complementary circuit part is considered to organize the part which with the CM0S apparatus using the Si single composition.

다음에, 제 1 실시예의 HCMOS 장치의 제조방법에 관해서, 도 5의 (a)~(f)를 참조하면서 설명한다. 도 5의 (a)~(f)는 도 1에 나타내는 HCMOS 장치의 구조를 실현하기 위한 제조공정의 일례를 나타내는 단면도이다.

Next, it illustrates about the manufacturing method of the HCMOS apparatus of the first preferred embodiment with reference to (a) ~ (f) of fig. 5. It is the cross-sectional view showing an example of the manufacturing process for realizing the structure of the HCMOS apparatus which (a) ~ (f) of fig. 5 shows in fig. 1.

우선, 도의 5(a)에 나타내는 공정에서, Si 기판(10)에 p 홀(11), n 홀(12)을 이온 주입에 의해 형성한다.

First, in the process of showing for 5 (a) of drawing, the p hole (11), and the n hall (12) are formed on the Si substrate (10) with the ion implantation.

다음에, 도 5의 (b)에 나타내는 공정에서 각 홀(11,12)상에, UHV-CVD 법에 의해 #948# 도핑층을 포함하는 Si 층(13)과, SiGeC 층(14)(Ge:8.2%, C:1%)과, SiGe 층(15)과, Si 층(17)을 각각 성장시킨다. 또, #948# 도핑층 및 스페이스층도 형성되어 있지만, 보기 쉽게 하기 위해서 이것들의 층의 도시는 생략되어 있다.

Next, in the process of showing for (b) of fig. 5, with the Si layer (13), with the SiGeC layer (14) (Ge:8.2%, C:1%), with the SiGe layer (15), si layer (17) including the δ doped layer is grown on thruholes (11,12) with the UHV-CVD method. And the δ doped layer and space layer are formed. However in order to make easy to look at, the illustration of the layer of these is omitted.

다음에, 도 5의 (c)에 나타내는 공정에서, PMOS 트랜지스터, NMOS 트랜지스터를 전기적으로 분리하기 위해서, 트랜치 분리용의 홈을 형성한 후, 이 홈을 실리콘 산화막으로 매립하여 트랜치 분리(20)를 형성한다. 이 처리에 의해, Si 층 (13), SiCeC 층(14), SiGe 층(15), Si 층(17)이 각각 NMOS 트랜지스터 측의 Si 층(13n), SiGeC 층(14n), SiGe 층(15n), Si 층(17n)과, PMOS 트랜지스터 측의 Si 층(13p), SiGeC 층(14p), SiGe 층(15p), Si 층(17p)과 분리된다. 또, Si 층(17n, 17p)의 표면을 산화하여 게이트 절연막(19n, 19p)을 각각 형성한다.

Next, in the process of showing for (c) of fig. 5, in order that the PMOS transistor, and the NMOS transistor are electrically separated after it grooves for the trench isolation the groove is reclaimed as the silicon oxide film and the trench isolation (20) is formed. Using this processing, the Si layer (13), the SiCeC layer (14), the SiGe layer (15), the Si layer (17) is separated from the Si layer (13p) of the Si layer (13n), the SiGeC layer (14n), the SiGe layer (15n), with the Si layer (17n), the PMOS transistor of the NMOS transistor, the SiGeC layer (14p), the SiGe layer (15p), and the Si layer (17p). And the surface of Si layers (17n, 17p) is oxidized and gate insulating layers (19n, 19p) are formed.

다음에, 도 5의 (d)에 나타내는 공정에서 기판의 전면 상에 폴리실리콘막을 퇴적한 후, 이것을 패터닝하여 NMOS 트랜지스터 및 PMOS 트랜지스터의 각 게이트 절연막(19n, 19p) 위에 게이트 전극(l8n, 18p)을 각각 형성한다. 그 후, 각 게이트 전극(18n, 18p)을 마스크로서 NMOS 트랜지스터 측에는 인 이온(P+)의 주입에 의해 소스#183#드레인 영역(16n)을 형성하고, PM0S 트랜지스터 측에는, 붕소 이온(B+)의 주입에 의해 소스#183#드레인 영역(16p)을 각각 형성한다. NMOS 트랜지스터의 소스#183#드레인 영역(16n)의 깊이는 적어도 SiCeC 층(14n) 내의 캐리어 축적층보다도 깊으면 되고, PMOS 트랜지스터의 소스#183#드레인 영역(l6p)의 깊이는, 적어도 SiGe 층(15p) 내의 캐리어 축적층보다 깊으면 된다. 이것은, SiGeC 층(14n), SiGe 층 (15p) 내의 각 캐리어 축적층에 채널

Next, in the process of showing for (d) of fig. 5, this the poly-silicon layer is patterned after doing the deposition and gate electrodes (l8n, 18p) are formed on the front of the substrate on each gate insulating layer (19n, 19p) of the PMOS transistor and NMOS transistor. Thereafter, in the NMOS transistor as the mask each gate electrode (18n, 18p), the source · drain region (16n) is formed with the injection of the phosphor ion (P+) and the source · drain region (16p) is formed in the PM0S transistor with the injection of the boron ion (B+). The depth of the source · drain region (16n) of the NMOS transistor becomes if it is deep than the carrier accumulation layer within at least SiCeC layer (14n) and the depth of the source · drain region (l6p) of the PMOS transi

GF Exhibit 1124 - 2062/2704

이 형성되기 때문이다.

stor becomes if it is deep than the carrier accumulation layer within at least SiGe layer (15p). As to this, the c hannel is due to be formed in the SiGeC layer (14n), an d each carrier accumulation layer within the SiGe layer (15p).

다음에, 도 5의 (e)에 나타내는 공정에서, 게이트 절연막(19n, 19p) 중 소스#183#드레인 영역(16n, 16p)의 위쪽의 부분에 개구를 형성하여, 도 5의 (f)에 나타내는 공정에서, 게이트 절연막(19n, 19p)의 개구에 소스#183#드레인 전극(21n, 21p)을 각각 형성한다.

Next, in the process of showing for (e) of fig. 5, the opening is formed on the part of the upside of source · drain regions (16n, 16p) among gate insulating layers (19n, 19p) and source · drain electrodes (21n, 21p) are formed on the opening of gate insulating layers (19n, 19p) on the process of showing for (f) of fig. 5.

이에 따라, S i 기판(10) 위에 NMOS 트랜지스터, PMOS 트랜지스터로 이루어지는 HCMOS 장치가 형성된다.

Accordingly, the HCMOS apparatus for being made of the NMOS transistor on the Si substrate (10), and PMO S transistor is formed.

이와 같이, 본 실시예의 제조방법에 의하면, NMOS 트랜지스터, PMOS 트랜지스터에서 다른 채널을 형성해야 하지만, 결정 성장은 NM0S 트랜지스터, PM0S 트랜지스터에 공통으로 할 수 있어 간단히 제조할 수가 있다.

In this way, according to the manufacturing method of this embodiment, the dissimilar channel has to be forme d on the NMOS transistor, and the PMOS transistor. Ho wever the crystal growth commonly can do and can ma nufacture the NM0S transistor, and the PM0S transisto r.

(제 2 실시예)

(The second preferred embodiment)

상술한 제 1 실시예로서는, SiGeC 층을 실리콘에 격자 정합시킨 것을 이용하여 전계 효과형 트랜지스터를 형성하였지만, 본 실시예에서는 결정성의 열화가 없는 범위에서 SiGeC 층에 적극적으로 왜곡을 도입하고, 이 왜곡에 의한 밴드 구조의 변화를 이용한 트랜지스터로 하는 것이다. 본 실시예에 의한 HCMOS 장치의 구조는 기본적으로는, 도 1에 나타내는 제 1 실시예에 의한 PM0S 트랜지스터, NMOS 트랜지스터를 1개의 트랜지스터 내에 실현한 구조로 되어 있다.

As the above-described first preferred embodiment, the field effect transistor was formed by using grid-matchin g the SiGeC layer in the silicone. However in the presen t preferred embodiment, the distortion is actively introd uced in the range without the deterioration of the crys tallization to the SiGeC layer and it does to the transist or using the change of the band structure by this disto rtion. The structure of the HCMOS apparatus by this e mbodiment consists of the PM0S transistor by the first preferred embodiment which it elementarily shows for fi g. 1, and the structure of realizing the NMOS transistor within one transistor.

도 6의 (a)~(c)는, 각각 SiGeC 층에 압축왜곡을 발생시킨 경우, SiGeC 층을 Si 층에 격자 정합시킨 경우(왜곡 없슴) 및 SiGeC 층에 인장왜곡을 발생시킨 경우에 있어서의 결정 구조의 상태를 도시한 도면이다. 도 6의 (a)에 도시한 바와 같이, SiGeC 층의 격자정수를 Si 층의 격자정수보다 크게 하면 SiGeC 층에는 압축왜곡이 생겨 SiGeC 층에 있어서의 전도대의 하단과 가전자대의 상단 사이의 밴드 갭 값이 확대된다. 한편, 도 6의 (c) 에 도시한 바와 같이 SiGeC 층의 격자정수를 Si 층의 격자정수보다 작게 하면 SiGeC 층에는 인장왜곡이 생겨 SiGeC 층에 있어서의 전도대의 하단과 가전자대의 상단 사이의 밴드 갭이 축소된다. 즉, SiGeC 층의 왜곡에 의해 밴드 구조가 변화하기 때문에 이 효과를 적극적으로 이용함으로써 SiGeC 층에 근접하는 Si 층 등의 층의 밴드 오프셋 값을 변경할 수가 있다.

In case (a) ~ (c) of fig. 6 generates the compressive strain in the SiGeC layer it is drawing showing the state of the crystalline structure (a) ~ (c) of fig. 6 has in ca se of generating the tensile distortion in (it there is no with distortion) and SiGeC layer in case of grid-matchin g the SiGeC layer in the Si layer. If it makes greater th an the lattice constant of the Si layer, the compressiv e strain is generated in the SiGeC layer and as shown i n (a) of fig. 6, the band gap value between the upper end of the lower part of the condition band in the SiGe C layer and the valence band are the lattice constant of the SiGeC layer expanded. In the meantime, if it mak es smaller than the lattice constant of the Si layer, the tensile distortion is generated in the SiGeC layer and as shown in (c) of fig. 6, the band gap between the upper end of the lower part of the condition band in the SiGe C layer and the valence band are the lattice constant of the SiGeC layer reduced. That is, by actively using t his effect because the band structure changes with th e distortion of the SiGeC layer the band offset value of the layer including the Si layer etc. can be changed co mes close to the SiGeC layer.

여기서, SiGeC 층의 격자정수를 Si 층의 격자정수로부터 벗어나게 한 경우에도 SiGeC 층의 두께를 격자 완화가 일어나지 않

Here, by being done by the extent in which the lattice mismatch distortion does not occur the thickness of th

GF Exhibit 1124 - 2063/2704

고 왜곡이 축적되는 정도로 함으로써 전위 등의 결정 결함의 발생에 기인하는 소자의 신뢰성의 저하를 효율적으로 방지할 수가 있다.

e SiGeC layer and the distortion is accumulated even in case of deviating from the lattice constant of the SiGe C layer from the lattice constant of the Si layer the de gradation of the reliability caused by the generation of the crystal defect including the electric potential etc. of the device can be efficiently prevented.

도 7의 (a), (b)는, 본 실시예에 의한 전계 효과 트랜지스터의 채널영역에서의 밴드 구조도 및 단면도이다. Si 기판의 위에 Si 층(13n)을 성장시킨 후, C의 조성비를 크게 한 SiGeC 층(14n)(Ge를 10%, C를 4%)을 성장시킴으로써, SiGeC 층(14n)에서의 밴드 갭 값은 크고, 격자정수는 작아지도록 설정할 수가 있다. 그리고, SiGeC 층(14n)의 두께를 격자완화가 일어나지 않고 왜곡이 축적되는 정도로 작게 함으로써, SiGeC 층(14n)은 인장왜곡을 받는다. 따라서, C의 조성비를 크게 하는 것에 의한 밴드 갭 값의 증대 효과에 덧붙여, SiGeC 층(14n)의 인장왜곡에 의해, SiGeC 층(14n)에서 Si 층(13n)의 경계면에 있어서의 전도대의 밴드 오프셋 값이 커져 2차원 전자 가스(2 DEG)의 폐쇄 효율이 향상한다.

(a) of fig. 7, and (b) is the band structure diagram at the channel region of the field effect transistor by this embodiment and cross-sectional view. After the Si laye r (13n) is grown in the upper part of the Si substrate t he composition ratio of C one SiGeC layer (14n) (10% t he Ge, 4% C) is grown. In that way the band gap value at the SiGeC layer (14n) is large and it can set up so t hat the lattice constant is small. And it makes small to the extent in which the lattice mismatch distortion doe s not occur the thickness of the SiGeC layer (14n) and the distortion is accumulated. In that way the SiGeC la yer (14n) receives the tensile distortion. Therefore, the band offset value of the condition band in the boundar y face of the Si layer (13n) is enlarged in the SiGeC lay er (14n) and moreover the closure efficiency of two di mensional electron gas (2 DEG) improves in the enlargin g effect of the band gap value which is according to b e the composition ratio of C with the tensile distortion of the SiGeC layer (14n).

또, SiGeC 층(14n)은 격자 완화되지 않기 때문에 표면의 격자정수는 Si 층 (13n)의 격자정수에 일치하고 있다. 따라서, SiGeC 층(14n)의 위에 SiGe 층(15p)을 성장시키면 SiGe 층(15p)의 격자정수가 Si 층(13n)의 격자정수보다 커지기 때문에 SiGe 층(15p)은 압축왜곡을 받는다.

And the lattice constant of the surface coincides with the lattice constant of the Si layer (13n) because the SiGeC layer (14n) is not the lattice mismatch distortio n. Therefore, if the SiGe layer (15p) is grown in the up per part of the SiGeC layer (14n), because the lattice constant of the SiGe layer (15p) is enlarged than the la ttice constant of the Si layer (13n) the SiGe layer (15 p) receives the compressive strain.

따라서, 본 실시예에 의한 반도체 장치에 의하면, SiGeC 층(14n)에 인장왜곡, SiGe 층(15p)에 압축왜곡이 도입됨으로써, SiGeC 층(14n)과 Si 층(13n)의 경계면에 있어서의 전도대에서의 밴드 오프셋 값을 크고 또한 SiGe 층(15p)과 Si 층(17p)의 경계면에 있어서의 가전자대에서의 밴드 오프셋 값을 크게 하고, 이 트랜지스터를 NMOS 트랜지스터로서 사용하는 경우에는 SiGeC 층(14n)에 형성되는 채널을 이용하는 한편,PMOS 트랜지스터로서 사용하는 경우에는 SiGe 층(15p)에 형성되는 채널을 이용함으로써 공통의 게이트 전극이나 소스#183 #드레인 영역을 갖으면서 채널 위치가 다른 HCMOS 장치를 형성할 수가 있다.

Therefore, according to the semiconductor device by this embodiment, the compressive strain is introduced t o the SiGeC layer (14n) by the tensile distortion, and t he SiGe layer (15p). In that way it is large and it make s moreover, the band offset value at the valence band in the boundary face of the SiGe layer (15p) and Si lay er (17p) the band offset value at the condition band in the boundary face of the SiGeC layer (14n) and Si laye r (13n) large and in case of using this transistor as the NMOS transistor the channel formed in the SiGeC layer (14n) is taken advantage of on the other hands while it has the gate electrode or the source · drain region of c ommon to that by taking advantage of the channel for med in the SiGe layer (15p) in case of using as PMOS, and the transistor the HCMOS apparatus in which the c hannel location is different can be formed.

더구나, 각 층의 두께를 적정히 설정함으로써, 격자 부정합에 의한 전위나 결함의 도입이 없고, 양호한 결정성에 의한 신뢰성이 높은 전계 효과형 트랜지스터를 갖는 HCMOS 장치를 얻을 수 있다.

Moreover, the thickness of each layer is appropriately set up. In that way there is no introduction of the elec tric potential by the lattice mismatch or the deformity and the HCMOS apparatus for having the field effect tr ansistor in which the reliability by the good crystallizati on is high can be obtained.

또, 상술한 도 4의 점선은, 본 실시예에 있어서의 SiGeC 층(14n)에 0.25%의 인장 왜곡이 가해지도록 조성을 나타내고 있다. 일반적으로, SiGeC 층에 있어서의 Ge의 조성비가 C의 조성비의 8.2배인 때에 Si 층에 격자정합하게 되므로, Ge의 조

And the above-described dotted line of fig. 4 shows the composition so that the tensile distortion of 0.25% is applied in the SiGeC layer (14n) in this embodiment. Generally, the composition ratio of the Ge in the SiGeC

GF Exhibit 1124 - 2064/2704

성비를 C의 조성비의 8.2배보다 작게 함으로써 SiGeC 층(14n)에 인장왜곡을 도입할 수가 있다. 또한, C의 조성비를 y로 하였을 때 Ge의 조성을 8.2y-0.12로 한 경우, SiGeC 층(14n)의 격자정수를 Si 층(13n)의 격자정수보다 0.25% 작게 할 수가 있다.

layer lattice-matches in the Si layer in 8.2 vane time of the composition ratio of C. Therefore the tensile distortion can be introduced to the SiGeC layer (14n) by making the composition ratio of the Ge smaller than 8.2 times of the composition ratio of C. Moreover, in case the composition of the Ge is made up to 8.2y-0.12 when being the composition ratio of C to the y it makes the lattice constant of the SiGeC layer (14n) smaller than the lattice constant of the Si layer (13n) with 0.25%.

도 4에 도시한 바와 같이, 무왜곡계의 경우와 같이 SiGeC 층(14n)과 Si 층(13n)의 경계면에서는 가전자대에는 밴드 불연속부가 없고 전도대에만 밴드 불연속이 형성되는 것을 알 수 있다. C의 조성율이 2% 이하의 경우는 전도대의 밴드 오프셋 값은 무왜곡의 경우와 거의 동일하며, C의 조성율과 Ge의 조성율의 비가 격자 정합의 조건을 만족하는 값으로부터 벗어나더라도 격자정합계와 거의 같은 소자특성을 얻을 수 있다. 이 것은, SiGeC 층(14n)을 결정 성장하는 때의 C의 조성율과

As shown in Figure 4, in the boundary face of the SiGeC layer (14n) like the case of the distortionless group and Si layer (13n), it can know that there is no band discontinuity part and the band discontinuity is formed in the condition band in the valence band. In case of the composition rate of C is 2% or less, the nearly the band offset value of the condition band is identical with the case of the distortionless and although it deviates from from the value in which the ratio of the composition rate of the composition rate of C and Ge are satisfied the condition of the lattice matching the device character which is nearly the same as that of the lattice-match system can be obtained. With the composition rate of C when this performs crystal growth of the SiGeC layer (14n).

Ge의 조성율의 제어의 면에서 본 조건에 폭을 유지시키는 것을 의미하고, SiGeC층의 결정성장을 용이하게 한다. 또, C의 조성율이 2% 이상일 경우 무왜곡의 경우와 비교하여 같은 C의 조성율에서도 밴드 오프셋 값을 크게 할 수 있다. 이것에 의해 밴드 오프셋 값을 더욱 더 크게 할 경우에도 대응할 수 있다.

It means maintaining the width in the condition looked at in the side of the control of the composition rate of the Ge and the crystal growth of the SiGeC layer is facilitated. And in case the composition rate of C is 2% or greater it compares with the case of the distortionless and the band offset value can be a lot in the composition rate of same C. According to this, it can correspond to even in case of more and more a lot a loting the band offset value.

여기에서는, SiGeC의 격자정수를 Si보다 작게 하여 사용하고 있지만, 층의 두께는 격자 완화가 일어나지 않는 왜곡이 축적되는 정도이기 때문에 전위 등의 결정 결함에 의해 소자의 신뢰성이 저하되지는 않는다.

Here, it makes smaller than the Si and the lattice constant of the SiGeC is used. However because it is the extent in which the distortion in which the thickness of the layer the lattice mismatch distortion does not occur is accumulated the reliability of the device is not lowered with the crystal defect including the electric potential etc.

(제 3 실시예)

(The third preferred embodiment)

상술한 제 1 실시예에서는, 전계 효과 트랜지스터의 채널영역에 SiGeC 층을 Si 층에 격자정합시킨 헤테로 구조를 형성하여 헤테로 경계면에 있어서의 밴드 불연속부에 전자 또는 정공을 폐쇄하여 캐리어로서 이용하였다.

In the above-described first preferred embodiment, the hetero structure of grid-matching the SiGeC layer in the Si layer was formed on the channel region of the field effect transistor and the electron or the hole was closed at the band discontinuity part in the hetero boundary face and it used as the carrier.

본 실시예에서는, 캐리어를 폐쇄하는 영역을 헤테로 경계면이 아니라 Si/SiGeC/Si 또는, Si/SiGe/Si의 구조로 양자 우물 구조를 형성하고 장벽층으로는 끼일 수 있는 양자 우물(SiGeC, SiGe)를 채널로서 동작하는 트랜지스터를 설치한다.

In the present preferred embodiment, it is not hetero boundary face but the domain isolating from all society the quantum well structure is formed into the structure of the Si / SiGeC / Si, or the Si / SiGe / Si and the transistor operating the quantum well (SiGeC, SiGe) fitting in as the channel is set up in barrier.

도 8은, 본 실시예에 의한 HCMOS 장치의 단면도이다. Si 기판(30)상에, NMOS 트랜지스터와 PMOS 트랜지스터가 형성된 CMOS 장치구조이다. 이 구조에서는, 실리콘 기판(30)상에 p홀(31) 및 n홀(32)을 설치하고 있는 점과, 그 위에 V 족

Figure 8 is a cross-sectional view of the HCMOS apparatus by this embodiment. It is the NMOS transistor and the CMOS device structure in which the PMOS transistor is formed on the Si substrate (30). In this stru

GF Exhibit 1124 - 2065/2704

원소가 고농도로 도핑된 #948# 도핑층을 갖는 제 1 Si 층(33n, 33p)을 마련하고 있는 점은, 제 1 실시예에 있어서의 도 1에 나타내는 HCMOS 장치의 구조와 동일하다. 단지, 이 제 1 Si 층(33n, 33 p) 상의 PMOS 트랜지스터, NMOS 트랜지스터의 구조는 상기 제 1 실시예의 구조와 다르다.

cture, it is identical with the structure of the HCMOS apparatus for showing for the first preferred embodiment fig. 1 to prepare for first Si layers (33n, 33p) having the δ doped layer in which Ⅴgroup element is doped in the upper part to the high concentration sets up the p hole (31) and n hall (32) on the silicon substrate (30). Area, the PMOS transistor on this first Si layers (33n, 33p) , and the structure of the NMOS transistor are different from the structure of the first preferred embodiment.

NMOS 트랜지스터에 있어서는, 제 1 Si 층(33n) 위에, 제 1 Si 층(33n)에 격자정합하는 조성을 갖는 SiGeC 층(34n)이 형성되어 있고, 또 SiGeC 층(34n) 위에 제 2 Si 층(35n)이 적층되어 있다. 본 실시예에서는, 제 1 Si 층(33n)-SiGeC 층(34n)과 제 2 Si 층(35n)에 걸치는 전도대에서, 2개의 밴드 불연속부에 의해서 좁아지는 양자 우물 영역(SiGeC 층(34n))이 존재하기 때문에, 이 양자 우물 영역인 SiGeC 층(34n)에 캐리어인 2차원 전자가스(2 DEG)를 폐쇄하기 위한 캐리어 축적층이 형성된다(도 8의 오른쪽의 밴드 도 참조). 즉, NMOS 트랜지스터의 동작시에는 SiGeC 층(34n)에 채널이 형성된다. 또, 제 2 Si 층(35n) 위에, 막 두께가 작은 SiGe 층(36n)과, 제 3 Si 층(37n)이 차례로 형성되어 있다.

It is in the NMOS transistor and the SiGeC layer (34n) having the composition lattice-matching is formed in the first Si layer (33n) on the first Si layer (33n) and the second Si layer (35n) is laminated on and, the SiGeC layer (34n). In the present preferred embodiment, in the condition band spanned the first Si layer (33n) -SiGeC layer (34n) and the second Si layer (35n), the quantum-well gain region (siGeC layer (34n)) which becomes narrow with the band discontinuity part of 2 exists. Therefore the carrier accumulation layer for closing two dimensional electron gas (2 DEG) which is the carrier is formed in the SiGeC layer (34n) which is this quantum-well gain region (the band of the right of fig. 8 is the reference). That is, the channel is formed in the SiGeC layer (34n) in the operation of the NMOS transistor. And the SiGe layer (36n), in which the film thickness is small and the third Si layer (37n) are successively formed on the second Si layer (35n).

이 구조에 의해, 상기 제 1 실시예와 같이, Si 층에 비교해서 전자의 이동도가 큰 SiGeC 층(34n)에 캐리어의 이동을 위한 채널이 형성되기 때문에, 동작 속도가 큰 NMOS 트랜지스터를 얻을 수 있다. 덧붙여, 양자 우물로 되는 SiGeC 층(34n)의 막 두께가 작기 때문에 캐리어의 폐쇄 효율이 상기 제 1 실시예에 있어서의 구조보다 향상되어 혼합 결정비가 작은 계로 실현될 수 있다. 그 때문에, 혼합 결정화에 따르는 결정구조의 규칙성 악화에 기인하는 캐리어의 산란 등의 캐리어로 되는 전자의 이동도를 열화시키는 요인을 억제할 수 있다.

Using this structure, the channel for the movement of the carrier is formed in the SiGeC layer (34n) which compares like the first preferred embodiment in the Si layer and in which the mobility of the electron is large. Therefore the NMOS transistor in which the working speed is large can be obtained. Moreover, because the film thickness of the SiGeC layer (34n) consisting of the quantum well is small the closure efficiency of the carrier is improved than the structure in the first preferred embodiment and the mixed crystal ratio can be realized by the small group. Consequently, the factor degrading the mobility of the electron consisting of the carrier including the scattering of the carrier caused by the regularity deterioration followed into the mixing crystallization of the crystalline structure etc. can be suppressed.

PMOS 트랜지스터에 있어서도, 제 1 Si 층(33p) 위에 제 1 Si 층(33p)에 격자정합하는 조성을 갖는 SiGeC 층(34p)과, 제 2 Si 층(35p)과, 막 두께가 작은 SiGe 층(36p)과, 제 3 Si 층(37p)이 차례로 형성되어 있는 점은 상기 NMOS 트랜지스터의 구조와 동일하다. 단지, PMOS 트랜지스터의 경우는, 제 2 Si 층(35p)과 SiGe 층(36p) 및 제 3 Si 층(37p)에 걸치는 가전자대에 있어서, 2개의 밴드 불연속부에서 좁아지는 양자 우물 영역(SiGe 층(36p))이 존재하고, 이 양자 우물 영역에 캐리어인 정공을 2차원적으로 폐쇄하기 위한 캐리어 축적층이 형성된다. 즉, PM0S 트랜지스터의 동작시에는, SiGe 층(36p)에 채널이 형성된다. SiGe 층(36p)도 Si 층에 비교해서 정공의 이동도가 크기 때문에, 이 PM0S 트랜지스터의 동작속도도 커진다.

It is identical with the structure of the NMOS transistor as to the PMOS transistor the third Si layer (37p) is successively formed that the film thickness is small has the composition lattice-matching on the first Si layer (33p) on the first Si layer (33p). Area, in case of the PMOS transistor, the quantum-well gain region (siGe layer (36p)) which becomes narrow in the band discontinuity part of 2 exists in the second Si layer (35p), the SiGe layer (36p) and the third Si layer (37p) as to the valence band spanned and the carrier accumulation layer for closing is formed with the hole which is the carrier as two dimensional in this quantum-well gain region. That is, the operation time of the PM0S transistor may be provided with the channel in the SiGe layer (36p). The SiGe layer (36p) compares in the Si layer and the working speed of this PM0S transistor is enlarged that the mobility of the hole is large.

또, NMOS 트랜지스터, PMOS 트랜지스터에 있어서 기판 위

And gate insulating layers (39n, 39p) consisting of

GF Exhibit 1124 - 2066/2704

에는 실리콘 산화막으로 이루어지는 게이트 절연막(39n, 39p)이 형성되고, 게이트 절연막(39n, 39p) 위에는 게이트 전극(38n, 38p)이 형성되어 있다. 게이트 전극(38n, 38p)의 양측에는 소스#183#드레인 영역(42n, 42p)이 형성되고 소스#183#드레인 영역(42n, 42p) 위에는 소스#183#드레인 전극(41n, 41p)이 콘택트하고 있다. 또, 말할 필요도 없지만, NMOS 트랜지스터, PMOS 트랜지스터에 있어서, 양자 우물 영역인 SiGeC 층(34n), SiGe 층(36p) 에서의 전자, 정공의 주행은 게이트 전극(38n, 38p)에 인가되는 전압에 의해 각각 제어되고 있다.

NMOS transistor, and the silicon oxide film on the substrate as to the PMOS transistor are formed and gate electrodes (38n, 38p) are formed on gate insulating layers (39n, 39p). In both sides of gate electrodes (38n, 38p), source · drain regions (42n, 42p) are formed and source · drain electrodes (41n, 41p) contact on source · drain regions (42n, 42p). And the need to refer to does not have. However the respectively the SiGeC layer (34n), the electron at the SiGe layer (36p) , and the driving of the hole which is the quantum-well gain region are controlled as to the NMOS transistor, and the PMOS transistor with the voltage applied in gate electrodes (38n, 38p).

또한, NMOS 트랜지스터와 PMOS 트랜지스터의 사이는 분리용 홈에 실리콘 산화막을 매립하여 되는 트랜치분리(40)가 형성되어 있고, 이 트랜치분리(40)에 의하여 NMOS 트랜지스터, PMOS 트랜지스터는 서로 전기적으로 분리되어 있다.

Moreover, the trench isolation (40) in which the interval of the PMOS transistor and NMOS transistor reclaims the silicon oxide film to the isolation groove and which becomes is formed and this trench isolation (40) electrically divides the NMOS transistor , and the PMOS transistor.

본 실시예의 HCMOS 장치에 의하면, 제 1 실시예와 같이, NMOS 트랜지스터에 있어서는, Si 층에 격자정합함과 동시에 양자 우물 영역으로 되는 SiGeC 층(34n)이 형성되어 있고, 이 SiGeC 층(34n)에 전자가 주행하기 위한 채널이 형성된다. 또한, PM0S 트랜지스터에 있어서도, 양자 우물 영역으로 되는 SiGe 층(36p)이 형성되어 있고, 이 SiGe 층(36p)에 정공이 주행하기 위한 채널이 형성된다. 따라서, 캐리어 폐쇄 효율이 높은 양자 우물 구조를 이용한 스위칭 속도가 큰 NMOS 트랜지스터와 PMOS 트랜지스터를 집적함으로써 고성능인 HCMOS를 실현할 수가 있다.

According to the HCMOS apparatus of this embodiment, it is in the NMOS transistor like the first preferred embodiment, and the SiGeC layer (34n) which consists of the quantum-well gain region with lattice-matching in the Si layer is formed and the channel in which the electron goes by boat is formed in this SiGeC layer (34n). Moreover, the SiGe layer (36p) consisting of the quantum-well gain region is formed as to the PM0S transistor and the channel in which the hole goes by boat is formed in this SiGe layer (36p). Therefore, by accumulating the NMOS transistor and the PMOS transistor in which the switching speed using the quantum well structure where the carrier closure efficiency is high is large HCMOS which is the high effectiveness can be realized.

단지, 본 실시예에 있어서, 소자의 속도가 요구되는 회로에 이 HCM0S 장치를 이용하고, 그 이외의 회로에는 통상의 Si 기판 상에 형성한 CM0S 장치를 제작하여도 되고, Si 기판 상에 직접 형성한 M0S 형 전계 효과 트랜지스터의 집적도 가능하다.

Area, as to this embodiment, this HCM0S apparatus is used for the circuit in which the speed of the device is required and the CM0S apparatus formed is comprised of the circuit of the except on the normal Si substrate and the integrated of the direct M0S type field effect transistor formed is possible on the Si substrate.

또, 반드시 NMOS 트랜지스터 및 PMOS 트랜지스터의 채널의 쌍방이 양자 우물 영역으로 되어있지 않더라도 된다.

And it becomes although it does not become certainly both parties of the channel of the NMOS transistor and PMOS transistor to the quantum-well gain region.

다음에, 제 3 실시예에 의한 HCMOS 장치의 제조방법에 관해서, 도 9의 (a)~(f)를 참조하면서 설명하기로 한다. 도 9의 (a)~(f)는, 도 8에 나타내는 HCM0S 장치의 구조를 실현하기 위한 제조공정의 일례를 나타내는 단면도이다.

Next, it decides to illustrate about the manufacturing method of the HCMOS apparatus by the third preferred embodiment with reference to (a) ~ (f) of fig. 9. It is the cross-sectional view showing an example of the manufacturing process for realizing the structure of the HCM0S apparatus which (a) ~ (f) of fig. 9 shows in fig. 8.

우선, 제조공정의 개략을 설명하면, SiGeC 층(34), 제 2 Si 층(35) 및 SiGe 층(36)을 성장시킬 때, SiGeC 층(34)및 SiGe 층(36)의 막 두께를 양자 우물 구조가 되도록 10nm이하, 예컨대 3nm로 하고 있다. 그 밖의 부분은, 도 5(a)~(f)에 나타내는 공정과 거의 같은 공정으로 형성된다.

First, if the outline of the manufacturing process is explained , when the SiGeC layer (34), and the second Si layer (35) and SiGe layer (36) are grown , it has the film thickness of the SiGe layer (36) and SiGeC layer (34) as for example, 3nm less than 10nm so that the quantum well structure is. The other part is formed in Figure 5(a) the ~ (f) into the process of showing and the process of being nearly the same.

GF Exhibit 1124 - 2067/2704

우선, 도 9의 (a)에 나타내는 공정에서, Si 기판(30)에 p홀(31), n홀(32)을 이온 주입에 의해 형성한다.

First, in the process of showing for (a) of fig. 9, the p hole (31), and the n hall (32) are formed on the Si subs trate (30) with the ion implantation.

그리고, 도 9의 (b) 에 나타내는 공정에서 p홀(31), n홀(32) 상에, UHV-CVD 법에 의해 #948# 도핑층을 포함하는 제 1 S i 층(33)과, SiGeC 층 (34)(Ge:36%, C:4%)과, 제 2 Si 층(35)과, SiGe 층(36) 및 제 3 Si 층(37)을 차례로 성장시켜 간다.

And with the first Si layer (33), with the SiGeC layer (34) (Ge:36%, C:4%), with the second Si layer (35), si Ge layer (36) and the third Si layer (37) including the p hole (31) in the process of showing for (b) of fig. 9, an d the δ doped layer by the UHV-CVD method on the n hall (32) are successively grown.

다음에, 도 9의 (c)에 나타내는 공정에서, PMOS 트랜지스터, NMOS 트랜지스터를 전기적으로 분리하기 위하여 트랜치분리용 홈을 형성한 후, 이 홈을 실리콘 산화막으로 매립하여 트랜치분리(40)를 형성한다. 이 처리에 의해 제 1 Si 층(33), SiGe C 층(34),제 2 Si 층(35), SiGe 층(36),제 3 Si 층(37) 및 게이트 절연막(39)이, 각각 NMOS 트랜지스터 측의 제 1 Si 층(33n), SiGeC 층(34n), 제 2 Si 층(35n), SiGe 층(36n), 제 3 Si 층(37n) 및 PMOS 트랜지스터 측의 제 1 Si 층(33p), Si GeC 층(34p), 제 2 Si 층(35p), SiGe 층(36p), 제 3 Si 층(37p)으로 분리된다. 그 후, 제 3 Si 층(37n, 37p)의 표면을 산화하여, 게이트 절연막(39n, 39p)을 형성한다.

Next, in the process of showing for (c) of fig. 9, after it grooves the trench isolation for the PMOS transistor, and the NMOS transistor are electrically separated the groove is reclaimed as the silicon oxide film and the tre nch isolation (40) is formed. The first Si layer (33), the SiGeC layer (34), the second Si layer (35), the SiGe lay er (36), the third Si layer (37) by this processing and g ate insulating layer (39) are divided into the first Si lay er (33n), the SiGeC layer (34n), the second Si layer (3 5n), the SiGe layer (36n), the third Si layer (37n) of th e NMOS transistor and the first Si layer (33p), the SiGe C layer (34p), the second Si layer (35p), the SiGe layer (36p), the third Si layer (37p) of the PMOS transistor. Thereafter, the surface of third Si layers (37n, 37p) is oxidized and gate insulating layers (39n, 39p) are forme d.

다음에, 도 9의 (d)에 나타내는 공정에서, 게이트 전극(38n, 38p)을 형성한 후, NMOS 트랜지스터 측에는 인 이온(P+)의 주입에 의해, 소스#183#드레인 영역(42n)을 형성하고, PMO S 트랜지스터 측에는 붕소 이온(B+)의 주입에 의해, 소스#18 3#드레인 영역(42p)을 형성한다. NMOS 트랜지스터의 소스 #183#드레인 영역(42n)의 깊이는 적어도 SiGeC 층(34n)보다 깊으면 되고, PMOS 트랜지스터의 소스#183#드레인 영역(42p)의 깊이는 적어도 SiGe 층(36p)보다 깊으면 된다. 이것은, SiGeC 층(34)n, SiGe 층 (36p) 내에 채널이 형성되기 때문이다.

Next, in the process of showing for (d) of fig. 9, gate electrodes (38n, 38p) the source · drain region (42n) a re formed after doing the formation in the NMOS transis tor with the injection of the phosphor ion (P+) and the source · drain region (42p) is formed in the PMOS transi stor with the injection of the boron ion (B+). The depth of the source · drain region (42n) of the NMOS transist or becomes if it is deep than at least SiGeC layer (34n) and the depth of the source · drain region (42p) of the PMOS transistor becomes if it is deep than at least SiG e layer (36p). As to this, the channel is due to be form ed within the SiGeC layer (34) n, and the SiGe layer (3 6p).

그 다음, 도 9의 (e)에 나타내는 공정에서, 소스#183#드레인 영역(42n, 42p)의 위쪽 부분의 게이트 절연막(39n, 39p)에 개구를 형성하여, 도 9의 (f)에 나타내는 공정에서 그 개구에 소스#183#드레인 전극(41n, 41p)을 각각 형성한다.

Next, in the process of showing for (e) of fig. 9, the opening is formed on gate insulating layers (39n, 39p) of the upper section of source · drain regions (42n, 42 p) and source · drain electrodes (41n, 41p) are formed on the opening on the process of showing for (f) of fig. 9.

이상의 공정에 의해, 제 3 실시예에 의한 NMOS 트랜지스터, PMOS 트랜지스터로 이루어지는 HCMOS 장치의 구조가 실현된다.

Using the process described in the above, the structure of the HCMOS apparatus for being made of th e NMOS transistor by the third preferred embodiment, a nd PMOS transistor is attained.

본 실시예의 제조방법에 의하면, NMOS 트랜지스터의 채널을 헤테로 접합을 이용한 양자 우물 구조의 SiGeC 층(34n)으로 하고, PMOS 트랜지스터의 채널을 헤테로 접합을 이용한 양자 우물 구조의 SiGe 층(36p)으로 하는 HCMOS 장치가 용이하게 형성된다. 더구나, 본 실시예의 제조방법에 의하면, NM0S 트랜지스터, PM0S 트랜지스터에 다른 채널을 형성해야 하지만, 결정성장은 NMOS 트랜지스터, PMOS 트랜지스터에 공통으로 할 수 있어 간단히 제조할 수가 있다.

According to the manufacturing method of this embodiment, it has the channel of the NMOS transistor as the SiGeC layer (34n) of the quantum well structure of using the heterojunction and the HCMOS apparatus f or doing is easily formed with the channel of the PMOS transistor as the SiGe layer (36p) of the quantum well structure of using the heterojunction. Moreover, accor ding to the manufacturing method of this embodiment, the dissimilar channel has to be formed on the NM0S tr ansistor, and the PM0S transistor. However the crystal

GF Exhibit 1124 - 2068/2704

growth commonly can do and can manufacture the NM OS transistor, and the PMOS transistor.

(제 4 실시예)

(The fourth preferred embodiment)

도 10은, 제 4 실시예에 의한 전계 효과 트랜지스터의 구조를 나타내는 단면도이다. 본 실시예는, 헤테로 전계 효과 트랜지스터에 적합한 소스#183#드레인 콘택트를 제공하는 구조에 관한 것이다.

Figure 10 is a cross-sectional view showing the structure of the field effect transistor by the fourth pre ferred embodiment. This embodiment relates to the str ucture of providing the source · drain contact which is suitable for the hetero field effect transistor.

도 10에 도시된 바와 같이, Si 층으로 이루어지는 홀(51) 위에는, SiGe 버퍼층(52)과, #948# 도핑층(53)과, 스페이스층(54)과, n-채널층(67)과, i-Si 층(55)과, i-Si1-xGex 층(56)과, i-Si 층(57)과, 게이트 절연막(58)이 형성되어 있다. 그리고, 게이트 절연막(58) 위에 게이트 전극(65)이 형성되어, i-Si1-xGex 층(56) 중 게이트 전극(65)의 양쪽에 위치하는 영역 위에, 소스#183#드레인 콘택트 W 층(61)과 Al 소스#183#드레인 전극(63)이 차례로 형성되어 있다. 또한, 게이트 전극(65)의 양측에서 SiGe 버퍼층(52)의 일부, #948# 도핑층(53), 스페이스층(54), n-채널층(67), i-Si 층(55), i-Si1-xGex 층(56) 및 i-Si 층(57)에 걸치는 영역에, 소스#183#드레인 영역(59)이 형성되어 있다. 또, 게이트 전극(65)과 Al 소스#183#드레인전극(63)의 사이는, 제 1층의 절연막(66)에 의하여 매립되고 있다.

As shown in FIG. 10, with the SiGe buffer layer (52), with the δ doped layer (53), with the space layer (54), with the n- channel layer (67), with the i-Si layer (55), with the i- Si 1- x Ge x layer (56), with the i-Si layer (57), gate insulating layer (58) is formed on the hole (5 1) consisting of the Si layer. And the gate electrode (6 5) is formed on the gate insulating layer (58) and the s ource · drain contact W layer (61) and Al source · drai n electrode (63) are successively formed among the i- Si 1- x Ge x layer (56) on the domain positioned in both sides of the gate electrode (65). Moreover, in both sid es of gate electrode (65), the source · drain region (5 9) is formed in the part, δ doped layer (53), space laye r (54), N- channel layer (67), I-Si layer (55), I- Si 1- x Ge x layer (56) and the domain spanned on the i-Si lay er (57) of the SiGe buffer layer (52). And the interval o f the Al source · drain electrode (63) and gate electrod e (65) is reclaimed with the insulating layer (66) of the first layer.

여기서, 상기 전계 효과 트랜지스터의 각음의 구조에 관해서 설명하기로 한다.

Here, it decides to illustrate about the structure of each negative principle in nature of the field effect tra nsistor.

우선, SiGe 버퍼층(52) 내에서의 Ge의 조성율은, 위쪽으로 가면서 커지고 있다. 이 SiGe 버퍼층(52)은, SiGe 혼합결정을 격자 완화시키는 데 충분한 막 두께로 형성함으로써, Si보다 큰 격자정수를 갖고, 그 위에 왜곡 효과를 이용한 n-채널의 형성이 가능가게 된다. 또, 이러한 격자 완화시킨 SiGe 버퍼층을 이용하지 않고, Si 기판에 격자 정합시킨 상태로 Si 층과 SiGe 층의 헤테로 접합을 형성한 경우, 가전자대에는 단차가 큰 불연속부가 나타나지만, 전도대에는 불연속부는 거의 나타나지 않기 때문에, 2차원 전자 가스를 폐쇄하여 n-채널을 형성하는 것은 곤란하다.

First, the composition rate of the Ge within the SiGe buffer layer (52) is enlarged while it goes to the upsid e. As to this SiGe buffer layer (52), the key in the latti ce mismatch distortion forms the SiGe mixed crystal int o enough demag thickness. In that way it has the latti ce constant which is greater than the Si and it become s the formation of the n-channel using the distorting ef fect for the upper part with the available shop. And th e keen SiGe buffer layer in such lattice mismatch distor tion is not used and in case the heterojunction of the SiGe layer and Si layer is formed into the state grid-ma tching in the Si substrate the discontinuity in which th e stepped pulley is large shows up in the valence band. However the discontinuity does not show up in the con dition band. Therefore it is difficult to close two dimens ional electron gas and build up the n-channel.

여기서, SiGe 버퍼층 (52)중에서의 Ge의 조성율은, 예컨대 0%~30%까지 연속적으로 또는 얇은 층마다 단계적으로 변화하고 있다. 이 때, 각 층에서 격자완화를 발생시켜 버퍼층의 최상면에서 기판면 내의 격자정수가 체적이 Si0.7Ge0.3과 동일하도록 한다. 조성율을 세로방향으로 변화시키는 것은, 격자완화에 따르는 전위 등의 결정 결함이 그 위의 채널에 주는 영향을 작게 하기 때문이다. 또, SiGe 버퍼층 (52) 전체의 막 두께는 대략 1#956#m 정도 필요하다.

Here, or the composition rate of the Ge among the SiGe buffer layer (52) consecutively gradually changes to 0%~30% at the thin layer for example. Then, in eac h layer, the lattice constant within the face of the sub strate of the volume is the lattice mismatch distortion i dentical with the Si 0.7 Ge 0.3 in the top surface of th e generate and the buffer layer. The crystal defect incl uding the electric potential etc. makes the influence af fected the channel small it follows the lattice mismatch distortion to diversify the composition rate to the lengt hwise. And the film thickness of the SiGe buffer layer (52) whole approximately, 1μm gad is necessary.

GF Exhibit 1124 - 2069/2704

이 SiGe 버퍼층(52)상에 불순물을 가하지 않은 Si0.7Ge0.3으로 이루어지는 스페이스층(54)을 배치한다. 이 스페이스층(54)과 그 위의 Si 층(55)의 헤테로 경계면에 존재하는 전도대의 불연속부에 캐리어 구조를 형성하여, 이 캐리어 축적층을 2차원적으로 전자를 폐쇄하는 n-채널(67)로 한다.

The space layer (54) consisting of the Si 0.7 Ge 0.3 which does not add the impurity on this SiGe buffer layer (52) is arranged. The carrier structure is formed on the discontinuity of the condition band existing in the hetero boundary face of the si layer (55) and this space layer (54) and this carrier accumulation layer is to the n-channel (67) closing the electron at two dimensional.

#948# 도핑층(53)은 n-채널(67)에 캐리어인 전자를 공급하기 위하여 P나 As 라고 하는 V 족의 원소를 고농도로 도핑한 층이다. #948# 도핑층 (53)상의 스페이스층(54)은 불순물을 도핑하지 않은 Si0.7Ge0.3으로 구성되고, n-채널(67)의 캐리어 전자와 #948# 도핑층(53)의 이온을 공간적으로 분리함으로써, 캐리어 전자의 이온에 의한 산란을 저감하여 이동도를 향상시키는 역할을 갖는다. 이 스페이스층(54)의 막 두께는 두꺼울수록 이온화된 불순물에 의한 캐리어의 산란 효과를 저감할 수가 있지만, 반대로 캐리어 밀도가 감소하기 때문에 3 nm 정도의 두께로 하는 것이 바람직하다.

It is the layer which dopes the element of V group which does as P or the As at the high concentration so that the δ doped layer (53) supply the electron which is the carrier to the n-channel (67). The space layer (54) on the δ doped layer (53) comprises the Si 0.7 Ge 0.3 which does not dope the impurity. And the carrier electron of the n-channel (67) and ion of the δ doped layer (53) are spatially separated. In that way it has the role of reducing the scattering by the ion of the carrier electron and improving mobility. The scattering effect of the carrier by the impurity which is ionized as the film thickness of this space layer (54) is thick can be reduced. However it on the contrary is the be desirable to be done by the thickness of about 3 nm because the carrier density reduces.

i-Si1-xGex 층(56)과 i-Si 층(57)은, 헤테로 경계면에 가전자대에 단차를 형성하여 p-채널(68)을 형성하기 위해서 사용된다. X는 0.7전후로 설정하는 것이 바람직하다.

The i- Si 1- x Ge x layer (56) and i-Si layer (57) are used it forms the stepped pulley on the valence band and it forms the p-channel (68) on the hetero boundary face. It is the be desirable that X sets up as 0.7 forward and backward.

게이트 절연막(58)은 게이트 전극(65)과 그 아래의 반도체층 사이를 절연함으로써, 게이트 누설전류를 저감시켜 소자의 저소비 전력 동작을 가능하게 한다. 또, SiGe 층(56)을 산화하여 형성되는 산화막은 수용성으로 불안정한 막으로 되기 때문에, SiGe 계 전계 효과 트랜지스터에 있어서도 게이트 절열막으로서 실리콘 산화막을 이용하는 것이 바람직하다. 따라서, Si 계 헤테로 M0S 장치에 있어서는 게이트 절연막 바로 아래의 반도체층은 Si 층 인 것이 바람직하다.

The gate insulating layer (58) insulates between the gate electrode (65) and following semiconductor layer. In that way the gate leakage current is reduced and it makes the lower power operation of the device possible. And the oxide film oxidizing the SiGe layer (56) and is formed are the be desirable silicon oxide film are used as the gate isolation layer as to the SiGe group field effect transistor it consists of film which are unstable to the water-soluble. Therefore, it is in the Si group hetero M0S apparatus and it is the be desirable that the gate insulating layer, immediately, the following semiconductor layer is the Si layer.

즉, 본 실시예에 의한 전계 효과 트랜지스터는 상기의 적층막으로 이루어지는 채널영역과, 도 10의 점선으로 표시되는 소스#183#드레인 영역(59)과, 트랜지스터의 동작을 위한 전류의 도입#183#취득을 위한 Al 소스#183#드레인 전극(63)과, 전류를 제어하기 위한 전압을 인가하기 위한 게이트 전극(65)에 의해 구성되고 있다. 그리고, 이 전계 효과 트랜지스터를 n-채널 전계 효과형 트랜지스터로서 사용하는 경우에는 n-채널(67)을 형성시키도록 게이트 전극(65)에 전압을 인가하고, p-채널 전계 효과형 트랜지스터로서 사용하는 경우에는 p-채널(68)을 형성시키도록 게이트 전극(65)에 전압을 인가한다.

That is, the Al source · drain electrode (63), for the introduction · captured of the current for the operation of the channel region, consisting of the lamination film described in the above and the source · drain region (59), expressed as the dotted line of fig. 10 and transistor and the gate electrode (65) for applying the voltage for controlling the current are organized by the field effect transistor by this embodiment. And the voltage is applied in the gate electrode (65) in order to form the n-channel (67) in case of using this field effect transistor as the n-channel field effect transistor and the voltage is applied in the gate electrode (65) in order to form the p-channel (68) in case of using as the p-channel field effect transistor.

본 실시예에 의한 발명의 특징은, i-Si1-x-yGexCy 층(0#8804#x#8804#1,0#8804#y#8804#1)을 포함하는 제 1 반도체층과, 상기 제 1 반도체층과는 다른 밴드 갭을 갖는 제 2 반도체층과, 상기 제 1, 제 2 반도체층 사이의 경계면 부근

The characteristic of the invention by this embodiment is the point which includes the source · drain contact layer consisting of the source · drain domain having the fourth semiconductor layer, and the conductor film of t

GF Exhibit 1124 - 2070/2704

의 영역에 형성된 캐리어 축적층을 갖는 채널 영역과, 제 3 반도체층과, 이 제 3 반도체층보다 큰 밴드 갭을 갖는 제 4 반도체층을 갖는 소스#183#드레인 영역과, 상기 제 3 반도체층의 바로 위에 형성된 저저항의 도체막으로 이루어지는 소스#183#드레인 콘택트층을 구비하고 있는 점이다.

he low resistance formed in the third semiconductor layer, immediately, the upper part having the channel region, and the third semiconductor layer, and the band gap which is greater than this third semiconductor layer that have the formed carrier accumulation layer to the second semiconductor layer, having of the first semiconductor layer including i- Si 1-x- y Ge x C y layers (0≤x≤1,0≤y≤1) and has the band gap different from the first semiconductor layer to that and the first, and the domain of the boundary area neighborhood between the second semiconductor layer.

그리고, 본 실시예의 전계 효과 트랜지스터를 n-채널 전계 효과형 트랜지스터로서 사용하는 경우에는, i-Si 층(55)은 i-Si 1-x-yGexCy 층(0#8804#x#8804#1,0#8804#y#8804#1)을 포함하는 제 1 반도체층이고(x = y = 0), SiGe 버퍼층(52)은 제 2 반도체층이고, i-Si1-xGex층(56)은 제 3 반도체층이며 i-Si 층(57)은 i-Si1-xGex층(56)보다 밴드 갭이 큰 제 4 반도체층으로서, 제 3 반도체층인 i-Si1-xGex층(56)의 바로 위에 소스#183#드레인 콘택트 W 층(61)이 형성되어 있다.

And in case the field effect transistor of this embodiment is used as the n-channel field effect transistor it is the first semiconductor layer in which the i-Si layer (55) includes i- Si 1-x- y Ge x C y layers (0≤x≤1,0≤y≤1) and the SiGe buffer layer (52) is the second semiconductor layer and it is the fourth semiconductor layer in which the i- Si 1- x Ge x layer (56) is the third semiconductor layer and the i-Si layer (57) the band gap is greater than the i- Si 1- x Ge x layer (56) and the source · drain contact W layer (61) is formed in the i-Si 1- x Ge x layer (56), which is the third semiconductor layer (x = y = 0) immediately, the upper part.

한편, 본 실시예의 전계 효과 트랜지스터를 p-채널 전계 효과형 트랜지스터로서 사용하는 경우에는, i-Si1-xGex층(56)은 i-Si1-x-yGexCy 층(0#8804#x#8804#1,0#8804#y#8804#1)을 포함하는 제 1 반도체층인 (y= 0) 동시에 제 3 반도체층이며, i-Si 층(57)은 제 2 반도체층인 동시에 제 3 반도체층보다 밴드 갭이 큰 제 4 반도체층으로서, 제 3 반도체층인 i-Si 1-xGex층(56)의 바로 위에 소스#183#드레인 콘택트 W 층(61)이 형성되어 있다.

In the meantime, in case the field effect transistor of this embodiment is used as the p-channel field effect transistor the it is the first semiconductor layer in which the i- Si 1- x Ge x layer (56) includes i- Si 1-x- y Ge x C y layers (0≤x≤1,0≤y≤1) simultaneously is the third semiconductor layer and it is the fourth semiconductor layer in which the i-Si layer (57) is the second semiconductor layer and the band gap is greater than the third semiconductor layer at the same time and the source · drain contact W layer (61) is formed in the i- Si 1- x Ge x layer (56), which is the third semiconductor layer (y= 0) immediately, the upper part.

이상과 같이, 본 실시예에서는, A1소스#183#드레인 전극(63)의 콘택트를 하는 기판측의 영역을, 채널 형성을 위한 각 반도체층 내 밴드 갭이 작은 층에 설치되어 있다. 이 실시예의 경우, p-채널 형성용의 Si 층(57)과 i-Si1-xGex층(56)의 헤테로 경계면 중, 밴드 갭이 작은 i-Si1-xGex층(56)의 바로 위에 소스#183#드레인 콘택트 W 층 (61)을 설치하고 있다. 이에 따라, 최상층의 반도체층인 i-Si 층(57)의 바로 위에 콘택트를 설치하는 것보다 콘택트 저항이 작아지고, 소자의 저소비 전력과 고속동작이 가능하게 된다.

As described above, in the present preferred embodiment, it is the domain of the substrate side contacted of the A1 source · drain electrode (63) installed in the layer in which each semiconductor layer my band gap for the channel-forming is small. In case of this embodiment, the source · drain contact W layer (61) is set up in the i- Si 1- x Ge x layer (56), in which the band gap is small immediately, the upper part among the hetero boundary face of the Si layer (57) for the p- channel-forming and i- Si 1- x Ge x layer (56). Accordingly, the contact resistance becomes smaller than the contact is set up in the i-Si layer (57), which is the semiconductor layer of the top layer immediately, the upper part and the low dissipation and high speed operation of the device are possible.

또, Si 층상의 Si0.7Ge0.3층의 위에 W를 성장시킨 후, 금속(이 경우 Al)을 퇴적시키면, 대단히 저항이 낮은 콘택트를 얻을 수 있다. 이 SiGe 막을 이용한 콘택트는 종래의 CMOS 장치로 일반적으로 저저항 콘택트로서 이용되고 있는 실리사이드 기술을 이용한 저저항 콘택트보다 1자리수 저항값이 낮은 콘택트를 얻을 수 있다 (IEEE Electron Device Letters 지 vol. I7. No.7, I996 pp360).

And after W is grown in the upper part of the Si 0.7 Ge 0.3 layer of the Si layer if the metal (in this case, the Al) is sedimented , the contact in which the resistance is very low can be obtained. The contact in which the single digit resistance value is lower than that of the low resistance contact using the silicide technology in which generally the contact using this SiGe film is used as the conventional CMOS apparatus as the low resistance contact can be obtained (the IEEE Electron Device Letters paper vol. I7. No.7, and the I996 pp360).

GF Exhibit 1124 - 2071/2704

이 논문에서는 SiGe 층은 소스#183#드레인 전극 콘택트 형성을 위해서만 성장시켜지고 있지만, 본 실시예와 같이, 채널 형성용의 SiGe 층에 콘택트를 잡는 구조를 잡으면, 후술하는 트랜지스터 제조방법으로 분명해지는 바와 같이, 새롭게 SiGe 결정을 성장시킬 필요가 없어져 생산성이 향상된다.

In this paper, the SiGe layer grows for the source · drain electrode contact formation. However if the structure of catching the contact in the SiGe layer for the channel-forming is caught like this embodiment , as shown in it is evident to the transistor manufacturing method which will be described later it news it does not have to grow and productivity is the SiGe Decision improved.

다만, 본 실시예에 있어서, 장치의 속도가 요구되는 곳에 이 HCMOS 장치를 이용하고, 그 이외에는, 통상의 Si 기판상에 형성한 CMOS 장치를 제작하여도 되고, Si 기판상에 직접 형성한 M0S 형 전계 효과 트랜지스터의 집적이 가능하다.

But as to this embodiment, this HCMOS apparatus is used for the place where the speed of the apparatus is required and the CMOS apparatus formed is comprised of the except on the normal Si substrate and the integrated of the direct M0S type field effect transistor formed is possible on the Si substrate.

다음에, 본 실시예에 의한 전계 효과 트랜지스터의 제조방법에 관해서 설명하기로 한다. 도 11의 (a)~(e) 및 도 12의 (a)~(e)는, 도 10에 도시된 전계 효과 트랜지스터의 구조를 실현하기 위한 제조공정의 예를 나타내는 단면도이다.

Next, it decides to illustrate about the manufacturing method of the field effect transistor by this embodiment. (a) ~ (e) of (a) ~ (e) of fig. 11 and fig. 12 are the cross-sectional view showing the example of the manufacturing process for realizing the structure of the field effect transistor illustrated in Figure 10.

우선, 도 11의 (a)에 나타내는 공정에서, 채널형성의 에피텍셜 성장에 앞서서, Si 기판(50)에 이온을 주입하고, NMOS 트랜지스터, PMOS 트랜지스터의 기초가 되는 p홀(51n), 및 n홀(51p)을 형성한다.

First, in the process of showing for (a) of fig. 11, ion is injected into the Si substrate (50) before the selective epitaxial growth of the channel-forming and the NMOS transistor, and the p hole (51n) and the based n hall (51p) of the PMOS transistor are formed.

다음에, 도 11의 (b)에 나타내는 공정에서, 기판상에 에피텍셜 성장을 하기 전에, 기판에 RCA 세정법 등을 이용한 세정을 하여 표면의 불순물을 제거한다. 그 후, 표면의 산화막을 제거하고, 기판을 에피텍셜 성장장치에 삽입하여 진공상태로 가열을 하여 청정한 표면을 얻는다. 그리고, 이 청정한 표면상에 채널 영역을 형성하기 위한 반도체층의 에피텍셜 성장을 한다. 이 반도체층에는, SiGe 버퍼층(52), #948# 도핑층(53), 스페이스층(54), n-채널층(67),i-Si 층(55), i-Si1-xGex층(56), p-채널층(68), i-Si 층(57) 등이 포함된다. 단지, 보기 쉽게 하기 위하여 #948# 도핑층 (53), 스페이스층(54), n-채널층(67) 및 p-채널층(68)의 도시는 생략한다. 이하, 이 반도체층 내의 각 층의 형성순서를 설명한다.

Next, in the process of showing for (b) of fig. 11, it does and uses the RCA washing method etc. the selective epitaxial growth on the substrate for the following total for the substrate the impurity of the surface is removed. Thereafter, the oxide film of the surface is removed and the substrate is inserted into the epitaxial growth apparatus and it heats up with the vacuum condition and the pure surface is obtained. And grow epitaxially of the semiconductor layer for forming the channel region on the pure surface. This semiconductor layer includes the SiGe buffer layer (52), the δ doped layer (53), the space layer (54), the n- channel layer (67) ,i-Si layer (55), the i- Si 1- x Ge x layer (56), the p- channel layer (68), the i-Si layer (57) etc. Area, in order to make easy to look at, the δ doped layer (53), the space layer (54) , and the illustration of the p- channel layer (68) and n- channel layer (67) omit. Hereinafter, the formation order of each layer within this semiconductor layer is illustrated.

반도체층의 성장방법에 있어서는, 고체 소스를 이용하는 MBE 법이나 기체 소스를 이용하는 UHV-CVD 법 등이 이용될 수 있다. UHV-CVD 법의 경우 장치 내의 분위기를 우선 초고진공 (1O-10 Torr 정도)으로 하여 결정성장에 필요한 소스를 진공용 기내에 도입하고 나서, 1O-5~1O-6 Torr 정도의 진공도에 도달한 상태로 결정성장을 한다.

It is in the growth process of the semiconductor layer and the molecular beam epitaxy method using the solid source or the UHV-CVD method etc. can be used. Uses the gaseous source. In case of the UHV-CVD method, the first has the mood of in the apparatus as the ultra-high vacuum (about 1 O - 10 Torr) and the source required for the crystal growth is introduced to vitro for the vacuum. And yet it performs crystal growth to the state reaching the degree of vacuum of about 1 O - 5 ~1 O - 6 Torr.

따라서, 본 실시예에 있어서도, 상술한 처리에 의해 기판에 청정한 표면을 생성한 후, 진공 용기 내의 진공도가 충분히 높게 된 시점에서 기판 온도를 500~700℃ 정도로 설정하여 각 반도체 결정층의 성장을 한다. 또, 기판 온도를 변화시키면, 단일의

Therefore, the substrate temperature is set up as about 500~700℃ after doing the production in the point of time when the degree of vacuum within the vacuum container is enough high and the pure surface is gro

GF Exhibit 1124 - 2072/2704

반도체 결정층 내에서 조성비가 변화하는 등 결정의 질에 영향을 주기 위하여, 기본적으로는 단일층을 성장시키고 있는 사이는 기판 온도를 변화시키지 않는다. 또한, 800℃ 이상이라고 하는 고온에서는 Ge와 Si가 상호 확산하여 헤테로 경계면의 급준성이 손상되거나, 왜곡 완화가 행하여져 채널특성이 악화하는 등 바람직하지 못한 일이 일어나기 때문에 성장온도는 상기한 바와 같이 700℃ 이하를 선택한다.

wn as to this embodiment with the above-described pr ocessing in the substrate of each semiconductor cryst al layer. And if the substrate temperature is diversifie d , it is to affect the quality of the Decision the compo sition ratio changes in the single semiconductor crystal layer and the interval which elementarily grows the mo nolayer does not diversify the substrate temperature. Moreover, in the high temperature which it is called 80 0℃ or greater, the Ge and Si cross-disperse and the st eepness of the hetero boundary face is damaged or be cause the things could not with the be desirable paper occurs the distortion mitigation is performed and the ch annel characteristic grows worse etc as described abo ve, the growth temperature chooses 700℃ or less.

결정성장은, 초고진공 상태로 한 진공용기 내에, 결정성장에 필요한 소스가스를 도입하는 것으로 한다. 결정성장에 사용하는 소스 가스로서는 Si 층의 성장용에는 지시랜을 사용하고 있다. SiGe 층의 성장에는 지시랜등의 Si 층을 성장시키기 위한 소스 가스에 가하여, 게르마늄을 Ge의 소스가스로서 사용한다. 이 때, 각 소스가스의 분압비의 조정에 의해 SiGe 층 내의 Si와 Ge의 조성비를 제어할 수가 있다. 가스유량은 진공도가 1 O-5~1O -6Torr 정도가 되도록 조정한다.

The crystal growth does that it introduces the necessary source gas to the crystal growth within the vacuum container done to the ultra-high vacuum stat e. In the growth dragon of the Si layer as the source g as used in the crystal growth, the indication LAN is use d. In the growth of the SiGe layer, it adds to the sourc e gas for growing the Si layer including the Ji SiRaen et c. and germanium is used as the source gas of the Ge. Then, the composition ratio of the Si within the SiGe la yer and Ge can be controlled with the control of the di vision rate of each source gas. The gas flow rate contr ols so that for the degree of vacuum, about 1 O - 5 ~1 O - 6 Torr is.

우선, 조성비를 단계적으로 변화시키고 또한 격자 완화된 다수의 SiGe 층을 적층하여 SiGe 버퍼층(52)을 형성한다. 이 때, 조성비를 단계적으로 변화시키기 위하여, 상술한 바와 같이 Si의 소스가스의 분압과 Ge의 소스가스의 분압의 비를 단계적으로 변화시킨다.

First, multiple siGe layers which gradually diversify the composition ratio and become with moreover, the lattic e mismatch distortion are laminated and the SiGe buffer layer (52) is formed. Then, in order that the compositio n ratio is gradually diversified as described above, the r atio of the partial pressure of the source gas of the par tial pressure of the source gas of the Si and Ge are gra dually diversified.

다음에, #948# 도핑층(53)의 형성에는 아루신 또는 포스핀이라고 하는 도우펀트 가스를, 지시랜 및 게르마늄과 동시에 진공용기 내에 도입한다.

Next, in the formation of the δ doped layer (53), the dopant gas which it is called leucine or the phosphine i s simultaneously introduced with the indication LAN and germanium within the vacuum container.

여기서, #948# 도핑층(53)에 도입한 불순물이 스페이스층(54)에 혼합되면, 트랜지스터 특성이 열화하기 때문에, 도우펀트 가스를 진공용기 내에 도입한 후는 일단 소스가스의 공급을 멈추고, 진공도가 충분히 향상된 후에 스페이스층(54)을 성장시키기 위한 가스를 도입하여 스페이스층 (54)을 성장시킨다. 스페이스층 (54)의 조성은 균일하게 Si0.7 Ge0.3으로 하여, 지시랜과 게르마늄의 유량을 고정하여 성장시킨다.

Here, if the impurity introduced to the δ doped layer (53) is mixed in the space layer (54) , the transistor ch aracteristic degrades. Therefore first of all, after introd ucing the dopant gas within the vacuum container stop s the supply of the source gas and the gas for growing the space layer (54) after the degree of vacuum is eno ugh improved is introduced and the space layer (54) is grown. The uniformly the composition of the space laye r (54) is done by the Si 0.7 Ge 0.3 and the flow rate of germanium and indication LAN is fixed and it grows.

스페이스층(54)의 성장 후, 소스가스의 공급을 일단 정지하고 진공도가 향상되고 나서 지시랜만을 성장실에 도입하여, 불순물을 도핑하지 않은 i-Si 층(55)을 성장시킨다.

The supply of the source gas is stopped and after the degree of vacuum is improved it introduces to the incu vator after the growth of the space layer (54) only the indication LAN and the i-Si layer (55) which does not d ope the impurity is grown.

i-Si 층(55)의 성장 후, 다시 지시랜과 게르마늄을 성장실에 도입하여, i-Si1-xGex층(56)을 성장시킨다. Ge의 조성비는 7 0%으로 한다. i-Si1-xGex층(56)의 성장 후, 소스가스의 공급을 일단 정지한 후, 진공도가 향상되고 나서 지시랜만을 성장실

The indication LAN and germanium are again introduced to the incuvator after the growth of the i-Si layer (55) and the i- Si 1- x Ge x layer (56) is grown. The compos ition ratio of the Ge is done by 70%. First of all, after t

GF Exhibit 1124 - 2073/2704

에 도입하여 i-Si 층(57)을 성장시킨다.

he supply of the source gas is stopped after the growt h of the i- Si 1- x Ge x layer (56) after the degree of v acuum is improved it introduces to the incuvator only t he indication LAN and the i-Si layer (57) is grown.

이상의 처리에 의해, 채널영역을 구성하는 반도체층의 에피텍셜 성장공정은 종료한다.

Using the processing described in the above, the epitaxial growth process of the semiconductor layer co mprising the channel region terminates.

다음에, 도 11의 (c)에 나타내는 공정에서는, 기판을 UHV-CVD 장치로부터 인출하여 열산화 화로 내에 도입하여, 최상층의 i-Si 층(57)의 표면을 산화하여 실리콘 산화막으로 이루어지는 게이트 절연막(58)을 형성한다.

Next, in the process of showing for (c) of fig. 11, the substrate is drawn out from the UHV-CVD apparatus an d it introduces within the thermal oxidation furnace and the surface of the i-Si layer (57) of the top layer is oxi dized and the gate insulating layer (58) consisting of th e silicon oxide film is formed.

다음에, 도 11의 (d)에 나타내는 공정에서, 게이트 절연막(58) 상에 게이트 전극(65)을 형성한다. 이 게이트 전극의 형성법은 종래의 CM0S 장치 공정과 마찬가지다. 즉, 폴리실리콘막을 퇴적하고, 불순물을 이온 주입한 후 드라이 에칭에 의해 폴리실리콘막을 패터닝하여 게이트 전극(65n, 65p)을 형성한다. 불순물 이온으로서는 불화 붕소이온(BF2+)을 사용할 수 있다. 이 게이트 전극용의 폴리실리콘막이 퇴적된 단계에서는 소스#183#드레인 영역은 형성되지 않는다.

Next, in the process of showing for (d) of fig. 11, the gate electrode (65) is formed on the gate insulating lay er (58). The formation method of this gate electrode is the conventional CM0S instrumental process and likene ss. That is, the poly-silicon layer is accumulated and th e poly-silicon layer the impurity is patterned after doing the ion implantation with the dry etching and gate elec trodes (65n, 65p) are formed. The fluorination boron io n (BF2+) can be used as the impurity ion. In the step t hat the poly-silicon layer for this gate electrode is acc umulated, the source · drain region is not formed.

다음에, 도 11의 (e)에 나타내는 공정에서, 게이트 전극(65n, 65p)을 마스크로서, 도우펀트가 되는 불순물 이온을 기판 내에 주입하여 소스#183#드레인 영역(59n, 59p)을 형성한 후, 콘택트를 취하기 위하여 기판상에 노출되는 산화막을 제거하기 위한 에칭을 한다. 또, 이온주입인 때는, 이온의 가속전압을 불순물 분포의 피크가 소스#183#드레인 전극의 콘택트를 설치하는 것과 같이 선택한다. 주입하는 불순물이온으로서는 NMOS 트랜지스터영역에는 n 형 불순물인 비소 이온(As+) 또는 인 이온(p+)을, PMOS 트랜지스터영역에는 p형 불순물인 붕소 이온(B+)을 사용한다. 따라서, NMOS 트랜지스터의 소스#183#드레인 영역(59n)을 형성하기 위한 이온 주입과, PMOS 트랜지스터의 소스#183#드레인 영역(59p)을 형성하기 위한 이온 주입은 각각 별개의 마스크를 이용할 필요가 있다.

Next, in the process of showing for (e) of fig. 11, it is gate electrodes (65n, 65p) the features and the etchin g for removing the oxide film exposed on the substrate in order to inject the impurity ion in which the dopant i s within the substrate and take the contact source · dr ain regions (59n, 59p) after doing the formation, is don e. And as the peak of the impurity distribution set up t he contact of the source · drain electrode the time whi ch is the ion implantation chooses the acceleration volt age of ion. In the nmos transistor area as the impurity i on injected, the arsenic ion (As+) which is the n type i mpurity or the boron ion (B+) which is the phosphor ion (p+) the p-type impurity in the PMOS transistor region i s used. Therefore, the ion implantation, and the ion imp lantation for forming the source · drain region (59p) of the PMOS transistor need to use the separate mask for forming the source · drain region (59n) of the NMOS tra nsistor.

또, 이온주입 직후는, 불순물의 활성화를 위한 아닐을 행한다. 단지, 아닐 열처리에 의해 헤테로 경계면에서의 Si와 Ge의 상호 확산이나, Si/SiGe 계에 존재하는 왜곡의 완화과정에서의 결정 결함의 발생이 없도록 1OOO℃ 정도로 단시간(30초)의 RTA (Rapid thermal anylling)을 하는 것이 바람직하다.

And the ion implantation work after performs the anneal for the activation of the impurity. Area, it is the be desirable to have the RTA (Rapid thermal anylling) o f the short time (30 second) as about 1OOO ℃ with not thermal process so that there are no generation of the crystal defect at the relax process of the interdiffusion of the Si at the hetero boundary face and Ge or the dis tortion of existing in the Si / SiGe group.

다음에, 도 12의 (a)에 나타내는 공정에서, 기판상에 다시 한 번 포토 레지스터 마스크(도시 생략)를 형성하고, 드라이 에칭에 의해 NMOS 트랜지스터 형성 영역과 PMOS 트랜지스터 형성 영역 사이의 영역을 적어도 채널영역보다 깊게 들어가 소자 분리용 홈(71)을 형성한다.

Next, in the process of showing for (a) of fig. 12, the photo resister mask (figures are omitted) is again forme d on the substrate and the domain of the PMOS transis tor between formation domain and NMOS transistor for ming region is deeply entered than at least channel regi on and the element isolating groove (71) is formed with the dry etching.

GF Exhibit 1124 - 2074/2704

다음에, 도 12의 (b)에 나타내는 공정에서, 홈(71)을 포함하는 기판의 전면 상에 제 1 층 절연막(72)을 퇴적한다. 절연막을 구성하는 재료로서는 고온 처리를 피하기 위하여, 500℃ 이하로 성막되는 플라즈마 CVD 법에 의한 TEOS 막 등을 사용하는 것이 바람직하다. 이 때, 홈(71)에 매립된 절연막에 의해 트랜치분리(73)가 구성된다.

Next, in the process of showing for (b) of fig. 12, the first layer insulating layer (72) is accumulated on the front of the substrate including the groove (71). It in order to avoid the high temperature processing as the material comprising the insulating layer is the be desirable to use the tetra ethyl ortho silicate layer by the plasma CVD method which 500℃ this harrow is layered etc. Then, the insulating layer reclaimed to the groove (71) is organized by the trench isolation (73).

다음에, 본 실시예의 특징인 소스#183#드레인 콘택트 이하의 순서에 의해 형성한다. 단지, 도 10에 나타내는 구조를 실현하기 위한 공정은, 이하의 순서에 한정되는 것은 아니다.

Next, it forms with the order less than the characterized source · drain contact of this embodiment. Area, the process for realizing the structure of showing for fig. 10 is not restricted to the order of less than.

본 실시예의 효과를 최대한 발휘하기 위해서는 최종적으로 콘택트의 기초가 되는 매우 얇은 특정한 반도체층이 존재할 필요가 있다. 그 때문에, 본 실시예에서는, 기초가 되는 특정한 반도체층으로서 i-Si1-xGex층(56n, 56p)을 선택하여, i-Si1-xGex층(56n, 56p)이 노출될 때까지 에칭을 한다. i-Si1-xGex층(56n, 56p)을 노출시킬 때는 습식 에칭에 의한 선택성이 높은 에칭을 이용하는 것이 바람직하다. 단지, 습식 에칭은 다른 방향성이 결핍되고 미세 가공에 적합하지 않기 때문에 ,우선, 드라이 에칭에 의해 제 1 층의 절연막(72) 중 소스#183#드레인 전극을 형성하고자 하는 영역을 선택적으로 제거하여 컨택트 홀을 형성하고, 게이트 절연막(58n, 58p)을 노출시킨 후, 습식 에칭을 하는 것이 바람직하다. 이러한 처리의 예 로서는 예컨대 이하의 처리가 있다.

In order to to the utmost exhibit the effect of this embodiment, based very thin specific semiconductor layer of the contact need to exist. Consequently, in the present preferred embodiment, i- Si 1 - xGe x layers (56n, 56p) are selected as the based specific semiconductor layer and it etches until i- Si 1 - xGe x layers (56n, 56p) are exposed. It is the be desirable to use the etching in which selectivity by the wet etching is high when exposing i- Si 1 - xGe x layers (56n, 56p). Area, it lacks the directionality in which the wet etching is different and because it is not suitable for the precision-machining first the domain to form the source · drain electrode among the insulating layer (72) of the first layer is selectively removed with the dry etching and the contact hole is formed and after gate insulating layers (58n, 58p) are exposed what performs a wet etching is the be desirable. For example, it has for example or less, the processing of such processing.

우선, 최상층의 산화막(게이트 절연막(58n, 58p))의 제거에는 잘 알려진 바와 같이 불산계의 용액을 사용한다. 그리고, i-Si 층(57n, 57p)이 노출되면, 불산은 실리콘을 거의) 제거하지 못하기 때문에, 에칭액을 i-Si 층(57)을 제거할 수 있는 에칭액으로 변경한다. 여기서, 본 실시예에서는, i-Si 층(57n, 57p)의 아래의 i-Si1-xGex층(56n, 56p)에 콘택트를 형성하기 때문에, i-Si1-xGex층(56n, 56p)을 그다지 에칭하지 않고, i-Si 층(57n, 57p)을 선택적으로 에칭할 수 있는 에칭액(엣첸트)을 선택한다. 그리고, 이 엣첸트를 사용하여, i-Si 층(57n, 57p)을 제거하여 i-Si1-xGex층(56n, 56p)을 노출시킨다. 이 때, i-Si1-xGex층(56n, 56p)의 일부가 오버 에칭에 의해 제거되어도 된다. 상술한 바와 같이, 이 i-Si1-xGex층(56n, 56p)은, NMOS 트랜지스터의 채널영역에 n-채널을 형성시키기 위하여 에피텍셜 성장시킨 것이다. 따라서, 본 실시예를 이용하면, SiGe 층을 이용한 저저항 콘택트를 형성하기 위하여 새롭게 i-Si1-xGex층(56n, 56p)을 성장시키기 위한 공정이 불필요하게 된다.

First, in the one of oxide films (gate insulating layers (58n, 58p)) of the top layer, as is well known, the solution of the hydrofluoric acid is used. And if i-Si layers (57n, 57p) are exposed , the hydrofluoric acid nearly is unable to remove the silicone. Therefore the etchant is changed into the etchant removing the i-Si layer (57). Here, in the present preferred embodiment, the contact is formed on the following I- Si 1- x Ge x layers (56n, 56p) of i-Si layers (57n, 57p). Therefore i- Si 1- x Ge x layers (56n, 56p) are not etched to the particularly and the etchant which the selectively can etch i-Si layers (57n, 57p) is chosen. And i-Si layers (57n, 57p) are removed using this etchant and i- Si 1- x Ge x layers (56n, 56p) are exposed. Then, over etching gets rid of the part of i- Si 1- x Ge x layers (56n, 56p). As described above, this i- Si 1- x Ge x layers (56n, 56p) are the ken in the selective epitaxial growth it forms the n-channel in the channel region of the NMOS transistor. Therefore, if this embodiment is used , unnecessarily it becomes the process new for growing i- Si 1- x Ge x layers (56n, 56p) in order to form the low resistance contact using the SiGe layer.

다음에, 콘택트를 형성하기 위하여, 이 노출된 i-Si1-xGex층(56n, 56p) 위에 저저항의 금속막을 퇴적시킨다. 이 금속막을 구성하는 금속 재료로서는, 상술한 바와 같이 텅스텐(W)을 사용하면 매우 저항값이 낮은 콘택트를 형성할 수가 있다. 그래

Next, in order that the contact is formed the metal layer of the low resistance is sedimented on exposed i-Si 1- x Ge x layers (56n, 56p). As the metal material comprising this metal layer, if the tungsten (W) is used, a

GF Exhibit 1124 - 2075/2704

서, 본 실시예에서는, LPCVD 법에 의해, WF6을 수소로 희석한 가스를 소스가스로서 이용하여, 온도조건을 400℃ 로서, i-Si1-xGex층(56n, 56p) 위에 소스#183#드레인콘택트 W 층(61n, 61p)을 선택 성장시키고 있다.

s described above, the contact in which the resistance value is very low can be formed. So, in the present pre ferred embodiment, using the low pressure chemical va por deposition, the gas diluting the WF6 to hydrogen is used as the source gas and it is the temperature condi tion 400℃ and source · drain contact W layers (61n, 61 p) selectively are grown on i- Si 1- x Ge x layers (56n, 56p).

다음에, 도 12의 (e)에 나타내는 공정에서, 스퍼터링을 하여 기판의 전면 상에 A1합금막을 퇴적한 후 패터닝하여, A1 소스#183#드레인 전극(63n, 63p)을 형성한다. 이상의 공정에서, 소스#183#드레인 영역 상에 저저항의 콘택트를 형성할 수가 있다.

Next, in the process of showing for (e) of fig. 12, it sputters and the A1 alloy film is patterned on the front of the substrate after doing the deposition and A1 sour ce · drain electrodes (63n, 63p) are formed. In the pro cess described in the above, the contact of the low re sistance can be formed on the source · drain region.

상술한 바와 같이, Si 계 헤테로 M0S 장치에 있어서는, 게이트 절연막으로서 실리콘 산화막을 사용하는 관계상, 반도체 최상층은 밴드 갭이 큰 Si 층인 것이 바람직하기 때문에, 본 실시예와 같은 반도체층을 제거한 후 콘택트 금속층을 형성하는 기술은, Si 계 헤테로 M0S 장치의 형성에 특히 알맞은 기술이다.

As described above, it is in the Si group hetero M0S apparatus and the relation phase , and the technology in which the semiconductor top layer forms the contac t metal layer after it therefore removes the semiconduc tor layer like this embodiment the Si layer in which the band gap is large with the be desirable are the technol ogy which is especially suitable for the formation of the Si group hetero M0S apparatus. Uses the silicon oxide f ilm as the gate insulating layer.

(제 5 실시예)

(The fifth preferred embodiment)

상기 실시예에서는 Si와 SiGe로 이루어지는 헤테로 접합체를 이용한 채널구조를 대표로 들었지만, HCMOS 장치의 소스#183#드레인 영역에 저저항의 콘택트를 형성하는 발명은, 이러한 실시예에 한정되는 것이 아니라, Si와 이 실시예의 SiGe의 적층 구조 이외의 구성을 갖는 헤테로 에피텍셜 적층막에 의한 채널, 예컨대 Si와 i-Si1-x-yGexCy층(0#8804#x#8804#1,0#8804#y#8804#1) 혼합 결정 반도체의 사이에 채널 형성한 것이라도 된다. 헤테로 경계면에 의한 채널형성에는, 반드시 밴드 갭이 다른 두 가지의 반도체의 접합이 필요하기 때문에 이러한 저저항의 콘택트 층의 형성이 유효하게 된다.

In the above preferred embodiment, the channel structure using the Si and the heterozygote consisting of the SiGe was given about the representative. Howev er the invention forming the contact of the low resista nce on the source · drain region of the HCMOS apparat us is not restricted to such embodiment. But it become s although it builds up the channel between the chann el by the hetero epitaxial lamination film, having the co nfiguration except the laminating structure of the SiGe of the Si and this embodiment for example, the Si and i- Si 1-x- y Ge x C y layer (0≤x≤1,0≤y≤1) mixed crystal lization semiconduction. In the channel-forming by the hetero boundary face, the formation of the contact lay er of such low resistance is effective because the junc tion of the semiconductor of two kinds of in which the band gap is certainly different is needed.

도 13은, 도 1에 나타내는 구조에 저저항의 콘택트 금속층을 형성한 제 5 실시예에 의한 HCMOS 장치의 단면도이다.

Figure 13 is a cross-sectional view of the HCMOS apparatus by the fifth preferred embodiment forming th e contact metal layer of the low resistance on the stru cture showing in fig. 1.

도 13에 도시하는 바와 같이, 본 실시예에 의한 HCMOS 장치에 있어서는, S iGe 층(15n, 15p)의 위에 소스#183#드레인 콘택트 W 층(25n, 25p)이 형성되어 있다.

As shown in Figure 13, it is in the HCMOS apparatus by this embodiment and source · drain contact W layers (25n, 25p) are formed in the upper part of S iGe layers (15n, 15p).

본 실시예에 의한 발명의 특징은, 상기 제 1 실시예의 특징에 덧붙여 상기 제 4 실시예와 같이, Si1-x-yGexCy층(0#8804#x#8804#1,0#8804#y#8804#1)을 포함하는 제 1 반도체층과, 상기 제 1 반도체층과는 다른 밴드 갭을 갖는 제 2 반도

The characteristic of the invention by this embodiment is the point which includes the source · drain contact l ayer consisting of the second semiconductor layer, the channel region having the carrier accumulation layer for

GF Exhibit 1124 - 2076/2704

체층과, 상기 제 1, 제 2 반도체층 사이의 경계면 부근의 영역에 형성된 캐리어 축적층을 갖는 채널영역과, 제 3 반도체층과, 이 제 3 반도체층보다 큰 밴드 갭을 갖는 제 4 반도체층을 갖는 소스#183#드레인 영역과, 상기 제 3 반도체층의 바로 위에 형성된 저저항의 도체막으로 이루어지는 소스#183#드레인 콘택트층을 구비하고 있는 점이다.

med in the first, and the domain of the boundary area neighborhood between the second semiconductor laye r, the third semiconductor layer, and the conductor film of the low resistance formed in the source · drain doma in having the fourth semiconductor layer having the ba nd gap having the band gap which has of the first semi conductor layer and which is different from the first se miconductor layer that includes moreover, Si 1-x- y Ge x C y layers (0≤x≤1,0≤y≤1) like the fourth preferred em bodiment to the characteristic of the first preferred em bodiment. The conductor film of the low resistance for med in the source · drain domain having the fourth sem iconductor layer having the band gap is greater than th is third semiconductor layer, and the third semiconduct or layer, immediately, the upper part.

그리고, 본 실시예의 NMOS 트랜지스터에 있어서는, SiGeC 층(14n)은 Si1-x-yGexCy층(0#8804#x#8804#1,0#8804#y#8804#1)을 포함하는 제 1 반도체층으로, Si 층(13n)은 제 2 반도체층이고, SiGe 층(15n)은 제 3 반도체층이며, Si 층(17n)은 SiGe 층(15n)보다 밴드 갭이 큰 제 4 반도체층으로서, 제 3 반도체층인 SiGe 층(15n)의 바로 위에 소스#183#드레인 콘택트 W 층(25n)이 형성되어 있다.

And it is in the NMOS transistor of this embodiment and the Si layer (13n) is the second semiconductor layer to the first semiconductor layer in which the SiGeC layer (14n) includes Si 1-x- y Ge x C y layers (0≤x≤1,0≤y≤1) and the SiGe layer (15n) is the third semiconductor lay er and it is the fourth semiconductor layer in which the Si layer (17n) the band gap is greater than the SiGe la yer (15n) and the source · drain contact W layer (25n) is formed in the SiGe layer (15n), which is the third se miconductor layer immediately, the upper part.

한편, 본 실시예의 PMOS 트랜지스터에 있어서는, SiGe 층(15p)은 Si1-x-yGexCy층(0#8804#x#8804#1,0#8804#y#8804#1)을 포함하는 제 1 반도체층(y= 0)인 동시에 제 3 반도체층이고, Si 층(17p)은 제 2 반도체층임과 동시에 제 3 반도체층보다 밴드 갭이 큰 제 4 반도체층으로서, 제 3 반도체층인 SiGe 층(15p)의 바로 위에 소스#183#드레인 콘택트 W 층(25p)이 형성되어 있다.

In the meantime, it is in the PMOS transistor of this embodiment and it is the first semiconductor layer (y= 0) in which the SiGe layer (15p) includes Si 1-x- y Ge x C y layers (0≤x≤1,0≤y≤1) and it is the third semicondu ctor layer and it is the fourth semiconductor layer in w hich the Si layer (17p) is the second semiconductor lay er and the band gap is greater than the third semicond uctor layer at the same time and the source · drain co ntact W layer (25p) is formed in the SiGe layer (15p), which is the third semiconductor layer immediately, the upper part.

이상과 같이, 본 실시예로서는, A1소스#183#드레인 전극(21n, 21p)의 콘택트를 하는 기판측의 영역(소스#183#드레인 콘택트 W 층 (25n, 25p))을, 채널 형성을 위한 각 반도체층 중 밴드 갭이 작은 층의 바로 위에 설치하고 있기 때문에, 최상층의 반도체층인 Si 층(17n, 17p)의 바로 위에 콘택트를 설치하는 것보다 콘택트 저항이 작아지게 되어, 소자의 저소비 전력과 고속동작이 가능하게 된다.

As described above, as this embodiment, domains (source · drain contact W layers (25n, 25p)) of the sub strate side contacted of A1 source · drain electrodes (21n, 21p) are set up in the layer, in which the band g ap is small immediately, the upper part among each se miconductor layer for the channel-forming. Therefore t he contact resistance becomes smaller than the conta ct is set up in Si layers (17n, 17p), which are the semi conductor layer of the top layer immediately, the upper part and the low dissipation and high speed operation o f the device are possible.

특히, SiGe 층(15n, 15p)에 접촉하도록 텅스텐(W)으로 되는 소스#183#드레인 콘택트 W 층(25n, 25p)을 설치하고 있기 때문에, 매우 낮은 콘택트 저항을 얻을 수 있다.

Especially, source · drain contact W layers (25n, 25p) consisting of the tungsten (W) are set up in order to c ontact SiGe layers (15n, 15p). Therefore the contact r esistance which is very low can be obtained.

즉, 본 실시예에서는 상기 제 1 실시예의 효과를 발휘하면서 콘택트 저항의 저감을 도모할 수 있다.

That is, in the present preferred embodiment, the reduction of the contact resistance can be planned whi le the effect of the first preferred embodiment is demo nstrated.

(제 6 실시예)

(Sixth preferred embodiment)

도 14는, 도 8에 나타내는 구조에 저저항의 콘택트 금속층을

Figure 14 is a cross-sectional view of the HCMOS

GF Exhibit 1124 - 2077/2704

형성한 제 6 실시예에 의한 HCMOS 장치의 단면도이다.

apparatus by the sixth preferred embodiment forming t he contact metal layer of the low resistance on the str ucture showing in fig. 8.

도 14에 도시하는 바와 같이, 본 실시예에 의한 HCMOS 장치에 있어서는, 양자 우물 영역으로 되는 SiGe 층(36n, 36p) 위에, 소스#183#드레인 콘택트 W 층(45n, 45p)이 형성되어 있다.

As shown in Figure 14, it is in the HCMOS apparatus by this embodiment and source · drain contact W layers (45n, 45p) are formed on SiGe layers (36n, 36p) consis ting of the quantum-well gain region.

본 실시예에 의한 발명의 특징은, 상기 제 3 실시예의 특징에 덧붙여, 상기 제 4 실시예와 같이, Si1-x-yGexCy층(0#8804#x#8804#1,0#8804#y#8804#1)을 포함하는 제 1 반도체층과, 상기 제 1 반도체층과는 다른 밴드 갭을 갖는 제 2 반도체층과, 상기 제 1, 제 2 반도체층 사이의 경계면 부근의 영역에 형성된 캐리어 축적층을 갖는 채널영역과, 제 3 반도체층과, 이 제 3 반도체층보다 큰 밴드 갭을 갖는 제 4 반도체층을 갖는 소스#183#드레인 영역과, 상기 제 3 반도체층의 바로 위에 형성된 저저항의 도체막으로 이루어지는 소스#183#드레인 콘택트층을 구비하고 있는 점이다.

The characteristic of the invention by this embodiment is the point which includes the source · drain contact l ayer consisting of the second semiconductor layer, the channel region having the carrier accumulation layer for med in the first, and the domain of the boundary area neighborhood between the second semiconductor laye r, the third semiconductor layer, and the conductor film of the low resistance formed in the source · drain doma in having the fourth semiconductor layer having the ba nd gap having the band gap which has of the first semi conductor layer and which is different from the first se miconductor layer that includes moreover, Si 1-x- y Ge x C y layers (0≤x≤1,0≤y≤1) like the fourth preferred em bodiment to the characteristic of the third preferred e mbodiment. The conductor film of the low resistance fo rmed in the source · drain domain having the fourth se miconductor layer having the band gap is greater than this third semiconductor layer, and the third semicondu ctor layer, immediately, the upper part.

그리고, 본 실시예의 NMOS 트랜지스터에 있어서는, 양자 우물 영역인 SiGeC 층(34n)은 Si1-x-yGexCy층(0#8804#x#8804#1,0#8804#y#8804#1)을 포함하는 제 1 반도체층으로, 제 1 Si 층(33n)은 제 2 반도체층이고, 양자 우물 영역인 SiGe 층(36n)은 제 3 반도체층이며, 제 3 Si 층(37n)은 SiGe 층(36n)보다 밴드 갭이 큰 제 4 반도체층으로서, 제 3 반도체층인 SiGe 층(36n)의 바로 위에 소스#183#드레인 콘택트 W 층(45n)이 형성되어 있다.

And it is in the NMOS transistor of this embodiment and the first Si layer (33n) is the second semiconductor lay er to the first semiconductor layer in which the SiGeC l ayer (34n) which is the quantum-well gain region includ es Si 1-x- y Ge x C y layers (0≤x≤1,0≤y≤1) and the Si Ge layer (36n) which is the quantum-well gain region is the third semiconductor layer and it is the fourth semic onductor layer in which the third Si layer (37n) the ban d gap is greater than the SiGe layer (36n) and the sour ce · drain contact W layer (45n) is formed in the SiGe l ayer (36n), which is the third semiconductor layer imm ediately, the upper part.

한편, 본 실시예의 PMOS 트랜지스터에 있어서는, SiGe 층(36p)은 Si1-x-yGexCy층(0#8804#x#8804#1,0#8804#y#8804#1)을 포함하는 제 1 반도체층(y= 0)인 동시에 제 3 반도체층이고, 제 3 Si 층(37p)은 제 2 반도체층인 동시에 제 3 반도체층보다 밴드 갭이 큰 제 4 반도체층으로서, 제 3 반도체층인 SiGe 층(36p)의 바로 위에 소스#183#드레인 콘택트 W 층(45p)이 형성되어 있다.

In the meantime, it is in the PMOS transistor of this embodiment and it is the first semiconductor layer (y= 0) in which the SiGe layer (36p) includes Si 1-x- y Ge x C y layers (0≤x≤1,0≤y≤1) and it is the third semicondu ctor layer and it is the fourth semiconductor layer in w hich the third Si layer (37p) is the second semiconduct or layer and the band gap is greater than the third sem iconductor layer at the same time and the source · drai n contact W layer (45p) is formed in the SiGe layer (36 p), which is the third semiconductor layer immediately, the upper part.

이상과 같이, 본 실시예에서는 Al 소스#183#드레인 전극(41n, 41p)의 콘택트를 하는 기판측의 영역(소스#183#드레인 콘택트 W 층(45n, 45p)을 채널 형성을 위한 각 반도체층 중 밴드 갭이 작은 층의 바로 위에 설치하고 있기 때문에, 최상층의 반도체층인 Si 층(37n, 37p)의 바로 위에 콘택트를 설치하는 것보다 콘택트 저항이 작아지게 되어 장치의 저소비 전력과 고속동작이 가능하게 된다.

As described above, in the present preferred embodiment, domain (source · drain contact W layers (45n, 45p) of the substrate side contacted of Al sourc e · drain electrodes (41n, 41p) are set up in the layer, i n which the band gap is small immediately, the upper p art among each semiconductor layer for the channel-fo rming. Therefore the contact resistance becomes small er than the contact is set up in Si layers (37n, 37p), w hich are the semiconductor layer of the top layer imme diately, the upper part and the low dissipation and high speed operation of the apparatus are possible.

GF Exhibit 1124 - 2078/2704

특히, SiGe 층(36n, 36p)에 접촉하도록 텅스텐(W)으로 되는 소스#183#드레인 콘택트 W 층(45n, 45p)을 설치하고 있기 때문에 매우 낮은 콘택트 저항을 얻을 수 있다.

Especially, because source · drain contact W layers (45n, 45p) consisting of the tungsten (W) are set up in order to contact SiGe layers (36n, 36p) , the contact r esistance which is very low can be obtained.

즉, 본 실시예로서는, 상기 제 3 실시예의 효과를 발휘하면서 콘택트 저항의 저감을 도모할 수 있다.

That is, as this embodiment, the reduction of the contact resistance can be planned while the effect of t he third preferred embodiment is demonstrated.

(그 밖의 변형 실시예)

(The other example of change execution)

상기 제 1~제 6 실시예로서는, 게이트 전극의 밑으로 게이트 절연막을 설치한 MOS 형 전계 효과 트랜지스터에 대하여 설명하였지만, 본 발명은 이러한 실시예에 한정되는 것은 아니다. 특히, 최상층에 절연막이 있는 헤테로 M0S 구조가 아니라 헤테로 경계면을 이용하는 전계 효과 트랜지스터이면, 절연막을 이용하지 않는 쇼트키 접합을 이용하는 장치라도 실시 가능하고, 저항의 저감효과를 얻는 것이 가능하여, 장치의 저소비전력 및 고속동작에 유리하게 된다.

As the 1~ sixth preferred embodiment, it illustrated for MOSFET setting the gate insulating layer up in the bott om of the gate electrode. However the invention is not restricted to such embodiment. Especially, if it is the fi eld effect transistor which is not hetero M0S structure where the insulating layer is in the top layer but uses t he hetero boundary face , although it is the apparatus for using the Schottky barrier which does not use the i nsulating layer it enables to implement and it is possible to obtain the reduction effect of the resistance and it i s advantageous for the low dissipation and high speed operation of the apparatus.

상기 제 1~제 6 실시예에서는, #948# 도핑층을 형성하였지만, 본 발명은 이러한 실시예에 한정되는 것이 아니고, #948# 도핑층을 설치하지 않더라도 본 발명의 효과를 발휘하는 것은 가능하다. 또한, #948# 도핑층을 형성하는 경우에도 스페이스층은 반드시 필요한 것은 아니다.

In the 1~ sixth preferred embodiment, the δ doped layer was formed. However the invention is not restrict ed to such embodiment but it is possible to exhibit the effect of the invention although the δ doped layer is no t set up. Moreover, the certainly the space layer is not necessary even in case of forming the δ doped layer.

상기 제 1, 제 2, 제 3, 제 5, 제 6 실시예에 있어서 SiGe 층에 대신하여 C층을 미량 첨가한 SiGeC 층을 설치하여도 된다.

The SiGeC layer replacing as to the first, second, third, fifth, sixth preferred embodiment in the SiGe layer and adds the layer with small amount is set up.

또, 상기 제 1, 제 2, 제 3, 제 5, 제 6 실시예에 있어서는, SiGeC 층과, SiGe 층의 상하관계를 반대로 하여도 되는 것으로 한다. 그 경우, 제 5,제 6 실시예에서는 소스#183#드레인 영역에서의 SiGeC 층 바로 위에 소스#183#드레인 콘택트 W 층을 형성하면 된다.

And it is in the first, second, third, fifth, sixth preferred embodiment and with up and down relation of the SiGe C layer, and SiGe layer are done on the contrary it doe s. In the case, the fifth, and the sixth preferred embodi ment, the source · drain contact W layer is formed on t he SiGeC layer at the source · drain region, immediatel y, the upper part.

도면에 대한 간단한 설명

Brief explanation of the drawing

도 1은 본 발명의 제 1 실시예에 의한 SiGeC 계 HCMOS 장치의 구조를 나타내는 단면도.

Figure 1 is a cross-sectional view showing the structure of the SiGeC group HCMOS apparatus by the first preferred embodiment of the invention.

도 2는 HCMOS 장치 내의 SiGeC 층의 격자 왜곡의 Ge 조성율 및 C 조성율에 대한 의존성을 도시한 도면.

Figure 2 is a drawing showing the dependability about the Ge composition rate of the lattice distortion of the SiGeC layer of the HCMOS in the apparatus and C comp osition rate.

도 3은 SiGeC 계 HCMOS 장치의 SiCeC 층과 Si 층 사이에 있어 격자정합 또는 인장 왜곡을 발생하는 Si, Ge, C의 조성율과의 관계를 도시한 도면.

Figure 3 is a drawing showing the SiCeC layer and the Si generated the lattice matching or the tensile distorti on as to the Si layer interval of the SiGeC group HCMO S apparatus, the Ge, and the relation with the composi tion rate of C.

도 4는 SiGeC 층의 C 조성비와 에너지 갭 값의 관계를 도시한 도면.

Figure 4 is a drawing showing C composition ratio of the SiGeC layer and relation of the energy gap value.

도 5는 본 발명의 제 I의 실시예에 의한 반도체 장치의 제조 공정을 나타내는 단면도.

Figure 5 is a cross-sectional view showing the manufacturing process of the semiconductor device by the embodiment of the I of the invention.

도 6은 본 발명의 제 2 실시예에 있어서의 SiGeC 층의 조성과

Figure 6 is a drawing showing the relation of the

GF Exhibit 1124 - 2079/2704

격자 부정합에 의한 왜곡의 관계를 도시한 도면.

distortion by the composition of the SiGeC layer in the second preferred embodiment of the invention and latti ce mismatch.

도 7은 본 발명의 제 2 실시예에 의한 격자 정합계 SiGeC-HCMOS 장치의 밴드-라인업을 도시한 도면.

Figure 7 is a drawing showing the band - lineup of the lattice-match system SiGeC-HCMOS apparatus accordi ng to the second preferred embodiment of the present invention.

도 8은 본 발명의 제 3 실시예에 의한 양자 우물 구조의 채널을 갖는 HCMOS 장치의 구조를 나타내는 단면도.

Figure 8 is a cross-sectional view showing the structure of the HCMOS apparatus for having the chan nel of the quantum well structure according to the thir d preferred embodiment of the present invention.

도 9는 본 발명의 제 3 실시예에 의한 반도체 장치의 제조공정을 나타내는 단면도.

Figure 9 is a cross-sectional view showing the manufacturing process of the semiconductor device ac cording to the third preferred embodiment of the prese nt invention.

도 10은 본 발명의 제 4 실시예에 의한 HCMOS 장치의 구조를 나타내는 단면도.

Figure 10 is a cross-sectional view showing the structure of the HCMOS apparatus according to the fo urth preferred embodiment of the present invention.

도 11은 본 발명의 제 4 실시예에 의한 HCMOS 장치의 제조공정 중의 전반 부분을 나타내는 단면도.

Figure 11 is a cross-sectional view showing the former half portion among the manufacturing process of the H CMOS apparatus according to the fourth preferred emb odiment of the present invention.

도 12는 본 발명의 제 4 실시예에 의한 HCMOS 장치의 제조공정 중의 후반 부분을 나타내는 단면도.

Figure 12 is a cross-sectional view showing the latter half part among the manufacturing process of the HCM OS apparatus according to the fourth preferred embodi ment of the present invention.

도 13은 본 발명의 제 5 실시예에 의한 HCMOS 장치의 구조를 나타내는 단면도.

Figure 13 is a cross-sectional view showing the structure of the HCMOS apparatus according to the fift h preferred embodiment of the present invention.

도 14는 본 발명의 제 6 실시예에 의한 HCMOS 장치의 구조를 나타내는 단면도.

Figure 14 is a cross-sectional view showing the structure of the HCMOS apparatus by the sixth preferr ed embodiment of the invention.

도 15는 종래의 HCMOS 장치의 구조를 나타내는 단면도

Figure 15 is a cross-sectional view showing the structure of the conventional HCMOS apparatus

도 16은 종래의 HCMOS 장치의 헤테로 경계면에 도입되는 격자 부정합에 의한 전위 등의 결함을 도시한 도면.

Figure 16 is a drawing showing the deformity including the electric potential by the lattice mismatch introduce d to the hetero boundary face of the conventional HCM OS apparatus etc.

도면의 주요한 부위를 나타내는 부호의 설명

The description * of the symbol showing the important site of * drawing.

1O, 30, 50 : Si 기판 11, 31, 51n : p 홀
12, 32, 51p : n 홀 13 : Si 층
14, 34 : SiGeC 층 15, 36 : SiGe 층
16 소스#183#드레인 영역 17 Si 층
18, 38, 65 : 게이트 전극 19, 39, 58 : 게이트 절연막

1O, 30, 50: si substrate 11, 31, 51n: the p hole.
12, 32, 51p: the n hall 13: si layer.
14, 34: siGeC layer 15, 36: siGe layer.
16 source · drain region 17 Si layer.
18, 38, 65: gate electrode 19, 39, 58: gate insulating layer.

21, 41 : 소스#183#드레인 전극 25, 45, 61 : 소스#183#드레인 콘택트W 층
33 : 제 1 Si 층 35 : 제 2 Si 층
37 : 제 3 Si 층 42, 49 : 소스#183#드레인 영역
52 : SiGe 버퍼층 53 : #948# 도핑층
54 : 스페이스 층 55, 57 : i-Si 층
56 : i-Sil-xGex 층 63 : Al 소스#183#드레인 전극
66 : 제 1 층 절연막 67 : n-채널
68 : p-채널

21, 41: source · drain electrode 25, 45, 61: source · drain contact W layer.
33: first Si layer 35: second Si layer.
37: third Si layer 42, 49: source · drain region.
52: siGe buffer layer 53: δ doped layer.
54: space layer 55, 57: i-Si layer.
56: i- Si l- x Ge x layer 63: al source · drain electrode.
66: first layer insulating layer 67: the n-channel.
68: the p-channel.

Disclaimer

본 문서는 특허 및 과학기술문헌 전용의 첨단 자동번역 시스템을 이용해 생성되었습니다. 따라서 부분적으로 오역의 가능성이 있으며, 본 문서를 자격을 갖춘 전문 번역가에 의한 번역물을 대신하는 것으로 이용되어서는 안 됩니다. 시스템 및 네트워크의 특성때문에 발생한 오역과 부분 누락, 데이터의 불일치등에 대하여 본원은 법적인 책임을 지지 않습니다. 본 문서는 당사의 사전 동의 없이 권한이 없는 일반 대중을 위해 DB 및 시스템에 저장되어 재생, 복사, 배포될 수 없음을 알려드립니다.

GF Exhibit 1124 - 2080/2704

(The document produced by using the high-tech machine translation system for the pate
nt and science & technology literature. Therefore, the document can include the mistrans
lation, and it should not be used as a translation by a professional translator. We hold n
o legal liability for inconsistency of mistranslation, partial omission, and data generated
by feature of system and network. We would like to inform you that the document canno
t be regenerated, copied, and distributed by being stored in DB and system for unauthori
zed general public without our consent.)

GF Exhibit 1124 - 2081/2704

(19) 대한민국특허청(KR)
(12) 공개특허공보(A)

(11) 공개번호 특1999-025041
(43) 공개일자 1999년04월06일

(51) 국제분류코드
H01L 27/02 (2006.01)

(21) 출원번호 특1997-046481

(22) 출원일자 1997년09월10일

(71) 출원인
김영환
현대전자산업 주식회사
경기도 이천시 부발읍 아미리 산 136-1, 경기도

(72) 발명자
윤경일
경기도 이천시 대월면 사동리 441-1 현대아파트 102동 603호, 경기도
최용진
서울특별시 동작구 사당1동 426-16, 서울특별시

(74) 대리인
김동진
정은섭
허진석

(77) 심사관
없음

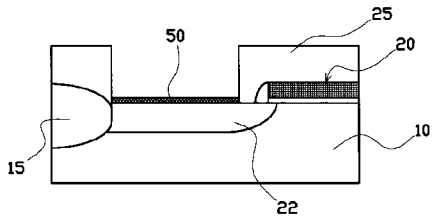
전체 청구항 수 : 총 3 항

(54)반도체장치의 캐패시터 제조방법

(57)요 약

본 발명은 반도체장치의 캐패시터 제조방법에 관한 것으로서, 본 발명의 목적은 메모리장치의 제조공정중 정보를 저장하는 셀캐패시터의 형성과정에서 장벽층 공정을 삽입하여 콘택의 접합손실을 감소시킴으로서 리플래쉬 특성을 향상시키도록 한 반도체장치의 캐패시터 제조방법를 제공함에 있다. 상기와 같은 목적을 실현하기 위한 본 발명은 캐패시터의 하부전극을 접합시키기 위한 콘택식각을 행하는 단계와, 콘택식각후 콘택플러그주입을 행하는 단계를 포함하여 이루어진 반도체장치의 캐패시터 제조방법에 있어서, 상기 콘택식각후 장벽층을 형성하는 단계와, 콘택플러그주입후 열공정하는 단계를 더 포함하여 이루어져 콘택형성시 발생되는 손상을 큐링시킬 수 있어 캐패시터의 특성향상 및 생산수율개선에 효과가 있다.

대 표 도 - 도 2



This Facsimile Page has been artificially created from KIPO data.

청구의 범위

청구항 1

캐패시터의 하부전극을 접합시키기 위한 콘택식각을 행하는 단계와, 콘택식각후 콘택플러그주입을 행하는 단계를 포함하여 이루어진 반도체장치의 캐패시터 제조방법에 있어서,

상기 콘택식각후 장벽층을 형성하는 단계와,

상기 콘택플러그주입후 열공정하는 단계

를 더 포함하여 이루어지는 것을 특징으로 하는 반도체장치의 캐패시터 제조방법.

청구항 2

제1항에 있어서, 상기 장벽층은

50Å정도 두께의 산화막인 것을 특징으로 하는 반도체장치의 캐패시터 제조방법.

청구항 3

제1항에 있어서, 상기 열공정은

900℃의 질소분위기에서 30분간 행하는 것을 특징으로 하는 반도체장치의 캐패시터 제조방법.

명세서

발명의 명칭

반도체장치의 캐패시터 제조방법

도면의 간단한 설명

도1은 일반적인 방법에 의한 반도체장치의 캐패시터 제조공정중 캐패시터의 하부전극의 접합을 위한 콘택형성공정을 나타낸 단면도이다.

도2 내지 도3은 본 발명에 의한 방법으로 반도체장치의 캐패시터 제조공정중 캐패시터의 하부전극의 접합을 위한 콘택형성공정을 나타낸 단면도이다.

- 도면의 주요부분에 대한 부호의 설명 -

10 : 기판 30 : 스페이서

40 : 하부전극 50 : 장벽층

발명의 상세한 설명

본 발명은 반도체장치의 캐패시터 제조방법에 관한 것으로서, 보다 상세하게는 메모리제조공정중 정보를 저장하는 셀캐패시터의 형성과정에서 장벽층형성 공정을 삽입하여 콘택의 접합손실을 감소시킴으로서 리플래쉬 특성을 향상시키도록 한 반도체장치의 캐패시터 제조방법에 관한 것이다.

메모리장치는 컴퓨터, 통신시스템, 화상처리시스템등에 사용되는 데이타나 명령어등을 일시적으로 또는 영구적으로 저장하기 위해 사용되는 총칭으로서 반도체, 데이프, 디스크, 광방식 등이 있는데 현재 반도체 메모리가 많은 비중을 차지하고 있다.

이러한 반도체 메모리장치도 데이타의 저장방식의 전기적인 특성에 따라 DRAM, SRAM, Flash 메모리, ROM 등으로 구분된다. 이중 전체 반도체메모리 시장의 대부분을 차지하고 있는 DRAM(Dynamic Random Access Memory)의 특징은 랜덤억세스가 가능하고 전기적으로 데이타의 읽기와 쓰기가 가능하며 특히 쓰기의 횟수에 제한이 없으며, 전원 공급이 중단되면 기억중인 데이타가 소실되는 휘발성 메모리이며, 주기적으로 리플레쉬(Refresh)가 필요하며, 리스토어동작을 만족시키기 위해 매 ROW사이클 동작마다 프리차지(Precharge)시간이 필요하다는 특징이있다.

메모리장치를 구성하는 소자로는 트랜지스터 및 캐패시터등으로 구성되는데 개패시터의 경우에는 적은 면적에도 불구하고 정전용량이 증가되어야 하며 캐패시터의 리플레쉬특성을 향상시키기 위한 리키지의 감소문제가 있다.

도1은 일반적인 반도체장치의 캐패시터 제조방법에 의해 형성된 메모리장치의 셀캐패시터의 하부전극부분을 나타낸 단면도이다.

도1은 기판(10)위에 형성된 트랜지스터(20)의 소오스/드레인(22)에 캐패시터의 하부전극(40)을 접합시키기 위해 BPSG(Boro Phospho Silicate Glass)층(25)위에 콘택마스크를 형성하여 콘택식각한후 콘택의 접합저항을 감소시키기위한 이온주입을 실행한후 콘택 스페이서(30)와 하부전극(40)을 증착한 상태를 나타낸 단면도이다.

일반적인 캐패시터의 셀구조는 스택(Stack)이나 핀(Fin) 또는 실린더(Cylinder)등의 구조로 이루어져 도1에서 보는 바와 같이 셀캐패시터의 노드로써 n-가 p기판위에 형성하는 접촉접합을 주로 사용하고 있다.

셀캐패시터에 저장되는 정보의 손실은 주로 이 접촉접합을 통하여 발생하게 되는데 하부전극(40)을 형성하기 위해 콘택식각하고 그위에 이온을 주입시키면서 물리적인 충격에 의한 손상으로 'A'와 같은 손상이 발생하여 이곳으로 접합손실이 발생된다. 이 손실은 DRAM의 경우에는 리플래쉬특성에 큰 영향을 준다는 문제점이 있다.

또한 이온주입에 의한 물리적 충격으로 손상된 기판(10)을 큐링(Curing)하는 공정으로 고온에서 어닐링을 수행하는데 일반적인 방법에서는 하부전극(40)이 완성된 뒤에 행하기 때문에 충분한 큐링이 이루어지지 않는다는 문제점이 있다.

본 발명은 상기와 같은 문제점을 해결하기 위해 창작된 것으로서, 본 발명의 목적은 반도체장치의 캐패시터 제조공정시 캐패시터의 하부전극을 위한 콘택식각에 의한 손상과 콘택저항을 감소시키기 위한 이온주입공정시의 손상을 줄이기 위해 콘택식각후 산화막을 형성하고 이온주입후 열공정을 추가하여 손상으로 인한 접합누설의 발생을 줄이도록 하는 반도체장치의 캐패시터 제조방법을 제공함에 있다.

상기와 같은 목적을 실현하기 위한 본 발명은 캐패시터의 하부전극을 접합시키기 위한 콘택식각을 행하는 단계와, 콘택식각후 콘택플러그 이온주입을 행하는 단계를 포함하여 이루어진 반도체장치의 캐패시터 제조방법에 있어서, 상기 콘택식각후 장벽층을 형성하는 단계와, 콘택플러그 이온주입후 열공정하는 단계를 더 포함하여 이루어지는 것을 특징으로 한다.

상기와 같은 방법에 의하여 제조된 캐패시터는 콘택식각에 의한 손상과 장벽층에 의해 이온주입시 발생되는 손상을 방지할 수 있고 열공정을 통해 손상된 기판을 큐링시킬 수 있어 캐패시터에 저장된 전하의 손실을 방지하여 리플래쉬의 특성을 향상시킬 수 있게 된다.

이하, 본 발명의 바람직한 실시예를 첨부된 도면을 참조하여 설명한다. 또한 본 실시예는 본 발명의 권리범위를 한정하는 것은 아니고, 단지 예시로 제시된 것이며 종래 구성과 동일한 부분은 동일한 부호 및 명칭을 사용한다.

도2 내지 도3은 본 발명의 방법에 따라 종래의 방법에 추가되는 공정을 단계적으로 나타낸 단면도이다.

도2는 기판(10)위에 형성된 캐패시터의 하부전극(40)부분을 나타낸 것으로서 기판(10)에 격리산화막(15)을 형성하고 트랜지스터(20)를 형성한후 BPSG층(25)을 증착한 다음 캐패시터를 형성하기 위해 트랜지스터(20)의 소오스/드레인(22) 영역에 콘택홀을 형성한 다음 장벽층(50)을 형성한 상태를 나타낸 단면도이다.

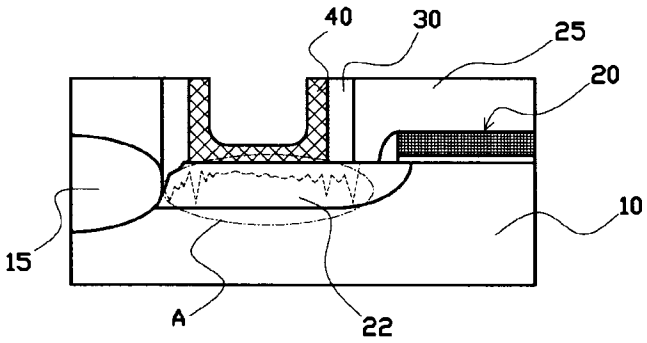
장벽층(50)은 산화공정으로 50Å정도의 두께로 형성된 산화막층이다.

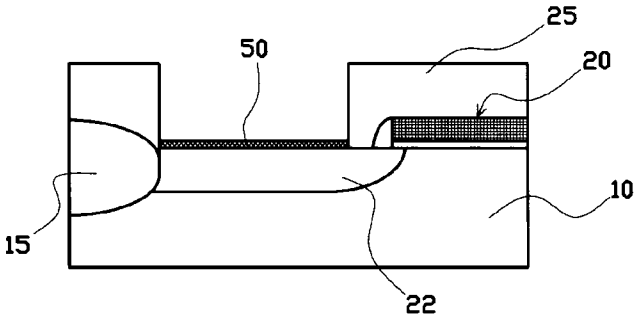
도3은 도2의 결과물에 접촉저항을 줄이기 위한 이온주입공정으로 인(PHOSPHORUS 31)이 주입된 상태를 나타낸 단면도이다.

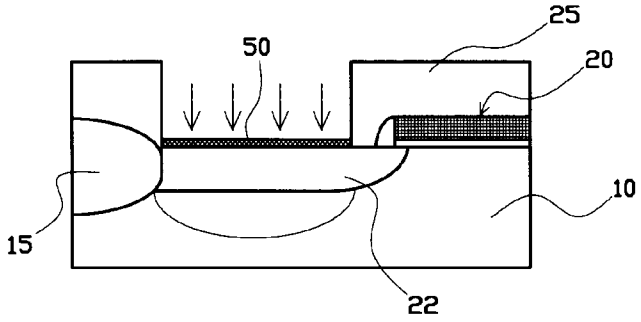
그런다음 900℃의 질소분위기에서 약 30분동안 열공정을 통해 콘택식각시 발생된 손상과 이온주입시 발생된 손상을 큐링시킨다.

이후 공정은 종래의 반도체장치의 캐패시터 제조방법과 동일하게 진행된다. 본 실시예에서는 콘택형성시와 이온주입시 발생되는 손상을 큐링하고 다음 공정을 진행하기 때문에 접합손실을 줄일 수 있게된다.

상기한 바와 같이 본 발명은 반도체장치에서 캐패시터의 하부전극을 접촉시키기 위한 콘택형성시 콘택식각과 접합저항을 줄이기 위한 이온주입시 발생되는 손상을 줄이기 위해 콘택형성후 장벽층을 형성하고 이온주입후 열공정을 통해 발생된 손상을 큐링시킴으로서 접합손실을 줄일수 있어 캐패시터의 리플래쉬 특성을 향상시켜 생산수율의 개선 및 제품의 수명은 연장시킬 수 있다는 이점이 있다.


40
30
25
20
10
15
A
22


25
50
20
10
15
22


25
50
20
10
15
22

Unexamined Patent Publication(A)

Bibliographic Data

Int.Cl.	H01L 27/108 | H01L 49/02
Application No.	1019970046481
Application Date	19970910
Unexamined Publication No.	1019990025041
Unexamined Publication Date	19990406
Agent.	AJU INTERNATIONAL LAW & PATENT GROUP | Kim Dong Jin | Huh Jin Seok
Inventor	Gyeong-Il Yoon | Yong-Jin Choi
Applicant	SK hynix Inc.

발명의 명칭

반도체장치의 캐패시터 제조방법

Title of Invention

METHOD FOR MANUFACTURING A POWER SEMICONDUCTOR DEVICE BY USING A SEMI-INSULATIN G POLY SILICON FILM FOR REDUCING GENERATION OF J UNCTION LEAKAGE BY ADDING THE STEPS OF FORMING A BARRIER LAYER AND HEAT PROCESSING

요약

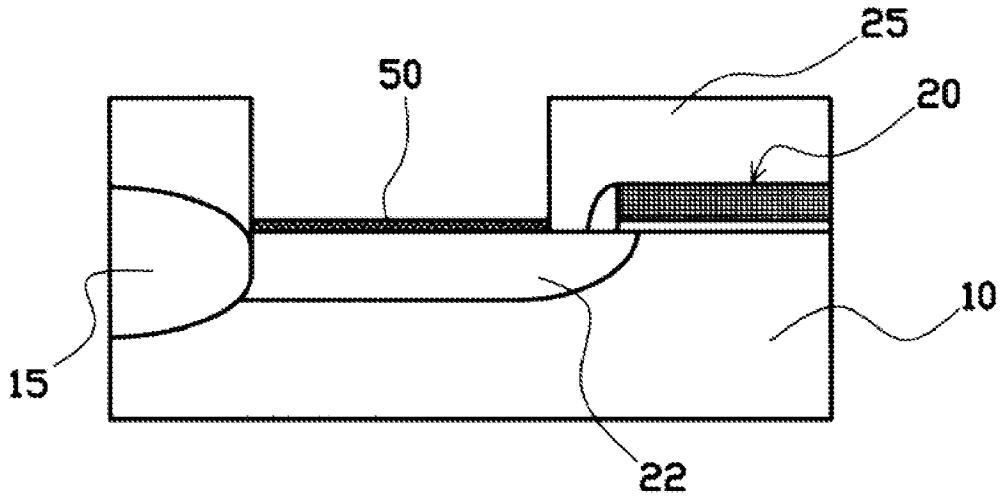
본 발명은 반도체장치의 캐패시터 제조방법에 관한 것으로서, 본 발명의 목적은 메모리장치의 제조공정중 정보를 저장하는 셀캐패시터의 형성과정에서 장벽층 공정을 삽입하여 콘택의 접합손실을 감소시킴으로서 리플래쉬 특성을 향상시키도록 한 반도체장치의 캐패시터 제조방법를 제공함에 있다. 상기와 같은 목적을 실현하기 위한 본 발명은 캐패시터의 하부전극을 접합시키기 위한 콘택식각을 행하는 단계와, 콘택식각후 콘택플러그주입을 행하는 단계를 포함하여 이루어진 반도체장치의 캐패시터 제조방법에 있어서, 상기 콘택식각후 장벽층을 형성하는 단계와, 콘택플러그주입후 열공정하는 단계를 더 포함하여 이루어져 콘택형성시 발생되는 손상을 큐링시킬 수 있어 캐패시터의 특성향상 및 생산수율개선에 효과가 있다.

Abstract

The invention is to provide the capacitor of a semiconductor device manufacturing method it inserts the barrier process as the invention relating to the cap acitor of a semiconductor device manufacturing metho d in the forming process of the cell capacitor in which t he object of the present invention stores the informati on among the manufacturing process of the memory de vice and it reduces the junction loss of the contact for improving the refresh characteristic. More comprises th e step of forming barrier after the contact etch for real izing the above-mentioned purpose, and the step of pr ocessing heat after the contact plug injection and the damage generated in the contact forming can be cured and the effect is in the characteristic enhancement an d production yield improvement of the capacitor.

대표도면(Representative drawing)

GF Exhibit 1124 - 2088/2704



청구의 범위

청구 1항:

캐패시터의 하부전극을 접합시키기 위한 콘택식각을 행하는 단계와, 콘택식각후 콘택플러그주입을 행하는 단계를 포함하여 이루어진 반도체장치의 캐패시터 제조방법에 있어서, 상기 콘택식각후 장벽층을 형성하는 단계와, 상기 콘택플러그주입후 열공정하는 단계를 더 포함하여 이루어지는 것을 특징으로 하는 반도체장치의 캐패시터 제조방법.

청구 2항:

제1항에 있어서, 상기 장벽층은50Å정도 두께의 산화막인 것을 특징으로 하는 반도체장치의 캐패시터 제조방법.

청구 3항:

제1항에 있어서, 상기 열공정은900℃의 질소분위기에서 30분간 행하는 것을 특징으로 하는 반도체장치의 캐패시터 제조방법.

배경기술

본 발명은 반도체장치의 캐패시터 제조방법에 관한 것으로서, 보다 상세하게는 메모리제조공정중 정보를 저장하는 셀캐패시터의 형성과정에서 장벽층형성 공정을 삽입하여 콘택의 접합손실을 감소시킴으로서 리플래쉬 특성을 향상시키도록 한 반도체장치의 캐패시터 제조방법에 관한 것이다.

메모리장치는 컴퓨터, 통신시스템, 화상처리시스템등에 사용되는 데이타나 명령어등을 일시적으로 또는 영구적으로 저장하기 위해 사용되는 총칭으로서 반도체, 데이프, 디스크, 광방식등이 있는데 현재 반도체 메모리가 많은 비중을 차지하고 있다.

Scope of Claims

Claim 1:

The capacitor of a semiconductor device manufacturing method which further includes the step of forming barrier after the contact etch, and the step of processing heat after the contact plug injection as to the capacitor of a semiconductor device manufacturing method which comprises the step of performing the contact etch for welding the bottom electrode of the capacitor, and the step of performing the contact plug injection after the contact etch and comprises.

Claim 2:

As for claim 1, the capacitor of a semiconductor device manufacturing method which is the oxide film of the barrier silver 50Å about thickness.

Claim 3:

As for claim 1, the capacitor of a semiconductor device manufacturing method performed in the nitrogen atmosphere of the thermal process silver 900℃ with 30 min.

Background Art

The invention relates to the capacitor of a semiconductor device manufacturing method, and more specifically, to the capacitor of a semiconductor device manufacturing method it inserts the barrier layer formation process in the forming process of the cell capacitor storing the information among the memory manufacturing process and it reduces the junction loss of the contact for improving the refresh characteristic.

The semiconductor, tape, the disc, the beam form etc as the general name which or is provisionally data or the instruction etc. used in order to store used for the memory device is the computer, the communication system, the image processing system etc it has but the specific gravity in which the current semiconductor memo

GF Exhibit 1124 - 2089/2704

ry is many is occupied.

이러한 반도체 메모리장치도 데이타의 저장방식의 전기적인 특성에 따라 DRAM, SRAM, Flash 메모리, ROM 등으로 구분된다. 이중 전체 반도체메모리 시장의 대부분을 차지하고 있는 DRAM(Dynamic Random Access Memory)의 특징은 랜덤억세스가 가능하고 전기적으로 데이타의 읽기와 쓰기가 가능하며 특히 쓰기의 횟수에 제한이 없으며, 전원 공급이 중단되면 기억중인 데이타가 소실되는 휘발성 메모리이며, 주기적으로 리플레쉬(Refresh)가 필요하며, 리스토어동작을 만족시키기 위해 매 ROW사이클 동작마다 프리차지(Precharge)시간이 필요하다는 특징이있다.

According to such semiconductor memory device is the electrical property of the store method of data, it is classified into DRAM, SRAM, flash memory, ROM etc. The characteristic of the DRAM (Dynamic Random Access Memory) occupying the majority of the whole semiconductor memory market among this the random access is possible and the reading and write of data are electrically possible and there is no limit in especially, the times of the write and it is the volatile memory in which data which it memorizes if the electric power supply is suspended are destroyed by fire and the refresh is necessary and in order to satisfy the restore operation, it has with the characteristic lice. That it need the pre charge (Precharge) time.

메모리장치를 구성하는 소자로는 트랜지스터 및 캐패시터등으로 구성되는데 개패시터의 경우에는 적은 면적에도 불구하고 정전용량이 증가되어야 하며 캐패시터의 리플레쉬특성을 향상시키기 위한 리키지의 감소문제가 있다.

It has the reduction problem of the leakage for being made up of the transistor and capacitor etc. of the device comprising the memory device but improving the refresh property of the capacitor while the electrostatic capacity has to be increased in spite of the area which is less in the capacitor.

도1은 일반적인 반도체장치의 캐패시터 제조방법에 의해 형성된 메모리장치의 셀캐패시터의 하부전극부분을 나타낸 단면도이다.

Figure 1 is a cross-sectional view showing the lower electrode part of the cell capacitor of the memory device formed by the general capacitor of a semiconductor device manufacturing method.

도1은 기판(10)위에 형성된 트랜지스터(20)의 소오스/드레인(22)에 캐패시터의 하부전극(40)을 접합시키기 위해 BPSG(Boro Phospho Silicate Glass)층(25)위에 콘택마스크를 형성하여 콘택식각한후 콘택의 접합저항을 감소시키기위한 이온주입을 실행한후 콘택 스페이서(30)와 하부전극(40)을 증착한 상태를 나타낸 단면도이다.

Figure 1 is a cross-sectional view showing the state depositing the ion implantation forms the contact mask on the BPSG (Boro Phospho Silicate Glass) layer (25) in order to weld the bottom electrode (40) of the capacitor to the source / drain (22) of the formed transistor (20) on the substrate (10) and , for reducing the junction resistance of the contact after doing the contact etch the contact space (30) and bottom electrode (40) after doing the execution.

일반적인 캐패시터의 셀구조는 스택(Stack)이나 핀(Fin) 또는 실린더(Cylinder)등의 구조로 이루어져 도1에서 보는 바와 같이 셀캐패시터의 노드로써 n-가 p기판위에 형성하는 접촉접합을 주로 사용하고 있다.

As shown in fig. 1 the cell structure of the general capacitor is made of the structure including the stack, the pin (Fin), or the cylinder etc, the contact bonding which the n- forms on the p upper part of substrate is mainly used as the node of the cell capacitor.

셀캐패시터에 저장되는 정보의 손실은 주로 이 접촉접합을 통하여 발생하게 되는데 하부전극(40)을 형성하기 위해 콘택식각하고 그위에 이온을 주입시키면서 물리적인 충격에 의한 손상으로 #39#A#39#와 같은 손상이 발생하여 이곳으로 접합손실이 발생된다. 이 손실은 DRAM의 경우에는 리플래쉬특성에 큰 영향을 준다는 문제점이 있다.

While it contact-etches the loss of the information stored in the cell capacitor is mainly generated through this contact bonding but the bottom electrode (40) is formed and ion is injected in the upper part the damage like the 'A' occurs by the damage by the physical impact and the junction loss comes to this place. In case of this loss is DRAM, it has the problem that it affects the refresh characteristic big.

또한 이온주입에 의한 물리적 충격으로 손상된 기판(10)을 큐링(Curing)하는 공정으로 고온에서 어닐링을 수행하는데 일반적인 방법에서는 하부전극(40)이 완성된 뒤에 행하기 때문에 충분한 큐링이 이루어지지 않는다는 문제점이 있다.

Moreover, it has the problem that enough curing is not comprised because it performs the annealing to the process of having the damaged substrate (10) as the physical impact by the ion implantation with the curing (Curing) in the high temperature but it performs after the bottom electrode (40) is completed in the general method.

발명의 내용

Summary of Invention

GF Exhibit 1124 - 2090/2704

발명의 효과

상기한 바와 같이 본 발명은 반도체장치에서 캐패시터의 하부전극을 접촉시키기 위한 콘택형성시 콘택식각과 접합저항을 줄이기 위한 이온주입시 발생되는 손상을 줄이기 위해 콘택형성후 장벽층을 형성하고 이온주입후 열공정을 통해 발생된 손상을 큐링시킴으로서 접합손실을 줄일수 있어 캐패시터의 리플래쉬 특성을 향상시켜 생산수율의 개선 및 제품의 수명은 연장시킬 수 있다는 이점이 있다.

Effects of the Invention

As described above, the invention has the advantage that in the semiconductor device, the damage which forms barrier after the contact forming in order to reduce the generated damage in the ion implantation for reducing the contact etch and junction resistance in the contact forming for contacting the bottom electrode of the capacitor and , is generated after the ion implantation through the thermal process is cured the junction loss can be reduced and the refresh characteristic of the capacitor is improved and the improvement of the production yield and lifetime of the product can lengthen.

기술적 과제

본 발명은 상기와 같은 문제점을 해결하기 위해 창작된 것으로서, 본 발명의 목적은 반도체장치의 캐패시터 제조공정시 캐패시터의 하부전극을 위한 콘택식각에 의한 손상과 콘택저항을 감소시키기 위한 이온주입공정시의 손상을 줄이기 위해 콘택식각후 산화막을 형성하고 이온주입후 열공정을 추가하여 손상으로 인한 접합누설의 발생을 줄이도록 하는 반도체장치의 캐패시터 제조방법을 제공함에 있다.

Technical Task

The invention provides the object of the present invention is the damage by the contact etch for the bottom electrode of the capacitor in the capacitor of a semiconductor device manufacturing process to solve problems described in the above, it is created and the capacitor of a semiconductor device manufacturing method forming the contact etch post oxide in order to reduce the damage in the ion implantation process for reducing the contact resistance and , adds the thermal process after the ion implantation and reduces the generation of the junction leakage due to the damage.

발명의 구성 및 작용

상기와 같은 목적을 실현하기 위한 본 발명은 캐패시터의 하부전극을 접합시키기 위한 콘택식각을 행하는 단계와, 콘택식각후 콘택플러그 이온주입을 행하는 단계를 포함하여 이루어진 반도체장치의 캐패시터 제조방법에 있어서, 상기 콘택식각후 장벽층을 형성하는 단계와, 콘택플러그 이온주입후 열공정하는 단계를 더 포함하여 이루어지는 것을 특징으로 한다.

Structure & Operation of the Invention

The step of forming barrier after the contact etch for realizing the above-mentioned purpose, and the step of processing heat after the contact plug ion implantation further are included and comprises.

상기와 같은 방법에 의하여 제조된 캐패시터는 콘택식각에 의한 손상과 장벽층에 의해 이온주입시 발생되는 손상을 방지할 수 있고 열공정을 통해 손상된 기판을 큐링시킬 수 있어 캐패시터에 저장된 전하의 손실을 방지하여 리플래쉬의 특성을 향상시킬 수 있게 된다.

The substrate which can prevent the generated damage and in which the capacitor manufactured with the above-mentioned method is damaged with the damage by the contact etch and barrier in the ion implantation through the thermal process can be cured and the loss of the electric charge stored in the capacitor is prevented and the property of the reflash is improved.

이하, 본 발명의 바람직한 실시예를 첨부된 도면을 참조하여 설명한다. 또한 본 실시예는 본 발명의 권리범위를 한정하는 것은 아니고, 단지 예시로 제시된 것이며 종래 구성과 동일한 부분은 동일한 부호 및 명칭을 사용한다.

Hereinafter, referring to the figure the preferred embodiment of the invention is illustrated. Moreover, this embodiment does not limit the scope of protection of the present invention and while being only presented as an example the same part as the conventional composition uses the same reference numbers and name.

도2 내지 도3은 본 발명의 방법에 따라 종래의 방법에 추가되는 공정을 단계적으로 나타낸 단면도이다.

Figures 2 through 3 are the cross-sectional view showing the process according to the method of the invention, it is added to the conventional method.

도2는 기판(10)위에 형성된 캐패시터의 하부전극(40)부분을 나타낸 것으로서 기판(10)에 격리산화막(15)을 형성하고 트랜지스터(20)를 형성한후 BPSG층(25)을 증착한 다음 캐패시터를 형성하기 위해 트랜지스터(20)의 소오스/드레인(22) 영역

Figure 2 is a cross-sectional view showing the state that forms the barrier (50) after it forms the contact hole on the source / drain (22) domain of the transistor (20) in order to form the capacitor after with it shows

GF Exhibit 1124 - 2091/2704

에 콘택홀을 형성한 다음 장벽층(50)을 형성한 상태를 나타낸 단면도이다.

the bottom electrode (40) part of the capacitor formed on the substrate (10) it forms the Isolation oxide film (15) on the substrate (10) and it deposits the transisto r (20) the boronphosphorus silicate glass layer (25) aft er doing the formation.

장벽층(50)은 산화공정으로 50Å정도의 두께로 형성된 산화막 층이다.

The barrier (50) is the oxide layer formed into the thickness of about 50Å to the oxidation process.

도3은 도2의 결과물에 접촉저항을 줄이기 위한 이온주입공정으로 인(PHOSPHORUS 31)이 주입된 상태를 나타낸 단면도이다.

Figure 3 is a cross-sectional view showing the state where the phosphorus (PHOSPHORUS 31) is injected in the outcome of fig. 2 to the ion implantation process fo r reducing the constant resistance.

그런다음 900℃의 질소분위기에서 약 30분동안 열공정을 통해 콘택식각시 발생된 손상과 이온주입시 발생된 손상을 큐링시킨다.

Next, in the nitrogen atmosphere of 900℃, the damage generated for about 30 minute through the thermal pro cess in the contact etch and the damage generated in the ion implantation are cured.

이후 공정은 종래의 반도체장치의 캐패시터 제조방법과 동일하게 진행된다. 본 실시예에서는 콘택형성시와 이온주입시 발생되는 손상을 큐링하고 다음 공정을 진행하기 때문에 접합손실을 줄일 수 있게된다.

Then, the process is progressed identically with the conventional capacitor of a semiconductor device man ufacturing method. In the present preferred embodimen t, because the damage generated in the contact formi ng time and ion implantation is cured and the next proc ess is progressed the junction loss is reduced.

도면에 대한 간단한 설명

도1은 일반적인 방법에 의한 반도체장치의 캐패시터 제조공정중 캐패시터의 하부전극의 접합을 위한 콘택형성공정을 나타낸 단면도이다.

도2 내지 도3은 본 발명에 의한 방법으로 반도체장치의 캐패시터 제조공정중 캐패시터의 하부전극의 접합을 위한 콘택형성공정을 나타낸 단면도이다.

- 도면의 주요부분에 대한 부호의 설명 -

10 : 기판 30 : 스페이서
40 : 하부전극 50 : 장벽층

Brief explanation of the drawing

Figure 1 is a cross-sectional view showing the contact forming process for the junction of the bottom electrod e of the capacitor among the capacitor of a semicondu ctor device manufacturing process by the general meth od.

Figures 2 through 3 are the cross-sectional view showing the contact forming process for the junction o f the bottom electrode of the capacitor among the met hod according to the invention the capacitor of a semi conductor device manufacturing process.

Description - of the denotation about the main part of - drawing.

10: substrate 30: spacer.
40: bottom electrode 50: barrier.

Disclaimer

본 문서는 특허 및 과학기술문헌 전용의 첨단 자동번역 시스템을 이용해 생성되었습니다. 따라서 부분적으로 오역의 가능성이 있으며, 본 문서를 자격을 갖춘 전문 번역가에 의한 번역물을 대신하는 것으로 이용되어서는 안 됩니다. 시스템 및 네트워크의 특성때문에 발생한 오역과 부분 누락, 데이터의 불일치등에 대하여 본원은 법적인 책임을 지지 않습니다. 본 문서는 당사의 사전 동의 없이 권한이 없는 일반 대중을 위해 DB 및 시스템에 저장되어 재생, 복사, 배포될 수 없음을 알려드립니다.
(The document produced by using the high-tech machine translation system for the pate nt and science & technology literature. Therefore, the document can include the mistrans lation, and it should not be used as a translation by a professional translator. We hold n o legal liability for inconsistency of mistranslation, partial omission, and data generated by feature of system and network. We would like to inform you that the document canno t be regenerated, copied, and distributed by being stored in DB and system for unauthori zed general public without our consent.)

GF Exhibit 1124 - 2092/2704

GF Exhibit 1124 - 2093/2704

(19) 대한민국특허청(KR)
(12) 공개특허공보(A)

(11) 공개번호 특1999-0045323
(43) 공개일자 1999년06월25일

(51) 국제분류코드
H01L 51/40 (2006.01)

(21) 출원번호 10-1998-0049107

(22) 출원일자 1998년11월16일

(30) 우선권주장 97-315682 98-37673 98-109983
1997년11월17일
1998년02월19일
1998년04월20일
일본(JP) 일본(JP) 일본(JP)

(71) 출원인
이데이 노부유끼
소니 가부시끼 가이샤
일본국 도쿄도 시나가와쿠 키타시나가와 6쵸메 7반 35고, 일본

(72) 발명자
하세가와 도시야키
일본국 도쿄도 시나가와구 기다시나가와 6쵸메 7반 35고 소니 가부시키가이샤내, 일본
나카야마 하지메
일본국 도쿄도 시나가와구 기다시나가와 6쵸메 7반 35고 소니 가부시키가이샤내, 일본

(74) 대리인
김재만
박종길

(77) 심사관
없음

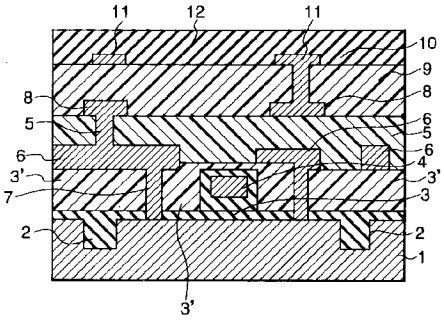
전체 청구항 수 : 총 44 항

(54) 저유전율막을 가지는 반도체 장치 및 그 제조 방법

(57) 요 약

본 발명은 반도체 기판, 이 반도체 기판 위에 형성되는 절연막, 이 절연막 위에 형성되고 유전율비가 3.0 이하인 유전체 유기막과, 이 유전체 유기막 중에 절연막에 접하는 배선층을 포함하고, 배선층의 상면은 유전체 유기막의 상면보다 높은 반도체 장치와, 이러한 반도체 장치의 제조 방법을 제공한다.

대 표 도 - 도 1



This Facsimile Page has been artificially created from KIPO data.

청구의 범위

청구항 1

반도체 기판과,

상기 반도체 기판 상에 형성된 절연막과,

상기 절연막 상에 형성되고 유전율비가 3.0 이하인 제1 유전체막과,

상기 제1 유전체막 상에 형성되고 상기 절연막에 접하는 배선층

을 포함하고,

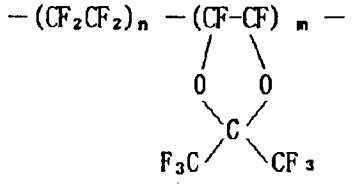
상기 배선층의 상면이 상기 제1 유전체막의 상면보다 높게 형성되는 반도체 장치.

청구항 2

제1항에 있어서, 상기 배선층과 제1 유전체막 상에 형성되고 최소한 3.0의 유전율비를 가지는 제2 유전체막을 추가로 포함하는 반도체 장치.

청구항 3

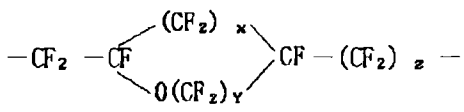
제1항에 있어서, 상기 제1유전체막은 사이클릭 플루오로 레진, 폴리테트라플루오로에틸렌, 플루오르화 에틸렌 프로필렌, 테트라플루오로에틸렌 공중합체, 퍼플루오로알콕시에틸렌, 폴리플루오로비닐리덴, 폴리트리플루오로클로로에틸렌, 플루오로아릴 에테르 레진, 폴리플루오로이미드, 벤조시클로부텐(BCB) 폴리머, 폴리이미드, 아몰퍼스 카본, 모노메틸트리하이드록시실란 (유기 SOG) 축합체, 하기의 식(1)로 표현되는 반복하는 단위 구조를 가지는 폴리머,



(1)

(상기 m, n은 자연수를 나타냄)

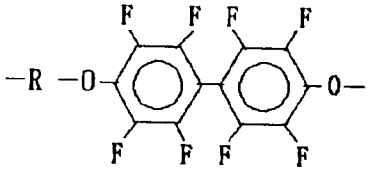
하기의 식(2)로 표현되는 반복하는 단위 구조를 가지는 폴리머,



(2)

(상기 x, y, z은 각각 자연수를 나타냄)

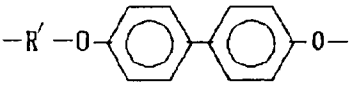
하기의 식(3)으로 표현되는 반복하는 단위 구조를 가지는 폴리머,



(3)

(상기 R은 알킬렌 또는 페닐렌 군을 나타냄)

하기의 식(4)로 표현되는 반복하는 단위 구조를 가지는 폴리머



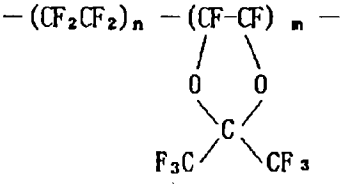
(4)

(상기 R'는 알킬렌 또는 페닐렌 군을 나타냄)

로 이루어지는 군으로부터 선택되는 최소한 하나의 재료로 이루어지는 반도체 장치.

청구항 4

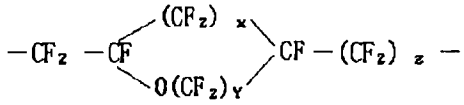
제1항에 있어서, 상기 제2 유전체막은 사이클릭 플루오로 레진, 폴리테트라플루오로에틸렌, 플루오로화 에틸렌 프로필렌, 테트라플루오로에틸렌 공중합체, 퍼플루오로알콕시에틸렌, 폴리플루오로비닐리덴, 폴리트리플루오로클로로에틸렌, 플루오로아릴 에테르 레진, 폴리플루오로이미드, 벤조시클로부텐 (BCB) 폴리머, 폴리이미드, 아몰퍼스 카본, 모노메틸트리하이드록시실란 (유기 SOG) 축합체, 하기의 식(5)로 표현되는 반복하는 단위 구조를 가지는 폴리머,



(5)

(상기 m, n은 자연수를 나타냄)

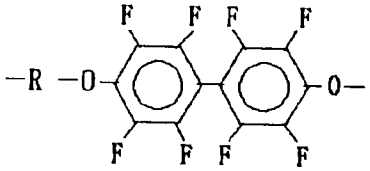
하기의 식(6)으로 표현되는 반복하는 단위 구조를 가지는 폴리머,



(6)

(상기 x, y, z은 각각 자연수를 나타냄)

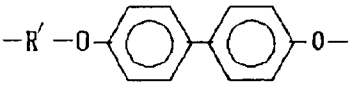
하기의 식(7)로 표현되는 반복하는 단위 구조를 가지는 폴리머,



(7)

(상기 R은 알킬렌 또는 페닐렌 군을 나타냄)

하기의 식(8)로 표현되는 반복하는 단위 구조를 가지는 폴리머



(8)

(상기 R'는 알킬렌 또는 페닐렌 군을 나타냄)

로 이루어지는 군으로부터 선택되는 최소한 하나의 재료로 이루어지는 반도체 장치.

청구항 5

제1항에 있어서, 상기 유전체막 중에 패턴에 대하여 최소한 3배 피치 이상의 배선간격 부분의 더미 배선을 가지는 반도체 장치.

청구항 6

제5항에 있어서, 상기 더미 배선은 최소한 3배 피치 이상의 배선 간격의 부분에 모든 배선 간격이 1 ㎛ 이하가 되도록 형성되는 반도체 장치.

청구항 7

제5항에 있어서, 상기 더미 배선의 아래의 절연막 중에 하층 도전층과 접속되지 않는 더미 콘택트홀을 추가로 포함하는 반도체 장치.

청구항 8

반도체 기판과,

상기 반도체 기판 상에 형성되는 절연막과,

상기 절연막 상에 크세로겔을 함유하는 막과,

상기 크세로겔을 함유하는 막중에 형성되고, 상기 절연막에 접하는 배선층

을 포함하는 반도체 장치.

청구항 9

제8항에 있어서, 상기 배선층의 상면이 상기 크세로겔을 함유하는 막의 상면보다 높게 형성되어 있는 반도체 장치.

청구항 10

제8항에 있어서, 상기 크세로겔을 함유하는 막 중에 패턴에 대하여 최소한 3배 피치 이상의 배선 간격 부분의 상기 크세로겔을 함유하는 막중에 더미 배선을 가지는 반도체 장치.

청구항 11

제10항에 있어서, 상기 더미 배선은 최소한 3배 피치 이상의 배선 간격의 부분에 모든 배선 간격이 1 ㎛ 이하로 되도록 형성되어 있는 반도체 장치.

청구항 12

제10항에 있어서, 상기 더미 배선의 아래의 절연막 중에 형성되고 하층 도전층과 접속되지 않는 더미 콘택트홀을 추가로 포함하는 반도체 장치.

청구항 13

제8항에 있어서, 상기 크세로겔을 함유하는 막위 또는 막아래에 실란 커플링제를 함유하는 막을 추가로 포함하는 반도체 장치.

청구항 14

제8항에 있어서, 상기 크세로겔을 함유하는 막이 배선 패턴에 대하여 3배 피치 이하의 배선 간격 부분의 상기 절면막의 위에 형성되어 있는 반도체 장치.

청구항 15

반도체 기판과,

상기 반도체 기판 상에 형성된 절연막과,

상기 절연막 상에 형성되고 유전율비가 3.0 이하인 제1 유전체막과,

상기 제1 유전체막 상에 크세로겔을 함유하는 막과,

상기 크세로겔을 함유하는 막 상에 형성되고 유전율비가 3.0 이하인 제2 유전체막과,

상기 크세로겔을 함유하는 막중에 형성되고 상기 절연막에 접하는 배선층

을 포함하는 반도체 장치.

청구항 16

제15항에 있어서, 상기 배선층의 상면이 상기 크세로겔을 함유하는 막의 상면보다 높게 형성되는 반도체 장치.

청구항 17

제15항에 있어서, 상기 유전율비가 3.0 이하인 제2 유전체막 중에 형성되고 배선들을 접속하기 위한 콘택트홀을 추가로 포함하는 반도체 장치.

청구항 18

제15항에 있어서, 상기 크세로겔을 함유하는 막 중에 배선 패턴에 대하여 최소한 3배 피치 이상의 배선 간격부분의 더미 배선을 가지는 반도체 장치.

청구항 19

제18항에 있어서, 상기 더미 배선은 최소한 3배 피치 이상의 배선 간격의 부분에 모든 배선 간격이 1 ㎛ 이하가 되도록 형성되는 반도체 장치.

청구항 20

제15항에 있어서, 상기 더미 배선의 아래의 절연막 중에 형성되고 하층 도전층과 접속되지 않는 더미 콘택트홀을 추가로 포함하는 반도체 장치.

청구항 21

제15항에 있어서, 상기 크세로겔을 함유하는 막위 또는 막아래에 실란 커플링제를 함유하는 막을 추가로 포함하는 반도체 장치.

청구항 22

반도체 기판 상에 절연막을 형성하는 공정과,

상기 절연막 위에 유전율비가 3.0 이하인 유전체막을 형성하는 공정과,

상기 유전체막 위에 무기막을 형성하는 공정과,

상기 무기막에 배선층을 형성하기 위한 패턴을 형성하는 공정과,

상기 배선층을 전체 표면상에 형성하는 공정과,

상기 배선층의 표면을 연마하는 공정과,

상기 무기막을 제거하는 공정

을 포함하는 반도체 장치의 제조 방법.

청구항 23

제22항에 있어서, 상기 배선층의 상면을 연마하는 공정이 화학적 기계적 연마(CMP)법에 의한 연마 공정인 반도체 장치의 제조 방법.

청구항 24

반도체 기판 상에 절연막을 형성하는 공정과,

상기 절연막의 위에 유전율비가 3.0 이하인 유전체막을 형성하는 공정과,

상기 유전체막 위에 무기막을 형성하는 공정과,

상기 무기막에 배선층을 형성하기 위한 패턴을 형성하는 공정과,

상기 배선층을 전체 표면상에 형성하는 공정과,

상기 배선층의 상면을 연마하는 공정과,

상기 무기막을 제거하는 공정과,

배선 패턴에 대하여, 상기 유전체막 중에 최소한 3배 피치 이상의 배선 간격 부분의 더미 배선을 형성하는 공정

을 포함하는 반도체 장치의 제조 방법.

청구항 25

제24항에 있어서, 상기 배선층의 상면을 연마하는 공정이 화학적 기계적 연마(CMP)법에 의한 연마 공정인 반도체 장치의 제조 방법.

청구항 26

반도체 기판 상에 절연막을 형성하는 공정과,

상기 절연막 위에 유전율비가 3.0 이하인 유전체막을 형성하는 공정과,

상기 유전체막 위에 무기막을 형성하는 공정과,

상기 무기막에 배선층 및 더미 배선층을 형성하기 위한 패턴을 형성하는 공정과,

상기 배선층 및 더미 배선층을 전체 표면상에 형성하는 공정과,

상기 배선층과 더미 배선층의 상면을 연마하는 공정과,

상기 무기막을 제거하는 공정

을 포함하는 반도체 기판의 제조 방법.

청구항 27

제26항에 있어서, 상기 배선층의 상면을 연마하는 공정이 화학적 기계적 연마(CMP)법에 의한 연마 공정인 반도체 장치의 제조 방법.

청구항 28

반도체 기판 상에 절연막을 형성하는 공정과,

상기 절연막 위에 유전율비가 3.0 이하인 유전체막을 형성하는 공정과,

상기 유전체막 위에 무기막을 형성하는 공정과,

상기 무기막에 배선층 및 더미 배선층을 형성하기 위한 패턴을 형성하는 공정과,

상기 배선층 및 더미 배선층을 전체 표면상에 형성하는 공정과,

상기 배선층의 상면을 연마하는 공정과,

상기 무기막을 제거하는 공정과,

상기 절연막 중에 상층 배선과 하층 도전층을 접속하기 위한 콘택트홀, 및 상기 더미 배선의 아래의 절연막 중에 하층 도전층과 접속되지 않는 더미 콘택트홀을 형성하는 공정

을 포함하는 반도체 장치의 제조 방법.

청구항 29

제28항에 있어서, 상기 배선층의 상면을 연마하는 공정이 화학적 기계적 연마(CMP)법에 의한 연마 공정인 반도체 장치의 제조 방법.

청구항 30

제28항에 있어서, 상기 무기막에 배선층 및 더미 배선층을 형성하기 위한 패턴을 형성하는 공정이, 배선 패턴 및 더미 배선 패턴에 대하여 최소한 3배 피치 이상의 배선 간격 부분에 상기 더미 배선을 형성하기 위한 패턴을 동시에 형성하는 공정인 반도체 장치의 제조 방법.

청구항 31

반도체 기판 상에 절연막을 형성하는 공정과,

상기 절연막 위에 유전율비가 3.0 이하인 유전체막을 형성하는 공정과,

상기 유전체막 위에 크세로겔을 함유하는 막을 형성하는 공정과,

상기 크세로겔을 함유하는 막 상에 무기막을 형성하는 공정과,

상기 무기막에 배선층을 형성하기 위한 패턴을 형성하는 공정과,

상기 배선층을 전체 표면상에 형성하는 공정과,

상기 배선층의 상면을 연마하는 공정과,

상기 무기막을 제거하는 공정

을 포함하는 반도체 장치의 제조 방법.

청구항 32

제31항에 있어서, 상기 배선층의 상면을 연마하는 공정이 화학적 기계적 연마(CMP)법에 의한 연마 공정인 반도체 장치의 제조 방법.

청구항 33

제31항에 있어서, 상기 유전체막 상에 크세로겔을 함유하는 막을 형성하는 공정이, 상기 배선 패턴에 대하여 3배 피치 이하의 배선 간격 부분에 상기 크세로겔을 함유하는 막을 형성하는 공정인 반도체 장치의 제조 방법.

청구항 34

제31항에 있어서, 상기 크세로겔을 함유하는 막을 형성하는 공정의 전 또는 후에, 실란 커플링제를 함유하는 막을 형성하는 공정을 추가로 포함하는 반도체 장치의 제조 방법.

청구항 35

반도체 기판 상에 절연막을 형성하는 공정과,

상기 절연막 위에 유전율비가 3.0 이하인 유전체막을 형성하는 공정과,

상기 유전체막 위에 크세로겔을 함유하는 막을 형성하는 공정과,

상기 크세로겔을 함유하는 막 상에 무기막을 형성하는 공정과,

상기 무기막에 배선층 및 더미 배선층을 형성하기 위한 패턴을 형성하는 공정과,

상기 배선층 및 더미 배선층을 전체 표면상에 형성하는 공정과,

상기 배선층 및 더미 배선층의 상면을 연마하는 공정과,

상기 무기막을 제거하는 공정

을 포함하는 반도체 장치의 제조 방법.

청구항 36

제35항에 있어서, 상기 배선층의 상면을 연마하는 공정이 화학적 기계적 연마(CMP)법에 의한 연마 공정인 반도체 장치의 제조 방법.

청구항 37

제35항에 있어서, 상기 무기막 상에 배선층 및 더미 배선층을 형성하기 위한 패턴을 형성하는 공정이, 상기 무기막 상에 배선 패턴 및 배선 패턴에 대하여 최소한 3배 피치 이상의 배선 간격 부분에 배선층 및 더미 배선층을 형성하기 위한 패턴을 동시에 형성하는 공정인 반도체 장치의 제조 방법.

청구항 38

제35항에 있어서, 상기 유전체막 상에 크세로겔을 함유하는 막을 형성하는 공정이, 상기 배선 패턴에 대하여 3배 피치 이하의 배선 간격 부분에 상기 크세로겔을 함유하는 막을 형성하는 공정인 반도체 장치의 제조 방법.

청구항 39

제35항에 있어서, 상기 크세로겔을 함유하는 막을 형성하는 공정의 전 또는 후에, 실린 커플링제를 함유하는 층을 형성하는 공정을 추가로 포함하는 반도체 장치의 제조 방법.

청구항 40

반도체 기판 상에 절연막을 형성하는 공정과,

상기 절연막 위에 유전율비가 3.0 이하인 유전체막을 형성하는 공정과,

상기 유전체막 위에 크세로겔을 함유하는 막을 형성하는 공정과,

상기 크세로겔을 함유하는 막 상에 무기막을 형성하는 공정과,

상기 무기막에 배선층 및 더미 배선을 형성하기 위한 패턴을 형성하는 공정과,

상기 배선층 및 더미 배선층을 전체 표면상에 형성하는 공정과,

상기 배선층 및 더미 배선층의 상면을 연마하는 공정과,

상기 무기막을 제거하는 공정과,

상기 절연막 중에 상층 배선과 하층 도전층을 접속하기 위한 콘택트홀, 및 상기 더미 배선의 아래의 절연막 중에 하층 도전층과 접속되지 않는 더미 콘택트홀을 형성하는 공정

을 포함하는 반도체 장치의 제조 방법.

청구항 41

제40항에 있어서, 상기 배선층의 상면을 연마하는 공정이 화학적 기계적 연마(CMP)법에 의한 연마 공정인 반도체 장치의 제조 방법.

청구항 42

제40항에 있어서, 상기 무기막 상에 배선층 및 더미 배선층을 형성하기 위한 패턴을 형성하는 공정이, 상기 무기막 상에 배선 패턴 및 배선 패턴에 대하여 최소한 3배 피치 이상의 배선 간격 부분에 더미 배선층을 형성하기 위한 패턴을 동시에 형성하는 공정인 반도체 장치의 제조 방법.

청구항 43

제40항에 있어서, 상기 유전체막 상에 크세로겔을 함유하는 막을 형성하는 공정이, 상기 배선 패턴에 대하여 3배 피치 이하의 배선 간격 부분에 상기 크세로겔을 함유하는 막을 형성하는 공정인 반도체 장치의 제조 방법.

청구항 44

제40항에 있어서, 상기 크세로겔을 함유하는 막을 형성하는 공정의 전 또는 후에, 실란 커플링제를 함유하는 막을 형성하는 공정을 추가로 포함하는 반도체 장치의 제조 방법.

명세서

발명의 명칭

저유전율막을 가지는 반도체 장치 및 그 제조 방법

도면의 간단한 설명

도 1은 본 발명인 반도체 장치의 제1 실시예를 도시한 도면이고,

도 2a 내지 도 2f는 본 발명의 제2 실시예에 따른 반도체 장치의 제조 방법의 주요부분을 나타내는 단면도이고, 여기서,

도 2a는 실리콘 반도체 기판 상에 산화 실리콘막을 형성한 도면이고,

도 2b는 p웰 영역을 형성한 도면이고,

도 2c는 p웰 영역을 형성한 후, 소자 분리 영역을 형성하기 위한 패터닝을 수행한 도면이고,

도 2d는 소자 분리 영역을 형성하기 위한 패터닝을 수행한 후, 로코스(LOCOS)법에 따라, 소자 분리막을 형성한 도면이고,

도 2e는 산화 실리콘막을 형성한 후, 게이트 전극을 형성하고, n+ 영역과 p+영역을 형성한 도면이고,

도 2f는 n+ 영역과 p+ 영역을 형성한 후, 전체면에 저유전율막을 형성한 도면이고,

도 2g는 전체면에 저유전율막을 형성한 후, 산화 실리콘막을 형성하고, 배선층을 형성하기 위한 패터닝을 수행한 도면이고,

도 2h는 배선층을 형성하기 위한 패터닝을 수행한 후, 포토 에칭으로 배선홈과 콘택트홀을 형성한 도면이고,

도 2i는 배선층을 형성하기 위한 패터닝을 수행한 후, 포토 에칭으로 배선홈과 콘택트홀을 형성하고, 알루미늄을 전체면에 퇴적시키고, CMP법에 의해 배선을 형성한 도면이고,

도 2j는 배선을 형성한 후, 전체면에 패시베이션막을 형성한 도면이다.

도 3a 내지 도 3f는 본 발명의 제3 실시예에 따른 반도체 장치의 제조 방법의 주요 부분을 나타내는 단면도이고, 여기서,

도 3a는 실리콘 반도체 기판 상에 산화 실리콘막을 형성하고, 그 위에 저유전율막을 형성하고, 다시 그 위에 산화 실리콘막을 형성한 도면이고,

도 3b는 산화 실리콘막을 형성한 후 레지스트막을 이용하여 배선을 위한 패터닝을 수행한 도면이고,

도 3c는 배선을 위한 패터닝을 수행한 후, 포토 에칭으로 콘택트홀을 형성한 도면이고,

도 3d는 콘택트홀을 형성한 후, 전체면에 동을 퇴적한 도면이고,

도 3e는 동을 퇴적한 후, CMP법에 의해 배선층을 형성한 도면이고,

도 3f는 패시베이션막으로서 저유전율막을 형성한 도면이다.

도 4a 내지 도 4i는 본 발명의 제4 실시예에 따른 반도체 장치의 제조 방법의 주요 부분을 나타내는 단면도이고, 여기서,

도 4a는 실리콘 반도체 기판 상에 산화 실리콘막을 형성하고, 저유전율막을 형성한 후, 배선과 더미 배선을 형성하고, 제2 저유전율막을 형성한 도면이고,

도 4b는 제2 저유전율막을 형성한 후, 레지스트를 사용하여 포토 에칭법에 의해 콘택트홀을 형성한 도면이고,

도 4c는 콘택트홀을 형성한 후, 해당 콘택트홀에 금속(W)을 매입한 도면이고,

도 4d는 콘택트홀에 금속(W)을 매입한 후, 전체면에 질화 실리콘막을 형성한 도면이고,

도 4e는 질화 실리콘막을 형성한 후, 레지스트를 사용하여 제2 배선층을 형성하기 위한 패터닝을 수행한 도면이고,

도 4f는 제2 배선층을 형성하기 위한 패터닝을 수행한 후, 포토 에칭에 의해 제2 배선층을 형성한 도면이고,

도 4g는 제2 배선층을 형성한 후, 전체면에 알루미늄막을 형성한 도면이고,

도 4h는 전체면에 알루미늄막을 형성한 후, CMP법에 의해 제2 금속배선을 형성한 도면이고,

도 4i는 제2 금속배선을 형성한 후, 패시베이션막을 형성한 도면이다.

도 5a 내지 도 5f는 본 발명의 제5 실시예에 따른 반도체 장치의 제조 방법의 주요 부분을 나타낸 단면도이고, 여기서,

도 5a는 반도체 기판 상에 콘택트 플러그를 형성한 후, 저유전율막을 형성한 도면이고,

도 5b는 제1 배선층을 형성하고, 그 위에 무기막을 형성한 도면이고,

도 5c는 제2 저유전율막을 형성한 도면이고,

도 5d는 제2 저유전율막(유기막) 내에 제2 콘택트홀 형성한 도면이고,

도 5e는 크세로겔을 함유하는 막을 형성한 후, 제2 배선층을 형성한 도면이고,

도 5f는 패시베이션막을 형성한 도면이다.

도 6a 내지 도 6f는 본 발명의 제6 실시예에 따른 반도체 장치의 제조 방법의 주요 부분을 나타낸 단면도이고, 여기서,

도 6a는 반도체 기판 상에 소자 분리막을 형성하고, 층간 절연막을 형성한 도면이고,

도 6b는 전체면에 레지스트막을 형성하고, 콘택트홀 및 더미 콘택트홀을 형성하기 위한 패터닝을 수행한 도면이고,

도 6c는 금속 재료를 채워서 콘택트 플러그 및 더미 콘택트 플러그를 형성한 도면이고,

도 6d는 저유전율 유기막을 형성하고, 그 위에 무기막을 형성한 도면이고,

도 6e는 전체면에 레지스트막을 형성한 후, 제1 배선층 및 더미 배선층을 형성하기 위한 패터닝을 수행한 도면이고,

도 6f는 제1 배선층을 형성한 도면이다.

도 7a 내지 도 7f는 본 발명의 제7 실시예에 따른 반도체 장치의 제조 방법의 주요 부분을 나타낸 단면도이고,

도 7a는 제2 저유전율막을 형성한 도면이고,

도 7b는 무기막을 형성한 후, 전체면에 레지스트막을 형성한 후, 비아 콘택트홀 및 더미 비아 콘택트홀을 형성하기 위한 패터닝을 수행한 도면이고,

도 7c는 비아 콘택트 플러그 및 더미 비아 콘택트 플러그를 형성한 도면이고,

도 7d는 제3 저유전율막을 형성하고, 그 위에 무기막을 형성한 도면이고,

도 7e는 레지스트막을 형성한 후, 제2 배선층 및 더미 배선층을 형성하기 위한 패터닝을 수행한 도면이고,

도 7f는 제2 배선층 및 더미 배선층을 형성한 도면이다.

도 8a 내지 도 8c는 본 발명의 제8 실시예에 따른 반도체 장치의 제조 방법의 주요 부분을 나타낸 단면도이고, 여기서,

도 8a는 제1 배선층을 형성한 도면이고,

도 8b는 무기막을 형성한 후, 전체면에 레지스트막을 형성하고, 더미 배선층을 형성하기 위한 패터닝을 수행한 도면이고,

도 8c는 더미 배선층을 형성한 도면이다.

도 9는 더미 리드선과 금속 리드선을 가지는 종래의 반도체 장치의 단면도이다.

[부호의 설명]

1, 13,30,37,50,62,81,87 : 반도체 기판

2, 19, 63, 82 : 소자 분리막, 3: 게이트 절연막, 4, 21 : 게이트 전극,

5, 9, 24, 29, 32, 36, 39, 41, 53, 57, 68, 73, 78, 94 : 저유전율막

6, 8, 11, 28, 35, 40, 48, 54, 60, 71, 81, 85, 91 : 배선층

7, 10, 27, 44, 52, 58, 66, 76, 84 : 콘택트홀

12, 49, 61 : 패시베이션막, 14, 20, 25, 31, 33, 38 : 산화 실리콘막

15, 18, 26, 34, 43, 46, 65, 70, 75, 80, 89 : 레지스트막

16 : p웰, 17, 45 : 질화 실리콘막, 22 : p+ 영역 23 : n+ 영역

42, 72, 82, 90 : 더미 배선층, 47 : 알루미늄막, 51 : 절연막

59 : 크세로겔을 함유하는 막, 3', 64, 74, 79 : 무기막, 92 : 기판

93 : 더미 리드선, 94 : 금속 리드선, 95 : 전열층

96 : 저유전율재료, 97 : 전열성 절연층

발명의 상세한 설명

이 발명은 저유전율막을 층간 절연막으로서 사용한 반도체 장치의 형성 방법 및 반도체 장치의 구조에 관한 것으로, 특히, 0.25㎛ 룰(rule) 이하의 디바이스 프로세스에 사용될 수 있는 다층 배선 형성 기술에 관한 것이다.

근년의 반도체 장치의 미세화에 따라, 배선의 미세화, 배선 피치(pitch)의 축소화가 필요되고 있다. 또, 동시에, 저소비 전력화 및 고속화 등의 요구에 따라서, 층간 절연막의 저유전율화도 요구되고 있다. 특히, 로직(logic)계의 디바이스에서는, 미세 배선에 의한 저항 상승, 배선 용량의 증가가 디바이스의 스피드 열화로 이어짐으로써, 미세하고 또한 저유전율막을 층간 절연막으로 하는 다층 배선이 요구불가결이다.

따라서, 배선폭의 미세화, 피치의 축소화는 배선 자체의 종횡비를 크게 할 뿐만 아니라, 배선간의 스페이스의 어스펙트비(aspect ratio)를 크게 하고, 결과로서 세로로 가늘고 긴 미세 배선을 형성하는 기술, 미세한 배선간을 층간막으로 매입하는 기술 등에 부담이 걸리고, 프로세스를 복잡하게 함과 동시에 프로세스의 수의 증대를 초래한다.

이러한 문제를 해결하는 것으로서, 종래에, 비아와 배선홈을 알루미늄 리플로우 스퍼터링(reflow sputtering)으로 동시에 매입하고, CMP (Chemical Mechanical Polishing) 법에 의해 표면의 알루미늄을 연마하는 이른바 다마신(damascene) 프로세스가 알려져 있다.

이 다마신 프로세스는 높은 아스펙트비의 알루미늄 배선을 에칭으로 형성하는 것도, 배선간의 좁은 간격을 층간막으로 매입할 필요도 없고, 대폭으로 프로세스수를 줄이는 것이 가능하다. 이 프로세스는 배선 어스펙트비가 높게 되는 만큼, 그리고 배선 총수가 증대하는 만큼, 토탈 코스트의 삭감에 기여하게 된다. 또한, 층간 절연막의 저유전율화는 배선간의 용량을 저감하는 것이 기득(期得)된다.

그러나, 유전율비가 작은 재료로 이루어진 막은, 종래의 디바이스에 사용되는 실리콘 산화막과는 크게 다르고, 그 프로세스 기술은 아직 개발되지 않았다. 따라서, 그 실용화가 요구되고 있다.

또한, 최근에 이르러, 유전율비가 2.0 이하가 기득될 수 있는 재료로서, 크세로겔(xerogel)을 반도체 장치에 응용하는 것이 주목되고 있다.

본 기술에 관련하는 것으로서, 특개 평8-70005호 공보에는, 도 9에 보여진 바와 같이, 금속 리드선(94)의 신뢰성을 높이는 방법으로서, 저유전율 재료(96) 중에 열확산용 더미 리드선(93)을 설치하는 구조가 개시되어 있다. 이 구조는, 기판(92)상에 알루미늄 합금 등으로 이루어진 금속 리드선(94)과, 최소한 금속 리드선(94) 사이에 공극, 실리카-에어로겔, 유기 SOG, 플루오로 산화 실리콘 등으로 이루

어진 저유전율 재료(96)와, 금속 리드선(94) 및 저유전율 재료(96)상에 데포지트(deposite)된 AlN, Si_3N_4 와 AlN과의 적층체 등으로 이루어진 전열성 절연층(97)과, 금속 리드선(94)에 근접한 알루미늄 합금 등으로 이루어진 더미(dummy) 리드선(93)을 가진다.

이 구조는, 금속 리드선(94)으로부터의 열은, 열을 확산할 수 있는 더미 리드선(93) 및 저유전율 재료보다 열전도도가 20% 높고, 바람직하게는 Si_3N_4 보다 20% 높은 열전도도를 가진 AlN 등의 절연 재료로 이루어진 전열성 절연층(97)에 이동될 수 있다. 이러한 구조로 하는 것에 의하여, 선간(또는 리드선간)의 배선 용량을 감소시키고, 또한, 저유전율 재료의 열전도도의 저하에 따라 높은 어스펙트비의 금속 리드선을 사용하는 경우에 문제가 되는, 줄(joule) 열효과에 의한 금속 리드선 파손 등을 방지하여 신뢰성이 높은 금속 리드선을 가지는 반도체 장치를 얻도록 하는 것이다.

위에 기술한 다마신(damascene)법은, 배선 패턴을 미리 층간 절연막에 형성해 놓고, 거기에 금속을 매입하고, CMP 법에 의해 금속을 연마하고, 배선을 형성하는 것이다. 종래의 층간 절연막에서는 산화 실리콘막 등의 무기재료를 사용할 수 있었지만 미세화에 따른 용량 증대를 억제하는 목적으로 저유전율의 재료가 채용되고 있다. 저유전율의 재료의 대부분은 유기막이고, 유기막의 막질은 종래의 산화 실리콘막 등의 무기막에 비하여 그 단단함은 1/10□1/100 이므로, 예를 들면 다마신 프로세스에 필요한 단단함이 불충분하다.

유전율비가 작은 물질, 특히 유전율비가 3 이하인 저유전율막 대부분은 유기막이다. 유기막은, 종래의 층간 절연막에 사용될 수 있는 실리콘 산화막에 비하여 부드러운 것이 특징이다. 예를 들면 영(young) 율로 비교하면, 실리콘 산화물이 5□10×10^{10} 에 대하여 유기막을 구성하는 수지는 0.3□0.8×10^{10} 으로 작다.

따라서, 다마신법으로 배선을 형성한 경우, 유기막에 많은 스크래치(scratch) 가 발생하게 된다. 스크래치는 수득율(product yield) 저하의 원인이 된다. 그 때문에, 일반적으로는 실리콘 산화막 또는 질화막을 유기막 상에 형성하지만, 이러한 막은 유전율이 유기막에 비하여 높고, 배선간의 용량이 증대해 버리는 문제가 있다.

그러므로, 다마신 프로세스시에, 산화 실리콘막이나 질화 실리콘막을 병용하는 아이디어가 제안되고 있다. 그러나, 그러한 막은 유전율이 높고, 유기막에 의한 저유전율화의 효과를 반감시켜 버리는 문제가 있다.

또, 유기막은 종래의 반도체 디바이스에 사용되었던 층간 절연막(실리콘 산화막)에 비하여 열전도율이 1/10 정도로 매우 작고, 소자의 열확산에 중대한 영향을 미친다. 즉, 디바이스의 축소화에 따라 단위 면적 정도의 열발생량은 저하하지만, 방열을 위한 경로의 열전도율이 떨어질 수 있다. 따라서, 방열 경로를 고려하는 디바이스 구조가 요구된다.

또한, 크세로겔은 실리카겔(silica gel)이라는 명칭으로 건조제 등에 사용되는 등, 일반적으로 널리 알려진 재료이지만, 반도체 장치에의 응용에는 다양한 신뢰성에 대한 요구가 있고, 현재로서는 반도체 장치에 적용하는 것은 곤란하다. 즉, 크세로겔은 그 체적의 50□90% 가 기포이고, 기계적 강도, 열전도성, 내열성, 내 습성, 층간 밀착성 등에 문제가 있다.

따라서, 이러한 문제를 해결하면서 저유전율의 크세로겔을 응용하는 디바이스 구조가 요구된다.

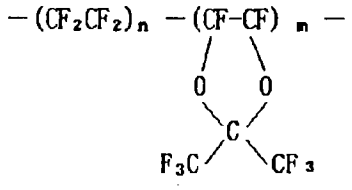
그러므로, 본 발명은 저유전율막을 층간 절연막으로서 사용하는 반도체 장치 및 그 제조 방법을 제공하는 것을 목적으로 한다.

본 발명자는 상기 문제점에 비추어, 저유전율막으로 유기막, 또는 유기막 및 크세로겔을 함유하는 막을 층간 절연막으로서 사용하는 반도체 장치를 다마신법으로 형성하는 방법 및 반도체 장치 및 이 반도체 장치의 제조 방법을 고안한다.

즉, 본 발명은 반도체 기판과, 이 반도체 기판 상에 형성된 절연막과, 유전율비가 3.0 이하인 유전체막과, 이 유전체막에 형성되고 절연막에 접하는 배선층을 가지는 반도체 장치를 제공하며, 상기 배선층의 상면이 상기 유전체막의 상면보다도 높다.

또, 본 발명은, 반도체 기판상에 절연막을 형성하는 공정과, 이 절연막의 위에 유전율비가 3.0 이하인 유전체막을 형성하는 공정과, 이 유전체막의 위에 무기막을 형성하는 공정과, 상기 유전체막에 배선층을 형성하기 위한 패턴을 형성하는 공정과, 상기 배선층을 전체면에 형성하는 공정과, 상기 배선층을 연마하는 공정과, 상기 무기막을 제거하는 공정을 가지는 반도체 장치의 제조 방법이다.

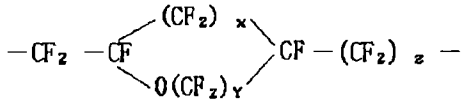
상기 본 발명의 반도체 장치 및 그 제조 방법에 있어서, 상기 유전체막은, 사이클릭 플루오로 레진, 폴리테트라플루오로에틸렌, 플루오로화 에틸렌 프로필렌, 테트라플루오로에틸렌 공중합체, 퍼플루오로알콕시에틸렌, 폴리플루오로비닐리덴, 폴리트리플루오로클로로에틸렌, 플루오로아릴 에테르 레진, 폴리플루오로이미드, 벤조시클로부텐(BCB) 폴리머, 폴리이미드, 아몰퍼스 카본, 모노메틸트리하이드록시실란 (유기 SOG) 축합체, 하기의 식(1)로 표현되는 반복하는 단위 구조를 가지는 폴리머,



(1)

(상기 m, n은 자연수를 나타낸다.)

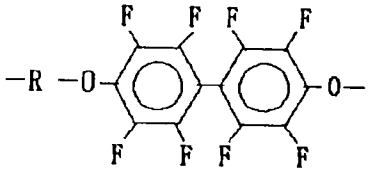
하기의 식(2)로 표현되는 반복하는 단위 구조를 가지는 폴리머,



(2)

(상기 x, y, z은 각각 자연수를 나타낸다.)

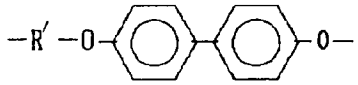
하기의 식(3)으로 표현되는 반복하는 단위 구조를 가지는 폴리머,



(3)

(상기 R은 알킬렌 또는 페닐렌 군을 나타낸다.)

하기의 식(4)로 표현되는 반복하는 단위 구조를 가지는 폴리머,



(4)

(상기 R'는 알킬렌 또는 페닐렌 군을 나타낸다.)

로 이루어지는 군으로부터 선택되는 최소한 하나의 재료로 이루어진다.

그 외, 상기 저유전율막의 재료로서, 상품명, 아몰퍼스 테플론(Amorphous Teflon), CYTPO(Phonetic), FLARE 등의 상품명으로 시판되는 것을 사용할 수 있다.

상기 본 발명의 반도체 장치는 바람직하게는 배선 패턴에 대하여, 최소한 3배 피치 이상의 배선 간격의 부분에, 보다 바람직하게는 모든 배선 간격이 1 ㎛ 이 되도록 더미 배선을 가진다.

상기 본 발명의 반도체 장치는, 바람직하게는 상기 유전체막 상에 크세로겔을 함유하는 층간 절연막을 가지고, 보다 바람직하게는 상기 크세로겔을 함유하는 층간 절연막 상에 실란 커플링(silane coupling)제를 함유하는 층을 가진다.

상기 본 발명의 반도체 장치는, 바람직하게는 상기 더미 배선의 아래의 절연막중에서 또, 하층 도전층과 접하지 않는 더미 콘택트홀을 더 가진다.

상기 하층 도전층으로서는 반도체 기판에 설치된 불순물 확산 영역 또는 하층 배선층을 추천할 수 있다.

상기 본 발명의 반도체 장치의 제조 방법에 있어서, 상기 무기막은 바람직하게는 산화 실리콘막, 플루오로화 실리콘막, 질화 실리콘막, 질화 산화 실리콘막, 실라놀(silanol) 축합체(무기 SOG)막, 포스포러스-도프드(phosphorus-doped) 산화 실리콘막, 보론-도프드(boron-doped) 산화 실리콘막 및 보론-포스포러스-도프드 산화 실리콘막으로 이루어진 군으로부터 선택되는 최소한 하나의 재료로 이루어진다.

상기 본 발명의 반도체 장치의 제조 방법에 있어서, 바람직하게는, 배선 패턴에 대하여, 최소한 3배 피치 이상의 배선 간격의 부분에, 보다 바람직하게는 모든 배선 간격이 1 ㎛ 이하로 되도록 더미 배선을 형성하는 공정을 가진다.

상기 더미 배선을 형성하는 공정은, 바람직하게는 배선 패턴 및, 배선 패턴에 대하여 최소한 3배 피치 이상의 배선 간격의 부분에, 보다 바람직하게는 모든 배선 간격이 1 ㎛ 이하로 되도록 더미 배선 패턴을 동시에 형성하는 공정이다.

상기 배선층을 연마하는 공정은, CMP법에 의해 연마하는 공정인 것이 바람직하다.

상기한 바와 같이, 본 발명은 유전율비가 낮은 유기막 또는 크세로겔을 사용한 반도체 장치를 다마신법으로 형성하는 방법 및 반도체 장치 구조에 관한 것이다.

다마신법은 배선 패턴을 미리 층간 절연막에 형성해 놓고, 거기에 금속을 매입하고, CMP(화학적 기계적 연막)법에 의해 금속을 연마하고, 배선층을 형성하는 것이다.

종래의 층간 절연막에는 산화 실리콘막 등의 단단한 재료를 사용하였다. 그러나, 반도체 장치의 미세화에 따른 용량 증대를 억제하는 목적으로 유기막이 저유전율 재료로서 채용되고 있다.

그러나 유기막 재료는 산화 실리콘막 등의 무기막 등과 크게 다르고, 예를 들면, 다마신 프로세스에 필요한 단단함이 불충분하다. 그 값은 1/10□1/100 이다. 그러므로 본 발명에서는 유기막 상에 무기막을 형성한 후에 배선층을 유기막중에 다마신법에 의해 형성하고, 무기막을 제거하는 방법을 고안하였다.

한편, 유기막은 열전도율이 낮기 때문에, 디바이스 동작시에 발생하는 방열이 문제가 되었다. 그래서 본 발명에서는 배선 형성 프로세스에 있어서, 방열 경로, 즉, 더미 배선층을 유기막중에 다마신법에 의해 형성하는 반도체 장치의 제조 방법을 고안하였다.

또, 본 발명에서는 하층 도전층과 상층 배선을 접속하는 콘택트홀(비아홀) 형성시에, 더미 배선의 아래에 하층 도전층과 접속하지 않는 더미 콘택트홀을 형성하는 것에 의하여 방열 효과를 더 높이는 구조를 제안한다.

또한, 본 발명에서는 저유전율막으로서 주목되고 있는 크세로겔막의 배선 형성 프로세스로의 적용을 고안한다. 크세로겔막은 저유전율막이지만, 유기적 강도, 열전도성, 밀착성, 내수성 등이 종래의 층간 절연막에 비하여 떨어진다. 그래서 본 발명에서는 크세로겔의 적용 개소(箇所)를 가능한 만큼 줄이고, 저유전율막과 무기 절연막을 조합하는 것에 의해 저유전율막이 이루는 효과를 손상하지 않고, 배선간의 용량을 저감하는 구조를 제안하였다. 즉, 크세로겔을 가장 배선 용량이 크게 되는 부분에 사용하고, 그 이외의 장소에는 유기막 무기 저유전율막을 사용하는 것이다.

더욱이, 본 발명은 크세로겔막이 층간 밀착성이 떨어지는 것이 비추어, 크세로겔막의 아래 및/또는 위에 실란 커플링제로 형성되는 막을 설치하는 것도 제안한다.

본 발명에 의하면, 층간 절연막을 유전율비가 3.0 이하인 유전체막(이하 저유전율막이라고 함)으로 하기 때문에, 배선간 용량의 증대가 대폭으로 억제된 미세한 반도체 장치를 제조할 수 있다.

또, 방열을 위한 더미 배선층을, 배선 패턴에 대하여 최소한 3배 피치 이상의 배선 간격의 부분에 설치하는 경우에는, 열전도율이 작은 저유전율막을 사용하는 것에 의한 열확산 효율의 저하를 효과적으로 방지할 수 있다.

상기 더미 배선층의 아래에 더미 콘택트홀을 설치하는 경우에는, 더욱더 열확산 효율을 높일 수 있다.

또한, 본 발명에 의하면, 배선층의 주위(배선층의 좌우), 바람직하게는, 배선 간격이 표준 피치의 3배 이하인 개소에는 유전율비가 매우 작은 크세로겔을 함유하는 막을 사용하고, 또한, 배선간의 콘택트홀의 주위(배선층의 상하)에는 저유전율막을 사용하는 것에 의하여 크세로겔막의 결점을 보충하면서, 배선 용량을 대폭 축소하는 것에 의하여 신뢰성이 높은 미세 구조를 가지는 반도체 장치를 수득률 좋게 제조할 수 있다.

또, 크세로겔을 함유하는 막의 상하에는 실린 커플링제로 이루어진 층을 설치하는 것에 의하여, 층간 밀착성에 뛰어난 반도체 장치를 제조할 수 있다.

이하, 본 발명을 상세히 설명한다.

본 발명의 반도체 장치는 반도체 기판으로서 트랜지스터, 배선 패턴 등이 형성된 n형 또는 p형 불순물이 주입된 실리콘 반도체 기판을 사용할 수 있다.

본 발명에 있어서, 상기 반도체 기판 상에는 절연막이 설치된다. 이 절연막으로서는 예를 들면 산화 실리콘막을 사용할 수 있다. 상기 절연막은 예를 들면 열산화에 의한 방법, CVD(Chemical Vapor Deposition)법, 스퍼터링법 등에 의해 형성할 수 있고, 두께는 300□700㎚ 정도가 바람직하다.

이 절연막의 위에는 저유전율막이 형성된다. 이 저유전율막은 유전율비가 3.0 이하인 것이 바람직하다. 상기 저유전율막으로서는 상기 예시한 유전율비가 3.0 이하인 유전체막, 크세로겔을 함유하는 막 등을 사용할 수 있다.

상기 유전체막은 예를 들면, 고분자의 전구체(precursor)를 스핀코터(spin coater)로 성막하고, 300□500℃로 소성(baking)하는 것에 의해 형성할 수 있다. 또, 아몰퍼스 카본 등의 재료의 경우는, 아세틸렌, 필요에 대응하여 플루오로 카본 가스를 사용하여 플라즈마(plasma) CVD 장치를 사용하여 형성할 수 있다. 상기 유기막의 두께는 통상 300□700㎚ 가 바람직하다. 또, 상기 크세로겔을 함유하는 막은 예를 들면 스핀코터법으로 제조할 수 있다.

본 발명에 있어서는, 상기 유기막 상에, 크세로겔을 함유하는 막을 형성하는 것이 바람직하다. 크세로겔은 건조한 상태에 있는 겔(gel)이고, 예를 들면, 실리카겔을 예시할 수 있다. 보다 구체적으로는 나노포러스(nanoporous)사가 개발한 제품명 Nanoporous Silica 가 있으며 포로스 실리카의 한 종류이다. 본 발명은 특히 이것에 한정되는 것은 아니고, 방향족 등의 비교적 고분자의 알킬(alkyl)기를 가지는 실라놀(silanol) 수지를 도포하고 그것을 겔화시키고 실란 커플링제 또는 수소화 처리를 사용하여 소수 처리 등을 행하여 형성한 것이라면, 어떤 크세로겔도 좋다. 크세로겔은 유전율비가 2.0 이하로 되는 것을 기대할 수 있는 재료이고, 배선간의 용량을 대폭 저감할 수 있다.

본 발명에 있어서, 크세로겔을 함유하는 막을 상기 저유전체막 상, 바람직하게는, 이 저유전체막 상에 있고 최소한 배선 간격이 3배 피치 이하인 영역에 형성한다. 그리고, 바람직하게는 크세로겔을 함유하는 막을 배선층의 좌우에 매입하도록 형성하는 것이 바람직하다.

또, 특히, 복수의 배선층을 가지는 반도체 장치에 있어서, 상기 유전율비가 3.0 이하인 유전체막중에, 배선간을 접속하기 위한 콘택트홀을 가지는 구조로 하는 것이 바람직하다.

반도체 장치를 이와 같은 구조로 하는 것에 의하여, 크세로겔을 함유하는 막의 적용 개소를 가능한 만큼 줄이고, 저유전율의 유기막과 크세로겔을 함유하는 막을 조합하는 것에 의하여 크세로겔막의 상기 결점을 보충하면서, 또한, 저유전율막의 효과를 손상하지 않고 배선간의 용량을 저감하는 것이 가능하게 된다.

또, 본 발명에 있어서는 크세로겔을 함유하는 막은 층간 밀착성이 부족하다. 따라서, 층간 밀착성을 높이기 위하여, 상기 크세로겔을 함유하는 막의 위에, 실란 커플링제를 함유하는 막을 형성하는 것도 바람직하다. 이 실란 커플링제는 예를 들면, 일반식 $RSiX_3$ 또는 $RR'SiX_2$ (R 및 R'는 알킬기, 알콕시기 등을 표시하고, X는 할로겐(halogen) 원자를 표시한다.)로 표시되는 규소화합물을 예시할 수 있다. 이 규소화합물은 분자중에 수소성 부분(R이나 R')과 극성 부분(X)을 가지고, 수소성의 유기막과 극성을 가지는 크세로겔을 함유하는 무기막의 층간 밀착성을 높이고, 박리를 방지하는 역할을 완수한다.

상기 실린 커플링제는 예를 들면, 스핀코터법으로 도포하여 막을 제조할 수 잇다.

다음에, 상기 유전체막, 크세로겔을 함유하는 막 또는 실란 커플링제를 함유하는 막의 위에 무기막을 형성한다. 이 무기막으로서는 산화 실리콘막, 플루오로화 실리콘막, 산화 질화 실리콘막, 실라놀 축합물(무기SOG)막, 포스포러스-도프드 산화 실리콘막, 보론-도프드 산화 실리콘막, 보론-포스포러스-도프드 산화 실리콘막 등을 예시할 수 있다.

상기 무기막의 형성은 통상, 플라즈마 CVD법에 의하지만 환원(還元) 분위기(atmosphere)로 수행할 필요가 있다. 산화 분위기 하에서 CVD를 수행하면, 유기막이 산화되고 막의 박리 등의 현상을 발생시키기 때문에 바람직하지 않다. 예를 들면 산화 실리콘막의 경우, 플라즈마 CVD 장치를 사용하여 실란 가스 및 N_2O 가스의 분위기 하에서 온도 300□500℃에서 성막할 수 있다.

상기 무기막을 퇴적한 후, 레지스트막을 형성하여 배선을 패터닝하고, 포토 에칭(photoetching)에 의하여 최상막의 무기막, 실란 커플링제를 함유하는 막, 크세로겔을 함유하는 막 및 유기막을 예를 들면, 일반적인 마그네트론(magnetron) 방식의 에칭 장치를 사용하여 에칭을 행한다. 에칭은 예를 들면 산화 실리콘 등의 무기막의 경우는 에칭 가스로서 C_2F_6, CO, Ar, O_2 가스를 사용하여 행할 수 있다.

또, 유기막의 경우에는 에칭 가스로서 예를 들면, CHF_3 와 O_2 가스를 사용하여 -10℃ 정도의 저온으로 수행할 수 있다. 이 경우, 상층의 무기막은 저유전율막을 에칭할 때의 마스크로도 사용된다. 또, 유기막을 에칭하는 조건에서는 레지스트막도 에칭된다.

다음에, 이른바 다마신법에 의해 배선층을 형성한다. 배선층 재료로서는 알루미늄, 동, 금, 텅스텐 및 이러한 합금으로 이루어진 군으로부터 선택되는 하나의 종류 이상을 예시할 수 있다. 배선 재료는 예를 들면, 스퍼터링법 또는 CVD법에 의해 형성할 수 있다.

이어서, CMP법에 의해 여분의 금속막을 연마한다. 연마에 사용할 수 있는 연마제로서는, 예를 들면, 알루미나(alumina), 이산화 망간, 실리카계 슬러리(slurry), 식 W_xO_y 로 표시되는 산화 텅스텐, 산화 세슘(cesium), 산화 지르코늄(sirconium), 산화 실리콘 등을 사용할 수 있고, 이러한 연마제에는 필요에 따라 과산화수소, 수산화 칼륨, 암모니아 등이 혼합된다.

완전하게 금속을 연마한 다음, 무기막에 새겨진 스크래치를 제거하기 위하여 CMP법에 의해 50㎚ 정도의 무기막을 연마한다.

다음에, 예를 들면, 플루오린(fluorine) 소원(素源)으로서 C_2F_6, CO 및 아르곤 가스를 사용하여 무기막, 실란 커플링제를 함유하는 막 및 크세로겔을 함유하는 막의 에칭을 행한다. 이 조건에서는 유기막은 거의 에칭되지 않는다.

이와 같은 조작을 행하면, 크세로겔을 함유하는 막을 사용하지 않는 경우에는, 배선층의 상면은 상기 유전체막의 상면보다도 높게 되는 구조가 얻어진다. 배선층의 상면은 상기 유전체막의 상면보다도 높게 되는 것은, 최후에 무기막을 에칭에 의해 제거하기 위한 것이다.

본 발명에 있어서는 또한 배선 패턴에 대하여 최소한 3배 피치 이상의 배선 간격의 부분에, 보다 바람직하게는 배선 간격이 1 ㎛ 이하로 되도록 더미 배선 패턴이 형성되는 것이 바람직하다.

반도체 장치의 배선 패턴에 대하여 3배 피치 이하의 간격의 부분이 있는 경우에는, 열전도도가 작은 유기막, 유기막 및 크세로겔을 함유하는 막을 사용하기 때문에, 동작시에 발생하는 열의 방출 경로가 없으므로, 미세 구조를 가지는 반도체 장치에 오동작 등을 발생시켜서 바람직하지 않다.

한편, 3배 피치 이상의 간격에 더미 배선을 설치하는 것도 가능하지만, 배선 구조가 미세하게 되고, 더미 배선을 설치하는 효과가 떨어지게 된다.

여기서, 상기 피치는 배선이 설계에 있어서 임의 배선의 중심과 이웃하는 배선의 중심과의 거리를 말한다. 반도체 장치는 임의 피치에서 배선층을 형성하지만, 반도체 장치의 다른 부분에서는 이 배선간의 거리가 3배 피치 이상인 개소가 있다. 일반적으로 유기막 및 크세로겔을 함유하는 막은 종래 층간 절연막으로서 사용되었던 산하 실리콘막에 비하여 열전도율이 1/10 정도로 상당히 작다. 본 발명은 이러한 열확산을 위하여 배선 패턴에 대하여 최소한 3배 피치 이상의 배선 간격의 부분에 더미 배선 패턴을 형성하는 것이다.

이 더미 배선 패턴은 상술한 배선의 패터닝 때, 더미를 위한 배선이 패터닝을 동시에 행하고, 통상의 배선의 형성과 동일하게 하여 형성하는 것이 제조 공정상 바람직하다.

GF Exhibit 1124 - 2114/2704

다음에, 상기 기판을 세정한 다음, 다층 배선의 경우에는, 제2 유전막을 200∼400㎚의 두께로 형성한다. 이 유전막으로서는 예를 들면 산화 실리콘막, 질화 실리콘막 이외에, 상술한 재료로 이루어진 유기막, 크세로겔을 함유하는 막 등을 추천할 수 있지만, 반도체의 용량을 작게 하기 위하여 유기막 및 크세로겔을 함유하는 막을 사용하는 것이 바람직하다.

다음에, 상기와 동일하게 하여 제2의 배선층을 형성한 다음, 이상의 조작을 반복하고, 최후에 상층을 패시베이션(passivation) 막으로 피복하는 것에 의하여 배선 가공을 완료한다.

이상과 같이 하여 제조된 본 발명의 반도체 장치의 제조 방법은 다층 배선 구조를 가지는 반도체 장치의 제조에 특히 바람직하게 적용할 수 있다.

다음에, 본 발명의 반도체 장치 및 이 반도체 장치의 제조 방법을 발명의 실시예의 설명에 따라 다시 상세히 설명한다.

제1 실시예

도 1에 본 발명의 반도체 장치의 제1 실시예의 단면도를 나타낸다. 이 반도체 장치는 2층의 배선 구조를 가지는 n채널 MOS형 트랜지스터이다.

이 반도체 장치는 p형 실리콘 반도체 기판(1)상에 트렌치(trench) 법에 의해 형성된 산화 실리콘막(2)으로 이루어진 아이솔레이션(isolation) 영역에, 도시하지 않은 n형 불순물이 이온 주입된 소스 영역과 드레인 영역을 가진다. 그리고, 이 반도체 기판(1)의 위에 게이트 산화막(3)을 통하여 중앙부에 폴리실리콘으로 이루어진 게이트 전극(4)이 설치되고, 게이트 전극(4)은 도시하지 않은 게이트와 접속한다. 또한 그 위에는 유전율비가 3.0 이하인 저유전율막으로 이루어진 층간 절연막(5)이 설치되어 있다.

그리고 또한 그 위에는 알루미늄으로 이루어진 배선층(6)이 설치된다. 이 배선층은 편의상 도면에서 구별하지 않는 통상의 배선층과 방열을 위한 더미 배선층으로 이루어진다. 이 더미 배선층은 배선 패턴에 대하여 최소한 3배 피치 이상의 배선 간격의 부분에 형성된다. 그리고, 상기 배선층은 콘택트홀(7)을 통하여 소스 영역과 드레인 영역과 접속한다.

이 반도체 장치에서는 이 배선층의 상층의 높이는 산화막을 제거하기 위한 상기 저유전율막(5)의 상측의 높이보다 조금 높게 형성되어 있다.

그리고, 상기 저유전율막(5)의 위에는 제2층째의 배선층(8)이 설치되어 있다. 또한, 이것의 상부에는 질화 규소로 이루어진 제2층째의 저유전율막(9)이 설치되고 또한, 비아 콘택트홀(10)을 통하여 제3층째의 배선층(11)이 설치되어 있다. 그리고 그 위에 패시베이션막(12)이 형성된 구조를 가지고 있다.

본 실시예의 반도체 장치는 층간 절연막에 유전율비가 3.0이하인 유전체막을 사용하기 때문에, 배선간 용량의 증대가 억제된 미세한 다층 구조를 가지는 반도체 장치로 되어 있다.

또, 방열을 위한 더미 배선층을 배선 패턴에 대하여 최소한 3배 피치 이상의 배선 간격의 부분에 설치하는 것에 의하여, 열전도율이 작은 저유전율막을 사용하는 것에 의한 열확산 효율의 저하를 효과적으로 방지할 수 있다.

제2 실시예

본 발명의 제2 실시예는 본 발명의 반도체 장치인 CMOS 집적 회로의 제조 방법이다.

우선, 도 2a에 도시한 바와 같이, 포스포러스를 도핑한 n형 실리콘 반도체 기판(13)상에 열산화법에 의해 산화 실리콘막(14)을 형성한다. 다음에, 포토레지스트(15)를 사용하여 산화 실리콘막(14)상에

p-웰(well)의 영역이 되는 패턴을 형성하고, 이온 주입법에 의해 보론(boron)을 실리콘 기판내에 박아 넣음을 수행한다(도2a). 그 후, 도 2b에 도시한 바와 같이, 레지스트막(15)을 제거한다.

다음에, 도 2c에 도시한 바와 같이, 예를 들면, CVD법에 의해 전체면에 질화 실리콘막(17)을 퇴적하고, 포토 레지스트로 소자 분리 영역을 형성한 후, 포토 레지스트의 개공부의 질화 실리콘막(17)을 에칭에 의해 제거하여 개공한다.

다음에, 도 2d에 도시한 바와 같이, 선택적 산화법 (LOCOS 법)에 의해 두꺼운 산화막(19)을 선택적으로 형성한다.

이어서, 도 2e에 도시한 바와 같이, 마스크로서 사용하는 질화 실리콘막(17)과 그 아래의 산화 실리콘막(14)을 에칭에 의해 제거하고, 새로운 산화 실리콘막(20)을 형성하고, 또한 그 위에 예를 들면, CVD법에 의해 폴리 실리콘막을 성장형성하고, 소자 분리의 패터닝과 동일한 방법에 의해 게이트 전극(21)을 형성한다.

또한, p-웰 형성과 동일한 방법으로 이온 주입법에 의해 p-웰 영역(16)에는 비소(砒素) (n+)를, p-웰 영역 이외에는 보론소 (p+)를 실리콘 기판중에 주입하고, 열확산에 의해 n+ 영역(23)과 p+ 영역(22)을 형성한다.

그리고, 도 2f에 도시한 바와 같이, 트랜지스터 등의 소자의 모양을 형성한 후, 그 위에 두께가 500㎚ 정도인 두꺼운 유전율비가 3.0 이하인 유전체막(24)을 형성한다. 이 유전체막(24)의 형성은 예를 들면, 전구체를 스핀코터로 기판 상에 성막하고 그 후, 300□450℃로 소성하는 것에 의해 수행할 수 있다. 또, 유전체막(24)이 아몰퍼스 카본 등인 경우에는 아세틸렌, 필요에 대응하여 플루오로 카본을 사용하여 플라즈마 CVD 장치를 사용하여 성막하고, 300□450℃로 소성하는 것에 의해 수행할 수 있다.

다음에, 도 2g에 도시한 바와 같이, 상기 유기막의 위에 예를 들면, 무기막으로서 산화 실리콘막(25)을 형성한 다음, 레지스트막(26)을 성막하여 각각의 소자와 금속 배선을 접속하기 위한 콘택트홀을 형성하기 위한 패터닝을 행한다. 상기 산화 실리콘막(25)은 예를 들면, 플라즈마 CVD 장치에 의해, 실란 가스 50 sccm, N_2O 가스 1000 sccm의 환원적 분위기 하에서 플라즈마 파워 500W, 압력 10 Torr, 온도 350℃에서 성막할 수 있다.

그 후, 도 2h에 도시한 바와 같이, 콘택트홀(27)을 형성한다. 콘택트홀(27)은 예를 들면 일반적인 마그네트론 방식의 에칭 장치를 사용하여, 최상층의 산화 실리콘막(25), 그 하층의 유기막(24)을 각각 에칭하는 것에 의해 형성한다. 에칭의 조건은 예를 들면, 저유전율막의 경우는 CHF_3 (5 sccm), O_2 (50 sccm), He (200sccm) 가스를 사용하여 RF 플라즈마 파워 500W, -10℃의 저온이고, 산화 실리콘막의 경우는 예를 들면, C_2F_6 (14 sccm), CO (180 sccm), Ar (240 sccm), O_2 (6 sccm) 가스를 사용하여 RF 플라즈마 파워 1500W이다. 이 경우, 상층의 산화 실리콘막(25)은 저유전율막을 에칭할 때의 마스크의 역할도 완수한다.

다음에, 도 2i에 도시한 바와 같이, 다마신법에 의해 배선(28)을 형성한다. 즉, 배선 재료로서 예를 들면, 동을 스퍼터링 장치 또는 CVD 장치에 의해 전체면에 퇴적시키고, 이어서, CMP법에 의해 여분의 금속을 예를 들면 알루미나를 사용하여 연마한다. 이것은 완전하게 여분의 금속을 제거하기 위함과, 산화 실리콘막에 새겨진 스크래치를 제거하기 위한 것이다. 그 후, 산화 실리콘막을 일반적인 마그네트론 방식의 에칭 장치를 사용하여 에칭한다. 이 때의 조건은 예를 들면, C_2F_6 (14 sccm), CO (180 sccm), Ar (240 sccm)이다. 이 조건에서는 유전체막(24)은 거의 에칭되지 않는다.

이와 같이 형성된 금속 배선층(28)의 상면은 산화막(25)을 제거하기 때문에, 유전체막보다도 높게 형성되게 된다.

다음에, 도 2j에 도시한 바와 같이, 기판 표면을 세정한 후, 패시베이션막으로서 산화 실리콘막(29)을 300㎚ 형성한다. 웨이퍼 프로세스의 완료 후, 마운팅(mounting), 본딩(bonding) 프로세스를 수행하는 것에 의해 요구되는 반도체 장치를 제조할 수 있다.

이상 설명한 바와 같이, 본 실시예에 의하면, 저유전율막을 사용하고, 배선간 용량의 증대가 억제된 미세 구조의 반도체 장치를 효율 좋게 제조할 수 있다.

제3 실시예

본 발명의 제3실시예는 패시베이션막으로서 저유전율막을 사용하는 반도체 장치의 제조 방법이다.

먼저, 도 2i에 도시한 것과 동일한 반도체 장치의 중간물이 형성된다. 즉, 반도체 기판 상에 소자 분리막에 의하여 분리된 영역의 산화 게이트막 상에 게이트 전극을 형성하고, 콘택트 플러그를 통하여 소스와 드레인 영역(22', 23')과 접속하는 저도전층을 형성하고, 전체면에 산화 실리콘막을 형성한 다음, 마스크로서 레지스트막을 사용하여 상층 배선층과 접속하는 비아 콘택트 플러그를 형성한다.

다음에, 도 3a에 도시한 바와 같이, 상세한 설명을 생략한 상기의 중간물을 실리콘 기판(30)상에 두께 500㎚로 산화 실리콘막(31)을 형성하고, 또한 그 위에 두께 500㎚ 로 유전율비가 3.0이하인 저유전율막(32) 및 두께가 100㎚로 무기막으로서 산화 실리콘막(33)을 형성한다.

이 저유전율막(32)은 제2 실시예와 동일하게 성막할 수 있다. 산화 실리콘막(33)은 제2 실시예의 경우와 동일하게 하여 플라즈마 CVD법에 의해 환원 분위기 하에서 행한다. 예를 들면, 실란 가스 50 sccm, N_2O 가스 1000 sccm, 플라즈마 파워 500W, 압력 10 Torr, 온도 350℃의 조건에서 행할 수 있다.

다음에, 도 3b에 도시한 바와 같이, 레지스트(34)를 마스크로 사용하여 배선 패턴(34)을 형성한다. 다음에, 도 3c에 도시한 바와 같이, 일반적인 마그네트론 방식의 에칭 장치를 사용하여 최상층의 산화 실리콘막(33) 및 그 하층의 유기막(32)을 에칭한다. 예를 들면, 저유전율막의 경우는, CHF_3 (5 sccm), O_2 (50 sccm), He (200 sccm) 가스를 사용하여 RF 플라즈마 파워 500W, -10℃의 저온으로 에칭을 행할 수 있다. 또, 산화 실리콘막의 경우는 예를 들면, C_2F_6 (14 sccm), CO (180 sccm), Ar (240 sccm), O_2 (6 sccm) 가스를 사용하여 RF 플라즈마 파워 1500W로 에칭할 수 있다. 이 경우, 상층의 산화 실리콘막(33)은 저유전율막(32)을 에칭할 때의 마스크의 역할도 완수한다.

다음에, 도 3d에 도시한 바와 같이, 배선 재료로서 예를 들면, 동을 스퍼터링 장치 또는 CVD 장치에 의해 퇴적시킨다. 이어서, CMP법에 의해 여분의 금속을 예를 들면 암모니아를 사용하여 연마한다. 이것은 완전하게 여분의 금속을 제거하기 위함과 산화 실리콘막에 새겨진 스크래치를 제거하기 위한 것이다.

그 후, 산화 실리콘막(33)을 일반적인 마그레트론 방식의 에칭 장치를 사용하여 에칭한다. 이 때의 에칭 조건은 예를 들면, C_2F_6 (14 sccm), CO (180 sccm), Ar (240 sccm)이다. 이 조건에서는 저유전율막(32)은 거의 에칭되지 않는다.

이와 같이 형성된 금속 배선(35)의 상면은 도 3e에 도시한 바와 같이, 유기막(32)의 상면보다도 높게 형성된다.

다음에, 도 3f에 도시한 바와 같이, 기판 표면을 세정한 후, 패시베이션막으로서 제2 저유전율막(36)을 제1의 저유전율막과 동일하게 하여 두께 300㎚로 형성한다.

최후에, 웨이퍼 프로세스의 완료 후, 마운팅, 본딩 프로세스를 수행하는 것에 의해 요구되는 반도체 장치를 제조할 수 있다.

이상 설명한 바와 같이, 본 실시예에 의하면, 저유전율막을 사용하는 미세 구조의 반도체 장치를 효율 좋게 제조할 수 있다. 또, 본 실시예에 의해 제조되는 반도체 장치는 패시베이션막으로서 제1의 저유전율막과 동일하게 하여 제2의 저유전율막을 사용하는 것에 의하여, 배선간의 용량이 작은 반도체 장치를 얻을 수 있다.

제4 실시예

제4 실시예는 2층의 배선 구조를 가지고 또한 더미 배선(42)을 가지는 반도체 장치의 제조예이다.

방열 경로로서 더미 배선이 설치되는 것 이외는 제3 실시예의 도 3f까지의 상태와 동일한 공정을 거치는 것에 의해 얻을 수 있는 구조의 단면도를 도 4a에 도시한다.

즉, 먼저, 도시하지 않은 트랜지스터, 배선 패턴 등이 형성된 실리콘 반도체 기판(37) 상에 두께 500㎚로 산화 실리콘막(38)을 형성하고, 그 위에 두께 500㎚로 유전율비가 3.0 이하인 저유전율막(39), 동으로 이루어진 배선(40) 및 제2의 유전율막(41)을 형성한다.

더미 배선(42)은 CMP법에 의해 금속 배선을 형성한 다음, 레지스트를 마스크로 사용하여 더미 패턴을 에칭하는 것에 의해 형성한다. 이 때, 배선 피치가 최소 피치의 3배 이상인 곳에 더미 패턴을 삽입하여 배선 간격이 최소한 1 ㎛ 이상의 개소를 제거한다. 배선 더미의 삽입은 배선 아스펙트비와 최소 배선 피치(절대치)에 의존한다. 예를 들면, 아스펙트비 2, 최소 배선 피치가 0.5 ㎛인 경우, 최소 배선 간격은 대략 0.25 ㎛가 됨으로, 0.75 ㎛ 이상의 배선 간격을 최소한 확보하고, 1 ㎛ 이상의 배선 간격을 없애도록 더미 배선을 형성하는 것이 바람직하다. 그 후, 제2의 저유전율막(41)을 제1의 저유전율막의 형성과 동일하게 하여 형성하는 것에 의하여 도4a에 도시한 상태를 얻는다.

다음에, 도 4b에 도시한 바와 같이, 레지스트막(43)을 전체면에 퇴적시킨 후, 제1층째의 배선과 제2층째의 배선을 접속하는 콘택트홀(44) 형성을 위한 패터닝을 수행하고, 도 4c에 도시한 바와 같이, 이 콘택트홀(44)에 텅스텐 등의 금속을 매입한다.

다음에, 도 4d에 도시한 바와 같이, 전체면에 질화 실리콘으로 이루어진 무기막(45)을 예를 들면, CVD법에 의해 두께 100㎚로 성막하고, 도4e에 도시한 바와 같이, 레지스트(46)에 의해 제2의 배선 패터닝을 행한다. 다음에, 도4f에 도시한 바와 같이, 배선 패턴을 포토 에칭에 의해 형성한다.

그리고, 도 4g에 도시한 바와 같이, 전체면에 배선 재료로서 알루미늄(47)을 진공 증착법에 의해 전체면에 퇴적시키고, 도 4h에 도시한 바와 같이, CMP법에 의해 상술한 것과 동일하게 하여 제2의 배선층(48)을 형성한다.

이와 같이 하여 형성된 제2의 금속 배선(48)의 상면은 제2의 유기막(40)의 상면보다도 높게 형성된다.

다음에, 도 4i에 도시한 바와 같이, 기판 표면을 세정한 후, 패시베이션막으로서 산화 실리콘막을 예를 들면 CVD법에 의해 두께 500㎚로 형성한다.

최후에, 웨이퍼 프로세스의 완료 후, 마운팅, 본딩 프로세스를 수행하는 것에 의해 요구되는 반도체 장치를 제조할 수 있다.

이상 설명한 바와 같이, 본 실시예에 의하면, 저유전율막을 사용하는 미세 구조의 신뢰성이 매우 높은 반도체 장치를 효율 좋게 제조할 수 있다.

본 실시예에 의해 제조되는 반도체 장치는 층간 절연막으로서 저유전율막을 사용함으로써, 반도체 장치의 배선간의 용량을 대폭 감소시킬 수 있다.

또, 더미 배선을 배선 피치가 최소 피치의 3배 이상인 곳에 더미 패턴을 삽입하여 배선 간격이 최소한 1 ㎛ 이상인 개소를 없애도록 함으로써, 열전도율이 낮은 유기막을 사용하는 경우에 있어서도 반도체 장치의 내부에서 발생하는 열을 외부에 방출할 수 있으므로, 발열에 의한 고장이 없는 신뢰성이 높은 반도체 장치이다.

제5 실시예

본 발명의 제5 실시예는 2층 구조를 가지는 반도체 장치에 있어서, 배선층간(좌우)의 층간 절연막으로서 크세로겔을 함유하는 막을 사용하고, 배선층간(상하)에 유전율비가 3.0 이하인 유전체막을 사용한 반도체 장치의 제조예이다. 본 실시예에 의해 제조되는 반도체 장치의 주요 공정 단면도를 도 5a 내지 도 5f에 도시한다. 또한, 이하의 도에 있어서는 편의상 소자 분리막, 전극 등은 도시를 생략한다.

먼저, 도시하지 않은 트랜지스터, 배선 패턴 등이 형성된 실리콘 반도체 기판(50)상에 실리콘 산화막, 실리콘 질화 산화막, 실리콘 질화막 등의 절연막(51)을 형성한다. 실리콘 산화막은 예를 들면, 스핀코터법을 사용하고, 시판되는 무기 SOG(실라놀 또는 실라놀을 포함하는 폴리머를 주요 성분으로 하는 것)를 약 50㎚의 두께로 형성한다. 이 경우, 스핀코터 후는 150∼200℃로 1분 정도의 베이킹(baking)을 행하여 큐어(cure)를 350∼450℃로 30분에서 1시간을 행한다. 실리콘 산화막은 플라즈마 장치를 사용하여 플라즈마 CVD 법에 의해 형성할 수 있지만, 동배선을 산화시키는 것을 가능한 방지하기 위하여, 산화제로서 N_2O 가스를 사용하고, 실리콘막으로서 모노실란, 디실란, 트리실란 등의 실란류를 사용하는 것이 바람직하다. 플라즈마 CVD법에 의한 경우는 기판 온도 300∼400℃, 플라즈마 파워 350W, 압력 1kPa 정도의 조건에서 성막할 수 있다.

실리콘 질화 산화막의 경우는 아미노기를 가지는 시판되는 무기 SOG를 스핀 코터법으로 성막할 수 있지만, 바람직하게는 플라즈마 CVD법을 사용하여 성막한다. 사용하는 가스로서 예를 들면, 실리콘 소스로서 모노실란, 디실란, 트리실란 등의실란류를 사용하고, 질화제로서 예를 들면 암모니아, 하이드라진 등을, 산화제로서 N_2O 가스를, 캐리어(carrier) 가스로서 질소, 헬륨, 아르곤 등을 각각 사용하고, 기판 온도를 300∼400℃, 플라즈마 파워 350W, 압력 1kPa 정도의 조건에서 성막할 수 있다.

다음에 전체면에 도시하지 않은 레지스트막을 성막한 후, 소정의 패터닝을 수행하고, 포토 에칭법으로 콘택트홀을 형성하고, 텅스텐 등의 금속을 매입하는 것에 의해 콘택트 플러그(52)를 형성한다.

다음에, 저유전율막(53)을 두께 300∼800㎚ 정도로 성막하는 것에 의해 도 5a에 도시한 상태도를 얻는다. 상기 저유전율막(53)은 유전율비가 3.0이하인 절연막이라면 특히 제한이 없다. 예를 들면, 저유전율막이나 크세로겔을 함유하는 막을 예시할 수 있다. 그 외 저유전율막으로서는 상기 예시한 것을 사용할 수 있다.

다음에, 예를 들면, 질화 실리콘, 실란 커플링제 등으로 이루어진 무기막(56)을 예를 들면, CVD 법에 의해 두께 100㎚로 전체면에 성막하고, 도시하지 않은 레지스크막에 의해 제1의 배선 패터닝을 수행하고, 배선 패턴을 포토 에칭에 의해 형성한다. 이 경우의 에칭은 예를 들면, 시판되는 에칭 장치로 C_2F_6 (14 sccm), CO (180 sccm), Ar (240 sccm) 가스를 사용하여 RF 플라즈마 파워 1500W로 수행할 수 있다.

이어서, 도 5b에 도시한 바와 같이, 전체면에 배선 재료로서 알루미늄, 동, 동합금, 텅스텐 등의 금속을 진공 증착 등에 의해 퇴적시키고, CMP법에 의해 제1의 배선층(54)을 형성한다. 이 때, 상기 무기막(56)은 완전하게 제거되는 것이 바람직하지만, 실제의 제조상은 도 5b에 도시한 바와 같이 기판 상에 잔존해도 된다.

다음에, 도 5c에 도시한 바와 같이, 전체면에 저유전율막(57)을 두께 800㎚ 정도로 성막한다. 성막은 예를 들면 전구체를 스핀코터로 성막하고 그 후, 300∼400℃로 큐어링(curing)(소성)하는 것에 의

해 수행할 수 있다. 상기 저유전율막의 재료로서는 유전율비가 3.0 이하인 것이 바람직하고, 예를 들면 상기 예시한 것을 사용할 수 있다.

또한, 아몰퍼스 카본 등의 재료를 사용하는 경우는 아세틸렌, 필요에 대응하여 플루오로 카본 가스를 사용하고, 플라즈마 CVD 장치를 사용하여 형성할 수 잇다. 이 경에도 300℃□400℃로 큐어링을 행한다.

다음에, 도시하지 않은 레지스트막을 전체면에 성막한 후, 소정의 패터닝을 수행하고, 포토 에칭에 의해 제2의 콘택트홀을 제1의 배선층까지 형성한 다음, 텅스텐 등의 금속을 매입하는 것에 의해 비아 콘택트 플러그(58)를 형성한다(도 5d).

다음에, 도 5e에 도시한 바와 같이, 전체면에 크세로겔을 함유하는 막(59)을 예를 들면, 두께 500㎚ 정도로 형성한다. 크세로겔로서는 예를 들면, 나노글래스(nanoglass)사가 개발한 Nonoporous Silica (제품명)를 사용할 수 있다. Nonoporous Silica (제품명)는 포로스 실리카의 일종이지만, 본 실시예에서는 이것에 한정되는 것은 아니고, 방향족 등의 비교적 고분자의 알킬기를 가지는 실라놀 수지를 웨이퍼 상에 도포하고, 그것을 겔화시켜서 실란 커플링제 또는 수소화 처리에 의해 소수 처리를 수행하여 형성되는 것도 된다.

또한, 이 경우 크세로겔을 함유하는 막은 특히 층간 밀착성이 부족하기 때문에, 상기 저유전율막 상에 상기 예시한 바와 같은 실란 커플링제를 박리 방지를 위하여 미리 도포하여 놓는 것이 바람직하다. 실린 커플링제로서는 일반식 $RSiX_3$, $RR'SiX_2$ (식 중, R, R'는 알킬기를 나타내고, X는 할로겐 원자를 나타낸다.)로 표시되는 알킬 실란류를 예시할 수 있다.

다음에, 도시하지 않은 레지스트막을 전체면에 성막한 후, 소정의 패터닝을 수행하고, 포토 에칭에 의해 배선층을 위한 홈(trench)을 형성한다. 이 경우의 에칭은 예를 들면, 시판되는 에칭 장치로 C_2F_6 (14 sccm), CO (180 sccm), Ar (240 sccm) 가스를 이용하여 RF 플라즈마 1500W 파워로 수행할 수 있다. 이어서, 도5e에 도시한 바와 같이, 전체면에 배선 재료로서 알루미늄, 동, 동합금, 텅스텐 등의 금속을 진공 증착법에 의해 퇴적시킨 다음, 도시하지 않은 무기막을 퇴적시키고 예를 들면 실리카계 슬러리를 사용하는 CMP법에 의해 제2의 배선층(60)을 형성한다. 이 경우 무기막으로서는 제1의 배선층을 형성할 때에 예시한 것과 동일한 것을 사용할 수 있다. 또한, 무기막은 완전히 제거되는 것이 바람직하지만, 실제의 제조에서는 기판 상에 잔존해도 된다.

최후에, 도 5f에 도시한 바와 같이, 전체면에 산화 실리콘막 등의 절연막(61)을 패시베이션막으로서 형성하여 배선층의 형성 공정을 완료한다.

본 실시예에서는 배선층의 주위(배선층의 좌우), 바람직하게는 배선 간격이 표준 피치의 3배 이하인 개소에는 유전율비가 매우 작은 크세로겔을 함유하는 막을 사용하고, 또한, 배선간의 콘택트홀의 주위(배선층의 상하)에는 유전율비가 3.0 이하인 유전체막을 사용한다. 따라서, 크세로겔막의 기계적 강도, 열전도성, 내열성, 내습성, 층간 밀착성이 부족한 결점을 보충하면서, 배선 용량을 대폭 축소하는 것에 의하여, 신뢰성이 높은 미세 구조를 가지는 반도체 장치를 수득률 좋게 제조할 수 있다.

또, 크세로겔을 함유하는 막의 상하에는 실란 커플링제로 이루어진 층을 설치하는 것에 의하여, 층간 밀착성이 뛰어난 반도체 장치를 제조할 수 있다.

또한, 방열을 위한 더미 배선을 설치함으로써, 반도체 장치 전체의 발열이 작고, 온도상승에 의한 오동작이 작은 신뢰성이 높은 반도체 장치이다.

제6 실시예

본 실시예에서는 층간 절연막으로서 저유전율 유기막을 사용하고 방열 경로로서 더미 배선층 및 더미 콘택트홀을 형성하는 예이다.

먼저, 도 6a에 도시한 바와 같이, 도시하지 않은 트랜지스터 등의 능동 소자, 소자 분리막(63)으로 구성된 실리콘 반도체 기판(62)상에 하층 층간 절연막(64)을 형성한다.

그 후, 도 6b에 도시한 바와 같이, 전체면에 레지스트막(65)을 성막하고 콘택트 플러그(콘택트홀) (66) 및 더미 콘택트 플러그(67)의 형성을 위한 패터닝을 수행한다. 더미 콘택트홀은 층간 절연막(63)상에서 상층에 형성하는 더미 배선의 하부에 형성하는 것이 제조상 바람직하다. 또, 콘택트 피치는 최소 피치가 되는 것이 바람직하다. 최소 피치로 하는 것에 의해 열전도성을 향상하고, 열확산 효율을 높일 수 있다.

또, 트랜지스터, 소자 분리막, 하층 층간 절연막, 콘택트 플러그 등의 형성은, 공지의 기술을 이용할 수 있다. 하층 층간 절연막으로서는 예를 들면 산화 실리콘막, 포스포러스, 또는 포스포러스 및 보론소가 불순물로서 도핑된 산화 실리콘막을 형성할 수 있다. 또, 콘택트 플러그(66,67)의 형성에는 텅스텐 등의 도전성 물질을 매입하는 것에 의해 형성할 수 있다. 이와 같이 하여 도 6c에 도시한 상태를 얻는다.

다음에, 도 6d에 도시한 바와 같이, 저유전율막(68)을 전체면에 형성한 후, 이 저유전율막(68)상에 산화 실리콘막, 질화 실리콘막, 질화 산화 실리콘막 또는 질화막계의 무기막(69)을 예를 들면 두께 100 ㎚ 정도로 성막한다.

또한 이 성막은, 통상, 플라즈마 CVD(Chemical Vapour Deposition) 법이 사용되지만, 화원 분위기 하에서 수행하는 것이 바람직하다. 산화 분위기에서 CVD법을 사용하는 경우에는 저유전체 유기막이 산화되고, 막박리 등의 바람직하지 않은 현상을 야기시키는 우려가 있다.

에칭 조건으로서, 산화 실리콘막을 성막하는 경우에는 예를 들면, 플라즈마 CVD 장치를 사용하고 실란 가스 50sccm , N_2O 가스 100sccm, 플라즈마 파워 500W, 압력 10 Torr, 온도 350℃의 조건으로 수행할 수 있다.

다음에 도 6e에 도시한 바와 같이, 전체면에 레지스트막(70)을 성막하고 배선 및 더미 배선을 형성하기 위한 더미 패터닝을 행한다. 더미 배선의 패터닝은 바람직하게는 최소한 3배 피치 이상의 배선 간격의 부분, 보다 바람직하게는 3배 피치 이상의 배선 간격의 부분에 있어서 모든 배선 간격이 1 ㎛ 이하로 되도록 수행한다.

또한, 이 경우, 배선의 패터닝과 더미 배선의 패터닝을 반드시 동시에 행할 필요는 없다.

다음에, 일반적인 마그네트론 방식의 에칭 장치를 사용하여 최상층의 산화 실리콘막(69) 및 그 하층의 저유전체막(68)을 에칭한다. 에칭은 예를 들면, 산화 실리콘막의 에칭의 경우는 예를 들면, C_2F_6 (14 sccm), CO (180 sccm), Ar (240 sccm), O_2 (6 sccm) 가스를 사용하여 RF 플라즈마 파워 1500W로 수행할 수 있다. 또, 저유전체막의 에칭의 경우는 CHF_3 (5 sccm), O_2 (50 sccm), He (200 sccm) 가스를 이용하여 RF 플라즈마 파워 500W, -10℃의 조건으로 수행할 수 있다.

상기 에칭에 있어서는, 상층의 산화 실리콘막(69)은 저유전체막(68)을 에칭할 때의 마스크의 역할도 완수한다. 즉, 저유전체막을 에칭하는 조건에서는 레지스트막(70)도 동시에 에칭된다. 또한, 본 실시예에서는 산화 실리콘막을 사용하지만 그 외, TiN, TiON, TaN, TaO, TaON, WN, W, Ti 등의 금속계 재료를 사용할 수도 있다.

다음에, 도 6f에 도시한 바와 같이, 다마신법에 의해 배선층(71) 및 더미 배선층(72)을 형성한다. 이와 같이 하여 형성되는 배선층(71) 및 더미 배선층(72)의 상면은, 저유전율막(68)의 상면보다도 높게 형성된다.

즉, 배선층의 형성은 스퍼터링 장치 또는 CVD 장치를 사용하고 배선 재료(금속)로서 예를 들면, 동을 전체면에 퇴적시키고, 이어서 CMP법에 의해 여분의 금속막을 연마한 후, 다시 CMP법에 의해 50㎚ 정도의 무기막(산화 실리콘막)(69)을 연마하는 것에 의해 행해진다. 이 연마는 완전히 금속을 제거하기 위함과, 산화 실리콘막에 새겨진 스크래치를 제거하기 위하여 수행하는 것이다.

다음에, 산화 실리콘막(69)을 일반적인 마그네트론 방식의 에칭 장치를 사용하여 에칭한다. 이 때의 조건으로서는 예를 들면, C_2F_6 (14 sccm), CO (180 sccm), Ar (240 sccm)을 사용할 수 있다. 이러한 조건에서는 유전체 유기막은 거의 에칭되지 않는다. 또한, 장치 성능보다도 신뢰성을 중시하는 경우에는 이 산화 실리콘막의 제거 공정을 생략할 수 있다.

이와 같이 하여 얻어지는 배선 구조는, 더미 배선층 이외에 더미 배선층에 접속하는 더미 콘택트 플러그를 가짐으로써, 더욱더 방열 효과가 높아진다. 따라서 신뢰성이 매우 높은 배선 구조를 가지는 반도체 장치이다.

제7 실시예

본 실시예에서는 2층의 배선 구조를 가지고, 더미 배선층 및 더미 콘택트홀(더미 비아 콘택트홀 및 비아 콘택트홀)을 가지는 반도체 장치의 제조예이다.

먼저, 상기 제6 실시예와 동일하게 하여 도 6f에 도시한 상태를 얻는다. 다음에, 상기 배선층(71) 및 더미 배선층(72)상에 두께 100㎚ 이상의 얇은 질화 실리콘막, 산화 실리콘막 또는 질화 산화 실리콘막 등의 도시하지 않은 무기막을 형성한다. 이 막은, 비아 콘택트홀 형성시에 에칭 스톱퍼(stopper) 층으로서 사용되기 때문에, 가능한 만큼 얇은 것이 바람직하다. 본 실시예에서는 예를 들면 질화 실리콘막을 두께 100㎚로 형성한다.

다음에, 도 7a에 도시한 바와 같이, 제2의 도전체막(73)을 전체면에 형성한다. 본 실시예에서는 이 저유전체막(73)으로서 상기 열거한 것 외에, 비교적 유전율이 높은 유기 SOG막, 플루오린 도프드 실리콘 산화막 등을 사용하는 것도 가능하다. 이 제2의 저유전체막(73)은 일반적으로 시판되는 CVD 장치 또는 SOG 코터(coater) 장치를 사용하고, 공지의 기술을 사용하여 형성할 수 있다.

다음에, 상기 제2의 저유전체막(73)상에, 실리콘 산화막, 질화 산화 실리콘막 또는 질화 실리콘막 등의 무기막(74)을 성막한다. 이러한 막은 일반적으로는 CVD 장치를 사용하여 성막할 수 있지만, SOG 코터, 진공 증착, 스퍼터링 장치를 사용할 수 있다. 이 무기막(74)은 배선층을 패터닝 후의 에칭할 때의 스톱퍼로서 작용한다.

다음에, 전체면에 레지스트막(75)을 성막한 후, 비아 콘택트 및 더미 비아 콘택트 형성을 위한 패터닝을 수행한다. 이 때, 더미 비아 콘택트홀의 형성은 상하에 더미 배선이 형성되는 곳에 최소 피치로 수행하는 것이 바람직하다.

다음에, 무기막(74) 및 제2의 저유전율막(73)을 에칭하고 비아 콘택트홀 및 더미 비아 콘택트홀을 형성하는 것에 의해, 도 7b에 도시한 상태를 얻는다. 무기막(74) 및 제2의 저유전율막(73)의 에칭은 상술한 무기막 및 저유전율막의 에칭 조건과 동일하게 하여 수행할 수 있다. 그 때에는 레지스트막(75)도 동시에 에칭 제거된다.

그 후, 동 등의 금속 배선 재료를 상기 비아 콘택트홀 및 더미 비아 콘택트홀에 매입하고, 비아 콘택트 플러그(74) 및 더미 비아 콘택트 플러그(75)를 형성하는 것에 의하여 도 7c에 도시한 상태도를 얻는다.

다음에, 전체면에 제3의 저유전율막(78)을 형성한다. 형성 방법은, 상기 제2의 저유전체막과 동일하다. 또한, 상기 제3의 저유전체막(78)상에 실리콘 산화막, 질화 산화 실리콘막 또는 질화 실리콘막 등의 무기막(79)을 성막하는 것에 의해 도7d에 도시한 상태도를 얻는다. 이러한 막은, 일반적으로는

CVD 장치를 사용하여 성막할 수 있지만, SOG 코터, 진공 증착, 스퍼터링 장치를 사용할 수도 있다. 이 무기막(79)은 배선층을 CMP법에 의해 연마할 때의 스톱퍼로서 작용한다.

다음에, 도 7e에 도시한 바와 같이, 전체면에 레지스트막(80)을 성막한 후, 배선층 및 더미 배선층 형성을 위한 패터닝을 수행한다. 더미 배선층의 패터닝은 배선 간격이 최소 피치 이상인 곳에 형성하는 것이 바람직하다. 더미 패턴을 설계 최소치법으로 형성한 경우에, 더미 배선층과 배선층과의 간격이 최소 피치 이상으로 하기 위한 것이다. 또한, 성능을 중시하는 경우에 있어서는 그 간격을 최소 간격보다도 2배 이상으로 해 놓는 것이 보다 바람직하다. 배선 간격을 2배 이상으로 하는 것에 의하여 배선간의 용량을 대략 반분할 수 있게 된다.

다음에, 일반적인 마그네트론 방식의 에칭 장치를 사용하여 최상층의 무기막(77) 및 그 하층의 제3의 저유전체막(78)을 에칭한다. 이 에칭은 예를 들면, 저유전체막의 경우는 CHF_3 (5 sccm), O_2 (50 sccm), He (200 sccm) 가스를 이용하여 RF 플라즈마 파워 500W, -10℃로 수행할 수 있다. 또, 무기막(산화 실리콘막)의 경우는, 예를 들면, C_2F_6 (14 sccm), CO (180 sccm), Ar (240 sccm), O_2 (6 sccm) 가스를 이용하여 RF 플라즈마 파워 1500W로 에칭을 수행할 수 있다.

이 경우, 상층의 무기막(79)은 제3의 저유전체막(78)을 에칭할 때의 마스크로도 된다. 즉, 제3의 저유전체막을 에칭하는 조건에서는 레지스트막980)도 동시에 에칭된다. 또한, 본 실시에에서는 산화 실리콘막 등의 무기막을 사용하지만, TiN, TiON, TaN, TaO, TaON, WN, W, Ti 등의 다른 금속막을 사용할 수도 있다.

또, 이 때 더미 콘택트의 패터닝을 수행하지 않고, 배선층을 형성한 후, 더미 콘택트홀 형성을 위한 패터닝을 수행하고, 그곳에 열전도성이 높은 산화 실리콘막, 질화 실리콘막, 질화 산화 실리콘막 등을 형성할 수 있다.

다음에, 다마신법에 의해 배선층(81) 및 더미 배선층(82)을 형성한다. 즉, 배선 재료(금속)로서 예를 들면, 동을 스퍼터링 장치 또는 CVD 장치로 형성하고 이어서, CMP법에 의해 여분의 금속막을 연마한다. 최후에 다시 CMP법에 의해 50㎚ 정도의 무기막(79)을 연마한다. 무기막을 다시 연마하는 것은, 완전하게 여분의 금속을 제거하는 것과 무기막(산화 실리콘막 등)에 새겨진 스크래치를 제거하기 위한 것이다.

이러한 방법으로, 도 7f에 도시한 바와 같은 2층의 배선층, 더미 배선층, 콘택트홀 및 더미 콘택트홀을 가지는 다층 배선 구조를 형성할 수 있다. 이 때, 배선층(81) 및 더미 배선층(82)의 상면의 높이는 제3의 저유전율막(78)의 상면의 높이 보다 높게 형성된다.

또한, 이상의 조작을 반복하는 것에 의해 3층 이상의 다층 배선 구조도 동일하게 하여 형성할 수 있다.

이와 같이 하여 얻어지는 배선 구조는, 더미 배선층 이외에 더미 콘택트 플러그를 가짐으로써, 더욱더 방열 효과가 높아진다. 따라서, 신뢰성이 높은 다층 배선 구조를 가지는 반도체 장치를 얻을 수 있다.

또한, 상기 실시예에서는 배선층 또는 콘택트홀(콘택트홀 또는 비아 콘택트홀) 형성을 위한 패터닝과 동시에 더미 배선층 또는 더미 콘택트홀 형성을 위한 패터닝을 동시에 수행하는 예를 나타낸다. 본 발명에 있어서는 배선층 또는 콘택트홀을 형성한 후에, 더미 배선층 또는 더미 콘택트홀을 형성하는 것을 수행하는 것도 가능하다.

예를 들면, 배선층을 형성한 후에 더미 배선층을 형성하는 것은 다음과 같이 행할 수 있다.

먼저, 도 8a에 도시한 바와 같이, 접속 플러그(85) 및 배선층(84)을 형성한 구조를 얻은 다음, 도 8b에 도시한 바와 같이, 산화 실리콘막 등의 무기막(89)을 전체면에 형성한 후, 레지스트막(89)을 성막하고 더미 배선층 형성을 위한 패터닝을 수행한다.

GF Exhibit 1124 - 2123/2704

그 후, 일반적인 마그네트론 방식의 에칭 장치를 사용하여 상기 무기막(89)을 예를 들면, C_2F_6 (14 sccm), CO (180 sccm), Ar (240 sccm), O_2 (6 sccm) 가스를 이용하여 RF 플라즈마 파워 1500W로 에칭한다. 또, 상기 유전체막(유전체 유기막)(86)을 CHF_3 (5 sccm), O_2 (50 sccm), He (200 sccm) 가스를 이용하여 RF 플라즈마 파워 500W, -10℃의 조건으로 에칭한다.

그 후, 더미 패턴을 CVD 또는 SOG 코터를 사용하여 산화 실리콘막, 질화 실리콘막 또는 질화 산화 실리콘막을 형성하여 매입한다. 산화 실리콘막, 질화 실리콘막 또는 질화 산화 실리콘막은 열전도성에 뛰어나다. 다음에, 절연막 연마용인 CMP 장치를 사용하여 실리카계 슬러리 또는 산화 세륨(cerium) 슬러리를 사용하여 연마하여 도 8c에 도시한 구조를 얻는다. 이 경우도 배선층(84) 및 더미 배선층(90)의 상면은 저유전율막(86)의 상면보다도 무기막(88)의 높이만큼 높게 형성된다.

또한, 본 실시예에서는 저유전율막으로서 유전체 유기막을 사용하지만, 크세로겔을 사용하는 경우에도 본 발명의 소기의 효과를 이루는 구조를 얻을 수 있다. 그 경우의 에칭 조건으로서는 상기 무기막의 에칭 조건과 동일하다.

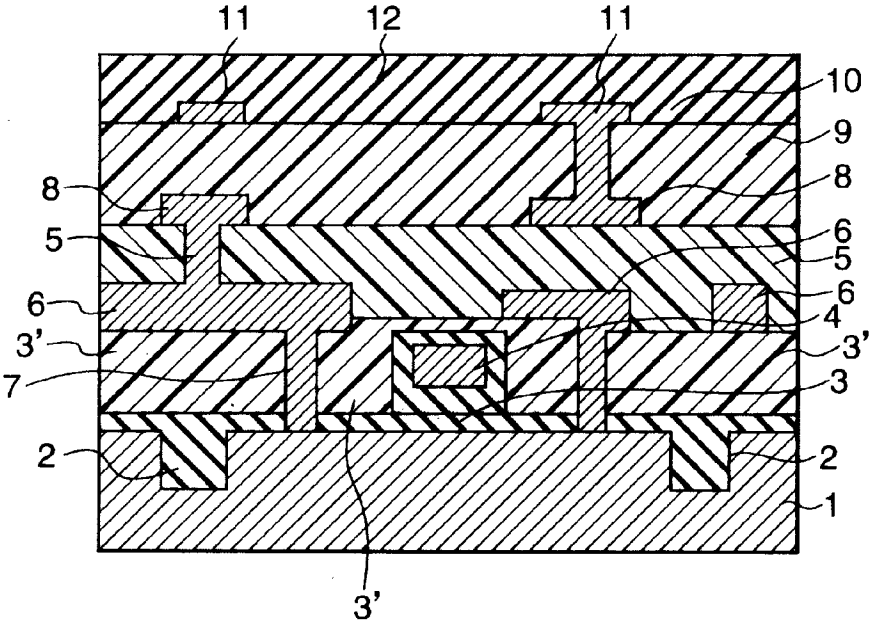
이상 설명한 바와 같이, 본 발명의 반도체 장치는 층간 절연막을 유전율비가 3.0 이하인 유전체막을 사용하기 때문에, 배선간 용량의 증대가 대폭 억제되는 미세한 반도체 장치이다.

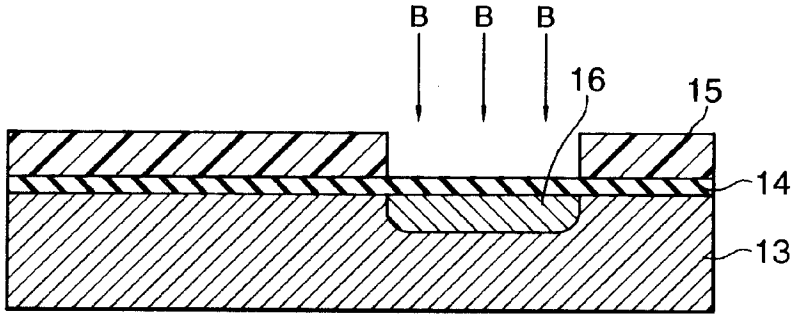
또, 방열을 위한 더미 배선층을 배선 패턴에 대하여, 최소한 3배 피치 이상의 배선 간격 부분에 설치하는 것에 의하여, 열전도율이 작은 저유전율막을 사용하는 것에 의한 열확산 효율의 저하를 효과적으로 방지할 수도 있다.

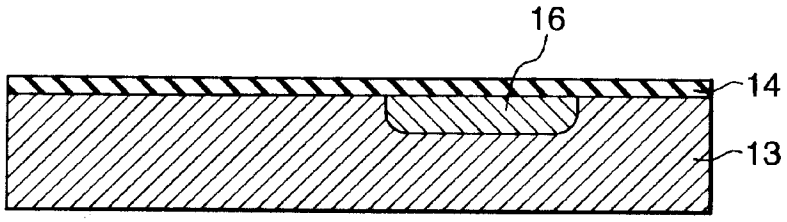
또, 더미 접속 플러그(콘택트 플러그 및 비아 콘택트 플러그)를 더미 배선층의 아래에 설치하는 경우에는 열전도율이 작은 저유전율막을 사용하는 것에 의한 열확산 효율의 저하를 보다 효과적으로 방지할 수 있다.

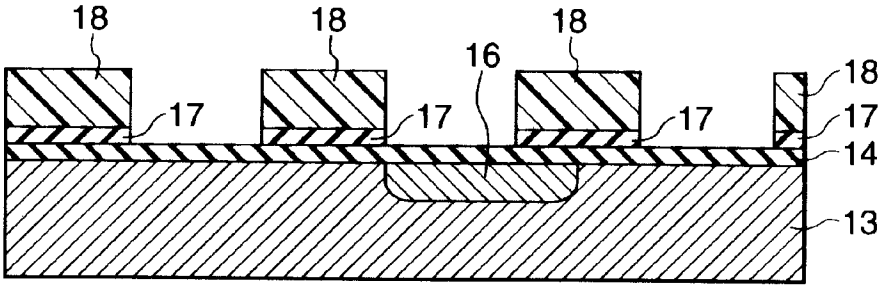
또한, 본 발명에 의하면, 배선층의 주위(배선층의 좌우), 바람직하게는 배선 간격이 표준 피치의 3배 이하인 개소에는 유전율비가 매우 작은 크세로겔을 함유하는 막을 사용하고, 또한, 배선간의 콘택트 홀의 주위(배선층의 상하)에는 저유전율막을 사용하는 것에 의하여 크세로겔막의 결점을 보충하면서, 배선 용량을 대폭 축소하는 것에 의하여 신뢰성이 높은 미세 구조를 가지는 반도체 장치를 수득률 좋게 제조할 수 있다.

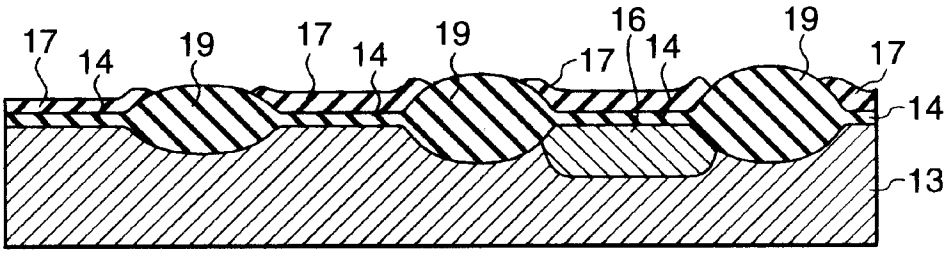
또, 크세로겔을 함유하는 막의 상하에는 실란 커플링제로 이루어진 층을 설치하는 것에 의하여, 층간 밀착성에 뛰어난 반도체 장치를 제조할 수 있다.

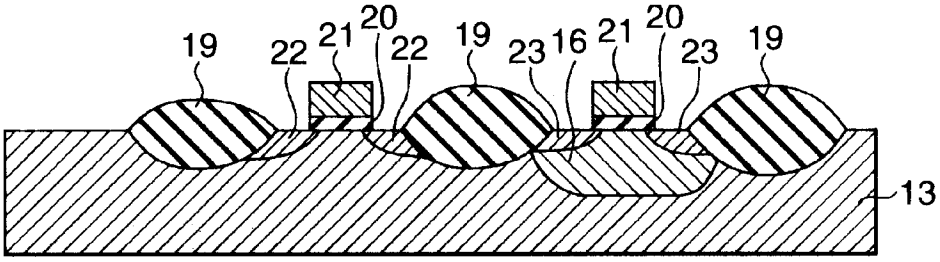

11
12
11
10
9
8
8
5
6
5
6
6
4
3'
3'
7
3
2
2
1
3'

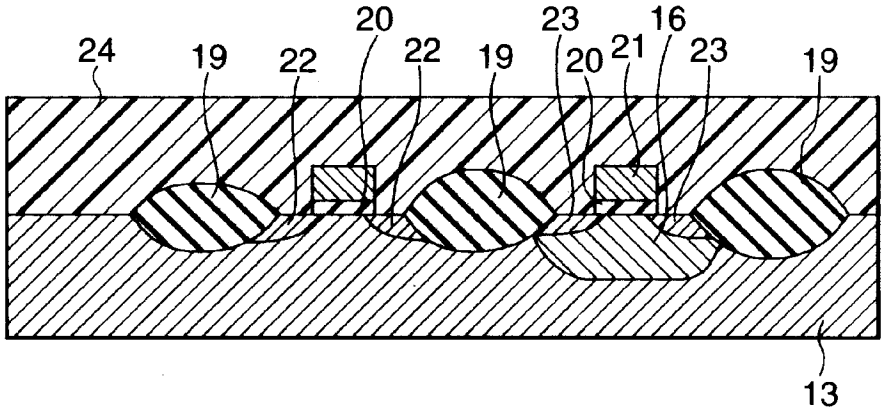

B
B
B
16
15
14
13

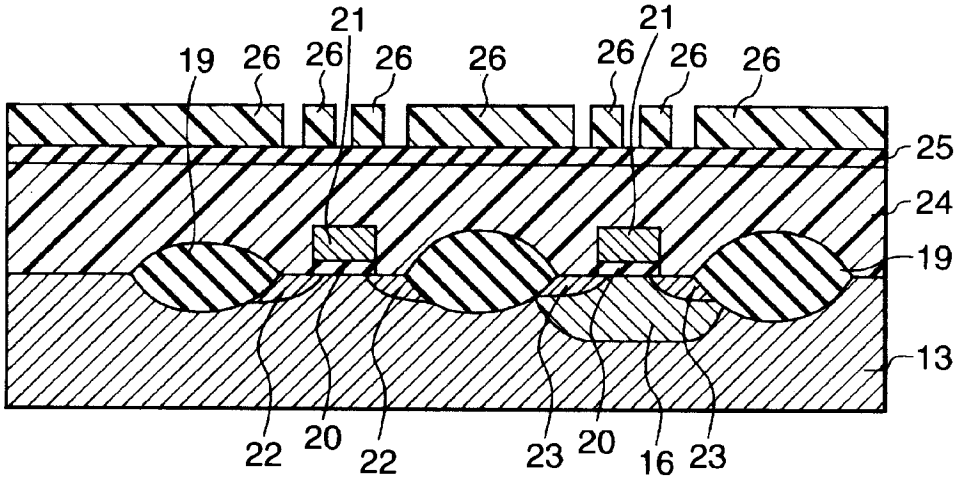

16
14
13

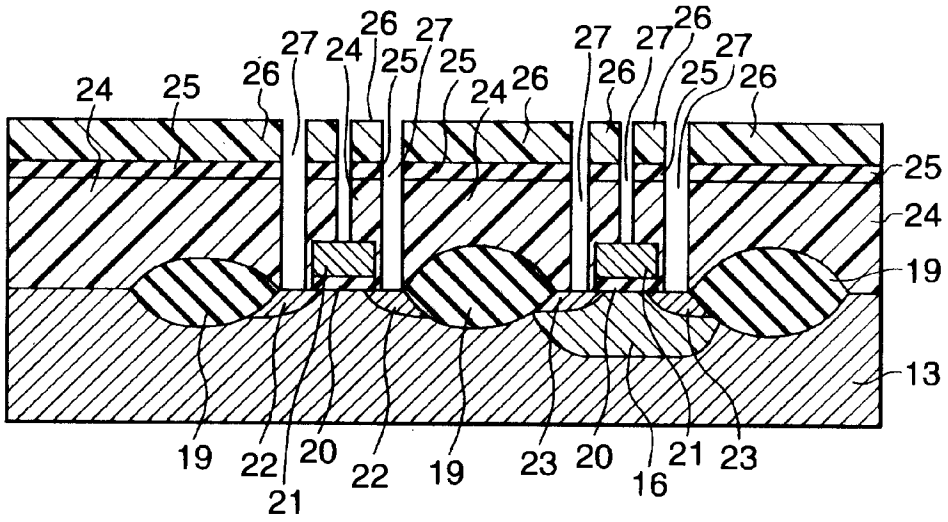

18
18
18
16
18
17
17
17
17
14
13

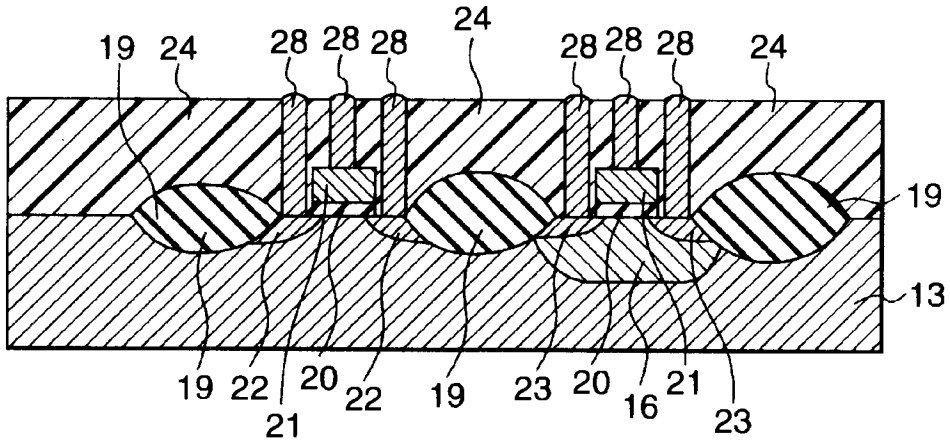

17
14
19
17
14
19
16
17
14
19
17
14
13

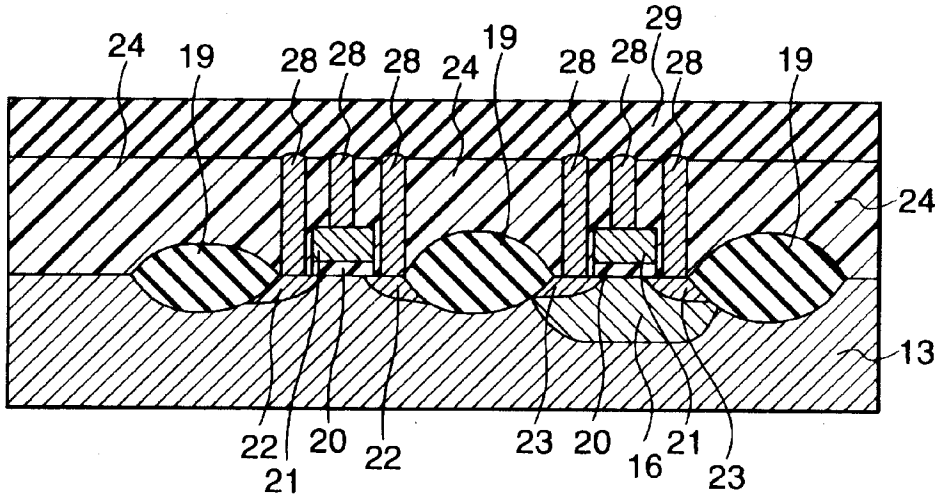

19
22
21
20
22
19
23
16
21
20
23
19
13

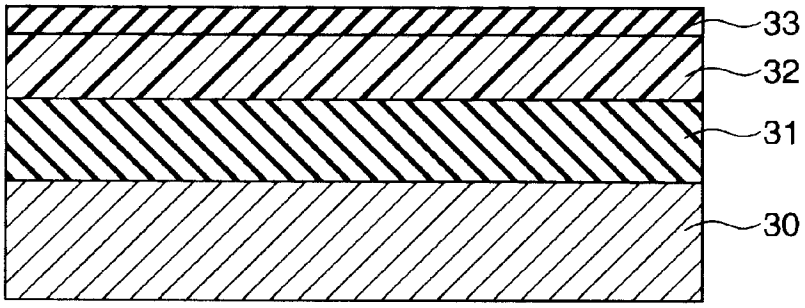

24
19
22
20
22
19
23
20
21
16
23
19
13

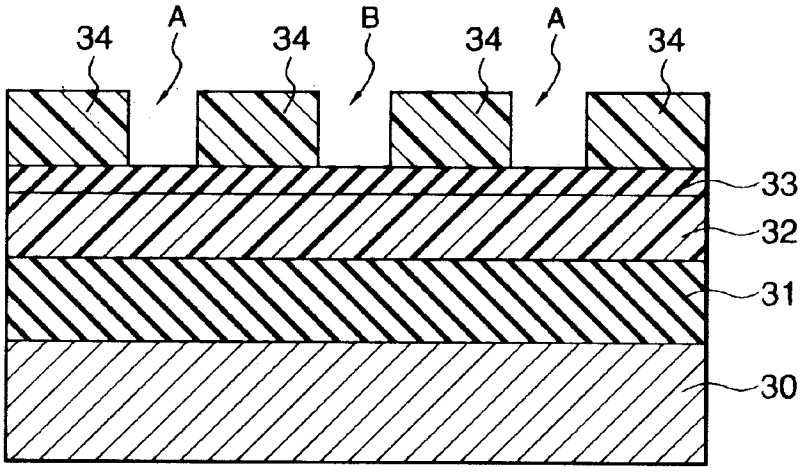

21
21
19
26
26
26
26
26
26
26
26
25
24
19
13
22
20
22
23
20
16
23

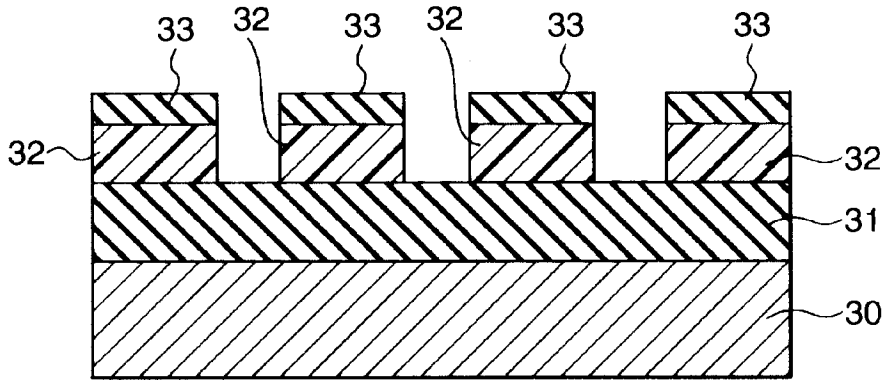

26
27
24
27
27
26
27
27
26
24
25
26
25
25
24
26
26
25
26
25
24
19
13
19
22
20
21
22
19
23
20
21
16
23

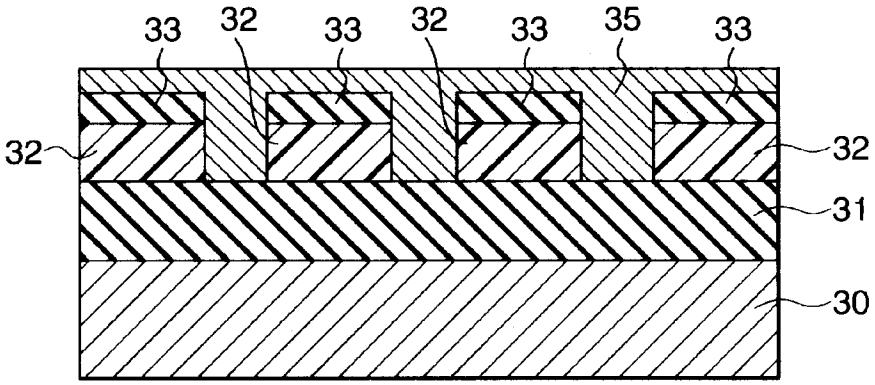

24
19
24
28
28
28
28
28
28
24
19
13
19
22
20
21
22
19
23
20
16
21
23

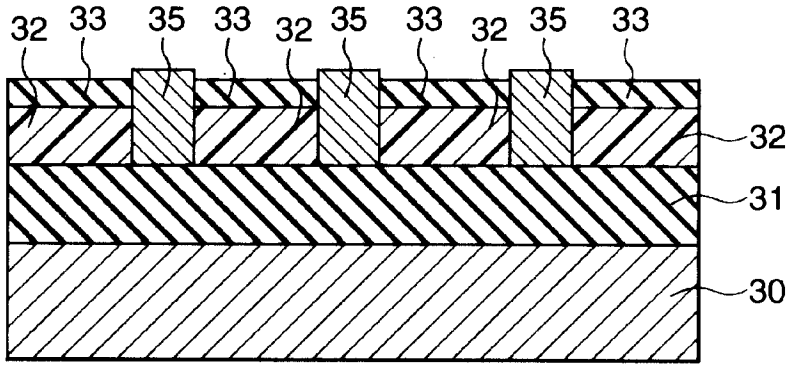

24
19
28
28
28
24
19
28
28
29
28
19
24
13
22
21
20
22
23
20
16
21
23

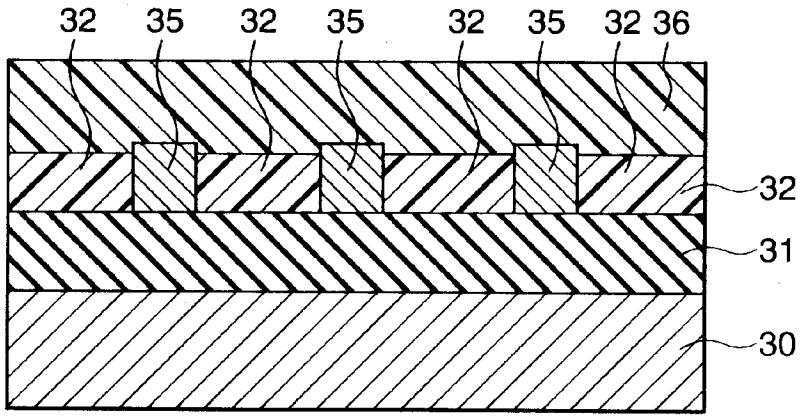

33
32
31
30

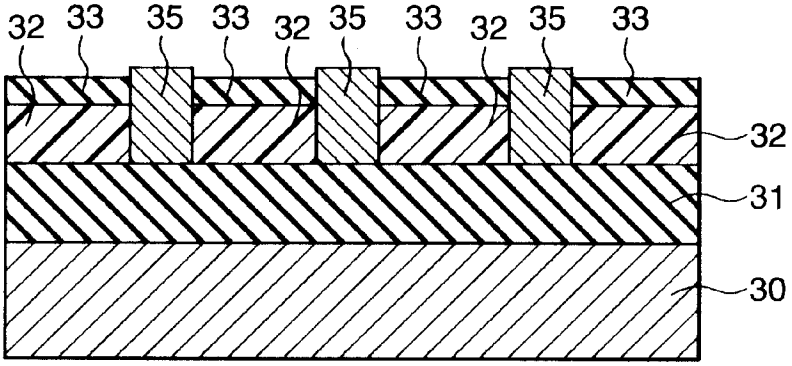

34
A
34
B
34
A
34
33
32
31
30

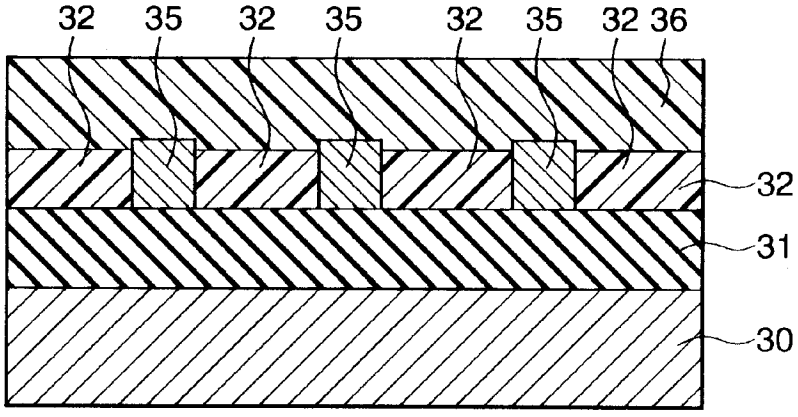

33
32
33
32
33
33
32
32
31
30

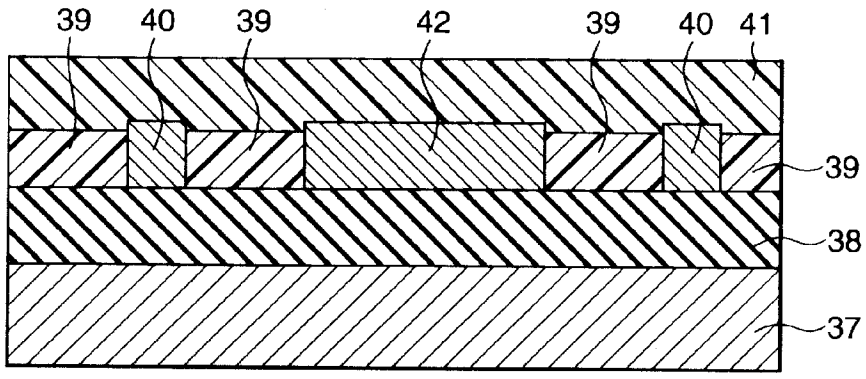

33
32
33
32
33
35
33
32
32
31
30

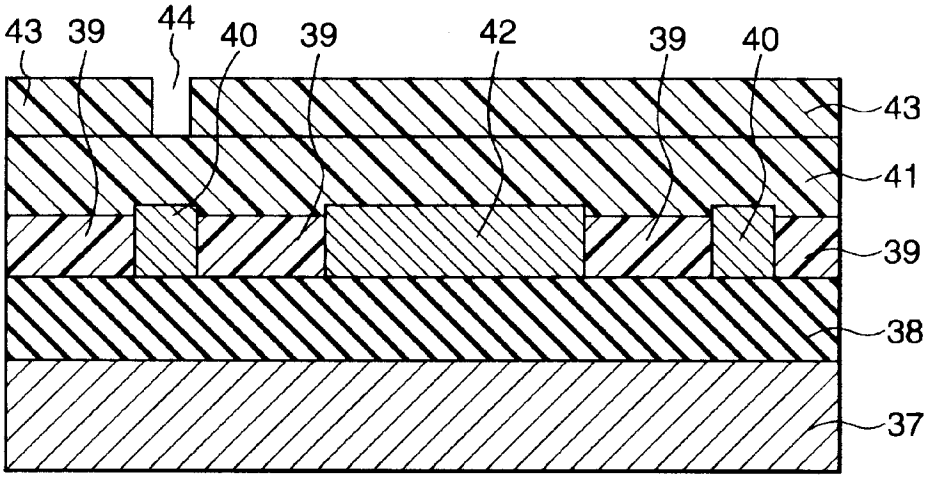

32
33
35
33
32
35
33
32
35
33
32
31
30

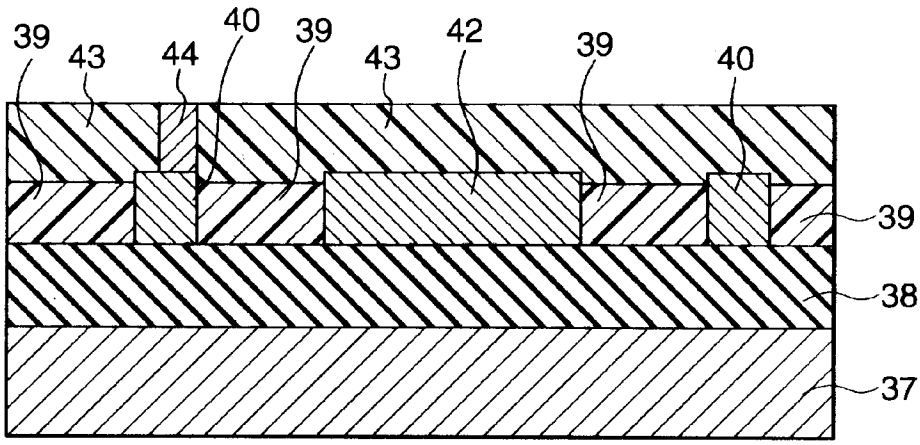

32
35
32
35
32
35
32
36
32
31
30

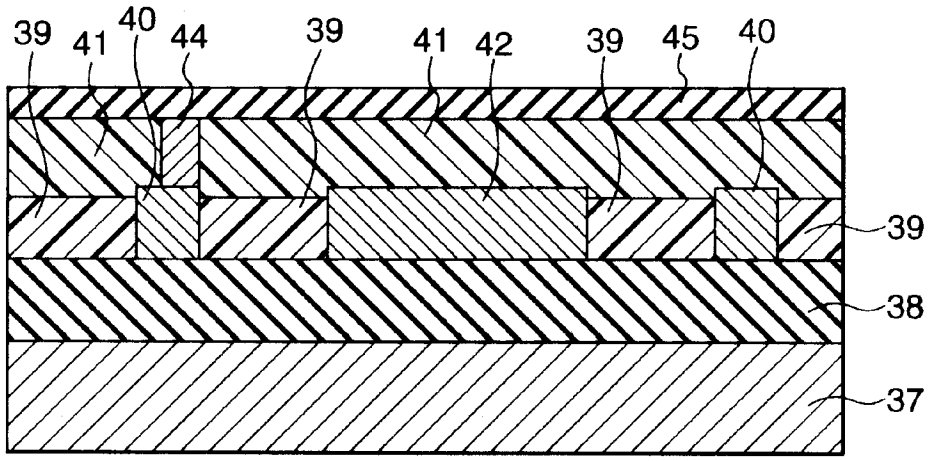

32
33
35
33
32
35
33
32
35
33
32
31
30

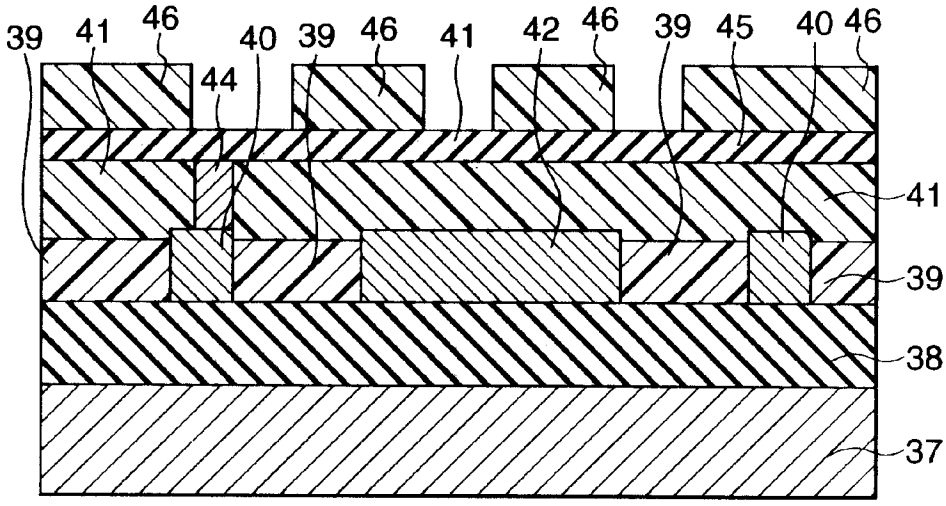

32
35
32
35
32
35
32
36
32
31
30

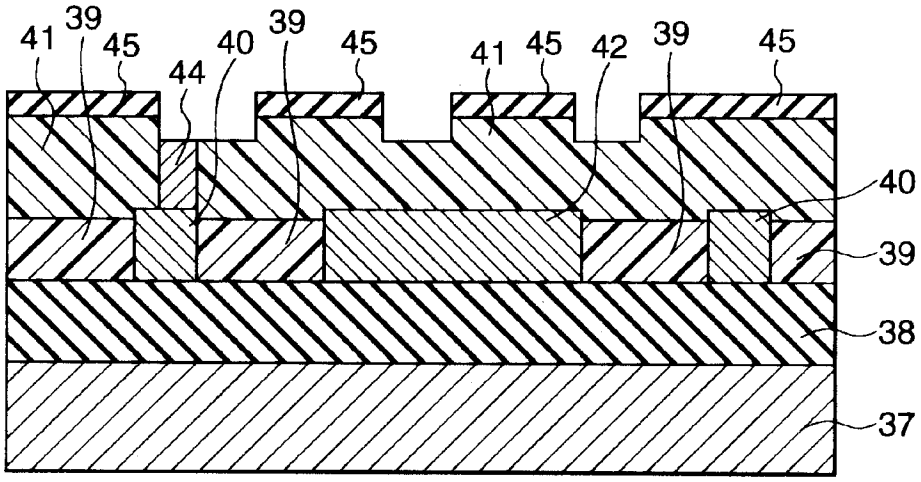

39
40
39
42
39
40
41
39
38
37

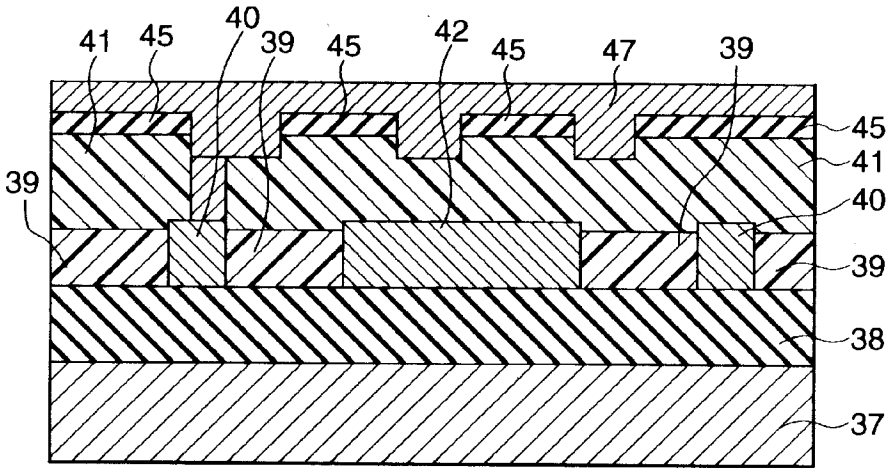

43
39
44
40
39
42
39
40
43
41
39
38
37

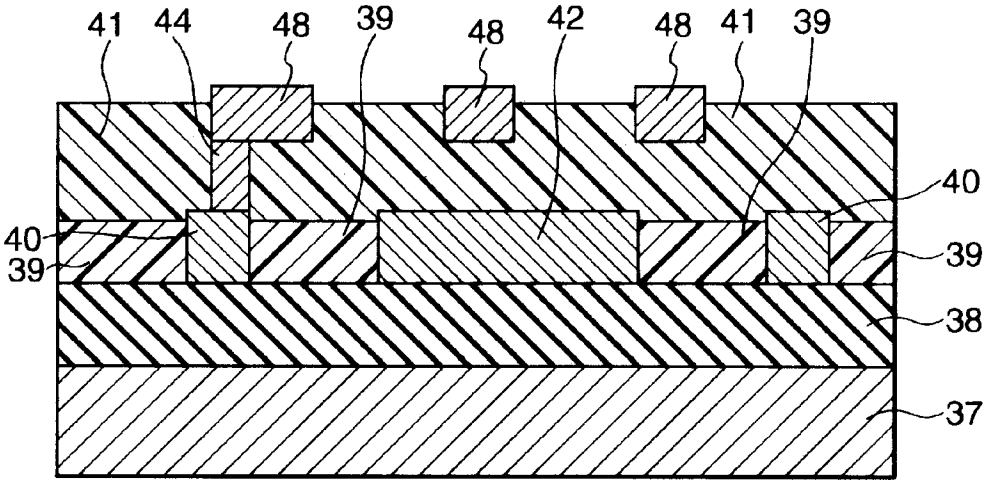

39
43
44
40
39
43
42
39
40
39
38
37

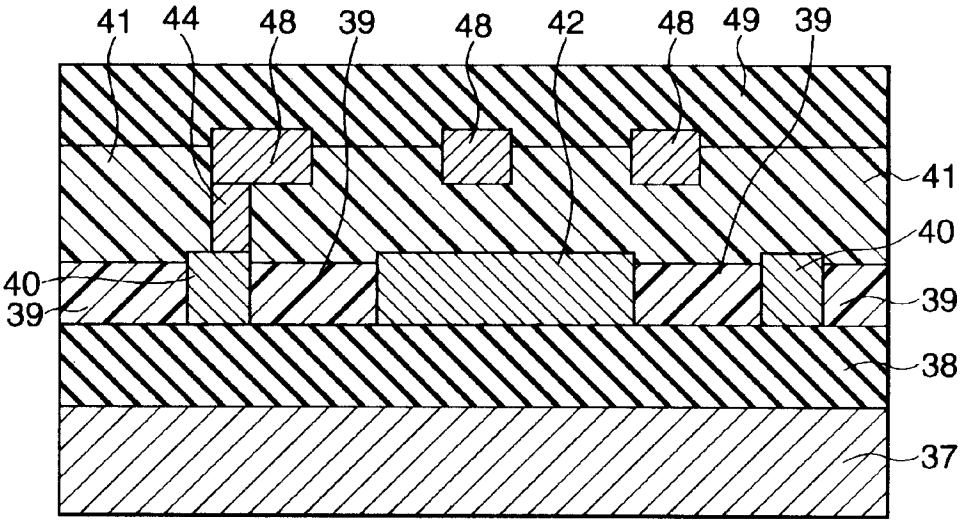

39
41
40
44
39
41
42
39
45
40
39
38
37

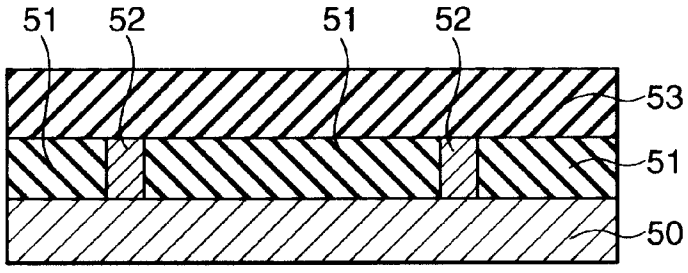

39
41
46
40
39
46
41
42
46
39
45
40
46
44
41
39
38
37

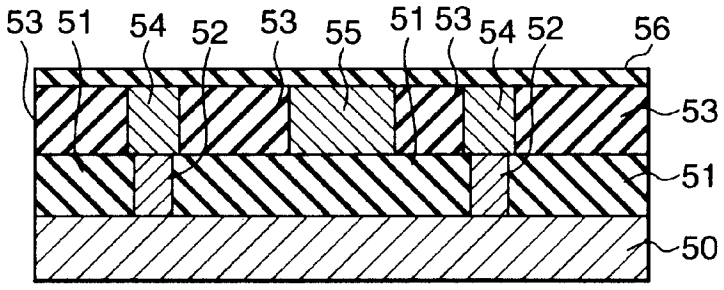

41
39
45
44
40
39
45
41
45
42
39
45
40
39
38
37

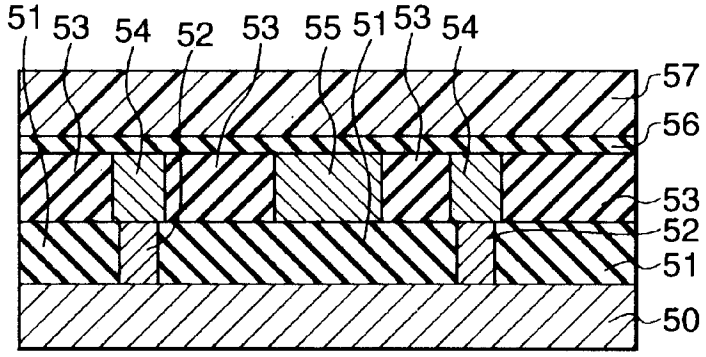

41
45
40
39
45
42
45
47
39
45
41
39
40
39
38
37

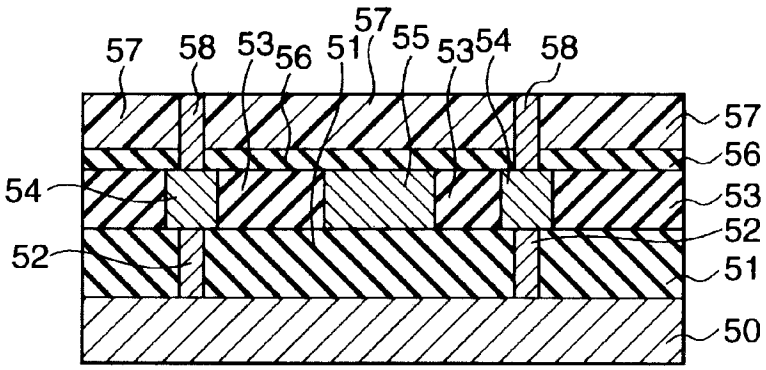

41
44
48
39
48
42
48
41
39
40
40
39
39
38
37

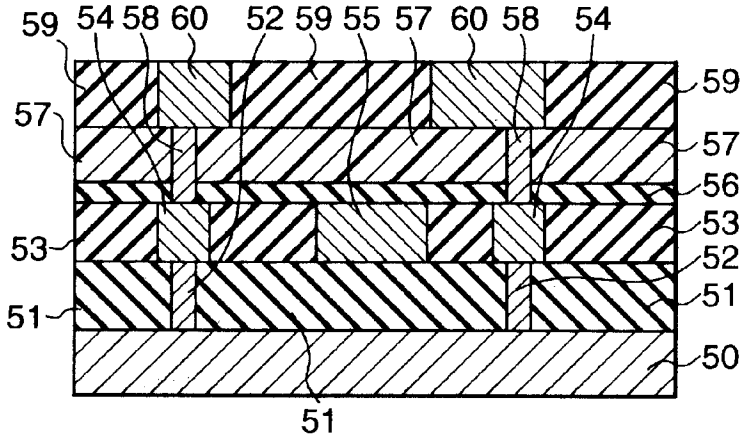

41
44
48
39
48
42
48
49
39
41
40
40
39
39
38
37

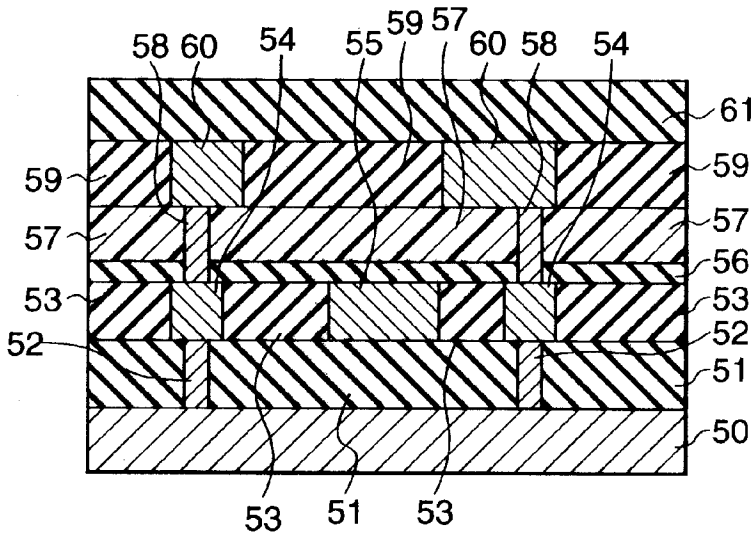

51
52
51
52
53
51
50

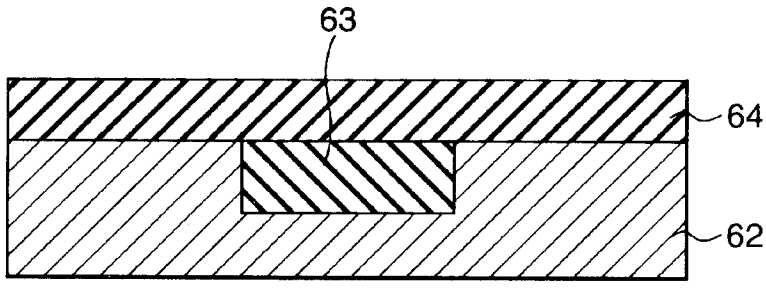

53
51
54
52
53
55
51
53
54
52
56
53
51
50

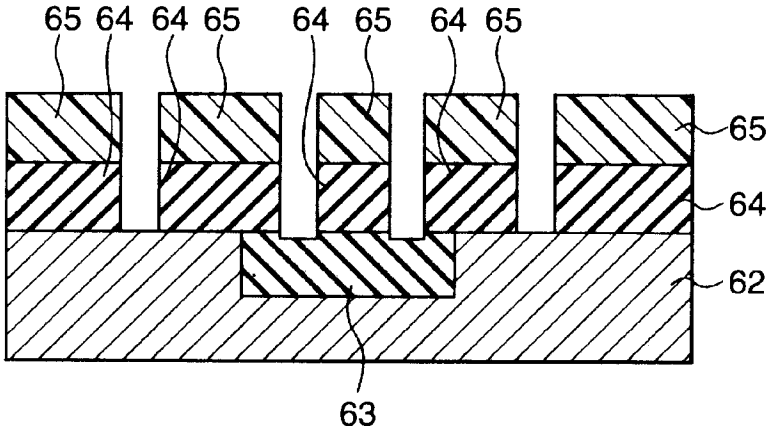

51
53
54
52
53
55
51
53
54
57
56
53
52
51
50

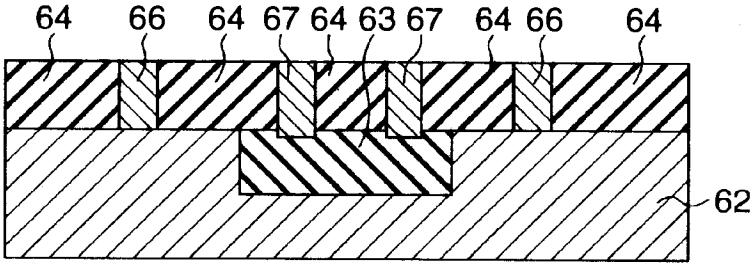

57
58
53
56
51
57
55
53
54
58
57
56
54
53
52
52
51
50

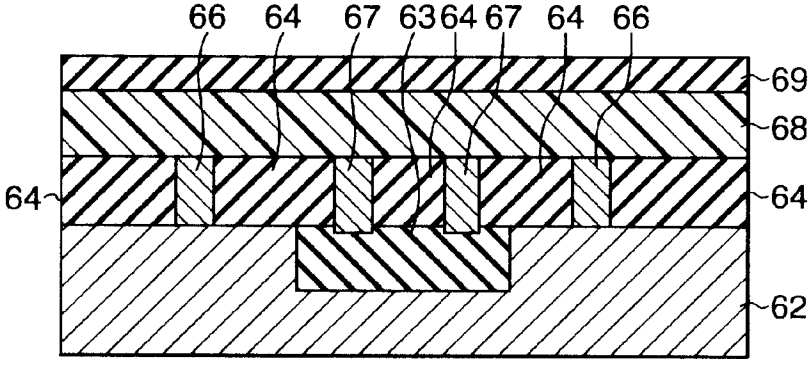

59
54
58
60
52
59
55
57
60
58
54
59
57
57
56
53
53
52
51
51
50
51

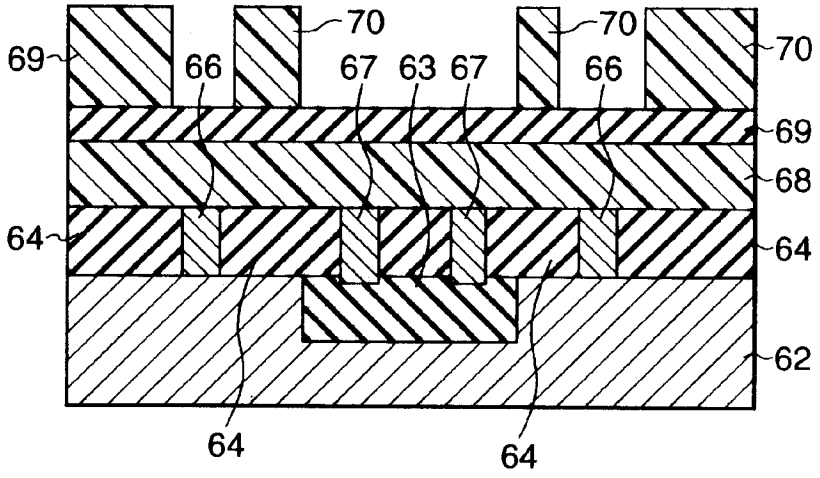

58
60
54
55
59
57
60
58
54
61
59
59
57
57
56
53
53
52
52
51
50
53
51
53

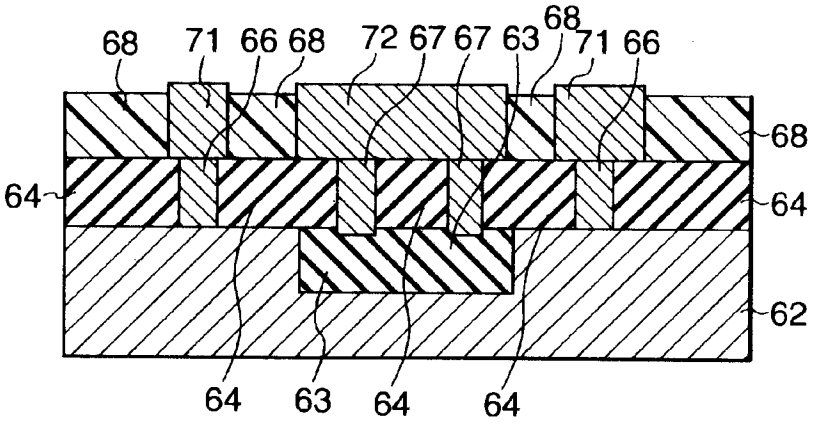

63
64
62

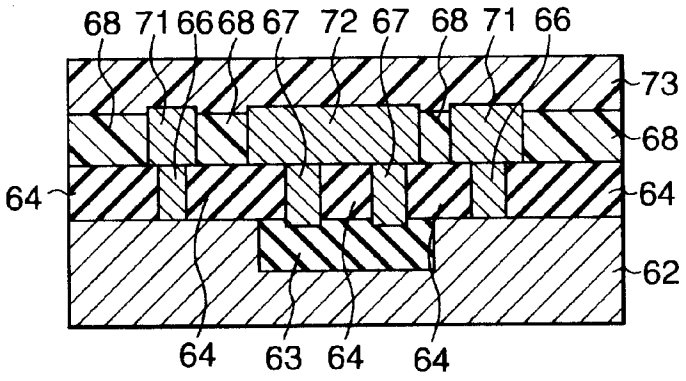

65 64 64 65 64 65 64 65
65
64
62
63

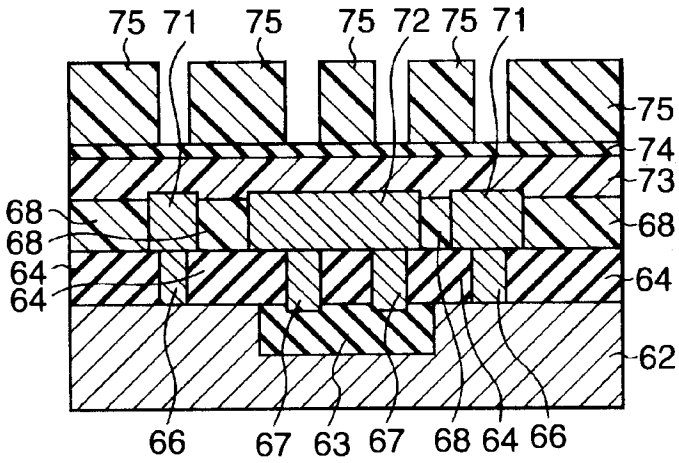

64 66 64 67 64 63 67 64 66 64
62

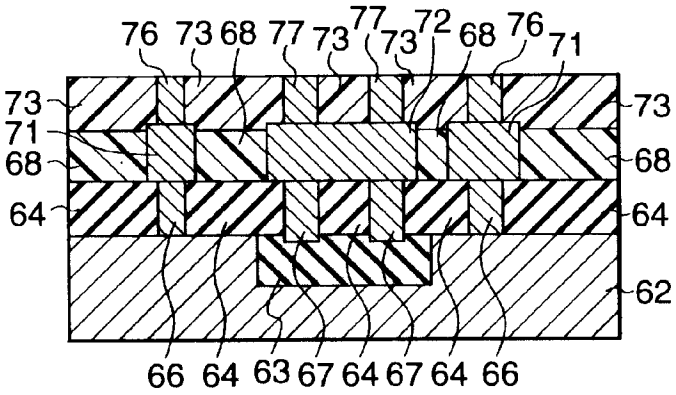

66 64 67 63 64 67 64 66
69
68
64
64
62

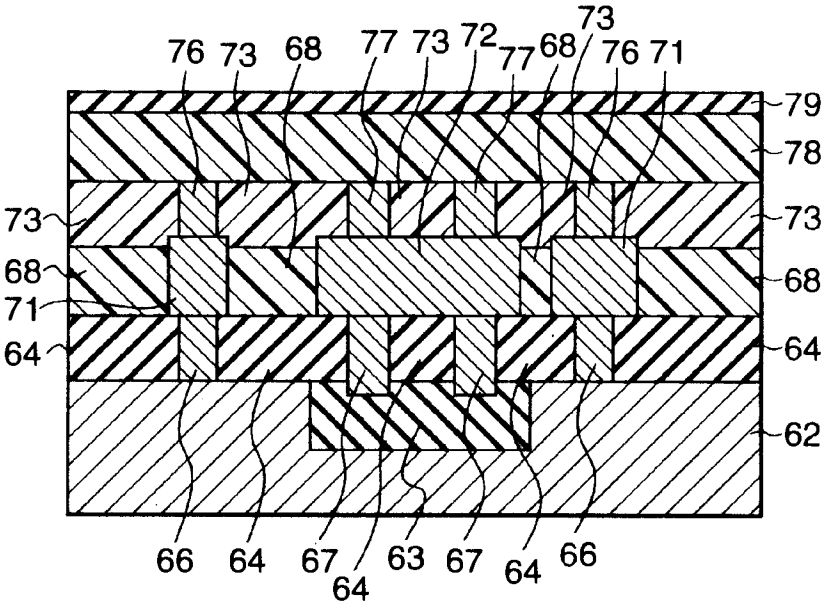

70
70
69
66
67
63
67
66
70
69
68
64
64
62
64
64

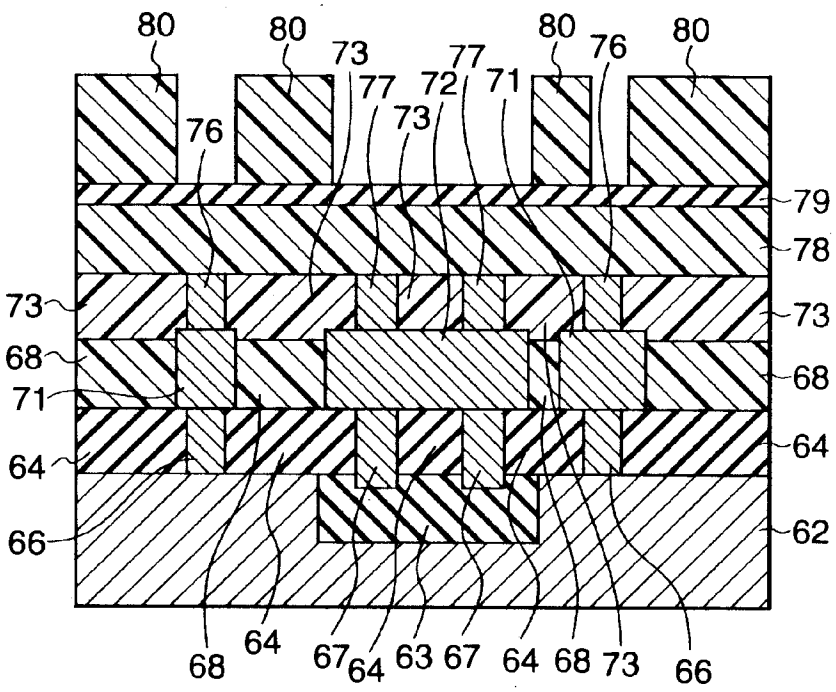

68
71
66
68
72
67
67
63
68
71
66
68
64
64
62
64
63
64
64

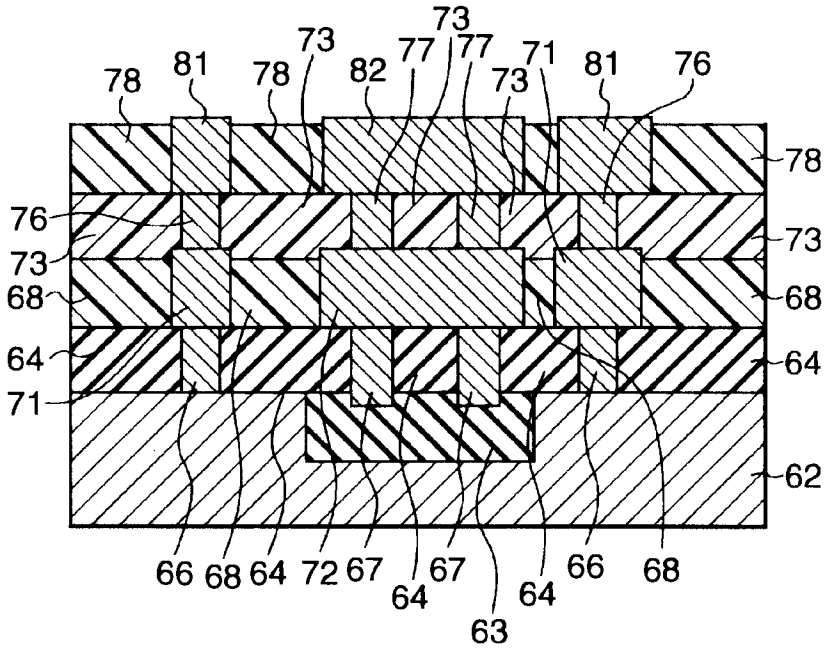

68
71
66
68
67
72
67
68
71
66
73
68
64
64
62
64
63
64
64

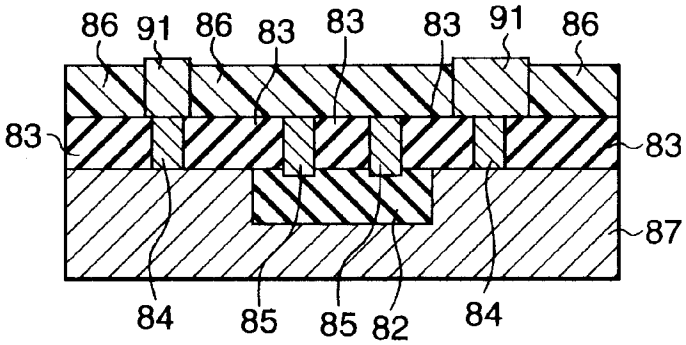

75 71 75 75 72 75 71
75
74
73
68
68
64
64
64
62
66 67 63 67 68 64 66

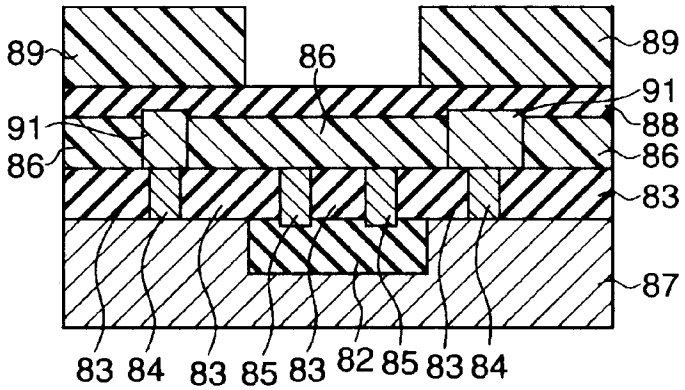

76 73 68 77 73 77 73 72 68 76 71
73
71
68
64
73
68
64
62
66 64 63 67 64 67 64 66

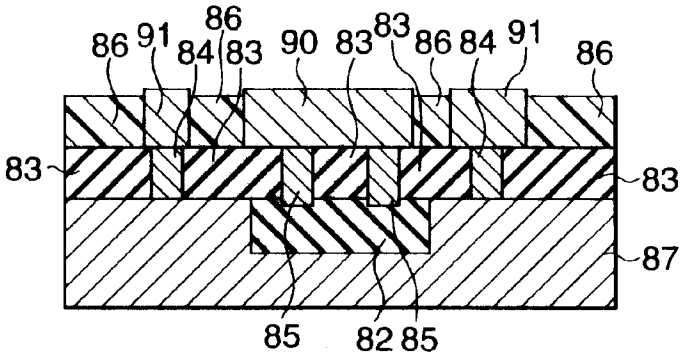

76
73
68
77
73
72
77
68
73
76
71
79
78
73
73
68
68
71
64
64
62
66
64
67
64
63
67
64
66

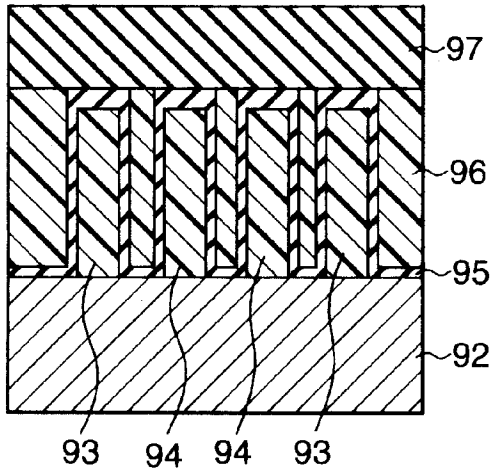

80
80
73
77
77
72
71
80
76
80
76
73
79
78
73
73
68
68
71
64
64
66
62
68
64
67
64
63
67
64
68
73
66

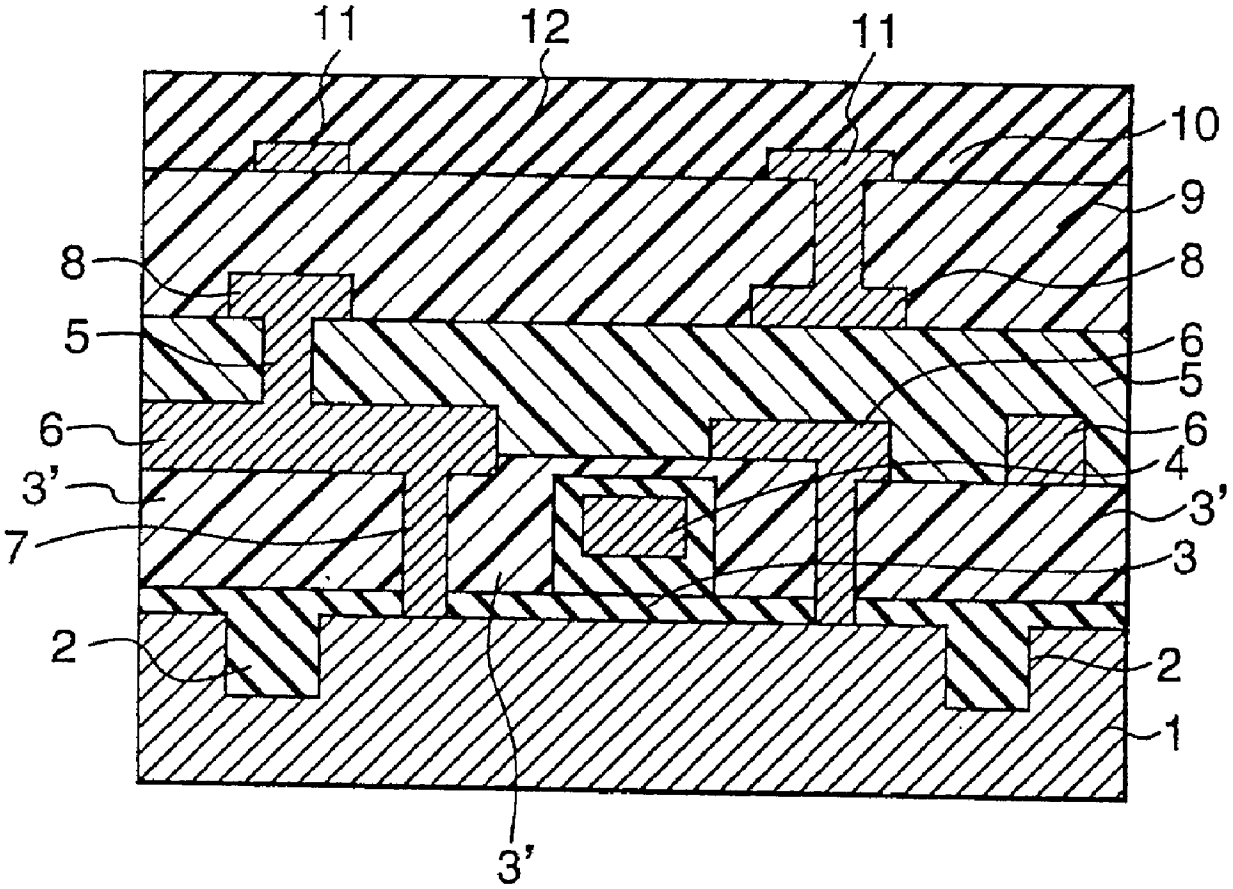

73
73
77
77
71
78
81
78
82
73
81
76
78
76
73
68
64
71
62
66
68
64
72
67
64
67
64
66
68
63


86
91
86
83
83
83
91
86
83
83
87
84
85
85
82
84


89
86
89
91
91
88
86
86
83
87
83 84 83 85 83 82 85 83 84


86
86 91 84 83 90 83 83 86 84 91 86
83
83
87
85 82 85


97
96
95
92
93 94 94 93



GF Exhibit 1124 - 2143/2704

Unexamined Patent Publication(A)

Bibliographic Data

Int.Cl.	H01L 21/768 | H01L 21/02 | H01L 21/312 | H01L 23/367
Published Date	20061201
Registration No.	1005987050000
Registration Date	20060703
Application No.	1019980049107
Application Date	19981116
Unexamined Publication No.	1019990045323
Unexamined Publication Date	19990625
Priority Claims	97-315682 | 19971117 | JP 98-37673 | 19980219 | JP 98-109983 | 19980420 | JP
Requested Date of Examination	20031017
Agent.	YOU ME PATENT & LAW FIRM | Kim Jae Man
Inventor	HaSeGaWaDoSiYaKi | NAKAYAMA HAJIME
Applicant	SONY CORPORATION
Rightholder	SONY CORPORATION

발명의 명칭

저유전율막을 가지는 반도체 장치 및 그 제조 방법

Title of Invention

SEMICONDUCTOR DEVICE HAVING LOW DIELECTRIC LAYER AND METHOD OF MANUFACTURING THE SAME C APABLE OF RESTRAINING EFFECTIVELY DEGRADATION OF THERMAL DIFFUSION EFFICIENCY

요약

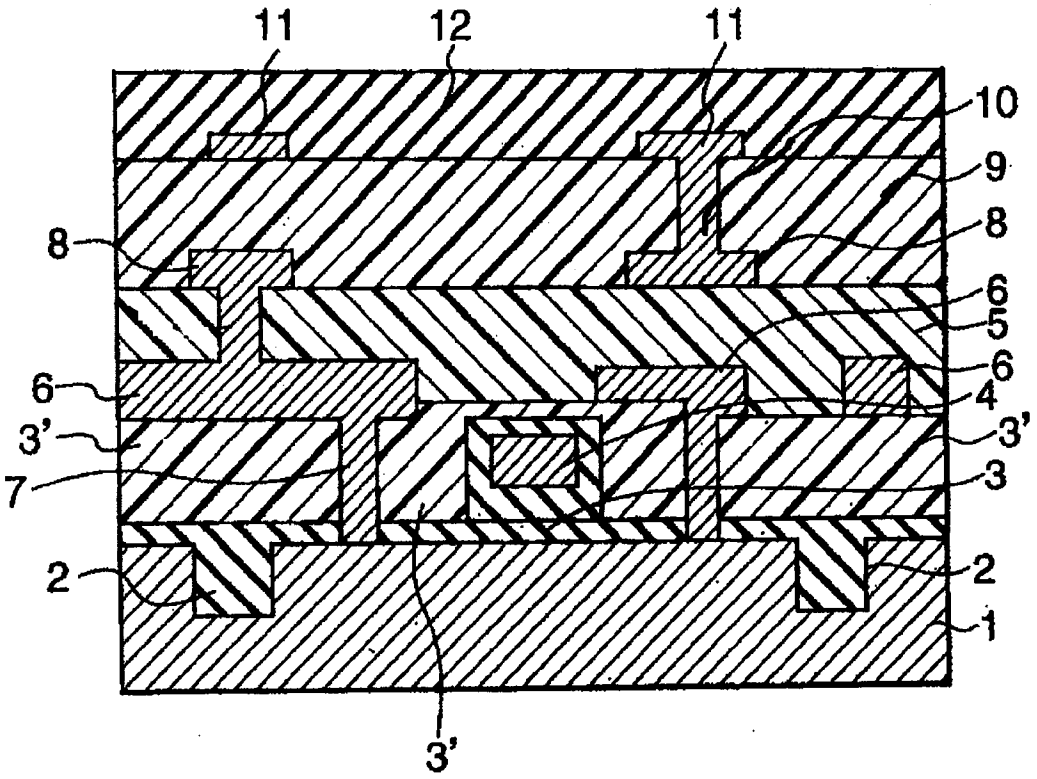
본 발명은 반도체 기판, 이 반도체 기판 위에 형성되는 절연막, 이 절연막 위에 형성되고 유전율비가 3.0 이하인 유전체 유기막과, 이 유전체 유기막 중에 절연막에 접하는 배선층을 포함하고, 배선층의 상면은 유전체 유기막의 상면보다 높은 반도체 장치와, 이러한 반도체 장치의 제조 방법을 제공한다.

Abstract

The present invention is to provide the manufacturing method of the semiconductor device, in which it includ es the semiconductor substrate, the insulating layer for med on this semiconductor substrate, the dielectric org anic layer which is formed on this insulating layer and, and the wiring layer contacting to the insulating layer a mong this dielectric organic layer and the upper side of the wiring layer is higher than the upper side of the diel ectric organic layer. And such semiconductor device. A s to the dielectric organic layer which is formed on thi s, the dielectric constant ratio is 3.0 or less.

대표도면(Representative drawing)

GF Exhibit 1124 - 2144/2704



청구의 범위

청구 1항:

반도체 기판과, 상기 반도체 기판 상에 형성된 절연막과,상기 절연막 상에 형성되고 유전율비가 3.0 이하인 제1 유전체막과, 상기 제1 유전체막 상에 형성되고 상기 절연막에 접하는 배선층을 포함하고, 상기 배선층의 상면이 상기 제1 유전체막의 상면보다 높게 형성되는 반도체 장치.

청구 2항:

제1항에 있어서, 상기 배선층과 제1 유전체막 상에 형성되고 최소한 3.0의 유전율비를 가지는 제2 유전체막을 추가로 포함하는 반도체 장치.

청구 3항:

제1항에 있어서, 상기 제1유전체막은 사이클릭 플루오로 레진, 폴리테트라플루오로에틸렌, 플루오르화 에틸렌 프로필렌, 테트라플루오로에틸렌 공중합체, 퍼플루오로알콕시에틸렌, 폴리플루오로비닐리덴, 폴리트리플루오로클로로에틸렌, 플루오로

Scope of Claims

Claim 1:

The semiconductor device in which it includes semiconductor substrate, the insulating layer formed o n the semiconductor substrate, the first dielectric film which is formed on the insulating layer and, and the wir ing layer ; and the upper side of the wiring layer is high formed than the upper side of the first dielectric film, a nd as to the first dielectric film which is formed on the, the dielectric constant ratio is 3.0 or less; and the wiri ng layer is formed on the first dielectric film and contac ts to the insulating layer.

Claim 2:

The semiconductor device of claim 1, further comprising the wiring layer and the second dielectric fil m which is formed on the first dielectric film and has th e dielectric constant rain of at least 3.0.

Claim 3:

As for claim 1, the semiconductor device for being made of the material of at least one selected from the group consisting of the polymer, the polymer having th e concatemer of repeating of being expressed as (2) (t

GF Exhibit 1124 - 2145/2704

아릴 에테르 레진, 폴리플루오로이미드, 벤조시클로부텐(BCB) 폴리머, 폴리이미드, 아몰퍼스 카본, 모노메틸트리하이드록시실란 (유기 SOG) 축합체, 하기의 식(1)로 표현되는 반복하는 단위 구조를 가지는 폴리머, (1)(상기 m, n은 자연수를 나타냄)하기의 식(2)로 표현되는 반복하는 단위 구조를 가지는 폴리머, (2)(상기 x, y, z은 각각 자연수를 나타냄)하기의 식(3)으로 표현되는 반복하는 단위 구조를 가지는 폴리머, (3)(상기 R은 알킬렌 또는 페닐렌 군을 나타냄)하기의 식(4)로 표현되는 반복하는 단위 구조를 가지는 폴리머 (4)(상기 R#39#는 알킬렌 또는 페닐렌 군을 나타냄)로 이루어지는 군으로부터 선택되는 최소한 하나의 재료로 이루어지는 반도체 장치.

he x, the y , and the z show the natural number) following formula (3), and the polymer (4) (the R' shows the alkylene or the phenylene group) having the concatemer of repeating of being expressed as (3) (R shows the alkylene or the phenylene group) following formula (4) wherein the first dielectric film has the concatemer of repeating of being expressed as the polymer, and (1) (the m , and the n show the natural number) following formula (2) that has the concatemer of repeating of being expressed as the cyclic *** in the resin, the poly tetra fluoro ethylene, the fluorinated ethylene propylene, the tetrafluoroethylene copolymer, the perfluoro alkoxy ethylene, the polyfluorovinylidene, the polytrifluorochloroethylene, the fluoroaryl ether resin, the poly fluoro imide, the benzocyclobutene (BCB) polymer, the polyimide, the amorphous carbon film, the monomethyl trihydroxy silane (organic spin on glass) condensation product, the following formula (1).

청구 4항:

Claim 4:

제1항에 있어서, 상기 제2 유전체막은 사이클릭 플루오로 레진, 폴리테트라플루오로에틸렌, 플루오로화 에틸렌 프로필렌, 테트라플루오로에틸렌 공중합체, 퍼플루오로알콕시에틸렌, 폴리플루오로비닐리덴, 폴리트리플루오로클로로에틸렌, 플루오로아릴 에테르 레진, 폴리플루오로이미드, 벤조시클로부텐 (BCB) 폴리머, 폴리이미드, 아몰퍼스 카본, 모노메틸트리하이드록시실란 (유기 SOG) 축합체, 하기의 식(5)로 표현되는 반복하는 단위 구조를 가지는 폴리머, (5)(상기 m, n은 자연수를 나타냄)하기의 식(6)으로 표현되는 반복하는 단위 구조를 가지는 폴리머, (6)(상기 x, y, z은 각각 자연수를 나타냄)하기의 식(7)로 표현되는 반복하는 단위 구조를 가지는 폴리머, (7)(상기 R은 알킬렌 또는 페닐렌 군을 나타냄)하기의 식(8)로 표현되는 반복하는 단위 구조를 가지는 폴리머 (8)(상기 R#39#는 알킬렌 또는 페닐렌 군을 나타냄)로 이루어지는 군으로부터 선택되는 최소한 하나의 재료로 이루어지는 반도체 장치.

As for claim 1, the semiconductor device for being made of the material of at least one selected from the group consisting of the polymer, the polymer having the concatemer of repeating of being expressed as (6) (the x, the y , and the z show the natural number) following formula (7), and the polymer (8) (the R' shows the alkylene or the phenylene group) having the concatemer of repeating of being expressed as (7) (R shows the alkylene or the phenylene group) following formula (8) wherein the second dielectric film has the concatemer of repeating of being expressed as the polymer, and (5) (the m , and the n show the natural number) following formula (6) that has the concatemer of repeating of being expressed as the cyclic *** in the resin, the poly tetra fluoro ethylene, the fluoro ethylene propylene, the tetrafluoroethylene copolymer, the perfluoro alkoxy ethylene, the polyfluorovinylidene, the polytrifluorochloroethylene, the fluoroaryl ether resin, the poly fluoro imide, the benzocyclobutene (BCB) polymer, the polyimide, the amorphous carbon film, the monomethyl trihydroxy silane (organic spin on glass) condensation product, the following formula (5).

청구 5항:

Claim 5:

제1항에 있어서, 상기 유전체막 중에 패턴에 대하여 최소한 3배 피치 이상의 배선간격 부분의 더미 배선을 가지는 반도체 장치.

As for claim 1, the semiconductor device for having the dummy line of the wiring space part more than at least treble pitch about the pattern among the dielectric film.

청구 6항:

Claim 6:

제5항에 있어서, 상기 더미 배선은 최소한 3배 피치 이상의 배선 간격의 부분에 모든 배선 간격이 1 ㎛ 이하가 되도록 형성되는 반도체 장치.

As for claim 5, the semiconductor device in which the dummy line all wiring spaces are formed in the part of the wiring space more than at least treble pitch so that 1 ㎛ this is.

청구 7항:

Claim 7:

제5항에 있어서, 상기 더미 배선의 아래의 절연막 중에 하층 도전층과 접속되지 않는 더미 콘택트홀을 추가로 포함하는 반도체 장치.

The semiconductor device of claim 5, further comprising the lower conductive layer among the following insulating layer of the dummy line and the dummy contact hole which is not connected.

GF Exhibit 1124 - 2146/2704

청구 8항:

반도체 기판과,상기 반도체 기판 상에 형성되는 절연막과,상기 절연막 상에 크세로겔을 함유하는 막과,상기 크세로겔을 함유하는 막중에 형성되고, 상기 절연막에 접하는 배선층을 포함하는 반도체 장치.

Claim 8:

The semiconductor device including semiconductor substrate, the insulating layer formed on the semiconductor substrate, the film containing the xerogel on the insulating layer, and the wiring layer, and the wiring layer is formed in the valuableness containing the xerogel ; and contacts to the insulating layer.

청구 9항:

제8항에 있어서, 상기 배선층의 상면이 상기 크세로겔을 함유하는 막의 상면보다 높게 형성되어 있는 반도체 장치.

Claim 9:

As for claim 8, the semiconductor device in which the upper side of the wiring layer is high formed than the upper side of the film containing the xerogel.

청구 10항:

제8항에 있어서, 상기 크세로겔을 함유하는 막 중에 패턴에 대하여 최소한 3배 피치 이상의 배선 간격 부분의 상기 크세로겔을 함유하는 막중에 더미 배선을 가지는 반도체 장치.

Claim 10:

As for claim 8, the semiconductor device for having the dummy line on the valuableness containing the xerogel of the wiring space part more than at least treble pitch among the film containing the xerogel about the pattern.

청구 11항:

제10항에 있어서, 상기 더미 배선은 최소한 3배 피치 이상의 배선 간격의 부분에 모든 배선 간격이 1 ㎛ 이하로 되도록 형성되어 있는 반도체 장치.

Claim 11:

As for claim 10, the semiconductor device in which the dummy line all wiring spaces are formed in the part of the wiring space more than at least treble pitch as as possible.

청구 12항:

제10항에 있어서, 상기 더미 배선의 아래의 절연막 중에 형성되고 하층 도전층과 접속되지 않는 더미 콘택트홀을 추가로 포함하는 반도체 장치.

Claim 12:

The semiconductor device of claim 10, further comprising the lower conductive layer it is formed among the following insulating layer of the dummy line and the dummy contact hole which is not connected.

청구 13항:

제8항에 있어서, 상기 크세로겔을 함유하는 막위 또는 막아래에 실란 커플링제를 함유하는 막을 추가로 포함하는 반도체 장치.

Claim 13:

As for claim 8, the semiconductor device further comprising the film the upper part containing the xerogel or the film containing the silane coupling agent in under film.

청구 14항:

제8항에 있어서, 상기 크세로겔을 함유하는 막이 배선 패턴에 대하여 3배 피치 이하의 배선 간격 부분의 상기 절면막의 위에 형성되어 있는 반도체 장치.

Claim 14:

As for claim 8, the semiconductor device in which the film containing the xerogel is formed in the upper part of the surface layer of the wiring space part less than the treble pitch about the wiring pattern.

청구 15항:

반도체 기판과, 상기 반도체 기판 상에 형성된 절연막과, 상기 절연막 상에 형성되고 유전율비가 3.0 이하인 제1 유전체막과, 상기 제1 유전체막 상에 크세로겔을 함유하는 막과,상기 크세로겔을 함유하는 막 상에 형성되고 유전율비가 3.0 이하인 제2 유전체막과,상기 크세로겔을 함유하는 막중에 형성되고 상기 절연막에 접하는 배선층을 포함하는 반도체 장치.

Claim 15:

The semiconductor device including semiconductor substrate, the insulating layer formed on the semiconductor substrate, the first dielectric film which is formed on the insulating layer and, the film containing the xerogel on the first dielectric film, the second dielectric film which is formed on the film containing the xerogel and, and the wiring layer, and as to the first dielectric film which is formed on the, the dielectric constant ratio is 3.0 or less; as to the second dielectric film which is formed on the film, the dielectric constant ratio is 3.0 or less; and the wiring layer is formed in the valuableness

GF Exhibit 1124 - 2147/2704

containing the xerogel and contacts to the insulating la yer.

청구 16항:

제15항에 있어서, 상기 배선층의 상면이 상기 크세로겔을 함유하는 막의 상면보다 높게 형성되는 반도체 장치.

Claim 16:

As for claim 15, the semiconductor device in which the upper side of the wiring layer is high formed than the u pper side of the film containing the xerogel.

청구 17항:

제15항에 있어서, 상기 유전율비가 3.0 이하인 제2 유전체막 중에 형성되고 배선들을 접속하기 위한 콘택트홀을 추가로 포함하는 반도체 장치.

Claim 17:

As for claim 15, the semiconductor device further comprising the contact hole for being formed among th e second dielectric film in which the dielectric constant ratio is 3.0 or less and connecting wirings.

청구 18항:

제15항에 있어서, 상기 크세로겔을 함유하는 막 중에 배선 패턴에 대하여 최소한 3배 피치 이상의 배선 간격부분의 더미 배선을 가지는 반도체 장치.

Claim 18:

As for claim 15, the semiconductor device for having the dummy line of the wiring space part more than at l east treble pitch about the wiring pattern among the fil m containing the xerogel.

청구 19항:

제18항에 있어서, 상기 더미 배선은 최소한 3배 피치 이상의 배선 간격의 부분에 모든 배선 간격이 1 ㎛ 이하가 되도록 형성되는 반도체 장치.

Claim 19:

As for claim 18, the semiconductor device in which the dummy line all wiring spaces are formed in the part of t he wiring space more than at least treble pitch so that 1 ㎛ this is.

청구 20항:

제15항에 있어서, 상기 더미 배선의 아래의 절연막 중에 형성되고 하층 도전층과 접속되지 않는 더미 콘택트홀을 추가로 포함하는 반도체 장치.

Claim 20:

The semiconductor device of claim 15, further comprising the lower conductive layer it is formed amon g the following insulating layer of the dummy line and t he dummy contact hole which is not connected.

청구 21항:

제15항에 있어서, 상기 크세로겔을 함유하는 막위 또는 막아래에 실란 커플링제를 함유하는 막을 추가로 포함하는 반도체 장치.

Claim 21:

As for claim 15, the semiconductor device further comprising the film the upper part containing the xerog el or the film containing the silane coupling agent in un der film.

청구 22항:

반도체 기판 상에 절연막을 형성하는 공정과,상기 절연막 위에 유전율비가 3.0 이하인 유전체막을 형성하는 공정과,상기 유전체막 위에 무기막을 형성하는 공정과,상기 무기막에 배선층을 형성하기 위한 패턴을 형성하는 공정과,상기 배선층을 전체 표면상에 형성하는 공정과,상기 배선층의 표면을 연마하는 공정과,상기 무기막을 제거하는 공정을 포함하는 반도체 장치의 제조 방법.

Claim 22:

The method for manufacturing semiconductor device including the process of forming the insulating layer on the semiconductor substrate, the process of forming th e dielectric film, the process of forming the inorganic fil m on the dielectric film, the process of forming the patt ern for forming the wiring layer on the inorganic film, th e process of forming the wiring layer on the whole surf ace, the process of polishing the surface of the wiring l ayer, and the process of removing the inorganic film, a nd as to the process of, the dielectric constant ratio is 3.0 or less on the insulating layer.

청구 23항:

제22항에 있어서, 상기 배선층의 상면을 연마하는 공정이 화학적 기계적 연마(CMP)법에 의한 연마 공정인 반도체 장치의 제조 방법.

Claim 23:

As for claim 22, the method for manufacturing semiconductor device in which the process of polishing the upper side of the wiring layer is the polishing proce ss by the chemical mechanical polishing (CMP) method.

GF Exhibit 1124 - 2148/2704

청구 24항:

반도체 기판 상에 절연막을 형성하는 공정과,상기 절연막의 위에 유전율비가 3.0 이하인 유전체막을 형성하는 공정과,상기 유전체막 위에 무기막을 형성하는 공정과,상기 무기막에 배선층을 형성하기 위한 패턴을 형성하는 공정과,상기 배선층을 전체 표면상에 형성하는 공정과,상기 배선층의 상면을 연마하는 공정과,상기 무기막을 제거하는 공정과,배선 패턴에 대하여, 상기 유전체막 중에 최소한 3배 피치 이상의 배선 간격 부분의 더미 배선을 형성하는 공정을 포함하는 반도체 장치의 제조 방법.

Claim 24:

The method for manufacturing semiconductor device including the process of forming the insulating layer on the semiconductor substrate, the process of forming th e dielectric film, the process of forming the inorganic fil m on the dielectric film, the process of forming the patt ern for forming the wiring layer on the inorganic film, th e process of forming the wiring layer on the whole surf ace, the process of polishing the upper side of the wiri ng layer, the process of removing the inorganic film, an d the process of forming the dummy line of the wiring s pace part more than at least treble pitch about the wiri ng pattern among the dielectric film, and as to the pro cess of, the dielectric constant ratio is 3.0 or less on t he upper part of the insulating layer.

청구 25항:

제24항에 있어서, 상기 배선층의 상면을 연마하는 공정이 화학적 기계적 연마(CMP)법에 의한 연마 공정인 반도체 장치의 제조 방법.

Claim 25:

As for claim 24, the method for manufacturing semiconductor device in which the process of polishing the upper side of the wiring layer is the polishing proce ss by the chemical mechanical polishing (CMP) method.

청구 26항:

반도체 기판 상에 절연막을 형성하는 공정과,상기 절연막 위에 유전율비가 3.0 이하인 유전체막을 형성하는 공정과,상기 유전체막 위에 무기막을 형성하는 공정과,상기 무기막에 배선층 및 더미 배선층을 형성하기 위한 패턴을 형성하는 공정과,상기 배선층 및 더미 배선층을 전체 표면상에 형성하는 공정과,상기 배선층과 더미 배선층의 상면을 연마하는 공정과,상기 무기막을 제거하는 공정을 포함하는 반도체 기판의 제조 방법.

Claim 26:

The manufacturing method of the semiconductor substrate which comprises the process of forming the i nsulating layer on the semiconductor substrate, the wir ing layer in the process, of forming the dielectric film in which the dielectric constant ratio is 3.0 or less on the insulating layer and the process, of forming the inorgani c film on the dielectric film and inorganic film, and the p rocess, of forming the pattern for forming the dummy w iring layer and wiring layer and the process of forming t he dummy wiring layer on the whole surface and the pr ocess, of polishing the upper side of the dummy wiring l ayer and wiring layer and the process of removing the i norganic film.

청구 27항:

제26항에 있어서, 상기 배선층의 상면을 연마하는 공정이 화학적 기계적 연마(CMP)법에 의한 연마 공정인 반도체 장치의 제조 방법.

Claim 27:

As for claim 26, the method for manufacturing semiconductor device in which the process of polishing the upper side of the wiring layer is the polishing proce ss by the chemical mechanical polishing (CMP) method.

청구 28항:

반도체 기판 상에 절연막을 형성하는 공정과,상기 절연막 위에 유전율비가 3.0 이하인 유전체막을 형성하는 공정과,상기 유전체막 위에 무기막을 형성하는 공정과,상기 무기막에 배선층 및 더미 배선층을 형성하기 위한 패턴을 형성하는 공정과,상기 배선층 및 더미 배선층을 전체 표면상에 형성하는 공정과,상기 배선층의 상면을 연마하는 공정과,상기 무기막을 제거하는 공정과, 상기 절연막 중에 상층 배선과 하층 도전층을 접속하기 위한 콘택트홀, 및 상기 더미 배선의 아래의 절연막 중에 하층 도전층과 접속되지 않는 더미 콘택트홀을 형성하는 공정을 포함하는 반도체 장치의 제조 방법.

Claim 28:

The method for manufacturing semiconductor device which comprises the process of forming the insulating l ayer on the semiconductor substrate, the wiring layer i n the process, of forming the dielectric film in which th e dielectric constant ratio is 3.0 or less on the insulatin g layer and the process, of forming the inorganic film o n the dielectric film and inorganic film, and the process, of forming the pattern for forming the dummy wiring lay er and wiring layer and the process of forming the dum my wiring layer on the whole surface and the process, of polishing the upper side of the wiring layer and the p rocess, of removing the inorganic film and the process of forming the contact hole for connecting the upper le vel wiring line and lower conductive layer among the in sulating layer and the dummy contact hole which is not

GF Exhibit 1124 - 2149/2704

connected with the lower conductive layer among the f ollowing insulating layer of the dummy line.

청구 29항:

제28항에 있어서, 상기 배선층의 상면을 연마하는 공정이 화학적 기계적 연마(CMP)법에 의한 연마 공정인 반도체 장치의 제조 방법.

Claim 29:

As for claim 28, the method for manufacturing semiconductor device in which the process of polishing the upper side of the wiring layer is the polishing proce ss by the chemical mechanical polishing (CMP) method.

청구 30항:

제28항에 있어서, 상기 무기막에 배선층 및 더미 배선층을 형성하기 위한 패턴을 형성하는 공정이, 배선 패턴 및 더미 배선 패턴에 대하여 최소한 3배 피치 이상의 배선 간격 부분에 상기 더미 배선을 형성하기 위한 패턴을 동시에 형성하는 공정인 반도체 장치의 제조 방법.

Claim 30:

As for claim 28, the method for manufacturing semiconductor device which is the process where the p rocess of forming the wiring layer and the pattern for f orming the dummy wiring layer on the inorganic film sim ultaneously forms the wiring pattern and the pattern fo r forming the dummy line on the wiring space part more than at least treble pitch about the dummy line patter n.

청구 31항:

반도체 기판 상에 절연막을 형성하는 공정과,상기 절연막 위에 유전율비가 3.0 이하인 유전체막을 형성하는 공정과,상기 유전체막 위에 크세로겔을 함유하는 막을 형성하는 공정과,상기 크세로겔을 함유하는 막 상에 무기막을 형성하는 공정과,상기 무기막에 배선층을 형성하기 위한 패턴을 형성하는 공정과,상기 배선층을 전체 표면상에 형성하는 공정과,상기 배선층의 상면을 연마하는 공정과,상기 무기막을 제거하는 공정을 포함하는 반도체 장치의 제조 방법.

Claim 31:

The method for manufacturing semiconductor device including the process of forming the insulating layer on the semiconductor substrate, the process of forming th e dielectric film, the process of forming the film containi ng the xerogel on the dielectric film, the process of for ming the inorganic film on the film containing the xerog el, the process of forming the pattern for forming the w iring layer on the inorganic film, the process of forming the wiring layer on the whole surface, the process of p olishing the upper side of the wiring layer, and the proc ess of removing the inorganic film, and as to the proce ss of, the dielectric constant ratio is 3.0 or less on the insulating layer.

청구 32항:

제31항에 있어서, 상기 배선층의 상면을 연마하는 공정이 화학적 기계적 연마(CMP)법에 의한 연마 공정인 반도체 장치의 제조 방법.

Claim 32:

As for claim 31, the method for manufacturing semiconductor device in which the process of polishing the upper side of the wiring layer is the polishing proce ss by the chemical mechanical polishing (CMP) method.

청구 33항:

제31항에 있어서, 상기 유전체막 상에 크세로겔을 함유하는 막을 형성하는 공정이, 상기 배선 패턴에 대하여 3배 피치 이하의 배선 간격 부분에 상기 크세로겔을 함유하는 막을 형성하는 공정인 반도체 장치의 제조 방법.

Claim 33:

As for claim 31, the method for manufacturing semiconductor device which is the process where the p rocess of forming the film containing the xerogel on the dielectric film forms the film containing the xerogel on t he wiring space part less than the treble pitch about th e wiring pattern.

청구 34항:

제31항에 있어서, 상기 크세로겔을 함유하는 막을 형성하는 공정의 전 또는 후에, 실란 커플링제를 함유하는 막을 형성하는 공정을 추가로 포함하는 반도체 장치의 제조 방법.

Claim 34:

As for claim 31, the method for manufacturing semiconductor device further comprising the process of forming total or the film containing the silane coupling a gent of the process of forming the film containing the x erogel.

청구 35항:

반도체 기판 상에 절연막을 형성하는 공정과,상기 절연막 위에

Claim 35:

The method for manufacturing semiconductor device

GF Exhibit 1124 - 2150/2704

유전율비가 3.0 이하인 유전체막을 형성하는 공정과,상기 유전체막 위에 크세로겔을 함유하는 막을 형성하는 공정과,상기 크세로겔을 함유하는 막 상에 무기막을 형성하는 공정과,상기 무기막에 배선층 및 더미 배선층을 형성하기 위한 패턴을 형성하는 공정과,상기 배선층 및 더미 배선층을 전체 표면상에 형성하는 공정과,상기 배선층 및 더미 배선층의 상면을 연마하는 공정과,상기 무기막을 제거하는 공정을 포함하는 반도체 장치의 제조 방법.

which comprises the process of forming the insulating layer on the semiconductor substrate, the wiring layer in the process, of forming the dielectric film in which the dielectric constant ratio is 3.0 or less on the insulating layer and the process, of forming the film containing the xerogel on the dielectric film and the process, of forming the inorganic film on the film containing the xerogel and inorganic film, and the process, of forming the pattern for forming the dummy wiring layer and wiring layer and the process of forming the dummy wiring layer on the whole surface and the process, of polishing the upper side of the dummy wiring layer and wiring layer and the process of removing the inorganic film.

청구 36항:

Claim 36:

제35항에 있어서, 상기 배선층의 상면을 연마하는 공정이 화학적 기계적 연마(CMP)법에 의한 연마 공정인 반도체 장치의 제조 방법.

As for claim 35, the method for manufacturing semiconductor device in which the process of polishing the upper side of the wiring layer is the polishing process by the chemical mechanical polishing (CMP) method.

청구 37항:

Claim 37:

제35항에 있어서, 상기 무기막 상에 배선층 및 더미 배선층을 형성하기 위한 패턴을 형성하는 공정이, 상기 무기막 상에 배선 패턴 및 배선 패턴에 대하여 최소한 3배 피치 이상의 배선 간격 부분에 배선층 및 더미 배선층을 형성하기 위한 패턴을 동시에 형성하는 공정인 반도체 장치의 제조 방법.

As for claim 35, the method for manufacturing semiconductor device in which the process of forming the wiring layer and the pattern for forming the dummy wiring layer on the inorganic film is the wiring pattern and the process of simultaneously forming the wiring layer and the pattern for forming the dummy wiring layer about the wiring pattern on the wiring space part more than at least treble pitch on the inorganic film.

청구 38항:

Claim 38:

제35항에 있어서, 상기 유전체막 상에 크세로겔을 함유하는 막을 형성하는 공정이, 상기 배선 패턴에 대하여 3배 피치 이하의 배선 간격 부분에 상기 크세로겔을 함유하는 막을 형성하는 공정인 반도체 장치의 제조 방법.

As for claim 35, the method for manufacturing semiconductor device which is the process where the process of forming the film containing the xerogel on the dielectric film forms the film containing the xerogel on the wiring space part less than the treble pitch about the wiring pattern.

청구 39항:

Claim 39:

제35항에 있어서, 상기 크세로겔을 함유하는 막을 형성하는 공정의 전 또는 후에, 실린 커플링제를 함유하는 층을 형성하는 공정을 추가로 포함하는 반도체 장치의 제조 방법.

As for claim 35, the method for manufacturing semiconductor device further comprising the process of forming the layer containing total or the later loaded coupling agent of the process of forming the film containing the xerogel.

청구 40항:

Claim 40:

반도체 기판 상에 절연막을 형성하는 공정과,상기 절연막 위에 유전율비가 3.0 이하인 유전체막을 형성하는 공정과,상기 유전체막 위에 크세로겔을 함유하는 막을 형성하는 공정과,상기 크세로겔을 함유하는 막 상에 무기막을 형성하는 공정과,상기 무기막에 배선층 및 더미 배선을 형성하기 위한 패턴을 형성하는 공정과,상기 배선층 및 더미 배선층을 전체 표면상에 형성하는 공정과,상기 배선층 및 더미 배선층의 상면을 연마하는 공정과,상기 무기막을 제거하는 공정과,상기 절연막 중에 상층 배선과 하층 도전층을 접속하기 위한 콘택트홀, 및 상기 더미 배선의 아래의 절연막 중에 하층 도전층과 접속되지 않는 더미 콘택트홀을 형성하는 공정을 포함하는 반도체 장치의 제조 방법.

The method for manufacturing semiconductor device which comprises the process of forming the insulating layer on the semiconductor substrate, the wiring layer in the process, of forming the dielectric film in which the dielectric constant ratio is 3.0 or less on the insulating layer and the process, of forming the film containing the xerogel on the dielectric film and the process, of forming the inorganic film on the film containing the xerogel and inorganic film, and the process, of forming the pattern for forming the dummy line and wiring layer and the process of forming the dummy wiring layer on the whole surface and the process, of polishing the upper side of the dummy wiring layer and wiring layer and the process, of removing the inorganic film and the process

GF Exhibit 1124 - 2151/2704

of forming the contact hole for connecting the upper le vel wiring line and lower conductive layer among the in sulating layer and the dummy contact hole which is not connected with the lower conductive layer among the f ollowing insulating layer of the dummy line.

청구 41항:

제40항에 있어서, 상기 배선층의 상면을 연마하는 공정이 화학적 기계적 연마(CMP)법에 의한 연마 공정인 반도체 장치의 제조 방법.

Claim 41:

As for claim 40, the method for manufacturing semiconductor device in which the process of polishing the upper side of the wiring layer is the polishing proce ss by the chemical mechanical polishing (CMP) method.

청구 42항:

제40항에 있어서, 상기 무기막 상에 배선층 및 더미 배선층을 형성하기 위한 패턴을 형성하는 공정이, 상기 무기막 상에 배선 패턴 및 배선 패턴에 대하여 최소한 3배 피치 이상의 배선 간격 부분에 더미 배선층을 형성하기 위한 패턴을 동시에 형성하는 공정인 반도체 장치의 제조 방법.

Claim 42:

As for claim 40, the method for manufacturing semiconductor device which is the process where the p rocess of forming the wiring layer and the pattern for f orming the dummy wiring layer on the inorganic film sim ultaneously forms the wiring pattern and the pattern fo r forming the dummy wiring layer on the wiring space p art more than at least treble pitch about the wiring pat tern on the inorganic film.

청구 43항:

제40항에 있어서, 상기 유전체막 상에 크세로겔을 함유하는 막을 형성하는 공정이, 상기 배선 패턴에 대하여 3배 피치 이하의 배선 간격 부분에 상기 크세로겔을 함유하는 막을 형성하는 공정인 반도체 장치의 제조 방법.

Claim 43:

As for claim 40, the method for manufacturing semiconductor device which is the process where the p rocess of forming the film containing the xerogel on the dielectric film forms the film containing the xerogel on t he wiring space part less than the treble pitch about th e wiring pattern.

청구 44항:

제40항에 있어서, 상기 크세로겔을 함유하는 막을 형성하는 공정의 전 또는 후에, 실란 커플링제를 함유하는 막을 형성하는 공정을 추가로 포함하는 반도체 장치의 제조 방법.

Claim 44:

As for claim 40, the method for manufacturing semiconductor device further comprising the process of forming total or the film containing the silane coupling a gent of the process of forming the film containing the x erogel.

배경기술

이 발명은 저유전율막을 층간 절연막으로서 사용한 반도체 장치의 형성 방법 및 반도체 장치의 구조에 관한 것으로, 특히, 0.25㎛ 룰(rule) 이하의 디바이스 프로세스에 사용될 수 있는 다층 배선 형성 기술에 관한 것이다.

Background Art

This invention relates to the multilayers forming technology which can be used for especially, the devic e process less than 0.25㎛ rule as the structure of the semiconductor device and the methods of forming semi conductor devices using the low-dielectric-layer as the inter-layer insulating film.

근년의 반도체 장치의 미세화에 따라, 배선의 미세화, 배선 피치(pitch)의 축소화가 필요되고 있다. 또, 동시에, 저소비 전력화 및 고속화 등의 요구에 따라서, 층간 절연막의 저유전율화도 요구되고 있다. 특히, 로직(logic)계의 디바이스에서는, 미세 배선에 의한 저항 상승, 배선 용량의 증가가 디바이스의 스피드 열화로 이어짐으로써, 미세하고 또한 저유전율막을 층간 절연막으로 하는 다층 배선이 요구불가결이다.

According to the miniaturization of the recent semiconductor device, the miniaturization of wiring, an d the demagnification of the wiring Pitch are necessitat ed. And according to simultaneously, the demand inclu ding the low consumption power and high speed etc, th e low permittivity of the inter-layer insulating film is req uired. Especially, in the device of the logic group, the i ncrease of resistance by the microwiring, and the incre ase of the wiring capacitance are in succession to the speed deterioration of the device. In that way the mult ilayer interconnection minute and having moreover, the low-dielectric-layer as the inter-layer insulating film is t he payment on demand passage.

GF Exhibit 1124 - 2152/2704

따라서, 배선폭의 미세화, 피치의 축소화는 배선 자체의 종횡비를 크게 할 뿐만 아니라, 배선간의 스페이스의 어스펙트비(aspect ratio)를 크게 하고, 결과로서 세로로 가늘고 긴 미세 배선을 형성하는 기술, 미세한 배선간을 층간막으로 매입하는 기술 등에 부담이 걸리고, 프로세스를 복잡하게 함과 동시에 프로세스의 수의 증대를 초래한다.

Therefore, the enlargement of the number of process the forms the long microwiring which is longways thin a nd as the result technology, make the process complic ated the miniaturization of the wiring width , and the d emagnification of pitch do the aspect ratio of the wirin g itself and In addition it makes the aspect rate of spa ce between wiring large and the burden hangs on the t echnology, which technology etc. Imports the minute wiring liver the inter-layer film is caused.

이러한 문제를 해결하는 것으로서, 종래에, 비아와 배선홈을 알루미늄 리플로우 스퍼터링(reflow sputtering)으로 동시에 매입하고, CMP (Chemical Mechanical Polishing) 법에 의해 표면의 알루미늄을 연마하는 이른바 다마신(damascene) 프로세스가 알려져 있다.

Such problem is resolved. The via and interconnection groove are simultaneously purchased in the convention to the aluminum -reflow sputtering and the damascene process polishing the aluminum of the surface with the CMP (Chemical Mechanical Polishing) method is known.

이 다마신 프로세스는 높은 아스펙트비의 알루미늄 배선을 에칭으로 형성하는 것도, 배선간의 좁은 간격을 층간막으로 매입할 필요도 없고, 대폭으로 프로세스수를 줄이는 것이 가능하다. 이 프로세스는 배선 어스펙트비가 높게 되는 만큼, 그리고 배선 총수가 증대하는 만큼, 토탈 코스트의 삭감에 기여하게 된다. 또한, 층간 절연막의 저유전율화는 배선간의 용량을 저감하는 것이 기득(期得)된다.

The aluminium wiring of the aspect ratio in which this damascene process is high is formed into the etching. Also the need to import the narrow gap between wiring the inter-layer film does not have and it is possible to l argely reduce the process number. As the wiring aspec t rate this process is high as and, the wiring total coun t increases it contributes to the reduction of the total cost. Moreover, it becomes with vested that the low p ermittivity of the inter-layer insulating film reduces cap acity between wiring.

그러나, 유전율비가 작은 재료로 이루어진 막은, 종래의 디바이스에 사용되는 실리콘 산화막과는 크게 다르고, 그 프로세스 기술은 아직 개발되지 않았다. 따라서, 그 실용화가 요구되고 있다.

But the film consisting of the material in which the dielectric constant ratio is small was different from the silicon oxide film used for the conventional device and t he processing technology was not developed. Therefor e, the put to practical use is requested.

또한, 최근에 이르러, 유전율비가 2.0 이하가 기득될 수 있는 재료로서, 크세로겔(xerogel)을 반도체 장치에 응용하는 것이 주목되고 있다.

Moreover, recently, it tells and the dielectric constant ratio is the material having with 2.0 less than vested n umber and it is watched to apply the xerogel to the se miconductor device.

본 기술에 관련하는 것으로서, 특개 평8-70005호 공보에는, 도 9에 보여진 바와 같이, 금속 리드선(94)의 신뢰성을 높이는 방법으로서, 저유전율 재료(96) 중에 열확산용 더미 리드선(93)을 설치하는 구조가 개시되어 있다. 이 구조는, 기판(92)상에 알루미늄 합금 등으로 이루어진 금속 리드선(94)과, 최소한 금속 리드선(94) 사이에 공극, 실리카-에어로겔, 유기 SOG, 플루오로 산화 실리콘 등으로 이루어진 저유전율 재료(96)와, 금속 리드선(94) 및 저유전율 재료(96)상에 데포지트(deposite)된 AlN, Si3N4 와 AlN과의 적층체 등으로 이루어진 전열성 절연층(97)과, 금속 리드선(94)에 근접한 알루미늄 합금 등으로 이루어진 더미(dummy) 리드선(93)을 가진다.

It relates to this technology. As shown in it is seen in JP8-70005 A in fig. 9 it is the method for heightening t he reliability of the metal lead line (94) and the structu re of setting up the dummy read line (93) for the therm al diffusion among the low dielectric constant material (96) is disclosed. This structure has the metal lead line (94), made of the aluminum alloy etc. in the substrate (92) and the low dielectric constant material (96), mad e of the oxidation silicon etc. among at least metal lea d line (94) of the air gap, the silica - aerogel, the orga nic spin on glass, *** and metal lead line (94) and the dummy (dummy) lead line (93) consisting of the propert y of transferring heat insulating layer (97), and the alu minum alloy etc. near to the metal lead line (94) consis ting of the AlN, and the laminate between the Si 3 N 4 and the AlN etc. The AlN becomes on the low dielectric constant material (96) with the deposit (deposite).

이 구조는, 금속 리드선(94)으로부터의 열은, 열을 확산할 수 있는 더미 리드선(93) 및 저유전율 재료보다 열전도도가 20% 높고, 바람직하게는 Si3N4 보다 20% 높은 열전도도를 가진 AlN 등의 절연 재료로 이루어진 전열성 절연층(97)에 이동될 수

Heat from the metal lead line (94) the thermal conductivity is higher than the dummy read line (93) an d the low dielectric constant material diffusing heat wit h 20% and it can be moved in the property of transferri

GF Exhibit 1124 - 2153/2704

있다. 이러한 구조로 하는 것에 의하여, 선간(또는 리드선간)의 배선 용량을 감소시키고, 또한, 저유전율 재료의 열전도도의 저하에 따라 높은 어스펙트비의 금속 리드선을 사용하는 경우에 문제가 되는, 줄(joule) 열효과에 의한 금속 리드선 파손 등을 방지하여 신뢰성이 높은 금속 리드선을 가지는 반도체 장치를 얻도록 하는 것이다.

ng heat insulating layer (97) consisting of the insulating material including the AlN etc. having the thermal conductivity higher than the Si 3 N 4 with 20%. It is according to be done by such structure and the wiring capacitance of the interline (between or, the lead line) is reduced and the semiconductor device it prevents the metal lead line damage by the line (joule) thermal effect etc. becomes a problem in case of using the metal lead line of the high aspect rate according to moreover, the degradation of the thermal conductivity of the low dielectric constant material and for having the metal lead line in which the reliability is high is obtained.

위에 기술한 다마신(damascene)법은, 배선 패턴을 미리 층간 절연막에 형성해 놓고, 거기에 금속을 매입하고, CMP 법에 의해 금속을 연마하고, 배선을 형성하는 것이다. 종래의 층간 절연막에서는 산화 실리콘막 등의 무기재료를 사용할 수 있었지만 미세화에 따른 용량 증대를 억제하는 목적으로 저율전율의 재료가 채용되고 있다. 저유전율의 재료의 대부분은 유기막이고, 유기막의 막질은 종래의 산화 실리콘막 등의 무기막에 비하여 그 단단함은 1/10~1/100 이므로, 예를 들면 다마신 프로세스에 필요한 단단함이 불충분하다.

The damascene method described in the upper part forms the wiring pattern on inter-layer insulating film in advance and it purchases the metal in addition and it polishes the metal with the CMP law and it forms wiring. In the conventional inter-layer insulating film, the inorganic material including the silicon dioxide film etc. could be used but the material of the low rate trepidation is employed as the purpose of suppressing the capacity enhancement according to the miniaturization. The majority of the material of the low permittivity is the organic layer and it continues with 1/10~1/100 that the thin film of the organic layer is solid in comparison with the inorganic film including the conventional silicon dioxide film etc. Therefore it is insufficient in for example, the damascene process that it is solid.

유전율비가 작은 물질, 특히 유전율비가 3 이하인 저유전율막 대부분은 유기막이다. 유기막은, 종래의 층간 절연막에 사용될 수 있는 실리콘 산화막에 비하여 부드러운 것이 특징이다. 예를 들면 영(young) 율로 비교하면, 실리콘 산화물이 5~10#215 #1010 에 대하여 유기막을 구성하는 수지는 0.3~0.8#215# 1010 으로 작다.

The low-dielectric-layer majority in which the material, in which the dielectric constant ratio is small especially, the dielectric constant ratio is 3 or less is the organic layer. As to the organic layer, what is soft in comparison with the silicon oxide film which can be used for the conventional inter-layer insulating film is characterized. For example, if it compares to the zero (young) rate , the resin in which the silicon oxide configures the organic layer about 5~10× 10 10 is small to 0.3~0.8× 10 10 .

따라서, 다마신법으로 배선을 형성한 경우, 유기막에 많은 스크래치(scratch) 가 발생하게 된다. 스크래치는 수득율(product yield) 저하의 원인이 된다. 그 때문에, 일반적으로는 실리콘 산화막 또는 질화막을 유기막 상에 형성하지만, 이러한 막은 유전율이 유기막에 비하여 높고, 배선간의 용량이 증대해 버리는 문제가 있다.

Therefore, in case wiring is formed into the damascene method many scratch is generated in the organic layer. Scratch is caused by the yield rate (product yield) degradation. Consequently, generally, such film the silicon oxide film or the nitride film is formed on the organic layer has the problem that the dielectric constant is high in comparison with the organic layer and capacity between wiring increases.

그러므로, 다마신 프로세스시에, 산화 실리콘막이나 질화 실리콘막을 병용하는 아이디어가 제안되고 있다. 그러나, 그러한 막은 유전율이 높고, 유기막에 의한 저유전율화의 효과를 반감시켜 버리는 문제가 있다.

Therefore, the idea using the silicon dioxide film or the silicon nitride film jointly is proposed in the damascene process. But that film has the problem that the dielectric constant is high and the effect of the low permittivity by the organic layer is reduced to half.

또, 유기막은 종래의 반도체 디바이스에 사용되었던 층간 절연막(실리콘 산화막)에 비하여 열전도율이 1/10 정도로 매우 작고, 소자의 열확산에 중대한 영향을 미친다. 즉, 디바이스의 축소화에 따라 단위 면적 정도의 열발생량은 저하하지만, 방열을 위한 경로의 열전도율이 떨어질 수 있다. 따라서, 방열 경로를 고려하는 디바이스 구조가 요구된다.

And the thermal conductivity is very little in comparison with the inter-layer insulating film (silicon oxide film) in which the organic layer was used for the conventional semiconductor device to about 1/10 and it affects. It is important in the thermal diffusion of the device. That is, according to the demagnification of the device, the heat production of about unit area is degraded. However the thermal conductivity of the route for the heat radiation can drop. Therefore, the device structure of considering the thermal via is required.

GF Exhibit 1124 - 2154/2704

또한, 크세로겔은 실리카겔(silica gel)이라는 명칭으로 건조제 등에 사용되는 등, 일반적으로 널리 알려진 재료이지만, 반도체 장치에의 응용에는 다양한 신뢰성에 대한 요구가 있고, 현재로서는 반도체 장치에 적용하는 것은 곤란하다. 즉, 크세로겔은 그 체적의 50~90% 가 기포이고, 기계적 강도, 열전도성, 내열성, 내 습성, 층간 밀착성 등에 문제가 있다.

Moreover, it is used as the name for the drying agent etc. The xerogel is the silica gel it is the material which generally is widely known. However the name has the demand about the reliability which is various in the application of the semiconductor device and it is difficult to now apply to the semiconductor device. That is, 50~90% of the volume as to the xerogel, is bubble and the problem is in the mechanical strength, thermal conductance, heat resistance, wet-proof property, the clinging etc.

따라서, 이러한 문제를 해결하면서 저유전율의 크세로겔을 응용하는 디바이스 구조가 요구된다.

Therefore, the device structure of applying the xerogel of the low permittivity while it resolves such problem is required.

발명의 내용

Summary of Invention

발명의 효과

Effects of the Invention

이상 설명한 바와 같이, 본 발명의 반도체 장치는 층간 절연막을 유전율비가 3.0 이하인 유전체막을 사용하기 때문에, 배선간 용량의 증대가 대폭 억제되는 미세한 반도체 장치이다.

As described above, the semiconductor device of the invention is the minute semiconductor device in which increase in capacity between wiring the inter-layer insulating film the dielectric film in which the dielectric constant ratio is 3.0 or less is used are drastically suppressed.

또, 방열을 위한 더미 배선층을 배선 패턴에 대하여, 최소한 3배 피치 이상의 배선 간격 부분에 설치하는 것에 의하여, 열전도율이 작은 저유전율막을 사용하는 것에 의한 열확산 효율의 저하를 효과적으로 방지할 수도 있다.

And it is according to set up the dummy wiring layer for the heat radiation in the wiring space part more than at least treble pitch about the wiring pattern and the degradation of the thermal diffusion efficiency which is according to use the low-dielectric-layer in which the thermal conductivity is little can be effectively prevented.

또, 더미 접속 플러그(콘택트 플러그 및 비아 콘택트 플러그)를 더미 배선층의 아래에 설치하는 경우에는 열전도율이 작은 저유전율막을 사용하는 것에 의한 열확산 효율의 저하를 보다 효과적으로 방지할 수 있다.

And dummy adapter plug (the contact plug and via contact plug) the degradation of the thermal diffusion efficiency which is according to use the low-dielectric-layer in which the thermal conductivity is little in case of beneath setting up of the dummy wiring layer can be more effectively prevented.

또한, 본 발명에 의하면, 배선층의 주위(배선층의 좌우), 바람직하게는 배선 간격이 표준 피치의 3배 이하인 개소에는 유전율비가 매우 작은 크세로겔을 함유하는 막을 사용하고, 또한, 배선간의 콘택트홀의 주위(배선층의 상하)에는 저유전율막을 사용하는 것에 의하여 크세로겔막의 결점을 보충하면서, 배선용량을 대폭 축소하는 것에 의하여 신뢰성이 높은 미세 구조를 가지는 반도체 장치를 수득률 좋게 제조할 수 있다.

Moreover, in according to the invention, surrounding (right and left of the wiring layer) of the wiring layer, and the place in which preferably the wiring space is the treble or less of the standard pitch, the film in which the dielectric constant ratio contains very small xerogel is used and while it is according to use the low-dielectric-layer in moreover, surrounding (top and bottom of the wiring layer) of the contact hole between wiring and the defect of the xerogel layer is supplemented it is according to drastically reduce the wiring capacitance and it is good with yield the semiconductor device for having the fine structure where the reliability is high can be manufactured.

또, 크세로겔을 함유하는 막의 상하에는 실란 커플링제로 이루어진 층을 설치하는 것에 의하여, 층간 밀착성에 뛰어난 반도체 장치를 제조할 수 있다.

And in top and bottom of the film containing the xerogel, it is according to set up the layer consisting of the silane coupling agent and the excel semiconductor device can be manufactured at a rate per the clinging.

기술적 과제

Technical Task

GF Exhibit 1124 - 2155/2704

그러므로, 본 발명은 저유전율막을 층간 절연막으로서 사용하는 반도체 장치 및 그 제조 방법을 제공하는 것을 목적으로 한다.

Therefore, the object of the invention is to provide semiconductor device and method for manufacturing same for using the low-dielectric-layer as the inter-layer insulating film.

본 발명자는 상기 문제점에 비추어, 저유전율막으로 유기막, 또는 유기막 및 크세로겔을 함유하는 막을 층간 절연막으로서 사용하는 반도체 장치를 다마신법으로 형성하는 방법 및 반도체 장치 및 이 반도체 장치의 제조 방법을 고안한다.

The inventor lights to the problem and the method, for forming the semiconductor device for using the film containing the organic layer or the organic layer and xerogel as the low-dielectric-layer as the inter-layer insulating film into the damascene method the semiconductor device and manufacturing method of this semiconductor device are devised.

즉, 본 발명은 반도체 기판과, 이 반도체 기판 상에 형성된 절연막과, 유전율비가 3.0 이하인 유전체막과, 이 유전체막에 형성되고 절연막에 접하는 배선층을 가지는 반도체 장치를 제공하며, 상기 배선층의 상면이 상기 유전체막의 상면보다도 높다.

That is, the invention provides the semiconductor device for having the semiconductor substrate, and the insulating layer, formed on this semiconductor substrate and the dielectric film, in which the dielectric constant ratio is 3.0 or less and the wiring layer which is formed in this dielectric film and contacts to the insulating layer. And the upper side of the wiring layer is higher than the upper side of the dielectric film.

또, 본 발명은, 반도체 기판상에 절연막을 형성하는 공정과, 이 절연막의 위에 유전율비가 3.0 이하인 유전체막을 형성하는 공정과, 이 유전체막의 위에 무기막을 형성하는 공정과, 상기 유전체막에 배선층을 형성하기 위한 패턴을 형성하는 공정과, 상기 배선층을 전체면에 형성하는 공정과, 상기 배선층을 연마하는 공정과, 상기 무기막을 제거하는 공정을 가지는 반도체 장치의 제조 방법이다.

And the invention relates to the method for manufacturing semiconductor device having the process, of forming the insulating layer on the semiconductor substrate and the process, of forming the dielectric film in which the dielectric constant ratio is 3.0 or less on the upper part of this insulating layer and the process, of forming the inorganic film on the upper part of this dielectric film and the process, of forming the pattern for forming the wiring layer on the dielectric film and the process, of forming the wiring layer on the total surface and the process, of polishing the wiring layer and the process of removing the inorganic film.

상기 본 발명의 반도체 장치 및 그 제조 방법에 있어서, 상기 유전체막은, 사이클릭 플루오로 레진, 폴리테트라플루오로에틸렌, 플루오로화 에틸렌 프로필렌, 테트라플루오로에틸렌 공중합체, 퍼플루오로알콕시에틸렌, 폴리플루오로비닐리덴, 폴리트리플루오로클로로에틸렌, 플루오로아릴 에테르 레진, 폴리플루오로이미드, 벤조시클로부텐(BCB) 폴리머, 폴리이미드, 아몰퍼스 카본, 모노메틸트리하이드록시실란 (유기 SOG) 축합체, 하기의 식(1)로 표현되는 반복하는 단위 구조를 가지는 폴리머,

The polymer which the dielectric film has the concatemer of repeating of being expressed as the resin, poly tetra fluoro ethylene, fluoro ethylene propylene, tetrafluoroethylene copolymer, perfluoro alkoxy ethylene, polyfluorovinylidene, polytrifluorochloroethylene, fluoroaryl ether resin, poly fluoro imide, benzocyclobutene (BCB) polymer, polyimide, amorphous carbon film, monomethyl trihydroxy silane (organic spin on glass) condensation product, following formula (1) as to semiconductor device and manufacturing method thereof of the present invention to the cyclic ***.

(1)

(1)

(상기 m, n은 자연수를 나타낸다.)

(the m , and the n show the natural number)

하기의 식(2)로 표현되는 반복하는 단위 구조를 가지는 폴리머,

The polymer having the concatemer of repeating of being expressed as the following formula (2).

(2)

(2)

(상기 x, y, z은 각각 자연수를 나타낸다.)

(The x, the y , and the z show the natural number.)

하기의 식(3)으로 표현되는 반복하는 단위 구조를 가지는 폴리머,

The polymer having the concatemer of repeating of being expressed as the following formula (3).

(3)

(3)

GF Exhibit 1124 - 2156/2704

(상기 R은 알킬렌 또는 페닐렌 군을 나타낸다.)

(r shows the alkylene or the phenylene group)

하기의 식(4)로 표현되는 반복하는 단위 구조를 가지는 폴리머,

The polymer having the concatemer of repeating of being expressed as the following formula (4).

(4)

(4)

(상기 R#39#는 알킬렌 또는 페닐렌 군을 나타낸다.)

(the R' shows the alkylene or the phenylene group)

로 이루어지는 군으로부터 선택되는 최소한 하나의 재료로 이루어진다.

It comprises the material of at least one selected from the group.

그 외, 상기 저유전율막의 재료로서, 상품명, 아몰퍼스 테플론(Amorphous Teflon), CYTPO(Phonetic), FLARE 등의 상품명으로 시판되는 것을 사용할 수 있다.

As the besides, and the material of the low-dielectric-layer, it can use coming into the market to the product name of the product name, the amorphous Teflon, CYT PO (Phonetic), FLARE etc.

상기 본 발명의 반도체 장치는 바람직하게는 배선 패턴에 대하여, 최소한 3배 피치 이상의 배선 간격의 부분에, 보다 바람직하게는 모든 배선 간격이 1 ㎛ 이 되도록 더미 배선을 가진다.

In the semiconductor device of the invention, preferably, the part of the wiring space more than at le ast treble pitch about the wiring pattern, more prefera bly, it has the dummy line so that all wiring spaces are 1 ㎛ a.

상기 본 발명의 반도체 장치는, 바람직하게는 상기 유전체막 상에 크세로겔을 함유하는 층간 절연막을 가지고, 보다 바람직하게는 상기 크세로겔을 함유하는 층간 절연막 상에 실란 커플링(silane coupling)제를 함유하는 층을 가진다.

Preferably the semiconductor device of the invention has the inter-layer insulating film containing the xerogel on the dielectric film and it has the layer containing the silane coupling agent on the inter-layer insulating film more preferably, containing the xerogel.

상기 본 발명의 반도체 장치는, 바람직하게는 상기 더미 배선의 아래의 절연막중에서 또, 하층 도전층과 접하지 않는 더미 콘택트홀을 더 가진다.

Preferably the semiconductor device of the invention more has the dummy contact hole which does not cont act with and, the lower conductive layer among the foll owing insulating layer of the dummy line.

상기 하층 도전층으로서는 반도체 기판에 설치된 불순물 확산 영역 또는 하층 배선층을 추천할 수 있다.

The impurity diffusion region or the lower wiring layer installed at the semiconductor substrate can be recom mended as the lower conductive layer.

상기 본 발명의 반도체 장치의 제조 방법에 있어서, 상기 무기막은 바람직하게는 산화 실리콘막, 플루오로화 실리콘막, 질화 실리콘막, 질화 산화 실리콘막, 실라놀(silanol) 축합체(무기 SOG)막, 포스포러스-도프드(phosphorus-doped) 산화 실리콘막, 보론-도프드(boron-doped) 산화 실리콘막 및 보론-포스포러스-도프드 산화 실리콘막으로 이루어진 군으로부터 선택되는 최소한 하나의 재료로 이루어진다.

The inorganic film as to the manufacturing method of the semiconductor device of the invention includes pref erably, the silicon dioxide film, the fluoro silicon film, th e silicon nitride film, the silicon oxynitride film, the silan ol (silanol) condensation product (inorganic spin on glas s) film, the phosphorous - doped (phosphorus-doped) s ilicon dioxide film, the boron - doped (boron-doped) sili con dioxide film, and the material of at least one select ed from the group consisting of the boron - phosphorou s - doped silicon dioxide film.

상기 본 발명의 반도체 장치의 제조 방법에 있어서, 바람직하게는, 배선 패턴에 대하여, 최소한 3배 피치 이상의 배선 간격의 부분에, 보다 바람직하게는 모든 배선 간격이 1 ㎛ 이하로 되도록 더미 배선을 형성하는 공정을 가진다.

As to the manufacturing method of the semiconductor device of the invention, preferably, more preferably, it has the impartiality where all wiring spaces form the du mmy line about the wiring pattern upon the part of the wiring space more than at least treble pitch.

상기 더미 배선을 형성하는 공정은, 바람직하게는 배선 패턴 및, 배선 패턴에 대하여 최소한 3배 피치 이상의 배선 간격의 부분에, 보다 바람직하게는 모든 배선 간격이 1 ㎛ 이하로 되도록 더미 배선 패턴을 동시에 형성하는 공정이다.

In preferably, the part of the wiring space more than at least treble pitch about the wiring pattern, and wirin g pattern, the process of forming the dummy line more preferably is the process where all wiring spaces simult aneously form the dummy line pattern as as possible.

상기 배선층을 연마하는 공정은, CMP법에 의해 연마하는 공정

The process of polishing the wiring layer is the be

GF Exhibit 1124 - 2157/2704

인 것이 바람직하다.

desirable the process of polishing with the CMP law.

상기한 바와 같이, 본 발명은 유전율비가 낮은 유기막 또는 크세로겔을 사용한 반도체 장치를 다마신법으로 형성하는 방법 및 반도체 장치 구조에 관한 것이다.

As described above, the invention relates to a method of forming into the damascene method the organic layer in which the dielectric constant rain is low or the semiconductor device using the xerogel and the semiconductor device structure.

다마신법은 배선 패턴을 미리 층간 절연막에 형성해 놓고, 거기에 금속을 매입하고, CMP(화학적 기계적 연마)법에 의해 금속을 연마하고, 배선층을 형성하는 것이다.

The damascene method forms the wiring pattern on the inter-layer insulating film in advance and the metal is purchased in addition and the metal is polished with the CMP (chemical mechanical polishing) method and the wiring layer is formed.

종래의 층간 절연막에는 산화 실리콘막 등의 단단한 재료를 사용하였다. 그러나, 반도체 장치의 미세화에 따른 용량 증대를 억제하는 목적으로 유기막이 저유전율 재료로서 채용되고 있다.

In the conventional inter-layer insulating film, the hard material including the silicon dioxide film etc. was used. But the organic layer is employed as the purpose of suppressing the capacity enhancement according to the miniaturization of the semiconductor device as the low dielectric constant material.

그러나 유기막 재료는 산화 실리콘막 등의 무기막 등과 크게 다르고, 예를 들면, 다마신 프로세스에 필요한 단단함이 불충분하다. 그 값은 1/10~1/100 이다. 그러므로 본 발명에서는 유기막 상에 무기막을 형성한 후에 배선층을 유기막중에 다마신법에 의해 형성하고, 무기막을 제거하는 방법을 고안하였다.

But the organic film material is different from the silicon dioxide film, including, the inorganic film etc. and it is insufficient in for example, the damascene process that it is solid. The value is 1/10~1/100. Therefore, in the present invention, the inorganic film the wiring layer was formed on the organic layer on the formation among the organic layer with the damascene method and the method for removing the inorganic film was devised.

한편, 유기막은 열전도율이 낮기 때문에, 디바이스 동작시에 발생하는 방열이 문제가 되었다. 그래서 본 발명에서는 배선 형성 프로세스에 있어서, 방열 경로, 즉, 더미 배선층을 유기막중에 다마신법에 의해 형성하는 반도체 장치의 제조 방법을 고안하였다.

In the meantime, the thermal conductivity as to the organic layer, was low. Therefore the generated heat radiation became a problem in the device operation. So, in the present invention, as to the wiring formation process, the method for manufacturing semiconductor device for forming the thermal via, in other words, the dummy wiring layer among the organic layer with the damascene method was designed.

또, 본 발명에서는 하층 도전층과 상층 배선을 접속하는 콘택트홀(비아홀) 형성시에, 더미 배선의 아래에 하층 도전층과 접속하지 않는 더미 콘택트홀을 형성하는 것에 의하여 방열 효과를 더 높이는 구조를 제안한다.

And in the present invention, it is according to form the dummy contact hole which beneath does not connect with the lower conductive layer of the dummy line in the contact hole (via hole) formation connecting the lower conductive layer and upper level wiring line and the structure of more enhancing the thermal performance is suggested.

또한, 본 발명에서는 저유전율막으로서 주목되고 있는 크세로겔막의 배선 형성 프로세스로의 적용을 고안한다. 크세로겔막은 저유전율막이지만, 유기적 강도, 열전도성, 밀착성, 내수성 등이 종래의 층간 절연막에 비하여 떨어진다. 그래서 본 발명에서는 크세로겔의 적용 개소(箇所)를 가능한 만큼 줄이고, 저유전율막과 무기 절연막을 조합하는 것에 의해 저유전율막이 이루는 효과를 손상하지 않고, 배선간의 용량을 저감하는 구조를 제안하였다. 즉, 크세로겔을 가장 배선 용량이 크게 되는 부분에 사용하고, 그 이외의 장소에는 유기막 무기 저유전율막을 사용하는 것이다.

Moreover, in the present invention, the application to the wiring formation process of the xerogel layer watched as the low-dielectric-layer is designed. The xerogel layer is the low-dielectric-layer. However the organic intensity, thermal conductance, adhesion, the water resistance etc falls down in comparison with the conventional inter-layer insulating film. So, in the present invention, the application place of the xerogel was decreased as much as it was possible and by assembling the low-dielectric-layer and inorganic insulation film the effect that the low-dielectric-layer was comprised was not injured and the structure of reducing capacity between wiring was suggested. That is, the xerogel is used in the part in which the wiring capacitance is most large and it is in the place of the except to use the organic layer in organic low dielectric constant film.

GF Exhibit 1124 - 2158/2704

더욱이, 본 발명은 크세로겔막이 층간 밀착성이 떨어지는 것이 비추어, 크세로겔막의 아래 및/또는 위에 실란 커플링제로 형성되는 막을 설치하는 것도 제안한다.

Furthermore, it lights that the clinging of the xerogel layer falls as to the invention, and it suggests to set up the film formed in the lower part of the xerogel layer and/or the upper part into the silane coupling agent.

본 발명에 의하면, 층간 절연막을 유전율비가 3.0 이하인 유전체막(이하 저유전율막이라고 함)으로 하기 때문에, 배선간 용량의 증대가 대폭으로 억제된 미세한 반도체 장치를 제조할 수 있다.

According to the invention, the minute semiconductor device in which the increase in the dielectric film (hereinafter, the low-dielectric-layer box), in which the dielectric constant ratio is the inter-layer insulating film 3.0 or less therefore, capacity between wiring is largely suppressed can be manufactured.

또, 방열을 위한 더미 배선층을, 배선 패턴에 대하여 최소한 3배 피치 이상의 배선 간격의 부분에 설치하는 경우에는, 열전도율이 작은 저유전율막을 사용하는 것에 의한 열확산 효율의 저하를 효과적으로 방지할 수 있다.

And in case the dummy wiring layer for the heat radiation is set up in the part of the wiring space more than at least treble pitch about the wiring pattern the degradation of the thermal diffusion efficiency which is according to use the low-dielectric-layer in which the thermal conductivity is little can be effectively prevented.

상기 더미 배선층의 아래에 더미 콘택트홀을 설치하는 경우에는, 더욱더 열확산 효율을 높일 수 있다.

In case the dummy contact hole is beneath set up of the dummy wiring layer the thermal diffusion efficiency can be more and more enhanced.

또한, 본 발명에 의하면, 배선층의 주위(배선층의 좌우), 바람직하게는, 배선 간격이 표준 피치의 3배 이하인 개소에는 유전율비가 매우 작은 크세로겔을 함유하는 막을 사용하고, 또한, 배선간의 콘택트홀의 주위(배선층의 상하)에는 저유전율막을 사용하는 것에 의하여 크세로겔막의 결점을 보충하면서, 배선 용량을 대폭 축소하는 것에 의하여 신뢰성이 높은 미세 구조를 가지는 반도체 장치를 수득률 좋게 제조할 수 있다.

Moreover, in according to the invention, surrounding (right and left of the wiring layer) of the wiring layer, and the place in which preferably the wiring space is the treble or less of the standard pitch, the film in which the dielectric constant ratio contains very small xerogel is used and while it is according to use the low-dielectric-layer in moreover, surrounding (top and bottom of the wiring layer) of the contact hole between wiring and the defect of the xerogel layer is supplemented it is according to drastically reduce the wiring capacitance and it is good with yield the semiconductor device for having the fine structure where the reliability is high can be manufactured.

또, 크세로겔을 함유하는 막의 상하에는 실린 커플링제로 이루어진 층을 설치하는 것에 의하여, 층간 밀착성에 뛰어난 반도체 장치를 제조할 수 있다.

And in top and bottom of the film containing the xerogel, it is according to set up the layer consisting of the loaded coupling agent and the excel semiconductor device can be manufactured at a rate per the clinging.

발명의 구성 및 작용

Structure & Operation of the Invention

이하, 본 발명을 상세히 설명한다.

Hereinafter, the invention is particularly illustrated.

본 발명의 반도체 장치는 반도체 기판으로서 트랜지스터, 배선 패턴 등이 형성된 n형 또는 p형 불순물이 주입된 실리콘 반도체 기판을 사용할 수 있다.

The semiconductor device of the invention can use the n-type in which the transistor, the wiring pattern etc. are formed or the silicon semiconductor substrate in which the p-type impurity is injected as the semiconductor substrate.

본 발명에 있어서, 상기 반도체 기판 상에는 절연막이 설치된다. 이 절연막으로서는 예를 들면 산화 실리콘막을 사용할 수 있다. 상기 절연막은 예를 들면 열산화에 의한 방법, CVD(Chemical Vapor Deposition)법, 스퍼터링법 등에 의해 형성할 수 있고, 두께는 300~700㎚ 정도가 바람직하다.

In the present invention, the insulating layer is installed on the semiconductor substrate. For example, the silicon dioxide film can be used as this insulating layer. The insulating layer is for example, the method by the thermal oxidation, and the thickness it can form with the CVD (Chemical Vapor Deposition) method, the sputtering method etc are about 300~700㎚ is the be desirable.

이 절연막의 위에는 저유전율막이 형성된다. 이 저유전율막은 유전율비가 3.0 이하인 것이 바람직하다. 상기 저유전율막으

The upper part of this insulating layer may be provided with the low-dielectric-layer. The dielectric constant ra

GF Exhibit 1124 - 2159/2704

로서는 상기 예시한 유전율비가 3.0 이하인 유전체막, 크세로겔을 함유하는 막 등을 사용할 수 있다.

tio this low-dielectric-layer is the be desirable 3.0 or less. The dielectric film, in which the above-mentioned exemplified dielectric constant ratio is 3.0 or less the film etc. can be used as the low-dielectric-layer containing the xerogel.

상기 유전체막은 예를 들면, 고분자의 전구체(precursor)를 스핀코터(spin coater)로 성막하고, 300~500℃로 소성(baking)하는 것에 의해 형성할 수 있다. 또, 아몰퍼스 카본 등의 재료의 경우는, 아세틸렌, 필요에 대응하여 플루오로 카본 가스를 사용하여 플라즈마(plasma) CVD 장치를 사용하여 형성할 수 있다. 상기 유기막의 두께는 통상 300~700㎚ 가 바람직하다. 또, 상기 크세로겔을 함유하는 막은 예를 들면 스핀코터법으로 제조할 수 있다.

The dielectric film deposits for example, the precursor of the polymer to the spin coater and it can form by the plasticity (baking) being done by 300~500℃. And in case of the material including the amorphous carbon film etc, it corresponds to the acetylene, and the need and it can form into *** using the carbon gas using the plasma performing apparatus. Generally 300~700㎚ the thickness of the organic layer is the be desirable. And the film containing the xerogel can manufacture with for example, the spin coating method.

본 발명에 있어서는, 상기 유기막 상에, 크세로겔을 함유하는 막을 형성하는 것이 바람직하다. 크세로겔은 건조한 상태에 있는 겔(gel)이고, 예를 들면, 실리카겔을 예시할 수 있다. 보다 구체적으로는 나노포러스(nanoporous)사가 개발한 제품명 Nanoporous Silica 가 있으며 포로스 실리카의 한 종류이다. 본 발명은 특히 이것에 한정되는 것은 아니고, 방향족 등의 비교적 고분자의 알킬(alkyl)기를 가지는 실라놀(silanol) 수지를 도포하고 그것을 겔화시키고 실란 커플링제 또는 수소화 처리를 사용하여 소수 처리 등을 행하여 형성한 것이라면, 어떤 크세로겔도 좋다. 크세로겔은 유전율비가 2.0 이하로 되는 것을 기대할 수 있는 재료이고, 배선간의 용량을 대폭 저감할 수 있다.

It is in the invention and it is the be desirable to form the film containing the xerogel on the organic layer. The xerogel is the gel which is in the dry state and for example, the silica gel can be exemplified. More specifically, it has the product name Nanoporous Silica which the nanoporous corp. develops and it is one kind of the porous silica. The invention is not restricted to especially, this and the kinds raised with the alkyl (alkyl) of the relative polymer including the aromatic family etc. coats with the silanol resin and that is gelled and the hydrophobic process etc. are performed using the silane coupling agent or the hydrotreating and it forms. If it is the case any kind of xerogel is good. The xerogel is the material in which the dielectric constant ratio can expect becoming less than 2.0 and capacity between wiring can be fully.

본 발명에 있어서, 크세로겔을 함유하는 막을 상기 저유전체막 상, 바람직하게는, 이 저유전체막 상에 있고 최소한 배선 간격이 3배 피치 이하인 영역에 형성한다. 그리고, 바람직하게는 크세로겔을 함유하는 막을 배선층의 좌우에 매입하도록 형성하는 것이 바람직하다.

In the present invention, it has on this low-k dielectric layer and preferably the film containing the xerogel is formed the low-k dielectric layer phase on the domain in which at least wiring space is the treble pitch or less. And preferably, it is the be desirable to form in order to purchase the film containing the xerogel in right and left of the wiring layer.

또, 특히, 복수의 배선층을 가지는 반도체 장치에 있어서, 상기 유전율비가 3.0 이하인 유전체막중에, 배선간을 접속하기 위한 콘택트홀을 가지는 구조로 하는 것이 바람직하다.

And as to the semiconductor device for having especially, the multiple wiring layers, it is the be desirable to be done by the structure of having the contact hole for connecting the wiring liver among dielectric film in which the dielectric constant ratio is 3.0 or less.

반도체 장치를 이와 같은 구조로 하는 것에 의하여, 크세로겔을 함유하는 막의 적용 개소를 가능한 만큼 줄이고, 저유전율의 유기막과 크세로겔을 함유하는 막을 조합하는 것에 의하여 크세로겔막의 상기 결점을 보충하면서, 또한, 저유전율막의 효과를 손상하지 않고 배선간의 용량을 저감하는 것이 가능하게 된다.

It is according to have the semiconductor device as this kind of structure and the application place of the film containing the xerogel is decreased as much as it is possible and while it is according to assemble the film containing the organic layer and xerogel of the low permittivity and the defect of the xerogel layer is supplemented the effect is possible not to injure moreover, the effect of the low-dielectric-layer and reduce capacity between wiring.

또, 본 발명에 있어서는 크세로겔을 함유하는 막은 층간 밀착성이 부족하다. 따라서, 층간 밀착성을 높이기 위하여, 상기 크세로겔을 함유하는 막의 위에, 실란 커플링제를 함유하는 막을 형성하는 것도 바람직하다. 이 실란 커플링제는 예를 들면, 일반

And as to the film, which is in the invention and contains the xerogel the clinging is insufficient. Therefore, in order that the clinging is enhanced it is the be desirable to form the film containing the silane coupling a

GF Exhibit 1124 - 2160/2704

식 RSiX3 또는 RR#39#SiX2 (R 및 R#39#는 알킬기, 알콕시기 등을 표시하고, X는 할로겐(halogen) 원자를 표시한다.)로 표시되는 규소화합물을 예시할 수 있다. 이 규소화합물은 분자 중에 수소성 부분(R이나 R#39#)과 극성 부분(X)을 가지고, 수소성의 유기막과 극성을 가지는 크세로겔을 함유하는 무기막의 층간 밀착성을 높이고, 박리를 방지하는 역할을 완수한다.

gent on the upper part of the film containing the xerogel. The silicide in which this silane coupling agent is indicated as for example, the general formula RSiX 3 or RR' SiX 2 (R and R' indicate the alkyl group, the alkoxy group etc. and X indicates the halogen atom.) can be exemplified. This silicide has the hydrogen star part (R or the R') and polarity part (X) during the molecule and the clinging of the inorganic film containing the xerogel having the organic layer and polarity of the hydrogen star is enhanced and the part of preventing the exfoliation is accomplished.

상기 실린 커플링제는 예를 들면, 스핀코터법으로 도포하여 막을 제조할 수 잇다.

It continues with number in which the above-mentioned loaded coupling agent coats in for example, the spin coating method and which manufactures the film.

다음에, 상기 유전체막, 크세로겔을 함유하는 막 또는 실란 커플링제를 함유하는 막의 위에 무기막을 형성한다. 이 무기막으로서는 산화 실리콘막, 플루오로화 실리콘막, 산화 질화 실리콘막, 실라놀 축합물(무기SOG)막, 포스포러스-도프드 산화 실리콘막, 보론-도프드 산화 실리콘막, 보론-포스포러스-도프드 산화 실리콘막 등을 예시할 수 있다.

Next, the inorganic film is formed on the upper part of the film containing the dielectric film, and the xerogel or the film containing the silane coupling agent. The silicon dioxide film, fluoro silicon film, silicon OXY nitride thin film, silanol condensate (inorganic spin on glass) film, phosphorous - doped silicon dioxide film, boron - doped silicon dioxide film, the boron - phosphorous - doped silicon dioxide film etc can be exemplified as this inorganic film.

상기 무기막의 형성은 통상, 플라즈마 CVD법에 의하지만 환원(還元) 분위기(atmosphere)로 수행할 필요가 있다. 산화 분위기 하에서 CVD를 수행하면, 유기막이 산화되고 막의 박리 등의 현상을 발생시키기 때문에 바람직하지 않다. 예를 들면 산화 실리콘막의 경우, 플라즈마 CVD 장치를 사용하여 실란 가스 및 N2O 가스의 분위기 하에서 온도 300~500℃에서 성막할 수 있다.

The formation of the inorganic film trades and it is according to due to the plasma CVD method but it need to perform to the reducing atmosphere. If CVD is performed under the oxidizing atmosphere , because the organic layer is oxidized and the phenomenon including the exfoliation of the film etc. is generated it knows. For example, in case of the silicon dioxide film, it can deposit using the plasma CVD apparatus under an atmosphere of the silane gas and N 2 O gas in the temperature 300~500℃.

상기 무기막을 퇴적한 후, 레지스트막을 형성하여 배선을 패터닝하고, 포토 에칭(photoetching)에 의하여 최상막의 무기막, 실란 커플링제를 함유하는 막, 크세로겔을 함유하는 막 및 유기막을 예를 들면, 일반적인 마그네트론(magnetron) 방식의 에칭 장치를 사용하여 에칭을 행한다. 에칭은 예를 들면 산화 실리콘 등의 무기막의 경우는 에칭 가스로서 C2F6, CO, Ar, O2 가스를 사용하여 행할 수 있다.

In case of the inorganic film of the best film by the photo- etching (photoetching), the film containing the silane coupling agent, and the film and the organic layer containing the xerogel wiring is patterned the inorganic film the resist film is formed after doing the deposition, the etching is performed using the etching device of the general magnetron mode. The etching can perform in case of for example, the inorganic film including the oxidation silicon etc. as the etching gas using C 2 F 6 , CO, ar, O 2 gas.

또, 유기막의 경우에는 에칭 가스로서 예를 들면, CHF3 와 O2 가스를 사용하여 -10℃ 정도의 저온으로 수행할 수 있다. 이 경우, 상층의 무기막은 저유전율막을 에칭할 때의 마스크로도 사용된다. 또, 유기막을 에칭하는 조건에서는 레지스트막도 에칭된다.

And in case of the organic layer, it can perform as the etching gas using for example, the CHF 3 and O 2 gas to the low temperature of about -10℃. In this case, the inorganic film of the upper layer is used for the mask when etching the low-dielectric-layer. And in the condition etching the organic layer, resist film are etched.

다음에, 이른바 다마신법에 의해 배선층을 형성한다. 배선층 재료로서는 알루미늄, 동, 금, 텅스텐 및 이러한 합금으로 이루어진 군으로부터 선택되는 하나의 종류 이상을 예시할 수 있다. 배선 재료는 예를 들면, 스퍼터링법 또는 CVD법에 의해 형성할 수 있다.

Next, the wiring layer is formed with so-called, the damascene method. One kind or greater selected from the group consisting of the aluminum, copper, gold, tungsten and such alloy can be exemplified as the material for wiring layer. The wiring material can form with for example, the sputtering method or the chemical vapor deposition.

GF Exhibit 1124 - 2161/2704

이어서, CMP법에 의해 여분의 금속막을 연마한다. 연마에 사용할 수 있는 연마제로서는, 예를 들면, 알루미나(alumina), 이산화 망간, 실리카계 슬러리(slurry), 식 WxOy 로 표시되는 산화 텅스텐, 산화 세슘(cesium), 산화 지르코늄(sirconium), 산화 실리콘 등을 사용할 수 있고, 이러한 연마제에는 필요에 따라 과산화수소, 수산화 칼륨, 암모니아 등이 혼합된다.

Subsequently, the extra metal layer is polished with the CMP law. As the abrasive can use in the grinding, t he tungsten oxide, ceO (cesium), zirconium oxide (sirco nium), the oxidation silicon etc indicated as the alumin a, manganese dioxide, silica-based slurry, equation W x O y can be used for example and the hydrogen peroxid e, the potassium hydroxide, ammonia etc. are mixed in such abrasive as necessary.

완전하게 금속을 연마한 다음, 무기막에 새겨진 스크래치를 제거하기 위하여 CMP법에 의해 50㎚ 정도의 무기막을 연마한다.

Completely, after the metal is polished in order to remove the scratch carved in the inorganic film, the ino rganic film of about 50㎚ is polished with the CMP law.

다음에, 예를 들면, 플루오린(fluorine) 소원(素源)으로서 C2F6, CO 및 아르곤 가스를 사용하여 무기막, 실란 커플링제를 함유하는 막 및 크세로겔을 함유하는 막의 에칭을 행한다. 이 조건에서는 유기막은 거의 에칭되지 않는다.

Next, for example, the etching of the film containing the xerogel and the film containing the inorganic film, a nd the silane coupling agent as the fluorine wish using C 2 F 6 , and CO and argon gas is performed. In this co ndition, the organic layer is not etched at the nearly.

이와 같은 조작을 행하면, 크세로겔을 함유하는 막을 사용하지 않는 경우에는, 배선층의 상면은 상기 유전체막의 상면보다도 높게 되는 구조가 얻어진다. 배선층의 상면은 상기 유전체막의 상면보다도 높게 되는 것은, 최후에 무기막을 에칭에 의해 제거하기 위한 것이다.

If this kind of operation is performed , in case the film containing the xerogel is not used the structure where the upper side of the wiring layer is higher than the up per side of the dielectric film is obtained. The inorganic film is to be removed in the last with the etching that t he upper side of the wiring layer is higher than the upp er side of the dielectric film.

본 발명에 있어서는 또한 배선 패턴에 대하여 최소한 3배 피치 이상의 배선 간격의 부분에, 보다 바람직하게는 배선 간격이 1㎛ 이하로 되도록 더미 배선 패턴이 형성되는 것이 바람직하다.

It is in the invention and it more preferably is the be desirable about moreover, the wiring pattern in the par t of the wiring space more than at least treble pitch th at the dummy line pattern of wiring space are formed a s as possible.

반도체 장치의 배선 패턴에 대하여 3배 피치 이하의 간격의 부분이 있는 경우에는, 열전도도가 작은 유기막, 유기막 및 크세로겔을 함유하는 막을 사용하기 때문에, 동작시에 발생하는 열의 방출 경로가 없으므로, 미세 구조를 가지는 반도체 장치에 오동작 등을 발생시켜서 바람직하지 않다.

In case it has the part of the gap less than the treble pitch about the wiring pattern of the semiconductor de vice the organic layer in which the thermal conductivit y is small, and the film containing the organic layer and xerogel are used. Therefore there is no sent-out passa ge generated in the operation of heat. Therefore malfu nction etc. are known at the semiconductor device for having the fine structure with the generate and the be desirable paper.

한편, 3배 피치 이상의 간격에 더미 배선을 설치하는 것도 가능하지만, 배선 구조가 미세하게 되고, 더미 배선을 설치하는 효과가 떨어지게 된다.

In the meantime, it is possible to set up the dummy line in the gap more than the treble pitch. However the wiri ng structure is minute and the effect setting up the du mmy line falls down.

여기서, 상기 피치는 배선이 설계에 있어서 임의 배선의 중심과 이웃하는 배선의 중심과의 거리를 말한다. 반도체 장치는 임의 피치에서 배선층을 형성하지만, 반도체 장치의 다른 부분에서는 이 배선간의 거리가 3배 피치 이상인 개소가 있다. 일반적으로 유기막 및 크세로겔을 함유하는 막은 종래 층간 절연막으로서 사용되었던 산하 실리콘막에 비하여 열전도율이 1/10 정도로 상당히 작다. 본 발명은 이러한 열확산을 위하여 배선 패턴에 대하여 최소한 3배 피치 이상의 배선 간격의 부분에 더미 배선 패턴을 형성하는 것이다.

Here, pitch wiring refers to the distance of the center-bloom fruit of the wiring adjacent with the center of th e arbitrary wiring as to the design. In the semiconduct or device is the arbitrary pitch, the wiring layer is form ed. However it has the place in which the distance bet ween this wiring is the treble pitch or greater in the dis similar part of the semiconductor device. Generally, the thermal conductivity is considerably little in comparison with the load diversity silicon film in which the film cont aining the organic layer and xerogel was used as the c onventional inter-layer insulating film to about 1/10. Th e invention forms the dummy line pattern for such ther mal diffusion about the wiring pattern on the part of th e wiring space more than at least treble pitch.

이 더미 배선 패턴은 상술한 배선의 패터닝 때, 더미를 위한 배

This dummy line pattern the wiring for the dummy

GF Exhibit 1124 - 2162/2704

선이 패터닝을 동시에 행하고, 통상의 배선의 형성과 동일하게 하여 형성하는 것이 제조 공정상 바람직하다.

simultaneously performs the patterning in the patterning of the above-described wiring and it is in manufacturing process be desirable to make identical with the formation of the normal wiring and form.

다음에, 상기 기판을 세정한 다음, 다층 배선의 경우에는, 제2 유전막을 200~400㎚의 두께로 형성한다. 이 유전막으로서는 예를 들면 산화 실리콘막, 질화 실리콘막 이외에, 상술한 재료로 이루어진 유기막, 크세로겔을 함유하는 막 등을 추천할 수 있지만, 반도체의 용량을 작게 하기 위하여 유기막 및 크세로겔을 함유하는 막을 사용하는 것이 바람직하다.

Next, after the substrate is washed the second dielectric layer is formed into the thickness of 200~400 ㎚ in the multilayer interconnection. The organic layer, consisting of this dielectric layer, for example, the silicon dioxide film, and the material describing in detail besides the silicon nitride film the film etc. can be recommended. However containing the xerogel it is the be desirable to use the film which contains the organic layer and xerogel in order to make the capacity of the semiconductor small.

다음에, 상기와 동일하게 하여 제2의 배선층을 형성한 다음, 이상의 조작을 반복하고, 최후에 상층을 패시베이션(passivation) 막으로 피복하는 것에 의하여 배선 가공을 완료한다.

Next, after it makes identical with the above and the second wiring layer is formed the operation described in the above is repeated and it is according to coat the upper layer on the last with the passivation film and the wiring processing is completed.

이상과 같이 하여 제조된 본 발명의 반도체 장치의 제조 방법은 다층 배선 구조를 가지는 반도체 장치의 제조에 특히 바람직하게 적용할 수 있다.

As described above, preferably the manufacturing method of the semiconductor device of the invention doing and is manufactured especially can apply to the manufacture of the semiconductor device for having the multi-layer interconnection structure.

다음에, 본 발명의 반도체 장치 및 이 반도체 장치의 제조 방법을 발명의 실시예의 설명에 따라 다시 상세히 설명한다.

Next, according to the description of the embodiment of the invention the manufacturing method of semiconductor device and this semiconductor device of the present invention, it again particularly illustrates.

<u>제1 실시예</u>

<u>First preferred embodiment</u> .

도 1에 본 발명의 반도체 장치의 제1 실시예의 단면도를 나타낸다. 이 반도체 장치는 2층의 배선 구조를 가지는 n채널 MOS형 트랜지스터이다.

The cross-sectional view of the first preferred embodiment of the semiconductor device of the invention is shown in fig. 1. This semiconductor device is the N-channel Metal Oxide Semiconductor type transistor having the wiring structure of 2 layer.

이 반도체 장치는 p형 실리콘 반도체 기판(1)상에 트렌치(trench) 법에 의해 형성된 산화 실리콘막(2)으로 이루어진 아이솔레이션(isolation) 영역에, 도시하지 않은 n형 불순물이 이온 주입된 소스 영역과 드레인 영역을 가진다. 그리고, 이 반도체 기판(1)의 위에 게이트 산화막(3)을 통하여 중앙부에 폴리 실리콘으로 이루어진 게이트 전극(4)이 설치되고, 게이트 전극(4)은 도시하지 않은 게이트와 접속한다. 또한 그 위에는 유전율비가 3.0 이하인 저유전율막으로 이루어진 층간 절연막(5)이 설치되어 있다.

This semiconductor device has the area-source in which the n-type impurity not shown is ion-implanted in the isolation domain consisting of the silicon dioxide film (2) formed on the p-type silicon semiconductor substrate (1) with the trench method and the drain region. And the gate electrode (4) consisting of the poly-silicon is installed at the upper part of this semiconductor substrate (1) through the gate oxidation film (3) in the central part and it connects with the gate which the gate electrode (4) does not show. Moreover, the inter-layer insulating film (5) consisting of the low-dielectric-layer in which the dielectric constant ratio is 3.0 or less may be installed in the upper part.

그리고 또한 그 위에는 알루미늄으로 이루어진 배선층(6)이 설치된다. 이 배선층은 편의상 도면에서 구별하지 않는 통상의 배선층과 방열을 위한 더미 배선층으로 이루어진다. 이 더미 배선층은 배선 패턴에 대하여 최소한 3배 피치 이상의 배선 간격의 부분에 형성된다. 그리고, 상기 배선층은 콘택트홀(7)을 통하여 소스 영역과 드레인 영역과 접속한다.

And moreover, the wiring layer (6) consisting of aluminum may be installed in the upper part. This wiring layer includes the normal wiring layer which it does not distinguish in for convenience drawing, and the dummy wiring layer for the heat radiation. This dummy wiring layer is formed in the part of the wiring space more than at least treble pitch about the wiring pattern. And the wiring layer connects through the contact hole (7) with the area-source and drain region.

GF Exhibit 1124 - 2163/2704

이 반도체 장치에서는 이 배선층의 상층의 높이는 산화막을 제거하기 위한 상기 저유전율막(5)의 상측의 높이보다 조금 높게 형성되어 있다.

In this semiconductor device, the height of the upper layer of this wiring layer is a little high formed than the height of the upper side of the low-dielectric-layer (5) for removing the oxide film.

그리고, 상기 저유전율막(5)의 위에는 제2층째의 배선층(8)이 설치되어 있다. 또한, 이것의 상부에는 질화 규소로 이루어진 제2층째의 저유전율막(9)이 설치되고 또한, 비아 콘택트홀(10)을 통하여 제3층째의 배선층(11)이 설치되어 있다. 그리고 그 위에 패시베이션막(12)이 형성된 구조를 가지고 있다.

And the wiring layer (8) of the second layer may be installed in the upper part of the low-dielectric-layer (5). Moreover, moreover, the wiring layer (11) of the t hird layer through the via contact hole (10) the low-die lectric-layer (9) of the second layer is installed consisti ng of the silicon nitride may be installed in the upper po rtion of this. And it has with the structure in which the passivation film (12) is formed in the upper part.

본 실시예의 반도체 장치는 층간 절연막에 유전율비가 3.0이하인 유전체막을 사용하기 때문에, 배선간 용량의 증대가 억제된 미세한 다층 구조를 가지는 반도체 장치로 되어 있다.

It consists of the semiconductor device for having the multi-layered structure of being minute in which the inc rease in capacity between wiring the semiconductor de vice of this embodiment uses the dielectric film in whic h the dielectric constant ratio is 3.0 or less in the inte r-layer insulating film is suppressed.

또, 방열을 위한 더미 배선층을 배선 패턴에 대하여 최소한 3배 피치 이상의 배선 간격의 부분에 설치하는 것에 의하여, 열전도율이 작은 저유전율막을 사용하는 것에 의한 열확산 효율의 저하를 효과적으로 방지할 수 있다.

And the part is according to set up the dummy wiring layer for the heat radiation in the part of the wiring spa ce more than at least treble pitch about the wiring pat tern and the degradation of the thermal diffusion efficie ncy which is according to use the low-dielectric-layer i n which the thermal conductivity is little can be effecti vely prevented.

제2 실시예

Second embodiment .

본 발명의 제2 실시예는 본 발명의 반도체 장치인 CMOS 집적회로의 제조 방법이다.

It is the CMOS integrated circuit producing method in which the second preferred embodiment of the inventio n is the semiconductor device of the invention.

우선, 도 2a에 도시한 바와 같이, 포스포러스를 도핑한 n형 실리콘 반도체 기판(13)상에 열산화법에 의해 산화 실리콘막(14)을 형성한다. 다음에, 포토레지스트(15)를 사용하여 산화 실리콘막(14)상에 p-웰(well)의 영역이 되는 패턴을 형성하고, 이온 주입법에 의해 보론(boron)을 실리콘 기판내에 박아 넣음을 수행한다(도2a). 그 후, 도 2b에 도시한 바와 같이, 레지스트막(15)을 제거한다.

First, as shown in Figure 2a, the silicon dioxide film (14) is formed on the n-type silicon semiconductor substrat e (13) doping the phosphorous with the thermal oxidati on method. Next, the pattern in which it becomes the domain of the P-well (well) is formed using the photore sist (15) on the silicon dioxide film (14) and it performs with the ion implantation method driving the boron with in the silicon substrate (Figure 2a). Thereafter, as sho wn in Figure 2b, the resist film (15) is removed.

다음에, 도 2c에 도시한 바와 같이, 예를 들면, CVD법에 의해 전체면에 질화 실리콘막(17)을 퇴적하고, 포토 레지스트로 소자 분리 영역을 형성한 후, 포토 레지스트의 개공부의 질화 실리콘막(17)을 에칭에 의해 제거하여 개공한다.

Next, as shown in Figure 2c, for example, the silicon nitride film (17) is accumulated with the chemical vapor deposition in the total surface and the silicon nitride fil m (17) of the opening of the photoresist is removed wit h the etching and the element isolation region is opene d and is holed in the photoresist after doing the formati on.

다음에, 도 2d에 도시한 바와 같이, 선택적 산화법 (LOCOS법)에 의해 두꺼운 산화막(19)을 선택적으로 형성한다.

Next, as shown in Figure 2d, the thick oxide film (19) is selectively formed with the selective oxidation method (LOCOS).

이어서, 도 2e에 도시한 바와 같이, 마스크로서 사용하는 질화 실리콘막(17)과 그 아래의 산화 실리콘막(14)을 에칭에 의해 제거하고, 새로운 산화 실리콘막(20)을 형성하고, 또한 그 위에 예를 들면, CVD법에 의해 폴리 실리콘막을 성장형성하고,

Subsequently, as shown in Figure 2e, the silicon nitride film (17) and the following silicon dioxide film (14) used as the mask are removed with the etching and the new silicon dioxide film (20) is formed and the poly-silicon la

GF Exhibit 1124 - 2164/2704

소자 분리의 패터닝과 동일한 방법에 의해 게이트 전극(21)을 형성한다.

yer the gate electrode (21) is formed on moreover, the upper part with for example, the chemical vapor deposi tion with the patterning of the growth formation, and e lement isolation and same method.

또한, p-웰 형성과 동일한 방법으로 이온 주입법에 의해 p-웰 영역(16)에는 비소(砒素) (n+)를, p-웰 영역 이외에는 보론소(p+)를 실리콘 기판중에 주입하고, 열확산에 의해 n+ 영역(23)과 p+ 영역(22)을 형성한다.

Moreover, in the p- well region (16) by the p- well formation and same method the ion implantation metho d, the arsenic (n+) the boron minor (p+) is injected bes ides the p- well region among the silicon substrate and the n+ domain (23) and p+ domain (22) are formed wit h the thermal diffusion.

그리고, 도 2f에 도시한 바와 같이, 트랜지스터 등의 소자의 모양을 형성한 후, 그 위에 두께가 500㎚ 정도인 두꺼운 유전율비가 3.0 이하인 유전체막(24)을 형성한다. 이 유전체막(24)의 형성은 예를 들면, 전구체를 스핀코터로 기판 상에 성막하고 그 후, 300~450℃로 소성하는 것에 의해 수행할 수 있다. 또, 유전체막(24)이 아몰퍼스 카본 등인 경우에는 아세틸렌, 필요에 대응하여 플루오로 카본을 사용하여 플라즈마 CVD 장치를 사용하여 성막하고, 300~450℃로 소성하는 것에 의해 수행할 수 있다.

And as shown in Figure 2f, the shape of the device including the transistor etc. the dielectric film (24) in w hich the thick dielectric constant ratio in which the thi ckness is about 500㎚ in the upper part is 3.0 or less is formed after doing the formation. By depositing and pla sticizing at 300~450℃ on the substrate the formation o f this dielectric film (24) can perform for example, the p recursor to the spin coater. And in case the dielectric f ilm (24) is the amorphous carbon film etc. it correspond s to the acetylene, and the need and it deposits to ** * using carbon using the plasma CVD apparatus and it can be performed by being plasticized at 300~450℃.

다음에, 도 2g에 도시한 바와 같이, 상기 유기막의 위에 예를 들면, 무기막으로서 산화 실리콘막(25)을 형성한 다음, 레지스트막(26)을 성막하여 각각의 소자와 금속 배선을 접속하기 위한 콘택트홀을 형성하기 위한 패터닝을 행한다. 상기 산화 실리콘막(25)은 예를 들면, 플라즈마 CVD 장치에 의해, 실란 가스 50 sccm, N2O 가스 1000 sccm의 환원적 분위기 하에서 플라즈마 파워 500W, 압력 10 Torr, 온도 350℃에서 성막할 수 있다.

Next, as shown in Figure 2g, after the silicon dioxide film (25) is formed on the upper part of the organic lay er as for example, the inorganic film the patterning for f orming the contact hole for the resist film (26) being d eposited and connecting each device and metal wiring i s performed. Using the silicon dioxide film (25), for exa mple, the plasma CVD apparatus, can deposit under th e silane gas 50 sccm, and the ring member mood of N 2 O gas 1000 sccm in the plasma power 500W, the press ure 10 Torr, and the temperature 350℃.

그 후, 도 2h에 도시한 바와 같이, 콘택트홀(27)을 형성한다. 콘택트홀(27)은 예를 들면 일반적인 마그네트론 방식의 에칭 장치를 사용하여, 최상층의 산화 실리콘막(25), 그 하층의 유기막(24)을 각각 에칭하는 것에 의해 형성한다. 에칭의 조건은 예를 들면, 저유전율막의 경우는 CHF3 (5 sccm), O2 (50 sccm), He (200sccm) 가스를 사용하여 RF 플라즈마 파워 500W, -10℃의 저온이고, 산화 실리콘막의 경우는 예를 들면, C2F6 (14 sccm), CO (180 sccm), Ar (240 sccm), O2 (6 sccm) 가스를 사용하여 RF 플라즈마 파워 1500W이다. 이 경우, 상층의 산화 실리콘막(25)은 저유전율막을 에칭할 때의 마스크의 역할도 완수한다.

Thereafter, as shown in Figure 2h, the contact hole (27) is formed. It forms by the result of that the conta ct hole (27) etches the silicon dioxide film (25) of the t op layer, and the organic layer (24) of the lower layer t o the respectively using for example, the etching devic e of the general magnetron mode. The condition of the etching is the CHF 3 (5 sccm), O 2 (50 sccm), the RF p lasma power 500W using the He (200sccm) gas, and th e low temperature of -10℃ in case of for example, the l ow-dielectric-layer and it is the RF plasma power 1500 W in case of silicon dioxide film using for example, C 2 F 6 (14 sccm), the CO (180 sccm), the Ar (240 sccm), O 2 (6 sccm) gas. In this case, the role of the mask whe n the silicon dioxide film (25) of the upper layer etches the low-dielectric-layer accomplishes.

다음에, 도 2i에 도시한 바와 같이, 다마신법에 의해 배선(28)을 형성한다. 즉, 배선 재료로서 예를 들면, 동을 스퍼터링 장치 또는 CVD 장치에 의해 전체면에 퇴적시키고, 이어서, CMP법에 의해 여분의 금속을 예를 들면 알루미나를 사용하여 연마한다. 이것은 완전하게 여분의 금속을 제거하기 위함과, 산화 실리콘막에 새겨진 스크래치를 제거하기 위한 것이다. 그 후, 산화 실리콘막을 일반적인 마그네트론 방식의 에칭 장치를 사용하여 에칭한다. 이 때의 조건은 예를 들면, C2F6 (14 sccm), CO (180 sccm), Ar (240 sccm)이다. 이 조건에서는 유전체막(24)은 거의 에칭되지 않는다.

Next, as shown in Figure 2i, the wiring (28) is formed with the damascene method. That is, in case of subseq uently, the extra metal by the CMP law for example, th e copper is sedimented on the total surface as the wiri ng material with the sputtering device or the performin g apparatus, it polishes using alumina. The scratch car ved in the silicon dioxide film is to be removed this is to this be perfect remove the extra metal. Thereafter, the silicon dioxide film is etched using the etching device of the general magnetron mode. The condition at this tim e is for example, C 2 F 6 (14 sccm), the CO (180 scc m), and the Ar (240 sccm). In this condition, the dielec tric film (24) is not etched at the nearly.

GF Exhibit 1124 - 2165/2704

이와 같이 형성된 금속 배선층(28)의 상면은 산화막(25)을 제거하기 때문에, 유전체막보다도 높게 형성되게 된다.

The upper side of the metal wiring layer (28) formed in this way removes the oxide film (25). Therefore it is for med than the dielectric film.

다음에, 도 2j에 도시한 바와 같이, 기판 표면을 세정한 후, 패시베이션막으로서 산화 실리콘막(29)을 300㎚ 형성한다. 웨이퍼 프로세스의 완료 후, 마운팅(mounting), 본딩(bonding) 프로세스를 수행하는 것에 의해 요구되는 반도체 장치를 제조할 수 있다.

Next, as shown in Figure 2j, the substrate surface the silicon dioxide film (29) is formed after doing washing as the passivation film with 300㎚. The semiconductor dev ice for being required by performing the mounting, and the bonding process after the completion of the wafer process can be manufactured.

이상 설명한 바와 같이, 본 실시예에 의하면, 저유전율막을 사용하고, 배선간 용량의 증대가 억제된 미세 구조의 반도체 장치를 효율 좋게 제조할 수 있다.

As described above, it is good with efficiency the semiconductor device of the fine structure in which the increase in capacity between wiring the low-dielectric-l ayer is used according to this embodiment is suppresse d can be manufactured.

제3 실시예

Third embodiment .

본 발명의 제3실시예는 패시베이션막으로서 저유전율막을 사용하는 반도체 장치의 제조 방법이다.

The third preferred embodiment of the invention is the method for manufacturing semiconductor device using t he low-dielectric-layer as the passivation film.

먼저, 도 2i에 도시한 것과 동일한 반도체 장치의 중간물이 형성된다. 즉, 반도체 기판 상에 소자 분리막에 의하여 분리된 영역의 산화 게이트막 상에 게이트 전극을 형성하고, 콘택트 플러그를 통하여 소스와 드레인 영역(22#39#, 23#39#)과 접속하는 저도전층을 형성하고, 전체면에 산화 실리콘막을 형성한 다음, 마스크로서 레지스트막을 사용하여 상층 배선층과 접속하는 비아 콘택트 플러그를 형성한다.

In advance, the medium of the it shows same semiconductor device is formed in the drawing 2i. That is, the gate electrode is formed on the oxidation gate fi lm of the domain separated on the semiconductor subs trate with element isolation film and the low-level front layer connecting through the contact plug with source and drain region (22', 23') is formed and after silicon di oxide film are formed on the total surface the via conta ct plug connecting using resist film with the upper layer wiring layer is formed as the mask.

다음에, 도 3a에 도시한 바와 같이, 상세한 설명을 생략한 상기의 중간물을 실리콘 기판(30)상에 두께 500㎚로 산화 실리콘막(31)을 형성하고, 또한 그 위에 두께 500㎚ 로 유전율비가 3.0이하인 저유전율막(32) 및 두께가 100㎚로 무기막으로서 산화 실리콘막(33)을 형성한다.

Next, as shown in Figure 3a, the medium described in the above omitting the detailed explanation the silicon dioxide film (31) is formed on the silicon substrate (30) into the thickness 500㎚ and the low-dielectric-layer (3 2) and the thickness in which the dielectric constant ra tio is 3.0 or less to the thickness 500㎚ form the silicon dioxide film (33) on moreover, the upper part into 100㎚ as the inorganic film.

이 저유전율막(32)은 제2 실시예와 동일하게 성막할 수 있다. 산화 실리콘막(33)은 제2 실시예의 경우와 동일하게 하여 플라즈마 CVD법에 의해 환원 분위기 하에서 행한다. 예를 들면, 실란 가스 50 sccm, N2O 가스 1000 sccm, 플라즈마 파워 500W, 압력 10 Torr, 온도 350℃의 조건에서 행할 수 있다.

This low-dielectric-layer (32) can deposit identically with the second preferred embodiment. It makes identi cal with the case of the second preferred embodiment and the silicon dioxide film (33) performs with the plasm a CVD method under the reducing atmosphere. For exa mple, it can perform in the condition of the silane gas 5 0 sccm, N 2 O gas 1000 sccm, plasma power 500W, pr essure 10 Torr, temperature 350℃.

다음에, 도 3b에 도시한 바와 같이, 레지스트(34)를 마스크로 사용하여 배선 패턴(34)을 형성한다. 다음에, 도 3c에 도시한 바와 같이, 일반적인 마그네트론 방식의 에칭 장치를 사용하여 최상층의 산화 실리콘막(33) 및 그 하층의 유기막(32)을 에칭

Next, as shown in Figure 3b, the wiring pattern (34) is formed by using the resist (34) as the mask. Next, as s hown in Figure 3c, the silicon dioxide film (33) of the to p layer and organic layer (32) of the lower layer are et

GF Exhibit 1124 - 2166/2704

한다. 예를 들면, 저유전율막의 경우는, CHF3 (5 sccm), O2 (50 sccm), He (200 sccm) 가스를 사용하여 RF 플라즈마 파워 500W, -10℃의 저온으로 에칭을 행할 수 있다. 또, 산화 실리콘막의 경우는 예를 들면, C2F6 (14 sccm), CO (180 sccm), Ar (240 sccm), O2 (6 sccm) 가스를 사용하여 RF 플라즈마 파워 1500W로 에칭할 수 있다. 이 경우, 상층의 산화 실리콘막(33)은 저유전율막(32)을 에칭할 때의 마스크의 역할도 완수한다.

ched using the etching device of the general magnetron mode. For example, in case of the low-dielectric-layer, the etching can be performed into the RF plasma power 500W, and the low temperature of -10℃ using the CHF 3 (5 sccm), O 2 (50 sccm), and the He (200 sccm) gas. And in case of the silicon dioxide film, it can etch for example to the RF plasma power 1500W using C 2 F 6 (14 sccm), the CO (180 sccm), the Ar (240 sccm), O 2 (6 sccm) gas. In this case, the role of the mask when the silicon dioxide film (33) of the upper layer etches the low-dielectric-layer (32) accomplishes.

다음에, 도 3d에 도시한 바와 같이, 배선 재료로서 예를 들면, 동을 스퍼터링 장치 또는 CVD 장치에 의해 퇴적시킨다. 이어서, CMP법에 의해 여분의 금속을 예를 들면 암모니아를 사용하여 연마한다. 이것은 완전하게 여분의 금속을 제거하기 위함과 산화 실리콘막에 새겨진 스크래치를 제거하기 위한 것이다.

Next, as shown in Figure 3d, for example, the copper is sedimented as the wiring material with the sputtering device or the performing apparatus. Subsequently, in case of the extra metal by the CMP law, it polishes using ammonia. The scratch carved in the silicon dioxide film this is to this be perfect remove the extra metal is to be removed.

그 후, 산화 실리콘막(33)을 일반적인 마그레트론 방식의 에칭 장치를 사용하여 에칭한다. 이 때의 에칭 조건은 예를 들면, C 2F6 (14 sccm), CO (180 sccm), Ar (240 sccm)이다. 이 조건에서는 저유전율막(32)은 거의 에칭되지 않는다.

Thereafter, the silicon dioxide film (33) is etched using the etching device of the general magnetron mode. The etching condition at this time is for example, C 2 F 6 (14 sccm), the CO (180 sccm), and the Ar (240 sccm). In this condition, the low-dielectric-layer (32) is not etched at the nearly.

이와 같이 형성된 금속 배선(35)의 상면은 도 3e에 도시한 바와 같이, 유기막(32)의 상면보다도 높게 형성된다.

As shown in the upper side of the metal wiring (35) formed in this way is 3e, it is high formed than the upper side of the organic layer (32).

다음에, 도 3f에 도시한 바와 같이, 기판 표면을 세정한 후, 패시베이션막으로서 제2 저유전율막(36)을 제1의 저유전율막과 동일하게 하여 두께 300㎚로 형성한다.

Next, as shown in Figure 3f, it makes identical with the first low-dielectric-layer and the substrate surface the second low-dielectric-layer (36) is formed after doing washing as the passivation film into the thickness 300 ㎚.

최후에, 웨이퍼 프로세스의 완료 후, 마운팅, 본딩 프로세스를 수행하는 것에 의해 요구되는 반도체 장치를 제조할 수 있다.

In the last, the semiconductor device for being required by performing the mounting, and the bonding process after the completion of the wafer process can be manufactured.

이상 설명한 바와 같이, 본 실시예에 의하면, 저유전율막을 사용하는 미세 구조의 반도체 장치를 효율 좋게 제조할 수 있다. 또, 본 실시예에 의해 제조되는 반도체 장치는 패시베이션막으로서 제1의 저유전율막과 동일하게 하여 제2의 저유전율막을 사용하는 것에 의하여, 배선간의 용량이 작은 반도체 장치를 얻을 수 있다.

As described above, according to this embodiment, it is good with efficiency the semiconductor device of the fine structure of using the low-dielectric-layer can be manufactured. And it makes identical with the first low-dielectric-layer and the semiconductor device for being manufactured with this embodiment uses the second low-dielectric-layer as the passivation film it is according to and the semiconductor device in which capacity between wiring is little can be obtained.

제4 실시예

Fourth embodiment .

제4 실시예는 2층의 배선 구조를 가지고 또한 더미 배선(42)을 가지는 반도체 장치의 제조예이다.

It is the manufacturing example of the semiconductor device in which the fourth preferred embodiment has moreover, the dummy line (42) with the wiring structure of 2 layer.

방열 경로로서 더미 배선이 설치되는 것 이외는 제3 실시예의 도 3f까지의 상태와 동일한 공정을 거치는 것에 의해 얻을 수 있는 구조의 단면도를 도 4a에 도시한다.

The cross-sectional view which it can obtain by the result of that the dummy line is installed as the thermal via the except goes through the same justice as state to the drawing 3f of the third preferred embodiment of the structure is shown in the drawing 4a.

GF Exhibit 1124 - 2167/2704

즉, 먼저, 도시하지 않은 트랜지스터, 배선 패턴 등이 형성된 실리콘 반도체 기판(37) 상에 두께 500㎚로 산화 실리콘막(38)을 형성하고, 그 위에 두께 500㎚로 유전율비가 3.0 이하인 저유전율막(39), 동으로 이루어진 배선(40) 및 제2의 유전율막(41)을 형성한다.

That is, the wiring (40) and the second permittivity layer (41) consisting of the transistor not shown in advance, the low-dielectric-layer (39), and copper are formed. As to the low-dielectric-layer (39), it forms the silicon dioxide film (38) into the thickness 500㎚ on the silicon semiconductor substrate (37) in which the wiring pattern etc. are formed and the dielectric constant ratio is 3.0 or less in the upper part to the thickness 500 ㎚.

더미 배선(42)은 CMP법에 의해 금속 배선을 형성한 다음, 레지스트를 마스크로 사용하여 더미 패턴을 에칭하는 것에 의해 형성한다. 이 때, 배선 피치가 최소 피치의 3배 이상인 곳에 더미 패턴을 삽입하여 배선 간격이 최소한 1 ㎛ 이상의 개소를 제거한다. 배선 더미의 삽입은 배선 아스펙트비와 최소 배선 피치(절대치)에 의존한다. 예를 들면, 아스펙트비 2, 최소 배선 피치가 0.5 ㎛인 경우, 최소 배선 간격은 대략 0.25 ㎛가 됨으로, 0.75 ㎛ 이상의 배선 간격을 최소한 확보하고, 1 ㎛ 이상의 배선 간격을 없애도록 더미 배선을 형성하는 것이 바람직하다. 그 후, 제2의 저유전율막(41)을 제1의 저유전율막의 형성과 동일하게 하여 형성하는 것에 의하여 도4a에 도시한 상태를 얻는다.

After the dummy line (42) forms the metal wiring with the CMP law by etching the dummy pattern by using the resist as the mask it forms. Then, the dummy pattern is inserted into the place where the wiring Pitch is the treble or greater of the minimum feature of pitch and the wiring space removes the place more than at least 1 ㎛. The insertion of the wiring dummy depends on the wiring aspect ratio and minimum wiring Pitch (absolute value). For example, in case the aspect ratio 2, and the minimum wiring Pitch are 0.5 ㎛ approximately, 0.25 ㎛ becomes the minimum wiring space. In that way the wiring space more than 0.75 ㎛ is secured at least and it is the be desirable to form the dummy line in order to remove the wiring space more than 1 ㎛. Thereafter, it is according to make identical with the formation of the first low-dielectric-layer and form the second low-dielectric-layer (41) and the state shown is obtained in the drawing 4a.

다음에, 도 4b에 도시한 바와 같이, 레지스트막(43)을 전체면에 퇴적시킨 후, 제1층째의 배선과 제2층째의 배선을 접속하는 콘택트홀(44) 형성을 위한 패터닝을 수행하고, 도 4c에 도시한 바와 같이, 이 콘택트홀(44)에 텅스텐 등의 금속을 매입한다.

Next, as shown in Figure 4b, after the resist film (43) is sedimented on the total surface the patterning for the contact hole (44) formation connecting the wiring of the first layer and wiring of the second layer is performed and as shown in Figure 4c, the metal of the tungsten lamp is purchased in this contact hole (44).

다음에, 도 4d에 도시한 바와 같이, 전체면에 질화 실리콘으로 이루어진 무기막(45)을 예를 들면, CVD법에 의해 두께 100㎚로 성막하고, 도4e에 도시한 바와 같이, 레지스트(46)에 의해 제2의 배선 패터닝을 행한다. 다음에, 도4f에 도시한 바와 같이, 배선 패턴을 포토 에칭에 의해 형성한다.

Next, as shown in Figure 4d, in case of the inorganic film (45) made of the silicon nitride in the total surface deposit with the chemical vapor deposition to the thickness 100㎚ and as shown in Figure 4e, the second wiring patterning is performed with the resist (46). Next, as shown in Figure 4f, the wiring pattern is formed with the photo- etching.

그리고, 도 4g에 도시한 바와 같이, 전체면에 배선 재료로서 알루미늄(47)을 진공 증착법에 의해 전체면에 퇴적시키고, 도 4h에 도시한 바와 같이, CMP법에 의해 상술한 것과 동일하게 하여 제2의 배선층(48)을 형성한다.

And as shown in Figure 4g, the aluminum (47) is sedimented on the total surface in the total surface as the wiring material with the vacuum deposition method and it makes identical and as shown in Figure 4h, describes in detail with the CMP law the second wiring layer (48) is formed.

이와 같이 하여 형성된 제2의 금속 배선(48)의 상면은 제2의 유기막(40)의 상면보다도 높게 형성된다.

The upper side of the metal wiring (48) of the second formed in this way is high formed than the upper side of the second organic layer (40).

다음에, 도 4i에 도시한 바와 같이, 기판 표면을 세정한 후, 패시베이션막으로서 산화 실리콘막을 예를 들면 CVD법에 의해 두께 500㎚로 형성한다.

Next, as shown in Figure 4i, in case of the silicon dioxide film as the passivation film after doing the washing, the substrate surface, it forms into the thickness 500㎚ with the chemical vapor deposition.

최후에, 웨이퍼 프로세스의 완료 후, 마운팅, 본딩 프로세스를 수행하는 것에 의해 요구되는 반도체 장치를 제조할 수 있다.

In the last, the semiconductor device for being required by performing the mounting, and the bonding p

GF Exhibit 1124 - 2168/2704

rocess after the completion of the wafer process can b e manufactured.

이상 설명한 바와 같이, 본 실시예에 의하면, 저유전율막을 사용하는 미세 구조의 신뢰성이 매우 높은 반도체 장치를 효율 좋게 제조할 수 있다.

As described above, according to this embodiment, it is good with efficiency the reliability of the fine structure of using the low-dielectric-layer can manufacture very high semiconductor device.

본 실시예에 의해 제조되는 반도체 장치는 층간 절연막으로서 저유전율막을 사용함으로써, 반도체 장치의 배선간의 용량을 대폭 감소시킬 수 있다.

The semiconductor device for being manufactured with this embodiment uses the low-dielectric-layer as the in ter-layer insulating film. In that way capacity between the wiring of the semiconductor device can be drastical ly reduced.

또, 더미 배선을 배선 피치가 최소 피치의 3배 이상인 곳에 더미 패턴을 삽입하여 배선 간격이 최소한 1 ㎛ 이상인 개소를 없애도록 함으로써, 열전도율이 낮은 유기막을 사용하는 경우에 있어서도 반도체 장치의 내부에서 발생하는 열을 외부에 방출할 수 있으므로, 발열에 의한 고장이 없는 신뢰성이 높은 반도체 장치이다.

And the dummy line the dummy pattern is inserted into the place where the wiring Pitch is the treble or greate r of the minimum feature of pitch and the place in whic h the wiring space is at least 1 ㎛ or greater is remove d. In that way even in case of using the organic layer i n which the thermal conductivity is low the heat gener ated within the semiconductor device can be emitted t o the outside. Therefore it is the semiconductor device in which the reliability without malfunction by the heat generation is high.

제5 실시예

Fifth embodiment .

본 발명의 제5 실시예는 2층 구조를 가지는 반도체 장치에 있어서, 배선층간(좌우)의 층간 절연막으로서 크세로겔을 함유하는 막을 사용하고, 배선층간(상하)에 유전율비가 3.0 이하인 유전체막을 사용한 반도체 장치의 제조예이다. 본 실시예에 의해 제조되는 반도체 장치의 주요 공정 단면도를 도 5a 내지 도 5f에 도시한다. 또한, 이하의 도에 있어서는 편의상 소자 분리막, 전극 등은 도시를 생략한다.

The fifth preferred embodiment of the invention is the manufacturing example of the semiconductor device wh ich uses the film containing the xerogel and uses the di electric film in which the dielectric constant ratio is 3.0 or less in wiring layer liver (top and bottom) as the inte r-layer insulating film of wiring layer liver (right and lef t) as to the semiconductor device, for having the two-l ayer structure. The major processing sectional view of the semiconductor device for being manufactured with this embodiment is shown in the figures 5a through 5f. Moreover, it is in the drawing of less than and for conv enience element isolation film, the electrode etc. omit t he illustration.

먼저, 도시하지 않은 트랜지스터, 배선 패턴 등이 형성된 실리콘 반도체 기판(50)상에 실리콘 산화막, 실리콘 질화 산화막, 실리콘 질화막 등의 절연막(51)을 형성한다. 실리콘 산화막은 예를 들면, 스핀코터법을 사용하고, 시판되는 무기 SOG(실라놀 또는 실라놀을 포함하는 폴리머를 주요 성분으로 하는 것)를 약 50㎚의 두께로 형성한다. 이 경우, 스핀코터 후는 150~200℃로 1분 정도의 베이킹(baking)을 행하여 큐어(cure)를 350~450℃로 30분에서 1시간을 행한다. 실리콘 산화막은 플라즈마 장치를 사용하여 플라즈마 CVD 법에 의해 형성할 수 있지만, 동배선을 산화시키는 것을 가능한 방지하기 위하여, 산화제로서 N2O 가스를 사용하고, 실리콘막으로서 모노실란, 디실란, 트리실란 등의 실란류를 사용하는 것이 바람직하다. 플라즈마 CVD법에 의한 경우는 기판 온도 300~400℃, 플라즈마 파워 350W, 압력 1kPa 정도의 조건에서 성막할 수 있다.

In advance, the insulating layer (51) including the silicon oxide film, the silicon nitride oxide film, the silico n nitride film etc. is formed on the silicon semiconducto r substrate (50) in which the transistor, not shown the wiring pattern etc. are formed. The silicon oxide film us es for example, the spin coating method and the inorga nic spin on glass (it has the silanol or the polymer inclu ding the silanol as the principal component) coming into the market is formed into the thickness of about 50㎚. In this case, about 1 minutes the baking is performed i nto 150~200℃ after the spin coater and the cure 1 ho ur is performed into 350~450℃ in 30 minutes. The silico n oxide film is the be desirable to use the silanes includi ng the monosilane as the silicon film, the disilane, the t risilane etc. N 2 O gas is used as the oxidizing agent it can form using the plasma device with the plasma CVD method and however possible oxidizing the copper wirin g. It prevents. The case by the plasma CVD method ca n deposit in the substrate temperature 300~400℃, the plasma power 350W, and the condition of about pressu re 1kPa.

실리콘 질화 산화막의 경우는 아미노기를 가지는 시판되는 무

In case of the silicon nitride oxide film, the inorganic

GF Exhibit 1124 - 2169/2704

기 SOG를 스핀 코터법으로 성막할 수 있지만, 바람직하게는 플라즈마 CVD법을 사용하여 성막한다. 사용하는 가스로서 예를 들면, 실리콘 소스로서 모노실란, 디실란, 트리실란 등의실란류를 사용하고, 질화제로서 예를 들면 암모니아, 하이드라진 등을, 산화제로서 N2O 가스를, 캐리어(carrier) 가스로서 질소, 헬륨, 아르곤 등을 각각 사용하고, 기판 온도를 300~400℃, 플라즈마 파워 350W, 압력 1kPa 정도의 조건에서 성막할 수 있다.

spin on glass which comes into the market to go to the amino group can be deposited to the spin coating method. However it preferably deposits using the plasma CVD method. The monosilane, the disilane, and the trisilane tergal silanes are used as the gas used as for example, the silicon source and for example, ammonia, hydrazine etc. N 2 O gas nitrogen, the helium, argon etc. are used as the nitriding agent as the oxidizing agent as the carrier gas and the substrate temperature can be deposited in 300~400℃, the plasma power 350W, and the condition of about pressure 1kPa.

다음에 전체면에 도시하지 않은 레지스트막을 성막한 후, 소정의 패터닝을 수행하고, 포토 에칭법으로 콘택트홀을 형성하고, 텅스텐 등의 금속을 매입하는 것에 의해 콘택트 플러그(52)를 형성한다.

Next, the resist film which it does not show in the total surface the predetermined patterning is performed after doing the deposition and the contact hole is formed into the photo etching method and the contact plug (52) is formed by purchasing the metal of the tungsten lamp.

다음에, 저유전율막(53)을 두께 300~800㎚ 정도로 성막하는 것에 의해 도 5a에 도시한 상태도를 얻는다. 상기 저유전율막(53)은 유전율비가 3.0이하인 절연막이라면 특히 제한이 없다. 예를 들면, 저유전율막이나 크세로겔을 함유하는 막을 예시할 수 있다. 그 외 저유전율막으로서는 상기 예시한 것을 사용할 수 있다.

Next, by depositing the low-dielectric-layer (53) to about thickness 300~800㎚ the phase diagram shown is obtained in the drawing 5a. If the low-dielectric-layer (53) is the insulating layer in which the dielectric constant ratio is 3.0 or less there is no especially, the limit. For example, film containing the low-dielectric-layer or the xerogel can be exemplified. The above-mentioned exemplified thing can be used as the besides low-dielectric-layer.

다음에, 예를 들면, 질화 실리콘, 실란 커플링제 등으로 이루어진 무기막(56)을 예를 들면, CVD 법에 의해 두께 100㎚로 전체면에 성막하고, 도시하지 않은 레지스크막에 의해 제1의 배선 패터닝을 수행하고, 배선 패턴을 포토 에칭에 의해 형성한다. 이 경우의 에칭은 예를 들면, 시판되는 에칭 장치로 C2F6 (14 sccm), CO (180 sccm), Ar (240 sccm) 가스를 사용하여 RF 플라즈마 파워 1500W로 수행할 수 있다.

Next, it for example in case of the inorganic film (56) consisting of silicon nitride, and the silane coupling agent etc deposits with the chemical vapor deposition to the thickness 100㎚ in the total surface and the first wiring patterning is performed with the register film not shown and the wiring pattern is formed with the photo- etching. The etching of this case can perform to for example, the etching device for coming into the market using C 2 F 6 (14 sccm), the CO (180 sccm), and the Ar (240 sccm) gas to the RF plasma power 1500W.

이어서, 도 5b에 도시한 바와 같이, 전체면에 배선 재료로서 알루미늄, 동, 동합금, 텅스텐 등의 금속을 진공 증착 등에 의해 퇴적시키고, CMP법에 의해 제1의 배선층(54)을 형성한다. 이 때, 상기 무기막(56)은 완전하게 제거되는 것이 바람직하지만, 실제의 제조상은 도 5b에 도시한 바와 같이 기판 상에 잔존해도 된다.

Subsequently, as shown in Figure 5b, the metal of the aluminum, copper, copper alloy, tungsten lamp is sedimented on the total surface as the wiring material with the vacuum evaporation etc. and the first wiring layer (54) is formed with the CMP law. Then, as shown in the actual aspect of manufacturing is 5b the inorganic film (56) is completely removed, it remains on the substrate.

다음에, 도 5c에 도시한 바와 같이, 전체면에 저유전율막(57)을 두께 800㎚ 정도로 성막한다. 성막은 예를 들면 전구체를 스핀코터로 성막하고 그 후, 300~400℃로 큐어링(curing)(소성)하는 것에 의해 수행할 수 있다. 상기 저유전율막의 재료로서는 유전율비가 3.0 이하인 것이 바람직하고, 예를 들면 상기 예시한 것을 사용할 수 있다.

Next, as shown in Figure 5c, the low-dielectric-layer (57) is deposited in the total surface to about thickness 800㎚. By the result of that for example, the precursor is deposited to the spin coater and the thereafter the deposition is done by 300~400℃ with the curing (curing) (plasticity) it can perform. The dielectric constant ratio is the be desirable as the material of the low-dielectric-layer 3.0 or less and for example, the above-mentioned exemplified thing can be used.

또한, 아몰퍼스 카본 등의 재료를 사용하는 경우는 아세틸렌, 필요에 대응하여 플루오로 카본 가스를 사용하고, 플라즈마 CVD 장치를 사용하여 형성할 수 잇다. 이 경에도 300℃~400℃로 큐어링을 행한다.

Moreover, the case of using the material including the amorphous carbon film etc. corresponds to the acetylene, and the need and the carbon gas is used as *** and the need continue with number. It forms using the plasma CVD apparatus. The curing is performed into 30

GF Exhibit 1124 - 2170/2704

0℃~400℃ in this sir.

다음에, 도시하지 않은 레지스트막을 전체면에 성막한 후, 소정의 패터닝을 수행하고, 포토 에칭에 의해 제2의 콘택트홀을 제1의 배선층까지 형성한 다음, 텅스텐 등의 금속을 매입하는 것에 의해 비아 콘택트 플러그(58)를 형성한다(도 5d).

Next, the resist film not shown the predetermined patterning is performed in the total surface after doing the deposition and after the second contact hole is for med with the photo- etching to the first wiring layer th e via contact plug (58) is formed by purchasing the me tal of the tungsten lamp (Figure 5d).

다음에, 도 5e에 도시한 바와 같이, 전체면에 크세로겔을 함유하는 막(59)을 예를 들면, 두께 500㎚ 정도로 형성한다. 크세로겔로서는 예를 들면, 나노글래스(nanoglass)사가 개발한 Nonoporous Silica (제품명)를 사용할 수 있다. Nonoporous Silica (제품명)는 포로스 실리카의 일종이지만, 본 실시예에서는 이것에 한정되는 것은 아니고, 방향족 등의 비교적 고분자의 알킬기를 가지는 실라놀 수지를 웨이퍼 상에 도포하고, 그것을 겔화시켜서 실란 커플링제 또는 수소화 처리에 의해 소수 처리를 수행하여 형성되는 것도 된다.

Next, as shown in Figure 5e, in case of the film (59) containing the xerogel in the total surface, it forms into about thickness 500㎚. The Nonoporous Silica (product name) which for example, the nano glass (nanoglass) c orp. develops can be used as the xerogel. The Nonopor ous Silica (product name) is a kind of the porous silica. However in the present preferred embodiment, it is not restricted to this and the kinds coats the silanol resin t he alkyl group of the relative polymer including the aro matic family etc. on the wafer and it becomes that tha t is gelled and the hydrophobic process is performed wi th the silane coupling agent or the hydrotreating and t hat is formed.

또한, 이 경우 크세로겔을 함유하는 막은 특히 층간 밀착성이 부족하기 때문에, 상기 저유전율막 상에 상기 예시한 바와 같은 실란 커플링제를 박리 방지를 위하여 미리 도포하여 놓는 것이 바람직하다. 실린 커플링제로서는 일반식 RSiX3, RR#39# SiX2 (식 중, R, R#39#는 알킬기를 나타내고, X는 할로겐 원자를 나타낸다.)로 표시되는 알킬 실란류를 예시할 수 있다.

Moreover, in this case, as to the film, containing the xerogel especially, the clinging is insufficient. Therefore it is the be desirable to coat in advance with the abov e-mentioned silane coupling agent like exemplifying on t he low-dielectric-layer for the exfoliation prevention. T he alkysilanes indicated as the general formula RSiX 3 , and RR' SiX 2 (R , and the R' show the alkyl group in th e formula and X shows the halogen atom.) can be exe mplified as the loaded coupling agent.

다음에, 도시하지 않은 레지스트막을 전체면에 성막한 후, 소정의 패터닝을 수행하고, 포토 에칭에 의해 배선층을 위한 홈(trench)을 형성한다. 이 경우의 에칭은 예를 들면, 시판되는 에칭 장치로 C2F6 (14 sccm), CO (180 sccm), Ar (240 sccm) 가스를 이용하여 RF 플라즈마 1500W 파워로 수행할 수 있다. 이어서, 도5e에 도시한 바와 같이, 전체면에 배선 재료로서 알루미늄, 동, 동합금, 텅스텐 등의 금속을 진공 증착법에 의해 퇴적시킨 다음, 도시하지 않은 무기막을 퇴적시키고 예를 들면 실리카계 슬러리를 사용하는 CMP법에 의해 제2의 배선층(60)을 형성한다. 이 경우 무기막으로서는 제1의 배선층을 형성할 때에 예시한 것과 동일한 것을 사용할 수 있다. 또한, 무기막은 완전히 제거되는 것이 바람직하지만, 실제의 제조에서는 기판 상에 잔존해도 된다.

Next, the resist film not shown the predetermined patterning is performed in the total surface after doing the deposition and the groove (trench) for the wiring la yer is formed with the photo- etching. The etching of t his case can perform to for example, the etching devic e for coming into the market using C 2 F 6 (14 sccm), t he CO (180 sccm), and the Ar (240 sccm) gas to the R F plasma 1500W power. Subsequently, as shown in Fig ure 5e, after the metal of the aluminum, copper, coppe r alloy, tungsten lamp is sedimented on the total surfac e as the wiring material with the vacuum deposition me thod the inorganic film not shown is sedimented and th e second wiring layer (60) is formed with the CMP law using for example, the silica-based slurry. In this case, when the first wiring layer as the inorganic film is forme d, it can use being identical of. Moreover, it is the be d esirable that the inorganic film is completely removed. However it remains in the actual manufacture on the s ubstrate.

최후에, 도 5f에 도시한 바와 같이, 전체면에 산화 실리콘막 등의 절연막(61)을 패시베이션막으로서 형성하여 배선층의 형성 공정을 완료한다.

In the last, the insulating layer (61) including the silicon dioxide film etc. is formed on the total surface a s the passivation film and as shown in Figure 5f, the for mation process of the wiring layer is completed.

본 실시예에서는 배선층의 주위(배선층의 좌우), 바람직하게는 배선 간격이 표준 피치의 3배 이하인 개소에는 유전율비가 매우 작은 크세로겔을 함유하는 막을 사용하고, 또한, 배선간의 콘택트홀의 주위(배선층의 상하)에는 유전율비가 3.0 이하인

In the present preferred embodiment, in surrounding (right and left of the wiring layer) of the wiring layer, a nd the place in which preferably the wiring space is the treble or less of the standard pitch, the film in which th

GF Exhibit 1124 - 2171/2704

유전체막을 사용한다. 따라서, 크세로겔막의 기계적 강도, 열전도성, 내열성, 내습성, 층간 밀착성이 부족한 결점을 보충하면서, 배선 용량을 대폭 축소하는 것에 의하여, 신뢰성이 높은 미세 구조를 가지는 반도체 장치를 수득률 좋게 제조할 수 있다.

e dielectric constant ratio contains very small xerogel is used and the dielectric film in which the dielectric constant ratio is 3.0 or less is used in moreover, surrounding (top and bottom of the wiring layer) of the contact hole between wiring. Therefore, while the defect that the mechanical strength, the thermal conductance, the heat resistance, the wet-proof property, the clinging of the xerogel layer is insufficient is supplemented it is according to drastically reduce the wiring capacitance and it is good with yield the semiconductor device for having the fine structure where the reliability is high can be manufactured.

또, 크세로겔을 함유하는 막의 상하에는 실란 커플링제로 이루어진 층을 설치하는 것에 의하여, 층간 밀착성이 뛰어난 반도체 장치를 제조할 수 있다.

And in top and bottom of the film containing the xerogel, it is according to set up the layer consisting of the silane coupling agent and the semiconductor device in which the clinging is excellent can be manufactured.

또한, 방열을 위한 더미 배선을 설치함으로써, 반도체 장치 전체의 발열이 작고, 온도상승에 의한 오동작이 작은 신뢰성이 높은 반도체 장치이다.

Moreover, the dummy line for the heat radiation is set up. In that way the heat generation of the semiconductor device total is small and it is the semiconductor device in which the reliability in which malfunction by the temperature rise is small is high.

제6 실시예

Sixth preferred embodiment .

본 실시예에서는 층간 절연막으로서 저유전율 유기막을 사용하고 방열 경로로서 더미 배선층 및 더미 콘택트홀을 형성하는 예이다.

In the present preferred embodiment, it is the example using the low permittivity organic layer as inter-layer insulating film and forms the dummy wiring layer and dummy contact hole as the thermal via.

먼저, 도 6a에 도시한 바와 같이, 도시하지 않은 트랜지스터 등의 능동 소자, 소자 분리막(63)으로 구성된 실리콘 반도체 기판(62)상에 하층 층간 절연막(64)을 형성한다.

In advance, as shown in Figure 6a, the lower layer interlayer isolation film (64) is formed on the silicon semiconductor substrate (62) consisting of the active circuit element including the transistor etc. not shown, and element isolation film (63).

그 후, 도 6b에 도시한 바와 같이, 전체면에 레지스트막(65)을 성막하고 콘택트 플러그(콘택트홀) (66) 및 더미 콘택트 플러그(67)의 형성을 위한 패터닝을 수행한다. 더미 콘택트홀은 층간 절연막(63)상에서 상층에 형성하는 더미 배선의 하부에 형성하는 것이 제조상 바람직하다. 또, 콘택트 피치는 최소 피치가 되는 것이 바람직하다. 최소 피치로 하는 것에 의해 열전도성을 향상하고, 열확산 효율을 높일 수 있다.

Thereafter, as shown in Figure 6b, the resist film (65) is deposited in the total surface and the patterning for the formation of the contact plug (contact hole) (66) and dummy contact plug (67) are performed. It is the aspect of manufacturing be desirable to form on the lower part of the dummy line which the dummy contact hole forms on the upper layer on the inter-layer insulating film (63). And it is the be desirable that in the contact pitch, the minimum feature of pitch is. The thermal conductance is improved by being done by the minimum feature of pitch and the thermal diffusion efficiency can be raised.

또, 트랜지스터, 소자 분리막, 하층 층간 절연막, 콘택트 플러그 등의 형성은, 공지의 기술을 이용할 수 있다. 하층 층간 절연막으로서는 예를 들면 산화 실리콘막, 포스포러스, 또는 포스포러스 및 보론소가 불순물로서 도핑된 산화 실리콘막을 형성할 수 있다. 또, 콘택트 플러그(66,67)의 형성에는 텅스텐 등의 도전성 물질을 매입하는 것에 의해 형성할 수 있다. 이와 같이 하여 도 6c에 도시한 상태를 얻는다.

And the formation of the transistor, element isolation film, lower layer interlayer isolation film, the contact plug etc can use the publicly known technology. For example, the silicon dioxide film, and the phosphorous or the phosphorous and boron minor can form the doped silicon dioxide film as the lower layer interlayer isolation film as the impurity. And in the formation of contact plugs (66,67), it can form by purchasing the conductive material of the tungsten lamp. In this way, the state shown is obtained in the drawing 6c.

다음에, 도 6d에 도시한 바와 같이, 저유전율막(68)을 전체면에 형성한 후, 이 저유전율막(68)상에 산화 실리콘막, 질화 실

Next, as shown in Figure 6d, in case of the silicon dioxide film on this low-dielectric-layer (68) after doing

GF Exhibit 1124 - 2172/2704

리콘막, 질화 산화 실리콘막 또는 질화막계의 무기막(69)을 예를 들면 두께 100㎚ 정도로 성막한다.

the formation, in the total surface the low-dielectric-layer (68), the silicon nitride film, and the inorganic film (69) of the silicon oxynitride film or the nitride layer base deposit to about thickness 100㎚.

또한 이 성막은, 통상, 플라즈마 CVD(Chemical Vapour Deposition) 법이 사용되지만, 화원 분위기 하에서 수행하는 것이 바람직하다. 산화 분위기에서 CVD법을 사용하는 경우에는 저유전체 유기막이 산화되고, 막박리 등의 바람직하지 않은 현상을 야기시키는 우려가 있다.

Moreover, the ordinarily, and the plasma CVD (Chemical Vapour Deposition) method are applied. However it is the be desirable to perform under the flower garden mood. In the oxidizing atmosphere, the low-K dielectric organic layer is oxidized in case of using the chemical vapor deposition and it has the concern causing the phenomenon noting the be desirable paper including the film exfoliation etc.

에칭 조건으로서, 산화 실리콘막을 성막하는 경우에는 예를 들면, 플라즈마 CVD 장치를 사용하고 실란 가스 50sccm , N2O 가스 100sccm, 플라즈마 파워 500W, 압력 10 Torr, 온도 350℃의 조건으로 수행할 수 있다.

As the etching condition, in case of depositing the silicon dioxide film for example, the plasma CVD apparatus can be used and it can perform to the condition of the silane gas 50sccm , N 2 O gas 100sccm, plasma power 500W, pressure 10 Torr, temperature 350℃.

다음에 도 6e에 도시한 바와 같이, 전체면에 레지스트막(70)을 성막하고 배선 및 더미 배선을 형성하기 위한 더미 패터닝을 행한다. 더미 배선의 패터닝은 바람직하게는 최소한 3배 피치 이상의 배선 간격의 부분, 보다 바람직하게는 3배 피치 이상의 배선 간격의 부분에 있어서 모든 배선 간격이 1 ㎛ 이하로 되도록 수행한다.

Next, as shown in Figure 6e, the resist film (70) is deposited and wiring and the dummy patterning for forming the dummy line are performed in the total surface. Preferably, more preferably, the patterning of the dummy line all wiring spaces perform as to the part of the wiring space more than the treble pitch as as possible.

또한, 이 경우, 배선의 패터닝과 더미 배선의 패터닝을 반드시 동시에 행할 필요는 없다.

Moreover, in this case, the need to certainly simultaneously perform the patterning of wiring and patterning of the dummy line does not have.

다음에, 일반적인 마그네트론 방식의 에칭 장치를 사용하여 최상층의 산화 실리콘막(69) 및 그 하층의 저유전체막(68)을 에칭한다. 에칭은 예를 들면, 산화 실리콘막의 에칭의 경우는 예를 들면, C2F6 (14 sccm), CO (180 sccm), Ar (240 sccm), O2 (6 sccm) 가스를 사용하여 RF 플라즈마 파워 1500W로 수행할 수 있다. 또, 저유전체막의 에칭의 경우는 CHF3 (5 sccm), O2 (50 sccm), He (200 sccm) 가스를 이용하여 RF 플라즈마 파워 500W, -10℃의 조건으로 수행할 수 있다.

Next, the silicon dioxide film (69) of the top layer and low-k dielectric layer (68) of the lower layer are etched using the etching device of the general magnetron mode. The etching can perform in case of for example, the etching of the silicon dioxide film using for example, C 2 F 6 (14 sccm), the CO (180 sccm), the Ar (240 sccm), O 2 (6 sccm) gas to the RF plasma power 1500W. And in case of the etching of the low-k dielectric layer, it can perform using the CHF 3 (5 sccm), O 2 (50 sccm), and the He (200 sccm) gas to the RF plasma power 500 W, and the condition of -10℃.

상기 에칭에 있어서는, 상층의 산화 실리콘막(69)은 저유전체막(68)을 에칭할 때의 마스크의 역할도 완수한다. 즉, 저유전체막을 에칭하는 조건에서는 레지스트막(70)도 동시에 에칭된다. 또한, 본 실시예에서는 산화 실리콘막을 사용하지만 그 외, TiN, TiON, TaN, TaO, TaON, WN, W, Ti 등의 금속계 재료를 사용할 수도 있다.

It is in the etching and the silicon dioxide film (69) of the upper layer the role of the mask when etching accomplishes the low-k dielectric layer (68). That is, in the condition etching the low-k dielectric layer, the resist film (70) is etched at the simultaneously. Moreover, in the present preferred embodiment, the silicon dioxide film is used but the metallic type material of the besides, the TiN, the TiON, the TaN, the TaO, the TaON, WN, W, the Ti etc can be used.

다음에, 도 6f에 도시한 바와 같이, 다마신법에 의해 배선층(71) 및 더미 배선층(72)을 형성한다. 이와 같이 하여 형성되는 배선층(71) 및 더미 배선층(72)의 상면은, 저유전율막(68)의 상면보다도 높게 형성된다.

Next, as shown in Figure 6f, the wiring layer (71) and dummy wiring layer (72) are formed with the damascene method. In this way, the upper side of the dummy wiring layer (72) and the formed wiring layer (71) is formed longer than the upper side of the low-dielectric-layer (68).

즉, 배선층의 형성은 스퍼터링 장치 또는 CVD 장치를 사용하고 배선 재료(금속)로서 예를 들면, 동을 전체면에 퇴적시키고, 이어서 CMP법에 의해 여분의 금속막을 연마한 후, 다시 CMP법에 의해 50㎚ 정도의 무기막(산화 실리콘막)(69)을 연마하

That is, the formation of the wiring layer uses the sputtering device or the performing apparatus and for example, the copper is sedimented on the total surface as the wiring material (metal) and subsequently after t

GF Exhibit 1124 - 2173/2704

는 것에 의해 행해진다. 이 연마는 완전히 금속을 제거하기 위함과, 산화 실리콘막에 새겨진 스크래치를 제거하기 위하여 수행하는 것이다.

he extra metal layer is polished with the CMP law it is performed by again polishing the inorganic film (silicon dioxide film) (69) of about 50㎚ with the CMP law. It performs the scratch carved in the silicon dioxide film is removed it is that this grinding completely removes the metal.

다음에, 산화 실리콘막(69)을 일반적인 마그네트론 방식의 에칭 장치를 사용하여 에칭한다. 이 때의 조건으로서는 예를 들면, C2F6 (14 sccm), CO (180 sccm), Ar (240 sccm)을 사용할 수 있다. 이러한 조건에서는 유전체 유기막은 거의 에칭되지 않는다. 또한, 장치 성능보다도 신뢰성을 중시하는 경우에는 이 산화 실리콘막의 제거 공정을 생략할 수 있다.

Next, the silicon dioxide film (69) is etched using the etching device of the general magnetron mode. For example, C 2 F 6 (14 sccm), the CO (180 sccm), and the Ar (240 sccm) can be used as the condition at this time. In such condition, the dielectric organic layer is not etched at the nearly. Moreover, the removal process of the silicon dioxide film can be omitted in case of considering the reliability more than the hardware performance.

이와 같이 하여 얻어지는 배선 구조는, 더미 배선층 이외에 더미 배선층에 접속하는 더미 콘택트 플러그를 가짐으로써, 더욱 더 방열 효과가 높아진다. 따라서 신뢰성이 매우 높은 배선 구조를 가지는 반도체 장치이다.

In this way, it has the dummy contact plug in which the wiring structure of being obtained connects to the dummy wiring layer besides the dummy wiring layer. In that way the thermal performance is more and more enhanced. Therefore, it is the semiconductor device in which the reliability has very high wiring structure.

제7 실시예

Seventh embodiment .

본 실시예에서는 2층의 배선 구조를 가지고, 더미 배선층 및 더미 콘택트홀(더미 비아 콘택트홀 및 비아 콘택트홀)을 가지는 반도체 장치의 제조예이다.

In the present preferred embodiment, it is the manufacturing example of the semiconductor device for having the dummy wiring layer and dummy contact hole (the dummy via contact hole and via contact hole) with the wiring structure of 2 layer.

먼저, 상기 제6 실시예와 동일하게 하여 도 6f에 도시한 상태를 얻는다. 다음에, 상기 배선층(71) 및 더미 배선층(72)상에 두께 100㎚ 이상의 얇은 질화 실리콘막, 산화 실리콘막 또는 질화 산화 실리콘막 등의 도시하지 않은 무기막을 형성한다. 이 막은, 비아 콘택트홀 형성시에 에칭 스톱퍼(stopper) 층으로서 사용되기 때문에, 가능한 만큼 얇은 것이 바람직하다. 본 실시예에서는 예를 들면 질화 실리콘막을 두께 100㎚로 형성한다.

In advance, it makes identical with the sixth preferred embodiment and the state shown is obtained in the drawing 6f. Next, the inorganic film not shown including the thin silicon nitride film more than the thickness 100㎚, the silicon dioxide film or the silicon oxynitride film etc. is formed on the wiring layer (71) and dummy wiring layer (72). This film is the thing it is used and therefore thin as much as it is possible. Is the be desirable as the etching stopper layer in the via contact hole formation. In the present preferred embodiment, for example, the silicon nitride film is formed into the thickness 100㎚.

다음에, 도 7a에 도시한 바와 같이, 제2의 도전체막(73)을 전체면에 형성한다. 본 실시예에서는 이 저유전체막(73)으로서 상기 열거한 것 외에, 비교적 유전율이 높은 유기 SOG막, 플루오린 도프드 실리콘 산화막 등을 사용하는 것도 가능하다. 이 제2의 저유전체막(73)은 일반적으로 시판되는 CVD 장치 또는 SOG 코터(coater) 장치를 사용하고, 공지의 기술을 사용하여 형성할 수 있다.

Next, as shown in Figure 7a, the second conductor film (73) is formed on the total surface. In the present preferred embodiment, it enumerates as this low-k dielectric layer (73) with the above. Besides it is possible to use the organic spin on glass film, in which the relative dielectric constant is high the fluorine doped silicon oxide film etc. The performing apparatus or the SOG cotter (coater) apparatus in which generally the low-k dielectric layer (73) of this second comes into the market is used and it can form using the publicly known technology.

다음에, 상기 제2의 저유전체막(73)상에, 실리콘 산화막, 질화 산화 실리콘막 또는 질화 실리콘막 등의 무기막(74)을 성막한다. 이러한 막은 일반적으로는 CVD 장치를 사용하여 성막할 수 있지만, SOG 코터, 진공 증착, 스퍼터링 장치를 사용할 수 있다. 이 무기막(74)은 배선층을 패터닝 후의 에칭할 때의 스톱퍼로서 작용한다.

Next, the inorganic film (74) including the silicon oxide film, the silicon oxynitride film or the silicon nitride film etc. is deposited on the second low-k dielectric layer (73). Such film generally can deposit using the performing apparatus. However the SOG cotter, the vacuum evaporation, and the sputtering device can be used. This inorganic film (74) acts the wiring layer as the stopper when etching after the patterning.

GF Exhibit 1124 - 2174/2704

다음에, 전체면에 레지스트막(75)을 성막한 후, 비아 콘택트 및 더미 비아 콘택트 형성을 위한 패터닝을 수행한다. 이 때, 더미 비아 콘택트홀의 형성은 상하에 더미 배선이 형성되는 곳에 최소 피치로 수행하는 것이 바람직하다.

Next, the resist film (75) the patterning for the via contact and dummy via contact formation is performed in the total surface after doing the deposition. Then, it is the be desirable that the formation of the dummy via contact hole performs in the place where the dummy li ne is formed in top and bottom to the minimum feature of pitch.

다음에, 무기막(74) 및 제2의 저유전율막(73)을 에칭하고 비아 콘택트홀 및 더미 비아 콘택트홀을 형성하는 것에 의해, 도 7b에 도시한 상태를 얻는다. 무기막(74) 및 제2의 저유전율막(73)의 에칭은 상술한 무기막 및 저유전율막의 에칭 조건과 동일하게 하여 수행할 수 있다. 그 때에는 레지스트막(75)도 동시에 에칭 제거된다.

Next, the inorganic film (74) and the second low-dielectric-layer (73) are etched and the via contact hol e and dummy via contact hole are formed. Accordingly the state shown is obtained in the drawing 7b. It make s identical with the etching condition of the low-dielect ric-layer and the above-described inorganic film and th e etching of the second low-dielectric-layer (73) and in organic film (74) can perform. In the then, the simultan eously the resist film (75) is etching-removed.

그 후, 동 등의 금속 배선 재료를 상기 비아 콘택트홀 및 더미 비아 콘택트홀에 매입하고, 비아 콘택트 플러그(74) 및 더미 비아 콘택트 플러그(75)를 형성하는 것에 의하여 도 7c에 도시한 상태도를 얻는다.

Thereafter, the metal wiring material of the equivalent is purchased in the via contact hole and dummy via co ntact hole and it is according to form the via contact p lug (74) and dummy via contact plug (75) and the phas e diagram shown is obtained in the drawing 7c.

다음에, 전체면에 제3의 저유전율막(78)을 형성한다. 형성 방법은, 상기 제2의 저유전체막과 동일하다. 또한, 상기 제3의 저유전체막(78)상에 실리콘 산화막, 질화 산화 실리콘막 또는 질화 실리콘막 등의 무기막(79)을 성막하는 것에 의해 도7d에 도시한 상태도를 얻는다. 이러한 막은, 일반적으로는 CVD 장치를 사용하여 성막할 수 있지만, SOG 코터, 진공 증착, 스퍼터링 장치를 사용할 수도 있다. 이 무기막(79)은 배선층을 CMP법에 의해 연마할 때의 스톱퍼로서 작용한다.

Next, the third low-dielectric-layer (78) is formed on the total surface. The formation method is identical wit h the second low-k dielectric layer. Moreover, by depo siting the inorganic film (79) including the silicon oxide f ilm, the silicon oxynitride film or the silicon nitride film e tc. on the third low-k dielectric layer (78) the phase di agram shown is obtained in the drawing 7d. It generally can deposit using the performing apparatus. However s uch film can use the SOG cotter, the vacuum evaporati on, and the sputtering device. It acts as the stopper w hen this inorganic film (79) polishes the wiring layer wit h the CMP law.

다음에, 도 7e에 도시한 바와 같이, 전체면에 레지스트막(80)을 성막한 후, 배선층 및 더미 배선층 형성을 위한 패터닝을 수행한다. 더미 배선층의 패터닝은 배선 간격이 최소 피치 이상인 곳에 형성하는 것이 바람직하다. 더미 패턴을 설계 최소치법으로 형성한 경우에, 더미 배선층과 배선층과의 간격이 최소 피치 이상으로 하기 위한 것이다. 또한, 성능을 중시하는 경우에 있어서는 그 간격을 최소 간격 보다도 2배 이상으로 해 놓는 것이 보다 바람직하다. 배선 간격을 2배 이상으로 하는 것에 의하여 배선간의 용량을 대략 반분할 수 있게 된다.

Next, as shown in Figure 7e, the resist film (80) the patterning for the wiring layer and dummy wiring layer f ormation is performed in the total surface after doing t he deposition. It is the be desirable that the patterning of the dummy wiring layer forms on the place where th e wiring space is the minimum feature of pitch or great er. In case the dummy pattern is formed into the desig n minimum value method it is that the gap between the dummy wiring layer and the wiring layer are called over the minimum feature of pitch. Moreover, it more is the be desirable to decide on the gap than the minimum sp ace over two times in case of taking very seriously the efficiency. It is according to the wiring space over two times and capacity between wiring is approximately hal ved.

다음에, 일반적인 마그네트론 방식의 에칭 장치를 사용하여 최상층의 무기막(77) 및 그 하층의 제3의 저유전체막(78)을 에칭한다. 이 에칭은 예를 들면, 저유전체막의 경우는 CHF3 (5 sccm), O2 (50 sccm), He (200 sccm) 가스를 이용하여 RF 플라즈마 파워 500W, -10℃로 수행할 수 있다. 또, 무기막(산화 실리콘막)의 경우는, 예를 들면, C2F6 (14 sccm), CO (180 sccm), Ar (240 sccm), O2 (6 sccm) 가스를 이용하여 RF 플라즈마 파워 1500W로 에칭을 수행할 수 있다.

Next, the inorganic film (77) of the top layer and the third low-k dielectric layer (78) of the lower layer are e tched using the etching device of the general magnetr on mode. This etching can perform in case of for exam ple, the low-k dielectric layer to the CHF 3 (5 sccm), O 2 (50 sccm), the RF plasma power 500W using the He (200 sccm) gas, and -10℃. And in case of the inorgani c film (silicon dioxide film), the etching can be performe d using C 2 F 6 (14 sccm), the CO (180 sccm), the Ar (240 sccm), O 2 (6 sccm) gas to the RF plasma power 1500W for example.

GF Exhibit 1124 - 2175/2704

이 경우, 상층의 무기막(79)은 제3의 저유전체막(78)을 에칭할 때의 마스크로도 된다. 즉, 제3의 저유전체막을 에칭하는 조건에서는 레지스트막980)도 동시에 에칭된다. 또한, 본 실시예에서는 산화 실리콘막 등의 무기막을 사용하지만, TiN, TiON, TaN, TaO, TaON, WN, W, Ti 등의 다른 금속막을 사용할 수도 있다.

In this case, it consists of the mask when the inorganic film (79) of the upper layer etches the third low-k dielectric layer (78). That is, in the condition etching the third low-k dielectric layer, the resist film 980) is etched at the simultaneously. Moreover, in the present preferred embodiment, the inorganic film including the silicon dioxide film etc. is used. However the dissimilar metal layer of the TiN, the TiON, the TaN, the TaO, the TaON, WN, W, the Ti etc can be used.

또, 이 때 더미 콘택트의 패터닝을 수행하지 않고, 배선층을 형성한 후, 더미 콘택트홀 형성을 위한 패터닝을 수행하고, 그곳에 열전도성이 높은 산화 실리콘막, 질화 실리콘막, 질화 산화 실리콘막 등을 형성할 수 있다.

And the patterning of the dummy contact is not then performed and the wiring layer the patterning for the dummy contact making hole is performed after doing the formation and the silicon dioxide film, in which the thermal conductance is there high the silicon nitride film, the silicon oxynitride film etc. can be formed.

다음에, 다마신법에 의해 배선층(81) 및 더미 배선층(82)을 형성한다. 즉, 배선 재료(금속)로서 예를 들면, 동을 스퍼터링 장치 또는 CVD 장치로 형성하고 이어서, CMP법에 의해 여분의 금속막을 연마한다. 최후에 다시 CMP법에 의해 50㎚ 정도의 무기막(79)을 연마한다. 무기막을 다시 연마하는 것은, 완전하게 여분의 금속을 제거하는 것과 무기막(산화 실리콘막 등)에 새겨진 스크래치를 제거하기 위한 것이다.

Next, the wiring layer (81) and dummy wiring layer (82) are formed with the damascene method. That is, it forms and subsequently for example, the copper the extra metal layer is polished as the wiring material (metal) to the sputtering device or the performing apparatus with the CMP law. The inorganic film (79) of about 50㎚ is again polished in the last with the CMP law. The scratch carved in the inorganic film (the silicon dioxide film etc) perfect it removes the extra metal is to be removed to again polish the inorganic film.

이러한 방법으로, 도 7f에 도시한 바와 같은 2층의 배선층, 더미 배선층, 콘택트홀 및 더미 콘택트홀을 가지는 다층 배선 구조를 형성할 수 있다. 이 때, 배선층(81) 및 더미 배선층(82)의 상면의 높이는 제3의 저유전율막(78)의 상면의 높이 보다 높게 형성된다.

In this way, the wiring layer like showing of 2 layer, the dummy wiring layer, and the contact hole and the multi-layer interconnection structure of owning the dummy contact hole can be formed on the drawing 7f. Then, the height of the upper side of the wiring layer (81) and dummy wiring layer (82) are high formed than the height of the upper side of the third low-dielectric-layer (78).

또한, 이상의 조작을 반복하는 것에 의해 3층 이상의 다층 배선 구조도 동일하게 하여 형성할 수 있다.

Moreover, by repeating the operation described in the above it makes identical and it can form.

이와 같이 하여 얻어지는 배선 구조는, 더미 배선층 이외에 더미 콘택트 플러그를 가짐으로써, 더욱더 방열 효과가 높아진다. 따라서, 신뢰성이 높은 다층 배선 구조를 가지는 반도체 장치를 얻을 수 있다.

In this way, the wiring structure of being obtained has the dummy contact plug besides the dummy wiring layer. In that way the thermal performance is more and more enhanced. Therefore, the semiconductor device for having the multi-layer interconnection structure where the reliability is high can be obtained.

또한, 상기 실시예에서는 배선층 또는 콘택트홀(콘택트홀 또는 비아 콘택트홀) 형성을 위한 패터닝과 동시에 더미 배선층 또는 더미 콘택트홀 형성을 위한 패터닝을 동시에 수행하는 예를 나타낸다. 본 발명에 있어서는 배선층 또는 콘택트홀을 형성한 후에, 더미 배선층 또는 더미 콘택트홀을 형성하는 것을 수행하는 것도 가능하다.

Moreover, in the above preferred embodiment, the old times which simultaneously simultaneously performs the patterning for the dummy wiring layer or the dummy contact making hole with the patterning for the wiring layer or the contact hole (the contact hole or the via contact hole) formation is indicated. After it is in the invention and the wiring layer or the contact hole is formed it is possible to perform forming the dummy wiring layer or the dummy contact hole.

예를 들면, 배선층을 형성한 후에 더미 배선층을 형성하는 것은 다음과 같이 행할 수 있다.

For example, it can perform like the next to form the dummy wiring layer after the wiring layer is formed.

먼저, 도 8a에 도시한 바와 같이, 접속 플러그(85) 및 배선층(84)을 형성한 구조를 얻은 다음, 도 8b에 도시한 바와 같이,

In advance, as shown in Figure 8a, after the structure of forming the adapter plug (85) and wiring layer (84) i

GF Exhibit 1124 - 2176/2704

산화 실리콘막 등의 무기막(89)을 전체면에 형성한 후, 레지스트막(89)을 성막하고 더미 배선층 형성을 위한 패터닝을 수행한다.

s obtained the resist film (89) is deposited and as show n in Figure 8b, the inorganic film (89) including the silic on dioxide film etc. the patterning for the dummy wiring layer formation is performed in the total surface after d oing the formation.

그 후, 일반적인 마그네트론 방식의 에칭 장치를 사용하여 상기 무기막(89)을 예를 들면, C2F6 (14 sccm), CO (180 sccm), Ar (240 sccm), O2 (6 sccm) 가스를 이용하여 RF 플라즈마 파워 1500W로 에칭한다. 또, 상기 유전체막(유전체 유기막)(86)을 CHF3 (5 sccm), O2 (50 sccm), He (200 sccm) 가스를 이용하여 RF 플라즈마 파워 500W, -10℃의 조건으로 에칭한다.

Thereafter, it etches in case of the inorganic film (89) using the etching device of the general magnetron mod e to the RF plasma power 1500W using C 2 F 6 (14 scc m), the CO (180 sccm), the Ar (240 sccm), O 2 (6 scc m) gas. And the dielectric film (dielectric organic layer) (86) is etched to the RF plasma power 500W, and the condition of -10℃ using the CHF 3 (5 sccm), O 2 (50 sc cm), and the He (200 sccm) gas.

그 후, 더미 패턴을 CVD 또는 SOG 코터를 사용하여 산화 실리콘막, 질화 실리콘막 또는 질화 산화 실리콘막을 형성하여 매입한다. 산화 실리콘막, 질화 실리콘막 또는 질화 산화 실리콘막은 열전도성에 뛰어나다. 다음에, 절연막 연마용인 CMP 장치를 사용하여 실리카계 슬러리 또는 산화 세륨(cerium) 슬러리를 사용하여 연마하여 도 8c에 도시한 구조를 얻는다. 이 경우도 배선층(84) 및 더미 배선층(90)의 상면은 저유전율막(86)의 상면보다도 무기막(88)의 높이만큼 높게 형성된다.

Thereafter, the silicon dioxide film, and the silicon nitride film or the silicon oxynitride film are formed using CVD or the SOG cotter and the dummy pattern is purch ased. The silicon dioxide film , and the silicon nitride fil m or the silicon oxynitride film are excellent in the ther mal conductance. Next, it polishes using the silica-base d slurry or the cerium oxide slurry and the illustrated st ructure is obtained in the drawing 8c using the insulatin g layer grinding tolerant chemical mechanical polishing apparatus. In this case, the upper side of the dummy wiring layer (90) and wiring layer (84) is high formed th an the upper side of the low-dielectric-layer (86) as th e height of the inorganic film (88).

또한, 본 실시예에서는 저유전율막으로서 유전체 유기막을 사용하지만, 크세로겔을 사용하는 경우에도 본 발명의 소기의 효과를 이루는 구조를 얻을 수 있다. 그 경우의 에칭 조건으로서는 상기 무기막의 에칭 조건과 동일하다.

Moreover, in the present preferred embodiment, the dielectric organic layer is used as the low-dielectric-lay er. However the structure of being comprised the effec t of the one's expectation of the invention even in cas e of using the xerogel can be obtained. It is identical w ith the etching condition of the inorganic film as the et ching condition of the case.

도면에 대한 간단한 설명

Brief explanation of the drawing

도 1은 본 발명인 반도체 장치의 제1 실시예를 도시한 도면이고,

Figure 1 is a drawing showing the first preferred embodiment of the semiconductor device which is the i nvention.

도 2a 내지 도 2f는 본 발명의 제2 실시예에 따른 반도체 장치의 제조 방법의 주요부분을 나타내는 단면도이고, 여기서,

Here, it is the cross-sectional view in which the figures 2a through 2f shows the main part of the manufacturin g method of the semiconductor device according to th e second preferred embodiment of the present inventio n.

도 2a는 실리콘 반도체 기판 상에 산화 실리콘막을 형성한 도면이고,

It is drawing in which the drawing 2a forms the silicon dioxide film on the silicon semiconductor substrate.

도 2b는 p웰 영역을 형성한 도면이고,

It is drawing in which the drawing 2b forms the p well domain.

도 2c는 p웰 영역을 형성한 후, 소자 분리 영역을 형성하기 위한 패터닝을 수행한 도면이고,

The drawing 2c is the p well domain drawing performing the patterning for forming the element isolation region after doing the formation.

도 2d는 소자 분리 영역을 형성하기 위한 패터닝을 수행한 후, 로코스(LOCOS)법에 따라, 소자 분리막을 형성한 도면이고,

It is the patterning in which the drawing 2d forms the element isolation region drawing forming the element is olation film after doing the performance according to th e LOCOS method.

도 2e는 산화 실리콘막을 형성한 후, 게이트 전극을 형성하고, n+ 영역과 p+영역을 형성한 도면이고,

The drawing 2e forms the gate electrode the silicon dioxide film after doing the formation and it is the n+ d omain and drawing forming the p+ domain.

도 2f는 n+ 영역과 p+ 영역을 형성한 후, 전체면에 저유전율막을 형성한 도면이고,

The drawing 2f is the n+ domain and p+ domain drawing forming the low-dielectric-layer on the total su rface after doing the formation.

도 2g는 전체면에 저유전율막을 형성한 후, 산화 실리콘막을

The drawing 2g forms the silicon dioxide film the low-

GF Exhibit 1124 - 2177/2704

형성하고, 배선층을 형성하기 위한 패터닝을 수행한 도면이고,

dielectric-layer on the total surface after doing the for mation and it is drawing performing the patterning for f orming the wiring layer.

도 2h는 배선층을 형성하기 위한 패터닝을 수행한 후, 포토 에칭으로 배선홈과 콘택트홀을 형성한 도면이고,

It is the patterning in which the drawing 2h forms the wiring layer drawing forming the interconnection groove and contact hole into the photo- etching after doing th e performance.

도 2i는 배선층을 형성하기 위한 패터닝을 수행한 후, 포토 에칭으로 배선홈과 콘택트홀을 형성하고, 알루미늄을 전체면에 퇴적시키고, CMP법에 의해 배선을 형성한 도면이고,

The patterning in which the drawing 2i forms the wiring layer the interconnection groove and contact hole is fo rmed after doing the performance into the photo- etchi ng and aluminum is sedimented on the total surface an d it is drawing forming wiring with the CMP law.

도 2j는 배선을 형성한 후, 전체면에 패시베이션막을 형성한 도면이다.

The drawing 2j is wiring drawing forming the passivation film on the total surface after doing the for mation.

도 3a 내지 도 3f는 본 발명의 제3 실시예에 따른 반도체 장치의 제조 방법의 주요 부분을 나타내는 단면도이고, 여기서,

Here, it is the cross-sectional view in which the figures 3a through 3f shows the main part of the manufacturin g method of the semiconductor device according to th e third preferred embodiment of the present invention.

도 3a는 실리콘 반도체 기판 상에 산화 실리콘막을 형성하고, 그 위에 저유전율막을 형성하고, 다시 그 위에 산화 실리콘막을 형성한 도면이고,

The drawing 3a forms the silicon dioxide film on the silicon semiconductor substrate and the low-dielectric-l ayer is formed on the upper part and it is drawing whic h again forms the silicon dioxide film on the upper part.

도 3b는 산화 실리콘막을 형성한 후 레지스트막을 이용하여 배선을 위한 패터닝을 수행한 도면이고,

It is drawing in which the drawing 3b performs the patterning for wiring the silicon dioxide film after doing the formation using the resist film.

도 3c는 배선을 위한 패터닝을 수행한 후, 포토 에칭으로 콘택트홀을 형성한 도면이고,

The drawing 3c is the patterning for wiring drawing forming the contact hole into the photo- etching after doing the performance.

도 3d는 콘택트홀을 형성한 후, 전체면에 동을 퇴적한 도면이고,

The drawing 3d is the contact hole drawing accumulating the copper in the total surface after doin g the formation.

도 3e는 동을 퇴적한 후, CMP법에 의해 배선층을 형성한 도면이고,

The drawing 3e is the copper drawing forming the wiring layer with the CMP law after doing the depositio n.

도 3f는 패시베이션막으로서 저유전율막을 형성한 도면이다.

The drawing 3f is drawing forming the low-dielectric-layer as the passivation film.

도 4a 내지 도 4i는 본 발명의 제4 실시예에 따른 반도체 장치의 제조 방법의 주요 부분을 나타내는 단면도이고, 여기서,

Here, it is the cross-sectional view in which the figures 4a through 4i shows the main part of the manufacturin g method of the semiconductor device according to th e fourth preferred embodiment of the present inventio n.

도 4a는 실리콘 반도체 기판 상에 산화 실리콘막을 형성하고, 저유전율막을 형성한 후, 배선과 더미 배선을 형성하고, 제2 저유전율막을 형성한 도면이고,

The drawing 4a forms the silicon dioxide film on the silicon semiconductor substrate and the low-dielectric-l ayer wiring and dummy line is formed after doing the fo rmation and it is drawing forming the second low-dielec tric-layer.

도 4b는 제2 저유전율막을 형성한 후, 레지스트를 사용하여 포토 에칭법에 의해 콘택트홀을 형성한 도면이고,

The drawing 4b is the second low-dielectric-layer drawing forming the contact hole using the resist with the photo etching method after doing the formation.

도 4c는 콘택트홀을 형성한 후, 해당 콘택트홀에 금속(W)을 매입한 도면이고,

The drawing 4c is the contact hole drawing purchasing the metal (W) in the corresponding contact hole after doing the formation.

도 4d는 콘택트홀에 금속(W)을 매입한 후, 전체면에 질화 실리콘막을 형성한 도면이고,

It is drawing in which the drawing 4d forms the silicon nitride film the metal (W) on the contact hole after doi ng the bury on the total surface.

도 4e는 질화 실리콘막을 형성한 후, 레지스트를 사용하여 제2 배선층을 형성하기 위한 패터닝을 수행한 도면이고,

The drawing 4e is the silicon nitride film drawing performing the patterning for forming the second wiring layer using the resist after doing the formation.

도 4f는 제2 배선층을 형성하기 위한 패터닝을 수행한 후, 포토 에칭에 의해 제2 배선층을 형성한 도면이고,

It is the patterning in which the drawing 4f forms the second wiring layer drawing forming the second wiring l ayer with the photo- etching after doing the performan ce.

도 4g는 제2 배선층을 형성한 후, 전체면에 알루미늄막을 형성한 도면이고,

The drawing 4g is the second wiring layer drawing forming the aluminium film on the total surface after doi ng the formation.

GF Exhibit 1124 - 2178/2704

도 4h는 전체면에 알루미늄막을 형성한 후, CMP법에 의해 제2 금속배선을 형성한 도면이고,

The drawing 4h is the aluminium film drawing forming the second metal wiring with the CMP law in the total s urface after doing the formation.

도 4i는 제2 금속배선을 형성한 후, 패시베이션막을 형성한 도면이다.

The drawing 4i is the second metal wiring drawing forming the passivation film after doing the formation.

도 5a 내지 도 5f는 본 발명의 제5 실시예에 따른 반도체 장치의 제조 방법의 주요 부분을 나타낸 단면도이고, 여기서,

Here, it is the cross-sectional view in which the figures 5a through 5f shows the main part of the manufacturin g method of the semiconductor device according to th e fifth preferred embodiment of the present invention.

도 5a는 반도체 기판 상에 콘택트 플러그를 형성한 후, 저유전율막을 형성한 도면이고,

The drawing 5a is the contact plug drawing forming the low-dielectric-layer on the semiconductor substrate aft er doing the formation.

도 5b는 제1 배선층을 형성하고, 그 위에 무기막을 형성한 도면이고,

The drawing 5b forms the first interconnection layer and it is drawing forming the inorganic film on the upper part.

도 5c는 제2 저유전율막을 형성한 도면이고,

It is drawing in which the drawing 5c forms the second low-dielectric-layer.

도 5d는 제2 저유전율막(유기막) 내에 제2 콘택트홀 형성한 도면이고,

It is drawing which the drawing 5d forms the second contact hole within the second low-dielectric-layer (or ganic layer).

도 5e는 크세로겔을 함유하는 막을 형성한 후, 제2 배선층을 형성한 도면이고,

Figure 5e is drawing forming the second wiring layer the film after doing the formation containing the xeroge l.

도 5f는 패시베이션막을 형성한 도면이다.

It is drawing in which the drawing 5f forms passivation film.

도 6a 내지 도 6f는 본 발명의 제6 실시예에 따른 반도체 장치의 제조 방법의 주요 부분을 나타낸 단면도이고, 여기서,

Here, it is the cross-sectional view in which the figures 6a through 6f shows the main part of the method for m anufacturing semiconductor device according to the six th preferred embodiment of the invention.

도 6a는 반도체 기판 상에 소자 분리막을 형성하고, 층간 절연막을 형성한 도면이고,

The drawing 6a forms the element isolation film on the semiconductor substrate and it is drawing forming the i nter-layer insulating film.

도 6b는 전체면에 레지스트막을 형성하고, 콘택트홀 및 더미 콘택트홀을 형성하기 위한 패터닝을 수행한 도면이고,

The drawing 6b forms the resist film on the total surface and it is drawing performing the contact hole a nd the patterning for forming the dummy contact hole.

도 6c는 금속 재료를 채워서 콘택트 플러그 및 더미 콘택트 플러그를 형성한 도면이고,

The drawing 6c fills up the metal material and it is the contact plug and drawing forming the dummy contact p lug.

도 6d는 저유전율 유기막을 형성하고, 그 위에 무기막을 형성한 도면이고,

The drawing 6d forms the low permittivity organic layer and it is drawing forming the inorganic film on the upper part.

도 6e는 전체면에 레지스트막을 형성한 후, 제1 배선층 및 더미 배선층을 형성하기 위한 패터닝을 수행한 도면이고,

The drawing 6e is the resist film drawing performing the patterning for forming the first interconnection layer an d dummy wiring layer in the total surface after doing th e formation.

도 6f는 제1 배선층을 형성한 도면이다.

It is drawing in which the drawing 6f forms the first interconnection layer.

도 7a 내지 도 7f는 본 발명의 제7 실시예에 따른 반도체 장치의 제조 방법의 주요 부분을 나타낸 단면도이고,

Figures 7a through 7f are the cross-sectional view showing the main part of the manufacturing method of the semiconductor device according to the seventh pre ferred embodiment of the present invention.

도 7a는 제2 저유전율막을 형성한 도면이고,

It is drawing in which the drawing 7a forms the second low-dielectric-layer.

도 7b는 무기막을 형성한 후, 전체면에 레지스트막을 형성한 후, 비아 콘택트홀 및 더미 비아 콘택트홀을 형성하기 위한 패터닝을 수행한 도면이고,

It is drawing performing the patterning in which the drawing 7b forms the via contact hole and dummy via c ontact hole the resist film the inorganic film after doing the formation on the total surface after doing the form ation.

도 7c는 비아 콘택트 플러그 및 더미 비아 콘택트 플러그를 형성한 도면이고,

The drawing 7c is the via contact plug and drawing forming the dummy via contact plug.

도 7d는 제3 저유전율막을 형성하고, 그 위에 무기막을 형성한 도면이고,

The drawing 7d forms the third low-dielectric-layer and it is drawing forming inorganic film on the upper part.

도 7e는 레지스트막을 형성한 후, 제2 배선층 및 더미 배선층을 형성하기 위한 패터닝을 수행한 도면이고,

The drawing 7e is the resist film drawing performing the second wiring layer and the patterning for forming the dummy wiring layer after doing the formation.

도 7f는 제2 배선층 및 더미 배선층을 형성한 도면이다.

The drawing 7f is the second wiring layer and drawing

GF Exhibit 1124 - 2179/2704

forming the dummy wiring layer.

도 8a 내지 도 8c는 본 발명의 제8 실시예에 따른 반도체 장치의 제조 방법의 주요 부분을 나타낸 단면도이고, 여기서,

Here, it is the cross-sectional view in which the figures 8a through 8c shows the main part of the manufacturing method of the semiconductor device according to the eighth preferred embodiment of the present invention.

도 8a는 제1 배선층을 형성한 도면이고,

It is drawing in which the drawing 8a forms the first interconnection layer.

도 8b는 무기막을 형성한 후, 전체면에 레지스트막을 형성하고, 더미 배선층을 형성하기 위한 패터닝을 수행한 도면이고,

The drawing 8b forms resist film inorganic film after doing the formation on the total surface and it is drawing performing the patterning for forming the dummy wiring layer.

도 8c는 더미 배선층을 형성한 도면이다.

It is drawing in which the drawing 8c forms the dummy wiring layer.

도 9는 더미 리드선과 금속 리드선을 가지는 종래의 반도체 장치의 단면도이다.

Figure 9 is a cross-sectional view of the conventional semiconductor device having the dummy read line and metal lead line.

[부호의 설명]

[The description of reference numerals]

1, 13,30,37,50,62,81,87 : 반도체 기판

1, 13,30,37,50,62,81,87: semiconductor substrate.

2, 19, 63, 82 : 소자 분리막, 3: 게이트 절연막, 4, 21 : 게이트 전극,

2, 19, 63, 82: element isolation film 3: gate insulating layer 4, 21: gate electrode.

5, 9, 24, 29, 32, 36, 39, 41, 53, 57, 68, 73, 78, 94 : 저유전율막

5, 9, 24, 29, 32, 36, 39, 41, 53, 57, 68, 73, 78, 94: low-dielectric-layer.

6, 8, 11, 28, 35, 40, 48, 54, 60, 71, 81, 85, 91 : 배선층

6, 8, 11, 28, 35, 40, 48, 54, 60, 71, 81, 85, 91: wiring layer.

7, 10, 27, 44, 52, 58, 66, 76, 84 : 콘택트홀

7, 10, 27, 44, 52, 58, 66, 76, 84: contact hole.

12, 49, 61 : 패시베이션막, 14, 20, 25, 31, 33, 38 : 산화 실리콘막

12, 49, 61: passivation film 14, 20, 25, 31, 33, 38: silicon dioxide film.

15, 18, 26, 34, 43, 46, 65, 70, 75, 80, 89 : 레지스트막

15, 18, 26, 34, 43, 46, 65, 70, 75, 80, 89: resist film.

16 : p웰, 17, 45 : 질화 실리콘막, 22 : p+ 영역 23 : n+ 영역

16: p well 17, 45: silicon nitride film 22: p+ domain 23: n+ domain.

42, 72, 82, 90 : 더미 배선층, 47 : 알루미늄막, 51 : 절연막

42, 72, 82, 90: dummy wiring layer 47: aluminium film 51: insulating layer.

59 : 크세로겔을 함유하는 막, 3#39#, 64, 74, 79 : 무기막, 92 : 기판

59: the film containing the xerogel, and 3' 64, 74, 79: inorganic film 92: substrate.

93 : 더미 리드선, 94 : 금속 리드선, 95 : 전열층

93: dummy read line 94: metal lead line 95: electrothermal layer.

96 : 저유전율재료, 97 : 전열성 절연층

96: low dielectric constant material 97: property of transferring heat insulating layer.

Disclaimer

본 문서는 특허 및 과학기술문헌 전용의 첨단 자동번역 시스템을 이용해 생성되었습니다. 따라서 부분적으로 오역의 가능성이 있으며, 본 문서를 자격을 갖춘 전문 번역가에 의한 번역물을 대신하는 것으로 이용되어서는 안 됩니다. 시스템 및 네트워크의 특성때문에 발생한 오역과 부분 누락, 데이터의 불일치등에 대하여 본원은 법적인 책임을 지지 않습니다. 본 문서는 당사의 사전 동의 없이 권한이 없는 일반 대중을 위해 DB 및 시스템에 저장되어 재생, 복사, 배포될 수 없음을 알려드립니다.

(The document produced by using the high-tech machine translation system for the patent and science & technology literature. Therefore, the document can include the mistranslation, and it should not be used as a translation by a professional translator. We hold no legal liability for inconsistency of mistranslation, partial omission, and data generated by feature of system and network. We would like to inform you that the document cannot be regenerated, copied, and distributed by being stored in DB and system for unauthorized general public without our consent.)

(19) 대한민국특허청(KR)
(12) 공개특허공보(A)

(11) 공개번호 특2000-0025576
(43) 공개일자 2000년05월06일

(51) 국제분류코드
H01L 27/08 (2006.01)

(21) 출원번호 10-1998-0042717

(22) 출원일자 1998년10월13일

(71) 출원인
윤종용
삼성전자 주식회사
경기도 수원시 팔달구 매탄3동 416, 대한민국

(72) 발명자
이조원
경기도 수원시 팔달구 매탄동 현대아파트 101동 104호, 대한민국
김정우
경기도 성남시 분당구 분당동 38 샛별우방아파트 306동 605호V, 대한민국
김병만
경기도 안양시 만안구 박달동 금호타운아파트 103동 1802호, 대한민국
김문경
서울특별시 송파구 풍납동 507 동아한가람아파트 102동 1405호, 대한민국

(74) 대리인
권석흠
이영필
이상용

(77) 심사관
없음

전체 청구항 수 : 총 30 항

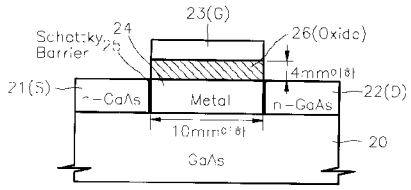
(54)쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터 및 그 제조방법

(57)요 약

본발명은 반도체와 금속 접합시 자연적으로 형성되는 쇼트키 터널 장벽(Schottky tunnel barrier)을 터널 장벽으로 이용하는 단일 전자 트랜지스터(single electron transistor) 및 그 제조 방법에 관한 것이다.

본 발명에 따른 단일전자 트랜지스터에서는, 기존의 산화물을 터널 장벽으로 이용하는 경우 문제가 되어 왔던 재현성 및 균일성을 획기적으로 개선하기 위해 금속과 반도체가 접합시 자연적으로 생기는 쇼트키 장벽을 터널 장벽으로 이용한다.

대 표 도 - 도 2



This Facsimile Page has been artificially created from KIPO data.

청구의 범위

청구항 1

반도체 기판;

상기 반도체 기판 상부에 도전성 불순물이 도핑되어 형성된 소스 및 드레인;

상기 소스 및 드레인 사이의 상기 반도체 기판 상에 금속으로 증착되어 상기 소스 및 드레인과의 경계면에 각각 쇼트키 베리어를 형성하는 아일런드;

상기 아일런드 상에 형성된 절연층; 및

상기 절연층 상에 형성된 게이트;를

구비한 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

청구항 2

제1항에 있어서,

상기 도전성 불순물은 n형 혹은 p형 불순물인 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

청구항 3

제2항에 있어서,

상기 반도체 기판은 GaAs로 형성되고, 상기 소스 및 드레인은 각각 n-GaAs로 형성되며, 상기 절연층은 금속 산화물로 형성된 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

청구항 4

제1항에 있어서,

상기 아일런드는 상기 기판 상부에 소정의 폭으로 도전성 불순물이 도핑된 반도체로 형성되고, 상기 소스 및 드레인은 상기 아일런드 양쪽의 상기 반도체 기판 상에 증착되어 상기 아일런드와의 경계면에 각각 쇼트키 베리어를 형성하도록 금속으로 형성되며, 상기 게이트는 상기 반도체 아일런드 상에 금속으로 증착되어 상기 반도체 아일런드와의 사경계면에 쇼트키 베리어가 형성된 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

청구항 5

제4항에 있어서,

상기 도전성 불순물은 n형 혹은 p형 불순물인 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

청구항 6

제5항에 있어서,

상기 반도체 기판은 GaAs로 형성되고, 상기 반도체 아일런드는 n-GaAs로 형성된 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

청구항 7

(가) GaAs 기판 상에 도전성 불순물을 포함하는 GaAs층을 10nm 이하의 두께로 형성하는 단계;

(나) 상기 도전성 불순물을 포함하는 GaAs층을 소정 폭을 갖는 세선들 및 소스들과 드레인들을 형성한 다음, 상기 세선들에서 각 단일 전자 트랜지스터의 아일런드 영역에 대응하는 영역들은 선택적으로 식각하여 아일런드들을 형성하는 단계;

(다) 상기 아일런드 영역에 금속을 증착하여 상기 소스 및 드레인과의 접합면에 쇼트키 접합이 형성되도록 금속층을 형성하는 단계;

(라) 상기 금속층 위에 두께 4 nm 이하의 유전체를 증착시켜 절연층을 형성하는 단계; 및

(마) 상기 절연층 상에 금속을 증착시켜 게이트를 형성하는 단계;를

포함하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

청구항 8

제7항에 있어서,

상기 (가) 단계에서 상기 도전성 불순물이 포함된 GaAs층은 호모 에피택시법으로 도핑 농도가 $10^{20}/cm^3$ 이하로 조절되게 성장시키는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

청구항 9

제7항에 있어서,

상기 (가) 단계에서 상기 도전성 불순물을 포함하는 GaAs층은 성장중 소스 물질에 의하거나 혹은 GaAs 성장후 확산법 혹은 이온-주입법을 이용하여, 깊이 10 nm, 도핑 농도 $10^{20}/cm^3$ 이하로 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

청구항 10

제7항에 있어서,

상기 (나) 단계에서 상기 세선들의 폭은 100nm이하로 형성하고, 상기 아일런드 영역은 10 nm 이하의 길이로 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

청구항 11

제7항에 있어서,

상기 (나) 단계에서 상기 세선들, 아일런드 영역, 소스 및 드레인은 리프트-오프 공정을 이용하여 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

청구항 12

제7항에 있어서,

상기 (다) 단계에서 상기 쇼트키 접합의 장벽 높이는 1.0 eV 이하로 조절하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

청구항 13

제7항에 있어서,

상기 (라) 단계에서 상기 절연층은 산화로에서 상기 금속층을 두께 4 nm 이하로 산화시킨 금속 산화막으로 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

청구항 14

제7항에 있어서,

상기 (가) 단계에서 상기 GaAs 기판 상에 금속층을 10nm 이하의 두께로 형성하고,상기 (나) 단계에서 상기 금속층을 소정 폭을 갖는 세선들 및 소스들과 드레인들을 형성한 다음, 상기 세선들에서 각 단일 전자 트랜지스터의 아일런드 영역에 대응하는 영역들을 선택적으로 선택적으로 식각하여 아일런드들을 형성하고, 상기 (다) 단계에서 상기 아일런드 영역에 도전성 불순물을 포함하는 GaAs층을 증착하여 상기 소스 및 드레인과의 접합면에 쇼트키 접합이 형성되도록 불순물 반도체층을 형성하며, 상기 (라) 단계를 없애고, 상기 (마) 단계에서 상기 불순물 반도체층 상에 금속을 증착시켜 게이트를 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

청구항 15

Si 기판;

상기 Si 기판 상에 도전성 불순물이 도핑된 반도체층으로 형성된 소스 및 드레인;

상기 소스 및 드레인 사이의 상기 Si 기판 상에 금속으로 증착되어 상기 소스 및 드레인과의 경계면에 각각 쇼트키 베리어를 형성하는 아일런드;

상기 아일런드 상에 형성된 절연층; 및

상기 절연층 상에 형성된 게이트;를

구비한 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

청구항 16

제15항에 있어서,

상기 도전성 불순물은 n형 혹은 p형 불순물인 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

청구항 17

제16항에 있어서,

상기 소스 및 드레인은 각각 n-SiGe 혹은 p-SiGe로 형성되며, 상기 절연층은 SiO_2로 형성된 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

청구항 18

제15항에 있어서,

상기 소스 및 드레인은 금속으로 형성되고, 상기 금속 소스와 Si 기판 사이 및 상기 금속 드레인과 Si 기판 사이에는 상기 Si 기판의 상부를 각각 선택적으로 산화시켜 형성된 제1절연층 및 제2절연층을 더 구비하며, 상기 아일런드는 상기 금속 소스 및 금속 드레인과의 경계면에 쇼트키 베리어가 형성되도록 도전성 불순물이 도핑된 반도체 화합물로 형성한 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

청구항 19

제18항에 있어서,

상기 반도체 아일런드는 n-SiGe 혹은 p-SiGe로 형성된 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

청구항 20

제18항에 있어서,

상기 반도체 아일런드 상에 상기 절연층을 형성하지 않고 바로 상기 금속 게이트를 형성하여 상기 반도체 아일런드와의 경계면에 쇼트키 베리어를 형성한 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

청구항 21

제20항에 있어서,

상기 반도체 아일런드는 n-SiGe 혹은 p-SiGe로 형성된 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

청구항 22

(가) Si 기판 상에 도전성 불순물을 포함하는 Si-Ge층을 10nm 이하의 두께로 형성하는 단계;

(나) 상기 도전성 불순물을 포함하는 Si-Ge층을 소정 폭을 갖는 세선들 및 소스들과 드레인들을 형성한 다음, 상기 세선들에서 각 단일 전자 트랜지스터의 아일런드 영역에 대응하는 영역들을 선택적으로 식각하여 아일런드들을 형성하는 단계;

(다) 상기 아일런드 영역에 금속을 증착하여 상기 소스 및 드레인과의 접합면에 쇼트키 접합이 형성되도록 금속층을 형성하는 단계;

(라) 상기 금속층 위에 두께 4 nm 이하의 유전체를 증착시켜 절연층을 형성하는 단계; 및

(마) 상기 절연층 상에 금속을 증착시켜 게이트를 형성하는 단계;를

포함하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

청구항 23

제22항에 있어서,

상기 (가) 단계에서 상기 도전성 불순물을 포함하는 Si-Ge층은 에피택시법으로 도핑 농도를 $10^{20}/cm^3$ 이하로 성장시키는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

청구항 24

제22항에 있어서,

상기 (가) 단계에서 상기 도전성 불순물을 포함하는 Si-Ge층은 성장시 소스 물질에 의하거나 혹은 성장 후 확산법 혹은 이온-주입법을 이용하여, 깊이 10 nm, 도핑 농도 $10^{20}/cm^3$ 이하로 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

청구항 25

제22항에 있어서,

상기 (나) 단계에서 상기 세선들의 폭은 100nm이하로 형성하고, 상기 아일런드 영역은 10 nm 이하의 길이로 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

청구항 26

제22항에 있어서,

상기 (나) 단계에서 상기 세선들, 아일런드 영역, 소스 및 드레인은 리프트-오프 공정을 이용하여 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

청구항 27

제22항에 있어서,

상기 (다) 단계에서 상기 쇼트키 접합의 장벽 높이는 1.0 eV 이하로 조절하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

청구항 28

제22항에 있어서,

상기 (라) 단계에서 상기 절연층은 산화로에서 상기 금속층을 두께 4 nm 이하로 산화시킨 금속 산화막으로 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

청구항 29

제22항에 있어서,

상기 (가) 단계에서 상기 Si 기판 상에 SiO_2막을 형성한 다음, 상기 SiO_2막 상에 금속층을 10nm 이하의 두께로 형성하고, 상기 (나) 단계에서 상기 금속층 및 SiO_2막을 소정 폭을 갖는 세선들 및 소스들과 드레인들을 형성한 다음, 상기 세선들에서 각 단일 전자 트랜지스터의 아일런드에 대응하는 영역들을 선택적으로 식각하여 아일런드들을 형성하고, 상기 (다) 단계에서 상기 아일런드 영역에 도전성 불순물을 포함하는 Si-Ge층을 증착하여 상기 소스 및 드레인과의 접합면에 쇼트키 접합이 형성되도록 불순물 반도체층을 형성하며, 상기 (라) 단계에서 상기 불순물 반도체층 상에 절연층을 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

청구항 30

제22항에 있어서,

상기 (가) 단계에서 상기 Si 기판 상에 SiO_2막을 형성한 다음, 상기 SiO_2막 상에 금속층을 10nm 이하의 두께로 형성하고, 상기 (나) 단계에서 상기 금속층 및 SiO_2막을 소정 폭을 갖는 세선들 및 소스들과 드레인들을 형성한 다음, 상기 세선들에서 각 단일 전자 트랜지스터의 아일런드들에 대응하는 영역들

을 선택적으로 식각하여 아일런드들을 형성하고, 상기 (다) 단계에서 상기 아일런드 영역에 도전성 불순물을 포함하는 Si-Ge층을 증착하여 상기 소스 및 드레인과의 접합면에 쇼트키 접합이 형성되도록 불순물 반도체층을 형성하며, 상기 (라) 단계를 없애고 상기 (마) 단계에서 상기 불순물 반도체층 상에 금속을 증착하여 게이트를 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

명세서

발명의 명칭

쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터 및 그 제조 방법

도면의 간단한 설명

도 1a 및 도 1b는 각각 종래의 단일 전자 트랜지스터의 개략적인 수직 단면도이고,

도 2는 본 발명에 따른 단일 전자 트랜지스터 제1실시예의 개략적인 수직 단면도이며,

도 3은 본 발명에 따른 단일 전자 트랜지스터 제2실시예의 개략적인 수직 단면도이며,

도 4는 본 발명에 따른 단일 전자 트랜지스터 제3실시예의 개략적인 수직 단면도이며,

도 5는 본 발명에 따른 단일 전자 트랜지스터 제4실시예의 개략적인 수직 단면도이며,

그리고 도 6은 본 발명에 따른 단일 전자 트랜지스터 제5실시예의 개략적인 수직 단면도이다.

<도면의 주요부분에 대한 부호의 설명>

1. 실리콘 기판 2. 소스

3. 드레인 4. 아일런드

5. 터널 장벽

11a. 실리콘 기판 11b. SiO_2 산화층

11. SOI 기판 12. 소스

13. 드레인 14. 아일런드

15. 유전체(터널장벽)

20. GaAs 기판 21. n-GaAs 소스

22. n-GaAs 드레인 23. 게이트

24. 금속층 25. 쇼트키 장벽

26. 산화물층

30. GaAs 기판 31. 금속 소스

32. 금속 드레인 33. 금속 게이트

34. n-GaAs 아일런드 35. 쇼트키 장벽

40. Si 기판 41. n-SiGe 혹은 p-SiGe 소스

42. n-SiGe 혹은 p-SiGe 드레인　　43. 금속 게이트

44. 금속 아일런드　　45. 쇼트키 장벽

46. SiO_2 산화물층

50. Si 기판　　51. 금속 소스

52. 금속 드레인　　53. 금속 게이트

54. n-SiGe 혹은 p-SiGe 아일런드　　55. 쇼트키 장벽

56. 산화물층　　57a, 57b. SiO_2 산화물층

60. Si 기판　　61. 금속 소스

62. 금속 드레인　　63. 금속 게이트

64. n-SiGe 혹은 p-SiGe 아일런드　　65. 쇼트키 장벽

67a. SiO_2 산화물층　　67b. SiO_2 산화물층

발명의 상세한 설명

본발명은 반도체와 금속 접합시 자연적으로 형성되는 쇼트키 터널 장벽(Schottky tunnel barrier)을 터널 장벽으로 이용한 단일 전자 트랜지스터(single electron transistor) 및 그 제조 방법에 관한 것이다.

도 1a 및 도 1b는 종래의 단일 전자 트랜지스터들의 개략적 수직 단면도이다. 종래의 단일 전자 트랜지스터는, 도 1a에 도시된 바와 같이, 실리콘 기판(1) 상에 소스(source)(2)와 드레인(drain)(3) 사이에 2개의 터널 장벽(tunnel barrier)(5)을 만들어 아일런드(island)(4)를 형성시킨 구조이거나, 혹은 도 1b에 도시된 바와 같이, 실리콘 기판(11a) 상에 SiO_2 절연막(11b)를 형성한 SOI 기판(11) 상면에 소스(12)와 드레인(13)을 형성한 후, 유전체(15) 속에 금속이나 반도체를 물리적(예, PVD) 혹은 화학적(예, CVD) 증착을 통해 나노미터(nm) 크기인 알갱이(granular) 모양의 아일런드(14)를 형성시킨 구조이다.

그러나, 참고 문헌 T.Wada etal Jpn.J.Appl.Phys 34,12B(1995)6961에 따르면, 도 1a에 도시된 바와 같은 단일 전자 트랜지스터의 경우 아일런드(15)의 크기를 나노미터 크기로 균일하게 제어하는 것이 매우 어렵다. 특히, 전자빔 리소그래피(E-beam lithography) 공정을 이용시 터널장벽을 형성키 위해 많은 공정을 거쳐야 하며 상온에서 작동하는 아일런드의 크기를 제어하는 것은 거의 불가능하다. 또한, K.Matsumoto et al Appl.Phys.Lett 68(1996)34에 따르면, SPM(scanning probe microscopy)을 응용할 경우 터널 장벽이 공기중에서 열화되기 때문에 단일 전자 트랜지스터의 작동 재현성이 전혀없다. 그리고 참고문헌 W.Chen etal Appl.Phys.Lett 66(1995)3383 및 A.Dutta etal Jpn.J.Appl.Phys 36,6B(1997)4038에 의하면, 도 1b에 도시된 바와 같은 단일 전자 트랜지스터의 경우, 아일런드(14)의 숫자를 결정하는 소스(12)와 드레인(13) 사이의 거리를 재현성 있게 제어하기도 어렵고 공정 자체도 복잡하여 제조상 어려움이 따른다. 따라서 재현성있는 상온 작동 단일 전자 트랜지스터를 구현하기 위해서는 공정이 간단하며 아일런드의 크기를 나노미터 크기로 쉽게 제어할 수 있는 새로운 구조 및 제조 방법이 요구된다.

본발명은 상기와 같은 문제점을 개선하기 위하여 창안된 것으로, 반도체와 금속 접합시 자연적으로 형성되는 쇼트키 터널 장벽(Schottky tunnel barrier)을 터널 장벽으로 이용하여 재현성 및 균일성을 개선한 단일 전자 트랜지스터 및 그 제조 방법을 제공하는데 그 목적이 있다.

상기와 같은 목적을 달성하기 위하여 본 발명에 따른 단일 전자 트랜지스터는, 반도체 기판; 상기 반도체 기판 상부에 도전성 불순물이 도핑되어 형성된 소스 및 드레인; 상기 소스 및 드레인 사이의 상기 반도체 기판 상에 금속으로 증착되어 상기 소스 및 드레인과의 경계면에 각각 쇼트키 베리어를 형성하는 아일런드; 상기 아일런드 상에 형성된 절연층; 및 상기 절연층 상에 형성된 게이트;를 구비한 것을 특징으로 한다.

본 발명에 있어서, 상기 반도체 기판은 GaAs로 형성되고, 상기 소스 및 드레인은 각각 n-GaAs로 형성되며, 상기 절연층은 금속 산화물로 형성된 것이 바람직하며, 상기 아일런드는 상기 기판 상부에 소정의 폭으로 도전성 불순물이 도핑된 반도체로 형성되고, 상기 소스 및 드레인은 상기 아일런드 양쪽의 상기 반도체 기판 상에 증착되어 상기 아일런드와의 경계면에 각각 쇼트키 베리어를 형성하도록 금속으로 형성되며, 상기 게이트는 상기 반도체 아일런드 상에 금속으로 증착되어 상기 반도체 아일런드와의 사 경계면에 쇼트키 베리어가 형성된 것도 바람직하다.

또한, 상기와 같은 목적을 달성하기 위하여 본 발명에 따른 단일 전자 트랜지스터의 제조 방법은, (가) GaAs 기판 상에 도전성 불순물을 포함하는 GaAs층을 10nm 이하의 두께로 형성하는 단계; (나) 상기 도전성 불순물을 포함하는 GaAs층을 소정 폭을 갖는 세선들 및 소스들과 드레인들을 형성한 다음, 상기 세선들에서 각 단일 전자 트랜지스터의 아일런드 영역에 대응하는 영역들을 선택적으로 식각하여 아일런드들을 형성하는 단계; (다) 상기 아일런드 영역에 금속을 증착하여 상기 소스 및 드레인과의 접합면에 쇼트키 접합이 형성되도록 금속층을 형성하는 단계; (라) 상기 금속층 위에 두께 4 nm 이하의 유전체를 증착시켜 절연층을 형성하는 단계; 및 (마) 상기 절연층 상에 금속을 증착시켜 게이트를 형성하는 단계;를 포함하는 것을 특징으로 한다.

본 발명에 있어서, 상기 (가) 단계에서 상기 도전성 불순물을 포함하는 GaAs층은 호모 에피택시법으로 도핑 농도를 $10^{20}/cm^3$ 이하로 성장시키거나 확산법 혹은 이온-주입법을 이용하여, 깊이 10 nm, 도핑 농도 $10^{20}/cm^3$ 이하로 형성하며, 상기 (나) 단계에서 상기 세선들의 폭은 100nm이하로 형성하고, 상기 아일런드 영역은 10 nm 이하의 길이로 형성하며, 상기 (다) 단계에서 상기 쇼트키 접합의 장벽 높이는 1.0 eV 이하로 조절하며, 상기 (라) 단계에서 상기 절연층은 산화로에서 상기 금속층을 두께 4 nm 이하로 산화시킨 금속 산화막으로 형성하는 것이 바람직하며,

상기 (가) 단계에서 상기 GaAs 기판 상에 금속층을 10nm 이하의 두께로 형성하고, 상기 (나) 단계에서 상기 금속층을 소정 폭을 갖는 세선으로 형성한 다음, 상기 세선들에서 각 단일 전자 트랜지스터의 아일런드 영역에 대응하는 영역들을 선택적으로 식각하여 아일런드들을 형성하고, 상기 (다) 단계에서 상기 아일런드 영역에 도전성 불순물을 포함하는 GaAs층을 증착하여 상기 소스 및 드레인과의 접합면에 쇼트키 접합이 형성되도록 불순물 반도체층을 형성하며, 상기 (라) 단계를 없애고, 상기 (마) 단계에서 상기 불순물 반도체층 상에 금속을 증착시켜 게이트를 형성하는 것도 바람직하다.

또한, 상기와 같은 목적을 달성하기 위하여 본 발명에 따른 또 다른 단일 전자 트랜지스터는, Si 기판; 상기 Si 기판 상에 도전성 불순물이 도핑된 반도체층으로 형성된 소스 및 드레인; 상기 소스 및 드레인 사이의 상기 Si 기판 상에 금속으로 증착되어 상기 소스 및 드레인과의 경계면에 각각 쇼트키 베리어를 형성하는 아일런드; 상기 아일런드 상에 형성된 절연층; 및 상기 절연층 상에 형성된 게이트;를 구비한 것을 특징으로 한다.

본 발명에 있어서, 상기 소스 및 드레인은 각각 n-SiGe 혹은 p-SiGe로 형성되고 상기 절연층은 SiO_2로 형성된 것이 바람직하며, 상기 소스 및 드레인은 금속으로 형성되고, 상기 금속 소스와 Si 기판 사이 및 상기 금속 드레인과 Si 기판 사이에는 상기 Si 기판의 상부를 각각 선택적으로 산화시켜 형성된 제1절연층 및 제2절연층을 더 구비하며, 상기 아일런드는 상기 금속 소스 및 금속 드레인과의 경계면에 쇼트키 베리어가 형성되도록 도전성 불순물이 도핑된 반도체 화합물로 형성한 것도 바람직하다.

또한 본 발명에 있어서, 상기 반도체 아일런드 상에 상기 절연층을 형성하지 않고 바로 상기 금속 게이트를 형성하여 상기 반도체 아일런드와의 경계면에 쇼트키 베리어를 형성한 것도 바람직하다.

또한, 상기와 같은 목적을 달성하기 위하여 본 발명에 따른 단일 전자 트랜지스터의 제조 방법은, (가) Si 기판 상에 도전성 불순물을 포함하는 Si-Ge층을 10nm 이하의 두께로 형성하는 단계; (나) 상기 도전성 불순물을 포함하는 Si-Ge층을 소정 폭을 갖는 세선들 및 소스들과 드레인들을 형성한 다음, 상기 세선들에서 각 단일 전자 트랜지스터의 아일런드 영역에 대응하는 영역들을 선택적으로 식각하여 아일런드들을 형성하는 단계; (다) 상기 아일런드 영역에 금속을 증착하여 상기 소스 및 드레인과의 접합면에 쇼트키 접합이 형성되도록 금속층을 형성하는 단계; (라) 상기 금속층 위에 두께 4 nm 이하의 유전체를 증착시켜 절연층을 형성하는 단계; 및 (마) 상기 절연층 상에 금속을 증착시켜 게이트를 형성하는 단계;를 포함하는 것을 특징으로 한다.

본 발명에 있어서, 상기 (가) 단계에서 상기 도전성 불순물을 포함하는 Si-Ge층은 에피택시법으로 도핑 농도를 $10^{20}/cm^3$ 이하로 성장시키거나 혹은 성장시 소스 물질에 의하거나 혹은 성장후 확산법 혹은 이온-주입법을 이용하여, 깊이 10 nm, 도핑 농도 $10^{20}/cm^3$ 이하로 형성하며, 상기 (나) 단계에서 상기 세선들의 폭은 100nm이하로 형성하고, 상기 아일런드 영역은 10 nm 이하의 길이로 형성하며, 상기 (다) 단계에서 상기 쇼트키 접합의 장벽 높이는 1.0 eV 이하로 조절하며, 상기 (라) 단계에서 상기 절연층은 산화로에서 상기 금속층을 두께 4 nm 이하로 산화시킨 금속 산화막으로 형성하는 것이 바람직하며, 상기 (가) 단계에서 상기 Si 기판 상에 SiO_2막을 형성한 다음, 상기 SiO_2막 상에 금속층을 10nm 이하의 두께로 형성하고, 상기 (나) 단계에서 상기 금속층 및 SiO_2막을 소정 폭을 갖는 세선들 및 소스들과 드레인들을 형성한 다음, 상기 세선들에서 각 단일 전자 트랜지스터의 아일런드 영역에 대응하는 영역들을 선택적으로 식각하여 아일런드들을 형성하고, 상기 (다) 단계에서 상기 아일런드 영역에 도전성 불순물을 포함하는 Si-Ge층을 증착하여 상기 소스 및 드레인과의 접합면에 쇼트키 접합이 형성되도록 불순물 반도체층을 형성하며, 상기 (라) 단계에서 상기 불순물 반도체층 상에 절연층을 형성하거나, 상기 (라) 단계를 없애고 상기 (마) 단계를 바로 실시하여 상기 불순물 반도체층 상에 바로 금속을 증착하여 게이트를 형성하는 것이 바람직하다.

이하 본 발명에 따른 단일 전자 트랜지스터의 여러 가지 실시예 및 그 제조 방법을 상세하게 설명한다.

본 발명에 따른 단일 전자 트랜지스터는 반도체와 금속 접합시 자연적으로 형성되는 쇼트키 터널 장벽(Schottky tunnel barrier)을 터널 장벽으로 이용함으로써, 기존의 산화물 터널 장벽(tunnel barrier)을 응용한 단일 전자 트랜지스터 제조시 기본적으로 문제가 된 재현성 및 균일성을 획기적으로 개선하고 제조 공정을 용이하게 한 점에 특징이 있다. 이러한 반도체-금속 접합의 쇼트키 터널장벽을 이용하여 단일 전자 트랜지스터를 제조하면 상온 작동이 가능하며 이를 응용하여 차세대 초고집적(1 Terra bit) 메모리 및 로직에 응용할 수 있다. 이러한 특징들을 도 2 내지 도 6을 참조하여 상세하게 설명하면 다음과 같다.

도 2는 본 발명에 따른 단일 전자 트랜지스터 제1실시예의 개략적인 수직 단면도이다. 도시된 바와 같이, 제1실시예는 GaAs 반도체 기판(20) 상에 n-GaAs 소스(21) 및 n-GaAs 드레인(22) 사이에 금속층(24)이 삽입된 트랜지스터 구조물이 적층되고, 금속층(24) 상에 산화물층(26) 및 게이트(23)가 순차로 적층된 구조로 형성된다. 따라서, n-GaAs 소스(21)와 금속층(24)의 접합면 및 n-GaAs 드레인(22)과 금속층(24)의 접합면에는 각각 쇼트키 장벽(25)이 형성된다.

이와 같은 구조의 제1실시예를 제조하는 방법은 다음과 같다.

먼저, 도 3a 및 도 3b에 도시된 바와 같이, 반(Semi)-절연체 즉 반도체인 GaAs를 포함한 화합물 반도체 기판(20) 상에 10 nm 이하 두께의 GaAs를 포함한 화합물 반도체(210)를 호모 에피택시(Homo Epitaxy)법으로 성장시킨다. GaAs를 포함한 화합물 반도체 성장시 도핑 레벨(doping level)을 $10^{20}/cm^3$ 이하로 하여 n-GaAs를 포함한 화합물 반도체(210)로 만든다. 그렇치 않으면, 도 3b에 도시된 바와 같이, GaAs

를 포함한 화합물 반도체 기판(20)에 확산(diffusion) 혹은 이온-주입(ion-implantation)을 이용하여 깊이 10 nm, 도핑 농도(concentration) $10^{20}/cm^3$ 이하의 n형 반도체(210')로 만든다.

다음에, 도 3a에 도시된 바와 같이, 식각 공정을 통해 폭 100 nm의 세선(wire)(210a, 210'a)을 만들어 소스(21)와 드레인(22)을 형성할 수 있도록 한다. 소스(21)와 드레인(22)은 저항을 고려하여 세선의 다른 영역(아일런드 영역(220a) 및 트랜지스터 경계 영역(220b)) 보다 도핑 농도를 높게한다. 세선(210a, 210'a), 센선들을 따라 배치되는 소스(21) 및 드레인(22)의 제조는 리프트-오프(lift-off) 공정을 통해 선택적 성장법을 적용해도 무방하다. 이렇게 형성된 세선(210a 혹은 210'a)에 형성된 소스(21)와 드레인(22) 사이에, 도 3d에 도시된 바와 같이, 길이 10 nm 이하의 아일런드 영역(220a)을 식각 후 금속 증착을 통해 금속층(24)을 도 2에 도시된 바와 같이 형성한다. 이 금속층(24; 아일런드) 위에 두께 4 nm 이하의 유전체(26)를 증착시키거나 산화로에서 그 금속 산화막(26)을 두께 4 nm 이하로 형성시킨 후 금속을 증착시켜 게이트(gate)(23)를 만든다. 이렇게 형성된 금속층(24)과 세선의 n-GaAs 영역(21, 22)을 포함한 화합물 반도체 사이에는 쇼트키 접합(Schottky junction)(25)이 형성되며, 쇼트키 장벽 높이(barrier height)는 1.0 eV 이하로 조절한다. 이 에너지 장벽을 이용하여 단일 전자 트랜지스터를 구현한다.

도 4은 도 2의 제1실시예와는 다른 제2실시예의 수직 단면도를 나타낸다. 도시된 바와 같이, 제2실시예는 GaAs 반도체 기판(30) 상에 금속 소스(31) 및 금속 드레인(32) 사이에 n-GaAs 도핑층(34)이 삽입된 트랜지스터 구조물이 적층되고, n-GaAs 도핑층(34) 상에 금속 게이트(33)가 순차로 적층된 구조로 형성된다. 따라서, 금속 소스(31)와 n-GaAs 도핑층(34)의 접합면 및 금속 드레인(32)과 n-GaAs 도핑층(34)의 접합면에는 각각 쇼트키 장벽(25)이 형성된다. 특히, 제1실시예에서와 같은 절연층이 형성되지 않고 n-GaAs 도핑층(34) 위에 바로 금속 게이트(33)가 형성된다. n-GaAs 도핑층(34)와 게이트(33) 사이에는 쇼트키 장벽이 형성되므로 별도의 절연층을 형성할 필요가 없다.

이와 같은 구조의 제2실시예는 제1실시예와 유사한 순서로 제조된다. 즉, GaAs를 포함한 화합물 반도체 기판(30)에 금속(31, 32)을 10 nm 두께 이하로 증착한 후 식각공정을 통해 폭 100 nm의 세선(34)을 이루도록 소스(31) 및 드레인(32)을 형성한다. 세선(미도시, 도 3a 참조)을 따라 배치되는 소스(31) 및 드레인(32)은 리프트-오프 공정을 통해 형성한다. 소스(31)와 드레인(32) 사이의 세선(미도시)에 길이 10 나노미터의 아일런드 영역(34)을 식각에 의해 형성한 후(도 3d 참조) GaAs를 포함한 화합물 반도체를 호모에피택시(Homo-Epitaxy)법에 의해 성장시킨다. GaAs를 포함한 화합물 반도체 성장시 혹은 성장 후에는 도핑 레벨 및 도핑법을 도 3b 혹은 도 3c와 동일하게 적용하여 n형으로 한다. 그 다음 n형 GaAs 혹은 화합물 반도체(34) 위에 금속을 증착시켜 게이트(33)를 형성한다. 이렇게 형성된 금속(소스, 드레인 및 게이트)과 n-GaAs를 포함한 화합물 반도체 사이에는 쇼트키 접합이 형성되며 장벽 높이는 1.0 eV 이하로 조절한다. 이 에너지 장벽을 이용하여 단일 전자 트랜지스터를 구현한다.

도 5는 제3실시예의 수직 단면도를 나타낸다. 제3실시예는 GaAs를 포함한 화합물 반도체 기판 대신에 실리콘(Si) 혹은 SOI 기판(40)을 사용하여 단일 전자 트랜지스터를 구현한 것이다. 도시된 바와 같이, 제3실시예는 Si 기판(40) 상에 n-SiGe 혹은 p-SiGe 소스(41) 및 n-SiGe 혹은 p-SiGe 드레인(42) 사이에 금속층(44)이 삽입된 트랜지스터 구조물이 적층되고, 금속층(44) 상에 SiO_2층(46) 및 게이트(43)가 순차로 적층된 구조로 형성된다. 따라서, n-SiGe 혹은 p-SiGe 소스(41)와 금속층(44)의 접합면 및 n-SiGe 혹은 p-SiGe 드레인(42)과 금속층(44)의 접합면에는 각각 쇼트키 장벽(45)이 형성된다.

이와 같은 구조의 제3실시예를 제조하는 방법은 기판 및 반도체 도핑층의 재료만 다를뿐 제1실시예의 제조 방법과 같다.

우선, 실리콘 기판(40) 상에 n 혹은 p 형 Si-Ge을 10 nm 두께 이하로 에피택시(Epitaxial)하게 성장시킨다. 이 때의 도핑 레벨은 $10^{20}/cm^3$ 이하로 하며 도핑하는 방법으로는 에피택시(Epitaxial) 성장시와 성장 후 이온-주입(ion-implantation) 혹은 확산(diffusion)에 의해 가능하다. 그 다음 식각 공정을 통해 폭 100 nm 이하의 세선(44)과 소스(41) 및 드레인(42)을 형성한 후, 소스(41) 및 드레인(42) 사이의 세선(44)을 길이 10 nm 이하로 식각하여 아일런드 영역을 형성한다. 다음에, 아일런드 영역에 금속을 증착하여 금

속층(44)을 형성한다. 소스(41) 및 드레인(42)의 도핑 레벨은 세선의 다른 영역들(아일런드 영역 및 트랜지스터가 경계 영역) 보다 높게 한다. 세선(미도시)을 따라 배치된 소스(41) 및 드레인(42)의 형성은 리프트-오프 공정에 의해서도 가능하다.

다음에, 아일런드용 금속층(44) 위에 두께 4 nm 이하의 유전체(46)를 증착시키거나 산화로에서 두께 4 nm 이하의 금속 산화물을 형성시킨후 그 위에 금속을 증착시켜 게이트(43)를 형성한다. 이렇게 형성된 세선의 금속(44)과 SiGe 소스 및 게이트(41, 42) 사이에는 쇼트키 접합이 형성되며, 장벽 높이는 1.0 eV 이하로 조절한다. 이 에너지 장벽을 이용하면 단일전자트랜지스터가 구현된다.

도 6은 도 5의 제3실시예와 다른 제4실시예의 수직 단면도를 나타낸다. 제4실시예는 소스(51)와 드레인(52)을 금속으로 형성하되 실리콘 기판과 SiO_2층(57a, 57b)에 의해 격리되고, 아일런드 영역을 n-SiGe 혹은 p-SiGe 도핑층(54)로 형성한 점에서 제3실시예와 차이가 있을뿐 구조적으로 제3실시예와 비슷하다.

이러한 구조의 제4실시예의 제조 방법은 다음과 같다.

먼저, SiO층이 형성된 실리콘 혹은 SOI 기판(50, 57a, 57b) 상에 10 nm 이하의 두께로 금속(51,52)을 증착한 후 식각 공정을 거쳐 100 nm 폭의 세선 형상을 따라 소스(51) 및 드레인(52)을 형성한다(도 3a 참조). 세선을 따라 형성된 소스(51) 및 드레인(52) 제조 공정은 리프트-오프 공정을 적용해도 무방하다.

그 다음 세선을 따라 배치되는 소스 및 드레인 영역 사이에 길이 10 nm 이하의 아일런드 영역을 식각 후 p-SiGe 혹은 n-SiGe을 증착하여 형성시킨다. 이 때의 도핑은 SiGe 성장시 혹은 성장후 이온주입 혹은 확산에 의해 수행되며, 그 레벨은 $10^{20}/cm^3$ 이하로 한다.

다음에, 게이트는 유전체를 4 nm 이하로 증착하거나 혹은 실리콘 -게르마늄층을 산화로에서 두께 4 nm 이하의 산화물을 형성시킨후 금속을 증착시켜 형성한다. 이렇게 형성된 금속과 n 혹은 p 형 사이에는 쇼트키 접합이 형성되며 장벽 높이는 1.0 eV 이하로 조절한다. 이 에너지 장벽을 이용하여 단일 전자 트랜지스터를 구현하는 것이다.

도 7은 제5실시예의 수직 단면을 보여주는 도면이다. 제5실시예는 아일런드 영역의 n-SiGe 혹은 p-SiGe 도핑층(64) 상에 바로 금속을 증착하여 게이트(63)를 형성한 점에서 제4실시예와 차이가 있을뿐 구조적으로 제4실시예와 비슷하다.

따라서, 제5실시예의 제조 방법은 도 6의 제5실시예에서와 유사하며, 다만 게이트(63)와 아일런드(64) 사이를, 제4실시예에서 처럼 4 nm 이하의 유전체(56)에 의해 분리해 놓지 않고, 금속 게이트(63)를 직접 SiGe층(64)에 접합시켜 생기는 쇼트키 장벽을 절연물로 이용하는 구조로서, 그 이외의 공정은 모든 것이 도 6의 제4실시예와 동일하다.

이상과 같은 방식으로 제작된 단일전자 트랜지스터의 동작 원리는 다음과 같다.

일반적으로 금속과 n 혹은 p형 반도체가 접합시 평형 상태를 얻기위해 캐리어(carrier)들이 이동한다. 이 때문에 접합 사이에는 쌍극자(dipole)가 생기게 되며, 이 것이 에너지 장벽 즉 쇼트키 장벽으로 작용한다. 이 다이폴이 생긴 영역 즉 공핍(depletion) 영역의 두께 d와 캐패시턴스(capacitance) C 는 다음 수학식 1 및 2로 표시된다.

수학식 1 :

$$d = (2\varphi\varepsilon\varepsilon_0 / ne)^{1/2}$$

수학식 2 :

$$C = A(\varepsilon\varepsilon_0 ne/\varphi)^{1/2}$$

여기서, n은 도핑레벨, e는 전하량, ε는 공기유전상수, ε_0는 물질의 유전상수, φ는 공핍층에의해 생긴 전압, A는 단면적이다. 만약, $n=10^{20}/cm^3$이고 φ=0.7 Volt 라면 d=3.3 nm 이고, $C/A= 3.4 \times 10^{-20}$ F/nm^2 가 된다. 수식 1 및 2에서 알 수 있듯이 도핑 레벨과 가해주는 전압을 조절함으로써 C 값을 더욱더 낮출 수 있다. 단일전자트랜지스터의 작동 온도는 아래 수학식 3에 의해서 결정된다.

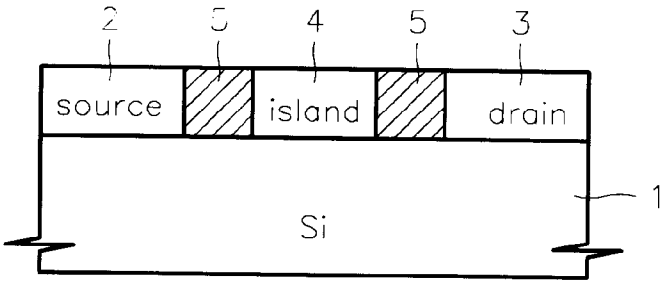
수학식 3 :

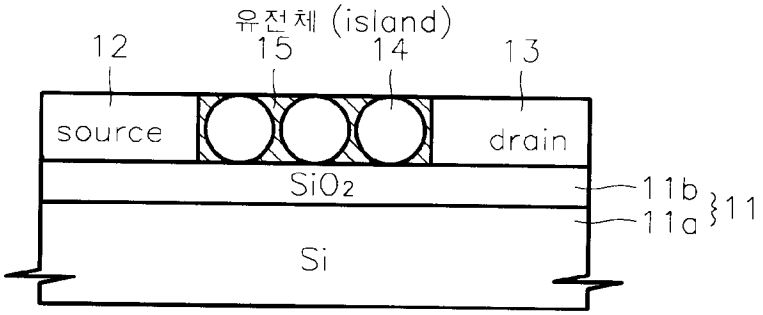
$$e^2/2C >> K_B T$$

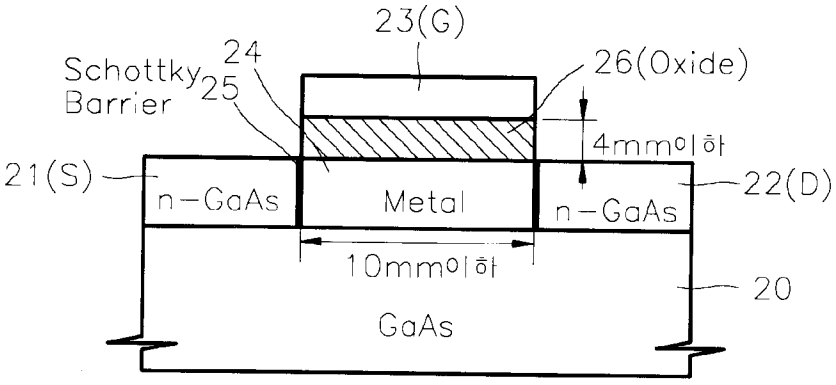
가령 $C = 3.4 \times 10^{-20}$ [F] 이라 하자. 그러면 $T = 273 \times 10^2$ K 가된다. 이상과 같은 물리적 변수를 이용하여 제작된 단일전자 트랜지스터는 아래와 같은 원리로 작동한다.

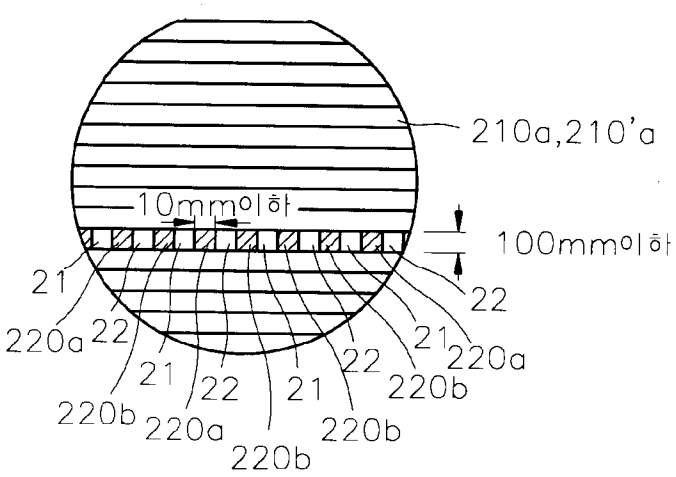
소스와 드레인 사이에 전압을 가하면 임의 전압에 이르러서야 전류가 흐른다. 이 때의 임의 전압을 쿠룽블러케이드갭(Coulomb blockade gap)이라 부르며, 전류가 흐르지 않는 것은 전자 하나가 소스에서 아일런드로 터널됨에 따라 아일런드에 충전(charging)이 일어나 더 이상의 전자를 받아들일 수 없기 때문이다. 만약 이 충전 에너지 보다 큰 에너지를 게이트에 공급하면 쿠룽블러케이드는 일어나지 않게되어 임의의 전류가 흐르게 된다. 그러므로 소스와 드레인 사이의 전압을 쿠룽부룩케이드 갭 이하로 고정시키고 게이트 전압을 조절하면 기존의 3단자 트랜지스터와 유사하게 스위칭(switching)이 일어난다.

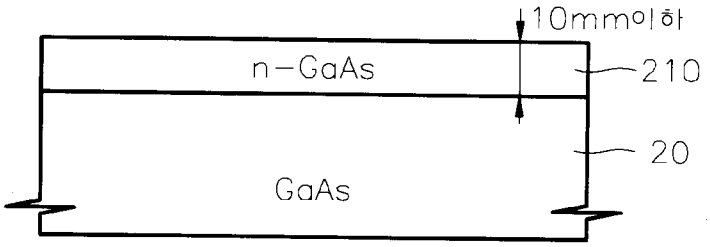
이상 설명한 바와 같이, 본 발명에 따른 단일전자 트랜지스터에서는, 기존의 산화물을 터널장벽으로 이용하는 공정으로는 상온에서 작동하기 위해 단일전자 트랜지스터의 아일런드의 크기를 10 nm 정도로 재현성 있게 제한해야 하는 어려움을 극복하기 위하여, 금속과 반도체가 접합시 자연적으로 생기는 쇼트키 장벽을 터널 장벽으로 이용하는 점에 특징이 있다. 기존의 단일전자 트랜지스터 제조시에는 산화물을 터널장벽으로 형성하기 위해 많은 제조 공정을 거쳐야 하며, 또한 많은 공정을 거친다 하더라도 아일런드 크기의 재현성을 보장할 수 없었다. 본 발명은 이러한 난점을 쇼트키 장벽을 터널 장벽으로 이용함으로써 상기 두 가지 문제를 크게 개선한다. 더욱이, 아일런드 크기를 nm 단위로 쉽게 제어할 수 있기 때문에 상온 작동이 가능하며 터널 장벽의 열화가 없어 오랫동안 신뢰성 있는 소자로서 작동할 수 있다. 따라서, 본 발명에 의해 제작된 단일전자 트랜지스터는 상온작동 1 Tb 급 메모리 및 로직소자에 응용된다

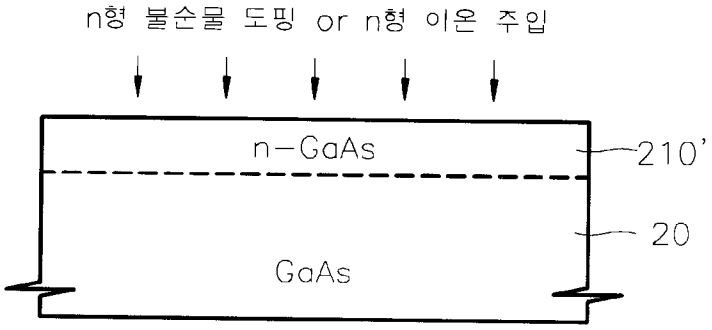

2
3
4
5
3
source
island
drain
1
Si

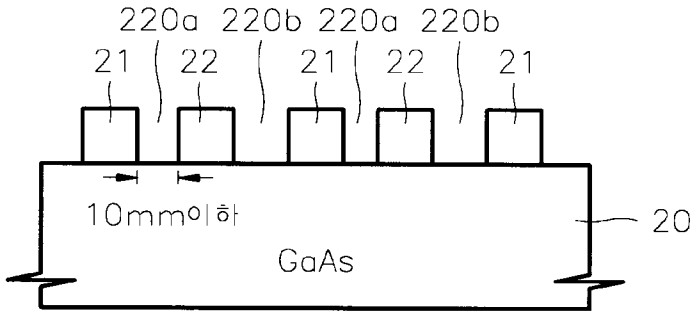

유전체 (island)
12
15
14
13
source
drain
SiO2
11b
11a
11
Si

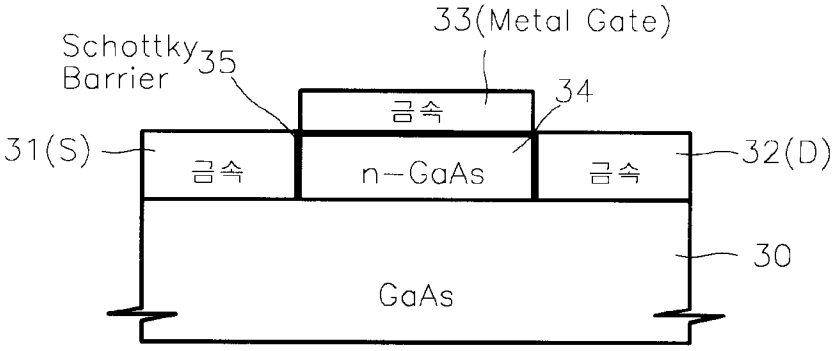

23(G)
24
Schottky
Barrier
25
26(Oxide)
4mm이하
21(S)
n-GaAs
Metal
n-GaAs
22(D)
10mm이하
20
GaAs

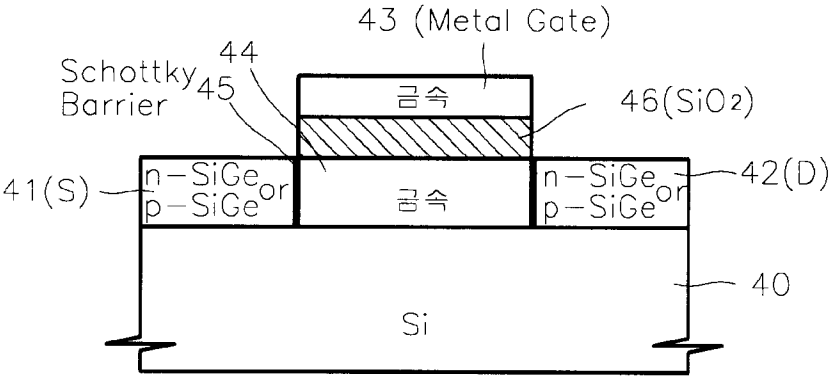

210a,210'a
10mm이하
100mm이하
21
220a
22
21
22
220b
21
22
220a
21
22
220b
220a
220b
220b
22
21
220a

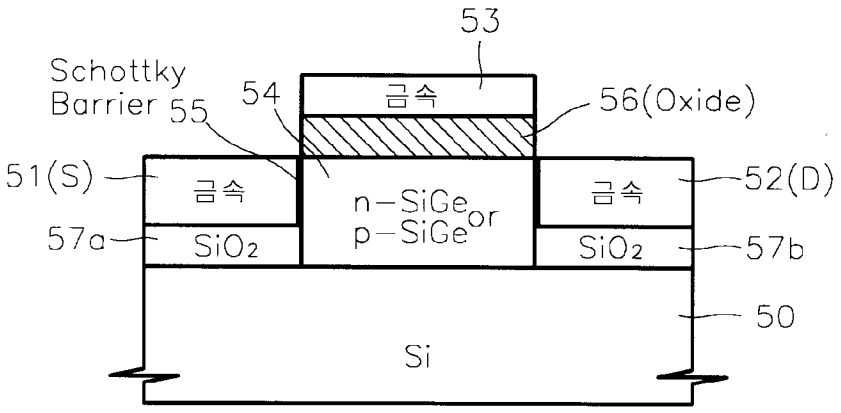

10mm이하
n-GaAs
210
20
GaAs

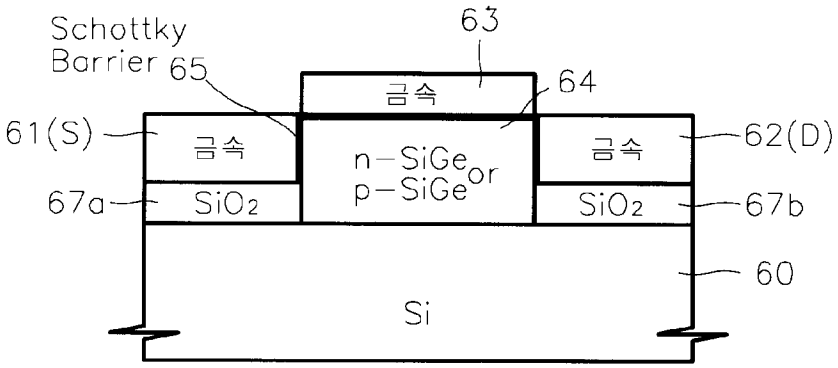

n형 불순물 도핑 or n형 이온 주입
n-GaAs
210'
20
GaAs


220a 220b 220a 220b
21 22 21 22 21
10mm이하
20
GaAs


33(Metal Gate)
Schottky Barrier
35
34
금속
31(S)
금속
n-GaAs
금속
32(D)
30
GaAs


43 (Metal Gate)
44
Schottky Barrier
45
금속
46(SiO2)
41(S)
n-SiGe or p-SiGe
금속
n-SiGe or p-SiGe
42(D)
40
Si


53
Schottky
Barrier
55
54
금속
56(Oxide)
51(S)
금속
n-SiGe or
p-SiGe
금속
52(D)
57a
SiO2
SiO2
57b
50
Si


63
Schottky
Barrier
65
금속
64
61(S)
금속
n-SiGe or
p-SiGe
금속
62(D)
67a
SiO2
SiO2
67b
60
Si

Unexamined Patent Publication(A)

Bibliographic Data

Int.Cl.	H01L 29/47 | H01L 29/78 | H01L 29/49
Published Date	20040716
Registration No.	1004345340000
Registration Date	20040525
Application No.	1019980042717
Application Date	19981013
Unexamined Publication No.	1020000025576
Unexamined Publication Date	20000506
Requested Date of Examination	20020624
Agent.	Lee Young Pil
Inventor	Jo-Won Lee | Jeong-U Kim | Byeong-Man Kim | Mun-Gyeong Kim
Applicant	SAMSUNG ELECTRONICS CO., LTD.
Rightholder	SAMSUNG ELECTRONICS CO., LTD.

발명의 명칭

쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터 및 그 제조방법

Title of Invention

SINGLE ELECTRON TRANSISTOR USING SCHOTTKY TUNNEL BARRIER AND METHOD FOR FABRICATING THE SAME

요약

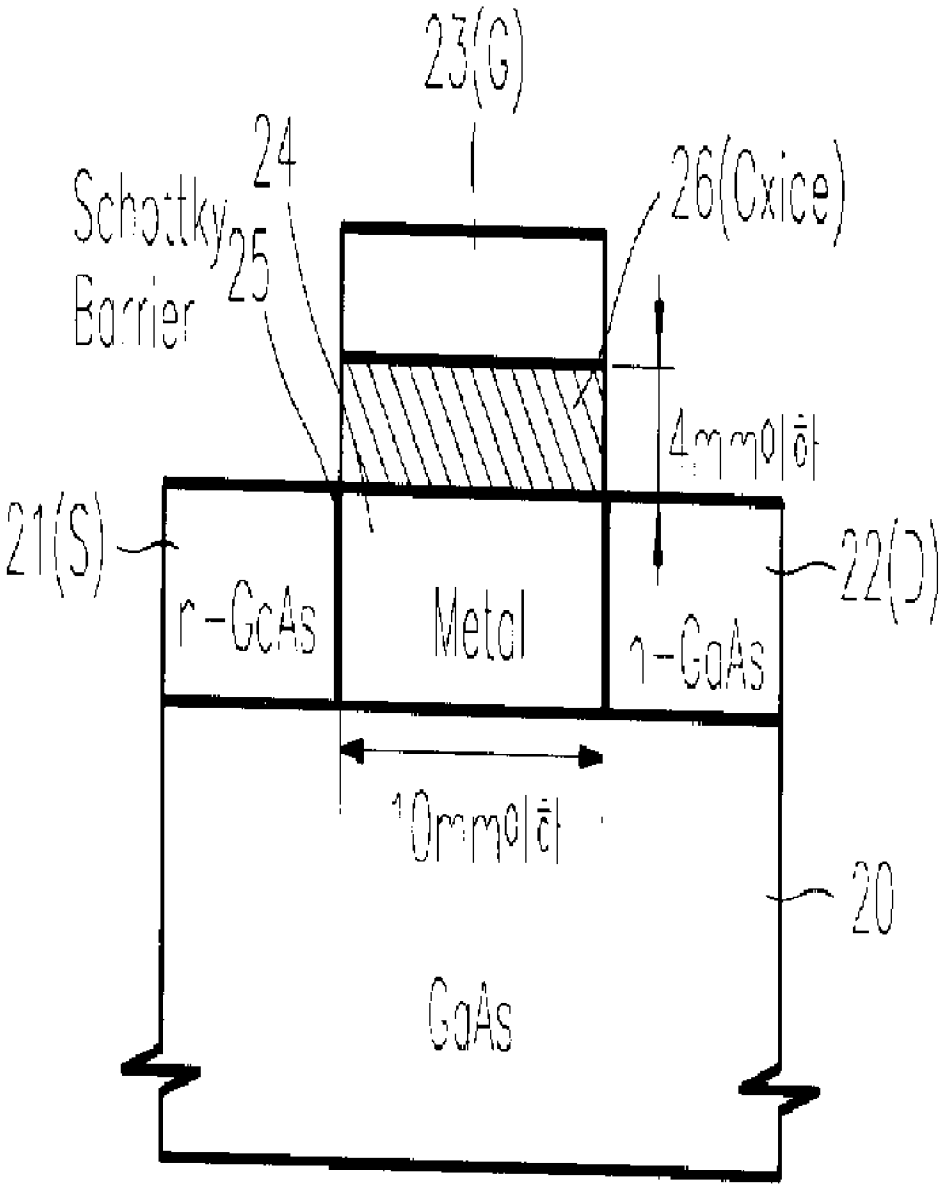
본발명은 반도체와 금속 접합시 자연적으로 형성되는 쇼트키 터널 장벽(Schottky tunnel barrier)을 터널 장벽으로 이용하는 단일 전자 트랜지스터(single electron transistor) 및 그 제조 방법에 관한 것이다. 본 발명에 따른 단일전자 트랜지스터에서는, 기존의 산화물을 터널장벽으로 이용하는 경우 문제가 되어 왔던 재현성 및 균일성을 획기적으로 개선하기 위해 금속과 반도체가 접합시 자연적으로 생기는 쇼트키 장벽을 터널 장벽으로 이용한다.

Abstract

The present invention relates to the single electron transistor using the formed Schottky tunnel barrier as the tunnel barrier in the semiconductor and metal junction and a manufacturing method thereof. The existing oxide in the single electron transistor according to the present invention can be used as the tunnel barrier the reproducibility which had been becoming a problem to the tunnel barrier in case the uses and the Schottky barrier in which the metal and semiconductor are naturally generated in the junction in order to conspicuously improve the uniformity.

대표도면(Representative drawing)

GF Exhibit 1124 - 2200/2704



청구의 범위

청구 1항:

반도체 기판;상기 반도체 기판 상부에 도전성 불순물이 도핑되어 형성된 소스 및 드레인;상기 소스 및 드레인 사이의 상기 반도체 기판 상에 금속으로 증착되어 상기 소스 및 드레인과의 경계면에 각각 쇼트키 베리어를 형성하는 아일런드;상기 아일런드 상에 형성된 절연층; 및상기 절연층 상에 형성된 게이트;를 구비한 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

Scope of Claims

Claim 1:

The single electron transistor using the Schottky tunnel barrier including the semiconductor substrate; the source and the drain in which the conductive is doped in the semiconductor substrate upper and which is formed; the island which is deposited on the semiconductor substrate between the drain and the source to the metal and forms the Schottky barrier on the boundary face between the source and the drain; the insulating layer formed on the island; and the gate formed on the insulating layer.

GF Exhibit 1124 - 2201/2704

청구 2항:

제1항에 있어서,상기 도전성 불순물은 n형 혹은 p형 불순물인 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

Claim 2:

As for claim 1, the single electron transistor in which the conductive uses the n-type or the Schottky tunnel barrier which is the p-type impurity.

청구 3항:

제2항에 있어서,상기 반도체 기판은 GaAs로 형성되고, 상기 소스 및 드레인은 각각 n-GaAs로 형성되며, 상기 절연층은 금속 산화물로 형성된 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

Claim 3:

The single electron transistor using the Schottky tunnel barrier of claim 2, wherein the semiconductor su bstrate is formed from the GaAs and the source and dr ain are formed from the insulating layer is the metal oxi de the respectively is formed with the n-GaAs.

청구 4항:

제1항에 있어서,상기 아일런드는 상기 기판 상부에 소정의 폭으로 도전성 불순물이 도핑된 반도체로 형성되고, 상기 소스 및 드레인은 상기 아일런드 양쪽의 상기 반도체 기판 상에 증착되어 상기 아일런드와의 경계면에 각각 쇼트키 베리어를 형성하도록 금속으로 형성되며, 상기 게이트는 상기 반도체 아일런드 상에 금속으로 증착되어 상기 반도체 아일런드와의 사경계면에 쇼트키 베리어가 형성된 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

Claim 4:

As for claim 1, the single electron transistor wherein the island is formed with the metal in order to form the Schottky barrier the source and drain are deposited on the semiconductor substrate of the island both sides it is formed with the semiconductor in which the conducti ve is doped in the substrate upside to the predetermin ed width, and gate uses the Schottky tunnel barrier wh ich is deposited on the above semiconductor island to t he metal and in which the Schottky barrier is formed in the deadly situation interface with the above semicond uctor island.

청구 5항:

제4항에 있어서,상기 도전성 불순물은 n형 혹은 p형 불순물인 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

Claim 5:

As for claim 4, the single electron transistor in which the conductive uses the n-type or the Schottky tunnel barrier which is the p-type impurity.

청구 6항:

제5항에 있어서,상기 반도체 기판은 GaAs로 형성되고, 상기 반도체 아일런드는 n-GaAs로 형성된 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

Claim 6:

The single electron transistor using the Schottky tunnel barrier of claim 5, wherein the semiconductor su bstrate is formed from the GaAs and the above semico nductor island are formed from the n-GaAs.

청구 7항:

(가) GaAs 기판 상에 도전성 불순물을 포함하는 GaAs층을 10nm 이하의 두께로 형성하는 단계;(나) 상기 도전성 불순물을 포함하는 GaAs층을 소정 폭을 갖는 세선들 및 소스들과 드레인들을 형성한 다음, 상기 세선들에서 각 단일 전자 트랜지스터의 아일런드 영역에 대응하는 영역들은 선택적으로 식각하여 아일런드들을 형성하는 단계; (다) 상기 아일런드 영역에 금속을 증착하여 상기 소스 및 드레인과의 접합면에 쇼트키 접합이 형성되도록 금속층을 형성하는 단계; (라) 상기 금속층 위에 두께 4 nm 이하의 유전체를 증착시켜 절연층을 형성하는 단계; 및(마) 상기 절연층 상에 금속을 증착시켜 게이트를 형성하는 단계;를포함하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

Claim 7:

(a) The manufacturing method of the single electron transistor using the Schottky tunnel barrier, wherein so urces like the force which has the fixed width the GaAs layer including the step : (b) conductive forming the G aAs layer including the conductive into the thickness le ss than 10nm on the GaAs substrate and *** which for ms drains ; and corresponds to fine lines with the islan d domain of each single electron transistor comprise th e step of forming islands, the step of depositing the me tal on (all) island domain and forming the metallic layer on the junction between the source and the drain to fo rm the Schottky barrier, and the step : (bad luck) it et ches the selectively, and the step : (bad luck) forms t he insulating layer on (at) metallic layer it evaporates t he dielectric less than the thickness 4 nm and the step of evaporating the metal on the insulating layer and for ming gate.

청구 8항:

Claim 8:

GF Exhibit 1124 - 2202/2704

제7항에 있어서,상기 (가) 단계에서 상기 도전성 불순물이 포함된 GaAs층은 호모 에피택시법으로 도핑 농도가 1020/cm3 이하로 조절되게 성장시키는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

As for claim 7, the manufacturing method of the single electron transistor using the Schottky tunnel barrier wh ich the GaAs layer in which in (a) step the conductive i s included grows so that the doping concentration be c ontrolled by the homo epitaxy method with 10 20 / cm 3 this harrow.

청구 9항:

Claim 9:

제7항에 있어서,상기 (가) 단계에서 상기 도전성 불순물을 포함하는 GaAs층은 성장중 소스 물질에 의하거나 혹은 GaAs 성장후 확산법 혹은 이온-주입법을 이용하여, 깊이 10 nm, 도핑 농도 1020/cm3 이하로 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

As for claim 7, the manufacturing method of the single electron transistor which is according to due to the so urce material among growth or in which the GaAs layer including the conductive in (a) step uses the Schottky tunnel barrier which 10 nm , and the doping chest deep ly form after the GaAs growth using the diffusion metho d or the ion implantation method with 10 20 / cm 3 this harrow.

청구 10항:

Claim 10:

제7항에 있어서,상기 (나) 단계에서 상기 세선들의 폭은 100nm이하로 형성하고, 상기 아일런드 영역은 10 nm 이하의 길이로 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

As for claim 7, the manufacturing method of the single electron transistor which the width of fine lines forms a t (b) step less than 100nm ; and uses the Schottky tu nnel barrier which the island domain forms into the leng th less than 10 nm.

청구 11항:

Claim 11:

제7항에 있어서,상기 (나) 단계에서 상기 세선들, 아일런드 영역, 소스 및 드레인은 리프트-오프 공정을 이용하여 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

As for claim 7, the manufacturing method of the single electron transistor using the Schottky tunnel barrier wh ich fine line the island domain , and the source and drai ns form at (b) step using the lift-off process.

청구 12항:

Claim 12:

제7항에 있어서,상기 (다) 단계에서 상기 쇼트키 접합의 장벽 높이는 1.0 eV 이하로 조절하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

As for claim 7, the manufacturing method of the single electron transistor in which the barrier height of the Sc hottky barrier uses the Schottky tunnel barrier controll ed in (all) step less than 1.0 eV.

청구 13항:

Claim 13:

제7항에 있어서,상기 (라) 단계에서 상기 절연층은 산화로에서 상기 금속층을 두께 4 nm 이하로 산화시킨 금속 산화막으로 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

As for claim 7, the manufacturing method of the single electron transistor using the Schottky tunnel barrier wh ich the insulating layer forms at (at) step into the meta l oxide layer oxidizing the metallic layer in the oxidation furnace less than the thickness 4 nm.

청구 14항:

Claim 14:

제7항에 있어서,상기 (가) 단계에서 상기 GaAs 기판 상에 금속층을 10nm 이하의 두께로 형성하고,상기 (나) 단계에서 상기 금속층을 소정 폭을 갖는 세선들 및 소스들과 드레인들을 형성한 다음, 상기 세선들에서 각 단일 전자 트랜지스터의 아일런드 영역에 대응하는 영역들을 선택적으로 선택적으로 식각하여 아일런드들을 형성하고, 상기 (다) 단계에서 상기 아일런드 영역에 도전성 불순물을 포함하는 GaAs층을 증착하여 상기 소스 및 드레인과의 접합면에 쇼트키 접합이 형성되도록 불순물 반도체층을 형성하며, 상기 (라) 단계를 없애고, 상기 (마) 단계에서 상기 불순물 반도체층 상에 금속을 증착시켜 게이트를 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

As for claim 7, the manufacturing method of sources like the force which has the fixed width the metallic lay er in (b) step it forms the metallic layer at (a) step on the GaAs substrate into the thickness less than 10nm a nd the single electron transistor which forms drains ; th e selectively selectively etches *** corresponding to fi ne lines with the island domain of each single electron t ransistor and it forms islands ; it deposits the GaAs lay er including the conductive on the island domain in (all) step and it forms the dopant semiconductor layer on th e junction between the source and the drain to form th e Schottky barrier ; it removes (at) step ; and uses th e Schottky tunnel barrier evaporating the metal at (ba d luck) step on the dopant semiconductor layer and for

GF Exhibit 1124 - 2203/2704

ms gate.

청구 15항:

Si 기판;상기 Si 기판 상에 도전성 불순물이 도핑된 반도체층으로 형성된 소스 및 드레인;상기 소스 및 드레인 사이의 상기 Si 기판 상에 금속으로 증착되어 상기 소스 및 드레인과의 경계면에 각각 쇼트키 베리어를 형성하는 아일런드;상기 아일런드 상에 형성된 절연층; 및상기 절연층 상에 형성된 게이트;를구비한 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

Claim 15:

The single electron transistor using the Schottky tunnel barrier including the Si substrate; the source and the drain formed into the semiconductor layer in which the conductive is doped on the Si substrate; the island which is deposited on the Si substrate between the drain and the source to the metal and forms the Schottky barrier on the boundary face between the source and the drain; the insulating layer formed on the island; and the gate formed on the insulating layer.

청구 16항:

제15항에 있어서,상기 도전성 불순물은 n형 혹은 p형 불순물인 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

Claim 16:

As for claim 15, the single electron transistor in which the conductive uses the n-type or the Schottky tunnel barrier which is the p-type impurity.

청구 17항:

제16항에 있어서,상기 소스 및 드레인은 각각 n-SiGe 혹은 p-SiGe로 형성되며, 상기 절연층은 SiO2로 형성된 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

Claim 17:

As for claim 16, the source and drain is the n-SiGe or the single electron transistor which is formed with the p-SiGe ; and uses the Schottky tunnel barrier in which the insulating layer is formed with the SiO 2 .

청구 18항:

제15항에 있어서,상기 소스 및 드레인은 금속으로 형성되고, 상기 금속 소스와 Si 기판 사이 및 상기 금속 드레인과 Si 기판 사이에는 상기 Si 기판의 상부를 각각 선택적으로 산화시켜 형성된 제1절연층 및 제2절연층을 더 구비하며, 상기 아일런드는 상기 금속 소스 및 금속 드레인과의 경계면에 쇼트키 베리어가 형성되도록 도전성 불순물이 도핑된 반도체 화합물로 형성한 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

Claim 18:

As for claim 15, the single electron transistor wherein the source and drain further include the first insulation layer and the second insulation layer which is formed in to the metal ; and it selectively oxidizes the upper portion of the Si substrate and is formed between the metal source, the Si substrate interval, the metal drain and Si substrate, and the island use the Schottky tunnel barrier formed into the semiconductor compound in which the conductive is doped so that the Schottky barrier is formed in the boundary face between the metal source and the metal drain.

청구 19항:

제18항에 있어서,상기 반도체 아일런드는 n-SiGe 혹은 p-SiGe로 형성된 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

Claim 19:

As for claim 18, the single electron transistor in which the above semiconductor island uses the n-SiGe or the Schottky tunnel barrier formed with the p-SiGe.

청구 20항:

제18항에 있어서,상기 반도체 아일런드 상에 상기 절연층을 형성하지 않고 바로 상기 금속 게이트를 형성하여 상기 반도체 아일런드와의 경계면에 쇼트키 베리어를 형성한 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

Claim 20:

As for claim 18, the single electron transistor using the Schottky tunnel barrier which does not form the insulating layer on the above semiconductor island and forms immediately, the metal gate and forms the Schottky barrier on the boundary face with the above semiconductor island.

청구 21항:

제20항에 있어서,상기 반도체 아일런드는 n-SiGe 혹은 p-SiGe로 형성된 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터.

Claim 21:

As for claim 20, the single electron transistor in which the above semiconductor island uses the n-SiGe or the Schottky tunnel barrier formed with the p-SiGe.

청구 22항:

Claim 22:

GF Exhibit 1124 - 2204/2704

(가) Si 기판 상에 도전성 불순물을 포함하는 Si-Ge층을 10nm 이하의 두께로 형성하는 단계; (나) 상기 도전성 불순물을 포함하는 Si-Ge층을 소정 폭을 갖는 세선들 및 소스들과 드레인들을 형성한 다음, 상기 세선들에서 각 단일 전자 트랜지스터의 아일런드 영역에 대응하는 영역들을 선택적으로 식각하여 아일런드들을 형성하는 단계; (다) 상기 아일런드 영역에 금속을 증착하여 상기 소스 및 드레인과의 접합면에 쇼트키 접합이 형성되도록 금속층을 형성하는 단계; (라) 상기 금속층 위에 두께 4 nm 이하의 유전체를 증착시켜 절연층을 형성하는 단계; 및(마) 상기 절연층 상에 금속을 증착시켜 게이트를 형성하는 단계;를포함하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

(a) The manufacturing method of sources like the force having the fixed width the Si-Ge layer including (b) conductive step of forming the Si-Ge layer including the conductive into the thickness less than 10nm on the Si substrate and the single electron transistor which forms drains ; and uses the Schottky tunnel barrier which comprises the step: step: step : (bad luck) evaporating the dielectric less than the thickness 4 nm and forms the insulating layer on (at) metallic layer and the step of evaporating the metal on the insulating layer and forming gate of depositing the metal on (all) island domain and forming the metallic layer on the junction between the source and the drain to form the Schottky barrier of the selectively etching *** corresponding to fine lines with the island domain of each single electron transistor and forming islands.

청구 23항:

제22항에 있어서,상기 (가) 단계에서 상기 도전성 불순물을 포함하는 Si-Ge층은 에피택시법으로 도핑 농도를 1020/cm3 이하로 성장시키는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

Claim 23:

As for claim 22, the manufacturing method of the single electron transistor using the Schottky tunnel barrier in which the Si-Ge layer including the conductive in (a) step grows the doping concentration to the epitaxy method with 10 20 / cm 3 this harrow.

청구 24항:

제22항에 있어서,상기 (가) 단계에서 상기 도전성 불순물을 포함하는 Si-Ge층은 성장시 소스 물질에 의하거나 혹은 성장후 확산법 혹은 이온-주입법을 이용하여, 깊이 10 nm, 도핑 농도 1020/cm3 이하로 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

Claim 24:

As for claim 22, the manufacturing method of the single electron transistor which is according to due to the grown in source material or in which the Si-Ge layer including the conductive in (a) step uses the Schottky tunnel barrier which 10 nm , and the doping chest deeply form after growth using the diffusion method or the ion implantation method with 10 20 / cm 3 this harrow.

청구 25항:

제22항에 있어서,상기 (나) 단계에서 상기 세선들의 폭은 100nm이하로 형성하고, 상기 아일런드 영역은 10 nm 이하의 길이로 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

Claim 25:

As for claim 22, the manufacturing method of the single electron transistor which the width of fine lines forms at (b) step less than 100nm ; and uses the Schottky tunnel barrier which the island domain forms into the length less than 10 nm.

청구 26항:

제22항에 있어서,상기 (나) 단계에서 상기 세선들, 아일런드 영역, 소스 및 드레인은 리프트-오프 공정을 이용하여 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

Claim 26:

As for claim 22, the manufacturing method of the single electron transistor using the Schottky tunnel barrier which fine line the island domain , and the source and drains form at (b) step using the lift-off process.

청구 27항:

제22항에 있어서,상기 (다) 단계에서 상기 쇼트키 접합의 장벽 높이는 1.0 eV 이하로 조절하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

Claim 27:

As for claim 22, the manufacturing method of the single electron transistor in which the barrier height of the Schottky barrier uses the Schottky tunnel barrier controlled in (all) step less than 1.0 eV.

청구 28항:

제22항에 있어서,상기 (라) 단계에서 상기 절연층은 산화로에서 상기 금속층을 두께 4 nm 이하로 산화시킨 금속 산화막으로 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

Claim 28:

As for claim 22, the manufacturing method of the single electron transistor using the Schottky tunnel barrier which the insulating layer forms at (at) step into the metal oxide layer oxidizing the metallic layer in the oxidation furnace less than the thickness 4 nm.

GF Exhibit 1124 - 2205/2704

청구 **29**항:

제22항에 있어서,상기 (가) 단계에서 상기 Si 기판 상에 SiO2막을 형성한 다음, 상기 SiO2막 상에 금속층을 10nm 이하의 두께로 형성하고, 상기 (나) 단계에서 상기 금속층 및 SiO2막을 소정 폭을 갖는 세선들 및 소스들과 드레인들을 형성한 다음, 상기 세선들에서 각 단일 전자 트랜지스터의 아일런드에 대응하는 영역들을 선택적으로 식각하여 아일런드들을 형성하고, 상기 (다) 단계에서 상기 아일런드 영역에 도전성 불순물을 포함하는 Si-Ge층을 증착하여 상기 소스 및 드레인과의 접합면에 쇼트키 접합이 형성되도록 불순물 반도체층을 형성하며, 상기 (라) 단계에서 상기 불순물 반도체층 상에 절연층을 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

Claim 29:

As for claim 22, the manufacturing method of sources like the force which has the fixed width the metallic layer and SiO 2 film in (b) step it forms the metallic layer into the thickness less than 10nm on the SiO 2 film it forms the SiO 2 film at (a) step on the Si substrate and the single electron transistor which forms drains ; the selectively etches *** corresponding to fine lines with the island of each single electron transistor and it forms islands ; it deposits the Si-Ge layer including the conductive on the island domain in (all) step and it forms the dopant semiconductor layer on the junction between the source and the drain to form the Schottky barrier ; and uses the Schottky tunnel barrier forming the insulating layer at (at) step on the dopant semiconductor layer.

청구 **30**항:

제22항에 있어서,상기 (가) 단계에서 상기 Si 기판 상에 SiO2막을 형성한 다음, 상기 SiO2막 상에 금속층을 10nm 이하의 두께로 형성하고, 상기 (나) 단계에서 상기 금속층 및 SiO2막을 소정 폭을 갖는 세선들 및 소스들과 드레인들을 형성한 다음, 상기 세선들에서 각 단일 전자 트랜지스터의 아일런드들에 대응하는 영역들을 선택적으로 식각하여 아일런드들을 형성하고, 상기 (다) 단계에서 상기 아일런드 영역에 도전성 불순물을 포함하는 Si-Ge층을 증착하여 상기 소스 및 드레인과의 접합면에 쇼트키 접합이 형성되도록 불순물 반도체층을 형성하며, 상기 (라) 단계를 없애고 상기 (마) 단계에서 상기 불순물 반도체층 상에 금속을 증착하여 게이트를 형성하는 것을 특징으로 하는 쇼트키 터널 장벽을 이용한 단일 전자 트랜지스터의 제조 방법.

Claim 30:

As for claim 22, the manufacturing method of sources like the force which has the fixed width the metallic layer and SiO 2 film in (b) step it forms the metallic layer into the thickness less than 10nm on the SiO 2 film it forms the SiO 2 film at (a) step on the Si substrate and the single electron transistor which forms drains ; the selectively etches *** corresponding to fine lines with the islands of each single electron transistor and it forms islands ; it deposits the Si-Ge layer including the conductive on the island domain in (all) step and it forms the dopant semiconductor layer on the junction between the source and the drain to form the Schottky barrier ; and uses the Schottky tunnel barrier removing (at) step and deposits the metal in (bad luck) step on the dopant semiconductor layer and forms gate.

배경기술

본발명은 반도체와 금속 접합시 자연적으로 형성되는 쇼트키 터널 장벽(Schottky tunnel barrier)을 터널 장벽으로 이용한 단일 전자 트랜지스터(single electron transistor) 및 그 제조 방법에 관한 것이다.

도 1a 및 도 1b는 종래의 단일 전자 트랜지스터들의 개략적 수직 단면도이다. 종래의 단일 전자 트랜지스터는, 도 1a에 도시된 바와 같이, 실리콘 기판(1) 상에 소스(source)(2)와 드레인(drain)(3) 사이에 2개의 터널 장벽(tunnel barrier)(5)을 만들어 아일런드(island)(4)를 형성시킨 구조이거나, 혹은 도 1b에 도시된 바와 같이, 실리콘 기판(11a) 상에 SiO2 절연막(11b)를 형성한 SOI 기판(11) 상면에 소스(12)와 드레인(13)을 형성한 후, 유전체(15) 속에 금속이나 반도체를 물리적(예, PVD) 혹은 화학적(예, CVD) 증착을 통해 나노미터(nm) 크기인 알갱이(granular) 모양의 아일런드(14)를 형성시킨 구조이다.

그러나, 참고 문헌 T.Wada etal Jpn.J.Appl.Phys 34,12B (1995)6961에 따르면, 도 1a에 도시된 바와 같은 단일 전자 트랜지스터의 경우 아일런드(15)의 크기를 나노미터 크기로 균일하게 제어하는 것이 매우 어렵다. 특히, 전자빔 리소그래

Background Art

The present invention relates to the single electron transistor using the formed Schottky tunnel barrier as the tunnel barrier in the semiconductor and metal juntion and a manufacturing method thereof.

Figures 1a and 1b are an approximate vertical cross section of conventional single electron transistors. The conventional single electron transistor may be the structure of making the tunnel barrier (tunnel barrier) (5) of 2 and as shown in FIG. 1a, forming the island (island) (4) on the silicon substrate (1) between the source (source) (2) and drain (drain) (3). And or, as shown in FIG. 1b, it is the source (12) and drain (13) the structure of forming the island (14) which is the nanometer (nm) size through Lee (the example, and PVD) or chemical (the example, and CVD) deposition of the granule (granular) shape the metal or the semiconductor in the dielectric (15) in the SOI substrate (11) upper side forming the SiO 2 insulating layer (11b) on the silicon substrate (11a) after doing the formation.

But according to the reference T Wada. etal Jpn J. Appl. Phys. 34,12 B (1995) 6961, the size is difficult in case of the single electron transistor as illustrated in Figure 1a to uniformly control the size of the island (15)

GF Exhibit 1124 - 2206/2704

피(E-beam lithography) 공정을 이용시 터널장벽을 형성키 위해 많은 공정을 거쳐야 하며 상온에서 작동하는 아일런드의 크기를 제어하는 것은 거의 불가능하다. 또한, K.Matsumoto et al Appl.Phys.Lett 68(1996)34에 따르면, SPM(scanning probe microscopy)을 응용할 경우 터널 장벽이 공기중에서 열화되기 때문에 단일 전자 트랜지스터의 작동 재현성이 전혀 없다. 그리고 참고문헌 W.Chen etal Appl.Phys.Lett 66(1995)3383 및 A.Dutta etal Jpn.J.Appl.Phys 36,6B(1997)4038에 의하면, 도 1b에 도시된 바와 같은 단일 전자 트랜지스터의 경우, 아일런드(14)의 숫자를 결정하는 소스(12)와 드레인(13) 사이의 거리를 재현성 있게 제어하기도 어렵고 공정 자체도 복잡하여 제조상 어려움이 따른다. 따라서 재현성있는 상온 작동 단일 전자 트랜지스터를 구현하기 위해서는 공정이 간단하며 아일런드의 크기를 나노미터 크기로 쉽게 제어할 수 있는 새로운 구조 및 제조 방법이 요구된다.

to the nano size. Especially, it is nearly impossible to control the size of the island operating at a room temperature while being fair the electron beam lithography (E-beam lithography) process after the process of being many in order to form on using tunnel barrier. Moreover, according to K Matsumoto. et al Appl Phys. Lett. 68 (1996) 34, in case of applying the SPM (scanning probe microscopy) because the tunnel barrier is degraded in the airborne there is no operation reproducibility of the single electron transistor at all. And according to the reference W Chen. etal Appl Phys. Lett. 66 (1995) 3383 and A Dutta. etal Jpn J. Appl. Phys. 36,6 B (1997) 4038, it is difficult in case of the single electron transistor as illustrated in Figure 1b that the distance have the distance between the drain (13) determining the number of the island (14) and the source (12) are controlled and the process itself is complicated and the aspect of manufacturing difficulty follows. Therefore, the structure of being new of easily controlling the size of the island to the nano size the process is simple it implements the room temperature operation single electron transistor having and a manufacturing method thereof are required.

발명의 내용

Summary of Invention

발명의 효과

Effects of the Invention

이상 설명한 바와 같이, 본 발명에 따른 단일전자 트랜지스터에서는, 기존의 산화물을 터널장벽으로 이용하는 공정으로는 상온에서 작동하기 위해 단일전자 트랜지스터의 아일런드의 크기를 10 nm 정도로 재현성 있게 제한해야 하는 어려움을 극복하기 위하여, 금속과 반도체가 접합시 자연적으로 생기는 쇼트키 장벽을 터널 장벽으로 이용하는 점에 특징이 있다. 기존의 단일전자 트랜지스터 제조시에는 산화물을 터널장벽으로 형성하기 위해 많은 제조 공정을 거쳐야 하며, 또한 많은 공정을 거친다 하더라도 아일런드 크기의 재현성을 보장할 수 없었다. 본 발명은 이러한 난점을 쇼트키 장벽을 터널 장벽으로 이용함으로써 상기 두 가지 문제를 크게 개선한다. 더욱이, 아일런드 크기를 nm 단위로 쉽게 제어할 수 있기 때문에 상온 작동이 가능하며 터널 장벽의 열화가 없어 오랫동안 신뢰성 있는 소자로서 작동할 수 있다. 따라서, 본 발명에 의해 제작된 단일전자 트랜지스터는 상온작동 1 Tb 급 메모리 및 로직소자에 응용된다

As described above, in the single electron transistor according to the present invention, in order that the difficulty the size has of to limiting the size of the island of the single electron transistor to about 10 nm in order to operate to the process of using the existing oxide as the tunnel barrier at a room temperature, is overcome the characteristic is in the point using the Schottky barrier in which the metal and semiconductor are naturally generated in the junction as the tunnel barrier. It did in the existing single electron transistor manufacturing after the manufacturing process of being many the oxide was formed into the tunnel barrier and although the justice of being moreover many was passed through the reproducibility of the island size could not be guaranteed. The crux in which the invention is like that is used as the tunnel barrier the Schottky barrier. And two kinds of problem is significantly. Furthermore, because the island size can be easily controlled by unit of the nm the room temperature operation is possible and there is no deterioration of the tunnel barrier and it can operate as the device having reliability for a long time. Therefore, the single electron transistor manufactured by the invention is applied to the room temperature operation 1 Tb class memory and logic device

기술적 과제

Technical Task

본발명은 상기와 같은 문제점을 개선하기 위하여 창안된 것으로, 반도체와 금속 접합시 자연적으로 형성되는 쇼트키 터널 장벽(Schottky tunnel barrier)을 터널 장벽으로 이용하여 재현성 및 균일성을 개선한 단일 전자 트랜지스터 및 그 제조 방법을 제공하는데 그 목적이 있다.

An object of the present invention is to provide the single electron transistor which is founded in order to improve and improves the reproducibility and uniformity by using the formed Schottky tunnel barrier as the tunnel barrier in the semiconductor and metal juntion and a manufacturing method thereof the above-mentioned problem.

GF Exhibit 1124 - 2207/2704

발명의 구성 및 작용

상기와 같은 목적을 달성하기 위하여 본 발명에 따른 단일 전자 트랜지스터는, 반도체 기판; 상기 반도체 기판 상부에 도전성 불순물이 도핑되어 형성된 소스 및 드레인; 상기 소스 및 드레인 사이의 상기 반도체 기판 상에 금속으로 증착되어 상기 소스 및 드레인과의 경계면에 각각 쇼트키 베리어를 형성하는 아일런드; 상기 아일런드 상에 형성된 절연층; 및 상기 절연층 상에 형성된 게이트;를 구비한 것을 특징으로 한다.

본 발명에 있어서, 상기 반도체 기판은 GaAs로 형성되고, 상기 소스 및 드레인은 각각 n-GaAs로 형성되며, 상기 절연층은 금속 산화물로 형성된 것이 바람직하며, 상기 아일런드는 상기 기판 상부에 소정의 폭으로 도전성 불순물이 도핑된 반도체로 형성되고, 상기 소스 및 드레인은 상기 아일런드 양쪽의 상기 반도체 기판 상에 증착되어 상기 아일런드와의 경계면에 각각 쇼트키 베리어를 형성하도록 금속으로 형성되며, 상기 게이트는 상기 반도체 아일런드 상에 금속으로 증착되어 상기 반도체 아일런드와의 사경계면에 쇼트키 베리어가 형성된 것도 바람직하다.

또한, 상기와 같은 목적을 달성하기 위하여 본 발명에 따른 단일 전자 트랜지스터의 제조 방법은, (가) GaAs 기판 상에 도전성 불순물을 포함하는 GaAs층을 10nm 이하의 두께로 형성하는 단계; (나) 상기 도전성 불순물을 포함하는 GaAs층을 소정 폭을 갖는 세선들 및 소스들과 드레인들을 형성한 다음, 상기 세선들에서 각 단일 전자 트랜지스터의 아일런드 영역에 대응하는 영역들을 선택적으로 식각하여 아일런드들을 형성하는 단계; (다) 상기 아일런드 영역에 금속을 증착하여 상기 소스 및 드레인과의 접합면에 쇼트키 접합이 형성되도록 금속층을 형성하는 단계; (라) 상기 금속층 위에 두께 4 nm 이하의 유전체를 증착시켜 절연층을 형성하는 단계; 및 (마) 상기 절연층 상에 금속을 증착시켜 게이트를 형성하는 단계;를 포함하는 것을 특징으로 한다.

본 발명에 있어서, 상기 (가) 단계에서 상기 도전성 불순물을 포함하는 GaAs층은 호모 에피택시법으로 도핑 농도를 1020/cm3 이하로 성장시키거나 확산법 혹은 이온-주입법을 이용하여, 깊이 10 nm, 도핑 농도 1020/cm3 이하로 형성하며, 상기 (나) 단계에서 상기 세선들의 폭은 100nm이하로 형성하고, 상기 아일런드 영역은 10 nm 이하의 길이로 형성하며, 상기 (다) 단계에서 상기 쇼트키 접합의 장벽 높이는 1.0 eV 이하로 조절하며, 상기 (라) 단계에서 상기 절연층은 산화로에서 상기 금속층을 두께 4 nm 이하로 산화시킨 금속 산화막으로 형성하는 것이 바람직하며,

상기 (가) 단계에서 상기 GaAs 기판 상에 금속층을 10nm 이하의 두께로 형성하고, 상기 (나) 단계에서 상기 금속층을 소정 폭을 갖는 세선으로 형성한 다음, 상기 세선들에서 각 단일 전

Structure & Operation of the Invention

To achieve the object, the single electron transistor according to the present invention comprises the semiconductor substrate; the source and the drain in which the conductive is doped in the semiconductor substrate upper and which is formed; the source; and the island: insulating layer: formed on the island and the gate formed on the insulating layer forms the Schottky barrier on the boundary face between the source and the drain it is deposited on the semiconductor substrate between the drain to the metal.

In the present invention, the semiconductor substrate is formed with the GaAs and the respectively the source and drain are formed with the n-GaAs and the be desirable, the island is formed with the semiconductor in which the conductive is doped in the substrate upside to the predetermined width that the insulating layer is formed with the metal oxide and the source and drain are formed into the metal so that it is deposited on the semiconductor substrate of the island both sides and the source and drain form the Schottky barrier on the boundary face with the island and it is the be desirable that gate is deposited on the above semiconductor island to the metal and the Schottky barrier is formed in the deadly situation interface with the above semiconductor island.

Moreover, to achieve the object, it comprises the step that the manufacturing method of the single electron transistor according to the present invention forms the GaAs layer including the conductive into the thickness less than 10nm on (a) GaAs substrate; sources like the force having the fixed width the GaAs layer including (b) conductive and the step after it forms drains of the selectively etching *** corresponding to fine lines with the island domain of each single electron transistor and forming islands; the step of depositing the metal on (all) island domain and forming the metallic layer on the junction between the source and the drain to form the Schottky barrier; and the step of forming the insulating layer, and the step of evaporating the metal on (bad luck) insulating layer and forming gate the dielectric less than the thickness 4 nm is evaporated on (at) metallic layer.

In the present invention, the be desirable the insulating layer forms on (at) step into the metal oxide layer oxidizing the metallic layer in the oxidation furnace less than the thickness 4 nm the GaAs layer including the conductive in (a) step grows the doping concentration to the homo epitaxy method with 10 20 / cm 3 this harrow or 10 nm , and the doping chest deeply form using the diffusion method or the ion implantation method with 10 20 / cm 3 this harrow and the width of fine lines forms at (b) step less than 100nm and the island domain forms into the length less than 10 nm and the barrier height of the Schottky barrier controls at (all) step less than 1.0 eV

In (a) step, the metallic layer is formed into the thickness less than 10nm on the GaAs substrate and after the metallic layer is formed at (b) step into the fine

GF Exhibit 1124 - 2208/2704

자 트랜지스터의 아일런드 영역에 대응하는 영역들을 선택적으로 식각하여 아일런드들을 형성하고, 상기 (다) 단계에서 상기 아일런드 영역에 도전성 불순물을 포함하는 GaAs층을 증착하여 상기 소스 및 드레인과의 접합면에 쇼트키 접합이 형성되도록 불순물 반도체층을 형성하며, 상기 (라) 단계를 없애고, 상기 (마) 단계에서 상기 불순물 반도체층 상에 금속을 증착시켜 게이트를 형성하는 것도 바람직하다.

line having the fixed width *** corresponding to fine lines with the island domain of each single electron transistor the selectively is etched and islands are formed and the GaAs layer including the conductive is deposited on the island domain in (all) step and the dopant semiconductor layer is formed on the junction between the source and the drain to form the Schottky barrier and (at) step is removed and it is the be desirable to evaporate the metal at (bad luck) step on the dopant semiconductor layer and form gate.

또한, 상기와 같은 목적을 달성하기 위하여 본 발명에 따른 또 다른 단일 전자 트랜지스터는, Si 기판; 상기 Si 기판 상에 도전성 불순물이 도핑된 반도체층으로 형성된 소스 및 드레인; 상기 소스 및 드레인 사이의 상기 Si 기판 상에 금속으로 증착되어 상기 소스 및 드레인과의 경계면에 각각 쇼트키 베리어를 형성하는 아일런드; 상기 아일런드 상에 형성된 절연층; 및 상기 절연층 상에 형성된 게이트;를 구비한 것을 특징으로 한다.

Moreover, to achieve the object, another single electron transistor according to the present invention comprises the Si substrate; the source and the drain formed into the semiconductor layer in which the conductive is doped on the Si substrate; the source; and the island: insulating layer: formed on the island and the gate formed on the insulating layer forms the Schottky barrier on the boundary face between the source and the drain it is deposited on the Si substrate between the drain to the metal.

본 발명에 있어서, 상기 소스 및 드레인은 각각 n-SiGe 혹은 p-SiGe로 형성되고 상기 절연층은 SiO2로 형성된 것이 바람직하며, 상기 소스 및 드레인은 금속으로 형성되고, 상기 금속 소스와 Si 기판 사이 및 상기 금속 드레인과 Si 기판 사이에는 상기 Si 기판의 상부를 각각 선택적으로 산화시켜 형성된 제1절연층 및 제2절연층을 더 구비하며, 상기 아일런드는 상기 금속 소스 및 금속 드레인과의 경계면에 쇼트키 베리어가 형성되도록 도전성 불순물이 도핑된 반도체 화합물로 형성한 것도 바람직하다.

In the present invention, the be desirable, the source and drain are formed with the metal that the respectively the source and drain are formed with the n-SiGe or the p-SiGe and the insulating layer is formed into the SiO 2 and the first insulation layer and the second insulation layer which selectively oxidizes the upper portion of the Si substrate and is formed are further between the metal source, the Si substrate interval, the metal drain and Si substrate and it is the be desirable that the island forms into the A -doped semiconductor compound the conductive so that the Schottky barrier is formed in the boundary face between the metal source and the metal drain.

또한 본 발명에 있어서, 상기 반도체 아일런드 상에 상기 절연층을 형성하지 않고 바로 상기 금속 게이트를 형성하여 상기 반도체 아일런드와의 경계면에 쇼트키 베리어를 형성한 것도 바람직하다.

Moreover, in the present invention, it is the be desirable not to form the insulating layer on the above semiconductor island and immediately, the metal gate be formed and form the Schottky barrier on the boundary face with the above semiconductor island.

또한, 상기와 같은 목적을 달성하기 위하여 본 발명에 따른 단일 전자 트랜지스터의 제조 방법은, (가) Si 기판 상에 도전성 불순물을 포함하는 Si-Ge층을 10nm 이하의 두께로 형성하는 단계; (나) 상기 도전성 불순물을 포함하는 Si-Ge층을 소정 폭을 갖는 세선들 및 소스들과 드레인들을 형성한 다음, 상기 세선들에서 각 단일 전자 트랜지스터의 아일런드 영역에 대응하는 영역들을 선택적으로 식각하여 아일런드들을 형성하는 단계; (다) 상기 아일런드 영역에 금속을 증착하여 상기 소스 및 드레인과의 접합면에 쇼트키 접합이 형성되도록 금속층을 형성하는 단계; (라) 상기 금속층 위에 두께 4 nm 이하의 유전체를 증착시켜 절연층을 형성하는 단계; 및 (마) 상기 절연층 상에 금속을 증착시켜 게이트를 형성하는 단계;를 포함하는 것을 특징으로 한다.

Moreover, to achieve the object, it comprises the step that the manufacturing method of the single electron transistor according to the present invention forms the Si-Ge layer including the conductive into the thickness less than 10nm on (a) Si substrate; sources like the force having the fixed width the Si-Ge layer including (b) conductive and the step after it forms drains of the selectively etching *** corresponding to fine lines with the island domain of each single electron transistor and forming islands; the step of depositing the metal on (all) island domain and forming the metallic layer on the junction between the source and the drain to form the Schottky barrier; and the step of forming the insulating layer, and the step of evaporating the metal on (bad luck) insulating layer and forming gate the dielectric less than the thickness 4 nm is evaporated on (at) metallic layer.

본 발명에 있어서, 상기 (가) 단계에서 상기 도전성 불순물을 포함하는 Si-Ge층은 에피택시법으로 도핑 농도를 1020/cm3 이하로 성장시키거나 혹은 성장시 소스 물질에 의하거나 혹은 성장후 확산법 혹은 이온-주입법을 이용하여, 깊이 10 nm, 도핑 농도 1020/cm3 이하로 형성하며, 상기 (나) 단계에서 상

In the present invention, in (a) step, whether the Si-Ge layer including the conductive grows the doping concentration to the epitaxy method with 10 20 / cm 3 this harrow or it is according to due to the grown in source material or 10 nm , and the doping chest deeply form

GF Exhibit 1124 - 2209/2704

기 세선들의 폭은 100nm이하로 형성하고, 상기 아일런드 영역은 10 nm 이하의 길이로 형성하며, 상기 (다) 단계에서 상기 쇼트키 접합의 장벽 높이는 1.0 eV 이하로 조절하며, 상기 (라) 단계에서 상기 절연층은 산화로에서 상기 금속층을 두께 4 nm 이하로 산화시킨 금속 산화막으로 형성하는 것이 바람직하며, 상기 (가) 단계에서 상기 Si 기판 상에 SiO2막을 형성한 다음, 상기 SiO2막 상에 금속층을 10nm 이하의 두께로 형성하고, 상기 (나) 단계에서 상기 금속층 및 SiO2막을 소정 폭을 갖는 세선들 및 소스들과 드레인들을 형성한 다음, 상기 세선들에서 각 단일 전자 트랜지스터의 아일런드 영역에 대응하는 영역들을 선택적으로 식각하여 아일런드들을 형성하고, 상기 (다) 단계에서 상기 아일런드 영역에 도전성 불순물을 포함하는 Si-Ge층을 증착하여 상기 소스 및 드레인과의 접합면에 쇼트키 접합이 형성되도록 불순물 반도체층을 형성하며, 상기 (라) 단계에서 상기 불순물 반도체층 상에 절연층을 형성하거나, 상기 (라) 단계를 없애고 상기 (마) 단계를 바로 실시하여 상기 불순물 반도체층 상에 바로 금속을 증착하여 게이트를 형성하는 것이 바람직하다.

after growth using the diffusion method or the ion implantation method with 10 20 / cm 3 this harrow and the width of fine lines forms on (b) step less than 100nm and the island domain forms into the length less than 10 nm and the barrier height of the Schottky barrier controls at (all) step less than 1.0 eV and after the SiO 2 film is formed at the be desirable, (a) step on the Si substrate that the insulating layer forms at (at) step into the metal oxide layer oxidizing the metallic layer in the oxidation furnace less than the thickness 4 nm the metallic layer is formed into the thickness less than 10nm on the SiO 2 film and after sources and drains are formed at (b) step like the force having the fixed width the metallic layer and SiO 2 film *** corresponding to fine lines with the island domain of each single electron transistor the selectively is etched and islands are formed In (all) step, the Si-Ge layer including the conductive is deposited on the island domain and the dopant semiconductor layer is formed on the junction between the source and the drain to form the Schottky barrier and the insulating layer is formed at (at) step on the dopant semiconductor layer or it is the be desirable to remove (at) step and (the bad luck) step be immediately performed and immediately, the metal be deposited on the dopant semiconductor layer and form gate.

이하 본 발명에 따른 단일 전자 트랜지스터의 여러 가지 실시예 및 그 제조 방법을 상세하게 설명한다.

Hereinafter, specifically various embodiments and a manufacturing method thereof of the single electron transistor according to the present invention are illustrated.

본 발명에 따른 단일 전자 트랜지스터는 반도체와 금속 접합시 자연적으로 형성되는 쇼트키 터널 장벽(Schottky tunnel barrier)을 터널 장벽으로 이용함으로써, 기존의 산화물 터널 장벽(tunnel barrier)을 응용한 단일 전자 트랜지스터 제조시 기본적으로 문제가 된 재현성 및 균일성을 획기적으로 개선하고 제조 공정을 용이하게 한 점에 특징이 있다. 이러한 반도체-금속 접합의 쇼트키 터널장벽을 이용하여 단일 전자 트랜지스터를 제조하면 상온 작동이 가능하며 이를 응용하여 차세대 초고집적(1 Terra bit) 메모리 및 로직에 응용할 수 있다. 이러한 특징들을 도 2 내지 도 6을 참조하여 상세하게 설명하면 다음과 같다.

The Schottky tunnel barrier in which the single electron transistor according to the present invention is naturally formed in the semiconductor and metal juntion are used as the tunnel barrier. And it has the characteristic in the reproducibility which becomes elementarily a problem in the single electron transistor manufacturing applying the existing oxide tunneling barrier (tunnel barrier) and the point which conspicuously improves the uniformity and facilitates the manufacturing process. If the single electron transistor is manufactured using the Schottky tunnel barrier of such semiconductor - metal junction, the room temperature operation is possible and this is applied and it can apply to the ULSI (1 Terra bit) memory and logic. Such characteristics is made to be equal to referring to figures 2 through 6, specifically, the next.

도 2는 본 발명에 따른 단일 전자 트랜지스터 제1실시예의 개략적인 수직 단면도이다. 도시된 바와 같이, 제1실시예는 GaAs 반도체 기판(20) 상에 n-GaAs 소스(21) 및 n-GaAs 드레인(22) 사이에 금속층(24)이 삽입된 트랜지스터 구조물이 적층되고, 금속층(24) 상에 산화물층(26) 및 게이트(23)가 순차로 적층된 구조로 형성된다. 따라서, n-GaAs 소스(21)와 금속층(24)의 접합면 및 n-GaAs 드레인(22)과 금속층(24)의 접합면에는 각각 쇼트키 장벽(25)이 형성된다.

Figure 2 is a summary vertical side view of the single electron transistor first preferred embodiment according to the invention. As shown in the figure, the transistor structure water in which as to the first preferred embodiment, the metallic layer (24) is inserted on the GaAs semiconductor substrate (20) between the n-GaAs source (21) and n-GaAs drain (22) is laminated and it is formed on the metallic layer (24) with the structure in which the oxide layer (26) and gate (23) are laminated to the seriatim. Therefore, the junction of the junction of the n-GaAs source (21) and metallic layer (24) and n-GaAs drain (22) and metallic layer (24) may be provided with the Schottky barrier (25).

이와 같은 구조의 제1실시예를 제조하는 방법은 다음과 같다.

The method for manufacturing the first preferred embodiment of this kind of the structure is same as those of the next.

GF Exhibit 1124 - 2210/2704

먼저, 도 3a 및 도 3b에 도시된 바와 같이, 반(Semi)-절연체 즉 반도체인 GaAs를 포함한 화합물 반도체 기판(20) 상에 10 nm 이하 두께의 GaAs를 포함한 화합물 반도체(210)를 호모 에피택시(Homo Epitaxy)법으로 성장시킨다. GaAs를 포함한 화합물 반도체 성장시 도핑 레벨(doping level)을 1020/cm3 이하로 하여 n-GaAs를 포함한 화합물 반도체(210)로 만든다. 그렇치 않으면, 도 3b에 도시된 바와 같이, GaAs를 포함한 화합물 반도체 기판(20)에 확산(diffusion) 혹은 이온-주입(ion-implantation)을 이용하여 깊이 10 nm, 도핑 농도(concentration) 1020/cm3 이하의 n형 반도체(210#39#)로 만든다.

In advance, as shown in FIG. figures 3a and 3b, the compound semiconductor (210) including the GaAs of the thickness less than 10 nm is grown on the compound semiconductor substrate (20) including the GaAs which is the half (Semi) - insulator, in other words, the semiconductor to the homoepitaxy (Homo Epitaxy) method. It makes the compound semiconductor (210) doing the compound semiconductor grown in doping level including the GaAs with 10 20 / cm 3 this harrow and includes the n-GaAs. If it is so it does not do , it deeply makes with 10 nm, and the N-type semiconductor (210') less than the doping concentration 10 20 / cm 3 on the compound semiconductor substrate (20) as shown in FIG. 3b, including the GaAs using the diffusion or the ion-implantation.

다음에, 도 3a에 도시된 바와 같이, 식각 공정을 통해 폭 100 nm의 세선(wire)(210a, 210#39#a)을 만들어 소스(21)와 드레인(22)을 형성할 수 있도록 한다. 소스(21)와 드레인(22)은 저항을 고려하여 세선의 다른 영역(아일런드 영역(220a) 및 트랜지스터 경계 영역(220b)) 보다 도핑 농도를 높게한다. 세선(210a, 210#39#a), 센선들을 따라 배치되는 소스(21) 및 드레인(22)의 제조는 리프트-오프(lift-off) 공정을 통해 선택적 성장법을 적용해도 무방하다. 이렇게 형성된 세선(210a 혹은 210#39#a)에 형성된 소스(21)와 드레인(22) 사이에, 도 3d에 도시된 바와 같이, 길이 10 nm 이하의 아일런드 영역(220a)을 식각 후 금속 증착을 통해 금속층(24)을 도 2에 도시된 바와 같이 형성한다. 이 금속층(24; 아일런드) 위에 두께 4 nm 이하의 유전체(26)를 증착시키거나 산화로에서 그 금속 산화막(26)을 두께 4 nm 이하로 형성시킨 후 금속을 증착시켜 게이트(gate)(23)를 만든다. 이렇게 형성된 금속층(24)과 세선의 n-GaAs 영역(21, 22)을 포함한 화합물 반도체 사이에는 쇼트키 접합(Schottky junction)(25)이 형성되며, 쇼트키 장벽 높이(barrier height)는 1.0 eV 이하로 조절한다. 이 에너지 장벽을 이용하여 단일 전자 트랜지스터를 구현한다.

Next, as shown in FIG. 3a, fine line (wire) (210a, 210'a) of the width 100 nm are made through the etching process and the source (21) and drain (22) are formed. It makes the doping concentration the source (21) and drain (22) high in consideration of the resistance than dissimilar domain (the island domain (220a) and transistor border area (220b)) of the fine line. It may be acceptable that the manufacture of the drain (22) and the source (21) arranged according to fine lines (210a, 210'a), and temperature sensors applies the selective growing method through the lift-off process. As shown in FIG. 2, as shown in FIG. 2, the island domain (220a) less than the length 10 nm the metallic layer (24) is formed between the source (21) and the drain (22) formed in the fine line (210a or 210'a) formed in this way after the etching through the metal deposition. After the dielectric (26) less than the thickness 4 nm is evaporated on this metallic layer (24: island) or the metal oxide layer (26) is formed in the oxidation furnace less than the thickness 4 nm the metal is evaporated and the gate (gate) (23) is made. The Schottky barrier (Schottky junction) (25) is formed between the compound semiconductor including n-GaAs domains (21, 22) of the fine line and metallic layer (24) formed in this way and the Schottky barrier height controls less than 1.0 eV. The single electron transistor is implemented using this energy barrier.

도 4은 도 2의 제1실시예와는 다른 제2실시예의 수직 단면도를 나타낸다. 도시된 바와 같이, 제2실시예는 GaAs 반도체 기판(30) 상에 금속 소스(31) 및 금속 드레인(32) 사이에 n-GaAs 도핑층(34)이 삽입된 트랜지스터 구조물이 적층되고, n-GaAs 도핑층(34) 상에 금속 게이트(33)가 순차로 적층된 구조로 형성된다. 따라서, 금속 소스(31)와 n-GaAs 도핑층(34)의 접합면 및 금속 드레인(32)과 n-GaAs 도핑층(34)의 접합면에는 각각 쇼트키 장벽(25)이 형성된다. 특히, 제1실시예에서와 같은 절연층이 형성되지 않고 n-GaAs 도핑층(34) 위에 바로 금속 게이트(33)가 형성된다. n-GaAs 도핑층(34)와 게이트(33) 사이에는 쇼트키 장벽이 형성되므로 별도의 절연층을 형성할 필요가 없다.

Fig. 4 shows the vertical side view of the second preferred embodiment different from the first preferred embodiment of 2. As shown in the figure, the transistor structure water in which as to the second preferred embodiment, the n-GaAs doped layer (34) is inserted on the GaAs semiconductor substrate (30) between the metal source (31) and metal drain (32) is laminated and it is formed with the structure in which the metal gate (33) is laminated to the seriatim on the n-GaAs doped layer (34). Therefore, the junction of the junction of the metal source (31) and n-GaAs doped layer (34) and metal drain (32) and n-GaAs doped layer (34) may be provided with the Schottky barrier (25). Especially, the same insulating layer is not formed at the first preferred embodiment and immediately, the metal gate (33) is formed on the n-GaAs doped layer (34). The separate insulating layer does not have to be formed since the Schottky barrier is formed between the n-GaAs doped layer (34) and gate (33).

이와 같은 구조의 제2실시예는 제1실시예와 유사한 순서로 제

It is manufactured with the order where the second

GF Exhibit 1124 - 2211/2704

조된다. 즉, GaAs를 포함한 화합물 반도체 기판(30)에 금속(31, 32)을 10 nm 두께 이하로 증착한 후 식각공정을 통해 폭 100 nm의 세선(34)을 이루도록 소스(31) 및 드레인(32)을 형성한다. 세선(미도시, 도 3a 참조)을 따라 배치되는 소스(31) 및 드레인(32)은 리프트-오프 공정을 통해 형성한다. 소스(31)와 드레인(32) 사이의 세선(미도시)에 길이 10 나노미터의 아일런드 영역(34)을 식각에 의해 형성한 후(도 3d 참조) GaAs를 포함한 화합물 반도체를 호모에피택시(Homo-Epitaxy)법에 의해 성장시킨다. GaAs를 포함한 화합물 반도체 성장시 혹은 성장후에는 도핑 레벨 및 도핑법을 도 3b 혹은 도 3c와 동일하게 적용하여 n형으로 한다. 그 다음 n형 GaAs 혹은 화합물 반도체(34) 위에 금속을 증착시켜 게이트(33)를 형성한다. 이렇게 형성된 금속(소스, 드레인 및 게이트)과 n-GaAs를 포함한 화합물 반도체 사이에는 쇼트키 접합이 형성되며 장벽 높이는 1.0 eV 이하로 조절한다. 이 에너지 장벽을 이용하여 단일 전자 트랜지스터를 구현한다.

preferred embodiment of this kind of structure is similar to the first preferred embodiment. That is, the source (31) and drain (32) are formed in order to be the fine line (34) of the width 100 nm metals (31, 32) comprised in the compound semiconductor substrate (30) including the GaAs less than 10 nm thickness after doing the deposition through the etching process. The source (31) and the drain (32) arranged according to the fine line (the not illustrated, refer to Figure 3a) form through the lift-off process. The compound semiconductor including the GaAs the island domain (34) of the length 10 nanometer with the etching after doing the formation (Figure 3d reference) is grown in the fine line (not illustrated) between the drain (32) and the source (31) with the homoepitaxy (Homo-Epitaxy) method. The doping level and doping method are applied after the compound semiconductor grown in or the growth including the GaAs identically with the figures 3b or 3c it appoints as the n-type. Next, the metal is evaporated on the n-type GaAs or the compound semiconductor (34) and the gate (33) is formed. While the Schottky barrier is formed between the compound semiconductor including metal (the source, and the drain and gate) formed in this way and n-GaAs the barrier height controls less than 1.0 eV. The single electron transistor is implemented using this energy barrier.

도 5는 제3실시예의 수직 단면도를 나타낸다. 제3실시예는 GaAs를 포함한 화합물 반도체 기판 대신에 실리콘(Si) 혹은 SOI 기판(40)을 사용하여 단일 전자 트랜지스터를 구현한 것이다. 도시된 바와 같이, 제3실시예는 Si 기판(40) 상에 n-SiGe 혹은 p-SiGe 소스(41) 및 n-SiGe 혹은 p-SiGe 드레인(42) 사이에 금속층(44)이 삽입된 트랜지스터 구조물이 적층되고, 금속층(44) 상에 SiO2층(46) 및 게이트(43)가 순차로 적층된 구조로 형성된다. 따라서, n-SiGe 혹은 p-SiGe 소스(41)와 금속층(44)의 접합면 및 n-SiGe 혹은 p-SiGe 드레인(42)과 금속층(44)의 접합면에는 각각 쇼트키 장벽(45)이 형성된다.

Figure 5 shows the vertical side view of the third preferred embodiment. The third preferred embodiment implements the single electron transistor using the silicone (Si) instead of the compound semiconductor substrate including the GaAs or the SOI substrate (40). As shown in the figure, the transistor structure water in which the metallic layer (44) is inserted between the n-SiGe or the p-SiGe source (41) and n-SiGe or the p-SiGe drain (42) as to the third preferred embodiment, is laminated on the Si substrate (40) and it is formed on the metallic layer (44) with the structure in which the SiO2 layer (46) and gate (43) are laminated to the seriatim. Therefore, the junction of the junction of the n-SiGe or the p-SiGe source (41) and metallic layer (44) and n-SiGe or the p-SiGe drain (42) and metallic layer (44) may be provided with the Schottky barrier (45).

이와 같은 구조의 제3실시예를 제조하는 방법은 기판 및 반도체 도핑층의 재료만 다를뿐 제1실시예의 제조 방법과 같다.

The method for manufacturing the third preferred embodiment of this kind of the structure is same as those of the manufacturing method of the first preferred embodiment the material of the semiconductor doped layer and substrate is different.

우선, 실리콘 기판(40) 상에 n 혹은 p 형 Si-Ge을 10 nm 두께 이하로 에피택시(Epitaxial)하게 성장시킨다. 이 때의 도핑 레벨은 1020/cm3 이하로 하며 도핑하는 방법으로는 에피택시(Epitaxial) 성장시와 성장후 이온-주입(ion-implantation) 혹은 확산(diffusion)에 의해 가능하다. 그 다음 식각 공정을 통해 폭 100 nm 이하의 세선(44)과 소스(41) 및 드레인(42)을 형성한 후, 소스(41) 및 드레인(42) 사이의 세선(44)을 길이 10 nm 이하로 식각하여 아일런드 영역을 형성한다. 다음에, 아일런드 영역에 금속을 증착하여 금속층(44)을 형성한다. 소스(41) 및 드레인(42)의 도핑 레벨은 세선의 다른 영역들(아일런드 영역 및 트랜지스터가 경계 영역) 보다 높게 한다. 세선(미도시)을 따라 배치된 소스(41) 및 드레인(42)의 형성은 리프트-오프 공정에 의해서도 가능하다.

First, it grows on the silicon substrate (40) to do the n or the p-type Si-Ge less than 10 nm thickness with the epitaxy (Epitaxial). It is possible through the method for doping while the doping level at this time does after the epitaxy (Epitaxial) grown in and growth with the ion-implantation or the diffusion. Next, the fine line (44) between the drain (42) and the source (41) are etched less than the length 10 nm and the fine line (44) less than the width 100 nm and source (41) and drain (42) the island domain are formed through the etching process after doing the formation. Next, the metal is deposited on the island domain and the metallic layer (44) is formed. It makes higher than dissimilar *** (the island domain and transistor is the border area) of the fine line. The formation of the drain (42) and the source (41) arr

GF Exhibit 1124 - 2212/2704

anged according to the fine line (not illustrated) is poss ible with the lift-off process.

다음에, 아일런드용 금속층(44) 위에 두께 4 nm 이하의 유전체(46)를 증착시키거나 산화로에서 두께 4 nm 이하의 금속 산화물을 형성시킨후 그 위에 금속을 증착시켜 게이트(43)를 형성한다. 이렇게 형성된 세선의 금속(44)과 SiGe 소스 및 게이트(41, 42) 사이에는 쇼트키 접합이 형성되며, 장벽 높이는 1.0 eV 이하로 조절한다. 이 에너지 장벽을 이용하면 단일전자트랜지스터가 구현된다.

Next, after the dielectric (46) less than the thickness 4 nm is evaporated on the metallic layer (44) for the isla nd or the metal oxide less than the thickness 4 nm in t he oxidation furnace is formed the metal is evaporated in the upper part and the gate (43) is formed. The Sch ottky barrier is formed between the metal (44) of the fi ne line formed in this way and SiGe source and gates (41, 42) and the barrier height controls less than 1.0 e V. The single electron transistor is implemented if this e nergy barrier is used.

도 6은 도 5의 제3실시예와 다른 제4실시예의 수직 단면도를 나타낸다. 제4실시예는 소스(51)와 드레인(52)을 금속으로 형성하되 실리콘 기판과 SiO2층(57a, 57b)에 의해 격리되고, 아일런드 영역을 n-SiGe 혹은 p-SiGe 도핑층(54)로 형성한 점에서 제3실시예와 차이가 있을뿐 구조적으로 제3실시예와 비슷하다.

Fig. 6 shows the vertical side view of the fourth preferred embodiment different from the third preferred embodiment of 5. The fourth preferred embodiment for ms the source (51) and drain (52) into the metal and it is isolated with the silicon substrate and SiO 2 layers (57a, 57b) and the forms the island domain into the n-SiGe or the p-SiGe doped layer (54) point has the third preferred embodiment and difference but difference are similar in the point which to the third preferred embodi ment.

이러한 구조의 제4실시예의 제조 방법은 다음과 같다.

The manufacturing method of the fourth preferred embodiment of such structure is same as those of the next.

먼저, SiO층이 형성된 실리콘 혹은 SOI 기판(50, 57a, 57b) 상에 10 nm 이하의 두께로 금속(51,52)을 증착한 후 식각 공정을 거쳐 100 nm 폭의 세선 형상을 따라 소스(51) 및 드레인(52)을 형성한다(도 3a 참조). 세선을 따라 형성된 소스(51) 및 드레인(52) 제조 공정은 리프트-오프 공정을 적용해도 무방하다.

In advance, the source (51) and drain (52) are formed into the thickness less than 10 nm on the silicone or S OI substrates (50, 57a, 57b) in which the SiO layer is f ormed after depositing metals (51,52) after the etching process according to the fine wire type of 100 nm widt h (refer to Figure 3a). It may be acceptable that the s ource (51) and the drain (52) manufacturing process of being formed according to the fine line apply the lift-off process.

그 다음 세선을 따라 배치되는 소스 및 드레인 영역 사이에 길이 10 nm 이하의 아일런드 영역을 식각 후 p-SiGe 혹은 n-SiGe을 증착하여 형성시킨다. 이 때의 도핑은 SiGe 성장시 혹은 성장후 이온주입 혹은 확산에 의해 수행되며, 그 레벨은 1020/cm3 이하로 한다.

Next, the p-SiGe or the n-SiGe is deposited after the etching and the island domain less than the length 10 n m is formed between the source and the drain region ar ranged according to the fine line. The doping at this ti me is performed by the ion implantation or diffusion aft er the SiGe grown in or growth and the level does less than 10 20 / cm 3 .

다음에, 게이트는 유전체를 4 nm 이하로 증착하거나 혹은 실리콘 -게르마늄층을 산화로에서 두께 4 nm 이하의 산화물을 형성시킨후 금속을 증착시켜 형성한다. 이렇게 형성된 금속과 n 혹은 p 형 사이에는 쇼트키 접합이 형성되며 장벽 높이는 1.0 eV 이하로 조절한다. 이 에너지 장벽을 이용하여 단일 전자 트랜지스터를 구현하는 것이다.

Next, the dielectric is deposited less than 4 nm or after the oxide less than the thickness 4 nm in the oxidation furnace is formed the metal is evaporated and gate for ms the silicon-germanium layer. The barrier height cont rols less than 1.0 eV while the Schottky barrier is forme d between the metal formed in this way and n or the p-type. The single electron transistor is implemented u sing this energy barrier.

도 7은 제5실시예의 수직 단면을 보여주는 도면이다. 제5실시예는 아일런드 영역의 n-SiGe 혹은 p-SiGe 도핑층(64) 상에 바로 금속을 증착하여 게이트(63)를 형성한 점에서 제4실시예와 차이가 있을뿐 구조적으로 제4실시예와 비슷하다.

Figure 7 is drawing showing the vertical section of the fifth preferred embodiment. The in which the fifth prefe rred embodiment deposits immediately, the metal on th e n-SiGe or the p-SiGe doped layer (64) of the island d omain and forming the gate (63) point has the fourth p referred embodiment and difference but difference are similar in the point to the fourth preferred embodiment.

GF Exhibit 1124 - 2213/2704

따라서, 제5실시예의 제조 방법은 도 6의 제5실시예에서와 유사하며, 다만 게이트(63)와 아일런드(64) 사이를, 제4실시예에서 처럼 4 nm 이하의 유전체(56)에 의해 분리해 놓지 않고, 금속 게이트(63)를 직접 SiGe층(64)에 접합시켜 생기는 쇼트키 장벽을 절연물로 이용하는 구조로서, 그 이외의 공정은 모든 것이 도 6의 제4실시예와 동일하다.

Therefore, the manufacturing method of the fifth preferred embodiment is similar in the fifth preferred em bodiment of 6 and but it separates between the gate (63) and island (64) like the fourth preferred embodime nt with the dielectric (56) less than 4 nm and it is the structure of using the Schottky barrier welding the met al gate (63) to the direct siGe layer (64) and is generat ed as the insulator and alls the process of the except a re identical with the fourth preferred embodiment of fi g. 6.

이상과 같은 방식으로 제작된 단일전자 트랜지스터의 동작 원리는 다음과 같다.

The principles of operation of the single electron transistor manufactured to the mode as above is same as those of the next.

일반적으로 금속과 n 혹은 p형 반도체가 접합시 평형 상태를 얻기위해 캐리어(carrier)들이 이동한다. 이 때문에 접합 사이에는 쌍극자(dipole)가 생기게 되며, 이 것이 에너지 장벽 즉 쇼트키 장벽으로 작용한다. 이 다이폴이 생긴 영역 즉 공핍(depletion) 영역의 두께 d와 캐패시턴스(capacitance) C 는 다음 수학식 1 및 2로 표시된다.

Generally, carrier move so that the metal and n or the P-type semiconductor obtain the equilibrium state in th e junction. For this reason, the dipole is generated bet ween the junction and this acts on the energy barrier, i n other words, the Schottky barrier. The domain, in oth er words, the thickness d and capacitance (capacitanc e) C of the depletion domain in which this dipole is gen erated are indicated with the equation 1 as 2.

$$d = (2\varphi\varepsilon\varepsilon_0/ne)^{1/2}$$

$$d = (2\varphi\varepsilon\varepsilon_0/ne)^{1/2}$$

$$C = A(\varepsilon\varepsilon_0\, ne/\varphi)^{1/2}$$

$$C = A(\varepsilon\varepsilon_0\, ne/\varphi)^{1/2}$$

여기서, n은 도핑레벨, e는 전하량, ε는 공기유전상수, ε0는 물질의 유전상수, φ는 공핍층에의해 생긴 전압, A는 단면적이다. 만약, n=1020/cm3이고 φ=0.7 Volt 라면 d=3.3 nm 이고, C/A= 3.4 x 10-20 F/nm2 가 된다. 수식 1 및 2에서 알 수 있듯이 도핑 레벨과 가해주는 전압을 조절함으로써 C 값을 더욱더 낮출 수 있다. 단일전자트랜지스터의 작동 온도는 아래 수학식 3에 의해서 결정된다.

Here, as to as to as to as to the n, the doping level, and the e, the charge quantity, and ε, the air dielectric constant, and ε 0 , the dielectric constant of the mate rial, the voltage in which φ is generated with the deple tion layer, and A is cross section. It the if is the n= 10 20 / cm 3 and it is φ =0.7 Volt instant noodle d=3.3 nm and C / A= 3.4 x 10 - 20 F / nm 2 is. By controlling the voltage adding with the doping level as seen in the for mula 1 and 2, C value can be more and more lowered. The operating temperature of the single electron transi stor is determined by the lower part equation 3.

$$e^2/2C\#62\#\#62\#K_BT$$

$$e^2/2C>>K_BT$$

가령 C = 3.4 x 10-20 [F] 이라 하자. 그러면 T = 273 x 102 K 가된다. 이상과 같은 물리적 변수를 이용하여 제작된 단일전자 트랜지스터는 아래와 같은 원리로 작동한다.

For example,, it says to be C = 3.4 x 10 - 20 [F] this. And then, it becomes with T = 273 x 10 2 K. The single electron transistor manufactured using the physical var iable as above operates to the following principles.

소스와 드레인 사이에 전압을 가하면 임의 전압에 이르러서야 전류가 흐른다. 이 때의 임의 전압을 쿠롱블러케이드갭(Coulomb blockade gap)이라 부르며, 전류가 흐르지 않는 것은 전자 하나가 소스에서 아일런드로 터널됨에 따라 아일런드에 충전(charging)이 일어나 더 이상의 전자를 받아들일 수 없기 때문이다. 만약 이 충전 에너지 보다 큰 에너지를 게이트에 공급하면 쿠롱블러케이드는 일어나지 않게되어 임의의 전류가 흐르게 된다. 그러므로 소스와 드레인 사이의 전압을 쿠롱부록케이드 갭 이하로 고정시키고 게이트 전압을 조절하면 기존의 3단자 트랜지스터와 유사하게 스위칭(switching)이 일어난다.

When the voltage tells to the arbitrary voltage if the voltage is added between source and drain the current flows. The arbitrary voltage at this time is called becau se of being the coulomb blockade gap and as the electr on one is tunneled to the island in the source the char ge (charging) occurs in the island and the electron of a ny more cannot be taken on that the current does not flow. If the energy large than this charge energy is sup plied gate with, the coulomb blockade does not occur a nd the arbitrary current flows. Therefore, if the voltage between source and drain are fixed less than the coulo mb blockade gap and the gate voltage is controlled, si milarly the switching occurs with the existing 3 terminal transistor.

GF Exhibit 1124 - 2214/2704

도면에 대한 간단한 설명

도 1a 및 도 1b는 각각 종래의 단일 전자 트랜지스터의 개략적인 수직 단면도이고,
도 2는 본 발명에 따른 단일 전자 트랜지스터 제1실시예의 개략적인 수직 단면도이며,

도 3은 본 발명에 따른 단일 전자 트랜지스터 제2실시예의 개략적인 수직 단면도이며,

도 4는 본 발명에 따른 단일 전자 트랜지스터 제3실시예의 개략적인 수직 단면도이며,

도 5는 본 발명에 따른 단일 전자 트랜지스터 제4실시예의 개략적인 수직 단면도이며,

그리고 도 6은 본 발명에 따른 단일 전자 트랜지스터 제5실시예의 개략적인 수직 단면도이다.

#60#도면의 주요부분에 대한 부호의 설명>

1. 실리콘 기판 2. 소스
3. 드레인 4. 아일런드
5. 터널 장벽
11a. 실리콘 기판 11b. SiO2 산화층
11. SOI 기판 12. 소스
13. 드레인 14. 아일런드
15. 유전체(터널장벽)
20. GaAs 기판 21. n-GaAs 소스
22. n-GaAs 드레인 23. 게이트
24. 금속층 25. 쇼트키 장벽
26. 산화물층
30. GaAs 기판 31. 금속 소스
32. 금속 드레인 33. 금속 게이트
34. n-GaAs 아일런드 35. 쇼트키 장벽
40. Si 기판 41. n-SiGe 혹은 p-SiGe 소스
42. n-SiGe 혹은 p-SiGe 드레인 43. 금속 게이트
44. 금속 아일런드 45. 쇼트키 장벽
46. SiO2 산화물층
50. Si 기판 51. 금속 소스
52. 금속 드레인 53. 금속 게이트
54. n-SiGe 혹은 p-SiGe 아일런드 55. 쇼트키 장벽

56. 산화물층 57a, 57b. SiO2 산화물층
60. Si 기판 61. 금속 소스
62. 금속 드레인 63. 금속 게이트
64. n-SiGe 혹은 p-SiGe 아일런드 65. 쇼트키 장벽

67a. SiO2 산화물층 67b. SiO2 산화물층

Brief explanation of the drawing

Figures 1a and 1b are the summary vertical side view of the conventional single electron transistor.
Fig. 2 is the summary vertical side view of the single electron transistor first preferred embodiment according to the present invention.
Fig. 3 is the summary vertical side view of the single electron transistor second embodiment according to the present invention.
Fig. 4 is the summary vertical side view of the single electron transistor third embodiment according to the present invention.
Fig. 5 is the summary vertical side view of the single electron transistor fourth embodiment according to the present invention.
And figure 6 is a summary vertical side view of the single electron transistor fifth embodiment according to the invention.
The description > of the denotation about the main part of the < drawing.
1. Silicon substrate 2. source.
3. Drain 4. island.
5. Tunnel barrier.
11a. Silicon substrate 11b. SiO 2 oxide layer.
11. SOI substrate 12. source.
13. Drain 14. island.
15.Dielectric(tunnel barrier)
20. GaAs substrate 21. n-GaAs source.
22. N-GaAs drain 23. gate.
24. Metallic layer 25. Schottky barrier.
26. Oxide layer.
30. GaAs substrate 31. metal source.
32. Metal drain 33. metal gate.
34. N-GaAs island 35. Schottky barrier.
40. The Si substrate 41. n-SiGe or the p-SiGe source.
42. The n-SiGe or the p-SiGe drain 43. metal gate.
44. Metal island 45. Schottky barrier.
46. SiO 2 oxide layer.
50. Si substrate 51. metal source.
52. Metal drain 53. metal gate.
54. The n-SiGe or the p-SiGe island 55. Schottky barrier.
56. The oxide layer 57a, and 57b. SiO 2 oxide layer.
60. Si substrate 61. metal source.
62. Metal drain 63. metal gate.
64. The n-SiGe or the p-SiGe island 65. Schottky barrier.
67a. SiO 2 oxide layer 67b. SiO 2 oxide layer.

Disclaimer

본 문서는 특허 및 과학기술문헌 전용의 첨단 자동번역 시스템을 이용해 생성되었습니다. 따라서 부분적으로 오역의 가능성이 있으며, 본 문서를 자격을 갖춘 전문 번역가에 의한 번역물을 대신하는 것으로 이용되어서는 안 됩니다. 시스템 및 네트워크의 특성때문에 발생한 오역과 부분 누락, 데이터의 불일치등에 대하여 본원은 법적인 책임을 지지 않습니다. 본 문서는 당사의 사전 동의 없이 권한이 없는 일반 대중을 위해 DB 및 시스템에 저장되어 재생, 복사, 배포될 수 없음을 알려드립니다.
(The document produced by using the high-tech machine translation system for the patent and science & technology literature. Therefore, the document can include the mistranslation, and it should not be used as a translation by a professional translator. We hold no legal liability for inconsistency of mistranslation, partial omission, and data generated by feature of system and network. We would like to inform you that the document canno

GF Exhibit 1124 - 2215/2704

t be regenerated, copied, and distributed by being stored in DB and system for unauthori zed general public without our consent.)

GF Exhibit 1124 - 2216/2704

(19) 대한민국특허청(KR)
(12) 공개특허공보(A)

(51) Int. Cl.[6]
H01L 21/8242

(11) 공개번호 특2000-0027908
(43) 공개일자 2000년05월15일

(21) 출원번호 10-1998-0045953
(22) 출원일자 1998년10월29일

(71) 출원인 유나이티드 마이크로일렉트로닉스 코퍼레이션 로버트 에이치. 씨. 차오
대만, 신츄, 사이언스-베이스드 인더스트리얼 파크,리신 로우드 2, 넘버 3

(72) 발명자 리우 푸-타이
대만 신츄 후-핑 1 로우드 넘버 40 2플로아
루 워터
대만 푸싱 엔 로우드 넘버 512 3플로아

(74) 대리인 임창현

심사청구 : 없음

(54) 임베디드 디램의 제조 방법

요약

본 발명은 메모리 회로 영역(memory circuit regions)과 로직 회로 영역(logic circuit regions)을 함께 집적할 수 있는 임베디드 DRAM의 제조 방법에 관한 것으로, 이들의 상부 표면이 동일한 높이를 갖고, 따라서 집적 회로 내의 높은 평탄도를 유지하도록 할 수 있다. 이 방법은 높은 종횡비의 콘택홀 전면에 내열 금속 산화막(refractory metal oxide)을 증착 하는 단계를 포함한다. 수소 플라즈마 처리(hydrogen plasma treatment) 또는 핫 수소 처리(hot hydrogen treatment)의 선택적인 적용을 통해 콘택홀 상에 증착된 내열 금속 산화막의 일부를 비도전성(non-conductive) 물질에서 도전성(conductive) 물질로 변화시키게 된다. 반면, 수소 플라즈마 처리 또는 핫 수소 처리를 수행하지 않은 내열 금속 산화막은 비도전성으로 남아 있게 된다. 따라서, 비도전성 내열 금속 산화막은 DRAM 커패시터의 유전막으로 사용될 수 있다.

대표도

도1b

색인어

DRAM

도면의 간단한 설명

도 1a 내지 도 1f는 본 발명의 실시예에 따른 임베디드 DRAM의 제조 방법의 단계들을 순차적으로 보여주는 단면도.

* 도면의 주요 부분에 대한 부호의 설명

100 : 반도체 기판 101 : 메모리 회로 영역
102 : 로직 회로 영역 103 : 트랜스퍼 FET
104 : 제 1 소오스/드레인 영역 105 : 제 2 소오스/드레인 영역
106 : 제 1 게이트 전극 107 : 로직 FET
108 : 제 3 소오스/드레인 영역 109 : 제 4 소오스/드레인 영역
110 : 제 2 게이트 전극 111 : 제 1 절연막
112 : 제 1 오프닝 113 : 제 2 오프닝
114 : 제 3 오프닝 115 : 제 1 도전막
116 : 내열 금속 산화막 117, 119 : 마스크막
118 : 제 2 도전막 120 : 커패시터
121 : 제 1 콘택 상호연결 122 : 제 2 콘택 상호연결
123 : 제 2 절연막 124 : 제 4 오프닝

GF Exhibit 1124 - 2217/2704

125 : 제 5 오프닝 126 : 제 3 도전막

126a : 제 1 도전 라인 126b, 126c : 제 2 도전 라인

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 DRAM(dynamic random access memory)의 제조 방법에 관한 것으로, 좀 더 구체적으로는 임베디드(embedded) DRAM의 제조 방법에 관한 것이다.

임베디드 DRAM은 반도체 기판 내에 DRAM 회로(DRAM circuits)와 로직 회로(logic circuits)가 함께 결합된 집적회로(integrated circuit; IC) 형태이다. 현재, 반도체 집적 회로의 제조 경향은 메모리 셀 어레이와 고속(high speed) 로직 회로 요소(elements)를 집적하는 것이다. 예를 들어, 마이크로프로세서(microprocessors) 또는 디지털 신호 처리기(digital signal processors)는 모두 임베디드 메모리와 결합된 집적회로를 갖는다.

요즈음, 반도체 제조자들은 생산 단가(production cost)를 유지하거나 낮추면서 소자의 성능(functionality)을 향상시키기 위해 노력하고 있다. 소형화 및 서브 미크론(sub-micron) 반도체 소자의 제조에 의해서, 성능 향상 및 생산 단가 감소의 목적이 부분적으로 충족되고 있다. 서브 미크론(sub-micron) 기술은 소자의 기능 저하와 기생 커패시턴스(parasitic capacitance)를 감소시킬 수 있기 때문에 소자의 성능을 향상시킬 수 있다. 더구나, 서브 미크론 기술은 보다 작은 반도체 칩(chip)을 생산해 낸다. 작은 크기의 칩 기능이 큰 칩과 유사하므로, 더 많은 실리콘 칩이 주어진 크기의 실리콘 웨이퍼 상에서 제조된다. 따라서, 각 칩의 평균 생산 단가가 더 낮아진다.

다른 반도체 제조자들은 반도체 칩 내에 로직 회로 요소와 메모리 소자를 집적화하고 있다. 이것은 소자의 성능을 향상시킬 뿐아니라 생산 단가를 줄이는 장점을 갖는다. 집적화는 로직 소자에 대한 반도체 칩의 일 부분의 메모리 소자에서 다른 반도체 칩의 다른 부분의 로직 소자로 전송되는 신호의 시간 딜레이(time delay)를 줄임으로써 성능을 향상시킨다. 게다가, 하나의 반도체 칩 상에 메모리와 로직 소자를 결합함으로써, 대부분 공통된 공정 단계를 공유할 수 있기 때문에 생산 단가가 낮아지게 된다.

하나의 단일 칩 내에 로직 회로와 메모리를 집적하는 방법을 제공하기 위한 시도가 다방면의 반도체 제조자들에 의해 행해지고 있다. 예를 들어, 미국 특허 No.5,292,677에서 Dennison et al.은 단일 반도체 칩(single semiconductor chip) 상에 CMOS(complementary metal oxide semiconductor) 소자와 DRAM 소자를 제조하는 방법을 제안하였다. 그러나, 이 두 요소를 제조함에 있어서, 상기 방법은 많은 제조 단계를 공유하지 못하고, 따라서 생산 단가에 두드러지게 영향을 주지 못한다. 또한, 상기 방법은 고효율(high-efficiency) 로직 소자의 제조를 포함하지 않는다.

단일 반도체 칩 상에 고효율 고속 로직 회로와 메모리 소자를 제조하기 위해서, 많은 제조 관점이 고려되어져야 한다. 가장 흔하게, 고려 사항은 로직 회로 공정 또는 메모리 회로에 관한 것이고, 둘 다의 관점은 거의 함께 고려되지 않는다.

상술한 바와 같이, 단일 실리콘 칩 상에 로직과 메모리 회로를 집적하는 개선된 방법이 요구된다.

발명이 이루고자하는 기술적 과제

본 발명은 상술한 제반 문제점을 해결하기 위해 제안된 것으로서, 고효율 고성능 로직 소자의 제조와 공유하는 공정 단계의 수를 증가시킬 수 있고, 따라서 생산 단가를 감소시킬 수 있는 임베디드 메모리 제조 방법을 제공함에 그 목적이 있다.

본 발명의 다른 목적은 메모리 소자 영역의 상부 표면과 로직 회로 영역의 상부 표면이 동일한 높이를 갖고, 따라서 집적 회로의 평탄도(degree of planarity)를 증가시킬 수 있는 임베디드 DRAM의 제조 방법을 제공함에 있다.

본 발명의 또 다른 목적은 개선된 임베디드 DRAM의 제조 방법을 제공함에 있다. 이 방법은 높은 종횡비(high aspect ration)를 갖는 콘택홀 전면에 내열 금속 산화막이 증착된다. 다음, 상기 내열 금속 산화막이 전기적 비도전성에서 도전성으로 변화되도록 하기 위해서 상기 증착된 내열 금속 산화막이 수소 플라즈마(hydrogen plasma) 또는 핫 수소(hot hydrogen)에 의해 처리된다.

본 발명의 또 다른 목적은 임베디드 DRAM의 제조 방법을 제공함에 있다. 이 방법은 높은 종횡비를 갖는 콘택홀 전면에 내열 금속 산화막이 증착된다. 다음, 상기 콘택홀 상에 증착된 내열 금속 산화막의 일부를 처리하기 위해 수소 플라즈마 또는 핫 수소가 사용된다. 수소 플라즈마 또는 핫 수소에 의해 처리된 내열 금속 산화막의 일부는 전기적 비도전성에서 도전성으로 변화된다. 한편, 수소 플라즈마 또는 핫 수소 처리에 노출되지 않은 내열 금속 산화막의 일부는 비도전성으로 남고, DRAM 커패시터의 유전막으로 사용될 수 있다.

발명의 구성 및 작용

(구성)

GF Exhibit 1124 - 2218/2704

상술한 목적을 달성하기 위한 본 발명에 의하면, 임베디드 DRAM의 제조 방법은, 먼저 미리 정의된 메모리 회로 영역 및 로직 회로 영역을 갖는 반도체 기판이 준비된다. 다음, 복수의 트랜스퍼 전계효과 트랜지스터가 메모리 회로 영역에 형성되고, 이때 각 트랜스퍼 전계효과 트랜지스터는 제 1 및 제 2 소오스/드레인 영역과 제 1 게이트 전극을 갖는다. 복수의 로직 전계효과 트랜지스터가 로직 회로 영역에 형성되고, 이때 각 로직 전계효과 트랜지스터는 제 3 및 제 4 소오스/드레인 영역과 제 2 게이트 전극을 갖는다.

상기 반도체 기판 전면에 제 1 절연막이 형성된 후, 메모리 회로 영역 내에 복수의 제 1 및 제 2 오프닝을 형성하기 위해서 각 트랜스퍼 전계효과 트랜지스터의 제 1 및 제 2 소오스/드레인 영역이 노출되도록 상기 제 1 절연막이 패터닝 된다. 유사하게, 복수의 제 3 오프닝이 상기 로직 회로 영역 내에 형성되고, 각 제 3 오프닝은 상기 로직 회로 영역 내의 적어도 하나의 도전막 영역이 노출되도록 형성된다.

다음, 상기 제 1 절연막 전면에 제 1 도전막이 형성된다. 상기 제 1 도전막은 상기 제 1 및 제 2 , 그리고 제 3 오프닝을 덮되, 상기 오프닝들을 완전히 채우지는 않는다. 다음, 상기 제 1 도전막 전면에 내열 금속 산화막이 형성된다. 상기 내열 금속 산화막 전면에 마스크층(mask layer)을 형성하되, 적어도 상기 제 1 오프닝을 덮고, 적어도 상기 제 2 오프닝과 제 3 오프닝을 노출하도록 형성한다. 상기 노출된 내열 금속 산화막을 도전막으로 변화시키기 위해서 수소 처리가 수행된다. 마스크층이 제거된다. 그 후, 상기 내열 금속 산화막 전면에 제 2 도전막이 형성된다. 제 2 도전막, 내열 금속 산화막, 그리고 제 1 도전막이 패터닝 된다. 그 결과, 각 제 1 오프닝 상부에 커패시터의 상부전극, 유전막, 그리고 하부전극이 형성되고, 각 제 2 및 제 3 오프닝 상부에 제 1 및 제 2 콘택 상호연결이 각각 형성된다.

이 방법의 바람직한 실시예에 있어서, 제 1 도전막이 내열 금속 산화막 형성 전에 패터닝 될 수 있다. 또한, 내열 금속 산화막은 수소 처리 전에 패터닝될 수 있다.

상술한 목적을 달성하기 위한 다른 본 발명에 의하면, 임베디드 DRAM의 제조 방법은 먼저, 제 2 도전막 상에 제 2 절연막이 형성된다. 각 커패시터의 상부전극이 노출되도록 상기 제 2 절연막 내에 복수의 제 4 오프닝이 형성되고, 상기 적어도 하나의 다른 도전막에 전기적으로 연결되는 제 2 도전막이 일부가 노출되도록 제 2 절연막 내에 복수의 제 5 오프닝이 형성된다. 상기 제 4 및 제 5 오프닝을 채우고 상기 제 2 절연막을 덮도록 제 3 도전막이 형성된다. 상기 제 3 도전막이 패터닝 되어 상기 제 5 오프닝을 통해 적어도 하나의 도전 영역(conductive region)에 각각 연결되는 복수의 제 2 도전 라인 뿐아니라, 각각 제 4 오프닝 및 상기 커패시터의 상부전극을 통해 레퍼런스 전압(reference voltage)에 연결되는 복수의 제 1 도전 라인(first conductive line)이 형성된다.

상술한 목적을 달성하기 위한 또 다른 발명에 의하면, 임베디드 DRAM의 제조 방법은, 먼저 메모리 회로 영역과 로직 회로 영역이 이미 정의된 반도체 기판이 준비된다. 적어도 하나의 트랜스퍼 전계효과 트랜지스터가 제 1 및 제 2 소오스/드레인 영역과 제 1 게이트 전극을 갖는 전계효과 트랜지스터를 구비한 메모리 회로 영역에 형성된다. 적어도 하나의 전계효과 트랜지스터가 제 3 및 제 4 소오스/드레인 영역과 제 2 게이트 전극을 갖는 로직 전계효과 트랜지스터를 구비한 로직 회로 영역에 형성된다.

반도체 기판 전면에 제 1 절연막이 형성된 후, 트랜스퍼 전계효과 트랜지스터의 제 1 및 제 2 소오스/드레인 영역이 노출되는 메모리 회로 영역 내에 제 1 오프닝 및 제 2 오프닝을 형성하기 위해 상기 제 1 절연막이 패터닝 된다. 유사하게, 로직 회로 영역 내에 적어도 하나의 도전 영역이 노출되도록 하는 제 3 오프닝이 형성된다. 상기 제 1 절연막 전면에 제 1 도전막이 형성된다. 제 1 도전막이 제 1 및 제 2 , 그리고 제 3 오프닝을 채운다. 상기 제 1 도전막 전면에 내열 금속 산화막이 증착된다. 적어도 상기 제 1 오프닝을 덮고, 적어도 상기 제 2 및 제 3 오프닝 상부 영역이 노출되도록 내열 금속 산화막 전면에 마스크층이 형성된다.

상기 노출된 도전막 내의 내열 금속 산화막을 변화시키기 위해서 수소 처리가 수행된다. 마스크층이 제거된다. 그 후, 상기 내열 금속 산화막 전면에 제 2 도전막이 형성된다. 제 2 도전막, 내열 금속 산화막, 그리고 제 1 도전막이 패터닝 된다. 마지막으로, 커패시터의 상부전극, 유전막, 그리고 하부전극이 제 1 오프닝의 상부에 형성되고, 상기 제 2 오프닝 및 제 3 오프닝 상부에 각각 제 1 및 제 2 콘택 상호연결이 형성된다.

이 방법의 바람직한 실시예에 있어서, 임베디드 DRAM의 제조 방법은 다음의 단계를 더 포함한다. 즉, 상기 제 2 도전막 상에 제 2 절연막이 형성된다. 제 2 절연막 내에 제 4 오프닝이 형성된다. 상기 커패시터의 상부전극이 노출되도록 제 2 절연막 내에 제 4 오프닝이 형성되고, 적어도 하나의 제 1 도전막과 전기적으로 연결되는 제 2 도전막의 일부가 노출되도록 제 2 절연막 내에 제 4 오프닝이 형성된다. 다음, 상기 제 4 및 제 5 오프닝을 채우고 상기 제 2 절연막을 덮도록 제 3 도전막이 형성된다. 상기 제 3 도전막이 패터닝 되어 상기 제 5 오프닝을 통해 적어도 하나의 도전 영역과 연결되는 제 2 도전 라인 뿐아니라 제 4 오프닝 및 커패시터의 상부전극을 통해 레퍼런스 전압에 연결되는 제 1 도전 라인이 형성된다.

상술한 바와 같은 일반적인 설명 및 다음의 상세 설명 둘 다는 실시예로서, 클레임된 본 발명을 더 상세히 설명하고자 한다.

(작용)

도 1b를 참조하면, 본 발명의 실시예에 따른 신규한 임베디드 DRAM의 제조 방법은, 수소 플라즈마 또는 핫 수소 처리를 통해 상기 콘택홀 상에 증착된 내열 금속 산화막의 일부가 비도전성에서 도전성 물질로 변화된다. 반면, 처리되지 않은 내열 금속 산화막의 부분은 비도전성으로 남게 된다. 이때, 처리되지 않은 내열 금속 산화막은 DRAM 커패시터의 유전막으로 사용될 수 있다. 이로써, 메모리 회로들과 로직 회로들을 함께 결합할 수 있고, 실리콘 웨이퍼에 대한 좋은 표면 평

GF Exhibit 1124 - 2219/2704

탄도를 유지하면서 생산 단가를 줄일 수 있다.

(실시예)

이하, 도 1을 참조하여 본 발명의 실시예를 상세히 설명한다.

도면과 상세 설명에 있어서, 동일하거나 그와 유사한 부분에 대해서는 가능한 동일한 참조 번호가 사용된다.

티타늄 옥사이드(titanium oxide)(TiO2), 탄탈륨 펜톡사이드(tantalum pentoxide)(Ta205), 페로스 옥사이드(ferrous oxide)(Fe203), 그리고 바륨 티타늄 옥사이드(barium titanium oxide)(BaTiO3)와 같은 내열 금속 산화막은 넓은 밴드 갭(wide band-gap)의 절연 물질이다. 만일, 내열 금속 산화막의 금속 이온들 또는 수소 베이컨시(vacancy)들 사이에 수소를 주입하기 위해 수소 플라즈마 처리 또는 핫 수소 처리가 수행된다면, 내열 금속 산화막 내의 산소 함량(oxygen content)이 감소된다. 따라서, 내열 금속 산화막은 n형 도전 산화막으로 바뀌게 될 것이다. 다시 말해, 원래의 내열 금속 산화막이 절연 특성(insulating properties)을 갖는 물질에서 반도체(semiconductive) 또는 도전(conductive) 특성을 갖는 물질로 변환될 것이다. 반응 메커니즘(reaction mechanism)은 다음의 식으로 요약된다.

[반응식]

$$O^{2-} \rightarrow \frac{1}{2} O_2 + 2e^-$$

수소 플라즈마 처리 또는 핫 수소 처리 후의 내열 금속 산화막의 전기적 도전성은 그 산소 함량에 의존하기 때문에, 내열 금속 산화막은 반도체 물질 또는 도전 물질로 만들어 질 수 있다. 또한, 내열 금속 산화막이 도전 물질로 바뀌었을 때의 저항값(resistance value)은 알맞게 조절될 수 있다.

내열 금속 산화막이 도전 물질로 변화되는 것과 관계된 방법들은 많은 간행물(articles)에서 볼 수 있다. 이러한 간행물들은 Fu-Tai Liou(본 발명의 발명자 중 하나임)에 의해 쓰여진 것으로서, 제목 'Semiconductor electrodes for photoelectrolysis'(1982년 뉴욕 주립대)로 발표된 것을 포함한다. C. Y. Yang et al.에 의해 쓰여진 두 번째 간행물은 제목 'Solid electrochemical modification of semiconductors'(Solid State Communication, Vol. 43, No. 8, pp. 633 - 636)로 발표되었다. 세 번째 간행물 또한 Fu-Tai Liou et al.에 의해 제목 'Photoelectrolysis at Fe203/TiO2 Heterojunction Electrode'(Journal of the Electrochemical Society, Vol. 129, No. 2, pp. 342 - 245)로 발표되었다.

본 발명은 임베디드 DRAM을 형성하는 방법을 개선하기 위해서 상술한 간행물들에서 제안된 기술들이 사용된다. 본 발명의 주된 특징은 큰 종횡비(high aspect ratio)를 갖는 콘택홀 전면에 내열 금속 산화막이 증착된다는 것이다. 콘택홀 상의 내열 금속 산화막의 전기 전도도는 수소 플라즈마 처리 또는 핫 수소 처리를 사용하여 비도전성에서 도전성으로 변화된다.

도 1a 내지 도 1f는 본 발명의 실시예에 따른 임베디드 DRAM의 제조 방법의 단계들을 순차적으로 보여주는 단면도이다.

먼저, 도 1a에서와 같이, 반도체 기판(100)이 준비된다. 반도체 기판(100)은 메모리 회로 영역(101)과 로직 회로 영역(102)으로 나누어질 수 있다. 상기 메모리 회로 영역(101)은 적어도 하나의 트랜스퍼 전계효과 트랜지스터(transfer FET; 이하, '트랜스퍼 FET'라 함)(103)를 갖는다. 트랜스퍼 FET(103)는 제 1 및 제 2 소오스/드레인 영역(104, 105), 그리고 제 1 게이트 전극(106)을 갖는다. 상기 로직 회로 영역(102)은 적어도 하나의 로직 전계효과 트랜지스터(이하, '로직 FET'라 함)(107)을 포함한다. 상기 로직 FET(107)는 제 3 및 제 4 소오스/드레인 영역(108, 109), 그리고 제 2 게이트 전극(110)을 갖는다. 반도체 기판(100) 전면에 제 1 절연막(111)이 형성된다. 다음, 메모리 회로 영역(101) 상에 제 1 오프닝(112) 및 제 2 오프닝(113)을 형성하기 위해 그리고, 로직 회로 영역(102) 상에 제 3 오프닝(114)을 형성하기 위해 상기 제 1 절연막(111)이 패터닝(patterning) 된다. 제 1 오프닝(112) 및 제 2 오프닝(113)은 각각 상기 트랜스퍼 FET의 제 1 및 제 2 소오스/드레인 영역(104, 105)을 노출시킨다. 상기 제 3 오프닝(114)은 상기 로직 회로 영역(102) 내의 적어도 하나의 도전 영역을 노출시킨다.

상기 노출된 도전 영역은 게이트 전극 또는 상기 로직 FET의 소오스/드레인 영역 중 하나일 수 있다. 예를 들어, 제 3 오프닝은 도 1a에 도시된 소오스/드레인 영역(108)을 노출시킨다. 상기 제 1 절연막(111) 전면에 제 1 도전막(115)이 형성된다. 상기 제 1 도전막(115)은 예를 들어, 금속 티타늄막(metallic titanium layer), 금속 텅스텐막(metallic tungsten layer), 티타늄 질화막(titanium nitride layer), 또는 티타늄/티타늄 질화막(titanium/titanium nitride layer)일 수 있다. 상기 제 1 도전막(115)은 제 1, 제 2, 그리고 제 3 오프닝(112, 113, 114)의 각각을 덮는다. 다음, 상기 제 1 도전막(115) 전면에 내열 금속 산화막(116)이 형성된다. 상기 내열 금속 산화막(116)을 형성하기 위해 티타늄 옥사이드(TiO2), 탄탈륨 펜톡사이드(Ta205), 페로스 옥사이드(Fe203), 그리고 바륨 티타늄 옥사이드(BaTiO3)가 사용될 수 있다. 여기서, 아직까지 내열 금속 산화막(116)은 절연막이다.

상기 제 1 도전막(115) 전면에 내열 금속 산화막(116)을 형성하기 전에 상기 제 1 도전막(115)이 패터닝 될 수 있다. 만일 상기 제 1 도전막(115)이 상기 내열 금속 산화막 증착 전에 패터닝 된다면, 후속 내열 금속 산화막 증착은 상기 제 1 도전막(115)의 가장자리(edge)를 덮게 된다.

다음, 도 1b를 참조하면, 상기 내열 금속 산화막(116) 전면에 마스크막(mask layer)(117)이 형성된다. 상기 마스크막(117)은 예를 들어, 적어도 상기 제 1 오프닝(112)을 덮고, 상기 제 2 오프

GF Exhibit 1124 - 2220/2704

닝(113) 및 제 3 오프닝(114)을 노출시키는 포토레지스트막(photoresist layer) 또는 확산 배리어막(diffusion barrier layer)일 수 있다. 예를 들어, 수소 플라즈마 처리 또는 핫 수소 처리와 같은 수소 처리(hydrogen treatment)후, 상기 노출된 내열 금속 산화막(116)은 도전막으로 변화된다. 상기 수소 처리 후, 내열 금속 산화막(116)의 노출된 부위는 도전성 내열 금속 산화막(116b)으로 변화되는 반면, 상기 노출되지 않은 내열 금속 산화막(116a)은 비도전성으로 남게 된다. 또한, 상기 내열 금속 산화막(116)은 상기 수소 처리가 수행되기 전에 패터닝될 수 있다.

이어서, 도 1c 및 도 1d에 있어서, 상기 마스크막(117)이 제거된다. 제 2 도전막(118) 예를 들어, 금속 텅스텐(metallic tungsten)이 상기 내열 금속 산화막(116)(116a 및 116b) 전면에 형성된다. 상기 제 2 도전막(118) 전면에 다른 마스크막(119)이 형성된다. 상기 제 2 도전막(118), 내열 금속 산화막(116), 그리고 제 1 도전막(115)이 상기 마스크막(119)을 사용하여 패터닝 된다. 그 결과로, 상기 제 1 오프닝(112) 상부에 도전막(118a), 비도전막(116a1), 그리고 도전막(115a)이 형성된다. 상기 도전막(118a), 비도전막(116a1), 그리고 도전막(115a)은 각각 커패시터(120)의 상부전극, 유전막(dielectric layer), 그리고 하부전극이 된다. 동시에, 상기 제 2 오프닝(113)의 상부 및 제 3 오프닝(114)의 상부에 각각 제 1 콘택 상호연결(first contact interconnect)(121) 및 제 2 콘택 상호연결(second contact interconnect)(122)이 형성된다.

상기 제 1 콘택 상호연결(121)은 제 2 도전막(118b), 내열 금속 산화막(116b1), 그리고 제 1 도전막(115b)을 포함한다. 상기 제 2 콘택 상호연결(122)은 제 2 도전막(118c), 내열 금속 산화막(116b2), 그리고 제 1 도전막(115c)을 포함한다. 마지막으로, 마스크층(119)이 제거된다.

도 1e에 있어서, 상기 제 2 도전막(118)(118a, 118b, 118c) 전면에 제 2 절연막(123)이 형성된다. 다음, 상기 커패시터의 상부전극(118a)이 노출되도록 상기 제 2 절연막(123) 내에 제 4 오프닝(124)이 형성된다. 그 동안, 상기 제 2 도전막(118) 예를 들어, 도전막 118b 또는 118c의 일부가 노출되도록 상기 제 2 절연막(123) 내에 제 5 오프닝(125)이 형성된다.

다음, 도 1f를 참조하면, 상기 제 4 및 제 5 오프닝(124, 125), 그리고 제 2 절연막(123) 전면에 제 3 도전막(126)이 형성된다. 상기 제 3 도전막(126)은 예를 들어, 알루미늄막(aluminum layer), 구리막(copper layer), 또는 알루미늄-구리 합금(aluminum-copper alloy)일 수 있다. 상기 제 3 도전막(126)이 패터닝 되어 레퍼런스 전압(reference voltage) 예를 들어, 1/2Vcc이 상기 제 4 오프닝(124)을 통해 커패시터의 상부전극(118a)에 공급되도록 하는 제 1 도전 라인(126a)이 형성된다. 유사하게, 상기 제 5 오프닝(125)을 통해 각각 적어도 하나의 도전 영역과 연결되는 제 2 도전 라인(126b 또는 126c)이 형성된다.

상술한 방법에 의해 제조된 상기 상부전극 및 콘택 상호연결의 상부 표면은 동일한 상대적 높이(relative height)를 갖는다. 따라서, 상기 메모리 회로 영역 및 로직 회로 영역이 또한 동일한 상대적 높이를 갖는다. 그 결과, 집적 회로에 대한 평탄도(degree of planarity)가 매우 증가된다.

더구나, 본 발명은 또한 큰 종횡비의 콘택홀 전면에 내열 금속 산화막을 증착 하여 임베디드 DRAM을 제조하는 방법을 제공한다. 수소 플라즈마 또는 핫 수소 처리를 통해 상기 콘택홀 상에 증착된 내열 금속 산화막의 일부가 비도전성에서 도전성 물질로 변화된다. 반면, 처리되지 않은 내열 금속 산화막의 부분은 비도전성으로 남게 된다. 따라서, 처리되지 않은 내열 금속 산화막은 DRAM 커패시터의 유전막으로 사용될 수 있다.

발명의 효과

본 발명은 본 발명은 메모리 회로들과 로직 회로들을 함께 결합할 수 있고, 따라서 실리콘 웨이퍼에 대한 좋은 표면 평탄도를 유지하면서 생산 단가를 줄일 수 있는 효과가 있다.

(57) 청구의 범위

청구항 1

메모리 회로 영역(memory circuit region) 및 로직 회로 영역(logic circuit region)을 갖는 기판을 준비하는 단계;

상기 메모리 회로 영역은 복수의 트랜스퍼(transfer) FET를 갖고, 각 트랜스퍼 FET는 제 1 및 제 2 소오스/드레인 영역과 제 1 게이트 전극을 포함하고, 상기 로직 회로 영역은 복수의 로직 FET를 갖고, 각 로직 FET는 제 3 및 제 4 소오스/드레인 영역과 제 2 게이트 전극을 포함하며,

상기 반도체 기판 전면에 제 1 절연막을 형성하는 단계;

상기 제 1 절연막을 패터닝 하여 상기 메모리 회로 영역 상에 복수의 제 1 및 제 2 오프닝을 형성하고, 상기 로직 회로 영역 상에 복수의 제 3 오프닝을 형성하는 단계;

상기 제 1 및 제 2 오프닝의 각각은 상기 트랜스퍼 FET의 각 제 1 및 제 2 소오스/드레인 영역을 노출시키고, 각 제 3 오프닝은 상기 로직 회로 영역 내의 도전 영역들 중 적어도 하나를 노출시키며,

상기 제 1 , 제 2 , 그리고 제 3 오프닝을 완전히 채우지 않고 덮도록 상기 제 1 절연막 상부에 제 1 도전막을 형성하는 단계;

상기 제 1 도전막 전면에 내열 금속 산화막을 형성하는 단계;

상기 내열 금속 산화막 상에 마스크막을 형성하되, 적어도 상기 제 1 오프닝을 덮고 적어도 상기 제 2 오프닝 및 제 3 오프닝을 노출시키도록 형성하는 단계;

GF Exhibit 1124 - 2221/2704

상기 노출된 내열 금속 산화막을 전기적으로 도전막이 되도록 변화시키기 위해서 수소 처리(hydrogen treatment)를 수행하는 단계;

상기 마스크막을 제거하는 단계;

상기 내열 금속 산화막 상에 제 2 도전막을 형성하는 단계; 및

상기 제 2 도전막, 내열 금속 산화막, 그리고 제 1 도전막을 패터닝 하여 각각 상기 제 1 오프닝 상부에 커패시터 상부전극, 유전막, 그리고 하부전극을 각각 형성하고, 상기 각 제 2 및 제 3 오프닝 상부에 제 1 및 제 2 콘택 상호연결을 형성하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

청구항 2

제 1 항에 있어서,

상기 내열 금속 산화막을 형성하는 단계는, 티타늄 옥사이드(Ti02), 탄탈륨 펜톡사이드(Ta205), 페로스 옥사이드(Fe203), 그리고 바륨 티타늄 옥사이드(BaTi03)를 포함하는 그룹에서 선택된 산화막들 중 하나를 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

청구항 3

제 1 항에 있어서,

상기 마스크막을 형성하는 단계는, 포토레지스트막을 형성하기 위해서 포토레지스트 물질(photoresist material) 또는 확산 배리어막(diffusion barrier layer)을 형성하기 위해서 확산 배리어 물질(diffusion barrier material)을 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

청구항 4

제 1 항에 있어서,

상기 수소 처리 단계는, 수소 플라즈마 처리(hydrogen plasma treatment) 또는 핫 수소 처리(hot hydrogen treatment)를 포함하는 임베디드 DRAM의 제조 방법.

청구항 5

제 1 항에 있어서,

상기 제 1 도전막을 형성하는 단계는, 티타늄 또는 텅스텐을 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

청구항 6

제 1 항에 있어서,

상기 제 1 도전막을 형성하는 단계는, 티타늄 나이트라이드(titanium nitride)를 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

청구항 7

제 1 항에 있어서,

상기 제 1 도전막을 형성하는 단계는, 상기 기판과 티타늄 질화막 사이에 티타늄막이 삽입되도록 티타늄 및 티타늄 나이트라이드를 차례로 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

청구항 8

제 1 항에 있어서,

상기 제 2 도전막 형성 단계는, 텅스텐을 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

청구항 9

제 1 항에 있어서,

상기 커패시터 상부전극의 측벽 에지(side edges)는 커패시터 하부전극의 측벽 에지와 일직선이 되도록 하는 임베디드 DRAM의 제조 방법.

청구항 10

제 1 항에 있어서,

상기 방법은, 상기 내열 금속 산화막 형성 단계 전에, 제 1 도전막을 패터닝 하는 단계를 더 포함하는 임베디드 DRAM의 제조 방법.

청구항 11

제 1 항에 있어서,

상기 방법은, 상기 수소 처리를 수행하는 단계 전에, 내열 금속 산화막을 패터닝 하는 단계를 더 포함하는 임베디드 DRAM의 제조 방법.

GF Exhibit 1124 - 2222/2704

청구항 12

제 1 항에 있어서,

상기 제 2 도전막, 내열 금속 산화막, 그리고 제 1 도전막을 패터닝 하는 단계 후, 상기 제 2 도전막 상에 제 2 절연막을 형성하는 단계;

상기 각 커패시터의 상부전극이 노출되도록 제 2 절연막 내에 복수의 제 4 오프닝을 형성하고, 적어도 하나의 도전 영역과 연결되는 제 2 도전막의 일부가 노출되도록 제 2 절연막 내에 복수의 제 5 오프닝을 형성하는 단계;

상기 제 4 오프닝, 제 5 오프닝, 그리고 제 2 절연막 전면에 제 3 도전막을 형성하는 단계; 및

상기 제 4 오프닝을 통해 상기 각 커패시터의 상부전극으로 레퍼런스 전압(reference voltage)을 공급하는 복수의 제 1 도전 라인(first conductive lines)과, 상기 제 5 오프닝을 통해 적어도 하나의 도전 영역과 각각 연결되는 복수의 제 2 도전 라인(second conductive lines)을 형성하기 위해서 상기 제 3 도전막을 패터닝 하는 단계를 더 포함하는 임베디드 DRAM의 제조 방법.

청구항 13

제 12 항에 있어서,

상기 레퍼런스 전압은 1/2 Vcc 전압을 포함하는 임베디드 DRAM의 제조 방법.

청구항 14

제 12 항에 있어서,

상기 제 3 도전막을 형성하는 단계는, 알루미늄, 구리, 또는 알루미늄-구리 합금을 증착 하는 단계인 임베디드 DRAM의 제조 방법.

청구항 15

제 1 항에 있어서,

상기 도전 영역은 상기 로직 FET의 제 3 또는 제 4 소오스/드레인 영역, 또는 제 2 게이트 전극을 나타내는 임베디드 DRAM의 제조 방법.

청구항 16

메모리 회로 영역 및 로직 회로 영역을 갖는 반도체 기판을 준비하는 단계;

상기 메모리 회로 영역은 적어도 하나의 트랜스퍼 FET를 갖고, 트랜스퍼 FET는 제 1 및 제 2 소오스/드레인 영역과 제 1 게이트 전극을 포함하고, 상기 로직 회로 영역은 적어도 하나의 로직 FET를 갖고, 로직 FET는 제 3 및 제 4 소오스/드레인 영역과 제 2 게이트 전극을 포함하며,

반도체 기판 전면에 제 1 절연막을 형성하는 단계;

상기 제 1 절연막을 패터닝 하여 상기 메모리 회로 영역 상에 제 1 및 제 2 오프닝을 형성하고, 상기 로직 회로 영역 상에 제 3 오프닝을 형성하는 단계;

상기 제 1 및 제 2 오프닝 각각은 상기 트랜스퍼 FET의 각 제 1 및 제 2 소오스/드레인 영역을 노출시키고, 각 제 3 오프닝은 상기 로직 회로 영역 내의 도전 영역들 중 적어도 하나를 노출시키며,

상기 제 1 , 제 2 , 그리고 제 3 오프닝을 완전히 채우지 않고 덮도록 상기 제 1 절연막 상부에 제 1 도전막을 형성하는 단계;

상기 제 1 도전막 전면에 내열 금속 산화막을 형성하는 단계;

상기 내열 금속 산화막 상에 마스크막을 형성하되, 적어도 상기 제 1 오프닝을 덮고 적어도 상기 제 2 오프닝 및 제 3 오프닝을 노출시키도록 형성하는 단계;

상기 노출된 내열 금속 산화막이 전기적으로 도전막이 되도록 변화시키기 위해 수소 처리를 수행하는 단계;

상기 마스크막을 제거하는 단계;

상기 내열 금속 산화막 상에 제 2 도전막을 형성하는 단계; 및

상기 제 2 도전막, 내열 금속 산화막, 그리고 제 1 도전막을 패터닝 하여 상기 각 제 1 오프닝 상부에 커패시터 상부전극, 유전막, 그리고 하부전극을 각각 형성하고, 상기 각 제 2 및 제 3 오프닝 상부에 제 1 및 제 2 콘택 상호연결을 형성하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

청구항 17

제 16 항에 있어서,

상기 내열 금속 산화막을 형성하는 단계는, 티타늄 옥사이드(TiO2), 탄탈륨 펜톡사이드(Ta2O5), 페로스 옥사이드(Fe2O3), 그리고 바륨 티타늄 옥사이드(BaTiO3)를 포함하는 그룹에서 선택된 산화막들 중 하나를 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

GF Exhibit 1124 - 2223/2704

청구항 18

제 16 항에 있어서,

마스크막을 형성하는 단계는, 포토레지스트막을 형성하기 위해서 포토레지스트 물질 또는 배리어막을 형성하기 위해서 확산 배리어 물질을 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

청구항 19

제 16 항에 있어서,

수소 처리를 수행하는 단계는, 수소 플라즈마 처리 또는 핫 수소 처리를 사용하여 수행되는 단계인 임베디드 DRAM의 제조 방법.

청구항 20

제 16 항에 있어서,

상기 제 1 도전막을 형성하는 단계는, 티타늄 또는 텅스텐을 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

청구항 21

제 16 항에 있어서,

상기 제 1 도전막을 형성하는 단계는, 티타늄 질화막을 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

청구항 22

제 16 항에 있어서,

상기 제 1 도전막을 형성하는 단계는, 반도체 기판과 티타늄 질화막 사이에 티타늄막이 삽입되도록 티타늄 및 티타늄 나이트라이드를 차례로 증착 하는 단계를 더 포함하는 임베디드 DRAM의 제조 방법.

청구항 23

제 16 항에 있어서,

상기 제 2 도전막을 형성하는 단계는, 텅스텐을 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

청구항 24

제 16 항에 있어서,

상기 커패시터 상부전극의 측벽 에지는, 상기 커패시터 하부전극의 측벽 에지와 일직선이 되도록 하는 임베디드 DRAM의 제조 방법.

청구항 25

제 16 항에 있어서,

상기 방법은, 내열 금속 산화막을 형성하는 단계 전에 제 1 도전막을 패터닝 하는 단계를 더 포함하는 임베디드 DRAM의 제조 방법.

청구항 26

제 16 항에 있어서,

상기 방법은, 상기 수소 처리 수행 단계 전에 내열 금속 산화막내열 금속 산화막을 패터닝 하는 단계를 더 포함하는 임베디드 DRAM의 제조 방법.

청구항 27

제 16 항에 있어서,

제 2 도전막, 내열 금속 산화막, 그리고 제 1 도전막을 패터닝 하는 단계는, 제 2 도전막 상에 제 2 절연막을 형성하는 단계;

상기 커패시터의 상부전극이 노출되도록 제 2 절연막 내에 제 4 오프닝을 형성하고, 적어도 하나의 도전 영역과 연결되는 제 2 도전막의 일부가 노출되도록 제 2 절연막 내에 제 5 오프닝을 형성하는 단계;

상기 제 4 오프닝, 제 5 오프닝, 그리고 제 2 절연막 전면에 제 3 도전막을 형성하는 단계; 및

상기 제 4 오프닝을 통해 상기 각 커패시터의 상부전극으로 레퍼런스 전압을 공급하는 제 1 도전라인과, 상기 제 5 오프닝을 통해 적어도 하나의 도전 영역과 각각 연결되는 제 2 도전 라인을 형성하기 위해서 상기 제 3 도전막을 패터닝 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

청구항 28

GF Exhibit 1124 - 2224/2704

제 27 항에 있어서,

상기 레퍼런스 전압은, 1/2 Vcc 전압을 포함하는 임베디드 DRAM의 제조 방법.

청구항 29

제 27 항에 있어서,

상기 제 3 도전막을 형성하는 단계는, 알루미늄, 구리 또는 알루미늄-구리 합금을 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

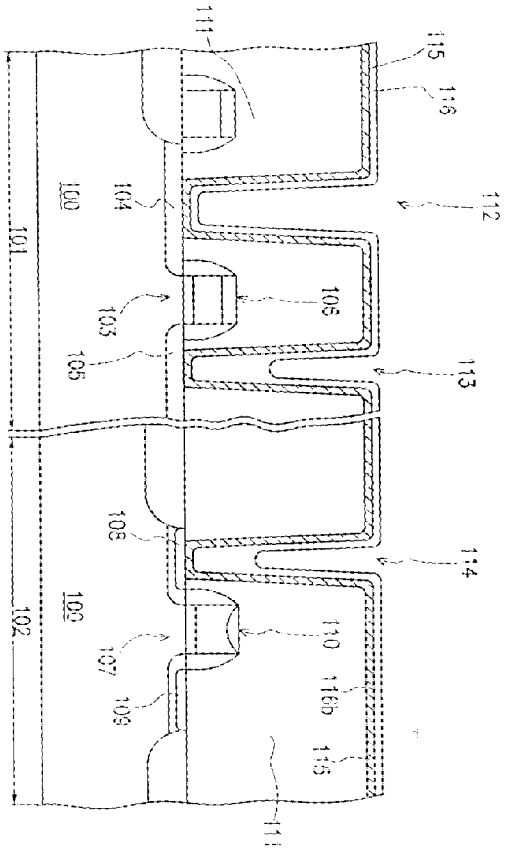
청구항 30

제 16 항에 있어서,

상기 도전 영역은, 로직 FET의 제 3 또는 제 4 소오스/드레인 영역, 또는 제 2 게이트 전극을 나타내는 임베디드 DRAM의 제조 방법.

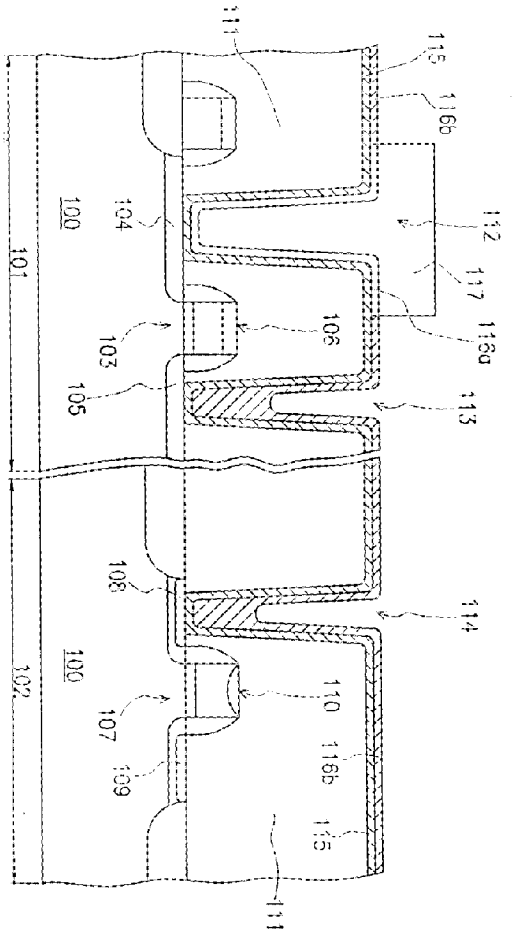
도면

도면1a



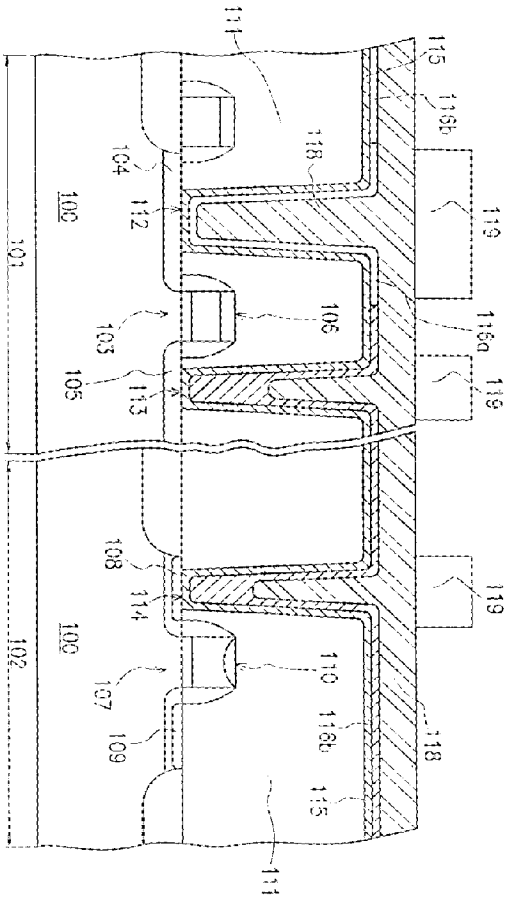
GF Exhibit 1124 - 2225/2704

도면6



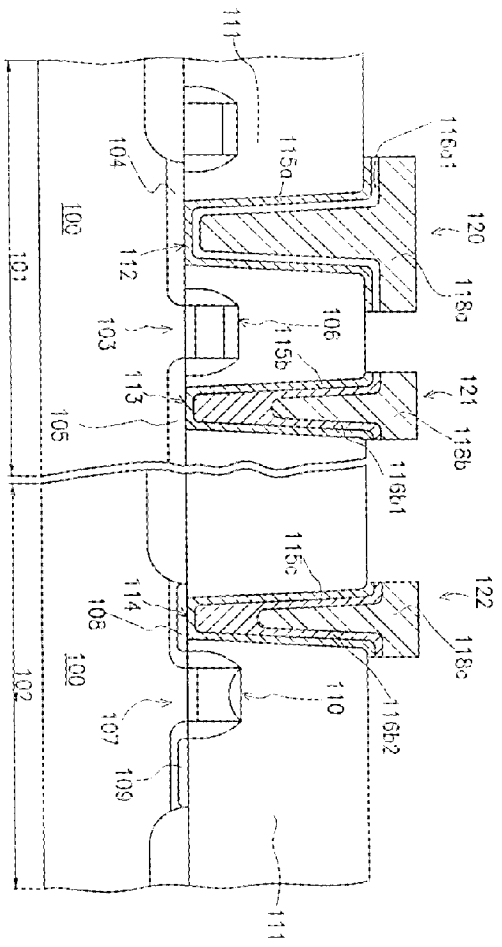
GF Exhibit 1124 - 2226/2704

도면2



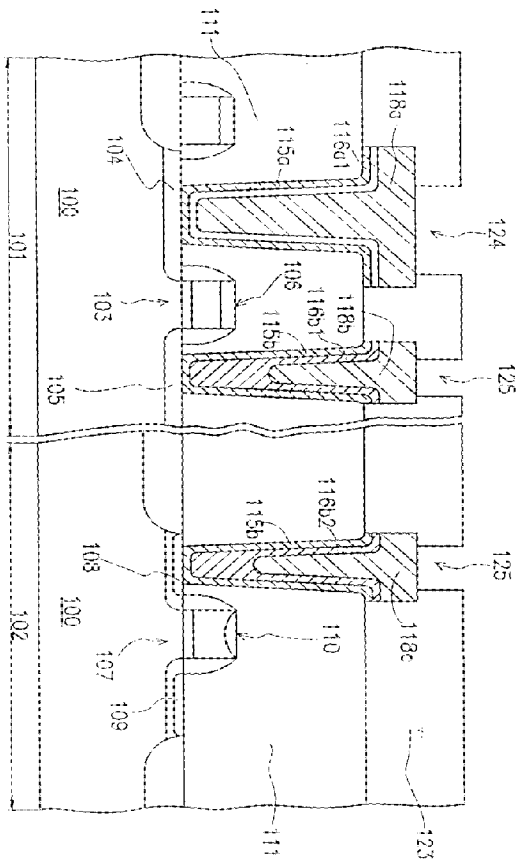
GF Exhibit 1124 - 2227/2704

도면12



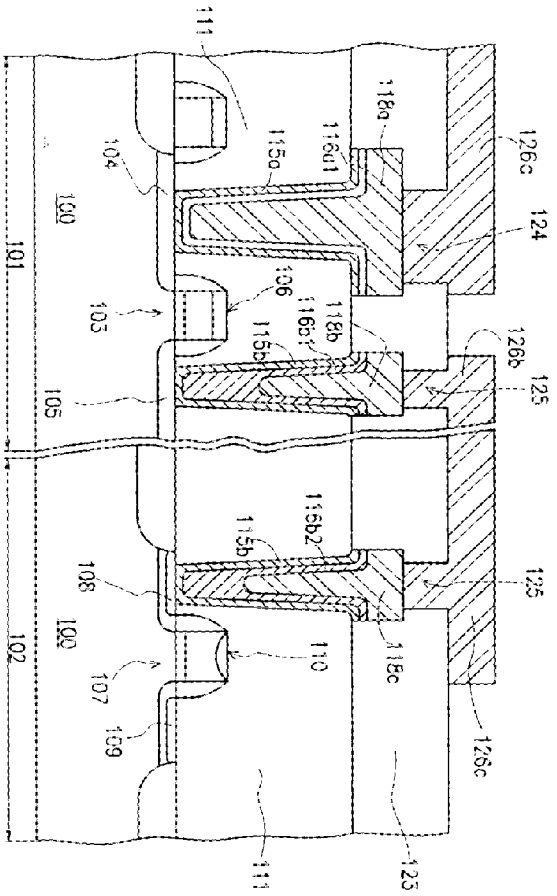
GF Exhibit 1124 - 2228/2704

도면2



GF Exhibit 1124 - 2229/2704

도면11



GF Exhibit 1124 - 2230/2704

Unexamined Patent Publication(A)

Bibliographic Data

Int.Cl.	H01L 27/108 | H01L 21/8234
Application No.	1019980045953
Application Date	19981029
Unexamined Publication No.	1020000027908
Unexamined Publication Date	20000515
Requested Date of Examination	20011017
Agent.	YIM, Chang Hyun
Inventor	RiUPu-TaI | Woe-Teo Ru
Applicant	UNITED MICROELECTRONICS CORP.

발명의 명칭

임베디드 디램의 제조 방법

Title of Invention

METHOD FOR MANUFACTURING AN EMBEDDED DRAM

요약

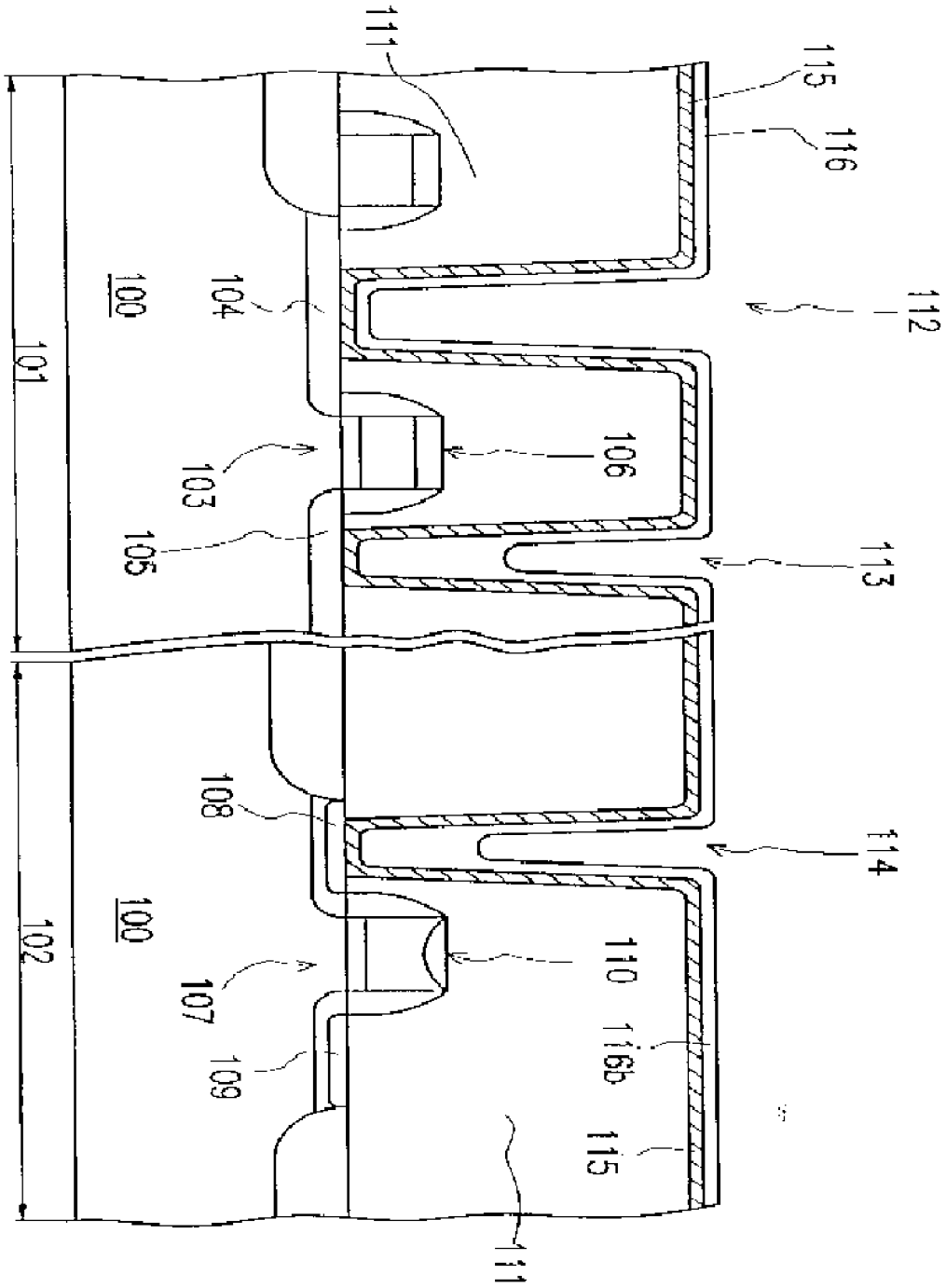
본 발명은 메모리 회로 영역(memory circuit regions)과 로직 회로 영역(logic circuit regions)을 함께 집적할 수 있는 임베디드 DRAM의 제조 방법에 관한 것으로, 이들의 상부 표면이 동일한 높이를 갖고, 따라서 집적 회로 내의 높은 평탄도를 유지하도록 할 수 있다. 이 방법은 높은 종횡비의 콘택홀 전면에 내열 금속 산화막(refractory metal oxide)을 증착 하는 단계를 포함한다. 수소 플라즈마 처리(hydrogen plasma treatment) 또는 핫 수소 처리(hot hydrogen treatment)의 선택적인 적용을 통해 콘택홀 상에 증착된 내열 금속 산화막의 일부를 비도전성(non-conductive) 물질에서 도전성(conductive) 물질로 변화시키게 된다. 반면, 수소 플라즈마 처리 또는 핫 수소 처리를 수행하지 않은 내열 금속 산화막은 비도전성으로 남아 있게 된다. 따라서, 비도전성 내열 금속 산화막은 DRAM 커패시터의 유전막으로 사용될 수 있다.

Abstract

The present invention relates to the manufacturing method of the embedded DRAM which together can accumulate the logic circuit area (logic circuit regions) and memory circuit domain (memory circuit regions), and it has the height in which their top surface is identical and therefore the high planarity within the integrated circuit is maintained. This method comprises the step of depositing the refractory metal oxide layer in the contact hole front side of the high aspect ratio. The part of the refractory metal oxide layer deposited through the selective application of the hydrogen plasma treatment or the hot hydrogen treatment on the contact hole is diversified in the non-conductive material to the conductivity (conductive) material. On the other hand, the hydrogen plasma treatment or the refractory metal oxide layer which does not perform the hot hydrogen treatment remains as the non-conductive. Therefore, the non-conductive refractory metal oxide layer can be used as the dielectric layer of the DRAM capacitor.

대표도면(Representative drawing)

GF Exhibit 1124 - 2231/2704



청구의 범위

청구 1항:

메모리 회로 영역(memory circuit region) 및 로직 회로 영역(logic circuit region)을 갖는 기판을 준비하는 단계; 상기 메모리 회로 영역은 복수의 트랜스퍼(transfer) FET를 갖고, 각 트랜스퍼 FET는 제 1 및 제 2 소오스/드레인 영역과 제 1 게이

Scope of Claims

Claim 1:

The memory circuit domain (memory circuit region) and the substrate having the logic circuit area (logic circuit region), and each transfer FET is first and second sour ce/drain region and the first gate electrode the memor

GF Exhibit 1124 - 2232/2704

트 전극을 포함하고, 상기 로직 회로 영역은 복수의 로직 FET를 갖고, 각 로직 FET는 제 3 및 제 4 소오스/드레인 영역과 제 2 게이트 전극을 포함하며, 상기 반도체 기판 전면에 제 1 절연막을 형성하는 단계; 상기 제 1 절연막을 패터닝 하여 상기 메모리 회로 영역 상에 복수의 제 1 및 제 2 오프닝을 형성하고, 상기 로직 회로 영역 상에 복수의 제 3 오프닝을 형성하는 단계; 상기 제 1 및 제 2 오프닝의 각각은 상기 트랜스퍼 FET의 각 제 1 및 제 2 소오스/드레인 영역을 노출시키고, 각 제 3 오프닝은 상기 로직 회로 영역 내의 도전 영역들 중 적어도 하나를 노출시키며, 상기 제 1 , 제 2 , 그리고 제 3 오프닝을 완전히 채우지 않고 덮도록 상기 제 1 절연막 상부에 제 1 도전막을 형성하는 단계; 상기 제 1 도전막 전면에 내열 금속 산화막을 형성하는 단계; 상기 내열 금속 산화막 상에 마스크막을 형성하되, 적어도 상기 제 1 오프닝을 덮고 적어도 상기 제 2 오프닝 및 제 3 오프닝을 노출시키도록 형성하는 단계; 상기 노출된 내열 금속 산화막을 전기적으로 도전막이 되도록 변화시키기 위해서 수소 처리(hydrogen treatment)를 수행하는 단계; 상기 마스크막을 제거하는 단계; 상기 내열 금속 산화막 상에 제 2 도전막을 형성하는 단계; 및 상기 제 2 도전막, 내열 금속 산화막, 그리고 제 1 도전막을 패터닝 하여 각각 상기 제 1 오프닝 상부에 커패시터 상부전극, 유전막, 그리고 하부전극을 각각 형성하고, 상기 각 제 2 및 제 3 오프닝 상부에 제 1 및 제 2 콘택 상호연결을 형성하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

y circuit domain has multiple transfer FETs are include d ; the logic circuit area has multiple logic FETs ; each logic FET includes the third and fourth source/drain regi on and the second gate electrode ; the first step of for ming the first insulating layer on the semiconductor sub strate front board the insulating layer is patterned and multiple first and second openings are formed on the m emory circuit domain ; each of step: first and second o pening of forming multiple third openings on the logic ci rcuit area exposes each first and second source/drain r egion of the transfer FET ; and each third opening exp oses at least one among the conductive regions within the logic circuit area. The manufacturing method of the embedded DRAM including forming first and second con tact interconnection at the upper part of each second and the third opening the mask film is formed on the st ep: step: refractory metal oxide layer of forming the re fractory metal oxide layer on the first conductive film fr ont side of forming the first conductive film on the first top portion of dielectric layer to completely nots fill up and cover first and second , and the third opening.

청구 2항:

제 1 항에 있어서,상기 내열 금속 산화막을 형성하는 단계는, 티타늄 옥사이드(TiO2), 탄탈륨 펜톡사이드(Ta2O5), 페로스 옥사이드(Fe2O3), 그리고 바륨 티타늄 옥사이드(BaTiO3)를 포함하는 그룹에서 선택된 산화막들 중 하나를 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

Claim 2:

The manufacturing method of the embedded DRAM of claim 1, wherein step of forming the refractory metal o xide layer comprises a step of depositing one among th e oxide film selected in the group including the titanium oxide (TiO2), the tantalum pentoxide (Ta2O5), and the ferrous oxide (Fe2O3) and barium titanium oxide (BaTiO 3).

청구 3항:

제 1 항에 있어서,상기 마스크막을 형성하는 단계는, 포토레지스트막을 형성하기 위해서 포토레지스트 물질(photoresist material) 또는 확산 배리어막(diffusion barrier layer)을 형성하기 위해서 확산 배리어 물질(diffusion barrier material)을 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

Claim 3:

The manufacturing method of the embedded DRAM of claim 1, wherein step of forming the mask film comprise s a step of depositing the diffusion-barrier material (diff usion barrier material) the photoresist material or the di ffusion barrier layer is formed in order to form the phot oresist film.

청구 4항:

제 1 항에 있어서,상기 수소 처리 단계는, 수소 플라즈마 처리(hydrogen plasma treatment) 또는 핫 수소 처리(hot hydrogen treatment)를 포함하는 임베디드 DRAM의 제조 방법.

Claim 4:

The manufacturing method of the embedded DRAM of claim 1, wherein the hydrogen treatment stage compris es the hydrogen plasma treatment or the hot hydrogen treatment.

청구 5항:

제 1 항에 있어서,상기 제 1 도전막을 형성하는 단계는, 티타늄 또는 텅스텐을 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

Claim 5:

The manufacturing method of the embedded DRAM of claim 1, wherein step of forming the first conductive fil m comprises a step of depositing titanium or tungsten.

청구 6항:

제 1 항에 있어서, 상기 제 1 도전막을 형성하는 단계는, 티타늄 나이트라이드(titanium nitride)를 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

Claim 6:

The manufacturing method of the embedded DRAM of claim 1, wherein step of forming the first conductive fil m comprises a step of depositing the titanium nitride.

GF Exhibit 1124 - 2233/2704

청구 7항:

제 1 항에 있어서, 상기 제 1 도전막을 형성하는 단계는, 상기 기판과 티타늄 질화막 사이에 티타늄막이 삽입되도록 티타늄 및 티타늄 나이트라이드를 차례로 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

Claim 7:

As for claim 1, the manufacturing method of the embedded DRAM wherein forming the first conductive fil m includes depositing the successively titanium and tit anium nitride such that the titanium film is inserted bet ween the substrate and TiN film.

청구 8항:

제 1 항에 있어서, 상기 제 2 도전막 형성 단계는, 텅스텐을 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

Claim 8:

As for claim 1, the manufacturing method of the embedded DRAM wherein the second conductive layer f orming step includes the step that deposits tungsten.

청구 9항:

제 1 항에 있어서, 상기 커패시터 상부전극의 측벽 에지(side edges)는 커패시터 하부전극의 측벽 에지와 일직선이 되도록 하는 임베디드 DRAM의 제조 방법.

Claim 9:

As for claim 1, the sidewall edge (side edges) of the capacitor upper part electrode is the manufacturing me thod of the sidewall edge of the capacitor lower part el ectrode and the embedded DRAM which it does in order to be straight.

청구 10항:

제 1 항에 있어서, 상기 방법은, 상기 내열 금속 산화막 형성 단계 전에, 제 1 도전막을 패터닝 하는 단계를 더 포함하는 임베디드 DRAM의 제조 방법.

Claim 10:

The manufacturing method of the embedded DRAM of claim 1, wherein the method further comprises patterni ng the first conductive film before the refractory metal oxide layer formation step.

청구 11항:

제 1 항에 있어서, 상기 방법은, 상기 수소 처리를 수행하는 단계 전에, 내열 금속 산화막을 패터닝 하는 단계를 더 포함하는 임베디드 DRAM의 제조 방법.

Claim 11:

The manufacturing method of the embedded DRAM of claim 1, wherein the method further comprises patterni ng the refractory metal oxide layer before the step, of performing the hydrogen treatment.

청구 12항:

제 1 항에 있어서, 상기 제 2 도전막, 내열 금속 산화막, 그리고 제 1 도전막을 패터닝 하는 단계 후, 상기 제 2 도전막 상에 제 2 절연막을 형성하는 단계; 상기 각 커패시터의 상부전극이 노출되도록 제 2 절연막 내에 복수의 제 4 오프닝을 형성하고, 적어도 하나의 도전 영역과 연결되는 제 2 도전막의 일부가 노출되도록 제 2 절연막 내에 복수의 제 5 오프닝을 형성하는 단계; 상기 제 4 오프닝, 제 5 오프닝, 그리고 제 2 절연막 전면에 제 3 도전막을 형성하는 단계; 및 상기 제 4 오프닝을 통해 상기 각 커패시터의 상부전극으로 레퍼런스 전압(reference voltage)을 공급하는 복수의 제 1 도전 라인(first conductive lines)과, 상기 제 5 오프닝을 통해 적어도 하나의 도전 영역과 각각 연결되는 복수의 제 2 도전 라인(second conductive lines)을 형성하기 위해서 상기 제 3 도전막을 패터닝 하는 단계를 더 포함하는 임베디드 DRAM의 제조 방법.

Claim 12:

As for claim 1, the manufacturing method of the embedded DRAM further including the step that pattern s the third conductive film for forming the step of formi ng the third conductive film on the fourth step of formi ng multiple fifth openings within the second insulating l ayer the part of the second conductive film connected to at least one conductive region is exposed the openi ng, and the fifth opening and the second dielectric laye r front surface it forms multiple fourth openings within t he second insulating layer the upper electrode of the s tep: each capacitor of forming the second insulating la yer on the second conductive film is exposed after the step of patterning the second conductive film, and the refractory metal oxide layer and the first conductive fil m and the multiple first conductive lines supplying the r eference voltage to the upper electrode of each capaci tor through the fourth opening and the multiple second conductive lines connected through the fifth opening t o at least one conductive region.

청구 13항:

제 12 항에 있어서, 상기 레퍼런스 전압은 1/2 Vcc 전압을 포함하는 임베디드 DRAM의 제조 방법.

Claim 13:

The manufacturing method of the embedded DRAM of claim 12, wherein the reference voltage comprises 1/2 Vcc voltage.

GF Exhibit 1124 - 2234/2704

청구 14항:

제 12 항에 있어서, 상기 제 3 도전막을 형성하는 단계는, 알루미늄, 구리, 또는 알루미늄-구리 합금을 증착 하는 단계인 임베디드 DRAM의 제조 방법.

Claim 14:

As for claim 12, the manufacturing method of the embedded DRAM in which the step of forming the third conductive film is aluminum, and the copper or the step of depositing the aluminum-copper alloy.

청구 15항:

제 1 항에 있어서, 상기 도전 영역은 상기 로직 FET의 제 3 또는 제 4 소오스/드레인 영역, 또는 제 2 게이트 전극을 나타내는 임베디드 DRAM의 제조 방법.

Claim 15:

As for claim 1, the manufacturing method of the embedded DRAM in which the conductive region shows the third of the logic FET or the fourth source/drain region or the second gate electrode.

청구 16항:

메모리 회로 영역 및 로직 회로 영역을 갖는 반도체 기판을 준비하는 단계; 상기 메모리 회로 영역은 적어도 하나의 트랜스퍼 FET를 갖고, 트랜스퍼 FET는 제 1 및 제 2 소오스/드레인 영역과 제 1 게이트 전극을 포함하고, 상기 로직 회로 영역은 적어도 하나의 로직 FET를 갖고, 로직 FET는 제 3 및 제 4 소오스/드레인 영역과 제 2 게이트 전극을 포함하며, 반도체 기판 전면에 제 1 절연막을 형성하는 단계; 상기 제 1 절연막을 패터닝 하여 상기 메모리 회로 영역 상에 제 1 및 제 2 오프닝을 형성하고, 상기 로직 회로 영역 상에 제 3 오프닝을 형성하는 단계; 상기 제 1 및 제 2 오프닝 각각은 상기 트랜스퍼 FET의 각 제 1 및 제 2 소오스/드레인 영역을 노출시키고, 각 제 3 오프닝은 상기 로직 회로 영역 내의 도전 영역들 중 적어도 하나를 노출시키며, 상기 제 1 , 제 2 , 그리고 제 3 오프닝을 완전히 채우지 않고 덮도록 상기 제 1 절연막 상부에 제 1 도전막을 형성하는 단계; 상기 제 1 도전막 전면에 내열 금속 산화막을 형성하는 단계; 상기 내열 금속 산화막 상에 마스크막을 형성하되, 적어도 상기 제 1 오프닝을 덮고 적어도 상기 제 2 오프닝 및 제 3 오프닝을 노출시키도록 형성하는 단계; 상기 노출된 내열 금속 산화막이 전기적으로 도전막이 되도록 변화시키기 위해 수소 처리를 수행하는 단계; 상기 마스크막을 제거하는 단계; 상기 내열 금속 산화막 상에 제 2 도전막을 형성하는 단계; 및 상기 제 2 도전막, 내열 금속 산화막, 그리고 제 1 도전막을 패터닝 하여 상기 각 제 1 오프닝 상부에 커패시터 상부전극, 유전막, 그리고 하부전극을 각각 형성하고, 상기 각 제 2 및 제 3 오프닝 상부에 제 1 및 제 2 콘택 상호연결을 형성하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

Claim 16:

The memory circuit domain and the semiconductor substrate having the logic circuit area, and the transfer FET is first and second source/drain region and the first gate electrode the memory circuit domain has at least one transfer FET are included ; the logic circuit area has at least one logic FET ; the logic FET includes the third and fourth source/drain region and the second gate electrode ; the first step of forming the first insulating layer on the semiconductor substrate front board the insulating layer is patterned and first and second opening are formed on the memory circuit domain ; step: first and second opening of forming the third opening on the logic circuit area expose each first and second source/drain region of the transfer FET ; and each third opening exposes at least one among the conductive regions within the logic circuit area. The manufacturing method of the embedded DRAM including forming first and second contact interconnection at the upper part of each second and the third opening the mask film is formed on the step: step: refractory metal oxide layer of forming the refractory metal oxide layer on the first conductive film front side of forming the first conductive film on the first top portion of dielectric layer to completely nots fill up and cover first and second , and the third opening.

청구 17항:

제 16 항에 있어서, 상기 내열 금속 산화막을 형성하는 단계는, 티타늄 옥사이드(TiO2), 탄탈륨 펜톡사이드(Ta2O5), 페로스 옥사이드(Fe2O3), 그리고 바륨 티타늄 옥사이드(BaTiO3)를 포함하는 그룹에서 선택된 산화막들 중 하나를 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

Claim 17:

The manufacturing method of the embedded DRAM of claim 16, wherein step of forming the refractory metal oxide layer comprises a step of depositing one among the oxide film selected in the group including the titanium oxide (TiO2), the tantalum pentoxide (Ta2O5), and the ferrous oxide (Fe2O3) and barium titanium oxide (BaTiO3).

청구 18항:

제 16 항에 있어서, 마스크막을 형성하는 단계는, 포토레지스트막을 형성하기 위해서 포토레지스트 물질 또는 배리어막을 형성하기 위해서 확산 배리어 물질을 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

Claim 18:

The manufacturing method of the embedded DRAM of claim 16, wherein step of forming the mask film comprises a step of depositing the diffusion-barrier material the photoresist material or the barrier film is formed in order to form the photoresist film.

청구 19항:

Claim 19:

GF Exhibit 1124 - 2235/2704

제 16 항에 있어서, 수소 처리를 수행하는 단계는, 수소 플라즈마 처리 또는 핫 수소 처리를 사용하여 수행되는 단계인 임베디드 DRAM의 제조 방법.

As for claim 16, the manufacturing method of the embedded DRAM in which the step of performing the hydrogen treatment is the hydrogen plasma treatment or the step of being performed using the hot hydrogen treatment.

청구 20항:

Claim 20:

제 16 항에 있어서, 상기 제 1 도전막을 형성하는 단계는, 티타늄 또는 텅스텐을 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

The manufacturing method of the embedded DRAM of claim 16, wherein step of forming the first conductive film comprises a step of depositing titanium or tungsten.

청구 21항:

Claim 21:

제 16 항에 있어서, 상기 제 1 도전막을 형성하는 단계는, 티타늄 질화막을 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

The manufacturing method of the embedded DRAM of claim 16, wherein step of forming the first conductive film comprises a step of depositing the TiN film.

청구 22항:

Claim 22:

제 16 항에 있어서, 상기 제 1 도전막을 형성하는 단계는, 반도체 기판과 티타늄 질화막 사이에 티타늄막이 삽입되도록 티타늄 및 티타늄 나이트라이드를 차례로 증착 하는 단계를 더 포함하는 임베디드 DRAM의 제조 방법.

As for claim 16, the manufacturing method of the embedded DRAM wherein forming the first conductive film further includes depositing the successively titanium and titanium nitride such that the titanium film is inserted between the semiconductor substrate and TiN film.

청구 23항:

Claim 23:

제 16 항에 있어서, 상기 제 2 도전막을 형성하는 단계는, 텅스텐을 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

The manufacturing method of the embedded DRAM of claim 16, wherein step of forming the second conductive film comprises a step of depositing tungsten.

청구 24항:

Claim 24:

제 16 항에 있어서, 상기 커패시터 상부전극의 측벽 에지는, 상기 커패시터 하부전극의 측벽 에지와 일직선이 되도록 하는 임베디드 DRAM의 제조 방법.

As for claim 16, the sidewall edge of the capacitor upper part electrode is the manufacturing method of the sidewall edge of the capacitor lower part electrode and the embedded DRAM which it does in order to be straight.

청구 25항:

Claim 25:

제 16 항에 있어서, 상기 방법은, 내열 금속 산화막을 형성하는 단계 전에 제 1 도전막을 패터닝 하는 단계를 더 포함하는 임베디드 DRAM의 제조 방법.

The manufacturing method of the embedded DRAM of claim 16, wherein the method further comprises patterning the first conductive film before the step of forming the refractory metal oxide layer.

청구 26항:

Claim 26:

제 16 항에 있어서, 상기 방법은, 상기 수소 처리 수행 단계 전에 내열 금속 산화막내열 금속 산화막을 패터닝 하는 단계를 더 포함하는 임베디드 DRAM의 제조 방법.

The manufacturing method of the embedded DRAM of claim 16, wherein the method further comprises patterning the refractory metal oxide layer refractory metal oxide layer before the hydrogen treatment execute phase.

청구 27항:

Claim 27:

제 16 항에 있어서, 제 2 도전막, 내열 금속 산화막, 그리고 제 1 도전막을 패터닝 하는 단계는, 제 2 도전막 상에 제 2 절연막을 형성하는 단계; 상기 커패시터의 상부전극이 노출되도록 제 2 절연막 내에 제 4 오프닝을 형성하고, 적어도 하나의 도전 영

As for claim 16, the manufacturing method of the embedded DRAM wherein patterning the second conductive film, and the refractory metal oxide layer and the first conductive film includes patterning the third conduc

GF Exhibit 1124 - 2236/2704

역과 연결되는 제 2 도전막의 일부가 노출되도록 제 2 절연막 내에 제 5 오프닝을 형성하는 단계; 상기 제 4 오프닝, 제 5 오프닝, 그리고 제 2 절연막 전면에 제 3 도전막을 형성하는 단계; 및 상기 제 4 오프닝을 통해 상기 각 커패시터의 상부전극으로 레퍼런스 전압을 공급하는 제 1 도전 라인과, 상기 제 5 오프닝을 통해 적어도 하나의 도전 영역과 각각 연결되는 제 2 도전 라인을 형성하기 위해서 상기 제 3 도전막을 패터닝 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

tive film the fourth opening is formed within the second insulating layer so that the upper electrode of the ste p: capacitor of forming the second insulating layer on t he second conductive film is exposed.

청구 28항:

Claim 28:

제 27 항에 있어서, 상기 레퍼런스 전압은, 1/2 Vcc 전압을 포함하는 임베디드 DRAM의 제조 방법.

The manufacturing method of the embedded DRAM of claim 27, wherein the reference voltage comprises 1/2 Vcc voltage.

청구 29항:

Claim 29:

제 27 항에 있어서, 상기 제 3 도전막을 형성하는 단계는, 알루미늄, 구리 또는 알루미늄-구리 합금을 증착 하는 단계를 포함하는 임베디드 DRAM의 제조 방법.

The manufacturing method of the embedded DRAM of claim 27, wherein step of forming the third conductive f ilm comprises a step of depositing aluminum, and the c opper or the aluminum-copper alloy.

청구 30항:

Claim 30:

제 16 항에 있어서, 상기 도전 영역은, 로직 FET의 제 3 또는 제 4 소오스/드레인 영역, 또는 제 2 게이트 전극을 나타내는 임베디드 DRAM의 제조 방법.

As for claim 16, the manufacturing method of the embedded DRAM which the conductive region shows th e third of the logic FET or the fourth source/drain regio n or the second gate electrode.

배경기술

Background Art

본 발명은 DRAM(dynamic random access memory)의 제조 방법에 관한 것으로, 좀 더 구체적으로는 임베디드(embedded) DRAM의 제조 방법에 관한 것이다.

The invention relates to the manufacturing method of the DRAM (dynamic random access memory), more spe cifically, to the manufacturing method of the embedded DRAM.

임베디드 DRAM은 반도체 기판 내에 DRAM 회로(DRAM circuits)와 로직 회로(logic circuits)가 함께 결합된 집적회로(integrated circuit; IC) 형태이다. 현재, 반도체 집적 회로의 제조 경향은 메모리 셀 어레이와 고속(high speed) 로직 회로 요소(elements)를 집적하는 것이다. 예를 들어, 마이크로프로세서(microprocessors) 또는 디지털 신호 처리기(digital signal processors)는 모두 임베디드 메모리와 결합된 집적회로를 갖는다.

It is the DRAM circuit (DRAM circuits) and the integrated circuit (integrated circuit: IC) form in which the logic circuit (logic circuits) is coupled together with in the embedded DRAM silver semiconductor substrate. The present , and the manufacturing trend of the semi conductor IC(integrated circuit) accumulate the memor y cell array and high speed (high speed) logic circuit el ement (elements). For example, the microprocessor (mi croprocessors) or the digital signal processing (digital si gnal processors) has altogether, the embedded memory and the combined integrated circuit.

요즈음, 반도체 제조자들은 생산 단가(production cost)를 유지하거나 낮추면서 소자의 성능(functionality)을 향상시키기 위해 노력하고 있다. 소형화 및 서브 미크론(sub-micron) 반도체 소자의 제조에 의해서, 성능 향상 및 생산 단가 감소의 목적이 부분적으로 충족되고 있다. 서브 미크론(sub-micron) 기술은 소자의 기능 저하와 기생 커패시턴스(parasitic capacitance)를 감소시킬 수 있기 때문에 소자의 성능을 향상시킬 수 있다. 더구나, 서브 미크론 기술은 보다 작은 반도체 칩(chip)을 생산해 낸다. 작은 크기의 칩 기능이 큰 칩과 유사하므로, 더 많은 실리콘 칩이 주어진 크기의 실리콘 웨이퍼 상에서 제조된다. 따라서, 각 칩의 평균 생산 단가가 더 낮아진다.

These days, it makes every effort while semiconductor manufacturers maintain the production cost or it lowers the element performance (functionality) is improved. T he object of the performance improvement by the man ufacture of the miniaturization and submicron (sub-micr on) semiconductor device and decrease of production cost are partly satisfied. The element performance can be improved because the submicron (sub-micron) tech nology can reduce the depression and parasitic capacit ance of the device. Moreover, the semiconductor chip smaller than the submicron technology is produced. It i s similar to the chip in which the chip function of the s mall size is large. Therefore the chip is manufactured o n the silicon wafer of the size in which more silicon chip s are given. Therefore, the average production cost of

GF Exhibit 1124 - 2237/2704

the angular chip is lower.

다른 반도체 제조자들은 반도체 칩 내에 로직 회로 요소와 메모리 소자를 집적화하고 있다. 이것은 소자의 성능을 향상시킬 뿐 아니라 생산 단가를 줄이는 장점을 갖는다. 집적화는 로직 소자에 대한 반도체 칩의 일 부분의 메모리 소자에서 다른 반도체 칩의 다른 부분의 로직 소자로 전송되는 신호의 시간 딜레이(time delay)를 줄임으로써 성능을 향상시킨다. 게다가, 하나의 반도체 칩 상에 메모리와 로직 소자를 결합함으로써, 대부분 공통된 공정 단계를 공유할 수 있기 때문에 생산 단가가 낮아지게 된다.

Dissimilar semiconductor manufacturers integrate the logic circuit element and memory device within the semiconductor chip. It has the advantage this improves the element performance of decreasing the production cost. The performance is improved by reducing the time delay of the signal in which integration is transmitted from the memory device of one part of the semiconductor chip about the logic device to the logic device of the dissimilar part of the dissimilar semiconductor chip. Moreover, the memory and logic device are combined on one semiconductor chip. In that way because the processing stage which is mostly common can be shared the production cost is decreased.

하나의 단일 칩 내에 로직 회로와 메모리를 집적하는 방법을 제공하기 위한 시도가 다방면의 반도체 제조자들에 의해 행해지고 있다. 예를 들어, 미국 특허 No.5,292,677에서 Dennison et al.은 단일 반도체 칩(single semiconductor chip) 상에 CMOS(complementary metal oxide semiconductor) 소자와 DRAM 소자를 제조하는 방법을 제안하였다. 그러나, 이 두 요소를 제조함에 있어서, 상기 방법은 많은 제조 단계를 공유하지 못하고, 따라서 생산 단가에 두드러지게 영향을 주지 못한다. 또한, 상기 방법은 고효율(high-efficiency) 로직 소자의 제조를 포함하지 않는다.

The attempt for providing the method for accumulating the logic circuit and memory within one one-chip is performed with the semiconductor manufacturers of many quarters. For example, in USNo.5,292,677 A, the CMOS (complementary metal oxide semiconductor) device and the method for manufacturing the DRAM device were suggested on the Dennison et al silver. single semiconductor chip. But this two elements are manufactured. The manufacturing step that the method is many is unable to be shared and therefore it outstandingly is unable to affect the production cost. Moreover, the method does not include the manufacture of the high efficiency (high-efficiency) logic device.

단일 반도체 칩 상에 고효율 고속 로직 회로와 메모리 소자를 제조하기 위해서, 많은 제조 관점이 고려되어져야 한다. 가장 흔하게, 고려 사항은 로직 회로 공정 또는 메모리 회로에 관한 것이고, 둘 다의 관점은 거의 함께 고려되지 않는다.

To produce the high efficiency fast logic circuit on the single semiconductor chip and memory device, many making viewpoint is considered. Most, common. The consideration is about the logic circuit process or the memory circuit and the viewpoint of both is not nearly together considered.

상술한 바와 같이, 단일 실리콘 칩 상에 로직과 메모리 회로를 집적하는 개선된 방법이 요구된다.

As described above, the improved method for accumulating logic and memory circuit on the single silicon chip is required.

발명의 내용

Summary of Invention

발명의 효과

Effects of the Invention

본 발명은 본 발명은 메모리 회로들과 로직 회로들을 함께 결합할 수 있고, 따라서 실리콘 웨이퍼에 대한 좋은 표면 평탄도를 유지하면서 생산 단가를 줄일 수 있는 효과가 있다.

The present invention has the effect that the invention together can combine the memory circuits and logic circuits and therefore the production cost can be decreased while the good surface flatness about the silicon wafer is maintained.

기술적 과제

Technical Task

본 발명은 상술한 제반 문제점을 해결하기 위해 제안된 것으로서, 고효율 고성능 로직 소자의 제조와 공유하는 공정 단계의 수를 증가시킬 수 있고, 따라서 생산 단가를 감소시킬 수 있는 임베디드 메모리 제조 방법을 제공함에 그 목적이 있다.

An object of the present invention is to provide the embedded memory manufacturing method it can increase the number of processing stage to solve the above-described overall problem, being proposed and of sharing with the manufacture of the high efficiency highly efficient logic devices and therefore for reducing the production cost.

본 발명의 다른 목적은 메모리 소자 영역의 상부 표면과 로직 회로 영역의 상부 표면이 동일한 높이를 갖고, 따라서 집적 회

It is another object of the present invention to provide the manufacturing method of the embedded DRAM whic

GF Exhibit 1124 - 2238/2704

로의 평탄도(degree of planarity)를 증가시킬 수 있는 임베디드 DRAM의 제조 방법을 제공함에 있다.

h has the height in which the top surface of the memory device area and top surface of the logic circuit area are identical and therefore can increase the planarity (degree of planarity) of the integrated circuit.

본 발명의 또 다른 목적은 개선된 임베디드 DRAM의 제조 방법을 제공함에 있다. 이 방법은 높은 종횡비(high aspect ratio)를 갖는 콘택홀 전면에 내열 금속 산화막이 증착된다. 다음, 상기 내열 금속 산화막이 전기적 비도전성에서 도전성으로 변화되도록 하기 위해서 상기 증착된 내열 금속 산화막이 수소 플라즈마(hydrogen plasma) 또는 핫 수소(hot hydrogen)에 의해 처리된다.

It is another object of the present invention to provide the manufacturing method of the improved embedded DRAM. The refractory metal oxide layer is deposited in the contact hole front side having the aspect ratio (high aspect ration) in which this method is high. In the next refractory metal oxide layer is the non-electrically-conductive, the above-mentioned deposited refractory metal oxide layer is processed by the hydro plasma (hydrogen plasma) or the hot hydrogen in order to makes be changed to conductivity.

본 발명의 또 다른 목적은 임베디드 DRAM의 제조 방법을 제공함에 있다. 이 방법은 높은 종횡비를 갖는 콘택홀 전면에 내열 금속 산화막이 증착된다. 다음, 상기 콘택홀 상에 증착된 내열 금속 산화막의 일부를 처리하기 위해 수소 플라즈마 또는 핫 수소가 사용된다. 수소 플라즈마 또는 핫 수소에 의해 처리된 내열 금속 산화막의 일부는 전기적 비도전성에서 도전성으로 변화된다. 한편, 수소 플라즈마 또는 핫 수소 처리에 노출되지 않은 내열 금속 산화막의 일부는 비도전성으로 남고, DRAM 커패시터의 유전막으로 사용될 수 있다.

It is another object of the present invention to provide the manufacturing method of the embedded DRAM. The refractory metal oxide layer is deposited in the contact hole front side having the aspect ratio in which this method is high. The hydro plasma or the hot hydrogen is used in order to handle the part of the refractory metal oxide layer deposited on the next contact hole. The part of the refractory metal oxide layer processed by the hydro plasma or the hot hydrogen is changed to conductivity in the non-electrically-conductive. In the meantime, the part of the refractory metal oxide layer which is not exposed to the hydro plasma or the hot hydrogen treatment may be used with the dielectric layer of the DRAM capacitor it remains with the non-conductive.

발명의 구성 및 작용

Structure & Operation of the Invention

(구성)

(configuration)

상술한 목적을 달성하기 위한 본 발명에 의하면, 임베디드 DRAM의 제조 방법은, 먼저 미리 정의된 메모리 회로 영역 및 로직 회로 영역을 갖는 반도체 기판이 준비된다. 다음, 복수의 트랜스퍼 전계효과 트랜지스터가 메모리 회로 영역에 형성되고, 이때 각 트랜스퍼 전계효과 트랜지스터는 제 1 및 제 2 소오스/드레인 영역과 제 1 게이트 전극을 갖는다. 복수의 로직 전계효과 트랜지스터가 로직 회로 영역에 형성되고, 이때 각 로직 전계효과 트랜지스터는 제 3 및 제 4 소오스/드레인 영역과 제 2 게이트 전극을 갖는다.

The manufacturing method of the embedded DRAM for achieving the above-described purpose the memory circuit domain defined in advance and the semiconductor substrate having the logic circuit area are prepared. Each transfer field effect transistor the transfer field effect transistor of the next plurality is formed in the memory circuit domain has first and second source/drain region and the first gate electrode. Each logic field effect transistor multiple logic field effect transistors are formed in the logic circuit area has the third and the fourth source/drain region and the second gate electrode.

상기 반도체 기판 전면에 제 1 절연막이 형성된 후, 메모리 회로 영역 내에 복수의 제 1 및 제 2 오프닝을 형성하기 위해서 각 트랜스퍼 전계효과 트랜지스터의 제 1 및 제 2 소오스/드레인 영역이 노출되도록 상기 제 1 절연막이 패터닝 된다. 유사하게, 복수의 제 3 오프닝이 상기 로직 회로 영역 내에 형성되고, 각 제 3 오프닝은 상기 로직 회로 영역 내의 적어도 하나의 도전막 영역이 노출되도록 형성된다.

After the first insulating layer is formed in the semiconductor substrate front board the first insulating layer is patterned so that first and second source/drain region of each transfer field effect transistor are exposed in order to form multiple first and second openings within the memory circuit domain. Similarly, multiple third openings are formed within the logic circuit area and each third opening is formed so that at least one conductive film domain within the logic circuit area is exposed.

다음, 상기 제 1 절연막 전면에 제 1 도전막이 형성된다. 상기 제 1 도전막은 상기 제 1 및 제 2 , 그리고 제 3 오프닝을 덮되, 상기 오프닝들을 완전히 채우지는 않는다. 다음, 상기 제 1 도전막 전면에 내열 금속 산화막이 형성된다. 상기 내열 금속 산

The first conductive film is formed in the next first dielectric layer front surface. The first conductive film covers first and second , and the third opening. Openings are not completely filled up. The refractory metal oxi

GF Exhibit 1124 - 2239/2704

화막 전면에 마스크층(mask layer)을 형성하되, 적어도 상기 제 1 오프닝을 덮고, 적어도 상기 제 2 오프닝과 제 3 오프닝을 노출하도록 형성한다. 상기 노출된 내열 금속 산화막을 도전막으로 변화시키기 위해서 수소 처리가 수행된다. 마스크층이 제거된다. 그 후, 상기 내열 금속 산화막 전면에 제 2 도전막이 형성된다. 제 2 도전막, 내열 금속 산화막, 그리고 제 1 도전막이 패터닝 된다. 그 결과, 각 제 1 오프닝 상부에 커패시터의 상부전극, 유전막, 그리고 하부전극이 형성되고, 각 제 2 및 제 3 오프닝 상부에 제 1 및 제 2 콘택 상호연결이 각각 형성된다.

de layer is formed in the next first conductive film front side. The mask layer is formed on the refractory metal oxide layer front side. At least first opening is covered and at least second opening and the third opening are formed in order to expose. The hydrogen treatment is p erformed in order to diversify the above-mentioned exp osed refractory metal oxide layer to the conductive fil m. The mask layer is removed. Thereafter, the second conductive film is formed in the refractory metal oxide l ayer front side. The second conductive film, and the re fractory metal oxide layer and the first conductive film are patterned. Consequently, the upper electrode of th e capacitor, and the dielectric layer and bottom electro de are formed at the upper part of each first opening a nd first and second contact interconnection are formed respectively at the upper part of each second and the third opening.

이 방법의 바람직한 실시예에 있어서, 제 1 도전막이 내열 금속 산화막 형성 전에 패터닝 될 수 있다. 또한, 내열 금속 산화막은 수소 처리 전에 패터닝될 수 있다.

The first conductive film can be patterned to a preferred embodiment of this method before the refract ory metal oxide layer formation. Moreover, the refracto ry metal oxide layer can be patterned before the hydro gen treatment.

상술한 목적을 달성하기 위한 다른 본 발명에 의하면, 임베디드 DRAM의 제조 방법은 먼저, 제 2 도전막 상에 제 2 절연막이 형성된다. 각 커패시터의 상부전극이 노출되도록 상기 제 2 절연막 내에 복수의 제 4 오프닝이 형성되고, 상기 적어도 하나의 다른 도전막에 전기적으로 연결되는 제 2 도전막이 일부가 노출되도록 제 2 절연막 내에 복수의 제 5 오프닝이 형성된다. 상기 제 4 및 제 5 오프닝을 채우고 상기 제 2 절연막을 덮도록 제 3 도전막이 형성된다. 상기 제 3 도전막이 패터닝 되어 상기 제 5 오프닝을 통해 적어도 하나의 도전 영역(conductive region)에 각각 연결되는 복수의 제 2 도전 라인 뿐아니라, 각각 제 4 오프닝 및 상기 커패시터의 상부전극을 통해 레퍼런스 전압(reference voltage)에 연결되는 복수의 제 1 도전 라인(first conductive line)이 형성된다.

The second insulating layer the dissimilar manufacturing method of the embedded DRAM for achieving the abov e-described purpose is formed on the second conductiv e film in advance. Multiple fourth openings are formed within the second insulating layer so that the upper ele ctrode of each capacitor is exposed and multiple fifth o penings are formed within the second insulating layer s o that the part of the second conductive film which is electrically connected to at least one dissimilar conduc tive film is exposed. The third conductive film is formed in order to fill up the fourth and fifth opening and cover the second insulating layer. The third conductive film is patterned and the multiple first conductive lines conne cted to the reference voltage through the upper electr ode of the capacitor and fourth opening not only the m ultiple second conductive lines, connected to at least one conductive region through the fifth opening is form ed.

상술한 목적을 달성하기 위한 또 다른 발명에 의하면, 임베디드 DRAM의 제조 방법은, 먼저 메모리 회로 영역과 로직 회로 영역이 이미 정의된 반도체 기판이 준비된다. 적어도 하나의 트랜스퍼 전계효과 트랜지스터가 제 1 및 제 2 소오스/드레인 영역과 제 1 게이트 전극을 갖는 전계효과 트랜지스터를 구비한 메모리 회로 영역에 형성된다. 적어도 하나의 전계효과 트랜지스터가 제 3 및 제 4 소오스/드레인 영역과 제 2 게이트 전극을 갖는 로직 전계효과 트랜지스터를 구비한 로직 회로 영역에 형성된다.

The manufacturing method of the embedded DRAM the memory circuit domain and the semiconductor substrat e in which the logic circuit area is already defined are p repared according to another invention for achieving th e above-described purpose in advance. It is formed in t he memory circuit domain equipped with the field effect transistor in which at least one transfer field effect tra nsistor has first and second source/drain region and th e first gate electrode. It is formed in the logic circuit ar ea equipped with the logic field effect transistor in whi ch at least one field effect transistor has the third and fourth source/drain region and the second gate electro de.

반도체 기판 전면에 제 1 절연막이 형성된 후, 트랜스퍼 전계효과 트랜지스터의 제 1 및 제 2 소오스/드레인 영역이 노출되는 메모리 회로 영역 내에 제 1 오프닝 및 제 2 오프닝을 형성하기 위해 상기 제 1 절연막이 패터닝 된다. 유사하게, 로직 회로 영

After the first insulating layer is formed in the semiconductor substrate front board in order to form th e first opening and the second opening within the mem ory circuit domain in which first and second source/drai

GF Exhibit 1124 - 2240/2704

역 내에 적어도 하나의 도전 영역이 노출되도록 하는 제 3 오프닝이 형성된다. 상기 제 1 절연막 전면에 제 1 도전막이 형성된다. 제 1 도전막이 제 1 및 제 2 , 그리고 제 3 오프닝을 채운다. 상기 제 1 도전막 전면에 내열 금속 산화막이 증착된다. 적어도 상기 제 1 오프닝을 덮고, 적어도 상기 제 2 및 제 3 오프닝 상부 영역이 노출되도록 내열 금속 산화막 전면에 마스크층이 형성된다.

n region of the transfer field effect transistor are exposed, the first insulating layer is patterned. Similarly, the third opening in which at least one conductive region is exposed within the logic circuit area is formed. The first conductive film is formed in the first dielectric layer front surface. The first conductive film fills up first and second , and the third opening. The refractory metal oxide layer is deposited in the first conductive film front side. At least first opening is covered and the mask layer is formed in the refractory metal oxide layer front side so that at least second and the third opening upper region are exposed.

상기 노출된 도전막 내의 내열 금속 산화막을 변화시키기 위해서 수소 처리가 수행된다. 마스크층이 제거된다. 그 후, 상기 내열 금속 산화막 전면에 제 2 도전막이 형성된다. 제 2 도전막, 내열 금속 산화막, 그리고 제 1 도전막이 패터닝 된다. 마지막으로, 커패시터의 상부전극, 유전막, 그리고 하부전극이 제 1 오프닝의 상부에 형성되고, 상기 제 2 오프닝 및 제 3 오프닝 상부에 각각 제 1 및 제 2 콘택 상호연결이 형성된다.

In order to change the refractory metal oxide layer within the above-mentioned exposed conductive film, the hydrogen treatment is performed. The mask layer is removed. Thereafter, the second conductive film is formed in the refractory metal oxide layer front side. The second conductive film, and the refractory metal oxide layer and the first conductive film are patterned. Finally, the upper electrode of the capacitor, and the dielectric layer and bottom electrode are formed in upper part of the first opening and first and second contact interconnection are formed at the upper part of the second opening and the third opening.

이 방법의 바람직한 실시예에 있어서, 임베디드 DRAM의 제조 방법은 다음의 단계를 더 포함한다. 즉, 상기 제 2 도전막 상에 제 2 절연막이 형성된다. 제 2 절연막 내에 제 4 오프닝이 형성된다. 상기 커패시터의 상부전극이 노출되도록 제 2 절연막 내에 제 4 오프닝이 형성되고, 적어도 하나의 제 1 도전막과 전기적으로 연결되는 제 2 도전막의 일부가 노출되도록 제 2 절연막 내에 제 4 오프닝이 형성된다. 다음, 상기 제 4 및 제 5 오프닝을 채우고 상기 제 2 절연막을 덮도록 제 3 도전막이 형성된다. 상기 제 3 도전막이 패터닝 되어 상기 제 5 오프닝을 통해 적어도 하나의 도전 영역과 연결되는 제 2 도전 라인 뿐아니라 제 4 오프닝 및 커패시터의 상부전극을 통해 레퍼런스 전압에 연결되는 제 1 도전 라인이 형성된다.

In a preferred embodiment further the manufacturing method of the embedded DRAM includes the following step of this method. That is, the second insulating layer is formed on the second conductive film. The fourth opening is formed within the second insulating layer. The fourth opening is formed within the second insulating layer so that the upper electrode of the capacitor is exposed and the fourth opening is formed within the second insulating layer so that the part of the second conductive film which is electrically connected with at least one first conductive film is exposed. The third conductive film is formed in order to fill up the next fourth and fifth opening and cover the second insulating layer. The third conductive film is patterned and the first conductive line connected to the reference voltage through the upper electrode of not only the second conductive line but also the fourth opening and the capacitor connected through the fifth opening to at least one conductive region is formed.

상술한 바와 같은 일반적인 설명 및 다음의 상세 설명 둘 다는 실시예로서, 클레임된 본 발명을 더 상세히 설명하고자 한다.

As the general description as described above and the following full description both is the embodiment, the claimed invention tries to be more particularly illustrated.

(작용)

(action)

도 1b를 참조하면, 본 발명의 실시예에 따른 신규한 임베디드 DRAM의 제조 방법은, 수소 플라즈마 또는 핫 수소 처리를 통해 상기 콘택홀 상에 증착된 내열 금속 산화막의 일부가 비도전성에서 도전성 물질로 변화된다. 반면, 처리되지 않은 내열 금속 산화막의 부분은 비도전성으로 남게 된다. 이때, 처리되지 않은 내열 금속 산화막은 DRAM 커패시터의 유전막으로 사용될 수 있다. 이로써, 메모리 회로들과 로직 회로들을 함께 결합할 수 있고, 실리콘 웨이퍼에 대한 좋은 표면 평탄도를 유지하면서 생산 단가를 줄일 수 있다.

Referring to Figure 1b, as to the manufacturing method of the embedded DRAM which is novel according to a preferred embodiment of the present invention, the part of the refractory metal oxide layer deposited through the hydro plasma or the hot hydrogen treatment on the contact hole is changed to the conductive material in the non-conductive. On the other hand, the part of the refractory metal oxide layer which is not processed remains as the non-conductive. Then, the refractory metal oxide layer which is not processed can be used as the dielectric layer of the DRAM capacitor. Therefore, the memory circuits and logic circuits can be together combined and while the good surface flatness about the sili

GF Exhibit 1124 - 2241/2704

con wafer is maintained the production cost can be de creased.

(실시예)

(embodiment)

이하, 도 1을 참조하여 본 발명의 실시예를 상세히 설명한다.

Hereinafter, referring to Figure 1, the embodiment of the invention is particularly illustrated.

도면과 상세 설명에 있어서, 동일하거나 그와 유사한 부분에 대해서는 가능한 동일한 참조 번호가 사용된다.

As to drawing and full description, it is identical or the possible same reference number is used about the part which is similar to that.

티타늄 옥사이드(titanium oxide)(TiO2), 탄탈륨 펜톡사이드(tantalum pentoxide)(Ta2O5), 페로스 옥사이드(ferrous oxide)(Fe2O3), 그리고 바륨 티타늄 옥사이드(barium titanium oxide)(BaTiO3)와 같은 내열 금속 산화막은 넓은 밴드 갭(wide band-gap)의 절연 물질이다. 만일, 내열 금속 산화막의 금속 이온들 또는 수소 베이컨시(vacancy)들 사이에 수소를 주입하기 위해 수소 플라즈마 처리 또는 핫 수소 처리가 수행된다면, 내열 금속 산화막 내의 산소 함량(oxygen content)이 감소된다. 따라서, 내열 금속 산화막은 n형 도전 산화막으로 바뀌게 될 것이다. 다시 말해, 원래의 내열 금속 산화막이 절연 특성(insulating properties)을 갖는 물질에서 반도체(semiconductive) 또는 도전(conductive) 특성을 갖는 물질로 변환될 것이다. 반응 메커니즘(reaction mechanism)은 다음의 식으로 요약된다.

The titanium oxide (titanium oxide) (TiO2), the tantalum pentoxide (tantalum pentoxide) (Ta2O5) , and the refractory metal oxide layer like the ferrous oxide (ferrous oxide) (Fe2O3) and barium titanium oxide (barium titanium oxide) (BaTiO3) are the insulation material of the wide band gap (wide band-gap). If the hydrogen plasma treatment or the hot hydrogen treatment is performed in order to inject hydrogen between the metal ions or hydrogen vacancy of the refractory metal oxide layer the oxygen content within the refractory metal oxide layer is reduced. Therefore, the refractory metal oxide layer is changed to the n-type conductive oxide. In other words, in the material in which the original refractory metal oxide layer has the insulation property (insulating properties), it will be transformed to the material having the semiconductor (semiconductive) or the electric conduction (conductive) property. The reaction mechanism is summarized to the following formula.

[반응식]

[Equation]

$O^{2-} \rightarrow 12O_2 + 2e^-$

$O^{2-} \rightarrow 12O_2 + 2e^-$

수소 플라즈마 처리 또는 핫 수소 처리 후의 내열 금속 산화막의 전기적 도전성은 그 산소 함량에 의존하기 때문에, 내열 금속 산화막은 반도체 물질 또는 도전 물질로 만들어 질 수 있다. 또한, 내열 금속 산화막이 도전 물질로 바뀌었을 때의 저항값(resistance value)은 알맞게 조절될 수 있다.

The electrical conductivity of the refractory metal oxide layer after the hydrogen plasma treatment or the hot hydrogen treatment depends on the oxygen content. Therefore the refractory metal oxide layer makes the semiconductor material or the conducting material. Moreover, the resistance value when the refractory metal oxide layer was changed to the conducting material can be controlled moderately.

내열 금속 산화막이 도전 물질로 변화되는 것과 관계된 방법들은 많은 간행물(articles)에서 볼 수 있다. 이러한 간행물들은 Fu-Tai Liou(본 발명의 발명자 중 하나임)에 의해 쓰여진 것으로서, 제목 "Semiconductor electrodes for photoelectrolysis"(1982년 뉴욕 주립대)로 발표된 것을 포함한다. C. Y. Yang et al.에 의해 쓰여진 두 번째 간행물은 제목 "Solid electrochemical modification of semiconductors"(Solid State Communication, Vol. 43, No. 8, pp. 633 - 636)로 발표되었다. 세 번째 간행물 또한 Fu-Tai Liou et al.에 의해 제목 "Photoelectrolysis at Fe2O3/TiO2 Heterojunction Electrode"(Journal of the Electrochemical Society, Vol. 129, No. 2, pp. 342 - 245)로 발표되었다.

The methods which the refractory metal oxide layer is changed to the conducting material is connected can look in many publication (articles). Such publications are used with the Fu-Tai Liou (it is one among the inventor of the invention). It includes being disclosed in the name of the title Semiconductor electrodes for photoelectrolysis (1982 year NewYork a state university). C. Y. The second publication which was due to the Yang et al and was used was disclosed in the name of the title Solid electrochemical modification of semiconductors (Solid State Communication, Vol. 43, No. 8, pp. 633 - 636). It was due to the third publication, moreover, the Fu-Tai Liou et al and it was disclosed in the name of the title Photoelectrolysis at Fe2O3 / TiO2 Heterojunction Electrode (Journal of the Electrochemical Society, Vol. 129, No. 2, pp. 342 - 245).

본 발명은 임베디드 DRAM을 형성하는 방법을 개선하기 위해서 상술한 간행물들에서 제안된 기술들이 사용된다. 본 발명의

Proposed technologies are used in publications which describe in detail it improves the method in which the i

GF Exhibit 1124 - 2242/2704

주된 특징은 큰 종횡비(high aspect ratio)를 갖는 콘택홀 전면에 내열 금속 산화막이 증착된다는 것이다. 콘택홀 상의 내열 금속 산화막의 전기 전도도는 수소 플라즈마 처리 또는 핫 수소 처리를 사용하여 비도전성에서 도전성으로 변화된다.

nvention forms the embedded DRAM. The refractory metal oxide layer is deposited in the contact hole front side having the aspect ratio (high aspect ratio) in which the main feature of the invention is large. In the conductivity of the refractory metal oxide layer on the contact hole is the non-conductive using the hydrogen plasma treatment or the hot hydrogen treatment, it is changed to conductivity.

도 1a 내지 도 1f는 본 발명의 실시예에 따른 임베디드 DRAM의 제조 방법의 단계들을 순차적으로 보여주는 단면도이다.

Figures 1a through 1f are the cross-sectional view which successively shows the steps of the manufacturing method of the embedded DRAM according to the embodiment of the invention.

먼저, 도 1a에서와 같이, 반도체 기판(100)이 준비된다. 반도체 기판(100)은 메모리 회로 영역(101)과 로직 회로 영역(102)으로 나누어질 수 있다. 상기 메모리 회로 영역(101)은 적어도 하나의 트랜스퍼 전계효과 트랜지스터(transfer FET; 이하, #39#트랜스퍼 FET#39#라 함)(103)를 갖는다. 트랜스퍼 FET(103)는 제 1 및 제 2 소오스/드레인 영역(104, 105), 그리고 제 1 게이트 전극(106)을 갖는다. 상기 로직 회로 영역(102)은 적어도 하나의 로직 전계효과 트랜지스터(이하, #39#로직 FET#39#라 함)(107)을 포함한다. 상기 로직 FET(107)는 제 3 및 제 4 소오스/드레인 영역(108, 109), 그리고 제 2 게이트 전극(110)을 갖는다. 반도체 기판(100) 전면에 제 1 절연막(111)이 형성된다. 다음, 메모리 회로 영역(101) 상에 제 1 오프닝(112) 및 제 2 오프닝(113)을 형성하기 위해 그리고, 로직 회로 영역(102) 상에 제 3 오프닝(114)을 형성하기 위해 상기 제 1 절연막(111)이 패터닝(patterning) 된다. 제 1 오프닝(112) 및 제 2 오프닝(113)은 각각 상기 트랜스퍼 FET의 제 1 및 제 2 소오스/드레인 영역(104, 105)을 노출시킨다. 상기 제 3 오프닝(114)은 상기 로직 회로 영역(102) 내의 적어도 하나의 도전 영역을 노출시킨다.

In advance, as shown in Figure 1a, the semiconductor substrate (100) is prepared. The semiconductor substrate (100) can be divided into the memory circuit domain (101) and logic circuit area (102). The memory circuit domain (101) has at least one transfer field effect transistor (it says to be the ' transfer FET' less than the transfer FET) (103). The transfer FET (103) has first and second source/drain regions (104, 105) and the first gate electrode (106). The logic circuit area (102) includes at least one logic field effect transistor (it the hereinafter says to be the ' logic FET') (107). The logic FET (107) has the third and fourth source/drain regions (108, 109) and the second gate electrode (110). The first insulating layer (111) is formed in the semiconductor substrate (100) front side. In order to form the third opening (114) on and, the logic circuit area (102) in order to form the first opening (112) and the second opening (113) on the next memory circuit domain (101), , the first insulating layer (111) is the patterning. The first opening (112) and the second opening (113) expose first and second source/drain regions (104, 105) of the transfer FET. The third opening (114) exposes at least one conductive region within the logic circuit area (102).

상기 노출된 도전 영역은 게이트 전극 또는 상기 로직 FET의 소오스/드레인 영역 중 하나일 수 있다. 예를 들어, 제 3 오프닝은 도 1a에 도시된 소오스/드레인 영역(108)을 노출시킨다. 상기 제 1 절연막(111) 전면에 제 1 도전막(115)이 형성된다. 상기 제 1 도전막(115)은 예를 들어, 금속 티타늄막(metallic titanium layer), 금속 텅스텐막(metallic tungsten layer), 티타늄 질화막(titanium nitride layer), 또는 티타늄/티타늄 질화막(titanium/titanium nitride layer)일 수 있다. 상기 제 1 도전막(115)은 제 1, 제 2, 그리고 제 3 오프닝(112, 113, 114)의 각각을 덮는다. 다음, 상기 제 1 도전막(115) 전면에 내열 금속 산화막(116)이 형성된다. 상기 내열 금속 산화막(116)을 형성하기 위해 티타늄 옥사이드(TiO2), 탄탈륨 펜톡사이드(Ta2O5), 페로스 옥사이드(Fe2O3), 그리고 바륨 티타늄 옥사이드(BaTiO3)가 사용될 수 있다. 여기서, 아직까지 내열 금속 산화막(116)은 절연막이다.

The above-mentioned exposed conductive region can be one among the source/drain region of the gate electrode or the logic FET. For example, the source/drain region (108) in which the third opening is illustrated in 1a is exposed. The first conductive film (115) is formed in the first insulating layer (111) front side. The first conductive film (115) may be for example, the metallic titanium layer, the metallic tungsten layer, and the TiN film (titanium nitride layer) or the titanium/titanium nitride layer. The first conductive film (115) covers the first, and each of the second and third openings (112, 113, 114). The refractory metal oxide layer (116) is formed in the next first conductive film (115) front side. The titanium oxide (TiO2), the tantalum pentoxide (Ta2O5), and the ferrous oxide (Fe2O3) and barium titanium oxide (BaTiO3) can be used in order to form the refractory metal oxide layer (116). Here, the so far the refractory metal oxide layer (116) is the insulating layer.

상기 제 1 도전막(115) 전면에 내열 금속 산화막(116)을 형성하기 전에 상기 제 1 도전막(115)이 패터닝 될 수 있다. 만일 상기 제 1 도전막(115)이 상기 내열 금속 산화막 증착 전에 패터닝 된다면, 후속 내열 금속 산화막 증착은 상기 제 1 도전막(115)의 가장자리(edge)를 덮게 된다.

The first conductive film (115) can be patterned before forming the refractory metal oxide layer (116) on the first conductive film (115) front side. If the first conductive film (115) is patterned to the if before the refractory metal oxide layer deposition the following refractory metal oxide layer deposition covers the edge of the first conductive film (115).

GF Exhibit 1124 - 2243/2704

다음, 도 1b를 참조하면, 상기 내열 금속 산화막(116) 전면에 마스크막(mask layer)(117)이 형성된다. 상기 마스크막(117)은 예를 들어, 적어도 상기 제 1 오프닝(112)을 덮고, 상기 제 2 오프닝(113) 및 제 3 오프닝(114)을 노출시키는 포토레지스트막(photoresist layer) 또는 확산 배리어막(diffusion barrier layer)일 수 있다. 예를 들어, 수소 플라즈마 처리 또는 핫 수소 처리와 같은 수소 처리(hydrogen treatment)후, 상기 노출된 내열 금속 산화막(116)은 도전막으로 변화된다. 상기 수소 처리 후, 내열 금속 산화막(116)의 노출된 부위는 도전성 내열 금속 산화막(116b)으로 변화되는 반면, 상기 노출되지 않은 내열 금속 산화막(116a)은 비도전성으로 남게 된다. 또한, 상기 내열 금속 산화막(116)은 상기 수소 처리가 수행되기 전에 패터닝될 수 있다.

Then, referring to Figure 1b, the mask film (mask layer) (117) is formed in the refractory metal oxide layer (116) front side. The mask film (117) covers for example, at least first opening (112) and it may be the second opening (113) and photoresist film (photoresist layer) or the diffusion barrier layer exposing the third opening (114). For example, the above-mentioned exposed refractory metal oxide layer (116) is changed to the conductive film after the hydrogen treatment such as the hydrogen plasma treatment and hot hydrogen treatment. Whereas the exposed site of the refractory metal oxide layer (116) is changed to the conductive refractory metal oxide layer (116b) after the hydrogen treatment the above-mentioned refractory metal oxide layer (116a) which is not exposed remains as the non-conductive. Moreover, the refractory metal oxide layer (116) can be patterned before the hydrogen treatment is performed.

이어서, 도 1c 및 도 1d에 있어서, 상기 마스크막(117)이 제거된다. 제 2 도전막(118) 예를 들어, 금속 텅스텐(metallic tungsten)이 상기 내열 금속 산화막(116)(116a 및 116b) 전면에 형성된다. 상기 제 2 도전막(118) 전면에 다른 마스크막(119)이 형성된다. 상기 제 2 도전막(118), 내열 금속 산화막(116), 그리고 제 1 도전막(115)이 상기 마스크막(119)을 사용하여 패터닝 된다. 그 결과로, 상기 제 1 오프닝(112) 상부에 도전막(118a), 비도전막(116a1), 그리고 도전막(115a)이 형성된다. 상기 도전막(118a), 비도전막(116a1), 그리고 도전막(115a)은 각각 커패시터(120)의 상부전극, 유전막(dielectric layer), 그리고 하부전극이 된다. 동시에, 상기 제 2 오프닝(113)의 상부 및 제 3 오프닝(114)의 상부에 각각 제 1 콘택 상호연결(first contact interconnect)(121) 및 제 2 콘택 상호연결(second contact interconnect)(122)이 형성된다.

Subsequently, as to figures 1c and 1d, the mask film (117) is removed. The second conductive film (118), for example, the metallic tungsten is formed in refractory metal oxide layer (116) (116a and 116b) front side. The dissimilar mask film (119) is formed in the second conductive film (118) front side. The second conductive film (118), and the refractory metal oxide layer (116) and the first conductive film (115) are patterned using the mask film (119). The conductive film (118a), and the non conductive film (116a1) and conductive film (115a) are formed with the result at the upper part of the first opening (112). The upper electrode of the capacitor (120), and the dielectric layer and bottom electrode become the conductive film (118a) , and the non conductive film (116a1) and conductive film (115a). Simultaneously, the first contact interconnect (first contact interconnect) (121) and the second contact interconnect (second contact interconnect) (122) are formed in the upper portion of the second opening (113) and upper portion of the third opening (114).

상기 제 1 콘택 상호연결(121)은 제 2 도전막(118b), 내열 금속 산화막(116b1), 그리고 제 1 도전막(115b)을 포함한다. 상기 제 2 콘택 상호연결(122)은 제 2 도전막(118c), 내열 금속 산화막(116b2), 그리고 제 1 도전막(115c)을 포함한다. 마지막으로, 마스크층(119)이 제거된다.

The first contact interconnect (121) comprises the second conductive film (118b), the refractory metal oxide layer (116b1), and the first conductive film (115b). The second contact interconnect (122) comprises the second conductive film (118c), the refractory metal oxide layer (116b2), and the first conductive film (115c). Finally, the mask layer (119) is removed.

도 1e에 있어서, 상기 제 2 도전막(118)(118a, 118b, 118c) 전면에 제 2 절연막(123)이 형성된다. 다음, 상기 커패시터의 상부전극(118a)이 노출되도록 상기 제 2 절연막(123) 내에 제 4 오프닝(124)이 형성된다. 그 동안, 상기 제 2 도전막(118) 예를 들어, 도전막 118b 또는 118c의 일부가 노출되도록 상기 제 2 절연막(123) 내에 제 5 오프닝(125)이 형성된다.

As to the drawing 1e, the second insulating layer (123) is formed in the second conductive film (118) (118a, 118b, 118c) front side. The fourth opening (124) is formed within the second insulating layer (123) so that the upper electrode (118a) of the next capacitor is exposed. The fifth opening (125) is formed within the second insulating layer (123) so that meantime, and the second conductive film (118), for example, the part of the conductive film 118b or 118c are exposed.

다음, 도 1f를 참조하면, 상기 제 4 및 제 5 오프닝(124, 125), 그리고 제 2 절연막(123) 전면에 제 3 도전막(126)이 형성된다. 상기 제 3 도전막(126)은 예를 들어, 알루미늄막(aluminum layer), 구리막(copper layer), 또는 알루미늄-구리

Then, referring to Figure 1f, the third conductive film (126) is formed in the fourth and fifth openings (124, 125) and the second insulating layer (123) front side. The third conductive film (126) may be for example, the a

GF Exhibit 1124 - 2244/2704

합금(aluminum-copper alloy)일 수 있다. 상기 제 3 도전막(126)이 패터닝 되어 레퍼런스 전압(reference voltage) 예를 들어, 1/2Vcc이 상기 제 4 오프닝(124)을 통해 커패시터의 상부전극(118a)에 공급되도록 하는 제 1 도전 라인(126a)이 형성된다. 유사하게, 상기 제 5 오프닝(125)을 통해 각각 적어도 하나의 도전 영역과 연결되는 제 2 도전 라인(126b 또는 126c)이 형성된다.

luminium film (aluminum layer), and the copper layer or the aluminum-copper alloy. The third conductive film (126) is patterned and the first conductive line (126a) in which the reference voltage, for example, 1/2Vcc is supplied to the upper electrode (118a) of the capacitor through the fourth opening (124) is formed. Similarly, the second conductive line (126b or 126c) connected to at least one conductive region through the fifth opening (125) is formed.

상술한 방법에 의해 제조된 상기 상부전극 및 콘택 상호연결의 상부 표면은 동일한 상대적 높이(relative height)를 갖는다. 따라서, 상기 메모리 회로 영역 및 로직 회로 영역이 또한 동일한 상대적 높이를 갖는다. 그 결과, 집적 회로에 대한 평탄도(degree of planarity)가 매우 증가된다.

It has the relative height in which the top surface of the contact interconnection and the upper electrode manufactured by the above-described method is identical. Therefore, it has the memory circuit domain and the relative height in which the logic circuit area is moreover identical. Consequently, the planarity (degree of planarity) about the integrated circuit is very increased.

더구나, 본 발명은 또한 큰 종횡비의 콘택홀 전면에 내열 금속 산화막을 증착 하여 임베디드 DRAM을 제조하는 방법을 제공한다. 수소 플라즈마 또는 핫 수소 처리를 통해 상기 콘택홀 상에 증착된 내열 금속 산화막의 일부가 비도전성에서 도전성 물질로 변화된다. 반면, 처리되지 않은 내열 금속 산화막의 부분은 비도전성으로 남게 된다. 따라서, 처리되지 않은 내열 금속 산화막은 DRAM 커패시터의 유전막으로 사용될 수 있다.

Moreover, the invention also provides the method for depositing the refractory metal oxide layer on the contact hole front side of the big aspect ratio and manufacturing the embedded DRAM. The part of the refractory metal oxide layer deposited through the hydro plasma or the hot hydrogen treatment on the contact hole is changed to the conductive material in the non-conductive. On the other hand, the part of the refractory metal oxide layer which is not processed remains as the non-conductive. Therefore, the refractory metal oxide layer which is not processed can be used as the dielectric layer of the DRAM capacitor.

도면에 대한 간단한 설명

도 1a 내지 도 1f는 본 발명의 실시예에 따른 임베디드 DRAM의 제조 방법의 단계들을 순차적으로 보여주는 단면도.

* 도면의 주요 부분에 대한 부호의 설명

100 : 반도체 기판 101 : 메모리 회로 영역

102 : 로직 회로 영역 103 : 트랜스퍼 FET
104 : 제 1 소오스/드레인 영역 105 : 제 2 소오스/드레인 영역
106 : 제 1 게이트 전극 107 : 로직 FET
108 : 제 3 소오스/드레인 영역 109 : 제 4 소오스/드레인 영역
110 : 제 2 게이트 전극 111 : 제 1 절연막
112 : 제 1 오프닝 113 : 제 2 오프닝
114 : 제 3 오프닝 115 : 제 1 도전막
116 : 내열 금속 산화막 117, 119 : 마스크막
118 : 제 2 도전막 120 : 커패시터
121 : 제 1 콘택 상호연결 122 : 제 2 콘택 상호연결

123 : 제 2 절연막 124 : 제 4 오프닝
125 : 제 5 오프닝 126 : 제 3 도전막
126a : 제 1 도전 라인 126b, 126c : 제 2 도전 라인

Brief explanation of the drawing

Figures 1a through 1f are the cross-sectional view which successively shows the steps of the manufacturing method of the embedded DRAM according to the embodiment of the invention.

* The description of reference numerals showing the main elements in drawings.

100: semiconductor substrate 101: memory circuit domain.
102: logic circuit area 103: transfer FET.
104: first source/drain region 105: second source/drain region.
106: first gate electrode 107: logic FET.
108: third source/drain region 109: fourth source/drain region.
110: second gate electrode 111: first insulating layer.
112: first opening 113: second opening.
114: third opening 115: first conductive film.
116: refractory metal oxide layer 117, 119: mask film.
118: second conductive film 120: capacitor.
121: first contact interconnect 122: second contact interconnect.
123: second insulating layer 124: fourth opening.
125: fifth opening 126: third conductive film.
126a: first conductive line 126b, 126c: second conductive line.

Disclaimer

본 문서는 특허 및 과학기술문헌 전용의 첨단 자동번역 시스템을 이용해 생성되었습니다. 따라서 부분적으로 오역의 가능성이 있으며, 본 문서를 자격을 갖춘 전문 번역가에 의한 번역물을 대신하는 것으로 이

GF Exhibit 1124 - 2245/2704

용되어서는 안 됩니다. 시스템 및 네트워크의 특성때문에 발생한 오역과 부분 누락, 데이터의 불일치등에 대하여 본원은 법적인 책임을 지지 않습니다. 본 문서는 당사의 사전 동의 없이 권한이 없는 일반 대중을 위해 DB 및 시스템에 저장되어 재생, 복사, 배포될 수 없음을 알려드립니다.
(The document produced by using the high-tech machine translation system for the patent and science & technology literature. Therefore, the document can include the mistranslation, and it should not be used as a translation by a professional translator. We hold no legal liability for inconsistency of mistranslation, partial omission, and data generated by feature of system and network. We would like to inform you that the document cannot be regenerated, copied, and distributed by being stored in DB and system for unauthorized general public without our consent.)

GF Exhibit 1124 - 2246/2704

SVERIGE

(19) SE

Översättning av europeisk patentskrift (T 3)

(87) Europeiskt publ nr 0875077 2004:02

(86) Europeiskt ansökningsnr 97901298.6

(51) Internationell klass 7

PATENTVERKET H01L 29/12 H01L 29/45

(86) Ingivningsdag för ansökan om europeiskt patent
1997-01-17

(45) Meddelandedatum för det europeiska patentet
2003-09-17

(60) Stamansökans nummer

(24) Löpdag
- -

(30) Prioritetsuppgifter
1996-01-19 SE 9600199

(54) Benämning
En halvledaranordning med en ohmsk kontakt med låg resistans mellan ett metallager och ett SiC-lager

(73) Patenthavare
ABB RESEARCH LTD. ,8050 Zürich CH

(72) Uppfinnare

C . HARRIS , S-191 72 Sollentuna SE

(84) Designerade stater
DE FR GB IT SE

GF Exhibit 1124 - 2247/2704

PRV Patent använder följande dokumentkoder för sina patentskrifter

kod	klartext
A	allmänt tillgänglig patentansökan
B	utläggningsskrift *
B5	rättad utläggningsskrift *
C	patentskrift *
C1	patentskrift *
C2	patentskrift
C3	rättad patentskrift
C5	rättad patentskrift *
C8	korrigerad förstasida till patentskrift
E	patentskrift i ändrad lydelse
E8	korrigerad förstasida till patentskrift i ändrad lydelse
E9	rättad patentskrift i ändrad lydelse

kod	klartext
L	allmänt tillgänglig
T1	översättning av kraven i europeisk patentansökan
T2	rättelse av översättning av kraven i europeisk patentansökan
T3	översättning av europeisk patentskrift
T4	översättning av europeisk patentskrift i ändrad avfattning
T5	rättad översättning av europeisk patentskrift
T8	rättad översättning av europeisk patentskrift
T9	korrigerad översättning av europeisk patentskrift

* publicerad under äldre lagstiftning

Nationskoder

AP	African Regional Industrial Property Organization (ARIPO)	CN	Kina	KI	Kiribati	RU	Ryska Federationen
		CO	Colombia	KM	Comorerna	RW	Ruanda
		CR	Costa Rica	KN	St Kitts	SA	Saudi-Arabien
EA	Euroasian Patent Office (EAPO)	CU	Kuba	KP	Dem. Folkrepubliken Korea	SB	Salomonöarna
		CV	Kap Verde	KR	Republiken Korea	SC	Seychellerna
EP	Europeiska Patentverket (EPO)	CY	Cypern	KW	Kuwait	SD	Sudan
		CZ	Tjeckiska republiken	KY	Cayman-öarna	SE	Sverige
OA	African Intellectual Property Organization (OAPI)	DE	Tyskland	KZ	Kazachstan	SG	Singapore
		DJ	Djibouti	LA	Laos	SH	St Helena
		DK	Danmark	LB	Libanon	SI	Slovenien
WO	World Intellectual Property Organization (WIPO)	DM	Dominica	LC	Saint Lucia	SK	Slovakien
		DO	Dominikanska republiken	LI	Liechtenstein	SL	Sierra Leone
		DZ	Algeriet	LK	Sri Lanka	SM	San Marino
IB	WIPO (i vissa fall)	EC	Ecuador	LR	Liberia	SN	Senegal
		EE	Estland	LS	Lesotho	SO	Somalia
AD	Andorra	EG	Egypten	LT	Litauen	SR	Surinam
AE	Förenade Arabemiraten	ES	Spanien	LU	Luxembourg	ST	São Thomé
AF	Afghanistan	ET	Etiopien	LV	Lettland	SV	El Salvador
AG	Antigua	FI	Finland	LY	Libyen	SY	Syrien
AI	Anguilla	FJ	Fiji-öarna	MA	Marocko	SZ	Swaziland
AL	Albanien	FK	Falklandsöarna	MC	Monaco	TD	Tchad
AM	Armenien	FR	Frankrike	MD	Moldavien	TG	Togo
AN	Nederländska Antillerna	GA	Gabon	MG	Madagaskar	TH	Thailand
AO	Angola	GB	Storbritannien	MK	Makedonien	TJ	Tadzjikistan
AR	Argentina	GD	Grenada	ML	Mali	TM	Turkmenistan
AT	Österrike	GE	Georgien	MM	Mayanmar	TN	Tunisien
AU	Australien	GH	Ghana	MN	Mongoliet	TO	Tonga
AZ	Azerbajdzjan	GI	Gibraltar	MR	Mauretanien	TR	Turkiet
BA	Bosnien och Hercegovina	GM	Gambia	MS	Monsterrat	TT	Trinidad och Tobago
		GN	Guinea	MT	Malta	TV	Tuvalu
BB	Barbados	GQ	Ekvatorial Guinea	MU	Mauritius	TW	Taiwan
BD	Bangladesh	GR	Grekland	MV	Maldiverna	TZ	Tanzania
BE	Belgien	GT	Guatemala	MW	Malawi	UA	Ukraina
BF	Burkina Faso	GW	Guinea-Bissau	MX	Mexiko	UG	Uganda
BG	Bulgarien	GY	Guyana	MY	Malaysia	US	Förenta Staterna (USA)
BH	Bahrain	HK	Hongkong	MZ	Mocambique	UY	Uruguay
BI	Burundi	HN	Honduras	NA	Namibia	UZ	Uzbekistan
BJ	Benin	HR	Kroatien	NG	Nigeria	VA	Vatikanstaten
BM	Bermuda	HT	Haiti	NI	Nicaragua	VC	St Vincent
BO	Bolivia	HU	Ungern	NL	Nederländerna	VE	Venezuela
BR	Brasilien	ID	Indonesien	NO	Norge	VG	Jungfruöarna
BS	Bahamaöarna	IE	Irland	NP	Nepal	VN	Viet Nam
BT	Bhutan	IL	Israel	NR	Nauru	VU	Vanuatu
BW	Botswana	IN	Indien	NZ	Nya Zeeland	WS	Samoa
BY	Vitryssland	IQ	Irak	OM	Oman	YD	Syd-Jemen
BZ	Belize	IR	Iran	PA	Panama	YE	Jemen
CA	Kanada	IS	Island	PE	Peru	YU	Yugoslavien
CF	Centralafrikanska Republiken	IT	Italien	PG	Papua Nya Guinea	ZA	Sydafrika
		JM	Jamaica	PH	Filippinerna	ZM	Zambia
CG	Kongo	JO	Jordanien	PK	Pakistan	ZR	Zaire
CH	Schweiz	JP	Japan	PL	Polen	ZW	Zimbabwe
CI	Elfenbenskusten	KE	Kenya	PT	Portugal		
CL	Chile	KG	Kirgistan	PY	Paraguay		
CM	Kamerun	KH	Kambodja	RO	Rumänien		

GF Exhibit 1124 - 2248/2704

HS/hj

Europapatentansökan nr: 97901298.6

Sökande: ABB Research Ltd.

EN HALVLEDARANORDNING MED EN OHMSK KONTAKT MED LÅG RESISTANS MELLAN ETT METALLAGER OCH ETT SiC-LAGER

Beskrivning

Uppfinningens tekniska område och känd teknik

Föreliggande uppfinning avser en halvledaranordning innefattande ett halvledarlager av SiC, ett metallager anordnat att bilda en ohmsk kontakt med låg resistans med SiC-lagret och ett tunt lager av en metall som har ett mindre bandgap än SiC hos SiC-lagret och placerat mellan SiC-lagret och metallagret, varvid nämnda SiC-lager är högt dopat åtminstone i området intill nämnda tunna lager.

Alla typer av halvledaranordningar i vilka en kontakt mellan ett metallager och ett SiC-lager ska bildas innefattar, såsom t ex olika typer av dioder, transistorer och tyristorer. P g a egenskaperna hos SiC är sådana anordningar oftast högeffektanordningar.

SiC är ett halvledarmaterial som har ett stort bandgap, vars storlek är mellan 2,3 och 3,3 eV beroende på polytypen ifråga, d v s avståndet mellan valensbandet och ledningsbandet. Av denna anledning har SiC, gemensamt med andra bredbandgapshalvledare, det problemet att det är mycket svårt att bilda ohmska kontakter med låg resistans på SiC. En anledning till denna svårighet är den stora skillnaden mellan övergångsarbetet hos metallen av ett sådant metallager och elektronaffiniteten hos

halvledaren, vilket resulterar i en stor Schottky-barriärhöjd. Man har försökt att lösa detta problem genom att åstadkomma en heteroövergångskontakt, varigenom ett material som har ett lägre bandgap växer som ett mellanliggande lager mellan metallagret och bredbandgapshalvledaren såsom definierad ovan och såsom beskriven i U.S. patent 3 984 261. Följaktligen borde definitionen "ett metallager anordnat att bilda en ohmsk kontakt med låg resistans med SiC-lagret" tolkas vittomfattande och det anger att en ohmsk kontakt med låg resistans ska bildas mellan ett metallager och ett SiC-lager, men detta kan göras genom att anbringa ett tunt lager av ett annat material däremellan.

Det europeiska patentet B1 0 249 777 beskriver hur en sådan heteroövergång används för att erhålla en ohmsk kontakt med låg resistans mellan ett halvledarmaterial och ett metallager, men halvledaren är inte SiC, utan ett III-V-material, t ex GaP, som har ett väsentligt lägre bandgap än SiC.

En känd halvledaranordning enligt den inledande delen har föreslagits (V.A. Dimitriev, K. Irvine, M. Spencer och G. Kelner Appl. Phys. Lett. Vol. 64(3) sid. 318 (1994) för 6H SiC, med användning av polytypen 3C SiC som ett mellanliggande lager, men nackdelen med detta är att polytypen 3C fortfarande är ett relativt bredbandgapsmaterial och kontaktproblemet är således inte löst.

Ett annat problem med olika material som hittills har använts som mellanliggande lager i sådan hetereoövergångar och också som halvledare, vilka halvledare gör en direktkontakt med ett metallager, är att Fermi-nivån hos dessa material är fastställd ("pinned") som ett resultat av en hög densitet av fällor inom halvledarens bandgap. Typiskt fastställande beror på djupa tillstånd (fällor) och Fermi-nivån uppehåller sig därför nära centrumet hos materialets bandgap. Dessa tillstånd är t ex bildade genom deponeringen av metallen. Fastställandet är endast avsett för ett snävt område, i detta fall gränssnittet mellan metallagret och halvledaren, så att Fermi-nivån inte är

"fastställd" i halvledarens bulk. Fastställandet definieras såsom fenomen där halvledarens Fermi-energi befinner sig i denna enda belägenhet, d v s vid nämnda gränssnitt, fixerad vid en enda energi (fällenergin) oberoende av dopningsförhållandet i halvledaren. Denna effekt kan typiskt ses mellan en metall och en halvledare, t ex III-V-föreningarna, såsom GaAs, och resulterar i en stor barriärhöjd. Det observeras inte vid hetereoövergången mellan halvledare förutsatt att gränssnittet är av god kvalitet, d v s av låg fälldensitet, och det skulle följaktligen inte vara närvarande mellan SiC-lagret och nämnda tunna lager i anordningen definierad i inledningen. Det är vanligtvis önskvärt att övergångsarbetet hos metallen ifråga är matchad med halvledarens elektronaffinitet för att åstadkomma en ohmsk kontakt med låg resistans, men p g a nämnda fastställande kommer mellangapstillstånden i halvledaren att bestämma höjden på Schottky-barriären oberoende av metallens övergångsarbete. Detta "fastställande"-fenomen finns även där i halvledaranordningen enligt det europeiska patentet B1 0 249 777, men detta fenomen är av mindre betydelse, eftersom bandgapet hos halvledarna som används där är mycket snäv.

Ett exempel på tidigare känd teknik är känt från US-A-4 985 742, vilket exempel beskriver ett Grupp 3B-nitridlager på SiC enligt ingressen hos krav 1. EP-A-0 458 352 beskriver ett Grupp 3B-nitridlager för ohmska kontakter på BN.

Sammanfattning av uppfinningen

Ändamålet med föreliggande uppfinning är att tillhandahålla en halvledaranordning enligt inledningen, vilken har en utmärkt ohmsk kontakt med låg resistans mellan SiC-lagret och metallagret.

Detta ändamål uppnås i enlighet med uppfinningen genom att åstadkomma nämnda tunna lager av en Grupp 3B-nitrid.

Det har således realiserats att Grupp 3B-nitrider inte har fastställda (fixerade) Fermi-nivåer vid gränssnittet med en metall, vilket innebär att metallens övergångsarbete kommer att bestämma Schottky-barriärhöjden, så att det kommer att vara möjligt att välja en lämplig metall för en låg barriär. Det är således möjligt att bilda en ohmsk kontakt med låg resistans mellan SiC-lagret och ett metallager genom att välja en Grupp 3B-nitrid som har ett mindre bandgap än SiC hos SiC-lagret som ett tunt lager mellan metallagret och SiC-lagret. Tack vare det faktum att SiC-lagret är högt dopat åtminstone i området intill nämnda tunna lager kan det tunna lagret vara odopat, eftersom det p g a "modulationsdoping" kommer att ske en överföring av laddning från SiC-lagret som har ett stort bandgap till det tunna lagret som har ett snävare bandgap, så att det snäva bandgapsmaterialet har ett överskott på laddning i ledningsbandet därav och kommer faktiskt att bete sig som en metall, så att en ohmsk kontakt med låg resistans kan etableras utan någon dopning i förväg av nämnda tunna lager. Detta betyder att det kommer att bli enklare att växa nämnda tunna lager av hög kvalitet. Vidare är det viktigt att anordningens heteroövergång har hög kvalitet för att undvika fällor där, d v s mellangapstillstånd, och detta erhålls tack vare den jämförelsevis goda gittermatchningen av Grupp 3B-nitriderna med SiC.

Enligt en föredragen utföringsform av uppfinningen innefattar nämnda Grupp 3B-nitrid en indiumhalt och åtminstone ett annat Grupp 3B-element. Indium är ett lämpligt element för att göra bandgapet hos Grupp 3B-nitriden snävare än den hos SiC av någon polytyp, så att det är mycket fördelaktigt att ha en sådan halt i nämnda Grupp 3B-nitrid. För att underlätta tillväxten av ett högkvalitativt tunt lager är det dock viktigt att det också innehåller åtminstone ett annat Grupp 3B-element förutom indium.

Enligt en annan föredragen utföringsform av uppfinningen har nämnda Grupp 3B-nitrid en halt av åtminstone indium och gallium. GaN har ett större bandgap än SiC, men det kan lätt växa på SiC och tack vare tillsatsen av indium görs bandgapet snä-

vare, så att nämnda Grupp 3B-nitrid kan vara lämplig för att bilda en ohmsk kontakt med låg resistans som eftersträvat.

Enligt en annan föredragen utföringsform av uppfinningen är nämnda Grupp 3B-nitrid $Ga_{1-x}In_xN$. Ett sådant material för nämnda tunna lager har funnits vara enkelt att växa på SiC, det har ett mindre bandgap än SiC och har en icke-fastställd Fermi-nivå vid gränssnittet med en metall.

Enligt en mycket föredragen utföringsform av uppfinningen justeras indiumhalten av Grupp 3B-nitriden till metallen vald för att matcha elektronaffiniteten hos nämnda material med metallens övergångsarbete hos nämnda metallager. Indiumhalten är således en parameter som är lätt att hantera för att justera elektron-affiniteten av Grupp 3B-nitriden för att matcha metallens övergångsarbete hos nämnda metallager för att minska barriärhöjden på nämnda ohmska kontakt mellan metallagret och nämnda tunna lager.

Enligt en ännu ytterligare, också mycket föredragen utföringsform av uppfinningen justeras indiumhalten av nämnda Grupp 3B-nitrid enligt dopningstyp, p eller n, hos nämnda SiC-lager. På detta sätt kommer indiumhalten att vara en parameter för att justera bandinriktningen beroende på om man vill ha en kontakt av p- eller n-typ. Det andra Grupp 3B-elementet hos nämnda Grupp 3B-nitrid kan nämligen ha ett gap mellan ledningsbandet och valensbandet vilket inte är centrerat med hänsyn till bandgapet av SiC hos nämnda SiC-lager, så att olika koncentrationer av indium i nämnda Grupp 3B-nitrid kan vara lämpliga beroende på dopningstypen hos SiC-lagret nära nämnda tunna lagers gränssnitt. Man tror t ex att GaN har ett bandgapscentrum som är förflyttat med hänsyn till bandgapscentrumet av SiC, vilket betyder att olika indium-halter kan behövas för p- och n-dopade SiC-lager.

Enligt en annan föredragen utföringsform av uppfinningen är nämnda tunna lager odopat. Fördelarna därmed har redan pre-

senterats ovan, och möjligheten att göra detta lager odopat tillhandahålls genom att en modulationsdopningsprocess äger rum tack vare den höga dopningen av SiC intill nämnda tunna lager, det mindre bandgapet hos det tunna lagret och det faktum att lagret verkligen är tunt.

Ytterligare fördelar och föredragna särdrag hos uppfinningen kommer att framgå av den följande beskrivningen och de andra beroende kraven.

Kort beskrivning av ritningarna

Med hänvisning till de bifogade ritningarna följer nedan en specifik beskrivning av en föredragen utföringsform av uppfinningen citerad som ett exempel.

I ritningarna:

Fig. 1 är en vy som illustrerar hur utsträckningen av ledningsbandet och valensbandet skulle vara i en halvledaranordning enligt uppfinningen från ett SiC-lager, ett tunt Grupp 3B-nitridlager och ett metallager vid en kontakt hos nämnda anordning om de olika lagren inte skulle ha någon påverkan på varandra, och

Fig. 2 är en vy motsvarande Fig. 1 men som illustrerar den riktiga utsträckningen av nämnda lednings- och valensband vid nämnda kontakt hos halvledaranordningen.

Detaljerad beskrivning av en föredragen utföringsform av uppfinningen

Fig.1 illustrerar en låg ohmsk kontakt med låg resistans mellan ett SiC-lager 1 och ett metallager 2 med ett mellanliggande tunt lager 3 av en Grupp 3B-nitrid i en halvledaranordning. SiC-lagret är ett monokristallinlager av SiC av någon polytyp. Grupp 3B-

nitriden är i det nuvarande fallet $Ga_{1-x}In_xN$, i vilken x väljs för att erhålla ett mindre bandgap av Grupp 3B-nitriden än SiC av SiC-lagret 1 och för att erhålla en elektronaffinitet av Grupp 3B-nitriden matchande övergångsarbetet hos metallen vald för nämnda metallager. Halvledaranordningen ifråga kan vara av vilken typ som helst, såsom en IGBT, en GTO och en likriktardiod.

På detta sätt bildas två övergångar, en första heteroövergång 4 mellan SiC-lagret 1 och nämnda tunna lager 3 och en annan övergång 5 mellan det tunna lagret och metallagret. SiC-lagret 1 är högt dopat med donatorer åtminstone nära hetereoövergången 4, men det skulle också vara möjligt att högdopa det med acceptorer. Högdopad betyder i detta sammanhang att koncentrationen av dopämnen överskrider 10^{17}, företrädesvis $10^{18}cm^{-3}$. Det är mycket schematiskt illustrerat att energigapet mellan valensbandet 6 och ledningsbandet 7 är större i SiC-lagret 1 än i nämnda tunna lager 3. På detta sätt erhålls en bandförskjutning vid nämnda heteroövergång 4. Eftersom SiC-lagret är högt dopat med donatorer har dessa sina extra elektroner 8 vid en högre energinivå än ledningsbandsnivån vid andra sidan av heteroövergången, vilket kommer att resultera i en nedgång av nämnda elektroner såsom indikerat av pilen till den lägre energinivån i nämnda tunna lager 3 medan nämnda donatorer joniseras och lämnar en positiv laddning 9 i SiC-lagret 1. Denna teknik som går ut på att tillhandahålla endast lagret med det största bandgapet med orenheter kallas för selektiv dopning eller modulationsdopning. På detta sätt skapas ett elektriskt fält vid heteroövergången, vilket fält böjer ledningsbanden på det sätt som visas i Fig. 2. Ju högre koncentrationen av donatorer i det första lagret förhållandevis nära heteroövergången desto skarpare kommer ledningsbandet att böjas. Tack vara den höga koncentrationen av dopämne i SiC-lagret kommer en mycket snäv barriär 9 på detta sätt etableras mellan SiC-lagret och nämnda tunna lager 3, så att elektroner kan tunnla lätt genom denna barriär och resistansen hos denna heteroövergång kommer att vara försumbar.

Det tunna lagret 3 kan vara odopat, eftersom ledningsbandet därav på detta sätt kommer att genom modulationsdopningsprocessen vara fylld med elektroner, så att detta tunna lager kommer att agera som en metall och ha en mycket låg resistans. Det skulle dock också vara möjligt att dopa det tunna lagret 3 med dopämnestypen motsvarande den hos SiC-lagret, såsom i fallet visat i figurerna med donatorer. Lagret 3 måste vara tunt för att erhålla detta metallbeteende därav, och tunn kommer att i denna utföringsform att betyda en tjocklek under 300Å och i några tillämpningar under 100Å. Det tunna lagret 3 är företrädesvis monokristallint, men det kan också vara polykristallint och fortfarande fungera beroende på korngränsens påverkan.

Fermi-nivåerna av de olika lagren måste, såsom känt, vara vid samma nivå, vilket kommer att resultera i en utsträckning av ledningsbandet och valensbandet i enlighet med Fig. 2. Man har funnit att Fermi-nivån hos en Grupp 3B-nitrid inte är fastställd, d v s fixerad, vid gränssnittet till en metall, vilket betyder att det finns relativt få mellangapstillstånd (fällor) vid nämnda gränssnitt, vilket skulle ändra positionen hos nämnda tunna lagers Fermi-nivå där, så att barriären 10 då skulle vara mycket högre. Följaktligen kan en ohmsk kontakt med låg resistans mellan ett SiC-lager och ett metallager uppnås genom att välja en Grupp 3B-nitrid som ett material för ett tunt lager mellan SiC-lagret och metallagret.

Såsom redan har nämnts ovan kan molbråkdelen av In innefattad i nämnda tunna lager 3 varieras för att ställa in bandförskjutningen med hänsyn till både SiC-lagret 1 och metallagret 2. Ju högre halt av In i Grupp 3B-nitriden desto mindre kommer bandgapet därav att vara. GaN har ett bandgap som är något större än de flesta polytyper av SiC och en indiumhalt däri kommer att minska detta bandgap. Bandgapet hos GaN är inte centrerat med avseende på bandgapet hos SiC, så att det kommer att vara lämpligt att välja olika koncentrationer av indium i nämnda Grupp 3B-nitrid enligt typen av dopning, p eller n, av

SiC-lagret. Indiumhalten kan således variera enligt vissa överväganden, och det kommer typiskt att vara mellan 5 och 20% av N-halten.

En kontakt av denna typ kan lätt framställas genom att bilda det högt dopade SiC-lagret 1 antingen genom epitaxiell tillväxt (CVD, MBE o s v) eller genom jonimplantation. Grupp 3B-nitridlagret 3 borde vara av högkvalitativ enkelkristall och borde återigen växas under användande av en epitaxiell teknik (CVD, MBE, magnetron förstoftning, o s v). Efter deponeringen av Grupp 3B-nitriden borde ett metallager 2 deponeras genom någon av de tillgängliga teknikerna, varvid nämnda metall är vald för att ge en bra kontakt med Grupp 3B-nitriden. Slutligen mönstras lagren under användande av litografi för att täcka endast de områden där en kontakt krävs. Glödgningstemperaturen borde vara låg, vilket betyder under 1000°C, men i de flesta fall kan den vara väsentligen lägre. Möjligheten att inte dopa nämnda tunna lager men att ändå erhålla en ohmsk kontakt med låg resistans förenklar framställningen av denna kontakt.

Uppfinningen är givetvis inte på något sätt begränsad till de föredragna utföringsformerna beskrivna ovan, utan flera möjligheter till modifikationer därav kommer att vara uppenbara för en fackman.

Alla definitioner avseende materialen hos de olika anordningslagren inkluderar givetvis ofrånkomliga orenheter såväl som avsiktliga dopning av lagren ifråga.

Definitionen lager är avsedd att tolkas vittomfattande och innefattar alla typer av volymutsträckningar och former.

Andra Grupp 3B-nitrider än GaInN är också tänkbara, såsom AlInN, i vilket fall In-halten måste vara jämförelsevis hög, eftersom AlN har ett mycket högre bandgap än SiC.

SiC-lagret kan vara av vilket polytyp av SiC som helst, såsom t ex 6H, 4H, 3C och 15R.

5

Patentkrav

1. En halvledaranordning innefattande ett halvledarlager (1) av SiC, ett metallager (2) anordnat att bilda en ohmsk kontakt med låg resistans med SiC-lagret och ett tunt lager (3) placerat mellan SiC-lagret och metallagret, varvid nämnda SiC-lager är högdopat åtminstone i området intill nämnda tunna lager, varvid materialet hos nämnda tunna lager är en Grupp 3B-nitrid, **kännetecknad** av att nämnda tunna lager är av ett material som har ett mindre bandgap än SiC hos SiC-lagret.

2. En anordning enligt krav 1, **kännetecknad** av att nämnda Grupp 3B-nitrid innefattar en indiumhalt och åtminstone ett annat Grupp 3B-element.

3. En anordning enligt krav 2, **kännetecknad** av att nämnda Grupp 3B-nitrid har en halt av åtminstone indium och gallium.

4. En anordning enligt krav 3, **kännetecknad** av att nämnda Grupp 3B-nitrid är $Ga_{1-x}In_xN$.

5. En anordning enligt något av kraven 2-4, **kännetecknad** av att indiumhalten av Grupp 3B-nitriden är justerad till metallen vald för att matcha elektronaffiniteten hos nämnda material med metallens övergångsarbete hos nämnda metallager.

6. En anordning enligt något av kraven 2-4, **kännetecknad** av att indiumhalten av nämnda Grupp 3B-nitrid är justerad enligt dopningstypen, p eller n, hos nämnda SiC-lager (1).

7. En anordning enligt något av kraven 1-6, **kännetecknad** av att nämnda tunna lager (3) är odopat.

8. En anordning enligt något av kraven 1-7, **kännetecknad** av att nämnda tunna lager (3) har en tjocklek under 300 Å.

9. En anordning enligt något av kraven 1-8, **kännetecknad** av att nämnda tunna lager (3) är ett monokristallint lager.

10. En anordning enligt något av kraven 1-9, **kännetecknad** av att högt dopat betyder en dopämneskoncentration överskridande $10^{18}cm^{-3}$.

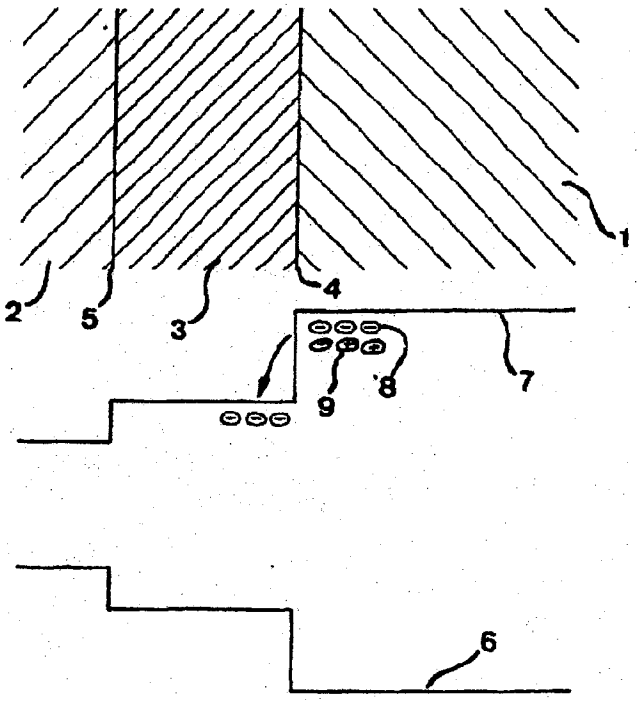


Fig 1

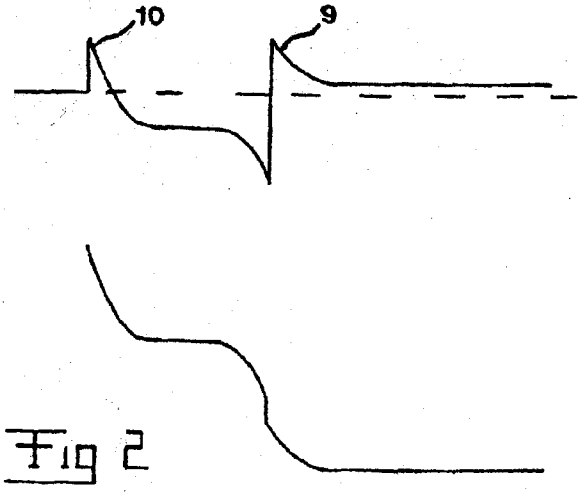


Fig 2

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Veröffentlichungsnummer:
(11) Publication number:
(11) Numéro de publication:

0 875 077

Internationale Anmeldung veröffentlicht durch die Weltorganisation für geistiges Eigentum unter der Nummer:

WO 97/26678 (art.158 des EPÜ).

International application published by the World Intellectual Property Organisation under number:

WO 97/26678 (art.158 of the EPC).

Demande internationale publiée par l'Organisation Mondiale de la Propriété sous le numéro:

WO 97/26678 (art.158 de la CBE).

GF Exhibit 1124 - 2262/2704

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H01L 29/45 // 21/28

A2

(11) International Publication Number: **WO 97/26678**

(43) International Publication Date: 24 July 1997 (24.07.97)

(21) International Application Number: PCT/SE97/00062

(22) International Filing Date: 17 January 1997 (17.01.97)

(30) Priority Data:
9600199-5 19 January 1996 (19.01.96) SE

(71) Applicant *(for all designated States except US)*: ABB RESEARCH LTD. [CH/CH]; P.O. Box 8131, CH-8050 Zürich (CH).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: HARRIS, Christopher [GB/SE]; Organistgränd 34, S-191 72 Sollentuna (SE).

(74) Agents: BJERKÉN, Håkan et al.; Bjerkéns Patentbyrå KB, P.O. Box 1274, S-801 37 Gävle (SE).

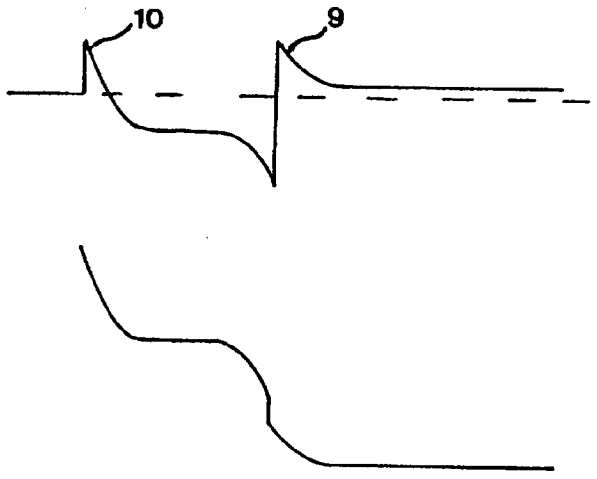
(81) Designated States: JP, US, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: A SEMICONDUCTOR DEVICE WITH A LOW RESISTANCE OHMIC CONTACT BETWEEN A METAL LAYER AND A SiC-LAYER

(57) Abstract

A semiconductor device comprises a semiconductor layer (1) of SiC, a metal layer (2) adapted to form a low resistance ohmic contact with the SiC-layer and a thin layer (3) of a material having a smaller bandgap than the SiC of the SiC-layer placed between the SiC-layer and the metal layer. The SiC-layer is at least in the region next to said thin layer highly doped. The material of said thin layer is a Group 3B-nitride.



GF Exhibit 1124 - 2263/2704

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AM	Armenia	**GB**	United Kingdom	**MW**	Malawi
AT	Austria	**GE**	Georgia	**MX**	Mexico
AU	Australia	**GN**	Guinea	**NE**	Niger
BB	Barbados	**GR**	Greece	**NL**	Netherlands
BE	Belgium	**HU**	Hungary	**NO**	Norway
BF	Burkina Faso	**IE**	Ireland	**NZ**	New Zealand
BG	Bulgaria	**IT**	Italy	**PL**	Poland
BJ	Benin	**JP**	Japan	**PT**	Portugal
BR	Brazil	**KE**	Kenya	**RO**	Romania
BY	Belarus	**KG**	Kyrgystan	**RU**	Russian Federation
CA	Canada	**KP**	Democratic People's Republic of Korea	**SD**	Sudan
CF	Central African Republic			**SE**	Sweden
CG	Congo	**KR**	Republic of Korea	**SG**	Singapore
CH	Switzerland	**KZ**	Kazakhstan	**SI**	Slovenia
CI	Côte d'Ivoire	**LI**	Liechtenstein	**SK**	Slovakia
CM	Cameroon	**LK**	Sri Lanka	**SN**	Senegal
CN	China	**LR**	Liberia	**SZ**	Swaziland
CS	Czechoslovakia	**LT**	Lithuania	**TD**	Chad
CZ	Czech Republic	**LU**	Luxembourg	**TG**	Togo
DE	Germany	**LV**	Latvia	**TJ**	Tajikistan
DK	Denmark	**MC**	Monaco	**TT**	Trinidad and Tobago
EE	Estonia	**MD**	Republic of Moldova	**UA**	Ukraine
ES	Spain	**MG**	Madagascar	**UG**	Uganda
FI	Finland	**ML**	Mali	**US**	United States of America
FR	France	**MN**	Mongolia	**UZ**	Uzbekistan
GA	Gabon	**MR**	Mauritania	**VN**	Viet Nam

GF Exhibit 1124 - 2264/2704

A semiconductor device with a low resistance ohmic contact between a metal layer and a SiC-layer

Technical field of the invention and prior art

The present invention relates to a semiconductor device comprising a semiconductor layer of SiC, a metal layer adapted to form a low resistance ohmic contact with the SiC-layer and a thin layer of a material having a smaller band gap than the SiC of the SiC-layer and placed between the SiC-layer and the metal layer, said SiC-layer being at least in the region next to said thin layer highly doped.

All types of semiconductor devices in which a contact between a metal layer and a SiC-layer is to be formed are comprised, such as for example different types of diodes, transistors and thyristors. Due to the characteristics of SiC such devices are often high power devices.

SiC is a semiconductor material having a large band gap, the magnitude of which is between 2,3 and 3,3 eV dependent on the polytype in question, i.e. the gap between the valence band and the conduction band. For this reason SiC has, in common with other wide band gap semiconductors, the problem that it is extremely difficult to form low resistance ohmic contacts on SiC. One reason for this difficulty is the large difference between the work function of the metal of such a metal layer and the electron affinity of the semiconductor, which results in a large Schottky-barrier height. It has been tried to solve this problem by making a heterojunction

GF Exhibit 1124 - 2265/2704

contact, whereby a material having a lower band gap is grown as an intermediate layer between the metal layer and the wide band gap semiconductor as defined above and as described in U.S. patent 3 984 261. Accordingly, the definition "a metal layer adapted to form a low resistance ohmic contact with the SiC-layer" is to be interpreted broadly and it expresses that there shall be formed a low resistance ohmic contact between a metal layer and a SiC-layer, but this may be done by interposing a thin layer of another material.

The European patent B1 0 249 777 describes how such a heterojunction is used for obtaining a low resistance ohmic contact between a semiconductor material and a metal layer, but the semiconductor is not SiC, but a III-V-material, for instance GaP, which has a considerably lower band gap than SiC.

A known semiconductor device according to the introduction has been suggested (V.A. Dimitriev, K. Irvine, M. Spencer and G. Kelner Appl. Phys. Lett. vol. 64(3) p. 318 (1994)) for 6H SiC, while using the polytype 3C SiC as an intermediate layer, but the disadvantage of this is that the polytype 3C is still a relatively wide band gap material and the contact problem is thus not solved.

Another problem of different materials used so far as intermediate layers in such heterojunctions and also as semiconductors making a direct contact with a metal layer is that the Fermi-level of these materials is pinned as a result of a high density of traps within the band gap of the semiconductor. Typically pinning is due to deep states (traps) and therefore the Fermi-level resides close to the centre of the band gap of the material. These states are for example formed by the deposition of the metal. The pinning is for a narrow region only, in this case the interface between the metal layer and the semiconductor, so that the Fermi-level

GF Exhibit 1124 - 2266/2704

is not "pinned" in the bulk of the semiconductor. Pinning is defined as the phenomena such that the Fermi-energy of the semiconductor is in this single location, i.e. at said interface, fixed at a single energy (the trap energy) independent of the doping condition in the semiconductor. This effect is typically seen between a metal and a semiconductor, for example the III-V compounds, such as GaAs, and results in a large barrier height. It is not observed at the heterojunction between semiconductors provided the interface is of good quality, i.e. of low trap density, and it would accordingly not be present between the SiC-layer and said thin layer in the device defined in the introduction. Normally, it is desired that the work function of the metal in question is matched with the electron affinity of the semiconductor for making a low resistance ohmic contact, but due to said pinning the midgap states in the semiconductor will determine the height of the Schottky-barrier independent of the work function of the metal. This "pinning" phenomena is also there in the semiconductor device according to the European patent B1 0 249 777, but this phenomena is of minor importance, since the band gap of the semiconductors used there is very narrow.

Summary of the invention

The object of the present invention is to provide a semiconductor device according to the introduction, which has an excellent low resistance ohmic contact between the SiC-layer and the metal layer.

This object is in accordance with the invention obtained by making said thin layer of a Group 3B-nitride.

Thus, it has been realised that Group 3B-nitrides do not have pinned (fixed) Fermi-levels at the interface with a metal, which means that the work function of the metal will

GF Exhibit 1124 - 2267/2704

determine the Schottky-barrier height, so that it will be possible to choose a suitable metal for a low barrier. Thus, it is possible to form a low resistance ohmic contact between the SiC-layer and a metal layer by choosing a Group 3B-nitride having a smaller bandgap than the SiC of the SiC-layer as a thin layer between the metal layer and the SiC layer. Thanks to the fact that the SiC-layer is highly doped at least in the region next to said thin layer the thin layer may be undoped, since there will due to "modulation doping" be a transfer of charge from the SiC layer having a large band gap to the thin layer having a narrower band gap, so that the narrow band gap material has an excess of charge in the conduction band thereof and will in fact behave as a metal, so that a low resistance ohmic contact may be established without any doping in advance of said thin layer. This means that it will be easier to grow said thin layer of a high quality. Furthermore, it is important that the heterojunction of the device has a high quality so as to avoid traps, i.e. mid gap states, there, and this is obtained thanks to the comparatively good lattice match of the Group 3B-nitrides with SiC.

According to a preferred embodiment of the invention said Group 3B-nitride comprises a content of indium and at least another Group 3B-element. Indium is a suitable element for making the band gap of the Group 3B-nitride narrower than that of SiC of any polytype, so that it is very advantageous to have such content in said Group 3B-nitride. However, it is for the ease of the growth of a high quality thin layer of importance that it also contains at least another Group 3B-element besides indium.

According to another preferred embodiment of the invention said Group 3B-nitride has a content of at least indium and gallium. GaN has a larger band gap than SiC, but it may be easily grown on SiC and thanks to the addition of indium the

band gap is made narrower, so that said Group 3B-nitride may be suited for forming a low resistance ohmic contact aimed at.

According to another preferred embodiment of the invention said Group 3B-nitride is $Ga_{1-x}In_xN$. Such a material for said thin layer has been found to be easy to grow on SiC, have a smaller band gap than SiC and have a not pinned Fermi-level at the interface with a metal.

According to a very preferred embodiment of the invention the indium content of the Group 3B-nitride is adjusted to the metal chosen for matching the electron affinity of said material with the work function of the metal of said metal layer. Thus, the indium content is a parameter easy to handle to adjust the electron affinity of the Group 3B-nitride for matching the work function of the metal of said metal layer for reducing the barrier height of said ohmic contact between the metal layer and said thin layer.

According to a still further, also very preferred embodiment of the invention the indium content of said Group 3B-nitride is adjusted according to the type of doping, p or n, of said SiC-layer. In this way the indium content will be a parameter to adjust the band-alingement according to whether you want a p- or n-type contact. The other Group 3B-element of said Group 3B-nitride may namely have a gap between the conduction band and the valence band which is not centered with respect to the band gap of the SiC of said SiC-layer, so that different concentrations of indium in said Group 3B-nitride may be appropriate depending on the type of doping of the SiC-layer close to the interface to said thin layer. For instance, it is believed that GaN has a band gap centre being displaced with respect to the band gap centre of SiC, which means that different indium-contents may be needed for p- and n-doped SiC-layers.

According to another preferred embodiment of the invention said thin layer is undoped. The advantages thereof has already been presented above, and the possibility to make this layer undoped is provided by the fact that a modulation doping process takes place thanks to the high doping of the SiC next to said thin layer, the smaller band gap of the thin layer and the fact that the layer really is thin.

Further advantages and preferred features of the invention will appear from the following description and the other dependent claims.

Brief description of the drawings

With reference to the appended drawings, below follows a specific description of a preferred embodiment of the invention cited as an example.

In the drawings:

Fig. 1 is a view illustrating how the extension of the conduction band and the valence band would be in a semiconductor device of the invention from a SiC-layer, a thin Group 3B-nitride layer and a metal layer at a contact of said device if the different layers would not have any influence on each other, and

Fig. 2 is a view corresponding to Fig. 1 but illustrating the real extension of said conduction and valence bands at said contact of the semiconductor device.

GF Exhibit 1124 - 2270/2704

Detailed description of a preferred embodiment of the invention

Fig. 1 illustrates a low resistance ohmic contact between a SiC-layer 1 and a metal layer 2 with an intermediate thin layer 3 of a Group 3B-nitride in a semiconductor device. The SiC-layer is a mono-crystalline layer of SiC of any polytype. The Group 3B-nitride is in the present case $Ga_{1-x}In_xN$, in which x is chosen to obtain a smaller bandgap of the Group 3B-nitride than the SiC of the SiC-layer 1 and for obtaining an electron affinity of the Group 3B-nitride matching the work function of the metal selected for said metal layer. The semiconductor device in question may be of any type, such as an IGBT, a GTO and a rectifying diode.

In this way two junctions are formed, a first heterojunction 4 between the SiC-layer 1 and said thin layer 3 and a second junction 5 between the thin layer and the metal layer. The SiC-layer 1 is highly doped with donors at least close to the heterojunction 4, but it would also be possible to highly dope it with acceptors. Highly doped does here mean that the concentration of dopants exceeds 10^{17}, preferably exceeding 10^{18} cm^{-3}. It is very schematically illustrated that the energy gap between the valence band 6 and the conduction band 7 is larger in the SiC layer 1 than in said thin layer 3. In this way a band-offset is obtained at said heterojunction 4. Since the SiC-layer is highly doped with donors these have their extra electrons 8 at a higher energy level than the conduction band level at the other side of the heterojunction, which will result in a fall of said electrons as indicated by the arrow to the lower energy level in said thin layer 3 while ionising said donors and leaving a positive charge 9 in the SiC-layer 1. This technique of providing only the layer with the largest band gap with impurities is called selective doping or modulation doping. In this way an electrical field is created at the

GF Exhibit 1124 - 2271/2704

heterojunction bending the conduction bands in the way shown in Fig. 2. The higher the concentration of donors in the first layer comparatively close to the heterojunction the sharper will the conduction band be bent. Thanks to the high concentration of dopants in the SiC-layer a very narrow barrier 9 will in this way be established between the SiC-layer and said thin layer 3, so that electrons may easily tunnel through this barrier and the resistance of this heterojunction will be neglectable.

The thin layer 3 may be undoped, since the conduction band thereof will in this way by the modulation doping process be filled with electrons, so that this thin layer will act as a metal and have a very low resistance. It would however also be possible to dope the thin layer 3 with the dopant type corresponding to that of the SiC-layer, thus in the case shown in the figures with donors. The layer 3 has to be thin for obtaining this metal behaviour thereof, and thin will in this embodiment mean a thickness below 300Å and in some applications below 100Å. The thin layer 3 is preferably monocrystalline, but it may also be poly-crystalline and still work depending on the influence of the grain boundary.

The Fermi-levels of the different layers have, as known, to be at the same level, which will result in an extension of the conduction band and the valence band in accordance with Fig. 2. It has been found that the Fermi-level of a Group 3B-nitride is not pinned, i.e. fixed, at the interface to a metal, which means that there are relatively few mid gap states (traps) at said interface, which would change the position of the Fermi-level of said thin layer there, so that the barrier 10 then would be much higher. Accordingly, a low resistance ohmic contact between a SiC-layer and a metal layer may be achieved by selecting a Group 3B-nitride as a material for a thin layer between the SiC-layer and the metal layer.

GF Exhibit 1124 - 2272/2704

As already mentioned above the mole fraction of In incorporated in said thin layer 3 can be varied to tune the band offset with respect to both the SiC-layer 1 and the metal layer 2. The higher the content of In in the Group 3B-nitride the smaller will the band gap thereof be. GaN has a band gap being slightly larger than most polytypes of SiC and a content of indium therein will reduce this band gap. The band gap of GaN is not centered with respect to the band gap of SiC, so that it will be suitable to choose different concentrations of indium in said Group 3B-nitride according to the type of doping, p or n, of the SiC-layer. Thus, the indium content may vary according to certain considerations, and it will typically be between 5 and 20% of the N content.

A contact of this type may be easily produced by forming the highly doped SiC-layer 1 either by epitaxial growth (CVD, MBE etc.) or by ion implantation. The Group 3B-nitride layer 3 should be of high quality single crystal and should again be grown using an epitaxial technique (CVD, MBE, magnetron sputtering, etc.). Following the deposition of the Group 3B-nitride a metal layer 2 should be deposited by any of the available techniques, said metal being chosen to give a good contact to the Group 3B-nitride. Finally, the layers are patterned using lithography to cover only those areas where a contact is required. The annealing temperature should be low, which means below 1000°C, but in most cases it may be considerably lower. The possibility to not dope said thin layer but nevertheless obtain a low resistance ohmic contact simplifies the production of this contact.

The invention is of course not in any way restricted to the preferred embodiments described above, but many possibilities to modifications thereof will be apparent to a man with ordinary skill in the art.

GF Exhibit 1124 - 2273/2704

All definitions concerning the materials of the different device layers do of course include inevitable impurities as well as intentional doping of the layers in question.

The definition layer is to be interpreted broadly and comprises all types of volume extensions and shapes.

Other Group 3B-nitrides than GaInN are also conceivable, such as AlInN, in which case the In-content has to be comparatively high, since AlN has a much higher bandgap than SiC.

The SiC-layer may be of any polytype of SiC, such as for example 6H, 4H, 3C and 15R.

GF Exhibit 1124 - 2274/2704

Claims

1. A semiconductor device comprising a semiconductor layer (1) of SiC, a metal layer (2) adapted to form a low resistance ohmic contact with the SiC-layer and a thin layer (3) of a material having a smaller bandgap than the SiC of the SiC-layer and placed between the SiC-layer and the metal layer, said SiC-layer being at least in the region next to said thin layer highly doped, **characterized** in that the material of said thin layer is a Group 3B-nitride.

2. A device according to claim 1, **characterized** in that said Group 3B-nitride comprises a content of indium and at least another Group 3B-element.

3. A device according to claim 2, **characterized** in that said Group 3B-nitride has a content of at least indium and gallium.

4. A device according to claim 3, **characterized** in that said Group 3B-nitride is $Ga_{1-x}In_xN$.

5. A device according to any of claims 2-4, **characterized** in that the indium content of the Group 3B-nitride is adjusted to the metal chosen for matching the electron affinity of said material with the work function of the metal of said metal layer.

6. A device according to any of claims 2-4, **characterized** in that the indium content of said Group 3B-nitride is adjusted according to the type of doping, p or n, of said SiC-layer (1).

7. A device according to any of claims 1-6, **characterized** in that said thin layer (3) is undoped.

GF Exhibit 1124 - 2275/2704

8. A device according to any of claims 1-7, **characterized** in that said thin layer (3) has a thickness below 300 Å.

9. A device according to any of claims 1-8, **characterized** in that said thin layer (3) is a mono-crystalline layer.

10. A device according to any of claims 1-9, **characterized** in that highly doped means a concentration of dopants exceeding 10^{18} cm^{-3}.

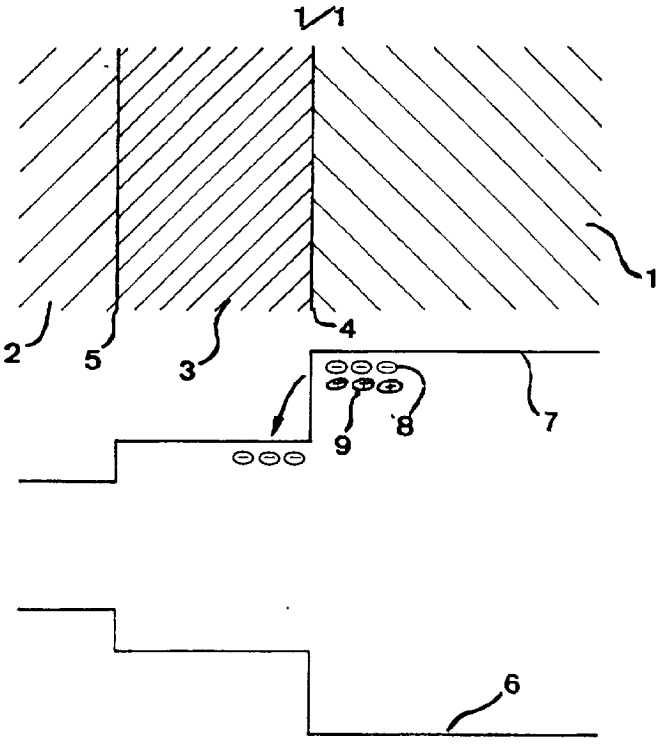


Fig 1

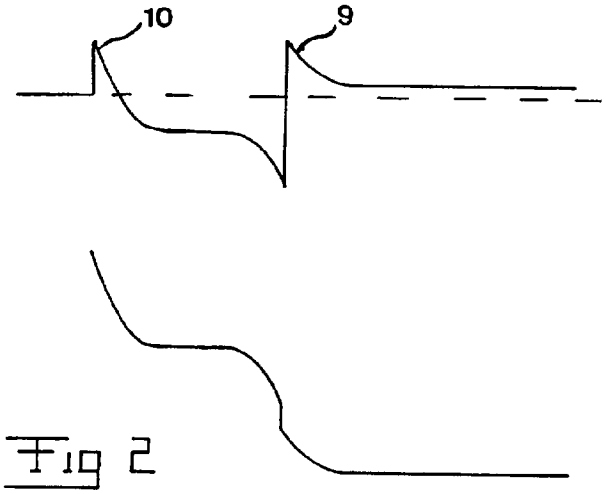


Fig 2

GF Exhibit 1124 - 2277/2704

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
26 April 2001 (26.04.2001)

PCT

(10) International Publication Number
WO 01/28677 A1

(51) International Patent Classification[7]: B01J 19/08

(21) International Application Number: PCT/US00/28801

(22) International Filing Date: 18 October 2000 (18.10.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

60/160,531	20 October 1999 (20.10.1999)	US
60/177,919	25 January 2000 (25.01.2000)	US
60/186,567	2 March 2000 (02.03.2000)	US
09/631,463	3 August 2000 (03.08.2000)	US

(71) Applicant: **NEOKISMET L.L.C.** [US/US]; Suite 1350, 456 Montgomery Street, San Francisco, CA 94104 (US).

(72) Inventors: **ZUPPERO, Anthony, C.**; 2631 Buena Terra, Pollock Pines, CA 95726-9456 (US). **GIDWANI, Jawahar, M.**; 2335 Leavenworth, San Francisco, CA 94133 (US).

(74) Agents: **JACOBS, James, D.** et al.; Baker & McKenzie, 805 Third Avenue, New York, NY 10022 (US).

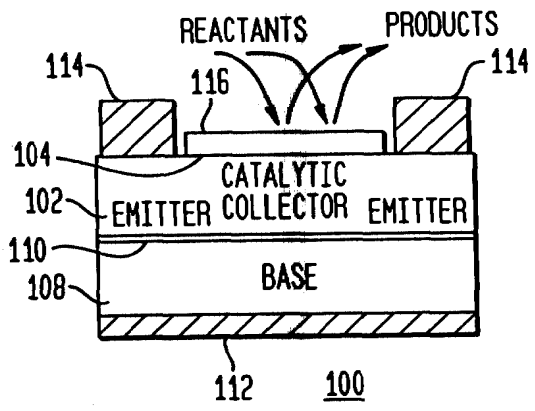
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *With international search report.*
— *With amended claims.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SOLID STATE SURFACE CATALYSIS REACTOR



(57) Abstract: A method and apparatus to stimulate chemical reactions on a catalyst surface (116) using electricity, and the reverse process to convert energy released from chemical reactions into electricity. A reversible emitter (102) generates electrons which are injected into reactants on the catalyst surface (116), exciting chemically reactive vibrational resonances. Hot electrons created in the emitter region of a semiconductor junction (110) diffuse to the co-located collector region and catalyst surface (116). Catalyst clusters or films bonded on the collector surface transfer the hot electrons to or from the catalyst surface (116) having adsorbed reactants. The dimension of the catalyst-collector (104) is less than the energy mean free path of hot electrons. The hot electrons excite reactant vibrations before thermalizing with the substrate lattice thereby accelerating reactions. The hot electrons are also generated by the same reactions on a catalyst surface. The method and apparatus is reversible and may be operated as an electric generator using chemical reactions.

WO 01/28677 A1

GF Exhibit 1124 - 2278/2704

SOLID STATE SURFACE CATALYSIS REACTOR

TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to an energy generator and more specifically to a method and apparatus to couple the excitation structure of a semiconductor substrate to the excitation structure of reactive adsorbates on the surface of a catalyst.

BACKGROUND OF THE INVENTION

Recent experimental and theoretical developments in surface science showed how hot electrons cause heating of the vibration of molecules or atoms adsorbed on a catalyst surface. The energy of hot electrons is defined as electrons with effective temperatures between 600 Kelvin and 60,000 Kelvin, which means equivalent energies between 0.05 and approximately 5 eV, or many times that of thermal energy at room temperature. 300 degrees Kelvin is 0.026 eV.

It has been discovered that hot electrons that diffuse to a catalyst metal surface interact strongly with the adsorbed surface chemicals, also called adsorbates, and can do so at a rate faster than the process of electrons thermalizing with the lattice of catalyst metal atoms. It has also been recently discovered that the adsorbates acquire vibrational energy when interacting with hot electrons from the catalyst surface. It has been further discovered that adsorbate vibrational energy strongly enhances the rate of chemical reactions, and in some cases enable reactions that do not occur by thermal means because of the activation energies or chemical thermodynamics involved. Hot electrons stimulate adsorbate chemical reactions on a catalyst surface. The reverse of this process has also been observed, where a surface chemical reaction resulted in the production of hot electrons.

GF Exhibit 1124 - 2279/2704

The presence of hot electrons on the surface of the catalyst can cause a pseudo-thermal regime in which the surface vibrations of adsorbate molecules, either against themselves or against the catalyst, are in equilibrium with the temperature of the substrate hot electrons rather than with the physical temperature of the substrate itself. This means the vibrations can be at several thousand degrees while the catalyst is at ambient temperature. Hot electrons excite the adsorbate from the bottom of its adsorption well in a stepwise manner, and may even do so until it overcomes the adsorption barrier and hops to a neighboring potential well, reacts or desorbs.

The hot electron energy or frequency need not exactly match that of the adsorbates. The adsorbate excitation structure is generally very broad, being spread over many frequencies, and the mechanism is often via an electronic excited state. That is, when the adsorbate acquires an electron it transitions to an excited electronic state. Within a few tens of femtoseconds it begins to move outward away from the surface, and then releases the electron. The adsorbate now transitions back to a non-electronic excited state. However, it retains the extra energy given to it by the hot electron. As a result, the adsorbate is in a higher vibration state. The tens of femtosecond lifetime for the process causes a broadband resonance feature and hence permits an energy mismatch between hot electron and the receiving adsorbate energy levels. The substrate electron in effect deposits energy into a vibration mode of adsorbate reactant, such as the vibration of the atoms in the adsorbate reactant molecule or in the vibration of the adsorbate against the catalyst surface. This process can repeat itself many times, to the point where the adsorbate desorbs. In the literature this is called "Desorption Induced by (Multiple) Electronic Transitions," Abbreviated DIMET or DIET. This is the stimulator process.

GF Exhibit 1124 - 2280/2704

The generator process works in reverse. An adsorbate with energy in one of its vibration modes attracts and acquires a cold electron from the catalyst. This causes a transition where the adsorbate with attached electron then becomes a charged adsorbate specie in an excited electron state. Within femtoseconds this specie in the excited electron state decays and ejects an electron. This leaves the adsorbate reactant with less energy in its vibration mode and the electron with excess kinetic energy. The effect is that the energetically excited reactant on the surface of the catalyst gave a fraction of its energy to an electron in the catalyst. This is the generator process.

This generator or reverse process has been observed in laboratories. The detector in this observation used a short circuit Schottky diode to measure an electron flux directly generated by the surface reactions. The laboratory detector measured a current in a short circuit diode, which means the detector generated almost exactly zero power. However, the detector confirmed the existence of the generator mode. Both hot electrons and hot holes were observed, and with energies in excess of the Schottky barrier in silicon, which is of order 0.5 eV.

Hot electrons on a catalyst surface have been shown to accelerate reactions. Experiments with vibrationally excited Nitrogen Oxide (NO) molecules interacting with a copper (Cu) surface showed thousand-fold enhancement of surface reactivity. Up to near unit reaction probability was observed. In that work, neither reactant translational energy nor surface temperature had a strong effect on the reaction probability, confirming the efficacy of using hot electrons.

In another experiment, carbon monoxide (CO) was oxidized on a ruthenium surface. A 1.5 eV, 110 femtosecond laser pulse duration created the hot electrons. It was observed that sub-picosecond

GF Exhibit 1124 - 2281/2704

reactions of adsorbed O with CO to produce CO2 in a reaction that is energetically not possible at all without the hot electrons. This means if one uses thermal energy alone, CO will desorb without reacting.

The efficiency of such hot electrons to impart vibrational energy to just the adsorbates can approach 100%. Nearly 100% desorption of CO from a copper surface was observed. A three order of magnitude increase in reaction rate of NO with Cu was also observed.

This establishes the strong, two way energy transfer between hot electrons and excited adsorbate specie on a metal catalyst surface. The collection of observations leads to both an apparatus and method to couple the excitation structures of the adsorbate reactants adsorbed, chemisorbed or physisorbed on a catalyst surface to the excitation structure of a semiconductor diode in close proximity to the adsorbates.

The semiconductor diode excitation structure is rather simple, consisting of holes in the valence band and electrons in the conduction band. The excitation structure of the chemically reactive adsorbate-catalyst system is dominated by vibrations of the atoms and molecules with themselves and against the substrate, forming energy level bands, and the energy level bands due to electronic excited states of these specie, where the adsorbates may acquire a transient or permanent charge.

Coupling of these structures occurs mainly by two paths, either directly through the direct, typically ballistic transport of the hot carriers such as hot electrons or hot holes, between adsorbate and semiconductor, or by resonant tunneling of energy. Resonant tunneling couples the two structures through oscillating electric fields produced by the excitation structures in the semiconductor and adsorbate-catalyst system. The coupling is greatly enhanced when the

GF Exhibit 1124 - 2282/2704

frequencies of the excitations on either side are close to each other.

Hot electrons are the easiest excitation to work with. The current method of choice to produce and inject the hot electrons into a metal catalyst surface relies on a pulsed laser. The usual method to produce these hot electrons is to irradiate the surface of the metal with a short laser pulse, typically with pulse duration in the range of 50 to 1000 femtoseconds and with photon energies of 1 eV or greater (0.2 to 1.5 micron wavelength). The photons are adsorbed and produce electrons with energies between 0 eV and up to the photon energy, splitting the energy with a hot hole, and with hot electron energies averaging approximately half the incident photon energy. A laser, however, is one of the most expensive energy sources available.

A theory to use a solid state metal-insulator-metal junctions to produce resonantly coupled, hot electrons has been proposed. The theoretical suggestion would produce resonance-assisted, hot-electron-induced femtochemical processing at surfaces. The energies relative to the catalyst Fermi level and associated with the metal-insulator junctions is higher than what is now known to be appropriate for surface resonances. No experiments using this theory are known at this time. No known mention of process reversibility has been claimed.

The use of a neutral semiconductor substrate as the injection mechanism into thin metal overlayers, with photons derived from a pulsed laser as the creator of hot carriers in the semiconductor, was also suggested in the literature. It was suggested that this could be an order of magnitude more efficient for stimulating gas-surface catalytic reactions than using the metal as the photon acceptor. It was suggested that using a semiconductor substrate, metal overlayer and catalyst device to produce hot electrons more efficiently with photons and inject them into a catalyst surface. A

GF Exhibit 1124 - 2283/2704

critical detail needed to render the process efficiency useful was not addressed in a way needed to assure process efficiency. One must tailor the Schottky junction, the ohmic junction or the almost ohmic junction between the semiconductor and the metal so that the coupling of either hot carriers such as hot electrons or holes is electrically efficient, or so that the resonant tunneling is efficient. The proper use of resonant tunneling and resonance-assisted processes can be valuable components in a useful device and method.

A Schottky junction diode has been used in experiments for hot electron injection into solutions. One of the co-authors of that work suggests that they did not achieve the success they wanted because the surface states associated with the electrolyte cooled the electrons. A catalyst electrode Schottky junction made of n-silicon and platinum metal was used to inject electrons into a reactive electrolyte solution. The platinum thickness was varied from less than the mean free path to several times thicker than the mean free path of hot electrons in platinum. They achieved some success, and also suffered severe problems with interactions between hot electrons and electrolyte. Flooding the surface with liquid electrolyte destroys the effectiveness of hot electrons. Metal-oxide junction surface states have been an unsolved problem with this approach, where liquids flood the reactive surface.

It is now known that outer layers, away from the catalyst surface, of multiple layers of adsorbates that accumulate on the metal-liquid interface trap hot electrons as "polaritons" and render them less useful as a source of prompt reaction stimulators or as generators of excitations. The efficacy of a semiconductor substrate under a metal and catalyst reactive surface is a valuable element. A semiconductor diode is a critical element.

Implicit in all the observations is the efficiency of pulsed operation. In the case of a reaction

GF Exhibit 1124 - 2284/2704

stimulator, the duration of the pulses generating hot electrons is less than the time associated with electron thermalization with the lattice. In the case of a generator, the sudden burst of chemical reactions causes a flood of hot electrons on the catalyst surface. This in turn causes a flood of electrons in the conduction band of the semiconductor substrate collecting those hot electrons. A sufficiently short burst causes the number of generated electrons to exceed the thermally occurring short circuit electrons, thereby increasing the efficiency of the generation of electricity.

Missing in the public domain are methods to tailor the surface of the catalyst to enhance resonant tunneling, to enhance the activation of selected energy bands, to enhance the probability of desired energy transitions, or to enhance the selected reaction pathways.

SUMMARY OF THE INVENTION

The present invention is directed to a method and apparatus to couple the excitation structure of a semiconductor substrate to the excitation structure of reactive adsorbates on the surface of a catalyst. Preferably, the coupling is reversible. The reversible reactor uses excitations originating in a semiconductor substrate to stimulate chemical reactions by the adsorbate species on the surface of a catalyst, and uses the reverse process to generate excitations in the substrate as the result of reactions. The method and apparatus when operated in the stimulator mode uses electrical or other forms of energy input to the semiconductor substrate to manipulate the reaction path so as to accelerate reactions, to steer the reactions, to manipulate the forms of energy produced by the reaction, and to reduce the temperature needed to stimulate surface catalytic reactions; when operated in the generator mode the apparatus converts excitation energy of the adsorbate-catalyst system into electricity

GF Exhibit 1124 - 2285/2704

or other forms of energy in the semiconductor substrate; and when operated in the stimulator-generator mode, may use electricity or other forms of energy to manipulate reactions and at the same time may generate electricity or other forms of energy from the adsorbate-catalyst system chemical reaction energy.

In the present invention, electricity or other forms of energy are used to create and inject excitation energy, such as hot carriers, into adsorbates on a catalyst surface and to stimulate adsorbate-surface catalytic reactions; and, because of the reversible nature of the process, one and the same type of apparatus may also be directed to collecting excitations that result from surface chemical reactions, such as hot carriers in a semiconductor substrate, and converting them into electricity or other forms of energy. In an exemplary embodiment, the present invention uses electronically energized semiconductor diodes in a novel way to stimulate the reactions. For example, in one embodiment, the present invention utilizes a p-n junction as the creator of hot carriers and as the injection mechanism to couple them into thin metal overlayer structures of catalyst material and to adsorbates on the catalyst surface. The same embodiment may use the same p-n junction to collect hot carriers in the semiconductor diode, forward biasing it and hence generating electricity.

The present invention includes a hot carrier emitter, also known as an excitation emitter, in intimate contact with a catalyst ensemble energy collector also known as a catalytic collector. The excitation emitter includes a semiconductor diode.

When the apparatus is operated in the stimulator mode, electrical or other energy input to the semiconductor diode causes it to generate excitations such as an excess of holes or electrons, and the resulting hot carriers and resonantly coupled excitation energy is coupled to and absorbed by the excitation

GF Exhibit 1124 - 2286/2704

structure of a catalyst-adsorbate system, thereby stimulating adsorbate chemical reactions.

When the apparatus is operated in the generator mode, excitation energy originating in a catalyst-adsorbate system is coupled into semiconductor band excitations, which can typically cause a forward bias in the semiconductor and generate electricity or other useful forms of energy.

The semiconductor diode includes an emitter, a diode junction and a semiconductor base. The emitter, which is in intimate contact with the catalytic collector, includes a semiconductor when the diode is a p-n junction diode, or the emitter includes a metal when the diode is a Schottky diode. The junction is the region of contact between the emitter and the base. The emitter also includes an electrical contact. When the hot carrier, semiconductor excitation, is chosen to be an electron then the base includes an n-type semiconductor and the emitter includes either p type semiconductor or a metal. When the hot carrier is chosen to be a hole, the base includes p type semiconductor and the emitter includes either n type semiconductor or a metal. The base also includes an electrical contact.

The catalytic collector is placed in intimate contact with the emitter and includes a catalyst, an optional underlayer, and optional reaction accelerator-decelerator materials. Elements of the catalytic collector may be one and the same with elements of the emitter. A surface of the catalyst and of the optional reaction accelerator-decelerator materials comes in intimate contact with the reactant chemicals.

Various regions of a device using this invention may include various and different catalytic collectors, hot carrier emitters and various modes of energy coupling, including ballistic transport and resonant tunneling.

GF Exhibit 1124 - 2287/2704

Further features and advantages of the present invention as well as the structure and operation of various embodiments of the present invention are described in detail below with reference to the accompanying drawings. In the drawings, like reference numbers indicate identical or functionally similar elements.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the present invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Figure 1 shows a general schematic cross section of a solid state surface catalysis reactor device of the present invention in one embodiment;

Figure 2 illustrates a cross section of a catalytic collector in one embodiment of the present invention;

Figure 3 shows a cross section of a reaction stimulator device with catalyst clusters forming the catalytic collector;

Figure 4 shows a cross section of a solid state surface catalysis reactor device with a thin electrode forming a substrate for catalyst clusters as part of a catalytic collector and also forming the electrical connection for the hot carrier emitter;

Figure 5 illustrates a cross section of a solid state surface catalysis reactor with reaction accelerator-decelerator materials surrounding or adjacent to catalyst metal;

Figure 6 illustrates a cross section of the solid state surface catalysis reactor having a single metal element that is at the same time an electrical connection to the emitter, the underlayer of the catalytic collector and forming the metal element of a Schottky diode; and

Figure 7 shows the electronic energy level diagram for the a solid state surface catalysis reactor,

GF Exhibit 1124 - 2288/2704

illustrating the regions from the n+ n type base to the adsorbate.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT OF THE INVENTION

An exemplary embodiment of the present invention uses electrons as the hot carriers and a p-n junction diode as the semiconductor diode. The base is n type semiconductor and the emitter is an p type semiconductor. A forward bias on the p-n junction diode injects minority carrier electrons into the conduction band of the p type emitter where they become minority carriers. The minority carriers diffuse and migrate to the catalytic collector and may also be resonantly coupled into the excitation structure of the adsorbate-catalyst system provided that the distance from the junction to the catalytic collector is less than several times the diffusion length of minority carriers in the p type semiconductor. For example, when InSb, InAs, or some alloy of InGaAsSb is the semiconductor, then the diffusion length can range from approximately 100 nanometers to several microns.

According to this invention, the minority carrier electrons are injected or resonantly coupled into the catalytic collector with an energy in excess of the Fermi level of the catalytic collector. This excess energy is nearly mono-energetic and has a value approximately equal to the forward bias on the diode. When the semiconductor is a p-n junction diode, the minority carrier energy may be within approximately several kT of the semiconductor band gap energy (kT = thermal energy, 0.026 eV). When the semiconductor diode is a Schottky junction the carrier energy may be within approximately several kT of the energy needed to overcome the Schottky barrier. The electrons with forward bias energy, also called hot electrons, may rapidly permeate on to a surface of the catalyst facing and in intimate contact with reactants if, for example,

GF Exhibit 1124 - 2289/2704

the distance from the p type semiconductor to the surface in contact with the reactants is less than the several times the energy mean free path of electrons in the catalytic collector.

When the catalyst is a metal such as platinum, palladium, rhodium or ruthenium the energy mean free path ranges between 5 and 50 nanometers. When the underlayer is copper or gold the energy mean free path ranges between 50 and 200 nanometers.

The flux of hot electrons interacting with the reactant chemicals is approximately that of the diode forward current if the distance from the catalytic collector to the diode junction is within the diffusion length of the emitter semiconductor and energy mean free path lengths of the catalyst and underlayer, as specified herein. Hot electrons interact strongly with adsorbates.

Another aspect of the present invention uses a Schottky diode designed to have a low barrier height, also referred to as a tunneling junction. Such a device is constructed by choosing the doping between the metal and the semiconductor of the Schottky junction to be intermediate between the very high doping used to make an almost ohmic junction, typical for making electrical contacts with the semiconductor, and the medium doping used to make a normal Schottky diode. The doping controls the width of the depletion region and hence the strength of the Schottky barrier. The value of the doping may be chosen between degenerate or high doping and conventional or moderate doping, depending on the application.

When the semiconductor is silicon and the metal is any metal associated with the catalytic collector then the doping may be adjusted to an effective value of order 0.1 eV. High doping in silicon yields effectively 0.0 eV barrier and normal doping yields barriers typically between 0.5 and 1.5 eV barrier. This tunneling junction Schottky diode permits the use of

GF Exhibit 1124 - 2290/2704

common semiconductor materials such as silicon. The use of such a diode is appropriate for use in the generator mode where reactions are pulsed.

With the methods and apparatus provided in either the p-n junction diode or the Schottky junction embodiment of the present invention, the semiconductor diode injects hot carriers or resonantly couples the carriers and with energy approximately equal to the energy of the diode forward bias voltage into the adsorbates on a surface of the catalytic collector. With the methods and apparatus provided in this invention, the energy of the injected electrons may be chosen by the user so as to steer reactions and to drive reactions in selected modes or pathways, including reaction paths inaccessible to thermal processes.

Another novel aspect of the present invention is the reversible nature of the present invention. For example, the inverse of the stimulation process is the collection of electrons generated by adsorbates reacting on the catalytic collector and the resonant coupling of energy into the semiconductor diode, creating carriers such as conduction band electrons or valence band holes. The catalytic collector acts like a collector of hot electrons generated by adsorbate chemical reaction energy instead of a collector of hot electrons generated by the hot carrier emitter. The catalytic collector couples excitations from the adsorbates to the semiconductor, instead of from the semiconductor to the adsorbates. The hot carrier emitter gets its hot electrons from the catalytic collector instead of from the diode junction. The hot carrier emitter may generate its electrons by resonant coupling of energy from the excitation structure of the adsorbate-catalyst system. The hot electrons go into the diode junction towards the base instead of out of the diode junction from the base. In so doing, the hot electrons maintain a forward bias on the diode, thereby generating electricity. This reversible nature of the present

GF Exhibit 1124 - 2291/2704

invention permits the device to generate electricity as a direct result of chemical reactions. This is a generator mode.

This same device may operate both in a stimulator and generator mode simultaneously, and thereby generate electricity more efficiently than operation in the generator mode alone. Operated in this way, the stimulator apparatus triggers and stimulates adsorbate reactions by the application of electricity or other forms of energy to the semiconductor diode. This initiates and causes the reactions to complete in a short time, for example, in the order of picoseconds. The burst of reactions result in a high peak power burst of chemical reactions, with concomitant release of electrons. The resulting flood of electrons may then be collected, thereby generating electricity. The resulting electrons may also stimulate more chemical reactions and may initiate a chain reaction analogous to an explosion or detonation. The result is a form of surface explosion. The electrons may then generate electricity much more efficiently in the semiconductor diode. The electric generating efficiency of a diode is a strong function of the peak power, and the stimulator may create a condition where the reactions achieve such high power.

When the device is operated in the stimulator mode, energy may be collected in any manner including by operating the solid state surface catalytic reactor in the generator mode. Other modes of collecting energy include but are not limited to collecting radiations emanating from reactions that have been stimulated, or by collecting heat, or by collecting the reaction products themselves, or by capturing the kinetic energy of the products as they desorb, or by collecting the phonons, or by stimulating and collecting coherent acoustic or optical radiation, or by stimulation of piezoelectric devices.

GF Exhibit 1124 - 2292/2704

When the device is operated in the generator mode, stimulation may be achieved in any manner, including by operating the solid state surface catalytic reactor in the generator mode. Other modes of stimulation include but are not limited to stimulation using pulsed laser light, a simple light flash, or the hot carriers generated on other regions of the device by other reactions whose energy outputs may include hot carriers and other catalytic products that stimulate reactions.

With the p-n junction semiconductor in the present invention, semiconductors with band gaps starting from approximately 0.05 eV to 5 eV may be used with room temperature heat sink operation, and band gaps less than 0.05 eV may be used when the system is operated at lower than room temperature. This does not preclude using materials with higher bandgaps, such as insulators like CaF2 with 12 eV bandgap, or any other material with higher bandgap. In particular, the commonly used InSb and InGaAsSb materials have band gaps that may be continuously chosen in the range 0.1 to 1.5 eV by suitable choice of the In / Ga ratio and the As / Sb ratio. The resulting range of band gaps lie precisely in the range of energies associated with hydrocarbon chemical bonds. The InSb material produces 0.18 eV electrons, which is ideal for favoring reaction stimulation Vs desorption, because higher energy electrons may stimulate an undesirable large fraction of desorptions, as opposed to surface reactions.

The p-n junction embodiment of this invention provides a substrate whose energy levels match the excited state energy levels of the adsorbates. This greatly enhances resonant transfers, in either direction, that is, to or from the adsorbate. The metals of the catalytic collector provide a resonant tunneling coupling, for example, via plasmons, between the adsorbate and the semiconductor substrate. The resonant tunneling coupling effectively connects the energy band structure of the substrate to the energy

GF Exhibit 1124 - 2293/2704

band structure of the adsorbates. An ohmic or almost ohmic junction between the catalytic collector and the semiconductor effectively pins the Fermi level of the catalytic collector to the valence band of the semiconductor. The conduction band of the semiconductor, being higher than the valence band by an amount equal to the band gap of the semiconductor, then appears above the Fermi level of the catalytic collector by the same amount, namely the band gap energy. Since the bandgap may be chosen from a palate between 0.05 to 5 eV, the bandgap energy may be made to match nearly any energy level of the system having the adsorbate and the catalytic collector. By choosing the semiconductor band gap to match the energy level of an adsorbate on the catalytic collector, one may effectively couple the two together through the well known and commonly used process of resonant tunneling. Resonant tunneling greatly increases the cross section for the transfer of energy.

This is useful in the stimulator mode to steer reactions because selected energy levels of the adsorbate may be resonantly activated by hot carriers coming from the semiconductor. This is useful in the generator mode because excited vibration states of adsorbates may be coupled resonantly to the semiconductor, enhancing energy transfer. This is useful in the stimulator-generator mode because the stimulator can trigger and initiate adsorbate reactions, using a relatively small stimulator energy, and the reactions may then spread in a manner analogous to an explosion or detonation on the surface catalytic collector exposed to reactants, which release hot carriers. The hot carriers may then generate electricity at a rate faster than they loose energy by generating heat.

In one embodiment, hot carrier emitters are fabricated using degeneratively doped or highly doped p-n junctions. In this embodiment, the switching speed

GF Exhibit 1124 - 2294/2704

can approach that of the Schottky junction because of the high carrier densities, and also because the high semiconductor doping densities form abrupt junctions, similar to that of a Schottky diode. High switching speed enhances the ability to pulse the stimulator and cause high peak power reactions. Next, the p-n junction may provide lower energy hot carriers, as low as 0.05 eV and certainly below 0.4 eV, and determined by the chosen bandgap. The p-n junction may provide very high energy monochromatic hot carriers, with energies equal to the semiconductor band gap, which exceed 5 eV for known devices. The p-n junction provides a much longer diffusion dimension than that of the Schottky junction, between 200 nanometers and several microns, over which the hot carrier can migrate and interact with surface catalysts, permitting much larger and manufacturable semiconductor devices. Further, highly doped or degeneratively doped semiconductor junctions may be produced with nearly ohmic contacts, mitigating the surface state problems.

Another novel aspect of the present invention is the co-location of both an electrically powered reaction stimulator and its inverse, a reaction driven electric generator. The stimulation causes a high rate of reaction, resulting in high peak power which in turn makes the energy generator more efficient.

In another novel aspect, the present invention allows the device to act as both stimulator and generator. The uses of combined reaction stimulation include: 1) controlling catalytic reactions; 2) monitoring those reactions using the generated electrical signal; 3) accelerating reactions on catalysts that have undesirable slow reaction rates but highly desirable selectivity; 4) causing non-thermal steering of reaction paths; 5) stimulating extremely rapid surface chain reactions to achieve high peak power while maintaining low average power; 6) causing chemical reaction temperatures like that of the hot carriers in

GF Exhibit 1124 - 2295/2704

the catalyst, which may be far in excess of the catalyst physical temperature; 7) in the stimulator-generator mode, using one type of stimulator to pulse the device to make electricity and another type to cause a self cleaning of the device, for example to remove unwanted chemical byproduct that may build up and accumulate with use, 8) initiating reaction avalanches such that the chemical reactions create their own hot carriers, forcing hot carriers to diffuse in the reverse direction, and causing the device to be an electric generator.

As described hereinabove, the present invention is directed to various aspects of the methods and devices that stimulate and manipulate chemical reactions using electrical energy input on selected catalyst surfaces, and that produce electrical energy through an inverse process.

For example, the present invention is directed to a method and apparatus for making a device that will generate hot carriers, especially hot electrons, transport them and couple them to reactant adsorbates on a catalyst surface and cause such adsorbates to acquire an effective vibrational temperature in excess of the temperature of the catalytic surface. Vibrational energy and temperature are used interchangeably. Energy is the product of the Boltzman constant and absolute temperature. Such an effective vibrational temperature in turn accelerates the reaction rates on the catalyst. Excited vibrational states of atomic and molecular adsorbates, both against the catalyst surface and internal to the adsorbates, are observed to be orders of magnitude more reactive than adsorbates in ground states. The methods and apparatus of the present invention increase adsorbate vibrational energy or temperature using an electrical stimulus without appreciably increasing the substrate thermal energy or temperature.

GF Exhibit 1124 - 2296/2704

In another aspect, the present invention is directed to methods and apparatus for reversing the above-described process, wherein excitation energies, electrons or holes generated by chemical reactions described herein above are converted coupled into a semiconductor substrate and into electricity.

Accordingly, one aspect of the present invention is directed to a reaction stimulator method and device to use electricity to create energetic carriers, particularly hot electrons, in a hot carrier emitter and inject those carriers efficiently into a catalytic collector. Preferably, the catalyst or substrate temperature need not be raised during the reaction stimulation.

In another aspect, the present invention is directed to methods and apparatus for a reaction stimulator - generator that efficiently collects energetic carriers generated by reactions on a catalyst surface, particularly hot electrons, and cause them to charge a forward biased diode through an emitter-base junction, thereby generating electricity.

In another aspect, the present invention is directed to a reaction stimulator that injects hot carriers or hot electrons with the range of energies needed to selectively favor desired types of surface chemical reactions. Preferably, the reaction stimulator is simple in design, rugged in construction, and economical to manufacture.

In another aspect, the present invention is directed to a reaction stimulator that is reversible, wherein the diffusion of hot carriers may proceed in either direction, that is, either from a chemical adsorbate reaction to a hot carrier emitter, which generates electricity, or from a hot carrier emitter to a chemical adsorbate, which uses electricity to stimulate reactions.

GF Exhibit 1124 - 2297/2704

In yet another aspect, the present invention uses the heat of vaporization of a reactant as a coolant for the operation of the semiconductor junction.

Accordingly, the method to stimulate reactions includes using electrical energy to forward bias a semiconductor diode, wherein an electric potential across the electrical contacts of the semiconductor diode creates hot carriers such as hot electrons that diffuse out of the diode junction and are transported through the catalytic collector to the chemical adsorbate, thereby stimulating the adsorbate to react.

Accordingly, the method to generate electricity includes creating hot carriers in the catalytic collector using chemical adsorbate reaction energy and transporting or coupling the hot carriers into the junction of the semiconductor diode, causing the diode to become forward biased and thereby generating electricity.

The method also includes utilizing a carrier diffusion process that transports the energetic carriers such as hot electrons to and from the diode junction to the catalytic collector.

The method also includes using a catalytic collector either to collect hot carriers provided by the emitter to transport or couple them to a chemical adsorbate on a catalyst surface or to optional reaction accelerator-decelerator materials, or, the reverse process, to collect hot carriers generated by the chemical adsorbate on a catalyst or optional reaction accelerator-decelerator materials and transport or couple them to an emitter.

The method also includes forming metal clusters, layers, atomically uniform monolayers, surface structures, crystalline layers or 1, 2 or 3 dimensional quantum confinement structures such as quantum dots, quantum stadia, quantum corrals and quantum wells from materials comprising the catalytic collector. The method includes using such layers and quantum confinement

GF Exhibit 1124 - 2298/2704

structures to tailor the density of electron and hole states of the materials, which in turn cause favorable conditions for the formation of or reaction with hot carriers. Such conditions include depletion of the number of electrons available for the decay of vibrational energies of the adsorbate-substrate system with values of transition energy less than that of the bandgap of the substrate.

This invention includes a surface catalyst reactor with tailored electron density of states and tailored energy decay modes. For example, the electron density of states may be modified by forming ordered, electron-reflective or hole-reflective structures of material on the catalytic collector surface exposed to reactants.

The method of this invention includes tailoring the carrier density of states near the Fermi surface of the catalytic collector so as to enhance the probability of forming electron-hole pairs with the desired energy distributions and for enhancing stimulation of resonant tunneling coupling of vibration states of the adsorbate-substrate system. Such tailoring may include forming and tailoring of the hot electron Fabry-Pérot modes of a thin-film electron interferometer.

The electron density of states may also be modified by forming electron interferometer structures using catalyst and other substrate materials to form structures to cause multiple path reflections of electrons including but not limited to steps, channels, stadia, corrals, pyramids, polygons, valleys, walls, periodic reflectors, and chaotic reflectors.

The method also may include using combinations of different catalyst materials and of optional reaction accelerator-decelerator materials as part of the catalytic collector, and of forming such materials in any geometry, including but not limited to pillars, islands, clusters, interdigital and random structures and stripes.

GF Exhibit 1124 - 2299/2704

The method also may include choosing catalyst and optimal accelerator-decelerator materials that delay or retard reactions of adsorbates, so that use of the stimulation mode may better control the reaction rates. Such materials may be part of the catalyst itself, adjacent to the catalyst, and may be expendables carried by the fuel - oxidizer mixture.

The method also may include choosing catalyst materials with Debye frequency lower than that of the desired hot carrier energy, to enhance the probability that the hot electron will interact with the adsorbate rather than with the phonon vibrations of the catalyst.

The shape of the device may fit contours specified by the user because the basic shape is determined by elements that are only limited in thickness by the dimensions of the semiconductor and in length and breadth by the ability to cut or form parts, which limitations permit component dimensions with less than 10 microns. This permits device contouring to nearly any macroscopic physical shape.

The method also includes using pulsed stimulation. Pulsed operation stimulates the reactions to occur with high peak power and short duration. This permits the device to remain relatively cool during the longer periods of zero stimulation after the reactions have completed and it permits the reactions to occur at a high temperature and high peak power during the relatively short periods of pulsed stimulation. Pulsing allows reactions to occur before thermal processes cause the reactions to occur. Pulsing permits the complete depletion of reactants in a time shorter than they can be replenished by the reactant gas mixture, that is, through gas kinetic means.

The method also includes using an optional underlayer material as part of the catalytic collector. The underlayer may be a metal such as copper, gold, silver or aluminum, and is chosen to be compatible with obtaining the desired properties with the semiconductor

GF Exhibit 1124 - 2300/2704

component of the hot carrier emitter. One desired property is an ohmic or almost ohmic junction. The underlayer may be used as an electrical connection in the hot carrier emitter and may also be used as an electrical connection to the catalytic collector. The underlayer may be used as a substrate upon which to fabricate catalyst structures, more underlayers or specified geometries and crystal orientations of materials deposited as part of the catalytic collector, or to tailor the lattice constants of materials deposited on the underlayer.

The method also includes limiting the thickness of the underlayer to less than several energy mean free paths of the hot carrier chosen for the device. For example, any underlayer may be between one monolayer (approximately 0.3 nanometers) and 50 nanometers when the underlayer metal includes but is not limited to platinum, nickel, palladium, rhodium, rhenium, copper, gold, silver or aluminum.

The method includes enclosing all or selected components of the device in an optical cavity tuned to an energy associated with the excitation structure of the semiconductor, or of the catalytic collector or of the adsorbates or of some combination of these elements.

An apparatus to stimulate reactions or to generate electricity according to the present invention includes a hot carrier emitter and a catalytic collector. The hot carrier emitter belonging to this apparatus includes a semiconductor diode. The semiconductor diode includes a semiconductor base, a diode junction also called an emitter-base junction, and an emitter. The emitter includes a semiconductor or a metal as a diode element. The apparatus may also include a first electrical connection to the emitter and a second electrical connection to the base.

An apparatus to stimulate reactions or to generate electricity according to the present invention may include an optional optical cavity tuned to a desired

GF Exhibit 1124 - 2301/2704

energy level transition of either the excitation structure of the semiconductor or of the system including the catalytic collector and chemical adsorbate. Such cavities may include and are not limited to metal and dielectric microcavities, periodic structures that exhibit photonic band gap properties, fabrey-perot cavities, textured mirrors, distributed Bragg reflectors, single and coupled semiconductor microcavities, external cavities with a wavelength filter or a large dispersion, quantum dot vertical cavities, microdisk cavities, quantum dot microdisk cavities, laser waveguides with or without cladding, dielectric slab waveguides, cavities associated electromagnetic surface waves, also called surface plasmons, at a metal-semiconductor interface where no additional confinement layer is needed, chaotic resonators, optical resonators with deformed cross section, resonator designs that incorporate chaotic ray motion, and symmetric resonators with whispering-gallery modes.

In one embodiment, the hot carriers are electrons, the diode is a p-n junction made of InSb with n type base and p type emitter and the catalytic collector is located or co-located in the proximity of the emitter electrical contact. The catalyst ensemble includes a catalyst metal such as any alloy of platinum and palladium and deposited in a surface structure, cluster or quantum confined structure. The configuration or geometry of the catalyst, for example, is such that the distance to the semiconductor from regions of catalyst exposed to adsorbates is predominantly less than 3 times the energy mean free path in platinum, which mean free path is approximately 20 nm. The catalyst metal is in direct contact with the semiconductor of the emitter, which semiconductor is degeneratively doped to form an ohmic or tunneling junction. In this embodiment, the p-n junction is formed a distance from the catalytic collector that is less than 3 times the diffusion

GF Exhibit 1124 - 2302/2704

distance for electrons in the conduction band of p type InSb, which diffusion distance may be as little as 200 nanometers. The device may be operated in the stimulator mode, the generator mode or the stimulator-generator mode, and where the hot electrons may be created either by the chemical adsorbate reactions or by electrical energy input to the semiconductor diode.

The reversible solid state surface catalysis excitation transfer reaction apparatus in the present invention couples the excitation band structures of the adsorbate-catalyst system with the excitation band structure of the semiconductor substrate. The apparatus may be designed to operate on gaseous reactants. In the generator mode, the energies of excitations associated with chemical reactions of adsorbates on and with the surface of a catalytic collector are converted into excitations such as hot carriers and electromagnetic fields.

The energies of excitations associated with reactions of adsorbates include excited reactant molecular vibrations molecule-surface vibrations, atom-surface vibrations, adsorption reactions, chemical reactions and excited electronic states. The converted excitations such as hot carriers and electromagnetic fields are transported to the excitation emitter where semiconductor or emitter excitations are created and may be converted into useful forms of energy. The emitter excitations include minority carriers, hot carriers, carrier diffusion, coupling electric fields, excitons, and plasmons in the semiconductor.

Also, in the generator mode, pulses of excitation energies associated with chemical reactions of adsorbates occurring on and with the surface of a catalytic collector, such as excited reactant molecular vibrations, molecule-surface vibrations, atom-surface vibrations, adsorption reactions, chemical reactions and excited electronic states, may be converted into excitations such as hot carriers and electromagnetic

GF Exhibit 1124 - 2303/2704

fields. These excitations are transported to an emitter or the excitation emitter where excitations such as minority carriers, hot carriers, carrier diffusion, coupling electric fields, excitons, and plasmons in the semiconductor are created and may be converted into useful forms of energy.

In one embodiment, the excitation emitter and the catalytic collector may share a component common to both of them.

Figure 1 illustrates a general schematic cross section of a solid state surface catalysis reactor device. The device 100 comprises an emitter 102 and a catalytic collector 104, formed on a base 108. A semiconductor p-n junction 110 is formed between the emitter 102 and the base 108. An emitter electrical connection 114 and catalytic collector 104 are arranged as shown in Figure 1. A base electrical connection 112 is also arranged in contact with the base 108 as shown in Figure 1. Reactants and products interact on the catalyst surface 116 of the catalytic collector 104. The reactants may include but are not limited to the hydrocarbon chains, ethane, ethylene, propane, propylene, propene, butane, butene, cetane, isomers thereof.

In the stimulation mode, the device 100 utilizes electrical energy to create energetic carriers, also referred to as hot carriers or hot electrons. The hot carriers diffuse into the catalytic collector 104, interact strongly with reactants on the catalyst surface 116 and accelerate the reactions to produce reaction products. The stimulated reactions may cause a chain reaction or the equivalent of a surface explosions. The stimulated reactions may also cause an autocatalyzed chain reaction.

In the generation mode, the hot electrons, generated by chemical reactions occurring on the catalyst surface 116 and diffusing across the junction

GF Exhibit 1124 - 2304/2704

110, for example, a p-n junction, cause a forward bias across the junction and generate electrical energy.

In an exemplary embodiment, a p-n junction is used with p type emitter and n-type base to create hot electrons. Accordingly, the junction 110 may be forward biased. When the hot carrier is a hot electron, as opposed to a hot hole, the junction may be a p-n junction with p type emitter and n-type base. Alternatively, the junction may be a Schottky junction with a metal emitter and n-type semiconductor base.

In the stimulation mode, the forward biased junction 110 creates hot electrons. For example, when the base contact 112 is biased negative and the emitter contact 114 is biased positive, hot electrons are created in the junction 110. The hot electrons diffuse through the emitter 102 and ballistically transport through the catalytic collector 104 to the catalyst surface 116.

In the generator mode, hot electrons originating on the catalyst surface 116 may also ballistically transport through the catalytic collector 104 and diffuse to the junction 110, causing the emitter-base junction diode 110 to become forward biased.

For example, when hot electrons transport and diffuse from the catalyst surface 116 to the junction 110, the base contact 112 becomes biased negative and the emitter contact 114 becomes biased positive, and the diode in the present invention becomes an electron source instead of a sink.

These hot electrons migrate or diffuse to or from the emitter 102, and to or from the catalyst surface 116. Accordingly, in an exemplary embodiment, the distance from the diode junction 110 to the adsorbates on the surface of the catalyst 116 is formed to be less than the distance over which the energy of these carriers degrades. This distance is generally less than several times the energy mean free path of such energetic hot electrons when evaluated over the path

GF Exhibit 1124 - 2305/2704

from the emitter-base junction 110 to the adsorbates on the catalyst surface 116.

Using the process described herein above, reactants adsorbing on the catalyst surfaces become vibrationally excited by the hot electrons, which excitation accelerates the reaction and forms products. Using these means, hot electrons created by the reactants adsorbed on the collector catalyst ensemble create a potential in the forward biased diode.

In an exemplary embodiment of the present invention, the catalytic collector 104 includes catalyst materials in layers, clusters, atomically uniform monolayers, or surface structures. Preferably, the layers or clusters have thickness dimension less than several times the total energy mean free path of hot electrons in the catalyst. The layers or clusters are formed close enough to the diode junction 110 such that hot electrons may diffuse directly between the junction 110 and the catalyst surface 116.

The total energy mean free path of hot electrons in catalysts such as platinum or palladium is of order 20 nanometers and is far shorter than in Au, Ag or Cu. Therefore, according to an exemplary embodiment, catalyst clusters or layers are fabricated with cluster, layer thickness or thickness dimension less than this smaller value. For example, the electron energy lifetime has been measured in Tantalum, a representative transition metal electronically similar to the platinum group, and is of order 15 fs. The calculated lifetime in palladium based on the Fermi inverse square scaling would be 600 fs at 0.3 eV and giving a total energy mean free path of 840 nanometers. Instead of this optimistic large value, it is presumed the lifetime is as poor as that measured in tantalum. This gives a total energy mean free path in platinum or palladium of order 21 nanometers. In this embodiment, the catalyst dimension is less than the measured energy mean free path of the hot electrons. These arguments concerning the total

GF Exhibit 1124 - 2306/2704

thickness of an underlayer, which is the electrical connection to the catalyst, and the catalyst, are only to assert that the path taken by the hot carrier through such catalyst and underlayer shall not be so long as to significantly degrade the hot carrier energy, and any dimension satisfying this condition is acceptable.

Preferably, the methods provided in the present invention generate electrons that have energies in the range that favor reaction over desorption. These energies are in the range 0.05 to 0.4 eV. Similarly, the method to collect electrons generated by chemical reactions on the catalyst surfaces collect electrons whose energies are also in the range of 0.05 to 0.4 eV. Accordingly, a semiconductor material with band gap less than approximately 0.4 eV may be used. Examples of such semiconductor material include indium antimonide (InSb) or indium arsenide (InAs) which have band gaps of 0.18 eV and 0.35 eV, respectively. The energetic electrons produced with these semiconductors have energy approximately equal to the band gap in the p type semiconductor emitter. Hot electrons diffusing back into the n-type base generate electric potentials whose magnitude approaches the band gap energy. Generally, the value of the band gap is selected based on the nature of the reactants and the energies associated with their surface activity.

In an exemplary embodiment, the catalyst clusters may further include activators, de-activators, decelerator or accelerators placed in their proximity, such as oxides or other materials, as shown in cross section in Figure 2. Figure 2 illustrates a cross section 200 of a catalytic collector including reaction accelerator-decelerator materials 206 adjacent to and co-located with the catalyst materials 202. As shown, the hot electron catalytic collector includes the catalyst materials 202, an optional thin electrode underlayer 204, and reaction accelerator-decelerator materials 206 such as oxides. For example, oxides of

GF Exhibit 1124 - 2307/2704

the catalyst itself, of cerium, titanium or aluminum may be formed between the catalyst islands or layers. The total dimension of the catalyst and thin electrode underlayer 204 is preferably less than several times the total energy mean free path of a hot electron.

Figures 3, 4, and 5 illustrate several different embodiments of the catalytic collector used in a solid state surface catalysis reactor of the present invention. As shown in the Figures, the catalytic collector may include catalyst material such as islands that reside directly on the semiconductor (Figure 3), or of catalysts on a thin electrode underlayer (Figure 4) which also forms the electrical connection for the hot carrier emitter, or catalysts with reaction accelerator-decelerator materials surrounding or adjacent to the catalysts, all residing on a thin electrode underlayer which also forms the electrical connection for the hot carrier emitter(Figure 5).

The catalyst may include materials such as Au, Ag, Pt, Pd, Cu, In, Fe, Ni, Sn, and Mo. The catalyst may be formed into structures including metal clusters, pillars, islands, layers, crystalline layers, atomically uniform monolayers, interdigital and random structures, stripes, or surface structures. The catalyst may also be formed into one, two, or three dimensional quantum confinement structures such as quantum dots, quantum stadia, quantum corrals and quantum wells.

Figure 3 shows a cross section 300 of the solid state surface catalysis reactor device comprising a hot carrier emitter where the carrier is an electron, a catalytic collector. The catalytic collector ensemble includes catalyst islands 302, preferably formed such that the distance to the semiconductor 304 less than the three times the total energy mean free path of the hot electron in the catalyst 302. Preferably, the catalyst islands 302 are bonded to the p doped or heavily p doped, p+ region of the semiconductor 304. In one embodiment, the catalyst materials 302 are spread over

GF Exhibit 1124 - 2308/2704

the surface of the semiconductor. In another embodiment, the catalyst is formed with surface structures containing atomically uniform monolayers.

The hot, for example, electron, carrier emitter includes the semiconductor diode formed by negative electrode 306 in contact with n type semiconductor 308, p type semiconductor 312, p-n junction 310 formed between the n type semiconductor 308 and the p type semiconductor 312, p doped or heavily p doped p+ semiconductor 304, and positive electrode 314.

Figure 4 illustrates a cross section 400 of a solid state surface catalysis reactor device with thin electrode 402 forming a substrate for catalyst structures. In this embodiment, the catalytic collector includes a thin electrode underlayer 402, catalyst structures 404 and a bus bar electrical connection 406 in electrical contact with the thin electrode underlayer 402. The hot electron emitter includes a semiconductor diode formed by negative electrical connection 408, n-type semiconductor 410, p-n junction 412, p type semiconductor 414, p doped or heavily p doped p+ semiconductor 416, and thin electrode underlayer 402. As shown, the thin electrode underlayer 402 may be common to the hot electron emitter and the catalytic collector. The thin electrode underlayer 402 may be a thin positive electrode. The thin electrode underlayer 402 is preferably selected from those materials that make an ohmic or almost ohmic junction to the semiconductor.

The thin electrode underlayer 402 provided in the present invention forms ohmic or almost ohmic junctions to the semiconductor 416 while also providing a path for hot electrons to enter or leave the catalyst 404. With some selection of combinations of catalyst metal and semiconductor, the ohmic properties of the junction between the semiconductor 416 and catalyst 404 may form a Schottky junction instead. In cases where a Schottky junction is formed, a layer of metal, i.e., the thin

GF Exhibit 1124 - 2309/2704

electrode underlayer 402 is used as the means to form a practically ohmic junction, which may be almost ohmic or a tunneling Schottky junction. The catalyst clusters or layers 404 are then placed on top of the thin electrode underlayer metal 402. In an exemplary embodiment, the thickness of the electrode underlayer 402 is selected to be much less than the energy mean free path of the hot electrons passing through it.

For 0.3 eV electrons in commonly used contact metals such as silver ("Ag"), gold ("Au"), and copper ("Cu"), the electron energy lifetime exceeds 200 femtoseconds and the electron velocity is of order 1.4e6 meters/second. The resulting energy mean free path is therefore of order 280 nanometers. This permits the underlayer electrical contact to the semiconductor to be an order of magnitude thicker than the catalytic collector and enhances manufacturability. Thin, 1 to 5 nanometer ("nm") layers of Au, Ag and Cu conductors are routinely fabricated on semiconductors, permitting a thin layer to form the ohmic or almost ohmic contact with semiconductor. This thin layer, e.g., the thin electrode 402, assures that the Fermi level of the catalyst and the Fermi level of the p type semiconductor emitter are the same or practically the same. In this embodiment, a thin, 1 to 20 nm layer of metal such as Au, Ag or Cu may be used as the electrode 402 or substrate for the catalyst ensemble. It should further be appreciated that the present invention does not limit the choice of contact metal used to form the electrode to Au, Ag or Cu, and other metals, alloys or semi-metals may be selected to form at least a nearly ohmic junction with the semiconductor.

For the embodiment in which the hot electron emitter includes a heavily doped semiconductor, for example as shown in 304 of Figure 3 and in 416 of Figure 4, the material used for the thin electrode 402 may be selected so that the junction between the electrode 402 and the heavily doped semiconductor 416 forms at least

GF Exhibit 1124 - 2310/2704

an almost ohmic junction. Preferably, the junction formed is an ohmic junction. To form an ohmic junction or an almost ohmic junction, the semiconductor doping is selected sufficiently high so that the dimension or thickness of any Schottky barrier formed by this junction is sufficiently small that electron tunneling dominates the current flow. Accordingly, the p type semiconductor may be heavily or degeneratively doped near the region of contact with the metal. Such heavy doping occurs when the dopant concentration exceeds approximately 1e18 per cubic centimeter. Figure 3 shows this heavily doped region 304 near both the emitter electrical connection 314 and catalyst clusters 302. Figure 4 shows this heavily doped region 416 in contact with the thin electrode underlayer 402.

As an example, a preferred doping of 2e19 per cc donors in InSb or InAs is considered to be such a heavy doping. Degenerative doping of the semiconductor to 2e20 per cc and bonding a suitable metal, such as Au, Ag, or cu, as the thin metal contact can make an almost ohmic electrical connection to the semiconductor. Nearly any metal may form such an almost ohmic junction because the junction dimension under heavy or degenerative doping is of order 1 nanometer or less, and at this dimension tunneling across the junction is predominating. A junction of this type typically has characteristic p-n junction dimension of order 3 nanometers or less and electron diffusion length in the emitter and collector regions in excess of 1 micron. The dimension may be limited by Auger recombination. Therefore, the junction between the emitter and the catalytic collector elements of the present invention can be readily constructed since .1 micron thickness and greater dimension is routinely achieved in practice.

The thin electrode is bonded to the p type semiconductor surface. The catalyst clusters or layers are placed on the thin electrode and preferably near to the p-n junction. "Near" is defined to be "a distance

GF Exhibit 1124 - 2311/2704

that is within the diffusion dimension of minority carriers in the emitter semiconductor." This dimension is typically of order 0.1 micron or more. The calculated diffusion length of electrons in p type InSb doped to 2e20 per cc is of order 7 microns and 5.5 microns in InAs. However, observed Auger lifetimes of 1 picosecond suggest the diffusion length is of order 1 micron. As will be appreciated by those skilled in the art, this dimension is well within current manufacturing state of the art. Accordingly, the catalyst metal 302 and 404 or the thin metal contact underlayer 402 may serve as both the catalytic collector and an emitter positive electrical connection. This also reduces the cost and complexity of fabrication.

Figure 5 shows a cross section 500 of a solid state surface catalysis reactor device similar to that illustrated in Figure 4 and with reaction accelerator-decelerator materials 502 surrounding or adjacent to catalyst structures 404. As described with reference to Figure 2, in an exemplary embodiment, the catalyst clusters may further include chemical surface reaction activators, accelerators or decelerators placed in their proximity, such as oxides or other materials. As shown, the catalytic collector includes the catalyst structures 404, an optional thin electrode underlayer 402, and catalyst accelerators or decelerators 502 such as oxides. For example, oxides of the catalyst itself, or oxides of cerium, titanium or aluminum may be formed between the catalyst islands or layers. The distance a hot electron must travel through the catalyst 404 and thin electrode underlayer 402 is preferably less than several times the total energy mean free path.

Figure 6 shows a cross section 600 of the solid state surface catalysis reactor device including a single metal element 605 that is at the same time an electrical connection to the emitter, the underlayer of the catalytic collector and forms the metal element of a Schottky diode.

GF Exhibit 1124 - 2312/2704

Shown in Figure 6 is a solid state surface catalysis reactor device using a Schottky diode. Reactants adsorb on the catalytic collector 605, 606 and 607. A Schottky diode is formed between the thin metal underlayer 605, the more heavily doped semiconductor 604 shown as n type for illustration appropriate for the hot carrier being hot electrons, the lesser doped semiconductor region 601, and the thicker negative electrical connection 606. Bus bar 602 provides the electrical connection for the current-carrying, positive, thin electrode 605. In operation, the diode is pulsed with a forward bias, that is, electrode 606 is pulsed negative with respect to positive electrode 605, consuming electric power. This triggers surface reactions on the catalyst ensemble 607 and causes products to be formed. Excess reaction energy may produce a burst of hot electrons which travel through the thin catalyst structure 607 and element 605, surpass the Schottky barrier potential and enter the diode regions 601 and 604, forward biasing the diode and producing electric power.

The reversible nature of this embodiment is shown for illustration. The reaction stimulation properties of the same device may be its principle function. The electrical generation properties may be the principle function.

Figure 7 illustrates the electronic energy levels diagram 700 of the elements of the solid state surface catalysis reactor device appropriate for the case where the hot carrier is a hot electron. These elements include an adsorbate 702, catalyst 704, positive electrode or electrical connection 718, electrode junction, highly doped semiconductor in the collector-emitter region 706, p doped semiconductor region 708, p-n junction region 710, n doped 712 and the heavily n doped 714 region.

In the stimulation mode, a forward bias 716 drives electrons from the n+ region 714 where they are majority

GF Exhibit 1124 - 2313/2704

carriers, into the p-n junction 710, into the p type region 708 of the semiconductor where they are minority carriers, into the catalyst 704, and then to the catalyst surface where they interact with the adsorbate 706. The hot electron excites states in the adsorbate which stimulate reactions.

In the generation mode, an energy decay path in the excited state of the adsorbate creates hot electrons on the catalyst surface; the hot electrons then travel through the catalyst to the p type semiconductor region and then continue to the p-n junction 710 where the internal electric fields in the semiconductor sweep them over to the n+ region 714, creating a forward bias, which becomes a source of electric power.

In this and all other embodiments, the effectiveness of the stimulator, generator and reactor may be greatly enhanced by providing reactants in the gas phase. In this case, the adsorbates on the catalyst surface interact with the hot carriers. When a liquid covers the catalyst, multiple layers of adsorbate absorb the hot electron and diminish its effectiveness. Thus, a point of novelty of this invention also include the use of forward biased devices for the purpose of reaction stimulation or electric generation.

While the invention has been particularly shown and described with respect to a preferred embodiment thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention. For example, those skilled in the art will appreciate that the features of the invention may sometimes be used to advantage without a corresponding use of the other features shown or described herein above. Similarly, some features may be combined, within the scope and equivalents of the present invention, to achieve a desired result.

GF Exhibit 1124 - 2314/2704

CLAIMS

We claim:

1. A solid state surface catalysis excitation transfer reaction apparatus comprising:

a catalytic collector; and

an excitation emitter including a p-n junction diode whose excitation band structure is coupled to excitation band structure associated with the catalytic collector,

wherein one or more energies associated with reactions of adsorbates occurring in the catalytic collector are converted into excitations and transported to the excitation emitter where emitter excitations are generated and converted into one or more forms of energy.

2. The apparatus as claimed in claim 1, wherein the reactions of adsorbates occur on a surface of the catalytic collector.

3. The apparatus as claimed in claim 1, wherein the reactions of adsorbates occur with a surface of the catalytic collector.

4. The apparatus as claimed in claim 1, wherein the one or more energies include one or more excited reactant molecular vibrations.

5. The apparatus as claimed in claim 1, wherein the one or more energies include one or more molecule-surface vibrations.

6. The apparatus as claimed in claim 1, wherein the one or more energies include one or more atom-surface vibrations.

GF Exhibit 1124 - 2315/2704

7. The apparatus as claimed in claim 1, wherein the one or more energies include one or more adsorption reactions.

8. The apparatus as claimed in claim 1, wherein the one or more energies include one or more chemical reactions.

9. The apparatus as claimed in claim 1, wherein the one or more energies include one or more excited electronic states.

10. The apparatus as claimed in claim 1, wherein the excitations include one or more hot carriers.

11. The apparatus as claimed in claim 1, wherein the excitations include one or more electromagnetic fields.

12. The apparatus as claimed in claim 1, wherein the emitter excitations include one or more minority carriers.

13. The apparatus as claimed in claim 1, wherein the emitter excitations include one or more hot carriers.

14. The apparatus as claimed in claim 1, wherein the emitter excitations include energies transported by carrier diffusion.

15. The apparatus as claimed in claim 1, wherein the emitter excitations include coupling electric fields.

16. The apparatus as claimed in claim 1, wherein the emitter excitations include one or more excitons.

GF Exhibit 1124 - 2316/2704

17. The apparatus as claimed in claim 1, wherein the emitter excitations include one or more plasmons.

18. The solid state surface catalysis excitation transfer reaction apparatus as claimed in claim 1, wherein the catalytic collector is in contact with the emitter.

19. The apparatus as claimed in claim 1, wherein the p-n junction diode is forward biased.

20. The apparatus as claimed in claim 1, wherein the emitter excitations are created when the p-n junction becomes forward biased.

21. The apparatus as claimed in claim 20, wherein an electric potential applied across the p-n junction diode causes a forward bias in the p-n junction diode.

22. The apparatus as claimed in claim 20, wherein optical absorption of photons in the p-n junction diode causes the forward bias in the p-n junction diode.

23. The apparatus as claimed in claim 10, wherein the one or more hot carriers include one or more hot electron.

24. The apparatus as claimed in claim 1, wherein the p-n junction diode includes a p-type emitter region and an n-type base.

25. The apparatus as claimed in claim 1, wherein the p-n junction diode includes a highly doped p+ region.

26. The apparatus as claimed in claim 24, wherein the p-type emitter region is highly doped.

GF Exhibit 1124 - 2317/2704

27. The apparatus as claimed in claim 1, wherein the p-n junction diode includes a highly doped n+ region.

28. The apparatus as claimed in claim 24, wherein the n-type base is highly doped.

29. The apparatus as claimed in claim 1, wherein the excitation emitter is fabricated from semiconductor material that includes any one or combination selected from In, Ga, As and Sb.

30. The apparatus as claimed in claim 1, wherein the excitation emitter is fabricated from semiconductor material that includes any one or combination selected from In, Sb, Bi, and T1.

31. The apparatus as claimed in claim 1, wherein the excitation emitter is fabricated from semiconductor material that includes any one or combination selected from Hg, Cd, and Te.

32. The apparatus as claimed in claim 31, wherein a concentration of cadmium (Cd) is between 20% and 30%.

33. The apparatus as claimed in claim 1, wherein a distance from a p-n junction in the p-n junction diode to the catalytic collector is less than three times a diffusion length of minority carriers in the p-n junction diode.

34. The apparatus as claimed in claim 1, wherein the catalytic collector further includes:

a catalyst,

wherein total path traveled by energetic carriers between a catalyst surface exposed to adsorbate reactants and a semiconductor of the excitation emitter

GF Exhibit 1124 - 2318/2704

is less than three times the total energy mean free path of the energetic carriers along the path.

35. The apparatus as claimed in claim 1, wherein ballistic carrier transport is used to transport energetic carriers in the catalytic collector and the excitation emitter.

36. The apparatus as claimed in claim 1, wherein the apparatus further includes an ohmic electrical connection connecting the catalytic collector and the excitation emitter.

37. The apparatus as claimed in claim 1, wherein the apparatus further includes a tunneling Schottky junction connecting the catalytic collector and the emitter.

38. The apparatus as claimed in claim 34, wherein the catalyst includes one or more catalyst clusters.

39. The apparatus as claimed in claim 38, wherein the catalyst further includes one or more reaction accelerator-decelerator surrounding the one or more catalyst clusters.

40. The apparatus as claimed in claim 39, wherein the one or more reaction accelerator-decelerator include an oxide.

41. The apparatus as claimed in claim 40, wherein the oxide includes one selected from titanium, cerium, rare earth metals, tin, lead, and aluminum.

42. The apparatus as claimed in claim 40, wherein the oxide includes material of the catalyst.

GF Exhibit 1124 - 2319/2704

43. The apparatus as claimed in claim 38, wherein the catalyst further includes one or more reaction accelerator-decelerator adjacent to the one or more catalyst clusters.

44. The apparatus as claimed in claim 38, wherein the catalyst further includes one or more reaction accelerator-decelerator in contact with the one or more catalyst clusters.

45. The apparatus as claimed in claim 34, wherein the catalyst has a Debye frequency less than the vibration decay frequency of the dominant mode of energy relaxation of at least one of adsorbate reactants.

46. The apparatus as claimed in claim 1, wherein the catalytic collector includes a material having Debye temperature less than 500 degrees Kelvin.

47. The apparatus as claimed in claim 34, wherein the catalyst includes material selected from any one of Au, Ag, Pt, Pd, Cu, In, Fe, Ni, An, and Mo.

48. The apparatus as claimed in claim 34, wherein the catalyst is formed into metal clusters.

49. The apparatus as claimed in claim 34, wherein the catalyst is formed into a quantum confinement structure.

50. The apparatus as claimed in claim 1, wherein the catalytic collector further includes at least one electrode underlayer metal formed between the excitation emitter and a catalyst in the catalytic collector.

51. The apparatus as claimed in claim 50, wherein the electrode underlayer metal forms a substrate for one or more catalysts in the catalytic collector.

GF Exhibit 1124 - 2320/2704

52. The apparatus as claimed in claim 50, wherein the electrode underlayer metal forms a substrate for one or more reaction accelerator-decelerator in the catalytic collector.

53. The apparatus as claimed in claim 50, wherein the electrode underlayer metal has a thickness less than three times energy mean free path of the excitations going through it.

54. The apparatus as claimed in claim 50, wherein an ohmic junction is formed between the electrode underlayer metal and the excitation emitter.

55. The apparatus as claimed in claim 50, wherein a tunneling Schottky junction is formed between the electrode underlayer metal and the excitation emitter.

56. The apparatus as claimed in claim 50, wherein an almost ohmic junction is formed between the electrode underlayer metal and the excitation emitter.

57. The apparatus as claimed in claim 1, wherein the apparatus further includes an optical cavity coupled to a region of adsorbate reactions.

58. The apparatus as claimed in claim 57, wherein the optical cavity is tuned to a selected energy level transition in the excitation band structure of at least one of the excitation emitter, the catalytic collector, and the adsorbate.

59. The apparatus as claimed in claim 57, wherein the optical cavity includes dielectric micro cavities.

60. The apparatus as claimed in claim 57, wherein the optical cavity stimulates emission of radiation.

GF Exhibit 1124 - 2321/2704

61. The apparatus as claimed in claim 57, wherein the optical cavity stimulates energy transitions of the excitation band structure of the excitation emitter.

62. The apparatus as claimed in claim 1, wherein the one or more forms of energy include pulsed energy.

63. The apparatus as claimed in claim 62, wherein the one or more forms of energy include pulsed electrical energy.

64. The apparatus as claimed in claim 62, wherein the one or more forms of energy include pulsed optical energy.

65. A method of converting adsorbate reaction energy into power, comprising:

coupling one or more excitation band structures of an adsorbate-catalyst into one or more excitation band structures of an excitation emitter;

optimizing the coupling to a diode in the excitation emitter; and

converting one or more excitations in the diode to power.

66. The method of claim 65, wherein the coupling includes forming a catalytic collector in the adsorbate-catalyst with one or more quantum confinement surface structures.

67. The method of claim 65, wherein the coupling includes tuning one or more optical cavities to a frequency of the one or more excitation band structures of at least one of the adsorbate-catalyst and the excitation emitter.

GF Exhibit 1124 - 2322/2704

68. The method of claim 65, wherein the coupling includes forming a catalytic collector in the adsorbate-catalyst and the optimizing includes constraining the thickness of a region between a surface of the catalytic collector exposed to adsorbate reactants and the excitation emitter, the region having a thickness of less than three energy mean free paths of hot carriers exchanged between the catalytic collector and the excitation emitter.

69. The method of claim 65, wherein the optimizing includes selecting a substrate with band gap energy less than or equal to a selected excitation in the adsorbate-catalyst.

70. The method of claim 65, wherein the optimizing includes adjusting a forward bias of the diode such that a band of excitation energy in the excitation emitter matches a band of excitation energies in the adsorbate-catalyst.

71. The method of claim 65, wherein the coupling includes selecting a catalyst with Debye frequency lower than a selected energy level of the one or more excitation structures of the adsorbate-catalyst system.

72. A method of converting reaction energy into power, comprising:

converting one or more adsorbate reactants into hot carriers;

keeping the hot carriers hot while the hot carriers are transported to a diode;

converting the hot carriers into a forward bias in the diode.

73. The method of claim 72, wherein the method further includes:

converting the hot carriers into minority carriers;

GF Exhibit 1124 - 2323/2704

conveying the minority carriers to a p-n junction region of the diode; and

generating a forward bias to generate power.

74. The method of claim 73, wherein the power includes electricity.

75. The method of claim 72, wherein the method further includes:

forming a population inversion by the hot carriers in the diode; and

extracting optical energy.

76. The method of claim 75, wherein the extracting includes extracting laser action.

77. The method of claim 75, wherein the extracting includes extracting super-radiant emissions.

78. The method of claim 72, wherein the method further includes:

modifying one or more electron density of states of a material in a catalytic collector to match a selected range of energy transitions of one or more excitation band structures of an adsorbate-catalyst system having the adsorbate reactants.

79. The method of claim 78, wherein the modifying includes forming one or more catalyst monolayers.

80. The method of claim 78, wherein the modifying includes forming one or more ordered electron-reflective structures on a surface exposed to the adsorbate reactants.

81. The method of claim 78, wherein the modifying includes forming one or more ordered hole-reflective

GF Exhibit 1124 - 2324/2704

structures on a surface exposed to the adsorbate reactants.

82. The method of claim 78, wherein the modifying includes forming one or more hot electron Fabry-Perot modes of a thin-film electron interferometer.

83. The method of claim 78, wherein the modifying includes forming one or more catalyst monolayers.

84. The method of claim 78, wherein the modifying includes forming one to one hundred catalyst monolayers.

85. The method of claim 78, wherein the modifying includes forming one or more integer catalyst monolayers.

86. The method of claim 78, wherein the modifying includes forming one or more electron interferometer structures to cause a plurality of electron path reflections.

87. The method of claim 72, wherein the method further includes adding one or more expendable additives to the adsorbate reactants.

88. The method of claim 87, wherein the expendable additives include one or more catalyst materials.

89. The method of claim 87, wherein the expendable additives include one or more reaction accelerator-decelerator materials.

90. The method of claim 72, wherein the one or more adsorbate reactants have a partial pressure such that no more than one monolayer for each of the one or more adsorbate reactants is formed.

GF Exhibit 1124 - 2325/2704

91. The method of claim 90, wherein the partial pressure is less than ten atmospheres.

92. The method of claim 72, wherein at least one of the adsorbate reactants is gaseous.

93. The method of claim 72, wherein the one or more adsorbate reactants include one or more decelerator materials.

94. The method of claim 72, wherein the one or more adsorbate reactants include one or more accelerator materials.

95. The method of claim 72, wherein the one or more adsorbate reactants include one or more hydrocarbon chains.

96. The method of claim 72, further including:

cooling the diode with a heat of vaporization of the one or more adsorbate reactants.

97. The method of claim 72, further including:

cleaning a catalyst by a reaction of the one or more adsorbate reactants.

98. A reversible solid state surface catalysis excitation transfer reaction apparatus comprising:

a catalytic collector; and

an excitation emitter whose excitation band structure is coupled to excitation band structure associated with the catalytic collector,

wherein one or more energies associated with reactions of adsorbates occurring in the catalytic collector are converted into excitations and transported to the excitation emitter where emitter excitations are generated and converted into one or more forms of energy, and

GF Exhibit 1124 - 2326/2704

wherein an energy applied to the excitation emitter creates the emitter excitations, the emitter excitations transported to adsorbates in the catalytic collector where the transported emitter excitations energize the excitations, the excitations causing reaction stimulation in the catalytic collector.

99. The apparatus as claimed in claim 98, wherein the energy applied to the excitation emitter is pulsed electric power.

100. The apparatus as claimed in claim 98, wherein the reaction stimulation generates hot carriers.

101. The apparatus as claimed in claim 100, wherein the hot carriers further stimulate additional reactions.

102. A method of stimulating reactions, comprising:

creating hot carriers in an excitation emitter, the excitation emitter in contact with a catalytic collector, by applying power to a diode in the excitation emitter;

transporting the hot carriers originating in the diode into the catalytic collector having catalyst material;

manipulating thickness properties of the catalyst material such that the hot carriers remain hot while they are transported to a surface of the catalytic collector, the surface being exposed to reactants.

103. The method of claim 102, wherein an electrical power pulse is applied to forward bias the diode.

104. The method of claim 102, wherein the power applied includes electrical power pulse with duration

GF Exhibit 1124 - 2327/2704

shorter than a lifetime of a longest lived excited state of the hot carriers.

105. The method of claim 102, wherein the power applied includes electrical power pulse with duration shorter than a lifetime of polariton states.

106. The method of claim 102, wherein the power applied includes electrical power pulse with duration less than 1 nanosecond.

107. The method of claim 102, wherein the power applied includes electrical power pulse with duty cycle less than 1/2.

108. The method of claim 102, wherein the power applied includes electrical power pulse with repetition times comparable to or less than an average time during which gaseous reactants can replenish a surface of depleted reactants.

109. The method of claim 102, wherein the power applied includes electrical power pulse with repetition rate higher than 50 megahertz.

110. The method of claim 102, wherein the reactants have a partial pressure such that not more than one monolayer forms for each of the reactants on a surface of the catalyst material.

111. The method of claim 102, wherein at least one of the reactants is gaseous.

112. The method of claim 102, wherein the method further includes:

modifying one or more electron density of the catalytic collector to a selected range of energy

GF Exhibit 1124 - 2328/2704

transitions of one or more excitation band structures of an adsorbate-catalyst system having the reactants.

113. The method of claim 112, wherein the modifying includes forming one or more catalyst monolayers.

114. The method of claim 112, wherein the modifying includes forming one or more ordered electron-reflective structures on the surface exposed to the reactants.

115. The method of claim 112, wherein the modifying includes forming one or more ordered hole-reflective structures on the surface exposed to the reactants.

116. The method of claim 112, wherein the modifying includes forming one or more hot electron Fabry-Perot modes of a thin-film electron interferometer.

117. The method of claim 112, wherein the modifying includes forming one or more catalyst metal monolayers.

118. The method of claim 112, wherein the modifying includes forming one to one hundred catalyst metal monolayers.

119. The method of claim 112, wherein the modifying includes forming one or more integer catalyst metal monolayers.

120. The method of claim 112, wherein the modifying includes forming one or more electron interferometer structures to cause a plurality of electron path reflections.

GF Exhibit 1124 - 2329/2704

121. The method of claim 102, wherein the method further includes adding one or more expendable additives to the reactants.

122. The method of claim 121, wherein the expendable additives include one or more catalyst materials.

123. The method of claim 121, wherein the expendable additives include one or more reaction accelerator materials.

124. The method of claim 121, wherein the expendable additives include one or more reaction decelerator materials.

125. The method of claim 102, wherein the reactants include hydrocarbon chains.

126. The method of claim 102, wherein the reactants deposit one or more compounds on the catalytic collector.

127. The method of claim 102, wherein the reactants include one or more compounds that form the catalytic collector.

128. The method of claim 102, wherein reaction stimulated by the hot carriers cause a surface explosion.

129. The method of claim 102, wherein reaction stimulated by the hot carriers cause an autocatalyzed chain reaction.

GF Exhibit 1124 - 2330/2704

130. The method of claim 102, further including cooling the diode with heat of vaporization of the reactants.

131. A solid state surface catalysis excitation transfer reaction apparatus comprising:

a catalytic collector; and

an excitation emitter whose excitation band structure is coupled to excitation band structure associated with the catalytic collector,

wherein an energy applied to the excitation emitter creates one or more emitter excitations, the emitter excitations transported to reactants in the catalytic collector where the transported emitter excitations energize excitations in the catalytic collector, the excitations stimulating reactions.

132. The apparatus as claimed in claim 140, wherein the emitter excitations include minority carriers.

133. The apparatus as claimed in claim 140, wherein the emitter excitations include hot carriers.

134. A solid state surface catalysis excitation transfer reaction apparatus comprising:

a catalytic collector; and

an excitation emitter whose excitation band structure is coupled to excitation band structure associated with the catalytic collector,

wherein one or more pulses of excitation associated with reactions of adsorbates occurring in the catalytic collector are converted into one or more second excitations and transported to the excitation emitter where emitter excitations are generated and converted into one or more forms of energy.

GF Exhibit 1124 - 2331/2704

135. The apparatus of claim 143, wherein the reactants include gaseous reactants.

136. The apparatus of claim 143, wherein the pulses of excitation include excited reactant molecular vibrations.

137. The apparatus of claim 143, wherein the reactions of adsorbates occur on a surface of the catalytic collector.

138. The apparatus of claim 143, wherein the reactions of adsorbates occur with a surface of the catalytic collector.

139. The apparatus of claim 143, wherein the emitter excitations include hot carriers.

140. The apparatus of claim 143, wherein the emitter excitations include minority carriers.

141. The apparatus of claim 149, wherein the one or more second excitations include hot carriers.

142. The apparatus as claimed in claim 1, wherein the emitter excitations include energies transported by resonant tunneling.

143. The apparatus as claimed in claim 1, wherein the catalytic collector further includes a catalyst, a material of the catalyst and an electrode of the p-n junction diode being one and the same.

144. The method of claim 70, wherein a hot carrier is an electron and the excitation band of the emitter is its conduction band.

GF Exhibit 1124 - 2332/2704

145. The method of claim 70, wherein a hot carrier is a hole and the excitation band of the emitter is its valence band.

146. The method of claim 72, wherein the method further includes:

modifying one or more electron density of states of a material in a catalytic collector to match a selected excitation band structure of an adsorbate-catalyst system having the adsorbate reactants.

147. The method of claim 78, wherein the modifying includes forming one or more electron interferometer structures to cause a plurality of hole reflections.

148. A method of stimulating reactions, comprising:

applying power to a diode in an excitation emitter, the excitation emitter being in contact with a catalytic collector;

creating hot carriers in the excitation emitter;

coupling excitation energy of the hot carriers to an excitation band structure of the catalytic collector by using resonant tunneling;

constraining the thickness properties of a coupling material of the catalytic collector such that the resonant tunneling of the excitation energy experiences an energy transfer rate between excitation emitter and catalytic collector not less than 3% of the competing, energy loss rates.

149. The method of claim 157, wherein the constraining the thickness properties includes constraining the thickness to less than 200 nanometre (nm) for a conducting coupling material of the catalytic collector.

GF Exhibit 1124 - 2333/2704

150. The method of claim 157, wherein the constraining the thickness properties includes constraining the thickness to less than 100,000 nanometre (nm) for a non-conducting coupling material of the catalytic collector.

GF Exhibit 1124 - 2334/2704

AMENDED CLAIMS
(received by the International Bureau on 23 March 2001 (23.03.01);
original claims 130-150 replaced by new claims 130-150;
remaining claims unchanged (4 pages))

130. The method of claim 102, further including cooling the diode with heat of vaporization of the reactants.

131. A solid state surface catalysis excitation transfer reaction apparatus comprising:

a catalytic collector; and

an excitation emitter whose excitation band structure is coupled to excitation band structure associated with the catalytic collector,

wherein an energy applied to the excitation emitter creates one or more emitter excitations, the emitter excitations transported to reactants in the catalytic collector where the transported emitter excitations energize excitations in the catalytic collector, the excitations stimulating reactions.

132. The apparatus as claimed in claim 131, wherein the emitter excitations include minority carriers.

133. The apparatus as claimed in claim 131, wherein the emitter excitations include hot carriers.

134. A solid state surface catalysis excitation transfer reaction apparatus comprising:

a catalytic collector; and

an excitation emitter whose excitation band structure is coupled to excitation band structure associated with the catalytic collector,

wherein one or more pulses of excitation associated with reactions of adsorbates occurring in the catalytic collector are converted into one or more second excitations and transported to the excitation emitter where emitter excitations are generated and converted into one or more forms of energy.

GF Exhibit 1124 - 2335/2704

135. The apparatus of claim 134, wherein the reactants include gaseous reactants.

136. The apparatus of claim 134, wherein the pulses of excitation include excited reactant molecular vibrations.

137. The apparatus of claim 134, wherein the reactions of adsorbates occur on a surface of the catalytic collector.

138. The apparatus of claim 134, wherein the reactions of adsorbates occur with a surface of the catalytic collector.

139. The apparatus of claim 134, wherein the emitter excitations include hot carriers.

140. The apparatus of claim 134, wherein the emitter excitations include minority carriers.

141. The apparatus of claim 140, wherein the one or more second excitations include hot carriers.

142. The apparatus as claimed in claim 1, wherein the emitter excitations include energies transported by resonant tunneling.

143. The apparatus as claimed in claim 1, wherein the catalytic collector further includes a catalyst, a material of the catalyst and an electrode of the p-n junction diode being one and the same.

GF Exhibit 1124 - 2336/2704

144. The method of claim 70, wherein a hot carrier is an electron and the excitation band of the emitter is its conduction band.

145. The method of claim 70, wherein a hot carrier is a hole and the excitation band of the emitter is its valence band.

146. The method of claim 72, wherein the method further includes:

modifying one or more electron density of states of a material in a catalytic collector to match a selected excitation band structure of an adsorbate-catalyst system having the adsorbate reactants.

147. The method of claim 78, wherein the modifying includes forming one or more electron interferometer structures to cause a plurality of hole reflections.

148. A method of stimulating reactions, comprising:

applying power to a diode in an excitation emitter, the excitation emitter being in contact with a catalytic collector;

creating hot carriers in the excitation emitter;

GF Exhibit 1124 - 2337/2704

coupling excitation energy of the hot carriers to an excitation band structure of the catalytic collector by using resonant tunneling;

constraining the thickness properties of a coupling material of the catalytic collector such that the resonant tunneling of the excitation energy experiences an energy transfer rate between excitation emitter and catalytic collector not less than 3% of the competing, energy loss rates.

149. The method of claim 148, wherein the constraining the thickness properties includes constraining the thickness to less than 200 nanometre (nm) for a conducting coupling material of the catalytic collector.

150. The method of claim 148, wherein the constraining the thickness properties includes constraining the thickness to less than 100,000 nanometre (nm) for a non-conducting coupling material of the catalytic collector.

GF Exhibit 1124 - 2338/2704

FIG. 1

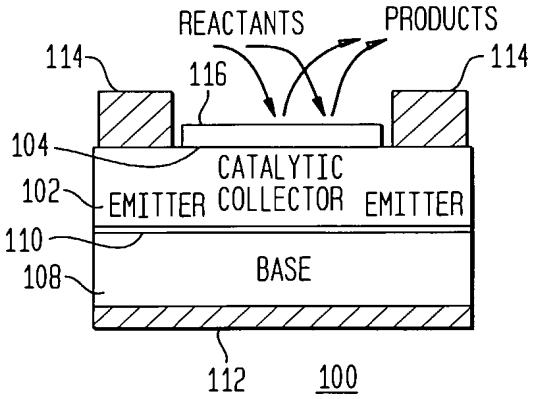
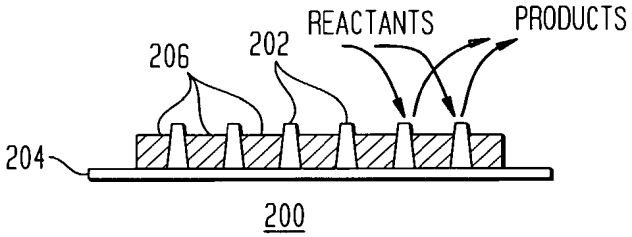


FIG. 2



GF Exhibit 1124 - 2339/2704

FIG. 3

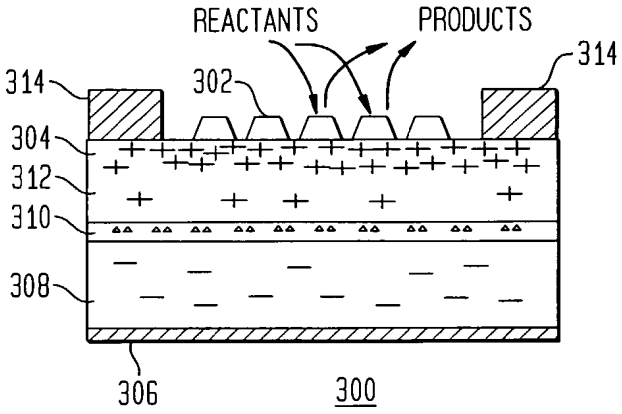
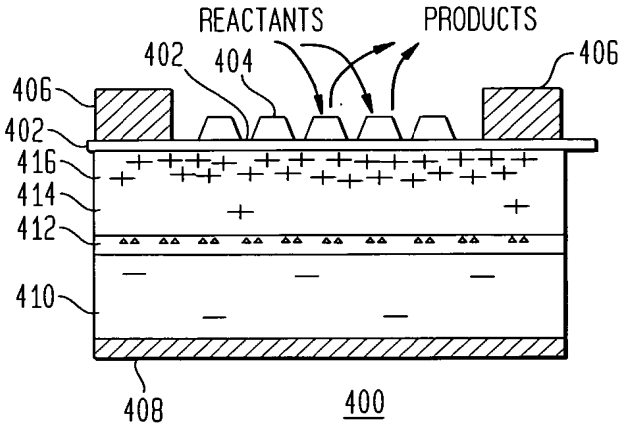


FIG. 4



GF Exhibit 1124 - 2340/2704

FIG. 5

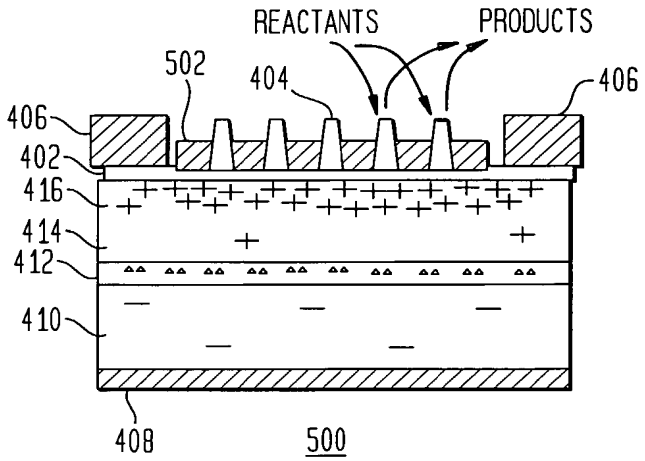
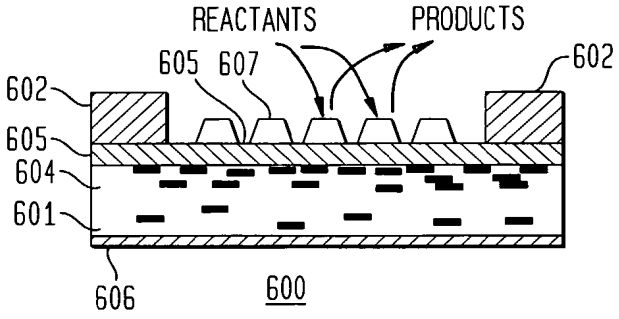
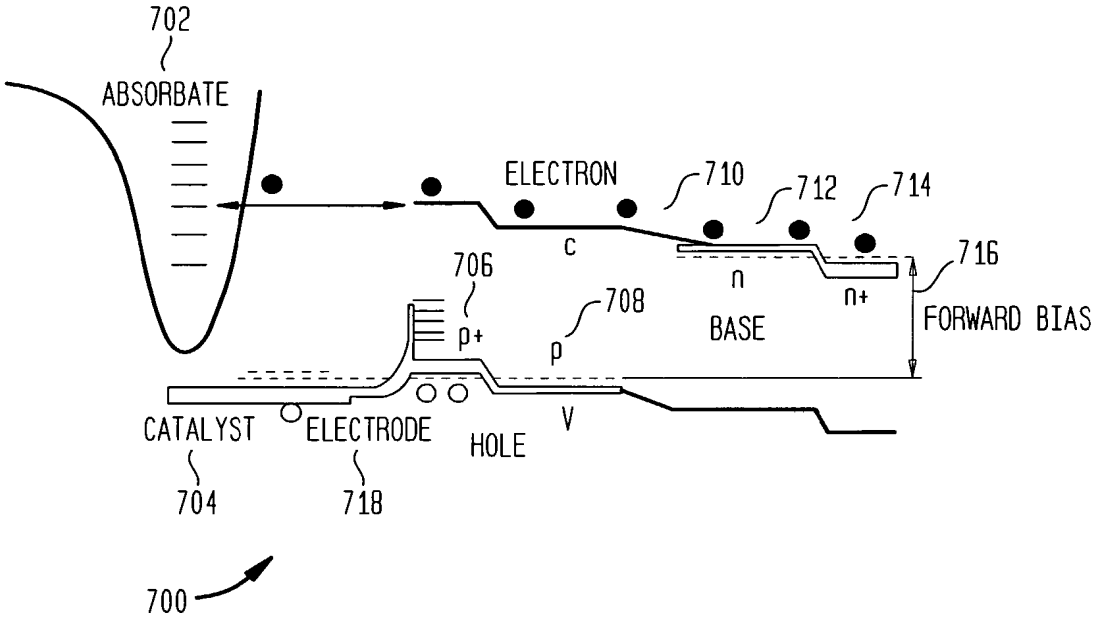


FIG. 6



GF Exhibit 1124 - 2341/2704

FIG. 7



GF Exhibit 1124 - 2342/2704

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/28801

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :B01J 19/08
US CL :422/186, 186.04; 204/164; 136/253, 254
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 422/186, 186.04; 204/164; 136/253, 254

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WEST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A,P	US 6,114,620 A (ZUPPERO et al.) 05 September 2000.	1-159

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 16 JANUARY 2001	Date of mailing of the international search report 06 FEB 2001
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer KISHOR MAYEKAR DEBORAH THOMAS PARALEGAL SPECIALIST Telephone No. (703) 308-0661

Form PCT/ISA/210 (second sheet) (July 1998)★

GF Exhibit 1124 - 2343/2704

(12) DEMANDE INTERNATIONALE PUBLIÉE EN VERTU DU TRAITÉ DE COOPÉRATION EN MATIÈRE DE BREVETS (PCT)

(19) Organisation Mondiale de la Propriété Intellectuelle
Bureau international

(43) Date de la publication internationale
30 août 2001 (30.08.2001)

PCT

(10) Numéro de publication internationale
WO 01/63677 A1

(51) Classification internationale des brevets[7] : H01L 29/78

(21) Numéro de la demande internationale :
PCT/FR01/00532

(22) Date de dépôt international :
23 février 2001 (23.02.2001)

(25) Langue de dépôt : français

(26) Langue de publication : français

(30) Données relatives à la priorité :
00/02237 23 février 2000 (23.02.2000) FR

(71) Déposant *(pour tous les États désignés sauf US)* : **CENTRE NATIONAL DE LA RECHERCHE SCIENTIFIQUE** [FR/FR]; 3, rue Michel-Ange, F-75794 Paris Cedex 16 (FR).

(72) Inventeur; et

(75) Inventeur/Déposant *(pour US seulement)* : **DUBOIS, Emmanuel** [FR/FR]; 13, allée du bel air, F-59890 Quesnoy sur Deule (FR).

(74) Mandataire : **LEHU, Jean**; c/o Brevatome, 3, rue du Docteur Lancereaux, F-75008 Paris (FR).

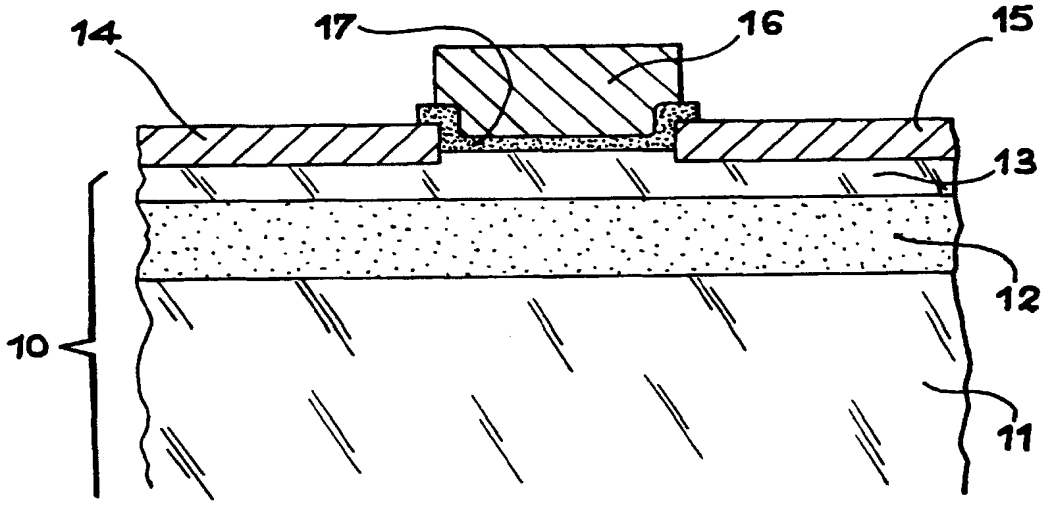
(81) États désignés *(national)* : AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) États désignés *(régional)* : brevet ARIPO (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), brevet eurasien (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), brevet européen (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU,

[Suite sur la page suivante]

(54) Title: MOS TRANSISTOR FOR HIGH DENSITY INTEGRATION CIRCUITS

(54) Titre : TRANSISTOR MOS POUR CIRCUITS A HAUTE DENSITE D'INTEGRATION



(57) Abstract: The invention concerns a MOS transistor produced in a silicon film of a SOI substrate (10), said film (13) being lightly doped and having a thickness less than 30 nm, the source (14) and drain (15) contacts being of the Schottky type with the lowest possible Schottky barrier height for the majority carriers, the operating conditions of the transistor being of the accumulative type.

(57) Abrégé : L'invention concerne un transistor MOS réalisé dans la couche mince de silicium d'un substrat SOI (10), ladite couche mince (13) étant faiblement dopée et ayant une épaisseur inférieure à 30 nm, les contacts de source (14) et de drain (15) étant du type Schottky à hauteur de barrière Schottky la plus faible possible pour les porteurs majoritaires, le régime de fonctionnement du transistor étant du type accumulation.

WO 01/63677 A1

GF Exhibit 1124 - 2344/2704

MC, NL, PT, SE, TR), brevet OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Publiée :

— *avec rapport de recherche internationale*

En ce qui concerne les codes à deux lettres et autres abréviations, se référer aux "Notes explicatives relatives aux codes et abréviations" figurant au début de chaque numéro ordinaire de la Gazette du PCT.

GF Exhibit 1124 - 2345/2704

TRANSISTOR MOS POUR CIRCUITS A HAUTE DENSITE D'INTEGRATION

DOMAINE TECHNIQUE

La présente invention concerne un transistor MOS utilisable pour réaliser des circuits à haute densité d'intégration.

ÉTAT DE LA TECHNIQUE ANTÉRIEURE

La figure 1 représente, de manière schématique, la structure d'un transistor MOS conventionnel. Il s'agit d'un transistor MOS à canal n. Il est réalisé sur un substrat massif 1 en silicium de type p. Deux régions 2 et 3 de type n^+ sont créées, par exemple par implantation ionique, pour former respectivement la source et le drain du transistor. La référence 4 désigne la couche d'oxyde de grille fabriquée sur la surface du substrat 1 et sous laquelle débordent les régions 2 et 3. Une électrode de grille 5 est déposée sur la couche d'oxyde de grille 4. Des électrodes de source 6 et de drain 7 sont réalisées respectivement sur les régions 2 et 3 et le transistor est isolé des dispositifs adjacents par une couche d'oxyde 8. On a représenté également le canal 9 qui se forme sous la couche d'oxyde de grille 4 lorsque le transistor est convenablement polarisé. Sur la figure sont indiqués les paramètres importants suivants :

- longueur de canal L,
- épaisseur de la couche d'oxyde de grille d,
- profondeur de jonction r_j.

L'intérêt soutenu pour le développement de technologies silicium à haute densité d'intégration, hautes fréquences et faible consommation est largement

GF Exhibit 1124 - 2346/2704

motivé par de nouvelles exigences de portabilité, en particulier pour les télécommunications et équipements informatiques. L'accroissement exponentiel des performances techniques (conformément à la loi de Moore) et économiques de la microélectronique sur silicium est révélateur de la plus formidable évolution industrielle du vingtième siècle.

L'utilisation massive du transistor MOSFET dans la fabrication des circuits intégrés a permis d'augmenter notablement la densité d'intégration. Cependant, l'accroissement soutenu en densité d'intégration et performances électroniques risque de se heurter aux limites physiques de fabrication. En première approximation, il est reconnu qu'une réduction d'un facteur α de la longueur de grille d'un transistor MOSFET doit être accompagnée d'une réduction simultanée d'un facteur α de l'ensemble des autres dimensions caractéristiques (épaisseur d'oxyde de grille, largeur de canal, profondeur de jonction), d'une réduction d'un facteur α de la tension d'alimentation et d'un accroissement d'un facteur α de la concentration en dopant dans le canal.

Il est actuellement possible d'obtenir une dimension minimale de grille de 22 nm. Cependant, une telle réduction implique des modifications d'autres dimensions caractéristiques du transistor qu'il est impossible de réaliser actuellement ni même dans un avenir proche d'après "The International Technology Roadmap for Semiconductors-ITRS", 1999, SIA Semiconductor Industry Association.

Les verrous technologiques qui empêchent la réalisation d'un transistor MOS conventionnel à longueur de grille de 22 nm sont notamment les suivants :

GF Exhibit 1124 - 2347/2704

- I : une très faible profondeur des extensions de source et de drain à leur jonction avec le canal (de 8 à 13 nm) ;

- II : un gradient de concentration extrêmement abrupt aux jonctions source-canal et drain-canal (0,5 nm/déc.) ;

- III : une très faible épaisseur de silicium (12 nm) ;

- IV : une consommation réduite du silicium lors de la réaction de siliciuration (de 7 à 17 nm) ;

- V : une faible résistance par carré du siliciure compte tenu de son épaisseur réduite (12,5 Ω/ pour une épaisseur de siliciure de 12 nm) ;

- VI : une très faible résistance spécifique de contact de source et de drain à l'interface siliciure-silicium (inférieure à $1,5 \cdot 10^{-8}\ \Omega \cdot cm^2$) ;

- VII : un très fort niveau de dopage dans le canal ($3 \cdot 10^{19}\ cm^{-3}$).

La miniaturisation des dispositifs MOS requiert la formation de jonctions de plus en plus courtes, ce qui rend extrêmement difficile l'optimisation de la résistance spécifique de contact. La réduction de cette résistance est en général obtenue par un procédé de siliciuration permettant d'obtenir un alliage qui assure une faible résistance de l'interface siliciure/silicium, par exemple des interfaces $TiSi_2$/Si, $CoSi_2$/Si. Cependant, la réaction de siliciuration induit une consommation de silicium qui peut mener d'une part à une diminution de la surface effective de contact et, d'autre part, à une augmentation de la résistance spécifique de contact dans la mesure où l'interface siliciure/silicium intervient à des valeurs de dopage trop faibles.

GF Exhibit 1124 - 2348/2704

L'article "Proposal of a Schottky-Barrier SET Aiming at a Future Integrated Device" de M. FUJISHIMA et al., paru dans IEICE Transactions on Electronics, JP, Institute of Electronics Information and Comm. Eng. Tokyo, vol. E 80-C, n°7, 1er juillet 1997, pages 881 à 885, divulgue un transistor MOS à un électron. Ce dispositif exploite le phénomène de Coulomb, à savoir un effet de quantification de charge permettant d'obtenir des oscillations de courant en fonction de la tension de grille appliquée. Plusieurs contraintes lui sont alors imposées. Le transistor doit fonctionner à basse température (par exemple 10 K) afin que la quantification de charge ne soit pas masquée par les fluctuations thermiques de charge. Il est formé d'un canal de silicium connecté à l'extérieur (contacts source/drain) par l'intermédiaire de barrières Schottky faisant office de barrière tunnel. Afin de pouvoir exploiter le phénomène de blocage de Coulomb, la résistance tunnel des barrières Schottky doit être supérieure au quantum de résistance. Cette contrainte justifie l'emploi de barrières Schottky relativement hautes. Enfin, le dispositif décrit dans cet article est un fil quantique sur silicium non dopé, ce qui implique une largeur de dispositif très réduite. Cette largeur très faible est indispensable pour le fonctionnement du transistor SET afin de réduire l'ensemble des capacités entre les contacts terminaux du transistor et le canal de silicium, le blocage de Coulomb ne pouvant être obtenu qu'au prix de capacités très faibles. La largeur très faible du dispositif permet d'obtenir une résistance tunnel des jonctions assez grande puisque la résistance est inversement proportionnelle à la surface d'émission.

GF Exhibit 1124 - 2349/2704

EXPOSÉ DE L'INVENTION

La présente invention permet de remédier aux problèmes de réalisation de transistors MOS pour circuits à haute densité d'intégration.

Elle a pour objet un transistor MOS réalisé dans la couche mince de silicium d'un substrat SOI, ladite couche mince étant faiblement dopée et ayant une épaisseur inférieure à 30 nm, les contacts de source et de drain étant du type Schottky à hauteur de barrière Schottky la plus faible possible pour les porteurs majoritaires, le régime de fonctionnement du transistor étant du type accumulation.

De préférence, le taux de dopage de la couche mince est compris entre $5 . 10^{14}$ cm^{-3} et 10^{17} cm^{-3}. Avantageusement, il est de l'ordre de 10^{15} cm^{-3}, par exemple 1 ou $2. 10^{15}$ cm^{-3}.

Si la couche mince est dopée p, pour obtenir un p-MOSFET, les contacts de source et de drain sont avantageusement constitués par un siliciure PtGeSi. Un recuit, par exemple à une température de l'ordre de 600°C pendant environ 10 minutes, permet d'abaisser la hauteur de barrière Schottky de ces contacts.

Si la couche mince est dopée n pour obtenir un n-MOSFET, les contacts de source et de drain peuvent être constitués par un siliciure à base d'erbium.

BRÈVE DESCRIPTION DES DESSINS

L'invention sera mieux comprise et d'autres avantages et particularités apparaîtront à la lecture de la description qui va suivre, donnée à titre d'exemple non limitatif, accompagnée des dessins annexés parmi lesquels :

GF Exhibit 1124 - 2350/2704

- la figure 1, déjà décrite, représente de manière schématique, la structure d'un transistor MOS de l'art connu, réalisé sur un substrat massif de silicium,

- la figure 2 représente, de manière schématique, la structure d'un transistor MOS selon la présente invention.

EXPOSÉ DÉTAILLÉ DE MODES DE RÉALISATION DE L'INVENTION

La figure 2 représente de manière schématique, la structure d'un transistor MOS selon la présente invention. Ce transistor est réalisé sur un substrat SOI 10 formé d'une plaquette de silicium 11 recouverte successivement d'une couche de dioxyde de silicium 12 et d'une couche mince de silicium 13.

La couche mince 13, ou couche active, possède une épaisseur inférieure à 30 nm, typiquement entre 5 et 20 nm. Cette couche est faiblement dopée, par exemple de l'ordre de 10^{15} cm^{-3}. Le dopage est de type n pour un n-MOSFET et de type p pour un p-MOSFET.

Le transistor comprend des contacts de source 14 et de drain 15 du type Schottky et une grille 16 isolée électriquement du reste de la structure par une couche d'isolant de grille 17 par exemple en dioxyde de silicium.

Le principe de fonctionnement est celui d'un transistor MOS à accumulation. Les porteurs qui constituent le canal sont les porteurs majoritaires du substrat, c'est-à-dire les trous pour un transistor p-MOS sur substrat SOI de type p et les électrons pour un transistor n-MOS sur substrat SOI de type n. Le canal de conduction qui s'établit entre les contacts de source et de drain est contrôlé par la tension appliquée sur la grille. Le dispositif est mis en

GF Exhibit 1124 - 2351/2704

conduction par une tension de grille négative par rapport à la tension de source pour un transistor de type p-MOS et pour une tension de grille positive par rapport à la tension de source pour un transistor de type n-MOS. La hauteur de barrière Schottky doit être aussi faible que possible pour les porteurs majoritaires et idéalement égale à 0 eV.

La réalisation des zones de source et de drain par des contacts Schottky directement sur la couche mince de silicium permet de parer aux verrous technologiques I et II cités plus haut.

L'épaisseur de siliciure et la consommation correspondante de silicium durant la réaction de siliciuration n'étant pas limitée, ceci permet de parer aux verrous technologiques III, IV et V.

On obvie au verrou technologique VI en choisissant une hauteur de barrière Schottky très faible pour les contacts de source et de drain. Dans le cas d'un transistor p-MOS, il est possible d'obtenir une hauteur de barrière de l'ordre de 0,05 eV, soit une résistivité de l'ordre de $6.10^{-9}\ \Omega\ .\ cm^2$, par dépôt de platine ou d'un alliage germanium-platine suivi d'un recuit thermique. Dans le cas d'un transistor n-MOS, un siliciure à base d'erbium pourrait donner une hauteur de barrière inférieure à 0,2 eV.

L'utilisation d'une couche mince de silicium peu dopée, par exemple de l'ordre de $10^{15}\ cm^{-3}$, pour le substrat SOI permet de parer au verrou technologique VII.

Dans le cas d'un transistor p-MOS, réalisé sur une couche mince faiblement dopée (de l'ordre de $10^{15}\ cm^{-3}$), les contacts de source et de drain peuvent être obtenus de la manière suivante. Un dépôt de germanium est réalisé par évaporation sous ultra-vide. Un dépôt de platine est ensuite réalisé par le même

GF Exhibit 1124 - 2352/2704

procédé. On procède ensuite à un recuit vers 600°C pendant une période typique de 10 minutes. Les contacts obtenus présentent une très faible hauteur de barrière (environ 0,05 eV). La résistance spécifique de contact obtenue est alors de l'ordre de $6 . 10^{-9}$ $\Omega . cm^2$ à 10^{-8} $\Omega . cm^2$.

Les contacts Schottky de source et de drain peuvent être réalisés avant la formation de la grille. En variante, il est possible de réaliser d'abord l'oxyde de grille et de déposer ensuite le matériau de grille. La grille et le canal auto-aligné sont alors définis par gravure. Le dépôt des contacts de source et de drain n'intervient qu'ultérieurement par auto-alignement après réaction de siliciuration.

GF Exhibit 1124 - 2353/2704

REVENDICATIONS

1. Transistor MOS réalisé dans la couche mince de silicium d'un substrat SOI (10), ladite couche mince (13) étant faiblement dopée et ayant une épaisseur inférieure à 30 nm, les contacts de source (14) et de drain (15) étant du type Schottky à hauteur de barrière Schottky inférieure à 0,2 eV pour les porteurs majoritaires, le régime de fonctionnement du transistor étant du type accumulation.

2. Transistor MOS selon la revendication 1, caractérisé en ce que le taux de dopage de ladite couche mince (13) est compris entre $5 . 10^{14}$ cm^{-3} et 10^{17} cm^{-3}.

3. Transistor MOS selon la revendication 2, caractérisé en ce que le taux de dopage de ladite couche mince (13) est de l'ordre de 10^{15} cm^{-3}.

4. Transistor MOS selon l'une quelconque des revendications 1 à 3, caractérisé en ce que, ladite couche mince (13) étant dopée p, les contacts de source (14) et de drain (15) sont constitués par un siliciure PtGeSi.

5. Transistor MOS selon la revendication 4, caractérisé en ce que les contacts de source (14) et de drain (15) sont constitués par un siliciure PtGeSi recuit à une température de l'ordre de 600°C pendant environ 10 minutes.

6. Transistor MOS selon l'une quelconque des revendications 1 à 3, caractérisé en ce que, ladite couche mince (13) étant dopée n, les contacts de source (14) et de drain (15) sont constitués par un siliciure à base d'erbium.

GF Exhibit 1124 - 2354/2704

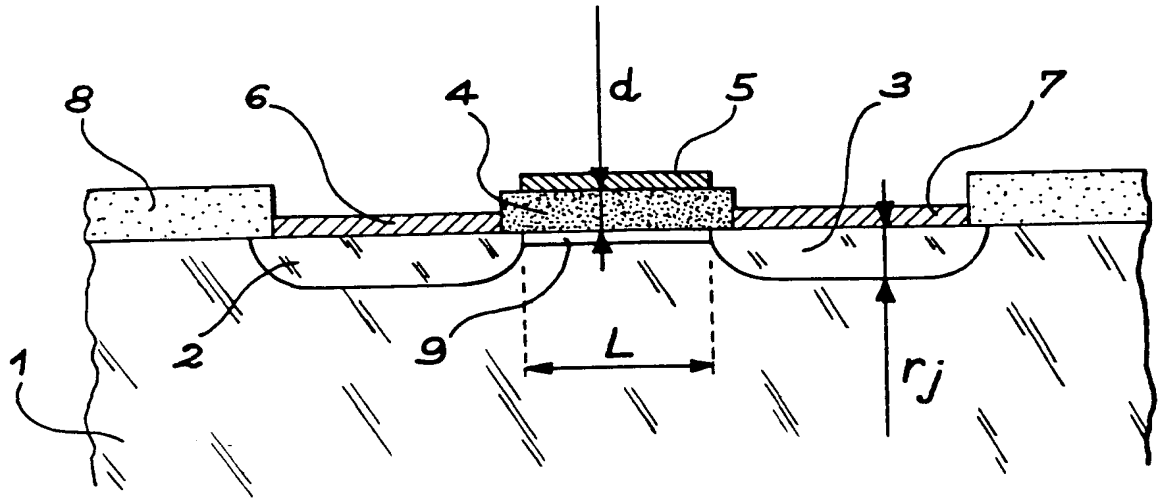


FIG. 1

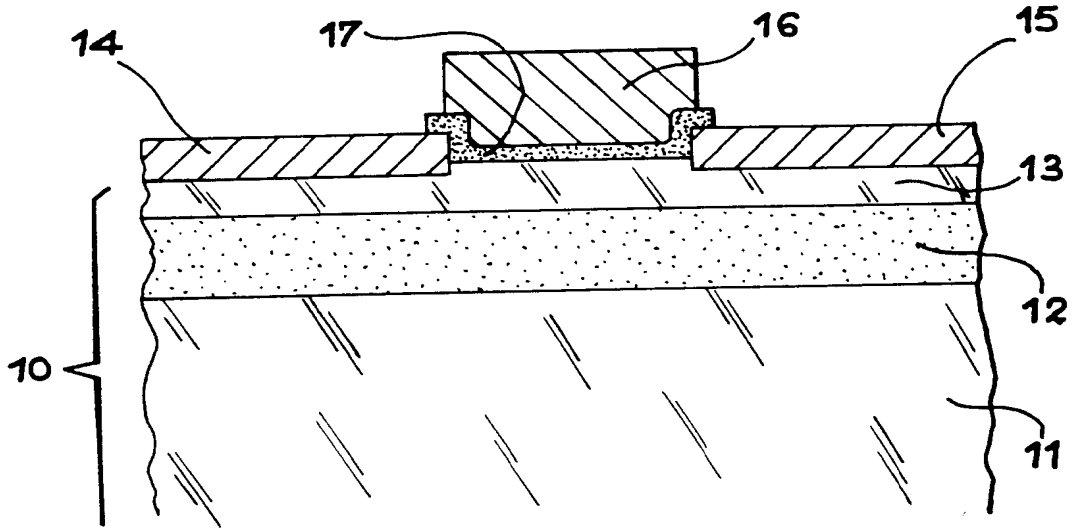


FIG. 2

INTERNATIONAL SEARCH REPORT

ernational Application No
PCT/FR 01/00532

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/78

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	FUJISHIMA M ET AL: "PROPOSAL OF A SCHOTTKY-BARRIER SET AIMING AT A FUTURE INTEGRATED DEVICE" IEICE TRANSACTIONS ON ELECTRONICS,JP,INSTITUTE OF ELECTRONICS INFORMATION AND COMM. ENG. TOKYO, vol. E 80-C, no. 7, 1 July 1997 (1997-07-01), pages 881-885, XP000740316 ISSN: 0916-8524	1-3
Y	page 883; figure 4 ---	4,6
Y	EP 0 469 611 A (HITACHI LTD) 5 February 1992 (1992-02-05)	4
A	column 11, line 24 -column 12, line 22; figures 8,10,11 ---	5
	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
3 May 2001	11/05/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Juhl, A

1

Form PCT/ISA/210 (second sheet) (July 1992)

GF Exhibit 1124 - 2356/2704

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 140 381 A (BADOZ PIERRE A ET AL) 18 August 1992 (1992-08-18) column 4, line 58 - line 66	6
A	NISHISAKA M ET AL: "REDUCTION OF THE FLOATING-BODY EFFECT IN SOI MOSFETS BY USING SCHOTTKY SOURCE/DRAIN CONTACTS" INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS,JA,JAPAN SOCIETY OF APPLIED PHYSICS. TOKYO, 1 September 1997 (1997-09-01), pages 160-161, XP000728068 page 160; figure 1	2,3
A	WANG P J: MATERIAL RESEARCH SYMPOSIUM PROCEEDINGS, vol. 260, 1992, pages 863-868, XP000900684 page 863	4,5
A	WANG C ET AL: "SUB-40 NM PTSI SCHOTTKY SOURCE/DRAIN METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTORS" APPLIED PHYSICS LETTERS,US,AMERICAN INSTITUTE OF PHYSICS. NEW YORK, vol. 74, no. 8, 22 February 1999 (1999-02-22), pages 1174-1176, XP000805877 ISSN: 0003-6951 page 1174	1
A	EP 0 456 059 A (NIPPON ELECTRIC CO) 13 November 1991 (1991-11-13) column 3, line 24 - line 51; figure 1 column 5, line 49 - line 54	1
A	KIMURA M: "A NEW TYPE MOS-GATED TUNNEL TRANSISTOR WITH A SCHOTTKY BARRIER" IEEE REGION TEN INTERNATIONAL CONFERENCE ON MICROELECTRONICS AND VLSI.(TENCON),US,NEW YORK, IEEE, 6 November 1995 (1995-11-06), pages 387-390, XP000585809 ISBN: 0-7803-2625-3 page 387, paragraph II	1

1

GF Exhibit 1124 - 2357/2704

INTERNATIONAL SEARCH REPORT

Information on patent family members

ernational Application No
PCT/FR 01/00532

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0469611 A	05-02-1992	JP 3039967 B	08-05-2000
		JP 4091480 A	24-03-1992
		DE 69108631 D	11-05-1995
		DE 69108631 T	04-01-1996
		KR 189691 B	01-06-1999
		US 5177568 A	05-01-1993
US 5140381 A	18-08-1992	FR 2660114 A	27-09-1991
		DE 69119809 D	04-07-1996
		DE 69119809 T	02-01-1997
		EP 0448465 A	25-09-1991
		JP 5322646 A	07-12-1993
EP 0456059 A	13-11-1991	DE 69121629 D	02-10-1996
		DE 69121629 T	13-02-1997
		JP 2751658 B	18-05-1998
		JP 4226081 A	14-08-1992
		US 5159416 A	27-10-1992

GF Exhibit 1124 - 2358/2704

RAPPORT DE RECHERCHE INTERNATIONALE

nande Internationale No
PCT/FR 01/00532

A. CLASSEMENT DE L'OBJET DE LA DEMANDE
CIB 7 H01L29/78

Selon la classification internationale des brevets (CIB) ou à la fois selon la classification nationale et la CIB

B. DOMAINES SUR LESQUELS LA RECHERCHE A PORTE

Documentation minimale consultée (système de classification suivi des symboles de classement)
CIB 7 H01L

Documentation consultée autre que la documentation minimale dans la mesure où ces documents relèvent des domaines sur lesquels a porté la recherche

Base de données électronique consultée au cours de la recherche internationale (nom de la base de données, et si réalisable, termes de recherche utilisés)
EPO-Internal, PAJ, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERES COMME PERTINENTS

Catégorie °	Identification des documents cités, avec, le cas échéant, l'indication des passages pertinents	no. des revendications visées
X	FUJISHIMA M ET AL: "PROPOSAL OF A SCHOTTKY-BARRIER SET AIMING AT A FUTURE INTEGRATED DEVICE" IEICE TRANSACTIONS ON ELECTRONICS,JP,INSTITUTE OF ELECTRONICS INFORMATION AND COMM. ENG. TOKYO, vol. E 80-C, no. 7, 1 juillet 1997 (1997-07-01), pages 881-885, XP000740316 ISSN: 0916-8524	1-3
Y	page 883; figure 4 ---	4,6
Y	EP 0 469 611 A (HITACHI LTD) 5 février 1992 (1992-02-05)	4
A	colonne 11, ligne 24 -colonne 12, ligne 22; figures 8,10,11 ---	5
	-/--	

[X] Voir la suite du cadre C pour la fin de la liste des documents

[X] Les documents de familles de brevets sont indiqués en annexe

° Catégories spéciales de documents cités:

"A" document définissant l'état général de la technique, non considéré comme particulièrement pertinent

"E" document antérieur, mais publié à la date de dépôt international ou après cette date

"L" document pouvant jeter un doute sur une revendication de priorité ou cité pour déterminer la date de publication d'une autre citation ou pour une raison spéciale (telle qu'indiquée)

"O" document se référant à une divulgation orale, à un usage, à une exposition ou tous autres moyens

"P" document publié avant la date de dépôt international, mais postérieurement à la date de priorité revendiquée

"T" document ultérieur publié après la date de dépôt international ou la date de priorité et n'appartenenant pas à l'état de la technique pertinent, mais cité pour comprendre le principe ou la théorie constituant la base de l'invention

"X" document particulièrement pertinent; l'inven tion revendiquée ne peut être considérée comme nouvelle ou comme impliquant une activité inventive par rapport au document considéré isolément

"Y" document particulièrement pertinent; l'inven tion revendiquée ne peut être considérée comme impliquant une activité inventive lorsque le document est associé à un ou plusieurs autres documents de même nature, cette combinaison étant évidente pour une personne du métier

"&" document qui fait partie de la même famille de brevets

Date à laquelle la recherche internationale a été effectivement achevée	Date d'expédition du présent rapport de recherche internationale
3 mai 2001	11/05/2001

Nom et adresse postale de l'administration chargée de la recherche internationale	Fonctionnaire autorisé
Office Européen des Brevets, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Juhl, A

1

Formulaire PCT/ISA/210 (deuxième feuille) (juillet 1992)

GF Exhibit 1124 - 2359/2704

C.(suite) DOCUMENTS CONSIDERES COMME PERTINENTS

Catégorie °	Identification des documents cités, avec,le cas échéant, l'indicationdes passages pertinents	no. des revendications visées
Y	US 5 140 381 A (BADOZ PIERRE A ET AL) 18 août 1992 (1992-08-18) colonne 4, ligne 58 - ligne 66	6
A	NISHISAKA M ET AL: "REDUCTION OF THE FLOATING-BODY EFFECT IN SOI MOSFETS BY USING SCHOTTKY SOURCE/DRAIN CONTACTS" INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS,JA,JAPAN SOCIETY OF APPLIED PHYSICS. TOKYO, 1 septembre 1997 (1997-09-01), pages 160-161, XP000728068 page 160; figure 1	2,3
A	WANG P J: MATERIAL RESEARCH SYMPOSIUM PROCEEDINGS, vol. 260, 1992, pages 863-868, XP000900684 page 863	4,5
A	WANG C ET AL: "SUB-40 NM PTSI SCHOTTKY SOURCE/DRAIN METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTORS" APPLIED PHYSICS LETTERS,US,AMERICAN INSTITUTE OF PHYSICS. NEW YORK, vol. 74, no. 8, 22 février 1999 (1999-02-22), pages 1174-1176, XP000805877 ISSN: 0003-6951 page 1174	1
A	EP 0 456 059 A (NIPPON ELECTRIC CO) 13 novembre 1991 (1991-11-13) colonne 3, ligne 24 - ligne 51; figure 1 colonne 5, ligne 49 - ligne 54	1
A	KIMURA M: "A NEW TYPE MOS-GATED TUNNEL TRANSISTOR WITH A SCHOTTKY BARRIER" IEEE REGION TEN INTERNATIONAL CONFERENCE ON MICROELECTRONICS AND VLSI.(TENCON),US,NEW YORK, IEEE, 6 novembre 1995 (1995-11-06), pages 387-390, XP000585809 ISBN: 0-7803-2625-3 page 387, alinéa II	1

1

GF Exhibit 1124 - 2360/2704

RAPPORT DE RECHERCHE INTERNATIONALE

Renseignements re. s aux membres de familles de brevets

mande Internationale No
PCT/FR 01/00532

Document brevet cité au rapport de recherche		Date de publication	Membre(s) de la famille de brevet(s)		Date de publication
EP 0469611	A	05-02-1992	JP	3039967 B	08-05-2000
			JP	4091480 A	24-03-1992
			DE	69108631 D	11-05-1995
			DE	69108631 T	04-01-1996
			KR	189691 B	01-06-1999
			US	5177568 A	05-01-1993
US 5140381	A	18-08-1992	FR	2660114 A	27-09-1991
			DE	69119809 D	04-07-1996
			DE	69119809 T	02-01-1997
			EP	0448465 A	25-09-1991
			JP	5322646 A	07-12-1993
EP 0456059	A	13-11-1991	DE	69121629 D	02-10-1996
			DE	69121629 T	13-02-1997
			JP	2751658 B	18-05-1998
			JP	4226081 A	14-08-1992
			US	5159416 A	27-10-1992

GF Exhibit 1124 - 2361/2704

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION WO0163677

TECHNICAL FIELD The present invention relates to a MOS transistor usable for producing circuits with high integration density.

STATE OF THE PRIOR ART FIG. 1 schematically represents the structure of a conventional MOS transistor. It is an n-channel MOS transistor.

It is produced on a solid substrate 1 of p-type silicon. Two n-type regions 2 and 3 are created, for example by ion implantation, to respectively form the source and the drain of the transistor. The reference 4 designates the gate oxide layer produced on the surface of the substrate 1 and under which the regions 2 and 3 extend beyond. A gate electrode 5 is deposited on the gate oxide layer 4. Source 6 and drain 7 electrodes are produced on regions 2 and 3 respectively and the transistor is isolated from adjacent devices by an oxide layer 8. There is also shown the channel 9 which forms under the gate oxide layer 4 when the transistor is suitably polarized. In the figure, the following important parameters are indicated: -length of channel L, -thickness of the gate oxide layer d, -depth of junction rj.

The sustained interest in the development of silicon technologies with high integration density, high frequencies and low consumption is largely motivated by new portability requirements, in particular for telecommunications and IT equipment. The exponential increase in technical (in accordance with Moore's law) and economic performance in silicon microelectronics is indicative of the most formidable industrial development of the twentieth century.

The massive use of the MOSFET transistor in the manufacture of integrated circuits has made it

GF Exhibit 1124 - 2362/2704

possible to significantly increase the integration density.

However, the sustained increase in integration density and electronic performance risks colliding with physical manufacturing limits. As a first approximation, it is recognized that a reduction of a factor a in the gate length of a MOSFET transistor must be accompanied by a simultaneous reduction of a factor of all the other characteristic dimensions (oxide thickness grid width, channel width, junction depth), a reduction by a factor of the supply voltage and an increase by a factor of the dopant concentration in the channel.

It is currently possible to obtain a minimum grid dimension of 22 nm. However, such a reduction implies modifications of other dimensions characteristic of the transistor which it is impossible to produce at present nor even in the near future according to "The International Technology Roadmap for Semiconductors-ITRS", 1999, SIA Semiconductor Industry Association.

The technological obstacles which prevent the realization of a conventional MOS transistor with a gate length of 22 nm are notably the following: -I: a very shallow depth of the source and drain extensions at their junction with the channel (from 8 to 13 nm); -II: an extremely steep concentration gradient at the source-channel and draincanal junctions (0.5 nm / dec.); -III: a very small thickness of silicon (12; -IV: a reduced consumption of silicon during the siliciding reaction (from 7 to 17 nm); -V: a low resistance per square of the silicide taking into account its reduced thickness (12.5 D / for a silicide thickness of 12 nm); -VI: a very low specific resistance of source and drain contact at the silicide-silicon interface (less than 1.5 × 10 −8 Q cm2) ; -VII: a very high level of doping in the channel (3-1019 cm-3).

The miniaturization of MOS devices requires the formation of increasingly shorter junctions, which makes it extremely difficult to optimize the specific contact resistance.

The reduction of this resistance is generally obtained by a siliciding process making it possible to obtain an alloy which provides low resistance of the silicide / silicon interface, for example TiSi2 / Si, CoSi2 / Si interfaces. However, the siliciding reaction induces silicon consumption which can lead on the one hand to a reduction in the effective contact surface and, on the other hand, to an increase in the specific contact resistance insofar as the interface silicide / silicon intervenes at too low doping values.

The article "Proposal of a Schottky-Barrier SET Aiming at a Future Integrated Device" by M.

GF Exhibit 1124 - 2363/2704

FUJISHIMA et al., Published in IEICE Transactions on Electronics, JP, Institute of Electronics Information and Comm. Eng. Tokyo, vol. E 80-C, n 7, July 1, 1997, pages 881 to 885, discloses a MOS transistor with one electron. This device exploits the Coulomb phenomenon, namely a charge quantization effect making it possible to obtain current oscillations as a function of the applied gate voltage. Several constraints are then imposed on it. The transistor must operate at low temperature (for example 10 K) so that the charge quantization is not masked by thermal load fluctuations. It is formed of a silicon channel connected to the outside (source / drain contacts) via Schottky barriers acting as a tunnel barrier. In order to be able to exploit the Coulomb blocking phenomenon, the tunnel resistance of the Schottky barriers must be greater than the quantum of resistance. This constraint justifies the use of relatively high Schottky barriers.

Finally, the device described in this article is a quantum wire on undoped silicon, which implies a very reduced device width. This very small width is essential for the operation of the SET transistor in order to reduce the set of capacities between the terminal contacts of the transistor and the silicon channel, the Coulomb blocking being able to be obtained only at the cost of very low capacities. The very small width of the device makes it possible to obtain a fairly large tunnel resistance of the junctions since the resistance is inversely proportional to the emission surface.

PRESENTATION OF THE INVENTION The present invention makes it possible to remedy the problems of producing MOS transistors for circuits with high integration density.

It relates to an MOS transistor produced in the thin silicon layer of an SOI substrate, said thin layer being lightly doped and having a thickness of less than 30 nm, the source and drain contacts being of the Schottky type at barrier height. Schottky as low as possible for majority carriers, the operating mode of the transistor being of the accumulation type.

Preferably, the doping rate of the thin layer is between 5.1014 cm-'and 1017 CM-3.

Advantageously, it is of the order of 1015 cm-3, for example 1 or 2.1015 cm ~ 3.

If the thin layer is p-doped, to obtain a p-MOSFET, the source and drain contacts are advantageously constituted by a PtGeSi silicide. Annealing, for example at a temperature of the order of 600 C for approximately 10 minutes, makes it possible to lower the height of the Schottky

GF Exhibit 1124 - 2364/2704

barrier of these contacts.

If the thin layer is doped n to obtain an n-MOSFET, the source and drain contacts can be constituted by an erbium-based silicide.

BRIEF DESCRIPTION OF THE DRAWINGS The invention will be better understood and other advantages and features will appear on reading the description which follows, given by way of nonlimiting example, accompanied by the appended drawings among which: FIG. 1, already described, shows schematically, the structure of a MOS transistor of the known art, produced on a solid silicon substrate, FIG. 2 represents, schematically, the structure of an MOS transistor according to the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION FIG. 2 schematically represents the structure of a MOS transistor according to the present invention. This transistor is produced on an SOI substrate 10 formed of a silicon wafer 11 successively covered with a layer of silicon dioxide 12 and a thin layer of silicon 13.

The thin layer 13, or active layer, has a thickness of less than 30 nm, typically between 5 and 20 nm. This layer is lightly doped, for example of the order of 1015 cm 3. The doping is of type n for an n-MOSFET and of type p for a p-MOSFET.

The transistor comprises source 14 and drain 15 contacts of the Schottky type and a gate 16 electrically insulated from the rest of the structure by a layer of gate insulator 17, for example made of silicon dioxide.

The operating principle is that of a MOS transistor with accumulation. The carriers that constitute the channel are the majority carriers of the substrate, that is to say the holes for a p-MOS transistor on SOI p-type substrate and the electrons for an n-MOS transistor on SOI n-type substrate. The conduction channel which is established between the source and drain contacts is controlled by the voltage applied to the grid. The device is turned on by a negative gate voltage with respect to the source voltage for a p-MOS type transistor and with a positive gate voltage with respect to the source voltage for an n-MOS type transistor. The Schottky barrier height should be as low as possible for majority carriers and ideally equal to 0 eV.

GF Exhibit 1124 - 2365/2704

The realization of the source and drain zones by Schottky contacts directly on the thin layer of silicon makes it possible to counter the technological obstacles I and II mentioned above.

As the thickness of silicide and the corresponding consumption of silicon during the siliciding reaction is not limited, this makes it possible to counter technological obstacles III, IV and V.

We obviate technological lock VI by choosing a very low Schottky barrier height for the source and drain contacts. In the case of a p-MOS transistor, it is possible to obtain a barrier height of the order of 0.05 eV, ie a resistivity of the order of 6.10-9 S2. cm2, by deposition of platinum or a germanium-platinum alloy followed by thermal annealing. In the case of an n-MOS transistor, an erbium-based silicide could give a barrier height of less than 0.2 eV.

The use of a thin layer of lightly doped silicon, for example of the order of 1015 cm-3, for the SOI substrate makes it possible to counter technological lock VII.

In the case of a p-MOS transistor, produced on a thin weakly doped layer (of the order of 1015 cm-3), the source and drain contacts can be obtained in the following manner. A germanium deposition is carried out by evaporation under ultra-vacuum.

A platinum deposition is then carried out by the same process. Annealing is then carried out at around 600 ° C. for a typical period of 10 minutes. The contacts obtained have a very low barrier height (approximately 0.05 eV). The specific contact resistance obtained is then of the order of 6.10-9 Q. cm2 at 10-8Q. cm2.

The source and drain Schottky contacts can be made before the grid is formed.

As a variant, it is possible to produce the gate oxide first and then deposit the gate material. The grid and the self-aligned channel are then defined by etching. The deposition of the source and drain contacts takes place only later by self-alignment after a siliciding reaction.

GF Exhibit 1124 - 2366/2704

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

CLAIMS WO0163677

CLAIMS

1.
MOS transistor made in the thin layer of silicon of an SOI substrate (10), said thin layer (13) being lightly doped and having a thickness of less than 30 nm, the source (14) and drain (15) contacts being of the Schottky type with a Schottky barrier height of less than 0.2 eV for majority carriers, the operating mode of the transistor being of the accumulation type.

2.
MOS transistor according to claim 1, characterized in that the doping rate of said thin layer (13) is between 5.1014 cm-3 and 10 "cm- \

3.
MOS transistor according to claim 2, characterized in that the doping rate of said thin layer (13) is of the order of 1015 cm ~ 3.

4.
MOS transistor according to any one of claims 1 to 3, characterized in that, said thin layer (13) being p-doped, the source (14) and drain (15) contacts consist of a PtGeSi silicide.

5.
MOS transistor according to claim 4, characterized in that the source (14) and drain (15) contacts

GF Exhibit 1124 - 2367/2704

consist of a PtGeSi silicide annealed at a temperature of the order of 600 C for approximately 10 minutes.

6.

MOS transistor according to any one of Claims 1 to 3, characterized in that, said thin layer (13) being n-doped, the source (14) and drain (15) contacts consist of a silicide based on erbium.

GF Exhibit 1124 - 2368/2704

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 4 :		(11) International Publication Number:
H01L 21/285, 29/40, 33/00	A1	WO 88/ 00392
		(43) International Publication Date: 14 January 1988 (14.01.88)

(21) International Application Number: PCT/US87/01520

(22) International Filing Date: 22 June 1987 (22.06.87)

(31) Priority Application Number: 878,077

(32) Priority Date: 24 June 1986 (24.06.86)

(33) Priority Country: US

(71) Applicant: AMERICAN TELEPHONE & TELEGRAPH COMPANY [US/US]; 550 Madison Avenue, New York, NY 10022 (US).

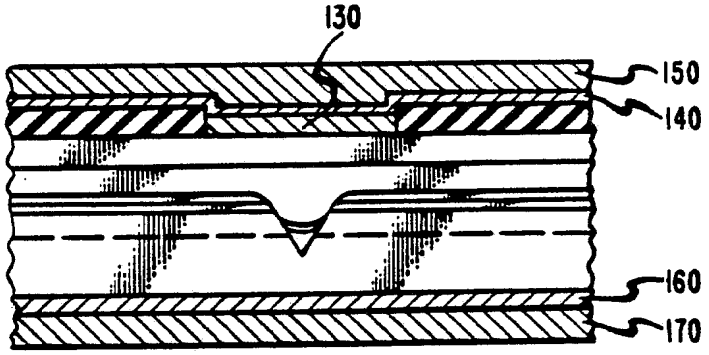
(72) Inventors: APPELBAUM, Amiram ; 11 Glenwood Road, Fanwood, NJ 07023 (US). ROBBINS, Murray ; 110 Kent Drive, Berkeley Heights, NJ 07922 (US).

(74) Agents: HIRSCH, A., E., Jr. et al.; Post Office Box 679, Holmdel, NJ 07733 (US).

(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), FR (European patent), GB (European patent), IT (European patent), JP, LU (European patent), NL (European patent), SE (European patent).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: METHOD FOR FABRICATING DEVICES IN III-V SEMICONDUCTOR SUBSTRATES AND DEVICES FORMED THEREBY



(57) Abstract

New technique for forming non-rectifying electrical contacts to III-V semiconductor materials, without the use of dopants or of an alloying procedure. In accordance with this technique, an electrical contact is formed simply by depositing a region of material e.g., 130, (onto the semiconductor material) having a composition which includes at least one metal element and at least one of three specific Group V elements, i.e., P, As, or Sb, and having a bulk electrical resistivity equal to or less than about 250 μΩ-cm. Alternatively, a contact is formed by depositing nickel, or a nickel-containing material essentially free of gold and silver, and having a composition which does not include any of the three Group V elements. The nickel, or nickel-containing material, is then reacted with the substrate to form a region, e.g., 130, including a compound having a composition which includes nickel as well as one of the three Group V elements.

GF Exhibit 1124 - 2369/2704

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	**FR**	France	**ML**	Mali
AU	Australia	**GA**	Gabon	**MR**	Mauritania
BB	Barbados	**GB**	United Kingdom	**MW**	Malawi
BE	Belgium	**HU**	Hungary	**NL**	Netherlands
BG	Bulgaria	**IT**	Italy	**NO**	Norway
BJ	Benin	**JP**	Japan	**RO**	Romania
BR	Brazil	**KP**	Democratic People's Republic of Korea	**SD**	Sudan
CF	Central African Republic			**SE**	Sweden
CG	Congo	**KR**	Republic of Korea	**SN**	Senegal
CH	Switzerland	**LI**	Liechtenstein	**SU**	Soviet Union
CM	Cameroon	**LK**	Sri Lanka	**TD**	Chad
DE	Germany, Federal Republic of	**LU**	Luxembourg	**TG**	Togo
DK	Denmark	**MC**	Monaco	**US**	United States of America
FI	Finland	**MG**	Madagascar		

GF Exhibit 1124 - 2370/2704

METHOD FOR FABRICATING DEVICES IN III-V SEMICONDUCTOR SUBSTRATES AND DEVICES FORMED THEREBY

Background of the Invention

1. Field of the Invention

The invention pertains generally to a method for fabricating devices in III-V semiconductor substrates, as well as the resulting devices.

2. Art Background

A wide variety of devices, including discrete electronic devices, discrete opto-electronic devices (devices which produce an optical output in response to an electrical input, or vice versa), as well as integrated circuit and integrated optical devices, are now being fabricated, or have been proposed for fabrication, in substrates which include III-V semiconductor materials, because these materials exhibit a number of significant advantages. (A III-V semiconductor material, for purposes of this disclosure, is a semiconductor which includes Group III and Group V elements.) Included among these advantages is the fact that the mobility of electrons in the III-V semiconductor materials is much higher than in other semiconductor materials, such as silicon. As a consequence, electronic and opto-electronic devices, e.g., discrete transistors, lasers and integrated circuit devices, fabricated in the III-V semiconductor materials are capable of achieving much higher operating speeds than are the corresponding devices fabricated in, for example, silicon. In addition, the III-V semiconductor materials are direct bandgap materials, rather than indirect bandgap materials, as is the case with silicon. As is known, stimulated emission of light is only achievable in the former type of materials. Consequently, opto-electronic devices which depend, for their operation, on stimulated light emission, e.g., lasers, must be fabricated in direct bandgap materials. Moreover, direct bandgap materials exhibit much higher quantum efficiencies than indirect bandgap materials, and therefore the former materials are preferred for the fabrication of optical detector, opto-electronic devices, such as avalanche photodiode (APD) detectors.

The various types of devices fabricated in III-V semiconductor substrates include a variety of device components, such as active regions (a region of semiconductor material in a light-emitting opto-electronic device from which most of the light is emitted), sources, drains, p-n junctions and heterojunctions. (The term heterojunction, as used in this disclosure, denotes the interface between two semiconductor materials having different compositions or different doping levels.) Each such device also includes one or more metallic wires or metallic runners, generally fabricated from gold (Au), terminating in one or more non-rectifying, low specific contact resistance (LSCR) electrical contacts to the substrate, through which electrical signals are communicated to the device. (As used herein, the term non-rectifying, LSCR electrical contact denotes an electrical contact which permits electrical current flow in two opposed directions across the contact, and exhibits a specific contact resistance less than or equal to about 10^{-4}ohm-cm^2 in both directions. Significantly, such contacts to III-V semiconductor substrates are essential because the gold (per se) in the gold wires and gold runners yields a rectifying, rather than non-rectifying, electrical contact to III-V semiconductor materials.)

A non-rectifying, LSCR electrical contact to a III-V semiconductor substrate is conventionally formed by depositing, e.g., e-beam evaporating, a region of material which includes gold and a p-type (e.g., zinc or beryllium) or n-type (e.g., tin or germanium) dopant (depending upon whether the underlying semiconductor material is of p-type or n-type conductivity) onto the substrate. Because ultra-high-vacuum conditions are typically not employed, a native oxide (or oxides) of the semiconductor material tends to form on the surface of the substrate during the deposition procedure. Such native oxides are generally undesirable because their presence serves to increase specific contact resistance. Although the surface of the substrate is typically cleaned to remove these oxides, it is generally acknowledged that complete removal of the oxides is impossible. However, the presence of these oxides does not, in this instance, preclude the formation of a LSCR electrical contact. That is, after deposition, the gold-and-dopant-containing region is alloyed at temperatures as high as about 450 degrees Centigrade (C) for periods of time equal to about 7 minutes. Significantly, it is believed that this alloying procedure serves to drive the dopant through the native oxide (or oxides) and into the substrate, and

electrically activate the dopant, to produce an electrical contact having a low specific contact resistance.

While the above alloying procedure does produce useful, non-rectifying, LSCR electrical contacts, this procedure does have a number of disadvantages, including undesirable interactions between the gold and the semiconductor substrate. For example, the relatively high temperatures involved in the alloying process result in the gold diffusing into the substrate, causing decomposition of the substrate material. As a consequence, and if, for example, the substrate material includes indium phosphide (InP), then the resulting free In and P (freed by the decomposition of the InP) tend to diffuse to the surface of the electrical contact, where they may undergo oxidation to form electrically insulating layers. In addition, the relatively high alloying temperatures also result in upward diffusion of the p- or n-type dopant to the surface of the electrical contact, where the dopant also tends to become oxidized to form an electrically insulating layer. Unless great care is taken to remove these insulating layers, the electrical contact will exhibit undesirably high series resistance.

The downward diffusion of gold into the substrate is also undesirable because the presence of gold in, for example, an active region constitutes a non-radiative recombination center, which serves to reduce the useful lifetime of light-emitting opto-electronic devices, such as lasers. In addition, the downward diffusion of gold into a substrate containing a relatively shallow p-n junction (a p-n junction having a depth equal to or less than about one-half micrometer) is undesirable because the gold penetrates through, and thus short circuits, these relatively shallow p-n junctions.

The relatively high alloying temperatures employed in forming the gold electrical contacts are further disadvantageous because they sometimes lead to significant, differential thermal expansions of the materials covering the substrate, which in turn leads to high stress in the substrate. Such high stress is undesirable because it leads to bending of the substrate, which makes conventional lithographic processing very difficult, if not impossible. This high stress often also leads to cracking and/or peeling of material layers overlying the substrate.

The above contact-fabrication procedure is further disadvantageous because it requires that the relative amounts of gold and dopant be precisely controlled to achieve the eutectic composition. Otherwise, the gold may not melt during the alloying process and/or the alloying process may not produce a sufficient or desired interaction between the dopant and the substrate, leading to an undesirably high specific contact resistance.

The above-described problems, resulting from the undesirable interactions between gold and III-V semiconductors, as well as scientific curiosity, have led to investigations of the interactions between various metals, including nickel, and III-V semiconductor substrates, such as InP. (Regarding these investigations see E. Hokelek et al., "A Study of Schottky Contacts on Indium Phosphide", Journal of Applied Physics, Vol. 54, No. 9, September 1983, pp. 5199-5205 and G. J. Hughes et al., "Nickel and Copper on Cleaved Indium Phosphide: Structure, Metallurgy and Electronic Properties," Journal of Physics C: Solid State Physics, Vol.16 (1983), pp. 2391-2405.) In these investigations, the various metals were deposited onto indium phosphide substrates cleaved under ultra-high-vacuum conditions to avoid adsorption of contaminants, such as carbon and oxygen (which might increase specific contact resistance, or preclude the formation of non-rectifying contacts). As a result of these investigations, it was concluded, among other things, that nickel produces a Schottky barrier contact (a rectifying, metal-semiconductor contact) to InP and, moreover, that a relatively thin nickel phosphide layer is formed at the interface between the nickel and the InP. While no connection was made (in these investigations) between the existence of the nickel phosphide layer and the existence of the Schottky barrier contact, it has long been believed that a non-rectifying, LSCR contact between a metal, such as nickel, and a substrate of InP can only be achieved if the metal-InP interface is rich in indium. But the interfacial nickel phosphide layer found in the investigations was, presumably, the result of nickel reacting, i.e. combining, with the phosphorus in the InP substrate. Such a reaction would necessarily produce free indium (In), which (under the resulting In concentration gradient) would diffuse to the surface of the nickel, resulting in a nickel-InP interface which is depleted of In. Significantly, a substantial amount of In was found (presumably the result of upward diffusion) on the surface of the nickel, in these investigations.

GF Exhibit 1124 - 2374/2704

Consequently, and on the basis of current beliefs, an In-depleted interface, produced by the formation of an interfacial, nickel phosphide layer, would preclude the formation of a non-rectifying, LSCR contact, and would be consistent with the Schottky barrier contacts found in the investigations.

Thus, those engaged in the development of III-V semiconductor devices have sought, and continue to seek, new materials and new methods for forming non-rectifying, LSCR electrical contacts to III-V semiconductor substrates.

Summary of the Invention

The invention embodies a method of fabricating a device in a body which includes Group III - Group V semiconductor material and involves the finding that simply depositing any one of a specific class of compounds onto a p- or n-type III-V semiconductor substrate, having a doping level equal to or greater than about 10^{17} per cubic centimeter (cm^{-3}), yields a non-rectifying, LSCR electrical contact to the substrate. The members of this class of compounds are those having compositions which include at least one metal element and at least one of three specific Group V elements, i.e., phosphorus (P), arsenic (As) or antimony (Sb), and having bulk electrical resistivities equal to or less than about 250 micro-ohm-centimeters ($\mu\Omega$-cm), and preferably equal to or less than about 100 $\mu\Omega$-cm. In addition, the invention involves the finding that depositing nickel, or a nickel-containing material which is essentially free of gold and silver and does not include any of the above three Group V elements, onto a III-V semiconductor material, and then reacting the nickel, or nickel-containing material with the semiconductor material to produce a compound having a composition which includes nickel as well as at least one of the three Group V elements, also yields a non-rectifying, LSCR electrical contact. Significantly, these contacts are formed without the use of dopants and without the need for an alloying procedure. Moreover, these contacts are formed (through deposition or deposition followed by chemical reaction) without the use of ultra-high-vacuum conditions, and despite the (presumed) adsorption of contaminants and formation of native oxides of the semiconductor material.

By way of example, a non-rectifying, LSCR electrical contact to a semiconductor substrate of, for example, InP is readily formed simply by depositing a region of nickel phosphide directly onto the substrate. Alternatively, a region of nickel is deposited onto the substrate and allowed to

spontaneously react with substrate material to form a relatively thin, interfacial layer of nickel phosphide. Contrary to the conventional wisdom, the (presumably) In-depleted interface between the deposited nickel and the semiconductor substrate does not preclude formation of a non-rectifying, LSCR electrical contact.

After being formed, the inventive LSCR electrical contacts are often subjected to relatively high temperatures during various device fabrication steps. Depending upon the particular compositions of the materials employed in the electrical contacts, these materials may (under the influence of the relatively high temperatures) undergo reactions with the substrate material. As a consequence, Group III and/or Group V elements in the substrate may be freed to diffuse to the surface of the electrical contacts, where they may undergo oxidation to form electrically insulating layers.

To avoid the possibility of reactions during high temperature processing, the compositions of the materials employed in the inventive LSCR electrical contacts are preferably chosen (in accordance with a two-step procedure, described below) to have heats of formation which preclude such reactions.

Significantly, it has been found that non-rectifying, LSCR electrical contacts having compositions which preclude reactions with the III-V semiconductor substrates, which are amorphous, and have thicknesses equal to or greater than about 20 nm, are effective barriers to the diffusion of gold (from overlying gold regions, used to facilitate bonding of gold wires or runners) into underlying substrates. As a consequence, light-emitting opto-electronic devices which include such contacts have significantly increased lifetimes. Moreover, LSCR electrical contacts to relatively shallow p-n junctions are now readily formed, without short-circuiting the p-n junctions.

Brief Description of the Drawings

The invention is described with reference to FIGS. 1-6, which depict the steps involved in fabricating a channel-substrate-buried-heterostructure indium phosphide laser, using the inventive device fabrication method.

Detailed Description

The invention involves a method for fabricating devices in III-V semiconductor substrates, which is distinguished from previous such methods in that it includes a new technique for forming non-rectifying, LSCR electrical

contacts to these substrates. The invention also involves the devices, e.g., transistors, lasers, light-emitting diodes, photodetectors, integrated circuits and integrated optical devices, resulting from the inventive method.

As discussed, the invention involves the finding that non-rectifying, LSCR electrical contacts to p- or n-type III-V semiconductor substrates, having doping levels equal to or greater than about $10^{17}cm^{-3}$, are readily formed, using either of two techniques. In the first technique, an electrical contact is formed by first cleaning the substrate (using conventional degreasers and oxide strippers), and then simply depositing, e.g., DC magnetron sputtering, any one of a specific class of compounds onto the substrate. The members of this class of compounds are those having compositions which include at least one metal element and at least one of three specific Group V elements, i.e., P, As or Sb, and having bulk resistivities equal to or less than about 250 $\mu\Omega$-cm, and preferably equal to or less than about 100 $\mu\Omega$-cm. The compounds which meet these requirements are typically (although not exclusively) binary, ternary, or quatenary metallic compounds which include, for example, Ni_3P, Ni_2P, NiP, $Ni_{11}In_4P_2$, Ni_3As, Ni_2As, NiAs, Ni_3Sb, Ni_2Sb, and NiSb.

Significantly, the compound deposition, referred to above, need not take place under ultra-high-vacuum conditions, and, if possible, even ordinary room atmospheric conditions are useful. Surprisingly, and even though contaminants are presumably adsorbed, and native oxides of the semiconductor material are presumed to form, during the time interval between cleaning and deposition, the resulting electrical contact is highly useful, i.e., exhibits a specific contact resistance equal to or less than about $10^{-4}ohm\text{-}cm^2$ to current flow in two opposed directions.

In the second technique, a non-rectifying, LSCR electrical contact to a III-V semiconductor substrate is formed by (cleaning the substrate and) depositing nickel, or a nickel-containing material which is essentially free of gold and silver and does not include any of the three Group V elements, onto the substrate. Then the deposited material is either induced to react (e.g., heat is supplied), or allowed to spontaneously react (i.e., no external stimulus, such as heat, is supplied), with the substrate to form a compound having a composition which includes both nickel as well as one (or more) of the three Group V elements. (Generally, it cannot be predicted whether any particular set of

deposition conditions will result in a spontaneous reaction between the deposited material and the substrate material to produce the desired compound. However, the presence or absence of the desired compound is readily detected using conventional techniques such as Auger electron spectroscopy. Thus, the utility of a particular deposition procedure for achieving the desired spontaneous reaction is readily determined empirically.)

By way of example, an electrical contact to a substrate of InP is formed by depositing, e.g., e-beam evaporating, a region of nickel directly onto the substrate, and then allowing the nickel to spontaneously react with the substrate (during and after the deposition procedure) to form a relatively thin, interfacial layer of nickel phosphide. (The thickness of this interfacial layer is typically several fractions of a nanometer.) If a thicker layer of nickel phosphide is desired, then the nickel-bearing InP-substrate should, for example, be heated, to react additional nickel with the substrate material. In this regard, it has been found that a relatively thick layer of essentially pure Ni_2P is readily formed by carrying out the heating process (at a temperature of, for example, 300 degrees C) in an atmosphere of forming gas, i.e., an atmosphere which includes about 15 percent (by volume) of H_2 and about 85 percent of N_2.

It is contemplated that the two techniques, described above, yield non-rectifying, LSCR contacts because Group III elements in the substrate form chemical bonds with the Group V elements in the contacts. Moreover, it is believed that electron-transport across the contact-substrate interface is largely due to thermionic emission.

Significantly, the nickel-containing electrical contacts formed by deposition and reaction are typically crystalline in nature. By contrast, the electrical contacts formed by deposition, alone, are either crystalline or amorphous in nature, depending upon deposition conditions. (For purposes of the invention, a material is amorphous if it either has no grains or, if grains are present, their dimensions are equal to or less than about 50 nm.) For example, if an electrical contact of Ni_2P is deposited using conventional DC magnetron sputtering techniques, then a relatively low substrate-support temperature (e.g., -100 degrees Centigrade) and/or a relatively low sputtering voltage (e.g., 280 volts) yields amorphous Ni_2P. On the other hand, a substrate-support maintained at room temperature (23 degrees Centigrade) and/or a relatively

high sputtering voltage (e.g., 300 volts) yields crystalline Ni_2P. This distinction between the natures of the electrical contacts results in different contact properties. That is, crystalline contacts typically exhibit lower bulk resistivities than amorphous contacts, which leads to reduced series resistance. On the other hand, as discussed more fully below, amorphous contacts are better diffusion barriers than crystalline contacts.

The inventive method for fabricating devices often involves relatively high temperature processing subsequent to the fabrication of a non-rectifying LSCR electrical contact (or contacts). Such high temperature processing may result in chemical reactions between the material of the electrical contact and the substrate material. As a consequence, some Group III and/or Group V elements in the substrate may be freed to diffuse to the surface of the electrical contact, where they may be oxidized to form electrically insulating layers. Such layers may lead to relatively high series resistance.

Preferably, to avoid the high temperature reactions, discussed above, the composition of the material employed in the inventive electrical contact is chosen in accordance with a two-step procedure. In the first step, those compositions are identified which include P, As, or Sb (and nickel, if the contact is formed by deposition and reaction), have bulk resistivities less than or equal to about 250 $\mu\Omega$-cm, and have heats of formation per metal atom (kilocalories per metal atom) which are more negative than that of the substrate composition, i.e., in magnitude (absolute value), the heats of formation per metal atom of the potentially useful compositions are larger than that of the substrate composition. (If a composition includes more than one metal element, then the average heat of formation per metal atom is employed.) Compositions which meet this requirement are (by definition) thermodynamically more stable than the substrate composition. However, one or more of these compositions might still react (under the influence of the relatively high temperatures) with substrate material to form an even more stable composition. To avoid this possibility, these particular compositions are identified and weeded out. That is, during the second step, the most stable composition, i.e., the composition having the most negative heat of formation per metal atom, is initially identified. Then, the magnitude (the absolute value) of the difference between the heat of formation per metal atom of each composition (identified in the first

step) and the most stable composition is calculated. If, for any particular composition, this magnitude is less than the magnitude (absolute value) of the heat of formation per metal atom of the semiconductor composition, then (thermodynamically) this particular composition is precluded from reacting with the substrate to form a more stable composition. Alternatively, and regardless of this requirement, if a particular composition has a larger relative amount of the Group V element than the most stable composition, then this composition too is precluded from reacting with the substrate.

By way of example, if the semiconductor substrate is of InP, then the first step (of the two-step procedure) implies that the potentially useful compositions include Ni_6P_5, Ni_3P_2, and Ni_2P. Significantly, Ni_6P_5 is the most stable of these compositions. Applying the criterion of the second step implies that all of these compositions are thermodynamically stable, i.e., will not react with InP. Moreover, NiP is also useful (will not react with InP) because it contains a larger relative amount of P than Ni_6P_5.

Typically, after an electrical contact is formed, a region of gold (and, perhaps, other materials) is deposited onto the contact to facilitate the bonding of gold wires and/or gold runners to the electrical contact. Significantly, it has been found that material regions which are thermodynamically stable, as defined by the above two-step procedure, are amorphous, and have thicknesses equal to or greater than about 20 nanometers are effective barriers to undesirable interdiffusion of gold (from the overlying gold region) and the underlying semiconductor material. (Such interdiffusion is undesirable for the reasons given above, in relation to conventional gold electrical contacts.) Thus, such materials are useful both as diffusion barriers and as non-rectifying, LSCR electrical contacts. In fact, such material regions are highly useful just as diffusion barriers interposed between any of a variety of electrical contacts and, for example, the corresponding, overlying gold regions.

Among other advantages, the inventive technique for forming electrical contacts makes it possible to form a relatively shallow electrical contact to a relatively shallow p-n junction or a relatively shallow heterojunction (a p-n junction or heterojunction having a depth less than or equal to about 1/2 micrometer), without short-circuiting the p-n junction or heterojunction. (For purposes of the invention, the depth of a p-n junction, or of a heterojunction, is

GF Exhibit 1124 - 2380/2704

defined with reference to the device surface, or interface between different material regions of the device, on which the electrical contact is formed, or from, or through which, the electrical contact extends. That is, the depth of a p-n junction formed, for example, by producing a p-type region within an n-type substrate, is defined as the length of a perpendicular extending from a least-squares-fit planar approximation to the above reference surface or reference material interface to the lowest point where the dopant concentration in the p-type region is equal to the dopant concentration in the n-type substrate. On the other hand, the depth of a heterojunction formed by different semiconductor materials is defined as the length of a perpendicular extending from the above least-squares-fit planar approximation to the lowest point of the interface between the two materials, as determined using, for example, Auger electron spectroscopy. Further, the depth of a heterojunction formed by semiconductor materials having the same composition but different doping levels is as defined above, except that the perpendicular extends to the lowest point of the interface between the two materials where the doping level is the average of the doping levels in the two materials as determined, for example, by SIMS analysis.) That is, and as discussed above, the alloying procedure involved in forming a conventional gold contact typically results in gold being diffused downwardly into the semiconductor substrate. If the electrical contact is to a substrate region containing a p-n junction or heterojunction having a depth equal to or less than about 1/2 micrometer, then the gold invariably diffuses more than about 1/2 micrometer, i.e., the gold diffuses into, and through, the junction, short-circuiting the junction. By contrast, the inventive technique involves no alloying procedure. Thus, provided the contact material is thermodynamically stable, amorphous, and has a thickness equal to or greater than about 20 nanometers, both gold and contact material are largely precluded from diffusing downwardly into the semiconductor substrate into electrical contact with the p-n junction or heterojunction.

Yet another advantage of the invention is the fact that it permits the useful lifetimes of light-emitting, discrete opto-electronic and integrated optical devices to be significantly increased. That is, by forming the material compositions with thicknesses equal to or greater than about 20 nanometers, the downward diffusion of gold into the active regions of such devices is largely

precluded. As a consequence, the formation of non-radiative recombination centers is largely avoided.

As a pedagogic aid to an even more complete understanding of the invention, the application of the inventive device fabrication method to the formation of a channel-substrate-buried-heterostructure InP laser, is described below.

With reference to FIGS. 1-6, the laser is formed in a substrate which initially includes just a bulk region 10 of, for example, n-type InP, e.g., a wafer of n-type InP. The doping level within the bulk region 10 is, for example, about $8 \times 10^{17} cm^{-3}$.

The first step in the fabrication of the laser is to form a blocking layer 30, i.e., a layer which blocks the flow of currents external to the active region (described below) into the bulk region 10, adjacent to the upper surface 20. The blocking layer 30 is formed, for example, by diffusing a p-type dopant, such as cadmium, into the bulk region 10. The doping level within the blocking layer should be equal to or greater than about $4 \times 10^{18} cm^{-3}$ to avoid the flow of undesirable leakage currents across the blocking layer and into the bulk region 10. In addition, the thickness of the blocking layer 30 ranges from about 0.5 μm to about 1.5 μm. Thicknesses less than about 0.5 μm are undesirable because they too result in undesirable leakage currents across the blocking layer. Thicknesses greater than about 1.5 μm are undesirable because they result in lasers which require undesirably large amounts of electrical power to achieve stimulated light emission.

Alternatively, the blocking layer 30 is formed by depositing a layer of semi-insulating InP onto the surface 20, using conventional metal organic chemical vapor deposition techniques. Here, the term semi-insulating means that the deposited semiconductor material has a bulk resistivity equal to or greater than about 10^7 ohm-cm.

After the formation of the blocking layer 30, an etch mask 40 is formed on the upper surface of the blocking layer. This etch mask includes, for example, a layer of silicon dioxide which is deposited onto the blocking layer 30 using conventional plasma deposition techniques. The etch mask is formed by patterning the silicon dioxide layer using, for example, conventional lithographic techniques. The thickness of the silicon dioxide layer ranges from 110 nm to

about 130 nm. Thicknesses less than about 110 nm are undesirable because they result in an undesirably large number of pinholes in the silicon dioxide. On the other hand, thicknesses greater than about 130 nm are undesirable because they make it difficult to achieve the desired sidewall inclination of the V-groove, described below.

With the etch mask 40 in place, a crystallographic, chemical etchant, e.g., 3:1 $HCl:H_3PO_4$, is applied to the exposed region of the substrate surface to form a V-groove 50. This V-groove 50 serves to channel, and confine, the electrical current to the active region of the laser. The etchant is chosen to expose (111) facets of the crystalline substrate. Moreover, the width of the V-groove ranges from about 3.5 micrometers (μm) to about 4.5 μm. Widths less than about 3.5 μm, or greater than about 4.5 μm, are undesirable because they result in devices which require an undesirably large amount of electrical power to achieve stimulated emission of light.

After the etching of the V-groove 50, and after removing (using conventional chemical etchants) the etch mask 40, an n-type InP buffer region 60 is grown in the bottom of the V-groove 50 (as well as on the surface of the blocking layer 30) using conventional liquid phase epitaxy (LPE) techniques. The thickness of the buffer region, as measured from the bottom of the V-groove, typically ranges from about 0.5 μm to about 1 μm. Unlike the sidewalls of the V-groove, the buffer region 60 is largely free of contaminants and defects.

An undoped, active region 70 of III-V semiconductor material is now grown on the buffer region 60 in the V-groove 50 (as well as on the upper surface of the blocking layer 30) using conventional LPE techniques. To ensure that electrical conduction is largely confined to the active region 70, the bandgap of the semiconductor material employed in the active region should be less than that of the semiconductor material employed both in the blocking layer 30 and in the cladding layer (discussed below). One such useful (active region) material is, for example, (undoped) indium gallium arsenide phosphide (InGaAsP). The thickness of the active region ranges from about 0.2 μm to about 0.7 μm. Thicknesses less than about 0.2 μm are undesirable because such thin regions result in undesirably little stimulated light emission from the laser. Thicknesses greater than about 0.7 μm are undesirable because they result in lasers which require an undesirably large amount of electrical power to achieve

stimulated emission of light.

The growth of the active region 70 is followed by the LPE-growth of a cladding layer 80 and of a cap layer 90. The former is, for example, of p-type InP, while the latter is of p-type indium gallium arsenide (InGaAs). The thickness of the cladding layer, and of the cap layer, is typically about 1 μm.

A (patterned) deposition mask 120 is now formed on the upper surface of the cap layer 90. As discussed below, the deposition mask permits the electrical contact to the laser to be formed in vertical alignment with the active region 70. The deposition mask 120 includes a layer 100 of silicon dioxide which is deposited onto the cap layer 90 using, for example, conventional plasma deposition techniques. In addition, the deposition mask includes a layer 110 of, for example, photoresist. The thickness of the silicon dioxide layer is typically about 0.3 μm, while the thickness of the photoresist is typically about 1 μm. In forming the deposition mask, the photoresist is initially patterned, i.e., a region of the photoresist overlying the active region 70 is removed, using conventional exposure and development techniques. The width of this region (and thus the ultimate width of the electrical contact) is typically about 6 μm. The patterned photoresist layer is then used as an etch mask during the etching of the silicon dioxide layer 100, resulting in the removal of a region of the silicon dioxide layer which also overlies the active region 70. Useful silicon dioxide-etchants include, for example, buffered HF.

An electrical contact to the laser is now produced by depositing, e.g., sputtering, an amorphous region 130 of, for example, Ni_6P_5 onto the exposed upper surface of the cap layer 90. Preferably, the thickness of the region 130 is equal to a greater than about 20 nanometers, to avoid the downward diffusion of gold (from a gold region subsequently formed on the region 130).

Preferably, to enhance the adhesion of the region 130 to the cap layer 90, a layer 140 of titanium is deposited onto the upper surface of the region 130 as well as onto the upper surface of the silicon dioxide layer 100. The thickness of the titanium layer is typically about 5 nanometers.

With the completion of the electrical contact, a layer 150 of gold is deposited onto the upper surface of the titanium layer 140, to facilitate the subsequent bonding of a gold wire to the electrical contact. The thickness of the gold layer is typically about 1 μm.

GF Exhibit 1124 - 2384/2704

A second electrical contact is, of course, needed to apply voltages to the laser. This second contact is formed on the backside of the substrate by initially thinning the bulk region 10 (typically by about 75 μm) using conventional mechanical lapping, and then depositing successive layers 160 and 170 of, respectively, Ni_6P_5 and gold, onto the backside, as described above.

The bulk region 10, which is now an integral part of the laser, is typically a portion of a wafer which, at this point, is cleaved (using conventional techniques) to form the end mirror-facets of the laser device. The laser device is separated from the wafer using saw cuts transverse to the mirror-facets.

The final steps in the fabrication of the laser typically involve soldering (at temperatures ranging from about 200 degrees C to about 350 degrees C) the laser to a stud which serves both as a heat sink for the device, as well as a device carrier or package. Then, gold wires are bonded to the gold regions 150 and 170 covering the top and bottom of the laser.

Example 1

The lower surface of a 1.27 cm (one-half-inch) diameter indium phosphide wafer, of n-type conductivity, and having a doping level of $8 \times 10^{17} cm^{-3}$, was cleaned using conventional degreasers and oxide strippers. Using conventional e-beam evaporation techniques, successive layers of gold, germanium, and gold were deposited onto the cleaned lower surface. The thicknesses of these layers were, respectively, 5 nm, 15 nm, and 100 nm.

The upper surface of the wafer was degreased, and a layer of SiO_2, having a thickness of 500 nm, was plasma deposited onto the upper surface. A layer of photoresist was spin-deposited onto the SiO_2, and conventionally lithographically patterned to remove circular regions of photoresist having diameters ranging from about 20 μm to about 200 μm. Using the patterned photoresist as an etch mask, the silicon dioxide was chemically etched with buffered HF to expose corresponding circular surface areas of the indium phosphide.

A layer of Ni_2P, having a thickness of about 100 nm, was deposited onto the exposed, circular surface areas of the wafer, as well as onto the photoresist, using DC magnetron sputtering. The gas within the sputtering chamber was argon, the pressure of the gas was 1.6 Pa (12 millitorr), and the DC voltage was 300 volts. The Ni_2P-covered photoresist was then stripped from the wafer using

conventional chemical etchants.

The conventional Cox and Strack technique (see R. H. Cox and H. Strack, Solid State Electronics, Vol. 10, page 1213 (1967)) was employed to measure the specific contact resistance at each of the Ni_2P-covered regions of the wafer, using electrical currents of opposite polarity. In all cases, the specific contact resistance was equal to or less than about 3×10^{-6} ohm-cm^2.

Example 2

A 1.27 cm (one-half-inch) indium phosphide wafer was processed, as in Example 1, except that a different technique was used to form the circular regions of Ni_2P on the upper surface of the wafer. That is, after the photoresist and SiO_2 were patterned, a 100 nm-thick layer of Ni was e-beam evaporated onto the exposed, circular surface areas of the wafer, as well as onto the photoresist. After stripping the Ni-covered photoresist, the wafer was placed in an atmosphere of forming gas, and heated to a temperature of 300 degrees C for 30 minutes to produce circular regions of Ni_2P, having thicknesses of about 130 nm, on the wafer.

Using the technique employed in Example 1, the specific contact resistance, in all cases, was found to be equal to or less than about 3×10^{-6} ohm-cm^2.

GF Exhibit 1124 - 2386/2704

Claims

1. A method for fabricating a device in a body which includes III-V semiconductor material, comprising the steps of:

forming a non-rectifying, low-specific-contact-resistance electrical contact to a region of said body having a doping level equal to or greater than about $10^{17}cm^{-3}$; and

completing the fabrication of said device,

CHARACTERIZED IN THAT

said forming step includes the step of

(a) depositing a metal-containing first region of material onto said region of said body, or

(b) depositing a nickel-containing second region of material, essentially free of gold and silver, onto said region of said body and reacting said second region with said semiconductor material to form a nickel-containing third region of material,

each of said first and third regions having a composition which includes at least one element chosen from the group consisting of phosphorus, arsenic and antimony, and having a bulk resistivity equal to or less than about 250 $\mu\Omega$-cm.

2. The method according to claim 1

CHARACTERIZED IN THAT

said metal of said first region includes nickel.

3. The method according to claim 1,

CHARACTERIZED IN THAT

said composition is chosen to preclude chemical reactions between said first or said third of material and said semiconductor material.

4. The method according to claim 1,

CHARACTERIZED IN THAT

said first region of material, or said third region of material, is amorphous.

5. The method according to claim 1,

CHARACTERIZED IN THAT

said first region of material, or said third region of material, has a thickness equal to or greater than about 20 nanometers.

6. The method according to claim 1,

CHARACTERIZED IN THAT

said device includes a discrete electronic device or an integrated circuit device or an opto-electronic or an integrated optical device.

7. The method according to claim 6,

CHARACTERIZED IN THAT

said discrete electronic device includes a transistor.

8. The method according to claim 6,

CHARACTERIZED IN THAT

said opto-electronic device includes a laser or a light-emitting diode or a photodetector.

9. A method according to claim 1,

CHARACTERIZED IN THAT

said body includes a surface or material interface, and said body region includes a p-n junction or a heterojunction adjacent said surface or material interface;

said p-n junction or said heterojunction has a depth, as measured from said surface or material interface, equal to or less than about 1/2 micrometer,

a non-rectifying, low-specific-contact-resistance electrical contact is on and/or extends from or through said surface or material interface, and

said electrical contact includes material which, if it extends into said body, does not extend into electrical contact with said p-n junction or said heterojunction.

FIG. 1

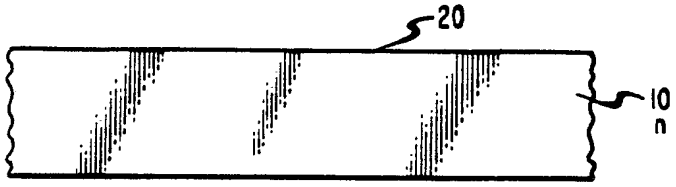


FIG. 2

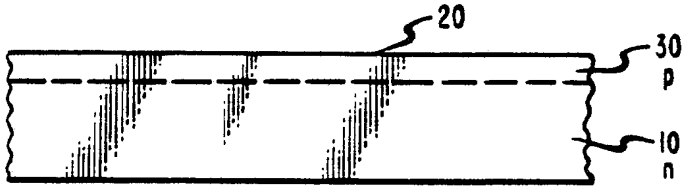


FIG. 3

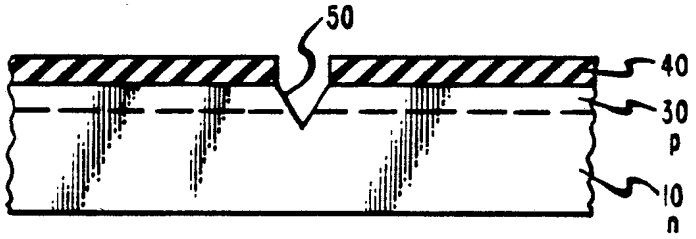
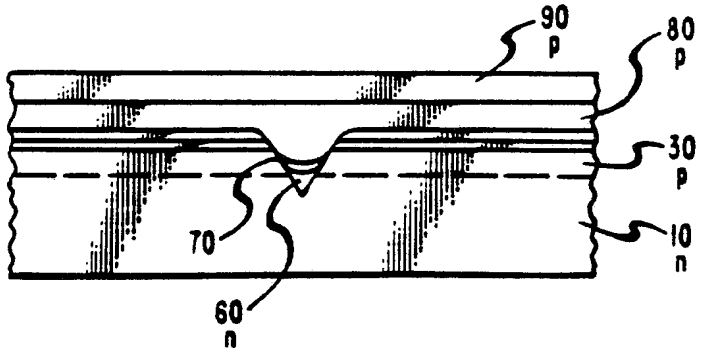


FIG. 4



GF Exhibit 1124 - 2389/2704

FIG. 5

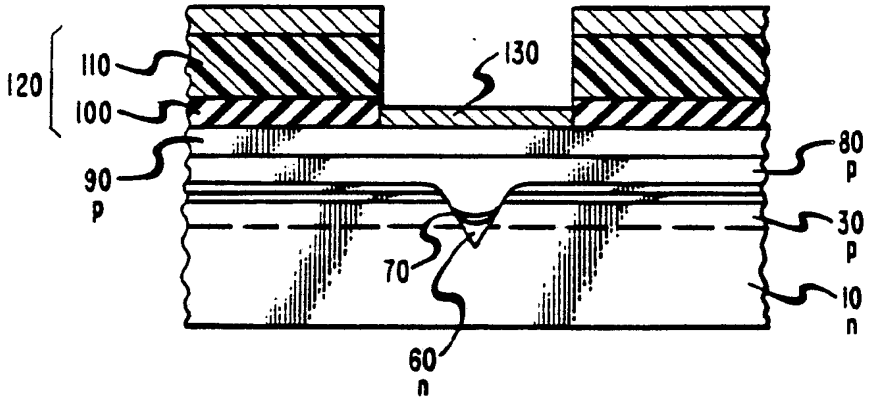
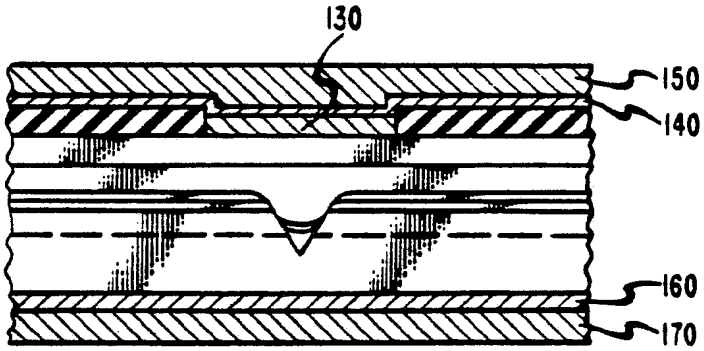


FIG. 6



INTERNATIONAL SEARCH REPORT

International Application No PCT/US 87/01520

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [5]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 01 L 21/285; H 01 L 29/40; H 01 L 33/00

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A	Materials Letters, volume 3, no. 7,8, May 1985, Elsevier Science Publishers B.V., (Amsterdam, NL), S.R. Smith et al.: "Stable ohmic contacts to n-GaAs using ion-beam mixing", pages 294-298 see the whole document --	1,2,6,9
A	GB, A, 2024506 (WESTERN ELECTRIC CO.) 9 January 1980 see the whole document --	1,6-9
A	Journal of Physics C: Solid State Physics, volume 16, 1983, The Institute of Physics, (London, GB), G.J. Hughes et al.: "Nickel and copper on cleaved indium phosphide: structure, metallurgy and electronic properties", pages 2391-2406 see paragraph 1: "Introduction"; paragraph 4: "Discussion" cited in the application -- ./.	1-3

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
21st September 1987	18 NOV 1987
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	M. VAN MOL

Form PCT/ISA/210 (second sheet) (January 1985)

GF Exhibit 1124 - 2391/2704

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
A	Thin Solid Films, volume 70, no. 1, July 1980, Elsevier Sequoia S.A., (Lausanne, CH), M. Ogawa: "Alloying reaction in thin nickel films deposited on GaAs", pages 181-189 see the whole document	1
A	Solid-State Electronics, volume 26, no. 3, March 1983, Pergamon Press Ltd, (Exeter, GB), A. Piotrowska et al.: "Ohmic contacts to III-V compound semiconductors: a review of fabrication techniques", pages 179-197	
A	Journal of Applied Physics, volume 54, no. 9, September 1983, American Insitute of Physics, (New York, US), E. Hökelek et al.: "A study of Schottky contacts on indium phosphide", pages 5199-5205 cited in the application	

GF Exhibit 1124 - 2392/2704

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 87/01520 (SA 17750)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 29/09/87

The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
GB-A- 2024506	09/01/80	BE-A-	877189	15/10/79
		NL-A-	7904979	02/01/80
		FR-A,B	2430090	25/01/80
		DE-A-	2925791	03/01/80
		US-A-	4186410	29/01/80
		JP-A-	55004999	14/01/80
		CA-A-	1125924	15/06/82

GF Exhibit 1124 - 2393/2704

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 :		(11) International Publication Number:
H01L 21/285	A1	WO 93/11558
		(43) International Publication Date: 10 June 1993 (10.06.93)

(21) International Application Number: PCT/US92/10213

(22) International Filing Date: 24 November 1992 (24.11.92)

(30) Priority data:
07/798,538 26 November 1991 (26.11.91) US

(71) Applicant: MATERIALS RESEARCH CORPORATION [US/US]; Route 303, Orangeburg, NY 10962 (US).

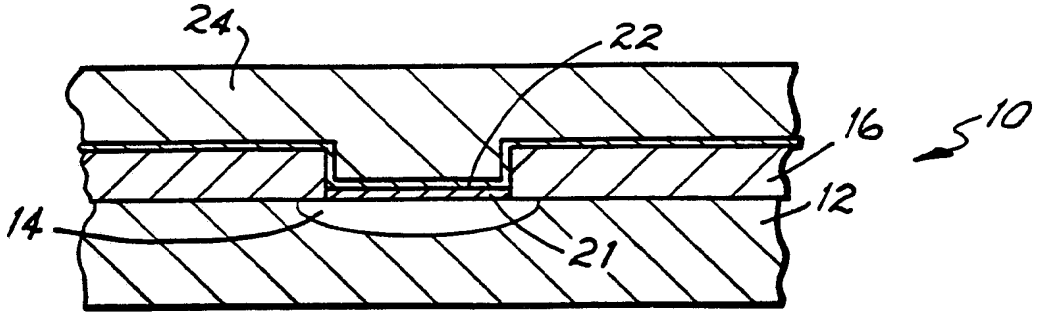
(72) Inventors: EICHMAN, Eric, C. ; 3619 Verdin Road, Phoenix, AZ 85044 (US). MARCUS, Steven, D. ; 3637 West Folley Street, Chandler, AZ 85044 (US). PRICE, J., B. ; 16861 Fillmer Avenue, Los Gatos, CA 95032 (US). BLAIR, James, C. ; 4303 East St. Joseph Way, Phoenix, AZ 85018 (US).

(74) Agents: FREI, Donald, F. et al.; Wood, Herron & Evans, 2700 Carew Tower, Cincinnati, OH 45202 (US).

(81) Designated States: AT, AU, BB, BG, BR, CA, CH, CS, DE, DK, ES, FI, GB, HU, JP, KP, KR, LK, LU, MG, MN, MW, NL, NO, PL, RO, RU, SD, SE, UA, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, SN, TD, TG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: METHOD OF MODIFYING CONTACT RESISTANCE IN SEMICONDUCTOR DEVICES AND ARTICLES PRODUCED THEREBY



(57) Abstract

A method is disclosed for modifying (reducing) the contact resistance in semiconductor devices having doped silicon junctions (14). The method includes selectively depositing a thin film of tungsten (21) on the exposed surface of a silicon wafer substrate (12) which has a native oxide layer thereon. The tungsten reduces or deteriorates the native oxide layer and makes clean contact to the silicon substrate. Subsequently a titanium nitride barrier layer (22) is deposited over the tungsten layer (21). Semiconductor devices produced according to the method of the invention have contact resistance values less than about $5x10^{-7}$ ohm cm^2.

GF Exhibit 1124 - 2394/2704

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria
AU	Australia
BB	Barbados
BE	Belgium
BF	Burkina Faso
BG	Bulgaria
BJ	Benin
BR	Brazil
CA	Canada
CF	Central African Republic
CG	Congo
CH	Switzerland
CI	Côte d'Ivoire
CM	Cameroon
CS	Czechoslovakia
CZ	Czech Republic
DE	Germany
DK	Denmark
ES	Spain
FI	Finland
FR	France
GA	Gabon
GB	United Kingdom
GN	Guinea
GR	Greece
HU	Hungary
IE	Ireland
IT	Italy
JP	Japan
KP	Democratic People's Republic of Korea
KR	Republic of Korea
KZ	Kazakhstan
LI	Liechtenstein
LK	Sri Lanka
LU	Luxembourg
MC	Monaco
MG	Madagascar
ML	Mali
MN	Mongolia
MR	Mauritania
MW	Malawi
NL	Netherlands
NO	Norway
NZ	New Zealand
PL	Poland
PT	Portugal
RO	Romania
RU	Russian Federation
SD	Sudan
SE	Sweden
SK	Slovak Republic
SN	Senegal
SU	Soviet Union
TD	Chad
TG	Togo
UA	Ukraine
US	United States of America
VN	Viet Nam

GF Exhibit 1124 - 2395/2704

METHOD OF MODIFYING CONTACT RESISTANCE IN SEMICONDUCTOR DEVICES AND ARTICLES PRODUCED THEREBY

Field of the Invention

The present invention relates to semiconductor devices and more particularly to a process for improving the contact resistance of doped silicon junctions in semiconductor devices.

Background of the Invention

Semiconductor devices are typically fabricated starting with a substrate, e.g., a silicon wafer, having an insulating dielectric layer such as silicon dioxide on the surface thereof. In many applications, the silicon substrate has contact or junction regions in which the silicon is doped with boron, phosphorous, arsenic, or any other suitable doping compound. The doped contact regions in the substrate are exposed by etching a desired pattern in the oxide layer to form contact or via holes therein. Such etching is performed using etching techniques well known in the art. The contact holes are then filled with a conductor, such as aluminum, to provide electrical contact between the doped regions of the substrate and a conductive film which may be deposited

over the dielectric insulating layer to serve as a low resistance interconnection within the semiconductor device. Such films may be aluminum, doped polycrystalline silicon, tungsten, or another refractory metal.

The deposition of aluminum as the interconnect layer over an oxide insulating layer having contact holes therein has several drawbacks. One of these which is of particular concern is that aluminum diffuses rapidly or "spikes" into the silicon contact or junction regions exposed in the contact holes. As a means for inhibiting aluminum spiking in doped silicon contacts, it is known to deposit a barrier layer in the contact holes over the silicon contacts. One suitable barrier material is titanium nitride (TiN) and it may be deposited by known chemical vapor deposition or sputtering techniques.

The fabrication of semiconductor devices including, among other things, a barrier layer and an interconnect layer, as described above, typically includes as a first step etching the insulating layer to form contact holes therein. Subsequently, the barrier layer is deposited in the contact holes, and thereafter the desired interconnect layer may be deposited. In such fabrication processes, it is imperative that the surfaces upon which the various layers are deposited be free from impurities such as oxide films which form upon exposure to oxygen, i.e.,

native oxide films. The failure to provide clean contact between the layers of conductive material results in undesirably high contact resistance of the semiconductor device at the location of the contact regions. This high contact resistance greatly limits overall device speed and limits the development of higher density semiconductor devices.

Various techniques are known for removing native oxide films prior to performing chemical vapor deposition of subsequent layers over silicon contact regions. For example, U.S. Patent No. 4,902,645 discloses a dry etching treatment in which the native oxide layer is removed by a sputtering process or, alternatively, is etched away using an activated halide in combination with microwaves, high frequency waves, or ultraviolet light. In either case, the native oxide layer and the adjacent oxide insulator layer are both simultaneously etched, which is undesirable in certain circumstances. Furthermore, such processes may require more complicated apparatus to achieve the desired result. U.S. Patent No. 5,023,201 discloses the removal of a native oxide layer on an exposed titanium silicide ($TiSi_2$) surface by exposing that surface to a dilute hydrogen fluoride (HF) acid solution. This method is undesirable where the semiconductor devices being fabricated includes sensitive components and/or materials which are

deleteriously affected by exposure to an acid solution.

There is a need for semiconductor devices which have improved contact resistance and for a process of making such devices wherein native oxides present during fabrication are removed by steps which do not have the drawbacks associated with the prior art methods.

Summary of the Invention

The present invention overcomes the problems of the prior art processes mentioned above and improves the contact resistance of semiconductor devices by removing native oxide layers and providing a low contact resistance intermediary layer prior to depositing a titanium nitride barrier layer and a subsequent conductive interconnect layer thereon.

One aspect of the present invention is directed to a method wherein a thin film of tungsten (W) is selectively deposited by chemical vapor deposition in the contact holes on the exposed doped regions of the semiconductor substrate. These exposed regions will have a native oxide film thereon due to their exposure to oxygen. The thin tungsten film deteriorates the native oxide present on the substrate surface and makes a clean contact to the doped silicon regions. The tungsten is selectively deposited by silane (SiH_4) reduction of tungsten hexafluoride (WF_6) in the presence of a suitable diluent carrier gas such

as hydrogen, nitrogen or argon. This selective tungsten deposition step is preferably carried out at a pressure in the range of 2 to 150 m torr and at a temperature in the range of 240-400°C.

Subsequently, a titanium nitride (TiN) barrier layer is deposited on the exposed surface of the tungsten film in the contact hole. Preferably, the titanium nitride layer is deposited by low pressure chemical vapor deposition utilizing titanium tetrachloride ($TiCl_4$) and ammonia (NH_3) as reactant gases. The deposition of titanium nitride is effected at a temperature in the range of 400-750°C. At this elevated temperature, any tungsten oxides present on the exposed tungsten surface are evolved, resulting in clean contact of the titanium nitride to the tungsten film. Alternatively, the titanium nitride may be deposited utilizing suitable sputtering techniques.

When the method of the present invention is used in connection with substrates having contact regions doped with p-type dopants, the contact resistance of the resulting semiconductor device is less than about $5x10^{-7}$ ohm cm^2. When the method is used in connection with substrates having contact regions doped with n-type dopants, the contact resistance of the resulting semiconductor device is less than about $1x10^{-7}$ ohm cm^2. This represents a substantial reduction in the contact resistance of devices wherein the titanium nitride barrier layer is deposited directly

onto the exposed substrate surface. Such devices have a contact resistance on the order of about $5x10^{-5}$ ohm cm^2. This significant reduction in contact resistance improves the speed at which the ultimate device can be operated.

In another aspect, the present invention encompasses semiconductor devices produced according to the method of this invention. More particularly, the semiconductor devices of this invention include a thin tungsten film deposited on the exposed doped regions of a semiconductor substrate in the contact holes. The tungsten film deteriorates or reduces any native oxide present on the substrate and makes a clean contact thereto. The devices of the invention further include a titanium nitride barrier layer deposited over the thin tungsten film. The titanium nitride barrier layer is deposited on the tungsten film at a sufficiently high temperature such that any tungsten oxides present on the exposed tungsten surface are evolved and the titanium nitride makes a clean contact to the tungsten layer. The device of the invention has significantly reduced contact resistance vis-a-vis prior art devices.

Brief Description of the Drawings

Fig. 1 is a schematic sectional view of a silicon substrate, an etched insulating layer and a native oxide layer on the exposed substrate surface.

Fig. 2 is a schematic sectional view of the silicon substrate of Fig. 1 wherein a thin tungsten film has been deposited in the contact hole.

Fig. 3 is a schematic sectional view of the semiconductor device shown in Fig. 2 wherein a titanium nitride barrier layer has been deposited on the tungsten film and an additional blanket conductor layer has been deposited thereon.

Fig. 4 is a schematic sectional view of an alternative embodiment of the semiconductor device shown in Fig. 3 wherein the titanium nitride barrier layer is a thin blanket layer.

Detailed Description of the Invention

For purposes of illustration and description of the present invention, a basic semiconductor device structure useful in the practice of the present invention will be described. It should be appreciated, however, that various other configurations and/or arrangements can be utilized.

Figure 1 shows a semiconductor device 10 which comprises a substrate 12, which is typically a silicon substrate. Substrate 12 has a plurality (only one shown) of doped contact or junction regions 14, which are formed by techniques well known in the art and which do not form a part of the present invention. Typically, a semiconductor device initially has a continuous dielectric insulating layer 16 formed on the substrate. This dielectric insulating layer may

be a doped or undoped, deposited or grown silicon dioxide insulating layer. Insulating layer 16 is then selectively etched by known techniques to form contact holes 18 (only one shown) in which the doped regions 14 are exposed. Exposure of the device to oxygen oxidizes the silicon substrate and a thin layer of native oxide 20 is formed on the exposed surface of doped regions 14. This native oxide layer 20 must be removed since it increases the contact resistance of the semiconductor device.

In accordance with one aspect of the present invention, native oxide layer 20 is removed or deteriorated by selectively depositing a thin film of tungsten 21 in the contact hole 18 on the surface of the exposed silicon substrate at the location of the doped regions 14. The deposition of tungsten removes the native oxide 20 and forms a clean contact with the doped region 14 of the substrate, as shown in Fig. 2. Deposition of selective tungsten is accomplished by the silane reduction of tungsten hexafluoride in the presence of a diluent carrier gas such as hydrogen, nitrogen or argon at a pressure in the range of 2 to 150 m torr and a temperature in the range of 240-400°C. Preferably, silane is utilized at a flow rate of about 0.5 to 4.0 sccm (standard cubic centimeters), tungsten hexafluoride is utilized at a rate of about 1.0 to 10.0 sccm, and hydrogen is utilized at a flow rate of about 6 to 50 sccm.

Once the thin tungsten film 21 has been deposited, a barrier layer 22 of titanium nitride is deposited by low pressure chemical vapor deposition on the exposed thin tungsten film 21, as shown in Fig. 3. Titanium nitride layer 22 is deposited using known techniques. More particularly, the deposition is effected at a temperature in the range of 400-750°C and at a pressure in the range of about 50-50,000 m torr. By depositing the titanium nitride at this elevated temperature, any tungsten oxides which may have formed on the exposed tungsten surface will be evolved and thus the titanium nitride layer will form a clean contact with the tungsten layer. The titanium nitride deposition preferably utilizes titanium tetrachloride at about 10-30 sccm, ammonia at approximately 100 sccm and argon at approximately 20-30,000 sccm.

The titanium nitride acts as a barrier layer to inhibit aluminum spiking when aluminum is deposited as a blanket conductive interconnect layer 24 on the semiconductor device 10, as shown in Fig. 3. It will be appreciated that other materials may be used for interconnect layer 24, such as tungsten, or other suitable refractory metals. Additionally, the titanium nitride layer 22 may act as an adhesion layer for subsequent blanket tungsten deposition.

In accordance with a further aspect of the present invention, a semiconductor device 10 comprises

a silicon wafer substrate 12, a dielectric insulating layer 16 having at least one contact hole 18 etched therein to expose doped regions 14 of the silicon substrate. The device 10 further comprises a thin film 21 of tungsten selectively deposited by chemical vapor deposition on the exposed substrate surface and making clean contact thereto by the reduction or deterioration of any native oxide layer present. The tungsten layer acts as a low contact resistance intermediary layer. The device further comprises a titanium nitride barrier layer deposited in the contact hole 18 on the exposed surface of the tungsten layer 21. The deposition of the titanium nitride barrier layer is sufficiently high (on the order of 400-750°C) that any tungsten oxides present on the exposed surface of tungsten layer 21 thus are evolved and the titanium nitride makes clean contact to the tungsten layer. The device 10 may further comprise an additional blanket layer 24 of aluminum, tungsten, or any other suitable conductor.

The semiconductor device 10 of the present invention possesses superior contact resistance properties. More particularly, because of the clean contact between the thin tungsten film 21 and the doped region 14 of the silicon substrate 12, together with the clean contact between the titanium nitride layer 22 and the tungsten film 21, the contact resistance of the final product is less than about $5x10^{-7}$

ohm cm^2 in the case of p-type dopants in the silicon substrate, and less than about $1x10^{-7}$ ohm cm^2 in the case of n-type dopants, both of which are significantly lower than prior art devices that may have contact resistance values on the order of $5x10^{-5}$ ohm cm^2.

Fig. 4 shows an alternative embodiment of the semiconductor device of the present invention. In this embodiment, the titanium nitride barrier layer 22 is a thin blanket layer which covers both the dielectric layer 16 as well as the tungsten film 21. The subsequently applied conductor layer 24 covers the titanium nitride layer and fills in the remainder of contact hole 18.

It will be appreciated by persons skilled in the art that various modifications can be made to the method and device of the present invention without departing from the scope of the present invention as defined by the appended claims.

What is claimed is:

1. A method of modifying the contact resistance of wafers used for integrated circuits, comprising the steps of:

selectively depositing, by chemical vapor deposition, a thin film of tungsten on the exposed surface of a silicon wafer substrate having a native oxide layer thereon, whereby said native oxide present on said exposed surface is reduced so that said tungsten film makes clean contact to said substrate; and

depositing, by chemical vapor deposition, a titanium nitride barrier layer over the exposed surface of said tungsten film, wherein said titanium nitride deposition is effected at a sufficiently high temperature to evolve any tungsten oxide present on the exposed tungsten surface so that said titanium nitride layer makes clean contact to said tungsten film.

2. The method of claim 1 wherein said tungsten film is deposited by silane reduction of tungsten hexafluoride in the presence of a carrier gas selected from a group comprising hydrogen, nitrogen and argon.

3. The method of claim 2 wherein said deposition takes place at a temperature in the range of about 240-400°C.

4. The method of claim 3 wherein said deposition takes place at a pressure in the range of about 2-150 m torr.

5. The method of claim 1 wherein said titanium nitride layer is deposited by low pressure chemical vapor deposition utilizing titanium tetrachloride and ammonia as reactant gases.

6. The method of claim 5 wherein said titanium nitride deposition takes place at a temperature in the range of about 400-750°C.

7. The method of claim 6 wherein said titanium nitride deposition takes place at a pressure in the range of about 50 to 50,000 m torr.

8. A method of making wafers used for integrated circuits, said wafers having reduced contact resistance, comprising the steps of:

selectively depositing, by chemical vapor deposition, a thin film of tungsten on the exposed surface of a silicon wafer substrate having a native oxide layer thereon, whereby said native oxide present on said exposed surface is reduced so that said tungsten film makes clean contact to said substrate;

depositing, by chemical vapor deposition, a titanium nitride barrier layer over the exposed surface of said tungsten film, wherein said titanium nitride deposition is effected at a sufficiently high temperature to evolve any tungsten oxide present on the exposed tungsten surface so that said titanium nitride layer makes clean contact to said tungsten film;

whereby the clean contact between said tungsten film and said substrate, and the clean contact between said titanium nitride layer and said tungsten film serve to reduce the contact resistance of said wafer at the location of said tungsten and titanium nitride layers.

9. The method of claim 8 wherein said contact resistance of said wafer is less than about $5x10^{-7}$ ohm cm^2.

10. The method of claim 8 wherein said tungsten film is deposited by silane reduction of tungsten hexafluoride in the presence of a carrier gas selected from a group comprising hydrogen, nitrogen and argon.

11. The method of claim 10 wherein said deposition takes place at a temperature in the range of about 240-400°C.

12. The method of claim 11 wherein said deposition takes place at a pressure in the range of about 2-150 m torr.

13. The method of claim 8 wherein said titanium nitride layer is deposited by low pressure chemical vapor deposition utilizing titanium tetrachloride and ammonia as reactant gases.

14. The method of claim 13 wherein said titanium nitride deposition takes place at a temperature in the range of about 400-750°C.

15. The method of claim 14 wherein said titanium nitride deposition takes place at a pressure in the range of about 50 to 50,000 m torr.

16. A wafer for integrated circuits having reduced contact resistance, comprising:

a substrate;

an insulating layer on one surface of said substrate, said insulating layer having a contact hole formed therein such that a portion of said one surface of said substrate is exposed;

a thin film of tungsten selectively deposited, by chemical vapor deposition, in said contact hole and on said exposed surface of said substrate, whereby any native oxide present on said exposed surface is reduced so that said tungsten film makes clean contact to said substrate; and

a barrier layer of titanium nitride deposited, by chemical vapor deposition, over the exposed surface of said tungsten film, wherein said titanium nitride deposition is effected at a sufficiently high temperature to evolve any tungsten oxide present on said exposed tungsten surface so that said titanium nitride layer makes clean contact to said tungsten film.

17. The wafer of claim 16 wherein said wafer has a contact resistance less than about $5x10^{-7}$ ohm cm^2 at the location of said tungsten and titanium nitride layers.

18. The wafer of claim 17 wherein said substrate is silicon.

19. The wafer of claim 18 wherein said insulating layer is a dielectric insulating layer.

20. The wafer of claim 19 wherein said substrate is doped at the location of the contact hole in said insulating layer.

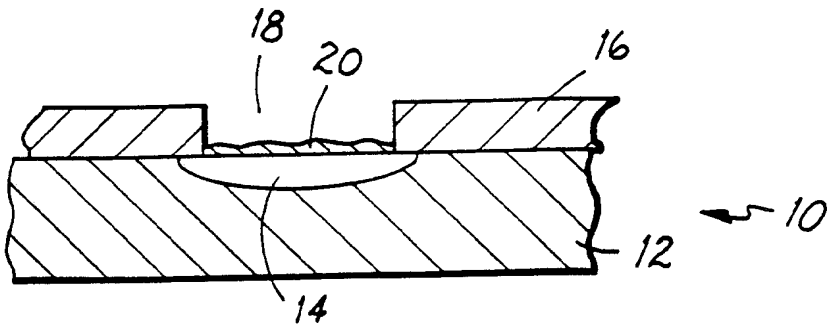


FIG. 1

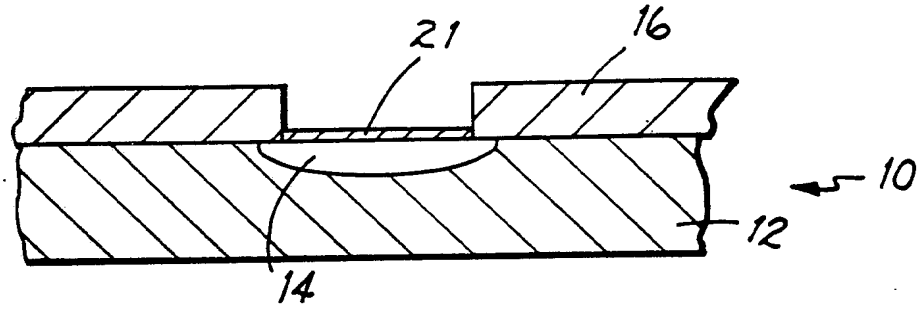


FIG. 2

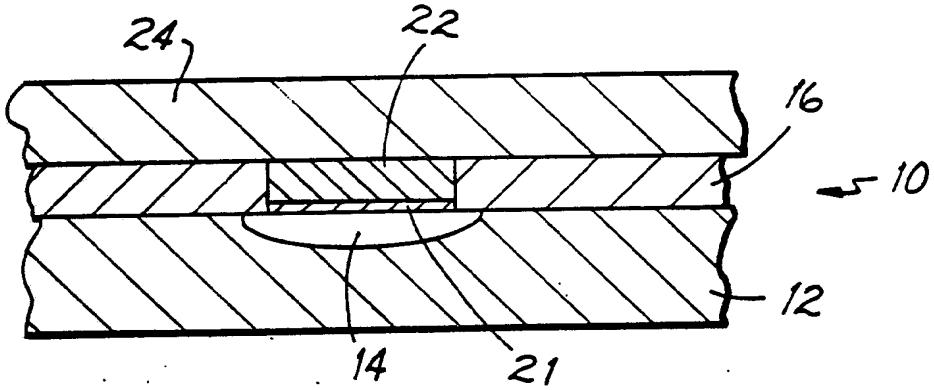


FIG. 3

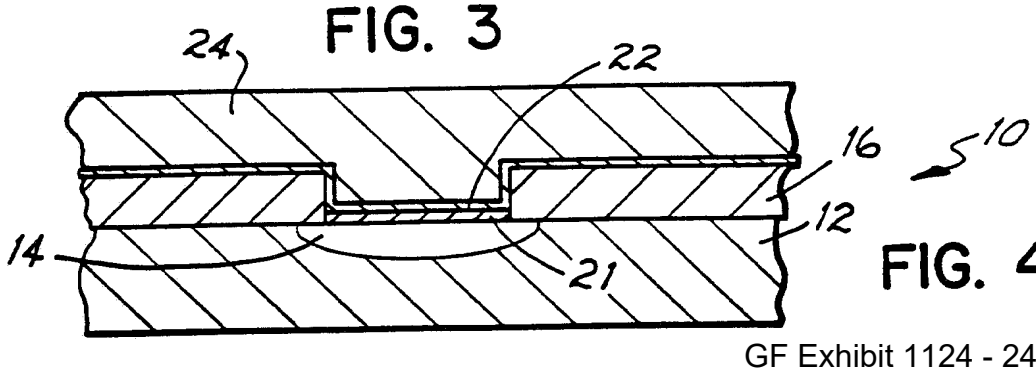


FIG. 4

GF Exhibit 1124 - 2413/2704

INTERNATIONAL SEARCH REPORT

PCT/US 92/10213

International Application No

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H01L21/285

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	H01L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
A	PATENT ABSTRACTS OF JAPAN vol. 014, no. 067 (E-0885)7 February 1990 & JP,A,12 86 447 (MITSUBISHI ELECTRIC CORP.) 17 November 1989 see abstract	1,8,16, 18-20
A	US,A,3 535 176 (P.J.WHORISKEY) 20 October 1970 see column 2, line 9 - line 19	1
A	PATENT ABSTRACTS OF JAPAN vol. 012, no. 425 (E-681)10 November 1988 & JP,A,63 164 242 (FUJITSU LTD) 7 July 1988 see abstract	1
A	EP,A,0 414 267 (APPLIED MATERIALS INC.) 27 February 1991 see column 7, line 28 - line 41	2-3, 10-11

-/--

° Special categories of cited documents :[10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
19 MARCH 1993	29. 03. 93
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	SCHUERMANS N.F.

Form PCT/ISA/210 (second sheet) (January 1985)

GF Exhibit 1124 - 2414/2704

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	US,A,4 897 709 (N.YOKOYAMA ET AL.) 30 January 1990 see column 14, line 10 - line 43	5-6, 13-14

GF Exhibit 1124 - 2415/2704

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO.

US 9210213
SA 68041

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information. 19/03/93

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A-3535176	20-10-70	None		
EP-A-0414267	27-02-91	US-A-	5028565	02-07-91
		JP-A-	3090572	16-04-91
US-A-4897709	30-01-90	JP-A-	1264258	20-10-89

EPO FORM P0479

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

GF Exhibit 1124 - 2416/2704

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H01L 31/0312, 29/22, 31/0256, 31/0296, 21/20

A1

(11) International Publication Number: **WO 95/34095**

(43) International Publication Date: 14 December 1995 (14.12.95)

(21) International Application Number: PCT/US95/06983

(22) International Filing Date: 2 June 1995 (02.06.95)

(30) Priority Data:
253,969 3 June 1994 (03.06.94) US

(71) Applicant: ADVANCED TECHNOLOGY MATERIALS, INC. [US/US]; 7 Commerce Drive, Danbury, CT 06810 (US).

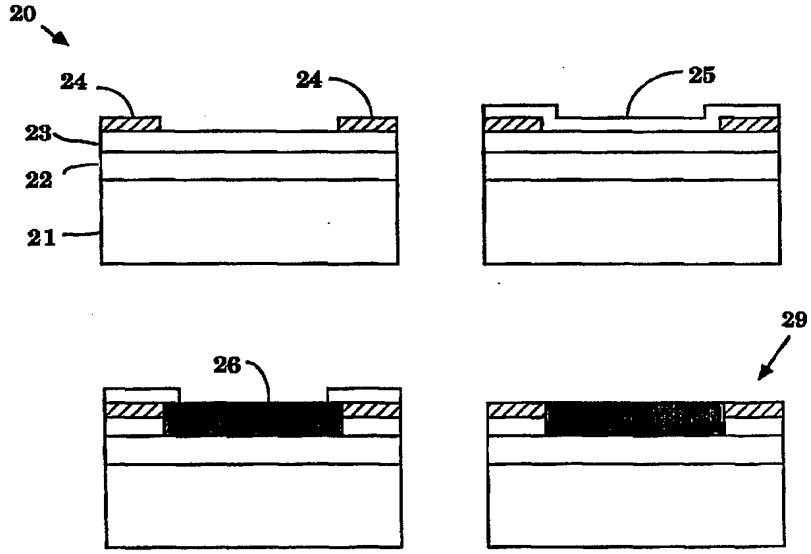
(72) Inventor: TISCHLER, Michael, A.; 83 Barclay Commons, Danbury, CT 06811 (US).

(74) Agent: HULTQUIST, Steven, J.; Intellectual Property/Technology Law, P.O. Box 14329, Research Triangle Park, NC 27709 (US).

(81) Designated States: JP, KR, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: LOW RESISTANCE, STABLE OHMIC CONTACTS TO SILICON CARBIDE, AND METHOD OF MAKING THE SAME



(57) Abstract

Stable, high temperature electrical contacts (29) to silicon carbide formed using a unique silicide formation process that employs a sacrificial silicon layer (23) between the silicon carbide (21) and the contacting metal (25) which forms a metal silicide interlayer (26) providing the resulting contact with low specific contact resistance and high electrical and structural stability. The contact interface is formed by reaction below the semiconductor surface, and thus the in situ silicide formation process is insensitive to surface impurities and oxides and permits the controlled formation of silicides without the formation of excess carbon and carbides at the contact interface. The silicon layer (23) may optionally be doped in situ during growth or implanted with dopants after growth, to lower the contact resistance and enhance its operational stability.

GF Exhibit 1124 - 2417/2704

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	**GB**	United Kingdom	**MR**	Mauritania
AU	Australia	**GE**	Georgia	**MW**	Malawi
BB	Barbados	**GN**	Guinea	**NE**	Niger
BE	Belgium	**GR**	Greece	**NL**	Netherlands
BF	Burkina Faso	**HU**	Hungary	**NO**	Norway
BG	Bulgaria	**IE**	Ireland	**NZ**	New Zealand
BJ	Benin	**IT**	Italy	**PL**	Poland
BR	Brazil	**JP**	Japan	**PT**	Portugal
BY	Belarus	**KE**	Kenya	**RO**	Romania
CA	Canada	**KG**	Kyrgystan	**RU**	Russian Federation
CF	Central African Republic	**KP**	Democratic People's Republic of Korea	**SD**	Sudan
CG	Congo			**SE**	Sweden
CH	Switzerland	**KR**	Republic of Korea	**SI**	Slovenia
CI	Côte d'Ivoire	**KZ**	Kazakhstan	**SK**	Slovakia
CM	Cameroon	**LI**	Liechtenstein	**SN**	Senegal
CN	China	**LK**	Sri Lanka	**TD**	Chad
CS	Czechoslovakia	**LU**	Luxembourg	**TG**	Togo
CZ	Czech Republic	**LV**	Latvia	**TJ**	Tajikistan
DE	Germany	**MC**	Monaco	**TT**	Trinidad and Tobago
DK	Denmark	**MD**	Republic of Moldova	**UA**	Ukraine
ES	Spain	**MG**	Madagascar	**US**	United States of America
FI	Finland	**ML**	Mali	**UZ**	Uzbekistan
FR	France	**MN**	Mongolia	**VN**	Viet Nam
GA	Gabon				

GF Exhibit 1124 - 2418/2704

"LOW RESISTANCE, STABLE OHMIC CONTACTS TO SILCON CARBIDE, AND METHOD OF MAKING THE SAME"

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to electrical contact structures formed between silicon carbide and silicide-forming metals, having low specific resistances and ohmic behavior and long-term electrical and structural stability, and methods for making the same.

Description of the Related Art

An extensive technology of semiconductor devices has been developed based upon the properties of single crystal silicon and other similar materials which may be doped, heat treated, and otherwise processed to produce adjacent layers and regions of varying electronic characteristics. The use of devices produced by silicon technology is generally limited to operation at ambient or, at most, moderately elevated temperatures and in non-corrosive, inert atmospheres. The temperature limitation is a consequence of the small band gap of silicon (1.1. eV), which leads to large leakage currents and device failure at elevated temperatures. In addition, rapid diffusion of dopants and/or impurity species can occur in silicon, which in turn can substantially alter the character of the fabricated semiconductor device. The limitation to relatively inert environments results from the high chemical reactivity of silicon in many corrosive environments, which also can alter the character of the fabricated device. Silicon devices are also limited as to power level, frequency, and radiation tolerance by the materials used therein.

For some applications, the temperature, environmental, and other use limitations on silicon microelectronic devices may be overcome by the use of

proper cooling and packaging techniques. In other applications, these limitations have prevented the use of silicon for integrated circuit technology. For example, in many spacecraft and aircraft applications, elevated temperatures are encountered, and it is not always possible to insure that adequate cooling will be provided. In high power applications, device temperatures can rise to levels which degrade or destroy the device solely through internal heating. Silicon's inability to withstand high temperatures limits the amount of power which can be generated or controlled by silicon electronics. In addition, internal thermal transients in devices otherwise operating at ambient temperature can rapidly destroy the operability of the device unless extensive cooling is provided. Such cooling requires that the device be larger in size than might otherwise be necessary, in part defeating the purpose of the integrated circuit technology.

There has therefore been an ongoing, but as yet not fully successful, search over a period of twenty years to identify and develop a semiconductor technology based in other materials. Such a technology would desirably allow the fabrication of devices for use at higher temperatures such as, for example, the range of at least about 400°C to 600°C, and in applications not amenable to the use of silicon. Because corrosive effects can be greatly accelerated at elevated temperatures and pressures, any such materials and devices must also exhibit excellent corrosion resistance at the elevated use temperatures and over a range of pressures from vacuum to many atmospheres. Some generally desirable characteristics of such materials have been identified, including large band gap, good electrical conductivity, high electric field breakdown strength, low dielectric constant, ability to be doped to produce regions of varying electronic characteristics, a high melting temperature, good strength at operating temperatures, resistance to diffusion by undesired foreign atoms, good thermal conductivity, thermal stability, chemical inertness, and the ability to form stable ohmic and rectifying external contacts.

Silicon carbide has been identified as a candidate material meeting the indicated requirements. Silicon carbide has a high decomposition temperature, good strength, good resistance to radiation damage, and good corrosion resistance in many environments. Silicon carbide has a high breakdown field strength, ten times that of silicon, a relatively large band gap, low dielectric constant, and a thermal conductivity of more than three times that of silicon at ambient

temperature. The diffusion coefficients in silicon carbide are also much smaller than those in silicon or gallium arsenide, and so silicon carbide is resistant to the diffusion of impurity species. Silicon carbide may be processed by several techniques similar to those used in silicon device technology, and in many instances silicon carbide devices may be substituted at moderate and low temperatures for silicon devices. Silicon carbide semiconductor device technology therefore offers the opportunity for supplementing, and in some instances replacing, conventional silicon device technology.

Silicon carbide crystallizes in a cubic polytype as well as numerous hexagonal and rhombohedral polytypes. The 6H-SiC hexagonal polytype is currently the most developed for electronic device applications, but other polytypes, especially the hexagonal 4H-SiC and the cubic 3C-SiC, have also attracted attention for use in high power, high temperature devices. Properties of the 6H polytype are compared with those of silicon and gallium arsenide below. Combined, these advantages in physical and electrical properties predict high maximum acceptable junction temperatures and will allow extremely high power and high temperature operation.

Property	Si	GaAs	6H-SiC
E_g (eV) 300K	1.11	1.43	2.93
Electron mobility (R.T. $cm^2/V\text{-}s$)	1400	8500	400
Hole mobility (R.T. $cm^2/V\text{-}s$)	600	400	40
Breakdown V (E_b, 10^6 V/cm)	0.3	0.4	4.0
Thermal conductivity (W/cm-°C)	1.5	0.5	5.0
Saturated electron drift velocity (10^7 cm/s)	1.0	2.0	2.0
Dielectric constant	11.8	12.8	10.0
Maximum junction temp (°C)	≈200	≈300	≈1000

Silicon carbide in single crystalline form may be prepared by sublimation growth. Silicon carbide epitaxial layers may be formed or deposited by many techniques, including reactive evaporation and chemical vapor deposition (CVD). CVD is a particularly desirable fabrication approach, as it permits the controlled growth of undoped and doped layers and structures of a variety of forms. The layers may be doped in situ by inclusion of dopant species in the source gases of the CVD process, or after growth by implantation. Thus many of the processes for silicon carbide device fabrication are well-known.

Ohmic contacts, important elements of any device, are critical to the performance and stability of high power and high temperature devices. Wide band gap materials, including silicon carbide (SiC), diamond, and the III-V nitrides, currently suffer from a dearth of suitable contact strategies. Contact strategies to date have been fairly conventional, involving implantation, metallization, and deposition of simple silicides directly onto the silicon carbide surface. Although silicon carbide devices have been operated at temperatures as high as 650°C (J.W. Palmour, H.S. Kong and R.F. Davis, Appl. Phys. Lett. **51** (2028 (1987), the contacts have not demonstrated contact resistances comparably low to those achieved in gallium arsenide or silicon, or long term stability.

In addition to the semiconductor material, the entire microelectronic device and package (including metallization) must be suitable for high temperature operation. Stability of the contact is extremely important. Typical projected junction operating temperatures for these devices are as high as 1000°C. High temperature operation exacerbates diffusion; contacts must be designed to remain stable, both structurally and electrically, over the expected life of the device.

In addition to being stable, the contact resistance must be very low. While low contact resistances are desirable in all devices, they are a necessity in high power devices. A high contact resistance will increase the forward voltage drop and thus severely decrease device efficiency. Specific examples of high temperature devices that would desirably be fabricated in silicon carbide include power MOSFETs, thyristors, rectifiers and high frequency devices such as IMPATTs. Today, typical specific contact resistances to SiC are in the range of mid 10^{-5} to 10^{-4} Ω-cm^2. Tomorrow, specific contact resistances need to be in the 10^{-6} Ω-cm^2 range, similar to those attained in GaAs-based materials. Without low resistance contacts, the GaAs devices would not work; an analogous fate will befall SiC devices if low specific contact resistance strategies are not deployed.

A number of metals have been investigated for ohmic contacts to SiC. Typical ohmic contacts to SiC are nickel for n-type contacts and aluminum for p-type contacts. Waldrop and Grant (Appl. Phys. Lett. **56** (1990) 557) have examined additional metals in the as-deposited state; Pd, Au, Co, Ti, Ag and Tb. From the I-V characteristics, Pd, Au and Co are rectifying whereas Ti, Ag, Tb and Al are

"ohmic-like" (essentially linear I-V curve in forward and reverse bias). However, as-deposited metals are not suitable for high temperature contacts – they must be annealed at a temperature higher than their intended operating temperature. During annealing, these metals chemically react with the SiC to produce metal carbides and/or metal silicides, which are stable at the device operating temperatures.

Direct silicide formation on SiC is complicated by the fact that SiC, in addition to silicon, also contains carbon. After annealing, complicated metallurgy at the interface results. For example, annealing Ti on SiC at temperatures between 570-800°C resulted in diffusion of C and Si into the titanium and the formation of TiC and excess silicon (M.B. Chamberlain, Thin Solid Films **72** (1980) 305). No titanium silicides were observed. While TiC is a potential contact, the silicide would be preferred because of its lower sheet resistance. In addition, carbide formation continued for at least 20 hrs at 606°C; clearly not acceptable metallurgy for a stable high temperature contact. Other examples include Mo and Pt on SiC. In the case of Mo, a $Mo_2C/Mo_5Si_3/SiC$ multilayer was observed after annealing (S. Hara et al., Jap. J. Appl. Phys. **29** (1990) L394). Annealing Pt on SiC resulted in a periodic structure consisting of alternating layers of platinum silicides and carbon (T.C. Chou, J. Mater. Res., **5** (1990) 601).

We have demonstrated Ti-based contacts to SiC with specific contact resistances as low as 10^{-4} Ω-cm^2, as well as co-evaporated TiSi contacts which showed resistances as low as ~5 x 10^{-3} Ω-cm^2. These results indicate that co-evaporation is not ideal for deposition of TiSi to produce low resistance contacts. From Chamberlain's results discussed above, it is likely that the actual contact in the Ti case was TiC. More recent results indicate that Ti_5Si_3, as well as TiC, form at the interface between silicon carbide and titanium (L.B. Rowland et al., ONR Workshop on SiC Materials and Devices, September 10-11, 1992, Charlottesville, VA pp. 8). This work used epitaxially deposited Ti, followed by 700°C annealing in vacuum.

Tungsten and tungsten-gold alloys, after annealing at temperatures between 800-1600°C, had contact resistances between 7 x 10^{-4} and 7 x 10^{-5} Ω-cm^2, depending on the SiC carrier concentration (M. Anikin et al., Ioffe Physico-Technical Institute, Academy of Sciences of the USSR, Leningrad). Sputtered and alloyed $TaSi_2$ has been used in devices operating up to 650°C, although no contact

resistances or stability data have been reported (J.W. Palmour, H.S. Kong and R.F. Davis, J. Appl. Phys. 64 (1988) 2168). Nickel has also been used in high temperature devices, but again no data specific to the contacts has been reported (R.F. Davis et al., Proc. IEEE. **79** (1991) 677). It is likely that in this case Ni_2Si was formed, as was reported when nickel was annealed at 600°C on SiC (I. Ohdomari, et al., J. Appl. Phys. **62** (1987) 3747). No carbides were detected, but carbon was distributed uniformly throughout the reacted film. Investigations of platinum silicide indicate that it forms a Schottky contact to SiC (N.A. Papanicolaou et al., J. Appl. Phys. **65** (1989) 3526).

Therefore there is a need for a technology capable of forming stable, low specific resistance contacts to silicon carbide in all of its useful polytypes. Key to making such stable contacts is to understand and control the metallurgy and band structure at the contact interface. In an ohmic contact, the current flow is proportional to the applied voltage, both in sign and magnitude. For a low resistance contact, large currents should be supported without a significant voltage drop across the contact region. Tunneling processes exhibit linearity over a larger range than thermionic or thermionic field emission and thus it is desired that current conduction be dominated by tunneling in a low resistance contact. A large conductance (or small specific contact resistance) is achieved with a heavily doped semiconductor and a small potential energy barrier height. Heavy doping decreases the barrier width, resulting in increased current flow and a lower potential drop across the contact. The depletion region under the contact for heavily doped material is very small, on the order of 100Å for a carrier concentration of 10^{19} cm^{-3}. This means that the heavily doped contact region can be extremely thin. A small barrier height at the contact interfaces facilitates current flow with little resistive loss. The barrier height in the ideal case is determined by the work function of the metal and the electron affinity of the semiconductor. However, because of interface states, the actual barrier height often does not agree with this value.

J.M. Andrews and J.C. Phillips (Phys. Rev. Lett. **35** (1975) 56) correlated the barrier height of a number of silicide-silicon interfaces with the heats of formation of the silicides. Their work clearly showed that those metals which are more reactive with silicon, i.e. form silicides with higher heats of formation, made better ohmic contacts (lower barrier heights). From these results, silicides

of Ni, Co, W, Ta, Ti, Cr, Mo and Zr have been identified as good candidate metals for formation of ohmic contacts to SiC.

One problem observed with all of these contacts is that many phases of metal silicides and carbides are possible. This is because both silicon and carbon are present in SiC. The case is much simpler for contacts to an elemental semiconductor such as silicon or germanium since only one element is available for reaction with the metal.

Accordingly, it is an object of the present invention to provide stable, low resistance ohmic contacts to silicon carbide for use in high temperature, high power devices by controlling the metallurgy of the contact interface through the use of a sacrificial interlayer structure. This interlayer presents only one element to the metal, which greatly simplifies the contact metallurgy. A further object of the invention is to provide methods for fabricating these contact structures.

Other objects and advantages of the present invention will be more fully apparent from the ensuing disclosure and appended claims.

SUMMARY

In one aspect, the present invention relates to stable, high temperature electrical contacts to silicon carbide formed using a unique silicide formation process that employs a sacrificial silicon layer between the silicon carbide and an appropriate contacting metal. The silicon layer reacts with the contacting metal to form a metal silicide interlayer providing the resulting contact with low specific contact resistance and high electrical and structural stability. This "sacrificial" silicon layer permits the controlled formation of silicides without the formation of excess carbon and carbides at the contact interface. These "non-carbonaceous" metal silicide contacts contain less than 5% and preferably less than 1% of carbonaceous species, including free elemental carbon, carbides, or other carbon-containing compounds. Elimination of extraneous species which can diffuse and degrade the contact enhances the long term stability of the contact. The contact interface is formed by reaction below the semiconductor surface, and thus the in-situ silicide formation process is insensitive to surface impurities and oxides.

In another aspect, the invention pertains to stable, high temperature electrical contacts to silicon carbide formed using a silicide formation process that employs a heavily doped sacrificial silicon layer between the silicon carbide and the contacting metal. The doped silicide interlayer provides a diffusion source to heavily dope the semiconductor-silicide interface to further lower contact resistance.

In yet another aspect, the invention pertains to a method of forming stable, high temperature electrical contacts to silicon carbide, wherein a sacrificial layer of silicon is deposited on the silicon carbide surface followed by an overlayer of the contacting metal. Upon annealing at temperatures of 800-1100°C, stable low resistance ohmic contacts are formed. The silicon layer may optionally be doped in situ during growth or doped after growth by implantation, in-diffusion of a deposited layer of dopant species, or other suitable means.

In yet another aspect, the present invention pertains to a method for fabricating self-aligned stable, high temperature electrical contacts to silicon carbide, wherein a sacrificial layer of silicon is deposited on the silicon carbide surface, and a dielectric film (i.e. SiO_2) is deposited and patterned followed by

deposition of an appropriate contact metal. Upon annealing, a silicide forms only where the contact metal touches the silicon layer. The remaining metal on the SiO_2 pattern is then etched off, leaving intact the self-aligned silicide contact, which is much more resistant to the etchant. The silicon layer may optionally be doped in situ during growth or doped after growth.

Other aspects and features of the invention will be more fully apparent from the ensuing disclosure and appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a schematic of the process for fabricating contacts to SiC, wherein a thin silicon layer in grown or deposited on top of the SiC (A), followed by metal deposition (B), and annealing to form the metal silicide (C). Optionally, if the silicon layer is heavily doped, a heavily doped interface region results (D).

Figure 2 shows a schematic wherein the process of the present invention can be used to make self-aligned contacts as well by first depositing and patterning a dielectric film (i.e. SiO_2) prior to metal deposition; upon annealing, a silicide forms only where the metal touches the silicon and the remaining metal on the SiO_2 pattern is then etched off, leaving intact the self-aligned silicide contact, which is much more resistant to the etchant. The remaining silicon layer may be removed if desired.

Figure 3 shows a number of I-V scans for 250 μm diameter nickel contacts to n-doped 6H-SiC annealed for 60 minutes at 900°C, of the same size contacts on different parts of the wafer, with Figure 3A showing scans of 15 contact structures fabricated with a 500Å sacrificial silicon interlayer structure and 3B showing scans of 12 contact structures for a sample fabricated with no silicon interlayer.

Figure 4 shows a number of I-V scans for palladium contacts to n-doped 6H-SiC, with 4A showing scans of five contact structures on different parts of the SiC wafer fabricated employing a 300Å Pd layer over a 600Å silicon interlayer, 40 μm diameter contact annealed at 1050°C for 30 minutes, and 4B showing scans of

eight contact structures fabricated employing a 500Å Pd layer over a 380Å silicon interlayer, 100 μm diameter contact annealed at 1100°C.

DETAILED DESCRIPTION OF THE INVENTION, AND PREFERRED EMBODIMENTS THEREOF

The present invention relates to stable, high temperature electrical contacts to silicon carbide formed using a unique silicide formation process that employs a sacrificial silicon layer between the silicon carbide semiconductor substrate and the contacting metal, wherein the silicon layer reacts with the contacting metal to form a metal silicide. The sacrificial silicon layer may optionally be heavily doped, in order to provide a diffusion source which will, during annealing, diffuse dopant into the immediate contact region and so provide a lower potential energy barrier between the semiconductor and the metal silicide contact. The silicide contact ensures operational stability at high temperatures. In the practice of the present invention, "heavily doped" refers to material that is doped to levels of $\geq 10^{18}$ carriers/cm^3, and preferably to levels $\geq 10^{19}$ carriers/cm^3.

The contact interface is formed by reaction below the semiconductor surface, and thus the process of reaction of the silicon layer with the contact metal to form metal silicide is relatively insensitive to surface impurities and oxides and permits the controlled formation of silicides without the formation of excess carbon and carbides at the contact interface. Elimination of extraneous species which can diffuse and degrade the contact enhances the long term structural and electrical stability of the contact. Because a metal or a metal silicide is not directly deposited upon the silicon carbide, carbides do not form upon annealing. The resulting "non-carbonaceous" metal silicide contacts contain less than 5% and preferably less than 1% of carbonaceous species, including free elemental carbon, carbides, or other carbon-containing compounds.

In addition to forming low resistance contacts, metal silicides useful in the practice of the invention should themselves have low resistivity to reduce parasitic resistances from the interconnects. The resistivities of thin films of various silicides and carbides are listed below:

Silicide	Resistivity ($\mu\Omega$-cm)	Thickness (nm)
PtSi	51	44
Pd_2Si	30	64
WSi_2	70	Thin film
$TaSi_2$	50-55	Thin film
TiC	50	Bulk
NiSi	14	36
$TiSi_2$	17	25
$CoSi_2$	16	29

In many ways, silicides are the ideal contact compounds. They are extremely stable at high temperatures and have low resistances, and, based on the results obtained with silicon semiconductors, have the potential to form contacts with low specific contact resistances. Silicides can be formed between silicon and almost half of the elements in the Periodic Table. Transition metal silicides are of the most interest because of their low resistivities. In addition to low resistivity, the metal silicide should preferably have a high melting point to provide the electrical contact with structural stability at high temperature. A low potential energy barrier between the metal silicide and the silicon carbide substrate is important, and so metal silicides that are known to make ohmic contact with silicon or silicon carbide are good candidate materials for the contacts of the present invention.

Suitable contacting metals for the present invention must form a stable, low resistivity silicide compound as described above. Such metals include the Group 4b, 5b, 6b, 7b, and 8 transition metals of the Periodic Table (CRC Handbook of Chemistry and Physics, 62nd Ed., 1981, CRC Press, Boca Raton, Florida) and their mixtures and alloys. In addition, the metal should form a silicide with a high melting point, greater than 1000°C and preferably greater than 1200°C. Of these metals, Ni, Cr, Pd, Ti, W, Ta, Mo, Co, Zr, and Ti-W alloy are preferred, and Mo, Ta, Ni, Pd, and Ti-W are most preferred.

The present invention provides a contact to SiC using a metal silicide formed in situ. The advantages of this technique include (1) the silicides provide stability at high temperatures, (2) the fabrication process permits self-alignment of the contact. Furthermore, the metal silicide layer may optionally be heavily doped, whereupon it may serve as a diffusion source for diffusing dopants into the contact region. Using the silicide as a diffusion source produces a heavily doped layer at the semiconductor-silicide interface, resulting in low contact resistance. A single dopant may be used to dope both the silicide and the SiC substrate, where such dopant is an effective doping species for both silicon and silicon carbide. Otherwise, two dopants may be used, one to dope the silicide and the other to dope the SiC. For p-type doping, boron can be used to dope both the silicide contact and the SiC substrate. Aluminum may also be used to dope the silicide. For n-type doping, P, As or Sb may be preferably employed to dope the silicide while N may be preferably employed to dope the SiC; As and Sb may be employed to dope both the silicide and the SiC.

The dopant may be implanted directly into the silicide. Co-doping during silicon growth, or during metal or silicide deposition may also be employed. To summarize, the doping may be accomplished using the following approaches:

1. After the metal is deposited, the structure may be implanted with the appropriate dopant. Ultra shallow silicide contacts have been formed to silicon by implanting arsenic or boron fluoride in this fashion (H. Jiang et al., J. Electrochem. Soc., **139** (1992), 196). However, implantation may cause damage and requires extra steps.

2. The silicon layer may be co-doped during growth by including the p- or n-type dopant source (e.g., AsH_3, PH_3, B_2H_6, etc.) in the source gas flowing into the CVD reactor. Better control of doping profile is possible via CVD compared to implantation, less damage results to the semiconductor lattice compared to the results from high energy species being implanted.

3. After the (undoped) silicon layer is grown, a thin layer of dopant may be deposited by, for example, sputtering, evaporation, CVD etc.) followed by deposition of the metal layer. The dopant is then diffused into the contact region by annealing. This technique is well-adapted for device fabrication schemes

employing sputtering or evaporation deposition processes. This process is also useful if it is desirable to avoid introducing silicon dopant species into the silicon carbide deposition reactor.

The advantages of doping the SiC-silicide interface from the silicide over conventional implantation into the interface are that (1) fewer process steps are required, (2) implantation damage in the SiC is eliminated, and (3) very shallow junctions can be formed.

The diffusion coefficients in SiC are very small, on the order of 10^{-13} to 10^{-16} cm^2/second at 1400°C (*Technology of Si, Ge and SiC*, subvolume C, Landolt-Bornstein, v. 17, ed. O. Madelung, M. Schulz and H. Weiss, Springer-Verlag, Berlin (1984)). However, as noted above, the thickness of the heavily doped region is very thin, less than 100Å. Thus annealing the silicon carbide / doped silicon / contact metal structure at temperatures near the epitaxial growth temperature of SiC (1400°C) for about 1 hour provides enough diffusion to form the required low resistance silicide contact structure.

The silicides are fabricated using a novel technique to prevent the formation of excess carbon or carbides at the SiC-contact interface, thus enhancing the thermal stability of the contact by eliminating extraneous species which could diffuse and degrade the contact. A thin silicon layer, optionally heavily doped, is grown on top of the SiC, followed by metal deposition on top of the silicon layer and annealing. A schematic of the process for fabricating contacts with this technique is shown in Figure 1. The structure 10 consists of a SiC substrate 11 on a surface of which is formed a heavily doped SiC contact layer 12 followed by a thin sacrificial silicon layer 13 (Figure 1A). In an actual device, these layers would be the last to be grown. Silicon is easily grown by simply turning off the carbon source in a SiC CVD growth reactor; or alternatively the silicon layer may be deposited by sputtering or evaporation. The silicon layer may be doped during or after growth to achieve even lower resistances in the metal silicide contact. After growth of the device and contact layers (heavily doped SiC followed by silicon), the metal layer 14 is deposited (Figure 1B), by sputtering, evaporation, CVD or any suitable technique. The silicide is then formed by annealing structure 17 in an inert ambient (Figure 1C), whereupon the metal and silicon layers react in situ to

form a metal silicide. These steps may optionally include introduction of a dopant, and annealing to diffuse the dopant to the SiC interface (Figure 1D).

It should be noted that this process can be used to make self-aligned contacts as well by first depositing and patterning a dielectric film (for example, SiO_2, silicon nitride, silicon oxynitride) prior to metal deposition. Upon annealing, a silicide forms only where the metal touches the silicon. The remaining metal on the dielectric pattern is then etched off, leaving intact the self-aligned silicide contact, which is much more resistant to the etchant. In addition, the deposited silicon (especially if it is undoped) and dielectric act as passivants for the SiC surface.

The steps for fabrication of such self-aligned contacts are shown schematically in Figure 2. Structure 20 in Figure 2A comprises a SiC substrate 21 on a surface of which is formed a heavily doped SiC contact layer 22 followed by a thin sacrificial silicon layer 23, upon which a dielectric masking material 24 such as silicon dioxide, silicon nitride, silicon oxynitride, etc. is deposited and patterned, leaving openings only where the contact is to be formed. The metal layer 25 for the silicide contact is then deposited over the entire sample as shown in Figure 2B. The sample is then annealed (Figure 2C), and the silicide 26 is only formed where the metal is in contact with the silicon interlayer. Finally the remaining metal is removed (Figure 2D) to leave the final self-aligned contact structure 29. The excess metal is typically removed using a wet chemical etch that preferentially etches the metal with respect to the silicide, but other removal techniques such as reactive ion etching, plasma etching, etc. are also possible. The remaining silicon (especially if it is undoped) and dielectric can be left on the sample to act as a passivation for the SiC surface or can optionally be removed, for example by using chemical etches such as HF/water etches for the silicon dioxide and HF/nitric acid etches for the silicon.

The thickness of the deposited silicon layer is selected so that the silicon is the stoichiometrically limiting material in reaction with the subsequently deposited metal to form metal silicide. In this way, excess carbon and carbide do not form, as they do when silicides are directly made on SiC. The amount of metal which should be deposited to consume a given layer of silicon during silicide formation may be calculated on the basis of stoichiometry of the silicide

compound formed and atomic weight and density of the pure metal. The deposited metal thicknesses required to consume a 30 nm layer of silicon during silicide formation are listed below for titanium, cobalt, nickel, and palladium, calculated on the basis of stoichiometry of the silicide compound formed and atomic weight and density of the pure metal:

Metal	Metal Thickness (nm)	Silicide Thickness (nm)
Ti	18	25
Co	8.3	29
Ni	16	36
Pd	45	64

After the deposition steps, the contact structure is typically annealed. It should be noted that annealing is required to form the ohmic silicide contact. If the silicon layer is heavily doped, the annealing step also promotes out-diffusion of the dopant into the immediate contact region to dope the interlayer structure and provide a narrower potential energy barrier. The contact structures may be annealed at 800-1100°C, with 900-1050°C preferred.

The contact structures of the present invention have been characterized based on two major parameters, specific contact resistances and reproducibility of electrical properties. The specific contact resistances to SiC were measured using the method of Cox and Strack (Solid State Electron., **10**, 1213 (1967)). This technique is easy to implement and does not require insulating substrates. Reproducibility was evaluated by recording current-voltage curves for contacts of the same size fabricated at different locations on the SiC wafers.

The features and advantages of the invention are more fully illustrated by the following non-limited examples.

EXAMPLE 1

Nine samples were prepared. First, 0.5 μm of heavily doped (~ 2 x 10^{18} cm^3 nitrogen-doped) n-type 6H-SiC was epitaxially grown by low pressure CVD. The substrates were single crystal 6H-SiC. On samples 2, 3, 5, 6, 8, and 9 a second

layer of silicon was grown on top of the n-type SiC epilayer in situ, without removal from the CVD reactor, by turning off the hydrocarbon source and lowering the reactor temperature to 850°C. All films had a specular appearance. The samples differed in the thicknesses of the silicon layers. Contact resistance patterns were fabricated on the samples by first forming the back contact to the SiC surface and then forming a silicide contact to the front silicon surface. The back contact consisted of a large area nickel ohmic contact that was annealed prior to deposition of the front metal. The front metal was deposited using lift-off lithography and evaporated metal. The diameters of the front contacts varied from 6 to 250 μm. Contact resistances were measured in the as-deposited state and after annealing. The annealing temperatures ranged from 900°C to 1100°C, the annealing time was 60 minutes, and the ambient gas was forming gas (N_2/H_2). The metal thicknesses were chosen to form most of the silicide from the silicon and not from the silicon carbide. Specific contact resistances R_C were measured by the Cox and Strack technique. The results are shown below:

Sample	Si Thickness (Å)	Ni Thickness (Å)	Anneal (°C)	R_C (x10^{-5} Ω-cm^2)
1	0	500	900	11±5
2	300	250	900	18±8
3	600	500	900	3±1.8
4	0	500	1000	5±4
5	300	250	1000	3±2.6
6	600	500	1000	1.3±0.5
7	0	500	1100	1.7±0.5
8	300	250	1100	n.o.*
9	600	500	1100	n.o.

* "n.o." means a non-ohmic contact was formed.

Clearly the samples with the silicon interlayer exhibited lower specific contact resistances. Nickel contacts required annealing to become ohmic. After a 900°C anneal in forming gas, most became ohmic and after annealing at 1000°C, all were ohmic. However, after a 1100°C forming gas anneal, only the large area contacts (>20 μm diameter) in most samples were ohmic. These results indicate that the optimum annealing temperature for nickel contacts is near 1000°C.

Because of the limitations of the Cox and Strack method, it is important to have an additional check on the calculated R_C values. The total resistance values have been measured for the same diameter contacts which have been processed together, with and without the silicon interlayer, as outlined below. Where all other parameters are the same, the contacts with the lowest total resistance will also have the lowest specific contact resistance. In virtually all cases, the samples with the lowest total resistance also have the lowest calculated R_C. Thus even though there may be some small errors in the determination of the absolute R_C values, the silicon interlayer does produce lower resistance contacts in this one-to-one comparison.

Total Resistance (Ω)	**Contact Diameter (μm)**						
Sample (Si thickness, Å)	**100**	**50**	**40**	**30**	**20**	**15**	**12**
1 (0)	16	18.9	21.9	28	41	-	-
2 (300)	22	23.8	26.2	31.2	-	-	-
3 (600)	8.8	12	13.4	15.4	33		
4 (0)	14	18.3	20.9	25.8	32.5	37.2	48
5 (300)	13.2	15.6	20	22	30	36	41
6 (600)	8.8	13	14.1	17.9	27.4	31.3	41.7

In addition to lower contact resistances, the silicon interlayer gave greatly improved reproducibility. Figure 3 shows many I-V scans for 250 μm diameter Ni contacts annealed at 900°C in forming gas for 60 minutes. Figure 3A shows scans of 15 contact structures on different parts of the wafer, fabricated with a 500Å sacrificial silicon interlayer structure, and 3B shows scans of 12 contact structures for a sample fabricated with no silicon interlayer. It is clear that the silicon interlayer greatly increases the reproducibility of the contact resistance.

EXAMPLE 2

Palladium contacts of sizes ranging from 10 μm up to 250 μm in diameter were fabricated to n-type 6H-SiC (nitrogen-doped) by the method described in Example 1, with silicon interlayer thicknesses varying from 300Å to 600Å and Pd

thicknesses of 300Å and 500Å. Annealing was performed in forming gas at temperatures varying from 800 to 1100°C, with the anneal at about 1000°C to 1100°C giving the ohmic contacts of the lowest contact resistances. Specific contact resistances of these were:

Sample	Si Thickness (Å)	Pd Thickness (Å)	Anneal (°C)	R_C (x10^{-5} Ω-cm^2)
10	600	300	1050	2±1
11	300	300	1100	3.5±1
12	380	500	1100	11±1

Figure 4 shows current-voltage scans of palladium contacts on n-doped 6H-SiC, with 4A showing scans of five contact structures on different parts of the SiC wafer fabricated employing a 300Å Pd layer over a 600Å silicon interlayer, 40 μm diameter contact annealed at 1050°C for 30 minutes in forming gas (5% H_2 in N_2, and 4B showing current-voltage scans of eight contact structures fabricated employing a 500Å Pd layer over a 380Å silicon interlayer, 100 μm diameter contact annealed at 1100°C for 30 minutes in forming gas.

While the invention has been described herein with reference to specific aspects, features, and embodiments, it will be apparent that other variations, modifications, and embodiments are possible, and all such variations, modifications, and embodiments therefore are to be regarded as being within the spirit and scope of the invention.

What is claimed is:

1. An ohmic contact SiC article, comprising:

a SiC base layer; and

a non-carbonaceous metal silicide ohmic contact structure on the SiC layer.

2. An article according to claim 1, further comprising a contact metal overlayer on the non-carbonaceous metal silicide ohmic contact structure.

3. An article according to claim 1, wherein the metal constituent of the metal silicide comprises a material selected from the group consisting of the Group 4b, 5b, 6b, 7b, and 8 transition metals and their mixtures and alloys.

4. An article according to claim 1, wherein the metal constituent of the metal silicide comprises a material selected from the group consisting of nickel, chromium, palladium, titanium, tungsten, tantalum, molybdenum, cobalt, zirconium, and their mixtures and alloys.

5. An article according to claim 1, wherein the metal constituent of the metal silicide comprises a material selected from the group consisting of molybdenum, tantalum, nickel, and titanium-tungsten alloys.

6. An article according to claim 1, wherein the metal silicide has a melting point of at least 1000°C.

7. An article according to claim 1, wherein the non-carbonaceous metal silicide ohmic contact structure comprises a metal silicide selected from the group consisting of platinum silicide, palladium silicide, tungsten silicide, tantalum silicide, nickel silicide, titanium silicide and cobalt silicide.

8. An article according to claim 1, wherein the non-carbonaceous metal silicide ohmic contact structure has been formed in situ by deposition of a silicon layer on the SiC base layer and deposition and deposition of a silicide-forming metal on the

silicon layer, with subsequent reaction of the silicide-forming metal with the silicon layer at sufficient temperature and for sufficient time to form said non-carbonaceous metal silicide ohmic contact structure.

9. An article according to claim 8, wherein the silicon layer comprises a dopant species, and the non-carbonaceous metal silicide ohmic contact structure is correspondingly doped in character.

10. An article according to claim 1, wherein the non-carbonaceous metal silicide ohmic contact structure comprises a material having a resistivity not exceeding 75 micro-ohms-cm.

11. An article according to claim 1, wherein the non-carbonaceous metal silicide ohmic contact structure comprises a material having a resistivity not exceeding 40 micro-ohms-cm.

12. An article according to claim 9, wherein the silicon layer is doped to a level of at least 10^{18} carriers/cm^3, with a dopant species selected from the group consisting of n-type dopant atoms and p-type dopant atoms.

13. An article according to claim 12, wherein the dopant species comprises an n-type dopant species.

14. An article according to claim 13, wherein the n-type dopant species is selected from the group consisting of phosphorus, arsenic, and antimony.

15. An article according to claim 12, wherein the dopant species comprises a p-type dopant species.

16. An article according to claim 15, wherein the p-type dopant species is selected from the group consisting of boron and aluminum.

17. An article according to claim 1, wherein the non-carbonaceous metal silicide ohmic contact structure has a specific contact resistance to SiC of less than about 5×10^{-5} ohm-cm^2.

18. A method of forming ohmic contacts on a SiC substrate, comprising the steps of:

forming a silicon layer on the SiC substrate;

providing a contact metal on the silicon layer; and

annealing the resulting article for sufficient time and at sufficient temperature to form a metal silicide contact by reaction of the silicon layer with the contact metal.

19. A method according to claim 18, wherein the reaction does not comprise the SiC substrate as a reactant.

20. A method according to claim 18, wherein said annealing is carried out at a temperature in the range of from about 800°C to about 1100°C.

21. A method according to claim 18, wherein the silicon layer is doped with a dopant species selected from the group consisting of p-type dopant atoms and n-type dopant atoms, at a doping concentration of at least 10^{18} carriers/cm^3.

22. A method according to claim 18, wherein the SiC substrate is grown by vapor deposition of silicon and carbon source reagents, immediately prior to growth of said silicon layer on the SiC substrate.

23. A method according to claim 22, wherein the SiC substrate is grown for a predetermined time by flowing of silicon-containing source reagent and carbon-containing source reagent to a deposition locus at which said growth is carried out, and wherein the supply of carbon-containing source reagent is discontinued to provide growth of silicon on the SiC substrate.

24. A method according to claim 18, comprising forming self-aligned contacts on the SiC substrate, by depositing and patterning a dielectric material on the SiC substrate prior to deposition of contact metal, so that upon annealing, a metal silicide forms only where the deposited metal contacts the silicon layer, and

etching to remove remaining metal on the patterned dielectric material to leave intact a self-aligned contact.

25. A method according to claim 18, wherein said step of forming the silicon layer on the SiC substrate comprises a forming method selected from the group consisting of chemical vapor deposition, sputtering, and evaporation from a silicon source.

26. A method according to claim 18, wherein the step of providing a contact metal on the silicon layer comprises a provision step selected from the group consisting of chemical vapor deposition, sputtering, and evaporation from a metal source.

27. A method according to claim 18 wherein the silicon layer is doped, by a doping method selected from the group consisting of ion implantation, co-deposition via chemical vapor deposition, sputtering and evaporation.

FIGURE 1

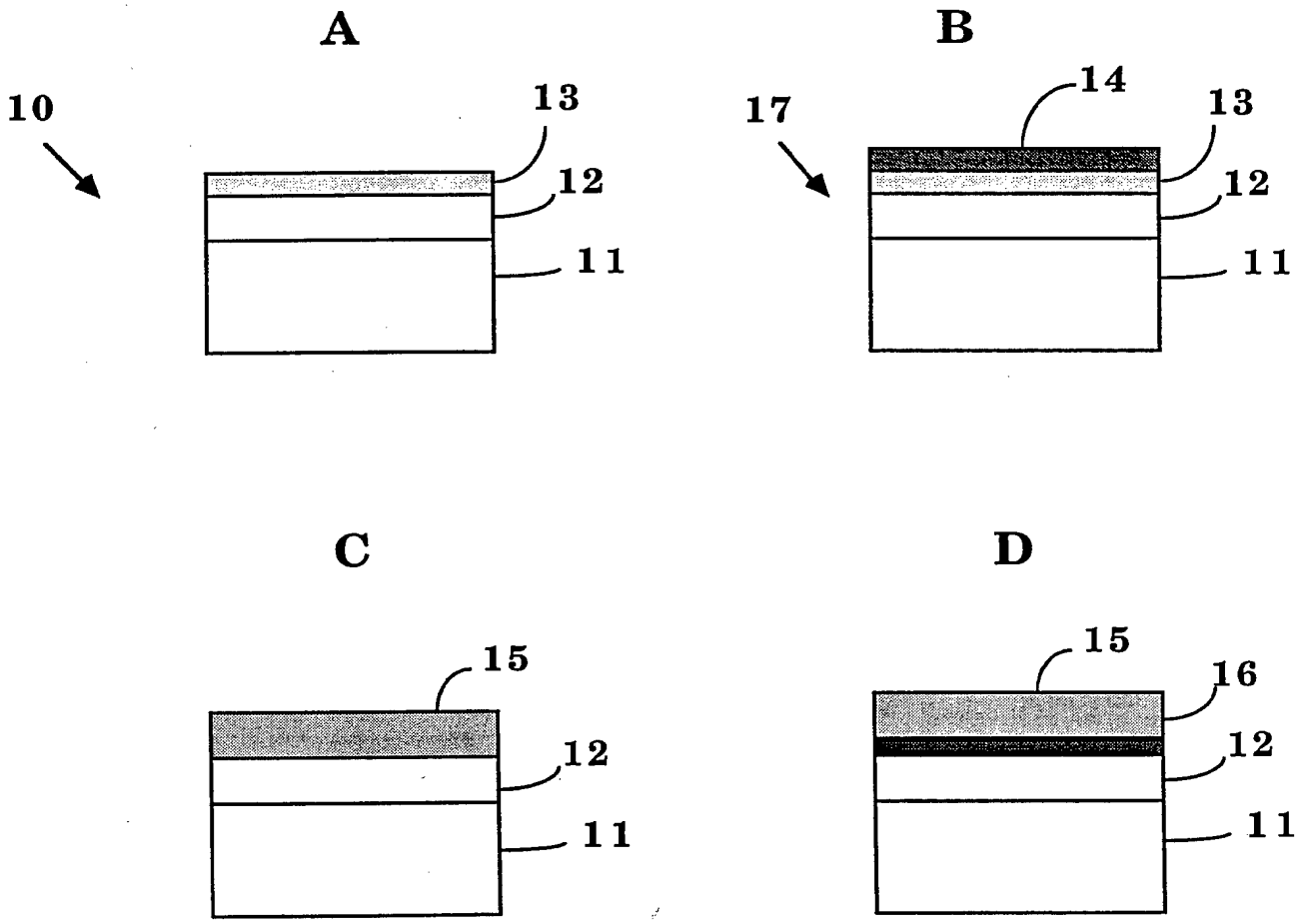


FIGURE 2

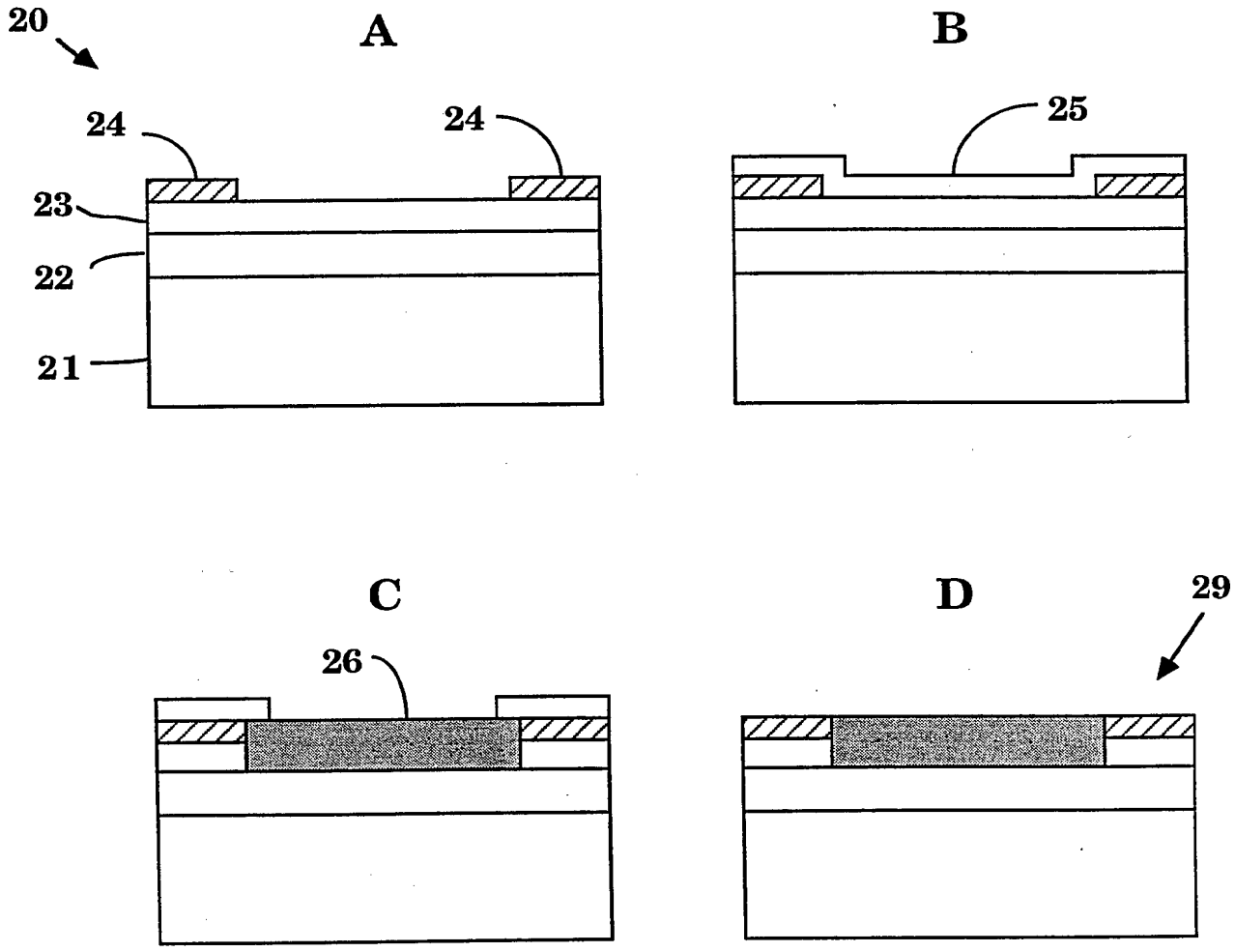
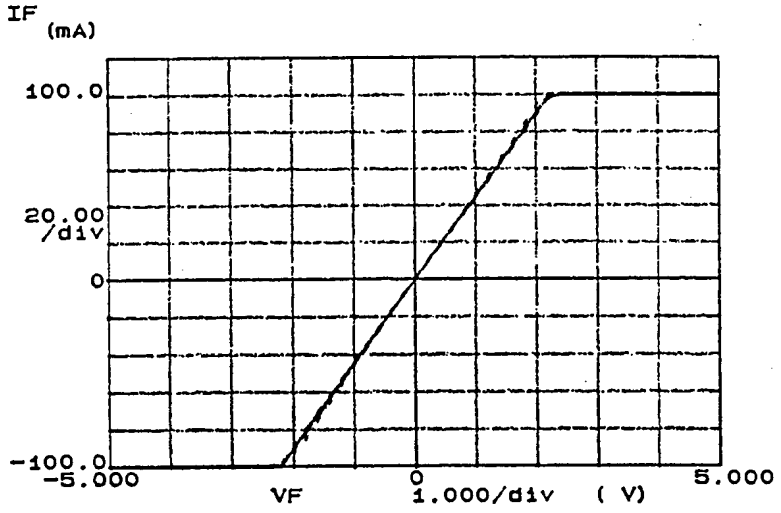


FIGURE 3

A


IF (mA)
100.0
20.00 /div
0
-100.0
-5.000
0
5.000
VF
1.000/div (V)

B

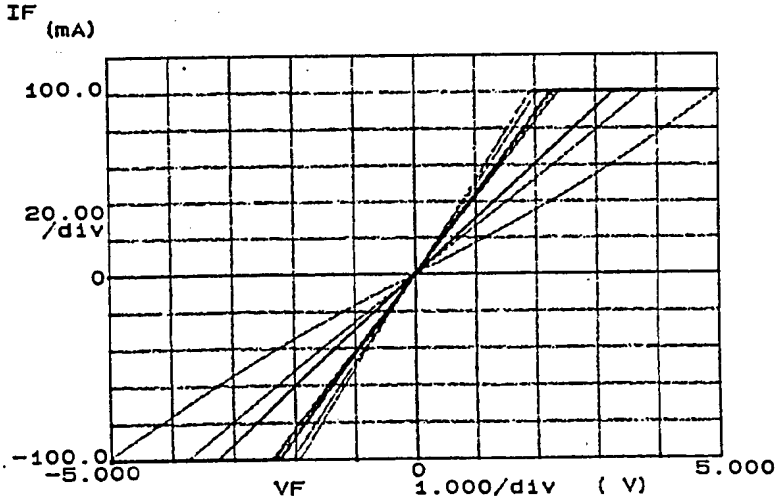
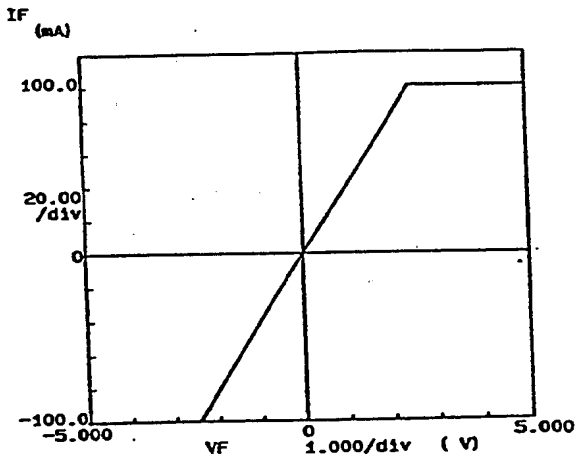
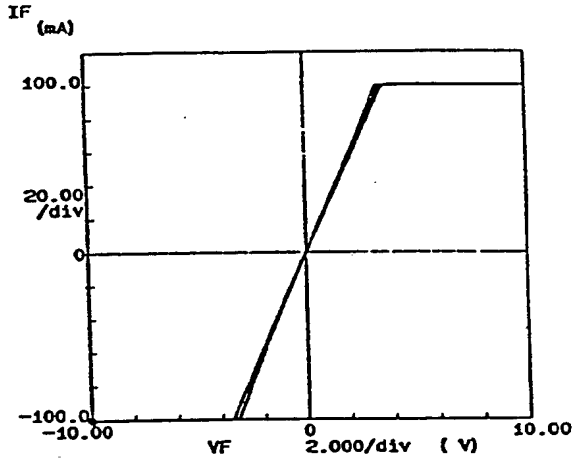

IF (mA)
100.0
20.00 /div
0
-100.0
-5.000
0
5.000
VF
1.000/div (V)

FIGURE 4

A


IF
(mA)
100.0
20.00
/div
0
-100.0
-5.000
VF
0
1.000/div
(V)
5.000

B


IF
(mA)
100.0
20.00
/div
0
-100.0
-10.00
VF
0
2.000/div
(V)
10.00

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/06983

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) : H01L 31/0312, 29/22, 31/0256, 31/0296, 21/20
US CL : 257/77, 78; 437/100
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/77, 78; 437/100

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Journal of Applied Physics, Volume 62, No. 9, issued 01 November 1987, I. Ohdomari et al, "Investigation of thin-film Ni/single-crystal SiC interface reaction", pages 3747-3750, particularly page 3748.	NONE
A	Semicounductor Devices - Physics and Technology, issued 1985, S.M. Sze, page 377.	NONE
A	US, A, 4,875,083 (PALMOUR) 17 October 1989, generally entire document.	NONE
A	Journal of Electrochemical Society, Volume 135, No 2, issued February 1988, J.A. Edmond et al, "Electrical Contacts to Beta Silicon Carbide Thin Films", pages 359-362.	NONE

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search
08 SEPTEMBER 1995

Date of mailing of the international search report
21 SEP 1995

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231
Facsimile No. (703) 305-3230

Authorized officer
STEPHEN MEIER
Telephone No. (703) 308-0956

Form PCT/ISA/210 (second sheet)(July 1992)*

GF Exhibit 1124 - 2445/2704

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/06983

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Japanese Journal of Applied Physics, Volume 29, No. 3, issued March 1990, S. Hara et al, "Solid State Reaction of Mo on Cubic and Hexagonal SiC", pages 395-397.	NONE
A	Journal of Materials Research, Volume 5, No. 12, issued December 1990, V.M. Bermudez et al, "Investigation of the structure and stability of the Pt/SiC(001) interface", pages 2882-2893.	NONE

GF Exhibit 1124 - 2446/2704

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 29/45 // 21/28 — A2

(11) International Publication Number: WO 97/26678

(43) International Publication Date: 24 July 1997 (24.07.97)

(21) International Application Number: PCT/SE97/00062

(22) International Filing Date: 17 January 1997 (17.01.97)

(30) Priority Data:
9600199-5 19 January 1996 (19.01.96) SE

(71) Applicant *(for all designated States except US)*: ABB RESEARCH LTD. [CH/CH]; P.O. Box 8131, CH-8050 Zürich (CH).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: HARRIS, Christopher [GB/SE]; Organistgränd 34, S-191 72 Sollentuna (SE).

(74) Agents: BJERKÉN, Håkan et al.; Bjerkéns Patentbyrå KB, P.O. Box 1274, S-801 37 Gävle (SE).

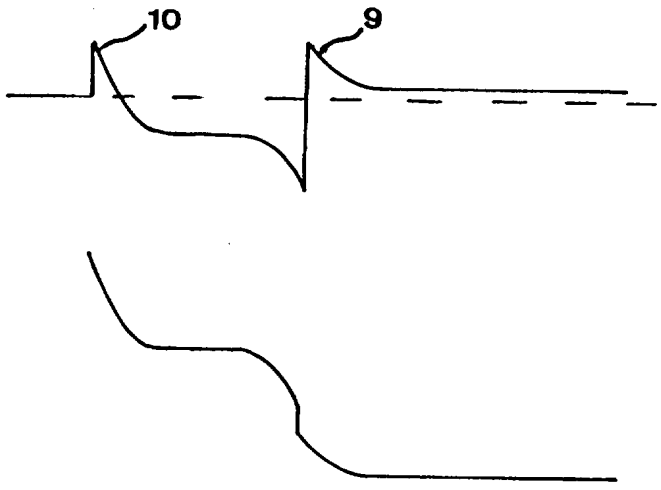
(81) Designated States: JP, US, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: A SEMICONDUCTOR DEVICE WITH A LOW RESISTANCE OHMIC CONTACT BETWEEN A METAL LAYER AND A SiC-LAYER

(57) Abstract

A semiconductor device comprises a semiconductor layer (1) of SiC, a metal layer (2) adapted to form a low resistance ohmic contact with the SiC-layer and a thin layer (3) of a material having a smaller bandgap than the SiC of the SiC-layer placed between the SiC-layer and the metal layer. The SiC-layer is at least in the region next to said thin layer highly doped. The material of said thin layer is a Group 3B-nitride.



GF Exhibit 1124 - 2447/2704

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AM	Armenia	**GB**	United Kingdom	**MW**	Malawi
AT	Austria	**GE**	Georgia	**MX**	Mexico
AU	Australia	**GN**	Guinea	**NE**	Niger
BB	Barbados	**GR**	Greece	**NL**	Netherlands
BE	Belgium	**HU**	Hungary	**NO**	Norway
BF	Burkina Faso	**IE**	Ireland	**NZ**	New Zealand
BG	Bulgaria	**IT**	Italy	**PL**	Poland
BJ	Benin	**JP**	Japan	**PT**	Portugal
BR	Brazil	**KE**	Kenya	**RO**	Romania
BY	Belarus	**KG**	Kyrgystan	**RU**	Russian Federation
CA	Canada	**KP**	Democratic People's Republic of Korea	**SD**	Sudan
CF	Central African Republic			**SE**	Sweden
CG	Congo	**KR**	Republic of Korea	**SG**	Singapore
CH	Switzerland	**KZ**	Kazakhstan	**SI**	Slovenia
CI	Côte d'Ivoire	**LI**	Liechtenstein	**SK**	Slovakia
CM	Cameroon	**LK**	Sri Lanka	**SN**	Senegal
CN	China	**LR**	Liberia	**SZ**	Swaziland
CS	Czechoslovakia	**LT**	Lithuania	**TD**	Chad
CZ	Czech Republic	**LU**	Luxembourg	**TG**	Togo
DE	Germany	**LV**	Latvia	**TJ**	Tajikistan
DK	Denmark	**MC**	Monaco	**TT**	Trinidad and Tobago
EE	Estonia	**MD**	Republic of Moldova	**UA**	Ukraine
ES	Spain	**MG**	Madagascar	**UG**	Uganda
FI	Finland	**ML**	Mali	**US**	United States of America
FR	France	**MN**	Mongolia	**UZ**	Uzbekistan
GA	Gabon	**MR**	Mauritania	**VN**	Viet Nam

GF Exhibit 1124 - 2448/2704

A semiconductor device with a low resistance ohmic contact between a metal layer and a SiC-layer

Technical field of the invention and prior art

The present invention relates to a semiconductor device comprising a semiconductor layer of SiC, a metal layer adapted to form a low resistance ohmic contact with the SiC-layer and a thin layer of a material having a smaller band gap than the SiC of the SiC-layer and placed between the SiC-layer and the metal layer, said SiC-layer being at least in the region next to said thin layer highly doped.

All types of semiconductor devices in which a contact between a metal layer and a SiC-layer is to be formed are comprised, such as for example different types of diodes, transistors and thyristors. Due to the characteristics of SiC such devices are often high power devices.

SiC is a semiconductor material having a large band gap, the magnitude of which is between 2,3 and 3,3 eV dependent on the polytype in question, i.e. the gap between the valence band and the conduction band. For this reason SiC has, in common with other wide band gap semiconductors, the problem that it is extremely difficult to form low resistance ohmic contacts on SiC. One reason for this difficulty is the large difference between the work function of the metal of such a metal layer and the electron affinity of the semiconductor, which results in a large Schottky-barrier height. It has been tried to solve this problem by making a heterojunction

GF Exhibit 1124 - 2449/2704

contact, whereby a material having a lower band gap is grown as an intermediate layer between the metal layer and the wide band gap semiconductor as defined above and as described in U.S. patent 3 984 261. Accordingly, the definition "a metal layer adapted to form a low resistance ohmic contact with the SiC-layer" is to be interpreted broadly and it expresses that there shall be formed a low resistance ohmic contact between a metal layer and a SiC-layer, but this may be done by interposing a thin layer of another material.

The European patent B1 0 249 777 describes how such a heterojunction is used for obtaining a low resistance ohmic contact between a semiconductor material and a metal layer, but the semiconductor is not SiC, but a III-V-material, for instance GaP, which has a considerably lower band gap than SiC.

A known semiconductor device according to the introduction has been suggested (V.A. Dimitriev, K. Irvine, M. Spencer and G. Kelner Appl. Phys. Lett. vol. 64(3) p. 318 (1994)) for 6H SiC, while using the polytype 3C SiC as an intermediate layer, but the disadvantage of this is that the polytype 3C is still a relatively wide band gap material and the contact problem is thus not solved.

Another problem of different materials used so far as intermediate layers in such heterojunctions and also as semiconductors making a direct contact with a metal layer is that the Fermi-level of these materials is pinned as a result of a high density of traps within the band gap of the semiconductor. Typically pinning is due to deep states (traps) and therefore the Fermi-level resides close to the centre of the band gap of the material. These states are for example formed by the deposition of the metal. The pinning is for a narrow region only, in this case the interface between the metal layer and the semiconductor, so that the Fermi-level

GF Exhibit 1124 - 2450/2704

is not "pinned" in the bulk of the semiconductor. Pinning is defined as the phenomena such that the Fermi-energy of the semiconductor is in this single location, i.e. at said interface, fixed at a single energy (the trap energy) independent of the doping condition in the semiconductor. This effect is typically seen between a metal and a semiconductor, for example the III-V compounds, such as GaAs, and results in a large barrier height. It is not observed at the heterojunction between semiconductors provided the interface is of good quality, i.e. of low trap density, and it would accordingly not be present between the SiC-layer and said thin layer in the device defined in the introduction. Normally, it is desired that the work function of the metal in question is matched with the electron affinity of the semiconductor for making a low resistance ohmic contact, but due to said pinning the midgap states in the semiconductor will determine the height of the Schottky-barrier independent of the work function of the metal. This "pinning" phenomena is also there in the semiconductor device according to the European patent B1 0 249 777, but this phenomena is of minor importance, since the band gap of the semiconductors used there is very narrow.

Summary of the invention

The object of the present invention is to provide a semiconductor device according to the introduction, which has an excellent low resistance ohmic contact between the SiC-layer and the metal layer.

This object is in accordance with the invention obtained by making said thin layer of a Group 3B-nitride.

Thus, it has been realised that Group 3B-nitrides do not have pinned (fixed) Fermi-levels at the interface with a metal, which means that the work function of the metal will

determine the Schottky-barrier height, so that it will be possible to choose a suitable metal for a low barrier. Thus, it is possible to form a low resistance ohmic contact between the SiC-layer and a metal layer by choosing a Group 3B-nitride having a smaller bandgap than the SiC of the SiC-layer as a thin layer between the metal layer and the SiC layer. Thanks to the fact that the SiC-layer is highly doped at least in the region next to said thin layer the thin layer may be undoped, since there will due to "modulation doping" be a transfer of charge from the SiC layer having a large band gap to the thin layer having a narrower band gap, so that the narrow band gap material has an excess of charge in the conduction band thereof and will in fact behave as a metal, so that a low resistance ohmic contact may be established without any doping in advance of said thin layer. This means that it will be easier to grow said thin layer of a high quality. Furthermore, it is important that the heterojunction of the device has a high quality so as to avoid traps, i.e. mid gap states, there, and this is obtained thanks to the comparatively good lattice match of the Group 3B-nitrides with SiC.

According to a preferred embodiment of the invention said Group 3B-nitride comprises a content of indium and at least another Group 3B-element. Indium is a suitable element for making the band gap of the Group 3B-nitride narrower than that of SiC of any polytype, so that it is very advantageous to have such content in said Group 3B-nitride. However, it is for the ease of the growth of a high quality thin layer of importance that it also contains at least another Group 3B-element besides indium.

According to another preferred embodiment of the invention said Group 3B-nitride has a content of at least indium and gallium. GaN has a larger band gap than SiC, but it may be easily grown on SiC and thanks to the addition of indium the

band gap is made narrower, so that said Group 3B-nitride may be suited for forming a low resistance ohmic contact aimed at.

According to another preferred embodiment of the invention said Group 3B-nitride is $Ga_{1-x}In_xN$. Such a material for said thin layer has been found to be easy to grow on SiC, have a smaller band gap than SiC and have a not pinned Fermi-level at the interface with a metal.

According to a very preferred embodiment of the invention the indium content of the Group 3B-nitride is adjusted to the metal chosen for matching the electron affinity of said material with the work function of the metal of said metal layer. Thus, the indium content is a parameter easy to handle to adjust the electron affinity of the Group 3B-nitride for matching the work function of the metal of said metal layer for reducing the barrier height of said ohmic contact between the metal layer and said thin layer.

According to a still further, also very preferred embodiment of the invention the indium content of said Group 3B-nitride is adjusted according to the type of doping, p or n, of said SiC-layer. In this way the indium content will be a parameter to adjust the band-alingement according to whether you want a p- or n-type contact. The other Group 3B-element of said Group 3B-nitride may namely have a gap between the conduction band and the valence band which is not centered with respect to the band gap of the SiC of said SiC-layer, so that different concentrations of indium in said Group 3B-nitride may be appropriate depending on the type of doping of the SiC-layer close to the interface to said thin layer. For instance, it is believed that GaN has a band gap centre being displaced with respect to the band gap centre of SiC, which means that different indium-contents may be needed for p- and n-doped SiC-layers.

GF Exhibit 1124 - 2453/2704

According to another preferred embodiment of the invention said thin layer is undoped. The advantages thereof has already been presented above, and the possibility to make this layer undoped is provided by the fact that a modulation doping process takes place thanks to the high doping of the SiC next to said thin layer, the smaller band gap of the thin layer and the fact that the layer really is thin.

Further advantages and preferred features of the invention will appear from the following description and the other dependent claims.

Brief description of the drawings

With reference to the appended drawings, below follows a specific description of a preferred embodiment of the invention cited as an example.

In the drawings:

Fig. 1 is a view illustrating how the extension of the conduction band and the valence band would be in a semiconductor device of the invention from a SiC-layer, a thin Group 3B-nitride layer and a metal layer at a contact of said device if the different layers would not have any influence on each other, and

Fig. 2 is a view corresponding to Fig. 1 but illustrating the real extension of said conduction and valence bands at said contact of the semiconductor device.

Detailed description of a preferred embodiment of the invention

Fig. 1 illustrates a low resistance ohmic contact between a SiC-layer 1 and a metal layer 2 with an intermediate thin layer 3 of a Group 3B-nitride in a semiconductor device. The SiC-layer is a mono-crystalline layer of SiC of any polytype. The Group 3B-nitride is in the present case $Ga_{1-x}In_xN$, in which x is chosen to obtain a smaller bandgap of the Group 3B-nitride than the SiC of the SiC-layer 1 and for obtaining an electron affinity of the Group 3B-nitride matching the work function of the metal selected for said metal layer. The semiconductor device in question may be of any type, such as an IGBT, a GTO and a rectifying diode.

In this way two junctions are formed, a first heterojunction 4 between the SiC-layer 1 and said thin layer 3 and a second junction 5 between the thin layer and the metal layer. The SiC-layer 1 is highly doped with donors at least close to the heterojunction 4, but it would also be possible to highly dope it with acceptors. Highly doped does here mean that the concentration of dopants exceeds 10^{17}, preferably exceeding 10^{18} cm^{-3}. It is very schematically illustrated that the energy gap between the valence band 6 and the conduction band 7 is larger in the SiC layer 1 than in said thin layer 3. In this way a band-offset is obtained at said heterojunction 4. Since the SiC-layer is highly doped with donors these have their extra electrons 8 at a higher energy level than the conduction band level at the other side of the heterojunction, which will result in a fall of said electrons as indicated by the arrow to the lower energy level in said thin layer 3 while ionising said donors and leaving a positive charge 9 in the SiC-layer 1. This technique of providing only the layer with the largest band gap with impurities is called selective doping or modulation doping. In this way an electrical field is created at the

GF Exhibit 1124 - 2455/2704

heterojunction bending the conduction bands in the way shown in Fig. 2. The higher the concentration of donors in the first layer comparatively close to the heterojunction the sharper will the conduction band be bent. Thanks to the high concentration of dopants in the SiC-layer a very narrow barrier 9 will in this way be established between the SiC-layer and said thin layer 3, so that electrons may easily tunnel through this barrier and the resistance of this heterojunction will be neglectable.

The thin layer 3 may be undoped, since the conduction band thereof will in this way by the modulation doping process be filled with electrons, so that this thin layer will act as a metal and have a very low resistance. It would however also be possible to dope the thin layer 3 with the dopant type corresponding to that of the SiC-layer, thus in the case shown in the figures with donors. The layer 3 has to be thin for obtaining this metal behaviour thereof, and thin will in this embodiment mean a thickness below 300Å and in some applications below 100Å. The thin layer 3 is preferably monocrystalline, but it may also be poly-crystalline and still work depending on the influence of the grain boundary.

The Fermi-levels of the different layers have, as known, to be at the same level, which will result in an extension of the conduction band and the valence band in accordance with Fig. 2. It has been found that the Fermi-level of a Group 3B-nitride is not pinned, i.e. fixed, at the interface to a metal, which means that there are relatively few mid gap states (traps) at said interface, which would change the position of the Fermi-level of said thin layer there, so that the barrier 10 then would be much higher. Accordingly, a low resistance ohmic contact between a SiC-layer and a metal layer may be achieved by selecting a Group 3B-nitride as a material for a thin layer between the SiC-layer and the metal layer.

As already mentioned above the mole fraction of In incorporated in said thin layer 3 can be varied to tune the band offset with respect to both the SiC-layer 1 and the metal layer 2. The higher the content of In in the Group 3B-nitride the smaller will the band gap thereof be. GaN has a band gap being slightly larger than most polytypes of SiC and a content of indium therein will reduce this band gap. The band gap of GaN is not centered with respect to the band gap of SiC, so that it will be suitable to choose different concentrations of indium in said Group 3B-nitride according to the type of doping, p or n, of the SiC-layer. Thus, the indium content may vary according to certain considerations, and it will typically be between 5 and 20% of the N content.

A contact of this type may be easily produced by forming the highly doped SiC-layer 1 either by epitaxial growth (CVD, MBE etc.) or by ion implantation. The Group 3B-nitride layer 3 should be of high quality single crystal and should again be grown using an epitaxial technique (CVD, MBE, magnetron sputtering, etc.). Following the deposition of the Group 3B-nitride a metal layer 2 should be deposited by any of the available techniques, said metal being chosen to give a good contact to the Group 3B-nitride. Finally, the layers are patterned using lithography to cover only those areas where a contact is required. The annealing temperature should be low, which means below 1000°C, but in most cases it may be considerably lower. The possibility to not dope said thin layer but nevertheless obtain a low resistance ohmic contact simplifies the production of this contact.

The invention is of course not in any way restricted to the preferred embodiments described above, but many possibilities to modifications thereof will be apparent to a man with ordinary skill in the art.

All definitions concerning the materials of the different device layers do of course include inevitable impurities as well as intentional doping of the layers in question.

The definition layer is to be interpreted broadly and comprises all types of volume extensions and shapes.

Other Group 3B-nitrides than GaInN are also conceivable, such as AlInN, in which case the In-content has to be comparatively high, since AlN has a much higher bandgap than SiC.

The SiC-layer may be of any polytype of SiC, such as for example 6H, 4H, 3C and 15R.

Claims

1. A semiconductor device comprising a semiconductor layer (1) of SiC, a metal layer (2) adapted to form a low resistance ohmic contact with the SiC-layer and a thin layer (3) of a material having a smaller bandgap than the SiC of the SiC-layer and placed between the SiC-layer and the metal layer, said SiC-layer being at least in the region next to said thin layer highly doped, **characterized** in that the material of said thin layer is a Group 3B-nitride.

2. A device according to claim 1, **characterized** in that said Group 3B-nitride comprises a content of indium and at least another Group 3B-element.

3. A device according to claim 2, **characterized** in that said Group 3B-nitride has a content of at least indium and gallium.

4. A device according to claim 3, **characterized** in that said Group 3B-nitride is $Ga_{1-x}In_xN$.

5. A device according to any of claims 2-4, **characterized** in that the indium content of the Group 3B-nitride is adjusted to the metal chosen for matching the electron affinity of said material with the work function of the metal of said metal layer.

6. A device according to any of claims 2-4, **characterized** in that the indium content of said Group 3B-nitride is adjusted according to the type of doping, p or n, of said SiC-layer (1).

7. A device according to any of claims 1-6, **characterized** in that said thin layer (3) is undoped.

GF Exhibit 1124 - 2459/2704

8. A device according to any of claims 1-7, **characterized** in that said thin layer (3) has a thickness below 300 Å.

9. A device according to any of claims 1-8, **characterized** in that said thin layer (3) is a mono-crystalline layer.

10. A device according to any of claims 1-9, **characterized** in that highly doped means a concentration of dopants exceeding 10^{18} cm^{-3}.

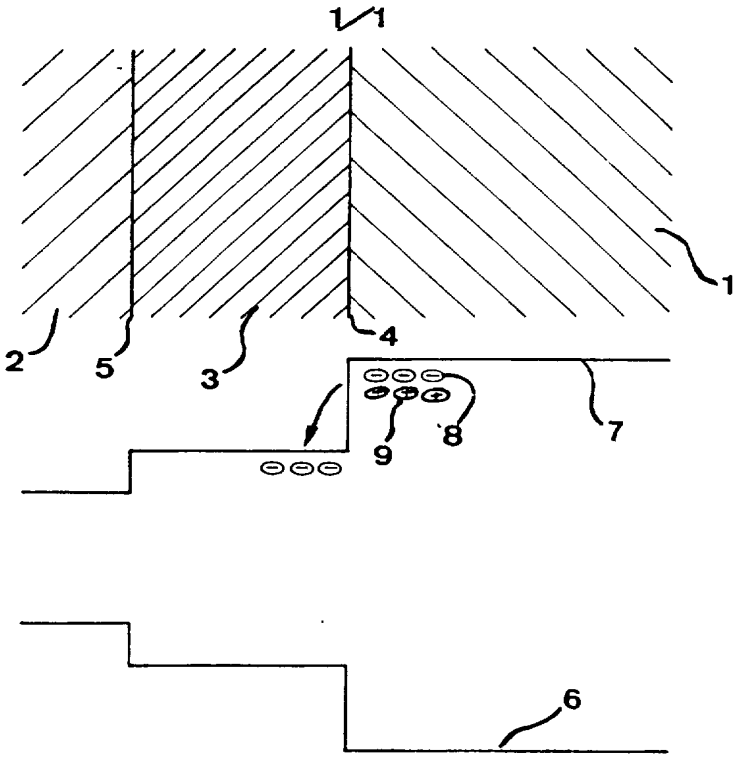


Fig 1

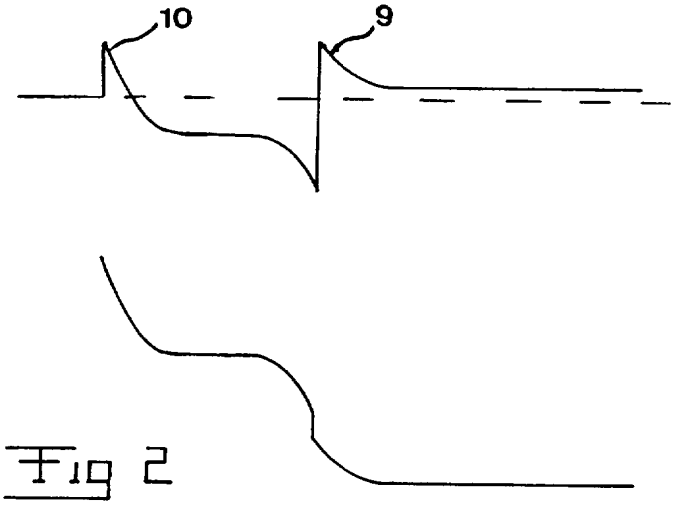


Fig 2

GF Exhibit 1124 - 2461/2704

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H01L 21/283, 21/338, 29/161, 29/45, 29/47, 29/73, 29/812

A1

(11) International Publication Number: **WO 97/33308**

(43) International Publication Date: 12 September 1997 (12.09.97)

(21) International Application Number: PCT/US97/03497

(22) International Filing Date: 4 March 1997 (04.03.97)

(30) Priority Data:
08/612,216 7 March 1996 (07.03.96) US

(60) Parent Application or Grant
(63) Related by Continuation
US 08/612,216 (CIP)
Filed on 7 March 1996 (07.03.96)

(71) Applicant *(for all designated States except US)*: 3C SEMICONDUCTOR CORPORATION [US/US]; Suite 406, 618 N.W. 12th Avenue, Portland, OR 97209-3002 (US).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: PARSONS, James, D. [US/US]; 15900 S.W. Raven Court, Beaverton, OR 97007 (US).

(74) Agents: JOHNSON, Alexander, C., Jr. et al.; Marger, Johnson, McCollom & Stolowitz, P.C., 1030 S.W. Morrison Street, Portland, OR 97205 (US).

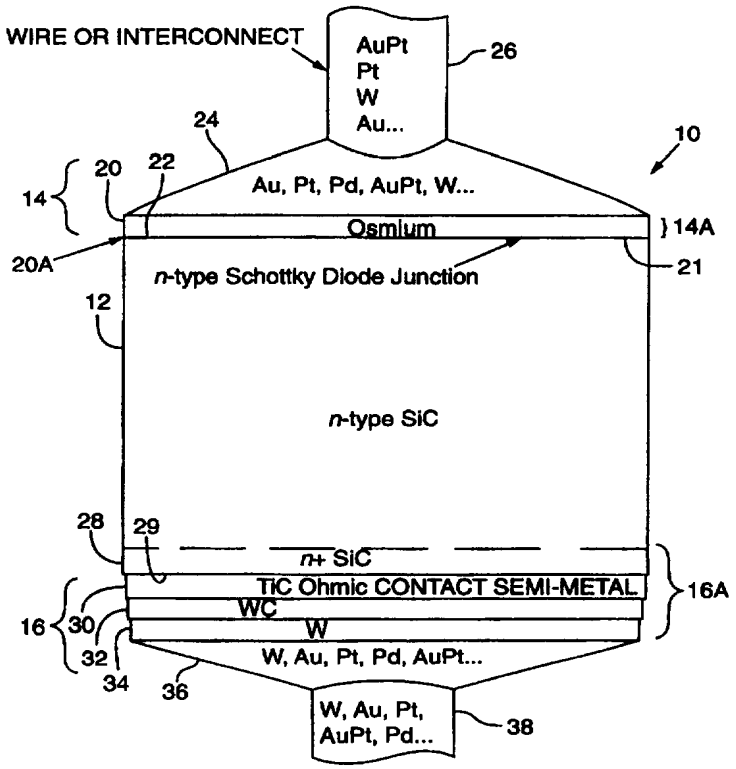
(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ARIPO patent (GH, KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: Os RECTIFYING SCHOTTKY AND OHMIC JUNCTION AND W/WC/TiC OHMIC CONTACTS ON SiC

(57) Abstract

Metallic osmium on SiC (either β or α) forms a contact that remains firmly attached to the SiC surface and forms an effective barrier against diffusion from the conductive metal. On n-type SiC (12), Os (20) forms an abrupt Schottky rectifying junction having essentially unchanged operating characteristics to at least 1050 °C and Schottky diodes that remain operable to 1175 °C and a barrier height over 1.5 eV. On p-type SiC, Os forms an ohmic contact with specific contact resistance of $<10^{-4}$ ohm-cm^2. Ohmic and rectifying contacts to a TiC layer (30) on a SiC substrate (12) are formed by depositing a WC layer (32) over the TiC layer (30), followed by a metallic W layer (34). Such contacts are stable to at least 1150 °C. Electrodes (38) connect to the contacts either directly or via a protective bonding layer (36) such as Pt or PtAu alloy.



GF Exhibit 1124 - 2462/2704

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AM	Armenia	**GB**	United Kingdom	**MW**	Malawi
AT	Austria	**GE**	Georgia	**MX**	Mexico
AU	Australia	**GN**	Guinea	**NE**	Niger
BB	Barbados	**GR**	Greece	**NL**	Netherlands
BE	Belgium	**HU**	Hungary	**NO**	Norway
BF	Burkina Faso	**IE**	Ireland	**NZ**	New Zealand
BG	Bulgaria	**IT**	Italy	**PL**	Poland
BJ	Benin	**JP**	Japan	**PT**	Portugal
BR	Brazil	**KE**	Kenya	**RO**	Romania
BY	Belarus	**KG**	Kyrgystan	**RU**	Russian Federation
CA	Canada	**KP**	Democratic People's Republic of Korea	**SD**	Sudan
CF	Central African Republic			**SE**	Sweden
CG	Congo	**KR**	Republic of Korea	**SG**	Singapore
CH	Switzerland	**KZ**	Kazakhstan	**SI**	Slovenia
CI	Côte d'Ivoire	**LI**	Liechtenstein	**SK**	Slovakia
CM	Cameroon	**LK**	Sri Lanka	**SN**	Senegal
CN	China	**LR**	Liberia	**SZ**	Swaziland
CS	Czechoslovakia	**LT**	Lithuania	**TD**	Chad
CZ	Czech Republic	**LU**	Luxembourg	**TG**	Togo
DE	Germany	**LV**	Latvia	**TJ**	Tajikistan
DK	Denmark	**MC**	Monaco	**TT**	Trinidad and Tobago
EE	Estonia	**MD**	Republic of Moldova	**UA**	Ukraine
ES	Spain	**MG**	Madagascar	**UG**	Uganda
FI	Finland	**ML**	Mali	**US**	United States of America
FR	France	**MN**	Mongolia	**UZ**	Uzbekistan
GA	Gabon	**MR**	Mauritania	**VN**	Viet Nam

GF Exhibit 1124 - 2463/2704

Os RECTIFYING SCHOTTKY AND OHMIC JUNCTION AND W/WC/TiC OHMIC CONTACTS ON SiC

BACKGROUND OF THE INVENTION

This invention relates generally to electrical contacts on SiC-based semiconductor devices. and more particularly to ohmic and rectifying contacts on silicon carbide semiconductors.

SiC possesses tremendous advantages for high temperature and high power solid state electronics. In addition, it offers potential advantages for high frequency and logic circuit applications: e.g., power conversion (mixer diodes, MESFETs), single chip computers (n-MOS, CMOS, bipolar transistors), non-volatile random access memory SiC CCDs can hold charge for more than a thousand years thus, for example, making hard disks a thing of the past.

The potential maximum average power, maximum operating temperature, thermal stability, and the reliability of SiC electronics far exceeds Si or GaAs based electronics. The degree to which these advantages of SiC can be utilized, however, is presently constrained by the thermal stability and electrical properties of the metal/SiC junctions. The primary reasons for this are: (1) the power density of SiC devices is limited by the thermal stability of the ohmic contact junctions, and (2) substantial cooling is required to insure the stability of electrical contact junctions.

For a long time, researchers have been striving without success to develop electrical contacts to silicon carbide trying overcome these constraints. Until these constraints are removed, SiC devices/circuits offer only marginal - if any - advantages over Si and GaAs. Utilization of the full performance potential of SiC itself (for all devices), requires four types of performance-limiting electrical contacts: (1) ohmic to p-type SiC, (2) ohmic to n-type SiC, (3) rectifying to p-type SiC, and (4) rectifying to n-type SiC.

The value of SiC electronics lies in its potential to extend the capabilities of solid state electronics beyond what is possible with Si or GaAs. Thus, suitable electrical contact characteristics obtained in the laboratory - under low stress conditions - must not drift or degrade, due to changes at the metal/SiC junctions, under actual device operating conditions. This requires two additional attributes of metal/SiC electrical contacts. First, the contact metal must form a junction with SiC that is chemically stable to approximately 1000°C (joule heating at high forward current densities in power SiC devices could easily cause metal/SiC junctions to reach such temperatures). Second, the contact metal (or metallization structure) must act as a diffusion barrier to circuit and bonding metals (electrode metals) at the same temperatures. Metal/SiC electrical contacts demonstrated previously do not come close to meeting all these stability requirements.

The best known p-type SiC ohmic contact metallizations demonstrated to date are Al, Al/Ti and Pt (Refs. 2,3).

Although specific contact resistances as low as $1x10^{-5}\Omega \cdot cm^2$ have been reported in laboratory studies, actual SiC devices exhibit p-type contact resistances of $1x10^{-2}\Omega \cdot cm^2$ to $1x10^{-3}\Omega \cdot cm^2$ (Refs 10, 11).

Aluminum and its silicides, and Al/Ti form thermally unstable interfaces with SiC and/or have melting problems (Ref. 12, pg. 2). Platinum reacts with SiC to form many different silicides at temperatures as low as 280°C. At temperatures as low as 400°C, Pt continues to react with SiC until it is entirely consumed by the formation of PtSi (Refs. 4, 5). Thus, Pt cannot protect its contact from circuit and bonding metal diffusion; this characteristic of Pt, in contact with SiC, requires that Pt itself not be used as a circuit or bonding metal. Further, PtSi reacts with virtually all suitable circuit and bonding metallizations at very low temperatures.

Virtually every electronic device -- unipolar or bipolar -- requires n-type ohmic contacts. The most successful n-type SiC ohmic contact metallizations demonstrated to date are Ni and TiC. Both exhibit specific contact resistances between $1x10^{-5}\Omega \cdot cm^2$ and $1x10^{-6}\Omega \cdot cm^2$ (Ni: Ref. 13; TiC: Refs. 7&9). Nickel forms silicides at very low temperatures. Its graded Ni-silicide junction is thermally unstable, and it cannot form a protective diffusion barrier to circuit and bonding metals. Other silicide, nitride, carbide-former, and multilayers of same ohmic contact approaches exhibit stability problems similar to Ni contacts. Transition metal such as Mo and W do not adhere well to SiC surfaces, and they spall at elevated

temperatures.

TiC forms an electrical ohmic contact junction with n-type SiC, that is stable to at least 1400°C (Ref. 14). However, it reacts with all candidate circuit and bonding metals at low temperatures; thus, it cannot form a protective diffusion barrier to circuit and bonding metals.

Low work function metals and semi-metals, that do not react with SiC to form tunnel junctions, can be used to form rectifying electrical contacts to p-type SiC. This type of electrical contact has not been required for SiC devices demonstrated to date; thus, there is little, if any, background literature. We have demonstrated that TiC forms an excellent rectifying contact to p-type SiC, that is stable to at least 1400° C (Ref 14.). However, it reacts with all candidate circuit and bonding metals at low temperatures; thus, it cannot form a protective diffusion barrier to circuit and bonding metals.

The n-type, rectifying Schottky diode is required to modulate the current and voltage in all majority carrier solid state devices. The most important devices of this type are Schottky diodes and MESFETs. Excellent adhesion and abrupt metal-SiC interfaces are cornerstone requirements for this type of contact. Metallizations previously developed for this purpose exhibit various deficiencies. For example, attempts to make thermally stable Schottky rectifying junctions on n-type SiC have been stymied. Many of the metals that are capable of forming such junctions (e.g., Ti, Au/Ti, Pt and PtSi) react with SiC to form silicides at relatively low temperatures,

or--in the case of Au--do not adhere to the SiC surface. The electrical contact junction is thermally unstable, leading to compositional grading of the junction interface at elevated temperatures. This grading effect is exacerbated by the creation of free carbon at the original metal/SiC interface, causing substantial performance degradation, and limiting SiC device operation to well below the capabilities of SiC itself. The (W/Ti, Ti, Au/Ti and Pt)/SiC n-type Schottky junctions demonstrated by Cree Research, N.C. State, NASA Lewis and the Japanese, are unstable at high temperatures or under sustained high current density conditions.

The best rectifying contact metal to n-type SiC, demonstrated to date appears to be W/Ti, extensively tested at the U.S. Army Res. Labs in Adelphi, MD. This contact, however, exhibited unstable leakage-current characteristics, probably due to thermally-driven reactions at the interface. The testing consisted of cycling the junctions between room temperature and 500°C (number of cycles unknown), and measuring the junction reverse leakage current I(L) at room temperature as a function of the number of cycles. During a first series of cycles, I(L) increased. During the next series of cycles, I(L) decreased, reaching a minimum value about 10 μA greater than it was before stress testing was begun. Thereafter, I(L) did not change.

U.S. Pat. No. 2,918,396 to Hall describes formation of rectifying and ohmic contacts on silicon carbide PN diodes and PNP and NPN transistors by alloying two silicon-

acceptor or silicon-donor alloy globules to an N-type or P-type silicon carbide crystal at high temperature, (1700°C). The alloying metals disclosed include aluminum, phosphorus, tungsten, molybdenum or tungsten-molybdenum, with nickel or tungsten conducting electrodes.

U.S. Pat. No. 3,308,356 to Rutz discloses a method of making rectifying contacts to PN junctions in a silicon carbide substrate bonded on one side to a tungsten block by alloying fragments of silicon doped with Ga (P-type) or As (N-type) onto the exposed face of the SiC substrate in a forming gas atmosphere (90% N, 10% H) at high temperature.

U.S. Pat. No. 3,510,733 to Addamiano discloses forming on SiC semiconductor devices electrical leads of an alloy consisting primarily of chromium and nickel, but which can include traces of Si, Fe, C and Fe.

U.S. Pat. No. 4,738,937 to Parsons describes a method of making nonrectifying (ohmic) Schottky contacts on a semiconductor substrate, such as Si or SiC, by epitaxially depositing a metal having suitable work function and lattice parameters, the identified metals including Yb on Si, $NiSi_2$ and ßW on N-type Si, and TiC on N-type ßSiC.

U.S. Pat. No. 5,442,200 to Tischler discloses forming an ohmic contact on a SiC surface by depositing a sacrificial silicon layer followed by a metal (Ni, Cr, Pd, Ti, W, Ta, Mb, Co, Zr or mixtures or alloys thereof to form a noncarbonaceous ohmic contact structure.

U.S. Pat. No. 5,448,081 to Malhi proposes a MOSFET device formed on a SiC substrate, with doped source and

drain regions but does not disclose any means for connecting electrodes to such regions.

U.S. Pat. No. 5,471,072 to Papanicolaou discloses a Pt rectifying contact and a Ti/Au ohmic contact on n-type SiC. Both forms of contacts degrade at high operating temperatures, e.g., subject to catastrophic degradation at over 800°C as disclosed and probably unstable at temperatures of 500°C or less.

Although the semiconductor materials α and ß-SiC have a demonstrated capability for stable, efficient performance at high temperatures, the same is not true of SiC devices/circuits, due to the instabilities of their electrical contact structures.

Also, applicant has learned that a TiC contact on ßSiC does not, by itself, form a diffusion barrier to circuit or bonding metals. Appropriate circuit/bonding metals such as W, Pt, Au and Pd, form intermetallics with TiC. These solid state reactions change the composition of the electrical contact junction, thus degrading it.

Accordingly, a need remains for thermally stable ohmic and rectifying electrical contacts to n-type and p-type SiC.

SUMMARY OF THE INVENTION

It is, therefore, one object of the invention to make an electrical contact to SiC; where, the contact metal exhibits the following properties:

1. Metal/SiC junction stable to over 1000°C,
2. Protects its junction with SiC from circuit and

bonding metal diffusion (forms an electrically transparent diffusion barrier) to >1000°C, and either

3. Forms an ohmic electrical contact to p-type SiC, or
4. Forms rectifying (Schottky) contact to n-type SiC.

Another object of the invention is to form an electrically transparent diffusion barrier (ETDB) for TiC electrical contacts to SiC; where, the ETDB exhibits the following properties:

1. ETDB/TiC junction is stable to over 1000°C,
2. Protects its junction with TiC from circuit and bonding metal diffusion to 1000°C; thereby, also protecting the TiC/SiC junction.

In one aspect of the invention, I have discovered that osmium (Os) forms a rectifying (Schottky) metal junction on n-type SiC semiconductor surfaces, which remains abrupt and firmly attached to at least 1050°C. A thermally stable contact structure is made by forming a metallic osmium layer on the surface of a semiconductive SiC substrate (either ß or α) and connecting a conductive metal electrode to the osmium layer through a suitable metal bonding and protective layer, such as Pt or PtAu alloy. The room temperature rectifying characteristics of this structure on n-type SiC are essentially unchanged by annealing at temperatures as high as 1050°C for 2 hours in an inert environment (Ar, hydrogen or vacuum). These junction degrade, but remain operable after annealing for 1 hour at temperatures as high as 1175°C. The resulting barrier height of Os / n-type SiC junctions is 1.78 ± 0.1 ev. Of equal importance, the Os layer forms a diffusion barrier,

which prevents diffusion of electrode metals to the Os/(n-type SiC) junction.

On P-type SiC, the Os layer will form a stable ohmic contact with the lowest specific contact resistance now possible with ohmic contacts to p-type SiC. Stable, low resistance, p-type ohmic contacts are the key to development of all SiC bipolar high temperature power electronics. Forming an Os contact on p-type SiC will provide a lower-energy tunneling barrier and thinner tunnel depth than Pt contacts on p-type SiC.

Os can also be deposited on SiO_2 to form MOS gate structures and field spreading structures. Os on SiO_2 forms a stable interface and has mechanical and thermal properties equal to those of Os on SiC.

Another aspect of the invention, is a method and structure for making an electrically transparent diffusion barrier (ETDB) which shields TiC/SiC junctions from electrode metals to 1150°C, and which forms a metallurgical junction with TiC that remains firmly attached and is stable to 1150°C. The ETDB structure consists of 2 layers: (1) a tungsten carbide (WC) layer in contact with the TiC surface, and (2) a layer of elemental tungsten (W) on the WC surface. This ETDB structure works because W is stable in contact with WC at a temperature greater than 1150°C. The TiC/SiC junction remains stable because W does not react with WC to form W_2C in this temperature range (unlike all other transition metals in contact with their mono-carbides). Thus, a concentration gradient to drive diffusion between the WC/TiC, and thus, TiC/SiC interfaces

does not exist. 1.78Elemental W is the actual diffusion barrier. It forms a bond with potential electrode metals because of solid solubility which increases with increasing temperature. Once "formed", the thin bonding layer is absolutely stable at or below the forming temperature. Electrodes can then be freely connected to this contact layer either directly or though a suitable intermediate bonding layer such as Pt or PtAu alloy. Such contacts are stable to at least 1050°C.

The invention enables fabrication of SiC devices and circuits that will not degrade, or become unstable, under all strain conditions (thermal, electric field, mechanical) for which SiC itself can perform as a semiconductor device. This invention removes all restrictions imposed by metal contacts on the operating envelope of SiC solid state device technology. In particular, it provides rectifying (Schottky) junctions and ohmic contacts that will withstand sustained exposure to temperature as high as 1150°C, and electron migration effects at high electric fields.

Os forms a rectifying Schottky junction to n-type SiC, as do several other metals. Os is set apart from all other metals by the following characteristics: (1) it forms an electrically transparent diffusion barrier to 1050° C {which protects the junction from diffusion of electrode metals}, (2) the Os/SiC junction itself remains stable to 1050°C, and (3) the electrical properties of the junction do not change after sustained exposure to temperatures as high as 1050°C. Os will form an ohmic contact junction to p-type SiC exhibiting the same unique stability characteristics

as the n-type SiC rectifying junction.

W/WC is an electrically transparent diffusion barrier, which forms a stable junction with TiC to 1150°C. Its purpose is to protect the chemical and electrical integrity of the TiC/SiC junction. TiC forms ohmic contact junctions to n-type SiC; and rectifying contact junctions to p-type SiC. The TiC/SiC junction, by itself, is stable to temperatures greater than 1400°C.

Based on the foregoing developments, applicant has developed a family of high temperature/power semiconductor devices which satisfy a number of unmet commercial needs. One immediate application is thermal sensors. The invention can be used to make junction or resistive thermistors, that measure temperatures to 1922°F (>1050°C), and 2100°F (1150°C). This development permits SiC thermistors to compete, for the first time, with thermocouples, oxide resistors and pyrometers in the temperature range of 300°F to 2100°F (150°C to 1150°C). It also enables the manufacture of hostile environment transducers, operable at temperatures above 460°F (238°C).

The invention enables making Schottky diodes, PN diodes and transistors as either discrete devices or as components of integrated circuits. Importantly, the invention opens up many potential applications in the power conditioning and conversion field, such as power rectifiers for converting AC power to clean DC power. N-SiC Schottky rectifiers could handle powers nearly as high as the best Si PN junction rectifiers, and PN junction SiC rectifiers could replace vacuum tubes. Other types of devices include

bipolar transistors, thyristors, MOSFETs, MESFETs, IGBTs, and mixer diodes for use in communications, as well as digital and analog to digital electronics.

In summary, all solid state semiconductor devices require one, or more, of the four electrical contacts discussed, which the present invention makes possible.

The foregoing and other objects, features and advantages of the invention will become more readily apparent from the following detailed description of a preferred embodiment of the invention which proceeds with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional diagram of a vertical n-type SiC Schottky diode structure made using prior electrical contacts, showing blurring (interdiffusion) of junctions that results from operation at temperatures greater than 300°C.

FIG. 2 is a cross-sectional diagram of a vertical n-type SiC Schottky diode structure made according to the present invention., as fabricated, and after sustained operation at temperatures up to 1050°C.

FIG. 3 is a cross-sectional diagram of a vertical SiC PN diode structure made according to the present invention.

FIGS. 4A, 4B, 4C, 4D and 4E are cross-sectional views showing the photolithography, Si deposition and osmium deposition and annealing to form a vertical n-type SiC Schottky diode (with electric field spreading SiO_2 ring) on the upper surface of the an n-type SiC substrate, in an Os/SiC n-Schottky diode fabrication process according to

the invention.

FIG. 5 is a top plan view of the diode structure formed by the fabrication process of FIGS. 4A, 4B, 4C, 4D and 4E; and an edge view of the diode structure.

FIG. 6 is a cross-sectional view of the diode of FIG. 5 after applying a platinum layer over the osmium layer.

FIG. 7 is a perspective view of a planar NPN bipolar transistor on a SiC substrate with an Os base contact and W/WC/TiC emitter and collector contacts in accordance with the invention.

FIGS. 8A and 8B are cross-sectional views of two MESFET structures formed on a semi-insulating SiC substrate with an Os/Si gate contact and W/WC/TiC ohmic source and drain contacts in accordance with the invention.

FIGS. 9A and 9B are cross-sectional views of N-channel and P-channel MOSFETs formed on a semiconducting SiC substrate with an Os/oxide gate structure and respective W/WC/TiC or Os ohmic source and drain contacts, in accordance with the invention.

FIGS. 10A and 10B are cross-sectional views of gate controlled thyristor/SCR/IGBT devices with W/WC/TiC, Os and Os-on-oxide contacts in accordance with the invention.

DETAILED DESCRIPTION

Referring to FIG. 1, applicant herein has experimented extensively trying to make devices are cross-sectional views of two versions of MESFET structures formed on a SiC substrate with an Os/Si gate contact and W/WC/TiC source and drain contacts in accordance with the invention.based

on the TiC/SiC metallic/semiconductor combination described in his prior U.S. Pat. No. 4,738,937. FIG.1 illustrates the problems encountered in trying to make contacts to both the upper SiC surface and the lower TiC surface of the structure. Even if the metal layers applied to such surfaces form clean, abrupt interfaces in their as-deposited state, the boundaries of these interfaces blur when the devices are annealed due to diffusion into and/or reactions with: (1) the silicon carbide (top rectifying junction, and (2) the TiC ohmic contact.

Schottky Diode with Os Schottky and TiC/WC/W Ohmic Contacts

Referring to FIG. 2, the present invention is described with reference to the fabrication of a vertical Schottky diode 10 formed on a silicon carbide (SiC) substrate 12, with a Schottky rectifying junction and contact structure 14 formed on an upper side thereof, and an ohmic contact structure 16 formed on an opposite or lower side thereof. The starting material is a single-crystal wafer of uniformly-doped, N-type SiC, designated as substrate 12. First, the n^+-SiC/TiC/WC/W structure 16A is formed (in which TiC = ohmic contact semi-metal; WC/W = ETDB); then, the Schottky rectifying junction and ETDB structure 14A is formed, by the processes described in further detail below together with examples of suitable dimensions of the various layers that form the contact structures. Subsequently, wires may be bonded to the structure to complete contact structures 14 and 16 as shown, or circuit metals may be deposited on and reacted with the ETDB surfaces to complete the structure. In

either case, the resulting contacts will be thermally stable to 1050°C (contact structure 14) and 1150°C (contact structure 16).

The Schottky rectifying junction and ETDB structure 14A preferably comprises a very thin layer 20A of Si (≥ 1 monolayer). The purpose of this layer is to permit Os to bond to the SiC surface 22 without creating a monolayer of free carbon. A layer 20 of osmium then deposited on and in contact with the upper surface 22 of substrate 12. The interface of the osmium layer with substrate 12 forms a Schottky rectifying junction 21, once the structure is annealed ("formed") at a temperature approximately equal to or greater than or 900°C. Preferably, layer 20 consists of elemental osmium (Os), but some impurities can be included, due to mixing of osmium and bonding/circuit metals at the exposed Os surface due to solid solubility, and a few monolayers of OsSi will form between the Os and the SiC when structure 14 is completed.

A metal protective cap and bonding layer 24 is formed on and in contact with the osmium layer 20. A first circuit metallization or wire 26 is electrically and mechanically connected to the upper side of the device 10 via the bonding layer 24. The bonding layer 24 preferably comprises a layer of gold (Au) or gold-platinum (AuPt) alloy, although other known electrical contact metals can be used, in particular tungsten or tungsten-platinum, but any metal selected from a group consisting of Pt, Pd, W, Ti, Hf, Zr, Au, PtAu, V, Cr, Fe, Ni, Cu, Nb, Mo, Tc, Ru, Rh, Ag, Ta, Re, Ir, can be used. The circuit metallization

or wire 26 is preferably tungsten (W), although an alloy of tungsten can also be used, as well as other metals compatible with the bonding metals and intended operating temperatures and environments. The use of Os removes all restrictions on the bonding/circuit metal type, method of application and the bond "forming" temperature.

The ohmic contact structure 16 on the underside of the substrate 12 includes a tungsten carbide (WC) layer 32 deposited on the TiC layer 30. Preferably, the structure of the Schottky diode 10 includes an n+ doped SiC layer 28 on the underside of the n-type substrate, with the TiC layer 30 contacting the lower surface 29 of layer 28 to form an ohmic contact. Tungsten carbide layer 32 covers the TiC layer 30 and a layer 34 elemental tungsten(W) is in turn deposited on the WC layer 32. A bonding layer 36 on the tungsten layer 34 connects a second circuit metallization or wire 38 to the device. The bonding layer 36 is preferably of PdAu or PtAu, but could alternatively be made of W, Pt, Pd, Au, or any other compatible electrical contact metals. The wire 38 is preferably tungsten but could alternatively be Pt, PtAu, Au, Pd or other compatible metals.

This structure forms a highly stable Schottky diode which remains stable under high temperature conditions, over 1050°C without discernible changes in I-V characteristics, and operative as a Schottky diode after annealing at temperatures up to about 1175°C.

Using elemental osmium to form the Schottky junction and ETDB structure 14A on N-type SiC ($n \leq 1x10^{18}cm^{-3}$)

produces the highest known barrier height: 1.78 ± 0.1 electron volts, as compared to a range of 1.1 to 1.2 ev. for prior Schottky junctions in SiC. The Os/n-SiC junctions will block substantially higher voltages than possible with any other known metal.

The physical properties of the Os/SiC interface are also advantageous, with good interface adhesion and expansion coefficient mismatch characteristics that will readily exceed device/circuit requirements, and so does not spall. The osmium film remains smooth after annealing, and does not scratch or peel. The osmium layer additionally provides a diffusion barrier to circuit metallizations that is effective to temperatures of at least 1050°C. Os will form an interface with SiC and a diffusion barrier that is stable over a broader range of thermal, electrical and mechanical stresses than any other known metals. Also, Os does not react with SiO_2, when annealed in H_2 in the absence of oxygen at up to 1050°C. Thus, the use of osmium is compatible with MOS fabrication processes and can readily be used as a gate metal over oxide, as shown in FIGS. 9A and 9B.

The ohmic contact structure 16 with WC layer 32 covering the TiC layer 30 and layer 34 of elemental tungsten (W) on the WC layer 32 forms a highly advantageous ohmic contact on the SiC substrate. It forms an electrically transparent interface to the substrate onto which it is practical to deposit all known electrical contact metals. It provides a very

hard surface as well as an effective diffusion barrier to circuit metallizations to at least 1150°C. It forms a stable interface that does not diffuse into the TiC layer or the SiC substrate, unlike other metals applicant has tried (e.g., Au, Ag, Ti). The W/WC layers form a diffusion barrier which is stable over a broader range of thermal, electrical and mechanical stresses than any other known metals. The WC layer 32 in contact with the TiC layer 30 stabilizes the TiC/SiC junction to about 1150°C. The W layer 34 on the WC layer stabilizes the WC/TiC junction to about 1150°C.

PN Diode with Osmium Ohmic Contact

Referring next to FIG. 3, the invention can also be used to form contacts on semiconductor devices comprising multiple layers of opposite dopant types, such as a vertical pn diode 40. Much of the structure shown in FIG. 3 is similar to that of FIG. 3, so similar reference numerals are used wherever applicable to identify like features already described above. The main difference is that the substrate is doped to form two dopant-type regions or layers, a p-type layer 12A and a n-type layer 12B, interfacing at a pn junction 42. The p-type layer is formed in the upper portion of the substrate to form a nonrectifying ohmic junction 41 at upper surface 22, instead of the Schottky junction described above, and can include a p+ region adjacent surface 22. Another difference between this ohmic contact and ETDB structure 14B and the Os/n-SiC

rectifying Schottky contact and ETDB structure 14A, is that the Si layer is not required in structure 14B. This is because a few monolayers of free carbon at the Os/SiC junction will not have any detrimental effects on the ohmic contact performance.

The ohmic junction 41 between the osmium layer 20 and the p-type SiC material 12A should exhibit a specific contact resistance of 10^{-4} ohm-cm^2 or less. Tests of a statistically significant sample of prototype devices consistently demonstrated low specific contact resistance (high 10^{-5} ohm-cm^2 range for both 4H- and 6H-SiC) of different crystallographic orientations, and thermally stable metal/SiC junction (>1050°C). The diffusion and mechanical properties of Os/SiC ohmic contacts are identical to those of the above-described Schottky contacts.

Description of Schottky Diode Fabrication Process

Following is a description of a process for making a vertical n-type SiC Schottky diode, as shown in FIGS. 5 and 6, with a field spreading ring, as shown in FIGS. 4A, 4B, 4C, 4D, 4E, 5 & 6, starting with a uniformly doped, n-type SiC, single crystal wafer (thickness ≈ 400 μms) as substrate 12. NOTE: the W/WC layers must be deposited and annealed before processing of the Os/n-SiC contact structure begins.

1. Deposit (or ion implant nitrogen and activate) approximately 100 Å to 1,000 Å of n+ SiC on one (bottom) side of substrate 12.

Cold wall chemical vapor deposition (CVD) @ 1400°C in diluent hydrogen.

Reactants: silane and ethylene for SiC growth, and ammonia as the nitrogen source for n-type doping ($n \approx\geq$ 1E18/cc).

No fundamental limit on layer thickness (>0 to ∞).

1A. On the top (opposite) n-type SiC surface, grow native oxide in wet oxygen at 1100-1250°C. Any other oxide formation procedure can be used.

2. Deposit approximately 700 Å of TiC on the n+ SiC (bottom) surface.

CVD @ 1290°C in diluent hydrogen; this temperature anneals the TiC as it is formed.

Reactants: titanium tetrachloride (Ti source) and ethylene (carbon source).

TiC thickness should be less than about 1,800 Å, or it will begin to introduce strain into the SiC layer (Ref. 14).

3. Perform photolithography and oxide etching procedures as shown in FIGS. 4A and 4B to mask the opposite (upper) SiC surface such that an array of circular areas are exposed on the SiC upper surface and each exposed SiC circle is surrounded by an annular oxide ring (the remainder of the

surface is covered with photoresist). The diameters of the exposed SiC circles in experimental devices were 20, 40, 80 and 200 μms.

3B. For the rectifying n-type contact only, we should have RF sputtered a few monolayers of Si on the structure shown in FIG. 4C.

4. Deposit approximately 1,000 Å of Os (>99% purity) on the masked SiC and oxide field ring surfaces. RF sputter deposit Os in a vacuum, as shown in FIG. 4D, after 20 sec. in-situ Ar sputter cleaning of the SiC surface. Note: Os can also be deposited by CVD, DC sputtering or electroplating.
No fundamental limit on layer thickness (>0 to ∞).

5. Remove photoresist mask (lift-off) and clean SiC surface containing circular Os diodes, as shown in FIG. 5.

6. Deposit ~400 Å of WC on TiC surface.
Reactive sputtering: DC sputter W and react with hydrocarbon gas to form WC at the TiC surface.
No fundamental limit on WC thickness (> 0 to ∞).

7. Deposit ~400 Å of W (>96% purity; >99.9% preferred) on WC surface, as shown in FIG. 2.
DC sputtering in vacuum.

8. Deposit ~150 Å Pt (or W, Pd, Au, Cu, Ni, etc.) cap over Os as shown in FIGS. 4E and 6. The cap serves several purposes: (1) protect Os from oxidation (Pt does not oxidize at any temperature, but Os forms a volatile oxide at about 160°C), (2) circuit metal, (3)

part of a bonding layer (electrode).

DC sputtering in vacuum.

9.1 Anneal structure at ≤1150°C, if Os/OsSi/SiC junction is desired.

9.2 Anneal structure at ~1000°C to obtain a thin OsSi layer and a fully formed Os/SiC junction. Annealing at 1000°C bonds Pt cap to Os surfaces to protect Os from oxidation; also bonds W layer to WC layer.

10. Continuation of the structure can be performed by standard techniques.

Description of PN Diode Fabrication Process

Following is a description of the process for fabrication of a vertical p+-n SiC diode as shown in Fig. 3, starting with a uniformly doped, n-type SiC, single crystal wafer (thickness ≈ 400 μms). Photolithography steps to define device shape and field spreading ring can be performed as shown in FIGS. 4A, 4B, 4C, 4D, 4E & 5.

1. Deposit approximately 1,000 Å of p+-SiC on one side.

Cold wall chemical vapor deposition (CVD) @ 1400°C in diluent hydrogen.

Reactants: silane and ethylene for SiC growth, and dimethylaluminum hydride as the A1 source for p-type doping [p ≥ 1E18/cc].

2. Deposit approximately 1,000 A of n+-SiC on opposite side.

Cold wall chemical vapor deposition (CVD) @ 1400°C

in diluent hydrogen. Reactants: silane and ethylene for SiC growth, and ammonia as the nitrogen source for n-type doping [n ≈ 1E18/cc].

No fundamental limit on layer thickness (> 0 to ∞).

3. Deposit approximately 700 Å of TiC on the n+-SiC surface.

CVD @ 1250°C in diluent hydrogen. Reactants: titanium tetrachloride (Ti source) and ethylene (carbon source).

TiC should be less than about 1,800 Å, or it will begin to introduce strain into the SiC layer(Ref. 14).

4. Deposit approximately 1,000 Å of Os on the p+-SiC surface.

DC sputter deposit Os in a vacuum, after 20 sec. in-situ Ar sputter cleaning of the SiC surface.

No fundamental limit on Os layer thickness (> 0 to ∞). Then deposit ~150 Å Pt cap over Os.

CVD or electroplating also can be used.

5. Deposit ~400 Å of WC on TiC surface.

Reactive sputtering: DC sputter W and react with hydrocarbon gas to form WC at the TiC surface.

No fundamental limit on WC thickness (>0 to ∞).

6. Deposit ~400 Å of W on WC surface.

DC sputtering in vacuum.

7. Anneal structure at ≤1150°C.

8. Continuation of the structure can be performed by standard techniques.

Other SiC Devices Using Os and Ti/WC/W Contacts

The basic solid state semiconductor devices used as building blocks for solid state electronic circuits are resistors, diodes, transistors and thyristors. All of these can be made in SiC using the contact structures of the present invention, using the foregoing processes.

RESISTORS:

Majority carrier devices requiring at least two spaced p-type or two spaced n-type ohmic contacts. Examples include varistors and resistance thermistors. A typical lateral form of such devices can be that of the MESFETs further described below with reference to FIGS. 8A and 8B but without a gate contact. Vertical varistors and resistance thermistors can be made in the manner shown in FIG. 2 but with ohmic contacts 16 at both ends.

Applications include temperature transducers operable over temperature ranges from 100°C. to at least 1050°C. for Os ohmic contacts on p-type devices and to 1150°C. for TiC/WC/W ohmic contacts on n-type devices.

DIODES:

Majority carrier diodes (p-type & n-type) require an ohmic and a rectifying metal contact, as described above with reference to FIGS. 2, 5 and 6. Examples include junction thermistors (thermal sensors) mixers (communications), ultrafast recovery (power conditioning), light emitting displays (LEDs).

Minority carrier diodes (p^+n & n^+p and pin) require

both n-type and p-type ohmic contacts, as described above with reference to FIG. 3. The range of applications and types of devices are enormous (see e.g. Sze). Such diodes are used for thermal sensing, power conditioning, power conversion, radiation detection and LED display electronics.

TRANSISTORS:

Bipolar transistors are minority carrier devices with two p-n junctions. They require two n-type and one p-type, or vise-versa, contacts. While the applications range is enormous, bipolar transistors are best known for use in TTL (transistor-transistor-logic). Referring to FIG. 7, an npn bipolar transistor 50 is shown. It includes an Os ohmic contact 52 to the p-type base region 54, preferably capped with Pt as shown in FIG. 6, a TiC/WC/W ohmic contact 56 to the emitter region 60 and a TiC/WC/W ohmic contact 58 to collector region 62 via n+ layer 62.

Unipolar transistors, commonly referred to as MESFETs (metal-semiconductor FETs) are majority carrier devices (usually n-type, but can be p-type). Two such devices are shown in FIGS. 8A and 8B. MESFET 70A in FIG. 8A is formed by diffusing n++ source and drain contact regions 72A, 74A into an n-channel layer 76 epitaxially-deposited on a semi-insulating SiC substrate 78. MESFET 70B in FIG. 8B is formed by epitaxially-depositing an n++ source and drain layer on channel layer 76 on a semi-insulating SiC substrate 78, and then dividing the n++ layer into separate source and drain contact regions 72B, 74B by etching a channel down to layer 76B prior to forming gate structure

82B. The source and drain each use an ohmic contact: in the illustrated example, this is the TiC/WC/W ohmic contact 80, made in the form of the contact structure 16 shown in FIGS. 2 and 3, on the n++ regions 72B, 74B. The gate requires a Schottky rectifying contact 82 which is provided by the Os contact 14 of the form shown in FIG. 6. The gate structure is formed in the same manner as the Schottky contact 14 shown in FIGS 4A-4E. In similar manner, a p-channel MESFET can be formed using p++ source and drain regions, a p-type channel, Os source and drain contact structures, and a TiC/WC/W rectifying gate contact over the p-channel. The MESFET Applications include power conversion (DC to high frequency), generally used for high frequency communications and radar.

MOSFET (depletion & inversion). Requires ohmic contacts to source and drain, parasitic p-n junction and back contact. FIGS. 9A and 9B respectively show n-channel and p-channel MOSFET devices, 88A, 88B. In FIG. 9A, the n-channel device 88A has n-type source and drain regions 90A, 92A formed in a p-type SiC substrate 94A. W/WC/TiC ohmic contacts 96 are formed over regions 90A, 92A, in the manner described above. In the p-channel device 88B, n-type source and drain regions 90B, 92B are formed in a p-type SiC substrate 94B. The source and drain regions 90B, 92B have Os ohmic contacts 98, as described above. In both devices 88A and 88B, the MOSFET gate is formed by a thin oxide layer 97 positioned over the channel between the source and drain regions and covered by a conductive Os layer 99. The use of Os as a gate metal on an oxide layer

could have significant advantages for creating n-channels in p-type SiC. Osmium has good adherence to SiO_2 and is highly conductive.

THYRISTORS (and GTO, IGT, IGBT, etc. devices):

Having three p-n junctions, these devices are typically used for power conditioning. Thyristor structures can requires as many as four ohmic contacts. MOS-gated and IGBT-type devices are essentially thyristors or silicon controlled rectifiers (SCRs) with capacitively coupled control electrodes, i.e. a MOSFET gate, as shown for example, in U.S. Pat. Nos. 3,831,187 to Neilson; 4,199,774 to Plummer; and 4,364,073 to Becke, and further described in Ref. 16. Such devices typically require ohmic contacts to the MOSFET source and drain, and ohmic contacts to the n and p sides of the two non-shorted junctions in order to control the voltage bias and polarity at each junction, as well as a MOS gate.

Examples of such devices are shown in FIGS. 10A and 10B. The illustrated vertical devices 100A, 100B are similar in overall arrangement, both being formed on an n-type SiC substrate 102 with an n+ buffer layer 104 and a p+ anode region 106 and an Os ohmic contact layer 108 capped by a Pt protective bonding layer 110. The MOS-gated structures on the opposite side of the device are also similar, having Ti/WC/W ohmic contacts 112 to the n+ source and drain regions 114 and also forming a tunneling junction short or field emission contact to p+ portions of the base or body regions 116 associated with each region 114. Alternatively, the Ti/WC/W ohmic contacts 112 can be

connected to the n+ source and drain regions 114 alone and an Os ohmic contact portion 112B can be connected to the adjoining P-type base in electrical contact to Ti/WC/W ohmic contacts 112. The MOS gate structure in device 100A is planar, similar to that of FIGS. 9A and 9B, with an oxide layer 118A and a platinum-capped Os electrode layer 120A forming the MOS gate contact. The MOS gate structure in device 100B is recessed in a trench formed between the source and drain regions, with an oxide layer 118B and a platinum-capped Os electrode layer 120B lining the sidewalls of the trench to form the MOS gate contact along the sidewalls adjacent the p-body.

Having described and illustrated the principles of the invention in a preferred embodiment thereof, it should be apparent that the invention can be modified in arrangement and detail without departing from such principles. While the devices shown herein are vertical and lateral devices formed on planar substrates, with the contacts either on both sides or spaced apart on one side of the substrate, other surface arrangements may be used, for example, a V-shaped notch or U-shaped trench, for placement of the claimed contacts. I claim all modifications and variation coming within the spirit and scope of the following claims.

REFERENCES

1. Parsons, J.D.; Wu, J. G.; Chaddha, A.K. and Chen, H-S., "Base for Device Quality β-SiC, "U.S. Pat. No. 5,492,752, issued February 22, 1996.

2. Daimon, H.; Yamanaka, M.; Sakuma, E.; Misawa, S. and Yoshida, S., "Annealing Effects on Al and Al-Si Contacts to 3C-SiC," Japan Jour. Appl. Phys., Vol. 25, No. 7 (1986) L592.

3. Crofton, J.; Barnes, P.A. and Williams, J.R., "Contact resistance measurements on p-type 6H-SiC," Appl. Phys. Lett., Vol. 62, No. 4 (1993) 384.

4. Chen, J.S.; Kolawa, E., Nicolet, M-A.; Ruiz, R.P., Baud, L.; Jaussaud, C. and Madar, R., "Solid-state reaction of Pt thin film with single crystal (001)β-SiC," J. Mater. Res., Vol. 9, No. 3 (1994) 648.

5. Paparicolaou, N.A.; Christou, A. and Gipe, M.L., "Pt and $PtSi_x$ Schottky contacts on n-type β-SiC," J.Appl. Phys., Vol. 65, No. 9 (1988) 3526.

6. Padovani, F.A. and Stratton, R., "Field and Thermionic-Field Emission in Schottky Barriers," Solid St. Elect., Vol. 9 (1966) 695.

7. Parsons, J.D.; Kruaval, G.B. and Chaddha, A.K., "Low specific resistance ($<6x10^{-6}\Omega cm^2$) TiC ohmic contacts to n-type β-SiC," A.P.L., Vol. 65, No. 16 (1994) 2075.

8. Parsons, J.D., "Method of Making Ohmic Contact Structure," U.S. Patent No. 4,738,937 (1988).

9. Chaddha, A.K.; Parsons, J.D. and Kruaval, G.B., "Thermally Stable, Low Specific Resistance ($1.30x10^{-5}\Omega cm^2$) TiC Ohmic Contacts to n-type 6Hα-SiC," A.P.L., Vol. 66,

No. 6 (1995).

10. GE Corporate Research & Development letter dated January 1, 1996, to Director BDMO, DoD.

11. Burke, Terence, Dr., Pulse Power Group, U.S. Army Res. Labs., Ft. Monmouth, NJ, (908) 532-0271/0475 (oral communication).

12. Glass, R.; Palmour, J.W.; Porter, L. and Baumgarner, J., "Platinum Contacts to p-type 6H-SiC" Research report of Cree Research & N.C. State University presented at ARPA-sponsored "Workshop on High Power Electronics" Washington D.D. (Sept. 1995).

13. Kimoto, T., et. al., IEEE Elect. Dev. Let., V. 14, No. 12 (1993) 548.

14. Zhao, Q. H., Parsons, J.D., et al. "Single Crystal Titanium Carbide, Epitaxially Grown on Zincblend and Wurtzite Structures of Silicon Carbide" Materials Research Bulletin, Vol. 30, No. 6, pp 761-769 (1995).

15. Fazi, Chris, Dr., U.S. Army Res. Labs., Adelphi, MD: (301) 394-3011 (oral communication).

16. Baliga, B. Jayant, Modern Power Devices, pages 344-405 (1987).

CLAIMS

1. A SiC semiconductor device comprising:

a semiconductor substrate comprising silicon carbide having a first surface and a second surface, the substrate including a first doped region adjacent the first surface and a second doped region adjacent the second surface;

a first conductive layer comprising metallic osmium (Os) contacting the first surface to form a first contact having an electronic interface to the first region; and

a second layer comprising a metal contacting the second surface to form a second electronic contact to the second doped region.

2. A SiC semiconductor device according to claim 1 in which the first region is doped n-type, and the first contact forms a Schottky junction as said electronic interface.

3. A SiC semiconductor device according to claim 2 in which the first conductive layer includes a thin film of Si or OsSi interfacing the metallic osmium to the first surface of the silicon carbide substrate.

4. A SiC semiconductor device according to claim 1 in which the first and second regions are doped n-type, the first contact forms a Schottky junction and the second contact forms an ohmic junction.

5. A SiC semiconductor device according to claim 4 in which the first and second regions and intervening portions of the substrate are doped n-type, the first contact forms a Schottky junction and the second contact

forms an ohmic junction, so that the device acts as a Schottky diode.

6. A SiC semiconductor device according to claim 1 in which the first region is doped p-type, and the first contact forms an ohmic junction as said electronic interface.

7. A SiC semiconductor device according to claim 6 in which the second region is doped n-type, to form a pn junction at an interface between said regions.

8. A SiC semiconductor device according to claim 7 in which the second layer includes:

a titanium carbide (TiC) layer contacting the second surface;

a tungsten carbide (WC) layer covering the titanium carbide (TiC) layer; and

a layer consisting essentially of elemental tungsten contacting the tungsten carbide (WC) layer.

9. A SiC semiconductor device according to claim 1 in which the first and second regions are doped to a first dopant type and an intervening portion of the substrate is doped to an opposite dopant type to form a first pn junction at an interface adjoining the first region and a second pn junction at an interface adjoining the second region.

10. A SiC semiconductor device according to claim 1 in which the first region is doped to a first dopant type and the second region is doped to a second, opposite dopant type, and an intervening portion of the substrate is doped to form a first pn junction at an interface adjoining the

first region, a second pn junction at an interface adjoining the second region and a third pn junction within the intervening portion.

11. A SiC semiconductor device according to claim 1 including a layer of a protective metal covering the Os first conductive layer, selected from a group of conductive metals that is protective of the Os layer against oxidation and adapted to bond to an osmium surface.

12. A SiC semiconductor device according to claim 1 including a layer of a protective metal selected from a group consisting of Pt, Pd, W, Au, PtAu, Ti, Zr, Hf, V, Cr, Fe, Ni, Cu, Nb, Mo, Tc, Ru, Rh, Ag, Ta, Re, Ir.

13. A SiC semiconductor device according to claim 1 in which the second conductive layer comprises metallic osmium (Os).

14. A SiC semiconductor device according to claim 13 in which the first and second regions and intervening portions of the substrate are doped p-type so that the first contact and the second contact each form an ohmic junction and the device acts as a resistive device.

15. A SiC semiconductor device according to claim 13 in which the first and second regions and an intervening portion of the substrate are doped p-type so that the first contact and the second contact each form an ohmic junction and a gate structure contacts a third surface portion contacting the intervening portion of the substrate so that the device acts as field effect transistor.

16. A SiC semiconductor device according to claim 13 in which the first and second regions of the substrate are doped p-type so that the first contact and the second contact each form an ohmic junction, and an intervening portion of the substrate is doped n-type to form a pn junction with at least one of said first and second regions.

17. A SiC semiconductor device according to claim 13 including a contact coupled to the intervening portion of the substrate so that the device acts as a transistor.

18. A SiC semiconductor device according to claim 17 in which the first and second regions are doped p-type and the intervening region is doped n-type and contact coupled to the intervening portion comprises a material which forms an ohmic contact therewith so that the device is operable as a bipolar transistor.

19. A SiC semiconductor device according to claim 17 in which the first and second regions are doped p-type and the contact coupled to the intervening portion includes a third metallic layer overlying an insulative layer to form an insulated gate over the intervening portion so that the device is operable as a field effect transistor.

20. A SiC semiconductor device according to claim 19 in which the third conductive layer includes an Os layer.

21. A SiC semiconductor device according to claim 19 in which the third conductive layer includes:

a titanium carbide (TiC) layer the insulative layer;

a tungsten carbide (WC) layer covering the titanium carbide (TiC) layer; and

a layer consisting essentially of elemental tungsten contacting the tungsten carbide (WC) layer.

22. A SiC semiconductor device according to claim 17 in which the first and second regions are doped p-type and the contact coupled to the intervening portion includes a conductive layer contacting a surface of the intervening portion so that the device is operable as a transistor.

23. A SiC semiconductor device according to claim 22 in which the contact coupled to the intervening portion includes:

a titanium carbide (TiC) layer contacting the a surface portion of the intervening layer;

a tungsten carbide (WC) layer covering the titanium carbide (TiC) layer; and

a layer consisting essentially of elemental tungsten contacting the tungsten carbide (WC) layer;

the intervening layer being doped p-type so that the device is operable as a transistor.

24. A SiC semiconductor device according to claim 22 in which the contact coupled to the intervening portion includes an Os layer contacting the a surface portion of the intervening layer.

25. A SiC semiconductor device according to claim 1 in which the second layer includes:

a titanium carbide (TiC) layer on the second surface;

a tungsten carbide (WC) layer on the titanium carbide (TiC) layer; and

a metallic tungsten (W) layer on the tungsten carbide (WC) layer.

26. A SiC semiconductor device comprising:

a semiconductor substrate comprising silicon carbide having a first surface and a second surface, the substrate including a first doped region adjacent the first surface and a second doped region adjacent the second surface;

a first conductive layer comprising a first contact metal layer on the first surface to form a first contact having an electronic interface to the first region; and

a second conductive layer contacting the second surface to form a second electronic contact to the substrate, the second layer including:

a titanium carbide (TiC) layer contacting the second surface;

a tungsten carbide (WC) layer covering the titanium carbide (TiC) layer; and

a layer consisting essentially of elemental tungsten contacting the tungsten carbide (WC) layer.

27. A SiC semiconductor device according to claim 26 in which the second region is doped n-type, and the second contact forms an ohmic junction.

28. A SiC semiconductor device according to claim 26 including a layer of a bonding metal contacting the tungsten layer, selected from a group of conductive metals that is adapted to bond to a tungsten surface.

29. A SiC semiconductor device according to claim 26 including a layer of a bonding metal contacting the tungsten layer, the bonding metal being selected from a group consisting of Pt, Pd, W, Au, PtAu, V, Ti, Zr, Hf,

Cr, Fe, Ni, Cu, Nb, Mo, Tc, Ru, Rh, Ag, Ta, Re, Ir.

30. A SiC semiconductor device according to claim 26 in which the second region is doped p-type, and the second contact forms a rectifying junction.

31. A SiC semiconductor device according to claim 26 in which the first layer includes:

a titanium carbide (TiC) layer on the first surface;

a tungsten carbide (WC) layer on the titanium carbide (TiC) layer; and

a metallic tungsten (W) layer on the tungsten carbide (WC) layer.

32. A SiC semiconductor device according to claim 31 in which the first and second regions and intervening portions of the substrate are doped n-type so that the first contacts and the second contact each form an ohmic junction and the device acts as a resistive device.

33. A SiC semiconductor device according to claim 31 in which the first and second regions are doped n-type and a contact is coupled to an intervening portion of the substrate, the contact including a third conductive layer overlying an insulative layer to form an insulated gate over the intervening portion so that the device is operable as a field effect transistor.

34. A SiC semiconductor device according to claim 33 in which the conductive layer overlying the insulative layer includes:

a titanium carbide (TiC) layer on the insulative surface;

a tungsten carbide (WC) layer on the titanium carbide

(TiC) layer; and

a metallic tungsten (W) layer on the tungsten carbide (WC) layer.

35. A SiC semiconductor device according to claim 33 in which the conductive layer overlying the insulative layer includes a layer of Os contacting the insulative layer.

36. A SiC semiconductor device according to claim 31 in which the first and second regions are doped n-type and a contact is coupled to an intervening portion of the substrate, the contact including a conductive layer contacting a surface of the intervening portion so that the device is operable as a transistor.

37. A SiC semiconductor device according to claim 36 in which the conductive layer includes:

a titanium carbide (TiC) layer on the surface of the intervening portion;

a tungsten carbide (WC) layer on the titanium carbide (TiC) layer; and

a metallic tungsten (W) layer on the tungsten carbide (WC) layer.

38. A SiC semiconductor device according to claim 36 in which the conductive layer includes a layer of Os contacting the surface of the intervening region.

39. A SiC semiconductor device according to claim 36 in which the intervening portion of the substrate is doped p-type so that the device is operable as a bipolar transistor.

40. A SiC semiconductor device according to claim 36 in which intervening portion of the substrate is doped n-type so that the device is operable as a MESFET.

41. A SiC semiconductor device according to claim 40 the contact contacting a surface portion of the intervening portion comprises an Os layer.

42. A SiC semiconductor device according to claim 31 including a contact coupled to an intervening portion of the substrate so that the device acts as a transistor.

43. A SiC semiconductor device according to claim 42 in which the gate contact material includes a third conductive layer overlying an insulative layer to form an insulated gate over the intervening portion so that the device acts as a field effect transistor.

44. A SiC semiconductor device according to claim 26 in which the first region is doped p-type and the first conductive layer is formed of a material suitable to form an ohmic contact with the first region, the second region is doped n-type to form an ohmic contact to the second layer, and the substrate includes a first n-type intervening portion adjoining the region and a second p-type intervening portion adjoining the second region of the substrate so as to define a four-layer device having three pn junctions electrically coupled between said first and second conductive layers.

45. A SiC semiconductor device according to claim 44 in which the first conductive layer comprises an Os layer contacting the first region.

46. A SiC semiconductor device according to claim 44 including a third conductive layer contacting a surface of one of the intervening portions.

47. A SiC semiconductor device according to claim 46 in which the third conductive layer comprises one of an Os layer and a TiC/WC/W layer.

48. A SiC semiconductor device according to claim 44 in the third conductive layer is capacitively coupled to a surface of one of the intervening portions.

49. A SiC semiconductor device according to claim 48 in which the third conductive layer comprises one of an Os layer and a TiC/WC/W layer.

50. A method of forming an electrical contact to a surface of SiC semiconductor substrate comprising:

depositing a layer comprising metallic osmium (Os) on an area of the substrate surface to form a contact having an electronic interface to the substrate; and

forming a protective cap over the osmium layer.

51. A method according to claim 50 including annealing the substrate after depositing the Os layer to bond the Os layer to the SiC substrate at said surface.

52. A method according to claim 51 including doping a portion of the substrate in said area with an n-type impurity so that the Os layer and the n-type doped substrate portion form a rectifying Schottky junction.

53. A method according to claim 52 including depositing a thin silicon layer on the substrate surface in said area prior to depositing the Os layer.

54. A method according to claim 51 including doping a portion of the substrate in said area with an p-type impurity so that the Os layer and the p-type doped substrate portion form an ohmic junction.

55. A method according to claim 51 in which the step of forming a protective cap over the osmium layer includes depositing a layer comprising platinum (Pt) over the osmium layer.

56. A method of forming an electrical contact to a surface of SiC semiconductor substrate comprising:

depositing a layer comprising metallic osmium (Os) on an area of the substrate surface to form a contact to the substrate; and

annealing the substrate after depositing the Os layer to bond the Os layer to the SiC substrate at said surface.

57. A method according to claim 56 including depositing a thin silicon layer on the substrate surface in said area prior to depositing the Os layer.

58. A method according to claim 56 including doping a portion of the substrate in said area with an n-type impurity so that the Os layer and the n-type doped substrate portion form a rectifying junction.

59. A method according to claim 56 including doping a portion of the substrate in said area with an p-type impurity so that the Os layer and the p-type doped substrate portion form an ohmic junction.

60. A method of forming an electrical contact to a surface of SiC semiconductor substrate comprising:

depositing a titanium carbide (TiC) layer on an area

of the substrate surface to form a contact having an electronic interface to the substrate;

depositing a tungsten carbide (WC) layer on the titanium carbide (TiC) layer; and

depositing a metallic tungsten (W) layer on the tungsten carbide (WC) layer.

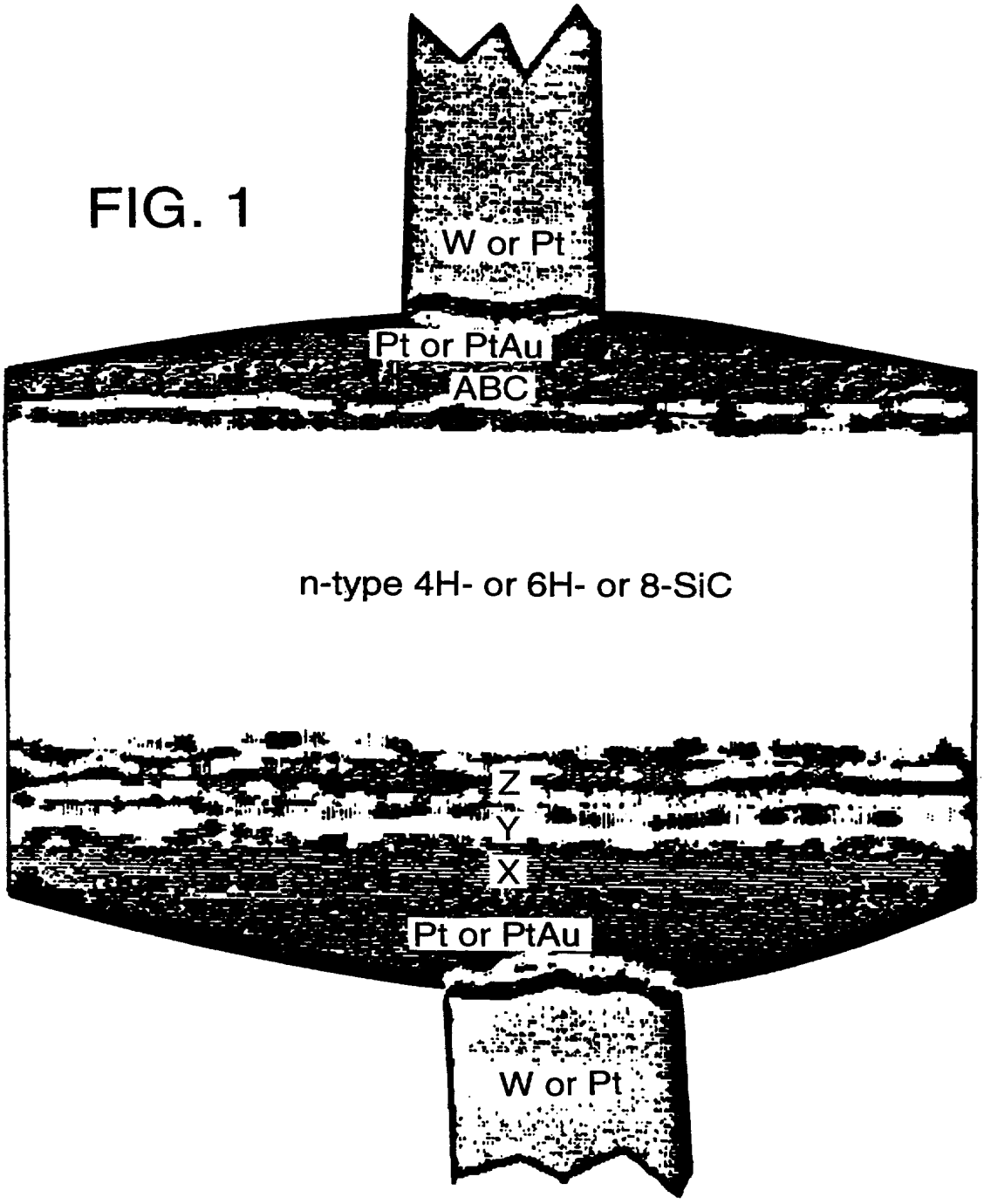
61. A method according to claim 60 including doping a portion of the substrate in said area with an n-type impurity so that the TiC/WC/W layer and the n-type doped substrate portion form an ohmic junction.

62. A method according to claim 60 including doping a portion of the substrate in said area with an p-type impurity so that the TiC/WC/W layer and the p-type doped substrate portion form a rectifying junction.

63. A method according to claim 60 including annealing the substrate during or after deposition of the W layer to bond the W layer to the WC layer.

64. A method according to claim 60 including annealing the substrate during or after deposition of TiC layer to densify the TiC layer before deposition of the WC layer.

FIG. 1



GF Exhibit 1124 - 2506/2704

FIG. 2

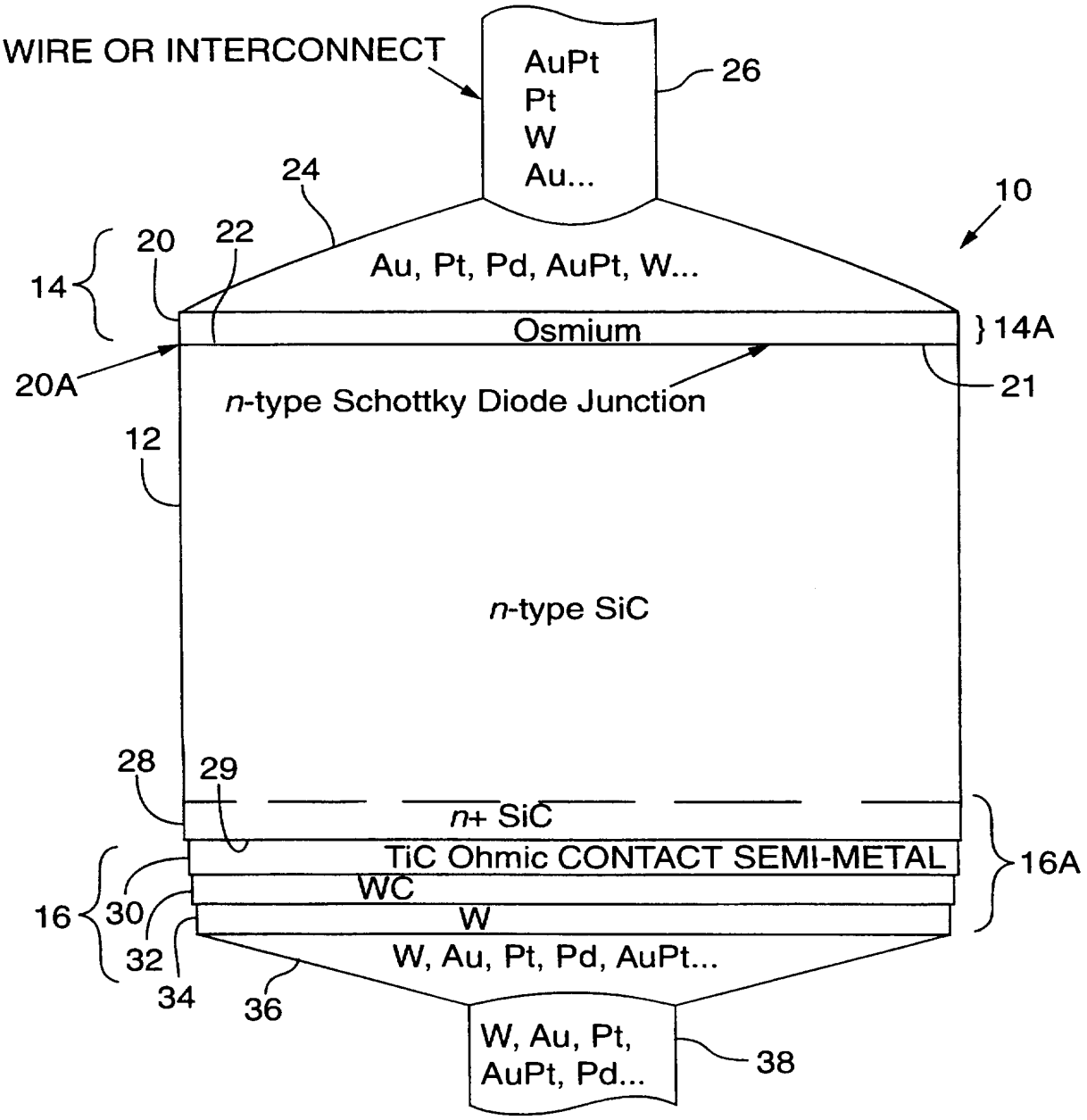

WIRE OR INTERCONNECT
AuPt
Pt
W
Au...
26
24
10
20
22
14
Au, Pt, Pd, AuPt, W...
Osmium
} 14A
20A
21
n-type Schottky Diode Junction
12
n-type SiC
28
29
n+ SiC
TiC Ohmic CONTACT SEMI-METAL
16A
WC
16
30
W
32
W, Au, Pt, Pd, AuPt...
34
36
W, Au, Pt,
AuPt, Pd...
38

FIG. 3

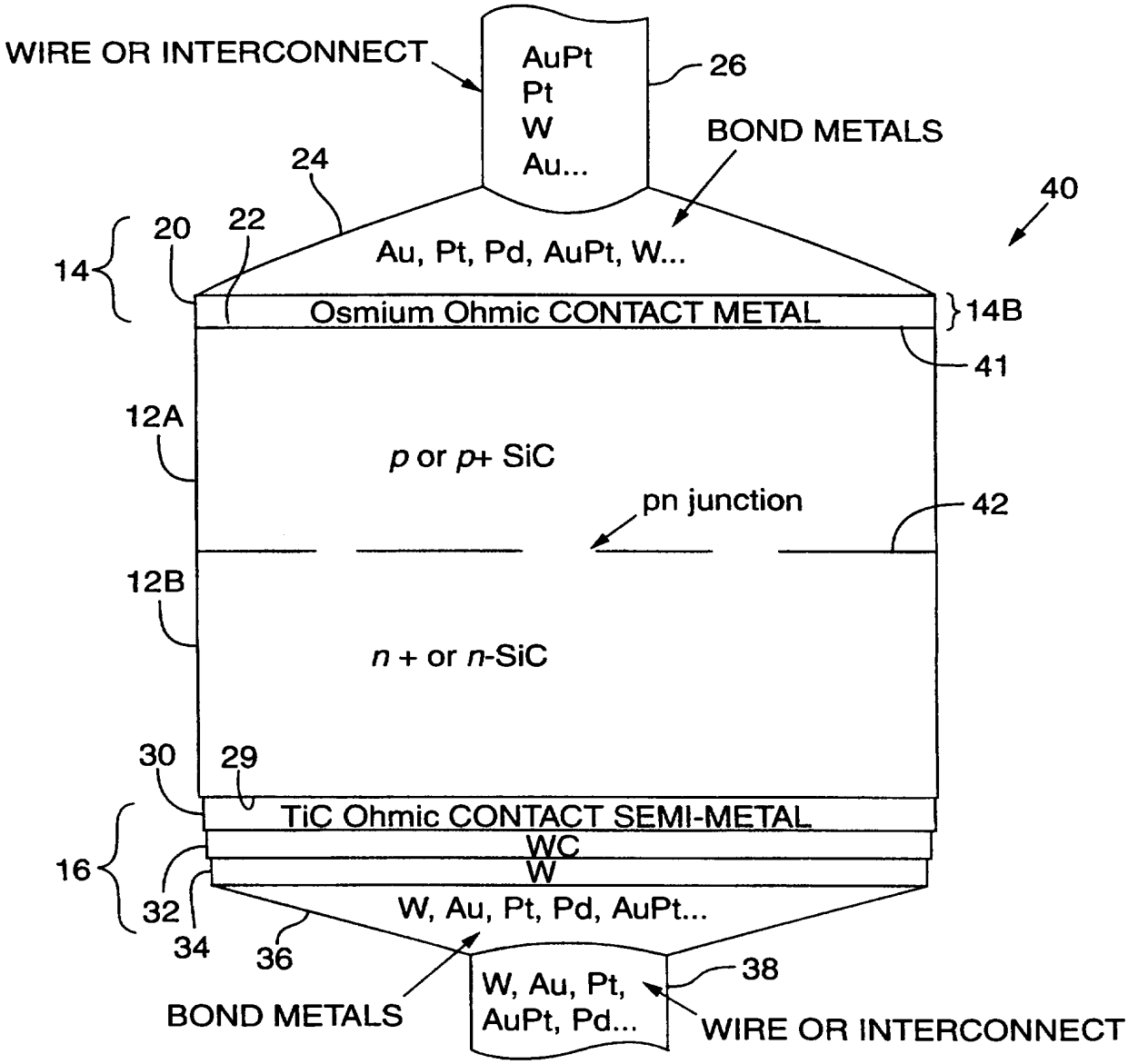

WIRE OR INTERCONNECT
AuPt
Pt
W
Au...
26
BOND METALS
24
40
20
22
14
Au, Pt, Pd, AuPt, W...
Osmium Ohmic CONTACT METAL
14B
41
12A
p or p+ SiC
pn junction
42
12B
n + or n-SiC
30
29
TiC Ohmic CONTACT SEMI-METAL
WC
W
16
32
34
36
W, Au, Pt, Pd, AuPt...
W, Au, Pt,
AuPt, Pd...
38
BOND METALS
WIRE OR INTERCONNECT

FIG. 4A

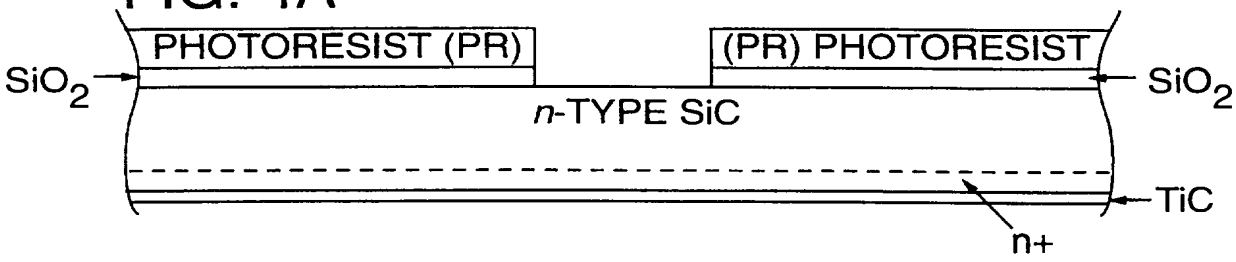


FIG. 4B

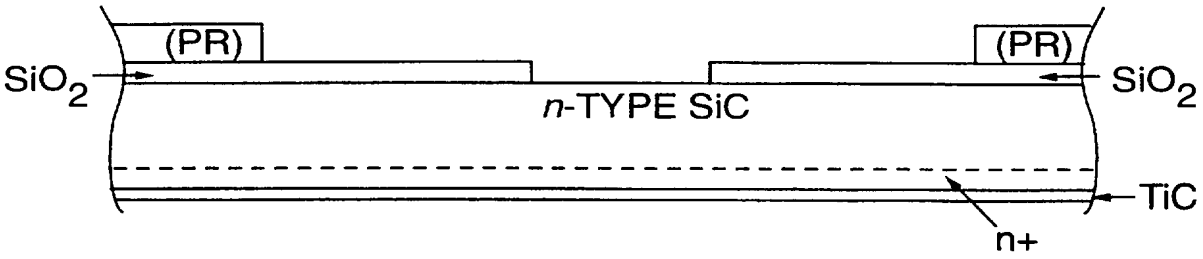


FIG. 4C

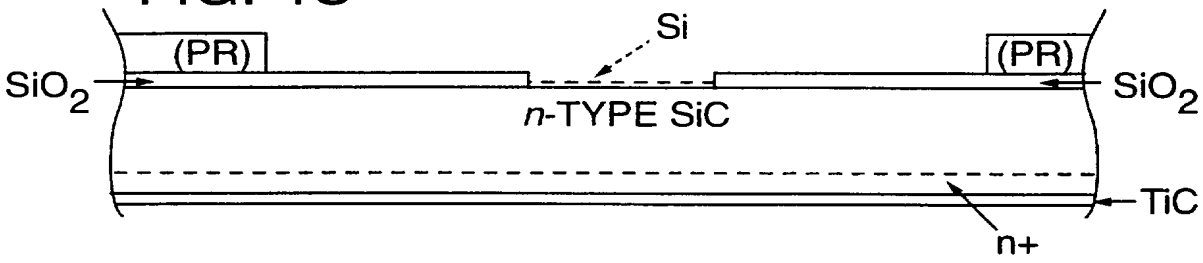


FIG. 4D

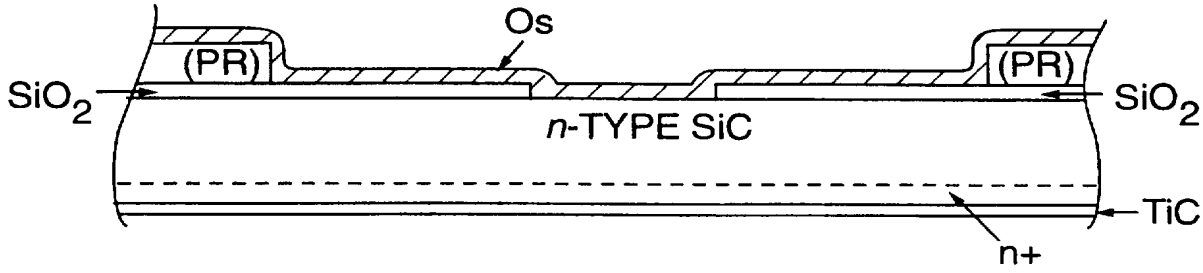


FIG. 4E

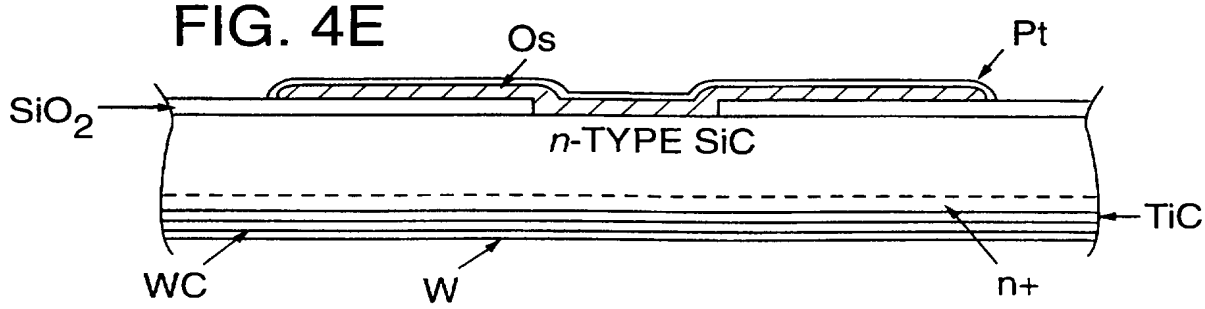


FIG. 5

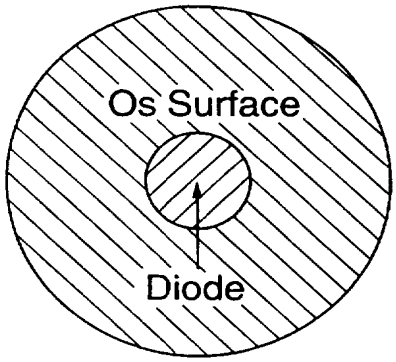


FIG. 6

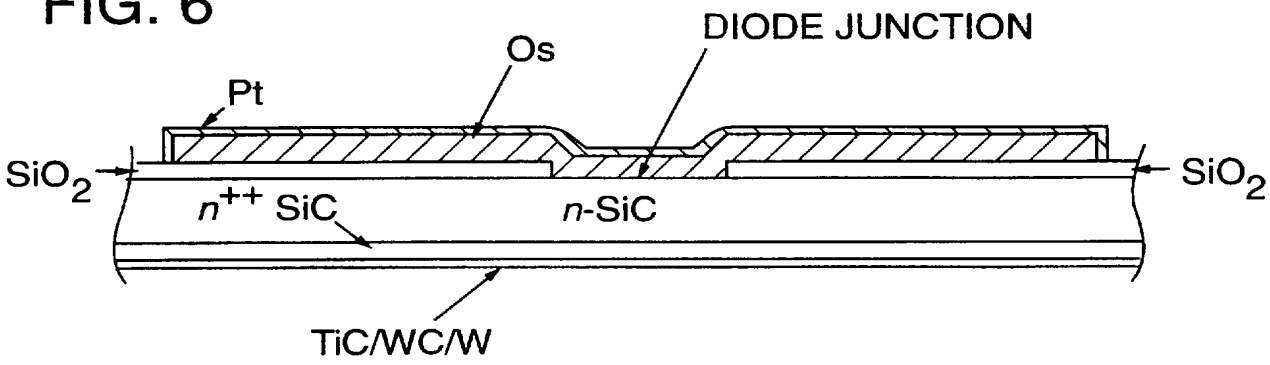
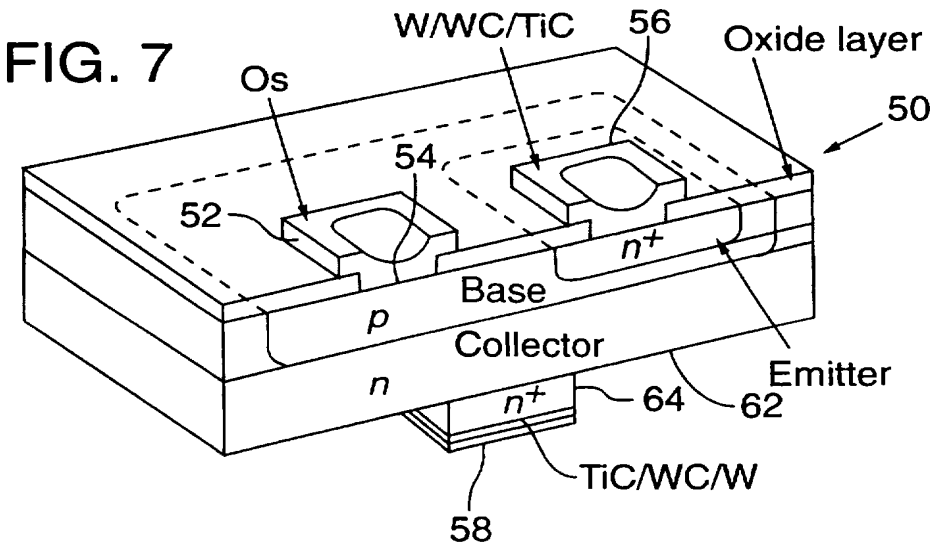


FIG. 7



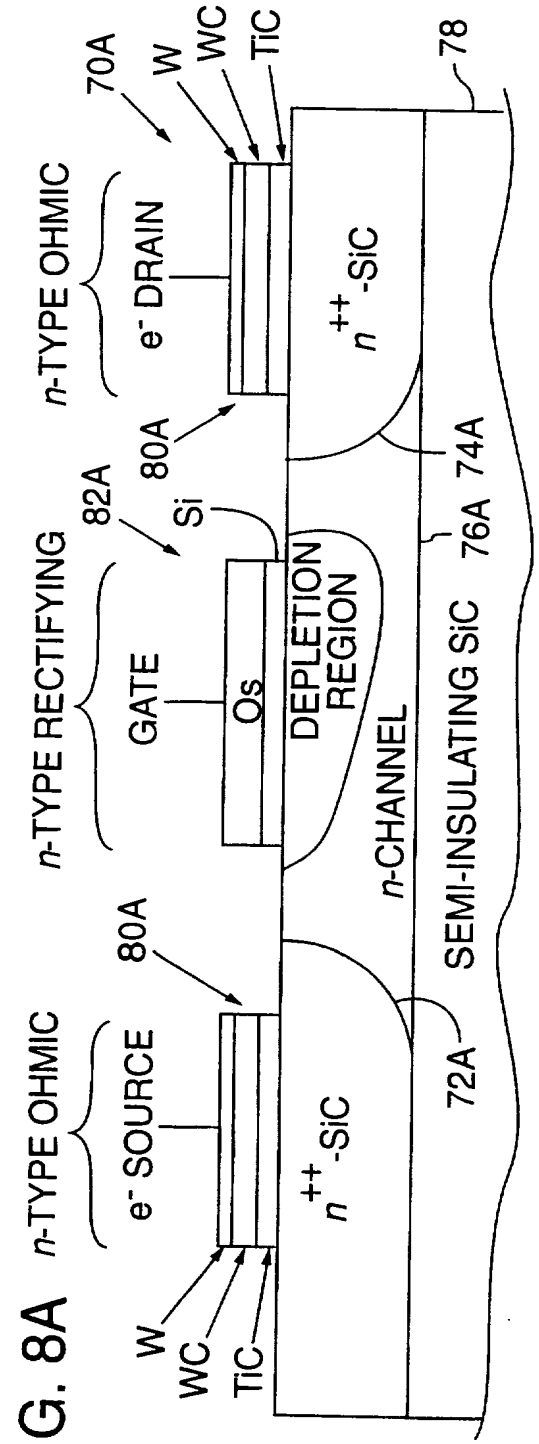

n-TYPE OHMIC
e- SOURCE
n-TYPE RECTIFYING
GATE
n-TYPE OHMIC
e- DRAIN
W
WC
TiC
80A
82A
Si
Os
80A
70A
W
WC
TiC
n++-SiC
DEPLETION REGION
n-CHANNEL
SEMI-INSULATING SiC
n++-SiC
72A
76A
74A
78

FIG. 8A

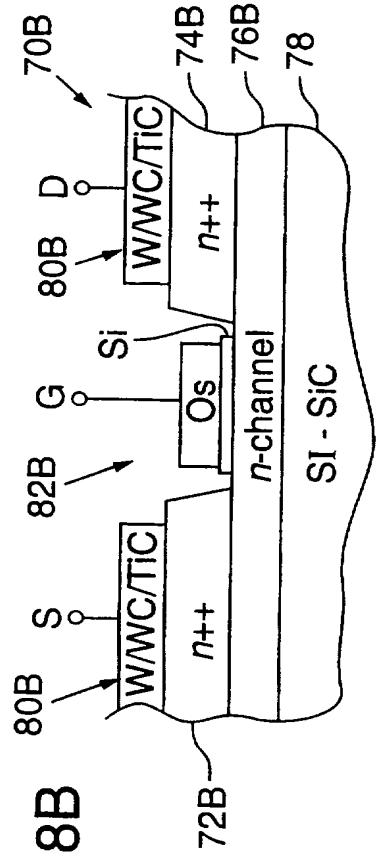

80B
S
82B
G
Si
80B
D
70B
W/WC/TiC
n++
Os
W/WC/TiC
n++
n-channel
SI - SiC
72B
74B
76B
78

FIG. 8B

FIG. 9A

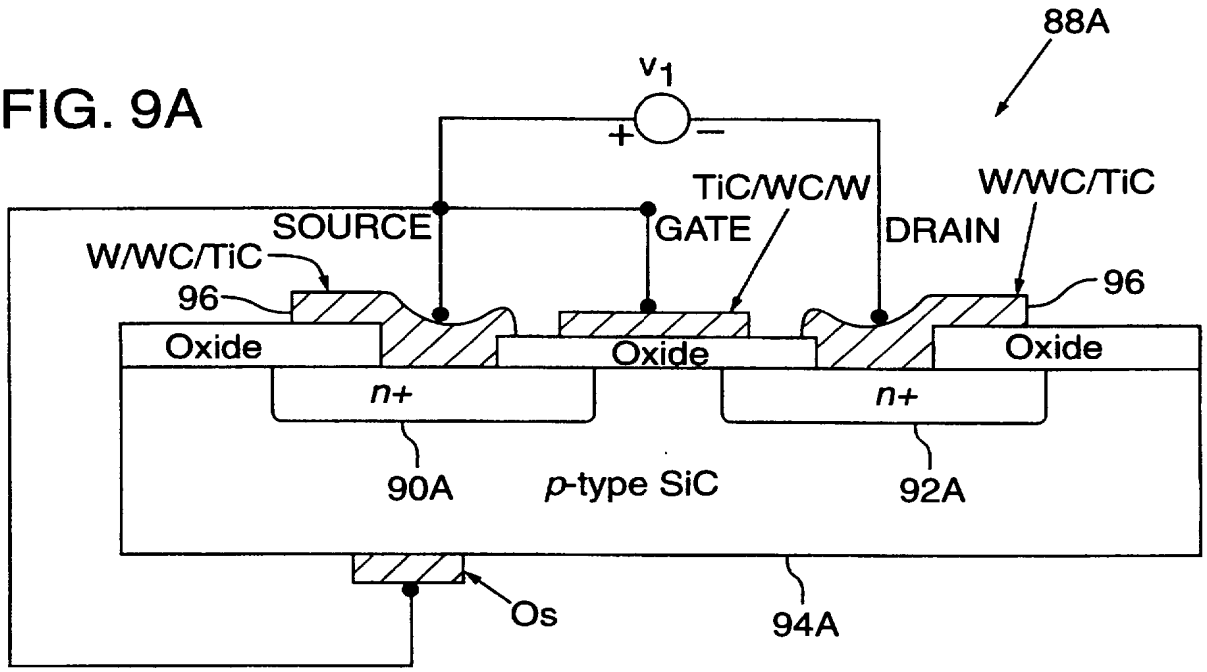

88A
v_1
+
−
TiC/WC/W
W/WC/TiC
SOURCE
GATE
DRAIN
W/WC/TiC
96
96
Oxide
Oxide
Oxide
n+
n+
90A
p-type SiC
92A
Os
94A

FIG. 9B

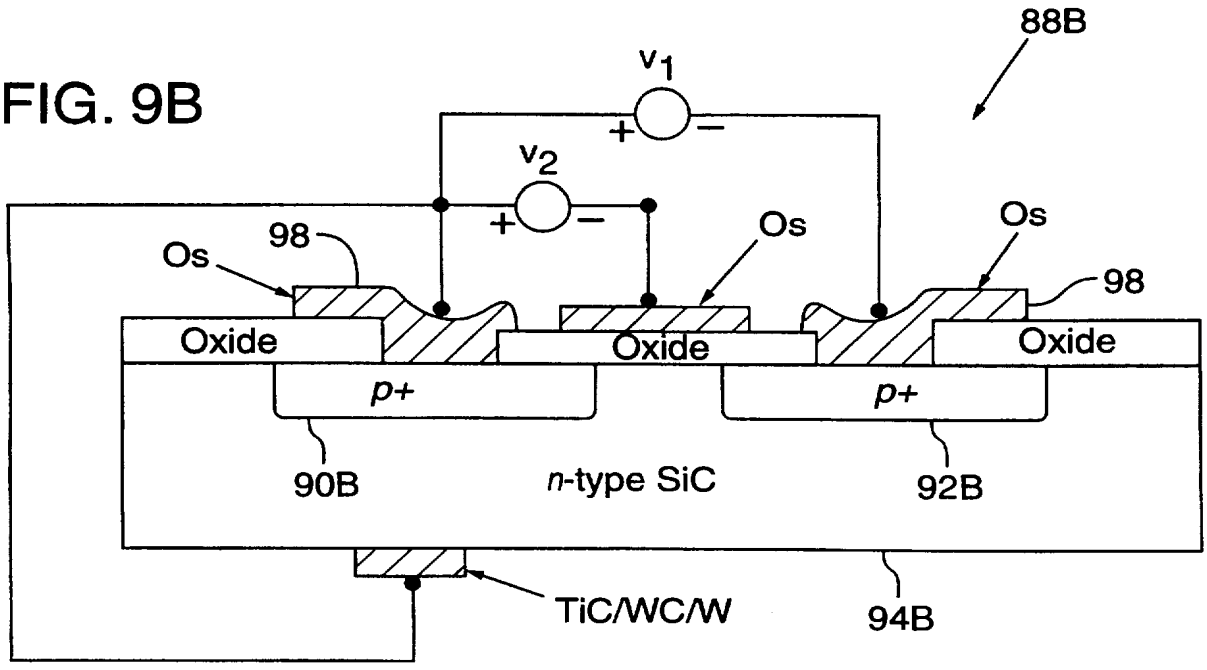

88B
v_1
+
−
v_2
+
−
Os
Os
98
Os
98
Oxide
Oxide
Oxide
p+
p+
90B
n-type SiC
92B
TiC/WC/W
94B

FIG. 10A

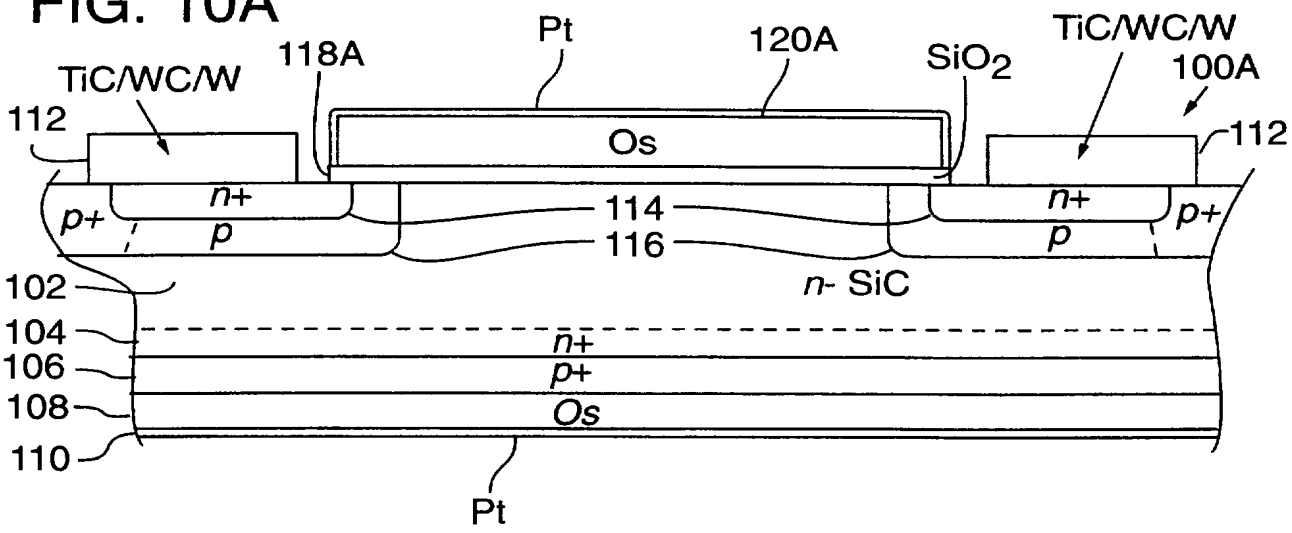
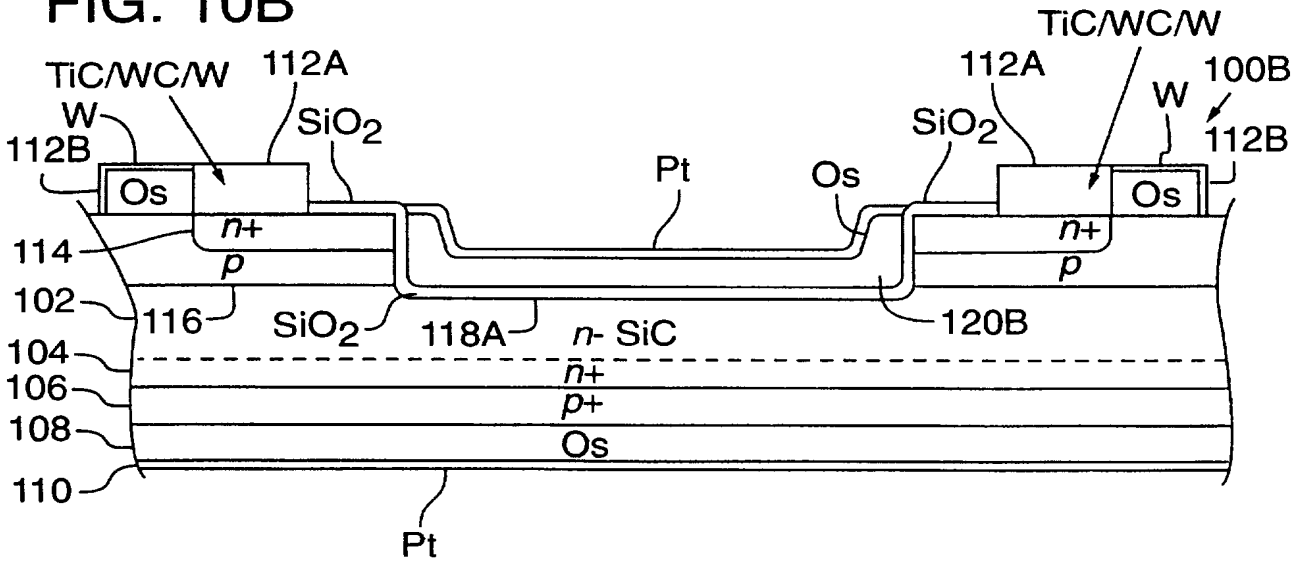


FIG. 10B



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/03497

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 21/283, 21/338, 29/161, 29/45, 29/47, 29/73, 29/812
US CL :257/77, 472, 473; 437/31, 39, 40, 176, 179, 192

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/77, 472, 473; 437/176, 179, 192

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS, STN (INSPEC, WPIDS)
search terms: silicon carbide, osmium, titanium carbide, tungsten carbide

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,270,252 A (PAPANICOLAOU) 14 December 1993 See column 2 line 40 to column 3 line 16.	1, 8, 12, 23-37, 50-60
A	US 5,278,431 A (DAS) 11 January 1994, col. 5, lines 40-65	8, 12, 21, 23, 25-37, 60-64
A	US 5,216,264 A (FUJII) 01 June 1993, col. 4 line 14 to col. 5 line 15.	15, 19, 33, 43
A	US 5,455,432 A (HARTSELL) 03 October 1995, col. 3 lines 37-65.	8, 12, 21, 26, 29, 31, 34, 37 47, 49, 60

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
08 MAY 1997	27 JUN 1997
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer TUAN QUACH Telephone No. (703) 308-0661

Form PCT/ISA/210 (second sheet)(July 1992)*

GF Exhibit 1124 - 2514/2704

Electronic Acknowledgement Receipt

EFS ID:	39744241
Application Number:	16506022
International Application Number:	
Confirmation Number:	3561
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC12
Receipt Date:	17-JUN-2020
Filing Date:	09-JUL-2019
Time Stamp:	13:30:35
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Foreign Reference	KR19910006249B1_wTransl.pdf	2481317 01541ff17116ae95f05bfb357fbd95a1d9d24dea	no	50

Warnings:

Information:					
2	Foreign Reference	KR19920010131B1_wTransl.pdf	1266892 5c9e1bd5435806a52195956e2bfa4159905761a5	no	37
Warnings:					
Information:					
3	Foreign Reference	KR19940020550A_wTransl.pdf	564431 0006fa629820be608ba2ed2368a9ab951cfbe402	no	6
Warnings:					
Information:					
4	Foreign Reference	KR19950010873B1_wTransl.pdf	480246 05fdf6f841ef2bceb4b56ba8a503064e1dac0aa3	no	15
Warnings:					
Information:					
5	Foreign Reference	KR19970030333A_wTransl.pdf	495197 e73846f41a34f4efa645f412c9721a6041284855	no	6
Warnings:					
Information:					
6	Foreign Reference	KR19980024649A_wTransl.pdf	5957415 cc815231b063b2ae0afc2acbdda5bd2bdd31a210	no	89
Warnings:					
Information:					
7	Foreign Reference	KR19990025041A_wTransl.pdf	734783 a3242e891c624e678a3bdee9f5e6d4fca393120d	no	12
Warnings:					
Information:					
8	Foreign Reference	KR19990045323A_wTransl.pdf	7414244 0af9f3102b565bedac724976dd411468fb74e64f	no	87
Warnings:					
Information:					

9	Foreign Reference	KR20000025576A_wTransl.pdf	1882134 a03d3d5da9bff4081240653d5aece8fff6b43519	no	36
Warnings:					
Information:					
10	Foreign Reference	KR20000027908A_wTransl.pdf	1105571 eeb820fd54018acedb55b81136b03ffa2f6603bb	no	30
Warnings:					
Information:					
11	Foreign Reference	SE0875077T3.pdf	2778881 ebb5258d01bcd8bb4ecf99eba122911b090eebcf	no	31
Warnings:					
Information:					
12	Foreign Reference	WO0128677A1_Original_document_20200529235136.pdf	4644482 7569f42af48e1eec46514e02ec84b2f74744bef8	no	66
Warnings:					
Information:					
13	Foreign Reference	WO0163677A1_Original_document_20200529235214.pdf	1227805 1f56e7ab0794e2fcff667c2961690be9f456c7b7	no	25
Warnings:					
Information:					
14	Foreign Reference	WO8800392A1_Original_document_20200529234536.pdf	2426856 ebd1cbd9f9f8a672e029355fe2b60bec17403341	no	25
Warnings:					
Information:					
15	Foreign Reference	WO9311558A1_Original_document_20200529234623.pdf	1462619 ad3834f0d848113148b81d9bd41d948da55e26f4	no	23
Warnings:					
Information:					

16	Foreign Reference	WO9534095A1_Original_document_20200529234715.pdf	2455141 0861779e7076f75f6131305bdd06ec7e48d855c5	no	30
Warnings:					
Information:					
17	Foreign Reference	WO9726678A2_Original_document_20200529234825.pdf	1004020 6856f68c8a5cdbf3e52b336e2c0e5178812b7ac7	no	15
Warnings:					
Information:					
18	Foreign Reference	WO9733308A1_Original_document_20200529235046.pdf	3613387 b77111f90e7b2c973c416dd6dc90b57d868ee441	no	53
Warnings:					
Information:					
19	Non Patent Literature	ABOELFOTOH_Materials_Res.pdf	688828 4516ac5a3f4268bda112167e418f3de284a443c0	no	13
Warnings:					
Information:					
20	Non Patent Literature	ABOELFOTOH_Physical_Rev33.pdf	941106 72b6b085dee50bc5bea70c4210de2baeea767a5d	no	7
Warnings:					
Information:					
21	Non Patent Literature	ABOELFOTOH_Physical_Rev34.pdf	980304 c3165cc4a2c2e2db4d99ab4dca2bf3600b01dbff	no	8
Warnings:					
Information:					
22	Non Patent Literature	ABOELFOTOH_Solid-State.pdf	657183 f07d929a89fbd8df1c2a8a4db941d65592691b7d	no	5
Warnings:					
Information:					

23	Non Patent Literature	ASAMIZU.pdf	1241711 a74882d2f8eb11d85546552a804b4f1564ab667d	no	8
Warnings:					
Information:					
24	Non Patent Literature	BARD.pdf	1578081 ee47e579927dc8a1b86af26a4e7e5750bd4577ca	no	8
Warnings:					
Information:					
25	Non Patent Literature	BEATTY.pdf	2470509 5077dd2056588083d527711d3f690c5a259a1981	no	26
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
26	Non Patent Literature	BOSWELL.pdf	209294 cc5236cc64c15527a04d383ded92625a03e2b8ac	no	2
Warnings:					
Information:					
27	Non Patent Literature	CALVET.pdf	12983774 7f032b2c95914c9b94bba7767dd4c82c55e04f20	no	183
Warnings:					
Information:					
28	Non Patent Literature	CAMPBELL.pdf	8988020 b4838d6c86b81dd4be6b5308fbe2a487c6517b2d	no	11
Warnings:					
Information:					
29	Non Patent Literature	CARD.pdf	1396292 be75830582d515ad4a5dc68b0999cdf56c4d1260	no	14
Warnings:					
Information:					

30	Non Patent Literature	CHANG.pdf	617160 9a992d7aa836362d6070f3e8f277f829cd9e070e	no	10
Warnings:					
Information:					
31	Non Patent Literature	CHEEK.pdf	354962 c7b8f6e9665d12e813b0d9448af37cbbf1b9718f	no	5
Warnings:					
Information:					
32	Non Patent Literature	CHEN_IEEE_1983.pdf	1315410 203db3cb2025d568f2dbda5eac366d853a71447e	no	9
Warnings:					
Information:					
33	Non Patent Literature	CHEN_NASA.pdf	8006180 065661af20c0ec67ea3af079d5a7f5b9c1f8d5e9	no	100
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
34	Non Patent Literature	CHEN_Physical_Rev.pdf	625699 830cad765b262177af29c0c7859a9855917dd267	no	6
Warnings:					
Information:					
35	Non Patent Literature	CHOURASIA.pdf	467706 5847581110a882dbc6bd4b90b971c94fe058a4b2	no	4
Warnings:					
Information:					
36	Non Patent Literature	CLAFLIN_JVACS_16-3.pdf	1206018 6753ec95e3ab1fcac5fc5bf5b715f1592e458794	no	6
Warnings:					
Information:					

37	Non Patent Literature	CLAFLIN_JVACS_16-4.pdf	552566 7edc550b01eebd35ebb04f129bc061d39db05b45	no	5
Warnings:					
Information:					
38	Non Patent Literature	CLARKE.pdf	1701625 a4f3d94c6ceb6b30890d196d2f394994519956fa	no	17
Warnings:					
Information:					
39	Non Patent Literature	COHEN.pdf	8640849 f63cf994d8004bd6be1616fa3bdafdbe4177b0c5	no	98
Warnings:					
Information:					
40	Non Patent Literature	CONNELLY.pdf	245713 8f44c75608d164d534efb951f815d51d38a2b067	no	2
Warnings:					
Information:					
41	Non Patent Literature	COSTA.pdf	2390675 782497296b83dbe542d916a470a8be749c8f3f15	no	13
Warnings:					
Information:					
42	Non Patent Literature	COWLEY.pdf	1208276 efec4d63cdbf55f313329f14e31593647ed1be53	no	12
Warnings:					
Information:					
43	Non Patent Literature	DAVIS.pdf	3572103 780300e240bdd2fbbaef9a93fa2611d763e7cd4a	no	32
Warnings:					
Information:					

44	Non Patent Literature	DEBOIS.pdf	997193 f42433b00cfbfa5b1b47a08e0f3c5300a7b22937	no	8
Warnings:					
Information:					
45	Non Patent Literature	DEPAS.pdf	877884 aade6e054681c145c4ea3ae5adbc416d2a0b1d17	no	9
Warnings:					
Information:					
46	Non Patent Literature	Dheurle_1996.pdf	2727568 c748d870692eeefc58a4171dd638abc67d685e2f	no	19
Warnings:					
Information:					
47	Non Patent Literature	Dheurle_1998.pdf	2332942 a71cc19eb1cd5f5f0bc428d828b5cd8b004962bb	no	16
Warnings:					
Information:					
48	Non Patent Literature	EMC.pdf	18676054 a6e6790885fdfd61a0f4e65a7eac2f2e534491eb	no	107
Warnings:					
Information:					
49	Non Patent Literature	EUN.pdf	8792985 df6d409e746e4babae8443f1522ba99e926ea8bf	no	113
Warnings:					
Information:					
50	Non Patent Literature	FAN.pdf	767348 934a97ebbfc81141058e5a65cad82852117ff85d	no	4
Warnings:					
Information:					

51	Non Patent Literature	FRANCIOSI.pdf	15438580 5e5b1e7ef3e9141830fe7c1965de828e23f1a665	no	140
Warnings:					
Information:					
52	Non Patent Literature	FRANGOUL.pdf	1736822 1c0c544f6b9f6a2353871fc872a3afe9184f6098	no	5
Warnings:					
Information:					
53	Non Patent Literature	FULTON.pdf	757428 65955f946046eb6dce28d680542a68412425536d	no	6
Warnings:					
Information:					
54	Non Patent Literature	GESSMANN.pdf	633678 fbc935e128cd91d87363c405d6a312f787d777d1	no	5
Warnings:					
Information:					
55	Non Patent Literature	GETTO.pdf	675339 9709aba12194dd2df40582f76cadbb73d7975b42	no	5
Warnings:					
Information:					
56	Non Patent Literature	GIBONEY.pdf	10834639 74172f47ecc3c5d6ba4450c451a40c7bc15ffabc	no	170
Warnings:					
Information:					
57	Non Patent Literature	GLASS.pdf	478905 f032a57967013d145fe79ddaab290c56f816174f	no	3
Warnings:					
Information:					

58	Non Patent Literature	GORDON.pdf	7541760 eb9e7db91526a2e16da0ed00c5dabf8fc9a1a684	no	14
Warnings:					
Information:					
59	Non Patent Literature	GREEN_349-365.pdf	1717644 c419f1c69faf75114b44fff0f8496bb82d788aab	no	17
Warnings:					
Information:					
60	Non Patent Literature	GREEN_551-561.pdf	1117326 a9639a8c1d62577ede8c598e7581ea7c30079230	no	11
Warnings:					
Information:					
			Total Files Size (in bytes):	181139560	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt

EFS ID:	39745110
Application Number:	16506022
International Application Number:	
Confirmation Number:	3561
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC12
Receipt Date:	17-JUN-2020
Filing Date:	09-JUL-2019
Time Stamp:	13:32:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	OMEARA.pdf	605324 056463dfeca76b11840986e3fb0b5b7471cea70c	no	7

Warnings:

Information:					
2	Non Patent Literature	OSKAM.pdf	2710354 4e7d63fdf889c8adb4cc366dbaf4705ebf942e14	no	23
Warnings:					
Information:					
3	Non Patent Literature	PARK_15.pdf	1587781 da57ae2b7261489b74ad347c762858619d43537f	no	8
Warnings:					
Information:					
4	Non Patent Literature	PARK_69.pdf	1242318 58d49d9f4e40cdf3b5c24139cea4316e2643ea14	no	6
Warnings:					
Information:					
5	Non Patent Literature	PARK_80.pdf	1208748 58d745d6fe1f1efe615f2cc4c1824d33d7bb1827	no	4
Warnings:					
Information:					
6	Non Patent Literature	PARK_81.pdf	1720768 143e8dfb5e3aecf0fcb70832b7b29c66d2cfe489	no	9
Warnings:					
Information:					
7	Non Patent Literature	PARK_Cambridge.pdf	4698354 7da43223ef969ba3c3cab6d536641acfb6056efc	no	6
Warnings:					
Information:					
8	Non Patent Literature	PATKAR.pdf	4394420 1ccffbc2831f6438d7289c8febddef668a23b117	no	5
Warnings:					
Information:					

9	Non Patent Literature	PLUMMER.pdf	3059524 ccfde516d0fff02508ac699be014e889d57fe69c	no	19
Warnings:					
Information:					
10	Non Patent Literature	POLISHCHUK.pdf	346212 b96dc607a664fbb8c5241b791f64beee1aa3022d	no	3
Warnings:					
Information:					
11	Non Patent Literature	PORTER.pdf	3851045 311b7fb66a75367669c5544a724e51dfd3cf34b9	no	67
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
12	Non Patent Literature	PROCTOR.pdf	1155563 b33796ec488f98e1824ab6e5ec99fccf80923b1e	no	8
Warnings:					
Information:					
13	Non Patent Literature	REN.pdf	11941371 c1fcea56bcb30bba59447d550c94a114c4af7e16	no	211
Warnings:					
Information:					
14	Non Patent Literature	RHODERICK_1970.pdf	1506395 b71821f8e9c446b3faff849096b473e1cbd45145	no	16
Warnings:					
Information:					
15	Non Patent Literature	RHODERICK.pdf	2176017 054ee6cc4fb31220bff5b54e4cf5267d7eaf63e9	no	14
Warnings:					
Information:					

16	Non Patent Literature	RICHARDS.pdf	23413871 b895a5552b48bbebcb96b107c94dabdac69e17e0	no	259
Warnings:					
Information:					
17	Non Patent Literature	ROHDIN.pdf	2100928 0f69d9ce94cf704e8c7d6779d51fa3387364393e	no	26
Warnings:					
Information:					
18	Non Patent Literature	SAMBELL.pdf	760314 eb6a702f692cd472330ec4e978380254c4375fad	no	8
Warnings:					
Information:					
19	Non Patent Literature	SCHENK_LAB.pdf	21349960 6f2e42c3809d2b6dc1943ca724f152763277ee8e	no	177
Warnings:					
Information:					
20	Non Patent Literature	SCHENK_SEMI.pdf	1119402 1b62363e4d30d17e22c4d77079b90ff2b2ac3d07	no	5
Warnings:					
Information:					
21	Non Patent Literature	Semi_Indus.pdf	15879853 54e6f7e782625e5fa4af8b939186ef8061adbb17	no	29
Warnings:					
Information:					
22	Non Patent Literature	SHARMA.pdf	2524927 8c09ce7529056bded5e8e717ebfc3f1df963d27e	no	10
Warnings:					
Information:					

23	Non Patent Literature	Shewchun_1977.pdf	1268063 46ae41e9d13f779c40756de8cee374970709b8a7	no	7
Warnings:					
Information:					
24	Non Patent Literature	SHEWCHUN_1979.pdf	1094397 ccb356df18db5a5a091cb2ea3a2d631ce0acc44d	no	25
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
25	Non Patent Literature	SHEWCHUN_1980.pdf	1527713 3646411cd39a8fd7cdb4f51f954b884e0a1266cf	no	12
Warnings:					
Information:					
26	Non Patent Literature	SHIH.pdf	2479502 7f695684ae2ea5330ba30b3cde1fe2ebf1a59479	no	10
Warnings:					
Information:					
27	Non Patent Literature	SINGH.pdf	20949851 c85203b3bb2c642ea8eb141e6dbd09c7c557d5ea	no	365
Warnings:					
Information:					
28	Non Patent Literature	SMITH.pdf	1072592 d096999892f0d4354180ff4a10186258c77a2b83	no	10
Warnings:					
Information:					
29	Non Patent Literature	SOBOLEWSKI_1987.pdf	401283 6812a856b485121fb34b4910826411c5a60fc006	no	6
Warnings:					
Information:					

30	Non Patent Literature	SOBOLEWSKI_1989.pdf	1791944 0f3735b25247ae413239574bb6102b6b16e268c7	no	9
Warnings:					
Information:					
31	Non Patent Literature	SONG.pdf	1137353 e8c6de41c7cc272b0aff9a6234ab07c82e0033d2	no	4
Warnings:					
Information:					
32	Non Patent Literature	SPICER_1980.pdf	537211 70bc30d0e53d6afb054202f6df831b3abfc9e435	no	4
Warnings:					
Information:					
33	Non Patent Literature	SPICER_1981.pdf	21030091 aa8456bd0e3472b68cf73650cbce4810da95edd1	no	158
Warnings:					
Information:					
34	Non Patent Literature	SRIVASTAVA.pdf	746119 f148e556859562fce25f5284469f38dbb7e4ffb7	no	7
Warnings:					
Information:					
35	Non Patent Literature	STREETMAN.pdf	9394198 80427d0c10483af9c57b86e14ce7308d52128f25	no	91
Warnings:					
Information:					
36	Non Patent Literature	SUGURO.pdf	1378575 2f9f1b57dce70b6e491549fb282838b787dd488a	no	14
Warnings:					
Information:					

37	Non Patent Literature	TABORYSKI.pdf	1154243 baa76902c34f563c18a7b3945ae12cd09e6dbc0d	no	6
Warnings:					
Information:					
38	Non Patent Literature	TARAJI.pdf	807422 8e93b9529e63820b777e81747e0c60f3f6ea718c	no	4
Warnings:					
Information:					
39	Non Patent Literature	TAUBEBLATT_1982.pdf	1430916 ec24f3eb0c4d025a371064c329cddd3472bdaaf7	no	9
Warnings:					
Information:					
40	Non Patent Literature	TAUBEBLATT_1984.pdf	1035721 a4ecd15a2f39b1f091e21cf3fd48aaaff32e9575	no	4
Warnings:					
Information:					
41	Non Patent Literature	THANAILAKIS_1975.pdf	1376466 4cbdcef04dc32cea39b1a20e6e6cdf8ac13e2254	no	15
Warnings:					
Information:					
42	Non Patent Literature	THANAILAKIS_1976.pdf	810825 b23bee6f74d672347bb9d535e058cb11b3b17670	no	8
Warnings:					
Information:					
43	Non Patent Literature	TIWARI.pdf	410690 7eace95ef6da79ea8e6397ba64781eec368bd4e7	no	3
Warnings:					
Information:					

44	Non Patent Literature	TOPHAM.pdf	2201376 b8e35ddcf0d7e465affd504de4b666078450db12	no	176
Warnings:					
Information:					
45	Non Patent Literature	TSUTSUMI.pdf	1099972 66de6abe4ee085d4625562823bccaef191e42f1b	no	8
Warnings:					
Information:					
46	Non Patent Literature	TUCKER.pdf	7811925 8989737b13cdbc582120fbb5b468b28492d30538	no	82
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
47	Non Patent Literature	TUNG.pdf	487106 e7d580cceb5068dce85e7b03a412168025e45338	no	4
Warnings:					
Information:					
48	Non Patent Literature	TURNER.pdf	995417 274f56eadf01053bff486da5bfc5e4c59879908c	no	10
Warnings:					
Information:					
49	Non Patent Literature	VanOTTERLOO.pdf	376672 38c136adaa945148927e72d9e4c4eb5301aa2e04	no	5
Warnings:					
Information:					
50	Non Patent Literature	Vilinaus_Univ.pdf	11922531 d0e64742a436e02f1232c1884724ae9410cc04af	no	18
Warnings:					
Information:					

51	Non Patent Literature	WALDROP_1992.pdf	1108043 aa11a839ae50faba4933b31d7998097fc2b7a6b6	no	5
Warnings:					
Information:					
52	Non Patent Literature	WALDROP_1998.pdf	696039 06c485fdc5052e18284255a37fd396895a07a14d	no	4
Warnings:					
Information:					
53	Non Patent Literature	WALDROP.pdf	517169 402022eb38c989d76e8e5d4d0579479bd951b965	no	3
Warnings:					
Information:					
54	Non Patent Literature	WALUKIEWICZ.pdf	1815436 5c1f2977c7e8ba3ae8644de10d026448aefd2e6b	no	23
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
55	Non Patent Literature	WERNER.pdf	2334486 d7cc97636c208901ceeea922260377bad62bd1bd	no	13
Warnings:					
Information:					
56	Non Patent Literature	WILLIAMS_1988.pdf	1008725 4f5a5b7053ef2c13987ad5a6227c6d84aa6098c9	no	19
Warnings:					
Information:					
57	Non Patent Literature	WILLIAMS_1989.pdf	996080 459985ca879c21cf1caff3254dcff8a993f0d5de	no	5
Warnings:					
Information:					

58	Non Patent Literature	wilson.pdf	6812869 8f973ddabb7ab485dfd12369ceeba1bb2993ebcf	no	68
Warnings:					
Information:					
59	Non Patent Literature	WITTMER.pdf	542579 5ef0469b400460864b5bda6b5d018f10d259ac2f	no	4
Warnings:					
Information:					
60	Non Patent Literature	WU_1980.pdf	1051178 4ca2c0a912431e051c29ece21ec119335bd4a327	no	5
Warnings:					
Information:					
			Total Files Size (in bytes):	222966227	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt

EFS ID:	39745216
Application Number:	16506022
International Application Number:	
Confirmation Number:	3561
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC12
Receipt Date:	17-JUN-2020
Filing Date:	09-JUL-2019
Time Stamp:	13:32:32
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	WU_1989.pdf	2125336 c66ff748ff01dcf6c5e4dadf403e38ca565bf806	no	9

Warnings:

Information:					
2	Non Patent Literature	YANG.pdf	316250 f5093d538eabda9626750ed3c3e8a0a837937b5f	no	3
Warnings:					
Information:					
3	Non Patent Literature	YEN.pdf	554730 0c20f4ee7542d380cdf032c0f427a15f2d560410	no	6
Warnings:					
Information:					
4	Non Patent Literature	ZAFAR.pdf	1144578 940d4aef21c06467c3166a1d35b65d2d6fabdd22	no	4
Warnings:					
Information:					
5	Non Patent Literature	ZAIMA_Applied_Sci.pdf	692912 0a3e0e3e2925406e265eddc6a22efd7d1a8f522a	no	5
Warnings:					
Information:					
6	Non Patent Literature	ZAIMA_JPN.pdf	1159522 cc09cf855f5118632a7960b742b00cde26965891	no	8
Warnings:					
Information:					
7	Non Patent Literature	ZAIMA.pdf	14584878 ca68c3b962df82e4c4b0e97ee3750ccdb66b2287	no	18
Warnings:					
Information:					
8	Non Patent Literature	1-250_Pages_from_WESTE_Part_1of3.pdf	19430566 9aff8fd510c065f437739a2777f301df963baf72	no	250
Warnings:					
Information:					

9	Non Patent Literature	251-500_Pages_from_WESTE_Part_2of3.pdf	22400296 eb5e2cf6312b19caf3fd6df508f2974b0e6f8fcc	no	250
Warnings:					
Information:					
10	Non Patent Literature	551-749_Pages_from_WESTE_Part_3of3.pdf	19503932 0954e01d7fb15b20da44762a27dc12bc9b1aad83	no	249
Warnings:					
Information:					
		Total Files Size (in bytes):	81913000		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16506022
Filing Date	2019-07-09
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.
Attorney Docket Number	3771-0003-DC12

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4304042	A	1981-12-08	Yeh	
	2	4691219	A	1987-09-01	Goth	
	3	5614745	A	1997-03-25	Motonami	
	4	6323508	B1	2001-11-27	Takahashi, et al.	
	5	6521502	B1	2003-02-18	Yu	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20060178015	A1	2006-08-10	Verhaverbeke	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16506022
	Filing Date	2019-07-09
	First Named Inventor	Daniel E. Grupp
	Art Unit	2815
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC12

	2	20140117465	A1	2014-05-01	Huang, et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	ARCHIBONG, et al., On the Structure of A12O3 and Photoelectron Spectra of A12O2 and A12O3; J. Phys. Chem.A 1999, 103, pp. 1109-1114.	
	2	BORTZ, et al., Temperature Dependence of the Electronic Structure of Oxides: MgO, MgAl2O4 and Al2O3; Physica Scripta., Col. 41, pp. 537-541, 1990.	
	3	CARVER, et al., Specific Contact Resistivity of Metal-Semiconductor Contacts - A New, Accurate Method Linked to Spreading Resistance; IEEE Transactions on Electron Devices, Vol. 35, No. 4, April 1988, pp. 489-497	
	4	LIDE, David R., CRC Handbook of Chemistry and Physics, Internet Version 2005; <http://www.hbcpnetbase.com>, CRC Press, Boca Raton, FL, 2005; 11 pp,	
	5	DISTEFANO, et al., The Band Edge of Amorphous SiO2 By Photoinjection and Photoconductivity Measurements; Solid State Communications, Vol. 9, pp. 2259-2261, 1971, Pergamon Press; Printed in Great Britain	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16506022
	Filing Date	2019-07-09
	First Named Inventor	Daniel E. Grupp
	Art Unit	2815
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC12

	6	Fitting, et al., Monte-Carlo Approach of Electron Emission from SiO2; Phys. Stat. Sol. (a) 81, 323 (1984) pp. 323-332	
	7	IPR2020-01182; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; June 23, 2020; 139 pp.	
	8	IPR2020-01182; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 7,084,423; June 24, 2020; 76 pp.	
	9	IPR2020-01183; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; June 24, 2020; 178 pp.	
	10	IPR2020-01183; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 9,209,261; June 24, 2020; 81 pp.	
	11	IPR2020-01204; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; June 29, 2020; 178 pp.	
	12	IPR2020-01204; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 8,766,336; June 29, 2020; 78 pp.	
	13	IPR2020-01205; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; June 29, 2020; 142 pp.	
	14	IPR2020-01205; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 9,461,167; June 29, 2020; 63 pp.	
	15	IPR2020-01206; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; June 29, 2020; 164 pp.	
	16	IPR2020-01206; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 9,905,691; June 29, 2020; 76 pp.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16506022
	Filing Date	2019-07-09
	First Named Inventor	Daniel E. Grupp
	Art Unit	2815
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC12

	17	IPR2020-01207; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; June 29, 2020; 146 pp.	
	18	IPR2020-01207; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 10,090,395; June 29, 2020; 66 pp.	
	19	IPR2020-01241; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; July 6, 2020; 165 pp.	
	20	IPR2020-01241; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 9,461,167; July 6, 2020; 84 pp.	
	21	IPR2020-01264; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; July 8, 2020; 194 pp.	
	22	IPR2020-01264; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 8,766,336; July 8, 2020; 83 pp.	
	23	IPR2020-01279; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; July 9, 2020; 182 pp.	
	24	IPR2020-01279; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 9,905,691; July 10, 2020; 84 pp.	
	25	IPR2020-01282; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; July 12, 2020; 217 pp.	
	26	IPR2020-01282; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 10,090,395; July 13, 2020; 85 pp.	
	27	LANG et al., Theory of Metal Surfaces: Work Functon *; Physical Review B, Volume 3, Number 4; February 15, 1971; pp. 1215-1223.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16506022
	Filing Date	2019-07-09
	First Named Inventor	Daniel E. Grupp
	Art Unit	2815
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC12

	28	ROHATGI et al., Comprehensive Study of Rapid, Low-Cost Silicon Surface Passivation Technologies; IEEE Transactions on Electron Devices, Vol 47, No. 5, May 2000; pp. 987-993.
	29	SAKURAI, et al., Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas; IEEE Journal of Solid-State Circuits, Vo. 25, No. 2, April 1990, pp. 584-594.
	30	SIMMONS, John G., Generalized Formula for the Electric Tunnel Effect Between Similar Electrodes Separated by a Thin Insulating Film; Journal of Applied Physics, Volume 34, Number 6, June 1963; pp. 1793-1803.
	31	STESMANS et al., Si Dangling-Bond-Type Defects at the Interface of (100)Si with Ultrathin Layers of SiOx, Al2O3, and ZrO2; Applied Physics Letters, Volume 80, Number 11, March 18, 2002; pp. 1957-1959.
	32	SZYDLO, et al., I-V and C-V Characteristics of Au/TiO2 Schottky Diodes; J. Appl. Phys. 51(6), June 1980; pp. 3310-3312.
	33	ZHENG et al., Electronic Structure Differences in ZeO2 vs HfO2; J. Phys. Chem. A 2005, 109, pp.11521-11525.

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

GF Exhibit 1124 - 2542/2704

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16506022
Filing Date	2019-07-09
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.
Attorney Docket Number	3771-0003-DC12

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2020-07-15
Name/Print	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

GF Exhibit 1124 - 2544/2704

Electronic Acknowledgement Receipt

EFS ID:	40014413
Application Number:	16506022
International Application Number:	
Confirmation Number:	3561
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Jennifer Stewart
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC12
Receipt Date:	15-JUL-2020
Filing Date:	09-JUL-2019
Time Stamp:	20:26:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	2020-07-15_3771-0003-DC12_IDS_Statement.pdf	72567 186fcf42ffe6488638d428a89d2b64fabc1da5bf	no	2

Warnings:

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	2020-07-15_3771-0003-DC12_IDS_SB08_as_filed.pdf	614514 b9390826ac74cd6f604aad6459b809c7b741ca9d	no	7
Warnings:					
Information:					
3	Non Patent Literature	Archibong.pdf	653411 c2dd24b668002d7713a4b4d420a746d604c036b9	no	6
Warnings:					
Information:					
4	Non Patent Literature	Bortz.pdf	1179466 23b5dd6536d0c02c595fd0cd42104a2f8d3bd5cf	no	5
Warnings:					
Information:					
5	Non Patent Literature	Carver.pdf	2041896 13256f3d2944a73ed3abd1ef140ff682fb03038d	no	9
Warnings:					
Information:					
6	Non Patent Literature	CRC_Excerpt.pdf	4410691 34e776a03388520b05b4557d762c06c82c3053a5	no	11
Warnings:					
Information:					
7	Non Patent Literature	DiStefano.pdf	728621 e2cdc7e5ce29ead9aaf7691fab31e9e07a6b93df	no	3
Warnings:					
Information:					
8	Non Patent Literature	Fitting.pdf	1281134 591b0468fec3ff75b8b656a7cee8dc7fb2a8c272	no	10
Warnings:					
Information:					

9	Non Patent Literature	IPR2020-01182_Dec.pdf	2487967 0d5f83f2281ab04ee1c5398aeab27eb3efc86ada	no	139
Warnings:					
Information:					
10	Non Patent Literature	IPR2020-01182_Petition.pdf	1387311 0a24a6f51a203b42adfe2a4f9c2aff20122fa1b3	no	76
Warnings:					
Information:					
11	Non Patent Literature	IPR2020-01183_Dec.pdf	2984254 cc62928e9ec4cbe1041a2d4a68fe71db67e2c218	no	178
Warnings:					
Information:					
12	Non Patent Literature	IPR2020-01183_Petition.pdf	1547558 2edbe403667bd793edf5c389e2fea28f53ca10b2	no	81
Warnings:					
Information:					
13	Non Patent Literature	IPR2020-01204_Dec.pdf	2721409 328cd337309c33f5093462e39c93b674316c6bfe	no	167
Warnings:					
Information:					
14	Non Patent Literature	IPR2020-01204_Petition.pdf	1394819 603ef07d0d65b315e164842677903360df94ca8c	no	78
Warnings:					
Information:					
15	Non Patent Literature	IPR2020-01205_Dec.pdf	2479918 d4c86729e9f52371f8997168c867c8f520e8bacf	no	142
Warnings:					
Information:					

16	Non Patent Literature	IPR2020-01205_Petition.pdf	1273626 ac66c9655ad5f16b67b4bd699151e2edf7ab95ae	no	63
Warnings:					
Information:					
17	Non Patent Literature	IPR2020-01206_Dec.pdf	2994366 2e0b0c33c5cfd07db570de3c3975c37756d42f4a	no	164
Warnings:					
Information:					
18	Non Patent Literature	IPR2020-01206_Petition.pdf	1075189 bb3c13428dff58f80bf53c0ff4e1328162d86ce1	no	76
Warnings:					
Information:					
19	Non Patent Literature	IPR2020-01207_Dec.pdf	2822842 f33c074f0bf06a00e666ebeb7a0ae4a0edebc09e	no	146
Warnings:					
Information:					
20	Non Patent Literature	IPR2020-01207_Petition.pdf	1313963 96171196afd0ddd1db91190637101ad3a6c232fb	no	66
Warnings:					
Information:					
21	Non Patent Literature	IPR2020-01241_Dec.pdf	2626941 300287c7706cfb1e4a8e652471326695729 0df6f	no	165
Warnings:					
Information:					
22	Non Patent Literature	IPR2020-01241_Petition.pdf	1824376 74d367ef671ae938f07edd05b54ad8cbaf3a97fa	no	84
Warnings:					
Information:					

23	Non Patent Literature	IPR2020-01264_Dec.pdf	2493153 5a52055504ef7ba68f12adbc67cdc1ff9c554aa5	no	194
Warnings:					
Information:					
24	Non Patent Literature	IPR2020-01264_Petition.pdf	2121917 d8d412e76e2264a30e6f5512cf393b6db6dbba75	no	83
Warnings:					
Information:					
25	Non Patent Literature	IPR2020-01279_Dec.pdf	3085537 c9f95ef31474dc4918dba3adfe8742f79d77a472	no	182
Warnings:					
Information:					
26	Non Patent Literature	IPR2020-01279_Petition.pdf	2053661 123227cb45dc58c38997033290bf53342530f730	no	84
Warnings:					
Information:					
27	Non Patent Literature	IPR2020-01282_Dec.pdf	3720361 46b04411e7422e222b0ad6e643215383d39d200d	no	217
Warnings:					
Information:					
28	Non Patent Literature	IPR2020-01282_Petition.pdf	860880 84e289b4c42e76b3f51c16b08ed63c73425399f7	no	85
Warnings:					
Information:					
29	Non Patent Literature	Lang.pdf	1293754 3a408331a9a75c0d98ceff217647ed412bdd68f7	no	9
Warnings:					
Information:					

30	Non Patent Literature	Rohatgi.pdf	1047833 6af7099070e885b67e81572e402fc5f1f5b4894f	no	7
Warnings:					
Information:					
31	Non Patent Literature	Sakurai.pdf	2667974 b0d3a2342e2ef1be5bca929af0dba20d697bf37c	no	11
Warnings:					
Information:					
32	Non Patent Literature	Simmons.pdf	2094070 f3690af22c63aff9809162579c1a02a1f75a7c4c	no	11
Warnings:					
Information:					
33	Non Patent Literature	Stesmans.pdf	632891 fd6ad3e11bd5622c7e24b8a76f6bd8d0dba1f183	no	3
Warnings:					
Information:					
34	Non Patent Literature	Szydlo.pdf	774312 61f735cec595e161c8f61b98637680dd27f5252b	no	3
Warnings:					
Information:					
35	Non Patent Literature	Zheng.pdf	655606 bc806d41f8239788eb919eb1af70f8a9e218d74d	no	5
Warnings:					
Information:					
			Total Files Size (in bytes):	63418788	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Daniel E. Grupp

Application No.: 16/506,022
Filed: 07/09/2019

Examiner: Harrison, Monica D.
Art Unit: 2815

Docket No.: 3771-0003-DC12

Customer No.: 27571

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

In accordance with the duty of disclosure, enclosed is a copy of IDS Citation Form PTO/SB/08, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g. copies of U.S. patents and U.S. published patent applications that need not be included). This IDS and IDS Citation Form are being submitted before the mailing of a First Office Action. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account No. 50-5798.

Respectfully submitted,

Date: July 15, 2020

/Tarek N. Fahmi/
Tarek N. Fahmi, Reg. No. 41,402

ASCENDA LAW GROUP, PC
2150 N First Street, Suite 420
San Jose, CA 95131
(866) 877-4883

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16506022
Filing Date	2019-07-09
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	HARRISON, MONICA D
Attorney Docket Number	3771-0003-DC12

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20040129087	A1	2004-07-08	ROWE; et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

GF Exhibit 1124 - 2554/2704

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16506022
	Filing Date	2019-07-09
	First Named Inventor	Daniel E. Grupp
	Art Unit	2815
	Examiner Name	HARRISON, MONICA D
	Attorney Docket Number	3771-0003-DC12

	1	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

GF Exhibit 1124 - 2555/2704

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16506022
Filing Date	2019-07-09
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	HARRISON, MONICA D
Attorney Docket Number	3771-0003-DC12

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2020-08-27
Name/Print	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

GF Exhibit 1124 - 2557/2704

Electronic Acknowledgement Receipt

EFS ID:	40404794
Application Number:	16506022
International Application Number:	
Confirmation Number:	3561
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC12
Receipt Date:	27-AUG-2020
Filing Date:	09-JUL-2019
Time Stamp:	17:24:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	3771-0003-DC12_IDS.pdf	1034325 0841840f6e36b1cbf495a654c8a20b8cb29f1650	no	4

Warnings:

Information:	
Total Files Size (in bytes):	1034325

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/506,022	07/09/2019	Daniel E. Grupp	3771-0003-DC12	3561

27571 7590 09/21/2020

Ascenda Law Group, PC
2150 N First Street
Suite 420
San Jose, CA 95131

EXAMINER
HARRISON, MONICA D

ART UNIT	PAPER NUMBER
2815	

NOTIFICATION DATE	DELIVERY MODE
09/21/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@ascendalaw.com
tarek.fahmi@ascendalaw.com

GF Exhibit 1124 - 2560/2704

Office Action Summary	Application No. 16/506,022	Applicant(s) Grupp et al.	
	Examiner MONICA D HARRISON	Art Unit 2815	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 7/9/19.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-20 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 7/9/19 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 6/17/2020,7/15/2020,8/27/2020.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Priority

1. This application discloses and claims only subject matter disclosed in prior application no 15/728,002, filed 10/19/17, and names the inventor or at least one joint inventor named in the prior application. Accordingly, this application may constitute a continuation or division. Should applicant desire to claim the benefit of the filing date of the prior application, attention is directed to 35 U.S.C. 120, 37 CFR 1.78, and MPEP § 211 *et seq.*

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been

obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP § 2146 *et seq.* for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should

be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 1-7 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 2 and 4 of U.S. Patent No. 9,905,691 B2 (Grupp et al). Although the claims at issue are not identical, they are not patentably distinct from each other because the claimed subject matter of claims 1-7 of the instant application may be found in claims 1, 2 and 4 of the patent.

2. Regarding claim 1, Grupp et al 691' discloses an electrical junction, comprising: a semiconductor region in a substrate; a metal electrical contact proximate to said semiconductor region; and an interface layer disposed between said semiconductor region and said metal electrical contact, said interface layer including a first layer containing a passivating material and a second layer that displaces the semiconductor region from the metal electrical contact, said semiconductor region being electrically connected to said metal electrical contact through said interface layer (claim 1).

3. Regarding claim 2, Grupp et al 691’ discloses wherein the metal electrical contact comprises a metal silicide (claim 2).

4. Regarding claim 3, Grupp et al 691’ discloses wherein the semiconductor region comprises a source of a transistor (claim 4).

5. Regarding claim 4, Grupp et al 691’ discloses wherein the semiconductor region comprises n-type doped silicon (claim 4).

6. Regarding claim 5, Grupp et al 691’ discloses wherein the second layer comprises an oxide (claim 1).

7. Regarding claim 6, Grupp et al 691’ discloses wherein the first layer comprises a semiconductor oxide (claim 1).

8. Regarding claim 7, Grupp et al 691’ discloses wherein the second layer comprises an oxide (claim 1).

Claims 8-20 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-3, 5-7 and 10 of U.S. Patent No. (9,425,277 B2). Although the claims at issue are not identical, they are not patentably distinct from each other because the claimed subject matter of claims 8-20 of the instant application may be found in claims 1-3, 5-7 and 10 of the patent.

9. Regarding claim 8, Grupp et al 277’ discloses an electrical junction, comprising: a semiconductor region in a substrate; a metal layer in electrical contact with said semiconductor region; and an interface layer disposed between said

semiconductor region and said metal layer, said interface layer including a monolayer of passivating material and configured to reduce a specific electrical contact resistance between the metal layer and the semiconductor region from that which would exist at a junction between the metal layer and the semiconductor region without the interface layer disposed between the semiconductor region and the metal layer, said semiconductor region being electrically connected to said metal layer through said interface layer (claims 1 and 3).

10. Regarding claim 9, Grupp et al 277’ discloses wherein the semiconductor region comprises silicon and the metal layer comprises a metal silicide (claim 2).

11. Regarding claim 10, Grupp et al 277’ discloses wherein the semiconductor region comprises n-type doped silicon (claim 5).

12. Regarding claim 11, Grupp et al 277’ discloses wherein the semiconductor region comprises a source of a transistor (claim 7).

13. Regarding claim 12, Grupp et al 277’ discloses wherein the semiconductor region comprises n-type doped silicon (claim 5).

14. Regarding claim 13, Grupp et al 277’ discloses wherein the monolayer of passivating material comprises arsenic (claims 1 and 3).

15. Regarding claim 14, Grupp et al 277’ discloses wherein the monolayer of passivating material comprises an element of same valence as arsenic (claims 1 and 3).

16. Regarding claim 15, Grupp et al 277’ discloses wherein the monolayer of passivating material comprises nitrogen (claim 1).

17. Regarding claim 16, Grupp et al 277’ discloses wherein the monolayer of passivating material comprises oxygen (claim 1).

18. Regarding claim 17, Grupp et al 277’ discloses wherein the specific electrical contact resistance between the metal layer and the semiconductor is less than 100 Ohm-micron2 (claim 1).

19. Regarding claim 18, Grupp et al 277’ discloses wherein the specific electrical contact resistance between the metal layer and the semiconductor is less than 1 Ohm-micron2 (claim 10).

20. Regarding claim 19, Grupp et al 277’ discloses wherein the semiconductor region comprises n-type doped silicon germanium (claims 5 and 6).

21. Regarding claim 20, Grupp et al 277’ discloses wherein the semiconductor region comprises n-type doped silicon germanium (claims 5 and 6).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MONICA D HARRISON whose telephone number is (571)272-1959. The examiner can normally be reached on M-F 7-4:30pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MONICA D HARRISON/
Primary Examiner, Art Unit 2815

mdh
September 15, 2020

Notice of References Cited	Application/Control No. 16/506,022	Applicant(s)/Patent Under Reexamination Grupp et al.	
	Examiner MONICA D HARRISON	Art Unit 2815	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-9905691-B2	02-2018	Grupp; Daniel E.	H01L29/1608	1/1
*	B	US-9425277-B2	08-2016	Grupp; Daniel E.	H01L29/78	1/1
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

GF Exhibit 1124 - 2570/2704

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/506,022	Grupp et al.
	Examiner	Art Unit
	MONICA D HARRISON	2815

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/10/2019	12/18/2019	09/15/2020						
1	1	✓	=	✓						
2	2		=	✓						
3	3		=	✓						
4	4		=	✓						
5	5		=	✓						
6	6		=	✓						
7	7		=	✓						
8	8		=	✓						
9	9		=	✓						
10	10		=	✓						
11	11		=	✓						
12	12		=	✓						
14	13		=	✓						
15	14		=	✓						
16	15		=	✓						
17	16		=	✓						
18	17		=	✓						
19	18		=	✓						
20	19		=	✓						
13	20		=	✓						

GF Exhibit 1124 - 2571/2704

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/506,022	Grupp et al.
	Examiner	Art Unit
	MONICA D HARRISON	2815

CPC - Searched*		
Symbol	**Date**	**Examiner**
H01L29/ 08,089,0895,16,160,1608,161,45,47,66,661,6614,66143,666,6664,6 6643,78,783,7839,785,80,806,81,812,87,872	09/10/2019	MDH
H01L21/28,285,2853,28537	09/10/2019	MDH
H01L29/45,456	09/15/2020	MDH

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
257	763	09/10/2019	MDH

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/MONICA D HARRISON/ Primary Examiner, Art Unit 2815	

GF Exhibit 1124 - 2572/2704

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/506,022	Grupp et al.
	Examiner	Art Unit
	MONICA D HARRISON	2815

Search Notes		
Search Notes	**Date**	**Examiner**
East (USPAT, US-PGPUB, USOCR, EPO, JPO, DERWENT, IBM_TDB, FPRS)	09/10/2019	MDH
East updated	12/18/2019	MDH
GRUPP ET AL .inv.	12/18/2019	MDH
ACORN SEMI .asn.	12/18/2019	MDH
USPAT, US-PGPUB txt .clm.	12/18/2019	MDH
East updated	09/15/2020	MDH
IPR2020-01182 Reviewed Petition for the Inter Partes Review of US. Patent No. 7,084,423 and Exhibits Ex.1001-Ex.1024	09/15/2020	MDH
IPR2-2020-1206 Reviewed Petition for the Inter Partes Review of US . Patent No. 9,905,691 and Exhibits Ex.1001-Ex.1035	09/15/2020	MDH
IPR2-2020-01279 Reviewed Petition for the Inter Partes Review of US. Patent No. 9,905,691 and Exhibits Ex.1101-Ex.1150	09/15/2020	MDH

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
	USPAT, US-PGPUB txt .clm.	12/18/2019	MDH

/MONICA D HARRISON/ Primary Examiner, Art Unit 2815	

GF Exhibit 1124 - 2573/2704

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	("7084423" | "3983264").pn. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 14:33
L2	1	("7084423" | "3983264").pn. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 14:40
L3	1	("7084423" | "3983264").pn. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4) and monolayer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 15:00

L4	60	("20040129087" | "20060178015" | "20140117465" | "4304042" | "4691219" | "5614745" | "6323508" | "6521502" | "0000001" | "0000002" | "10090395" | "20050093027" | "2981877" | "3614548" | "3623925" | "3719797" | "3877054" | "3983264" | "4110488" | "4278830" | "4356622" | "4485265" | "4538342" | "4696828" | "4698652" | "4752815" | "4763176" | "4772934" | "4794444" | "4796082" | "4800415" | "4801984" | "4835580" | "4960732" | "4961194" | "6724088" | "7176483" | "9461167" | "9905691" | "3590471" | "3708360" | "3983574" | "4019113" | "4056642" | "4300152" | "4338616" | "4422090" | "4485550" | "4566021" | "4583110" | "4689869" | "4723197" | "4811077" | "4843029" | "4999685" | "5021365" | "5027166" | "5098859" | "5191322" | "5216262").PN.	US-PGPUB; USPAT	OR	OFF	2020/09/15 15:08
L5	6	(substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4) and monolayer and L4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 15:09
L7	0	257/763.ccls. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4) and monolayer and L4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 15:47
L8	3	257/'$'.ccls. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4) and monolayer and L4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/09/15 15:49

			DERWENT; IBM_TDB			
L9	1,551	H01L29/45,456.cpc. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 15:57
L10	119	H01L29/45,456.cpc. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4) and monolayer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 15:59
L11	119	H01L29/45,456.cpc. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4) and monolayer and transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 15:59
L12	93	H01L29/45,456.cpc. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide)	US-PGPUB; USPAT;	OR	ON	2020/09/15 16:00

		and (source drain) with (metal electrode conduct$4) and monolayer and (semiconductor near oxide)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L13	66	H01L29/45,456.cpc. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4) and monolayer and (semiconductor near oxide) and junction	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 16:09
L14	165	H01L29/08,089,0895,16,1608,161,45,456,66,661,6614,66143,664,666,66643,78,783,7839,785,80,806,81,812,872.cpc. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4) and monolayer and (semiconductor near oxide) and junction	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 16:10
L15	51	H01L21/28,285,2853,28537.cpc. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4) and monolayer and (semiconductor near oxide) and junction	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 16:20

L16	14	"15728002"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 16:28
L17	12	"15251210"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 16:38
L18	18	"15048877"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 16:39
L19	4	"16847878"	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2020/09/15 16:55

			JPO; DERWENT; IBM_TDB			
L20	2	"15506022"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 16:56
L21	14	"15728002"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 16:57
L22	12	"15251210"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 17:24
L23	18	"15048877"	US-PGPUB; USPA	OR	ON	2020/09/15 17:27

			T; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L24	22	"13552556"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 17:33
L25	25	"13022522"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 17:34
L26	25	"12197996"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2020/09/15 17:35

			IBM_TDB			
L27	36	"11181217"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 17:35
L28	76	"10217758"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 17:36
S1	4	"16506022"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 09:51
S2	60	("20040129087" | "20060178015" | "20140117465" | "4304042" | "4691219" | "5614745" | "6323508" | "6521502" | "0000001" | "0000002" | "10090395" | "20050093027" | "2981877" | "3614548" | "3623925" | "3719797" | "3877054" | "3983264" | "4110488" | "4278830" | "4356622" | "4485265" | "4538342" | "4696828" | "4698652" | "4752815" | "4763176" | "4772934" | "4794444" | "4796082" | "4800415" | "4801984" | "4835580" |	US-PGPUB; USPAT	OR	OFF	2020/09/15 12:38

		"4960732" | "4961194" | "6724088" | "7176483" | "9461167" | "9905691" | "3590471" | "3708360" | "3983574" | "4019113" | "4056642" | "4300152" | "4338616" | "4422090" | "4485550" | "4566021" | "4583110" | "4689869" | "4723197" | "4811077" | "4843029" | "4999685" | "5021365" | "5027166" | "5098859" | "5191322" | "5216262").PN.				
S3	7	("7084423" | "3983264").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 12:39
S4	2	("7084423" | "3983264").pn. and (substrate wafer carrier base plate) with semiconductor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 12:45
S5	2	("7084423" | "3983264").pn. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 12:56
S6	2	("7084423" | "3983264").pn. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with	US-PGPUB;	OR	ON	2020/09/15 12:58

		semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S7	2	("7084423" | "3983264").pn. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 13:10

EAST Search History (Interference)

<This search history is empty>

9/15/2020 7:04:03 PM
C:\Users\mharrison1\Documents\EAST\Workspaces\16506022.wsp

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	1	of	24	**Attorney Docket No:** 3771-0003-DC12

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number-Kind Code[2](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		2981877	1961-04-25	Noyce	
		3614548	1971-10-19	Inoue	
		3623925	1971-11-30	Jenkins, et al.	
		3719797	1973-03-06	Andrews, Jr., et al.	
		3877054	1975-04-08	Boulin, et al.	
		3983264	1976-09-28	Schroen, et al.	
		4110488	1978-08-29	Risko	
		4278830	1981-07-14	Stirn, et al.	
		4356622	1982-11-02	Widmann	
		4485265	1984-11-27	Gordon, et al.	
		4538342	1985-09-03	Camlibel, et al.	
		4696828	1987-09-29	Schachter, et al.	
		4698652	1987-10-06	Umemoto, et al.	
		4752815	1988-06-21	Tsao	
		4763176	1988-08-09	Ito	
		4772934	1988-09-20	Cunningham, et al.	
		4794444	1988-12-27	Liu, et al.	
		4796082	1989-01-03	Murakami, et al.	
		4800415	1989-01-24	Simmons, et al.	
		4801984	1989-01-31	Woodall	
		4835580	1989-05-30	Havemann, et al.	
		4960732	1990-10-02	Dixit, et al.	
		4961194	1990-10-02	Kuroda, et al.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	2	of	24	**Attorney Docket No:** 3771-0003-DC12

		5013685	1991-05-07	Chiu, et al.	
		5019530	1991-05-28	Kleinsasser, et al.	
		5021840	1991-06-04	Morris	
		5045502	1991-09-03	Lau, et al.	
		5086321	1992-02-04	Batey, et al.	
		5093280	1992-03-03	Tully	
		5216271	1993-06-01	Takagi, et al.	
		5216282	1993-06-01	Cote, et al.	
		5231306	1993-07-27	Meikle, et al.	
		5238872	1993-08-24	Thalapaneni	
		5292677	1994-03-08	Dennison	
		5294834	1994-03-15	Fatemi, et al.	
		5355021	1994-10-11	Crouch, et al.	
		5358574	1994-10-25	Sapori	
		5442200	1995-08-15	Tischler	
		5480829	1996-01-02	Abrokwah, et al.	
		5488231	1996-01-30	Kwon, et al.	
		5534449	1996-07-09	Dennison, et al.	
		5563448	1996-10-08	Lee, et al.	
		5592736	1997-01-14	Akram, et al.	
		5619057	1997-04-08	Komatsu	
		5654234	1997-08-05	Shih, et al.	
		5677553	1997-10-14	Yamamoto, et al.	
		5689125	1997-11-18	Vaccaro, et al.	
		5744817	1998-04-28	Shannon	
		5789312	1998-08-04	Buchanan, et al.	
		5793109	1998-08-11	Nakamura	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	3	of	24	**Attorney Docket No:** 3771-0003-DC12

		5793788	1998-08-11	Inaba, et al.	
		5851912	1998-12-22	Liaw, et al.	
		5869364	1999-02-09	Nakano, et al.	
		5876796	1999-03-02	Regolini, et al.	
		5897331	1999-04-27	Sopori	
		5903053	1999-05-11	Iijima, et al.	
		5962883	1999-10-05	Hong, et al.	
		5985759	1999-11-16	Kim, et al.	
		6004879	1999-12-21	Hu, et al.	
		6015997	2000-01-18	Hu, et al.	
		6017790	2000-01-25	Liou, et al.	
		6057564	2000-05-02	Rennie	
		6130503	2000-10-10	Negishi, et al.	
		6144097	2000-11-07	Asahina, et al.	
		6144098	2000-11-07	Iyer	
		6150246	2000-11-21	Parsons	
		6150672	2000-11-21	Kaneko	
		6166487	2000-12-26	Negishi, et al.	
		6190975	2001-02-20	Kubo, et al.	
		6222267	2001-04-24	Omura, et al.	
		6225168	2001-05-01	Gardner, et al.	
		6268233	2001-07-31	Sano	
		6274905	2001-08-14	Mo	
		6284557	2001-09-04	Yiu, et al.	
		6287946	2001-09-11	Micovic, et al.	
		6303942	2001-10-16	Farmer, II	
		6320238	2001-11-20	Kizilyalli, et al.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	4	of	24	**Attorney Docket No:** 3771-0003-DC12

		6346465	2002-02-12	Miura, et al.	
		6350685	2002-02-26	Asahina, et al.	
		6372536	2002-04-16	Fischer, et al.	
		6373076	2002-04-16	Alok, et al.	
		6388272	2002-05-14	Odekirk	
		6396191	2002-05-28	Hagelstein, et al.	
		6426542	2002-07-30	Tan	
		6444516	2002-09-03	Clevenger, et al.	
		6451690	2002-09-17	Matsumoto, et al.	
		6468890	2002-10-22	Bartsch, et al.	
		6509254	2003-01-21	Matsumoto, et al.	
		6511905	2003-01-28	Lee, et al.	
		6511910	2003-01-28	Asahina, et al.	
		6555455	2003-01-29	Wang, et al.	
		6559069	2003-05-06	Goldbach, et al.	
		6593219	2003-07-15	Matsumoto, et al.	
		6593229	2003-07-15	Yamamoto, et al.	
		6599644	2003-07-29	Zekentes, et al.	
		6605832	2003-08-12	Van De Walle	
		6639288	2003-10-28	Kunikiyo	
		6914272	2005-07-05	Goetz, et al.	
		6972436	2005-12-06	Das, et al.	
		6979846	2005-12-27	Yagishita, et al.	
		6995430	2006-02-07	Langdo, et al.	
		7579231	2009-08-25	Matsuo, et al.	
		7863606	2011-01-04	Sung	
		9209261	2015-12-08	Grupp, et al.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	5	of	24	**Attorney Docket No:** 3771-0003-DC12

		20010030342	2001-10-18	Ohnishi, et al.	
		20010030352	2001-10-18	Ruf, et al.	
		20010030352	2001-10-18	Ruf, et al.	
		20020017658	2002-02-14	Tsubouchi, et al.	
		20020098692	2002-07-25	Miura	
		20020106536	2002-08-08	Lee, et al.	
		20020163012	2002-11-07	Nihei, et al.	
		20020179980	2002-12-05	Yagishita, et al.	
		20020179993	2002-12-05	Hshieh, et al.	
		20030015707	2003-01-23	Bosco, et al.	
		20030020069	2003-01-30	Holmes, et al.	
		20030020165	2003-01-30	Matsumoto	
		20030098489	2003-05-29	Amos, et al.	
		20030132452	2003-07-17	Boriuchi	
		20030109114	2003-06-12	Niwa	
		20030193074	2003-10-16	Hshieh, et al.	
		20040038467	2004-02-26	Darwish, et al.	
		20040093575	2004-05-13	Heath, et al.	
		20041029087	2004-07-08	Rowe, et al.	
		20120181632	2012-07-19	Watanabe, et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3]-Number[4]-Kind Code[5](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		EP 0 042 066 A2	1981-12-23	IBM		

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	6	of	24	**Attorney Docket No:** 3771-0003-DC12

		EP 0 068 897 A2	1983-01-05	HITACHI LTD		
		EP 0 111 364 A2	1984-06-20	PHILIPS NV		
		EP 0 168 125 A1	1986-01-15	FUJITSU LTD		
		EP 0 458 353 B1	1991-11-27	SUMITOMO ELECTRIC INDUSTRIES		
		EP 0 789 388 A2	1997-08-13	AGENCY IND SCIENCE TECHN		
		FR 2 814 856 A1	2002-04-05	ST MICROELECTRONICS SA		X
		GB 1 22 594 A	1919-01-30	LETTS GEORGE KNIGHT		
		JP S62-61363 A	1987-03-18	HITACHI LTD		X
		JP S63-157466 A	1988-06-30	FUJITSU LTD		X
		JP 2000-101064 A	2000-04-07	SANYO ELECTRIC CO		X
		JP 2000-101100 A	2000-04-07	TOSHIBA CORP		X
		JP 2000-174261 A	2000-06-23	FUJITSU LTD		X
		JP 2000-195954 A	2000-07-14	SEIKO EPSON CORP		X
		JP 2000-216241 A	2000-08-04	APPLIED MATERIALS INC		X
		JP 2000-228523 A	2000-08-15	NEC CORP		X
		JP 2000-236086 A	2000-08-29	NEC CORP		X
		JP 2000-299479 A	2000-10-24	NEW JAPAN RADIO CO LTD		X
		JP 2001-223180 A	2001-08-17	HITACHI LTD		X
		JP 2002-075909 A	2002-03-15	NAT INST OF ADV IND & TECHNOL; et al.		X
		JP 2002-093742 A	2002-03-29	NAT INST OF ADV IND & TECHNOL; et al.		X
		JP 2002-151428 A	2002-05-24	TOSHIBA CORP		X

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	7	of	24	**Attorney Docket No:** 3771-0003-DC12

		JP 2002-184978 A	2002-06-28	TOSHIBA CORP		X
		JP 2002-217425 A	2002-08-02	SANKEN ELECTRIC CO LTD		X
		JP 2630279 B2	1997-07-16	NIPPON DENKI KK		X
		JP 3191728 B2	2001-07-23	NEC CORP		X
		JP 3208599 B2	2001-09-17	SONY CORP		X
		JP H01-186672 A	1989-07-26	NEC CORP		X
		JP H02-26073 A	1990-01-29	IBM		X
		JP H03-29355 A	1991-02-07	SANYO ELECTRIC CO		X
		JP H03-191518 A	1991-08-21	NEC CORP		X
		JP H03-274735 A	1991-12-05	HITACHI LTD; et al.		X
		JP H04-199628 A	1992-07-20	SEIKO EPSON CORP		X
		JP H04-284668 A	1992-10-09	FUJITSU LTD; et al.		X
		JP H06-5737 B2	1994-01-19	NIPPON ELECTRIC CO		X
		JP H06-53165 A	1994-02-25	SONY CORP		X
		JP H06-61177 A	1994-03-04	HITACHI LTD; et al.		X
		JP H07-122519 A	1995-05-12	OMI TADAHIRO		X
		JP H07-263375 A	1995-10-13	TELEFUNKEN MICROELECTRON		X
		JP H08-64800 A	1996-03-08	HITACHI LTD		X
		JP H08-167693 A	1996-06-25	SHARP KK		X
		JP H09-289178 A	1997-11-04	MATSUSHITA ELECTRIC IND CO LTD		X
		JP H10-27847 A	1998-01-27	MITSUBISHI ELECTRIC CORP		X
		JP H10-74707 A	1998-03-17	APPLIED MATERIALS INC		X
		JP H10-135452 A	1998-05-22	IBM		X
		JP H10-209445 A	1998-08-07	NEC CORP		X

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	8	of	24	**Attorney Docket No:** 3771-0003-DC12

		JP H10-335265 A	1998-12-18	SONY CORP		X
		JP H11-26713 A	1999-01-29	HITACHI LTD		X
		JP H11-162874 A	1999-06-18	SHINDENGEN ELECTRIC MFG		X
		JP H11-233760 A	1999-08-27	JAPAN ATOMIC ENERGY RES INST		X
		JP H11-330482 A	1999-11-30	TOSHIBA CORP		X
		JP S61-133646 A	1986-06-20	TOSHIBA CORP		X
		JP S63-175471 A	1988-07-19	NIPPON TELEGRAPH & TELEPHONE		X
		KR 10-0197653 B1	1999-06-15	HYUNDAI ELECTRONICS IND		X
		KR 10-0290467 B1	2001-03-02	HYNIX SEMICONDUCTOR INC		X
		KR 92-002350 B1	1992-03-21	PANASONIC CORPORATION		X
		KR 1991-0006249 B1	1991-08-17	HITACHI, LTD.		X
		KR 1992-0010131 B1	1992-11-16	AT&T Corp.		X
		KR 1994-0020550 A	1994-09-16	SAMSUNG ELECTRONICS CO., LTD.		X
		KR 1995-0010873 B1	1995-09-25	SAMSUNG ELECTRONICS CO., LTD.		X
		KR 1997-0030333 A	1997-06-26	SK hynix Inc.		X
		KR 1998-0024649 A	1998-07-06	KUBO; et al.		X
		KR 1999-0025041 A	1999-04-06	YOON; et al.		X
		KR 1999-0045323 A	1999-06-25	HASEGAWA; et al.		X
		KR 2000-0025576 A	2000-05-06	SAMSUNG ELECTRONICS CO LTD		X

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	9	of	24	**Attorney Docket No:** 3771-0003-DC12

		KR 2000-0027908 A	2000-05-15	UNITED MICROELECTRONICS CORP.		X
		SE 0875077 T3	2004-01-07	ABB RESEARCH LTD.		X
		WO 88/00392 A1	1988-01-14	AMERICAN TELEPHONE & TELEGRAPH		
		WO 93/11558 A1	1993-06-10	MATERIALS RESEARCH CORP		
		WO 95/34095 A1	1995-12-14	ADVANCED TECH MATERIALS		
		WO 97/26678 A2	1997-07-24	HARRIS CHRISTOPHER; et al.		
		WO 97/33308 A1	1997-09-12	3C SEMICONDUCTOR CORP; et al.		
		WO 01/28677 A1	2001-04-26	NEOKISMET LLC		
		WO 01/63677 A1	2001-08-30	CENTRE NAT RECH SCIENT; et al.		

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No.**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T2**
		Aboelfotoh, Schottky Barrier Heights of Refractory Metals on Silicon, Materials Research Soc., Vol. 71, 1986, pp. 273-285.	
		Aboelfotoh, et al., Schottky-barrier heights of Ti and TiSi2 on *n*-type and *p*-type Si(100), Physical Review B, Vol. 34, No. 4, Aug. 15, 1986, pp. 2311-2317.	
		Aboelfotoh, et al., Schottky-barrier height of a Ti-W alloy on n- type and p-type Si, Physical Review B, Vol. 33, No. 10, May 15, 1986, pp. 6572-6578.	
		Aboelfotoh, Temperature Dependence of the Schottky-Barrier Height of Tungsten on n-Type and p-Type Silicon, Solid-State Elecs, Vol. 34, No. 1, 1991, pp. 51-55.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	10	of	24	**Attorney Docket No:** 3771-0003-DC12

		Asamizu, et al., Formation Mechanism of Low Contact Resistance PdZn-Based Ohmic Contacts for p-type InP, Materials Transactions, Vol. 43, No. 6, 2002, pp. 1352-1359.	
		Bard, et al., The Concept of Fermi Level Pinning at Semiconductor/Liquid Junctions, Consequences for Energy Conversion Efficiency and Selection of Useful Solution Redox Couples in Solar Devices, Journal of the Am. Chem. Soc., Vol. 12, No. 11, May 21, 1980, pp. 3671-3677.	
		Beatty, Metallization Systems for Integrated Circuits, NASA Technical Note D-5866, Jul. 1970., 26 pgs.	
		Boswell, Low Resistance Gold Contacts for Gallium Nitride, Gold Bulletin, Vol. 31, No. 4, 1998, pp. 132-133.	
		Calvet, Electrical Transport in Schottky Barrier MOSFETS, Dissertation, Yale Univ., May 2001, 183 pgs.	
		Campbell, et al., Titanium dioxide (TiO2)-based gate insulators, IBM Journal of Research Development, Vol. 43, No. 3, May 1999, pp. 383-392.	
		Card, et al., Studies of tunnel MOS diodes I. Interface effects in silicon Schottky diodes, Journal of Applied. Physics, Vol. 4, Jun. 1971, pp. 1589-1601.	
		Chang, et al., Specific Contact Resistance of Metal-Semiconductor Barriers, Solid-State Elecs., Vol. 14, 1971, pp. 541-550.	
		Cheek, et al., MIS and SIS Silicon Solar Cells: A Review, Photovoltaic Solar Energy Conf., 1981, pp. 353-357.	
		Chen, et al., Band structure of Al/Si/n-type GaAs with a strained Si interfacial layer, Physical Review B, Vol. 52, No. 7, Feb. 15, 1996, pp. 3879-3884.	
		Chen, et al., Properties of TiO2- GaAs Interface, Final Report on NASA Grant No. NSG 1202-S1, Jun. 1977, 100 pgs.	
		Chen, et al., The Use of Refractory Metal and Electron- Beam Sintering to Reduce Contact Resistance for VLSI, IEEE Trans. on Electron Devices, Vol. ED-30, No. 11, Nov. 1983, pp. 1542-1550.	
		Chourasia, et al., X-ray photoelectron study of TiN/SiO2 and TiN/Si interfaces, Thin Solid Films, Vol. 266, 1995, pp. 298-301.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	11	of	24	**Attorney Docket No:** 3771-0003-DC12

		Claflin, et al., Interface formation and thermal stability of advanced metal gate and ultrathin gate dielectric layers, Journal of Vacuum Sci., & Tech., Vol. 16, No. 4, Jul./Aug. 1998, pp. 2154-2158.	
		Claflin, et al., Interface studies of tungsten nitride and titanium nitride composite metal gate electrodes with within dielectric layers, Journal of Vacuum Sci., & Tech., Vol. 16, No. 3, May/Jun. 1998, pp. 1757-1761.	
		Clarke, et al., Non-Equilibrium Effects on Metal-Oxide-Semiconductor Tunnel Currents, Solid-State Elecs., Vol. 14, 1971, pp. 957-973.	
		Cohen, et al., Chapter 6: Practical Ohmic Contacts to Silicon, VLSI Electronics Microstructure Sci., Vol. 13, 1986, pp. 213-310.	
		Connelly, et al., Speed Advantage of Optimized Metal S/D in 25 nm Dual-Gate Fully-Depleted CMOS, 60th DRC Conf. Digest Device Research Conf., 2002, pp. 1-2.	
		Costa, et al., Unpinned GaAs Schottky barriers with an epitaxial silicon layer, Journal of Applied Physics, Vol. 70, No. 4, Aug. 15, 1991. Pp. 2173-2184.	
		Cowley, Titanium-Silicon Schottky Barrier Diodes, Solid-State Elecs., Vol. 12, 1970, pp. 403-414.	
		Davis, et al., Low Temperature Deposition and Characterization of N- and P-Type Silicon Carbide Thin Films and Associated Ohmic and Schottky Contacts, Semiannual Technical Report, Jun. 1995, 32 pgs.	
		Depas, et al., Electrical Characteristics of A1/SiO2/n-Si Tunnel Diodes with an Oxide Layer Grown by Rapid Thermal Oxidation, Solid-State Elecs., Vol. 37, No. 3, 1994, pp. 433-441.	
		d'Heurle, Interfaces in Silicides, Journal de Physique IV Colloque, Vol. 6, Mar. 1996, pp. C2-29-C2-46.	
		d'Heurle, Silicide interfaces in silicon technology, Journal of Elec. Materials, Vol. 27, No. 11, Nov. 1998, 16 pgs.	
		Dubois, et al., Low Schottky barrier source/drain for advanced MOS architecture: device design and material considerations, Solid-State Elecs., Vol. 46, 2002, pp. 997-1004.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	12	of	24	**Attorney Docket No:** 3771-0003-DC12

		EMC Corp., 2002 EMC At-a-Glance: EMC Plenary Lecture/Student Awards, 2002 Elec. Materials Conf., Jun. 26, 2002, 107 pgs.	
		Eun, et al., High Temperature Ohmic Contact Technology to N-Type GaAs, ECE Technical Reports, Purdue Univ., Jan. 1993, 113 pgs.	
		Fan, et al., Very low resistance multilayer Ohmic contact to n-GaN, Applied Physics Letters, Vol. 68, No. 12, Mar. 18, 1996, pp. 1672-1674.	
		Franciosi, et al., Heterojunction band offset engineering, Surface Sci. Reports, Vol. 25, 1996, pp. 1-140.	
		Frangoul, et al., The Fabrication of Metal-Oxide Semiconductor Transistors Using Cerium Dioxide as a Gate Oxide Material, Journal of Vacuum Sci. & Tech, Vol. 9, No. 1, Jan./Feb. 1991, pp. 181-183.	
		Fulton, et al., Electronic states at the interface of Ti-Si oxide on Si(100), Journal of Vacuum Sci. & Tech., Vol. 20, No. 4, Jul./Aug. 2002, pp. 1726-1731.	
		Gessmann, et al., Ohmic contact technology in III nitrides using polarization effects of cap layers, Journal of Applied Physics, Vol. 92, No. 7, Oct. 1, 2002, pp. 3740-3744.	
		Getto, et al., Characterization of sputtered titanium silicide ohmic contacts on n-type 6H-silicon carbide, Materials Sci. and Eng'g B61-62, 1999, pp. 270-274.	
		Giboney, Travelling-Wave Photodetectors, Thesis, Univ. of Calif. at Santa Barbara, Aug. 1995, 170 pgs.	
		Glass, et al., Low energy ion- assisted deposition of titanium nitride ohmic contacts on alpha (6H)-silicon carbide, Applied Physics Letters, Vol. 59, No. 22, Nov. 25, 1991, pp. 2868-2870.	
		Gordon, 5 – Depositions and Reactions of Metals and Metal Compounds, Harvard Univ., pp. 171-196.	
		Green, et al., Current Multiplication in Metal-Insulator-Semiconductor (MIS) Tunnel Diodes, Solid-State Elecs., Vol. 17, 1974, pp. 349-365.	
		Green, et al., Minority Carrier MIS Tunnel Diodes and Their Application to Electron- and Photo- Voltaic Energy Conversion – I. Theory, Solid-State Elecs., Vol 17, 1974, pp. 551-561.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	13	of	24	**Attorney Docket No:** 3771-0003-DC12

		Grove, et al., Investigation of Thermally Oxidised Silicon Surfaces Using Metal-Oxide- Semiconductor Structures, Solid-State Elecs., Vol. 8, 1965, pp. 145-163.	
		Guo, et al., High Quality Ultra- thin (1.5 nm) TiO2/Si3N4 Gate Dielectric for Deep Sub-micron CMOS Technology, IEEE, 1999, pp. 137-140.	
		Guo, et al., High Temperature Lifetesting of Silicon Metal-Thin Insulator-Semiconductor Heterojunction Emitter Bipolar Transistors, Solid-State Elecs., Vol. 31, No. 6, 1998, pp. 1071-1075.	
		Hara, Characterization of the 6H-SiC(0001) surface and the interface with Ti layer with the Schottky limit, Applied Surface Sci., Vol. 162-163, 2000, pp. 19-24.	
		Hara, et al., New Technique for Ohmic Formation, Materials Research Soc., Vol. 427, 1996, pp. 159-164.	
		Hartstein, et al., Determination of the inversion-layer thickness from capacitance measurements of metal-oxide- semiconductor field-effect transistors with ultrathin oxide layers, Physical Review B, Vol. 38, No. 2, Jul. 15, 1988, pp. 1235-1240.	
		Hasegawa, et al., Control of compound semiconductor- insulator interfaces by an ultrathin molecular- beam epitaxy Si layer, Journal of Vacuum Sci. & Tech., Vo. 7, No. 4, 1989, pp. 870-878.	
		Hasegawa, et al., Control of Structure and Properties of Compound Semiconductor Interfaces by Si Interface Control Layer, 1993 (5th) Int'l Conf. on Indium Phosphide & Related Materials, 1993, pp. 289-292.	
		Hasegawa, et al., Correlation Between Atomic-Scale Structures and Macroscopic Electrical Properties of Metal-Covered Si(111) Surfaces, Int'l Journal of Modern Physics B, Vol. 7, No. 22, 1993, pp. 3817-3876.	
		Hasegawa, Fermi Level Pinning and Schottky Barrier Height Control at Metal-Semiconductor Interfaces of InP and Related Materials, Japanese Journal of Applied Physics, Vol. 38, 1999, p. 1098-1102.	
		Ho, et al., Low-resistance ohmic contacts of p-type GaN achieved by the oxidation of Ni/Au films, Journal of Applied Physics, Vol. 86, No. 8, Oct. 1999, pp. 4491-4497.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	14	of	24

Complete if Known

Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.
Attorney Docket No:	3771-0003-DC12

		Hofmann, et al., In situ fabrication of vertical tunnel junctions for SET devices, Microelec Eng'g, Vols. 57-58, 2001, pp. 851-856.	
		Horiguchi, et al., Evaluation of interface potential barrier heights between ultrathin silicon oxides and silicon, Journal of Applied Physics, Vol. 58, No. 4, 1985, pp. 1597.	
		Horváth, et al., The effect of the metal-semiconductor interface on the barrier height in GaAs Schottky junctions, Vacuum, Vol. 41, No. 4, 1990, pp. 804-806.	
		Hudait, et al., Interface states density distribution in Au/n- GaAs Schottky diodes on n-Ge and n-GaAs substrates, Materials Sci. & Eng'g, Vol. B87, 2001, pp. 141-147.	
		Hui, et al., Specific Contact Resistivity of TiSi2 to p+ and n+ Junctions, IEEE Electron Device Letters, Vol. EDL-6, No. 9, Sep. 1985, pp. 479-481.	
		Ilderem, et al., Investigation of the Effects of Very Low Pressure Chemical Vapor Deposited TiSi2 on Device Electrical Characteristics, Journal Electrochem. Soc., Vol. 136, No. 10, Oct. 1989, pp. 2989-2993.	
		Ingerly, et al., Low resistance ohmic contacts to n-GaN and n-AlGaN, Applied Physics Letters, Vol. 77, No. 3, Jul. 17, 2000, pp. 382-384.	
		Itoh, et al., Analysis of Schottky Barrier Heights of Metal/SiC Contacts and Its Possible Application to High-Voltage Rectifying Devices, Physica Status Solidi, Vol. 162, 1997, pp. 389-408.	
		ITRS, Process Integration, Devices, and Structures and Emerging Research Devices, 2001 Ed., 51 pgs.	
		Ivančo, et al., Electrical Characterization of Au/SiOx/n-GaAs Junctions, Solid-State Elecs., Vol. 42, No. 2, 119, pp. 229-233.	
		Ivančo, et al., Schottky barrier height dependence on the silicon interlayer thickness of Au/Si/n- GaAs contacts: chemistry of interface formation study, Vacuum, No. 50, Issues 3-4, Jul. 1998, pp. 407-411.	
		Ivančo, et al., Unpinning of the Au/GaAs interfacial Fermi level by means of ultrathin undoped silicon interlayer inclusion, Journal of Applied Physics, Vol. 87, No. 2, Jan. 15, 2000, pp. 795-800.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	15	of	24	**Attorney Docket No:** 3771-0003-DC12

		Ivey, Platinum Metals in Ohmic Contacts to III- V Semiconductors, Platinum Metals Research, Vol. 43, No. 1, 1999, pp. 2-12.	
		Jacobs, et al., Optimisation of the Ti/Al/Ni/Au ohmic contact on AlGaN/GaN FET structures, Journal of Crystal Growth, Vol. 241, 2002, pp. 15-18.	
		Kar, et al., Interface States in MOS Structures with 20-40 Å Thick SiO2 Films on Nondegenerate Si*, Solid-State Elecs., Vol. 15, 1972, pp. 221-237.	
		Kasai, Control of Metal/III-V Compound Semiconductor Interfaces and Its Application to Quantum Effect Devices, Thesis, Hokkaido Univ., Dec. 1996, 309 pgs.	
		Kedzierski, Complementary silicide thin-body silicon-on-insulator CMOS devices, Thesis, U.C. Berkeley, 2001, 134 pgs.	
		Kim, et al., Low-Resistance Ti/Ai Ohmic Contact on Undoped ZnO, Journal of Elec Materials, Vol. 31, No. 8, 2002, pp. 868-871.	
		Kipperman, et al., Improved efficiency of MIS-silicon solar cells by HF treatment of the oxide layer, Applied Physics Letters, Vol. 28, No. 620, 1976, pp. 620-621.	
		Kobayashi, et al., Studies of interface states at ultrathin SiO2/Si(100) interfaces by means of x-ray photoelectron spectroscopy under biases and their passivation by cyanide treatment, Journal of Applied Physics, Vol. 83, No. 4, Feb. 15, 1998, pp. 2098-2103.	
		Kolodzey, et al., Electrical Conduction and Dielectric Breakdown in Aluminum Oxide Insulators on Silicon, IEEE Trans. on Electron Devices, Vol. 47, No. 1, Jan. 2000, pp. 121-128.	
		LaBrasca, et al., Scanning tunneling microscopy and spectroscopy on pn junctions formed by ion implantation, Journal of Vacuum Sci. & Tech., Vol 9, Mar./Apr. 1991, pp. 752-757.	
		Lee, et al., Effects of interfacial layer growth on the electrical characteristics of thin titanium oxide films on silicon, Journal of Applied Physics, Vol. 74, No. 21, May 24, 1999, pp. 3143-3145.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	16	of	24	**Attorney Docket No:** 3771-0003-DC12

		Lee, et al., Ohmic contact formation mechanism of nonalloyed contacts to p-type GaN observed by positron annihilation spectroscopy, Applied Physics Letters, Vol. 74, No. 16, Apr. 19, 1999, pp. 2289-2291.	
		Lee, Processing and Characterization of Silicon Carbide (6H- and 4H-SiC) Contacts for High Power and High Temperature Device Applications, Ph.D. Dissertation, KTH, Royal Institute of Technology, 2002, 106 pgs.	
		Leprince- Wang, et al., Study of the growth morphology of TiO2 thin films by AFM and TEM, Surface and Coatings Tech., Vol. 140, 2001, pp. 155-160.	
		Levy, et al., Selective LPCVD Tungsten for Contact Barrier Applications, Journal Electrochem. Soc., Vol. 133, No. 9, Sep. 1986, pp. 1905-1912.	
		Liauh, et al., Electrical and microstructural characteristics of Ti contacts on (001)Si, Journal of Applied Physics, Vol. 74, No. 4, Aug. 15, 1993, pp. 2590-2597.	
		Lillington, et al., Effects of interfacial oxide layers on the performance of silicon Schottky-barrier solar cells, Applied Physics Letters, Vol. 28, No. 2, Jan. 15, 1976, pp. 97-98.	
		Lin, et al., A novel Pd/oxide/GaAs metal- insulator- semiconductor field- effect transistor (MISFET) hydrogen sensor, Semiconductor Sci. Tech., Vol. 16, 2002, pp. 997-1001.	
		Lin, et al., Low resistance ohmic contacts on wide band-gap GaN, Applied Physics Letters, Vol. 64, No. 8, Feb. 1994, pp. 1003-1005.	
		Look, et al., Unpinning of GaAs Surface Fermi Level by 200 Degrees C Molecular Beam Epitaxial Layer, Applied Physics Letters, Vol. 57, No. 24, Dec. 10, 1990, pp. 2570-2572.	
		Lucovsky, Reaction/annealing pathways for forming ultrathin silicon nitride films for composite oxide-nitride gate dielectrics with nitrided crystalline silicon-dielectric interfaces for application in advanced complementary metal- oxide-semiconductor devices, Journal of Vacuum Sci. & Tech A, Vol. 17, No. 4, Jul./Aug. 1999, pp. 1340-1351.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	17	of	24	**Attorney Docket No:** 3771-0003-DC12

		Lue, et al., A method to characterize the dielectric and interfacial properties of metal-insulator- semiconductor structures by microwave measurement, Journal of Applied Physics, Vol. 91, No. 8, Apr. 15, 2002, pp. 5275-5282.	
		Luther, et al., Analysis of a thin AlN interfacial layer in Ti/Al and Pd/Al ohmic contacts to n- type GaN, Applied Physics Letters, Vol. 71, No. 26, Dec. 29, 1997, pp. 3859-3861.	
		Maeda, et al., A Highly Reliable Interconnection for a BF2-Implanted Junction Utilizing TiN/Ti Barrier Metal System, IEEE Trans. of Electron Devices, Vol. ED-34, No. 3, Mar. 1987, pp. 599-606.	
		Mahalingam, Trench MOS Based Power Devices with Graded Doped Profile, Thesis, No. Carolina Univ., 1999, 295 pgs.	
		Mamor, et al., Schottky Barrier Heights on IV-IV Compound Semiconductors, Journal of Elec Materials, Vol. 25, No. 11, Nov. 1996, pp. 1748-1753.	
		Marinova, et al., Nickel based ohmic contacts on SiC, Materials Sci. & Eng'g, Vol. B46, 1997, pp. 223-226.	
		Matsuzawa, et al., A Unified Simulation of Schottky and Ohmic Contacts, IEEE Trans. on Electron Devices, Vol. 47, No. 1, Jan. 2000, pp. 103-108.	
		Miller, et al., Ohmic Contacts to n- Type GaN, Journal of Elec Materials, Vol. 25, No. 11, 1996, pp. 1709-1714.	
		Mönch, Electron properties of ideal and interface- modified metal-semiconductor interfaces, Journal of Vacuum Sci. & Tech. B, Vol. 14, No. 4, Jul./Aug. 1998, pp. 2985-2993.	
		Morita, et al., Growth of native oxide on a silicon surface, Journal of Applied Physics, Vol. 68, No. 3, Aug. 1990, pp. 1272-1281.	
		Muret, et al., Unpinning of the Fermi level at erbium silicide/silicon interfaces, Physical Review B, Vol. 56, No. 15, Oct. 15, 1997, pp. 9286-9289.	
		Nakasaki, et al., Tungsten/titanium nitride low-resistance interconnections durable for high-temperature processing, Journal of Applied Physics, Vol. 64, No. 8, Sep. 15, 1988, pp. 3263-3268.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	18	of	24	**Attorney Docket No:** 3771-0003-DC12

		Nielsen, Current mechanism of tunnel m.i.s. solar cells, IEE Proceedings, Vol. 127, Part 1, No. 6, Dec. 1980, pp. 301-307.	
		Nielsen, Current Mechanism of Tunnel MIS Solar Cells, IEE Proceedings, Vol. 129, Part 1, No. 4, Aug. 1982, pp. 153-156.	
		O'Donnell, et al., Temperature dependence of semiconductor band gaps, Applied Physics Letters, Vol. 58, No. 25, Jun. 24, 1991, pp. 2924-2926.	
		Okada, et al., Electrical Characteristics and Reliability of Pt/Ti/Pt/Au Ohmic Contacts to p-Type GaAs, Japanese Journal of Applied Physics, Vol. 30, No. 4A, Apr. 1991, pp. L558-L560.	
		O'Meara, et al., Experimental Design Study of Coincident Titanium Nitride/Titanium Silicide Formation from Rapid Thermal Processing, Materials Research Soc. Symposium Proceedings, Vo. 260, 1992, pp. 805-811.	
		Oskam, et al., Electrochemical deposition of metals onto silicon, Journal of Applied Physics, Vol. 31, 1998, pp. 1927-1949.	
		Park, et al., Impact of atomic- layer-deposited TiN on the gate oxide quality of W/TiN/SiO2/Si metal- oxide-semiconductor structures, Applied Physics Letters, Vol. 80, No. 14, Apr. 8, 2002, pp. 2514-2516.	
		Park, et al., Improved Low Resistance Contacts of Ni/Au and Pd/Au to p- Type GaN Using a Cryogenic Treatment,Cambridge Univ. Press, Jun. 13, 2014, 6 pgs.	
		Park, et al., Metal-insulator- semiconductor structure on GaAs using a pseudomorphic Si/GaP interlayer, Journal of Vacuum & Sci. Tech., Vol. 15, Mar./Apr. 1997, pp. 252-258.	
		Park, et al., Si3N4/Si/In0.05Ga0.95As/n-GaAs metal- insulator- semiconductor devices, Journal of Applied Physics, Vol. 81, No. 1, Jan. 1, 1997, pp. 516-523.	
		Park, et al., Thermal stability of molybdenum-silicon nitride-silicon Schottky diodes, Journal of Applied Physics, Vol. 69, No. 5, Mar. 1, 1991, pp. 3149-3153.	
		Patkar, et al., Very low resistance nonalloyed ohmic contacts using low-temperature molecular beam epitaxy of GaAs, Am. Institute of Physics, Vol. 66, No. 11, Mar. 13, 1996, pp. 1412-1414.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	19	of	24	**Attorney Docket No:** 3771-0003-DC12

		Plummer, et al., Material and Process Limits in Silicon VLSI Technology, IEEE, Vol. 89, No. 3, Mar. 2000, pp. 240-258.	
		Polishchuk, et al., Dual Work Function Metal Gate CMOS Technology Using Metal Interdiffusion, IEEE Electron Device Letters, Vol. 22, No. 9, Sep. 2001, pp. 444-446.	
		Porter, et al., Effect of Interfacial Oxide Layers on the Current-Voltage Characteristics of Al- Si Contacts, NASA Contracte #NAS8-26379, Nov. 1976, 67 pgs.	
		Proctor, et al., Direct Measurements of Interfacial Contact Resistance, End Contact Resistance, and Interfacial Contact Layer Uniformity, IEEE Trans. of Electron Devices, Vol. ED-30, No. 11, Nov. 1983, pp. 1535-1542.	
		Ren, Nanoscale MOSFETS: Physics, Simulation and Design, Thesis, Purdue Univ., Oct. 2001, 211 pgs.	
		Rhoderick, Metal-semiconductor contacts, IEEE Proceedings, Vol. 129, Part 1, No. 1, Feb. 1982, pp. 1-14.	
		Rhoderick, The physics of Schottky barriers, Review of Physics in Tech., 1970, pp. 81-95.	
		Richards, Novel Uses of Titanium Dioxide of Solar Cells, Thesis, Univ. of New South Wales, Apr. 2002, 259 pgs.	
		Rohdin, et al., Interfacial Gate Resistance in Schottky-Barrier-Gate Field-Effect Transistors, Hewlett-Packard Company, 1998, pp. 1-25.	
		Sambell, et al., Unpinning the GaAs Fermi Level with Thin Heavily Doped Silicon Overlayers, IEEE Trans. of Electron Devices, Vol. 37, No. 1, Jan. 1990, pp. 88-95.	
		Schenk, Halbleiterbauelemente - Physikalische Grundlagen und Simulation, Integrated Sys Lab, Dec. 18, 2001, 177 pgs.	
		Schenk, Semiconductor components Physical basics and simulation, Integrated Sys Lab, Dec. 18, 2001, 5 pgs.	
		Semi. Indus. Assocation, The International Technology Roadmap for Semiconductors 2001 Edition – Interconnect, 2001, pp. 1-25.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	20	of	24

Complete if Known

Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.
Attorney Docket No:	3771-0003-DC12

		Sharma, Influence of thin inversion layers on Schottky diodes, Revue de Physique Applicquee, Vol. 21, Jan. 1986, pp. 25-33.	
		Shewchun, Metal-Insulator- Semiconductor (MIS) and Semiconductor- Insulator-Semiconductor (SIS) Solar Cells: 1. Basic Principles, 1979, pp. 843-867.	
		Shewchun, et al., MIS and SIS Solar Cells, IEEE Trans. On Electron Devices, Vol. ED-27, Vol. 4, Apr. 1980, pp. 705-716.	
		Shewchun, et al., Theory of metal-insulator-semiconductor solar cells, Journal of Applied Physics, Vol. 48, Nov. 2, Feb. 1977, pp 765-770.	
		Shih, et al., Effects of interfacial microstructure on uniformity and thermal stability of AuNiGe ohmic contact to n-type GaAs, Journal of Applied Physics, Vol. 62, No. 2, Jul. 15, 1987, pp.582-590.	
		Singh, Theory of Metal- Insulator- Semiconductor (MIS) and Semiconductor-Insulator- Semiconductor (SIS) Solar Cells, Thesis, McMaster University, Apr. 1979, 365 pgs.	
		Smith, et al., Chemical Vapour Deposition of the Oxides of Titanium, Zironium and Hafnium for Use as High-k Materials in Microelectronic Devices. A Carbon-free Precursor for the Synthesis of Hafnium Dioxide, Adv. Materials for Optics and Elecs, Vol. 10, 2000, pp. 105-114.	
		Sobolewski, et al., Analysis of Thin Thermal Silicon Nitride Films on Silicon, Applied Surface Sci., Vol. 30, 1987, pp. 210-215.	
		Sobolewski, et al., Studies of barrier height mechanisms in metal-silicon nitride-silicon Schottky barrier diodes, Journal of Sci. Tech., Vol. 7, No. 4, Jul./Aug. 1989, pp. 971-979.	
		Song, et al., Effects of sulfur passivation on Ti/Al ohmic contacts to n- type GaN using CH3CSNH2 solution, Applied Physics Letters, Vol. 80, No. 17, Apr. 29, 2002, pp. 3129-3131.	
		Spicer, et al., Study of the Electronic Surface States of III-V Compounds and Silicon, DARPA Order No. 3564, Program Code No. HX 1241, Oct. 1, 1981, 158 pgs.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	21	of	24	**Attorney Docket No:** 3771-0003-DC12

		Spicer, et al., Unified Mechanism for Schottky-Barrier Formation and III-V Oxide Interface States, Physical Review Letters, Vol. 44, No. 6, Feb. 11, 1980, pp. 420-423.	
		Srivastava, et al., Theory of Metal- Oxide-Semiconductor Solar Cells, Solid-State Elecs., Vol.22, 1987, pp. 581-587.	
		Streetman, Solid State Electronic Devices, Fourth Ed., Prentice-Hall, Inc., 1995, 91 pgs.	
		Suguro, et al., Reaction Kinetics in Tungsten/Barrier Metal Silicon Systems, Thin Solid Films, Vol. 166, 1988, pp. 1-14.	
		Taboryski, et al., Superconductor- Semiconductor- Superconductor Planar Junctions of Aluminum on δ-doped Gallium-Arsenide, IEEE Trans. on Applied Superconductivity, Vol. 7, No. 2, Jun. 2, 1997, pp. 2809-2813.	
		Taubeblatt, et al., Interface effects in titanium and hafnium Schottky barriers on silicon, Applied Physics Letters, Vol. 44, No. 9, May 1, 1984, pp. 895-897.	
		Taubenlatt, et al., Silicide and Schottky barrier formation in the Ti-Si and the Ti-SiOx-Si systems, Journal of Applied Physics, Vol. 53, No. 9, Sep. 1982, pp. 6308-6315.	
		Teraji, et al., Ideal Ohmic contact to n-type 6H-SiC by reduction of Schottky barrier height, Applied Physics Letters, Vol. 71, No. 5, Aug. 1997, pp. 689-691.	
		Thanailakis, Contacts between simple metals and atomically clean silicon, Journal of Physics C: Solid State Physics, Vol. 8, 1975, pp. 655-668.	
		Thanailakis, et al., Transition-metal contacts to atomically clean silicon, Journal of Physics C: Solid State Physics, Vol. 9, 1976, pp. 337-343.	
		Tiwari, et al., Unpinned GaAs MOS Capacitors and Transistors, IEEE Electron Device Letters, Vol. 9, No. 9, Sep. 1988, pp. 488-490.	
		Topham, Ohmic Contacts to N- Type Indium Phosphide, Thesis, Univ. of Surrey, Sep. 1983, 176 pgs.	
		Tsutsumi, et al., A Selective LPCVD Tungsten Process Using Silane Reduction for VLSI Applications, IEEE Trans. on Electron Devices, Vol. 37, No. 3, Mar. 1990, pp. 569-576.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	22	of	24	**Attorney Docket No:** 3771-0003-DC12

		Tucker, Dynamic Capacitance of Metal-Oxide- Semiconductor Field- Effect Transistors, Thesis, Univ. of Missouri, 1968, 82 pgs.	
		Tung, Schottky-Barrier Formation of Single- Crystal Metal- Semiconductor Interfaces, Physical Review Letters, Vol. 52, No. 6, Feb. 6, 1984, pp. 461-464.	
		Turner, et al., Metal-Silicon Schottky Barriers, Solid-State Elecs., Vol. 11, 1968, pp. 291-300.	
		Van Otterloo, Schottky Barriers on Clean-Cleaved Silicon, Surface Science, Vol. 104, 1981, pp. L205-L209.	
		Vilinaus Univ., The Metal- Semiconductor Junction. Schottky Diode Ohmic Contacts, Vilinaus Univ., Semiconductor Physics Dept., Lithuania, downloaded 1/25/20, 18 pgs.	
		Waldrop, et al., Formation and Schottky barrier height of metal contacts to β-SiC, Applied Physics Letters, Vol. 56, No. 6, Feb. 5, 1990, pp. 557-559.	
		Waldrop, et al., Metal Schottky barrier contacts to alpha 6H- SiC, Journal of Applied Physics, Vol. 72, No. 10, Nov. 15, 1992, pp. 4757-4760.	
		Waldrop, et al., Wide range of Schottky barrier height for metal contacts to GaAs controlled by Si interface layers, Journal of Vacuum Sci. & Tech. B, Vol. 4, No. 4, Jul./Aug. 1988, pp. 1432-1435.	
		Walukiewicz, Mechanism of Schottky Barrier Formation: The Role of Amphoteric Native Defects, Lawrence Berkeley Nat'l Lab., Feb. 1, 1987, 23 pgs.	
		Werner, et al., Barrier inhomogeneities at Schottky contacts, Journal of Applied Physics, Vol. 69, No. 3, Feb. 1, 1991, pp. 1522-1533.	
		Weste, et al., Principles of CMOS Technology: A Systems Perspective, Second Ed., Addison Wesley Longman, 1993, 749 pgs.	
		Williams, Interfaces in Semiconductor Structures and Devices, Physik Bl., Vol. 45, Nr. 7, 1989, pp. 219-222.	
		Williams, Metal-Semiconductor Interfaces, The Physics of Submicron Semiconductor Devices, 1988, pp. 683-701.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	23	of	24	**Attorney Docket No:** 3771-0003-DC12

		Wilson, et al., Differential Capacitance-Voltage Profiling of Schottky Barrier Diodes for Measuring Implanted Depth Distributions in Silicon, U.S. Dept. of Commerce, Nat'l Bureau of Standards, Feb. 1982, 68 pgs.	
		Wittmer, et al., Ideal Schottky Diodes on Passivated Silicon, Physical Review Letters, Vol. 69, No. 18, Nov. 2, 1993, pp. 2701-2704.	
		Wu, Barrier height reduction of the Schottky barrier diode using a thin highly doped surface layer, Journal of Applied Physics, Vol. 51, No. 9, Sep. 1980, pp. 4919-4922.	
		Wu, et al., Interface capacitance in metal- semiconductor junctions, Journal of Applied Physics, Vol. 65, No. 9, May 1, 1989, pp. 3560-3567.	
		Yang, et al, Tunneling in a Metal- Semiconductor- Semiconductor Thin- Film Diode, Solid-State Elec., Vol. 29, No. 3, 1986, pp. 355-357.	
		Yen, et al., Thermally Assisted Multiphoton Photoelectric Emission from Tungsten, Optics Communications, Vol. 35, No. 2, Nov. 1980, pp. 277-282.	
		Zafar, A method for measuring barrier heights, metal work functions and fixed charge densities in metal/SiO2/Si capacitors, Applied Physics Letters, Vol. 80, No. 25, Jun. 24, 2002, pp. 4858-4860.	
		Zaima, et al., Electrical Properties and Crystallographic Structures of Transition Metal/Silicon Interface, Materia Japan, Vol. 33, No. 6, 1994, pp. 691-696.	
		Zaima, et al., Formation of silichide at metal/silicon interface and low-resistivity contacts, Applied Physics, Vol. 63, No. 11, 1994, pp. 1093-1105.	
		Zaima, et al., Study on determining factors of low contact resistivity in transition metal-silicon systems, Applied Surface Science, Vols. 70/71, 1993, pp. 624-628.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

	Complete if Known
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	**24**	**of**	**24**	**Attorney Docket No:** 3771-0003-DC12

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2020-06-17
Name/Print	Tarek N. Fahmi	Registration Number	41,402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENDFEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16506022
Filing Date	2019-07-09
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.
Attorney Docket Number	3771-0003-DC12

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4304042	A	1981-12-08	Yeh	
	2	4691219	A	1987-09-01	Goth	
	3	5614745	A	1997-03-25	Motonami	
	4	6323508	B1	2001-11-27	Takahashi, et al.	
	5	6521502	B1	2003-02-18	Yu	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20060178015	A1	2006-08-10	Verhaverbeke	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16506022
	Filing Date	2019-07-09
	First Named Inventor	Daniel E. Grupp
	Art Unit	2815
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC12

	2	20140117465	A1	2014-05-01	Huang, et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	ARCHIBONG, et al., On the Structure of A12O3 and Photoelectron Spectra of A12O2 and A12O3; J. Phys. Chem.A 1999, 103, pp. 1109-1114.	
	2	BORTZ, et al., Temperature Dependence of the Electronic Structure of Oxides: MgO, MgAl2O4 and Al2O3; Physica Scripta., Col. 41, pp. 537-541, 1990.	
	3	CARVER, et al., Specific Contact Resistivity of Metal-Semiconductor Contacts - A New, Accurate Method Linked to Spreading Resistance; IEEE Transactions on Electron Devices, Vol. 35, No. 4, April 1988, pp. 489-497	
	4	LIDE, David R., CRC Handbook of Chemistry and Physics, Internet Version 2005; <http://www.hbcpnetbase.com>, CRC Press, Boca Raton, FL, 2005; 11 pp,	
	5	DISTEFANO, et al., The Band Edge of Amorphous SiO2 By Photoinjection and Photoconductivity Measurements; Solid State Communications, Vol. 9, pp. 2259-2261, 1971, Pergamon Press; Printed in Great Britain	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16506022
	Filing Date	2019-07-09
	First Named Inventor	Daniel E. Grupp
	Art Unit	2815
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC12

	6	Fitting, et al., Monte-Carlo Approach of Electron Emission from SiO2; Phys. Stat. Sol. (a) 81, 323 (1984) pp. 323-332	
	7	IPR2020-01182; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; June 23, 2020; 139 pp.	
	8	IPR2020-01182; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 7,084,423; June 24, 2020; 76 pp.	
	9	IPR2020-01183; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; June 24, 2020; 178 pp.	
	10	IPR2020-01183; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 9,209,261; June 24, 2020; 81 pp.	
	11	IPR2020-01204; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; June 29, 2020; 178 pp.	
	12	IPR2020-01204; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 8,766,336; June 29, 2020; 78 pp.	
	13	IPR2020-01205; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; June 29, 2020; 142 pp.	
	14	IPR2020-01205; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 9,461,167; June 29, 2020; 63 pp.	
	15	IPR2020-01206; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; June 29, 2020; 164 pp.	
	16	IPR2020-01206; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 9,905,691; June 29, 2020; 76 pp.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16506022
	Filing Date	2019-07-09
	First Named Inventor	Daniel E. Grupp
	Art Unit	2815
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC12

	17	IPR2020-01207; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; June 29, 2020; 146 pp.	
	18	IPR2020-01207; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 10,090,395; June 29, 2020; 66 pp.	
	19	IPR2020-01241; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; July 6, 2020; 165 pp.	
	20	IPR2020-01241; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 9,461,167; July 6, 2020; 84 pp.	
	21	IPR2020-01264; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; July 8, 2020; 194 pp.	
	22	IPR2020-01264; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 8,766,336; July 8, 2020; 83 pp.	
	23	IPR2020-01279; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; July 9, 2020; 182 pp.	
	24	IPR2020-01279; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 9,905,691; July 10, 2020; 84 pp.	
	25	IPR2020-01282; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; July 12, 2020; 217 pp.	
	26	IPR2020-01282; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 10,090,395; July 13, 2020; 85 pp.	
	27	LANG et al., Theory of Metal Surfaces: Work Functon *; Physical Review B, Volume 3, Number 4; February 15, 1971; pp. 1215-1223.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16506022
	Filing Date	2019-07-09
	First Named Inventor	Daniel E. Grupp
	Art Unit	2815
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC12

	28	ROHATGI et al., Comprehensive Study of Rapid, Low-Cost Silicon Surface Passivation Technologies; IEEE Transactions on Electron Devices, Vol 47, No. 5, May 2000; pp. 987-993.
	29	SAKURAI, et al., Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas; IEEE Journal of Solid-State Circuits, Vo. 25, No. 2, April 1990, pp. 584-594.
	30	SIMMONS, John G., Generalized Formula for the Electric Tunnel Effect Between Similar Electrodes Separated by a Thin Insulating Film; Journal of Applied Physics, Volume 34, Number 6, June 1963; pp. 1793-1803.
	31	STESMANS et al., Si Dangling-Bond-Type Defects at the Interface of (100)Si with Ultrathin Layers of SiOx, Al2O3, and ZrO2; Applied Physics Letters, Volume 80, Number 11, March 18, 2002; pp. 1957-1959.
	32	SZYDLO, et al., I-V and C-V Characteristics of Au/TiO2 Schottky Diodes; J. Appl. Phys. 51(6), June 1980; pp. 3310-3312.
	33	ZHENG et al., Electronic Structure Differences in ZeO2 vs HfO2; J. Phys. Chem. A 2005, 109, pp.11521-11525.

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/MONICA D HARRISON/	Date Considered	09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16506022
Filing Date	2019-07-09
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.
Attorney Docket Number	3771-0003-DC12

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2020-07-15
Name/Print	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16506022
Filing Date	2019-07-09
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	HARRISON, MONICA D
Attorney Docket Number	3771-0003-DC12

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20040129087	A1	2004-07-08	ROWE; et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16506022
Filing Date	2019-07-09
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	HARRISON, MONICA D
Attorney Docket Number	3771-0003-DC12

	1	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/MONICA D HARRISON/	Date Considered	09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16506022
Filing Date	2019-07-09
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	HARRISON, MONICA D
Attorney Docket Number	3771-0003-DC12

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2020-08-27
Name/Print	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	9

Complete if Known

Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.
Attorney Docket No:	3771-0003-DC12

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		4845050	1989-07-04	Kim, et al.	
		6724088	2004-04-20	Jammy, et al.	
		7176483	2007-02-13	Grupp, et al.	
		9461167	2016-10-04	Grupp, et al.	
		9905691	2018-02-27	Grupp, et al.	
		10090395	2018-10-02	Grupp, et al.	
		20050093027	2005-05-05	Grupp; et al.	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T2
		DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 79 pgs.	
		APPENDIX A1., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 5 pgs.	
		APPENDIX A2., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 7 pgs.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	2	of	9	**Attorney Docket No:** 3771-0003-DC12

		APPENDIX A3., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 19 pgs.	
		APPENDIX A4., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 21 pgs.	
		APPENDIX A6., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 15 pgs.	
		APPENDIX A7., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 26 pgs.	
		APPENDIX A8., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 28 pgs.	
		APPENDIX A10., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 18 pgs.	
		APPENDIX B1., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 41 pgs.	
		APPENDIX B2., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 43 pgs.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	3	of	9	**Attorney Docket No:** 3771-0003-DC12

		APPENDIX B3., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 48 pgs.	
		APPENDIX B4., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 48 pgs.	
		APPENDIX B5., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 47 pgs.	
		APPENDIX B6., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 32 pgs.	
		APPENDIX B7., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 42 pgs.	
		APPENDIX B8., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 41 pgs.	
		APPENDIX B10., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 30 pgs.	
		APPENDIX C1., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 5 pgs.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	4	of	9	**Attorney Docket No:** 3771-0003-DC12

		APPENDIX C2., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 5 pgs.	
		APPENDIX C3., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 7 pgs.	
		APPENDIX C4., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 9 pgs.	
		APPENDIX C5., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 9 pgs.	
		APPENDIX C6., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 8 pgs.	
		APPENDIX C7., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 9 pgs.	
		APPENDIX C8., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 9 pgs.	
		APPENDIX C10., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 4 pgs.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	5	of	9	**Attorney Docket No:** 3771-0003-DC12

		APPENDIX D1., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 16 pgs.	
		APPENDIX D2., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 20 pgs.	
		APPENDIX D3., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 14 pgs.	
		APPENDIX D4., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 11 pgs.	
		APPENDIX D5., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 16 pgs.	
		APPENDIX D6., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 12 pgs.	
		APPENDIX D7., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 22 pgs.	
		APPENDIX D8., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 15 pgs.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	6	of	9	**Attorney Docket No:** 3771-0003-DC12

		APPENDIX D10., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 21 pgs.	
		APPENDIX E1., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 8 pgs.	
		APPENDIX E2., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 8 pgs.	
		APPENDIX E3., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 8 pgs.	
		APPENDIX E4., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 8 pgs.	
		APPENDIX E5., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 8 pgs.	
		APPENDIX E6., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 8 pgs.	
		APPENDIX E7., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 8 pgs.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	7	of	9	**Attorney Docket No:** 3771-0003-DC12

		APPENDIX E8., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 8 pgs.	
		APPENDIX E10., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 8 pgs.	
		APPENDIX F1., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 13 pgs.	
		APPENDIX F2., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 15 pgs.	
		APPENDIX F3., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 11 pgs.	
		APPENDIX F4., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 15 pgs.	
		APPENDIX F5., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 9 pgs.	
		APPENDIX F6., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 9 pgs.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED**

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.

Sheet	8	of	9	**Attorney Docket No:** 3771-0003-DC12

		APPENDIX F7., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 17 pgs.	
		APPENDIX F8., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 17 pgs.	
		APPENDIX F10., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 11 pgs.	
		De Bosscher, et al., The influence of silicide formation on the barrier height of Ti/Si MIS Schottky barriers, Semiconductor Sci., Tech., Vol. 1, 1986, pp. 376-382.	
		Defives, et al., Electrical behaviour and microstructural analysis of metal Schottky contacts on 4H-SiC, Microelec. Eng'g, Vol. 55, 2001, pp. 369-374.	
		Goodnick, et al., Effects of a thin SiO2 layer on the formation of metal-silicon contacts, Journal of Vacuum Sci. & Tech., Vol. 18, No. 3, Apr. 1981, pp. 949-954.	
		Schmidt, et al., Increased dependence of Schottky barrier height on metal work functions due to a thin-oxide layer, Journal of Vacuum Sci. & Tech., Vol. 6, No. 4, Jul./Aug. 1988, pp. 1436-1439.	
		Waldrop, et al., Schottky barrier height and interface chemistry of annealed metal contacts to alpha 6H-SiC: Crystal face dependence, Applied Physics Letters, Vol. 62, No. 21, May 24, 1993, pp. 2685-2687.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	9	of	9

Complete if Known

Application Number	16/506,022
Filing Date	07-09-2019
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.
Attorney Docket No:	3771-0003-DC12

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2020-06-17
Name/Print	Tarek N. Fahmi	Registration Number	41,402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENDFEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

Doc Code: DIST.E.FILE Document Description: Electronic Terminal Disclaimer - Filed	PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	16506022
Filing Date	09-Jul-2019
First Named Inventor	Daniel Grupp
Attorney Docket Number	3771-0003-DC12
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
Acorn Semi, LLC	100%

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

9425277

9905691

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

◉ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

○ I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicant claims the following fee status:

◉ Small Entity

○ Micro Entity

○ Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

◉ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

Registration Number 41402

○ A sole inventor

○ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application

○ A joint inventor; all of whom are signing this request

Signature	/Tarek N. Fahmi/
Name	Tarek N. Fahmi

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	16506022
Filing Date:	09-Jul-2019
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Filer:	Tarek N. Fahmi/Sarah Zizzo
Attorney Docket Number:	3771-0003-DC12

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	2814	1	170	170
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**170**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 16506022

Filing Date: 09-Jul-2019

Applicant/Patent under Reexamination: Grupp

Electronic Terminal Disclaimer filed on December 21, 2020

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	41448179
Application Number:	16506022
International Application Number:	
Confirmation Number:	3561
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC12
Receipt Date:	21-DEC-2020
Filing Date:	09-JUL-2019
Time Stamp:	14:11:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$170
RAM confirmation Number	E2020BKE11399105
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	33526 2805a0e0fc111194d10e766bcbb9617ebe041f81	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30541 8fdc16b7b9fbb8c6357ddb514f2c30a58a483373	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	64067		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 16/506,022

First Named Inventor: Daniel E. Grupp

Filed: 07/09/2019

Art unit: 2815

Examiner: Harrison, Monica D.

Docket No.: 3771-0003-DC12

Confirmation No.: 3561

Commissioner for Patents
P.O. Box 1450
Alexandria VA, 22313-1450

RESPONSE TO OFFICE ACTION

Dear Commissioner:

Responsive to the office action dated September 21, 2020, reconsideration of this application is respectfully requested.

A Terminal Disclaimer with respect to US Pat. 9,905,691 and US Pat. 9,425,277 accompanies this response. In view of the terminal disclaimer, the obviousness-type double patenting rejections of the claims should be withdrawn.

If there are any additional fees due in connection with this communication, please charge Deposit Account No. 50-5798.

Respectfully submitted,
Ascenda Law Group, PC

Dated: December 21, 2020

/Tarek N. Fahmi/
Tarek N. Fahmi
Reg. No. 41,402

2150 N First St., Ste. 420
San Jose, CA 95131
(866) 877-4883

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16506022
Filing Date	2019-07-09
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.
Attorney Docket Number	3771-0003-DC12

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

GF Exhibit 1124 - 2636/2704

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16506022
	Filing Date	2019-07-09
	First Named Inventor	Daniel E. Grupp
	Art Unit	2815
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC12

	1	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Joint Claim Construction and Prehearing Statement, 10 pgs. (Jul. 23, 2020).	
	2	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Ex. A to Joint Claim Construction and Prehearing Statement, 9 pgs. (Jul. 23, 2020).	
	3	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Ex. B to Joint Claim Construction and Prehearing Statement, 8 pgs. (Jul. 23, 2020).	
	4	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Revised Joint Claim Construction and Prehearing Statement, 9 pgs. (Aug. 20, 2020).	
	5	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Ex. A to Revised Joint Claim Construction and Prehearing Statement, 7 pgs. (Aug. 20, 2020).	
	6	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Ex. B to Revised Joint Claim Construction and Prehearing Statement, 7 pgs. (Aug. 20, 2020).	
	7	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Plaintiff's Opening Claim Construction Brief, 39 pgs. (Aug. 21, 2020).	
	8	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Defendant's Responsive Claim Construction Brief, 33 pgs. (Sep. 4, 2020).	
	9	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Plaintiff's Reply Claim Construction Brief, 17 pgs. (Sep. 11, 2020).	
	10	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Joint Claim Construction Chart, 20 pgs. (Sep. 18, 2020).	
	11	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Joint Claim Construction Chart Appendices, 12 pgs. (Aug. 21, 2020).	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16506022
	Filing Date	2019-07-09
	First Named Inventor	Daniel E. Grupp
	Art Unit	2815
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC12

	12	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Construction Memorandum Opinion and Order, 40 pgs. (Oct. 16, 2020).	
	13	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Order Correcting Typographical Error in Claim Construction Memorandum Opinion and Order, 2 pgs. (Nov. 18, 2020).	
	14	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Order of Judge R. Gilstrap Adopting Claim Construction Memorandum Opinion and Order, 2 pgs. (Dec. 10, 2020).	
	15	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Expert Report of Dr. Jeffrey Bokor Regarding Invalidity of U.S. Patent No. 7,084,423, U.S. Patent No. 8,766,336, U.S. Patent No. 9,209,261, U.S. Patent No. 9,461,167, U.S. Patent No. 9,905,691, and U.S. Patent No. 10,090,395 (Redacted) (Nov. 16, 2020).	
	16	Exhibit A to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), CV of Dr. Jeffrey Boker, 36 pgs. (Nov. 16, 2020).	
	17	Exhibit B to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Materials Considered in Connection with Report, 4 pgs. (Nov. 16, 2020).	
	18	Exhibit C to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipation of '336 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Patent 7,176,483, 38 pgs. (Nov. 16, 2020).	
	19	Exhibit D to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipation of '261 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Patent 7,176,483, 7 pgs. (Nov. 16, 2020).	
	20	Exhibit E to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipation of '167 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Patent 7,176,483, 16 pgs. (Nov. 16, 2020).	
	21	Exhibit F to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipation of '691 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Patent 7,176,483, 8 pgs. (Nov. 16, 2020).	
	22	Exhibit G to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipated of '395 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Patent 7,176,483, 8 pgs. (Nov. 16, 2020).	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16506022
	Filing Date	2019-07-09
	First Named Inventor	Daniel E. Grupp
	Art Unit	2815
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC12

	23	Exhibit H to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), List of Claims by Grouping, 4 pgs. (Nov. 16, 2020).
	24	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Rebuttal Expert Report of Edwin Piner, Ph.D. (Redacted) (Dec. 14, 2020).

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16506022
Filing Date	2019-07-09
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.
Attorney Docket Number	3771-0003-DC12

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2020-12-21
Name/Print	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

GF Exhibit 1124 - 2641/2704

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
16/506,022	12/21/2020 05:37:10 PM ET	3771-0003-DC12

Title of Invention

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3561	FILED BY	Sarah Zizzo
PATENT CENTER #	60122492	AUTHORIZED BY	Tarek Fahmi
CUSTOMER #	27571	FILING DATE	07/09/2019
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Daniel E. Grupp

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 4028	E2020BKH37476010	Sarah Zizzo

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
2806	SUBMISSION OF AN INFORMATION DISCLOSURE STATEMENT	130.00	1	130.00
			TOTAL AMOUNT:	$130.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
16/506,022	**12/21/2020 05:37:10 PM ET**	**3771-0003-DC12**

Title of Invention

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3561	FILED BY	Sarah Zizzo
PATENT CENTER #	60122492	FILING DATE	07/09/2019
CUSTOMER #	27571	FIRST NAMED INVENTOR	Daniel E. Grupp
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Tarek Fahmi

Documents

TOTAL DOCUMENTS: 26

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
2020-12-21_3771-0003-DC12_R-OA.pdf	1	Amendment/Req. Reconsideration-After Non-Final Reject	87 KB
2020-12-21_3771-0003-DC12_IDS.pdf	6	Information Disclosure Statement (IDS) Form (SB08)	1011 KB
2020-07-23 Joint Claim Construction and Prehearing Statement.pdf	10	Non Patent Literature	154 KB
2020-07-23 Joint Claim Construction Exhibit A - Plaintiffs Proposed	9	Non Patent Literature	147 KB

Construction for Disputed Terms.pdf			
2020-07-23 Joint Claim Construction Exhibit B - Defendants Proposed Construction for Disputed Terms.pdf	8	Non Patent Literature	140 KB
2020-08-20 Revised Joint Claim Construction Ex A - Pltfs Proposed Constructions for Disputed Terms.pdf	7	Non Patent Literature	130 KB
2020-08-20 Revised Joint Claim Construction and Prehearing Statement.pdf	9	Non Patent Literature	157 KB
2020-08-20 Revised Joint Claim Construction Ex B - Defs Revised Proposed Constructions for Disputed Terms.pdf	7	Non Patent Literature	134 KB
2020-08-21 Pltfs Opening Claim Construction Brief.pdf	39	Non Patent Literature	516 KB
2020-09-04 Defendants Responsive Claim Construction Brief.pdf	33	Non Patent Literature	367 KB
2020-09-11 Acorns Reply Claim Construction Brief.pdf	17	Non Patent Literature	219 KB
2020-09-18 Joint Claim Construction Chart Appendices.pdf	12	Non Patent Literature	137 KB
2020-09-18 Joint Claim Construction Chart.pdf	20	Non Patent Literature	241 KB

2020-12-14 Piner Rebuttal Report.pdf	114	Non Patent Literature	867 KB
EDTX-2-19-cv-00347-85.pdf	40	Non Patent Literature	443 KB
EDTX-2-19-cv-00347-103.pdf	2	Non Patent Literature	234 KB
Exhibit A.pdf	36	Non Patent Literature	429 KB
Exhibit B.pdf	4	Non Patent Literature	86 KB
Exhibit C.pdf	38	Non Patent Literature	350 KB
Exhibit D.pdf	7	Non Patent Literature	106 KB
Exhibit E.pdf	16	Non Patent Literature	198 KB
Exhibit F.pdf	8	Non Patent Literature	145 KB
Exhibit G.pdf	8	Non Patent Literature	144 KB
Exhibit H.pdf	4	Non Patent Literature	61 KB
Expert Report of Dr Jeffry Bokor re Invalidity.pdf	254	Non Patent Literature	10353 KB
Order Adopting Claim Construction Recommendation.pdf	2	Non Patent Literature	230 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
2020-12-21_3771-0003-DC12_R-OA.pdf	64BE0B8CE8A60A4091F4BED9809BFA3E276B1FBCDCE6E6C96DA2361988D46B638CC31D2BBA7B06F2AB3DE64C0120E374FE9F52DB09BC6792CB148395604CF63B

2020-12-21_3771-0003-DC12_IDS.pdf	BEA53047DB7D20EC1AAEE01B190398C22A4EBED7AFB1F28EDC28BD8561C244D182BA2734855AA349274F533157254ED5CAD58EFDB8AAA7E96428FED4331F3198
2020-07-23 Joint Claim Construction and Prehearing Statement.pdf	6F4E946CA8A46BBA360C9F441ED2733A80FC4C3B1D35A9CA85E6A61EDEA5AE09ED0E8305990EB672B9EB8CC11488071BF66C081B0DA77CA337B3C7EC33836C26
2020-07-23 Joint Claim Construction Exhibit A - Plaintiffs Proposed Construction for Disputed Terms.pdf	8EBDAFF7C3E965C26BF8CCB5CF1C99CA7E789242CAEC05C4E9E3C061346CA6BB318934A8AE985DD441456EA70D039CDA1EE4D2039A8259C17AE7313970F8CA58
2020-07-23 Joint Claim Construction Exhibit B - Defendants Proposed Construction for Disputed Terms.pdf	1EE1874DDE7F82B85800B546CE91F9E7C04E35197D03A27118971842E7CF6404BEA7325FEB3349C7821DDFBF7CB3341376A7471F1ADE117581F0B1688DB6CF71
2020-08-20 Revised Joint Claim Construction Ex A - Pltfs Proposed Constructions for Disputed Terms.pdf	97FF44A7A8007A50779C33CD17EFE7BBD2206AC19D59B56B5E065A1E0A2FCCED06E091F517DD35CD030AC1DC9E4FC2DCB730DA1DB5B957F8C923DD68DA2979EA
2020-08-20 Revised Joint Claim Construction and Prehearing Statement.pdf	69A2FA2EB90E7B6051FDF546CB9BC9246F2EB36F487F27DCA33EE09E5A24FF751E0DEE3F667E2F4538EAACA09377FDD605CC4B8D99B0A79C5FBE42E280ABA8D3
2020-08-20 Revised Joint Claim Construction Ex B - Defs Revised Proposed Constructions for Disputed Terms.pdf	53AF43FDAFCD62A323F08E6BF10581F6C558895D75BD3EE98C7E5600AB4950294FC3963052B740F3A499B6335AB37D2E6033A95AB039978FDCAB044A8DF8FE78
2020-08-21 Pltfs Opening Claim Construction Brief.pdf	A412AF74CB5A0D0D3A4E89DDFC25AC4719E661378B75EF211BDD260465A7EF319CBD68F26ACAAF775681B3C8BA4B4481D349FDAFB569B2B4983721E8354D0A88
2020-09-04 Defendants Responsive Claim Construction Brief.pdf	868F1F1B53EFFC18069CEFE15B66DC6E6878147936FC946F8978317A992F5E6B8A67DD1EDB6BE91F3C9338A7816280DB414A373C2687C3417A2495FE1CCB8964

2020-09-11 Acorns Reply Claim Construction Brief.pdf	49B35929D7891A7DE5D394806347D9B3516F17637805E7643394C26C5A22052AFDC82802E4F0C58A7D28E29588B838F44E458DA734206469E88DDA24851CDB99
2020-09-18 Joint Claim Construction Chart Appendices.pdf	9FDEC7CCC3CFC59D97F3DDC9F54A1E8D44B239E0D030BF617A2DC00A1AD202F56DEB4FDF32E5801EDD6A0E2ADC37EC8E92936A1C191550F320D88D305593DB27
2020-09-18 Joint Claim Construction Chart.pdf	01F92CAB7BB52A9A2196370AC418F0B28390BAE3A336B5159C5A0DA1214250833E86CBF6B643DF984335A21A08B973864E38FC253B2EAECB0107CA6ADB7999A9
2020-12-14 Piner Rebuttal Report.pdf	924C9B77686757E00FA7AC61FF5FCF4738FD2015813127BA115BBE9F744F4E8A99BBA6F816DF32388E8001ED605EF3E135484C2C5344F1521386143A0FB4EC82
EDTX-2-19-cv-00347-85.pdf	45117B81F914EF82AA6BE2AD943A9E6F73464176D20AC57DC1EDFE15BE5079BB931988049501ACB4BBA0614BFB2E75439F4B42244EF29A418256D3EB1E96DE65
EDTX-2-19-cv-00347-103.pdf	5350756BACBEE18AC6C731313F1AD812229D064DE1B26CBC2DE9C417877C090D4FE37309D423B7EAB715AFD72DA03122463C4F2BDE2BCA027F95390BBF6EB93D
Exhibit A.pdf	35C8E44BE90149656E7B608F265A195F6956F40CB6E761F733278E328BBA590B46FA5BB0B157A7E8C62AEA32527A28178472BEF79D2197675C1E848C9C0FF015
Exhibit B.pdf	B7F5EE80971C53A303C0C643E425A2AF8E75A7B1CC51E3F379CF7F1EFF25288BAA6D741C558A31DE0DF69250D7FABBED97808A87C7DD12EB51626BF34898BB59
Exhibit C.pdf	5765EFF86E29CBB24B6CB6359EC5888399EB587400C1D24AA4340DE38120B683E8DC0024DB9B14A23F838DB111188A0061C84609747901051CE7F113439B0972
Exhibit D.pdf	EEFC2F3F8D8953381640535439B2A87ABF4242D47AB1C17CA94255DA4C10C69BAF88BDD2A0391B92E20BFEB87697163A6D81E0ED145A6973D8720EB3C5023124

Exhibit E.pdf	22BA94AEF5A1104CC7D474716AF1659D592865A18781A3C6D19C77FD7D262715EE80B4808772719576642000504749020DBFEE82F724F618BF473FD16AC5E2F0
Exhibit F.pdf	E14D29374ADA9F03771BBA14BC5A6A7392ADC61E9528D6D836222DC86CD29584FBD17E29C8DC5D0ECD14E1BAAFC464866BA46181E6AE21C69128499C883E0E68
Exhibit G.pdf	483BD5B5A258F85AB8034D2A0F023FA5A4F3D4920FE5A6A07FDEB7B8F8CC0D20BBB68B66DA36A4688AF1CB213DC62F06DF9934317BB19A972E21ED25B9DAF5D8
Exhibit H.pdf	EB6905903E8243AA12AFF10193B326847231CD8CA1450D51FCB6F6456881AF375A886627EFABA9CFF246C0F040E56CE10EAFE29201CFB0A74B8240D94E67C874
Expert Report of Dr Jeffry Bokor re Invalidity.pdf	1B75884B0931A0D0C383FE61620FB373D297AC78797CB7DD896C7B5977B9D998C14795E8C3EC7D4961DB44CC2EBC6FFCD721B146FBCEC2A259C38A0308E19D62
Order Adopting Claim Construction Recommendation.pdf	DC060FEE38ED6FFF6A5F575109F324CBD90995C7D8B56AF62CD6D974F5CB65C102062FDB9AF114DC14F82A5936BB07D082966E3F214FAE4E128562D6AB964841

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

27571 7590 02/10/2021

Ascenda Law Group, PC
2150 N First Street
Suite 420
San Jose, CA 95131

EXAMINER	
HARRISON, MONICA D	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/10/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/506,022	07/09/2019	Daniel E. Grupp	3771-0003-DC12	3561

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$500.00	$100	05/10/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

GF Exhibit 1124 - 2650/2704

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27571 7590 02/10/2021

Ascenda Law Group, PC
2150 N First Street
Suite 420
San Jose, CA 95131

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/506,022	07/09/2019	Daniel E. Grupp	3771-0003-DC12	3561

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$500.00	$100	05/10/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
HARRISON, MONICA D	2815	257-763000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

GF Exhibit 1124 - 2651/2704

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/506,022	07/09/2019	Daniel E. Grupp	3771-0003-DC12	3561

27571 7590 02/10/2021

Ascenda Law Group, PC
2150 N First Street
Suite 420
San Jose, CA 95131

EXAMINER	
HARRISON, MONICA D	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/10/2021

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

GF Exhibit 1124 - 2652/2704

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/506,022	Applicant(s) Grupp et al.	
	Examiner MONICA D HARRISON	Art Unit 2815	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 12/21/2020.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-20 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 12/21/2020.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MONICA D HARRISON/
Primary Examiner, Art Unit 2815

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

1. Applicant's remarks and terminal disclaimer filed 12/21/2020 have been entered and considered.

Terminal Disclaimer

2. The terminal disclaimer filed on 12/21/2020 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of **9,425,277 B2 and 9,905,691 B2 (Grupp et al)** has been reviewed and is accepted. The terminal disclaimer has been recorded.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 12/21/2020 was filed after the mailing date of the Non-Final rejection on 9/21/2020. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Allowable Subject Matter

4. Claims 1-20 are allowed over the prior art of record.

Reasons for Allowance

5. The following is an examiner's statement of reasons for allowance: After consideration of applicant's remarks, approval of applicant's terminal disclaimer and a further search of the

prior art of record, examiner has concluded that the prior art does not disclose nor fairly suggest the electrical junctions as described in independent claims 1 and 8.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MONICA D HARRISON whose telephone number is (571)272-1959. The examiner can normally be reached on M-F 7-4:30pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MONICA D HARRISON/
Primary Examiner, Art Unit 2815

mdh
January 29, 2021

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/506,022	Grupp et al.
	Examiner	Art Unit
	MONICA D HARRISON	2815

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/10/2019	12/18/2019	09/15/2020	01/29/2021					
1	1	✓	=	✓	=					
2	2		=	✓	=					
3	3		=	✓	=					
4	4		=	✓	=					
5	5		=	✓	=					
6	6		=	✓	=					
7	7		=	✓	=					
8	8		=	✓	=					
9	9		=	✓	=					
10	10		=	✓	=					
11	11		=	✓	=					
12	12		=	✓	=					
14	13		=	✓	=					
15	14		=	✓	=					
16	15		=	✓	=					
17	16		=	✓	=					
18	17		=	✓	=					
19	18		=	✓	=					
20	19		=	✓	=					
13	20		=	✓	=					

GF Exhibit 1124 - 2658/2704

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/506,022	Grupp et al.
	Examiner	Art Unit
	MONICA D HARRISON	2815

CPC - Searched*		
Symbol	**Date**	**Examiner**
H01L29/ 08,089,0895,16,160,1608,161,45,47,66,661,6614,66143,666,6664,6 6643,78,783,7839,785,80,806,81,812,87,872	09/10/2019	MDH
H01L21/28,285,2853,28537	09/10/2019	MDH
H01L29/45,456	09/15/2020	MDH

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
257	763	09/10/2019	MDH

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/MONICA D HARRISON/ Primary Examiner, Art Unit 2815	

GF Exhibit 1124 - 2659/2704

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/506,022	Grupp et al.
	Examiner	Art Unit
	MONICA D HARRISON	2815

Search Notes		
Search Notes	**Date**	**Examiner**
East (USPAT, US-PGPUB, USOCR, EPO, JPO, DERWENT, IBM_TDB, FPRS)	09/10/2019	MDH
East updated	12/18/2019	MDH
GRUPP ET AL .inv.	12/18/2019	MDH
ACORN SEMI .asn.	12/18/2019	MDH
USPAT, US-PGPUB txt .clm.	12/18/2019	MDH
East updated	09/15/2020	MDH
IPR2020-01182 Reviewed Petition for the Inter Partes Review of US. Patent No. 7,084,423 and Exhibits Ex.1001-Ex.1024	09/15/2020	MDH
IPR2-2020-1206 Reviewed Petition for the Inter Partes Review of US . Patent No. 9,905,691 and Exhibits Ex.1001-Ex.1035	09/15/2020	MDH
IPR2-2020-01279 Reviewed Petition for the Inter Partes Review of US. Patent No. 9,905,691 and Exhibits Ex.1101-Ex.1150	09/15/2020	MDH
East updated	01/29/2021	MDH
GRUPP ET AL .inv.	01/29/2021	MDH
ACORN SEMI .asn.	01/29/2021	MDH

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
	USPAT, US-PGPUB txt .clm.	12/18/2019	MDH
	USPAT, US-PGPUB txt .clm.	01/29/2021	MDH

/MONICA D HARRISON/ Primary Examiner, Art Unit 2815	

GF Exhibit 1124 - 2660/2704

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/506,022	Grupp et al.
	Examiner	**Art Unit**
	MONICA D HARRISON	2815

CPC						
Symbol					**Type**	**Version**
H01L	/	29	/	456	F	2013-01-01
H01L	/	29	/	0895	I	2013-01-01
H01L	/	29	/	16	I	2013-01-01
H01L	/	29	/	161	I	2013-01-01
H01L	/	29	/	1608	I	2013-01-01
H01L	/	29	/	45	I	2013-01-01
H01L	/	29	/	47	I	2013-01-01
H01L	/	29	/	66143	I	2013-01-01
H01L	/	29	/	66643	I	2013-01-01
H01L	/	29	/	78	I	2013-01-01
H01L	/	29	/	7839	I	2013-01-01
H01L	/	29	/	806	I	2013-01-01
H01L	/	29	/	812	I	2013-01-01
H01L	/	29	/	872	I	2013-01-01
H01L	/	21	/	28537	I	2013-01-01
H01L	/	29	/	785	A	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/MONICA D HARRISON/ Primary Examiner, Art Unit 2815	29 January 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	Fig. 6

U.S. Patent and Trademark Office — Part of Paper No.: 20210129

GF Exhibit 1124 - 2661/2704

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/506,022	Grupp et al.
	Examiner	**Art Unit**
	MONICA D HARRISON	2815

INTERNATIONAL CLASSIFICATION					
CLAIMED					
H01L	/	29	/	45	
H01L	/	21	/	28	

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
257	763

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/MONICA D HARRISON/ Primary Examiner, Art Unit 2815	29 January 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	Fig. 6

U.S. Patent and Trademark Office — Part of Paper No.: 20210129

GF Exhibit 1124 - 2662/2704

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/506,022	Grupp et al.
	Examiner	Art Unit
	MONICA D HARRISON	2815

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	10	10	20	19										
2	2	11	11	13	20										
3	3	12	12												
4	4	14	13												
5	5	15	14												
6	6	16	15												
7	7	17	16												
8	8	18	17												
9	9	19	18												

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/MONICA D HARRISON/ Primary Examiner, Art Unit 2815	29 January 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	Fig. 6

U.S. Patent and Trademark Office

Part of Paper No.: 20210129

GF Exhibit 1124 - 2663/2704

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4	"16506022"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/29 16:16
L2	11	257/763.ccls. and (electrical near junction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/29 16:18
L3	3	257/763.ccls. and (electrical near junction) and (source with (substrate wafer carrier base plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/29 16:18

L4	349	257/763.ccls. and (source with (substrate wafer carrier base plate)) and (metal contact electrode) with source	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/29 16:29
L5	14	257/763.ccls. and (source with (substrate wafer carrier base plate)) and (metal contact electrode) with source and (passivat$4 with source)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/29 16:30
L6	3	257/763.ccls. and (source with (substrate wafer carrier base plate)) and (metal contact electrode) with source and (passivat$4 with source) and (semiconductor near region) with (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/29 16:33
L7	0	257/763.ccls. and (source with (substrate wafer carrier base plate)) and (metal contact electrode) with source and (passivat$4 with source) and (semiconductor near region) with (substrate wafer carrier base plate) and (dangling near bond)	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2021/01/29 16:34

			JPO; DERWENT; IBM_TDB			
L8	0	257/763.ccls. and (source with (substrate wafer carrier base plate)) and (metal contact electrode) with source and (passivat$4 with source) and (semiconductor near region) with (substrate wafer carrier base plate) and (dang$4 near bond$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/29 16:35
L9	89	257/'$'.ccls. and (source with (substrate wafer carrier base plate)) and (metal contact electrode) with source and (passivat$4 with source) and (semiconductor near region) with (substrate wafer carrier base plate) and (dang$4 near bond$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/29 16:35
L10	6	257/'$'.ccls. and (source with (substrate wafer carrier base plate)) and (metal contact electrode) with source and (passivat$4 with source) and (semiconductor near region) with (substrate wafer carrier base plate) and (dang$4 near bond$4) and fermi	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/29 16:36
L11	10	H01L29/08,089,0895,16,1608,161,45,456,66,661,6614,66143,664,666,66643,78,783,7839,785,80,806,81,812,872.cpc. and (source with (substrate wafer carrier base plate)) and (metal contact electrode) with source and (passivat$4 with source) and	US-PGPUB; USPA	OR	ON	2021/01/29 16:39

		(semiconductor near region) with (substrate wafer carrier base plate) and (dang$4 near bond$4) and fermi	T; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L12	15	H01L29/'$'.cpc. and (source with (substrate wafer carrier base plate)) and (metal contact electrode) with source and (passivat$4 with source) and (semiconductor near region) with (substrate wafer carrier base plate) and (dang$4 near bond$4) and fermi	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/29 16:41
L13	8	H01L21/28,285,2853,28537.cpc. and (source with (substrate wafer carrier base plate)) and (metal contact electrode) with source and (passivat$4 with source) and (semiconductor near region) with (substrate wafer carrier base plate) and (dang$4 near bond$4) and fermi	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/29 16:48
L14	13	H01L21/'$'.cpc. and (source with (substrate wafer carrier base plate)) and (metal contact electrode) with source and (passivat$4 with source) and (semiconductor near region) with (substrate wafer carrier base plate) and (dang$4 near bond$4) and fermi	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2021/01/29 16:51

			IBM_TDB			
L15	17	(source with (substrate wafer carrier base plate)) and (metal contact electrode) with source and (passivat$4 with source) and (semiconductor near region) with (substrate wafer carrier base plate) and (dang$4 near bond$4) and fermi	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/29 16:53
L16	4	(source with (substrate wafer carrier base plate)) and (metal contact electrode) with source and (passivat$4 with source) and (semiconductor near region) with (substrate wafer carrier base plate) and (dang$4 near bond$4) and fermi and (grupp connelly).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/29 16:55
L17	2	(source with (substrate wafer carrier base plate)) and (metal contact electrode) with source and (passivat$4 with source) and (semiconductor near region) with (substrate wafer carrier base plate) and (dang$4 near bond$4) and fermi and acorn.asn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/29 16:56
S1	4	"16506022"	US-PGPUB; USPAT; USOCR;	OR	ON	2020/09/15 09:51

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S2	60	("20040129087" | "20060178015" | "20140117465" | "4304042" | "4691219" | "5614745" | "6323508" | "6521502" | "0000001" | "0000002" | "10090395" | "20050093027" | "2981877" | "3614548" | "3623925" | "3719797" | "3877054" | "3983264" | "4110488" | "4278830" | "4356622" | "4485265" | "4538342" | "4696828" | "4698652" | "4752815" | "4763176" | "4772934" | "4794444" | "4796082" | "4800415" | "4801984" | "4835580" | "4960732" | "4961194" | "6724088" | "7176483" | "9461167" | "9905691" | "3590471" | "3708360" | "3983574" | "4019113" | "4056642" | "4300152" | "4338616" | "4422090" | "4485550" | "4566021" | "4583110" | "4689869" | "4723197" | "4811077" | "4843029" | "4999685" | "5021365" | "5027166" | "5098859" | "5191322" | "5216262").PN.	US-PGPUB; USPAT	OR	OFF	2020/09/15 12:38
S3	7	("7084423" | "3983264").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 12:39
S4	2	("7084423" | "3983264").pn. and (substrate wafer carrier base plate) with semiconductor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 12:45
S5	2	("7084423" | "3983264").pn. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor	US-PGPUB;	OR	ON	2020/09/15 12:56

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S6	2	("7084423" | "3983264").pn. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 12:58
S7	2	("7084423" | "3983264").pn. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 13:10
S8	2	("7084423" | "3983264").pn. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2020/09/15 14:33

			IBM_TDB			
S9	1	("7084423" | "3983264").pn. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 14:40
S10	1	("7084423" | "3983264").pn. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4) and monolayer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 15:00
S11	60	("20040129087" | "20060178015" | "20140117465" | "4304042" | "4691219" | "5614745" | "6323508" | "6521502" | "0000001" | "0000002" | "10090395" | "20050093027" | "2981877" | "3614548" | "3623925" | "3719797" | "3877054" | "3983264" | "4110488" | "4278830" | "4356622" | "4485265" | "4538342" | "4696828" | "4698652" | "4752815" | "4763176" | "4772934" | "4794444" | "4796082" | "4800415" | "4801984" | "4835580" | "4960732" | "4961194" | "6724088" | "7176483" | "9461167" | "9905691" | "3590471" | "3708360" | "3983574" | "4019113" | "4056642" | "4300152" | "4338616" | "4422090" | "4485550" | "4566021" | "4583110" | "4689869" | "4723197" | "4811077" | "4843029" | "4999685" | "5021365" | "5027166" | "5098859" | "5191322" | "5216262").PN.	US-PGPUB; USPAT	OR	OFF	2020/09/15 15:08
S12	6	(substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4) and monolayer and S11	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2020/09/15 15:09

			EPO; JPO; DERWENT; IBM_TDB			
S13	0	257/763.ccls. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4) and monolayer and S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 15:47
S14	3	257/'$'.ccls. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4) and monolayer and S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 15:49
S15	1,551	H01L29/45,456.cpc. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 15:57
S16	119	H01L29/45,456.cpc. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric)	US-PGPUB;	OR	ON	2020/09/15 15:59

		with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4) and monolayer	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S17	119	H01L29/45,456.cpc. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4) and monolayer and transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 15:59
S18	93	H01L29/45,456.cpc. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4) and monolayer and (semiconductor near oxide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 16:00
S19	66	H01L29/45,456.cpc. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4) and monolayer and (semiconductor near oxide) and junction	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2020/09/15 16:09

			IBM_TDB			
S20	165	H01L29/08,089,0895,16,1608,161,45,456,66,661,6614,66143,664,666,66643,78,783,7839,785,80,806,81,812,872.cpc. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4) and monolayer and (semiconductor near oxide) and junction	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 16:10
S21	51	H01L21/28,285,2853,28537.cpc. and (substrate wafer carrier base plate) with semiconductor and (metal electrode conduct$4) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with semiconductor and (interface passivat$4 oxide insulat$4 dielctric) with (metal electrode conduct$4) and (metal near silicide) and (source drain) with (metal electrode conduct$4) and monolayer and (semiconductor near oxide) and junction	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 16:20
S22	14	"15728002"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 16:28
S23	12	"15251210"	US-PGPUB; USPAT; USOCR;	OR	ON	2020/09/15 16:38

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S24	18	"15048877"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 16:39
S25	4	"16847878"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 16:55
S26	2	"15506022"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 16:56

S27	14	"15728002"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 16:57
S28	12	"15251210"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 17:24
S29	18	"15048877"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 17:27
S30	22	"13552556"	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2020/09/15 17:33

			JPO; DERWENT; IBM_TDB			
S31	25	"13022522"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 17:34
S32	25	"12197996"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 17:35
S33	36	"11181217"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/15 17:35
S34	76	"10217758"	US-PGPUB; USPA	OR	ON	2020/09/15 17:36

			T; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L18	2	(source with (substrate wafer carrier base plate)) and (metal contact electrode) with source and (passivat$4 with source) and (semiconductor near region) with (substrate wafer carrier base plate) and (dang$4 near bond$4) and fermi.clm.	US-PGPUB; USPAT	OR	ON	2021/01/29 16:57

1/29/2021 5:50:08 PM
C:\Users\mharrison1\Documents\EAST\Workspaces\16506022.wsp

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16506022
Filing Date	2019-07-09
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.
Attorney Docket Number	3771-0003-DC12

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16506022
	Filing Date	2019-07-09
	First Named Inventor	Daniel E. Grupp
	Art Unit	2815
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC12

	1	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Joint Claim Construction and Prehearing Statement, 10 pgs. (Jul. 23, 2020).	
	2	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Ex. A to Joint Claim Construction and Prehearing Statement, 9 pgs. (Jul. 23, 2020).	
	3	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Ex. B to Joint Claim Construction and Prehearing Statement, 8 pgs. (Jul. 23, 2020).	
	4	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Revised Joint Claim Construction and Prehearing Statement, 9 pgs. (Aug. 20, 2020).	
	5	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Ex. A to Revised Joint Claim Construction and Prehearing Statement, 7 pgs. (Aug. 20, 2020).	
	6	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Ex. B to Revised Joint Claim Construction and Prehearing Statement, 7 pgs. (Aug. 20, 2020).	
	7	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Plaintiff's Opening Claim Construction Brief, 39 pgs. (Aug. 21, 2020).	
	8	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Defendant's Responsive Claim Construction Brief, 33 pgs. (Sep. 4, 2020).	
	9	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Plaintiff's Reply Claim Construction Brief, 17 pgs. (Sep. 11, 2020).	
	10	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Joint Claim Construction Chart, 20 pgs. (Sep. 18, 2020).	
	11	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Joint Claim Construction Chart Appendices, 12 pgs. (Aug. 21, 2020).	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	16506022
Filing Date	2019-07-09
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.
Attorney Docket Number	3771-0003-DC12

	12	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Construction Memorandum Opinion and Order, 40 pgs. (Oct. 16, 2020).	
	13	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Order Correcting Typographical Error in Claim Construction Memorandum Opinion and Order, 2 pgs. (Nov. 18, 2020).	
	14	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Order of Judge R. Gilstrap Adopting Claim Construction Memorandum Opinion and Order, 2 pgs. (Dec. 10, 2020).	
	15	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Expert Report of Dr. Jeffrey Bokor Regarding Invalidity of U.S. Patent No. 7,084,423, U.S. Patent No. 8,766,336, U.S. Patent No. 9,209,261, U.S. Patent No. 9,461,167, U.S. Patent No. 9,905,691, and U.S. Patent No. 10,090,395 (Redacted) (Nov. 16, 2020).	
	16	Exhibit A to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), CV of Dr. Jeffrey Boker, 36 pgs. (Nov. 16, 2020).	
	17	Exhibit B to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Materials Considered in Connection with Report, 4 pgs. (Nov. 16, 2020).	
	18	Exhibit C to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipation of '336 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Patent 7,176,483, 38 pgs. (Nov. 16, 2020).	
	19	Exhibit D to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipation of '261 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Patent 7,176,483, 7 pgs. (Nov. 16, 2020).	
	20	Exhibit E to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipation of '167 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Patent 7,176,483, 16 pgs. (Nov. 16, 2020).	
	21	Exhibit F to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipation of '691 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Patent 7,176,483, 8 pgs. (Nov. 16, 2020).	
	22	Exhibit G to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipated of '395 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Patent 7,176,483, 8 pgs. (Nov. 16, 2020).	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16506022
	Filing Date	2019-07-09
	First Named Inventor	Daniel E. Grupp
	Art Unit	2815
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC12

	23	Exhibit H to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), List of Claims by Grouping, 4 pgs. (Nov. 16, 2020).
	24	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Rebuttal Expert Report of Edwin Piner, Ph.D. (Redacted) (Dec. 14, 2020).

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/MONICA D HARRISON/	Date Considered	01/29/2021

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16506022
Filing Date	2019-07-09
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.
Attorney Docket Number	3771-0003-DC12

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2020-12-21
Name/Print	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

Document Description: Issue Fee Payment (PTO-85B)

OPAP AKIMA-8 MAY 07 2021 PATENT & TRADEMARK OFFICE

Issue Fee Transmittal Form

Application Number	Filing Date	First Named Inventor	Atty. Docket No.	Confirmation No.
16506022	09-Jul-2019	Daniel Grupp	3771-0003-DC12	3561

TITLE OF INVENTION:

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Entity Status	Application Type	Art Unit	Class - Subclass	EXAMINER
Small	Utility under 35 USC 111(a)	2815	763000	MONICA HARRISON

Issue Fee Due	Publication Due	Total Fee(s) Due	Date Due	Prev. Paid Fee
$600	$0	$600	10-May-2021	$500

1.Change of Correspondence Address and/or Indication Of Fee Address (37 CFR 1.33 & 1.363)

Current Correspondence Address:	Current Indicated Fee Address:
27571 Ascenda Law Group, PC 2150 N First Street Suite 420 San Jose CA 95131 UNITED STATES 408-799-0612 patents@ascendalaw.com	
☐ Change of correspondence address requested, system generated AIA/122-EFS form attached	☐ Fee Address indication requested, system generated SB/47-EFS form attached

2.Entity Status

Change in Entity Status

○ Applicant certifying micro entity status; system generated Micro Entity certification form attached. See 37 CFR 1.29.
Note: Absent a valid certification of micro entity status, issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment. If this box is checked, you will be prompted to choose a micro entity status on the gross income basis (37 CFR 1.29(a)) or the institution of higher education basis (37 CFR 1.29(d)), and make the applicable certification online.

◉ Applicant asserting small entity status. See 37 CFR 1.27.
Note: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

○ Applicant changing to regular undiscounted fee status.
Note: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

GF Exhibit 1124 - 2685/2704

Document Description: Issue Fee Payment (PTO-85B)

3.The Following Fee(s) Are Submitted:

☐ Issue Fee	☐ I authorize USPTO to apply my previously paid issue fee to the current fees due
☐ Publication Fee	☒ The Director is hereby authorized to apply my previously paid issue fee to the current fee due and to charge deficient fees to Deposit Account Number 505798
☐ Advance Order - # of copies _____	☐ If **in addition to** the payment of the issue fee amount submitted with this form, there are any discrepancies in any amount(s) due, the Director is authorized to charge any deficiency, or credit any overpayment, to Deposit Account Number _____ . The **issue fee must be submitted** with this form. **If payment of the issue fee does not accompany this form, checking this box and providing a deposit account number will NOT be effective to satisfy full payment of the fee(s) due.**

4.Firm and/or Attorney Names To Be Printed

NOTE: If no name is listed, no name will be printed
For printing on the patent front page, list to be displayed as entered

1. Ascenda Law Group, PC
2.
3.

5.Assignee Name(s) and Residence Data To Be Printed

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

Name	City	State	Country	Category
Acorn Semi, LLC	Palo Alto	CALIFORNIA	united states	other

6.Signature

I certify, in accordance with 37 CFR 1.4(d)(4) that I am an attorney or agent registered to practice before the Patent and Trademark Office who has filed and has been granted power of attorney in this application. I also certify that this Fee(s) Transmittal form is being transmitted to the USPTO via EFS-WEB on the date indicated below.

Signature	/Tarek N. Fahmi/	**Date**	05-07-2021
Name	Tarek N. Fahmi	**Registration Number**	41402

Document Description: Issue Fee Payment (PTO-85B)

Issue Fee Transmittal Form

Application Number	Filing Date	First Named Inventor	Atty. Docket No.	Confirmation No.
16506022	09-Jul-2019	Daniel Grupp	3771-0003-DC12	3561

TITLE OF INVENTION :

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Entity Status	Application Type	Art Unit	Class - Subclass	EXAMINER
Small	Utility under 35 USC 111(a)	2815	763000	MONICA HARRISON

Issue Fee Due	Publication Due	Total Fee(s) Due	Date Due	Prev. Paid Fee
$600	$0	$600	10-May-2021	$500

1.Change of Correspondence Address and/or Indication Of Fee Address (37 CFR 1.33 & 1.363)

Current Correspondence Address:	Current Indicated Fee Address :
27571 Ascenda Law Group, PC 2150 N First Street Suite 420 San Jose CA 95131 UNITED STATES 408-799-0612 patents@ascendalaw.com	
☐ Change of correspondence address requested, system generated AIA/122-EFS form attached	☐ Fee Address indication requested, system generated SB/47-EFS form attached

2.Entity Status

Change in Entity Status

○ Applicant certifying micro entity status; system generated Micro Entity certification form attached. See 37 CFR 1.29.
Note: Absent a valid certification of micro entity status, issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment. If this box is checked, you will be prompted to choose a micro entity status on the gross income basis (37 CFR 1.29(a)) or the institution of higher education basis (37 CFR 1.29(d)), and make the applicable certification online.

◉ Applicant asserting small entity status. See 37 CFR 1.27.
Note: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

○ Applicant changing to regular undiscounted fee status.
Note: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

GF Exhibit 1124 - 2687/2704

Doc Code: IFEE PTOL/85B-EFS

Document Description: Issue Fee Payment (PTO-85B)

3.The Following Fee(s) Are Submitted:

☐ Issue Fee

☐ I authorize USPTO to apply my previously paid issue fee to the current fees due

☐ Publication Fee

☒ The Director is hereby authorized to apply my previously paid issue fee to the current fee due and to charge deficient fees to Deposit Account Number 505798

☐ Advance Order - # of copies _____

☐ If **in addition to** the payment of the issue fee amount submitted with this form, there are any discrepancies in any amount(s) due, the Director is authorized to charge any deficiency, or credit any overpayment, to Deposit Account Number _____ . The **issue fee must be submitted** with this form. **If payment of the issue fee does not accompany this form, checking this box and providing a deposit account number will NOT be effective to satisfy full payment of the fee(s) due.**

4.Firm and/or Attorney Names To Be Printed

NOTE: If no name is listed, no name will be printed
For printing on the patent front page, list to be displayed as entered

1. Ascenda Law Group, PC
2.
3.

5.Assignee Name(s) and Residence Data To Be Printed

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

Name	City	State	Country	Category
Acorn Semi, LLC	Palo Alto	CALIFORNIA	united states	other

6.Signature

I certify, in accordance with 37 CFR 1.4(d)(4) that I am an attorney or agent registered to practice before the Patent and Trademark Office who has filed and has been granted power of attorney in this application. I also certify that this Fee(s) Transmittal form is being transmitted to the USPTO via EFS-WEB on the date indicated below.

Signature	/Tarek N. Fahmi/	**Date**	05-07-2021
Name	Tarek N. Fahmi	**Registration Number**	41402

GF Exhibit 1124 - 2688/2704

Electronic Acknowledgement Receipt

EFS ID:	42664338
Application Number:	16506022
International Application Number:	
Confirmation Number:	3561
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC12
Receipt Date:	07-MAY-2021
Filing Date:	09-JUL-2019
Time Stamp:	12:28:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Web85b.pdf	46018 c77c718068af446670b76c00008f825341f9ae5f	no	2

Warnings:

Information:	
Total Files Size (in bytes):	46018

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

United States Patent and Trademark Office

Office of the Chief Financial Officer

Document Code:WFEE

User :C46472

Sale Accounting Date:05/10/2021

Sale Item Reference Number	Effective Date
16506022	05/07/2021

Document Number	Fee Code	Fee Code Description	Amount Paid	Payment Method
I202150856272181	2501	UTILITY APPL ISSUE FEE	$500.00	Salea
I202150856272181	2501	UTILITY APPL ISSUE FEE	$100.00	Deposit Account

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/506,022	07/06/2021	11056569	3771-0003-DC12	3561

27571 7590 06/16/2021

Ascenda Law Group, PC
2150 N First Street
Suite 420
San Jose, CA 95131

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Acorn Semi, LLC, Palo Alto, CA;
Daniel E. Grupp, Palo Alto, CA;
Daniel J. Connelly, Redwood City, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

GF Exhibit 1124 - 2692/2704

REVOCATION OF PREVIOUS POWERS OF ATTORNEY WITH NEW GENERAL POWER OF ATTORNEY TO PROSECUTE APPLICATIONS AND REEXAMINATION PROCEEDINGS BEFORE THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby revoke all previous powers of attorney given in the application(s), reexamination proceeding(s) and/or patent(s) listed below and appoint:

	Practitioners associated with the Customer Number	27571	

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications and reexamination proceedings assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73.

Please change the correspondence address for the application(s), reexamination proceeding(s) and/or patent(s) listed below to the address associated with Customer Number 27571.

Assignee Name and Address:

Oak IP, LLC
812 West McDermott Dr. #1026
Allen, TX 75013

A statement under 37 CFR 3.73 is attached.

List of application(s), reexamination proceeding(s) and/or patent(s):

See Attached List

SIGNATURE OF ASSIGNEE OF RECORD
The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date: 12/27/24
Name	David Pridham	Telephone: 214-414-1164
Title	CEO	

Patent Number	Title	Issue Date
US-7084423-B2	Method for depinning the Fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	08/01/2006
US-7462860-B2	Method for depinning the Fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	12/09/2008
US-7884003-B2	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	02/08/2011
US-8431469-B2	Method for depinning the Fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	04/30/2013
US-9209261-B2	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	12/08/2015
US-9425277-B2	Method for depinning the Fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	08/23/2016
US-9812542-B2	Method for depinning the Fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	11/07/2017
US-10186592-B2	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	01/22/2019
US-10388748-B2	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	08/20/2019
US-11355613-B2	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	06/07/2022
US-10937880-B2	Method for depinning the Fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	03/02/2021
US-10950707-B2	Method for depinning the Fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	03/16/2021
US-11018237-B2	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	05/25/2021
US-11056569-B2	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	07/06/2021
US-8766336-B2	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	07/01/2014
US-9461167-B2	Method for depinning the Fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	10/04/2016

GF Exhibit 1124 - 2694/2704

Patent Number	Title	Issue Date
US-9905691-B2	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	02/27/2018
US-10090395-B2	Method for depinning the Fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	10/02/2018
US-6833556-B2	Insulated gate field effect transistor having passivated schottky barriers to the channel	12/21/2004
US-7112478-B2	Insulated gate field effect transistor having passivated Schottky barriers to the channel	09/26/2006
US-7883980-B2	Insulated gate field effect transistor having passivated schottky barriers to the channel	02/08/2011
US-8377767-B2	Insulated gate field effect transistor having passivated schottky barriers to the channel	02/19/2013
US-8916437-B2	Insulated gate field effect transistor having passivated schottky barriers to the channel	12/23/2014
US-9583614-B2	Insulated gate field effect transistor having passivated schottky barriers to the channel	02/28/2017
US-11043571-B2	Insulated gate field effect transistor having passivated schottky barriers to the channel	06/22/2021
US-6891234-B1	Transistor with workfunction-induced charge layer	05/10/2005
US-7382021-B2	Insulated gate field-effect transistor having III-VI source/drain layer(s)	06/03/2008
US-7176483-B2	Method for depinning the Fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	02/13/2007
US-7902029-B2	Process for fabricating a self-aligned deposited source/drain insulated gate field-effect transistor	03/08/2011
US-8263467-B2	Process for fabricating a self-aligned deposited source/drain insulated gate field-effect transistor	09/11/2012
US-8212336-B2	Field effect transistor source or drain with a multi- facet surface	07/03/2012
US-9620611-B1	MIS contact structure with metal oxide conductor	04/11/2017
US-10147798-B2	MIS contact structure with metal oxide conductor	12/04/2018

GF Exhibit 1124 - 2695/2704

Patent Number	Title	Issue Date
US-10553695-B2	MIS contact structure with metal oxide conductor	02/04/2020
US-10872964-B2	MIS contact structure with metal oxide conductor	12/22/2020
US-11843040-B2	MIS contact structure with metal oxide conductor	12/12/2023

GF Exhibit 1124 - 2696/2704

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
16/506,022	**01/10/2025 05:07:46 PM Z ET**	**3771-0003-DC12**

Title of Invention

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	11056569
CONFIRMATION #	3561	FILED BY	SARAH ZIZZO
PATENT CENTER #	68691997	FILING DATE	07/09/2019
CUSTOMER #	27571	FIRST NAMED INVENTOR	Daniel E. Grupp
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Tarek Fahmi

Documents

TOTAL DOCUMENTS: 3

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
Oak_IP_LLC_Exe_POA.pdf	4	Power of Attorney	258 KB
16506022_Statement_3-73c.pdf	3	Assignee showing of ownership per 37 CFR 3.73	118 KB
16506022_ADS_Acorn-Semi.pdf	2	Application Data Sheet	137 KB

Warning: This is not a USPTO supplied ADS fillable form. Data in the form cannot be automatically loaded to other USPTO systems.

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)

Oak_IP_LLC_Exe_POA.pdf	EB6526859CF929C3D04F15E92BD8DC1D4154F6AAFCF6F4BD08692FDA0C79D61A0524084B92C1C8911741CAD66222687A929690F36A553B7ED3CD75DF8D353B3E
16506022_Statement_3-73c.pdf	80A72FF856E78D35064209E8D09DA0EFAD9F44C8EF2AA952A2FA0B601B943E8155349899AA8B4BE650D9277050BBF4935C0EC8877D7511159A20E3EF62B322C3
16506022_ADS_Acorn-Semi.pdf	8935F922F565B910F41F35BADC92D294CDFA9DF2C525188B2ABCBCA3ED6094E9D958FEBE76A5D4A5D4F89E1D6CF9071031FF1ABA8F95DED959DA037AF4B76C91

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: OAK IP, LLC

Application No./Patent No.: 11,056,569 Filed/Issue Date: 07/06/2021

Titled: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

OAK IP, LLC, a company

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: GRUPP, DANIEL E.; et al. To: ACORN TECHNOLOGIES, INC.

   The document was recorded in the United States Patent and Trademark Office at Reel 053773, Frame 0225, or for which a copy thereof is attached.

2. From: ACORN TECHNOLOGIES, INC. To: ACORN SEMI, LLC

   The document was recorded in the United States Patent and Trademark Office at Reel 053773, Frame 0306, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: ACORN SEMI, LLC To: OAK IP, LLC

The document was recorded in the United States Patent and Trademark Office at
Reel 069681, Frame 0837, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Tarek N. Fahmi/	2025-01-10
Signature	Date
Tarek N. Fahmi	41402
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/14 (01-22)
Approved for use through 05/31/2024. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3771-0003-DC12
	Application Number	16/506,022
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

(●) Assignee	( ) Legal Representative under 35 U.S.C. 117	( ) Joint Inventor
( ) Person to whom the inventor is obligated to assign.	( ) Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	~~Acorn Semi, LLC~~ Oak iP, LLC		
Mailing Address Information For Applicant:			
Address 1	~~455 Cambridge Ave.~~ 812 West McDermott Dr. #1026		
Address 2			
City	~~Palo Alto~~ Allen	**State/Province**	~~CA~~ TX
Country US		Postal Code	~~94306~~ 75013
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

GF Exhibit 1124 - 2702/2704

PTO/AIA/14 (01-22)
Approved for use through 05/31/2024. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3771-0003-DC12
	Application Number	16/506,022
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Tarek N. Fahmi/			Date (YYYY-MM-DD)	2025-01-10
First Name	Tarek	Last Name	Fahmi	Registration Number	41402

Additional Signature may be generated within this form by selecting the Add button.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/506,022	07/09/2019	Daniel E. Grupp	3771-0003-DC12

CONFIRMATION NO. 3561

27571
Ascenda Law Group, PC
2150 N First Street
Suite 420
San Jose, CA 95131

POA ACCEPTANCE LETTER

DC00000008342562B

Date Mailed: 01/29/2025

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/10/2025.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/atesfai/

GF Exhibit 1124 - 2704/2704